



## ABSTRACT

Title of dissertation:           HIGH-IMPEDANCE ELECTROMAGNETIC SURFACES  
  FOR MITIGATION OF SWITCHING NOISE IN HIGH-  
  SPEED CIRCUITS

Telesphor Kamgaing, Doctor of Philosophy, 2003

Dissertation directed by:       Professor Omar M. Ramahi  
  Mechanical Engineering Department,  
  Electrical and Computer Engineering Department

With the increasing gate density, the rising clock frequency, printed circuit board (PCB) level simultaneous switching noise (SSN) has become a major bottleneck for the signal integrity in high-speed microprocessors and computers. All approaches that are currently being used to address this problem have been proven inefficient for switching frequencies of 500 MHz and above. The research work carried out in this dissertation addresses a novel technique for mitigating high-frequency SSN by suppressing the natural parallel-plate resonant modes encountered in traditional power planes. This is done by replacing at least one of the power planes of the power distribution network with a high-

impedance electromagnetic surface (HIS). The high-impedance electromagnetic surface, which indeed is an artificial magnetic conductor, prevents any surface wave propagation in its forbidden band-gap, therefore leading to the suppression of resonant modes. Using full wave electromagnetic simulation and experimental verification, the fundamental limitations of SSN mitigation using standard HIS is investigated. It is found that the thickness of the dielectric substrate and the metal line spacing offered by most PCB technologies are fundamental limitations for achieving broadband simultaneous switching noise mitigation at frequencies below 3 GHz for high-density packaging. This restriction is addressed by developing a new family of HIS, whose surface impedance is mainly controlled by the inductance density. These novel inductively-tuned HIS offer the possibility of mitigating switching noise at frequencies of 1 GHz and below frequencies and can be fabricated using conventional PCB technology. It is also demonstrated that the combination of these novel HIS with RC dissipative edge termination (DET) leads to broadband simultaneous switching noise mitigation from DC to about 3 or 4 GHz. Finally physics-based compact models that allow the use of the novel power planes with other components for full package simulation are developed and validated for power planes with integrated standard and double-layer HIS. These models utilize only frequency independent lumped-components and are, therefore, particularly attractive for transient analysis.

HIGH-IMPEDANCE ELECTROMAGNETIC  
SURFACES FOR MITIGATION OF SWITCHING  
NOISE IN HIGH-SPEED CIRCUITS

by

Telesphor Kamgaing

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Advisory Committee:

Professor Omar Ramahi, Chair  
Professor Amr Baz  
Professor Victor Granatstein  
Professor Isaak Mayergoyz  
Professor Robert Newcomb

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2003

## DEDICATION

To my family and especially my wife Clarisse

To the memories of my father Tchegho and my mother Odette Youogo

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The road to the completion of this work has been very long. The path has been rough at certain times. The landscape has gone from the beautiful spring vegetation to the dormant trees of the winter. The temperatures have varied throughout all possible levels on the thermometer. BUT at any time, there has always been someone, one of you out there, to help me maintain my focus, to help me concentrate on the most important thing. Only your constant support and God's grace have guided me safely through the hard road and made sure that I don't get too much distracted by the beautiful flowers of the spring either.

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# Chapter 1

## Objective of the dissertation and background

### 1.1 Introduction

#### 1.1.1 Motivation

With the continuous downscaling of MOSFETs, the increasing gate density and the increasing clock frequency in modern microprocessors, simultaneous switching noise (SSN) has become a major concern. When many active devices switch at the same time, the switching noise generated can cause fluctuations or disturbances in the power distribution system, which in turn leads to a degradation of the signal integrity [1], [2], [3]. This problem of SSN, also known as delta-I noise or power/ground plane bounce, has been discussed intensively over the last decade and different approaches have been taken to mitigate it. In printed circuit board (PCB) technology, the most common approach for mitigating SSN consists of using discrete decoupling capacitors around sensitive integrated circuits [4]-[9], whereby most of the recent work has been focused on optimizing the number and the location of these capacitors on the PCB. These capacitors are usually connected between the power and ground planes and are expected to behave as a short circuit between the two planes at high frequencies. It has been found, however, that the lead inductance of these real capacitors strongly limits their noise mitigation capability [10]. In fact, with its parasitic inductance, real capacitors used today in PCBs act as a series LC resonant circuit for frequencies beyond a few hundred megahertz. In fact, the capacitor

becomes a short circuit only around its self-resonant frequency, and acts as an open circuit at all other frequencies. An alternative to the discrete capacitors is embedded capacitance, which is obtained by strongly reducing the separation between the two power planes [11], [12], [13]. Embedded capacitance shows slightly better high frequency performance because of the absence of lead inductance. Most limitation to this methodology is given by the costs associated with new technology development. At this point there is practically no solution that addresses the noise mitigation in power planes at high frequencies. The question that remains unanswered is if there are alternative or complementary solutions to decoupling capacitors.

Frequency selective surfaces have been around for several years. Until most recently they have been regarded by the US government as a classified area of research because of their importance in military applications [14]. One important class of frequency selective surfaces are electromagnetic band-gap structures, which have the property of suppressing surface wave propagation at microwave frequencies. Recently Sievenpiper introduced a new class of periodic structures called high-impedance electromagnetic surfaces (HIS) [15], which stop surface wave propagation in designated frequency bands called band-gaps. These structures, which are very similar to electromagnetic band-gap structures, have been proven very efficient in suppressing surface waves. Their applications include their use as ground planes for high-efficiency antennas [15], [16], [17] and also as walls for rectangular waveguides [18]. The most pertinent question that is being asked here is whether such structures can also be used as a replacement for the ground-plane in the power distribution network of high-speed digital systems, where ground-bounce is an issue.

One specific requirement for such applications is the ability to design high-impedance surfaces to have their forbidden band-gap in the frequency range, where SSN is pronounced in the circuit. In addition, it has to be taken into account that many components do not switch simultaneously, which leads to a requirement of HIS with wide forbidden band-gap at the frequencies of interest.

The research question this dissertation addresses is: **Can high-impedance electromagnetic surfaces be used for resonance mitigation in parallel-plate waveguides in general, and in power planes of high-speed digital circuits in particular?**

### *1.1.2 Contribution of this work*

Simultaneous switching noise (SSN) mitigation through the suppression of natural resonances in parallel-plate power planes of high-speed circuits is addressed in this dissertation. The main contributions of this work are:

- A novel concept is introduced for mitigating switching noise in power distribution networks of high-speed circuits. This novel concept consists of replacing the ground plane of a traditional power plane pair with a high-impedance electromagnetic surface. Effective noise mitigation occurs in the frequency range, where the high-impedance surface has its forbidden band-gap. Details on this concept are discussed in chapter 2.
- The concept of designing high-impedance surfaces with forbidden band-gap at very low frequencies by enhancing the inductance per unit area is introduced. Contrary to the enhancement of the per unit area capacitance, an enhancement of the inductance density

leads to simultaneous decrease of the self-resonance frequency and an increase of the fractional bandwidth, therefore allowing broadband designs at low frequencies.

- A method is introduced for designing double-layer inductance-enhanced high-impedance electromagnetic surfaces. In this novel design, the straight via of the standard HIS unit cell is replaced by an inductance-enhanced element, consisting of two vias and a single-loop or a multi-turn spiral inductor. This type of structures applied in a power plane configuration offers noise mitigation below 1 GHz for structures with lattice constant of 10 mm. This contribution is discussed in section 3.2.1.
- It is demonstrated in section 3.2.2 that broadband noise mitigation can be achieved by combining RC dissipative edge termination (DET) with inductance-enhanced high-impedance electromagnetic surfaces. Using a combination of HIS and RC DET as example, noise mitigation from DC to 4 GHz is achieved on a 10 cm x 10 cm power plane.
- Two novel single-layer inductance-enhanced HIS topologies are introduced and discussed in section 3.3.1 and 3.3.2. The fundamental idea behind these structures consists of increasing the inductance per unit cell by appropriate patterning of the patch of the standard HIS cell. It is demonstrated that both HIS using a cross embedded in the patch and HIS using a closed-loop spiral inductor as patch can mitigate noise at much lower frequency band-gap than standard HIS with similar periodicity and patch spacing, when used in power planes.
- A novel type of single-layer high-impedance electromagnetic surfaces using an open-loop spiral inductor as patch is introduced in section 3.3.3. and thoroughly investigated in section 3.4. It is shown that this type of structures exhibits two very close

frequency band-gaps that can be adjusted (or tuned) independently. This type of structures offers the possibility for multi-band noise mitigation.

- Physics-based lumped-element compact models for HIS in power plane configuration are developed in chapter 4. The model is based on the development of a compact model for single unit cell, several of whom can be connected into a two-dimensional array to build the full model for the periodic power planes. The model is validated on power planes with integrated standard and inductance-enhanced HIS.

### *1.1.3 Organization of the dissertation*

The rest of this chapter covers the general background of the thesis which includes the problem of simultaneous switching noise in high-speed systems, the propagation of surface waves in “empty” and periodically loaded parallel-plate waveguides and the general characterization of periodic structures. Chapter 2 introduces the concept of power planes with integrated high-impedance surfaces. Fundamental limits of power planes using HIS with the standard HIS are analyzed using dispersion diagrams as well as simulated and measured S-parameters. The concept of power planes with nested HIS is also introduced and investigated. Power planes using inductively tuned high-impedance surfaces are studied in chapter 3. The various structures introduced offers significant size advantage for low frequency design and can be designed for single or multiple band simultaneous switching noise mitigation. Chapter 4 discusses the development of compact models for the HIS in power plane environments and shows how they can be used for a fast analysis of

the power plane and also for the optimization of the dissipative edge termination in achieving broadband noise mitigation.

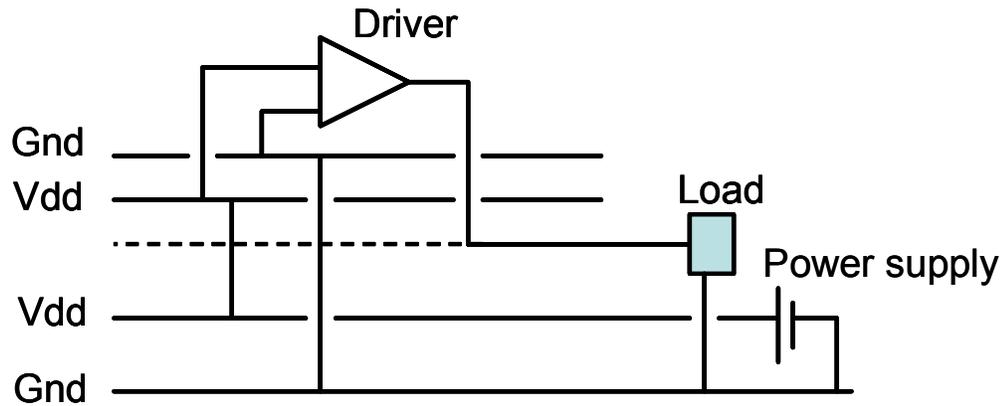


Figure 1-1: General configuration of a simultaneous switching noise environment for a multilayer board.

## 1.2 Simultaneous switching noise in high-speed systems

Today's computer systems and microprocessors utilize multilayer printed circuit boards (PCBs). These PCBs, which are made out of multiple metal layers separated by dielectric substrate, provide both a packaging functionality and a power distribution network for the components. As illustrated in Figure 1-1, the power distribution network is usually distributed on several metal layers, whereby the minimum requirement is to have at least two layers: one for the supply voltage  $V_{dd}$  and the other for the reference voltage or ground (Gnd). These power supply layers usually extend over the entire width and length of the PCB and are often referred to as power planes. Typically the output drivers are made out of active devices or gates, which are all part of a microprocessor or of a high-speed

integrated circuit (IC). These ICs are mounted on the surface of the PCB and connected to the different layers using wire bonds, bond pads and vias.

Simultaneous switching noise occurs, when the simultaneous switching of many of these internal gates causes a voltage glitch in the power distribution network. Since the output drivers have to drive both the load and board parasitics, the rate of change in the output drivers switching current can become greater than the rate of change in the switching current in the internal gates. Traditionally the voltage drop or the current surge has been inferred to the inductive nature of the board parasitics. In fact the chip interconnects (wire bonds and bond pads), the via and the power can be modeled as an effective inductance  $L$ , that together with the load and the output driver build a closed loop. When a time varying current  $i$  flows through the conductive path (of the closed loop), an electromagnetic flux  $\phi$  is generated within the loop. The effective self-inductance  $L$  of the loop is then given by (1.1) as

$$L = \frac{\phi}{i} \quad (1.1).$$

The associated induced voltage is obtained from Faraday's law as (1.2)

$$V = \frac{d\phi}{dt} \quad (1.2)$$

The combination of (1.1) and (1.2) gives (1.3), which is the noise voltage or effective variation in voltage, when a single gate switches.

$$V = L \frac{di}{dt} \quad (1.3)$$

In equation (1.3),  $V$  can be either positive or negative. It is often referred to as delta-I noise because of its direct dependence on the rate of change in current or as ground-bounce because the voltage glitch corresponds to an effective change of the supply voltage and can therefore be seen as a displacement of the ground level.

Initial work on the estimation of simultaneous switching noise was carried out by [19] and suggested that at a given time the total simultaneous switching noise can be obtained by multiplying (1.3) by the number of gates switching with the same  $di/dt$ . In [20] it was shown, however, that the total simultaneous switching noise saturates with the number of gates and that an accurate determination of the board effective inductance was critical in modeling the SSN.

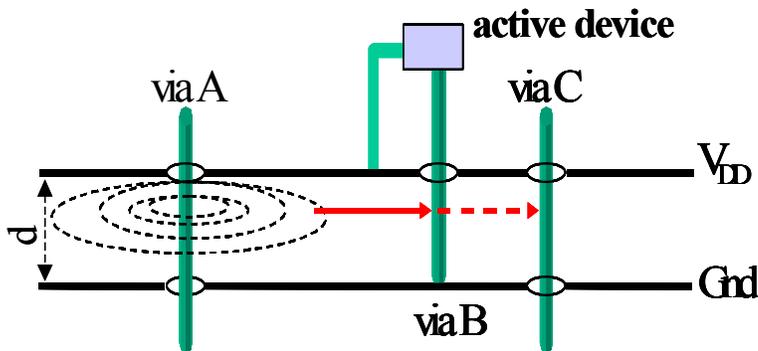


Figure 1-2: Simplified simultaneous switching noise environment (2-layer board).

### 1.3 High frequency simultaneous switching noise

As the clock frequency increases above one GHz, the problem of simultaneous switching noise becomes even more complex. From equation (1.3), it can be seen that the

rate of change of the current, which can also be related to the switching speed is very important in determining the switching noise. As illustrated in Figure 1-2 for the two-layer power plane system, when the active device switches, not only does a sudden change in current consumption occur at that location, but one or more modes are excited, and propagate radially as voltage waves between the two power planes, which by themselves constitute a parallel-plate waveguide. When these voltage waves make contact with vias connected to other gates, they will directly disturb the power supply or voltage level of these gates [21]. This could in turn lead to a false logic or signal integrity issue: For example a gate switching from a logic 0 to a logic 1 could be read 0, when there is a strong negative surge in the voltage, or a gate switching from a logic 1 to a logic 0 could be read incorrectly if there is a strong positive surge in the voltage. It is well known that high-frequency radiations are usually higher order harmonics of the clock switching frequency, whereby most of the radiated power is concentrated around the second harmonic, i.e.  $2*f_0$  with  $f_0$  being the clock frequency.

#### **1.4 Radiation from an electric dipole**

As the active device connected to the via switches back and forth, the via can be approximated with a small electric dipole or current element of length  $d$ , which is about the thickness of the power plane pair. This distance is very small compared to the wavelength, such that the via can be considered as a small line source. If it is assumed that the current is a sinusoidal time variation  $I = I_0 e^{-j\omega t}$ , then the time-dependent field distribution can be

found at any point in the space by looking at the retarded potential A [22], which for the y-direction is given by (1.4)

$$A_y = \mu \frac{dI_0}{4\pi r} e^{-j(\omega r/c)} \quad (1.4).$$

In the system of spherical coordinates, the potential can be written in form of its components as:

$$A_r = A_y \cos \theta \quad (1.5),$$

and

$$A_\theta = -A_y \sin \theta \quad (1.6).$$

The electric and magnetic fields can be found directly from the potential as

$$H_\phi = \frac{I_0 d}{4\pi} e^{-jkr} \left( \frac{jk}{r} + \frac{1}{r^2} \right) \sin \theta \quad (1.7a),$$

$$E_r = \frac{I_0 d}{4\pi} e^{-jkr} \left( \frac{2\eta}{r^2} + \frac{2}{j\omega\epsilon r^3} \right) \cos \theta \quad (1.7b),$$

$$E_\theta = \frac{I_0 d}{4\pi} e^{-jkr} \left( \frac{j\mu\omega}{r} + \frac{1}{j\omega\epsilon r^3} + \frac{\eta}{r^2} \right) \sin \theta \quad (1.7c).$$

In the vicinity of the dipole, the fields behave more like the TEM static field. At infinity they can be approximated by the first order TM spherical wave. In [21] and [23], it was shown that the TEM wave is the dominant mode radiated by a via in parallel-plates environment.

## 1.5 Parallel-plate waveguides

The ground and supply voltage planes of the power distribution network constitute a parallel-plate waveguide. This type of structures can therefore support TE, TM and TEM modes [24]. In the idealization of the parallel-plate waveguide illustrated in Figure 1-3, the dimensions in the  $z$ - and  $x$ -directions are assumed to be much larger than the thickness  $d$  of the waveguide such that all fringing fields and any variation in the  $x$ -direction can be neglected. In the present analysis it is also assumed that the wave propagation is one-dimensional and in the  $z$ -direction.

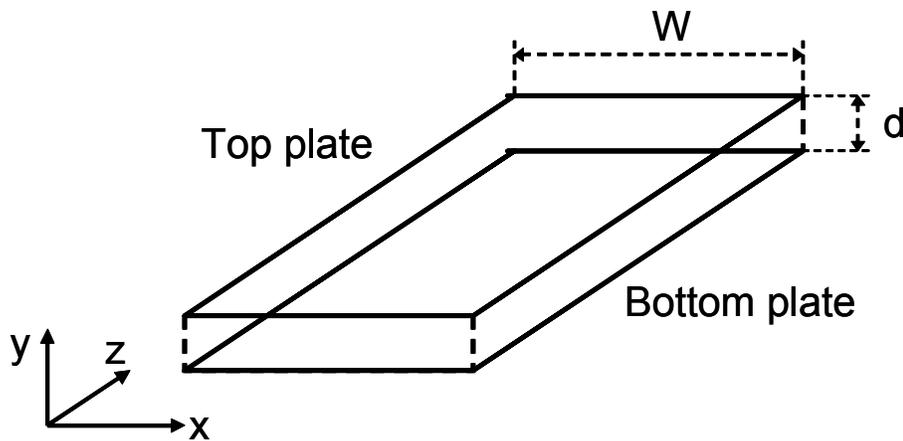


Figure 1-3: Illustration of a parallel-plate waveguide

### 1.5.1 Transverse electromagnetic (TEM) waves

The TEM waves correspond to the situation, where there are neither electric nor magnetic fields in the direction of propagation. In this case the wave solution can be obtained by solving Laplace's equation (1.8) for the scalar electrostatic potential  $\Phi(x,y)$  for

$0 < x < W$  and  $0 < y < d$ , whose boundary conditions are given by (1.9a) and (1.9b) for the power plane pair.

$$\nabla^2 \Phi(x, y) = 0 \quad (1.8)$$

$$\Phi(x, 0) = 0 \quad (1.9a)$$

$$\Phi(x, d) = V_{dd} \quad (1.9b)$$

With the assumption that there is no variation in the x-direction, the general solution is of the type

$$\Phi(x, y) = A + By \quad (1.10)$$

By including the boundary condition at  $y=0$  and  $y=d$ , the constants  $A = 0$  and  $B = V_{dd} / d$ , meaning that the electrostatic potential is given as:

$$\Phi(x, y) = V_{dd} \frac{y}{d} \quad (1.11).$$

The transverse electric field is then calculated as

$$\vec{E}(x, y) = -\nabla \Phi(x, y) = \hat{y} \frac{V_{dd}}{d} \quad (1.12),$$

so that the total electric field is

$$\vec{E}(x, y, z) = -\hat{y} \frac{V_{dd}}{d} e^{-jkz} \quad (1.13).$$

The magnetic field is then obtained as

$$\vec{H}(x, y, z) = \frac{1}{\eta} \hat{z} \times \vec{E}(x, y, z) = \hat{x} \frac{V_{dd}}{\eta d} e^{-jkz} \quad (1.14),$$

where

$$k = \omega \sqrt{\mu \epsilon} \quad (1.15)$$

and

$$\eta = \sqrt{\frac{\mu}{\epsilon}} \quad (1.16)$$

are respectively the propagation constant of the TEM wave and the intrinsic impedance of the medium between the parallel-plate.

The characteristic impedance and phase velocity (which is the velocity of light in the medium) are given by (1.17) and (1.18) and are only dependent on the geometry and material property.

$$Z_0 = \frac{V}{I} = \frac{\eta d}{W} \quad (1.17)$$

$$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{\mu\epsilon}} \quad (1.18)$$

Here it is important to note that TEM waves are excited and supported by parallel-plate waveguides at all frequencies.

### 1.5.2 Transverse magnetic (TM) waves

The TM solution is obtained by solving the reduced ( $d/dx=0$ ) wave equation (1.19) to obtain the non-vanishing component of the electric field in the z-direction.

$$\left( \frac{\partial^2}{\partial y^2} + k_c^2 \right) e_z(x, y) = 0 \quad (1.19),$$

where  $k_c^2 = k^2 - \beta^2$  is the cutoff wave number and  $E_z(x, y, z) = e_z(x, y)e^{-jkz}$ .

The general solution to (1.19) is of the form

$$e_z(x, y) = A \sin k_c x + B \cos k_c y \quad (1.20).$$

By applying the boundary conditions (1.9a) and (1.9b) to (1.20), one obtains

$$B = 0 \text{ and } k_c = \frac{n\pi}{d} \quad n=0, 1, 2 \dots \quad (1.21).$$

The electric field in the z-direction is then given as

$$E_z(x, y, z) = A_n \sin \frac{n\pi y}{d} e^{-j\beta z} \quad (1.22a).$$

The transverse fields can be derived from the Ez-field component to be

$$H_x = \frac{j\omega\epsilon}{k_c} A_n \cos \frac{n\pi y}{d} e^{-j\beta z} \quad (1.22b),$$

$$E_y = \frac{-j\beta}{k_c} A_n \cos \frac{n\pi y}{d} e^{-j\beta z} \quad (1.22c),$$

$$E_x = H_y = H_z = 0 \quad (1.22d).$$

For  $n=0$ , the  $TM_0$  mode is the same as the TEM mode. For  $n \geq 1$ , each value of  $n$  corresponds to a different  $TM_n$  mode with its own propagation constant given by:

$$\beta = \sqrt{k^2 - k_c^2} = \sqrt{k^2 - \left(\frac{n\pi}{d}\right)^2} \quad (1.23).$$

For a wave to propagate, its propagation constant has to be real. This requires that the wave number be larger than the cut-off wave number  $k_c$ . The cut-off frequency for the  $TM_n$  wave can then be defined as

$$f_c = \frac{k_c}{2\pi\sqrt{\mu\epsilon}} = \frac{n}{2d\sqrt{\mu\epsilon}} \quad (1.24).$$

Thus the lowest TM mode is  $TM_1$  with cutoff frequency of  $1/2d\sqrt{\mu\epsilon}$  and all higher modes are multiples of this. The wave impedance  $Z_{TM}$  and the phase velocity are given by (1.25)

and (1.26) and are both frequency-dependent, with the latter being larger than the speed of light in the medium.

$$Z_{TM} = -\frac{E_y}{H_x} = \frac{\beta}{\omega\epsilon} = \frac{\beta\eta}{k} = \eta\sqrt{1 - \left(\frac{\omega_c}{\omega}\right)^2} \quad (1.25)$$

$$v_p = \frac{\omega}{\beta} = \frac{c}{\sqrt{1 - (\omega_c / \omega)^2}} \quad (1.26)$$

From (1.26), the group or energy velocity can be found as

$$v_g = \frac{d\omega}{d\beta} = c\sqrt{1 - \left(\frac{\omega_c}{\omega}\right)^2} \quad (1.27),$$

where  $c$  is the velocity of light in the medium.

### 1.5.3 Transverse electric (TE) waves

Since the TE waves have no electric field component in the  $z$ -direction, the solution for these modes is obtained by first solving the reduced ( $d/dx=0$ ) wave equation for the non-vanishing component of the magnetic field in the  $z$ -direction. This is the same as solving (1.19) with  $e_z(x,y)$  replaced by  $h_z(x,y)$ . The solution is of the form

$$h_z(x, y) = A \sin k_c y + B \cos k_c y \quad (1.28).$$

From (1.28) the electrical field in the direction of propagation can be obtained as

$$E_x(x, y, z) = \frac{-j\omega\mu}{k_c} [A \cos k_c y - B \sin k_c y] e^{-j\beta z} \quad (1.29).$$

Applying the boundary conditions (1.9a) and (1.9b) to (1.29) results in  $A=0$  and  $k_c = \frac{n\pi}{d}$ ,

$n=0, 1, 2, \dots$  The final solution for  $H_z$  is then given by

$$H_z(x, y, z) = B_n \cos \frac{n\pi y}{d} e^{-j\beta z} \quad (1.30a).$$

And the transverse fields are given as

$$E_x(x, y, z) = \frac{j\omega\mu}{k_c} B_n \sin \frac{n\pi y}{d} e^{-j\beta z} \quad (1.30b)$$

$$H_y(x, y, z) = \frac{j\beta}{k_c} B_n \sin \frac{n\pi y}{d} e^{-j\beta z} \quad (1.30c)$$

$$E_z = E_y = H_x = 0 \quad (1.30d)$$

The propagation constant and the cutoff frequency are the same as those of the TM<sub>n</sub> waves.

The wave impedance is given as:

$$Z_{TE} = \frac{E_x}{H_y} = \frac{\omega\mu}{\beta} = \frac{k\eta}{\beta} \quad (1.31)$$

#### 1.5.4 Wave propagation in practical power planes

The cut-off frequency was found to be  $1/2d\sqrt{\mu\epsilon}$  for the lowest TE and TM modes and increases with the mode number. Typical power planes have a thickness of less than 5 mm. This implies that the parallel-plate TE<sub>n</sub> and TM<sub>n</sub> modes have cut-off frequencies in the order of hundreds of Gigahertz and are not a major concern for systems operating at 10 GHz and below. The only modes of concerns are the TEM modes and the rectangular waveguide modes induced by the finite nature of the power planes. In fact, in the

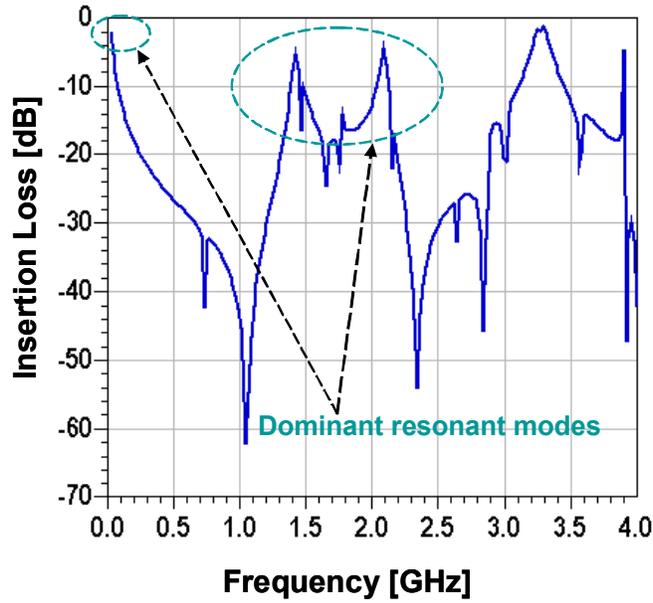


Figure 1-4: Typical transmission characteristic of a 10 cm x 10 cm parallel-plate waveguide showing dominant resonant modes at DC and at high frequencies

calculation of the parallel-plate waveguide modes, it was assumed that the plates have infinite length in the z-direction. In practical power planes, the width (W) and length (L) of the plates are finite. In this case, waves propagating to the edge of the waveguide have to be reflected back and forth. In addition to the parallel-plate modes, rectangular cavity modes are also excited. Both  $TE_{mn}$  and  $TM_{mn}$  modes have the same propagation constant and cutoff frequency given by (1.31) and (1.32) respectively.

$$\beta = \sqrt{k^2 - k_c^2} = \sqrt{k^2 - \left(\frac{n\pi}{W}\right)^2 - \left(\frac{m\pi}{L}\right)^2} \quad (1.31)$$

$$f_{cmn} = \frac{1}{2\pi\sqrt{\mu\epsilon}} \sqrt{\left(\frac{m\pi}{W}\right)^2 + \left(\frac{n\pi}{L}\right)^2} \quad (1.32).$$

Figure 1-4 is an illustration of the dominant modes in the power plane, where high transmission coefficients can be seen at both DC and at GHz frequencies.

## 1.6 Periodic structures

### 1.6.1 *Electromagnetic band-gap structures*

Artificial magnetic conductors have generated a lot of attention during the recent years, mostly because of their ability to suppress surface wave propagation at microwave and optical frequencies. In the early research, efforts were mainly focused on photonic band-gap structures (PBG) or photonic crystals, which were mainly artificial periodic structures, in which optical wave propagation was very similar to electron wave propagation in natural crystals. Starting from uniform dielectric substrates, photonic band-gap structures were realized by first creating periodic holes in the dielectric substrate and then filling them with another dielectric material of different dielectric constant. The generation of a (frequency) stop-band by any of these structures relies solely on the Bragg reflection condition, which requires that the period of the structure has to be at least half the wavelength at the frequency of interest. With the dielectric posts replaced by either metallic patches [25]- [28] or metallic posts [29], the structure could exhibit the pass-/stop-band behavior at microwave frequencies, leading to the creation of so-called Electromagnetic Band-Gap structures (EBGs). (a) (b)

Figure 1-5 illustrates the different types of photonic band-gap structures. The microwave community has shown interest in EBGs because of their tremendous potential for eliminating surface wave-related performance degradation in antennas [30]-[35], filters

[36]-[43], [50] and other waveguides. In general only a few novel electromagnetic band-gap structures have been proposed in the literature [44]-[46], and these structures have been directly used in applications [47]-[49] by other researchers.

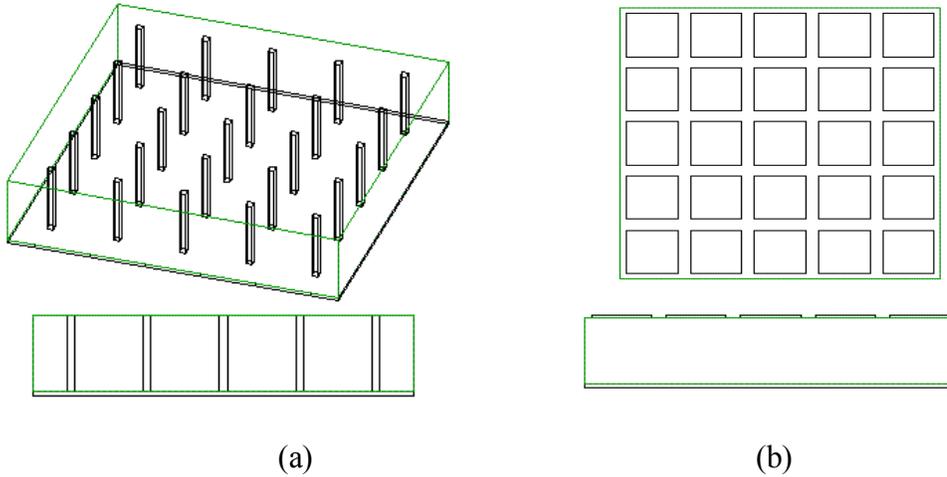


Figure 1-5: Illustration of electromagnetic band-gap structures with (a) vertical posts and (b) planar surface patches.

### 1.6.2 High-impedance electromagnetic surfaces

The concept of high-impedance electromagnetic surface was first introduced by [15]. The very basic structure illustrated in Figure 1-6 is a combination of the two traditional periodic EBGs of Figure 1-5. While the periodic nature of the high-impedance electromagnetic surfaces may be very practical in analyzing them, their fundamental operation is based on the lumped behavior of the vias and of the patches to produce a band-stop filter-like behavior. The planar patches provide fringing capacitance, whereas inductance is provided mostly by the vertical vias, such that the HIS can be approximated

as a two-dimensional array of LC resonators. In an open environment, these surfaces support TM surface waves only at low frequencies, where its inductive behavior is dominant and TE surface waves only at high frequencies, where its capacitive behavior is dominant. Between the two regions, there is a transition region or forbidden band-gap, where the HIS behaves as a perfect magnetic conductor and supports no electromagnetic waves. The HIS can roughly be modeled as a parallel LC resonant circuit, where L and C are the sheet inductance and sheet capacitance of the surface. According to [15], both L and C can be determined as a function of the geometry and material property using the effective medium mode (1.33), (1.34). In equation (1.33) it is assumed that the substrates below and above the patches have different dielectric constants.

$$C = \frac{W(\epsilon_1 + \epsilon_2)}{\pi} \text{Cosh}^{-1}\left(\frac{a}{g}\right) \quad (1.33)$$

$$L = \mu \cdot t \quad (1.34).$$

Since the introduction of the HIS, numerous works have focused on designing those structures for even lower frequency, most of which use the method of enhancing the capacitance density.

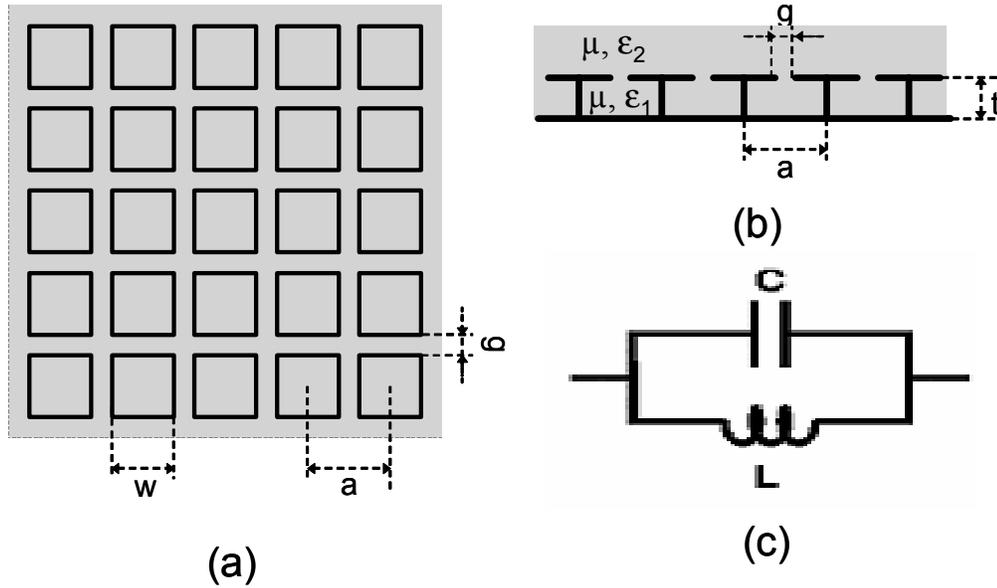


Figure 1-6: (a) Top view, (b) cross section and parallel-LC equivalent circuit of a single-layer high-impedance surface as described in [15].

## 1.7 Wave propagation in periodically loaded parallel-plate waveguides

### 1.7.1 Periodically loaded transmission line as one-dimensional periodic structure

A simple example of one-dimensional periodically loaded parallel-plate waveguide is the parallel-plate transmission line of Figure 1-7 [22], where the ground plane is replaced by a corrugated surface of period  $Lz$ , gap  $g$  and height  $t$ . Such a structure can be approximated as a periodic shorted transmission line. If a TM wave with no variation in the  $x$ -direction is assumed, then there is only an electric field component in the  $z$ -direction. A unit cell of this waveguide is illustrated in Figure 1-7. At the plane  $y=0$ , a good approximation for the boundary conditions for the electric field is given by (1.35).

$$E(0, z) = 0 \text{ for } g/2 < z < Lz - g/2 \text{ and } E_0 \text{ elsewhere} \quad (1.35),$$

where  $E_0$  is a constant. When the propagating wave reaches the discontinuities there is a wave scattering that results in the excitation of both forward and backward propagating higher order modes. Since all these modes exist at the same time, a solution to Maxwell's equations that satisfies the boundary condition  $E_z(0,z)=0$  are the spatial harmonics obtained by summing the solutions of the discrete modes for the smooth surface give by (1.22a)-(1.22d). The solution for the electric field in the z-direction is then given by (1.36a)-(1.36c)

$$E_z(y, z) = \sum_{n=-\infty}^{\infty} A_n \sin K_n (d - y) e^{-j\beta_n z} \quad (1.36a)$$

$$E_y(y, z) = \sum_{n=-\infty}^{\infty} \frac{j\beta_n}{K_n} A_n \cos K_n (d - y) e^{-j\beta_n z} \quad (1.36b)$$

$$H_x(y, z) = \sum_{n=-\infty}^{\infty} \frac{j\omega\epsilon}{K_n} A_n \cos K_n (d - y) e^{-j\beta_n z} \quad (1.36c)$$

where

$$K_n^2 = \omega^2 \mu\epsilon - \beta_n^2 = k^2 - \beta_n^2 \quad (1.37)$$

and

$$\beta_n = \beta_0 + \frac{2\pi n}{L_z} \quad (1.38).$$

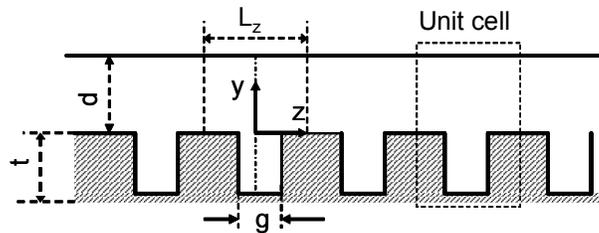


Figure 1-7: Cross section and of periodically loaded transmission line used to illustrate one-dimensional wave propagation in periodically loaded parallel-plate waveguide.

If the boundary conditions for the field are known the coefficient  $A_n$  can be determined in each of the three regions of the unit cell. The exact solution can then be obtained by solving the boundary conditions for the electric field at  $y=0$ . For a given point  $(x, y, z = z_0 + mL_z)$  such that  $m$  is an integer and  $0 < z < L_z$ , the field solutions can be obtained by multiplying the field at  $(x,y,z_0)$  by the phase shift  $e^{-j\beta_0 mL_z}$ . This is also known as Floquet's theorem [52].

### 1.7.2 Two-dimensional wave propagation in a 2-dimensional periodic lattice

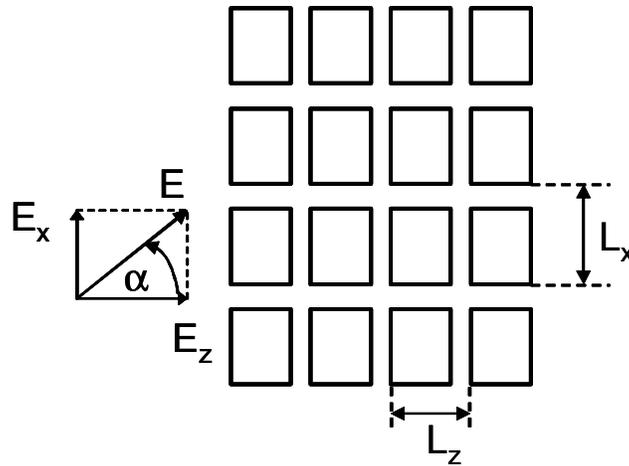


Figure 1-8: Illustration of two-dimensional wave propagation in a periodic lattice

Let us consider an in-plane TM wave that is propagating along the 2-D periodically loaded transmission waveguide with an incident angle  $\alpha$ , with respect to the normal incidence as illustrated in Figure 1-8. The periodic structure is supposed to have a rectangular lattice with lattice constants  $L_z$  in the  $z$ -direction and  $L_x$  in the  $x$ -direction. For

the TM wave the only field component in the direction of propagation is the electric field

E. E has to satisfy the basic wave equation:

$$\left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + k_c^2 \right) \vec{E} = 0 \quad (1.39)$$

A decomposition of the electric field in its z- and x-components gives

$$\vec{E} = \hat{x}E_x + \hat{z}E_z \quad (1.40).$$

By combining (1.39) and (1.40) the wave equation can be rewritten for each component of the field as given by (1.41a) and (1.41b).

$$\left( \frac{\partial^2}{\partial z^2} + \frac{\partial^2}{\partial y^2} + k_{cx}^2 \right) E_x = 0 \quad (1.41a)$$

$$\left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + k_{cz}^2 \right) E_z = 0 \quad (1.41b)$$

The solution to (1.41b) was given by (1.36a)-(c) by assuming no variation of the field in the x-direction. To find the solutions to (1.41a) it is also assumed that the field component  $E_x$  does not vary with z such that  $d/dz=0$ . The solutions for the fields are very similar to that of (1.41b) and are given by

$$E_x(x, y) = \sum_{m=-\infty}^{\infty} A_m \sin K_m (d - y) e^{-j\beta_m x} \quad (1.42a).$$

From (1.42a) the electric and magnetic field in the x and y-directions are derived as

$$E_y(x, y) = \sum_{m=-\infty}^{\infty} \frac{j\beta_m}{K_m} A_m \cos K_m (d - y) e^{-j\beta_m x} \quad (1.42b),$$

$$H_z(x, y) = \sum_{m=-\infty}^{\infty} \frac{j\omega\epsilon}{K_m} A_m \cos K_m (d - y) e^{-j\beta_m x} \quad (1.42c),$$

where

$$K_m^2 = \omega^2 \mu \epsilon - \beta_m^2 = k^2 - \beta_m^2 \quad (1.43)$$

and

$$\beta_m = \beta_0 + \frac{2\pi m}{L_x} \quad (1.44).$$

The general solution of the field for a two-dimensional propagation is obtained by adding the solutions of equations (1.41a) and (1.41b) such that,

$$E_x(x, y) = \sum_{m=-\infty}^{\infty} A_m \sin K_m (d - y) e^{-j\beta_m x} \quad (1.42a)$$

$$E_y(x, y, z) = \sum_{n=-\infty}^{\infty} \frac{j\beta_n}{K_n} A_n \cos K_n (d - y) e^{-j\beta_n z} + \sum_{m=-\infty}^{\infty} \frac{j\beta_m}{K_m} A_m \cos K_m (d - y) e^{-j\beta_m x} \quad (1.45),$$

$$E_z(y, z) = \sum_{n=-\infty}^{\infty} A_n \sin K_n (d - y) e^{-j\beta_n z} \quad (1.36a),$$

$$H_x(y, z) = \sum_{n=-\infty}^{\infty} \frac{j\omega \epsilon}{K_n} A_n \cos K_n (d - y) e^{-j\beta_n z} \quad (1.36c),$$

$$H_z(x, y) = \sum_{m=-\infty}^{\infty} \frac{j\omega \epsilon}{K_m} A_m \cos K_m (d - y) e^{-j\beta_m x} \quad (1.42c),$$

$$H_y(x, y, z) = 0 \quad (1.46).$$

All coefficients can be obtained for the unit cell by applying the known boundary conditions for the field. The solution outside the unit cell is then obtained by applying Floquet's theorem.

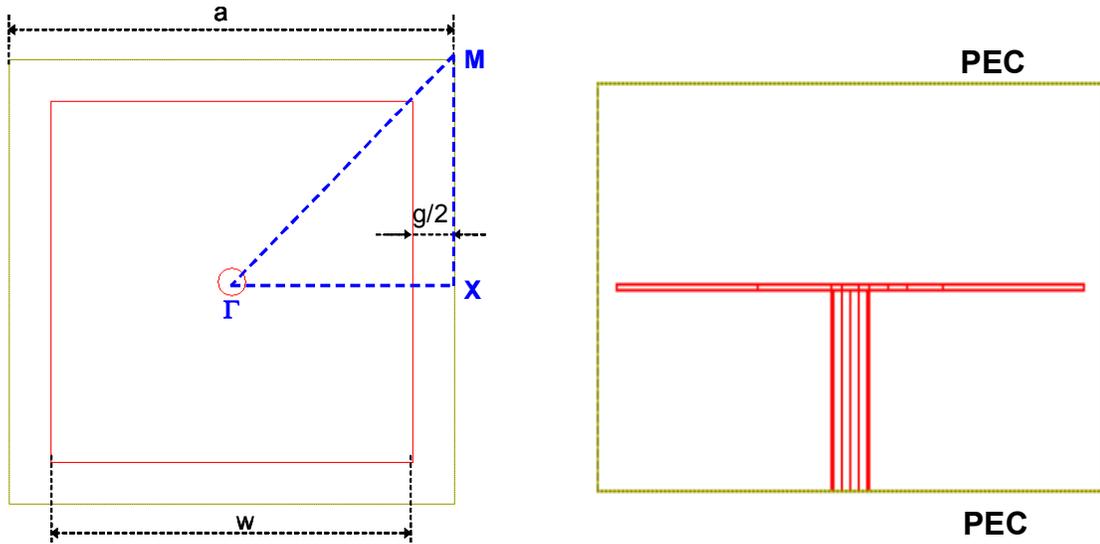


Figure 1-9: Top view and cross section of the unit cell of a periodic HIS in parallel-plate environment.

## 1.8 Characterization of periodic structures

### 1.8.1 Dispersion diagram

The dispersion or  $\beta$ - $\omega$  or  $k$ - $\omega$  diagram can be calculated from the unit cell. Two-dimensional eigenmode solutions for Maxwell's equations are obtained for the restricted unit cell (or Brillouin zone) under periodic boundary conditions. Algorithms for solving Maxwell equations under periodic boundary conditions have been implemented using both the Green's function based method of moments [53] and the finite element method. In the present work we used a commercially available simulation tool based on the vectorial finite element method [55]. For open surfaces this code also utilizes the perfectly matched layer (PML) [56] proposed by [56] to model perfect absorbing or open boundary conditions. For periodically loaded parallel-plate waveguides, where both top and bottom plates are

conducting material as illustrated by the perfect electric conductor (PEC) of Figure 1-9, a PML is not necessary. Figure 1-9 shows the top view and cross section of a typical HIS unit cell in parallel-plate environment. A square cell of period,  $a$ , and gap,  $g$ , is considered. The reduced Brillouin triangle  $\Gamma$ -X-M is included as well.

The calculation of the dispersion diagram involves three major steps [85]. First, the phase constant (phase2) between the two sides (of the unit cell) parallel to the segment M-X is fixed to 0 and the phase constant (phase1) between the two sides (of the unit cell) parallel to the segment  $\Gamma$ -X is varied from 0 to 180 degrees, while Maxwell's equations are being solved for the first N eigenmode frequencies. This corresponds to one-dimensional wave propagation with the direction of propagation orthogonal to the segment  $\Gamma$ -X. Second, phase1 is fixed to 180 degrees and phase2 is varied from 0 to 180 degrees while Maxwell's equations are being solved for the first N eigenmode frequencies. This corresponds to one-dimensional wave propagation in the direction perpendicular to the segment X-M. In the third step, both phase1 and phase2 are varied simultaneously from 180 to 0 degrees, which corresponds to two-dimensional wave propagation with direction of propagation diagonal to the lattice. For most (symmetric) cells the  $\Gamma$ -X section of the dispersion diagram is sufficient to describe its frequency behavior. Since the phase shift is given by  $\exp(-j\beta L)$ , according to Floquet's theorem for the periodic boundary condition, a variation of the phase corresponds to a change in the wave number and/or propagation constant.

The resulting dispersion diagram for the sample unit cell of Figure 1-9 is shown in Figure 1-10. A frequency bandgap, where the infinite structure does not allow any wave

propagation, can be seen between the first and second modes. In addition to the first three eigenmodes the dispersion diagram also includes the light line, which corresponds to the one-dimensional (x or z) and two-dimensional propagation of light in that medium. For the  $\Gamma$ -X section of the triangle, the light line falls on  $\text{phase1} \cdot c/a \cdot 360$ , where  $c$  is the speed of light in the medium and  $a$  is the period of the lattice. For the M- $\Gamma$  section of the triangle, the light line falls on  $\text{phase2} \cdot c/d \cdot 360$ , where  $d$  is the hypotenuses of the triangle. Periodic structures are often called slow wave waveguides because they support waves whose speed is lower than that of light in the medium as it is the case for mode 1 seen in Figure 1-10. Additional information that can be extracted from the dispersion diagram is the group or energy velocity given by the slope of the  $\beta$ - $\omega$  curve or equation (1.27).

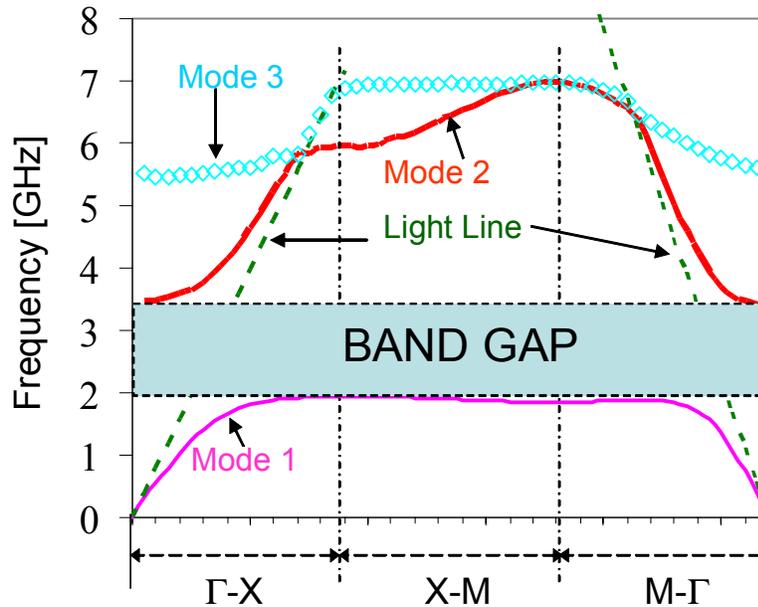


Figure 1-10: Full dispersion diagram of typical parallel-plate waveguide loaded with periodic HIS.

### 1.8.2 Scattering parameters

Performance of periodic microwave structures can be analyzed using the scattering or S-parameters. These are usually easy to calculate and are obtained from power transfer and reflection between two designated ports on the structure. S-parameters of structures with finite physical dimensions are very useful as they directly give the location of the bandgap (or stopband), its width and the center frequency. In addition it provides the level of signal attenuation at different frequencies.

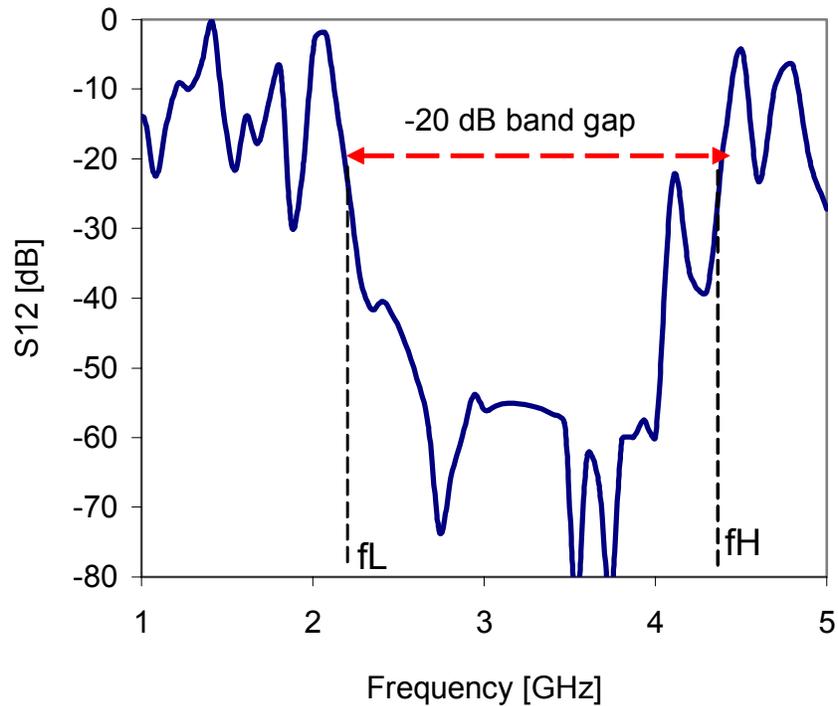


Figure 1-11: Typical insertion loss of finite size parallel-plate waveguide loaded with periodic HIS showing the -20 dB band-gap and the corner frequencies.

Figure 1-11 is an example of S-parameters (S12 only) of a parallel-plate waveguide loaded with a periodic high-impedance electromagnetic surface. From the S12 curve an  $x$ -dB (-20 dB in this case) bandwidth, with lower and upper corner frequencies  $f_L$  and  $f_H$  can be defined.  $x$  represents the level of the insertion loss. The center frequency  $f_0$ , the fractional bandwidth  $\Delta BW$  and the absolute bandwidth  $BW$  are defined from  $f_L$  and  $f_H$  as:

$$f_0 = \frac{f_H + f_L}{2} \quad (1.47),$$

$$BW = f_H - f_L \quad (1.48),$$

$$\Delta BW = \frac{BW}{f_0} = \frac{2(f_H - f_L)}{f_H + f_L} \quad (1.49).$$

## Chapter 2

# **Power Planes with Integrated Standard High-Impedance Electromagnetic Surfaces**

### **2.1 Introduction**

Until recently most efforts in mitigating packaging or board level simultaneous switching noise has been limited to the use of decoupling capacitors between the ground and the Vdd plane [2], [6]-[9]. This was mainly due to the limited understanding of the impact of propagating waves in the parallel plate environment on switching noise. Although the switching frequency has steadily increased, the solution being looked upon is still the one used for transient switching at low frequency. The mitigation of noise due to electromagnetic radiation has still not been addressed. Instead, most attempts are towards designing to avoid the high resonant region of the parallel-plate power planes. A new concept for mitigating simultaneous switching noise mainly due to high-speed radiation is introduced in this chapter. It consists of replacing either the ground or the Vdd plane of a parallel-plate power plane with a high-impedance electromagnetic surface (HIS). Parallel-plate resonant modes that normally support the propagation of voltage waves between simple power plane pairs are suppressed in the frequency range, where the HIS has its forbidden band-gap. Section 2.2 discusses the simulation setup and the limitation of the conventional decoupling. The novel concept is described in section 2.3. Simulated S-parameters are used in section 2.4 to study the impact of the geometry on the performance

of the novel power plane system. In section 2.5 a systematic study based on the dispersion diagram extraction is used to study the fundamental limitations of the power planes in mitigating simultaneous switching noise. The concept of nested power planes is introduced in the last part of the chapter.

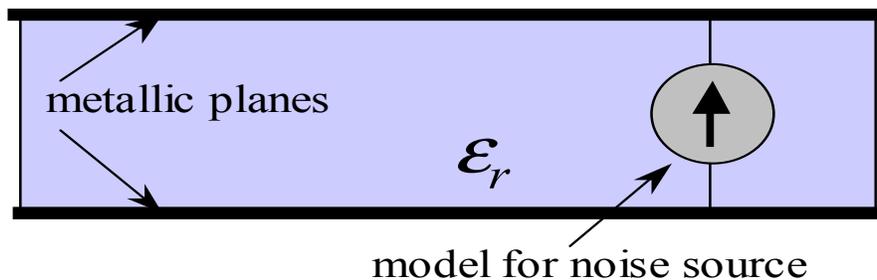


Figure 2-1: Full wave model of a traditional power plane with noise source.

## 2.2 Full wave model of a traditional power plane and EM simulator validation

Figure 2-1 shows the simplified model used for the traditional power plane analysis. The two planes are represented by two solid metallic plates, separated by dielectric material. The connecting or through via, which actually is the source of the radiating waves (or noise source), is replaced with an ideal wave port. The characteristics of the power planes are evaluated by calculating the S-parameters, which gives the power transfer from the noise source to any load located on the power plane. The simulation is performed in a 50-Ohm environment using the finite-element method based simulator HFSS [55].

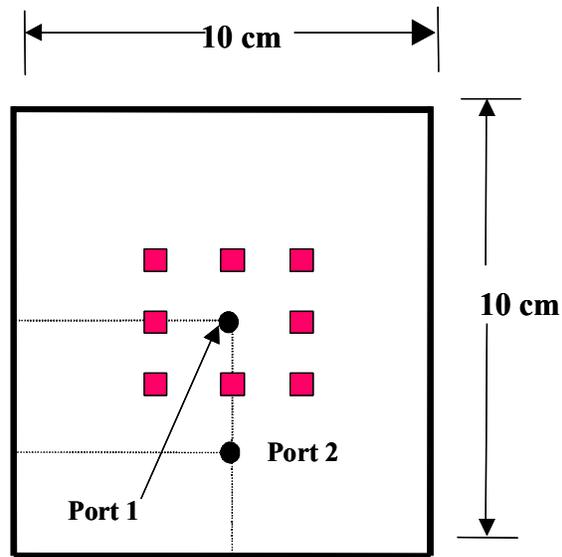


Figure 2-2: Top view of traditional power plane with decoupling capacitors around noise source. The noise source can be a via or a sensitive IC.

The validation of the simulator is established by comparing the S-parameters generated through measurement and simulation for the 10 cm x 10 cm reference board shown in Figure 2-2. The total height of the power plane is 1.54 mm, and the dielectric constant is 4.4. The parasitic inductance and resistance of the decoupling capacitors are also taken into consideration. The noise source is placed at the center of the board with coordinate (5 cm, 5 cm) and the load is placed at (5 cm, 2 cm). The simulation is performed for the board without decoupling capacitance and then with eight decoupling capacitors spread around the noise source as in [5]. The transmission coefficient S12 calculated by HFSS is presented in Figure 2-3 along with a comparison to experimental measurements performed in [5]. The power plane without decoupling capacitors exhibits very high transmission at low, intermediate and high frequencies. A very good agreement can be seen

over the entire frequency range between the measured and simulated data. As expected, the decoupling capacitors are only effective at low frequencies ( $< 500$  MHz), where the impedance associated with the lead inductance of the discrete decoupling capacitors is negligible.

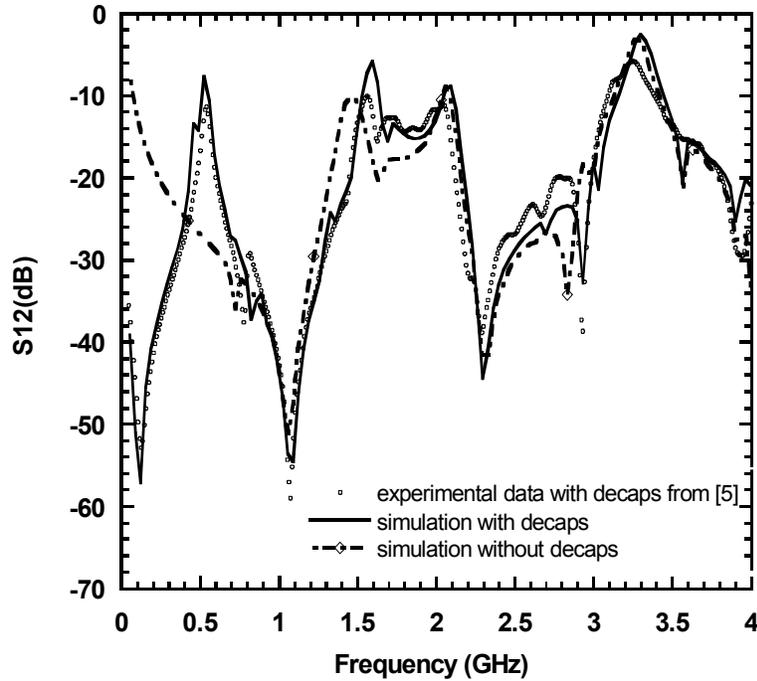


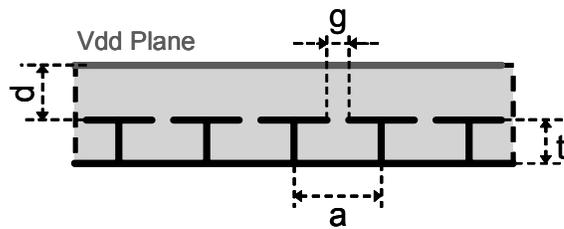
Figure 2-3: Measured vs. simulated S-parameters of a power plane with and without decoupling capacitors.

## 2.3 Power planes using high-impedance electromagnetic surfaces

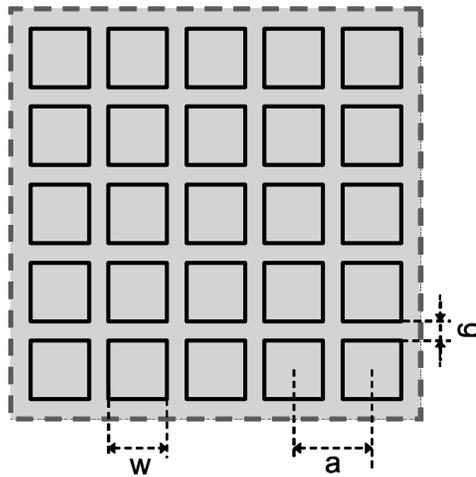
### 2.3.1 Power plane geometry

Figure 2-4 shows the top view and cross section of a typical power plane with integrated HIS, which was obtained by replacing the bottom plate or ground plane of the traditional power plane (Figure 2-1) with a HIS. The HIS has the ability of stopping surface

wave propagation in a given frequency band [15]. It consists of polygon-shaped metallic patches connected to a bottom metallic plate through straight metallic posts (or vias) with square or circular cross section and is filled with dielectric material. The key geometrical parameters of the power plane system include the via to via distance or period,  $a$ , of the HIS, the via height,  $t$ , the separation or gap,  $g$ , between the patches, the patch width,  $w$ , and the thickness,  $d$ , of the dielectric material between the HIS and the top or  $V_{dd}$  plane.



(a)



(b)

Figure 2-4: Typical geometry of power plane with integrated HIS: (a) Cross section and (b) top view.

### 2.3.2 Performance evaluation of the power planes with integrated HIS

Once the simulation capability is established, physical parameters of interest are varied to find the optimized noise mitigation capability or to analyze the parameter sensitivity. To illustrate this, the geometrical parameters  $t$  and  $g$  are varied and the resultant changes of the S-parameters are evaluated. From the S-parameters, which in principle represent the frequency response of the power plane, the center frequency, the fractional bandwidth, the noise mitigation bandwidth and the maximum insertion loss in the stop-band can be extracted. In the HFSS analysis, we used a lumped gap source [55] between the top of the HIS and the bottom of the Vdd plane. This illustrates a typical case, where the via or noise source is terminated at the top of the HIS. The width and length of the power plane are fixed at 9 cm x 10 cm for this analysis. The thickness  $d$  of the substrate above the HIS is 1.54 mm. The noise source is located at (4.5 cm, 4.5 cm) and the receiving port is at (4.5 cm, 1.5 cm).

#### 2.3.2.1 Effect of via height $t$

The first parameter to be studied is the via height. Figure 2-5 shows the frequency response of the power plane when the via height is varied from 1.54 mm to 4.62 mm. All other geometrical parameters are fixed. In this case  $g=150\ \mu\text{m}$  and  $a=10\ \text{mm}$ . When  $t$  increases the center frequency as well as the corner frequencies of the stop-band are all shifted towards lower frequencies. This decrease of the center frequency is associated with an effective increase of the sheet inductance, which is proportional to the via length as was

discussed in section 1.6.2 for the HIS as an open surface. The self-resonance frequency of the HIS is given as

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (2.1),$$

where L and C represent the sheet inductance and sheet capacitance of the HIS respectively [18]. At the same time the fractional bandwidth does not decrease significantly. This is attributed to the fact that it is proportional to

$$BW \sim \sqrt{L/C} \quad (2.2).$$

It is also important to notice that a significant increase of the via height is necessary to achieve noise mitigation in the hundreds MHz range.

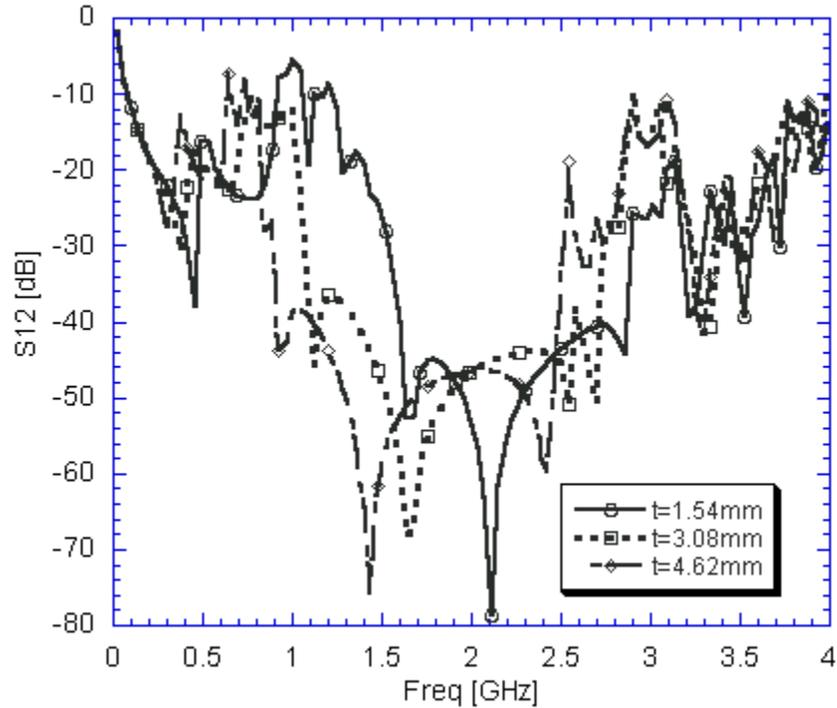


Figure 2-5: Effect of via length on frequency response of power plane with integrated HIS.

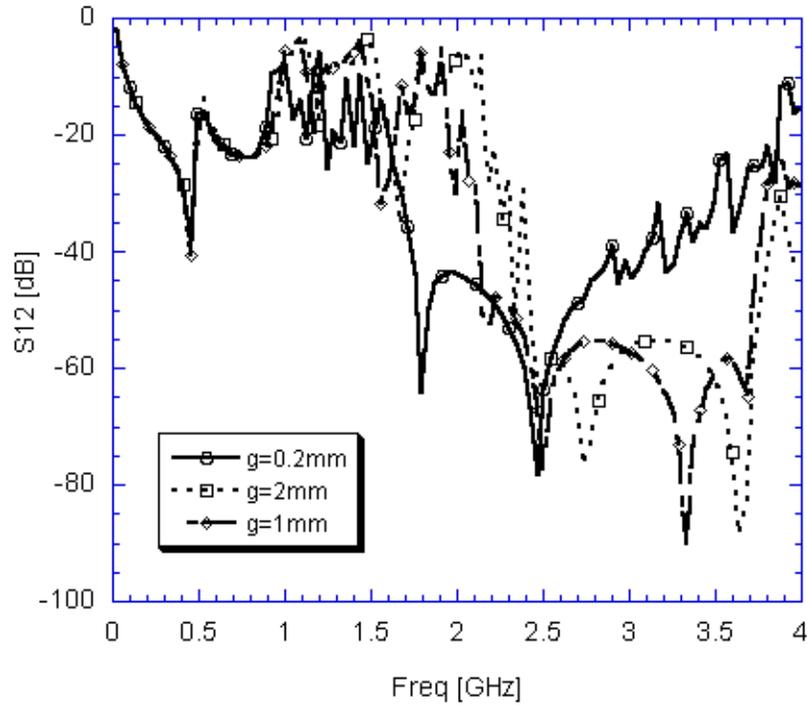


Figure 2-6: Effect of varying the patch separation on the frequency response of power planes with integrated HIS.

### 2.3.2.2 Effect of patch separation $g$

The patch separation  $g$  is varied from 2 mm to 0.20 mm with the via height fixed at 1.54 mm. All other geometrical parameters are kept constant. The distance between the HIS and the top plate is fixed at 1.54 mm. A decrease  $\Delta g$  of the spacing between the patches corresponds to an increase  $\Delta w = \Delta g$  of the patch width. When the spacing  $g$  decreases, the fringing capacitance between adjacent patches increases according to equation (1.33), which in turn leads to an overall increase of the HIS sheet capacitance. This implies both a decrease of the center frequency and of the fractional bandwidth according to equation (2.1) and equation (2.2) as illustrated by Figure 2-6. Especially it can

be seen that the lower edge of the stopband is moving towards lower frequencies with increasing spacing.

### 2.3.3 *Fundamentals limitations of power planes with integrated HIS*

In the previous section it was verified that the operating frequency of power planes with integrated HIS could be decreased by increasing the via height or by reducing the spacing between adjacent patches. To further understand what the fundamental limitations of this concept are, the period,  $a$ , and the spacing,  $g$ , are varied systematically and the  $\Gamma$ -X section of the dispersion diagram extracted for each structure. The electrical characteristics of interests, which are the center frequency, the lower corner frequency, the upper corner frequency, the absolute and the fractional bandwidths are then derived from the dispersion diagram. The study assumes an FR4 substrate with dielectric constant of 4.4 and a standard PCB technology, where the thickness of each substrate laminate is 1.54 mm. Table 2.1 shows the list of designs used in the simulation.

Design Number	$a$ [mm]	$t$ [mm]	$d$ [mm]	$g$ [mm]
1	3	1.54	1.54	0.4
2	5	1.54	1.54	0.4
3	8	1.54	1.54	0.4
4	10	1.54	1.54	0.4
5	15	1.54	1.54	0.4
6	20	1.54	1.54	0.4

Table 2-1: Summary of designs used for analyzing the fundamental limitations of power planes with integrated high-impedance electromagnetic surface. The same designs are also repeated for  $g=0.8, 1.2$  and  $2$  mm.

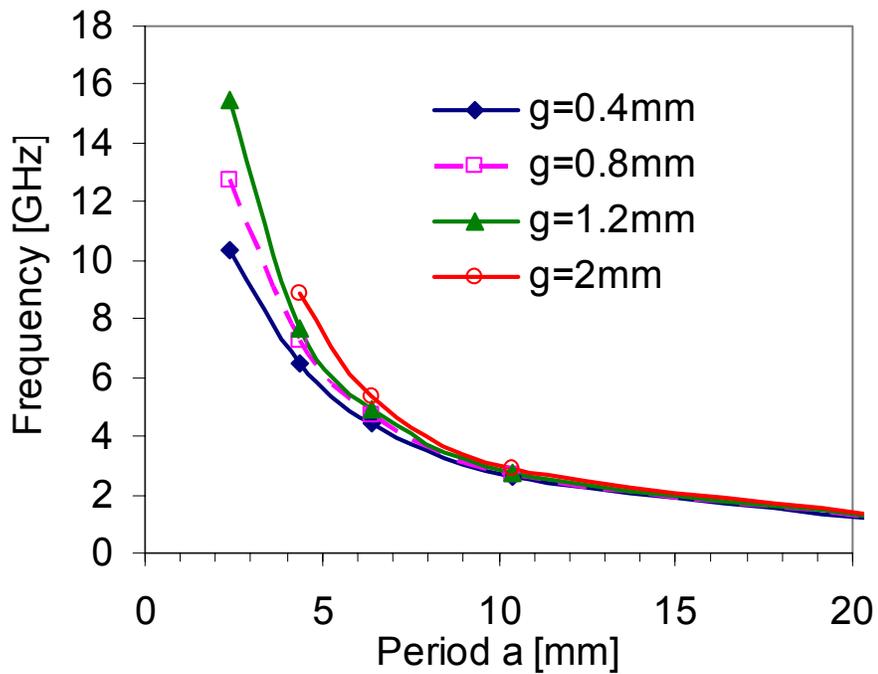


Figure 2-7: Dependence of the band-gap's center frequency on period and gap spacing.

Figure 2-7 shows the center frequency vs. period, where the gap is used as parameter. An increase in the period (with constant  $g$ ) corresponds to an increase in the patch dimensions, which effectively increases the sheet capacitance of the EBG. This leads to a decrease of the center frequency.

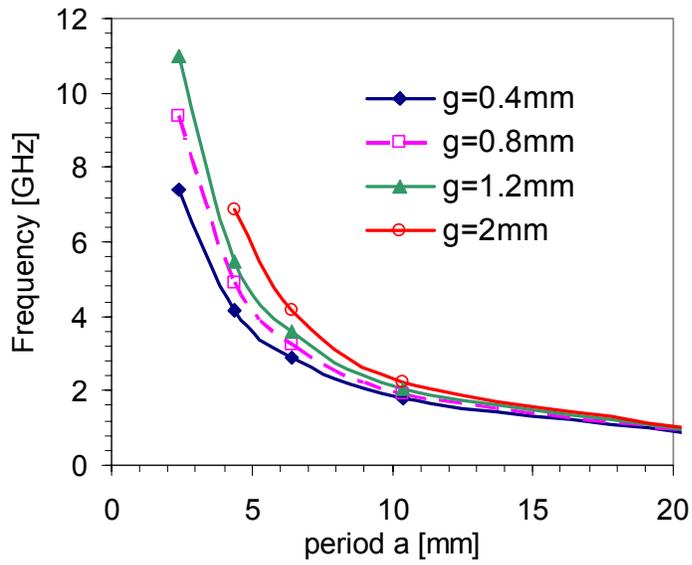


Figure 2-8: Dependence of the band-gap's lower corner frequency on the period and gap spacing.

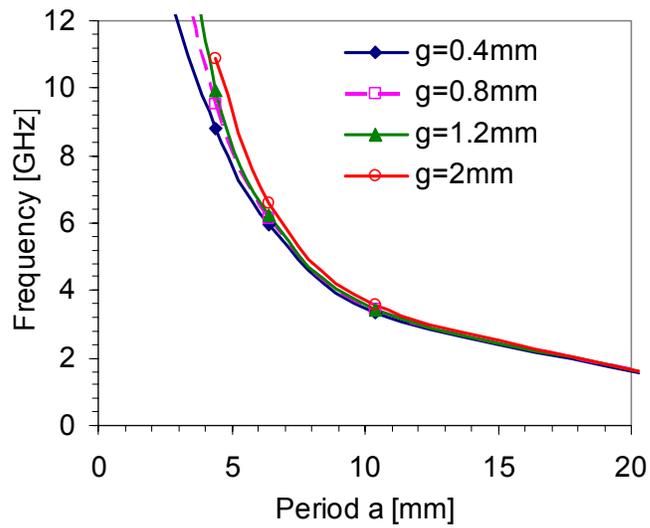


Figure 2-9: Dependence of the band-gap's upper corner Frequency on the period and gap between the patches.

Figure 2-8 and Figure 2-9 show the upper and lower corner frequencies of the stop-band vs. period, where the gap is used as parameter. The period has the most impact on the location of the upper corner frequency as it was discussed in [51] for capacitance-enhanced photonic band-gap structures (PBGs). The lower corner frequency on the other hand changes mostly with the gap, indicating its strong dependence on the lumped behavior of the high-impedance surface.

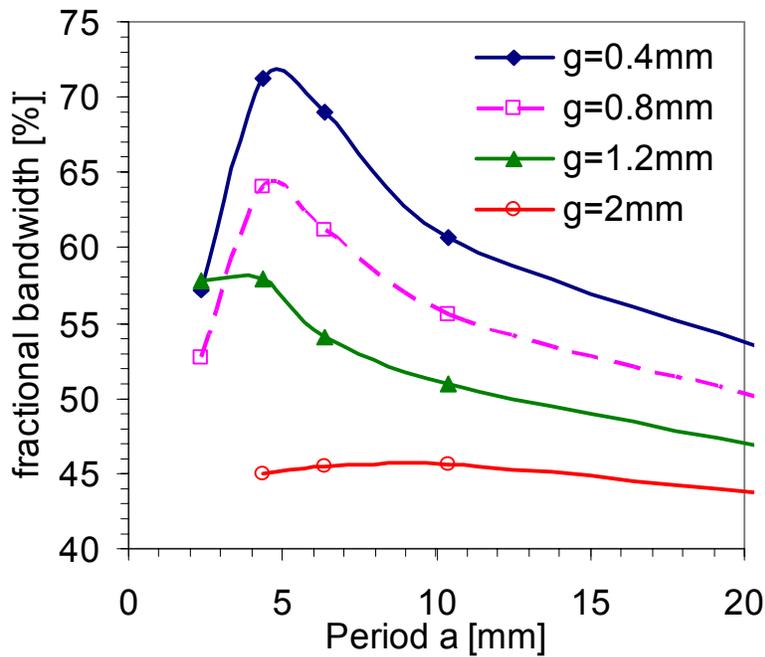


Figure 2-10: Dependence of the fractional bandwidth on the period and gap between the patches.

Figure 2-10 shows the fractional bandwidth vs. period. It starts at a low value, increases to a maximum and then decreases again. As the period increases, both the inductance of the patch and the fringing capacitance between adjacent patches increase.

When the width of the patch is much larger than the via height, the total inductance of the patch saturates against the sheet inductance of the regular parallel-plate wave guide given by (1.34). This results in a saturation of the total sheet inductance, which is equal to sum of the patch and via inductances. At this point the fractional bandwidth is at its maximum. Any increase of the period beyond this value only increases the sheet capacitance, which then leads to a decrease of the fractional bandwidth.

## **2.4 Power planes with nested high-impedance surfaces**

### *2.4.1 Geometry description*

So far we have discussed only cases, where either the ground or the Vdd plane was replaced with a high-impedance surface. In this section we introduce the concept of nested power planes, where the two plates are replaced with high-impedance surfaces. Figure 2-11 and Figure 2-12 show possible geometries for these structures that can be implemented on a two-substrate three-metal layer PCB. The two outer layers are solid metal plates and the intermediate or middle layer is used for the patches. In the power plane 1, the rows of patches, either in the x- or z-directions, are alternatively connected to the ground or the Vdd plane using straight vias. For the power plane of type 2, no two adjacent patches in the x- or z-directions are connected to the same potential. In other words, patches on the same diagonal are all connected to either the Vdd or the ground plane.

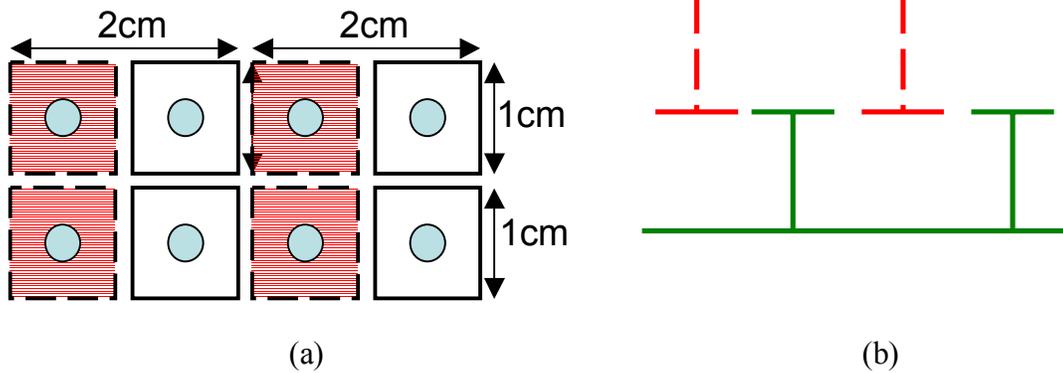


Figure 2-11: (a) Top view and (b) cross section of two calls of nested plane 1. Dashed lines represent the Vdd plane and solid lines represent the Gnd plane.

In order to validate the concept, we consider three different power plane pairs of lateral dimensions 10 cm x 10 cm each. The patches have square shapes of period 10 mm with a gap of 1 mm between adjacent patches. The height of each HIS is 1.54 mm. For the simplicity the vias have square cross section of 0.4 mm x 0.4 mm and the substrate is lossless FR4 with a dielectric constant of 4.4.

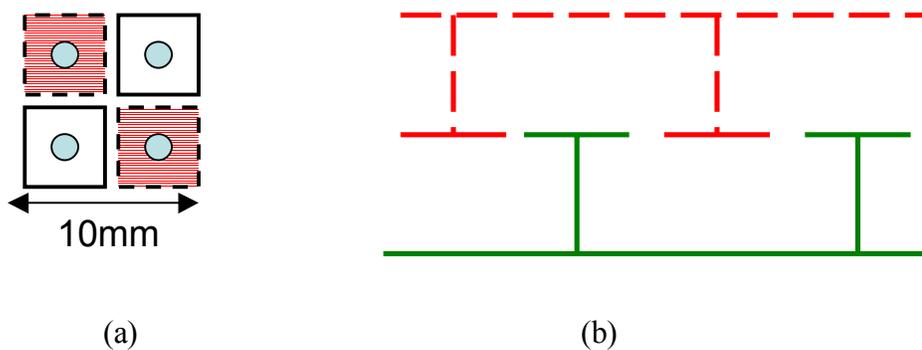


Figure 2-12: (a) Top view and (b) cross section of a unit cell of nested plane 2. . Dashed lines represent the Vdd plane and solid lines represent the Gnd plane.

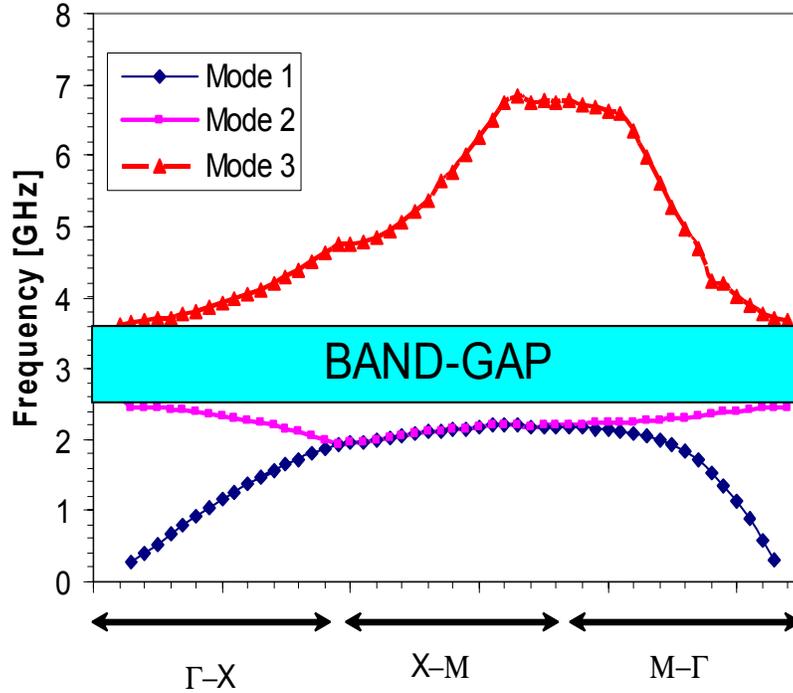


Figure 2-13: Dispersion diagram of nested plane 1.

#### 2.4.2 Simulation and discussion of results

The dispersion diagram of the nested plane 1 was extracted over the entire  $\Gamma$ -X-M triangle and is shown in Figure 2-13 for the first three modes. On the  $\Gamma$ -X and X-M portions of the triangle, the first mode is a slow-wave TM<sub>n</sub> mode that is tightly bound to the surface. The group velocity ( $d\omega/d\beta$ ) of this mode is positive on the  $\Gamma$ -X and X-M sections of the triangle, where the phase constant is positive, and negative on the on the M- $\Gamma$  segment, where the phase constant is negative. This implies that this mode is forward

propagating as a slow wave. The second mode is a  $TM_n$  surface wave, which falls exactly on the first mode on the X-M portion of the triangle. In the  $\Gamma$ -X and M- $\Gamma$  portions, it has a negative group and a positive phase velocities respectively and therefore corresponds to a backward propagating wave. The third mode is an undisturbed  $TE_n$  mode, which has its cutoff frequency at about 3.6 GHz. The forbidden band-gap of this nested plane resides between the second and third modes and is between 2.4 GHz and 3.6 GHz.

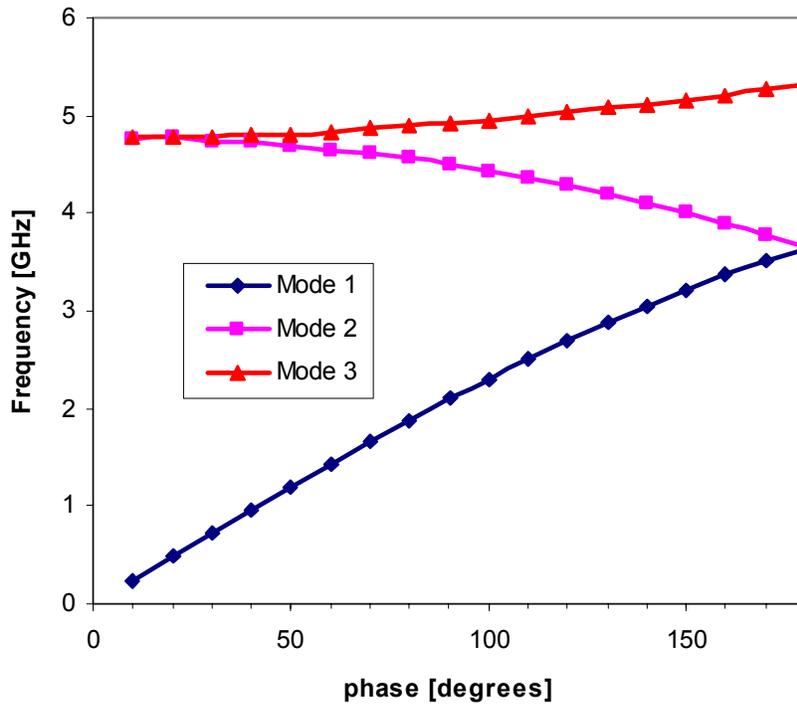


Figure 2-14: Dispersion diagram of nested plane 2. Only  $\Gamma$ -X portion is presented.

The dispersion diagram of the nested plane 2 is shown in Figure 2-14 for the first three modes. The first mode is a forward traveling surface-bound  $TM_n$  wave. The second

mode is a backward mode that coincides with the first mode in the X-M portion of the triangle. The third mode is a forward propagating TEn mode. For this power plane pair, the band-gap corner frequencies are not clearly defined.

Figure 2-15 shows the insertion loss of the two nested power planes along with that of a non-nested power plane (reference plane) of similar geometry. The emitting and receiving ports are placed at (5 cm, 2 cm) and (5 cm, 5 cm) respectively. The nested plane 1 has an effective shift of the upper corner frequency with respect to the reference structure. The lower corner frequency is about the same. The nested plane 2 exhibits a shift of the upper and lower corner frequencies towards lower frequencies with a simultaneous shrinking of the band-gap. The latter also shows some resonance mitigation at much lower frequencies, which corresponds to increased embedded capacitance between the ground and Vdd planes. This is even more important as decreasing the space between the patches will further increase the embedded capacitance and therefore eliminate the need for dissipative edge terminations. The insertion loss of the three power planes with the gap reduced from 1 mm to 0.2 mm is shown in Figure 2-16.

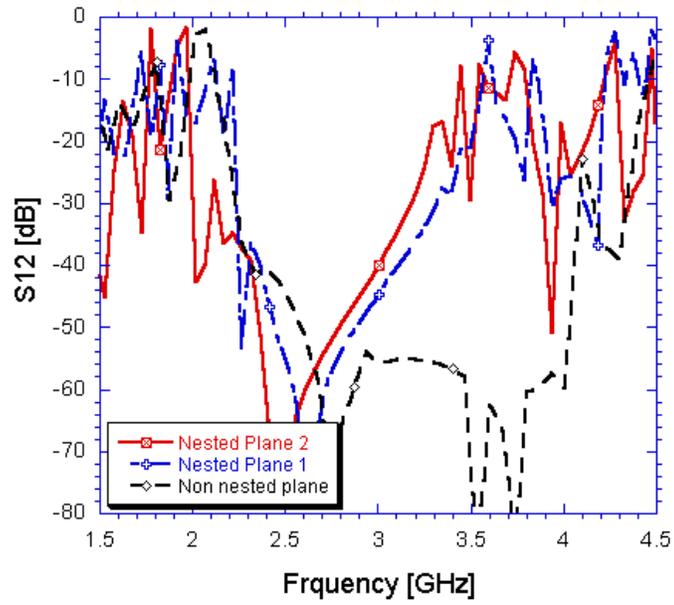


Figure 2-15: Insertion loss of nested vs. non nested power planes,  $g = 1$  mm.

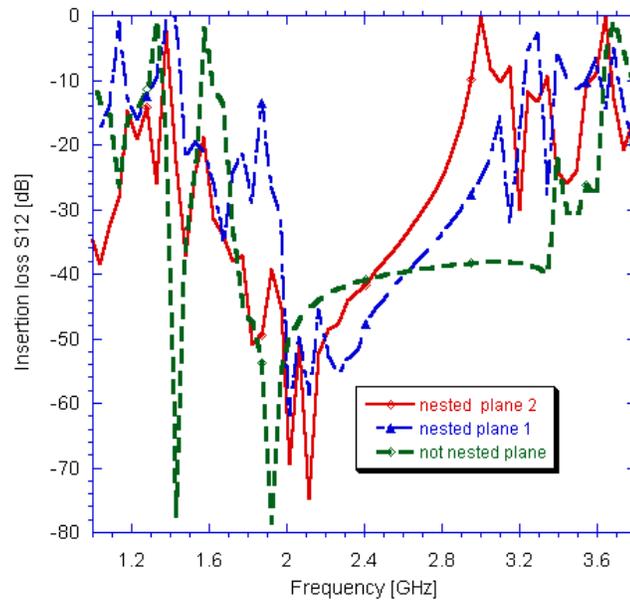


Figure 2-16: Insertion loss of nested vs. non nested power planes,  $g = 0.2$  mm.

## 2.5 Experimental verification

The concept of power planes with integrated standard HIS has been verified experimentally. Several structures with patch size varying from 2 mm to 20 mm and constant gap of 400  $\mu\text{m}$  have been fabricated and characterized using a two-port network analyzer. In the experimental setup the Vdd plane is a solid metallic plate and the Gnd plane only has 4 rows of HIS cells separating the emitting and the receiving ports as illustrated by the example of Figure 2-17. The thickness of the structure was 3.08 mm, which consists of 1.54 mm for the HIS and 1.54 mm for the distance between the HIS and Vdd plane. The fabrication was realized in a commercially available typical PCB technology. In Table 2-2 we summarize the measured power plane characteristics, which were also in good agreement with performance obtained from the simulated dispersion diagram.

Design Number	Patch Width (mm)	Lower corner Frequency (GHz)	Upper corner Frequency (GHz)	Bandwidth (GHz)	Relative Bandwidth
1	5	4.2	8.4	4.2	66%
2	6	3.6	7.1	3.5	65%
3	8	2.7	5.2	2.5	63%
4	10	2.2	4	1.8	58%
5	15	1.6	2.9	1.3	57%
6	20	1	1.75	0.75	54%

Table 2-2: Extracted characteristics of fabricated power planes with integrated high-impedance surface.  $g=0.4$  mm,  $t=d=1.54$  mm,  $\epsilon_r=4.1$ .

Measured S-parameters for a typical power plane are shown in Figure 2-18. There is a wide frequency bandgap between 2.2 and 4.0 GHz as expected for that geometry. The

signal transmission level is also very low at very high frequencies. This transmission drop, which is actually good for the resonance attenuation, can be primarily inferred to the resistive and dielectric losses.

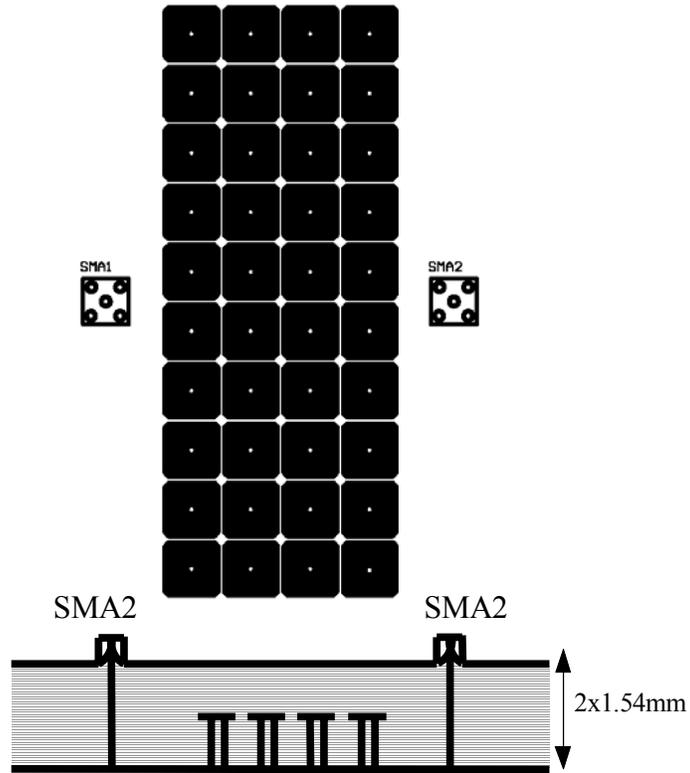


Figure 2-17: Experimental setup for power planes with integrated HIS. Measurement is performed using SMA connectors on both sides of the four HIS rows.

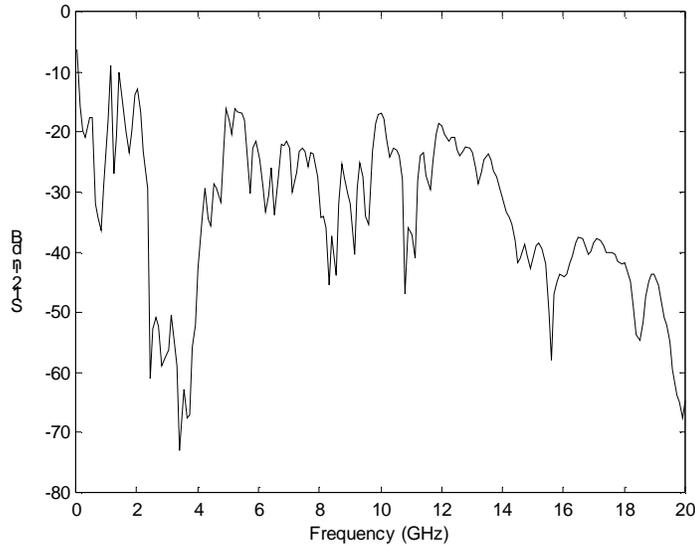


Figure 2-18: Measured insertion loss of a 10 cm x 10 cm power plane with cells of period 10 mm and gap of 0.8 mm.

## 2.6 Summary

A novel concept for mitigating simultaneous switching noise in power planes of high-speed circuits has been developed. The concept consists of replacing at least one plate of the power plane pair with a high-impedance electromagnetic surface. Simultaneous switching noise, which is reduced by mitigating the ground bounce observed in traditional power planes is strongly dependent on the frequency region, where the HIS has its forbidden band-gap. Contrary to the approaches reported previously in the literature, HIS can mitigate SSN in all directions and, therefore, represents a global solution. Using a systematic analysis, the impact of the geometrical parameters of the HIS on its ability to mitigate noise has been studied. Usually large lattice constants (or periods) and small gaps between the patches are required to achieve SSN immunity at very low frequencies. The concept of nested power planes, which consists of replacing both plates of the power plane

pair with high-impedance electromagnetic surfaces without increasing the PCB thickness (in comparison with planes with standard HIS on either Gnd or Vdd plane), has also been introduced. The latter provides a smaller bandwidth for noise mitigation and the bandgap is located between the second and third modes. In addition, the close proximity of the planes can lead to noise suppression at very low frequencies without use of DC decoupling capacitors.

## Chapter 3

# **Inductively-Tuned High-Impedance Electromagnetic Surfaces Integrated in Power Plane Environments**

### **3.1 Introduction**

High-impedance electromagnetic surfaces (HIS), as discussed in [15], have two fundamental limitations for low frequency designs. For a given technology, where the dielectric constant is fixed, a decrease in the center frequency can only be reached by increasing either the inductance per unit area or the capacitance per unit area. A substantial increase of the sheet inductance can only be reached by increasing the via height [54]. If the thickness of the substrate has to be kept minimum the latter approach is not optimum and the only remaining alternative is the enhancement of the per unit area capacitance, which can be obtained by increasing the period of the structures or by minimizing the gap or spacing between adjacent patches. In recent years, there has been substantial research work [58]-[62] towards the design of high-impedance electromagnetic surfaces (HIS) or electromagnetic band-gap structures (EBG) for low frequency designs, all of which was focused on enhancing the per unit area capacitance of the high-impedance surfaces. In [58] and [59] the capacitance enhancement was obtained by using double-layer patches. In this

case, the fringing capacitance between adjacent cells is comparable to that of the parallel-plate capacitors. For such structures a low-loss high-k dielectric constant can be used between the patches, while a high-loss dielectric is used in the other regions. Obviously the implementation of this approach in standard PCB technology requires an increase of the number of metal layers. In [59], the patches on the second layer were modified to concentric rings. This minimizes the area of the top patch that does not have a direct overlap with the patch of the first layer and therefore contributes less to the fringing capacitance. In [60] a two-layer HIS was designed with micro-electromechanical systems (MEMS) switches between the patches. External DC voltages were then used to tune the capacitance of the MEMS, which adds to the capacitance of the HIS to enhance the overall capacitance performance. In [61] and [62], the MEMS switch was replaced by other components with voltage variable capacitance such as varactors, MOS capacitors and PiN diodes in a single layer HIS. This capacitance enhancement led to devices with operating frequencies in the 1 to 2 GHz range, but the use of power to operate the HIS as well as the noise associated with active devices remains a major drawback. While most attention has been focused on designing for low frequencies, only little attention has been paid to the importance of the actual bandwidth as most designs such as antennas are usually narrowband. In designing HIS for application in power planes of high-speed circuits it is very important to examine the ability of these structures to mitigate SSN over a broad frequency range. In this case tradeoffs may be required between the per unit area inductance and the per unit area capacitance to meet both the center frequency and the bandwidth requirements.

This chapter introduces various novel concepts for designing high-impedance electromagnetic surfaces with forbidden frequency band-gap at low frequencies. These concepts are based on enhancing the inductance per unit area with little or no increase on the overall thickness of the board. All structures are primarily evaluated in conjunction with their application in mitigating simultaneous switching noise in parallel-plate power planes. In section 3.2 we discuss the concept of power planes with double-layer inductance-enhanced HIS and its combination with dissipative edge termination (DET) for broadband noise mitigation. Three types of power planes with single layer inductively-tuned high-impedance surfaces are discussed in section 3.3. Section 3.4 discusses the size optimization of HIS with spiral inductor patches to improve noise mitigation and increase the IC packaging density and the work is concluded in section 3.5.

## **3.2 Two-layer HIS with inductance-enhanced vias**

### *3.2.1 Power plane with inductance-enhanced vias*

The two-layer inductance-enhanced high-impedance surface is realized by replacing the straight via of the single-layer HIS with an inductive element such as the one illustrated in Figure 3.1. Its implementation in a power plane is shown in Figure 3.2. The inductive element consists of a single loop conductor, which is connected to the patch and the bottom metallic plate using an upper and a lower via respectively. The overall per unit cell or per unit area inductance enhancement due to the use of this element can roughly be approximated by the sum of the self-inductance in nanohenry (nH) of the individual segments (3.1) also known as Greenhouse formula [63]

$$L = \sum_{i=1}^n 2l_i \left\{ \ln \left[ \frac{2l_i}{w_i + t_i} \right] + 0.50049 + \frac{w_i + t_i}{3l_i} \right\} \quad (3.1),$$

where  $l_i$ ,  $w_i$ , and  $t_i$  represent the length in cm, the width in cm and the thickness in cm of each segment.  $N$  is the total number of segments. Depending on the size of the patches and the inductance per unit area requirement, the intermediate conductor, which is in effect an inductor, can be designed to have more (or even less) than one turn and can also be distributed on several layers without impacting the periodicity of the high-impedance surface. This is especially important if SSN mitigation below 1 GHz is desired. Since the area required by the inductor is very small, unwanted inductive coupling with adjacent cells is also minimized. In a power plane environment the HIS with multi-turn spiral inductor is expected to behave similarly to power planes using HIS with long single-loop inductor as both approaches mainly contribute to an increase in inductance.

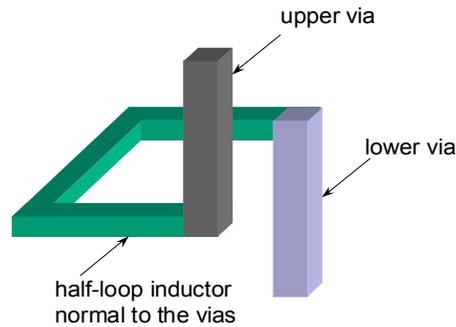


Figure 3-1: Single-loop inductive element for inductance enhancement.

This novel concept of extending the conductor in the direction perpendicular to the via achieves the following two important objectives:

- It allows increased inductance without increasing the overall PCB thickness.
- It introduces a degree of freedom that allows fine-tuning of the inductance while keeping the capacitance constant.

By using a multi-turn or spiral inductor, the inductance per unit area is increased significantly. In fact the total inductance per unit cell increases to

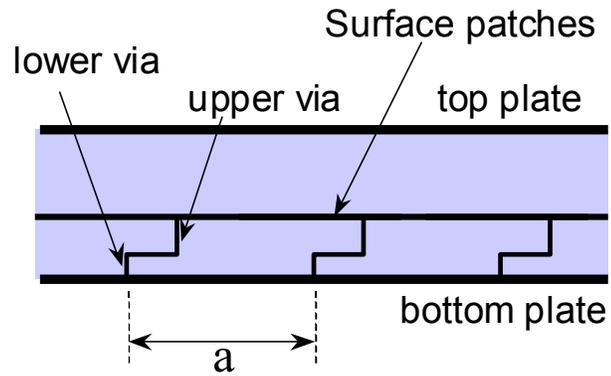
$$L_t = L + M \quad (3.2),$$

where L is the self inductance of the individual segments given by equation (3.1) and M is the total mutual inductance between the individual segments of the inductor. The mutual inductance between two parallel coplanar metal segments (of the spiral inductor) is given by equation (3.3) and is equal to zero when the segments are orthogonal. In addition  $m_{ij}$  is negative when the current in the segments flows in opposite directions, such that for a square spiral inductor segments on the same site have positive mutual inductance between them and segments on opposite side have negative mutual inductance between them.

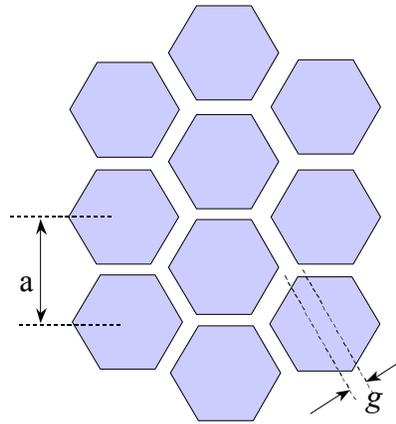
$$m_{ij} = 2l_{ij} \left\{ \ln \left( \frac{1}{d_{ij}} + \sqrt{1 + \frac{l_{ij}^2}{d_{ij}^2}} \right) - \sqrt{1 + \frac{d_{ij}^2}{l_{ij}^2}} + \frac{d_{ij}}{l_{ij}} \right\} \quad (3.3)$$

In equation (3.3)  $l_{ij}$  is the length of the segments and  $d_{ij}$  is the center-to-center distance between the parallel segments i and j. From equation (3.3) the total mutual inductance can be calculated as (3.4)

$$M = \frac{1}{2} \sum_{i=1}^n \sum_{j=1}^n m_{ij} \quad (3.4).$$



(a)



(b)

Figure 3-2: (a) Cross section and (b) top view of power plane with double-layer inductance-enhanced HIS.

The performance of the power plane with two-layer inductance-enhanced HIS was evaluated by considering a 10 cm x 10 cm power plane. The total thickness of the power plane including HIS was fixed at 1.54 mm. This corresponds to upper and lower via heights of 0.5 mm and a substrate of thickness 0.5 mm between the top of the HIS and the top plate. Square patches were used with the separation between adjacent patches fixed at 0.4

mm. The substrate was lossless FR4 of dielectric constant 4.4. Copper was used as conductor material. The period was 10 mm and the ports located at (4.5 cm, 1.5 cm) and (4.5 cm, 4.5 cm). Here the ports were between the Vdd plane and the top of the HIS. Different simulations were then performed with the length of the single-loop conductor varying from 5 mm to 16 mm. Figure 3.3 shows the insertion loss for the two extreme cases. If we consider the -30 dB bandwidth as the stop-band of the power plane, we notice that the fractional bandwidth increases with the loop length. At the same time there's a decrease in the bandwidth, suggesting that for any given structure the noise mitigation capability would also "saturate" as the inductance increases. More importantly, resonance suppression is achieved down to 700 MHz without any major increase of the power plane thickness. It is also important to point out that the location and width of the stop-band would vary if the ports are between the Vdd plane and the bottom of the HIS.

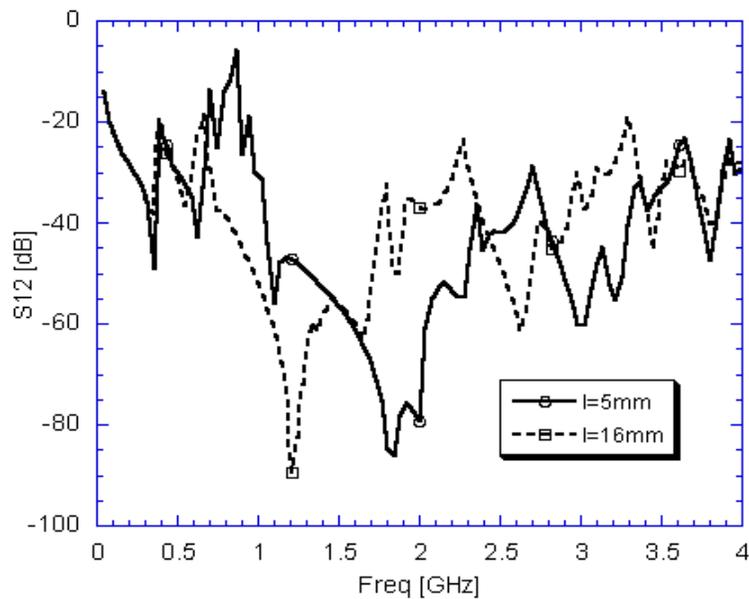


Figure 3-3: Effect of inductor loop length on insertion loss.

### 3.2.2 Combination of HIS with dissipative edge termination (DET)

In power planes with finite dimensions, the low-inductance bypass capacitance of the planes is of vital importance in mitigating simultaneous switching noise. But this bypass capacitance does not mitigate resonances induced by standing waves and edge radiation, which are very pronounced at very low frequencies. Inherent dielectric and conductor losses can help mitigate these resonances up to a certain extent [64]-[66]. These resonances can also be reduced by using either capacitive or resistive terminations along the edge of the PCB. In [67], a design methodology was proposed for the determination of dissipative edge termination for traditional power planes. The dissipative edge elements consist of series  $R_e C_e$ , where  $C_e$  acts as a decoupling capacitor between the Vdd and the ground planes since they have to be at different potential, and  $R_e$  is selected according to equation (3.5)

$$R_e = 2Z_{0u} \quad (3.5),$$

where  $Z_{0u}$  is the characteristic impedance of a square unit cell given by

$$Z_{0u} = 120\pi \frac{h}{W_u \sqrt{\epsilon_r}} \quad (3.6).$$

In (3.6),  $h$  is the height of the power plane pair and  $W_u$  is the width of the unit cell. To assure effective termination up to a given frequency  $f_0$ , the spacing  $W_u$  between the termination components, which is also the width of the unit cell, has to be smaller than 10% of the wavelength at the highest frequency  $f_0$  of interest and  $R_e$  has to be less than the impedance  $\omega_0 L_e$  of the parasitic edge inductance associated with the discrete. As it was

discussed in the previous chapter the parasitic inductance associated with the components is fixed, but the value of  $R_e$  varies with  $W_u$  according to (3.5)-(3.6).

As it is shown in Figure 3.4 the inductance-enhanced HIS can mitigate SSN down to the low GHz frequencies, but there is still a very strong resonance close to DC frequencies. In order to evaluate the impact of dissipative edge termination on power planes with integrated HIS, we consider a 10 cm x 10 cm power plane of type shown in Figure 3.2. The upper and lower vias are of length 1 mm each. The period of the lattice is 10 mm and the gap between the hexagonal patches,  $g$ , is 0.4 mm. The top plate is placed 1 mm above the patches. The transmission characteristics  $S_{12}$  are plotted together with those of a simple parallel-plate structure of same height with and without a wall of RC pairs placed around the edges of the board (the inductance of the capacitor leads,  $L_e$  is included as before) in Figure 3.4. A total of 40  $R_e C_e$  pairs were uniformly placed around the PCB, with  $R_e=5.36$  Ohms and  $C_e=1$  nF and  $L_e=0.5$  nH. The resistance of the RC combination is selected to match the impedance of the simple parallel- plate system as in [68]. The wall of capacitors offers a good SSN mitigation capability at lower frequencies. For higher frequencies, however, the noise suppression capability of the HIS is remarkable. In fact, the frequency width of the resulting -20 dB band-gap is approximately 3.3 GHz. Over the band-gap, the HIS significantly diminished the surface waves that travel within the plates, which in turn results in significantly reduced  $Q$  for the parallel-plate cavity.

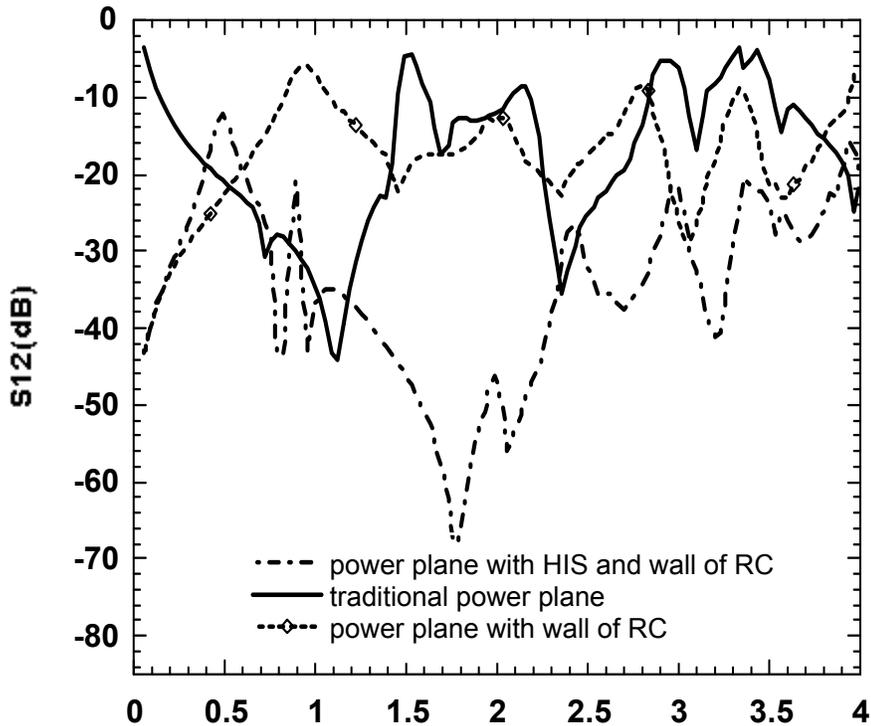


Figure 3-4: Transmission characteristics of a 10 cm x 10 cm power plane with RC dissipative edge termination and combination of RC dissipative edge termination and HIS.

### 3.3 Power planes with single-layer inductive-enhanced high-impedance surfaces

The fundamental idea behind the single-layer inductance enhanced HIS consists of bringing the inductance-enhancing loop (or its equivalent) to the same layer as the patch and in series with the via. This would result in an effective increase of the via inductance. For very low frequency design and bandwidth considerations a substantial increase in inductance per unit area should not always lead to a strong decrease of the per unit area capacitance. The structures considered in this section all have a period of 10 mm with a gap or spacing of 1 mm between adjacent patches. The substrate is lossless FR4 of dielectric

constant 4.4 and the thickness of a single layer is 1.54 mm. For the power plane or parallel-plate waveguide configuration, this is equivalent to a total thickness of 2 layers, where one layer is used for the HIS and the other layer is the substrate between the Vdd and the ground planes. The conductor material is perfect conductor. The initial analysis of the structures is done by calculating the dispersion diagram based on the unit cell as it was described in section 1.8.1.

### *3.3.1 Power planes using single-layer cross structure*

#### *3.3.1.1 Structure topology*

The top-view of the cross structure unit cell is shown in Figure 3.5. It is realized by altering the patch of the standard Sievenpiper structure at its center to include a metallic cross. The cross fingers can be considered as narrow transmission line segments, whose inductance effectively adds to that of the via to increase the total sheet inductance or inductance per unit area. For fixed via height, period and gap, the impedance of the surface can be controlled by varying  $n_f$ ,  $w_f$ ,  $l_f$  or  $g_f$ , which represent the number, width, length of fingers as well as the gap between the finger and the rest of the patch as illustrated in Figure 3.5. Small finger width and large  $g_f$  both increase the sheet inductance. It can also be expected that the qualitative effect of the period and patch separation will be similar to that of the standard HIS.

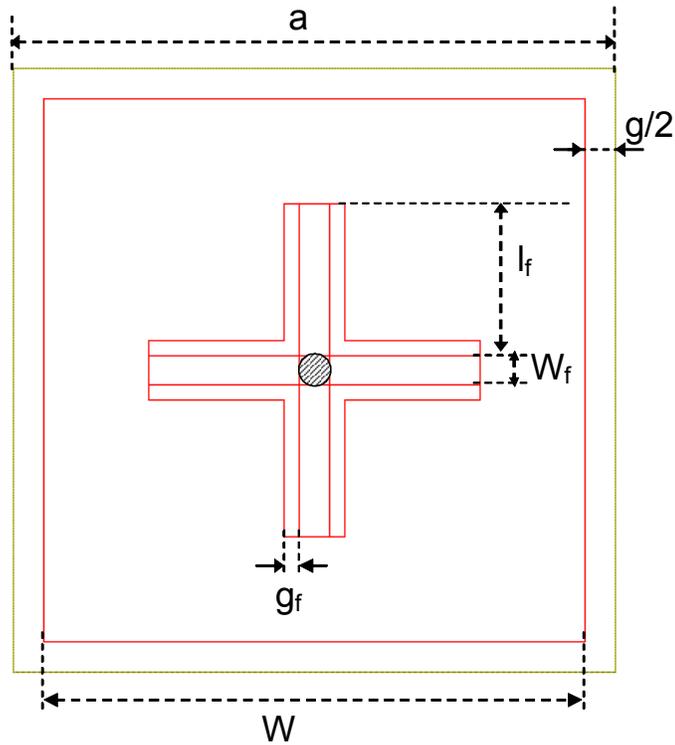


Figure 3-5: Top view of the cross structure unit cell with design parameters indicated. The circle at the center is the via connecting to the bottom plate.

### 3.3.1.2 Structure simulation and discussion of results

The effect the number of fingers on the power plane performance was evaluated using electromagnetic (EM) simulation, where the  $\Gamma$ -X portion of the dispersion diagram was calculated for three structures having  $n_f=4, 2$  and  $1$  as variable, while the other parameters were fixed at  $l_f=2.5$  mm,  $g_f=0.25$  mm,  $W_f=0.5$  mm,  $W=9$  mm and  $g=1$  mm. Figure 3.6 shows the dispersion diagram of the structures, where only the first two modes that determine the location of the band-gap (or stop-band) are plotted. The resulting stop-band locations are summarized in Table 3.1. When the number of fingers is equal to 4, the

4 transmission line segments are electrically almost in parallel, leading therefore to an inductance contribution that is comparable to one fourth of the inductance of a single finger. The inductance is maximal, when the number of fingers is equal to one. In this case the center frequency has the lowest value, as expected.

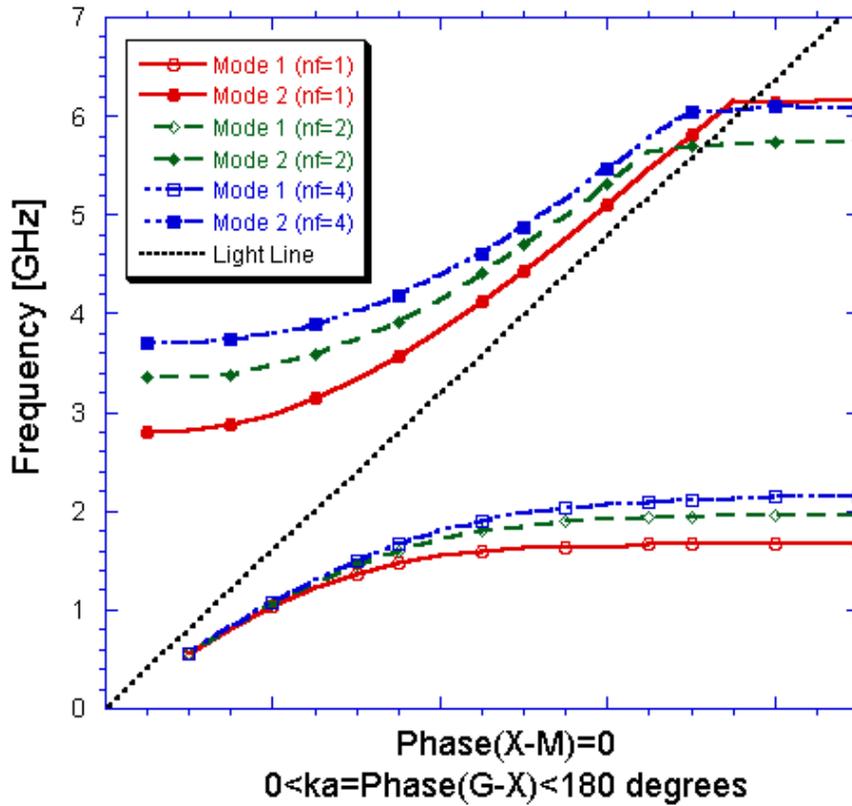


Figure 3-6: Effect of number of fingers on the stop-band location and width. Filled symbols correspond to upper band edge, whereas non-filled symbols correspond to lower band edge,  $l_f=2.5$  mm,  $g_f=0.25$  mm,  $W_f=0.5$  mm,  $W=9$  mm,  $g=1$  mm.

Structure ID	Number of fingers	Lower corner frequency [GHz]	Upper Corner Frequency [GHz]	Bandwidth [GHz]
Cross 1	4	2.14	3.7	1.56
Cross 2	2	1.97	3.4	1.43
Cross 3	1	1.67	2.8	1.13

Table 3-1: Summary of the location and width of the band-gap of power planes with single-layer cross high-impedance surface,  $l_f=2.5$  mm,  $g_f=0.25$  mm,  $W_f=0.5$  mm,  $W=9$  mm,  $g=1$  mm.

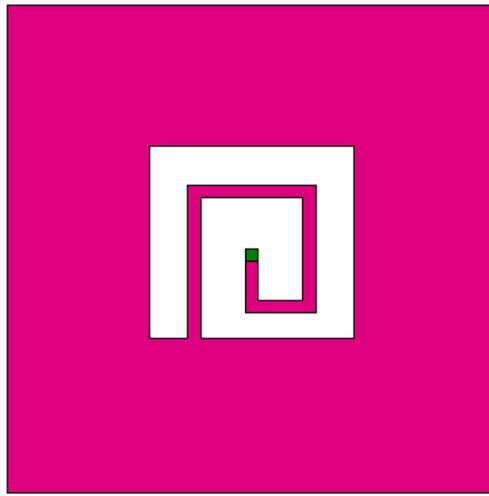


Figure 3-7: Top view of unit cell of single-layer of HIS unit cell with closed loop spiral.

### 3.3.2 Power planes using single-layer HIS with closed loop spiral as patch

#### 3.3.2.1 Structure topology

Figure 3.7 shows the top view of the general topology of the patch used in the high-impedance electromagnetic surface with closed loop spiral. It is obtained by opening a hole at the center of the patch of the standard Sievenpiper's cell, where a spiral inductor is inserted. The spiral inductor has one end connected to the via and the other end connected to the rest of the patch. An estimate of the inductance enhancement due to the spiral can be

obtained from equation (3.4). The surface impedance can be controlled by varying the geometrical parameters of the inner inductor, which the inner diameter, the number of turns, the line width and the line spacing. In order to achieve a large inductance value with simultaneously large fringing capacitance, the outer turn or loop has to maintain a large width, whereas the inner spiral inductor should have narrow metal traces, with narrow spacing between the turns as well as a large number of turns. As the number of turns of the spiral inductor increases the surface inductance increases very fast, leading to the lowering of the center frequency. At the same time there is a decrease in the absolute bandwidth. In order to achieve wideband design at low frequencies, the high number of turns can be combined with a smaller period as will be shown in section 3.4.

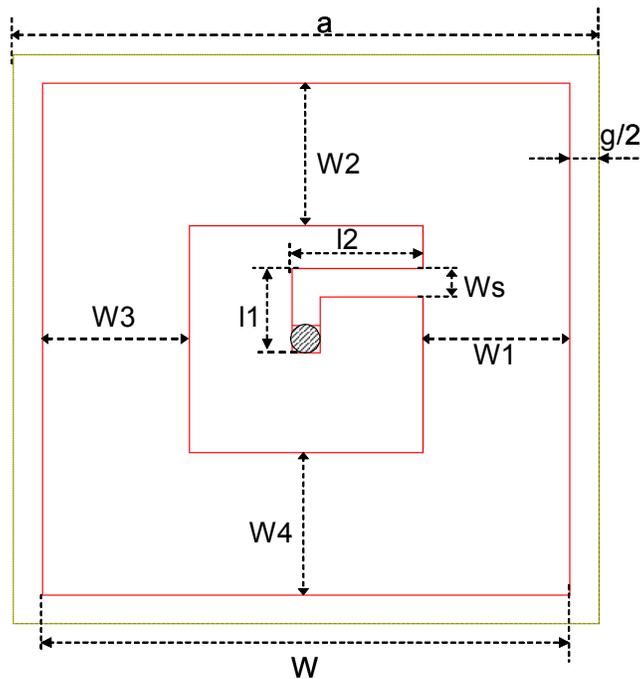


Figure 3-8: Implementation of the single-layer HIS with closed loop for a lattice constant of 10 mm.

### 3.3.2.2 *Simulation and discussion of results*

The initial validation of the concept was done by simulating the structures based on the unit cell of Figure 3.8, where the spiral inductor is limited to two transmission line segments. The detailed geometrical parameters were  $W=9$  mm,  $g=1$  mm,  $a=10$  mm,  $W_1=3.5$ ,  $W_2=W_3=W_4=2.5$  mm,  $l_1=1.5$  mm,  $l_2=2$  mm,  $W_s = 0.5$  mm. A much significant increase of the inductance would result in a stop-band that is in the hundreds MHz range. The  $\Gamma$ -X section of the dispersion diagram was calculated and is shown in Figure 3.9. Figure 3.10 shows the insertion loss of a parallel-plate power plane based on a  $10 \times 10$  array of the unit cell of Figure 3.9. Here the distance between the transmitting and receiving ports was 30 mm or three unit cells. Both graphs show that power planes with this HIS would provide parallel-plate mode immunity in the frequency range from 1.7 GHz to 2.7 GHz, which is a much lower frequency range than that of power planes with standard HIS of same period, gap and material properties.

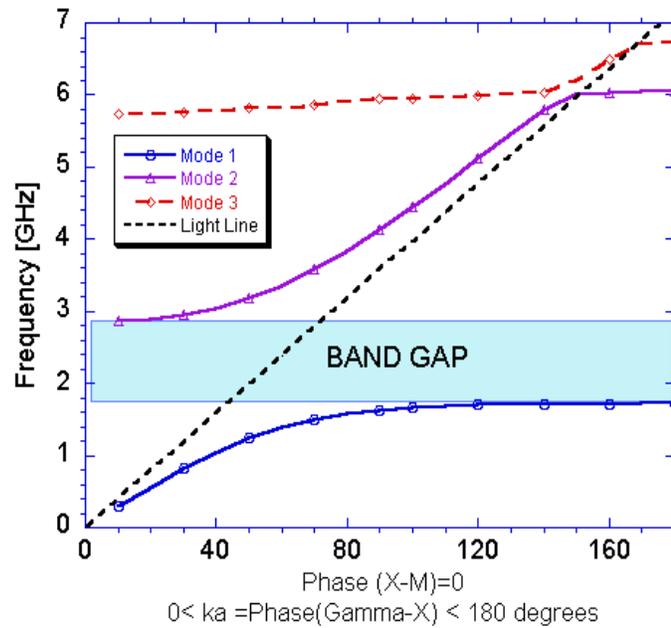


Figure 3-9: Dispersion diagram of power plane using single-layer HIS with outer loop closed spiral.  $W=9 \text{ mm}$ ,  $g=1 \text{ mm}$ ,  $a=10 \text{ mm}$ ,  $W_1=3.5$ ,  $W_2=W_3=W_4=2.5 \text{ mm}$ ,  $l_1=1.5 \text{ mm}$ ,  $l_2=2 \text{ mm}$ ,  $W_s=0.5 \text{ mm}$ .

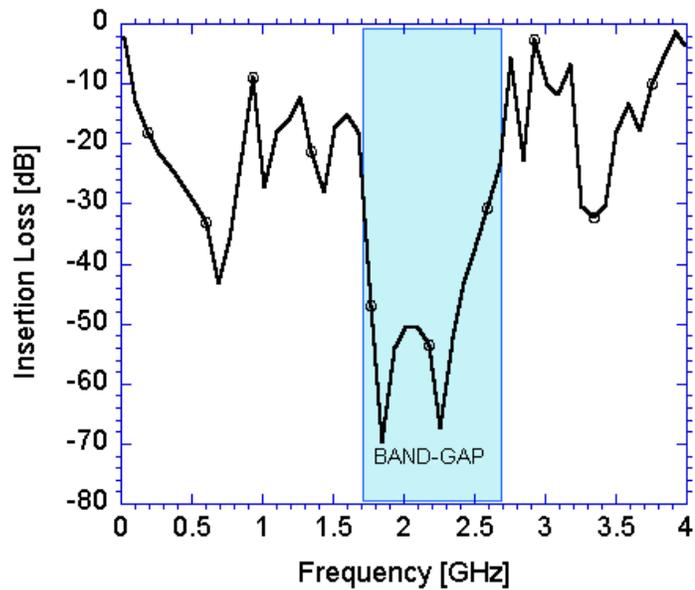


Figure 3-10: Insertion loss of structure with closed open loop,  $W=9 \text{ mm}$ ,  $g=1 \text{ mm}$ ,  $a=10 \text{ mm}$ ,  $W_1=3.5$ ,  $W_2=W_3=W_4=2.5 \text{ mm}$ ,  $l_1=1.5 \text{ mm}$ ,  $l_2=2 \text{ mm}$ ,  $W_s=0.5 \text{ mm}$ .

### 3.3.3 Power planes using HIS with open loop spiral inductors as patch

#### 3.3.3.1 Structure topology

Figure 3.11 shows the top view of the patch used in the HIS with open loop spiral inductor. It is obtained by opening the outer loop of the structure of Figure 3.7. The surface impedance is controlled by varying the geometrical parameters of the spiral inductor, which include the inner diameter, the line width, the line spacing and the number of turns.

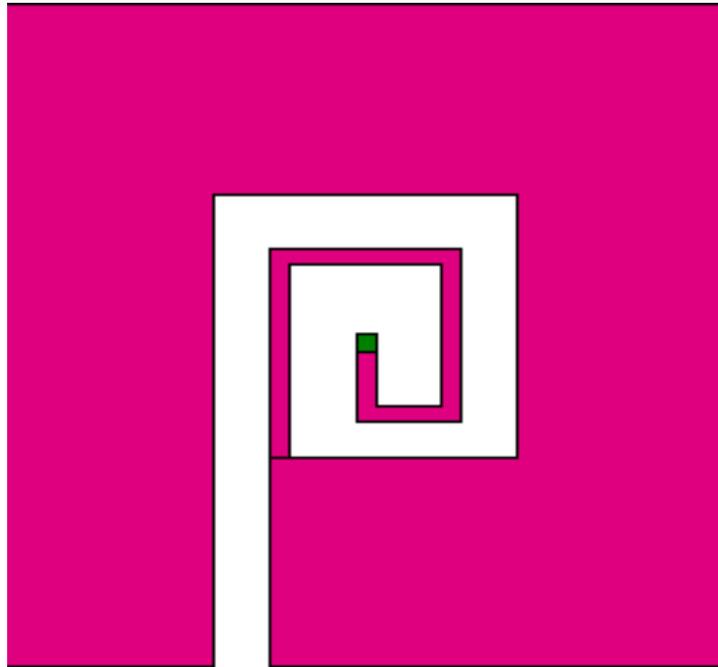


Figure 3-11: Top view of HIS unit cell with open loop spiral inductor as patch.



minimum in the insertion loss curve at 2.6 GHz. A direct comparison with the dispersion diagram indicates that this frequency point does not represent a narrow stop-band, but it is rather the frequency point, where the second mode starts to transition from a predominantly TE wave to a predominantly TM wave. At this frequency point the second mode is a pure TEM mode as it intercepts the light line in the medium. This is further illustrated in the  $\Gamma$ -X portion of the dispersion diagram of Figure 3-15.

The first mode is a  $TM_n$  mode, which is a surface bound wave. It starts as a forward propagating TEM mode at very low frequency and low wave number, and transitions to a forward propagating TM surface wave. At very high wave numbers a slight decrease in the group velocity of this mode indicates that it is propagating backward. The second mode is a hybrid mode, which starts as a TE wave at very low wave number and behaves like a TM wave at very high wave number. The third mode is a pure TE wave.

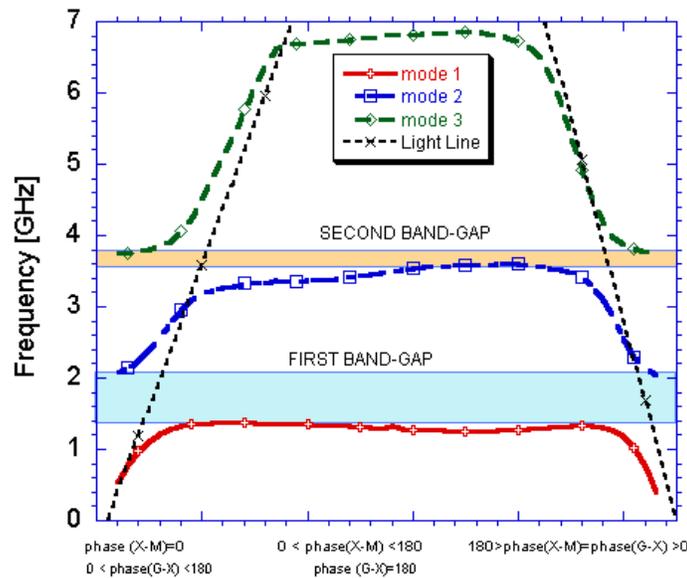


Figure 3-13: Full band-structure of a power plane with open loop spiral inductor as HIS' patch.

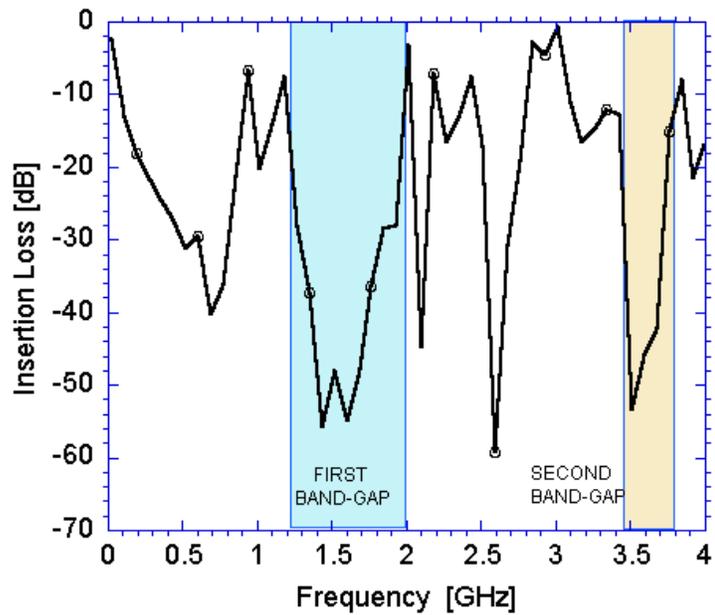


Figure 3-14: Insertion loss of the structure with open outer loop. A 10 cm x 10 cm power plane was considered with a separation of 3 cm between the emitting and receiving ports.

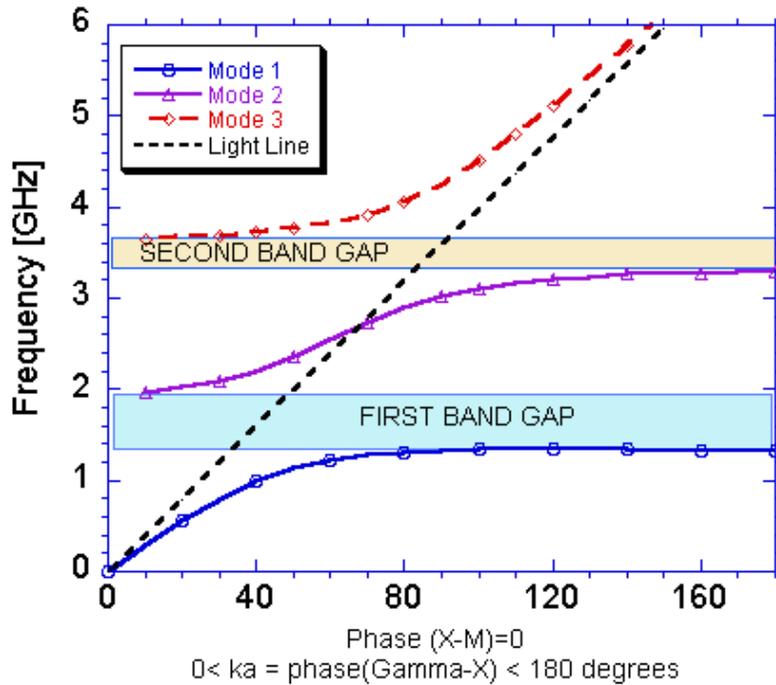
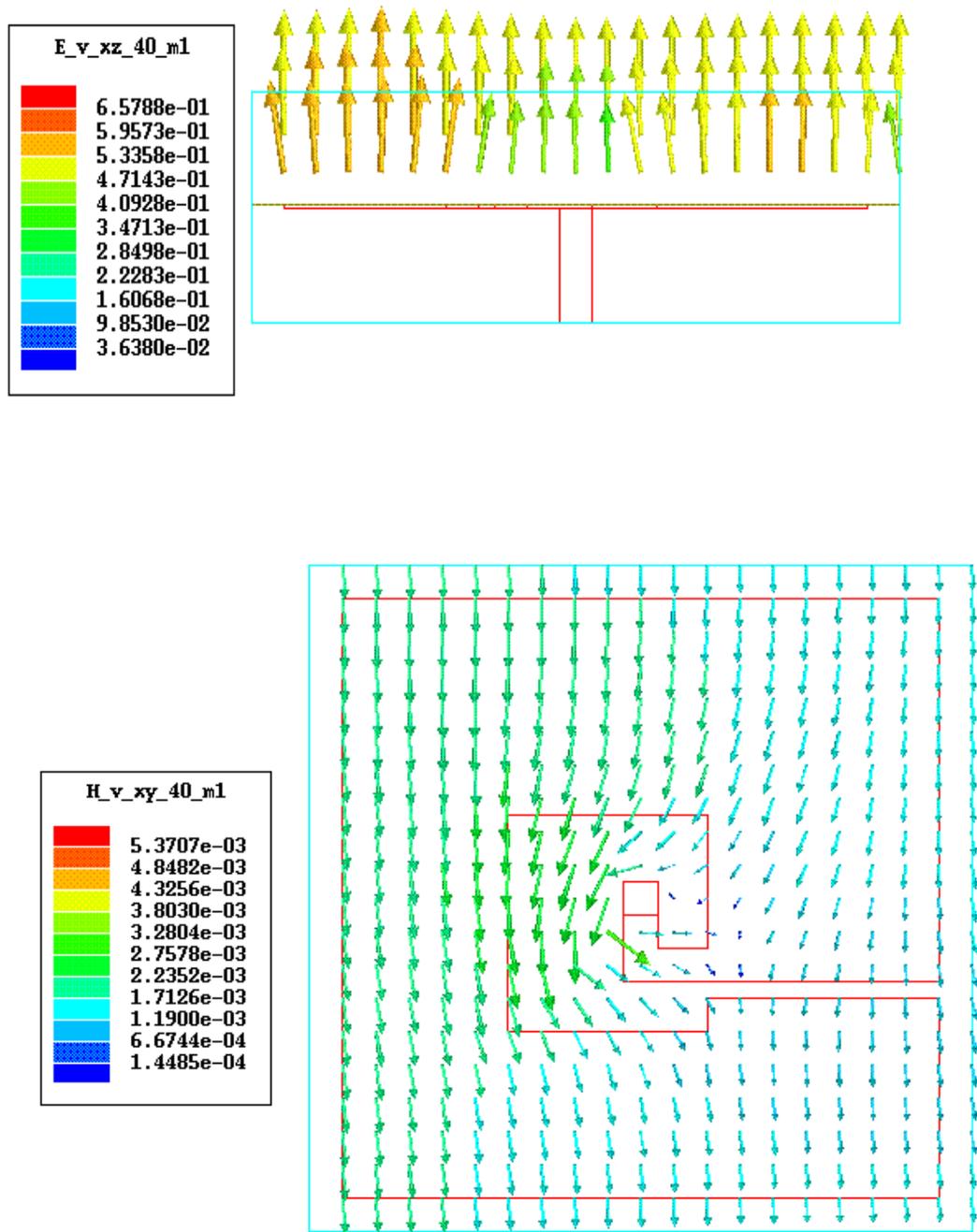


Figure 3-15: Dispersion diagram of the structure with open outer loop.

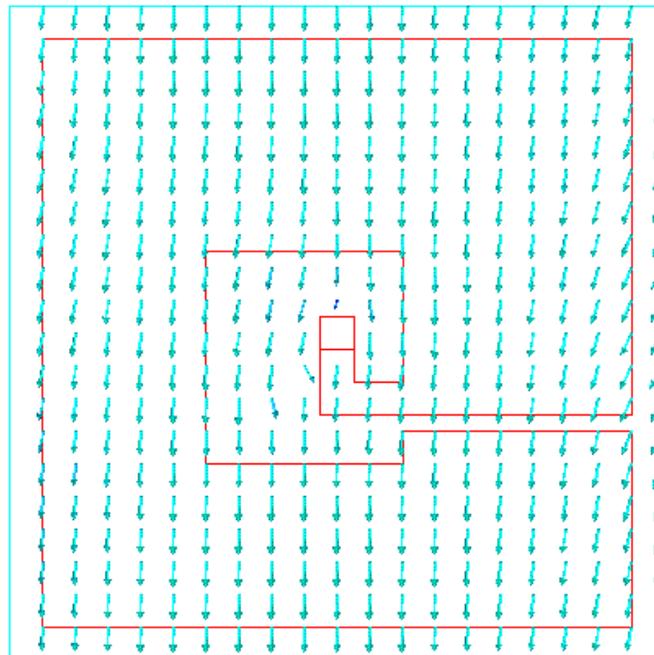
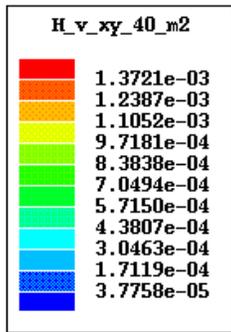
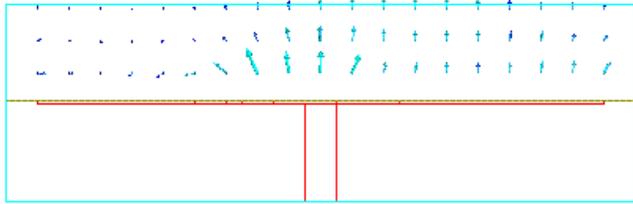
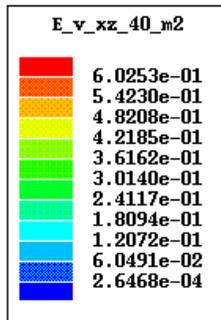
More insights on the nature of the propagating waves can be gained by looking at the electrical and magnetic field plots between the top of the HIS and the Vdd plane for different wave numbers. Based on the  $\Gamma$ -X section of the dispersion diagram three different wave numbers have been selected to capture the three regions of the second mode. Table 3.2 summarizes the eigenmode solutions for these three wave numbers. The dominant field modes are obtained after comparison of the field intensity in x-, y- and z-directions are shown in Figure 3-16a-h.

Phase angle[degrees]	Mode 1 [GHz]	Mode 2 [GHz]	Mode 3 [GHz]
40	0.99	2.17	3.7
70	1.28	2.72	3.9
110	1.365	3.124	4.82

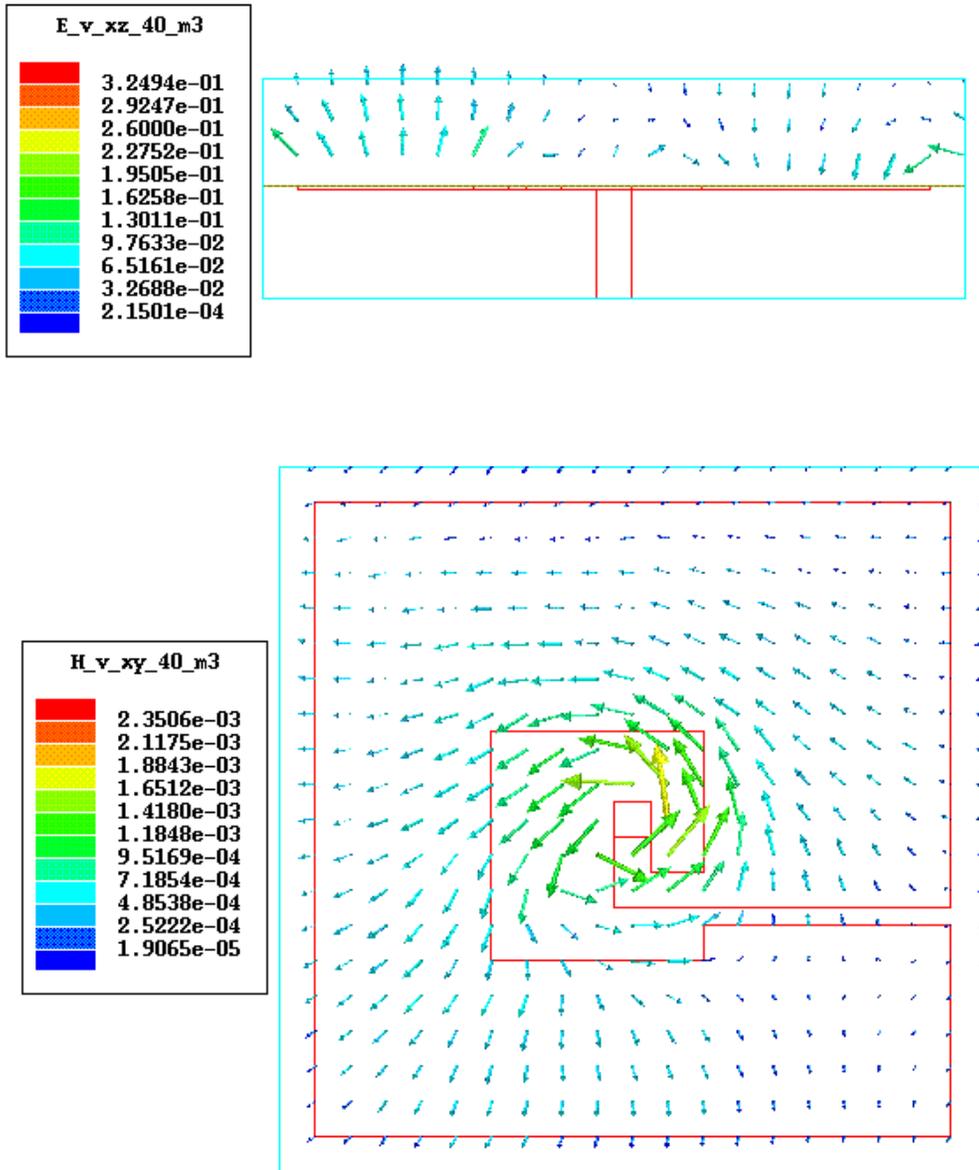
Table 3-2: Eigenmode solutions of the parallel-plate power plane using HIS with open outer loop open spiral inductor.



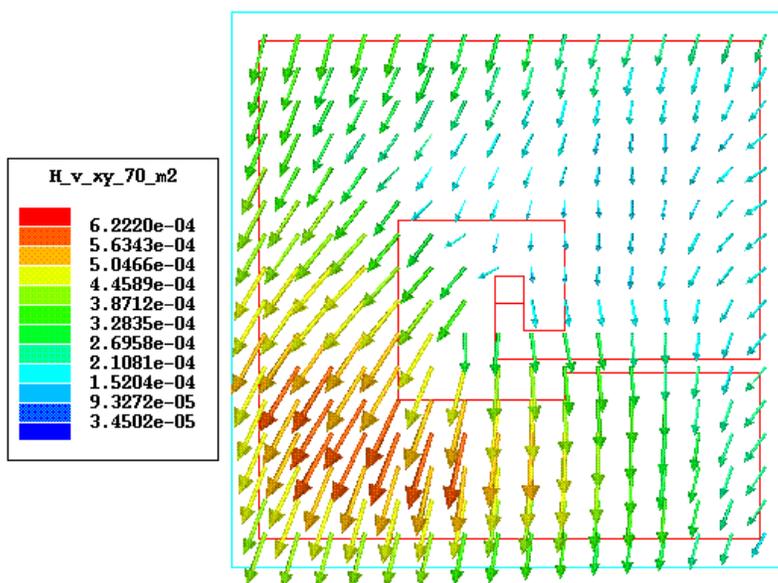
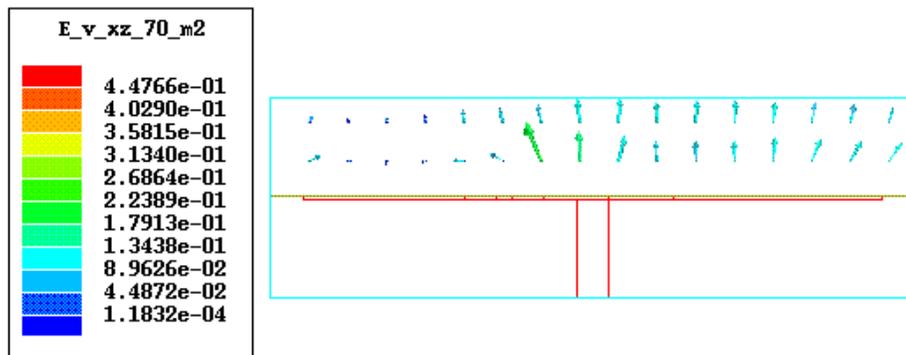
(a) Electric and magnetic fields of mode 1 at 40 degrees.



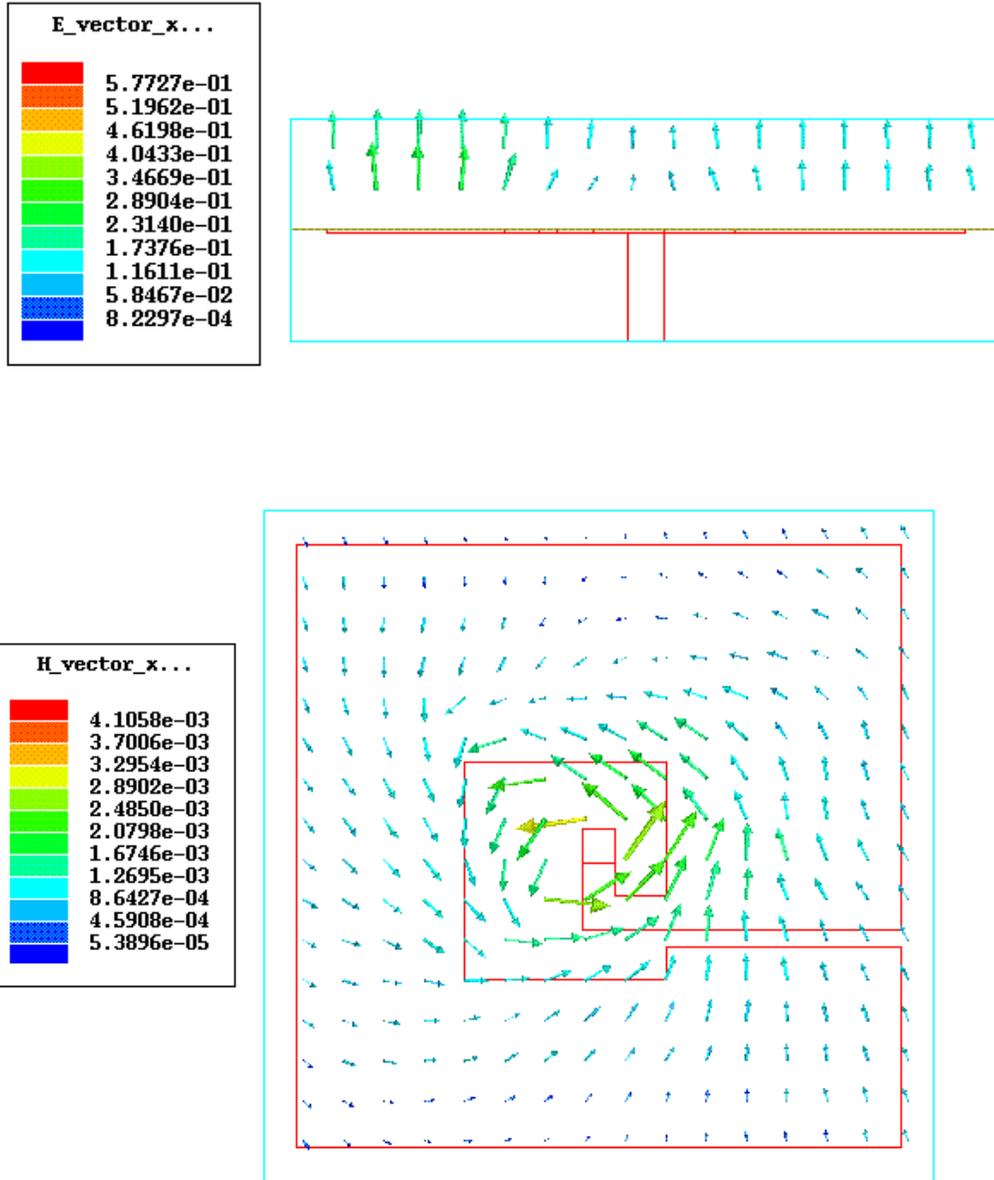
(b) Electric and magnetic fields of mode 2 at 40 degrees.



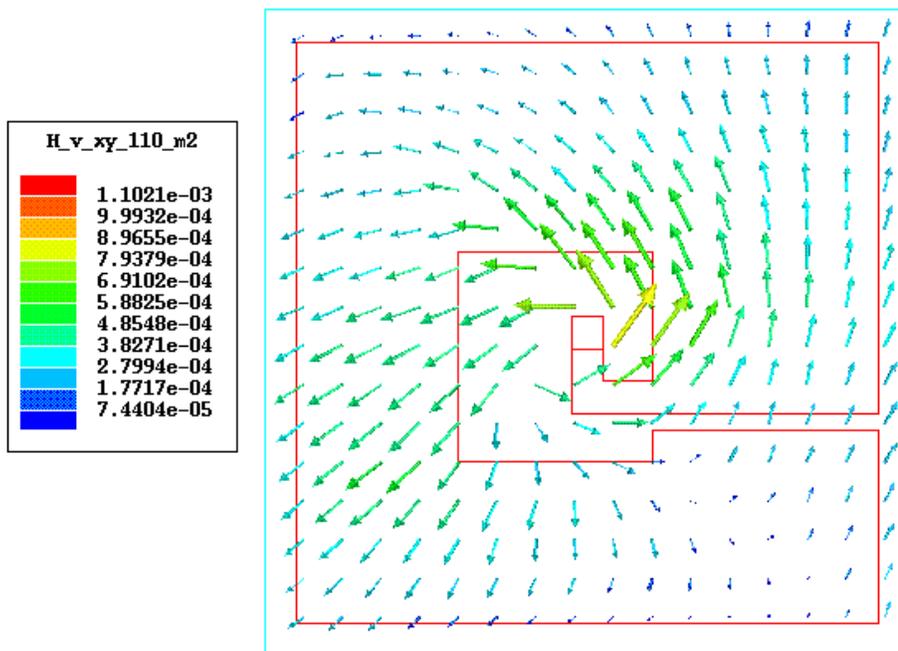
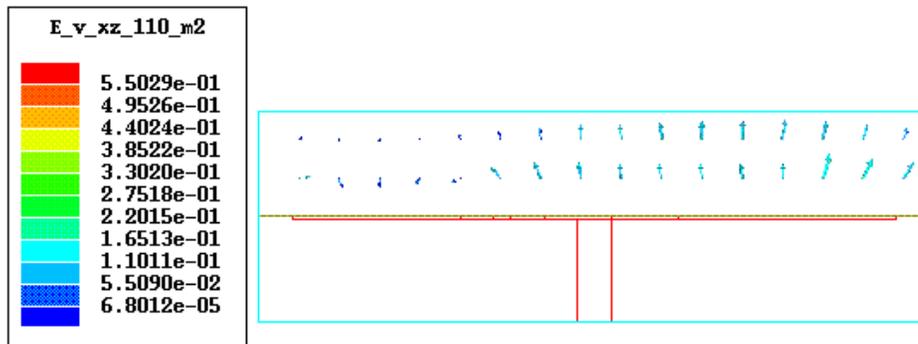
(c) Electric and magnetic fields of mode 3 at 40 degrees.



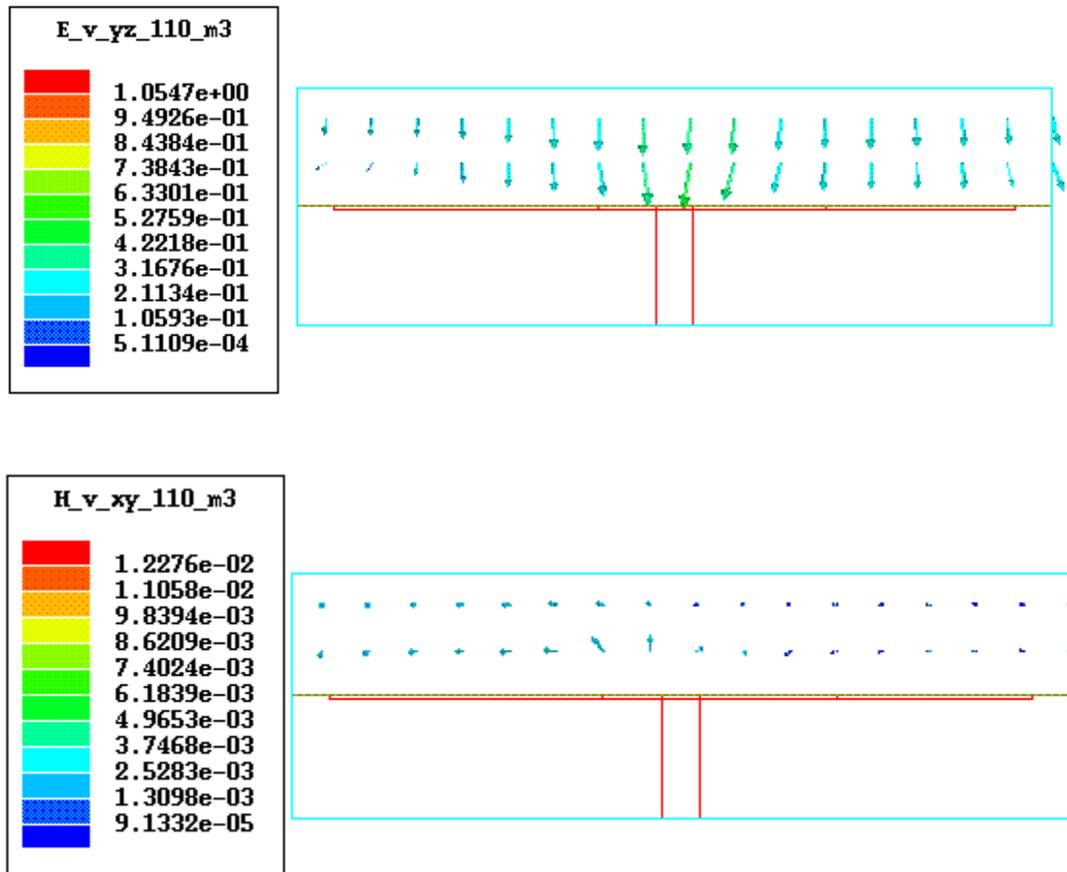
(d) Electric and magnetic fields of mode 2 at 70 degrees.



(e) Electric and magnetic fields of mode 1 at 110 degrees



(f) Electric and magnetic fields of mode 2 at 110 degrees



(h) Electric and magnetic fields of mode 3 at 110 degrees

Figure 3-16 (a)-(h): Electromagnetic field plots at different phase angles

### 3.3.3.3 Effect of varying the location of the outer-loop slot

The variation of the width,  $s$ , of the slot from 0.1 to 1 mm does not show a significant difference on the performance of the power plane. The relative location of the slot on the outer loop was changed to the opposite site. Table 3.3 summarizes the relative position of the band-gap. For comparison the attributes of the same structure without slot are also included.

Description of outer loop	a [mm]	W1-4 [mm]	Band-gap 1 [GHz]	Band-gap 2 [GHz]
closed	10	2.5	1.52-2.46	None
open	10	2.5	1.15-173	3.24-3.5
open on opposite side	10	2.5	1.49-2.35	2.74-2.83

Table 3-3: Relative position of the outer loop slot on the location and size and band-gaps,

$W_s=0.5$  mm,  $l_1=1.5$  mm,  $l_2=2.25$  mm,  $g=1$  mm.

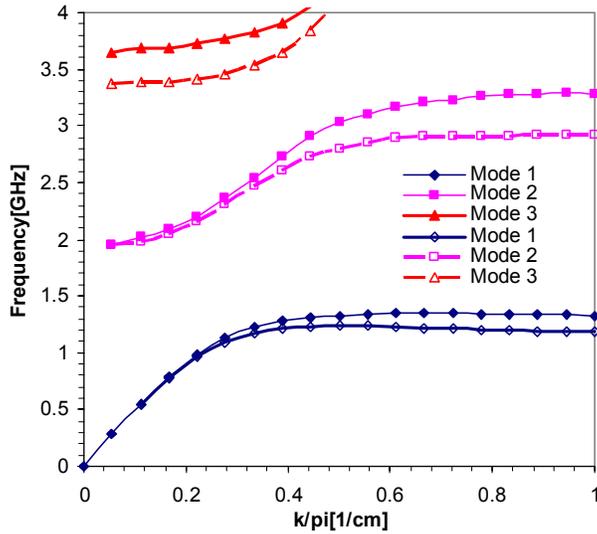


Figure 3-17: Effect of varying the gap size on the dispersion diagram of the power plane using an open loop spiral inductor as patch.

### 3.3.3.4 Effect of the gap width

Figure 3.17 shows the dispersion diagram of the cell, where the patch separation  $g$  between adjacent patches has been varied from 1 mm to 0.4 mm. This is done by increasing

the width of the outer loop of the spiral inductor. The upper band moves towards lower frequencies with a slight variation in the bandwidth, whereas the lower band is only slightly affected. When the gap between patches is very large a second band-gap is generated. As the size of the gap decreases, the 3<sup>rd</sup> mode moves faster towards lower frequencies and at about the same rate across the entire spectrum (wave numbers). The second mode also moves towards lower frequency. This shift is more pronounced at higher frequencies. Since the second mode shifts much slower, the second band-gap will eventually disappear. In general the changes in the fundamental or first band-gap are negligible. With the decrease of the gap there is a strong capacitive (and even inductive) coupling between the patches.

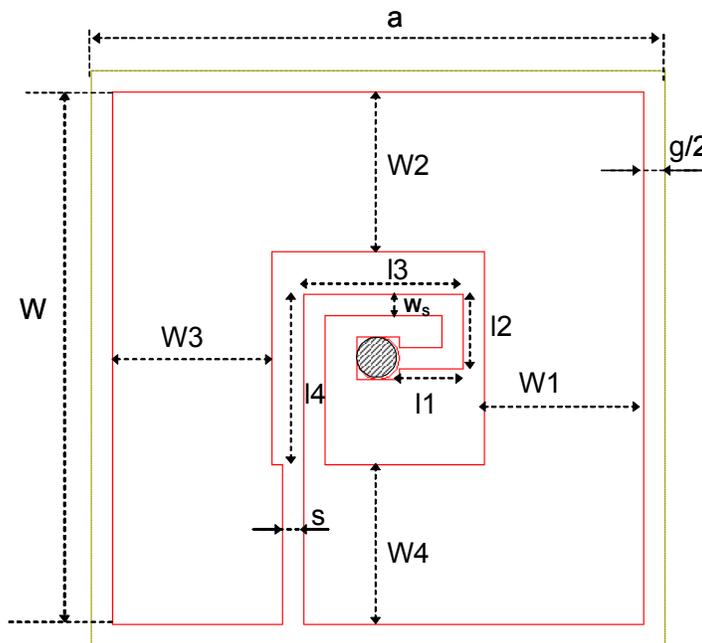


Figure 3-18: Top view of unit cell used to study the impact of the gap (between patches) on the frequency response of the power plane.

A further study of the effect of the gap was performed by studying the structure of Figure 3.18, where the portion of the inductor with the smaller line width has been extended to a full turn. The width and location of the stop-bands are summarized in Table 3.4. It can be seen that when the gap goes beyond a certain value the second band-gap vanishes.

Structure	A [mm]	G [mm]	W1-4 [mm]	Ws [mm]	Band-gap 1 [GHz]	Band-gap 2 [GHz]
1	5.4	1.2	1.1	0.2	2.12-3.1	6.55-8.89
2	5.4	0.6	1.4	0.2	1.94-3.1	6.2-6.2
3	5.4	9.4	1.5	0.2	1.89-3.1	None
4	10	5.2	1.4	0.2	1.9-2.26	5.8-6.14
5	10	0.6	3.9	0.2	1.1-1.8	None

Table 3-4: Effect of the gap size on the location and width of the band-gaps,  $l_1=0.6$  mm,  $l_2= 0.7$  mm,  $l_3=1.5$  mm,  $l_4= 1.6$  mm,  $s=0.2$  mm.

### 3.4 Design of power planes using high-impedance electromagnetic surfaces with a period of 5 mm

In the previous sections the concept of power planes with single-layer inductively-tuned HIS was demonstrated using cells with a period of 10 mm. As it was reported in [69], for power planes with integrated HIS, efficient noise mitigation is achieved at distances of at least two periods away from the noise source. This implies that the smaller the period, the smaller the distance required between individual ICs on a PCB for high level noise immunity. At the same time this will lead to a high packaging density. In this section we investigate the possibility of using smaller periods to achieve SSN mitigation in the same

order as previously described for larger periods. For all structures the via height and the substrate height between the HIS and the Vdd plane are fixed to 1.54 mm. The period of the HIS is 5 mm. The via diameter is 0.4 mm. The structures are first evaluated with a gap  $g$  (separation between adjacent patches) of 0.6 mm. The main electrical performance attributes of interest are the bandgaps or stopbands, which are all derived from the  $\Gamma$ -X section of the dispersion diagram.

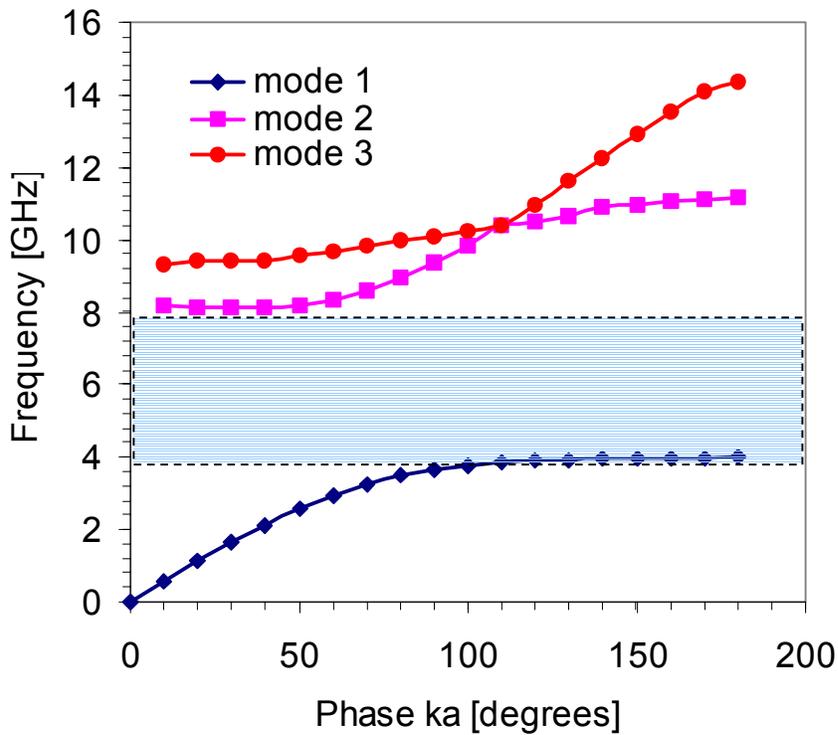


Figure 3-19: Dispersion diagram of reference power plane with standard HIS,  $a=5$  mm,  $g=0.6$  mm,  $w=4.4$  mm,  $t=d=1.54$  mm.

A reference power plane cell with the standard HIS is first analyzed and the resulting dispersion diagram shown in Figure 3-19. It has a single band-gap between 4 GHz

and 8 GHz. This band-gap resides between the first and second modes, which are  $TM_n$  and  $TE_n$  respectively. It can also be seen that when the phase constant is about  $110^\circ$ , the 2<sup>nd</sup> and 3<sup>rd</sup> mode swap.

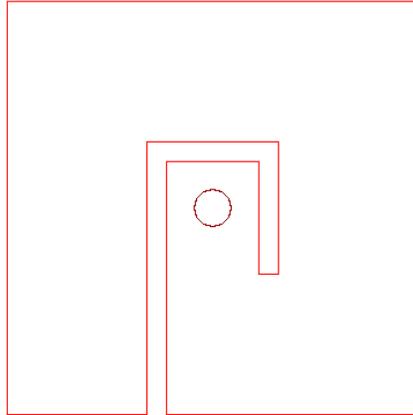
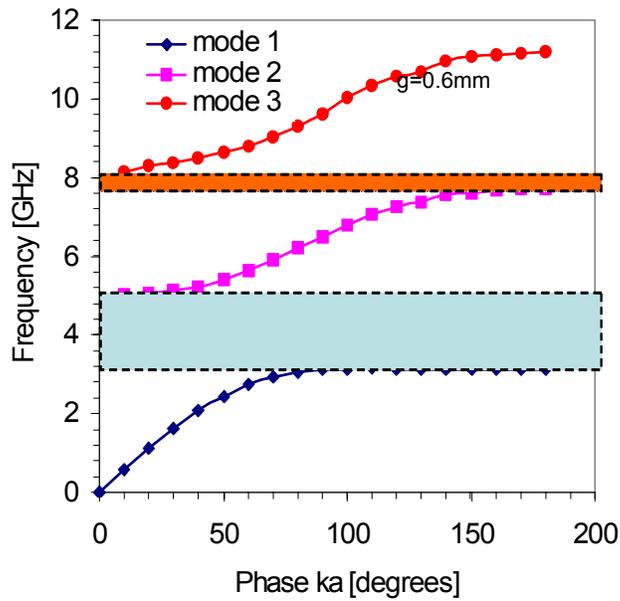
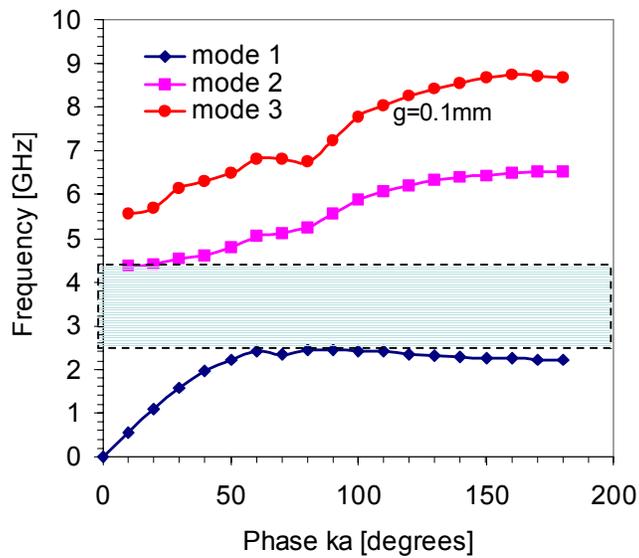


Figure 3-20: Top view of HIS unit cell with single-turn fat spiral as patch

Figure 3-20 shows the top view of the modified reference patch, where a 0.2 mm wide slot has been opened in the patch to change it into a single-turn “fat” inductor. The corresponding dispersion diagram is shown in Figure 3-21a. The fundamental band-gap is from 3.15 to 5.02 GHz and resides between the first and second modes. In this case a second band-gap, as expected for large values of  $g$ , is exhibited, between 7.72 and 8.2 GHz. In the dispersion diagram of Figure 3-21b, the gap size has been reduced to 0.1 mm. In general the changes in the fundamental or first band-gap are negligible. With the decrease of the gap there is a strong capacitive (and inductive) coupling between the patches. The negative slope seen in the first mode has been described in [70] for the open HIS as an indication of a backward traveling surface wave.



(a)



(b)

Figure 3-21 : Dispersion diagram of power plane unit cell with single turn fat spiral as patch for patch separation of (a) 0.6 mm and (b) 0.1 mm. Slot on outer loop is 0.2 mm wide.

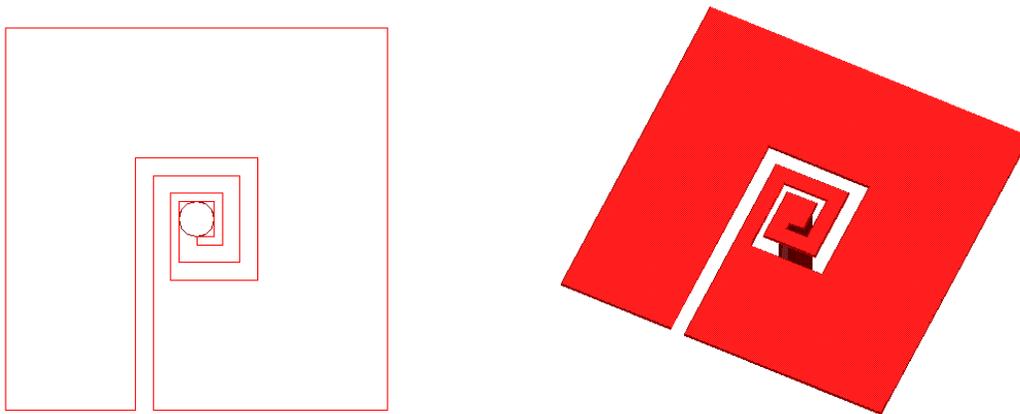
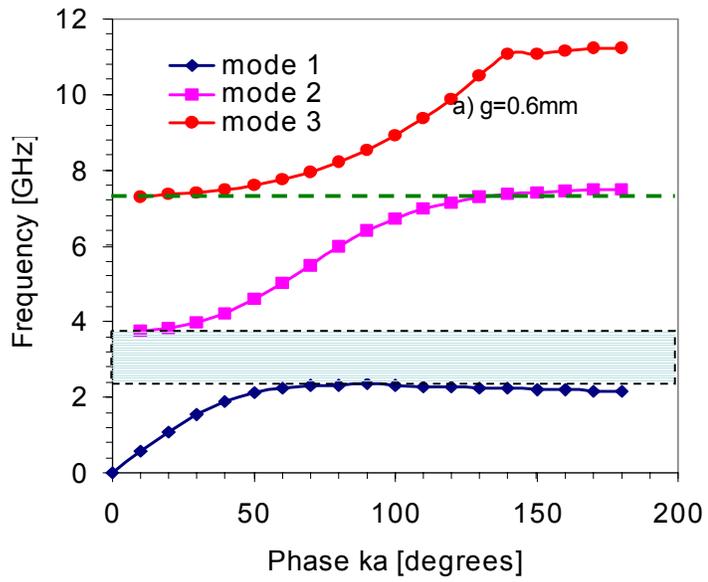


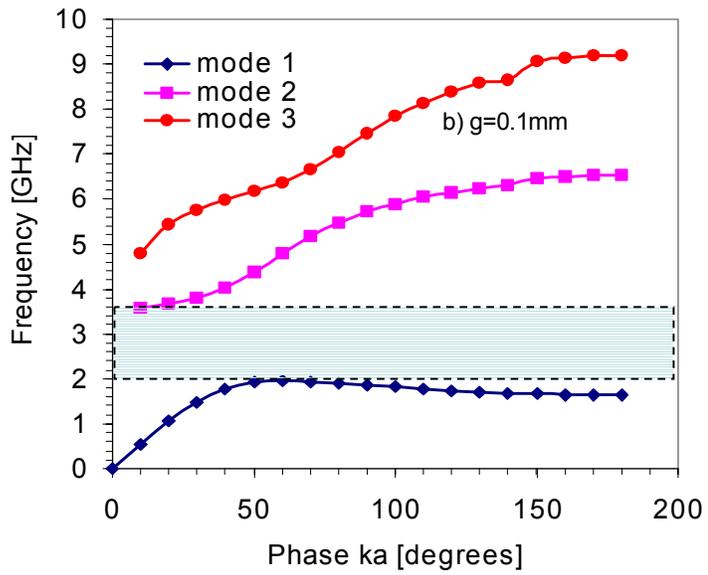
Figure 3-22: Top view and isometric view of HIS unit cell using a 2-turn spiral inductor with varying line width.

In Figure 3-22, the patch has been further modified to a two-turn spiral inductor with varying line width, whereby the inner turn has the smaller line width. When the gap is 0.6 mm the second band-gap is at its onset as shown in Figure 3-23a. A very sharp second band-gap can be obtained if the gap is slightly increased. The increase in inductance leads to the generation of backward propagating  $TM_n$  mode. As shown in Figure 3-23b, the backward propagating wave is even stronger with decreasing gap. The latter can be inferred to the stronger capacitive and inductive coupling between the patches.

In Figures 3-24a and 3-24b the number of turns of the inner inductor has been increased incrementally by  $\frac{1}{4}$  turns. Here it is important to note that the outer most turn of the spiral inductor no longer has a uniform line width. The corresponding dispersion diagrams are shown in Figures 3-25 and 3-26 respectively.



(a)



(b)

Figure 3-23: Dispersion diagram of a 2-turn spiral inductor with varying line width and a gap of (a) 0.6 mm and (b) 0.1 mm.

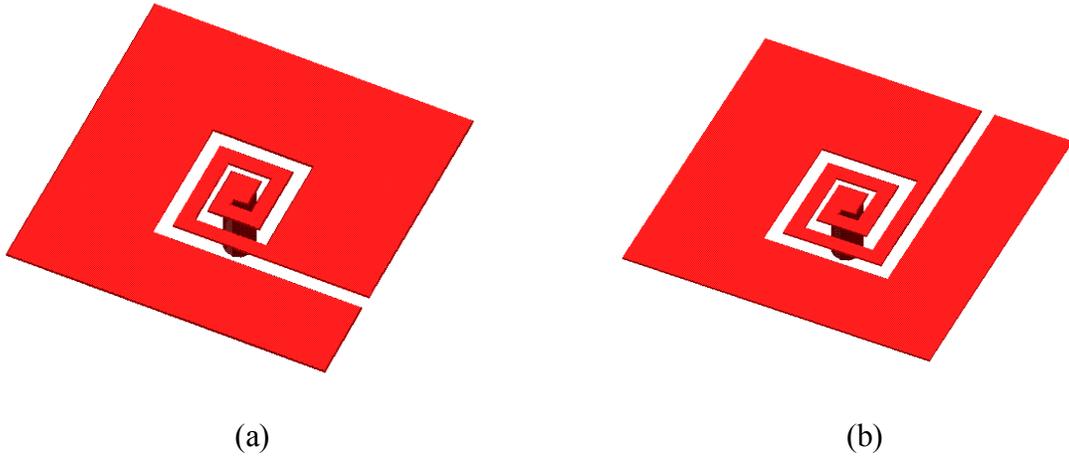


Figure 3-24: Isometric view of HIS cell using (a) a 2-1/4 turn inner inductor and (b) a 2-1/2 turn spiral inductor with varying line width.

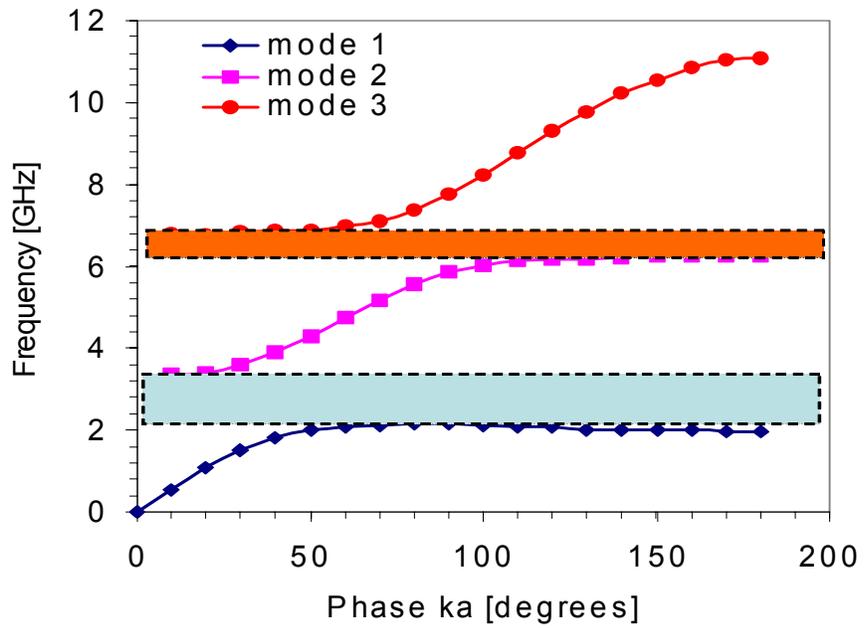


Figure 3-25: Dispersion diagram of structure with 2-1/4 turn spiral inductor as patch.

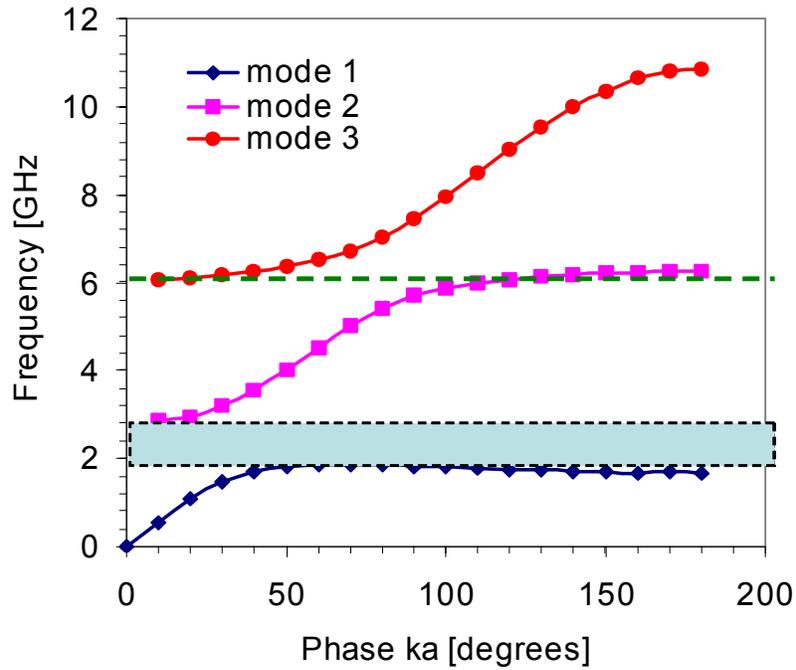


Figure 3-26: Dispersion diagram of structure with a 2-1/2 turn spiral inductor as patch.

Several inductively-tuned HIS structures have been analyzed in a power plane configuration, where a constraint was given on the maximum area for the unit cell. By increasing the number of turns of the spiral, a substantial shift of the stop-band towards lower frequencies could be achieved. It is further expected that additional increase of the number of turns would lead to even lower center frequencies. This would also be accompanied with a reduction of the width of the fundamental band-gap, which can partially be compensated by designing the HIS to exhibit a second band-gap. Table 3.5 shows a summary of performance of all power planes discussed in this section.

Cell description	g [mm]	Band-Gap [GHz]	Center Freq. [GHz]	Bandwidth [GHz]	Fractional bandwidth [%]
standard	0.6	4-8.1	6.05	4.1	67.8
Single turn	0.6	3.15 - 5.02	4.085	1.87	45.8
Single turn	0.1	2.45 - 4.36	3.405	1.91	56
Two turn	0.6	2.34 - 3.74	3.04	1.4	46
Two-turn	0.1	1.96 - 3.57	2.765	1.61	58.2
Two and 1/4	0.6	1.87 - 2.85	2.36	0.98	41.5
Two and 1/2	0.6	2.15 - 3.37	2.76	1.22	44.2

Table 3-5: Location and width of the fundamental stop-band of power planes using various HIS with open loop spiral inductor with variable line width,  $a=5$  mm.

### 3.5 Conclusion

Novel types of high-impedance electromagnetic surfaces have been proposed and studied in conjunction with their applications into parallel-plate power planes. The surface impedance of these structures is primarily controlled by their sheet inductance. Using the example of the double-layer HIS, it was shown that a combination of HIS and proper dissipative edge termination (DET) can lead to power planes with broadband SSN immunity starting at DC frequencies. Single-layer structures introduced here also showed that HIS can be designed at very low frequency without increasing the height of the board or the lattice constant. When the inductance is significantly increased in the HIS with open loop spiral inductors, the fractional bandwidth of the fundamental band-gap becomes very small. But at the same time there is a second bandgap, which allows dual-band switching noise mitigation. It has also been shown that the two stopbands of the HIS with open-loop

spiral inductor can be tuned independently. In addition, the fact that the location of the bandgaps is merely dependent on the “lumped” loading of the periodic structure enables low-frequency designs with very small lattice constants, therefore leading to higher packaging integration, when these HIS are used for noise mitigation in the power distribution network of high-speed circuits.

## Chapter 4

# **Development and Application of Physics-Based Compact Models for High-Impedance Electromagnetic Surfaces Integrated in Power Plane Environments**

### **4.1 Introduction**

As the physical size of electronic components increases, their analysis using electromagnetic (EM) simulation becomes very lengthy and memory intensive. In some cases, one could take advantage of the symmetry or of the periodicity to reduce the size of the problem to be solved. The solution of the full problem is then obtained through post processing of the simulation data. It is for example possible to represent a full characterization of infinite periodic structures using dispersion diagrams obtained from the electromagnetic (EM) simulation of a single cell. Practical limitations of the dispersion diagram include their inability to predict how abrupt the transition from stop- to pass-band regions may be or what is the level of signal attenuation at different regions of the transmission curves. This complementary information can generally be obtained from the scattering or S-parameters, which in most cases are generated from large structures with finite dimensions. Transmission characteristics of one-dimensional periodic structures using S-parameters obtained indirectly from the analysis of a single cell have been reported in [24] and [52], where the interaction between individual cells is neglected. This

assumption allows the calculation of the transmission matrix of a long chain of cells by chain-matrix multiplication of the ABCD-matrix of the individual cell. A more accurate approach described in [71], and which includes cell-to-cell interaction, utilizes full wave simulation to determine the overall transmission matrix of a limited number of cells. A recursive formula is then used to derive the transmission matrix (ABCD) of the longer chain. The two-port S-parameter matrix for the entire chain can then be obtained by using the transformation (ABCD) to S-parameter transformation described in [24].

At frequencies where the physical length of transmission line based devices and interconnects is much smaller than the wavelength, passive components can be modeled using lumped-elements. This same approach can be applied to periodic structures as long as the period is much smaller (one fifth) than the wavelength. In general lumped-element equivalent circuits for one-dimensional two-port structures can be obtained from the two-port Z- or Y-matrices. This concept, which has been applied intensively in the modeling of traditional power plane pairs [72]-[75], describes the behavior of the system only with respect to the ports by determining the transfer impedance. A more rigorous modeling of power plane resonance has been demonstrated in [76]-[77], where the planes are divided into identical cells and each cell modeled individually using either a lumped-element or a transmission line approach. In either case the values of the model parameters can be calculated using quasi-static formulation of the electromagnetic fields.

In general, compact models are combinations of physical and behavioral aspects of a structure and can be obtained using numerical optimization to match measured or EM-simulation-based S-parameters to those of the equivalent circuit. A very important point in

developing such models is the identification of a proper model form that incorporates the physical effects of the components. Numerical optimization can then be used to determine the right parameter values by optimizing measurement or EM-simulation data against those of the equivalent circuit. While the lumped-element approach has been used to model coplanar electromagnetic bandgap structures (EBGs) [84] or to explain the general behavior of HIS [15], the most detailed approach for modeling HIS has been reported by [17] and uses a transmission line approach.

This chapter introduces physics-based lumped-element compact models for HIS in parallel-plate environment. The model form is first developed for a unit cell and several of them connected in a two-dimensional array to build the model of large structures. Section 4.2 presents the development of the model form. Section 4.3 discusses the validation of the model for power planes with integrated standard and double-layer HIS. The developed compact model is applied in section 4.4 to study the mitigation of simultaneous switching noise (SSN) across the power planes, and to determine the dissipative edge termination (DET) requirements for broadband SSN mitigation. The extension of the compact model to include frequency dependent resistive losses using only frequency-independent components is discussed in section 4.5. The latter makes the model of particular interest for integration in linear time domain simulators such as SPICE.

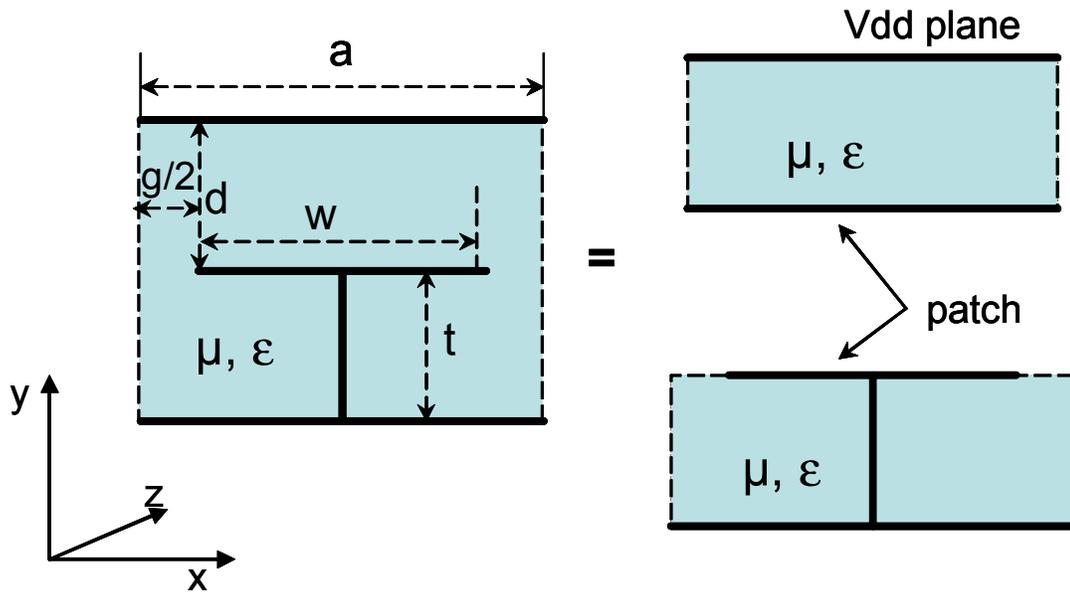


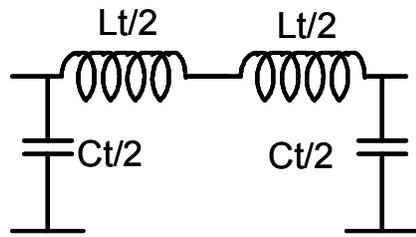
Figure 4-1: Cross-sectional view and decomposition of power plane unit cell into a parallel-plate transmission line and HIS cells.

## 4.2 Compact model development

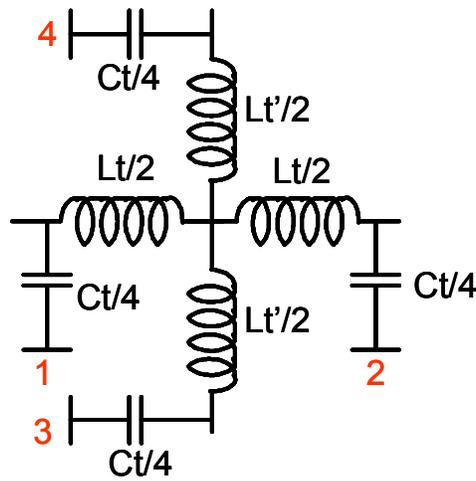
### 4.2.1 Model form definition for power planes using standard HIS

For the development of the model a power plane using a standard HIS with square patches is considered. Figure 4-1 shows the cross sectional view of the power plane unit cell and its decomposition into two effective cells for the HIS and the section between the HIS and the Vdd plane. The latter can be approximated by a parallel-plate transmission line, whereby it is important to note that the reference for this transmission line is the patch of the HIS. For one-dimensional wave propagation the parallel-plate transmission line cell can be modeled with the equivalent circuit of Figure 4-2a, where  $L_t$  is the total inductance of the Vdd plane and  $C_t$  is the total capacitance between the patch and the Vdd plane.

Similarly the HIS cell can be modeled for one-dimensional wave propagation using the equivalent circuit of Figure 4-3a, where  $L_p$  is the total inductance of the patch,  $L_v$  is the via inductance,  $C_p$  is the total capacitance between the patch and the bottom plate of the HIS and  $C_f$  is the fringing capacitance to the adjacent unit cell. The total capacitance between the Vdd plane and the bottom of the HIS as well as the mutual inductance between adjacent cells, which are not shown directly, are redistributed in the other components of the model.



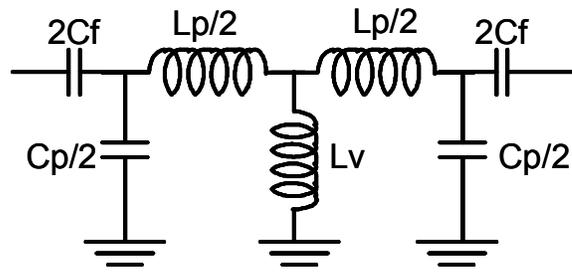
(a)



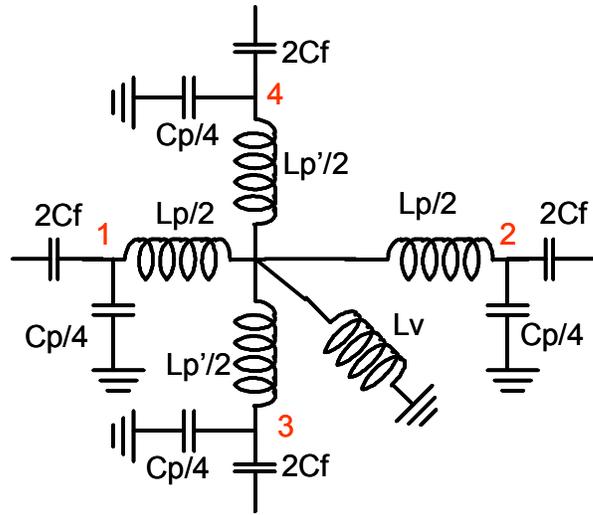
(b)

Figure 4-2: Equivalent circuit of HIS unit cell for (a) one-dimensional and (b) two-dimensional wave propagation with nodes 1-4 indicated.

For two-dimensional wave propagation the same model forms of Figures 4-2a and 4-3a are used for the other main direction of propagation since the cells are square and symmetric. This results in a 4-port compact model for both the transmission line and the HIS cells as illustrated in Figures 4-2b and 4-3b respectively. The stacking (cascading) of the two individual unit cell models results in the model of the power plane unit cell shown in Figure 4-4.



(a)



(b)

Figure 4-3: Equivalent circuit of parallel-plate transmission line for (a) one-dimensional and (b) two-dimensional wave propagation with nodes 1-4 indicated.

The compact model of a full power plane can then be obtained by connecting several of these unit cell models into a two-dimensional array. Figure 4-5 is an illustration of the 2D-model of a large power plane using the cascading of many cells. Each rectangle (box) is a multiport (10-port in this case) equivalent circuit of the unit cell. This compact model form is very generic and can be used for power planes with inductance or capacitance-enhanced HIS as well since the most significant difference resides only on the via inductance.

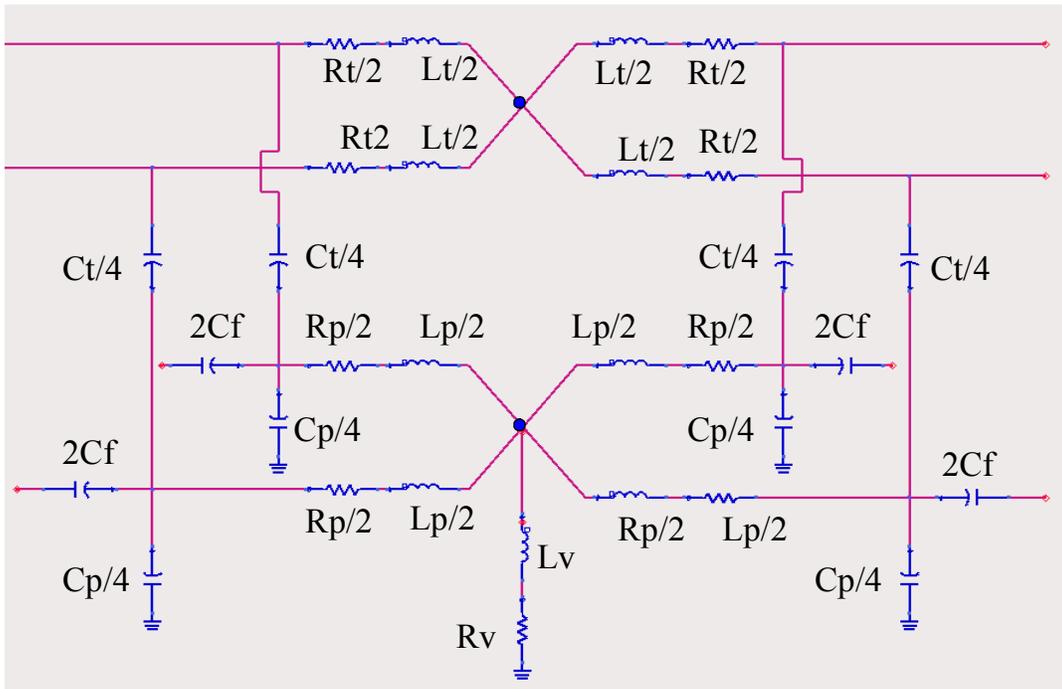


Figure 4-4: Full compact model of the power plane unit cell

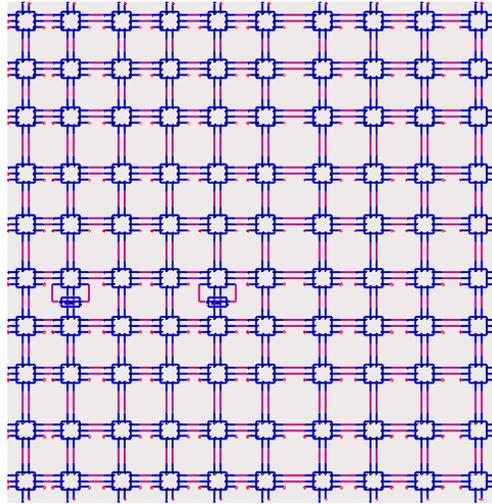


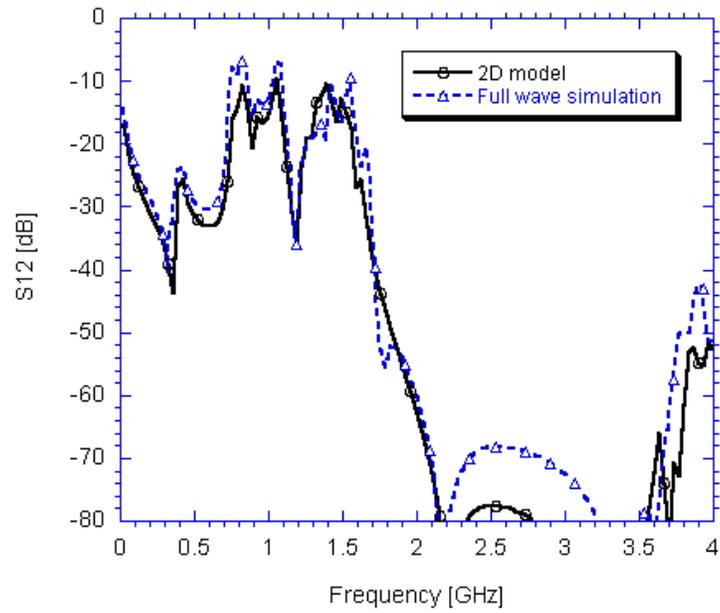
Figure 4-5: Illustration of power plane compact model based on cascading of several unit cell models.

#### 4.2.2 Expansion of the model form to power plane using HIS with polygonal shapes

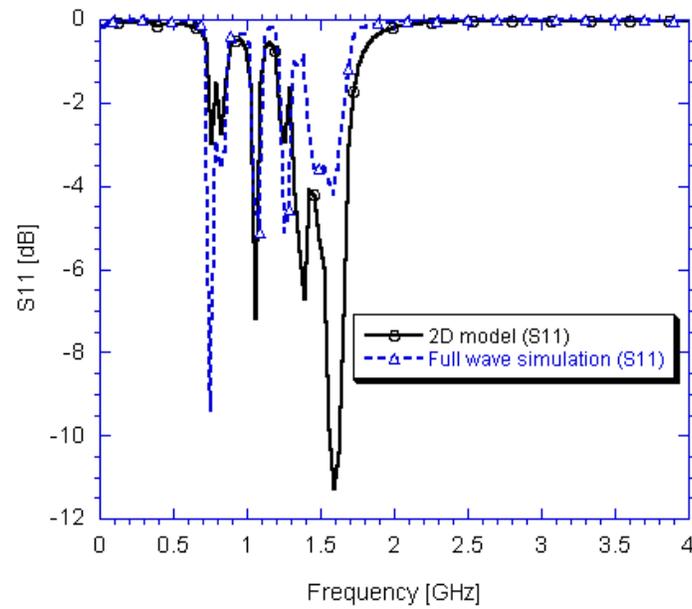
In general, when the polygonal patch has  $n$  sides, the shape of the Vdd plane section of the unit cell is the same and the only difference in width is the gap. In the compact model the number of  $L$  originating from the center of the patch is also equal to  $n$ . The coupling capacitors to ground and to adjacent patches are available on each side of the unit cell as discussed earlier for the case of square patches.

### 4.3 Compact model extraction

The extraction of the compact involves the following steps: First S-parameters are generated for a system of two-unit cells using electromagnetic full wave simulation. Second initial values are assigned to the model form using existing formulas for thin film inductors and parallel-plate waveguides described in [63], [78]-[79], and a circuit analysis tool



(a) Insertion loss



(b) Return loss

Figure 4-6: Modeled vs. simulated S-parameters of plane 1 (a) S12, (b) S11.

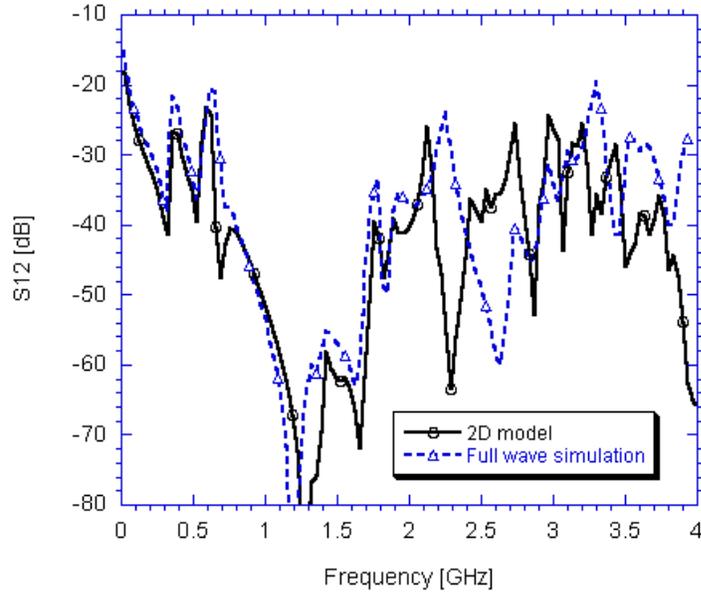
such as Agilent ADS [83] is used to extract the values of the model components by fitting the simulated S-parameters against that of the model. The final model of a full-size power plane is then obtained by connecting several of the unit cell models into a two-dimensional array. The validation of the full-plane model can then be obtained by direct comparison of the simulated and modeled S-parameters.

For the validation of the model, two power planes denoted as plane 1 and plane 2 are considered. Plane 1 is a 9 cm x 10 cm power plane with a standard HIS. The HIS has a height  $t=1.54$  mm and square patches. The periodicity is  $a = 10$  mm. The separation between the patches is  $g=400\mu\text{m}$  and the distance between the HIS and the  $V_{\text{dd}}$  plane is  $d=1$  mm. Plane 2 is a 10 cm x 10 cm power plane that utilizes a double layer HIS. The intermediate metal layer of the power HIS has a single loop of length 16 mm. The total thickness of the power plane 2 (including HIS) is 1.54 mm and the spacing between the patches is  $400\mu\text{m}$ .

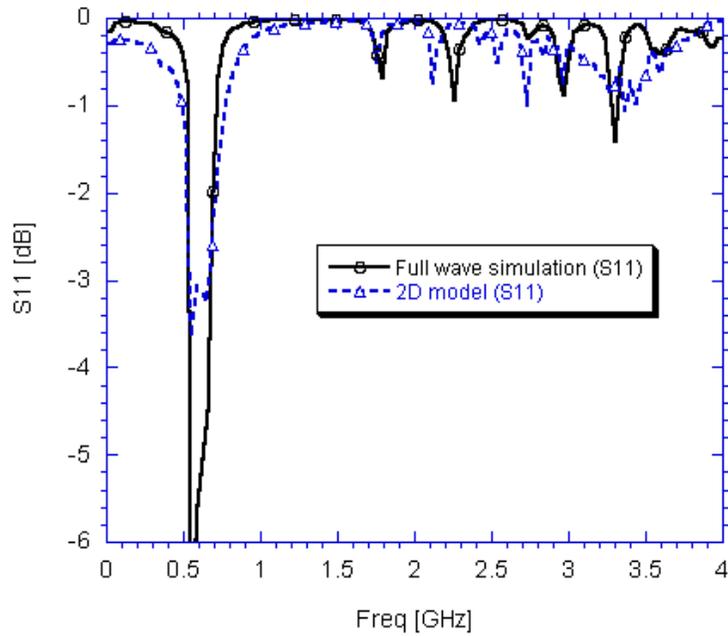
Figure 4-6 shows the simulated vs. modeled S-parameters of power plane 1. The noise source (port 1) is located at (4.5 cm, 4.5 cm) and the load (port 2) is located at (4.5 cm, 1.5 cm). Good agreement is obtained over the frequency range of interest for both the return loss S11 and The insertion loss S12.

Figure 4-7 shows the modeled vs. simulated insertion loss (S12) of power plane 2. Port 1 and port 2 are located at (4.5 cm, 4.5 cm) and (4.5 cm, 1.5 cm) respectively. Good agreement is obtained from DC up to the upper edge of the stopband as well. Above this upper corner frequency, the two curves have the same shape, with a frequency (phase) shift

of about 0.4 GHz between simulation and modeling. This discrepancy can be adjusted by additional tuning of the model component values.



(a) Insertion loss



(b) Return loss

Figure 4-7: Simulated vs. modeled S-parameters of the power plane 2.

## 4.4 Compact model application

### 4.4.1 Noise mitigation at different locations on the power plane

The compact model defined above can now be used in a circuit simulator for the analysis of the noise mitigation capability of the power plane system. Since the model is physics-based and periodic, its validation is not restricted to the position of the load and noise sources as defined in the reference full wave simulation used to extract the model component values. For a 10 cm x 10 cm power plane, the total simulation time using the compact model is less than ten seconds compared to more than 40 hours for the EM simulation on the same workstation.

To study the position dependency of the noise mitigation plane 1 is considered. First, the noise source (port 1) was fixed at point A (4.5 cm, 4.5 cm) and the load was moved through the points E-D-G-C of coordinates (4.5 cm, 3.5 cm), (4.5 cm, 2.5 cm), (4.5 cm, 1.5 cm) and (4.5 cm, 0.5 cm) respectively as illustrated in Figure 4-8. The resulting insertion loss (S12) is plotted in Figure 4-9. When the receiving port is closest to the noise source, the minimum insertion loss in the stop band increases, indicating the presence of strong capacitive coupling. As the distance increases, the bandgap converges to a fixed width with a simultaneous increase in the signal transmission at low frequencies. When the distance from the noise source to the load is about twice the lattice constant, the bandgap tends to saturate as the stopband insertion loss is well below -40 dB.

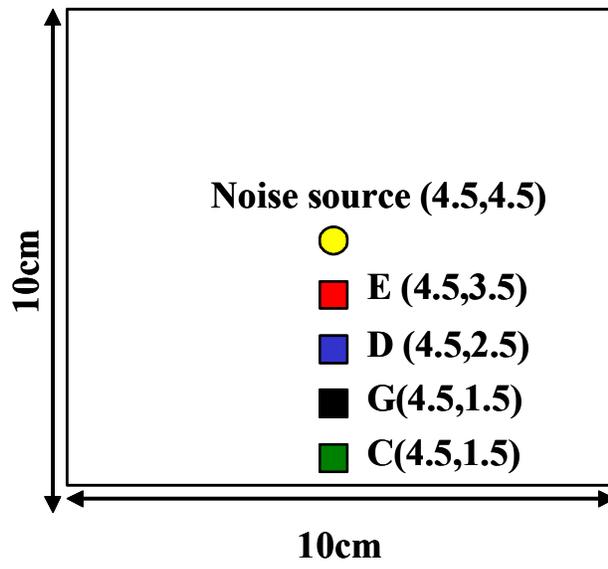


Figure 4-8: Top view of test power planes illustrating the position of noise source as what as that of the receiving load.

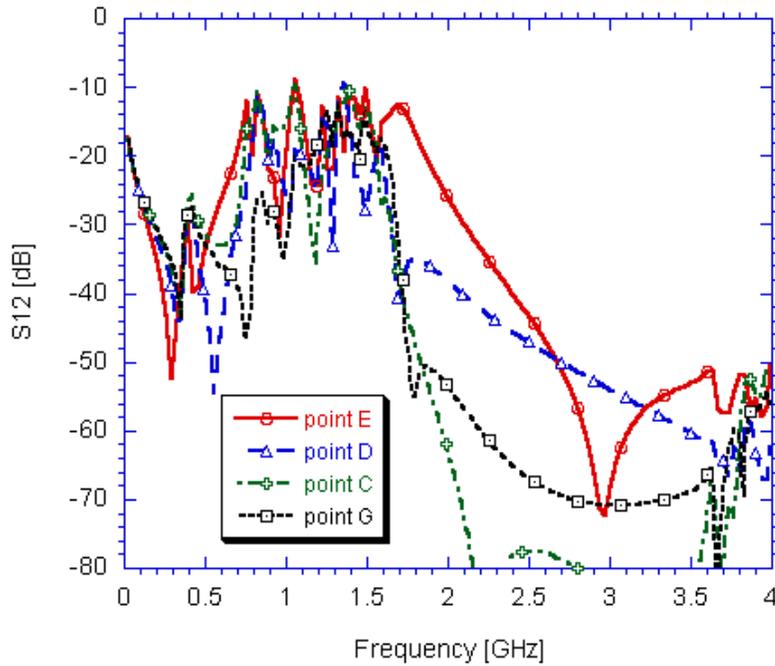
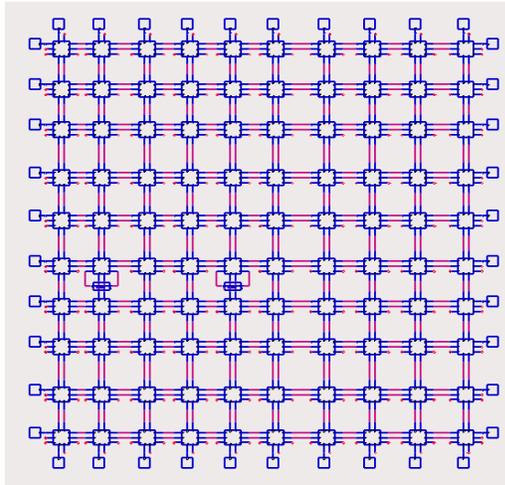
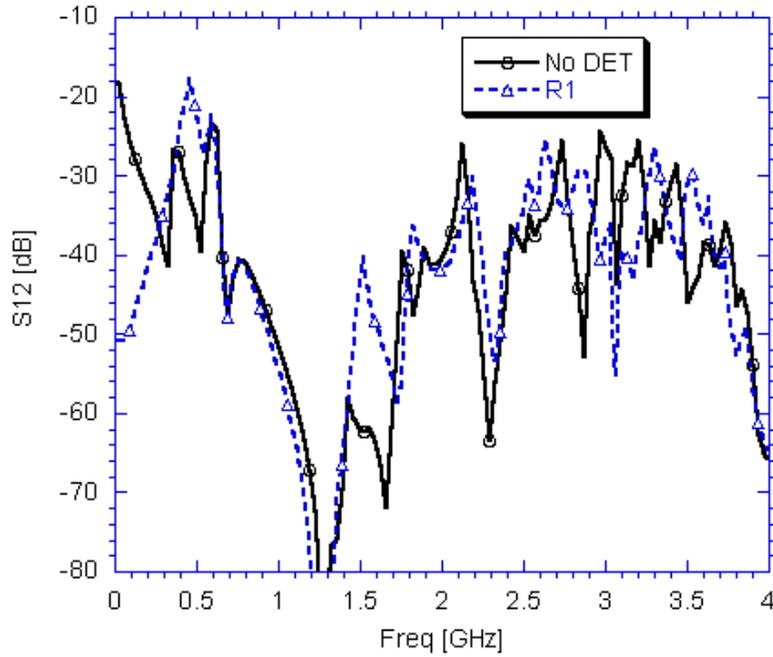


Figure 4-9: Insertion loss of plane 1 for different noise source to load distances



(a)



(b)

Figure 4-10: (a) Two-dimensional array of unit cell compact models with dissipative edge termination and (b) Insertion loss of the power plane 2 with and without wall of RC dissipative edge termination.

#### 4.4.2 *Combination of HIS with decoupling capacitors*

Resonance in parallel-plate power planes (waveguides) with finite width is usually due to the in-phase addition of incident and reflected waves, which results in standing waves. To mitigate those resonances, RC dissipative edge termination (DET) can be placed between the Vdd and the ground plane at the edges of the board as reported in [67]-[68]. This technique is applicable to both traditional power planes and power planes with integrated HIS. Figure 4-10a is an illustration of the concept with the compact model of power plane 2. Figure 4-10b shows the insertion loss of power plane 2 with and without decoupling capacitors. A substantial attenuation of the transmission coefficient is achieved at very low frequencies (close to DC) with DET using a series resistance R of 1 Ohm. Here each decoupling capacitor is modeled as a series RLC, with C being the desired decoupling capacitance, L the associated lead inductance and R a resistance (generally) selected to match the impedance of the parallel plate waveguide without HIS [68].

Unlike for regular parallel-plate waveguides, there are no established formulas for the impedance of parallel-plate waveguide with integrated HIS. In order to determine the optimum value of R for broadband SSN mitigation, 40 decoupling capacitors (RLC) connecting the Vdd and the ground planes were placed around the perimeter of power plane 2. With L and C fixed at 0.5 nH and 1 nF respectively, the resistance R was varied from 5 to 40  $\Omega$ . As illustrated in the insertion loss plot of Figure 4-11, the resonant mode attenuation improves at high frequencies as R increases, but at the same time there is a small degradation of the resonant mode mitigation at low frequencies. For too large value

of  $R$  there is no mitigation due to the DET since  $R$  is larger than  $1/\omega C$  at all frequencies. For the case considered here a resistance value of  $20\ \Omega$  provides reasonable noise mitigation at DC and also minimizes the high-resonant mode transmission seen around 600 MHz.

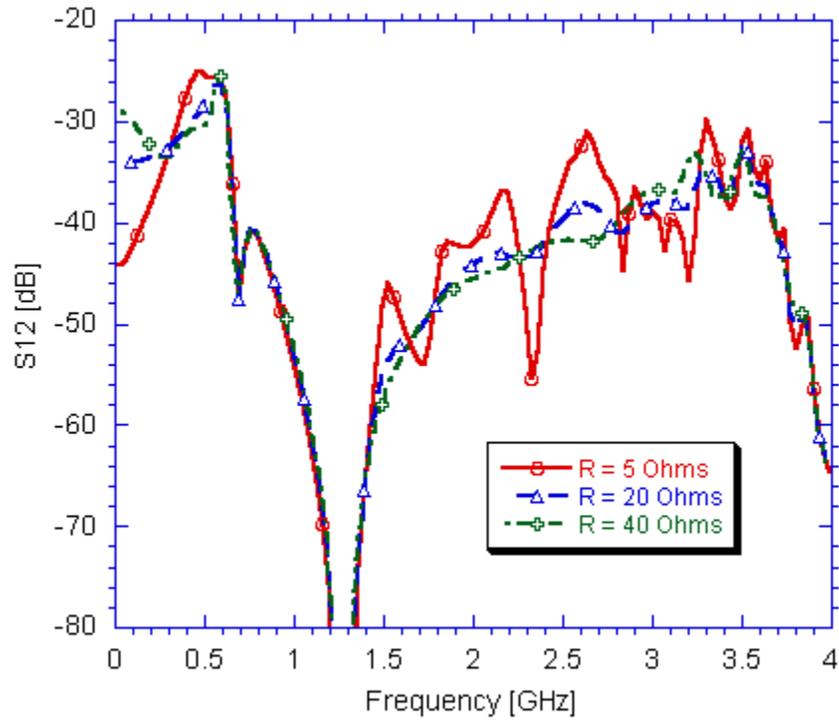


Figure 4-11: Effect of shunt resistance on high-frequency noise mitigation.

#### 4.5 Resistive losses consideration in power plane models

As the clock frequency increases beyond 1 GHz, frequency-dependent losses become very important in the accurate modeling of power planes. These losses can be grouped into two main categories: (1) The dielectric losses which can be modeled by adding a conductance  $G$  in parallel to the capacitors and (2) the conductor losses, which can be

modeled by adding a frequency-dependent resistance  $R(f)$  to the inductors as illustrated in Figure 4-12.

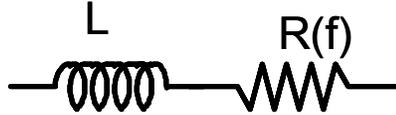


Figure 4-12: Typical inclusion of resistive losses in the conductor model.

At high frequencies, metallic losses are predominantly due to skin effect. The current flow is restricted to a very thin layer underneath the conductor surface. The thickness of this layer also known as skin depth is given by equation (4.1) [22].

$$\gamma = \sqrt{\frac{1}{\pi f \sigma \mu}} \quad (4.1),$$

where  $f$ ,  $\sigma$ , and  $\mu$  represent the frequency, the conductivity and the permeability, respectively. For copper for example  $\sigma = 5.8 \times 10^7$  S/m leading to a skin depth in meters of  $0.066 / \sqrt{f}$ .

In the power planes, except for the vias, the conductors have rectangular cross sections. For a conductor of length,  $l$ , and cross section,  $a \times b$ , as shown in Figure 4-13a, the skin effect only occurs when both  $a$  and  $b$  are each larger than twice the skin depth at the frequency of interest. If it is assumed that the skin depth is uniformly distributed then the effective cross section is defined as

$$A_e = ab - (a - 2\gamma)(b - 2\gamma) = 2\gamma(a + b) - 4\gamma^2 \quad (4.2).$$

The resistance of the conductor is then given as

$$R = \frac{l}{\sigma A_e} = \frac{\rho l}{2\gamma(a+b) - 4\gamma^2} \quad (4.3).$$

By substituting (4.1) into (4.3) one obtains

$$R = \frac{\mu f l}{2(a+b)\sqrt{\mu \sigma f} - 4} \quad (4.4).$$

For a via of length,  $l$ , and of circular cross section with radius  $r$ , if it is assumed that the diameter is larger than twice the uniformly distributed skin depth at a given frequency, then the effective cross section of the conductor that carries the current at that frequency is given as

$$A_e = \pi r^2 - \pi(r - \gamma)^2 = 2\pi r\gamma - \pi\gamma^2 \quad (4.5).$$

The resistance of the via can then be found as

$$R_v = \frac{l}{\sigma A_e} = \frac{\mu f l}{2\pi r\sqrt{\mu \sigma f} - \pi} \quad (4.6).$$

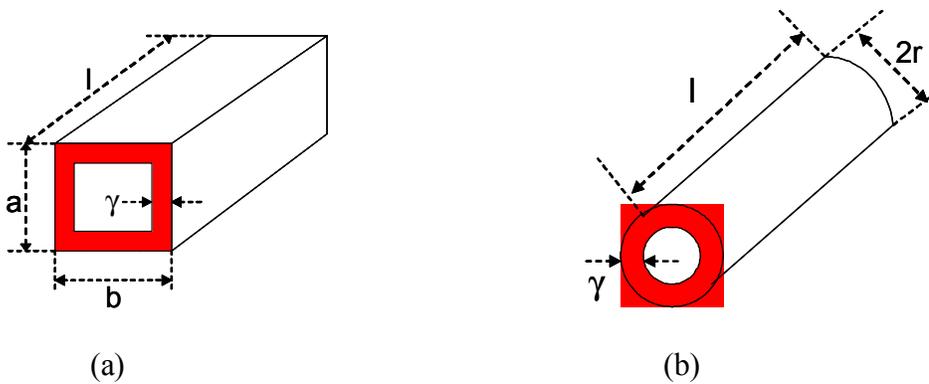


Figure 4-13: Illustration of skin effect in conductor with (a) rectangular and (b) circular cross sections.

In equations (4.4) and (4.6) the first term in the denominator is usually much larger than the second term such that the skin effect resistance can be approximated as being proportional to the square root of the frequency. As the spacing between the patches decreases, the proximity effect starts to contribute to the resistive losses as well. This effect is usually characterized by current crowding at the edge of the conductors and therefore further reduces the fraction of the conductor cross section that carries the current.

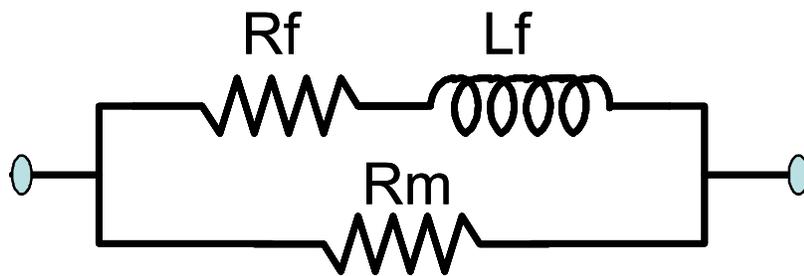


Figure 4-14: Compact model of the resistive losses using frequency independent lumped-elements.

While all these losses are all frequency-dependent their synthesis using a lumped-element model with only frequency-independent components is necessary for the implementation of the model in time-domain simulators such as PSPICE. The model of Figure 4-14 can be used in place of the frequency dependent  $R(f)$  of Figure 4-12. The parameters  $R_m$ ,  $R_f$  and  $L_f$  are all frequency independent elements. This network was used previously by [81] to model the skin effect of straight conductors in free space and in a dielectric medium. Its detailed analysis, however, was not performed. Instead, numerical

fitting techniques were used to show that adding more series RL elements in parallel to the network provide better accuracy. Successful implementation of this model form to model frequency dependent resistive losses in inductors on conductive substrates has been demonstrated in [82]. The overall impedance of the network of Figure 4-14 is given by

$$Z(j\omega) = R(\omega) + jX(\omega) \quad (4.7),$$

where

$$R(\omega) = R_m \cdot \frac{R_m R_f + R_f^2 + \omega^2 L_f^2}{(R_m + R_f)^2 + \omega^2 L_f^2} \quad (4.8)$$

and

$$X(\omega) = R_m^2 \cdot \frac{\omega L_f}{(R_m + R_f)^2 + \omega^2 L_f^2} \quad (4.9)$$

Although  $R(\omega)$  (4.8) is not proportional to the square-root of the frequency, it begins as  $R_m/R_f$  at DC, then increases with the frequency and saturates against  $R_m$  at high frequencies. It also has an inflection point, which occurs at the frequency  $f_0$ , with

$$\omega_0 = 2\pi \cdot f_0 = \frac{(R_m + R_f)}{\sqrt{3} \cdot L_f} \quad (4.10).$$

For given values of  $R_f$  and  $R_m$ , the value of  $\omega_0$ , which gives the best approximation of the skin effect is empirically determined. The imaginary part of the impedance begins very low at DC and peaks at

$$\omega_{peak} = \frac{R_m + R_f}{L_f} = \sqrt{3} \cdot \omega_0 \quad (4.11)$$

before dropping again. The value  $X_{peak}$  at  $\omega_{peak}$  is given by

$$X_{peak} = X(\omega_{peak}) = \frac{1}{2} \cdot \frac{R_m^2}{R_m + R_f} \quad (4.12)$$

From equation (4.9) the resulting frequency dependent inductance

$$L(\omega) = \frac{X(\omega)}{\omega} = \frac{R_m^2 \cdot L_f}{(R_m + R_f)^2 + \omega^2 L_f^2} \quad (4.13)$$

decreases quadratically with the frequency and thus has only minor contribution to the overall high-frequency impedance. Indeed, the decrease in inductance with frequency of this network is even stronger than the skin-effect decrease of straight wire inductance as predicted by [79] and [83].

#### 4.6 Summary

Lumped-element based compact models have been developed for high-impedance electromagnetic surfaces integrated in power plane environments. The model is based on the development of a model for a single cell. Several of these unit cell models are connected into a two-dimensional array to realize the model of large structures. This model form, which has been validated for power plane with standard and double-layer HIS requires only a few second for the analysis, and can also be combined with other component models to allow for a fast system level analysis of high-speed circuits. In addition, it can be used as tool to study the noise mitigation across the power plane and to determine necessary dissipative edge termination (DET) for broadband noise mitigation. The incorporation of frequency dependent losses using lumped-elements makes the compact model suitable for full package time domain linear simulator such as PSPICE.



## Chapter 5

### Conclusions and Future Work

#### 5.1 Conclusions

Simultaneous switching noise (SSN) mitigation through the suppression of natural resonances in parallel-plate power planes of high-speed circuits has been addressed in this thesis and the following results obtained.

A novel concept for mitigating simultaneous switching noise (SSN) in high-speed circuits has been developed. The SSN mitigation is primarily achieved by suppressing the dominant parallel-plate mode encountered in traditional parallel-plate power planes. This is achieved by replacing one or both planes of a traditional power plane pair with a high-impedance electromagnetic surface (HIS), which has the ability to prevent AC current flow in a given frequency band known as its band-gap. Using EM simulation the concept was verified and some fabrication was carried out to complete the validation of the concept.

Standard HIS has fundamental limitations for designs below 1 GHz. In order to achieve noise mitigation at low frequencies, large patch sizes are required. This inherently leads to large power planes and low package integration density. This issue has been addressed by developing a new family of HIS, whose surface impedances are mainly controlled by the inductance density. Contrary to the enhancement of the per unit area capacitance, an enhancement of the inductance density leads to simultaneous decrease of

the self-resonance frequency and an increase of the fractional bandwidth, therefore allowing broadband designs at low frequencies.

A method is introduced for designing double-layer inductance-enhanced high-impedance electromagnetic surfaces. In this novel design, the straight via of the standard HIS unit cell is replaced by an inductance-enhanced element, consisting of two vias and a single-loop or a multi-turn spiral inductor. This type of structures applied in a power plane configuration offers noise mitigation below 1 GHz for structures with lattice constant of 10 mm. This contribution was discussed in section 3.2.1.

It was demonstrated in section 3.2.2 that broadband noise mitigation can be achieved by combining RC dissipative edge termination (DET) with inductance-enhanced high-impedance electromagnetic surfaces. Using a combination of HIS and RC DET as example, noise mitigation from DC to 4 GHz is achieved on a 10 cm x 10 cm power plane.

Two novel single-layer inductance-enhanced HIS topologies were introduced and discussed in section 3.3.1 and 3.3.2. The fundamental idea behind these structures consists of increasing the inductance per unit cell by appropriate patterning of the patch of the standard HIS cell. It was demonstrated that both HIS using a cross embedded in the patch and HIS using a closed-loop spiral inductor as patch can mitigate noise at much lower frequency band-gap than standard HIS with similar periodicity and patch spacing, when used in power planes.

A novel type of single-layer high-impedance electromagnetic surfaces using an open-loop spiral inductor as patch was introduced in section 3.3.3. and thoroughly investigated in section 3.4. It was shown that this type of structures exhibits two very close

frequency band-gaps that can be adjusted (or tuned) independently. This type of structures offers the possibility for multi-band noise mitigation.

Physics-based lumped-element compact models for HIS in power plane configuration were developed in chapter 4. The model was based on the development of a compact model for single unit cell, several of whom were connected into a two-dimensional array to build the full model for the periodic power planes. The model was validated on power planes with integrated standard and inductance-enhanced HIS.

## **5.2 Future work**

Most simulations and all experimental results have been limited to structures that can be fabricated in standard PCB technology, where the thickness of the substrate is 1.54 mm. Since the thickness of typical PCB in today's computers is on the order of a few hundred microns per layer it is recommended that future work address thinner structures.

The compact model of the power plane integrated HIS, which has been primarily extracted using numerical optimization, could also be expressed analytically in form of formulas that relate the model parameters to the physical and material properties.

The introduction of high-impedance with two independently tunable band-gaps opens plenty of opportunities for future research work that go beyond noise mitigation in high-speed circuits. This could especially be very attractive for filters, antennas, where photonic bandgap structures have already been applied.

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## BIOGRAPHY

Telesphor Kamgaing was born in 1971 in Baham, Cameroon, where he pursued his education throughout graduation from high-school. In 1997 he received a Dipl.-Ing. (M.S.) degree in Electrical Engineering from Darmstadt University of Technology, Darmstadt, Germany. He is currently pursuing a Ph.D. degree in Electrical Engineering at the University of Maryland at College Park, Maryland, USA. In fall 1999, he was a guest researcher with the National Institute for Standard and Technology (NIST) in Gaithersburg, MD, where he was involved in the modeling and applications of silicon carbide PiN diodes. Since January 2000 he has been with the Digital DNA Laboratories of Motorola Semiconductor Product Sector, where he is involved in the design and modeling of advanced radio frequency (RF) modules and silicon integrated passive components. Mr. Kamgaing was the recipient of a government scholarship in 1990, of the best Baham student award in 1990, of the 1996 Foreign Student award sponsored by the German Academic Exchange Service and of a conference travel grant from the NSF in 2003. He was also a finalist for the best student paper award at the 2003 IEEE International Symposium on Antennas and Propagation. He has authored or co-authored about 15 technical papers in refereed international journals and conference proceedings. Following is a list of Mr. Kamgaing's publications:

1. O.M. Ramahi, S. S. Shahparnia, B. Mohajer-Iravani, and **T. Kamgaing**, "Noise Mitigation in High-Speed Systems using Electromagnetic High-Impedance surfaces," to be presented at the 2003 International Semiconductor Device Research Meeting, Washington, DC.

2. **T. Kamgaing** and O.M. Ramahi, "Design and modeling of high impedance surfaces for mitigation of simultaneous switching noise in PCB power planes," in proceedings of Mediterranean Microwave Symposium, Cairo, Egypt, pp. 97-100, May 6-8, 2003.
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