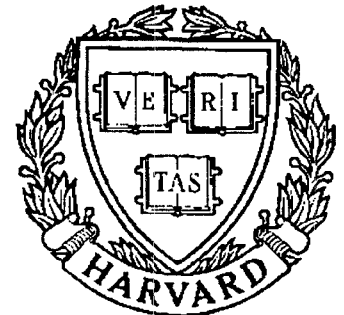


TECHNICAL RESEARCH REPORT



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*Supported by the
National Science Foundation
Engineering Research Center
Program (NSFD CD 8803012),
the University of Maryland,
Harvard University,
and Industry*

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*by J-F. Lin, W-H. Ki,
K.E. Thompson and S. Shamma*

COCHLEAR FILTERS DESIGN USING A PARALLEL DILATING-BIQUADS SWITCHED-CAPACITOR FILTER BANK

Jyhfang Lin¹, Wing-Hung Ki², K. Thompson¹ and Shihab Shamma¹

¹SRC and EE Dept.
University of Maryland
College Park, MD 20742

²ICSL, EE Dept.
University of California
Los Angeles, CA 90024

ABSTRACT

A parallel filter bank is proposed to implement cochlear filters using very large time-constant (VLT) switched-capacitor (SC) biquads. Significant hardware reduction is achieved in three ways. Firstly, the number of biquads is reduced by biquad-sharing such that each channel consists of three biquads in parallel, and a n -channel filter bank requires only $n+2$ biquads and n sum-gain amplifiers for implementation. Secondly, area-efficient SC biquads are used, and the capacitor spread of each biquad is approximately $1/\sqrt{\Omega_0 T}$, where Ω_0 is the pole frequency and T is the sampling period. Finally, lowpass notch (LPN) biquad is used to avoid a zero at $z=-1$ which results in a very small capacitor in each biquad.

1. INTRODUCTION

Cochlear filters are used extensively in speech research. Software implementations are computationally intensive and difficult to process information in real time, while hardware implementations promise to achieve real-time performance. Previous attempts included building biquads using subthreshold and operational transconductance amplifier[1, 2]. Another approach is to use switched-capacitor multi-channel filter bank[3], which is more reliable and no post-fabrication tuning is needed.

Several difficulties arise when implementing the cochlear filters for sound processing using switched-capacitor biquads. One is the broad frequency range that stretches to relatively low frequencies. Another is the large number of channels needed. Finally, some zeroes of the cochlear transfer functions are at $z = -1$ in the z -domain and this always results in a large capacitor spread.

In this paper, we propose a parallel dilating-biquads VLT SC filter bank to solve the above problems. The SWITCAP simulation result of a 32-channel filter bank is given to demonstrate the validity of this design.

2. SYSTEM DESIGN: DILATING-BIQUADS FILTER BANK

The cochlea can be thought of as a filter bank consisting of a series of bandpass filters, with bandwidths and center

frequencies that change systematically along its length. The transfer functions of the channels are related by a dilation.

The system topology of a 32 dilating-biquads filter bank is shown in Fig. 1. In the present design, each channel is a 6th order bandpass filter, which can be implemented by connecting 3 lowpass notch biquads in parallel. Gains of the biquads are chosen such that after summing the 3 outputs by a sum-gain amplifier, the bandpass function is obtained. Biquads are designed to be dilated w.r.t. one another. This parallel structure results in reduction of hardware by biquad-sharing. For example, Channel 1 consists of biquads 1, 2 and 3 (Fig. 1) which are dilated with respect to one and other, and their responses are scaled and summed by the sum-gain amplifier 1 (to be discussed in Sec. 3). Channel 2 can be realized with the addition of biquad 4 and the sum-gain amplifier 2 as shown in Fig. 1. Thus, for a 32-channel cochlear filters, the parallel structure requires $32+2=34$ biquads and 32 sum-gain amplifiers.

Based on the above discussion, the transfer function of the n -th biquad is chosen as

$$G_n(s) = H(k^{n-1}s)$$

where, $H(s)$ is a 2nd order LPN filter in the s -domain, k = dilation constant, and $n = 1, \dots, 34$. That is, biquads are related by a dilation. Using these biquads, the transfer function of the m -th channel of the cochlear filter is

$$Y_m(z) = \sum_{i=1}^{i=3} a_i G_{i+m-1}(z)$$

where, a_i 's are gain factors. Since the same set of a_i 's is used in every channel, only one sum-gain amplifier has to be designed. The rest will just be its duplicates. Note that more biquads can be used to approximate the cochlear responses and this usually depends on application.

More cochlear channels can also be realized by using more biquads and sum-gain amplifiers, but then the IC chips will be too complex. Another possibility is to take advantage of the SC circuits. It is well known that by changing the sampling frequency by a factor F , then all the zero and pole frequencies will be changed by the same factor. Hence, by connecting several similar chips together, each with a different sampling frequency, more cochlear channels can be obtained.

In realizing lowpass notch functions with very low pole frequencies, the Type II charge differencing LPN biquad[4] shown in Fig. 4 is used to avoid an extremely small capacitor (c_6).

3. CIRCUIT DESIGN I: SUM-GAIN AMPLIFIER

In this filter bank design, the outputs of 3 biquads are added together to simulate one channel of the cochlear filters. Therefore, a sum-gain amplifier which can sum input signals in the same phase is needed in this system. A new sum-gain amplifier is shown in Fig. 2 and its principle of operation is as follows:

Consider input v_{in1} first, while v_{in2} and v_{in3} are set to zero. In phase 2, c_{a2} is discharged, and since in phase 1, its left plate is connected to v_- of the op-amp only, no charge can be injected to c_{a2} , and the output remains at ground level, which helps c_{a1} to discharge in this phase. During phase 2, c_1 , c_{a1} , and the op-amp constitute a non-inverting gain stage, which gives $v_{out}(n+1/2) = (c_1/c_{a1})v_{in1}(n)$. The input v_{in3} can be analyzed in similar fashion.

Next, set v_{in1} and v_{in3} to zero. In phase 2, c_{a2} is discharged as in the previous case, but in phase 1, c_2 , c_{a2} , and the op-amp constitute an inverting amplifier, hence, $v_{out}(n) = -(c_2/c_{a2})v_{in2}(n)$. This voltage is stored in c_{a1} , and is to be held constant during the next phase 2.

The final output is the superposition when all the 3 inputs are activated. The signal flow graph of the sum-gain amplifier is shown in Fig. 3, and the transfer function can be obtained as,

$$v_{out}(z) = \left(\frac{c_1}{c_{a1}} v_{in1}(z) - \frac{c_2}{c_{a2}} v_{in2}(z) + \frac{c_3}{c_{a1}} v_{in3}(z) \right) z^{-1/2}$$

Hence, the output is the sum of v_{in1} and v_{in3} , while subtracts v_{in2} , all of which are scaled by appropriate gain factors. The gain factors can be individually controlled through c_1 , c_2 , and c_3 . Moreover, it is obvious that this sum-gain amplifier can be designed to include any number of inputs for either addition or subtraction.

One disadvantage of this sum-gain amplifier is the lack of a continuous feedback path across the op-amp. Hence, if the op-amp used in this circuit is very fast, a glitch at the output may occur at the non-overlapping interval between the two clock phases. This glitch is readily removed by connecting a capacitor c_M between the op-amp output and the left plate of c_2 [5].

4. CIRCUIT DESIGN II: AREA-EFFICIENT BIQUADS

The design of the lowpass notch biquads falls into two categories. For the 17 biquads with high center frequencies (Table 1), the Type II gain- and offset-compensated (GOC) Nagaraj VLT biquads are used[6]. The circuit diagram is shown in Fig. 3 of [6], and the design equations are given by eqns. 6 and 9 of [6]. For the other 17 biquads with low center

frequencies (Table 1), the capacitor spread using the above biquads will be too large. In order to reduce the capacitor spread, the Type II GOC charge differencing biquads are used[4, 6]. The corresponding circuit diagram is shown in Fig. 4. Define α , β and γ as in eqn. 3 of [6], and assign the capacitor values as follows :

$$\begin{aligned} c_{a2} &= c_{b2} = c_1 = c_2 = c_{o1} = c_{o2} = 1 \\ c_{a1} &= c_{b1} = 1 + \delta \\ c_A &= c_B = K \end{aligned}$$

to reduce the capacitance spread, then K is the solution of

$$(K+1)^4 + 2(K+1)^3\delta + (K+1)^2\delta^2 + \frac{(K+1)\beta\delta}{\alpha} - \frac{\delta^2(1-\beta)}{\alpha} = 0$$

For unity DC gain, $\Omega_0 T \ll 1$ and $\Omega_1 T \ll 1$, it can be shown,

$$\begin{aligned} K &\approx \sqrt{\delta/(\Omega_0 T)} - 1 \\ c_2 &= c_5 = 1 \\ c_4 &= (\beta\delta)/(\alpha(K+1+\delta)(K+1)) \approx 1/Q_0 \\ c_6 &= (\alpha/\gamma)(K+1+c_4) \approx (\Omega_0^2/\Omega_1^2)(K+1+c_4) \end{aligned}$$

Note that δ should not be too small due to the sensitivity problem[4]. In this filter bank, we choose $\delta = 0.5$ in designing the biquads with low center frequencies. The largest capacitor is K units and the smallest capacitor is 1 unit ($Q_0 < 1$ all the biquads).

5. SIMULATION RESULT OF THE FILTER BANK

To demonstrate the validity of this design, the capacitor values of biquads based on a 500kHz sampling frequency are given in Table 1 and the capacitors of the sum-gain amplifiers are chosen as $c_{a1} = c_{a2} = 1.0$, $c_1 = 9.574$, $c_2 = 20.939$, and $c_3 = 11.365$. The capacitor spread ratio of this filter bank is less than 25. The SWITCAP simulation output of this filter bank is shown in Fig. 5.

6. CONCLUSIONS

A parallel dilating-biquads switched-capacitor filter bank is described in simulating the cochlea. Area-saving is achieved by biquad-sharing and using area-efficient biquads. The structure is easily expandable to include more channels by extending to include more biquads and sum-gain amplifiers, or using several chips with different sampling frequencies in parallel connection.

ACKNOWLEDGEMENTS

The authors gratefully thank Prof. Gabor Temeš of Oregon State University for his helpful discussions. This work was supported by grants from the Air Force of Scientific Research and the Office of Naval Research.

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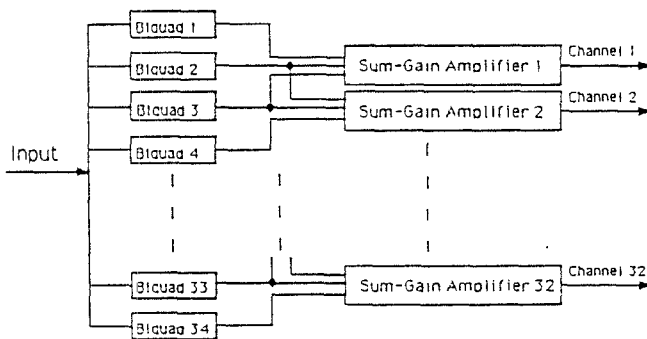


Figure 1: Dilating-biquads filter bank.

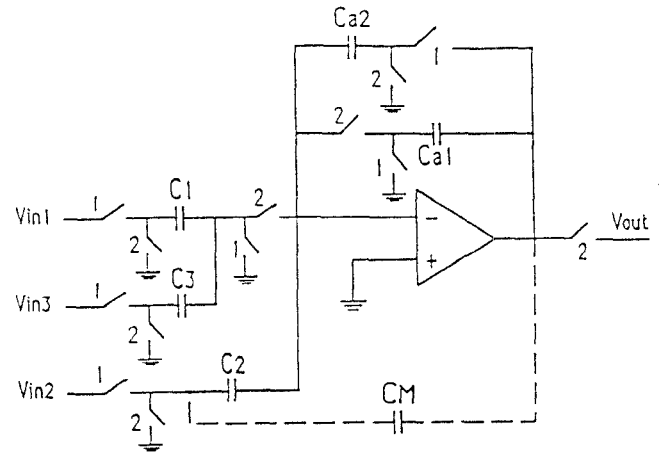


Figure 2: Sum-gain amplifier circuit.

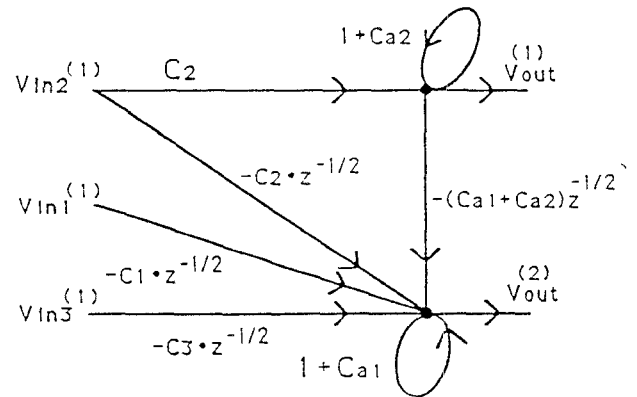


Figure 3: SFG of sum-gain amplifier circuit.

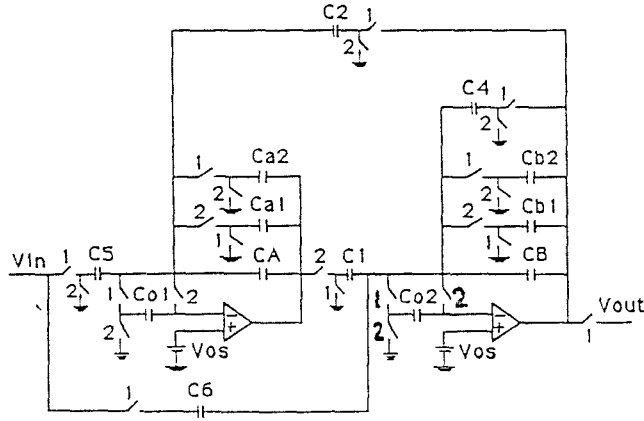


Figure 4: Type II GOC charge differencing biquad.

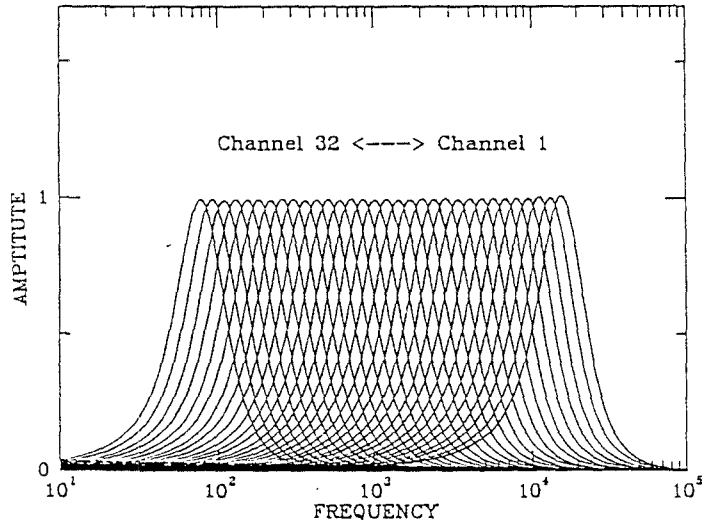


Figure 5: Simulation result of the filter bank.

$C_1 = C_2 = C_5 = C_{o1} = C_{o2} = 1$				
$C_{a1} = C_{b1} = 1$ and $C_{a2} = C_{b2} = 0$				
Biquad #	Center freq.	C_A and C_B	C_4	C_6
1	20000.00	1.313	1.310	1.038
2	16849.20	1.484	1.281	1.109
3	14194.78	1.673	1.254	1.190
4	11958.53	1.879	1.230	1.279
5	10074.58	2.106	1.208	1.378
6	8487.43	2.353	1.188	1.487
7	7150.32	2.623	1.171	1.606
8	6023.86	2.918	1.155	1.737
9	5074.86	3.241	1.141	1.879
10	4275.37	3.592	1.128	2.036
11	3601.83	3.976	1.117	2.206
12	3034.40	4.394	1.106	2.392
13	2556.36	4.851	1.097	2.595
14	2153.62	5.348	1.088	2.817
15	1814.35	5.891	1.081	3.058
16	1528.51	6.482	1.074	3.321
17	1287.71	7.126	1.067	3.607
$C_{a1} = C_{b1} = 1.5$ and $C_{a2} = C_{b2} = 1$				
18	1084.85	4.558	1.089	2.931
19	913.94	5.100	1.081	3.170
20	769.96	5.690	1.074	3.431
21	648.66	6.334	1.068	3.716
22	546.47	7.034	1.062	4.027
23	460.38	7.798	1.057	4.365
24	387.85	8.630	1.052	4.734
25	326.75	9.536	1.047	5.136
26	275.27	10.524	1.043	5.574
27	231.90	11.600	1.040	6.051
28	195.37	12.772	1.036	6.572
29	164.59	14.049	1.033	7.139
30	138.66	15.440	1.030	7.757
31	116.82	16.956	1.028	8.430
32	98.41	18.608	1.025	9.164
33	82.91	20.407	1.023	9.963
34	69.84	22.369	1.021	10.835

Table 1: capacitor values of the filter bank.