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OPNET Simulator of the ALAX: Preliminary Results

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1 Introduction

In this short report we briefly discuss the the results of various preliminary simulation runs which we have performed with the OPNET simulator of the ALAX. These results provide range estimate on the size of various buffers as well as a rough idea of the trade-offs which are involved between the processor and switching speed, and buffer sizes. In order to allow the simulations to stabilize quickly in this initial set of simulation runs the source used was a simple process with an embedded two–state Markov chain. More complex source models are described in the companion report [1] and will be considered during the next six months.

2 The Traffic Model

This model is driven by an underlying two–state Markov chain. with state space $\{1, 2\}$. As long as the Markov chain is in a particular state i, $(i = 1, 2)$. the source emits packets according to an i.i.d. Gaussian sequence with mean $m(i)$ and variance $\text{var}(i)$, i.e., if $X(n)$ denotes the packet size (in bits) generated during time slot n, then $X(n)$ is normally distributed with mean $m(i)$ and variance $\text{var}(i)$.

The underlying Markov chain transitions from state 1 to 2 with probability p, $0 < p < 1$. However on reaching state 2, it stays there just for one time slot and then returns back to state 1. In other words, the one–step transition probability

matrix $P \equiv (p_{ij})$ for the underlying two–state Markov chain has the form

$$p_{12} = p = 1 - p_{11}, \quad p_{21} = 1 \quad \text{and} \quad p_{22} = 0. \tag{2.1}$$

State 2 can be interpreted as representing a scene change of a VBR source. The steady–state probability vector for P is obtained by solving

$$\pi = \pi P, \quad \pi(1) + \pi(2) = 1 \tag{2.2}$$

It is easy to check that

$$\pi(1) = (1+p)^{-1}, \quad \pi(2) = p(1+p)^{-1}. \tag{2.3}$$

Here, we assume $m(2) = 2m(1)$ for sake of concreteness, and in steady state the net rate of this source is therefore given by

$$R = \mathbf{E}\left[X(n)\right] = m(1)(1+p)^{-1} + m(2)p(1+p)^{-1}. \tag{2.4}$$

The variances are scaled to the corresponding mean through the relation

$$\text{var}(i) = \frac{m(i)^2}{C(i)}, \quad i = 1, 2 \tag{2.5}$$

where $C(1) = 20$ and $C(2) = 400$.

The OPNET simulation model is summarized in Fig. 1. It contains an ATM source and three Ethernet sources; the traffic distribution is specified later.

Each source is generated according to the model described above. The said model is completely specified once we select the rate F at which packets are generated per time slot by the source; in other words F refers to the number of packets emitted by the source. For the simulation runs reported below, we have chosen the following values:

$p = 0.01595$;

$R = 12.10^6/F$ on the ATM side;

$R = 4.10^6/F$ on the Ethernet side.

We assume here that the ATM side transmits at 12 Mbps and all three Ethernet sources transmit at 4 Mbps each.

3 CASE 1: Effect of speed of the T9000 on the ATM side

We assume :

(i) The ATM side transmits to Ethernet side only and viceversa; the ATM source uniformly distributes its traffic to the three Ethernet destinations;

(ii) All sources transmit at 30 frames/sec;

(iii) The processor speed is given by $k\times$ (Interarrival time of Ethernet packet) with k varying from 0.1 to 0.5 in steps of 0.1. Here k refers to the "processor speed multiplication factor" so that $k = 0.5$ corresponds to being on the verge of instability;

(iv) The switch speed is 1 μsec per P1355–packet.

The results are shown in tabular form; Table 1 deals with the ATM side and Table 2 contains the results for the Ethernet side.

We notice that as expected the queue sizes decrease as processor speed increases on the ATM side. However the the effect on the Ethernet side is not much. This could be attributed to the following reasons:

(i) Queue-2b is the place where the P1355 packets coming from the C104 are collected. The effect of the burstiness of the ATM source is not felt here probably because of the smoothing effect of the switch;

(ii) Since there is no LAN emulation to be done on the Ethernet side the build up in queue-0b is only because of the context switching of the T9000;

(iii) The comparatively large buildup in the Ethernet side queue-1 (as compared to queue-1 on the ATM side) can be traced to the fact that there is contention between the three Ethernet modules transmiting through the switch to the ATM side. This contention is absent on the ATM side.

4 CASE 2: Effect of burst rate of the sources

We assume :

(i) The ATM side transmits to Ethernet side only and viceversa; the ATM source uniformly distributes its traffic to the three Ethernet destinations;

(ii) The ATM source transmits at an average rate of 12 Mbps while Ethernet sources transmit at 4 Mbps;

(iii) The frame rate varies from 10 frames/sec. to 60 frames/sec.;

(iv) The processor speed is given by $0.45\times$ (Interarrival time of Ethernet packet);

(v) The switch speed is 1 μsec per P1355–packet.

Th results are shown in tabular form; Table 3 deals with the ATM side and Table 4 contains the results for the Ethernet side. There are three entries under

each heading corresponding to the three Ethernet T9000's, and F refers to the number of frames (bursts) per second.

The queue buildup (on the ATM side) decreases as processor speed increases. However on the Ethernet side the effect is not significant. Again it is likely that this is due to the factors mentionned in Case 1.

References

[1] S. Rao, *Traffic Models for the OPNET Simulator of the ALAX*, Laboratory for Advanced Switching Technologies, University of Maryland, College Park (MD), 1995.

Table 1: **Case 1 – ATM side**

k hline	**Delay (sec.)**	q_{0a} **(mac)**	q_{1a} **(P1355)**	q_{3a} **(P1355)**	q_{4a} **(P1355)**	q_{5a} **(P1355)**
0.5	0.04	31.31	2.77	979	435	630
0.4	0.007	11.41	2.78	126	102.7	114.35
0.3	0.0038	7.8	2.78	61.3	53.02	58.7
0.2	0.00069	4.5	2.77	8.21	6.57	7.95
0.1	0.00041	.367	5.49	3.11	2.89	3.06

Table 2: **Case 1 – Ethernet side**

k hline	**Delay (sec.)**	q_{0b} **(mac)**	q_{1b} **(P1355)**	q_{2b} **(P1355)**
0.5	0.033	3.15	2548	788
hline		3.46	2637	1255
hline		3.44	2649	846
0.4	0.0123	3.15	2548	794
hline		3.47	2637	1255
hline		3.44	2649	846
0.3	0.008	3.15	2548	795
hline		3.46	2637	1255
hline		3.44	2649	846
0.2	0.0049	3.15	2549	795
hline		3.46	2638	1255
hline		3.46	2648	846
0.1	0.00059	3.15	2549	794
hline		3.46	2637	1255
hline		3.44	2648	846

Table 3: **Case 2 – ATM side**

F hline **(Frames/sec.)**	**Delay (sec.)**	q_{0a} **(mac)**	q_{1a} **(P1355)**	q_{3a} **(P1355)**	q_{4a} **(P1355)**	q_{5a} **(P1355)**
10	0.027	51.9	2.99	393	443.1	377.84
20	0.014	22.9	2.81	221	213	198
30	0.010	14.4	2.77	178.4	142.9	152.7
60	0.0058	7.15	2.7	87	84	88

Table 4: **Case 2 – Ethernet side**

F hline **(frames/sec.)**	q_{0b} **(mac)**	q_{1b} **(P1355)**	q_{2b} **(P1355)**
10	3.11	2452	572
hline	3.25	2528	757
hline	3.26	2500	794
20	3.27	2513	718
hline	3.25	2528	1327
hline	3.21	2570	889
30	3.15	2548	794
hline	3.4	2637	1255
hline	3.44	2649	846
60	3.36	2548	853
hline	3.21	2511	1139
hline	3.71	2590	864.5