

ABSTRACT

Title of Dissertation: A NOVEL CMOS IC SENSOR
FOR REMOTE RF SIGNAL SENSING

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This research dissertation reports the development of an RF sensor IC chip capable of tracking the directionality of RF remote emissions. The IC design uses an angle-of-arrival algorithm, and it is designed for the 180 nm CMOS technology, and also applicable to other technologies. The sensor chip requires two pairs of antennas aligned and placed at distance s for detection of azimuthal and polar angles of the RF incident wave. The circuit consists of custom designed low-noise amplifiers (LNAs) at the front-end, with a novel design of double-balanced Gilbert cell mixers (GCMs). This amplifies and mixes the signals from the antennas and converts the phase difference $\Delta\phi$ into an equivalent output voltage map suitable for an 18-bit analog-to-digital converter. Systematic optimization techniques were developed to maximize the third-order intercept point, and suppress flicker noise for the LNAs and GCMs, resulting in improved sensing accuracy. The overall system-level evaluation results showed state-of-art angle-of-arrival sensing capability with an upper limit error of 3.447° .

A NOVEL CMOS IC SENSOR
FOR REMOTE RF SIGNAL SENSING

by

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Dedication

I dedicate this doctoral dissertation to my parents and my girlfriend, Morgan for devotedly supporting and encouraging me to continue working on my doctoral studies. It would have been an impossible journey to get through without their endless care and gracious love.

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First, I would like to thank my research advisor, Dr. Agis Iliadis, for supporting me to commit myself to this amazing research opportunity and guiding me to finish my doctoral research dissertation. His unique academic perspective and kind mentorship truly led me to where I am now, as I am wrapping up my doctoral studying and dissertation. I would also like to express my gratitude to Dr. Aris Christou, Dr. Kevin Daniels, Dr. Alireza Khaligh, and Dr. Robert Newcomb for agreeing to be my dissertation committee members and providing remarkable academic reviews. Special thanks to my research group, Semiconductor Nanotechnology Research Laboratory member, Hyun-Soo Kim, and Muhammad Khan for assisting me with RF testing instruments and collaboration. I also thank Melanie Prange for always assisting me with the departmental administration. I cannot forget to express my appreciation to my Electrical and Computer Engineering department colleagues, Bathiya Senevirathna, Ankit Mondal, Proloy Das, Abhishek Chakraborty, Mike Zuzak, Yuntao Liu, Jaime Campos, Yongwan Park, and Yungjun Yoo for their encouragement and warm-hearted friendship, helping me to overcome difficult times and encouraging me. Lastly, I am forever grateful to my family and my girlfriend for always standing by me and encouraging me.

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List of Abbreviations

AoA	Angle-of-arrival
ADC	Analog to Digital Converter
BALUN	Balanced-to-unbalanced
CG	Common-gate
CS	Common-source
CVG	Conversion Gain
ESD	Electrostatic Diode
FoM	Figure of Merits
GCM	Gilbert cell mixer
GND	Ground
IF	Intermediate Frequency
IIP3	Input referred
IMD	Intermodulation distortion
IMD3	Third-order intermodulation distortion
IoT	Internet-of-Things
LIDAR	Light Detection and Ranging
LO	Local Oscillator
LNA	Low noise amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
PDK	Process Design Kit
RADAR	Radio Detection and Ranging
RF	Radio Frequency
SEM	Scanning Electron Microscope
SNR	Signal to Noise Ratio
TOA	Time of Arrival
TDOA	Time Difference of Arrival
W	Width

Chapter 1: Introduction

1.1 Research Motivation

In the rich RF spectrum of mobile communications, Wi-Fi, RADAR, digital data, and control systems, it is crucial to identify the RF interference signals that can threaten the cybersecurity of well-protected systems, and can breach the integrity of the system introducing malware and/or soft and hard errors. The origin and identification of such interference threats are critical. The need for a sensor for remote detection and identification of such RF signals is of paramount importance. In addition, the soaring market of automated vehicle systems is another field where recognition of the surrounding environment is vital, where RF communication often becomes a source for detection of nearby vehicles and surroundings. While there are some existing techniques that are employed in these situations, hardly any applications exist that are capable of appropriate sensing with reasonable flexibility which can be used in any situation and placement with compact size. Compact size applications are beneficial because they expand applications of these sensors widely. Flexibility is also important to be able to cover up various frequency ranges. Lastly, many existing implementations do not have enough robustness required to handle the harsh real RF environment. Therefore, developing a proper platform

with an IC processing chip is the most important step for development of a system which qualifies these special applications. In this context, the evolution of modern integrated circuits draws attention and shows enormous potential for realization of all types of analog electrical signal processing. Hence, this dissertation focuses on the development of an RF tracking sensor in CMOS integrated circuit (IC) technology to provide early detection of remote RF emissions.

1.2 Research Contributions

1.2.1 Design, Modeling and Evaluation of a Novel Angle-of-Arrival Sensor

A design, modeling, and proof-of-concept of an on-chip AoA system was accomplished, capable of accurate detection of remote RF emitter source tracking[15]. The sensor chip consists of optimized LNAs, double-balanced Gilbert cell mixers and local oscillator balance-to-unbalanced (LO BALUN) circuits. It captures phase difference information transforming it into an analog voltage map that can be post-processed by a microcontroller to provide the corresponding angle-of-arrival of the remote signal. This AoA system has wider sensing capabilities. It is easily repurposed to different ranges of frequencies, and applications. It is more accurate in comparison to traditional large-scale six-port interferometer AoA devices.

1.2.2 A Parametric Optimization Platform for Low Noise Amplifiers

The low noise amplifier parametric optimization platform was established based on the combination of the g_m/I_D algorithm and g_{m3} cancellation technique[13]. Specific parametric optimization guidelines were provided to maximize performance of interest. This design platform is expected to assist overcoming the optimization of RF front-end module, where analog circuit engineers often face challenges on meeting performance requirements due to complicated analog circuits trade-off relations.

1.2.3 A Novel Approach to Develop Universal Strategies for Gilbert Cell Mixers Design

This design methodology combines the current-bleeding method, the inductive resonance method, the g_m/I_D algorithm technique, and the flicker noise optimization technique to develop the key parameters necessary for the given application of AoA sensing[14]. This methodology can become a universal approach to optimizing the design of such Gilbert cell mixer modules.

1.3 Summary of the Dissertation

The design, modeling and evaluation of a novel RF directional tracking sensor IC is the main focus of this dissertation. Starting with the survey research on remote RF source tracking devices and discussion on overall system design ap-

proach, each specific module design and analysis are implemented, followed by the system-level evaluation of the designed RF sensor. Chapter 2 discusses previous research reports, and possible design approaches of remote RF source tracking. In the following, the system description of the remote RF directional tracking sensor IC along with theoretical background of the angle-of-arrival concept and antenna placement for the design of this sensor is presented. Chapter 3 concentrates on the design of a low-noise, high-linearity LNA. Various design techniques such as the g_m/I_D algorithm, the g_{m3} cancellation technique are studied and developed to meet the main focus of an LNA required for this sensor. Chapter 4 introduces a local-oscillator BALUN circuit to enhance and support the operation of the next Gilbert cell mixer stage. Important aspects including prevention of reverse-leakage and magnitude matching are studied and discussed in order to arrive at the optimal system. Chapter 5 reports the design and modeling of the novel double-balanced Gilbert cell mixer based on the combined optimization methodology developed in this work. The combined optimization methodology includes the current-bleeding, inductive resonance, g_m/I_D algorithm, and the flicker noise optimization techniques to suppress spurious signals and noise that inhibit angle-of-arrival sensing activity. In addition, a further optimization technique is discussed to put the LO transistors in optimal status. Chapter 6 discusses the circuit layout, the pad frame and the packaging effects. These aspects are critical for confident angle-of-arrival sensing, and are incorporated in the design process. The design strategy is investigated and developed to improve robustness and reliability of the sensor operation. Finally in Chapter 7, the detailed overall system-level evaluation is discussed, and experimen-

tal results from the first prototype are presented. The conclusion section of the dissertation is discussed. Future work and future directions are also included.

Chapter 2: Angle-of-Arrival Sensor Design and Development

2.1 Introduction

There are few applicable principles that utilize RF signals as sensing elements. Time-of-arrival (TOA) technique and Time-difference-of-arrival (TDOA) technique are the two main principles. These two approaches are both based on timely computation of RF signal reception. The TOA technique is rooted in the transmission of a signal and reception of the reflected. This requires complete implementation of transmitting and reception modules. Such transceiver operation can accomplish detection of target objects accurately by measuring time-of-flight.

The TDOA technique concentrates on the signal reception time difference between two signal receivers or more, to track a signal origin. It is solely based on processing the received signal information, and hence is conceptually a passive application in comparison to TOA devices. For example, multilateration algorithm is a great example of an RF positioning system. However realization of the multilateration algorithm requires a room-scale distance between multiple sensor nodes (stations) for successful few nanoseconds-scale time sensing which expands system scale dramatically. In addition, ultra-high sampling rate ADCs above Gbps are necessary to post-process very short time differences. The scarcity of such high-speed

ADCs and scattering sensor nodes in room-scale space constrain the portable-size implementation of a sensor, making it impractical. Alternatively, an angle-of-arrival algorithm can be used for RF directional sensing. A six-port interferometer system has been used for angle-of-arrival sensing[55]. However, the angle-of-arrival detection through this system is inherently limited by the sensing range dependency on the placement of the antennas and the phase detection mechanism.

To overcome the prerequisites of scattered RF sensor stations for multilateration and the limited angle-of-arrival detection range of a six-port interferometer, a CMOS IC-based RF directional sensor is developed and introduced in this dissertation that consists of LNAs and double-balanced Gilbert cell mixers (GCM) that allow phase detection for angle-of-arrival computation. The sensor provides high angle-of-arrival accuracy, and also enables flexible RF incident angle-sensing range regardless of antenna placement. Moreover, the integration of the whole system into a single chip greatly reduces the physical scale of the sensor and extends its use to a wider range of applications such as automotive, airspace, and medical technologies.

The CMOS IC chip is composed of custom designed LNAs coupled with either on-chip, or external mini-chip antenna modules at the front-end. It includes a double-balanced GCM and low-pass filters for phase detection, targeting a frequency of $f_c = 2.4\text{GHz}$, which can be tuned to a wider range of frequencies to target different applications. The content discussed in this chapter was published in [15].

2.2 Survey Research

An RF location tracking sensor is required to sense two types of information for accurate source location tracking which are direction and distance. To begin, relevant algorithms are introduced to achieve these goals. Such algorithms are either used to track the distance to the sensing object or directional or distance information of an RF emitter, or a coordinate which practically provides both direction and distance information at the same time.

2.2.1 The TOA-based Positioning Systems

The RADARs and LIDARs are the commonly known examples of TOA technique-based applications[11][48]. Fig. 2.1 shows the block diagram of the wide-angle laser ranging system that is based on the TOA principle [9]. In spite of development of alternative algorithms that can achieve similar functionalities, this is still a highly praised algorithm for applications because of its long-proven technical reliability.

However, these devices inherently demand higher power dissipation due to their fundamental technical constraints, and also have the potential to expose their origins by transmitting signals, which can negate their usages critically in situations such as military applications that require stealth features.

2.2.2 The TDOA-based Multilateration

The TDOA-based MLAT algorithm senses the target RF emitter's location by using signal reception-time difference between each station. Each distinct signal

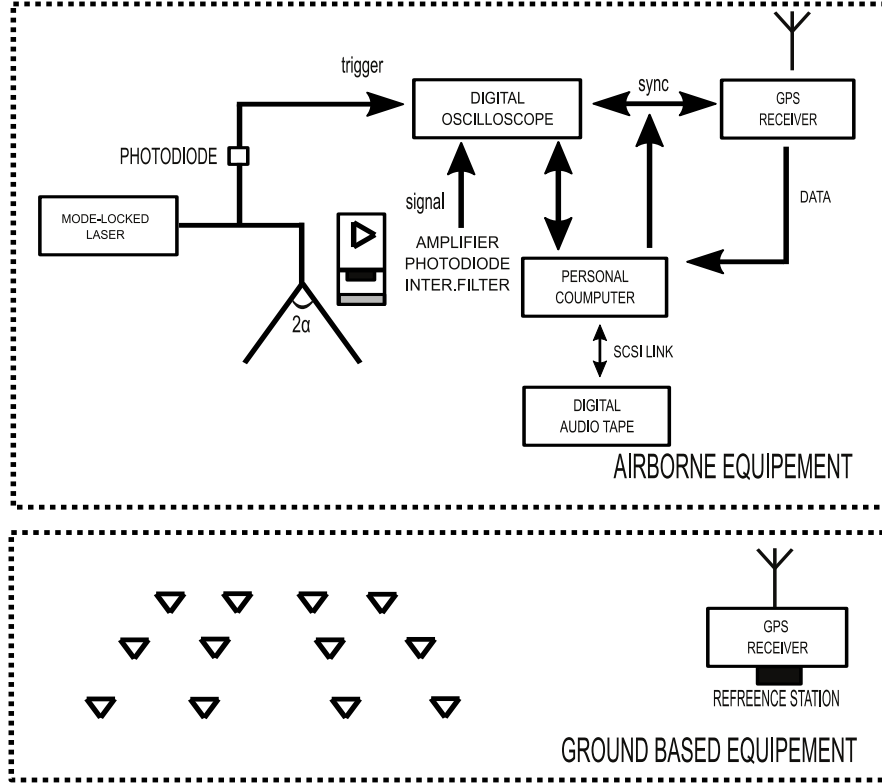


Figure 2.1: Block diagram of the wide-angle airborne laser ranging system[9].

path of the received signals at each antenna that originate from the signal source location contributes to a reception time difference among them. These reception time differences with respect to the signal source, set mathematical relations that represent potential emitter locations formed in hyperbolic surfaces as represented in Fig. 2.2. Studies reported by Szullo et.al. [52] showed great potential of the MLAT technique for positioning an unmanned air vehicle application. The unique single point of the emitter's origin can be calculated by specifying the intersection of these hyperbolic surfaces that are formed by multiple TDOAs from antenna pairs. An animation of the MLAT with an RF emitter E is shown in Fig. 2.3. A pair of antenna stations R_0 , R_m and reception time difference τ_{0m} form the Equation 2.1.

$$\begin{aligned}
R_{m0}^2 &= (v \cdot \tau_{m0} + R_0)^2 \\
R_{m0}^2 &= (v \cdot \tau_{m0})^2 + 2 \cdot v \cdot \tau_{m0} + R_0^2 \\
0 &= (v \cdot \tau_{m0})^2 + 2 \cdot v \cdot \tau_{m0} \cdot R_0 + R_0^2 - R_{m0}^2 \\
0 &= v \cdot \tau_{m0} + 2 \cdot R_0 + \frac{R_0^2 - R_{m0}^2}{v \cdot \tau_{m0}}
\end{aligned} \tag{2.1}$$

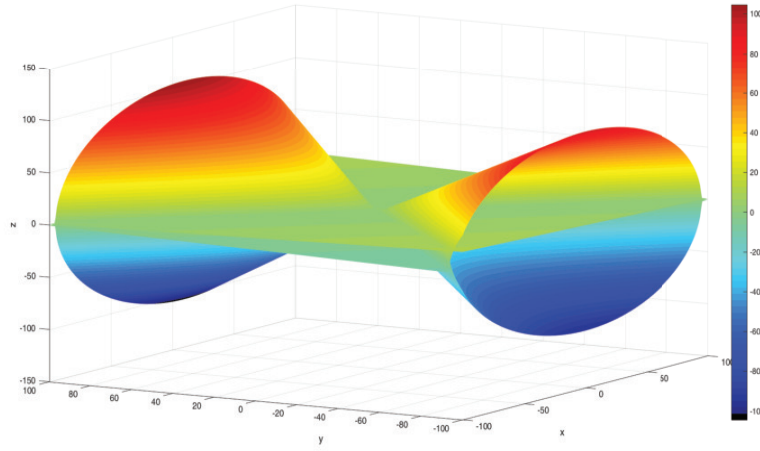


Figure 2.2: Visualization of hyperboloid surface as a result of time difference between two antennas.

The sensing station coordinates R_m and R_0 are given since the placement of stations is determined by the system designer. Assuming the TDOA between the pair of station τ_{m0} is given which must be measured in a real device, it can be multiplied by the speed of electromagnetic waves since it travels in the air which is equivalent to the difference of the signal path $d_{diff} = c \cdot \tau_m$. These relations are presented in hyperbolic surfaces which are infinite sets of the emitter's possible location. Since hyperbolic surfaces are formed in three-dimensional space, equating each 3rd order hyperbolic surfaces provides a 2nd order solution in two-dimensional space, forming an intersecting line. Similarly, equating these 2nd order solutions

provide a 1st order solution, which becomes the unique source origin coordinate. It requires at least three pairs of stations to determine a target location. Therefore the system can be formed with four antennas, for example, which formulates six unique sets of hyperbolic equations.

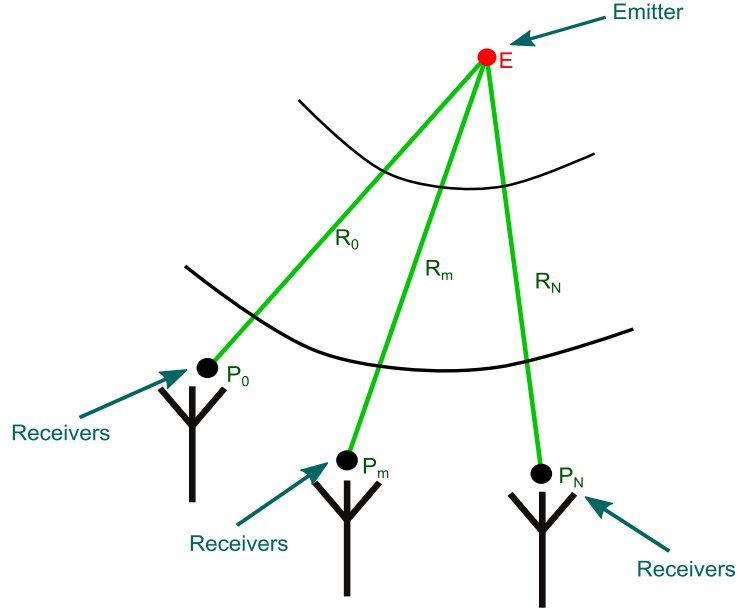


Figure 2.3: TDOA-based multilateration geometry

Although the description above thoroughly demonstrates the theoretical background of the MLAT algorithm, a realization of the MLAT system faces multiple challenges. The first problem is the difficulty of sensing the time difference of arrival between each station, which is only a few nanoseconds. It demands extremely fast-sampling speed ADCs (above 10Gbps) to be capable of sensing the time in this scale. Such ADCs are difficult to implement due to physical constraints to sample signals on time. The other problem is the matter of time synchronization at reception stations. Before the received signals from each station enters into the digital

processing units, it is imperative that the signal stations are all synchronized in timing to avoid miscalculation of the signal origin. Various off-synchronization sources such as propagation delay and RC delay can incapacitate and negatively impact accurate time difference sensing. These two major systematic requirements lead to serious challenges in the realization of this technique, although the algorithm can be a great solution for signal sources with much lower propagation velocity such as acoustic waves or sonar waves. An alternative approach is the angle-of-arrival algorithm.

2.2.3 The TDOA based Angle-of-Arrival with Six-Port Devices

There is another algorithm based on the TDOA, the angle-of-arrival. It utilizes phase differences in two antennas to compute the signal origin. The major difference between the multilateration and the angle-of-arrival is that multilateration computes the coordinates of a signal origin while the angle-of-arrival computes the direction of a signal origin with respect to the sensor station. Laemmle et.al.[\[30\]](#) came up with a six-port device to realize an implementation of an AoA sensor. The six-port interferometer has a long history ever since the first introduction by Engen and Hoer[\[18\]](#). A six-port interferometer has wide applications such as in demodulation, modulation, radar, and power detection, while angle-of-arrival sensing is one of its major uses. It consists of the two input and the four output ports by forming six ports in total. For angle-of-arrival application, it requires three 90 degree phase-shifting couplers and one Wilkinson power divider to process the two input

signals into the four different relative phased outputs (Fig. 2.4) [21]. While the devices accomplished the emitter tracking that covers certain ranges showing potential for the AoA sensing, but it does have limitations. First, the sensing range is extremely limited. Only the incident angle of up to ~ 5 degrees is detectable which restricts practical sensing significantly in a real environment. Second, it is highly antenna-distance dependent. The antenna distance in the device crucially affects the incident angle detection range which impacts detection flexibility to be unreliable. In addition, the complexity of the system demanding couplers and a power divider for the six-port device adds instability to the sensing activity.

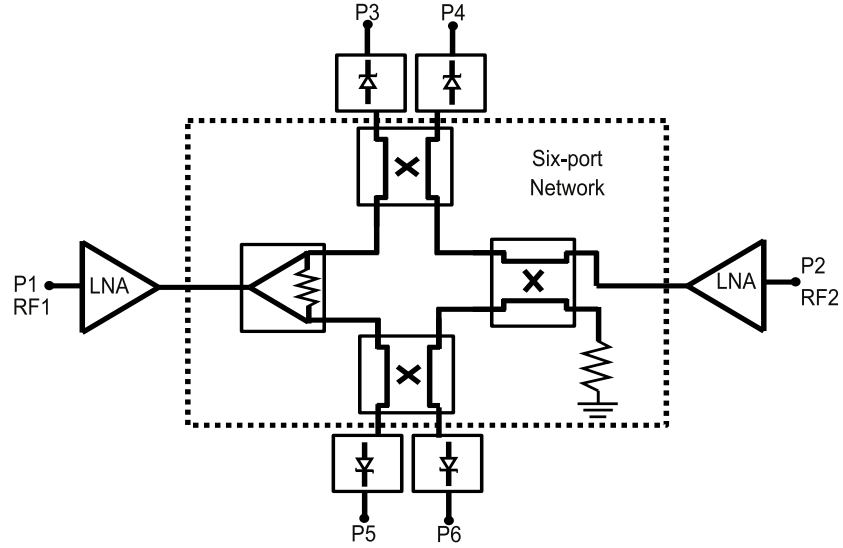


Figure 2.4: The schematic overview of the integrated six-port system including two LNAs, four power detectors, and a passive six-port network[21].

Similarly Alexander Koelpin et.al.[28][54] reported a six-port interferometer for an angle-of-arrival application. Combinations of the two inputs form the phase-shifted superposition outputs where these are down-converted through power detec-

tors (Fig. 2.5)[53]. The device applied the angle-of-arrival algorithm to compute direction of an RF source by focusing on phase difference between the signals received by the two antennas. Hence the essence of its application is on phase detection through the four output ports.

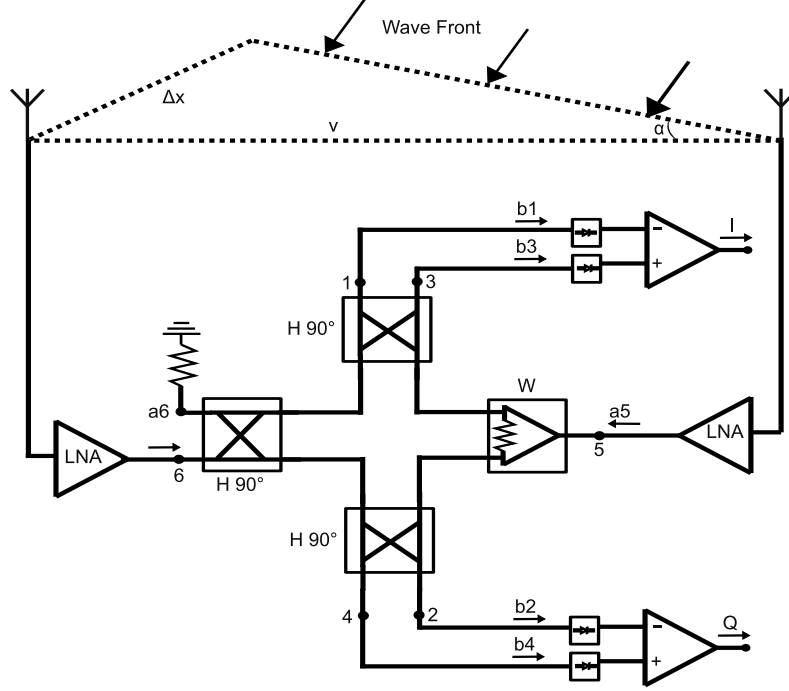


Figure 2.5: An AoA detector based on one six-port system[53].

While the angle-of-arrival algorithm is an efficient way for emitter tracking, the idea can be achieved in a more reliable and efficient way. The most important thing is to secure accurate sensing and to cover a wide variety of frequencies, regardless of antenna placement by overcoming the inherited limitation of a six-port interferometer device. A transistor-based IC sensor was chosen in this dissertation as a platform to achieve accurate and reliable AoA.

2.3 System Description

The fundamentals of the angle-of-arrival (AoA) sensing technique based on multiple antennas are discussed in this section, followed by a system description and the sensing mechanism of the system. Essential modules of this sensor demand optimal design of LNAs and GCMs. To these, the systematic optimization processes of the LNAs, the BALUNs, and the GCMs are mandatory, concentrating on suppression of noise and enhancing linearity.

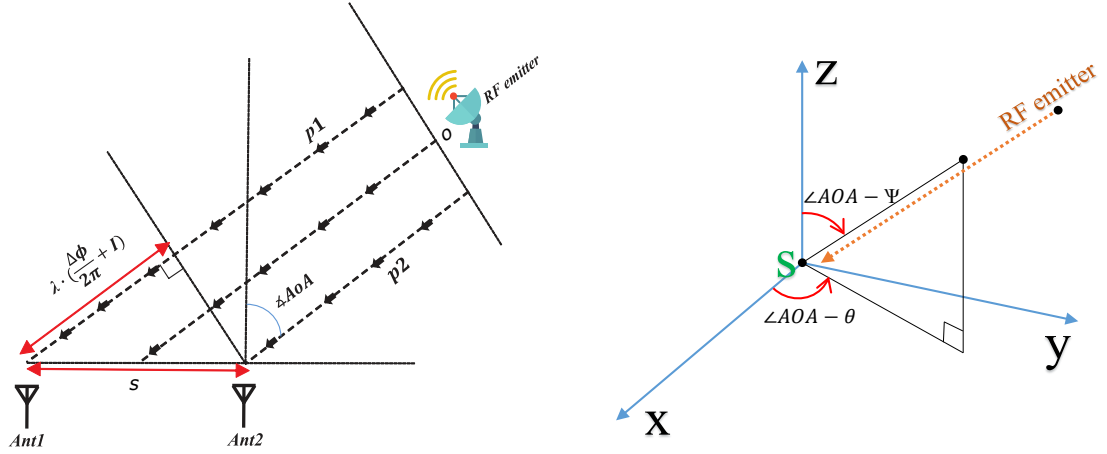


Figure 2.6: (a) Angle-of-arrival diagram in planar view. The RF emitter O is shown as a single point from $Ant1-\theta$ and $Ant2-\theta$ that are placed in distance s . (on left)
(b) Angle-of-arrival diagram in 3D view showing the azimuthal and polar angle of the RF incident wave. (on right)

2.3.1 Angle-of-Arrival Fundamentals and Antenna Placement

Fig. 2.6(a) displays the example of an RF incident wave entering into the RF sensor in the angle $\angle AoA$. It depicts the RF emitter location at O , the RF propagation paths $p1$ and $p2$ and the antenna placement at $Ant1-\theta$, $Ant2-\theta$. The RF propagation path $p1$ travels the extra distance $\lambda((\Delta\phi/2\pi) + I)$ until it reaches

$Ant1 - \theta$ compared to the distance that the path $p2$ that travels to $Ant2 - \theta$ from O , the signal origin. λ , the wavelength of RF signals, is equal to $\lambda = c/f_c = 12.5(cm)$ for $f_c = 2.4GHz$. $\Delta\phi$ represents the phase difference between $p1$ and $p2$ entered $Ant1 - \theta$ and $Ant2 - \theta$. The two antenna positions $Ant1 - \theta$ and $Ant2 - \theta$ are separated by the distance s . The distance s is correlated to I and is always larger than $\lambda(\Delta\phi/2\pi + I)$ as it is shown in Fig 2.6(a). I represents the multiples periods of the received signal that the extra distance $p1$ travels and can be 0 or any natural numbers which does not restrict the AoA detection range and is determined by the antenna distance s . Based on Fig 2.6(a), the angle-of-arrival $\angle AoA$ can be shown as Equation 2.2.

$$\sin(\angle AoA) = \frac{\lambda(\frac{\Delta\phi}{2\pi} + I)}{s} \quad (2.2)$$

This equation can be simplified when the antennas are placed at the distance of the target signal wavelength $s = \lambda$ which then automatically determines I to be 0 since $s \leq \lambda((\Delta\phi/2\pi) + I)$ must be valid. This antenna placement is the closest distance possible between $Ant1 - \theta$ and $Ant2 - \theta$ and consequently minimizes the system scale. The angle-of-arrival $\angle AoA$ can be rearranged in Equation 2.3.

$$\angle AoA = \sin^{-1}\left(\frac{\Delta\phi}{2\pi}\right) \quad (2.3)$$

An implementation of this sensor is achieved by detection of $\Delta\phi$ from equation 2-10. The $\Delta\phi$ detection is accomplished both on antenna pairs that are aligned on the X-Y plane and Y-Z plane to detect AoA in azimuthal and polar angle,

respectively as shown on Fig. 2.6(b). Both antenna pairs are placed in the same distance $s = \lambda$.

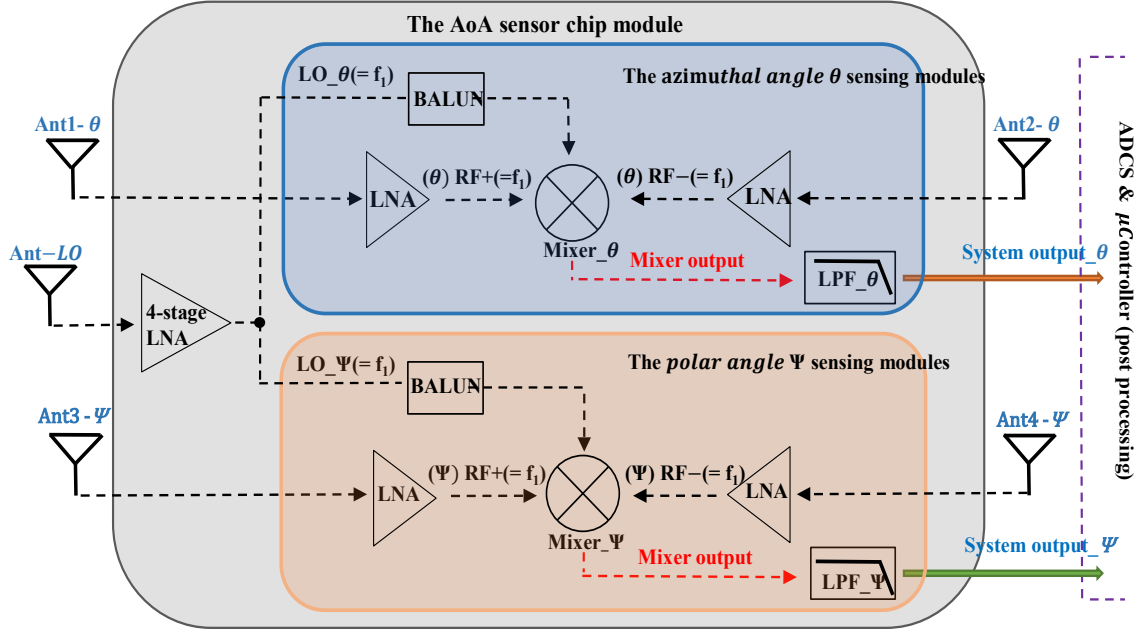


Figure 2.7: The system block diagram (grey area) consisting of two identical pairs of AoA modules for the detection of azimuthal and polar angle.

2.3.2 System Block Diagram and AoA Detection Algorithm

Fig. 2.7 shows the system block diagram. The front-end modules consist of a pair of the antennas $Ant1-\theta$ and $Ant2-\theta$ for the azimuthal angle detection and the low noise amplifiers to amplify the received signals while maintaining a reasonable signal to noise ratio. The next stage is the double-balanced GCM. It mixes the RF input signals with the Local Oscillator (LO) signal where the RF+ and RF- signals are fed to the amplified signals of $Ant1-\theta$ and $Ant2-\theta$, respectively. The RF+ and RF- inputs of the GCM are not differential input signals as in traditional applications, but are single-ended with the phase difference of $\Delta\phi$. By applying

the RF+ and RF- into the GCM this way, it enables phase detection between the signals at $Ant1 - \theta$ and $Ant2 - \theta$ when mixing them with the LO signal. The LO input is fed to the $Ant - LO$ to guarantee an identical carrier frequency f_c to the RF input for zero-IF mixing since $Ant - LO$ and the pair of $Ant1 - \theta$ and $Ant2 - \theta$ receive the same RF source signal. It is amplified through the four-stage LNAs and converted to the differential-ended LO+ and LO- by an LO BALUN circuit. Multistage amplification of the LO signal is required to secure enough magnitude to guarantee switching operation of the LO stage transistors for a clear multiplication in the GCM. The output of the GCM can be derived mathematically into Equation 2.4, 2.5. where $RF+ = C \cos(\omega_1 - \kappa x_1)$, $RF- = C \cos(\omega_1 - \kappa x_2)$ and $LO+ = D \cos(\omega_1 - \alpha)$, $LO- = D \cos(\omega_1 - \alpha + 180^\circ)$.

$$V'_{OUT+} = V_{max} \cos(2\omega_1 - (\kappa x_1 + \alpha)) + V_{max} \cos(-\kappa x_1 - \alpha) \quad (2.4)$$

$$V'_{OUT-} = V_{max} \cos(2\omega_1 - (\kappa x_2 + \alpha + 180^\circ)) + V_{max} \cos(-\kappa x_2 - \alpha + 180^\circ) \quad (2.5)$$

Filtering the first $2\omega_1$ term out using low-pass filters, it leaves Equation 2.6, 2.7.

$$V_{OUT+} = V_{max} \cos(-\kappa x_1 - \alpha) \quad (2.6)$$

$$V_{OUT-} = V_{max} \cos(-\kappa x_2 - \alpha + 180^\circ) \quad (2.7)$$

which are the outputs of this present system. These filtered DC outputs are converted to digital by ADCs and coupled to a microcontroller. A microcon-

troller matches DC voltages V_{out+}/V_{max} and V_{out-}/V_{max} to a corresponding phase angle of $\cos$ function (Equation 2-8, 2-9), which in this case are $-\kappa x_1 - \alpha$ and $-\kappa x_2 - \alpha + 180^\circ$.

$$-\kappa(x_1 + \alpha) = \cos^{-1}(V_{out+}/V_{max}) \quad (2.8)$$

$$-\kappa(x_2 + \alpha + 180^\circ) = \cos^{-1}(V_{out-}/V_{max}) \quad (2.9)$$

Next, subtract Equation 2.8 and Equation 2.9 to attain the phase difference represented in Equation 2.10.

$$\Delta\phi = \kappa x_1 - \kappa x_2 \quad (2.10)$$

Which is the phase difference of the RF+ and RF- input and completely independent of the phase α of the LO signals. Lastly, simply mapping $\Delta\phi$ to the corresponding $\angle AoA$ from Equation 2-3 concludes the angle-of-arrival sensing. The same process is repeated for the polar angle detection set. As the detection algorithm is represented above, the major key factor of accurate angle-of-arrival sensing is at the precise detection of $\Delta\phi$.

2.3.3 Post-Processing Examination

Microcontrollers are available to process data converted by ADCs. Since most of modern microcontrollers include ADCs within them, it is possible to instantly data-process analog inputs. Therefore, a microcontroller including two ADCs is

applied externally for the post-processing in this system. The post-processing should be achieved in the following order. First, receive the analog voltage V_{out+} and V_{out-} on the ADCs. Second, convert these two into digital. Third, divide the converted V_{out+} and V_{out-} by V_{max} . Fourth, apply arccosine on these two values. Next, subtract these two to finally get $\Delta\phi$. Finally, $\Delta\phi$ is mapped to $\angle$ AoA based on the table internally programmed in a microcontroller to finalize the AoA sensing. The higher the resolution of ADCs are, the more accurate sensing is achievable.

2.3.4 Antenna Arrangement

Antennas are the very first front-end signal receivers and as discussed above, this sensor is designed with four antennas. Possible antenna types for this sensor are on-chip antennas and mini-chip antenna modules. However, implementation of an on-chip antenna in this RF sensor can be difficult, while it is an attractive option if it can be designed, since these antennas require a sophisticated ground plane that has to be completely independent from any devices nearby for concrete resonance at a target frequency. The ground plane in this case would be silicon substrate which is composed of many different circuit devices and metal traces. Securing completely isolated antenna modules is not realistic. Alternatively, mini chip antenna modules are ready-to-go commercial antennas which can easily be applied and become a great option. The benefit is much less noise and interruptive sources, as they are protected with an isolated ground plane for sensitive antenna devices.

Beamforming and gain determine the signal reception range at the antennas

hence these two factors must satisfy the sensor's requirement to be eligible to sense signals from all direction. Therefore, beamforming of the antennas to be used must be isotropic, meaning it has to retain homogenous and universe gain through spherical space. Antennas of 0 dBi are ideal candidates. One of the great example antenna modules is the Johnson technology's antenna module 2450AT42E0100, that shows excellent characteristics for this application with the peak gain of -2.0 dBi, frequency bandwidth of 2.4G~2.48GHz and 50Ω impedance[1]. Fig. 2.8 shows the PCB layout of the chip antenna where the ground plane comes with a 50 mm x 30 mm platform and the chip antenna is designated a space of 3 mm x 6.3 mm in the yellow footprint. Fig. 2.9 shows a detailed layout in achieving 50Ω impedance matching using the LC network involving stubs, inductors, and capacitors. At the end of the trace is where a BNC connector can be connected to through the 50Ω feed line.

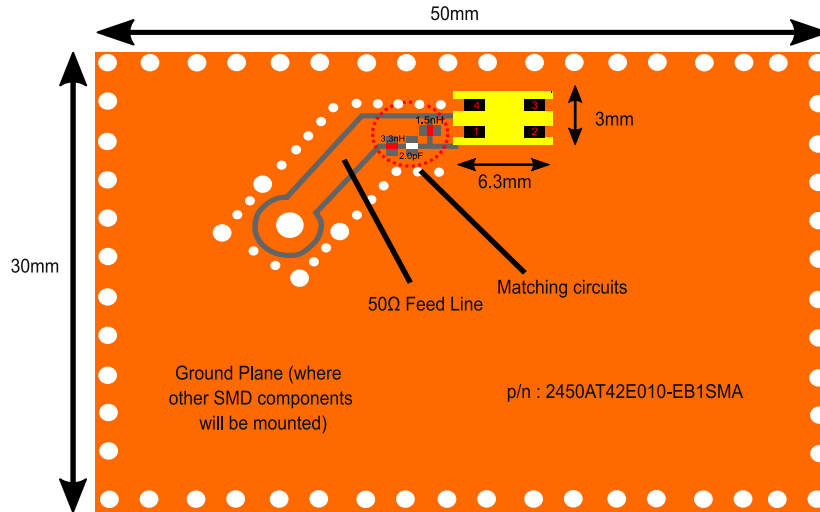


Figure 2.8: PCB layout of the antenna module[1].

The placement of four of these antenna modules can be achieved on the RF

sensor PCB where the RF sensor IC, external components, and the antenna modules are all placed, space permitting as shown in Fig. 2.10. BNC connectors are applied to hardwire each of the antenna modules and the RF sensor chip through coax cables.

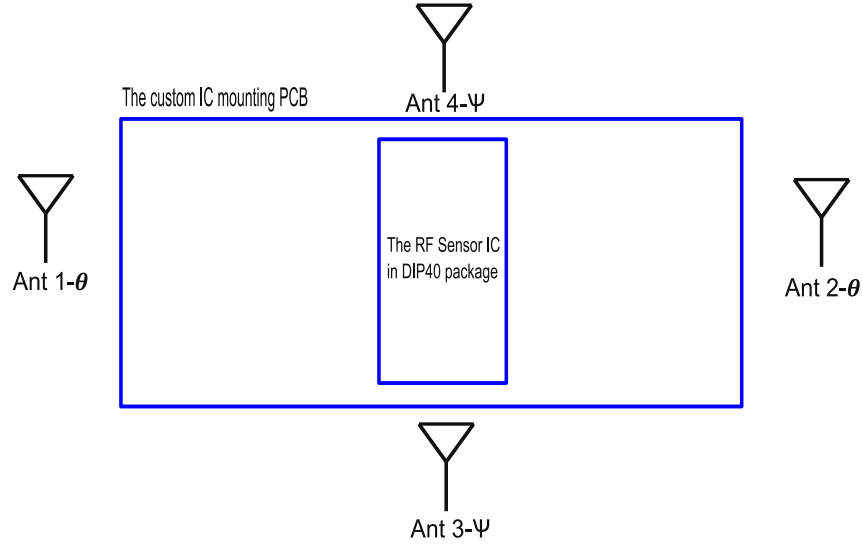


Figure 2.9: Geometries of the antenna system, RF integrated circuits and its mounting PCBs.

It is possible to achieve a pocket size system in the RFIC platform including the antenna modules, the RFIC in DIP40 package and the mounting PCB, even though this antenna module takes the space of 50mm x 30mm, which is larger scale than that of on-chip antennas.

2.4 Summary

This chapter discusses a design approach for a novel angle-of-arrival sensor, followed by the theoretical background of TDOA based angle-of-arrival algorithm. The sensor is founded on transistor devices as an integrated circuit, targeting a system-

on-chip application. The module design's unique approach exploits low noise amplifiers, double-balanced Gilbert cell mixers, and LO BALUNs for effective on-chip phase detection. It represents superior sensing potential for six-port interferometer implementations by revealing flexible detection bandwidth which can easily be re-tuned if needed, and better angle-of-arrival detection range which is independent to antenna placement. Lastly, antenna candidates appropriate for this sensor application were discussed.

Chapter 3: Modeling High Linearity Low Noise Amplifiers

3.1 Introduction

The current congested RF spectrum of mobile communications, internet-of-things (IoT), RADAR, wireless internet, and digital systems, they can be exposed to various sources of interference, resulting in critical cybersecurity threats[22]. Most systems utilize RF front-end modules such as low noise amplifiers (LNAs) and mixer circuits. Reliable modeling and implementation of such integrated circuits is increasingly more challenging due to the evolving submicron technologies. For this reason, this chapter introduces an efficient optimization technique and analysis of an LNA that combines the g_m/I_D algorithm, the g_{m3} cancellation technique and the figure of merit (FoM) index method. The design concentrates on low noise and high linearity applications to guarantee robustness in congested RF environments while still providing sufficient levels of power gain, bandwidth, and power dissipation. Current submicron CMOS technology requires a design strategy different than traditional design approaches, due to enhanced short channel effects and increased parasitic effects. Previous studies demonstrated the reliability of the g_m/I_D design approach for submicron technologies[19][40]. This design approach characterizes a transistor model for quantitative analysis by developing lookup charts of pre-evaluated data

of g_m/I_D , f_t , and I_D/W . Another index that specifies trade-off factors analysis of a transistor model, is the figure of merit (FoM). Often times, analog/RF integrated circuits deal with various performance factors such as gain, linearity, power, and noise. Hence, circuit designers have to make appropriate decisions to satisfy specific design requirements and the FoM becomes a clear indicator to quantify the design validity. The g_{m3} cancellation technique is another powerful technique to reduce inherent nonlinearity of transistor devices. Combining these three design methods results in developing an optimal solution reaching the design goals effectively.

Low noise amplifiers are located in between the 50Ω antennas and the Gilbert cell mixer stage and are important front-end modules since the received RF signal has to be properly amplified for precise angle-of-arrival sensing. Any noise in the RF signal from the front-end modules can negatively, and critically impact the angle of arrival sensing result. This is because noise from the earlier stage accumulates as it goes toward the system output according to the Friis formula[29] which is Equation 3.1.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \quad (3.1)$$

In this chapter, different topologies for LNA design are examined in order to arrive at the best topology for the LNAs for this RF sensor. Then the combined optimization methodology mentioned above is introduced to get the best performance for the given topology, followed by result analysis of the design. The content

discussed in this chapter was published in [13].

3.2 Comparison of LNA Topologies

There are various LNA topologies developed and used in a wide range of applications. Common-source, common-gate, and cascode low noise amplifiers are the most commonly used topologies. Each has pros and cons and their characteristics can provide a platform to determine an optimal topology for this application. The common-source amplifier features high input impedance, while it has relatively low noise since it only consists of a single transistor. Its gain is moderate and so is its linearity. Its reverse isolation is relatively low which derives from the feedback parasitic capacitance C_{gd} feeding the input and output, causing reverse leakage and a stability issue. The common-gate amplifier shows the smallest input impedance among the three topologies and readily allows impedance matching with a standard 50Ω antenna. Also, high reverse isolation owing to relatively small feedback capacitance C_{ds} (compared to C_{gd}) enhances stability. However, it has relatively low gain, and noise figure that rises significantly along frequency. Third is the cascode topology. It provides high gain due to the stacked structure with two transistors and has the highest linearity due to high input and output isolation. In terms of stability, it is better than the common-source (CS) amplifiers since the input and output transistors are separated, which minimizes the feedback effect. However, its noise level can only be higher than the CS topology amplifiers stemming from the cascode topology that comes with two transistors. Table 1 shows the comparison of

these three topologies.

Characteristic	common-source	common-gate	cascode
Noise Figure	Lowest	Rises rapidly with frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly broad	Broad
Stability	Often requires compensation	Higher	Higher
Reverse Isolation	Low	High	High
Sensitivity to Process Variation, Temperature, Power Supply, Component Tolerance	Greater	Lesser	Lesser

Table 3.1: Comparison of the Three LNA Topologies[17][33][6].

To enhance and achieve better performance, there are various modified topologies reported, based on these three topologies. First is the folded cascode amplifier. It consists of NMOS and PMOS transistors in parallel. The biggest advantage of this topology is that it extends the output swing range by $1 \cdot V_{ov}$ when compared to the cascode amplifiers, allowing more headroom for the output signal. Second is the shunt feedback amplifier. It has RC feedback interconnecting the input and output of the common-source topology. In this way, the effective gain becomes less affected by the gain of the amp itself and it enhances linearity and expands bandwidth. It is especially advantageous with its ability to maintain input and output impedance matching over a wide range of frequencies.

The topological analysis and focus on the few critical design factors provide guidance to narrow down an optimal topology for this particular application. The

goal is to provide an accurate phase detection of $\Delta\phi$ which is heavily influenced by noise, jitter, and third-order intermodulation distortion (IMD3) effects. These factors can be controlled and optimized based on (a) choosing an appropriate topology, and (b) developing improvements through further optimization. Both of these two design strategies are important particularly because it is a front-end module that propagates its effect to the adjacent modules. For these motivations, the common-source LNA can be a great choice due to its low noise nature and better immunity to process variation and power supply variation. In addition, relatively fewer restraints on space and power consumption of this application makes the use of the common-source topology here more suitable. Various design parameters such as total gate width, finger length per width and number of fingers, RF shielding guard rings, layout factors and many more are considered and adjusted to satisfy the requirements.

3.3 Noise Analysis

In this section, noise analysis is discussed to be utilized for LNA optimization. Noise analysis is a complicated process as it is often correlated to several factors such as gain, power, bias, and linearity, as shown in Fig. 3.1 where the analog design trade-off octagon is shown. For the application developed here, our combined optimization methodology takes targets noise, linearity and gain into an account. To get a lower noise figure, certain degrees of gain should be sacrificed. In addition, linearity of devices is correlated to both noise and gain level. Therefore the design goal is to characterize noise figure, S_{21} , IIP3 and their relations to find a balance

among them.

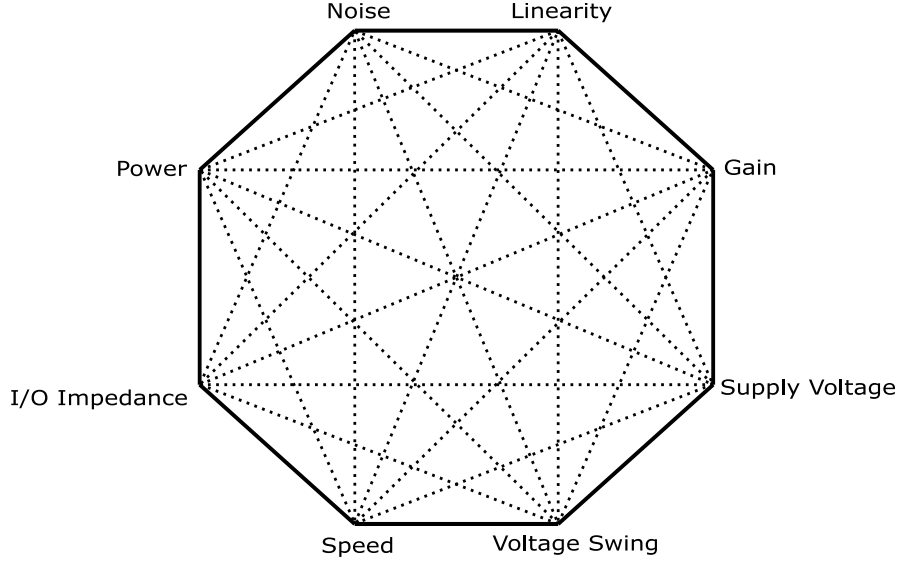


Figure 3.1: Analog design octagon showing trade-off relation among design factors[44].

There are different kinds of noise sources in LNAs. Channel noise, source resistor noise, gate resistance noise, induced gate noise and flicker noise are the major noise sources that appear in integrated circuits. Shot noise and, substrate resistance noise also exist but these will be disregarded since they are negligible compared to the other noise sources that are listed above. Both the channel noise power density spectral i_d^2 (Equation 3.2) and the induced gate noise power density spectral i_g^2 (Equation 3.3) are thermally derived and are defined, respectively. g_g represents the zero-bias gate conductance (Equation 3.4)[31].

$$\overline{i_d^2} = 4kT\Delta f\gamma g_{d0} \quad (3.2)$$

$$\overline{i_g^2} = 4kT\Delta f\delta g_g \quad (3.3)$$

$$g_g = \frac{(\omega C_{gs})^2}{5g_{d0}} \quad (3.4)$$

where Δf is the bandwidth, γ and δ are both bias dependent parameters, T is temperature and k is Boltzmann constant. The channel noise and induced gate noise are correlated and their relation i_g^2 and i_d^2 is defined by Equation 3.5[31].

$$\kappa = \frac{\overline{i_g}^2}{\overline{i_d}^2} = \frac{\delta g_g}{\gamma g_{d0}} = \frac{\delta \omega_0^2 c_{gs}^2}{\gamma 5 g_{d0}^2} = \frac{\delta \alpha^2 \omega_0^2}{\gamma 5 \omega_t} \quad (3.5)$$

As shown from Equation 3.5, the gate noise is much smaller than the channel noise since the gate noise to channel noise proportion increases as operation frequency increases toward the unity gain frequency ω_t , while the channel noise is independent to operation frequency. For most applications, ω_0 stays below ω_t and channel noise is more dominant accordingly. Flicker noise, on the other hand, is dominant in a low frequency domain, and is the main interest for the Gilbert cell mixer stage since it operates with zero-IF mixing. In the LNA stage, channel noise and induced gate noise are of primary interest since they deal with high RF frequency signals, targeting the operation frequency of $f = 2.4\text{GHz}$.

A small signal model of a common-source amplifier is shown in Fig. 3.2 for closer look into noise analysis. The three noise sources here are i_{Rs} , i_g and i_d , which are the source resistance noise, gate noise and channel noise, respectively, related to the total output noise i_o , and it should be calculated using a small signal model. The output noise contribution from the source resistance noise $I_{o,Rs}$ (Equation 3.6), channel noise $I_{o,d}$ (Equation 3.7), and gate noise $I_{o,g}$ (Equation 3.8) can be indepen-

dently described as the following based on the small signal model in Fig. 3.2[31].

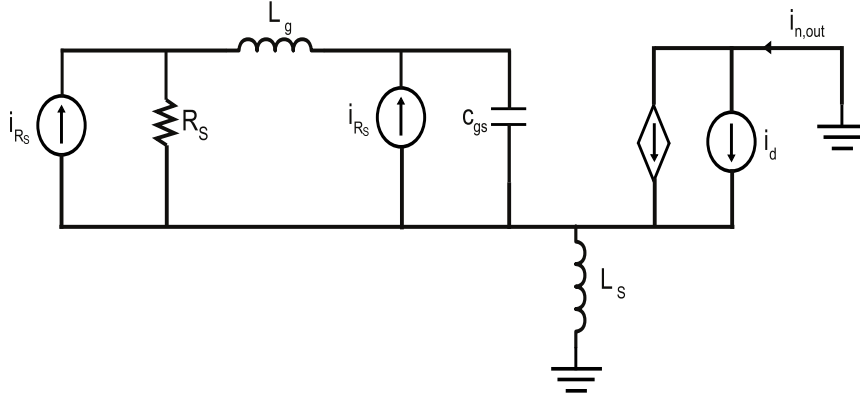


Figure 3.2: An equivalent small signal model for noise analysis[31].

$$i_{o,Rs} = \frac{R_s}{R_s + \omega_t L_s} \frac{g_m}{s C_{gs}} i_{Rs} = \frac{R_s}{R_s + \omega_t L_s} \frac{\omega_t}{j\omega} i_{Rs} \quad (3.6)$$

$$i_{o,d} = \frac{R_s}{R_s + \omega_t L_s} i_d \quad (3.7)$$

$$\begin{aligned} i_{o,g} &= \frac{R_s}{R_s + \omega_t L_s} \frac{g_m}{s C_{gs}} \left(1 - \frac{1}{s C_{gs} R_s}\right) i_g = \frac{R_s}{R_s + \omega_t L_s} \frac{g_m}{j\omega C_{gs}} \left(1 - \frac{1}{j\omega C_{gs} R_s}\right) i_g \\ &= \frac{R_s}{R_s + \omega_t L_s} \frac{\omega_t}{j\omega} (1 + jQ) i_g \end{aligned} \quad (3.8)$$

At the impedance matching status, the small signal noise analysis shows the channel noise output $i_{o,d}$ is half the i_d , while $i_{o,Rs}$ is proportional to $(\omega_t/j\omega) \cdot I_{Rs}$, which amplifies the I_{Rs} since $\omega_t/j\omega$ is usually at least above 3. On the other hand, the gate output noise is amplified by the factor of $(1 + jQ) \cdot \omega_t/j\omega$. For this reason, the gate noise can become significant, possibly even more dominant than channel noise depending on the Q and the operating frequency. According to this analysis, the common-source amplifier's noise figure is defined as Equation 3.9 [31].

$$F = \frac{\overline{i_{n,out}^2}}{\overline{i_{Rs}^2}} = 1 + \frac{\gamma}{\alpha} \frac{1}{Q} \left(\frac{\omega}{\omega_t} \right) \left[1 + \frac{\delta \alpha^2}{5\gamma} (1 + Q^2) + 2|c| \sqrt{\frac{\gamma \alpha^2}{5\gamma}} \right] \quad (3.9)$$

where the first and the second term represents the channel noise and gate noise, respectively, and the third term shows their correlated noise. The minimum noise level is found when differentiating the NF with respect to Q , which provides the optimal Q value that the channel noise and the gate noise balance. The channel noise is inversely proportional to Q while the gate noise is proportional to Q . Therefore, finding the optimal Q is key to the noise optimization. In this consideration, the mathematically optimal Q is defined as Equation 3.10 [31].

$$Q_{opt} = \sqrt{1 + 2|c| \sqrt{\frac{5\gamma}{\delta \alpha^2}} + \frac{5\gamma}{\delta \alpha^2}} \quad (3.10)$$

where c is the correlation coefficient which is normally a purely imaginary number, γ is a bias dependent empirical factor and is approximately 2/3 for MOSFET devices operating in saturation region. δ is another bias dependent empirical factor and α is the intrinsic gain $g_m r_0$. Although this analysis becomes a strong guidance to get minimal NF, it is impossible to count every single factor 100% accurately. It is more objective to find the optimal Q to find the minimum NF, by sweeping device width, bias, and the fabrication/bias dependent parameters γ , δ , c . Since ω_t is inversely proportional to the square of device length, setting the device length to be $L_{min} = 180\text{nm}$ to maximize ω_t is a good starting point. Then device width and bias point V_{OV} is swept to measure NF. ω_t is W/L dependent and Q is dependent on bias c , γ , δ which are bias-dependent, and α which is device width, length, and

bias-dependent.

3.4 Nonlinearity Issues

The real RF environment is harsh, noisy and, filled with various electromagnetic sources that interrupt proper communication of devices. Proximate frequency signals to the target signal can easily interfere with the fundamental frequency by creating nonlinearity and noise issues even with efforts to filter them out. For example, having an unwanted signal source of $f = 2.35\text{GHz}$ for the device with a target frequency $f_0 = 2.4\text{GHz}$ can be very difficult to filter out. It negatively interacts with the target signal so that they are unwillingly processed together within the system, causing errors in result. In addition to it, harmonics of the input signal of the original signal of interest are potential causes of misled sensing through intermodulation distortion. Therefore, prevention of spurious signals from these sources is one of the main challenges to build a robust system for an LNA and a mixer. For example, an input signal of the fundamental frequency $f = 2.4\text{GHz}$ that accompanies its n th harmonics such as 4.8GHz , 7.2GHz , 9.6GHz all interact together with transistors undesirably due to the nonlinear characteristics of transistor devices.

Ideally, analog circuit designers consider just the first-order transconductance in modeling process (as in assuming $i_{DS} = I_{dc} + g_m v_{gs}$). While this estimation works adequately in some cases, it is not always the case since the second or third-order transconductance terms may not be negligible for some applications, and especially so in mixer circuits where multiple fundamental frequency/harmonic terms are dealt

with. In this sensor, the Gilbert cell mixers are followed by the LNAs. This means high nonlinearity from the LNAs cascades to the GCMs. Hence, it is critical to suppress nonlinearity from the LNAs. To begin, a transistors' transconductance has to be defined using the Taylor's expansion (Equation 3.11).

$$i_{DS} = I_{dc} + g_m v_{gs} + \frac{g_{m2}}{2!} v_{gs}^2 + \frac{g_{m3}}{3!} v_{gs}^3 + \dots \quad (3.11)$$

where $v_{gs} = A \cos \omega_1 t + B \cos \omega_2 t$. The square term v_{gs}^2 becomes Equation 3.12.

$$\begin{aligned} & A^2 \cos^2(\omega_1 t) + 2AB \cos(\omega_1 t) \cos(\omega_2 t) + B^2 \cos^2(\omega_2 t) \\ &= A^2 \frac{1 + \cos 2\omega_1 t}{2} + AB \cos((\omega_1 + \omega_2)t) + AB \cos((\omega_1 - \omega_2)t) + B^2 \frac{1 + \cos 2\omega_2 t}{2} \end{aligned} \quad (3.12)$$

and similarly, the cubic term v_{gs}^3 becomes Equation 3.13.

$$\begin{aligned} &= \left(\frac{3A^3}{4} + \frac{3AB^2}{2}\right) \cos(\omega_1 t) + \left(\frac{3A^2B}{2} + \frac{3B^3}{4}\right) \cos(\omega_2 t) + \frac{A^3}{4} \cos(3\omega_1 t) + \frac{B^3}{4} \cos(3\omega_2 t) \\ &+ \frac{3A^2B}{4} \cos((2\omega_1 + \omega_2)t) + \frac{3AB^2}{4} \cos((\omega_1 + 2\omega_2)t) \\ &+ \frac{3A^2B}{4} \cos((2\omega_1 - \omega_2)t) + \frac{3AB^2}{4} \cos((2\omega_2 - \omega_1)t) \end{aligned} \quad (3.13)$$

As seen above, there are various spurious terms such as $n\omega_1$, $n\omega_2$, and $n\omega_1 \pm n\omega_2$ which are wide variations of the fundamental frequency ω_1 . These represent nonlinear elements generated within transistors. Particularly, the third-order intermodulation term (red line in Fig 3.3) magnitude grows three times faster with respect to the increase of the original signal (black line in Fig. 3.3), and the third-order terms

can surpass the original term's power. The point where the original signal and the third-order intermodulation magnitudes intersect (Fig 3.3). This is called the third-order intersect point (IP3) and the input power at the IP3 is called input-referred third-order intersect point (IIP3). Fig. 3.3 and Fig. 3.4 depicts their relationship and how they stand in transistor devices. Therefore, the design goal is to minimize the inevitable g_{m2} and g_{m3} to restrict critical spurious signals.

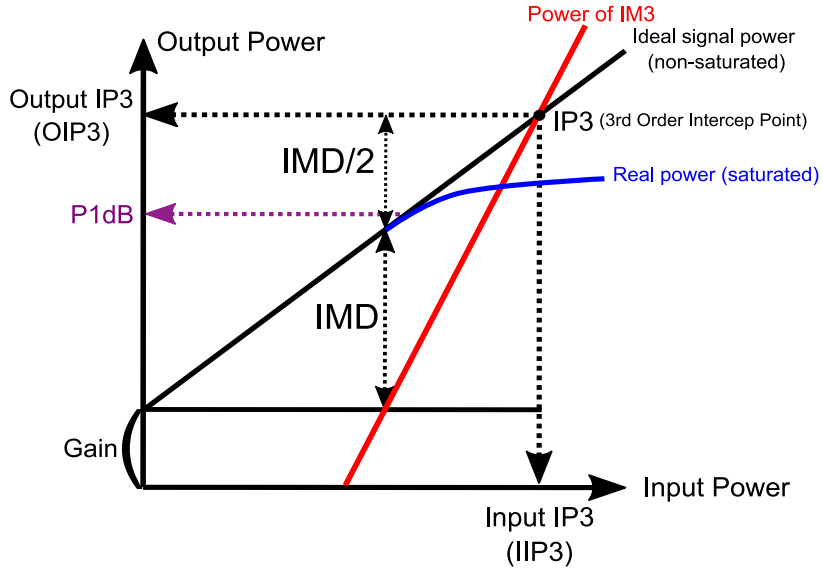


Figure 3.3: Diagram showing the IMD3 (the red line) to the RF input signal (the black line), where the intersect point indicates the IP3 [46].

3.5 Design Steps for Common-Source LNAs

The CS topology that features low-noise, fast speed, and moderate gain suit the requirements for the AoA sensing operating at $f_c = 2.4\text{GHz}$ and demanding low-noise and great linearity. Systematic optimization techniques were developed focusing on input-referred third-order input intercept point (IIP3) and noise figure

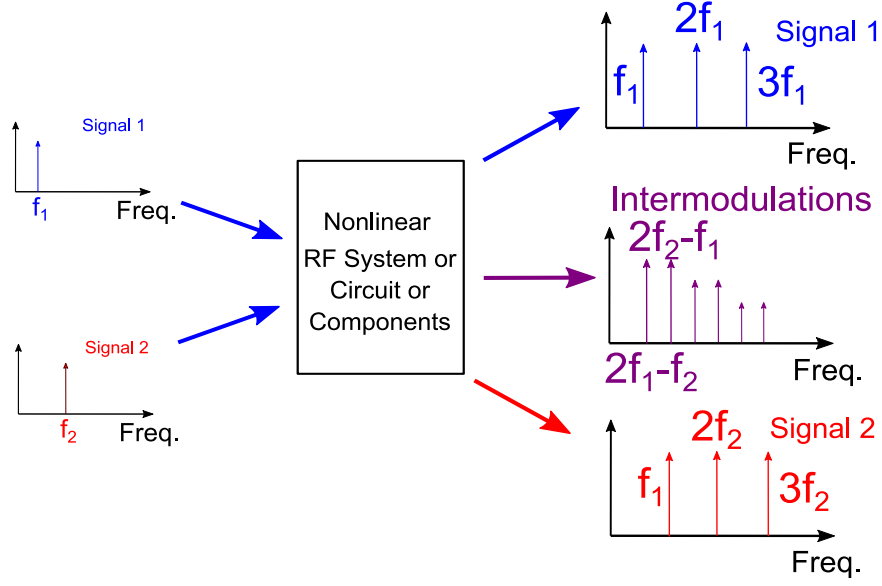


Figure 3.4: An illustration of harmonic signals (red and blue) and their intermodulation (purple) in nonlinear transistor devices. In our application, such intermodulation has to be suppressed[46].

(NF). Fig. 3.9 shows the circuit schematic of the common-source LNA ($M1$) and the g_{m3} suppression technique accompanied by the auxiliary transistors $M2$ and $M3$. It has inductors at the gate and source nodes L_G and L_D for input impedance matching and noise optimization. The inductor at the drain L_D forms an LC tank with parasitic capacitance C_D seen at the drain node for output resonance at $f_c=2.4\text{GHz}$. To begin the design process, the circuit parameters for the 180nm CMOS model must be defined. C_{ox} , the oxide capacitance is Equation 3.14.

$$c'_{ox} = \frac{\epsilon_{sio2} \cdot \epsilon_0}{t_{ox}} = \frac{3.45 \cdot 10^{-11}}{4 \cdot 10^{-9}} = 8.63 \cdot 10^{-3} \left(\frac{F}{m^2} \right) = 8.63 \cdot 10^{-15} \left(\frac{F}{\mu m^2} \right) \quad (3.14)$$

The c'_{gs} is approximately 2/3 of c'_{ox} for a transistor in saturation mode (Equa-

tion 3.15).

$$c'_{gs} = \frac{2}{3}c'_{ox} \approx 5.7 \frac{fF}{\mu m^2} \quad (3.15)$$

Kappa for NMOS transistors with the electron mobility $\mu_n=405.36(cm^2/V \cdot s)$ in 180nm CMOS technology platform is Equation 3.16.

$$\kappa_n = \mu_n \cdot \frac{c'_{ox}}{2} = 405.36 \cdot \frac{cm^2}{V \cdot s} \cdot \frac{0.421\mu A \cdot s}{V \cdot cm^2} = 170.65 \frac{\mu A}{V^2} \quad (3.16)$$

The goal is to get a maximum g_m for a given bias current I_D . It is a rule of thumb to set $v_{D,sat} = V_{GS} - V_{TH} \geq 200mV$ for devices' region of operation in saturation mode, in strong channel inversion, or weak channel inversion. Since low linearity can cause severe third-order intermodulation distortion (IMD3) and heavily distort the signal, channel inversion intensity must be determined in consideration of linearity. A device in weak inversion worsens the IMD3, hence the device is put in strong inversion by setting $v_{D,Sat} \geq 200mV$. Given this condition, the transconductance is aimed at $g_m = 20mA/V$ for $v_{D,Sat} = 200mV$. For this case, I_D is set at $g_m \cdot v_{D,sat} = 5mA$. The next step is to determine the size W/L of the device. Since

$$g_m = 2\kappa_n \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})$$

which can be rearranged with respect to W/L (Equation 3.17).

$$\frac{W}{L} = \frac{g_m}{2\kappa_n \cdot (V_{GS} - V_{TH})} = 20 \frac{mA}{V} \cdot \frac{1}{2 \cdot 170.65 \frac{\mu A}{V^2} \cdot 200(mV)} = 293 \quad (3.17)$$

With W/L determined, c_{gs} is also determined (Equation 3.18).

$$c_{gs} = W \cdot L \cdot c'_{gs} = 293 \cdot (0.18) \cdot (0.18) \cdot (\mu m^2) \cdot 5.7 \frac{fF}{\mu m^2} \approx 54 fF \quad (3.18)$$

c_{gd} and the overlap capacitance $c_{gs,ov}$ and $c_{gd,ov}$ should also be added which are relatively negligible in scale compared to c_{gs} and c_{gd} . It is difficult to estimate c_{gd} , $c_{gd,ov}$, $c_{gs,ov}$ since overlap length x_d isn't given. However it is considered approximately about 1/3 the scale of c_{gs} generally. With that, the sum of c_{gd} , $c_{gd,ov}$, $c_{gs,ov}$ capacitance is evaluated to be $80 fF$. This evaluation result provides the total gate capacitance to be $c_{gate}=134 fF$. Next is the input impedance Z_{in} . A common-source amplifier's input impedance network is equivalent to the model presented in Fig. 3.5 (Equation 3.19).

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{m1}}{C_{gate}}L_s \quad (3.19)$$

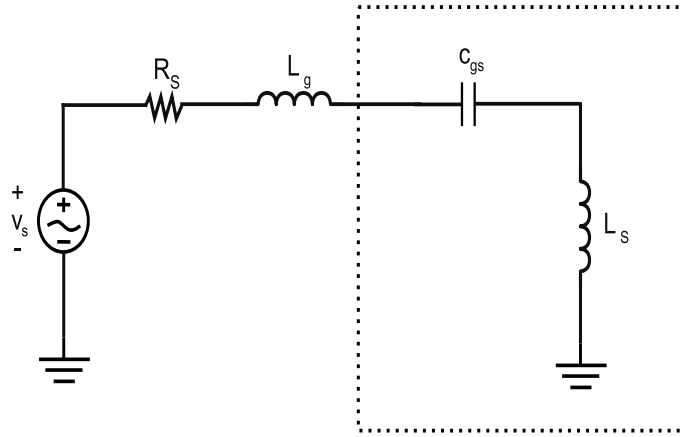


Figure 3.5: Equivalent input impedance network for the LNA.

The first and the second signal terms in (10) have to cancel each other out at the operating frequency f_c and so that the real term $(g_m/c_{gs})L$ is matched to the $50\ \Omega$ antenna. Therefore the reactive impedance becomes zero by selecting the parameters that satisfy $s(L_g + L_s) + 1/(sC_{gs}) = 0$. By rearranging the equation with respect to s , it gives

$$s = \frac{1}{\sqrt{(L_g + L_s) \cdot c_{gate}}}$$

Given c_{gate} value and the real impedance $(g_{m1}/c_{gate})L_s = 50\Omega$, L_s is determined.

$$L_s = 50\Omega \cdot \frac{c_{gs}}{g_{m1}} = 50\Omega \cdot \frac{134fF}{20mA/V} = 0.34nH$$

This is very small inductance. Since $s = \frac{1}{\sqrt{(L_g + L_s) \cdot c_{gate}}}$, $L_g + L_s$ can be found at

$$L_g + L_s \approx L_g = \frac{1}{s^2 c_{gate}} = \frac{1}{(2\pi \cdot 2.4GHz)^2 \cdot 134fF} = 32.8nH$$

An LC tank resonance at the operating frequency at the output stage of the CS amplifier also has to be achieved. The corresponding L,C parameters can be selectively chosen according to $f = 1/(2\pi\sqrt{LC})$. The output inductor $L_d=0.9nH$ was correspondingly decided by the drain parasitic capacitance $C_d = 4.6pF$ which was the evaluated value from simulation. Finally, a buffer stage is essential for low output impedance. Since LNA will be used in multiple stages, the output impedance needs to be 50Ω for source follower $M4$. For this, g_{m4} has to be

$$g_{m4} = \frac{W \cdot 2\kappa_n (V_{GS} - V_{TH})}{L} = \frac{W \cdot 2 \cdot 170.65 \frac{\mu A}{V^2} \cdot 200mV}{L} = \frac{20mA}{V}$$

which leads to the sizing of $M4$ to be

$$\frac{W}{L} = 292$$

Device width, length sizing and gate, source and drain inductance are deter-

mined from these initial parametric decision steps. This is foundational for further optimization and an iterative design process which are introduced in section 3.3.

Next is noise analysis. It embodies various correlation factors including device width, length, bias point, gate resistance, fabrication-dependent constants, operation frequency, and more. To start, NF_{min} for the common-source LNA has to be defined. The noise figure and input referred third-order intercept point can be approximated and defined in Equation 3.20, and Equation 3.21[45], respectively.

$$NF_{min} = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} g_{m1} R_s \frac{\omega_0^2}{\omega_t^2} \quad (3.20)$$

$$IIP3 = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|} = \sqrt{\frac{2}{3} \frac{g_m}{R_s} \frac{1 + g_m R_s^2}{K}} \quad (3.21)$$

where gate-induced noise, drain-noise, and MOSFET source resistance noise are accounted. $K = \mu C_{ox} W/L$, and $Q = 1/R_s C_{gs}$. γ is a bias dependent value and typically 1 in saturation region for an 180nm channel length device. α is intrinsic gain g_{m0} . Reduction of gate resistance R_g , securing balance between the transconductance, device width and ω_t are considered to maintain a minimum noise figure according to (11). Although (11) shows that the higher the Q is, the lower the channel is, various studies[3][49] reported that there is an optimal Q for each LNA application deriving from the balance between the gate noise and the channel noise. Hence, it is most realistic to find the optimal Q empirically by varying V_{GS} and device width which will be discussed in 3.6.

3.6 Optimization Methodology based on the g_m/I_D Algorithm and g_{m3} Cancellation

The width optimization process of W_{M1} is achieved by adjusting V_{OV} . For this, the g_m/I_D algorithm suggests a quantitative circuit design guidance for submicron MOSFET devices. Three reference graphs must be acquired for the algorithm in advance: g_m/I_D vs. V_{OV} (Fig. 3.6) and f_t vs. V_{OV} (Fig. 3.6) and I_D/W vs. g_m/I_D (Fig. 3.7). The simulation is run at $V_{DS} = 0.85V$ and $1.8V$, $L=180$ nm to acquire a reference for 180 nm transistor characteristics. g_m/I_D describes the transconductance efficiency, f_t represents a unity current gain frequency that implies the maximum speed of MOSFETs. I_D/W stands for the current density for the unit width serving as a reference to determine device width which is dependent on the device's DC current.

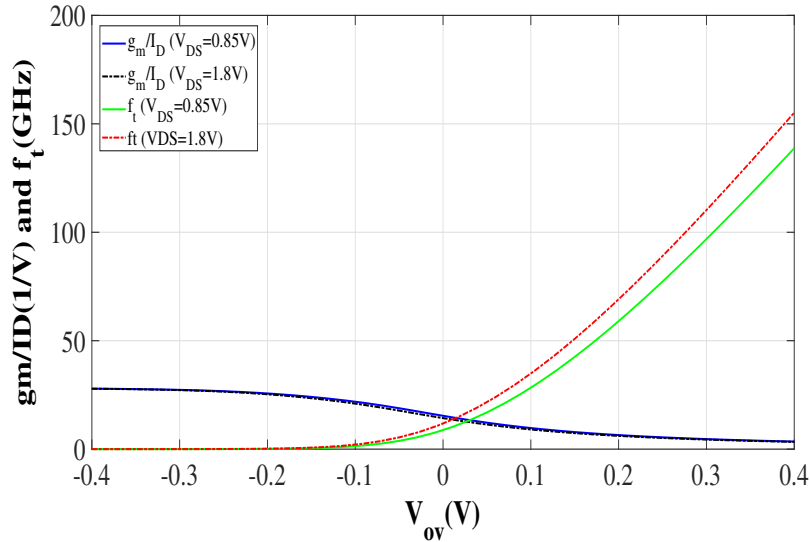


Figure 3.6: g_m/I_D , f_t vs. V_{OV} reference graphs for $V_{DS} = 0.85V$ and $1.8V$ at $L_{min} = 0.18 \mu m$.

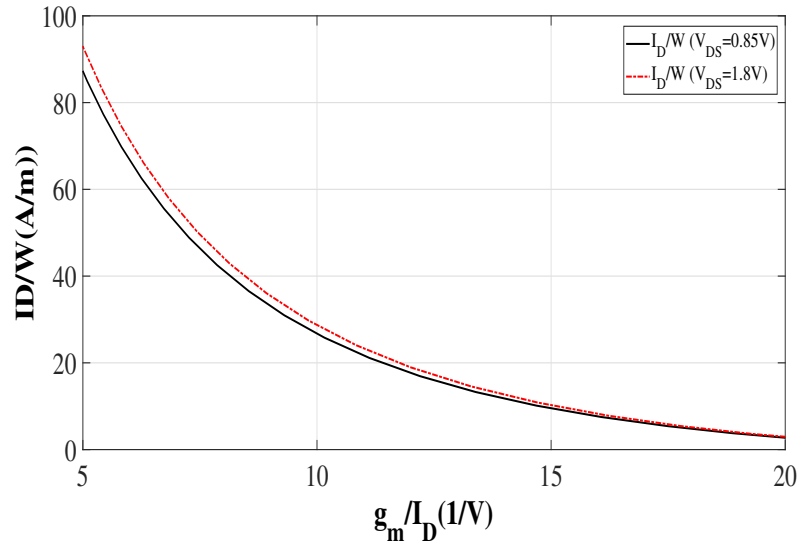


Figure 3.7: I_D/W vs. g_m/I_D reference graph for $V_{DS} = 0.85V$ and $1.8V$ at $L_{min} = 0.18 \mu m$.

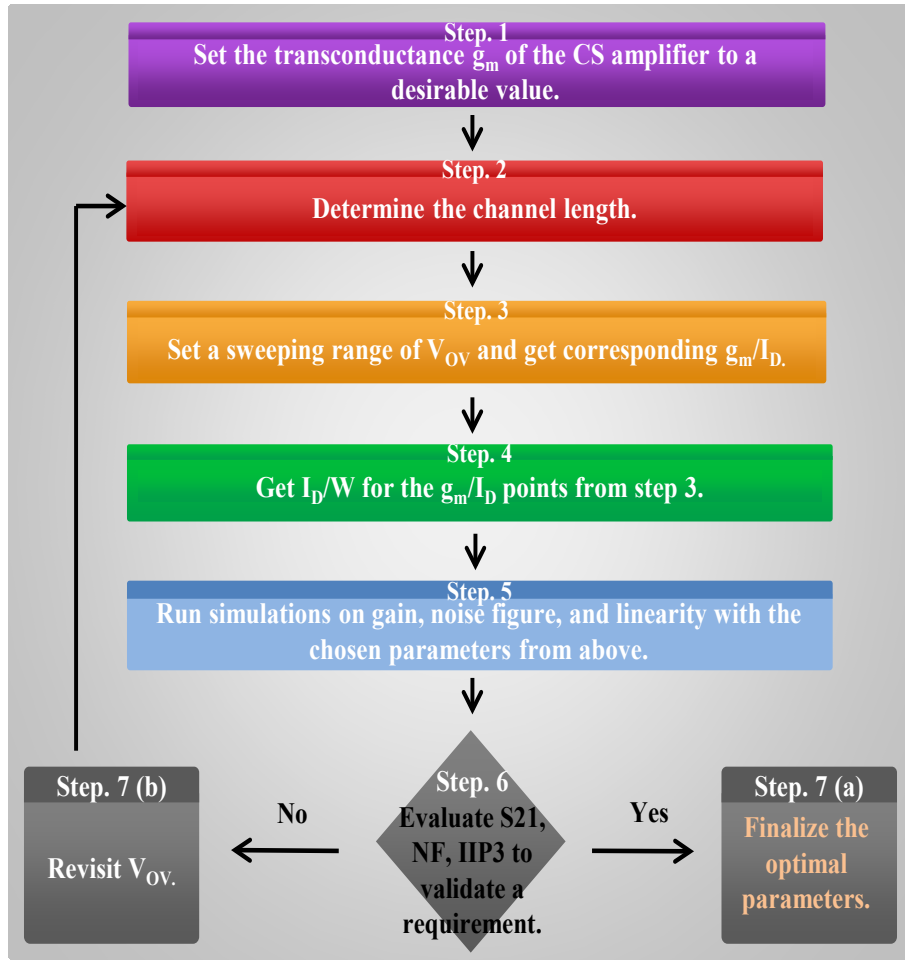


Figure 3.8: The parametric optimization flow chart for LNA design.

Fig. 3.8 shows the design optimization process developed based on g_m/I_D algorithm. A moderate transconductance is desired (20mA/V) to secure power gain S_{21} above 15 dB (Step. 1). The next step is to confirm the channel length of the MOSFET $M1$. A unity gain frequency $f_t = g_m/c_{gs}$, is inversely proportional to L^2 and accordingly high f_t increases intrinsic gain and lessens noise figure as described in (11). To get better performance in noise and speed, the channel length is set to a minimum length of $L = 180$ nm (Step. 2). Then, V_{OV} is adjusted to find an appropriate g_m/I_D for the design (Step. 3, 4). From Fig. 3.6 and Fig. 3.7, reference graphs are generated which demonstrate that as V_{OV} increases, g_m/I_D decreases while f_t increases. Therefore, when V_{OV} is high (strong inversion), g_m/I_D is low and f_t is high, while in weak inversion where V_{OV} is low, g_m/I_D is high and f_t is low. Hence an optimal range for the V_{OV} can be determined, and W_{M1} is computed for this V_{OV} (step. 5). Next, the gain, noise, linearity, and power are evaluated. (Step. 6). Finally, the parameters setting (Step.7 (a)) or V_{OV} can be revisited (Step.7 (b)). Table 3.2 becomes an index guide for finalizing the optimal bias point V_{OV} and the corresponding widths, W_{M1} at the V_{OV} point. Based on parametric analysis, the optimal V_{OV} is determined.

Once the optimal V_o is determined, optimal performance on S_{21} , NF, and IIP3, the CS amplifier can extend its linearity performance further by applying the g_{m3} enhancement technique since the third-order intercept point IIP3 in (12) can be maximized when the ratio of g_{m1} to g_{m3} is high[42][57]. Fig. 3.9 shows how the g_{m3} enhancement technique is applied. $M1$ of the CS amplifier is connected in parallel with the complementary $M2$ and $M3$ to suppress g_{m3} of $M1$ effectively in

the appropriate V_{OV} bias domain when $M2$ and $M3$ are set to optimal W/L and body-bias V_{BS} . Thus $M2$ and $M3$ are set to generate equal levels of g_{m3} to that of $M1$ but in the opposite direction. This effectively cancels out the third-order transconductance of $M1$ without affecting S_{21} and NF, since $M2$ and $M3$ have significantly higher threshold voltages due to higher V_{BS} relative to $M1$ which leads to low first-order g_m .

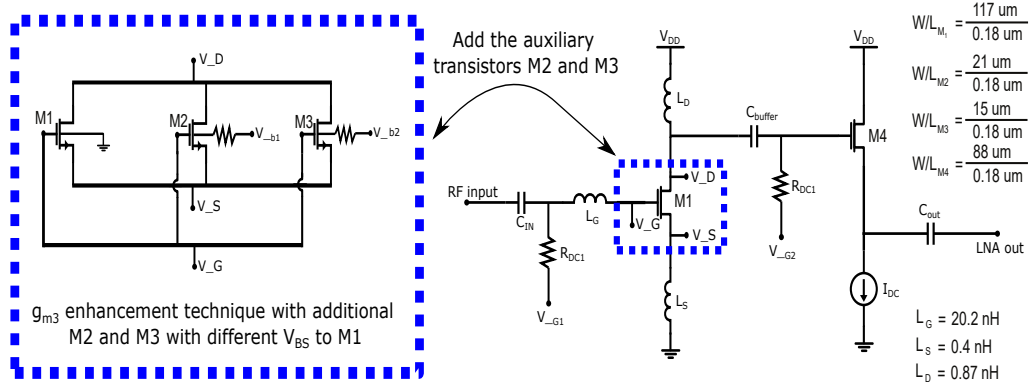


Figure 3.9: The schematic view of the designed CS LNA with the g_{m3} suppression technique using the complementary MOSFETs $M2$, $M3$.

3.7 Results and Analysis

To define the optimal bias point V_{OV} where noise, linearity, and power gain level balance out, S_{21} (Fig. 3.10), NF (Fig. 3.11), IIP3 (Fig. 3.12) vs V_{OV} is evaluated for V_{OV} from 0 to 0.25 V in 50 mV steps. This V_{OV} range covers weak channel inversion ($V_{OV} = 0 \text{ V}$, 0.05 V), moderate channel inversion ($V_{OV} = 0.1 \text{ V}$, 0.15 V) and strong channel inversion ($V_{OV} = 0.2 \text{ V}$, 0.25 V) ranges. The device width for each V_{OV} is computed from the I_D/W in Fig. 3.7 and as shown in Table 3.2. S_{21} in Fig. 3.10 shows higher S_{21} as the channel inversion gets stronger but

saturates above $V_{OV} = 0.15$ V at $S_{21} = 15$ dB. It reveals just a 3 dB higher level than in the worst case scenario of $S_{21} = 12$ dB at $V_{OV} = 0$ V. NF shows very weak dependence on V_{OV} as the NF at f_0 stays at 2.5 dB regardless of V_{OV} . (Fig. 3.11).

In comparison, IIP3 shows large variation with V_{OV} (Fig. 3.12). IIP3 is relatively high in the weak channel inversion domain, showing IIP3 = -2.46 dBm and -4.81 dBm at $V_{OV} = 0$ V and 0.05 V, respectively. In the moderate and strong channel inversion domain, IIP3 ranges from -6 to -7 dBm which is 2 ~ 5 dBm lower than in the weak channel inversion domain. Thus, the weak channel inversion has a better response on IIP3 while the strong channel inversion is more advantageous in the power gain S_{21} . This analysis provides important guidelines to determine the optimal bias for this circuit. The strong channel inversion with the bias $V_{OV} = 0.2$ V is a great choice since IIP3 has more room for enhancement by the g_{m3} suppression technique through the complementary MOSFETs $M2$, $M3$ as introduced in the section 3.1. Fig. 3.13 shows the g_{m3} profile of $M1$, $M2$, $M3$ w.r.t V_{OV} . The width and the body bias of $M2$ and $M3$ are adjusted to secure low g_{m3} around $V_{OV} = 200$ mV. Given the bias point $V_{OV} = 0.2$ V where the device width $W_{M1} = 48$ μm (Table 3.2), the device width of $M2$ and $M3$ are determined to $W_{M2} = 21$ μm , $W_{M3} = 15$ μm (Fig. 3.13), where g_{m3} is shown to be low. The IIP3 analysis in Fig. 3.12 demonstrates IIP3 improvement by 10 dBm with the g_{m3} enhancement technique, maximizing optimization of the circuit. All results are post-layout simulation results from the layout Fig. 3.14. Table 3.3 shows that this LNA demonstrates excellent IIP3 and S_{21} with moderate NF as compared to previous works[24][4][16][2][8][32].

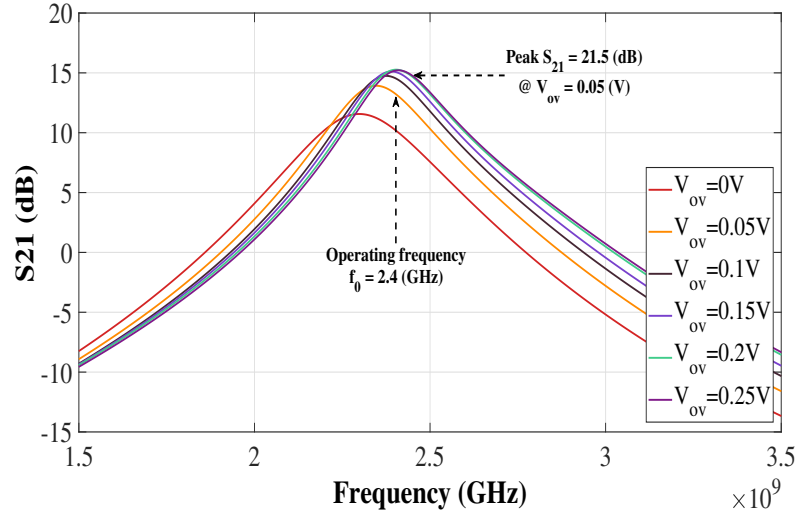


Figure 3.10: S_{21} vs. V_{OV} of the LNA. The highest gain is shown at $V_{OV} = 0.05$ V

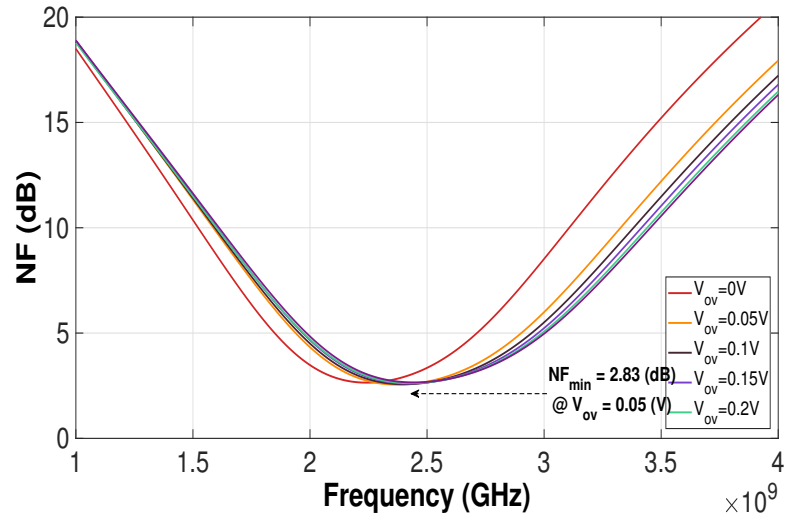


Figure 3.11: NF vs. V_{OV} of the LNA. The lowest noise figure is shown at $V_{OV} = 0.05$ V

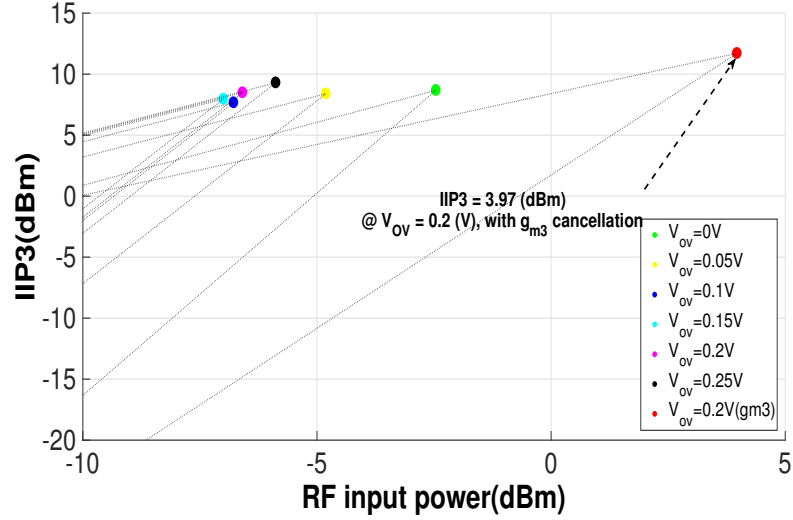


Figure 3.12: IIP3 vs. V_{OV} of the LNA showing the highest linearity of IIP3 = 3.97dBm at $V_{OV} = 0.2$ V.

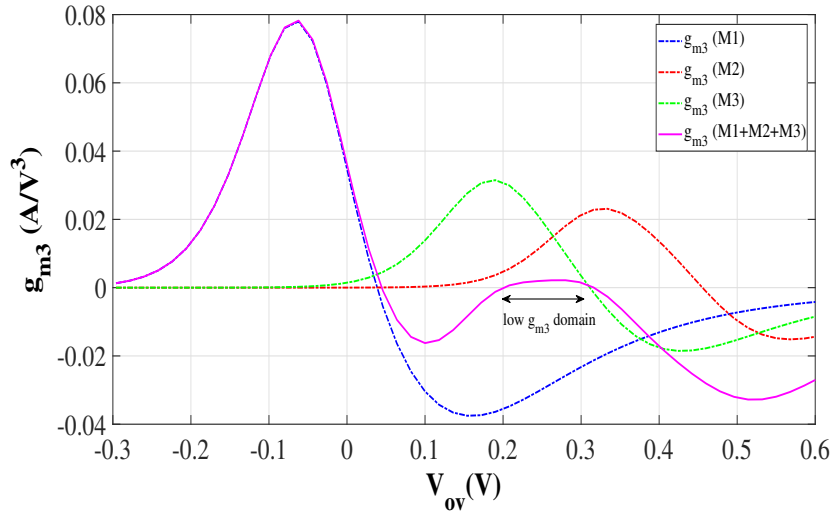


Figure 3.13: The LNA g_{m3} parameter vs. V_{OV} , before applying g_{m3} suppression technique(blue). The optimal domain with the gm3 cancellation technique with low g_{m3} is shown between 0.2 and 0.3 V (V_{OV}) in purple.

V_{OV} (V)	g_m/I_D (1/V)	f_t (GHz)	S_{21} (dB)	IIP3 (dBm)	NF (dB)	W (μ m)	P_{DC} (mW)
0	14.6	2.8	11.6	-2.46	2.9	117	2.43
0.05	11.4	11	13.9	-4.81	2.58	81	3.15
0.1	9.1	15.8	14.8	-6.78	2.55	63	3.96
0.15	7.3	20	15.2	-7	2.57	54	4.95
0.2	6.1	24.1	15.3	-6.59	2.61	48	5.9

Table 3.2: The LNA parameters according to V_{OV} (before applying g_{m3} suppression technique).

References	S_{21} (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	f_c (GHz)	CMOS tech (nm)
This work	15.3	2.97	5.84	5.9	2.4	180
[24]	3	12.81	10.5	12.6	2.1	130
[4]	11.6	4.2	1.15	11.6	8	180
[16]	27.5	3.88	-11	11.25	24	130
[2]	31	2.6	-2.5	9.75	2.4	180
[32]	13.7	2.3	N/A	18	6.5	180
[8]	9.3	6.5	-6.7	9	6.5	180

Table 3.3: Comparison of the low noise amplifier with previous works.

3.8 Summary

In this chapter, the combined optimization methodology was developed for the low noise amplifier. The design applied g_m/I_D , f_t/I_D , and I_D/W reference figures to determine an optimal bias and width of the device. In addition, the g_{m3} suppression technique was utilized to enhance linearity. Both optimization techniques proved robust and organized design platforms by showing a significant improvement in terms of linearity and noise figures. The LNA showed excellent linearity of IIP3 = 5.84 dBm, great noise level of NF = 2.97 dB, and sufficient gain of S_{21} = 15.3 dB, which are satisfying specification for angle-of-arrival sensing.

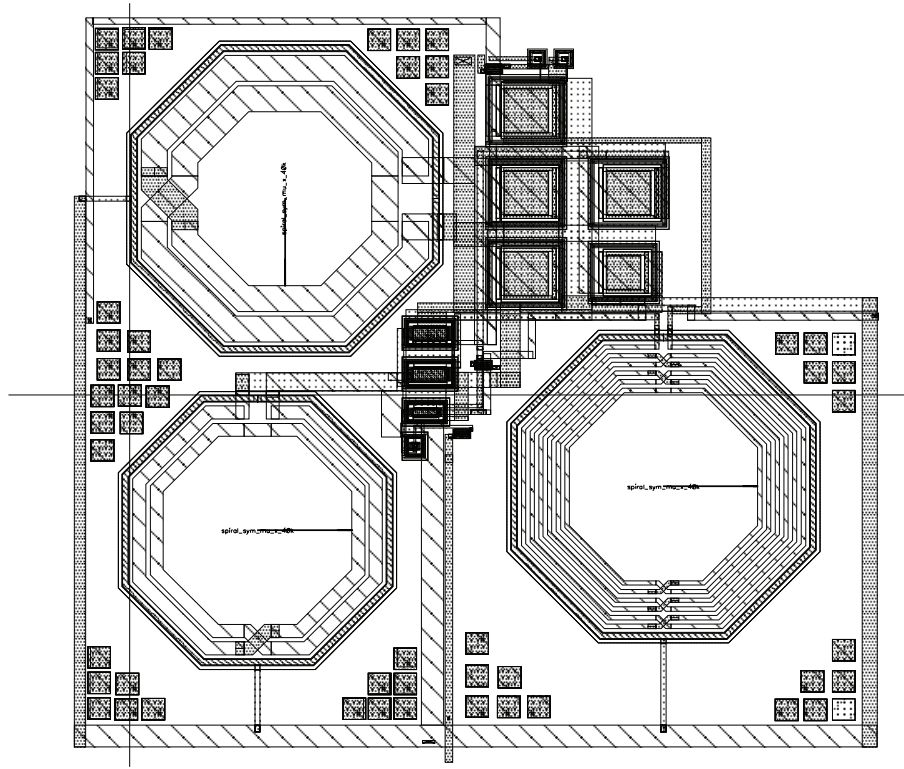


Figure 3.14: The layout design of the LNA including the three spiral inductors.

Chapter 4: Development of a Local Oscillator Balanced-to-Unbalanced (BALUN) Module for the AoA Sensor

4.1 Introduction

In the analog electronic signal approach, signals can be single-ended and/or differential-ended mode. Differential-ended signals are beneficial in terms of suppressing common-mode noise sources by cancelling out the noise while retaining the signal of interest in the opposite polarity. Differential-mode is particularly important in congested and harsh RF environments where sensing remote and weak RF signals of interest requires suppression of noise and an enhanced SNR. In order to develop low-noise signal sensing, it is necessary to develop a single input to differential output signal circuit in the form of a balanced-to-unbalanced (BALUN) module that can be designed to generate clean low noise LO+ and LO- signals for the multiplier. So the BALUN module is required for the LO input of the Gilbert cell mixer (GCM) which has to be a balanced input of LO+ and LO-. The BALUN module converts, and amplifies the LO signal received at $ANT - LO$ and feeds the differential input to the GCM. The design goal of the BALUN is to provide stable differential LO input signals, ideally with equal magnitude in the exact opposite polarity on the LO+

and LO- with low noise. There are three different approaches to accomplish such a BALUN module. Candidates for the BALUN will first be introduced and details on the chosen BALUN model will then be analyzed and evaluated. The content discussed in this chapter was published in [15].

4.2 BALUN Module Options

One option of BALUN implementation is by interleaved structured metal traces, as shown in Fig. 4.1[10][37]. An interleaved structure-based BALUN is theoretically equivalent to a transformer circuit with a turn ratio of 1:1, not $N:1$ as in actual transformers. Although it is a very popular option, the CMOS 180nm PDK used for this research work does not support fabrication of interleaving structures of spiral inductors but only allows one spiral inductor in a given area. The only available inductors are spiral inductors formed by the two layers which are: the top layer (N th) and $(N - 1)$ th metal layers. Therefore, the implementation of an interleaved BALUN can only be achieved by an external device which goes against the goal of the RFIC sensor design to include the whole system on the chip.

A second option is using delay-line based RC circuits[23](Fig. 4.2). It can form a system that delays half the period of a signal and generate a 180 degrees converted signal by applying a corresponding RC parameter that matches to a half period of the signal time. Utilizing an original input signal and the generated inverted signal forms a differential signal which in principle, is effectively a single-ended to differential-ended conversion. While it can be an easy and intuitive implementation,

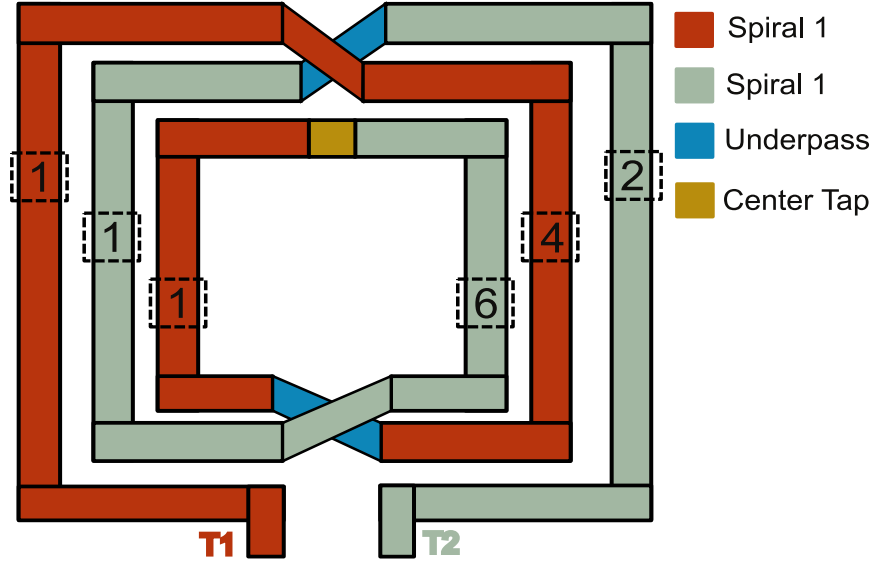


Figure 4.1: An example of a transformer-based inductor[10].

it has a critical drawback: an accuracy problem due to mistmatching magnitude and phase. Converting a single-ended into a differential signal with an exact 180 degrees difference that corresponds to the exact half period signal can be very difficult due to mismatching RC time constant. This discrepancy can trigger a critical phase error which fails the purpose of a BALUN. In addition, sensitivity due to processing and fabrication variation can add even more mismatching.

The third approach option which is developed in this work is combining a common-source and a common-gate amplifier, which has distinct advantages over the previous options. This approach is as simple as combining a non-inverted and an inverted signal from the common-gate and the common-source amplifier just as represented in Fig. 4.3[27]. It produces a lower phase error because the CS and the CG together provide a differential output signal by taking the same single-ended signal from the antenna as an input and generates an output in the same polarity

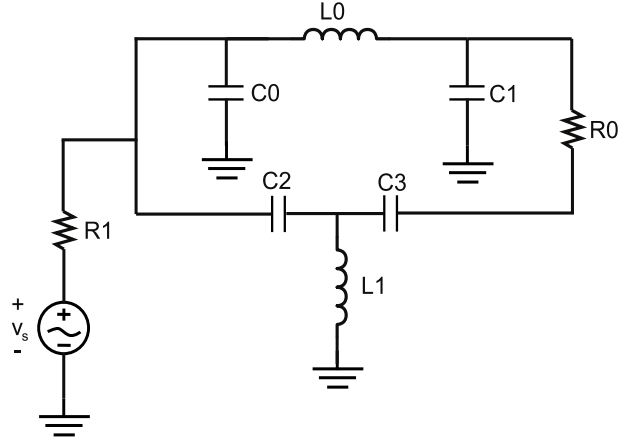


Figure 4.2: An example of a BALUN using RC delay circuits[23].

as the input signal for the CG amplifier and an inverse phase signal for the CS amplifier[58]. Although this approach easily generates a differential signal, it isn't a perfect way due to the drawback that a signal amplitude from the CS and the CG can be slightly different. This can be adjusted through fine tuning of the parameter of each CS and CG amplifier circuits and additionally executing symmetry circuit layout for better matching.

The other noticeable difference to a transformer BALUN (option one, Fig. 4.1) is that it does not just transform a signal to a differential signal in the same amplitude, i.e. unity gain, but it also amplifies the signal because this circuit is essentially equivalent to an amplifier stage. As there is no need to maintain a unity gain since the system indeed requires an amplified signal for a better LO's switching function, transforming a single to differential signal with amplification is beneficial as mentioned above. Therefore, the combinational CS and CG amplifiers approach was determined to be best for this application and developed in this work.

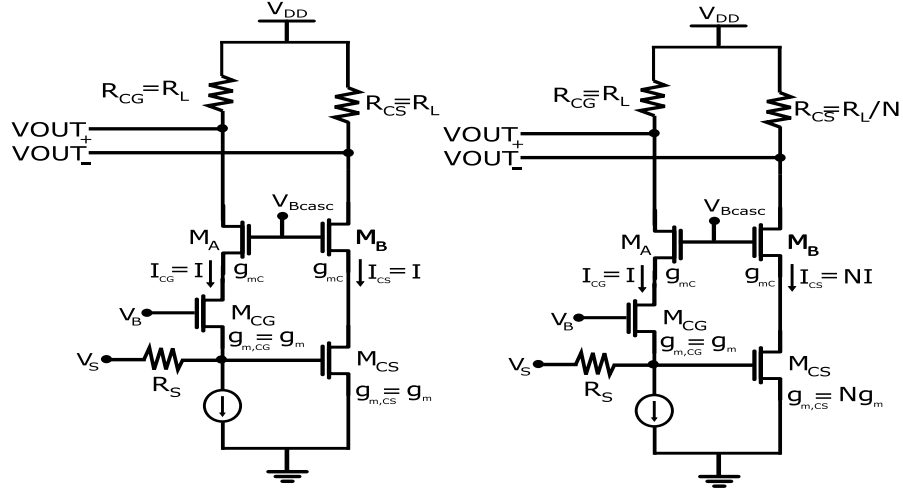


Figure 4.3: The CS-CG amplifier BALUN option[27].

4.3 BALUN Circuit Topologies

There are two BALUN topologies based on the combination of the CS and CG amplifiers. First is the single stage CS and the CG combination. The second is the combination of the cascode CS and CG. The first option consists of just two transistors while the second option consists of four transistors. This structural difference deviates the noise boundary since the second option inevitably always has higher noise-level potential with double the number of transistors. However, the cascoded stage option comes with higher gain and most importantly with lower reverse leakage. Low reverse leakage prevents noisy mixing that causes self-mixing, and eventually contributes to minimizing mismatches in the AoA, hence the cascode stage option is more advantageous. Although the relatively higher noise of the cascode stage itself is not beneficial, the system is not as vulnerable to the LO signal as it is toward the RF input. This is because the LO signal has to have much

higher SNR than the RF signal's that enables flexible switching of the mixer's LO transistors for appropriate zero-IF mixing. Therefore, it has a significantly lower impact on the LO relative to the RF signal and the use of the cascode LO BALUN can be justified.

4.4 The LO BALUN Design and Modeling

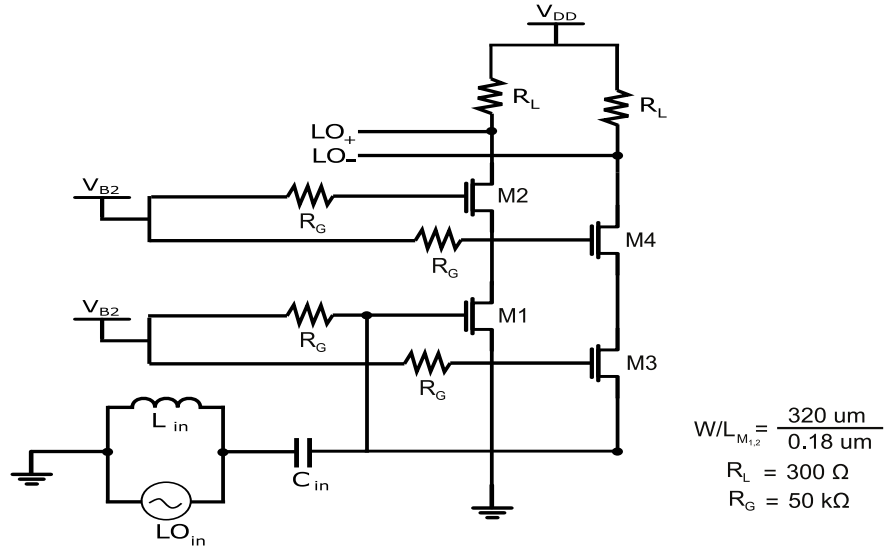


Figure 4.4: The schematic of the on-chip LO BALUN based on the cascode CG and CS amplifiers developed in this work.

There are three important design aspects to be considered for the BALUN operation. First is matching the output magnitude of the CS and CG amplifiers to guarantee the symmetrical LO+ and LO-. The mismatched magnitudes can be adjusted by the W/L ratio of transistors. If the CS stage needs more amplification due to a smaller amplitude compared to the CG, the W/L ratio of the CS stage can be increased for a larger g_m value and vice versa. Second is maintaining low noise levels to minimize negative influence on the $\Delta\phi$ detection. Although the LO

input is less sensitive to noise than that of the RF input in the mixer, low noise still leads to more accurate AoA sensing consequently. Third is the suppression of the LO reverse leakage. Reversely leaking in the LO adds jitter to the LO, and distorts mixing. Taking these three design focuses into consideration, an on-chip BALUN is implemented with an inductor connected to the source node of the CG which is parallel to the LO input port. This provides DC ground to the input of the CG amplifier which guarantees the same bias voltage V_{GS} for both the CS and CG amplifiers. In addition, no direct input and output feedback through the parasitic capacitance of C_{gd} , results in lower reverse leakage. Furthermore, loads are formed with resistive loads because these are superior to active loads in reducing flicker noise and increasing linearity. Fourth, a minimum phase error between the V_{out+} and V_{out-} is critical. Certain levels of phase error do not critically impact the result, however, when large, it may distract a stable switching operation of the LO transistors in the mixer. Therefore, it is important to evaluate the maximum error range to evaluate the performance of the Gilbert cell mixers.

Lastly, the output headroom has to be well established. Since the input power of the BALUN stage is relatively much stronger due to the significant amplification through the four consecutive LNA stages, it is important to secure large output headroom to process the signal without getting distorted. Choosing an appropriate load is one way to maximize the output swinging range. Not only does the output power saturation have to be handled properly, but also the input power capability needs serious attention to avoid saturation of the input signal. Appropriate gate biasing is required to cover the input swinging range while still maintaining stronger

inversion condition in the channel. Fig. 4.4 presents the schematic of the LO BALUN designed based on the consideration of all critical aspects discussed in this section.

4.5 Results and Analysis

The LO BALUN transforms the single-ended LO input into the differential-ended signal by providing a reasonable amplitude with low noise while avoiding signal attenuation. Fig. 4.5 shows the transient evaluation of the LO+ and LO-. LO+ from the CG amplifier and LO- from the CS amplifier in the opposite polarity shows greatly matching amplitudes with less than a 1% difference in magnitude. This result is ideal for the LO differential input of the GCM for clear switching operation for zero-IF mixing as the BALUN output swings with respect to the threshold voltage of the LO transistors in the mixer. Fig. 4.6 shows the NF versus frequency exhibiting an NF = 3.83 dB at $f_0 = 2.4$ GHz which is slightly higher than that of general single common-source LNAs or common-gate LNAs. The noise level in the LO has a relatively lower impact than that of the RF input since the LO amplitude at the GCM is much larger and is used for mixing without affecting the detection of $\Delta\phi$. The results demonstrate single-ended to differential ended output signal conversion to provide appropriate LO+ and LO- for the GCM.

The Fig. 4.7 shows the layout of the BALUN unit, with the chip area corresponding to $200\ \mu m \times 500\ \mu m$.

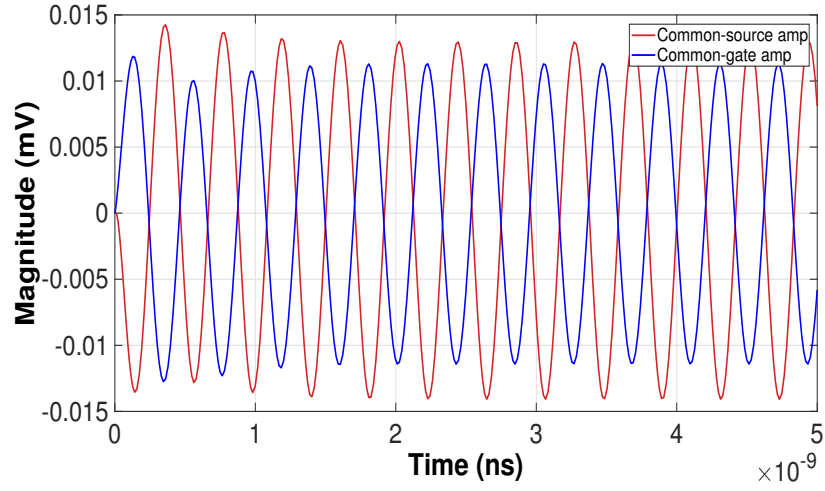


Figure 4.5: Transient simulation on the LO BALUN representing the matching amplitude of LO+(red) and LO-(blue).

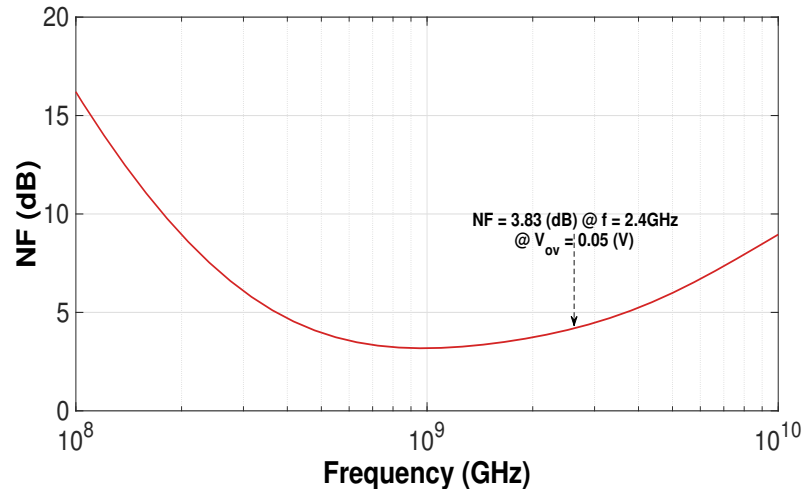


Figure 4.6: NF vs. frequency of the LO BALUN. For the targeted 2.4GHz operation, NF = 3.83 dB at $V_{OV} = 0.05$ V as shown in the figure.

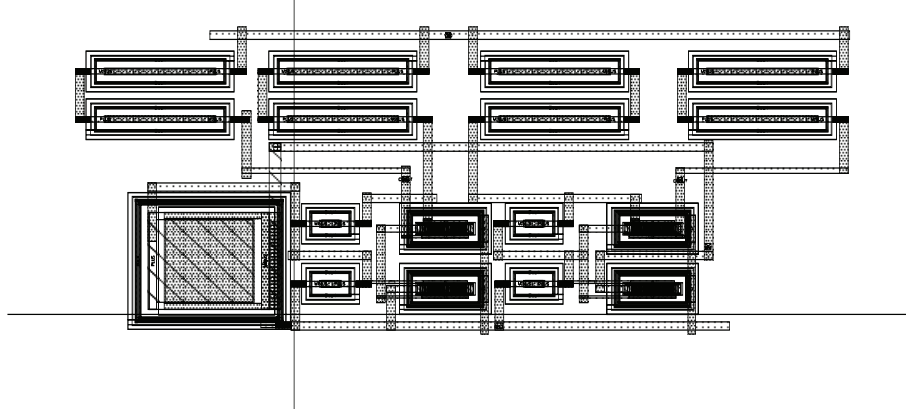


Figure 4.7: The LO BALUN layout. The large top four are resistor elements, the small four at the bottom are the cascode transistors and the large square on the bottom left is the capacitor.

4.6 Summary

Based on the key considerations described above The BALUN design and modeling was developed based on a combination of cascode common-source and common-gate amplifiers. The design resulted in a high performance BALUN with very low gain mismatching less than a 1% of error. NF was also shown to be low at $NF = 3.83\text{dB}$ at the operating frequency. Both results showed the ability to deliver the signal without any significant distortion the original signal, especially considering that LO BALUN comes after the four consecutive LNA stages where their output is a massively amplified signal. In conclusion, the result showed that the LO BALUN is well suited for the RF tracking sensor to be used in the differential LO input of the Gilbert cell mixer since it shows greatly matching magnitude in the opposite polarity to switch the LO stage on and off clearly enough.

Chapter 5: Optimization Methodology for Gilbert Cell Mixers

5.1 Introduction

In advanced wireless communication systems, it is essential to develop a stable, low noise mixing stage for the high frequency carrier signal to provide an efficient transfer of the voice, video, and/or media data signal of interest. A Gilbert cell mixer is one of the most commonly used active mixers. In this sensor application, a Gilbert cell mixer is the core module for phase detection that is utilized in the angle-of-arrival sensing. The AoA sensor takes the RF input on the two antennas $Ant1 - \theta$ and $Ant2 - \theta$ with a certain phase difference and feeds them into the Gilbert cell mixer's RF+ and RF- input, respectively, for zero-IF mixing of the RF input and LO input. The zero-IF outputs the phase differences of RF+ and RF- that contain the angle-of-arrival information. Although it is a simple principle of zero-IF mixing, a phase detection performance can vary widely depending on the completeness of the design. Poor optimization of the Gilbert cell mixer can easily lead to the failure of the AoA sensing. The mixer is particularly sensitive to linearity degradation, noise generation, and gain attenuation that become significant factors in limiting phase detection. Previous studies report various topologies for Gilbert cell mixers such as the g_{m3} cancellation technique[5][25], common-gate based designs[26], and

an inductor-less design[20] to enhance their performance in one way or the other.

The Gilbert cell mixer presented in this chapter concentrates on three main design elements for the AoA detection in this sensor: conversion gain, linearity, and noise. Linearity degradation can become a serious problem in a congested RF environment. Suppressing such nonlinearity to prevent intermodulation distortion, is a challenging task. Noise is critical on the Gilbert cell mixers as the switching operation at the local oscillator (LO) stage can produce severe flicker noise, in addition to the MOSFET channel noise. These noise sources must be suppressed accordingly. Noise level determines the minimum signal the system is capable of processing that in turn becomes an indicator of the minimum AoA sensing sensitivity. Finally, conversion gain is another crucial factor to be considered, as higher conversion gain is also related to higher AoA sensing accuracy. The conversion gain defines an analog-to-digital conversion error range that influences the AoA computational process of the microcontroller. Thus, achieving an optimal balance between conversion gain, linearity, and noise is the key to the successful design and implementation of a Gilbert cell mixer for the AoA application.

In this chapter, the fundamentals of Gilbert cell mixers are discussed and some of the modified Gilbert cell mixer existing topologies, are examined and evaluated. Following that, the design strategy of the Gilbert cell mixer for this RF sensor based on the novel combined optimization methodology, is presented. The proposed methodology combines four key design techniques which are the current bleeding technique, the inductive resonance technique, the g_m/I_D based width (W) optimization technique, and the flicker noise optimization technique to develop the

key parameters optimal for the AoA sensing application. The concurrent application of these four techniques can provide a universal optimization approach to different RFIC system applications to determine an optimal performance point for a Gilbert cell mixer. Current bleeding is an important step to reduce flicker noise and acquire better linearity in the mixer by directly supplying some portion of DC current to an RF transistor pair which results in the reduction of the DC current through the switching stage[36]. The second method is the inductive resonance which counteracts the parasitic capacitances that negatively impact the leakage current at the source node of the LO stage. Optimizing the inductive parameter choice can greatly reduce noise and improve linearity further[34][38]. The third optimization technique in this proposed methodology, is the g_m/I_D based width (W) optimization of the MOSFETs. The g_m/I_D based design approach provides guidance to reach the design goal by using lookup charts for the given CMOS technology, which in this case is 180nm. Lastly, the flicker noise optimization technique is discussed by focusing on the load resistance and current bleeding resistance ratio. This technique can dramatically reduce low frequency noise which can be a great solution for accurate AoA detection. The content discussed in this chapter was published in [14].

5.2 Gilbert Cell Mixer Topologies

There are two types of Gilbert cell mixers that are applied depending on signal types: a single-balanced and a double-balanced Gilbert cell mixer which are for a single-ended signal and a differential-ended signal, respectively. This RF sensor

in particular requires a double-balanced mixer for a differential RF input since it needs to differentiate the phase differences between the RF+ and RF-. The base topology of a double-balanced Gilbert cell is shown in Fig. 5.1[45]. It mixes a differential RF input ($f=f_1$) with a differential LO input ($f=f_2$) and provides an intermediate frequency (IF) output that consists of two frequency signal terms which are up-converted ($f=f_1+f_2$) and down-converted ($f=f_1-f_2$) signals. Depending on applications, a mixer can be concentrated on either the up-converted or down-converted signals. In this application, zero-IF mixing is intended, which requires the RF and LO signals to be the same frequency. Therefore, the zero-IF outputs consist of the $f=2f_1$ term and the DC signal term. This DC signal term includes the phase difference information to be used for angle-of-arrival computation.

To successfully achieve this goal, there are many design aspects that must be set appropriately. The most important thing is to guarantee the switching operation of the LO stage. This can only be fulfilled when sufficient LO input magnitude is provided to sufficiently swing the LO transistors. For this, there are two conditions to be satisfied. First, sufficient amplification of the LO signal has to be secured before it reaches the LO transistors of the mixer and second, appropriate DC bias must be applied. The first prerequisite is realized by using 4-stage LNAs that take the input from the antenna *Ant-LO* and provide the output to the LO BALUN. The BALUN then converts the amplified single-ended LO to the differential signal to provide the LO+ and LO- for the Gilbert cell mixer. Second, DC biasing of the LO stage must be set as close as $V_{OV} = V_{GS} - V_{TH}=0$. However, achieving $V_{OV}=0$ is not as simple as adjusting the gate bias of the LO transistors. The difficulty

originates from the source node voltage of the LO stages being passively determined along the bias current, the biasing of the RF stages, and the load resistances, as well as secondary factors such as possible process variations and unstable voltage references. To alleviate these issues, an appropriate topology has to be selected that is resilient to these issues.

There are a few topologies of Gilbert cell mixers reported that are intended to enhance the performance of Gilbert cell mixers by taking such issues into account. First is the Gilbert cell mixer with a tail current source (Fig. 5.1)[43]. The tail current source can provide a very specific amount of current to both the RF and LO stages. However, securing the region of operation in saturation for the current source transistors causes the reduction of headroom and linearity of the mixer, limiting the output voltage swing range. Second is the Multi-tahn topology. It has the RF stage consisting of three RF transistor pairs in parallel to maintain constant transconductance g_m throughout a wide range of input as indicated in Fig 5.2[41]. This can be beneficial for wide bandwidth applications, but the headroom and linearity of the mixer is still limited. Third is the current bleeding topology which is shown in Fig. 5.3[50]. The goal of this topology is to provide current directly to the RF stage transistors. The idea is realized by adding an additional transistor stage that provides DC current that flows through the LO stages. In this way, DC current through load resistors is reduced, resulting in increased output headroom, but still a limited linearity. Fourth is the folded cascode mixer (Fig 5.4)[51]. This can reduce power consumption but has drawbacks in linearity.

There are several other topologies for Gilbert cell mixer design, but each topol-

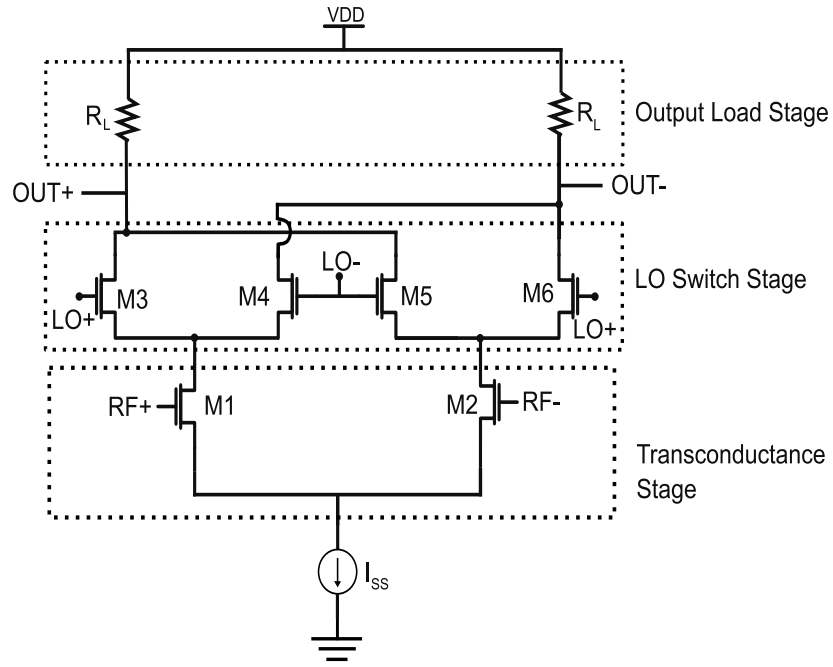


Figure 5.1: A basic double-balanced Gilbert cell mixer schematic with tail current[43].

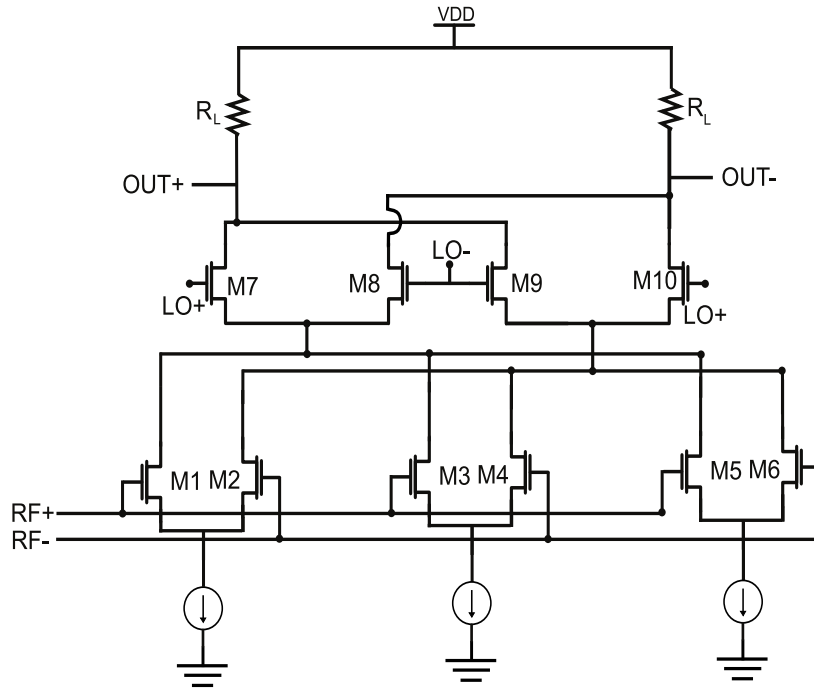


Figure 5.2: A schematic of the Multi-Tanh technique mixer[41].

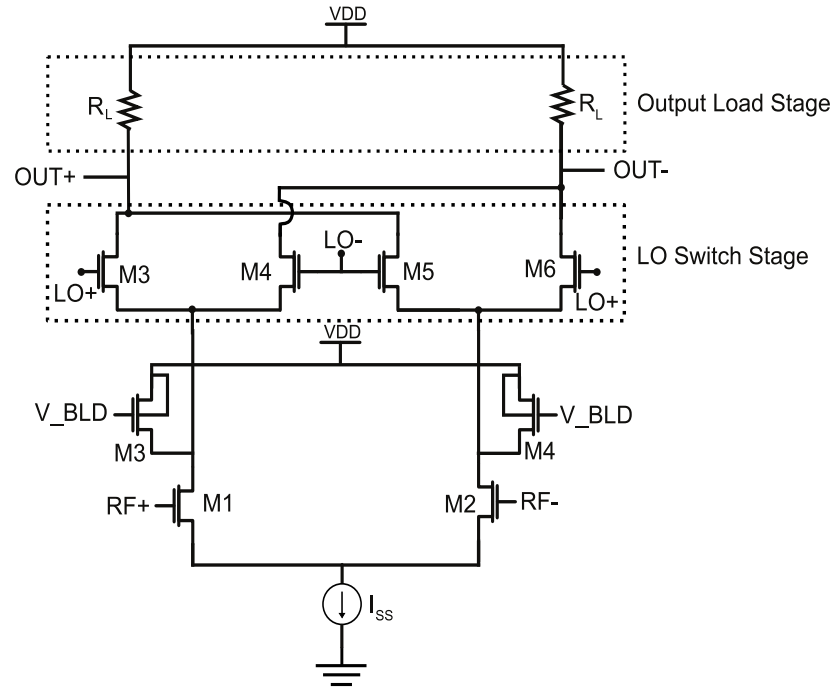


Figure 5.3: A double-balanced mixer with the current bleeding technique[50].

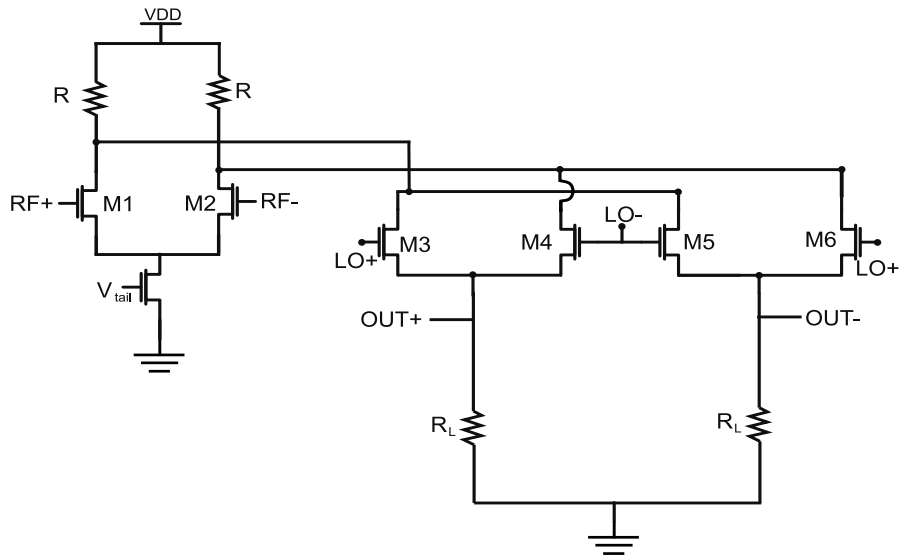


Figure 5.4: A folded cascode mixer[51].

ogy has different design targets with pros and cons depending on applications. In the present application, the main goal is to zero-IF mix with low noise and high linearity.

5.3 Design Approaches and Strategy

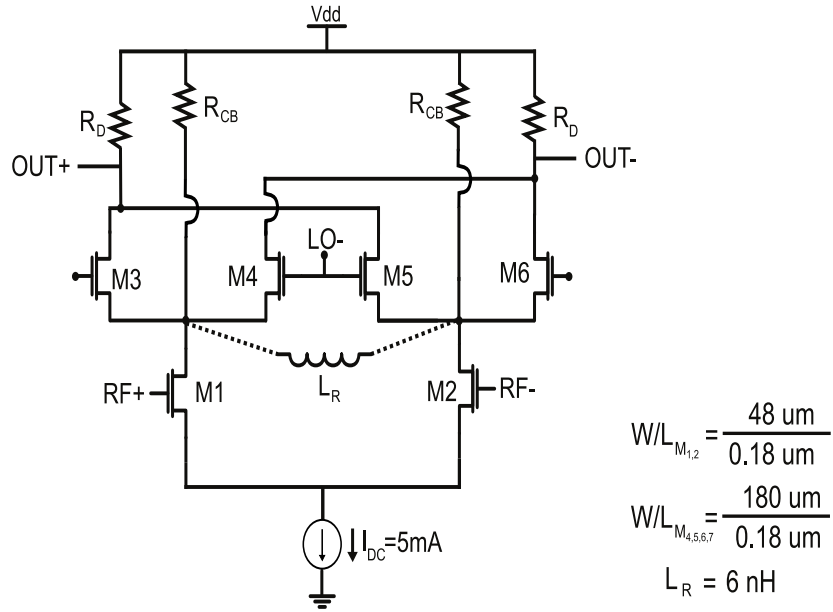


Figure 5.5: The circuit schematic of the designed Gilbert cell mixer in this work based on the developed combined methodology.

Active mixers have high NF, typically above 10dB beyond the flicker noise corner frequency f_c and even higher NF below f_c which derives from flicker noise, and potentially limiting the AoA sensing unless reduced. Specifically, suppression of flicker noise plays a critical role in this sensor since the flicker noise, which is dominant at a low frequency, can generate serious levels of jitter in Equation 2.6 and Equation 2.7, affecting the accuracy of the $\Delta\phi$. In addition, active mixers are vulnerable to intermodulation distortion, particularly to third-order intermodulation

distortion. The Gilbert cell mixer displayed on Fig. 5.5 is designed and developed in order to reduce NF and improve IIP3 while maintaining reasonable conversion gain. For this, the combined methodology with three optimization techniques is applied here. The three techniques applied concurrently are: the current-bleeding, inductive resonance, and g_m/I_D width optimization techniques.

The current bleeding method effectively provides a bypass path for some portion of DC current through the LO switching stages which results in: firstly, less current through the switching stage transistors $M3 - M6$ and secondly, the load resistors R_D allow more headroom for an intermediate frequency (IF) output enabling better linearity and lower flicker noise. There are several ways to achieve current bleeding such as using passive resistors or active loads. In the present model, polysilicon resistors were chosen, which do not contribute flicker noise by themselves (R_{CB}), and are placed between the supply voltage VDD and the drain of the RF transconductance stage $M1$ and $M2$.

The inductive resonance approach deals with the parasitic capacitance at the source node of the switching stage. This parasitic capacitance becomes a source of AC current leakage preventing smooth switching, causing increases in flicker noise, and attenuating or degrading conversion gain (CVG). Placing an inductor across the source node of the LO switching stage effectively cancels out capacitive leakage, enhancing CVG, linearity, and noise.

Lastly, the g_m/I_D based width optimization for the RF and LO stage transistors is used as an alternative to the MOSFET square law which is an inaccurate model for a submicron CMOS technology. The pre-simulated lookup charts gener-

ated in this work and shown in Fig. 3.6 and Fig. 3.7 precisely render intrinsic gain, current density (I_D/W), and unity gain frequency (f_t) to achieve the design goal. The W/L ratio on the RF stage and its bias point determine the transconductance g_m and circuit speed f_t which are both correlated to the circuit linearity and noise level. The W/L ratio on the LO stage and its bias point have a critical impact on flicker noise and MOSFET channel noise, but relatively minor effects on linearity. Significant improvement can be made in the Gilbert cell mixer performance based on these principles and design approaches.

The LO signal is a key element of this circuit. This stage switches on and off to trigger mixing with the RF input signal. Ideally the LO signal has to be a square wave to instantly turn on and off the LO stage transistors for the switching activity. However, the LO input is received from the RF input antenna sources, indicating that it will be coupled to one of the RF antenna input signals, and is in the exact same form as the RF input in sinusoidal waveform. The up-conversion output deriving from these two sources is not symmetrical with 50% duty cycle due to the nonmatching waveform phase of the RF and the LO inputs. However, this non-symmetry is negligible since the sensor is only interested in the down-conversion output which is a DC signal.

Moreover, the LO signal magnitude has an impact on the noise, conversion gain, and total power dissipation. In general, the larger the LO signal is, the cleaner mixing outcome it gets with better SNR resulting in lower NF. This is because the larger the magnitude of the LO, the better chance there is to clearly switch the LO transistors on and off. Although it requires more power to generate a sufficiently

amplified signal for the LO input, it comes with benefits such as cleaner mixing performance with lower NF which is the core interest of this sensor. For this reason, the LO power is targeted to be amplified around the targeted -5 dBm through four consecutive LNA stages.

Conversion gain represents relative amplitude of the IF output to the RF input. While conversion gain is an important factor to secure sufficient SNR, it is also important to secure high phase detection accuracy in this sensor since it directly determines the overall AoA sensing detection quality. The ideal conversion gain (CVG) is equivalent to Equation 5.1.

$$CVG = g_m R_L \quad (5.1)$$

However, the CVG output generally ends up lower than the theoretical model due to the incomplete switching operation of the LO transistors and signal loss due to parasitic capacitances. Therefore, development of an optimal balance among CVG, NF, IIP3 is required to satisfy the need for this mixer's AoA sensing.

5.4 Noise Analysis

Noise is attributed to a few different noise sources such as flicker noise, thermal noise from resistors, and MOSFET channel noise. Flicker noise is frequency-dependent and dominant in the lower frequency range. It is inversely proportional to $W \cdot L$ hence the bigger the $W \cdot L$ is, the lower flicker noise generally. Thermal noise is proportional to resistance of resistors, and channel noise is proportional to

g_{ds} which is approximately equivalent to λI_D . This indicates that higher tail current (I_{DC} , Fig. 5.5) causes more channel noise. On the other hand, a higher tail current lowers conversion gain. Therefore, a balance between the channel noise and CVG is determined by the tail current.

5.5 g_m/I_D Width Parameter Optimization

Maintaining high current and high f_t contribute to overall lower noise. All the transistors in this design are set to the minimum length $L = 180$ nm since L_{min} settles with high I_D/W , f_t and reasonable intrinsic gain. To secure CVG in the ~ 10 dB range, the RF stage is targeted to $g_{m1,2} = 25$ mS with the load resistor $R_L = 500\Omega$. Having both $g_m = 25$ (mS) and $I_{M1,2} = 2.5$ (mA) ($=I_D / 2$) set for $M1$ and $M2$, the $V_{OV} = 0.1$ (V) is found at $g_m/I_D = 10$ (1/V) where $f_t = 40$ (GHz) in Fig. 3.7. Similarly $I_D/W = 22$ (A/m) is determined at $g_m/I_D = 10$ (1/V), providing the $W_{RF} = 113$ (μm). The LO stage bias sits just at the verge of $V_{OV} = 0$ (V) for swift switching action which concludes $W_{LO} = 166$ (μm) for $M3 - M6$ where $I_{M3} = 1.25$ (mA) at $I_D/W = 7.5$ (A/m).

5.6 Further Optimization of the LO Transistors

In addition to the combined optimization methodology given in the three previous sections, further optimization steps and analysis are introduced that resulted in significantly lower flicker noise. The current bleeding technique supplies DC current through the RF transistors ($M1, M2$) which limits DC current through the LO

transistors ($M3-M6$). This reduction of current in the LO stage lowers flicker noise caused during the switching operation. In addition, it leads to more headroom for V_{out} with less DC current through load resistors R_D , allowing higher linearity. To get the best performance from this technique, the present design analysis is focused on the impact of the R_D to R_{CB} ratio. This ratio indirectly determines the DC operation point of the LO transistors and has a significant impact in terms of noise as discussed in section 3.3.

5.7 A Current Mirror for the Gilbert Cell Mixer

The Gilbert cell mixer uses a tail current source. It is comprised of a beta-multiplier circuit and a current mirror stage. The goal of this current source is to provide an accurate 5mA while not being affected by voltage variation of the source node of the RF input transistors. To achieve this goal, the output impedance of the current mirror's output has to be large since it becomes more insensitive to the output voltage variation. This states that the output voltage has to be wide-swing operational.

A cascode current mirror structure is chosen as a base topology. This topology requires a bias voltage reference. The beta-multiplier is used here, (Fig. 5.6) and it is designed upon the consideration to overcome the none-start-up status issue. The presence of the start-up circuit, MSU1, MSU2, MSU3 helps resolving this issue by guaranteeing start-up of the current mirror when the supply voltage turns on[7].

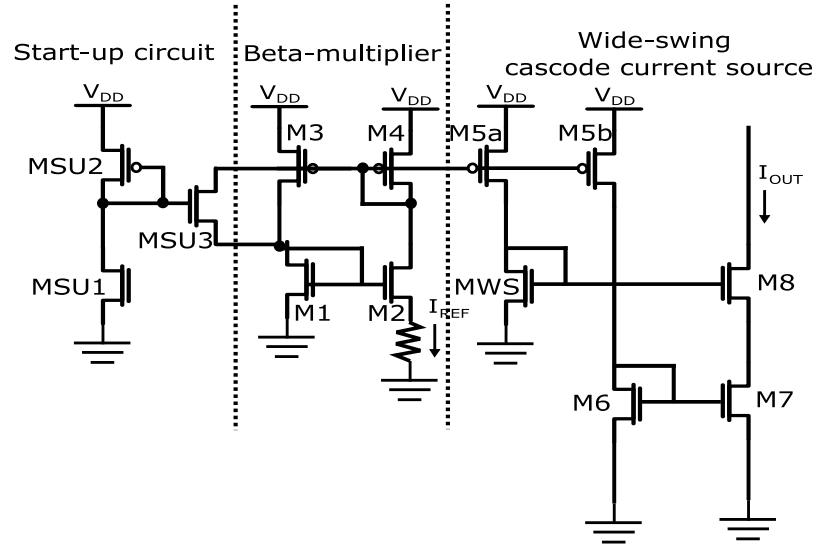


Figure 5.6: A current source circuit developed in this work that includes a beta-multiplier for a voltage reference, a start-up circuit and wide-swing current source[7].

5.8 Results and Analysis

Several simulations were run to determine the ideal parameters and demonstrate the performance of the Gilbert cell mixer. The RF input frequency was at $f = 2.4$ GHz with the IF bandwidth of 10 MHz. Simulations were run on CVG vs. RF power, third-order input intercept point (IIP3) vs. RF power, and noise figure vs. frequency for each of the current bleeding and inductive resonance techniques to characterize their effects independently. The following is the width optimization simulation run for the RF and LO stage transistors employing the current bleeding resistors $R_{CB} = 500 \Omega$ and inductive resonance with $L_R = 6\text{ nH}$. Here, the RF power is swept from -50 dBm to 20 dBm for both CVG vs. RF power and IIP3 vs. RF power. Two tone RF small signals of $f = 2.401$ GHz, 2.401.1 GHz were applied for

IIP3 simulation which results in the output IM1 frequency at 1.1 MHz and IM3 frequency at 0.9 MHz. In the noise figure simulation, an IF sweep from 10 kHz to 100 MHz is carried out.

5.8.1 The Current Bleeding Technique

To estimate the appropriate amount of current bleeding, the simulation is run on varying R_{CB} from 300 Ω to 1100 Ω in 200 Ω steps. Fig. 5.7 shows CVG vs. RF power and IIP3 vs. RF power. It shows the best flat region CVG = 7.3 dB and second highest IIP3 = 2.8 dBm at $R_{CB} = 500 \Omega$. Fig. 5.8 depicts a noise figure where NF = 13.02 dB at $f = 10$ MHz at $R_{CB} = 500 \Omega$. The results indicate that current bleeding resistance has a moderate impact on CVG and IIP3, and a small impact on the noise level.

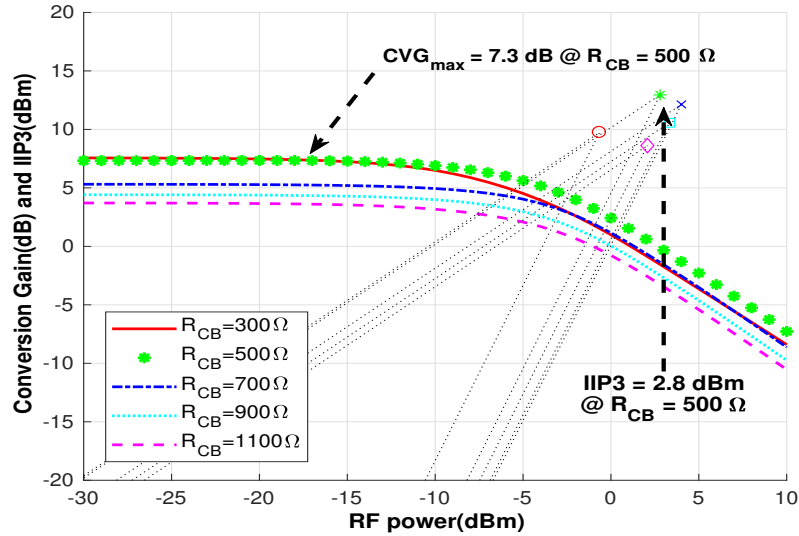


Figure 5.7: CVG and IIP3 vs. P_{RF} (RF input power) with the current bleeding technique. The figure shows the conversion gain and IIP3 with different R_{CB} . The optimal $CVG_{max} = 7.3$ dB, and IIP3 = 2.8 dBm (both in green) at $R_{CB} = 500 \Omega$

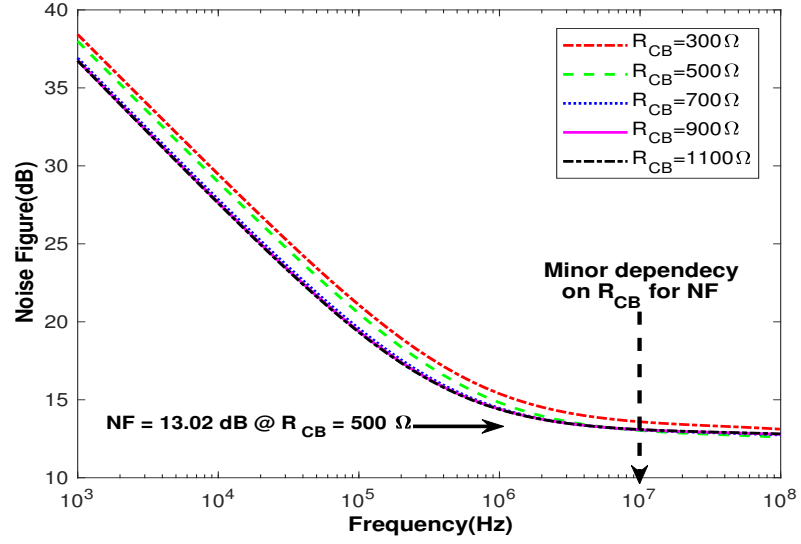


Figure 5.8: NF vs. frequency with the current bleeding technique. The figure shows the minor dependency of NF on R_{CB} at frequency at 10MHz and above.

5.8.2 The Inductive Resonance

The inductive resonance effectively lessens the AC leakage in the LO stage. To find the optimal inductance, the following simulation tested the inductance variables L_R from 2 nH to 10 nH in 2 nH increment steps. Fig. 5.9 shows the CVG and IIP3 vs. RF power demonstrating a flat region of CVG at 7.7 dB and IIP3 at 2 dBm for an inductive value of $L_R = 6$ nH. The noise figure in Fig. 5.10 validates the best flicker noise and flat region noise response $NF = 13.1$ dB with $L_R = 6$ nH at $f = 10$ MHz. The simulation describes critical response to inductance L_R on CVG and NF, while exhibiting minor dependence on IIP3.

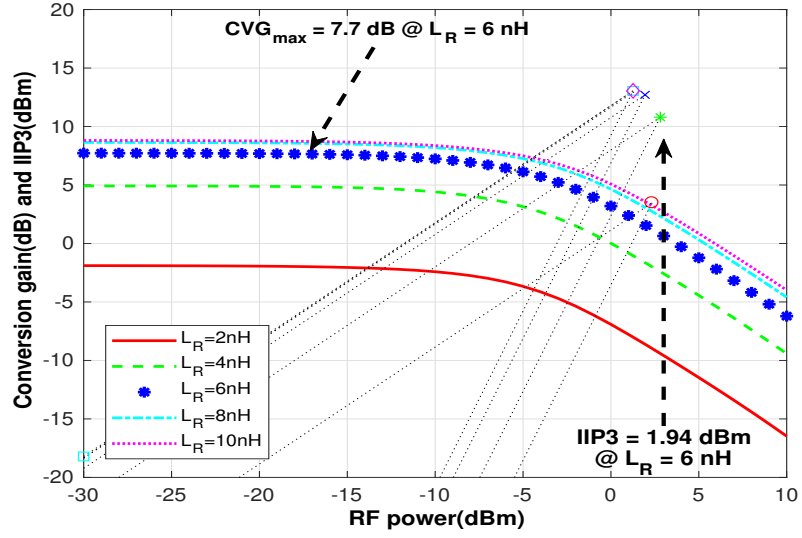


Figure 5.9: CVG and IIP3 vs. P_{RF} with the inductive resonance technique. The figure shows the conversion gain and IIP3 with different L_R . The optimal $CVG_{max} = 7.7\text{dB}$, and $IIP3 = 1.94 \text{ dBm}$ (both in green) at $L_R = 6\text{nH}$.

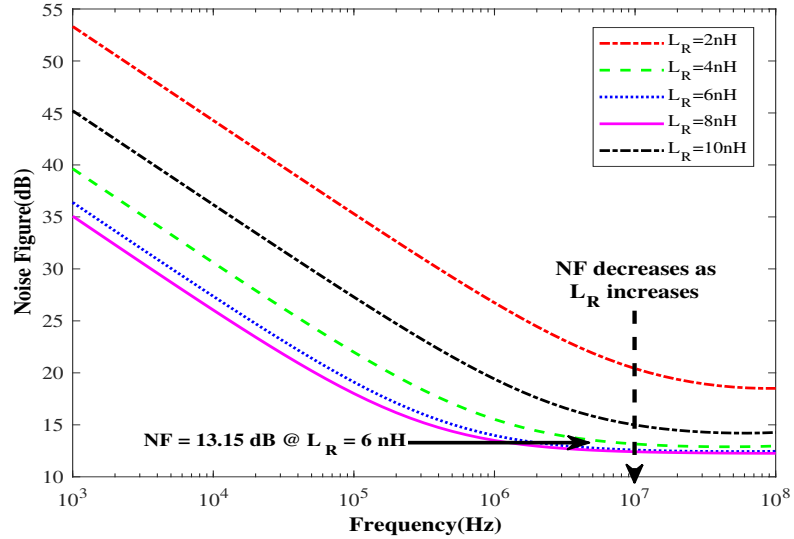


Figure 5.10: NF vs. frequency with the inductive resonance technique. The figure shows that the L_R has significant effects on NF at frequency at 10MHz and above.

5.8.3 The g_m/I_D Algorithm based Width Optimization

The simulation is executed on the RF transistors with width variation from $40\ \mu m$ to $240\ \mu m$ in increments of $40\ \mu m$ in an effort to specify the optimal width for W_{RF} . The model has the inductive resonance with $L_R = 6\text{ nH}$ and the current bleeding with $R_{CB} = 500\ \Omega$ applied and the LO width is set $W_{LO} = 166\ \mu m$. CVG, IIP3 vs. RF power and NF vs. frequency in Fig. 5.11 and Fig. 5.12 which display their width dependence. Here, the RF stage width increment had increases on CVG and decreases on NF representing moderate dependency on RF width, while it showed the best IIP3 at $W_{RF} = 120\ \mu m$ where $g_{m1} = g_{m3}$ is at its maximum. Having the optimized $W_{RF} = 120\ \mu m$, the post simulation was run to characterize the actual performance. With all three optimization techniques combined together, it showed CVG = 4.13 dB, IIP3 at RF power of 11.5 dBm and NF = 14.77 dB at $f = 10\text{ MHz}$ where $W_{RF} = 120\ \mu m$ and $W_{LO} = 160\ \mu m$. Table 5.2 represents the performance comparison of this work against other works. It proves the excellent balance among conversion gain, IIP3, and noise figure of this model.

5.8.4 Flicker Noise Optimization

Even with the optimization technique that enhanced the performance of the mixer, it is necessary to further optimize the low frequency flicker noise, as the low frequency noise still appeared to be at a high level, above 20 dB at f below 10 kHz. In order to analyze the impact of R_{CB} to R_D ratio on the GCM, R_D ranges between $400\ \Omega$ to $2400\ \Omega$ in $400\ \Omega$ steps. Fig. 5.13 shows the NF vs. R_{CB} at $R_{CB} = 500$

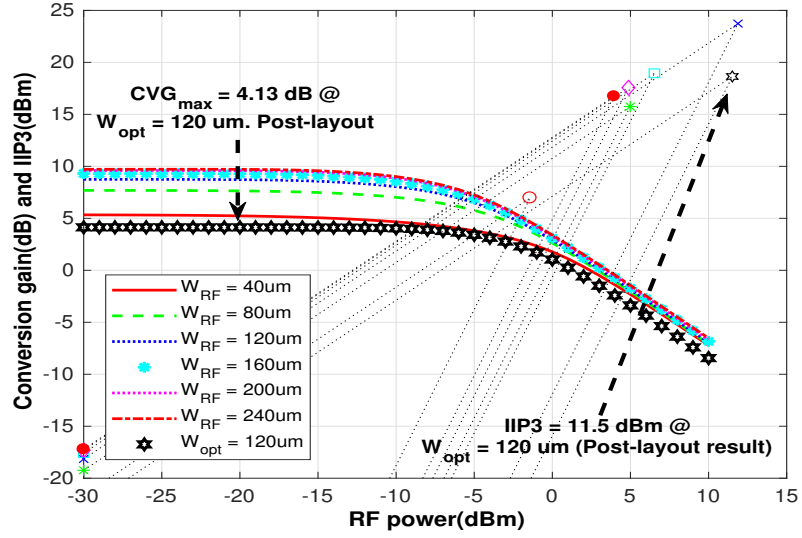


Figure 5.11: CVG and IIP3 vs. P_{RF} with width W_{opt} variation of the RF transistor. The figure shows A. The pre-layout shows the optimal CVG and IIP3 at $W_{opt} = 120 \mu m$ (light blue). B. The post-layout evaluation also showing the optimal width at $W_{opt} = 120 \mu m$, where it shows CVG = 4.13 dB and IIP3 = 11.5 dBm(black).

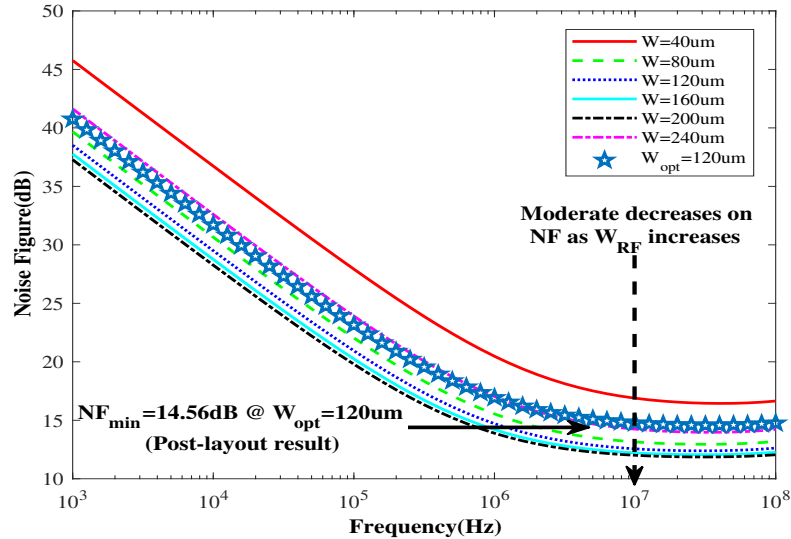


Figure 5.12: NF vs. frequency with width W_{opt} variation of the RF transistor. The figure shows moderate NF dependency to RF transistor width. The NF = 14.56 dB at $W_{opt} = 120 \mu m$ in post-layout.

Ω . A critical difference is observed on flicker noise ranging from $NF = 42.74$ dB ($R_D = 400 \Omega$) to 14.68 dB ($R_D = 2400 \Omega$) at $f=1$ kHz. Flicker noise level saturates above $R_D = 2000 \Omega$. To understand the origin of this high level of flicker noise at low R_{CB} to R_D ratio, the transconductance g_m of $M7-10$ vs. R_D is examined and plotted Fig. 5.14. The result reveals an inverse relationship between g_m and R_D which explains the significant decrease in flicker noise at the higher ratio. Next, the conversion gain vs. frequency is shown in Fig. 5.15 where it showed the flat-region gain of 4.29 dB that is a reasonable level of gain to process the AoA sensing. Another important feature examined is the IIP3 shown in Fig. 5.16. It demonstrates minor dependence to R_D on linearity for R_D above 800Ω , indicating the highest IIP3 = 11.63 dBm at $R_D = 400 \Omega$. The flicker noise also shows dependence on DC operation points of the LO transistors, which can be explained by the choice of R_D (Table 5.1). As R_D increases, V_{DS} gets dramatically smaller similar to flicker noise decreases. Specifically, the flicker noise level has a noteworthy improvement as V_{DS} is almost equal to $V_{DS,sat}$ which validates that flicker noise is optimized around the triode and saturation region of the MOSFETs. Based on the results, $R_D = 2000 \Omega$ is chosen as the optimal value giving $NF = 15.07$ dB at $f = 1$ kHz, IIP3 = 5.85 dBm and conversion gain = 4.29 dB. This result is far better than that at $R_D = 400 \Omega$ where it showed almost 30 dB higher NF at $f = 1$ kHz although with a higher IIP3 at 10.85 dBm.

In summary, adjusting R_D in a way that V_{DS} gets close to $V_{DS,sat}$ and additionally reducing the g_m allows the LO transistors to operate right at the edge of the triode to the saturation region where the flicker noise is low with a reasonable

R_D (Ω)	V_{GS} (mV)	V_{DS} (mV)	$V_{DS,sat}$ (mV)	g_m (mA/V)	NF @ f= 1kHz
400	652.35	695.27	57.01	8.52	42.74
800	661.492	391.57	57.69	8.15	33.68
1200	673.13	124.446	59.29	7.56	20.77
1600	705.91	21.77	69.128	4.66	16.16
2000	738.98	10.209	82.16	2.95	15.07
2400	762.94	6.43	92.698	2.14	14.68

Table 5.1: The GCM parameters according to R_D .

IIP3. Table 5.2 compares the performance of the GCM with previous works. The presented Gilbert cell mixer shows superior linearity of IIP3 = 5.85 dBm and excellent low flicker noise with NF = 15.07 dB at $f = 1$ kHz, demonstrating the great potential for the AoA sensing applications.

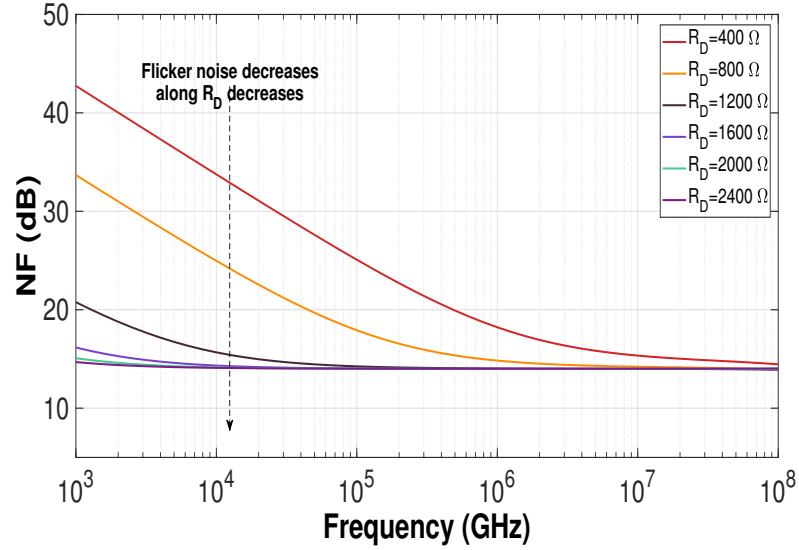


Figure 5.13: NF vs. R_{CB} on the GCM. Flicker noise decreases as R_{CB} increases.

5.9 Summary

The development of the double-balanced Gilbert cell mixer circuit demonstrated an efficient systematic design process based on combined optimization method-

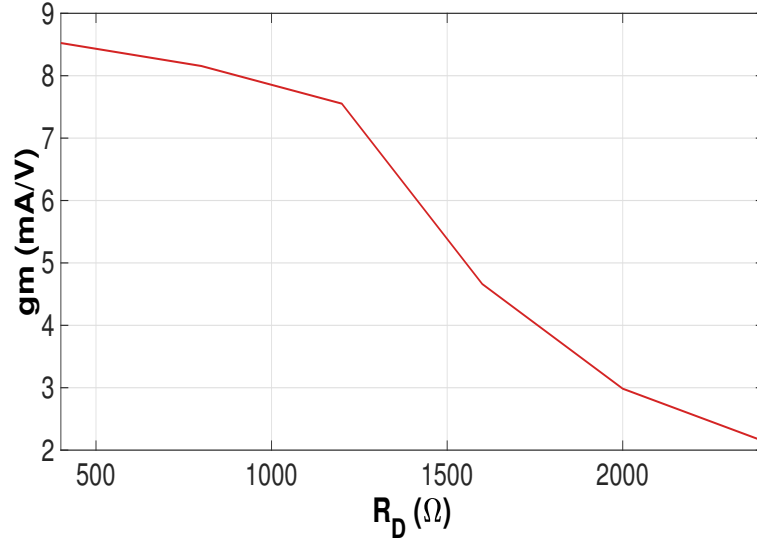


Figure 5.14: g_m of the LO transistors vs. R_{CB} on the GCM. The figure shows g_m dramatically decrease with higher R_{CB} .

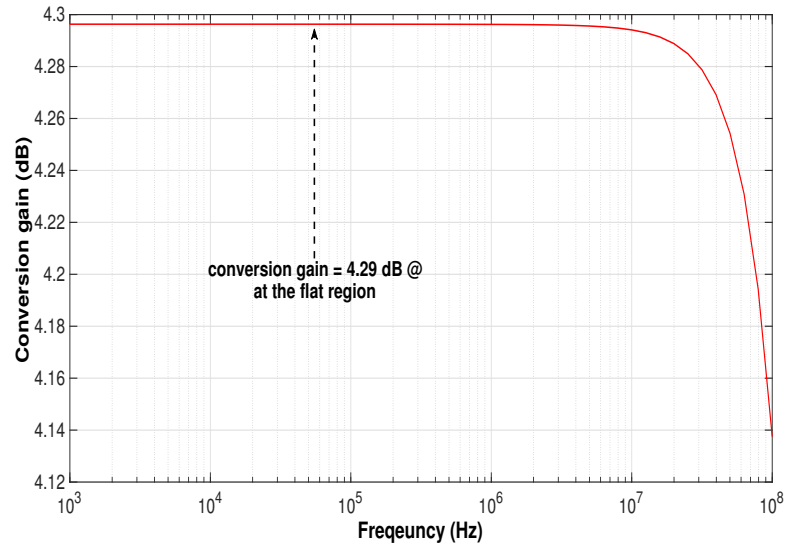


Figure 5.15: Conversion gain vs. frequency on the GCM at the RF power of $P_{RF} = -30$ dBm. The conversion gain settles at CVG = 4.29dB in the flat region.

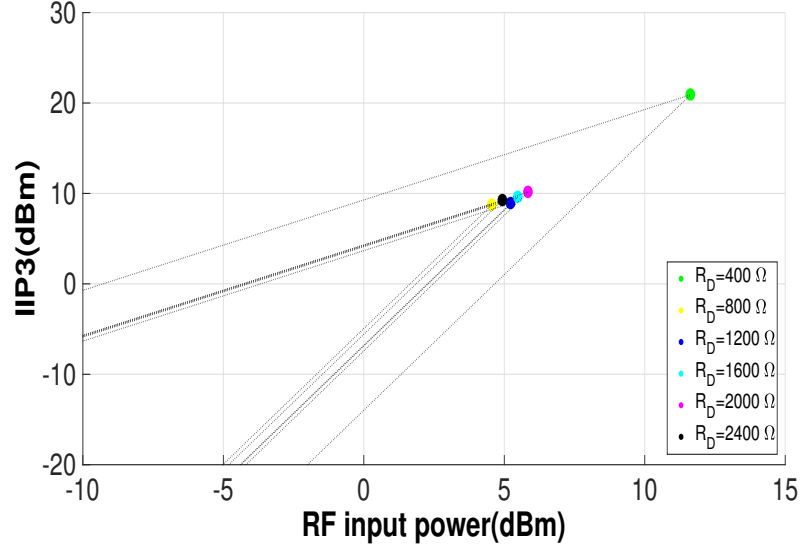


Figure 5.16: IIP3 vs. R_D on the GCM with the two tone RF inputs of $f_1 = 2.4$ GHz and $f_2 = 2.41$ GHz. The figure shows the minor IIP3 dependency on R_{CB} .

ology developed here, that concurrently included current bleeding, inductive resonance, and g_m/I_D based width optimization techniques. The mixer is based on 180 nm CMOS technology for target operation frequency at 2.4 GHz. The current bleeding resulted in great improvement on CVG by 3.8 dB and IIP3 by 4.6 dBm, and the inductive resonance validated significant enhancement in NF and CVG by 7.2 dB and 10.7 dB comparing the best and the worst scenario. The g_m/I_D based width optimization showed strong agreement between the estimated calculation and

References	CVG (dB)	IIP3 (dBm)	NF (dB)	Power (mW)	CMOS tech (nm)
This work	4.29	5.85	15.07	9	180
[38]	10.3	0	12	4.3	130
[42]	13.8	-4	8.2**	2.7	130
[39]	13.1	-2.8	11.9	1.5	130
[56]	7.1	-6.9	19.6*	2.95	180
[34]	2	12.7	12.87*	4.32	180
[47]	9.95	N/A	8.12	3.5	180

Table 5.2: Comparison of the Gilbert cell mixer with previous works.

the simulation results to be utilized for systematic optimization. The optimal current bleeding was validated to work optimally when it put the LO transistors in the vicinity of the linear mode and saturation mode operation. Combining all the optimization techniques, the Gilbert cell mixer exhibited an excellent post-layout simulation result with $\text{CVG} = 4.13 \text{ dB}$, $\text{NF} = 14.77 \text{ dB}$, $\text{IIP3} = 11.5 \text{ dBm}$.

Chapter 6: Chip Layout, Pad Frame, Packaging, and PCB Effects

6.1 Introduction

This chapter discusses the side effects of layout, a pad frame, and a package and ways to mitigate and reduce such side effects. These are essential parts of the AoA sensor that consist of the IC chip that is interconnected to the 2 *mm* x 2 *mm* pad frame and the DIP40 package. Each circuit module in the system is established on the initial schematic design. The circuit layout is created and extracted to evaluate layout factors. Then their parasitic effects are counted in for post-layout design characterization for the most accurate estimation of the circuit module. Intersections in the layout generally degrade the performance to a certain extent relative to the ideal schematic design performance due to inherent parasitic RLCs. Therefore, the layout design is a major focus in minimizing parasitics.

A pad frame and an electrical package are essential parts of this sensor since they are responsible for delivering signals in and out of the chip, interconnecting the chip and the outside world. While wafer level measurement shows the true performance of the circuit on its own, a pad frame and an electrical package cause signal attenuation, distortion, delay, and noise to some degree, constraining the capability of the designed circuit. Therefore, the objectives of a pad frame design

and electrical packaging are to reduce degrading effects. The content discussed in this chapter was published in [15].

6.2 Layout Considerations and Floor Planning

One of the side effects that RLC parasitics cause is the DC offset, which can become a major source of mismatching between the final system output V_{OUT+} and V_{OUT-} . An effective floor plan is essential to equalize the metal trace length between differential signal inputs/outputs such as V_{IN+} , V_{IN-} and V_{OUT+} , V_{OUT-} to minimize such offset. Moreover, metal layers interconnect overlapping, or crisscrossing become sources of parasitic R,L and C. Ideally, it is beneficial to keep an optimum distance between signal traces to avoid any unwanted crosstalk and possible inductive parasitic effects. Especially interconnection traces delivering large signals such as VDD and GND have a significant impact on the chip, and must be carefully located and routed to secure a sufficient distance with other interconnect traces.

In addition, there are non-negligible parasitic capacitances that originate from intersecting interconnect-traces. For example, traces that stretch vertically and the ones that run horizontally form an intersecting node and build parasitic capacitances. Therefore, attention needs to be paid to minimize such parasitics since they may cause a failure of the chip operation. Since a capacitance is inversely proportional to the distance between two metallic plates separated by a dielectric medium, increasing the distance of these intersecting node lowers capacitances. Therefore, using far-distanced two metallic layers (e.g. $M6$ and $M1$ layers) can be very ef-

fective in reducing the parasitics in comparison to relatively closer distanced layers (e.g. $M3$ and $M2$ layers), without sacrificing other performance factors. This layout strategy can be important in order to avoid performance degradation, especially in those nodes that are more sensitive to parasitic capacitances rather than parasitic resistances.

Another consideration is to secure an appropriate signal interconnect trace width to achieve a good balance between low parasitic resistance and capacitance. Resistance in metal is proportional to $\rho \cdot l/A$. Therefore, enlarging an area lessens parasitic resistance effectively. However, it also becomes a source of larger parasitic capacitance. Thus, an optimal width must be determined according to the traces of interest that may require more suppression either on parasitic resistance or capacitance. In this sensor design, metal interconnect trace are prioritized to $M1$, $M2$, $M3$ layers for horizontal traces and $M4$, $M5$, $M6$ layers for vertical traces.

I/O pin assignment on this pad frame also has an impact and must be designated as symmetrically as possible. After establishing a fundamental floor plan and layout strategies, finalizing the chip layout becomes an iterative process as the layout has to be revisited by reflecting the post-layout simulation results analysis. That way, it can reduce the DC offset as low as possible. In addition, certain levels of DC offset can also be compensated by dummy metal traces. Fig. 6.1 indicates the chip layout floor plan. The $2\text{ mm} \times 2\text{ mm}$ layout is equally divided into 9 sections. The LNAs for $Ant1 - \theta$, $Ant2 - \theta$, $Ant3 - \psi$, $Ant4 - \psi$ are located at each corner section of the layout and four-stage LNAs in series for the LO signal amplification are located in between these LNAs sections, resulting all the surrounding 8 corners

occupied by the four RF LNAs and the four-stage LO LNAs. Each LNA section takes approximately $600\ \mu m \times 600\ \mu m$ space. Three spiral inductors that come with each LNA take up large portion in these module areas represented in circular spaces as shown in Fig 6.2.

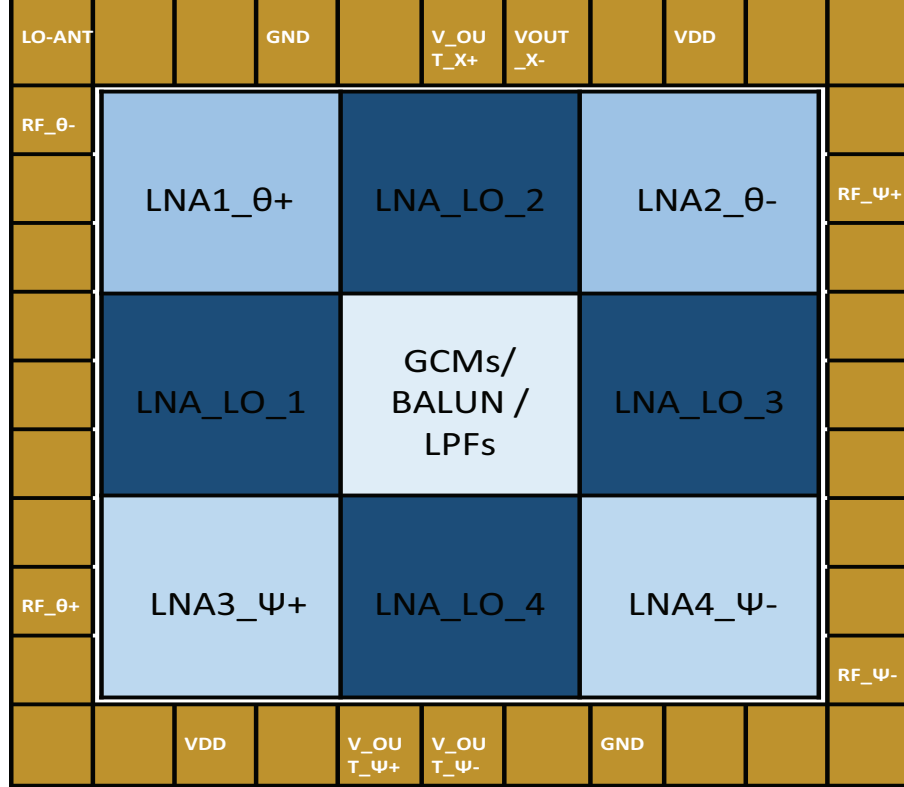


Figure 6.1: The equivalent floor planning and I/O pin assignments on the pad frame.

The GCMs and their corresponding current mirror stages, the low-pass filters, and the LO BALUN circuits are concentrated at the very center section of the chip in the $600\ mm \times 600\ mm$ space. Having these modules located at the center of the chip enables better symmetry to the RF and LO LNAs. This is especially so, since the Gilbert cell mixer is the most sensitive module towards DC offset amongst all the others. I/O pin assignments for $Ant1 - \theta$, $Ant2 - \theta$, $Ant3 - \psi$, and $Ant4 - \psi$ are presented in the bond pads shown in the outer most space in Fig. 6.1. These

are all distributed at each corner of the pad frame for symmetry. Lastly the design rules, wirebond rules, and antenna rules have to be taken into consideration so that the layout can be fabricated along the vendor's requirements.

Pin assignments were placed to secure tolerable space among critical pins. Having two or more critical pins placed right next to each other derives mutual inductance, capacitance and/or more additional noise. This tendency is especially true for pins with low SNR such as the LNA input sources. Similarly, it was vital to minimize the number of pins assigned to the pad frame to reduce any additional noise. Although it would be easier for diagnostic purposes to get as many pins connected as possible by allowing a probe access to more circuit nodes, it also can trigger systematic chaos by adding more noise, and electromagnetic induction. The overall chip layout is shown in Fig. 6.2.

6.3 Bond Pads and Pad Frame Issues

After finalizing the circuit layout, the pad frame comes into play in order to interconnect all I/O signals of the chip and the custom designed chip mounting PCB. The signal travels through the IC to the DIP40 package to the chip mounting PCB and vice versa. In this sensor, the DIP40 package is used with the custom designed chip mounting PCB that includes connectors and external components to interconnect them together with the sensor IC. The pad frame is placed around the border of the IC and takes up the outer most space of the $2\text{ mm} \times 2\text{ mm}$ and is built with 40 bond pads. Each of these I/O bond pads are hardwired to the DIP

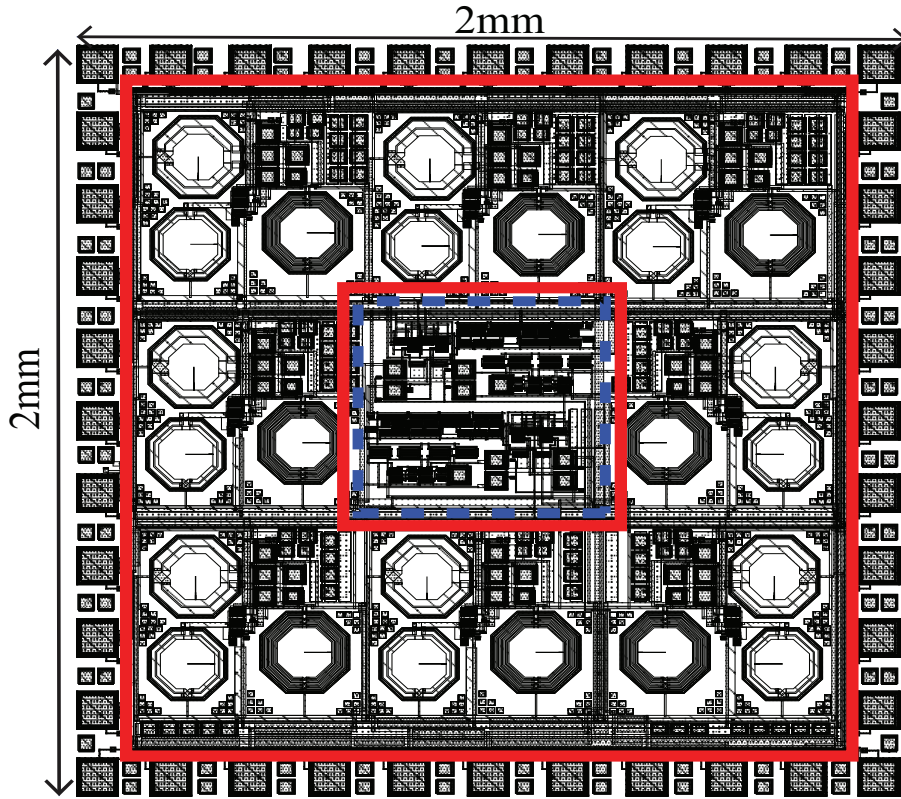


Figure 6.2: The chip layout including the pad frame. The center section includes the GCMs, LPFs, and BALUN circuit.

40 package pins through a gold wirebond. Space dimension of bond pads differs depending on the vendor's specification and systematic requirements, although they generally range from $40\ \mu m \times 40\ \mu m$ to $120\ \mu m \times 120\ \mu m$ in square shape. This sensor pad frame is designed with the $100\ \mu m \times 100\ \mu m$ bond pads. Bond pads must always be located at the top metal layer since the top most metal surface is where the wirebond is applied. Before this process is accomplished, the glass passivation cut process has to be completed as shown in Fig. 6.3. These $100\ \mu m \times 100\ \mu m$ bond pads reveal that the metal layers of the overlapped bond pads had to be accounted in the design process since this large area constructs relatively larger parasitic capacitance.

The connection between the I/O bond pads and the ICs has to be accomplished in a tapered manner by avoiding abrupt changes of traces as an example shown in Fig. 6.4. While the one side of the interconnection on the bond pad has $100\ \mu m$ metal trace width, the signal paths in the circuit node usually measures at a $\sim 1\mu m$ scale. This disparity in width can cause significant resistance. Metal traces are designed in a tapered shape to transform this shifting smoothly.

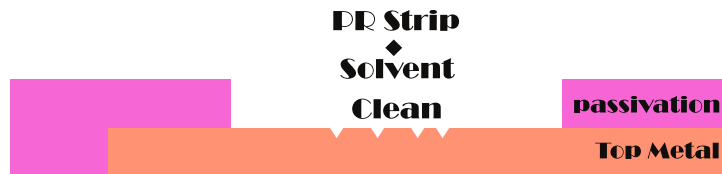


Figure 6.3: Cross-section view of Top Metal and Passivation of Bond Pad [1].

The pitch of the IC Pad frame is set in $187\ \mu m$ so that all 40 bond pads are

aligned with equal distances between them, using the maximum space for the 2 mm x 2 mm chip area. The 187 μm pitch allows for aligning 11 pads on each side that corresponds to the dimension of 1970 μm . Specifically, 11 pads of 100 μm which are a distance of 87 μm from each other, form the total dimension of 1970 μm ($11 \times 100 \mu m + 10 \times 87 \mu m$ (corner pitch) = $1100 \mu m + 870 \mu m = 1970 \mu m$) on each side. A space of 30 μm space is left on each corner as a margin, to ensure room for saw-cutting during the fabrication process.

The next consideration in the pad frame design is an electrostatic discharge diode (ESD) protection. ESDs are necessary to protect the chip from potential electrostatic discharge. To achieve the protection through them, each bond pad is set up with the ESD protection circuits with low 50 fF load capacitance. These diodes are bidirectional to protect the circuit when circuit nodes are exposed to impulsive (spike) signals, releasing the charge effectively towards either VDD or GND depending on the direction of the impulsive signals. Impulsive signals momentarily change the bias of either the D1 or D2 which activates a diode forward bias, effectively bleeding excessive charges and protecting the chip accordingly (Fig. 6.5). 50 fF capacitance can still be heavy for certain circuit application, such as RF circuits that require sophisticated impedance matching. For this reason, critical circuit nodes have to count ESD diode capacitance within the design process to specifically predict and be able to analyze true performance of chips.

A guard ring is another protective layout tactic. A guard ring is paired with each RF transistor since RF transistors require extra protection for better sensitivity. In addition, VDD and GND metal traces surrounding the pad frame come with

guard rings. They can flexibly provide power rails to any part of the chip while effectively insulating them from noise by draining noise to substrate.

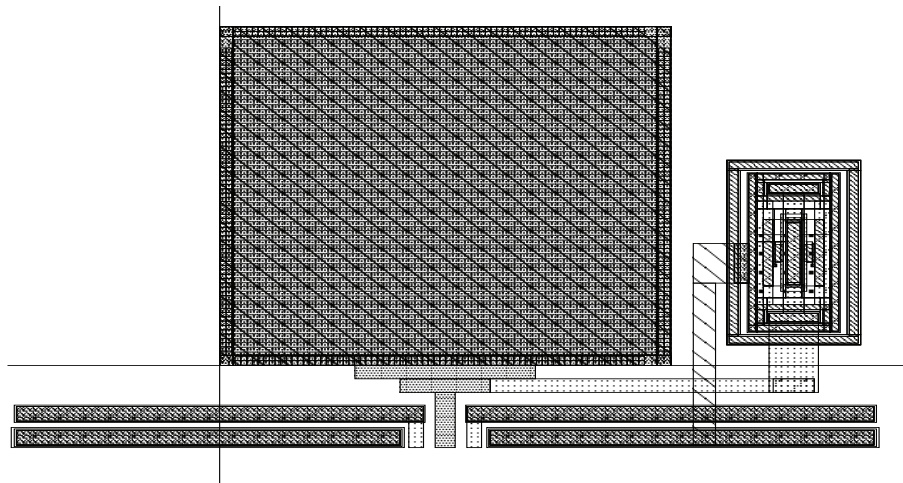


Figure 6.4: I/O Bond Pad layout. The bond pad is $100\ \mu m \times 100\ \mu m$ dimension with the ESD protection circuits on its side.

Fig. 6.4 displays the layout of the I/O bond pad with a $100\ \mu m \times 100\ \mu m$ dimension with the ESD protection circuits on its side. At the bottom, the VDD and GND guard rings are shown. The 40 cells of these modules organizes the pad frame that surrounds the ICs. The pad frame layout is shown in Fig. 6.6.

6.4 Packaging and PCB Consideration

The DIP40 package manufacturer provides a datasheet that represents an equivalent RLC circuit model for characterization. Fig. 6.7 shows an equivalent serial RLC model that characterizes the wirebond represented by R_1 , L_1 , and C values. These values vary depending on pins since each pin has different signal traces and are shown in Table 6.1.

These values become an indicator to decide which pins to assign to specific

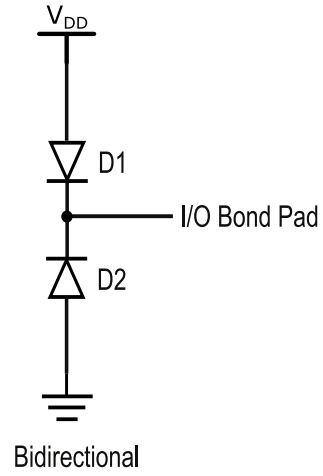


Figure 6.5: Bidirectional ESD protection circuits. The two diodes D1 and D2 together form 50 fF load.

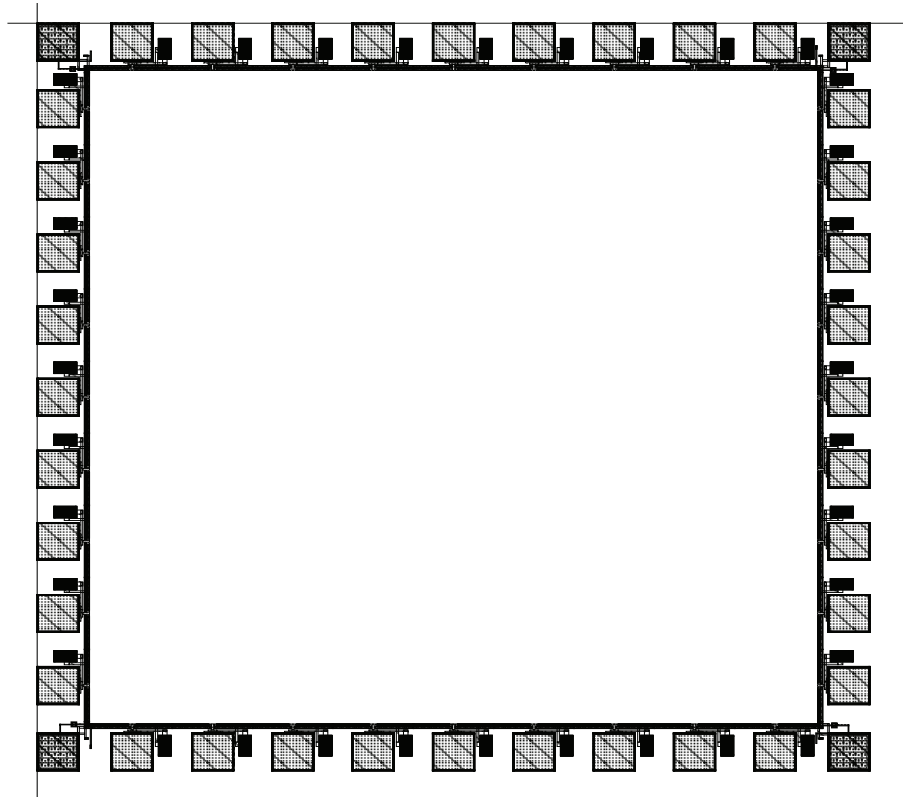


Figure 6.6: The designed pad frame with 40 I/O bond pads in 1.97 mm x 1.97 mm dimension.

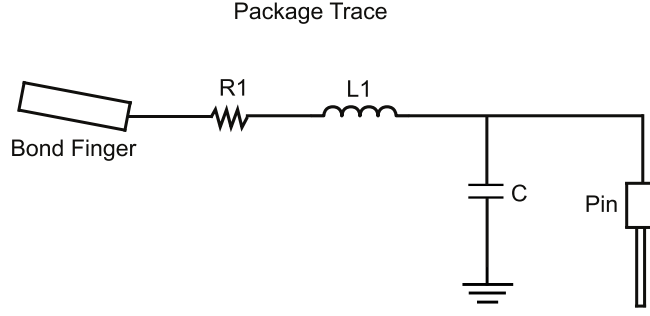


Figure 6.7: An equivalent RLC model between bond finger to pin for the DIP 40 package[35].

nodes because these parameters must be counted to accurately evaluate the model. Otherwise, it results in failure, particularly negatively affecting the operation of sensitive nodes with low SNR. Therefore the data in Table 6.1 turn into a gauge for I/O assignments.

PIN	R1 (Ω)	L1 (nH)	C (pF)	t_{of} (ps)
1,20,21,40	0.217	8.18	5.32	209
2,19,22,39	0.177	7.92	4.39	187
3,18,23,38	0.154	7.34	3.37	156
4,17,24,37	0.110	6.48	2.34	123
5,16,25,36	0.103	5.69	2.16	111
6,15,26,35	0.0661	4.37	1.43	79.0
7,14,27,34	0.0646	4.54	1.48	81.9
8,13,28,33	0.0498	3.69	1.05	62.3
9,12,29,32	0.0378	3.54	0.863	55.3
10,11,30,31	0.0247	3.15	0.660	45.6

Table 6.1: Electrical characteristics of the DIP 40 package[35].

It is also possible to take advantage of these unwanted parasitic parameters in the Table 6.1 and use their values instead of components. Source inductance of LNAs is sometimes utilized by using these parameters since the inductance range for the source inductances is usually small (below 1nH) which is a realistic value to be covered by these RLC parasitics. However, this approach was not applied for

this sensor since the provided data from Table 6.1 did not meet the requirements for the sensor.

A custom chip mounting PCB was designed and fabricated to accommodate the chip mount and peripheral elements for the RF inputs/outputs and testing. The PCB includes a chip mount for the chip packaged in DIP40, I/O BNC connectors for antennas and RF test signals, final system output, and other external components that are needed for on-chip implementation such as coupling capacitors and inductors. Fig. 6.8 shows the overall structure of the sensor system which consists of the four RF inputs, each going into the LNAs, and the two LO input connections which are fed to one of the four RF inputs for zero-IF mixing. Two sets of the RF+, RF- are for the azimuthal and polar angle measurement, respectively. One of the biggest challenges of this PCB layout is keeping critical signal traces as symmetrical as possible to avoid unwanted offset and errors that negatively influence the AoA computation. This is especially true at the PCB design-level because physical scale of the traces is much bigger than those inside the chip. Unwanted crosstalk from proximity signal traces induces noise and signal attenuation, so optimizing PCB space among critical signal traces, space allowing, is very important to attenuate these side effects.

6.5 Summary

The sensor IC layout and floor planning optimization strategy developed here, was discussed to effectively minimize signal transmission interruption due to their

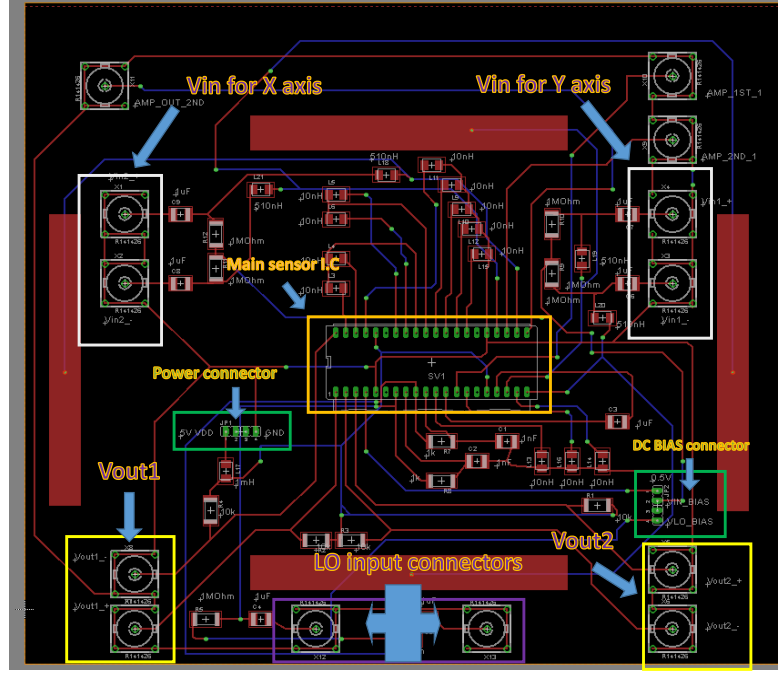


Figure 6.8: The custom mounting PCB with its floorplan.

proximity and parasitic effects. Next, the pad frame design was presented including the details of bond pads and the accompanied ESD protection circuits. Sizing of bond pads and their I/O assignments were carefully inspected to suppress DC offset and avoid potential sources of parasitics and signal degradation. Finally, the DIP40 package characterization table was analyzed to optimally adapt its RLC data to match each pin to corresponding nodes in the sensor IC.

Chapter 7: Evaluation of the AoA Sensor and Conclusions

7.1 Overall System-Level Evaluation

The AoA sensor receives the remote RF signal through the antennas and extracts the phase difference (Equation 2.10) for polar and azimuthal incident angle as discussed in chapter 2, which it then converts into a DC voltage map (Equation 2.6, 2.7) capable of input to analog-to-digital converter (ADC) (Equation 2.8, 2.9) for processing. Thus the sensor provides the V_{OUT} of Equation 2.6, 2.7 dependent on the RF input phase. The purpose of a system-level simulation in this section is to verify the phase difference $\Delta\phi$ to the corresponding analog voltage response. This testing was done by generating direct RF+ and RF- signals entering the sensor at incident angle $\angle\text{AoA}$. This is realized by having the RF+ input phase swept from 0° to 360° while keeping the RF- phase fixed to 0° for simplicity to ensure relative phase difference between the RF+ and RF- signal inputs. The sensor then transforms the phase difference into a DC voltage map as shown in Fig. 7.1. Fig. 7.1 shows the differential low pass filter outputs, Equation 2.6, 2.7, for the RF+ input phase which varied between 0° and 360° in 20° increments for the pre-layout circuit which excludes any layout parasitic effects. The results in Fig. 7.1 show the transformation of $\Delta\phi$ into output DC voltage with a family of output voltages

corresponding to $\Delta\phi$ in every 20° increments where an increase is observed as $\Delta\phi$ increases from 0° to 180° and a decrease from 180° to 360° reaching a steady-state saturated DC voltage at 130 ns. The phase difference $\Delta\phi$ is measured at the steady-state point (130ns) to allow multiple measurements of an event within seconds and provide a fast-sampling rate for the microcontroller to increase sensing confidence.

To further characterize and analyze the performance of the chip, a post-layout evaluation (Fig 7.2) is also run based on the chip post-layout parameters. Both results show that a steady-state is reached at approximately $t = 130$ ns. As $\Delta\phi$ varies on the RF+ and RF-, the pre-layout result shows increases in voltage from $V_{out}=-12.6$ mV at $\Delta\phi = 0^\circ$ to $V_{out}=+12.6$ mV at $\Delta\phi = 180^\circ$ and symmetrically decreases in voltage from $V_{out}=+12.6$ mV at $\Delta\phi = 180^\circ$ to $V_{out}=-12.6$ mV at $\Delta\phi = 360^\circ$ ($=0^\circ$) providing a swing range of 25.2 mV. Similarly the post-layout result shows increases in voltage from $V_{out}=-13.6$ mV at $\Delta\phi = 0^\circ$ to $V_{out}=+7.4$ mV at $\Delta\phi = 180^\circ$ and symmetrically decreases in voltage from $V_{out}=+7.4$ mV at $\Delta\phi = 180^\circ$ to $V_{out}=-13.6$ mV at $\Delta\phi = 360^\circ$ ($=0^\circ$), with a reduced swing range of 21 mV in comparison to the 25.2 mV of the pre-layout result. Furthermore, the output DC offset voltage at $t = 0$ s for the pre-layout and the post-layout are 0 mV and -13.4 mV, respectively. This non-symmetry originates from the parasitic RLCs of the metal interconnects in the post-layout circuit and it is accounted for the circuit extraction parameters for AoA computation. In addition, the reduction in the swing range derives from the reduced conversion gain in the post-layout case.

The compression of the swing range in the post-layout case (21 mV) can reduce somewhat the detection accuracy during the analog-to-digital conversion process for

Equation 2.8 and Equation 2.9. Therefore, in order to characterize the maximum error of the sensor, an 18 bit analog-to-digital converter (ADC) is used as a reference. For example, an 18 bit ADC with a maximum input voltage of 5V has a maximum error of $5/2^{18} = 0.019 \text{ mV}$. The calculation of the maximum AoA error around $\angle \text{AoA} = 90^\circ$ and for AoA error around $\angle \text{AoA} = 0^\circ$ are shown below in Equation 7.1, 7.2 and Equation 7.3, 7.4, respectively.

$$\frac{A \cos(90^\circ) - A \cos(\phi_x)}{A \cos(0^\circ) - A \cos(180^\circ)} = \frac{0.019 \text{ mV}}{21 \text{ mV}} \quad (7.1)$$

$$\phi_x = \cos^{-1}(\cos(90^\circ) - (0.019/21) * (\cos(0) - \cos(\pi))) = 90.103^\circ \quad (7.2)$$

The calculation above shows a maximum AoA detection error of $\Delta\phi = 90^\circ - \phi_x = 0.103^\circ$ for an 18 bit ADC. Similarly, the calculation of the maximum AoA error around $\angle \text{AoA} = 0^\circ$ follows below.

$$\frac{A \cos(0^\circ) - A \cos(\phi_y)}{A \cos(0^\circ) - A \cos(180^\circ)} = \frac{0.019 \text{ mV}}{21 \text{ mV}} \quad (7.3)$$

$$\phi_y = \cos^{-1}(\cos(0^\circ) - (0.019/21) * (\cos(0) - \cos(\pi))) = 3.447^\circ \quad (7.4)$$

where $\Delta\phi = 0^\circ - \phi_y = 3.447^\circ$. A relatively large error range is shown in this case. In summary, the results demonstrate stable AoA sensing capability of this system, with a quantified upper limit of AoA error of 3.447° .

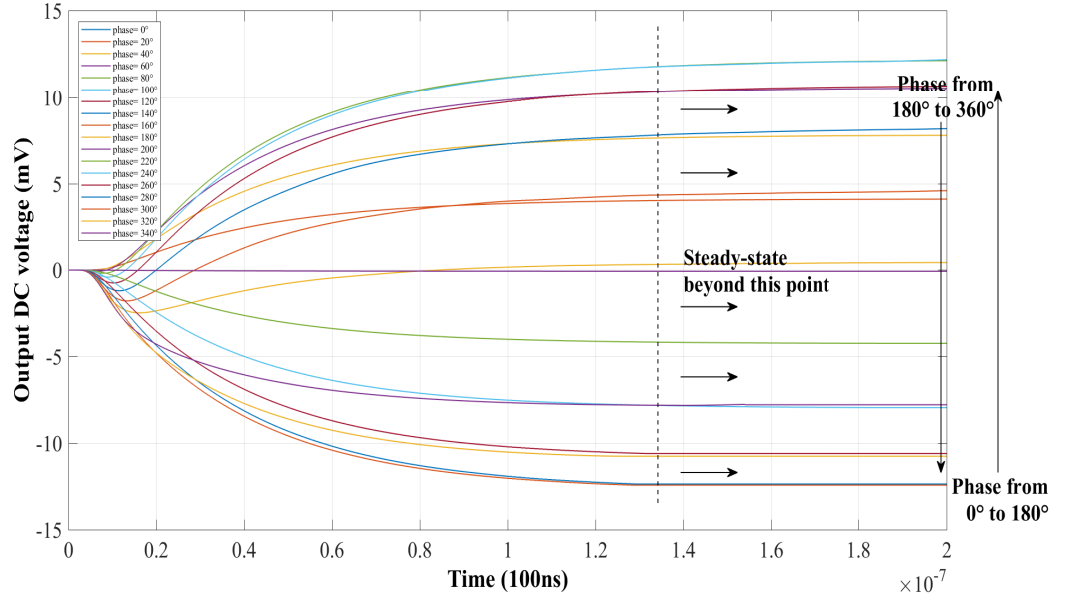


Figure 7.1: Overall system pre-layout phase conversion into a map of DC output voltages. The figure shows the conversion into DC output voltage reaches steady-state at 130ns which is fast enough for multi-sampling and confident measurement of events.

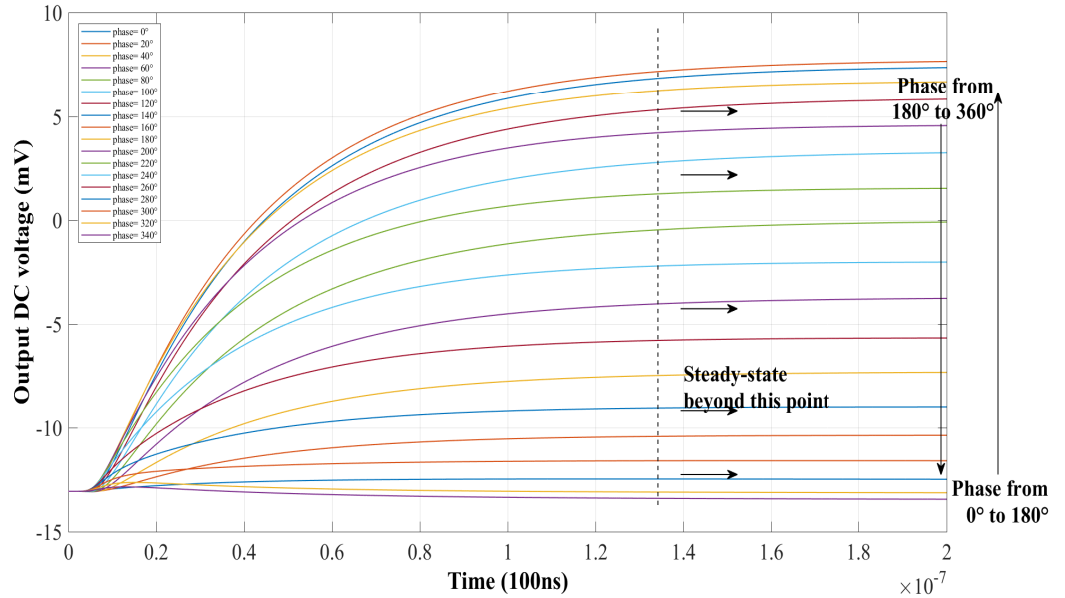


Figure 7.2: Overall system post-layout phase conversion into a map of DC output voltages. Similar to the pre-lay result, the figure shows the conversion into DC output voltage reaches steady-state at 130ns which is also fast enough for multi-sampling and confident measurement of events.

7.2 First RF Sensor Prototype Results and Analysis

The first remote RF sensor prototype was designed and fabricated in accordance with the 500nm CMOS technology. This first realization of the circuit design is essentially similar in terms of module structure and design flow compared to the later version realization in the 180nm CMOS technology, albeit with a few noticeable differences. For example, the first prototype did not include any on-chip inductors due to the ineligible fabrication of on-chip spiral inductors by the vendor's requirement for the specific 500nm CMOS technology used. Alternatively, off-chip inductors were adapted. The other difference was the presence of a phase-locked loop in the 500nm version for analog signal demodulation since originally the sensor was required to process demodulation of the received RF signal on top of RF directional sensing. That option was removed in the latest prototype fabricated in the 180nm CMOS technology, to solely focus the system capability to the AoA sensing.

Fig. 7.3 is the scanning electron microscope (SEM) view of the first prototype chip. The chip is in an area of 1.5 mm x 1.5 mm chip at the center, wirebonding shown to the I/O pads of the DIP40 package and the chip. Fig. 7.4 displays a top-down view of the chip. The circuit chip, in 1.5mm x 1.5mm dimensions, largely consists of two pairs of the GCMs, LNAs, low-pass filters, and the phase-locked loop circuit for demodulation and the AoA structure.

The experimental testing of the first prototype chip focused on demonstration of the mixing functionality of the GCM modules which was accomplished by observing a multiplication function. Starting from a 10MHz RF input, the maximum

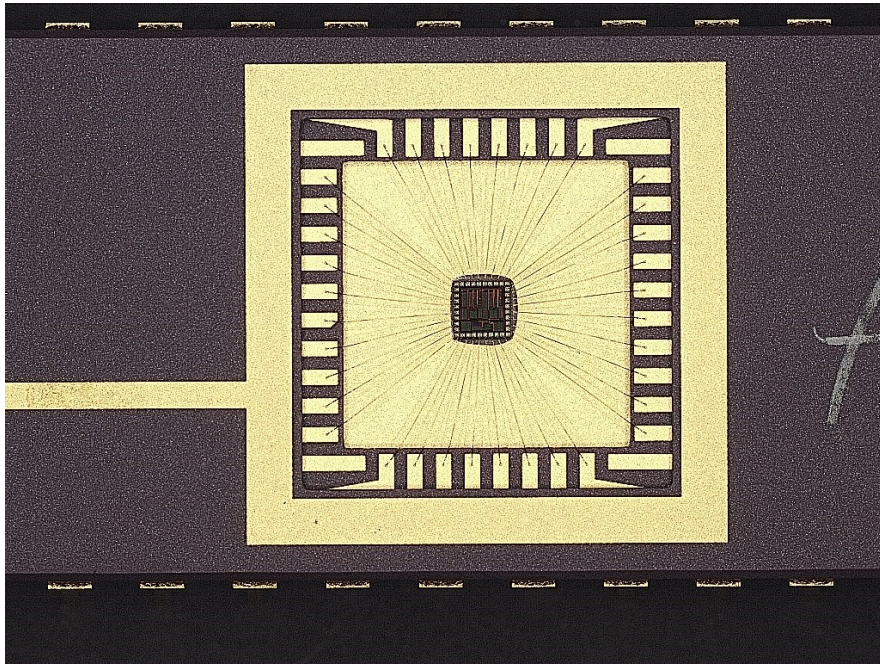


Figure 7.3: The first prototype chip in SEM view which shows the chip at the center, wirebonding shown to the I/O pads of the DIP40 package and the chip.

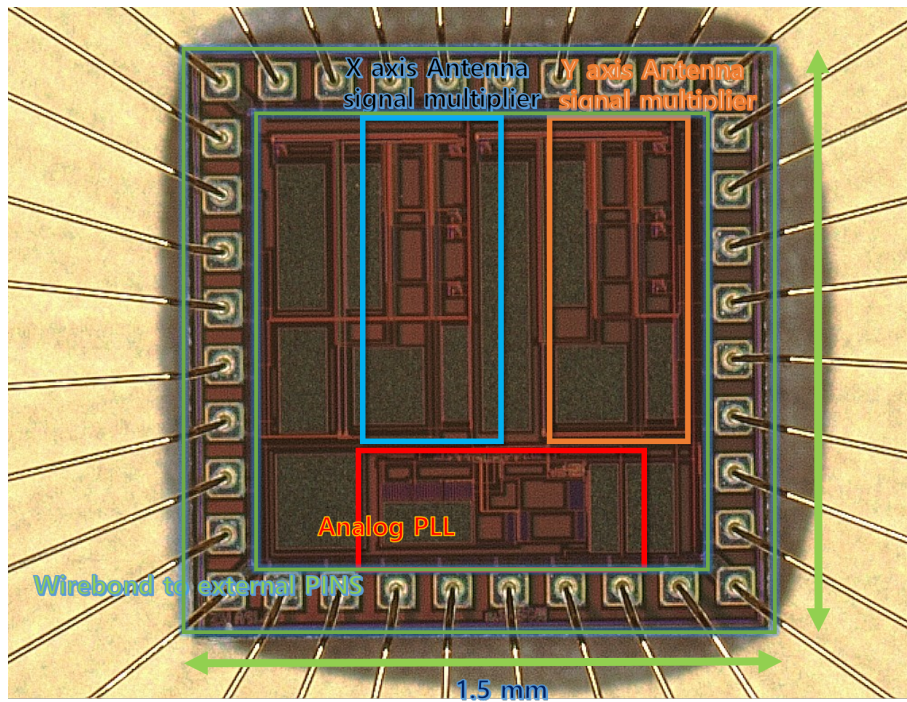


Figure 7.4: The top-down view of the first prototype chip. The chip, in $1.5\text{ mm} \times 1.5\text{ mm}$ dimensions, consists of two pairs of the GCMs, LNAs, low-pass filters, and the phase-locked look circuit.

frequency range of the chip was tested by increasing the RF input frequency, to define its maximum bandwidth. This procedure was preceded by another experiment to define the threshold LO power that shows multiplication operation because the RF input maximum bandwidth can only be defined once the operation of the LO transistors switching is guaranteed. The outputs were measured by a spectrum analyzer that represented a magnitude in the dBm scale equivalent to the power ratio in decibels of the measured power relative to 1mW.

First, the threshold LO power experiment validated threshold multiplication response at the LO power of -35 dBm, which is equivalent to $0.316\mu W$ in $50\ \Omega$ input impedance. To accomplish proper mixing, a sufficient level of input common mode voltage bias setting was required to place the LO transistors right around $V_{ov} = 0$. Since the source node of the LO transistors was passively determined, the turn-on bias that is, the LO transistor gate bias voltage was found at $V_{LO,bias} = 1052\text{ mV}$ at the RF input frequency of $f_{RF} = 10\text{MHz}$, by manually sweeping the voltage until the $f_1 + f_2$, and $f_1 - f_2$ signal terms appear in the spectrum analyzer.

Second, the RF input maximum bandwidth was tested by varying the RF input frequency from 10MHz to 50MHz in 10 MHz steps at the LO frequency which was fixed at 4.3MHz for the testing. The RF signal was directly fed to the sensor input. External components such as BNCs, coupling capacitors and off-chip inductors were placed on the breadboard to solely test the chip operation, despite increased parasitic effects and noise. The data in Table 7.1 represent the down and up conversion power measurement along the RF input frequency variation at the RF power at -45 dBm. The mixing performance is shown to be solid below $f_{RF} = 40\text{MHz}$, and

sharp output power decreases above 40MHz. The spurious signals, $m * f_1 \pm n * f_2$ as a result of the harmonics of the f_1 and f_2 signals, are mixed together and these mixed signals are repeatedly mixed with others creating even further spurious signals as shown by the spectrum analyzer in Fig. 7.5(a) and 7.5(b). As predicted, the third-order terms $2f_1 \pm f_2$ and $f_1 \pm 2f_2$ among all the spurious signals increased faster than the target output, $f_1 - f_2$, $f_1 + f_2$ increases with increasing input power. Eventually the third-order intermodulation distortion (IMD3) surpassed the original output power when the RF input signal reached above ~ -10 dBm. These third-order intermodulation distortion IMD3 proved to be the main source of spurious signals/noise, and were particularly difficult to filter out since it was close to the targeted signal frequency. This signal proximity due to IMD3 was the main reason for developing the g_{m3} cancellation technique to compensate and suppress IMD3, for increased linearity in the 180nm CMOS technology prototype. The test results validated mixing functionality of the chip for the the proof of concept, demonstrating operation up to $f_{RF} = 50$ MHz, providing a platform for further optimization and higher frequency ranges.

0	$f_1 - f_2$ (dBm)	$f_1 + f_2$ (dBm)
10MHz	-26.83	-24.79
17MHz	-29.76	-23.86
20MHz	-29.06	-27.79
30MHz	-24.30	-36.18
40MHz	-31.51	-27.13
50MHz	-46.29	-48.98

Table 7.1: The down and up-converted output responses with respect to the RF input frequency varied from 10MHz to 50MHz for the first prototype chip.



Figure 7.5: (a) Spectrum analyzer view for the mixer's output at $f_{RF}=40\text{MHz}$, $f_{LO}=4.3\text{MHz}$. (on left)
(b) Spectrum analyzer view for the mixer's output at $f_{RF}=50\text{MHz}$, $f_{LO}=4.3\text{MHz}$. (on right)

The 500nm prototype showed limited potential in comparison to the latest 180nm CMOS prototype which also provided better libraries for on-chip inductors, RF NMOS, PMOS, polysilicon resistors, allowing a more flexible and complete design. Furthermore, the first prototype had non-optimal sized devices, failing to properly bias the RF and the LO transistors, contributed to less effective operation of the sensor with higher noise, gain attenuation, and lower linearity. The 180nm CMOS technology showed obvious advantages in terms of minimum transistor length because a smaller minimum MOSFET length affects faster operating speed, although it has limits with lower intrinsic gain. The minimum length of 180nm was chosen for transistors to improve operation speed for such reasons.

7.3 Conclusions

The development, design, modeling, and evaluation of an RF sensor IC chip for remote RF directional tracking has shown that the IC design approach using

the guidelines developed in this work based on the novel combined optimization methodology for optimizing RF sensor for AoA detection, resulted in significant improvements in the performance of the sensor. The design approach using novel low noise amplifiers, BALUNs and Gilbert cell mixers, provided the basic elements for enhanced on-chip sensing. The sensor effectively converted the phase difference from the incident signals into a map of output voltages suitable for an 18 bit ADC readout. The method developed here is highly accurate and provides effective guidelines to optimize chip design. The phase difference conversion to the output voltage map reaches a steady-state condition for measurement at 130 ns which allows for a fast multi-sampling approach to enhance confidence and accuracy of the measurement. The design of the low noise amplifier was developed based on the g_m/I_D parametric optimization and g_{m3} suppression techniques. The BALUNs were implemented with the cascode common-source, common-gate amplifiers combinational design. The Gilbert cell mixers were developed with the g_m/I_D parametric optimization, inductive resonance, and current bleeding techniques and optimization of DC operation points of the LO transistors that resulted in a dramatic reduction of flicker noise and high balancing linearity. The LNA showed high linearity at IIP3 = 5.84 dBm, NF = 2.97 dB, and a good gain at S_{21} = 15.3 dB. The LO BALUN circuit showed greatly matching cascode CG and CS amplifier outputs in the opposite polarity with less than a 5% difference in magnitude and NF = 3.83 dB. The GCM showed excellent NF = 15.07 dB @ f = 1 kHz, high linearity IIP3 of 5.85 dBm, conversion gain of 4.29 dB at the RF input power of 30 dBm. Both the LNA and the GCM showed excellent linearity and low noise levels through the optimization

process presented here. A system level post-layout evaluation provided the conversion of the phase difference into an output voltage map for accurate $\angle$ AoA sensing. From the post-layout evaluation, the upper limit of AoA detection error of 3.447° was determined[\[15\]](#).

7.4 Future Work

The dissertation work demonstrates the robustness of the AoA sensing and provides a solid theoretical background for the CMOS Process Design Kit (PDK) based prototype chip development. In future work, the calibration data of the chip in the actual RF environments would provide further validation of the remote RF sensor. The combined optimization methodology developed here can be applied to develop high performance sensor chips for different applications at different frequencies, such as biosensors, and biomedical devices.

7.5 Publication Record

7.5.1 Referred Journal Articles

- **J. Chung** and A. A. Iliadis. Design and Optimization of a CMOS IC Novel RF Tracking Sensor. International Journal of Circuit Theory and Applications 49.3 (2021): 801-819.

7.5.2 Referred Articles in Press

- **J. Chung** and A. A. Iliadis. (accepted, in press) Novel Approaches and Methods for Optimizing Highly Sensitive Low Noise Amplifier Design Strategy for Congested RF Environments. TechConnect Briefs (2021).

7.5.3 Referred Conference Proceedings

- **J. Chung** and A. A. Iliadis, "Modeling a High Linearity, Low Noise Gilbert Cell Mixer using Three Optimization Techniques," 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA, 2020, pp. 790-793, doi: 10.1109/MWSCAS48704.2020.9184485.

Bibliography

- [1] High frequency ceramic solutions, 2.4 ghz surface mount, above metal, low profile mini chip antenna. Technical report, Johanson Technology, 2017.
- [2] Z. Albataineh, J. Moheidat, and Y. Hamada. Design of high gain 2.4GHz CMOS LNA amplifier for wireless sensor network applications. In *Proc. 10th Jordanian Int. Electrical and Electronics Engineering Conf. (JIEEEEC)*, pages 1–5, 2017.
- [3] D. J. Allstot, Xiaoyong Li, and S. Shekhar. Design considerations for CMOS low-noise amplifiers. In *Proc. IEE Radio Frequency Integrated Circuits (RFIC) Systems. Digest of Papers*, pages 97–100, 2004.
- [4] and Yang-Chaun Chen and Chien-Nan Kuo. A 6-10-GHz ultra-wideband tunable LNA. In *Proc. IEEE Int. Symp. Circuits and Systems*, pages 5099–5102 Vol. 5, 2005.
- [5] Meysam Asghari and Mohammad Yavari. Using the gatebulk interaction and a fundamental current injection to attenuate im3 and im2 currents in rf transconductors. 24:223–232, 2016.
- [6] Anishaziela Azizan, S. A. Z. Murad, R. C. Ismail, and M. N. M. Yasin. A review of lna topologies for wireless applications, 2014.
- [7] CMOS Baker and CMOS Boyce. circuit design, layout, and simulation, 2010.
- [8] A. Bevilacqua and A. M. Niknejad. An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers. *IEEE Journal of Solid-State Circuits*, 39(12):2259–2268, 2004.
- [9] O. Bock, C. Thom, M. Kasser, and J.R. Pelon. Multilateration with the wide-angle laser ranging system: ranging performance and first ground-based validation experiment. 37:739–747, 1999.
- [10] Ji Chen and Juin J. Liou. Modeling of on-chip differential inductors and transformers/baluns. *IEEE Transactions on Electron Devices*, 54(2):369–371, February 2007.

- [11] Xiaolong Chen, Baoxin Chen, Jian Guan, Yong Huang, and You He. Space-range-doppler focus-based low-observable moving target detection using frequency diverse array MIMO radar. *IEEE Access*, 6:43892–43904, 2018.
- [12] J. Chung and A. A. Iliadis. Modeling a high linearity, low noise gilbert cell mixer using three optimization techniques. In *Proc. IEEE 63rd Int. Midwest Symp. Circuits and Systems (MWSCAS)*, pages 790–793, 2020.
- [13] Jooik Chung and Agis Iliadis. Novel approaches and methods for optimizing highly sensitive low noise amplifier design strategy for congested rf environments (accepted, in press). *TechConnect Briefs*, 2021.
- [14] Jooik Chung and Agis A. Iliadis. Modeling a high linearity, low noise gilbert cell mixer using three optimization techniques, 2020.
- [15] Jooik Chung and Agis A. Iliadis. Design and optimization of a cmos ic novel rf tracking sensor. 49:801–819, 2021.
- [16] J. Dang, P. Sakalas, A. Noculak, M. Hinz, and B. Meinerzhagen. A k-band high gain, low noise figure LNA using 0.13 m logic CMOS technology. In *Proc. 10th European Microwave Integrated Circuits Conf. (EuMIC)*, pages 120–123, 2015.
- [17] Tim Das. Practical considerations for low noise amplifier design. Technical report, Freescale Semiconductor, 2013.
- [18] Glenn F. Engen and Cletus A. Hoer. Application of an arbitrary 6-port junction to power-measurement problems. 21:470–474, 1972.
- [19] Salim El Ghouli, Wladyslaw Grabinski, Jean-Michel Sallese, Andre Juge, and Christophe Lallement. Analog RF and mm-wave design tradeoff in UTBB FDSOI: application to a 35 ghz LNA. In *25th International Conference "Mixed Design of Integrated Circuits and System", MIXDES 2018, Gdynia, Poland, June 21-23, 2018*, pages 57–62. IEEE, 2018.
- [20] S. K. Hampel, O. Schmitz, Marc Tiebout, and Ilona Rolfes. Wideband inductorless minimal area RF front-end. In *35th European Solid-State Circuits Conference, ESSCIRC 2009, Athens, Greece, 14-18 September 2009*, pages 96–99. IEEE, 2009.
- [21] Siti Zuraidah Ibrahim, Mohammad Shahrazel Razalli, Wee Fwen Hoon, and Mohd Nazri A. Karim. Six-port interferometer for direction-of-arrival detection system. pages 1–4. IEEE, 2016.
- [22] Agis A. Iliadis and Kye-chong Kim. Theoretical foundation for upsets in cmos circuits due to high-power electromagnetic interference. 10:347–352, 2010.
- [23] Nikita Ivanov and Alexander S. Korotkov. Comparative analysis of rc- and rlc-complex filters for microwave microelectronic phaseshifters, 2016.

- [24] J. Jussila and P. Sivonen. A 1.2-V highly linear balanced noise-cancelling LNA in 0.13- μm CMOS. *IEEE Journal of Solid-State Circuits*, 43(3):579–587, 2008.
- [25] Sanghoon Kang, Byounggi Choi, and Bumman Kim. Linearity analysis of cmos for rf application. *IEEE Transactions on Microwave Theory Techniques*, 51(3):972–977, March 2003.
- [26] H. Kilicasian, Hong-Sun Kim, and M. Ismail. A 1.9 ghz cmos rf down-conversion mixer.
- [27] Sinyoung Kim and Kuduck Kwon. A 50-mhz1-ghz 2.3-db nf noise-cancelling balun-lna employing a modified current-bleeding technique and balanced loads. 66:546–554, 2019.
- [28] Alexander Koelpin, Fabian Lurz, Sarah Linz, Sebastian Mann, Christoph Will, and Stefan Lindner. Six-port based interferometry for precise radar and sensing applications. *Sensors*, 16(10):1556, 2016.
- [29] John D. Kraus and Alan T. Moffet. Radio astronomy. 35:450–450, 1967.
- [30] Benjamin Laemmle, Gabor Vinci, Linus Maurer, Robert Weigel, and Alexander Koelpin. A 77-ghz sige integrated six-port receiver front-end for angle-of-arrival detection. 47:1966–1973, 2012.
- [31] Xiayong Li. *Low Noise Design Tehchniques for Radio Frequency Integrated Circuits*. PhD thesis, University of Washington, 2004.
- [32] Y. Lin, C. Wang, G. Lee, and C. Chen. High-performance wideband low-noise amplifier using enhanced π -match input network. *IEEE Microwave and Wireless Components Letters*, 24(3):200–202, 2014.
- [33] Michael Angelo G. Lorenzo and Maria Theresa G. de Leon. Comparison of lna topologies for wimax applications in a standard 90-nm cmos process, 2010.
- [34] Ehsan Morad, Ehsan Rasouli, and Maryam Alasvandi. High linearity common gate gilbert cell mixer design using cmos 0.18 μm technology for 2.4 ghz applications. *Electrical and Electronic Engineering*, 4(3):52–57, 2014.
- [35] MOSIS. Package handbook, dip40. Technical report, University of Southern California, 1993.
- [36] Kumar Munusamy and Zubaida Yusoff. A highly linear cmos down conversion double balanced mixer, 2006.
- [37] Domenico Pepe, Ilias Chlis, and Domenico Zito. 67ghz three-spiral transformer cmos oscillator. 44:1798–1813, 2016.

- [38] G. Piccinni, G. Avitabile, G. Coviello, and C. Talarico. Gilbert cell mixer design based on a novel systematic approach for nanoscale technologies. In *Proc. IEEE 18th Wireless and Microwave Technology Conf. (WAMICON)*, pages 1–4, April 2017.
- [39] G. Piccinni, G. Avitabile, G. Coviello, and C. Talarico. A novel optimization framework for the design of gilbert cell mixers. In *Proc. IEEE 60th Int. Midwest Symp. Circuits and Systems (MWSCAS)*, pages 1418–1421, 2017.
- [40] S. L. Pinjare, G. Nithya, V. S. Nagaraja, and A. Sthuthi. A gm/id based methodology for designing common source amplifier. In *Proc. 2nd Int. Conf. Micro-Electronics and Telecommunication Engineering (ICMETE)*, pages 304–307, 2018.
- [41] Hong Qi, Chen Junning, Pan Hao, and Meng Jian. A 1.2v high linearity mixer design, 2007.
- [42] H. Rashtian, A. H. Masnadi Shirazi, and S. Mirabbasi. Improving linearity of CMOS gilbert-cell mixers using body biasing. In *Proc. IEEE 55th Int. Midwest Symp. Circuits and Systems (MWSCAS)*, pages 61–64, 2012.
- [43] B. Razavi. Rf ic design challenges.
- [44] Behzad Razavi. *Design of analog CMOS integrated circuits*. McGraw-Hill series in electrical and computer engineering. McGraw-Hill, Boston Burr Ridge, IL, 2001. Includes bibliographical references and index.
- [45] Behzad Razavi. *RF microelectronics*. The @Prentice Hall communications engineering and emerging technologies series. Prentice Hall, Upper Saddle River, NJ [u.a.], 2. ed. edition, 2012. Includes bibliographical references and index.
- [46] rfdh.com. Understanding imd, p1db, ip3. Technical report, RF Design House, 2000.
- [47] Shasanka Sekhar Rout and Kabiraj Sethi. Design of high gain and low noise cmos gilbert cell mixer for receiver front end design. In *2016 International Conference on Information Technology (ICIT)*, pages 1–5. IEEE, 2016.
- [48] Meriem Salhi and Nouredine Boudriga. Multi-array spherical LIDAR system for drone detection. In *22nd International Conference on Transparent Optical Networks, ICTON 2020, Bari, Italy, July 19-23, 2020*, pages 1–5. IEEE, 2020.
- [49] Derek K Shaeffer and Thomas H Lee. A 1.5-v, 1.5-ghz cmos low noise amplifier. *IEEE Journal of solid-state circuits*, 32(5):745–759, 1997.
- [50] Rahul Sharma, , Abhay Chaturvedi, Manish Kumar, and and. A comparative study of different types of mixer topologies. 2:182–187, 2016.

- [51] Pokuri Sravanthi and Aniruddha Chandra. Current-bleeding folded gilbert rf mixer design for wireless applications, 2013.
- [52]  Sz, Rudolf Seller, D Roh, and P Renner. Multilateration based uav detection and localization. In *2017 18th International Radar Symposium (IRS)*, pages 1–10. IEEE, 2017.
- [53] Serioja Ovidiu Tatu, Adriana Serban, Mohamed Helaoui, and Alexander Koelpin. Multiport technology: The new rise of an old concept. 15:S34–S44, 2014.
- [54] Gabor Vinci, Francesco Barbon, Robert Weigel, and Alexander Koelpin. A high accuracy direction-of-arrival and misalignment angle detector. In *2011 German Microwave Conference*, pages 1–3. IEEE, 2011.
- [55] Gabor Vinci, Alexander Koelpin, Francesco Barbon, and Robert Weigel. Six-port-based direction-of-arrival detection system. In *2010 Asia-Pacific Microwave Conference*, pages 1817–1820. IEEE, 2010.
- [56] Hung-Che Wei, Chih-Lung Hsiao, and Ro-Min Weng. A broadband low power high isolation double-balanced subharmonic mixer for 4g applications. *Progress In Electromagnetics Research*, 138:143–155, 2013.
- [57] Yen-Liang Yeh and Hong-Yeh Chang. Linearity enhancement of cmos device using a modified third-order transconductance cancellation technique for microwave amplifier. In *2011 IEEE MTT-S International Microwave Symposium*, pages 1–4. IEEE, 2011.
- [58] Lv Zhao and Chunhua Wang. A linearized and low noise cmos mixer with b-type amplifier-based sub-harmonic balun. *International Journal of Circuit Theory and Applications*, 44(11):2003–2017, 2016.