

ABSTRACT

Title of Thesis: **DESIGN OF PIXEL LEVEL CMOS
READOUT CIRCUITRY FOR
CONTINUOUS BIAS UNCOOLED
BOLOMETRIC LONG WAVE INFRARED
FOCAL PLANE ARRAYS**

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2004**

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Modern IC foundries do not provide large analog storage capacitors. This limits the charge storage capacity for modern uncooled long wave infrared readout circuits. A long integration time in the pixel helps to extend the effective charge storage capacity, reduces the temporal noise, and subsequently reduces the noise bandwidth of the pixel. Modern infrared readout arrays that employ *current skimming*, a technique which extends the integration time, usually do so at the end of a row or column in the readout array. This thesis research describes an advanced concept of a *per-pixel skimming* readout approach by incorporating the skimming function inside the pixel. DC pedestal removal techniques such as current skimming allow the pixels to integrate longer by subtracting the DC bias signal. However, a low output conductance current sink is needed to subtract the DC pedestal. This thesis

explores the use of cascode circuitry to decrease output conductance. Current
skimming alternatives for increasing the integration time in the pixel while
maintaining a low output conductance sink for continuously biased uncooled long
wave infrared arrays are presented.

DESIGN OF PIXEL LEVEL CMOS READOUT CIRCUITRY FOR CONTINUOUS
BIAS UNCOOLED BOLOMETRIC LONG WAVE INFRARED FOCAL PLANE
ARRAYS

By

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Preface

Thesis Contributions:

- Design of long wave infrared current skimming readout circuits for DC pedestal removal in continuously biased uncooled bolometer focal plane arrays
- Successfully developed and tested appropriate scaling techniques for self-biased cascode transistors operating in the subthreshold state
- Achieved greater than 8 ms integration time in one of the first reported per-pixel current skimming readout approaches designed and intended for continuous bias uncooled infrared focal plane arrays

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Chapter 1: Introduction

Motivation for DC pedestal removal

The chief motivations for current skimming are to reduce the overall temporal noise (noise which varies in time) by enabling longer integration times and to enhance dynamic range for signals of interest. Though analyzing the temporal noise is not the focus of this thesis, this gives a fundamental justification for removing the DC bias pedestal and integrating the signal of interest. The DC bias pedestal for the uncooled bolometer sensor contains no useful scene information for signal processing (Appendix A) and must be removed, thus a low output conductance current sink (n-channel transistor) must be designed to subtract or *skim* off the DC signal.

Furthermore, reducing the temporal noise will help improve the signal-to-noise ratio (maximum integrated signal divided by the temporal noise floor) in the pixel. Concurrently, decreasing temporal noise reduces the integrated noise bandwidth during a given frame time. Integration time is usually smaller in high background (long wave infrared) applications¹ due to the finite integration capacitances and operating voltages. Commonly used input circuits to perform signal processing in the long wave infrared are called injection circuits (e.g. *direct injection*) as seen in Figure 1.1. I_{det} in Figure 1.1 represents the injected detector (Appendix A) current through the channel of the $M_{\text{direct_injection}}$ transistor. Typical integration times for the direct injection circuit discussed for this thesis are approximately 45 μs - 300 μs without the current skimming function in

¹ High backgrounds refer to a spectral region where the amount of photon flux present on the detector is very large. For example, the long wave infrared (8 μm – 14 μm) is considered to have the largest photon background concentration in the infrared spectrum. There are approximately 10^{16} photons/cm²/s in the long wave IR that transmit through the atmosphere in the above mentioned pass-band. Most readout integration times are consequently limited by such high levels of photon flux, thus leading to shorter integration times by saturating the integration capacitor relatively quickly.

the pixel. Employing a current skimming sink in this thesis allows the pixel to integrate up to approximately 10 ms (one third of a frame time for 30 Hz operation). Goals of this research are to design and test approaches to implement a low output conductance current sink to efficiently subtract or “skim” the DC bias pedestal. The following section gives a brief description of the direct injection input transistor used in long wave infrared signal processing.

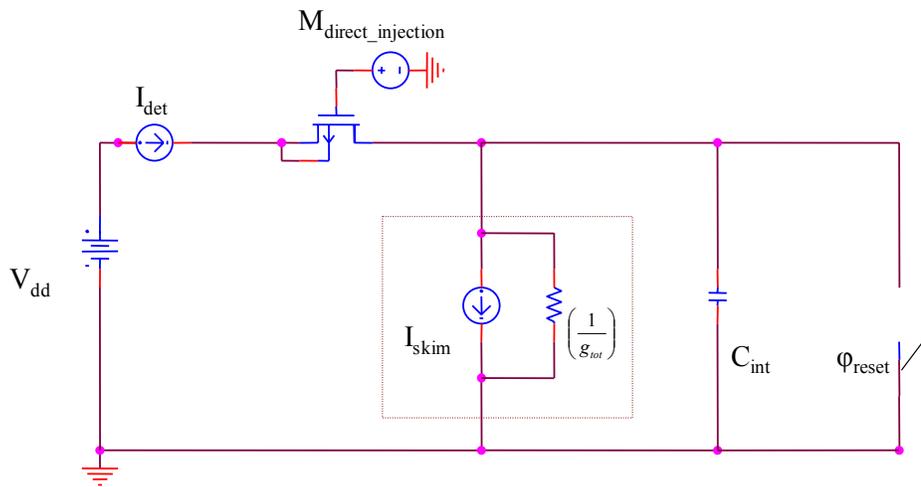


Figure 1.1: A direct injection pixel with a basic current sink model

Description of Direct Injection

Injection circuits perform current-to-voltage signal conversion (integration) through the channel of an active transistor onto a capacitive storage element. The gain of the input circuit or otherwise known as the pre-amplifier is set by the integration capacitor [1]. A feature of the direct injection input circuit is that it requires minimal area; usually a direct injection, reset, and a source follower transistor are used for biasing the output signal in voltage mode operation [1].

The direct injection approach in this thesis is a common gate (p-channel) amplifier (or current buffer) whereby the input signal is sensed at the source and outputs the signal at the drain. The gate is connected to a voltage bias which sets a proper DC bias operating point [2]. An important criteria for the direct injection transistor as seen in Figure 1.1 is to maintain DC bias stability on the gate to minimize injection transistor noise as a result of fluctuations in long wave photon irradiance (causing resistive changes in the bolometer (Appendix A)). The source or sense node of the direct injection transistor should provide a low input impedance $\left(\frac{1}{g_m}\right)$ path to ensure the signal is injected efficiently through the active channel of the direct injection transistor. Since the current signals of the detector have a very small magnitude (Appendix A), the injection transistor is biased in the subthreshold state (weak inversion) which makes the transistor transconductance, g_m , relatively small [3].

Current Skimming

Without any skimming circuitry in the pixel, the voltage for a given maximum change on the integration capacitor is shown in (1.1) where the DC bias detector (input) current is given by I_{det} , integration capacitor (C_{int}), integration time (τ_{int}), and the current signal of interest (ΔI_{det}). As mentioned above, the basic pixel topology in Figure 1.1 is considered a *current integrator* which converts integrated current to a voltage signal across the terminals of the storage capacitor. The boxed in region is a simple small signal circuit model of the current skimming transistor. The parallel resistor $\left(\frac{1}{g_{tot}}\right)$ represents the inverse of the total output conductance of the current skimming device. By saturating

the skimming transistor's drain, this provides a relatively low input impedance path to subtract the injected DC current from $M_{\text{direct_injection}}$. In parallel with the integration capacitor is the reset switch (ϕ_{reset}). With the reset switch function, the pixel performs a classical ramp, sample, and transfer of signal through a voltage buffer (source follower) at the pixel output (voltage buffer is not shown in Figure 1.1). The signal readout for an integration and reset approach is essentially a *destructive process*, which means the signal charge is lost during readout (as opposed to a non-destructive readout in which the pixel is not automatically reset upon readout).

$$\Delta V = \frac{(I_{\text{det}} + \Delta I_{\text{det}}) \times \tau_{\text{int}}}{C_{\text{int}}} \quad (1.1)$$

Equation (1.2) includes the skimming current which is a larger fraction of the total current contributed by the important small signal current changes (ΔI_{det}) in the bolometer (detector sensing element) related to temperature variations in the observed scene (refer to Appendix A for a detailed discussion on the uncooled sensing mechanism; the bolometer).

$$\Delta V = \frac{(I_{\text{det}} + \Delta I_{\text{det}} - I_{\text{skim}}) \times \tau_{\text{int}}}{C_{\text{int}}} \quad (1.2)$$

Equation (1.3) assumes if some fraction of the DC bias current, I_{det} , (ideally 100 %) is subtracted or *skimmed* off then we can integrate the current signal of interest, ΔI_{det} , for a much longer time without saturating the integration capacitor. Since a significant portion of the integration current is subtracted, the value of C_{int} can essentially be decreased (for subsequent future designs) without saturating it (a reduction in the value of C_{int} leads to smaller pixels). As a result, sensitivity is increased since the same integration current produces a larger voltage swing on a much smaller capacitance.

$$\tau_{\text{int}} = \frac{\Delta V \times C_{\text{int}}}{\Delta I_{\text{det}}} \quad (1.3)$$

Chapter 1 has briefly outlined the problem and justification for the DC pedestal removal in uncooled long wave infrared readout circuits. A broad solution was formulated; a low output conductance current sink is needed to skim off the DC pedestal in order to integrate the current signal of interest (e.g. the signal which contains relevant scene or signal processing information). Chapter 1 also gave a brief description of the preferred input readout circuit in the long wave infrared; the direct injection transistor. The interested reader is referred to Appendix A to gain a more detailed understanding on the detector and its operational mechanics studied in this thesis.

Chapter 2: Readout System Design

This chapter gives the reader a brief look at the pixel and system level readout electronics. The first section describes two readout methods, voltage and charge readout, used in today's infrared imaging systems. The method employed in this thesis is the voltage mode readout using an output source follower transistor. The direct injection pixel is considered the optimum architecture employed in long wave infrared readout applications [3]. Concluding Chapter 2, we briefly discuss the differences between readout modes, rolling and snapshot.

Readout Systems

Imaging systems employ readout circuits that process and convert the scene signal to an electrical signal that represents the observed scene over a fixed integration period or frame. The primary functions of the readout are to provide pre-amplification (*at the pixel level*), gain (*in the column amplifier*), offset correction (the signal of each pixel is measured with respect to a value that represents the pixel's response to a given reference input signal), multiplexing of the column outputs, and finally video amplification for the final image display or storage to some memory element for subsequent signal processing. Figure 2.1 shows an example of a typical single readout signal path from pre-amplification to video output. The primary design driver for readout electronics is signal-to-noise ratio. Design trade-offs include detector temperature, readout pixel area, and power dissipation. Other performance drivers are dynamic range, linearity, and operability [1].

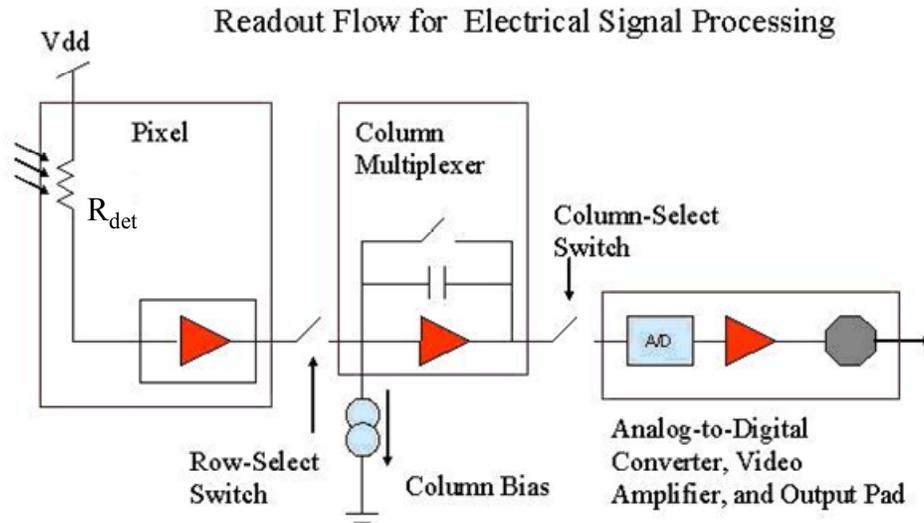


Figure 2.1: Readout system electronics

Two methods of pixel readout are *voltage* and *charge* mode output. The first method usually converts current to voltage through integration on a capacitor and buffers the voltage signal with a *source follower*. Doping concentration of the source and drain diffusions as well as the substrate and oxide thicknesses determine the source follower gain. The source follower (*small signal*) intrinsic voltage gain $A_v = \left(\frac{g_m}{g_{ds}} \right)$ determines the signal level transferred to the output. The current-to-voltage conversion is performed by a *common gate current amplifier* and integration capacitor. This circuit is commonly referred to as *direct injection readout* as mentioned in Chapter 1.

For voltage mode output, the source follower in Figure 2.2 usually operates above the threshold voltage (*in saturation*). An immediate drawback of using a source follower is the *body effect or back-gate effect*. The body effect causes the threshold voltage to rise and reduces gate overdrive, which translates to decreased source follower gain and loss of the integration signal.

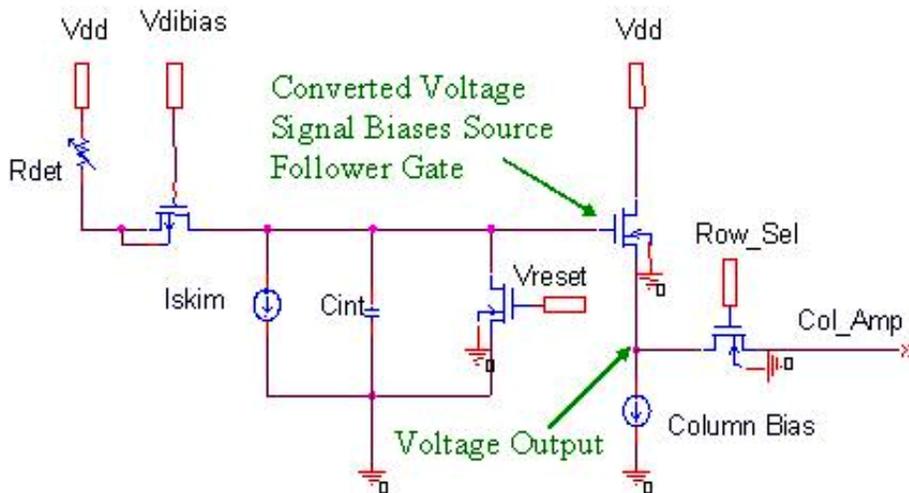


Figure 2.2: Direct injection pixel in voltage mode readout

Using a p-channel source follower can eliminate this problem by *connecting the well and source* at the expense of increased capacitance at the output node. Also, because bulk carrier mobility is lower in p-channel transistors compared to n-channel transistors, a smaller amount of input (*summed at the gate*) referred noise is introduced into the signal path. A note to the reader, the column bias is not in every pixel but rather biases all the source followers for a particular column. Not displayed in Figure 2.2 is the column switch which passes the accumulated signal to the column integrator for amplification. Both the row and column switches do not lie in the pixel. Another method of readout is to operate in *charge mode*, as shown in Figure 2.3. This architecture is chosen to; 1) minimize power consumption by eliminating the source follower; 2) lower noise; and 3) decrease pixel area. In charge-mode readout, when the row select switches are open and closed, the integration capacitors are exposed to the column capacitance where charge

sharing occurs, thus a decreased voltage swing results; hence the voltage mode achieves a higher dynamic range than the charge mode readout.

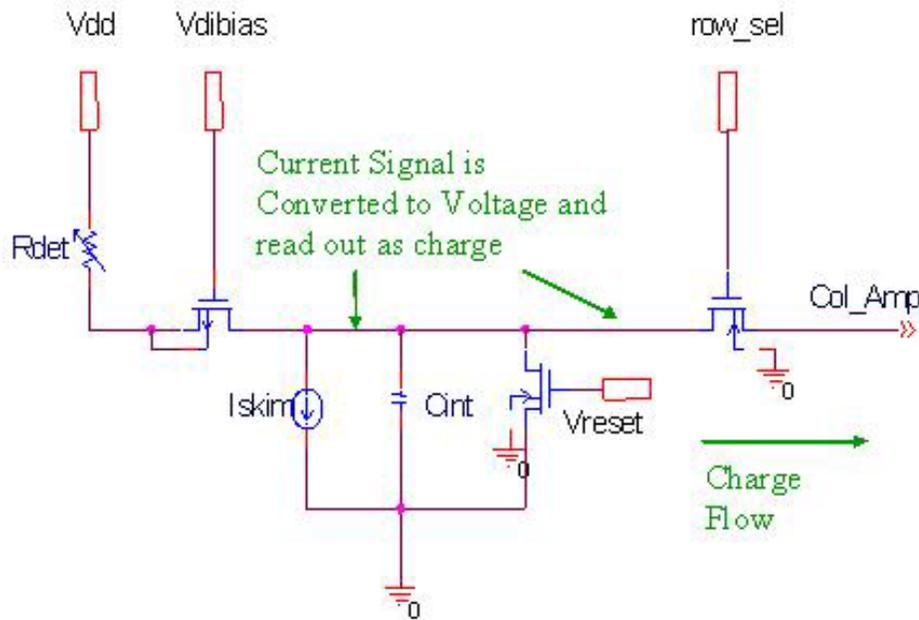


Figure 2.3: Direct injection pixel in charge mode readout

We have briefly discussed the system architecture and will now explain the two modes of the readout process, *rolling and snapshot*. Rolling mode or *integrate-while-read* mode is a sequential and continuous readout where the system software clocks the first row to be read then moves on to the next row. Simultaneously, the columns are read in parallel. As the clock software cycles to a new row for readout, the previous row has begun to integrate again. This method reads one row at a time, and integration is staggered over the frame for individual rows. There is usually no delay time between consecutive frames. In this mode, the pixels do not integrate simultaneously. Rolling mode is useful for short integration times and large photon irradiance conditions.

Snapshot mode or *integrate-then-read* is where all pixels integrate simultaneously

and is then read out. Essentially, each row integrates in parallel and then is readout after all the pixels have integrated simultaneously. Snapshot is useful for long integration times with relatively low background photon irradiance conditions. Snapshot is also useful in obtaining the fastest pixel response since reading in this mode is not limited to the frame readout period as is the case in integrate-while-read or rolling mode. Usually the integration capacitor lies between a sample and hold-switch and a row-select switch. This approach holds the value until the row-select switch is high. Once integration is complete, the system software clocks the row select switch and the charge is transferred out of the pixels to the column integrators. Since snapshot mode is a simultaneous readout, the pixel must require a hold capacitor and more sophisticated clocking electronics [4].

In summary, this chapter has presented the fundamentals of some typical readout architectures. We have shown the path from pre-amplification of the integrated signal to video output. This chapter described two methods of signal readout, *voltage* and *charge mode*. Finally we discussed two operating modes of the readout process, *rolling* and *snapshot*.

Chapter 3: DC pedestal removal in the Long Wave Infrared Region

Chapter 1 introduced the motivation for subtracting or “skimming” the DC pedestal current signal (Appendix A) and now we formally introduce three current skimming methods of DC pedestal removal for long wave infrared imaging pixels.

Chapter 3 highlights include:

- Explanation of subthreshold operation for uncooled readouts
- Illustrate a MOS transistor, MOS cascode, or a self-biased cascode as DC bias suppression alternatives
- Describe fundamental design and subthreshold operation of the self-biased cascode transistor
- Compare output conductance of the devices to device area and geometry, as a measure of predicted skimming performance using simulated and measured data

These current skimming transistors operate in the subthreshold region of operation where channel currents are exponentially dependent on the gate voltage. The rationale for subthreshold operation in uncooled readout circuit design is due to the desire for high pixel resolution, low power dissipation which is directly related to the overall imaging system size (e.g. weight), and the signal magnitudes indicative of high resistive bolometers (Appendix A).

A more accurate description of the current skimming and direct injection transistor operation region within subthreshold is that they operate in *weak inversion* [3]. In the weak inversion region, an electric field does not exist nor does an inversion layer in the channel. The dominant carrier transport mechanism from source to drain is diffusion (e.g. carrier gradient) as opposed to drift currents for above threshold operation.

Operating currents (depending on device geometry) are very small and only require a saturation voltage, V_{sat} , of at least 100 mV at the drain terminal. The saturation voltage is the point at which the drain current becomes constant or independent of drain voltage. Since subthreshold operation requires so little bias and small current magnitudes, power dissipation is kept at a minimum. As a result, subthreshold circuit design is a very attractive option for applications requiring minimum power dissipation and small size (e.g. biologically inspired neural systems and various imaging arrays). The fundamental equation for subthreshold operation is seen in (3.1),

$$I_D = \frac{W}{L} I_o e^{-\frac{q\kappa V_g}{kT}} \left(e^{\frac{qV_s}{kT}} - e^{\frac{qV_d}{kT}} \right) \quad (3.1)$$

where q is the electronic unit of charge, W/L is the gate aspect ratio, I_o (temperature and threshold voltage dependant) is a process scaling term, V_g and V_s and V_d are the gate, source, and drain voltages with respect to the substrate potential, κ is a factor which corrects for the gate's effectiveness in controlling the drain current and varies from approximately .66 to .75 ($\kappa \approx \frac{C_{ox}}{C_{ox} + C_{dep}}$ where C_{ox} is the gate-oxide capacitance and

C_{dep} is the depletion region capacitance), k is Boltzman's constant, and T is the temperature [5]. Additional advantages for subthreshold operation include:

- Maximum g_m for a given drain current (g_m/I); as a *consequence* subthreshold operation achieves maximum intrinsic voltage gain (g_m/g_{ds})
- Low power consumption
- Saturation voltage of $\approx 4V_t$ (where V_t is defined as the thermal voltage $\left(\frac{kT}{q}\right) = 26 \text{ mV @ } T = 300 \text{ K}$)
- Subthreshold operation usually gives higher Early voltages

Current Skimming Alternatives for DC pedestal removal

Current skimming in this thesis is implemented by a current sink (*n-channel device*). Maintaining a constant current² sink requires very low output conductance in the channel. This chapter explores three different approaches for designing a low output conductance current sink. Advantages and disadvantages are explained for the different approaches with results from simulated and measured data. A recurring theme in Chapter 3 is the motivation to increase the *Early*³ voltage by increasing the transistors channel length. In subthreshold, the saturation region can have some finite slope in output current. The Early voltage (V_E) is considered (to first order) inversely proportional to a transistor's output conductance as seen in (3.1) [5,6, and 7].

$$g_{ds} \approx \frac{I_{ds}}{V_E} \quad (3.1)$$

The measured data in this thesis takes into account various geometric sizes (this thesis neglects the channel length modulation parameter λ since channels are much greater than the minimum required design length) of potential current skimmers and different bias points to gain an intuitive sense of device operation. To make a comparison to the measured data, simulated data in this thesis was performed using the PSPICE circuit simulator while implementing the BSIM3v3 MOSFET model [8]. Device and pixel layout was created using a set of scalable process-independent CMOS design rules implementing a +5 volt (3 metal layers and 2 poly-silicon layers) AMI 0.5 μm CMOS

² I-V output characteristics which have negligible slope or appear to be flat with the transistor drain-to-source voltage. The point at which the drain current is independent of drain voltage

³ Jim Early discovered modulation effects in bipolar conductance [6] as a result of reduced length in the neutral base region. This mimics the effect of *channel length modulation* in above and below threshold MOSFET's where the channel is "pinched-off" at the drain end and effectively decreases L_{eff} ; an increase in V_{ds} causes an increase in the drain current

process [9]. We begin the operational description of the current sinks presenting the single MOS transistor as the first current skimming approach.

MOS transistor

The first circuit approach is the *MOS transistor current skimmer*. Figure 3.1 illustrates a single n-channel transistor current skimmer, M_{skim} , connected in a *common gate amplifier* configuration. The common gate amplifier is also referred to as a current buffer with a current gain from source to drain of approximately unity. M_{skim} attempts to subtract the injected bias current set up by the direct injection sense node (source), the direct injection threshold voltage, the direct injection gate voltage, and the supply [1]. Current I_{det} is buffered from the detector through the injection transistor M_{di} .

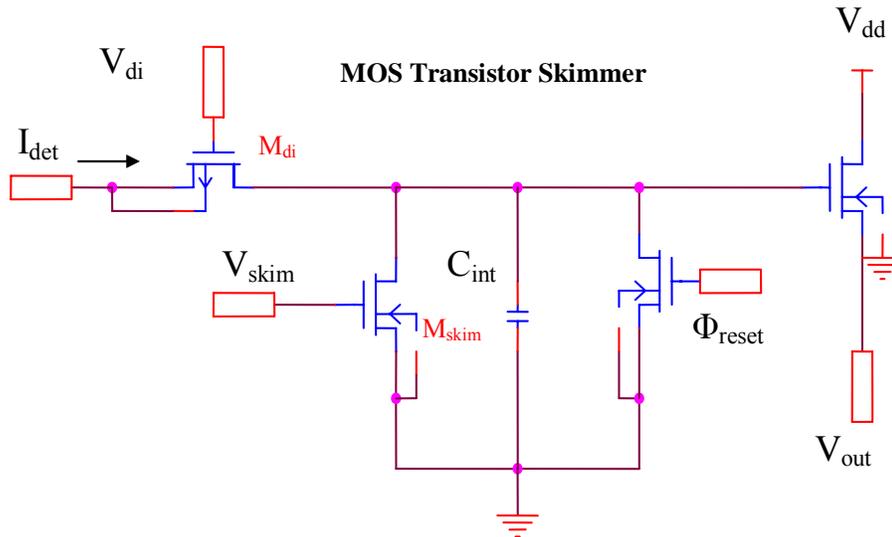


Figure 3.1: Direct injection pixel in a MOS transistor current skimming configuration

The placement of the direct injection transistor is such that it isolates the detector from the integration capacitor and therefore bias changes on the detector do not integrate

onto the capacitor. A greater signal swing results from placing the direct injection transistor between the detector and integration capacitor without influencing the detector gain [10]. One of the serious drawbacks of the configuration in Figure 3.1 is that the drain-to-source voltage on the skimming transistor varies with the voltage on the integration capacitor. An increase in V_{ds} in M_{skim} causes an increase in I_{ds} during integration, leading to a non-flat current skimming response [10]. This phenomenon is caused by the Early effect [6] mentioned in footnote 3. The Early effect manifests itself through channel length modulation, which can, in the case of the MOS transistor current skimmer, cause the effective channel to shorten while resulting in higher drain currents at the end of the integration [4, 8]. The Early voltage can also be described as the intercept of the tangent to the drain current curve with respect to the negative pseudo-current (does not physically exist) axis. The Early voltage is proportional to the drain voltage and channel length. Essentially in subthreshold saturation, the drain concentration of carriers is approximately zero; hence no carriers are injected into the drain from the drain end of the MOSFET.

Higher drain currents may cause the integration capacitor to saturate sooner than expected during a given frame. Figures 3.2 shows simulated MOS output I-V characteristics (using a BSIM3v3 MOSFET model) saturating at equal currents of 16.6 nA and a saturation voltage of 204 mV. Note, as the channel length is increased the slope of the curves decrease; the curves become more flat. Very long channels would have to be employed in the current skimmer to obtain the desired low output conductance levels at the expense of increased device area (a precious commodity in infrared imaging pixel design).

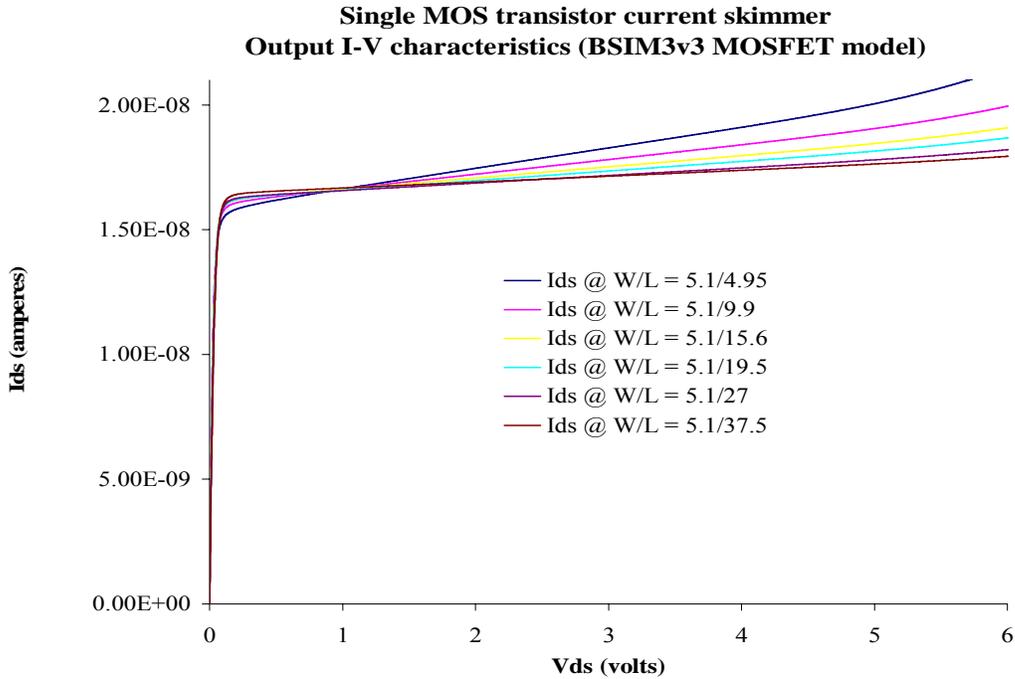


Figure 3.2: Simulated BSIM3v3 MOS model I-V data for MOS transistor at I_{sat} equal to 16.6 nA with a $V_{\text{sat}} = 204$ mV

Figure 3.3 illustrates measured data from test chip IRCHIP2 (MOSIS run ID T44L; Appendix C) where MOS transistors are saturating at equal currents and measured at equal saturation voltages of 204 mV. Their drawn widths are fixed at 5.1 μm and the lengths range from 4.95 μm to 37.5 μm . Again, notice the I-V characteristics have some slope in the output current as V_{ds} increases. This dependence in the current output on drain voltage is a result of the transistor's non-infinite output resistance for increasing V_{ds} . The experimental data appears to have less output conductance than the model would indicate from Figure 3.2. Nonetheless, there still is some significant output conductance from Figure 3.3. Relatively high output conductance from a MOS transistor for current skimming applications in uncooled infrared pixels places the design in a

suboptimal situation (e.g. the capacitor will integrate less charge within a given frame due to the skimmers drain current dependence on drain-to source voltage).

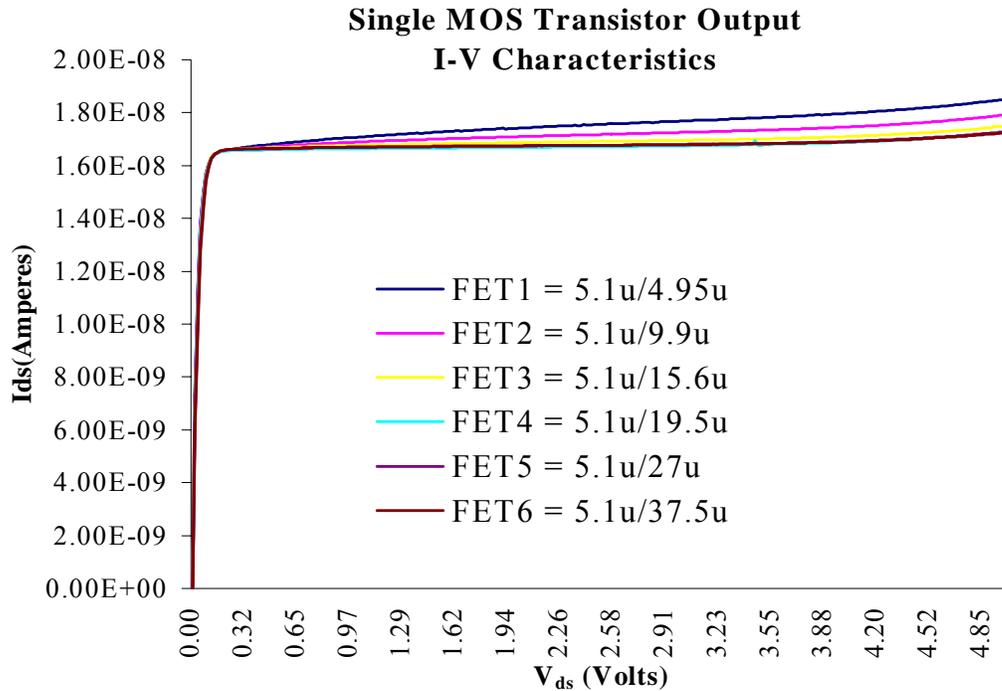


Figure 3.3: Measured I-V data for MOS transistor at $I_{sat} = 16.6$ nA with a $V_{sat} = 204$ mV

Figure 3.4 illustrates the output conductance (fixed width and increasing length) compared to channel lengths. As seen in Table 3.1, increasing the transistor length increases the Early voltage which further reduces output conductance (refer to 3.2). Table 3.1 displays transistor area versus output conductance and Table 3.2 compares gate voltage levels. None of the simulated gate voltages were below a threshold voltage. Figure 3.4 illustrates a discrepancy between the measured data and the model for subthreshold operation.

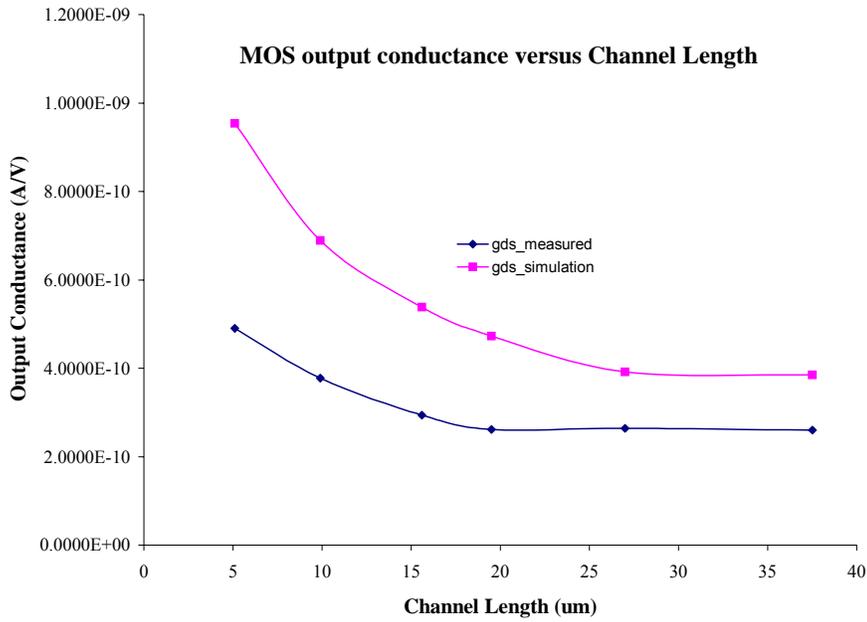


Figure 3.4: Measured and simulated output conductance versus channel length for the MOS transistor

Transist or Area (um ²)	Transistor dimensions (W/L)	gds_measured (A/V)	gds_simulation(A/V)
25.5	FET1 = 5.1u/4.95u	4.90E-10	9.54E-10
50.49	FET2 = 5.1u/9.9u	3.78E-10	6.89E-10
79.56	FET3 = 5.1u/15.6u	2.94E-10	5.38E-10
99.45	FET4 = 5.1u/19.5u	2.61E-10	4.73E-10
137.7	FET5 = 5.1u/27u	2.64E-10	3.92E-10
191.25	FET6 = 5.1u/37.5u	2.60E-10	3.86E-10

Table 3.1: Measured at the onset of saturation for $I_{ds} = 16.6$ nA and $V_{sat} = 204$ mV

Measured gate voltage (mV)	Simulated gate voltage (mV)
576.0	725.2
593.2	754.4
612.0	773.8
624.3	783.3
639.0	797.4
655.6	812.2

Table 3.2: V_{gs} at the onset of saturation for $I_{ds} = 16.6$ nA and $V_{sat} = 204$ mV

Figure 3.5 shows a direct injection pixel with a simplified small signal circuit representation for the MOS transistor current skimmer.

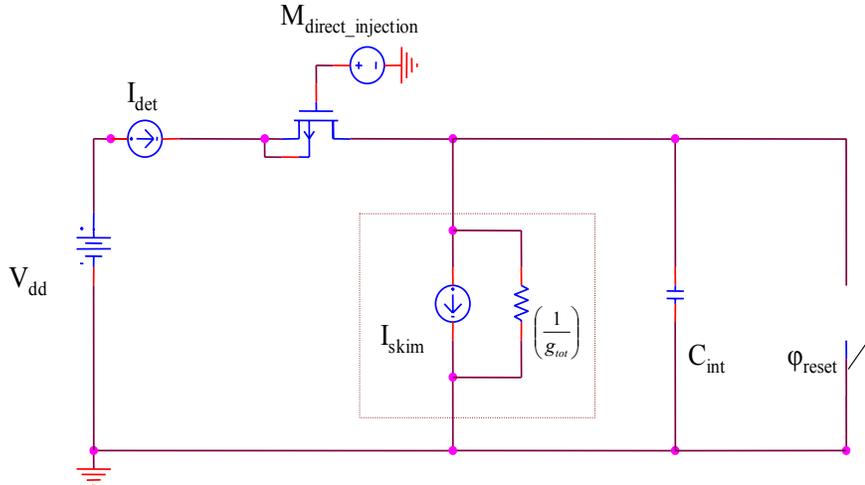


Figure 3.5: Circuit schematic and basic small signal model for current skimming

In order to provide the highest efficiency of skimming, g_{tot} (total output conductance) must theoretically approach zero (infinite output resistance). Figure 3.6 shows that by theoretically decreasing the output conductance further within the range of the desired integrated voltage signal, the slope of the output characteristics becomes more linear. At the right of Figure 3.6 are the corresponding output conductances.

By substituting different values for the small signal output resistance (the inverse of output conductance), Figure 3.5 is able to show the reader that in order to effectively remove the DC bias pedestal, the current skimmer must have a very low output conductance to minimize the slope of the output current (in saturation) as seen in Figure 3.2 and 3.3. If output conductance is high, the skimming drain current becomes dependent on changes in the drain to source voltage of the MOS transistor current

skimmer and voltage changes on the integration capacitor. The relatively high output conductance for MOS transistor leaves much doubt to the efficiency of this device's ability to extend the integration time efficiently. According to Figure 3.6, using a MOS transistor as a current skimming option can effectively increase integration times up to 2 ms; a possible factor increase of 47 (refer to Chapter 1).

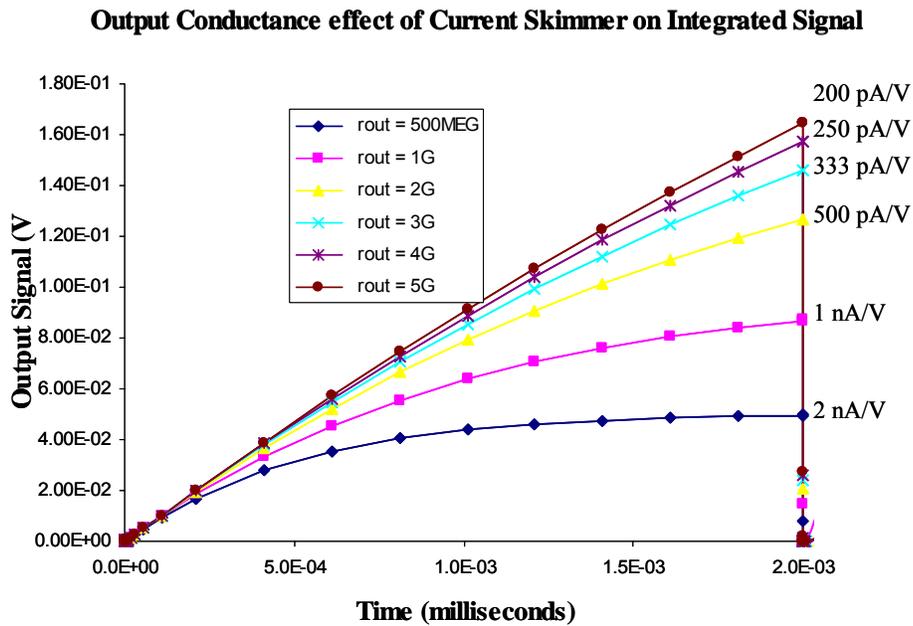


Figure 3.6: Affect on integration node signal as a function of MOS transistor output conductance and small signal output resistance

MOS cascode

A second circuit-approach of current skimming uses a cascoded *MOS transistor current sink* shown in Figure 3.7. The cascode is a series connection of a common source (M_{input}) amplifier and a common gate amplifier ($M_{cascode}$). The purpose of the cascoding is to decrease the output conductance further compared to that of the MOS transistor. Reduction in output conductance is caused by adding a transistor connected in series

which effectively increases the overall channel length of the configuration. The output conductance in a MOS cascode, due to an effectively longer channel, affects a smaller proportion of the overall channel length than with a MOS transistor. Another parameter is also introduced at the expense of an additional bias wire (V_{cascode} in Figure 3.7). This configuration is very effective in obtaining low output conductance and the dimensions can be made relatively small. The common source amplifier, M_{input} , performs voltage-to-current conversion with gain $\frac{g_m}{g_d}$ and the common gate amplifier, M_{cascode} , performs current-to-current conversion with gain $\frac{g_s}{g_d}$ [11]. M_{cascode} is considered a common gate configuration because V_{cascode} is at a constant, fixed voltage (known as a *fixed biased cascode*) [11]. M_{input} essentially biases the current while M_{cascode} acts as output resistance multiplier to the small signal output resistance of M_{input} .

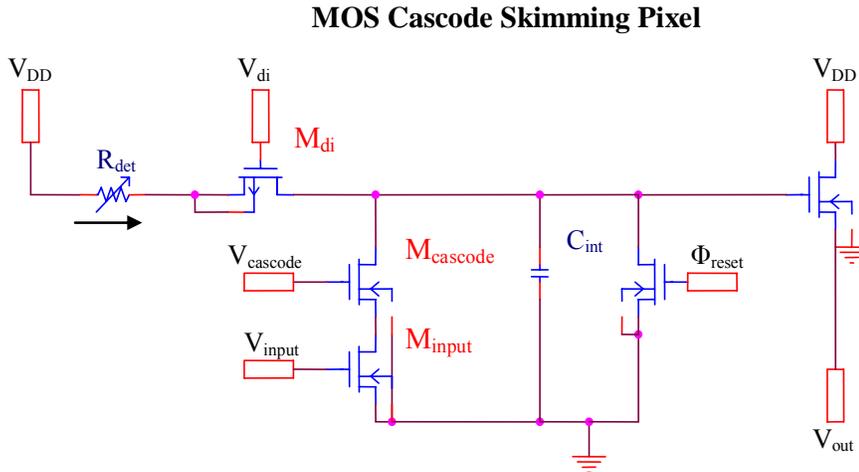


Figure 3.7: Direct injection pixel with MOS cascode skimming configuration

An immediate disadvantage for this configuration is the saturation voltage required to keep both M_{input} and M_{cascode} in saturation. For example, in subthreshold, saturation voltage V_{sat} for a MOS transistor requires approximately 100 mV. However, V_{input} may swing between a V_{min} and V_{max} voltage value in order to adjust for various current skimming levels. As a consequence, $V_{\text{cascode}} - V_{\text{dMininput}}$ also varies between V_{min} and V_{max} . In order to ensure M_{input} is saturated, $V_{\text{dMininput}}$ must be larger than V_{sat} . From this fact, V_{cascode} must be larger than $V_{\text{sat}} + V_{\text{max}}$. For example, if $V_{\text{cas}} = V_{\text{sat}} + V_{\text{max}}$, then when V_{min} occurs at the gate of M_{skim} , $V_{\text{cascode}} = V_{\text{dMininput}} + V_{\text{min}}$. The output voltage of the cascode configuration must be greater than $V_{\text{sat}} + V_{\text{dMininput}}$. Therefore, the output voltage to ensure that both M_{input} and M_{cascode} remain in saturation is $2V_{\text{sat}} + V_{\text{max}} - V_{\text{min}}$ [11]. Figure 3.8 shows simulated data for four different cascode transistors with increasing width.

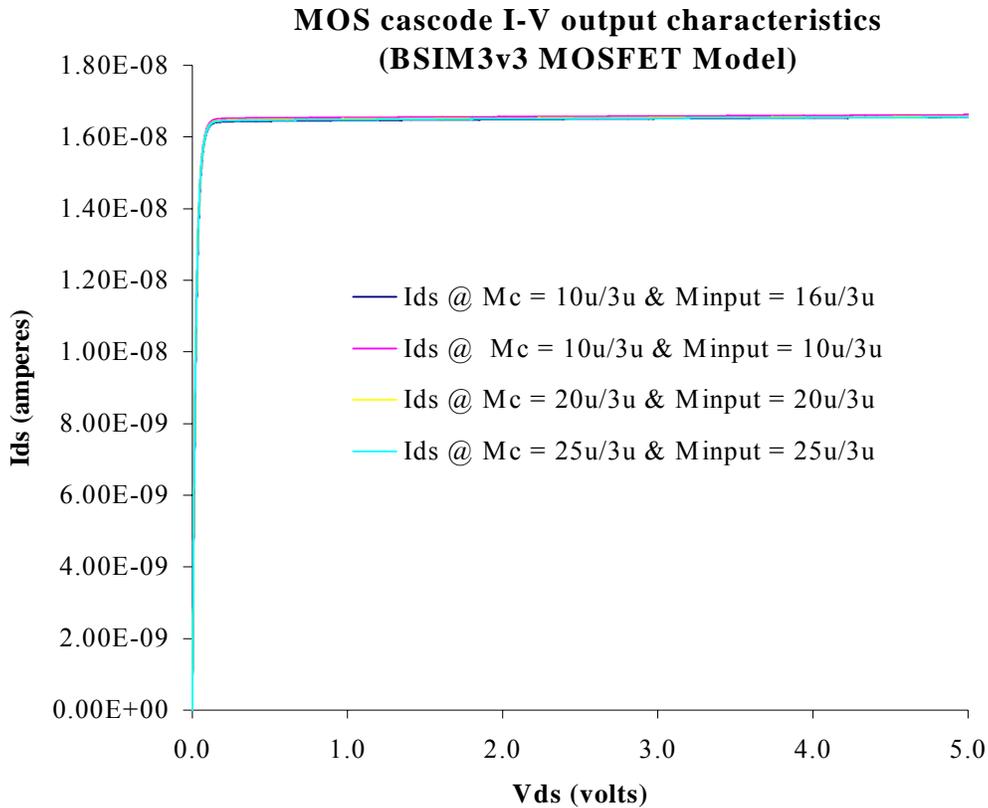


Figure 3.8: Simulated I-V data for the MOS cascode at $I_{\text{sat}} = 16.6$ nA with a $V_{\text{sat}} = 204$ mV

While keeping the lengths equal and forcing both cascode and input transistors into subthreshold, the widths had to be made very wide. Figure 3.9 takes the data from Figure 3.8 and plots the output conductance versus MOS cascode area for increasing widths and a fixed length.

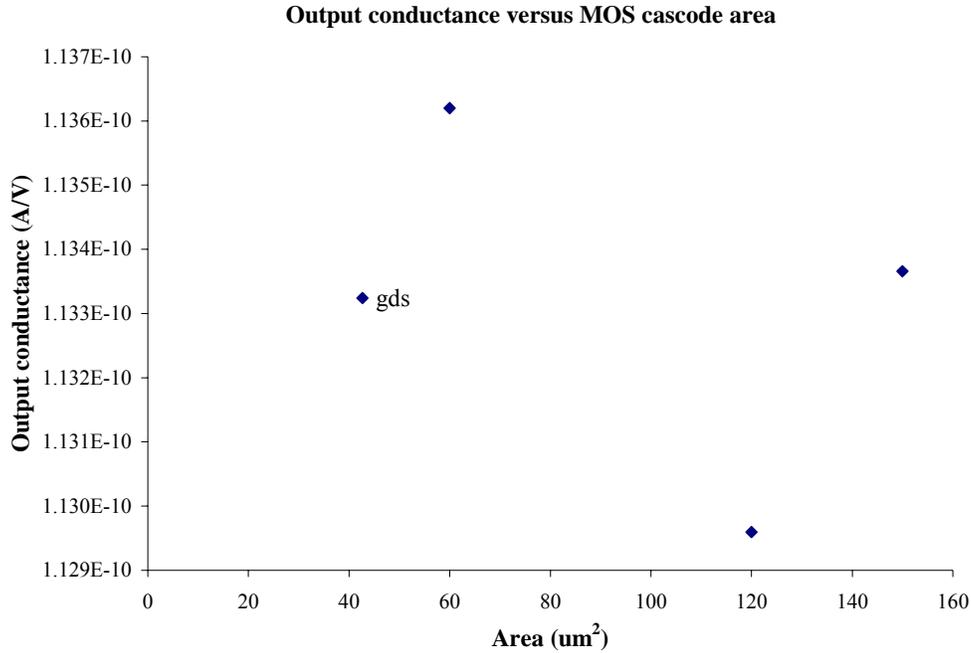


Figure 3.9: Simulated output conductance of MOS cascode transistor $I_{\text{sat}} = 16.6$ nA and $V_{\text{sat}} = 204$ mV

The widths must be increased to maintain equal saturation currents of 16.6 nA and saturation voltages of 204 mV for a fixed length while operating in the subthreshold state (implies a gate-to-source voltage much less than a threshold for both M_{cascode} and M_{input}). However, to maintain equal saturation currents and voltages while keeping the widths fixed and increasing the channel lengths requires an increase in gate-to-source voltage which causes above threshold operation. The MOS cascode operating above a threshold voltage is an undesirable condition for this current skimming application.

Self-biased cascode transistor

Instead of two separate bias lines as seen in the MOS cascode configuration, another way to reduce the output conductance in *subthreshold operation* is to have the gates connected to a common bias line and employ an unusual transistor aspect ratio; M_{cascode} is much larger than the width to length ratio of M_{skim} for purposes of saturating M_{cascode} in weak inversion. The self-biased cascode transistor consists of two common-gate transistors in series [12]. The transistor with the shorter length is the cascoded transistor. The transistor with the longer length is the bias or skimming transistor.

As a result of the aforementioned width to length ratio requirements and operating in the subthreshold state, the gate and threshold voltage of M_{cascode} is less than M_{skim} . The design of the self-biased cascode is such that V_{sat} (drain saturation voltage) of M_{skim} is approximately 100 mV. Therefore, the gate voltage of M_{cascode} is the difference between the gate voltage of M_{skim} and V_{sat} of M_{skim} [13].

Self-Biased Cascode Skimming Pixel

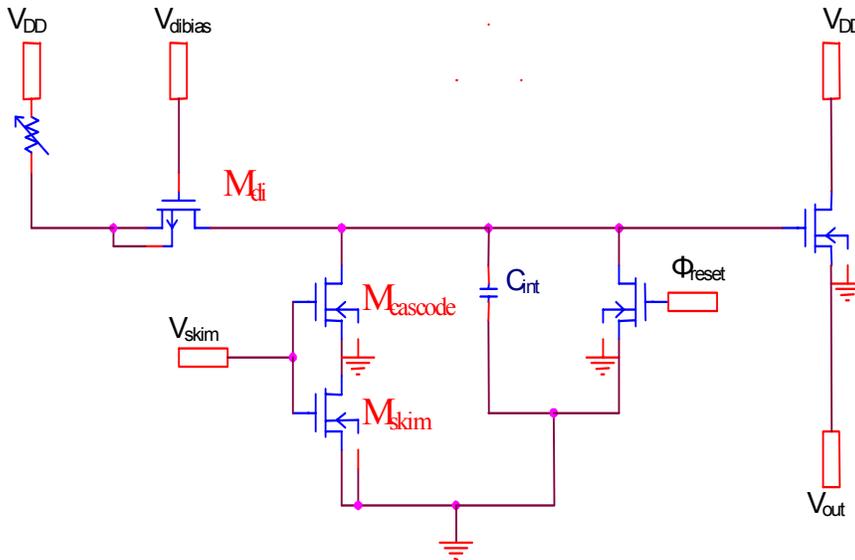


Figure 3.10: Direct injection pixel with the self-biased cascode skimming configuration

The self-biased cascode has the added advantage over the MOS cascode configuration of only requiring $2V_{\text{sat}}$ to keep M_{cascode} and M_{skim} in saturation (the self-biased cascode saturates earlier [11] than either the MOS cascode or MOS transistor). A disadvantage of the self-biased cascode is that it requires additional area to achieve similar output conductance levels as the MOS cascode configuration. However, since both the MOS cascode and self-biased cascode transistors effectively operate with different threshold voltages between M_{cascode} and M_{skim} (M_{input}), it is worth while to mention the availability of a *multiple threshold voltage* standard CMOS process⁴.

The first reports of this unusual *subthreshold* state device originated in the early 1990's from NASA's Jet Propulsion Laboratory and has been analyzed and verified by the Swiss Federal Institute of Technology's Eric A Vittoz [14].

Self-Biased Cascode Transistor

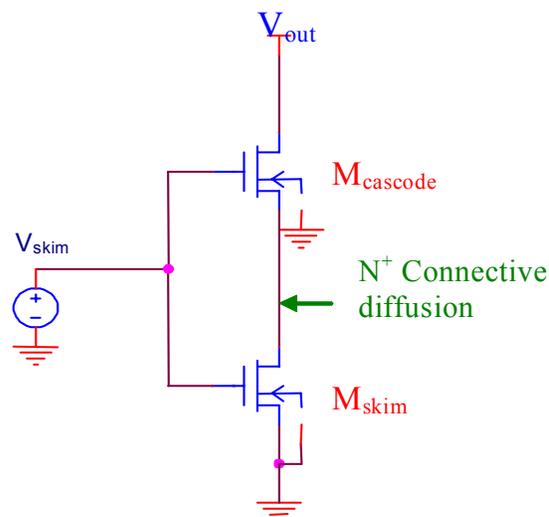


Figure 3.11: Self-Biased Cascode Composite Transistor

⁴With the availability of a multiple threshold voltage processes at STmicroelectronics (<http://www.st.com>) and Peregrine (SOS) (<http://www.peregrine-semi.com/>), a self-biased cascode transistor can be constructed with comparable to smaller area than that of a conventional MOS cascode

This unique structure in Figure 3.11 known as a self-biased cascoded transistor [12] is connected through n^+ diffusion between the source of M_{cascode} and the drain of M_{skim} . The intended original purpose of this device was to provide a lower output conductance source while reducing the Early voltage [15] compared to that of a MOS transistor or MOS cascode. Since then, the self-biased cascode transistor has gained attention for its high performance as an efficient low output conductance device implemented in low voltage system design.

Compactness is ultimately limited by the minimum poly-to-poly distance rule for the cascode and skimming transistor gates as illustrated in Figure 3.12. Explanation for eliminating the contacts between the source of the cascode and drain of the skim transistor provides a more compact design by decreasing device area and reducing junction capacitance as illustrated in Figure 3.12 [2]. Having contact connections on the connective diffusion also imposes minimum contact spacing rules.

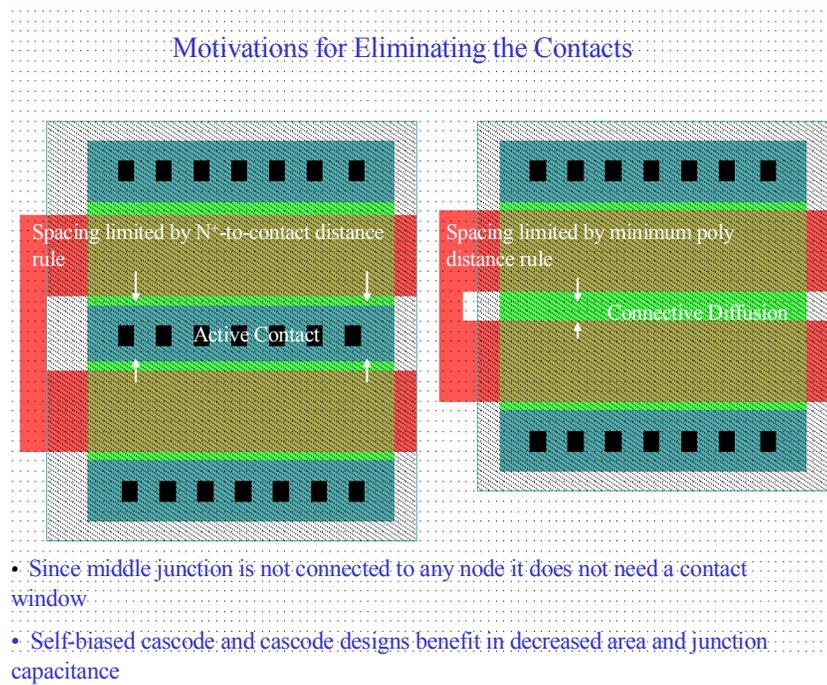


Figure 3.12: Motivations for eliminating the contacts in the self-biased cascode

Figure 3.13 shows simulated data of the self-biased cascode transistor. The blue data curve exhibits high output conductance and proves the necessity of M_{cascode} to have a larger width to length ratio than M_{skim} . As the length of M_{skim} increases, the output conductance reduces as seen by Figure 3.13. We can compare relative results from the simulated data to Figure 3.14's recorded data from test chip IRCHIP2.

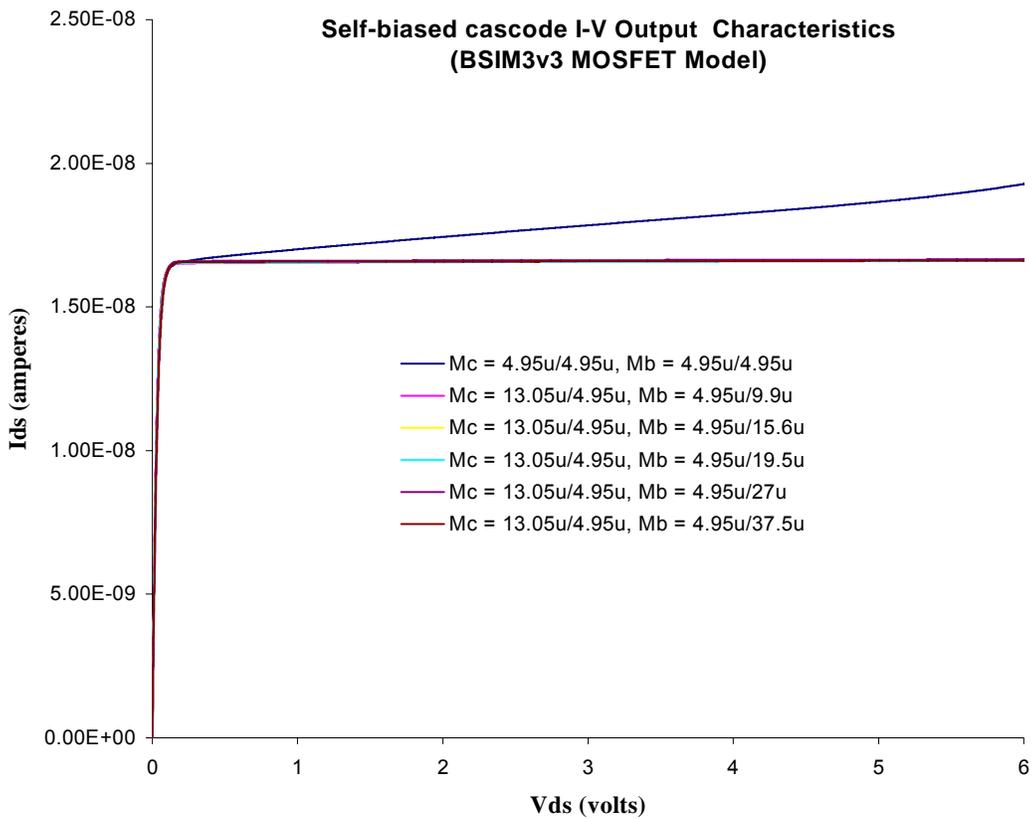


Figure 3.13: Simulated I-V data for the self-biased cascode at $I_{\text{sat}} = 16.6 \text{ nA}$ with a $V_{\text{sat}} = 204 \text{ mV}$

Both Figures 3.13 and 3.14 illustrate an equal saturation current of 16.6 nA of the self-biased cascode at a saturation voltage of 204 mV (albeit at different V_{gs} due to differences between the simulation model and measured data). The simulated data has the

I-V output characteristics predominately flat for the entire range of V_{ds} . The actual results exhibit some slope toward the power supply rail V_{dd} . Ironically, the slope increase at approximately 4.5 V appears for all the data curves. A possible reason for this might be the self-biased cascode transitioning from subthreshold to above threshold operation. The threshold voltage used in simulation was approximately 670 mV (for an n-channel device) and the actual extracted threshold voltage reported from the foundry was 611 mV (see Appendix C). Nonetheless, the output characteristics in both simulation and experimentally recorded data both display virtually flat curves for a majority of the V_{ds} range and are vast improvement over the MOS transistors' output characteristics.

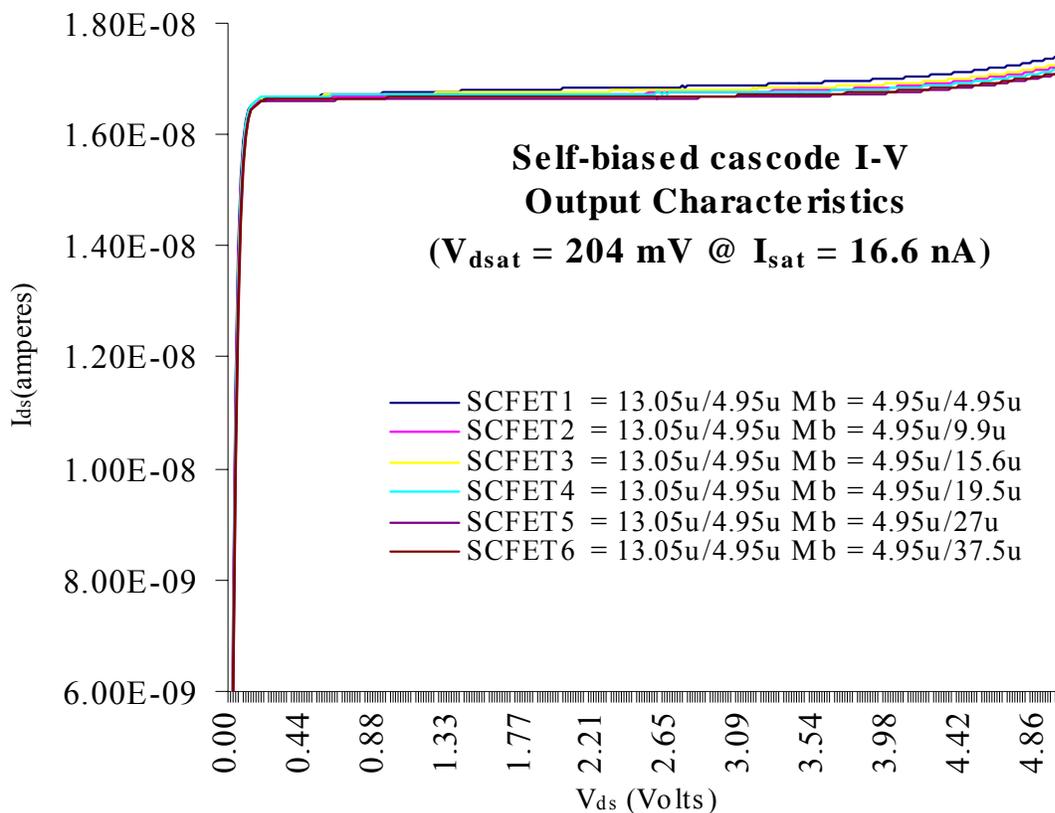


Figure 3.14: Measured I-V data for self-biased cascode at $I_{dsat} = 16.6 \text{ nA}$ and $V_{sat} = 204 \text{ mV}$

Table 3.3 shows that for fixed cascode geometry and bias transistor width, increasing bias transistor length decreases the total output conductance as long as subthreshold operation is maintained.

Area (μm^2)	Self-biased cascode dimensions	gds_measured (A/V)	gds_simulated (A/V)
89.1	SCFET1 = 13.05u/4.95u Mb = 4.95u/4.95u	2.6089E-10	5.02E-10
113.6025	SCFET1 = 13.05u/4.95u Mb = 4.95u/9.9u	2.4000E-10	9.94E-11
141.8175	SCFET1 = 13.05u/4.95u Mb = 4.95u/15.6u	2.4097E-10	8.93E-11
161.1225	SCFET1 = 13.05u/4.95u Mb = 4.95u/19.5u	2.2201E-10	8.89E-11
198.2475	SCFET1 = 13.05u/4.95u Mb = 4.95u/27u	2.2504E-10	9.04E-11
250.2225	SCFET1 = 13.05u/4.95u Mb = 4.95u/37.5u	2.3000E-10	9.32E-11

Table 3.3: Self-biased cascode area compared to measured and simulated output conductance at $I_{\text{sat}} = 16.6 \text{ nA}$ and $V_{\text{sat}} = 204 \text{ mV}$

To first order, Early voltage is proportional to length of transistor [5, 7, and 11]. For widths and lengths of transistors in this thesis, transistors are likely to have Early voltages in the range of 34-100 V for n-channel transistors and 50-100 V for p-channel transistors [16].

M_{cascode} performs the same function as in a conventional cascode structure; it acts as a *shield* [2, 13] from the time dependent integration node, while M_{skim} sets the bias current in the self-biased cascode. The total output conductance from a single transistor to the self-biased cascode is reduced by the common gate gain of the cascode shown in (3.3).

$$A_{\text{cg}} = \frac{g_s}{g_d} \quad (3.3)$$

Since output resistance is inversely proportional to output conductance, the interested reader may note that the ratio, $\left(\frac{L_{\text{skim}}}{L_{\text{cascode}}}\right)$, normalized to a unity bias transistor geometry shows a saturated output resistance at a length ratio of approximately 6:1[13].

Figure 3.15 displays output conductance versus device area. The output conductance decreases with increasing device area. Because this increasing tail appears in subsequent graphs it is again worth while to mention to the reader that the increasing gate voltages to obtain equal saturation currents may be causing the bias transistor to slip out of subthreshold for reasons of simulated versus reported threshold voltages (Appendix C). But interestingly enough, the increasing slope does not appear until at least $V_{ds} = 4$ V as seen in Figure 3.14.

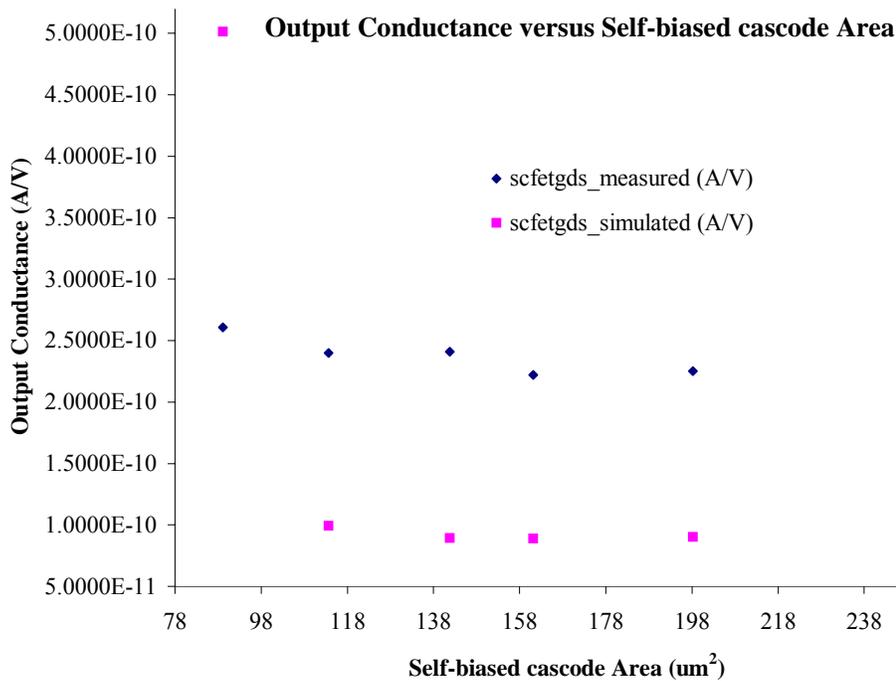


Figure 3.15: Measured and simulated output conductance versus area for the self-biased cascode at $I_{sat} = 16.6$ nA and $V_{sat} = 204$ mV

Comparing Figure 3.14 to the simulation data in Figure 3.13 emphasizes the point of increasing the cascode-to-bias transistor length ratio as seen in Figure 3.16. The essential

goal is to reduce the g_{ds} of M_{skim} (seen in (3.3)) by making the transistor length longer so that the output conductance affects a smaller proportion of the overall channel length.

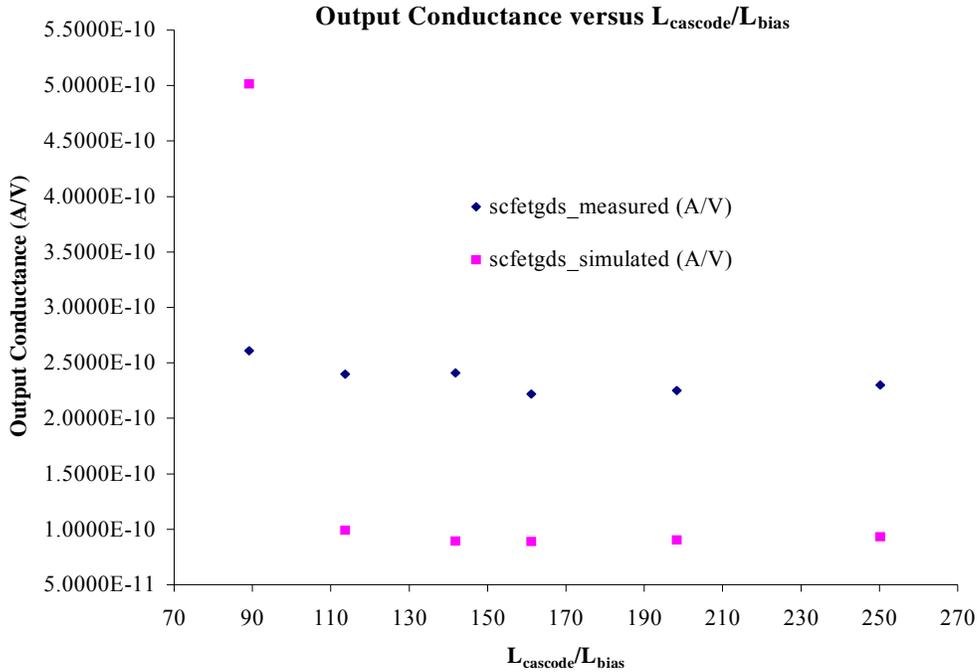


Figure 3.16: Measured and simulated output conductance for the self-biased cascode at $I_{sat} = 16.6$ nA and $V_{sat} = 204$ mV versus $\left(\frac{L_{bias}}{L_{cascode}}\right)$

Figure 3.17 takes another vantage point of showing the decreasing output conductance versus the increasing aspect ratio of the $M_{cascode}$ to M_{skim} .

For a moment, let us assume that the length and width of $M_{cascode}$ and M_{skim} are equal. If we make the width of $M_{cascode}$ sufficiently larger while increasing the length of M_{skim} , proportionately we will need a correspondingly less amount of bias voltage on the gate of $M_{cascode}$. Setting the width of the skimming transistor to minimum geometry causes in an increase in threshold voltage with respect to the threshold voltage of the

cascode transistor. This is caused by the narrow-channel effect on the skimming transistor [16]. Essentially, the threshold voltage increases due to fringing field lines from the gate terminating on charges outside the effective channel [8]. This is the rationale for biasing the cascode transistor in subthreshold while acting as a shield to M_{skim} . Furthermore, the threshold voltages between M_{cascode} and M_{bias} are different as result of their aspect ratios. The inability to indirectly control the two threshold voltages is a disadvantage. Earlier in this section we mentioned a possible solution of being able to have a device with two distinct threshold voltages using a multiple threshold voltage CMOS process. If this is the case, then the need for the unique aspect ratios would not apply and the self-biased cascode could be made very small with only one common bias line.

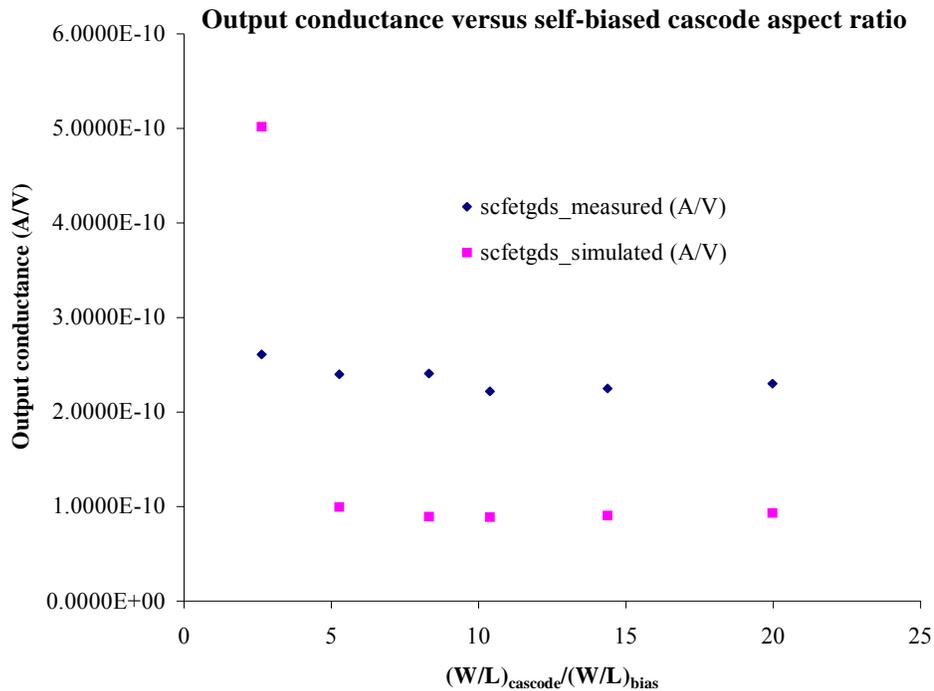


Figure 3.17: Measured and simulated output conductance for the self-biased cascode at $I_{\text{sat}} = 16.6 \text{ nA}$ and $V_{\text{sat}} = 204 \text{ mV}$ versus aspect ratio

The following guidelines highlight some self-biased cascode design rules.

Self-biased cascode scaling and biasing rules:

- Cascode transistor must have a *large width*
- Cascode transistor must remain in weak inversion (*The bias or skim transistor's drain potential must be $\approx 100\text{ mV}$. The drop at this node is seen across the gate of the cascode transistor which determines the cascode region of operation*)
- $\frac{L_{bias}}{L_{cascode}} \geq 1$
- Ratio of cascode to bias transistor geometry > 1 and $\left(\frac{W}{L}\right)_c > \left(\frac{W}{L}\right)_b$
- Use minimum bias transistor width (*when possible*)
- Use minimum cascode transistor length (*when possible*)

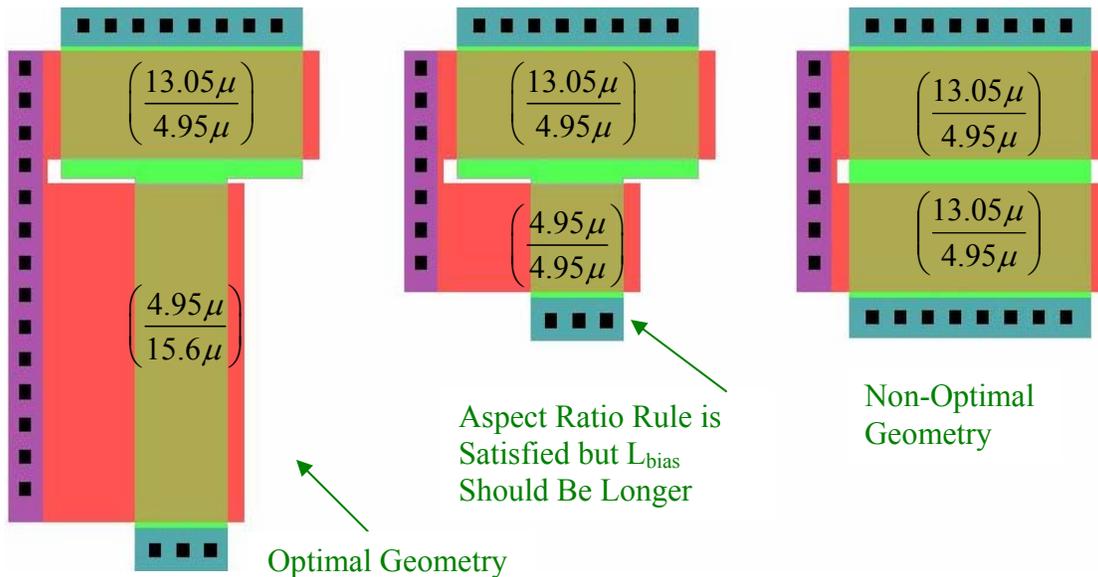


Figure 3.18: Examples of the scaling design criteria for self-biased cascode

Figure 3.18 shows the application of scaling rules for self-biased cascode transistors. Depending on the requirements, the design should employ minimum geometry when possible. The motivation for having unique aspect ratios for the self-

biased cascode is to force the cascode transistor to operate in weak inversion (e.g. having a large width and lower threshold voltage) with the bottom bias transistor operating in weak-to-moderate inversion [12, 13]. By driving the cascode into weak inversion with a large width and a weak-to-moderately inverted long skimming transistor, I_{skim} is not dependent on V_{ds} or the range of Early voltages. [15]. The interested reader is referred to [8, 16] for a comprehensive resource on MOSFET modeling in the subthreshold region. Table 3.4 gives the reader a comparison analysis of the proposed current skimming devices for DC pedestal removal in continuous bias uncooled (infrared) imaging arrays.

Subthreshold Current Skimming Device	Output Conductance	Output resistance	Number of bias lines	Advantages	Disadvantages	Recommendations
MOS transistor	g_{d_skim}	r_{ds_skim}	1	-simple -1 bias line -high output voltage swing	- channel length modulation - requires large area - high g_{ds}	- use a MOS cascode or self-biased cascode
MOS cascode	$g_{d_skim} \left(\frac{g_{d_cascode}}{g_{s_cascode}} \right)$	$g_{m_cascode} r_{ds_cascode} r_{ds_skim}$	2	-small area -low g_{ds}	-2 bias lines -requires $2V_{sat} + (V_{max} - V_{min})$ - reduced dynamic range -relatively large area	-low voltage cascode design - use a self-biased cascode for reduced supplies
Self-biased cascode	$g_{d_bias} \left(\frac{g_{d_cascode}}{g_{s_cascode}} \right)$	$g_{m_cascode} r_{ds_cascode} r_{ds_bias}$	1	-1 bias line -low g_{ds} -excellent performance in subthreshold -requires only $2V_{sat}$ to operate	-large area -cannot control threshold voltages	-take advantage of a multiple threshold voltage process to gain area advantage of MOS cascode - use floating gate technology

Table 3.4: Subthreshold current skimming device comparison

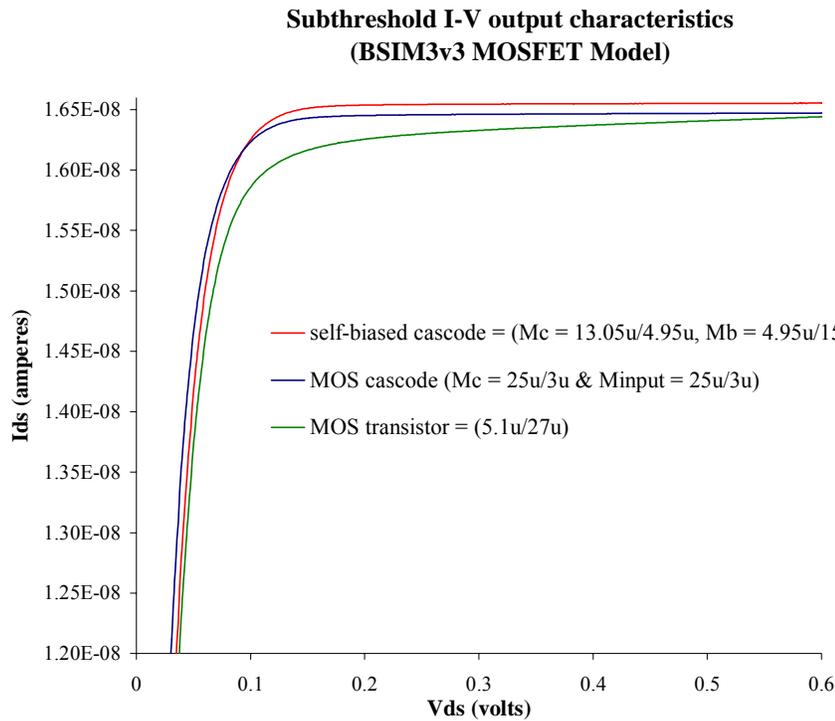


Figure 3.19: Comparison of saturation levels for current skimmers

Figure 3.19 illustrates the saturation points for the three different skimming devices. It is apparent that the MOS transistor has a higher output conductance and never stabilizes over the range of integrated V_{ds} . To have the MOS cascode operate efficiently in subthreshold, both transistors (from simulation) must be made relatively wide so that the threshold voltage is effectively reduced (gate voltage is distributed proportionately less over a wider region). Ironically for the MOS cascode, if we invert the W/L of M_{input} (Figure 3.8) and connect the two transistor gates we essentially form a self-biased cascode. In general, the self-biased cascode drain will saturate quicker than the MOS cascode's drain [11]. As power supplies reduce (with modest decreases in threshold

voltages), the MOS cascode is suboptimal in subthreshold as opposed to optimal operation for the self-biased cascode for subthreshold operation.

In conclusion, Chapter 3's main objective was to present three different current skimming approaches that attempted to remove the DC pedestal from the uncooled infrared pixel. Table 3.4 summarizes the various aspects with recommendations on improving the performance of the current skimming device or suggests an alternative technology. Table 3.4 mentions the use of a multiple threshold voltage process (refer to footnote 4) and a floating gate technology. These two alternatives are not the focus of this thesis however it is noteworthy to mention that these solutions justify the significance for a self-biased cascode structure (over a MOS cascode) used for current skimming applications in uncooled infrared imaging. A multiple threshold voltage or floating gate process can accommodate a self-biased cascode structure with decreased area (as seen in the MOS cascode), a common gate line, and ultra-low output conductance.

At this point, it is important to clarify to the reader that a *per-pixel skimming approach* has not been implemented (to date) in a continuous bias uncooled infrared imaging array. Chapter 4 discusses experimental data recorded from two test chips that were designed for this thesis research. Much of the transistor I-V and output conductance data that was seen throughout Chapter 3 was designed on IRCHIP2 using models in Appendix C. The subsequent chip, IRCHIP1, contained a prototype design of a direct injection pixel incorporated with the current skimming function. Since uncooled bolometer detectors are not readily available to academia (nor very cheap), a fixed metal film resistor was substituted in the detector's place to set a *pseudo-detector current*. As a consequence of no infrared detector present, no actual infrared signal could be measured.

Therefore, the experiment aimed to test the DC operation of the pixel to prove the concept of current skimming. **The reader should not get confused between the proof of concept used here in this thesis using DC bias operation as a test and current skimming which aims to remove the DC bias. The fundamental concern was to demonstrate and design current sinks with very low output conductance which will effectively remove the DC bias signal when a detector is in place.**

Chapter 4: Experimental Results and Discussion

Chapter 4 will describe the experimental results from two chip designs, *IRCHIP1* and *IRCHIP2* using MOSFET model data seen in Appendix C. The test circuits were simulated and designed with software from Cadence (<http://www.cadence.com/>) while the layout and verification were performed with L-Edit Pro-9TM (Tanner Research Corporation; <http://www.tanner.com/>) and LVS respectively. Upon successful layout versus schematic, the design was sent to the MOSIS foundry for fabrication⁵. The chip was designed using the 5 volt AMI 0.5um (C5N family) process. The die area was 1.5 mm² and included 40 pads for pin-out. All waveforms were acquired with a Tektronix TDS-3052B 2-channel digital oscilloscope. To power particular input pads, the Agilent E3610A DC Power supply was used in the experiments. All calculations in this thesis were based on the drawn widths and lengths. For example, measurements for output conductance versus area were done so with the drawn widths and lengths. The area measurements refer to the device's surface area (e.g. $L_{\text{drawn}} \times W_{\text{drawn}}$). In the case of the MOS cascode and self-biased cascode, the two drawn surface areas were added from both the cascode and bias or input (bottom) transistors. Data was saved in MS Excel format (<http://www.microsoft.com/>) and plotted in the figures throughout this thesis. No error analysis was performed on the measurements made in this thesis research therefore no error bars appeared in the acquired data. We begin by describing *IRCHIP1*. Figure 4.1 illustrates a schematic of the test setup.

⁵ <http://www.mosis.org>

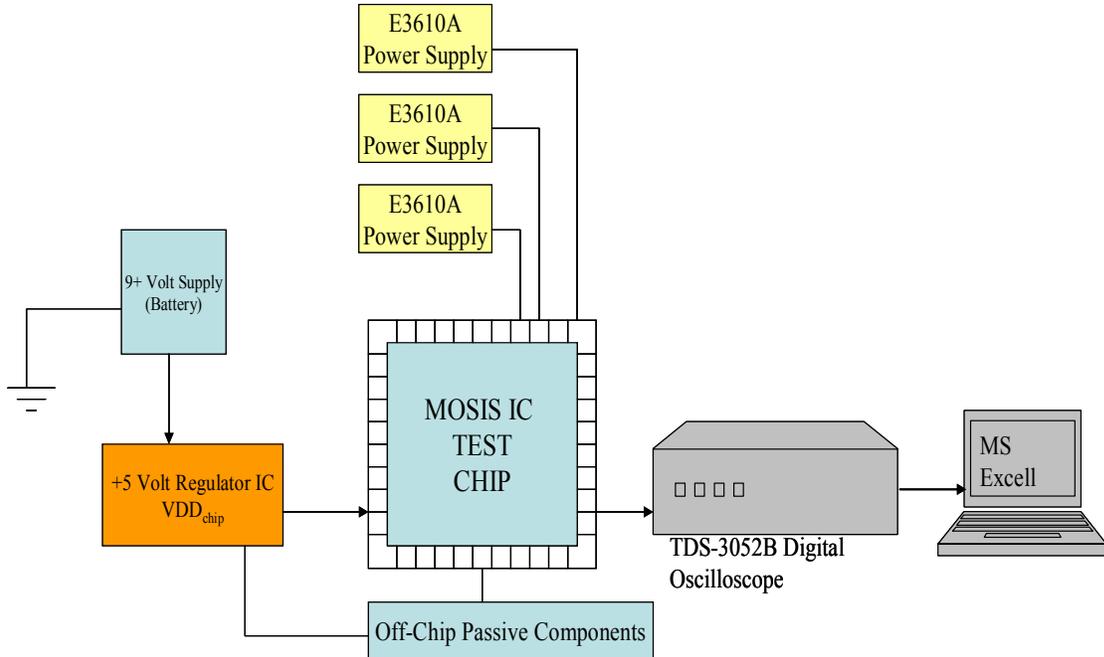


Figure 4.1: System setup configuration

IRCHIP1

Chip Description & Function

The goal of IRCHIP1 was to demonstrate, through DC operation, long integration times by implementing a current skimming device. The principle behind continuous bias operation is that there are small resistance changes around a known DC bias point (Appendix A). Since a bolometer detector could not be acquired, a fixed metal film resistor was used as a replacement. Because only the DC operation of the current skimming pixel was being tested, the use of a fixed known input detector resistance was appropriate. By measuring the voltage drop across both known input detector resistance and the reference current resistance, both the input detector and reference current could be experimentally determined.

An off-chip resistor connected to V_{dd} generated a reference current that was subsequently buffered through a common gate amplifier (current buffer). This p-channel current buffer was geometrically identical to the direct injection transistor for the purpose of matching and establishing equal injection and skimming currents. The buffered current was injected to a linear array of self-biased cascode current mirrors which in turn created an equal copy of current to the self-biased cascode in the pixel. Gate voltage adjustments on the current buffer allowed the reference current to be modulated as well as the copied version to the self-biased cascode skimmer in the pixel. This modulation was the controlling mechanism of the skimming current. The user could either increase the skimming current or decrease the skimming current.

Furthermore, by dividing the known reference current from the number of current mirrors, the actual skimming current could be experimentally determined with reasonable accuracy. Pixel reset timing was controlled by an external Labview program from National Instruments (<http://www.ni.com/labview/>) and a National Instruments digital-to-analog converter card which pulsed the gate of the reset transistor. Pixel output was taken at the source follower (voltage buffer) output pad and viewed on the digital oscilloscope.

Figure 4.2 shows the layout of IRCHIP1. The upper right corner Figure 4.2 is magnified in Figure 4.3, which shows the biasing setup of a test pixel explained above. Since the input current to the pixel is constant, this setup makes it easier to just manipulate one variable, the skimming current. The integrated DC current charges the capacitor in the pixel to a particular voltage level (current-to-voltage conversion) and then is subsequently buffered out by a source follower. The implementation of a reset transistor allows the signal shaping function in the form of a ramp, sample, and dump of

the integrated DC charge. For example, the DC signal charges for a period of time (ramping of signal), the reset goes high (sampled to output), and then the switch closes (signal is dumped to ground). Essentially, this pixel employs a destructive readout sequence. The signal is sampled for a brief period of time and then is destroyed by being routed to ground only to repeat itself once again through the pixel reset clock.

To obtain the best sensitivity and matching for copying currents, designs should employ the maximum number of current mirrors [9, 15]. In Figure 5.3, we see 17 parallel self-biased cascode current mirrors. As a note to the reader, a common centroid layout of current mirrors (Appendix B) would have provided better matching and sensitivity than a linear array of current mirrors [15].

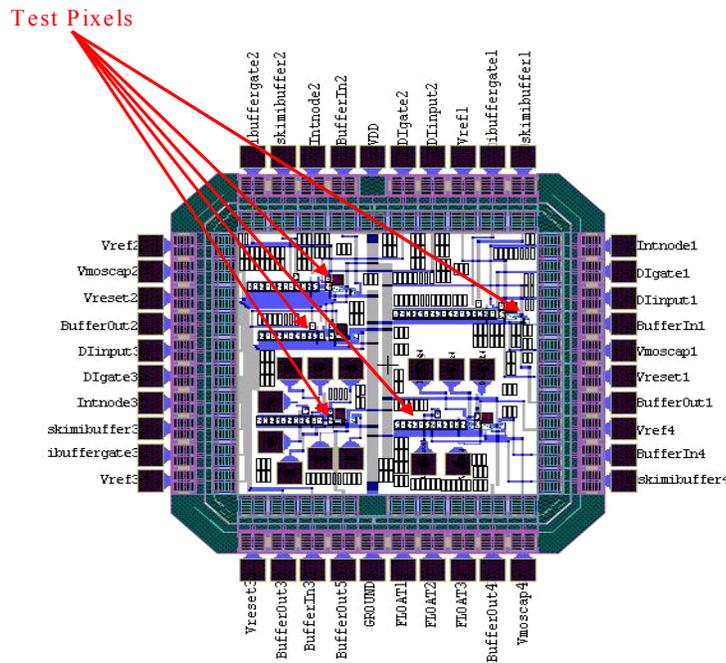


Figure 4.2: IRCHIP1 test chip on MOSIS run T3AJ (AMI C5N 0.5 μm)

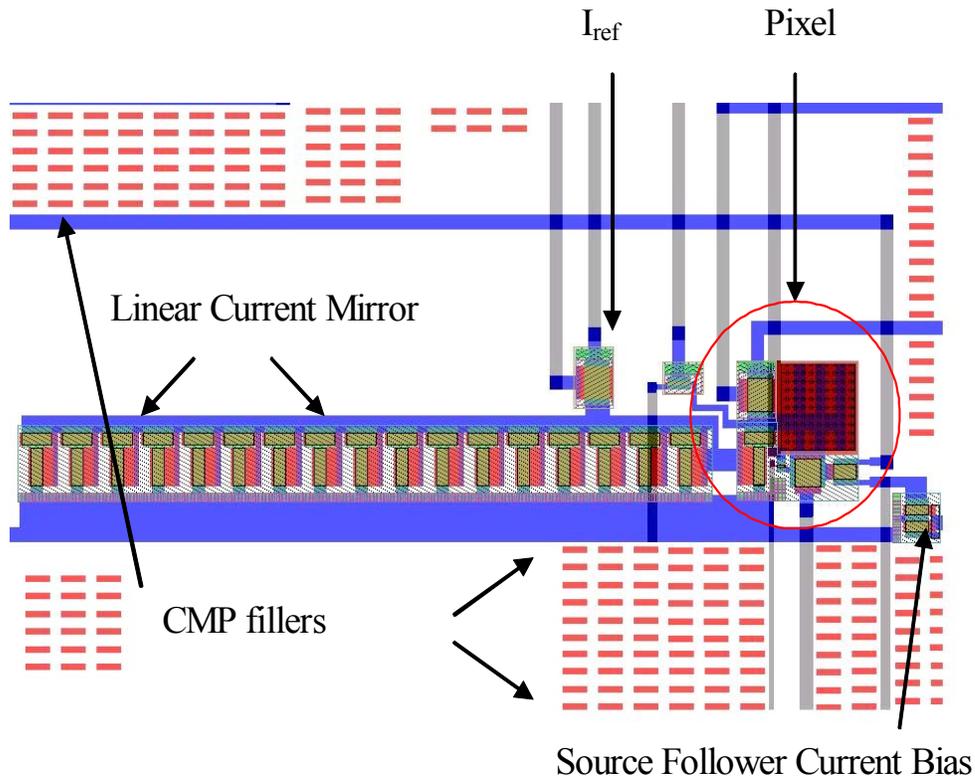


Figure 4.3: Enlarged pixel section and associated circuitry

Figure 4.4 shows an improved design over Figure 4.3 by implementing a common centroid layout which minimizes drain current mismatch and increases sensitivity of the copied current to be skimmed off in the pixel. The edges of the Figure 4.4 employ dummy self-biased cascode current mirrors, which were electrically disconnected. Their function was to eliminate any edge effects from improper or anisotropic etching [19]. The current mirror array consisted of 61 current mirrors with the skimmer geometrically located in the center to provide an equidistant path for current division.

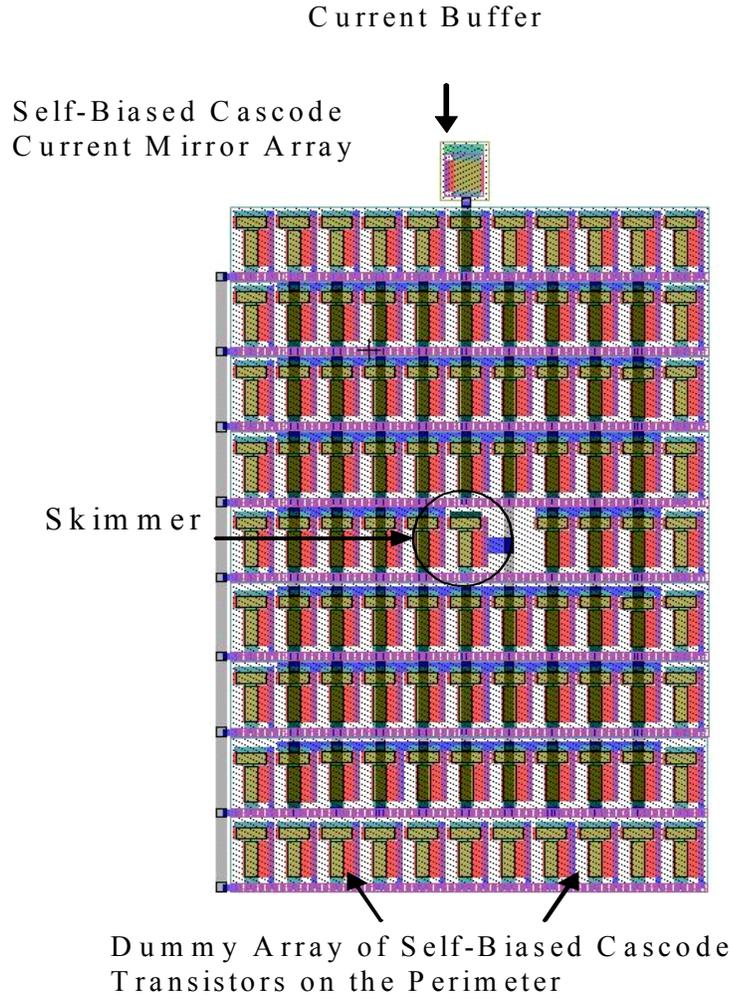


Figure 4.4: Improved layout of self-biased cascode current mirror array

Figure 4.5 shows a layout prototype of a long wave infrared pixel with current skimming capability in the pixel. The prototype pixel height and width measured approximately $57\ \mu\text{m}$ x $54\ \mu\text{m}$ respectfully.

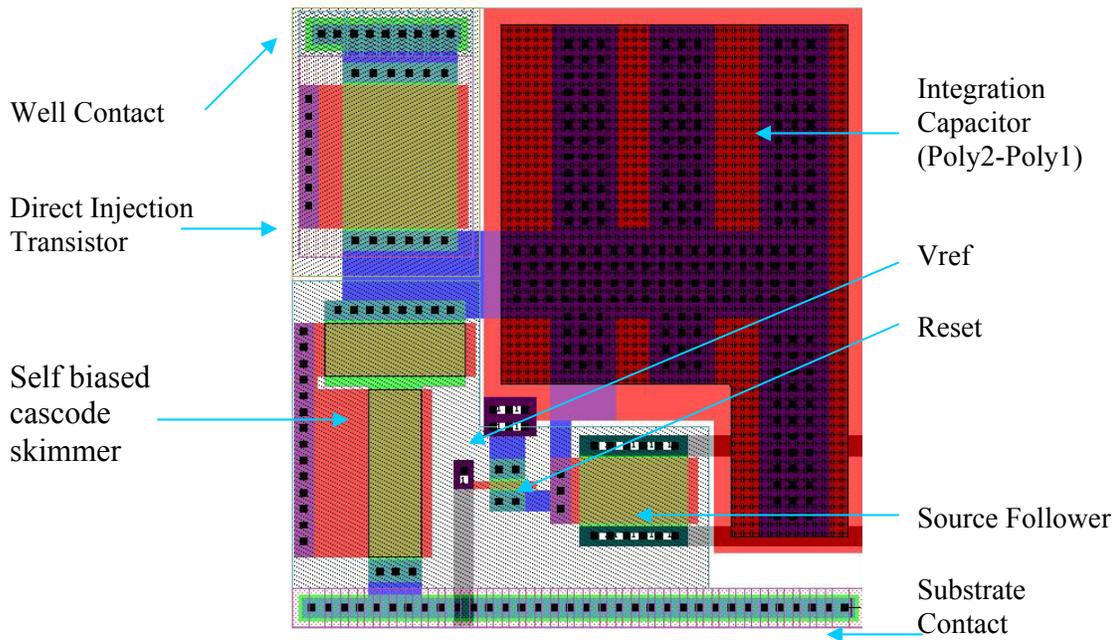


Figure 4.5: Direct injection pixel with incorporated current skimming. Cell dimensions are ($57 \mu\text{m} \times 54 \mu\text{m}$)

Test Results

This test assumed the readout array and detector array were thermally stabilized to a known temperature of 300 K ⁶. Table 4.1 shows a sequence of actions of current skimming actions and the resulting DC pixel output. The pixel reset period of $212 \mu\text{s}$ as a beginning integration time is an arbitrary point. Figures 4.6 through 4.9 graphically illustrate the progression of current skimming.

⁶ These tests assume a bolometer array that is thermo-electrically stabilized to 300 K . Incoming infrared radiation induces tiny changes around the operating point of 300 K . This method of operation incorporates a TEC (Thermo-Electrically Cooled) device to maintain a particular operating temperature. A TEC device increases the power consumption of the array but provides better sensitivity than a TEC less bolometer array

Integration time (s)	Action taken	Measured I_{input} (A)	Measured $I_{reference}$ (A)	Measured I_{skim} (A)	Measured I_{Cint} (A)	Current Skimming %	Pixel output (V)
212 μ s	Set integration time	20 nA	79 nA	4.66 nA	15.34 nA	23%	2.4 V
212 μ s	Increase skimming to 78.5 %	20 nA	267 nA	15.7 nA	4.3 nA	78.5%	680 mV
212 μ s	Increase skimming to 98%	20 nA	335 nA	19.7 nA	300 pA	98 %	\approx 100 mV
10 ms	Extend integration time	20 nA	335 nA	19.7 nA	300 pA	98%	2.5V

Table 4.1: Current skimming sequence

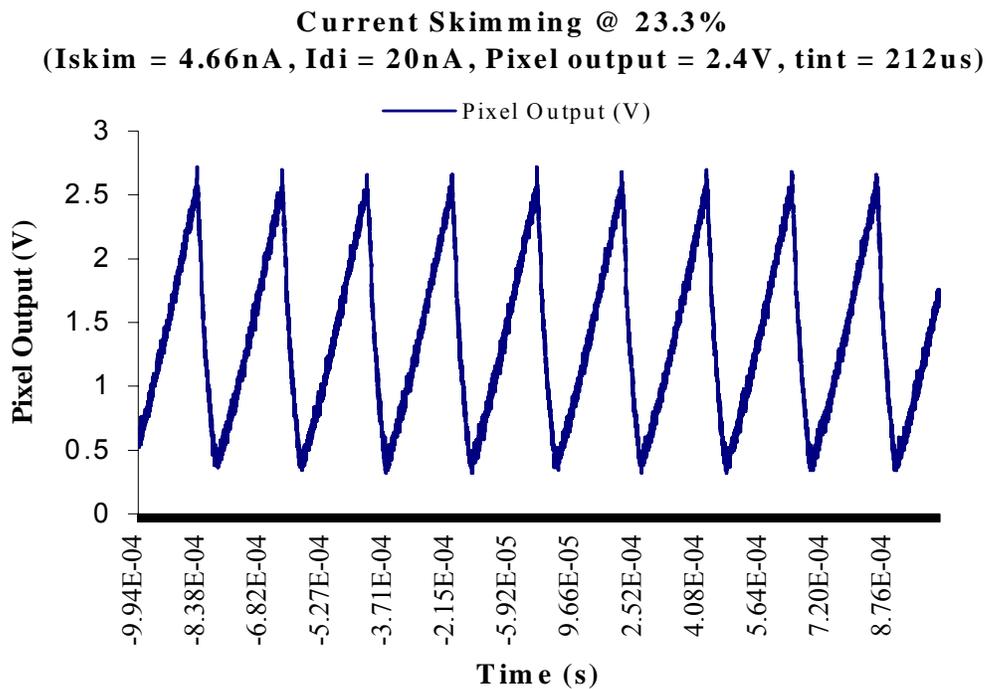


Figure 4.6: Measured DC signal at 23% current skimming

Figure 4.6 shows integrated DC charge in the form of voltage as seen at the pixel source follower output. Initially, the pixel clock was set at 212 μ s as a reference point for demonstrating the current skimming function.

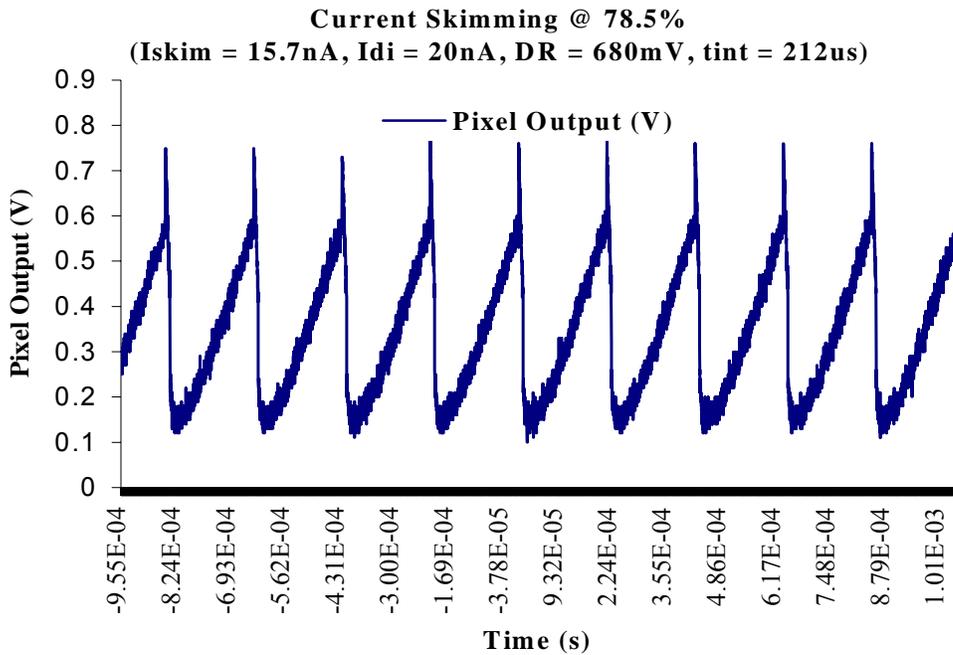


Figure 4.7: Measured DC signal at 78.5% current skimming

As the skimming current increases, the pixel output decreases in magnitude as seen in Figure 4.7. The spike in voltage seen in Figure 4.7 is due to the pixel rise and fall times set in the Labview pixel timing program. The jagged appearance in the signal output is essentially due to temporal noise from the entire system. Since noise was not a main focus in this thesis it is worth while to mention. In Figure 4.8, a DC signal level is present as a result of a voltage reference placed in the pixel. The reference was supplied externally. This reference was implemented to help raise the DC signal level at the source follower output to prevent any subthreshold conduction. The reference was also used to help determine a known calibration point to examine the integrated DC background output signal. The DC signal for this current skimming level of 98% is approximately 100 mV seen in Figure 4.8. A percentage of DC current (98%) is being subtracted off by

the self-biased cascode and the residual current integrating on the integration capacitor is greatly reduced for a fixed integration time of 212 μs . For this particular case, 19.7 nA is being skimmed off from an available 20 nA; therefore approximately 300 pA is integrating on the integration capacitor. Ideally, this 300 pA would represent a detector signal.

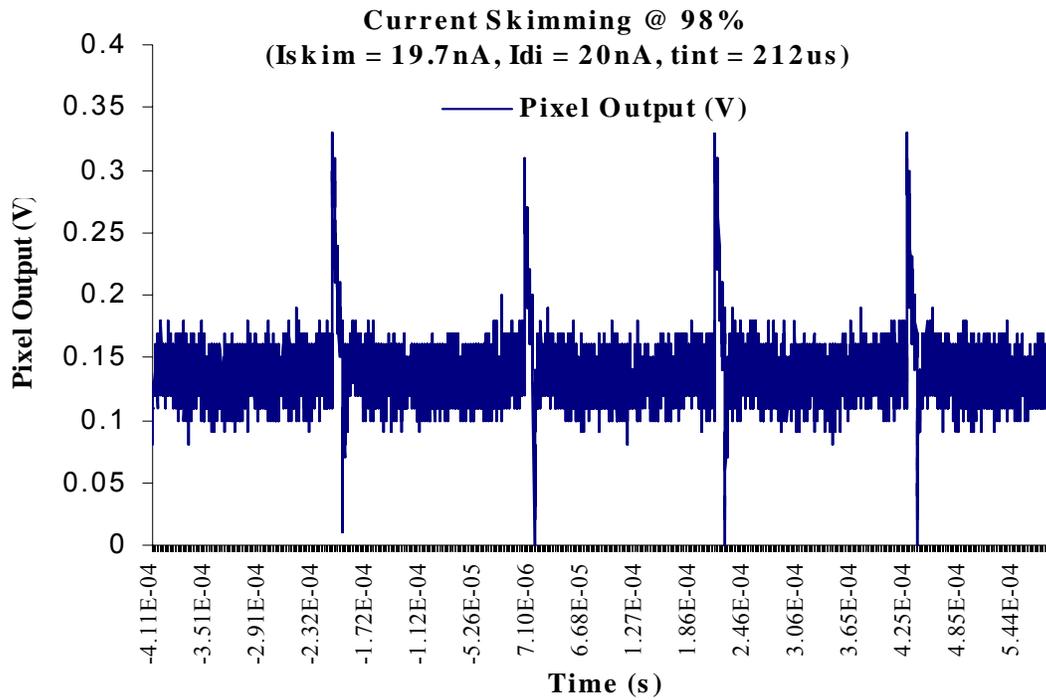


Figure 4.8: Measured DC signal at 98% current skimming

Figure 4.9 illustrates the fundamental goal of this thesis research, to be able to skim off the DC pedestal and to increase the integration times. Though this seems like a simple test of current nodal analysis, this example fundamentally tests output conductance levels from the current skimming transistors presented to the integration node.

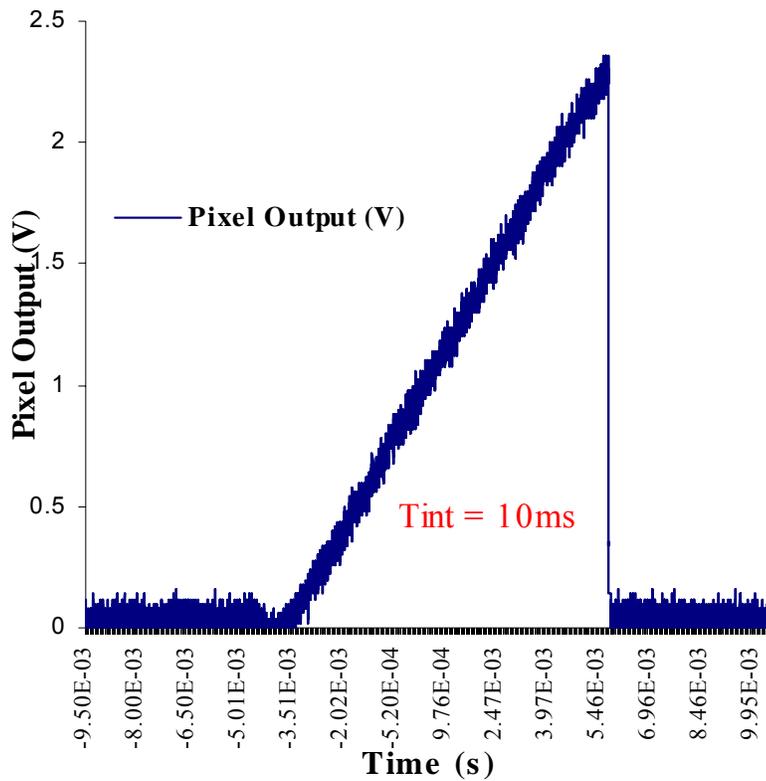


Figure 4.9: Measured DC signal after integration time increase while current skimming

IRCHIP2

Chip Description & Function

Figure 4.10 shows IRCHIP2, which consisted of MOS transistors and self-biased cascode transistors. The purpose of the test chip was to characterize the I-V output characteristics for MOS and self-biased cascode transistors, calculate the output conductance, and calculate the Early voltage in subthreshold [18] to first order (refer to 3.1) by dividing the saturation current by the measured output conductance. The Early voltage measurements correspond to measured saturation current, I_{sat} , of 16.6 nA and a output saturation voltage, V_{dsat} , of 204 mV. Early voltages were measured and compared to transistor length and device area as a measure of predicted output conductance performance for the given bias level [13]. The design goal was to study the relationship between increased device length, output conductance, area, and Early voltage.

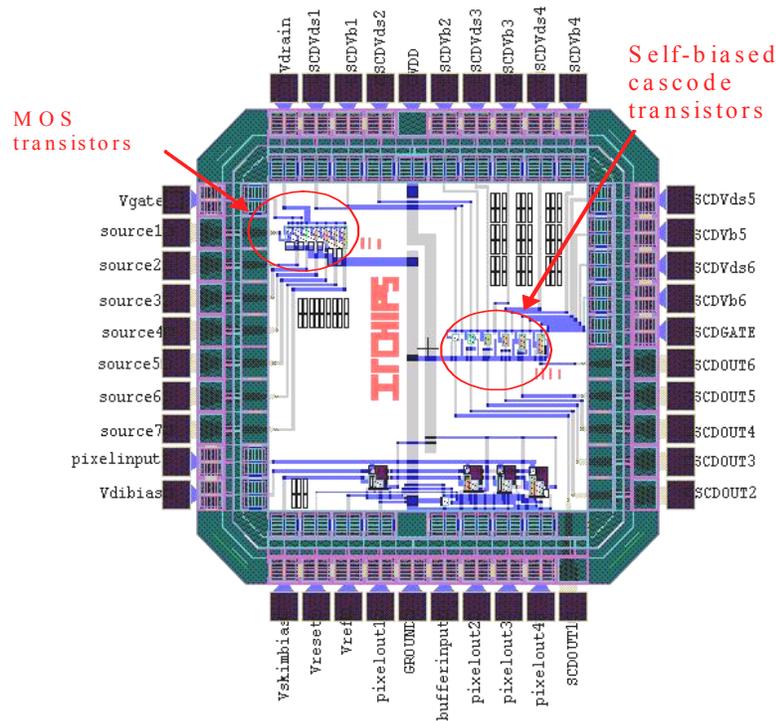


Figure 4.10: IRCHIP2 test chip on MOSIS run T44L (AMI 0.5 μm)

Test Results

Figure 4.11 illustrates that for relative areas, the MOS transistor area exhibits a higher output conductance than the self-biased cascode. To attain self-biased cascoding action, the minimum dimensions are shown in Table 4.2 for SCFET1.

The channel lengths between the devices are equal. The cascode transistor acts like a shield [10, 12] in subthreshold for the self-biased cascode transistor. As a result, the bottom input transistor essentially acts as the bias transistor. Aside from the reduction in output conductance from the common gate gain of the cascode transistor, the channel length of the bias transistor is largely responsible for controlling the Early voltage and output conductance since it is the only variable changing [5]. Table 4.2 illustrates the gate voltages required to bias both devices with an $I_{\text{sat}} = 16.6 \text{ nA}$ and $V_{\text{sat}} = 204 \text{ mV}$.

Measured self-biased cascode output conductance (A/V)	Self-biased cascode dimensions	V_{gs} (mV)	Measured MOS transistor output conductance (A/V)	MOS transistor dimensions	V_{gs} (mV)
2.6089E-10	SCFET1 = 13.05u/4.95u Mb = 4.95u/4.95u	578	4.93E-10	FET1 = 5.1u/4.95u	576
2.4000E-10	SCFET2 = 13.05u/4.95u Mb = 4.95u/9.9u	603	3.78E-10	FET2 = 5.1u/9.9u	593
2.4097E-10	SCFET3 = 13.05u/4.95u Mb = 4.95u/15.6u	620	2.95E-10	FET3 = 5.1u/15.6u	612
2.2201E-10	SCFET4 = 13.05u/4.95u Mb = 4.95u/19.5u	630	2.61E-10	FET4 = 5.1u/19.5u	624
2.2504E-10	SCFET5 = 13.05u/4.95u Mb = 4.95u/27u	645	2.64E-10	FET5 = 5.1u/27u	639
2.3000E-10	SCFET6 = 13.05u/4.95u Mb = 4.95u/37.5u	656	2.60E-10	FET6 = 5.1u/37.5u	656

Table 4.2: Gate bias levels required for $I_{\text{sat}} = 16.6 \text{ nA}$ and $V_{\text{sat}} = 204 \text{ mV}$ while increasing aspect ratios

Output Conductance versus Device Area

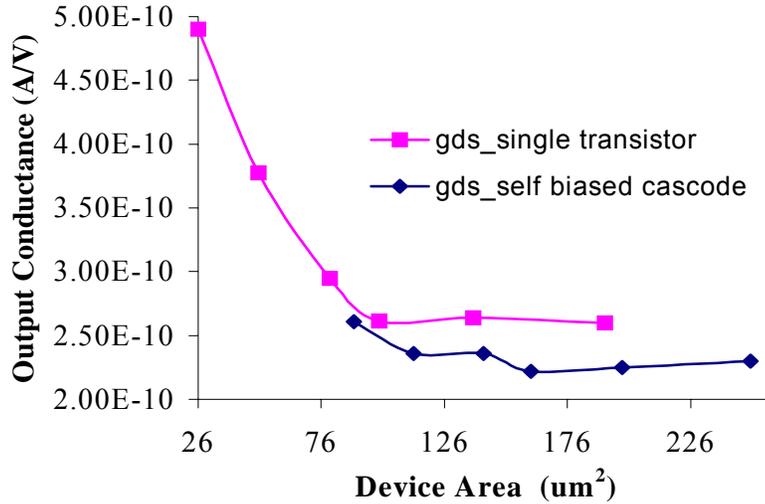


Figure 4.11: Measured device output conductance versus area at $I_{\text{sat}} 16.6$ nA and $V_{\text{sat}} = 204$ mV

An explanation for the slight increase in output conductance in Table 4.2 and seen through the graphs in this thesis, is the device's gradual transitioning from subthreshold to above threshold operation. As device lengths are increased for both the MOS transistor and bias transistor (self-biased cascode) the required gate voltage must be increased to obtain equal saturation currents. The threshold voltage used in the model was approximately 670 mV. The threshold voltage reported from the parametric results from the test chip was approximately 611 mV. Therefore, it is no wonder why we see an increase in output conductance from Table 4.2. Though the experimental data supports the goals of this thesis, a slightly lower saturation current would eliminate this apparent

increase output conductance for the larger devices. In retrospect, an experiment to determine the actual threshold voltages would prove beneficial to know where to set the proper bias points.

The values for Early voltage in subthreshold (refer to 3.1) were experimentally determined to first order [5]. Table 4.3 summarizes the Early voltages at a measured saturation current of 16.6 nA and drain saturation voltage of 204 mV along with the output conductance compared to the device area. Figure 4.12 shows the increase in Early voltage with device area.

Measured g_{ds} of self-biased cascode (A/V)	Simulated g_{ds} of self-biased cascode (A/V)	Self-Biased Cascode Area (μm^2)	Early Voltage (V)	Measured g_{ds} of MOS transistor (A/V)	Simulated g_{ds} of MOS transistor (A/V)	MOS Transistor Area (μm^2)	Early Voltage (V)
2.61E-10	5.02E-10	89.1	63.63	4.93E-10	9.54E-10	26.01	33.88
2.36E-10	9.94E-11	113.6025	70.34	3.78E-10	6.89E-10	50.49	43.96
2.36E-10	8.93E-11	141.8175	70.34	2.95E-10	5.38E-10	79.56	56.31
2.22E-10	8.89E-11	161.1225	74.77	2.61E-10	4.73E-10	99.45	63.53
2.25E-10	9.04E-11	198.2475	73.76	2.64E-10	3.92E-10	137.7	62.88
2.30E-10	9.32E-11	250.2225	72.17	2.60E-10	3.86E-10	191.25	63.88

Table 4.3: Output Conductance versus device area with corresponding Early voltages

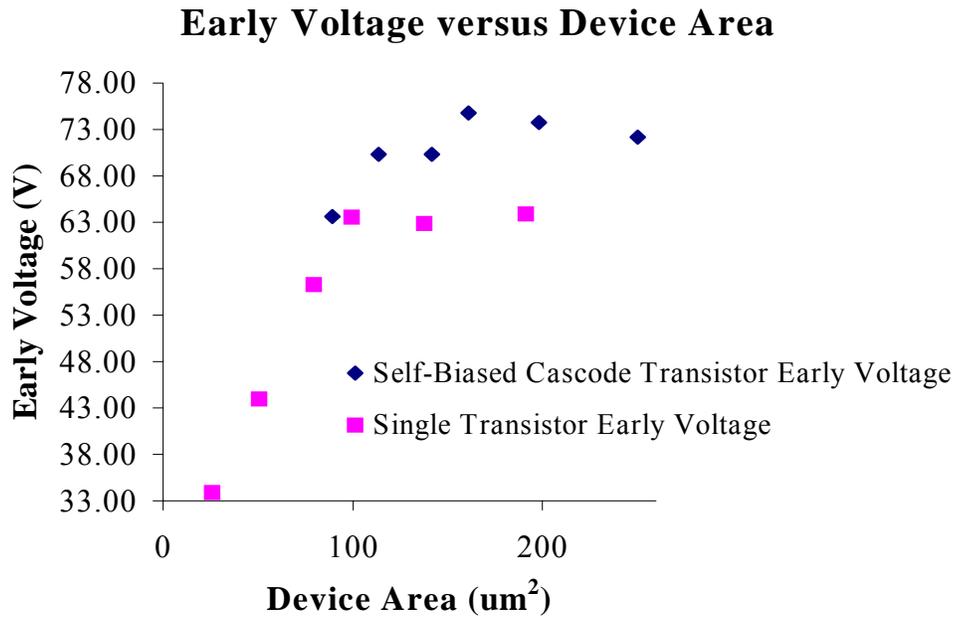


Figure 4.12 Early voltage versus device area

IC Test Chip Design	Chip Feature	Function	Test Result
IRCHIP1 (MOSIS run T3AJ)	54 μm x 57 μm prototype direct injection pixel with associated bias circuitry	DC bias pedestal removal employing the function of current skimming	Achieved integration times from 50 μs to 10 ms. The long integration time goal was achieved.
IRCHIP2 (MOSIS run T44L-BF)	MOS transistor	I-V, output conductance versus, device area, length, and aspect ratios	Determined that the output conductance was too high for DC bias pedestal removal as a result of the Early effect
IRCHIP2 (MOSIS run T44L-BF)	Self-biased cascode transistor	I-V, output conductance versus, device area, length, and aspect ratios	Achieved lower output conductance over the MOS transistor skimmer and virtually eliminated the Early effect.

Table 4.4 Test chip summary

Appendix A:

Uncooled Thermal Imaging

Background

Minimizing power consumption with reduced size and weight, uncooled (*requires no cooling stage*) thermal imaging systems offer a new technological advantage with equal performance to current state of the art cooled thermal imaging systems. Cooled systems are much heavier and require cooling apparatus (*usually to 77 K*) to keep the power consumption to reasonable levels while maintaining high performance thermal imaging. Feeling heat waves emanating from hot objects without seeing any visible light gave clues to early scientists that light is a form of radiation and exists beyond our eye's response range. These heat waves emanating from a recently extinguished fire, a hot plate, or molten iron ore indicated the *emissive* nature of "*invisible*" (infrared) light [20]. *Visible images* are a result of an external radiation source (e.g. *sun light*), which varies in reflectivity across a given scene. For example, the visible "green light" has a wavelength of 510 nm (which is also approximately the peak emission wavelength of the sun). Some tree leaves appear green because the tree leaves absorb all of the other colors in the visible spectrum except green; the 510 nm green wavelength is reflected. In contrast, *thermal images* (heat) are formed by the variance in the quantity of passively emitted radiation from objects [20]. The laws of thermodynamics state that all material bodies *spontaneously* absorb and radiate electromagnetic radiation. Uncooled detectors operate by *converting* absorbed infrared photons into heat which in turn exhibits a change in some measurable property that coincides with a change in temperature of the sensitive

element [21]. Uncooled detectors in this thesis integrate wavelengths from $8\ \mu\text{m} - 14\ \mu\text{m}$, which is considered the *long wave* infrared region. Terrestrial objects with temperatures typically at 300 K have peak long wave infrared photon absorption at approximately $10\ \mu\text{m}$. Since the peak photon absorption level (for the long wave region) occurs at a wavelength of $10\ \mu\text{m}$ in the infrared spectrum (approximately $7\ \mu\text{m}$ to $30\ \mu\text{m}$) and the integrated photon radiation over the long wave infrared region is approximately one third of the total infrared spectrum, it is apparent why the long wave infrared region is preferred for target identification and recognition. Since most of the terrestrial objects in the scene tend to have the same background temperature, the difference in photon emission by the various objects is quite small, often less than 1 % [21]. The low contrast infrared scene therefore requires extremely sensitive detectors.

Military and Commercial Developments

Considerable research in uncooled imaging systems, including sensing materials, electrical readout, and system packaging, have lead to the most prominent areas of bolometer materials research for long wave infrared detectors. These are 1) ferroelectric and pyroelectric bolometry and; 2) resistive bolometry [21]. *The term bolometer refers to an instrument for measuring minute quantities of electromagnetic radiation.* A “bolometer detector” typically implies a resistive device. The physical behavior of the bolometer incorporates a temperature increase from the absorption of long wave infrared photons which cause a change in electrical resistance. A resistive bolometer, which is the detector of choice for this study, is also defined as a *temperature sensitive resistor*. Resistive bolometer analysis assumes that a temperature increase as a result of some long wave infrared photon absorption is small enough so that the resistance change is linear

with the change in temperature [22]. Figure A.1 displays bolometer material's resistance as a function of temperature.

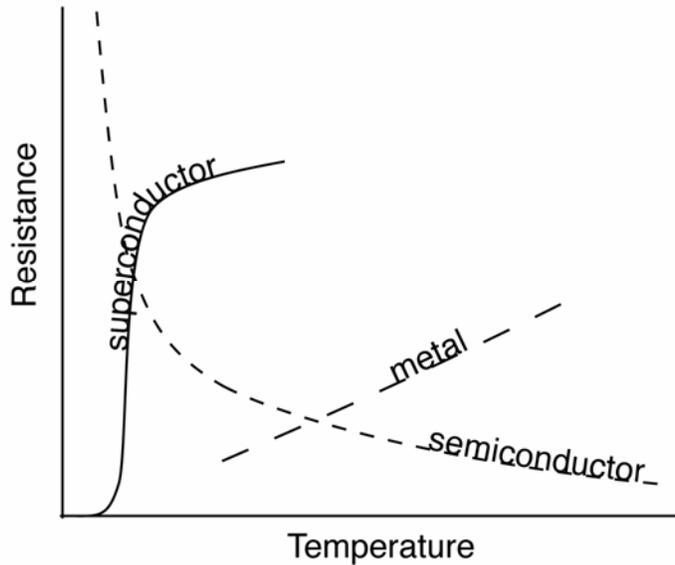


Figure A.1: Resistance of superconductive, metal, and semiconductor materials as a function of temperature

In most instances, the sensor material is comprised of a thin metal or semiconductor film suspended over the top surface of the readout circuitry to provide excellent thermal isolation and minimize thermal conductance to the surroundings. Thermal detector performance improves with increased thermal isolation while assuming also there is a reduction in thermal mass of the bolometer conducting legs [22]. The principal heat loss mechanism occurs through the conducting support legs. The thin film temperature rises when radiation is absorbed by the detector element. With a rise in detector temperature, the resistance either increases (if the sensing film is a metal) or decreases (if it is a semiconductor film). The opposite effect occurs in the absence of radiation; as the detector temperature decreases, the resistance of the metal film decreases

and the resistance of the semiconductor film increases [22]. For the remainder of this thesis, characterization of the CMOS readout process will focus only on the semiconductor resistive bolometric detector.

Efforts began in the mid 1970's to create (solid-state) room temperature 2-D imaging arrays for both military and commercial applications. In 1983 Honeywell reported vanadium oxide (VO_x) bolometric arrays implementing solid-state 2-D readout. This was considered one of the first (silicon) MEMS devices (*Micro-Electro-Mechanical System*), which promised to offer a new era of low-cost monolithic uncooled imaging arrays. Implementing silicon micro-machining to achieve roughly a 1 μm (suspended by two mechanical legs) height over the substrate below, offered the highest thermal isolation attainable thus leading to high performance arrays [4]. Throughout the 1970's and 1980's, most of this research was classified under Department of Defense guidelines for the military. The US Army Night Vision Laboratory (now NVESD) and the Defense Advanced Research Project Agency (DARPA) saw a great advantage for developing potentially low-cost monolithic uncooled infrared focal plane arrays. The transition from bump bonding the detector array to the readout to a monolithic approach improved both the cost and yield of the array.

An important consideration that allowed uncooled infrared imaging to flourish from the 1980's, 1990's, and present was the rapid improvement of silicon process technologies (e.g. *Moore's Law*). CMOS, rather than mature bipolar readouts provided more cost-effective arrays with higher overall performance advantages (e.g. *lower power consumption*). Today, advanced BiCMOS (a process which incorporates bipolar and CMOS devices) processes are expensive and require several additional mask steps. The

chief advantages for CMOS relative to standard bipolar and BiCMOS for uncooled applications are: 1) increased cost effectiveness; 2) greater availability; 3) higher yield; and 4) well defined process parameters for modeling and simulation. While the industry standard is currently CMOS, bipolar or BiCMOS readouts remain possible for future niche applications. Moore's Law has scaled the device dimensions to sub-micron levels and today 1000 x 1000 (typically considered *high definition imaging*) arrays or greater are realizable. Considerable advancements in MEMS and material science have provided extreme precision and high performance uncooled infrared focal plane arrays.

The following section explains in detail why and how current skimming implementation will enhance pixel performance. This section's chief aim is to show the reader that the desired signal to be integrated is a very small fraction of the DC background signal and that integrating this tiny current signal (representative of the scene temperature change) for extended integration times, leads to an increased signal-to-noise ratio.

Bolometer Operation

The detector resistance $R_{\text{det}}(T)$ is a function of temperature. Figure A.2 illustrates the basic bolometer architecture which is suspended over a readout input circuit and provides high thermal isolation as a result. Figure A.3a shows a resistive bolometer biased by a constant voltage source V_d , and Figure A.3b shows a resistive bolometer biased by a constant current source I_{det} .

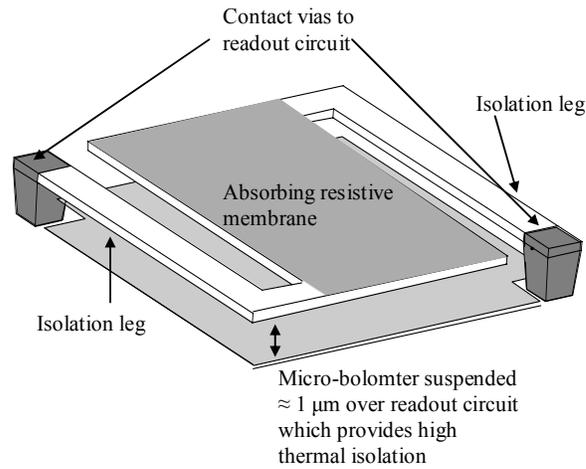


Figure A.2: Basic architecture of a micro-bolometer which is Suspended over the readout circuit

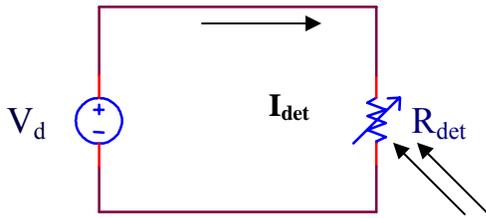
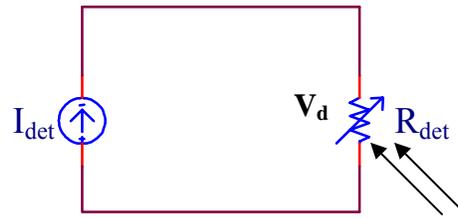


Figure A.3a: Ideal constant voltage bias



A.3b: Ideal constant current bias

Taking the case for no infrared radiation present, the applied bias across the bolometer causes the device to heat (called *joule heating*) up to a temperature above the underlying readout circuit (for example 1 or more increase in K over the ≈ 300 K substrate) when a current flows through the structure and its conducting legs (see Figures A.2 and A.3b). This causes an initial rise in bolometer temperature and also causes the DC bias power dissipation which does not contain any signal of interest. In fact, only when infrared radiation is present are we interested. However, this small infrared signal is

impressed upon a very large DC bias signal and cannot be extracted unless somehow the DC bias pedestal is removed. The following lays the fundamentals behind extracting the small infrared signal from a large DC bias pedestal.

From Figure A.3b the potential drop across the bolometer is $V_d = I_{\text{det}} \times R_{\text{det}}(T)$.

The first order change in detector voltage due to a small change in bolometer temperature ΔT is

$$\Delta V_d = I_{\text{det}} \frac{dR_{\text{det}}}{dT} \Delta T = \frac{V_d}{R_{\text{det}}} \frac{dR_{\text{det}}}{dT} \Delta T = V_d \alpha \Delta T \quad (\text{A.1})$$

where $\alpha = \left(-\frac{1}{R_{\text{det}}} \frac{dR_{\text{det}}}{dT} \right)$, is the equation for the *temperature coefficient of resistance* (or

TCR). TCR gives the percentage change in resistance per degree change in temperature at a particular temperature T. From Figure A.1, the TCR is negative for the semiconductor

bolometer. From Figure A.3a, the current through the bolometer is $I_{\text{det}} = \frac{V_d}{R_{\text{det}}}$. A small

first order change in bolometer current due to a tiny change in bolometer temperature results in (A.2).

$$\Delta I_{\text{det}} = \frac{d}{dT} \left(\frac{V_d}{R_{\text{det}}} \right) \Delta T = -\frac{V_d}{R_{\text{det}}^2} \frac{dR_{\text{det}}}{dT} \Delta T = -I_{\text{det}} \alpha \Delta T \quad (\text{A.2})$$

Note (A.2) is negative because of the simple derivative (quotient rule). The goal now is to determine the small temperature fluctuation in the bolometer, ΔT in (A.1) and (A.2), caused by a heat source (from a given scene) impressed upon the absorbing membrane surface (Figure A.2) of the bolometer sensor. Equation (A.2) is the central focus of this thesis, which represents the signal of interest (information bearing component), a fractional portion of the total DC current, $I_{\text{tot}} = I_{\text{det}} + \Delta I_{\text{det}}$. We are not

interested in I_{det} and therefore would like to subtract (or skim) this component. Consider the heat flow equation seen in (A.3).

The bolometer is governed by the 1st order differential heat equation seen in (A.3), which is a consequence of energy conservation. We must solve (A.3) in order to determine ΔT in (A.1) and (A.2) caused by a heat source from a distant scene which appears as a small change in temperature in the bolometer.

$$C_{th} \frac{dT_{\text{det}}}{dt} = -G_{\text{mech}}(T_{\text{det}} - T_{\text{sub}}) + W_s + V_d I_{\text{det}} \quad (\text{A.3})$$

- G_{mech} is the total thermal conductance due to the thin bolometer support legs
- W_s is the net power absorbed by the bolometer due to radiation. In infrared imaging systems, the magnitude of W_s is dependent on camera optics, infrared pass band, detector area, absorption efficiency, and scene temperature variation. $W_s = \eta \frac{1}{4F^2} A_{\text{det}} \frac{dP_s}{dT_s} \Delta T_s$, where $\frac{dP_s}{dT_s} \Delta T_s$ is the power emitted from the scene for a small change in scene temperature around some average background scene temperature (e.g. 300 K).
- T_{det} is the bolometer temperature and T_{sub} is the underlying substrate temperature
- C_{th} is the total heat capacity of the bolometer. The bolometer is composed of layers of individual material each with its own heat capacity
- $V_d I_{\text{det}} = I_{\text{det}}^2 \mathbf{R}(\mathbf{T})$ is the bias power dissipated by the bolometer due to the applied bias. This term introduces a non-linear dependence on current and must be expanded in a Taylor series for linearization and small signal extraction by keeping only the first term and neglecting higher order terms. Thus this signal has no practical information content for the readout to process and is only used to set the DC operating point

The temperature change $\left(\frac{dT_{\text{det}}}{dt} \right)$ in the bolometer material multiplied by its heat

capacity C_{th} is equal to the net energy that flowed into the bolometer structure; hence the total energy impressed upon the absorbing membrane multiplied by the time interval for that energy. Any heat loss mechanisms are offset (or cancelled) by any absorbed infrared

radiation in the absorbing membrane. Thus the goal is to minimize as much as possible any thermal conducting paths which contribute to heat loss so that the *absorbed infrared radiation* alters the stored heat; hence the ΔT as seen in (A.1) and (A.2). The bias power $V_d I_{det} = I_{det}^2 R(T)$ dissipated from the applied bias introduces non-linearity into (A.3) and does not admit closed form solutions. Therefore, (A.3) cannot be solved by ordinary linear methods until the analysis of the bolometer assumes a linear behavior; hence to perform a small signal analysis for changes occurring around some steady state bias power.

The mathematical derivations describing the physics of bolometer operation are not the focus of this thesis. The heat flow process is governed by the first order differential heat equation. In an effort to focus on the important features of readout circuits, the mathematics are kept to a minimum and only used to emphasize the small signal operation around a steady state operating point of the bolometer. The interested reader is referred to comprehensive resources [4, 21, and 22].

Equation (A.3) has an obviously known solution that consists of the homogeneous solution $Ae^{-\frac{t}{\tau}}$ with a fixed initial condition A , thermal time constant $\tau = \frac{C_{th}}{G_{mech}}$, and the sum of the particular solutions which originates from radiation sources, W_s , and the constant $G_{mech}T_{sub}$. The particular solution caused by $G_{mech}T_{sub}$ is T_{sub} . The temperature response in the bolometer from absorbed input infrared radiation, W_s , follows a simple first order low pass filter with 3_{dB} cutoff frequency of $\omega_c = \left(\frac{1}{\tau}\right)$. The temperature response caused by W_s (as a function of angular frequency) is seen in equation (A.4) assuming that the input infrared signal, W_s , is a sufficiently small

signal in magnitude (e.g. small signal changes in the steady state) which causes small temperature changes and small signal voltage or current changes as seen in (A.1) and (A.2).

$$\Delta T \equiv T(\omega) = \frac{W_s(\omega)}{G_{mech}} \frac{1}{1 + j\omega\tau} \quad (\text{A.4})$$

Thus a small signal change in the bolometer due to a small temperature change in the bolometer which is directly related to the scene temperature change for the circuit configurations of Figures A.3a and A.3b are respectively seen in (A.5).

$$\Delta V_d = -V_d \alpha \left[\frac{\overbrace{W_s(\omega)}^{\Delta T}}{G_{mech}} \frac{1}{1 + j\omega\tau} \right]; \quad \Delta I_{det} = I_{det} \alpha \left[\frac{\overbrace{W_s(\omega)}^{\Delta T}}{G_{mech}} \frac{1}{1 + j\omega\tau} \right] \quad (\text{A.5})$$

Take for example the following situation: we have a 50 μm x 50 μm pixel with $G_{mech} \approx 10^{-7}$ W/K, no transmission loss, and F/1 optics [21]. With a one degree (1000 mK) scene temperature change (*which assumes the scene is a perfect black body*⁷) and a pass band from 8 μm to 12 μm , we expect approximately a 10 mK change in bolometer temperature (*the ratio of scene to bolometer change is 100:1*). If the TCR = -2.5% and our desired resolution of scene temperatures is 20 mK, we see a 200 μK change in bolometer temperature. Seen in (A.6) is the ratio of a small signal current or voltage change to an applied voltage or current bias.

$$\frac{\Delta V_d}{V_d} = \alpha \Delta T; \quad \frac{\Delta I_{det}}{I_{det}} = -\alpha \Delta T$$

(A.6)

⁷ A blackbody refers to an object that “perfectly” absorbs all incident radiation upon it and “perfectly” emits radiation energy

Equation (A.6) also indicates that temperature coefficient of resistance multiplied by the small change in bolometer temperature due to small change in scene temperature is

$$|\alpha\Delta T| = (0.025)(2 \times 10^{-4}) \text{ or } 5 \text{ parts per million.}$$

Take the situation for an uncooled bolometer operation at 300 K where the DC bias current ≈ 20 nA. Given the above information and using (A.2), we find that the change in current as a result of a 200 μ K change in bolometer temperature with a 20 mK desired resolution will have a small signal change in current of $\Delta I_{\text{det}} = (-20 \text{ nA}) \times \left(\frac{-0.025}{\text{K}} \right) \times (200 \mu\text{K}) = 100 \text{ fA}$. Thus the signal we want to integrate, the change in bolometer current, is 2.0×10^5 smaller than the DC background. As a note to the reader, the direct injection (input) transistor must operate in the subthreshold state to accommodate such small magnitude currents [3, 10, and 13].

To reiterate, the term I_{det} has no practical use for signal processing and must be subtracted. ΔI_{det} is the most important signal and contains quantitative scene temperature changes represented as changes in bolometer resistance. This thesis introduces a way to subtract I_{det} and thus integrating ΔI_{det} over an extended integration time, which ultimately improves the signal-to-noise ratio. This DC current subtraction method is known as *current skimming*.

Continuously “DC” Biased Bolometer Operation

The detector is continuously biased so that a stable operating point is reached. Small temperature fluctuations in the observed scene induce equivalent temperature fluctuations around the bolometer operating point set by DC bias across the bolometer. We assume that the substrate which houses the readout circuitry is thermally stabilized to

some known temperature reference we will call $T_{\text{sub}} (\approx 300 \text{ K})$. *The following situation illustrates typical DC bias conditions.* With no radiation present, the initial DC current that flows through the bolometer heats up the resistor (*joule heating*), altering the resistance and raising the bolometer temperature to T_{det} . Therefore without absorbed infrared radiation, we have an initial temperature difference $\Delta T_1 = T_{\text{det}} - T_{\text{sub}}$. Introducing infrared radiation will further raise bolometer temperature to $\Delta T_3 = \Delta T_2 - \Delta T_1$. Detector resistances (in this thesis) are valued on the order of 10-60 $\text{M}\Omega$ with typical detector biases from 1-3V. Typical current bias ranges from approximately 16 nA to 1 μA . Thus, power dissipation per-pixel is between 16 nW to 3 μW for typical array sizes of 120 x 160 and 320 x 240. In this thesis, typical bias current ranges are from 1 nA to 50 nA with approximately 1 nW to 50 nW power dissipation per pixel.

Figures A.3 and A.4 illustrate scanning electron microscopy photographs of the bolometer structure.

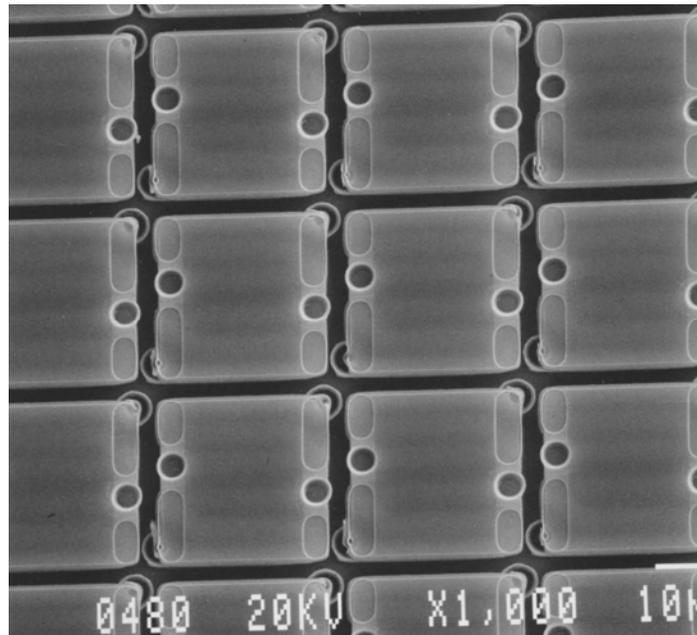


Figure A.4: 25 μm x 25 μm microbolometer array

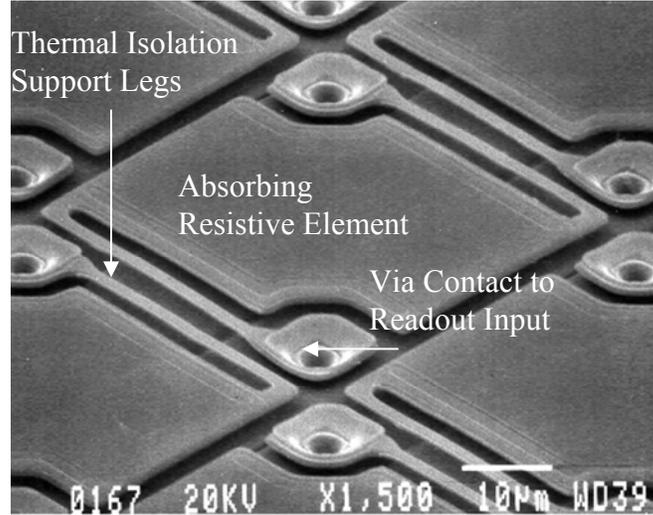


Figure A.5: Uncooled pixel element



Figure A.6: Uncooled imagery from a 120 x 160 long wave infrared focal plane array

In summary, the chapter gave background on uncooled thermal imaging. Next, we discussed bolometer operation describing the importance of the tiny change in bolometer current signal, which related to a scene temperature change and also showed the DC signal carried no practical information. Finally, we explained the definition of DC bias

and described briefly amorphous silicon as the sensing material. The next chapter introduces the readout process and gives background on the different methods of processing the integrated signal from the detector.

Conclusion

In conclusion, techniques for long wave infrared DC pedestal removal have been presented. Current skimming and charge subtraction are two effective means of eliminating the DC background signal to enable the read-out pixel to integrate for an extended period of time to reduce integrated noise bandwidth (of the bolometer) and thus to improve the signal-to-noise ratio.

Future considerations for this study include the design of an adaptive skimming pixel, which would enable each pixel individually to self-calibrate itself for each frame. The challenges facing DC pedestal removal schemes for continuously biased uncooled bolometer arrays are available pixel area, power constraints, and noise mechanisms. To achieve low-cost and high-density (*continuously biased*) uncooled focal plane arrays for increased targeting ranges, current pixel sizes must be less than $28\ \mu\text{m} \times 28\ \mu\text{m}$. Therefore, considerable current skimming research must be focused on achieving very low output conductance in the smallest available area for the self-biased cascode composite transistor. Because of the highest capacitance per unit area from a MOS capacitor, charge subtraction may prove a more effective “skimmer” at smaller pixel designs than the self-biased cascode composite transistor. This thesis concludes with the accomplished objectives.

- Developed and tested successfully appropriate scaling techniques for self-biased cascode transistors.
- Designed a novel long wave infrared per-pixel current skimming readout specifically for continuously bias uncooled bolometer focal plane arrays.
- Achieved greater than 8 ms integration time in one of the first reported *per-pixel current skimming* readout approaches designed and intended for continuous bias uncooled infrared focal plane arrays.

Appendix B:

Analog Layout Design Guide

The following suggestions from [19] are intended to maximize performance for analog design.

- Devices to be matched must have the same structure.
- Devices should maintain the same operating temperature
- Devices must have same physical size; (e.g. capacitors must have the same aspect ratio and transistors have the same W and L).
- Layout must incorporate a minimum distance rule to “take advantage of spatial correlation of fluctuating physical parameters.”
- Designs should implement common-centroid geometries used to cancel parameter gradients.
- Identical orientation eliminates “dissymmetries” as a result of anisotropic etching in the manufacturing process. In particular, the channel currents (I_{ds}) are parallel to achieve optimal matching.
- Devices must have the same physical surroundings in the layout. For example a row of current mirrors will have dissimilar currents from the transistors on the ends.
- Analog devices must use non-minimum geometries. This helps to reduce the “effect of edge fluctuations and to improve spatial averaging of fluctuating parameters.”

Appendix C:

BSIM3v3 MOSFET Models

Simulation Models:

*These parameters are extracted from the process corner wafers that are provided by AMI

* DATE: May 22/02

* Tech: AMI_C5N

* LOT: T22Y_TT (typical)

WAF: 3104

* Temperature_parameters=Optimized

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 49
+XJ = 1.5E-7           NCH = 1.7E17       TOX = 1.39E-8
+K1 = 0.8351612        K2 = -0.0839158      VTH0 = 0.6696061
+K3B = -7.6841108      W0 = 1E-8           K3 = 23.1023856
+DVT0W = 0             DVT1W = 0           NLX = 1E-9
+DVT0 = 2.9047241      DVT1 = 0.4302695    DVT2W = 0
+U0 = 458.439679       UA = 1E-13          DVT2 = -0.134857
+UC = 1.629939E-11     VSAT = 1.643993E5   UB = 1.485499E-18
+AGS = 0.1194608       B0 = 2.674756E-6    A0 = 0.6103537
+KETA = -2.640681E-3   A1 = 8.219585E-5    B1 = 5E-6
+RDSW = 1.387108E3     PRWG = 0.0299916    A2 = 0.3564792
+WR = 1                WINT = 2.472348E-7  PRWB = 0.0363981
+XL = 0                XW = 0              LINT = 3.597605E-8
+DWB = 5.306586E-8     VOFF = 0            DWG = -1.287163E-8
+CIT = 0               CDSC = 2.4E-4        NFACTOR = 0.8365585
+CDSCB = 0             ETA0 = 0.0246738    CDSCD = 0
+DSUB = 0.2543458      PCLM = 2.5945188    ETAB = -1.406123E-3
+PDIBLC2 = 2.311743E-3 PDIBLCB = -0.0272914 PDIBLC1 = -0.4282336
+PSCBE1 = 5.598623E8   PSCBE2 = 5.461645E-5 DROUT = 0.7283566
+DELTA = 0.01          RSH = 81.8          PVAG = 0
+PRT = 8.621           UTE = -1            MOBMOD = 1
+KT1L = -2.58E-9       KT2 = 0              KT1 = -0.2501
+UB1 = -4.8E-19        UC1 = -7.5E-11      UA1 = 5.4E-10
+WL = 0                WLN = 1              AT = 1E5
+WWN = 1               WWL = 0              WW = 0
+LLN = 1               LWL = 0              LL = 0
+LWL = 0               CAPMOD = 2           LWN = 1
+CGDO = 2E-10          CGSO = 2E-10        XPART = 0.5
+CJ = 4.197772E-4      PB = 0.99            CGBO = 1E-9
+CJSW = 3.242724E-10  PBSW = 0.1           MJ = 0.4515044
+CJSWG = 1.64E-10     PBSWG = 0.1          MJSW = 0.1153991
+CF = 0                PVTH0 = 0.0585501   MJSWG = 0.1153991
+PK2 = -0.0299638     WKETA = -0.0248758  PRDSW = 133.285505
+AF = 1                KF = 0)              LKETA = 1.173187E-3
*
```

```
.MODEL CMOSP PMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 49
+XJ = 1.5E-7           NCH = 1.7E17       TOX = 1.39E-8
+K1 = 0.5553722        K2 = 8.763328E-3    VTH0 = -0.9214347
+K3B = -0.6487362      W0 = 1.280703E-8    K3 = 6.3063558
+DVT0W = 0             DVT1W = 0           NLX = 2.593997E-8
+DVT0 = 2.5131165      DVT1 = 0.5480536    DVT2W = 0
+U0 = 212.0166131      UA = 2.807115E-9    DVT2 = -0.1186489
+UC = -5.82128E-11     VSAT = 1.713601E5   UB = 1E-21
+AGS = 0.1328608       B0 = 7.117912E-7    A0 = 0.8430019
+KETA = -3.674859E-3   A1 = 4.77502E-5     B1 = 5E-6
                        A2 = 0.3
```

+RDSW	= 2.837206E3	PRWG	= -0.0363908	PRWB	= -1.016722E-5
+WR	= 1	WINT	= 2.838038E-7	LINT	= 5.528807E-8
+XL	= 0	XW	= 0	DWG	= -1.606385E-8
+DWB	= 2.266386E-8	VOFF	= -0.0558512	NFACTOR	= 0.9342488
+CIT	= 0	CDSC	= 2.4E-4	CDSCD	= 0
+CDSCB	= 0	ETA0	= 0.3251882	ETAB	= -0.0580325
+DSUB	= 1	PCLM	= 2.2409567	PDIBLC1	= 0.0411445
+PDIBLC2	= 3.355575E-3	PDIBLCB	= -0.0551797	DROUT	= 0.2036901
+PSCBE1	= 6.44809E9	PSCBE2	= 6.300848E-10	PVAG	= 0
+DELTA	= 0.01	RSH	= 101.6	MOBMOD	= 1
+PRT	= 59.494	UTE	= -1	KT1	= -0.2942
+KT1L	= 1.68E-9	KT2	= 0	UA1	= 4.5E-9
+UB1	= -6.3E-18	UC1	= -1E-10	AT	= 1E3
+WL	= 0	WLN	= 1	WW	= 0
+WWN	= 1	WWL	= 0	LL	= 0
+LLN	= 1	LW	= 0	LWN	= 1
+LWL	= 0	CAPMOD	= 2	XPART	= 0.5
+CGDO	= 2.9E-10	CGSO	= 2.9E-10	CGBO	= 1E-9
+CJ	= 7.235528E-4	PB	= 0.9527355	MJ	= 0.4955293
+CJSW	= 2.692786E-10	PBSW	= 0.99	MJSW	= 0.2958392
+CJSWG	= 6.4E-11	PBSWG	= 0.99	MJSWG	= 0.2958392
+CF	= 0	PVTH0	= 5.98016E-3	PRDSW	= 14.8598424
+PK2	= 3.73981E-3	WKETA	= 5.292165E-3	LKETA	= -4.205905E-3
+AF	= 1	KF	= 0)		

Extracted models from run T44L: IRCHIP2

T44L SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```

* DATE: Jul  9/04
* LOT: T44L                WAF: 0102
* Temperature_parameters=Default
.MODEL CMOSN NMOS (
+VERSION = 3.1             TNOM      = 27             LEVEL   = 49
+XJ      = 1.5E-7         NCH     = 1.7E17         TOX      = 1.42E-8
+K1      = 0.8791418     K2      = -0.0928691    VTH0    = 0.6106006
+K3B     = -8.1787847    W0      = 1E-8          K3      = 18.3613087
+DVT0W   = 0             DVT1W   = 0             NLX     = 1E-9
+DVT0    = 3.5655768     DVT1    = 0.3802648    DVT2W   = 0
+U0      = 452.6968866   UA      = 1.406301E-13 DVT2    = -0.0874051
+UC      = 5.36169E-12   VSAT    = 1.802287E5   UB      = 1.618501E-18
+AGS     = 0.1061895     B0      = 2.728576E-6   A0      = 0.5750334
+KETA    = -8.123787E-5  A1      = 4.190554E-4   B1      = 5E-6
+RDSW    = 1.06188E3     PRWG    = 0.0883334    A2      = 0.3323258
+WR      = 1             WINT    = 2.308608E-7 PRWB    = 0.0315574
+XL      = 1E-7         XW      = 0             LINT    = 7.347987E-8
+DWB     = 3.927415E-8  VOFF    = 0             DWG     = -1.605516E-8
+CIT     = 0             CDSC    = 2.4E-4         NFACTOR = 0.4571776
+CDSCB   = 0             ETA0    = 2.176689E-3    CDSCD   = 0
+DSUB    = 0.0553447    PCLM    = 2.4898877    ETAB    = -8.669487E-5
+PDIBLC2 = 2.156583E-3  PDIBLCB = -0.0394428    PDIBLC1 = 1
+PSCBE1  = 6.238215E8   PSCBE2  = 1.760403E-4 DROUT   = 0.9016259
+DELTA   = 0.01        RSH     = 83.8          PVAG    = 0
+PRT     = 0            UTE     = -1.5          MOBMOD  = 1
+KT1L    = 0            KT2     = 0.022         KT1     = -0.11
+UB1     = -7.61E-18   UC1     = -5.6E-11     UA1     = 4.31E-9
+WL      = 0            WLN     = 1             AT      = 3.3E4
+WWN     = 1            WWL     = 0             WW      = 0
+LLN     = 1            LW      = 0             LL      = 0
+LWL     = 0            LWL     = 0             LWN     = 1

```

```

+LWL      = 0                CAPMOD = 2                XPART    = 0.5
+CGDO     = 1.97E-10        CGSO     = 1.97E-10        CGBO     = 1E-9
+CJ       = 4.315315E-4     PB       = 0.9194059       MJ       = 0.4344423
+CJSW     = 3.335714E-10    PBSW    = 0.8             MJSW    = 0.1985616
+CJSWG    = 1.64E-10       PBSWG   = 0.8             MJSWG   = 0.1985616
+CF       = 0                PVTH0   = 0.1570368     PRDSW   = 187.3761409
+PK2      = -0.0254353     WKETA   = -0.0181601     LKETA   = 1.265053E-3
)
*
*
.MODEL CMOSP PMOS (
+VERSION = 3.1                TNOM     = 27                LEVEL    = 49
+XJ      = 1.5E-7            NCH     = 1.7E17            TOX     = 1.42E-8
+K1      = 0.5265664        K2      = 0.0213923        VTH0   = -0.9836276
+K3B     = -0.6532905      W0      = 1E-8             K3      = 4.4911263
+DVT0W   = 0                DVT1W   = 0                NLX     = 1E-9
+DVT0    = 2.6487289       DVT1    = 0.4862165      DVT2W  = 0
+U0      = 222.1424772     UA      = 3.307877E-9     DVT2   = -0.0896609
+UC      = -5.80948E-11    VSAT    = 2E5             UB      = 2.667897E-21
+AGS     = 0.1156322       B0      = 7.044894E-7     A0      = 0.8813584
+KETA    = 4.719307E-4     A1      = 0                B1      = 3.350124E-6
+RDSW    = 3E3             PRWG    = -0.0562354     A2      = 0.3
+WR      = 1                WINT    = 2.962387E-7    PRWB   = -5.560433E-3
+XL      = 1E-7            XW      = 0                LINT    = 9.667582E-8
+DWB     = 1.377762E-8     VOFF    = -0.0788978     DWG     = -3.741786E-8
+CIT     = 0                CDSC    = 2.4E-4           NFACTOR = 0.6687895
+CDSCB   = 0                ETA0    = 0.4372057        CDSCD   = 0
+DSUB    = 1                PCLM    = 2.1801812       ETAB    = -0.0880016
+PDIBLC2 = 3.544969E-3     PDIBLCB = -0.0720123     PDIBLC1 = 0.0430345
+PSCBE1  = 5.329158E9     PSCBE2  = 5E-10           DROUT   = 0.2036798
+DELTA   = 0.01           RSH     = 106.9           PVAG    = 0.2660196
+PRT     = 0                UTE     = -1.5            MOBMOD  = 1
+KT1L    = 0                KT2     = 0.022           KT1     = -0.11
+UB1     = -7.61E-18      UC1     = -5.6E-11        UA1     = 4.31E-9
+WL      = 0                WLN     = 1                AT      = 3.3E4
+WWN     = 1                WWL     = 0                WW      = 0
+LLN     = 1                LW      = 0                LL      = 0
+LWL     = 0                CAPMOD  = 2                LWN     = 1
+CGDO    = 2.72E-10        CGSO    = 2.72E-10        XPART   = 0.5
+CJ      = 7.257637E-4     PB      = 0.9604987       CGBO    = 1E-9
+CJSW    = 3.242689E-10    PBSW    = 0.99             MJ      = 0.4949935
+CJSWG   = 6.4E-11       PBSWG   = 0.99             MJSW   = 0.3345497
+CF      = 0                PVTH0   = 5.98016E-3     MJSWG  = 0.3345497
+PK2     = 3.73981E-3     WKETA   = 3.808346E-3    PRDSW  = 14.8598424
)
*

```

Extracted models from run T3AJ: IRCHIP1 (Not Available from MOSIS)

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