ABSTRACT

Title: COMPOSITE QUANTUM WELL: CO-EXISTENCE OF ELECTRONS AND HOLES

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A field effect transistor is fabricated using a composite quantum well structure consisting of adjacent semiconductor quantum wells, GaSb and InAs, sandwiched by AlSb and GaSb barriers. It is found that with a proper gate bias the concentration of the hole and the electron carriers in this device can be controlled. Properties of this device can be utilized in realizing lateral resonant interband tunneling diodes, single electrons transistors and other interesting quantum devices.

COMPOSITE QUANTUM WELL: CO-EXISTENCE OF ELECTRONS AND HOLES

By

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Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
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2005

Advisory Committee:
Professor Chia-Hung Yang, Chair
Professor Julius Goldhar
Professor Martin Peckerar

Dedication

To my

Family for their support

Friends for their encouragement and help,

Mother Saraswati and Mother India

Acknowledgements

To my Committee, Dr M J Yang, my colleagues and others in AV Williams and LPS

And various others who helped me on different occasions

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1. Introduction

The GaAs/AlGaAs heterojunction is probably the most investigated III–V system. It has not only provided a sample system for studying fundamental semiconductor physics, but has also offered commercial applications. The success of this heterostructure system is in part due to the fact that the GaAs and AlGaAs are almost lattice matched, which makes the growth of device-quality material easier. Another system, including InAs, GaSb, and AlSb, is not nearly as well lattice matched, but it offers other useful and unique properties for device applications.

First, the electron mobility in InAs can be high because of low effective mass, an advantage for high-speed electronic devices. Second, the surface Fermi level is pinned above the InAs conduction band minimum, allowing straightforward formation of ohmic contacts to *n* type InAs. As a result of the aforementioned properties, this system has recently prompted a number of fundamental studies and device demonstrations.

It has been found, from interband transitions on InAs/GaSb superlattices, that the GaSb valence-band maximum, is located about 150 meV above the InAs conduction-band minimum. By suitably controlling the width of the the quantum wells, the position of the lowest electron-subband energy in the InAs quantum well (E_0) and the lowest heavy-hole-subband energy in the GaSb quantum well (HH_0) can be controlled. The difference between E_0 and HH_0 is the effective band gap. This can be made positive or negative providing opportunities for a semi conducting or a

semimetal superlattice and a variety of device applications. The semiconducting superlattice provides an ideal heterostructure for nanofabrication of a variety of devices like lateral resonant interband tunneling diodes (RITDs), single electron transistors (SETs) and so on. This is due to the possibility of having electron and hole carriers in adjacent quantum wells. But the first step to realizing such devices is to be able to control the carrier concentration in these quantum wells, possibly using a gated structure. This work is an attempt to fabricate a field effect transistor device on this composite quantum well heterostructure to achieve this

2. Experiment

2.1 Sample properties

The sample used in the experiment is grown using molecular beam epitaxy (MBE) on a semi- insulating GaAs substrate. The schematic diagram of the top part is shown in figure 1. The top layers consist of (from the bottom) AlSb bottom barrier, a 200 Å GaSb quantum well, 40 Å InAs quantum well followed by a 100 Å GaSb top barrier and a 21 Å InAs cap layer to prevent GaSb from oxidation . The final wafers are 2 inches in diameter.

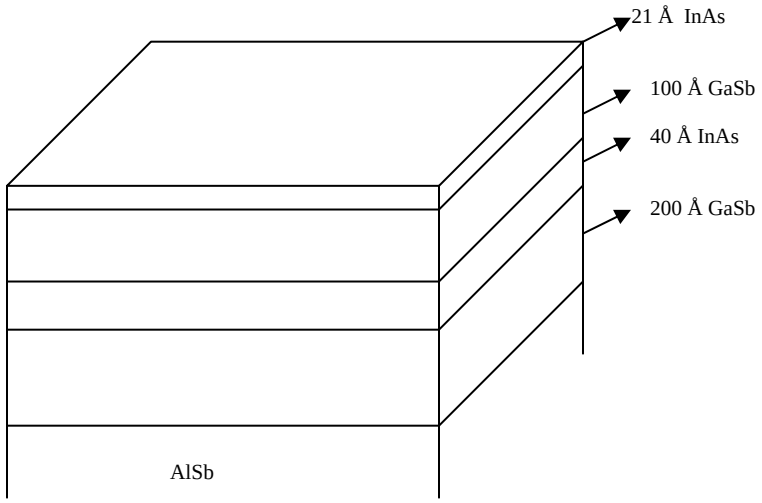


FIG. 1. Schematic diagram of the top layers of the sample

For the following experiment, typically a sample of size 1.2 cm * 1.2 cm is cut from the 2 inch wafer

2.2 Device fabrication

The final device is a Hall bar on a non-conducting substrate. Bonding pads make ohmic contacts to the InAs quantum well layer. A metal gate with silicon dioxide dielectric beneath it goes over the channel area of the Hall bar. This involves three photolithography steps or levels as described below – the bonding pad level for ohmic contacts, the mesa level to define the actual Hall bar pattern and the gate level. The device processing is done in a class-10 clean room. For all the three levels, the photo resist used is OiR 906-10, a positive tone photo resist.

2.2.1 Bonding pad

a. Spin coating of resist:

Spin positive photoresist OiR 906-10 at 3000 rpm, 60 s

Thickness measurements using an Alphastep AS500 profilometer measurements show a resist thickness of about 1.1 μm.

b. Pre-exposure bake:

Bake wafer at 90°C, 60s on hotplate

This soft-bake helps to evaporate all the solvents from the photo resist coating and makes it photosensitive. Vacuum is used to suck the sample onto the heater plate to ensure uniform temperature.

c. UV exposure:

Exposure using a 5X stepper (projection lithography).

Stepper specification: MANN GCA DSW 4800 wafer stepper

Exposure time: 0.17 s Focal number: 0

A chromium mask with the pattern, 5 times the size of the desired device is used to mask the ultraviolet (UV) light in the required places. Since it is a positive tone resist, the exposed area is removed. The first level mask design consists of 9 squares each approximately 150 μm * 150 μm in area. This is a dark field mask and so the square areas are exposed to UV light. The resist in the square areas is removed during subsequent development.

A chuck suited to the thickness of the wafer is selected and the sample is held to the chuck with vacuum. The chuck is held firmly to the base of the stepper also using vacuum. The stepper is programmed in order to do the required task. Among other features, the programming includes leveling so that the wafer is flat. The desired spacing and the number of rows and columns can also be programmed. The mask set design has 4 rows and 3 columns of Hall bars in one unit. Alignment is an important aspect in such multilevel processes. In the first level, the pattern is aligned to be parallel to the cleave line, using angle correction of the stepper.

The exposure time controls the time which the resist will be exposed to the UV flux and focal number (a unit-less parameter on the stepper) controls how much above or below the plane of the sample does the focus of the light beam fall. From a set of focus-exposure experiments, by varying the focus across the columns and the exposure time across the rows in a suitable range, the best values were found out to be 0.17 s and 0 respectively. The flux of the stepper is around 180 mW/cm^2 and hence the dose (exposure time * flux) will be around 30 mJ/cm^2. The photo resist has the property that the areas exposed to the UV light will become soluble in the developer.

d. Post-exposure bake:

Soft-bake at 120°C, 60 s on hotplate with vacuum

Standing waves due to interference of incident and reflected radiations from the stepper results in periodic variations in exposure dose throughout the depth of the photoresist. The post-exposure bake helps to reduce this effect.

e. Resist development:

Develop in developer OCG OPD 4262 for 40 s with 1 Hz stirring frequency

Rinse: Rinse in running deionized (DI) water for 3 minutes

Nitrogen blow dry

The sample is observed under optical microscope with up to 1500x zoom to make sure that it is well developed. Alpha step profiler is used to verify the resist profile in the developed areas.

f. Wet etching:

InAs - thickness: 21 Å	etch time: 6 s	DI water rinse: 10 s
GaSb- thickness: 100 Å	etch time: 8 s	DI water rinse: 20 s

InAs etchant: Acetic acid: hydrogen peroxide: DI water 5:10:100 by volume

Etch rate – 25A/s (approx)

GaSb etchant: Hydrogen peroxide: hydrofluoric acid: lactic acid 1:1:200 by volume Etch rate – 20-25A/s (approx)

Wet etching is selected over dry etching so as not to cause damage to the surface. The photo resist that remains on the sample acts as the etch mask. Both the etchant solutions are stirred thoroughly for about 3 minutes using magnetic stirrers to

ensure thorough and uniform mixing. The over etching is to account for the possibility of having a thin layer of resist which might block or slow the etching in the first few seconds.

g. Metallization:

E-beam evaporator: CHA MARK 40 evaporator

Recipe used: 400 Å Ge, 100 Å Ni and 2000 Å Au.

The thick gold layer is to connect gold wires to the leads, for measurements, either by hand soldering or by wire bonding

h. Lift off:

Leave the sample in acetone for 30 min

i. Resist stripping and cleaning:

Transfer sample to fresh acetone beaker with squeeze bottle spray and rinse for 2 min

Transfer sample to iso-propanol (IPA) beaker with squeeze bottle spray and rinse for 2 min

Transfer sample to fresh IPA beaker with squeeze bottle spray and rinse for 1 min

Nitrogen blow dry

Acetone helps to remove the organic resist and IPA removes the acetone. The sample is again observed under optical microscope. A typical image after the first level is as shown in figure 2. Alpha step profiler can be used to verify the thickness of the metal.

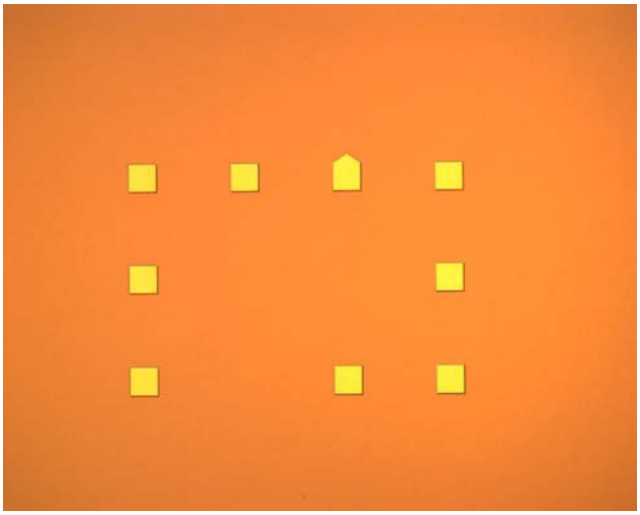


FIG. 2. 50X optical microscope image of the device after level 1

2.2.2 Hall bar Mesa

The basic lithography steps remain the same as in section 2.2.1. The mask pattern consists of dark Hall bar patterns and clear field. Each Hall bar consists of a channel of 10 µm width, with three leads on each side, separated by 30 µm each. The total length of the channel area is 150 µm. The neck area where the leads connect to the channel is 2 µm wide. The mask is aligned to the pattern in level 1. The alignment accuracy is about 1 µm which is good enough for this application. The process steps are as follows

a. Spin coating of resist:

Spin positive photoresist OiR 906-10 at 3000 rpm, 60 s

b. Pre-exposure bake:

Bake wafer at 90°C, 60s on hotplate with vacuum

c. UV exposure:

Exposure using a 5X stepper (projection lithography).

Stepper specification: MANN GCA DSW 4800 wafer stepper

Exposure time: 0.17 s Focal number: 0

d. Post-exposure bake:

Soft-bake at 120°C, 60 s on hotplate with vacuum

e. Resist development:

Develop in OCG OPD 4262 for 40 s with 1 Hz stirring frequency

Rinse: Rinse in running deionized (DI) water for 3 minutes

Nitrogen blow dry

f. Wet etching:

InAs - thickness: 21 Å	etch time: 6 s	DI water rinse: 10 s
GaSb- thickness: 100 Å	etch time: 8 s	DI water rinse: 20 s
InAs - thickness: 40 Å	etch time: 6 s	DI water rinse: 10 s
GaSb- thickness: 200 Å	etch time: 12 s	DI water rinse: 25 s

g. Resist stripping and cleaning:

Leave the sample in acetone beaker for 5 min

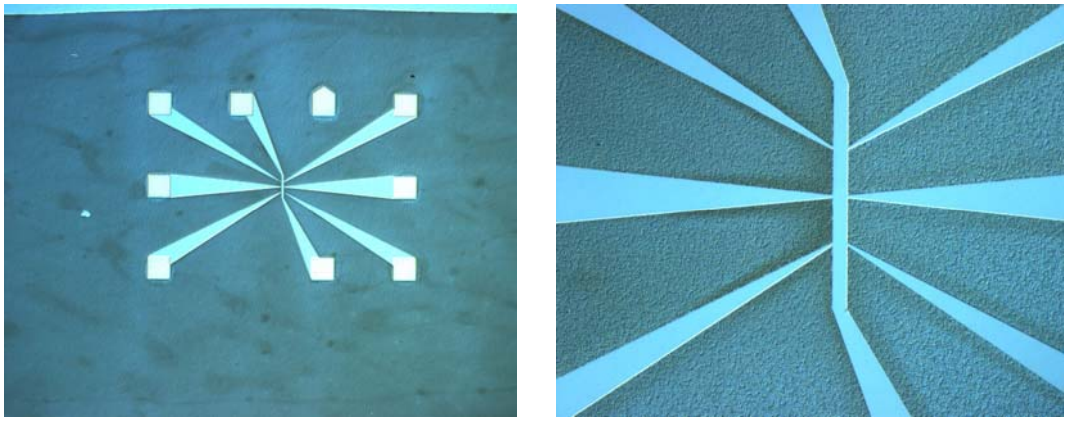
Transfer sample to fresh acetone beaker with squeeze bottle spray and rinse for 2 min

Transfer sample to iso-propanol (IPA) beaker with squeeze bottle spray and rinse for 2 min

Transfer sample to fresh IPA beaker with squeeze bottle spray and rinse for 1 min

Nitrogen blow dry

Alpha step profiler is used to verify the height of the mesa. Figure 3 shows the pictures of the device after this level both at 50X and 1000X magnification



(a) (b)

FIG.3. Optical image of device after level 2 (a)50X magnification (b)1000X magnification

2.2.3 Gate

The dark field mask used in this level consists of a gate pattern, which goes over the Hall bar channel as well as leads to a bonding pad. The length of the gate area is 125 µm and width 20 µm. The processing steps are as follows

a. Spin coating of resist:

Spin positive photoresist OiR 906-10 at 3000 rpm, 60 s

b. Pre-exposure bake:

Bake wafer at 90°C, 60s on hotplate with vacuum

c. UV exposure:

Exposure using a 5X stepper (projection lithography).

Stepper specification: MANN GCA DSW 4800 wafer stepper

Exposure time: 0.17 s

Focal number: 0

d. Post-exposure bake:

Soft-bake at 120°C, 60 s on hotplate with vacuum

e. Resist development:

Develop in OCG OPD 4262 for 40 s with 1 Hz stirring frequency

Rinse: Rinse in running deionized (DI) water for 3 minutes

Nitrogen blow dry

f. Wet etching:

InAs - thickness: 21 Å etch time: 6 s DI water rinse: 10 s

g. Metallization:

E-beam evaporator: CHA MARK 40 evaporator

Recipe used: 1000 Å SiO_2, 100 Å Ti and 2000 Å Au.

h. Lift off:

Leave the sample in acetone for 30 min

i. Resist stripping and cleaning:

Transfer sample to fresh acetone beaker with squeeze bottle spray and rinse for 2 min

Transfer sample to iso-propanol (IPA) beaker with squeeze bottle spray and rinse for 2 min

Transfer sample to fresh IPA beaker with squeeze bottle spray and rinse for 1 min

Nitrogen blow dry

The silicon dioxide layer acts as a dielectric for the gate ensures that the leakage current is less and the breakdown voltage is high enough. The quality and the thickness of the oxide is tested using an n and k analyzer on the oxide grown on a dummy wafer just before the actual sample run. This completes the fabrication part of the device. A schematic diagram of the final sample is shown in figure 4.

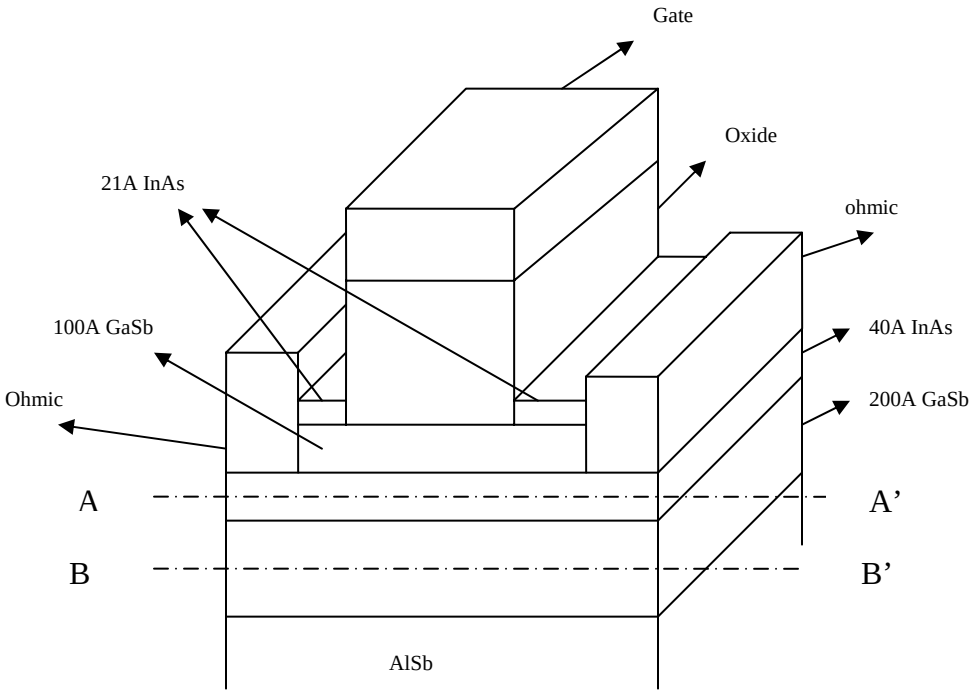
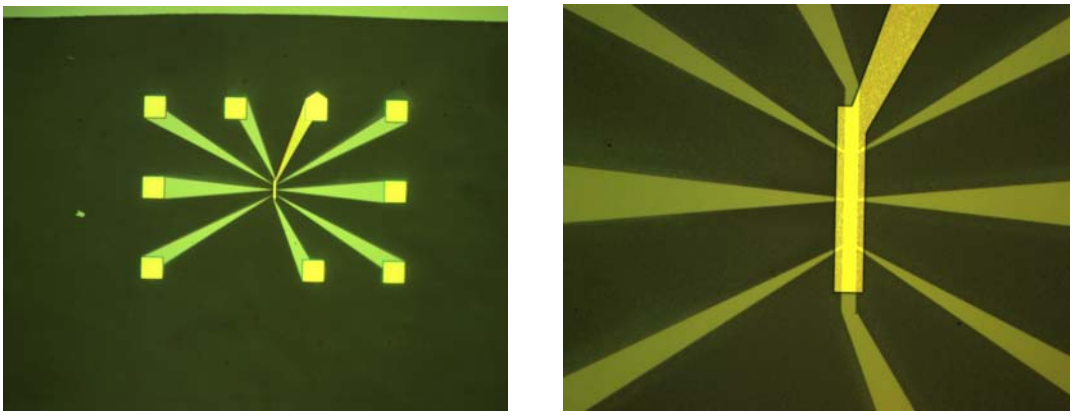


FIG. 4. Schematic diagram of the final device

Pictures of the final device at 50X and 1000X magnification are shown in figure 5 and the actual mask design for the three levels is shown in figure 6.



(a) (b)

FIG. 5. Optical Microscope images of the final device (a) 50Xmagnification (b) 1000X magnification

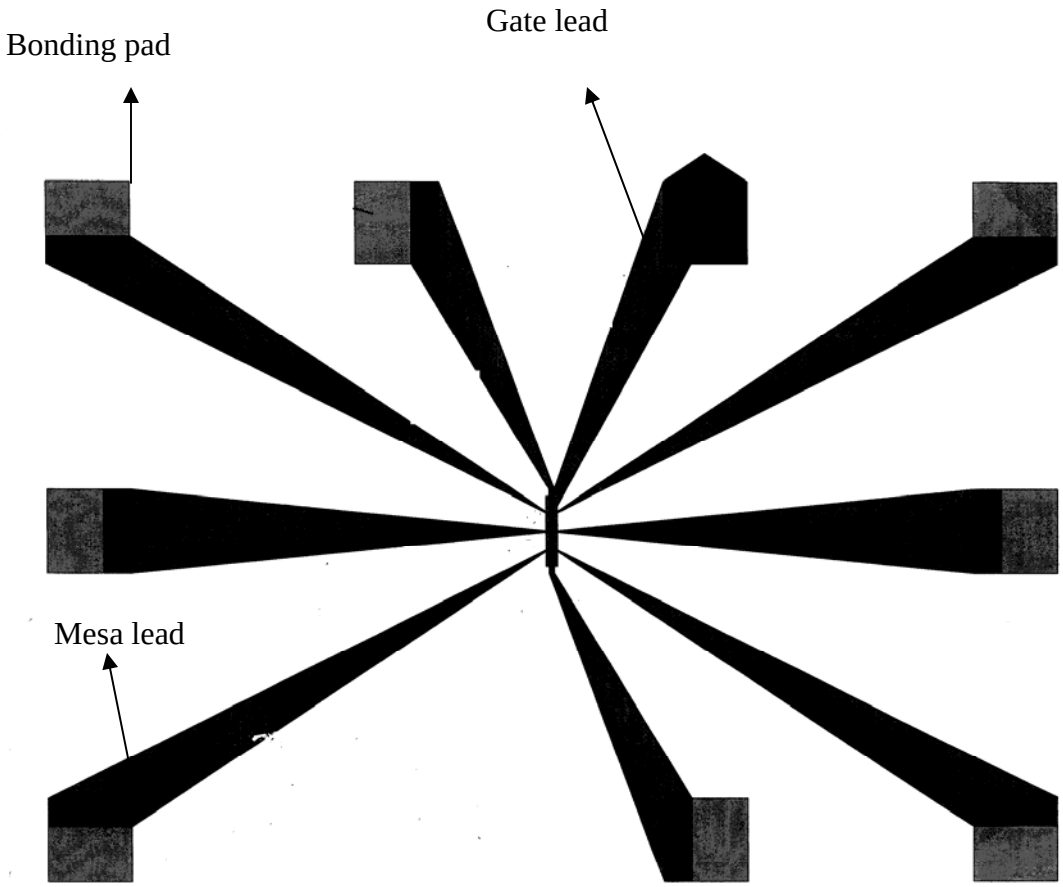


FIG. 6. Mask design for all 3 levels combined

3. Measurements and Results

3.1 Measurement set up

Gold wires are hand soldered onto the sample using indium as the solder and the sample is glued on a 14 pin header using rubber cement. The header is then mounted on a home made sample holder, specially made for liquid helium dewar. The sample holder essentially consists of coaxial cables connecting the 14 pins to the male part of a 19-pin connector

The sample holder unit is then connected to another unit which consists of the female part of the connector, and coaxial cables that connect to a switch board. The switch board has provision to control the connection of each of the wires to either the core or the insulation of a coaxial cable that can be externally connected. In off position, the wire is connected to the ground loop through a 1 Mohm resistor. The switch board is then connected to a semiconductor parameter analyzer (SPA) which has the ability to apply a varying DC voltage and measure the current . There are 3 channels in the SPA, to which the source, drain and the gate are connected. The voltage and current at each of these terminals can be measured. The measurements are plotted using a Lab Windows program.

I-V measurements are done to verify the ohmic contacts of the leads. Then the two leads which connect the two ends of the channel are chosen as source and the drain. I-V measurements are done from gate to source and gate to drain to ensure

minimum leakage current. This is followed by a drain current (I_d) measurement with gate to source voltage(V_{gs}) being swept from a negative to positive voltage keeping drain to source voltage(V_{ds}) at a small voltage (1 mV). This is the crux of the measurements, where one expects to see the carriers changing from holes to electrons. This result is then confirmed by selecting two other leads as source and drain. This is also verified by a field-effect transistor (FET) type measurement where drain current is measured with the drain to source voltage being swept at various gate voltages. All the measurements are done at liquid Helium temperature

3.2 Observations and results

The following were the prominent observations in the measurements as discussed in section 3.1

I_d vs V_{gs} : V_{ds} is kept at 10 mV and V_{gs} is swept from -4 V to + 4 V and back. It is observed that the drain current falls from about 35.9 nA at -4 V to less than pA at zero bias. I_d again starts rising for a positive voltage up to about 37.3 nA at +4V. See figure 7 for the plot and figure 8 for the voltage schematic for the measurement.

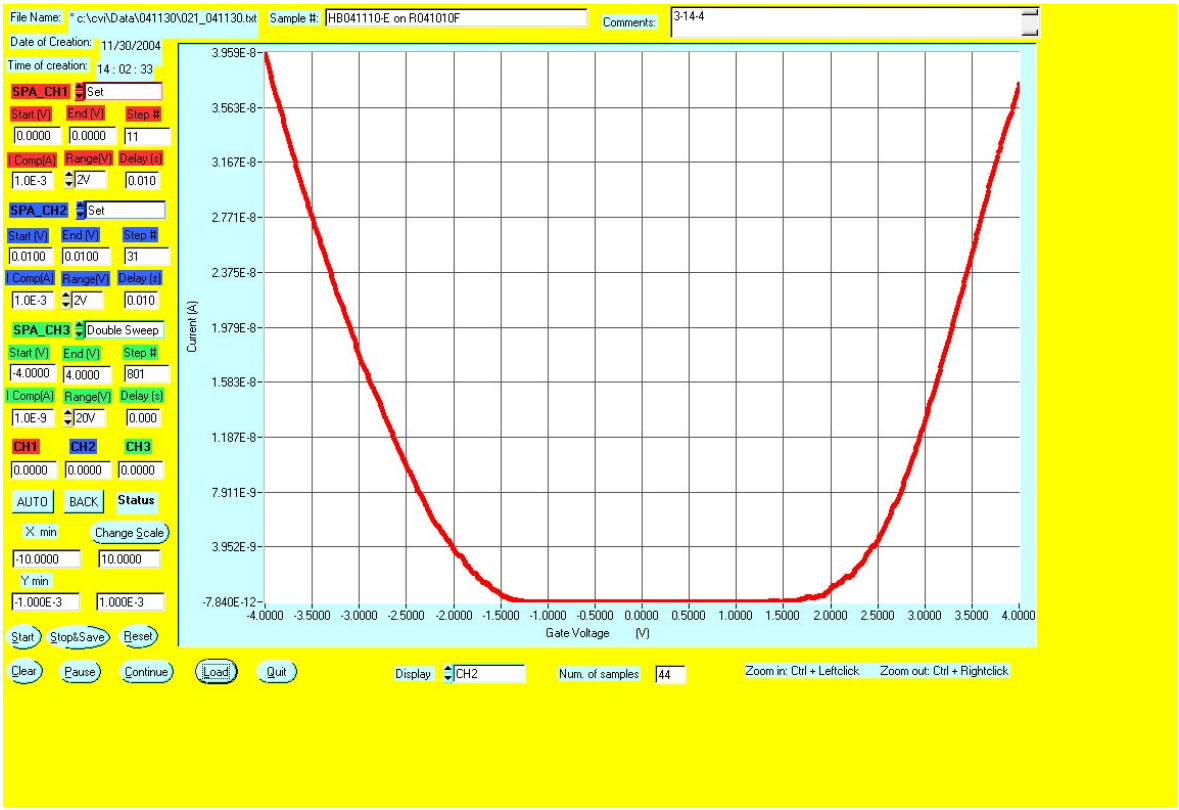


FIG. 7. I_d vs V_{gs} for V_{ds}=10mV. V_{gs} is swept from -4V to +4V

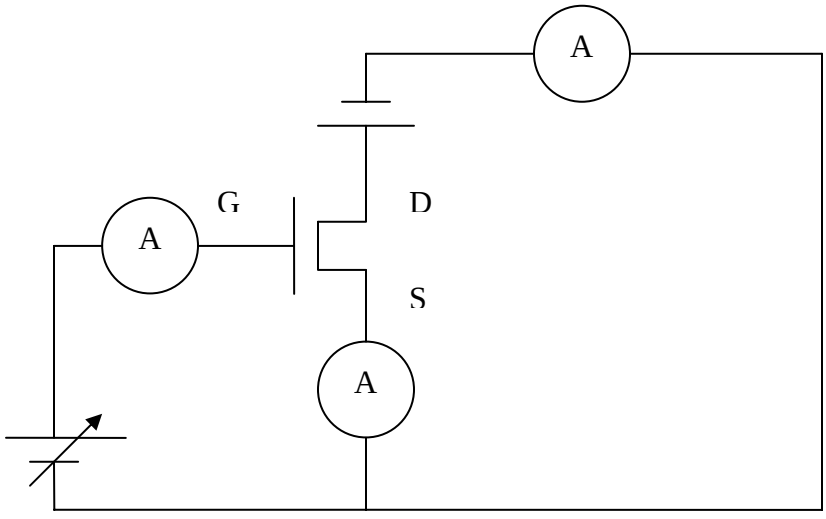


FIG. 8 . Voltage schematic for I_d vs V_{gs} measurement

FET measurements: V_{ds} is swept from -0.15V to +0.15V for V_{gs} values of -3.5V, -2.5V,
-1.5V, +1.5 V, +2.5 V and +3.5 V. The results correlate with the observation in the I_d vs V_{gs} measurement. With increasing gate voltage, the drain current first decreases and then increases. See figure 9 for the plots and figure 10 for the voltage schematic

FIG. 9. I_d vs V_{ds} for V_{gs}=-3.5V, -2.5V,-1.5 V,+1.5V,+2.5V,+3.5V.

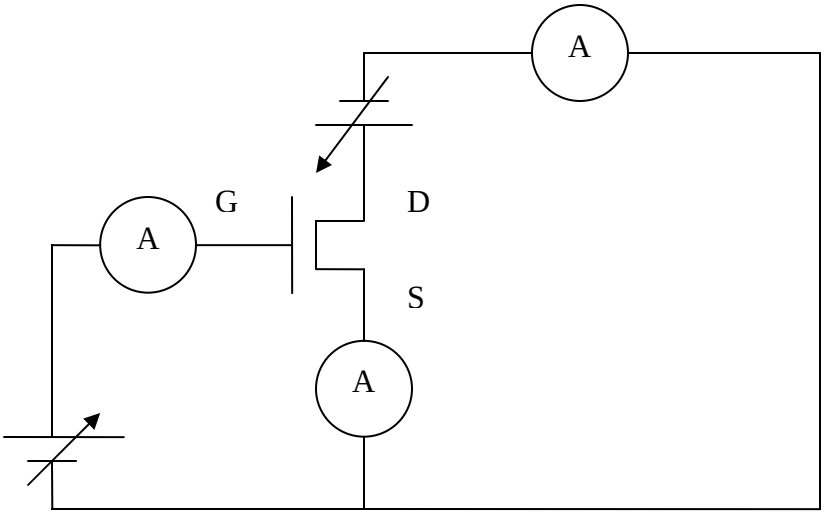
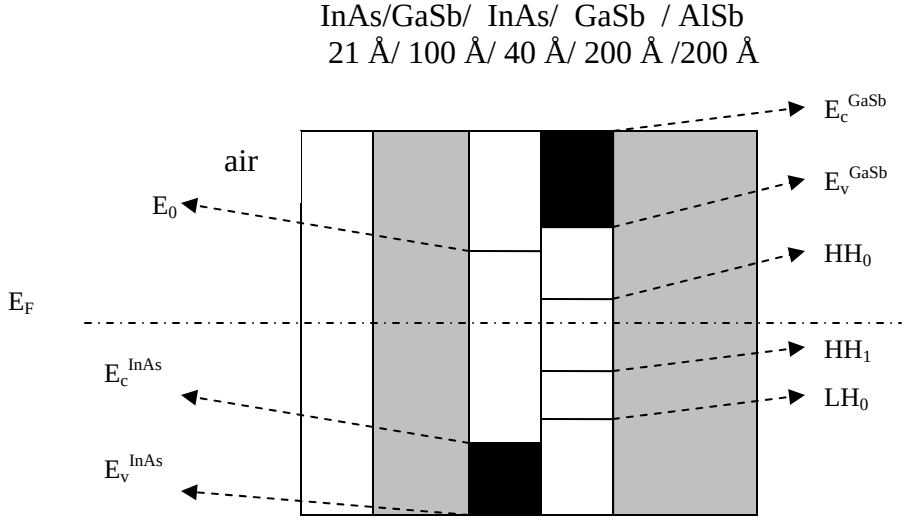


FIG. 10. Voltage schematic for I_d vs V_{gs} measurement

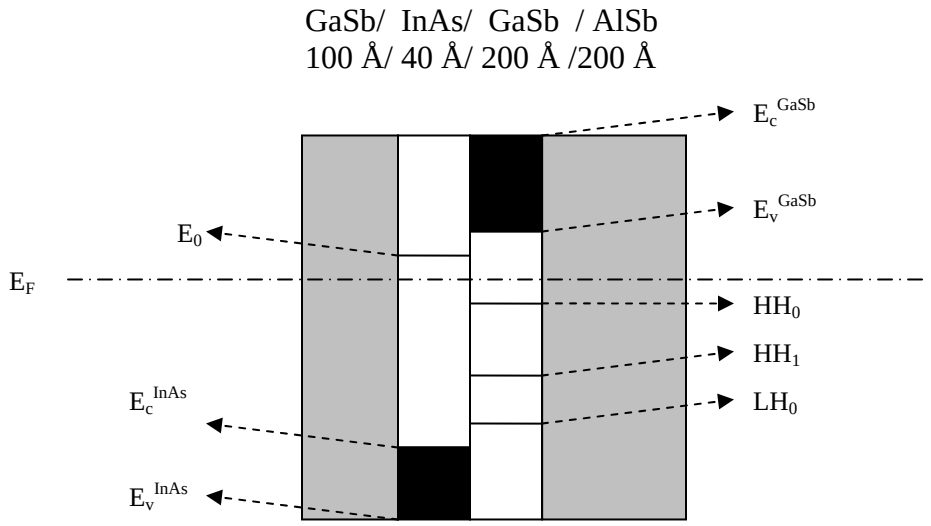
3.3 Discussion

The simple explanation for the observation in section 3.2 I_d vs V_{gs} measurement is that the increasing gate voltage first depletes the hole carriers in the GaSb quantum well and then induces electrons in the InAs quantum well.

This can be detailed using the band diagram picture. The exact band diagram can be obtained by solving the 2-Dimensional quantum well problem and also incorporating the Fermi level pinning position. There has been some previous work which can help solve band diagram picture [1]. However an analysis based on similar work [2] can give a qualitative picture of the band alignments at zero bias of the vertical cross section along the gated region. This is shown in figure 11 below



a)

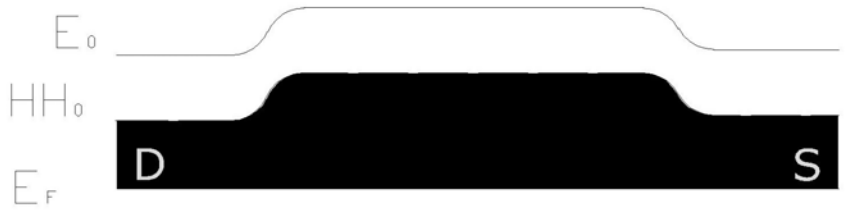


b)

FIG. 11 . Energy diagram (qualitative) a) For as grown sample. b) at zero gate bias, for the layers below the gated area. Note that the top InAs cap layer is etched off below the gate layer

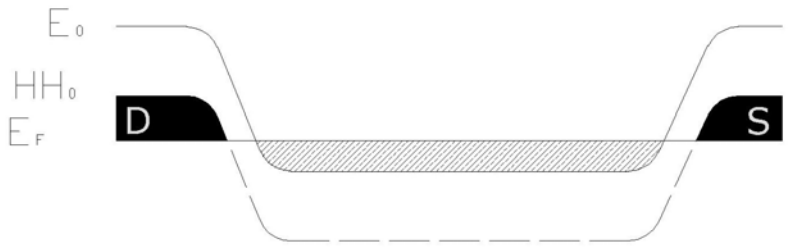
By a suitable choice of the thicknesses of various layers the Fermi level is pinned between E_0 and HH_0 for zero gate bias for the layers below the gate. This results in very low conductance at zero gate bias and more or less symmetric transfer characteristics for positive and negative bias. Also, when the top layer is InAs, the Fermi level is pinned such that there are holes induced in the GaSb quantum well. This helps in making the p-type ohmic contact

The potential profiles horizontally along the two quantum well levels (along the AA' and BB' lines shown in the figure 4), for various gate bias conditions are shown in figure 12 (qualitative picture)



a.

b.



c.

FIG. 12. Band diagrams along AA' and BB' for various gate biases (a) negative bias (b) zero bias (c) positive bias . Note: The dark shaded region represents hole carriers and the light shaded region represents electron carriers

For a negative gate bias, the both E_0 and HH_0 are above the Fermi level and hence there are 2D holes in the GaSb quantum well.. As the gate voltage is increased the subbands move down and the HH_0 goes below the Fermi level where as E_0 still stays above it. The 2D holes get depleted resulting in the negative transconductance. At zero bias there are no carriers in either of the quantum wells and the current goes to close to zero. With a positive gate bias, the E_0 goes below the Fermi level. This results in an accumulation layer in the InAs quantum well, thereby causing the increase in current. At the ohmic contact region there is the presence of hole carriers thereby making a p-type ohmic contact.

This unique transfer characteristic has potential circuit applications like frequency doublers [2].

4. Extension of work

4.1 Hall bar and Magnetic measurements

Hall bar devices make it possible to do various magnetic measurements like Van der Pauw measurements to find out the carrier concentration and mobility on the same device. The measurement involves two major steps. First, the longitudinal and transverse resistances are calculated by applying the suitable ac voltage and measuring the current between the appropriate leads using a lock-in amplifier. Then the Hall voltage is measured and plotted against a sweeping Magnetic field up to about 1 T, both into and out of the plane of the device. The carrier concentration and the mobility of the carriers can be calculated from the results from these measurements at various temperatures like room temperature (about 300K), liquid nitrogen temperature (77K) and at liquid helium temperature (4.2K).

As mentioned in the introduction, with slight change in the quantum well thicknesses, we can achieve various band alignments [3]. This versatility for band gap engineering has potential applications in various other areas, e.g., high-density memories, GaSb/InAs superlattices for infrared detectors, as well as AlSb/InGaSb/InAs for mid-infrared lasers. In addition, this system also offers opportunities for exploring fundamental phenomena under the coexistence of two dimensional electrons and holes. Magnetocapacitance and far-infrared photoconductivity measurements have been done in the past to confirm the presence of a hybridization gap and to measure it [4].

4.2 Lateral resonant interband tunneling diodes (RITDs)

A natural extension to the Hall bar-FET photolithography work is to extend this to nanometer dimension using e-beam lithography. This provides a lateral resonant interband tunneling diode structure as tunneling can take place due to reduced dimension as shown in figure 13. Resonant tunneling is of interest due to the negative differential resistance (NDR) feature that it shows which has potential applications like in memory devices

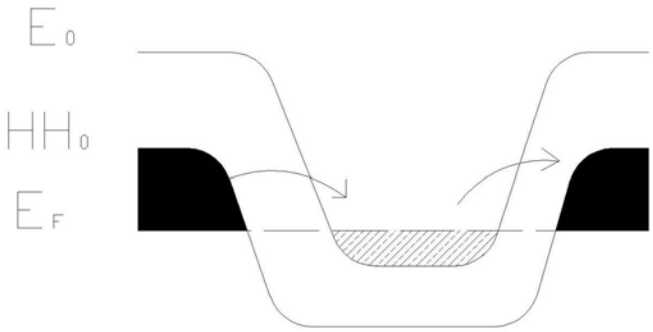


FIG. 13. Lateral resonant interband tunneling

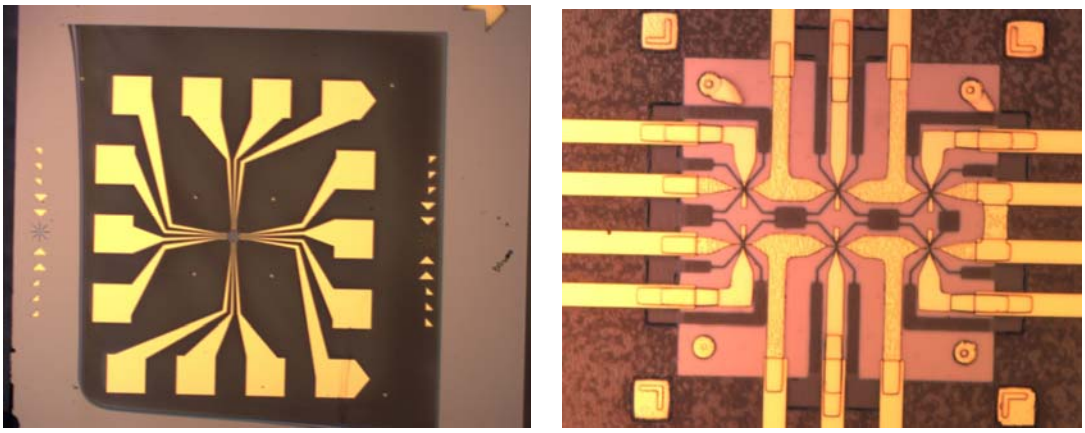
A brief summary of the fabrication process is as given below. First a 14 pin lead pattern is defined using photolithography on a large piece of the sample using stepper. LOR5B/OiR 906-10 bilayer photoresist is used to prevent side wall on the 100 Å Ti/2000 Å Au that is to be deposited by e-beam evaporation. These leads help to connect the future e-beam pattern to the gold wires used for measurements. Defining this pattern using photolithography will help to make the processing faster. Along with the 14 pin leads, the design consists of the alignment pattern for the multi-

level e-beam lithography. This typically consists of a set of 4 crosses at the corners of 500 µm square 4 L patterns at corners of a 80 µm square and 4 square patterns at the corners of a 55 µm square

The e-beam pattern to be written and the alignment pattern are designed in nanometer pattern generating system (NPGS) developed by J.C.Nabity and written using a JOEL scanning electron microscope (SEM). The pattern consists of 6 channels of widths varying from 0.6 µm to 1.6 µm in steps of 0.2 µm. The design of the channel is tapered, and at the neck area, they are 250nm long. The gate patterns run across these channels and are designed to be 100nm wide lines. The e-beam resist used is EL11 in all the levels and has a thickness of about 6000 Å at 3000 rpm for 60 s. Its pre-exposure bake temperature is 150ºC for 60 s

The first e-beam lithography step involves defining the trenches that would define the 6 channels. After writing, the resist is developed in a MIBK/IPA solution. The first 4 layers of the devices are etched off similar to the Hall bar process, there by isolating the channel area. The quantum well layers of this isolated area are the conducting channels. The second e-beam lithography defines the gate pattern. After developing, the InAs top layer is etched off and 1000 Å SiO_2/ 100 Å Ti / 2000 Å Au gate is defined. The third e-beam level defines both ohmic contacts and interconnects. The ohmic contacts for the channels extends to about 1 µm close to the channel on both sides and goes all the way to the corresponding leads which are already defined. The interconnects connect the gate leads to the corresponding leads of the 14 pin

pattern. In this level, the top two cap layers are etched off and Ge 400 Å / Ni 100 Å / Au 2500 Å is deposited . The final step involves a photolithography step to isolate the leads from each other. The mask used has a 34 µm * 34 µm area in the center which is dark and thereby protects the device area. The rest of the field is subject to the 4 layer etching similar to the Hall bar mesa level. This completes the device. Pictures of the final device, both the zoomed in image of the pattern and the full device are shown in figure 14.



(a) (b)

FIG. 14. Optical microscope images of RITD devices fabricated using the composite quantum wall structure (a) entire device including bonding pads: 50X magnification (b) The e-beam patterned area: 1500X magnification

The same set of measurements as in the Hall bar and more like the RITD measurements can be made on this device. However it is found that there are some issues that remain to be solved and a possible better design and/or process scheme needs to be implemented paving the way for future research

5. Conclusion and future direction

Transport properties of a composite quantum well filed effect transistor which consists of two adjacent quantum wells are investigated. The CQW FET shows a strong negative transconductance. This unique transfer characteristic can be accounted for by the switching between 2D electrons and 2D hole channels. This is due to the fact the Fermi level in the CQW can be adjusted between electron subband and the hole subband through the forbidden band gap. This system provides further opportunities for novel devices and circuits

The system opens up lot of opportunities for future research, including realizing devices such as the lateral RITDs, single electron transistors, and their applications such as memory devices, quantum computing

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