ABSTRACT

Title of Dissertation: MICROFABRICATION AND ANALYSIS OF MANIFOLD MICROCHANNEL COOLERS FOR POWER ELECTRONICS

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This research presents the analysis and realization of a single phase high performance manifold microchannel cooler for improving the thermal and hydrodynamic performance of multi-chip power electronic modules. This heat exchanger, microfabricated directly into the substrate, enables higher power density electronic products by more efficiently removing the high levels of heat generated. The improved thermal performance and efficiency of the heat exchanger is demonstrated using both numerical and experimental techniques. The improved heat removal is due to the reduction in the number of packaging layers between the device and the heat exchanger and by improvement in convective heat transfer. In addition, the efficiency of the device is enhanced by minimizing fluid pressure drop through the use of large manifold channels to transport fluid to the cooling area and smaller crossover microchannels in the active cooling area. This combination of channels also improves the uniformity of the

temperature distribution across the device. The manifold microchannel coolers were fabricated and tested both with and without electrical isolation between the chip and the coolant. Experimentally, the coolers without electrical isolation demonstrated thermal resistivity values as low as 0.06 $K/(W/cm^2)$, which is up to a 50X improvement over a standard power package with significant size and weight reduction. The coolers with an incorporated aluminum nitride electrical isolation layer experimentally demonstrated up to a 15X improvement.

In addition to experimental results, the interaction between the manifold channels and multiple microchannels was numerically modeled and compared to simpler, one-dimensional approximations based on the Hagen-Poiseuille equation. The comparison shows that the one-dimensional model, while under-predicting total pressure drops, can provide insight into the effect of varying dimensions on system performance. The numerical models were used to identify the impact of varying dimensions across the entire length of the cooler, and a sensitivity analysis was performed with respect to system pressure drop, thermal resistance and uniformity. Additionally, large microchannel velocity gradients, some larger than 10X, were observed along the length of the device which impacts the chip non-uniformity. The simulations showed that when comparing the manifolded design to a comparable straight microchannel cooler, there is a 38X reduction in system pressure drop for similar thermal performance.

MICROFABRICATION AND ANALYSIS OF MANIFOLD MICROCHANNEL COOLERS FOR POWER ELECTRONICS

by

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Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
2011

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ACKNOWLEDGEMENTS

It is a pleasure to thank those who have helped me achieve my academic accomplishments, for without them, this would not be possible.

It is an honor for me to first thank my advisor, Dr. F. Patrick McCluskey, whose mentorship has been invaluable in both my undergraduate and graduate career and has taught me much about electronics packaging. I owe my deepest gratitude to my mentors at the Army Research Laboratory: Bruce Geil, Nicholas Jankowski, and Dr. Brian Morgan. Bruce has given me the chance to explore my research interests with sufficient guidance along the way. Nick's vast knowledge and patience has taught me about thermal management and fluid dynamics. Brian asked the hard questions and really pushed me to understand and explain. All of their advice and leadership throughout my tenure as a graduate student has made this thesis possible.

I am indebted to my many colleagues at the Army Research Laboratory whose help and advice has made this thesis possible: Gail Koebke, Dimeji Ibitayo, Andrew Bayba, Dr. Ron Green, among many more. Additionally, I would like to thank the cleanroom and support staff at the Army Research Laboratory who trained me on all the equipment and helped me through all my fabrication hurdles along the way. Special thanks also go to Bahman Abbasi at the University of Maryland who was very patient as he helped me learn Fluent.

I am deeply grateful to my committee and all my teachers at the University of Maryland who have given their time and inspired me to love the field of engineering.

A special thanks to my parents, William and Patricia Everhart, who have supported me and provided me the confidence and determination to allow me to excel

both academically and personally. I also would like to thank my friends and family whose emotional support and caring have helped me along the way: Denise Everhart, Rebecca Cohen, Dan Feng, Rifat Jaffreen, Candice Nogueira, Bruno Nogueira, Erin Boteler, Richard Chang, Dana Boteler, Mike Boteler Sr., Eric Stewart, and Betsy Heim.

Lastly, I am also eternally thankful to my husband, Mike Boteler, who has been unwaveringly supportive and loving throughout this entire process. To him I dedicate this thesis.

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List of Abbreviations

AC	-	Alternating Current
AlN	-	Aluminum Nitride
Au	-	Gold
AuSn	-	Gold Tin
CFD	-	Computational Fluid Dynamics
Cr	-	Chrome
CTE	-	Coefficient of Thermal Expansion
Cu	-	Copper
CVD	-	Chemical Vapor Deposition
DBC	-	Direct Bonded Copper
DC	-	Direct Current
DRIE	-	Deep Reactive Ion Etching
HF	-	Hydroflouric Acid
HMDS	-	Hexamethyldisilazane
MEMS	-	Microelectromechanical Systems
MMC	-	Manifold Microchannel
MMC1	-	Manifold Microchannel Version 1
MMC2	-	Manifold Microchannel Version 2
MMC3	-	Manifold Microchannel Version 3
MMC4	-	Manifold Microchannel Version 4
MOSFET	-	Metal–Oxide–Semiconductor Field-Effect Transistor
PECVD	-	Plasma Enhanced Chemical Vapor Deposition
PR	-	Photoresist
PRS	-	Photoresist Stripper
RIE	-	Reactive Ion Etching
RTA	-	Rapid Thermal Anneal
SAM	-	Scanning Acoustic Microscope
SEM	-	Scanning Electron Microscope
Si	-	Silicon
SiC	-	Silicon Carbide
SiO_2	-	Silicon Dioxide
TIM	-	Thermal Interface Material

1 Introduction

There is a continual market pull in the electronics industry for smaller products with more capabilities (i.e. increased functional density). This results in electronics with ever higher heat generation requiring more effective cooling. The objective of this thesis is to create a novel micro-fabricated manifold microchannel cooler that will efficiently cool power devices by reducing the thermal stack and minimizing pressure drop during single phase liquid forced convective flow. The manifold design uses larger channels to transport fluid into and out of the cooling area and smaller crossover microchannels in the active cooling area. This reduces pressure drop while increasing heat transfer and allows for a more uniform temperature distribution across the area of the device. The design also allows for a significant reduction in the thermal stack between the device and the cooling fluid, which reduces overall package size and improves heat transfer.

1.1 Electronics Heat Problem

The current trend in the electronics industry is towards smaller products with increased capabilities, which results in products that have a higher overall power density. This in turn means that the electronics will generate more heat that must be removed. Moore's law, which was proposed for memory devices in 1965, states that the number of transistors in a given area will double every two years. [1] This law has been estimated to be accurate until at least 2015 and even further with new materials other than silicon or with self-assembling nanotechnology. [2] Similar increases in power density have been seen in power electronic devices as well. And it has been estimated that in the near future, it will be necessary to cool power electronics components having heat fluxes approaching

1000 W/cm^2 [3]. These high heat fluxes mean that developing improved cooling technologies is now critical.

Without proper cooling, the increased heat fluxes will result in higher device operating temperatures, which can cause adverse effects on device performance. As the temperature increases, the reverse leakage current increases exponentially, the forward voltage drops in p-n junctions increases, the thermal and electrical conductivities decrease, the gain in bipolar junction transistors (BJTs) increases, and the threshold voltages in metal oxide semiconductor field effect transistors (MOSFETs) decreases. If the temperature gets high enough, the p-n junctions can cease to function. Short of complete loss of junction action, increased leakage current (at temperatures above 150ºC) is often considered to be the most significant problem. In commercial applications, silicon devices are commonly derated if used at elevated temperatures. But in high performance systems, derating devices could significantly reduce system performance and therefore is not a desirable solution. High temperature can also increase susceptibility to a wide range of degradation mechanisms including electromigration, corrosion, passivation cracking and intermetallics formation. [4]

1.2 Standard Power Package

Figure 1-1 shows a cross-section schematic of a standard power package used today. Starting from the top, the power device (made of silicon or silicon carbide) is attached to the top copper layer of a direct bonded copper (DBC) substrate using a high temperature solder or braze (typically gold-tin). DBC substrates are comprised of a ceramic (either alumina or aluminum nitride) that has thick (200 – 300 μm) copper foil directly attached to both sides using a high temperature eutectic bonding process. The

circuit interconnections are patterned in the top layer of the copper onto which the devices and external electrical connections are attached. The backside layer of copper is of the same thickness as the top layer and acts primarily to even the stress induced by the CTE (coefficient of thermal expansion) mismatch between the top copper layer and the ceramic, thus avoiding bowing of the DBC. The center ceramic layer is used as an electrical isolation layer. The DBC substrate is then soldered to a metal (typically copper) heat spreader, which is in turn attached to a metal (typically copper-finned) heat sink using a thermal interface material (TIM) such as a thermal grease or thermal pad.

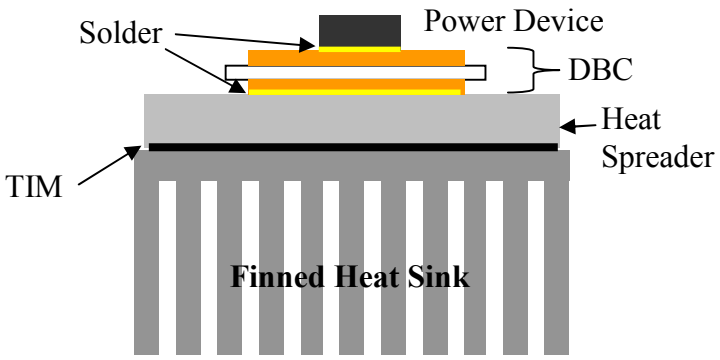


Figure 1-1: Cross section schematic of a standard power package

1.3 Maintaining Operating Temperatures

Maintaining operating temperatures refers to operating devices within their allowable temperature ranges. High temperature electronics are typically considered to be devices operating above 125 ºC. Two ways to extend the allowable operating temperatures include using alterative device materials and/or improving the cooling capabilities.

1.3.1 Alternative Electronic Materials (GaN, SiC)

Power electronics applications (e.g., military and automotive control electronics) are already reaching the temperature limit of silicon electronics, which is around 150-175 ºC. [4] Therefore, alternative materials, such as gallium nitride (GaN) and silicon carbide (SiC) wide band-gap semiconductors are being researched for high temperature operation. [5] These alternative materials have many benefits over silicon: increased power density, faster switching speed, higher temperature operation, and higher reverse breakdown voltage. SiC is already in heavy development and many devices have been fabricated such as MOSFETs, JFETs, thyristors, and diodes. A SiC schottky diode has been shown to operate at temperatures up to 700 ºC and a MOSFET up to 650 ºC [6], whereas the silicon devices degrade at temperatures greater than 175 ºC.

1.3.2 Enhance Cooling Capabilities

The higher heat loads of today's electronics create a need for improved cooling methods to improve heat transfer from power devices. Cooling is necessary to maintain performance of electronics components, as devices tend to perform better and more reliably at lower temperatures. Current standard cooling technology uses a forced air cooled finned heat sink which is oftentimes noisy, large, fluid limited, and the performance of which, at a fixed air flow velocity, can only be improved by increasing its surface area and size. Today's applications are pushing the temperature limits of these heat sinks; therefore, improvements must be made. Four ways to improve upon the current air-cooled heat sink technology to make it more efficient are 1) to use a liquid coolant instead of air, 2) to use a microchannel fin structure to maximize surface area, 3) to utilize an enclosed structure, and 4) to reduce the thermal stack. These four items

are shown schematically in Figure 1-2 and are discussed in detail in the following sections.

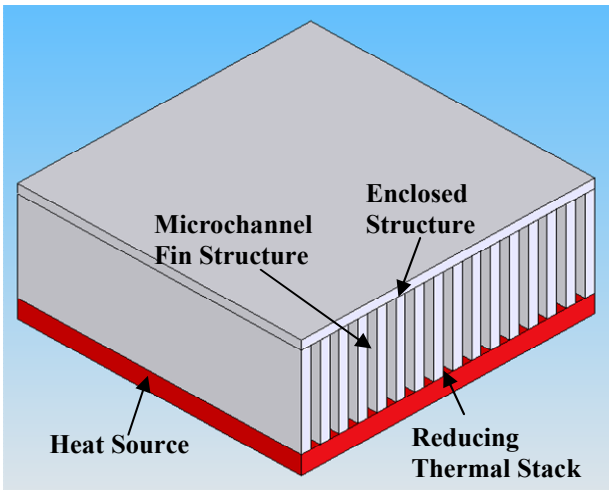


Figure 1-2: Schematic of a microchannel cooler with its main components

1.3.2.1 Liquid versus Air

Cooling with liquids, such as water, is much more effective at removing heat than cooling with air because water has both a higher thermal conductivity and specific heat. The thermal conductivity of air is 0.024 W/mK whereas the thermal conductivity of water is 0.58 W/mK, almost 25 times higher. Additionally, the specific heat is about four times greater. Therefore, for high heat fluxes, liquid cooling is necessary. [7]

However, there are disadvantages to liquid cooling: additional system components are necessary which make a more complicated and less reliable system, and liquids, such as water, are corrosive and electrically conductive, which could damage/short the device. Liquid systems generally require large flow rates to achieve high convective rates. Therefore, care must be taken if using a liquid to cool electronic systems.

1.3.2.2 Microchannel Fin Structure

Convection is a surface effect; therefore, only the fluid in contact with a surface will be effective at removing heat. In order to maximize the cooling potential, a large surface area is necessary, and to minimize volume, densely packed extended surfaces are desired. These dense extended surfaces can be achieved through the use of microchannels, which are sub-millimeter scale cooling channels. This maximizes surface area in a minimal volume thus bringing a larger percentage of fluid closer to the heated surface. [8] Microchannel cooling is based on the idea that the heat transfer coefficient is inversely proportional to the hydraulic diameter of the channel. Microchannels show great promise because they allow for smaller packaging and better performance. A disadvantage to microchannel cooling is the complicated fabrication methods.

1.3.2.3 Enclosed Fin Structure

Since any fluid that is not in contact with the finned surface is poorly utilized in heat transfer, an enclosed fin structure is desirable, which is shown schematically in Figure 1-3. An enclosed fin structure means that the ends of the fins are capped off, causing the fluid to flow strictly through the channels. This also has the additional benefit of minimizing wasted pumping work.

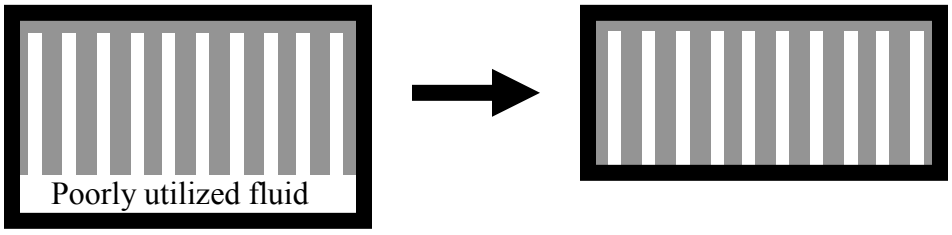


Figure 1-3: Figure depicting the enclosed fin structure where there is no gap at the base of the channels

1.3.2.4 Thermal Stack Reduction

The thermal stack is the sum of materials between the heat source and the coolant through which heat must be conducted. These materials act as a thermal impediment; therefore, the closer the cooling fluid is to the heat source, the more heat will be absorbed per unit flow. A description of the thermal stack and thermal resistance equations can be found in Appendix B.1.3.

1.3.2.4.1 Reducing the Thermal Stack with Microchannels

In order to cool more effectively, minimizing the thermal stack is imperative. The total thermal resistance (R_{th}) of the standard power package is shown in Figure 1-4 on the left side below the packaging stack and includes the sum of the chip, die attach, DBC, heat spreader, TIM, and heat sink. A common practice today is to simply replace the standard copper finned heat sink with a higher performing microchannel heat sink, as is shown on the upper right side of Figure 1-4. While this does have a significant improvement on the effectiveness of the heat sink, the only reduction in the thermal resistance equation is in the heat sink resistance, shown circled in original thermal stack equation. However, the rest of the terms in this equation remain the same. A significant improvement in the thermal stack could be made by incorporating the microchannel heat sink into the substrate, as is shown in the lower right portion of Figure 1-4. The thermal resistance equation has now been reduced to the sum of only the chip, the die attach and the heat sink. This is essentially the logical limit of the thermal stack reduction.

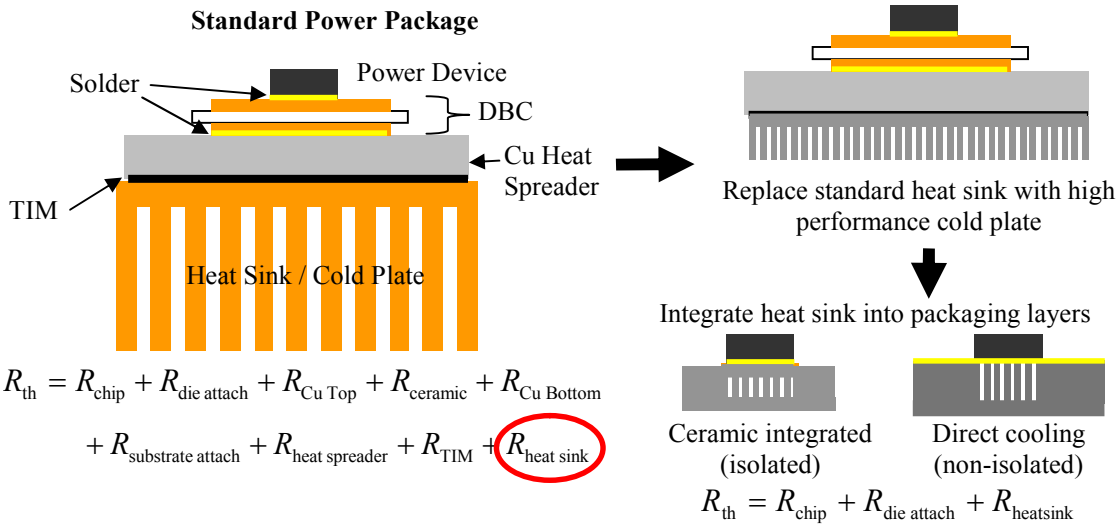


Figure 1-4: Schematic showing a reduction in the thermal stack by first replacing the standard copper heat sink with a microchannel heat sink, then replacing the entire stack with a microchannel heat sink

Figure 1-5 shows how the thermal stack affects the rise in chip temperature. A typical standard power package has thermal resistance values between 0.6 and 3.3 K-cm^2/W with the majority (0.5 to 3 K-cm^2/W) of the resistance coming from the TIM and the heat sink. By simply replacing the standard heat sink with a high performance cold plate (as was shown in Figure 1-4), the total thermal resistance can be reduced significantly to between 0.15 and 0.8 K-cm^2/W. To reduce this further it becomes necessary to reduce the thermal stack and incorporate the heat sink into the substrate. This could reduce the thermal resistance to less than 0.1 K-cm^2/W. This substantial reduction in thermal resistance is one of the main goals of this study.

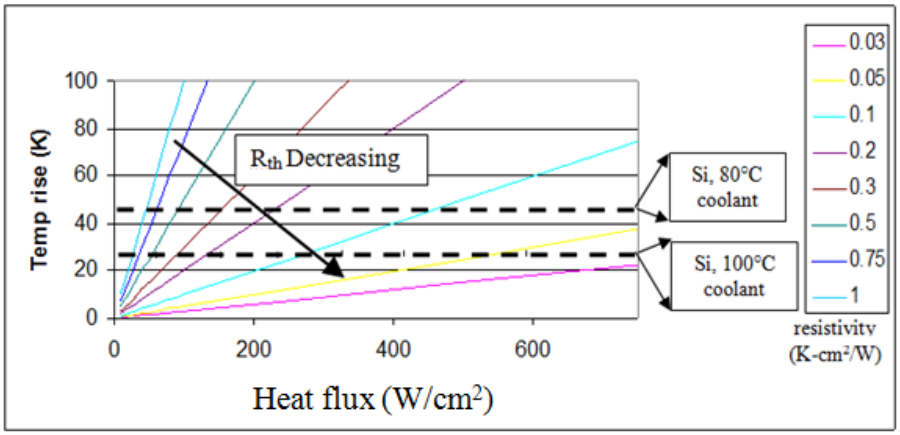


Figure 1-5: Graph of the thermal stack effect on die temperature

The effect of the thermal stack on the die temperature is also seen in Figure 1-5. Two dashed lines are shown on the figure at 25 ºC and at 45 ºC which represent the allowable chip temperature rise for a 100 ºC and 80 ºC coolant, respectively. This assumes a maximum silicon operating temperature of 125 ºC. These high coolant temperatures are common for automotive power electronics applications. It can be seen from the graph, that in order to achieve a heat flux of 500 W/cm^2 with a coolant temperature of 100 ºC, the thermal resistance must be less than 0.05 K-cm^2/W, which requires a very efficient heat sink and significantly reduced thermal stack.

1.3.2.4.2 Direct Backside Cooling

In order to significantly reduce the thermal stack and improve the cooling performance, it would be desirable to mate the cooling channels directly to the backside of the device, as shown in the bottom right of Figure 1-4. This reduces the thermal stack equation to simply the thermal resistance of the chip, die attach, and heat sink. This reduction is essentially the logical limit for thermal stack reduction and practically eliminates the thermal stack, providing significant cooling improvement and overall

package size reduction. However, it has the potential to cause large thermal gradients in the device. Figure 1-4 shows this thermal stack reduction both with and without electrical isolation. In some cases, it will be necessary to have electrical isolation between the chip and the fluid. If electrical isolation is required, it is desirable to minimize its effect on the thermal stack by designing it to be thin and made of a material with a high thermal conductivity and high dielectric strength. Electrical isolation could also be achieved by using a dielectric fluid which would not conduct electricity.

1.3.2.5 Summary of Enhancing the Cooling Capabilities

Maximum cooling potential can be achieved by flowing a liquid through microchannels with an enclosed fin structure and situated directly on the back of the heated surface.

1.4 Microchannel Cooling Limitations

Competing effects exist that preclude simply making the channels as small as possible. First, is the competing effect of improved heat transfer versus increased flow restriction and particulate clogging in smaller channels. Second, is the competing effect of improves heat transfer versus increased non-uniformity across the length of the channel. Both of these effects will be discussed in more detail below.

1.4.1 Increased Pressure Drop with Decreased Channel Size

While smaller channels lead to better heat absorption because of increased total surface area, they also lead to significantly increased flow restriction along the channel. A description of calculating pressure drops can be found in Section 3.2. The pressure drop increases exponentially with decreasing hydraulic diameter, shown in Figure 1-6.

The increase in pressure drop equates to an increase in the necessary pumping power. Smaller channels also increase the chance of particulate clogging, reducing performance.

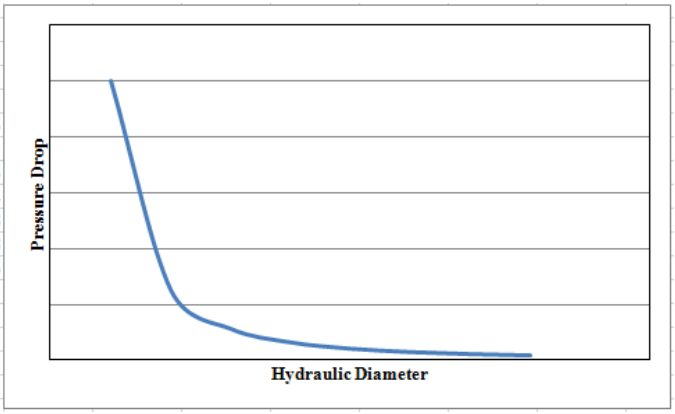


Figure 1-6: A non-dimensional graph of pressure drop versus hydraulic diameter

1.4.2 Non-uniform Cooling

On top of the problem of the smaller channels increasing the flow restriction, is the problem of non-uniform cooling caused by the fluid absorbing heat as it flows through the channels. This creates a thermal gradient along the surface of the device, shown in Figure 1-7, which can lead to a decreased overall performance and mechanical failure.

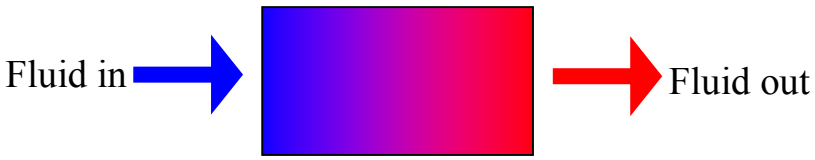


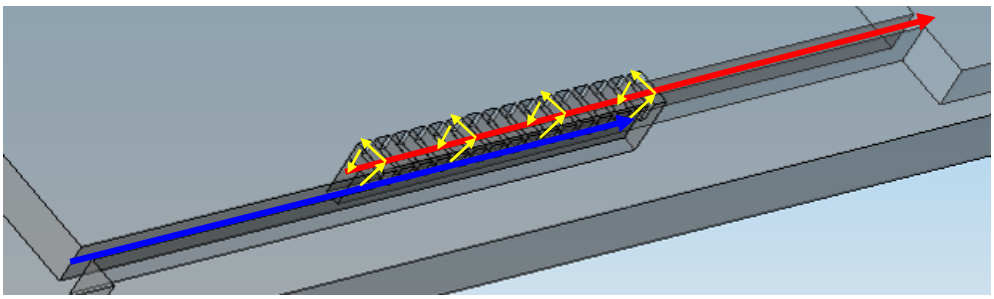
Figure 1-7: Schematic depicting non-uniform cooling along the surface of the device

Non-uniform cooling can be reduced by increasing the velocity of the fluid through the channels, but this in turn increases the pressure drop. Two-phase is another

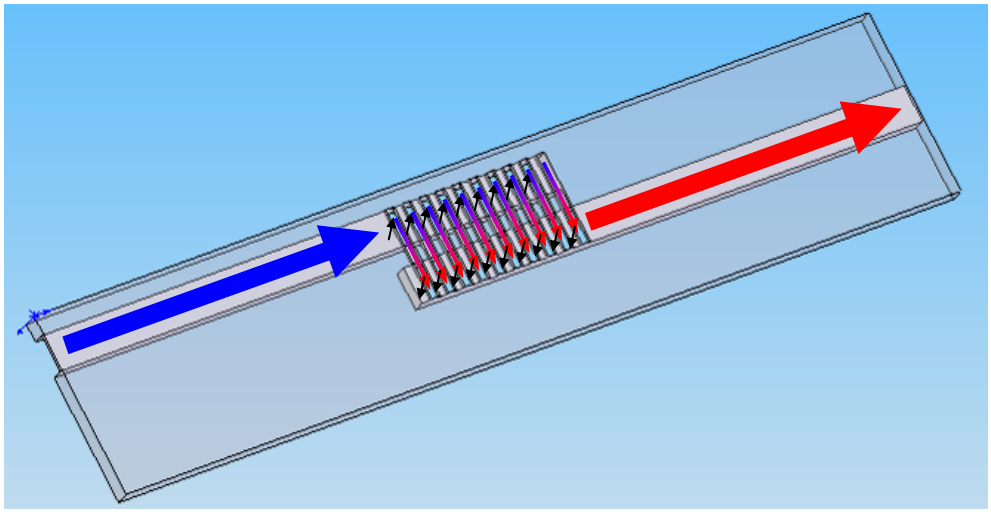
method that has been proposed to reduce the effect of non-uniform cooling; but this creates a much more complicated system design.

1.5 Solution: Manifold Microchannel Coolers

One solution to the problems of increased pressure drop and non-uniform cooling due to smaller channels is to use a manifold microchannel design [10]. Figure 1-8 shows the manifold microchannel unit cell. The manifold design incorporates a two-stage flow that is designed to take advantage of both large and small channels. The fluid flows in through channels with a large cross-sectional area (manifold channels), then is forced through much smaller perpendicular channels (microchannels), and then flows out through another large channel (manifold channel). This flow pattern is depicted in Figure 1-8a, with the blue arrow indicating the cold fluid in, the yellow arrows representing the crossover flow through the microchannels, and the red arrow indicating the exiting heated fluid. The large, long channels are responsible for fluid delivery into and out of the active cooling area. They are located away from the heated surface and due to their large size; the pressure drop of the system is reduced. The smaller, short channels are located adjacent to the heated surface and are responsible for removing heat. Figure 1-8b shows how the fluid is heated in the microchannel from cold (blue) to heated (red).



(a)



(b)

Figure 1-8: Manifold microchannel unit cell schematic. (a) The blue arrow shows the fluid going in through a manifold channel. The yellow arrows show the fluid passing through the smaller microchannels and the red arrow shows the heated fluid traveling back out through a manifold channel (b) this schematic depicts how the fluid heats up against the heated surface.

The basic structure, depicted in Figure 1-8, is repeated multiple times, as is shown in Figure 1-9, in order to achieve temperature uniformity over a larger cooling area and to reduce the fluid flow distance in the microchannels. The dashed yellow box in the figure represents the active cooling area and it should be noted that the overall temperature inside the box is much more uniform than would be the case with straight microchannels.

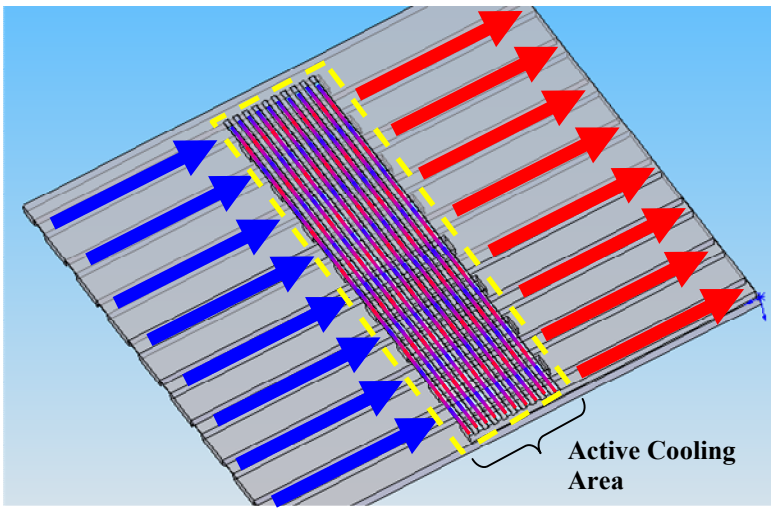


Figure 1-9: The repeated basic structure of the manifold microchannel design showing temperature uniformity over the active cooling area, depicted as the yellow dashed box.

1.5.1 Benefits of the Manifold Microchannel Design

One benefit of the manifold microchannel design is that it increases the cooling potential by utilizing smaller microchannels in the active cooling area. It also reduces flow resistance by allowing the majority of the flow to happen in larger cross sectional channels creating a flow restriction somewhere between that associated with the small and large channels. Finally, this design significantly improves the temperature uniformity along the active cooling area, lowering the chance of mechanical failures caused by in-plane spatial temperature gradients.

1.6 Manifold Microchannel Dimension Labels

For reference, the critical dimensions for the manifold microchannel design are shown in Figure 1-10. The lowercase "m" refers to the microchannel dimensions and the capital "M" refers to the manifold dimensions. There are three subscripts: h, f, and w which refer to the height, fin width and channel width, respectively.

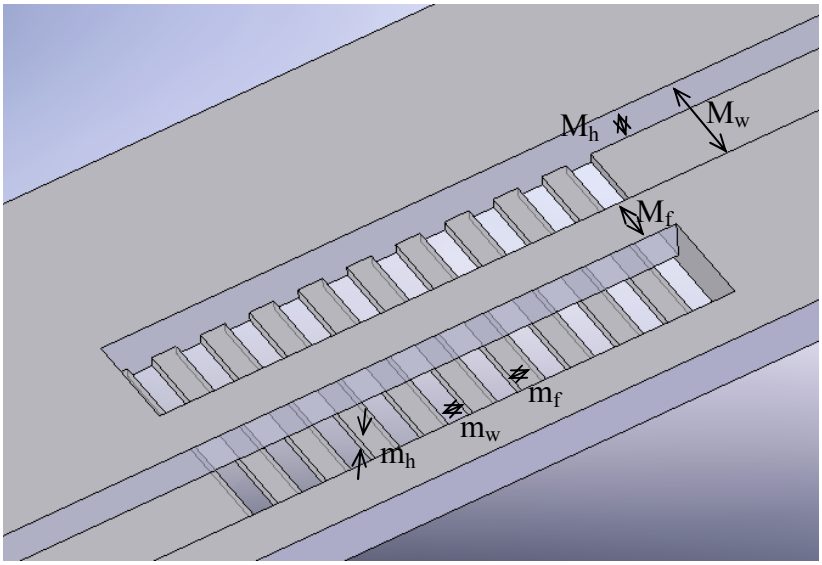


Figure 1-10: Critical dimensions for the MMC design

Appendix A gives a full list of the nomenclature used throughout this document. Appendix B summarizes the classical equations of heat transfer and fluid flow used throughout this paper.

1.7 Design Considerations

The three main considerations when designing MMC structures are the manufacturability, the reliability and the performance. The manufacturability is a critical factor because fabrication limitations will set boundaries on the types of geometries that can be manufactured. The reliability is important because if it will not function reliably, then it will never be able to be utilized. The performance is based both on both the thermal performance and system pressure drop, as will be discussed in more detail in Section 1.10. In most design decisions in this thesis, compromises will have to be made such that not all factors will be improved. Many things must be considered during the

design process including dimensions, number of manifold and microchannels, fabrication limitations, and attachment materials.

Another consideration is fabrication limitations. DRIE is a critical fabrication step and it has depth limitations along with the effects of lagging, loading and tapering. All these limitations must either be worked around or accounted for when designing the devices and their masks. Additionally, MEMS processing is inherently based on planar topologies, thus limiting the types of features that can be fabricated.

Another design consideration, especially for multi-chip modules, is electrical isolation between the chips and fluid. A dielectric fluid could also be used for electrical isolation. This isolation must also be considered for its effect on the thermal performance, as it will most likely impair it.

The sizes of both the manifold channels and the microchannels have a large effect on the pressure drop of the system. Maximizing the channel size will improve the pressure drop but in general, it will decrease the thermal performance. Additionally, clogging is a concern for actual applications therefore, to minimize the impact of channels clogging; the channels sizes should also be increased. The tradeoff between the pressure drop and thermal performance is a dominant design consideration and is discussed further in Section 1.10.

It is essential to consider the thermal path from the die to the fluid as it is a critical determining factor of the overall thermal performance. Each layer should be thin, highly thermally conductive and have a strong bond between each layer.

The whole structure must also be fluidically sealed. Therefore, the bonds between layers must be designed such that they are sufficient to prohibit fluid from exiting the

structure and also can withstand flow rates and pressures typical of the intended application.

The method by which the chip is attached to the substrate must also be considered. In order to minimize the thermal resistance, the bond layer must be thin and made of a highly thermally conductive material. If there is no electrical isolation between the bottom of the chip and the fluid, then this attach must also act as a fluidic seal.

Size is a key design factor as well. A goal of this thesis is to reduce the overall size of a heat sink. Therefore, when designing the structure, reducing the size will always be advantageous.

During the fabrication sequence, it is much easier to work with a whole wafer as opposed to individual pieces. Therefore, when designing the fabrication sequence, wafer dicing should occur towards the end. Maximizing the number of devices per wafer is also desirable in order to achieve maximum yield.

How to get the fluid into and out of the cooler is also a consideration. Fluidic connections should not cause a huge pressure drop, while permitting ease of connection/disconnection. They should also not interfere with thermal measurement or electrical access.

1.8 Fabrication and Experimental Procedure

The devices presented in this report were all fabricated using MEMS (Micro-Electro-Mechanical Systems) processes. MEMS processing was developed as an offshoot of the semiconductor industry for the purpose of making very small, precise mechanical systems. Silicon is the most common material for MEMS fabrication and is the material used in this study. The MEMS processes are described in Appendix E.

1.9 Advantages and Disadvantages of Using Silicon versus Other Materials

When considering which material would be best for fabrication of the manifold microchannel design, a list of qualities was made. Ideally the chosen material would be hard, durable, highly thermally conductive, electrically isolating, and should facilitate precise machining of small channels. Silicon was chosen as the material of choice for this study mainly for its ability to be precisely machined using MEMS techniques. Further advantages of choosing silicon include its hardness, ability to easily grow a single native oxide, and mature fabrication processes. It also has a very small thermal expansion and fairly good thermal conductivity ($k_{silicon}$ = 149 W/mK). Its disadvantages include the fact that it is a brittle material and it is not an electrical insulator.

Other materials that were considered include ceramics (such as aluminum oxide or aluminum nitride) and metals (such as copper or anodized aluminum). Ceramics have the distinct benefit of being both highly thermally conductive and electrically isolating. Although their major disadvantage is that they are extremely hard to machine, especially when small features must be created. Metals are also highly thermally conductive and there are ways to micro-machine them but they are electrically conductive and cannot be machined as precisely and readily as silicon. For a commercial implementation of the MMC structure, it would be advantageous to look into fabricating it in a different material but to prove out the concept and to show the capabilities of an MMC design, silicon has proven to be the best choice.

1.10 Performance Factors: Pressure Drop and Chip Temperature

Two factors that have been determined to best indicate the performance of each manifold system are the rise in chip temperature and the overall system pressure drop. In

general, these are competing factors such that as the chip temperature decreases, the pressure drop increases, and vice versa. This occurs because, in general, smaller channels have better cooling potential but also more flow restriction. Reducing both the rise in chip temperature and the pressure drop in a manufacturable prototype manifold microchannel device for a given set of conditions is the desired result of this study. A significant contribution of this thesis is to discuss the tradeoffs between improving the thermal performance and reducing the system pressure drop.

1.11 Applications

The focus of this thesis includes applications for cooling of high power density systems such as DC/DC, DC/AC, and AC/AC inverters and converters. It is useful in any high-power or high-temperature application or in applications where uniform cooling of the device is necessary. Therefore, it can also be used for harsh environment electronics to allow silicon to operate in a higher temperature ambient but still remain within its operating limits. It can also handle large power loads for silicon carbide or other wide band-gap devices or for laser cooling applications.

1.12 Dissertation Outline

The dissertation presented here consists of nine chapters. The current chapter, Chapter 1, introduces the electronics heat problem and ways to effectively remove heat from electronics packages. It then discusses the limitations of current microchannel technologies and introduces the solution of manifold microchannel coolers. Chapter 2 comprises the literature review including discussion of past works on manifold microchannels and other similar proposed technologies. Chapter 3 looks at the extensive

modeling that was performed using Fluent. It starts with the model set-up and assumptions then does a complete analysis of a single geometry. Chapter 4 then discusses numerical models that show the effect of various parameters on both the thermal performance and the pressure drop of the system. The parameters it considers are the manifold height (M_h), the manifold fin width (M_f), the manifold channel width (M_w), the chip length (L_{chip}), the microchannel width (m_w) and the microchannel fin width (m_f). Chapter 5 describes the first prototype version of the manifold microchannels coolers: MMC1, whose main purpose was to prove the fabrication sequence. Chapter 6 discusses the design and manufacture of MMC2, a fully-functioning cooler with no electrical isolation. It then presents the results of the testing and modeling of MMC2. Chapters 7 and 8 focus on the two designs that have an incorporated electrical isolation layer. Chapter 7 discusses MMC3 which has a thin oxide membrane for electrical isolation. Chapter 8 discusses the fabrication and experimental results of MMC4 which uses an AlN layer for electrical isolation. The final chapter, Chapter 9, concludes with a summary of the work presented, the contributions of this dissertation, and a discussion of future work.

1.13 Problem Statement and Purpose

Due to the inherent problems with straight microchannels, the manifold microchannel cooler (MMC) design is a promising alternative to reduce the pressure drop and allow for temperature uniformity. The goal of this research is to model, develop and demonstrate the use of a MMC fabricated directly into the substrate of an electronics package. The purpose of the research is to minimize the thermal resistance, reduce the package size, improve the thermal performance and reduce the system pressure drop.

This will accomplished by fabricating and testing the MMC directly fabricated into a substrate powered by multiple power devices. The design will also be optimized and understood by modeling the manifold channels and the microchannels with varying dimensions and geometries.

2 Literature Review

As was stated in Chapter 1, the trend in the electronics industry is towards higher power which means there is a need for advanced cooling technologies. Many types of cooling technologies are currently being investigated including: spray cooling, immersion cooling, microchannel cooling, heat pipes, pool boiling, and jet impingement. This thesis focuses on microchannel cooling, specifically manifold microchannel cooling, which reduces the pressure drop and allows for uniform cooling on the surface of the device.

2.1 Microchannel Research

Microchannels, as a cooling technology, were first proposed by Tuckerman and Pease in 1981 [8]. This was a seminal paper that sparked all subsequent research into microchannels. The paper presented a technology that could dissipate 790 W/cm^2 with a temperature rise of 71 ºC. This was demonstrated with straight rectangular microchannels that were 50 μm wide and 302 μm deep with 50 μm spacing for a heated area of 1 cm^2. The pressure drop and thermal resistances were measured to be 31 psi and 0.1 C/W, respectively. This paper showed thermal performance results that had never before been seen and introduced the benefits of microchannel cooling.

2.2 Manifold Microchannel Research

Microchannels have been shown to have extremely good performance while having a minimal volume. However, there are two main disadvantages of microchannel cooling: 1) large pressure drops and 2) non-uniform cooling. Manifold microchannels have been shown to alleviate both of these problems. The first normal flow heat exchanger (NFHX) was proposed by Valenzuela and Izenson in 1990 – a precursor to the

manifold microchannel, which was first proposed by Harpole and Eninger in 1991. Copeland wrote a series of papers looking at the performance of the channels over different operating and dimensional parameters. Various other authors have looked at the manifold microchannel design since then.

2.2.1 Valenzuela and Izenson – First NFHX - 1990

The first normal flow heat exchanger (NFHX), shown in Figure 2-1, was proposed in 1990 by Valenzuela and Izenson [9]. The fluid enters from the right side into a porous layer, which is made of a highly conductive material such as metal. The fluid then flows into grooves placed close to the heated surface with a larger cross-sectional area to minimize pressure drop. The majority of the heat transfer occurs in the porous layer; therefore, the porous layer must be in close contact with the exit grooves to ensure good heat transfer. The three main advantages to this type of design over a typical microchannel are the reduced pressure drop, the uniform heat transfer coefficient, and the high heat transfer effectiveness. The high effectiveness is due to the fact that the heat transfer is occurring as the fluid flows towards the heated surface; therefore, the fluid can be close to the wall temperature all along the heated surface. The reduced pressure drop is due to the fact that the majority of the pressure drop happens in the porous layer, which is only a short distance. Experimental results have shown a 0.04 psi pressure drop at a heat flux of 60 W/cm^2 and a heat transfer coefficient of 4 W/cm2-C, They proposed theoretically they could achieve up to 20 W/cm2-C with an effectiveness of 80% and pressure drop of 0.14 psi.

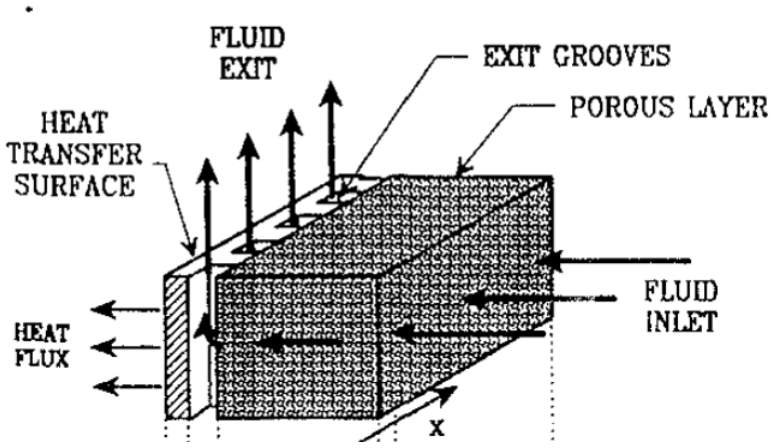


Figure 2-1: Normal flow heat exchanger concept. From [9]

The main disadvantage of this design compared to the manifold microchannel design is that this design has the main heat transfer surface area away from the heated surface while the fluid delivery occurs against the heated surface. It is more desirable to have the main heat transfer occur as close to the heated surface as possible.

2.2.2 Harpole and Eninger 1991

The first manifold microchannel design was proposed by Harpole and Eninger in 1991, as shown in Figure 2-2. [10] The design incorporated a high pressure side (H=inlet) and a low pressure side (L=outlet). The smallest microchannels were capped with a diamond sheet and fabricated by silicon microfabrication. The design has three layers of channels that subdivide the flow making smaller flow distances in the smallest channels to reduce pressure drop. Their results are completely numerical.

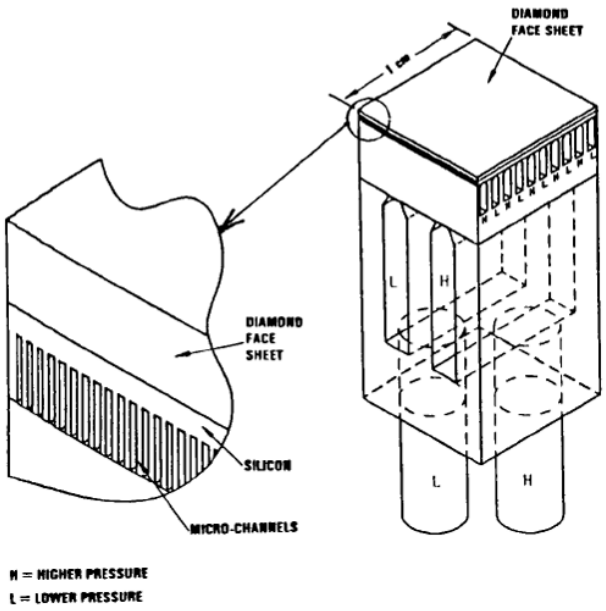


Figure 2-2: First manifold microchannel cooler design. From [10]

Harpole and Eninger did a numerical optimization study on the MMC, with the optimization charts shown in Figure 2-3. The first graph, Figure 2-3a, shows that either increasing the number of manifold channels (n) in a given area or increasing the flow rate decreases the temperature non-uniformity of the device. The research indicates that by doubling the number of manifold channels from 10 to 20, temperature non-uniformity decreases from about 2 ºC to 0.6 ºC for a flow rate of 25 cc/s. The allowable value of thermal non-uniformity depends on the application. The second graph, Figure 2-3b shows how increasing the number of manifold channels decreases the surface temperature rise above the inlet coolant temperature. This is a substantial difference since the difference between 10 and 30 channels makes a difference of about 10 ºC in all cases. The graph also shows that by increasing the microchannel fin height compared to the fin width has a small impact on reducing the chip temperature rise. Figure 2-3c indicates that increasing the pressure drop for a given flow rate, decreases the surface temperature rise. It also

shows that there is a certain temperature rise that cannot be avoided by the thermal resistance through the silicon, diamond and fluid. Figure 2-3d shows that there is an optimum fin to channel width ratio and the fins should be smaller than the channels.

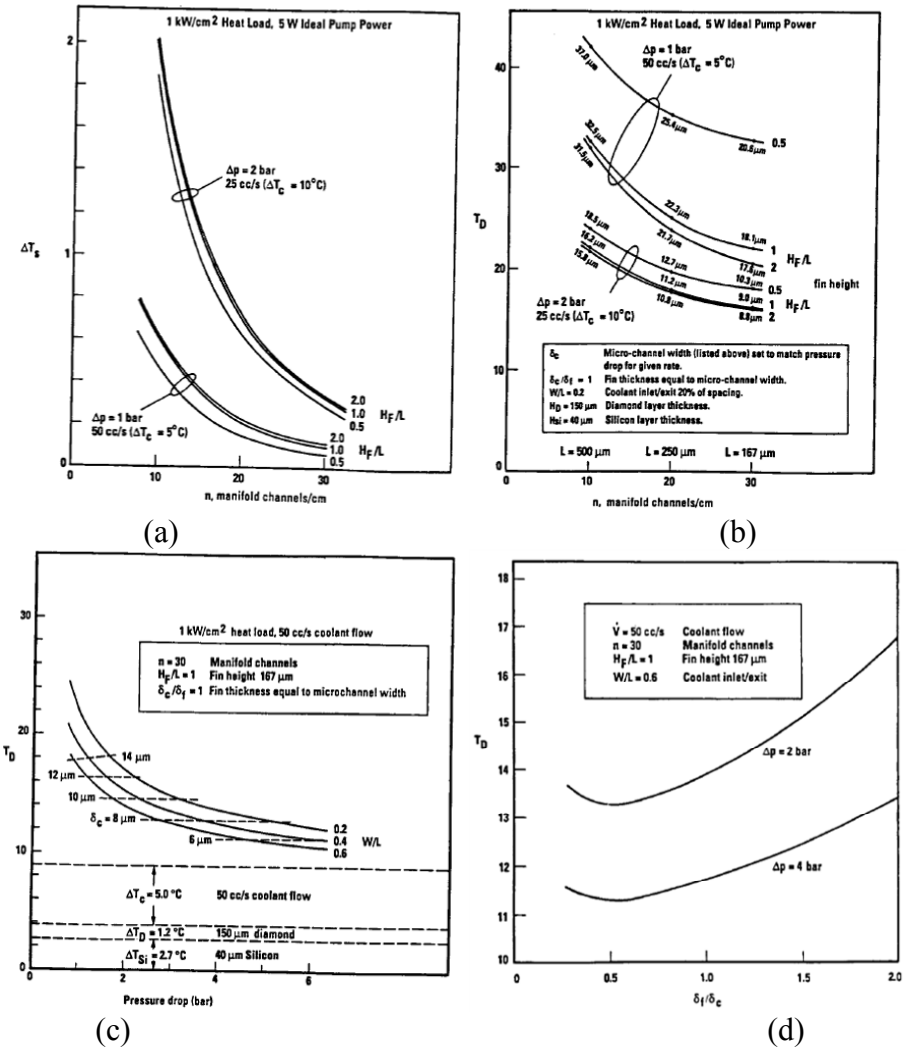


Figure 2-3: Optimization charts from Harpole and Eninger [10] (a) Graph showing how increasing the number of manifold channels decreases the chip temperature (b) Graph showing how increasing the number of manifold channels decreases the surface temperature rise above the inlet coolant temperature (c) Graph showing the relationship between an increase in pressure drop and a decrease in chip temperature rise (d) Graph showing the optimum fin to channel width ratio.

Harpole and Eninger did a very good job to introduce the MMC. Their results showed the following things:

- An optimum microchannel width to microchannel fin width is around 0.5 to 0.6
- Increasing the number of manifold channels has a significant effect on the performance both by decreasing the rise in chip temperature and decreasing the temperature non-uniformity. Therefore, the number of manifolds should be maximized.

The results presented by Harpole and Eninger show that MMC's are a very promising technology although the results are completely numerical and so have not been compared to experiment. They proposed that the MMC should have a flow rate of 50 cc/s per square centimeter of area. The optimum dimensions they proposed are an optimum MMC with the following dimensions: a manifold width of 200 μm, a manifold fin width of 130 μm, a microchannel height of 167 μm, a microchannel width between 7 and 14 μm, and a microchannel fin to width ratio from between 0.5 to 1. The heat transfer coefficients are on the order of 100 W/cm^2K for pressure drops of 2 bar. The authors suggest that for smaller heat fluxes the size of the microchannels and flow rates could be scaled accordingly. For example, for 100 W/cm^2 (a 10X decrease in heat flux), the microchannel size could be increased 10X to 100 μm and the flow rate could be decreased 10X to 5 cc/s. The authors suggest this would leave the device temperatures the same while reducing the pressure drop 100X to 0.01 bar.

This research is lacking in that is only models a single microchannel unit with no experimental validation. It does not account for the pressure drop in the manifold

channels or even the manifold depth, although it does estimate that the pressure drop would increase about 0.31 bar in the manifold channels. The microchannels are also proposed to be between 7 to 14 μm wide and 167 μm deep which is a depth ratio as large as 24, which is not very easy to fabricate. The proposed small microchannels also have a strong possibility of clogging.

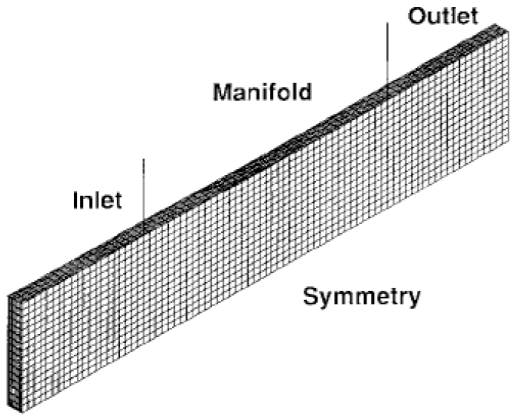
2.2.3 Copeland 1997

In 1997, David Copeland continued the research of Harpole and Eninger with further modeling. The paper titled "Manifold microchannel heat sinks: Isothermal analysis," by Copeland, et al., focused on a numerical analysis of the manifold microchannel (MMC) cooling design. [11] A MMC cooler uses multiple channel sizes to minimize pressure drop, maximize heat transfer, and improve temperature uniformity across the area of the cooled device. This paper discussed the analysis of a manifold microchannel cooler. The unit cell is shown in Figure 2-4b. It is a single half-channel of a single microchannel section. In Figure 2-5, it is shown by the yellow dashed line as half of a single cross section with symmetry boundary conditions on 3 of the 4 vertical wall surfaces. The other vertical wall (the one against the channel wall) is defined as being at a constant temperature. The wall against the heated surface is also defined as being at a constant temperature. A constant velocity and temperature is assumed at the inlet.

BOUNDARY CONITIONS OF THE UNIT CELL

$x = 0$	symmetry	$\frac{\delta U}{\delta x} = 0$	$\frac{\delta T}{\delta x} = 0$
$x = X$	symmetry	$\frac{\delta U}{\delta x} = 0$	$\frac{\delta T}{\delta x} = 0$
$y = 0$	isothermal wall	$U = 0$	$T = T_{wall}$
$y = D$	inlet	$U = U_{in}$	$T = T_{in}$
$y = D$	adiabatic wall	$U = 0$	$\frac{\delta T}{\delta y} = 0$
$x = D$	outlet	$\frac{\delta U}{\delta y} = 0$	$\frac{\delta T}{\delta y} = 0$
$z = 0$	symmetry	$\frac{\delta U}{\delta z} = 0$	$\frac{\delta T}{\delta z} = 0$
$z = C$	isothermal wall	$U = 0$	$T = T_{wall}$

(a)



(b)

Figure 2-4: Fluent analytical model (a) boundary test conditions and (b) the unit cell

The model was tested under 16 different conditions (eight different geometrical conditions and two flow rates). The list is shown in Table 2-1. The results of the analysis indicated a wider channel allowed for a much more uniform heat flux distribution. A deeper channel had a decreased velocity for the same volumetric flow rate but in general the heat flux distribution remained the same. A shorter channel caused a less uniform heat flux. A value of thermal resistance per unit area was defined and the lowest value happened at dimensions of X = 1000 μm, D = 200 μm and C = 28.3 μm and also at X = 400 μm, D = 200 μm, and C = 28.3 μm for both the 1 m/s and the 0.1 m/s flow. This shows that the skinniest and deepest channels are the best. Additionally, the length does not have a large effect on the thermal performance, though the longer channels have a substantially higher pressure drop (on the order of three times greater).

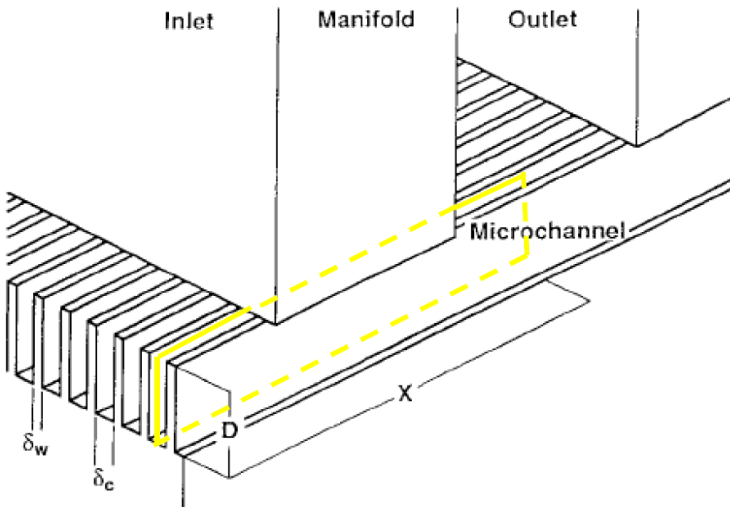


Figure 2-5: Schematic of the flow in a manifold microchannel design [11]

Table 2-1: Geometrical, fluidic, and thermal parameters

GEOMETRIC, FLUID, AND THERMAL PARAMETERS

Manifold channel pitch	X	400,	1000	μm
Microchannel depth	D	150,	200	μm
Microchannel half-width	C	28.3,	56.7	μm
Inlet velocity	U	0.1,	1.0	m/s
Wall temperature difference	ΔT_{wi}	10		°C.

A separate, more detailed analysis was performed on the channels with the dimensions of X = 1000 µm, D = 200 µm, and C = 28 µm (one of the thermally optimum points from above). Inlet velocity was set to 0.1 m/s, 0.2 m/s, 0.5 m/s, and 1 m/s, and the velocity distribution and heat flux distribution were determined in the unit cell. The velocity distributions are shown in Figure 2-6 and indicate the regions of maximum velocity change as the inlet velocity increases. At the lower velocities, two regions of maximum velocity were seen (one in the middle below the heated surface and one near the exit). As the velocity increased, the region near the exit disappears and the region below the heated surface becomes elongated. Stagnation points were also seen at the symmetry conditions near the heated surface, which is expected.

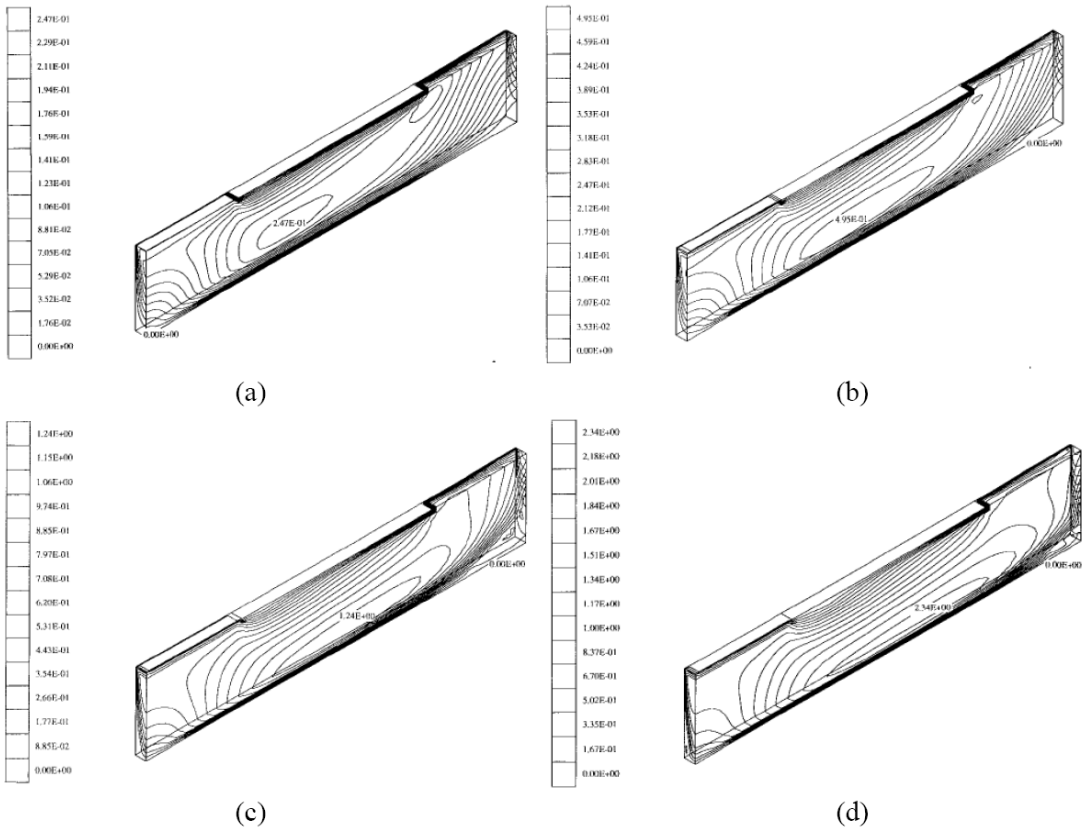


Figure 2-6: Velocity distribution for inlet velocities (a) 0.1 m/s (b) 0.2 m/s (c) 0.5 m/s and (d) 1.0 m/s

Similar plots were also made for the heat flux distribution throughout the channel. At lower flow rates the heat flux was relatively constant through the channel with a stagnation point below the exit, but as the flow rate increases, the stagnation point lessens and the heat flux becomes much more non-uniform.

Graphs of the numerical results are shown in Table 2-2. The table indicates thermal resistances as small as 0.25 C/W for a pressure drop as small as 0.384 psi (2650 Pa), a heat flux of 34.8 W/cm^2 and a flow rate of 1.0 m/s.

Table 2-2: Numerical results from Copeland [11]

Summary of Isothermal Numerical Results, $U = 1.0$ m/s

X	D	$\delta_c/2$	Q_{max}	V_{max}	ΔP	Θ_{wf}
μm	μm	μm	W/m^2	m/s	Pa	^{o}C/W
1000	200	56.6	1.86e5	2.15	6.57e3	0.42
1000	200	28.3	3.48e5	2.35	7.90e3	0.25
1000	150	56.6	1.87e5	2.76	12.12e3	0.48
1000	150	28.3	3.56e5	2.99	12.26e3	0.27
400	200	56.6	1.86e5	1.30	2.17e3	0.42
400	200	28.3	3.48e5	1.38	2.65e3	0.25
400	150	56.6	1.87e5	1.25	2.79e3	0.47
400	150	28.3	3.56e5	1.37	3.33e3	0.27

Summary of Isothermal Numerical Results, $U = 0.1$ m/s

X	D	$\delta_c/2$	Q_{max}	V_{max}	ΔP	Θ_{wf}
μm	μm	μm	W/m^2	m/s	Pa	^{o}C/W
1000	200	56.6	1.55e5	0.25	146	1.70
1000	200	28.3	2.15e5	0.25	280	0.91
1000	150	56.6	1.62e5	0.33	230	1.78
1000	150	28.3	2.37e5	0.33	392	1.04
400	200	56.6	1.55e5	0.13	47	1.70
400	200	28.3	2.15e5	0.15	97	0.92
400	150	56.6	1.62e5	0.14	59	1.85
400	150	28.3	2.37e5	0.16	109	1.04

While the results are interesting to show the velocity profiles within a microchannel unit, it does nothing to look to optimize the thermal performance of the channels. Only two data points are taken for each parameter and therefore it is difficult to determine the real effect each parameter has on the performance. There is also no experimental data to compare the results to and only half a single microchannel portion was modeled so seeing the flow in the entire structure is not possible.

2.2.4 Ng and Poh 1998 and 1999

Ng and Poh also did a numerical study on the manifold microchannel designs [12,13] using ANSYS/FLOTRAN. Only the portion of the microchannel was modeled, as can be seen in Figure 2-7. This was the same portion that was modeled in the previous Copeland study.

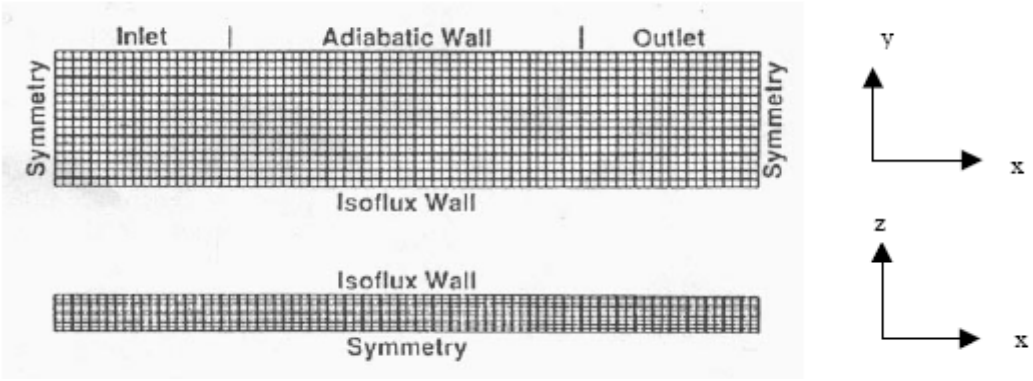


Figure 2-7: The modeled microchannel portion with the boundary conditions and grid. From [13].

Sixteen conditions were modeled, as shown in Figure 2-8, which are the same conditions modeled in the previous Copeland study. The analysis was performed at two different inlet velocities (1.0 m/s and 0.1 m/s). The microchannel length measures from the center of one manifold to the center of the next and two of these were modeled (1000 μm and 400 μm). Two microchannel depths (D) were also modeled for each value of microchannel length and inlet velocity (200 μm and 150 μm). In all the models, the microchannel fin thickness was taken to be the same as the microchannel width. Two different microchannel widths (δ_c) were used in this study, 56.6 μm and 113.2 μm.

No.	X	D	$C = \delta_c/2$	Q_w
1	1000	200	56.6	4.42e5
2	1000	200	28.3	2.48e5
3	1000	150	56.6	5.49e5
4	1000	150	28.3	3.17e5
5	400	200	56.6	4.42e5
6	400	200	28.3	2.48e5
7	400	150	56.6	5.49e5
8	400	150	28.3	3.17e5

(a)

No.	X	D	$C = \delta_c/2$	Q_w
9	1000	200	56.6	4.42e4
10	1000	200	28.3	2.48e4
11	1000	150	56.6	5.49e4
12	1000	150	28.3	3.17e4
13	400	200	56.6	4.42e4
14	400	200	28.3	2.48e4
15	400	150	56.6	5.49e4
16	400	150	28.3	3.17e4

(b)

Figure 2-8: 16 test conditions for the model (a) for 1.0 m/s inlet velocity (b) for 0.1 m/s inlet velocity

The numerical results of each case are shown in Table 2-3. Looking at the effect of length, this had no effect on the hydraulic diameter of the channel, but the increase in length decreased the average velocity through the channel. These effects complement each other causing only a slight increase in thermal resistance as the length is reduced. As the microchannel depth is decreased, the thermal resistance increases. Also, as the microchannel width is increased, the thermal resistance also increases. As the inlet velocity decreases, the thermal resistance increases.

Table 2-3: Numerical and analytical results from each test condition. From [13].

No	Numerical					
	ΔT_{max}	V_{max}	ΔP	fRe	Nu	θ_{wf}
1	81.964	1.76	5.624e3	10.89	3.61	0.77
2	56.735	1.93	6.799e3	4.9	1.79	0.54
3	83.966	2.361	8.291e3	12.78	3.91	0.79
4	56.449	2.435	10.209e3	6.385	2.14	0.53
5	91.181	1.311	1.916e3	9.27	3.25	0.86
6	59.661	1.374	2.22e3	4.00	1.70	0.56
7	108.902	1.404	2.642e3	10.18	3.01	1.03
8	62.755	1.454	2.99e3	4.68	1.92	0.59
9	46.471	0.2077	124.041	2.4	0.64	6.66
10	17.512	0.2588	274.324	1.98	0.58	3.65
11	52.532	0.2591	184.553	2.84	0.62	4.96
12	52.464	0.2566	314.654	1.97	0.23	4.95
13	48.263	0.1412	44.617	2.16	0.61	5.97
14	17.435	0.1626	90	1.62	0.58	3.01
15	52.539	0.1459	51.166	1.97	0.62	6.05
16	21.638	0.1676	102.289	1.6	0.56	3.46

Comparing these results to Copeland's previous results shows similar results although the thermal performance of this model does not appear to be as good. For data set number 6, the above table indicates a thermal resistance of 0.56 C/W (Copeland showed 0.25 C/W) for a pressure drop of 0.322 psi (2220 Pa) (Copeland was 0.384 psi), a heat flux of 24.8 W/cm^2 (Copeland was 34.8 W/cm^2) and a flow rate of 1.0 m/s.

Therefore, for the same dimensions and inlet velocity, Ng and Poh's model showed a much worse thermal resistance, a slightly better pressure drop for a much lower heat flux. There are clear discrepancies between the two models.

The same problem with this model is that it is difficult to see a trend from this study because only two points are studied for each variable. At least three points are necessary to see a trend and so no optimization can be seen from this study. Additionally, there is no experimental data for this study.

2.2.5 Ryu 2003

In the paper entitled, "Three-dimensional numerical optimization of a manifold microchannel heat sink," by Ryu et al., the authors use numerical techniques to optimize the manifold microchannel design. [14] The optimum is found by minimizing the thermal resistance for a given pumping power. The authors found that the manifold microchannel design reduces the thermal resistance by more than 50% and the temperature uniformity is improved by ten times over the traditional microchannel design for a constant pumping power.

The geometry used in the study to perform the analysis is shown in Figure 2-9. Due to the symmetry conditions of the manifold design only a small section of the geometry is considered. The manifold was considered to be made of copper and the microchannels of silicon. A constant heat flux was applied to the top of the microchannels and water was used as the cooling fluid.

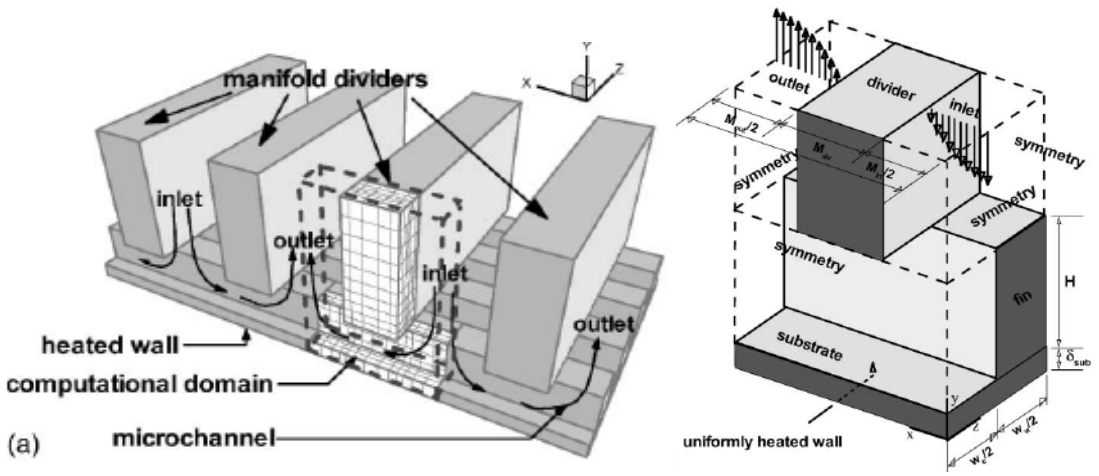


Figure 2-9: Manifold microchannel geometry used for the modeling. From [14]

The design variables that were evaluated were the channel depth, the channel width, the fin thickness and the inlet/outlet ratio. Figure 2-10 shows that for a given condition, there is an optimum geometry to minimize the thermal resistance. The figure also shows that some variables impact the thermal performance more than others; namely, the channel width and depth. If the channel depth is less than optimum, as shown in Figure 2-10a, the thermal resistance rises more than if the channel depth is greater than the optimum. A similar trend is also seen in Figure 2-10b for the channel width. The fin thickness is not impacted as significantly if it is not at the optimum. Figure 2-10c shows that an optimum inlet to outlet ratio should be about two. Therefore, the inlet should be two times bigger than the outlet although only a small increase in performance is seen after about 1.5.

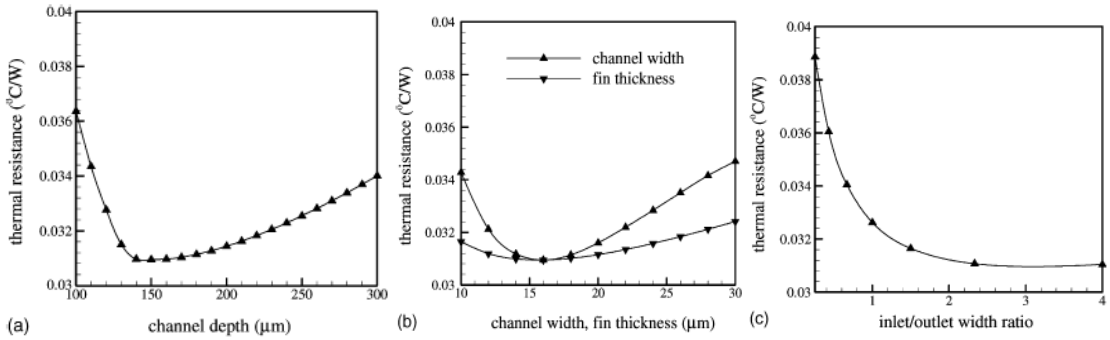


Figure 2-10: Graphs showing the relationship of the channel depth, width and fin thickness

The paper also found that 95% of heat is removed by the fins, showing they are very efficient at heat removal. The temperature on the heated wall was also observed to be very uniform. The lowest temperature on the surface was observed near the entrance of the channel just past the stagnation point whereas, the highest temperature is found near the inlet and outlet stagnation points. The thermal resistance at the optimal values was found to be 3.1×10^{-2} C/W. It was pointed out that if the size of the manifold was reduced, the thermal resistance could be decreased. The proposed microchannel dimensions are on the order of 15 μm wide and 150 μm deep which could be difficult to fabricate and is prone to particulate clogging.

This paper does a good job to try and optimize the dimensions for thermal performance but it still does not compare to experimental data. It also does not discuss the pressure drop in the channels and does not look to minimize the pressure drop, just the thermal resistance. Optimization should be made for both the pressure drop and the thermal performance.

2.2.6 Escher 2009 and 2010

In the papers entitled, "Experimental Investigation of an Ultrathin Manifold Microchannel Heat Sink for Liquid-Cooled Chips" [15] and "A novel high performance, ultra thin heat sink for electronics" [16] by Escher et al., the authors discuss a manifold microchannel unit with impinging slot jets. The design is shown in the top of Figure 2-11 indicating slot regions at the top of the manifold channel as the fluid enters the microchannel region. The microchannels were assumed to be fabricated directly in the backside of the chip.

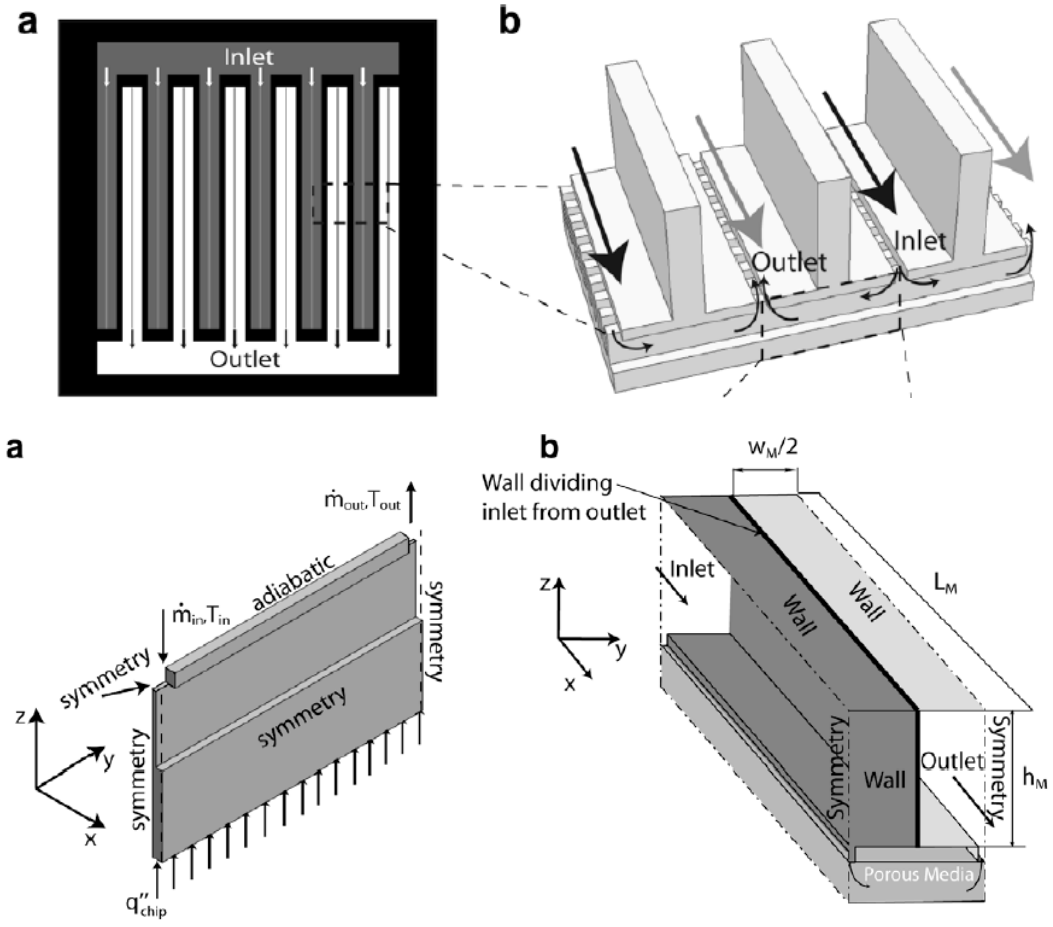


Figure 2-11: Eschers manifold microchannel design with impinging slot jets. From [16].

The authors performed a numerical simulation with the modeled geometry shown in the bottom half of Figure 2-11, assuming a porous region for the microchannels. The models showed that the system pressure drop was largely dependent on the slot width and channel width while the thermal performance was dominated by the channel width. The authors also addressed the non-uniformity going down the channel and designed a tapered inlet and outlet to reduce the non-uniformity to less than 4%. A semi-empirical model was also developed with an error of <15% for both the thermal performance and pressure drop. The semi-empirical model was used to do a sensitivity analysis on a number of parameters: channel width, number of manifold channels, fin thickness to channel width ratio and pumping power on the performance of the heat sink. The optimums found were dependent on the tradeoff between the thermal performance and pressure drop. The models showed an optimum design with a thermal resistance of 0.087 K/(W/cm^2) for flow rates <1 L/min and a pressure drop <0.1 bar to cool 750 W/cm^2 with a chip temperature rise of 65 C. The author compared to literature for microchannels showing a 20X smaller pumping power for the same thermal performance.

In addition to the numerical model, it was also fabricated and tested. Experimentally the authors looked at the effect of the width of the microchannels, the number of manifolds, the volumetric flow rate, and the pumping power. The experiments correlated to the semi-empirical to within 25%. The number of manifold and the channel width were shown to dominate the performance. The best experimental thermal performance was shown to be 0.09 K/(W/cm^2) at 1.31 L/min and a pressure drop of 0.22 bar at 700 W/cm^2 and a chip rise of 65 °C.

This paper shows a good review of the manifold microchannels with incorporated slot jets which improve the thermal performance but cause the system pressure drop to increase. Additionally, the microchannels were assumed to be fabricated directly into the backside of a die which is unlikely in power electronics which have a backside contact. The model also assumed a porous media instead of microchannels which limits its accuracy.

2.2.7 Summary of MMC Literature

In conclusion is a brief summary of the work to date on the MMC design. Tuckerman and Pease first proposed the straight microchannel design in 1981 and showed experimentally they could achieve 790 W/cm^2 with a temperature rise of 71 ºC and a thermal resistance of 0.1 C/W. But the pressure drop in the channels was very high, the authors measured 31 psi. Many years of research went into microchannels but they still have the problems of high pressure drops and non-uniform cooling. Therefore, Valenzuela proposed the first normal flow heat exchanger (NFHX) in 1990 to try to reduce the pressure drop while still allowing improved performance. They claimed pressure drops could be reduced 1 to 2 orders of magnitude compared to standard microchannels. They measured experimentally up to 60 W/cm^2 with a pressure drop of only 0.04 psi and a heat transfer coefficient of 4 W/cm2-ºC but theoretically up to 10 W/cm2-ºC with an effectiveness of 80% and pressure drop of 0.14 psi. The major flaw of this design is that fluid transport layers are located against the heated surface and the porous layer is located away from the heated surface. This significantly reduced the thermal performance.

Therefore, in 1991, Harpole and Eninger proposed the first MMC. The study was completely numerical and only looked at a single microchannel section. The models showed heat transfer coefficients on the order of 100 W/cm^2K for pressure drops of 1 to 2 bar (14.5 to 29 psi). It also showed that for a heat flux of $1kW/cm^2$, the chip temperature rise was only 17 ºC for a pressure drop of 2 bar (29 psi). The chip temperature uniformity in all cases was less than 2 ºC.

In 1997, Copeland, et. al, continued the research previously done by modeling the velocity contours of the microchannel unit inside the MMC. This study was performed to mainly see the velocity profiles into the microchannels and not to optimize the dimensions. A downfall of this research is that only two points were modeled for each parameter therefore the effect of each parameter is very difficult to see.

In 1999, Ng and Poh repeated Copeland's model using the same dimensions but with a different modeling program and achieved different results. The thermal performance did not seem as good in this model as in Copeland's. But this paper has the same disadvantages as Copeland's in that it only uses two data points for each parameter, has no experimental validation, and only models a single microchannel unit with no manifold.

The most recent MMC study was performed in 2003 by Ryu. This was also a strictly numerical study but did include a section of the manifold in the model and did look to optimize performance by looking to reduce the thermal resistance. It found thermal resistance values around 0.031 C/W, lower than in previous studies. But the study did not consider pressure drop or experimental methods.

Therefore, the existing research that has been done on the MMC design is lacking. There is very little experimental data and the modeling has only been done on small sections of the manifold design. No modeling has been done to date looking at the entire length of a manifold to see how the microchannels are affected on the entire length. Also no research has been done to look at the effect of the manifold sizes on the microchannels. In addition, no research has looked into implementing this into the substrate of an actual power module and how to connect the flow channels to powered devices.

A slight alternative to the traditional MMC design was proposed by Escher incorporating slot jets between the manifold channels and the microchannels. Both models and experiments were used to validate and test the design. The best experimental thermal performance was shown to be 0.09 K/(W/cm^2) at 1.31 L/min and a pressure drop of 0.22 bar at 700 W/cm^2 and a chip rise of 65 °C

Other researchers have proposed alternative designs to the MMC to mitigate the effects of temperature non-uniformity and pressure drops. Some of these designs are discussed in the following section.

2.3 Similar Alternative Technologies to the Manifold Design

The problems of non-uniform cooling and high pressure drops are well known problems in the microchannel industry. Many researchers have looked into ways of minimizing these effects. Some of these are shown in this section.

2.3.1 Two-layered microchannel heat sink concept

The two-layered microchannel heat sink concept, depicted in Figure 2-12, was first proposed by Vafai and Zhu. [17] The concept is a simple adaptation of the straight microchannels by stacking two sets of microchannels of top of each other with flows in opposite directions. The goal of this design is to minimize the streamwise temperature rise along with the pressure drop.

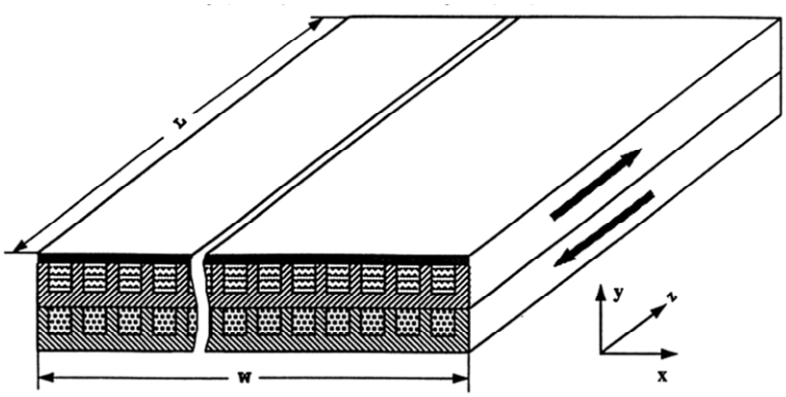
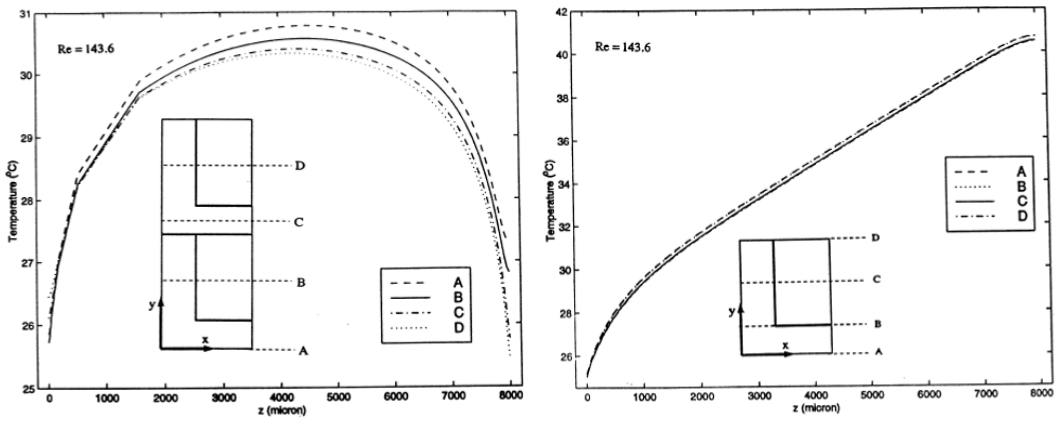


Figure 2-12: Schematic of the two-layered microchannel heat sink concept. From [17].

Figure 2-13 shows the numerical results of the temperature profile along the channel for both the two-layered and single layered (standard microchannel) concepts. The temperature raises only about 6 ºC in the first case and about 15 ºC in the later, showing substantial improvement.



(a) (b)

Figure 2-13: Temperature plots along the channel for (a) two-layer design (b) single layer design. From [17].

Further improvement was made on this design by Cheng [18], who included a passive mixing structure which enhanced mixing by fabricating small V-shaped grooves inside the channel. Figure 2-14 indicated the improvement of the thermal resistance by both the stacked channels and the passive mixing structures.

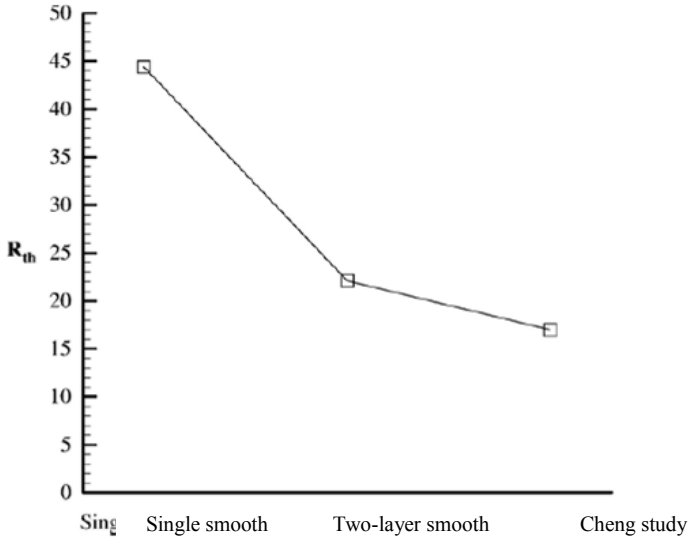


Figure 2-14: Comparison of the thermal resistance for the single smooth microchannel, a two-layer smooth microchannel and a microchannel with mixing enhancements. From [18]

In comparison to the manifold microchannel design, the two-layered microchannel is a simpler design. The fabrication is simpler, and the knowledge on standard microchannel flow is better understood. However, there is still a temperature differential across the chip surface – even though it was reduced – and the pressure drop will be higher due to the small cross-sectional channels. The stacked channel design could be more complicated because it is necessary to have fluidic connections on each side.

2.3.2 Alternative Configuration of Manifold Microchannels

An alternative geometrical configuration to the manifold design was proposed by Weng et al. in 2007 and is shown in Figure 2-15 [19, 20]. This configuration has both the manifold and microchannels in the same plane. The design is proposed to increase the heat transfer surface area and improve overall heat transfer performance. The channels are micro-fabricated using a combination of KOH wet etching and electroplating.

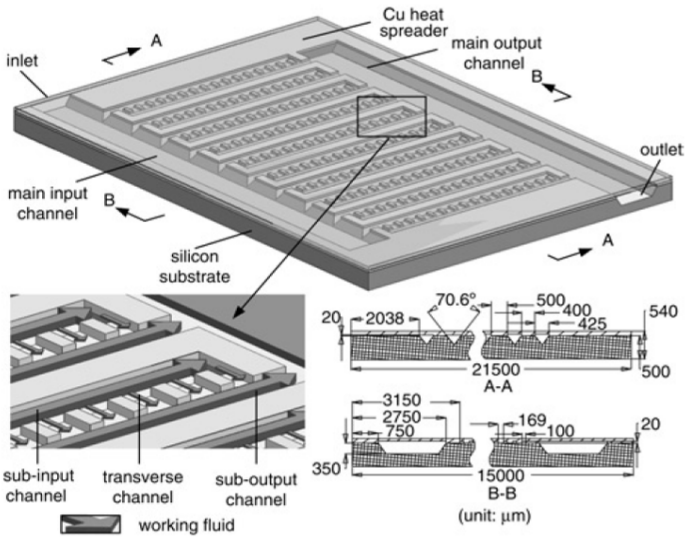


Figure 2-15: Alternative geometry of a manifold microchannel cooler. From [19]

The results of this new geometry compared to a standard straight channel are shown in Figure 2-16. The straight channel for comparison is the manifold channels without the cross-over channels connecting them. As can be seen in the figure from the maximum temperature plots, this design can achieve a ΔT of less than 5 ºC for a flow rate of 22 ml/min to 33ºC for a flow rate of 2 ml/min. The authors reported a 75% increase in maximum heat flux of the new design and a more efficient heat transfer.

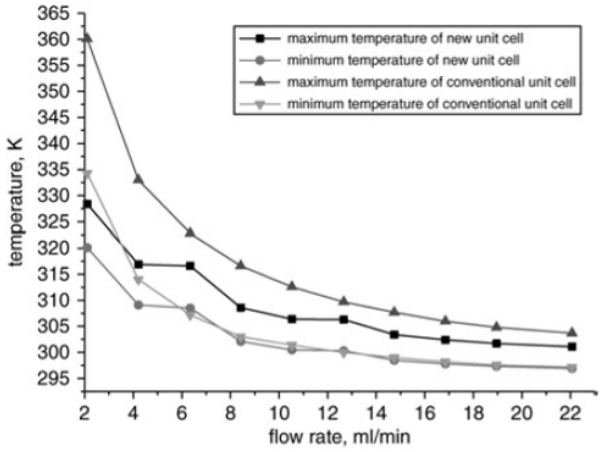


Figure 2-16: Comparison of the new manifold geometry to a straight channel. From [19]

In comparison to the multi-level manifold geometry (as in the MMC designs), this planar geometry has a potentially simpler fabrication sequence because the entire structure can theoretically be fabricated in a single DRIE etch step, although the authors did not use DRIE. However, the amount of microchannels that can fit into the same area is substantially decreased, which means a reduced cooling potential.

2.3.3 Stacked Microchannels

Wei and Joshi [21, 22, 23] have proposed the concept of stacked microchannels which are microchannels that have been layered over one another and bonded. The results show that the pressure drop is reduced by a factor equal to the number of layers compared to traditional microchannels. They also show a pumping power that is reduced by 30% compared to traditional microchannels. The fluid also flows in opposite directions which improves the temperature uniformity. A schematic of the stacked microchannels is shown in Figure 2-17. The structure is a five wafer stack where all the layers are fabricated using silicon micromachining. The layers are bonded by silicon-silicon fusion bonding. The structure was tested for both channel flow in the same direction (parallel flow) and in opposite directions (counterflow).

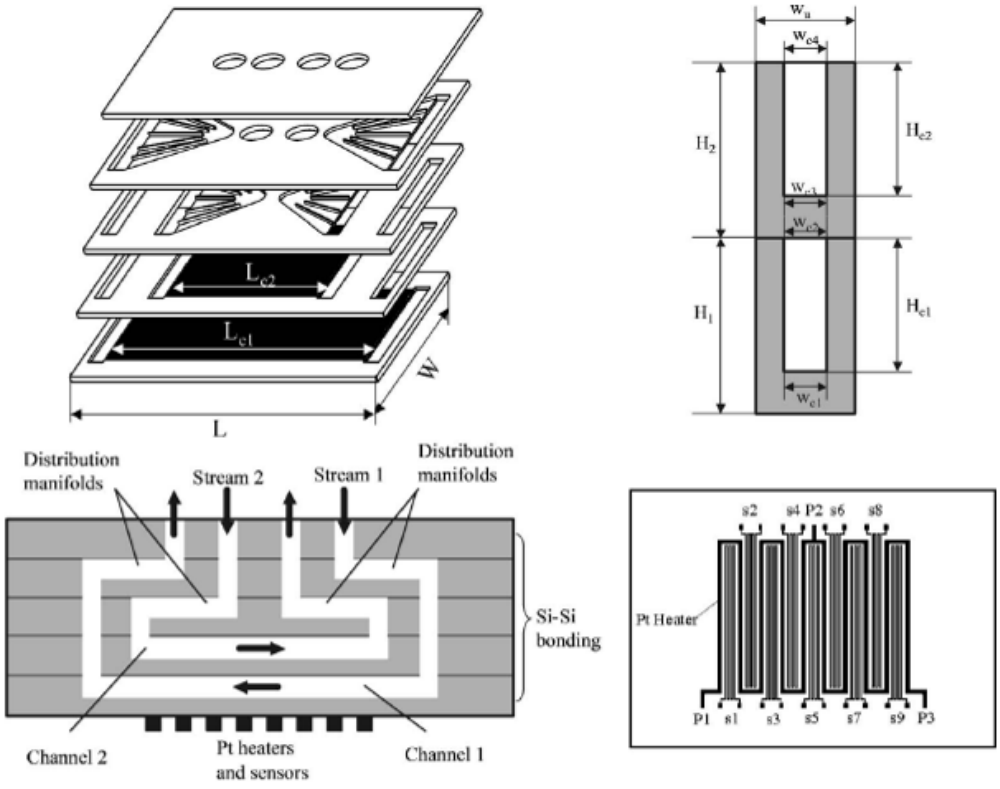


Figure 2-17: Schematic of the stacked microchannel design proposed by Wei. From [23].

The temperature distribution is shown in Figure 2-18 for both the counter flow and the parallel flow cases. The temperature rises linearly for the parallel flow and has a maximum in the middle for the counter flow case.

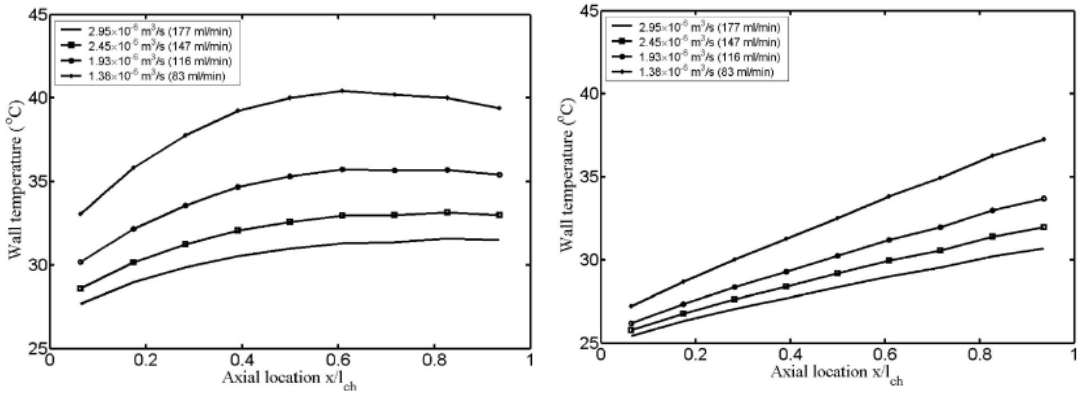


Figure 2-18: Temperature distribution along channel for (a) counterflow (b) parallel flow. From [23].

The flow rate compared to thermal resistance for both flow conditions is shown in Figure 2-19. At low flow rates the parallel flow performs better and at higher flow rates, both cases perform similarly, with thermal resistivity values less than 0.1 C/(W/cm^2)

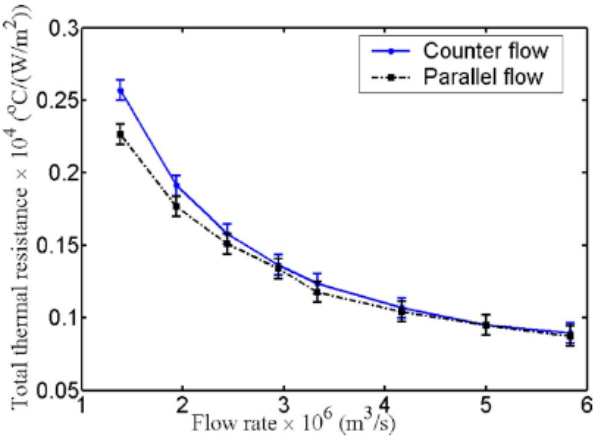


Figure 2-19: Flow rate versus thermal resistance for the parallel and counter flow. From [23].

The results showed that the counter flow design was better at temperature uniformity. At the same flow rate, the counter flow showed 40% less non-uniformity than the parallel flow. Experiments were also performed with different flow rates on each channel level. In both fluid designs, the thermal resistance was decreased when more fluid was flowed through the channels closest to the resistive heater but the pressure drop was also found to increase significantly.

In general, the results of such a design are promising. But in comparison to the MMC design, this design is complex and thus costly and difficult to manufacture. The thermal performance is similar to what can be achieved through MMC, but the MMC shows better temperature uniformity across the surface of the device.

2.3.4 Fractal/Bifurcating Tree-Like Channels

Another alternative to the MMC design is based in nature and uses fractal channels, shown in Figure 2-20. Both Chen and Cheng [24] and Escher [25] compared the fractal network to a microchannel network.

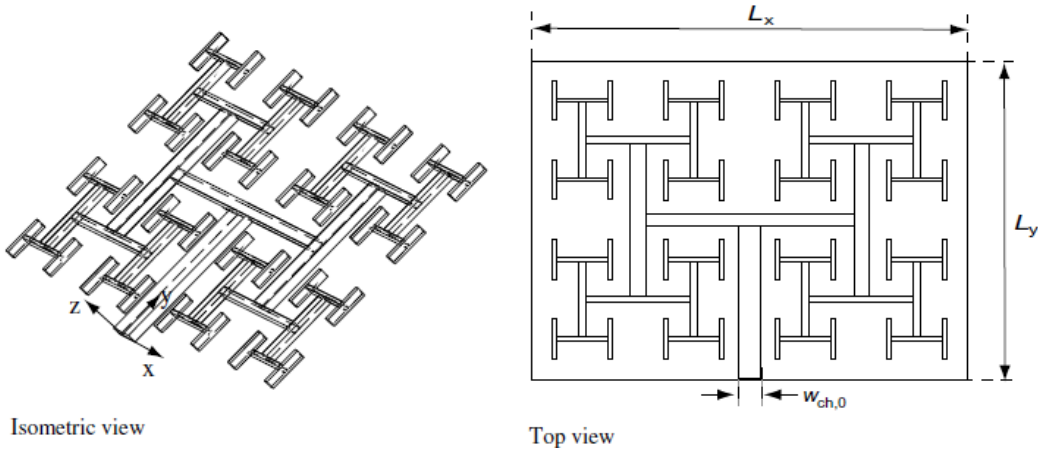


Figure 2-20: Schematic of fractal microchannels as a micro heat exchanger. From [25].

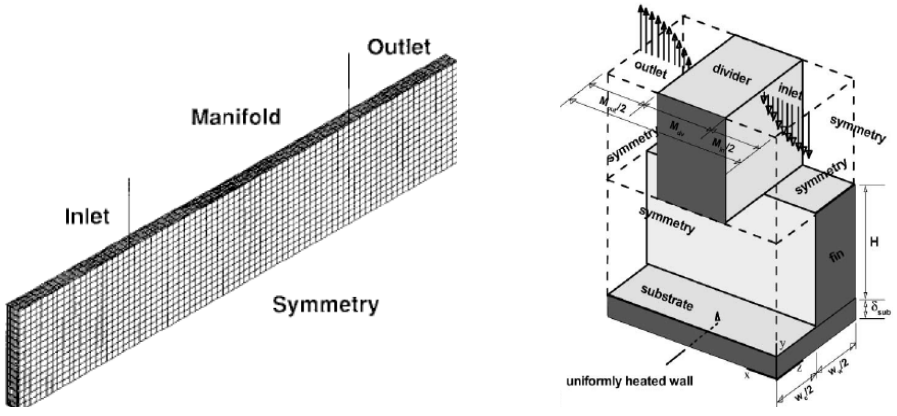
Chen and Cheng used a model to compare various channel hydraulic diameters and number of branching levels to show that increasing the number of branching levels enhances the efficiency and reduced the pressure drop as compared to a microchannel design. Escher had a dual layer bifuricating microchannel, one for fluid into the structure and one for fluid out. The author found the microchannels perform better than the fractal microchannels with almost four times more heat removed for the same pressure drop.

The fabrication sequence for a fractal network would be equivalent in complexity to a MMC design which both involves etching complicated channels into a material. However, the fractal channels have thermal performance less than that of the microchannels showing they would not be as effective as a MMC structure.

3 Modeling

This chapter and the next covers the modeling that was performed to help understand the complicated relationships between dimensions, thermal performance and pressure drops in MMC structures. In order to qualify the testing results and to create predictive equations, modeling must be performed. With the aim of more completely understanding the complex fluid structure, a series of models have been performed using the commercially available Computational Fluid Dynamic (CFD) software Fluent. The mesh generator that was used for this analysis was Gambit.

The main difference of the modeling presented in this work compared to previous models, is that it includes both the inlet and exit manifold channels along with all the microchannels. Previous models just modeled either just a single microchannel unit cell, as shown in Figure 3-1a [11, 12, 13] or modeled a single microchannel unit cell along with a portion of the manifold as shown in Figure 3-1b [14].



(a) (b)

Figure 3-1: Model sections from previous literature showing the modeling of (a) just a single microchannel unit [From 11] and (b) microchannel unit with the corresponding manifold [From 14]

A main contribution of this work is to show that there is extreme variation in the flow parameters along the length of the chip and so it is not sufficient to model a MMC structure without including all the microchannels. For example, some models have shown a >10X difference in flow rates between the first and last microchannels.

The modeling results are shown in both this chapter and the next. This chapter covers the general overview of the modeling and a complete analysis of a single geometry. Section 3.1 includes the general model structure and dimensions, the boundary conditions and the basic modeling procedure. Section 3.2 discusses the analytical pressure drop calculations. Section 3.3 discusses briefly mesh convergence and independence, with a full analysis is shown in Appendix D. The final section in this chapter, Section 3.4, is a complete modeling study of a single geometry showing the thermal profiles, pressure drop plots and velocity profiles. The next chapter, Chapter 4, covers the results of a parametric analysis of various geometric parameters including the manifold width, manifold fin width, manifold height, microchannel fin with and microchannel width.

The main goals of this chapter are to:

a. Develop plots showing the tradeoff between the pressure drop and thermal performance for various flow rates.
b. Show the benefit of the MMC design over a standard microchannel structure.
c. Show that modeling a single microchannel is not sufficient to understanding the complex flow in a manifold microchannel structure.
d. Work to develop general rules of thumb and equations such that designers of manifold microchannel structures can utilize.

3.1 Model Structure, Boundary Conditions and Expected Results

A basic manifold structure is shown in Figure 3-2 with the rectangular box indicating the portion modeled in this study which includes the inlet and exit manifold channels along with all the microchannels. The manifold inlet and outlet channels are included to generate more realistic results to the flow profiles. Depending on the model, the number of microchannels varied between 2 and 19. The modeled geometry includes only half of both the inlet and exit manifold channels allowing a symmetry assumption to be used for simplicity and to reduce computational time. This assumption is reasonable because the center manifold channels will have similar flow structures and performance. The manifold channels towards each side of the device will most likely perform differently and the results from this study should not be used to approximate their performance. The results from this study are a reasonable approximation of the overall performance of the system because the performance of the system will be primarily based on the performance of the center manifold channels which are located under the hottest part of the chip and cover the majority of the underside of the device.

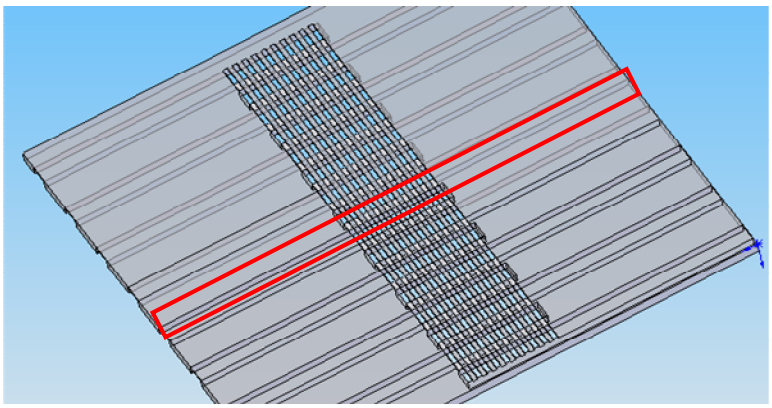


Figure 3-2: Schematic showing a complete MMC structure with the red box indicating the portion that will be modeled in this study

The model structure, illustrated in Figure 3-3, consists of a section of the chip and the portion of the cooling structure directly below the chip. The figure shows the three main layers of the MMC structure: the chip, the wafer containing the microchannels, and the wafer containing the manifold channels.

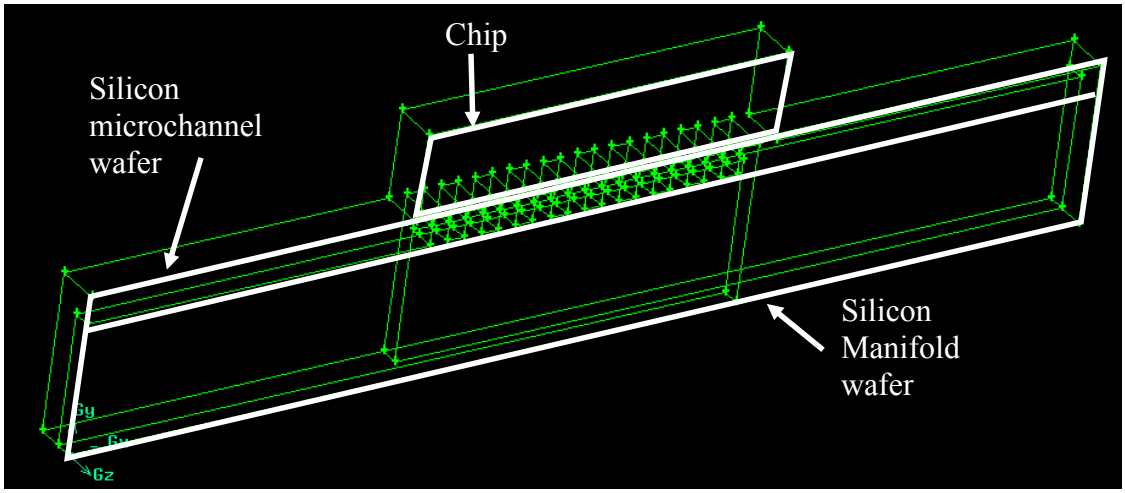


Figure 3-3: Schematic of the overall geometry of a typical model showing the chip on the top with the microchannel structure directly below it and the manifold structure on the bottom

A view of the model geometry from various perspectives is shown in Figure 3-4. All models consisted of a two mm long inlet and exit channels into and out of the microchannels. The chip size is set to be slightly larger than the microchannel cooling allowing for a bond area.

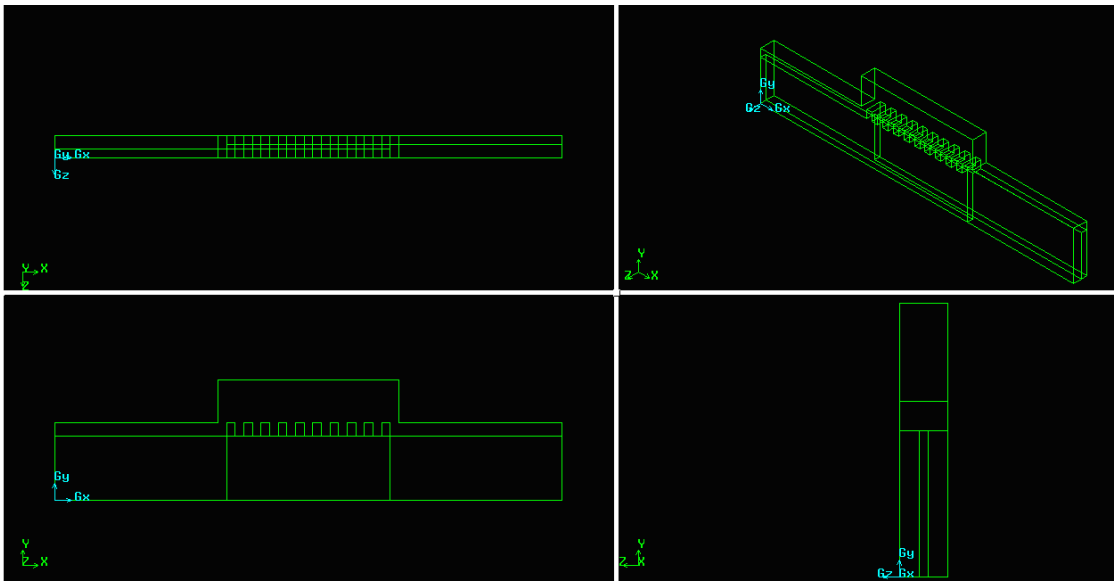


Figure 3-4: Sample of the model structure from various perspectives.

The model is comprised of two volumes shown in Figure 3-5: a solid volume (shown in green) defined as silicon and a fluid volume (shown in red) defined as water. In actuality, the solid would consist of multiple volumes: the chip, die attach, silicon microchannels and silicon manifold channels. It may also include an optional dielectric layer between the device and the fluid. But for simplification, the solid has been assumed to be one material with the properties of silicon. This is a reasonable assumption because the manifold and microchannel are fabricated out of silicon and devices are typically silicon. The devices alternately could be made of silicon carbide, which has similar thermal properties to silicon. There would be an additional thermal resistance in the die attach layer which is knowingly neglected but neglecting this should have no impact on how the manifold microchannel perform. The device temperature would just be higher in actuality. It should be noted that the simulations do not include pressure losses or any heat transfer occurring outside the modeled unit-cell region.

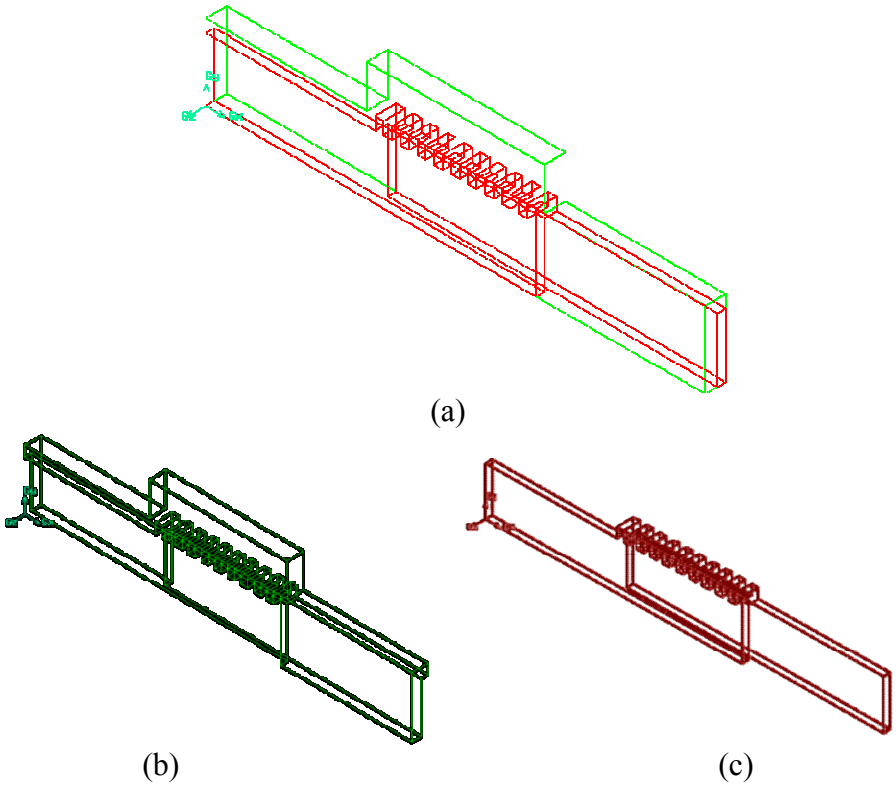


Figure 3-5: Schematic of the two volumes (a) shows the two volumes interacting (b) solid volume (c) fluid volume

A complete summary of the model procedure can be read in Appendix C. A depiction of the final meshed structure is shown in Figure 3-6.

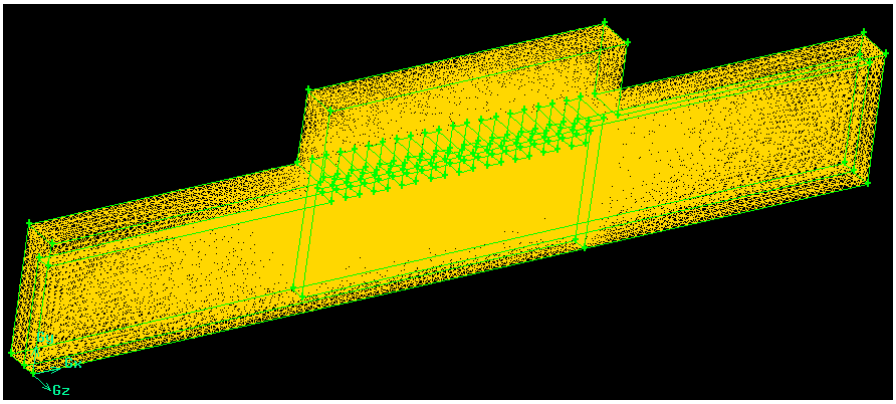


Figure 3-6: Figure showing an example of a meshed structure

3.1.1 Boundary Conditions

The model employs four main boundary conditions:

- Constant velocity inlet
- Symmetry in the transverse direction about both the inlet and outlet manifold channels
- Constant heat flux applied evenly across the upper surface of the chip ($q'' = 400$ W/cm^2)
- Laminar flow

In most cases, we are interested in the volumetric flow rate into the model, but this can easily be calculated to a corresponding velocity by dividing the volumetric flow rate by the inlet area of the manifold channels. In actuality, the flow velocity into the manifold will not be a constant velocity, but for the purposes of this study it is a reasonable assumption.

Symmetric boundary conditions are imposed on each side. The boundary between one unit cell and the next is through the centerline of both the inlet and outlet, as was shown in Figure 3-2. The fluid entering each manifold is assumed to evenly split between the microchannels on each side, thus allowing symmetry.

Constant heat flux is another boundary condition that is imposed and applied evenly to the top surface of the chip in the model. This is a good assumption as in reality typically there is a constant heat flux that can be measured on the top of the device. In some cases, there might be slight imperfections in the device which would cause non-uniform heating of the device or hot-spots. But this is outside the scope of this model.

Laminar flow is a reasonable assumption because in almost all cases modeled, the Reynolds number of the fluid is well below the transition regime. Therefore, a laminar assumption has been made for all channels which simplified the computation and allowed for shorter model run times.

External surface convection was not incorporated into the model to allow the cooling to strictly occur as a result of the manifold design. While this does not model reality, it gives a purer understanding of the effect of manifolding microchannels. If the external surface convection was incorporated, the average device temperature will decrease thus showing better performance, therefore, neglecting the surface convection is a conservative result in terms of thermal performance.

3.1.2 Model Results

Once the model is run, a variety of results are gathered. The two most important results are the average device temperature rise and the system pressure drop. At the completion of each run, the following data is extracted:

- Average pressure at the inlet = p_{in}
- Average pressure at the outlet = p_{out}
- Average fluid temperature at the inlet = T_{fluid_in}
- Average fluid temperature at the outlet = T_{fluid_out}
- Maximum device temperature = T_{chip_max}
- Minimum device temperature = T_{chip_min}
- Average device temperature = T_{chip}
- Average velocity at the inlet = v_{in}
- Average velocity at the outlet = v_{out}

- Average velocity at the center of each of the microchannels
- Average pressure at the center of each of the microchannels
- Average temperature at the center of each of the microchannels
- Temperature profile along the center line of the chip

From these data points, a variety of data is calculated for each model and compiled into a spreadsheet for analysis, including:

- System pressure drop:

$$\Delta p = p_{out} - p_{in} \tag{3-1}$$

- Temperature rise of fluid:

$$\Delta T_{fluid} = T_{fluid\_out} - T_{fluid\_in} \tag{3-2}$$

- Gradient in device temperature:

$$\Delta T_{chip\_surface} = T_{chip\_\max} - T_{chip\_\min} \tag{3-3}$$

- Average chip temperature rise

$$\Delta T_{chip} = T_{chip} - T_{fluid\_in} \tag{3-4}$$

- Thermal resistivity ($K/(W/cm^2)$):

$$R = \frac{\Delta T_{chip}}{q''} \tag{3-5}$$

- Thermal Resistance (K/W):

$$R_{th} = \frac{R}{A_{chip}} \tag{3-6}$$

- Pumping Power (W):

$$P = \Delta p \times Q \tag{3-7}$$

3.1.3 Model Cuts

In analyzing the model, there are a variety of locations on the structure in which the above data points are taken. The cuts that are shown in Figure 3-7 include the chip top area, the chip center line, the outlet area, the inlet area and the center channel areas. The chip top area is the area over which the average, maximum and minimum chip temperatures are calculated. The chip center line is used to depict the temperature profile across the chips surface and to determine the locations of the maximum and minimum chip temperatures. For all models, the center line is the length of the chip and centered on the width of the model. The outlet and inlet areas are used to calculate the rise in fluid temperature along with the pressure drop of the system. Both the fluid temperatures and pressures are averaged across both the inlet and exit areas and then subtracted from each other to determine the rise in fluid temperature and the system pressure drops. The center channel areas are primarily used to calculate properties in each channel including the flow velocity, temperature and pressure.

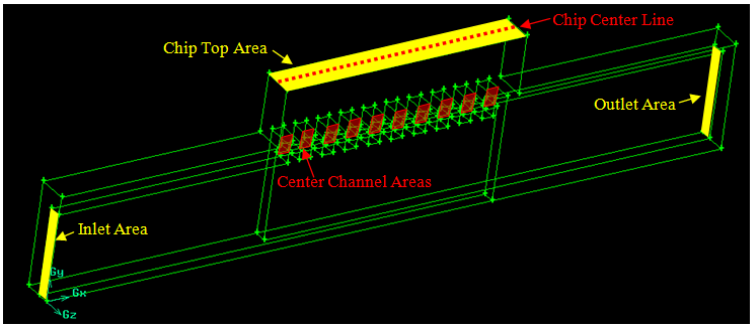


Figure 3-7: Depiction of some of the various locations on the structure at which data is obtained

Figure 3-8 shows the structure center cut which is primarily used to depict flow and temperature profiles through the center of the structure. The center cut is located on

the plane equidistant between the inlet and outlet manifolds. The figure also shows the Y-Z channel cut which is only shown for one of the microchannels but could be a cross section for any microchannel. The Y-Z cuts are used to show the flow and temperature profiles inside the structure.

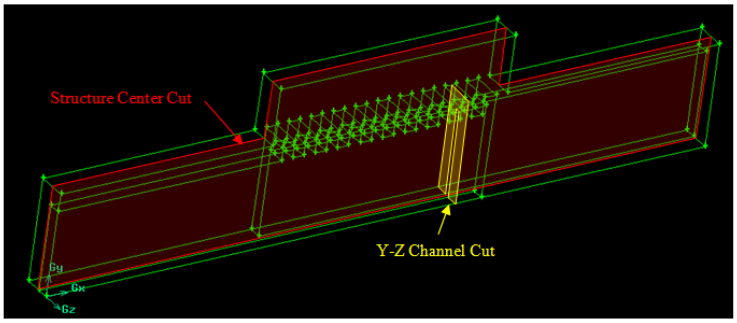


Figure 3-8: Depiction of the locations of the cuts on the structure used to show profiles

3.1.4 Volumetric Flow Rate versus System Volumetric Flow Rate

The three main parameters to consider when determining the inlet boundary condition are the system volumetric flow rate (Q_{system}), the volumetric flow rate (Q) and the inlet velocity (v_{in}). The inlet velocity is the parameter that is entered into Fluent but typically is not the parameter of interest, which is either the volumetric flow rate or the system volumetric flow rate. The volumetric flow rate is simply the volume of fluid entering a manifold channel per unit time (shown in mL/min). The inlet velocity is calculated from the volumetric flow rate through the following equation:

$$v_{in}\left(m/s\right) = \frac{Q}{M_h \times M_w} \tag{3-8}$$

A second flow condition that is interesting to look at in addition to the volumetric flow rate is the system volumetric flow rate, which is defined such that the volumetric

flow rate into the system is constant independent of the number of manifold channels. An example of this is shown in Figure 3-8; which shows that for the same size chip, the system on the right has twice the number of manifold channels as the left. Simply forcing the same volume of fluid through each of the manifold channels in the figure would give different results. Therefore, if the total volumetric flow rate was assumed to be constant for each of these chips at 30 mL/min, then the image on the left will have a volumetric flow rate per channel of 10 mL/min (30 mL/min / 3 inlet channels) and the image on the right will have a volumetric flow rate of 5 mL/min per channel (30 mL/min / 6 inlet channels). This allows the total volumetric flow rate to be constant by varying the flow rate into each manifold channel instead of leaving it constant.

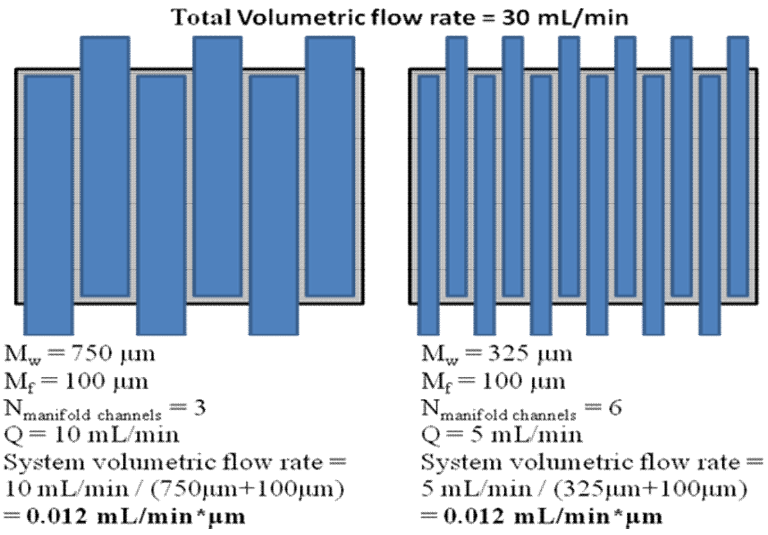


Figure 3-9: Depiction showing how to define the system volumetric flow rate, a flow rate parameter that is independent of the number of manifold channels for comparison in modeling

In order to define a volumetric flow rate independent of the number of manifold channels and the size of the chip, the volumetric flow rate is linearized. This is done by

taking the volumetric flow rate into each channel and dividing it by the sum of the manifold channel width and manifold fin width.

$$Q_{system}\left(mL/\min * \mu m\right) = \frac{Q}{M_f + M_w} \tag{3-9}$$

Continuing the example from the previous figure and setting the dimensions of the manifold width for the left image to be 750 μm and 325 μm for the figure on the right with 100 μm spacing for each system. Then using equation (3-9), the system volumetric flow rate in both cases is determined to be 0.012 mL/(min*μm).

This section has described the parameter of system volumetric flow rate, which has the units of mL/(min*μm), as compared to the standard volumetric flow rate, mL/min. The system volumetric flow rate is independent of the number of manifold channels, allowing the total flow rate into the system to be constant for a given chip size.

3.2 Pressure Drop Calculations

The pressure drop in the system is critical to determining the necessary pump size for a system. One of the focuses of the current research is to design a MMC structure that will minimize the system pressure drop. Two ways will be shown to calculate the pressure drop in a MMC system. The first way is termed a zeroth order calculation. It is simply the major losses which include the losses in both the manifold and the microchannels. The next calculation is termed a first order calculation and includes both the major losses from the zeroth order and also the minor losses from the system component, such as entrance effects and bends.

The pressure drop in the system should be the same independent of the path chosen; therefore, the pressure drop measurements are calculated along the path shown in Figure 3-18.

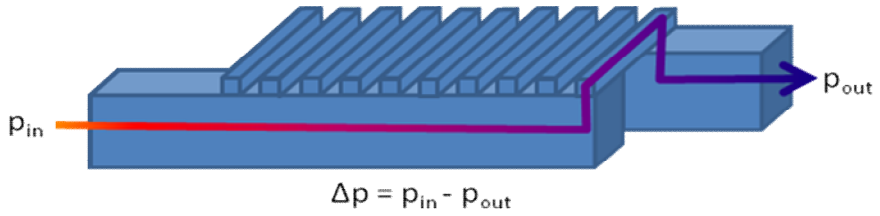


Figure 3-10: Schematic of the flow path used for the pressure drop calculations

3.2.1 Zeroth Order Pressure Drop Calculations

In order to estimate the pressure drop in a MMC system analytically, a method has been devised using the Hagen-Poiseuille equation which is shown in Equation (3-10) for rectangular cross sections [26]:

$$\Delta p = \frac{8\mu L \mathrm{v}(W+H)^2}{(WH)^2} = \frac{8\mu L Q(W+H)^2}{(WH)^3} = \frac{32\mu L \mathrm{v}}{D_h^2} \tag{3-10}$$

In the above equation, Q is the volumetric flow velocity, v is the linear flow velocity, μ is the liquid viscosity, L is the channel length, Δp is the pressure drop, W is the channel width and H is the channel height he channel. The width and height of the channels vary based on the channels being modeled. This equation makes it apparent that $\Delta p \propto 1/D_h^2$, indicating that the pressure drop increases exponentially as the hydraulic diameter decreases.

In order to use the equation to approximate the pressure drop in a manifold microchannel structure, the structure is broken down into two manifold portions and a microchannel portion as is shown in Figure 3-11.

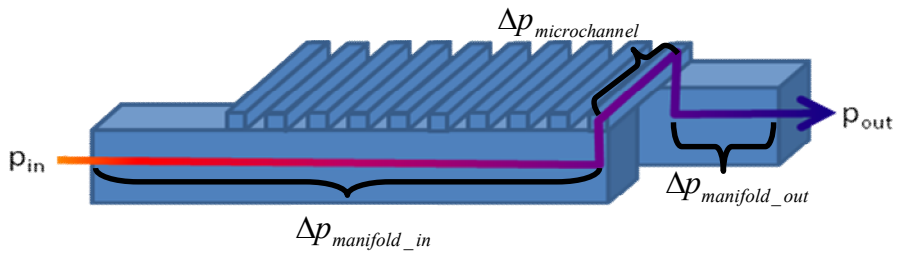


Figure 3-11: Schematic of the three pressure drops used to calculate the zeroth order pressure drop approximation

The total pressure drop is calculated by adding the three pressure drops:

$$\Delta p = \Delta p_{manifold\_in} + \Delta p_{microchannel} + \Delta p_{manifold\_out} \tag{3-11}$$

Just a single microchannel is used to calculate the pressure drop because of the assumption that the pressure drop in each microchannel will be similar. In the pressure drop equations, the length for the microchannels is assumed to be from the midpoint of the inlet manifold to the midpoint of the exit manifold; which equates to the sum of the manifold channel width and the manifold fin width:

$$L_{microchannel} = M_f + M_w \tag{3-12}$$

The average microchannel velocity is calculated based on a simple area calculation by taking the total volumetric flow rate into the manifold and dividing it by the total cross sectional area of the microchannels. It must also be divided by two because the flow from the manifold is split into the microchannels on each side. Therefore the microchannel velocity is:

$$v_{microchannel} = \frac{Q}{2\left(m_w \times m_h \times N_{ch}\right)} \tag{3-13}$$

Plugging Equations (3-12) and (3-13) into Equation (3-10) gives the value of the microchannel portion of the pressure drop as:

$$\Delta p_{microchannel} = \frac{8\mu Q\left(M_w + M_f\right)\left(m_w + m_h\right)^2}{2N_{ch}\left(m_w \times m_h\right)^3} \tag{3-14}$$

The flow rate into the manifold is set to the volumetric flow rate or inlet velocity of the structure. There is an inlet and an outlet portion of the pressure drop, which is the same equation except with different length terms, both of which are shown here:

$$\Delta p_{manifold\_in} = \frac{8\mu Q\left(L_{entrance} + L_{chip}\right)\left(M_w + M_h\right)^2}{\left(M_w \times M_h\right)^3} \tag{3-15}$$

$$\Delta p_{manifold\_out} = \frac{8\mu Q\left(L_{exit}\right)\left(M_w + M_h\right)^2}{\left(M_w \times M_h\right)^3} \tag{3-16}$$

In order to simplify the manifold portion of the pressure drop equation, a total manifold length term can be defined by adding the manifold entrance length, manifold exit length and the chip length as is shown in Equation (3-17). In all the models presented in this study, the inlet and outlet manifold length are assumed to be the same but this does not have to always be true.

$$L_{manifold} = L_{entrance} + L_{chip} + L_{exit} \tag{3-17}$$

The pressure drop in the manifold is simplified using the new manifold length term to the following equation:

$$\Delta p_{manifold} = \Delta p_{manifold\_in} + \Delta p_{manifold\_out} = \frac{8\mu Q L_{manifold}\left(M_w + M_h\right)^2}{\left(M_w \times M_h\right)^3} \tag{3-18}$$

The total pressure drop is then calculated by combining Equations (3-11), (3-14), and (3-18). A complete pressure drop equation for the MMC system for just the major losses is shown here:

$$\Delta p = 8\mu Q\left(\frac{L_{manifold}\left(M_w + M_h\right)^2}{\left(M_w \times M_h\right)^3} + \frac{\left(M_w + M_f\right)\left(m_w + m_h\right)^2}{2N_{ch}\left(m_w \times m_h\right)^3}\right) \tag{3-19}$$

Using this zeroth order approximation has led to pressure drops that underestimate the model results by about 50%. A comparison of all the models run in this thesis to the calculated results is shown in Figure 3-12. The models have been sorted by increasing pressure drops obtained by the numerical model.

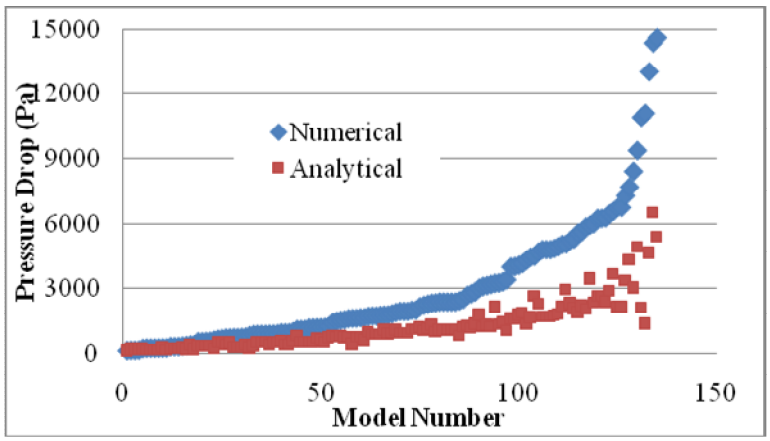


Figure 3-12: Plot comparing the analytical solutions for the zeroth order pressure drop equations to the numerical solutions for every model run sorted by increasing pressure drops

The zeroth order pressure drop approximation has been shown to give a reasonable approximation of the pressure drop in the system. It can be easily used for design and comparison purposes. But the zeroth order equation is missing all of the minor losses which will be accounted for in a first order approximation.

3.2.2 First Order Pressure Drop Calculation

The previous section discussed how to measure the pressure drop of just the channels but the equation is neglecting the effects of the minor channel losses. Therefore, in order to get a more accurate understanding of the pressure drops, these minor losses must be accounted for. The four types of minor losses that will be accounted for are: entrance losses, 90° bend losses, losses down the manifold, and expansion losses. The four losses are depicted in Figure 3-13 and each will be discussed independently.

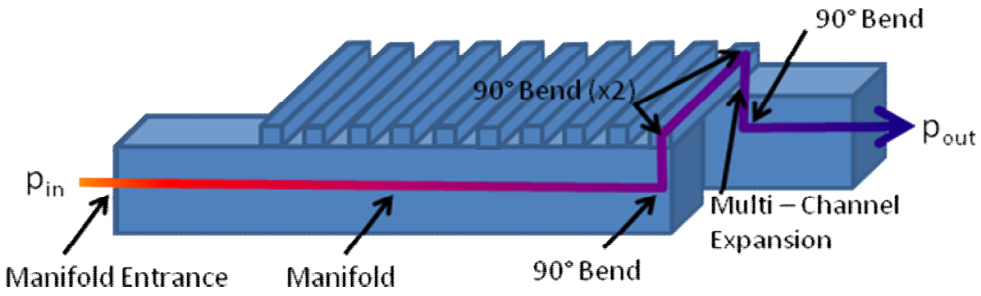


Figure 3-13: Schematic of the flow path used for pressure drop calculations along with the locations of all the included minor losses

The minor pressure losses are calculated from the Darcy-Weisbach equation:

$$\Delta p = K \times \frac{\rho \, v^2}{2} \tag{3-20}$$

This equation is based on only three things: fluid viscosity (ρ_{water} = 1000 Pa*s), channel velocity (v), and the minor loss coefficient (K). The pressure d rop is proportional to v^2 which means that it is heavily dependent on the velocity. The K factor is a measure of the pressure loss and depends on the geometry and sometimes also the fluid properties.

3.2.2.1 Entrance Losses [27]

When the fluid enters the manifold it is not fully developed; therefore, there are some pressure losses at the entrance of the manifold. Miller and Han looked at the effect of the entrance region of a rectangular shaped channel and came up with the plot shown in Figure 3-14 to determine the loss factor K. [27] The x-axis is a measurement of how developed the flow is. It is a ratio of the full length divided by the hydraulic diameter multiplied by the Reynolds number. The curves differ depending on γ, the ratio of channel height to width, or vice versa, depending on which is less than 1.

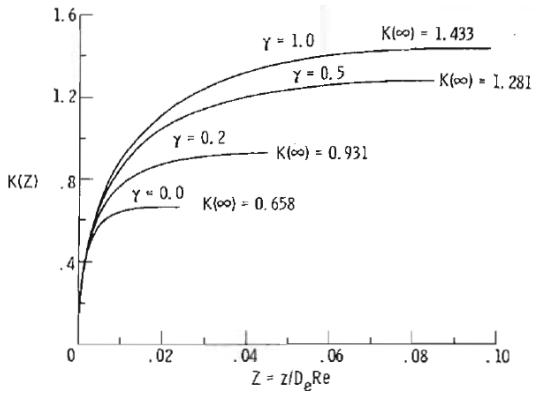


Figure 3-14: Plot of the effect of the K factor as a function of the distance into the developing flow regime for various ratios. From [27].

For each geometry, a K is determined from the above graph and inserted into the Darcy-Weisbach pressure drop equation to determine the effect on the pressure drop of the manifold entrance effect. The velocity is assumed to be the velocity entering the manifold. Therefore, the total pressure drop contribution from the manifold inlet is:

$$\Delta p_{man\_inlet} = K_{man\_inlet} \times \frac{\rho v_{in}^{2}}{2} \tag{3-21}$$

3.2.2.2 Manifold [28]

The K factor for the pressure drop through the manifold section is shown in Equation (3-22) and depends on the number of microchannels, the chip length, the Darcy-Weisbach friction factor, and the hydraulic diameter.

$$K_{manifold\_sys} = \left(\frac{1}{3} - \frac{1}{6N_{ch}}\right) f \frac{L_{chip}}{D_h} \tag{3-22}$$

The hydraulic diameter and friction factors are calculated from the equations in Sections B.2.2 and B.2.3, respectively. The velocity is assumed to be the velocity which enters the manifold. Therefore, the total pressure drop contribution from the manifold is:

$$\Delta p_{manifold\_sys} = K_{manifold} \times \frac{\rho \mathrm{v}_{in}^{\ 2}}{2} \tag{3-23}$$

3.2.2.3 90° Bends

Due to the geometry of the MMC design, there are multiple 90° bends. For this analysis, there are assumed to be four 90° bends: one entering the microchannels from the manifold, one exiting the microchannels from the manifold, and two in the microchannel geometry. In reality, this is not quite the case, but it is a fair approximation. For 90° bends with a sharp radius, the minor loss coefficient, K approaches 1.1. [29] Therefore, the additional pressure drop is simply:

$$\Delta p = 1.1 \times \frac{\rho \mathrm{v}^2}{2} \tag{3-24}$$

The velocity for each of the 90° bends differs. The velocity of the bend going from the manifold into the microchannel is assumed to be 1/nth of the inlet volumetric flow rate normalized over the cross sectional area of the manifold. Therefore, the total pressure drop contribution from the bend going from the manifold to the microchannel is:

$$\Delta p_{bend\_into\_manifold} = 1.1 \times \frac{\rho}{2}\left(\frac{v_{microchannel} \times m_h \times m_w}{M_h \times 0.5 M_w}\right)^2 \quad (3\text{-}25)$$

The velocity for the bends in the microchannel is assumed to be the velocity through the microchannel, which is assumed to be constant and calculated from Equation (3-13). The same velocity is assumed for the bend exiting the microchannels into the manifold. Therefore, the pressure drop contribution for each microchannel bend and the bend from the microchannels to manifold is:

$$\Delta p_{microchannel\_bends} = 1.1 \times \frac{\rho v_{microchannel}^2}{2} \quad (3\text{-}26)$$

3.2.2.4 Multi-Channel Expansion [30]

The final K factor that will be considered is the expansion from a multi-channel core which is shown in Figure 3-15.

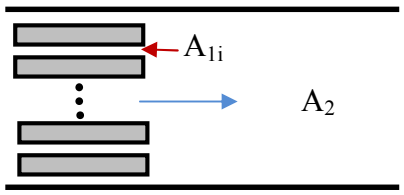


Figure 3-15: Depiction of the geometry used to calculate the K factor for a multi-channel expansion. Adapted from [30].

The K factor for this pressure drop portion for expanding from a multichannel core is given by Equation (3-27) and involves the ratio of two areas. The first area is the cross section of the inlet manifold which has been assumed to be the chip length multiplied by the manifold width. The other area is the total cross sectional area of the

inlet portion of the microchannels which is the product of the manifold width, microchannel width, and the number of microchannels.

$$K_{\exp ansion} = \left(1 - \frac{A_1}{A_2}\right)^2 = \left(1 - \frac{N_{ch} \times m_w \times M_w}{L_{chip} \times M_w}\right)^2 \tag{3-27}$$

The velocity for the multichannel expansion is assumed to be the microchannel velocity; therefore, the pressure drop contribution from the multichannel expansion is:

$$\Delta p_{\exp ansion} = K_{\exp ansion} \times \frac{\rho \, \mathrm{v}_{microchannel}^{\,2}}{2} \tag{3-28}$$

3.2.3 First Order Pressure Drop Summary

The first order pressure drop is calculated by summing the zeroth order pressure drops and the minor losses: Equations (3-14), (3-18), (3-21), (3-23), (3-25), (3-26), and (3-28). The total pressure drop is given as:

$$\begin{aligned}\Delta p = {} & \Delta p_{manifold} + \Delta p_{microchannel} + \Delta p_{man\_inlet} + \Delta p_{manifold\_sys} + \Delta p_{bend\_int o\_manifold} \\ & + 3\Delta p_{microchannel\_bends} + \Delta p_{\exp ansion}\end{aligned} \tag{3-29}$$

A plot of the numerical versus analytical pressure drops is shown in Figure 3-16 for both the zeroth and the first order approximations. The average error is now around 35%, a 15% improvement over the zeroth order.

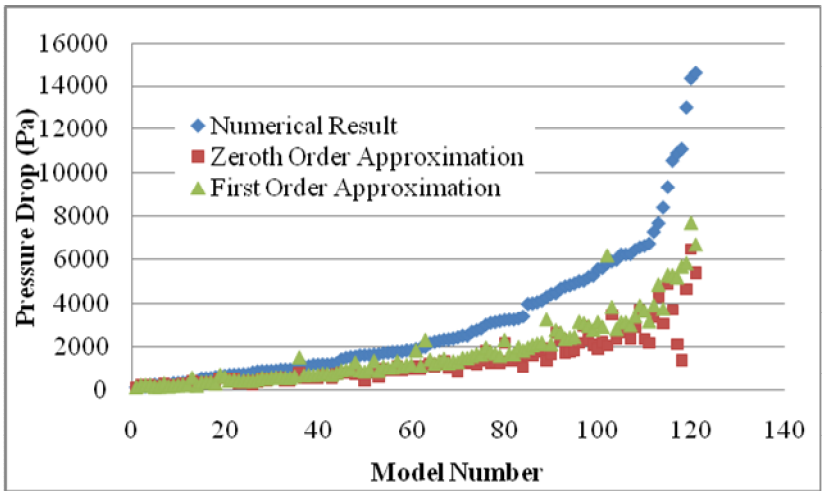


Figure 3-16: Plot comparing the analytical solutions for the zeroth and first order pressure drop equations to the numerical solutions for every model run sorted by increasing pressure drops

A plot of the percent error is shown in Figure 3-17 with sections called out to indicate the various types of models run. Most of the models are around 35-40% error but there are a few outliers. The majority of the outliers on the figure occur in geometries with an increased manifold width, which causes an over approximation in the microchannel length. As will be shown later, a stagnation region forms in the microchannel above the center of the manifold channel which increases in size as the manifold width increases. Therefore, when the manifold width is large, this over approximation dominates causing the calculated pressure drop to be over calculated. When the M_w is small, this is a reasonable approximation because the stagnation region is also small and the fluid flows through the majority of the microchannel. Additionally, there is a vertical pressure drop that is not accounted for when the fluid goes from the manifold into the microchannels. Therefore, when the manifold height is large, the pressure drop is under approximated. Furthermore, increasing velocities causes the flow maldistribution through each channel to increase, which in turn causes the actual velocity

in the channels closest to the exit to have a higher velocity than the channels closer to the inlet. Since the equations are based on equal velocities through each channel determined by the velocity of the channel closest to the exit, this causes the equations to underestimate the pressure drop and the error is increased. Additionally, increasing velocity causes flow eddies which are not accounted for in the pressure drop equations and cause increased error.

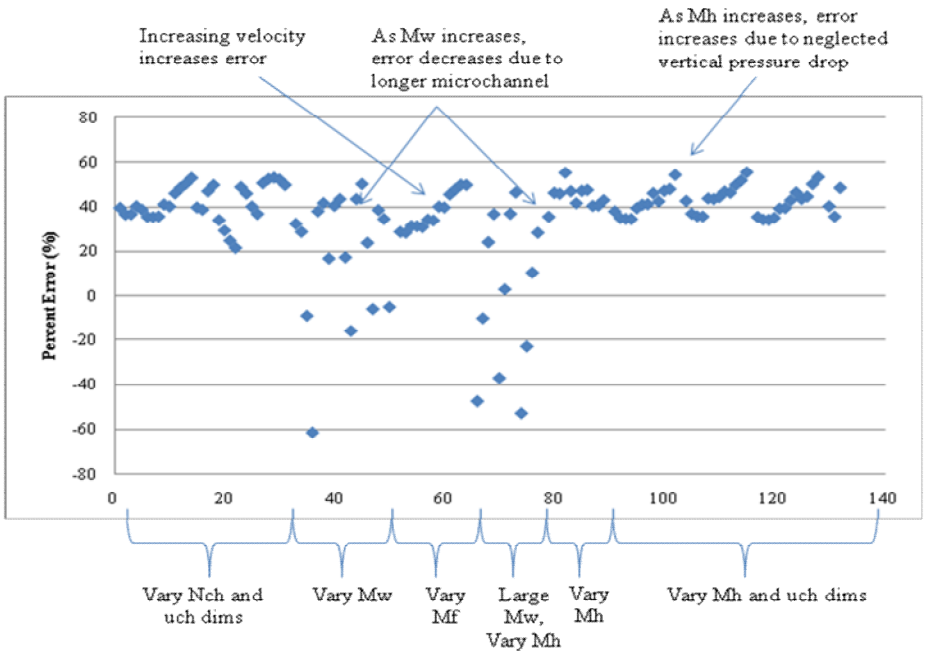


Figure 3-17: Percent error plot for the first order pressure drop approximation

3.3 Mesh Convergence

In order to show that the mesh that was created is satisfactory, the mesh must be proven to have converged and be independent. A full analysis of the mesh convergence is shown in Appendix D but a summary is presented here. In order to mesh the structure, it was broken down into five meshing regions with the microchannels being the most

critical region with the finest meshing. Local mesh refinement was performed in each of these five regions for two different microchannel sizes (m_w = m_f = 100 μm and $m_w = m_f = 50$ μm). It was proven that a Gambit mesh density of 0.0125 in the microchannel region was sufficient to show mesh independence for both of these dimensions. Therefore, it is also going to be assumed that this is a sufficient mesh density for the other two microchannel dimensions that will be modeled: m_w = 100 μm, $m_f = 50$ μm and $m_w = 50$ μm, $m_f = 100$ μm.

The mesh analysis in Appendix D also showed that laminar is a reasonable assumption because the Reynolds numbers for most modeled channels are well within the laminar region and also because running the model with both a laminar and a turbulent boundary conditions produced similar results. The Reynolds numbers in the microchannels had an average of 55, which is well within the laminar region. Some manifold Reynolds numbers are in the transition region at the higher flow rates, but most are well in the laminar region. Both the average rise in device temperature and the overall system pressure drop were used to test the convergence of the models. It was shown that $1 \text{ X } 10^{-4}$ is a sufficient criterion to obtain convergent results. All of the modeling was performed for simulated devices having only a few channels, but it is going to be assumed that simply changing the number of channels and leaving the mesh the same for each channel, will still give converged independent solutions.

With the mesh now defined and proven to be both independent and converged, focus can be placed on determining results for a single geometry, the thermal and fluidic results for which are discussed in the next section.

3.4 Modeling Case Study for a Single Geometry

The intention of this section is to show a basic result of the models by showing a thorough analysis of a single geometry. The model will be looked at in terms of its pressure drop, average rise in chip temperature, velocity profiles, etc.

The geometry that is being looked at has the following dimensions: M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, and N_{ch} = 10. Both the inlet and outlet manifolds have a 2 mm length before entering the microchannel region. The fluid portion of the model showing the dimensions is depicted in Figure 3-18. The model was run with a constant heat flux of 400 W/cm^2.

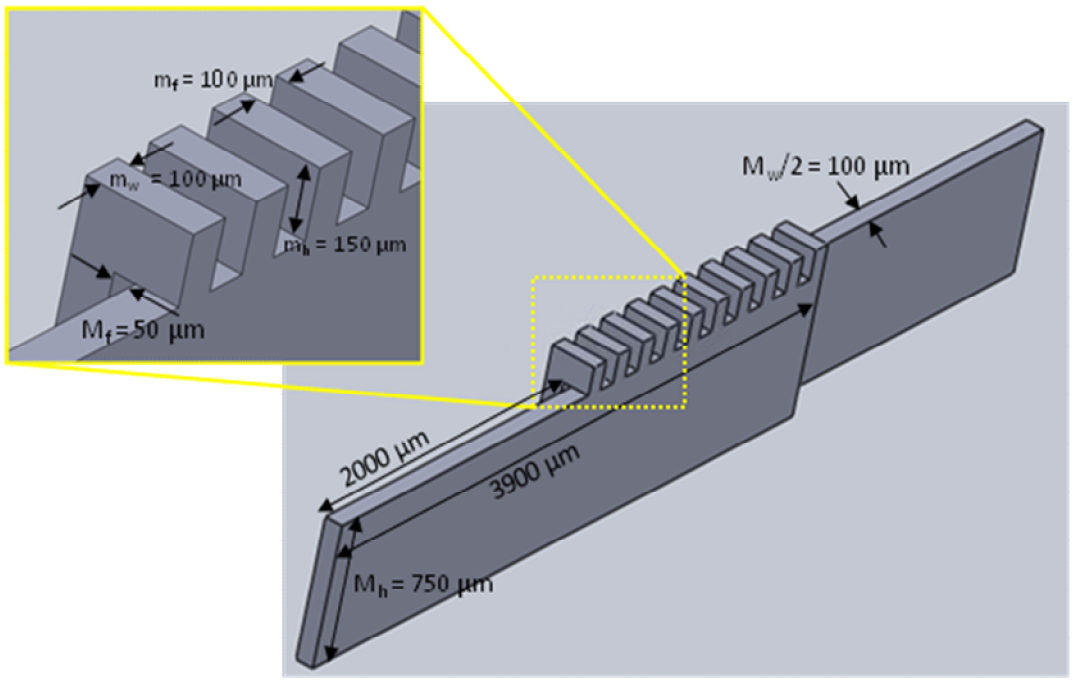


Figure 3-18: Fluid geometry for a manifold microchannel structure with M_h = 750 µm, M_f = 50 µm, M_w = 200 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q"=400 W/cm^2

3.4.1 Pressure Drop versus Thermal Performance and 1% Rule

For each geometry, a plot of pressure drop versus flow rate can be determined for various inlet flow rates. This model was run for various volumetric flow rates into each manifold (Q = 0.9 mL/min, 1.125 mL/min, 1.8 mL/min, 2.7 mL/min, 4.5 mL/min, 4.875 mL/min, 5.625 mL/min, 9 mL/min and 11.25 mL/min) which equates to an inlet velocity condition as was calculated by Equation (3-8) above. The model was run for each of these conditions and a plot was made showing the average device temperature and the system pressure drop versus the volumetric flow rate, as is shown in Figure 3-19.

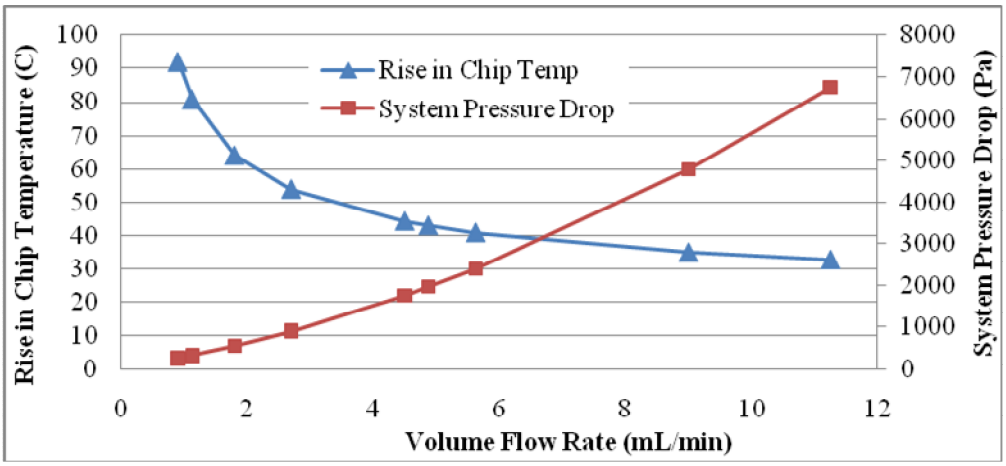


Figure 3-19: Tradeoff between pressure drop and thermal performance for a system with M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2

This chart indicates the pressure drop versus thermal performance tradeoff, a trend which is found for almost all heat sinks. In terms of thermal performance, decreasing the flow rate causes the average chip temperature to exponentially increase. Conversely, increasing the flow rates equate to better thermal performance. But too high

of a flow rate produces a marginal thermal performance improvement while having a significant increase in pressure drop. Therefore, each geometry has a flow condition that is most beneficial for operation.

A reasonable rule of thumb for addressing this tradeoff is to define the preferred range of operation at the point which the temperature changes less than 1% for a 0.1 mL/min change in volumetric flow rate. This allows the temperature to be relatively stable with pressure drop such that small changes in flow rate will not have a large impact on the chip temperature. In this case, that occurs at 4.2 mL/min. But this 1% convention is not a rule set in stone. These values are heavily dependent on the system needs. For example, if it is required to have a pressure drop less than 1000 Pa, then the flow rate would have to decrease to a maximum of just around 3 mL/min and the average chip temperature would have to increase. The chip temperature rise will be about 52 °C if it is necessary to keep the pressure drop less than 1000 Pa in this case. This is shown with the black dashed lines in Figure 3-20. But the same would work if there is a maximum allowable chip temperature rise. Say for example, the chip was only allowed to rise 36 °C, then the flow rate would have to be at least 8.6 mL/min and the pressure drop will now be over 4500 Pa. This case is shown with the green dotted lines in Figure 3-20. If it is required to have pressure drops less than 1000 Pa and a chip temperature rise less than 36 °C, then it would not be possible with this geometry and this heat flux. Either a different geometry would have to be used or the heat flux must be reduced to lower the chip temperature.

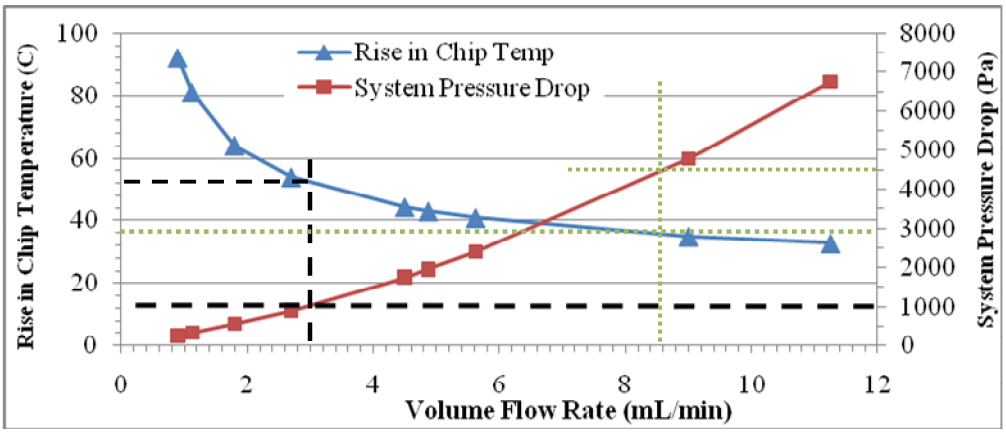


Figure 3-20: Tradeoff between pressure drop and thermal performance for a system with $M_w = 200$ µm, $M_f = 50$ µm, $M_h = 750$ µm, $m_w = 100$ µm, $m_f = 100$ µm, $m_h = 150$ µm, $N_{ch} = 10$, q" = 400 W/cm^2

It is important to emphasize that all of these numbers are for this specific geometry; a different geometry will lead to different charts as will be discussed in the next chapter. But all the charts will have a similar trend. The 1% rule should be used if there is not a requirement for either the pressure drop or the thermal performance and the interest is to reduce both parameters.

3.4.2 Thermal Profiles at Various Flow Rates

Four inlet flow conditions will be analyzed further including 0.9 mL/min, 2.7 mL/min, 5.625 mL/min and 11.25 mL/min. The overall temperature distributions for both the inlet and outlet sides of the device are shown in Figure 3-21. As expected, as the flow rate increases, the chip temperature decreases. At the higher flow rates, there is very little heating of the fluid before it enters the microchannels and there is very little heat transfer outside of the device and into the manifold sections. In contrast, for the low flow rates, there is quite a bit of heat transfer into the manifold and the fluid is heated up quite

a bit before it enters the microchannels. The fluid is also heated up quite a bit more while in the microchannels for the lower flow rates than the higher flow rates.

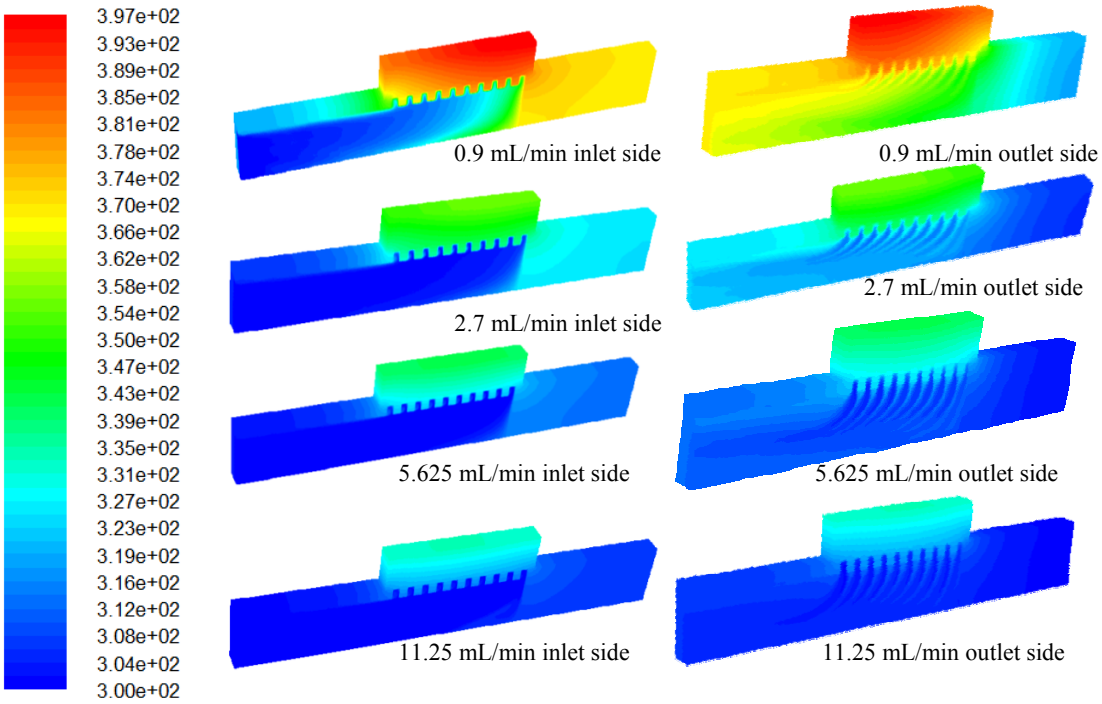


Figure 3-21: Temperature contours for various inlet flow rates from both the inlet and outlet perspective for a MMC with parameters $M_w = 200$ µm, $M_f = 50$ µm, $M_h = 750$ µm, $m_w = 100$ µm, $m_f = 100$ µm, $m_h = 150$ µm, $N_{ch} = 10$, q" = 400 W/cm^2

The temperature profiles of a cut line through the middle of the geometry are shown in Figure 3-22 for various inlet velocities. The only fluid portion of this cut is through the center of the microchannels. Magnified images of the heat transfer to the microchannels are shown for each of the four conditions. The most important thing to notice in this figure is that as the fluid flow rate is increased, less of the fluid is being heated. This is why the thermal performance levels off as the flow rate is increased, because the fluid is flowing so fast that the channel walls no longer effectively transfer

heat to the fluid. The thermal performance also levels off, to a lesser degree, from the fact that there is less heat being transferred to the fluid from the manifold.

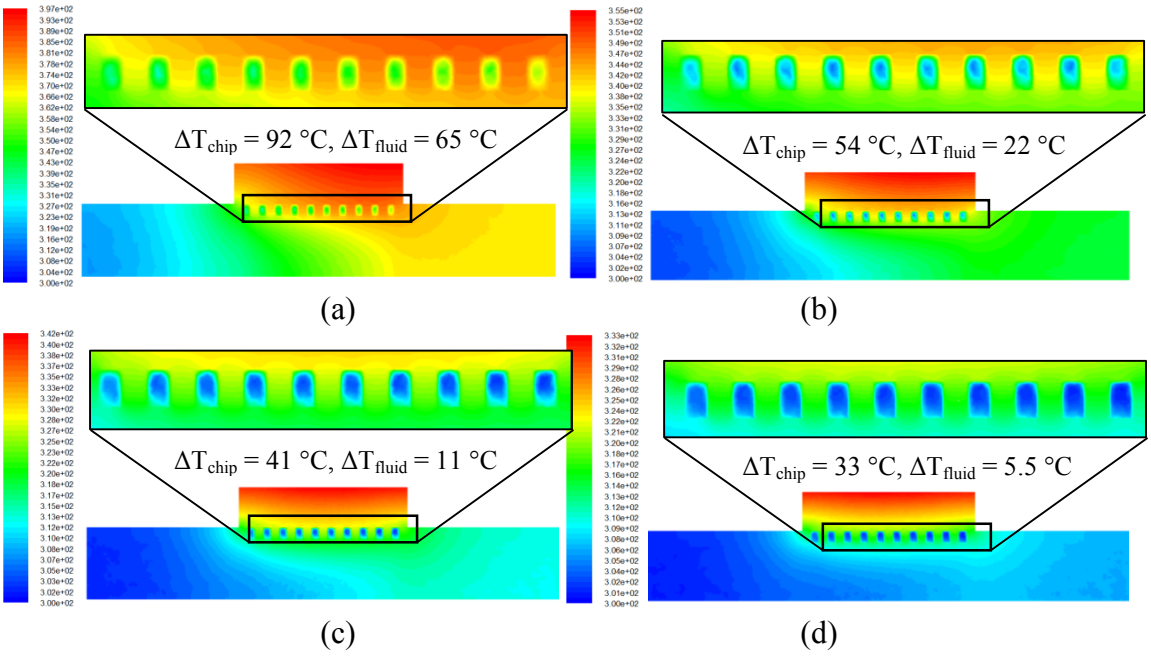


Figure 3-22: Center cut through the model showing the thermal contours for various flow rates (a) 0.9 mL/min (b) 2.7 mL/min (c) 5.625 mL/min and (d) 11.25 mL/min (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

Figure 3-23 shows the center two fluidic microchannels for each flow rate from the previous figure scaled to the same temperature scale. Arrows indicate the corresponding data point on the temperature versus flow rate curve. This shows how the heat is transferred to the fluid for various velocities and gives an idea of why the temperature curve looks the way it does. For the slowest velocity, 0.9 mL/min, the entire bulk of the fluid has been heated and therefore is on the part of the curve where the chip temperature rises exponentially. The fluid has been saturated with the heat and further heat transfer is difficult thus raising the temperature of the chip. For the fastest velocity,

11.25 mL/min, the fluid passes through the channel, while picking up very little heat, which is why this condition lies on the saturated portion of the temperature curve. The two middle velocities are in a preferred operating region where heat is being transferred to the fluid, as the fluid is neither heat saturated nor flowing too rapidly such that the majoring of the fluid is not absorbing heat.

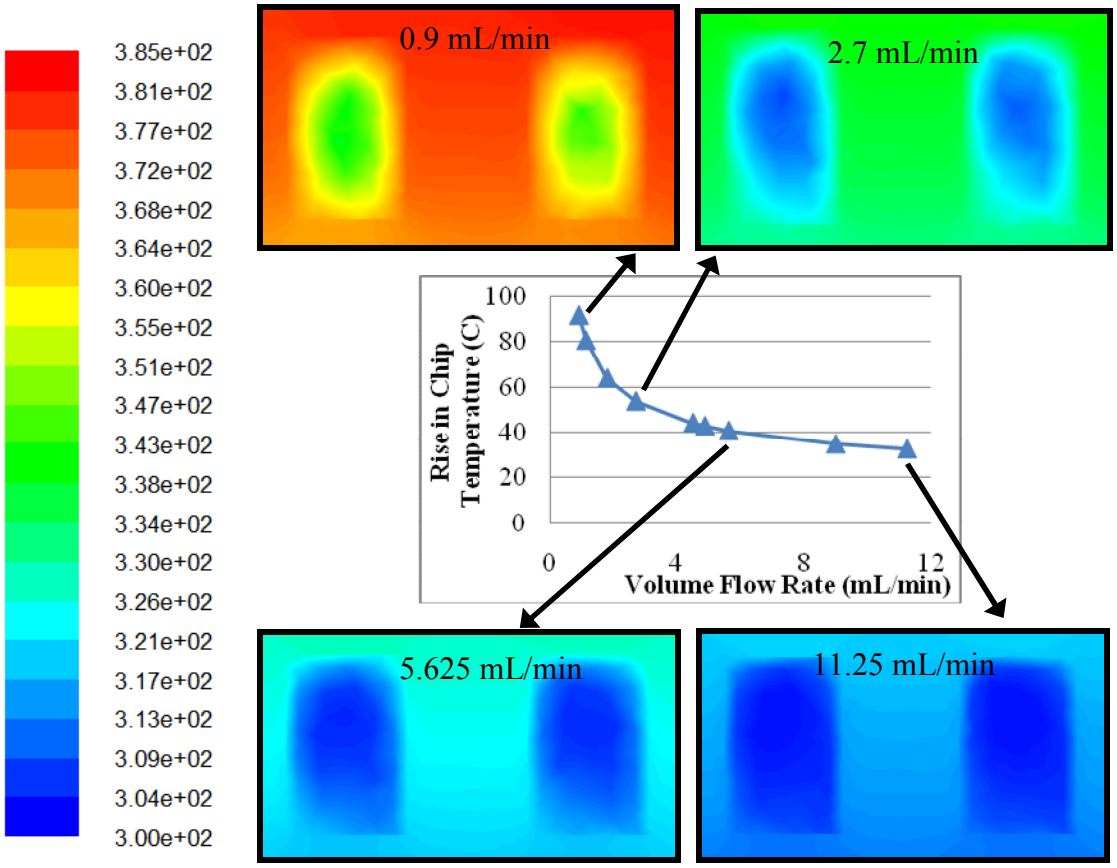


Figure 3-23: Expanded image of the center channels for various flow rates showing the heat transfer into the fluid and how it relates to the rise in chip temperature (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

Figure 3-24 shows the thermal contours of the Y-X cuts of channels 2, 4, 6, 8 and 10. All of the channels were not shown for simplification and the channels that are shown

give a good representation of the thermal effect. These cuts show the fluid coming in through the manifold, crossing over through the microchannels then exiting out through the exit manifold. The fluid in the manifold portion of the second channel has not absorbed much heat but by the last channel, the fluid in the manifold has absorbed quite a bit of heat. It is also shown in the image how the fluid is heated as it flows through the microchannel.

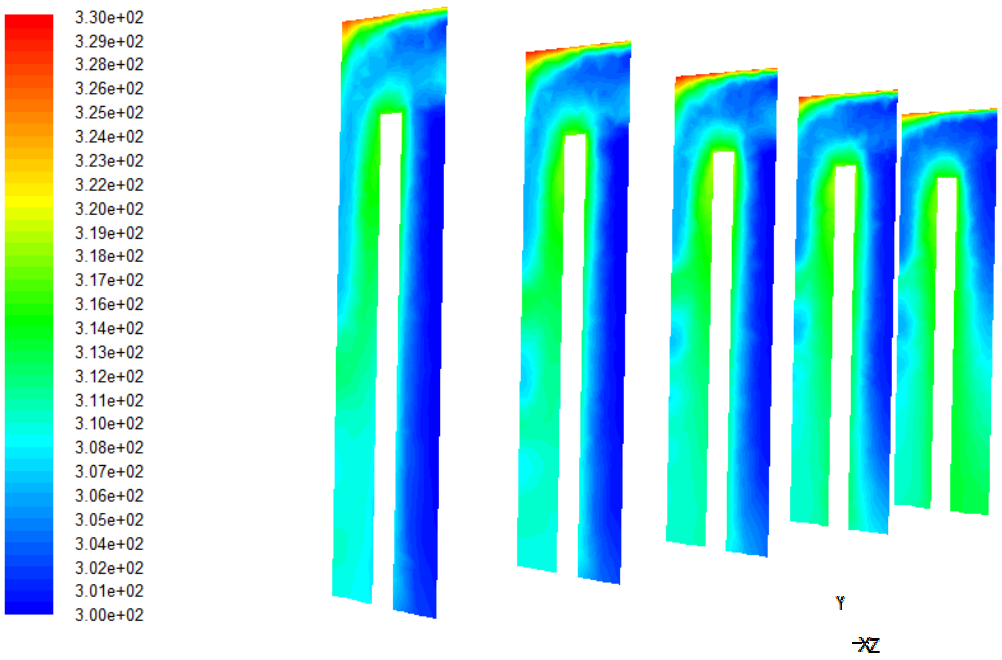


Figure 3-24: Thermal contour plots for cuts through the center of channels 2,4, 6, 8 and 10 including the manifold portions (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2, Q = 5.625 mL/min)

A plot of the temperature profiles of a line across the center of the top of the chip for various inlet flow rates is shown in Figure 3-25. One interesting fact to notice when looking at Figure 3-25 is that the location of maximum chip temperature (denoted by a black asterisk) varies as the flow rate in increased. For the slower flow rates, the

maximum temperature occurs closer to the exit, whereas, as the velocity increases, the location of maximum temperature trends towards the center. In addition, the solid black line in Figure 3-25 shows the surface temperature gradient, the difference between the maximum and the minimum temperatures. Clearly the gradient increases substantially for the slower volumetric flow rates.

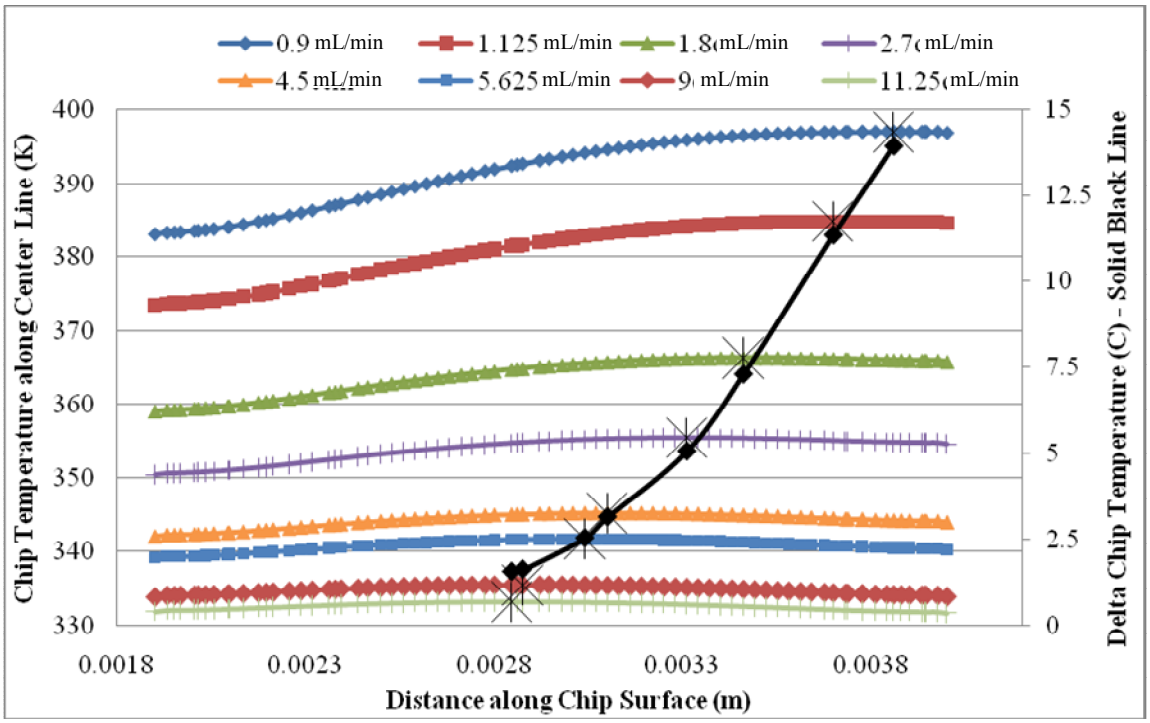


Figure 3-25: Chart showing the variation of chip temperatures along the centerline of the chip surface for various inlet flow rates. The large stars indicate the location of maximum chip temperature and the solid black line indicates the variation in chip temperature along the line. (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

3.4.3 Effect of Inlet Velocity on Chip Surface Temperature

Four of the flow rates have been expanded upon: 0.9 mL/min, 2.7 mL/min, 5.625 mL/min and 11.25 mL/min. For each of these flow rates, the chip surface temperature profiles along with their centerline temperatures are shown in Figure 3-26. The images clearly show how the locations of the hottest temperature are moving from closer to the exit to closer to the center of the chip.

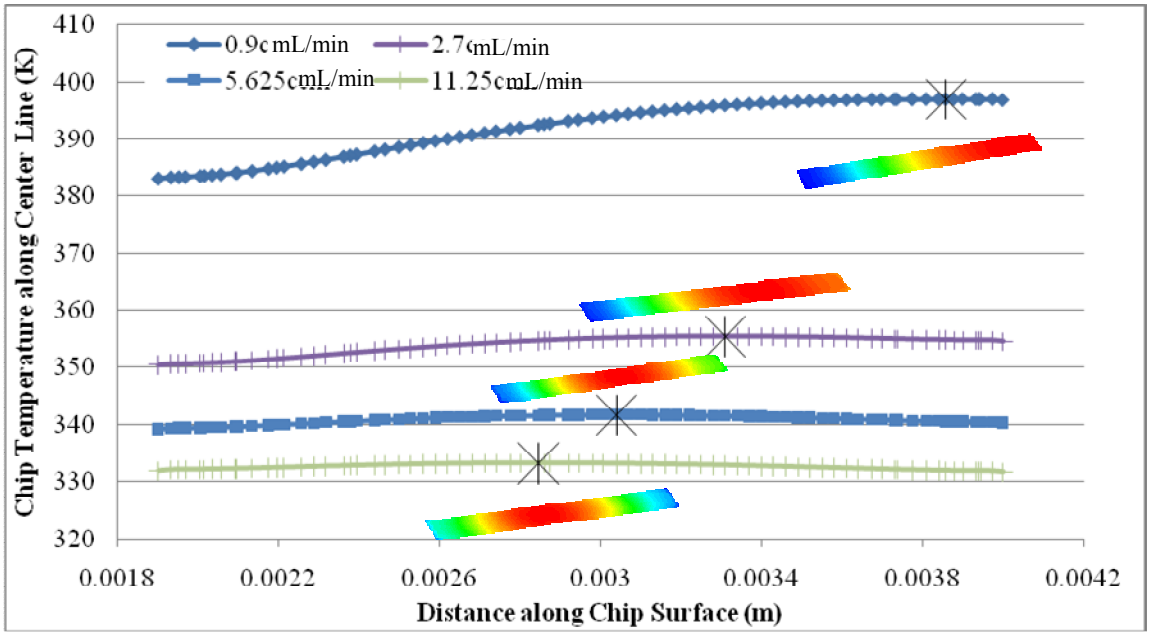


Figure 3-26: Chart showing the variation of chip temperatures along the centerline of the chip for four various flow rates along with a surface temperature contour plot showing how the hottest part of the chip shifts more centralized as the flow rate increases. (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

Figure 3-27 gives us a clue as to why the temperature shift occurs. This figure shows the average channel velocity for a cross section of each of the ten channels. As the flow rate increases, so does the variation in the channel velocity.

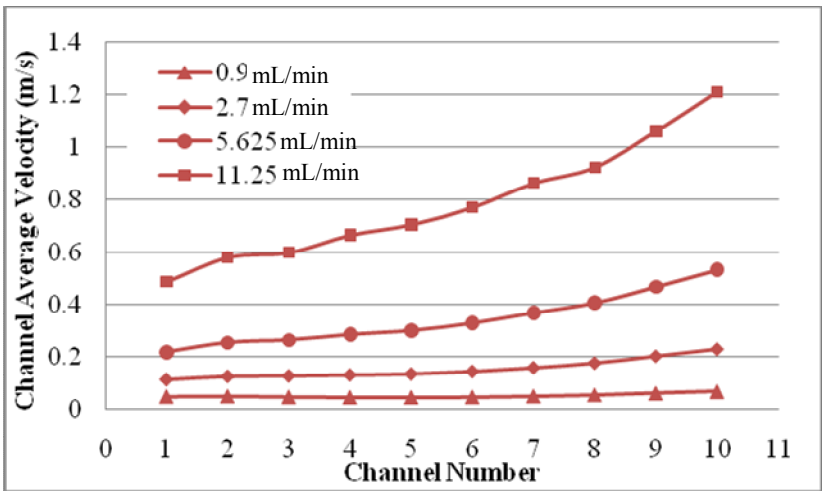


Figure 3-27: Average flow velocities through each channel for various flow rates (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

The velocities through each channel are very uniform for the lower flow rates and progressively become non-uniform for the increased flow rates. Comparing this trend to the non-uniformity of the chip temperature from Figure 3-26, the devices with the centralized hot spot had the most non-uniform channel velocity profiles. This leads to the conclusion that the higher velocities at the exit are reducing the effect of the heating of the fluid down the structure and allowing the hottest part of the chip to be in the center; whereas, for the channels that have a more uniform velocity profile, the heating up along the length of the structure causes the hot spot to occur closer to the exit.

3.4.4 Velocity Profiles

An interesting thing to look at is the velocity flow per microchannel, which as was shown in Figure 3-27, increases along the length of the device. A plot of the velocity magnitude profiles are shown in Figure 3-28 for various flow rates. Clearly, the smaller flow rates have a much smaller velocity gradient across the channels. This velocity

gradient occurs because as the fluid flows through the manifold, when it gets to the end, it essentially hits a flat wall and is forced into the channels closest to the exit. The faster the inlet velocity, the more pronounced effect this has because the fluid strikes the wall at the end of the manifold channel with a stronger velocity.

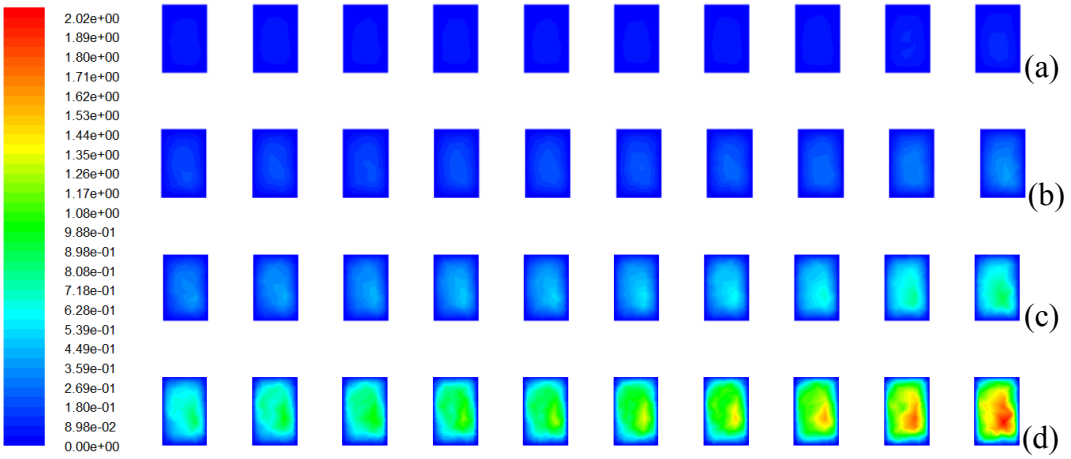


Figure 3-28: Velocity magnitude contours through the center cut of the microchannels for (a) 0.9 mL/min (b) 2.7 mL/min (c) 5.625 mL/min (d) 9 mL/min (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

Although the contours from figures Figure 3-27 and Figure 3-28 make it appear that the for the lower velocities, the flow rates in all the channels are the same, there is in fact a slight increase, as can be seen in Figure 3-29 for the 0.9 mL/min flow rate. In this case, the flow velocities are still the quickest at the channels closest to the end, but the magnitude between the smallest and largest channel velocities is quite a bit smaller than for the larger inlet flow rates. For smaller flow rates, there is sometimes an increase in the velocity in the first couple channels as can be seen in Figure 3-29. This is due to the fact that since the flow does not have as much of a forward momentum, it has more of a

chance to flow into the channels. The velocity profiles shown here are similar to the profiles seen for other geometries.

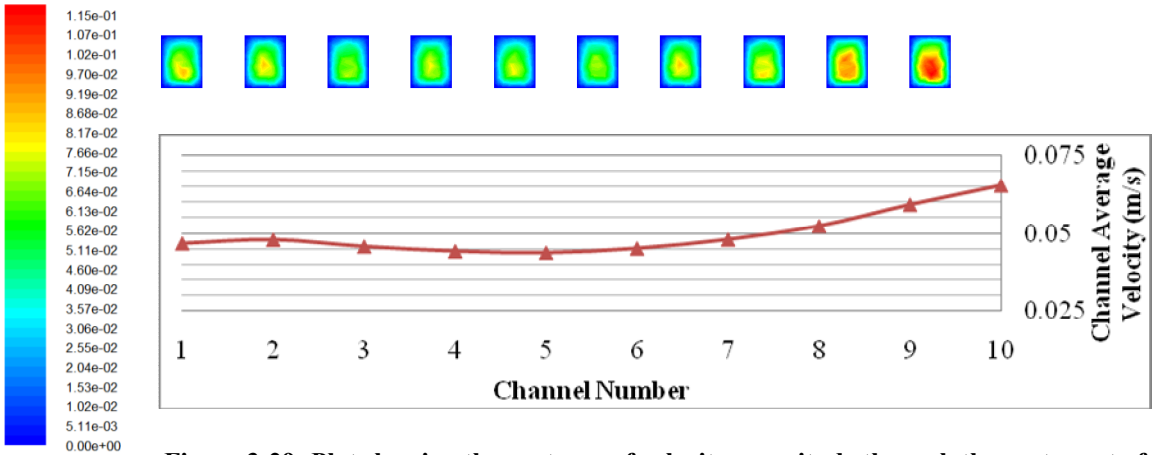


Figure 3-29: Plot showing the contours of velocity magnitude through the center cut of the microchannels and also a graph showing the average velocities for each of these channels (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2, Q = 0.9 mL/min)

The velocity vectors for a volume flow rate of 5.625 mL/min are shown in Figure 3-30. An interesting thing to note is the stagnation regions directly above the center of each manifold channel and at the base of the manifold channel. The location of maximum velocity is at the fluid exiting the microchannels closest to the exit. There are also areas of fast velocity in the inlet portion of the manifold channel immediately before the fluid starts to enter the microchannels and also in the exit manifold toward the base.

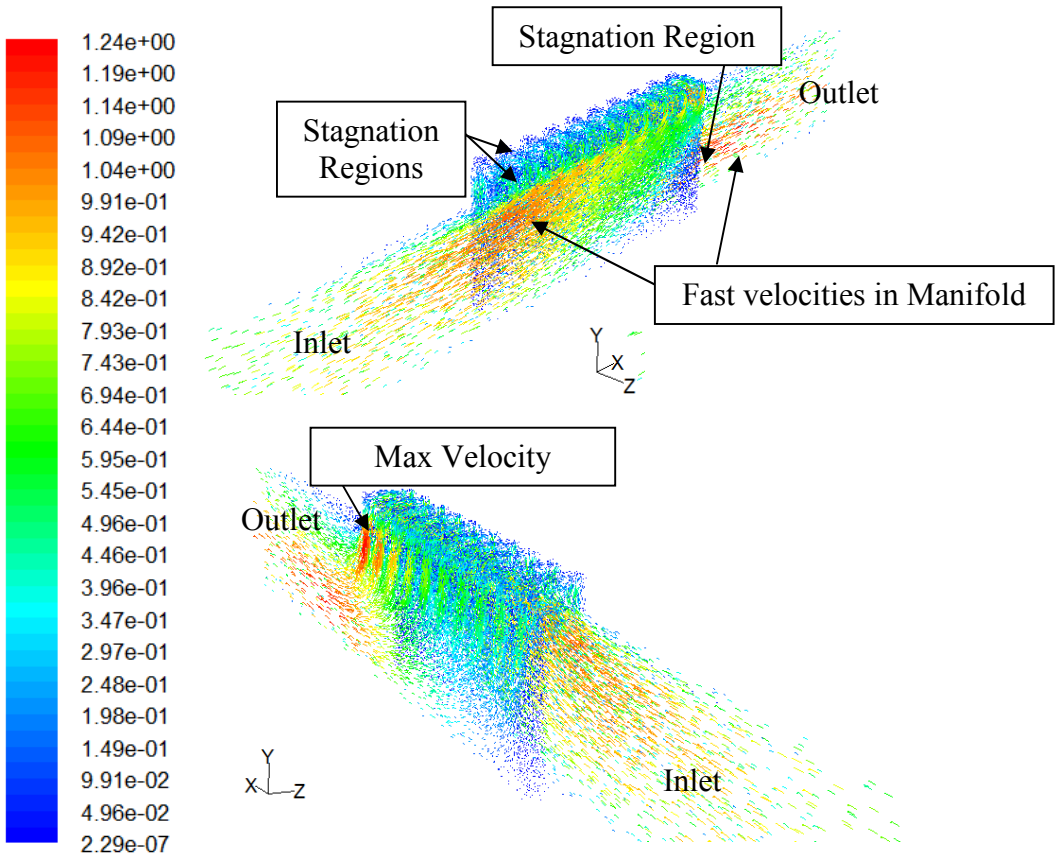


Figure 3-30: Depiction of the velocity vectors from both the perspective of the inlet manifold and the exit manifold channels (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2, Q = 5.625 mL/min)

Figure 3-31 shows a zoomed-in image of the velocity vectors of the microchannels including an even more focused image of the two microchannels at the end. In each of the microchannels, although it is most pronounced for the microchannels at the exit, the flow makes a loop path through the microchannel. The flow goes up and slightly towards the exit as it enters the channel. Then as it reaches the top it flows slightly backward and then down and out of the channel.

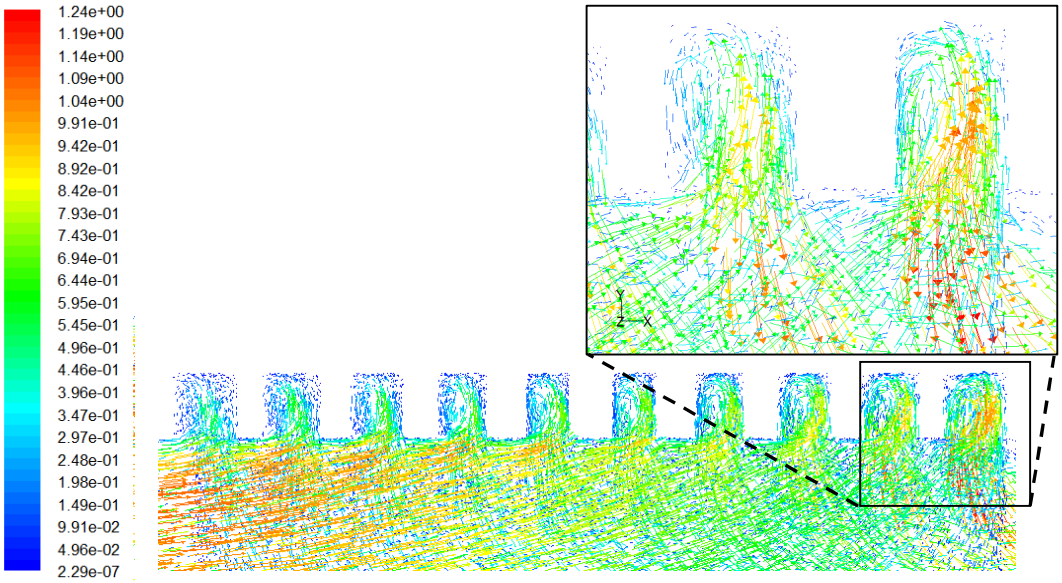


Figure 3-31: Velocity vectors of the fluid from the perspective of perpendicular to the inlet manifold channel with a magnified image of the last two microchannels where the largest velocity vectors occur showing the swirling action of the fluid in the microchannels (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2, Q = 5.625 mL/min)

Figure 3-32 shows the overall velocity contours for four different flow rates. The most notable thing in this figure is the development of the swirl pattern as the flow rate increases. For the slow velocities, 0.9 mL/min in Figure 3-32a, there is very little swirling flow and the fluid just flows into the microchannels and back out. By 9 mL/min, Figure 3-32d, a clear swirling flow pattern has developed whereas the fluid flows up into the channels towards the exit and swirls in the channel towards the entrance before exiting into the exit manifold channel. This swirl pattern was shown in vector form in the previous figure for a volumetric flow rate of 5.625 mL/min, shown in Figure 3-32c.

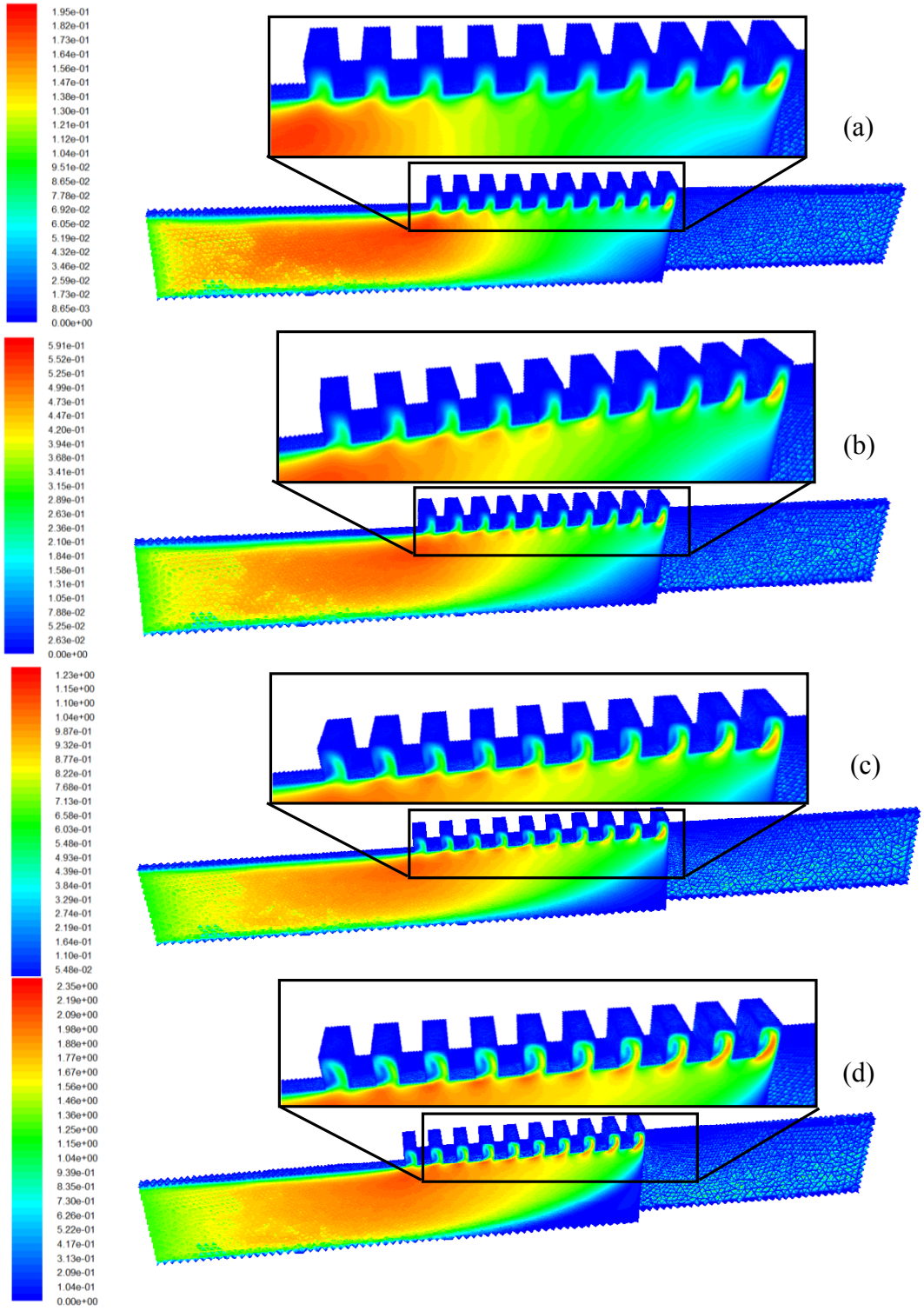


Figure 3-32: Velocity magnitude contours for (a) 0.9 mL/min (b) 2.7 mL/min (c) 5.625 mL/min (d) 9 mL/min (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

The set of figures over the next few pages, Figure 3-33 to Figure 3-36 shows the overall velocity magnitude contours along with the velocity contours in the x, y and z directions for various flow rates. Figure 3-33 is a center cut through the microchannels and shows the x and y direction velocities for each of the ten channels. In this figure it is interesting to see how the swirl pattern that is shown in Figure 3-32 is developed as the velocity increases. For the slower velocities, there is very little definable swirl flow profile, but by 9 mL/min, the swirl pattern is clearly defined. In the y-direction, the fluid has a strong upward velocity on the right side of the channels and a clearly defined, although slightly weaker, downward velocity towards the front of the channels. In the x direction, there is a strong velocity going through the lower left side of the channel that can be seen at all velocities. A slightly negative x-direction velocity also appears at the top center of the channels at higher velocities which is due to the swirl as the fluid flows back towards the front of the channel.

Figure 3-34 is the same cut through the channels but shows the z-direction and overall velocity contours of the channels. It is clear that they are almost exactly the same except in opposite direction. This means that the velocity magnitude is dominated by the velocity in the z-direction and if you compare the velocity scales of the z-direction to that of the x and y-directions, it is clear that this direction is substantially larger, this is elaborated on in Figure 3-37.

Both Figure 3-35 and Figure 3-36 show the x and velocity contours, respectively, from the perspective of perpendicular to both the inlet and the outlet manifold channels. In each image, the inlet is on the top and the outlet is on the bottom. Figure 3-35 shows that for all velocities, the channels closest to the exit have the largest magnitude of

velocity in the y-direction. This effect is more pronounced for faster velocities because the fluid tends to bypass the first couple channels and collects at the last channel. At slower manifold volumetric flow rates, the velocity in the manifold is much more uniform allowing a more even distribution of flow into the microchannels. Figure 3-36 shows that the velocities in the x-direction flow away from the inlet at the bottom of the microchannel and flow back towards the inlet at the top, indicating the swirling motion. This becomes more pronounced at higher flow rates.

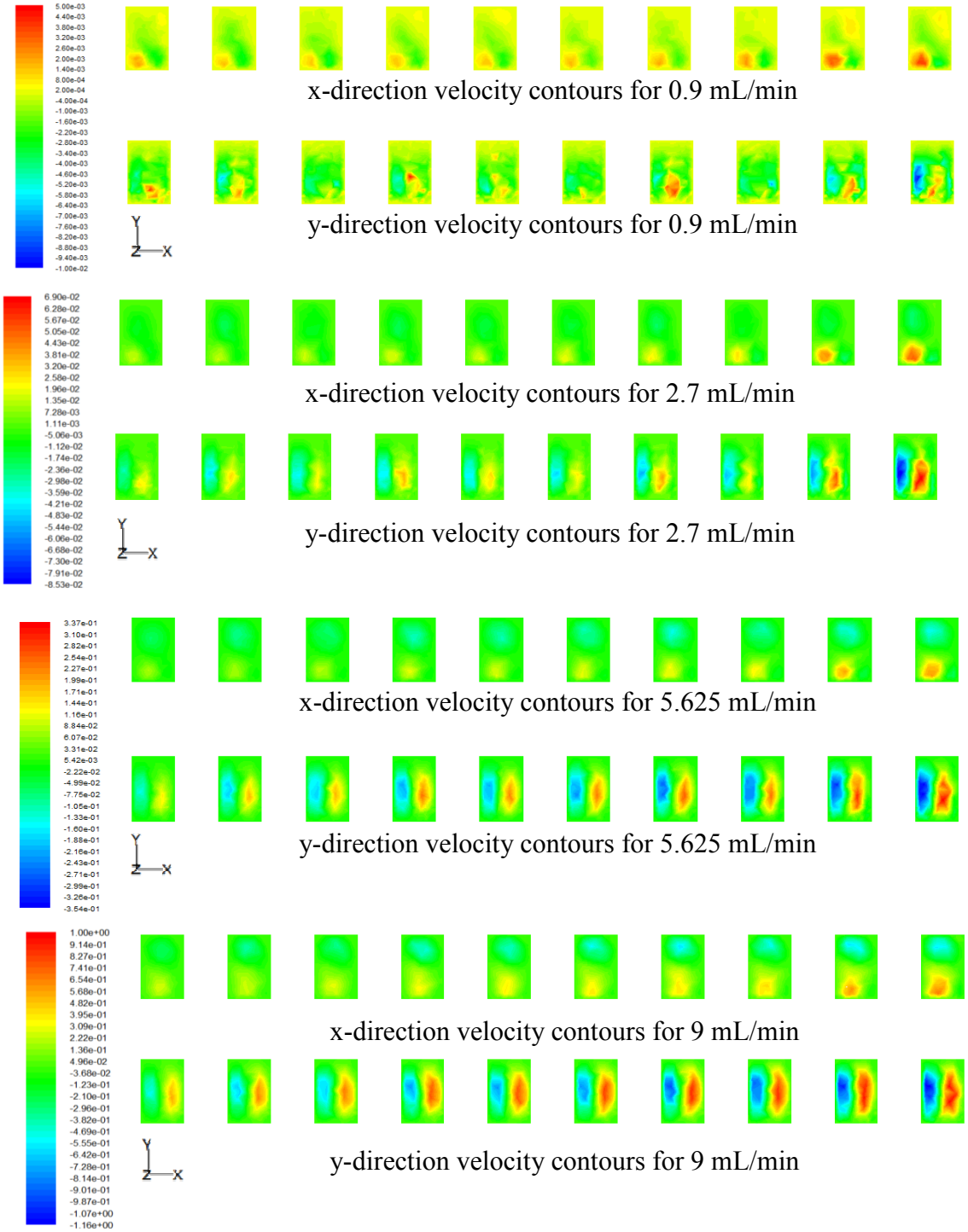


Figure 3-33: X and Y direction velocity profiles for various flow rates (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

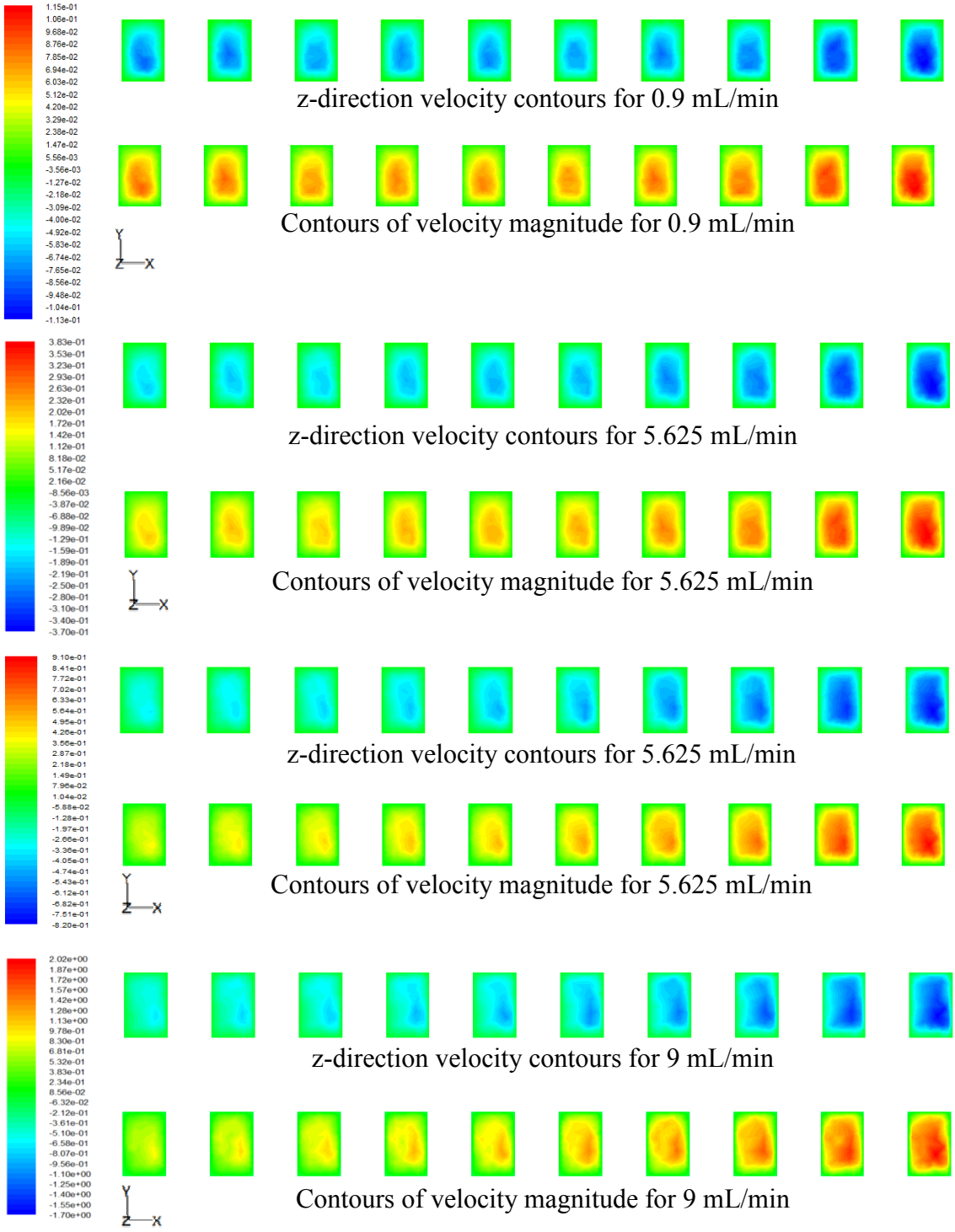


Figure 3-34: Z-direction and total velocity for various flow rates

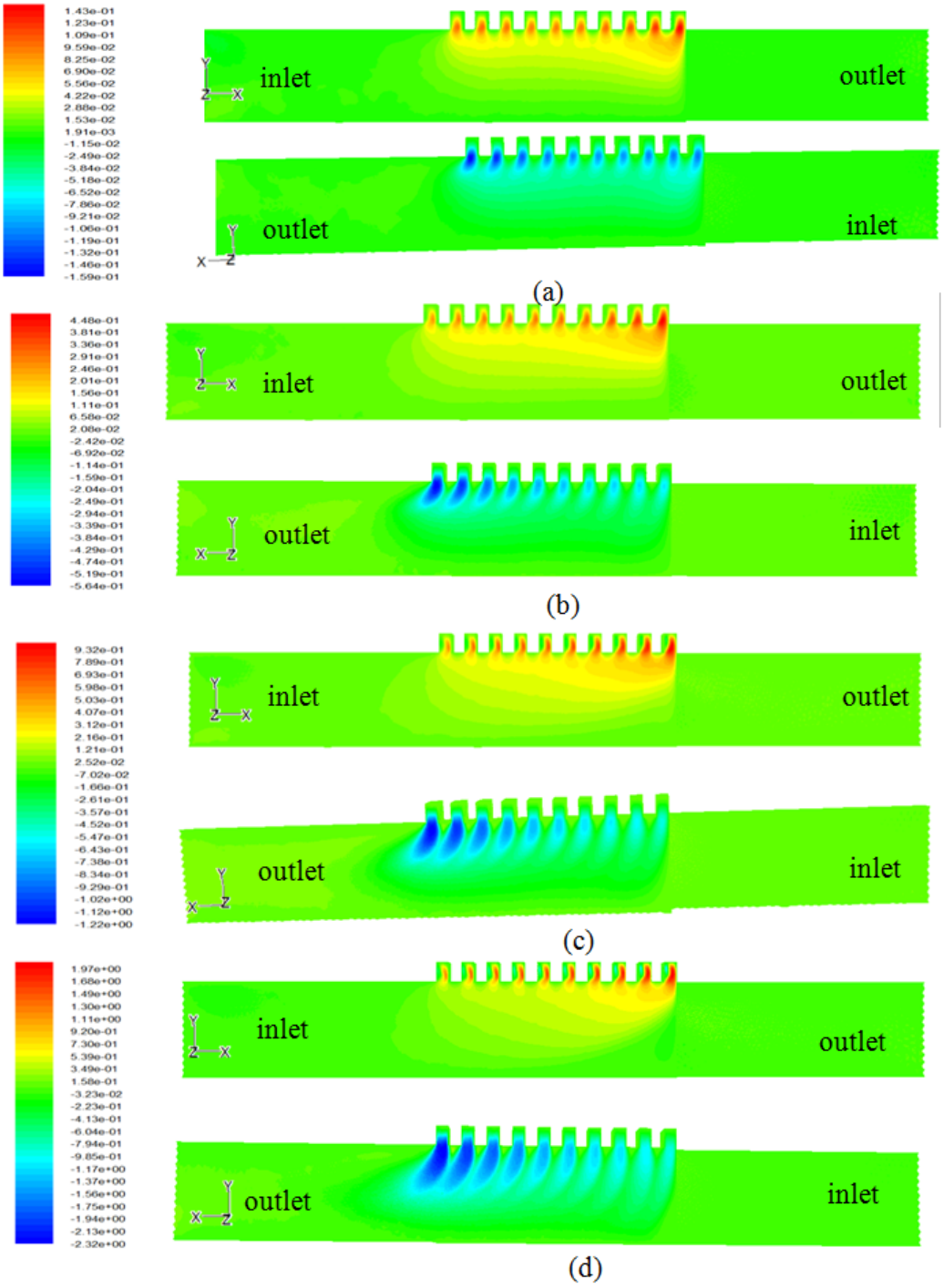


Figure 3-35: Y-velocity profiles from the inlet and exit perspectives for (a) 0.9 mL/min (b) 2.7 mL/min (c) 5.625 mL/min (d) 9 mL/min

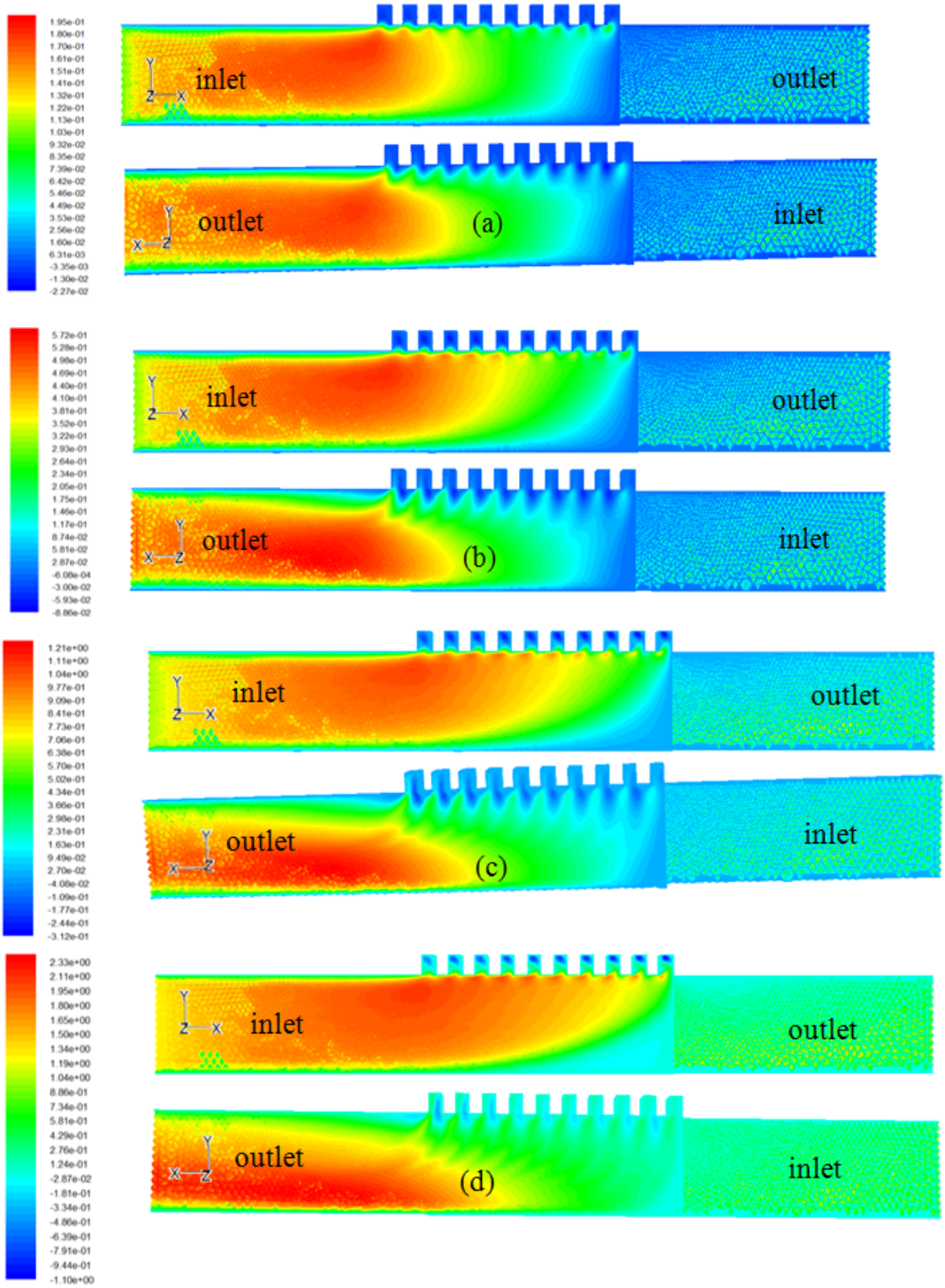


Figure 3-36: X-velocity profiles from the inlet and exit perspectives for (a) 0.9 mL/min (b) 2.7 mL/min (c) 5.625 mL/min (d) 9 mL/min

Figure 3-37 shows a chart of the maximum and minimum velocities for each of the x, y and z directions. These velocities have been found by analyzing the velocities in the center cut of each of the ten microchannels and obtaining both the maximum and minimum values at various flow rates. The chart shows that for all flow rates, the velocities in the z-direction are of the greatest magnitude, indicating this is the primary flow path. The minimum velocity in the z-direction is 0 indicating there is no reverse velocity. Both the x and y velocities have very similar maximum and minimum velocities indicating that there is almost equivalent flow in each direction.

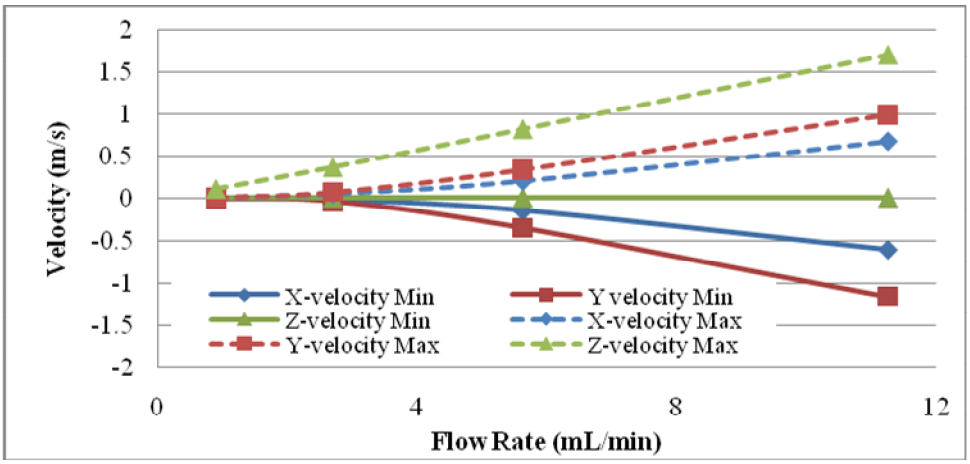


Figure 3-37: Graph of the maximum and minimum x, y and z velocities in the center channel cuts for various inlet flow rates (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

Figure 3-38 shows the velocity contours at the Y-Z cuts through the centers of channels 2, 4, 6, 8, and 10. It shows the velocity magnitudes along with the contours of the velocity in the x, y, and z directions. The velocity magnitude plot shows that the highest velocities start at the inlet channels then move to the outlet channels as the

channels get closer to the exit. The velocity through the microchannels also increases closer to the exit. The plots show the manifold channels have the majority of the flow in the x-direction with very little flow in either the y or z directions. The tops of the microchannels have the majority of the flow in the z-direction and the connection between the manifold and the microchannels is shown in the y-direction.

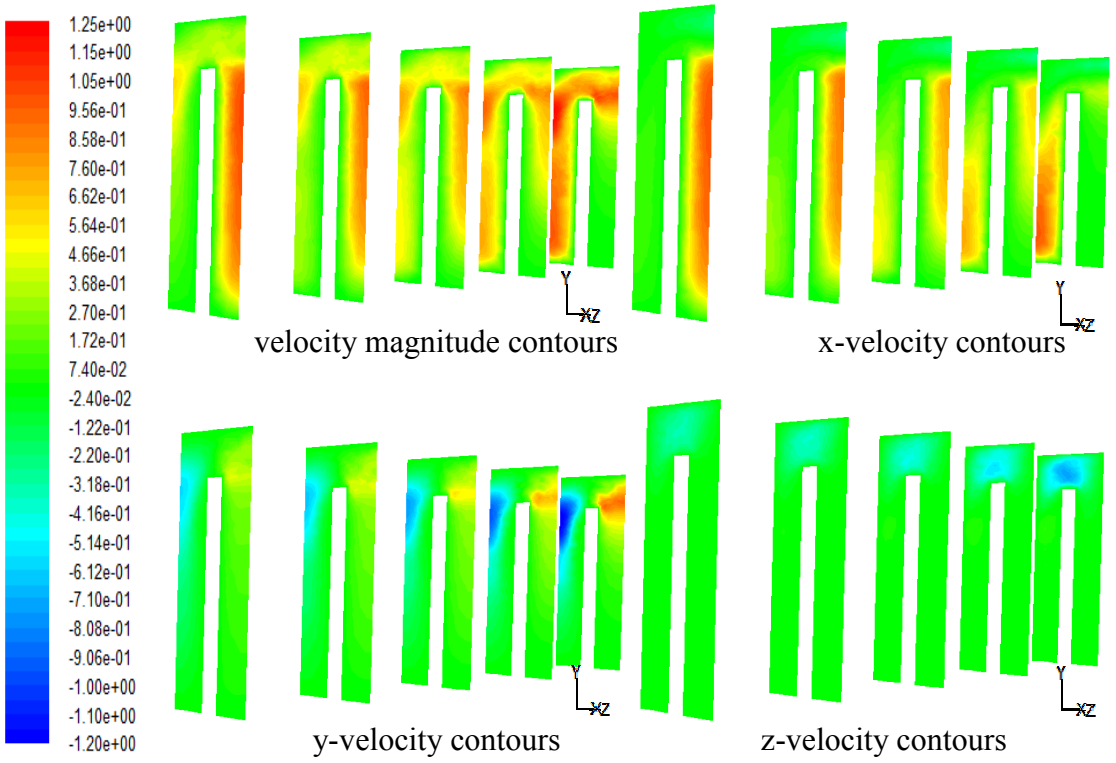


Figure 3-38: Y-Z cuts through channels 2, 4, 6, 8, and 10 showing the velocity magnitude contours, the x-velocity contours, the y-velocity contours and the z-velocity contours (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

3.4.5 Pressure Drops

As was discussed previously, the most important parameters are the pressure drop and the chip temperature. The pressure drop is measured by subtracting the pressure at

the outlet from the pressure at the inlet. The pressure drops for this geometry are shown in both Figure 3-39 and Figure 3-40 for various inlet flow rates. The two figures are the same data but at different scales with the first figure at individual scales and the second figure showing all the figures at the same scale. The figures show that the pressures at the inlet are higher than the pressure at the outlet and also that the pressure drops at lower flow rates are substantially lower than the pressure drops at higher flow rates.

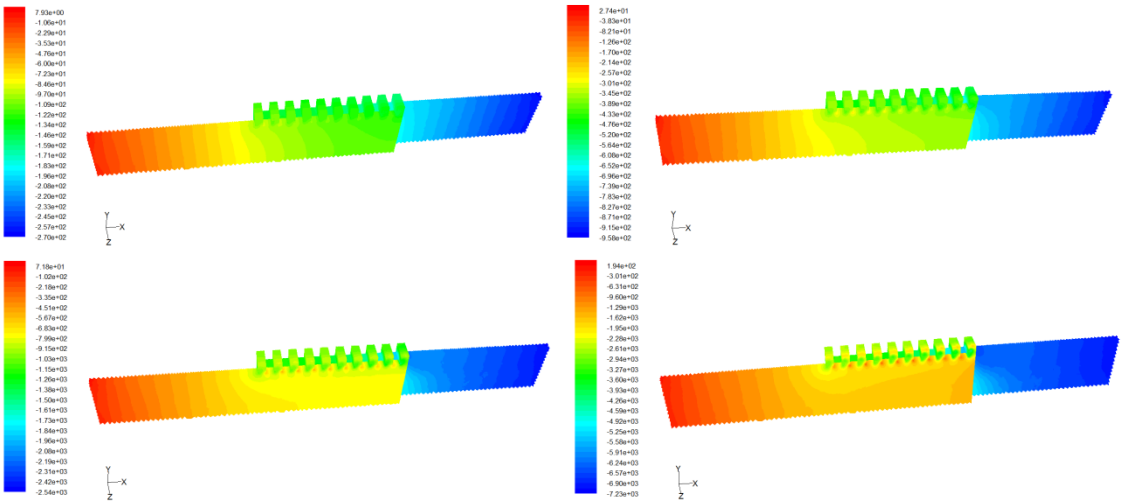


Figure 3-39: Contours of pressure drop for (a) 0.9 mL/min (b) 2.7 mL/min (c) 5.625 mL/min (d) 9 mL/min (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

It is interesting to look at how the pressure drops change as the velocity is increased. At the lower flow rates, the pressure drop in the microchannels is very uniform and quite small across the microchannel, but as the velocity increases, the pressure drop becomes much more apparent.

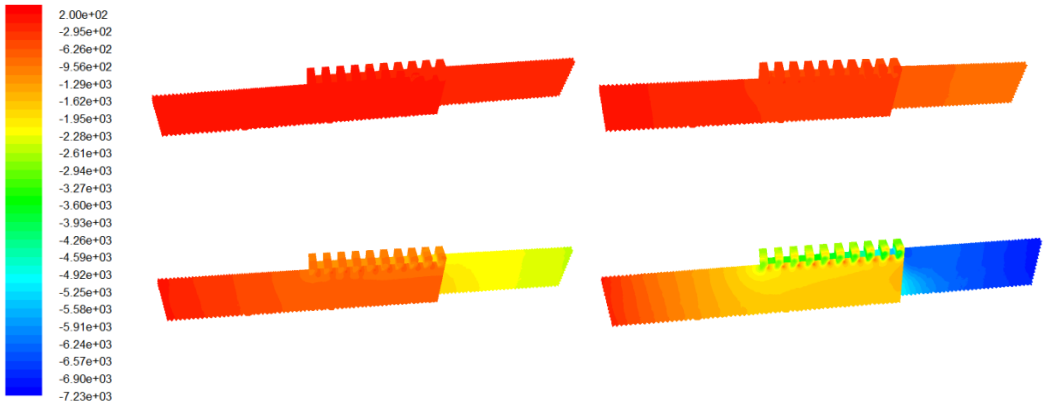


Figure 3-40: Contours of pressure drop shown at the same scale for (a) 0.9 mL/min (b) 2.7 mL/min (c) 5.625 mL/min (d) 9 mL/min pressure drop plots (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

3.4.6 Comparing Single Microchannel to Manifolded Structure

It is interesting to look at how the performance of a single microchannel compares to a manifold structure. Therefore, a model was run for just a single 100 µm microchannel with 100 µm fins whose geometry is shown in Figure 3-41. A chip similar to that used in the MMC model was assumed with the same heat flux (400 W/cm^2) applied to the top surface.

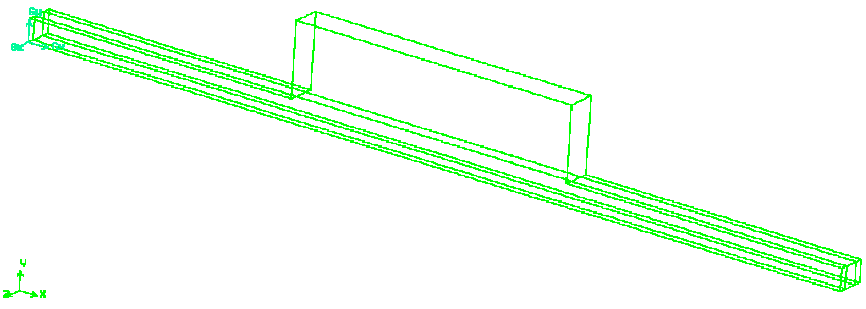


Figure 3-41: Model structure for a single microchannel with m_w = 100 µm and m_f = 100 µm

The models were run with a constant system volumetric flow rate which causes a substantially higher velocity into the microchannels as compared to the manifold geometry. For example, in the case of a system volumetric flow rate of 0.0225 mL/(min*µm), the inlet velocity of the microchannels is 5 m/s and the inlet velocity of the manifold channels is 0.625 m/s which equates to an average flow rate through each microchannel of also 0.625 m/s. (a factor of eight smaller). A plot of the thermal performance versus pressure drop for each of these geometries is shown in Figure 3-42 for various flow rates.

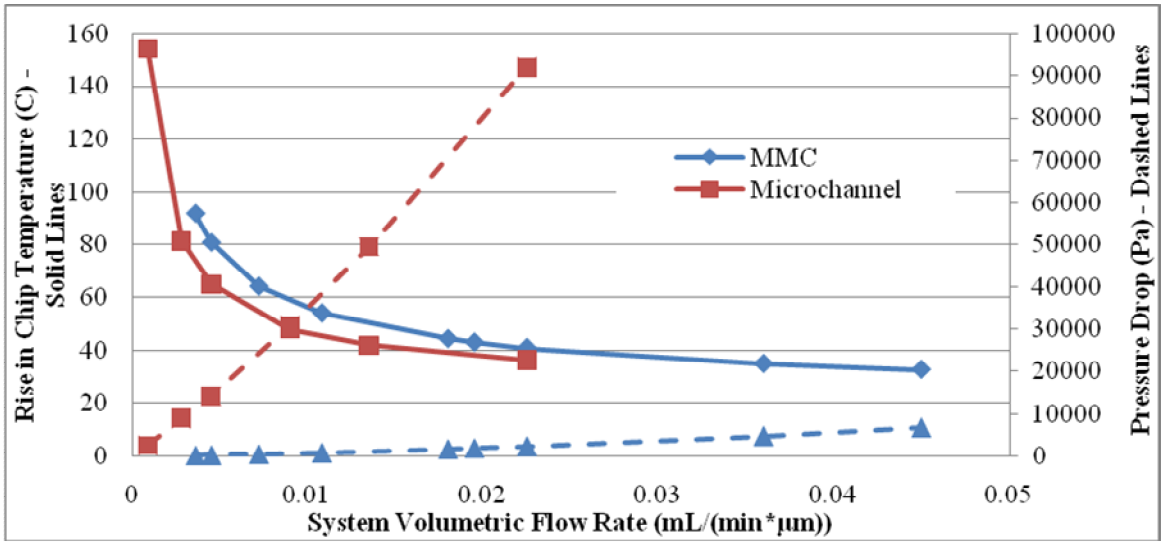


Figure 3-42: Pressure drop versus thermal performance comparing the manifold to microchannel structure each with m_w = 100 µm, m_f = 100 µm and m_h = 150 µm.

Figure 3-42 shows similar thermal performance between the manifold and microchannel systems with the microchannels actually performing slightly better. Whereas, the figure shows the pressure drop is substantially higher for the microchannels than for the manifold channels.

A closer look at the case of 0.0225 mL/(min*µm) shows that the chip temperature rises 40.8 °C for the MMC structure and 36.3 °C for the microchannel, an 11.7% difference and only 4.5 °C increase. The pressure drop of the manifold system and microchannel geometries are 2395 Pa and 91925 Pa, respectively. That is more than a 38 X increase in pressure drop. The thermal contours for the microchannel and the manifold channel is shown in Figure 3-43 and Figure 3-44, respectively.

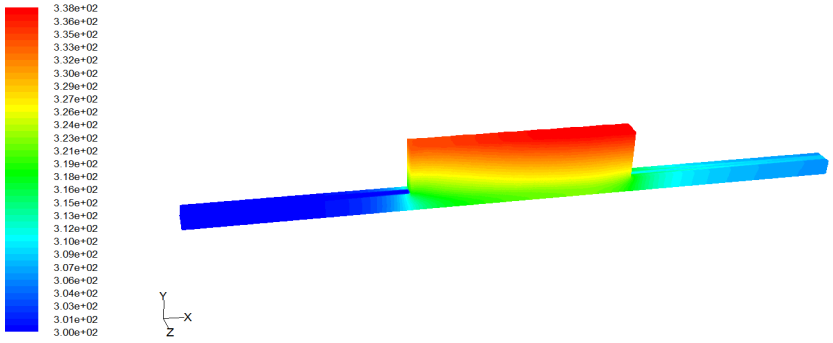


Figure 3-43: Thermal contours results for a single microchannel model at m_w = 100 µm, m_f = 100 µm at q" = 400 W/cm^2 and Q_{system} = 0.0225 mL/(min*µm)

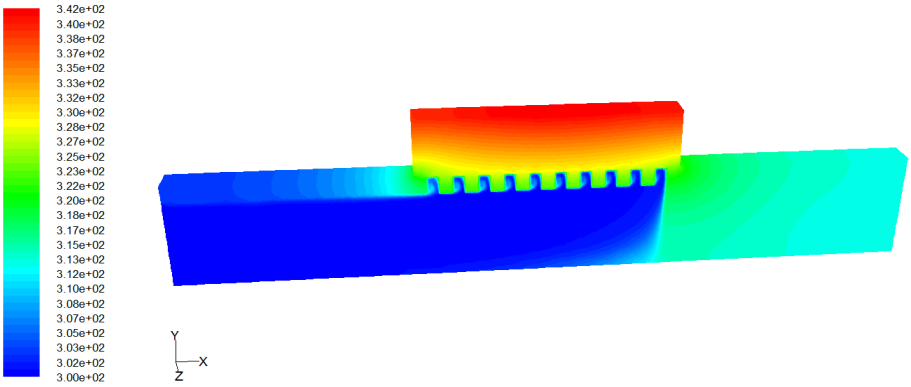


Figure 3-44: Thermal contours results for a manifold structure with m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, M_h = 750 µm, M_w = 200 µm, M_f = 50 µm, q" = 400 W/cm^2, Q_{system} = 0.0225 mL/min*µm

It is interesting to also look at the thermal performance as a function of pressure drop, which is shown in Figure 3-45. The figure clearly shows that for the same system pressure drop, the thermal performance is substantially lower.

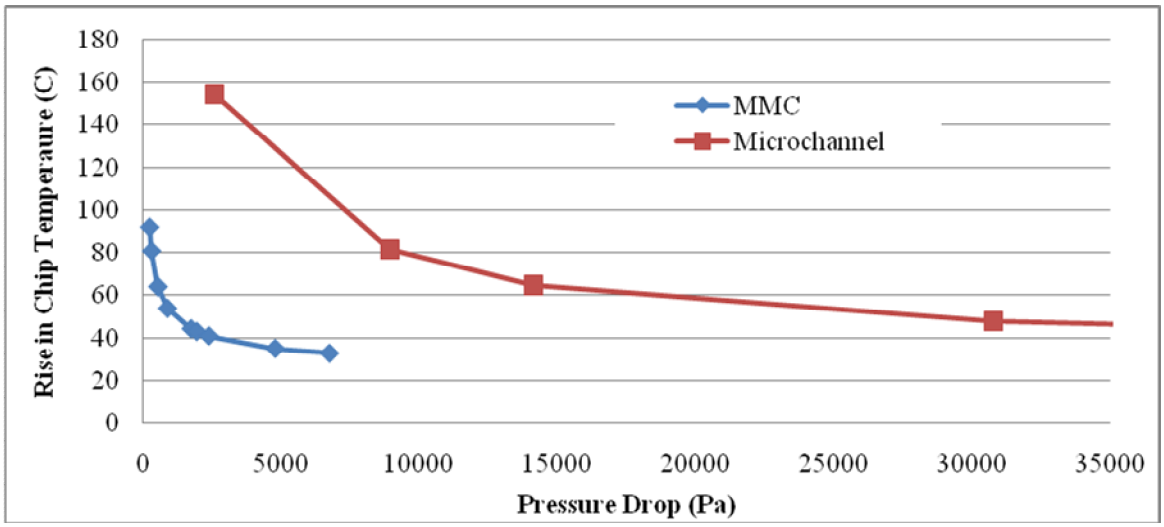


Figure 3-45: Comparison of a manifold and microchannel system showing how the chip temperature increases as a function of the system pressure drop (MMC: m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, M_h = 750 µm, M_w = 200 µm, M_f = 50 µm; Microchannels: m_w = 100 µm, m_f = 100 µm, m_h = 150 µm) both at q" = 400 W/cm^2

3.4.7 Summary of Results from Analysis of a Single Geometry

This section has looked in depth at a single geometry under various flow conditions. Results have been shown for the overall pressure drop, thermal performance and flow conditions. The geometry that was analyzed had parameters: M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, L_{inlet} = 2 mm, and q" = 400 W/cm^2. All of the results in this section are for this specific geometry; a different geometry will lead to different results, but the trends are similar.

The first results that were presented showed the tradeoff between the pressure drop and the thermal performance, which is typical for most microchannel designs. Increased flow rates improve thermal performance but increase system pressure drop. This section discussed a 1% rule to determine a preferred flow rate condition where the temperature changes less than 1% for a 0.1 mL/min change in volumetric flow rate. This allows the temperature to be relatively stable with pressure drop such that small changes in flow rate will not have a large impact on the chip temperature. In this case, the optimum occurs at 4.2 mL/min. This 1% rule should only be used if there are no design restrictions on the chip temperature and/or system pressure drop.

This section also looked at the thermal performance of the microchannels and showed that at low flow rates the fluid heats substantially and at higher flow rates most of the fluid passes through without being heated. This explains why the thermal performance levels off as the flow rate is increased and also why at lower flow rates the temperature increases substantially. The figures also show that there is actually quite a bit of heat transfer occurring in the manifold channels, especially at low flow rates.

The models also showed that the location of the maximum chip temperature shifts from near the exit to being more centralized as the flow rates increase. This has been shown to be due to the velocity variations in the microchannels. The velocities through each channel are very uniform for the lower flow rates and progressively become non-uniform for the increased flow rates. Additionally, the temperature difference across the chips surface increases as the flow rate decreases.

The velocity magnitude vectors show stagnation regions directly above the center of each manifold channel and also at the base of the manifold channel. The area of

maximum velocity is at the fluid exiting the microchannels closest to the exit. These vectors show a looping structure through each microchannel which is more pronounced for faster velocities. The flow goes up and slightly towards the exit as it enters the channel. Then as it reaches the top it flows slightly backward and then down and out of the channel. The flow path is better shown through velocity contour profiles that show the velocity magnitudes in the x, y, and z directions. A clear swirling flow pattern has developed whereas the fluid flows up into the channels towards the exit and swirls in the channel towards the entrance before exiting into the exit manifold channel. Looking at the center cut of the channels, it is clear that the velocity is dominated by the flow in the z-direction through the microchannels with the swirling happening to a lesser extent in the x and y directions.

Plots of pressure contours indicate that the pressures at the inlet are higher than the pressure at the outlet and also that the pressure drops at lower flow rates are substantially lower than the pressure drops at higher flow rates.

The manifold structure is also compared to an equivalent microchannel structure to see the advantage of the MMC structure. When both structures were run at a constant system volumetric flow rate, the straight microchannel showed a slightly better thermal performance (a difference of 4 °C), but a 38 X increase in pressure drop as compared to the MMC structure. The thermal performance of the manifold structure was far superior at the same pressure drop.

This section has looked in depth at a single geometry. While these results are only for this single geometry, their trends are used to understand the conditions of the MMC structure in general. A parametric analysis is conducted in the next chapter.

4 Modeling Parametric Analysis

Simulations were performed to analyze the effects of varying both the manifold and the microchannel dimensions on the overall system performance. Due to the complicated structure of the manifold microchannels, several geometric parameters affect both the thermal performance and overall pressure drop of the system. These include, but are not limited to: manifold channel width (M_w), manifold fin width (M_f), manifold channel height (M_h), microchannel width (m_w), microchannel fin width (m_f), microchannel height (m_h), and the number of microchannels (N_{ch}). All of these parameters, except the microchannel height (m_h) are analyzed in this study for their effect on the performance of the manifold microchannel structure. Other non-geometric parameters also affect the performance, such as inlet flow rates and the heat flux at the chip surface. The main goals of this chapter include:

a. Gain an understanding of the effects on both thermal performance and pressure drop of varying the manifold height, manifold width, manifold fin width, microchannel width and microchannel spacing.
b. Develop plots showing the tradeoff between the pressure drop and thermal performance for various geometric dimensions.
c. Work to find preferred dimensions for given system parameters.
d. Discover the relationships between varying multiple dimensions and try to understand the effect of varying both manifold and microchannel dimensions.
e. Perform a sensitivity analysis on various dimensional parameters to determine which ones have the largest effect on the performance.

4.1 Effect of Varying Manifold Height (M_h) on Performance

The first parameter that will be looked at is the effect of varying the manifold height (M_h) on the performance of the system. A series of manifold heights were modeled while maintaining other dimensions constant: the manifold width (M_w = 200 μm), the manifold fin width (M_f = 50 μm), and the microchannel height (m_h = 150 μm). The manifold heights were varied for four different microchannel geometries, creating a total of 16 different geometries that were analyzed:

- m_w = 100 μm, m_f = 100 μm (M_h = 3750, 1500, 750, and 375 μm): N_{ch} = 10
- m_w = 50 μm, m_f = 50 μm (M_h = 1425, 750, 712.5 and 356.25 μm): N_{ch} = 19
- m_w = 100 μm, m_f = 50 μm (M_h = 1950, 975, 750, and 487.5 μm): N_{ch} = 13
- m_w = 50 μm, m_f = 100 μm (M_h = 975, 750, 487.5, and 243.75 μm): N_{ch} = 13

In order to create a fair comparison between the different microchannel dimensions, the number of channels for each geometric condition was varied to account for a set chip length, L_{chip} = 2 mm. The number of microchannels (N_{ch}) was calculated according to the following equation:

$$N_{ch} = \frac{m_f + L_{chip}}{m_w + m_f} \tag{4-1}$$

Each model was run at various inlet volumetric flow rates. Since the system volumetric flow rate is calculated by dividing the volumetric flow rate by the sum of the manifold channel width and manifold fin width, neither of which is being varied in this modeling study, the system volumetric flow rate is simply a linearly scaled version of the volumetric flow rate. Therefore, both flow rates will produce the same curves and thus only one of the flow rates needs to be investigated.

A list of all the pertinent models is shown in Table 4-1 showing various volumetric flow rates were applied to each of the 16 geometries. For each of the four microchannel geometries, as the M_h is increased for a constant volumetric flow rate, the inlet velocity is reduced but flow rate through each microchannel remained the same.

Table 4-1: List of all pertinent models of the varying microchannel dimensions, various manifold heights and various inlet flow rates

m_w (μm)	m_f (μm)	M_h (μm)	M_w (μm)	M_f (μm)	m_h (μm)	Q (mL/min)	v_{in} (m/s)	v_{uch} (m/s)	Q_{system} (mL/min*μm)	N_{ch}
100	100	3750	200	50	150	9	0.2	1	0.036	10
100	100	1500	200	50	150	9	0.5	1	0.036	10
100	100	750	200	50	150	9	1	1	0.036	10
100	100	375	200	50	150	9	2	1	0.036	10
100	100	3750	200	50	150	5.625	0.125	0.625	0.0225	10
100	100	1500	200	50	150	5.625	0.3125	0.625	0.0225	10
100	100	750	200	50	150	5.625	0.625	0.625	0.0225	10
100	100	375	200	50	150	5.625	1.25	0.625	0.0225	10
100	100	3750	200	50	150	4.5	0.1	0.5	0.018	10
100	100	1500	200	50	150	4.5	0.25	0.5	0.018	10
100	100	750	200	50	150	4.5	0.5	0.5	0.018	10
100	100	375	200	50	150	4.5	1	0.5	0.018	10
50	50	1425	200	50	150	3	0.175	0.351	0.012	19
50	50	712.5	200	50	150	3	0.351	0.351	0.012	19
50	50	356.3	200	50	150	3	0.702	0.351	0.012	19
50	50	1425	200	50	150	5.625	0.329	0.658	0.0225	19
50	50	750	200	50	150	5.625	0.625	0.658	0.0225	19
50	50	712.5	200	50	150	5.625	0.658	0.658	0.0225	19
50	50	356.3	200	50	150	5.625	1.316	0.658	0.0225	19
50	50	1425	200	50	150	9	0.526	1.053	0.036	19
50	50	712.5	200	50	150	9	1.053	1.053	0.036	19
50	50	356.3	200	50	150	9	2.105	1.053	0.036	19
100	50	1950	200	50	150	3	0.128	0.256	0.012	13
100	50	975	200	50	150	3	0.256	0.256	0.012	13
100	50	487.5	200	50	150	3	0.513	0.256	0.012	13
100	50	1950	200	50	150	5.625	0.240	0.481	0.0225	13
100	50	750	200	50	150	5.625	0.625	0.481	0.0225	13
100	50	975	200	50	150	5.625	0.481	0.481	0.0225	13
100	50	487.5	200	50	150	5.625	0.962	0.481	0.0225	13
100	50	1950	200	50	150	9	0.385	0.769	0.036	13
100	50	975	200	50	150	9	0.769	0.769	0.036	13
100	50	487.5	200	50	150	9	1.538	0.769	0.036	13
50	100	975	200	50	150	3	0.256	0.513	0.012	13
50	100	487.5	200	50	150	3	0.513	0.513	0.012	13
50	100	243.8	200	50	150	3	1.026	0.513	0.012	13
50	100	975	200	50	150	5.625	0.481	0.962	0.0225	13
50	100	750	200	50	150	5.625	0.625	0.962	0.0225	13
50	100	487.5	200	50	150	5.625	0.962	0.962	0.0225	13
50	100	243.8	200	50	150	5.625	1.923	0.962	0.0225	13
50	100	975	200	50	150	9	0.769	1.538	0.036	13
50	100	487.5	200	50	150	9	1.538	1.538	0.036	13
50	100	243.8	200	50	150	9	3.077	1.538	0.036	13

Figure 4-1 shows plots of the pressure drop versus the rise in chip temperature for various M_h's and microchannel dimensions. For each of the four microchannel dimensions, as the flow rate is increased, the rise in chip temperature decreases. The interesting thing to point out here is that for any given system volumetric flow rate, there is very little difference in the rise in chip temperature when the M_h is varied.

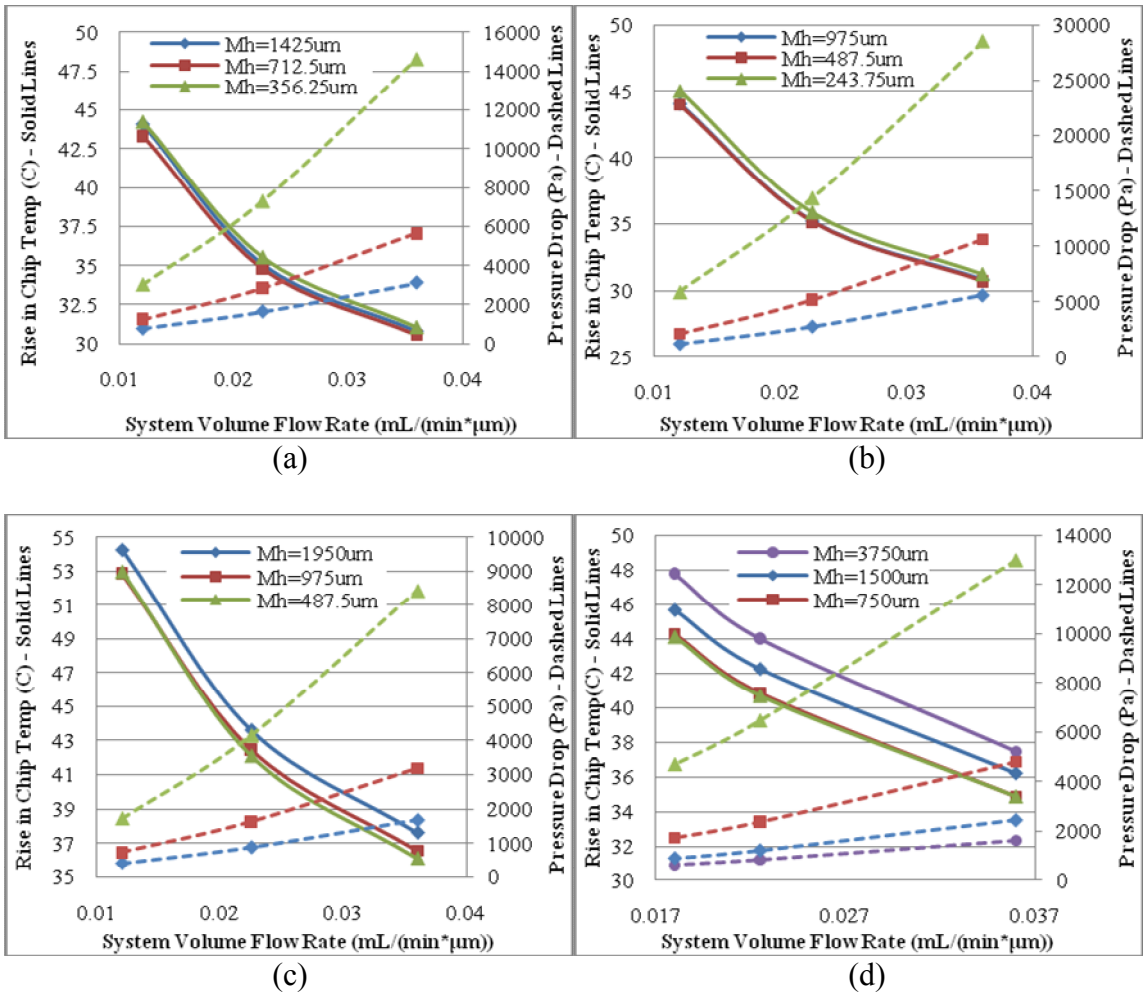


Figure 4-1: The effect of the pressure versus thermal tradeoff for varying the manifold channel height for a variety of system volumetric flow rates (a) m_w = 50 µm, m_f = 50 µm, N_{ch} = 19 (b) m_w = 50 µm, m_f = 100 µm, N_{ch} = 13 (c) m_w = 100 µm, m_f = 50 µm, N_{ch} = 13 (d) m_w = 100 µm, m_f = 100 µm, N_{ch} = 10 (M_w = 200 µm, M_f = 50 µm, m_h = 150 µm, q" = 400 W/cm^2)

The data from Figure 4-1 has been replotted in Figure 4-2 such that the M_h is on the x-axis and the data has been varied according to its volumetric flow rate. Again the graphs show that varying the M_h has very little effect on the device temperature. This is an expected result because the average velocities through the microchannels should be similar because the volumetric flow rate is the same. Since the microchannels are where the majority of the cooling takes place, then the temperature should also be the same.

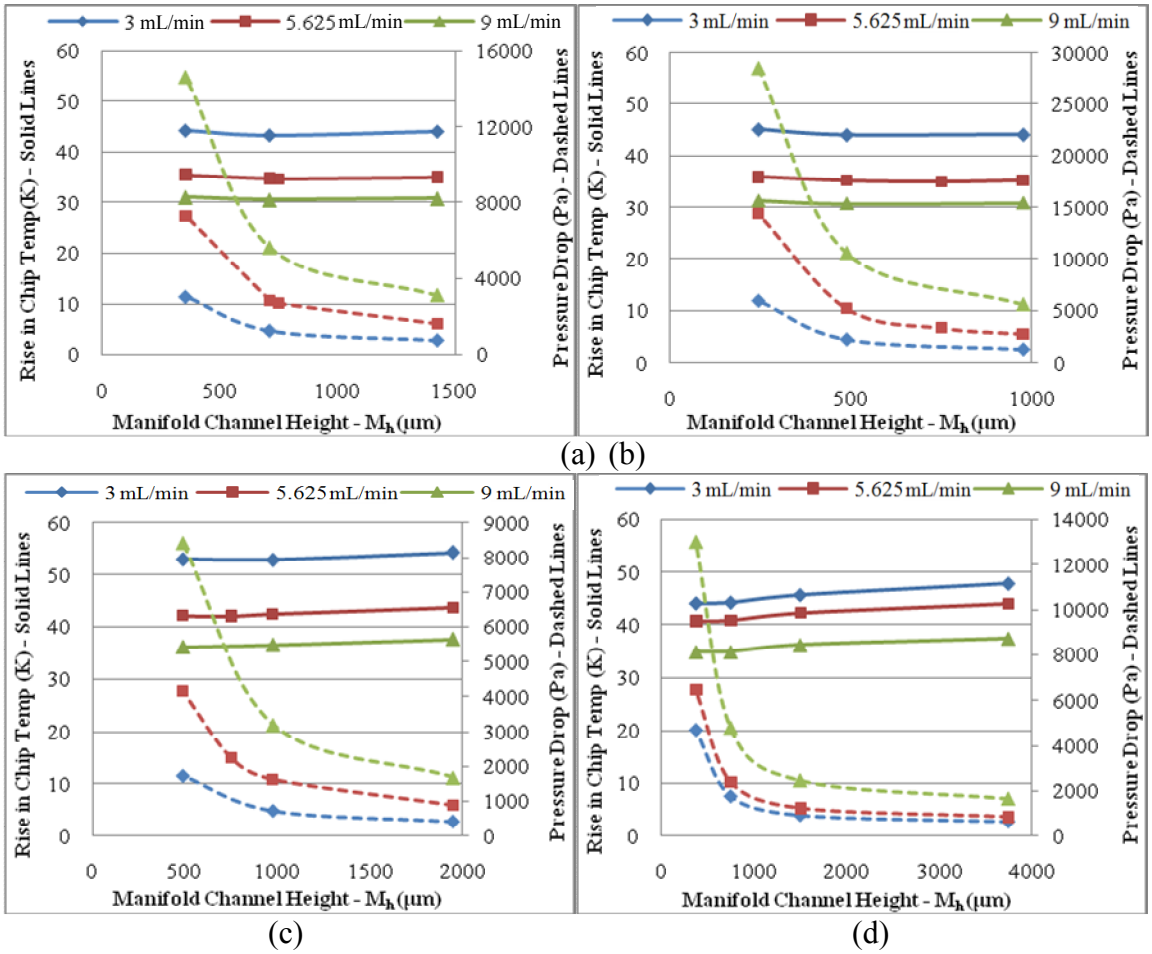


Figure 4-2: The effect of the pressure versus thermal tradeoff for varying the manifold channel height for a variety of microchannel dimensions (a) m_w = 50 µm, m_f = 50 µm, N_{ch} = 19 (b) m_w = 50 µm, m_f = 100 µm, N_{ch} = 13 (c) m_w = 100 µm, m_f = 50 µm, N_{ch} = 13 (d) m_w = 100 µm, m_f = 100 µm, N_{ch} = 10 (M_w=200 µm, M_f=50 µm, m_h = 150 µm, q" = 400 W/cm^2)

Both Figure 4-1 and Figure 4-2 also show the effect of the flow rates and the M_h on the pressure drop. As the flow rates increase, the pressure drops also increase. But the interesting thing to notice is that as the manifold heights decrease, there is a substantial increase in the pressure drop, especially at smaller manifold heights. For example, in Figure 4-1d, as the M_h is decreased from 750 μm to 375 μm, a factor of two, the pressure drop increases from about 5000 Pa to about 13000 Pa, almost a factor of three for a system volumetric flow rate of 0.036 mL/(min*μm). As the M_h is increased this effect on the pressure drop is lessened, as is shown in Figure 4-2.

Since altering the M_h has little effect on the chip temperature and increasing the M_h decreases the pressure drop for a given flow rate, then making the M_h as large as possible is ideal. But due to fabrication limitations and size restrictions, simply making the manifold as tall as possible is not an option. Additionally, as the manifold height is increased, the magnitude of the reduction in pressure drop levels off. Therefore, there is a point at which increasing the M_h any further will have little effect on the system pressure drop. This leads to the conclusion that there is an ideal manufacturable M_h.

While a more thorough analysis of the effect of the microchannel dimensions will be shown in Section 4.5, a brief look at how they affect the performance for varying manifold heights is shown in Figure 4-3. The figure shows pressure drops for each microchannel dimensions is relatively similar. But it is clear that the m_w has a substantially larger effect on thermal performance than the m_f. This is clear because when the fin width differs for a constant microchannel width, the rise in chip temperature is relatively constant. But if the microchannel fin width is held constant and the microchannel width is increased, there is a significant rise in device temperature.

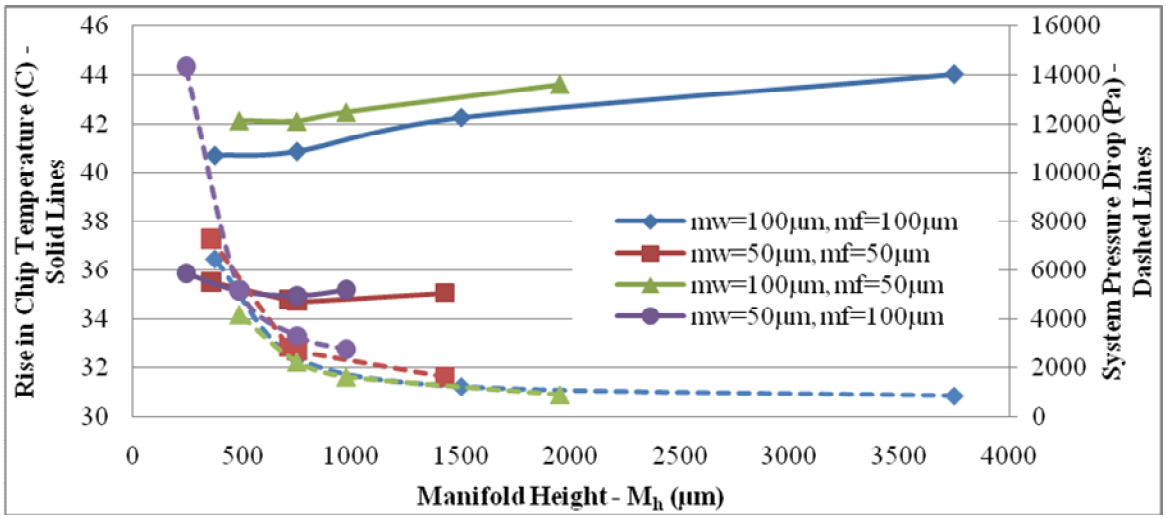


Figure 4-3: The effect of the pressure versus thermal tradeoff for varying the manifold channel height for varying microchannel dimensions all at a volumetric flow rate of 5.625 mL/min (q" = 400 W/cm^2, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_h = 150 µm, L_{chip} = 2 mm)

When determining the geometric parameters it is important to take into account the system requirements. For example, if a design requires the pressure drop be less than 5000 Pa, then a dashed line can be drawn at that parameter and the designer must design in this region. This is shown in Figure 4-4 along with the horizontal dashed line at 5000 Pa. Clearly, under this requirement, it makes a manifold height of 375 µm out of the question. If it is also desirable to have a volumetric flow rate less than 7 mL/min, then another vertical line must be drawn and only parameters in the dark grey rectangle on the lower left of the image can be used. In this region, the lowest chip temperature occurs with a M_h = 750 µm, but the lowest pressure drop occurs at M_h = 3750 µm. Since a M_h = 750 µm is well within the required 5000 Pa pressure drop, then that will probably be the best choice to satisfy the requirements without over designing. Taking the system requirements into consideration is a necessity when considering all geometric conditions, not just the manifold height.

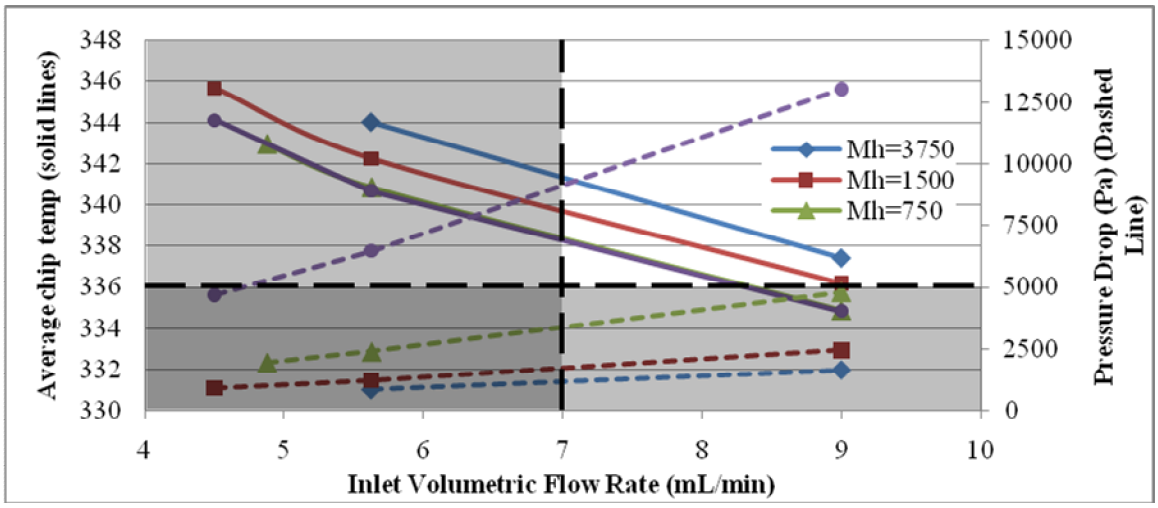


Figure 4-4: Image showing how the system requirements will determine the dimensions of the system by limiting portions of the curve based on the pressure drop and flow rate requirements (m_w = 100 µm, m_f = 100 µm, N_{ch} = 10, M_w = 200 µm, M_f = 50 µm, m_h = 150 µm, q" = 400 W/cm^2)

As was shown previously, chip temperature uniformity is based on the velocity flow rates through the microchannels; therefore, it is interesting to see how the flow rates and chip temperature are affected for varying M_h's. For the MMC model with dimensions M_w = 200 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, and N_{ch} = 10 with M_h varying from 375 µm to 3750 µm, the plots of the center line chip temperatures and the velocity flow rates per channel are shown in Figure 4-5. The graphs on the left side show the velocity flow distribution in the channels for various volumetric flow rates. Clearly as M_h increases, the microchannel flow rates become more uniform. At the smallest M_h, the flow rate is extremely varied with the flow velocities of the microchannels closest to the exit being 6-8 times faster than microchannels closest to the inlet.

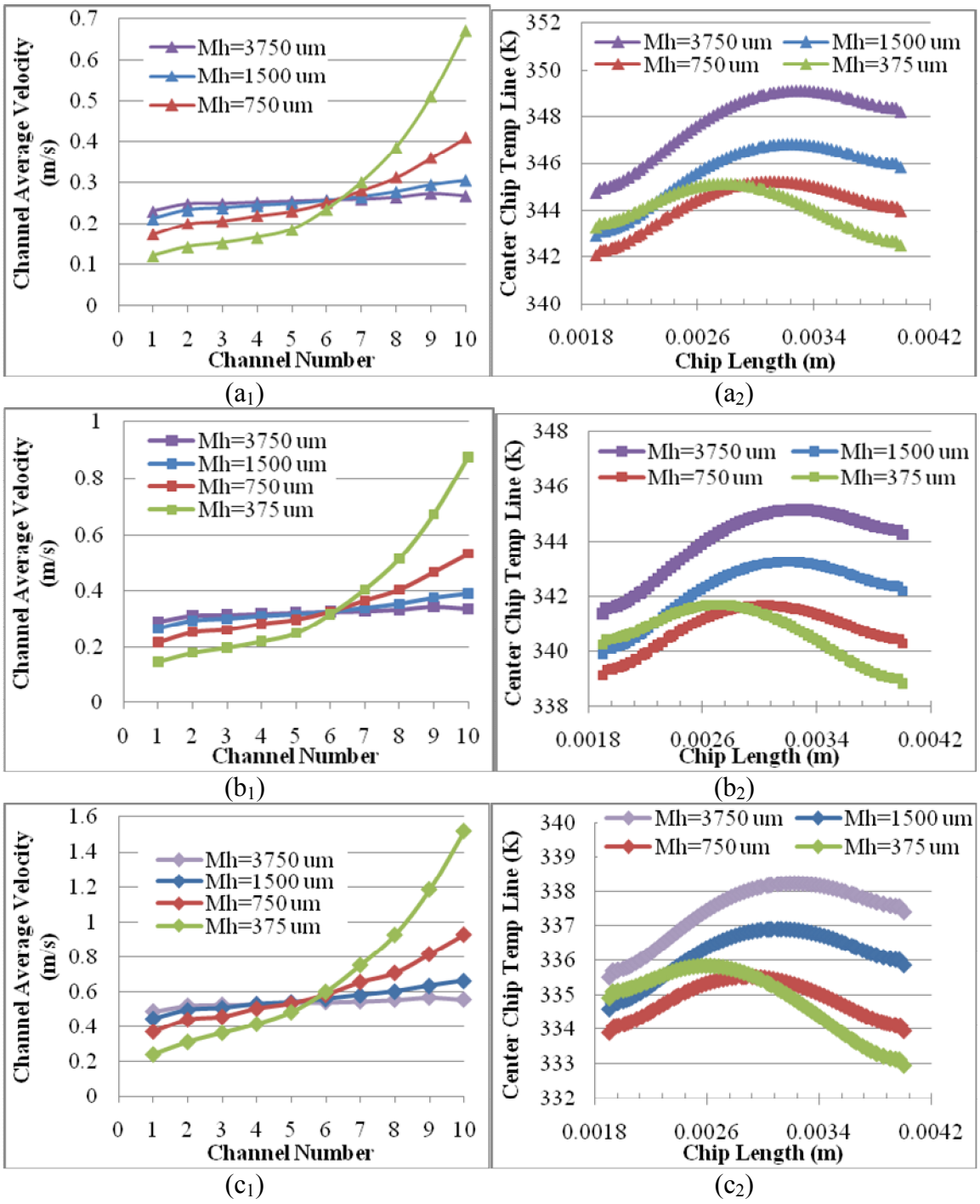


Figure 4-5: Graphs showing the effect of varying the manifold channel height for the (a_1) average flow rate per channel for 4.5 mL/min (a_2) center chip temperature line for 4.5 mL/min (b_1) average flow rate per channel for 5.625 mL/min (b_2) center chip temperature line for 5.625 mL/min (c_1) average flow rate per channel for 9 mL/min (c_2) center chip temperature line for 9 mL/min (M_w = 200 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, and N_{ch} = 10)

The increasing velocity gradient with decreasing manifold height is caused by the faster velocity entering the smaller manifold channels, which happens because they have the same inlet volumetric flow rate. This faster velocity causes the fluid in the manifold to flow quickly to the end of the manifold where it hits a wall and it forced into the channels with substantially more velocity at that end. Therefore, the manifold height has a substantial effect on the velocity profiles in the channels. Therefore, as was shown earlier, this means that the M_h will have an effect on the chip temperature uniformity as is shown by the graphs on the right side of Figure 4-5. The figures show that for all velocities, as the manifold height decreases, the hot spot moves towards the inlet of the structure. In these cases though, there appears to be a point at which the chip temperature is minimized before the hot spot starts progressing towards the inlet causing the average device temperature to increase. In this example, the preferred manifold height appears to be at around 750 μm for all volumetric flow rates.

A visual look at the velocity gradients in the inlet manifold channel is shown in Figure 4-6. It is clear that when the M_h is very tall, that the velocity through the manifold is very small which allows the flow distribution into each channel to be very even, Figure 4-6a. On the other hand, when the M_h is very small, Figure 4-6d, the velocity through the manifold is very large which causes the velocities in the microchannels closer to the end to be much larger than the microchannels at the beginning.

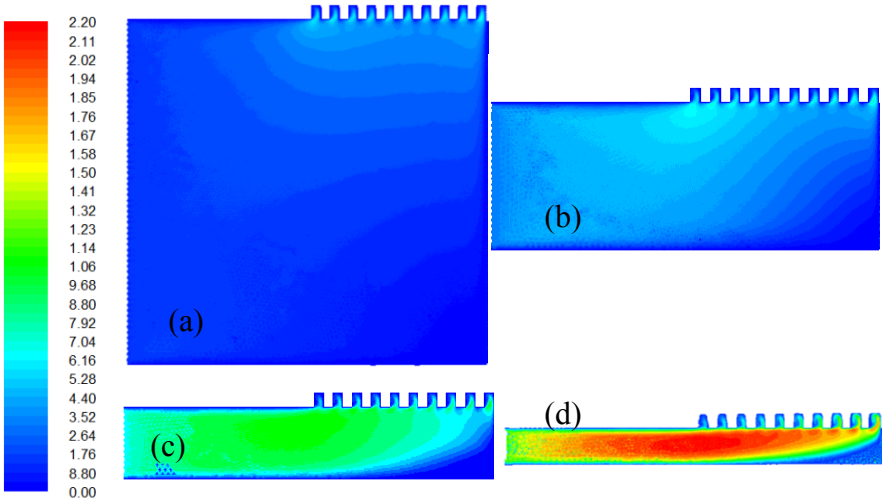


Figure 4-6: Velocity profiles through the center cut of the inlet manifold channel into the microchannels for Q = 5.625 mL/min at (a) M_h = 3750 µm (b) M_h = 1500 µm (c) M_h = 750 µm (d) M_h = 375 µm (M_w = 200 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, and N_{ch} = 10)

Figure 4-7 shows the thermal profiles through the center cut of the device. The figure shows that there is actually quite a bit of heat that is transferred into the manifold channel both from the fins and from the exiting heated fluid. The location of the hottest part of the chip can also be seen moving toward the inlet as the manifold height increases. It is necessary to point out that while there is deviation in the center chip line profiles in Figure 4-5, the difference between the temperatures is not substantial. This is also seen in the figure below such that the thermal profiles in all cases are relatively similar and in most cases, the difference between chip temperatures is just a few degrees.

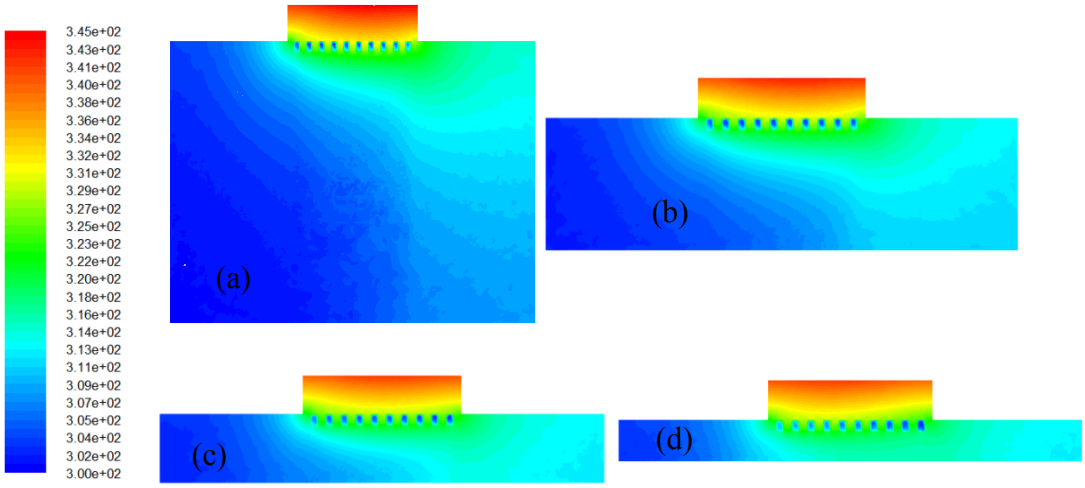


Figure 4-7: Thermal profiles through the center cut of the device for Q = 5.625 mL/min at (a) M_h = 3750 µm (b) M_h = 1500 µm (c) M_h = 750 µm (d) M_h = 375 µm (M_w = 200 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, and N_{ch} = 10)

Since varying the manifold height has very little influence on the chip temperature, but a significant effect on the pressure drop, in general a larger manifold height would be better because it would decrease the pressure drop. However, there is a point at which the improvement in pressure drop outweighs the increase in size. Therefore, the charts can be used to determine the optimum manifold height.

4.2 Effect of Varying Manifold Fin Width (M_f) on Performance

A series of models were run to assess the effect of varying the manifold fin width (M_f) on the MMC performance. The list of all the pertinent models that were run is shown in Table 4-2. The M_w and M_h were both held constant at 200 µm and 750 µm, respectively. The M_f was varied between 50, 100 and 150 µm. The microchannel dimensions were also constant at m_w = 100 µm, m_f = 100 µm and m_h = 150 µm. Each of the three geometric conditions was modeled at a variety of inlet flow rates.

Table 4-2: List of models and their parameters for assessing the effect of M_f on performance.

m_w (μm)	m_f (μm)	M_h (μm)	M_w (μm)	M_f (μm)	m_h (μm)	Q (mL/min)	v_{in} (m/s)	$V_{microchannel}$ (m/s)	Q_{system} (mL/(min*μm))	N_{ch}
100	100	750	200	50	150	0.9	0.1	0.1	0.0036	10
100	100	750	200	100	150	0.9	0.1	0.1	0.003	10
100	100	750	200	150	150	0.9	0.1	0.1	0.00257	10
100	100	750	200	50	150	1.8	0.2	0.2	0.0072	10
100	100	750	200	100	150	1.8	0.2	0.2	0.006	10
100	100	750	200	150	150	1.8	0.2	0.2	0.005142	10
100	100	750	200	50	150	2.7	0.3	0.3	0.0108	10
100	100	750	200	100	150	2.7	0.3	0.3	0.009	10
100	100	750	200	150	150	2.7	0.3	0.3	0.0077	10
100	100	750	200	50	150	4.875	0.5417	0.54167	0.0195	10
100	100	750	200	50	150	4.5	0.5	0.5	0.018	10
100	100	750	200	100	150	4.5	0.5	0.5	0.015	10
100	100	750	200	150	150	4.5	0.5	0.5	0.01286	10
100	100	750	200	50	150	5.625	0.625	0.625	0.0225	10
100	100	750	200	100	150	6.75	0.75	0.75	0.0225	10
100	100	750	200	150	150	7.875	0.875	0.875	0.0225	10
100	100	750	200	50	150	9	1	1	0.036	10
100	100	750	200	100	150	9	1	1	0.03	10
100	100	750	200	150	150	9	1	1	0.0257	10

A plot of the tradeoffs between the system pressure drop and the thermal performance for various system volumetric flow rates are shown in Figure 4-8. The figure shows that varying the manifold fin width has very little effect on the thermal performance but a significant effect on the overall system pressure drop. In order to demonstrate this, it is interesting to look at one of the flow rates more closely. For a system volumetric flow rate of 0.0225 mL/(min*μm), the average device temperature when the M_f = 50 μm is 340.8 K and is 338.7 K when the M_f = 150 μm. That is a decrease of only 5.3% when the manifold fin is increased by a magnitude of three. Whereas the system pressure drop is 2395 Pa when the M_f = 50 μm and is 4020 Pa when the M_f = 150 μm, which is a substantial 50.7% increase in the system pressure drop. It might be a little confusing as to why the thermal performance actually improves when the M_f is increased. This is because in this situation, it is the system volumetric flow rate that

is being held constant which means that the system with the smaller M_f will have a smaller volumetric flow rate. For example, when the system volumetric flow rate is 0.0225 mL/(min*µm), the volumetric flow rate for M_f = 50 µm is 5.625 mL/min and the volumetric flow rate for M_f = 150 µm is 7.875 mL/min. Since the microchannel dimensions remain the same, the larger fin widths have a much faster flow rate per channel (0.625 m/s for M_f = 50 µm and 0.875 m/s for M_f = 150 µm). The longer manifold fin width should allow for more heating of the fluid which would cause the chip to get hotter but the faster flow rate counteracts with that to cause the chip temperature to remain relatively the same and actually slightly better for the larger manifold fin. But the larger manifold fin width creates a faster flow rate in the microchannels and also a longer distance the fluid is in the channels, both of which cause the pressure drop to increase substantially. Therefore, in general the manifold fin width should be minimized.

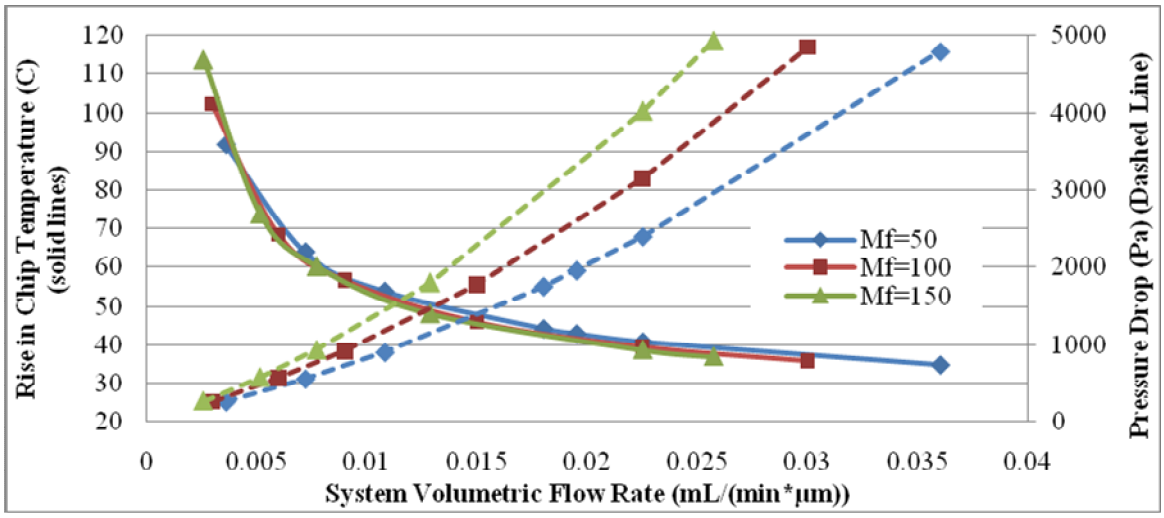


Figure 4-8: Plot depicting the tradeoff between the system pressure drop and the thermal performance as a function of the system volumetric flow rate for various manifold fin widths (M_w = 200 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch}=10, q" = 400 W/cm^2)

Another thing to point out in Figure 4-8 is the effect of the system volumetric flow rate on the performance. The figure shows that for these particular geometries, the average chip temperature rises drastically for flow rates less than about 0.01 mL/(min*µm), therefore it would be advantageous to operate the system at flow rates greater than this. Increasing the flow rate too much past this point causes a significant increase in pressure drop for a minimal increase in thermal performance.

In addition to the system volumetric flow rate, it is also interesting to look at how the volumetric flow rate affects the system performance. A plot of the tradeoff between thermal performance and pressure drop is shown in Figure 4-9. The plot shows that for any given inlet volumetric flow rate, if the M_f is increased, the pressure drop remains practically equivalent while the chip temperature rises. This shows that increasing M_f does not have a significant effect on pressure drop for a constant volumetric flow rate.

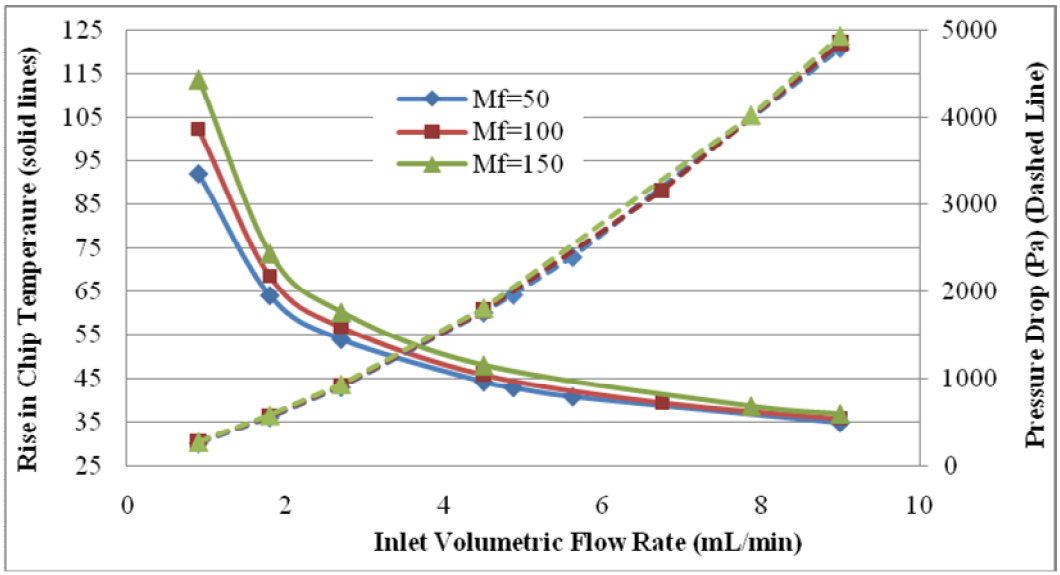


Figure 4-9: Plot depicting the tradeoff between the system pressure drop and the thermal performance as a function of the volumetric flow rate for various manifold fin widths (M_w = 200 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch}=10, q" = 400 W/cm^2)

It is interesting to take a closer look at the data from Figure 4-9 by evaluating the data at three different volumetric flow rates: 0.9 mL/min, 4.5 mL/min and 9 mL/min. The pressure drops are shown in Table 4-3 along with the percent difference. In all flow rate cases, the percent difference in the pressure drops from a manifold fin width of 50 to 150 μm is less than 5% and on average only 3.25%. This indicates that there may be a slight increase in the pressure drop when the manifold fin width is increased, which could be attributed to the longer distance the fluid has to flow through the microchannel.

Table 4-3: Table showing the pressure drops and the average chip temperature rise for both manifold fin widths of 50 and 150 μm for various volumetric flow rates (M_w = 200 μm, M_h = 750 μm, m_w = 100 μm, m_f = 100 μm, m_h = 150 μm, N_{ch}=10, q" = 400 W/cm^2)

	Pressure Drops (Pa)			Chip Temperature Rise (°C)		
	0.9 mL/min	**4.5 mL/min**	**9 mL/min**	**0.9 mL/min**	**4.5 mL/min**	**9 mL/min**
M_f = 50 μm	256.4	1752.8	4789.5	91.9	44.3	34.9
M_f = 150 μm	267.4	1801.5	4926.4	113.8	48	36.9
% Difference	4.2%	2.7%	2.8%	21.3%	8.0%	5.6%

Table 4-3 also shows the chip temperature rise for various flow rates when the M_f is increased from 50 to 150 μm which is much more significant than the pressure drops. The lower flow rates have a much larger difference in the temperature rise than the higher flow rates. It is over a 20% difference in the rise in chip temperature between 50 μm and 150 μm at 0.9 mL/min, whereas at 9 mL/min the percent difference is less than 6%.

Therefore, as the manifold fin width is increased, at any given volumetric flow rate, there is only a slight increase in the pressure drop of the system. But the variation in thermal performance is dependent on the flow rate where at low flow rates, there is a large deviation in performance but at higher flow rates there is little difference.

Consequently, at higher volumetric flow rates, varying the manifold fin has little effect on either the pressure drop or the thermal performance of the system. In general, this does indicate that for a given volumetric flow rate, a smaller manifold fin width would allow for better performance both thermally and in terms of required system pumping power.

It is interesting to see the effect of increasing the M_f the chip surface non-uniformity in the z-direction. Figure 4-10 shows the surface temperature profiles for a volumetric flow rate of 0.9 mL/min for each of the three modeled M_f's. It is clear that in each case, there is no detectable increase in the temperature in the z-direction. Since these plots were made at the slowest flow rate (0.9 mL/min) with no detectable change, it is reasonable to assume no change would be detected at any faster flow rate. A change might be detected if the M_f was further increased but due to the increase in pressure drop this would cause, it is unlikely the M_f would be increased much further.

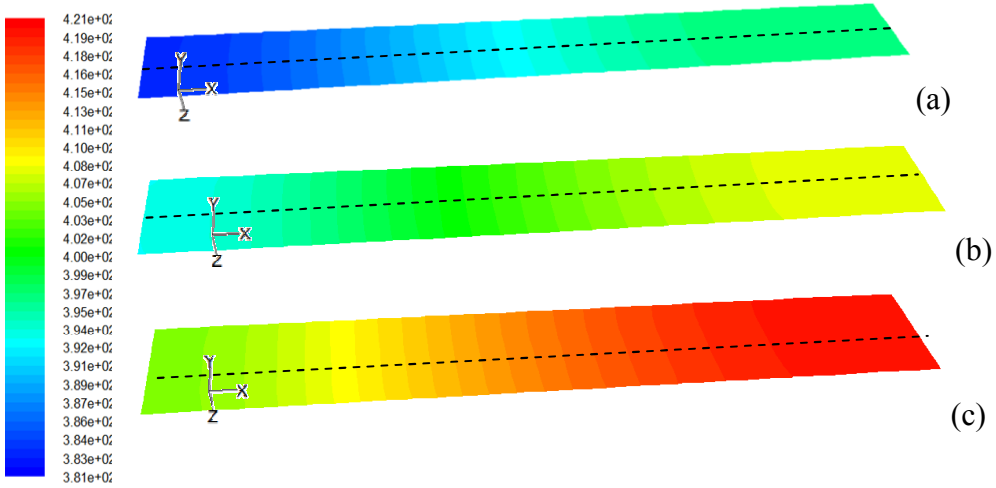


Figure 4-10: Graphs showing the temperature contours across the chip surface at 0.9 mL/min for (a) M_f = 50 µm (b) M_f = 100 µm and (c) M_f = 150 µm (M_w = 200 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch}=10, q" = 400 W/cm^2). Units are in Kelvin.

Since Figure 4-11 shows such significant thermal gradients across the chip surface, the next thing to investigate is the surface temperature profiles. The center line chip temperature profiles, shown by the dashed lines in Figure 4-10, are plotted in Figure 4-11 for the three M_f's at 0.9 mL/min, 2.7 mL/min and 9 mL/min.

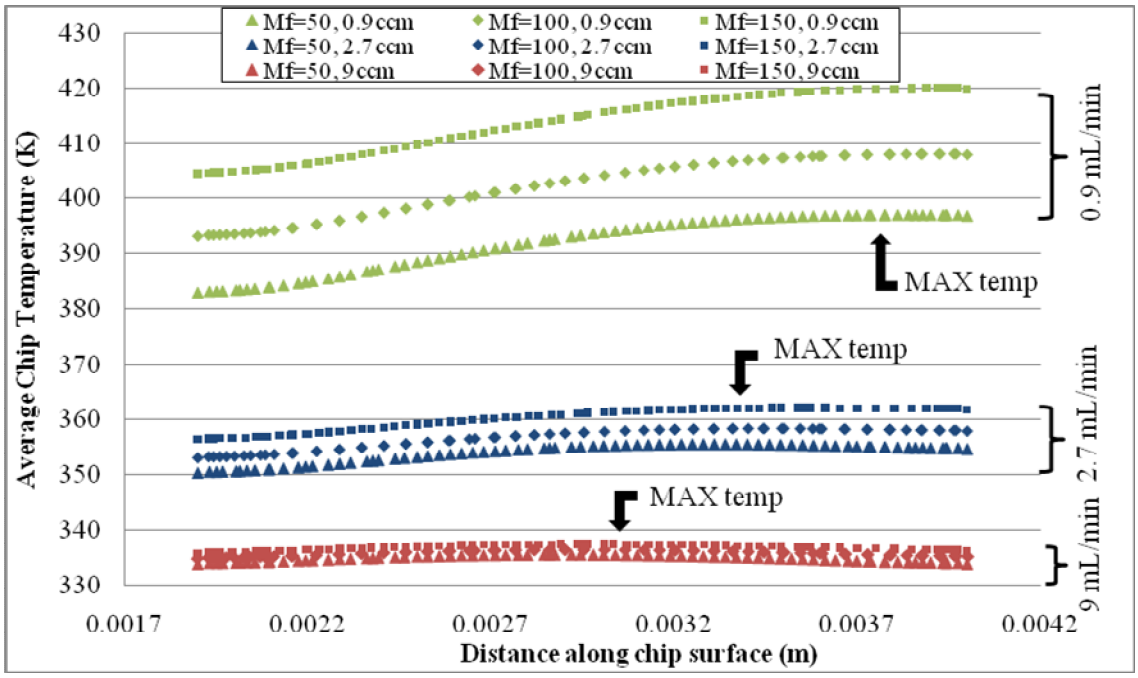


Figure 4-11: Center line chip surface temperature profiles for various inlet velocities and Mf's (M_w = 200 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch}=10, q" = 400 W/cm^2)

It is interesting to point out from Figure 4-11 that the shape of the temperature profiles for a given flow rate does not change as the manifold fin width is changed; it is simply offset by a certain temperature. This offset is plotted in Figure 4-12 and is larger for the smaller volumetric flow rates and vice versa. This means that by increasing the manifold width, the overall chip temperature rises by a fixed offset and the location of the hot spot and the temperature difference across the chips surface do not change.

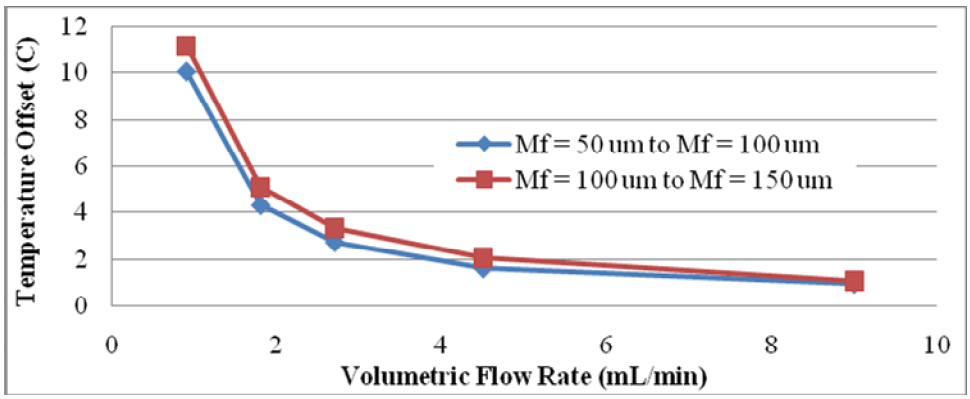


Figure 4-12: Plot of the temperature offset versus volumetric flow rate for varying between a manifold fin width of 50 µm to 100 µm and also from 100 µm to 150 µm (M_w = 200 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch}=10, q" = 400 W/cm^2)

Figure 4-11 also shows that as the volumetric flow rate increases, the location of the maximum chip temperature becomes more centralized. This was shown previously in Section 3.4.3 to be due to the velocity magnitudes in the microchannels. The average velocity through each of the channels is shown in Figure 4-13. The chart indicates that the average flow rate per channel is relatively independent of manifold fin width. This is less accurate at the smaller flow rates, but at the larger flow rates there is little difference. The microchannel velocities are much faster in the microchannels closer to the end which, as was described previously, explains why the chip temperature moves closer to the center. The velocity profiles also explain why the offset occurs. They are the same for a given flow rate; just offset themselves which means that the temperature would simply be offset as well. The flow rates into the channels are the same for various manifold fin widths because the areas of the manifold flow channel and the microchannels do not vary.

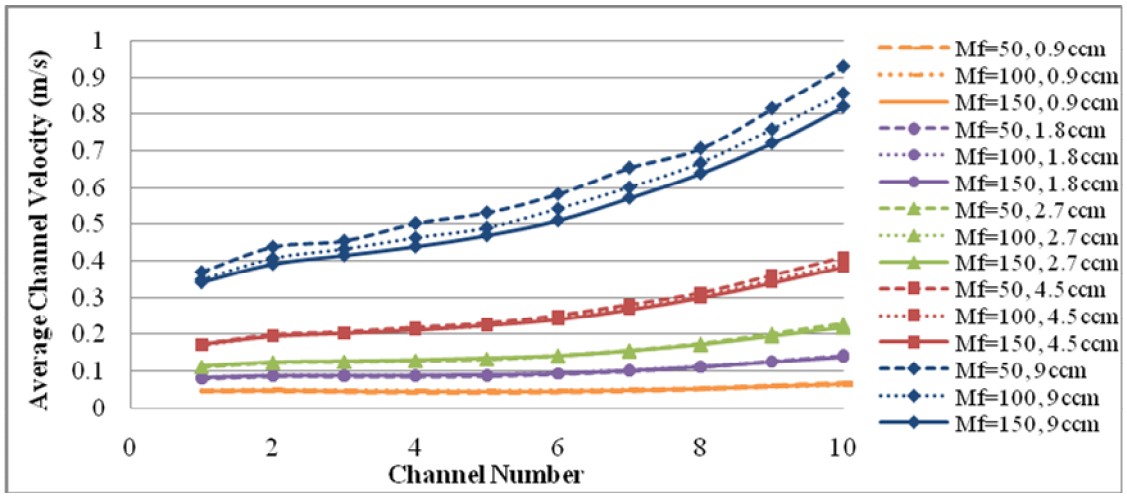


Figure 4-13: Average flow velocities through each microchannel for various flow rates (M_w = 200 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch}=10, q" = 400 W/cm^2)

It is also interesting to look at the microchannel pressure drops for various manifold fin widths and flow rates, which is plotted in Figure 4-14. This pressure drop is calculated by taking the average pressure in each channel and subtracting that from the inlet pressure.

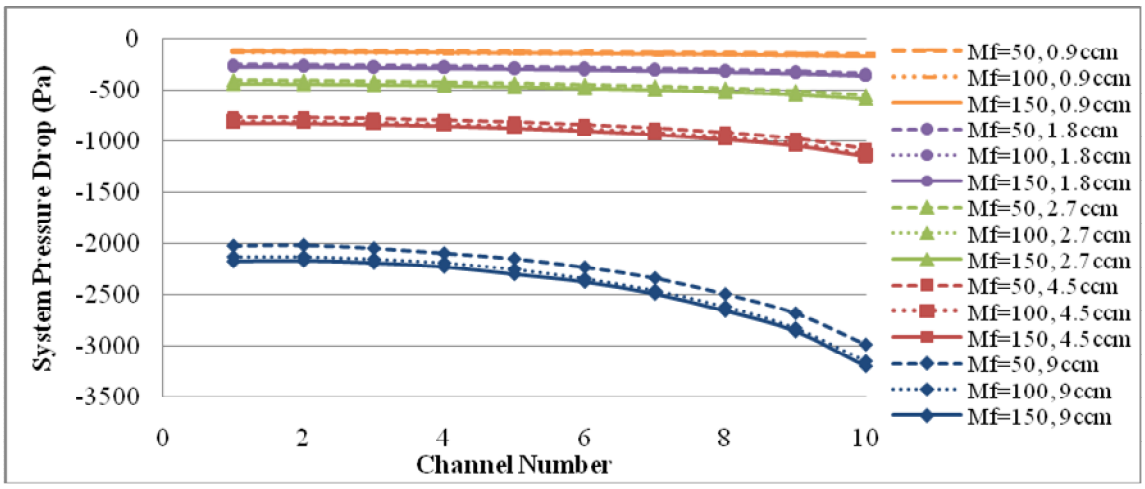


Figure 4-14: Average pressure drop through each microchannel for various flow rates (M_w = 200 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch}=10, q" = 400 W/cm^2)

In summary, after analyzing the effect of the manifold fin width on the performance it is desirable to minimize the M_f. When comparing varying M_f's for a constant system volumetric flow rate, the M_f has very little effect on the thermal performance but a significant effect on the overall system pressure drop. When comparing for a constant volumetric flow rate, there is little effect on the system pressure drop but the device temperature rises as the M_f increases. This effect is more pronounced at lower flow rates. Varying the M_f also has little effect on the heating across the chips surface. For a given volumetric flow rate, the temperature distribution on the chip surface remains the same independent of manifold height, it is simply offset by a certain temperature. Therefore, as M_f is increased for a given flow rate, the location of the hottest spot on the chip and the magnitude of chip non-uniformity remains the same. The hot spot becomes more centralized for all M_f's as the flow rate is increased due to the velocity distribution. The velocity distribution is also relatively independent of the M_f. In conclusions, it is desirable to minimize the M_f in all designs to the extent permitted by manufacturable and structural limits.

4.3 Effect of Varying Manifold Channel Width (M_w) on Performance

A series of models was also run varying the manifold channel width (M_w) to assess its effect on the performance, a list of which is shown in Table 4-4. The manifold channel fin width and manifold height were both constant at 50 μm and 750 μm, respectively. But the manifold width varied between 100, 200, 400 and 600 μm. The microchannel dimensions were also constant at m_w = 100 μm, m_f = 100 μm and m_h = 150 μm. Each geometric condition was modeled at a variety of inlet flow rates.

Table 4-4: List of models and their parameters for assessing the effect of M_w on performance.

m_w (µm)	m_f (µm)	M_h (µm)	M_w (µm)	M_f (µm)	m_h (µm)	Q (mL/min)	v_{in} (m/s)	$v_{microchannel}$ (m/s)	Q_{system} (mL/(min*µm))	N_{ch}
100	100	750	100	50	150	0.45	0.1	0.05	0.003	10
100	100	750	200	50	150	0.9	0.1	0.1	0.0036	10
100	100	750	400	50	150	1.8	0.1	0.2	0.004	10
100	100	750	600	50	150	2.7	0.1	0.3	0.004	10
100	100	750	100	50	150	2.438	0.542	0.271	0.016	10
100	100	750	200	50	150	4.875	0.542	0.542	0.020	10
100	100	750	400	50	150	9.750	0.542	1.083	0.022	10
100	100	750	600	50	150	14.625	0.542	1.625	0.023	10
100	100	750	100	50	150	3.375	0.75	0.375	0.0225	10
100	100	750	200	50	150	5.625	0.625	0.625	0.0225	10
100	100	750	400	50	150	10.125	0.5625	1.125	0.0225	10
100	100	750	600	50	150	14.625	0.542	1.625	0.0225	10
100	100	750	100	50	150	4.5	1	0.5	0.03	10
100	100	750	200	50	150	9	1	1	0.036	10
100	100	750	400	50	150	18	1	2	0.04	10
100	100	750	600	50	150	27	1	3	0.042	10
100	100	750	100	50	150	2.7	0.6	0.3	0.018	10
100	100	750	200	50	150	2.7	0.3	0.3	0.0108	10
100	100	750	400	50	150	2.7	0.15	0.3	0.006	10
100	100	750	600	50	150	2.7	0.1	0.3	0.004	10

4.3.1 Effect of System Volumetric Flow Rate on Varying M_w Performance

A plot of the tradeoff between the system pressure drop and the thermal performance versus the system volumetric flow rate for the models run is shown in Figure 4-15. A power curve has been fit to the chip temperature data to show that as the manifold channel width increases, so does the average chip temperature. In this case, as is typical, the temperature increases drastically for slower volumetric flow rates. Significantly increasing the volumetric flow rate causes a significant increase in pressure drop for a minimal decrease in device temperature. Therefore, a system volumetric flow rate of around 0.02 mL/(min*µm) seems to be a reasonable flow rate. For a system volumetric flow rate of 0.0225 mL/(min*µm), when the M_w = 100 µm, the chip temperature is 36.9 °C and when the M_w = 600 µm, the chip temperature is 44.9 °C, which is just under a 20% increase in average chip temperature and an 8 °C increase in

temperature. For lower flow rates, this difference would be much larger and at higher flow rates, the thermal performance would be more similar.

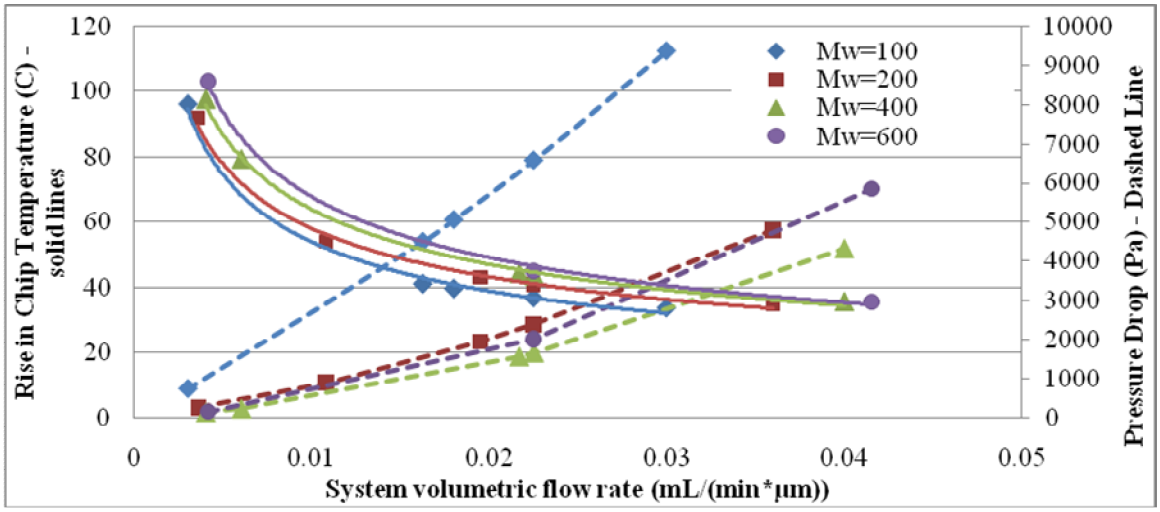


Figure 4-15: Plot depicting the tradeoff between the system pressure drop and the thermal performance as a function of the system volumetric flow rate for various manifold fin widths (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

When looking how the pressure drop relates to an increasing manifold channel width, it is interesting to see that as the manifold width increases, the pressure drop at first decreases but after a certain point it starts to increase again, indicating an optimum manifold width. To more clearly show this minimum point, a plot has been made to show both the rise in chip temperature and overall pressure drop as a function of the manifold channel width for a system volumetric flow rate of 0.0225 mL/(min*µm). This plot is shown in Figure 4-16. Clearly there is a minimum in the pressure drop curve around 400 µm. Also, as the manifold width increases, the rise in chip temperature begins to level off such that increasing the manifold width further would have less of an impact on further increasing the chip temperature.

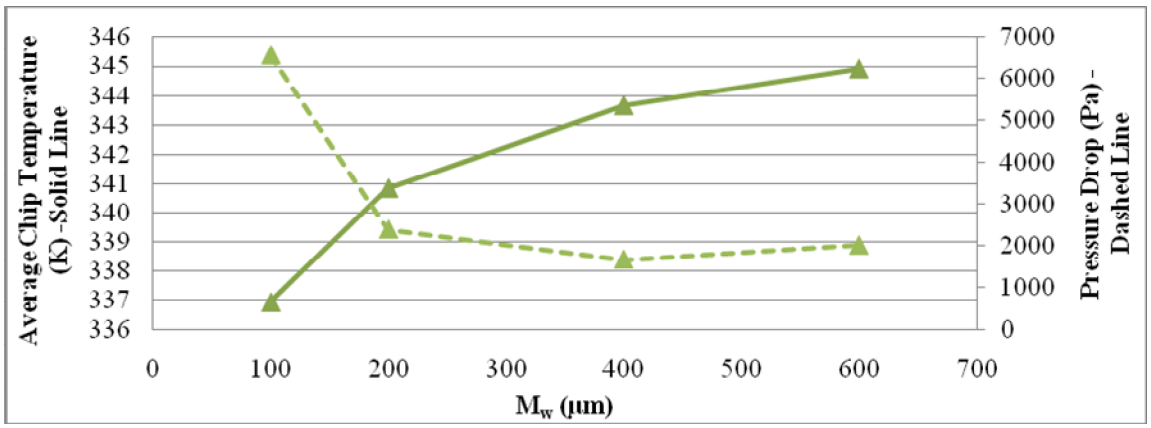


Figure 4-16: Plot showing the tradeoff between the thermal performance and the system pressure drop for various manifold widths at 0.0225 mL/min*µm (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

It is interesting to understand why this pressure drop minimum occurs for a varying M_w. Therefore, using the Hagen-Poiseuille pressure drop equation previously discussed in Section 3.2, a plot of the modeled versus calculated pressure drops are shown in Figure 4-17. It is clear that both the calculated and the modeled results have a similar trend indicating that there is a manifold width such that the pressure drop is minimized for a given system volumetric flow rate. Manifold widths less than this minimum causes the pressure drop to increase substantially and manifold widths greater than this minimum have a much less drastic increase in pressure drop. Therefore, if it is desirable to minimize pressure drop, then when designing for the manifold width it is probably most advisable to design for a manifold channel width slightly larger than the optimum. This allows the designer to be in a region where it is not likely for the pressure drop to have the potential to increase substantially.

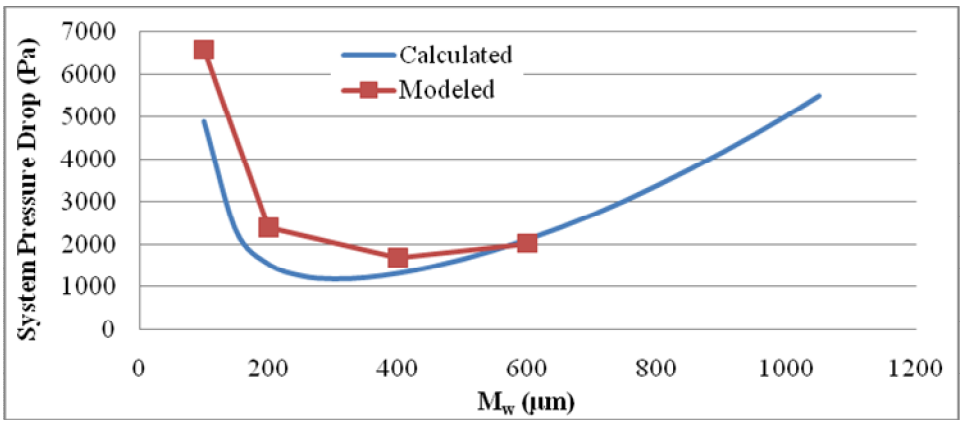


Figure 4-17: Plot showing the relationship between the modeled and the calculated system pressure drops at 0.0225 ccm/µm for various manifold channel widths (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

Figure 4-18 takes a closer look at why this minimum occurs in the pressure drop plot. This plot has divided the total analytical pressure drop into portions from both the manifold and the microchannels. For manifold widths less than the optimum, the pressure drop in the manifold dominates due to the fact that the manifold is very narrow and thus has a very large pressure drop. For manifold widths larger than the optimum, the pressure drop in the microchannels starts to dominate. This is because as the M_w increases, so does both the microchannel length and velocity through the microchannel, both of which cause an increase in the microchannel pressure drop. It has already been established in Section 3.2.3 that the microchannel portion over estimates when the manifold width is large. Therefore, this explains why the calculated trend has a larger slope on the right side of the optimum than appears for the modeling results.

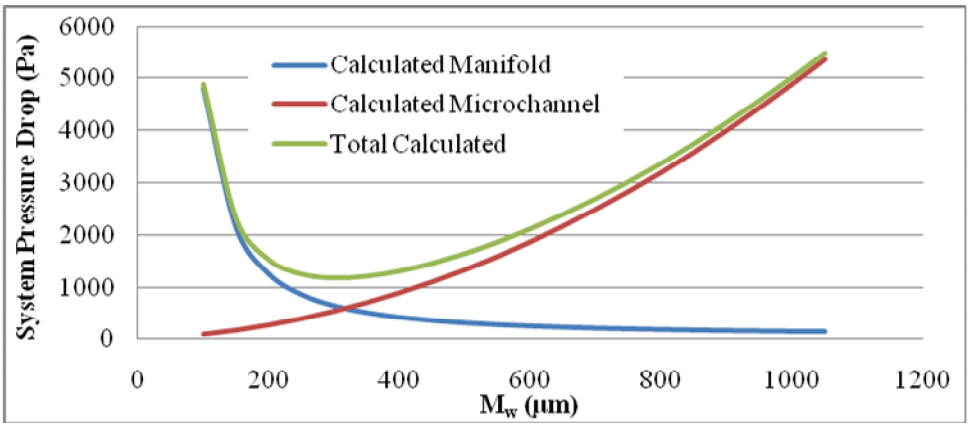


Figure 4-18: Plot showing a breakdown of the total analytical system pressure drop as a function of the manifold portion and the microchannel portion (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2, Q_{system} = 0.0225 mL/(min*µm))

A look at the pressure drops in the channels can be seen in Figure 4-19. This depicts this Y-Z cut through the center of the fifth channel, which is located near the middle of the device. A low pressure region can be found at the corner of the interior 90 degree bends which is due to the separated flow region. A higher pressure region can be seen on the upper right corner of each of the four conditions which is due to the stagnation region found at this location.

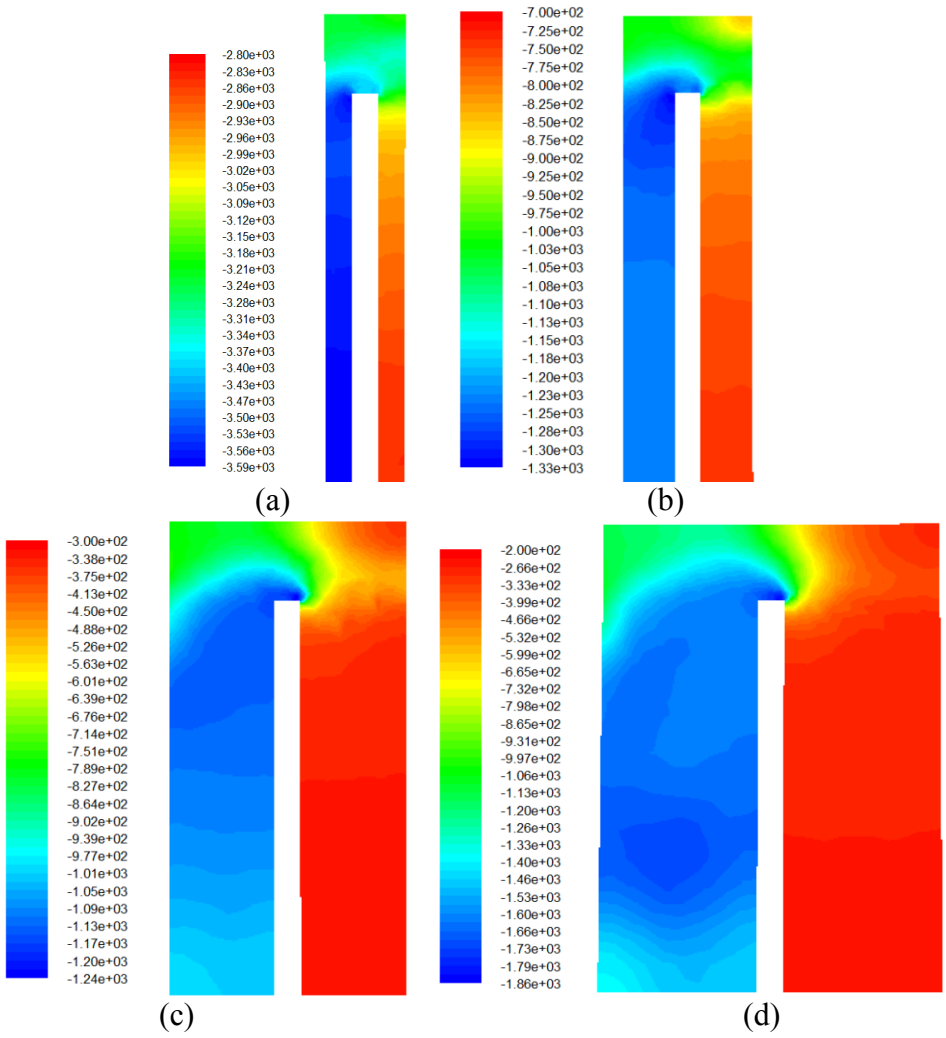


Figure 4-19: Pressure drop profiles through the Y-Z cut through the center of the fifth channel for (a) M_w = 100 µm (b) M_w = 200 µm (c) M_w = 400 µm (d) M_w = 600 µm (M_h = 750 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, Q_{system} = 0.0225 mL/(min*µm)). Units are in Pa.

The effect of the individual channel flow rates on the chip temperature profile is shown in Figure 4-20. For manifold widths greater than 100 µm, the velocity gradients are similar with about a 0.3 m/s difference in velocity from the first to the last channel. This indicates that their chip temperature profiles will be similar as is the case from

Figure 4-20b. When the manifold becomes extremely thin, the velocity profiles change slightly as was discussed in Section 3.4.3.

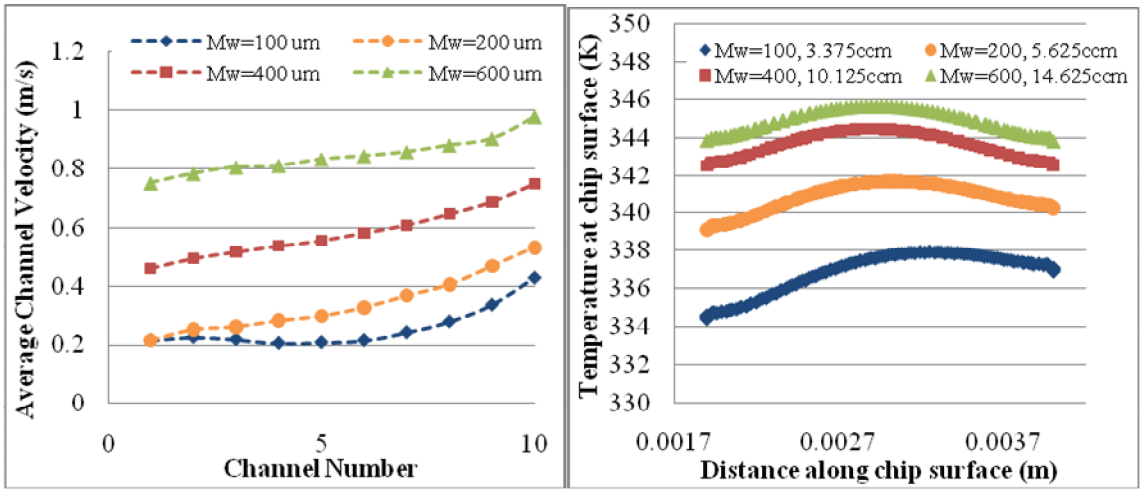


Figure 4-20: Plots at various manifold widths showing the (a) velocity magnitudes through the center cuts of each channel (b) chip temperature profile at the center cut of the chip (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2, Q_{system} = 0.0225 mL/(min*µm))

As was shown in Figure 4-20, even though the velocities through the microchannels are increasing, the device temperature is also rising. The images in Figure 4-21 and Figure 4-22 give a closer look as to why this occurs. Figure 4-21 shows the thermal profiles through the fifth channel Y-Z cut for various manifold widths with a close up on the microchannel fluidic portion. The fluid near the chip is clearly hotter for the larger manifold widths causing the chip temperature to be higher.

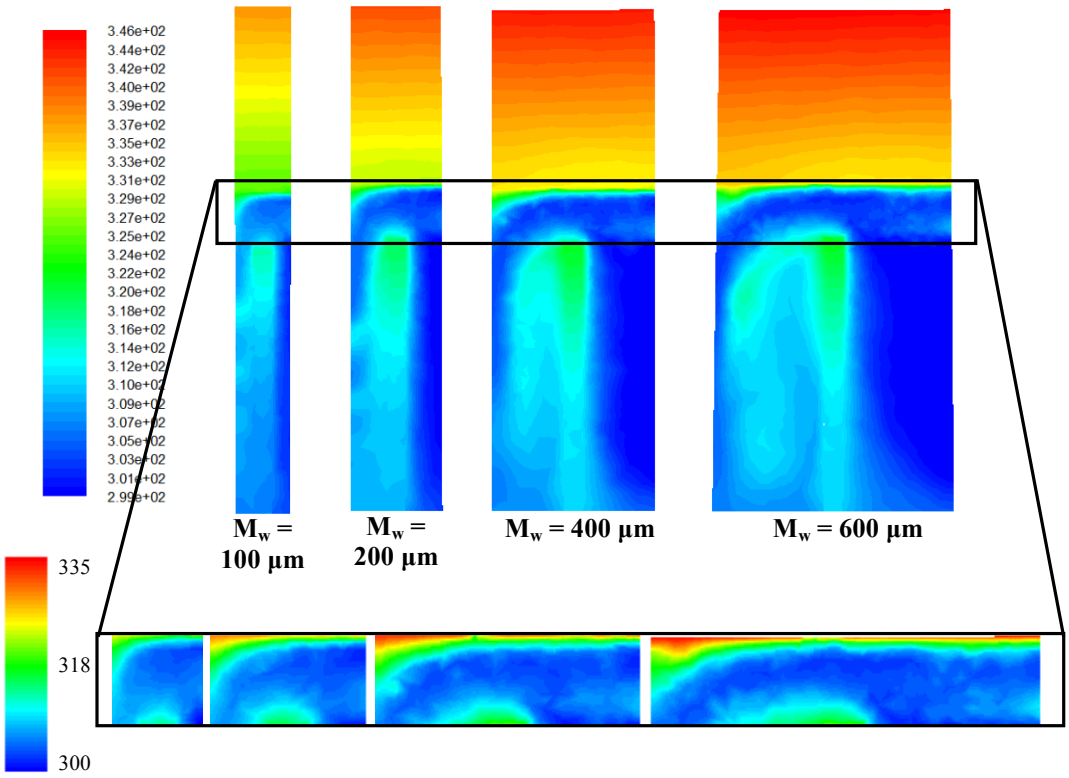


Figure 4-21: Thermal profiles through the Y-Z cut through the center of the fifth channel for various manifold widths (M_h = 750 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, Q_{system} = 0.0225 mL/(min*µm)). Units are in degrees Kelvin.

An explanation as to why the fluid is hotter under the chip for the wider manifolds is given through the velocity contours in Figure 4-22. The figure indicates a stagnation region in the upper right corner of each velocity contour plot. As the manifold width increases, so does this stagnation region. This stagnation region inhibits heat transfer in these locations, thus causing the device temperature to increase as a result.

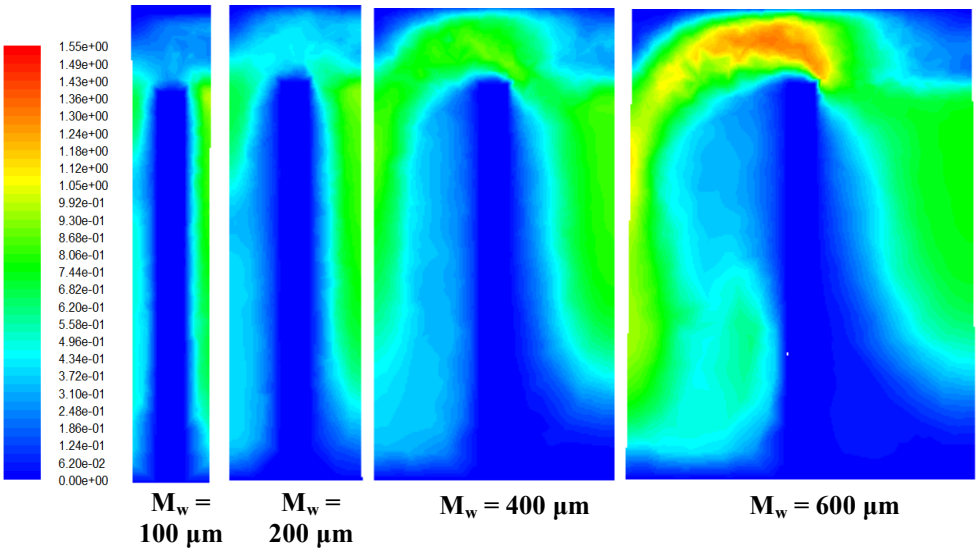


Figure 4-22: Velocity profiles through the Y-Z cut through the center of the fifth channel for various manifold widths (M_h = 750 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, Q_{system} = 0.0225 mL/(min*µm)). Units are in m/s.

For a constant system volumetric flow rate, as the M_w increases, so does the average rise in chip temperature. This is due to a stagnation region that forms in the microchannel above the center of the manifold channel which increases with increasing manifold width. But as the M_w increases, the rise in chip temperature begins to level off. But it is more complicated for the pressure drop. In terms of pressure drop, there is as optimum manifold width that minimizes the system pressure drop and it was shown that designing for a manifold width slightly larger than the optimum allows for the least variation in performance. The minimum occurs because of the tradeoff between the pressure drop in the manifold and the microchannel. At smaller manifold widths, the pressure drop in the manifold dominates and at larger manifold widths, the pressure drop in the microchannel dominates. Therefore, determining the correct manifold width for a given system will be heavily dependent on the design requirements.

4.3.2 Effect of Volumetric Flow Rate on Varying M_w Performance

Another case to explore is when the inlet flow rate is constant, of which a plot of the tradeoff between thermal performance and pressure drop is shown in Figure 4-23. The plot shows that at the same inlet volumetric flow rate, the chip temperature rises substantially and the pressure drop decreases substantially when the manifold width is increased. Therefore, since both the thermal performance and pressure drop are significantly affected by varying the manifold width, it would be difficult to determine an optimum operating parameter for varying M_w. The manifold width would be based on the design parameters.

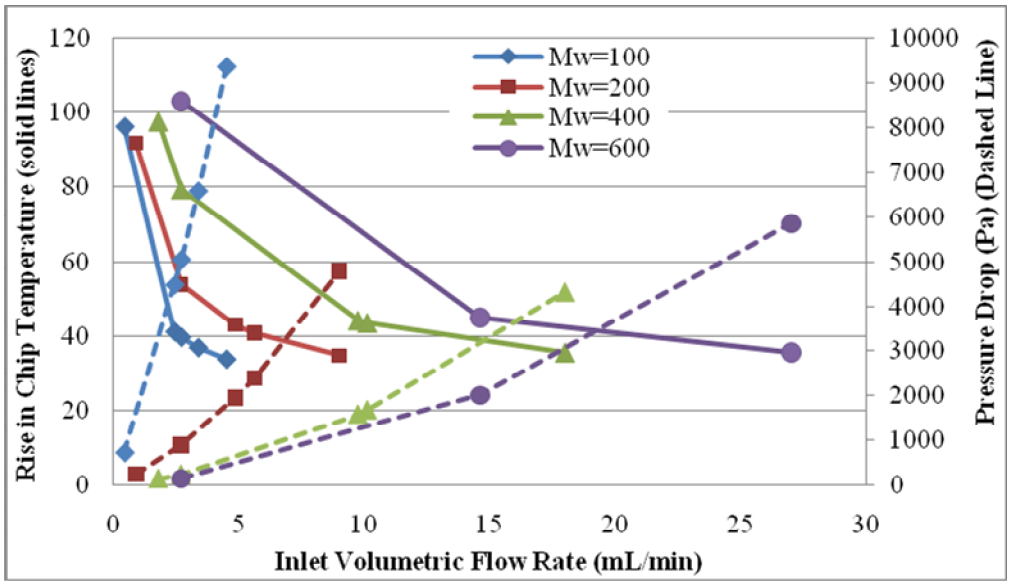


Figure 4-23: Plot depicting the tradeoff between the system pressure drop and the thermal performance as a function of the inlet volumetric flow rate for various manifold widths (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

A closer look at the effect of manifold width at a single volumetric flow rate, 2.7 mL/min, is discussed. Figure 4-24 shows how varying the manifold width affects both

the chip surface temperature and the pressure drop. Clearly, as the M_w increases, the chip surface temperature increases almost linearly and the pressure drop decreases exponentially. Therefore, it could be deduced that an optimum manifold width could be found. It would be located where there is little additional improvement in the pressure drop of the device, around 300-400 µm in this case.

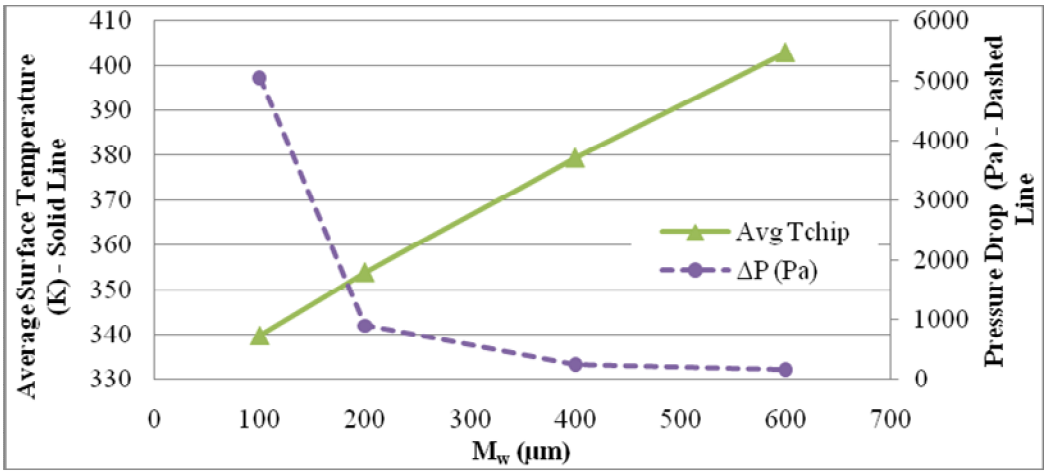


Figure 4-24: Plot showing the tradeoff between the thermal performance and the system pressure drop for various manifold widths at flow rates of 2.7 mL/min (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

It is expected that by increasing the manifold width, that the variation across the chip surface would vary. This is indeed the case as can be seen in Figure 4-25 and Figure 4-26. Figure 4-25 is a plot of the chip surface temperature contours for various manifold widths. It is clear that as the manifold width increases, the chip surface temperature rises in the z-direction along the chip.

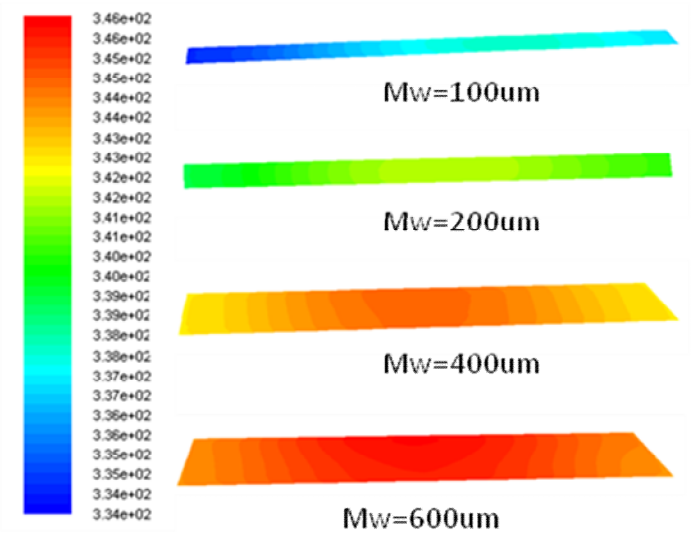


Figure 4-25: Chip surface temperature contour plots for various manifold widths at flow rates of 2.7 mL/min (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2). Units are in degrees Kelvin.

It is interesting to see how much of an effect this rise in chip temperature has on the overall chip uniformity. Therefore, Figure 4-26 plots the average, maximum, minimum and difference in temperature across the surface of the chip. Clearly, even though the chip temperatures are increasing linearly with increasing manifold widths, the difference in chip temperature is leveling out. Thus, the uniformity of the chip is not significantly affected by increasing the manifold width.

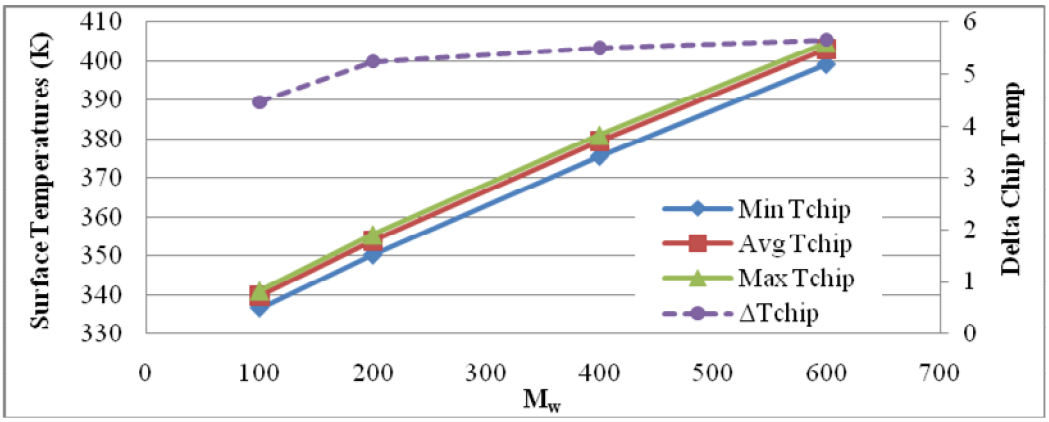


Figure 4-26: Plot showing the maximum, minimum and average chip temperatures along with difference in chip temperature for various manifold widths at flow rates of 2.7 ccm (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2)

Figure 4-27 shows the velocity profiles for each microchannel for various manifold fin widths along with the chip temperature profile when the volumetric flow rate is 2.7 mL/min. Clearly, as the manifold width increases, the chip temperature rises dramatically. For a M_w = 100 µm, the device is around 340 K and when M_w = 600 µm, the device temperature is around 405 K, 65 degrees higher. The reason for this was discussed in the previous section, Section 4.3.1. The velocities through each channel increase in non-uniformity as the manifold width decreases. This occurs for the same reason that this happens when the manifold height is increased, as was discussed in Section 4.1. The velocity through each manifold channel increases with decreasing channel width causing the flow to be higher in the last channels.

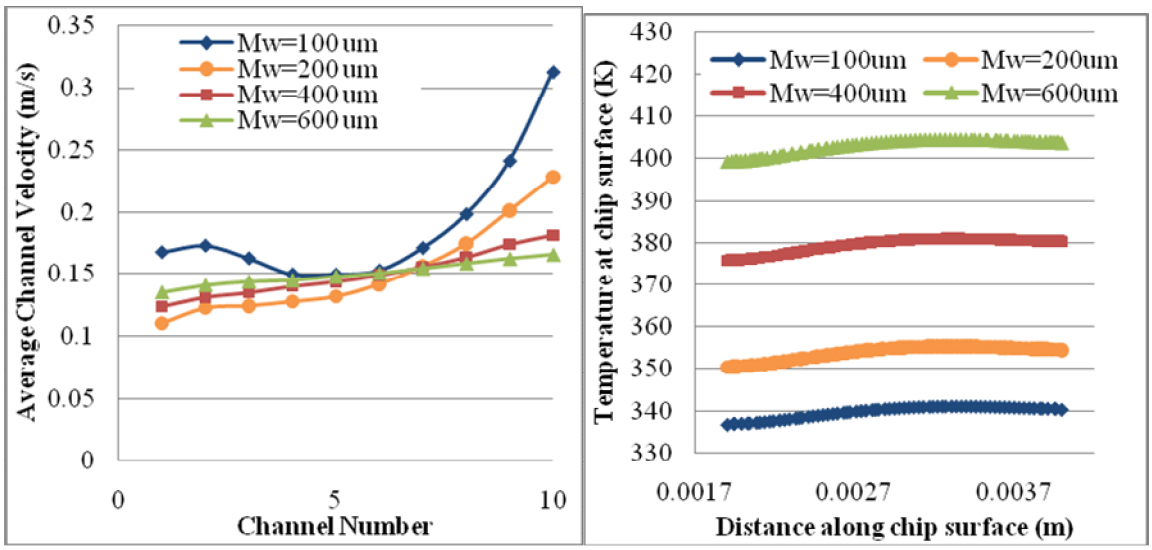


Figure 4-27: Plots at various manifold widths showing the (a) velocity magnitudes through the center cuts of each channel (b) chip temperature profile at the center cut of the chip (M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10, q" = 400 W/cm^2, Q = 2.7 mL/min)

For a constant volumetric flow rate, the chip temperature rises substantially and the pressure drop decreases substantially when the manifold width is increased. Therefore, since both the thermal performance and pressure drop are significantly affected by varying the manifold width, it would be difficult to determine an optimum operating parameter for varying M_w. Additionally, as the M_w increases, so does the chip non-uniformity, but this levels out. The manifold width would be based on the design parameters.

4.4 Varying the Microchannel Dimensions

Section 4.1 previously discussed the effect the manifold height had on the performance but it also touched on the effect of varying the microchannel dimensions. This section is going to elaborate on how varying the microchannel dimensions effects

both the thermal performance and the overall system pressure drop. In all cases, the manifold dimensions were constant (M_w = 200 μm, M_f = 50 μm, and M_h = 750 μm) and the microchannel height was a constant 150 μm. The models were run for four different microchannel dimensions:

- m_f = 100 μm, m_w = 100 μm, N_{ch} = 10
- m_f = 100 μm, m_w = 50 μm, N_{ch} = 13
- m_f = 50 μm, m_w = 100 μm, N_{ch} = 13
- m_f = 50 μm, m_w = 50 μm, N_{ch} = 19

The number of microchannels was varied for each of the four microchannel dimensions to allow the number of channels to cool a 2 mm chip. It was assumed that the microchannels would fill 1.9 mm of the 2 mm chip to allow room for bonding around the outside of the channels and to avoid fluid leaking. For comparison, the volume flow rate was also held constant at 5.625 mL/min which is equivalent to a system volumetric flow rate of 0.0225 mL/(min*μm). The channels in this experiment are a fair comparison to each other because they have the same volumetric inlet flow condition, the same manifold channel dimensions, and the same linear area for which they cool.

Section 4.1 above shows the pressure drop versus thermal performance plots for each of the above microchannel dimensions. They will not be presented here again but portions of their data will be analyzed in this section. This section will first look into the effect the m_w and m_f have on the pressure drop for a constant flow rate, then it will look into their effect on the thermal performance at a constant flow rate, then it will sum up with a look at their effect at various volumetric flow rates.

Using the pressure drop equation shown previously in Section 3.2, the pressure drops have been calculated for each of the four microchannel geometries. A comparison of the numerical and analytical pressure drops is shown in Figure 4-28. While the magnitudes of the pressures drops vary quite a bit from the calculated to the modeled results, the trend is the same. In both cases it shows that the highest pressure drop is for the m_w = 50 µm, m_f = 100 µm microchannels. This at first may seem a little counter-intuitive because it would seem as if the largest pressure drop should be for the smallest channels (m_w = 50 µm, m_f = 50 µm). But the pressure drop depends on both the microchannel dimensions as well as the flow velocity through the channels which explains why this occurs.

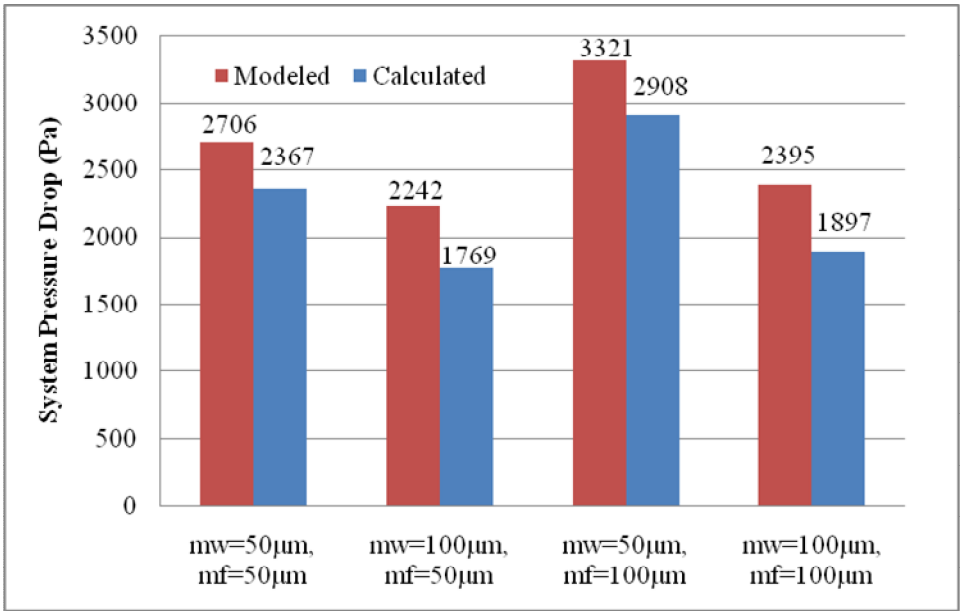
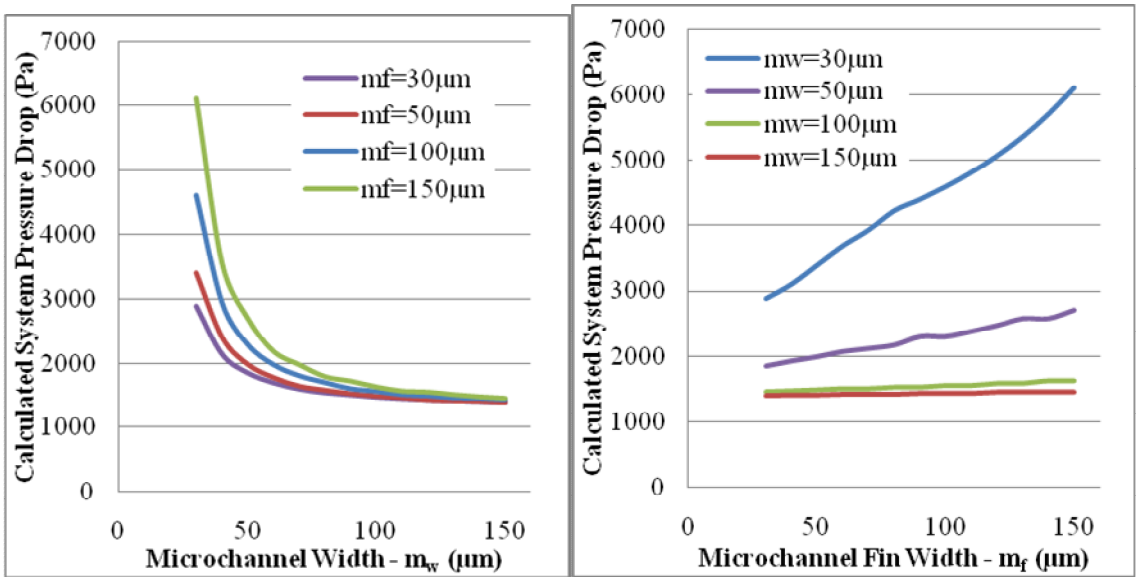


Figure 4-28: Chart showing the modeled versus analytic pressure drops for various microchannel dimensions (Q = 5.625 mL/min, q" = 400 W/m^2, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_h = 150 µm, L_{chip} = 2 mm)

Figure 4-28 indicates that the pressure drop equations give a fair approximation to the effect of the manifold and microchannels on the performance. Therefore, the equations are used to show the effect of varying both the width and spacing of the microchannels, the results of which are shown in Figure 4-29. Figure 4-29a shows the effect of the m_w on the pressure drop. The difference curves represent different microchannel fin widths. The charts indicate that there is an optimum m_w at which you get minimal enhancement for your pressure drop. Figure 4-29b shows the effect the m_f has on the pressure drop indicating almost a linear relationship. The different curves represent different microchannel widths showing a higher slope for the smaller widths which equate to the exponential trend of the first chart.



(a) (b)

Figure 4-29: Calculated system pressure drops for varying independently the (a) m_w and (b) m_f dimensions (Q = 5.625 mL/min, q" = 400 W/cm^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_h = 150 µm, L_{chip} = 2 mm)

Therefore, in terms of minimizing the pressure drop, optimum microchannel dimensions can be approximated utilizing the simplified pressure drop equations. The m_f should be minimized and the m_w should be calculated such that increasing it would have minimal improvement on improving the overall system pressure drop. Figure 4-30 shows the pressure gradients for each of the four geometries that were modeled.

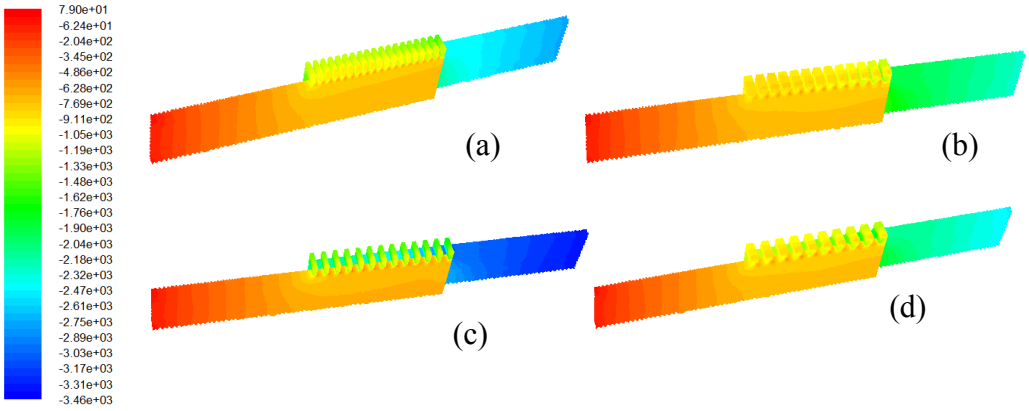


Figure 4-30: Pressure gradient for various microchannels (a) m_w = 50 µm, m_f = 50 µm (b) m_w = 100 µm, m_f = 50 µm (c) m_w = 50 µm, m_f = 100 µm (d) m_w = 100 µm, m_f = 100 µm (Q = 5.625 mL/min, q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

Figure 4-31 shows the average chip temperature rise for each of the four microchannel geometries. It is expected that the smaller microchannels will perform better than the wider microchannels; therefore, it is no surprise that the best performance is by the microchannels with m_w = 50 µm and m_f = 50 µm. But it is a little surprising that the m_w = 50 µm, m_f = 100 µm channels perform almost exactly the same thermally. It is also surprising that the m_w = 100 µm, m_f = 100 µm channels perform better thermally than the m_w = 50 µm, m_f = 100 µm channels. This is due to the fact that there is a larger

velocity through each of the m_w = 100 µm, m_f = 100 µm channels than through the m_w = 50 µm, m_f = 100 µm channels because there are fewer of them.

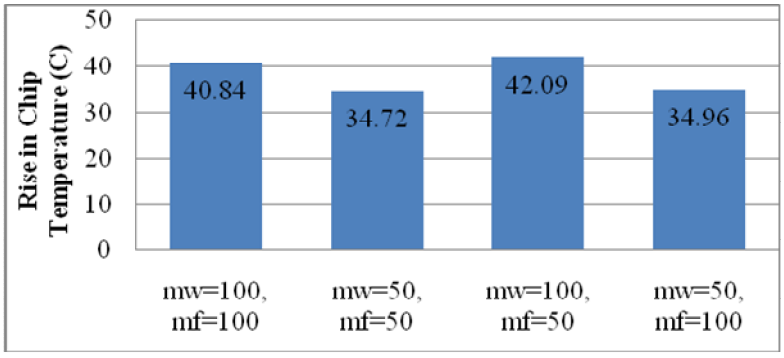


Figure 4-31: Plot showing the rise in chip temperature for various microchannels (Q = 5.625 mL/min, q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

A conclusion that can be formed from Figure 4-31 is that varying the m_w has a larger impact on the thermal performance than varying the m_f. This is clear because the microchannels that are 50 µm wide perform similarly whether the m_f is 50 or 100 µm and the same is true for the 100 µm wide microchannels. But when the m_w varies between 50 to 100 µm, there is about a 6 °C increase in chip temperature, a 17% increase.

The average flow through each channel is calculated by taking half the volumetric flow rate and dividing it by the total cross sectional area of the microchannel:

$$v_{microchannel} = \frac{0.5Q}{N_{ch} * m_w * m_h} \tag{4-2}$$

The average flow rate per microchannel is found for the model by simply averaging all the average velocities in each of the microchannels. The results are shown in Table 4-5 and illustrate that this calculation gives a very good agreement with at most 0.28 m/s difference, which is an 8% error. Similar results are seen for all models.

Table 4-5: The calculated and modeled pressure drops for the microchannels (Q = 5.625 mL/min, q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

m_w (µm)	m_f (µm)	N_{ch}	Avg. Chip Rise (C)	Calculated (m/s)	Average Modeled (m/s)	Min Modeled (m/s)	Max Modeled (m/s)	Max – Min (m/s)
100	100	10	40.84	0.313	0.341	0.216	0.532	0.316
50	50	19	34.72	0.329	0.327	0.218	0.473	0.255
100	50	13	42.09	0.240	0.259	0.129	0.490	0.361
50	100	13	34.96	0.481	0.480	0.393	0.585	0.192

A graph of the temperature profile across the chip surface for each of the four geometries is shown in Figure 4-32a, with the corresponding microchannel velocities shown in Figure 4-32b. As can be seen in Table 4-5 and this figure, there is a large velocity difference between microchannels, between 1.5 X (m_w = 50 µm, m_f = 100 µm) and 3.8 X (m_w = 100 µm, m_f = 50 µm) increase from the first to last channel.

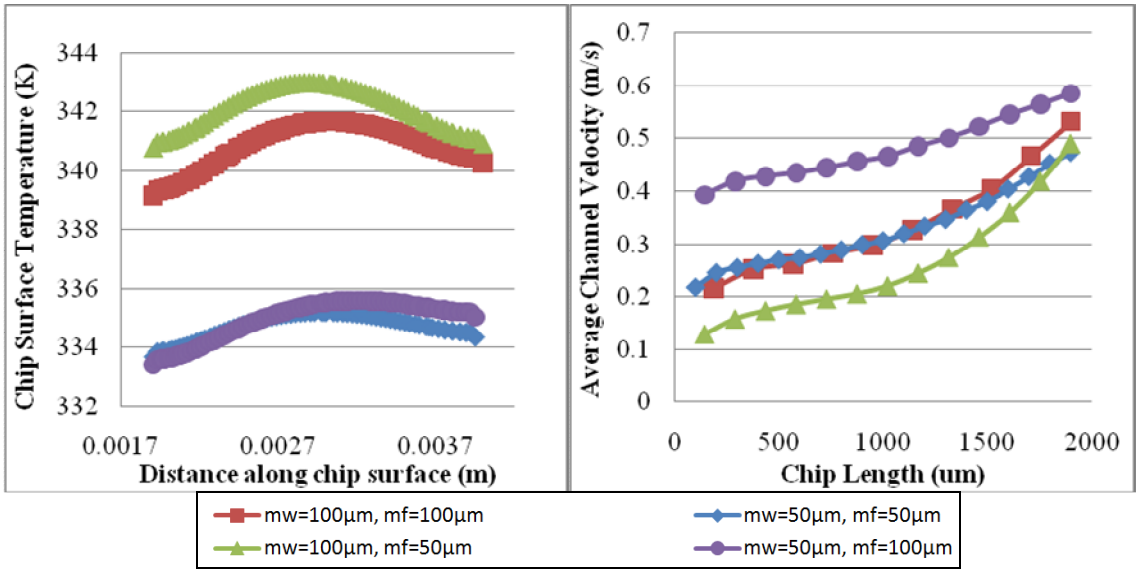


Figure 4-32: Plots of various microchannel dimensions showing the (a) surface chip temperature profile (b) velocity magnitudes through the center cuts of each microchannel (Q = 5.625 mL/min, q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

All of the previous data has been for a constant volumetric flow rate of 5.625 mL/min, but it is also interesting to look at how varying m_w and m_f affects the performance at other flow rates. Figure 4-33a, b, c and d show the effects at three different volumetric flow rates of average chip temperature, average system pressure drop, average rise in fluid temperature and the chip non-uniformity, respectively.

Figure 4-33a shows how the chip temperature decreases with increasing flow rate. Additionally it shows that the trend seen previously of the microchannel width dominating the thermal performance still holds at the various velocities. The same is true for the plots of pressure drops in Figure 4-33b where the trend is still the same in that the m_w = 50 μm, m_f = 100 μm has the highest pressure drop and m_w = 100 μm, m_f = 50 μm has the lowest pressure drop for all flow rates. It is interesting to note that the effect of pressure drop with flow rate is quite a bit larger than the thermal effect. For example, the pressure drop nearly doubles for each increase in flow rate whereas the average temperature decreases just a few degrees.

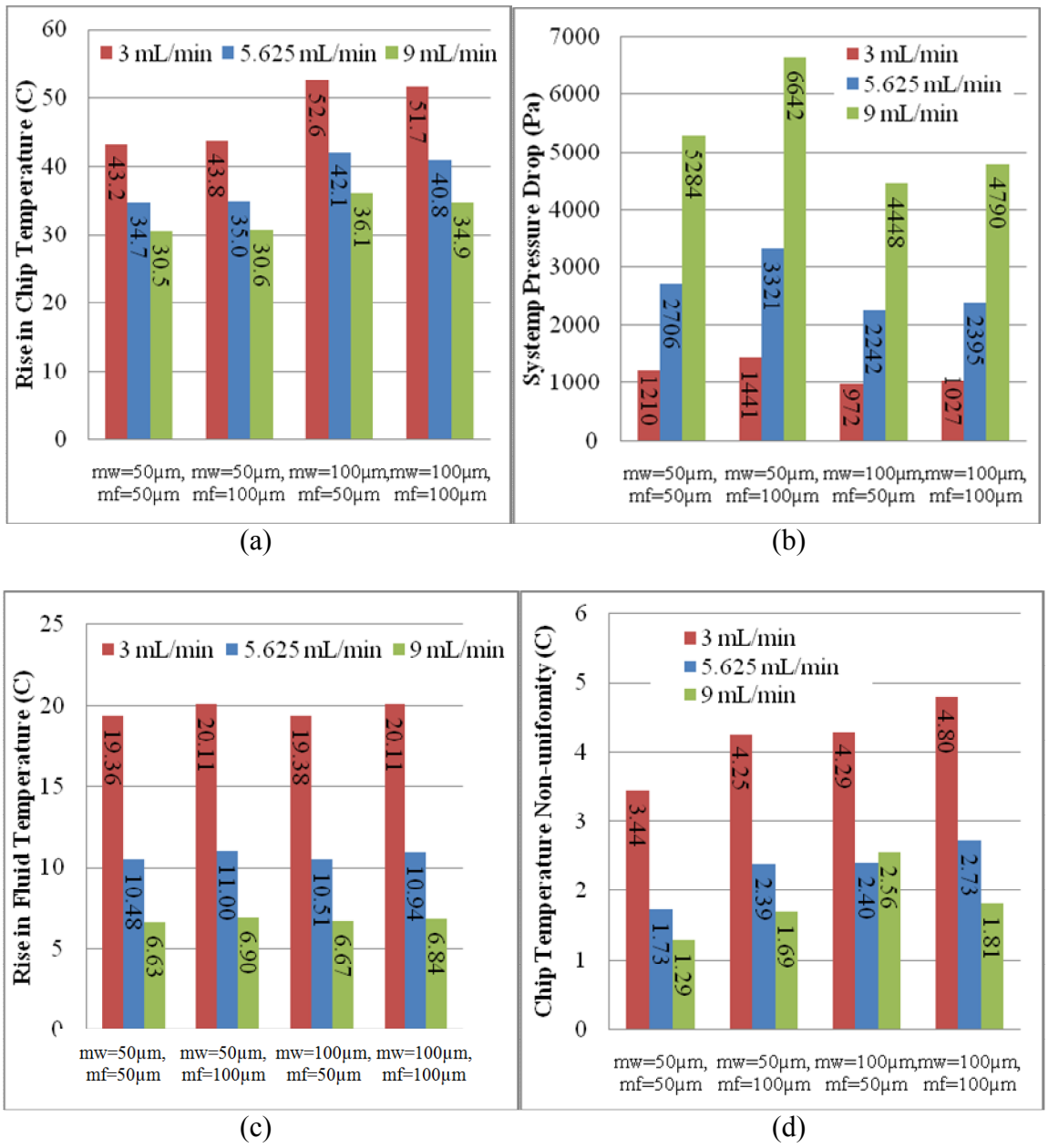


Figure 4-33: Plot showing the (a) average rise in chip temperature and (b) average system pressure drop (c) average rise in fluid temperature and (d) average chip temperature non-uniformity for various microchannel dimensions and flow rates (q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

Figure 4-33c shows the rise in fluid temperature for various microchannel velocities at three different flow rates. The rise in fluid temperature depends on the fin

width with a smaller fin heating up the fluid more than a wider fin. The non-uniformity of the chips surface is shown in Figure 4-33d indicating for the most part that it decreases as the velocity increases. Additionally, the m_w = 50 μm, m_f = 50 μm channels are the most uniform and the m_w = 100 μm, m_f = 100 μm channels are the least uniform.

Shown below in Figure 4-34, Figure 4-35, and Figure 4-36 are the cross sectional cuts of the devices showing the thermal profiles for 3 mL/min, 5.625 mL/min, and 9 mL/min, respectively. The figures show the complete center cut of each of the four microchannel geometries along with an expanded image of just the microchannel portion and a further expanded portion of just two of the center microchannels. The most notable points in all the images are the amount of heat transferred into the fluid along with the amount of heat transferred into the manifold. At lower flow rates both of these are much higher and at 3 mL/sec there is actually quite a bit of heat that makes its way into the manifold. At 9 mL/min, there is a large amount of fluid that is flowing through the microchannels that is not being heated at all.

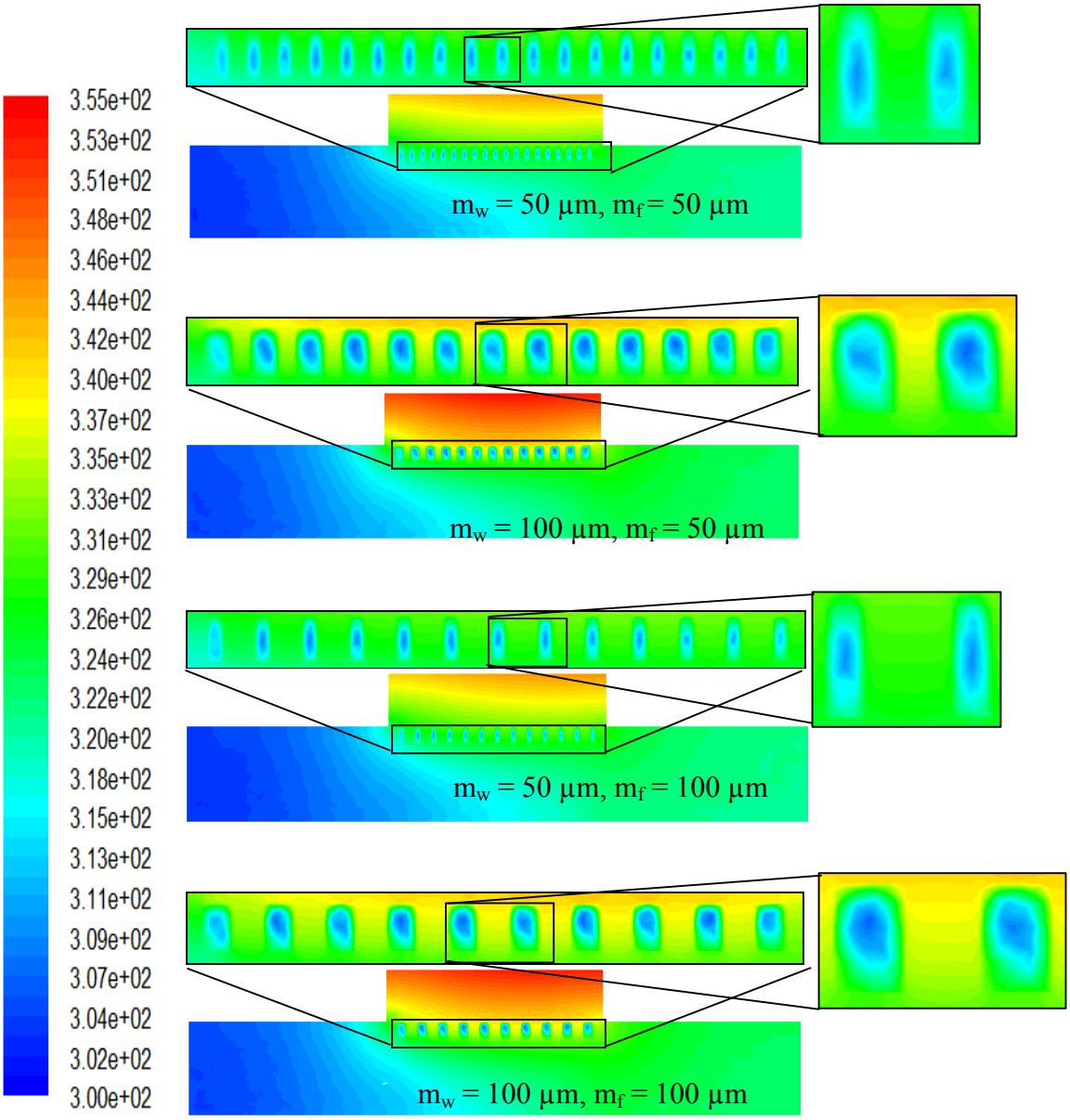


Figure 4-34: Thermal gradient plots for a volumetric flow rate of 3 mL/min for various microchannel geometries showing the center cut through the device, then a magnified image of all the microchannels, than another magnified image of just two of the microchannels to show how the heat is transferring into the fluid (q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

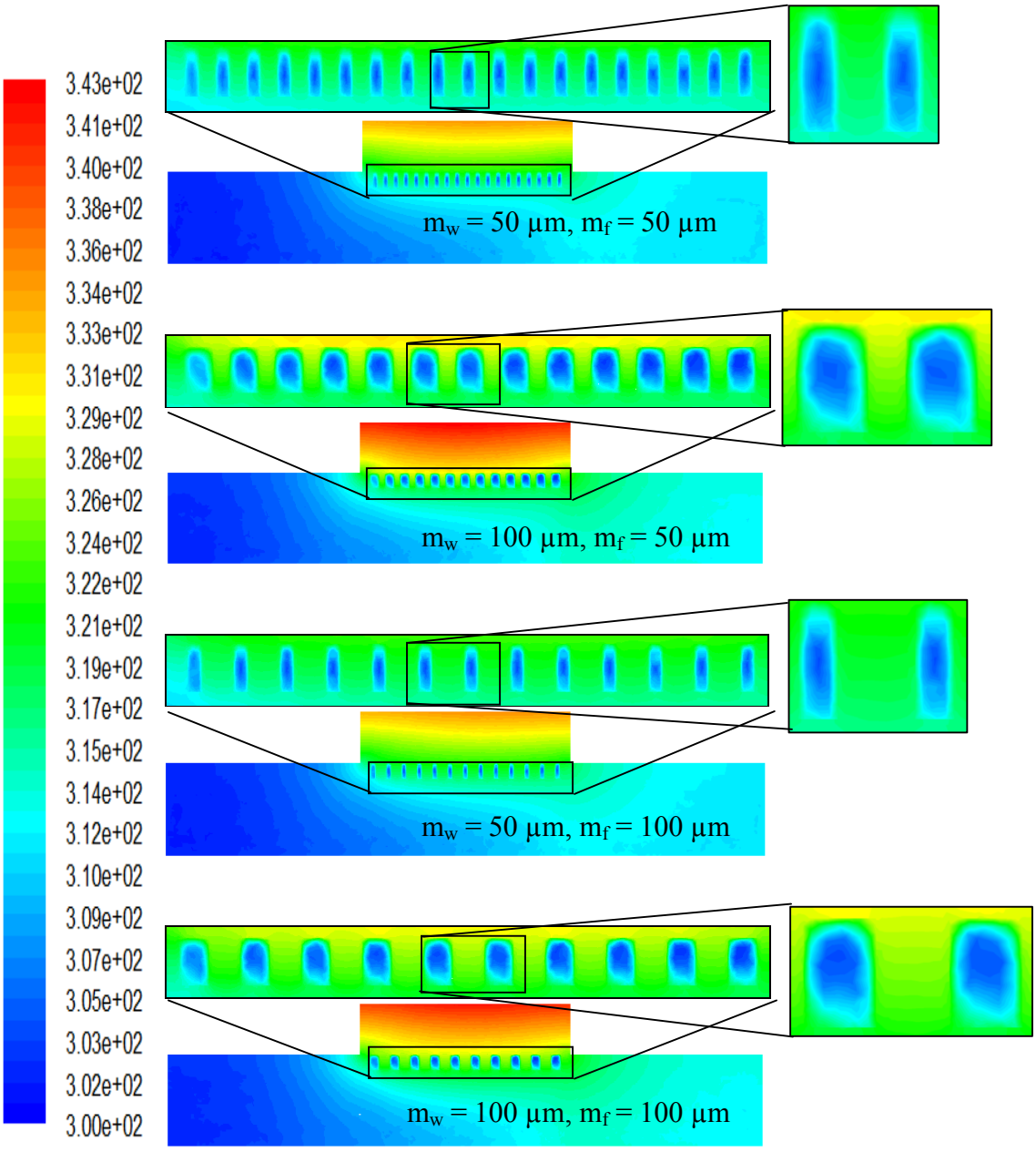


Figure 4-35: Thermal gradient plots for a volumetric flow rate of 5.625 mL/min for various microchannel geometries showing the center cut through the device, then a magnified image of all the microchannels, than another magnified image of just two of the microchannels to show how the heat is transferring into the fluid (q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

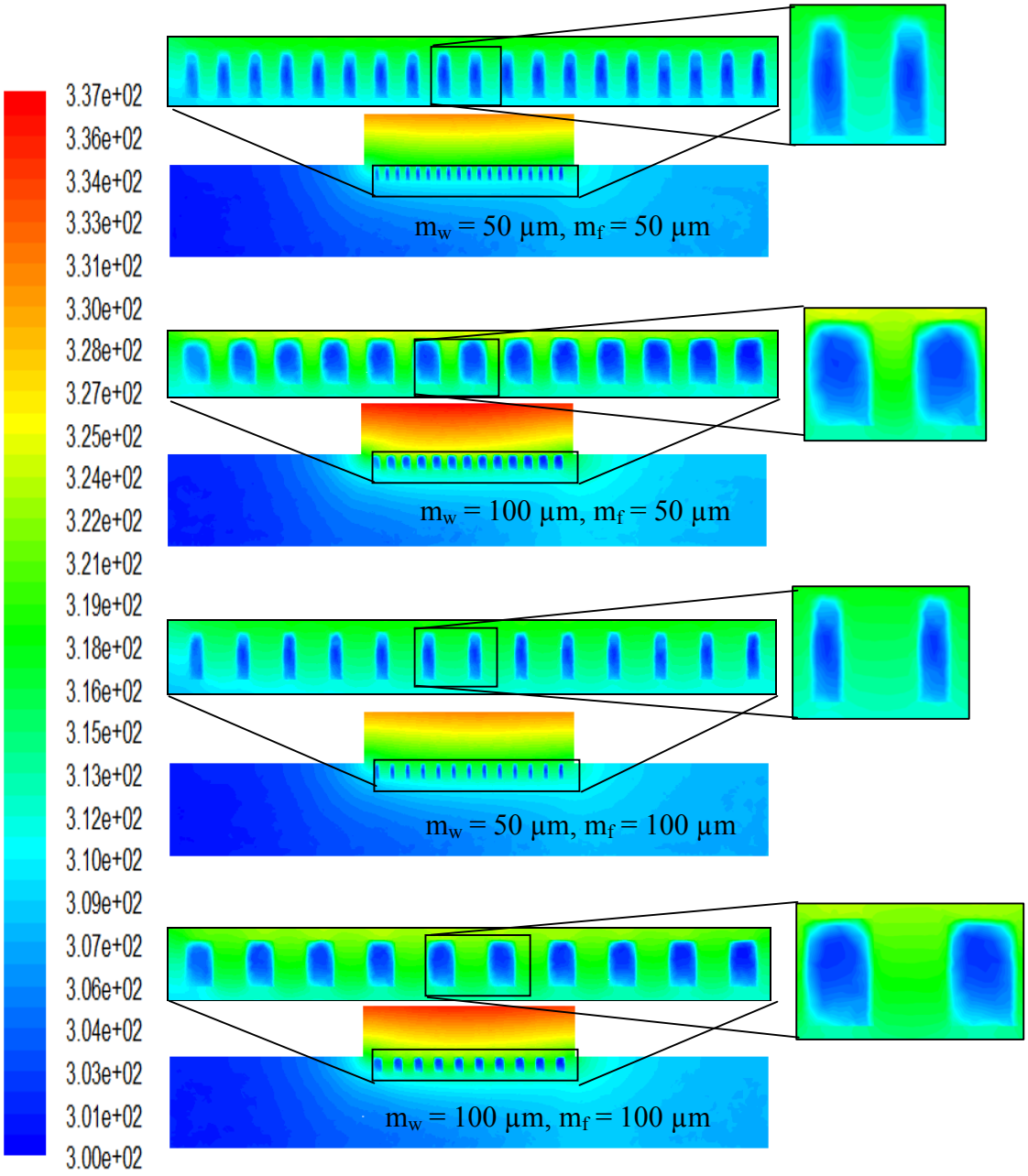


Figure 4-36: Thermal gradient plots for a volumetric flow rate of 9 mL/min for various microchannel geometries showing the center cut through the device, then a magnified image of all the microchannels, than another magnified image of just two of the microchannels to show how the heat is transferring into the fluid (q" = 400 W/m^2, m_h = 150 µm, M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, L_{chip} = 2 mm)

In conclusion, this section has investigated how varying the microchannel dimensions effects both the thermal performance and the overall system pressure drop. Four microchannel geometries were modeled with varying manifold fin and microchannel width dimensions. The results have shown that the microchannel width has a larger impact on the thermal performance than the microchannel fin width. It was also shown that at low flow rates, quite a bit of heat makes its way into the manifold and at high flow rates, most of the fluid flowing through the microchannels is not being heated at all. Additionally there was shown to be quite a large difference in flow rates between the microchannels with the velocity increasing down the channel.

It has been shown that while the magnitudes of the pressures drops vary quite a bit from the calculated to the modeled results, the trend is the same. Thus the numerical pressure drop equations have been shown to give a fair approximation of the trends of varying the microchannel dimensions on the pressure drop. The calculations have shown that there is an optimum microchannel width at which you get minimal pressure drop enhancement and the microchannel fin width should be minimized.

4.5 Varying the Number of Microchannels (N_{ch})

Since devices vary quite a bit in size, it is interesting to look at how the chip length affects the performance for a constant power density (i.e. constant heat flux). The number of microchannels (N_{ch}) will depend on the chip length (L_{chip}) according to:

$$N_{ch} = \frac{m_f + L_{chip}}{m_w + m_f} \tag{4-3}$$

The performance of the system was assessed in terms of both a constant volumetric flow rate and a constant flow rate per channel. Depending on the application,

one of these would probably be a better metric. A constant volumetric flow rate is interesting because it leaves the system the same such that there is the same volume of fluid entering the system independent of chip width. But it is also interesting to look at how the system performs when the flow rate through each channel is held constant such that it has similar thermal performance. This is logical because it is more likely larger chips will have larger flow rates and simply setting the flow rate the same would show the smaller chips to perform better thus giving a potentially unfair comparison.

4.5.1 Results for Constant Flow Rate per Microchannel

The first condition that was analyzed was where the flow velocity through each microchannel was constant while the number of channels was varied. In all cases the flow rate per channel was assumed to be 0.625 m/s, which was chosen to correspond to previously run models so as to minimize the number of additional models that must be run. The system volumetric flow rate was then calculated by a simple area calculation:

$$Q = \mathrm{v}_{microchannel} \times m_w \times m_h \times N_{ch} \tag{4-4}$$

In the equation, the flow rate per channel ($v_{microchannel}$) was set in every case to be 0.625 m/s. Table 4-6 shows the complete list of models that were run at $v_{microchannel} = 0.625$ m/s. The manifold channel dimensions were kept constant for each model (M_h = 750 μm, M_w = 200 μm, M_f= 50 μm). The number of channels varied from 2 to 20 channels for four different microchannel dimensions:

- m_w = 50 μm, m_f = 50 μm
- m_w = 50 μm, m_f = 100 μm
- m_w = 100 μm, m_f = 50 μm
- m_w = 100 μm, m_f = 100 μm

Table 4-6: Models run for the average flow rate per channel of 0.625 m/s

m_w (µm)	m_f (µm)	M_h (µm)	M_w (µm)	M_f (µm)	m_h (µm)	Q (mL/min)	v_{in} (m/s)	$v_{microch}$ (m/s)	Linear Vol. Flow rate (mL/(min*µm))	N_{ch}
50	50	750	200	50	150	0.5625	0.0625	0.625	0.00225	2
50	50	750	200	50	150	1.40625	0.15625	0.625	0.005625	5
50	50	750	200	50	150	2.8125	0.3125	0.625	0.01125	10
50	50	750	200	50	150	5.34375	0.59375	0.625	0.021375	19
50	100	750	200	50	150	0.5625	0.0625	0.625	0.00225	2
50	100	750	200	50	150	1.40625	0.15625	0.625	0.005625	5
50	100	750	200	50	150	2.8125	0.3125	0.625	0.01125	10
50	100	750	200	50	150	3.65625	0.40625	0.625	0.014625	13
100	50	750	200	50	150	1.125	0.125	0.625	0.0045	2
100	50	750	200	50	150	2.8125	0.3125	0.625	0.01125	5
100	50	750	200	50	150	5.625	0.625	0.625	0.0225	10
100	50	750	200	50	150	7.3125	0.8125	0.625	0.02925	13
100	50	750	200	50	150	8.4375	0.9375	0.625	0.03375	15
100	50	750	200	50	150	11.25	1.25	0.625	0.045	20
100	100	750	200	50	150	1.125	0.125	0.625	0.0045	2
100	100	750	200	50	150	2.8125	0.3125	0.625	0.01125	5
100	100	750	200	50	150	5.625	0.625	0.625	0.0225	10
100	100	750	200	50	150	8.4375	0.9375	0.625	0.03375	15
100	100	750	200	50	150	11.25	1.25	0.625	0.045	20

In order to compare the different microchannel dimensions to each other, it is interesting to look at the total length of the microchannels, which would equate to the length of the chip, and is calculated with the following equation:

$$L_{chip} = N_{ch} \times m_w + \left(N_{ch} - 1\right) \times m_f \tag{4-5}$$

Plotting the rise in chip temperature versus the system pressure drop is shown in Figure 4-37 as a function of the chip length for various microchannel dimensions. As the chip length increases, both the pressure drop and temperature increase. The pressure increases because of the additional length of the manifold channel. The temperature increases because of the additional heating of the fluid in the manifold. This plot also shows the effect of varying the microchannel dimensions, which was discussed in detail in Section 4.4.

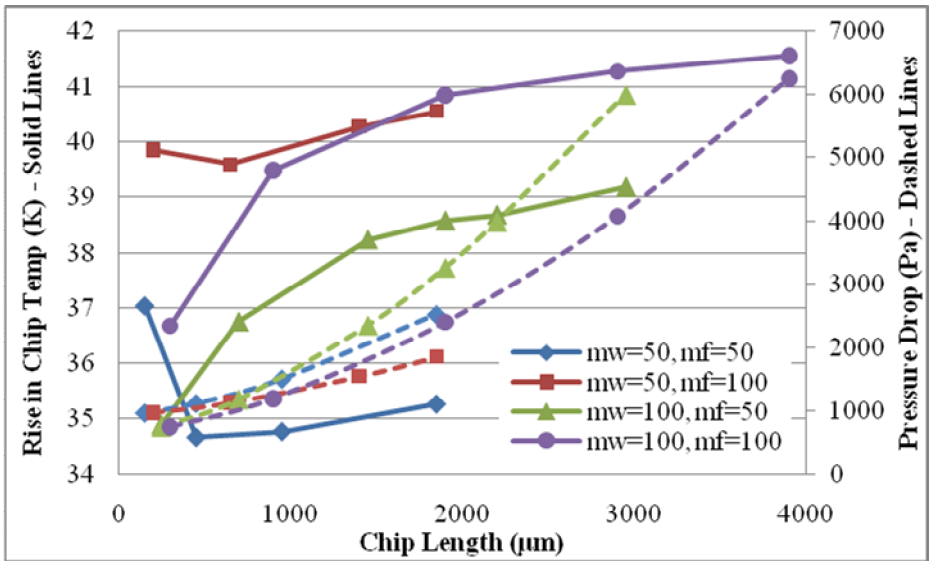


Figure 4-37: Pressure drop versus thermal performance tradeoff for various microchannel dimensions and number of channels (M_h = 750 µm, M_w = 200 µm, M_f= 50 µm, $v_{microchannel}$ = 0.625 m/s).

A closer look at the pressure drop portion of Figure 4-37 is shown in Figure 4-38. It is interesting to see that at the smaller chip lengths, there are portions where different microchannel dimensions perform better than others.

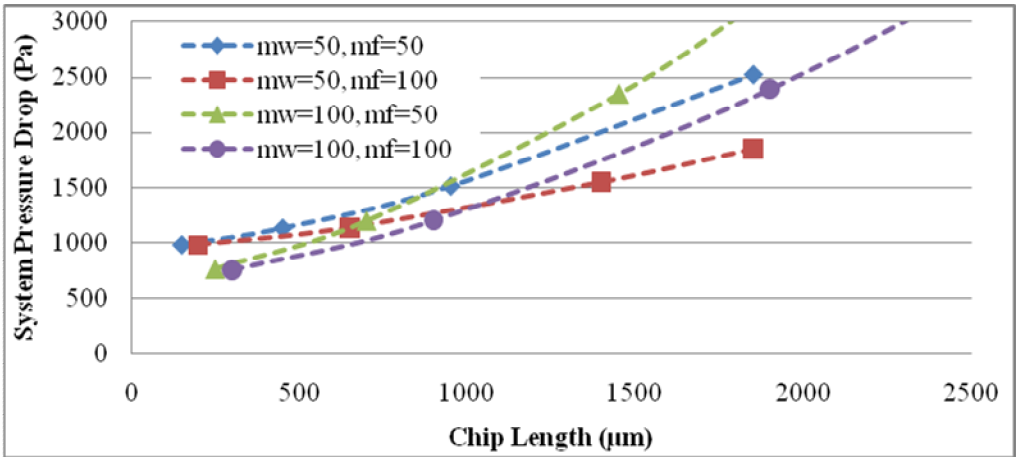


Figure 4-38: Pressure drop plots from the Fluent models for various microchannel dimensions as a function of chip length (M_h = 750 µm, M_w = 200 µm, M_f= 50 µm, $v_{microchannel}$ = 0.625 m/s).

In order to understand why certain microchannel dimensions perform better than others, it is necessary to look to the analytical pressure drop solutions described in Section 3.2. The results are shown in Figure 4-39 with a closer look at the region where the chip length is less than 2.5 mm, the same region as Figure 4-38. Clearly the modeling solution and the analytical solutions give similar results when comparing the two figures although the model shows a higher overall pressure drop than the analytical due to the neglected minor losses. Figure 4-39 shows that as the chip length increases, the microchannel dimension that performs the best in terms of minimizing pressure drop is m_w = 50 µm, m_f = 100 µm and the dimension that has the highest system pressure drop for the same length of chip is m_w = 100 µm, m_f = 50 µm. The systems with m_w = 100 µm, m_f = 100 µm and m_w = 50 µm, m_f = 50 µm had very similar pressure drops with the m_w = 100 µm, m_f = 100 µm having a slightly lower drop.

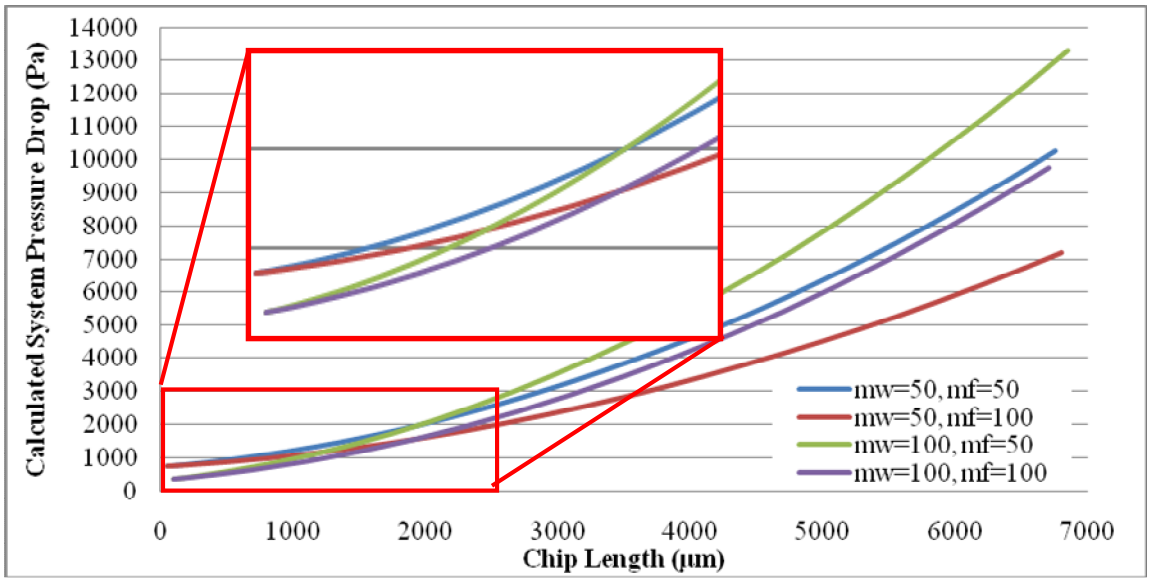


Figure 4-39: Pressure drop plots from the analytical pressure drop calculations for various microchannel dimensions as a function of chip length (M_h = 750 µm, M_w = 200 µm, M_f = 50 µm, $v_{microchannel}$ = 0.625m/s).

In order to understand why these crossovers occur, it is beneficial to look at the pressure drop contributions from both the manifolds and microchannels, shown in Figure 4-40. The microchannel portion is shown as dashed lines and is only based on the microchannel width and is independent of the chip length. Thus, since the microchannel velocity is defined as constant, the microchannel pressure drop is also constant for all chip lengths for both m_w = 50 µm and m_w = 100 µm.

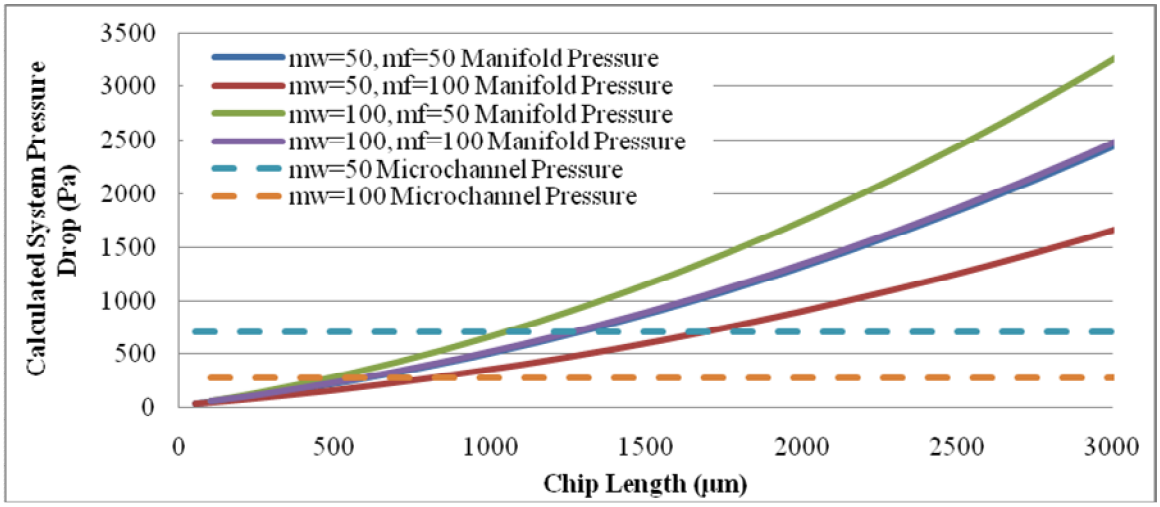


Figure 4-40: Figure showing the analytical pressure drop calculations broken up into the manifold and the microchannel portions for various microchannel dimensions as a function of chip length (M_h = 750 µm, M_w = 200 µm, M_f = 50 µm, $v_{microchannel}$ = 0.625 m/s).

The portion of the pressure drop from the manifold increases as the chip length increases, as is shown in Figure 4-40. This is because pressure increases as both the flow rate and the channel length increases according to the equations derived in Section 3.2:

$$\Delta p_{manifold} = \frac{8\mu L_{manifold} Q\left(M_w + M_h\right)^2}{\left(M_w M_h\right)^3} \tag{4-6}$$

The length of the manifold channel is calculated by adding the inlet and outlet manifold channel lengths (which are equivalent) to the chip length, as is shown in Equation (4-7). As the number of microchannel increases, the manifold length also increases which causes the pressure drop to increase.

$$L_{manifold} = 2L_{manifold\,inlet} + L_{chip} = 2L_{manifold\,inlet} + N_{ch} \times m_w + (N_{ch} - 1) \times m_f \qquad (4\text{-}7)$$

The manifold volumetric flow rate increases because it is dependent on the N_{ch} and m_w, as is shown in Equation (4-8). As the N_{ch} and m_w increases, so does in manifold volumetric flow rate which causes the pressure drop to increase.

$$Q = \mathrm{v}_{microchannel} \times N_{ch} \times m_w \times m_h \qquad (4\text{-}8)$$

It is interesting to look at how varying the m_w's and m_f's independently effects the pressure drop. Therefore, each of these conditions is looked at next. Figure 4-41 shows that the pressure drop increases when the m_f decreases. So in terms of minimizing pressure drop, the m_f should be maximized.

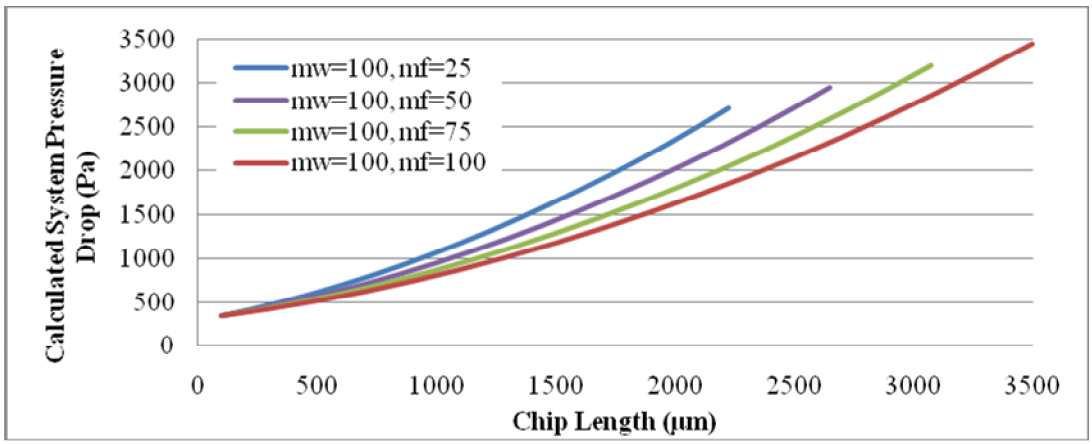


Figure 4-41: Graph of the calculated pressure drops for various microchannel fin widths showing as the fin width increases, the pressure drop decreases (M_w = 200 µm, M_f = 200 µm, M_h = 750 µm, m_w = 100 µm, m_h = 150 µm, $v_{microchannel}$ = 0.625 m/s)

The pressure drop is then looked at in terms of the m_w and this relationship is slightly more complicated as is shown in Figure 4-42. Various chip lengths have different m_w's which would minimize pressure drop. For smaller chip lengths, it is clear that maximizing the m_w minimizes the pressure drop but for the larger chip sizes, the largest m_w now creates the largest pressure drop and the minimum is around 40-50 µm.

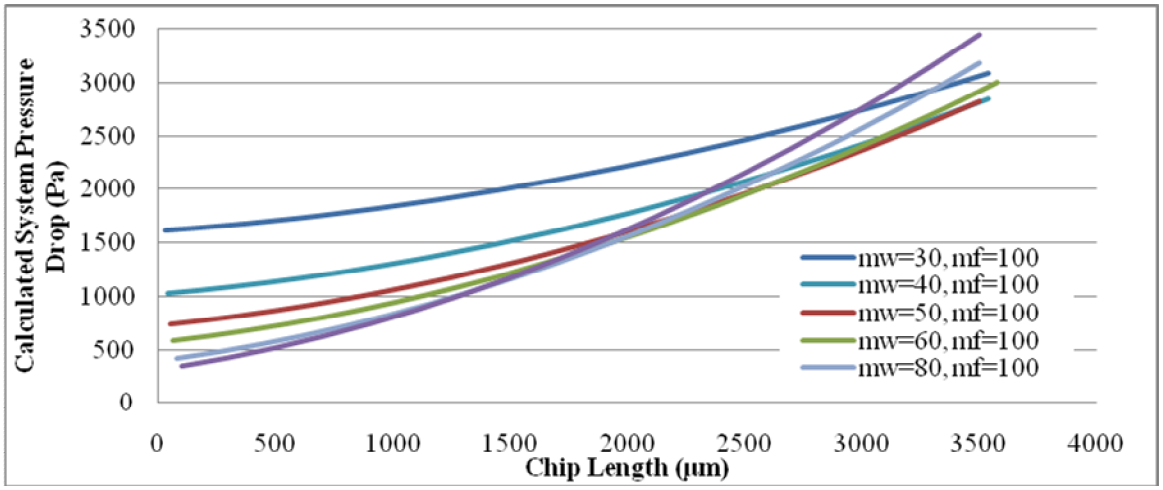
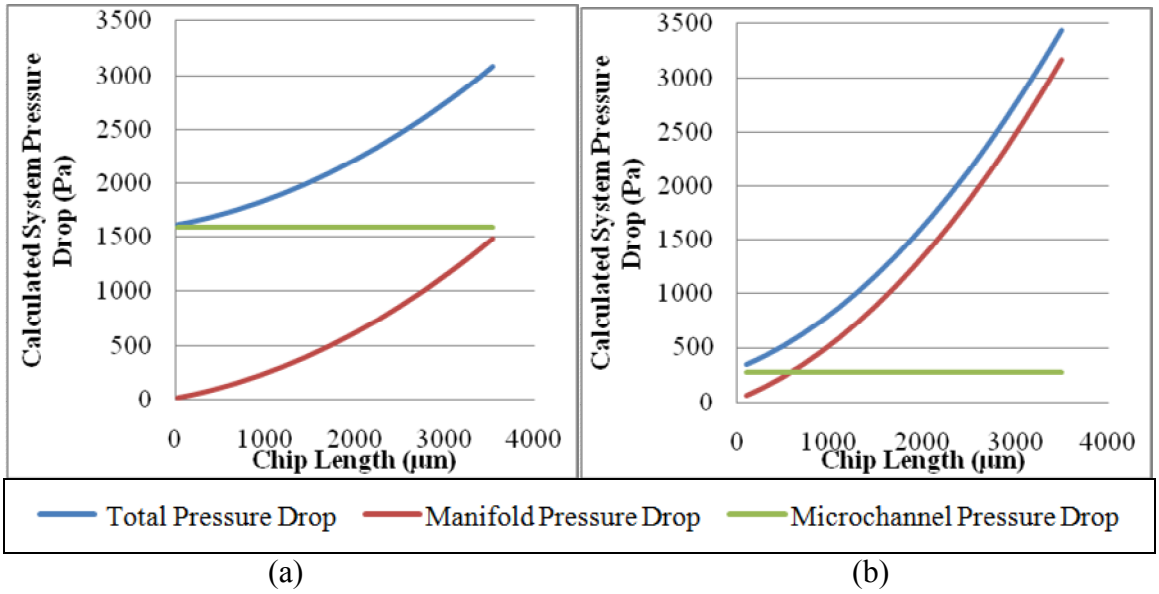


Figure 4-42: Graph of the calculated pressure drops for various microchannel widths (M_w = 200 µm, M_f = 200 µm, M_h = 750 µm, m_f = 100 µm, m_h = 150 µm, $v_{microchannel}$ = 0.625 m/s)

A closer look at why this variation happens is shown by breaking the total pressure drop into the portion contributed from the manifold and the portion from the microchannel, which is shown in Figure 4-43 for a m_w = 30 µm (Figure 4-43a) and a m_w = 100 µm (Figure 4-43b). Since the flow rate through each microchannel is, by definition, the same, the pressure drop is constant for the various chip lengths and only depends on the m_w. A smaller m_w would lead to a larger pressure drop in that channel which is shown clearly in the figure where the pressure drop is almost 6 times larger for the m_w = 30 µm channel as compared to the m_w = 100 µm channel. Thus for smaller chip

lengths, the pressure drop of the smaller manifold widths dominate. As the chip length increases, the manifold pressure drop starts to dominate. This is because even though the manifold channels dimensions are the same, the volumetric flow rates are quite different. For a chip length of 3500 µm, there are twenty-eight 30 µm channels which require a volumetric flow rate into the manifold of 4.7 mL/min. Whereas, for the same chip length, there are only eighteen 100 µm channels which require 10.1 mL/min into the manifold.

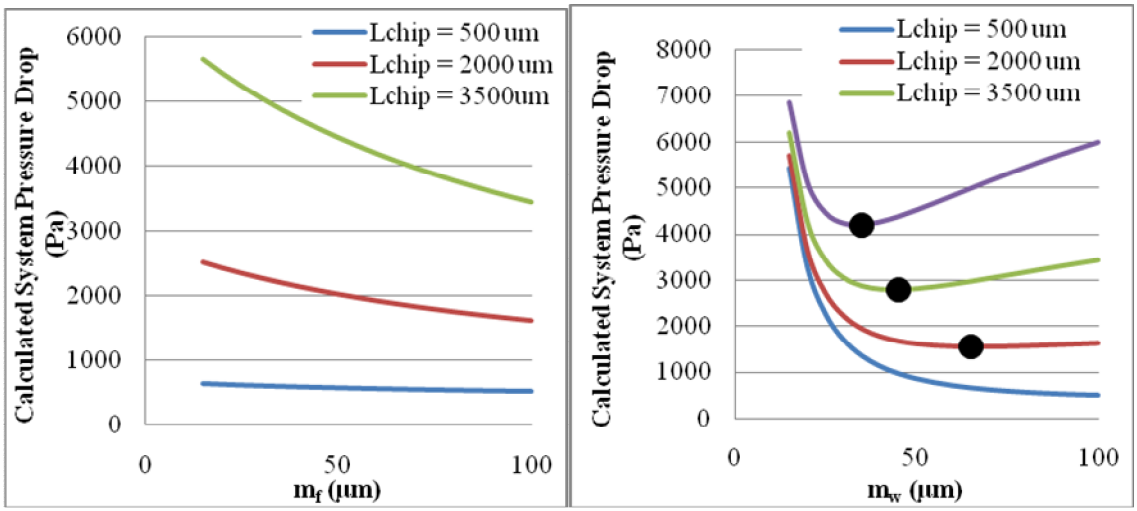


(a) (b)

Figure 4-43: A breakdown of the total system pressure drop into the manifold and microchannel portions for (a) m_w=30 µm and (b) m_w = 100 µm (M_w = 200 µm, M_f = 200 µm, M_h = 750 µm, m_f = 100 µm, m_h = 150 µm, $v_{microchannel}$ = 0.625 m/s)

It is also interesting to look at how the pressure drop is affected when the chip length is constant and microchannel fin width and microchannel width are varied, which is shown in Figure 4-44a and b, respectively. For a given chip length, as the microchannel fin width is increases, the pressure drop goes down. This is because the flow rate and width of each microchannel are the same, so the pressure drop in each microchannel is

the same. But as the microchannel fin increases, the pressure drop in the manifold decreases which decreases the overall pressure drop of the system. The manifold pressure drop decreases because the number of channels decreases while the flow per channel remains the same. Therefore, maximizing the microchannel fin width is desirable.

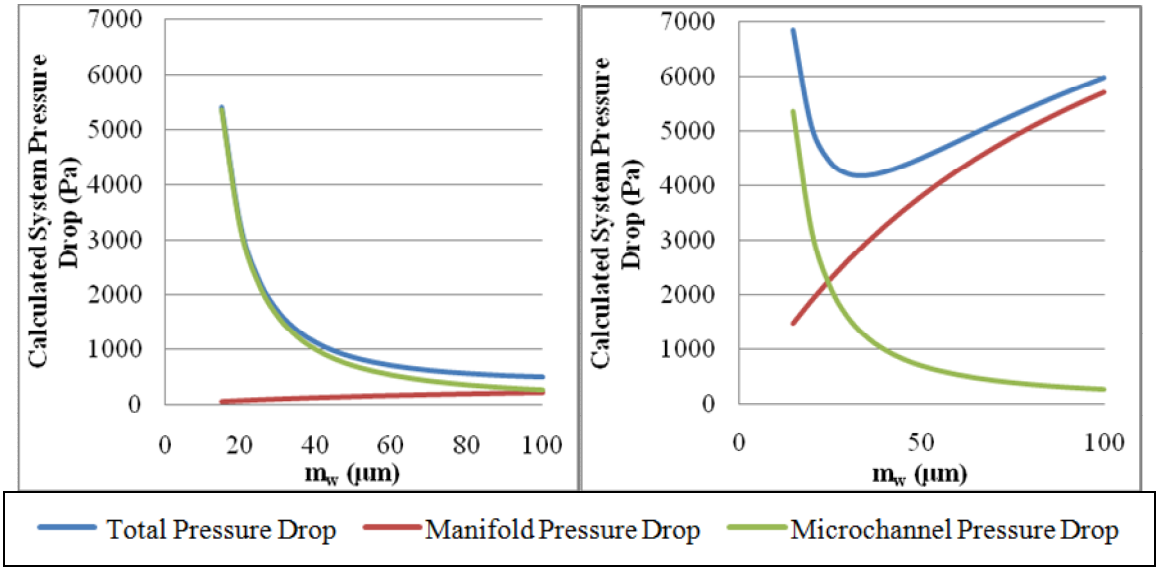


(a) (b)

Figure 4-44: A plot of how varying the (a) microchannel fin width and (b) microchannel width affects the pressure drops for a given chip length (M_w = 200 µm, M_f = 200 µm, M_h = 750 µm, m_f = 100 µm, m_h = 150 µm, $v_{microchannel}$ = 0.625 m/s)

The effect of varying the m_w, shown in Figure 4-44b is a little more interesting. The black dots in the image indicate a minimum that occurs in each case. For the smallest chip length, a minimum has not yet been reached; therefore a black dot is not shown. In order to explain why this minimum occurs, it is advantageous to look at the effect from both the manifold and the microchannel portions, as is shown in Figure 4-45a and b for the cases of a chip length of 500 µm and 5000 µm, respectively. The figure shows the pressure drop contributed from the microchannel, the pressure drop contributed from the

manifold, and the total pressure drop (the sum of both portions). In both cases the contribution to the pressure drop from the microchannel is the same. The difference is in the contribution from the manifold, which is substantially larger for a larger chip causing this portion to dominate the overall pressure drop. The pressure drop in the manifold increases for a given chip length because as the m_w increases, the number of channels decreases, but the volumetric flow rate increases as the microchannel velocity remains the same. The volumetric flow rate depends on the increase in m_w, which has a larger effect than the reduction in the number of microchannels. Therefore, it can be seen that for a given chip length, an optimum microchannel width can be found.



(a) (b)

Figure 4-45: Calculated system pressure drops showing the portion contributed from the microchannel, the portion contributed from the manifold and the total pressure drops neglecting the minor loss terms for (a) L_{chip} = 500 µm (b) L_{chip} = 5000 µm (M_w = 200 µm, M_f = 200 µm, M_h = 750 µm, m_f = 100 µm, m_h = 150 µm, $v_{microchannel}$ = 0.625 m/s)

Since devices vary quite a bit in size, it is interesting to look at how the chip length affects the performance. The first condition that was analyzed was where the flow velocity through each microchannel was constant while the number of channels was varied from 2 to 20 channels for four different microchannel geometries. As the chip length increases, both the pressure drop and temperature increase. The temperature increases because of the additional heating of the fluid going down the manifold. The pressure increases because of the additional length of the manifold channel. The pressure drop curves show that at the smaller chip lengths some microchannel dimensions perform better than others. Using the zeroth order pressure drop calculations, the pressure drop in each microchannel will be constant whereas the pressure drop in the manifold will increase with increasing chip length. It is interesting to look at how varying the m_w's and m_f's affects the pressure drop for a constant microchannel velocity. As the m_f is increased, the pressure drop decreases; therefore, m_f should be maximized. An optimum m_w can be found which depends on the chip length due to the pressure drop relation between the manifold and the microchannels. As the chip length increases, so does the optimum m_w which minimizes the pressure drop.

4.5.2 Results for Constant Volumetric Flow Rate

The condition where the flow velocity in each microchannel was constant for various chip lengths was just investigated; therefore, the second condition that will be analyzed is when the volumetric flow rate into the system is constant with the same geometries as in the previous section. The channels were varied between 2, 5, 10, 15 and 20 channels for various flow rates. The full set of models is shown in Table 4-7.

Table 4-7: Models run for $m_w = 100$ µm, $m_f = 100$ µm channels for a variety of number of channels

m_w (µm)	m_f (µm)	M_h (µm)	M_w (µm)	M_f (µm)	m_h (µm)	Q (mL/min)	v_{in} (m/s)	$v_{microchannel}$ (m/s)	Q_{system} (mL/(min*µm))	N_{ch}
100	100	750	200	50	150	1.125	0.125	0.625	0.0045	2
100	100	750	200	50	150	1.125	0.125	0.25	0.0045	5
100	100	750	200	50	150	1.125	0.125	0.125	0.0045	10
100	100	750	200	50	150	1.125	0.125	0.0833	0.0045	15
100	100	750	200	50	150	1.125	0.125	0.0625	0.0045	20
100	100	750	200	50	150	5.625	0.625	3.125	0.0225	2
100	100	750	200	50	150	5.625	0.625	1.25	0.0225	5
100	100	750	200	50	150	5.625	0.625	0.625	0.0225	10
100	100	750	200	50	150	5.625	0.625	0.4167	0.0225	15
100	100	750	200	50	150	5.625	0.625	0.3125	0.0225	20
100	100	750	200	50	150	11.25	1.25	6.25	0.045	2
100	100	750	200	50	150	11.25	1.25	2.5	0.045	5
100	100	750	200	50	150	11.25	1.25	1.25	0.045	10
100	100	750	200	50	150	11.25	1.25	0.833	0.045	15
100	100	750	200	50	150	11.25	1.25	0.625	0.045	20

A summary of the modeled data is shown in Figure 4-46 indicating the rise in chip temperature versus pressure drops for various chip lengths and flow rates. The figure shows that for a given inlet velocity, as you increase the chip length, the chip temperature rises because the average flow through each channel is decreased. Additionally, Figure 4-46 shows that increasing the chip length causes the pressure drop to decrease.

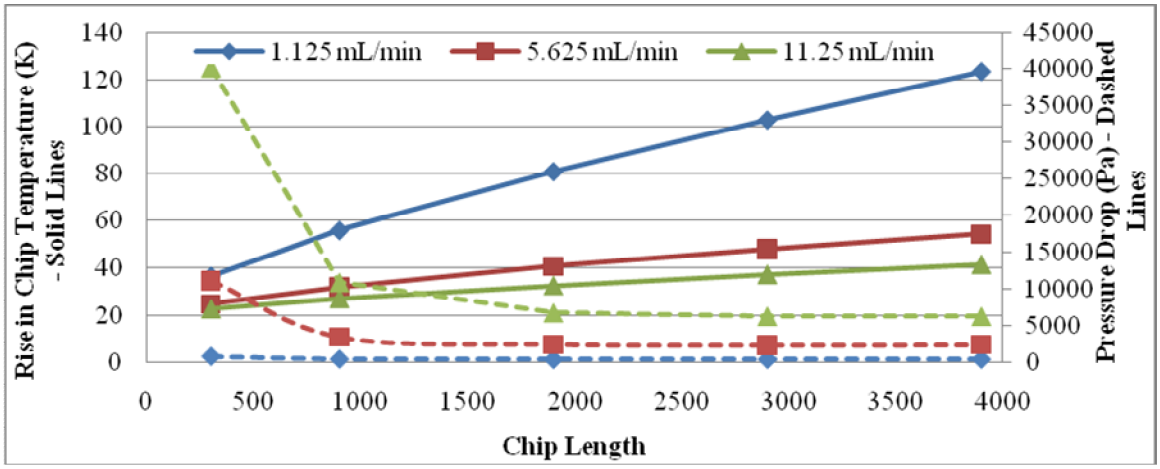
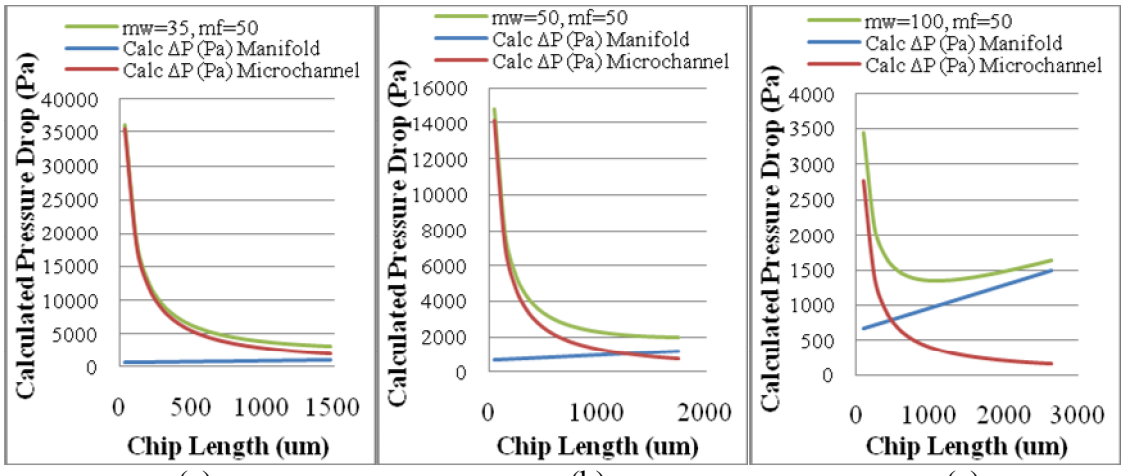


Figure 4-46: Thermal performance and pressure drop for various number of microchannels for $M_w = 200$ µm, $M_f = 50$ µm, $M_h = 750$ µm, $m_w = 100$ µm, $m_f = 100$ µm, $m_h = 150$ µm

In order to explain the pressure drop trends a little more, the pressure drops are calculated using Hagan-Poiseuille's pressure drop equations with multiple microchannel geometries for a given system flow rate, as is shown in Figure 4-47. The figure shows that as the chip length increases, the pressure drop approximates that of the manifold channel alone. At any given chip length, depending on the geometry, either the manifold or the microchannel will dominate the pressure drop. For small chips, typically the microchannel will dominate and for large chips, typically the manifold will dominate. The crossover point will depend on the geometry and will have a minimum pressure drop. In general, the pressure drop in the manifold will be the same for a given chip length, just the pressure drop from the microchannel will vary. Therefore, there is an optimum chip length to minimize the pressure drop. As the chip length gets very large, the pressure drops will be the same independent of microchannel dimensions because the manifold will dominate.



(a) (b) (c)

Figure 4-47: Calculated pressure drops for various microchannel dimensions (M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, v_{in} = 0.625 m/s)

The second condition that was analyzed was where the volumetric flow rate into the system is constant. The results show that as you increase the chip length, the average chip temperature rises because the average flow through each channel is decreased. Additionally, increasing chip length causes the pressure drop to decrease because as the chip length increases, the total system pressure drop approximates that of the manifold alone which decreases with increasing chip length.

4.6 Thermal Performance Independent of Manifold Dimensions

As was pointed out in this chapter, varying the M_f and M_h has very little effect on the thermal performance. In order to emphasize this point, all the models with m_w = 100, m_f = 100, M_w = 50 and m_h = 150 for all the various manifold heights and widths is plotted in Figure 4-48. A magnified portion of the curve is also shown in the figure with ±10% error lines. Similar plots can be made for all other microchannel geometries.

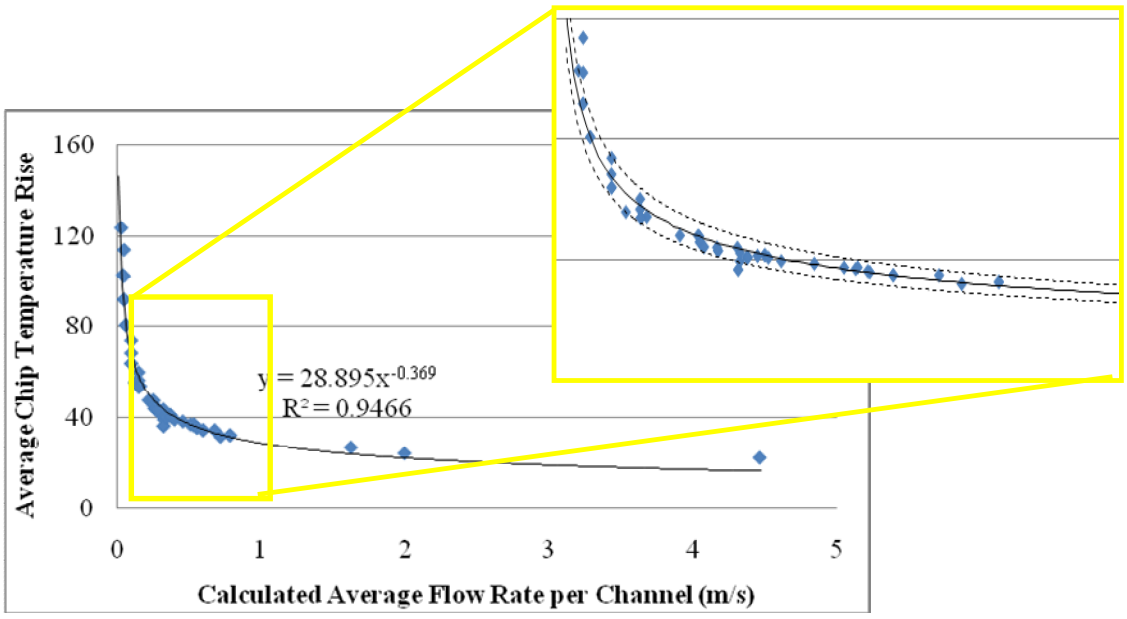


Figure 4-48: Plot showing the independence of the average chip temperature on both the manifold height and the manifold fin width

The average flow through each channel can be calculated by taking half the volumetric flow rate and dividing it by the total cross sectional area of the microchannel:

$$v_{microchannel} = \frac{0.5Q}{N_{ch} * m_w * m_h} \tag{4-9}$$

The average flow rate per microchannel is found for the model by simply averaging all the average velocities in each of the microchannels. Plotting the calculated versus the average modeled for every model run is shown in Figure 4-49. The plots show a very good comparison.

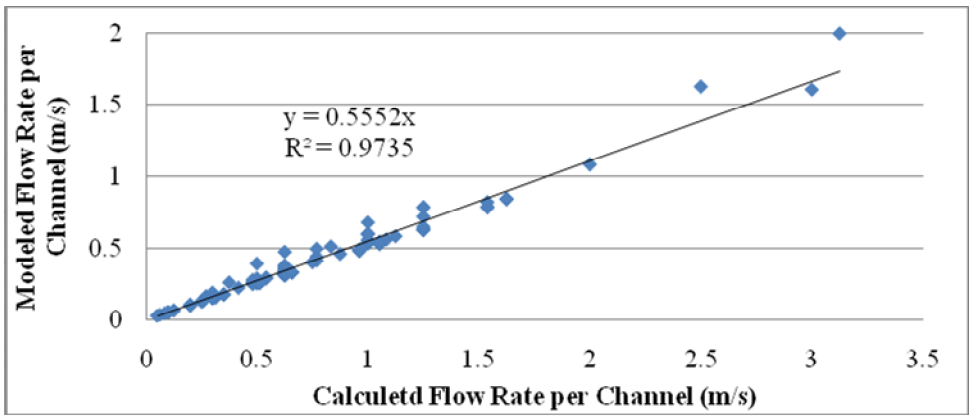
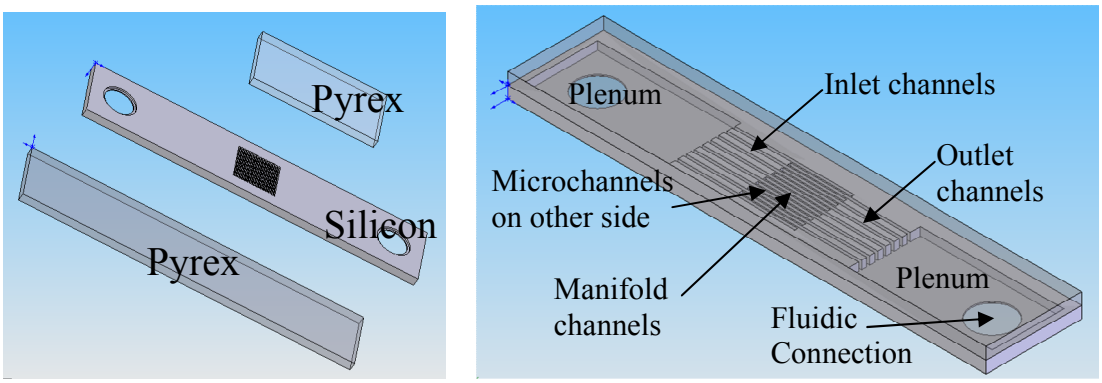


Figure 4-49: Plot comparing the average flow rate per channel calculated versus modeled

5 Manifold Microchannel Version 1 (MMC1)

MMC1 was the first iteration of the manifold microchannel cooler fabricated in this study. Its purpose was to test the fabrication procedure without using actual devices, to learn the fabrication sequence, and to determine complications that might occur.

The exploded view of MMC1 is depicted in Figure 5-1a. The structure consists of three strips, a 500 µm thick four-inch silicon wafer sandwiched by a four-inch Pyrex wafer on the backside and Pyrex strips on the top side. The top side is where the device would normally be attached but Pyrex is used at first for visual inspection and to test the fabrication procedure. The main aspects of the MMC1 design, shown in Figure 5-1b, include the plenums, inlet and exit manifold channels, microchannels, and the fluidic connections. The bottom side refers to the side containing the plenums and the manifold channels; whereas, the top side refers to the side containing the fluidic connections and microchannels. The plenums purpose is to minimize turbulence of the water entering the manifold.



(a) (b)

Figure 5-1: Schematic views of MMC1 (a) three layer exploded view (b) labeled with the main parts

The holes for the fluid connection were designed with a two-step etch for easier tube alignment and connection, as shown in Figure 5-2a. The smaller circle is designed to act as a ledge for the stainless steel tube to rest on so it will not protrude into the plenum. The diameter of the smaller circle was designed to be the same diameter as the inside of the tube and the larger diameter was designed to be the exterior dimension of the tube. Figure 5-2b shows the completed cooler and its overall dimensions: 20 mm long, 3 mm wide and 1.5 mm thick.

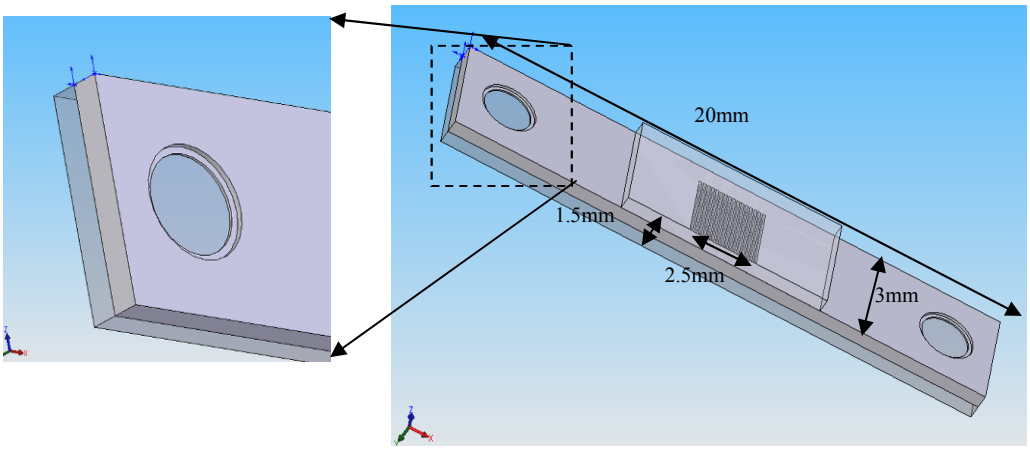
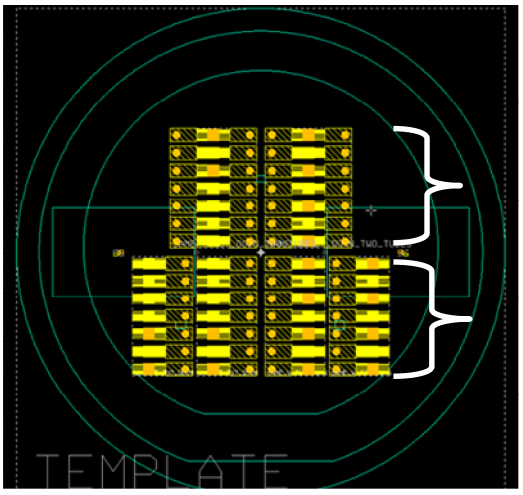


Figure 5-2: Schematic depicting (a) the double etches for the inlet tube and (b) the overall dimensions

5.1 MMC1 Wafer and Dimensions

The complete wafer layout is shown in Figure 5-3. This layout was drawn in LASI, the program used to design the photolithography masks. The 14 devices on the top half of the wafer were designed with both inlet and outlet fluidic connections; whereas, the lower 28 devices were designed with only inlet tubes. For testing purposes, omitting the exit simplifies testing because the fluid can exit the device at a known atmospheric pressure. In actual applications, an exit channel is necessary.



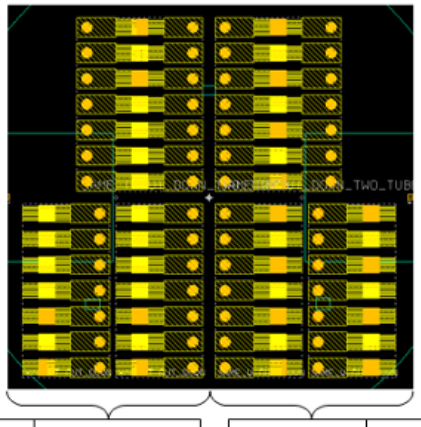
14 pieces have both an inlet and an exit, this will be necessary in the final design

For testing purposes, most pieces (28) have just an inlet. To test feasibility and flow rates, this is all that is necessary.

Figure 5-3: Overall wafer template drawn in LASI

The dimensional layout, shown in Figure 5-4, shows the left side with constant fin thickness and the right side with constant microchannel thickness. On the left side, all of the devices have a fin thickness of 50 μm with microchannel widths varying from 32.3 μm to 146.2 μm. The right side has devices with a constant microchannel thickness of 50 μm and the fin thickness varies from 31.7 μm to 154.2 μm. This allows for a wide range of microchannel dimensions.

On this side of the wafer, all the microchannels have the same fin thickness but the channel width varies between 32.3µm and 146.2µm.



On this side of the wafer, all the microchannels have the same thickness but the fin width varies between 31.7µm and 154.2µm.

	w (µm)	t (µm)	number of channels
Constant Fin Thickness	32.3	50	31
	41.1	50	28
	52	50	25
	65.9	50	22
	84.2	50	19
	109.4	50	16
	146.2	50	13

	w (µm)	t (µm)	number of channels
Constant Microchannel Width	50	31.7	31
	50	40.7	28
	50	52.1	25
	50	66.7	22
	50	86.1	19
	50	113.3	16
	50	154.2	13

Figure 5-4: Wafer layout with the dimensional information

5.2 Fabrication Process Sequence

The full fabrication sequence is outlined in Figure 5-5. The fabrication sequence starts with a standard thickness (500 µm) four-inch diameter silicon wafer (Step 1). The wafer has a 1 µm thermal oxide grown on both sides. MEMS processes are outlined in Appendix E.

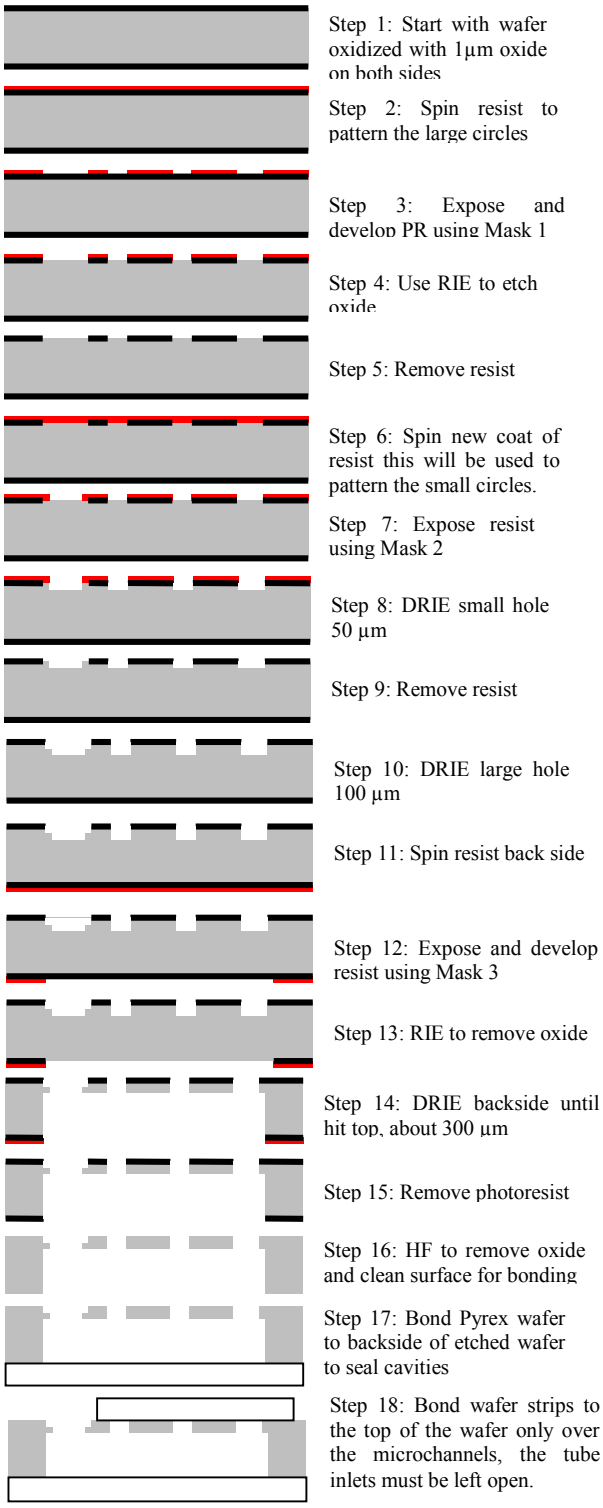


Figure 5-5: Process sequence for MMC1

The purpose of steps 2 through 10, shown in Figure 5-5, is to create the tube attachment and microchannels. Steps 2 and 3 involve spinning and exposing a 5 µm thick AZ9245 positive resist using Mask 1, shown in Figure 5-6. This mask contains the larger circles for the tube inlet and also the rectangular microchannel pattern. The resist is then developed for about four minutes in the AZ400K resist developer. The development was checked with an optical microscope. Step 4 uses reactive ion etching (RIE) to etch the oxide while using the resist as a masking layer. Then the resist is removed using a photoresist stripper, PRS-3000 heated to 80 ºC (Step 5).

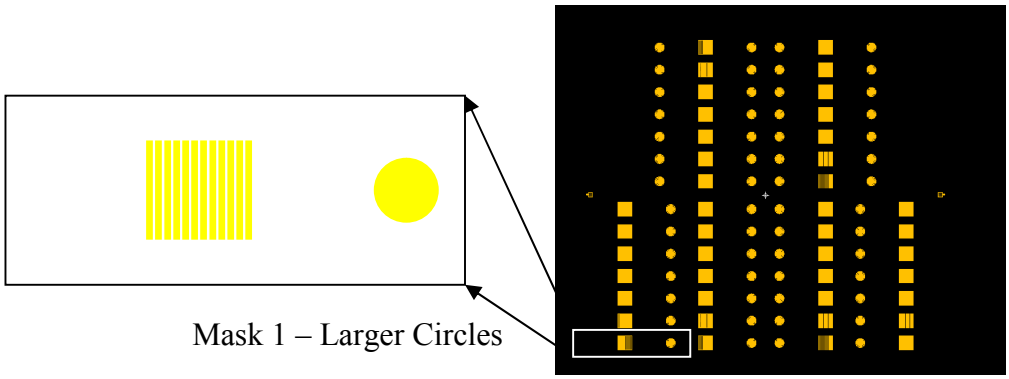


Figure 5-6: Image of Mask 1 for MMC1

The same steps as above are used to spin, expose and develop PR again for the small holes and microchannels (Steps 6 and 7) using Mask 2, shown in Figure 5-7. Next is a DRIE etching of the small inlet holes and the microchannels (Step 8). This etch is about 50 µm deep. The resist is then removed using PRS-3000 (Step 9) and a subsequent DRIE etch is performed to etch the inlet tube holes and to further etch the microchannels using the remaining oxide as a mask (Step 10). This etch is about 100 µm. At this point both the inlet holes and the microchannels have been etched to their desired depth.

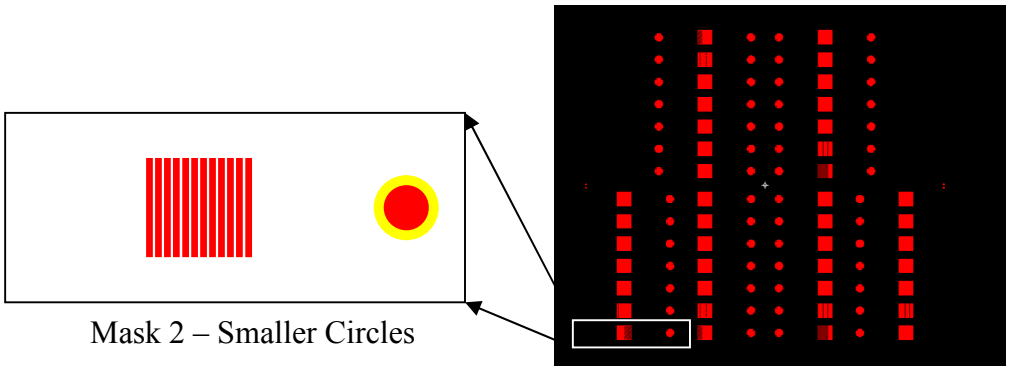


Figure 5-7: Image of Mask 2 for MMC1

The microchannels and the holes for the stainless steel tube attachment are now complete. The next set of steps, 11 through 15, involves etching the manifold channels onto the backside of the silicon wafer. This set of steps is very similar to the lithography performed on the top side of the wafer. First the resist is spun onto the backside of the wafer (Step 11), and then it is exposed and developed using Mask 3, shown in Figure 5-8 (Step 12). The oxide is then removed with a RIE process (Step 13). Both the oxide and the PR are then used as masking layers for the subsequent DRIE etch (Step 14). The remaining PR is then removed by submersing the wafer into heated PRS.

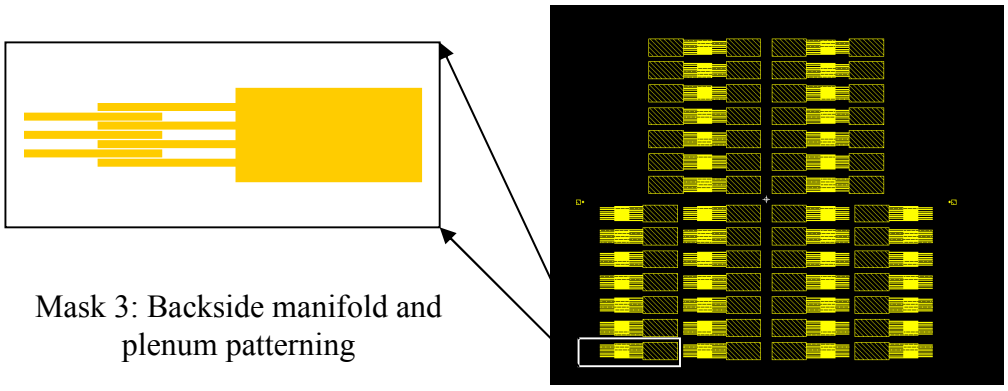


Figure 5-8: Image of Mask 2 for MMC1

Now both the manifold and the microchannels have been etched into the wafer. The next step (Step 16) involves dipping the entire wafer in hydrofluoric acid (HF) to remove any remaining oxide on the wafer. It is necessary to remove the oxide for two reasons. The first is that the oxide is now roughened and uneven due to the etching and therefore is not conducive to an anodic bond. Secondly, oxides are thermally insulating and therefore should be removed to maximize the thermal conductivity. Removing the oxide with HF also cleans the surface in preparation for the subsequent bonding step. Step 17 anodically bonds a Pyrex wafer to the backside of the etched wafer. Once this bond is complete, strips of Pyrex are placed on top of the wafer to cover the microchannel openings and are also anodically bonded, as shown in Figure 5-9 (Step 18). These strips replicate the device attachment with the additional benefit of being optically transparent and easily attached. The strips are cut using a diamond bladed dicing saw.

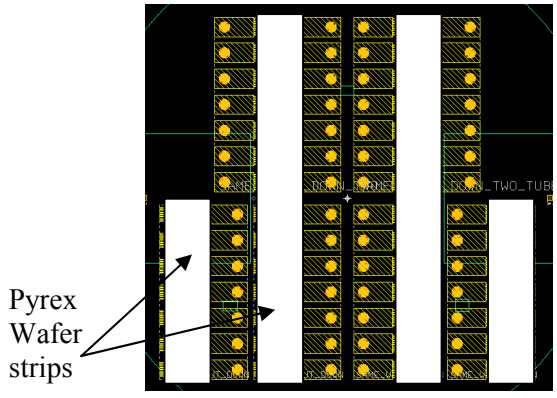
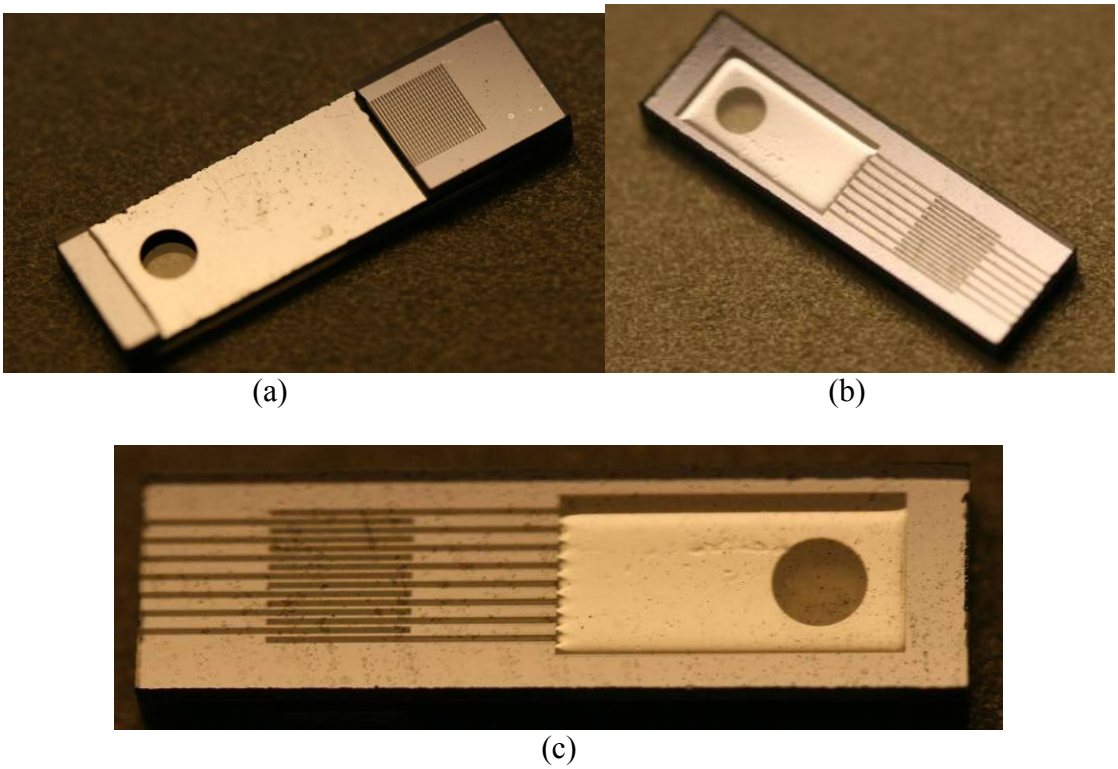


Figure 5-9: Schematic of the Pyrex strips placed on top of the wafer

5.3 Fabricated Device

Once the fabrication is complete, the devices are diced apart using a diamond bladed dicing saw. The completed device is shown in Figure 5-10.



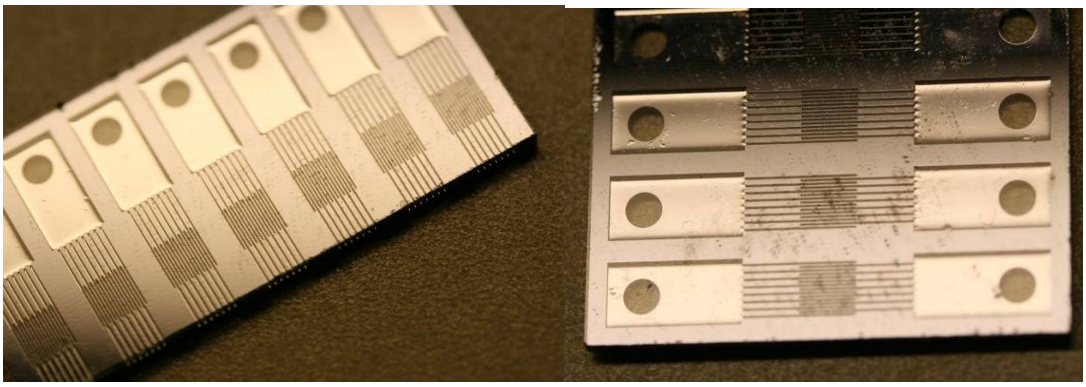
(a) (b)

(c)

Figure 5-10: Photos of the complete fabricated MMC1 device

An array of devices that have been partially diced is shown in Figure 5-11. The devices shown in Figure 5-11a depict ones with an outlet that opens to the ambient; whereas, the devices shown in Figure 5-11b have both an inlet and an outlet that would connect to tubes. The latter is what an actual operating device would look like to allow a closed loop system. The first one is more practical for testing conditions to allow a known exit pressure and minimize variations. The spots that can be seen on the devices

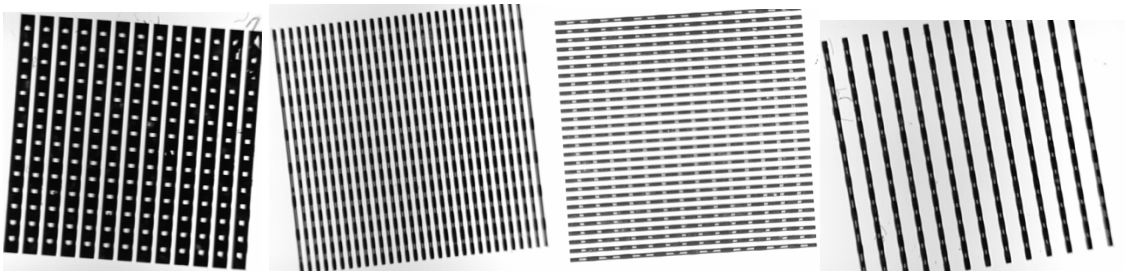
are from contamination in the Pyrex and do not affect the quality of the device. The anodic bond was visually observed to be void free.



(a) (b)

Figure 5-11: Photo showing the array of devices on the wafer (a) outlets opening to ambient (b) cooler showing both an inlet and an exit plenum

Figure 5-12 shows the varying dimensions of the microchannels. Figure 5-12a shows the microchannels of varying channel widths but with constant fin spacing. Figure 5-12b shows microchannels with varying fin spacing but constant channel width.



(a_1) (a_2) (b_1) (b_2)

Figure 5-12: Microscope images of devices with (a) the same fin spacing but with varied channel widths (b) the same channel width but with varied fin spacing (microchannels shown as black strips)

5.4 Fabrication Limitations: Loading and Lagging

Loading is an effect of DRIE where the edges etch faster than the middle due to heavier silicon loading towards the middle of the wafer. Loading was measured to be pretty substantial over the wafer as shown in Figure 5-13. The plenums on the exterior are up to 40 μm deeper than the plenums at the middle.

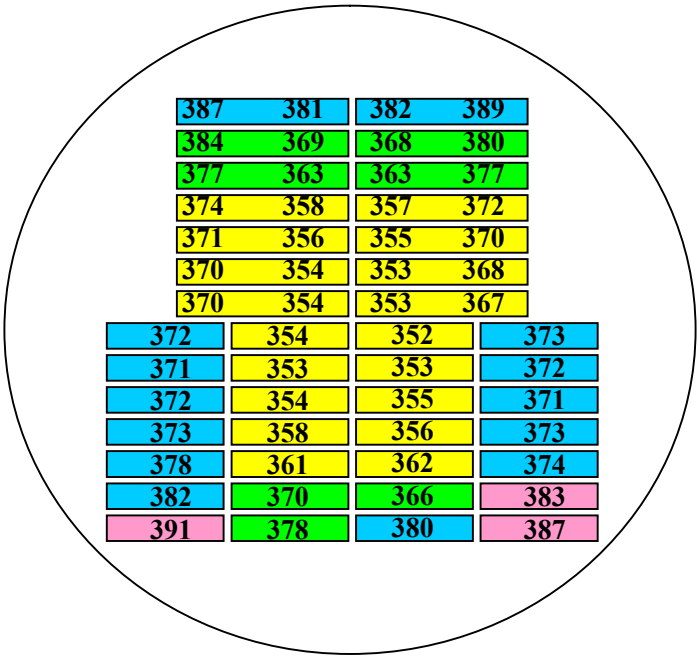


Figure 5-13: Values of loading on the plenums of MMC1

The loading of the manifold channels was also measured it was found that the manifold channels around the exterior were between 20 to 30 μm deeper than the channels toward the middle of the wafer.

Lagging is an effect of DRIE where the smaller areas etch slower than the larger areas. In the case of the manifold side, the plenums are substantially larger than the manifold channels and so would be expected to etch faster. This was in fact the case, as

can be seen by Figure 5-14, which shows the height difference between the height of the manifold channels and the height of the plenums. The height is seen to vary from 25 to 51 μm, which is substantial.

44	38	38	45
51	36	31	43
46	32	31	45
48	32	31	46
46	31	31	46
47	31	31	46
47	31	32	46
25	31	30	30
25	30	31	30
26	30	32	29
27	33	31	29
30	34	34	27
33	36	31	33
38	40	39	34

Figure 5-14: Values of lagging of the plenums on MMC1

5.5 Summary and Improvements

MMC1 was a proof of concept whose intended purpose was to proved the fabrication sequence. For the next MMC design, an active device will be used instead of the Pyrex. The lessons learned from MMC1 include the fact that lagging and loading will be a major consideration in future designs.

6 Manifold Microchannel Version 2 (MMC2)

The second version of the manifold microchannels was labeled MMC2 (Manifold Microchannel Version 2). As stated previously, the objective of this work is to create a manifold microchannel cooler that will reduce the thermal stack and efficiently cool the backside of a power device. The manifold microchannel concept has been elaborated on previously, but the main idea is to have larger manifold channels to transport the fluid into and out of the device at a lower pressure drop, while maintaining smaller microchannels in the active cooling area which improves cooling potential. MMC2 has no electrical isolation between the chip and fluid and has been fabricated and tested using water.

6.1 Microcooler Design

Many considerations were taken into account when designing the manifold cooler. Two design requirements that were accomplished simultaneously were a water tight seal of the device and an electrical connection. Both of these are provided by the AuSn eutectic bond. It is necessary to have minimal voiding to ensure a solid thermal conduction path from the chip into the silicon, no leaking of the fluid, and good electrical connection to the backside of the device. Another design consideration is to ensure electrical isolation of the anode and cathode. This was accomplished with a 2 μm thick oxide layer. Standard copper leads soldered onto the silicon based cooler showed significant coefficient of thermal expansion (CTE) mismatch causing catastrophic failure. Therefore, gold coated leads with “fingers” have been used, as depicted in Figure 6-9 to alleviate the CTE mismatch.

6.2 The Cooler

A 25 mm x 5 mm x 1.5 mm thick cooler was fabricated to cool a 4 mm x 4 mm x 0.4 mm thick SiC diode. MMC2 consists of a three layer stack as is shown in Figure 6-1. The center layer is an etched 1 mm thick silicon wafer which is AuSn eutectically bonded to a silicon carbide (SiC) diode on the topside and a to silicon capping wafer on the backside. For consistency, the topside of the wafer refers to the side with the device and inlet hole and the backside refers to the side with the manifold channels and plenums. Twenty devices are fabricated on each wafer.

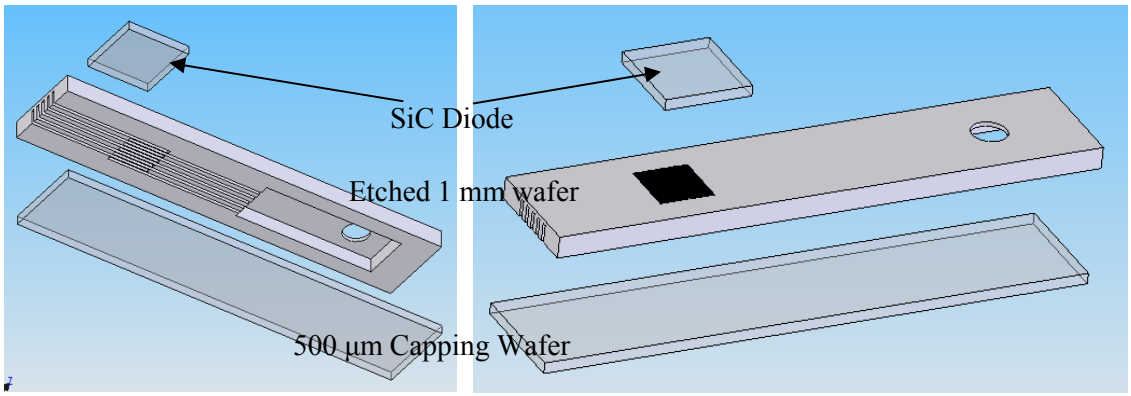


Figure 6-1: Exploded view of MMC2 depicting the three wafer stack

The cooler has been MEMS fabricated out of a single 1 mm thick silicon wafer using deep reactive ion etching (DRIE) to create both the microchannels and the manifold channels. The final design schematic is shown in Figure 6-2. There are five inlet and five exit manifold channels whose dimensions are: 200 µm wide, 250 µm pitch, and 800 µm deep. There are 63 microchannels that are 20 µm wide with a 40 µm pitch and a 200 µm depth. The dimensions were chosen to maximize the ratio of the cross sectional area of the manifold to the microchannels while staying within fabrication limitations. The SiC

diode is bonded directly onto the cooler using a gold-tin eutectic bond. The bond is designed to act as an electrical connection to the backside of the die, a fluidic seal, and a mechanical attachment. A 1.6 mm outer diameter stainless steel capillary tube is sealed to the device with an epoxy. Its purpose is to flow the liquid coolant into the manifold channels. The top side electrical connection is made with 1 mil gold wirebonds and the leads are attached with AuSn solder paste. The active cooling area is 6.25 mm^2; the diode has an active cooling area of 3 mm by 3 mm on a 4 mm square die.

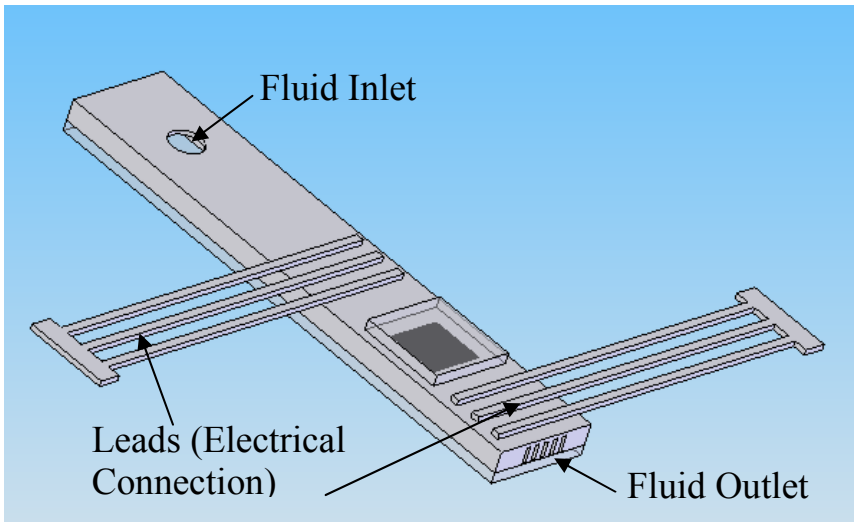


Figure 6-2: Schematic of the final MMC2 device

6.3 Numerical Values

The hydraulic diameter of the microchannels is 36.4 µm and the hydraulic diameter of the manifold channels is 320 µm. Table 6-1 shows the Reynolds numbers for both the manifold and the microchannels at the different tested velocities. All of the Reynolds numbers are well below 2300 so it is in the laminar regime.

Table 6-1: Reynolds numbers for both the manifold and microchannels at different velocities

Q (mL/sec)	Re microchannels	Re manifold channels
0.5	71.9	199.2
1.0	143.7	398.4
1.5	215.6	597.6
2.0	287.5	796.8
2.5	359.3	996.0

6.4 Fabrication Sequence

The basic outline of the fabrication steps is shown in Figure 6-3. This design starts with a 1 mm thick double-side polished silicon wafer of any orientation. The first step is to deposit a 2 μm thick PECVD oxide layer on both sides. This thick oxide is going to act as a masking layer for the backside during DRIE and on the topside it is going to act as an electrical isolation layer for device operation. After the oxide has been deposited, the backside (where the manifold channels are) is patterned with a thick photoresist (10 μm), which is necessary to hold up to the 800 μm deep silicon DRIE that will follow. The oxide is then selectively etched using an RIE dry etch process in Step 3.

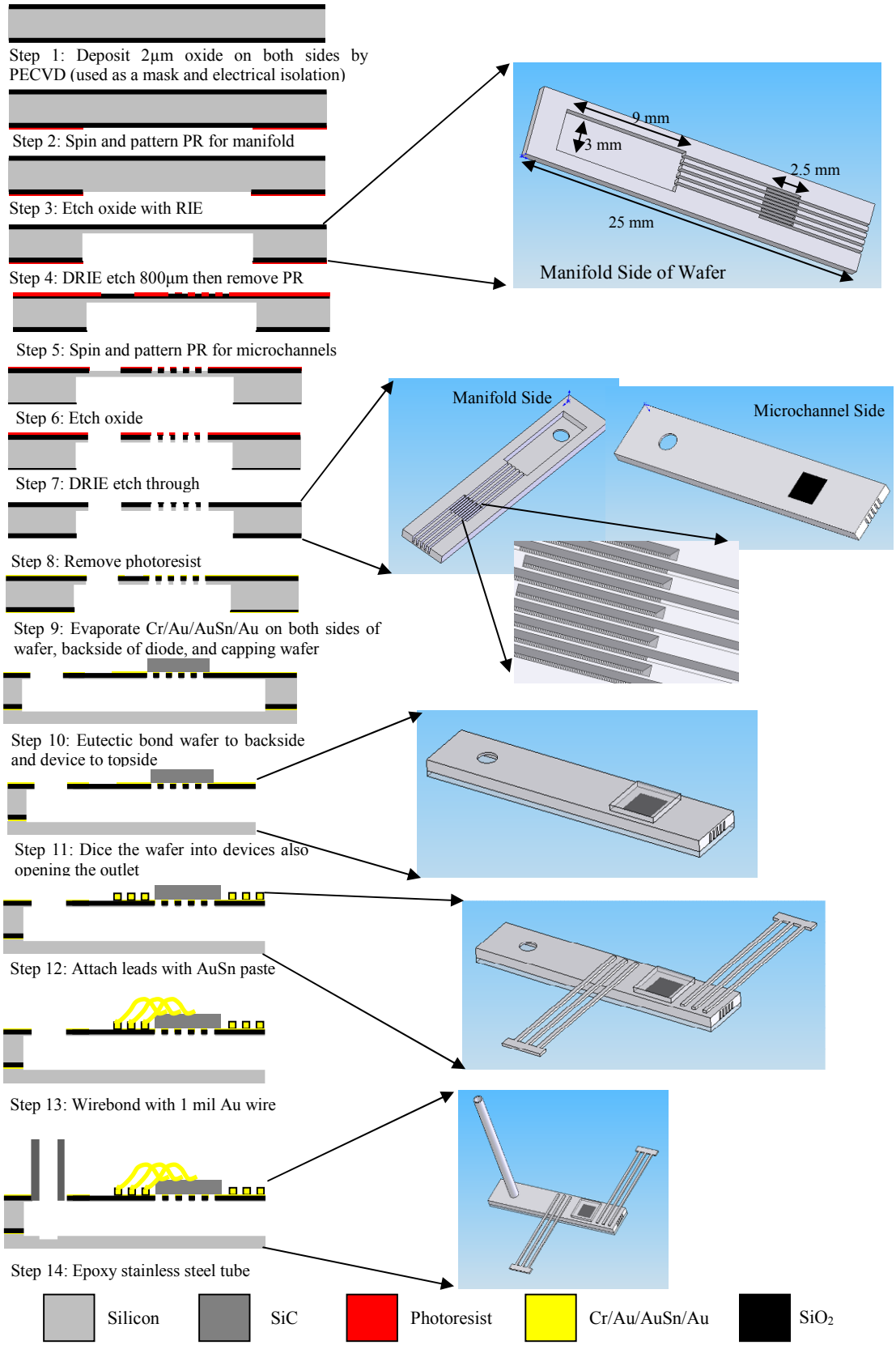


Figure 6-3: MMC2 Fabrication Sequence

Next, in Step 4, the wafer is DRIE etched 800 μm. The current state of the device can be seen in Figure 6-3 alongside Step 4. While attempting to produce a vertical sidewall, this deep etch did however cause a noticeable negative taper, as seen in Figure 6-4, where the bottoms of the channels are wider than the tops. This is a view of the plenums at the entrance to the five inlet manifold channels. Each channel is 200 μm wide and 800 μm deep with 250 μm spacing between the top edges.

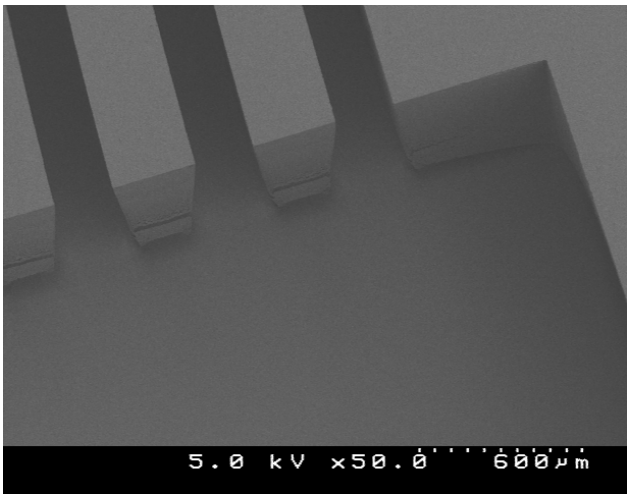


Figure 6-4: Manifold channels with negatively tapered sidewalls.

After the deep etch, the remaining photoresist is chemically stripped and the topside of the wafer is patterned to create the microchannels and the fluidic inlet holes. This is done by patterning a relatively thick photoresist (6 μm) on the top side of the wafer and dry etching the oxide (Steps 5 and 6).

Next, the top side is etched using a DRIE process until it reaches the manifold channels (Step 7). This etch is approximately 200 μm deep and the microchannels are 20 μm wide with 20 μm fins. Figure 6-5 is an SEM image showing the microchannels

meeting the manifold channels, taken from the back side (manifold side). The photoresist is then removed in a heated PRS solution.

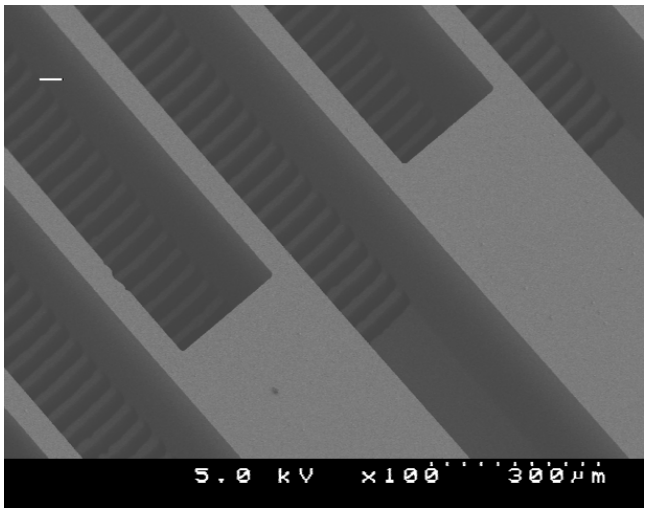


Figure 6-5: SEM image of the etched manifold channels with the visible microchannels at the bottom. Viewed from the back side.

Finally, a metal layer stack is deposited on both sides of the wafer in a CHA e-Beam Evaporator, as is shown in Step 9 of the process sequence. These layers serve as bonding layers for the AuSn eutectic bonds and also provide electrical connections to the SiC device after bonding. The composition of the metal layers is as follows: 50 nm Cr, 50 nm Au, 1 μm AuSn, 50 nm Au. The chrome serves as an adhesion layer between the metal layers and the silicon substrate, while the gold layers act as diffusion and oxidation barriers for the AuSn. This same metal layer stack is deposited on a blank silicon wafer and on the bonding side of the SiC devices.

Because no alignment is required between the capping silicon wafer and the processed wafer, all metal bonding can be performed in a single step in a wafer bonder (Step 10). The capping wafer is placed on the bonding chuck, the processed wafer is

placed onto the capping wafer, and then the devices are placed on top of the open microchannels on the processed wafer. Extra devices or dummy silicon pieces are placed around the individual coolers in non-critical regions to even the pressure distribution across the wafers. To prevent device contact metal from sticking to the bonding chuck, a dummy silicon wafer is placed over the entire stack. Finally, the wafers are placed into the bonder, where they undergo a ten minute eutectic bond process consisting of 1 kTorr applied tool pressure and are heated to 285˚C in a 1.33 kTorr H_2N_2 atmosphere. After removing the dummy wafer, the device structure is as shown in Step 10. Finally, a wafer dicing saw is used to separate the individual cooler devices from the wafer in Step 11. During this process, a cut is made across the exit manifolds providing the fluid exit path.

The bonded and diced wafer is shown below in Figure 6-6. Devices were not used on every opening due to manufacturing defects and a lack of devices. Additional pieces were used around the exterior, and an extra device was placed in the center to balance weight. These pieces distributed the force evenly during the bonding process.

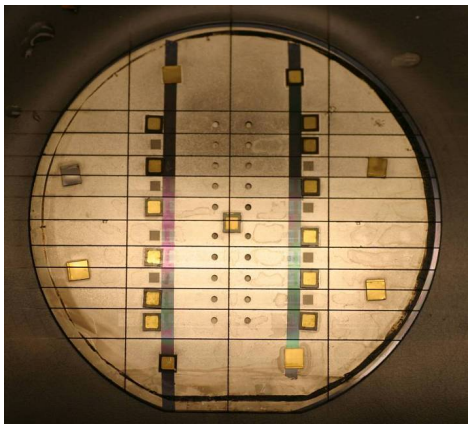
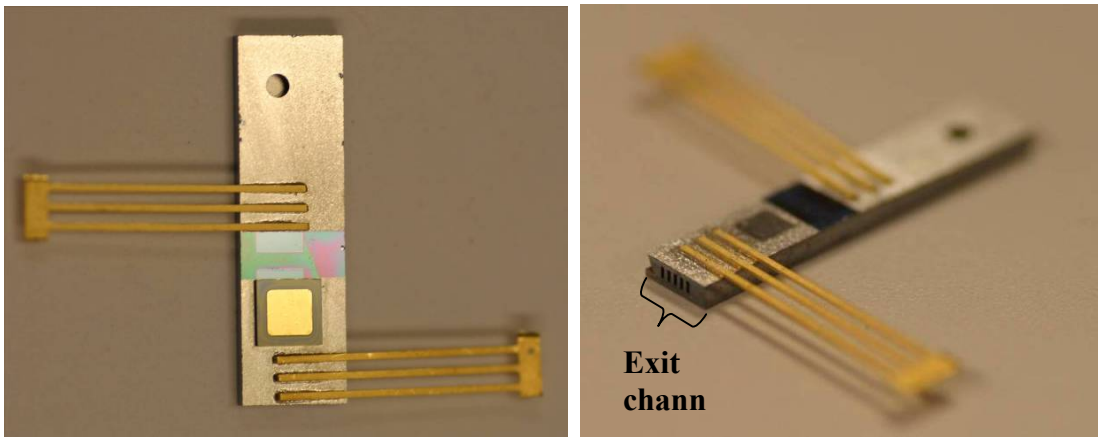


Figure 6-6: Picture of the bonded wafer

The electrical connections to the anode and cathode of the diode are made by soldering the leads then wirebonding, which is shown in Steps 12 and 13 of Figure 6-3. The leads are soldered using a gold-tin solder paste. The leads that were used are gold coated Kovar that was cut from a standard 40-pin leadframe package. Figure 6-7 shows the completed device both (a) with and (b) without a device. Figure 6-7 also shows the 5 exit channels of the device that have been opened with the dicing saw. The three skinny leads were used instead of a one thick lead to minimize the effect of the CTE mismatch between silicon and the metal lead.



(a) (b)

Figure 6-7: Microchannel cooler depicted without (a) and with (b) a SiC device attached

Finally, a 1/16" stainless steel tube is mounted with an epoxy into the etched hole and held in place until cured, shown in Figure 6-8. The epoxy used is Hysol E-20HP, a two-part epoxy that bonds very well to both metals and silicon. The epoxy softens at 80 ºC, so care must be taken to ensure it does not reach this temperature during testing.

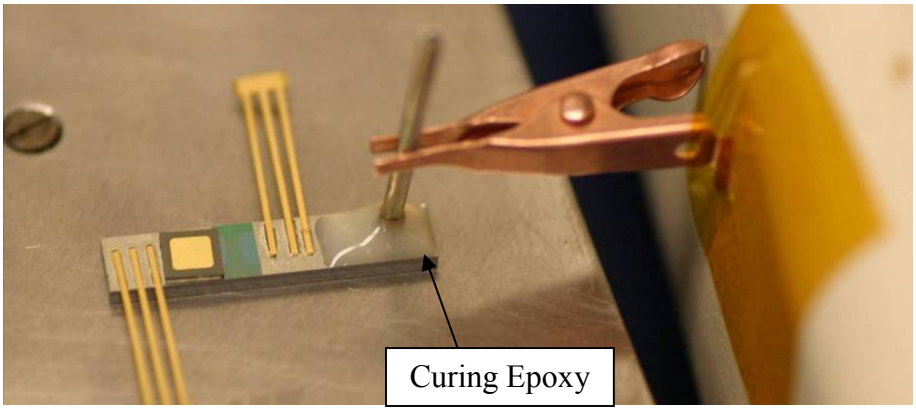
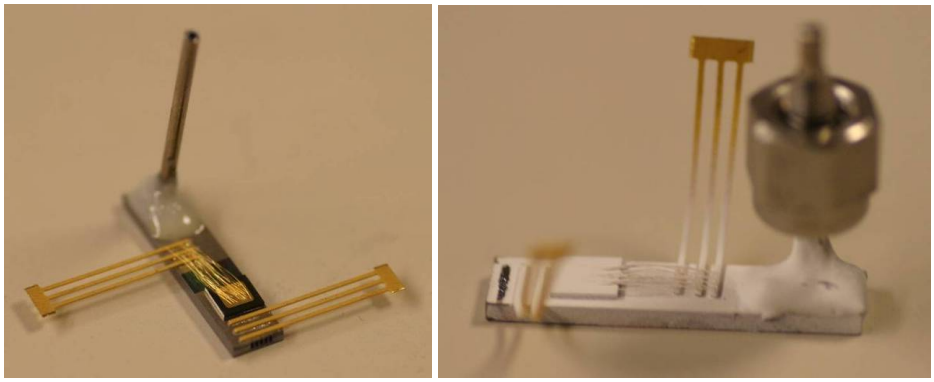


Figure 6-8: Photo showing how the stainless steel tube is held in place while the epoxy cures

6.5 Completed Device

The final cooler, with attached electrical connections and epoxied tube, is shown in Figure 6-9. The wirebonding was performed with 1 mil gold wire. During testing, each device is fitted with a Swagelok fitting, for fluidic connection, and sprayed with boron nitride, for even emissivity when monitored with a thermal camera (Figure 6-9b). [31]



(a) (b)

Figure 6-9: Completed microchannel cooler with leads, SiC device attached, wirebonds, and stainless steel tube connected with epoxy (b) shows the device with Swagelok fitting and boron nitride

For size comparison, a device is shown next to a U.S. quarter in Figure 6-10.

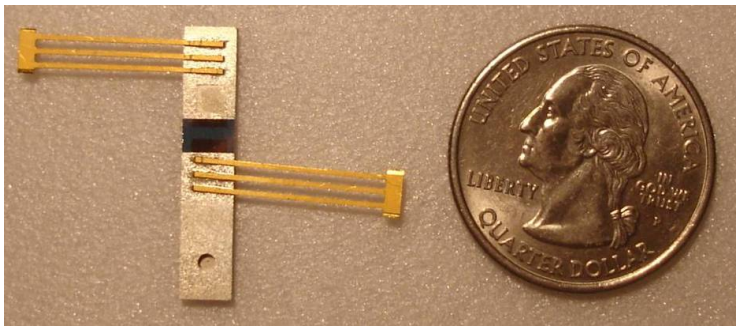
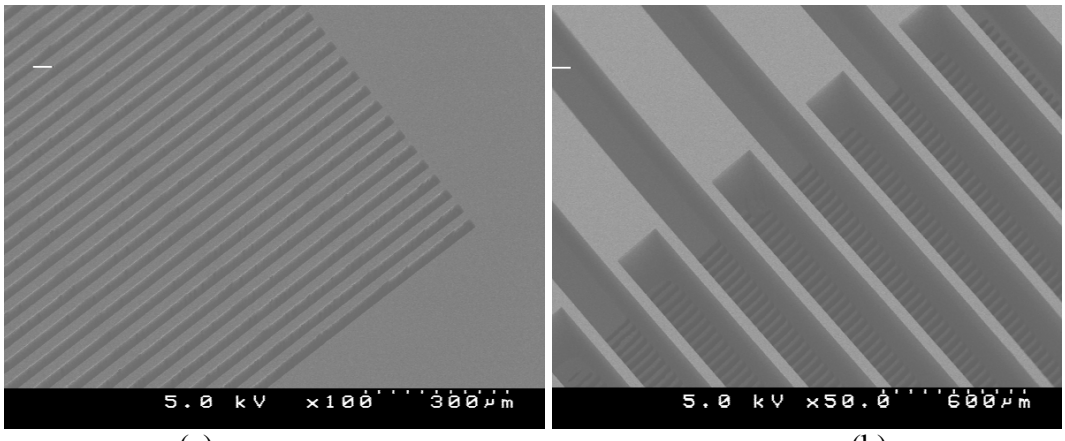


Figure 6-10: A completed microchannel cooler next to a U.S. quarter for size comparison

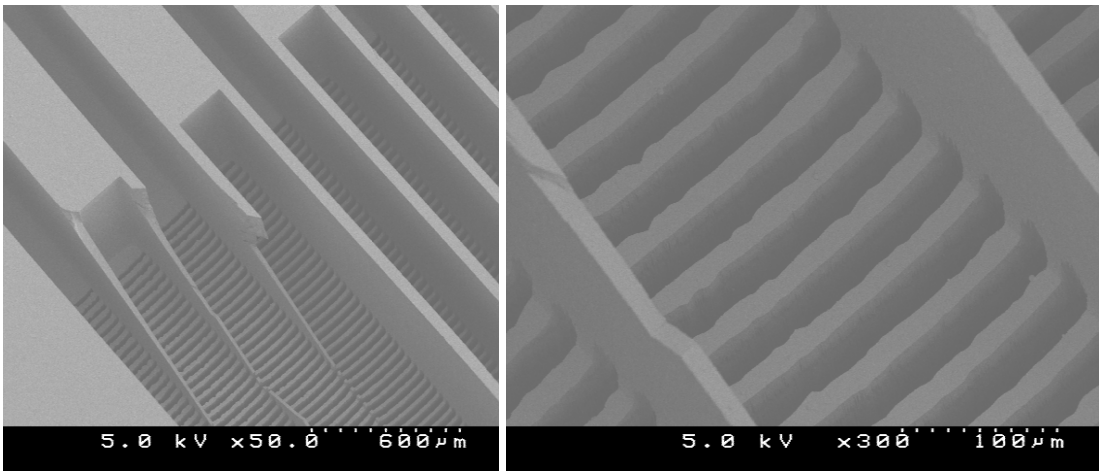
The etched microchannels are 20 µm wide with 20 µm fins. A 100 X magnification SEM of the etched microchannels is shown in Figure 6-11a. The etched manifold channels (200 µm wide and 50 µm spacing) are shown in Figure 6-11b. The microchannels can be seen at the base of the manifold channels. This image shows good alignment between the two sets of channels and also shows clean etches.



(a) (b)

Figure 6-11: SEM of the etched channels (a) 20 µm wide microchannels (b) manifold channels looking into the microchannels

Figure 6-12 shows a broken manifold channel which is intended to show the interface between the microchannels and the manifold channels and the negative tapering of the sidewalls. Figure 6-12a shows the negative tapering because at the top of the fins they are 50 μm but by the bottom of the fins, they have been significantly reduced. Figure 6-12b shows a magnified image of the interface between the microchannels and the manifold channels. Some over-etching can be seen, which is required to etch through all the devices and allow for the lagging and loading.



(a) (b)

Figure 6-12: SEM image of a broken manifold channel (a) shows the negative tapering of the fins (b) shows the interface between the manifold and microchannels

X-ray images were taken of the packaged device to assess the bonding and placement of the devices and leads. Figure 6-13 is an x-ray image of a portion of the completed and diced wafer. The cut lines can clearly be seen along with some devices that have been bonded towards the top, the plenums, the inlet holes, and the manifold channels. The microchannels are a little too small to be seen in this image but they would

cross over the manifold channels under the devices. A device has already been removed at the bottom center of this image.

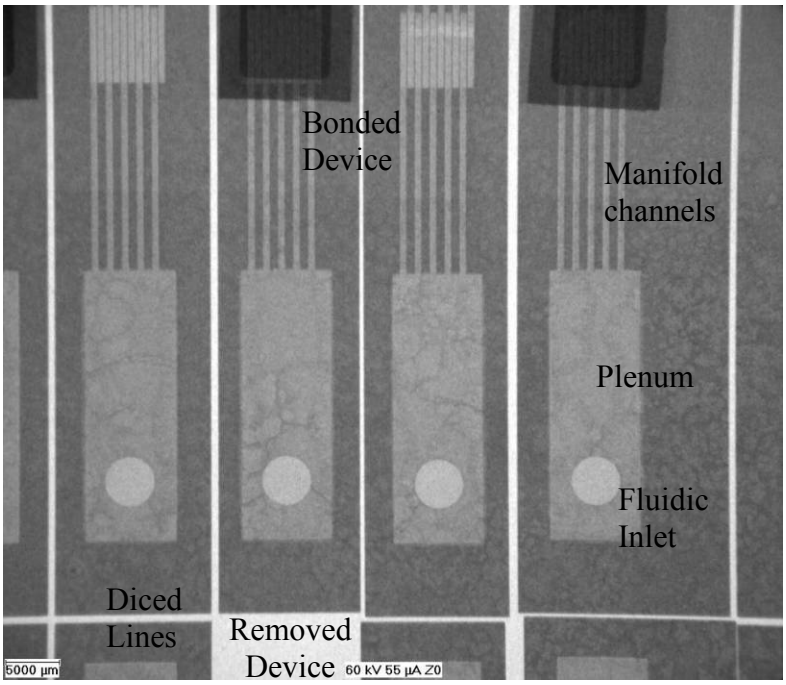


Figure 6-13: X-ray image of the cut wafer with devices attached

Figure 6-14 shows a depiction of the placement and the voiding in a typical lead attachment. Figure 6-14a shows the placement of the leads with the leads on the top slightly overlapping the base of the plenum, which has no effect on the cooler performance. Figure 6-14b and c show the voiding in both the base leads and top leads, respectively. The lighter colored areas indicate voids. The yellow arrow in the image points to a typical void. The voiding is not critical on the leads as they are not designed to be thermal conduction paths or to carry large currents, so the voiding should have no effect on the performance of the device.

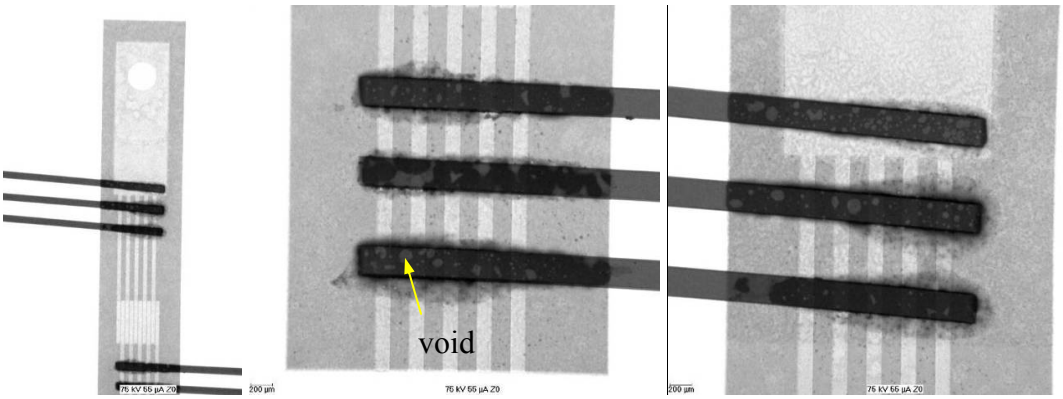


Figure 6-14: X-ray image of the placement and voiding in the leads

Figure 6-15 is an x-ray image showing standard voiding under the device, which is far less than 1%. The arrow in the image points to one of only a few very small voids on the image.

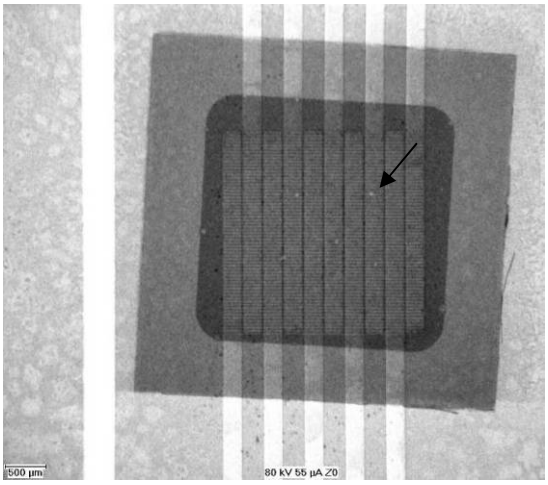
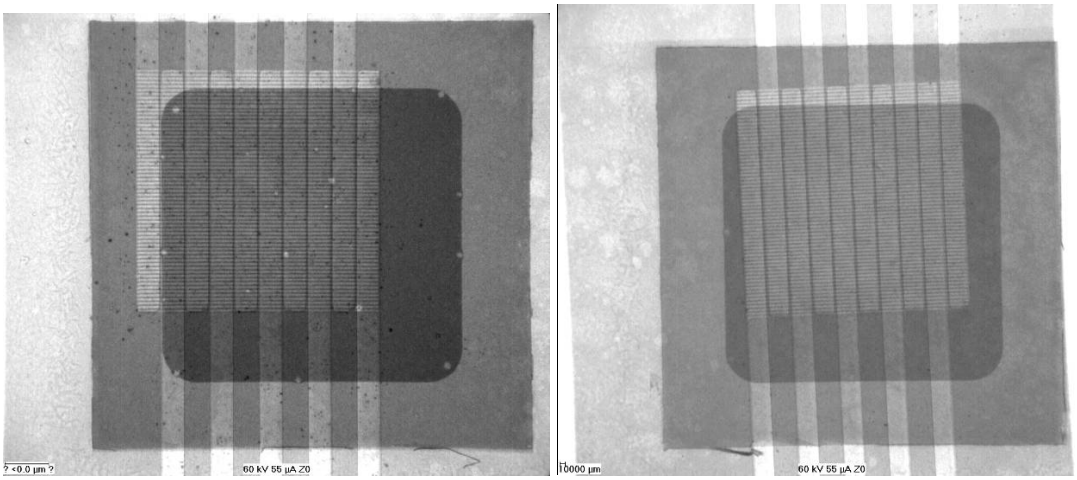


Figure 6-15: X-ray image depicting very little voiding in the eutectic bond of the SiC device to the microchannels, arrows point to the voids

Some devices did not have good alignment. Two examples are shown in Figure 6-16. The image on the right is misaligned in only one direction, and the image on the left is misaligned in two directions. The image on the left is the most misaligned device on the wafer.



(a) (b)

Figure 6-16: Bonded devices that are slightly misaligned

This misalignment was corrected for in the next version of microchannels as shown in the following chapter. The only thing used to align these devices was visual inspection. The etched squares were easy to see but ensuring the square was centered under the device was difficult, especially because it was possible for the devices to move during the bonding process.

6.6 Testing of MMC2

After fabrication was completed, the devices were tested experimentally. Modeling was also performed using the Floworks® module of Solidworks® modeling software. The experimental and numerical results were then compared.

6.6.1 Experimental Description

The experimental set-up is shown in Figure 6-17. It consists of a tank that is pressurized through a nitrogen line and holds room temperature demineralized water. The water leaves the tank through standard 3/8" tubing and is controlled (open loop) by a flow valve and pressure gauge. The water enters the microchannel manifold through a 1/16" capillary stainless steel tube and exits the manifold through the other end into a beaker to measure flow rate and outlet temperature of the water.

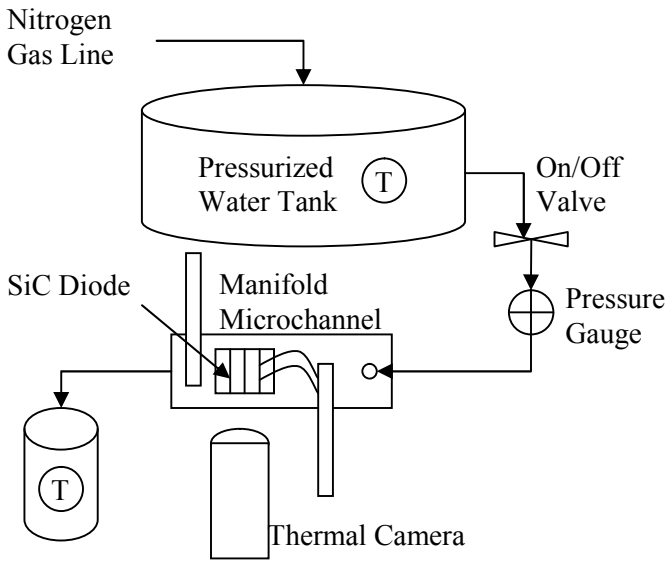


Figure 6-17: Schematic of the microchannel manifold test set-up.

A silicon carbide (SiC) diode is attached to the microchannel manifold cooler and is powered to heat the fluid. The voltage drop across the device and the current is measured such that the total power dissipation of the device is known. A photo of the device during operation is shown in Figure 6-18. In the picture, the purple glow is the SiC device during operation and the alligator clips are for the electrical connection.

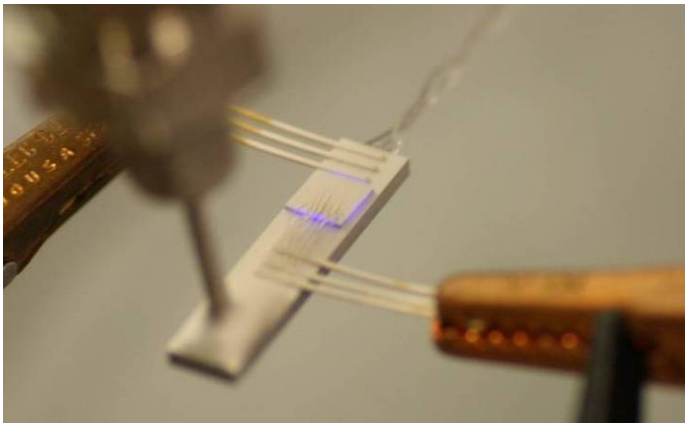


Figure 6-18: Photo of a device during operation

The flow rate was controlled with an Alicat brand flow controller that measures between 0 - 200 mL/min. It has been tied into Labview and controls and measures the flow rate to 2% of the full scale. The Labview block diagram is shown in Figure 6-19.

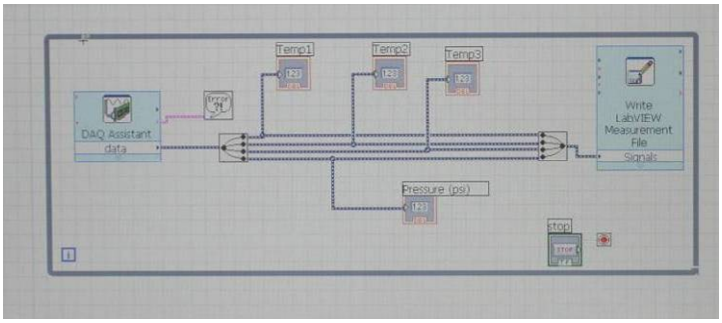


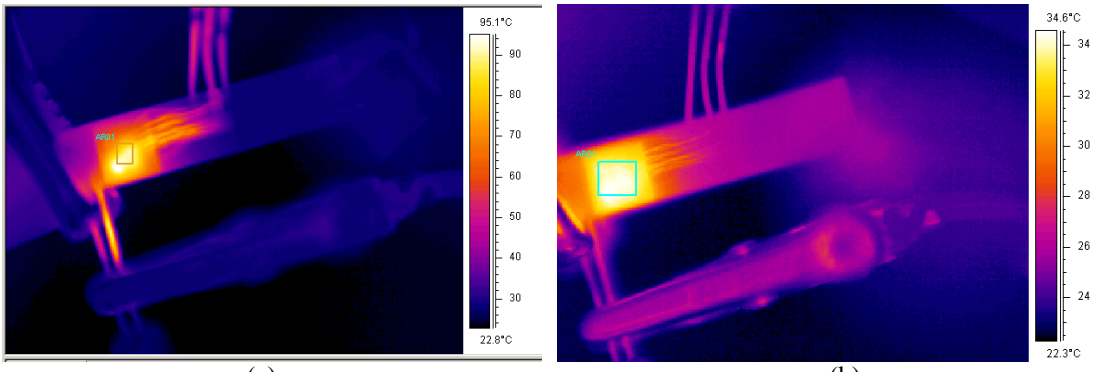
Figure 6-19: Labview block diagram

The pressurized water tank holds 11 liters of water and is rated up to 900 kPa. It is filled manually with demineralized water, sealed with an O-ring, and pressurized with nitrogen. The tank temperature is measured before the tank is sealed and assumed to have a constant inlet temperature for the test duration. The fluid flows through the channels, is heated by the powered SiC diode bonded to the structure, and then flows out through the

backside of the manifold where a thermocouple measures the outlet fluid temperature. The thermocouple is placed in the center of the fluid flow soon after it exits the cooler.

6.6.2 Experimental Procedure

In order to test the devices, they are connected to a power supply and DC current is used to heat the diodes by forward biasing. An oscilloscope is used to measure the voltage drop across the device at a supplied current. A thermocouple is used to measure the temperature of the water in the tank, assumed to be the inlet temperature. A thermocouple is placed in the fluid exiting the cooler to measure the outlet fluid temperature. A Labview code was written to read the inlet water temperature, outlet water temperature, ambient temperature, and pressure drop. The temperature across the top of the device is measured with a thermal camera. Figure 6-20 depicts a typical thermal camera image for a powered SiC diode on the manifold microchannel cooler. Each device is tested at a variety of pressure drops (between 0 and 138 kPa (20 psi)) and a variety of currents (from 1 to 5 amps).



(a) (b)

Figure 6-20: Thermal camera image of the SiC diode during operation

6.6.3 Experimental Test Results

The fabricated coolers were tested under a variety of fluid pressures and power densities. The largest analyzed pressure drop was 138 kPa but the cooler was run at pressures above 200 kPa with no fluid leakage, showing an adequate fluidic seal. No device leaked throughout its testing period indicating the seal is also good over time. A flow rate calculation test was performed by measuring how long the fluid passing through the cooler takes to fill a 100 mL graduated cylinder at different pressure drops; the results are shown in Figure 6-21. The flow rate increases with increasing pressure drop.

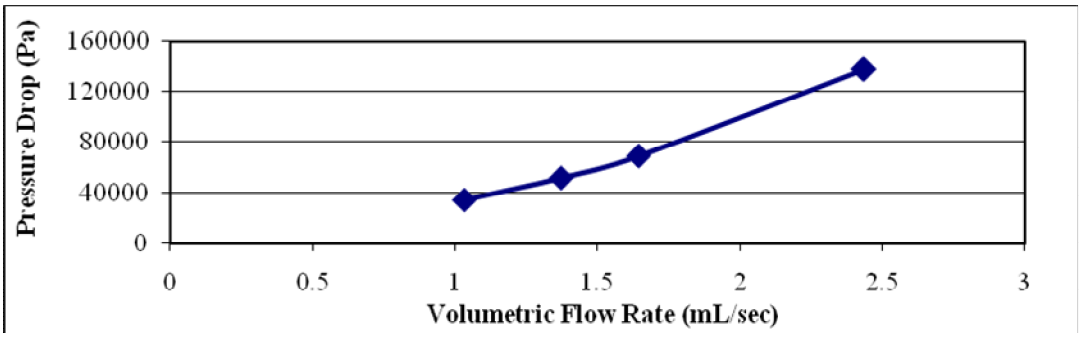


Figure 6-21: Graphical representation showing the flow rate versus pressure for the manifold microchannel cooler.

The theoretical flow rates of the microchannels and the manifold channels were calculated using the Hagen-Poisseuille flow model which has been adjusted for rectangular cross-section and is shown in Section 3.2. The results are shown in Figure 6-22 and show that the flow rates of the manifold microchannel design are about half of the manifold alone and 100 times faster than microchannels alone.

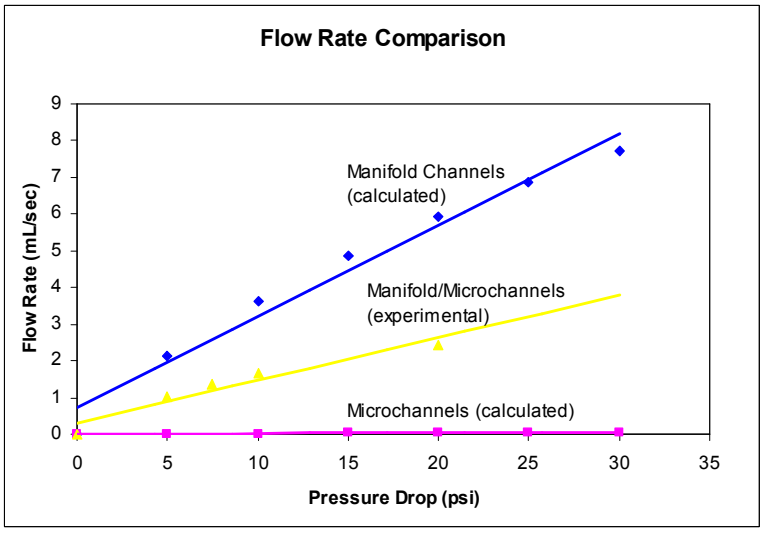


Figure 6-22: Flow rate comparison of the measured manifold microchannels compared to the manifold alone and the microchannels alone

Two important parameters of a heat sink when cooling a device are the thermal resistance and the change in the device temperature. Figure 6-23 shows how the input power affects the thermal resistivity. This initial data is very promising showing very low thermal resistivity values (<0.09 K/(W/cm^2)). The figure also shows that as the pressure is increased, the thermal resistivity decreases.

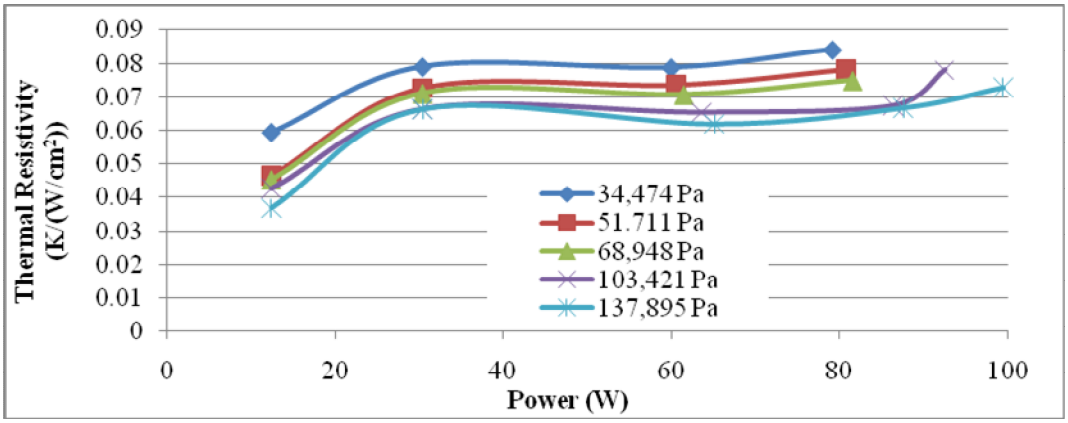


Figure 6-23: Graphical representation of the power versus change in the thermal resistance

Figure 6-24 shows how the chip temperature rises linearly based on input power and pressure drop. For an input power of 100 Watts, the chip temperature has only increased by about 45 ºC. At 30 Watts of power, the chip temperature has only increased 11.5 ºC. Therefore, experimental results show excellent cooling capabilities. As was shown in Figure 6-21, the pressure drop is directly dependent on the flow rate. So as the pressure drop or flow rate decreases, the rise in chip temperature increases. At a pressure drop of 138 kPa, the chip temperature rises by about 32 ºC, whereas, as 34.5 kPa, the chip temperature rises by about 42 ºC.

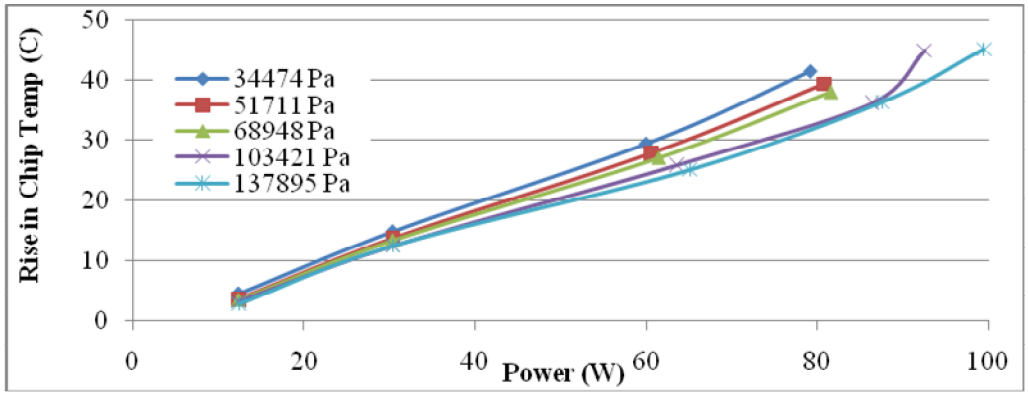


Figure 6-24: Graphical representation of the power versus the rise in chip temperature

A summary of the experimental results for one cooler can be seen in Table 6-2. The table shows results for a variety of powers and pressure drops with an inlet fluid temperature of 25 ºC. Key points to note from this set of data are that the change in fluid temperature never exceeds 12.6 ºC and the chip temperature rises by at most 45 ºC. Table 6-2 calculates heat flux using the cross-sectional area of the device (4 mm square) resulting in values up to 622 W/cm^2. If the heat flux is calculated using the cross section

of the active cooling area (2.5 mm square) then values would be just under 1600 W/cm^2 for this sample set.

Table 6-2: Summary of experimental results

Pressure (Pa)	Power (W)	ΔT_{fluid} (K)	ΔT_{chip} (K)	Heat Flux (W/cm^2)
34474	12.40	2.4	4.6	77.5
68948	12.40	1.6	3.5	77.5
103421	12.40	1.4	3.3	77.5
137895	12.40	1.1	2.85	77.5
34474	30.40	5.8	15	190.0
68948	30.40	4	13.5	190.0
103421	30.40	3.2	12.6	190.0
137895	30.40	2.8	12.6	190.0
34474	60.00	9.4	29.5	375.0
68948	61.50	6.7	27.15	384.4
103421	63.60	5.3	25.95	397.5
137895	65.10	4.5	25.15	406.9
34474	79.20	12.6	41.6	495.0
68948	81.60	9.2	38.2	510.0
103421	86.40	7.3	36.35	540.0
137895	87.60	6.4	36.5	547.5
103421	92.50	9.1	45.05	578.1
137895	99.50	7.9	45.25	**621.9**

In summary, the experimental results of MMC2 show thermal fluxes >600 W/cm^2 with an increase in chip temperature of 45 ºC. Also the AuSn eutectic bond never failed or leaked during testing; therefore, it has been shown to be an effective fluidic seal for the size of contact area here.

6.7 Modeling and Modeling Results

Modeling of the effect on performance of various dimensional parameters was shown in Chapter 3. The modeling presented here looks at just the specific geometry that was fabricated in this chapter. The modeling will be on a similar section of the device as was done in Chapter 3, except with a slightly shorter inlet and exit channels.

Simulations of heat dissipation and fluid flow in the assembly were conducted using the Floworks® module of Solidworks® modeling software. The model, illustrated in Figure 6-25, consists of a section of the chip and the portion of the cooling structure directly below the chip. The model employs symmetry in the transverse direction about both the inlet and outlet manifold channels, making the conservative assumption that heat is not dissipated transversely between manifold channel groups. This also includes the assumption that there is no transverse swirl across a channel. All 63 microchannels are included in the model. A distributed heat load was applied evenly across the surface of the chip, shown in yellow in the figure. The model was constructed of 611,298 fluid elements, 240,696 solid elements, and 338,678 partial elements.

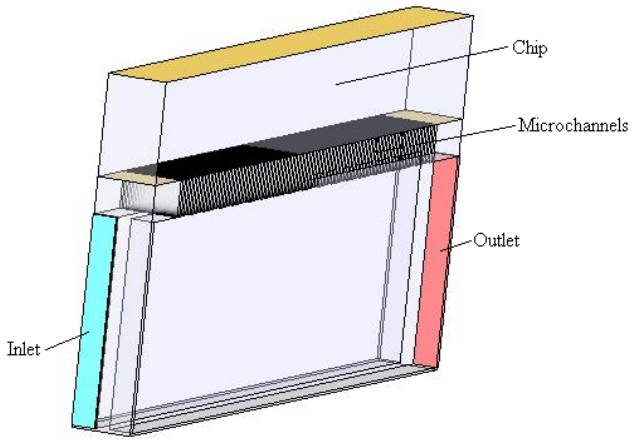


Figure 6-25: Model used for simulations

The parameter of primary interest in the simulations is thermal resistance as a function of imposed inlet and outlet pressure, a plot of which is shown in Figure 6-26.

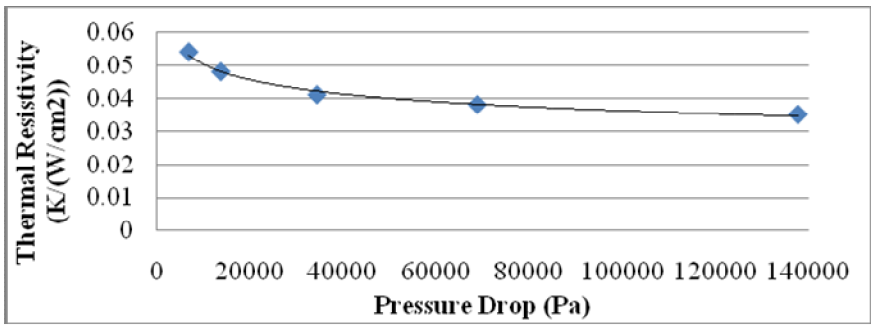


Figure 6-26: Thermal resistance as a function of pressure drop for 80 W power and 20 °C inlet water. For a pressure drop of 34474 Pa, the thermal resistance is 0.041 K/(W/cm^2)

The exponential shape of Figure 6-26 indicates there is a point of diminishing returns, such that an increase in pressure drop will give a marginal increase in thermal performance. For the case of 80 Watts, it is about 34744 Pa. The same data is plotted on a log-log plot shown in Figure 6-27, it shows a very linear relationship; therefore, it can be represented by the exponential equation shown on the graph.

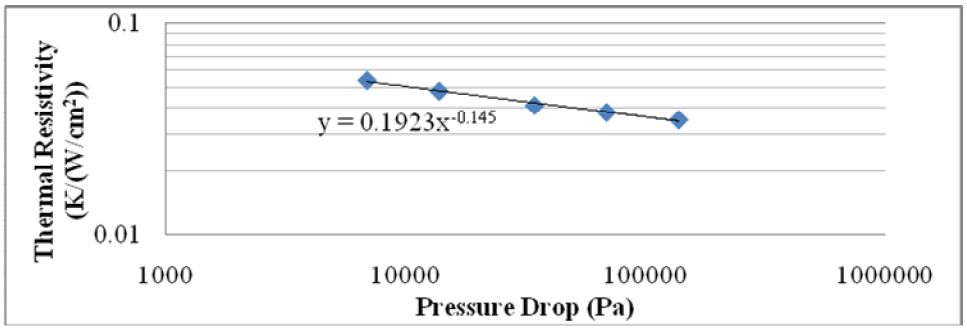


Figure 6-27: Log-Log plot of thermal resistance versus pressure drop showing a very linear relationship for 80 W power and 20 °C inlet water temperature.

Heat load for the pressure drops were adjusted iteratively such that a maximum temperature of about 125 ºC was reached in the chip and such that 100 ºC was never

reached in the fluid (boiling point). In Figure 6-28, simulated chip surface temperatures are shown as high as 123 ºC with fluid temperatures never exceeding 100ºC; therefore, the water never reached boiling for a power density of 2500 W/cm^2 at 34474 Pa. This image is a cross-section of the plane through the center of a manifold wall, perpendicular to the microchannels where the highest chip temperature occurs.

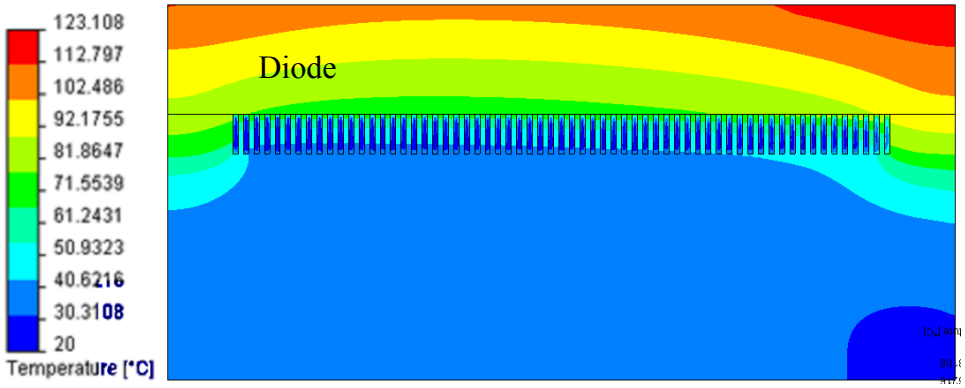


Figure 6-28: Simulated cross sectional temperature distribution of the chip and the cooling structure [34474 Pa pressure drop, 2500 W/cm^2 power density]

By its nature, direct cooling of the backside of the chip tends to produce high thermal gradients within the chip. Minimizing these gradients is required for providing consistent electrical performance and for avoiding the risk of damage due to internal thermal stresses which could cause die cracking or other failures. The effects of the temperature gradients through the device are yet to be studied in detail, but it is recognized that if determined to be sufficiently detrimental, they may limit the maximum operating power. Figure 6-29 is the same as Figure 6-28 but with an altered temperature scale that has been adjusted to the maximum and minimum chip temperatures to emphasize the temperature gradient within the chip.

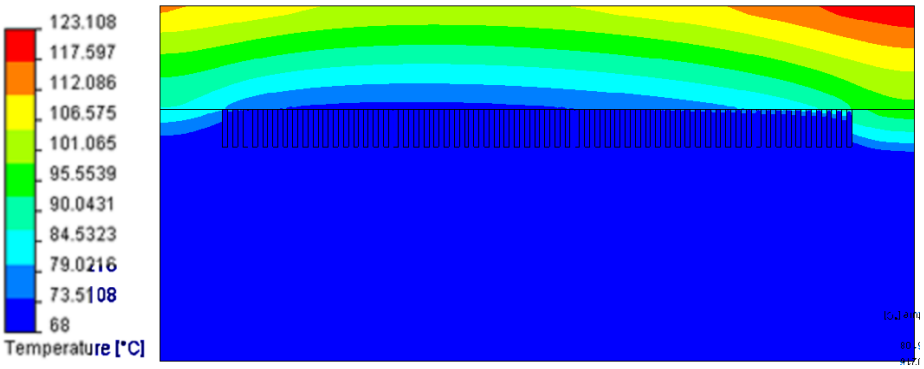


Figure 6-29: Simulated cross section emphasizing the temperature gradients within the chip [34474 Pa pressure drop, 2500 W/cm^2 power density]

6.7.1 Model of Effect of Fin Attachment

Due to the possibility of poor attachment or lack of attachment of the microchannel fins to the chip base, the question arose as to what benefit the attachment of the fins have in heat removal compared to a cooler where fluid flows directly over the chip backside. Therefore, a numerical study was performed on the effect of the fin attachment. Three cases were simulated:

a. Ideal case (all fins perfectly attached to the chip surface)

b. Worst fin attachment case (all fins separated from chip by 20 microns)

c. No fins at all (the fins were removed, but the space still exists to allow flow)

In all cases the chip maintained contact to the manifold substrate around the periphery of the chip. The simulations were performed with 20 ºC water at various pressure drops and an input heat load of 1500 W/cm^2, results provided in Figure 6-30.

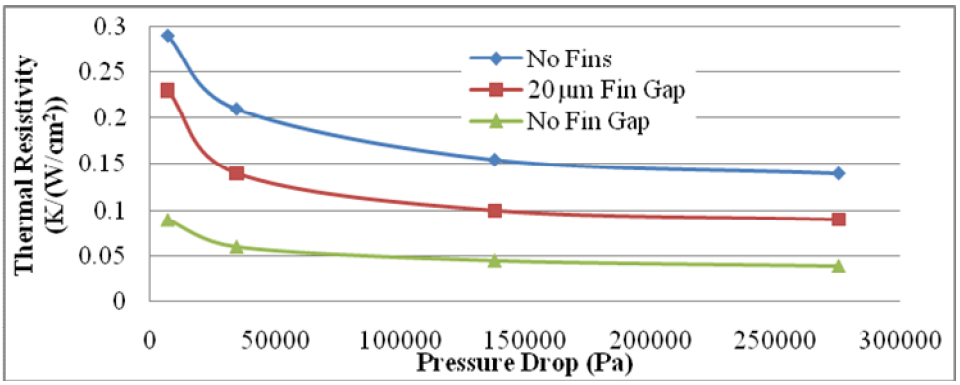


Figure 6-30: Effect of the gap between the fins

The results show that the fins do play a substantial role in heat removal. When the fins are detached the thermal resistance is at least doubled, and when the fins are removed the thermal resistance is at least tripled. Note that this study was not intended to examine cases of partial attachment.

6.7.2 Optimum Fin Analysis

The next question was if there was an optimum in terms of the microchannel geometry. Therefore, a numerical model was first run for various fin widths while maintaining a constant microchannel width. The microchannel with was chosen to be 60 µm and the fin widths were varied between 20 to 85 µm. In all cases, the pressure drop was assumed to be 137895 Pa with a power input of 80 W. The results in Figure 6-31 show that there is an optimum fin spacing under these conditions of about 63 µm.

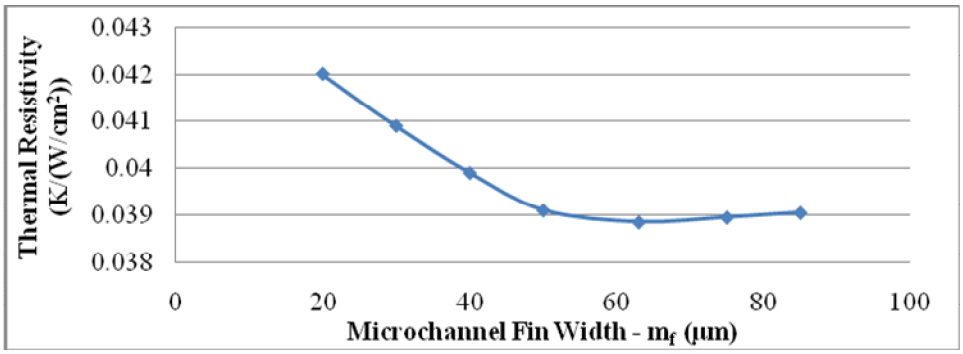


Figure 6-31: Thermal resistance compared to fin width to show optimum when m_w = 60 µm, Δp = 137,895 Pa, power = 80 W (890 W/cm^2) for a 3 mm x 3 mm device

The same experiment was repeated for a pressure drop of 13,789 Pa, and the results are shown in Figure 6-32 with the results for thermal resistance normalized to the lowest value. For the lower pressure, the optimum fin width appears to occur closer to 80 µm. Therefore, if the flow in the channel is expected to vary between 13,789 and 137,895 Pa, a fin width should be chosen to be between 60-80 µm. As can be seen in the graph, there is very little change in thermal resistance within that range, so choosing a value of about 70 µm should work out well for all pressure drops.

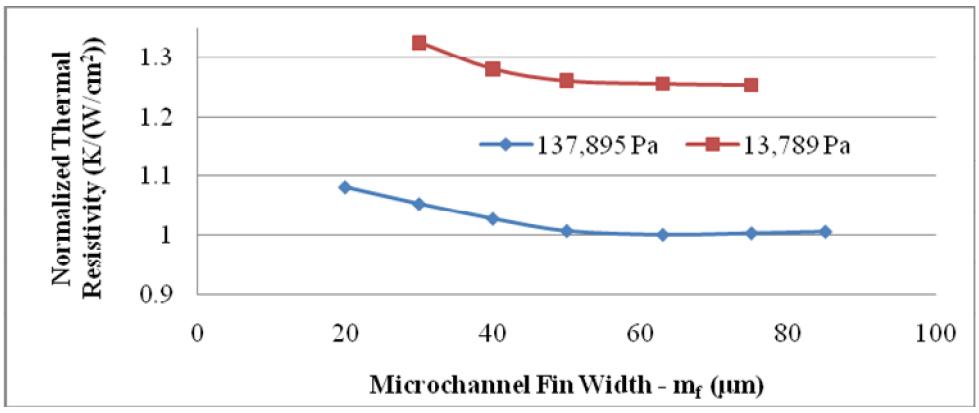


Figure 6-32: Normalized thermal resistance compared to fin width for m_w = 60 µm

6.7.3 New Dimensions Results

Due to the effects of clogging, larger microchannels are desirable. Therefore, simulations were performed to show the performance m_w = 100 µm, m_f = 20 µm. The thermal resistance compared to pressure drop is shown in Figure 6-33. The results show thermal resistance values less than 0.1 C/(W/cm^2) but not as good as the 20 µm channels.

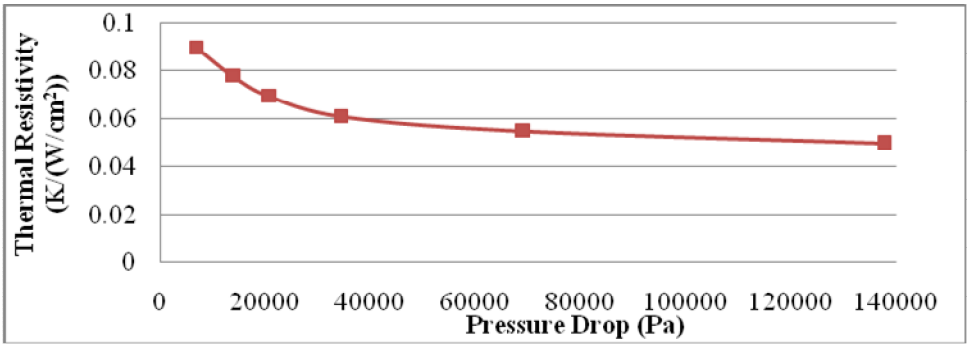


Figure 6-33: Thermal resistance versus pressure drop for m_w = 100 µm and m_f = 20 µm

The results of the 100 µm channels are compared to the previous results of the 20 µm channels and are shown in Figure 6-34. The performance of the 20 µm channels is clearly better, with lower thermal resistance values. But due to the effects of clogging, a 100 µm channel is more likely to be implemented in an actual application.

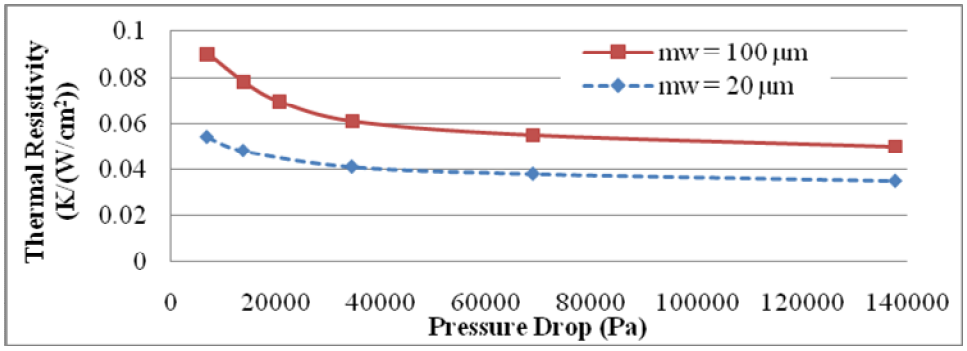


Figure 6-34: Thermal resistance versus pressure drop for 100 µm wide channels compared to 20 µm wide channels, both with 20 µm fin width

It is common that devices are only rated up to 125 ºC; therefore, maintaining their temperature below this is desirable to maintain performance within manufacturer specified limits and reduce failures. Figure 6-35 shows the maximum power that can be dissipated from the chip while still maintaining the chip temperature at 125 ºC for different pressure drops. For a 4 mm square chip size and a 34.5 kPa pressure drop, the power is limited to 1200 W/cm^2. If the pressure drop is increased to 138 kPa, the power dissipation could raise to almost 200 W. But since this is an exponential relation, the pressure drop would have to increase substantially to achieve power dissipations greater than 200 W.

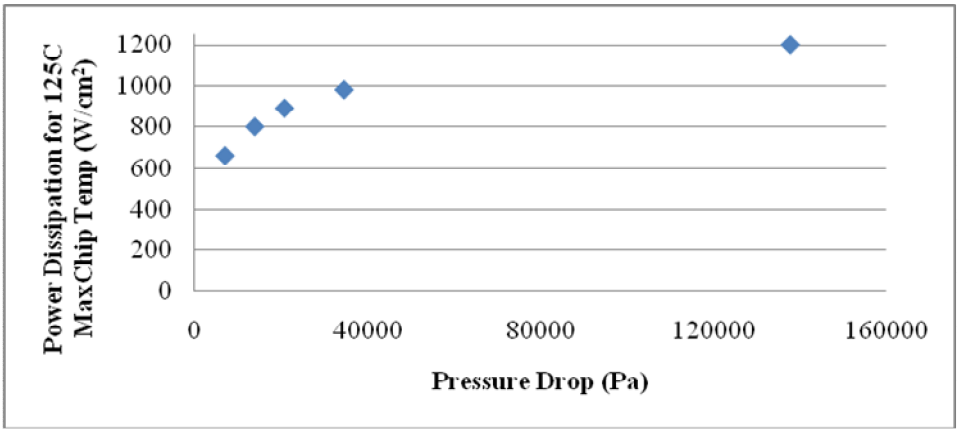


Figure 6-35: Power dissipation versus pressure drop to maintain chip temperatures less than 125C

6.8 Comparison of Experimental to Modeling Results

A simulation was run with the same parameters as one of the test cases: 87.6 W, 137,895 Pa pressure drop, and 25 °C inlet water temperature. The simulation results for these parameters are shown in Figure 6-36 where the maximum temperature of the chip is only slightly higher than 59 ºC when the cooling fluid is 25 ºC. This cross-section was

taken on the plane equidistant between the inlet and outlet manifolds. The chip is at the top of the image. This image shows the effectiveness of the chip cooling. A zoomed in image showing the fluid temperature distribution is also shown in the figure indicating a maximum fluid temperature of only 38 ºC. The image shows the fins are effectively pulling heat away from the device and transferring it to the fluid.

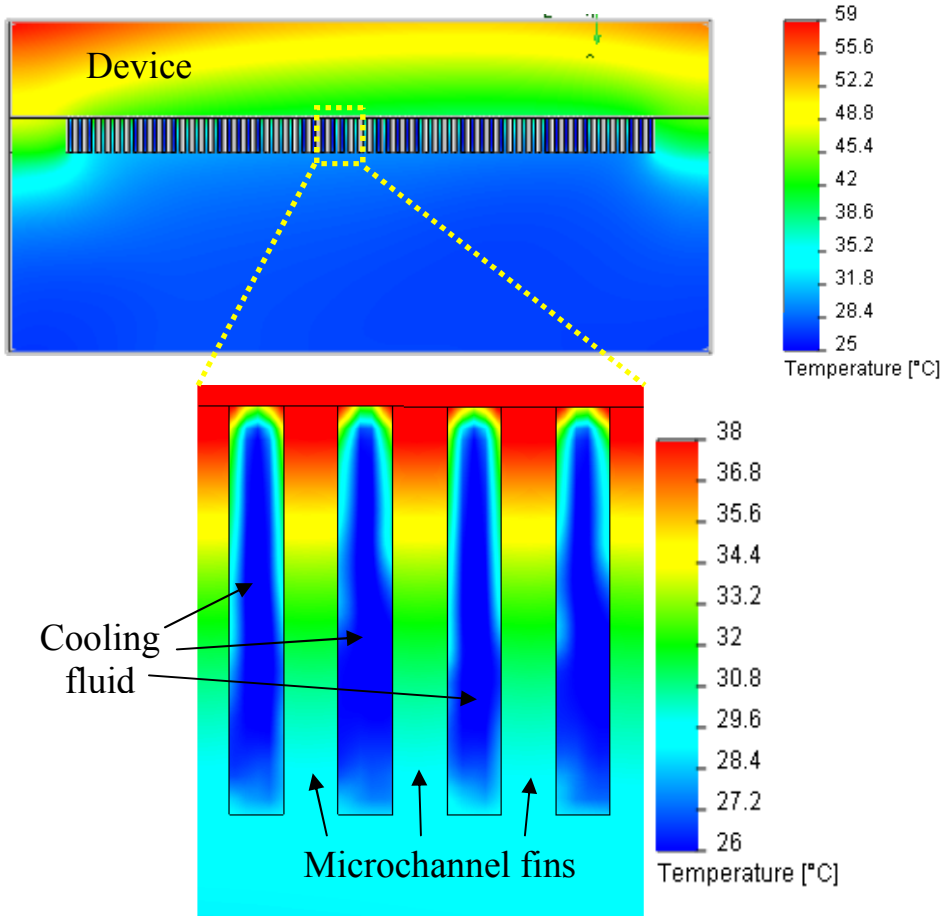


Figure 6-36: Temperature distribution in the chip and cooling structure with a larger image of the distribution within the microchannel fin structure [20 psi pressure drop, 890 W/cm^2 power density]

The experimental results at about 80 W are shown in Table 6-3 and are to be used for comparison to the analytical results.

Table 6-3: Experimental results for 80 Watts

Pressure Drop Psi	Power Watts	ΔT_{fluid} °K	ΔT_{chip} °K	Heat Flux W/cm^2	Thermal Resistance °K/(W/cm2)
5	79.20	12.6	41.6	495.0	0.084
10	81.60	9.2	38.2	510.0	0.075
15	86.40	7.3	36.35	540.0	0.067
20	87.60	6.4	36.5	547.5	0.067

Both the theoretical and experimental values of the thermal resistance versus pressure drop are plotted on a log-log plot in Figure 6-37. The linear trend correlates well between the experimental and simulation results. However, the experimental results do not show thermal resistance values as low as the simulation. The discrepancy could caused by heat lost to the ambient, heat lost through the leads, poor bonding between the chip and microchannels, or non-optimum flow in the channels.

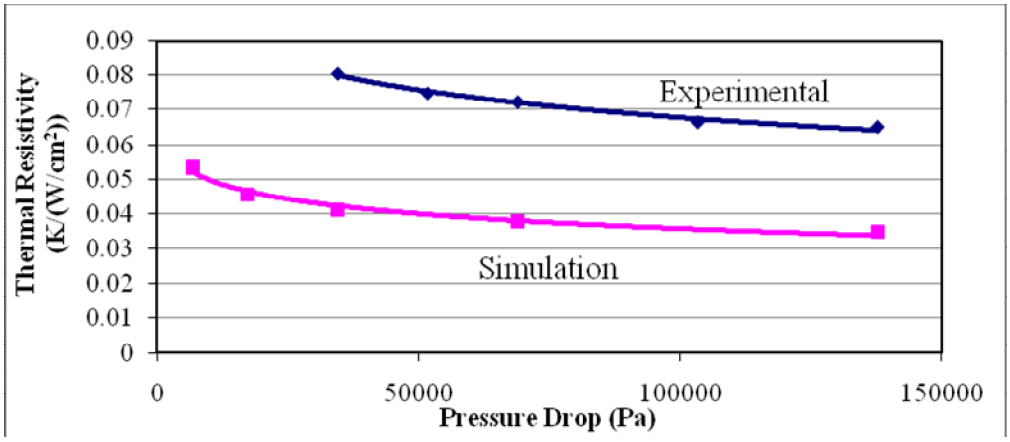


Figure 6-37: Plot of the pressure drop vs. thermal resistance comparing experimental to simulation

The simulation shows the chip temperature rising 34 ºC for an input power of 80 W. The experimental results show the chip temperature rising 40 ºC for an input power of 87.6 W. This is only a 6 ºC difference between the simulation and experiment,

and considering the different in power, it would be even closer. The simulation calculated the average temperature rise of the fluid to be 1.5 ºC and the experimental calculated an increase of about 6.4 ºC. A cross-section of the inlet manifold is shown in Figure 6-38. The fluid inlet is on the right side of the image. Therefore the triangular area of slight temperature increase is where the fluid is stopped and forced over to the exit manifold.

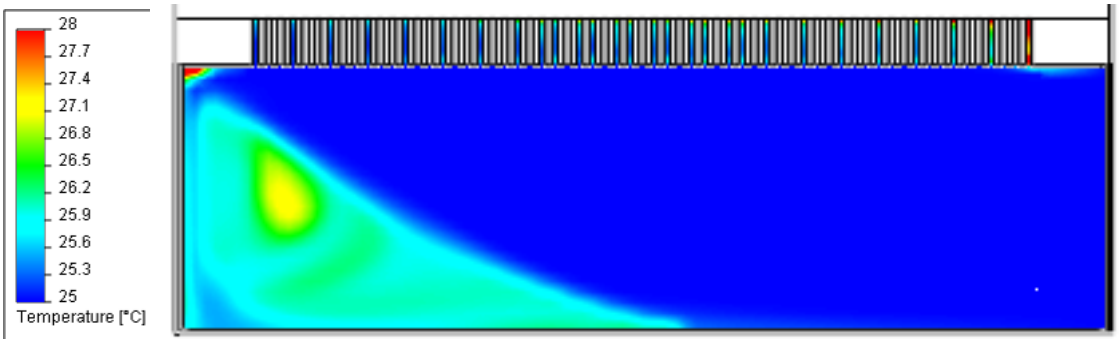


Figure 6-38: Cross section of the inlet manifold

A cross section of the outlet manifold is shown in Figure 6-39.

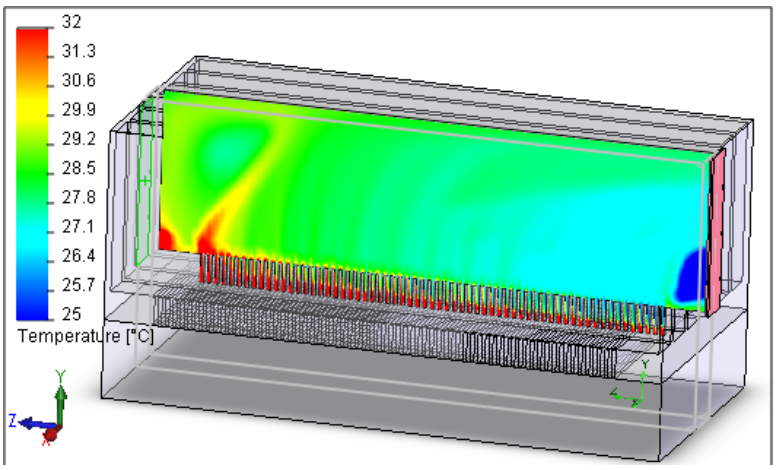


Figure 6-39: Cross section of the outlet manifold with fluid exiting to the right side.

6.9 Conclusion

In conclusion, the cooler has shown excellent thermal results with thermal resistances less than 0.1 C/(W/cm^2) and heat fluxes over 600 W/cm^2 with an increase in chip temperature of only 45 ºC. The fabrication procedure is easily reproducible and uses standard MEMS techniques. The AuSn eutectic bond has been shown to be an effective fluidic seal to pressure drops above 207 kPa. Simulations show that the water temperature does not reach the boiling point and the device stays under 125 ºC for a heat flux of 2500 W/cm^2. The active cooling area is about the size of the active area of the chip. Flow rates have been calculated to be about half the rate of the manifold alone and 100 times faster than the microchannels alone.

The experimental results showed that MMC2 performed very well. A single SiC diode was powered and cooled by flowing water through a manifold microchannel that was MEMS fabricated into a silicon wafer. There was no electrical isolation between the device and the cooling fluid. After fabricating and testing it was determined that some improvements to the design should be made. MMC2 uses microchannels that are only 20 μm wide and are therefore susceptible to particulate clogging which can block the flow through the channels. Slightly larger channels or channels of varying dimensions would help to alleviate this problem while also reducing the pressure drop due to the increase in hydraulic diameter. The SiC diode was also found to create uneven heating along the die surface so it is going to be replaced with a device that creates a more evenly heated surface to reduce the measurement error. The design will also be changed to increase the number of devices that can be fabricated on each wafer and to allow for a multi-chip module. The square inlets will also be replaced with a design that would

reduce the pressure drop in the manifold channels to allow for more efficient cooling. Each of these changes is discussed in detail in Section 7.1.2 below and has been incorporated into the next design, MMC3.

MMC2 was designed with no electrical isolation layer and the experimental results showed it had performed very well. Certain applications do not require isolation between the device and the fluid. Such applications could include when a dielectric fluid is used, or when the devices do not have a backside electrical contact, or when only one chip is being cooled by the fluid. But other applications do require electrical isolation to the fluid which is why both MMC3 and MMC4 were fabricated. Applications that would require electrical isolation could include multi-chip modules where electrical shorting could occur between devices or modules that utilize a conductive cooling fluid. The following section discusses MMC3, a cooler that utilizes an oxide membrane as the electrical isolation layer.

7 Manifold Microchannel Version 3 (MMC3)

The results from MMC2 showed very good performance but some applications require an electrical isolation layer between the fluid and the device. Therefore, MMC3 was designed with an incorporated electrical isolation layer in the form of a silicon dioxide membrane. Some changes were also made to the basic design: incorporating larger and various sized microchannels, fabricating the manifolds and the microchannels in two separate wafers, and using a ceramic chip resistor to allow a more uniform temperature distribution. Other changes were also made that allowed lower pressure drop, more devices per wafer, and both a single or dual chip design.

7.1 Design of MMC3

The new dual device MMC3 design is shown in Figure 7-1. Figure 7-1a shows the top view of MMC3 with the devices on the top. Figure 7-1b shows the view from the bottom into the plenum and the manifold channels. Both images show the fluid inlet and outlet holes.

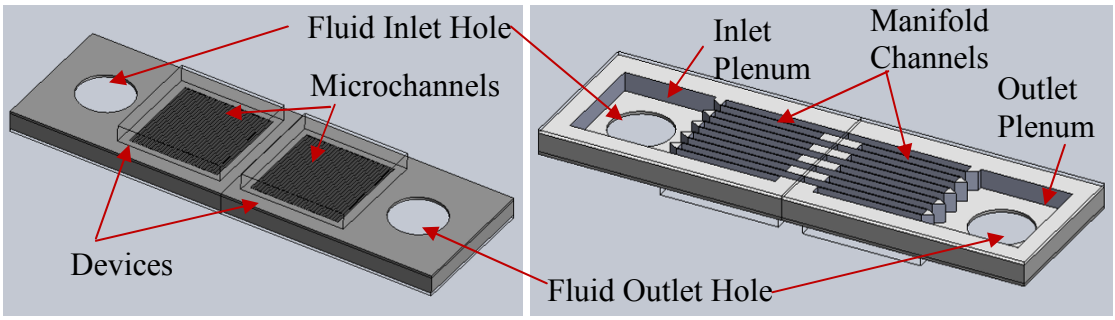


Figure 7-1: Schematic of MMC3 (a) view from the device side (b) view from the backside

A cross-section with the thickness dimensions and flow profiles is shown in Figure 7-2. Both the manifold and microchannel wafer are made of silicon and are 1 mm and 150 µm thick, respectively. The manifold wafer is capped on the bottom with a 175 µm thick Pyrex wafer. The fluid flows in through the entrance hold on the left side, it then enters into the microchannels under the first device, cooling the device and heating the fluid. The fluid then enters back into the manifold channels and then into the microchannels under the second device where it cools the second chip and is further heated. It then enters back into the manifold channels before exiting the device through the exit hole. Due to this structure, it is expected that the second chip will be hotter than the first chip, especially at lower flow rates.

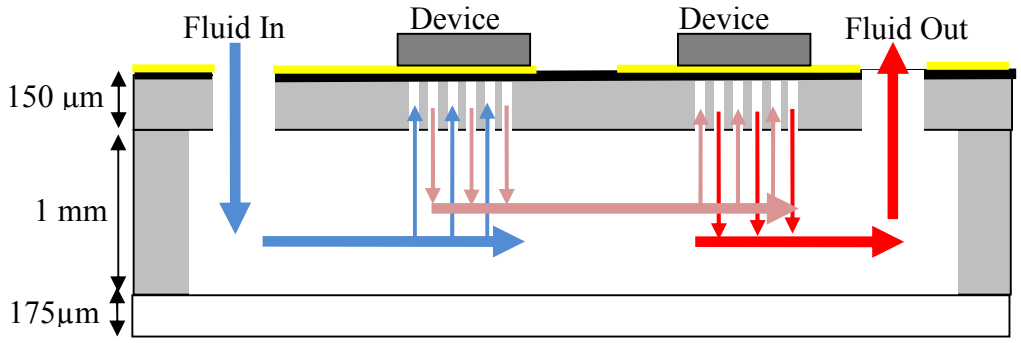


Figure 7-2: Cross-section of MMC3 with the wafer thicknesses and fluid flow

7.1.1 MMC3 Dimensions

The major dimensions of the MMC3 structure are shown in Table 7-1. The device is a square chip that is 6.22 mm on each side. The microchannels are designed to cover an area of 5.45 mm on a side, leaving 0.39 mm between the edge of the microchannels and the edge of the chip on each side. This area is used for the device bonding and fluidic

sealing of the channels. This area is substantially less than in the previous design, but this design has better alignment procedures to account for this difference. The alignment procedure will be discussed later in this chapter. The size of the manifold channels does not change across the wafer, only the microchannel dimensions vary. There are four inlet and four exit manifolds which are 550 μm wide (M_w) with 150 μm fins (M_f) and a depth of 1 mm. The cross sectional area of each manifold channel is 0.55 mm^2. All of these dimensions are summarized in Table 7-1.

Table 7-1: Major dimensions for MMC3

Chip Width	6.22	mm
Chip Length	6.22	mm
Spacing left around chip edge	0.39	mm
Manifold space	5.45	mm
μchannel Space	5.45	mm
Manifold Width (M_w)	550	μm
Manifold Fin Width (M_f)	150	μm
Inlet/exit manifold channels	4	
Manifold Height (M_h)	1	mm
Cross sectional Area	0.55	mm^2
Microchannel Height (m_h)	0.15	mm

Unlike the manifold channels, the microchannels have varying dimensions, which are shown in Table 7-2. The microchannel width (m_w) changes from 40 to 120 μm in increments of 20 μm. The microchannel fin width (m_f) changes from 40 to 100 μm, also in increments of 20 μm. There is a control device, labeled "blank," which has no microchannels and is used to compare the effects of pressure drop and thermal performance to the devices with microchannels. All microchannels are 150 μm deep. Each of the microchannel width dimensions is paired with each of the fin dimensions. The number of microchannels is then determined to be the maximum number that can fit

in 5.45 mm without going over. The microchannel area is then calculated by multiplying the microchannel width (m_w) by the depth (150 μm) then by the total number of microchannels.

Table 7-2: Table showing the different sizes of microchannels

	m_w (μm)	m_f (μm)	N_{ch}	μchannel Area (mm^2)	D_h (μm)	Re
1	40	40	68	0.408	63.2	1027.9
2	40	60	55	0.33	63.2	1270.8
3	40	80	46	0.276	63.2	1519.5
4	40	100	39	0.234	63.2	1792.2
5	60	40	54	0.486	85.7	1171.1
6	60	60	45	0.405	85.7	1405.3
7	60	80	39	0.351	85.7	1621.5
8	60	100	34	0.306	85.7	1860.0
9	80	40	45	0.54	104.3	1283.1
10	80	60	39	0.468	104.3	1480.5
11	80	80	34	0.408	104.3	1698.2
12	80	100	30	0.36	104.3	1924.7
13	100	40	39	0.585	120.0	1362.1
14	100	60	34	0.51	120.0	1562.4
15	100	80	30	0.45	120.0	1770.7
16	100	100	27	0.405	120.0	1967.4
17	120	40	34	0.612	133.3	1446.6
18	120	60	30	0.54	133.3	1639.5
19	120	80	27	0.486	133.3	1821.7
20	120	100	25	0.45	133.3	1967.4
Blank	5450	0	1	0.8175		

Both the Reynolds numbers and hydraulic diameters were calculated for both the manifold and the microchannels at the highest flow rate of 400 mL/min. The results are shown in the last two columns of Table 7-2. Clearly all Reynolds numbers are less than 2300 so it is considered laminar flow. The same calculations were performed on the manifold channels. The manifold channels are 550 μm wide and 1 mm deep so they have a hydraulic diameter of 710 μm and at 400 mL/min (the fastest flow rate); the Reynolds

number was calculated to be 2142. This number is only slightly less than 2300 but is still considered to be in the laminar region.

The placement of the different microchannel sizes on the wafer is shown in Figure 7-3. The smaller microchannels were placed around the edges and the larger ones towards the middle of the wafer to minimize the effects of loading and lagging during the DRIE process. Each spot on the wafer indicates a two-chip device with identical microchannels under each device with the exception of the device on the bottom left side of the wafer which has different microchannel dimensions under each device. These were chosen because they are two of the smallest channels and one of the goals of this version of microchannels is to increase the channel size to minimize the clogging.

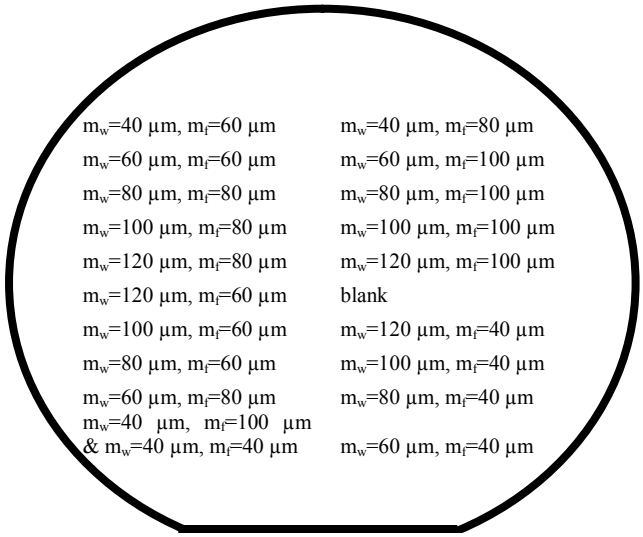


Figure 7-3: Depiction of the varying microchannel sizes across the wafer

7.1.2 Oxide Isolation Layer

A major difference between this device and MMC2 is that MMC3 has an oxide layer for electrical isolation between the chip and cooling fluid. As was previously

discussed, in some applications it is desirable to incorporate some sort of electrical isolation if a conductive fluid is used to reduce the possibility of electrically shorting devices thus causing electrical failure. Other applications do not require the electrical isolation; therefore, whether or not to incorporate it is application dependent. The electrical isolation layer increases the thermal resistance and so should only be incorporated if the application requires it.

If a dielectric fluid is used, the isolation is not necessary. Dielectric fluids are very common for cooling applications, but they have the problem that their thermal properties are substantially worse than water. Additionally, they are more viscous and therefore create larger pressure drops and the need for a larger pump. They are also substantially more expensive than water, harder to come by, and require special testing equipment to use them. For these reasons, using water is desirable but then an electrical isolation would be necessary which is why MMC3 was designed with a dielectric layer.

MMC3 utilizes an oxide layer as the isolation layer because of its availability in MEMS fabrication. It is simple to create an oxide layer by either growing a thermal oxide or depositing a CVD oxide. MMC3 uses both a thermal and a CVD oxide. A 1.5 μm thermal oxide was grown on the wafer followed by depositing a 2 μm PECVD oxide. This thick oxide is needed to stand off the large voltage from the fluid. A thermal oxide can hold off $>1x10^7$ V/cm and a PECVD oxide can hold off about $1x10^6$ V/cm. This means that the total voltage hold off of the 3.5 μm thick oxide stack is 1500 V for the thermal oxide and 200 V for the PECVD oxide. This equates to a total voltage hold off of over 1700 V. The current power requirements of the Army are to hold off greater than 1200 V, which means that this would be a sufficient thickness.

An additional benefit of the oxide layer is its ability to be used as an etch stop during the DRIE process. This allows it to easily be incorporated into the fabrication sequence when a three wafer stack is used, as it in MMC3.

The disadvantages of using an oxide are the poor thermal properties of the oxide and the large amounts of stress that can occur in thick oxides. The thermal conductivity of thermal and PECVD oxides are 1.4 W/mK and 1.1 W/mK, respectively, which is very low. But since the layer is very thin, only 3.5 μm, the effect should be small but not negligible. Another disadvantage of the oxide membrane is that it is difficult to bond a chip to in that a standard die bonding processes cannot be used. Due to the disadvantages of using an oxide, the cooler was also fabricated with an AlN ceramic isolation layer replacing the oxide. This is discussed in further detail in the next chapter and is MMC4.

7.1.3 Changes from MMC2

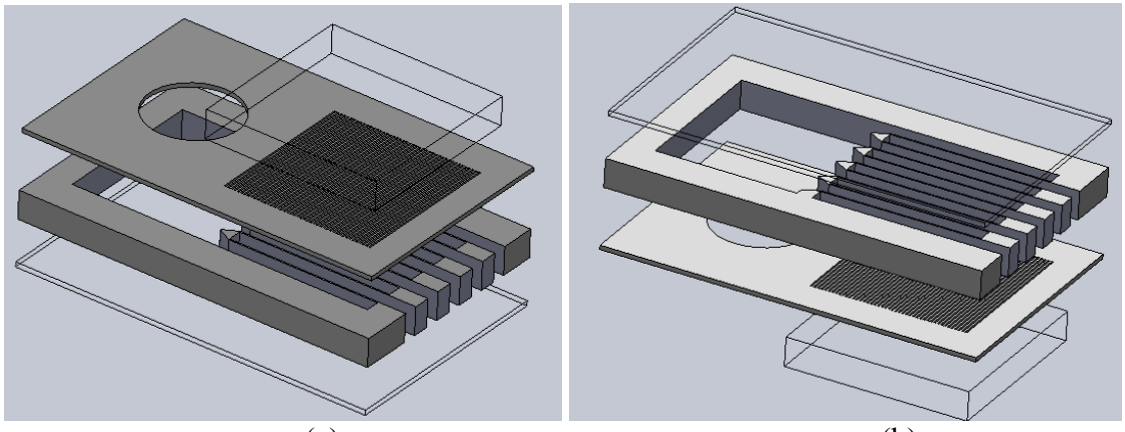
After fabricating and testing MMC2, it was determined that some changes should be made to improve the next design. The main changes that were include:

- Three wafer stack to reduce DRIE effects of lag and load and allow uniform depth
- Increased microchannel size to reduce clogging
- Chip resistor to allow for temperature uniformity
- Pyrex for visual inspection of channels
- External electrical connections to maximize number of devices per wafer
- One or two chip capability
- Triangular inlets to reduce pressure drop
- Larger inlet tube to reduce pressure drop

Each of these changes is discussed in detail below.

7.1.3.1 Three wafer stack

The new design, MMC3, incorporated a three wafer stack as opposed to the previous two wafer stack which allows the manifold and microchannels to be fabricated in separate wafers. In MMC2 they were fabricated in the same wafer. A schematic of the MMC3 wafer stack is shown in Figure 7-4. The bottom wafer is a thin Pyrex wafer whose purpose is mainly fluidic sealing of the device. The center wafer is a 1 mm thick silicon wafer containing the manifold channels. The top wafer is a 150 μm thick silicon wafer containing the microchannels. The device is bonded on top of this wafer. The two main benefits of using a three wafer stack are to allow for constant depth across the wafer and also to allow for an oxide membrane. The depth is uniform because each wafer is etched completely through. Therefore, the 1 mm wafer is etched to a constant 1 mm throughout, which eliminates the effect of lagging and loading on the etch depth. Since the wafer does not have to be etched from both sides, it is possible to leave a thin oxide membrane on one side of the microchannel wafer for electrical isolation.



(a) (b)

Figure 7-4: Exploded view of MMC3 showing the three wafer stack and the through etch of both the manifold and the microchannel wafers.

7.1.3.2 Increased microchannel size

In MMC2, the microchannels were 20 μm wide with 20 μm fins, which is very small and can easily be affected by particulate clogging. Larger channels are more desirable from a system view because smaller channels create the need for filters in the system, making it more complicated. The new channels range in size from 40 to 120 μm and so are less likely to clog. The pressure drop will also be reduced by increasing the channel size. However, the larger channels will reduce the performance.

7.1.3.3 Chip resistor allows for temperature uniformity

Using a ceramic chip resistor instead of a SiC diode allowed for increased surface temperature uniformity. The previous SiC diodes often had hot spots on their surface, which can cause disparities during testing. Additionally, the cost of a ceramic chip resistor is substantially less than a SiC diode. The chip resistor, whose datasheet is shown in shown in Appendix F, is a CR style from American Technical Ceramic (ATC). It has an operating temperature range between -55 to 155 ºC and is made of an AlN substrate with a proprietary thin film resistive coating and silver plated terminals.

7.1.3.4 Pyrex capping wafer

The back capping wafer of the wafer stack up is a Pyrex wafer which is anodically bonded to the silicon manifold wafer. The previous design, MMC2, incorporated a silicon wafer which was eutectically bonded. The Pyrex allows for visual inspection of the microchannels after processing. Anodic bonding of Pyrex to silicon is a very well-known and established process and creates a virtually void-free bond. The Pyrex also acts as an etch stop during the DRIE etching process of the manifold wafer.

Pyrex has a very low thermal conductivity, which is beneficial during testing because it minimizes the conduction through the bottom of the device, allowing more heat to be transferred into the fluid. A disadvantage of the Pyrex is that it has a slightly different CTE to silicon which could lead to stresses in the device. The CTE of silicon is $3x10^{-6}$/ºC and Pyrex is $3.25x10^{-6}$/ºC. Therefore, all subsequent processes after the anodic bonding must not have extreme temperatures due to the possibility of cracking.

7.1.3.5 Maximize Number of Devices per Wafer

In comparison to MMC2, MMC3 has been designed with the electrical connections to be connected externally to the device. Due to the nature of the chip resistor, both of the electrical connections are on the top side of the device. The SiC diode used previously had one of its electrical connections on the backside of the die, so external connections were difficult. In MMC3, wirebonds connect the top side of the resistor to external copper straps. The two benefits of the external connections are to allow for more devices per wafer and to eliminate the CTE mismatch of the connections to the silicon.

More devices per wafer are possible because wafer real estate is not used for the electrical connections, only for the devices and the fluidic inlets and outlets. In MMC2, about half of the area of each device was used for electrical connections and that has been eliminated in this design. In MMC2, silicon cracking was caused by the CTE mismatch between the silicon and metal connections. In MMC2, three skinny leads were used to work around this problem, but in the current design, this problem has been eliminated by using external connections instead of on-device connections.

7.1.3.6 One or Two Chip Capability

A benefit of this design is the capability for either a single or two chip module, as shown in Figure 7-5. To make the two-chip device into two single-chip devices, the device can be cut at the cut line shown in the figure with a diamond bladed dicing saw. With this option, it can be fabricated as either a single chip or as two chips to make testing easier. It can also be first tested as two chips in series, then cut apart and tested again as two single chip devices.

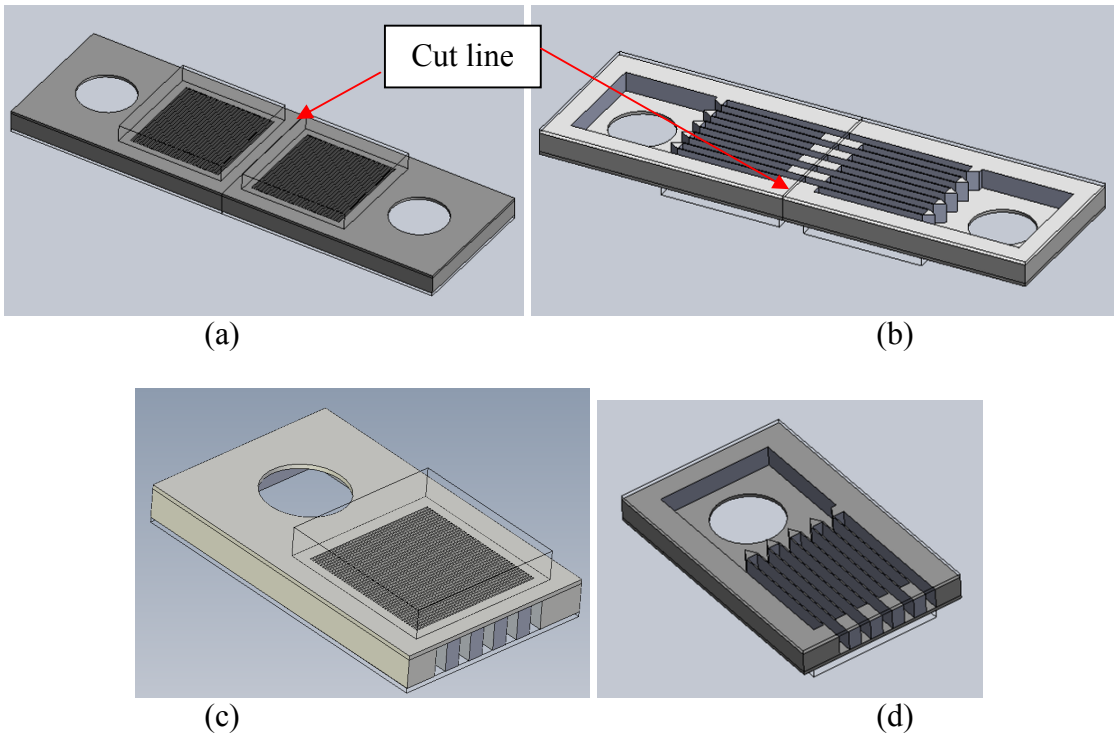


Figure 7-5: Schematic depicting the multichip capability (a) view from the top (b) backside view with the cut line shown (c) single device top side (d) single device backside

7.1.3.7 Triangular Inlets

Another design feature that was incorporated into MMC3 is triangular inlets (Figure 7-6) which allows the fluid to enter the channels with less recirculation, thus reducing the pressure drop. The flow path is depicted in the image with yellow arrows. The triangular shapes were created by simply changing the photolithography mask.

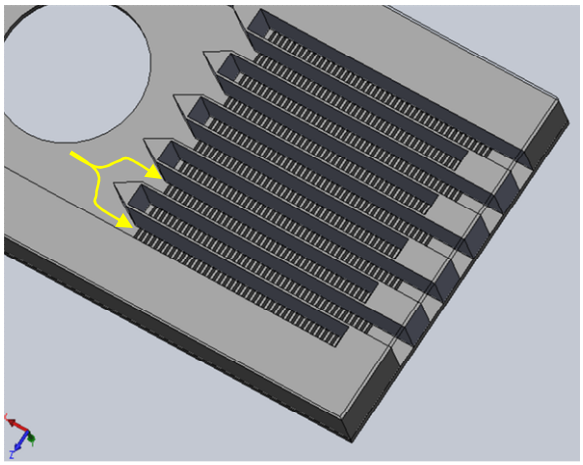


Figure 7-6: Schematic depicting the triangular fluidic inlets (yellow arrows indicate flow path)

7.1.3.8 Larger Inlet Tube

The size of the inlet tube was also increased to minimize pressure drop before the fluid enters the device. This larger size was possible because of the larger device and the larger plenums incorporated into this design. The inlet pressure is measured before the inlet tube and so minimizing the pressure drop between the point where the fluid is being measured and the channels reduces measurement errors.

7.2 Alignment Technique

Since a single wafer was used in MMC2 for both the microchannels and the manifold channels, it was not necessary to align the wafers to each other but in MMC3, this is now necessary. Also, the spacing allowed for misalignment of the device is substantially smaller in MMC3 than in MMC2, so it is also necessary to create a template on the top to align the devices. The wafer shown in Figure 7-7 is the wafer that was used to align the devices on the topside of the microchannel wafer. It was fabricated by patterning a masking PR then etching using a DRIE process through a standard single side polished 500 μm silicon wafer.

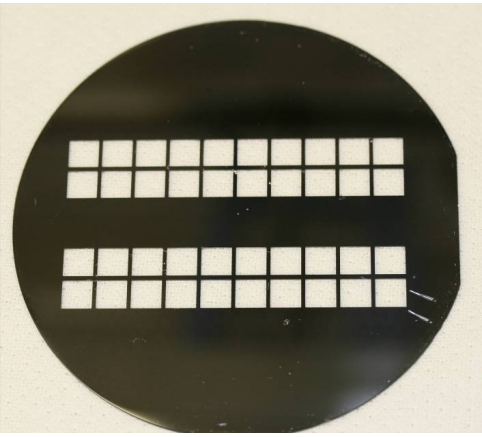
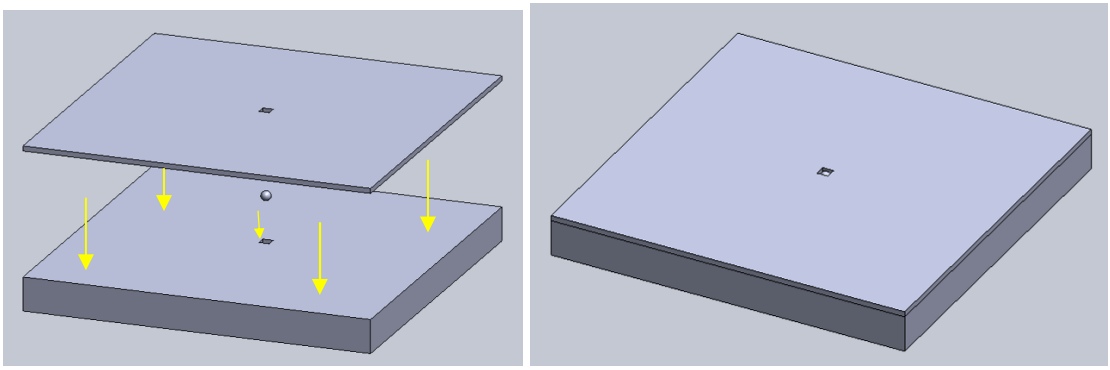


Figure 7-7: Top wafer for device alignment

The technique that was used to align the wafers to each other uses small stainless steel ball bearings which are manufactured to be exactly 280 μm in diameter. [32] The assembly is depicted in Figure 7-8 indicating the ball bearing is dropped into a square hole that is etched to the depth of half the diameter of the ball bearing (about 140 μm). There are four holes spaced equally around the perimeter of the wafer and a ball bearing

is dropped into each hole. Matching holes are etched into the 150 µm thick microchannel wafer and then gently placed on top and moved around until it lines up with the balls and falls securely into place.



(a) (b)

Figure 7-8: Depiction of the ball bearing alignment technique (a) exploded view (b) bonded view

7.3 Fabrication Sequence

To fabricate MMC3, it was necessary to etch through a 1 mm thick silicon wafer. Initial attempts were made to etch through the wafer using a single etch from one side of the wafer. Due to the effects of negative tapering and masking limitations it was determined that a two-step etch was necessary. The first step etches over half the wafer before being bonded to a Pyrex wafer. In the second step, the etch pattern is aligned to the opposite side of the wafer and a second DRIE etch is completed through the remainder of the wafer. The loading during the second DRIE etch has been reduced by adding a square to the inside of each plenum that will drop out.

Since the manifold channels and the microchannels are now fabricated in two separate wafers, the fabrication sequence is shown in three parts: Figure 7-9 shows the

fabrication sequence for the 1 mm thick manifold wafer; Figure 7-13 shows the fabrication sequence for the 150 μm microchannel wafer; and Figure 7-18 shows the final bonding step of the two wafers. The manifold and microchannel wafers were fabricated simultaneously, but for simplicity, they are presented separately.

7.3.1 Fabrication of the Manifold Wafer

Figure 7-9 shows the fabrication sequence for the manifold wafer which starts with a 1 mm thick silicon wafer with 1.5 μm of thermal oxide on both sides. An additional 2 μm of PECVD oxide is then deposited on the top side of the wafer. A 10 μm thick positive PR is then spun and patterned on the top side of the wafer (Step 3). In Step 4, RIE is used to etch the oxide that is not covered with photoresist. This oxide and photoresist stack is designed to be used as the masking layers during subsequent etching. In Step 5, DRIE is used to etch over halfway through the 1 mm thick silicon wafer, around 600 to 700 μm, until the masking layers (oxide and photoresist) have almost been depleted. The remaining photoresist and oxide are then removed in PRS and HF, respectively (Step 6). The side that has been etched is then anodically bonded to a Pyrex wafer causing sealed cavities within the wafer (Step 7). Thick (10 μm) PR is then spun and patterned on the other side of the wafer (Step 8). This pattern also includes the squares incorporated to reduce the loading across the wafer and cause the etch profile to be straighter and faster. Step 9 is the second DRIE etch to etch the remainder of the way through the wafer. In order to reduce loading, only the exterior of the manifold holes are etched and the middles are left to drop into the manifold holes with no affect and they are removed once the etch has finished. The Pyrex acts as an etch stop. The PR is then

removed with PRS (Step 10) and a Cr/Au/AuSn/Au stack is deposited on the bottom side of the wafer for subsequent bonding (Step11).

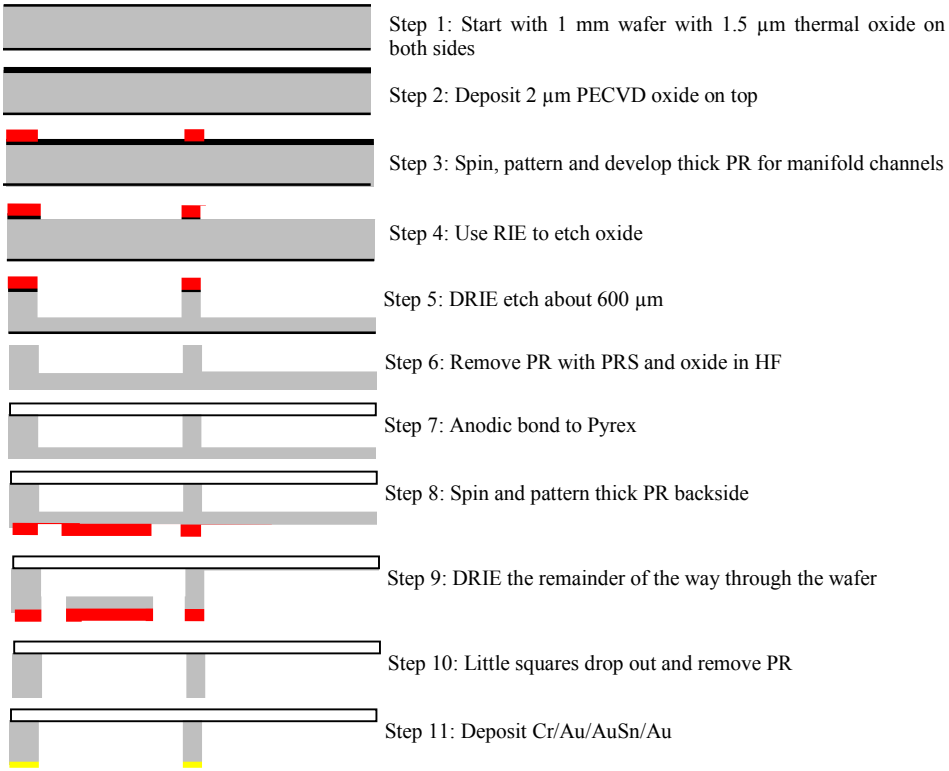
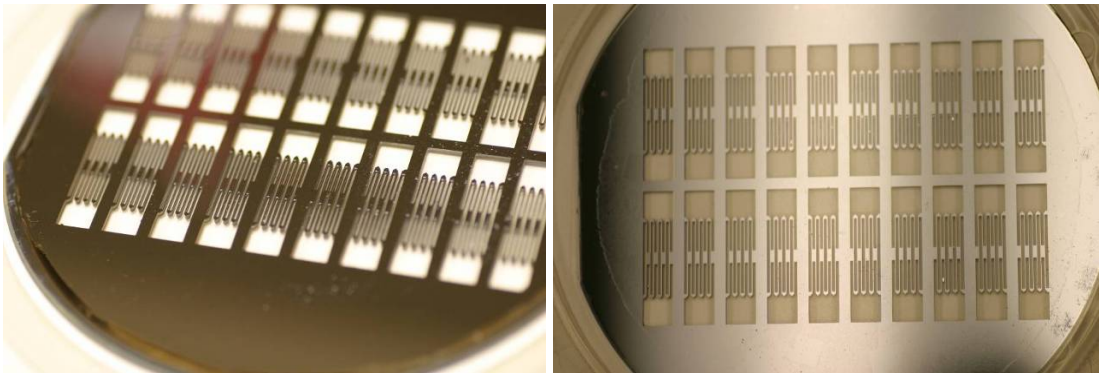


Figure 7-9: 1 mm manifold wafer fabrication sequence

The manifold wafer after DRIE etching can be seen in Figure 7-10. This is the point after Step 10 in Figure 7-9. The wafer has been anodically bonded to a Pyrex wafer and has been completely etched through.



(a) (b)

Figure 7-10: Manifold wafer after anodic bonding and DRIE etching

Figure 7-11 shows SEM images of the manifold channels and inlets. The first two images, Figure 7-11a and b show the channels right before they were completely etched through. The "fin" that is created and shown in the images happens as a result of the DRIE effect. The center etches slower than the edges and so the edges take longer to etch through completely than the middle. The next four images, Figure 7-11c - f, show the manifold channels once they have been completely etched through.

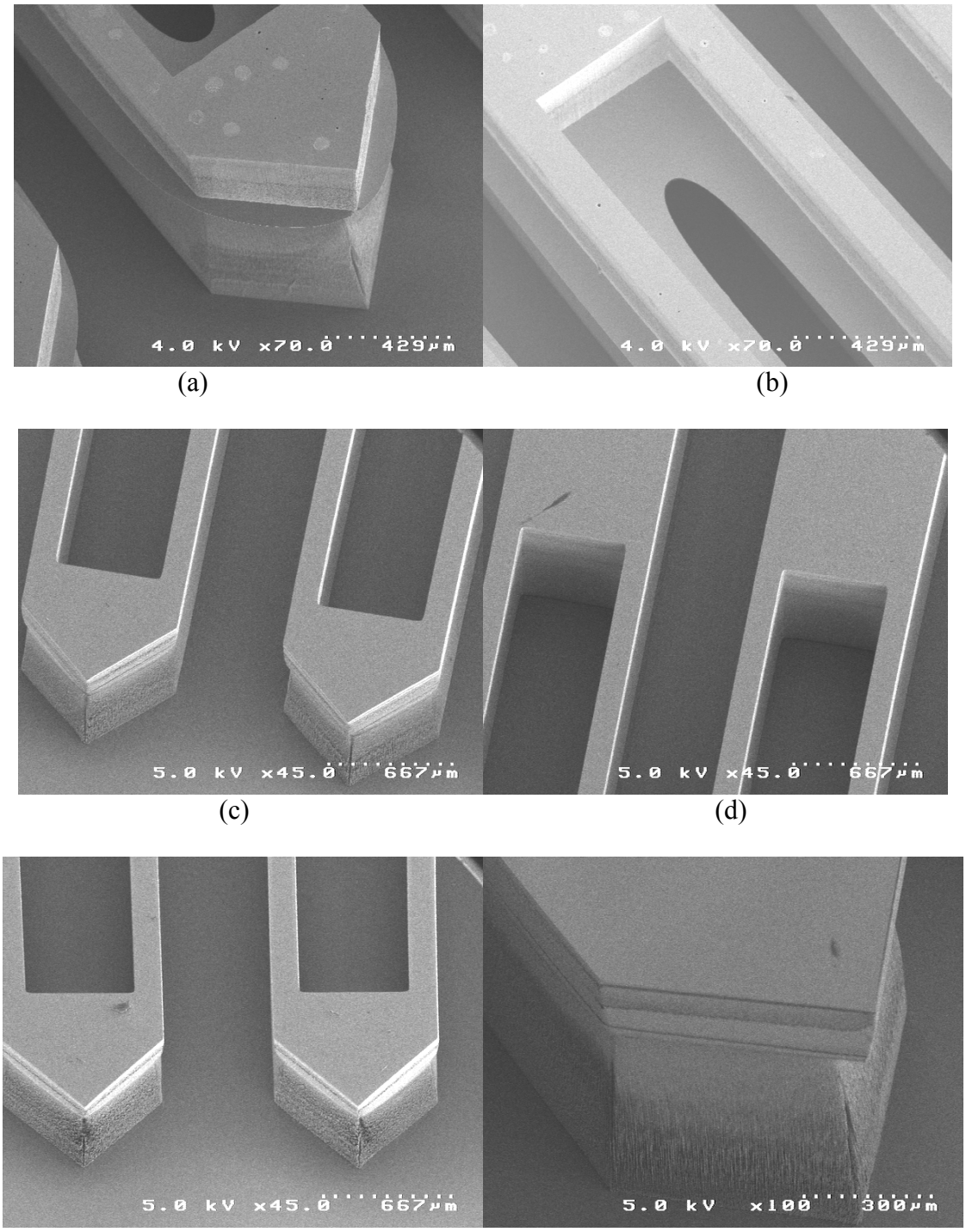
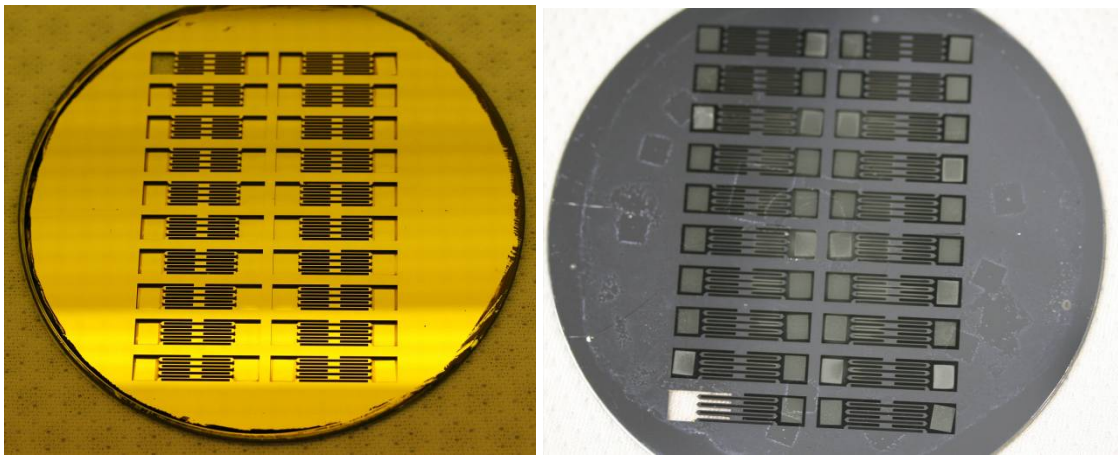


Figure 7-11: SEM images of the triangular fluidic inlet of the manifold wafer

The manifold wafer immediately before bonding is shown in Figure 7-12. The photo on the left is of the top-side wafer with the manifold channels etched into it. It has been coated with Cr/Au/AuSn/Au. It should be noted that the upper left hand manifold has had its gold removed from the inside. This was done by putting CR-9, a chrome etchant, into the cavity and allowing the gold to lift off. The image on the right, Figure 7-12b, is a picture of the backside of the wafer, from the Pyrex side. The Pyrex is clear, so you can see down to the silicon underneath. There is residue on the wafer (seen as squares and whitish coloring) which is caused from the graphite sheet that was placed on top of the Pyrex wafer during the anodic bonding process. It has no effect on the performance. In this image, the lower left device is the one that had metal removed with the CR-9 solution. The metal is also removed from the other devices as well.



(a) (b)

Figure 7-12: Manifold wafer immediately before bonding (a) top side with the manifold channels (b) backside looking through the backside capping Pyrex wafer

7.3.2 Fabrication of the Microchannel Wafer

Figure 7-13 shows the fabrication sequence for the microchannel wafer. The fabrication sequence starts with a 150 µm thick wafer with 1.5 µm of thermal oxide on both sides. In Step 2, the oxide is removed from the backside of the wafer by spinning and baking photoresist on the top side then submersing it in HF to remove the oxide on the backside. In Step 3, an additional 2 µm of PECVD oxide is deposited on top of the thermal oxide. The oxide must then be rapid thermal annealed due to the high stress of the thick oxide, which is used for the necessary voltage hold-off of the device. The next step, Step 4, involves spinning, exposing, and developing the PR for the microchannels and fluidic connections. The microchannels and fluidic connections are then formed by a DRIE etch through the wafer which is stopped when it reaches the oxide membrane (Step 5). The PR is then removed in a PRS solution (Step 6) and the remaining oxide membrane is broken manually from the fluidic inlets to open them. The final step, Step 7, involves depositing Cr/Au/AuSn/Au on both side of the wafer in the evaporator.

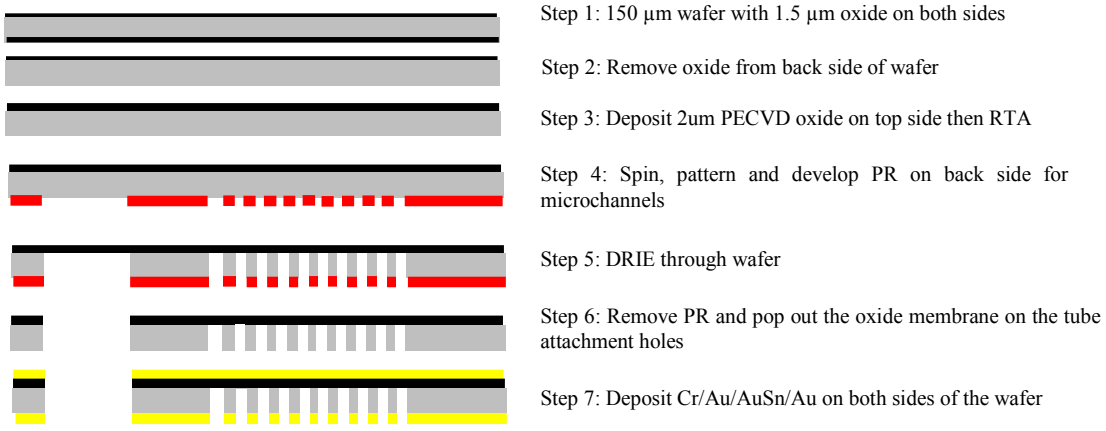
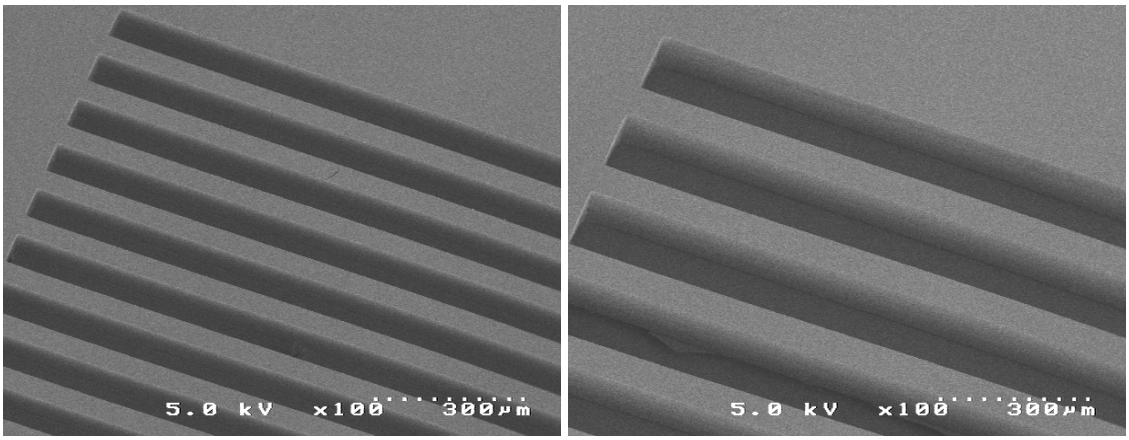


Figure 7-13: 150 µm microchannel wafer fabrication sequence

The SEM image below, Figure 7-14, shows images of two different sized microchannels. Both images are at the same magnification and so it is clear the channels on the right (b) are substantially larger than the ones on the left (a). In the larger channels on the right side, the oxide membrane can be seen at the bottom of the channels.



(a) (b)

Figure 7-14: SEM image of the microchannels

The microchannel wafer after DRIE fabrication is shown in Figure 7-15. The picture on the left, Figure 7-15a, depicts the top side of the wafer where the oxide membrane still remains. Some of the etch rings can still be seen from the loading effect where the center of the wafer has been etched completely through to the oxide and the exterior has not. The picture on the right, Figure 7-15b, is from the silicon side. It shows that the stressed oxide membrane still remains in some of the fluidic outlets, indicated by arrows on the image. It will be removed before further processing by breaking it with tweezers.

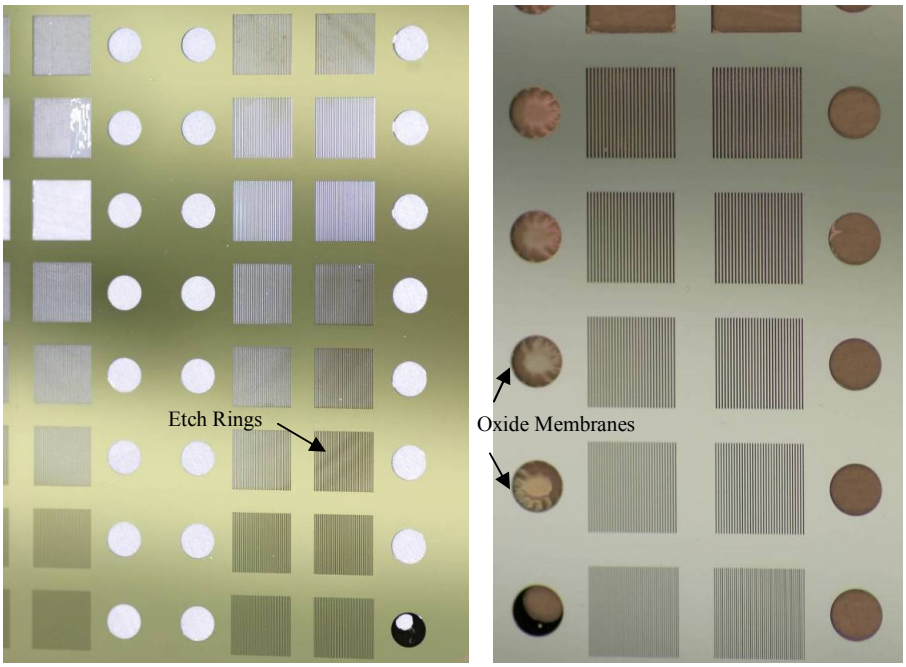


Figure 7-15: 150 µm microchannel wafer after DRIE etching (a) oxide side (b) silicon side

The microchannel wafer immediately before bonding is shown in Figure 7-16. The image on the left is the backside of the wafer after the AuSn has been deposited. It is the side with the microchannels etched into it. The photo on the right, Figure 7-16b, is of the front side of the wafer. This is the side that includes the fluid inlets and is also the side with the oxide membrane where the devices will be attached.

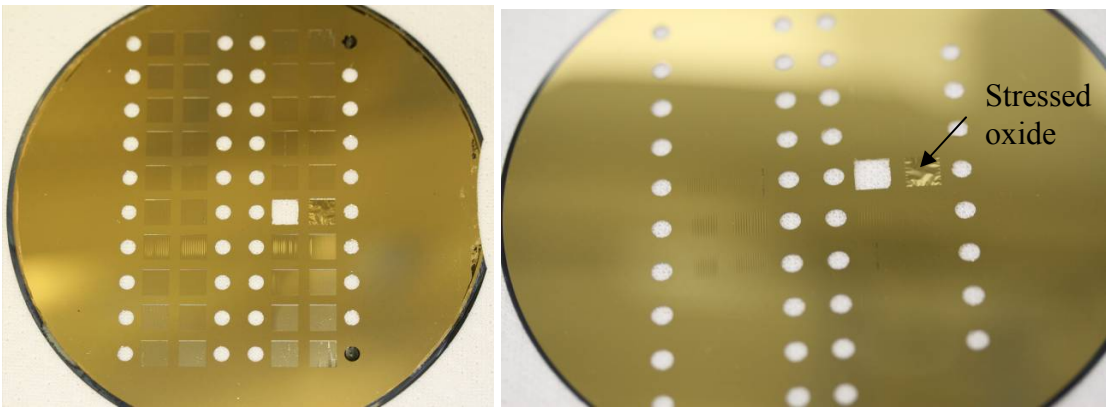


Figure 7-16: Microchannel wafer immediately before bonding (a) backside with the etched microchannels (b) topside with the fluidic inlets

A close up image of the microchannels is shown in Figure 7-17. Figure 7-17a and Figure 7-17b, depict both smaller and larger microchannel sets, respectively.

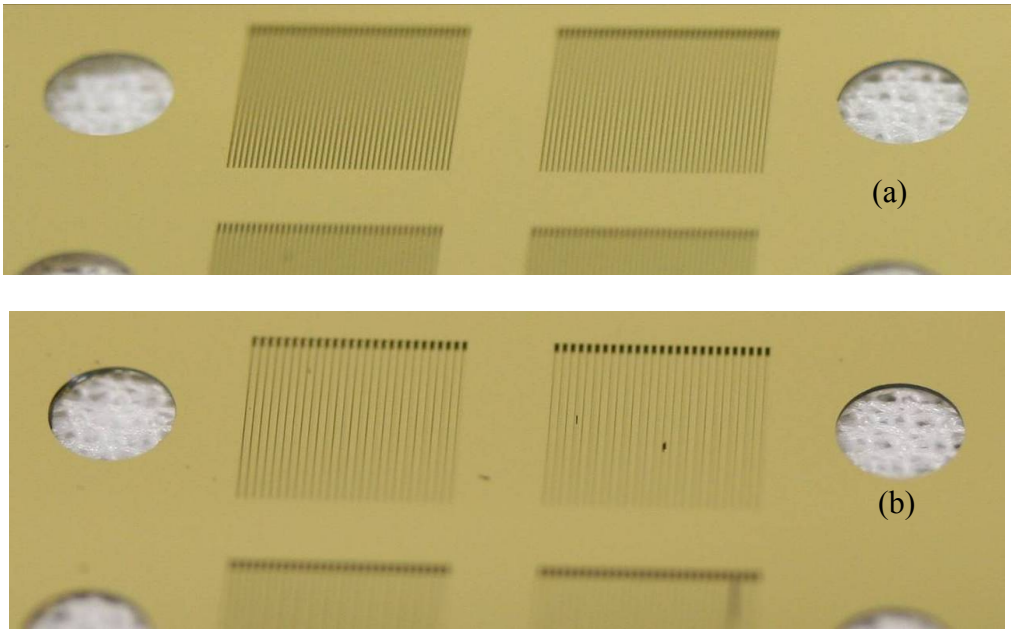


Figure 7-17: Zoomed in image of the microchannels (a) smaller channels (b) larger channels

7.3.3 Final Bonding Step

The final step of the new fabrication sequence is shown in Figure 7-18, which is bonding the wafers and chip resistor together with a gold-tin bond in the wafer bonder.

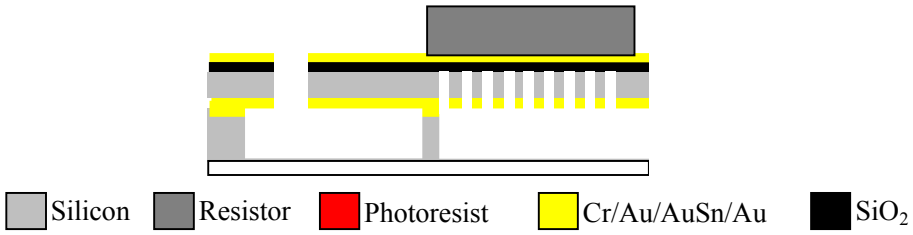
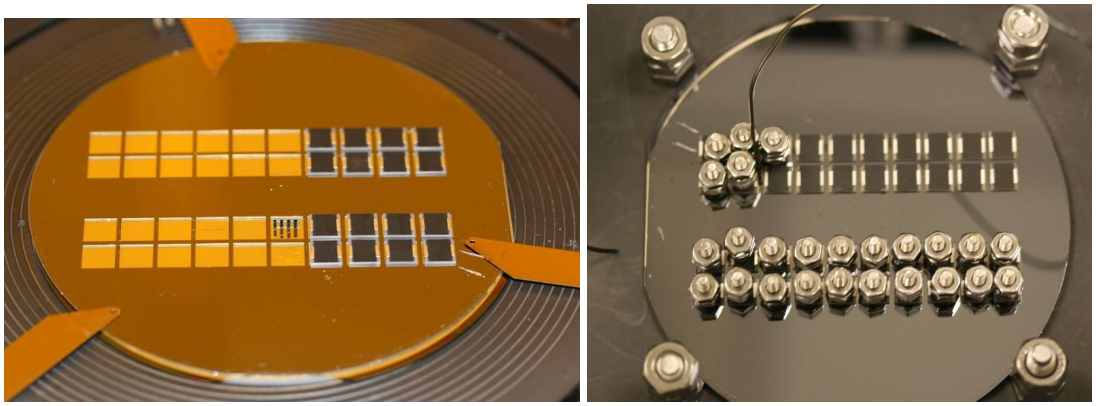


Figure 7-18: Final bonding step between the manifold and the microchannel wafers

There were two methods that were tried during bonding: a wafer bonder and a solder reflow oven, shown in Figure 7-19a and Figure 7-19b, respectively.



(a) (b)

Figure 7-19: Image of bonding using the (a) wafer bonder and (b) solder reflow oven

For bonding in the reflow oven, the wafer is placed on the graphite chuck with weights (large stainless steel bolts with nuts screwed on) placed in four places around the perimeter to inhibit potential movement. The devices are then put into place and

individual weights (small stainless steel bolts with two nuts) are placed onto each individual device. Thermocouples are then placed on the graphite chuck and the surface of the wafer to measure their respective temperatures.

The method found to have worked better was the wafer bonding chamber, but as will be discussed in the next section, it did not perform satisfactorily.

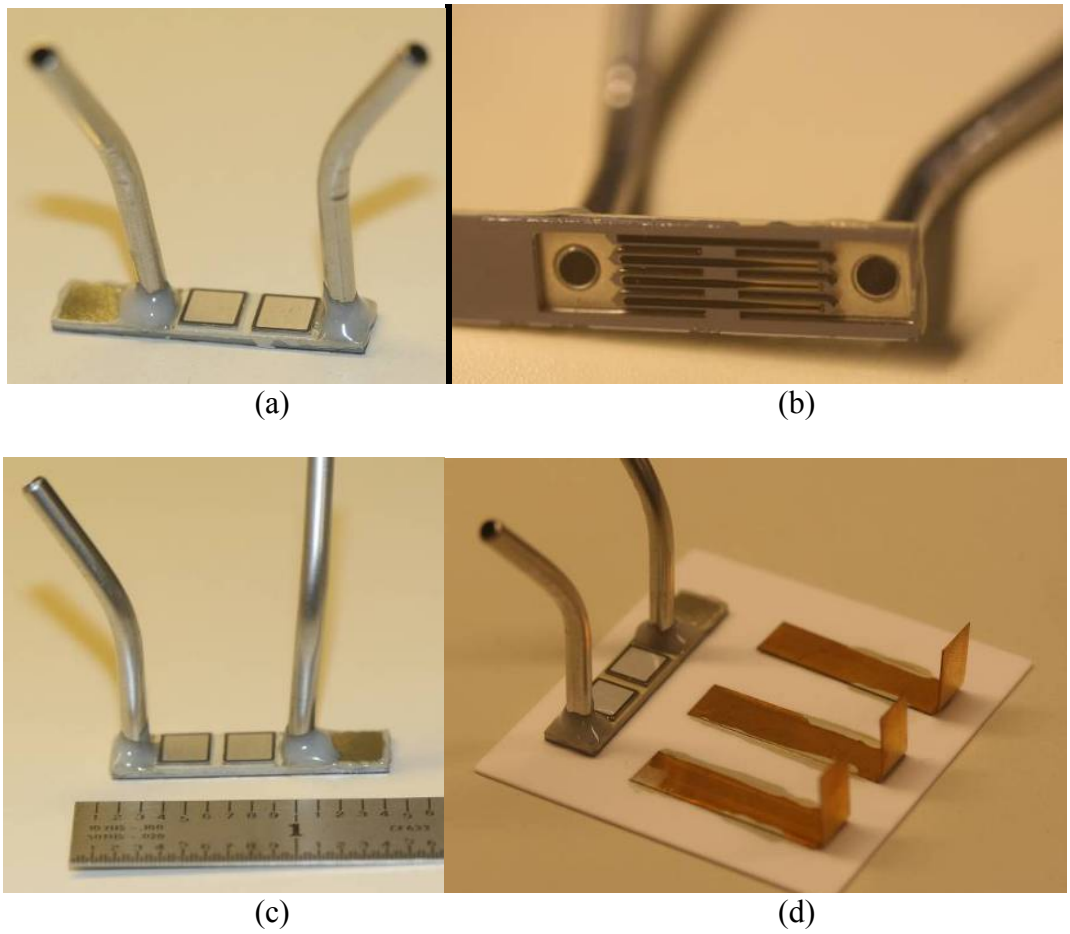
7.3.4 Problem with Aluminum Nitride Chip Resistors and AuSn Bonds

After attempting to make bonds with both the reflow oven and the wafer bonding chamber, satisfactory bonds could not be formed in either. After further investigation it was discovered that the backside of the AlN chip resistors is concave up to 10 to 15 μm, therefore, the thin film bond (<3 μm) could not be made on these devices. The devices were replaced with similar sized silicon diodes and slight alterations had to be made to account for the backside connection to the die.

Additionally, an effort was made to do a two-layer AuSn bond. The first thing was to research the temperatures, times, and pressures required to make a good quality AuSn bond. The second step was to incorporate this into a recipe in the wafer bonder and run sample devices. The sample devices were pieces of a wafer that has been coated in the desired metallization stack. After each sample is made, the bond quality was analyzed by dicing the sample into one millimeter square pieces and then trying to shear them apart. If the samples do not come apart during shear testing, it was considered to be a good bond. Bonds were also made between silicon and aluminum nitride to assure that the CTE mismatch between the two materials is not detrimental. But despite multiple attempts to form a two-layer AuSn bond, it was determined that a reliable bond could be made for only one AuSn layer.

7.4 Completed Device

The completed device after the tube attachment is shown in Figure 7-20. The tubes were attached with an epoxy. Due to the lack of a good bond between the device and the microchannel silicon wafer, the AuSn bond was made and then it was secured around the edges with a conductive epoxy. Figure 7-20a shows the view from the top of the two silicon diodes with the inlet and outlet tubes on each side. Figure 7-20b shows an image of the bottom of the device indicating the placement of the tubes as they enter the plenum area. Figure 7-20c shows the device next to a ruler indicating the total size of the structure, with its length being almost 1.5 inches.



(a) (b)

(c) (d)

Figure 7-20: Final fabricated version of MMC3 after the stainless steel tubes were epoxied on

After the tubes were attached, the structure was attached to a two inch square piece of alumina using an epoxy that could subsequently be removed with acetone for rework or observation, if necessary. Copper tabs were also cut, bent, and attached to the alumina with P-1011, a silver epoxy. These copper tabs are for the electrical connections. They are used to keep the external electrical connections away from the device to minimize any unnecessary stress on the device. This is depicted in Figure 7-20d.

Figure 7-21 is a zoomed in image of the bottom of MMC3 and its microchannels which clearly shows the relationship between the manifold and the microchannels.

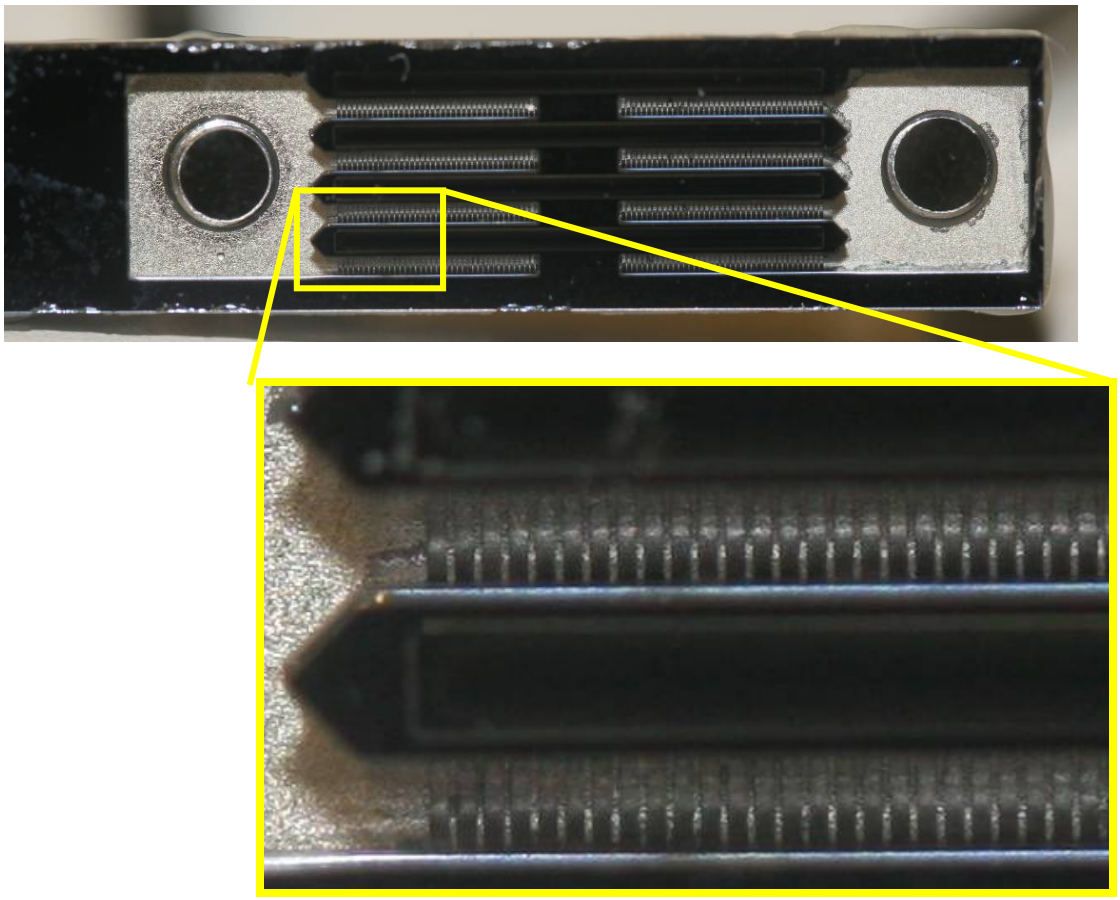


Figure 7-21: Image of the bottom side of the device showing the manifolds and the microchannels with a zoomed image of the microchannels

The electrical and fluidic connections are then made to the device, shown in Figure 7-22. Ten-mil aluminum wirebonds are connected from the top of each diode to one of the copper tabs. In order to obtain the necessary backside connection for the silicon diodes, a common backside connection is bonded from one side of the structure. The fluidic connections are standard Swagelok connections and the ferrule is compression fit onto the stainless steel tubes to create a fluidic seal.

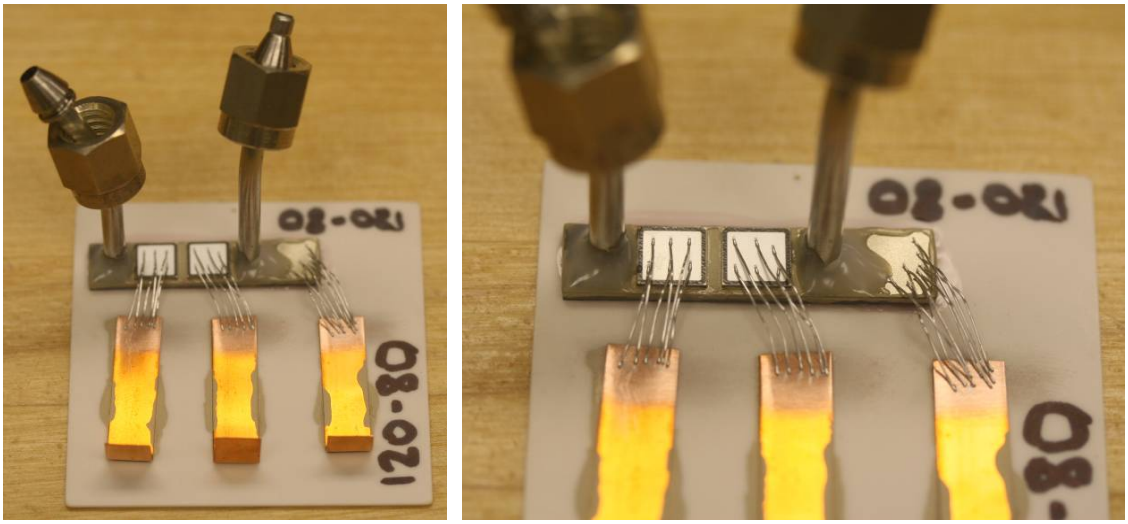


Figure 7-22: Completed device after wirebonding and attachment of Swagelok connections

7.5 Testing Results

Testing showed that the gold-tin bonds were not adequate. Multiple devices were tested, and they all failed after very little powering. The thermal camera showed that the metal on the backside of the die heated up more than the device, which indicated resistive heating of the backside metallization. This was likely the cause of the failures wherein the excessive heating caused a failure of the backside connection and/or the oxide. As each die-attach connection failed, more current was forced through the remaining

connections, which made those heat up even more, ultimately causing complete failure of the backside contact.

7.6 Conclusions of MMC3

The failures that occurred during testing indicated two manufacturing problems: inadequate bonding of the chip to the cooler and not a sufficiently thick metallization to carry the current. The oxide is still a feasible option but some changes must be made to the fabrication. In addition to the use of an oxide as an electrical isolation layer, aluminum nitride was also used, as will be discussed in the next chapter.

8 Manifold Microchannel Version 4 (MMC4)

In addition to the use of an oxide as an electrical isolation layer, AlN was also determined to be a viable option. Therefore, in this version, MMC4, the isolation layer is AlN instead of an oxide. The bonding process was also changed due to the additional bonding layer from the AlN. A cresol novolak epoxy resin bond was used between the two wafers.

8.1 AlN as a Material for Electrical Isolation

Aluminum Nitride (AlN) is standard packaging material that has proved to be a feasible material because of its very high thermal conductivity, strength, and very good CTE match to silicon. The use of the AlN also allows for the use of standard die attach methods (such as pre-form die attach and solder reflow) as opposed to the thin film methods used previously.

Calculations in Table 8-1 show the thermal performance of the AlN is comparable to that of the oxide. The table shows that a 381 μm thick piece of AlN has a thermal resistance value of 0.058 K/W versus a 3.5 μm thick oxide layer, which has a thermal resistance value of 0.065 K/W. Thus, the thermal performance is very similar even though the AlN is 100 times thicker. The AlN does not have to be 381 μm thick as it only has to be thick enough to hold off the required voltage and provide stability. An AlN that is 381 μm will hold off more than 6 kV and in most power electronics systems, a voltage hold off of 1.2 kV is sufficient which would equate to a AlN layer that is only 75 μm thick, using the dielectric strength of AlN is about 16.7 V/μm. A thinner AlN layer will improve thermal performance and reduce size.

Table 8-1: Thermal resistance calculations of AlN versus silicon dioxide

	t (μm)	k (W/mK)	A (cm^2)	R_{th} (K/W)
Oxide	3.5	1.4	0.3844	0.065
AlN	381	170	0.3844	0.058

But AlN has disadvantages over the oxide. Although the AlN does not have to be as thick as was used in this study. Also, the AlN will add an additional bonding layer that was not previously there, thus complicating the fabrication sequence. AlN also has a CTE mismatch with silicon that can cause stresses in the structure.

8.2 Design of MMC4

The design of MMC4 is the same as MMC3 in terms of dimensions and structure. The same masks were used for the patterning and etching. The same two-chip design was also used with fluidic inlets on both sides. For a reference, the device dimensions are shown in Table 7-1 and Table 7-2. Figure 7-1 shows the overall design of the structure. A cross-section of MMC4 is shown in Figure 8-1 indicating the placement of the 380 μm AlN layer in the structure between the top microchannel wafer and the aluminum nitride chip resistor. AlN chip resistors are used as the active devices. The same wafer layout is used with the top 150 μm thick microchannel wafer bonded on top of the 1 mm thick manifold channel wafer. The bottom is capped with a 175 μm thick Pyrex wafer.

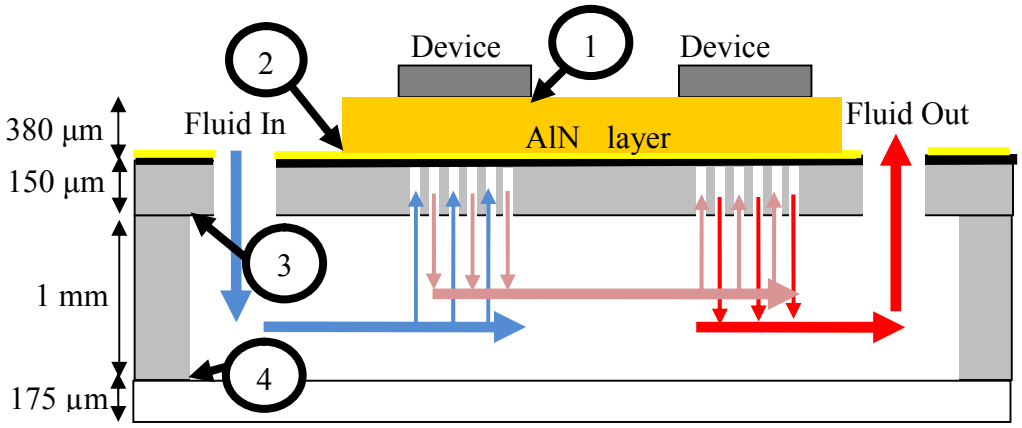


Figure 8-1: Cross-section of MMC3 with the wafer thicknesses and fluid flow

The current stack requires four bonding layers which are numerically labeled in Figure 8-1: attach the bottom capping wafer to the manifold (4), attach the manifold to the microchannel wafer (3), attach the AlN to the microchannel wafer (2), and to attach the device to the AlN layer (1). The anodic bond between the manifold wafer and the Pyrex wafer (4) has proven to be easy to replicate and reliable; therefore, this bonding layer will remain the same. The bonding layers between the device and the AlN (1) and the AlN to the microchannel wafers (2) are both in the critical thermal path, therefore, they should have a high thermal conductivity and should be thin. The layer attaching the two wafers to each other (3) does not need to be thermally conductive but should be thin and fluidically sealing. A single layer thin-film AuSn eutectic bond has been proven to be reproducible and reliable. Therefore it will be used for the critical bond between the AlN layer and the microchannel structure.

Two changes were made to the processing sequence to account for the additional AlN layer. The first change is to use a cresol novolak epoxy resin bond (a photoresist

material) between the microchannel and the manifold channel wafer (2) and the second is the ability to use standard solder bonding processes between the chip and the AlN (1).

AuSn bonding is conducted between the top silicon microchannel wafer and the AlN wafer because the attach is in the thermal path, but a different method can be used between the manifold and microchannel wafer due to the difficulty of making a reliable two-layer AuSn bond, as was discussed in Section 7.3.4. It was determined to use cresol novolak epoxy resin as a thin adhesive material between the manifold and microchannel wafer because it can create a fluidic seal, does not need to be electrically or thermally conductive, and is easily spray coated.

Having the AlN as the topmost layer on the stack allows for standard die attach methods to be used between the die and the cooler. The top surface is simply bare AlN, which can be metalized so that the chip (bonded with a solder or a silver polyimide) can be attached directly to the AlN.

8.3 Fabrication Sequence

The fabrication sequence was altered slightly from the MMC3 to the MMC4 to account for the additional AlN layer. The main differences include the removal of the previous isolation oxide layer on the microchannel wafer and the bonding techniques. Figure 7-9 in the previous chapter shows the fabrication sequence for the 1 mm thick silicon manifold wafer. The sequence is exactly the same except the last step (Step 11) where the AuSn is deposited does not happen in this case.

Figure 8-2 shows the MEMS fabrication sequence for the 150 μm microchannel wafer. It starts with a 150 μm thick wafer that has 1.5 μm of thermal oxide on both sides. The first step is to spin and pattern photoresist one of the sides of the wafer. Then remove

the oxide in the pattern using RIE. The wafer is then DRIE etched through to the oxide, which acts as an etch stop on the other side. Both the oxide and the PR are removed and a metal stack of Cr/Au/AuSn/Au is evaporated on the top side of the wafer.

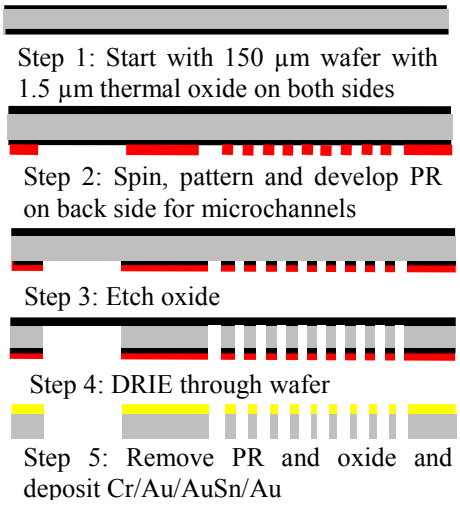


Figure 8-2: MMC4 150 µm microchannel wafer fabrication sequence

Two bonding techniques were used to attach layer structures together, both of which are pictured in Figure 8-3. The first technique is shown in Figure 8-3a and involves a wafer level epoxy resin bond and a die attach using P1011. P1011 has a very high thermal resistance and the wafer level epoxy resin bond did not perform as well as needed. Therefore, a second bonding process, shown in Figure 8-3b, was utilized which uses a standard AuSn solder to attach the die and individual epoxy resin device bonds.

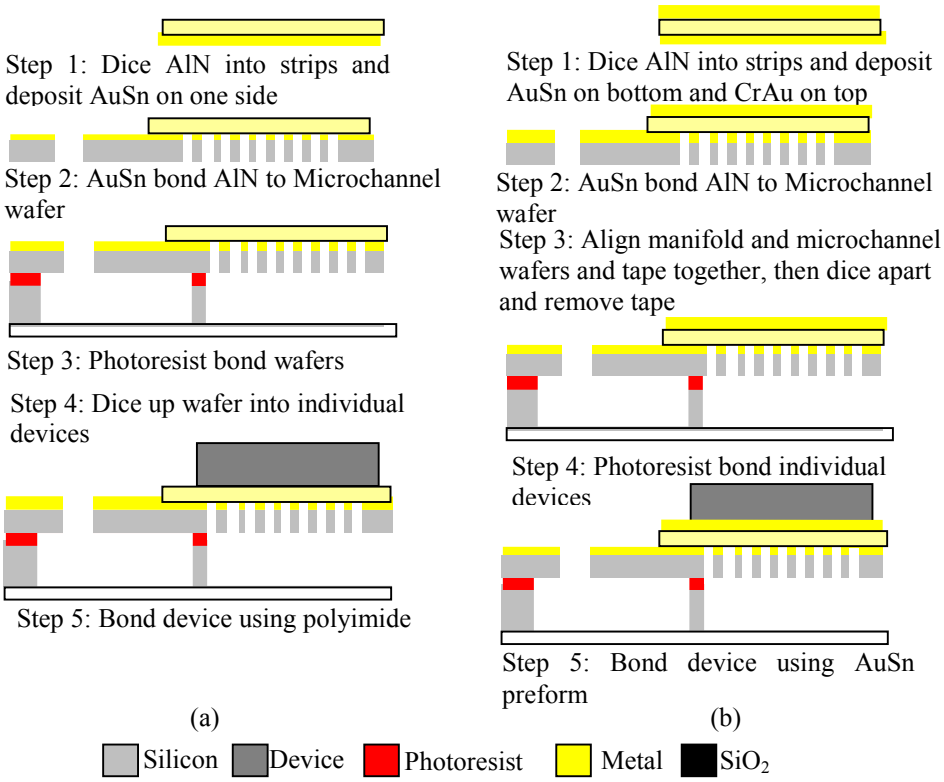


Figure 8-3: Final bonding step between the manifold and the microchannel wafers

In both processes, the first step involves dicing the AlN into properly sized strips to cover the microchannels then metalizing them with Cr/Au/AuSn/Au on one side. In the AuSn bond process (Figure 8-3b); the other side of the AlN is also metalized with Cr/Au which creates a bonding surface for the subsequent AuSn bonding process. In both processes, Step 2 is to bond the top silicon wafer to the metalized AlN strips using a AuSn eutectic bonding process in the wafer bonder. The next two steps are now switched in the two processes. In the P1011 process (Figure 8-3a), the wafers are bonded with an epoxy resin bond and then diced; and in the AuSn process, they are first diced and then epoxy resin bonded. This makes the difference of doing a wafer level bond or individual die bonds. A wafer level bond is preferred because it bonds all the devices in one step, but this proved to not be an acceptable bond because the devices would oftentimes split

during the dicing process. In the AuSn process, the two wafers are aligned and held together using a blue Mylar film while they are diced to ensure they align properly during the next bonding step. In each case, the epoxy resin bond was made by spray-coating about 5 μm of epoxy resin only on the thick manifold wafer. Then the two wafers were aligned and pushed together. Finally, they were placed onto the hot plate under a compressed load and baked at 120 ºC for 15 minutes to hard-bake the epoxy resin and form a solid water-tight bond. The fifth and final bonding step involves attaching the die to the top of the AlN. In the P1011 process, the die is attached with a P1011 silver epoxy which cures at 150 C. In the AuSn process, a solder reflow oven is used to properly reflow the solder below the die.

8.4 Device with Silver Polyimide Die Attach

The initial set of devices were die attached using P1011, a silver polyimide paste which cures at 150 ºC. A polyimide was chosen instead of a solder because of concerns that the epoxy resin bond would not be able to handle the extreme temperatures required for soldering. Additionally, unlike solders, the P1011 can be attached directly to the AlN layer with no additional metallization. The stainless steel inlet and exit tubes were attached with a room temperature curing two-part epoxy. The cooler was then secured to a 2-inch square piece of alumina having two copper straps attached for electrical connections using a removable epoxy. Aluminum wirebonds, with a 127 μm diameter, were used for the electrical connections and the aluminum nitride chip resistors were connected in series for even heating. Plastic tubing with Swagelok fittings were then secured to the stainless steel tubes for the fluidic inlet and outlet connections. The final packaged device is shown in Figure 8-4.

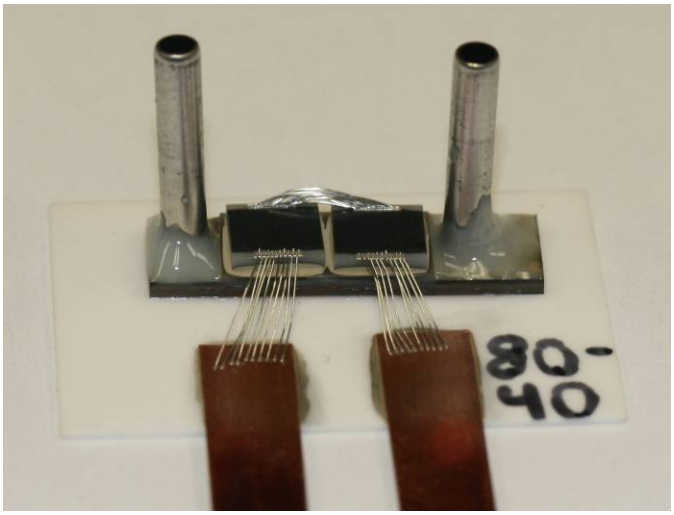


Figure 8-4: Final packaged device with both electrical and fluidic connections

8.4.1 Testing Results for the Initial Packaging Process

The fabricated cooler was tested under a variety of fluid pressures and power densities. The device was tested to 39 kPa, which equates to a flow rate of 400 mL/min. A graph of the flow rate versus pressure drop is shown in Figure 8-5.

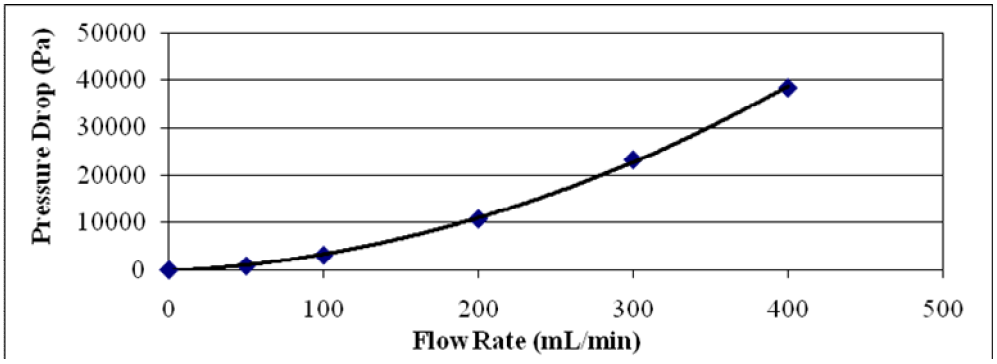
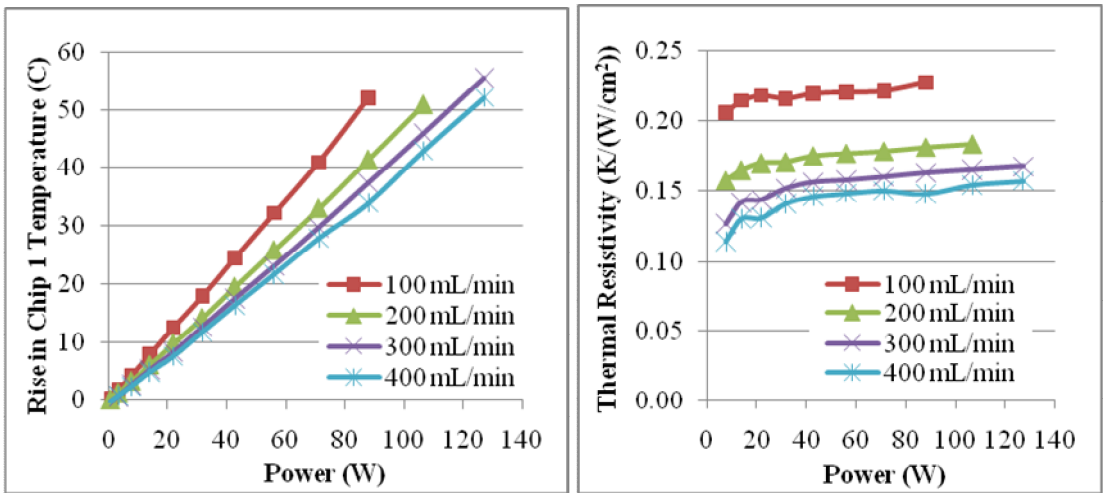


Figure 8-5: Graphical representation of the flow rate versus pressure for the two chip manifold microchannel cooler.

Two important parameters of a heat sink when cooling a device are the thermal resistance and the change in the device temperature. Figure 8-6 shows how much the chip temperature increases for varying input powers. The data indicates a linear trend between the power and the device temperature rise. When inputting 80 W of power, the chip temperature rises from 30 to 45 ºC for flow rates varying between 400 and 100 mL/min, respectively. For 100 mL/min, the chip temperature rises about 0.59 ºC for every 1 W in power increase, for a thermal resistance value of 0.59 C/W. For 400 mL/min, the thermal resistance is 0.41 C/W. These test results indicate very good performance. The air temperature during all tests was measured to be 19.2 ºC and the inlet fluid temperature was measured to be 19.1 ºC.



(a) (b)

Figure 8-6: Graphical representation for various flow rates of the (a) power versus change in device temperature and (b) power versus the thermal resistance

The graph of the thermal resistance compared to the input power is shown in Figure 8-6b. This chart indicates thermal resistivity values of around 0.15 K/(W/cm^2).

These values are not as good as the results from MMC2, but in MMC4, a standard silver-filled polyimide paste was used for the die attach and an electrical isolation layer was also included, both of which increase the thermal resistance.

A graph of the pressure drop compared to the thermal resistivity is shown in Figure 8-7. The thermal resistivity decreases with increasing pressure drop. However, due to the exponentially decreasing trend of the graph, increasing the flow rate after a certain point has limited effects on the performance. This point would be application specific. Additionally, the graph shows that increasing the power also causes an increase in the thermal resistivity. This is due to the increased chip non-uniformity at higher powers which causes the average chip temperature to be slightly elevated.

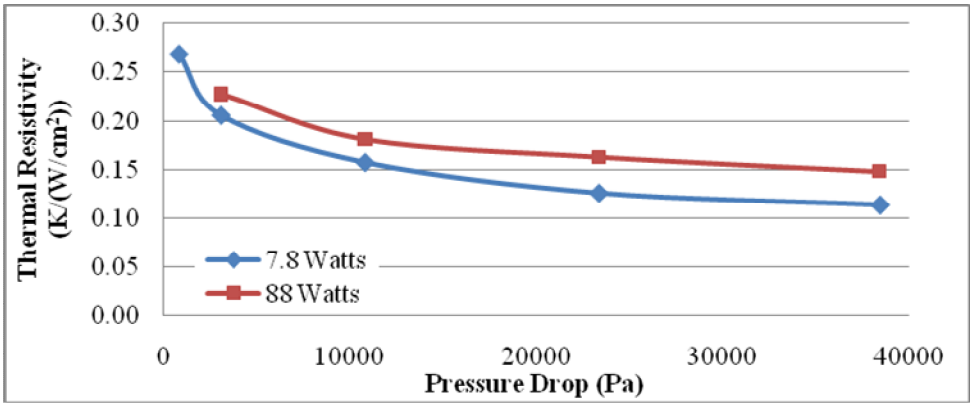
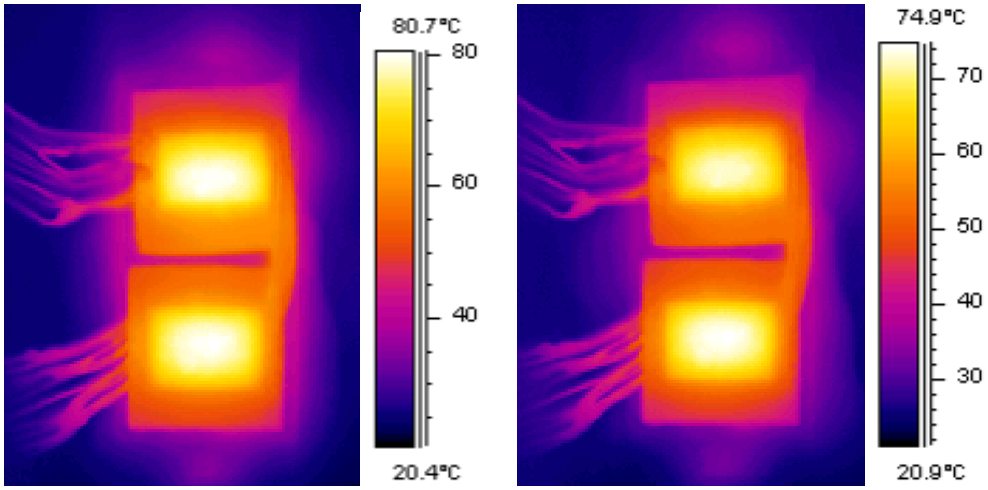


Figure 8-7: Graph of thermal resistivity compared to the pressure drop for varying powers

Because two devices were used in this experiment, the second chip was expected to be substantially hotter than the first; however, this did not happen. In most cases the difference in temperature between the two devices was less than 0.5 ºC. Figure 8-8 shows thermal images during testing of the two devices at 88 W at both 100 and 400 mL/min. It

should be noted that the center of the chips are hotter than the rest of the chip; therefore, the average chip temperature was used when reporting the chip temperature.



(a) (b)

Figure 8-8: Thermal images of the devices at 88 W and (a) 200 mL/min (b) 400 mL/min

A summary of the experimental results for one cooler can be seen in Table 8-2. The table shows results for the device at 71.2 W (185.2 W/cm^2) at a variety of flow rates. The fluid temperature rose between 3.25 ºC and 11.74 ºC, depending on the flow rate. The similar thermal performance between the two chips should also be noted.

Table 8-2: Sample set of data for 71.2W power and 185.2W/cm^2

Flow Rate	ΔT_{fluid}	ΔT_{chip1}	ΔT_{chip2}	Rth Chip 1	Rth Chip 2
mL/min	C	C	C	C/W	C/W
100	11.74	41.02	38.08	0.58	0.53
200	6.21	33.03	32.30	0.46	0.45
300	4.24	29.69	29.88	0.42	0.42
400	3.25	27.87	28.51	0.39	0.40

In conclusion, the cooler shows excellent thermal results with thermal resistances less than 0.6 ºC/W and in some tests, less than 0.4 ºC/W. Thermal resistivity values were

measured around 0.15 K/(W/cm^2). Tests were performed up to 127.2 W which equates to a heat flux of 331 W/cm^2, yet the chip temperature increased only 53 ºC. The results of the testing show very good thermal performance of this device.

8.5 Final Bonding Process: Device with AuSn Die Attach

After running into the problems with the P1011 and wanting to use a true solder material, it was decided to use a AuSn solder perform along with a individual device epoxy resin bond instead of a wafer level bond. Additionally, a metallization had to be added to the surface of the AlN to solder to. P1011 also has a very low thermal conductivity, so it is more desirable to use a solder instead of a silver filled epoxy.

Tests were made that show that the epoxy resin can actually withstand the solder reflow profile, which is designed to ramp to about 315 ºC for 1 minute before ramping back down to room temperature. The stainless steel inlet and exit tubes were attached with a room temperature curing two-part epoxy. The cooler was then secured in place using a removable epoxy to a piece of alumina with two copper straps attached for electrical connections. All the layers of the package can be seen in Figure 8-9.

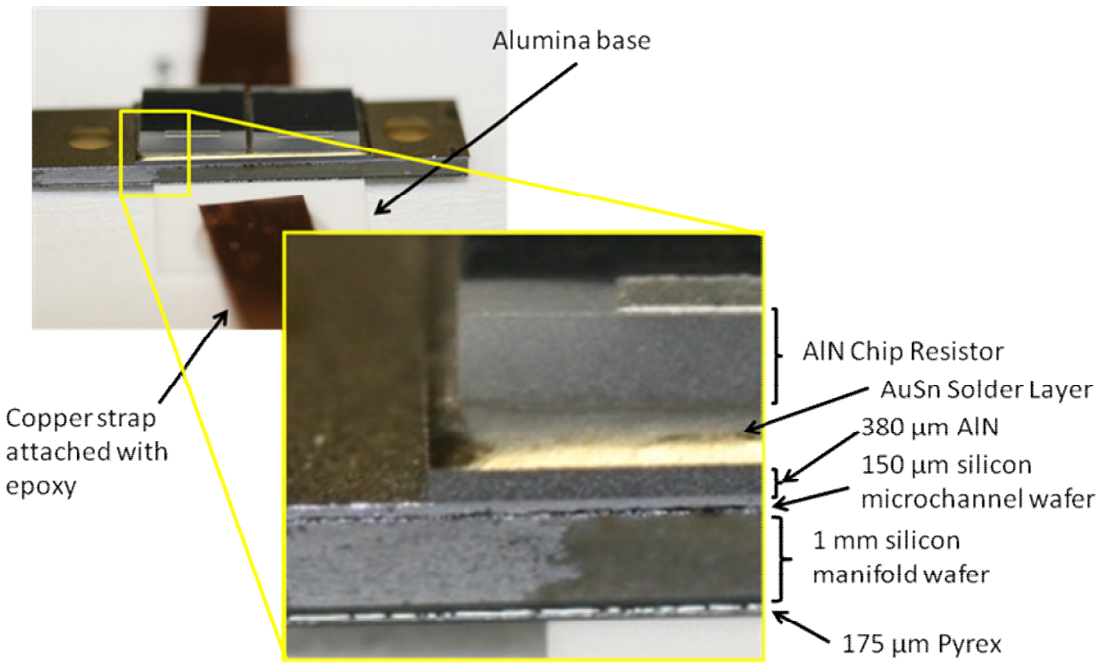


Figure 8-9: Photo labeling all the layers of the complete device

Five-mil aluminum wirebonds were used for the electrical connections and the aluminum nitride chip resistors were connected in series for even heating. The packaged device with the wirebonds is shown in Figure 8-10.

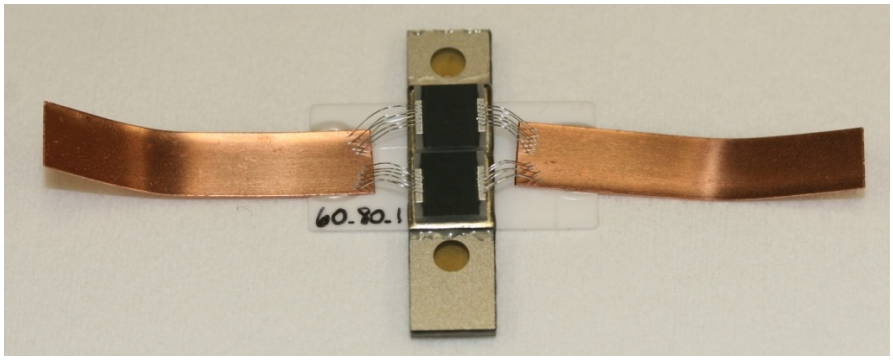
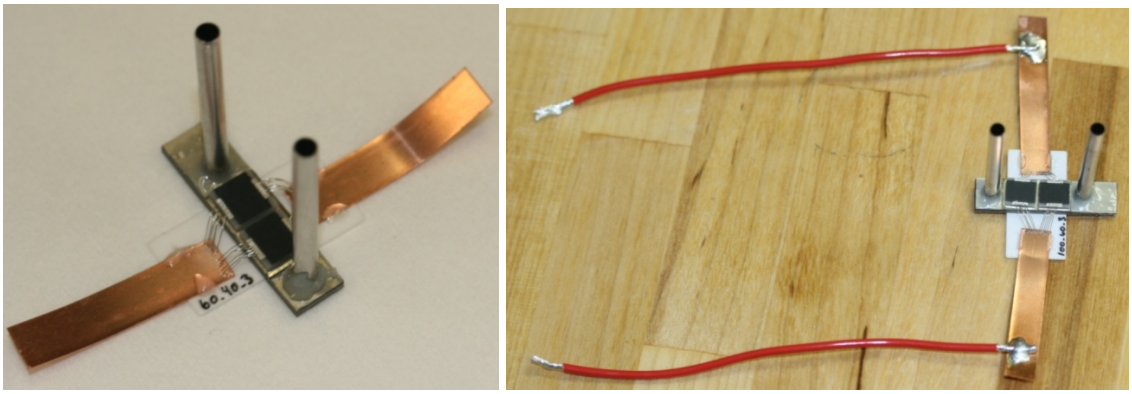


Figure 8-10: MMC4 device attached to alumina substrate and with electrical connections made with 5 mil wirebonds

Plastic tubing with Swagelok fittings were then secured to the stainless steel tubes for the fluidic inlet and outlet connections, shown in Figure 8-4a. Then wires were soldered onto the copper straps, shown in Figure 8-4b. The device is now ready for testing.



(a) (b)

Figure 8-11: Packaged MMC4 device with (a) stainless steel tubes attached and (b) electrical connections soldered onto copper straps

8.6 Experimental Set Up

After fabrication was completed, the devices were tested experimentally. The experimental set-up is shown in Figure 8-12. All experiments were run with room temperature demineralized water that originated in a pressurized tank. A digital flow controller is used to control the flow rate through the device with pressure transducers and thermocouples at both the inlet and the outlet to measure conditions. A power supply is used to power the chip resistors which apply the heating to the structure.

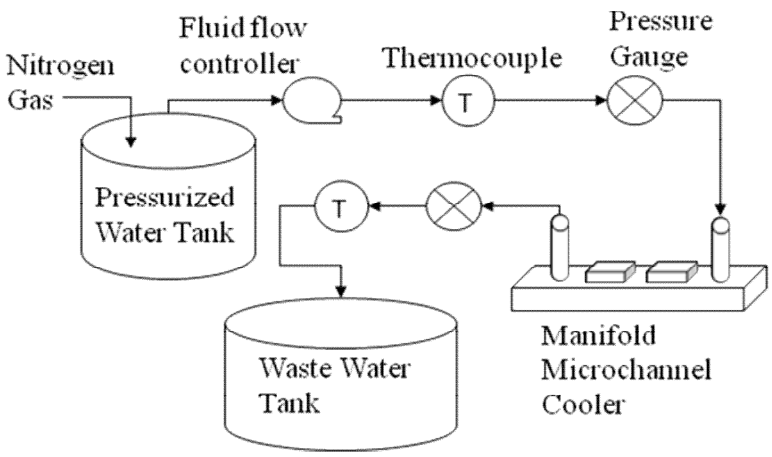


Figure 8-12: Schematic of the microchannel manifold test set-up.

Labview is used to gather most of the experimental data and to control the flow controller. A National Instruments SCXI-1000 DAQ is used to gather the data from the inlet pressure transducer, outlet pressure transducer, inlet thermocouple, outlet thermocouple, ambient thermocouple, inlet voltage, outlet voltage, and current. Labview then takes all this data along with the output from the flow controller (the flow rate, line pressure and fluid temperature) and outputs it all into a time stamped text file which can be copied into Excel. When the experiment is running, Labview constantly exports data at 10 times per second.

The only data that was gathered externally to Labview was the data from the thermal camera. The thermal camera was used to measure the maximum, minimum and average chip temperatures for both chips along with point measurements along the center line of the chip. The locations of all these measurements are shown in Figure 8-13. On each device there is a larger box covering the entire chips surface and an inner box covering only the portion of the chip between the two electrical connections. As can be seen, most of the heat generation occurs between the two electrical connections. The

maximum, minimum and average temperatures of each of these boxes are measured. A series of point measurements are also placed along the centerline of the chip to obtain the thermal profile along the centerline. The x-position and the temperature are obtained for each of these points. At each test condition, once the system has reached steady state, two time-stamped images are captured using the thermal camera. Each data point is obtained by averaging the data obtained from each image. The time-stamps are then matched to the data taken in Labview and the last 25 data points in Labview are averaged (~2.5 seconds of data) to obtain the steady state data.

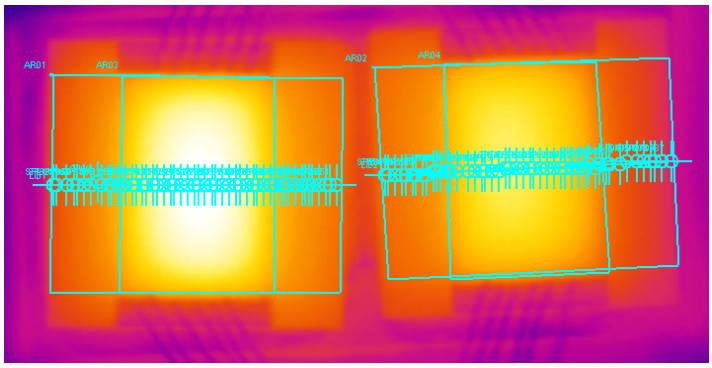


Figure 8-13: Thermal camera image showing the locations of all the data locations

The flow rate was controlled with an Alicat brand flow controller that measures between 0-2000 mL/min with an accuracy of 2% of the full scale (40 mL/min). The pressurized tank that was used holds 11 liters of fluid and is rated to about 900 kPa. It is filled manually with demineralized water, sealed with an O-ring, and pressurized with a house nitrogen line to about 275 kPa. Two pressure transducers were placed to measure both the inlet and the outlet pressure of the MMC. The pressure transducers were rated for 0 – 100 kPa with an output of 1 -5 V. They were calibrated by sealing off the end of

the line and applying known pressures and inputting into Labview. Standard k-type thermocouples are used to measure the inlet fluid temperature, outlet fluid temperature and ambient air temperatures during the test.

Two aluminum nitride chip resistors are used to provide the heat and are wirebonded in a parallel configuration. A 120 V, ±170 A power supply is used to power the devices and is controlled through a remote operating program on a laptop. The current through the system is constant and was measured with a current probe attached to the inlet. The voltage is measured using the DAQ but was first put through an attenuator to scale it by 1/100. Both the current and voltage were calibrated in the DAQ Assistant in Labview using a voltmeter. The total power dissipation is obtained by multiplying the current times the voltage drop. A photo of the device in the test bed is shown in Figure 8-14. Plastic tubing was attached to the stainless steel tubes using plastic cable ties which sufficiently sealed the tubes. They also proved to be easy to attach and remove with no harm to the device. Wires are soldered onto each of the copper straps using standard tin-lead solder, and are connected via screw terminals to the power supply.

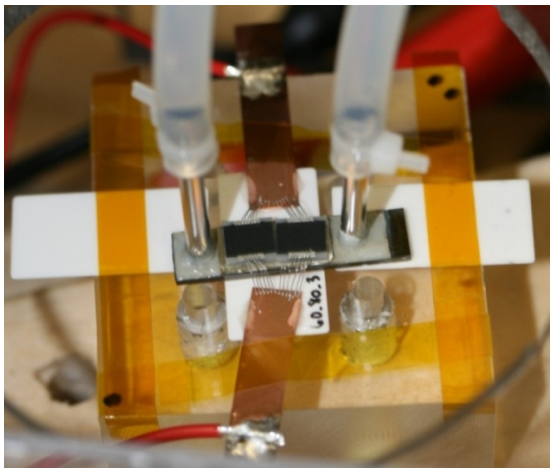


Figure 8-14: Photo of a device in the test bed

Each device was tested at a variety of flow rates and power conditions. For each structure, the tests started at 100 mL/min and went in 100 mL/min increments up until the pressure drop reached about 100 kPa. A final test was then performed at 50 mL/min since the device heated up quite substantially at this low flow rate. At each flow condition, the voltage was raised in increments of 10 V until the chip temperature reached about 100 °C or just a little over to ensure the fluid remained single phase.

8.7 Experimental Test Results

The fabricated coolers were tested under a variety of fluid pressures and power densities. Nine devices were chosen from the wafer to be packaged and tested. The devices were chosen to include a wide range of dimensions with some overlapping dimensions in both the microchannel width and the microchannel fin width. The chosen dimensions that were tested include:

- $m_w = 60$ μm, $m_f = 40$ μm, $N_{ch} = 54$
- $m_w = 60$ μm, $m_f = 60$ μm, $N_{ch} = 45$
- $m_w = 60$ μm, $m_f = 80$ μm, $N_{ch} = 39$
- $m_w = 80$ μm, $m_f = 80$ μm, $N_{ch} = 34$
- $m_w = 100$ μm, $m_f = 40$ μm, $N_{ch} = 39$
- $m_w = 100$ μm, $m_f = 60$ μm, $N_{ch} = 34$
- $m_w = 100$ μm, $m_f = 100$ μm, $N_{ch} = 27$
- $m_w = 120$ μm, $m_f = 60$ μm, $N_{ch} = 30$
- Blank

8.7.1 Tradeoff of Pressure Drop vs. Thermal Performance

As was discussed previously, there is a tradeoff between the pressure drop and the thermal performance. The average chip temperature rise is calculated by taking the average temperature obtained by the thermal camera in the center portion of the chip surface for each of the two chips and averaging them together. A typical plot is shown in Figure 8-15 for the blank device.

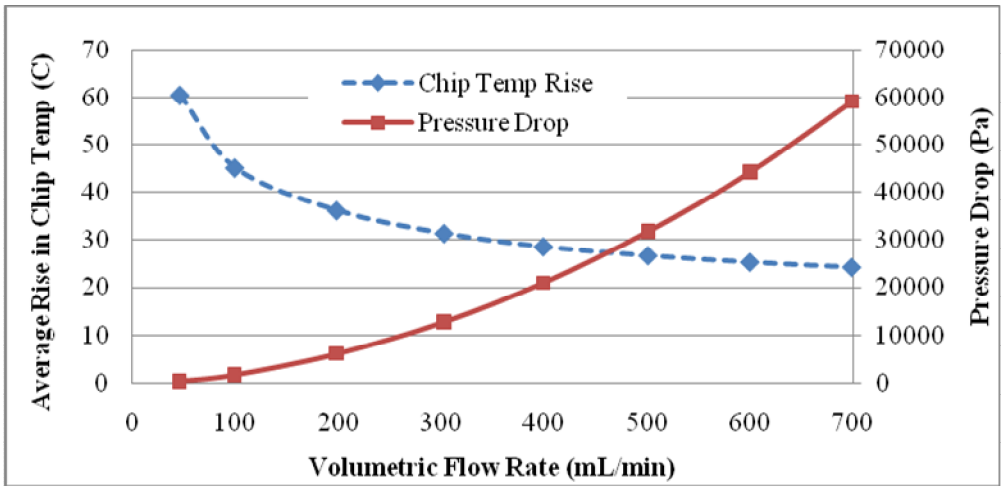


Figure 8-15: Tradeoff plot of pressure drop versus thermal performance for the blank device with no microchannels at 67 W (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm, no channels)

Tradeoff plots of each of the other eight geometries are shown in Figure 8-16. In each case, the tradeoff between thermal performance and pressure drop can clearly be seen. Additionally, an optimum flow rate can be found such that increasing flow beyond that flow rate produces minimal improvement in thermal performance while continuing to increase the system pressure drop. In most cases, this point appears to be around 200 - 300 mL/min but it is heavily dependent on the system requirements.

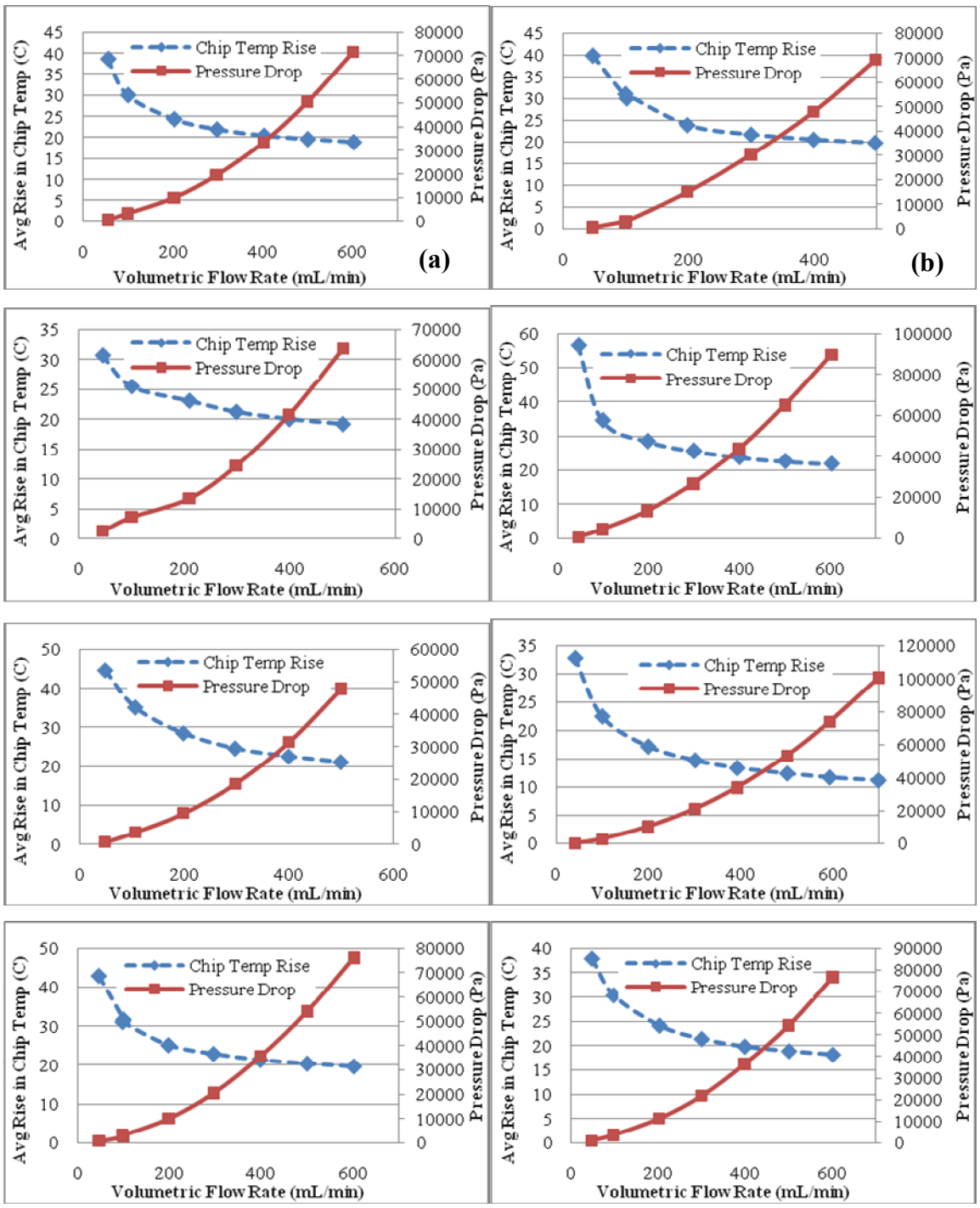


Figure 8-16: Tradeoff plot of pressure drop versus thermal performance for (a) m_w = 60 µm, m_f = 40 µm (b) m_w = 60 µm, m_f = 60 µm (c) m_w = 60 µm, m_f = 80 µm (d) m_w = 80 µm, m_f = 80 µm (e) m_w = 100 µm, m_f = 40 µm (f) m_w = 100 µm, m_f = 60 µm (g) m_w = 100 µm, m_f = 100 µm (h) m_w = 120 µm, m_f = 60 µm (67 W, M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

Figure 8-17 shows the measured pressure drop and thermal performance for each of the nine devices at 67 Watts power and a flow rate of 200 mL/min. Similar plots can be drawn at other power settings and flow rates. In this case it is clear by comparing the blank device to the other devices; the blank device has both the highest rise in device temperature and the lowest pressure drop, clearly showing the worst thermal performance. This is expected because it has no microchannels to enhance the thermal performance or to raise the pressure drop. The device which has the smallest rise in chip temperature is $m_w = 60$ µm, $m_f = 40$ µm. However, the highest pressure drop happens for the device with $m_w = 60$ µm, $m_f = 60$ µm. The blank device has a pressure drop 1.5 to 2.25 times smaller than any the devices with microchannels but its average rise in device temperature is 1.25 to 1.5 times higher. This would vary for other flow rates and powers.

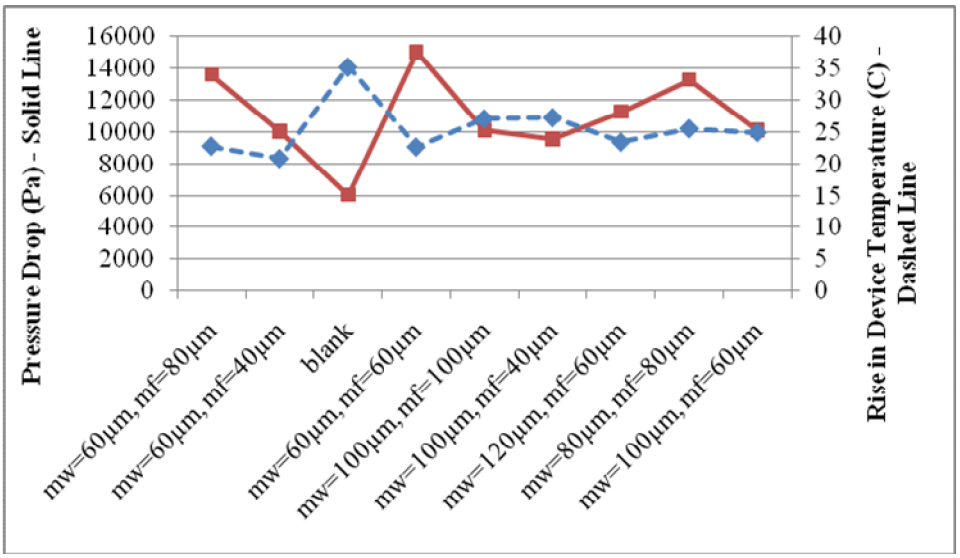


Figure 8-17: Tradeoff comparison plot of pressure drop versus thermal performance for all the devices at 67 W and 200 mL/min ($M_h = 1$ mm, $M_w = 550$ µm, $M_f = 150$ µm, $m_h = 150$ µm)

8.7.2 Pressure Drop Results

A plot of the pressure drop for each of the microchannel dimensions is shown in Figure 8-18. The blank device exhibits a lower pressure drop than all other devices.

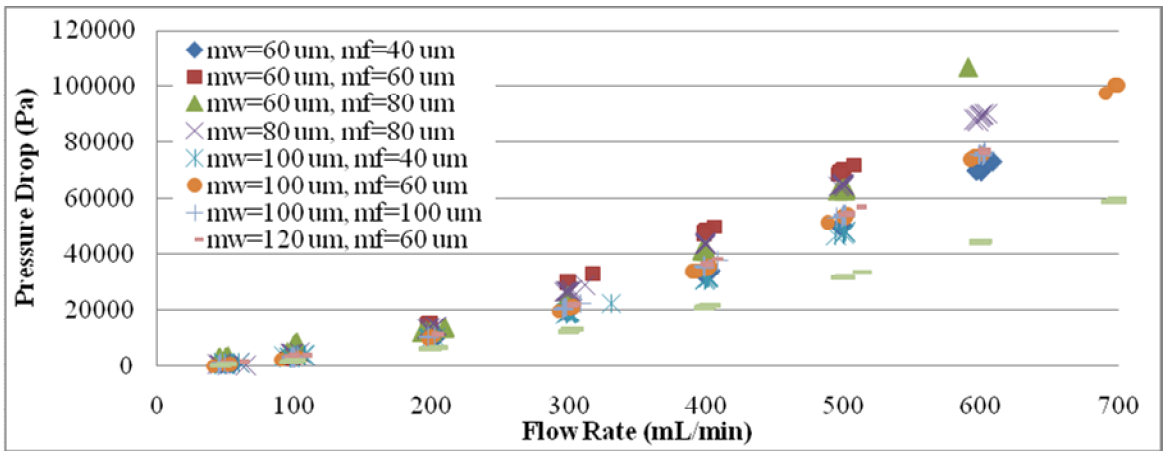


Figure 8-18: Graphical representation showing the flow rate versus pressure for the manifold microchannel cooler for all nine devices (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

A closer look at the two cases where the m_f varies and the m_w is constant at 60 µm and 100 µm is shown in Figure 8-19a and b, respectively.

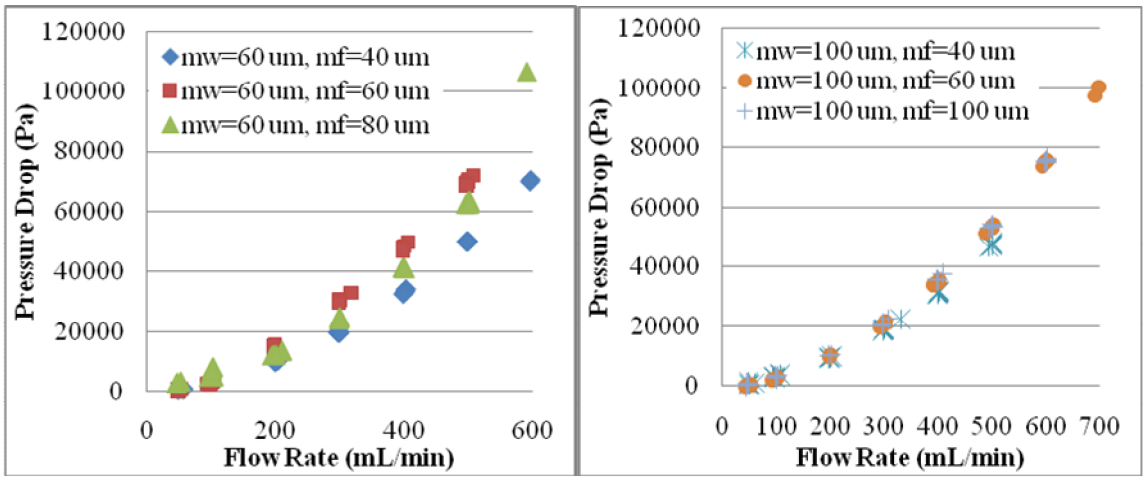


Figure 8-19: Graphical representation showing the flow rate versus pressure for the MMC cooler with varying microchannel fin dimensions at a constant microchannel width of (a) m_w = 60 µm and (b) m_w = 100 µm (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

A closer look at the case where the m_f is constant at 60 µm and the m_f varies from 60 µm to 120 µm is shown in Figure 8-19.

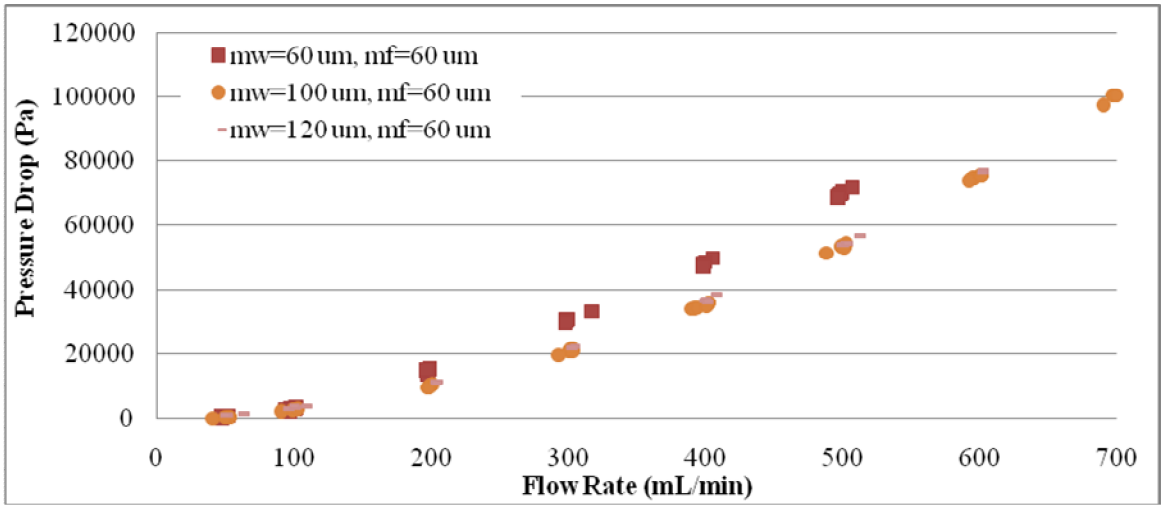
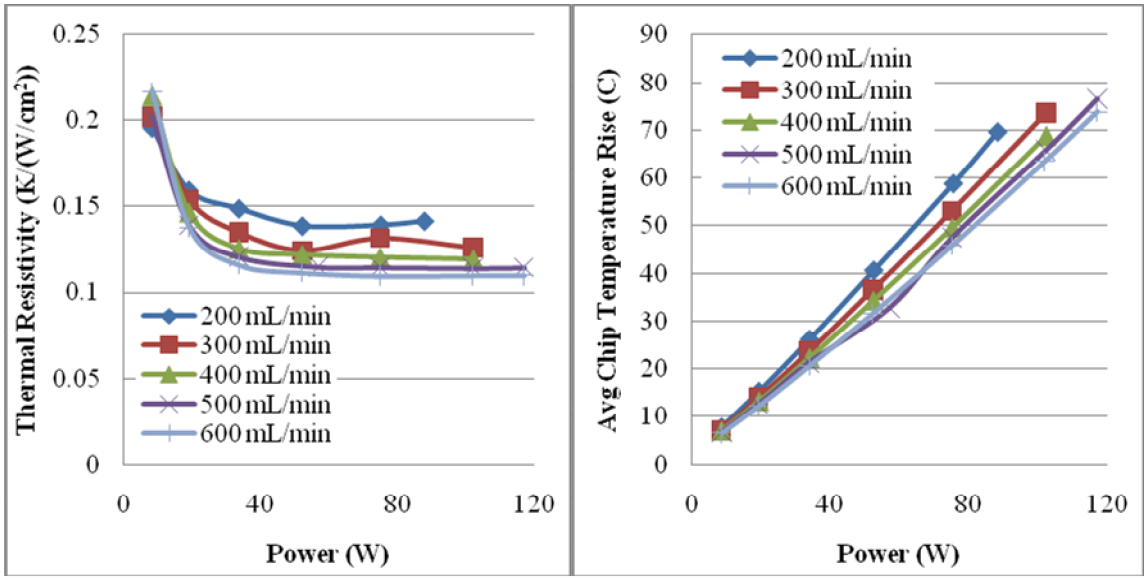


Figure 8-20: Graphical representation showing the flow rate versus pressure for the MMC cooler with varying microchannel width dimensions at a constant microchannel fin width of 60 µm (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

8.7.3 Experimental Thermal Performance

Figure 8-21 shows the thermal resistivity and the rise in chip temperature for various powers for a device with m_w = 100 µm and m_f = 60 µm. The graph on the left shows very low thermal resistivity values. For all flow rates, the thermal resistivity is <0.15 K/(W/cm^2) and for the flow rate of 600 mL/min, the thermal resistivity reaches a minimum at 0.11 K/(W/cm^2). This indicates that as the pressure drop increases (flow rate increases) the thermal resistivity decreases.



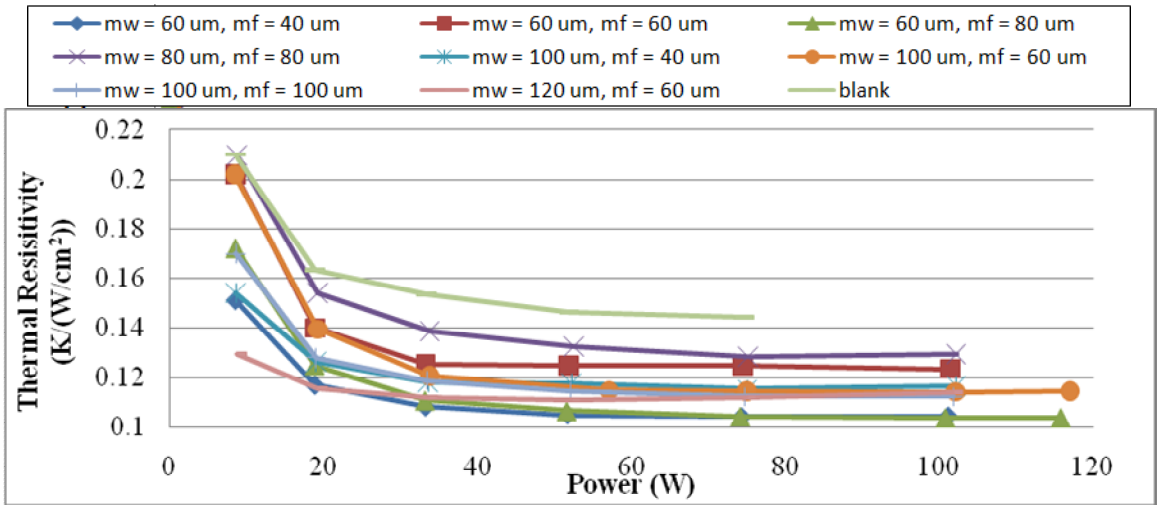
(a) (b)

Figure 8-21: Graphical representation for m_w = 100 µm, m_f = 60 µm of the (a) power versus change in the thermal resistance and (b) power versus average chip temperature rise (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

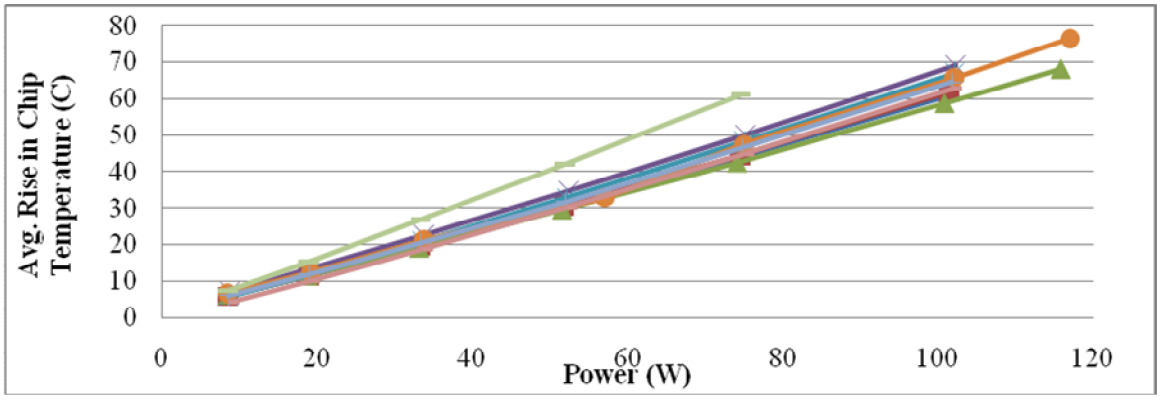
Figure 8-21b shows how the chip temperature rises linearly based on input power and pressure drop. For an input power of about 100 Watts at a 600 mL/min flow rate, the chip temperature has only increased by 63.4 ºC. At about 50 Watts of power and

600 mL/min, the chip temperature has increased 31.7 ºC. Therefore, experimental results show excellent cooling capabilities.

Figure 8-22a and b show the plots for 500 mL/min for the power versus the average chip temperature rise and the thermal resistivity, respectively. The blank device clearly has the highest thermal resistivity, with the m_w = 80 µm, m_f = 80 µm following. The best performance is by the m_w=60 µm, m_f = 80 µm device.



(a)



(b)

Figure 8-22: Graphical representation for various microchannel dimensions at 500 mL/min of the (a) power versus thermal resistance and (b) power versus average chip temperature rise (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

Figure 8-23 shows the results of the thermal resistivity at 200 mL/min for all the tested devices at 293 W/cm^2. Clearly the m_w = 60 µm, m_f = 80 µm performs the best but with a few devices performing very similarly, while the blank device performs the worst. The blank device shows on average a 1.33 X increase in thermal resistance over any of the devices with microchannels.

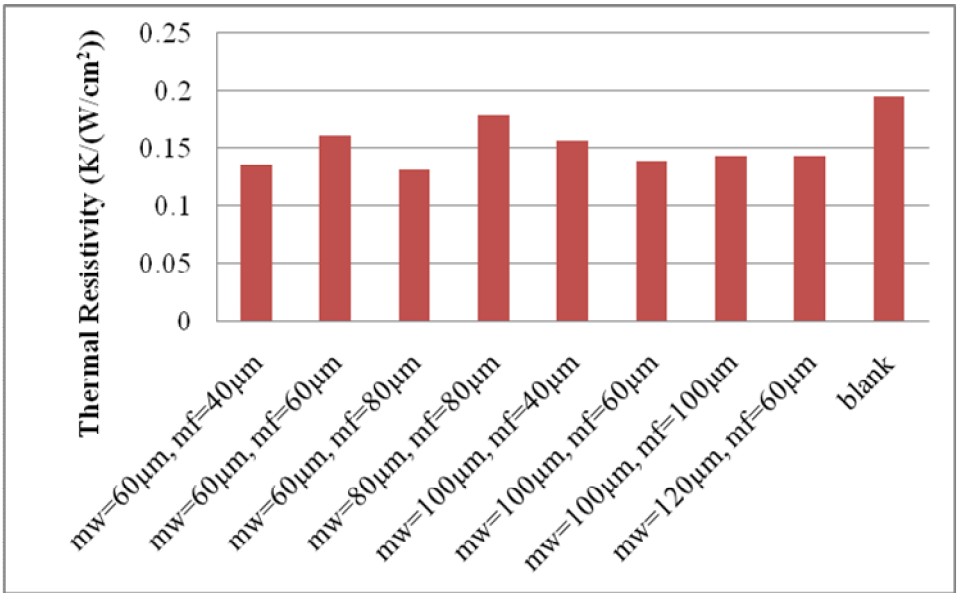


Figure 8-23: Plot of thermal resistivity for each of the tested devices at 293 W/cm^2 at 200 mL/min (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

The thermal resistivity as a function of flow rate for all the different channel dimensions is shown in Figure 8-24. At a flow rate of 300 mL/min, the thermal resistivities for the devices vary between 0.12 - 0.15 K/(W/cm^2) for all geometries except the blank device, which is 0.17 K/(W/cm^2).

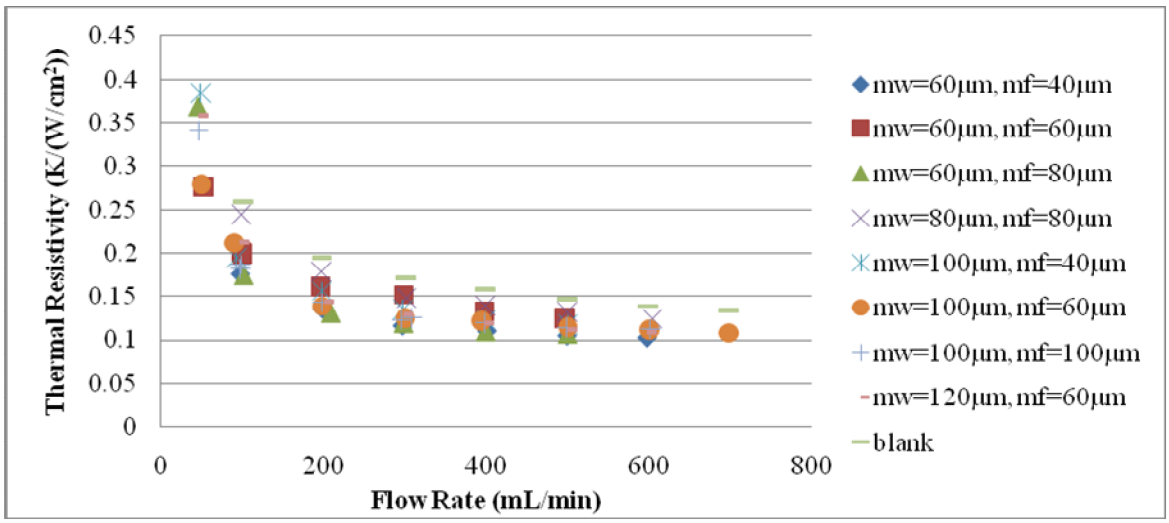


Figure 8-24: Plot of thermal resistivity as a function of volumetric flow rate for each of the tested devices at 52 W (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

Thermal camera images for each of the tested microchannel dimensions at 52 W and 300 mL/min are shown in Figure 8-25. The chip on the left is always the chip on the inlet side which is why it is slightly cooler than the chip on the right. Additionally the heat is generated only between the two electrical connections which is the area used for calculations.

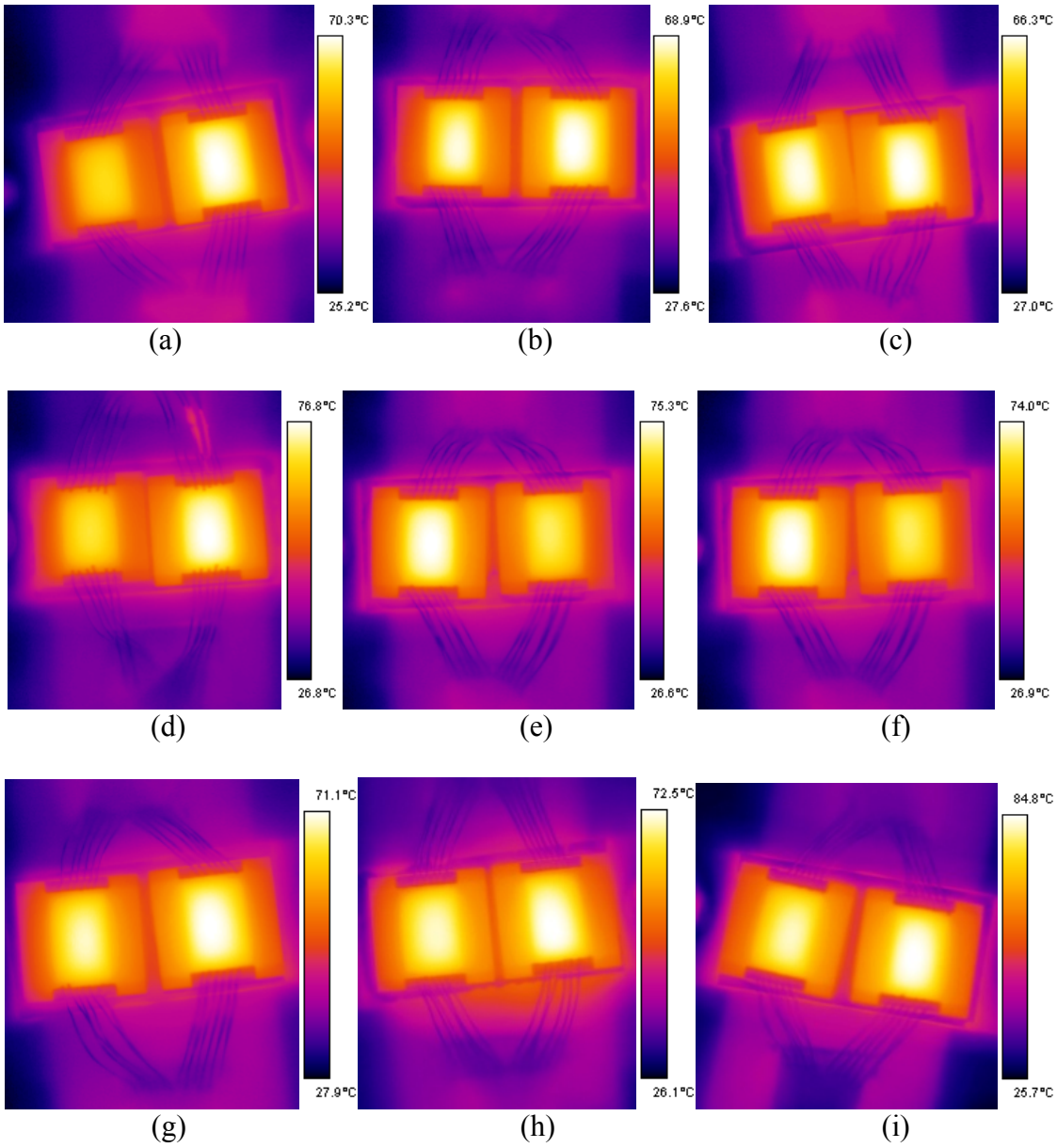


Figure 8-25: Thermal camera images for the tested devices at 50 V and 300 mL/min (a) m_w = 60 µm, m_f = 40 µm (b) m_w = 60 µm, m_f = 60 µm (c) m_w = 60 µm, m_f = 80 µm (d) m_w = 80 µm, m_f = 80 µm (e) m_w = 100 µm, m_f = 40 µm (f) m_w = 100 µm, m_f = 60 µm (g) m_w = 100 µm, m_f = 100 µm (h) m_w= 120 µm, m_f = 60 µm (i) blank (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

Figure 8-26 is a graphical representation of the difference in chip temperature between the first and the second chips. In most cases, the second chip is at least a few

degrees hotter than the first. This is expected because the fluid absorbs heat from the first chip before cooling the second chip.

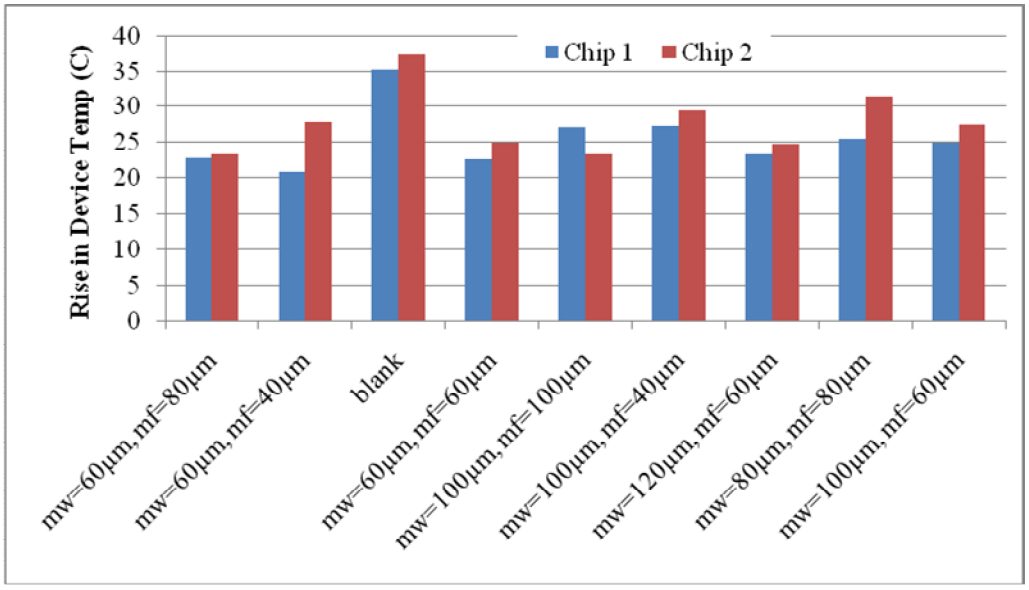


Figure 8-26: Plot of the average rise in chip temperatures for each chip for all the tested devices at a power dissipation of 67 W and a flow rate of 200 mL/min (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

Figure 8-27 shows the thermal images for the tested device with m_w = 60 µm and m_f = 60 µm at 52 W for flow rates varying between 50 – 500 mL/min.

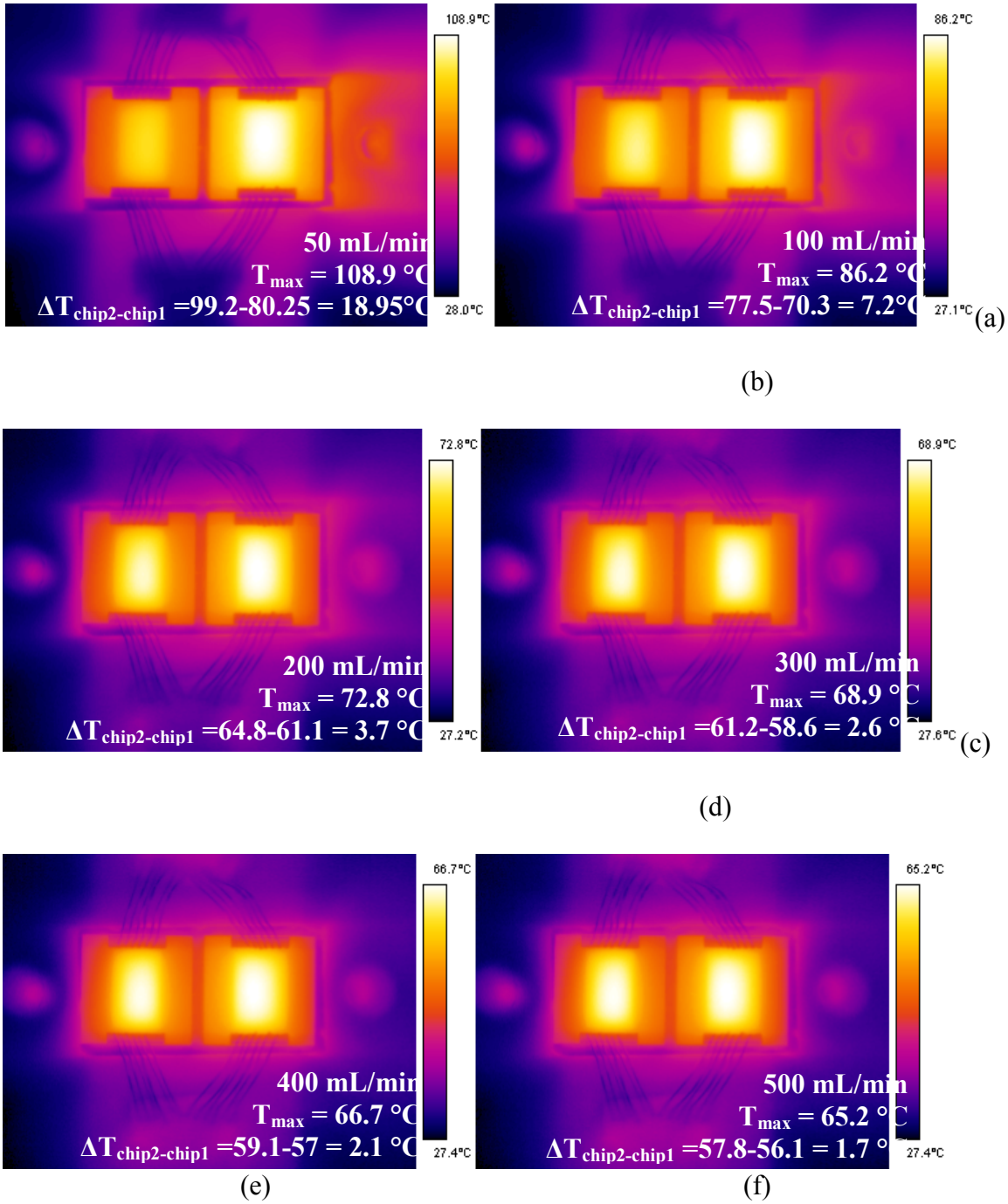


Figure 8-27: Thermal camera images for the device with m_w = 60 µm and m_f = 60 µm at 52 W (50 V) for various volumetric flow rates (a) 50 mL/min (b) 100 mL/min (c) 200 mL/min (d) 300 mL/min (e) 400 mL/min (f) 500 mL/min (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

Figure 8-28 is a graphical image of the type of data shown in Figure 8-27 but for a power of 33 W instead of 52 W. As the flow rate increases both the average device temperature and the gradient between the first and the second chips decrease.

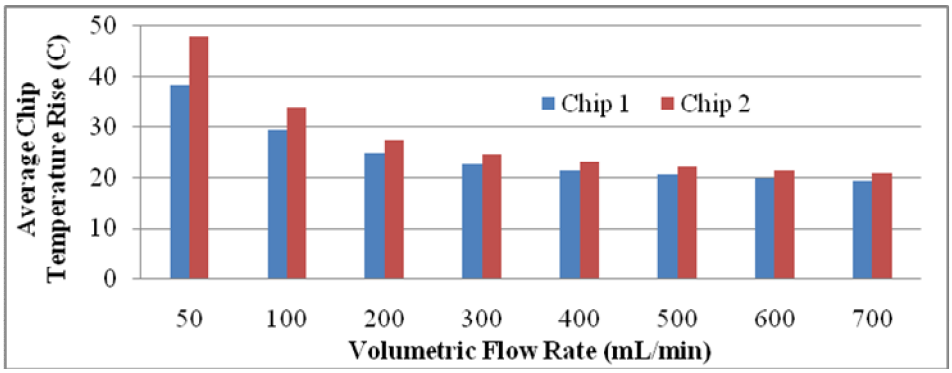


Figure 8-28: Graph showing the difference in average chip temperature rise for each of the two chips on a device with m_w = 100 µm and m_f = 60 µm at 33W (40 V) for various flow rates (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

Figure 8-29 shows the center chip line profiles for m_w = 100 µm, m_f = 60 µm at 67 W power dissipation at various flow rates. Clearly the second device is hotter than the first and this is even more apparent at lower flow rates. Additionally, both chips are slightly hotter on their side closer to the other chip which is probably due to heat transferring between devices.

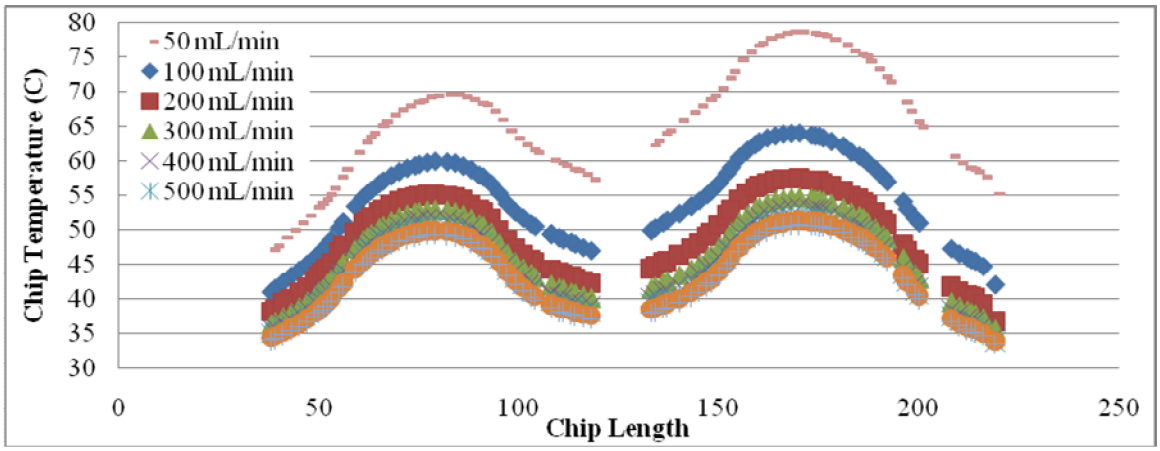


Figure 8-29: Chip surface temperature profiles for the device with m_w = 100 µm, m_f = 60 µm at 67 W of power dissipation and various flow rates (M_h = 1 mm, M_w = 550 µm, M_f = 150 µm, m_h = 150 µm)

The devices tested in this section incorporated an AlN electrical isolation layer and used standard AuSn as the die attach material. Nine different microchannel dimensions were packaged and tested including a blank device with no microchannels. The blank device experimentally showed pressure drops 1.5 to 2.25 times smaller and device temperatures between 1.25 to 1.5 times larger than any tested devices with microchannels (at 67 W and 200 mL/min). Thermal resistivity values were measured <0.3 K/(W/cm^2) and as low as 0.18 K/(W/cm^2), which is about 3 to 15 times better than standard power packages.

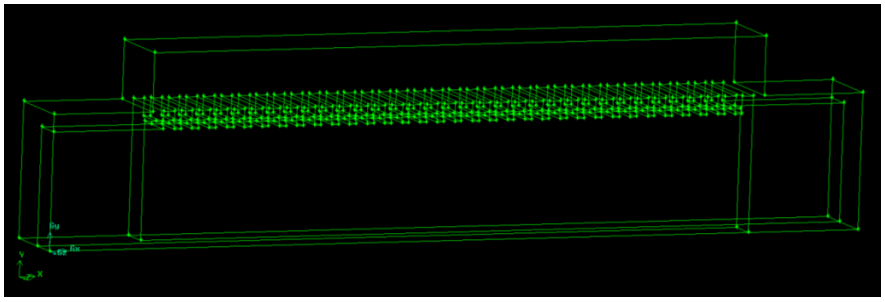
8.8 Simulation Results

The models that were run in Chapter 3 have been adjusted to correspond to three of the geometries that were experimentally tested. The simulations were rerun assuming the same boundary conditions and mesh density but the heat flux was assumed to be 161 W/cm^2, which corresponds to one of the experimental conditions. Each of the three geometries was run at 100 mL/min, which equates to an inlet velocity of 0.75 m/s into

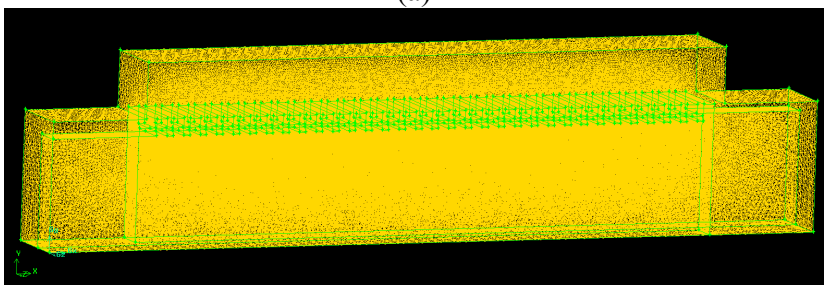
one of the manifold channels. One of the geometries was also simulated at a variety of other flow rates. As was the case in the fabricated channels, the Mw = 550 um, Mf = 150 um, Mh = 1000 um and mh = 150 um. The three modeled geometries and their flow rates include:

- m_w = 60 µm, m_f = 60 µm, N_{ch} = 45 at 100 mL/min
- m_w = 100 µm, m_f = 60 µm, N_{ch} = 34 at 25, 50, 100 and 200 mL/min
- m_w = 120 µm, m_f = 60 µm, N_{ch} = 30 at 100 mL/min

The geometry and the meshed structure for the m_w = 100 µm, m_f = 60 µm is shown in Figure 8-30 which has 34 microchannels. It has 1,611,097 fluid elements and 1,386,200 solid elements for a total of about 3 million elements. The model consists of a section of the chip and the portion of the cooling structure directly below the chip.



(a)



(b)

Figure 8-30: Pictures of the (a) geometry outline (b) meshed model for m_w = 100 µm, m_f = 60 µm with 34 microchannels and M_w = 550 µm, M_f = 150 µm, M_h = 1000 µm and m_h = 150 µm

While results were obtained for all the models run, a typical thermal result is shown in Figure 8-31 for when the m_w = 120 µm, m_f = 60 µm, N_{ch} = 30, M_w = 550 µm, M_f = 150 µm, M_h = 1000 µm, m_h = 150 µm, Q = 100 mL/min, and q" = 161 W/cm^2. This image shows the maximum chip temperature of around 326 K with the location of maximum chip temperature closer to the chip entrance than exit.

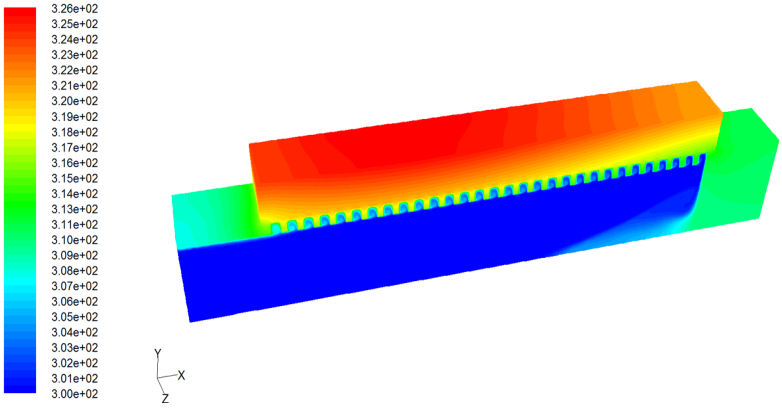


Figure 8-31: Typical thermal result for m_w = 120 µm, m_f = 60 µm, N_{ch} = 30, M_w = 550 µm, M_f = 150 µm, M_h = 1000 µm and m_h = 150 µm, Q = 100 mL/min, q" = 161 W/cm^2

Figure 8-32 shows the temperature contours for the three geometries through the center cut of each model. They are all shown at a flow rate of 100 mL/min and 161 W/cm^2. The images show that the device with mw = 60, mf = 60 has the lowest average device temperature. Additionally, the hottest part of each chip is located closer to the fluidic entrance than the exit.

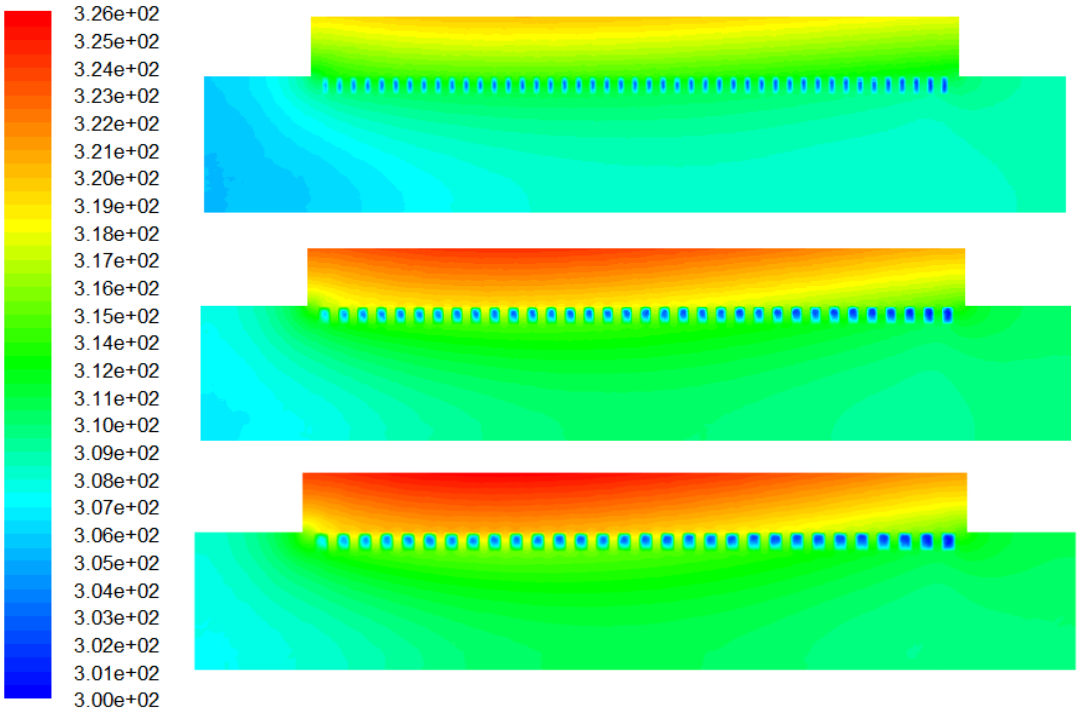


Figure 8-32: Center cuts through each of the three geometries depicting the thermal contours for (a) m_w = 60 µm, m_f = 60 µm, N_{ch} = 45 (b) m_w = 100 µm, m_f = 60 µm, N_{ch} = 34 (c) m_w = 120 µm, m_f = 60 µm, N_{ch} = 30 (M_w = 550 µm, M_f = 150 µm, M_h = 1000 µm, m_h = 150 µm, Q = 100 mL/min, q" = 161 W/cm^2)

The thermal images in Figure 8-32 show that the fluid in the microchannels is colder closer to the exit, which indicates a faster fluid velocity in these channels. This is indeed the case, as can be seen by the microchannel velocity plots in Figure 8-33. In each of the three cases, the microchannel velocity in each channel increases as the channels get closer to the exit. The reason for this was previously discussed in Section 4.1.

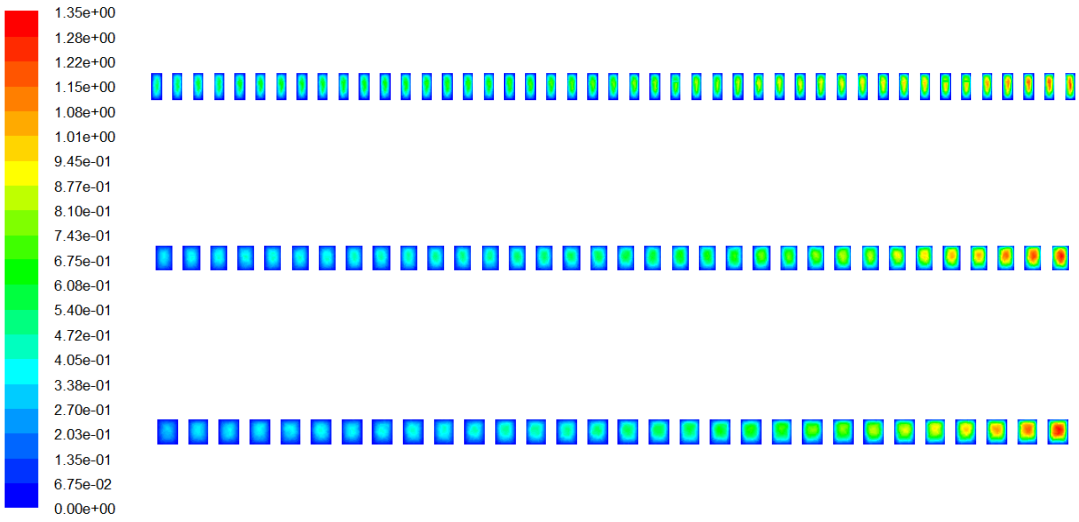


Figure 8-33: Velocity profiles through the center cut of the microchannels for each of the three geometries (a) m_w = 60 µm, m_f = 60 µm, N_{ch} = 45 (b) m_w = 100 µm, m_f = 60 µm, N_{ch} = 34 (c) m_w = 120 µm, m_f = 60 µm, N_{ch} = 30 (M_w = 550 µm, M_f = 150 µm, M_h = 1000 µm, m_h = 150 µm, Q = 100 mL/min, q" = 161 W/cm^2)

In each of the three geometries, the location of the max chip temperature is closer to the inlet as was previously discussed. Figure 8-34 shows the surface temperature profile for m_w = 120 µm, m_f = 60 µm. A similar profile can be made for each of the three geometries. Additionally this image shows that there is a temperature increase along the length of the microchannel which is due to the fact that a large manifold channel width was used in the MMC4 devices.

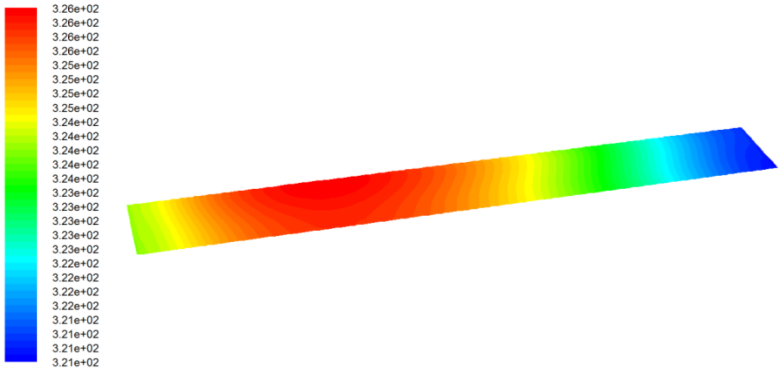


Figure 8-34: Thermal profile for the chip top for the device with m_w = 120 µm, m_f = 60 µm, N_{ch} = 30 (M_w = 550 µm, M_f = 150 µm, M_h = 1000 µm, m_h = 150 µm, Q = 100 mL/min, q" = 161 W/cm^2). Units are in degrees Kelvin.

In addition to the three geometries that were run, m_w = 100 µm, m_f = 60 µm was run for four different flow velocities, with the thermal results shown in Figure 8-35. As the flow rates increase, the amount fluid passing through the channel without being heated increases. Additionally, the hottest part of the chip progressively moves towards the inlet.

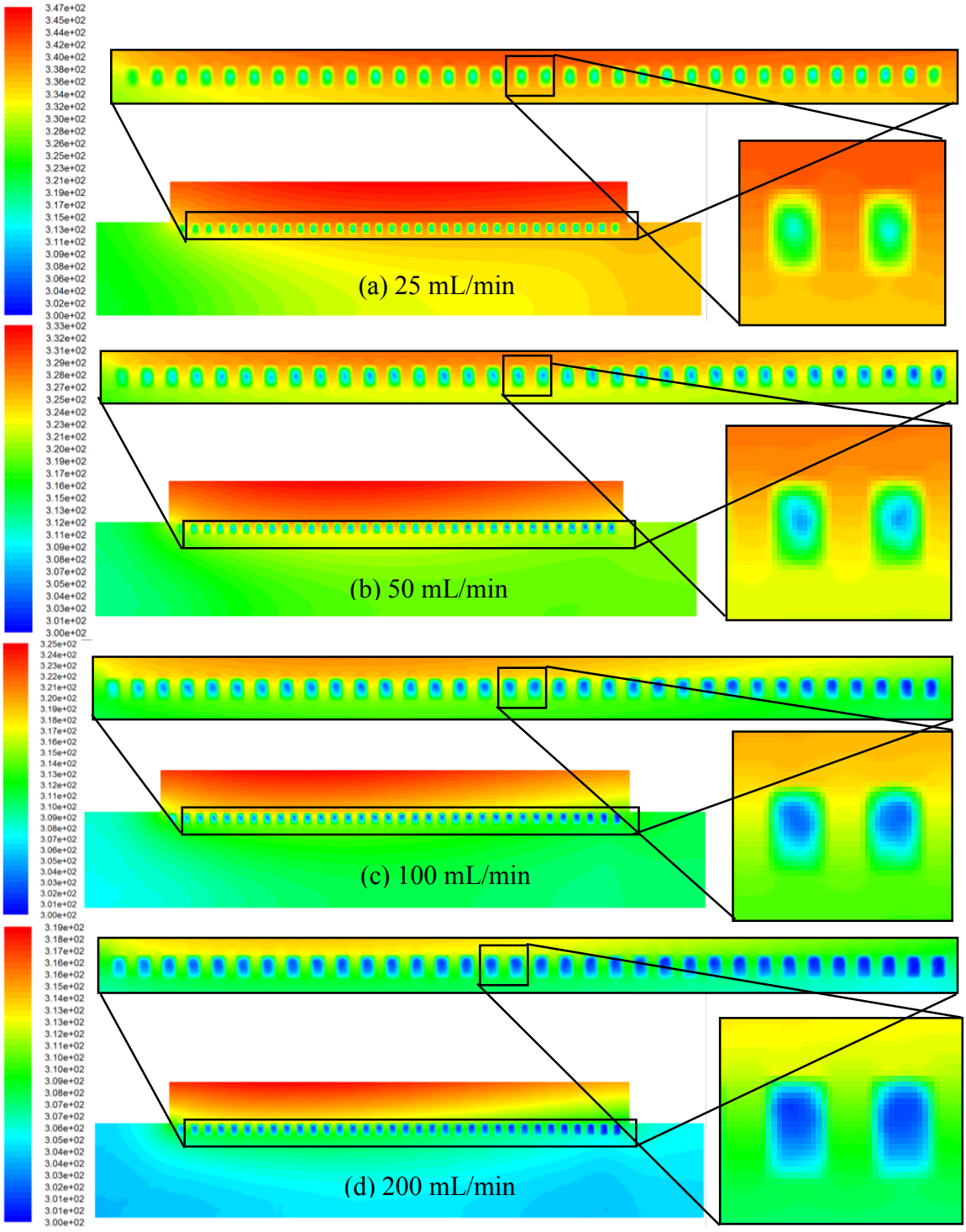


Figure 8-35: Thermal profile for the center cut with zoomed images of the microchannels and two of the center channels for m_w = 100 µm, m_f = 60 µm, N_{ch} = 30 at (a) 25 mL/min (b) 50 mL/min (c) 100 mL/min and (d) 200 mL/min (M_w = 550 µm, M_f = 150 µm, M_h = 1000 µm, m_h = 150 µm, q" = 161 W/cm^2). Units are in degrees Kelvin.

8.9 Comparing the Experiment to the Analytic and Numeric Results

Simulations were run with the same parameters as 5 of the test cases:

- m_w = 60 µm, m_f = 60 µm, N_{ch} = 45 at 100 mL/min
- m_w = 100 µm, m_f = 60 µm, N_{ch} = 34 at 50 mL/min
- m_w = 100 µm, m_f = 60 µm, N_{ch} = 34 at 100 mL/min
- m_w = 100 µm, m_f = 60 µm, N_{ch} = 34 at 200 mL/min
- m_w = 120 µm, m_f = 60 µm, N_{ch} = 30 at 100 mL/min

8.9.1 Pressure Drop Comparison

A plot comparing the numerical, analytical and experimental results is shown in Figure 8-36. The analytical results are obtained using the first order pressure drop calculations derived in 3.2.2. The graph shows very good agreement between the three results.

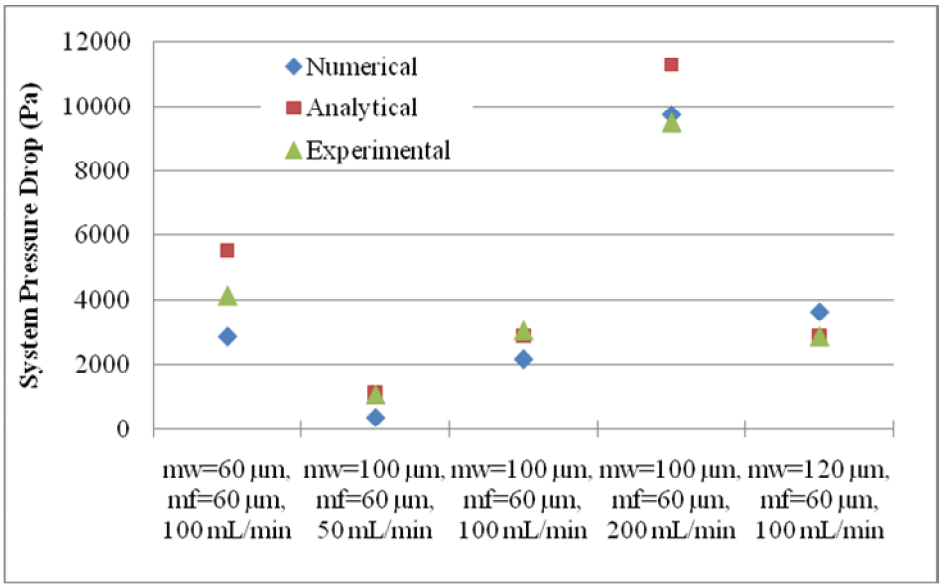


Figure 8-36: Plot comparing the pressure drops obtained from the numerical, analytical and experimental results showing very good correlation

8.9.2 Thermal Results Comparison

The models were run assuming a silicon chip intimately in contact with the fluidic channels which is not the case in the experiment. In the experiment, there is a layer of aluminum nitride and a gold-tin solder layer both between the device and AlN and also between the AlN and the microchannels. Additionally, the device is a 1 mm thick AlN chip resistor and not a 500 μm silicon device as was assumed in the model. Therefore, these additional resistances had to be added to the model results using thermal resistance equations from Appendix B.1.3. This was done by adding the additional thermal resistivities imposed by the 1 mm thick AlN chip resistor, the 2-mil thick AuSn solder layer, the 380 μm thick AlN electrical isolation layer and the 2 μm thick AuSn microchannel bond then subtracting the resistivity imposed by the 500 μm thick silicon chip from the Fluent model.

The model was defined such that all the heat was transferred to the fluid and not lost to the ambient. In the experiment some heat is lost to the ambient and to other parts of the system, therefore, to make a good comparison, only the heat that is transferred to the fluid during the experiment will be used. The heat that is transferred to the fluid (Q_{fluid}) is calculated by using the convective heat transfer equation:

$$Q_{fluid} = \dot{m} C_p \Delta T \tag{8-1}$$

In the above equation, Q_{fluid} is the heat transferred to the fluid (W), $\dot{m}$ is the mass flow rate (kg/sec), C_p is the specific heat of water (J/(kg*K)) and ΔT is the rise in fluid temperature (K).

As was shown in Figure 8-13, the majority of the heat is only generated in the resistive film between the two electrical connections. This is also the area of which the

average chip temperature rise is measured during the experiment. Therefore, in order to determine the appropriate heat flux in W/cm^2, the heat transferred to the fluid (Q_{fluid}) is divided by the center heated area which is measured to be 0.177 cm^2. The thermal resistivity is then calculated by dividing the rise in device temperature by the newly calculated heat flux.

Both the theoretical and experimental values of the thermal resistivity for each of the five models are plotted in Figure 8-37. The numerical results include the calculated interfacial layer resistances of the metallization layers and the AlN layers. The correlation between the numerical and experimental is very good. In most cases, the experimental results are slightly higher than the numerical results and this is expected due to the fact that any additional thermal resistances caused by imperfect bonding or other imperfections is not accounted for in the additional thermal resistances.

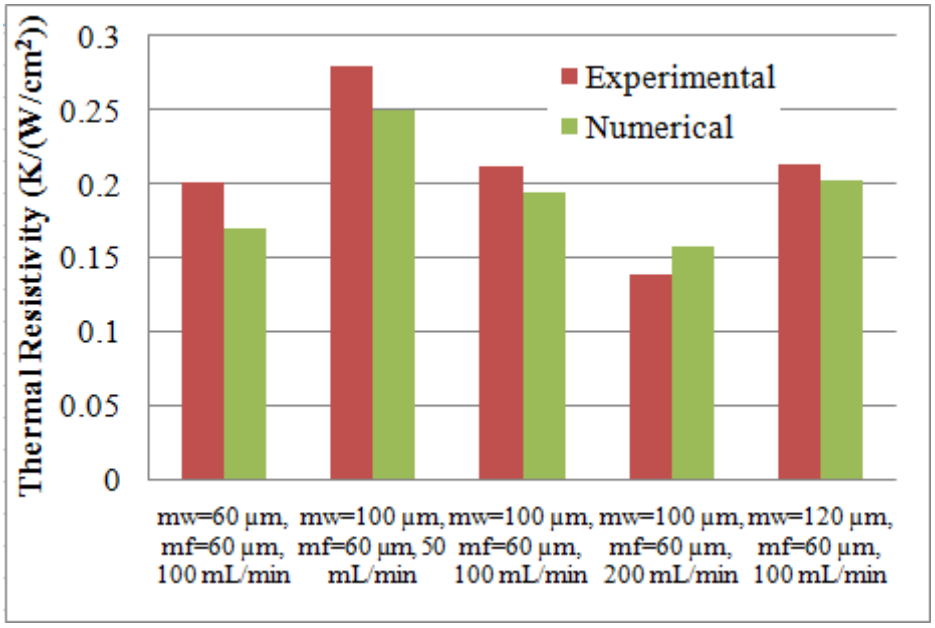


Figure 8-37: Plot comparing the numerical to experimental results of the rise in chip temperature for each of the five models

9 Summary, Conclusions, Contributions and Future Work

The MMC has been shown to alleviate the inherent problems associated with straight microchannels. Past researchers who have looked into the MMC design have not had much experimental data to correlate with their models and the models have not accounted for the full manifolded structure. Therefore, this study assessed the MMC design and explored its implementation into actual power modules. This research has focused on fabricating the MMC directly into the substrate of an electronics package both with and without electrical isolation between the device and fluid. The goal of this research has been to minimize the thermal resistance, reduce the package size, improve the uniformity of the chip surface and reduce the system pressure drop. It achieved this goal by modeling and demonstrating the use of a MMC fabricated directly into the substrate of an electronics package.

9.1 Experimental Conclusions

In order to demonstrate experimentally both the thermal performance and the improved pressure drop, the MMC structure was fabricated directly into a substrate powered by devices. Four versions of the MMC design were microfabricated: MMC1, MMC2, MMC3 and MMC4. MMC1 was the first prototype, the main purpose of which was to prove the fabrication sequence. MMC2 was a fully-functioning MMC cooler with the channels intimately contacting the backside of the die, thus having no electrical isolation. MMC3 was fabricated incorporating a thin silicon dioxide membrane as an electrical isolation layer. Due to failures occurring in MMC3, the device was redesigned utilizing a AlN layer for electrical isolation instead. The device was packaged in two

different ways and each of these was experimentally tested. A summary of the results from MMC2, MMC3 and MMC4 are discussed here.

MMC2 was fabricated into a single 1 mm silicon wafer that was DRIE etched from both sides. The microchannels were 20 μm wide with 20 μm fins. There was no electrical isolation between the device and the cooling fluid. A SiC diode was attached using a thin film AuSn attach which has been shown to be an effective fluidic seal to pressure drops above 207 kPa. The fabrication procedure is easily reproducible and uses standard MEMS techniques. The cooler has shown excellent thermal results with thermal resistances less than 0.09 K/(W/cm^2) and as low as around 0.06 K/(W/cm^2) at higher flow rates. Heat fluxes over 600 W/cm^2 were shown experimentally with an increase in chip temperature of only 45 ºC. **This device has shown a 10 to 50 times improvement in thermal resistivity values over standard power packaging technology, which has a thermal resistivity between 0.6 - 3.3 K/(W/cm^2).**

MMC2 did not incorporate an electrical isolation layer; therefore, MMC3 was designed with a silicon dioxide membrane between the device and the fluidic channels. Additionally, the fabrication sequence was altered to allow for: incorporating larger and various sized microchannels, fabricating the manifolds and the microchannels in two separate wafers, and using a silicon diode to allow a more uniform temperature distribution. Other changes were also made that allowed lower pressure drop, more devices per wafer, and to allow a dual-chip module. Unfortunately, testing indicated resistive heating of the backside metallization which caused failure of the backside connection. While an oxide membrane can still be used with a redesign of the fabrication, it was decided to also look into using an AlN layer as the electrical isolation layer.

MMC4 was fabricated to incorporate AlN as the electrical isolation layer. The design of MMC4 is the same as MMC3 in terms of microchannel and manifold dimensions and structure, but the bonding process had to be changed due to the additional bonding layer. The thicker AlN has very similar thermal properties to the oxide membrane but it can allow for standard bonding processes for the die attachment. The initial set of MMC4 devices were die attached using a silver polyimide paste. The results of the testing show very good thermal performance of this device with thermal resistivity values of around 0.15 K/(W/cm^2).

Due to the low thermal conductivity of the P1011 and the desire to make a more reliable bonding process, a new set of devices was fabricated which used a standard AuSn solder. Nine different microchannel dimensions were packaged and tested under a variety of fluid pressures and power densities including a blank device with included manifold channels with no microchannels. The blank device experimentally showed pressure drops 1.5 to 2.5 times smaller and thermal resistivities on average of 1.33 X larger than any tested devices with microchannels (at 293 W/cm^2 and 200 mL/min). Thermal resistivity values were measured as low as 0.104 K/(W/cm^2). The thermal resistivity of these devices is less than 2 X larger than the thermal resistivity for MMC2 which has no electrical isolation. But this is expected because of the additional layers which add to the thermal resistance. **This device, with an incorporated AlN electrical isolation layer, showed thermal resistivity values 7 to 30 X better than standard power packages.**

9.2 Modeling Conclusions

In order to understand the complicated relationships between dimensions, thermal performance and pressure drops in manifold microchannel structures, a series of models were performed using the commercially available CFD software Fluent. The modeling in this thesis included a complete analysis of a single geometry and a parametric study of multiple geometric parameters including the manifold height (M_h), manifold fin width (M_f), manifold channel width (M_w), chip length (L_{chip}), microchannel width (m_w) and microchannel fin width (m_f). The modeling in this work has expanded on previous modeling by including both the inlet and exit manifold channels along with all the microchannels instead of just an individual microchannel unit cell. This is necessary because, as was shown in this work, there is extreme variation in the microchannel velocities along the length of the chip. Some models have shown that the microchannels that are closest to the exit have velocities that are 10 times greater in magnitude than the channels closest to the entrance along with impacting the device temperature. This velocity maldistribution impacts the device temperature by moving the hot spot from the exit to closer to the center which decreases the chip non-uniformity and impacts the power loss, reliability and electrical performance.

9.2.1 Pressure Drop Calculation Results

Both a zeroth and a first order pressure drop equations have been developed for the MMC system. The pressure drops in the manifold channels and the microchannels were calculated using the Hagen-Poiseuille equation, which has been adjusted for a rectangular cross section. The zeroth order pressure drop equation has been developed to be:

$$\Delta p = 8\mu Q\left(\frac{L_{manifold}\left(M_w + M_h\right)^2}{\left(M_w \times M_h\right)^3} + \frac{\left(M_w + M_f\right)\left(m_w + m_h\right)^2}{2N_{ch}\left(m_w \times m_h\right)^3} \right) \quad (9\text{-}1)$$

The zeroth order approximation has been shown to underestimate the model result by about 50% which allows it to be readily used for design and comparison purposes. But the zeroth order equation is missing a number of minor losses that are accounted for in a first order approximation.

The four types of minor losses that were accounted for in the first order approximation are: entrance losses, 90° bend losses, losses down the manifold, and expansion losses. All of these minor pressure losses are based on the Darcy-Weisbach pressure drop equation where a loss factor K is calculated for each minor loss. The pressure drops from each of the losses is added to the zeroth order pressure drop equation to obtain a total system pressure drop. This first order pressure drop equation shows an average error of about 35% which is a 15% improvement over the zeroth order.

9.2.2 Results of Modeling a Single Geometry

The results of a single geometry were analyzed in depth for various inlet flow rates to show the effect on pressure, thermal performance and flow conditions. The geometry that was analyzed had parameters: $M_w = 200$ μm, $M_f = 50$ μm, $M_h = 750$ μm, $m_w = 100$ μm, $m_f = 100$ μm, $m_h = 150$ μm, $N_{ch} = 10$, $L_{inlet} = 2$ mm, q" = 400 W/cm^2. As is the case with any geometry, a plot can be made showing the tradeoff between the pressure drop and the thermal performance. Increased flow rates improve thermal performance but increase system pressure drop. A flow rate can be found such that any additional increase in the flow rate would cause less than a 1 °C improvement in the chip temperature.

Analyzing the thermal results of the model shows that there is quite a bit of heat transfer to the manifold at low flow rates, while at high flow rates, most of the fluid passes through the microchannels with minimal heat absorption. Additionally, the location of the maximum chip temperature was shown to shift from closer to the exit to being more centralized as the flow rates increase. This is because as the inlet velocity increases, so does the velocity variation in the microchannels, with the microchannels closest to the exit having higher velocities. This additional flow counteracts the heating along the channel which causes the hot spot to be more centralized.

Analyzing the velocity profiles has indicated a stagnation region in the microchannel directly above the center of the inlet manifold channel. The location of the maximum velocity typically occurs in the microchannel closest to the exit. The fluid flow through each microchannel forms a loop path which is more pronounced at higher velocities. Pressure contours show how the pressure drops decrease from the inlet to the exit. **Comparing this MMC structure to a comparable straight microchannel design has shown similar thermal performance but an almost 40 times improvement in pressure drop.**

9.2.3 Results of Varying Geometric Parameters

Models were performed to analyze the effects of varying both the manifold and the microchannel dimensions on the overall system performance including the manifold width (M_w), manifold fin width (M_f), manifold height (M_h), microchannel width (m_w), microchannel fin width (m_f), microchannel height (m_h), and the chip length (L_{chip}).

9.2.3.1 Varying Manifold Height (M_h)

It can be concluded that there is in fact an optimum manifold height. Since the height has very little influence on the chip temperature, but a significant effect on the pressure drop, in general a larger manifold height would be better because it would decrease the pressure drop. However, there is a point at which the improvement in pressure drop outweighs the increase in size or additional manufacturing difficulty.

9.2.3.2 Varying Manifold Fin Width (M_f)

After analyzing the effect of the M_f on the performance, it has been shown that it should be minimized. For a constant system volumetric flow rate, increasing the M_f has very little effect on the thermal performance but causes the pressure drop to increase. For a constant volumetric flow rate, increasing the M_f has very little effect on the pressure drop, but it causes the device temperature to rise. Therefore, in both cases, it is desirable to minimize the M_f. The limit to which the M_f can be minimized is based on fabrication limitations. It was also shown that as M_f is varied for a given flow rate, the location of the hottest spot on the chip and the magnitude of chip non-uniformity remain the same.

9.2.3.3 Varying Manifold Width (M_w)

For a constant system volumetric flow rate, as the M_w increases, so does the average rise in chip temperature due to a stagnation region forming above the manifold channel in the microchannel. There has been determined that an M_w can be found which minimizes the system pressure drop. This minimum occurs because of the tradeoff between the pressure drop in the manifold and the microchannel. At smaller manifold widths, the pressure drop in the manifold dominates and at larger manifold widths, the

pressure drop in the microchannel dominates. For a constant volumetric flow rate, the chip temperature rises substantially and the pressure drop decreases substantially when the M_w is increased. Therefore, since both the thermal performance and pressure drop are significantly affected by varying the manifold width, determining the correct M_w for a given system will be heavily dependent on the intended application.

9.2.3.4 Varying Microchannel Dimensions (m_w and m_f)

In order to determine the effect of varying the m_w and the m_f, four microchannel geometries were modeled with varying dimensions. The results have shown that the m_w has a larger impact on the thermal performance than the m_f. It has been shown that the zeroth order pressure drop calculations do a good job of showing the trend of the effect of the microchannel dimensions on performance. The calculations have shown that there is an optimum m_w which reduces the pressure drop and that the m_f should be minimized when the flow rate into the manifold is held constant.

9.2.3.5 Varying Chip Length (L_{chip})

Since devices vary quite a bit in size, it is interesting to look at how the chip length affects the performance. When the flow rate per microchannel is constant and the chip length is increased, both the pressure drop and chip temperature increase due to the additional manifold length. Using the zeroth order pressure drop equations with a constant microchannel velocity, it was shown that as the m_f is increased, the pressure drop decreases; therefore, m_f should be maximized when the microchannel velocity is assumed constant. Each chip length has an optimum m_w which increases as the chip length increases. When the volumetric flow rate into the system is constant and the chip

length is increased, the average chip temperature rises due to the decreased flow through each channel. Additionally, increasing chip length causes the pressure drop to decrease because the total system pressure drop starts to approximate the manifold channel alone, which decreases with increasing chip length.

9.3 Contributions

At the completion of this study, the main contributions I have made include:

- Fabricating and testing the first ever microfabricated multi-chip design for the manifold microchannel. The MMC design was incorporated directly into the substrate allowing significant thermal stack reduction.
    - The MMC2 design has experimentally demonstrated up to a 50 X improvement in thermal resistivity over a standard power package with significant size and weight reduction, while the MMC4 design has experimentally demonstrated up to a 15 X improvement in thermal resistivity.
    - The design has been fabricated both with (MMC4) and without (MMC2) an electrical isolation layer that can hold off over 6000 V.
    - When comparing the MMC design to the straight microchannel, it was shown that for a design with similar thermal performance, there is a 38 X improvement in system pressure drop.
- Proved that a simple zeroth order pressure drop equation, developed from the Hagen-Poiseuille pressure drop equation, can be used to help a designer determine how different dimensions impact the system pressure drop.

- Creating the first MMC numerical model that incorporates all the microchannels and not just a single microchannel. Simply modeling a single manifold unit cell is not sufficient to understanding the complex flow in a manifold microchannel structure as there are significant differences in the flow properties of each microchannel.
- Creating the first ever full sensitivity analysis of the impact of various manufacturable MMC parameters on the system pressure drop and thermal performance. The dimensions that were analyzed include the manifold height, manifold width, manifold fin width, microchannel width and microchannel spacing. Plots were also developed to show the tradeoff between the pressure drop and thermal performance for various flow rates and dimensional parameters. These plots are critical for designers in determining the required dimensions for their intended application.

9.4 Future Work

Three areas in which this technology can be advanced are manufacturing the cooler from another material, exploring two-phase cooling, and varying dimensions to control flow rates.

9.4.1 Fabricate MMC Structure in an Alternative Material

Silicon was chosen as the material of choice in this study mainly for its manufacturability. Established MEMS processes have made fabricating the complicated MMC structure possible. But, as was discussed previously in Section 1.9, there are a

number of alternative materials to silicon that might be more appropriate for use as a substrate material.

The ideal MMC substrate material would be hard, durable, highly thermally conductive, electrically isolating, and easy to precisely machine small channels. Silicon has many of these properties but it is not durable or electrically isolating. The material that has almost all of these properties is a ceramic, specifically aluminum nitride (AlN). AlN has the distinct benefit of being both highly thermally conductive and electrically isolating. It is also currently used commercially as a substrate material in direct bond copper (DBC). The disadvantage of using AlN as the substrate material for a MMC structure is that it is extremely hard to machine, especially small features. Therefore, a future study could look into techniques for fabricating the MMC structure out of AlN.

9.4.2 Assess MMC Structure with a 2-Phase System

Two-phase systems have been shown to be a very effective way to cool electronics systems due to the higher heat transfer coefficients, more isothermal surface and reduced pumping power for the same heat transfer rate [33, 34]. Therefore, incorporating them along with a MMC design could be very interesting. But a two phase cooling will significantly increase the complexity of the design along with adding the potential for system failure due to dry out.

9.4.3 Vary Dimensions to Control Channel Flow Rates

As was pointed out in this thesis, there can be substantial variation between the flow rates in each channel. Therefore, a study that looks into varying either the manifold and or microchannel dimensions to better control the deviation of the flow rates in the

microchannels would be beneficial. This could be done by changing the shape of the individual microchannels to make the ones closest to the exit smaller than the ones closer to the entrance, or vice versa. Or it could also be done by changing the shape of the manifold such that it is tapered down the length of the manifold and an opposite shape for the exit manifold. Additionally, the inlet and exit manifolds were assumed to be the same shape in this study but looking into varying their shapes independently of each other could help to balance and control the velocities in the microchannels as well.

Appendix ANomenclature

A	=	channel cross sectional area (m^2)
A_{chip}	=	chip area (m^2)
C_p	=	specific heat (J/kgK)
D_h	=	hydraulic diameter (m)
h	=	convection coefficient (W/m^2K)
H	=	rectangular channel height (m)
I	=	current (A)
k	=	thermal conductivity (W/mK)
L	=	channel length (m)
L_{chip}	=	length of chip (m)
$L_{microchannel}$	=	microchannel lenght
m_w	=	microchannel width (μm)
m_f	=	microchannel fin width (μm)
m_h	=	microchannel height (μm)
M_w	=	Manifold width (μm)
M_f	=	Manifold fin width (μm)
M_h	=	Manifold height (μm)
N_{ch}	=	number of microchannels
$N_{manifold}$	=	number of manifold channels
P	=	pumping power (W)
P_e	=	electrical power (W)
p	=	pressure (Pa)

p_{in}	=	inlet pressure (Pa)
p_{out}	=	outlet pressure (Pa)
Δp	=	system pressure drop (Pa)
$\Delta p_{manifold}$	=	manifold pressure drop (Pa)
$\Delta p_{microchannel}$	=	microchannel pressure drop (Pa)
Q	=	fluid volumetric flow rate (mL/min)
Q_{system}	=	system volumetric flow rate (mL/min)
q	=	heat flow (W)
q’	=	heat flow per length (W/m)
q”	=	heat flux (W/m^2)
R	=	thermal resistivity ($K/(W/cm^2)$)
Re	=	Reynold’s number
R_e	=	electrical resistance (Ω)
R_{th}	=	thermal resistance ($K\text{-}cm^2/W$)
t	=	thickness (m)
T	=	temperature (C)
T_{fluid_in}	=	inlet fluid temperature (C or K)
T_{fluid_out}	=	outlet fluid temperature (C or K)
ΔT_{fluid}	=	change in fluid temperature (C or K)
T_{chip}	=	average chip surface temperature (C or K)
ΔT_{chip}	=	increase in chip temperature (C or K)
$\Delta T_{chip\_surface}$	=	difference in temperature across chip surface (C or K)

T_{chip_max}	=	max chip temperature
T_{chip_min}	=	min chip temperature
U	=	perimeter of cross-section
v_{in}	=	inlet velocity (m/s)
v	=	velocity (m/s)
$v_{microchannel}$	=	microchannel velocity (m/s)
V	=	voltage (V)
W	=	rectangular channel width (m)

Greek Symbols

μ	=	dynamic viscosity
ν	=	kinematic viscosity
ρ	=	density

Appendix BEquations of Heat Transfer and Fluid Flow

A brief overview of classical equations of both heat transfer and channel flow equations used in this thesis are presented here.

B.1 Heat Transfer

There are three types of heat transfer: conduction, convection, and radiation. In this paper, the primary modes of heat transfer are conduction and convection so radiation will be ignored. Each of these are presented in more detail below.

B.1.1 Conduction

Conduction is the method of heat transfer in a solid object. The standard equation of conduction heat transfer, known as Fourier's Law, is:

$$q'' = \frac{q}{A} = k\frac{dT}{dx} \tag{B-1}$$

In this equation, k is the thermal conductivity of the material (W/mK) and A is the area over which the heat is being applied (m^2). T is the temperature (C), x is the distance through the solid (m), q is the input power (W), and q" is the heat flux (W/cm^2).

B.1.2 Convection

Convection is the method of heat transfer where a fluid is moved along a surface to cool the surface. The main equation for convection is:

$$q = hA\Delta T \tag{B-2}$$

In this equation, h is the convective heat transfer coefficient of the fluid (W/m^2K), ΔT is the difference in temperature between the surface and the fluid, A is surface area of the heat transfer (m^2), and q is the power (W).

B.1.3 Thermal Resistance

Thermal resistance is a way to represent a thermal system as a thermal "circuit." Thermal resistance has units of K/W which indicates that it is a way to calculate how much the chip temperature will rise for each watt that is input into the system. The thermal stack is the layers between the chip surface (which is the heat generation point) and the cooling fluid. Each of these thermal layers has its own thermal resistance, which can be used to calculate the total thermal resistance of the system. The conduction thermal resistance equation is:

$$R_{th\_conduction} = \frac{t}{kA} \tag{B-3}$$

Here, t is the thickness of the material, k is the thermal conductivity (W/mK), and A is the cross-sectional area that the heat is transferring through.

The convection thermal resistance equation is:

$$R_{th\_convection} = \frac{1}{hA} \tag{B-4}$$

The h represents the convection coefficient (W/m^2K) and the A is again the cross-sectional area that the heat is transferred through. For natural convection, h has a value of between 5-15 W/m^2K.

A simple thermal resistance network of a simplified package is shown in Figure 9-1. The left side of the figure shows the package with a device that has been soldered to a substrate with convection cooling on both the top and bottom surfaces. The right side of

the figure shows the equivalent thermal network with the five thermal resistances in series.

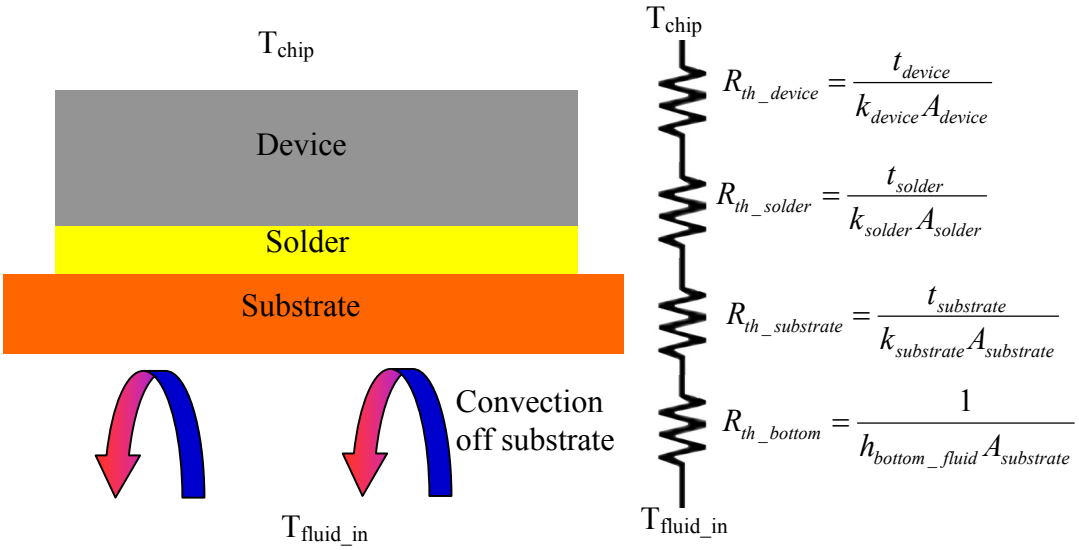


Figure 9-1: Basic thermal resistance network

The total thermal resistance is then calculated by adding up the thermal resistances, just like a series electrical circuit, as is shown in Equation (B-5).

$$R_{th\_total} = R_{th\_device} + R_{th\_solder} + R_{th\_substrate} + R_{th\_bottom} \quad \text{(B-5)}$$

This equation can then be used to calculate temperatures or powers based on Equation (B-6). This is equivalent to V=IR in electronics. In the equation, the ΔT represents the difference in temperature between the device junction on the top surface and the fluid on the bottom surface (T_{chip}-T_{fluid_in}) and the q is the power into the system.

$$\Delta T = R_{th\_total} \times q \quad \text{(B-6)}$$

B.2 Channel Flow equations

The research in this paper is based on channel flow through rectangular channels. This section describes the basic equations for channel flow including the hydraulic diameter, Reynolds number, and pressure drop equations.

B.2.1 Hydraulic diameter

Hydraulic diameter is defined as: $D_h = \frac{4A}{U}$ where A is the cross-sectional area and U is the wetted perimeter of the cross-section. Therefore, for a rectangular channel, the cross sectional area (A) would be the height of the channel (H) times the width (W) and the wetted perimeter would be the sum of the four sides of the channel (2*H+2*W). Therefore, the hydraulic diameter of a rectangular channel is calculated as:

$$D_h = \frac{4HW}{2(H+W)} = \frac{2HW}{H+W} \tag{B-7}$$

B.2.2 Reynolds Number

The Reynolds number is a dimensionless number that indicates the ratio of the inertial to the viscous forces of a fluid during certain flow conditions. It is used to determine if the fluid is in the laminar or turbulent region. The Reynolds number equation is defined as:

$$\mathrm{Re} = \frac{\rho \mathrm{v} D_h}{\mu} = \frac{\mathrm{v} D_h}{\nu} = \frac{Q D_h}{\nu A} \tag{B-8}$$

In this equation, v is the fluid velocity, D_h is the hydraulic diameter, μ is the dynamic viscosity of the fluid, ρ is the density of the fluid, ν is the kinematic viscosity (ν=μ/ρ), Q is the volumetric flow rate, and A is the channel cross sectional area.

The value of the Reynolds number indicates whether the flow is turbulent or laminar. A flow is laminar if Re < 2300, transient for 2300 < Re < 4000, and turbulent if Re > 4000.

B.2.3 Darcy-Weisbach Friction Factor [29]

The Darcy-Friction factor describes the friction losses in pipe flow and can be found by finding it on the Moody Chart. However, for laminar flow, it can be calculated by simply dividing 64 by the Reynolds number:

$$f = \frac{64}{\mathrm{Re}} \tag{B-9}$$

For turbulent flows, the Colebrook equation can be used to calculated the Darcy-Weisbach friction factor:

$$\frac{1}{\sqrt{f}} = -2\log\left(\frac{\varepsilon/D}{3.7} + \frac{2.51}{\mathrm{Re}\sqrt{f}}\right) \tag{B-10}$$

However, it is difficult to solve this equation for the friction factor without an iterative scheme. Therefore, some equations can be used that approximate the friction factor without the need for an iterative process. One such equation is shown in Equation (B-11).

$$f = \frac{1.325}{\left\{\ln\left[\left(\varepsilon/3.7D\right) + \left(5.74/\mathrm{Re}^{0.9}\right)\right]\right\}^2} \tag{B-11}$$

Appendix CBasic Fluent Modeling Procedure

This section is going to describe the modeling procedure that was used to create all the models. The general sequence of steps is to draw the fluidic portion in Solidworks, import the drawing into Gambit, apply boundary conditions to the fluidic portion, draw the solid portion in Gambit, apply boundary conditions to the solid portion, mesh the structure, import into Fluent, apply modeling and boundary conditions in Fluent, run the model and finally process the results. Each of these will be elaborated on.

The first step is to draw the fluidic portion in Solidworks. A representative drawing is shown in Figure C-1. In all cases there is a 2 mm inlet and exit channel. This section represents a complete inlet and outlet manifold channel with all the cross-over microchannels. Each manifold channels is half of its standard width due to symmetry.

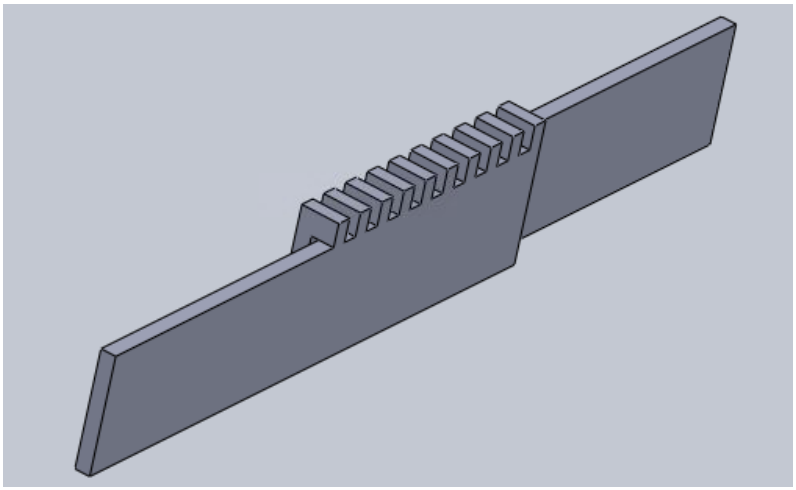


Figure C-1: Representative Solidworks schematic

The Solidworks file is then saved as a .step file and then imported into Gambit. After importing, the image is shown in Figure C-2.

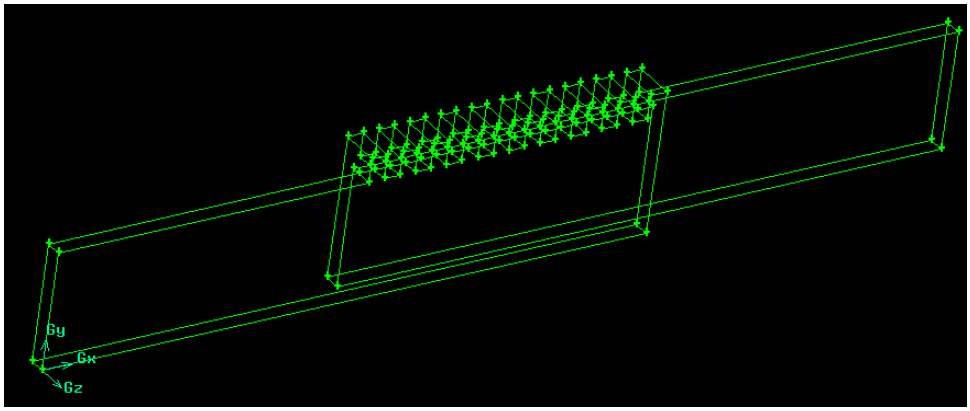


Figure C-2: Fluidic portion after importing .step file into Gambit

The next step is to add the wall boundary conditions to the fluidic geometry. It is easier to add the boundary conditions now before the solid is added so then the fluid and solid walls can be clearly delineated. The wall which acts as the area where the fluid enters is defined as a velocity inlet and the wall where the fluid exits is defined as an outflow. These two boundary types are shown in Figure C-3.

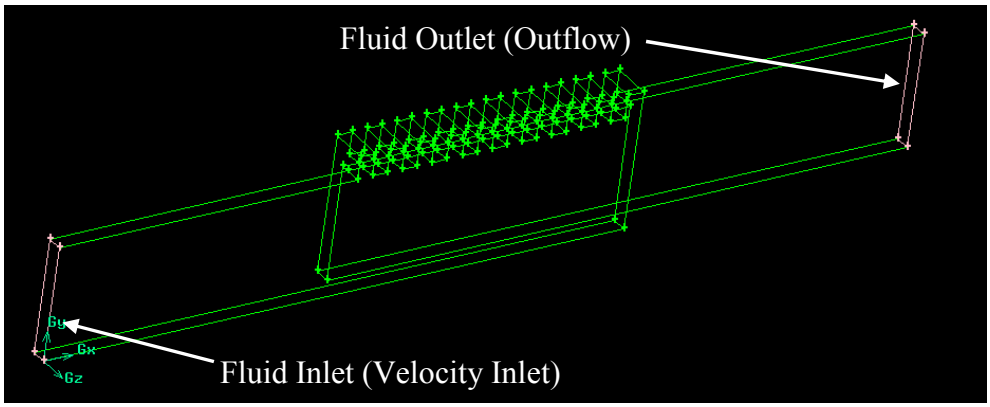


Figure C-3: Schematic showing the location of the boundary types of the velocity inlet and the outflow which are denoted in pink

The exterior of the fluid must be defined as a wall. The two exterior walls of the fluid are shown in Figure C-4. The exterior walls of the solid will be added to this boundary type once the solid has been added to the figure.

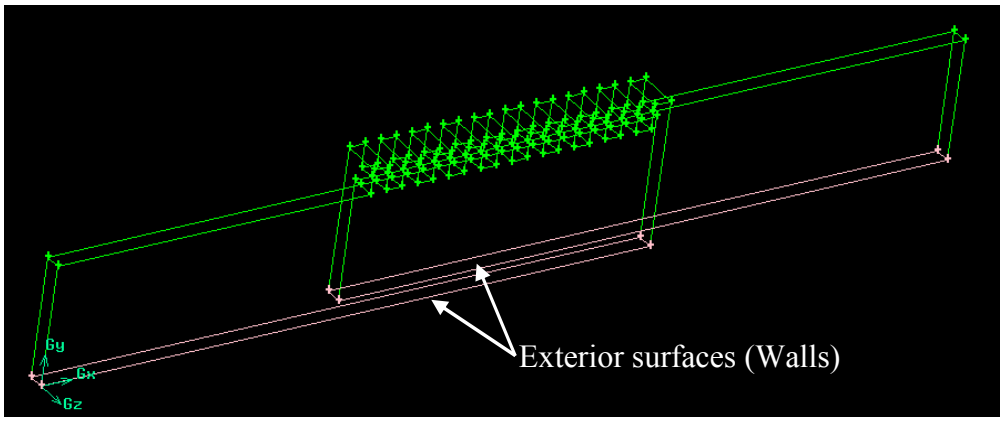


Figure C-4: Image denoting the exterior walls of the fluid

This model is designed to be symmetrical on each of its x-y planes. The model is cut right down the center of both an inlet and an outlet manifold channel with symmetry conditions applied to each of these planes, as is shown in Figure C-5.

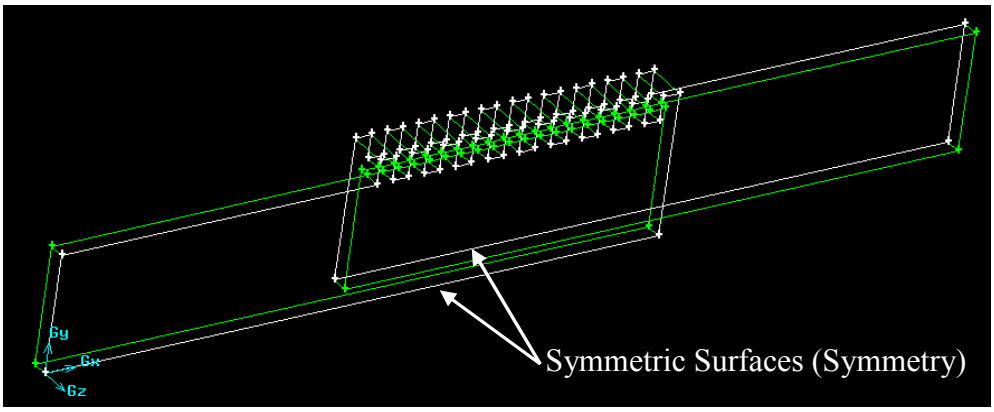


Figure C-5: Image showing the symmetrical boundary conditions of the model

After this, the remainder of the surfaces that have not been defined are the surfaces that contact the solid surfaces and are surfaces of heat transfer. These surfaces are defined as interfaces.

Now that all the walls of the fluid have been defined a boundary type, the solid can be drawn. This is done by drawing a solid square and subtracting the fluid portion from the solid to leave behind the area of solid. Two other rectangular sections are also subtracted to create the chip which is 0.5 mm in all models. The geometry now is shown in Figure C-6.

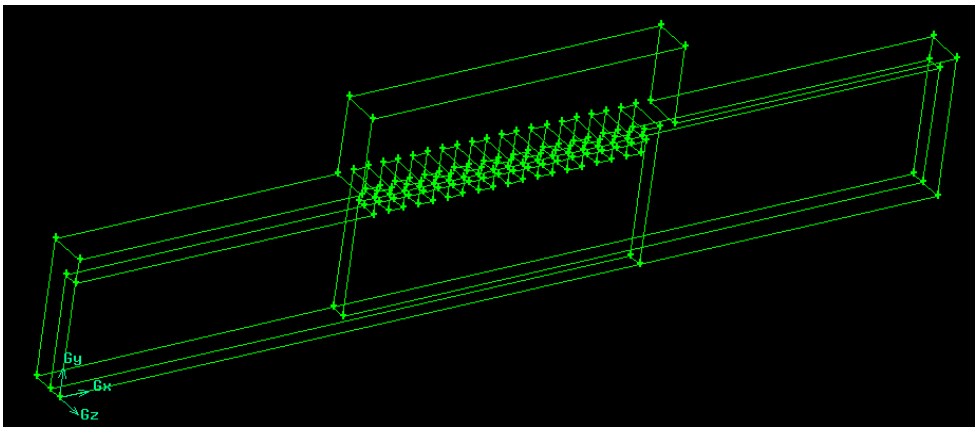


Figure C-6: Gambit figure showing both the solid and the fluid volumes

The boundary types must now be added to the walls of the solid. The exterior walls of the fluid have already been defined so the walls of the solid must be added. All the exterior walls are shown in pink in Figure C-7.

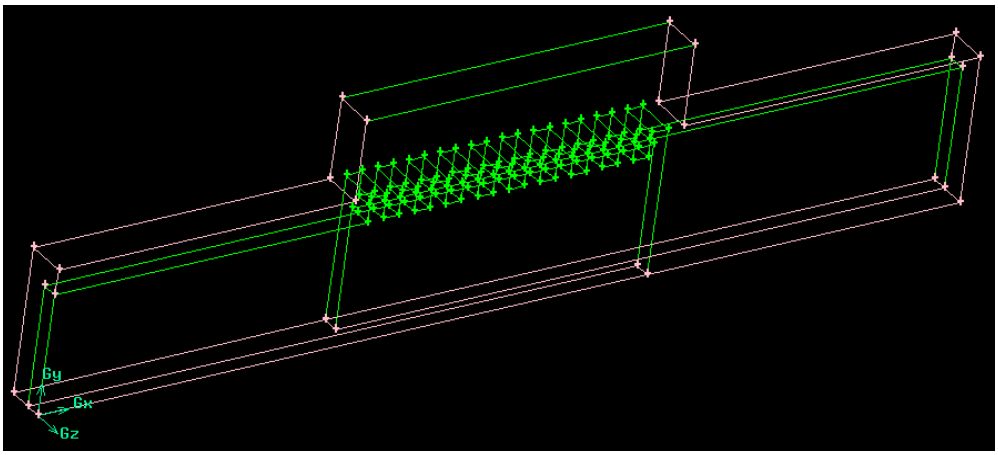


Figure C-7: All exterior walls

As was discussed in Section 3.1.1, the sides along the x-y plane are symmetric boundary conditions. There are two walls on each side, one for the fluid and one for the solid, both of which are defined as a symmetric as is shown in Figure C-8.

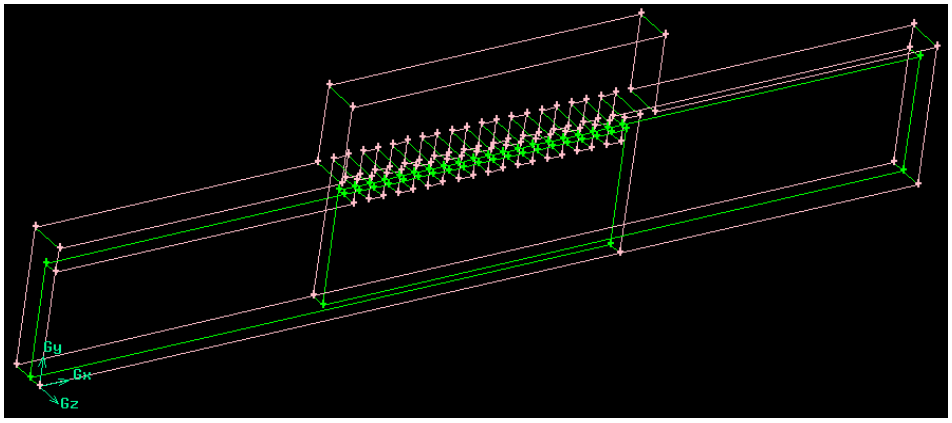


Figure C-8: Symmetry walls

The surface of the chip is defined as a wall but must be defined separately than the rest of the exterior walls because it will have a different boundary condition. It will have a heat flux applied to it so it must be defined separately. The chip top is shown in Figure C-9.

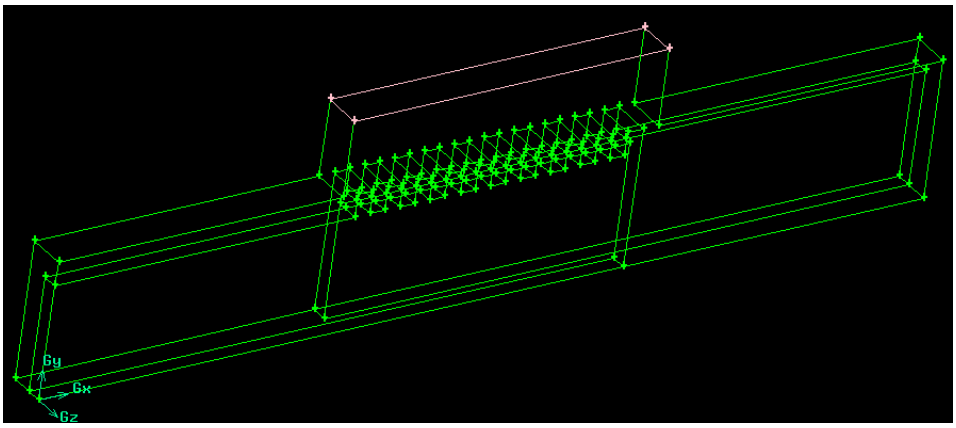
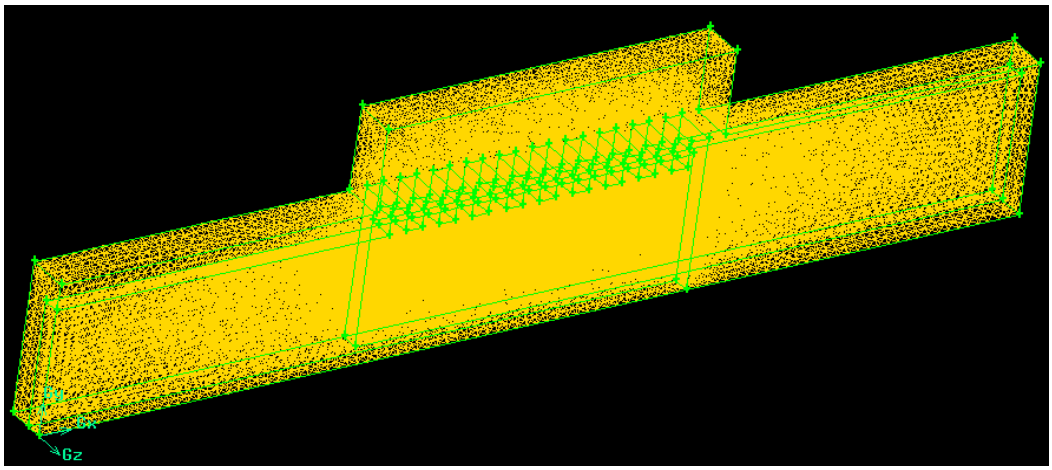


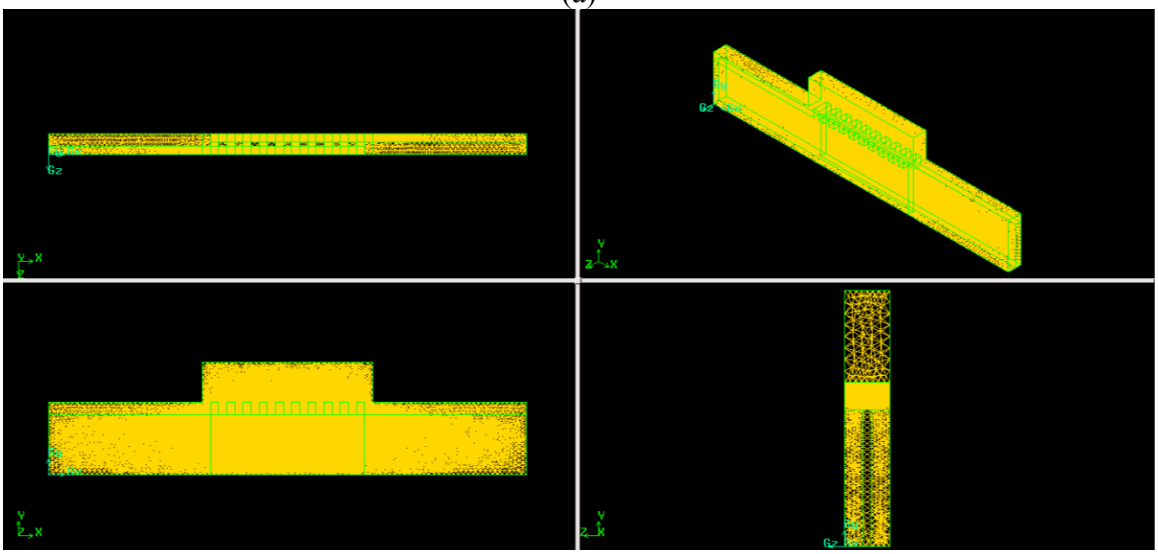
Figure C-9: Chip top

The remainders of the surfaces at this point that have not been defined are the solid interface walls, the surfaces of the solid that contact the fluid surfaces. They are defined as a separate interface boundary to the fluid interface boundary but they are both of the same boundary type.

The continuum types are defined next, where the fluid volume is defined as a fluid and the solid volume is defined as a solid. Everything is then meshed according to the mesh scheme that was discussed in the mesh convergence section. It is critical that the surfaces of the solid and the surfaces of the fluid that are in contact with each other have the same mesh. This is to ensure they transfer heat properly between themselves. The final meshed structure is shown in Figure C-10.



(a)



(b)

Figure C-10: Final meshed structure (a) schematic of a standard mesh (b) view of final meshed structure from different perspectives

The meshed structure is then exported as a mesh file (.msh) and read into Fluent. Then in Fluent the first thing that must be done is to define the grid interfaces and couple the solid and fluid interfaces. This allows the heat transfer to occur between the two surfaces. Next to do a grid check to make sure everything was properly drawn. The next step is to scale the model to microns since Fluent defaults to meters and the model was drawn in microns.

The models must be defined. All the defaults were used except for the Gradient option which was changed to Green-Gauss Node based as is shown in Figure C-11. The pressure based solver is a segregated solver and is used in most situations except for very high pressures and/or velocities, neither of which occurs in these simulations. The model is a 3D model and will be run in steady state with an absolute velocity scale.

The Green-Gauss Node based model was chosen because it is known to be more accurate for tetrahedral meshing, as was done in these models. It calculated the values by the weighted average of the surrounding nodes and so can preserve the second order accuracy. The energy equation was turned on to allow heat transfer.

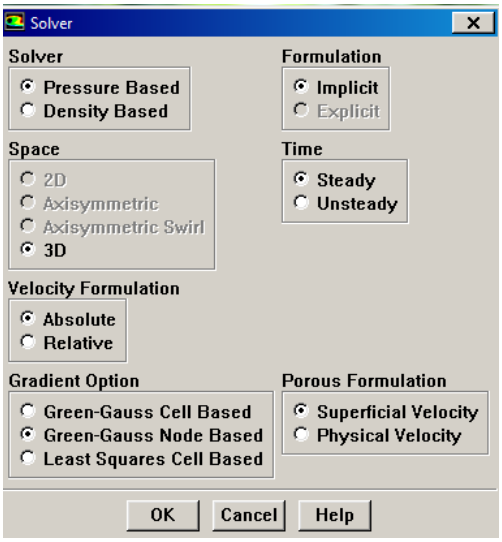
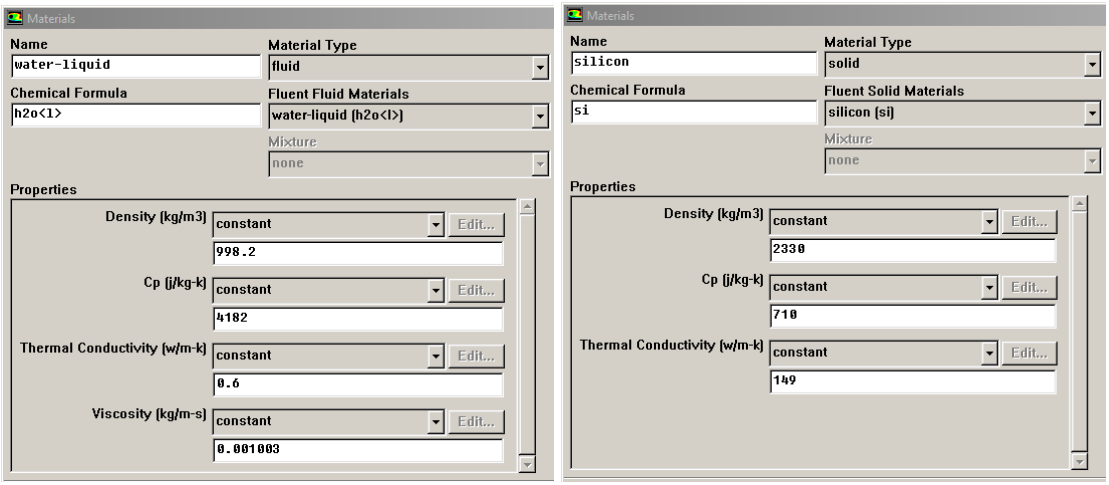


Figure C-11: Solver Window in Fluent

The two materials used in this study are water as the fluid and silicon as the solid. Water is already defined in the Fluent library but silicon had to be defined. The properties for each material are shown in Figure C-12.



(a) (b)

Figure C-12: Screenshots of the Fluent properties for (a) water and (b) silicon

The next step is to define the operating conditions. All the conditions were left at their default values in Fluent except gravity which was added in the y-direction as is shown in Figure C-13.

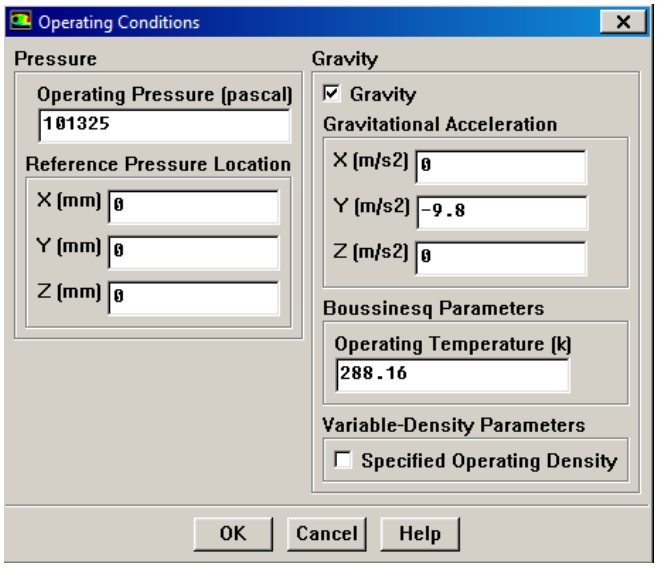


Figure C-13: Fluent window to define gravity condition

The next thing that must be done is to define the boundary conditions on the different zones that were defined in Gambit. The first zone to have its boundary conditions applied is the top of the chip. This was previously defined in Gambit as its own boundary so then a heat flux could be applied to it. As is shown in Figure C-14, the thermal condition is checked at heat flux and a heat flux if 4000000 W/m^2 (400 W/cm^2) is applied to this surface. The material is also defined at silicon at this surface.

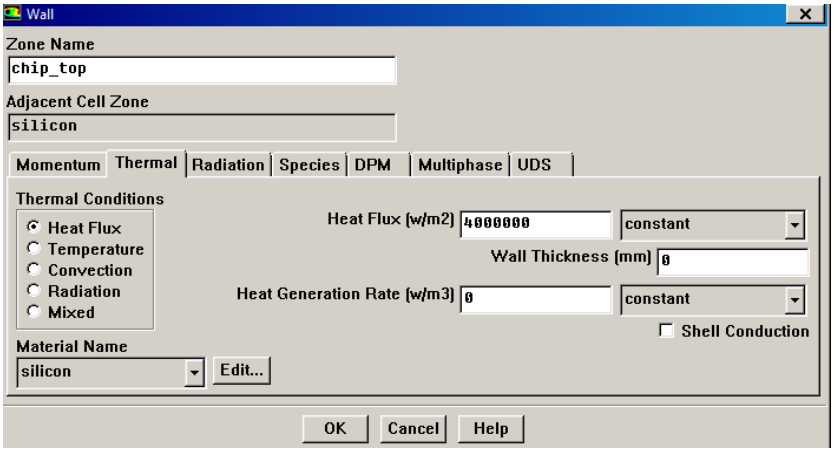


Figure C-14: Define the surface conditions of the chip

Other boundary conditions must also be applied to other surfaces. For the fluid volume, it must be set to water and the solid volume must be set to silicon. The last boundary that must be defined is the velocity inlet which is defined as a certain velocity magnitude in m/s.

One of the final tasks is to define the order of the solution in the solution controls window, which is shown in Figure C-15. The pressure-velocity coupling was defined as SIMPLEC which stands for SIMPLE-Consistent. This allows laminar solutions to converge faster by allowing higher under-relaxation factors. For the discretization, the pressure is set to PRESTO! because it gives more accurate solutions for problems over

the standard solver. Second order for the pressure is not necessary because it is recommended only for solutions with compressible flows. Both the momentum and energy are set to Second Order Upwind to achieve second-order accuracy. Upwind refers to the fact that the cell value is calculated based on the cell upwind or upstream of the cell.

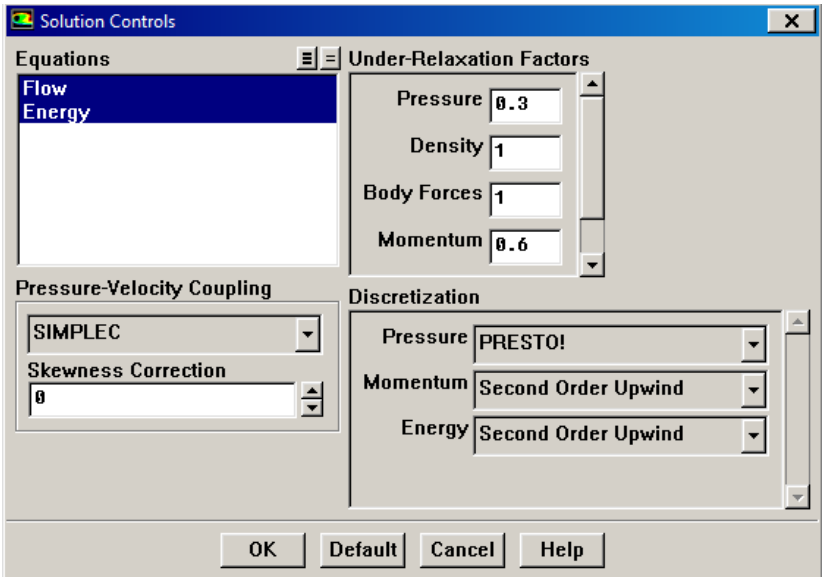


Figure C-15: Screenshot of the Solution Controls window in Fluent

The next step is to set the initialization conditions. In order to speed up convergence, the inlet it initialized to the previously defined inlet velocity condition. Next, the residual monitors are defined, as is shown in Figure C-16. The convergence is set to 1E-4 in almost all conditions, which is sufficient, as will be shown in Section Appendix D.

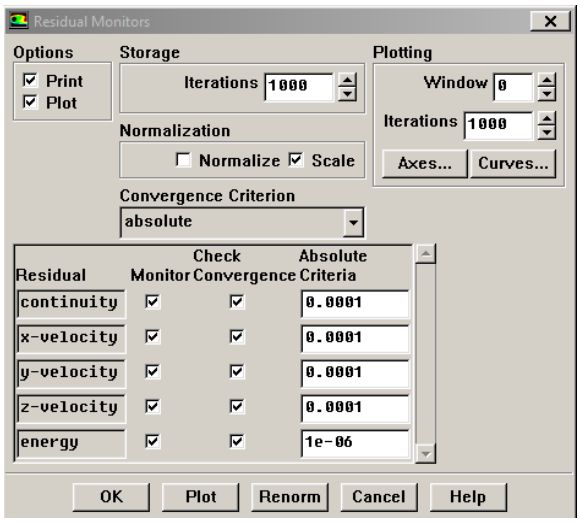


Figure C-16: Screenshot of the convergence criteria screen in Fluent

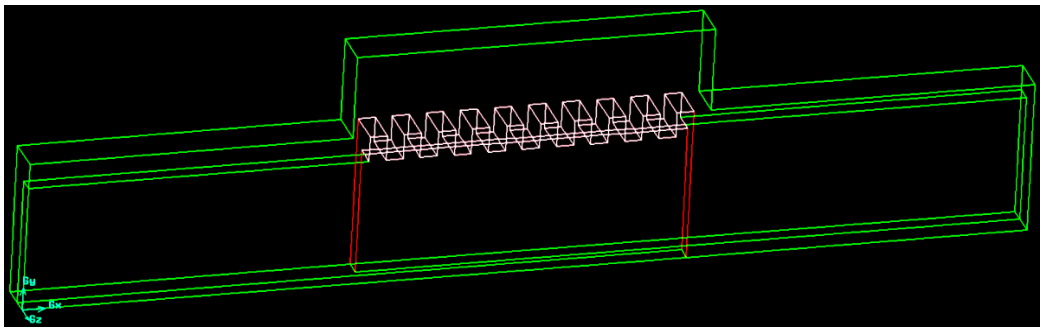
The last two steps are to do the case check to ensure everything is properly entered into the system and there are no errors. Then set the number of iterations and press iterate to run the model. The model is then run until it converges, then data is retrieved from the solution.

Appendix DFluent Modeling Mesh Convergence

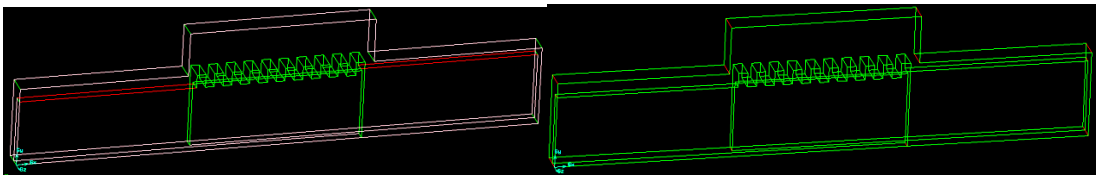
In order to show that the mesh that was created is satisfactory, the mesh must be proven to have converged and be independent. Mesh convergence is proven by showing that when the number of elements in a mesh is increased, the solution converges to a single value. Mesh convergence was achieved by increasing the mesh density until the data becomes mesh independent. Mesh independence is creating a mesh such that changing the mesh slightly has little effect on the solution. This shows that the solution is independent of the mesh and this is critical because a sufficiently fine mesh should converge to the desired solution. This will allow the mesh to be sufficiently dense such that an accurate solution can be obtained but not too dense such that the computing time is reduced.

Since some parts of the model require a finer mesh than others, there were defined areas of mesh refinement as shown in Figure D-1 and listed here:

- Microchannels
- Vertical walls extending from microchannels
- Horizontal walls extending from microchannels
- Long Exterior walls
- Short exterior walls



(a)



(b) (c)

Figure D-1: Figures showing the various portions of the model that had various mesh densities and gradients (a) pink is the microchannels and red is the vertical walls extending from the microchannels (b) pink is the long exterior walls and red is the horizontal walls extending from microchannels (c) red lines indicate the small exterior walls

Each of these five areas had separate meshing criteria. The meshing of the microchannels, shown as pink in Figure D-1a, was the finest since this is the critical area of heat transfer and fluid flow. The walls extending from the microchannels to the exterior were finely meshed close to the microchannels, then progressively coarser as they approached the exterior. The horizontal and vertical walls are shown as red in Figure D-1a and b, respectively. The coarsest mesh is around the exterior and these walls are shown in pink in Figure D-1b. Along the exterior are short walls in the z-direction which require a slightly finer mesh than the other exterior channels since they are so short. These walls are shown in Figure D-1c in red. In order to determine the mesh spacing,

local mesh refinement was done. Local mesh refinement was most critical in the microchannel region since this is the location of the majority of heat transfer.

D.1 Defining Convergence Criteria

In order to determine when a model has converged, a convergence plot is used which plots the residuals as a function of the number of iterations. A typical convergence plot is shown in Figure D-2 for a model with M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, Q = 3 ccm, q" = 400 W/cm^2, N_{ch} = 19. A solution is determined to have converged when the residuals have reached a certain value.

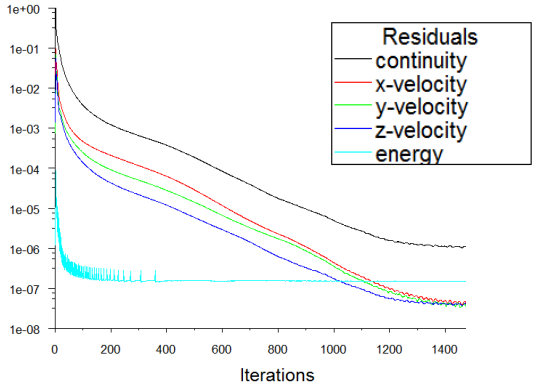


Figure D-2: Sample scaled residual convergence plots for M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, Q = 3ccm, q" = 400 W/cm^2, N_{ch} =19

As was discussed in Section 1.10, the two primary outputs of this study are the average chip temperature and the system pressure drop. In order to determine the value of sufficient convergence, multiple models were run to various convergence criteria and their average chip temperature and pressure drop were plotted as a function of the convergence criteria. This plot is shown in Figure D-3 for three different conditions:

- Geometry 1 (shown as blue): M_h = 545.45 µm, M_w = 550 µm, M_f = 150 µm, m_h = 100 µm, m_w = 100 µm, m_f = 150 µm, N_{ch} = 10, Q = 11.25 mL/min.
- Geometry 2 (shown as red): M_h = 356.25 µm, M_w = 200 µm, M_f = 50 µm, m_h = 50 µm, m_w = 50 µm, m_f = 150 µm, N_{ch} = 19, Q = 5.625 mL/min.
- Geometry 3 (shown as green): M_h = 750 µm, M_w = 200 µm, M_f = 50 µm, m_h = 100 µm, m_w = 100 µm, m_f = 150 µm, N_{ch} = 10, Q = 5.625 mL/min.

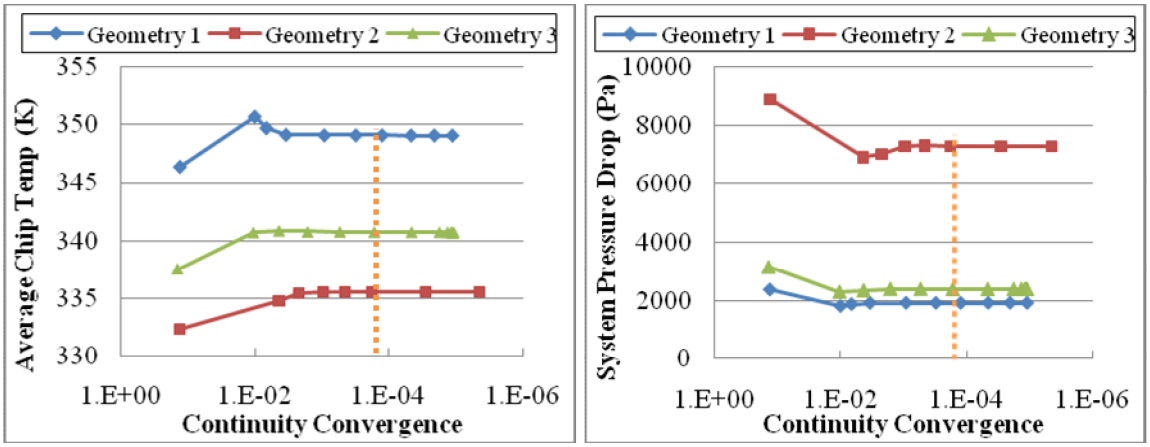


Figure D-3: Convergence plots for various geometries showing that 1E-4 (shown with an orange dashed line) is more than sufficient to get a consistent result for both (a) average chip temperature and (b) system pressure drop

The charts show that the solutions for both the average chip temperature and the system pressure drop converge very early on. By the time they reach 1E-3 there is very little difference in the solution. The difference is less than 0.05 °C in chip temperature and less than 1 Pa in pressure drop. Therefore, converging the solution to 1E-4 is more than sufficient for the solution to have converged to a solution both thermally and fluidically.

D.2 Proving Mesh Independence

The mesh has been shown to converge at 1E-4, but it must also be proven that the mesh is independent. That means that the mesh has reached density such that the solution is independent (a slight variation in mesh density has little effect on the final solution). For a given geometry, each of the above mesh zones are varied and then run to 1E-4 convergence. The system pressure drop and average chip temperature are then extracted from the solution and plotted as a function of mesh density. For the MMC structure with dimensions M_w = 200 µm, M_f = 50 µm, M_h = 750 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, and N_{ch} = 10, the independence plot for the microchannels are shown in Figure D-4. The red data points refer to the pressure drop and the blue data points refer to the average chip temperature. A similar plot was made for all the other five mesh zones which are not shown here.

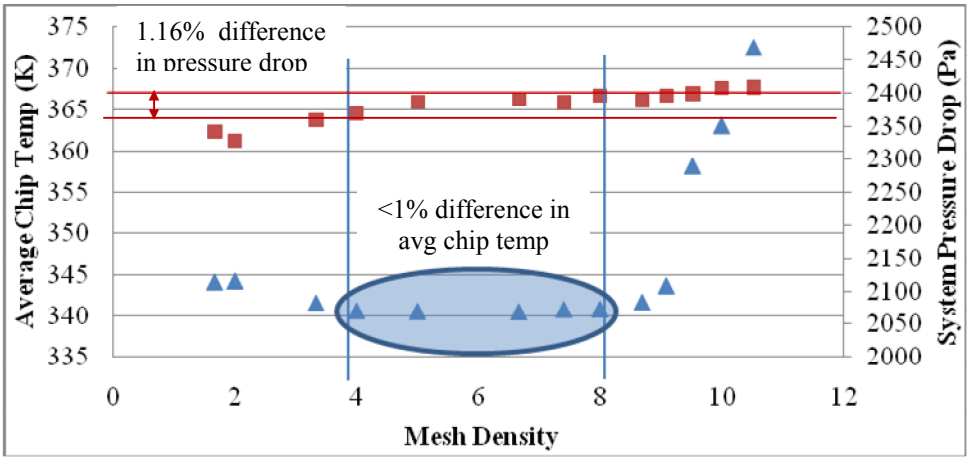


Figure D-4: Mesh independence plot for m_w = 100 µm and m_f = 100 µm

The x-axis of the plot is the mesh density which is the number of divisions in a 100 µm length. This equates to the larger numbers indicating a higher mesh density. The

figure shows that the pressure drop is converged after a mesh density of about five. It can be seen in the figure that after about a meshing density of 9, the temperature diverges quite substantially. After looking into this, it is shown that this occurs due to a loss of transfer of heat between the solid and liquid boundary layer, as is shown in Figure D-5. Figure D-5 shows how the heat transfer stops occurring for increased mesh densities. Figure D-5a shows a very fine mesh where it is clear that there is no heat transferring between the solid and fluid causing the top of the chip to be substantially hotter. Figure D-5b and c show some heat transferring to the fluid in select areas in the channel. It is not until Figure D-5d that the heat is being completely transferred to the fluid.

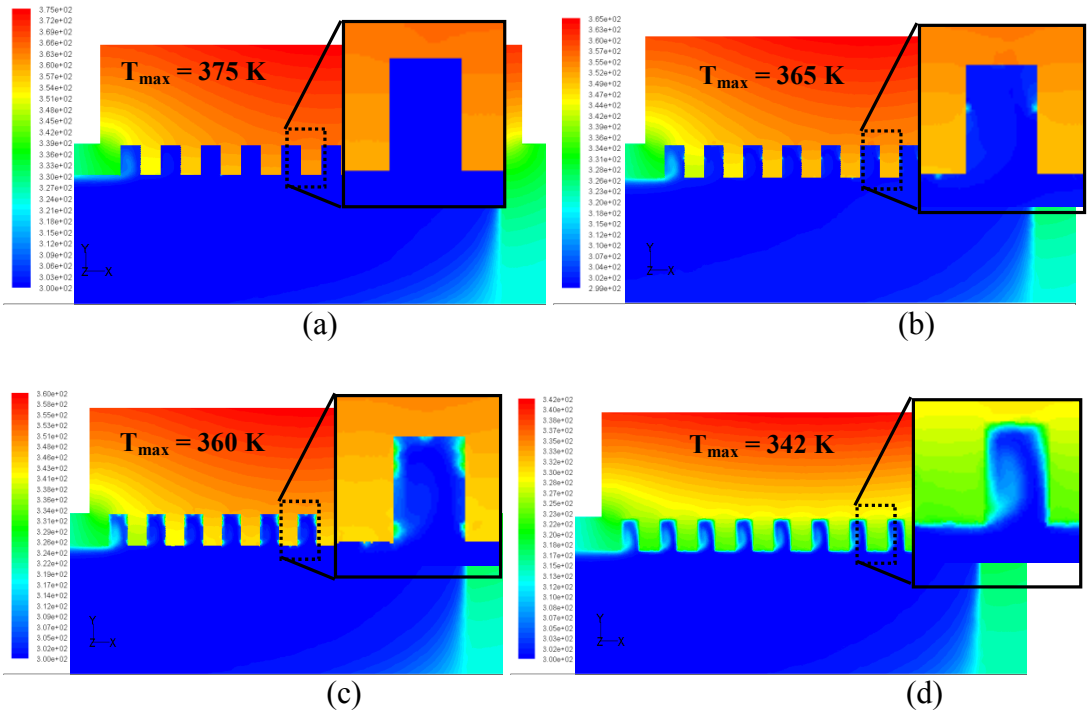


Figure D-5: Cross section indicating for higher mesh densities, a decreased heat transfer (a) 10.5 (b) 10 (c) 9.5 (d) 8

Comparing Figure D-3 and Figure D-5, it can be seen that the temperature above a density of 8 increases substantially and the reason is that the heat transfer is not occurring. This is most likely occurring because when a grid gets too fine, numerical round-off errors could occur causing the mesh to give inaccurate answers. Therefore, looking atFigure D-3, both the temperature and pressure are relatively constant between densities of about 4 and 8. Therefore, for this mesh, a mesh density of around 8 which equates to a mesh spacing of 0.0125 in Gambit was chosen.

The microchannels that were just shown had dimensions of m_w = 100 µm and m_f = 100 µm, which is the largest channels that will be modeled in this study. But there are finer channels that must be meshed as well. So this leads to the question of how this convergence plot relates to other dimensions. Therefore the same procedure was performed for the smallest channels that will be modeled, m_w = 50 µm and m_f = 50 µm. The manifold dimensions remained the same. The plot is shown in Figure D-6. This plot also shows the trend of the average chip temperature rising after a mesh density of around 8. The figure also indicates that the mesh is converged at a mesh density of around 8.

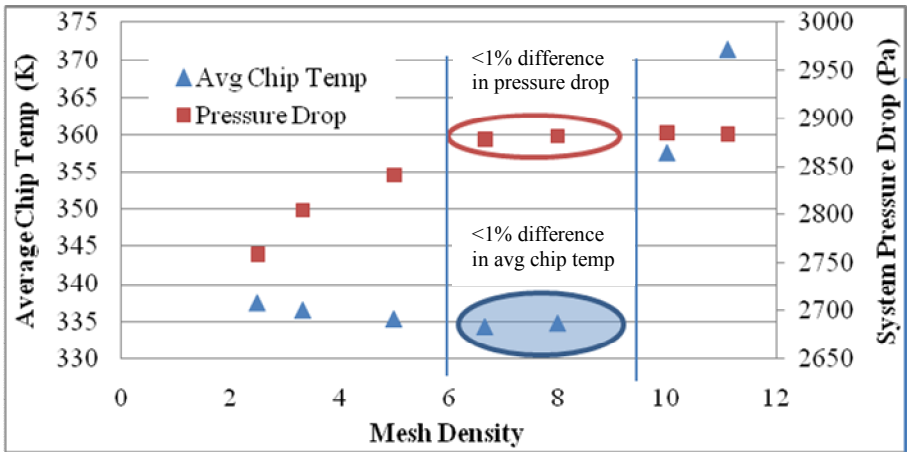


Figure D-6: Pressure and Average chip temperature convergence plot for m_w = 50 µm, m_f = 50 µm

Both of the microchannel geometries ($m_w = m_f = 100$ µm and $m_w = m_f = 50$ µm) are plotted against each other to see how their trends compare, as is shown in Figure D-7.

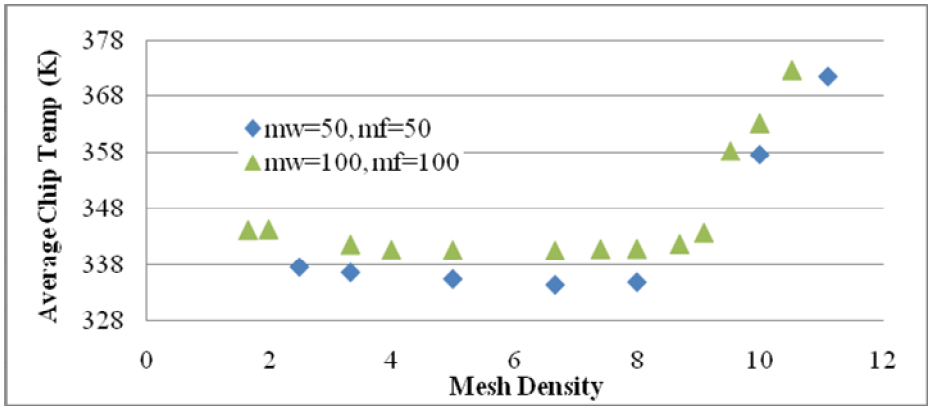


Figure D-7: Convergence plot comparing two different geometries ($m_w = 50$ µm, $m_f = 50$ µm and $m_w = 100$ µm, $m_f = 100$ µm) indicating they have similar convergence trends

The trends in Figure D-7 are very similar for each of the two geometries and therefore, a mesh density of 8 (or a Gambit spacing of 0.0125) would give sufficient convergence for both microchannel geometries. There are four microchannel geometries that are modeled during this study:

- $m_w = 100$ µm, $m_f = 100$ µm
- $m_w = 100$ µm, $m_f = 50$ µm
- $m_w = 50$ µm, $m_f = 100$ µm
- $m_w = 50$ µm, $m_f = 50$ µm

Since it has been shown that a density of 8 is sufficient for both the largest and the smallest channel dimensions, then it is going to be assumed that the density is also sufficient for the middle dimensions both of which contain dimensions of the geometries

that were proven to be mesh independent. Therefore, all geometries will have microchannel spacing of 0.0125 (mesh density = 8).

A similar procedure was performed on the other areas of different mesh densities including the vertical walls extending from the microchannels, the horizontal walls extending from microchannels, the long exterior walls and the short exterior walls. For the vertical and horizontal walls extending from the microchannels, the ratio also had to be accounted for allowing the mesh density close to the channels to be similar to the microchannels and the density around the exterior to be close to the density of the exterior. The exterior meshing was much coarser than the density around the microchannels.

D.3 Laminar vs. Turbulent

The Reynolds number calculations indicate that all of the models fall in the laminar regime but it is hard to calculate a true Reynolds number with a complicated geometry like the manifold microchannel structure. Therefore, models were run using both the laminar and the turbulent solvers in Fluent to see the difference in the solution. The models that were run were all for the geometry with dimensions M_w = 200 μm, M_f = 50 μm, M_h = 750 μm, m_w = 100 μm, m_f = 100 μm, m_h = 150 μm, and N_{ch} = 10. The models were run for various mesh densities both as laminar and turbulent, as is shown in Table D-1. In these cases, the results were plotted in terms of maximum velocity and system pressure drop.

Table D-1: The various meshes used to prove mesh convergence for 100 micron microchannels

	Microchannels		Manifold Walls		Outside Manifold				
Number of Elements	Element Size	Ratio	Element Size	Ratio	Element Size	Ratio		v_{max} (m/s)	Δp (Pa)
9870	0.05	1	0.05	1	0.05	1	laminar	2.391	4356.2
							turbulent	2.358	4274.9
29780	0.03	1	0.06	1.02	0.1	1	laminar	3.018	2673.5
							turbulent	2.763	5208.5
74362	0.02	1	0.04	1.02	0.08	1	laminar	3.091	5906.2
							turbulent	2.889	5846.1
111093	0.02	1	0.03	1.02	0.06	1	laminar	3.105	5939.3
							turbulent	2.956	5820.8
240549	0.01	1	0.03	1.02	0.06	1	laminar	3.162	6131.6
							turbulent	3.083	6258.0
294268	0.015	1	0.02	1.02	0.04	1	laminar	3.082	6147.5
							turbulent	2.993	6080.2

Figure D-8 shows the plots of the pressure drop and the maximum velocity as a function of the number of elements in the mesh. The plot indicates that once the geometry has reached a converged solution, that the difference between the laminar and turbulent flow models is 3.5% for the velocity and 3.7% for the pressure drop. The models also show similar flow performance when looking at the flow profiles. Therefore, in conclusions, laminar mesh models are sufficient to model the flow conditions and the more complicated, computer and time intensive turbulent meshing is not necessary.

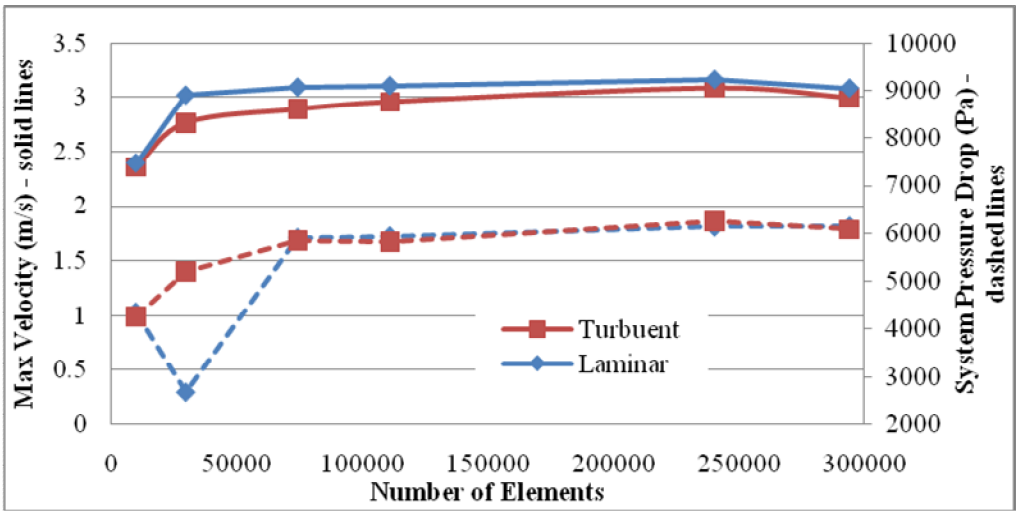


Figure D-8: Mesh convergence plot for the maximum velocity of 100 micron channels

D.4 Example of a Converged Mesh

An example of a converged mesh is shown in Figure D-9 for a manifold structure with dimensions M_h = 750 µm, M_w = 200 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10. The mesh clearly shows that the mesh is much finer in the center of the mesh where the microchannels are versus the broader mesh around the inlet, outlets and chip.

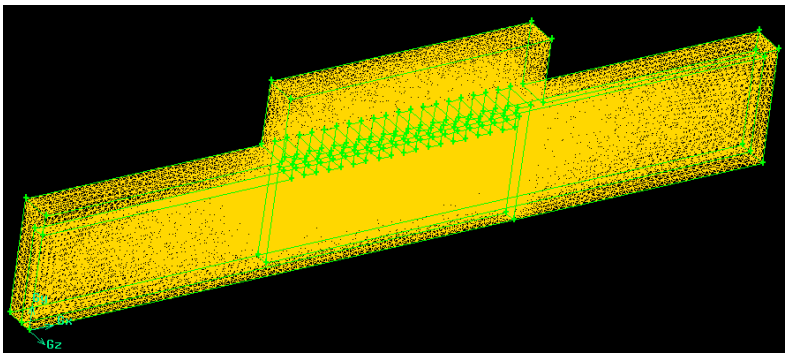


Figure D-9: Image depicting the converged mesh for a MMC structure with dimensions M_h = 750 µm, M_w = 200 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10

The various meshing parameters for the mesh shown in Figure D-9 are listed in Table D-2. The microchannels have the smallest spacing and the long exterior walls have the largest spacing.

Table D-2: A sample meshing density and spacing for M_h = 750 µm, M_w = 200 µm, M_f = 50 µm, m_w = 100 µm, m_f = 100 µm, m_h = 150 µm, N_{ch} = 10

microchannels		**Vertical walls from microchannels**		**Horizontal walls from microchannels**		**long exterior**		**short exterior**	
spacing	ratio	spacing	ratio	spacing	ratio	spacing	ratio	spacing	ratio
0.0125	1	0.0125	1	0.03	1.02	0.06	1	0.03	1

This particular mesh consisted of 331,634 fluid cells and 303,522 solid cells, for a total of 635,156 cells. The models that were run had as few as 206,192 elements and as much as 1,444,191 elements. The number of elements was primarily dependent on the manifold height and the size and number of microchannels.

Appendix EMEMS Processes Used in the Report

This appendix gives a brief description of the basic MEMS processes that have been used throughout this report. All of the processes that are listed are standard and well understood MEMS fabrication processes that are available in most cleanrooms.

E.1 Oxide Growth

Silicon dioxide (SiO_2) is a critical feature in MEMS fabrication. In this study, it is going to be used as both a masking layer and for electrical isolation. It has a very high electrical resistance but a very low thermal conductivity and can be highly stressed. The two types of oxides that are used in this paper are thermal oxides and PECVD oxides, discussed further below.

E.1.1 Thermal Oxide

A dry thermal oxide is grown when a wafer is placed into a pure oxygen chamber at very high temperatures between 800-1200 ºC. The oxygen reacts with the silicon to create silicon dioxide, as shown in Equation (E-1). The reaction slows down parabolically over time; therefore, it takes a very long time to obtain thick oxide layers. The oxide layers formed this way are often very good with few pinholes or contaminants.

$$Si + O_2 \rightarrow SiO_2 \tag{E-1}$$

E.1.2 PECVD Oxide

PECVD (plasma enhanced chemical vapor deposition) is a method to deposit oxide at a much lower temperature (300-350 ºC) and at constant rates. The machine used in this study is the Plasma-Therm 790. The oxide is formed by a chemical reaction

between silane and oxygen excited by a plasma that enhances the formation of the silicon dioxide and its deposition onto the wafer surface.

E.1.3 Rapid Thermal Anneal (RTA)

Oftentimes when the oxide is formed, it is heavily stressed. A rapid thermal anneal (RTA) can be used to relieve some of the stress and densify the oxide. The wafer is quickly brought up to 700 ºC and held there for 60 seconds before being cooled back down to room temperature.

E.2 Oxide Removal

Selective or complete removal of oxide is necessary when an oxide is used as a masking material. The two methods of oxide removal used in this report include wet chemical etching with HF and dry etching through reactive ion etching (RIE).

E.2.1 Chemical Oxide Etching with HF

Oxides can be wet chemically etched using hydrofluoric (HF) acid. The chemical reaction is shown in Equation (E-2). The wafer is submersed in diluted HF acid to remove the oxide. This type of etch creates an isotropic etch profile and can be used with a photoresist mask.

$$SiO_2 + 4HF \rightarrow SiF_4 + 2H_2O \qquad \text{(E-2)}$$

E.2.2 Reactive Ion Etching (RIE)

Reactive Ion Etching (RIE) uses chemically reactive plasma to remove the oxide from the wafer. The gases (CF_4, He, and CHF_3) are pumped into the chamber and then broken into free Fluorine radicals which react with the SiO_2. The etching is performed at

2.8 Torr in the LAM 590. RIE etching creates an anisotropic etch profile of the remaining oxide and can be used with a photoresist mask.

E.3 Photolithography

Photolithography is the backbone of MEMS processing, as it defines the product features. Three basic steps of lithography are shown in Figure E-1 (spinning, exposing, and developing).

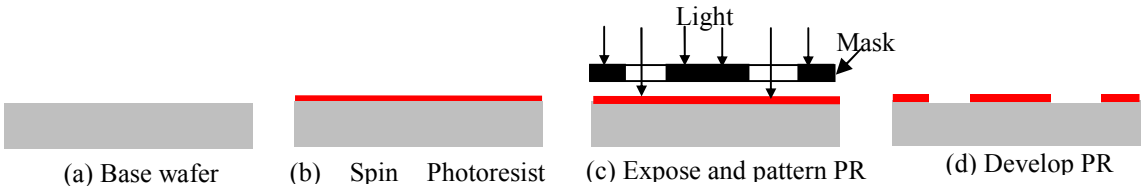


Figure E-1: Basic Photolithography Procedure

E.3.1 Mask Writing

A mask is used for selectively exposing the photoresist during the photolithography step. A mask has both dark and light areas which allow the UV light to pass only through the clear areas. Glass masks that are patterned with chrome metal are used for all the masks in this paper. The mask starts as a glass sheet that is metalized with chrome then coated in photoresist. The desired design is typically drawn in a CAD program. The program used in this paper is LASI, which is a program designed for chip layouts, so it works well for mask writing. The design is then converted into a format used by the mask writer (a Mann PG3600), is downloaded into the mask writer, and is written by selectively developing the photoresist. Subsequent processing of the generated mask is needed to remove the unwanted chrome and masking photoresist.

E.3.2 Spinning Photoresist (PR)

The first step of the photolithography process is to spin the photoresist (PR), shown in Figure E-1b. The wafer is placed onto a spinning chuck and is held in place by a vacuum. Hexamethyldisilazane (HMDS) is typically spun before the photoresist to aid in adhesion. A standard spin recipe is as follows:

1. Bake wafer at 110ºC for 10 minutes to dry it.
2. Use a pipette to drip HMDS onto the wafer.
3. Spin HMDS.
4. Pour PR onto the wafer, allowing it to coat most of the wafer.
5. Spin PR.
6. Soft bake PR on hot plate at 110ºC.

The PR spin speeds vary depending on the desired thickness: the faster the spin, the thinner the photoresist will be. Photoresists also have different initial viscosities, which can also change final thicknesses at any fixed spin rate.

E.3.3 Exposing Photoresist

Once the PR has been spun to the desired thickness, it is then exposed to UV light through a patterning mask, as shown in Figure E-1c. A photoresist can either be positive or negative. A positive resist means that the photoresist that is exposed to the light becomes soluble and washes away. A negative resist acts oppositely in that the photoresist that is exposed to light cross-links and becomes insoluble. All photoresists used in this paper were positive.

E.3.4 Developing Photoresist

Once the pattern has been exposed onto the wafer, the wafer is then developed by placing it into a liquid developing solution. The soluble areas of the positive photoresist wash away and the insoluble portions remain. This is shown in Figure E-1d.

E.3.5 Removing Photoresist

After processing, it is often necessary to remove the photoresist which is done in a number of ways: acetone, photoresist stripper (PRS), or the downstream asher. Both acetone and PRS are chemical strippers of the photoresist and they remove the PR by simply immersing the wafer in the liquid. The downstream asher heats the photoresist up to very high temperatures, in essence burning it off the wafer. It leaves a very clean surface but the wafer must be able to handle the high temperatures. Another option is the Metroline which can be used as an asher but can also be used to de-scum the wafer by removing any re-deposited photoresist after developing.

E.4 Evaporation: Metal Deposition

There are many ways to deposit metals but the technique used in this study is evaporation. The typical composition of the metal layers is: 50 nm Cr, 50 nm Au, 1 μm AuSn, 50 nm Au. These layers serve as bonding layers for the gold tin (AuSn) eutectic bonds, and also to provide electrical connections to the SiC device after bonding. The chrome serves as an adhesion layer between the metal layers and the Silicon or SiO_2 substrate, while the gold layers act as diffusion and oxidation barriers for the AuSn.

E.5 Bonding

In order to bond multiple wafers together, two methods were used in this report: anodic bonding and eutectic AuSn bonding.

E.5.1 Anodic

Anodic bonding is used to bond a silicon wafer to a Pyrex wafer. The two wafers are aligned to each other then put in a chamber under vacuum to remove any air between the wafers. The bond is then made at 400 ºC with a high DC potential placed across the two wafers, about 1 kV. The sodium ions from the Pyrex wafer move away from the bonding surface causing the Pyrex wafer to react with the silicon wafer, forming a solid chemical bond.

E.5.2 Eutectic AuSn Bonding

In order to bond silicon to silicon and devices to silicon, a gold-tin eutectic bond was used. This bond is performed by depositing metals onto both sides, then bonding them in a wafer bonder at an elevated temperature and inert environment. The wafers are stacked and aligned on the bonding platform ensuring even distribution of the pressure. Additional pieces could be added to further distribute the pressure and minimize the potential for cracking. A dummy silicon wafer is placed on top of the entire stack to protect the bonding chamber from contamination. The bond is a 10 minute eutectic bond process consisting of 1 kTorr applied tool pressure and heating to 285˚C in a 1.33 kTorr H_2N_2 atmosphere.

E.6 Deep Reactive Ion Etching (DRIE)

Deep Reactive Ion Etching (DRIE) is the process that makes this study feasible and one of the reasons MEMS is successful. DRIE (also known as the Bosch Process) is a process used to etch vertical walls into silicon wafers with aspect ratios up to 20:1. An example of the vertical features that can be created by the Bosch Process is shown in Figure E-2a. The Bosch process alternates between an isotropic plasma etch and a passivation layer. The plasma etch etches the wafer further while the passivation layer puts a coating on the sidewalls that prevents subsequent etching of the walls. This creates what is known as a scalloping effect, as shown in Figure E-2b.

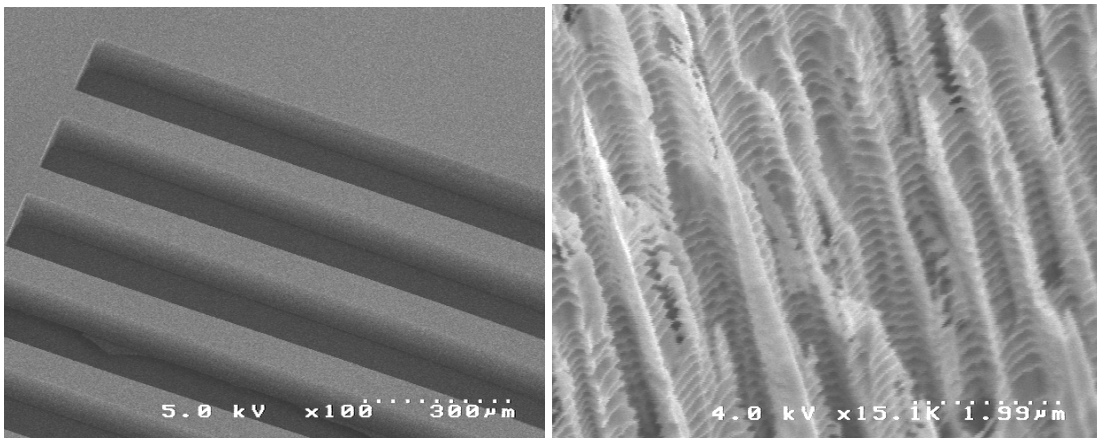


Figure E-2: DRIE images (a) example of features created by DRIE etching (b) SEM of the DRIE scalloping effects

E.7 Dicing using the Diamond Saw

The wafers are diced apart using a wafer saw with a diamond blade that is typically 250 µm wide. The wafer is attached to a holder with an adhesive Mylar film which is removed after dicing has been completed. The wafer is aligned in the direction

of the desired dice line, then the number of dicing lines and spacing between the lines is entered into the machine. The wafer saw then cuts the lines and the process is repeated in the other direction if necessary.

E.8 Simplified Process Sequence

The basic outline of the fabrication steps that will be presented in this paper is shown in Figure E-3. The first step (a) is to deposit a PECVD oxide layer on both sides and then do a rapid thermal anneal (RTA) to reduce the stress in the oxide. After the oxide has been deposited, photoresist (PR) is patterned. The oxide is then etched away using RIE (step b) with the PR acting as a masking layer. At this point, both the oxide and the PR will act as masks for the subsequent DRIE etch.

Next, the wafer is etched using DRIE (step c) then the PR is stripped from the wafer. PR is then reapplied to one side and repatterned and the oxide is RIE etched again to create the masking layer for the subsequent DRIE step (step d). A second DRIE is performed until it reaches the original etch (step e). PR is then stripped and the metal bonding layers are evaporated on both sides of the wafer (step f). Finally, the wafer is bonded using the wafer bonder (step g) and the devices are then separated using a diamond bladed dicing saw.

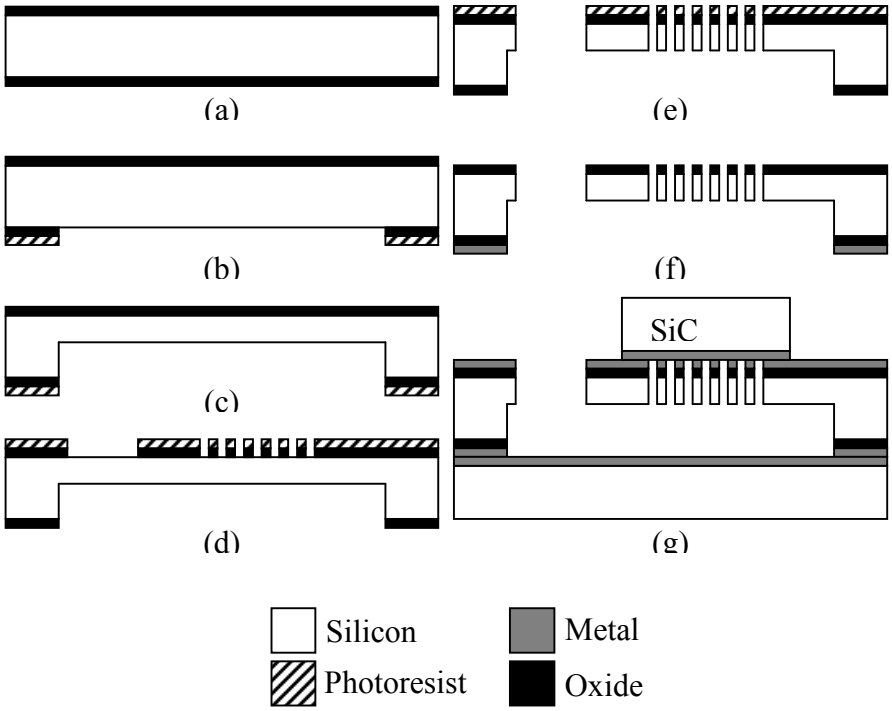


Figure E-3: Brief outline of the fabrication procedure to create the manifold microchannel cooler

Appendix F Data Sheet for ATC Chip Resistor

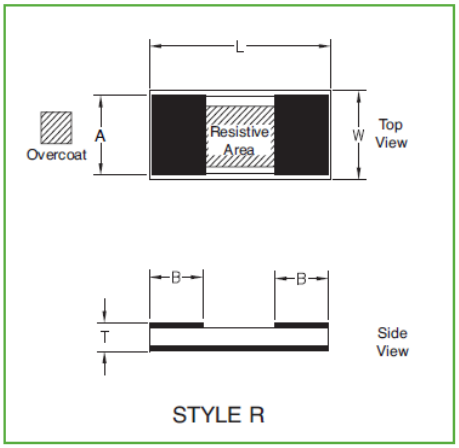
ATC HIGH POWER RESISTIVE PRODUCTS

Chip Resistors

Style CR

General Specifications

- **Resistance:** 100 Ω standard, (other Ω values available)
- **Resistive Tolerance:** ±5% standard (2% Available)
- **Operating Temp Range:** -55 to +150˚C
- **Temperature Coefficient:** <150 ppm/˚C
- **Resistive Elements:** Proprietary Thin Film
- **Substrate Material:** Aluminum Nitride
- **Terminals:** Silver
- **Lead-Free, RoHS Compliant**
- **Reliability:** MIL-PRF-55342
- **Non-Magnetic**
- **Tape and Reel Specifications:** See Page 37 of full Resistive Products Brochure



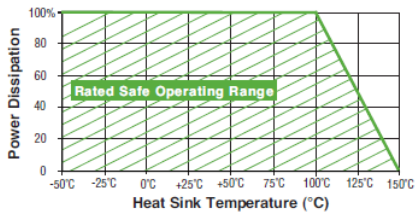
STYLE R

ATC Part Number*	W ±.010	L ±.010	T ±.005	A ±.005	B (Typ.)	Capacitance (pF)	Power Max* (Watts)
CR11005TxxxxJ	.050	.100	.025	.045	.020	.75	5W
CR11206TxxxxJ	.060	.120	.025	.055	.020	.90	15W
CR12010TxxxxJ	.100	.200	.040	.090	.020	1.0	30W
CR12525TxxxxJ	.245	.245	.040	.130	.020	2.0	60W
CR12525TxxxxJ01	.245	.245	.040	.130	.020	2.0	100W
CR13725TxxxxJ	.250	.375	.040	.198	.025	4.15	150W
CR13737TxxxxJ	.370	.370	.040	.330	.025	6.0	250W

** xxxx denotes Ohm value.*

*** Test Condition: Chip soldered to a large copper carrier whose surface is at 100˚C; maximum rated power applied.*
Specification: The resistance of the film shall change no more than 0.5% during and after a 1000-hr. Burn-in per Mil-PRF-55342.

Power Derating



ATC Part Number Code

CR1 2010 T xxxx J TR

- Case Style
- Case Size
- Termination
- Value: 100 Ω = 0100, 50 Ω = 0050
- Tolerance: See table below.
- Packaging: TR - Tape & Reel, BK - Plastic Carrier

Resistive Tolerances		
Code	G (%)	J (%)
Tol.	± 2	± 5

Excerpt from ATC # 001-944; Rev. I, 1/09

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