ABSTRACT

Title of Dissertation: A GALLIUM NITRIDE INTEGRATED ONBOARD CHARGER

Shenli Zou, Doctor of Philosophy, 2020

Dissertation directed by: Professor, Alireza Khaligh, Department of Electrical and Computer Engineering

Compared to Silicon metal–oxide–semiconductor field-effect transistors (MOSFETs), Gallium Nitride (GaN) devices have a significant reduction in gate charge, output capacitance, and zero reverse recovery charge, enabling higher switching frequency operation and efficient power conversion. GaN devices are gaining momentum in power electronic systems such as electric vehicle (EV) charging system, due to their promises to significantly enhance the power density and efficiency. In this dissertation, a GaN-based integrated onboard charger (OBC) and auxiliary power module (APM) is proposed for EVs to ensure high efficiency, high frequency, high power density, and capability of bidirectional operation.

The high switching frequency operation enabled by the GaN devices and the integration of OBC and APM bring many unique challenges, which are addressed in this dissertation. An important challenge is the optimal design of high-frequency magnetics for a high-frequency GaN-based power electronic interface. Another challenge is to achieve power flow management among three active ports while minimizing the circulating power. Furthermore, the impact of circuit layout parasitics

could significantly deteriorate the system interface, due to the sensitivity of GaN device switching characteristics.

In this work, the aforementioned challenges have been addressed. First, a comprehensive analysis of the front-end AC-DC power factor correction stage is presented, covering a detailed magnetic modeling technique to address the high-frequency magnetics challenge. Second, the modeling and control of a three-port DC-DC converter, interfacing the AC-DC stage, high-voltage traction battery and low-voltage battery, are discussed to address the power flow challenge. Advanced control methodologies are developed to realize power flow management while maintaining minimum circulating power and soft switching. Furthermore, a new three-winding high-frequency transformer design with improved power density and efficiency is achieved using a genetic-algorithm-based optimization approach. Finally, a GaN-based integrated charger prototype is developed to validate the proposed theoretical hypothesis. The experimental results showed that the GaN-based charging system has the capability of achieving simultaneous charging (G2B) of both HV and LV batteries with a peak efficiency of 95%.

# A GALLIUM NITRIDE INTEGRATED ONBOARD CHARGER

by

Shenli Zou

Dissertation submitted to the Faculty of the Graduate School of the
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# Table of Contents

# List of Tables

# List of Figures

# Chapter 1 : Introduction

## *1. 1 Background*

### 1. 1. 1 GaN devices

The development of Wide Bandgap (WBG) devices, including Silicon Carbide (SiC) and GaN, have promoted the implementation in the power electronic system. Compared to Silicon (Si) metal–oxide–semiconductor field-effect transistors (MOSFETs), WBG devices have a significant reduction in gate charge and output capacitance, enabling higher switching frequency operation and efficient power conversion [1]–[5]. Consequently, the power density of the converter system can be improved. As shown in Table 1-1, WBG devices have much higher electric breakdown fields than Si devices, which leads to increased voltage blocking capabilities [6]. Moreover, WBG devices have higher temperature operation capability due to higher bandgap energy, compared to Si devices [7].

Table 1-1. Comparison of key properties of Silicon and WBG devices [8].

| Items | Si | 4H-SiC | GaN |
|---|---|---|---|
| Bandgap (eV) | 1.1 | 3.2 | 3.4 |
| Electron mobility ($cm^2V^{-1}s^{-1}$) | 1400 | 1000 | 1200 |
| Thermal conductivity ($W\ cm^{-1}K^{-1}$) | 1.5 | 2.7 | 2.1 |
| Breakdown electric field (MV/cm) | 0.3 | 2.2 | 3.3 |

In particular, GaN devices possess a superior relationship between breakdown voltage and on-resistance. In other words, for a given on-resistance and breakdown voltage, the die size of a GaN device is much smaller than that of its Si counterpart, and thus, there is significant

potential for improving the power density [9]. A more vivid way to visualize the performance of semiconductor devices is to plot the figure of merit, which is a combination of on-resistance and gate charge. As shown in Fig. 1-1, at least one order of magnitude improvement in specific figure-of-merit can be achieved for GaN devices over Si and SiC devices. Furthermore, GaN devices have zero reverse recovery charge due to the absence of the intrinsic body diode. Because of the extremely low gate charge and junction capacitance in GaN devices, the current and voltage transition intervals are shortened, and thus the switching loss is reduced.

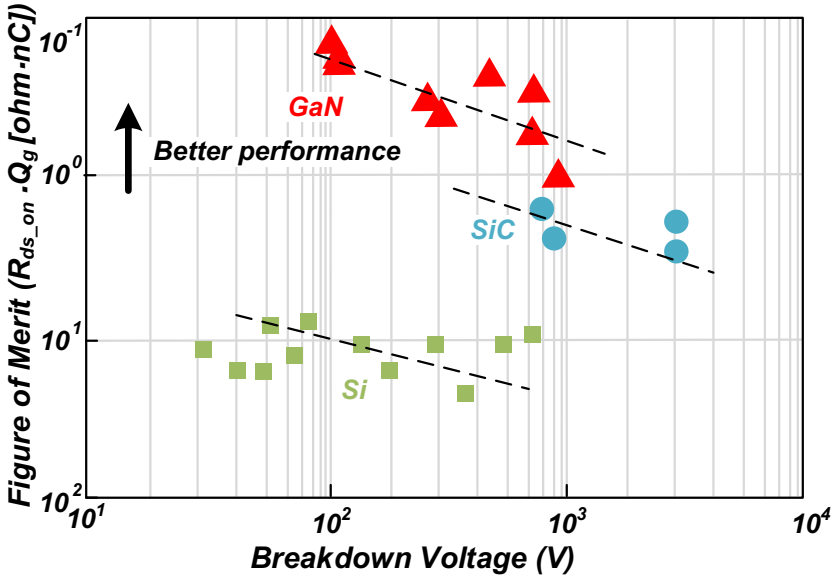



Fig. 1-1. The comparison of figure-of-merit over Si, SiC, and GaN devices [10]–[12].

The properties of the GaN devices make them appealing candidates for the power-dense applications, including consumer electronics, data center power supplies, and EV battery chargers. Fig. 1-2 demonstrates the long term GaN power device market evolution [13]. Following an initial small-volume adoption of GaN-based power supplies in AC/DC adapters, a broader acceptance of GaN devices is expected in the near future with the development of high-voltage and high-power GaN devices. The Department of Energy estimated that the global

market for GaN power devices would rise to $1.4 billion by 2030, with a significant improvement in the cost-competitiveness and reliability [14].

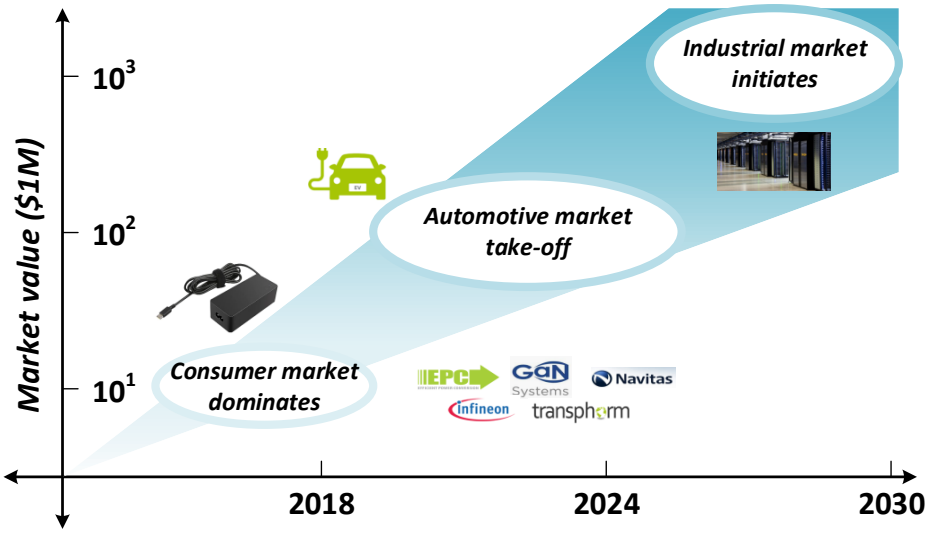



Fig. 1-2. Long term GaN power market evolution [13].

1. 1. 2 EV Charging System

With the growing interest in transportation electrification [15], electric vehicles (EVs) are gaining more attention and acceptance. It is predicted that 30% of the U.S. auto market share will be electric vehicles by 2030 [16]. For China and India, the number is 40% by 2030 [17]. As EVs become more widespread in the near future, it is critical to be prepared for the large energy concentration onboard.

One focus of current research in EVs involves the charging system. Conventionally, there are two independent charger units inside EVs. An onboard charger (OBC) is the power electronic interface between the power grid and the high voltage (HV) traction battery. The auxiliary power module (APM) is another separate power unit that charges the low voltage (LV) battery, which is utilized to supply auxiliary loads and consumer electronics onboard the vehicle. According to Society of Automotive Engineers (SAE) J1772 standard [18], OBCs can be categorized as Level 1, Level 2, and Level 3 chargers in terms of their power ratings. Most

EVs can be charged at home overnight in a garage for Level 1 charging with a convenience outlet [19]. Level 2 charging is generally implemented as the primary method for both private and public facilities [20]. Traditionally, Level 2 OBCs have a power rating of 3.3kW with a typical weight of 6kg, a volume of 7L, and maximum efficiency of 93% [21], [22] using Silicon MOSFETs. The OBC power ratings are increasing, and 6.6kW, 11kW, and 22kW OBCs are becoming popular as a result of the increase in the battery capacity [23]. For instance, a 6.6kW OBC product was released by Currentways [24]; this OBC weighs 11kg, occupies 11L in volume, and has a peak efficiency of 90%.

The most prominent challenges for EV onboard chargers are volume, weight, and efficiency. A light and power-dense onboard charger would provide additional space for a high-volume battery pack [25]. The use of GaN devices will accelerate the development of high power density, high-efficiency EV charging system. In [26], a 6.6 kW bi-directional onboard charger based on both SiC and GaN devices is developed. The power density of 2.3 kW/L and 96% efficiency are reported. Furthermore, a 22kW OBC using GaN Systems' power semiconductors is demonstrated in [27], which achieves a power density of 4kW/L and 96% efficiency. In [28], an indirect matrix converter-based EV battery charger is presented. It is reported that the peak efficiency is 97% at 7.2kW with the implementation of GaN devices.

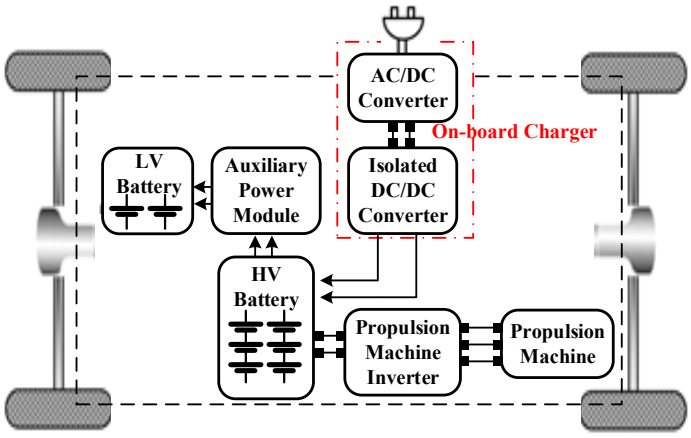



Fig. 1-3. The typical EV power system, including OBC and APM interfaces.

The typical EV charging system is shown in Fig. 1-3, where the OBC and APM are configured as separate charging interfaces. Many efforts have been made to improve the power density of the EV charging system by using integrated OBCs with associated functionalities [29]–[35]. In [36], an integrated onboard charger using Si devices is introduced. The OBC and APM are integrated through a three-winding transformer. However, there are many drawbacks in this design: (i) the implementation of Silicon devices, to keep a low and competitive cost, leads to low efficiency and low power density as a result of slow switching frequency operation; (ii) the control for the three-port converter is not optimized to reduce the circulating energy, due to the limitation of using only the two phase-shift variables; (iii) the three-winding transformer design has a large volume and the existence of inter- and intra-winding parasitic capacitances lead to distorted voltage/current waveforms and spikes.

In this dissertation, a GaN-based integrated charging system is proposed to address these issues, while achieving high power density and high efficiency.

### 1. 1. 3 Challenges of GaN-Based System Design

Despite the aforementioned advantages of GaN devices, there are a few challenges raised by GaN devices in the integrated charging system, including sensitivity to circuit parasitics, complexity of high-frequency magnetic design, control problems for the integrated system, robust gate driver design to handle high switching speed, and soft switching technique [4], [37]–[40].

(a) High-frequency magnetic design

Increasing the switching frequency brings additional challenges in terms of skin effect and proximity effect, which in turn would lead to the reduced effective cross-section area in the windings [41], and consequently significantly increases the conduction loss. At the high-frequency operation, it is also desired to achieve the low parasitic capacitance to ensure that the operating waveforms are not distorted. Thus, a systematic magnetic modeling approach,

including the loss, inductance, and parasitics, becomes a necessity to achieve the optimal design of high-frequency magnetic components in GaN-based power converters.

(b) Control challenges

Since a GaN device has a small package for the limited heat dissipation, good dynamic performance under high-frequency operation is of significance to relieve the hardware burden; in particular, there is a need for inrush current control during system start-up. Moreover, with the increased switching frequency, the switching losses of the MOSFETs will rise significantly. Therefore, soft switching under all the load conditions should be ensured as a part of the control target. Furthermore, in a GaN-based integrated charging system, power flow management among three active ports is required. This involves a detailed modeling problem to decouple three power loops and a comprehensive control strategy that considers both efficiency and voltage/power regulations. In other words, the circulating power needs to be minimized while ensuring soft switching transitions.

(c) High-frequency gate driver

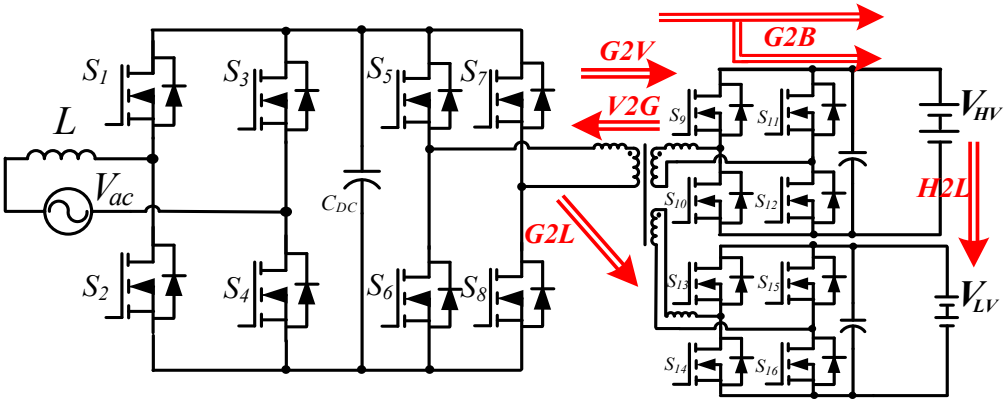
GaN devices have small gate charge and low junction capacitance, which can translate into high switching speed. Hence, $dv/dt$ and $di/dt$ during the switching transitions are ~5 times higher than those of Si MOSFETs [42]. As a result, it brings many challenges in the gate loop design. The $dv/dt$ is coupled through the parasitic capacitance between the switching node and the ground plane, which can lead to mis-trigger of the gate signals. The normal operation of the converter can be significantly affected. Moreover, the $di/dt$ introduces a voltage drop on the common source inductance, which is defined as the inductance shared by the power loop and the gate driver loop. This affects the turn-on and turn-off processes, and the ringing caused by the $di/dt$ contributes to the switching loss. Hence, a robust gate driver design with high noise immunity is essential in a GaN-based charging system.

## *1. 2 Objectives and Research Problems*

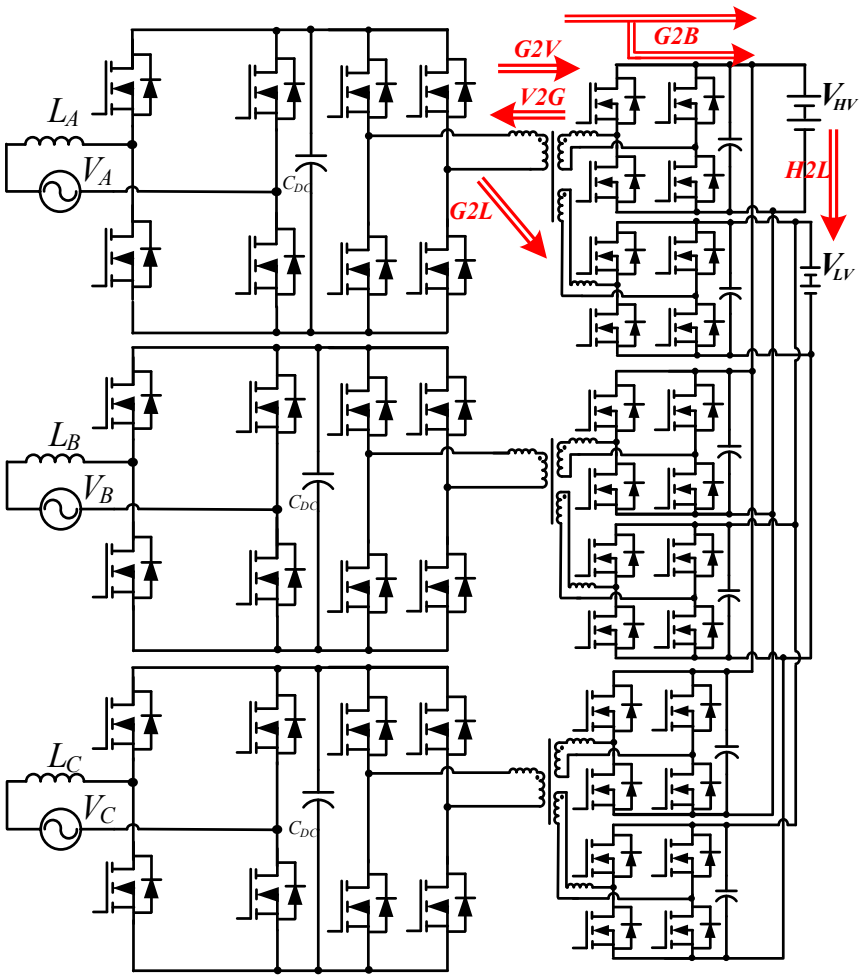
The objective of this work is to propose a new design for an integrated charger using GaN devices, which enables simultaneous charging and satisfies all of the requirements of an integrated OBC and APM. The challenges raised by GaN devices are addressed, including the thermal management, high-frequency magnetic design, power loop and driver circuitry, and soft switching under all load conditions. Hence, the research concentrates on enhancing the power density of the AC-DC conversion unit and also, on improving the performance metrics including efficiency, dynamics, start-up, input power quality, and electromagnetic interference (EMI) over wide load ranges. The major contributions of this work are briefly summarized as follows:

- A three-port GaN-based power electronic system design with one input and two outputs, capable of simultaneously charging of both HV and LV batteries while achieving tight regulation of output voltages.
- A comprehensive control method to suppress the start-up inrush current at the input side.
- Innovative control and modulation methodologies to minimize the circulating power using a hybrid phase shift-duty ratio modulation strategy for the triple-active-bridge-based topologies.
- A detailed analytical model for the boost inductor design considering the dynamic current ripple of GaN devices, to achieve an accurate prediction of inductor performance.
- Optimal design of a high-frequency three-winding transformer, considering the design space variables, i.e. core geometry and wire types, and the performance space variables, i.e. efficiency, volume, and weight.

The topology of the proposed single-phase charger system is shown in Fig. 1-4 (a). The single-phase system is composed of a bi-directional single-phase PFC rectifier and a triple active full-bridge (TAB) converter. The single-phase topology is proposed due to the following reasons: (i) it is modular and can be easily extended to any power level; (ii) it consists of a two-stage topology, which reduces the control burden with a fixed DC link voltage; (iii) By using a phase-shifted structure, the maximum power transfer capability is achievable with reduced conduction loss and voltage/current stress on components. As shown in Fig. 1-4 (b), the proposed single-phase system is extended to a three-phase high-power system with three modular units. Due to various challenges raised during the project, we are first focusing on the design and development of a single-phase module, while a three-phase system could be considered in future research.




(a)



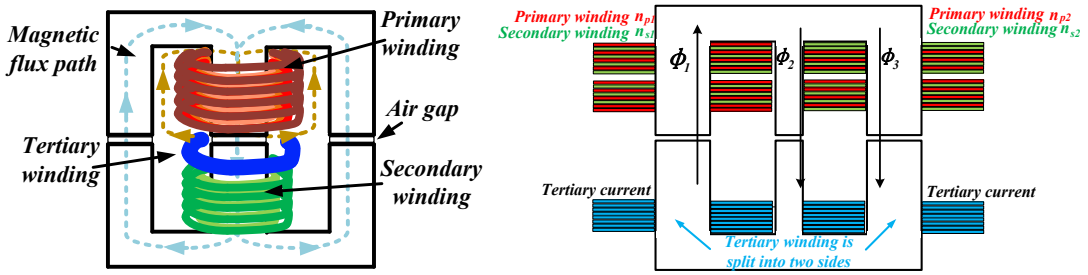

(b)

Fig. 1-4. The proposed GaN-based integrated EV charging systems: (a) a single-phase module; (b) a three-phase system.

The shim inductors in the DC-DC conversion stage play the role of transferring power and achieving soft-switching for the GaN switches inherently, which can be obtained through the leakage inductance control of the three-winding integrated transformer. It is the first GaN-based integrated OBC capable of simultaneous charging of both HV and LV batteries from the grid while minimizing the circulating power. The integrated charging system also has the capabilities of grid to HV battery (G2H) charging, grid to LV battery (G2L) charging, HV battery to LV battery (H2L) charging, vehicle to grid (V2G) discharging. This dissertation

addresses many of the aforementioned challenges at a switching frequency of ~100kHz to investigate and develop some of the fundamental and basic required knowledge to extend the future designs of a 500kHz and consequently a 1MHz switching frequencies.

In this dissertation, to reduce the converter size and the magnetic component losses, a three-winding integrated transformer is implemented. Detailed transformer modeling and loss analyses are conducted, and a transformer optimization problem is formulated, considering the design space variables, i.e. core geometry and wire types, and the performance space variables, i.e. efficiency, volume, and weight. Thus, two sets of transformer designs are developed, namely, a Litz-wire transformer and a planar transformer with the printed circuit board (PCB), which are shown in Fig. 1-5.




(a) (b)

Fig. 1-5. The integrated transformer configuration: (a) the Litz-wire based transformer; (b) the planar transformer.

The proposed GaN-based integrated charger is expected to be smaller in volume and lighter in weight compared to the previously investigated Silicon counterparts [36]. The reduced conduction and switching losses are achieved by using GaN devices, which demonstrate low on-resistance, fast switching speed, and zero reverse recovery charge.

## *1. 3 Synopsis of the Dissertation*

This dissertation presents the first GaN-based integrated onboard charging with the capability of simultaneous charging of both HV and LV batteries for EVs.

In Chapter 2, a comprehensive analysis of a single-phase totem-pole PFC rectifier is disclosed. First, a thorough review of single-phase PFC topologies is presented. Then totem-pole PFC rectifier is selected as the front-end PFC stage. An integrated control strategy is proposed to resolve the zero-crossing distortion in a totem-pole PFC rectifier, and a soft transition-based algorithm with closed-loop control is developed considering the GaN switching characteristics, junction capacitor of GaN MOSFETs, abrupt duty ratio changes and digital delays. Furthermore, a start-up control to achieve the minimum inrush current is proposed to enhance the dynamic performance and relieve the hardware burden. Besides, a comprehensive design for differential mode (DM) filters is established to satisfy the required noise spectrum attenuation. Finally, in order to obtain an accurate estimation of the boost inductance and its losses, a dynamic ripple-based estimation method is proposed considering the variation of material permeability and ripple function. As the verification, the totem-pole PFC rectifier is built and tested. It is experimentally reported that at 2.8kW output power, the efficiency is 98.5% and the power factor is 0.995. In addition, the total harmonic distortion (THD) is reported below 1%.

In Chapter 3, a comprehensive design approach for a three-winding transformer is presented for both the Litz-wire and PCB-winding transformers. A systematic transformer loss model, including both core and winding losses, is investigated. Different winding configurations are discussed. In the planar transformer design, the primary and secondary windings are split unevenly in both side legs, with the aim of reducing the winding loss and sustaining the required leakage inductances. A modified transformer model is developed and utilized to obtain the magnetizing and leakage inductances, which are then verified using both

the analytical model and simulations. Moreover, a comprehensive study on the parasitic capacitance is conducted, considering the trade-offs between the winding loss and the parasitic capacitance. Hence, a multi-objective optimization problem is formulated to optimize the integrated transformer design considering core geometry, losses, and inductances. Finally, the proposed transformer design is experimentally validated.

In Chapter 4, the design and control of a GaN-based three-port DC-DC converter are discussed. Two candidate DC-DC converter topologies are first investigated considering the design specifications, control flexibility and complexity. It is confirmed that TAB converter is the better topology candidate for the operation of simultaneous charging. Furthermore, the detailed modeling of a TAB converter is presented. The decoupled power circuits considering the phase shifts and duty ratios as control variables are developed. Based on the delta equivalent circuit model, an analytical model is established using the generalized harmonic approximation (GHA), which can fundamentally maintain high accuracy concerning different orders of harmonic components. The proposed model is verified by the experimental results. Moreover, two control algorithms are discussed: a circulating power-oriented control and a current-oriented control. The first control algorithm is focused on the minimization of the circulating energy. The second control method is focused on the suppression of the winding current summation. All the winding current waveforms and their root mean square (RMS) values are predicted and computed from the GHA model. With a given range of all the control variables, an executive iteration is conducted to obtain the optimum solution minimizing the total RMS currents. Hence, a hybrid phase shift-duty ratio modulation strategy is synthesized to minimize the circulating power, while realizing the power flow management, and to achieve the soft switching of all switches. To validate the proposed system, an integrated onboard charger hardware is developed and tested. It is reported that the G2B mode peak efficiency is 95.8%, the G2V mode peak efficiency is 96.6%, and the V2G mode peak efficiency is 96%.

Chapter 5 puts forward the conclusion of this dissertation and introduces the remaining research tasks to be completed, the design of a generalized multi-winding transformer, the quadruple-active-bridge (QAB) DC-DC converter, the MHz integrated onboard charger and extension to three-phase modular topologies.

# Chapter 2 : Single-Phase Boost PFC Rectifier

The proposed integrated OBC system in this dissertation is composed of a front-end AC-DC PFC stage followed by a DC-DC three-port converter. Active PFC rectifiers are commonly implemented as the rectifier systems [43], [44], and can be divided into Boost-type PFC [45], [1], [46], Buck-type PFC [47], [48] and Buck-Boost PFC [49] converters. Buck-type PFCs inherently involve discontinuous input phase currents with a heavy EMI burden to shape the grid current [50]. Consequently, a large differential mode (DM) capacitor is often required to deal with the discontinuous ripple current. Therefore, Buck-type PFCs are not suitable for grid-tied EV charger applications.

In other words, an AC-DC topology with continuous input current is a good candidate, as it improves the input power factor due to the less reactive power required by the DM capacitors. This makes a single-phase boost-derived PFC a suitable choice for active AC-DC conversion [51]. Moreover, the front-end boost-derived PFC stage can be implemented using different topologies with a different number of active devices. In a two-switch topology, the two switches in one phase leg are operated at high frequency while the diodes in another leg conduct during each half line cycle. Specifically, the dual-boost bridgeless PFC rectifier [52] is widely used in industrial products due to its low conduction loss and suppressed common-mode (CM) noise. In a four-switch topology, four switches in two legs are actively operated in the switching frequency, which is known as the single-phase H-bridge PFC rectifier [53]. However, the switching loss is significant due to all switches being active. Besides, four active switches cause higher EMI noise and fundamentally require a larger filter inductor as compared to the two-switch topology.

In terms of topology, the totem-pole PFC rectifier eliminates the usage of a Schottky diode and requires only four switches and one inductor [1]. Two switches are operated with the switching frequency while the other two conduct complimentarily in a half-line cycle. The

totem-pole PFC draws attention for several reasons: (i) elimination of the front-end diode bridge, which results in a significant reduction of loss at high power; (ii) substantial suppression of the common mode noise compared to the conventional bridgeless PFC, where the neutral point fluctuates with the switching frequency [54]; (iii) simplification of the topology among the Boost-type bridgeless PFC rectifiers; and (iv) reduction of the switching loss by using one high-frequency leg and one line frequency leg, as shown in Fig. 2-1, compared to H bridge-based PFC. By using the GaN devices, the switching frequency can be pushed to the ~100kHz range or even to MHz level.

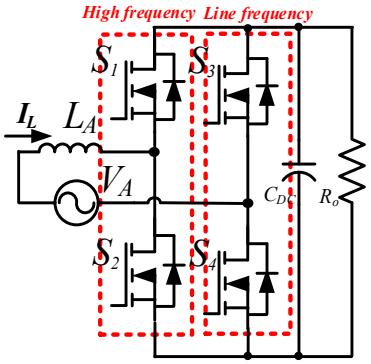


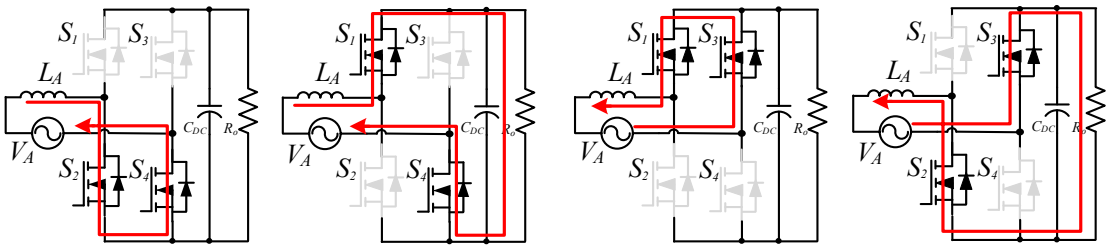

Fig. 2-1. Topology of a single-phase totem pole PFC rectifier.

In order to avoid voltage distortions of the grid arising from power supplies, a total harmonic distortion (THD) less than 5% and an input power factor (PF) greater than 0.99 are often required [43]. Detailed operation analyses and design specifications with several proposed control techniques for the performance improvement are discussed in the following sections.

## *2. 1 Totem-Pole Bridgeless PFC Operation*

The totem-pole PFC rectifier operates periodically in the positive and negative cycles of the single-phase AC input, and determines the current flow depending on how the high-frequency MOSFETs are switched. $S_1 \sim S_4$ are GaN MOSFETs with junction capacitors, and $L_A$ represents the boost inductor, as shown in Fig. 2-1.

In Fig. 2-2, there is one high-frequency leg and one line-frequency leg. The high-frequency GaN MOSFETs together with the inductor form a synchronous mode boost converter. During the positive half-cycle, $S_2$ performs as the boost switch, which is driven with duty cycle $D$, and $S_1$ is driven with a complementary control signal. Similarly, at the time $S_2$ is switched with $1-D$, $S_1$ is driven with duty cycle $D$. It is worth mentioning that the line frequency switch $S_4$ conducts continuously during the positive half-cycle. Because of the symmetry of topology, the commutation processes of the positive and negative half-cycles are similar, except that the roles of the top and bottom switches are swapped.




(a) (b) (c) (d)

Fig. 2-2. Operation modes: (a) Mode I: $S_2$ is ON during positive half-cycle; (b) Mode II: $S_2$ is OFF during positive half-cycle; (c) Mode III: $S_1$ is ON during negative half-cycle; (d) Mode IV: $S_1$ is OFF during negative half-cycle.

The boost inductor $L_A$ plays the role of filter inductor for the input current, as well as boosting the input voltage while transferring power to the DC link side. In Mode I, the inductor is charged through the input current. In Mode II, the inductor energy is discharged to the output. The duty cycle $D(t)$ is changed along with the AC input to maintain unity power factor and realize the output voltage regulation.

## *2. 2 Control of Totem-Pole Bridgeless PFC*

### 2. 2. 1 Current Loop

To regulate the input current and maintain the power factor close to 1, the inner current loop design is implemented. In this work, a continuous-current-mode (CCM) control strategy [55] is utilized for PFC current control, since the switching frequency is ~100kHz. The inductor current is sensed through the current sensor, which is placed away from the switching node to reduce the sampling noise.

Since it is a Boost-type PFC rectifier, the plant transfer function can be expressed as,

$$G(s) = \frac{V_o}{sL_A} \tag{2.1}$$

Using a PI controller $C(s)$ in the current loop, the control block is shown in Fig. 2-3. The closed-loop gain $H(s)$ can be derived as,

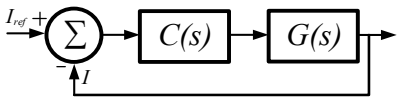



Fig. 2-3. The current control loop.

$$H(s) = \frac{CG}{1+CG} = \frac{K_p(s+z)}{L_A s^2 + K_p s + K_p z} \tag{2.2}$$

where $z$ denotes the zero, $z = \frac{K_p}{K_i}$. The cut-off frequency can be obtained as,

$$\omega_c = \sqrt{\frac{K_i}{L_A}} \tag{2.3}$$

The placement of the zero and the cut-off frequency is critical to the control loop design, which inherently determines the system steady-state and dynamic performance. As shown in Eq. (2.3), $\omega_c$ is directly related to the integral term of the PI controller. If $\omega_c$ is located at a very high frequency, the loop bandwidth would be high, and the input current shape will be distorted. Similarly, the zero cannot be placed at a very high frequency, or it will jeopardize the power factor. The zero also cannot be placed at a very low frequency, where most noises

cannot be filtered. In practice, $\omega_c$ is placed around 1/10 of the switching frequency, and the zero of the current loop is then placed around 1/20 of the bandwidth frequency.

The feedforward control technique is applied to the current loop to improve the robustness of the system [56]. The basic idea is to obtain a "nominal duty ratio pattern" using feedback linearization to partially share the task of the controller. For the Boost-type PFC, the feedforward duty ratio signal is defined as [57],

$$d_n = 1 - \frac{|V_{in}|}{V_o} \tag{2.4}$$

The average voltage across the switch over one switching cycle equals the rectified input voltage. The controller regulates the duty ratio around the nominal pattern to generate a sinusoidal input current. Given the low impedance of the boost inductor at line frequency, a small segment of the duty ratio will lead to enough voltage across the inductor to ensure the desired sinusoidal current shape.

### 2. 2. 2 Voltage Loop

The DC link voltage loop is implemented to provide the power reference and can be utilized as the outer loop of PFC control. The power reference is multiplied by the AC line voltage and further divided by the square of its RMS value to give the instantaneous current reference command [58], as shown in Fig. 2-4. Note that the polarity detection is included in the AC line voltage sensing and computation, which determines the proper ON and OFF timing of the two line-frequency switches.

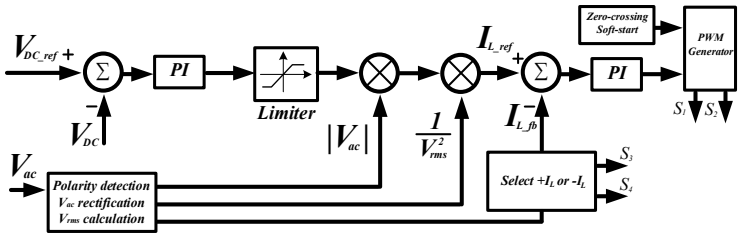



Fig. 2-4. Overall control block of the totem-pole PFC rectifier.

The voltage loop cut-off frequency is set below the double line frequency to ensure low THD under steady-state operation. Moreover, the current sensing filter bandwidth should be higher than the current loop PI controller, such that the loop bandwidth is not affected by the filter. The bode plot of the control loop is shown in Fig. 2-5, where the discretization is considered.

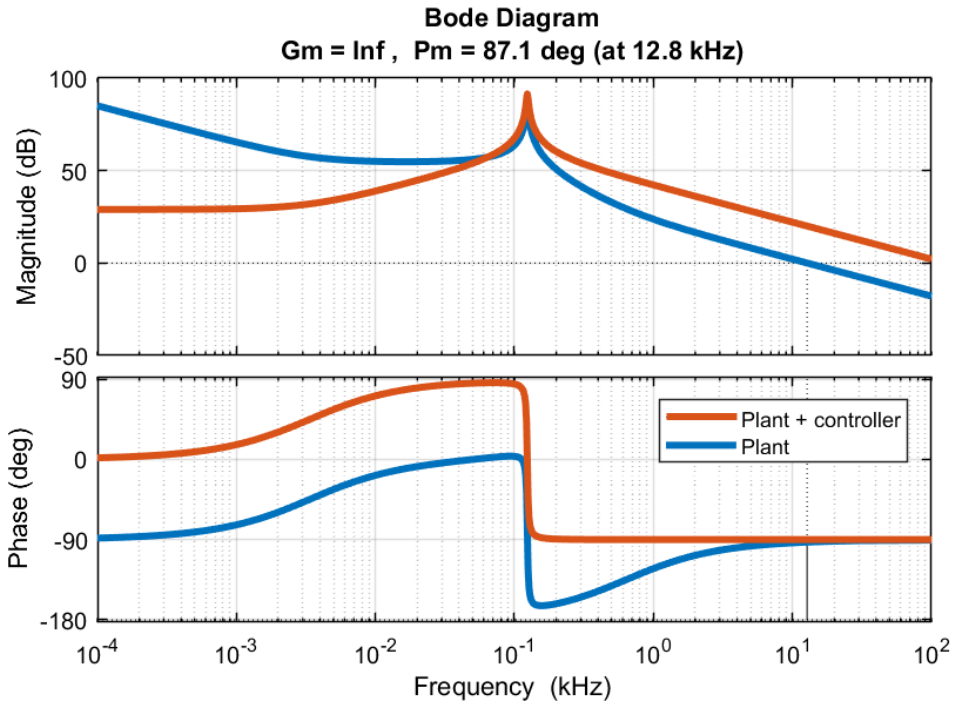



Fig. 2-5. The Bode plot of the plant and the controller.

To validate the dual-loop control method, a simulation has been conducted to examine the THD, voltage ripple, and power factor correction. The simulation shows that tight input current and output voltage regulation are achieved, where the power factor is maintained at a level greater than 0.99, and the THD is lower than 5%.

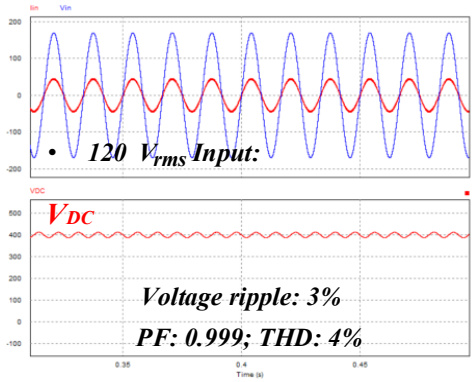



Fig. 2-6. Simulation results for the PFC operation with 120V AC input voltage.

2. 2. 3 Zero-Crossing Distortion and Soft Transition

The input current zero-crossing distortion is a common problem in the totem-pole PFC converter, which is caused by the nature of the circuit operation when high-frequency MOSFETs switch abruptly, and one line frequency MOSFET forms the reverse recovery current at the zero crossing of the line voltage [59]. At the zero-crossing point, the duty cycle of upper and lower switches in the high-frequency leg suddenly change between 0 and 1. Due to the switching characteristics of GaN devices, some current spike will be induced in the following switching period, which will not only degrade the power quality but also increase the loss on the inductor and switches. Furthermore, the junction capacitor of one line frequency switch is charged up to $V_{DC}$, and needs the additional discharging time, which increases the distortion during the transition. Note that the digital delay caused by sensor circuitry and signal processing will also lead to the current spike and zero-crossing distortion [60].

In order to resolve this issue, a soft-transition-based algorithm is developed considering the GaN device $dv/dt$, the junction capacitor $C_{oss}$ in high frequency GaN MOSFETs, and digital delays caused by the sensors and processor. The goal is to avoid abrupt changes in the duty ratio. Instead, the duty ratio needs to be adjusted gradually according to the current waveform. The duty ratio change around the zero crossing region is discretized and described as a function of,

$$\Delta D = f(st, C_{oss}, dv/dt) \tag{2.5}$$

where $st$ represents the number of steps during the soft transition. The control diagram for the zero-crossing transition is shown in Fig. 2-7.

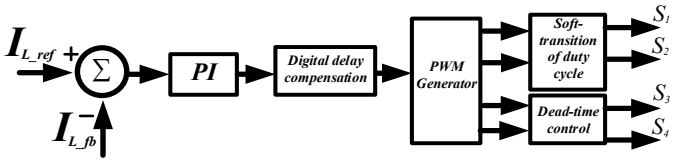



Fig. 2-7. Control diagram for the zero-crossing transition in the totem-pole PFC rectifier.

2. 2. 4 Start-Up Inrush Control

Smooth start-up to limit the inrush current is an important requirement in the development of active PFC rectifiers [61]. The inrush current by start-up resistors is set to the level, which the hardware can tolerate. A non-linear compensator is proposed to limit the inrush current and simultaneously minimize the start-up time for a three-phase Boost PFC [62]. Besides, an innovative start-up scheme is introduced for a three-phase isolated Boost PFC with an innovative topology configuration [63]. In addition to the aforementioned compensator design and topology innovation, a more practical and easy-to-execute start-up technique is proposed [64], where the PWM signal is multiplied with a linear ramp signal before it is applied to the PFC MOSFETs. Furthermore, a variable step-size control technique is proposed in [65] to limit the inrush current during the start-up procedure. The above-mentioned literatures are mainly focused on the start-up procedure of direct three-phase PFC rectifiers; however, the research for analyzing and improving the start-up procedure of the high-frequency totem-pole PFC, in a systematic fashion is currently absent.

In order to address the issues above and concerns with the start-up process in a high-frequency totem-pole PFC rectifier, an algorithm to achieve minimized inrush current [61] is discussed in this work. The main contributions are: (i) mathematical analyses and modeling the

start-up procedure of a single-phase totem pole PFC; and (ii) development of the desired start-up technique by properly adjusting the timing instant of the PFC controller to achieve zero inrush current. It is mathematically proven that the inrush current can be made zero if the PFC action control is engaged at the negative-to-positive zero crossing of the input AC voltage.

***First inrush:*** After powering up the circuit, note that the active semiconductors are initially disabled, as the auxiliary power supply driving the control ICs requires start-up intervals. Therefore, the converter works as a passive diode bridge rectifier. In this mode of operation, the relay is off, and hence, the inrush current is limited by the ratio of the peak-to-peak input AC voltage to the parallel resistor of the relay. By proper selection of the protective resistor, the inrush current amplitude can be suppressed to the desired value.

$$i_{max} = \frac{V_{in,max}}{R_{relay}} \tag{2.6}$$

***Second inrush:*** At the instant when the relay turns on, and the paralleled resistor is bypassed, there is a transient in the input current. An equivalent circuit in this mode of operation is shown in Fig. 2-8, which assumes that the relay-ON event occurs during the positive half-cycle. Applying the KVL relationship at the node connected to the DC link capacitor and output load, the following equations are derived,

$$V_A = L_A \frac{di}{dt} + V_o \ , \ C \frac{dV_o}{dt} + \frac{V_o}{R} = i \tag{2.7}$$

Substituting $\frac{dV_o}{dt}$ in the derivative expression, the following equation is derived as,

$$V_A = L_A C \frac{d^2V_o}{dt^2} + \frac{L_A}{R}\frac{dV_o}{dt} + V_o \tag{2.8}$$

$$V_o(t) = e^{\frac{Rt}{L_A}}[Asin(\omega t) + Bcos(\omega t)] + V_A \tag{2.9}$$

Assume $V_o(t = 0^-) = V_1$, note that $i(0^-) = i(0^+) = i_0$ holds true with the continuous inductor current. Therefore, the coefficients $A$ and $B$ are expressed as,

$$A = \frac{1}{\omega C}\left(i_0 - \frac{V_1}{R}\right) + \frac{R}{\omega L_A}(V_1 - V_A), \qquad B = V_1 - V_A \tag{2.10}$$

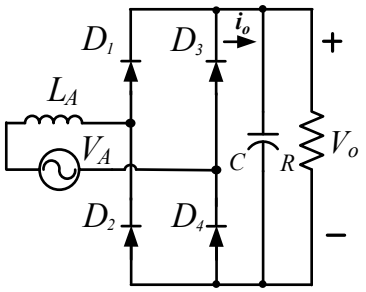



Fig. 2-8. The equivalent circuit after relay-ON.

On the other hand, the grid current at $t = 0^+$ is expressed as follows,

$$i(0^+) = C\frac{dV_0}{dt} + \frac{V_0}{R} = C\left[A\omega - \frac{R}{L_A}(V_1 - V_A)\right] + \frac{V_1}{R} \tag{2.11}$$

Therefore, the instantaneous grid current expression for the second inrush is given by,

$$i(t) = e^{-\frac{Rt}{L_A}}\left[\begin{array}{l}\left\{\left(\frac{1}{\omega C}\left(i_0 - \frac{V_1}{R}\right) + \frac{R}{\omega L}(V_1 - V_A)\right)C\omega + \frac{CR(V_A - V_1)}{L_A} + \frac{V_1 - V_A}{R}\right\}\cos(\omega t) \\ + \left\{(\frac{1}{\omega C}\left(i_0 - \frac{V_1}{R}\right) + \frac{R}{\omega L}(V_1 - V_A))(\frac{1}{R} - \frac{CR}{L_A}) - \omega C(V_A - V_1)\right\}\sin(\omega t)\end{array}\right] + \frac{V_A}{R} \tag{2.12}$$

***Third inrush:*** The third inrush takes place during the transition from the uncontrolled diode rectifier to the actively controlled PFC. It is worth mentioning that the third inrush scenario must be controlled through proper timing of the PFC control signals, as it involves switching behaviors and cannot be passively resolved. It is observed that the output side of the inductor (point *A*) and source neutral point (point *n*) become duty-cycle-dependent, as shown in Fig. 2-9.

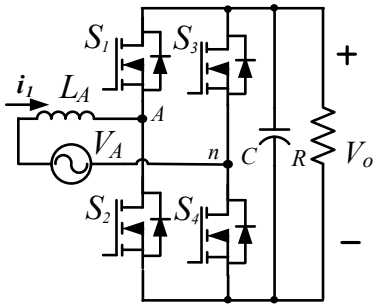



Fig. 2-9. The equivalent circuit at steady-state PFC operation.

Consequently, the current flowing through the parallel branch of the capacitor and load resistor is also duty-cycle-dependent and the relationship is given by,

$$i(2D-1) = C\frac{dV_o}{dt} + \frac{V_o}{R} \tag{2.13}$$

$$D(t) = k_p e(t) + k_i \int_0^t e(\tau)\, d\tau \tag{2.14}$$

where, $e(t)$ is the instantaneous error in the input current, which is expressed by $e(t) = GV_A - i_1$; and $G$ is the DC voltage controller output implying the equivalent input trans-conductance. The duty is generated by the current loop PI controller. Therefore, the expression for the duty cycle is shown as,

$$D(t) = k_p(GV_A - i_1) + k_i \int_0^t (GV_A - i_1(\tau))\, d\tau \tag{2.15}$$

Further simplify the expression with some defined coefficients,

$$D(t) = A_3 i_1 + B_3 \int_0^t i_1(\tau)\, d\tau + Y \tag{2.16}$$

where $A_3 = -k_p; B_3 = -k_i;\ Y = k_p G V_{in} + k_i G \int_0^t V_{in}(\tau)\, d\tau$. The general solution of the above differential equations regarding the input current can be expressed as,

$$\frac{y}{X} e^{\frac{t}{RC}} = \int_0^\tau \frac{y}{X} i_1 \left(2\frac{dX}{dt} + i_1 - 1\right) dt \tag{2.17}$$

Due to the diode bridge operation, the input current will be held at zero for a significant portion of the line cycle. Assuming the control is turned on while $i_1 = 0$, '$y$' simply equates to $V_A$. Assuming the peak current occurs at $t = t^*$, $\frac{di_1}{dt} = 0$ holds at the current peak value. Since obtaining a deterministic expression for $i_1$ through a particular integral solution would be challenging, the variation of the input current is determined using the initial and final values of '$y$'. Therefore, the general expression of the input current $i_1$ can be formulated as,

$$i_1 = GV_A[1 - e^{-\frac{B_3 t}{A_3}} \sin\left(\sqrt{\frac{B_3}{A_3}} t + \varphi\right)] \tag{2.18}$$

If the control is applied during the transient from positive to negative half-cycle, the maximum input current $i_{1,max1}$ will be given by the following expression, which can be as large as $2GV_{in}$,

$$i_{1,max1} = GV_A[1 + e^{-B_3 t^*/A_3}] \tag{2.19}$$

On the other hand, if the control is applied near the zero crossing from negative to positive half-cycle, the peak input current can be $i_{1,max2}$, whose maximum value is $GV_A$,

$$i_{1,max2} = GV_A[1 - e^{-B_3 t^*/A_3}] \tag{2.20}$$

In order to accurately determine the peak input current value and its corresponding time instant, it is necessary to solve for $\frac{di_1}{dt} = 0$. The solution is given by,

$$tan\left(\sqrt{\frac{B_3}{A_3}}t^* + \varphi\right) = \sqrt{\frac{B_3}{A_3}} \tag{2.21}$$

which implies $t^* = \sqrt{\frac{A_3}{B_3}}[tan^{-1}\left(\sqrt{\frac{B_3}{A_3}}\right) - \varphi]$. Although the circuit operation and the implementation of the control algorithm are symmetric at the two zero crossings from positive-to-negative and negative-to-positive half-cycles, the inrush transient dynamics after enabling the control are not symmetric at the two zero crossings.

The control block diagram is shown in Fig. 2-10, describing the proposed start-up inrush current control. Due to the reduced peak current, the PFC control loop is performed during the zero crossing from negative to positive half-cycle. The trigger signal is enabled when the negative to positive zero crossing of the input AC voltage occurs. This process involves the zero-crossing detection and polarity detection, which can be achieved through sensing the input voltage using a second-order generalized integrator (SOGI)-based phase locked loop (PLL) and low pass filter.

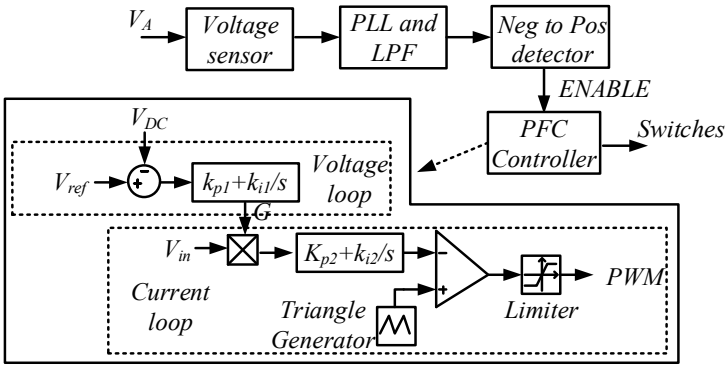



Fig. 2-10. Block diagram for the PFC minimal start-up inrush current control.

## *2. 3 EMI Filters*

The PWM-based PFC operation is engaged to retain a high power factor, which inherently results in certain amounts of high-frequency noise. Also, the high-frequency switching harmonics and the parasitic capacitors and inductors lead to the electromagnetic interference (EMI), which degrades the input power quality and pollutes the grid. Therefore, EMI filters are employed to attenuate the noise and comply with the relevant EMI standard, depending on the particular application. For EV charger applications, CISPR/B (also known as FCC Class B) specifies the minimum interference requirement for industrial equipment, power lines and electric tractions [66]. A proper design of EMI filters is essential to ensure the desired volume, efficiency, stability, and manufacturability of the converter.

EMI can be divided into two categories: (1) radiated noise; and (2) conducted noise [67]. In this work, the radiated EMI spectrum, ranging from 30 MHz to 1 GHz, is excluded; the conducted EMI noise, ranging from 150 kHz to 30 MHz, is considered. The conducted noise can occur via two modes of emissions: differential mode (DM) and common mode (CM). In Boost PFC rectifiers, DM noise is commonly caused by the current ripple and magnetic coupling [68], [69], whereas CM noise arises primarily due to the parasitic capacitances (i.e., between heat sink and switches), and interleaving capacitances in the magnetic components. In this section, DM noise will be modeled, and the corresponding DM filter will be designed with the help of the proposed dynamic ripple-based estimation method. As verification, the simulation results are given to validate the proposed EMI filter design.

### 2. 3. 1 DM Filter Modeling

The selection of DM cut-off frequency is critical in the design process. In practice, a feasible approximation to initiate the design would be around $1/15^{th}$ to $1/10^{th}$ of the switching frequency [70], considering the trade-off between high-frequency noise damping and EMI peak attenuation. The equivalent circuit of the DM filters along with the PFC rectifier is shown in

Fig. 2-11. As shown in the figure, the filter design also accounts for the presence of the boost inductor and the noise measurement equipment: a line impedance stabilization network (LISN). Note that the total impedance seen into the EMI filters needs to be much larger than the impedance offered by the LISN in order for the DM noise to be measured. The LISN is illustrated by its simplified circuit, where $V_{noise}$ represents the measured noise through a 50Ω measuring resistor $R_{LISN}$.

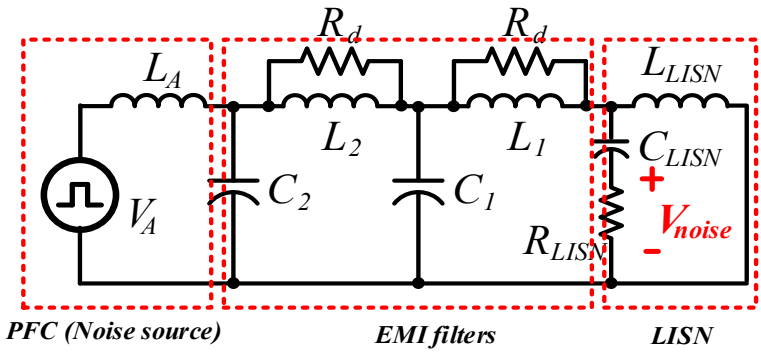



Fig. 2-11. The equivalent circuit of the DM filters with the PFC rectifier and LISN.

Considering the nonideality of the CM chokes, the effective DM inductance $L_1$ per stage can be expressed as the sum of leakage inductance $L_{CM1_{leak}}$ and DM choke inductance $L_{DM1}$. Similarly, the effective DM inductance can be obtained as $L_2 = L_{CM2_{leak}} + L_{DM2}$. Therefore, the DM cut-off frequencies are defined as,

$$f_{c,DM1} = \frac{1}{2\pi\sqrt{L_1 C_1}},\ f_{c,DM2} = \frac{1}{2\pi\sqrt{L_2 C_2}} \tag{2.22}$$

Given the specified EMI standard (CISPR/B) [71], the required attenuation can be presented as,

$$Attenuation_{DM} = v_{DM}(f_s) + margin - limit \tag{2.23}$$

A proper selection of $LC$ values is obtained by considering the cut-off frequency, volume and attenuation performance ($L_1 = L_2 = 50\mu H, C_1 = C_2 = 2\mu F$). Furthermore, damping resistors $R_d$ connecting in parallel with DM inductors are utilized to achieve a high-Q peak suppression in the frequency spectrum, which offers considerable impedance as compared to

the inductor branch in the first peak frequency (210kHz). Thus, an *RL* branch is formed by the damping resistor and the DM inductor, and the equivalent impedance can be expressed as,

$$Z_{RL} = \frac{j\omega L_{DM} R_d}{j\omega L_{DM} + R_d} \tag{2.24}$$

Note that the selection of the damping resistors would significantly affects the high-frequency noise attenuation. If a lower value is selected, the *RL* branch will appear to be resistive at a lower frequency, resulting in poorer attenuation and inducing more power loss. In this design, the damping resistors are selected as 100Ω. Thus, the DM filter frequency response in terms of magnitude is shown in Fig. 2-12. It is observed that at the first spectrum peak (210kHz), the desired filters offer a good noise attenuation of 110 dB.

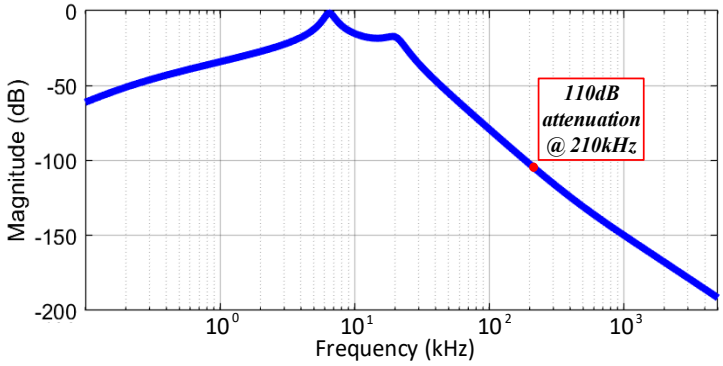



Fig. 2-12. DM filters frequency response attenuation.

By considering the inductance variation and current ripple function over the line cycle $I_{ripple}(t, L_A)$, the corresponding DM filter design can be confirmed under the worst-case scenario. In fact, the boost inductance and the current ripple can be optimized with the EMI filter stage, which constitutes a multi-objective optimization problem with the following cost function,

$$f\left(I_{ripple}, L_A, t, B_{high}, N_{EMI}\right) = \frac{P_{EMI,loss}}{P_{EMI,loss,max}} \frac{V_{EMI}}{V_{EMI,max}} \frac{EMI}{EMI_{max}} \tag{2.25}$$

where $N_{EMI}$ represents the number of EMI stages required. $V_{EMI}$ is the total volume of the boost inductors and EMI filters, which is given by,

$$V_{EMI} = f_{DM,cap}(C,V) + f_{DM,ind}\left(L, I_{ripple}\right) + f_{CM,cap\&ind}(C,L) + f_{Boost,ind}\left(L, I_{ripple}, \omega_c\right) \quad (2.26)$$

The volume estimation for the boost inductor is based on the current loop bandwidth and current ripple requirement, which can be minimized to achieve a compact design while maintaining a good cooling solution.

### 2. 3. 2 Simulation Verification

The EMI spectrum is examined through a simulation using the fast Fourier transform (FFT). Since this design is concerned with the DM filters, the focus of the frequency range will be below 5MHz, where DM noise dominates the EMI spectrum. The PFC rectifier used in the simulation has been discussed in the last section. The noise measured in the simulation at the LISN resistor, along with the FCC Class B standard, is given in Fig. 2-13.

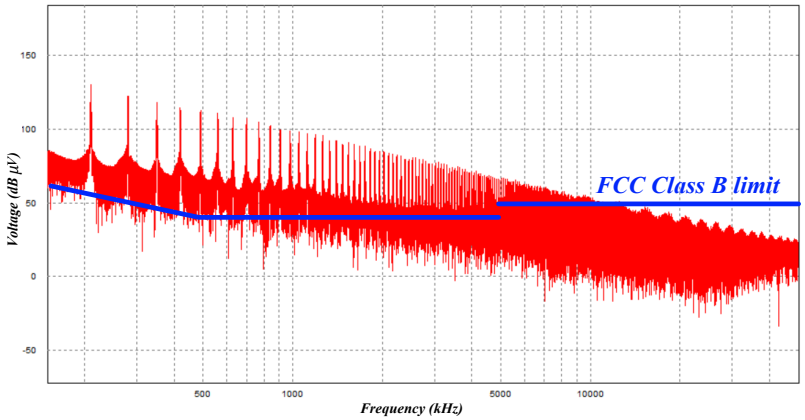



Fig. 2-13. Simulated EMI spectrum at the LISN without any filters.

For comparison, Fig. 2-14 shows the EMI spectrum with the DM filter stage. It is observed that the first several peaks are under good suppression and the high-frequency attenuation conforms to the required limit.

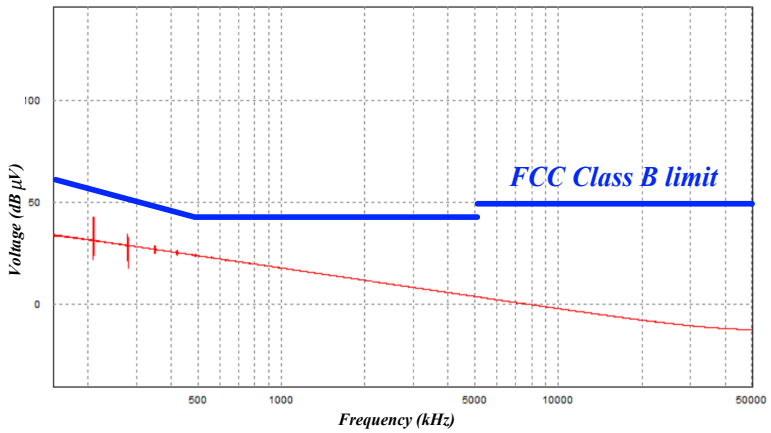



Fig. 2-14. Simulated EMI spectrum at the LISN with DM filters.

## *2. 4 Improved Dynamic Ripple-Based Inductor Design*

To realize the benefits of GaN devices, the optimal design of the high-frequency magnetic components becomes a necessity. Particularly, the input current switching ripples flowing through GaN devices affect the performance of the boost inductor. Some research has been conducted to develop the accurate loss and behavior model for the PFC rectifiers. In [72], a detailed analytical model for the Boost PFC rectifier was proposed, and backed up by the experimental results. However, this work did not consider the influence of the inductance variation on the current ripple, which degrades the accuracy of the loss breakdown. In fact, the permeability of the magnetic material is partially affected by the inductor current rating [73]. As a result, the inductance value varies over the line cycle, which leads to deviations from the value calculated under the assumption of an ideal inductor. The work in [74] considered the non-ideality, variation of the PFC inductance value, and its influence on the input current ripple. A loss estimation model was proposed based on this premise, and comparisons were made to validate the accuracy of the proposed model. However, the current ripple tracking methodology is limited to the continuous current mode (CCM) operation because the current ripple is averaged over one switching cycle. Moreover, since there is one sampling value over the

switching cycle, the high-frequency current ripple is ignored. The resulting error can be significant, depending on the current rating and the material characteristics.

In this section, an improved modeling and loss estimation method for the PFC inductor is proposed. Compared to [74], two current sampling values are calculated over the switching cycle, such that both switching frequency and line frequency ripples are included. Thus, a realistic cycle-by-cycle current ripple tracking technique is synthesized with the dynamic inductance function to improve the accuracy, considering the operation temperature, current rating, and flux density. Moreover, due to the improved ripple tracking method, the proposed loss estimation model is no longer restricted to the CCM operation PFC rectifiers, but can be applied to the critical current mode (CRM) and discontinuous current mode (DCM) as well.

### 2. 4. 1 Current Ripple Analysis

The boost inductor needs to be carefully designed, considering the weight, volume, efficiency, flux variation, and current ripple requirement. It is also related to the current loop bandwidth in the PFC control. In order to pursue an accurate estimation of the inductance and the corresponding loss, a dynamic inductance model is established by considering the current ripple over one switching cycle.

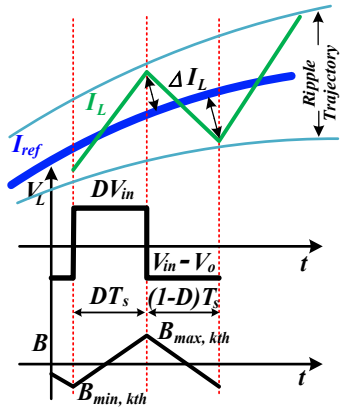
In terms of the shape, the toroid core is commonly used because of its small size and manufacturability. On the other hand, High Flux material [73] is selected due to its highest biasing capability of all powder core materials. This material has a high saturation flux density ($1.5T$) and relatively low loss characteristics, making it suitable for high-power high-frequency applications. Based on the project specifications, the boost inductor current can be calculated. The current ripple is required to be within 10% of RMS magnitude of the inductor current $I_m$, which can be expressed as,

$$|\Delta i_L| = \left| \frac{V_A\left(\frac{V_A}{V_{DC}} - 1\right)}{2L_A f_s} \right| \leq 0.1 I_m \tag{2.27}$$

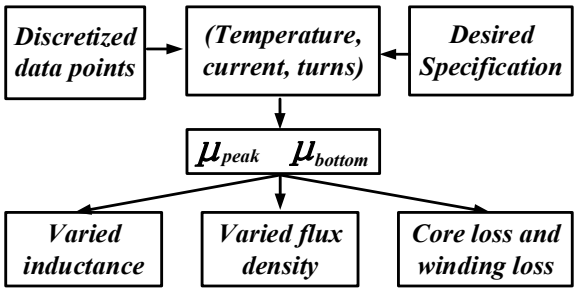
where $L_A$ represents the boost inductance, $f_s$ is the switching frequency, and $V_{DC}$ is denoted as the DC output voltage of the Boost PFC rectifier. $|\Delta i_L|$ is defined as half of the difference between adjacent peak and bottom currents. Eq. (2.27) is formed from the averaged ripple perspective to achieve the initially desired inductance. Depending on the ratio between the magnitude of the input voltage $V_{inm}$ and the DC output voltage, the maximum current ripple can be derived as,

$$|\Delta i_L|_{max} = \begin{cases} \frac{V_{DC}}{4L_A f_s} & if\ \frac{V_{inm}}{V_{DC}} \geq 0.5 \\ \frac{V_{inm}\left(1-\frac{V_{inm}}{V_{DC}}\right)}{L_A f_s} & if\ \frac{V_{inm}}{V_{DC}} < 0.5 \end{cases} \tag{2.28}$$

The first case happens when $\frac{V_{inm}}{V_{DC}} \geq 0.5$, which means that the maximum current ripple is achieved within one quarter line cycle. The second case takes place when the input voltage is smaller than the half of the output voltage, and the maximum current ripple is achieved in the $\pi/2$ and $3\pi/2$ of each line cycle. Moreover, the current ripple varies along with the sinusoidal input current, which unavoidably affects the material permeability and flux density, as shown below. As the duty cycle $D(t)$ is a constant in each half switching cycle, the inductor current function can be computed using the sampling rate $2f_s$. The modeling diagram is shown in Fig. 2-15 (b).




(a)




(b)

Fig. 2-15. (a) Inductor ripple over one switching cycle; (b) Dynamic ripple-based estimation flowchart.

As can be seen in the figure, the current ripple $\Delta i_L$ rises and falls during each switching cycle, depending on the duty cycle $D(t)$. Thus, the general form of current ripple is defined as,

$$\Delta i_L(t) = \begin{cases} \frac{V_{in}(t)D(t)}{2L_A(t)f_s}, \ when\ the\ switch\ is\ ON \\ \frac{(V_{in}(t)-V_{DC})(1-D(t))}{2L_A(t)f_s}, \ when\ the\ switch\ is\ OFF \end{cases} \tag{2.29}$$

$$D(t) = \frac{1}{1-\frac{V_{DC}}{V_{in}(t)}} \tag{2.30}$$

where $L_A(t)$ is the time-varied inductance function. Hence, the dynamic inductor current with the ripple consideration is given by,

$$I_A(t) = I_m \sin(2\pi f_l t) + \Delta i_L(t) \tag{2.31}$$

where $f_l$ denotes the line frequency. With the predicted real-time current waveform, both the core loss and winding loss can be calculated accurately using the sum of the losses in each switching cycle.

### 2. 4. 2 Inductance Variation

Note that flux density has both line frequency and switching frequency terms, which could potentially lead to loss increase, permeability and inductance variation due to the switching frequency current ripple. Conventionally, the flux density in switching frequency has the following expression,

$$\left|B_{high}\right|_{max} = \frac{\int V_L dt}{2n_{toroid}A_{et}} \tag{2.32}$$

where $A_{et}$ is the cross-sectional area of the toroid core and $n_{toroid}$ is denoted as the number of turns. However, this expression fails to consider both the material permeability change and the excitation variation. A dynamic permeability estimation technique is proposed using the fit equations from the datasheet, where the realistic current ripple model is utilized. Similarly, the

flux density function can be calculated considering the time variations of $B_{max}(t)$ and $B_{min}(t)$ over different switching cycles, which are determined by the current levels at the moment of switching. The flux density function $B(t)$ and the material permeability $\mu(t)$ are given by,

$$B(t) = \left[\frac{a_1+b_1H(t)+c_1H(t)^2}{1+d_1H(t)+e_1H(t)^2}\right]^{f_1}, \quad H(t) = \left|\frac{I_{in}(t)n_{toroid}}{l_e}\right|, \qquad \mu(t) = \frac{0.01\mu_0(1+a_2+b_2T+c_2T^2)}{a_0+b_0H(t)^{c_0}} \tag{2.33}$$

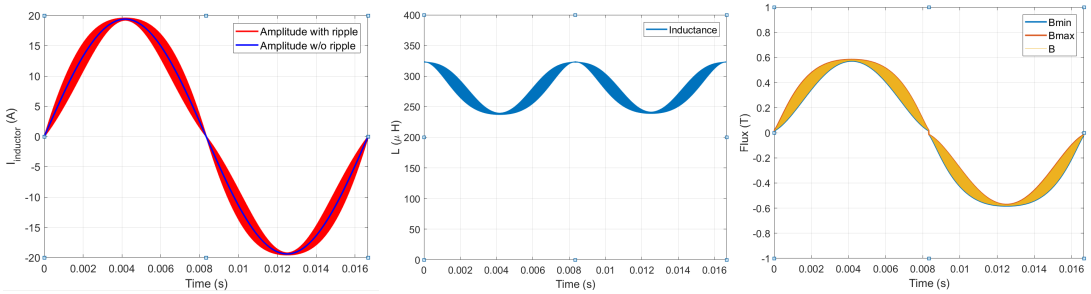
where $l_e$ is the magnetic path of the toroid core. $a_1$, $b_1$, $c_1$, $d_1$, $e_1$, $f_1$, $a_0$, $b_0$, $c_0$, $a_2$, $b_2$, and $c_2$ are denoted as the magnetic material coefficients from the datasheet. $T$ is the temperature of the core during the operation. Therefore, the inductance function is obtained as,

$$L(t) = \left|\frac{4\pi\mu(t)A_{et}n_{toroid}^2}{l_e}\right| \tag{2.34}$$

The inductor current discretization leads to two sets of sampling data: the maximum current and the minimum current values in each switching cycle. Correspondingly, the inductance and the flux density discretization are obtained with two sets of data, where the dataset length is determined by the ratio between the switching frequency and the line frequency. It is worth mentioning that the flux density datasets can be re-configured into two sets using the averaging model: the line frequency set and the switching frequency set. In Fig. 2-16, the inductor current waveforms, inductance, and flux density variations are obtained using the dynamic ripple-based estimation. In this computation example, the core is selected as 0058725A2 High Flux with 40 turns of AWG#14 Litz wire. The initial static inductance is taken to be 300 $\mu H$, assuming $\frac{V_{inm}}{V_{DC}} \geq 0.5$.

As seen in Fig. 2-16, the inductance variation trajectory moves across the desired static inductance with the double line frequency, which confirms the functionality of the proper inductor design. It is observed that the dynamic inductance difference can be up to 23% of the static value, which is helpful in defining a reasonable allowance in the design phase. Furthermore, the flux density behavior and the hysteresis loss can be fully examined using the

computed waveforms. Note that the waveform envelopes are formed by the maximum and minimum flux density values, as shown in blue and red in Fig. 2-16 (c).




(a) (b) (c)

Fig. 2-16. The computed variations over one line cycle from the proposed algorithm: (a) the inductor current waveform comparisons between with ripple and without ripple; (b) the inductance variation; (c) the high-frequency flux density $B_{high}$ variation.

It is worth mentioning that the proposed model is applicable to the cases where there is no air gap inside the inductor core, regardless of the PFC operation modes (CCM, DCM, or CRM). For the CRM operation, the additional design variable, the switching frequency, can be incorporated into the proposed model, which can be useful in the CRM PFC design and loss breakdown.

### 2. 4. 3 Loss Breakdown

The realistic inductor model can be utilized to better estimate power loss and examine the required inductance value. The total core loss in the inductor can be divided into the line frequency and switching frequency components, based on the computed flux density datasets. The core loss density is a function of maximum AC flux swing, effective volume, and operating frequency. The empirical coefficients ($A$, $\alpha$, $\beta$) and effective core volume can be obtained from core loss charts, datasheets and the curve fit loss equation. Thus, the core loss is expressed as,

$$P_{core} = \sum_{k=1,2,\dots 2f_s} V_{tor} A(\Delta B_{high,k})^{\alpha} f_s^{\beta} + V_{tor} A(|B_{line}|_{max})^{\alpha} f_l^{\beta} \quad (2.35)$$

where, $V_{tor}$ is the effective volume of the toroid core. $A, \alpha$, and $\beta$ are the empirical coefficients provided by the core manufactures. The switching frequency component is a summation of losses over all the switching cycles in one line period. The high frequency flux density difference $\Delta B_{high}$ at the $k^{th}$switching cycle is expressed in the following equation, which is the magnitude of the switching frequency flux density function over one switching cycle.

$$\Delta B_{high,k} = B_{max,k^{th}} - B_{min,k^{th}} \tag{2.36}$$

where $B_{max,k^{th}}$ and $B_{min,k^{th}}$ are denoted as the $k^{th}$ switching cycle maximum and minimum flux density caused by the switching operation in one line cycle. Furthermore, the winding loss can be calculated considering the current ripple. Similarly, the winding loss is divided into two components: DC loss and AC ripple loss, which is expressed as,

$$R_{winding} = I_{rms}^2 R_{DC} + < I_{ripple}^2 > R_{AC} \tag{2.37}$$

where $< I_{ripple}^2 >$ is the average value of the ripples. $R_{AC}$ is obtained using the simplified 1-D Dowell equation [75] to estimate the proximity effect, which is given by,

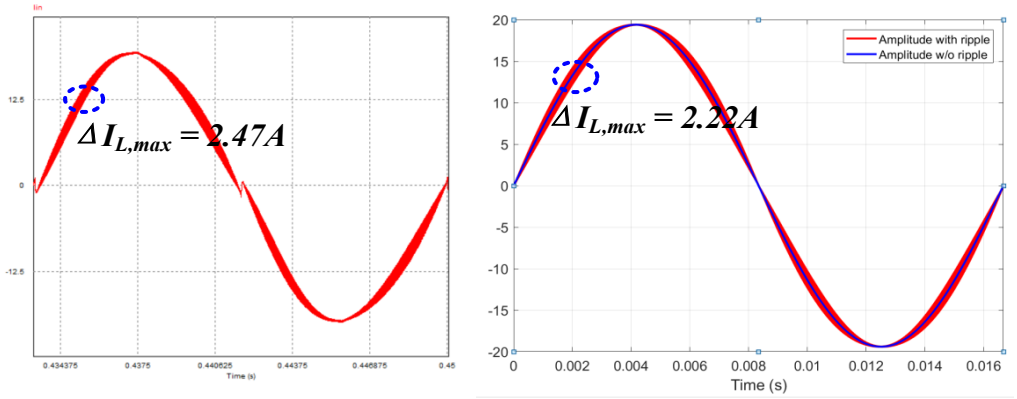
$$R_{AC} = \frac{\pi^2 \omega^2 \mu_o^2 N^2 {n_s}^2 d_c^6}{768 \rho_c^2 b_c^2} R_{DC} \tag{2.38}$$

where $N$ is the number of turns, $n_s$ is the number of strands in the Litz wire, $d_c$ is the diameter of a single strand, $\rho_c$ is the resistivity of the copper, and $b_c$ is the breadth of the core. Compared to the conventional loss estimation for a toroid core-based inductor, the proposed method is more accurate as it involves the dynamic computation of the current ripple, the high frequency and line frequency difference, and the corresponding variations in the magnetic materials.

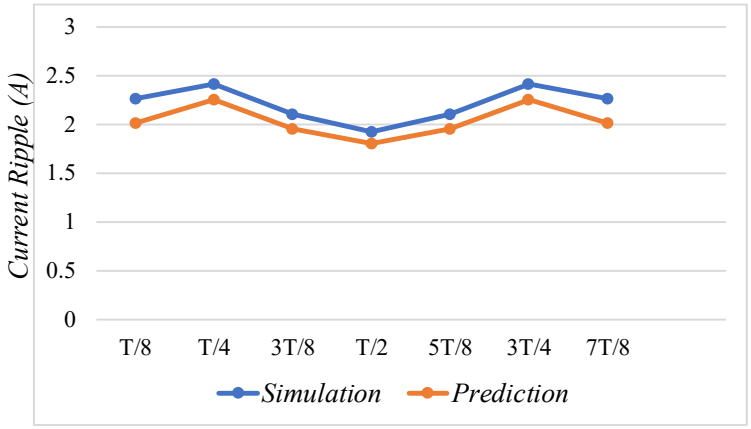
Therefore, a comprehensive inductor loss estimation algorithm is proposed using the predicted real-time current waveforms and material properties. The duty cycle function is computed from the feedback loop. The current reference $I_{ref}$ is compared with the estimated current with the predefined error allowance, which forms the current ripple trajectory.

2. 4. 4 Simulation Verification

The simulation verification is conducted to examine the accuracy of the ripple estimation. Note that the zero crossing distortion, which was not considered in the computation model, is observed in the simulation. However, the simulation results and the theoretical estimations are in good agreement, displaying a 10% of current ripple error, as shown in the following figure. Note that this error could arise from the constant inductance in the simulation.




(a) (b)




(c)

Fig. 2-17. Comparison of the current waveforms in the PSIM simulation result and the prediction: (a) the simulated inductor waveform; (b) the predicted inductor waveform; (c) comparison of the current ripples.

## *2. 5 Design Details*

The totem-pole PFC rectifier requires one boost inductor, one set of DC link capacitors and four GaN MOSFETs. Apart from the power stage components, a set of three sensors (one for line voltages, one for line current, one for DC link voltage) along with the sensing circuits is required. The converter specifications are listed in Table 2-1. The minimum DC link voltage needs to be greater than the line-line peak voltage corresponding to maximum AC input voltage, which is fundamentally required by the Boost-type PFC rectifier. In this design, the DC link voltage is selected as 400V, considering cost-effectiveness, efficiency and flat gain characteristics in the DC-DC stage.

Table 2-1. The PFC stage design specifications.

| Items | Specifications |
|---|---|
| Input | Line frequency: 50~60Hz<br>Single-phase voltage source; 85~265Vrms |
| Output | DC link voltage: 400V |
| Nominal power | 3.7kW (at 240Vrms input) |
| Operation modes | G2V and V2G |
| Topology | Totem-pole PFC, CCM |
| Efficiency | >98% |

The DC link capacitor needs to be large enough to suppress the line-frequency voltage ripple. On the other hand, the capacitor needs to store enough energy to maintain a minimum DC link voltage value over the hold-up time (i.e., 10ms). Assume the output voltage and current waveforms are in phase. Thus, the capacitance value can be expressed concerning the ripple requirement ($\Delta V = 5\%$) and hold up time ($t_{hold}$) [76],

$$C_o = \left\{ \frac{P_{o,max}}{\Delta V 2\pi f_{line} V_{o,min}}, \frac{2P_{o,max} t_{hold}}{V_{o,max}^2 - V_{o,min}^2} \right\}_{max} \quad (2.39)$$

Therefore, the desired DC link capacitor value is calculated as ~1000μF. In this work, two 1000μF/350V aluminum capacitors are connected in series to meet the maximum voltage requirement. Two groups of the series-connected capacitor branch are connected in parallel to achieve the desired value.

Considering the trade-off among the power loss, cost-effectiveness, operation performance (*di/dt, dv/dt*), and footprint size, the GaN Systems GS66516T is selected for the high frequency and line frequency switches; this device has a top cooling pad feature for the heat dissipation. A complete list of the components selected for the PFC stage, with the brief specifications, is given in Table 2-2.

Table 2-2. Summary of the component selection in the PFC stage.

| Component | Part No. | Quantity | Remarks |
|---|---|---|---|
| Fast MOSFET | GS66516T | 2 | High-frequency switch |
| Slow MOSFET | GS66516T | 2 | Line-frequency switch |
| DC link capacitor | LLS2V102MELC | 4 | PFC output capacitor |
| Current sensor IC | ACS780LLRTR | 1 | Hall-based IC |
| Zener diode | 1SMA12AT3G | 6 | Protection from voltage surge |
| Chip inductor | MLP2012SR82T | 10 | 820nH; filtering purpose |
| Toroid core | 0058725A2 | 1 | Inductor core |

Power losses in the PFC stage are mainly composed of boost inductor loss (magnetic core loss and winding loss), ESR loss in DC link capacitors, and semiconductor loss, which includes

switching and conduction loss in MOSFETs. In this work, the loss breakdown is conducted at full power rating.

### 2. 5. 1 DC Link Capacitor Loss

It is clear that instantaneous input power varies between 0 and $V_{in}I_{in}$ with twice the line cycle frequency i.e. 120 Hz. Thus, the output current ripple, which can be derived from the power balance equation, also has twice the line cycle frequency. The output ripple in the DC output side essentially leads to the capacitor loss, which is determined by the RMS value of the ripple current through the DC link capacitor and the ESR of the capacitor. It can be expressed as follows,

$$I_{ripple} = DI_A - \frac{V_{DC}}{R} = \frac{P_{avg}}{V_{DC}} cos(2\omega_{line}t) \tag{2.40}$$

$$P_{ESR} = {I_{ripple,RMS}}^2 \cdot ESR = \frac{P_{avg}^2}{2V_{DC}^2} \times ESR \tag{2.41}$$

$$tan\,\delta = \frac{ESR}{X_c} = 2\pi fC \times ESR \tag{2.42}$$

Therefore, the total capacitor loss and its related specifications are listed in Table 2-3.

Table 2-3. DC link capacitor specification.

| Part No. | LLS2V102MELC |
|---|---|
| Tan $\delta$ | 0.15 |
| ESR (Ω) | 0.2 |
| $P_{cap}$ (W) | 13.8 |

A detailed comparison between the film capacitors and the aluminum capacitors is conducted for one modular design. As shown in the following table, the film capacitors have

much more volume but negligible efficiency improvement. Thus, the aluminum capacitors are utilized in this system.

Table 2-4. Detailed comparison between the film capacitors and the aluminum capacitors.

| Part No. | LLS2V102MELC | DCP4I061509JD4KSSD |
|---|---|---|
| Number per set | 4 | 6 |
| Effective ESR (Ω) | 0.2 | 0.024 |
| Effective capacitance (μF) | 1000 | 900 |
| Volume ($cm^3$) | 245 | 1000 |
| Estimated loss (W) | 13.8 | 2.1 (0.28% efficiency improvement) |

2. 5. 2 Semiconductor Loss

The conduction loss $P_{cond}$ can be obtained from the RMS value of the inductor current based on the dynamic ripple-based current estimation. Note that for each operation modes, only one fast MOSFET and one slow MSOFET are conducting. The conduction loss is given by the following formula, where the ON resistance $R_{ds\_on}$ is estimated from the datasheet,

$$P_{cond} = {I_{RMS}}^2 R_{ds\_on} \tag{2.43}$$

The total conduction loss is calculated to be 22W. For the switching loss, since the converter operates in CCM, both turn-on and turn-off losses of two fast switches need to be considered. It is worth noting that the rising time $t_r$ and fall time $t_f$ of the MOSFET need to be recalculated based on the testing environment; they cannot be taken directly from the datasheet [77]. For the turn-on process of the GaN MOSFET, the relationship between $V_{ds}$, $V_{gs}$ and $I_d$ is illustrated in Fig. 2-18.

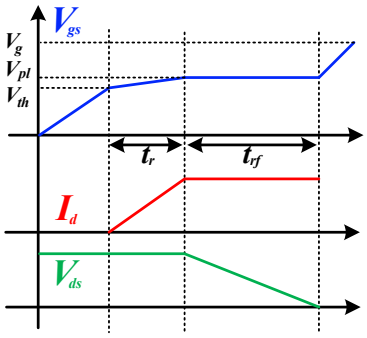



Fig. 2-18. The relationship between $V_{ds}$, $V_{gs}$ and $I_d$ during the turn-on process.

Apart from the rising time during the turn-on process, there is an additional time interval $t_{rf}$ for the discharging of the output capacitor from $V_{DC}$ to 0. Considering the parasitic capacitors of the MOSFET, $t_r$ and $t_{rf}$ can be represented as,

$$t_r = C_{in}R_g ln\left(\frac{V_g - V_{th}}{V_g - V_{pl}}\right), t_{rf} = \frac{C_{gd}R_g V_{DC}}{V_g - V_{pl}} \tag{2.44}$$

where $C_{in}$ is the input capacitor of the switch; $R_g$ is the gate resistance; $V_{pl}$ represents the Miller plateau voltage and $V_{th}$ is the threshold voltage. Similarly, the fall time $t_f$ and the extra time interval $t_{fr}$ for the charging output capacitor can be expressed as,

$$t_f = C_{in}R_g ln\left(\frac{V_{pl}}{V_{th}}\right), t_{fr} = \frac{C_{gd}R_g V_{DC}}{V_{pl}} \tag{2.45}$$

Apart from the rising and falling times, the power loss caused by the output capacitor needs to be considered. The switching loss per fast switch can be expressed as,

$$P_{sw} = 0.5 I_d V_{DC} f_s\left(t_r + t_{rf} + t_f + t_{fr}\right) + 0.5 C_{oss} {V_{ds}}^2 f_s \tag{2.46}$$

Therefore, the total switching loss is calculated to be 20W. The loss breakdown at the peak power is represented using a pie chart in Fig. 2-19. The overall efficiency is 98.5% at full power.

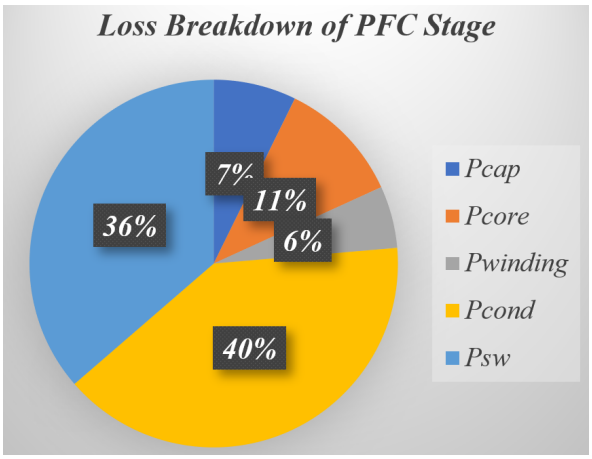



Fig. 2-19. Loss breakdown for the PFC stage.

2. 5. 3 Robust Gate Driver

GaN devices have the small gate charge and low junction capacitance, which can translate into high switching speed. This brings many challenges in the gate loop design. The $dv/dt$ is coupled through the parasitic capacitance between the switching node and the ground plane, which can lead to mis-trigger of the gate signals. Moreover, the $di/dt$ introduces the voltage drop on the common source inductance, which affects the turn-on and turn-off processes. These factors can significantly affect the normal operation of the converter. Hence, a robust gate driver design with high noise immunity is essential in a GaN-based charging system.

A +6/-3 V gate control voltage logic is selected, as shown in Fig. 2-20. The -3 V gate voltage is established by the Zener diode, which reduces the false triggering at the gate terminal. The gate loop routing is placed with the minimum distance, such that the induced parasitic inductance can be suppressed. For the gate drive return at the bottom side, the creation of a Kelvin connection to the source is recommended [78]. Lower risk of cross-conduction and gate oscillation, and faster turn-off (lower switching loss) can be achieved through a robust gate driver design.

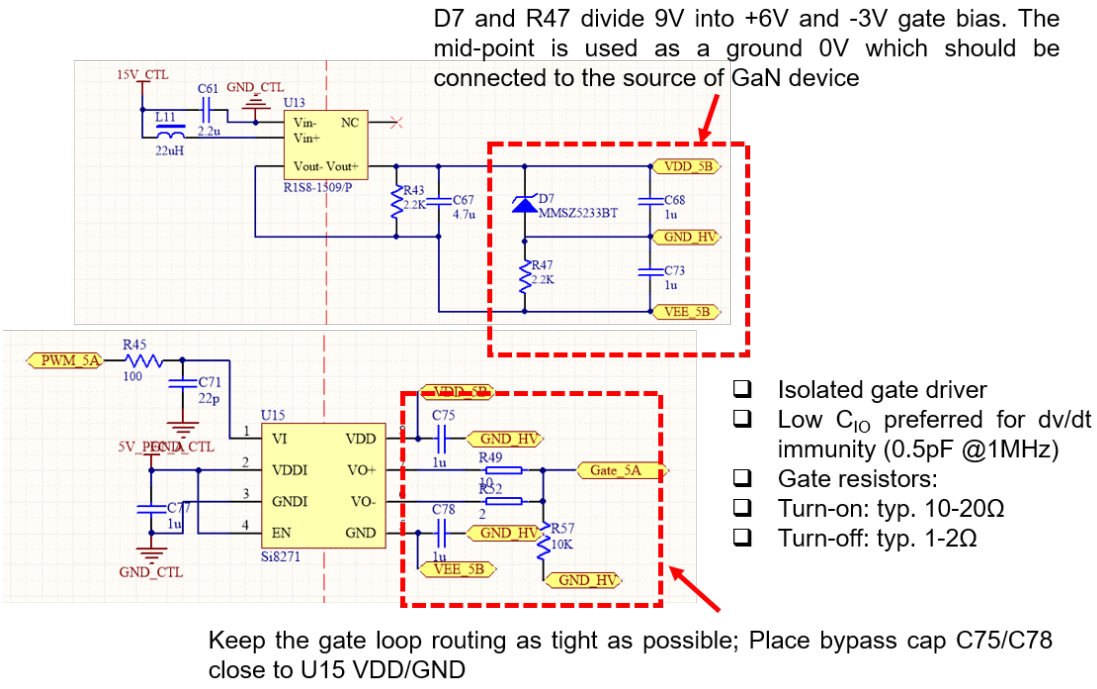



Fig. 2-20. The gate driver schematic.

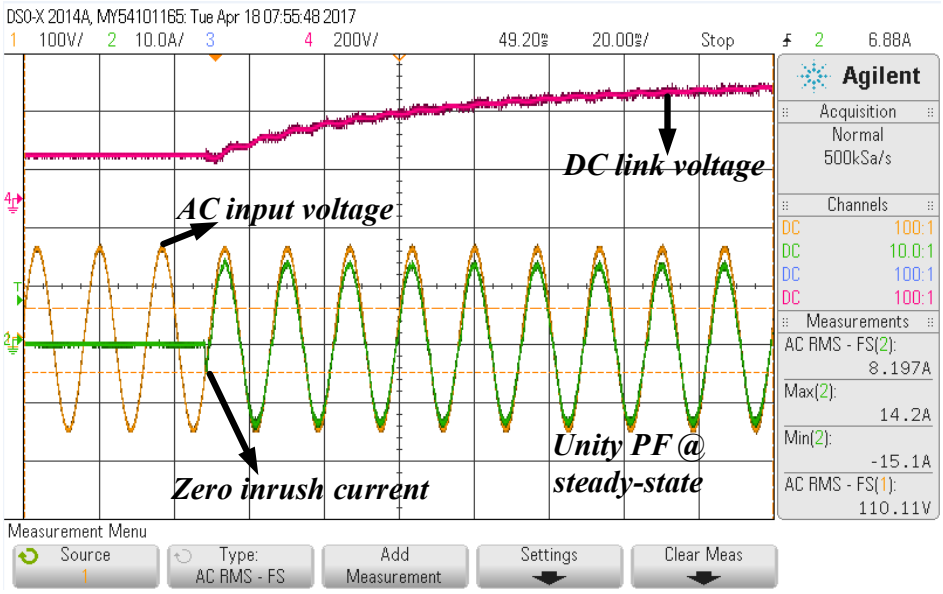
## *2. 6 Experimental Verification*

### 2. 6. 1 Minimum Inrush Current

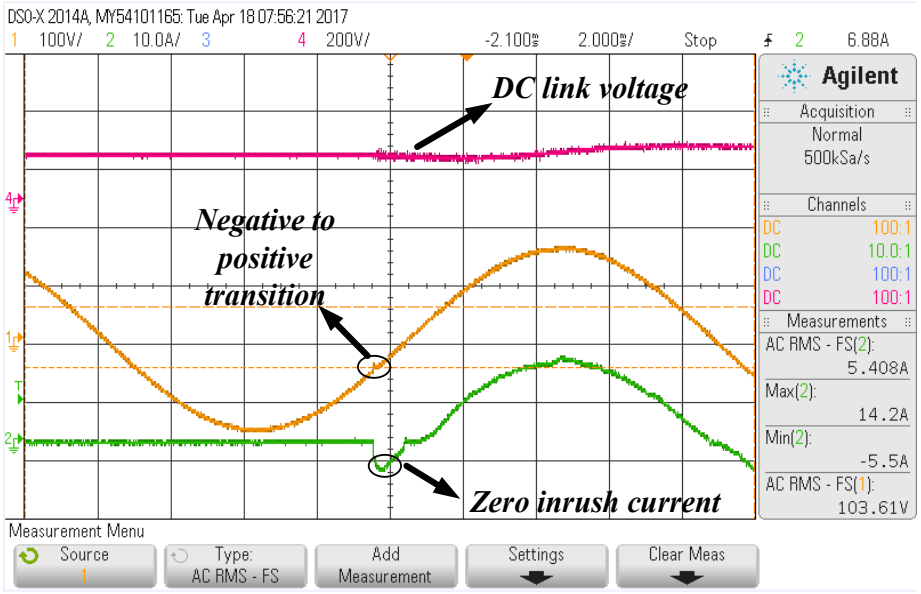
In order to validate the proposed start-up algorithm for minimizing the inrush current in the 100kHz PFC rectifier, a laboratory prototype is built and tested. The control algorithm is digitally implemented in the TI Digital Signal Processor (DSP).

The PFC converter waveforms at 100kHz switching frequency are shown in Fig. 2-18, which indicates an efficiency of 98%, input current THD of 4.7% and power factor of 0.996 during steady-state operation. The start-up waveforms of the PFC are shown in Fig. 2-21 (a) and Fig. 2-21 (b). At a rated power (1.5kW) operation, the first inrush occurring during the turn-on of uncontrolled diode bridge circuit is limited to 8A; this is determined by the input AC voltage, output capacitor and load resistance. The most significant inrush (i.e. the third inrush) occurring during the turn-on of control is non-existent while the transient happens near the zero crossing from negative to positive half-cycle. On the other hand, Fig. 2-21 (c)

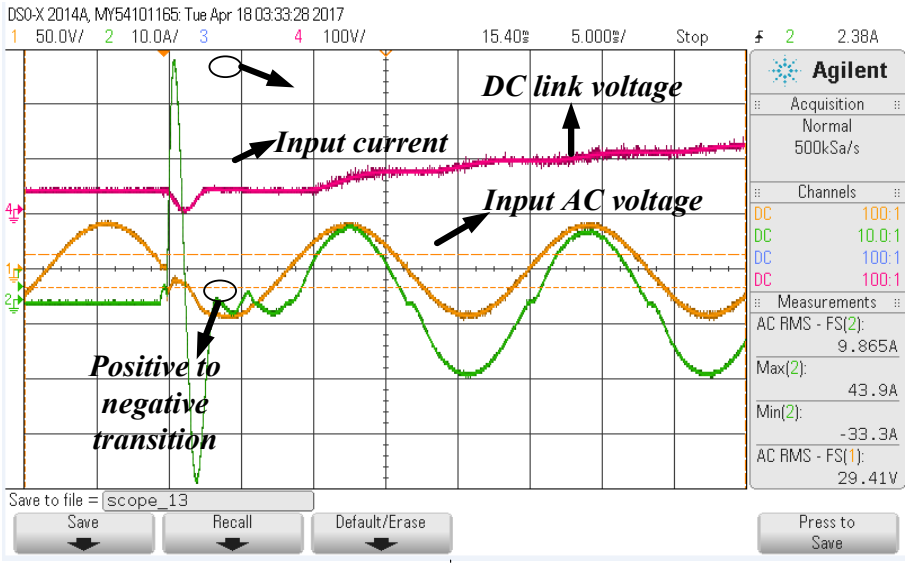
demonstrates a higher start-up current of 40A, if the transition is made at crossing from positive to negative half-cycle, which maintains good agreement with the analytical prediction.




(a)




(b)




(c)

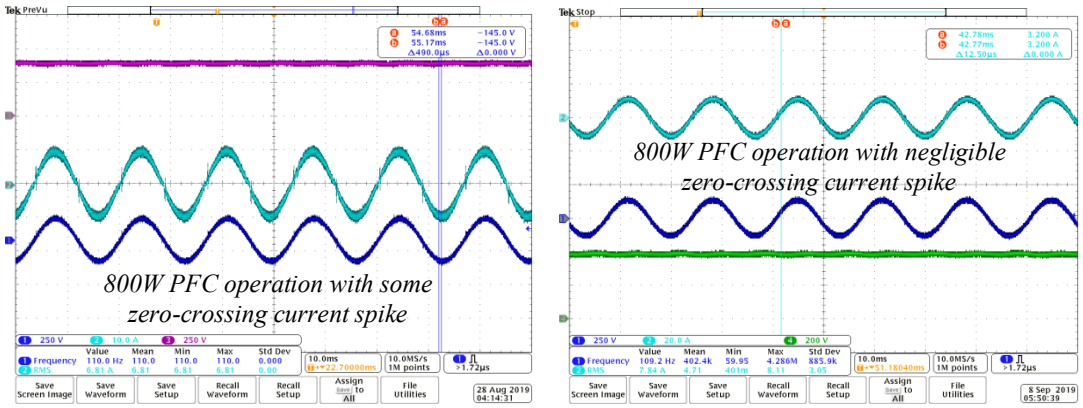
Fig. 2-21. The experimental waveforms: (a) PFC start-up waveform at 1.5kW load, $V_{in}$=120V 60Hz AC RMS, $V_{DC}$(ref)=400V; (b) the transition of the converter from uncontrolled to controlled PFC action during negative to positive zero crossing; (c) PFC start-up waveform while the PFC control is engaged during positive to negative zero crossing of input voltage; the inrush current goes as high as 40A.

In the overall event sequence of the PFC start-up, the maximum current inrush can potentially occur during the transition of converter operation from passive diode-bridge to actively controlled PFC stage. By properly adjusting the time at which the PFC controller is engaged in the start-up process, the inrush current can be made zero. The proposed approach is verified in the experiment, which exhibits a power factor >0.996 in the steady state and 100 ms start-up time with zero inrush current during the transition to PFC operation.

### 2. 6. 2 Zero-Crossing Current Spike Mitigation

The soft-transition-based algorithm is implemented in the controller, considering the switching characteristics of the GaN device, the junction capacitor of MOSFETs $C_{oss}$ in high frequency GaN MOSFETs, and digital delays. Since GaN devices are utilized in the system,

the reverse-recovery current of the switch is close to zero. The duty ratio needs to be adjusted gradually according to the current waveform. The following figures show the comparison between the PFC steady-state waveforms with and without the soft transition implementation. It can be seen from Fig. 2-22 that the zero-crossing current spike is fully eliminated with the implementation of the soft transition technique.




(a) (b)

Fig. 2-22. The experimental waveforms regarding the zero-crossing current distortion: (a) the PFC controller without soft transition algorithm; (b) the PFC controller with soft transition algorithm.

2. 6. 3 Steady-State Operation

First, the dual-pulse-test (DPT) is performed to verify the switching performance of the GaN device. Two pulses have the ON time of $16\mu s$ and $5\mu s$, respectively, such that the turn-on and turn-off characteristics can be captured. It is observed that the overshoot voltage can be up to 440V with the 400VDC input and 15A turn-on current, which is acceptable for a 650V device. Moreover, the turn-on speed of the GaN device is measured as 80V/ns. Thus, the gate driver exhibits good noise immunity. As shown in the Fig. 2-23, the overshoot voltage is suppressed and there is low ringing during the switching intervals, which validates the hardware design of the gate loop and power loop.

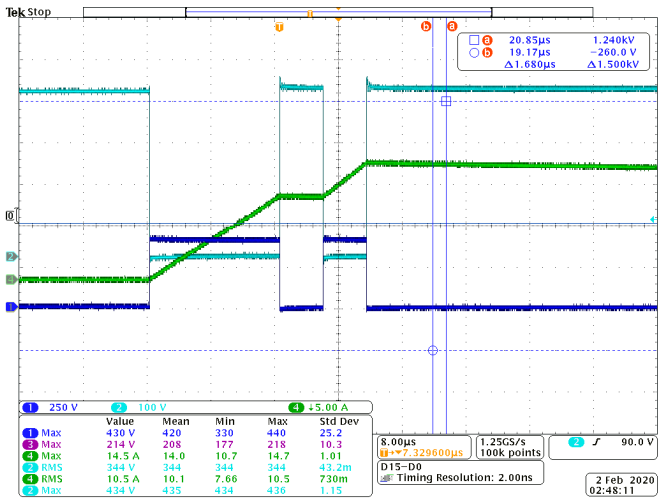



Fig. 2-23. The DPT waveforms for the PFC GaN switch.

The steady-state PFC operation waveforms are illustrated in Fig. 2-24. The four-channel power analyzer PA3000 from Tektronix is utilized for the data acquisition. At 2.8kW output power, the efficiency is measured as 98.5% and the power factor is 0.995. In addition, the total harmonic distortion (THD) is below 1%. It is confirmed that the control loop is well designed.

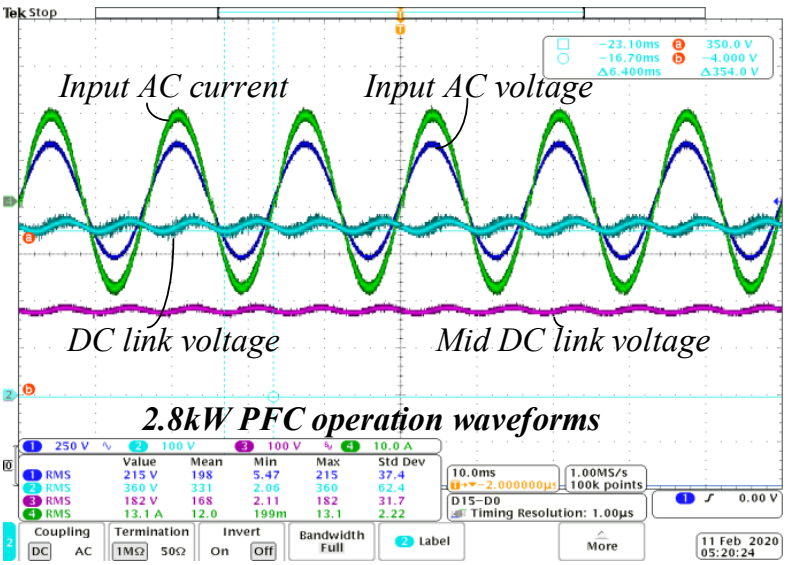



Fig. 2-24. The steady-state PFC operation waveforms at 2.8kW output power in G2V mode. The input voltage is 240V AC.

As shown in the figure, the zero-crossing current distortion is minimized using the soft transition technique. The double line frequency DC voltage ripple is observed in the figure, where the amplitude is in good agreement with the predicted values (within 5%). Moreover, the inverter operation of the totem-pole PFC rectifier is verified experimentally. As can be seen from Fig. 2-25, the V2G mode is tested at 2kW. In this case, the peak efficiency is 98.4%. The measured efficiency curves and the power factor are shown in Fig. 2-26. Note that higher efficiency is achieved with the 240V AC input voltage.

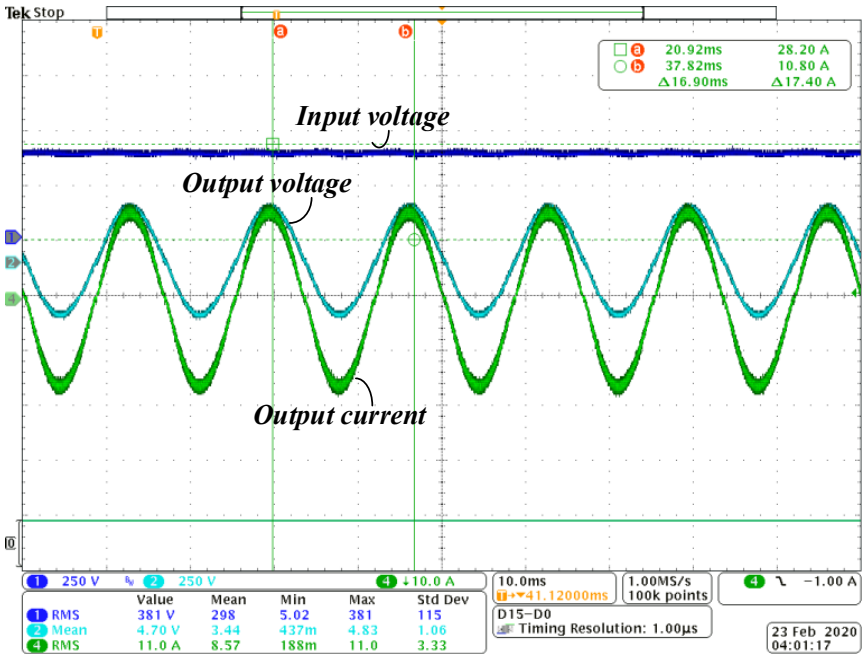



Fig. 2-25. The steady-state PFC operation waveforms at 2kW output power in V2G mode.

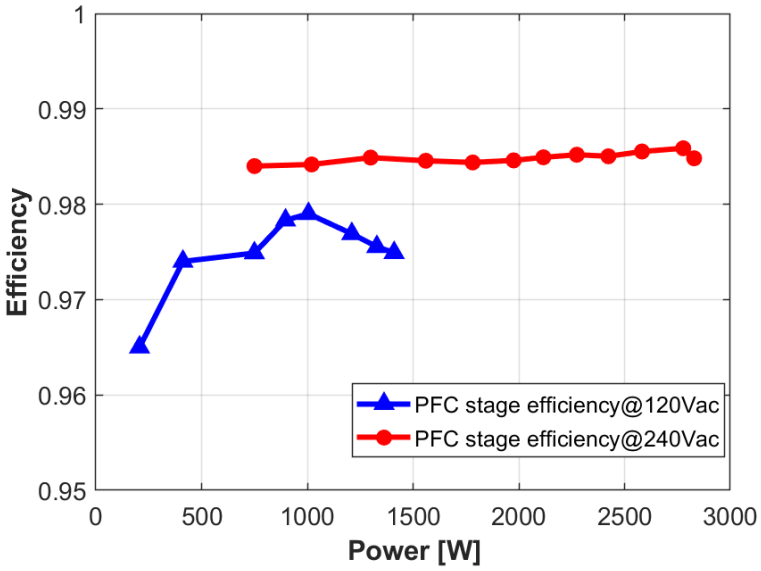



Fig. 2-26. The measured efficiency curves for different line voltages.

## *2. 7 Summary*

This chapter introduces the operation modes and control of a GaN-based totem-pole PFC rectifier. An integrated control strategy to resolve the zero-crossing distortion is proposed and analyzed. This strategy involves a soft transition-based algorithm with the closed-loop control, which considers the switch characteristics, junction capacitors, abrupt duty ratio changes in high-frequency MOSFETs, and digital delays. To validate the proposed integrated control method, a simulation has been conducted to examine the THD, voltage ripple and power factor correction. It is observed that tight input current and output voltage regulations are achieved, with the power factor maintained at a level greater than 0.99 and the THD lower than 5%. Furthermore, a start-up control to obtain the minimum inrush current is proposed in this work. It is mathematically proved that the inrush current can be made zero if the PFC action control is engaged at the negative-to-positive zero crossing of the input AC voltage. The proposed approach is verified using a 1.5kW experimental prototype of the PFC rectifier at 100kHz switching frequency, which exhibits a fast start-up time (100ms) with zero inrush current during the transition to PFC operation.

Apart from the control, detailed practical implementation is considered. A comprehensive design for DM filters is provided to achieve the required noise spectrum attenuation. The effectiveness of the proposed two-stage DM filters is verified through a simulation. Consequently, the EMI stage components along with the boost inductors can be optimized together considering the total volume, power loss, and ripple requirement. Moreover, the gate loop is designed to ensure the noise immunity. In order to obtain an accurate estimation of boost inductance and its losses, a dynamic ripple-based estimation method is proposed considering the variation of material permeability, GaN device switching characteristics, and operating temperature. Based on the ripple model, a systematic loss breakdown is conducted, covering boost inductor loss, ESR loss in DC link capacitors, and semiconductor loss. Robust gate driver design is discussed. It is experimentally reported that at 2.8kW output power, the efficiency is measured as 98.5% and the power factor is 0.995. In addition, the total harmonic distortion (THD) is below 1%.

# Chapter 3 : Integrated Transformer Design and Optimization

Magnetic integration can be achieved through multi-winding transformers or coupled inductors to achieve the electrical integration with fewer component counts and capability of providing additional operation modes [79], [80]. It is a key technology part to integrate the OBC with APM and enable the simultaneous charging of both HV and LV batteries. Multi-winding transformers have been studied in the literatures [81]–[83]. A split-winding structure is proposed in [84] to realize the multi-port integration, in which the minimum leakage inductance is calculated from a mathematical model. Compared with simply interleaving primary and secondary windings in two winding transformers, this method is able to realize the traversal of all the possible configurations while maintaining the low winding losses. However, in this design, the leakage inductor cannot be large enough to account for the required shim inductance in phase-shifted based converter (i.e., dual-active-bridge converter) and resonant converter (i.e., CLLC converter). Moreover, since the system is designed for low power applications, the analysis on parasitic capacitances with the interleaved winding structure is out of the scope.

Research has also been conducted to model the transformers using magnetic equivalent circuit (MEC) [85]–[87]. In [85], the derivation for the leakage permeances is achieved in a core-type transformer using MEC. However, this flux model is highly structure dependent. For optimization purposes, an integrated transformer with leakage inductance is established in [86] using the flux model. However, only reluctance of the air gap is taken into consideration and hence, neglecting the leakage flux in the air decreases the model accuracy. Besides, the flux model in [87] using the magnetomotive force (MMF) variation method and the stored energy in the magnetic shunt provides a calculation methodology for the leakage inductance of the transformer with a magnetic shunt. In sum, some previous modeling methods use well-established FEA-based simulations [88], [89] and MEC to determine the leakage inductances

[90]–[92]. However, the tradeoffs between losses, weight and volume were not fully considered in those studies. This makes the optimal design of a transformer challenging, and hence, solidifies the necessity for multi-objective optimization [83], [93], [94]. In [93], a systematic approach to minimize the losses and footprint area is proposed as a universal design tool for PCB-integrated inductors and transformers. However, this approach is not applicable to the integrated transformer with a three-winding structure. Aiming at designing the optimal transformer for medium-frequency applications, a genetic-algorithm-based methodology is implemented in [83], which not only meets all the design requirements, but also is fast and accurate. However, the optimization constraints become much different in cases of high-frequency applications. The work in [94] proposes the particle swarm method to optimize the high-frequency transformer with minimum power loss and leakage inductance. However, the influences of the air gap on the magnetomotive force (MMF) distribution, leakage inductance, and core loss are not carefully analyzed.

### *3. 1 The Proposed Litz-Wire Based Single-Phase Integrated Transformers*

In this work, a new configuration of the integrated transformer is proposed to achieve the reduction of the weight and volume, the mitigation of the magnetic component losses, and low parasitic capacitance. Meanwhile, the integrated transformer enables the desired functionality of simultaneous charging and power flow management among three ports. The EE-shape core structure is utilized since it provides enough space for the three winding configurations with the flexibility to shape the leakage flux path [95]. Two large leakage inductances are integrated into the three-winding transformer using Litz wire to reduce the converter size. In addition, the Litz wire offers excellent flexibility with different kinds of terminal configurations, where the terminals in each side can either be parallelly connected, star-connected or delta-connected. Moreover, galvanic isolation is achieved by the transformer in a single-phase system. The diagram of a single-phase integrated transformer [35] using EE-shape core is illustrated in Fig.

3-1. In this design, the primary winding is located on one side of the EE cores while the secondary winding is placed on the other side. The tertiary winding is located above the secondary winding. The air gap between primary and secondary windings is utilized to ensure appropriate leakage inductances.

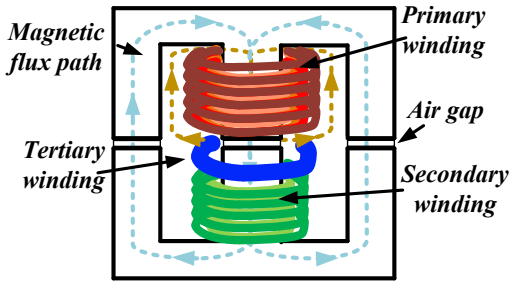



Fig. 3-1. The diagram of a single-phase integrated transformer using EE-shape core.

As shown in Fig. 3-1, the trajectory of the leakage flux path substantially contributes to the leakage inductance. The air gap between the central legs of two E cores and the gaps among three windings can be adjusted to precisely set the leakage and magnetizing inductances. It is important to mention that the distance of the gap between two E cores has less influence on the leakage inductance in comparison to the gaps between windings. In addition, the air gap between the central legs significantly reduces the risk of saturation while the gaps among windings help enhance the insulation safety. Moreover, three sets of single-phase integrated transformer can be implemented as a three-phase transformer using the delta or star configuration.

### 3. 1. 1 Transformer Core Loss Model

*1) Conventional Core Loss Model*

Transformer losses can be categorized into core and winding losses [96]. The high-frequency resonant tank current excites the AC sinusoidal flux passing through the core and therefore results in core loss. In common practice, the area-related Steinmetz equation [97] with

empirical coefficients provided by the magnetic manufactures is used to evaluate the core loss as follows,

$$P_{core} = \sum_{n=1}^{\infty} V_n A(\Delta B)^{\alpha} f_s^{\beta} \ , \sum V_i = V_c \tag{3.1}$$

where $V_c$ is the effective volume of the core. Given each infinitesimally small piece with volume $V_n$, the total core loss is a summation of the core loss of each small piece. $\Delta B$ is the AC flux variation which is defined as $\Delta B = \frac{B_{max} - B_{min}}{2}$, where $B_{max}$ and $B_{min}$ are the maximum and minimum flux density of each piece. $A, \alpha$, and $\beta$ are the empirical coefficients provided by the core manufactures for different material. $f_s$ is the switching frequency.

This conventional model still has the following limitations: (a) the computation time is long; and (b) the Steinmetz equation is based on sinusoidal excitation, which may not hold true in reality. Thus, a more accurate and simplified core loss model needs to be established.

*2) Proposed Transformer Core Loss Model*

Considering the symmetrical structure of the integrated transformer, a novel transformer core loss model as shown in Fig. 3-2 is proposed to achieve more accurate results using magnetic equivalent circuit. This core loss model includes the leakage flux path from both windings and air gap, meanwhile splits the location of magnetic flux path from the side legs and the center leg.

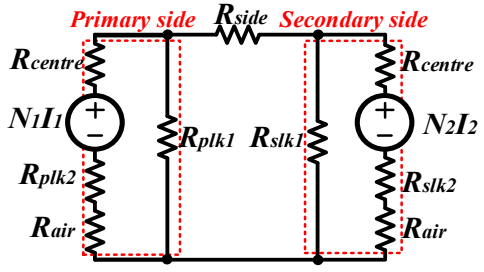



Fig. 3-2. The equivalent magnetic circuit of the integrated transformer.

In Fig. 3-2, $N_1 I_1$ and $N_2 I_2$ denote the magnetomotive forces (MMFs) across the primary and secondary windings, respectively. $R_{centre}$ represents the reluctance of the center leg, $R_{side}$

denotes the equivalent reluctance of two side legs. Meanwhile $R_{air}$ is the air gap reluctance, $R_{plki}$ and $R_{slki}$ denote the primary and secondary leakage inductances, respectively, which are distributed among the center leg, excitations and air gaps. Due to the symmetrical geometry of the E core, the equivalent model is symmetric as well.

A further reduced magnetic circuit using superposition is synthesized in Fig. 3-3. There are some assumptions to simplify the computation: (a) since the leakage inductances across the excitation and the air gap are very small (<0.01% obtained from electromagnetic simulation), they are lumped with the leakage inductance across the center leg and $R_{side}$ is added into $R_{centre}$; and (b) $R_{centre}$ stays unchanged in the ideal and proposed model. It is worthy to mention that sum of MMFs associated with $N_1 I_1$ and $N_2 I_2$ is nonzero as shown in Eq. (4.2), since this is not an ideal transformer.

$$F = N_1 I_1 - N_2 I_2 = \emptyset_c (R_{centre} + R_{air}) // R_{plk} // R_{slk}' \tag{3.2}$$

$$R_{air} = \frac{l_g}{\mu_{air} A_c} \tag{3.3}$$

where $F$ represents the total MMF of the magnetic circuit; $\emptyset_c$ is the magnetic flux through the integrated transformer core; $R_{slk}'$ denotes the reflected secondary leakage reluctance; and $l_g$ is the length of air gap.

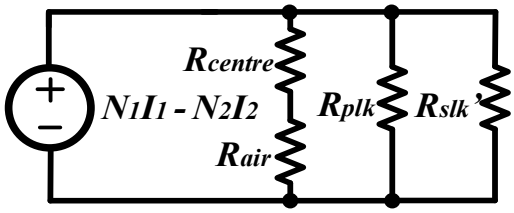



Fig. 3-3. The reduced magnetic circuit of the integrated transformer.

For an ideal transformer model, $R_{centre}$ can be obtained from Eq. (4.2), where the cross-sectional area $A_c$ is given in the datasheet. The maximum flux density $B$ is obtained from the volt-second balance. Note that the volt-second balance is not suitable for air-gapped or any non-ideal transformer model.

$$\begin{cases} \emptyset_{ideal} = \frac{N_1 I_1 - N_2 I_2}{R_{centre}} = BA_c,\ B = \frac{V\Delta T}{N_1 A_c} \\ R_{centre} = \frac{4nf_s(N_1 I_1 - N_2 I_2)}{V} \end{cases} \tag{3.4}$$

From the perspective of energy, the core, primary and secondary leakage inductances can be expressed as follows.

$$\begin{cases} \frac{1}{2} L_M I_M^2 = \frac{MMF^2}{R_{centre}} \\ \frac{1}{2} L_{plk} I_M^2 = \frac{MMF^2}{R_{plk}},\ \frac{1}{2} n^2 L_{slk} I_M^2 = \frac{MMF^2}{R_{slk'}} \end{cases} \tag{3.5}$$

Therefore, $\emptyset_c$ can be derived by substituting $R_{plk}$ and $R_{slk}{}'$ with their equivalent expressions, which would lead to the following equation,

$$\emptyset_c = \frac{L_{plk} + n^2 L_{slk}}{L_M} \frac{V}{4N_1 f_s} + \frac{A_c V}{4N_1 A_c f_s + \frac{lgV}{\mu_{air}(N_1 I_1 - N_2 I_2)}} \tag{3.6}$$

where $L_M$, $L_{plk}$ and $L_{slk}$ are the magnetizing, primary leakage and secondary leakage inductances, respectively.

Since $L_M$, $L_{plk}$ and $L_{slk}$ are the tuned known parameters from the design phase, $R_{plk}$ and $R_{slk}{}'$ can be obtained. $\emptyset_c$ can be calculated from Eq. (4.4) and the maximum flux density $B_{\max 0}$ with high accuracy is achieved in the proposed model. In fact, considering the square AC voltage excitation for the transformer, the real waveform of the magnetizing current is triangular. Since Steinmetz equation is more accurately applicable for a sinusoidal waveform, therefore an equivalent frequency for calculating the core loss using Steinmetz equation should be determined for a triangular waveform. This is derived using a method mentioned in [97] and presented as follows,

$$f_{eq} = \frac{1}{2{B_{max0}}^2 \pi^2} \int_0^{f_s} \left(\frac{dB}{dt}\right)^2 dt = \frac{8f_s}{\pi^2} \tag{3.7}$$

Therefore, a more accurate core loss result for the integrated transformer is achieved as,

$$P_{core} = V_c A (B_{max0})^{\alpha} f_{eq}^{\beta} \tag{3.8}$$

3. 1. 2 Litz Wire Winding Loss Analyses

Various details need to be considered to get an accurate estimate of the winding loss. In the range of ~100kHz, the skin effect is negligible if the winding wire is suitably selected (suitable Litz wire or PCB winding design). However, the proximity effect takes a significant portion of the winding loss in such a frequency range, especially in TAB converters where the high frequency and high amplitude resonant current flows through the transformer windings.

There are two aspects of proximity effect in windings: strand level and bundle level. The bundle level effect is not related to the number and diameter of a single strand but instead is only associated with the twisted pattern when constructing the Litz wire. This part of the effect has already been well considered during manufacturing and thus is not within the scope of this paper. On the other hand, the strand level effect is a key design consideration for wire selection in the high-frequency transformer design, since, in the strand level, proximity effect dominates the skin effect [41]. To estimate the proximity effect, the AC resistance of the winding can be determined using a simplified 1-D model [75]. The DC and AC losses can be expressed as follows, assuming $R_{DC}$ to be the DC resistance of the winding.

$$P_{winding.total.1D} = F_R I_{winding}^2 R_{DC} \tag{3.9}$$

$$F_R = \frac{R_{AC}}{R_{DC}} + 1 = \frac{\pi^2 \omega^2 \mu_0^2 N^2 {n_s}^2 d_c^6}{768 \rho_c^2 b_c^2} + 1 \tag{3.10}$$

where $N$ is the number of turns, $n_s$ is the number of strands in the Litz wire, $d_c$ is the diameter of a single strand, $\rho_c$ is the resistivity of the copper and $b_c$ is the breadth of the core.

Considering the gapped transformer structure, the external flux caused by the fringing field of air gaps would increase the eddy current effect inside the conductors. Hence, in addition to the skin effect loss and proximity effect loss, an additional power loss caused by the fringing field must be considered for gapped transformers [98]. The fringing effect can be quantified as the fringing flux factor [99], and other geometry parameters of the core, which contribute to the equivalent winding turns when calculating the winding loss.

$$FF = 1 + \frac{l_g}{\sqrt{A_c}} ln \frac{2G}{l_g} \tag{3.11}$$

where, $G$ is the window length of the core. Thus, the equivalent turns can be calculated using the fringing flux factor. The revised loss winding loss model is expressed as,

$$N_{new} = \sqrt{\frac{L_m l_g}{0.4\pi A_c FF 10^{-8}}} \tag{3.12}$$

$$P_{winding.total} = \left(\frac{\pi^2 \omega^2 \mu_o^2 N_{new}^2 {n_s}^2 d_c^6}{768 \rho_c^2 b_c^2} + 1\right) I_{winding}^2 R_{DC} \tag{3.13}$$

In general, using finer strands to construct the Litz wire leads to less eddy current and thus, less proximity effect losses [41]. However, there is a limitation to decrease the size of each strand because, with the decrease of strand diameter, the fraction of copper occupied in the window will decrease. Therefore, the DC resistance increases due to less total cross section area of the copper. Considering the tradeoffs between DC and AC losses, conductor size and type, there exists an optimum solution to the wire selection.

### 3. 1. 3 Optimal Design Process

There is always a trade-off among the magnetizing inductance $L_m$, leakage inductance $L_k$ and winding AC resistance $R_{AC}$. For instance, if the transformer windings are placed in a sandwich-type configuration, the coupling factor between primary and secondary windings is close to 1, which means they are well interleaved and the $R_{AC}$ is minimized. However, the $L_k$ is infinitesimally small under this condition, making it impossible to be utilized as a separate inductor. On the other hand, the winding location can be changed to adjust the $L_k$ and the $R_{AC}$. However, the $L_m$ would be affected if the windings are no longer placed around the center leg. Thus, a multi-objective problem is formulated to achieve the optimal design of the Litz-wire based transformer. The calculation of winding loss considers the proximity effect, as shown in Eq. (4.10). The geometry parameters of core determine the length of windings, core loss and weight. In general, the major calculations can be summarized as follows,

$$\begin{cases} B = \frac{\emptyset_c}{A_c} = \frac{L_{plk}+n^2L_{slk}}{L_M}\frac{V}{4N_1f_s} + \frac{V}{4N_1A_cf_s+\frac{lgV}{\mu_{air}(N_1I_1-N_2I_2)}} \\ f_{r_{G2V}} = \frac{1}{2\pi\sqrt{2L_{plk}C_1}}, f_{r_{V2G}} = \frac{1}{2\pi\sqrt{2L_{slk}C_2}} \\ n = \frac{N_1}{N_2} \\ P_{loss} = P_{core} + P_w \\ P_{core} = V_cA(B)^{\alpha}f_{eq}^{\beta} \\ P_w = \sum_{i=1}^{2} N_iP_{winding.total.i} \\ W_c = \rho_mV_c \\ \frac{N_1A_1+N_2A_2}{A_w} \leq \sigma \end{cases} \tag{3.14}$$

where, $V$ is the peak voltage for each switching cycle that can be obtained from simulation; $\rho_m$ is the mass density of core; $A_1$ and $A_2$ are the cross areas of primary and secondary conductors; and $\sigma$ is the maximum window factor, which is assumed 0.6 in this design.

The objective function is the total loss incurred in the transformer, which is the sum of winding and magnetic core loss. The constraints are imposed on the minimum window area requirement and maximum allowable flux density. The parameters to be selected in the optimization process are number of Litz strands, diameter of each conductor, breadth, window area and volume of the core. The optimization process yields the following results, as listed in Table 3-1.

Table 3-1. The computed parameters from the optimization process.

| Parameters | Resulted optimum value |
|---|---|
| Number of conductor strands | 780 |
| Diameter of each conductor (μm) | 60 |
| Effective core length (mm) | 61 |
| Effective core area ($mm^2$) | 600 |
| Core volume ($cm^3$) | 80 |
| Winding area ($mm^2$) | 400 |

It turns out that these required specifications for optimum solution match well with the selection of E65 core with R material, AWG12 Litz winding (700/40) and more importantly, achieve the lowest normalized loss with a relatively larger volume than some other solutions, as presented in Fig. 3-4. However, this cannot satisfy the window factor requirement considering additional high-current winding for LLC converter. Meanwhile, R material E65 core with AWG14 Litz winding (660/42) achieves second highest efficiency and can satisfy the window factor requirement. Although PQ50 core provides a solution with a smaller volume, prioritizing efficiency over volume for better thermal management makes E65, R-material, AWG14 (660/42) the final candidate in the design with a minimum sacrifice in volume. As can be seen in Fig. 3-4, the Pareto frontier is marked as dashed red line, which is a set of non-dominated optimal solutions with the tradeoffs in improving one objective and sacrificing another. The details of Cases I~IV are listed in Table 3-1.

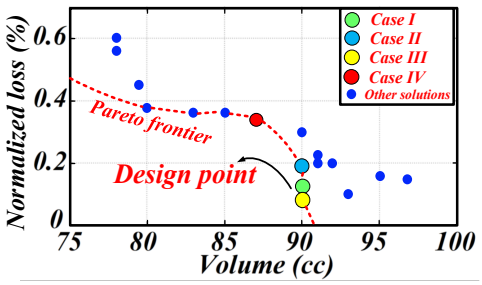



Fig. 3-4. Normalized loss vs volumes of different cores from database.

In fact, there are some criteria to select the "optimal" design from the Pareto-front solutions resulted by genetic algorithm, where the objectives are to minimize three functions: loss, weight, and volume. Here the multi-objective optimization problem is converted into a single objective function, formulated as the product of normalized loss, normalized weight, and normalized volume, where the normalization is performed with respect to the maximum loss, weight, volume of any (core, winding) candidates in the defined database. Finally, the cost function under optimization stands out as follows,

$$F(N_{strands}, D_c, l_c, A_c, V_c, A_w) = \frac{P_{loss}}{P_{loss,max}} \frac{Vol}{Vol_{max}} \frac{weight}{weight_{max}} \quad (3.15)$$

where, $P_{loss,max}$, $Vol_{max}$, $weight_{max}$ represent the maximum power loss, maximum volume and maximum weight of any candidates in the formed database. The optimal design is based on the minimum cost function value of any candidate.

3. 1. 4 Comparison and Simulation Results

To illustrate the aforementioned analyses and verify the effectiveness of the optimal design, several numerical examples are presented to show the loss analysis. Table 3-2 gives the specifications of the transformer in different cases. EE65 core with R material from MAGNETICS is selected for Cases I~III, while PQ50 with 3C96 material from FERROXCUBE are selected for Case IV.

Table 3-2. The detailed transformer specifications for different cases.

| | Case I | Case II | Case III | Case IV |
|---|---|---|---|---|
| Transformer Core | EE65 | EE65 | EE65 | PQ50(3C96) |
| Turns ratio | 20:14 | 20:14 | 15:11 | 20:14 |
| Primary winding | AWG14 (660/42) | AWG14 (150/36) | AWG12 (700/40) | AWG14 (150/36) |
| Secondary winding | AWG14 (660/42) | AWG12 (259/36) | AWG12 (700/40) | AWG12 (259/36) |
| Frequency (*kHz*) | 127 | 127 | 127 | 127 |
| Separate cores | N/A | N/A | N/A | PQ35(3C96) |
| Separate windings | N/A | N/A | N/A | AWG14 (150/36) |

Case I is the optimal transformer solution. Case II is the initial transformer solution from the genetic algorithm, which represents the parent set in the iteration. Case III is to illustrate that having fewer turns using thicker wires would greatly reduce the winding loss, although the

turns-ratio fails to meet the LLC side requirement. Case IV is a combination of the separate transformer and inductors, which is aimed to show the improvement by using the integrated transformer. The control variables are the winding and core candidates. Both theoretical calculations and FEA-based simulation results are presented as follows.

*1) Theoretical Analyses*

By implementing the derived equations, the losses can be estimated, and the calculation results are given as follows,

Table 3-3. The calculation results for different cases.

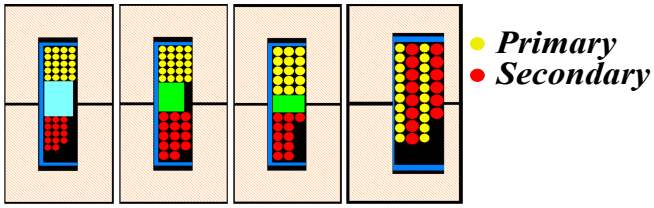
| Items | Case I | Case II | Case III | Case IV |
|---|---|---|---|---|
| Primary current $I_P$ $(A)$ | 12.375 | 12.375 | 12.375 | 12.375 |
| Secondary current $I_S$ $(A)$ | 16.5 | 16.5 | 16.5 | 16.5 |
| Primary DC resistance $(\Omega)$ | 0.0161 | 0.0177 | 0.0074 | 0.0111 |
| Secondary DC resistance $(\Omega)$ | 0.0121 | 0.0077 | 0.0054 | 0.0045 |
| Primary $F_R$ | 2.21 | 4.65 | 3.6 | 4.65 |
| Secondary $F_R$ | 1.9 | 6.92 | 2.63 | 6.3 |
| Core loss $(W)$ | 13.12 | 13.12 | 13.12 | 16.73 |
| Winding loss $(W)$ | 13 | 30.5 | 10.3 | 17.8 |
| PQ35 core loss $(W)$ | N/A | N/A | N/A | 4.15 |
| PQ35 winding loss $(W)$ | N/A | N/A | N/A | 8.9 |
| Total loss $(W)$ | 26.12 | 43.62 | 23.42 | 47.58 |
| Volume $(mm^3)$ | 90000 | 90000 | 90000 | 86800 |
| Weight $(g)$ | 570 | 585 | 567 | 491 |

Table 3-3 confirms that Case I is the optimal transformer solution over the other cases except Case III, which fails to meet the gain range requirement as aforementioned. Theoretically, it is expected that Case I should have the best thermal performance in the core

and relatively low temperature in the windings. Further simulation and experiments are implemented to verify this claim, which are presented in the later sub-sections.

*2) Simulation Results*

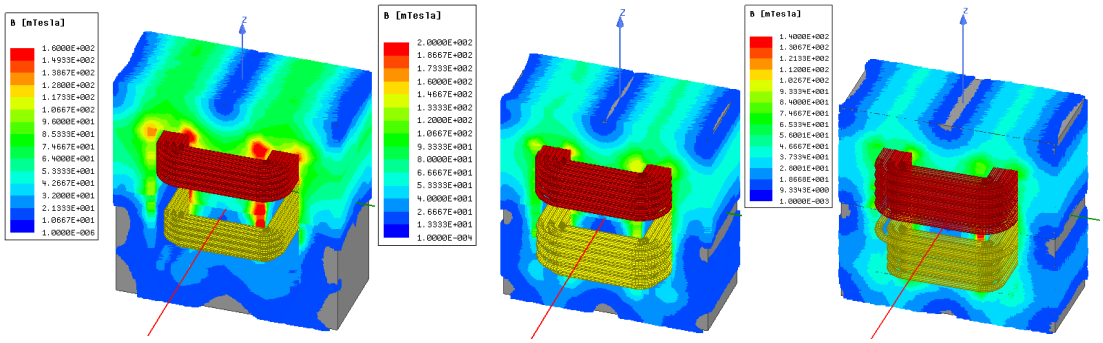
Four FEA-based three-dimensional models are developed in the simulation. The air gap is set at 1mm as in the real cases, based on the magnetizing inductance requirement. Detailed electromagnetic material characteristics and Litz wire models are developed to assure accuracy. Fig. 3-5 gives a cross-sectional view of the winding methodologies of transformers for each case. Note that Cases I ~ III all have separate winding structures while Case IV has the sandwich winding structure.



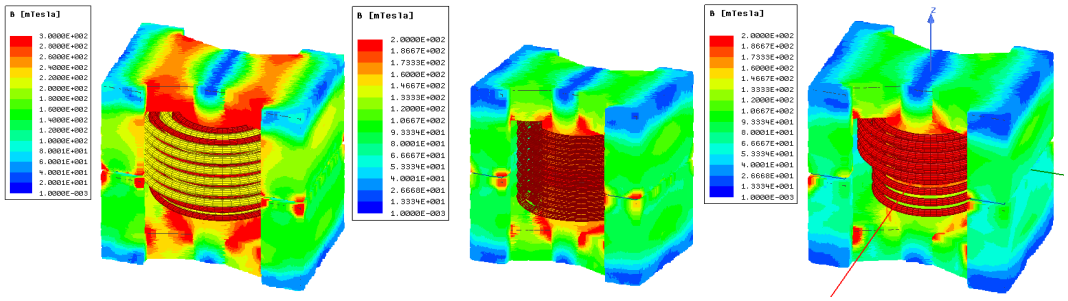

(a) (b) (c) (d)

Fig. 3-5. Winding distribution in the cross section of transformers: (a) Case I. (b) Case II. (c) Case III. (d) Case IV.

Fig. 3-6 illustrates the FEA simulation results of the magnetic field for each case. To reduce the computation time, each turn is assumed to be evenly wound around the center leg. It is observed that the maximum magnetic flux in Cases I ~ III are similar, which is consistent with the theoretical calculations. Case IV has greater flux, resulting in larger core loss. Thus, core losses for each case can be obtained using in the $\rho - B$ curve from the datasheet.



(a) Case I. (b) Case II. (c) Case III.



(d) Case IV PQ50. (e) Primary PQ35. (f) Secondary PQ35.

Fig. 3-6. The simulated magnetic field of cores for each case.

Apart from the magnetic field simulations, the current density of windings is investigated. In comparison to the calculated one, the simulated current density reflects the AC resistance using frequency sweep mode at 100kHz. Therefore, $F_R$ can be expressed as,

$$F_R = \frac{\rho_{si}}{\rho_{cal}}, \rho_{cal} = \frac{I}{A_{eff}} \tag{3.16}$$

where, $\rho_{si}$ is the simulated current density and $A_{eff}$ is the effective area of Litz wire. It is worth to mention that there are some quantified flux errors (<20%) between FEA simulation and the simplified transformer model. This is because the flux in the transformer model is single discrete quantity signifying the maximum flux, while the flux distribution from the simulation is continuous. In order to perform a fair comparison, the maximum flux density value is picked up from simulations results. For the sake of clarity, a table listing the errors in flux densities obtained from model-based calculation and simulation is presented in Table 3-4.

Table 3-4. The quantified errors between simulation and proposed flux model.

| Items | Case I | Case II | Case III |
|---|---|---|---|
| Maximum flux in model (*mT*) | 142 | 142 | 158 |
| Maximum flux in simulation (*mT*) | 160 | 155 | 140 |
| Flux error (%) | 11.2 | 8.4 | 12.8 |
| Core loss error (%) | 6 | 19 | 20 |

3. 1. 5 Experimental Verifications

To validate the transformer model and optimization results, a packaged prototype of 3.3kW onboard charger using dual-output DC/DC resonant converter is developed, as shown in Fig. 3-7. The testing procedure includes assembling the transformer inside of the charger and running up to the steady state.

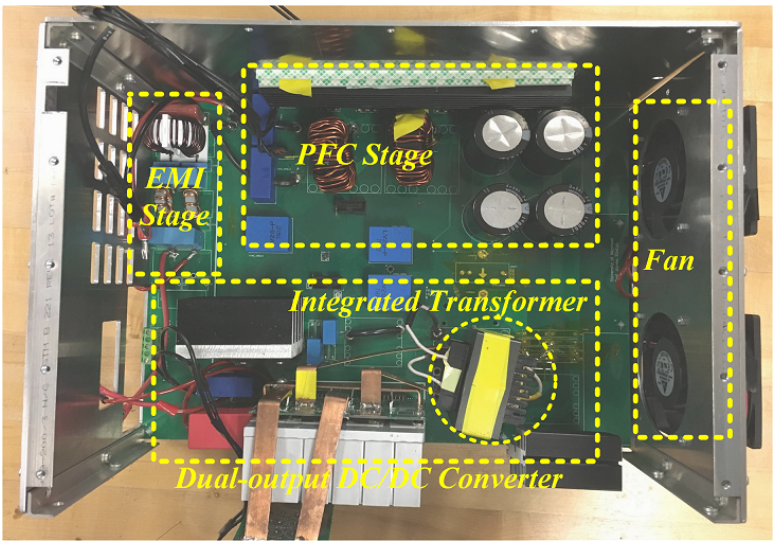



Fig. 3-7. Three-stage onboard charger with transformer-under-test.

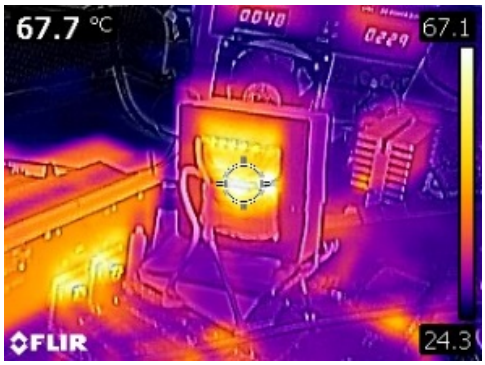


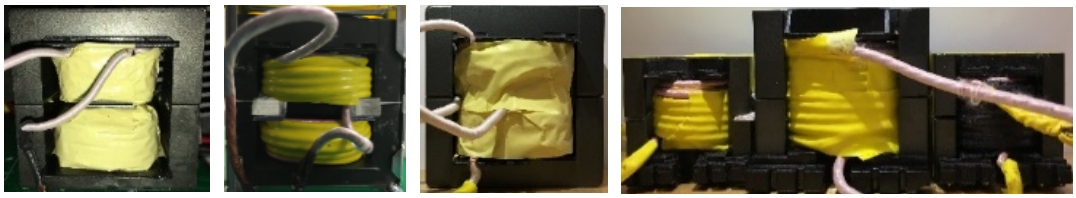

Fig. 3-8. Thermal image of the Case I transformer at 2.5$kW$.

Fig. 3-8 shows the thermal image of the Case I transformer when reaching steady state at 2.5kW. It is observed that the hottest spot in the transformer is around 68ºC and is located within the proximity of the air gap, which is a major thermal burden to the system. A transformer enclosure with thermal potting compound can be added to further address the thermal issue if needed. The experimental peak efficiency of DC-DC stage with Case I is 98.2%, measured at thermal steady state.

To further validate the proposed loss model, four sets of transformers are built for different cases under consideration. Photographs of the built transformers are illustrated in Fig. 3-9. Acrylic glass is implemented to ensure a consistent uniform gap between primary and secondary windings. The measured inductances for each case are listed as follows,

Table 3-5. The measured parameters for different cases.

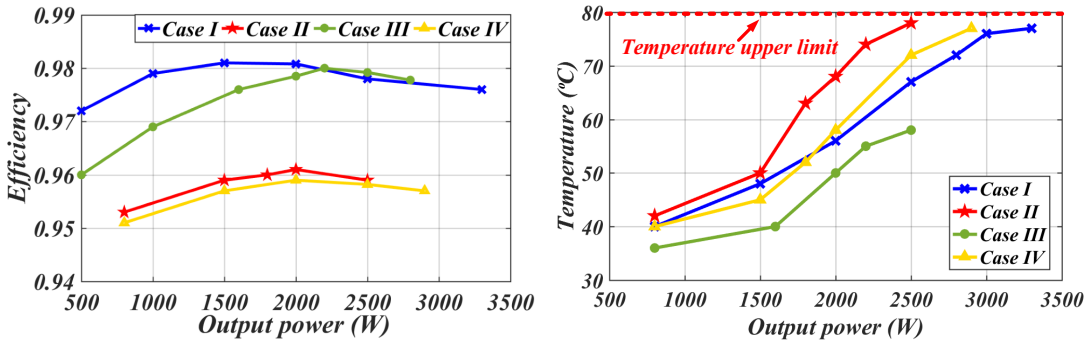
| Items | Case I | Case II | Case III | Case IV |
|---|---|---|---|---|
| $L_{r1}$ $(\mu H)$ | 22.9 | 33 | 30.8 | 22 |
| $L_{r2}$ $(\mu H)$ | 19.6 | 20.3 | 18 | 18 |
| $L_m$ $(\mu H)$ | 346.2 | 381 | 350.5 | 345.3 |



(a) (b) (c) (d)

Fig. 3-9. Imagines of the built transformers: (a) Case I; (b) Case II; (c) Case III; (d) Case IV.

The efficiency curves for each case are shown in Fig. 3-10 (a). Case I has the best efficiency performance among all cases, which further proves the effectiveness of the optimal design and analyses. Note that the regular transformer with separate inductors has a comparatively lower efficiency because of higher core loss. This further substantiates the advantage of using the integrated transformer. Moreover, the comparison between Case I and Case II confirms the optimization of Litz wire and thus, the winding loss is minimized in Case I. Fig. 3-10 (b) shows the temperature comparison of different cases at the steady state. The temperature upper limit is set at 80°C to avoid any potential thermal damage to the system. An overall performance comparison of four cases is presented in Fig. 3-11 using the built prototype, where the temperature is reported experimentally for the steady-state operation at 2.5kW.




(a) (b)

Fig. 3-10. The comparison curves: (a) Efficiency comparison of CLLC converters using different transformers; (b) Temperature comparison.

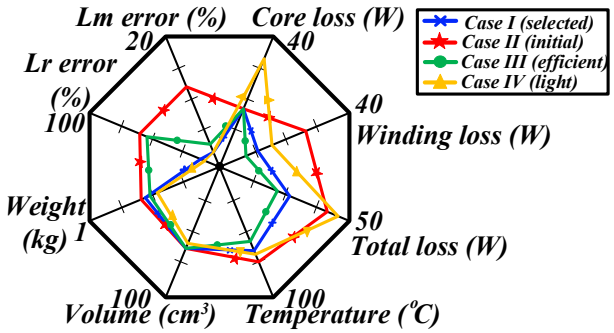



Fig. 3-11. Different cases overall performance comparison.

To show the effectiveness of the accurate power loss estimation, comparison of power loss error between the conventional and the proposed methods is given as follows. Given that it is difficult to measure the transformer loss directly, the transformer loss was obtained by subtracting other part of the loss from the measured total loss (obtained from power analyzer) in experiments. Case I's data is utilized since it is tested up to full power. The table below clearly shows a significant decrease of error in loss estimation using the proposed model instead of the conventional method.

Table 3-6. Errors between the conventional and proposed model (Case I).

| | Real power loss | Conventional model | Proposed model |
|---|---|---|---|
| Value ($W$) | 28 | 23.8 | 26.12 |
| Error ($\%$) | - | 15 | 6.7 |

## *3. 2 The Proposed Integrated Planar Transformer*

In fact, the Litz-wire transformer design (Case I) has the following drawbacks: (i) The winding AC resistance $R_{AC}$ is not optimized and is still relatively large, leading to increased loss with large amounts of winding current, which significantly decreases the efficiency and may require a demanding thermal solution. More specifically, since the magnetomotive forces (MMFs) across each winding sum up in the end, the AC resistance would be substantially large in the middle point, as can be seen in Fig. 3-12; (ii) the Litz-wire-based winding configuration

is difficult for manufacturing as the leakage inductance is sensitive to the accuracy of distance between primary and secondary windings; (iii) the tertiary winding is made of copper bar and needs massive labor work, making it difficult for commercial manufacturing; (iv) the implementation of a standard EE core limits the simultaneous charging function due to high winding loss; and (v) the wire-wound transformer leads to the higher height for the system.

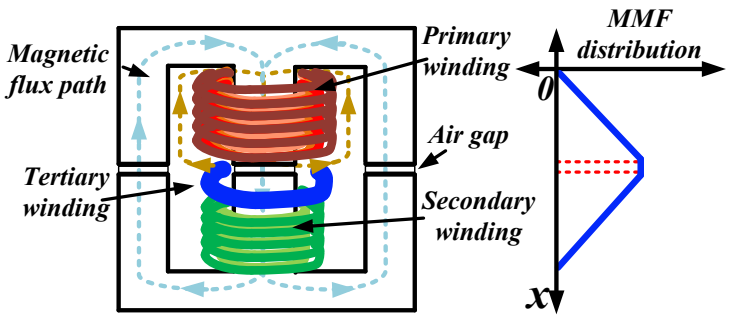



Fig. 3-12. The integrated transformer with MMF distribution.

Thus, a new three-winding planar transformer configuration is proposed using the optimization algorithm, as shown in Fig. 3-13. The primary and secondary windings of the transformer are split unevenly in both side legs. The reasons behind winding in two legs are: (1) to compensate the magnetizing inductance reduction due to the interleaved structure; and (2) to obtain a controllable leakage inductance. To reduce the winding loss, each PCB layer has one turn. The planar transformer with the proposed PCB winding configuration is utilized to further improve the manufacturability, power density, and efficiency. A systematic transformer loss model, including both core and winding losses, is investigated. Magnetizing and leakage inductances can be obtained from both the analytical model and simulation. Consequently, a multi-objective optimization problem is formulated to optimize the integrated transformer design considering core geometry, losses, and inductances. The objective is to determine a set of core and winding specifications to achieve minimum transformer loss. The traditional approach of using a three-winding transformer with a center leg with twice the width of the

outer legs [81], [82] is not suitable in this case due to the inherently unbalanced flux distribution of the core. Finally, the design is accomplished using a customized core.

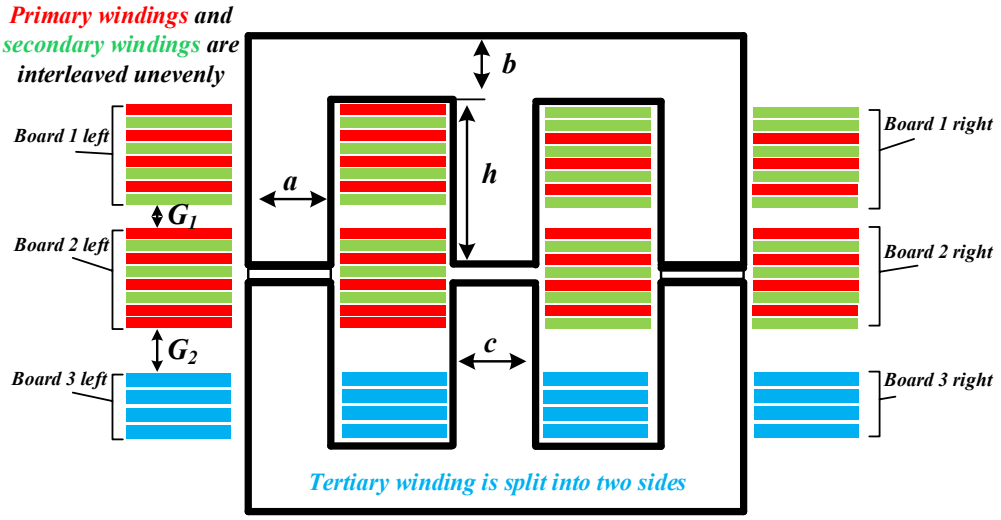



Fig. 3-13. The integrated planar transformer with three PCB winding boards.

The leakage inductance can be controlled by the adjustment of the center leg width $c$, as shown in Fig. 3-13. The width $a$ and height $h$ of side legs can be adjusted to reduce the core loss while maintaining enough magnetizing inductance. The increase of the thickness $d$ reduces the effective reluctance and core loss, however, it leads to a smaller window area. The width ratio $k = \frac{c}{a}$ between the center and side legs contributes to the core loss and the leakage inductance. It is worth mentioning that the center leg enables the leakage flux path, which is determined by the reluctance of the center leg air gap. If the center leg air-gap reluctance is large, less leakage flux will flow through it, resulting in smaller leakage inductance. Consequently, the leakage flux in the proposed magnetic structure is confined within the core instead of in the air. The confined flux can contribute to the less radiated EMI and eddy current loss in the surrounding metals.

### 3. 2. 1 The Planar Transformer Loss Model

*1) The Proposed Transformer Core Loss Model*

Considering the symmetrical structure of the integrated transformer, a novel transformer core loss model based on the proposed winding structure is established to achieve more accurate results using the magnetic equivalent circuit. This core loss model includes the leakage flux path from both windings and air gap, meanwhile splits the location of magnetic flux path from the side legs and the center leg. Three current sources are considered to form the equivalent magnetic circuit, where the reluctance is obtained from each leg piece to improve the accuracy of the model.

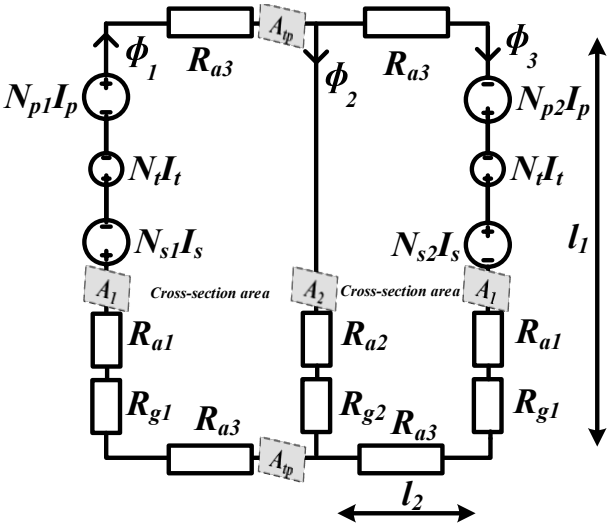



Fig. 3-14. The equivalent magnetic circuit of the integrated transformer.

As shown in Fig. 3-14, primary and secondary windings are asymmetrically placed in both side legs to obtain controllable leakage inductance. The tertiary windings in the side legs are connected in parallel to reduce the overall resistance. Meanwhile, the cross-section areas of the side and center legs are denoted as $A_1$ and $A_2$ in Fig. 3-14. The relations among the winding turns are expressed as,

$$N_{p1} + N_{p2} = N_p\ ,\ N_{s1} + N_{s2} = N_s\ ,\ N_{p1} = N_{s2}\ ,\ N_{p2} = N_{s1} \tag{3.17}$$

where $N_{p1}$ represents the primary winding on the left column and $N_{p2}$ represents the primary winding on the right column; $N_{s1}$ represents the secondary winding on the left column and $N_{s2}$ represents the secondary winding on the right column. Furthermore, $N_{p1}I_p$ and $N_{p2}I_p$ denote

the magnetomotive forces (MMFs) of primary winding excitation across the left and right column; $N_{s1}I_s$ and $N_{s2}I_s$ denote the magnetomotive forces (MMFs) of secondary winding excitation across the left and right column. $R_{a1}$ and $R_{a2}$ represent the reluctance of the side leg and center leg, respectively. $R_{g1}$ and $R_{g2}$ represent the reluctance of the side leg air gap and center leg air gap, respectively. $R_{a3}$ denotes the equivalent reluctance of upper / bottom leg piece. The reluctance expressions are related to the cross-sectional area of the core, which are given by,

$$R_{\mathrm{g1}} = \frac{l_{air}}{\mu_0 A_1},\ R_{\mathrm{g2}} = \frac{l_{air}}{\mu_0 A_2} \tag{3.18}$$

$$R_{\mathrm{a1}} = \frac{l_1}{\mu A_1},\ R_{\mathrm{a2}} = \frac{l_1}{\mu A_2}, R_{\mathrm{a3}} = \frac{l_2}{\mu A_{tp}} \tag{3.19}$$

where $l_{air}$, $l_1$ and $l_2$ is the magnetic path of the air gap, side leg and top/bottom leg magnetic piece, $\mu_0$ is the permeability of the air. Assume $N_{p1} \geq N_{p2}$, the flux direction is determined from the left leg to the center leg and right leg. It is worth mentioning that the center leg flux contributes to the leakage flux, which forms the leakage inductance of the transformer. Therefore, the total reluctance $R_{tp}$ can be expressed as a function of core geometry and its magnetic parameters,

$$R_{tp} = f(l, geo, l_{air}) = R_{\mathrm{a1}} + R_{\mathrm{g1}} + 2R_{\mathrm{a3}} + \frac{(R_{\mathrm{g2}}+R_{\mathrm{a2}})(2R_{\mathrm{a1}}+2R_{\mathrm{g1}}+4R_{\mathrm{a3}})}{2R_{\mathrm{a1}}+R_{\mathrm{a2}}+R_{\mathrm{g2}}+2R_{\mathrm{g1}}+4R_{\mathrm{a3}}} \tag{3.20}$$

where $l$ is the magnetic path parameter, $geo$ is the core geometry parameter, $l_{air}$ is the air gap length. $\emptyset_1$, $\emptyset_2$ and $\emptyset_3$ are the magnetic flux flowing through each leg. Therefore, the magnetizing inductance and the leakage inductance can be derived as,

$$L_m = \frac{N_{p1}^2+N_{p2}^2}{R_{tp}} = \frac{N_{p1}\emptyset_{1|I_s=I_t=0}+N_{p2}\emptyset_{2|I_s=I_t=0}}{I_p} \tag{3.21}$$

$$L_{lk} = \frac{N_{p1}\emptyset_{1|I_s=I_t=0}+N_{p2}\emptyset_{3|I_s=I_t=0}-N_{s1}\emptyset_{1|I_s=I_t=0}-N_{s2}\emptyset_{3|I_s=I_t=0}}{I_p} \tag{3.22}$$

On the other hand, the flux density for the different magnetic piece $B_i$ can be examined. For instance, the flux density of the left leg is presented as,

$$B_{left} = \frac{N_{p1}I_p - N_{s1}I_s - N_tI_t}{R_{tp}A_1} \tag{3.23}$$

Thus, the flux density for the different magnetic piece $B_i = \emptyset_i R_i$ can be examined. Since the Steinmetz equation is more accurately applicable for a sinusoidal waveform, an equivalent frequency for calculating the core loss using the Steinmetz equation should be determined for a triangular waveform in a TAB-based converter. This is derived using a method mentioned in [97] and presented as follows,

$$f_{eq} = \frac{1}{2{B_i}^2\pi^2}\int_0^{f_s}\left(\frac{dB}{dt}\right)^2 dt = \frac{8f_s}{\pi^2} \tag{3.24}$$

Therefore, a more accurate core loss result for the integrated transformer is achieved using the proposed reluctance model,

$$P_{core} = \sum V_i A_i (B_i)^{\alpha} f_{eq}^{\beta} \tag{3.25}$$

where $V_i$ is the volume for each piece and $\sum V_i = V_c$.

*2) PCB winding loss*

Regarding the PCB winding, the winding loss is mainly determined by the MMF distribution, which means that the winding layer structure needs to be carefully considered. The MMFs are suppressed using the interleaved winding structure, where the primary and secondary windings are asymmetrically placed in both side legs. The top two boards 1 and 2 are composed of the primary and secondary windings while all the tertiary winding is located in the bottom board 3, where the distances between the boards are denoted as $G_1$ and $G_2$, as shown in Fig. 3-13.

The layer change for the same winding is realized by the vias. Both left and right PCB layers with the same vertical height share the same PCB board. The proposed winding structure along with the MMF distribution is demonstrated in Fig. 3-15. The connections between boards are realized in the main board. Given $N_{p1} = 9, N_{p2} = 7$ , the proposed winding structure along with the MMF distribution is demonstrated as,

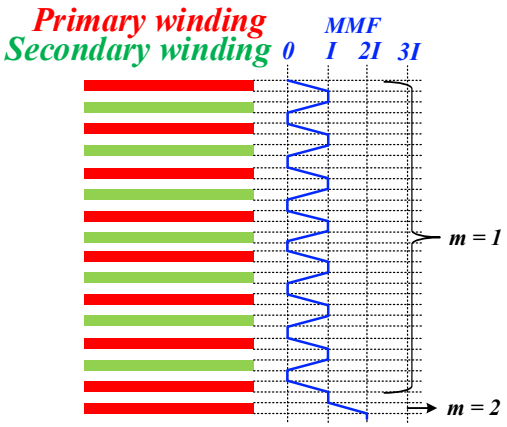



Fig. 3-15. One side leg winding configuration with MMF distribution.

Consequently, only the bottom two layers have the non-interleaved windings in the left leg, and the top two layers in the right leg have non-interleaved windings. This kind of winding configuration takes the advantage of interleaving to reduce the winding loss while maintaining the magnetizing and leakage inductances. In general, $N$ (e.g. $i$, $j$, $k$, and $l$ in Fig. 3-16) bottom/top layers can be implemented as the non-interleaved windings to achieve the desired inductances. The increase of $N$ leads to larger magnetizing and leakage inductances, and winding loss. As shown in Fig. 3-16, $i$, $j$, $k$ and $l$ are denoted as the number of non-interleaved windings in the left top, left bottom, right top, and right bottom, respectively. They can be the same or different values, depending on the design specifications.


Fig. 3-16. The generalized non-interleaved winding configuration.

Based on Dowell's assumptions for single winding per layer structure, the expression for total resistance $R_{total}$ of the $\alpha$th layer including $R_{AC}$ and $R_{DC}$ is derived in [100],

$$R_{total} = \frac{xR_{DC}}{2}\left[\frac{\sinh(x)+\sin(x)}{\cosh(x)-\cos(x)} + (2m-1)^2\frac{\sinh(x)-\sin(x)}{\cosh(x)+\cos(x)}\right] \quad (3.26)$$

where $m$ and $x$ are given by,

$$m = \frac{MMF(\alpha)}{MMF(\alpha)-MMF(\alpha-1)},\ x = \frac{Thickness\ of\ PCB}{Skin\ depth} \quad (3.27)$$

Note that a lower MMF ratio $m$ leads to a weaker proximity effect in the adjacent layers. Thus, this winding configuration can achieve a low MMF ratio for all the layers while maintaining the sufficient leakage inductance. Furthermore, the DC resistance of PCB copper trace is represented as,

$$R_{dc} = \frac{\rho_{copper} l_{sur} N}{A_{PCB}} \quad (3.28)$$

Therefore, the total winding resistance of primary winding [32] can be expressed as,

$$R_{eff} = \left(1 - \left|\frac{N_{p1}-N_{s1}}{2N}\right|\right) \times R_{total_{m=1}} + \left|\frac{N_{p1}-N_{s1}}{2N}\right| \times R_{total_{m=2}} \quad (3.29)$$

Meanwhile, the winding loss can be further reduced by settling the layer thickness less than the skin depth, which allows the effective cross-section area to be increased. Considering the high current rating, the tertiary windings can be split into two parts and wound around the side legs to maintain the flux balance.

### 3. 2. 2 Parasitic Capacitance Study

The parasitic capacitance of the planar transformer can lead to many issues, including the winding current/bridge voltage waveform distortion, unexpected voltage gain, increased EMI noise, and reduced power conversion efficiency. Thus, it is necessary to conduct a thorough study on the parasitic capacitance mitigation in the proposed transformer. The simplified equivalent parasitic circuit is shown in Fig. 3-17, which can be utilized to obtain the inter/intra-winding capacitances from the network analyzer measurement. The inter-winding capacitance refers to the parasitic capacitance between primary and secondary windings, which have little effect in distorting the waveforms; the intra-winding capacitance, on the other hand, contributes to the waveform distortion.

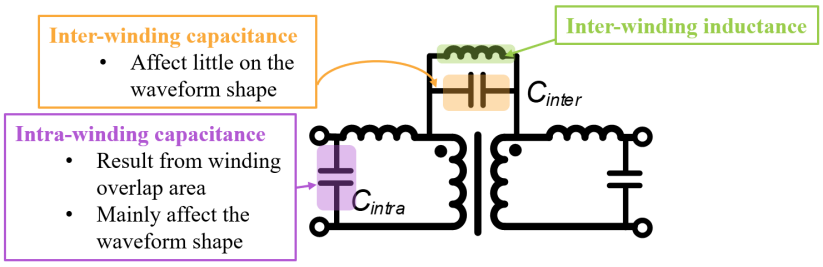



Fig. 3-17. The simplified equivalent parasitic circuit of the proposed planar transformer with PCB windings.

The parasitic capacitances are related to the following factors:

(i) Adjacent winding overlap surface area $S$. It directly determines the parasitic capacitance value. However, the decrease of $S$ also increases the AC winding loss due to the eddy effect.

(ii) Distance between two winding layers $\Delta h$. The increase of $\Delta h$ leads to the larger leakage inductance and smaller parasitic capacitance;

(iii) Dielectric material property. Usually, FR4 material is used for PCB manufacturing with the $\varepsilon_r$ of 4.3;

(iv) Winding configuration, which is related to the MMF distribution;

(v) Core geometry. The increase of the cross-section area leads to the reduced reluctance and lower core loss. On the other hand, it increases the winding loss as the width of the winding trace needs to be compromised.

The formula for the capacitance between two parallel conductive plates is given by,

$$C_o = \varepsilon_r \varepsilon_o \frac{S}{\Delta h} \tag{3.30}$$

where $\varepsilon_o$ is the permittivity of the air and $\varepsilon_r$ is the relative permittivity of the dielectric material. As shown in Fig. 3-18, both intra/inter winding capacitances are decreased in a small range when the frequency increases.

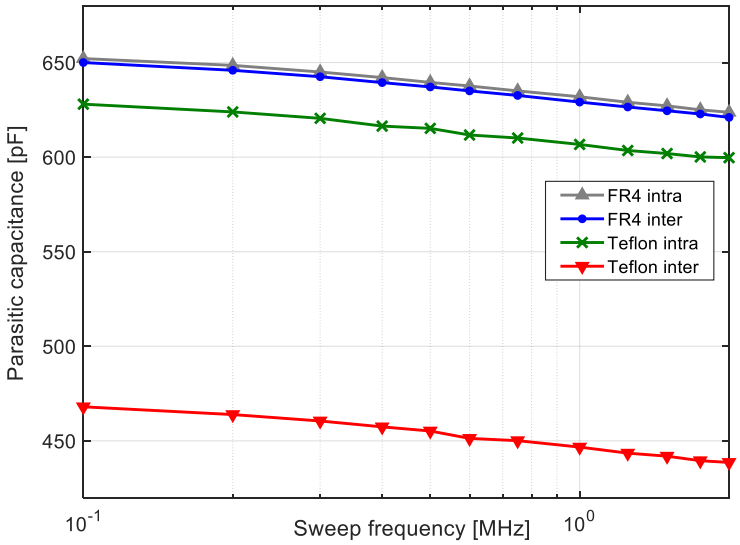



Fig. 3-18. The inter/intra-winding capacitance frequency sweep with FR4 and Teflon materials from ANSYS.

Moreover, the turns ratio sweep is conducted to investigate the relation between the parasitic capacitance and the circulating power, as shown in Fig. 3-19. It is observed that both the objective function (formed by the circulating power) and the winding loss function are inversely proportional to the turns ratio, as shown in Fig. 3-19. The high step-down turns ratio help reduce the circulating energy in the tank. However, the increase of the turns ratio leads to the increase in the parasitic capacitance due to the increased overlapping area. It is worth mentioning that although more winding turns lead to more winding resistance, considering the reduced winding current, the winding loss is in fact reduced. In other words, the control burden can be relieved with the high step-down turns ratio. Thus, the turns ratio 16:1 for the primary/secondary to tertiary is the solution considering high conduction loss and manufacture capability, which can be realized by the two PCB boards with 8 layers on each board. The PCB board with 8+ layers is not preferred due to the high manufacturing cost, especially for high-power applications.

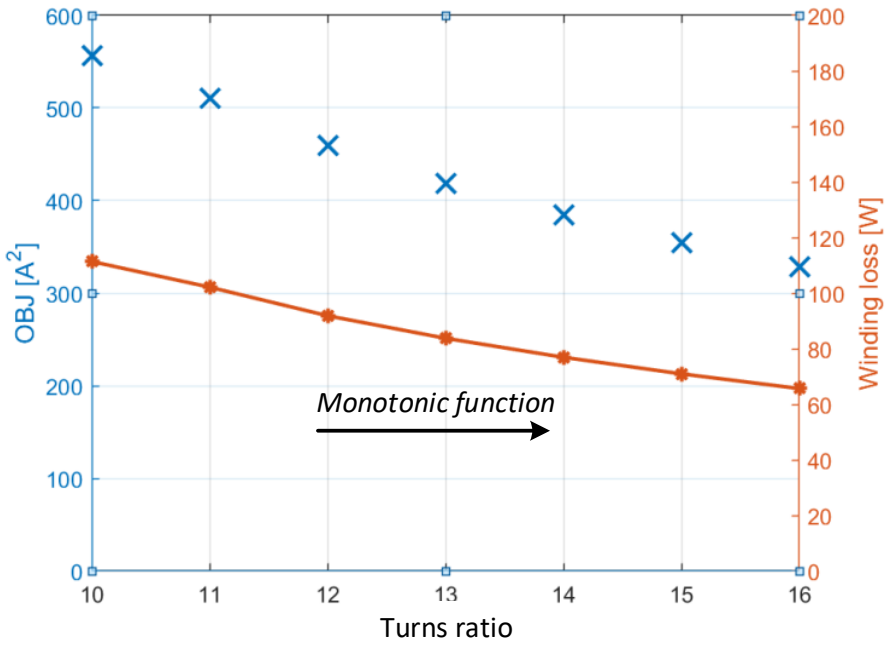



Fig. 3-19. The turns ratio sweep considering the circulating power and winding loss.

Apart from the turns ratio, the overlap area between the adjacent layers contribute to the parasitics and winding loss. A series of simulation studies are conducted in Ansys to achieve the relationship between the overlap area, winding loss, magnetizing inductance, core loss, and parasitic capacitance. 5.5mm PCB trace width with 3oz copper thickness is implemented in the design. The transformer 3D model is shown in Fig. 3-20. The parameter variation on the PCB traces overlapping between the primary and secondary windings is achieved using the optimetrics analysis, as shown in Fig. 3-21 and Fig. 3-22. It is observed that the core loss is not varied with different overlapping displacements. However, with the decrease of the PCB overlapping area, the copper loss increase correspondingly due to the eddy effect. The parasitic capacitances, including intra-winding and inter-winding capacitances, are reduced.

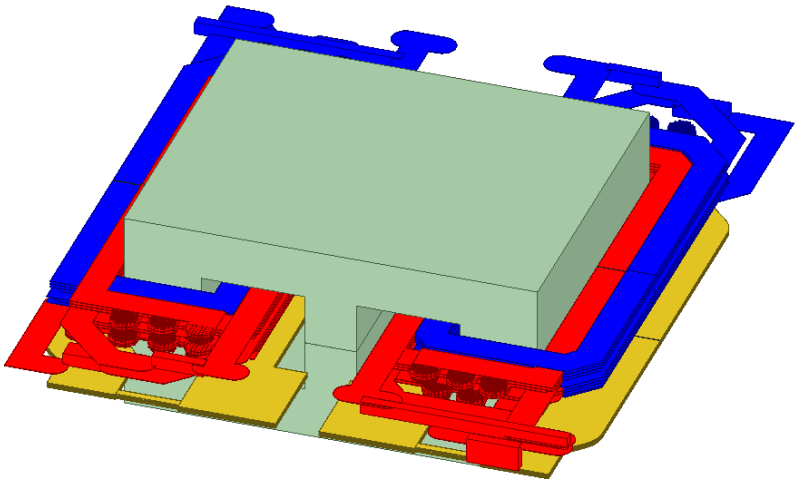


Fig. 3-20. The proposed transformer 3D model with high fidelity in Ansys.

A comprehensive winding study is conducted with different overlapping displacements, where the PCB trace model is extracted from the PCB layout software to ensure the model fidelity, and the winding loss and capacitance values are obtained from the Ansys. The displacement range is not only determined by the PCB trace width, but also is related to the core geometry, where the minimum clearance requirement between the core and the winding board needs to be satisfied. To better understand these factors, two cases of the PCB winding configurations are investigated and manufactured for the laboratory testing, which are shown in red and green color in Fig. 3-21 and Fig. 3-22.

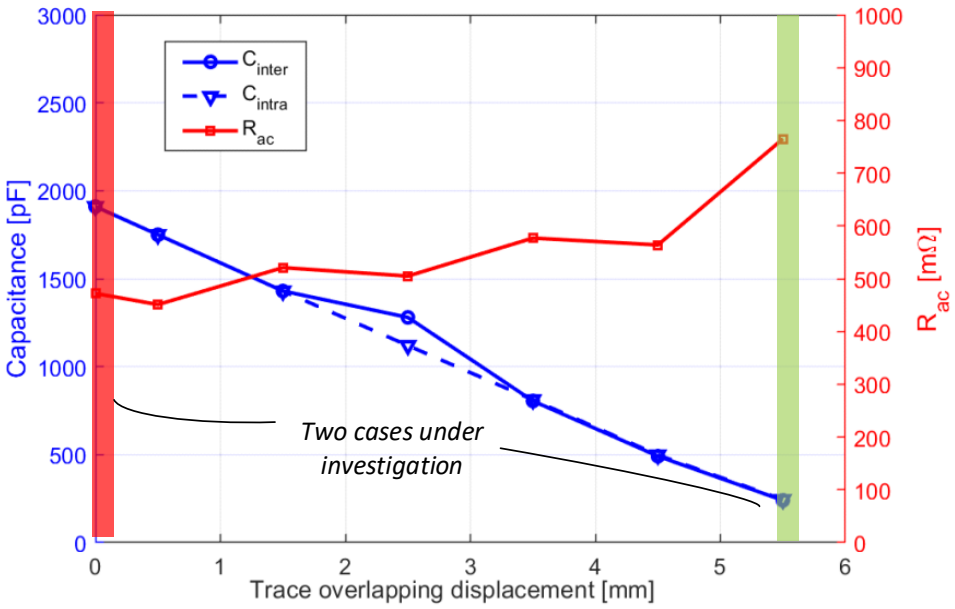



Fig. 3-21. The trace overlapping variation study on winding loss and parasitic capacitances. The red color represents the winding configuration with non-split structure; the green color represents the winding configuration with fully split structure.

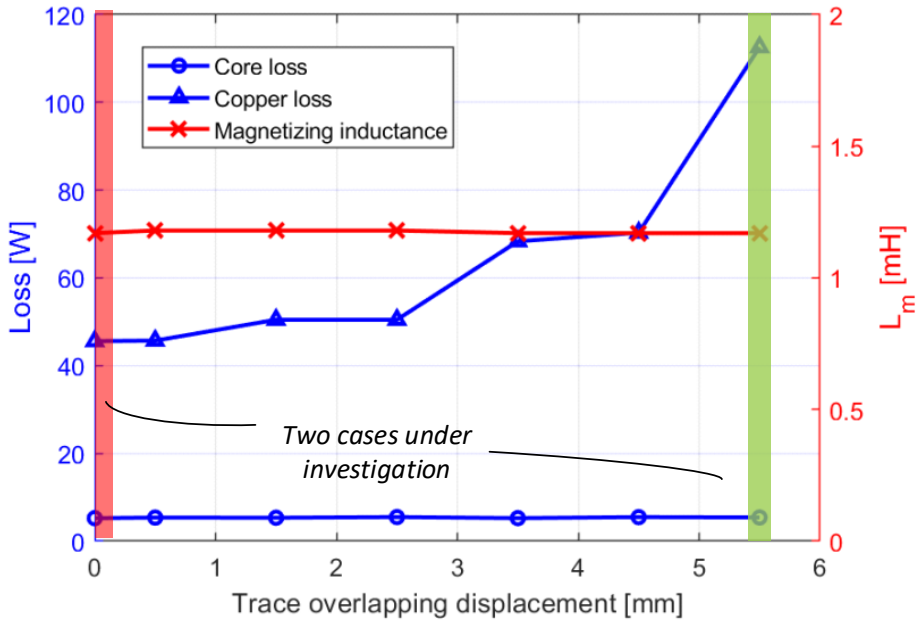



Fig. 3-22. The trace overlapping variation study on transformer loss and magnetizing inductance. The red color represents the winding configuration with non-split structure; the green color represents the winding configuration with fully split structure.

Fig. 3-23 and Fig. 3-24 illustrate the simulation results of the current density distribution in the PCB windings. It is observed that the current density increases when the split-structure is implemented. As can be seen from Fig. 3-23, the split structure merits the parasitic capacitance because of the minimum overlapping area. However, the current vector is concentrated in the adjacent terminals between the primary and secondary windings, which results in lower effective conduction area and higher winding resistance. In Fig. 3-24, the current density is distributed along with all the sections, which leads to lower winding resistance.

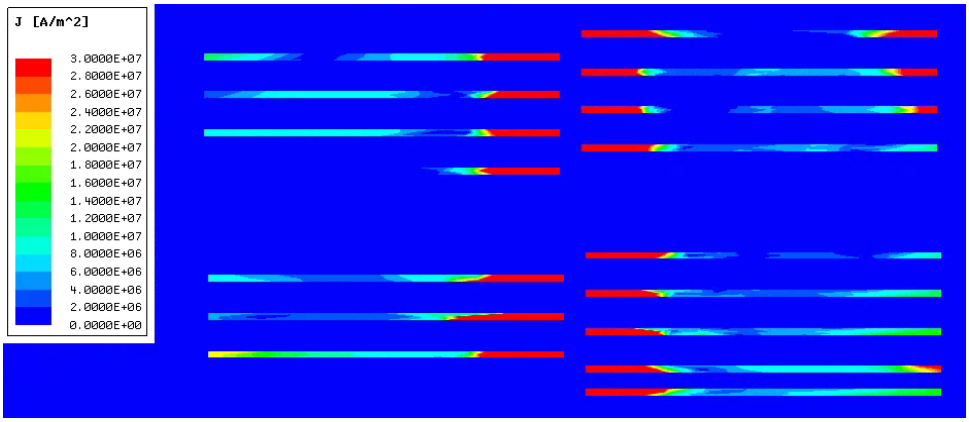



Fig. 3-23. The current density distribution in the split winding structure.

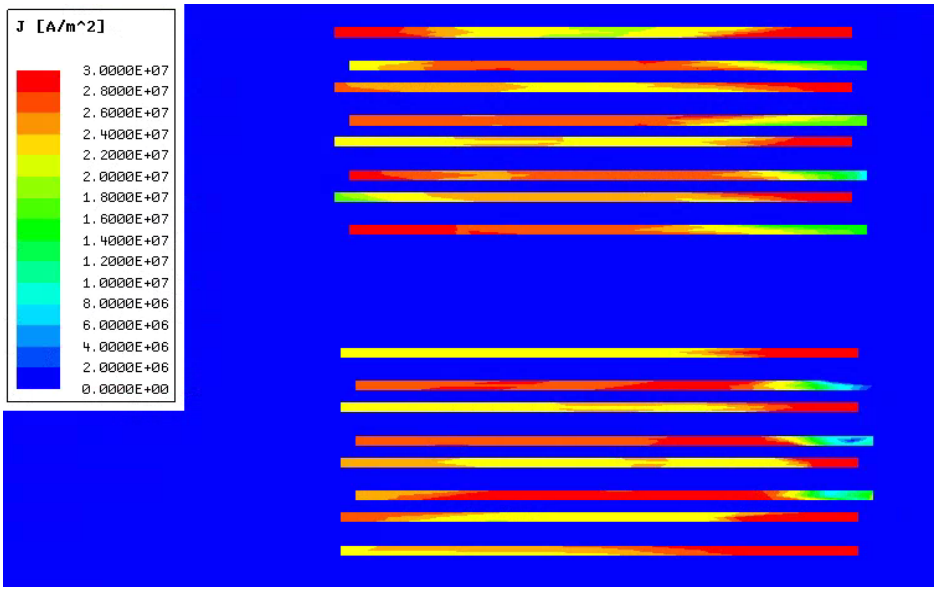



Fig. 3-24. The current density distribution in the non-split winding structure.

Therefore, the parasitic capacitances need to be suppressed in the PCB design process. The overlap area between the adjacent layers needs to be optimized to reduce the parasitic capacitances while maintaining the low winding loss. Moreover, the thickness of the dielectric material can be increased to further reduce the intra-winding/inter-winding capacitances. Teflon or Polyimide can be chosen as the insulation material due to their higher permittivity compared to FR4.

### 3. 2. 3 Multi-Objective Optimization

Some effort has been made in [101] to achieve the controllable leakage inductance while maintaining a small $R_{AC}$ for a two-terminal transformer. By means of an asymmetric winding placement in both side legs of an EE core, $R_{AC}$ and $L_k$ can be controlled simultaneously. However, the modeling technique in [101] is not suitable for the desired three-terminal transformer. In order to achieve an optimal design of the magnetic core with suitable PCB winding type, a multi-objective optimization process is conducted with an iteration & perturbation-based algorithm [102].

Considering the proposed transformer performance model including loss, inductance, and parasitics, a multi-objective optimization process is conducted to achieve the optimal design. The flowchart describing the transformer optimization process is shown in Fig. 3-25. The objectives are minimizing the losses and achieving the smallest possible volume. Prior to applying the optimization process, the first and foremost target is to determine the transformer parameters from the TAB converter operation requirement, which is able to satisfy the range of desired power transferred to the HV and LV batteries. Therefore, the fixed parameters are as follows: primary winding turns, secondary winding turns, tertiary winding turns and turns ratio. In order to identify the candidates for core and winding with optimized performance in terms of loss, volume and weight, the tuning variables for the optimization process are effective volume, air gap length, cross-sectional area, core geometry, magnetizing and leakage

inductance, width and thickness of PCB winding, and asymmetric winding distribution. In addition, the transformer can further be optimized with the estimation of circulating current, which can be obtained by the Generalized Harmonic Approximation (GHA).

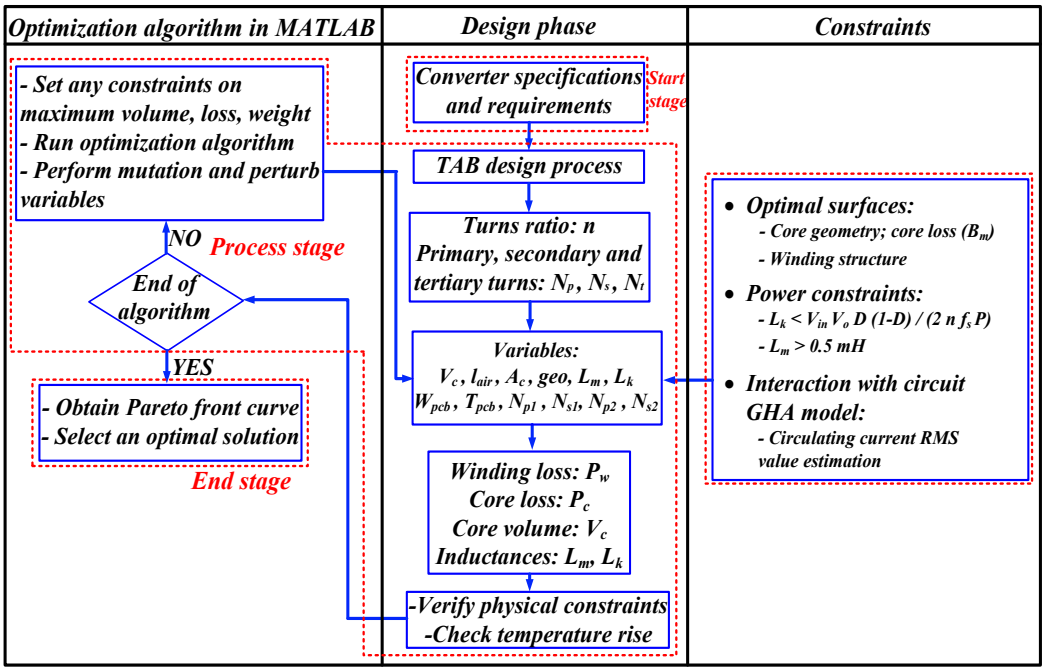



Fig. 3-25. Flowchart of the optimal integrated transformer design.

Fig. 3-26 shows the core loss density comparison between several core material candidates, which are suitable for high-frequency operation and adequate permeability. PC95 from TDK is selected due to its lowest core loss density at 100 kHz frequency.

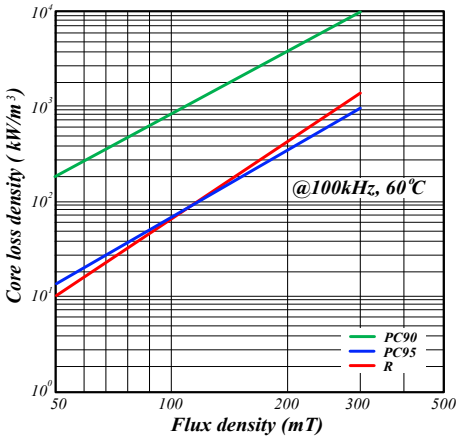



Fig. 3-26. Core loss density comparison between different materials.

Based on the selected material, the objective function is to minimize the total loss incurred in the transformer concerning the geometry parameters and electrical parameters, which is the sum of winding and magnetic core loss. The constraints are imposed on the minimum window area requirement, maximum allowable flux density, and the requirement for power transfer capability and magnetizing inductance value. The objective function is given by,

$$f\left(V_c, l_{air}, A_c, geo, L_m, L_k, W_{pcb}, T_{pcb}, N_{p1}, N_{p2}, N_{s1}, N_{s2}\right) = \frac{P_{loss}}{P_{loss,max}} \frac{V}{V_{max}} \frac{weight}{weight_{max}} \tag{3.31}$$

Fig. 3-27 shows the 3D surface of the magnetizing inductance with two independent variables from geometry parameters. Given the fixed value of air gap length, the requirement for the minimum magnetizing inductance applies an additional restriction for the transformer design, which helps define the optimal solution with air gap length iteration. On the other hand, the peak flux density can be demonstrated in Fig. 3-28 with a 3D surface similarly. Taking into consideration of the magnetic saturation, the computed surface can be reshaped.

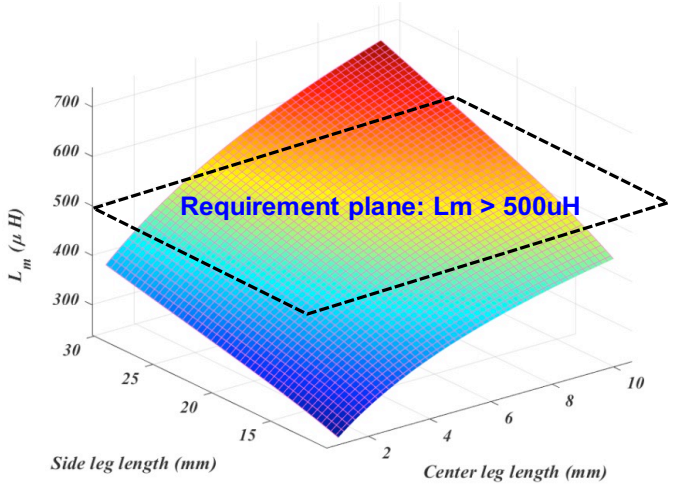



Fig. 3-27. The 3D surface of the magnetizing inductance concerning the side leg length and center leg length.

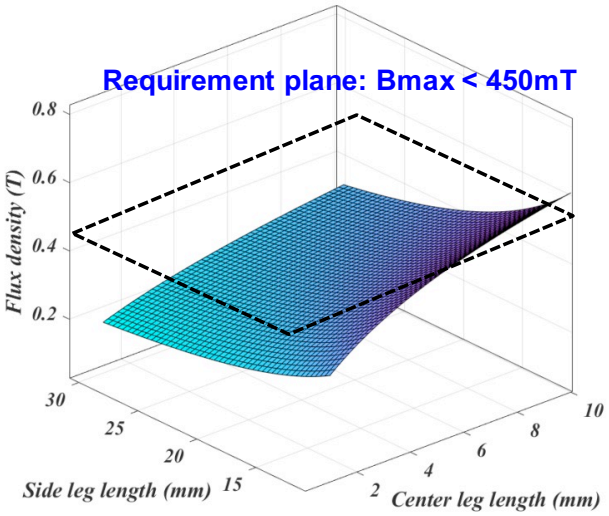



Fig. 3-28. The 3D surface of the flux density concerning the side leg length and center leg length.

Furthermore, the variation of air gap length can affect the magnetizing inductance, flux density, and core loss. The 3D surface is given in Fig. 3-29 concerning both air gap length and center leg length. It shows that the configuration with 6mm center leg length and 0.02mm air gap provides the minimum required magnetizing inductance.

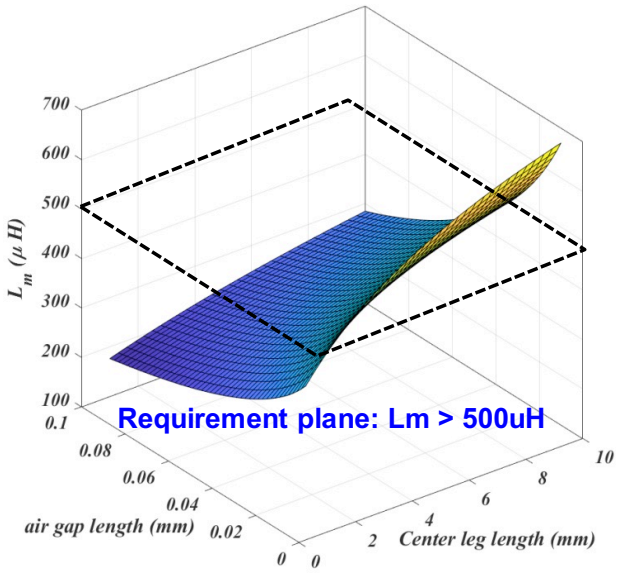



Fig. 3-29. The 3D surface of the magnetizing inductance concerning the side leg length and center leg length.

Different core geometries are obtainable using the optimization method, given different dimension constraints (similar to the current objective function). As indicated, there is a trade-off among the volume, magnetizing inductance, and core loss. The computed core geomtery database using the simplified winding model is shown in Fig. 3-30.

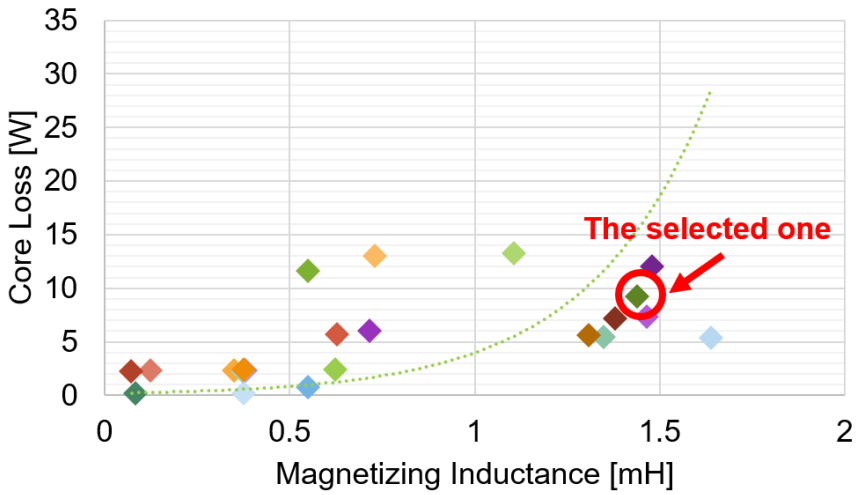



Fig. 3-30. The computed core geometry database considering core loss and magnetzing inductance.

## *3. 3 Verification*

Some preliminary Finite-Element-Analysis (FEA)-based simulations have been conducted to verify the proposed design methodology. The detailed geometrical parameters of the customized EE core are shown in Fig. 3-31. Considering the turns ratio is 16: 16: 1, it is confirmed from the simulation that $N_{p1} = 9, N_{p2} = 7$ is the optimal winding configuration to achieve the enough leakage inductance.

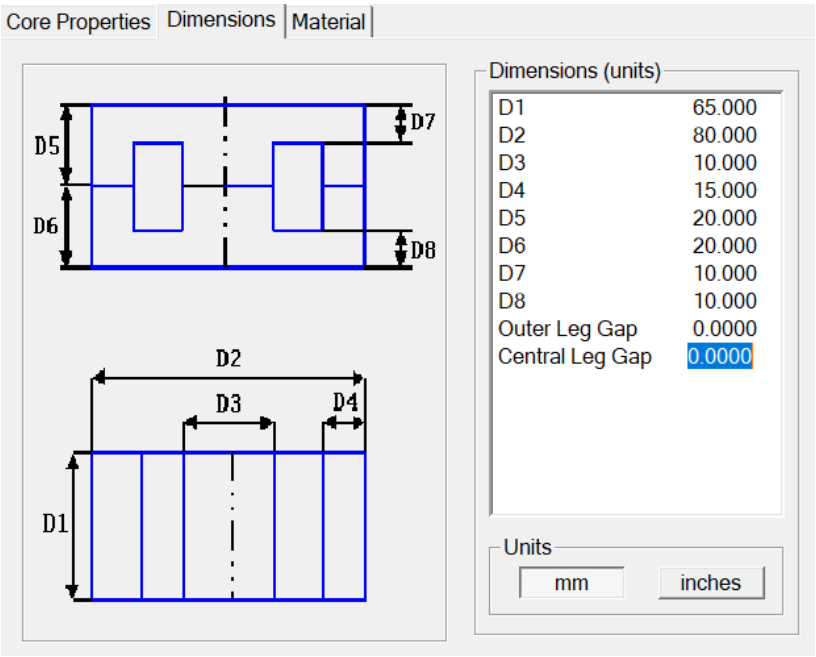



Fig. 3-31. Optimized core geometry out of the given condition.

3. 3. 1 Scale-Down Transformer

Given $N_{p1} = 3, N_{p2} = 2$ and $N_t = 1$, a preliminary integrated transformer prototype (Case III) is developed using EE planar core 0R49938EC from Magnetics, as shown in Fig. 3-32, prior to ordering the customized core.

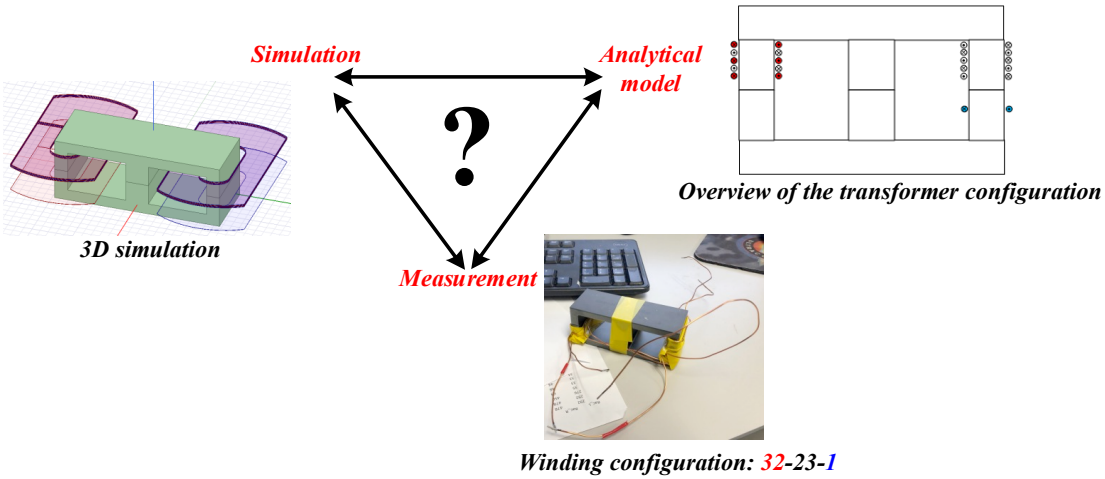



Fig. 3-32. The diagrams of the multi-method verification.

Three different cases are conducted using simulation, measurement, and analytical model. The results of the magnetizing inductance are listed in Table 3-7. Note that the magnetizing inductance value is most representative in the proposed transformer design considering its modeling complexity.

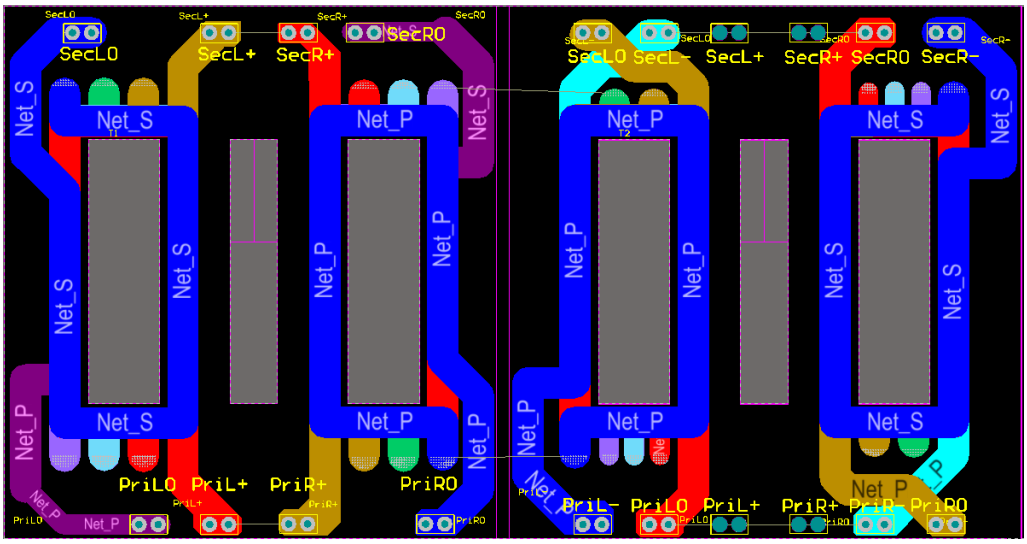
Table 3-7. $L_m$ comparison from different methods.

| Category | Remarks | Analytical (μH) | Measurement (μH) | 2D simu. (μH) | 3D simu. (μH) |
|---|---|---|---|---|---|
| Case I | Side leg 5 turns only | 112.3 | 126 | 33 | 123.6 |
| Case II | Interleaved single winding | 58.4 | 65 | 18 | 70.2 |
| Case III | Center leg 5 turns only | 197.8 | 186 | 29 | 224.8 |

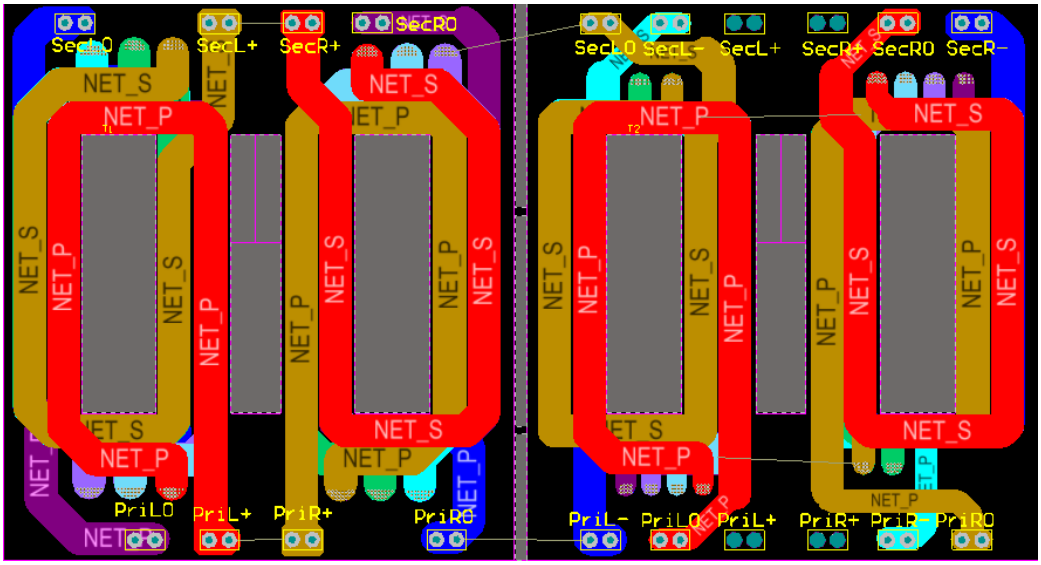
It is observed that the measurement is consistent with the analytic model and 3D simulation results. Furthermore, the magnetizing inductance decreased significantly using the interleaved structure due to the cancellation of magnetic path in the side legs.

### 3. 3. 2 Validation of the Transformer Prototype

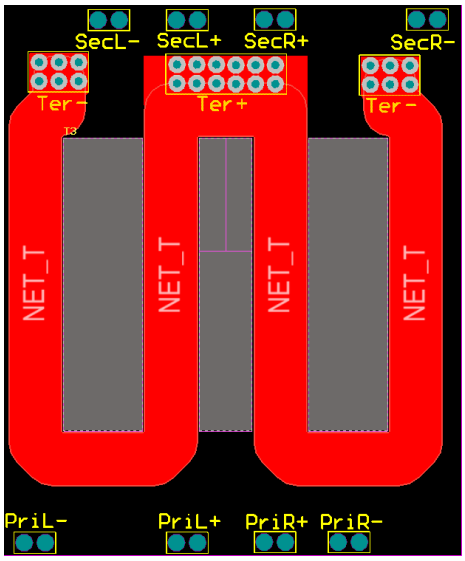
Two cases of the winding designs are achieved. The finished board thickness is around 4mm with silver immersion technique, where the dielectric layer thickness is maximized considering the manufactory capability. Moreover, the layer change terminals need to be minimized because the effective winding turns are affected by them.


SecLO
SecL+
SecR+
SecRO
SecL-
SecR-
Net_S
Net_P
PriLO
PriL+
PriR+
PriRO
PriL-
PriR-

(a)


SecLO
SecL+
SecR+
SecRO
SecL-
SecR-
NET_S
NET_P
PriLO
PriL+
PriR+
PriRO
PriL-
PriR-

(b)




(c)

Fig. 3-33. The designed PCB layout for the transformer windings: (a) with non-split structure; (b) with split structure; (c) the tertiary winding board.

As can be seen from Fig. 3-33 (c), the tertiary winding board with 4 layers in parallel forms a “W” shape PCB trace, where the left leg winding is connected in parallel with the right leg winding to increase the ampacity. Moreover, since the adjacent layer is not utilized, the intra-winding capacitance is reduced in the tertiary winding.

The customized EE core is made from TDK PC95 material because of its low core loss density at 100 kHz frequency. The assembled integrated planar transformer is shown in Fig. 3-34. The copper bars are utilized as the spacers and connectors.

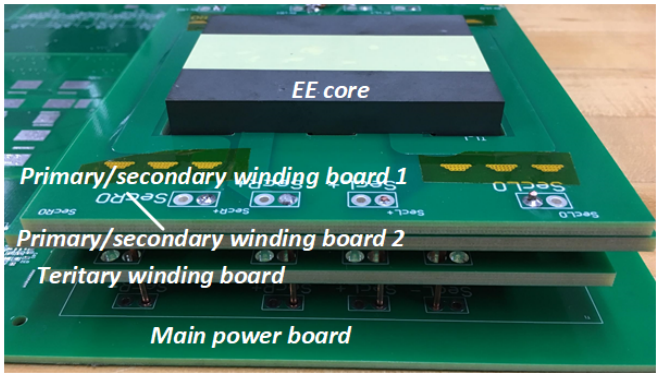



Fig. 3-34. The assembled integrated planar transformer with the main power board.

1) Transformer characterization

The transformer characterization is investigated before conducting the power test. The impedance analyzer E4990A is utilized with a wide frequency range of 20Hz to 120MHz. As shown in the figures, both open and short circuit tests are conducted for the split and non-split winding boards. One-layer tape-based air gap is employed to obtain the required leakage inductance. Thus, the parasitic capacitances, the leakage inductance, and the magnetizing inductance can be extracted using the equivalent model. The measured results are summarized in Table 3-8.

Table 3-8. The measured parameters for the split and overlap winding boards.

| Type | $f_r\ (kHz)$ | $L_m\ (mH)$ | $C_{intra}\ (nF)$ | $L_k\ (\mu H)$ |
|---|---|---|---|---|
| Split | 270 | 1.17 | 0.3 | 20 |
| Overlap | 150 | 1.68 | 0.67 | 18.5 |

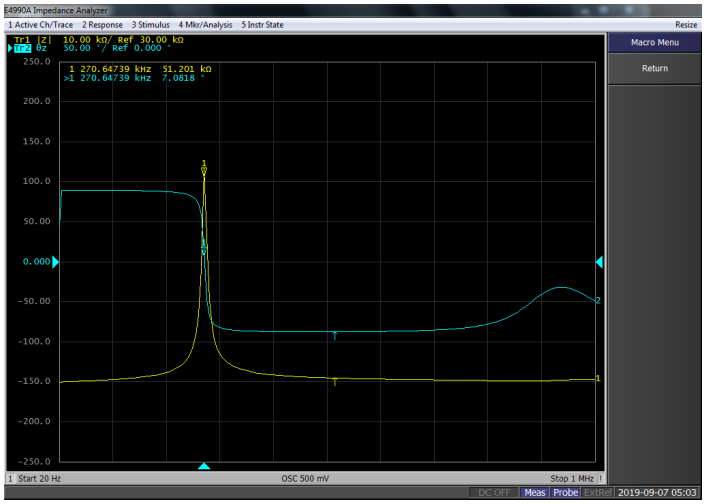



Fig. 3-35. The frequency spectrum of the transformer open circuit testing with the split PCB winding board.

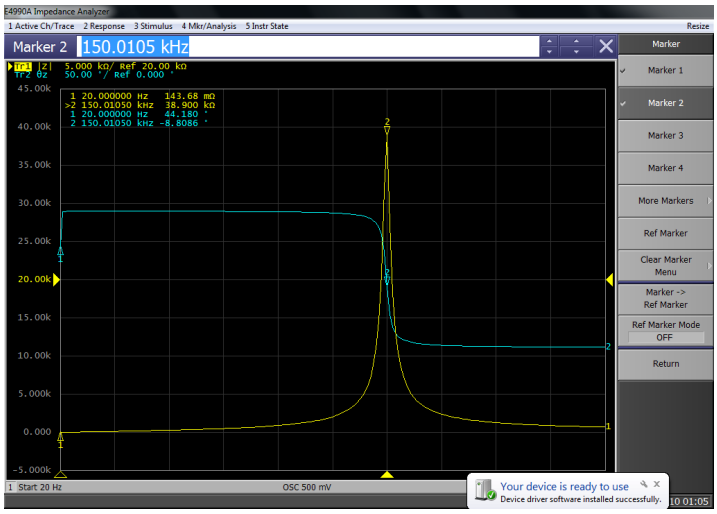



Fig. 3-36. The frequency spectrum of the transformer open circuit testing with the non-split PCB winding board.

The measured intra-winding capacitances are in consistency with the prediction. It is observed that higher parasitic capacitances are formed in the non-split winding board. Moreover, the intra-winding capacitance is reduced to 0.3nF in the split winding structure.

## *3. 4 Summary*

In this Chapter, the conventional integrated transformers are first reviewed, which have inherent drawbacks in efficiency and cannot be implemented in the proposed system. Thus, a Litz-wire based integrated transformer is proposed using genetic algorithm based design approach. Detailed core and winding loss models are discussed in the optimization process. In addition, four sets of optimized cases are selected to conduct comprehensive comparisons including the theoretical calculation, FEA simulation, and manufacturability. As a verification to the proof-of-concept, the integrated transformers are tested with a 3.3kW onboard charger prototype. It is shown that the experimental transformer loss results are in agreement with the theoretical predictions. It is reported that the optimal selection of transformer exhibits up to 2% efficiency enhancement and 10$^{o}$C temperature improvement in comparison to other feasible candidates.

In the second part, a new three-winding planar transformer configuration is introduced to further reduce the volume and improve the performance, where the primary and secondary windings are split unevenly in both side legs. To reduce the winding loss, each PCB layer has one turn. Furthermore, a systematic transformer loss model, including both core and winding losses, is investigated. Therefore, an accurate core loss model with the help of the reluctance model is proposed. Moreover, the trade-off study among the parasitic capacitances, winding loss, and leakage inductance is investigated. The magnetizing inductance and leakage inductances are obtained and verified from both the analytical model and simulations. Moreover, a comprehensive study on the parasitic capacitance is conducted, considering the trade-offs between the winding loss and the parasitic capacitance. Thus, a multi-objective optimization problem is formulated to optimize the integrated transformer design considering core geometry, losses, and inductances. The optimal winding configuration with the customized core is built and tested. It is reported from the experiment that the intra-winding capacitance is reduced to 0.3nF in the split winding structure.

# Chapter 4 : Triple-Active-Bridge GaN-Based DC-DC Converter

Typically, in the selection of the DC-DC stage topology following the PFC rectifier for traditional onboard chargers, an LLC resonant converter is a suitable candidate for unidirectional grid-to-vehicle (G2V) chargers due to its high efficiency and wide output range [103]. Recently, vehicle-to-grid (V2G) has drawn significant attention due to the flexibility for feeding electricity back into the grid for load leveling purposes [104]. Thus, CLLC and Dual Active Bridge (DAB) are examined as two most commonly used DC-DC converter topologies for bidirectional EV charger applications [105], [106]. However, considering all the charging functionalities in an integrated OBC and APM, the DC-DC stage should provide the capability of charging both HV and LV batteries simultaneously. Some recent studies have been conducted towards the integrated DC-DC converters. In [35], an integrated resonant converter based on a three-winding transformer is proposed. This integrated transformer allows integration between a half-bridge CLLC resonant converter and a high step-down LLC resonant converter with a full bridge rectifier. However, this topology is only capable of G2V, V2G and H2L operations. Simultaneous charging of HV and LV batteries is not achieved due to the topology limitation of the half-bridge resonant converters.

To overcome the aforementioned concerns, this work proposes a solution for the OBC and APM integration using the triple-active-bridge (TAB) converter. The TAB converter was first introduced in [107] for the energy storage application, and later the basic controls were developed in [108], [109]. As a topological extension to the dual-active-bridge (DAB) converter [110], the TAB converter enjoys these similar features: wide voltage gain, bidirectional power flow, and flexibility in control, however, loss of zero-voltage-switching (ZVS) under certain conditions is a concern. A unique and essential feature of a TAB topology is its flexibility to control the charging of both the HV and LV batteries simultaneously. However, due to its coupled structure, the complexity and difficulty in modeling and control

are dramatically increased. Many research projects have been conducted on the control of TAB converters, especially focusing on the power flow management. In [108], a comprehensive control method is proposed using the decoupled control network. The phase shift control is implemented for the power flow management between the ports while the duty cycle control is utilized to improve the system performance. However, since the control-to-output transfer function is dependent on the power references, the control loop may lose stability when both output voltages and power references are adjusted. Moreover, based on the voltage-second balance, [109] introduces a control method to maintain ZVS over the wide input voltage range. However, the system efficiency is not fully optimized. In [111] and [112], the modeling and control of the TAB converter are discussed, considering a wide range of power distribution between the ports using the load factor and distribution ratio. However, these works are based on the fundamental harmonic approximation (FHA), which may be invalidated when the phase between bridges is highly shifted, and thus the waveforms contain large amounts of higher order harmonics. These high order harmonic components are not negligible. In [113], a piece-wise-linear based model is developed for a two-source one-load TAB converter, which mitigates the magnetic short-circuit condition. However, the analyses on the circulating power between the two source ports are missing, which decreases the accuracy of the model. Most importantly, all the literatures regarding the TAB converter are focused on the energy storage application and distributed power system, where the wide output voltage range is out of the scope.

The major contributions of this work are summarized as: (i) a new modeling technique for a TAB converter using generalized-harmonic-approximation (GHA) considering higher odd-order harmonics; (ii) an optimal selection of shim inductance using the proposed modeling technique to enhance the efficiency; and (iii) a comprehensive control method based on GHA to minimize the circulating power and winding currents while maintaining ZVS for TAB converters to satisfy the wide output voltage range requirement. Consequently, the approach

simplifies the analysis of the power flow. By adjusting the power references, all functionalities of the EV charger can be accomplished, namely: simultaneous charging (G2B) of two batteries; grid to HV battery (G2H) charging; grid to LV battery (G2L) charging; HV battery to LV battery (H2L) charging; and vehicle to grid (V2G) discharging. Moreover, a systematic design and optimization process of the integrated transformer is proposed using the analytical model and simulation. A new configuration of the planar transformer is achieved to enhance manufacturability, power density, and efficiency.

## *4. 1 Topology Study of the Three-Port DC-DC Converter*

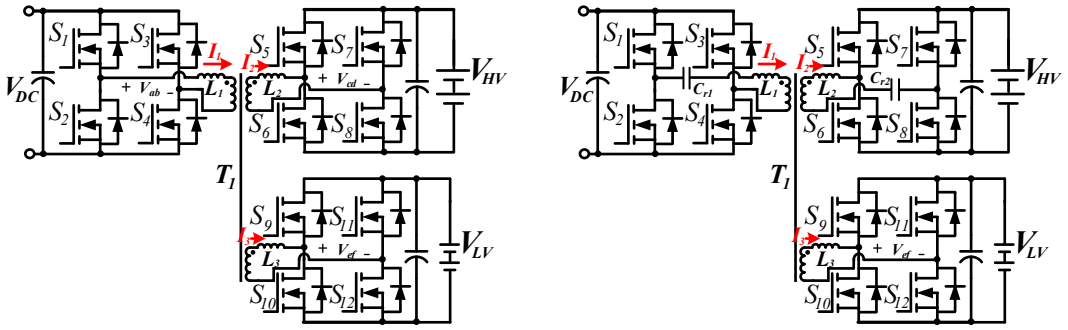
### 4. 1. 1 Topology Comparisons

A dual-output DC-DC converter is proposed in [35] to realize OBC and APM integration using pulse frequency modulation (PFM) [114]. The topology utilizes an integrated transformer to provide galvanic isolation and synthesis of a CLLC resonant converter with an LLC resonant converter. Even though the resonance can help achieve soft switching under the wider range of the load, it also creates higher voltage stress across the resonant capacitors. It is worth mentioning that the full-bridge CLLLC resonant converter can provide enough control variables to achieve G2B operation compared to the half-bridge CLLLC converter.

Thus, a thorough comparison between the full-bridge CLLLC resonant converter and the triple-active-bridge (TAB) converter needs to be conducted. They both can be considered as two viable options to integrate the OBC with the APM, which can realize the wide range voltage gain, bidirectional power flow, and zero-voltage-switching operation. The circuit diagrams are shown in Fig. 3-1. The major differences are summarized:

(1) In the TAB converter, the shim inductors are performed as the power transfer inductors, which leads to the winding currents with the piecewise-linear shape;

(2) In the CLLLC resonant converter, as shown in Fig. 3-1 (b), three resonant tanks are formed by the resonant capacitors and inductors from the CLLC and LLC converters. The output voltage regulation is realized by the frequency modulation. Therefore, the winding currents are close to sinusoidal waveforms.




(a) (b)

Fig. 4-1. The topology of two three-port DC-DC converters with the integrated transformer: (a) the TAB converter; (b) the CLLLC full-bridge resonant converter.

The TAB converter provides enough control flexibility for the control scheme. In a TAB converter, there are six independent control variables: three duty ratios ($\delta_1$, $\delta_2$, $\delta_3$) of three full bridges (primary, secondary and tertiary), the phase angle differences ($\varphi_2$, $\varphi_3$) between the primary-secondary and primary-tertiary bridge voltage waveforms, and the switching frequency. In a full bridge CLLLC resonant converter, the resonance can help achieve ZVS under a wide range of load variations; however, it creates higher voltage stress across the resonant capacitors ($C_{r1}$, $C_{r2}$). To sustain the voltage stress, multiple film capacitors are required to be placed in series, which will result in a design with larger size, higher cost, and lower reliability. To justify this claim, a simulation verification is conducted with the configuration summarized in Table 3-1. The resonant inductor in a CLLLC topology is larger than the TAB inductor, making it difficult to be integrated with the transformer. The efficiency can be examined through the winding current comparison, which is defined as,

$$OBJ = \sum_{i=1}^{3} {I_{L_i\,RMS}}^2 \tag{4.1}$$

It is reported from the simulation that the peak AC voltage on the resonant capacitor can be up to 1000V given the same power rating in the CLLLC converter, which means that a large capacitor bank is required. A radar chart on the performance comparison between a CLLLC full-bridge converter and a TAB converter is presented in Fig. 3-2.

Table 4-1. Simulated performance study between the CLLLC converter and the TAB converter.

| | $P_{HV}$ (W) | $P_{LV}$ (W) | $OBJ$ (A$^2$) | $L_{1\sim3}$ (μH) | $C_{r1\sim2}$ (nF) |
|---|---|---|---|---|---|
| CLLLC | 2188.7 | 1450 | 611 | 50 | 25.6 |
| TAB | 2200 | 1500 | 157.3 | 24 | N/A |

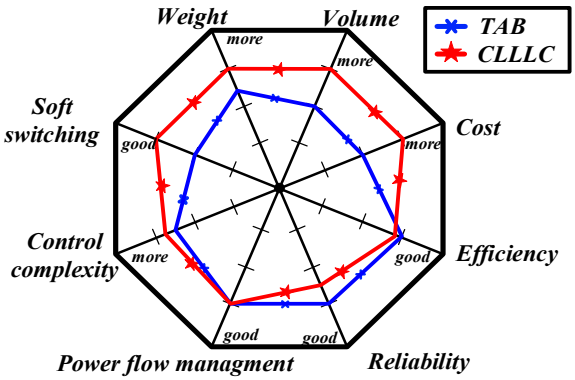



Fig. 4-2. The radar chart for the performance comparison between a CLLLC converter and a TAB converter.

4. 1. 2 Simultaneous Charging Architecture

In the conventional EV power system, the APM is a separate power unit that charges the LV battery from the HV battery. The power conversion efficiency of LV battery charging from the power grid can be defined as,

$$\eta_{G2L} = \eta_{G2V} \cdot \eta_{H2L} \tag{4.2}$$

where $\eta_{G2V}$ is the power conversion efficiency from the grid to the HV battery, which is around 94% [23]; $\eta_{H2L}$ is the APM efficiency, which is around 90% [115]. Thus, it is expected that

$\eta_{G2L}$ is <87% in the conventional charging system. On the other hand, the proposed integrated charger system enhances the G2L efficiency since the LV battery can be charged directly from the power grid with one DC-DC converter. Compared to the conventional charging method, it essentially reduces the power stage and improves the efficiency and power density.

## *4. 2 TAB Converter Basic Operation and Design Considerations*

Fig. 4-3 shows the topology of the TAB converter using a coupled three-winding integrated transformer $T_1$, where $T_1$ provides the power coupling of HV and LV sides, integration of leakage inductance and galvanic isolation. $L_{1\sim3}$ are the primary, secondary and tertiary power inductors, which are essential for power transfer and can be obtained through leakage inductance control of the integrated transformer. $S_{5\sim16}$ are the GaN MOSFETs in TAB converter, and the three winding turns are defined as $N_p$, $N_s$ and $N_t$, respectively. Considering the charging range of an EV HV traction battery $V_{HV}$ is from 200V to 500V, and that the auxiliary LV battery's nominal voltage $V_{LV,nominal} = 12V$, a three-winding transformer turns ratio is given as follows for simplicity and manufacturability.

$$N_p = N_s = 16\ ,\ N_t = 1 \tag{4.3}$$

where $N_p$, $N_s$ and $N_t$ are defined as primary, secondary and tertiary winding turns, respectively.

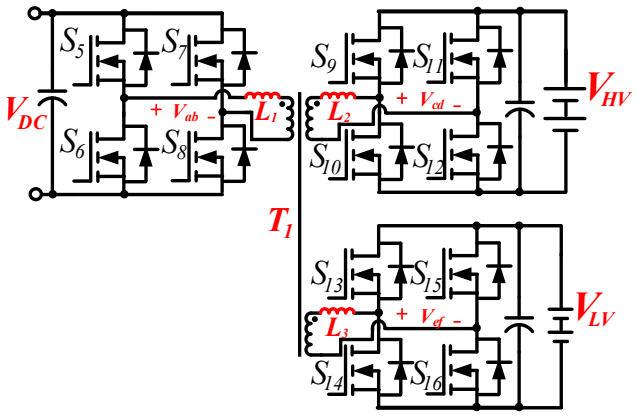



Fig. 4-3. The topology of a TAB converter with a coupled transformer structure.

4. 2. 1 Operation Modes Analyses

The triple phase shift (TPS) modulation scheme [116], which provides three control freedoms, is commonly utilized in a dual active bridge (DAB) converter to achieve optimal operation [117]. Note that a dual-output triple active bridge cannot be viewed as two independent dual active bridge converters due to the nature of multi-directional power flow. For the TAB converter, there are five independent control variables: three duty ratios ($\delta_1, \delta_2, \delta_3$) of three full-bridges (primary, secondary and tertiary) and the phase angle differences ($\varphi_2$, $\varphi_3$) between the primary-secondary and primary-tertiary fundamental bridge voltage waveforms, where the three bridge voltages are illustrated in Fig. 4-4.

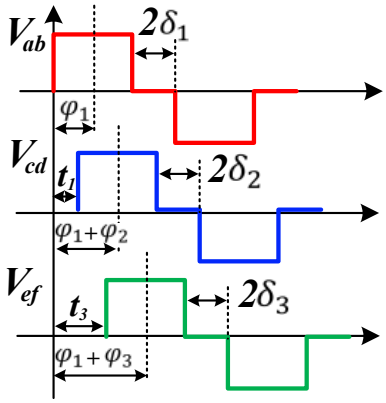



Fig. 4-4. The bridge voltages with respect to five control variables.

$\varphi_2$ is defined as the phase difference between primary and secondary bridge voltages and $\varphi_3$ is the phase difference between secondary and tertiary bridge voltages. The phase differences and duty ratios adjust the shape of bridge voltages and further affect the power inductor current, which results in ten different operation modes depending on the winding current shape.

4. 2. 2 Design Consideration

The power transfer requirement is fundamentally considered at the beginning of the design process. The power flow for the active-bridge-based converter is determined by the power inductor [118], which can be expressed as,

$$L_{path} < \frac{V_{in}V_o\, D\, (1-D)}{2Nf_sP_{path}} \tag{4.4}$$

where $L_{path}$ is denoted as the power inductor in each power loop; $P_{path}$ is defined as the transferred power in each power loop; $D$ is the phase shift between two bridge voltages and is related with $\varphi$; $N$ is the turns ratio of the transformer in the loop. The formation and modelling of power loops will be discussed in a later section.

The magnetizing inductance of the transformer needs to be very large (i.e., $1mH$), which leads to a large impedance when operating at high frequency. Thus, the current flowing through the magnetizing inductor is negligible, making it possible for the desired power transfer. For instance, the total magnetizing inductance can be expressed as,

$$L_{m\_total} > 1mH \tag{4.5}$$

If two pairs of magnetic cores are utilized, the magnetizing inductance for each pair is given by,

$$L_{m\_each} > 0.5mH \tag{4.6}$$

Eq. (4.6) gives a general guide for the transformer design. Furthermore, the switch selection is based on the current and voltage level under the worst scenario. The number of PWM channels and ADC channels is determined by the control and observability of the system, which is listed in Table 4-2. In terms of the requirements, sufficient ADC channels and adequate conversion accuracy needs to be guaranteed. More importantly, enough PWM channels are desired with the capability of phase shift and duty ratio adjustment in the microcontroller unit (MCU).

Table 4-2. The required number of PWM and ADC channels and their specifications.

| ADC channels | PWM channels |
|---|---|
| PFC input voltage | Two complementary PWMs on the PFC stage |
| PFC input current | Two complementary PWMs on TAB primary side |
| PFC DC link voltage | Two complementary PWMs on TAB secondary side |
| HV/LV output voltages/currents | Two complementary PWMs on TAB tertiary side |

As can be seen from Table 4-2, the minimum number for ADC channels is 7, which should provide at least 10 bits resolution (i.e., 0.1% of full scale). Meanwhile, the total number of 8 PWM channels is required. Apart from the requirements rising from PWM and ADC channels, the system clock needs to be fast and the code execution must be finished by 10 μs in order to enable the 100kHz sampling; otherwise, it will lead to the under-sampling condition and even the instability. Typically, the following equation holds true,

$$execution\ time \propto f_{clock} \tag{4.7}$$

This implies that MCU (with PFC control) should have a clock frequency above ~110MHz. Thus, TI dual-core 32-bit MCU TMS320F28379D is selected with the clock frequency of 200MHz. It has 24 pulse width modulator (PWM) channels with enhanced features and up to 24 channels of analog-to-digital converters (ADCs).

## *4. 3 Phase-Shift and Duty-Ratio Combined Control*

Considering the cross-couplings of power flow among different ports, classical control loops implemented in dual active bridge converters are inapplicable. Conventionally, the control strategy for an active-bridge-based converter involves phase shift modulation [119] of switches, which brings convenience for circuit modeling and control loop design. However, the integrated DC-DC conversion stage of the proposed converter is a three-port network

consisting of one input and two outputs. Due to the nature of multi-directional power flow, this control method suffers from high circulating power in the tank, especially when the converter operates at high power rating, which results in high conduction loss and demanding hardware design.

To overcome the high current circulation issue, a comprehensive phase shift and duty ratio combined control strategy is proposed in this work, which is capable of simultaneously charging of both HV and LV batteries from the grid (G2B). This strategy enables all the functionalities, including grid to HV battery (G2H) charging, grid to LV battery (G2L) charging, HV battery to LV battery (H2L) charging and vehicle to grid (V2G) discharging. Among them, G2B is the most challenging as it involves five control variables. The control strategy can be formed from both the detailed modeling and power loop analyses. The control target is to pursue high efficiency at the G2B operation while maintaining tight regulation for both HV and LV side outputs. Thus, two control methods are proposed and discussed in this work. The effectiveness of the proposed methods is verified through simulations.

### 4. 3. 1 Decoupled Power Circuits

For G2B operation, it is difficult to analyze the equivalent circuit reflected to the primary side since all the power loops are coupled with each other, as shown in Fig. 4-5. $L_m$ is the magnetizing inductor of the transformer. It is worth mentioning that the system can be viewed as a network of inductors driven by voltage sources with controlled phase displacements and duty cycles. Each bridge voltage contains different phase information, for convenience, $V_{pri}$ occurs with the zero phase. The primary, secondary and tertiary bridge voltages are the bipolar quasi-square waves with different phase shifts.

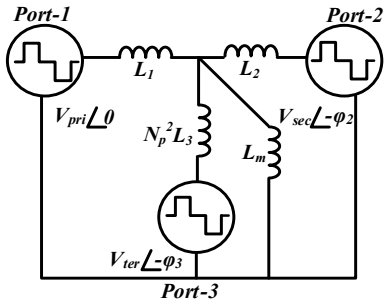



Fig. 4-5. Coupled power loops in the TAB converter.

Thus, for the purpose of decoupling, the topology of a TAB-based converter is transformed into a delta configuration, as shown in Fig. 4-6. The primary, secondary and tertiary bridge voltages are the bipolar quasi-square waves with different phase shifts. Note that the magnetizing inductance of the transformer can be ignored in the equivalent circuit without any loss in generality since it is much greater than leakage inductances. The equivalent inductances are expressed in Eq. (4.8).

$$\begin{cases} L_{12} = L_1 + L_2 + \frac{L_1 L_2}{N_p^2 L_3} \\ L_{23} = L_2 + N_p^2 L_3 + \frac{L_2 N_p^2 L_3}{L_1} \\ L_{13} = L_1 + N_p^2 L_3 + \frac{L_1 N_p^2 L_3}{L_2} \end{cases} \tag{4.8}$$

where $L_1$, $L_2$ and $N_p^2 L_3$ are the primary, secondary and tertiary power inductors reflected to the primary side, respectively. Note that the power flowing through each port remains unchanged under delta configuration, which yields to,

$$\begin{cases} P_1 = -(P_{12} + P_{13}) \\ P_2 = P_{12} - P_{23} \\ P_3 = P_{13} + P_{23} \end{cases} \tag{4.9}$$

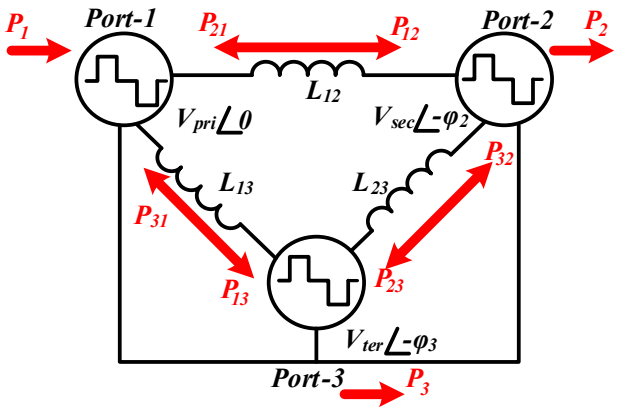



Fig. 4-6. The delta equivalent configuration of a TAB-based converter.

4. 3. 2 Modeling of a TAB Converter

The piece-wise-linear based modeling may not be appropriate for a TAB converter due to the complexity of its operation modes. Instead, the modeling of the system needs to be conducted from the frequency domain using harmonic analysis. In practice, Fundamental Harmonic Approximation (FHA) is commonly used for modeling of DC-DC resonant converters [120], which works accurately near the resonant frequency point. However, for the PWM-based converter, the accuracy of FHA would be reduced as the waveforms are no longer sinusoidal, which leads to the ignorance of large amounts of higher harmonic components. Therefore, a proper modeling technique should include the influence of other odd-order harmonic terms in the bridge voltages [121], which can compute accurate information regarding the current RMS value and shape without the loss of generality. The basic idea of the Generalized Harmonic Approximation (GHA) is to establish a set of equivalent circuits concerning different odd-order harmonics, where the amplitude and the RMS value of inductor current at each order can be calculated accordingly. In addition to the fundamental harmonic approximation, the GHA model of the TAB converter considers higher odd-order harmonic components that lead to a series of equivalent circuits with respect to the order of harmonics. First, the bridge voltage amplitude needs to be synthesized. Consequently, the transferred

power and inductor current are derived as the summations of different odd-order harmonic components.

The amplitudes of $V_{ab}$, $V_{cd}$ and $V_{ef}$ can be derived in the forms of generalized harmonics and they are not related to any phase information, according to Fig. 4-4. Therefore, the sets of amplitudes are expressed as,

$$< V_{p,k} > = < V_{ab,k} > = \frac{4V_{DC}\cos(k\delta_1)}{k\pi} \tag{4.10}$$

$$< V_{s,k} > = < V_{cd,k} > = \frac{4V_{HV}\cos(k\delta_2)}{k\pi} \tag{4.11}$$

$$< V_{t,k} > = < V_{ef,k} > = \frac{4N_pV_{LV}\cos(k\delta_3)}{k\pi} \tag{4.12}$$

where $k$ represents the order of harmonics (i.e., 1, 3, 5….). Consequently, the phase diagram for the bridge voltages and inductor currents, and the corresponding equivalent circuits are shown in Fig. 4-7 for the $k^{th}$ harmonic component. Besides, $\theta_{12,k}$ is denoted as the phase between the primary voltage and the current flowing through $L_{12,k}$. Based on the trigonometric relation, $\theta_{12,k}$ is derived as follows,

$$\theta_{12,k} = arctan\left(\frac{<V_{p,k}> - <V_{s,k}>\cos(\varphi_{2,k})}{<V_{s,k}>\sin(\varphi_{2,k})}\right) \tag{4.13}$$

where $\varphi_{2,k}$ represents the $k^{th}$ harmonic component for the phase shift, which is equal to $k\varphi_2$. Similar definitions are applied to $\theta_{13,k}$ and $\theta_{23,k}$.

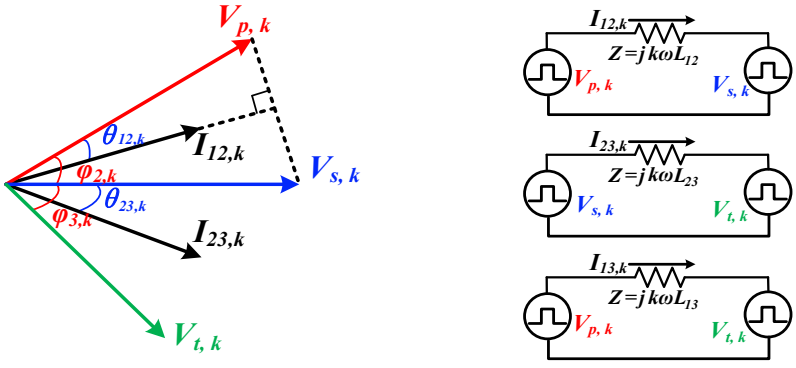



Fig. 4-7. Phase diagrams of the bridge voltages and inductor currents and the corresponding equivalent circuits.

The phase diagrams illustrate how the active power transferred to each port can be determined in the delta configuration. Considering the summation of each odd-order component, the total powers are expressed as,

$$P_{12} = \sum_{k=1}^{2i+1} \frac{<V_{p,k}><V_{s,k}>\sin(k\varphi_2)}{4k^2\pi f_s L_{12}} \tag{4.14}$$

$$P_{23} = \sum_{k=1}^{2i+1} \frac{<V_{s,k}><V_{t,k}>\sin(k(\varphi_3-\varphi_2))}{4k^2\pi f_s L_{23}} \tag{4.15}$$

$$P_{13} = \sum_{k=1}^{2i+1} \frac{<V_{p,k}><V_{t,k}>\sin(k\varphi_3)}{4k^2\pi f_s L_{13}} \tag{4.16}$$

where $2i+1$ represents the maximum index of odd-order harmonics.

Likewise, the amplitudes of inductor currents can be calculated using the existing variables. In Fig. 4-7, the inductor current amplitude of the $k^{th}$ harmonic component is given by,

$$<I_{12,k}> = \frac{\sqrt{<V_{p,k}>^2+<V_{s,k}>^2-2<V_{p,k}><V_{s,k}>cos(k\varphi_2)}}{2k^2\pi f_s L_{12}} \tag{4.17}$$

$$<I_{23,k}> = \frac{\sqrt{<V_{s,k}>^2+<V_{t,k}>^2-2<V_{s,k}><V_{t,k}>cos(k(\varphi_2-\varphi_3))}}{2k^2\pi f_s L_{23}} \tag{4.18}$$

$$<I_{13,k}> = \frac{\sqrt{<V_{p,k}>^2+<V_{t,k}>^2-2<V_{p,k}><V_{t,k}>cos(k\varphi_3)}}{2k^2\pi f_s L_{13}} \tag{4.19}$$

The final step is to synthesize the actual current waveforms from the decoupled loop results. The instantaneous current expressions are presented as,

$$I_{RMS,12} = \sqrt{\sum \frac{<I_{12,k}>^2}{2}} \tag{4.20}$$

$$I_{RMS,23} = \sqrt{\sum \frac{<I_{23,k}>^2}{2}} \tag{4.21}$$

$$I_{RMS,13} = \sqrt{\sum \frac{<I_{13,k}>^2}{2}} \tag{4.22}$$

By means of the GHA-based modeling technique, the bridge current and voltage amplitudes can be obtained accurately. Besides, the corresponding time-domain waveforms can also be computed with the help of the phase diagram, which is fundamentally important for the control implementation and synthesis of ZVS constraints.

$$V_p(t) = \sum_{k=1}^{2i+1} < V_{p,k} > \sin(k\omega_s t) \tag{4.23}$$

$$V_s(t) = \sum_{k=1}^{2i+1} < V_{s,k} > \sin(k\omega_s t - k\varphi_2) \tag{4.24}$$

$$V_t(t) = \sum_{k=1}^{2i+1} < V_{t,k} > \sin(k\omega_s t - k\varphi_3) \tag{4.25}$$

Similarly, the current expressions in the time domain are achieved as,

$$I_{12}(t) = \sum_{k=1}^{2i+1} < I_{12,k} > \sin(k\omega_s t - \theta_{12,k}) \tag{4.26}$$

$$I_{23}(t) = \sum_{k=1}^{2i+1} < I_{23,k} > \sin(k\omega_s t - \theta_{23,k} - k\varphi_2) \tag{4.27}$$

$$I_{13}(t) = \sum_{k=1}^{2i+1} < I_{13,k} > \sin(k\omega_s t - \theta_{13,k}) \tag{4.28}$$

The final step is to synthesize the actual current waveforms from the decoupled loop results. It is worth mentioning that the bridge voltages are not affected by the decoupled configurations. The instantaneous current expressions are presented as,

$$I_{L_1}(t) = I_{12}(t) + I_{13}(t) \tag{4.29}$$

$$I_{L_2}(t) = I_{12}(t) - I_{23}(t) \tag{4.30}$$

$$I_{L_3}(t) = I_{13}(t) + I_{23}(t) \tag{4.31}$$

where $I_1(t)$, $I_2(t)$ and $I_3(t)$ represent the primary, secondary and tertiary winding current in the coupled power loops, respectively. Fig. 4-8 gives the computation results from the GHA-based model. The HV power is set as 2700W, and the LV power is set as 1000W for each module. The leakage inductance is given as $20uH$. The switching frequency is set as 100kHz. It is observed that the analytical waveforms are in consistency with the simulated waveforms in terms of shape and amplitude, which confirms the effectiveness of the proposed modelling technique.

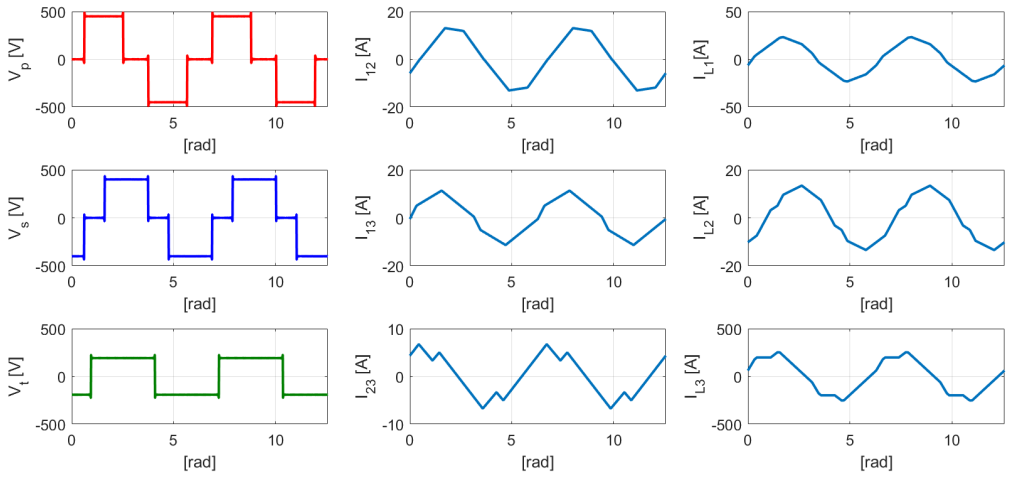



Fig. 4-8. The computed waveforms of the bridge voltage and inductor current in TAB converter.

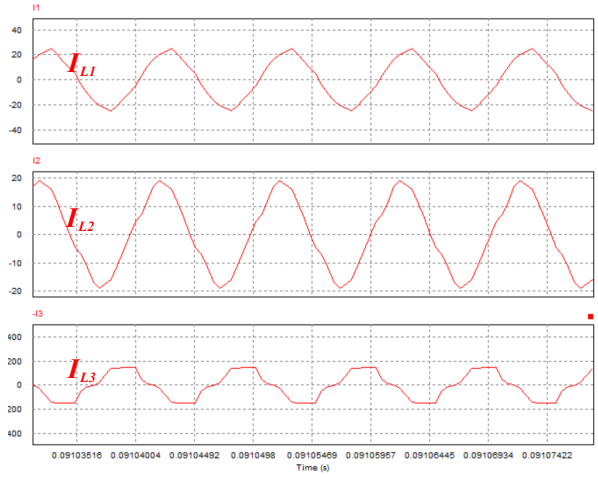



Fig. 4-9. The simulated inductor currents with the same angle information and circuit parameters.

Moreover, a scaled-down experiment prototype is built and tested to validate the GHA-based model, as illustrated in Fig. 3-10. Three full bridge modules are developed with the voltage/current sensors and connected with a three-winding transformer to form a TAB converter. The control strategy is implemented with five degrees of control variables, i.e., the phase displacements and the duty cycles. The optimum operating points are calculated

numerically in advance and are stored in the DSP as lookup tables with the current reference signals as the indexes.

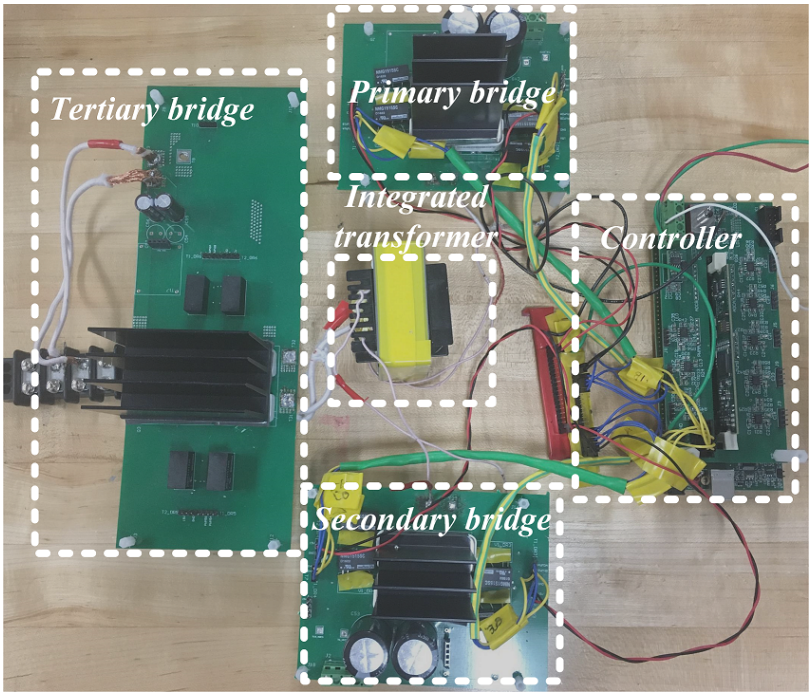



Fig. 4-10. The assembled experimental set-up for the TAB converter.

Given $k = 61$, all the harmonic components are calculated and summed. From the computation, the harmonic components higher than $61^{th}$ are negligible. The extracted waveforms from the experiment exhibit good consistency with the predicted waveforms from the GHA-based model, including the amplitude and phase information, as shown in Fig. 3-11.

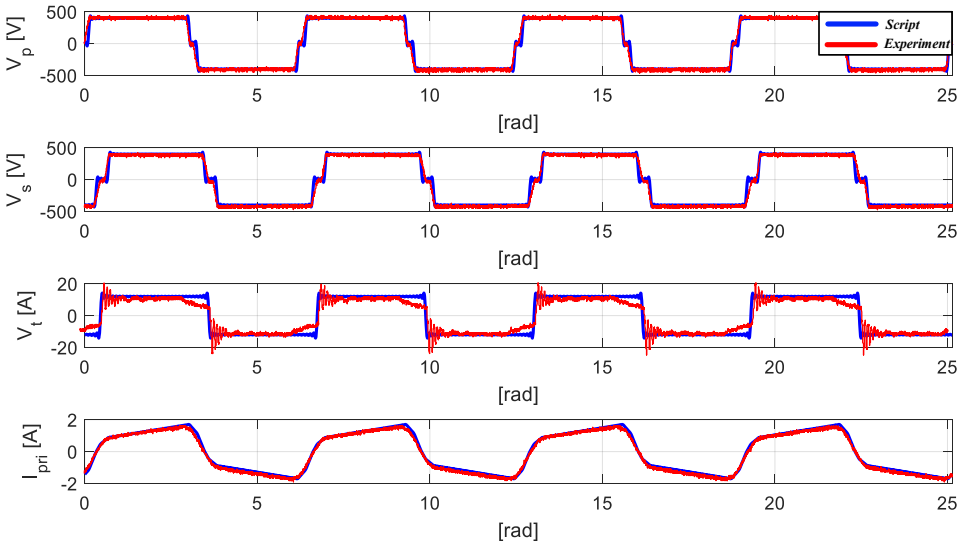



Fig. 4-11. The comparison waveforms between the prediction and the experiment. The operation power is 400W with 400V $V_{HV}$ and 12V $V_{LV}$.

### 4. 3. 3 Control Loop Design

In this section, two control loop designs are proposed for the voltage/current regulation and efficiency improvement, both of which are theoretically supported. The first control loop design is focused on the minimization of the circulating power using the power balance concept. The second one is to achieve the optimum sets of control variables to reduce the winding currents using the GHA model. The details are discussed below.

#### 4. 3. 3. 1 Circulating Power-Oriented Loop

The first control loop is established based on the minimization of the circulating power. The control scheme with the three-loop structure is shown in Fig. 4-12 to achieve simultaneous charging while maintaining tight voltage regulations. $\varphi$ represents the phase shift control variable, and $\delta$ represents the duty ratio control variable. The computation block gives a real time feedback for $\delta$ control, which is derived from the ZVS constraint considering the charging and discharging of the MOSFET output capacitors.

$$\cos(\delta_1) = \frac{M\left(\frac{\pi^2}{2} f_s \sqrt{2C_{OSS}L_{12}}\right)}{1-sin\varphi_2} \tag{4.32}$$

$$\cos(\delta_2) = \frac{\cos(\delta_1)}{M} \tag{4.33}$$

where $M$ is denoted as the input/output voltage ratio and $C_{OSS}$ is the output capacitor of the switch.

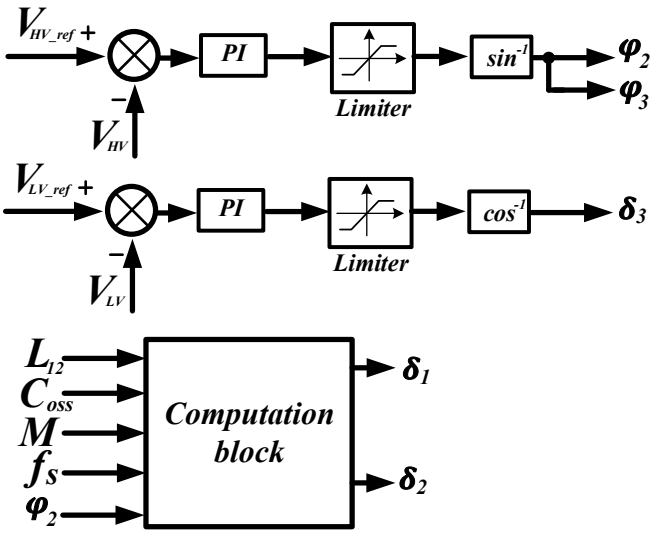



Fig. 4-12. The proposed control loop configuration implemented with both $\varphi$ and $\delta$ control.

In order to control the power flow towards the two output ports as well as to achieve output voltage regulations, the proposed control methodology uses up-to five independent control variables: three duty ratios ($\delta_1, \delta_2, \delta_3$) of three full-bridges (primary, secondary and tertiary) and two phase angle differences ($\varphi_2$, $\varphi_3$) between the primary-secondary and primary-tertiary fundamental bridge voltage waveforms, respectively. As shown in Fig. 4-6, both $P_{12}$ and $P_{32}$ involve the control variable $\varphi_2$, which implies that the phase angle $\varphi_2$ can be used as a control variable for the port-2 output voltage regulation. To minimize the circulating active power, the modulus sum of power transferred between ports needs to be suppressed,

$$f(\delta_1, \delta_2, \delta_3, \varphi_1, \varphi_2, \varphi_3) = Min\{|P_{12}| + |P_{23}| + |P_{31}|\} \tag{4.34}$$

On the other hand, there are some restrictions on the reactive power control. Because of the three-port structure, reactive power flows between ports are not inherently equal, which

needs the boundary condition of the $\delta$ control variable. $\varphi_1$ is set as 0 to obtain maximum power flow capability. By applying $\varphi_2 = \varphi_3$, no circulating active power flows between port-2 and port-3. $\delta_3$ is utilized for LV side voltage regulation. One quick solution of Eq. (4.35) can be obtained by reducing one freedom of control variable,

$$\varphi_1 = 0, \ \varphi_2 = \varphi_3 \tag{4.36}$$

Fig. 4-13 shows the mode transients from G2H to simultaneous charging using the proposed control. The HV load is set as 80ohm, and the LV load is set as 0.1ohm. As can be seen from the figure, the overshoot is suppressed in both HV and LV output voltages. The settling time of the LV side is ~30ms due to the large current, which shows a good dynamic performance.

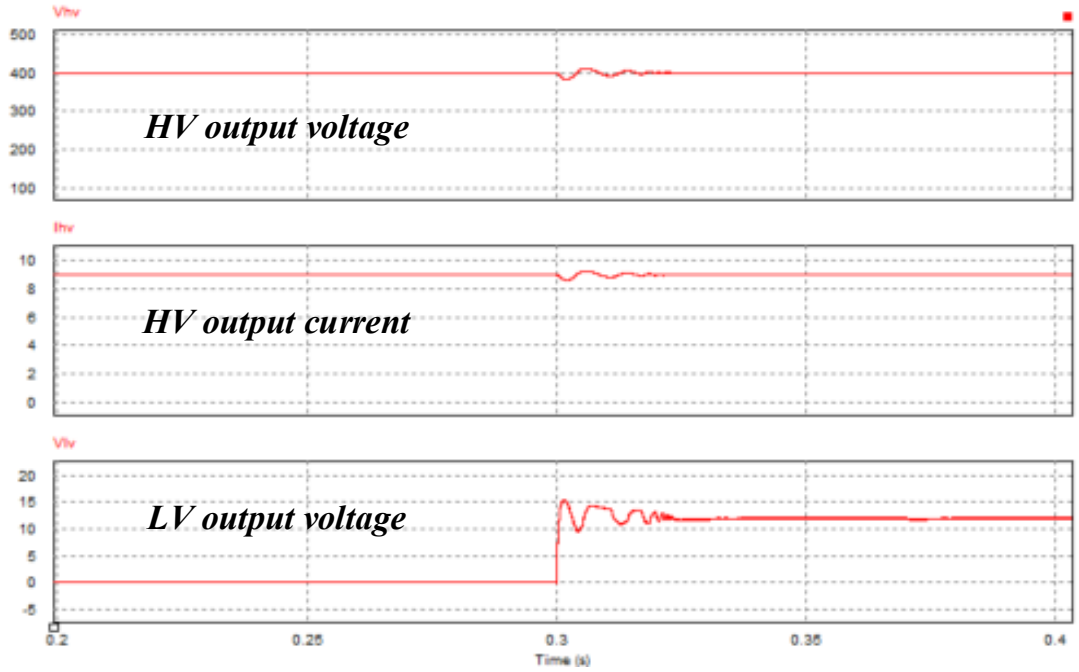



Fig. 4-13. Mode transients from G2H to simultaneous charging.

4. 3. 3. 2 Current-Oriented Loop

With the help of the GHA-based model, a current-oriented control loop is proposed to minimize the RMS value of the circulating current. $\varphi_1$ is selected as 0 to obtain maximum

power flow capability. Given a practical range of $\delta_1, \delta_2, \delta_3, \varphi_2, \varphi_3$ (i.e., [0, π/2]), the RMS winding currents can be computed using Eq. (4.29)-(4.31) with the iteration of harmonic orders. Thus, the optimum solution can be obtained using the objective function below,

$$f(I_{rms}) = {I_{L_1\,RMS}}^2 + {I_{L_2\,RMS}}^2 + {I_{L_3\,RMS}}^2 \tag{4.37}$$

It is worth mentioning that the optimization process can be further conducted considering the influence of the power inductors in the TAB converter. There is a power transfer constrain rising from the power inductance value. Note that the sweep of power inductance values can be achieved in the outer iteration loop. The detailed flowchart is shown in Fig. 4-14, where the power transfer requirements are expressed as,

$$P_{HV} = P_{12} - P_{23} \tag{4.38}$$

$$P_{LV} = P_{13} + P_{23} \tag{4.39}$$

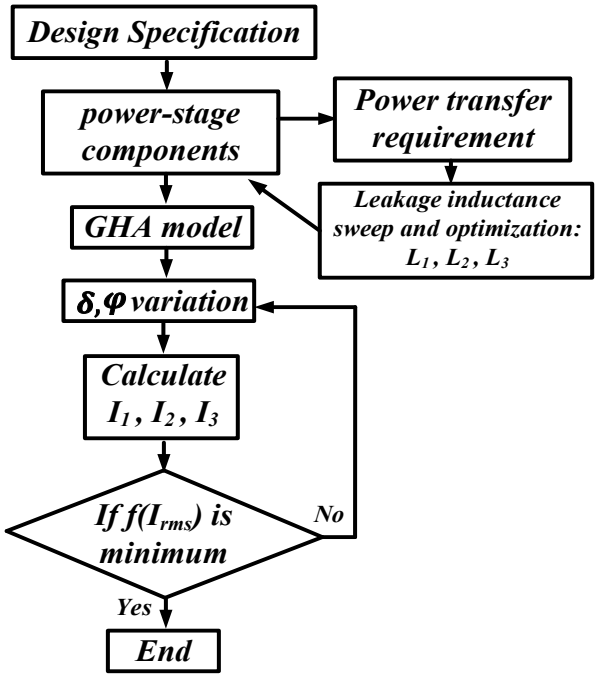



Fig. 4-14. The flowchart of the proposed current-oriented control loop.

The real-time computation results concerning $\delta_1, \delta_2, \delta_3, \varphi_2, \varphi_3$ are obtained as the control variables in this loop. The output voltage regulation is automatically achieved once the required

power is satisfied in the analyses. Therefore, this method can be viewed as an alternative control strategy to pursue high efficiency and minimize the circulating currents, but also requires massive computation capability in MCU.

As shown in Fig. 4-14, the constraint comes from the power transfer requirement for both HV and LV sides. On the one hand, for a single power branch, the large leakage inductance reduces the RMS current due to the flat waveform shape. However, since the TAB converter has three coupled power branches, this statement may not hold true. Therefore, based on the RMS current optimization, the leakage inductance sweep is conducted to further optimize the system performance.

Given the initial leakage inductance range using the power transfer estimation, the optimal leakage inductance is obtained. Fig. 4-15 illustrates the leakage inductance sweep at $P_{HV} = 2000W, P_{LV} = 1700W$.

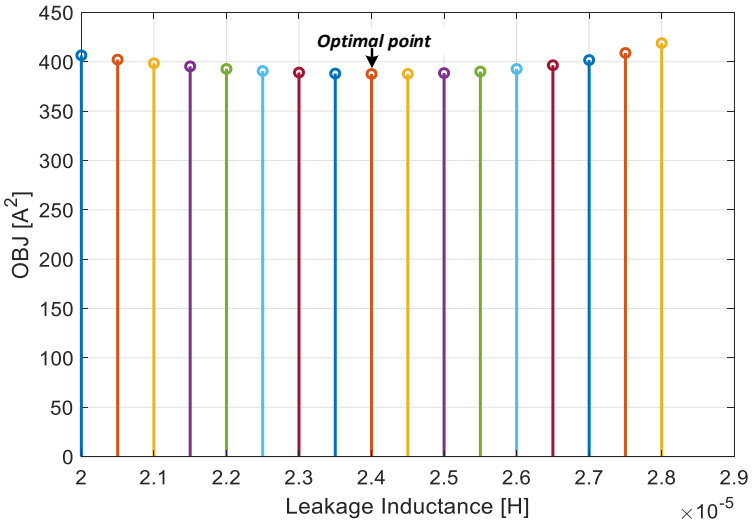



Fig. 4-15. Leakage inductance sweep while satisfying the power transfer requirements.

Moreover, considering the power flow management at full power, the sweep is conducted with the variation of $P_{HV}$. It is confirmed that $L_{leakage} = 24\mu H$ is the optimal solution for all the operation points, as shown in Fig. 4-16.

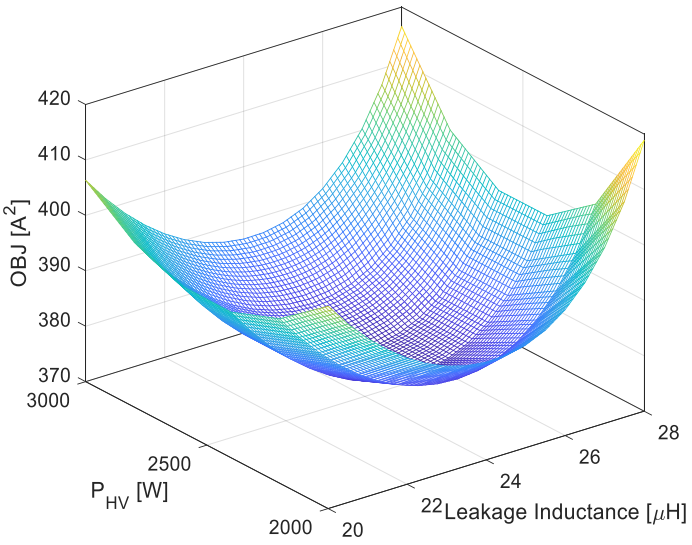



Fig. 4-16. 3D leakage inductance sweep considering the $P_{HV}$ variation.

### 4. 3. 4 ZVS Constraints

Based on the proposed GHA-based TAB converter model, the phase and amplitude information of winding currents and bridge voltages are obtained. Thus, soft switching can be examined considering the polarity of the winding current, which is of significance in GaN device high switching operation to ensure that the system efficiency will not be compromised. A set of typical waveforms using the optimization algorithm is shown in Fig. 4-17 to illustrate the ZVS conditions.

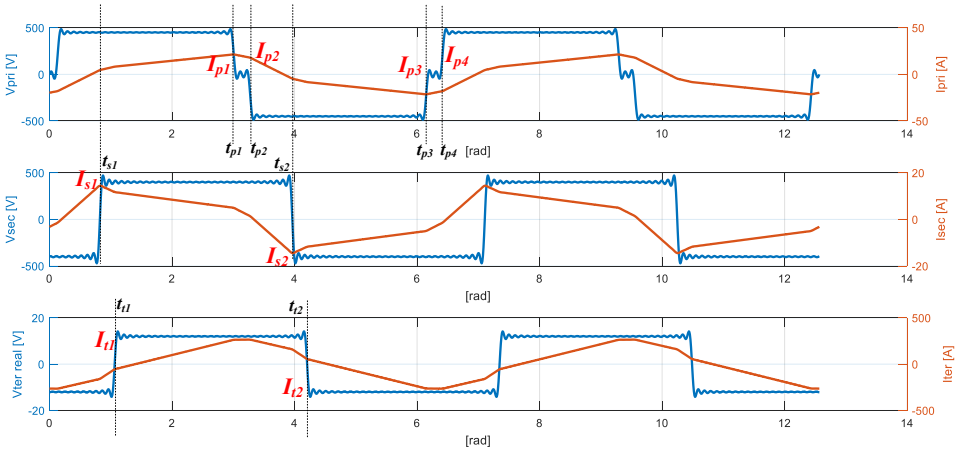


Fig. 4-17. Computed TAB converter bridge voltages and currents under the RMS current optimization. Each module has the power transfer of: $P_{HV} = 2000W;\ P_{LV} = 1700W$.

As shown in the figure, ZVS can be achieved in both primary and secondary bridges. However, due to the high step-down ratio of tertiary winding, it is relatively difficult for the tertiary bridges to maintain the ZVS condition for every operation point following the examination criteria, which are summarized in Table 4-3,

Table 4-3. ZVS examination criteria.

| Current direction | Condition |
|---|---|
| $I_{s1} > 0$ | ZVS |
| $I_{p1} > 0$ | ZVS |
| $I_{p1} > 0$ | ZVS |
| $I_{s2} < 0$ | ZVS |
| $I_{p3} < 0$ | ZVS |
| $I_{p4} < 0$ | ZVS |
| $I_{t1} < 0$ | NO ZVS |
| $I_{t2} > 0$ | NO ZVS |

Therefore, ZVS constraints can be implemented considering the polarity of the winding currents during switching. Moreover, considering that circulating energy contributes to the switching loss, another ZVS constraint can be formed when there is no circulating active power flow between port-2 and port-3 ($\varphi_2 = \varphi_3$),

$$P_{23} = 0 \tag{4.40}$$

Since satisfying Eq. (3.39) is not a necessary condition for achieving ZVS, it can be added as a separate factor in the objective function. Therefore, the new objective function $f_2(I_{rms})$ is synthesized as,

$$f_2(I_{rms}) = {I_{L_1\,RMS}}^2 + {I_{L_2\,RMS}}^2 + {I_{L_3\,RMS}}^2 + KP_{23} \tag{4.41}$$

where $K$ is the weight coefficient for the zero circulating power flow.

4. 3. 5 Extended Operation Range

Based on the required maximum current rating, a comprehensive comparison between the $\varphi\ \delta$ control and $\varphi$ control is obtained considering the difference in the operation ranges.

Compared to the $\varphi$ control method, the $\varphi\ \delta$ control method achieves an extended operation range for HV and LV battery charging. Take an example of a 11kW charger configuration with a 48kWh HV battery, where each module has a 3.7kW power rating. Fig. 4-18 gives a comparison of the operation range between $\varphi\ \delta$ control and $\varphi$ control. As seen from the figure, the proposed control method enables a wide operation range of HV and LV batteries, especially under the unbalanced loads conditions.

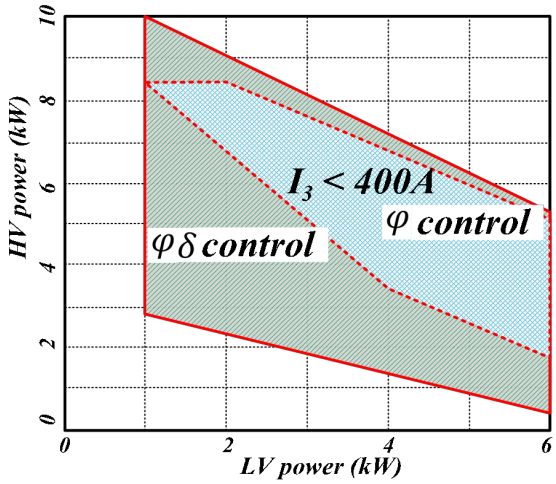
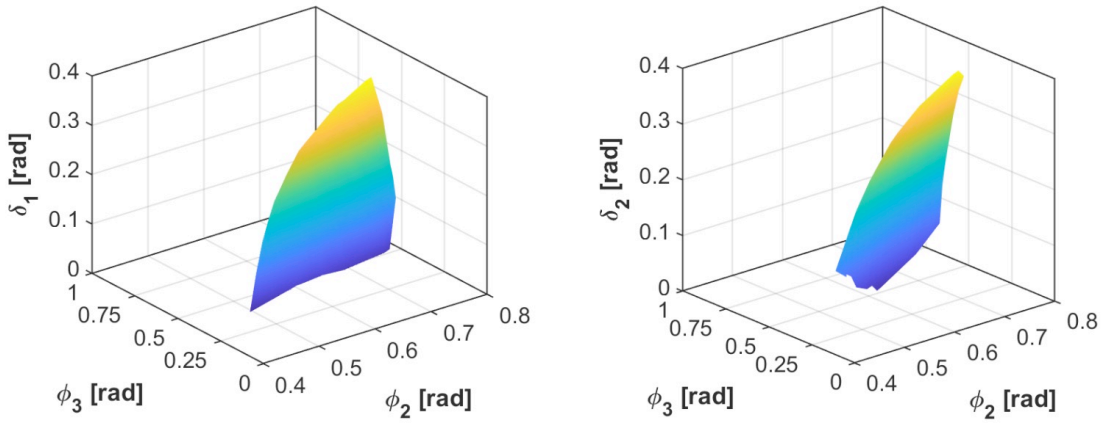



Fig. 4-18. The comparison of operation range between $\varphi$ control and $\varphi\ \delta$ control.

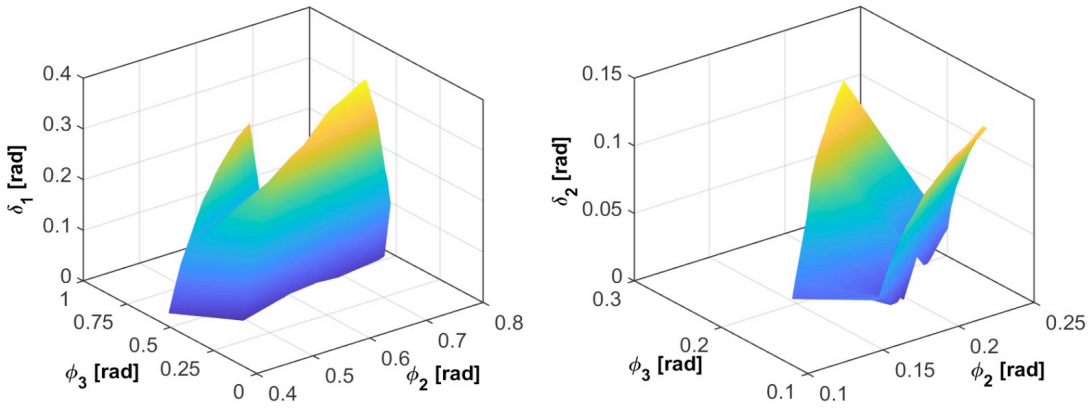
Under the full power operation, the increase of $P_{HV}$ would lead to the reduced operation ranges of all the control variables $\delta_1, \delta_2, \delta_3, \varphi_2, \varphi_3$ due to high-step-down characteristics at the light load of the tertiary side. Meanwhile, a narrow range would lead to a higher RMS current using the proposed optimization algorithm. As a verification, an exhaustive study of the control variable ranges is investigated, which is essentially important to determine the

variable range for the optimization. Note that in order to achieve the maximum allowable power transfer, $\delta_1$ is set as 0. Fig. 4-19 and Fig. 4-20 show the comparison results regarding the variable ranges for two sets of power operation points.




(a) (b)

Fig. 4-19. 3D surface of the operation ranges for the control variables when $P_{HV} = 3000W, P_{LV} = 700W$: (a) with respect to $\delta_1$; (b) with respect to $\delta_2$.




(a) (b)

Fig. 4-20. 3D surface of the operation ranges for the control variables when $P_{HV} = 2000W, P_{LV} = 1700W$: (a) with respect to $\delta_1$; (b) with respect to $\delta_2$.

Moreover, the power sweep is based on the power ratio between the HV port and the LV port. The ratio of $P_{HV}$ and $P_{LV}$ can be expressed as,

$$\gamma = \frac{P_{HV}}{P_{LV}} = \frac{\sum_{k=1}^{2i+1} <V_{p,k}> <V_{s,k}> \sin(k\varphi_2) - <V_{s,k}> <V_{t,k}> \sin(k(\varphi_3 - \varphi_2))}{\sum_{k=1}^{2i+1} <V_{p,k}> <V_{t,k}> \sin(k\varphi_3) + <V_{s,k}> <V_{t,k}> \sin(k(\varphi_3 - \varphi_2))} \quad (4.42)$$

where $\gamma$ is defined as the power ratio between two outputs. Based on the statistic results computed from the GHA modeling in Fig. 3-20 and Fig. 3-21, it is observed that given the same total power rating at G2B mode, the decrease of $\gamma$ would lead to the reduced operation range of control variables and increased winding currents due to high step-down characteristics of the tertiary side.

Moreover, the state-of-charge (SoC) map is given in Fig. 4-21, describing the relationship of charging modes (CC, CP, CV) and operation modes (G2B, G2V, G2L). It is observed that the simultaneous charging is enabled during CC mode, where the output current is regulated and raises the battery terminal voltage until the upper charge voltage limit is reached when the current drops due to saturation.

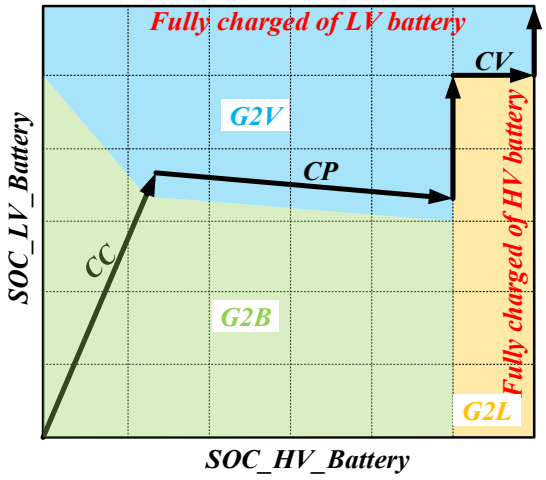



Fig. 4-21. The SoC mapping in terms of different charging stages.

## *4. 4 Experimental Verification*

To verify the proposed theoretical hypothesis, a GaN-based integrated onboard charger module hardware is developed with the power rating of 3.7kW. The GaN Systems GS66516T switches are utilized for the primary and secondary bridge. The proof-of-concept image are shown in Fig. 4-22. The module is composed of the EMI filter stage, the totem-pole PFC rectifier, the TAB converter, the MCU, and the auxiliary power supply for the gate and sensor signals.

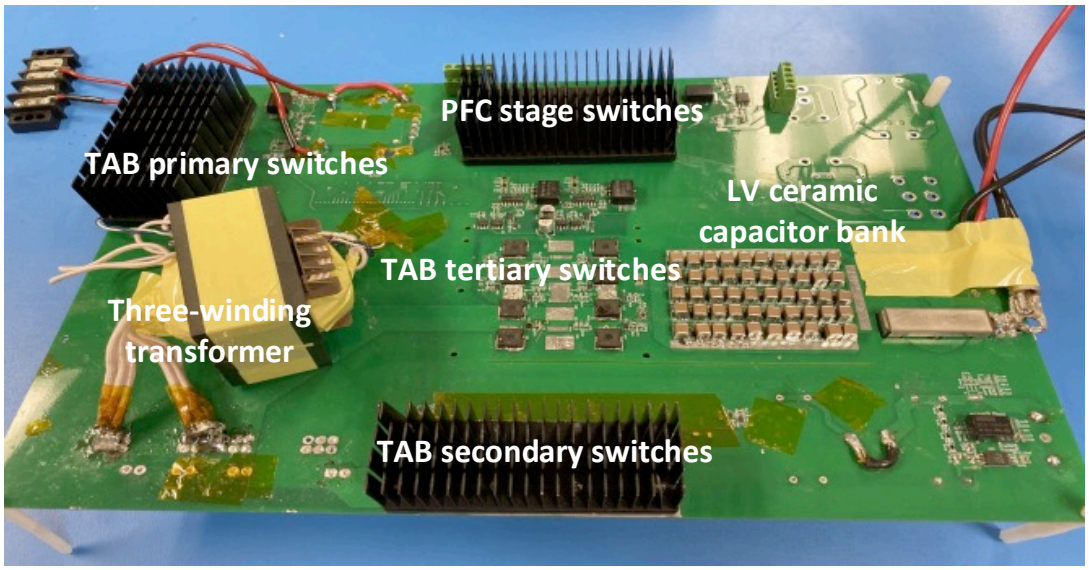



Fig. 4-22. One modular system: the hardware prototype.

### 4. 4. 1 Simultaneous Charging of HV and LV Batteries

The G2B operation mode is verified experimentally using the proposed current-oriented control technique. As shown in Fig. 4-23, the steady-state waveforms of the G2B mode are achieved at 2.5kW. The tertiary winding current is measured up to 39.3A using the hall-effect current probe. The power distribution of this testing condition is: $P_{HV}$ = 2095W, $P_{LV}$ = 290W. The HV resistance is 47$\Omega$, and the LV resistance is 0.33 $\Omega$. Low profile ceramic capacitor bank is employed in the tertiary output side to suppress the output voltage ripple while maintaining

high efficiency. It is observed that the there is some ringing in the tertiary bridge voltage, which is caused by the parasitic capacitance reflected to the tertiary side.

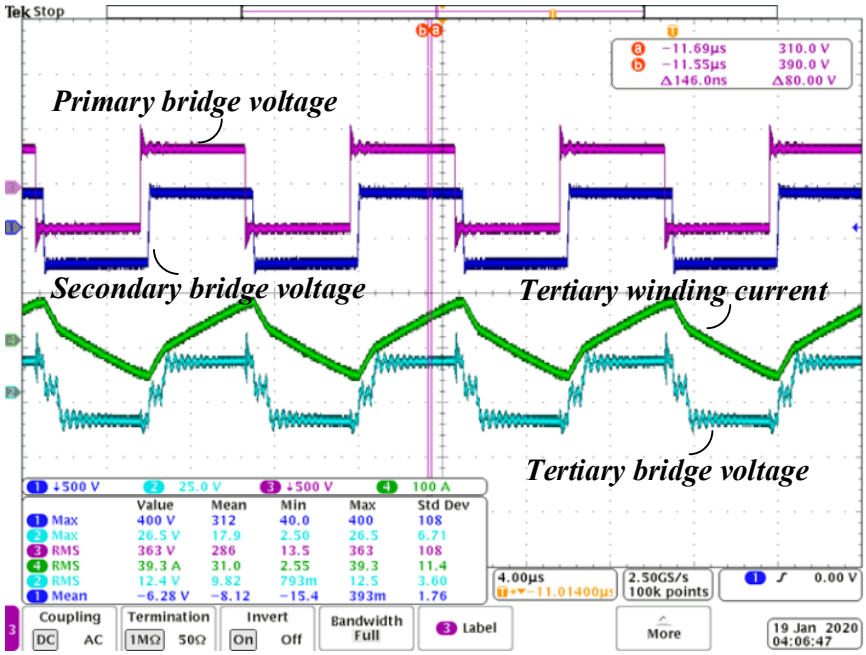



Fig. 4-23. The steady-state waveforms at G2B mode with the input power 2.5kW (tertiary winding current RMS 39.3A).

Moreover, the power conversion efficiency is measured through the power analyzer PA3000 from Tektronix. The peak efficiency of the G2B mode is 95.8% at the input power 1163W. It is confirmed that the circulating power is suppressed among three ports since the efficiency is not compromised.

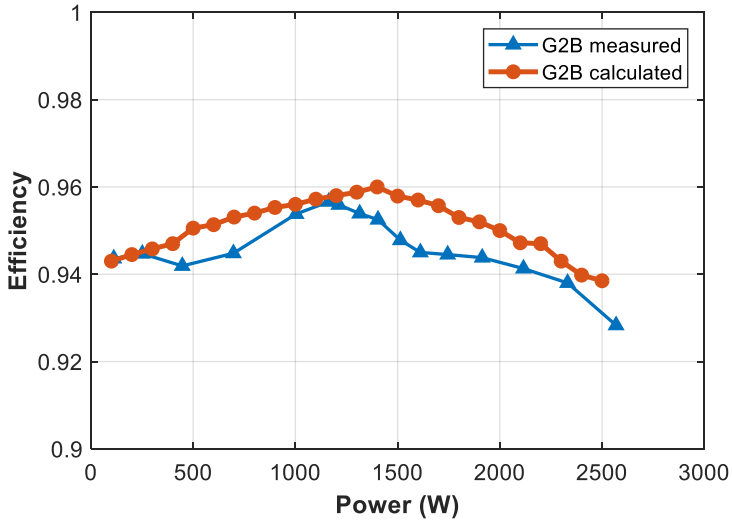



Fig. 4-24. The efficiency measurement of the TAB converter at G2B mode.

4. 4. 2 Other Operation Modes

Other operation modes are verified, including G2V mode, V2G mode, and G2L mode. Fig. 4-25 shows the steady-state waveforms of the G2V mode operation at 2.83kW input power. It is reported that the peak efficiency 96.6% is achieved at the input power 1550W. The phase difference between the primary and secondary bridges are optimized to enhance the efficiency. The steady-state waveforms at V2G mode are presented in Fig. 4-26. The peak efficiency of the V2G mode in the DC-DC stage is 96%. As can be seen from the figures, soft switching is achieved in both primary and secondary bridge switches.

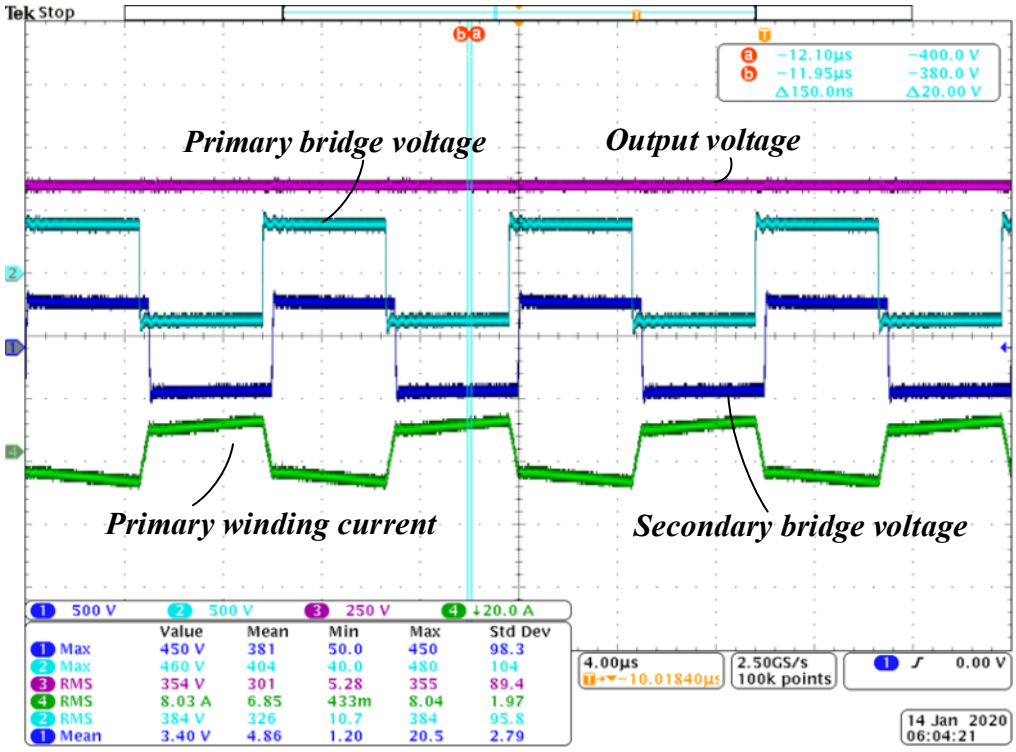



Fig. 4-25. The steady-state waveforms at G2V mode with $P_{in}$ = 2.8kW.

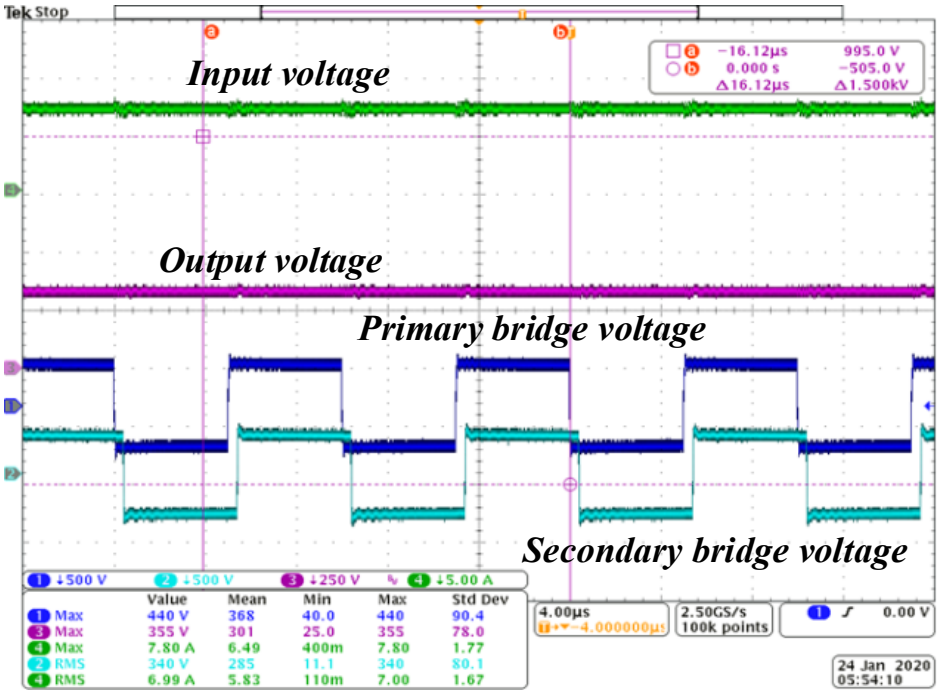



Fig. 4-26. The steady-state waveforms at V2G mode with $P_{in}$ = 2.5kW.

The measured efficiency curves are shown in Fig. 4-27. Both G2V and V2G modes have similar power conversion performance over a wide range of powers due to the zero reverse recovery charge of the GaN device and the symmetric circuit tanks. Hence, the bidirectional power flow is achieved without compromising the efficiency.

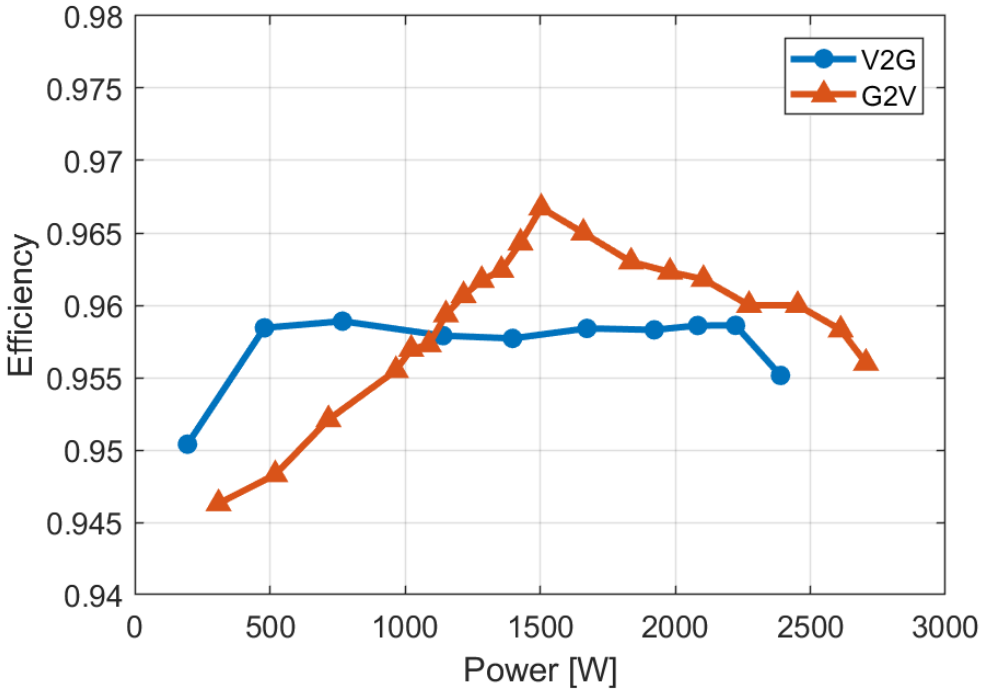



Fig. 4-27. The measured efficiency curves for different operation modes.

Moreover, G2L mode is verified experimentally. As shown in Fig. 4-28, there is low voltage spike in the bridge voltage, which leads to small output voltage ripple. In the steady-state operation, it is reported that the efficiency is up to 93.4% at 712W input power.

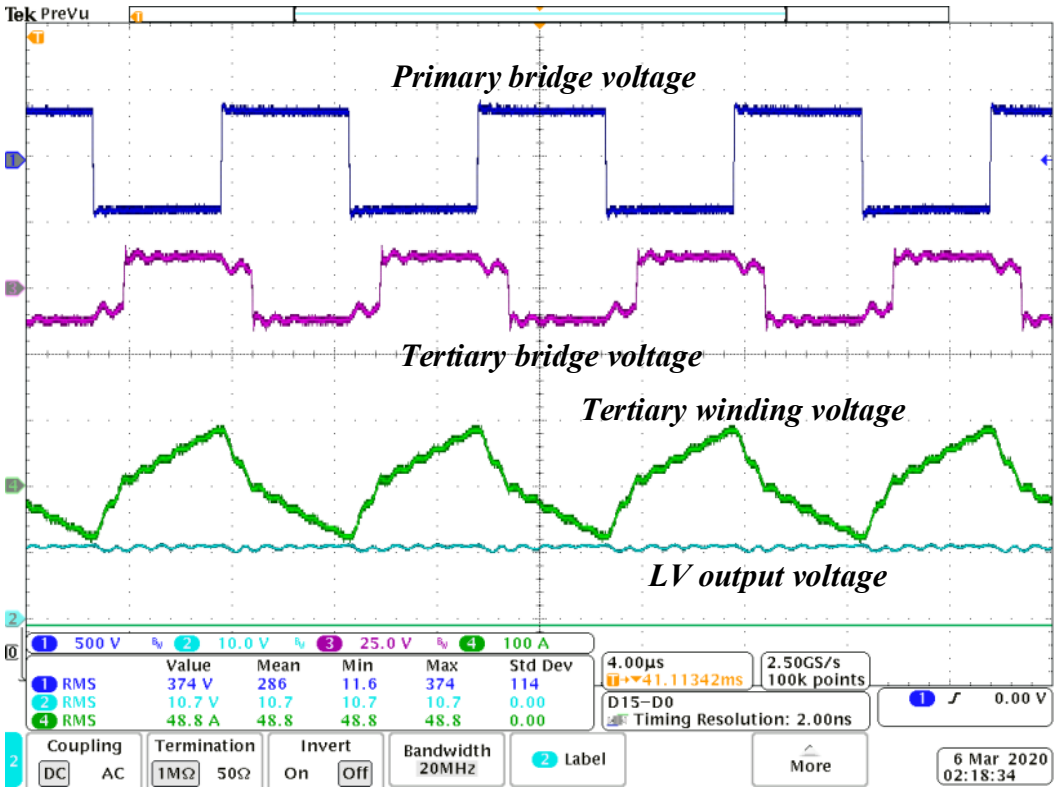



Fig. 4-28. The steady-state waveforms at G2L mode. The tertiary winding current is close to 50A.

## *4. 5 Summary*

This section first introduced the basic characteristics of a GaN-based TAB converter. Based on the decoupled delta equivalent circuit, the modeling of a TAB converter is conducted using GHA with the phase shift variables $\varphi$ and duty ratio variables $\delta$, which can essentially maintain high accuracy with respect to different odd orders of harmonic components. Moreover, two control algorithms are proposed to improve the efficiency: circulating power-oriented control and current-oriented control. The first control method is focused on the minimization of the circulating energy. The HV and LV output voltages are regulated through $\varphi_2$, $\varphi_3$ and $\delta_3$. By applying $\varphi_2 = \varphi_3$, no circulating active power flows between port-2 and port-3. The second control method is focused on the suppression of the winding current summation. A current-oriented control loop is developed using the GHA-based model to predict the winding currents.

By means of defining a range of all control variables, an executive iteration is conducted to obtain the optimum solution. The objective function is to minimize the sum of RMS currents in primary, secondary and tertiary windings and realize ZVS for all bridges, such that the circulating energy can be minimized. To verify the proposed modelling technique and control method, simulations are developed in PSIM. The simulated waveforms are consistent with the analytical estimation, which proves the effectiveness of the GHA-based model. Based on the required maximum current rating, a comprehensive comparison between the $\varphi$ $\delta$ control and $\varphi$ control is achieved considering the difference in the operation ranges. To verify the proposed system, an integrated onboard charger module hardware is developed and tested. The DC-DC converter is tested up 2.83kW. It is reported that the G2B mode peak efficiency is 95.8%, the G2V mode peak efficiency is 96.6%, the V2G mode peak efficiency is 96%, and the G2L mode peak efficiency is 93.6%.

# Chapter 5 : Conclusions and Future Work

## *5. 1 Conclusions*

In this dissertation, a novel GaN-based integrated onboard charger is proposed with the capability of simultaneous charging of both HV and LV batteries. The system is composed of a totem-pole PFC rectifier and a TAB converter. First, an integrated control strategy in the totem-pole PFC rectifier to resolve the zero-crossing distortion is proposed and analyzed, where a soft transition-based algorithm with closed-loop control is developed considering the switch characteristics, abrupt duty ratio changes in high-frequency MOSFETs, and digital delays. To validate the proposed integrated control method, simulation has been conducted to examine the THD, voltage ripple and power factor correction. Tight input current and output voltage regulations are achieved, where the power factor is maintained greater than 0.99 and the THD is lower than 5%. Furthermore, a start-up control to obtain the minimum inrush current is proposed in this work. It is mathematically proven that the inrush current can be made zero if the PFC action control is engaged at the negative-to-positive zero crossing of the input AC voltage. Furthermore, a comprehensive design for DM filters is achieved to satisfy the required noise spectrum attenuation. The effectiveness of the proposed two-stage DM filters is verified through simulation. In order to obtain an accurate estimation of boost inductance and its losses, a dynamic ripple-based estimation method is proposed considering the variation of material permeability and ripple function. It is experimentally reported that at 2.8kW output power, the efficiency is measured as 98.5% and the power factor is 0.995. In addition, the total harmonic distortion (THD) is below 1%.

Furthermore, the three-winding transformer for the TAB converter is disclosed. Both the Litz-wire and PCB winding transformers are designed using the optimization method. In the planar transformer design, the primary and secondary windings are split unevenly in both side

legs. The planar transformer with the proposed PCB winding configuration is utilized to further improve the manufacturability, power density, and efficiency. A systematic transformer loss model, including both core and winding losses, is investigated. Note that due to this specific winding structure and customized core, the conventional core loss models are not applicable. Therefore, an accurate transformer model based on reluctance determination is proposed to predict the core loss, magnetizing and leakage inductances. The magnetizing inductance and leakage inductance are obtained and verified from both analytic model and simulations. The magnetizing inductance model is experimentally validated using a preliminary transformer prototype. Consequently, a multi-objective optimization problem is formulated to optimize the integrated transformer design considering core geometry, losses, and inductances. The optimal configuration has a customized core geometry that can achieve good electrical and thermal performance.

The modeling and control of a TAB converter is presented. First, the decoupled power circuits considering the control variables $\varphi$ and $\delta$ are developed. Based on the delta equivalent circuit, the modeling of the TAB converter is conducted using GHA, which can essentially maintain high accuracy with respect to different orders of harmonic components. Moreover, two control loops are proposed to improve the efficiency: circulating power-oriented loop and current-oriented loop. The first control method is focused on the minimization of the circulating energy. The second control method is focused on the suppression of the winding current summation using the GHA-based model. By means of defining a range for all the control variables, an executive iteration is conducted to obtain the optimum solution to minimize the sum of RMS currents in primary, secondary and tertiary windings. To verify the proposed modelling technique and control method, simulations are conducted in PSIM. The simulated waveforms are consistent with the analytical estimation, which proves the effectiveness of the GHA-based model. Based on the required maximum current rating, a comprehensive comparison between the $\varphi$ $\delta$ control and $\varphi$ control is presented. To verify the proposed system,

an integrated onboard charger module hardware is developed and tested. The DC-DC converter is tested up 2.83kW. It is reported that the G2B mode peak efficiency is 95.8%, the G2V mode peak efficiency is 96.6%, the V2G mode peak efficiency is 96%, and the G2L mode peak efficiency is 93.6%.

## *5. 2 Future Work*

Future works can be carried out to extend this research project, including the generalized multi-winding transformer design, the Quadruple-Active-Bridge (QAB) DC-DC converter, the MHz integrated onboard charger and extension to three-phase modular topologies.

(1) Multi-winding Transformer Design

Based on the proposed three-winding integrated transformer design technology, the extended model for the multi-port transformers can be developed. Various core shapes can be implemented with both the Litz wire and PCB winding, depending on the design specifications and considering acceptable values for parasitic capacitances. The transformer turns ratios can be chosen according to the range of operating voltages at each port,

$$N_1 : N_2 : \dots : N_k = V_{1,nom} : V_{2,nom} : \dots : V_{k,nom} \quad (5.1)$$

where $V_{1,nom}, V_{2,nom}, \dots, V_{k,nom}$ are the nominal operating voltages. For instance, a four or five-winding integrated transformer can be developed for the satellite or other applications. The typical bus voltage of a satellite power supply is 28V, and the loads can be multiple loads connected in parallel with low dc voltages of 3.3, 5, ±12 V, etc. Thus, a hypothetically possible multi-winding transformer winding structure could be the one as shown in Fig. 5-1, where the high current winding can be connected in parallel across both side legs to share the current.

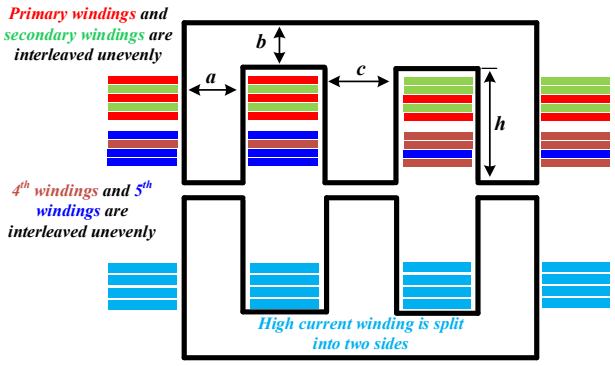



Fig. 5-1. The diagram of a five-winding integrated transformer using PCB windings.

The five-winding integrated transformer can also be realized using the Litz wire-wound in the side legs. The winding arrangement can be interleaved or non-interleaved. The flux balance can be achieved by the implementation of the asymmetric winding configuration. It is worth mentioning that the intra-winding/inter-winding capacitance in the PCB windings needs to be minimized. Thus, a multi-objective optimization problem needs to be developed to optimize the transformer design considering core geometry, losses and inductances, and parasitic capacitance. Given the transformer model with the desired inductances and minimized parasitic capacitances, the system level analysis and simulation will need to be conducted to determine the component parameters. The research on multi-winding transformers can be expanded to various systems, as it is an interdisciplinary research area with various challenges unique to each and every system.

(2) Quadruple-Active-Bridge (QAB) DC-DC Converter

Furthermore, the proposed work can be expanded to other active-bridge-based converter designs such as residential DC microgrids. Fig. 5-2 illustrates the power conversion architecture of the DC microgrid using a QAB converter. Multiple subsystems with different voltage levels can be integrated using a multi-winding transformer. This architecture enables seamless integration of renewable energy systems such as Photovoltaic (PV) arrays, LED lightings, energy storage systems, and consumer electronics. Thus, the DC microgrid system

can be more compact, efficient, and scalable using a single multi-port power electronic interface compared to the utilization of discrete converters between different ports.

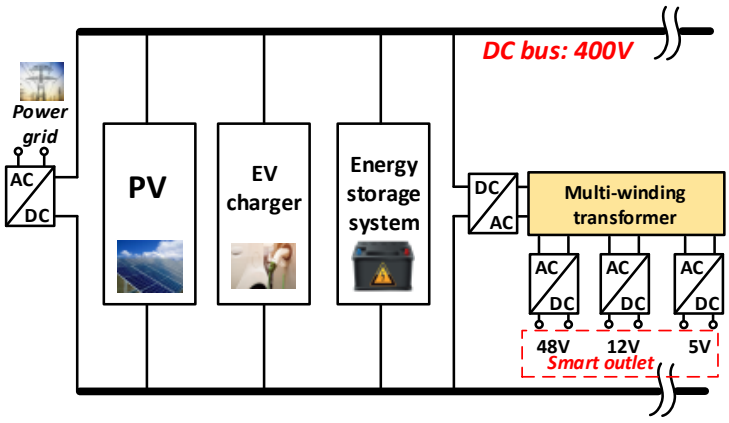



Fig. 5-2. The diagram of a residential DC microgrid power with a multi-winding transformer.

To achieve such integration, innovative modulation schemes such as hybrid phase shift-duty ratio modulation strategy needs to be investigated to realize the power flow management between all the ports while maintaining tight voltage/current regulations. The control variables, such as the phase differences among different bridge voltages and the duty ratios, need to be carefully selected to satisfy control objectives while ensuring system convergence within an acceptable computation time.

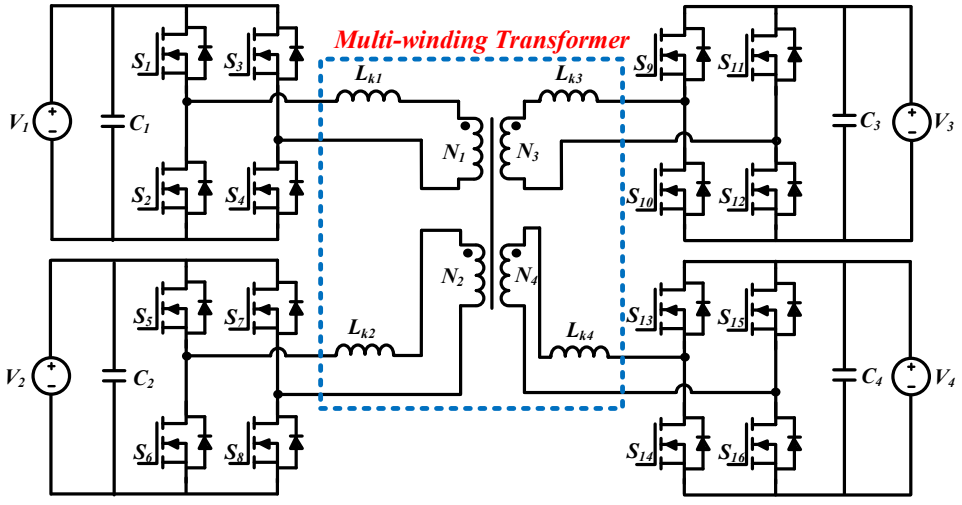



Fig. 5-3. A possible topology for a four-winding-transformer-based QAB converter.

(3) MHz Integrated Onboard Charger and Extension to Three-Phase Modular Topologies

The size and weight of power electronic systems can be reduced with the increase of the switching frequency. Thus, a MHz integrated onboard charger can be a future work to advance this technology not only with the utilization of the GaN device, but also substantially increasing the switching frequency. However, increasing the switching frequency will bring many new challenges, for instance the AC-DC PFC rectifier needs to be operated at the critical conduction mode. Additional challenges will need to be considered in DC-DC stage.

Furthermore, the magnetic design will be very challenging at MHz operation frequency. The parasitic capacitances will also play a more critical appearance in MHz operation and different techniques need to be proposed to reduce such capacitances. Moreover, the EMI burden at the MHz operation will substantiate the design of EMI stage, particularly for a single-phase system. Furthermore, initially this research had the objective of designing a three-phase GaN based integrated OBC; however, due to the various unexpected challenges, it could only investigate the design complexities for a single-phase GaN integrated OBC. Therefore, a modular three-phase integrated OBC could be another extension to this research.

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