ABSTRACT

Title of Document:	HIGH FREQUENCY GENERATION FROM CARBON NANOTUBE FIELD EFFECT TRANSISTORS USED AS PASSIVE MIXERS
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The high mobilities, low capacitances (due to small sizes), and high current densities of carbon nanotube field-effect transistors (CNT FETs) make them valid candidates for high frequency applications. The high cost of high frequency measurement equipment has been the largest hurdle to observing CNT transistor behavior at frequencies above 50 GHz. One economic solution to this barrier is to use an external harmonic mixer to convert high frequency signals to lower frequencies where they can be detected by a standard spectrum analyzer. By using this detection method, a new regime of high frequency CNT FET behavior is available for study.

In this dissertation, we describe the design and fabrication of CNT FETs on quartz substrates using aligned arrays of CNTs as the device channel. The nonlinear input voltage to output drain current behavior of the devices is explained and approximated to the first order by using a Taylor expansion. For the high frequency mixing experiments, two input voltages of different frequencies are sourced on the

gate of the devices without any device biasing. The input frequencies are limited to 100 kHz to 40 GHz by the signal generators used. The nonlinearities of the fabricated CNT FETs cause the input frequencies to be mixed together, even in the absence of a source-drain bias (passive mixing). The device output is the drain current, which contains sum and difference products of the input frequencies. By using an external harmonic mixer in combination with a spectrum analyzer to measure the drain current, output frequencies from 75 to 110 GHz can be observed. Up to 11th order mixing products are detected, due to the low noise floor of the spectrum analyzer. Control devices are also measured in the same experimental setup to ensure that the measured output signals are generated by the CNTs. The cutoff frequencies from previous passive mixing experiments predict that our devices should stop operating near 13 GHz, however our measurement setup extends and overcomes these cutoffs, and the generation of high frequency output signals is directly observed up to 110 GHz. This is the highest output frequency observed in CNT devices to date.

HIGH FREQUENCY GENERATION FROM CARBON NANOTUBE FIELD
EFFECT TRANSISTORS USED AS PASSIVE MIXERS

By

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When I began writing this dissertation, I instinctively used the pronoun "we" instead of "I" when referencing the work that was done and would be presented. The use of a majestic plural pronoun was not motivated by the high esteem in which I hold myself, but by the dishonesty involved in claiming this work as the fruits of my labor alone. My nearly seven years at the University of Maryland have convinced me of the benefits of collaborations, and I'd like to mention a few of the people who have aided me along the way.

I first must thank my advisor, Ellen Williams, for accepting me into her research group before I even arrived in Maryland. Ellen has provided guidance and always made time for my questions, in spite of her many responsibilities. It is tempting to grow discouraged with failed experiments and incomprehensible results, but Ellen is a master of highlighting the positive sides and telling a clear story. When Ellen's responsibilities took her to London, John Cumings took over my weekly advising. John helped me narrow the scope of my research to what is presented in this dissertation. I have met many graduate students who grow to dislike their field and/or the whole experience of being in graduate school. I very much enjoy my field and being a researcher in this group. If not for John reminding me that my goal should be graduation, I would still be pursuing every experimental dead-end that struck me as interesting. John and Ellen, thank you for getting me here.

The first scientist with whom I began working was Dan Hines. My first day in the lab, Dan began patiently training me on cleanroom equipment. A significant portion of my time here has been devoted to device fabrication, and nearly all of my

lithography skills can be traced to Dan. My first two publications came from our early work together. As my focus shifted from organic electronics to carbon nanotubes, Dan and I have worked less together, but he has always given practical advice and has been very generous in the correction process for several chapters. For my most recent experiments, I have worked most closely with Vince Ballarotto. For experimental design, equipment acquisition, proper measurement techniques, data analysis, and more, Vince has been essential every step of the way. He has an excellent sense of when to motivate and when to encourage. Vince's hard work in editing much of this dissertation is very much appreciated. I also want to thank Steven Anlage for helping design our high frequency mixing experiments.

Most of my fellow graduate students graduated ahead of me and offered me encouragement from beyond the academic world. Mihaela Ballarotto was the senior graduate student when I began. Hers was the first defense I attended, and even then she assured me that I would be in her position soon enough. She has provided moral support throughout the years. Tracy Moore and Vinod Sangwan have been allies in the lab and good friends outside of it. Vinod trained me in chemical vapor deposition (CVD) and helped me get up to speed on CNT devices. Major thanks to Enrique Cobas for providing our first samples of aligned CNTs on quartz. He did the hard work of fine-tuning the CVD recipes. Merijntje Bronsgeest contributed significantly to the experiments on burning CNTs and charge trap measurements. Her eagerness to investigate and understand models that aren't directly related to her research path both impressed and helped me. And my appreciation to Dan Lenski and Jia Huang for

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List of Abbreviations

AC – alternative current

AFM – atomic force microscope

W – channel width

C_{GCNT} – gate-nanotube capacitance

C_{GD} – gate-drain capacitance

C_{GS} – gate-source capacitance

CNT – carbon nanotube

DC – direct current

DUT – device under test

GSG – ground-signal-ground

GPIB – general purpose interface bus

LO – local oscillator

dBm – decibel milliwatts

E_F – Fermi energy

FET – field-effect transistor

CVD – chemical vapor deposition

G – gate length

HF – high frequency

IV – current voltage

SCCM – standard cubic centimeters per minute

SSP – single-side polished

I_d – drain current

IPA – isopropyl alcohol

L – channel length

PET – polyethylene terephthalate

PMMA – poly(methyl methacrylate)

RFID – radio-frequency identification

RIE – reactive ion etcher

SEM – scanning electron microscope

SMA – SubMiniature Version A

V_{ds} – drain-source voltage

V_{gs} – gate-source voltage

Chapter 1: Introduction

1.1 Introduction to Carbon Nanotubes

Carbon is the basic building block of life on earth. In its neutral electronic state, it has four valence electrons that allow up to four covalent chemical bonds to be formed with adjacent atoms. In organic compounds, carbon atoms form the molecular skeleton to which other elements attach to functionalize the molecule and account for most of the chemical behavior. Hydrogen, oxygen, and nitrogen are the most common functional elements in organic chemistry. Plastics, pharmaceuticals, fats, proteins, and DNA are all composed of organic compounds.

Carbon can also exist as a pure solid in multiple allotropes. The kinds of bonds that each carbon atom forms with its neighbor will determine the bulk structure. When each carbon atom is sp^3 hybridized, it forms four covalent bonds with other carbon atoms. This allotrope of carbon is diamond. With all valence electrons held in covalent bonds, no electrons are free to move through the bulk material, so diamond is an insulator.

When each carbon atom is sp^2 hybridized, it forms three bonds with other carbon atoms which produces a honeycomb pattern of carbon atoms in a flat sheet. This material is called graphene. Since only three of the four valence electrons are used in bonds, each carbon atom contributes a free electron that is delocalized in two pi bond orbitals above and below the graphene plane. Unlike diamond, these free electrons allow graphene to conduct electricity.

Being only one atom thick, graphene is thought of as a two-dimensional material. When layers of graphene are stacked on top of each other, the three-dimensional material graphite is formed. When one sheet of graphene is rolled into a tube, a carbon nanotube is formed, which is thought of as a one-dimensional material and the material investigated in this dissertation. Molecules called fullerenes, which are thought of as zero- dimensional materials due to their small size, can also be made from a sheet of graphene. A diagram showing the structure of a fullerene (C-60), a carbon nanotube, and graphite from a graphene sheet is shown in Figure 1.1. This illustrates the material structure only and not how each material is made.
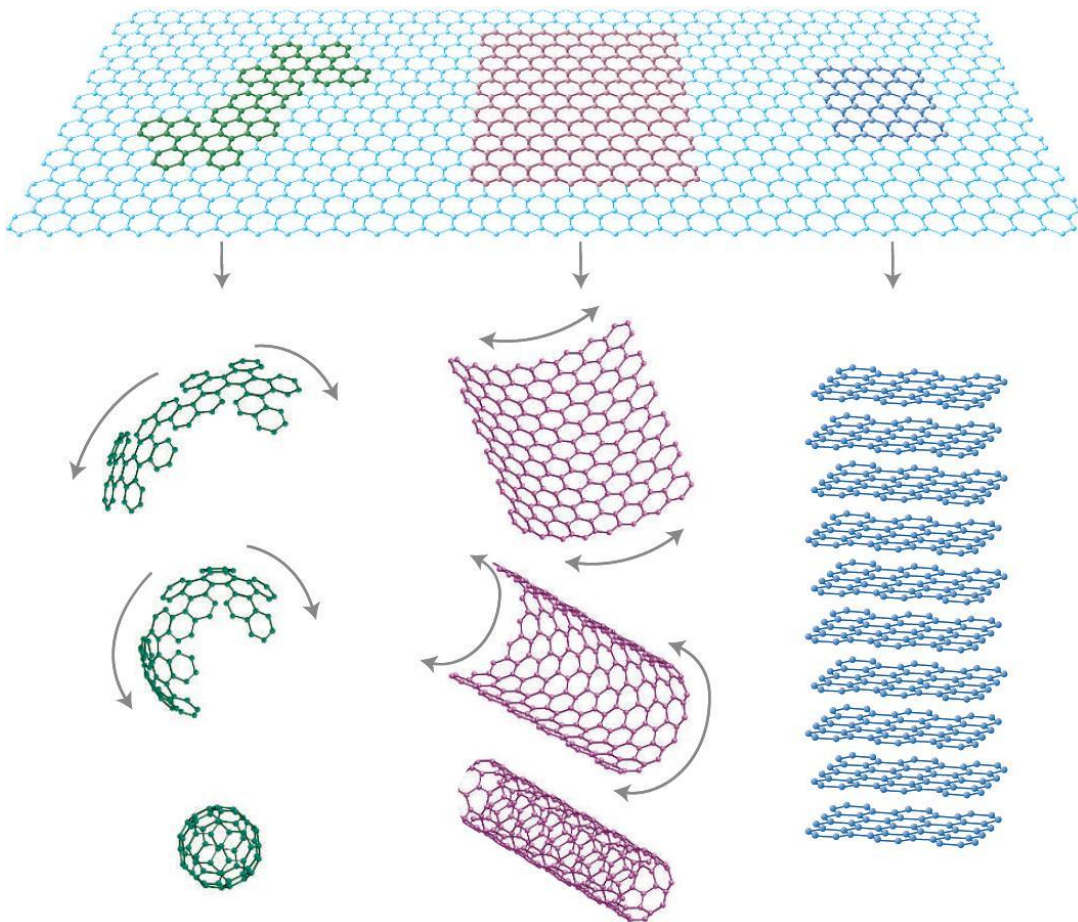
Figure 1.1 Structural diagrams of the sp^2 allotropes of carbon as formed from the theoretical shaping of a section of graphene. When wrapped into a ball it forms the fullerene C60; when wrapped into a cylinder it forms a carbon nanotube. When stacked into sheets it forms graphite.

Experimentally fabricated carbon nanotubes (CNTs) were first observed by transmission electron microscopy in 1991.[1] The observed "helical microtubules of graphitic carbon" were micrometers in length but had diameters of a few nanometers. The longest measured CNTs so far have been 18.5 cm long.[2] This large aspect ratio (10^8) provides an interesting bridge between nanoscale quantum behavior and macroscopic electronic devices.

Nanotubes can exist as single cylinders (single-walled carbon nanotubes) or as multiple concentric cylinders (multi-walled carbon nanotubes). Since many different cylindrical geometries can be formed from the sp2 honeycomb graphene lattice, each nanotube geometry is specified by a chiral vector ($\mathbf{C_h}$) that forms the nanotube circumference. The chiral vector is specified by integer multiples of the graphene unit vectors $\mathbf{a_1}$ and $\mathbf{a_2}$ and is written as $\mathbf{C_h} = n\mathbf{a_1} + m\mathbf{a_2} = (n, m)$. To avoid multiple vectors describing identical nanotube geometries, the convention $0 \leq |m| \leq n$ is used. While n and m could theoretically be any positive integer, single- walled carbon nanotube diameters are rarely seen to exceed 10 nm,[3, 4] so the number of different CNT geometries are experimentally limited to a few hundred. The unit vectors and examples of different chiral vectors are shown in the graphene lattice in Figure 1.2a.

Nanotube geometries fall into three main geometric types. When the first chiral index is zero (0, m), the resulting nanotube circumference makes a zigzag pattern. These are called zigzag nanotubes. Nanotubes that have equal chiral indices (n = m), are called armchair nanotubes, again due to the carbon pattern around the circumference. Both zigzag and armchair nanotubes are achiral, meaning that they are the same as their mirror image along the circumference. All other nanotube

geometries are chiral, not the same as their mirror images. An example of a zigzag, armchair, and chiral nanotube are shown in Figure 1.2 b, c, and d.
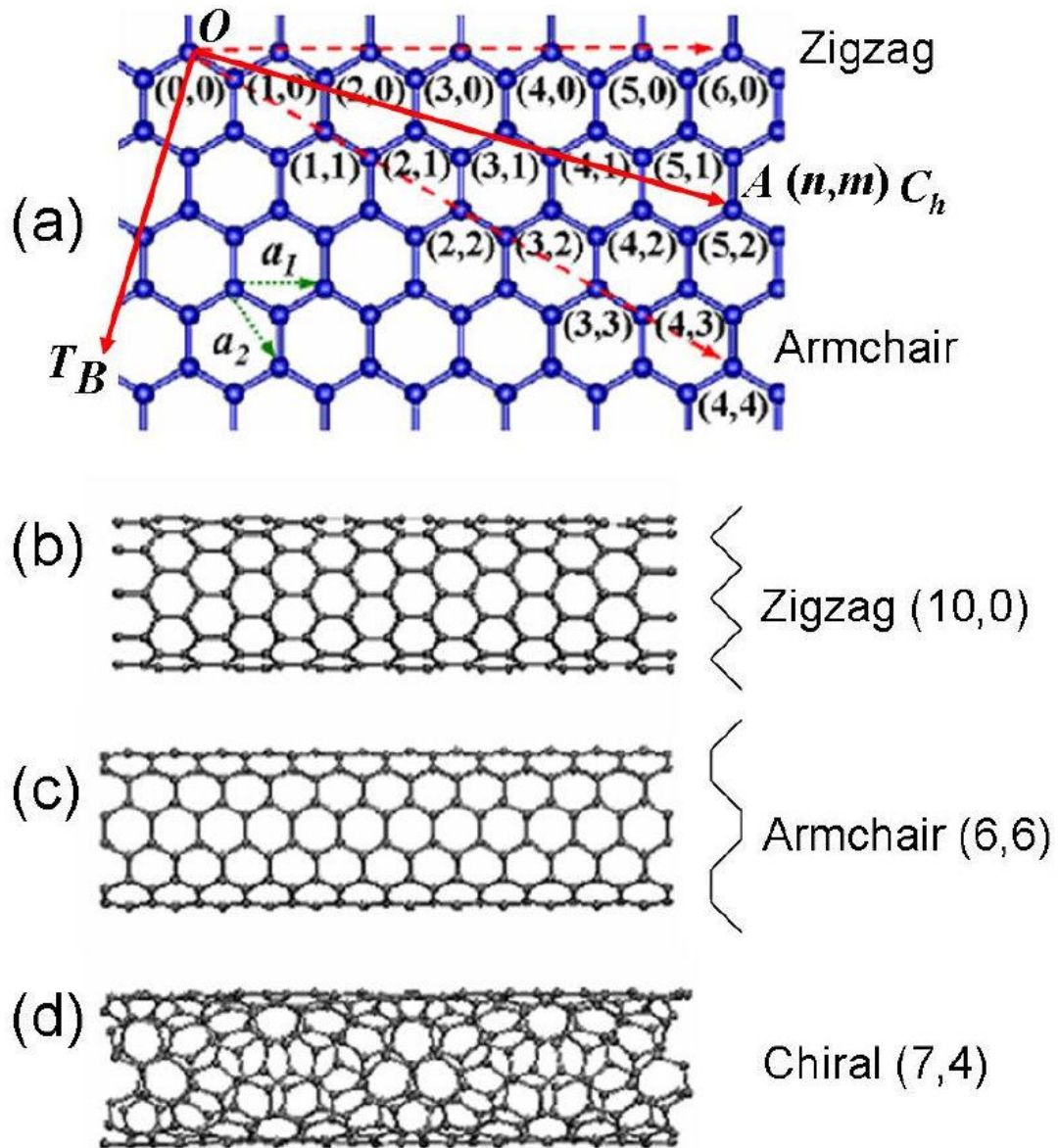
Figure 1.2 a) Image of the honeycomb graphene lattice structure with the unit vectors (a_1 and a_2) and chiral vectors shown. A chiral vector defines the circumference of a nanotube. Examples of a zigzag, armchair, and chiral nanotube are shown in b), c), and d). Image courtesy of Professor Susan Sinnott, UFL

Since the chiral vector forms the circumference of the CNT, the tube diameter is the magnitude of the chiral vector divided by pi, shown in EQ 1.1. *a* is the graphene unit vector length, which is equal to 2.49 Å.

$$d = \frac{\left|\vec{C}\right|}{\pi} = \frac{a}{\pi}\sqrt{n^2 + m^2 + nm}$$

EQ 1.1

1.2 Carbon Nanotube Electronic Properties

The electronic band structure of CNTs comes from the band structure of graphene with boundary conditions added from the cylindrical symmetry. The graphene band structure was derived by Wallace using the tight binding model in 1947.[5] The energy dispersion relation is shown in EQ 1.2, where E_F is the Fermi energy, γ_0 is the transfer integral of overlapping orbitals, and k_x and k_y are the momentum wave vector.

$$E(k_x, k_x) = E_F \pm \gamma_0 \sqrt{1 + 4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right) + 4\cos^2\left(\frac{k_y a}{2}\right)}$$

EQ 1.2

The square root quantity is equal to zero for six k vectors (k_x, k_y): $\left(0, \pm\frac{4\pi}{3a}\right)$ and $\left(\pm\frac{2\pi}{\sqrt{3}a}, \pm\frac{2\pi}{3a}\right)$. At these points, called K points, the conduction and valence bands meet. Since they meet but do not overlap, graphene is considered to be a zero-bandgap semiconductor. A diagram of this band structure is given in Figure 1.3. The structure near each K point is conical for small energies above and below the Fermi level.

Carbon nanotube band structures deviate from graphene because not all k

vectors are allowed. The finite circumference sets a periodic boundary condition on

momentum vectors parallel to the chiral vector. That boundary condition is given by

EQ 1.3, where p is an integer.

$$\vec{k} \cdot \vec{C}_h = nk_x + mk_y = 2\pi p \qquad\qquad \text{EQ 1.3}$$
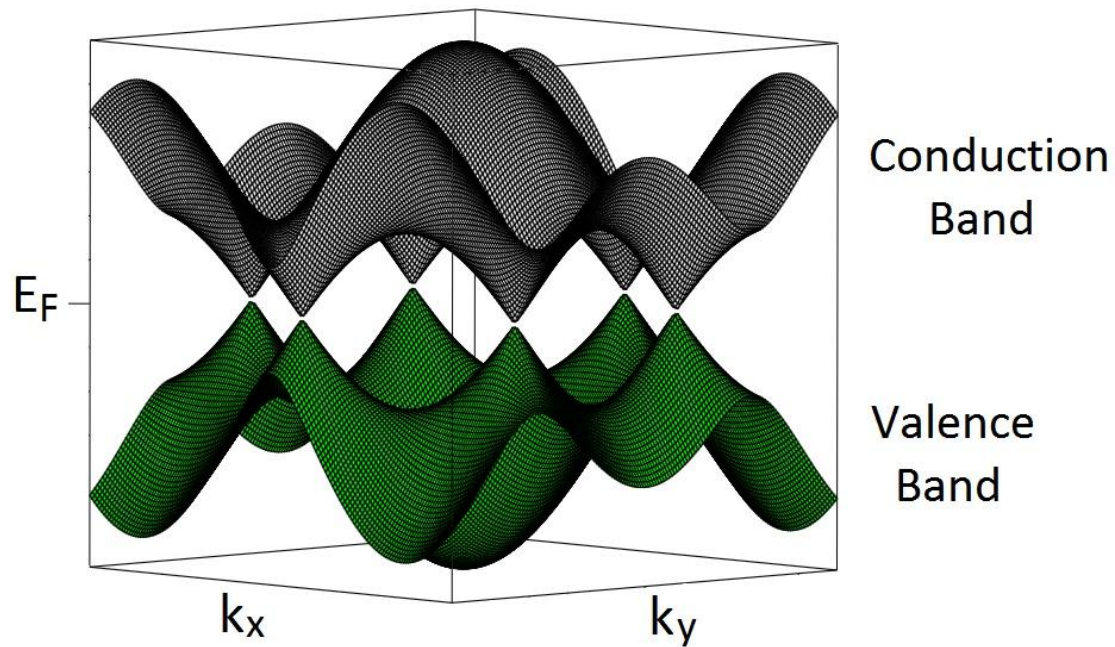
Figure 1.3 Band structure of graphene. The conduction band (gray) and valence band (green) lie above and below the Fermi level respectively. Image plotted in Maple from EQ 1.2.

This boundary condition divides the graphene band structure into a discrete

number of allowed momentum vectors for each CNT chirality. Only when the

difference between the chiral indices (n – m) is divisible by 3 do the allowed

momentum vectors pass through the K points. In those cases, there is no bandgap and

the CNT is metallic. Armchair nanotubes meet this condition and are all metallic. In

reality, the curvature of CNTs induce deviations to this band structure, and many of

the nanotubes that meet this condition contain small band gaps (~10 meV) and are

semimetallic.[6] For most measurements, such a small band gap will be

indistinguishable from a metal, so we treat semimetallic CNTs as metallic CNTs for

the rest of this dissertation. For all the CNTs where the difference in chiral indices is

not divisible by 3, a bandgap will exist, and the CNT will be semiconducting. This

results in twice as many possible semiconducting CNTs as metallic CNTs. Diagrams

of the band structures for a metallic and semiconducting nanotube are given in Figure

1.4.
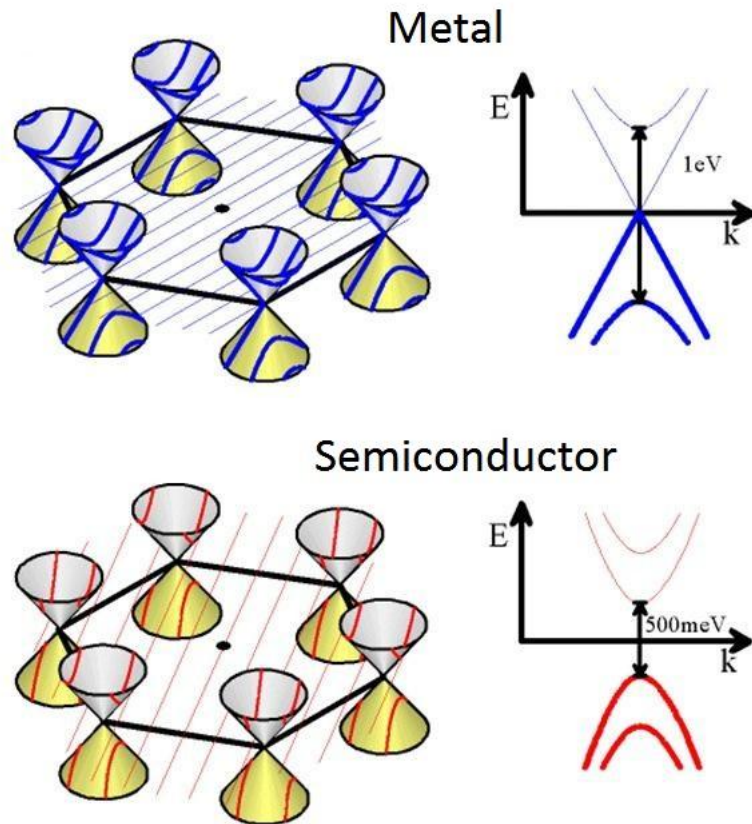
Figure 1.4 Band structures for a metallic and semiconducting carbon nanotube, shown as lines of allowed momentum wave vectors from the periodic boundary condition EQ 1.3. Image provided by Michael Fuhrer.

1.3 Advantages of Carbon Nanotubes in High Frequency Applications

Carbon nanotubes have many impressive properties. They are the stiffest

material known, with a Young's modulus ranging from 1 to 5 TPa.[7, 8] Diamond, the

hardest naturally occurring mineral, has a Young's modulus of 1.22 TPa,[9] and steel

has a Young's modulus of 200 GPa. CNTs are also excellent thermal conductors,

with experimental room temperature thermal conductivities near 3000 W/mK,[10]

while diamond is between 900 and 2320 W/mK[11] and copper is 400 W/mK. But it is

the extraordinary electronic properties of carbon nanotubes and their potential for

high frequency applications that is the motivation and focus of this dissertation.

The quantity that best describes a semiconductor's high frequency

performance is its charge carrier mobility (μ), which defines how quickly charges can

move through a material in response to an electric field. It is related to the drift

velocity through a material by EQ 1.4.

$$V_d = \mu E \hspace{5cm} \text{EQ 1.4}$$

The larger the drift velocity of a charge carrier, the faster it can respond to a

change in electric field. When an AC signal is input on a semiconductor, the electric

field changes at the input frequency, so the higher the input frequency, the less time

carriers will have to travel through the semiconductor before the field changes and

they reverse direction. The larger the carrier mobility, the greater distance carriers

will cover in each period. When carriers stop moving, a semiconductor can no longer

function. Carbon nanotubes have a measured room temperature carrier mobility of

100,000 cm^2/Vs[12], which is 70 times greater than the room temperature mobility of

silicon (1,400 cm^2/Vs for electrons).

Silicon has dominated the semiconductor industry due to its ease of growth into high purity wafers, its elemental abundance on earth, and its robust thermal oxide. The miniaturization of silicon devices has doubled the operating frequency of silicon transistors every 18 months, following Moore's Law. This trend must eventually come to an end as silicon devices approach atomic barriers. To continue increasing semiconductor operational frequencies, other materials with larger mobilities will have to be used.

For semiconductor operation at frequencies beyond what silicon can provide, gallium arsenide and indium antimonide have been used, which have room temperature electron mobilities of 8,500 and 77,000 cm^2/Vs respectively. Neither of these semiconductors have threatened silicon's dominance for two reasons. First, they do not produce a high quality thermal oxide which is a useful feature when constructing field effect transistors. Second, they are much more expensive to manufacture. The source minerals are less abundant on earth, and high quality wafers require slow and expensive fabrication processes such as molecular beam epitaxy. The high fabrication costs have limited their incorporation into all but a few expensive high frequency components.

Carbon nanotubes do not produce a natural thermal oxide either, requiring the deposition of dielectric layers that may not form an ideal interface with the nanotube surface. These issues are discussed in Chapter 4. However, nanotubes are very inexpensive to produce. Large volumes of CNTs can be synthesized from arc discharge[1], laser ablation[13], and chemical vapor deposition[14, 15], all cheaper processes than those used to produce gallium arsenide and indium antimonide. Also, the carbon

source materials are much more abundant on earth than gallium, arsenic, indium, or antimony.

One other limitation to a semiconductor's performance at high frequencies comes from its resistance and capacitance. At frequencies above $1/2\pi RC$, more than half of the input power is lost through that capacitance, so the smaller the resistance and capacitance of the nanotube, the faster it will be able to operate efficiently. Due to its nanometer scale diameter, the quantum capacitance from a CNT is very small, with a theoretical minimum value of 100 aF / μm of channel length.[16] The conduction through a CNT is quantized, with the ideal quantum conductance per CNT equal to 155 μS. That corresponds to a impedance of 6.45 kΩ.[16] If a nanotube device were able to be made with these minimum values, the RC cutoff frequency would scale with channel length as EQ 1.5.

$$f_{RC} = \frac{1}{2\pi R_Q (C_Q / L)} \approx 250 \text{ GHz}$$

Real devices will include contact resistances and capacitances between the CNT with other device electrodes, but the scale of this approximation demonstrates the appeal of using carbon nanotubes in high frequency devices. One barrier to integrating CNTs into everyday electrical components is the high impedance of individual tubes. To preserve power transmission down multiple electronic components, each is typically impedance matched to 50 Ω. The minimum impedance of a single CNT is 130 times that impedance. For this reason, our devices include hundreds of CNTs in our channels, with the goal of coming closer to matching the impedance of the other electrical equipment used in our experiments.

The goal of this research is to fabricate carbon nanotube field-effect transistors to be used as mixers in a frequency regime where their behavior has not yet been directly observed. In Chapter 2 we introduce carbon nanotube field-effect transistors, how they are expected to behave in our experiments, and how they were fabricated. Chapter 3 discusses the problems associated with imperfect dielectric layers in our CNT FET devices, most notably the existence of charge traps visible as hysteresis in transfer curves. A measurement technique utilizing short voltage pulses is presented to reduce the effects of trapped charges, eliminating hysteresis in transfer curves. In Chapter 4 we discuss the removal of metallic CNTs from our as-grown networks. Though common on standard silicon substrates, this had not been done before on our quartz device substrates. Chapter 5 summarizes the published experimental results of other research groups and clarifies how our experiments differ to overcome expected frequency cutoffs. Chapter 6 describes how passive frequency mixing occurs in field-effect transistors by exploiting the nonlinear input voltage output drain current behavior of CNT FETs. Two-tone mixing experiments are performed in two frequency regimes (1 to 25 GHz and 75 to 110 GHz) in Chapter 7. CNT devices are compared with controls to confirm that the observed output is due to the nanotubes. Chapter 8 summarizes and concludes the dissertation, with some suggestions of future work.

Chapter 2: Carbon Nanotube Field Effect Transistor Behavior and Fabrication

In this chapter, we describe the general operation of a field-effect transistor. We present the expected drain current dependence on input voltages in the operational regime in which we will be taking our high frequency measurements. The nonlinear relationship between the drain current and the source-drain input voltage in carbon nanotube field-effect transistors (CNT FETs) is described and demonstrated through DC measurements. Lastly, the design and fabrication of our CNT FETs is briefly described.

2.1.1 Field Effect Transistor Basic Operation

A field-effect transistor (FET) is a three-terminal device composed of metal electrodes, a semiconducting channel, and an insulating dielectric layer. The electrodes contacting the semiconductor are called the source and drain, while the third electrode that is not in electrical contact with the channel is called the gate. When a bias is set between the source and drain, current flows through the channel. The conductivity of the channel is tuned by the voltage on the gate electrode, which sets the Fermi level in the semiconductor relative to the conduction and valence bands, controlling the number of available carriers. Carbon nanotube field-effect transistors (CNT FETs) use semiconducting CNTs as the channel. Metal contacts and oxide dielectric layers typically dope CNT FETs p-type, meaning that the Fermi level lies closer to the valence band (where holes are carriers) than the conduction band

(where electrons are carriers). A negative voltage applied to the gate electrode of a p-type CNT FET will lower the Fermi level closer to the valence band, allowing more holes to flow through the channel. A positive gate voltage will move the Fermi level up into the band gap, decreasing conduction. Some CNT FETs demonstrate ambipolarity, in which a large gate voltage moves the Fermi level close enough to the conduction band that electrons begin to be conducted. An illustration of these gating situations along with energy levels for a top-gated p-type CNT FET are shown in Figure 2.1. Figure 2.2 plots conduction vs. gate voltage for a CNT FET, demonstrating the different gating conditions shown in Figure 2.1.

Hole Conduction   Band Gap   Electron Conduction

a)   b) $V_{gs} < 0$ c) $V_{gs} > 0$ d) $V_{gs} \gg 0$

+ + +   − − −   − − − − −
− − −   + + +   + + + + +

E_C ——————

$\overline{E_C - eV_{gs}}$

$E_C - eV_{gs}$

$\overline{E_V - eV_{gs}}$

E_F - - - - - - - - - - -   - - - - - - - - - - - -

E_V ——————

$E_V - eV_{gs}$

$E_C - eV_{gs}$

$E_V - eV_{gs}$
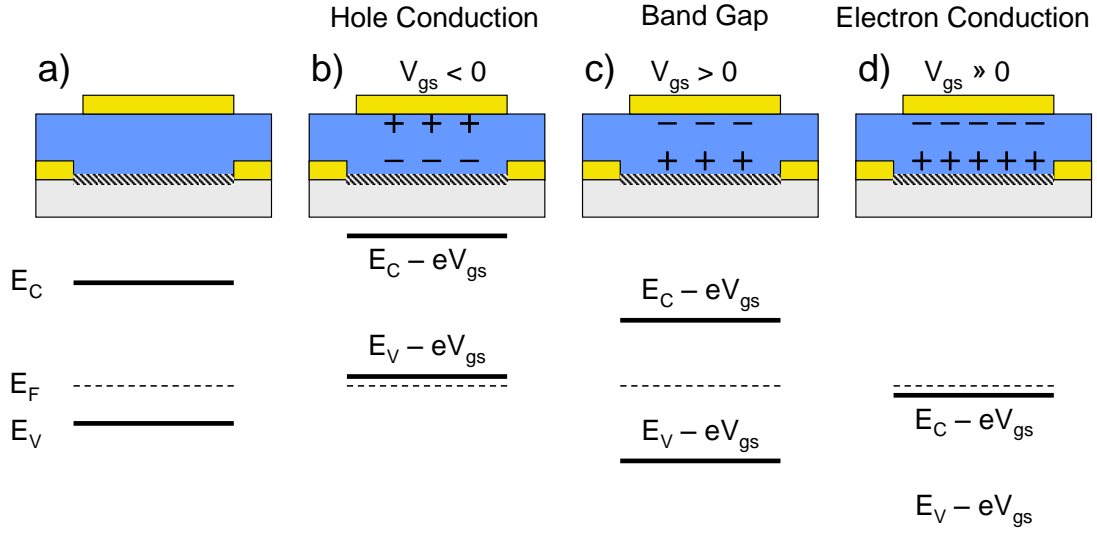
Figure 2.1 Diagrams of a top-gated p-type CNT FET with corresponding energy levels for different gate voltages. a) The Fermi level in a p-type FET will lie closer to the valence band than the conduction band. b) With a negative gate voltage, the Fermi level moves down (or the other bands move up) increasing the number of holes available. c) A positive gate voltage moves the Fermi level up, further into the band gap, decreasing conduction. d) Large enough positive gate voltages move the Fermi level close to the conduction band where electrons can act as carriers.

CNT FET Transfer Curve

Hole Conduction

Electron Conduction

Band Gap

G (μS)

V_{gs} (V)
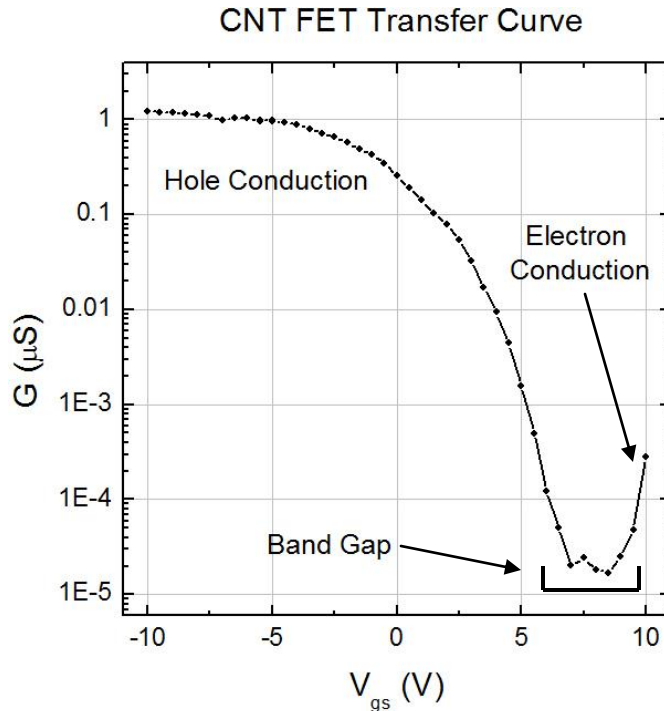
Figure 2.2 Plot of conduction (logarithmic scale) vs. gate voltage for a CNT FET. For negative gate voltages, the Fermi level lies in the valence band, and holes are charge carriers. For positive gate voltages, the Fermi level lies in the band gap and conduction is suppressed. For large positive gate voltages, the Fermi level approaches the conduction band, allowing electrons to conduct. The measurement was taken at 1 V source-drain bias.

By convention, the source electrode is typically grounded and is considered the charge carrier source (hole source for p-type FETs). The gate voltage and source-drain voltage are usually referenced relative to the source. In this dissertation, they will be referred to as V_{gs} and V_{ds}. The drain current is the standard device output quantity.

2.1.2 Field Effect Transistor DC Modes of Operation

DC operation of a CNT FET falls into three modes. The cutoff or subthreshold region corresponds to when the Fermi level lies in the band gap. The only conduction in this regime comes from a Boltzmann distribution, depending exponentially on the gate voltage. The gate voltage where the channel conduction begins to approach zero is called the threshold voltage. When the gate voltage is greater than the threshold voltage, the FET is considered off.

1) When the gate voltage is less than the threshold voltage, the CNT FET acts like a variable conductor in which the number of charge carriers contributing to the current through the channel is a function of gate voltage.

2) When the magnitude of the source-drain voltage is greater than the gate voltage, all the carriers available for conduction are being used. Therefore, increasing the source-drain voltage further, fails to increase the drain current. This region is called saturation. Our CNT FETs rarely demonstrate saturation as the source drain biases necessary can result in channel currents large enough to burn out the CNTs.

3) The last operational mode occurs when the gate voltage is less than the threshold voltage, and the magnitude of the source-drain bias is less than the gate voltage. This regime is called triode mode or the linear regime. It is in this regime that most of our high frequency experiments were conducted. The equation for the device drain current in this regime is given by EQ 2.1, where μ is the effective carrier mobility, C_g is the gate capacitance per unit length, L is the channel length, and V_{th} is the threshold voltage.

$$I_d = \frac{\mu C_g}{L}\left(V_{th} - V_{gs} + \frac{1}{2}V_{ds}\right)V_{ds}$$
EQ 2.1[17]

The conductance (G), dynamic conductance (G$_D$), and transconductance (g$_m$) in this regime are given by EQ 2.2-4.

$$G \equiv \frac{I_d}{V_{ds}} = \frac{\mu C_g}{L}\left(V_{th} - V_{gs} + \frac{1}{2}V_{ds}\right)$$
EQ 2.2

$$G_D \equiv \frac{\partial I_d}{\partial V_{ds}} = \frac{\mu C_g}{L}\left(V_{th} - V_{gs} + V_{ds}\right)$$
EQ 2.3

$$g_m \equiv \frac{\partial I_d}{\partial V_{gs}} = -\frac{\mu C_g}{L}V_{ds}$$
EQ 2.4

The dynamic conductance dependence on gate voltage is equal and opposite to the dependence on the source-drain voltage. The local charge distribution will be equally be increased by a positive change in source-drain voltage or a negative change in gate voltage. This equivalence is given in EQ 2.5 and is used as a substitution in Chapter 5.

$$\frac{\partial G_D}{\partial V_{ds}} = -\frac{\partial G_D}{\partial V_{gs}}$$
EQ 2.5

Our high frequency CNT FET experiments are done mostly in the absence of a source-drain bias. To the first order in this low bias regime, the conductance and dynamic conductance are equal, and the transconductance is zero, as shown in EQ 2.6 and 2.7.

$$G\big|_{Vds=0} = G_D\big|_{Vds=0} = \frac{\mu C_g}{L}\left(V_{th} - V_{gs}\right)$$ EQ 2.6

$$g_m\big|_{Vds=0} = 0$$ EQ 2.7

To confirm this behavior, measurements of a CNT FET were taken for all three conductance regimes as a function of source-drain voltage. For each measured source-drain voltage, the gate voltage was swept between ± 50 mV to extract the transconductance. The conductance was calculated as the measured drain current divided by the source-drain voltage, and the dynamic conductance was extracted as the slope of a linear fit to the drain current over the source-drain voltage over five points. The conductances are plotted in Figure 2.3.
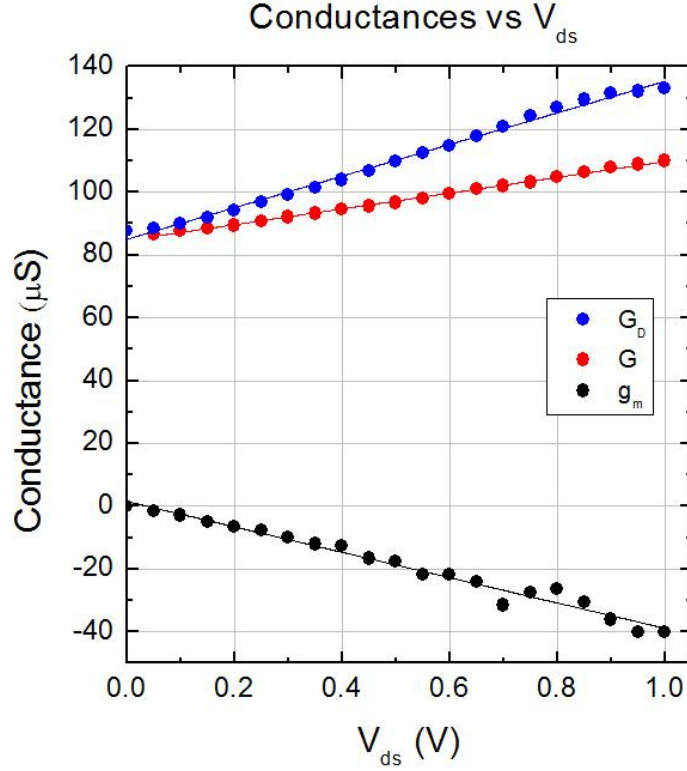
Figure 2.3 Plots of conductance, dynamic conductance, and transconductance for a CNT FET as a function of source-drain voltage. The lines correspond to linear fits to each conductance.

As expected at $V_{ds} = 0$, the transconductance is zero, and the conductance and dynamic conductance are equal. The slopes of the dynamic conductance and transconductance should be equal and opposite. Their ratio from Figure 2.3 is -1.25. The slope of the dynamic conductance should be twice that of the conductance. Their ratio from Figure 2.3 is 2. The correspondence of the measured conductances to EQ 2.2-4 confirms the form of the drain current in this linear region.

2.1.3 CNT FET Nonlinearities

The dependence of conductance on gate voltage and source-drain voltage makes the CNT FET's drain current non-linear in both input voltages. It is the non-linearity of CNT FETs that allows them to be used as mixers, as presented in Chapter

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5. There are two physical sources for this nonlinearity. The first comes from the source and drain contacts to the CNT. When materials with different work functions come into contact, electrons flow from the higher work function material to the lower work function material, accumulating in the interface until the Fermi levels are equal. These charges create a dipole between the materials and are responsible for bending of the conduction and valence bands. When the work function of a metal contact is less than the work function of a p-type semiconductor, the dipole created impedes hole transport from the metal to the semiconductor. The energy barrier associated with this dipole is called a Schottky barrier (Φ_B)[18, 19]. The metal contact material used in our devices is titanium, which has a work function of 4.33 eV. The work function of a p-type CNT ranges from 4.7 to 5.1 eV, so small Schottky barriers should exist at both ends of our channels. Ignoring the effect of the gate field, the conduction at low source-drain bias should be reduced in both directions by the Schottky contacts. When the bias is large enough, the Schottky barriers will be overcome and conduction should increase. This small difference in conductance should be symmetric about $V_{ds} = 0$ and is the first source of CNT FET nonlinearity.

The larger nonlinear behavior of the CNT FET drain current comes from the gate field. Since the gate fixes the Fermi level inside the semiconductor, the relative biases of the other two electrodes will determine the band bending, which can introduce barriers to conduction. When the gate, source, and drain are all grounded, the Fermi level is constant through all three materials. The potential energy diagram for this configuration is shown in Figure 2.4 a). Energy diagrams are typically drawn for electrons, so hole energy increases in the negative y direction. When a bias is

applied to the drain relative to the source, the Fermi level is fixed from the source

through the CNT, with most of the bias-induced band bending occurring at the CNT-

drain interface. When a positive drain bias is applied (Figure 2.4 b) the drain Fermi

level is lowered. Holes will move from the drain to the source in this configuration.

There are energy barriers for holes conducting from the drain to the CNT and from

the CNT to the source, both equal to Φ_B. When a negative drain bias is applied

(Figure 2.4 c) the drain Fermi level is raised. Holes will move from the source to the

drain in this configuration. The energy barrier for holes conducting from the source to

the CNT is still equal to Φ_B, but the barrier for conduction from the CNT into the

drain has been reduced to $\Phi_B - eV_{ds}$. This difference in energy barriers with drain bias

causes an asymmetry about $V_{ds} = 0$ in the channel conduction.
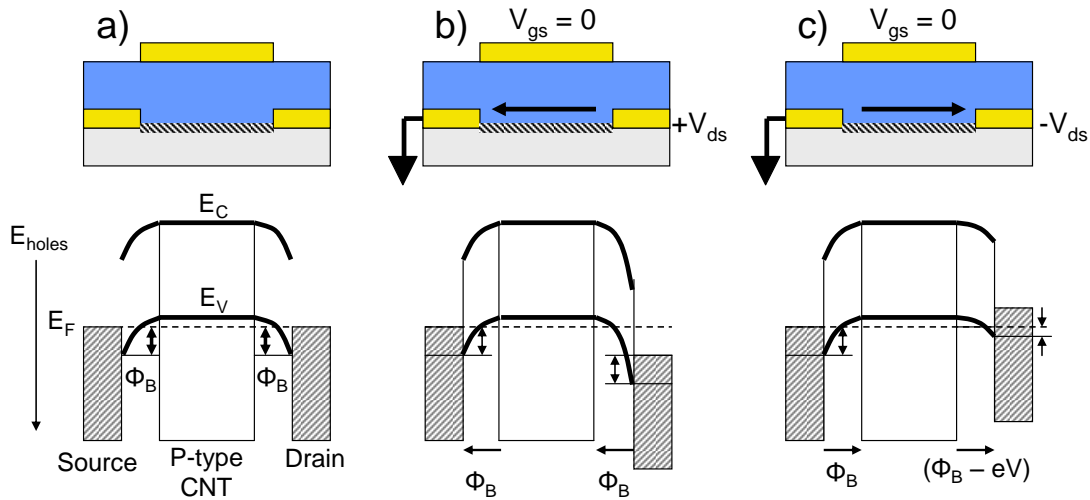
Figure 2.4 – Diagrams of a top-gated p-type CNT FET with corresponding potential energy diagrams for different source drain biases. a) Unbiased, Schottky contacts exist at the source and drain due to the work function difference of the metal contacts and p-type CNT. b) For a grounded gate and source and positive source-drain bias, holes conduct from right to left and energy barriers exist at both interfaces. c) For a grounded gate and source and negative source-drain bias, holes conduct from left to right and the energy barrier from the CNT to drain has been reduced.

This modeling assumes that the gate voltage relative to the source voltage

(V_{gs}) is parameter responsible for the position of the Fermi level in the

semiconductor, which is the convention most commonly used with FETs. This means that changing the voltage on the drain has no effect on the Fermi level inside the CNT. However, in a symmetric device geometry, the labeling of source and drain is arbitrary. If the gate voltage relative to the (V_{gd}) drain was used instead of V_{gs}, the effective gate voltage would be changing as source-drain bias changed. The real gating effect is a combination of V_{gs} and V_{gd}. It is more accurate to consider the gate voltage relative to the voltage in the center of the CNT as responsible for setting the Fermi level. This is only used in this section; the standard gating convention of V_{gs} is used for the rest of this dissertation.

To evaluate the energy bands with this as the Fermi level reference, the voltages are adjusted so that the center of the CNT is at ground. This is valid since it is the potential differences that are relevant, not the absolute potential. Energy diagrams with this labeling are shown in Figure 2.5. The gate and source are still at the same potential. When a positive bias (V) is applied to the drain relative to the source, the source has a potential of $-V/2$ while the drain has a potential of $+V/2$ (Figure 2.5 a). Similar band bending near the contacts as in Figure 2.4 b) is shown. However, since the gate potential is equal to the source potential, which is negative, the Fermi level relative to conduction and valence bands is lowered, increasing the number of carriers in the valence band and increasing conduction. When a negative bias is applied to the drain relative to the source, the source has a potential of $+V/2$ while the drain has a potential of $-V/2$ (Figure 2.5 b). Now the gate potential is positive, which raises the Fermi level relative to the conduction and valence bands, decreasing the number of carriers, and decreasing conduction.
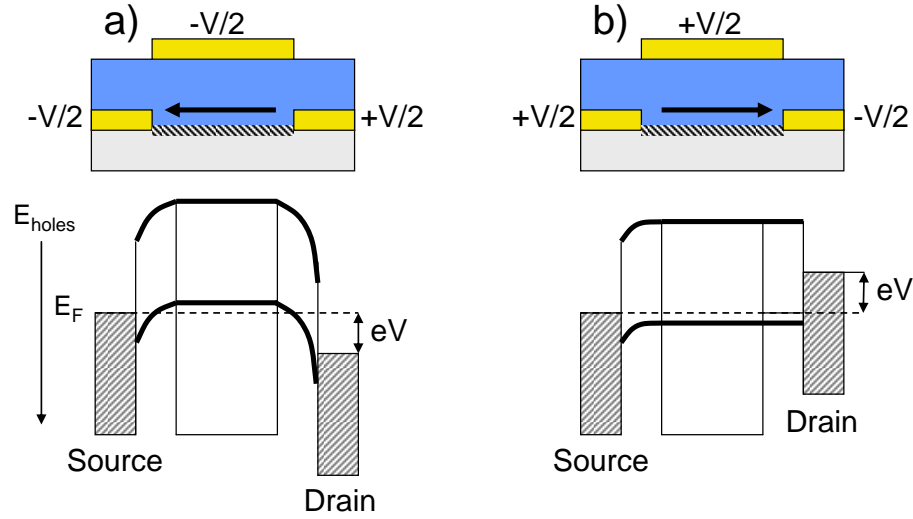
Figure 2.5 Diagrams of a top-gated p-type CNT FET with corresponding potential energy diagrams for different source drain biases. a) For a positive bias on the drain relative to the source, an effective negative potential exists at the gate, shifting the Fermi level down relative to the conduction and valence bands. b) For a negative bias on the drain relative to the source, an effective positive potential exists at the gate, shifting the Fermi level up relative to the conduction and valence bands.

The size of the energy barrier at both contacts and the relative position of the Fermi level both contribute to the nonlinear dependence of drain current on source-drain voltage. These nonlinear effects are directly seen in our CNT FET devices. Drain current vs. source-drain voltage measurements were made on a CNT FET with the gate electrode left floating to observe the nonlinear effects from the Schottky contacts and with the gate electrode grounded to observe the gate field induced nonlinearity. Plots of the resulting current and dynamic conductance of both measurements are shown in Figure 2.6.
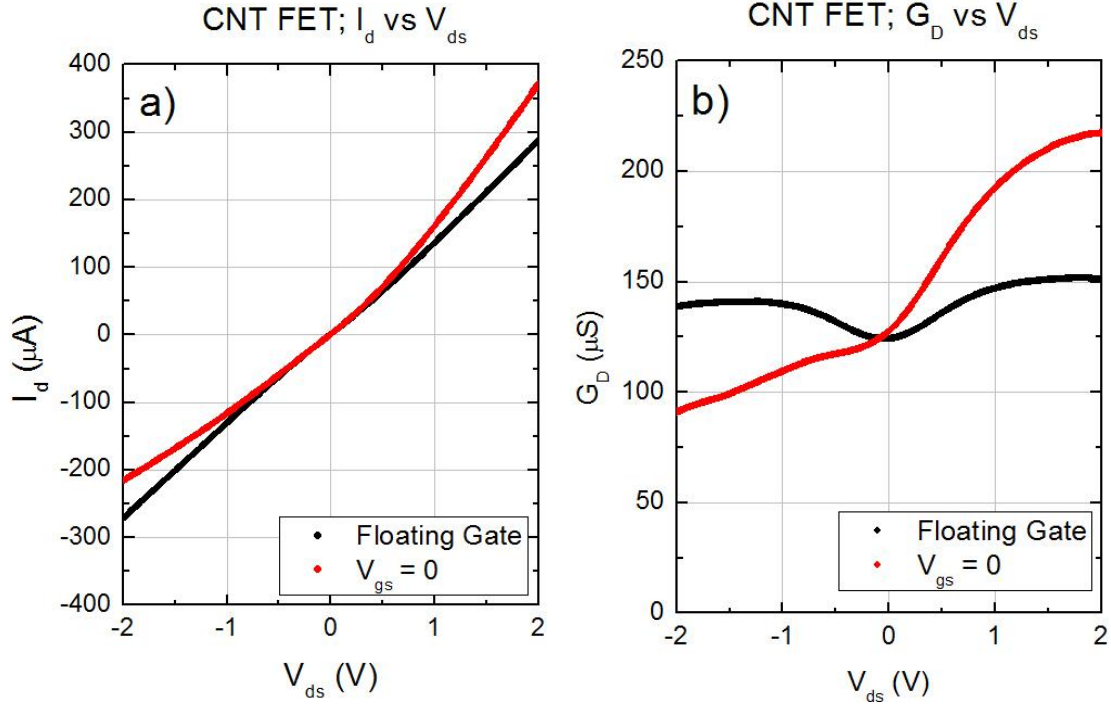
Figure 2.6 Plots of a) drain current and b) dynamic conductance of a CNT FET with a floating gate and with a grounded gate. When the gate is floating, the deviations in the dynamic conductance with source-drain bias are due to Schottky contacts. When the gate is grounded, the deviations in dynamic conductance with source-drain bias are due to the gate field. The dynamic conductance was calculated from a linear fit over 100 mV.

The dynamic conductance plots demonstrate the asymmetry expected from the potential energy diagrams. The effects of Schottky contacts are visible as a reduction in conductance for low bias. A slight asymmetry in that curve is visible, likely due to slightly different contact resistances for the source and drain. The contact resistance can be extracted by comparing the resistance at zero bias where the contacts contribute, to the resistance at ± 2 V when the Schottky contacts have been overcome. In this device, which was composed of hundreds of CNTs, the contact resistance is near 4 kΩ. When the gate is fixed, the field it produces breaks the symmetry in the dynamic conductance. The gate-induced nonlinearity in the CNT FET drain current has a larger effect than the nonlinearity due to the Schottky contacts. It is this gate-

induced nonlinear behavior that will be used in the mixing experiments reported later in this dissertation.

2.2.1 Device Substrate Selection

The most commonly used device substrate for micrometer-scaled electronics is a silicon wafer with a silicon dioxide layer. The conductive silicon can act as a global bottom gate in field-effect transistors (FETs), and the thermal oxide layer provides a robust insulating dielectric. Lithography on silicon is well-established, so the only new obstacles in fabricating carbon nanotube (CNT) FETs involves growing and patterning the CNTs. The global silicon back gate is convenient in not requiring the extra fabrication steps for adding a local top-gate, and its presence aids in the removal of metallic CNTs from the network, as will be discussed in Chapter 4. However, it is not always ideal. Integrated circuits with multiple FETs will require local gating, with the output of one FET feeding into the gate of another. In such cases, one could ignore the global back gate and add local top-gates in integrating devices. For DC applications, that solution is appropriate. However, for AC applications, especially as frequencies approach radio and microwave frequencies, the presence of the conductive silicon layer will add unwanted parasitic capacitance. Every metal electrode will be capacitively coupled to the silicon layer through the thermal oxide, like a parallel plate capacitor, which is in turn capacitively coupled to every other metal electrode. This extra capacitance will short every electrode together as frequency is increased. One solution researchers use to overcome this problem is to

use highly resistive silicon substrates. Lower conductivity in the silicon will reduce the capacitive coupling but not eliminate it. For our high frequency (HF) devices, which are designed to operate at 1 GHz and above, we use insulating substrates. Control devices fabricated on Si/SiO_2 substrates are mentioned in Chapter 4. The step by step fabrication procedure we follow for a CNT FET on a Si/SiO_2 substrate is given in Appendix A.

The last decade has shown a lot of interest in flexible electronics. Liberating circuits from rigid substrates can have many advantages, such as less expensive materials, adjustable sizes, such as a display that can roll up like a scroll, and potentially fully transparent circuits, as many of the commonly used thermal plastic substrates are optically transparent. It also allows for new applications, such as smoothly integrating electronics into living anatomy[20]. Fabricating devices on plastics presented new challenges since many of the chemical processes involved in silicon lithography would damage or dissolve most plastic substrates. The method our group developed to build devices on plastic was to fabricate each layer using standard photolithography on silicon wafers first, and then transfer print each layer sequentially to a plastic substrate. Our transfer printing process uses a nanoimprint lithography machine to facilitate transfer from the hard silicon substrate to the soft plastic one and is well documented in other publications.[21-26] Alignment is the biggest limitation in our ability to fabricate devices on plastic. Our alignment of subsequent layers is limited to around 5 μm resolution, which is insufficient for our HF FETs. This is only a limitation of our equipment, not a fundamental limitation of plastic electronics. Though some devices were transfer-printed into plastic, our HF

measurements were all performed on devices on quartz substrates. The step-by-step fabrication procedure we follow for a CNT FET on a plastic substrate (polyethylene terephthalate) is given in Appendix B.

One economic and simple way to grow single-walled carbon nanotubes is via chemical vapor deposition (CVD). After depositing a ferritin catalyst solution onto a substrate surface, the sample is heated in a tube furnace to nearly 1000 °C and a carbon-containing gas is introduced. The carbon nanotubes assemble themselves in this environment. On most substrates there is no preferred growth direction, so the result is a random network with CNTs going in all directions. While these random networks can have useful bulk properties,[27, 28] for most applications one would prefer to have all the CNTs aligned along the same direction, with each CNT connecting the source and drain. Since many of the CNTs in a random network will not bridge the channel themselves, the current will pass from tube to tube as it passes through the channel. Each tube crossing adds unwanted impedance and metallic CNTs will inevitably be a part of the current pathway through channel. This will make it impossible to completely remove all the metallic CNTs from the network, as will be discussed in Chapter 4.

In 2005, John Roger's research group at Northwestern demonstrated aligned CVD growth of CNTs, under certain conditions, on quartz substrates.[29] The alignment was due to using quartz wafers that had been "miscut" at a small angle off the 011 plane. It was previously thought that the miscut produced periodically spaced atomic steps, along which the single-walled CNTs grew, but more recently it has been suggested that alignment is due to anisotropy in polarizability along the quartz surface

bond orientations.[30] Whatever the mechanism, the ability to easily grow aligned

CNTs via CVD made quartz the substrate of choice for most of our devices. The lack

of a conductive back plane also made it a suitable substrate for our high frequency

devices.

2.2.2 CVD Growth and Lithography

For our device substrates, we used 3-inch-diameter single crystal quartz

wafers (0.5 mm thick, ST-cut 42°45', single-side polished (SSP), from Hoffman

Materials). To prevent the CNTs from growing in all directions, producing a random

network, thermal annealing in air for 12 hours at 900 °C is necessary before growth to

prepare the surface. The catalyst that we used for our nanotube growth was ferritin

purchased from Sigma Aldrich, a protein complex that contains iron nanoparticles.

Ferritin was deposited onto the sample surface by dipcoating, submerging the sample

in a dilute solution for twenty minutes. This distributes ferritin catalyst particles over

the whole sample surface. The sample is then rinsed with deionized water, blown dry

with nitrogen, and placed in a tube furnace for CVD growth. The sample is then

heated in air to 700 °C to burn away the organic ferritin protein complex, leaving

behind iron nanoparticles. It is then cooled to room temperature and re-heated up to

925 °C under hydrogen to prevent the particles from oxidizing. Methane is then

introduced at a flow rate of 1000 sccm to grow the CNTs. After 20 minutes the

methane is turned off and the sample is cooled to room temperature under hydrogen.

A scanning electron microscope (SEM) image of the resulting CNT array on the quartz surface is shown in Figure 2.7.

Not all CNTs are perfectly aligned. This is due to the large number of ferritin particles covering the surface, which will occasionally block the straight growth of a CNT. This alignment is still preferred to a random network. The typical CNT density for our samples ranged from 1 to 3 CNTs per micrometer.
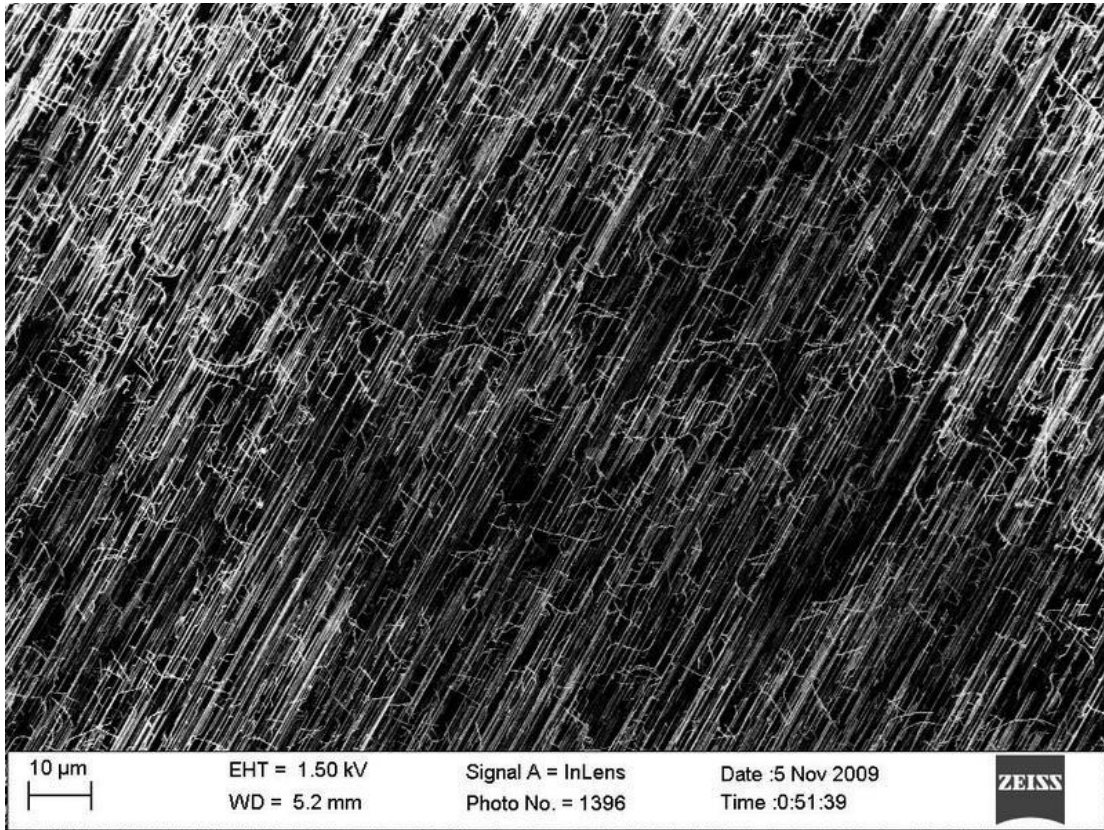
Figure 2.7 SEM image of aligned CNTs grown on a quartz substrate by chemical vapor deposition (CVD).

After the CNTs are on the quartz substrate, source and drain electrodes consisting of 5 nm of titanium and 50 nm of gold are deposited via photolithography. Alignment marks for the remaining layers are also patterned in this step. Since the CNTs are grown over the entire surface, the channels of each device are covered with

photoresist and the uncovered CNTs are destroyed with an oxygen plasma. This step

defines the channel width. A 65 nm Al_2O_3 dielectric layer is then deposited via

atomic layer deposition (ALD) and lithographically patterned afterward with a

buffered oxide etch. Lastly, 100 nm gold local top-gates are added, again with a 5 nm

titanium adhesion layer. A detailed step-by-step procedure that we used to fabricate

our CNT FETs on quartz, including the CNT growth parameters and lithographic

recipes, is given in Appendix C.

2.2.3 Device Geometries

The field-effect transistor geometry used for our carbon nanotube devices is

shown in Figure 2.8. We utilize two carbon nanotube channels that share one drain

electrode and have separate outer source electrodes. The top local gates for each

channel are connected together at the gate contact pad. This device geometry was

chosen because of the ground-signal-ground (GSG) high frequency probes used for

AC measurements. The center electrode (signal) of one probe contacts the drain

electrode while the center electrode (signal) of the other touches the gate. The

grounded outer electrodes of both probes contact both source electrodes. The pitch of

the probes used was 150 μm, so the spacing between each contact pad is also 150 μm.

Devices were made with different channel widths (*W*), channel lengths (*L*), and gate

lengths (*G*). The channel width is set by etching the CNTs into different-sized strips,

producing channel widths of 100, 50, 25, 5, and 0 μm. The channel lengths ranged

from 1 to 75 μm. The gate lengths varied from overlapping the channel by 5 μm to

leaving 5 μm of the channel uncovered by a gate. The purpose of a gate electrode not spanning the whole channel is to reduce the parasitic capacitance that comes from a gate-to-source and gate-to-drain overlap. The standard device geometry used for most measurements in this dissertation had a 100 μm channel width, 10 μm channel length, and 8 μm gate length.
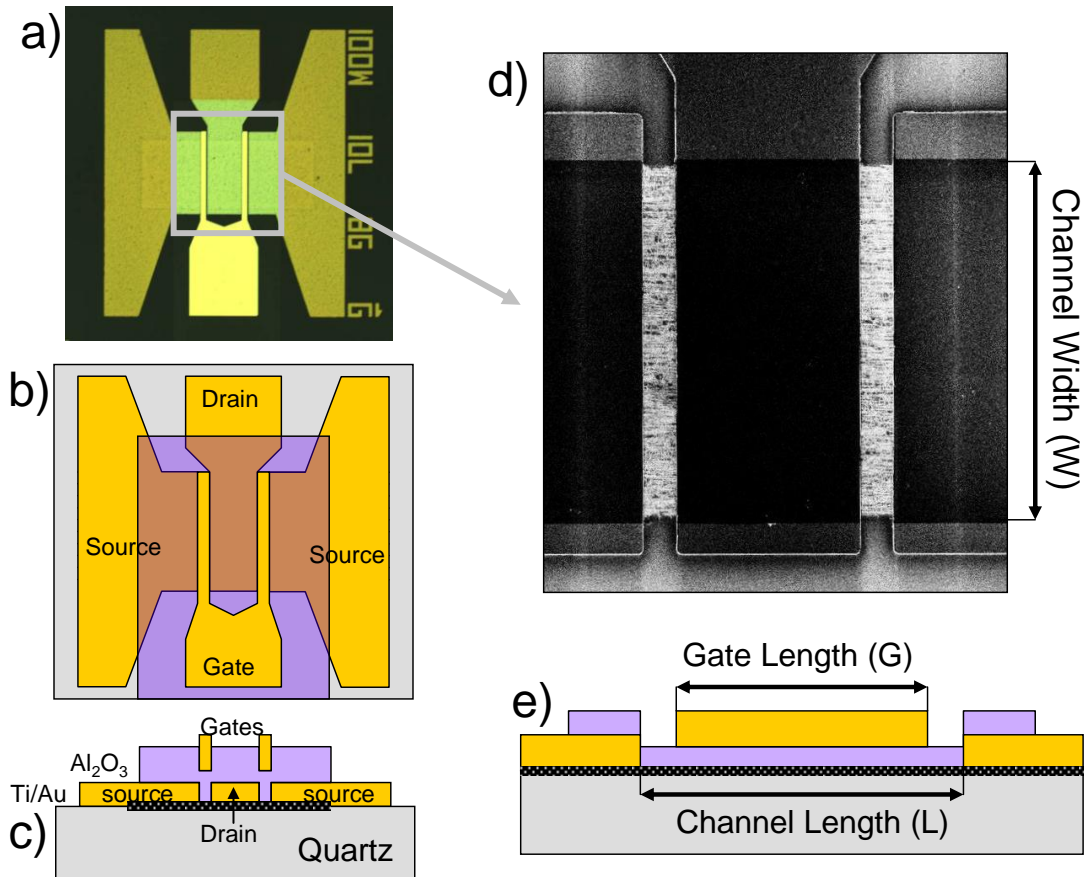
Figure 2.8 a) An optical image of a completed CNT FET in a high frequency probing geometry. b) A top-view diagram of the same CNT FET geometry with the source, drain, and gate electrodes labeled. c) A side-view diagram of the same CNT FET geometry showing the substrate, source and drain electrodes, Al_2O_3 dielectric layer, and top-gate electrodes. d) An SEM image of the nanotubes in a CNT FET dual channel before the dielectric layer and gate are added. The channel width is labeled. e) An enlarged side-view diagram of a single channel showing the gate length and channel length. Diagrams are not to scale.

Other components were also fabricated on each CNT FET device chip to be used as calibration references and controls. Each included ground pads on each side

of the device in the same 150 μm GSG spacing to enable probing in the same configuration. The calibration references were open and through electrodes, used for impedance calibration in vector network analyzer (VNA) measurements. They are shown in Figure 2.9. All nanotubes near these electrodes were removed.
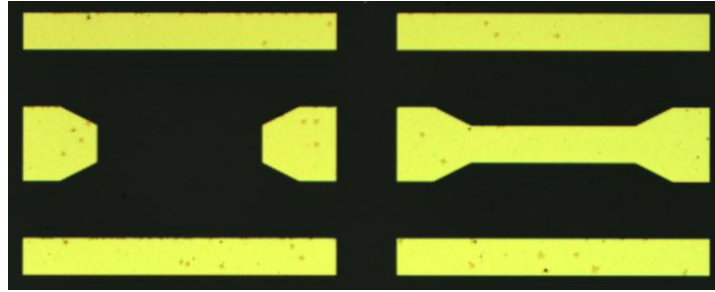
Figure 2.9 Optical images of the open and through electrodes used for VNA calibration.

Lastly, parallel plate capacitors with different plate sizes were also fabricated to function as AC controls and to verify our capacitance measurement techniques. Optical images of the fabricated capacitors and the side-view diagram showing the dielectric and metal layers are shown in Figure 2.10. DC calculations and AC measurements were used to extract the capacitances of these devices and of the CNT FETs. The details of those calculations and measurements are given in Appendix D.
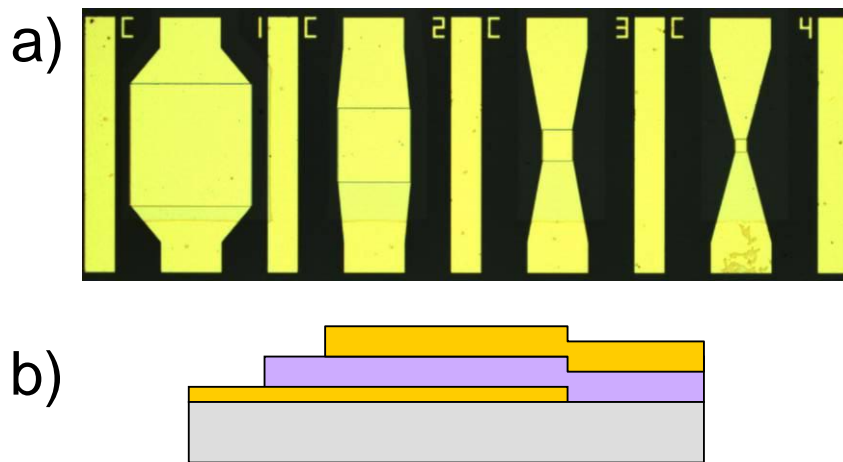
Figure 2.10 a) Optical image and b) side-view diagram of fabricated parallel plate capacitors.

Chapter 3: Charge Traps

3.1 Introduction to Charge Traps and Hysteresis in CNT FETs

In an ideal dielectric material, local charges are able to freely move within the material in response to an external field inducing a polarization, but they cannot conduct into adjacent materials. When the external field is removed, the charges should go back to an electrically neutral arrangement. However, in real materials, solids are rarely perfect crystals. Any variation in the atomic lattice, called a defect, will produce a local change in the electric potential, which will attract or repel free charges. These defects include the absence of an atom from a lattice point, leaving behind dangling bonds, or an extra or different kind of atom at a lattice point. Surfaces will also provide a local potential change because the bonds of an atom at the surface of a material will be terminated differently than the atoms in the bulk of the material. The interface joining two materials is a common location for defects since different materials can have different lattice shapes and spacings. Also, conduction between a dielectric and a conductor is possible through tunneling. When an external field is applied through a real dielectric material, free charges may become trapped at defect sites, such that when the field is removed, they remain fixed, preventing the material from returning to an electronically neutral state. In a field-effect transistor, the population of these trap states is strongly dependent on the applied electric field (i.e. gate voltage) and is visible as an offset between electrical measurements acquired with increasing, as opposed to decreasing, gate voltage. This difference in current with sweep direction is due to the trap occupations that occurred at previous gate voltages, the history of the electric field. Thus, it is referred to as

hysteresis and is commonly seen in carbon nanotube field-effect transistors (CNT

FETs) with SiO_2 dielectric layers and is most often attributed to charge traps in the

dielectric layer or in water molecules on the dielectric surface if the CNTs are

exposed to air.[31-42]

The presence of trapped charges affects the CNT conduction by screening the

gate voltage from reaching the CNT. It can be thought of as follows: When the gate

voltage is negative, electron traps are being evacuated and leaving behind positive

holes, so when sweeping the gate voltage in the positive direction, the field reaching

the CNTs is more positive, so the drain current magnitude is decreased. For positive

gate voltages, electron traps are being filled, reducing the number of positive empty

traps, so when sweeping the gate voltage in the negative direction, the field reaching

the CNTs is less positive (more negative), so the drain current magnitude is increased.

A transfer curve of a CNT FET device is shown in Figure 3.1. The magnitude of the

hysteresis is quantified by the difference in threshold voltage (ΔV_{gs}) between the two

sweeps and by the difference in drain current at $V_{gs} = 0$ (ΔI_d).

For devices with significant hysteresis, one cannot accurately predict what the

drain current will be at a particular source-drain and/or gate voltage; the output

depends on how the device arrived at those voltages, the device history. For some

applications, such as memory devices, hysteresis can be exploited to serve a

function,[31, 43-45] but in typical field-effect transistors, it is problematic both for

extracting physical parameters from a device and for impedance matching when

integrating FETs into circuits. In order to reduce the problems associated with

hysteresis, the behavior of drain current as a function of time and gate voltage is investigated.
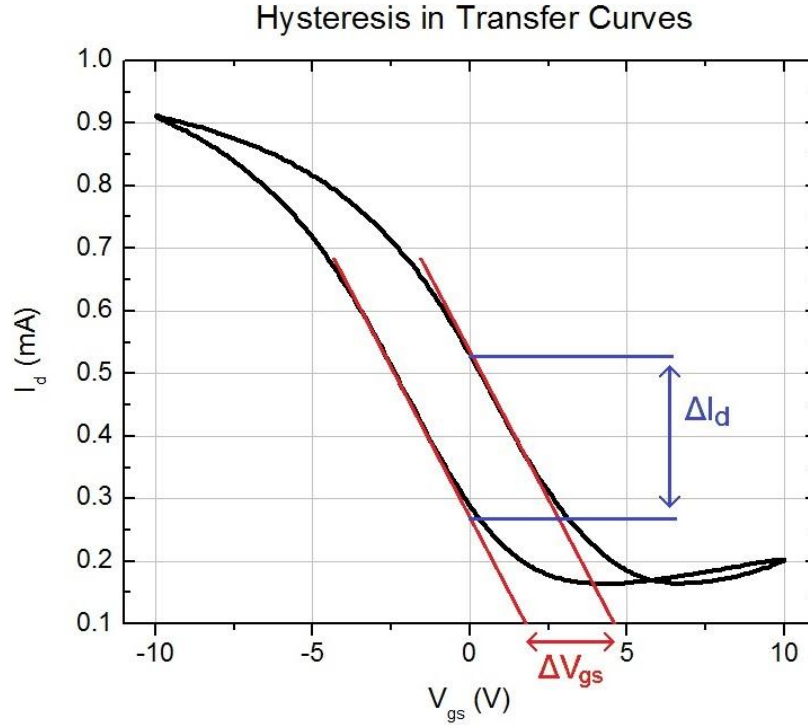
Figure 3.1 Plot of a transfer curve taken at $V_{ds} = 5$ V of a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm) demonstrating hysteresis. The change in threshold voltage and drain current at $V_{gs} = 0$ is shown.

3.2 Measurements of Traps Emptying Over Time

The most commonly referenced analysis of hysteresis in CNT FETs was published by Slava Rotkin in 2005.[41] Charge traps were modeled as a single cylindrical trap surrounding the CNT. The total potential (EQ 3.1) was a combination of the gate voltage (V_{gs}), a fitting parameter (V_-), the potential due to the cylindrical trap (V_T), and charge distribution on the CNT (ρ). The Fowler-Noidheim tunneling mechanism was used to account for charges moving from the CNT into a trap state in

the dielectric layer (EQ 3.2), and the charge distribution was calculated from the CNT

density of states (v) and Fermi distribution at the total potential (EQ 3.3). The drain

current was then calculated as the source-drain voltage divided by the nanotube

resistance. There is no closed form solution for the drain current in this model, but

numerical simulations can be made. All the physical values used with this model are

given in the article.

$$\phi = V_{gs} - V_- + V_T(\phi,t) + \frac{\rho(\phi,t)}{C_G} \qquad \text{EQ 3.1}$$

$$V_T(\phi,t) = \frac{2\pi R_T}{C_T} N_T \left[1 - \exp\left(\frac{-J_{FN}(\phi)\sigma}{e}t\right)\right] \qquad \text{EQ 3.2}$$

$$\rho(\phi,t) = e \int v(E) f[E + e\phi - \Delta] dE \qquad \text{EQ 3.3}$$

$$I_d(\phi,t) \approx \frac{V_{ds}}{L/e\mu\rho(\phi,t)} \qquad \text{EQ 3.4}$$

Transfer curve hysteresis was analyzed as a function of both gate voltage

sweep rate and maximum/minimum voltages values. As expected from a tunneling

mechanism, the more slowly the gate voltage is swept and the larger the bounds, the

greater the hysteresis. Rather than analyze the hysteresis in transfer curves, as has

been done already, we chose to observe how drain current changes over time after a

change in gate voltage.

As mentioned in Chapter 2, Our CNT FETs on quartz substrates are

encapsulated in atomic layer deposited (ALD) Al_2O_3 dielectric layers. Encapsulation

eliminates the charge traps associated with water molecules in the air and

significantly increases the operational lifetime of the device. Most of the devices

measured throughout this dissertation were over one year old. ALD is known to produce very pure, pin-hole free dielectric layers.[46, 47] However, CNT walls are inert to most ALD precursors,[48, 49] producing an imperfect interface between the CNT and the dielectric bulk, providing a possible source for charge traps.

Most of the following measurements utilize the gate voltage waveform shown in Figure 3.2. The gate voltage was first held at ground, then a short voltage pulse of duration T_{on} and magnitude V_{gs} was applied to the gate. The gate voltage was then returned to ground for a duration of T_{off} at which time an opposite gate voltage ($-V_{gs}$) pulse was applied. Data acquisition is performed only during the T_{off} time interval where $V_{gs} = 0$. $T_{off} = 100$ s for all the data presented in this section. The source-drain voltage is held fixed throughout all measurements.
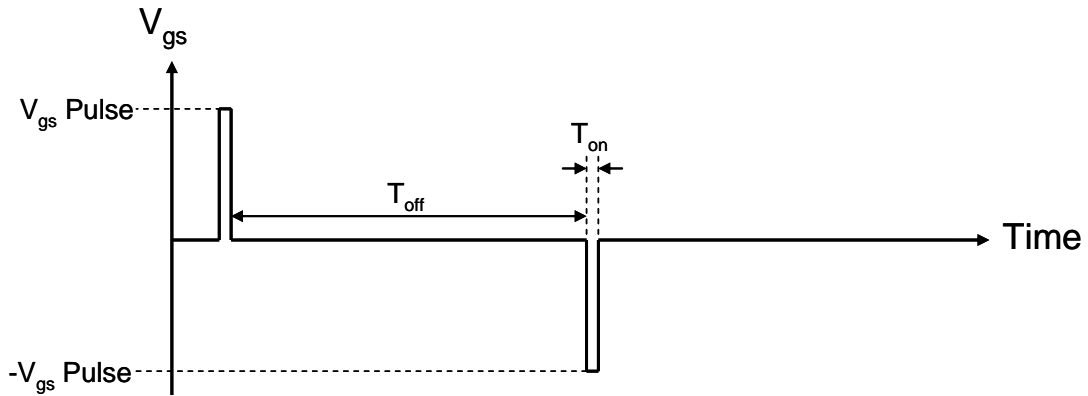
Figure 3.2 Diagram of the gate voltage waveform used to observe charge traps empty after short pulses on the gate. The gate is held at ground until it is pulsed with the magnitude V_{gs} Pulse for T_{on}. Then the gate is returned to ground for T_{off} to allow the charge traps to empty. Then the gate is pulsed with the magnitude of $-V_{gs}$ Pulse for T_{on}, and again returned to ground for T_{off}.

Drain current data for a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm) for both a positive and negative gate pulse, ($T_{on} = 1$ s, $T_{off} = 100$ s, V_{gs} Pulse $= 1$ V) are shown in Figure 3.3. This type of data will be referred to as discharge data. $t = 0$ is set when gate voltage is returned to zero during the T_{off} interval. The response from the

positive and negative gate pulses are plotted together on the same time axis for direct

comparison. Measurements were made with a Keithley 2612A sourcemeter, which is

limited to ~ 500 μs pulses. The sourcemeter was controlled with Keithley's Test

Script Building software, which uses the Lua programming language.
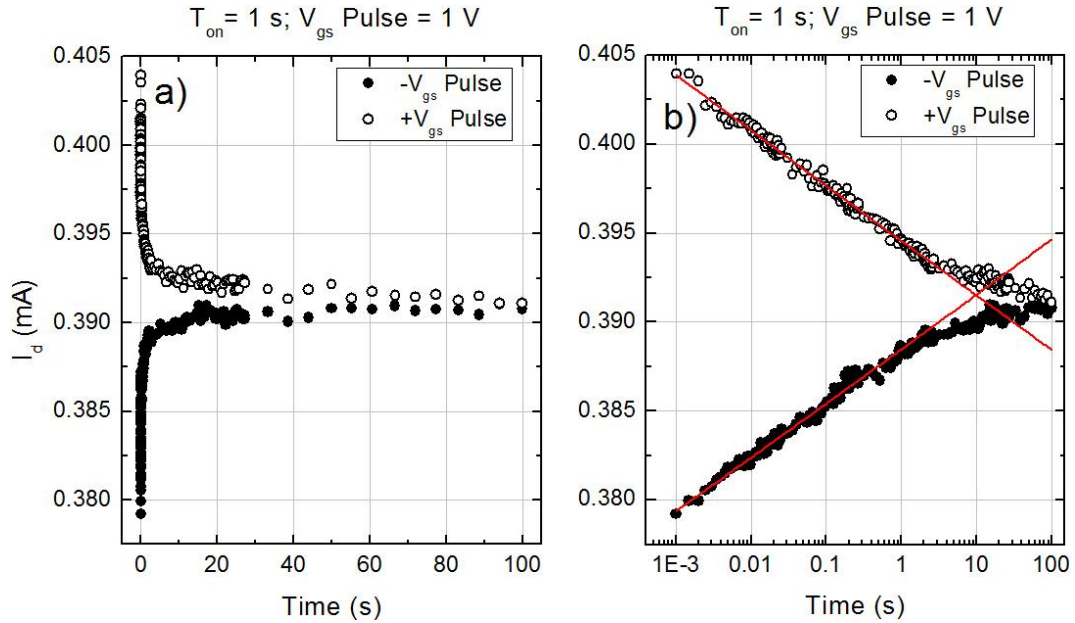
Figure 3.3 Plots of discharge data over the 100 s T_{off} interval for $T_{on} = 1$ s and V_{gs} *Pulse* = 1 V. The black circles correspond to $-Vgs$ *Pulse* and the white circles correspond to + V_{gs} *Pulse*. a) is plotted on a linear scale and b) is a linear-log plot. The red lines correspond to logarithmic fits to the data.

Plotting using a linear time scale (Figure 3.3 a), the discharge data indicates

that the majority of the change in current after both gate voltage pulses occurs in the

first second. The same data is replotted on a logarithmic scale for the time axis

(Figure 3.3 b) and fit to the logarithmic function given in EQ 3.5. Eventually, the

drain current reaches an equilibrium value and stops following this trend, seen as

deviations from the red lines in Figure 3.3 b). This equilibrium current value ($I_{eq} = I(t$

$= \infty$)) is included in EQ 3.5 to highlight the deviations from equilibrium over time.

The logarithmic dependence on time will only last until the current reaches

equilibrium, at which point it will remain constant.

$$I_d(t) = I_{eq} + I_0 + ALOG\left(\frac{t}{t_0}\right) \qquad \text{for t < t}_{eq} \qquad\qquad \text{EQ 3.5}$$

In EQ 3.5, I_0 is referred to as the initial drain current offset and is equal to the

drain current difference from I_{eq} at t = t_0 after a change in gate voltage (during T_{off}). t_0

was chosen to be 1 ms because it is near the limit of our equipment measurement

resolution. The slope of the equation, A, is referred to as the discharge rate because it

specifies the slope (on a linear-log plot) of the drain current approaching equilibrium.

In the next section, we acquire discharge data as functions of the two variables (T_{on}

and V_{gs} *Pulse*) in our gate voltage measurement waveform (Figure 3.2). That data is

then fit to the logarithmic equation given in EQ 3.5 and analyzed in terms of I_0 and A.

The purpose of this analysis is to gain insight into methods for minimizing the effect

of hysteresis. This logarithmic dependence with time of the drain current was

observed in simulations following the previously mentioned Rotkin charge trap

model. However, the model did not yield any significant dependence on the gate

voltage pulse duration nor the voltage pulse magnitude, so a more accurate model,

including a distribution of trap depths, would be needed to compare with our

measurements.

3.2.1 Dependence on Pulse Duration

Discharge data measurements were performed on a CNT FET with V_{gs} *Pulse*

= 1 V, and different T_{on} durations are shown in Figure 3.4. The points at the top of the

graph (negative slope) correspond to positive gate voltage pulses, while the points at

the bottom (positive slope) correspond to negative gate voltage pulses.
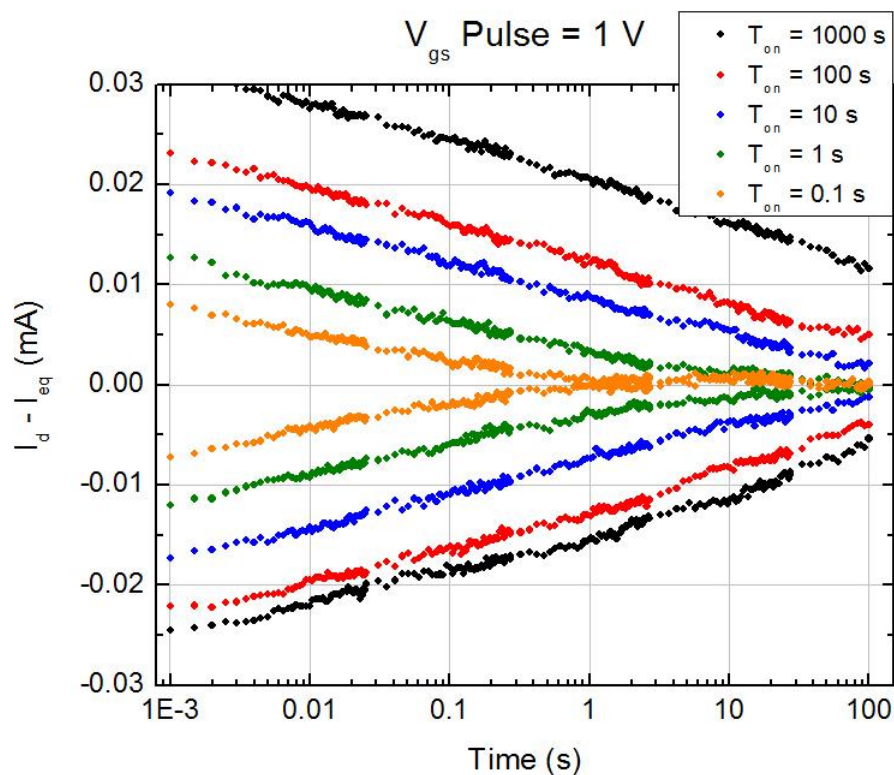
Figure 3.4 Plot of discharge data over 100 s for V_{gs} *Pulse* = 1 V and several values of T_{on} on a logarithmic time scale. The initial offset current values are seen to depend strongly on T_{on}.

For T_{on} = 100 ms, the charge traps that were filled during the gate pulse are

mostly unoccupied after the first second into T_{off}. For T_{on} > 1 s the effects of filled

traps are still evident after 100 s. The data from these measurements were fit to

logarithms with time, and the extracted parameters are plotted vs. T_{on} in Figure 3.5 for

V_{gs} *Pulse* = 1 and 5 V. Since deviations from the logarithmic behavior occur when the

drain current approaches equilibrium, fits were made over the first 100 ms of

discharge data. The discharge rate will be referred to as the initial discharge rate, *A*.
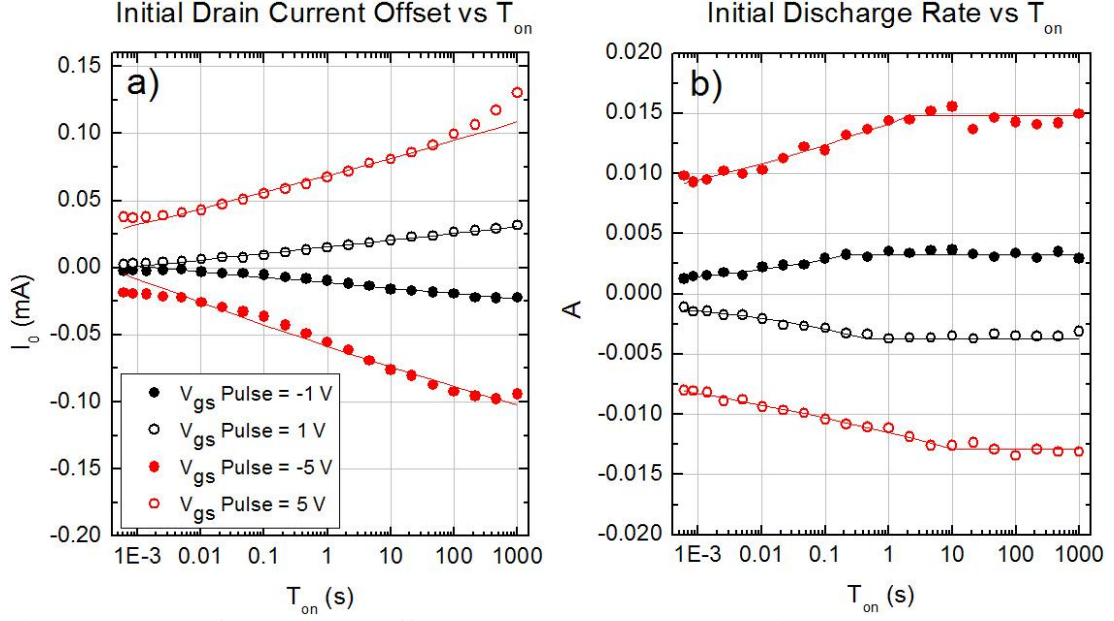
Figure 3.5 Plots of a) the initial offset current values and b) the initial discharge rates vs. T_{on} for V_{gs} *Pulse* = 1 V and V_{gs} *Pulse* = 5 V. For both, T_{on} is plotted on a logarithmic scale. The initial offset current is defined as the current 1 ms after the gate transition from $\pm V_{gs}$ *Pulse* to ground. The initial discharge rate is derived from a logarithmic fit to the discharge data during the first 100 ms.

For most values of T_{on} the initial offset drain current follows an additional logarithmic trend with T_{on}, shown as lines fit to the data. This dependence on the Logarithm of T_{on} demonstrates the advantages of using equipment capable of sourcing short pulse widths. T_{on} must be reduced by orders of magnitude to substantially reduce the initial offset current. This indicates that the longer the gate is held at a non-zero bias, the more trap states are filled. The lesson from this trend is that the key to not populating charge traps with long decay times is to only use short pulses on the gate when sourcing non-zero voltages.

The initial discharge rate, A, initially also depends logarithmically on T_{on} before reaching a maximum value. For the V_{gs} *Pulse* = 5 V data, leveling off occurs near T_{on} = 10 s. Considering that our fitting regime was 1 – 100 ms, this suggests that even trap states filled after long periods of gating will begin to empty immediately

(within 1 ms). This trend eventually ends, and traps filled at very long periods of gating will not contribute to the initial discharge rate.

Though the discharge rate increases with T_{on}, this increased slope does not compensate for the larger initial offset drain current. Therefore, I_0 is the more informative parameter. Employing the lesson from these measurements, in the next experiment, discharge data was taken for $T_{on} = 1$ ms as a function of the gate voltage pulse magnitude.

3.2.2 Dependence on Pulse Magnitude

Discharge data measurements were performed on a CNT FET with $T_{on} = 1$ ms and five equally spaced values of V_{gs} *Pulse* are shown in Figure 3.6. The points at the top of the graph (negative slope) correspond to positive gate voltage pulses, while the points at the bottom (positive slope) correspond to negative gate voltage pulses.
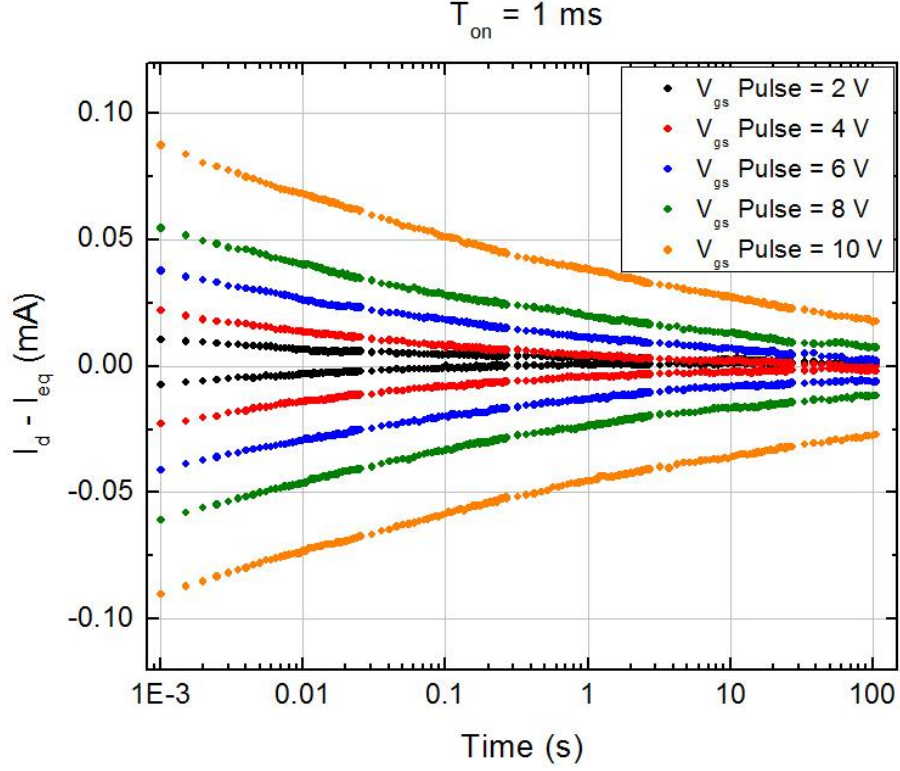
Figure 3.6 Plots of discharge data over 100 s for T_{on} = 1 ms for several values of V_{gs} *Pulse* on logarithmic time scales. The initial offset current values and the slopes of the discharging currents can be seen to depend on V_{gs} *Pulse*.

The curvature of the discharge data on a log-log plot slightly deviates from the logarithmic trend even for V_{gs} *Pulse* = 10 V which is not near equilibrium at the end of the 100 s T_{off} period. For T_{on} = 1 ms the traps filled in 2 and 4 V gate pulses mostly empty in 100 s. For the larger gate voltage magnitudes, 100 s is not long enough for the current to reach equilibrium, even with the minimum T_{on} duration we can apply. The data from these measurements were fit to logarithmic equations, and the extracted parameters are plotted vs. V_{gs} *Pulse* in Figure 3.7.
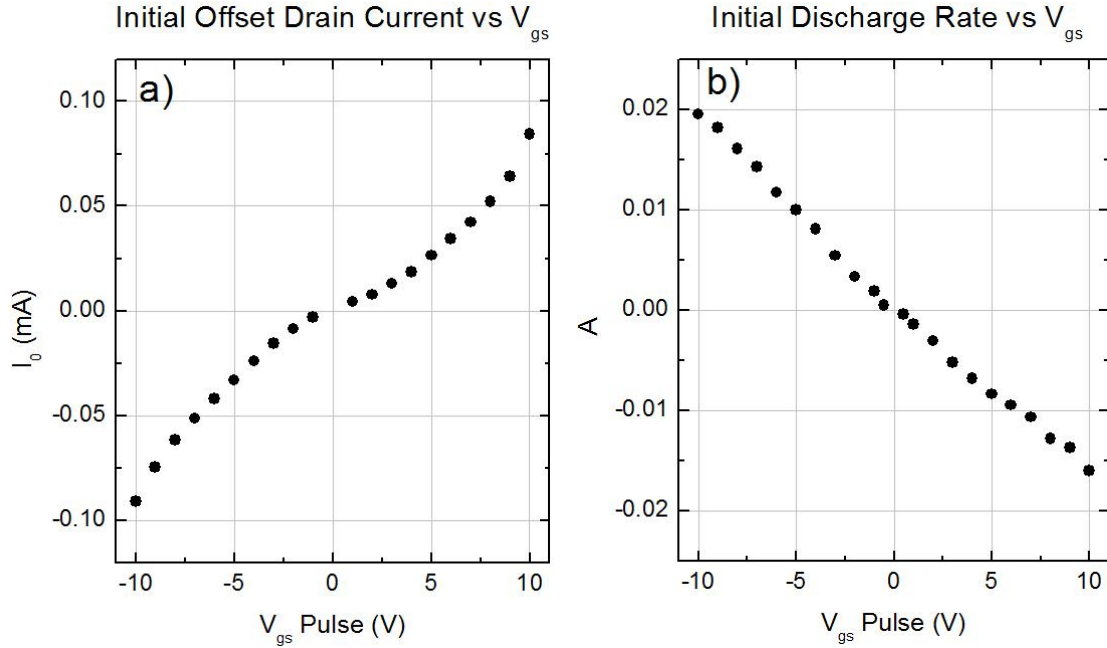
Figure 3.7 Plots of a) the initial offset current values and b) the initial discharge rates vs. V_{gs} *Pulse* for $T_{on} = 1$ ms. The initial offset current is defined as the current 1 ms after the gate transition from $\pm V_{gs}$ *Pulse* to ground. The initial discharge rate is derived from a logarithmic fit to the discharge data during the first 100 ms.

The initial offset drain current is approximately linearly dependent on V_{gs} *Pulse* for small voltage magnitudes, with larger than linear offsets induced for large values of V_{gs} *Pulse*. The initial discharge rates follow a linear relationship with V_{gs} *Pulse*. This direct dependence of trap occupation on gate voltage magnitude indicates that the gate voltage could be used to fill and empty trap states in a predictable way.

The initial offset drain current is seen to depend directly on both the gate voltage pulse duration (T_{on}) and magnitude (V_{gs} *Pulse*). The logarithmic dependence on duration indicates that using short pulses will minimize the number of traps occupied during a non-zero gate voltage pulse. However, even when using 1 ms pulses, 100 s of T_{off} is not enough time for all the traps filled at large voltage magnitudes to empty, as seen in Figure 3.6. Projecting the trend forward, it would take orders of magnitude more time for some of the measured currents to reach

equilibrium. Rather than waiting for them to empty, we use the trap occupation

dependence on gate voltage to force the occupied traps to empty in a controlled

fashion. The process will be modeled in the next section.

3.3 Preisach Model of Hysteresis

The presence of charge traps in our encapsulated CNT FETs is a consequence

of the materials and deposition methods we have available. We would therefore like

to minimize their effects during measurements, most notably by reducing the

hysteresis in transfer curves. Since hysteresis is caused by having different charge

trap occupations when different measurements are taken, one solution is to set a

default trap occupation in between measurements. We have seen that both time and

gate voltage affect trap occupation. One solution is to set the gate voltage to ground

after each measurement pulse and wait for the filled traps to empty, but as we have

seen, for large gate voltages the length of time until the drain current reaches

equilibrium can be orders of magnitude larger than 100 seconds, an impractical time-

period between measurements. Instead we focus on using the gate effect to set a

default trap occupation.

Ignoring the time dependence allows us to use the Preisach hysteresis model[50,51] to predict what kind of gate voltage waveform might set a default trap occupation.

This model is regularly used with ferromagnetic systems but has not been widely

applied to electronic hysteresis. The Preisach model approximates hysteresis by

representing data as a collection of hysterons. A hysteron is a simple relay whose

output is 0 if the input is less than α, 1 if the input is greater than β, and maintains its previous value if the input is between α and β. A diagram of a hysteron is shown in Figure 3.8 and its output is given by EQ 3.6.
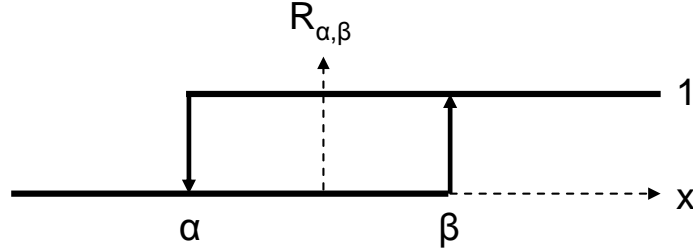
Figure 3.8 Diagram of a hysteron relay: x is the input, y is the output, and α and β are the transition x values.

$$R_{\alpha,\beta}(x) = \begin{cases} 0 & for & x < \alpha \\ 1 & for & x > \beta \\ k & for & \alpha < x < \beta \end{cases} \qquad k = \text{previous y value} \qquad \text{EQ 3.6}$$

Figure 3.9 shows how a hysteron can be related to a single trap state in a CNT FET. At point a, the positive field from the gate draws an electron into the trap. A trapped electron produces a negative field that encourages p-type CNT channel conduction, so the output from that trap is one and the relay is considered on. At point b the gate field has been removed, but the electron remains trapped, so the relay is still on. At point c the negative gate voltage emptied the trap, leaving behind a hole that produces a positive field, diminishing CNT channel conduction, so the output from the trap is 0 and the relay is considered off. At point d the gate field has been removed, but the hole is still trapped, so the relay is still off.
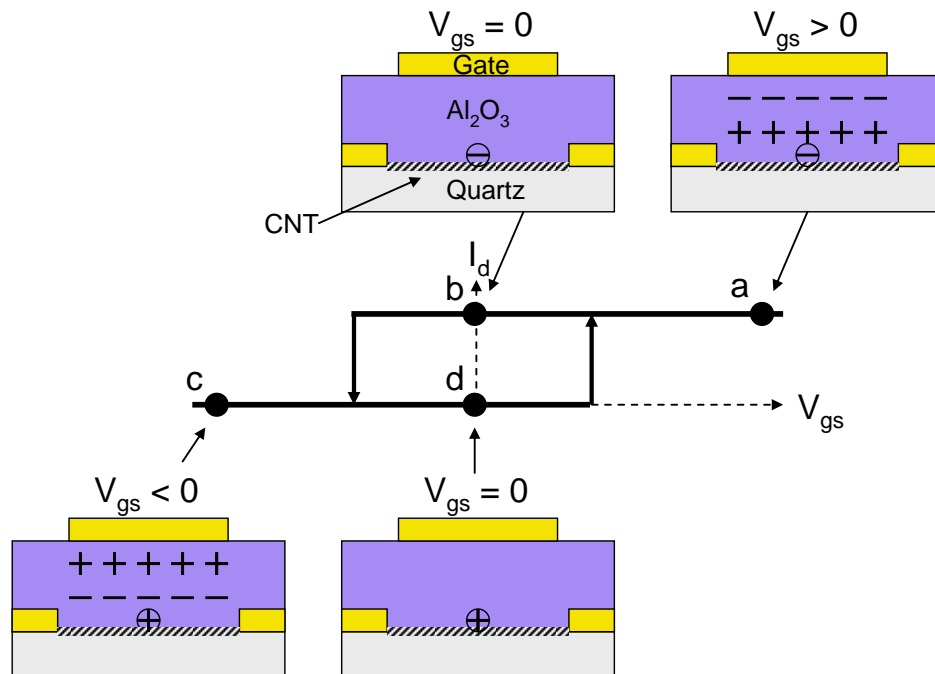
Figure 3.9 Diagrams relating a single trap state in a CNT FET to a hysteron relay in the Preisach model. Four points on the relay are matched with device diagrams showing the dielectric polarization and the trap state occupation.

By filling the α-β parameter space with hysterons and weighting them properly, any hysteresis loop data can be represented. An example of six hysterons representing a filled system is shown in Figure 3.10.
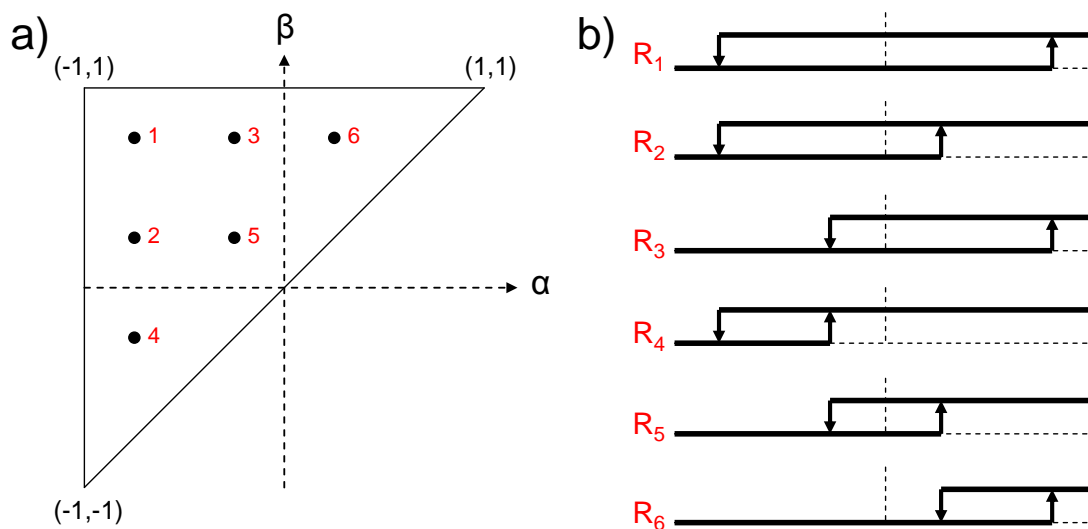
Figure 3.10 Diagrams of a) α-β parameter space with six hysterons and b) the associated relays plotted with equal weights.

A Matlab script was written to execute sweeps of the input variable and see the resulting Preisach output and hysteron states. The script is included in Appendix E. Dividing the α-β plane into 100 vertical and horizontal sections produced 5050 equally spaced hysterons. As the input (x) is swept, the output is the sum of the equally weighted hysterons, computed for each input value. Sweeps from $x = \pm 1$ to 0 by steps of 0.01 are shown in Figure 3.11. The red dot in the x-y plane represents the output at $x = 0$ for the path taken. The α-β plane shows which hysterons are on at the end of the sweep. At x = -1, all the hysterons are off, so when x is swept to 0, most remain off and the output is low. At x = 1, all the hysterons are on, so when x is swept to 0 most remain on and the output is high. Our goal is to achieve a neutral hysteron arrangement, which would correspond to half of the hysterons on and half off. Since these hysterons are equally weighted, that would relate to the center of the x-y plot (0, 0.5).
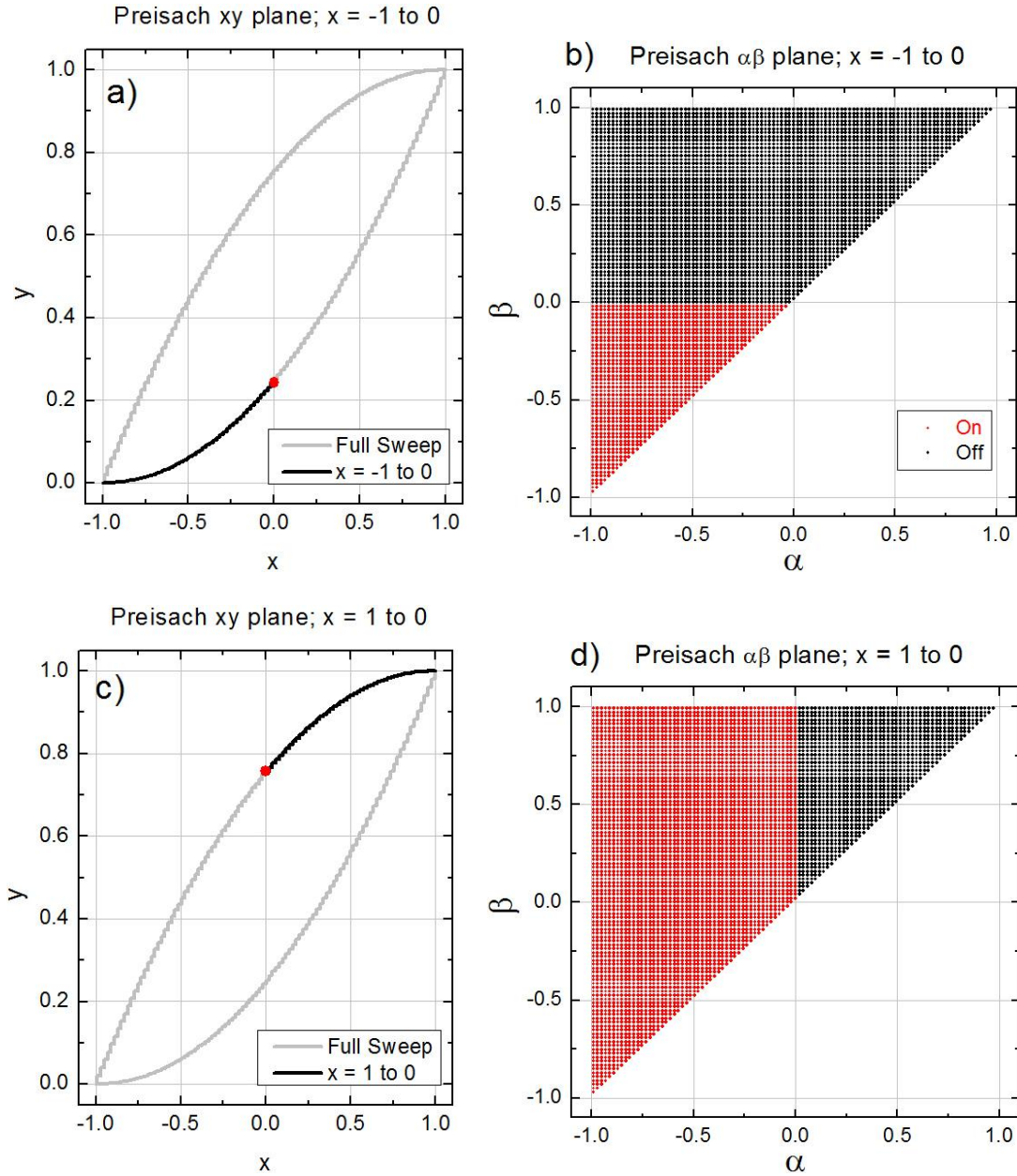
Figure 3.11 Plots of x-y planes from the Preisach hysteresis model using 5050 equally weighted hysterons to sweep from a) $x = -1$ to 0 and c) $x = 1$ to 0. b) and d) are the α-β planes corresponding to $x = 0$ after each sweep. Hysterons that have been switched "on" are shown in red; those in the off state are plotted in black.

In this model, there is no difference in the final output state between sweeping to a value and jumping directly to that value, since each hysteron only depends on x being less than α or greater than β. The final x value will switch all the hysterons that would have been triggered in the sweep up to that final value. Figure 3.11 clearly

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shows that sweeping directly to $x = 0$ from a large x value cannot reach the center of

the plot. Our method is to approach $x = 0$ by alternating between positive and

negative inputs that decrease in magnitude. It is similar to a degaussing a cathode ray

tube to reduce magnetic hysteresis. The particular values used are most easily

understood in the for-next loop labeled EQ 3.7.

For i = 0 to N

$$x = x_{max}\left(1 - \frac{i}{N}\right)$$

$$x = -x_{max}\left(1 - \frac{i}{N}\right) \hspace{4cm} \text{EQ 3.7}$$

Next i

N is the number of divisions as the magnitude of the input approaches zero.

For $N = 4$, the inputs would be $x = 1$, -1, 0.75, -0.75, 0.5, -0.5, 0.25, -0.25, 0, 0.

Preisach output plots for $N = 4$ and $N = 100$ are shown in Figure 3.12. Plot a) shows

the output spiraling in toward the center of the plane. Plot b) shows a nearly even

distribution of hysterons on and off, but more are off than on, so the final output is

less than 0.5. When N is increased to 100 the hysterons appear evenly divided

between off and on, and the final output is 0.5.
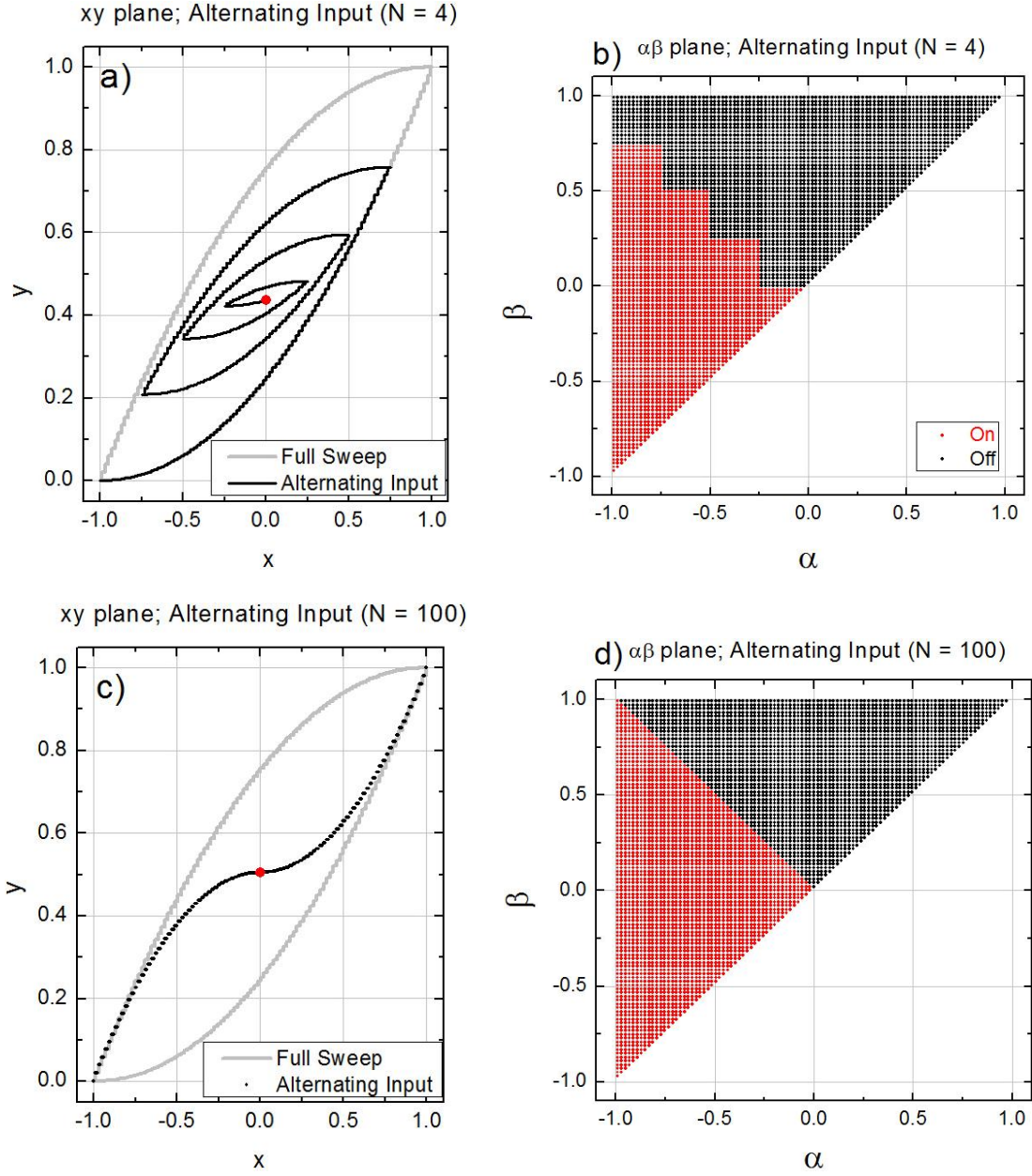
Figure 3.12 Plots of x-y planes from the Preisach hysteresis model using 5050 equally weighted hysterons to perform an alternating input sweep down to $x = 0$ a) for $N = 4$ and c) $N = 100$. b) and d) are the α-β planes corresponding to $x = 0$ after each sweep. Hysterons that have been switched "on" are shown in red; those in the off state are plotted in black.

This simple model indicates that if charge traps behave like input-dependent relays, this alternating input on the gate should bring the current to its equilibrium value, setting a default trap state occupation. In the next section this alternating gate input will be tested on our devices to see if the charge trap effects are reduced.

<u>3.4 Hysteresis Reducing Gate Waveforms</u>

Multiple research groups have published waveforms intended to reduce
hysteresis in transfer curves for CNT FETs.[37, 42, 52-55] Four will be tested in this
section, including the one derived from the Preisach model in the previous section.
They are shown in Figure 3.13 and labeled simply waveform A, B, C, and D. The rest
of the data in this section will correspond to the colors of each waveform.
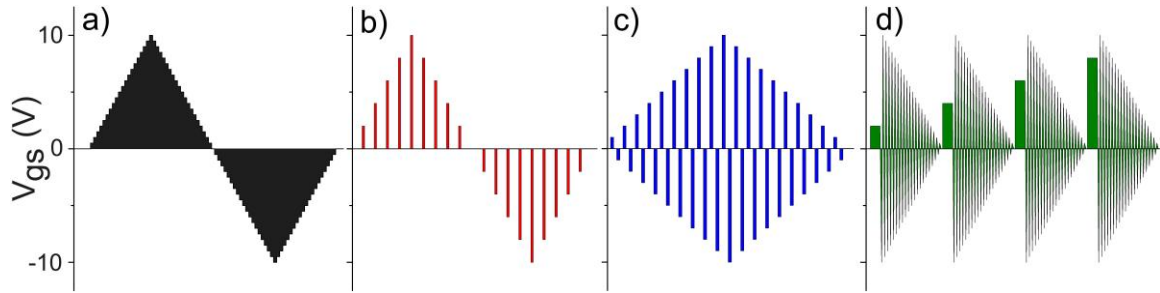
Figure 3.13 Waveforms of gate voltage vs. time used to reduce hysteresis in transfer curves.
a) Waveform A sources each gate voltage sequentially. b) Waveform B returns to ground in
between pulses. c) Waveform C returns to ground in between alternating pulses. d)
Waveform D executes an alternative decreasing waveform in between measurement pulses.

Waveform A is a continuous sweep, the standard transfer curve measurement.
It acts as a control and should produce the most hysteresis. Waveform B comes from
a 2010 publication by Pop.[42] It sources a gate voltage for $T_{on} = 1$ ms before returning
to ground for $T_{off} = 10$ s to allow the trap states to empty. Waveform C comes from a
2010 publication by Mattman.[54] It is very similar to Waveform B except that it
alternates gate polarity between measurements and $T_{off} = 1$ ms. Waveform D is our
method derived from the Preisach model to set a default trap configuration between
measurement pulses. A series of alternating pulses ($N = 100$) that decrease in
magnitude are executed after each measurement pulse to empty the trap states filled
during each measurement pulse.

The same CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm) was measured using all four waveforms. For the pulsed waveforms (B through D) $T_{on} = 1$ ms. Gate voltages were swept between ±10 V by steps of 100 mV. Keithley's Test Script Builder was used to load each sweep waveform into the buffer of a Keithley 2612A sourcemeter which carried out the measurements. The resulting transfer curves are shown in Figure 3.14 and hysteresis width (ΔV_T), hysteresis height (ΔI_d), and measurement duration are listed in Table 3.1.
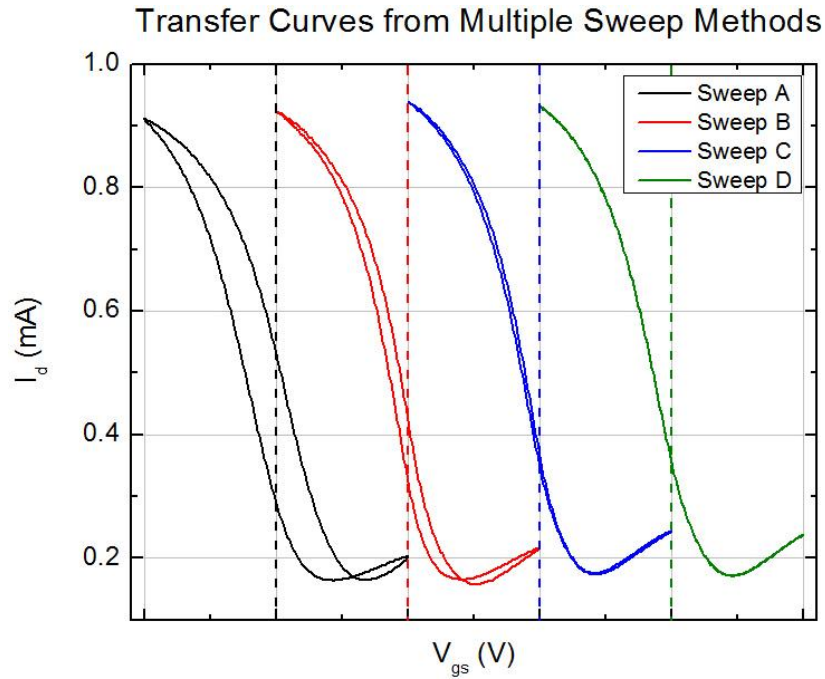
Figure 3.14 Transfer curves of a top-gated aligned CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm). Each curve corresponds to a different measurement sweep. To observe each curve clearly, they are offset by increments on 10 V, with the vertical dashed lines corresponding $V_{gs} = 0$ for each sweep. Each method swept between +-10 V by steps of 100 mV.

Waveform	ΔI_d	ΔV_T	Time
A	265 uA	2.81 V	0.925 s
B	136 uA	0.90 V	4013 s
C	36.3 uA	0.19 V	1.90 s
D	1.8 uA	0.01 V	29.4 s

Table 3.1 Hysteresis data from the transfer curves in Figure 3.15. ΔI_d is the difference in drain current between sweep directions at $V_{gs} = 0$. ΔV_T is the difference in threshold voltage between sweep directions, extracted from the linear extrapolation method at the point of maximum transconductance. Time is the measurement duration.

All three pulsed methods produce transfer curves with reduced hysteresis from the sequential sweep, Waveform A. Waveform B cut the hysteresis width by three but took over an hour to execute. Waveform C was the fastest, completing a full sweep in less than two seconds. Waveform D showed the least amount of hysteresis and took 30 seconds to execute, which is a reasonable time frame to acquire a transfer curve. As discussed in section 3.2, hysteresis is not the only indicator of charge trap behavior. Waveforms B through D all return to $V_{gs} = 0$ in between measurement pulses. The drain current immediately before a measurement pulse should provide an indication of the device trap state. If a waveform successfully sets a default trap state occupation in between measurements, this current value should be independent of V_{gs} *Pulse*. The Presiach model was used to predict the drain current at $V_{gs} = 0$ in between measurement pulses for waveforms B – D. Those results were scaled to match our output current range and are plotted next to the measured data in Figure 3.15.

Since all three methods successfully reduce hysteresis, observing this drain current in between measurements better distinguishes the waveform effects than comparing transfer curves. Considering that the Preisach model does not consider the time dependence of trap states and that all the hysterons were evenly weighted, the correspondence between the model and the measurement is impressive. Waveforms B and C produce drain currents with a strong dependence on V_{gs} *Pulse*, while the drain current in between pulses from Waveform D is close to a single value, independent of V_{gs} *Pulse*. This demonstrates that our proposed method successfully sets a default charge trap occupation in between each pulse measurement.
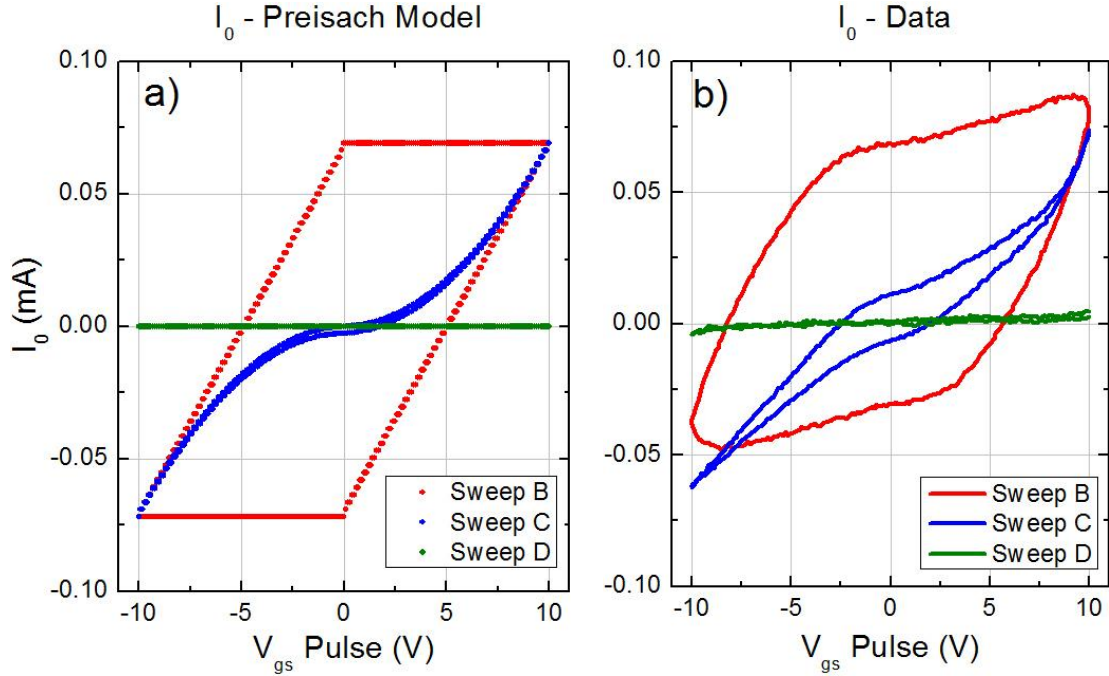
Figure 3.15 Drain current offsets from a) the Preisach model and b) measurements at $V_{gs} = 0$ in between the measurement gate pulses for gate voltage waveforms B, C and D. The predictions used the Preisach model and were scaled to match the measured data.

To evaluate the effectiveness of this measurement waveform, multiple transfer curves were taken of the same device with Waveform D for different values of N. The resulting hysteresis width (ΔV_T) and hysteresis height (ΔI_d) are plotted in Figure 3.16. Surprisingly, even a single alternating pulse on the way to $V_{gs} = 0$ (10 V, -10 V, 0 V) reduced hysteresis more than the other waveforms. The trap state that input would induce is not the equilibrium state, but since it is executed in between each measurement, the dependence on the measurement pulse magnitudes is small.
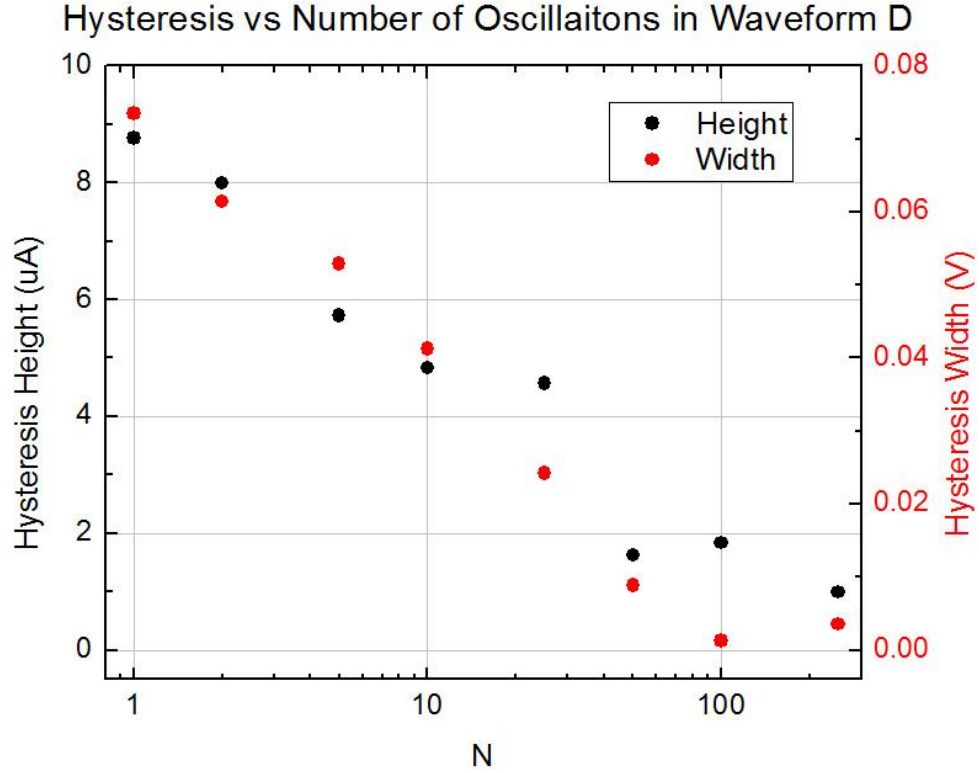
Figure 3.16 Plot of the resulting hysteresis height (ΔV_T) and width (ΔI_d) for transfer curves taken with Waveform D vs. the number of oscillations (N) in the waveform. Eight transfer curves between +-10V at a step of 0.1V were taken of the same device.

3.5 Summary

In this chapter we have introduced the phenomenon of defects in dielectric material that act as traps for free charges. The effects of these charge traps are visible as hysteresis in transfer curves. By sourcing pulses on the gate electrode of our CNT FETs and observing how the drain current responds over time, we find that the initial drain current offset (the distance the drain current is from its equilibrium value 1 ms after a gate pulse) is linearly dependent on the pulsed gate voltage and has a logarithmic dependence on pulse duration. This information was used to devise a measurement scheme that would minimize the effects of trapped charges.

By using short pulses on the gate, charges have less time to become trapped by defects, and therefore the number of charges trapped will be minimized when the gate voltage is changed. The strong linear dependence of the offset current on the gate voltage allows us to use a gate voltage waveform to force a default charge trap occupation in between measurements, eliminating the production of hysteresis in transfer curves. The time-independent Preisach model is used to derive this waveform, which consists of alternating polarities as the voltage magnitude collapses, similar to the method used to degauss a cathode ray tube. Transfer curves of encapsulated CNT FETs were taken with this gate voltage waveform and with other published gate voltage waveforms intended to reduce hysteresis in transfer curves. Our Preisach-derived gate voltage waveform demonstrated the greatest reduction in hysteresis, with the hysteresis width and height reduced to the level of measurement noise. With a source-meter capable of 1 ms pulses, a typical transfer curve can be taken in less than one minute by using this method.

Chapter 4: Removal of Metallic CNTs from Mixed Arrays: Burning

In this chapter we discuss the role of the on/off current ratio in carbon nanotube (CNT) field-effect transistors (FETs). The CNTs arrays produced by chemical vapor deposition (CVD) contain a mixture of metallic and semiconducting CNTs, which produce an as-grown on/off ratio near 3. Some applications require a larger on/off ratio to properly function, so the on/off ratio is increased in CNT devices on SiO_2 by using the standard technique of selective electrical breakdown from Joule heating, referred to as burning. Improvements are made to the method to preserve more on-state drain current after burning.

The standard method of burning cannot be directly applied to CNTs on high frequency substrates, like quartz, because they lack a conductive backplane to be used as a gate. A method is devised and employed to adapt the standard burning procedure to devices on quartz. That process is further adapted to simultaneously burn many CNT channels in parallel. The presence of metallic CNTs in FETs used for high frequency applications produces a DC current offset when biased. If CNTs are ever to be used in RF handheld electronics, power consumption will be a concern, so increasing the on/off ratio of as-grown CNT arrays on HF-compatible substrates is a necessary step toward that goal.

4.1 On/Off Current Ratio

As mentioned in Chapter 1, carbon nanotubes' (CNTs) structure exhibits a variety of chiralities which give rise to both metallic and semiconducting properties.

The three most common techniques for synthesizing CNTs (arc discharge[1], laser ablation[13], and chemical vapor deposition[14, 15, 56-59]) each produce a mixture of both types of tubes which typically contain twice as many semiconducting tubes as metallic tubes.[60] However, not all chiralities will be equally likely to grow in all circumstances. The CNT diameter is related to the catalyst particle size and the growth temperature and pressure[24, 61-64]; therefore the ratio of semiconductor to metallic tubes can be somewhat variable.

The presence of metallic CNTs is non-ideal in most semiconductor applications. One of the most significant problems is the inability of a CNT device containing metallic tubes to be gated off. When a positive gate voltage is applied to a p-type CNT FET, the associated electric field depletes the semiconducting CNTs of charge carriers but leaves the metallic CNTs unaffected. Therefore the presence of metallic tubes limits the degree to which a CNT FET can be turned off. For a given source-drain voltage, the ratio of the on-state current to the off-state current is referred to as the on/off ratio and is a key metric for the FETs.

Experiments have shown that typical CNT FETs fabricated from CVD grown nanotubes will have an on/off ratio of around 3. One simple explanation for this is that the on/off ratio is directly related to the ratio of semiconducting to metallic CNTs. When a device is gated on, the total current is due to both N metallic CNTs and 2N semiconducting CNTs; thus 3N total CNTs contribute to the on-state current. When the device is gated off, only the N metallic CNTs should be conducting, so the on/off ratio should be close to $3N/N = 3$. The on/off ratios of our as-grown CNT FETs range from 1.5 to 10.

Whether or not an on/off ratio near 3 is acceptable depends on the application. Many DC circuits require an on/off ratio of 1000 or greater to function properly. For high frequency (HF) purposes, a low on/off ratio merely gives rise to a DC offset when the channel is biased. With regard to power consumption and/or heat dissipation, the presence of a constant channel current could be detrimental. Therefore, the performance of both DC and AC circuits benefit from improved on/off ratios. Increasing the on/off ratio requires the selective removal of the metallic CNTs. This is typically accomplished by joule heating in air, leading to electrical breakdown, and is commonly referred to as burning.

4.2.1 Standard Burning Procedure on SiO$_2$

The standard method for burning metallic CNTs was first published in 2001.[65] It is typically performed on thermally oxidized silicon wafers (Si/SiO$_2$) substrate with CNT contact electrodes in place. The conductive silicon wafer provides a global back gate to turn off semiconducting tubes while a voltage is held between the CNT contact electrodes. As the voltage between the CNT contact electrodes is increased, the amount of current and power dissipated in each CNT increases, causing significant self-heating. Once the CNT temperature reaches approximately 600 °C in air, it will oxidize and physically break at the point of maximum temperature, usually in the middle of the CNT.[66] Though current will be flowing through all the CNTs bridging the channel, by using the back gate to increase the resistance of the

semiconducting CNTs, the metallic CNTs should pass more current and therefore heat up and burn before the semiconducting CNTs.

This method is straightforward when dealing with single CNT channels or aligned arrays where each CNT spans the channel, but is more difficult to execute on CNT random networks where some metallic CNTs may be necessary for channel conduction. Each tube-to-tube crossing can provide a defect where local heating may destroy a CNT prematurely.[67] An analysis of the on/off ratio dependence on CNT density, channel width, and channel length for random network CNT FETs was performed by a group member, Vinod Sangwan, and is detailed in his publications.[27,68] To avoid the complications associated with random networks, aligned arrays of CNTs were transferred from quartz to SiO_2/Si for devices. Without CNT crossings, each CNT could be thought of as independent, so the burning process can theoretically be carried to completion resulting in the removal of all the metallic CNTs connecting the channel.

Field-effect transistors on SiO_2/Si substrates utilizing aligned arrays of CNTs were prepared following the procedure described in detail in Appendix A. Briefly, aligned CNTs were grown on a quartz substrate via CVD, covered with a 100 nm layer of gold in an e-beam evaporator and then covered with a layer of thermal tape. The gold-covered CNTs were peeled off of the quartz growth substrate and transferred to a SiO_2/Si substrate with the thermal tape. The SiO_2/Si sample was then heated on a hot plate above 120 °C to melt the tape adhesive and remove the tape, leaving behind the gold/CNT layer on the SiO_2 surface. The gold layer is then etched away with a potassium chloride chemical etchant. With the aligned arrays of CNTs

now on an SiO_2/Si substrate, 50 nm gold (with a 5 nm titanium adhesion layer)

contact electrodes were fabricated using standard photolithography, e-beam

deposition and lift-off. CNTs not in the channel region or covered by the electrodes

were removed using standard photolithography followed by O_2 plasma etching (100

Watts, 16 SCCM and 200 mTorr for 10 sec) and photoresist removal in acetone. The

resulting structures, shown in Figure 4.1, can also be used as FET devices, with the

silicon substrate acting as the gate.
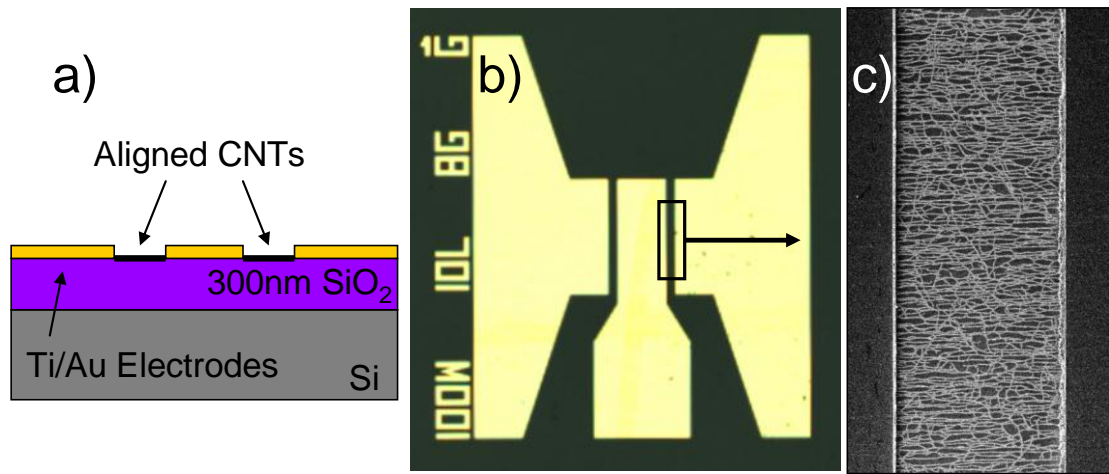
Figure 4.1 a) Diagram of FET geometry on Si/SiO2 with aligned CNTs in the device channel. b) Optical image of device geometry and c) SEM image of aligned CNTs in one channel.

Before burning, standard IV curves were taken. The removal of the metallic

CNTs was accomplished by setting a constant gate voltage of 40 V using the silicon

substrate as a global back gate. Then the source-drain bias was swept from 0 to 35 V

and back to 0 V as a rate of 1 volt per second. Standard IV curves were then

measured again. The on/off ratio was calculated with a source-drain bias of -2 V, with

V_{gs} = -10 V and +10 V for the on and off states, respectively. To increase the on/off

ratio, the burning process was repeated with a higher maximum bias of 40 V for a

second sweep and 45 V for a third sweep.

An example of the I_d vs. V_{ds} measurements associated with this burning process is show in Figure 4.2. The drain current is plotted against the source-drain voltage measured during three sequential voltage sweeps of burning a device with a channel length of 10 μm and a channel width of 500 μm. The noise in the curves at high source-drain voltages correspond to individual CNTs breaking.
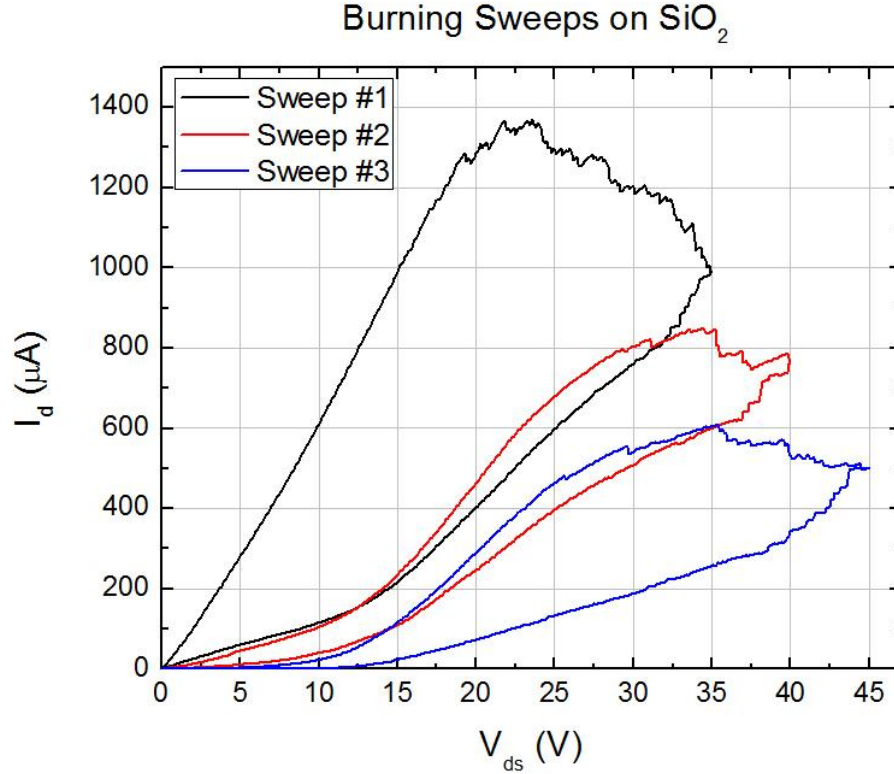
Figure 4.2 Drain current vs. source-drain voltage plot of three burning sweeps of a CNT channel in SiO_2. The gate voltage used during burning was +40V. The device had a channel width of 250 μm, a channel length of 10 μm, and used the silicon global backgate.

Analysis of CNT breakdowns from multiple publications have shown an approximate breakdown voltage dependence on channel length of ~ 5 V/μm.[66, 69] With a 10 μm long channel, one would expect all the CNTs to experience electrical breakdown around 50 V source-drain bias. We observe initial breakdown occurring below half that bias. Output and transfer curves for both CNT FETs containing as-grown and burned CNT are shown in Figure 4.3.
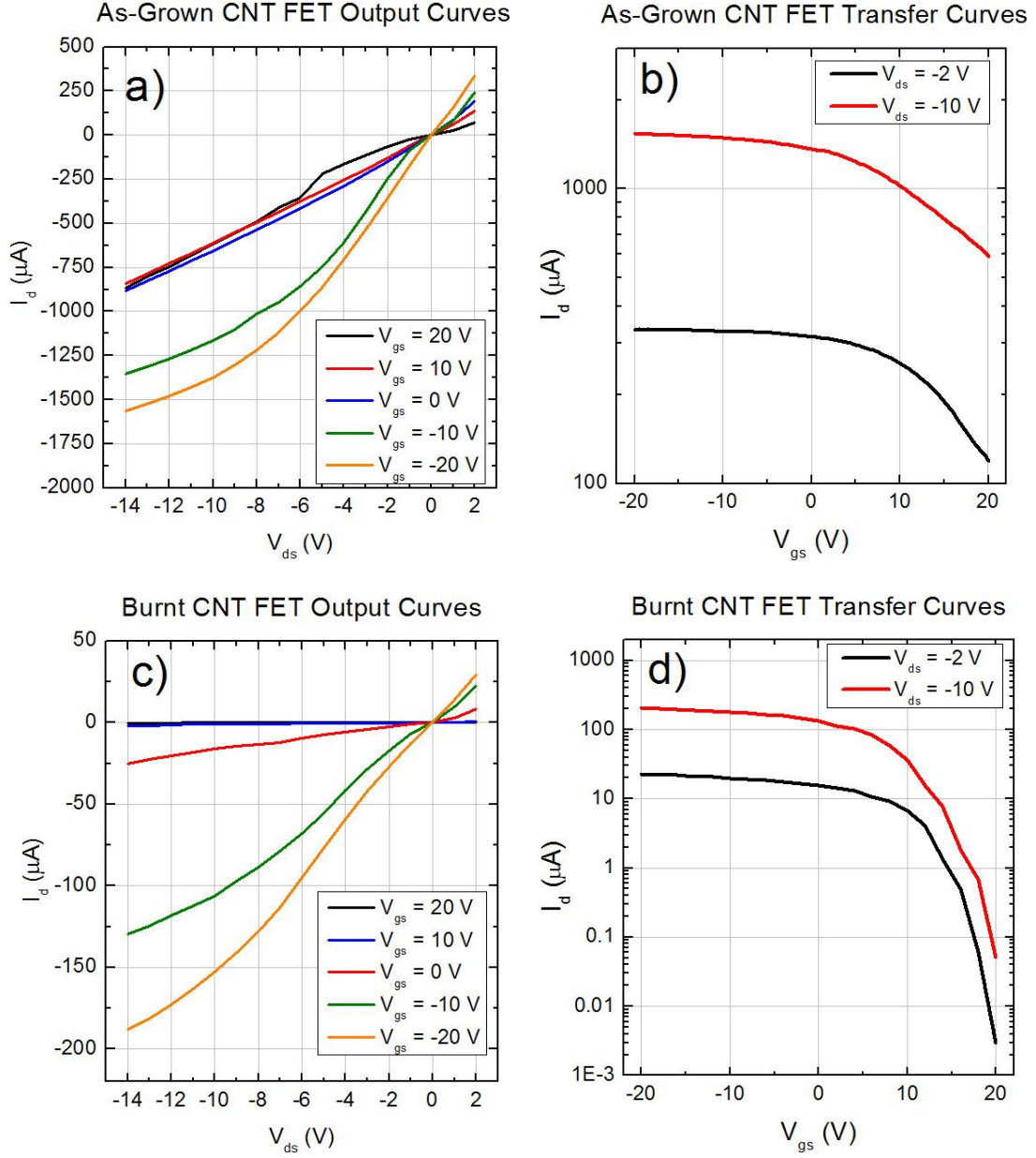
Figure 4.3 IV curves of a CNT FET on SiO_2. a) and b) correspond to the as-grown device, and c) and d) were taken after a burning procedure was executed. The device had a channel width of 250 μm, a channel length of 10 μm, and used the silicon global backgate. The transfer curves are plotted with drain current on a log scale.

A comparison of the transfer curves indicate that the on/off ratio has been increased by approximately three orders of magnitude. After burning, however, the on-state current has been reduced to 6 to 11% of the original on-state current measured for the as-grown CNT FET before burning, depending on source-drain bias.

This is much lower than the 1/3 reduction that would be expected from removing the metallic CNTs only and leaving all the semiconducting CNTs intact. This implies that either a large number of semiconducting CNTs have been destroyed along with the removal of the metallic tubes as a result of this burning process, or the metallic nanotubes carry higher current on average.

Experiments on highly dense aligned arrays of CNTs have demonstrated that a single CNT electrical breakdown can trigger breakdowns in adjacent CNTs that cascade across an entire channel.[67, 70] This suggests that semiconducting tubes less than a critical distance from a metallic CNT will also be destroyed during burning. It has been shown that a transition from destroying single CNTs to a correlated breakdown of neighboring CNTs occurs in the density range of 1-30 CNTs per μm of channel width. Since the aligned arrays of CNTs used in these measurements are in the density range of 1-3 CNTs/μm, it can be expected that some of the semiconducting CNTs will be damaged by this process. As a result, there is a trade-off between on/off ratio and on-state current magnitude. To preserve current, the burning process can be stopped once an adequate on/off ratio has been reached.

To establish some statistics for the relationship between improved on/off ratio and the reduction in on-state current, 36 separate CNT FETs with channel lengths of 10 μm and channel widths of 200, 500, and 1000 μm were fabricated on a single chip and measured before burning, after one burning cycle, and after multiple burning cycles. A plot of the normalized on-state current (normalized to the as-grown on-state current) vs. on/off ratio for these devices is shown in Figure 4.4.
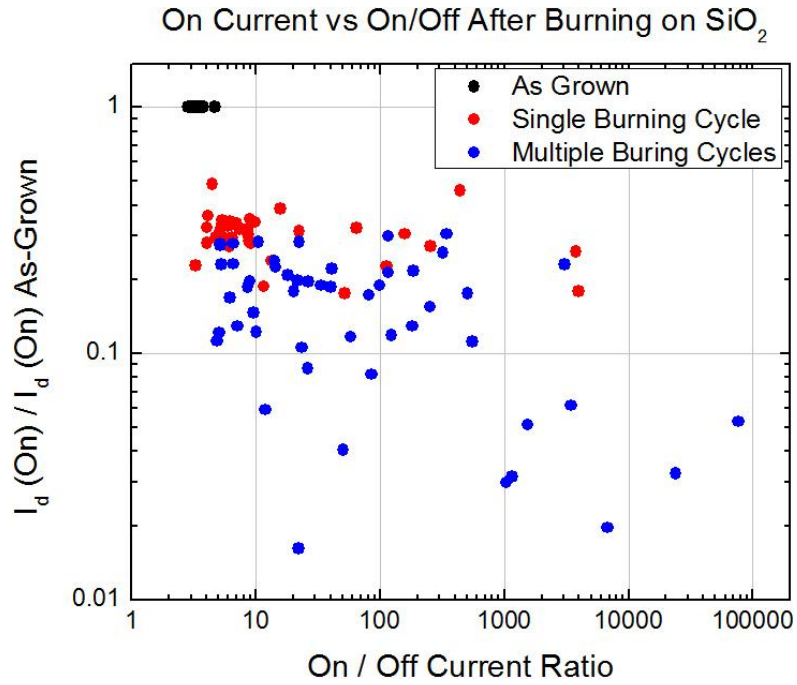
Figure 4.4 Plot of normalized on-state drain current vs. on/off ratio for 36 different CNT FETs on SiO_2 at multiple stages of burning.

Regardless of the number of burning cycles, a large variation in both on-state current and on/off ratio is evident. The results range from on-state current reduction of 74% with an on/off ratio $> 10^3$ to an on-state current reduction of 94% with an on/off ratio near 10. Order of magnitude on-state current losses have been reported elsewhere.[71] It is clear from these results that better burning methods are needed if high performance CNT FETs with burned channels are to be routinely fabricated. The next section of this chapter will introduce and develop concepts of pulsed burning methods as a way of preserving more on-state current and achieving more consistent final devices.

4.2.2 Pulsed Burning on SiO$_2$

One cause of the large distribution in results shown in Figure 4.3 may involve

charge trapping. As discussed in Chapter 3, the field reaching each CNT is a

complicated combination of the source-drain bias, gate-source bias, adjacent CNTs,

and charge traps in the dielectric or on the surface from water molecules. By holding

the gate at a constant 40 V for an extended time period, charges are drawn into traps

and diminish the effect of gating. To reduce this effect, the burning procedure is

adjusted to only source the gate voltage shortly before the burning source-drain bias

is applied.

A plot of a voltage waveform used for employing pulses instead of fixed

voltages during burning is shown in Figure 4.4. Initially, both the gate and source-

drain are grounded. The gate bias is then increased to a large positive voltage (20 V)

to gate off the semiconducting CNTs 100 ms before the source-drain voltage is

sourced for 100 ms to burn out the metallic CNTs. Then both voltages are returned to

ground. An on/off measurement is taken at V_{ds} = 1 V with V_{gs} = -10 V and +10 V for

the on and off states, respectively. The process is then repeated with a higher pulsed

source-drain bias. Only one period is shown in Figure 4.5.
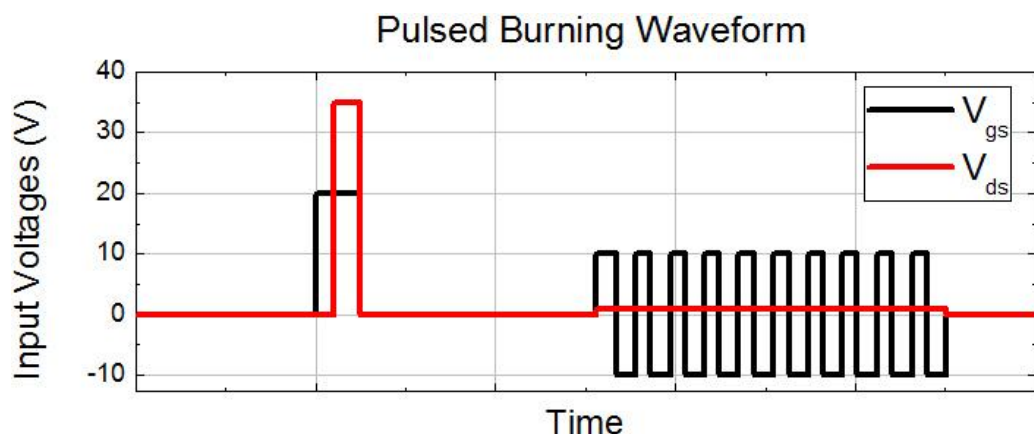
Figure 4.5 Gate voltage and source-drain voltage waveforms used to perform pulsed burning, then perform an on/off ratio measurement of CNT FETs.

The results of one CNT FET burned with the pulsed gate voltage method are plotted in Figure 4.6 with the previous data from Figure 4.3 of the 36 devices burned with a constant gate voltage. The one device that underwent pulsed burning does not demonstrate any statistics, but it shows the approximate on-state current vs. on/off ratio path that devices typically exhibit when burned in this way. Though some devices from the previous method did produce on/off ratios and on-current magnitudes higher than this sample using pulsed burning, on average this method preserves more current. Other research groups have published similar pulse-style burning procedures with shorter time scales and showed improvements over fixed gate voltages and source-drain sweeps as well.[72]
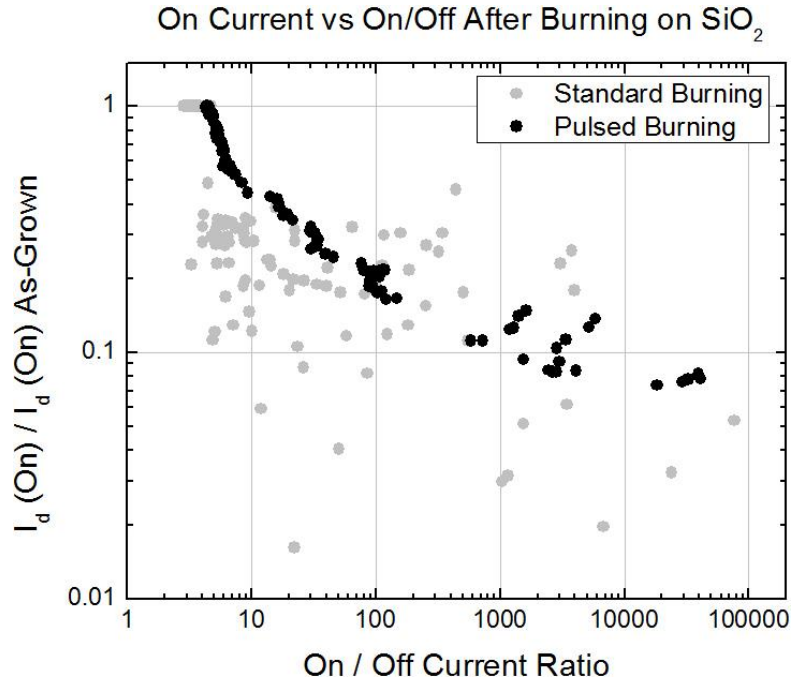
Figure 4.6 Plot of normalized on-state drain current vs. on/off ratio for a CNT FET on SiO_2 that underwent pulsed burning (black) for 36 CNT FETs on SiO_2 at multiple stages of burning (gray).

4.3 Burning on Quartz

Aligned CNTs grown on quartz can be transferred to SiO_2/Si substrates for burning, as was done for the devices in the previous section. Once burned, encapsulating dielectrics and local top-gates can be added to gate each FET separately. However, for AC applications the conductive silicon substrate will add parasitic capacitance. To enable proper high frequency operation, an insulating substrate like quartz must be used. Transferring CNTs from SiO_2 back to quartz after burning would subject them to the additional processing of etching away the CNT contact electrodes, covering them in a transfer material like gold, transferring that layer to a new substrate, etching away the transfer material, and re-depositing contact

electrodes and an encapsulating dielectric. Additionally, a very difficult degree of alignment would be needed to re-use burned channels, which our thermal tape transfer method cannot accommodate. During the burning process, metallic CNTs are broken, not completely destroyed, so a slight offset in redefining new contact electrodes could produce channels with previously broken metallic CNTs now bridging the new channel. It would be more efficient to burn away metallic CNTs on the growth quartz substrate.

Since a quartz substrate does not contain a back gate for burning, another way of controlling the electric field in the channel is necessary. Burning after encapsulation is impractical since the breakdown temperatures for encapsulated CNTs have been found to be higher than 600 °C.[73-75] Also, without air to provide oxygen and dissipate heat, the breakdown of CNTs can damage electrodes. The method that we employed to burn on quartz before encapsulation was to bring a separate SiO_2/Si piece to rest on top of the CNT contact electrodes to act as a temporary global top-gate. The contact electrodes were made thicker than previously (100 nm) to provide an air gap. With the added air gap, the field reaching the CNTs will be weaker than it would be from a native global back gate, so the gate voltage used for burning was increased. The surfaces of the quartz sample and the SiO_2/Si sample were carefully cleaned with acetone, methanol, and isopropyl alcohol and then blown dry with nitrogen. The cleaner the two surfaces, the better the contact will be, producing a more effective gate field. The SiO_2/Si sample was held in place by a DC probe. Proper conduction was assured by scratching the back of the silicon piece

with a diamond scribe and adding silver paint. A diagram of this procedure is shown

in Figure 4.7
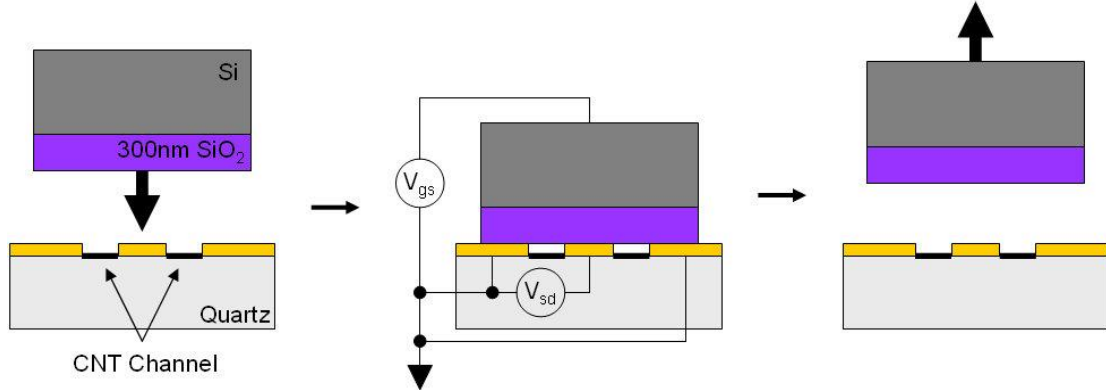
Figure 4.7 Diagram of the external Si/SiO$_2$ top-gate burning method on a quartz CNT FET before dielectric encapsulation.

To access the CNT source-drain electrodes with probes while the SiO$_2$/Si

external top-gate was in place, the contact electrodes were lithographically extended

several millimeters away from the center of the sample. In addition to extending the

contact electrodes, several devices shared the extended contact electrodes to enable

burning multiple devices at once, as shown in Figure 4.7. With these electrodes in

place, the combination of several devices connected in parallel resemble one device

with multiple channels. The number of devices able to be burned simultaneously is

limited by the magnitude of the collective drain currents associated with so many

CNTs in parallel under the source-drain biases necessary to achieve burning. The

largest number of CNT FETs we have burned in parallel is 15, which produced a

drain current greater than 60 mA during burning. The IV curves for 15 CNT FETs on

quartz measured in parallel before and after employing the external top-gate burning

method are shown in Figure 4.9. Before burning, the on-state current at V_{ds} = 1 V was

9.3 mA, and the on/off ratio for V_{gs} = ± 100 V was 1.3. After burning, the on-state

current at V_{ds} = 1 V is 100 µA (~ 1% of the as-grown current) and the on/off ratio for

$V_{gs} = \pm 100$ V is 52. These on/off ratios are measured using the external top-gate. The on/off ratios of the completed devices should improve with a local top-gate as shown below.
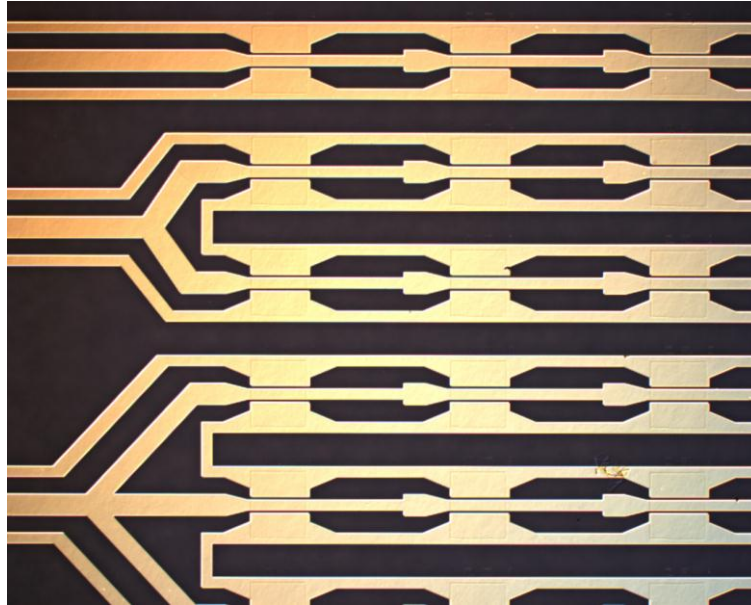
Figure 4.8 Optical image of joined and extended CNT contact electrodes on quartz. These electrodes link together up to 15 FET channels so that they may be burned simultaneously.
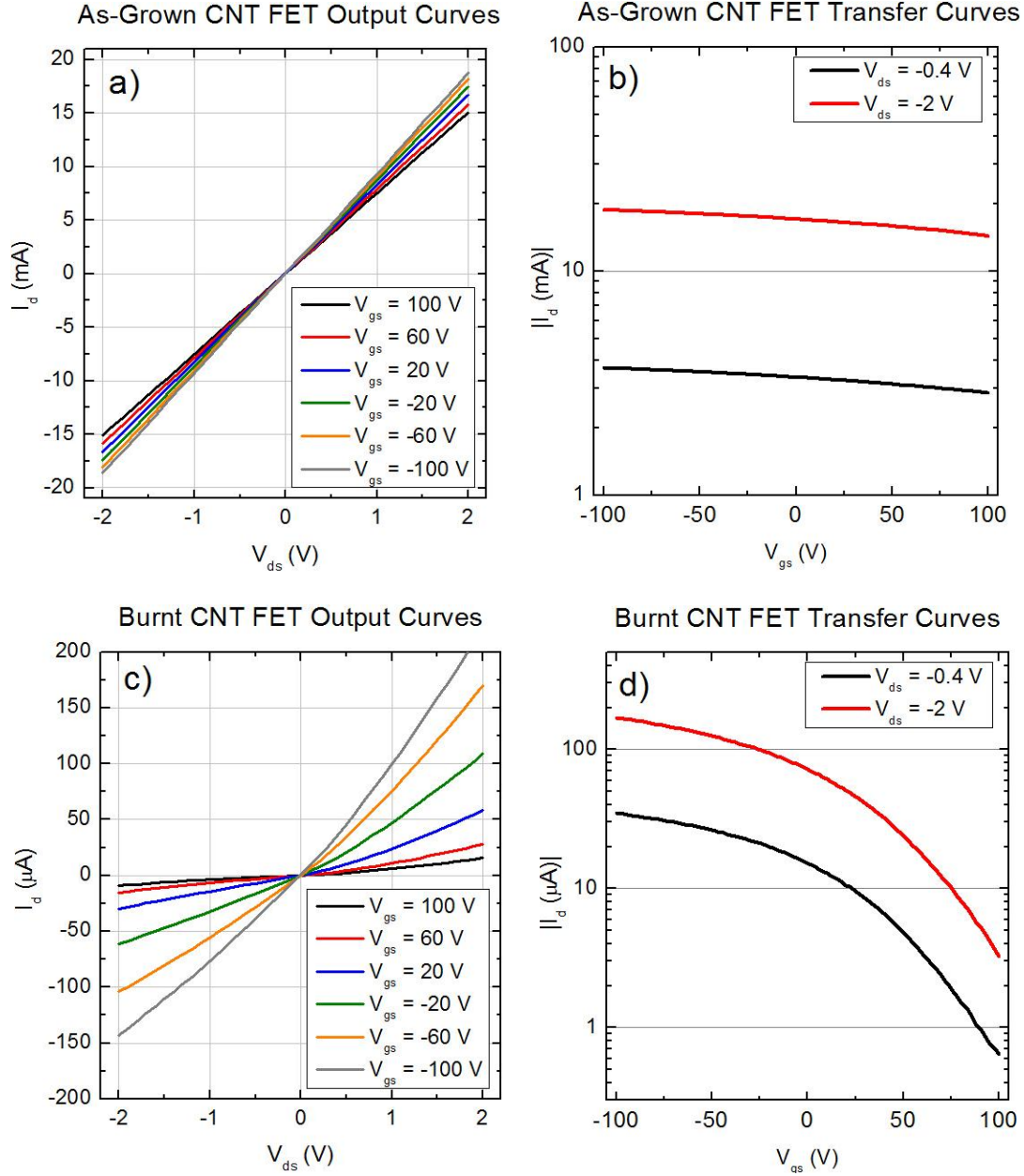
Figure 4.9 a), c) Output and b), d) transfer curves for 16 CNT FETs measured in parallel on quartz using an external Si/SiO$_2$ piece as a top-gate measured a), b) before and c), d) after burning.

These plots show a reduction in the on-state current to near 10% of the original as-grown CNTs, which is similar to the reduction observed with devices on SiO$_2$. After burning is complete, the electrodes connecting the FETs are lithographically removed. First, a lithographic pattern is defined that is open where

the electrodes are to be etched away. Then a potassium iodide gold etchant is used to

remove the 100 nm gold top electrode layer, and after that a fluoroform plasma

(40mTorr, 175W, 18sccm CHF_3, 2sccm O_2) is used for one minute to etch away the

remaining 5 nm titanium adhesion layer. After the source-drain electrodes are

isolated, a 150 nm Al_2O_3 dielectric layer and 100 nm gold (with a 5 nm titanium

adhesion layer) local top-gate are added. Optical images of a sample showing

connected devices with a) photoresist in place before etching, b) separated electrodes

after etching, and c) completed devices are shown in Figure 4.10.
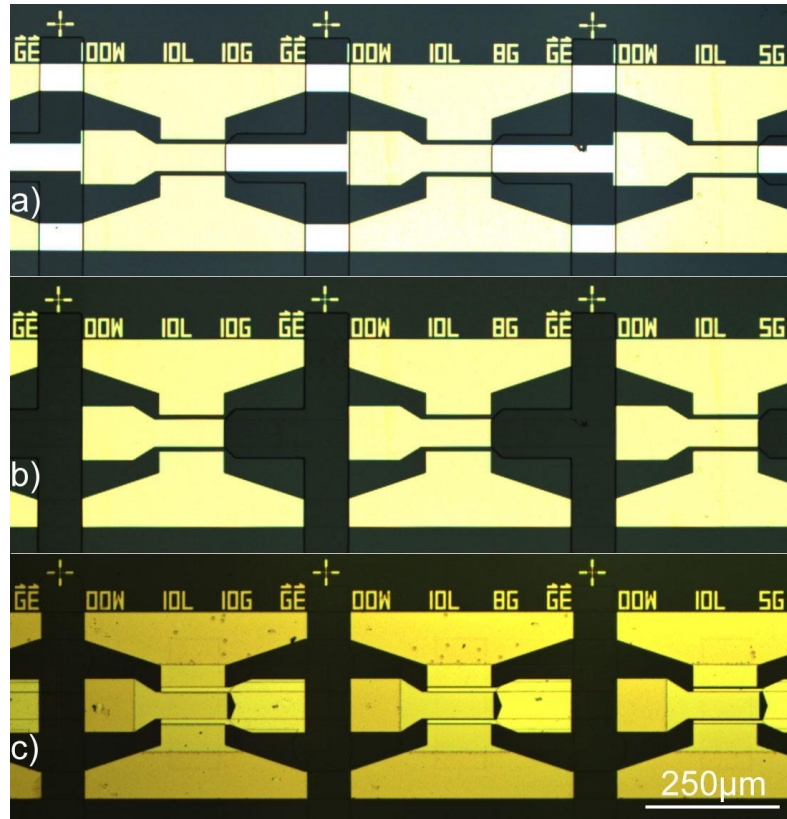
Figure 4.10 Optical images of the lithographic steps of isolating and completing CNT FETs on quartz after electrical breakdown. a) Patterned CNTs and source-drain electrodes are in place with the connections between FETs uncovered by photoresist. b) The electrodes previously connecting devices have been removed. c) Patterned ALD alumina layers and local top-gates were added to complete each device.

Output and transfer curves are shown in Figure 4.11 for one of the 15 devices. A local gate functions much more efficiently than the external silicon top-gate with an air gap, so the resulting device on/off ratio is greater than 10^5. All of the devices burned in parallel demonstrated on/off ratios above 10^3 after they were completed with local top-gates. Ambipolarity at large positive gate voltages is visible, as is typical of encapsulated CNT FETs. These results demonstrate the effectiveness of this external top-gate burning method on quartz.
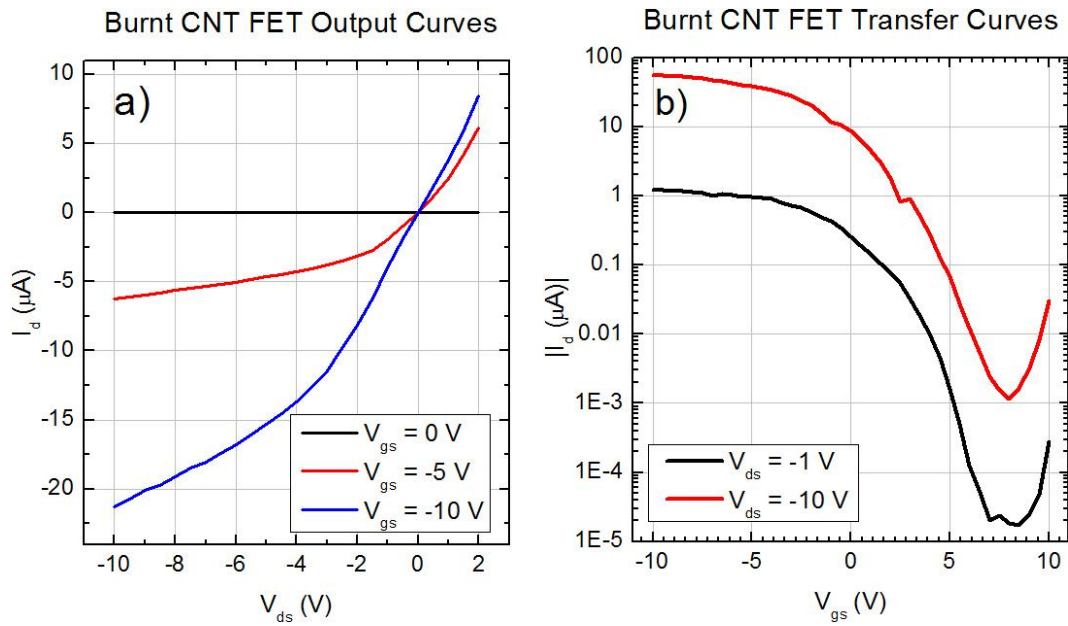
Figure 4.11 a) Output and b) transfer curves for a CNT FET on quartz encapsulated in Al_2O_3 with a local top-gate after external top-gate burning was executed and devices were separated.

4.4 Summary

CVD growth of CNTs produces a mixture of semiconducting and metallic tubes. The presence of metallic CNTs prevent a CNT FET from being effectively turned off, providing a constant drain current when biased that is undesirable for

applications that require low power operation. The standard method of removing metallic CNTs is typically performed on a Si/SiO$_2$ substrate, utilizing the silicon as a global back gate to turn off semiconducting tubes while a voltage is held between the CNT contact electrodes.

Burning experiments on SiO$_2$ produce a large variation of resulting on/off ratios among samples due to the effect of adjacent CNTs, contact resistance, defects, and variations in breakdown temperature due to chirality. To reduce the effects of trapped charges due to defects, the standard burning procedure was adjusted to use pulses instead of constant biases, which resulted in preserving more on-state current.

To remove the metallic CNTs from aligned arrays on quartz substrates, a method was developed to use an external Si/SiO$_2$ substrate to rest on top of the source-drain electrodes and act as a temporary global top-gate. Additionally, several devices were connected in parallel to allow burning up to 15 channels at once. This method was shown to be successful, consistently increasing the on/off current ratio of the CNTs from around 3 to greater than 10^3. If active CVD-grown CNT devices are to be used for high frequency applications where power consumption is important, this is a necessary step toward that goal.

Chapter 5: HF CNT Measurement Techniques and Limitations

Many research groups have investigated the high frequency (HF) properties of carbon nanotubes. The standard figures of merit for high frequency devices are cutoff frequencies, which correspond either to frequencies where operation ceases (hard cutoffs) or frequencies where the output signal attenuation becomes significant. At frequencies above attenuation cutoffs, a device may continue to operate, but the magnitude of the output signal decreases with frequency, eventually reaching a level where it cannot be detected.

In this chapter, the published HF results from other research groups will be presented along with the expected cutoff frequencies from their measurements. If these cutoffs were applied to our devices, significant attenuation would occur at GHz input frequencies, and device operation would cease near 13 GHz. Our measurements are performed in a way that overcomes these cutoff frequencies and demonstrates continued device operation up to input frequencies of 40 GHz. By using a spectrum analyzer with a low noise floor (near 90 dBm), high frequency output signals are detectable in spite of attenuation. Also, by using an external mixer in combination with the spectrum analyzer, output frequencies can be measured up to 110 GHz, higher than any other directly observed output frequencies from CNT devices to date.

5.1 Active Devices: Current Gain Cutoff Frequency

The most commonly used figure of merit for an active device is the current gain cutoff. It is the frequency at which the current gain drops below 1 (0 dB). Since our mixing was performed passively, our devices cannot operate at gain, so this cutoff does not apply to our experiments. It is discussed here because it has received the most attention in recent publications.

To measure the current gain cutoff frequency, a source-drain and gate bias is applied to the device as it would be when integrated into a circuit. The most common method of extracting this frequency is with a vector network analyzer (VNA). VNAs can be used to extract the parameter H_{21}, which is a hybrid parameter equal to output current over input current. The input and output currents are compared at the same frequency, so $F_{in} = F_{out}$. When $|H_{21}|$ is plotted vs. frequency, the point at which it crosses 0 dB is the current gain cutoff frequency. When extracted this way, this frequency is sometimes called the extrinsic current gain cutoff frequency because it corresponds to the current gain of the whole device.

Non-ideal device properties, such as parasitic capacitances from electrodes, can lower this cutoff from its possible intrinsic value. The intrinsic current gain cutoff frequency can be extracted by subtracting the parasitics from H_{21} by using measurements from control devices, a process called de-embedding. In the event that the de-embedded |H21| plot does not cross 0 dB in the frequency regime of the VNA, it can be projected to follow a slope of -20 dB per decade. This method was used to extract an intrinsic current gain cutoff frequency of 100 GHz for a graphene FET[76] in 2010, even though the VNA used was limited to 25 GHz.

Another way to extract the intrinsic current gain cutoff frequency is with the equation 5.1.

$$F_{T\,int} = \frac{g_m}{2\pi C_{GS}}$$ EQ 5.1

Using the largest measured transconductance of CNTs (20 μS) measured in 2004 and an ideal geometrical capacitance (44 aF/μm), this intrinsic cutoff was calculated by Burke to scale with channel length as:

$$F_{T\,int} = \frac{80GHz}{L_{gate}(\mu m)}\,[16]$$ EQ 5.2

Like the de-embedding VNA process, this equation ignores device parasitics. The largest extrinsic current gain cutoff frequency for a CNT device published so far is 15 GHz.[77] That particular device used hundreds of CNTs and had a channel length of 300 nm. Its intrinsic current gain cutoff frequency extracted from the VNA de-embedding procedure was 80 GHz. Some selected published current gain cutoff frequencies are plotted vs. publication year in Figure 5.1.

Current Gain Cutoff Frequency

76-82
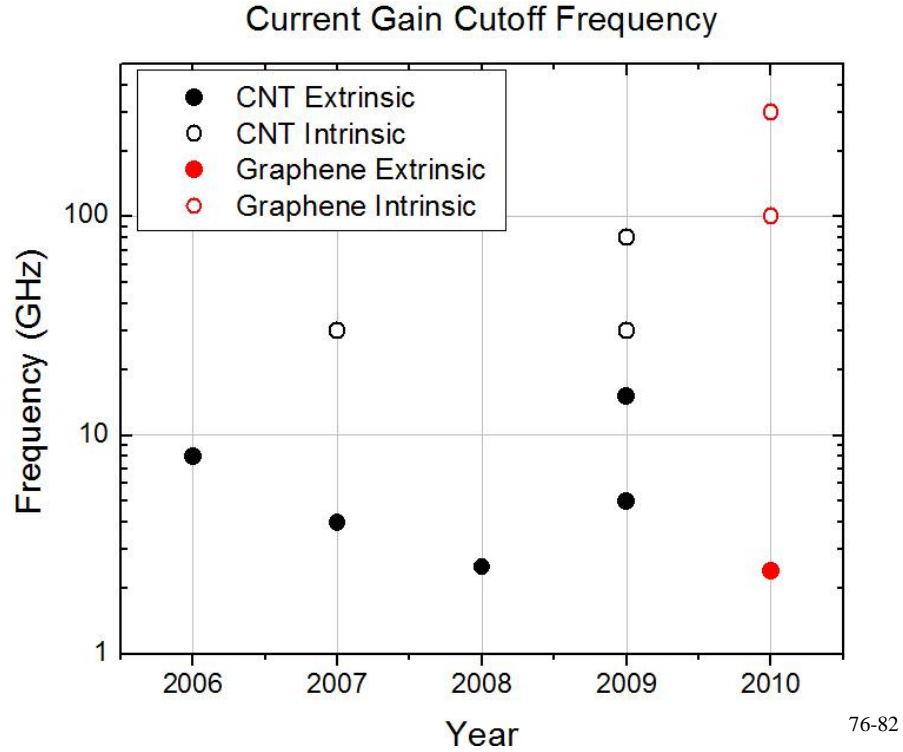
Figure 5.1 Plot of published current gain cutoff frequencies on a log scale for CNT and graphene devices with sub-micron channel lengths vs. the year of publication.

By using EQ 5.1 for our standard 10 um channel length device, with the transconductance extracted from IV curves (120 μS at V_{ds} = 5V) and the measured gate-source capacitance (30 fF), gives F_{Tint} = 640 MHz, demonstrating that if used actively, our devices would not be expected to perform as well as most recently published devices. All the devices referenced in Figure 5.1 had sub-micron channel lengths.

<u>5.2 Direct Observation of HF CNT Nonlinear Behavior in Literature</u>

Another way to evaluate the high frequency performance of carbon nanotube

devices is to use their nonlinear properties to convert input frequencies to different

output frequencies, typically called mixing. Mixing will be described in detail in the

next chapter. Direct observation of high frequency nonlinear responses in CNT

devices has ranged from 250 MHz[83] to ~100 GHz[84] over the past few years. The

results of five such publications are summarized in Table 5.1.

Year	Author	Maximum Input Frequency (GHz)	Output Frequency	Type of Detection
2004	Appenzeller[85]	0.58	DC	DC mixing current
2005	Rosenblatt[86]	50	DC	DC mixing current
2006	Pesetski[87]	23	10 kHz	10 kHz mixing product
2008	Cobas[88]	18	DC	Diode rectification
2008	Zhong[84]	106-160	DC	DC mixing current

Table 5.1 Summary of high frequency CNT device experiments that directly observed CNT nonlinear behavior. The input frequencies, output frequencies, and the type of experiment are listed.

All of these publications take high frequency input signals and convert them

to low frequency or DC signals. There are two reasons for this. One is that the high

output impedance of individual CNTs causes the output signals to be of low

amplitudes. Output DC mixing currents typically require lock-in amplifiers to be

accurately measured. The other barrier to the detection of high frequency output

signals is the high cost of measurement equipment necessary to access high frequency

regimes. Until very recently, 50 GHz was near the limit of commercially available

spectrum analyzers, network analyzers, and oscilloscopes. Signal detection above 50

GHz has been prohibitively expensive. In the next section, we will describe our

method of detecting high frequency output signals.

The publication by Pesetski in 2006 was of an active device, where input signals were placed on the gate. The center frequency between two input signals separated by 10 kHz was swept up to 23 GHz. The 10 kHz mixing product, due to the difference between the two input frequencies, was detected for the full range of the input frequency sweep, indicating that the nonlinear behavior of the device continued up to 23 GHz. For the rest of publications in Table 5.1, the input signals were placed on the source and output was measured at the drain (or vice versa).

With this type of measurement setup, the device can be approximated as a low-pass filter (LPF), shown in Figure 5.2. In a low-pass filter, the capacitor acts as a complex voltage divider. For low frequency signals, the impedance of the capacitor is high, and the output voltage is close to the input voltage. As frequency is increased, the impedance of the capacitor decreases until it acts as a short to ground, and the voltage output is close to zero. There is a cutoff frequency associated with low-pass filters, called the corner frequency. It is defined as the frequency at which the output power drops to one-half of its low frequency value, which corresponds to a drop of 3.01 dB. It occurs when the magnitude of the reactance of the capacitor is equal to the resistance of the resistor, as shown in EQ 5.3 – 5.5.
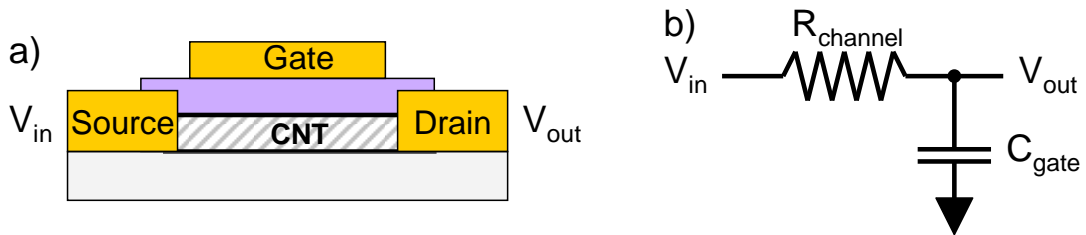
Figure 5.2 a) Diagram of CNT FET with the input signal on the source and the output signal on the drain. b) Circuit diagram of a low-pass filter.

$$|Z_c| = \left| \frac{1}{2\pi F_C C} \right| = R \quad \rightarrow \quad F_C = \frac{1}{2\pi RC} \qquad \text{EQ 5.3}$$

$$\left.\frac{V_{out}}{V_{in}}\right|_{F=F_C} = \left.\left|\frac{Z_C}{Z_C + R}\right|\right|_{F=F_C} = \frac{|-jR|}{|R - jR|} = \frac{R}{\sqrt{2R^2}} = \frac{1}{\sqrt{2}} \qquad \text{EQ 5.4}$$

$$\left.\frac{P_{out}}{P_{in}}\right|_{F=F_C} = \left(\left.\frac{P_{out}}{P_{in}}\right|_{F=F_C}\right)^2 = \frac{1}{2} \qquad \text{EQ 5.5}$$

A corner frequency indicates output signal attenuation. It does not mean that a device no longer responds to frequencies above F_C, but that the power available is reduced. Beyond the corner frequency, the output power from a LPF decreases with a slope of 20 dB per decade. Many publications on the HF performance of CNT devices take R to be the channel resistance, and C to be the gate capacitance, to extract a corner frequency. If that were done with one of our typical CNT FETs ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm), the channel resistance would be 7 kΩ, and the gate-CNT capacitance would be 100 fF, resulting in $F_C = 230$ MHz.

There is one more cutoff frequency to consider in such a measurement setup. For an output signal to reach the drain electrode, charges originating at the source electrode must span the nanotube device channel. If the period of an input frequency is greater the transit time of charges in the channel, the field in the nanotube will change direction before charges have reached the drain, sending them back toward the source. At frequencies well above this transit time cutoff frequency, no signal will be detected at the drain. This cutoff frequency is given by EQ 5.6, where L is the channel length.[83, 89, 90]

$$f_{tr} = \frac{v_{drift}}{2\pi L} \qquad \text{EQ 5.6}$$

The drift velocity is directly proportional to the carrier mobility ($v_{drift} = E\mu$), so using high mobility semiconductors, like carbon nanotubes, increases this cutoff

frequency. An approximation for this cutoff can be made using the Fermi velocity in the ballistic limit for metallic or highly-doped semiconducting CNTs, which is 8 x 10^5 m/s.[16] The input field would need to be strong enough to accelerate charges to that velocity, and the channels would need to be short enough to allow ballistic transport, so this Fermi velocity provides an upper limit. For a 10 μm channel length device, the upper limit of the transit time cutoff frequency is 13 GHz. This cutoff is one of the reasons that short device channels are being pursued.

5.3 Tomonaga-Luttinger Liquid Theory

The one-dimensional nature of carbon nanotubes may enable an extension of this transit time cutoff frequency. For three-dimensional semiconductors, the Fermi gas model is used and the repulsive Coulomb interactions between charges are ignored as typical electron densities make them improbable. However, in the one-dimensional channels of carbon nanotubes, Coulomb interactions between charges are unavoidable and result in wave-like excitations called plasmons, which behave more like bosons than fermions. The theoretical analysis of transport in one-dimensional systems is the Tomonaga-Luttinger Liquid theory.[91-93]

The velocity of plasmon waves is expected to be greater than the velocity of non-interacting free charges. The ratio of these velocities is given by g, a dimensionless parameter that indicates the strength of the electron-electron interactions. For non-interacting charges in the Fermi model, $g = 1$. For repulsive electron-electron interactions, $g < 1$.

$$v_p = \frac{v_F}{g}$$
EQ 5.7

83

This same effect can be seen when considering a carbon nanotube as a transmission line with a distributed kinetic inductance.[94, 95] The velocity of charges through a transmission line is known to follow EQ 5.8.

$$v = \sqrt{\frac{1}{L_{tot}C_{tot}}} \qquad \text{EQ 5.8}$$

For nanotubes on a high frequency insolating substrate, the only inductance will be the kinetic inductance (L_k). The total capacitance will be a combination of the quantum capacitance (C_Q) and the electrostatic capacitance (C_{ES}) from the nanotube to the gate electrode. These quantities are shown in EQ 5.9, where h is the dielectric thickness and d is the nanotube diameter.

$$L_k = \frac{h}{2e^2 v_F} \qquad C_Q = \frac{2e^2}{hv_F} \qquad C_{ES} = \frac{2\pi \in}{\ln(h/d)} \qquad \text{EQ 5.9}$$

Using this transmission line analysis gives the same wave velocity dependence on g as expected from Tomonaga-Luttinger Liquid Theory. Considered the four quantum channels in a single CNT, the wave (plasmon) velocity would follow EQ 5.10.

$$v_p = \sqrt{\frac{1}{L_k C_{tot}}} = \sqrt{\frac{1}{L_k C_Q} + \frac{4}{L_k C_{ES}}} = v_F \sqrt{1 + \frac{4C_Q}{C_{ES}}} \equiv \frac{v_F}{g} \qquad \text{EQ 5.10}$$

The g-parameter for metallic CNTs (or highly doped semiconducting CNTs) has been measured in tunneling experiments to be between 0.25 and 0.33.[96-99] This would mean that the velocity of plasmons should be three to four times the Fermi velocity, allowing plasmons to span longer channels than would possible with non-interacting charge transport. The publication by Zhong et al.[84] in Table 5.1 attempted to detect this plasmon velocity by using a THz laser to excite broadband 1 – 1.5 ps

signals in a transmission line attached to a CNT FET. By controlling the delay time between two pulses, resonances can be induced in the channel corresponding to the overlap of the reflected first pulse with the incident second pulse. These resonances were detected in devices of several channel lengths as changes in output currents, and from the resonance time delays, the charge carrier velocities were extracted. Surprisingly, the velocities were found to match the Fermi velocity of non-interacting charges and not the expected plasmon velocity. Even at input frequencies near 100 GHz, non-interacting charge motion appears to dominate transport in CNTs.

5.4 Our High Frequency Experimental Method

As seen in the recent publications investigating the nonlinear high frequency behavior of CNT devices (Table 5.1), high frequency input signals are typically converted to low frequency or DC output signals because of large output impedance of individual CNTs and the high cost of high frequency measurement equipment. We use our CNT FETs as mixers to convert high frequency input signals to even higher frequency output signals (between 75 and 110 GHz) that are directly observed. This is accomplished first by decreasing the device output impedance by using hundreds of CNTs in parallel. Though this increases the output amplitude of the generated signals, they are still much smaller than the input amplitudes. Detection is accomplished with a spectrum analyzer which has a low noise floor, near 90 dBm, allowing the precise measurement of very small signals. Lastly, the financial obstacle is overcome by combining an external harmonic mixer with our spectrum analyzer to shift the detection range up to 110 GHz. Our devices mix input frequencies up into the 75 to

110 GHz regime, then the external mixer down-converts them to frequencies that the spectrum analyzer can detect. This allows for the direct observation of high frequency output signals, something that has not been done with nanotube devices before.

Three cutoff frequencies were mentioned in the previous section. Largely because of our relatively long device channel lengths, if applied to our devices, these cutoff frequencies would be below the input frequencies where our devices are operated. If our devices were used actively, they would have an expected intrinsic current gain cutoff frequency near 640 MHz. If they were measured passively, with an input signal on the source and an output signal taken at the drain, they would have an expected corner frequency of 230 MHz and an expected maximum transit time cutoff frequency of 13 GHz, beyond which no output signal should be detectable. To overcome these relatively low frequency restrictions, our devices are used in a new measurement setup that allows proper operation beyond these cutoff frequencies.

Our CNT FETs are used as passive mixers. Passive operation cannot achieve gain, so the current gain cutoff does not apply to our experiments. Instead of placing our input signals on the source, as was done for passive operation in the publications previously mentioned, our input signals are placed on the gate. This measurement setup changes the equivalent circuit geometry so that it no longer closely resembles a low-pass filter. A first order circuit model of our measurement technique is shown in Figure 5.3. The capacitive coupling from the gate to the CNT is treated as linked to the middle of the tube. There is a still a capacitance from the input signal to ground (C_{GS}), but it is in parallel with capacitors from the gate to the CNT (C_{GCNT}) and the gate to the drain (C_{GD}). As the input frequency is increased, the impedance of all three

capacitors decreases. It is only because of the extra resistances from the nanotubes and the drain to ground that the power lost to the grounded source becomes significant.
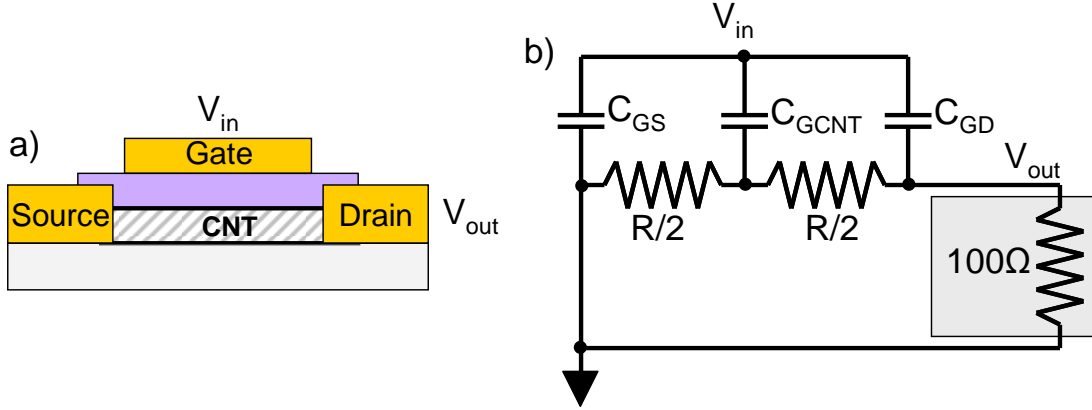
Figure 5.3 a) Diagram of CNT FET with the input signal on the gate, the output signal on the drain, and the source grounded. b) Circuit diagram of CNT FET shown in a).

The resistances of our nanotube channels are typically on the order of $k\Omega$s, much larger than the 100 Ω impedance of our measurement equipment. Therefore, the equivalent resistance from the drain (where the output signal is taken) to ground will be close to 100 Ω. The output voltage will thus be divided by the impedance of C_{GD} and the 100 Ω path from the drain to ground, given by EQ 5.11.

$$\left| \frac{V_{out}}{V_{in}} \right| = \left| \frac{100}{Z_{GD} + 100} \right| \qquad \text{EQ 5.11}$$

$$Z_{GD} = \frac{-j}{2\pi f C_{DG}} \qquad \text{EQ 5.12}$$

Using $C_{GD} = 30$ fF (extracted in Appendix D), at f = 1 GHz, $V_{out}/V_{in} \approx 0.019$. At f = 10 GHz, $V_{out}/V_{in} \approx 0.19$. At f = 40 GHz, our maximum possible input frequency, $V_{out}/V_{in} \approx 0.60$. So at low frequencies, small voltages are induced at drain electrode from the input voltage at the gate. As the input frequency increases, larger voltages are induced at the drain. Since the source electrode is grounded, this voltage

at the drain is equal to the source-drain bias. This demonstrates how an AC signal on the gate induced an AC signal at the drain. Even in a perfectly symmetric device, where $C_{gs} = C_{gd}$, the extra impedance through the measurement equipment at the drain will allow a source-drain bias to be induced. However, attenuation could be decreased my minimizing the gate-source capacitance, so a slightly asymmetric device may be preferable.

Note that it is power that is measured by the spectrum analyzer, so a low output voltage does not necessarily mean the output power is low. Opposite charges accumulate on the plates of a capacitor, so when the AC voltage on the gate is positive, a negative voltage is induced at the drain. From the transistor equation in the linear region presented in Chapter 2 (EQ 2.3), both a positive gate voltage and negative source-drain voltage decrease the channel conductance. When the AC voltage on the gate is negative, the induced voltage on the drain is positive, both of which increase the channel conductance. This difference in conductance maintains the nonlinear behavior of the CNT FET.

This analysis ignored the current passing through the CNTs, since the resistance through the measurement equipment is much smaller than the resistance through the channel. It is only the current passing through the carbon nanotubes that will produce the mixing signals that we measure. To estimate the attenuation of mixing output signals, the ratio of the power passing through the CNTs over the total power needs to be found.

The equations for the three current paths leaving the gate are shown in EQ 5.13 to 5.15. The sum of these currents will be the total current.

$$I_{GS} = V_{in} 2\pi C_{GS} F \qquad\qquad \text{EQ 5.13}$$

$$I_{GD} = \frac{V_{in}}{\dfrac{1}{2\pi C_{GD} F} + 100 \parallel R} \qquad\qquad \text{EQ 5.14}$$

$$I_{GCNT} = \frac{V_{in}}{\dfrac{1}{2\pi C_{GCNT} F} + \dfrac{R}{2} \parallel \left(\dfrac{R}{2} + 100 \right)} \qquad\qquad \text{EQ 5.15}$$

There are two current paths responsible for mixing. One passes through the gate-CNT capacitor, then through half of the nanotube channel into the drain. The other mixing current path passes through gate-drain capacitor, then through the full nanotube channel. These currents are given in EQ 5.16. Power goes as the square of current, so the power ratio is EQ 5.17.

$$I_{mix} = \frac{V_{in}}{\dfrac{1}{2\pi C_{GCNT} F} + \dfrac{R}{2} + 100} + \frac{V_{in}}{\dfrac{1}{2\pi C_{GD} F} + R} \qquad\qquad \text{EQ 5.16}$$

$$\frac{P_{CNT}}{P_{TOT}} = \left(\frac{I_{CNT}}{I_{TOT}} \right)^2 \qquad\qquad \text{EQ 5.17}$$

The device values used are $C_{GD} = 30$ fF, $C_{GS} = 30$ fF, $C_{GCNT} = 100$ fF, and R = 7 kΩ as extracted in Chapter 2 and Appendix D. The mixing output power using this circuit analysis is plotted, along with the output power from a low-pass filter with a corner frequency of 230 MHz, in Figure 5.4.
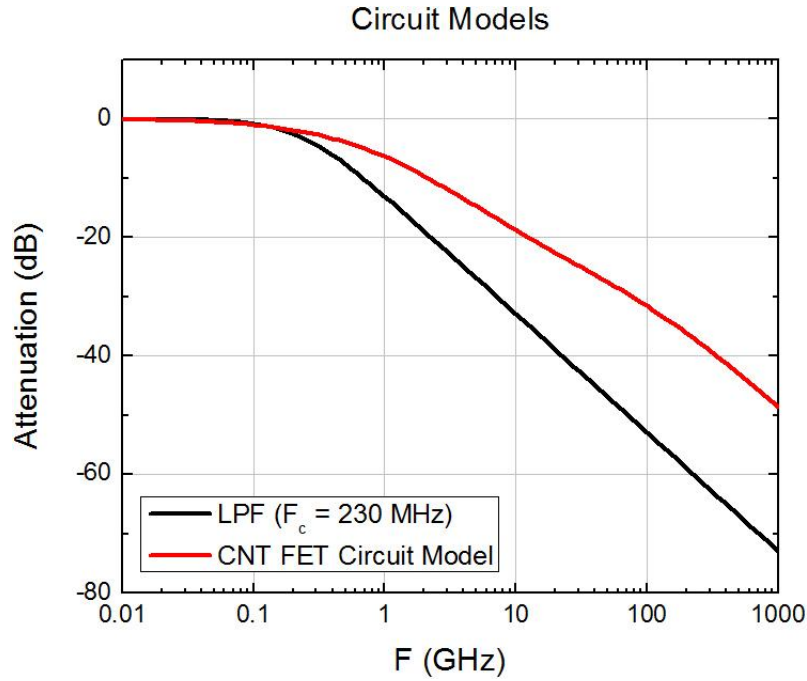
Figure 5.4 Output power drop as a function of frequency for a low-pass filter with a corner frequency of 230 MHz and for the nanotube circuit model shown in Figure 5.3.

Figure 5.4 shows that the output attenuation when the input signal is placed on the gate is less than when it is placed on the source. For the input frequencies that will be used during our high frequency measurements (25 to 37 GHz), attenuation between 20 and 30 dB is expected. However, since we are using a spectrum analyzer with a noise floor near 90 dBm, these output signals will still be detectable.

The other cutoff frequency when devices were used passively came from the transit time of charges in the channel. With an input signal on the source, charges had to span the channel to reach the drain, where the output was measured. Since our input signal is placed on the gate, spanning the device channel is no longer required. Charges entering the CNT will come from the drain as well as the source. At high frequencies, these charges will not span our long channel lengths, but the current coming from the drain will still be detected. The drain electrode charging time will be given by the resistance of our measurement equipment (100 Ω) and the gate-drain

capacitance (30 fF). That corresponds to a frequency of 53 GHz, which is greater than our maximum input frequency of 40 GHz. This means that for all of our measurements, charges should be able to move from the drain electrode in the CNTs, producing a measurable output, regardless of channel length.

So, by placing our input signal on our gate electrode and measuring the output signal on the drain, the output attenuation is reduced and the transit time cutoff is overcome. By using an external mixer in combination with a spectrum analyzer with a low noise floor, up to 110 GHz output signals are easily detectable. In the next chapter, the mechanisms of frequency mixing will be described, and an approximation of the device drain current under mixing will be derived.

Chapter 6: Carbon Nanotube Mixing Theory

In this chapter we will introduce a way of analyzing frequency mixing by using a simple Taylor expansion. The expected terms from single-tone and two-tone input signals will be derived, and the nomenclature used to distinguish two-tone mixing products is presented. The Taylor expansion is then modified for our passive mixing experiments, and its validity is experimentally tested by comparing the DC current from a 5 GHz input signal with the expected output. These models will then be used in the next chapter to understand the results from high frequency mixing experiments with carbon nanotube field-effect transistors.

6.1.1 Taylor Expansion of Input to Output Nonlinearity

Before discussing the high frequency (HF) mixing experiments done on the CNT FET devices, a brief review of frequency conversion is given. Frequency conversion is usually referred to as mixing because two or more input signals are effectively multiplied to generate new output frequencies. The multiplication comes from the non-linearity of the device under test.

Conventional analysis of mixing is done by using a Taylor expansion of a function that is non-linear in one input variable. The classic case is the description of a transistor with the output drain current I_{ds} expanded in terms of a small AC voltage δV about the input bias V_{ds}

$$I_d\left(V + \delta V\right) = I_d(V) + \frac{\partial I_d}{\partial V} \cdot (\delta V) + \frac{\partial^2 I_d}{\partial V^2} \cdot \frac{(\delta V)^2}{2!} + \frac{\partial^3 I_d}{\partial V^3} \cdot \frac{(\delta V)^3}{3!} + ... \qquad \text{EQ 6.1}$$

If the relationship between drain current and source-drain voltage in the CNT

FET devices were linear (Ohmic), all the higher order derivatives of the drain current

would be zero. However, as shown in Chapter 2, non-linearities in the output curve

(I_d vs. V_{ds}) exist due to Schottky contacts and the gate-induced field, so higher order

terms are necessary for the description of our devices.

For the expansion to be valid, δV must be small relative to the features of the

function. The magnitude of the oscillating voltage reaching the device depends on the

experimental setup, the frequency used, and the input power. We estimate that the

magnitude of the oscillating voltage reaching the device is significantly less than 1 V,

the typical magnitude of the DC bias. The largest signal output from our signal

generators in the high frequency mixing (75-110 GHz) experiments is +20 dBm (100

mW). Assuming we have an ideal transmission line, the power at the device input

will be the same as the power at the port of the signal generator.

$$P(port) = P(DUT) = \mathrm{Re}\!\left(V_{rms} \cdot I_{rms}^{*}\right) = 1/2\,\mathrm{Re}\!\left(V \cdot I^{*}\right) \qquad \text{EQ 6.2}$$

The maximum power is given by :

$$P_{max}(port) = P_{max}(DUT) = \frac{1}{2}VI = \frac{1}{2}\frac{V^{2}}{Z_{0}} \qquad \text{EQ 6.3}$$

where Z_0 is the characteristic impedance of the transmission line (i.e. 50 Ω).

Thus, V_{max} is given by:

$$V_{max} = \sqrt{2P_{max}(DUT)Z_{0}} = \sqrt{2 \cdot 100mW \cdot 50\Omega} = 3.16V \qquad \text{EQ 6.4}$$

However, measurements have shown that the transmission line is lossy in the

HF measurements described here. We typically observe 30 dB loss or more in the

signal, so the power reaching the device is at most -10 dBm (100 μW), and the

magnitude of the AC signal at the device is on the order of:

$$V_{device} = \sqrt{2 \cdot 100 \mu W \cdot 50\Omega} = 100 mV \qquad \text{EQ 6.5}$$

Since the amplitudes of the AC signal are 100 mV or less, we conclude that

the Taylor expansion can be safely applied in the analyses of our devices.

6.1.2 Harmonic Generation

Now consider a single-tone input signal of frequency ω with amplitude A:

$$\delta V = A\cos(\omega t). \qquad \text{EQ 6.6}$$

Obviously, the higher order terms in EQ 6.1 produce increasingly higher

powers of sinusoidal input, which in turn produces outputs at higher frequencies. For

example, using the trig identity for cosine squared:

$$(\cos \omega t)^2 = \frac{1}{2}(1 + \cos 2\omega t) \qquad \text{EQ 6.7}$$

the second order term becomes:

$$(\delta V)^2 = \frac{A^2}{2} + \frac{A^2}{2}\cos 2\omega t,$$

and thus the output frequency is doubled. $\qquad$ EQ 6.8

Similarly, the third and fourth-order products are:

$$(\delta V)^3 = \frac{3A^3}{4}\cos \omega t + \frac{A^3}{4}\cos 3\omega t \qquad \text{EQ 6.9}$$

$$(\delta V)^4 = \frac{3A^4}{8} + \frac{A^4}{2}\cos 2\omega t + \frac{A^4}{8}\cos 4\omega t. \qquad \text{EQ 6.10}$$

So even with only one input frequency, a non-linear device will produce harmonics of the input frequency. Also, note the presence of frequency-independent terms in the even-numbered products. This means that when an AC voltage is applied to a non-linear device, a DC current is generated. This fact will be examined more thoroughly later in this chapter.

6.1.3 Two-Tone Mixing Products and Corresponding Nomenclature

If the input signal consists of two tones ω_1 and ω_2, then the cross product terms in the expansion produce new frequencies at the sum and difference of ω_1 and ω_2. The first three products for two-tone mixing are shown below in EQ 6.11.

$$\delta V_{2tone} = \begin{cases} V_1 \cos\omega_1 t + \\ V_2 \cos\omega_2 t \end{cases}$$

$$(\delta V_{2tone})^2 = \begin{cases} \dfrac{V_1^2}{2} + \dfrac{V_2^2}{2} + \\ V_1 V_2 \cos(1\omega_1 - 1\omega_2)t + \\ \dfrac{V_2^2}{2} \cos(0\omega_1 + 2\omega_2)t + \\ V_1 V_2 \cos(1\omega_1 + 1\omega_2)t + \\ \dfrac{V_1^2}{2} \cos(2\omega_1 + 0\omega_2)t + \end{cases}$$

$$(\delta V_{2tone})^3 = \begin{cases} \left[\dfrac{3}{4}V_1 V_2^2\right]\cos(-1\omega_1 + 2\omega_2)t + \\ \left[\dfrac{2}{3}V_1^2 V_2 + \dfrac{3}{4}V_2^3\right]\cos(0\omega_1 + 1\omega_2)t + \\ \left[\dfrac{2}{3}V_1 V_2^2 + \dfrac{3}{4}V_1^3\right]\cos(1\omega_1 + 0\omega_2)t + \\ \left[\dfrac{3}{4}V_1^2 V_2\right]\cos(2\omega_1 - 1\omega_2)t + \\ \left[\dfrac{1}{4}V_2^3\right]\cos(0\omega_1 + 3\omega_2)t + \\ \left[\dfrac{3}{4}V_1 V_2^2\right]\cos(1\omega_1 + 2\omega_2)t + \\ \left[\dfrac{3}{4}V_1^2 V_2\right]\cos(2\omega_1 + 1\omega_2)t + \\ \left[\dfrac{1}{4}V_1^3\right]\cos(3\omega_1 + 0\omega_2)t + \end{cases}$$

EQ 6.11

To identify peaks in the output spectrum, we introduce the standard naming convention used for identifying the various frequencies that arise. By convention the ordered pair (n, m), which represents $n\omega_1 + m\omega_2$ where n and m are integers, is used to identify the particular output frequency of interest. **Note that these integers are NOT the same as those in CNT chiral vectors.** For the rest of this dissertation, the ordered pair (n, m) will always be used to refer to a particular mixing output frequency.

Furthermore, the sum $|n| + |m|$ is used to identify the mixing order of a particular measurement, which also corresponds to the lowest order expansion that would produce an output at that frequency. However, higher order products can also fall into lower order frequencies. For example a 3rd order expansion will produce a signal at the 3rd harmonic of F_1, $(3, 0) = 3F_1 + 0F_2$. A 5th order expansion will also produce a signal at the same frequency from the 4th harmonic mixing with the fundamental, $4F_1 - F_1 = 3F_1$, which is still $(3, 0)$. Since the Taylor expansion carries the coefficient of 1/(order factorial), each output frequency is typically dominated by the contribution from the lowest order term.

As an illustration, consider Figure 6.1, where the output from the spectrum analyzer centered at 75.5 GHz is shown. The input frequencies are 25.1667 GHz $\pm$ 50 kHz. Since the acquisition window is centered near $3F_{1,2}$, higher ordered odd terms up to the 11th order can be seen before the spectral output drops into the noise floor at -90 dB. The labeling procedure illustrated below is useful for identifying particular output frequencies of interest that are present in the acquisition window of the

spectrum analyzer. We note here that the mixing products shown below will be evaluated in detail in Chapter 6.
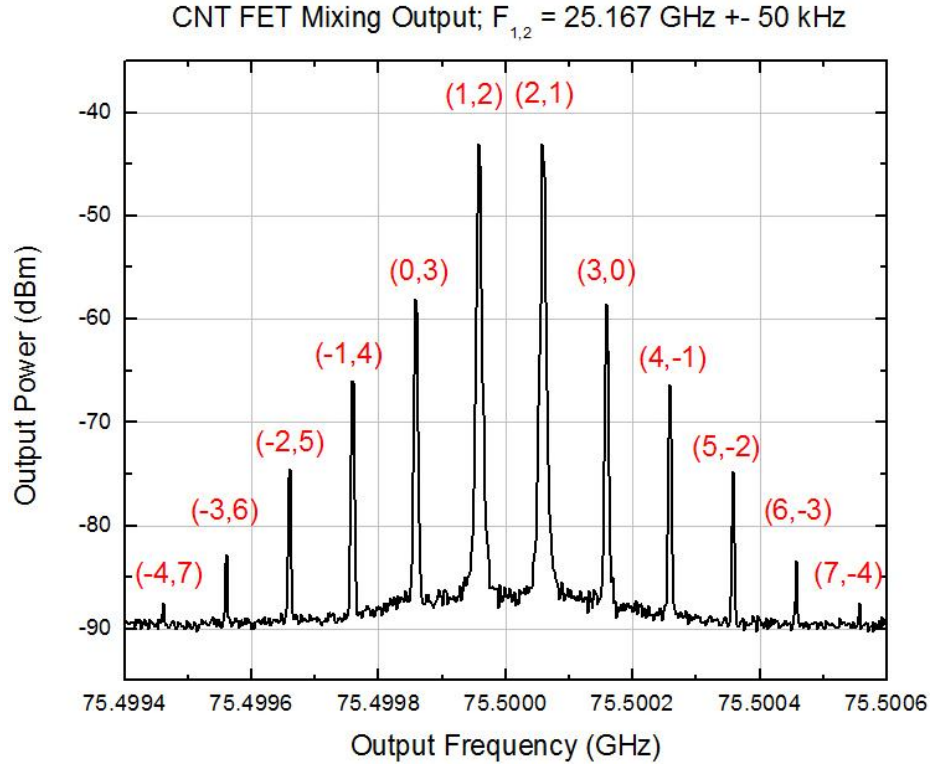
Figure 6.1 Output power spectrum read by an Agilent MXG analog signal generators when using a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm) as a passive mixer. The input signals on the gate were -10 dBm at frequencies = 25.1667 GHz ± 50 kHz. The peaks are labeled with their corresponding (n, m) notation.

6.2 Modified Taylor Expansion for Passive CNT Mixing

Now we modify the Taylor expansion to describe how the CNT FET devices were measured. Our AC input signal is placed on the gate electrode. Because of the large number of CNTs in the channel, a signal on the gate will also induce a signal in the channel (as shown in the previous chapter), resulting in two AC voltages in our expansion.

$$V + \delta V = V_{gs} + \delta V_{gs}, V_{ds} + \delta V_{ds} \qquad \text{EQ 6.12}$$

$$I_d\left(V_{gs}+\delta V_{gs},V_{ds}+\delta V_{ds}\right)=I_d(V_{gs},V_{ds})+\left\{\begin{array}{l}\dfrac{\partial I_d}{\partial V_{gs}}\cdot(\delta V_{gs})+\dfrac{\partial^2 I_d}{\partial V_{gs}^{~2}}\cdot\dfrac{\left(\delta V_{gs}\right)^2}{2!}+...\\[3mm]\dfrac{\partial I_d}{\partial V_{ds}}\cdot(\delta V_{ds})+\dfrac{\partial^2 I_d}{\partial V_{ds}^{~2}}\cdot\dfrac{\left(\delta V_{ds}\right)^2}{2!}+...\end{array}\right\}\quad\text{EQ 6.13}$$

Substituting in the definitions of transconductance and dynamic conductance (EQ 2.3 And EQ 2.4) produces EQ 6.14.

$$I_d\left(V_{gs}+\delta V_{gs},V_{ds}+\delta V_{ds}\right)=I_d(V_{gs},V_{ds})+\left\{\begin{array}{l}g_m\cdot(\delta V_{gs})+\dfrac{\partial g_m}{\partial V_{gs}}\cdot\dfrac{\left(\delta V_{gs}\right)^2}{2!}+...\\[3mm]G_D\cdot(\delta V_{ds})+\dfrac{\partial G_D}{\partial V_{ds}}\cdot\dfrac{\left(\delta V_{ds}\right)^2}{2!}+...\end{array}\right\}\quad\text{EQ 6.14}$$

Our high frequency mixing experiments are done in the absence of a constant source-drain bias, which means the mixing is being done passively. More specifically, this means that our devices do not have a source-drain bias because the only power reaching the device is applied to the gate electrode. The primary reason for this experimental configuration is that we were unable to find bias-tees rated in the W-frequency regime, and our electrodes were not designed to be large enough to allow an extra DC probe to add that bias.

Passive mixing cannot produce gain, but apart from a reduced output signal, it can perform the same functions as active mixing, and if necessary, the output signals can be amplified post-mixing. A significant advantage of passive mixing is that it eliminates the power losses associated with the source-drain bias-induced current through metallic CNTs in the as-grown networks, as mentioned in Chapter 4. Recall that we demonstrated that the metallic CNTs can be successfully burned out, which reduces the total number of CNTs and effectively increases the channel impedance. Here, the mixing signals being measured are related to the device output impedance,

so samples with more CNTs will produce larger output signals, making them easier to detect. Thus, passive mixing allows us to use samples with the largest number of CNTs while avoiding the unwanted constant drain current from the presence of metallic CNTs.

Without a DC source-drain bias, the first term in the expansion, the DC drain current, will be zero. The transconductance and all its derivatives will also be zero for $V_{ds} = 0$, as shown in Chapter 2. Our expansion then reduces to EQ 6.15.

$$I_d\left(V_{gs} + \delta V_{gs}, \delta V_{ds}\right) = G_D \cdot (\delta V_{ds}) + \frac{\partial G_D}{\partial V_{ds}} \cdot \frac{(\delta V_{ds})^2}{2!} + \dots \qquad \text{EQ 6.15}$$

This shows that even though our input signal is placed on the gate, it is the induced signal across the channel that generates all the mixing products. This probing arrangement allows us to ground the source with one probe, apply a signal on the gate with another, and measure the output on the drain. Our last step is to take the derivatives of the dynamic conductance with respect to the gate voltage instead of the source drain voltage, a substitution derived in Chapter 2 (EQ 2.5). This form is useful in the DC mixing current measurements in the next section. The final form of our expansion is EQ 6.16.

$$I_d\left(\delta V_{ds}\right) = G_D \cdot (\delta V_{ds}) - \frac{\partial G_D}{\partial V_{gs}} \cdot \frac{(\delta V_{ds})^2}{2!} + \dots \qquad \text{EQ 6.16}$$

We briefly mention a subtle point about EQ 6.16. It only applies to the bulk of the nanotube, assuming that the contact resistances are negligible. However, when the contacts resistances are comparable with the resistance of the CNT, an adjustment to include the contact effects will have to be made to EQ 6.16. When unbiased, our CNT FETs are in an off-state, and EQ 6.16 is expected to apply.

As mentioned in the single-tone analysis of section 6.1.2, the even power products in the expansion contain a DC term, so an AC input voltage should produce a DC current. Previous groups have reported measuring this DC current, referred to as the mixing current, in the absence of an external source-drain bias in CNT FETs and diodes.[85, 86, 88] The effect was described by Appenzeller as "the *increase* in current for one half cycle of an AC oscillation is different from the *decrease* in current for the other half of the cycle,"[85] so over time, more charges are pushed in one direction than in the other, resulting in a net DC current. Considering only the second-order mixing product, the DC mixing current due to the CNT should be:

$$I_{mixCNT}(\delta V) \approx -\frac{A^2}{4}\frac{\partial G}{\partial V_{gs}}$$

EQ 6.17

To test this relation, the DC mixing current was measured as a function of gate voltage for our CNT FETs. At the same time, measurements of conductance were taken so that both sides of EQ 6.17 could be compared. The following experimental setup was used:
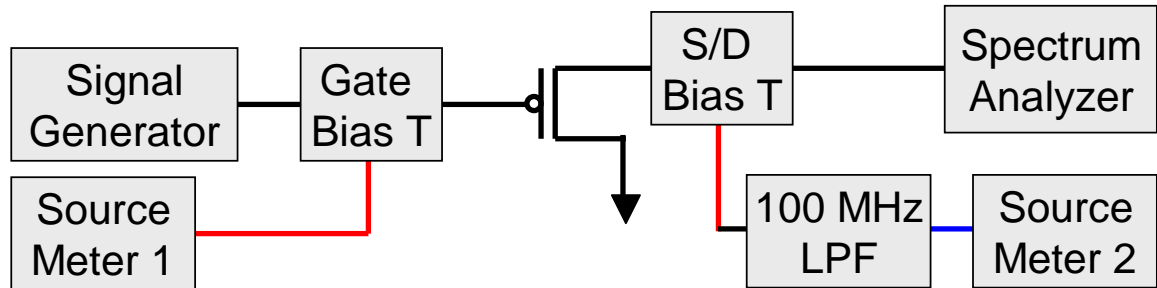
Figure 6.2 Diagram of the experimental setup used to measure the DC mixing current produced from a single frequency input. The black, red, and blue lines correspond to SMA, SMC, and BNC cables respectively.

The components used were:

Agilent MXG Analog Signal Generators (N5183A): 100 kHz – 40 GHz
Anritsu K250 Bias Tees: DC – 40 GHz
Keithley 2400 Source-Meters: DC
Picoprobe 40A-GSG-150µm-LP probes: DC – 40 GHz
Crystek 100 MHz Low Pass Filter (CLPFL – 0100)
Agilent ESA-E Series Spectrum Analyzer (E4407B): 9kHz – 26.5 GHz
SMA coaxial cables: DC – 18 GHz (shown in black)
SMC coaxial cables: DC – 10 GHz (shown in red)
BNC coaxial cables: DC – 3 GHz (shown in blue)

The bias tees allow the setting of a DC bias but also the measurement of the

DC current. Typically, measurements of DC mixing current require the use of a lock-

in amplifier. However, measuring this current was possible with a source-meter

because of the large number of CNTs in the device channel.

To ensure a large enough signal to accurately measure, a large input power of

18 dBm was used. This corresponds to a maximum voltage of 3.55 V. Not all of the

voltage drop occurs across the CNTs, so this estimate provides an upper limit for the

input voltage, A. We note that this input amplitude is 25 times larger than the

maximum amplitude used in the high frequency mixing experiments.

The microwave signal generator sourced a constant 5 GHz 18 dBm AC signal.

The measurement procedure was to set a gate voltage with the first source-meter, then

the source-drain bias was swept with the second source-meter between ± 50 mV by

10 mV increments. The resulting I_d vs. V_{ds} data for each gate voltage was fit to a line,

where the extracted slope was the conductance, and the intercept was the DC mixing

current. The gate voltage was swept between ±10 V in steps of 100 mV. The

measured conductance is plotted in Figure 6.3, clearly showing the non-linear

features of the device.
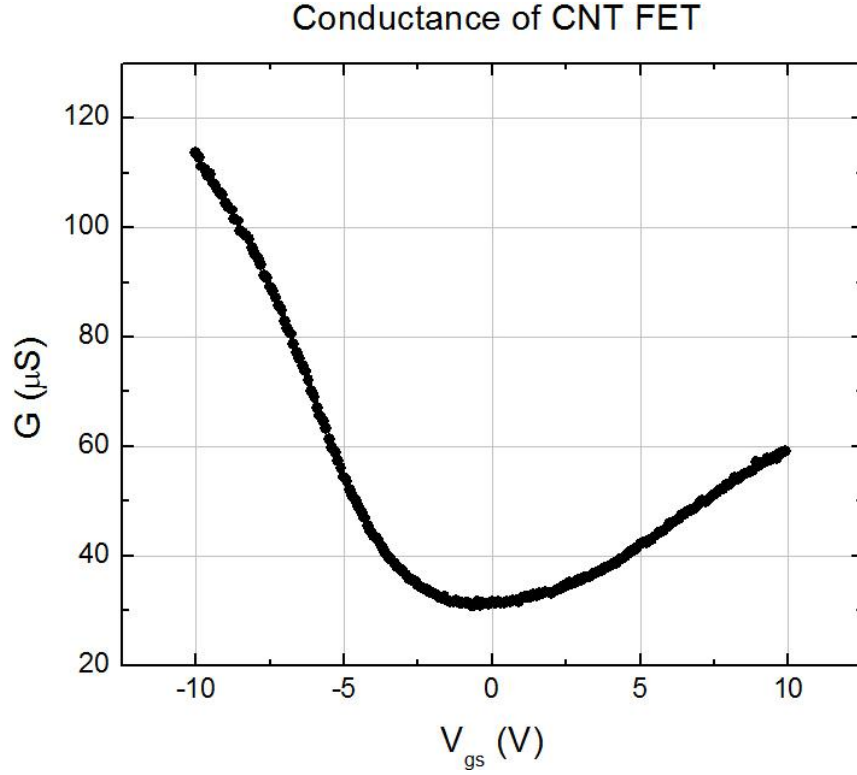
Figure 6.3 Conductance vs. gate voltage for a top-gated CNT FET on quartz ($W = 100$ μm, $L = 10$ μm, and $G = 8$ μm). Measurements were made with an 18 dBm 5 GHz signal input on the gate. Conductances were computed at each gate voltage by sweeping the source-drain bias between ±50 mV by 10 mV steps and equal to the extracted slope of each sweep.

The derivative of this conductance (with respect to gate voltage) was taken to compare it with the measured DC mixing current. To calculate the derivative, a line was fitted over five points (400 mV span) and the slope extracted. Using $A = 3.55$ V,

EQ 6.17 becomes: $I_{mixCNT} \approx -3.15 \dfrac{\partial G}{\partial V_{gs}}$. Both sides of that equation are plotted in

Figure 6.4.

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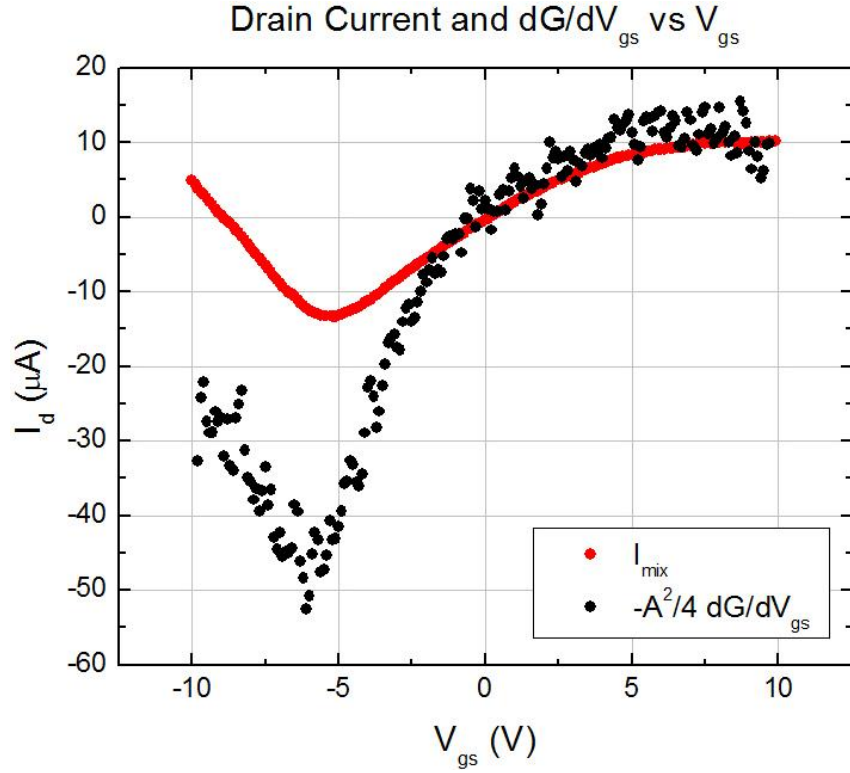
Figure 6.4 Plot of the measured drain current and the derivative of the measured conductance with respect to gate voltage scaled by 3.15 while a 5 GHz signal is input on the gate. The 3.15 comes from A = 3.55 V in EQ 6.17.

There appears to a qualitative agreement between the two quantities, with the least amount of agreement for large negative gate voltages. This is expected, since the expansion used should only apply when the voltage drop is primarily across the nanotube, which is when the semiconducting CNTs are gated off. When the semiconducting CNTs are gated on, the gate-independent mixing due to the Schottky barrier will compete with the mixing due to CNT non-linearities. In addition, when the semiconducting CNTs are gated on, the resistance of the CNT network is now roughly the same as the contact resistance between the CNT and metal electrodes. Previously, the contact resistance was estimated to be about 4 kΩ. Correcting for these voltage drops produces EQ 6.18 and Figure 6.5.

$$I_{mix} = I_{mixCNT} \frac{R_{CNT}}{R_{tot}} \qquad\qquad \text{EQ 6.18}$$

Drain Current and (R_{cnt}/R_{tot}) dG/dV$_{gs}$ vs V$_{gs}$
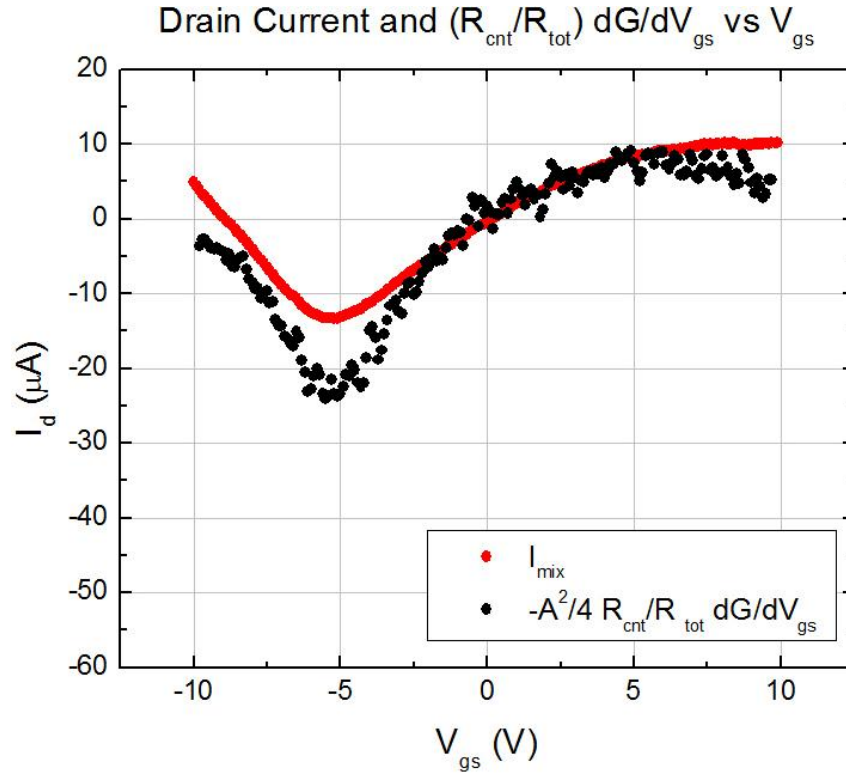
Figure 6.5 Plot of the measured drain current and the derivative of the measured conductance with respect to gate voltage, times the nanotube resistance, divided by the total channel resistance, scaled by 3.15 while a 5 GHz signal is input on the gate. The 3.15 comes from A = 3.55 V and EQ 6.17.

The correspondence between the measured mixing current and the calculated change in conductance is much better when considering the effects of contacts. The observed deviations could be due to several causes. First, we have only considered the second order DC contribution, while all higher order even terms will add to the DC current and have their own gate voltage dependences. Moreover, the conductance that we used for our derivative is the DC conductance. Nanotube conductance may be frequency-dependent, though this measurement indicates that conductance at 5 GHz is close to the DC conductance. Lastly, the amplitude used for our input signal was an

upper limit which assumed that all the power fell across the CNTs. Considering all of these effects, the agreement between the curves is reasonable and suggests that the Taylor expansion we use to represent the drain current is appropriate.

We note that no source-drain biases are used in our high frequency mixing measurements (to be discussed in Chapter 6), and our input signals are centered at V_{gs} = 0. This is a regime where the semiconducting CNTs are gated off and the agreement between the DC mixing current and the change in conductance is reasonably high.

6.4 Summary

We have presented an approximation of the drain current of a CNT FET as a Taylor expansion of a small input voltage. A single tone input will generate harmonics of the input frequency, while a two-tone input will produce many mixing products. The expected amplitudes of up to third-order products are listed, and the nomenclature used to specific mixing products is presented. The Taylor expansion was then modified to represent passive mixing (V_{ds} = 0) and expressed in terms of the gate voltage dependence of conductance. A single tone mixing experiment was performed to test the validity of this expansion. The DC mixing current was measured and compared with the expected output derived from the derivative of conductance with respect to gate voltage. The two were shown to match well in the regions where the approximation was valid. This verifies that our Taylor expansion is a valid representation of our devices under small AC inputs.

Chapter 7: CNT Mixing Data

In this chapter, the results from two-tone mixing experiments are presented with output frequencies in two different regimes. This division is due to the availability of experimental components needed to perform the measurements. Frequency regimes will be referred to by the type of coaxial connectors used in each regime. The three regimes involved in our experiments are SMA (up to 26.5 GHz), K (up to 40 GHz), and W (up to 110 GHz). We first discuss experiments with output frequencies from 250 MHz to 26.5 GHz (SMA regime). In this regime, CNT FETs are compared with control devices to determine if any mixing signals come from the experimental setup itself. Then we present the measurements performed with output frequencies from 75 to 110 GHz (W regime). In this regime, the mixing output amplitudes are compared with their expected values from our Taylor expansion of drain current. Lastly, measurement sweeps of the output frequency in the W regime are made with one input signal fixed and the other swept to compare different types of devices and understand their frequency dependent outputs.

7.1 250 MHz to 25 GHz (SMA Regime) Measurements

Mixing experiments in the 100 kHz to 26.5 GHz are discussed in this section. The measurements are limited to 26.5 GHz by the spectrum analyzer. The experimental setup used in the SMA regime is shown in Figure 7.1.
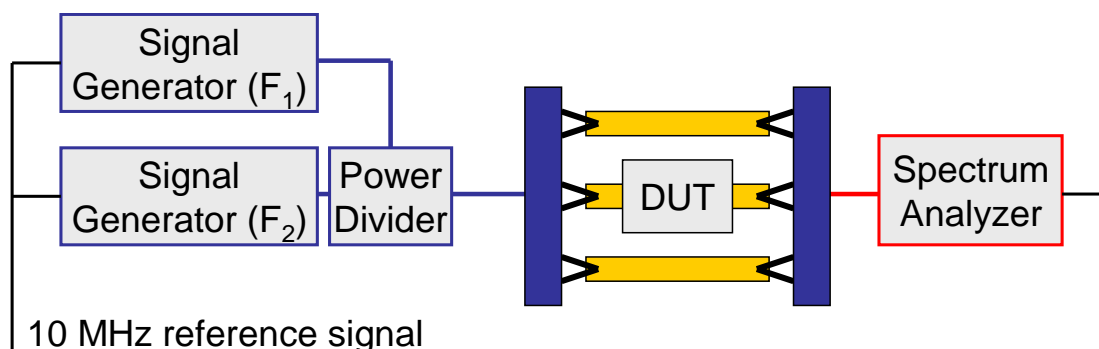
Figure 7.1 Diagram of the experimental setup used to perform mixing experiments in the SMA regime. The black, red, and blue lines correspond to BNC, SMA, and K coaxial cables respectively. A 10 MHz reference signal is generated by the spectrum analyzer and input to both signal generators. The outer wings of the probes are grounded through the coaxial cables.

The components used and the frequencies over which they are rated are:

Agilent MXG Analog Signal Generators (N5183A): 100 kHz – 40 GHz
Anritsu Power Divider (K240C): DC – 40 GHz
Picoprobe 40A-GSG-150μm-LP probes: DC – 40 GHz
Agilent ESA-E Series Spectrum Analyzer (E4407B): 9kHz – 26.5 GHz
BCN coaxial cables: DC – 3 GHz (shown in black)
SMA (3.5 mm) coaxial cables: DC – 26.5 GHz (shown in red)
K (2.92 mm) coaxial cables: DC – 46 GHz (shown in blue)

The first signal generator is connected to the power divider through a K

coaxial cable. The second signal generator is connected to the power divider through

a male-male (M-M) K connector. The attenuation through the coaxial cable is about 1

dB greater than through the M-M connector, so to have roughly equal input powers

from both sources, the output amplitude of the first signal generator is 1 dB higher

than the second signal generator. The power divider is not a directional coupler, but

merely divides the power at each terminal to the other two. All the CNT devices

measured contain outer electrodes separated by 300 μm that are grounded by the

outer electrodes of the GSG probes. A 10 MHz reference signal from the spectrum

analyzer is used to synchronize both signal generators. The signal generators and

spectrum analyzer were controlled with Labview with GPIB communication. Unless

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otherwise specified, all the data was acquired with the spectrum analyzer window set

to the following: a center frequency of 1.2 MHz, a resolution bandwidth of 3 kHz,

and the number of points per sweep is 600. The two tones from the signal generators

were separated by 100 kHz .

$$F_1 = F_{in} + 50kHz \qquad\qquad F_2 = F_{in} - 50kHz \qquad\qquad \text{EQ 7.1}$$

The center frequency between the two tones (F_{in}) was swept from 0.25 to 25

GHz in steps of 250 MHz. The output spectra were captured at acquisition windows

centered at the input frequency

Measurements were performed on four different types of devices. Later, we

refer to them as devices under test (DUTs). Three of the four devices are controls

used to assess the parasitic attenuation in the measurement setup, shown in Figure

7.2. The first two controls, through electrodes and a parallel plate capacitor, allow for

direct measurement of the system parasitics. For the parallel plate capacitor, the

center electrodes are vertically separated by an ALD Al_2O_3 dielectric layer (65 nm

thick). This structure has a DC capacitance near 44 pF. The third control consisted of

the same electrode geometry as the CNT FETs but with all the CNTs etched out of

the channel (essentially, a channel width of zero). This control (DC capacitance ~ 30

fF) allows for a direct comparison with the CNT device to clearly show the

contribution of the tubes to the output signals. The CNT FET structure was described

previously in Chapter 2. The CNT FET device measured had a channel width (*W)* of

100 μm, a channel length (*L*) of 10 μm, and a gate length (*G*) of 8 μm with a DC

capacitance of ~100 fF. The capacitances are extracted in Appendix D.
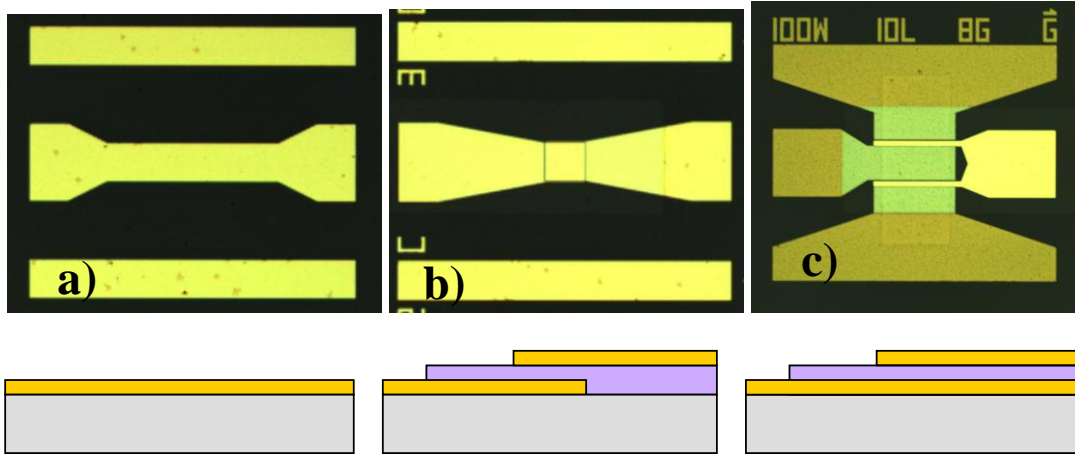
Figure 7.2 Optical images and side profile views of the different control DUTs used in the SMA two-tone mixing experiments. a) Through electrodes, b) parallel plate capacitors, c) FET geometry. The spacing between the center of the horizontal electrodes in each device is 150 μm.

The spectrum analyzer is used to measure the mixing output power levels. The output power attenuation is defined as the signal generator input power (17 dBm in these measurements) subtracted from the measured output power. Since the two-tone inputs are similar in magnitude, the calculated output power attenuation is the average of both peaks.

The output power attenuation for the three controls and the CNT device is plotted vs. input frequency in Figure 7.3. Obviously, the through electrodes and parallel plate capacitor devices attenuate the input signals nearly identically. The output from these two controls demonstrates the parasitic attenuation in the experimental setup due primarily to attenuation in the probes, but also to the cables and connectors. This attenuation runs from 8 dB at low frequencies to 30 dB at 25 GHz. We note that this output amplitude is not necessarily the power that drops across the channel of the CNT FET device because for the FET device the signal passes directly from the gate to the drain, and thus the signal across the FET channel is probably smaller. The attenuation for both of the FET structures (with and without

CNTs) is qualitatively similar. At low frequencies the attenuation is larger for the

control device (-55 dB) than the CNT FET device. At 20 GHz, the attenuation is

nearly identically for the two devices. By 25 GHz, the attenuation of all four device

structures is similar (~ -30 dB).
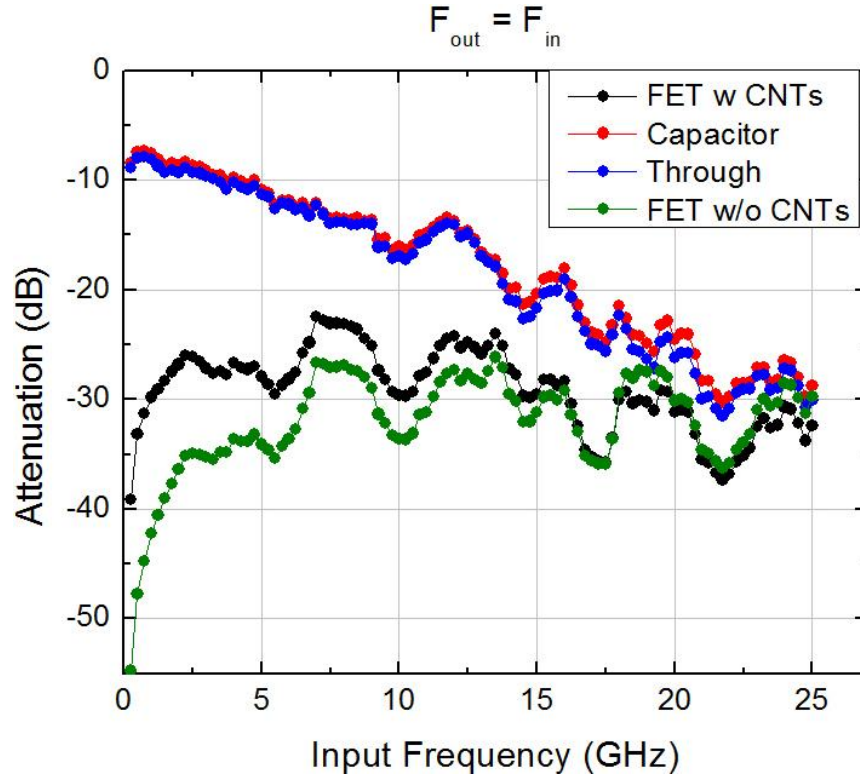
Figure 7.3 Plot of output power attenuation for four different device types vs. input frequency used in two-tone mixing. The input frequency was swept from 0.25 to 25 GHz by steps of 250 MHz, and the outputs were taken at the input frequency. The parallel plate capacitor used had a DC capacitance near 44 pF. The CNT FET measured had $W = 100$ μm, $L = 10$ μm, and $G = 8$ μm.

Output mixing spectra for the CNT FET and the capacitor control are plotted

in Figure 7.4 at input frequencies of 1 GHz and 25 GHz, near the minimum and

maximum of our spectrum analyzer. The output window is centered about the input

frequency. The spectra of the two devices are separated in each plot to more easily

see their features. At 1 GHz, both the CNT FET and the capacitor's spectra contain

many mixing products. At 25 GHz, the two spectra now have fewer mixing products, but are similar. Since the capacitor itself should not contain any non-linearities, we attribute the observed mixing signals to the experimental setup. Furthermore, the devices are not properly impedance-matched so significant power is reflected back from the device to the input of the signal generators, where mixing can occur. Mixing can also take place at the input of the spectrum analyzer, but the powers reaching the input of the spectrum analyzers are significantly lower than the rated input limit of 20 dBm. Thus, undesired mixing at the spectrum analyzer should be a negligible contribution to the parasitic mixing observed in the capacitor control device.
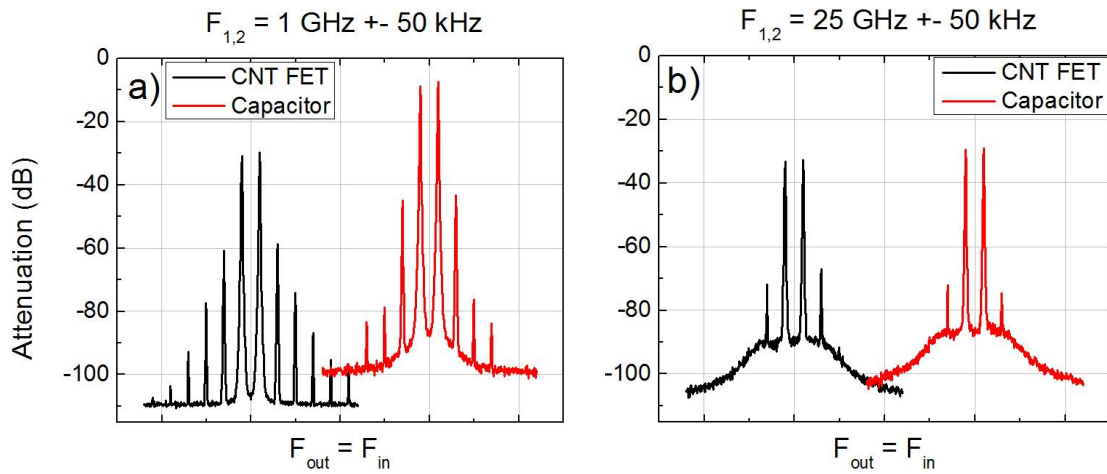
Figure 7.4 Output spectra captured from a spectrum analyzer from two-tone mixing experiments performs on a parallel plate capacitor and a CNT FET. The vertical axis is input power subtracted from the output power. The input frequencies were a) 1 GHz and b) 25 GHz. The two spectra in each plot are separated by 1 MHz to more clearly see their features.

The similarities between the mixing products of the CNT FET and the control around the input frequencies are problematic for quantitative analysis of the data. There is no clear way to determine if the mixing products are coming from the CNTs or the equipment.

To address this problem, output spectra were taken at three times the input frequency, centered about the third-order harmonics. This arrangement minimizes the contributions from the input signals passing directly through the devices. The output spectra for the CNT FET and the three controls at three different input frequencies are plotted in Figure 7.5. As the input frequency increases, the mixing products from the controls decrease, falling near or below the noise floor by input frequencies of 3 GHz. The mixing products from the CNT FET remain strong for all three input frequencies. The two highest amplitude mixing products remain in the through-electrode control spectra even at an output frequency of 24.75 GHz. However, their amplitudes are 20 dB (100 times) below the CNT FET. Since this mixing is performed passively, the CNTs cannot be amplifying products from the system, so any CNT FET mixing products of higher output amplitudes than the controls must be due to the CNTs and not the equipment. Comparing the CNT FET to the control FET device without CNTs clearly shows that above output frequencies of 9 GHz the CNTs are responsible for the mixing products.
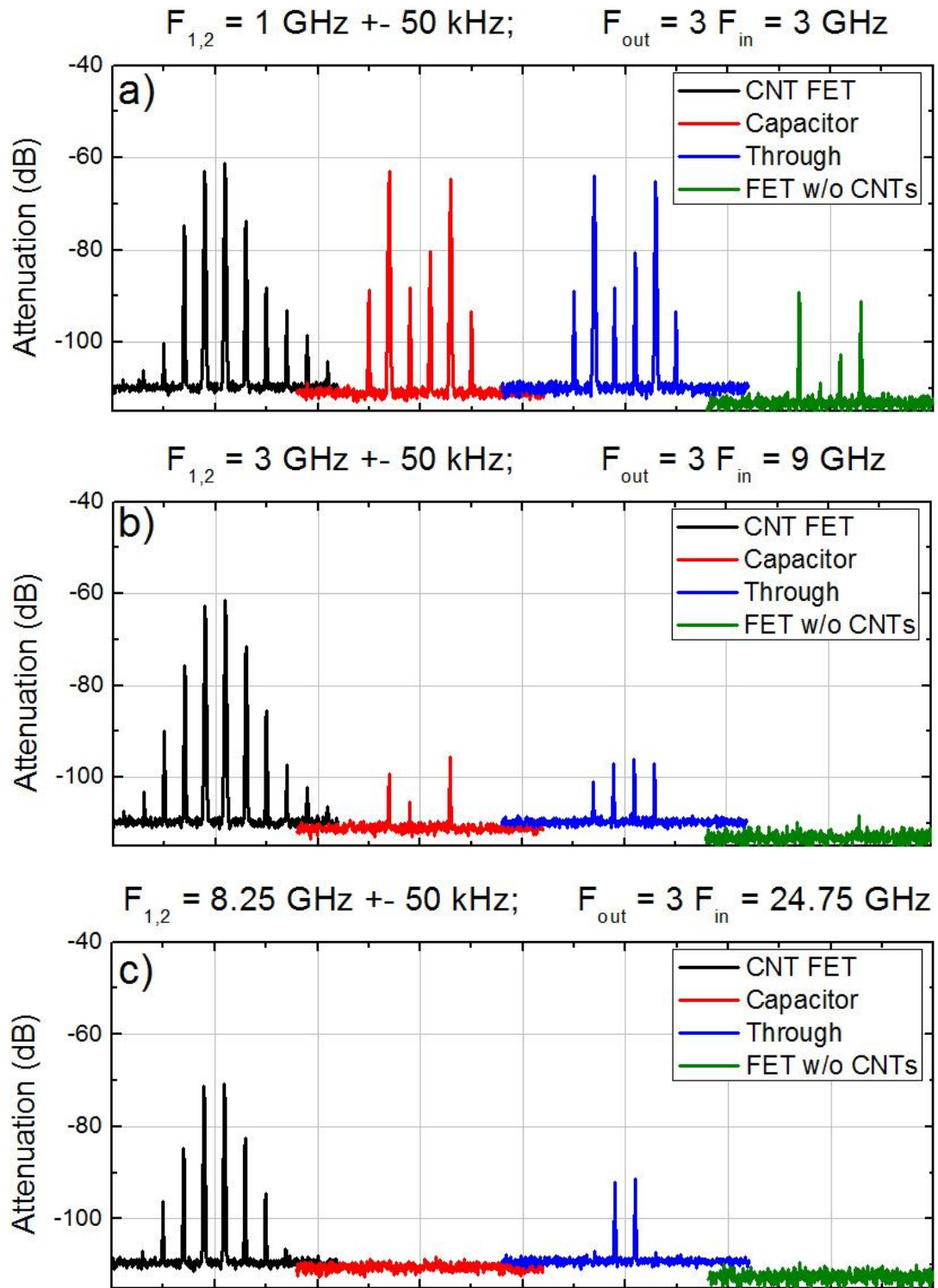
Figure 7.5 Output spectra captured at three times the input frequency from a spectrum analyzer from two-tone mixing experiments performs on a parallel plate capacitor and a CNT FET. The vertical axis is input power subtracted from the output power. The input frequencies were a) 1 GHz, b) 3 GHz, and c) 8.25 GHz. The two spectra in each plot are separated by 100 kHz to more clearly see their features.

Figure 7.5 represents only a small portion of the data taken. To compare data over the complete frequency range examined, the peak amplitudes at specific mixing product frequencies are plotted in Figure 7.6 for the four types of devices. The spectra used were captured at three times the input frequency. Only the third and fifth-order mixing products are plotted, as the higher order products are near the noise floor for the CNT FET. Each point in the graphs represents an average of the two corresponding peaks, labeled in the (n, m) notation. The amplitudes of each peak were computed as the maximum value in a 50 kHz span centered at each peak. The noise floor was computed as the minimum value in the 50 kHz span between the two center peaks. Spectra were captured with a resolution bandwidth of 3 kHz.
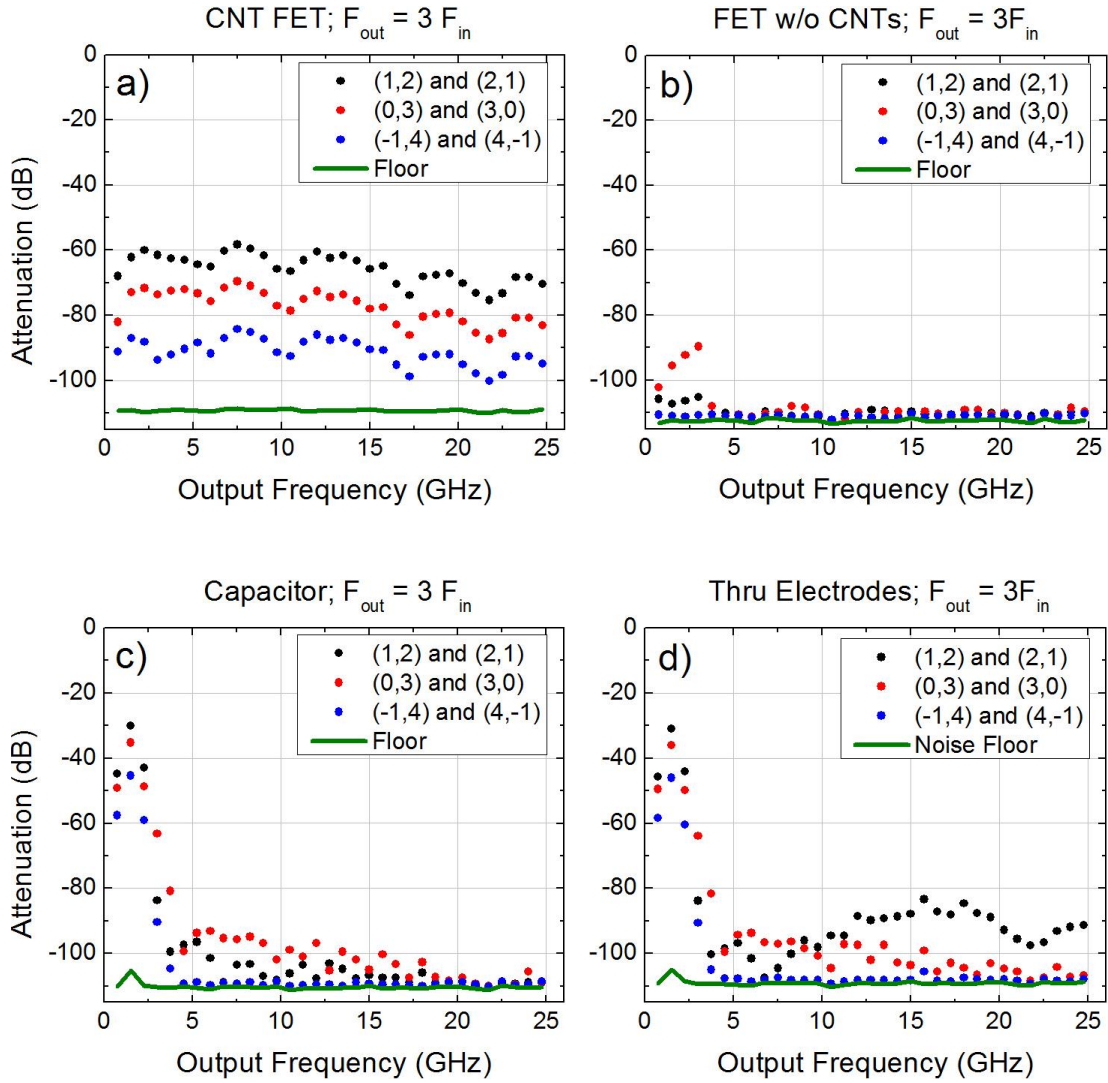
Figure 7.6 Mixing product amplitudes vs. output frequency for a) a CNT FET, b) an FET without CNTs in the channel, c) a parallel plate capacitor, and d) through electrodes used as devices in two-tone mixing. The vertical axis is input power subtracted from the output power. The output spectra were taken at three times the input frequencies.

The CNT FET produces output mixing peak amplitudes spaced similarly over the measured frequency regime, with a gradual decrease in magnitude of around 10 dB from 7 GHz to 25 GHz. The mixing products from the FET electrode geometry without CNTs fall completely below the noise floor by an output frequency of 3 GHz. Both the capacitor and through electrodes show strong mixing products for output frequencies below 3 GHz, which fall quickly near the noise floor at higher frequencies. This indicates that either the mixing due to the equipment cannot

respond at these higher frequencies, or the attenuation of the input signals becomes

large enough that they no longer meet the power threshold where equipment mixing

can occur. Note also that at lower frequencies the attenuation of the input signal

through the CNT FET is much higher (Figure 7.3) than the capacitor and through

electrodes, so the amplitudes resulting in the mixing observed in these controls are

not present in the CNT FET device. These plots show that the mixing output

produced by the CNT FET device above 3 GHz is due to the presence of nanotubes

and not other components. This is well below the frequencies that will be used in the

W regime.

7.2 75 to 110 GHz (W Regime) Measurements with External Mixer

Carbon nanotubes are being considered for high frequency applications

because other electronic materials are either very expensive or cannot operate in high

frequency regimes. Because of this, equipment using conventional electronic

materials to source and analyze high frequency signals substantially increase in cost

with increasing maximum frequency. The signal generators we are using, which are

limited to 40 GHz, cost around 25,000 USD and the spectrum analyzer we are using,

which is limited to 26.5 GHz, costs around 44,000 USD. Moving up a frequency

regime can increase the cost to hundreds of thousands of USD. For this reason, direct

observation of AC signals above the K regime is prohibitively expensive.

To access higher frequency regimes, Agilent produces external harmonic

mixers that are compatible with their spectrum analyzers. These function by receiving

high frequency input signals that are then mixed down with a local oscillator (LO)

produced by the spectrum analyzer to frequencies in the SMA regime that are passed

on to the spectrum analyzer where they can be accurately measured. These inputs are

then corrected for attenuation during the external down mixing and plotted at the

original mixing input frequency. By having a stand-alone external mixer responsible

for a limited frequency regime, the range of a spectrum analyzer can be economically

extended. Each external mixer costs about $4,000. We chose the highest frequency

external mixer available from Agilent, which operates from 75 – 110 GHz, which is

the maximum of the W-band (1 mm). This corresponds to the highest output

frequencies directly observed with CNT FETs.

7.2.1 Experimental Setup

The experimental setup we use in the W regime is shown in Figure 7.7.
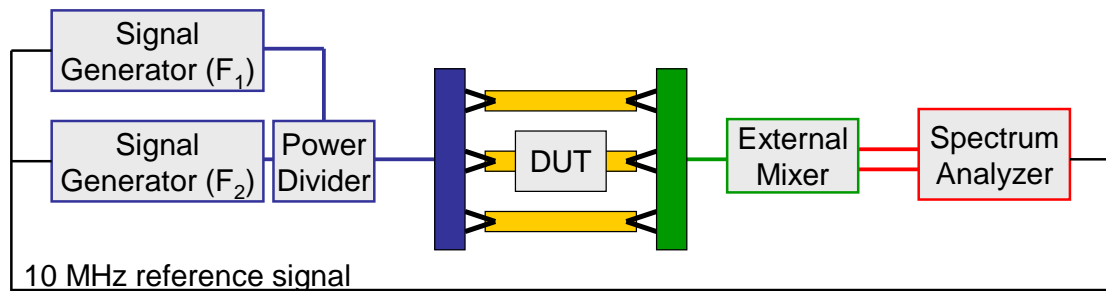
Figure 7.7 Diagram of the experimental setup used to perform mixing experiments in the W regime. The black, red, blue, and green lines correspond to BNC, SMA, K, and W coaxial cables respectively. A 10 MHz reference signal is generated by the spectrum analyzer and input to both signal generators. The outer wings of the probes are grounded through the coaxial cables.

The components used and the frequencies over which they are rated are:
Agilent MXG Analog Signal Generators (N5183A): 100 kHz – 40 GHz
Anritsu Power Divider (K240C): DC – 40 GHz
Picoprobe 40A-GSG-150µm-LP probe: DC – 40 GHz (shown in blue)
Cascade Mictrotech i110-A-GSG-150µm probe: DC – 110 GHz (shown in green)

Agilent 11970 Series Harmonic Mixer (11970W): 75-110 GHz
Agilent ESA-E Series Spectrum Analyzer (E4407B): 9kHz – 26.5 GHz
BCN coaxial cables: DC – 3 GHz (shown in black)
SMA (3.5 mm) coaxial cables: DC – 26.5 GHz (shown in red)
K (2.92 mm) coaxial cables: DC – 46 GHz (shown in blue)
W (1 mm) coaxial cables: DC – 110 GHz (shown in green)

The input of the experimental setup is the same as in the SMA regime in the

previous section. No bias is applied to the gate or the source-drain, so this is a passive

mixing experimental setup. The output probe has been replaced with a W probe,

which connects to a W coaxial cable and then a waveguide adaptor on the external

mixer. The external mixer converts the W regime frequencies down to the SMA

regime. The two SMA cables connecting the external mixer and the spectrum

analyzer correspond to the local oscillator (LO) signal from the spectrum analyzer

(4.15 to 6.09 GHz) and the intermediate frequency (IF) signal from the mixer

carrying the down-converted signal to be measured. The nominal uncertainty of the

spectrum analyzer with this external mixer is ±5.6 dB for the input powers we use.

7.2.2 Two-Tone Mixing in W Regime with 100 kHz Separation

By using a W-band external mixer, we are able to measure output signals in

the 75 – 110 GHz regime. However our signal generators are limited to a maximum

output frequency of 40 GHz, leaving a gap from 40 to 75 GHz in our acquisition

window. Therefore, we are unable to observe the fundamentals of our input

frequencies with this experimental setup. It is possible to observe mixing products at

two times our input frequencies, but that would limit the maximum output frequency

to 80 GHz ($2 \cdot 40$ GHz = 80 GHz). To utilize the entire frequency range of our

external mixer with our equipment and a two-tone input separated by 100 kHz, our

acquisition window will be three times our input signals. This is why the mixing

products centered at three times the input frequency were measured in the SMA

regime in the previous section. The frequency input and output ranges are: $25 \leq F_{in} \leq$

36.67 GHz and $75 \leq F_{out} \leq 110$ GHz.

First, we discuss measurements where the input frequencies span the complete

output range of the external mixer in steps of 500 MHz. Then we observe the mixing

product peak amplitudes as a function of input power at a fixed frequency to see if

they correspond to the expected dependence from our Taylor expansion. Lastly, we

use the CNT mixers in a conventional setup, with a fixed local oscillator frequency

and a variable input frequency. The output range of the external mixer is varied with

the output mixing products. That output is used to characterize CNT FETs with

different gate lengths and channel lengths.

7.2.2.1 Varying the Output Frequency from 75 to 110 GHz

Mixing measurements were performed on a CNT FET ($W = 100$ μm, $L = 10$

μm, $G = 8$ μm) as described above. Output spectra near the minimum and maximum

frequencies of the external mixer ($F_{out} = 75.5$ GHz and 109.5 GHz) are shown in

Figure 7.8. They clearly demonstrate mixing in both windows, indicating that the

carbon nanotubes continue to act as mixers up to 109.5 GHz. The output powers of

the signal generators were fixed at 16 and 15 dBm to provide symmetric input powers

after the 1 dB loss through the extra cable connected to the first signal generator.

There is a reduction in output peak amplitude from 75.5 to 109.5 GHz. This is not a trend across this frequency regime, as will be seen next, but an unusually large difference between these two particular input frequencies. These two spectra were chosen because they represent the maximum and minimum output frequency measured in this sweep.

Figure 7.8 Output spectra at a) 75.5 GHz and b) 109.5 GHz of a CNT FET used to mix two input frequencies separated by 100 kHz. The output frequencies are three times the input frequencies. The vertical axis is the input power (15 dBm) subtracted from the output power.

This measurement was repeated by sweeping through the input frequencies that span the output range of the external mixer by steps of 500 MHz. This corresponds to $F_{1,2} = 25$ to 36.67 GHz $\pm$ 50 kHz. The signal generators and spectrum analyzer were controlled with Labview over GPIB. The spectrum analyzer window was set to 1.2 MHz, the resolution bandwidth was 3 kHz, and the number of points in each sweep was 600. The amplitudes of each peak were computed as the maximum value in a 50 kHz span centered at each peak. The noise floor was computed as the minimum value in the 50 kHz span between the two center peaks.
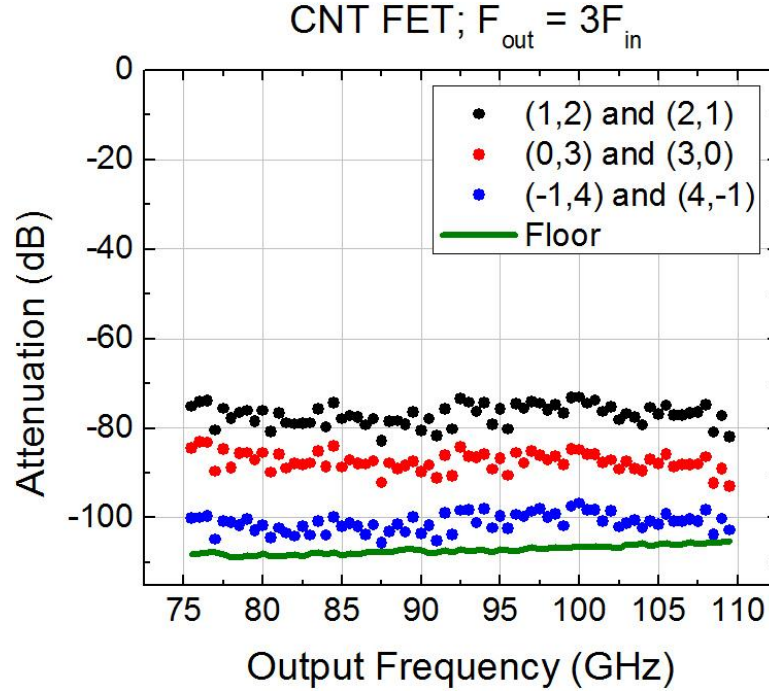
Figure 7.9 Mixing product amplitudes vs. output frequency for a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm) used as devices in two-tone mixing. The vertical axis is input power subtracted from the output power. The output frequency is three times the input frequency.

In Figure 7.9 we show three output peaks corresponding to third and fifth-order mixing. There is no appreciable decrease in output power over the frequency range measured. Point-to-point variations can change by as much as 7 dB. While this falls within the uncertainty of external mixer and spectrum analyzer, it could also be due to standing waves forming at specific frequencies in components of the experimental setup, resulting in higher reflection that reduces the output signal.

To compare these output mixing amplitudes with the attenuation expected from the circuit model in Chapter 5, data from both the SMA and W regimes are combined. Since all six of the measured peaks show similar trends, only the highest amplitude peaks, (1,2) and (2,1), are compared. This data, along with the expected attenuation from the circuit model and a low-pass filter with a corner frequency of

121

230 MHz is shown in Figure 7.10. Both models are scaled to the same low frequency

output power of -40 dBm.
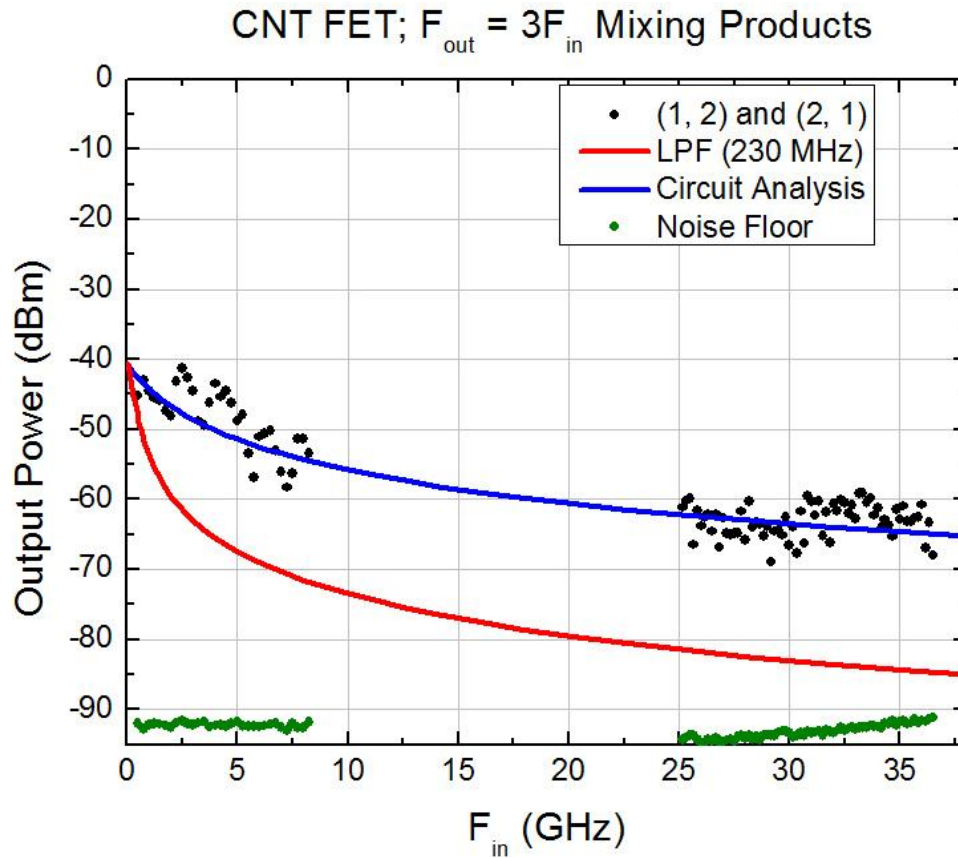
Figure 7.10 Mixing produce amplitudes plotted against two input frequency regimes for a
CNT FET FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm) used as a device in two-tone mixing.
The FET circuit model frequency-dependent output power and a low-pass filter with a corner
frequency of 230 MHz are also plotted, matched to the low frequency output.

As expected, the low-pass filter model undershoots the mixing product output

power from our measurements. The circuit analysis from Chapter 5 provides a much

better approximation. This result is evidence that by placing our input signal on the

gate instead of the drain, the signal attenuation is reduced. The corner frequency from

the resistance of the channel and gate capacitance does provide a rough estimate of

where significant attenuation will begin, but predicting output amplitudes requires a

more careful circuit analysis. Any loss in output power is undesirable, but as was

shown with our experiments, input frequencies beyond F_C do not prevent CNT

response. We already lose 30 dB at $F_{in} = 25$ GHz from our experimental setup, using components rated up to that frequency. Preventing high power losses at frequencies an order of magnitude above that will be nontrivial.

Two quick comments are made about the output signals we detect. The external harmonic mixers can produce their own mixing signals when the local oscillator frequency (LO) from the spectrum analyzer and input radio frequency (RF) from the device are separated by the intermediate frequency (IF) of the down-mixed signal. As a result, false signals can appear in the spectrum analyzer window. To confirm that the spectra seen are real outputs from the device and not false signals from the external mixer, the spectrum analyzer can be put into signal identification mode[100] which eliminates false signals and only displays input signals with uncalibrated amplitudes. Signal identification mode was used at both 75.5 and 109.5 GHz for CNT FET devices, and the output peaks in Figure 7.8 remained unchanged.

We also briefly mention that a false mixing output was once observed on the through electrodes control when the W probe was lowered too far, broke through the electrode pad and penetrated into the quartz substrate. As a result a mixing output signal appeared and faded sporadically over time. The probe tip material is listed as "special" by Cascade and may contain a semiconductor, thus forming a Schottky diode which could explain the production of a mixing signal. When the controls were probed properly, no such anomalous mixing signals were observed.

7.2.2.2 Varying the Input Power

The mixing product coefficients in the Taylor expansion we use to represent our drain current under mixing (EQ 5.16) contain no direct frequency dependence, but the attenuation of input signals from our experimental setup can vary with input frequency, so comparisons of measured data with that approximation are best accomplished at fixed frequencies as a function of input signal amplitudes. Mixing experiments were performed at an output frequency of 75.5 GHz by sweeping the first signal generator's output power (labeled A_1) from -10 to 20 dBm in steps of 0.5 dBm. The second signal generator was held at a fixed 15 dBm output power (labeled A_2). Each captured spectrum was an average of 25 sweeps in the spectrum analyzer. Note that A_1 and A_2 are the powers reported by the signal generators, not the powers reaching the device. From measurements in the SMA regime, a drop of 30 dB is expected for input frequencies near 25 GHz. The spectra at $A_1 = 0$, 10, and 20 dBm for $A_2 = 15$ dBm are shown in Figure 7.11. Vertical lines mark the center of each spectrum.

The asymmetry of the spectra is seen to shift from left to right as the input power of the higher-frequency signal generator is increased. Also, the peaks seem to increase in amplitude as expected. To better analyze the changes with input power, Figure 7.12 shows a plot of the six mixing output powers vs. the first signal generator's output power over the full range of powers used.
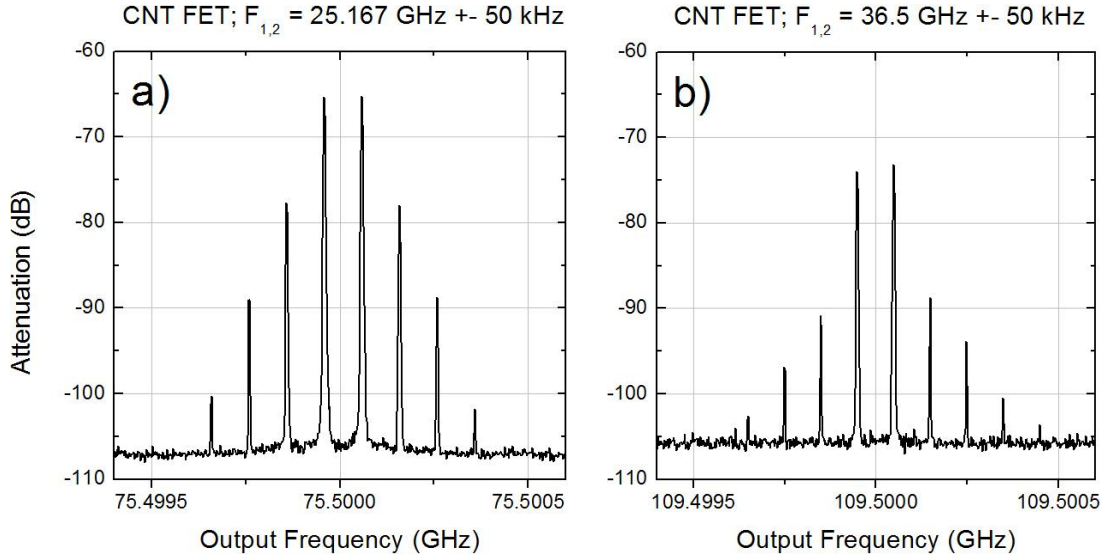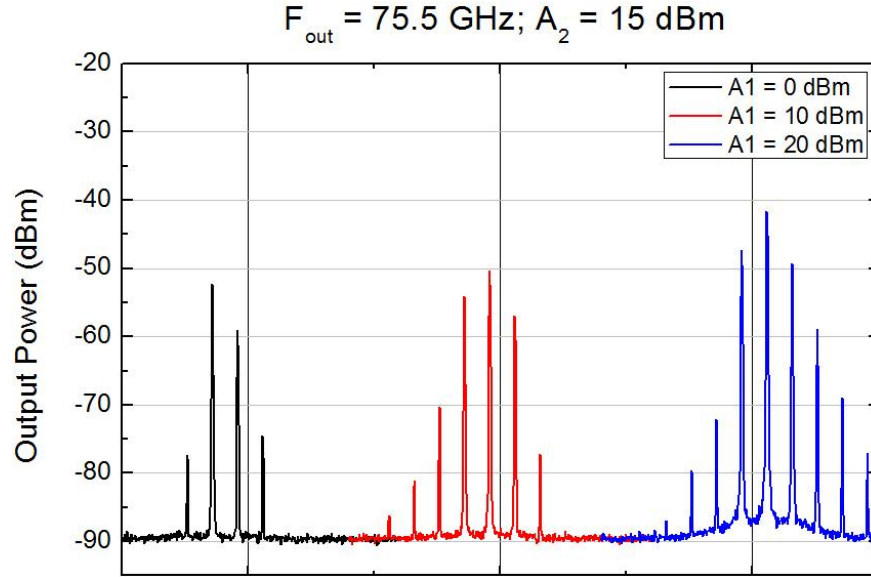
Figure 7.11 Output spectra at 75.5 GHz of a CNT FET used to mix two input frequencies separated by 100 kHz. The output frequencies are three times the input frequencies. One signal generator power was kept fixed ($A_2 = 15$ dBm) while the other was 0 dBm (black), 10 dBm (red), and 20 dBm (blue).

Figure 7.12 Plot of the output power of six mixing products vs. the output power of one signal generator in a two-tone mixing setup performed on a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm). The other signal generator was held at a fixed output power of 15 dBm. The

output frequency was 75.5 GHz, which is three times the input frequencies, which were separated by 100 kHz.

Each peak intersects its complementary peak at the same A_1 value of 16 dBm (green dashed vertical line). This is where the output spectra would be symmetric and is expected since it is 1 dB above where the second signal generator is held at 15 dBm. However, the drop in output power for some of the peaks was not expected. Consider for example the (0, 3) peak. Using only one term in the expansion, this output amplitude should only depend on the output power of the second signal generator, which is fixed, so it should continue as a straight line. By including a second term in the expansion, the fifth-order contribution will have an A_1 dependence as well, so it should increase slightly with A_1, but certainly not decrease. This decrease in (0, 3) indicates that the power reaching the device from the second signal generator is not held fixed but depends on the power from the first signal generator. Since the powers reaching the input of the device are unknown, they are extracted from the third-order harmonics of the input tones and used to predict the mixing peak output power dependence on input power. The reason why the signal power from the second signal generator reaching the device did not stay constant and the method of recalibration are presented in Appendix F.

The mixing peak amplitudes could be directly analyzed at low input powers where the device input powers are as expected, but fewer peaks are produced at those input powers. To consider the six main peaks observed, the powers produced by the signal generators are converted to the powers incident upon the device. To summarize the conversion method, when ignoring the fifth-order and higher expansion terms, the third-order harmonics of the two fundamentals, (0, 3) and (3, 0), do not depend on the

input power of the other tone; therefore their outputs should primarily depend only on one signal generator. The (3, 0) data are used to extract the signal power at the input of the device from signal generator #1 and the (0, 3) data are used to extract the same from signal generator #2. After the input powers reaching the CNT FET are known, they are used with our Taylor expansion of drain current under mixing to produce the expected output amplitude dependence on input power for six mixing products, which is compared with the measured data.

Considering only one term in each peak's expansion, the output power as a function of the input power for all six peaks are listed in EQ 7.2, where A_{out} is the output power in dBm, A_{in} is the device input power in dBm, and β_n is given by EQ 7.3.

$$A_{out}\big|_{(1,2)} \approx 10Log(\beta_3) + 20Log\left(\frac{3}{4}\right) + A_{in}1 + 2A_{in}2$$

$$A_{out}\big|_{(2,1)} \approx 10Log(\beta_3) + 20Log\left(\frac{3}{4}\right) + 2A_{in}1 + A_{in}2$$

$$A_{out}\big|_{(0,3)} \approx 10Log(\beta_3) + 20Log\left(\frac{1}{4}\right) + 3A_{in}2$$

$$A_{out}\big|_{(3,0)} \approx 10Log(\beta_3) + 20Log\left(\frac{1}{4}\right) + 3A_{in}1$$

$$A_{out}\big|_{(-1,4)} \approx 10Log(\beta_5) + 20Log\left(\frac{5}{16}\right) + A_{in}1 + 4A_{in}2$$

$$A_{out}\big|_{(4,-1)} \approx 10Log(\beta_5) + 20Log\left(\frac{5}{16}\right) + 4A_{in}1 + A_{in}2 \qquad \text{EQ 7.2}$$

$$\beta_n = \alpha_n^2 R^4 \qquad\qquad\qquad \alpha_n = \frac{\partial^{n-1}G_D}{\partial V_{gs}^{n-1}}\frac{1}{n!} \qquad \text{EQ 7.3}$$

By matching the expected output to the (0, 3) and (3, 0) measured data, the beta parameters were $\beta_3 = 0.537$ mW and $\beta_5 = 20.0$ mW. These values

give: $\dfrac{\partial^2 G_D}{\partial V_{gs}^2} = 55.6\ \mu S\ /\ V^2$ and $\dfrac{\partial^4 G_D}{\partial V_{gs}^4} = 6.78\ \mu S\ /\ V^4$. Figure 7.13 displays the

measured data for each mixing product plotted against the expected product behavior

using EQ 7.2. The agreement for the (0, 3) and (3, 0) plots is nearly perfect. This may

seem inevitable since they were used to predict the input amplitudes, but they were

not transposed point-by-point. Simple functions fit their behavior very well. The other

four mixing product projections follow the same trends as the data, falling short at

large signal generator powers. Including more terms in the expansion would raise the

projected output power in each plot. These plots confirm that the mixing behavior we

observe in our high frequency two-tone mixing experiments follow the input signal

amplitudes expected from our Taylor expansion of drain current. The lesson from

these measurements is that at low input powers, the powers reaching the device are

directly related to the powers generated by the signal generators. At larger input

powers, even though unexpected power-dependent attenuation occurs in the system,

the measured mixing product amplitudes follow the device input power dependencies
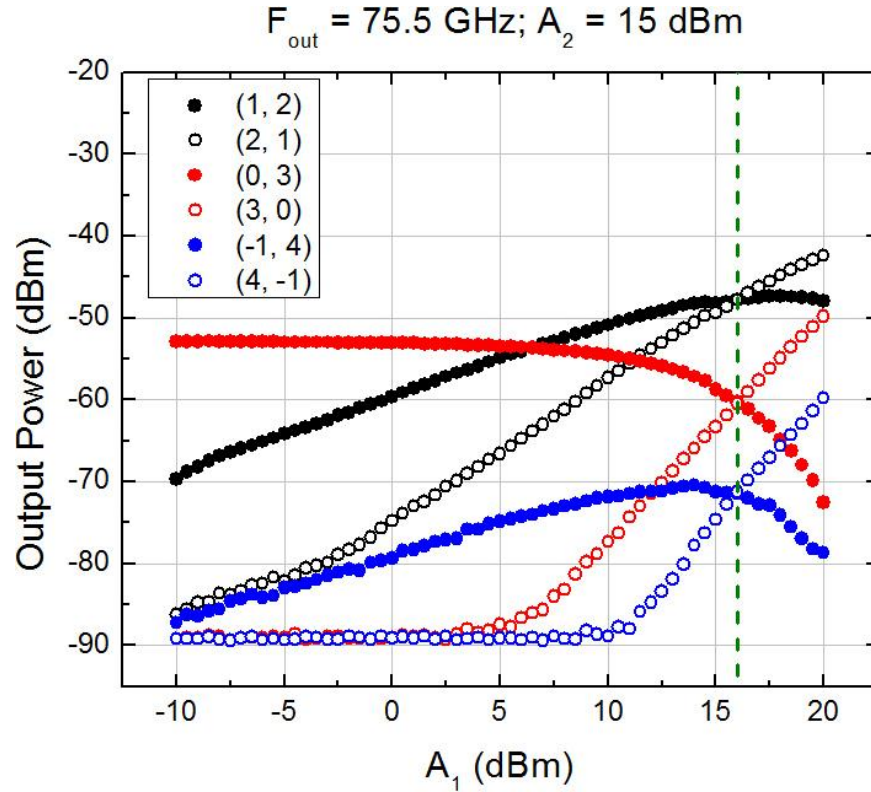
derived from the Taylor expansion.
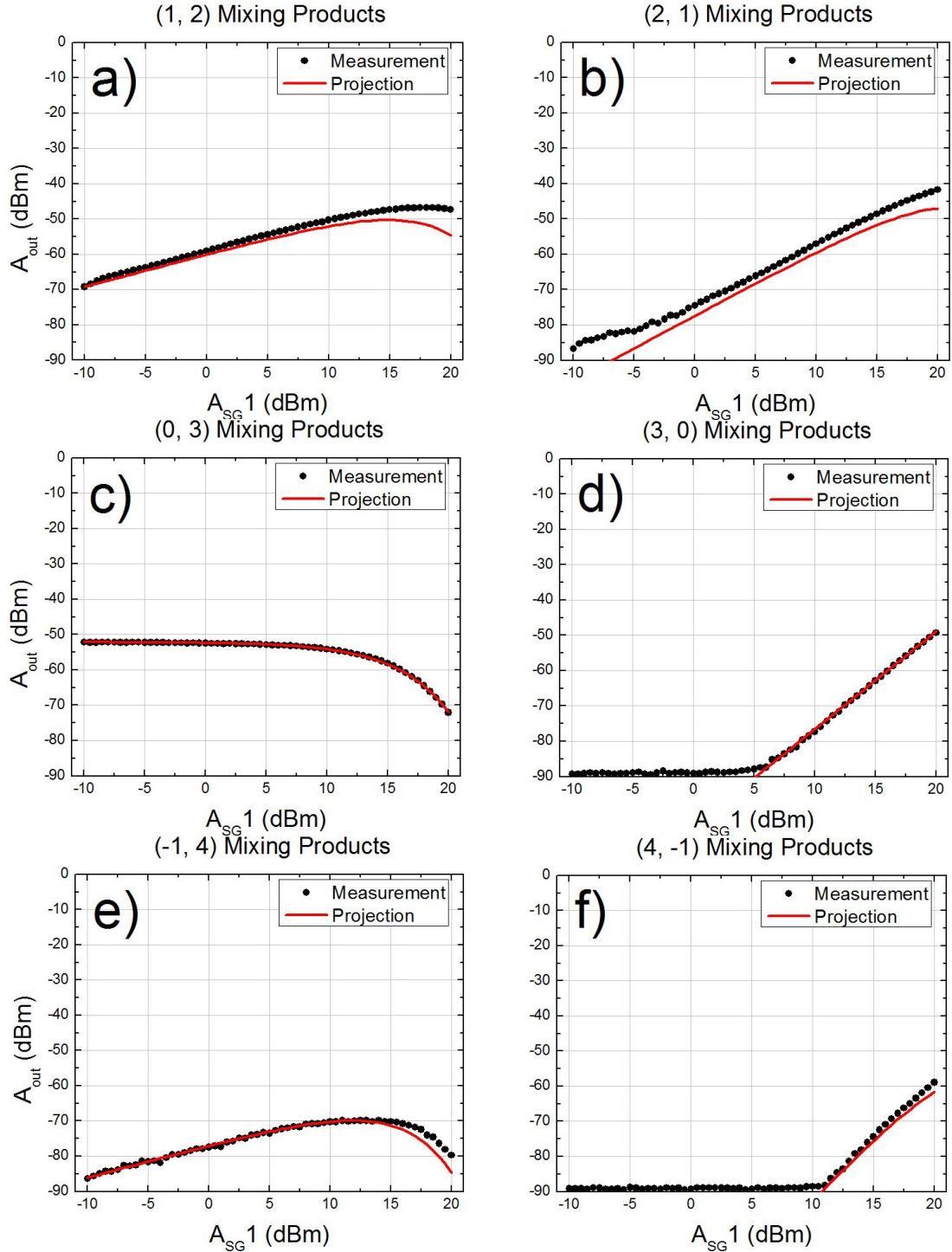
Figure 7.13 Plots of the output power of six mixing product peaks vs. the output power of one signal generator in a two-tone mixing setup performed on a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm). The black dots are the measurements taken, and the red lines are the expected mixing product amplitudes based on a single expansion term per peak. The other signal generator was held at a fixed output power of 15 dBm. The output frequency was 75.5 GHz + 300 kHz, which is three times the input frequency of the first signal generator.

7.2.2.3 Examining the (1, 2) to (3, 0) Amplitude Difference

An additional confirmation cross-check for the output amplitudes is to compare the amplitudes of the (1, 2) and (2, 1) products with the (0, 3) and (3, 0) peaks for equal inputs. An example of these amplitudes is shown in Figure 7.14. Since all four peaks are 3rd order products, they have the same coefficients in front of the first terms in their expansion and should maintain the same ratio independent of input frequency and power.
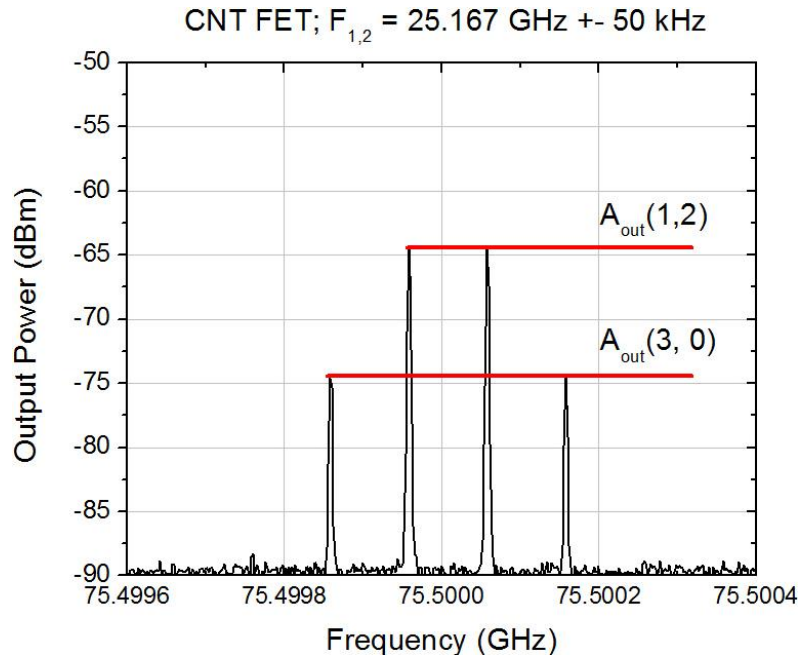
Figure 7.14 Output spectra at 75.5 GHz of a CNT FET used to mix two input frequencies separated by 100 kHz. The two input amplitudes were equal, producing the symmetric spectrum. The (1,2) and (3,0) mixing peak amplitudes are shown in red. The output frequencies are three times the input frequencies.

For $P_{in}1 = P_{in}2$,

$$\frac{P_{out}\big|_{(2,1)}}{P_{out}\big|_{(3,0)}} \approx \frac{\beta_3 \left(\frac{3}{4}\right)^2 (P_{in}1)^3}{\beta_3 \left(\frac{1}{4}\right)^2 (P_{in}1)^3} = 3^2 = 9 \qquad\qquad \text{EQ 7.4}$$

A power ratio of 9 corresponds to 9.54 dB, so to first order approximation, these peaks should always have an amplitude difference of 9.54 dB. If the expansion includes more terms and the input amplitudes are high enough, this amplitude difference can decrease, shown in the two-term expansion case of EQ 7.5 – 8.

$$I_d\left(\delta V\right)\Big|_{(1,2)} \approx \alpha_3\frac{3}{4}\left(V\right)^3 + \alpha_5\frac{25}{8}\left(V\right)^5 = \alpha_5 V^3\left[\frac{3}{4}\frac{\alpha_3}{\alpha_5} + \frac{25}{8}\left(V\right)^2\right]$$

$$I_d\left(\delta V\right)\Big|_{(0,3)} \approx \alpha_3\frac{1}{4}\left(V\right)^3 + \alpha_5\frac{25}{16}\left(V\right)^5 = \alpha_5 V^3\left[\frac{1}{4}\frac{\alpha_3}{\alpha_5} + \frac{25}{16}\left(V\right)^2\right] \qquad \text{EQ 7.5}$$

$$\frac{P_{out(1,2)}}{P_{out(0,3)}} = \frac{\left(\dfrac{3}{4}\dfrac{\alpha_3}{\alpha_5} + \dfrac{25}{8}V^2\right)^2}{\left(\dfrac{1}{4}\dfrac{\alpha_3}{\alpha_5} + \dfrac{25}{16}V^2\right)^2} \qquad \text{EQ 7.6}$$

$$\text{For } \frac{\alpha_3}{\alpha_5} >> V^2: \qquad \frac{P_{out(1,2)}}{P_{out(0,3)}} = \frac{\left(\dfrac{3}{4}\dfrac{\alpha_3}{\alpha_5}\right)^2}{\left(\dfrac{1}{4}\dfrac{\alpha_3}{\alpha_5}\right)^2} = 9 \qquad \text{EQ 7.7}$$

$$\text{For } \frac{\alpha_3}{\alpha_5} << V^2: \qquad \frac{P_{out(1,2)}}{P_{out(0,3)}} = \frac{\left(\dfrac{25}{8}V^2\right)^2}{\left(\dfrac{25}{16}V^2\right)^2} = 4 \qquad \text{EQ 7.8}$$

From the derivatives of G_D extracted previously, $\dfrac{\alpha_3}{\alpha_5} = 164$ for our measured device. That would require input voltages on the order of 13V or higher to see the (1, 2) and (3, 0) peaks come closer together, which is much larger than we ever approach. We are therefore in the regime when only the first term in the expansion should significantly contribute the output product height, and we expect a constant 9.54 dB amplitude difference in our measurements.

Symmetric spectra at 75.5 GHz and 109.5 GHz were captured for twelve different CNT FET device geometries. The devices measured covered all of the different FET geometries fabricated on one chip, which are mentioned in Chapter 2. The particular channel widths, channel lengths, and gate lengths for each device are given in Table 7.1

Device	1	2	3	4	5	6	7	8	9	10	11	12
W	100	100	100	100	100	100	100	100	100	100	50	25
L	10	10	10	10	5	10	25	50	75	10	10	10
G	5	8	10	12	3	8	21	46	71	8	8	8

Table 7.1 Channel widths, channel lengths, and gate lengths in micrometers for twelve CNT FETs that were used for two-tone high frequency mixing measurements

The difference between the (1, 2) and (3, 0) peak amplitudes for all 12 devices are plotted in Figure 7.15. All the points fall within the maximum uncertainty of the equipment (shown in green) of the expected value. This shows that the essential nanotube nonlinearity that generates these mixing peaks continues to operate up to 110 GHz.
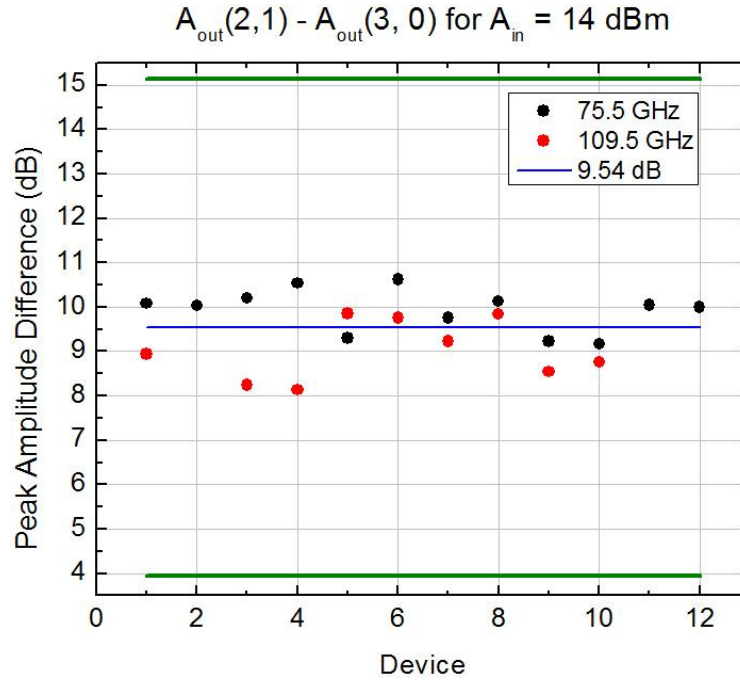
Figure 7.15 Output amplitude difference between the (2,1) and (3,0) mixing products when the input powers are equal. Twelve different CNT FET devices with different electrode geometries were measured. The expected amplitude difference of 9.54 dB should be independent of frequency and device type. The experimental uncertainty bounds are displayed as green lines.

7.2.3 Heterodyne Detection at 37 GHz LO Operation

The two-tone mixing experiments performed in the last section had the two input frequencies separated by 100 kHz so that many mixing peaks could be observed in a small output window (1.2 MHz). For real-world applications, a mixer is typically used for heterodyne signal detection. This is accomplished by having one input, the local oscillator (LO) at the fixed frequency and the second input signal varied over a specified frequency range. The resulting output signal is selected to correspond to one particular mixing product. This arrangement is now used with our CNT FETs acting as mixers to take a RF input signal from the K frequency regime (DC – 40 GHz) and

mix it up to the W regime that we can observe with our external mixer experimental setup (75 – 110 GHz).

Our first signal generator produces our LO signal at a fixed frequency and power of 37 GHz and 18 dBm, respectively. Our second signal generator produces our RF signal from 1 GHz to 36 GHz at a fixed power of 10 dBm. The output mixing product of interest is (2, 1). The advantage of using this arrangement is that magnitude of the fixed LO signal is much larger than the varied RF signal, so the frequency dependent attenuation of the RF signal will have a minimized effect on the output amplitude. Since the LO power is 7 dB greater than the RF power (including the 1 dB loss from extra cable), the contribution to the output power of the mixing product from the LO signal is 14 dB greater than the contribution from RF signal, as shown in EQ 7.9.

$$A_{out}\big|_{(2,1)} \approx 10Log(\beta_3) + 20Log\left(\frac{3}{4}\right) + 2A_{in}LO + A_{in}IR \qquad\qquad \text{EQ 7.9}$$

Several different devices were measured in this configuration. The input frequency of the RF signal was swept from 1.25 GHz to 35.75 GHz by steps of 250 MHz. The spectra were captured in a 120 kHz window, resolution bandwidth of 3 kHz, and the peak amplitude extracted as the maximum value in that window. The signal generators and spectrum analyzer were controlled with Labview over GPIB.

The results for the three control devices mentioned earlier are plotted in Figure 7.16. They are through electrodes, a parallel plate capacitor, and a 10 μm channel length, 8 μm gate length FET geometry without CNTs in the channel. No peaks were visible in the output frequency window, so the output signals for each form the noise floor, indicating that if any unintended mixing does occur in this

frequency regime without a CNT FET as the DUT, it is not detectable with our

equipment. This suggests that any mixing signals observed in the measurement of

CNT FETs is attributed to the presence of CNTs.
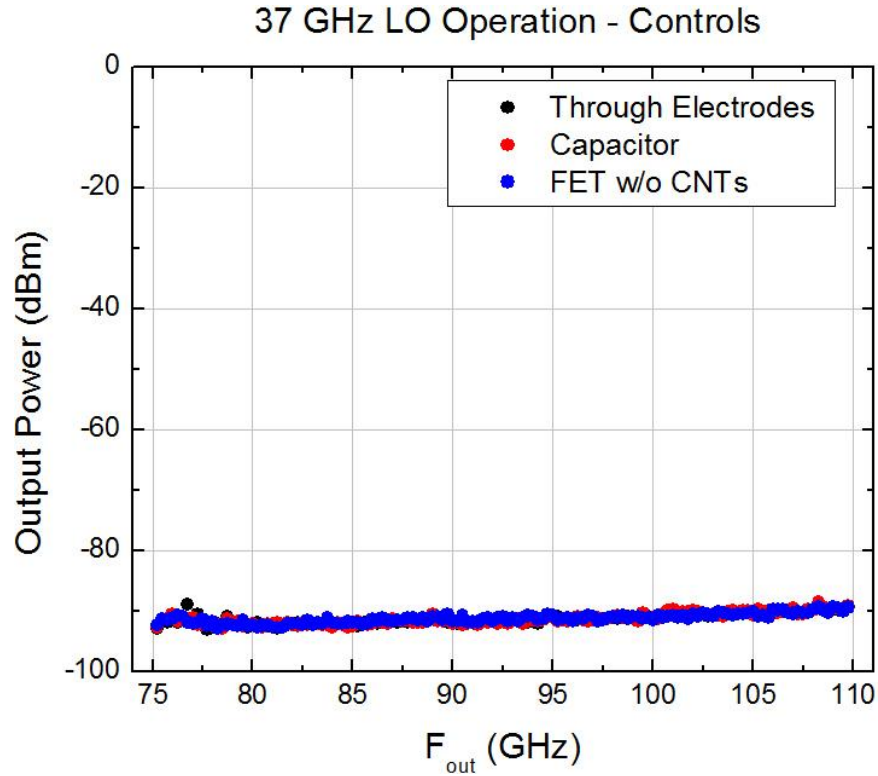
Figure 7.16 Output power of the mixing product from the 37 GHz LO mixing measurements for the three control devices. The LO signal is fixed at 37 GHz and 18 dBm while the RF signal is swept from 1.25 to 35.75 GHz at a power of 10 dBm.

Also measured were CNT FETs with channel lengths of 10 μm but with

different gate lengths (5, 10, 15 μm). The results of those measurements are shown in

Figure 7.17. For devices that have gates that do not entirely span the channel, the

capacitance of the gate to the CNTs is expected to be greater than the capacitance of

the gate to the source and drain. Increasing the gate length increases all three

capacitances similarly, but as the gate begins to overlap the source and drain

electrodes, the electrode capacitance grows considerably while the gate-CNT

capacitance remains constant. This increased gate-source capacitance provides a low

resistance path to ground that will reduce the amount of the signal passing through the

channel of the device. Figure 7.17 shows this increasing loss of signal as the gate

length is increased.
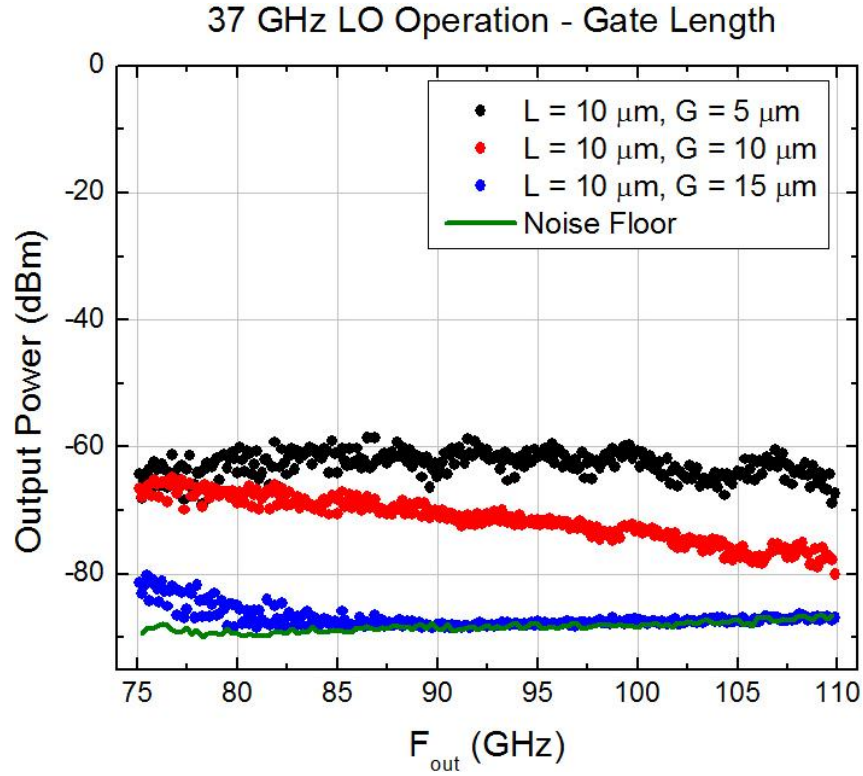
Figure 7.17 Output power of the mixing product from the 37 GHz LO mixing measurements
for CNT FETs with channel lengths of 10 μm but different gate lengths. The LO signal is
fixed at 37 GHz and 18 dBm while the RF signal is swept from 1.25 to 35.75 GHz at a power
of 10 dBm.

By performing the same circuit analysis as in Chapter 5, the extra attenuation

due to the increased gate-source and gate-drain capacitances from gate overlap can be

predicted. Those predictions with no overlap, 1 μm of overlap, and 5 μm of overlap

are shown in Figure 7.18. Increased attenuation with increasing gate overlap is

shown. However, the slopes of all three curves are predicted to be similar for the

input frequency range of 25 to 37 GHz, while the data appears to show an increase in

slope with increasing gate overlap. Acquiring a more accurate representation of the

output mixing peak amplitudes requires an analysis beyond lumped elements,

representing the CNT as a transmission line.
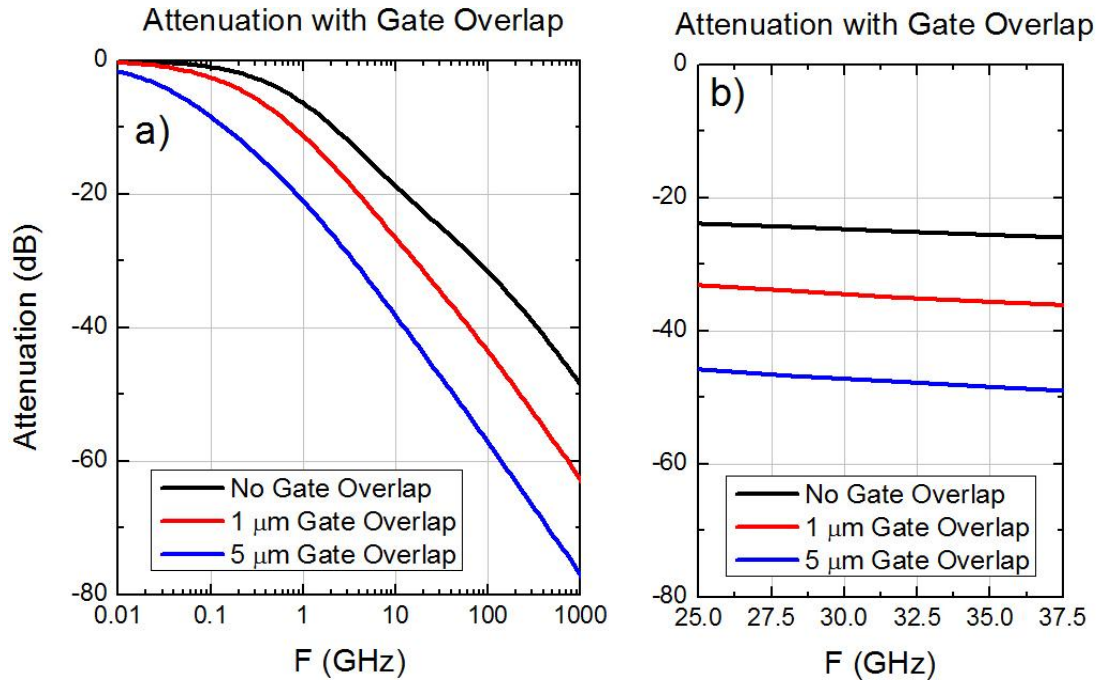
Figure 7.18 Predicted attenuation from the CNT FET circuit model in Chapter 5 for three different amounts of gate overlap. a) is on a logarithmic frequency scale over five orders of magnitude and b) is on a linear scale over the HF input frequency range, 25 to 37.5 GHz.

The last devices compared with this measurement setup are CNT FETs with

different channel lengths. The output data for a device with a 5 μm channel length

and a 75 μm channel length are plotted in Figure 7.19. For both devices, the gate

length is shorter than the channel length. The results for both devices are nearly

identical, which is surprising considering that the channel impedance of the $L = 75$

μm device is 40 times greater than the $L = 5$ μm device. These results show that the

transit time cutoff, present when the input signal is placed on the source and the

output is taken at the drain, does not apply to this measurement setup. Using the

ballistic limit of the Fermi velocity, the maximum transit length of charges at our

maximum input frequency of 37 GHz is 3.5 μm. This only corresponds to 5% of the

75 μm channel length. This suggests that only a few microns of the nanotube length near the drain are active at such high frequencies; charges in the rest of the nanotube length do not contribute to the output current. If charges needed to span the entire device channel, no output would be observed in the long channel length device.
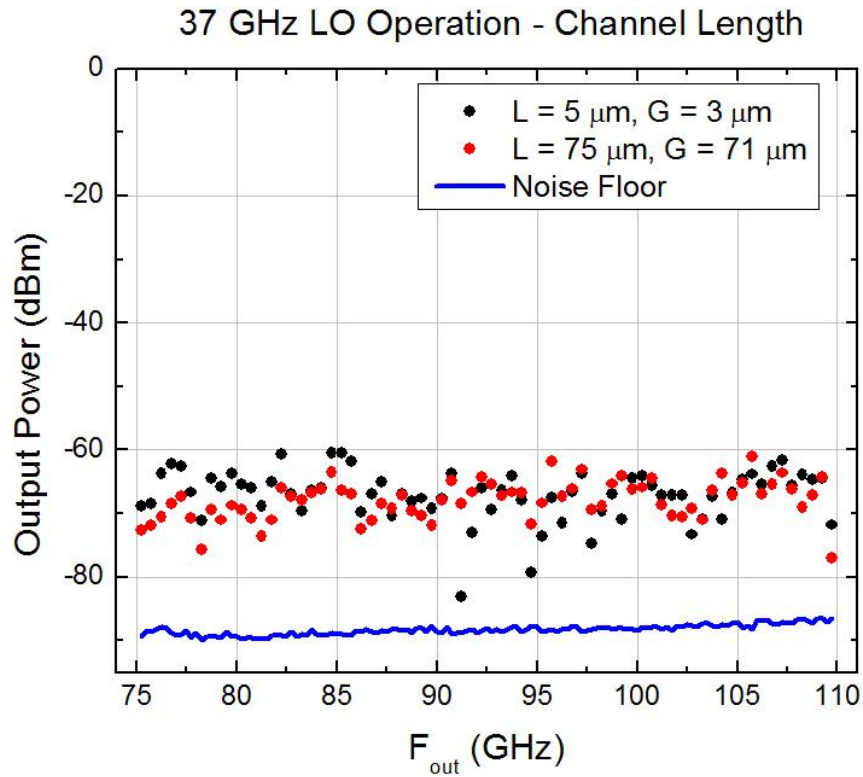
Figure 7.19 Output power of the mixing product from the 37 GHz LO mixing measurements for CNT FETs with different channel lengths. The LO signal is fixed at 37 GHz and 18 dBm while the RF signal is swept from 1.25 to 35.75 GHz at a power of 10 dBm.

Output detection beyond the transit time cutoff from the Fermi velocity could be explained with plasmon excitations, which are expected to travel faster than non-interacting charges. If the plasmon velocity was four times the Fermi velocity, plasmons could span the 5 μm channel at such high input frequencies but not the 75 μm channel. The plasmon velocity would need to be 21 times the Fermi velocity for plasmons originating at the source to the reach the drain in one period. The more likely explanation is that by placing the input signal on the gate, charge motion

responsible for mixing occurs at both ends of the channel. These devices demonstrate CNT non-linear operation at the highest frequency directly observed to date and at channel lengths 100 times larger the submicron channel lengths previously assumed necessary for GHz operation.[77-79, 83, 85]

7.3 Summary

In this chapter, we have reviewed our results from two-tone mixing experiments in two frequency regimes. Measurements from 1 GHz to 26.5 GHz (SMA regime) showed that at low frequencies output mixing signals are visible from control devices, demonstrating unwanted mixing from the equipment used in the experimental setup. These third-order output signals die out around $F_{out} = 5$ GHz in control devices while they remain in the CNT FETs, confirming that the CNTs are responsible for the mixing behavior seen above this frequency.

In the high frequency regime, the mixing product outputs are found to only slightly decrease in amplitude from 75 to 110 GHz. The mixing product amplitudes are compared with their expected values from our Taylor expansion of drain current by sweeping the input power while holding the input frequency fixed. Some unexpected output behavior is seen and attributed to input power limitations of the power divider used. Recalibration of the input powers reaching the device, extracted from the third harmonic products of the two input tones, allows us to project the expected output amplitudes of other peaks. Results closely matching the data show our results to be consistent with the Taylor expansion form of mixing we use.

Finally, sweeps of the output frequency range are made in a practical mixing configuration using a fixed 37 GHz LO input to compare different types of devices. The controls did not produce any measurable mixing products in these measurements while the CNT FETs did. In devices with gates overlapping the source and drain electrodes, the output signal quickly decreases with frequency, as expected with increased gate-source capacitance and our circuit model. No strong dependence on channel length was observed, with mixing signals from a 75 μm channel length device of similar magnitude to devices with 10 and 5 μm channel lengths, indicating that our measurement technique overcomes the transit time cutoff frequency. These experiments clearly show CNT mixing behavior up to 110 GHz, the highest output frequency directly observed to date, with no indication of the output dropping below the noise floor at even higher frequencies.

Chapter 8: Summary and Conclusions

In this dissertation, field-effect transistors using aligned arrays of carbon nanotubes were used as passive mixers to convert input frequencies to output frequencies as high as 110 GHz, the highest CNT FET output frequencies observed to date. After describing the design and fabrication of the devices, the role of defects in the dielectric layer acting as charge traps was investigated by observing how the drain current approached an equilibrium value in response to non-zero gate pulses when held at a constant source-drain bias. These currents were observed to follow a power law with time until nearly reaching equilibrium. By observing the behavior of charge traps as a function of the gate voltage magnitude and pulse duration, a measurement method that minimizes the effects of traps was developed. By using short measurement pulses, the number of traps filled during each pulse was minimized. A default trap state occupation was set in between each measurement pulse by applying an alternating decreasing voltage waveform to the gate, similar to a degaussing method used on cathode ray tubes. This measurement method was shown to reduce hysteresis in transfer curves beyond other published measurement waveforms. The time-independent Preisach hysteresis model was used to derive this waveform and to predict the drain current output for the waveforms considered, matching the measured data well. For passive high frequency measurements, only small input voltages centered at $V_{gs} = 0$ were used, so the presence of charge traps was not detrimental. For DC measurements, our method reduced the hysteresis in transfer curves to the level of measurement noise, with a standard transfer curve taking less than one minutes to acquire.

We then presented a method to successfully remove metallic CNTs from as-grown aligned arrays on quartz, increasing the on/off current ratio to 10^3 and higher. The presence of metallic CNTs in the channel prevented the FET from being gated off, adding a constant channel current that does not contribute to device operation whenever the device is biased. Our high frequency mixing experiments were performed passively, without any bias, so this constant current under bias did not apply to our measurements. For active devices, this would be a necessary step to avoid unwanted power losses. Since increasing the on/off ratio also reduces the on-state current, the devices we used for our high frequency mixing experiments used as-grown nanotube arrays to minimize the device input impedance and maximize our output signal magnitudes.

The last three chapters focused on high frequency CNT measurements. First, the work by previous research groups was presented. The experiments most similar to ours used CNT FETs as passive mixers by placing input signals on the source and measuring outputs at the drain. Two frequency cutoffs were expected in such a measurement setup. First, the device resembled a low-pass filter with an associated RC corner frequency, above which significant attenuation would occur. The second cutoff frequency corresponded to the transit time necessary for charges to span the channel. This transit time cutoff frequency was a hard cutoff, above which no output signal should be detected. Because of these cutoffs, submicron channel lengths were used and only DC or low frequency output signals were measured.

Our experimental method placed the input signal on the gate instead of the drain, even though our CNT FETs were used passively. This changed the circuit

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model so that it no longer directly resembled a low-pass filter and the output attenuation should be decreased. This measurement technique also overcame the transit time cutoff frequency because signals would be induced at the drain electrode without needing to span the channel. Instead of merely measuring the DC or low frequency mixing output signals, high frequency outputs were directly measured using an external mixer and a spectrum analyzer with a low noise floor (-90 dBm).

After introducing our experimental setup, generic frequency mixing was introduced. We presented an approximation of the drain current of a CNT FET as a Taylor expansion of a small input voltage. A single-tone mixing experiment was performed to test the validity of this expansion. The DC mixing current was measured and compared with the expected output derived from the derivative of conductance with respect to gate voltage. The two were shown to match well in the regions where the approximation was valid.

We then performed two-tone mixing experiments on CNT FETs and control devices to eliminate any mixing contributions from the experimental setup. By using an external harmonic mixer to convert our device output signals to frequencies that our spectrum analyzer could detect, our CNT FETs demonstrated generated output frequencies as high as 110 GHz. Up to 11th order mixing products were observed in this regime. The difference between two third-order mixing product amplitudes was found to be within the measurement uncertainty of the difference expected from our drain current approximation, and all the mixing product amplitudes were found to depend on input power as expected.

The attenuation of our output signals followed the frequency dependence expected from our circuit model. Power loss is never an intended device feature, but certain levels of power loss may be acceptable for many applications. In telecommunication systems, for example, a link budget accounts for all the gains and losses from a transmitter to a receiver. Each component does not need to provide gain itself; the total losses need merely fall within a range. Our two-tone W regime mixing experiments are an example of high frequency function in spite of large power loss. Input signals of 36.5 GHz were mixed up to 109.5 GHz, experiencing a total power loss near 70 dB from signal generator output power to device output power. Then the external mixer down-mixed the produced signals to below 6 GHz where they were at a power level where they could still be measured. Amplification in that frequency regime is a much easier task. By mixing passively, no power was wasted in powering the CNT devices themselves.

The output signals from devices with different channel lengths were compared. If measured with the input signal on the source, the transit time cutoff of the long channel length device (75 μm) should have prevented any signal from being detected. With our measurement technique, the output signals from both devices were nearly identical, possibly indicating that only a few microns of the device length near the drain are active at high frequencies. This shows that high frequency performance can be achieved in CNT devices without slow and costly submicron fabrication methods like electron beam lithography. Standard photolithography and even shadow mask deposition can produce devices of this scale.

Further experiments could clarify these results. It would first be beneficial to fill in the gap (25 to 75 GHz) of our output frequency window with additional external mixers. This would provide continuous data that could be better compared with circuit models. We would also like to access even higher output frequency regimes (> 110 GHz) to see if other limitations begin to appear. To verify the mechanism of signal propagation through the device, electrode geometries with long channel lengths like those in Figure 8.1 would be measured. If only a few microns of channel length near the drain are active at high input frequencies, devices a), b), and c) should have similar output signals, even though the gate-CNT capacitance is changing. In devices e) and f), the gate-drain capacitance will be very small and charge motion should only occur in CNTs themselves under the gate. The transit time cutoff should apply in such a case, with a transit length equal to the ungated length of CNTs from the gate to the drain. If HF output signals were detected in such devices, different mechanisms of mixing/and or signal propagation would be necessary.
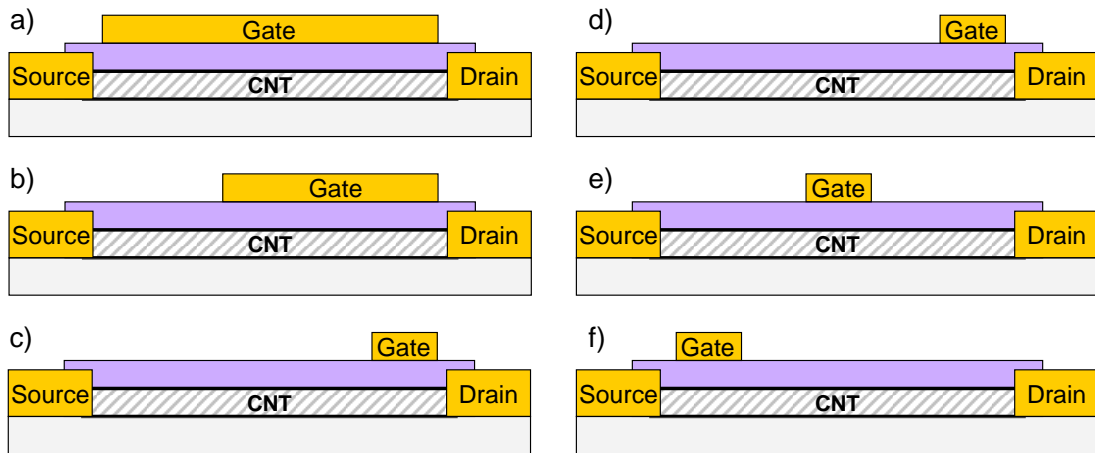
Figure 8.1 Electrode geometries for a long channel length device that could indicate how an input signal on the gate induces a mixing current in the CNT channel.

We have increased the observable output frequency regime for carbon nanotube field-effect transistors. Even uncommonly large devices (channel lengths of

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75 μm) continued to operate up to 110 GHz without indication that performance was beginning to fail. By mixing up input frequencies in the SMA regime, we have demonstrated an economical way of producing clean high frequency output signals in an expensive frequency regime. Passive operation eliminates the need for a local power supply, allowing for incorporation into small and portable circuits such as radio frequency identification (RFID) tags. Our devices could be made wafer scale by standard photolithography methods, and the attenuation of the generated output frequencies could be improved with more carefully designed electrode geometries. Output current and power could also be easily increased by using wider channels (more CNTs).

Appendix A: Fabrication Procedure for Aligned CNT FETs on Si/SiO$_2$ Substrate

These instructions produce a top local gate, bottom global gate aligned CNT FET on a silicon/silicon dioxide substrate. The typical device geometries are: silicon substrate with 500 nm thermal oxide, aligned CNT channel, 50 nm Ti/Au source-drain, 75 nm Al$_2$O$_3$ dielectric, 100 nm Ti/Au gate. If the metallic CNTs are to be removed by joule heating, that should be done after patterning the CNTs and before depositing the Al$_2$O$_3$ dielectric. Two substrates are necessary, the quartz CNT growth substrate and the silicon/silicon dioxide device substrate.

Quartz CNT Growth Substrate

Purchase Wafers:
3" diameter, single crystal quartz wafers, 0.5mm thick, ST-cut 42°45', single side polished (SSP), Hoffman Materials

Dicing:
CNTs align themselves perpendicular to the wafer flat, so either mark the back side of the wafer with a diamond scribe to indicate the alignment direction or dice into shapes which allow one to identify the alignment direction.
Cover wafers with photoresist to protect surface during dicing. Many photoresists would do.
    spin HMDS at 4000 rpm for 60 sec
    spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
    bake on hotplate at 90 C for 60 sec
    dice with diamond saw, both sides of wafers covered by tape
    remove tape
    soak and sonicate in Acetone for 10 minutes
    rinse with acetone, methanol, and isopropanol (IPA)
    blow dry with nitrogen

Annealing: necessary for CNT alignment. To prevent cracking, heating and cooling rates should be < 10 C/min.
    heat quartz pieces in open tube furnace (air) to 900 C
    hold for 12 hours
    cool to room temperature

Catalyst Deposition: Ferritin - for medium density and partial alignment over whole sample surface.

    dilute ferritin solution with DI to 1 mg/mL

    soak quartz pieces in solution for 20 min in refrigerator, 3 C

    rinse with DI

    blow dry with nitrogen

    keep ferritin refrigerated - do not let freeze

CVD: Hydrogen Anneal - to clean the quartz surface of residual photoresist.[101] To prevent cracking, heating and cooling rates should be < 10 C/min.

We use a three-zone tube furnace from Lindberg Blue, 2 in quartz tube, mass flow controllers, and quartz boats from Glass Tech. All three zones are set to the same temperature.

    insert samples in boats into the center of the tube

    flush with 200 sccm argon for five minutes

    flow 1700 sccm argon and 1900 sccm hydrogen

    heat to 400 C

    hold temperature and flow rates for 1 hour

    cool to room temperature

    stop hydrogen flow

    stop argon flow after 5 minutes

    remove samples

CVD: CNT Growth

Many papers report using different gases: methane, ethylene, methanol and ethanol bubblers, water bubblers, etc. No significant difference in density was found from these other sources. To prevent cracking, heating and cooling rates should be < 10 C/min.

    insert samples in boats into the center of the tube

    heat in air to 700 C - to burn away the organics in ferritin

    hold for 10 min (oxidizing step)

    cool to room temperature

    seal tube ends

    flush with 1000 sccm argon, hydrogen, and methane for 5 min

    stop argon and methane flow

    set hydrogen flow to 250 sccm

    heat to 925 C

    hold for 10 min (reducing step)

    introduce methane flow 1000 sccm

    hold for 20 min

    stop methane flow

    cool to room temperature

    stop hydrogen flow

    flush with 1000 sccm argon for 5 min

    remove samples

Remove CNTs from Substrate: Uses single sided thermal tape (120 C transistion temperature, Revalpha 3195MS, Nitto Denko)

    e-beam evaporate 100 nm Au over whole quartz piece
    cut a piece of thermal tape with scissors
    remove plastic coating from adhesive side
    carefully press tape against gold coated quartz piece
    smooth tape over the surface with fingers
    carefully peel tape away from quartz substrate with tweezers, removing gold layer and CNTs

Silicon Device Substrate

Purchase Wafers:
    3" diameter silicon wafers, 0.381mm thick, 1-0-0 orientation, 500 nm thermal oxide, Silicon Quest Int'l

Clean Wafers and Dice Wafers:
    soak full wafers in TCE, acetone, methanol, and IPA for 5 min
    blow dry with nitrogen
    bake at 120 C in an over for 20 min
    dice wafer into quarter pieces with a diamond scribe
    rinse with acetone, methanol, IPA
    blow dry with nitrogen

Transfer CNTs from Thermal Tape to Silicon Device Substrate
    e-beam evaporate 100 nm Au over whole Si/SiO2 piece
    carefully press the adhesive side of the thermal tape piece carrying the Au/CNT layer to the Si/SiO2 piece
    wipe a clean razor blade across the tape surface to ensure uniform contact
    place Si/SiO2/Au/CNT/Tape assembly on a 150 C hot plate
    remove the tape with tweezers as it peels away
    gently rinse Si/SiO2 piece with acetone, methanol, and IPA
    blow dry with nitrogen
    run 45 sec oxygen plasma (100 W, 200 mTorr, 16 sccm O2) in reactive ion etcher
    soak sample in diluted gold etchant (2:1 DI to gold etchant) for 2 min
    rinse with DI
    blow dry with nitrogen

Photolithography: Source-Drain Electrodes
For the high frequency CNT devices, some channel lengths are < 1um, so a stepper was used instead of a contact aligner. The procedure would be very similar if using a contact aligner.

    spin HMDS at 4000 rpm for 60 sec
    spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
    bake on hotplate at 90 C for 60 sec

align source-drain mask pattern in stepper
expose pattern in stepper (400um chuck, 0.24s exposure)
bake on hotplate at 120 C for 60 sec
develop in OPD 4262 for 60 sec
e-beam evaporate 5 nm Ti and 45 nm Au (CHA Mark IV)
liftoff in acetone for 1 hr
use tweezers to remove large flakes of metal weakly sticking to the sample
use strong acetone sprayer to ensure liftoff of small features
rinse in acetone, methanol, IPA
blow dry with nitrogen

Photolithography: Pattern CNTs
This step defines the channel width for each FET and prevents separate devices from being shorted together.
spin OIR 908-35 at 4000 rpm for 60 sec
bake at 90 C for 60 sec
align the CNT pattern mask to the sample alignment marks or source-drain electrodes
expose mask pattern in contact aligner for 13 sec
develop in OIR 4262 for 60 sec
rinse in DI for 30 sec
run 10 sec oxygen plasma (100 W, 200 mTorr, 16 sccm O2) in reactive ion etcher
expose full sample in contact aligner for 13 sec
develop in OIR 4262 for 60 sec
soak in acentone for 3 min
rinse with acetone, methanol, IPA
blow dry with nitrogen

CVD: Hydrogen Anneal - best if done immediately before the next ALD step.
Included in ensuring a clean surface, this process encourages p-type devices.[101]
insert samples in boats into the center of the tube
flush with 200 sccm argon for five minutes
flow 1700 sccm argon and 1900 sccm hydrogen
heat to 400 C
hold temperature and flow rates for 1 hour
cool to room temperature
stop hydrogen flow
stop argon flow after 5 minutes
remove samples

Atomic Layer Deposition: Dielectric Layer
As is discussed in Chapter 3, the deposition temperature will have an effect on the dielectric quality and the charge traps in the sample. There is no procedural difference when using different temperatures. We use a Beneq TFS 500 system.
place Si/SiO2 samples on a clean silicon wafer (the wafer will be used to determine an etch rate later)

load growth recipe (Al_2O_3 baseline, 220 C)
vent system and insert sample
pump system and wait until it reaches temperature
run recipe - set target for 75 nm
vent lines
vent system and remove sample
pump system
log run

Photolithography: Determining Etch Rate:
    dice the silicon wafer that held the Si/SiO2 pieces in the ALD into a few pieces
    spin OIR 908-35 at 4000 rpm for 60 sec on silicon pieces
    bake at 90 C for 60 sec
    expose any mask pattern in contact aligner for 13 sec
    develop in OIR 4262 for 60 sec
    rinse in DI for 30 sec
    dilute buffered oxide etch (BOE) with DI to be 1:3, giving a total molarity of:
    rinse a silicon piece in dilute BOE for 60 sec
    soak in DI for 2 min
    soak in acetone for 2 min
    rinse with acetone, methanol, IPA
    determine etch depth with profilometer
    using that rate, predict the length or time needed to etch 90% of the total dielectric
        thickness (67.5 nm in our case)
    rinse a different silicon piece in the dilute BOE for that length of time
    soak in DI for 2 min
    soak in acetone for 2 min
    rinse with acetone, methanol, IPA
    determine etch depth with profilometer
    use the new depth and time to predict a more accurate etch rate
    continue trial etching in BOE with different silicon pieces if necessary

Photolithography: Dielectric Etching
    spin OIR 908-35 at 4000 rpm for 60 sec on Si/SiO2 samples
    bake at 90 C for 60 sec
    align the dielectric pattern mask to the sample alignment marks or source-drain
    electrodes
    expose in contact aligner for 13 sec
    develop in OIR 4262 for 60 sec
    rinse in DI for 30 sec
    use the same dilute BOE as when determining the etch rate
    add 5% to the total etch time, as it is worse to etch too little than too much
    rinse the Si/SiO2 samples in dilute BOE for the new etch time
    soak in DI for 2 min
    soak in acetone for 2 min
    rinse with acetone, methanol, IPA

Photolithography: Gate

spin HMDS at 4000 rpm for 60 sec
spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
bake on hotplate at 90 C for 60 sec
align gate mask pattern to sample alignment marks in stepper
expose pattern in stepper (400um chuck, 0.24s exposure)
develop in OPD 4262 for 60 sec
rinse with DI for 30 sec
blow dry with nitrogen
e-beam evaporate 5 nm Ti and 95 nm Au (CHA Mark IV)
liftoff in acetone for 1 hr
use tweezers to remove large flakes of metal weakly sticking to the sample
use strong acetone sprayer to ensure liftoff of small features
rinse in acetone, methanol, IPA
blow dry with nitrogen

Appendix B: Fabrication Procedure for Top-Gate aligned CNT FET on PET with Tri-Layer Dielectric and Vertical Integration

These instructions produce an integrated top-gate aligned carbon nanotube FET circuit on a PET substrate with a tri-layer dielectric. The tri-layer dielectric was needed because the CNTs in the channel tend to meander through the PMMA dielectric and short the gate to the source-drain. The Al_2O_3 layer acts as a physical barrier, and the two layers of PMMA are necessary with flexible devices to produce a thick enough dielectric (around 600 nm after printing) to prevent significant gate leakage. The instructions are only one method of fabricating such a device. Other lithographic means could achieve a similar result. Three transfer substrates and one device substrate are necessary to complete device.
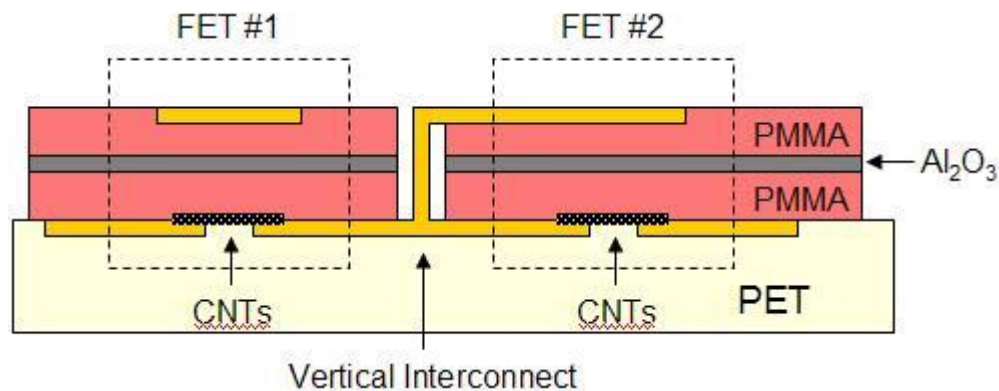
Figure B.1 Diagram of completed integrated circuit using CNT FETs with aligned CNT channels on PET
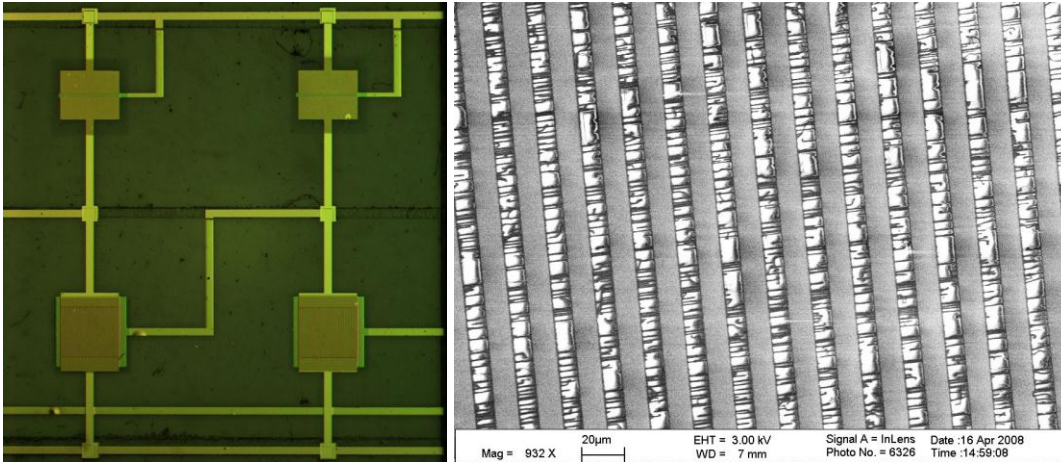
Figure B.2 a) Optical image of completed integrated CNT FET circuit on PET and b) SEM image of CNTs between fingered electrodes before dielectric layers and top-gate are added.

Quartz Transfer Substrate: Quartz Piece with CNTs

Purchase Wafers:
3" diameter, single crystal quartz wafers, 0.5mm thick, ST-cut 42°45', single side polished (SSP), Hoffman Materials

Dicing:
CNTs align themselves perpendicular to the wafer flat, so either mark the back side of the wafer with a diamond scribe to indicate the alignment direction or dice into shapes which allow one to identify the alignment direction.
Cover wafers with photoresist to protect surface during dicing. Many photoresists would do.

    spin HMDS at 4000 rpm for 60 sec
    spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
    bake on hotplate at 90 C for 60 sec
    dice with diamond saw, both sides of wafers covered by tape
    remove tape
    soak and sonicate in Acetone for 10 minutes
    rinse with acetone, methanol, and isopropanol (IPA)
    blow dry with nitrogen

Annealing: necessary for CNT alignment. To prevent cracking, heating and cooling rates should be < 10 C/min.

    heat quartz pieces in open tube furnace (air) to 900 C
    hold for 12 hours
    cool to room temperature

Catalyst Deposition: Ferritin - for medium density and partial alignment over whole sample surface.

    dilute ferritin solution with DI to 1 mg/mL
    soak quartz pieces in solution for 20 min in refrigerator, 3 C
    rinse with DI

blow dry with nitrogen
keep ferritin refrigerated - do not let freeze

CVD: Hydrogen Anneal - to clean the quartz surface of residual photoresist.[101] To prevent cracking, heating and cooling rates should be < 10 C/min.
We use a three-zone tube furnace from Lindberg Blue, 2 in quartz tube, mass flow controllers, and quartz boats from Glass Tech. All three zones are set to the same temperature.

    insert samples in boats into the center of the tube
    flush with 200 sccm argon for five minutes
    flow 1700 sccm argon and 1900 sccm hydrogen
    heat to 400 C
    hold temperature and flow rates for 1 hour
    cool to room temperature
    stop hydrogen flow
    stop argon flow after 5 minutes
    remove samples

CVD: CNT Growth
Many papers report using different gases: methane, ethylene, methanol and ethanol bubblers, water bubblers, etc. No significant difference in density was found from these other sources. To prevent cracking, heating and cooling rates should be < 10 C/min.

    insert samples in boats into the center of the tube
    heat in air to 700 C - to burn away the organics in ferritin
    hold for 10 min (oxidizing step)
    cool to room temperature
    seal tube ends
    flush with 1000 sccm argon, hydrogen, and methane for 5 min
    stop argon and methane flow
    set hydrogen flow to 250 sccm
    heat to 925 C
    hold for 10 min (reducing step)
    introduce methane flow 1000 sccm
    hold for 20 min
    stop methane flow
    cool to room temperature
    stop hydrogen flow
    flush with 1000 sccm argon for 5 min
    remove samples

Release Layer:
    2 hour vapor phase deposition of SAM release layer (tridecafluoro-1,1,2,2-tetrahydrooctyle trichlorosilane)

Silicon Transfer Substrate 1: Silicon Piece with Source-Drain Electrodes

Purchase Wafers:
    3" diameter silicon wafers, 0.381mm thick, 1-0-0 orientation, Silicon Quest Int'l

Clean Wafers and Release Layer:
    soak full wafers in TCE, acetone, methanol, and IPA for 5 min
    blow dry with nitrogen
    bake at 120 C in an over for 20 min
    2 hour vapor phase deposition of SAM release layer (tridecafluoro-1,1,2,2-tetrahydrooctyle trichlorosilane)

Photolithography: Source-Drain Electrodes
    e-beam evaporate 30 nm Au (CHA Mark IV) over full wafer
    dice wafer into quarter pieces with diamond scribe
    gently blow clean with nitrogen
    spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
    bake on hotplate at 90 C for 60 sec
    expose source-drain mask pattern in contact aligner for 13 sec
    develop in OPD 4262 for 60 sec
    rinse with DI for 30 sec
    blow dry with nitrogen
    expose whole sample in contact aligner for 13 sec
    etch electrode pattern in diluted gold etchant (2:1 DI to gold etchant) for 20 sec
    rinse with DI for 30 sec
    develop in OPD 4262 for 60 sec
    rinse with acetone, methanol, and IPA
    blow dry with nitrogen

Silicon Transfer Substrate 2: Silicon Piece with Gate Electrodes, Interconnects, and Dielectric

Purchase Wafers:
    3" diameter silicon wafers, 0.381mm thick, 1-0-0 orientation, Silicon Quest Int'l

Clean Wafers and Release Layer:
    soak full wafers in TCE, acetone, methanol, and IPA for 5 min
    bake at 120 C in an over for 20 min
    2 hour vapor phase deposition of SAM release layer (tridecafluoro-1,1,2,2-tetrahydrooctyle trichlorosilane)

Photolithography: Gate Electrodes
    e-beam evaporate 30 nm Au (CHA Mark IV) over full wafer
    dice wafer into quarter pieces with diamond scribe
    gently blow clean with nitrogen
    spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
    bake on hotplate at 90 C for 60 sec
    expose source-drain mask pattern in contact aligner for 13 sec

develop in OPD 4262 for 60 sec
rinse with DI for 30 sec
blow dry with nitrogen
expose whole sample in contact aligner for 13 sec
etch electrode pattern in diluted gold etchant (2:1 DI to gold etchant) for 20 sec
rinse with DI for 30 sec
develop in OPD 4262 for 60 sec
rinse with acetone, methanol, and IPA
blow dry with nitrogen

Shadowmask Deposition: Interconnects and Dielectric Layer
align interconnect shadowmask to the gate electrodes on sample
e-beam evaporate 600 nm Au (CHA Mark IV) through the shadowmask
remove mask
spin e-beam resist PMMA A7 at 4000 rpm for 60 sec
bake at 120C for 2 min
align dielectric layer shadowmask to the gate electrodes on sample
e-beam evaporate 25 nm of Al_2O_3 (CHA Mark IV) through the shadowmask
remove mask
spin e-beam resist PMMA A7 at 4000 rpm for 60 sec
align dielectric etching shadowmask to interconnects on sample
run 5 minute oxygen plasma (100 W, 200 mTorr, 16 sccm O2) in reactive ion etcher

Assembling Device

Purchase PET:
Polyethylene terephthalate with one side treated for adhesion and the other coated with ITO.
Melinex 453/700 from Dupont Teijin Films

Transfer Printing: Details of the procedure can be found in group publications.[22, 23]
cut piece of PET with scissors to appropriate size for the device substrate
sandwich PET device substrate between Si transfer substrate 1 and a blank Si
    piece with a release layer (Si 1/RL/Au -> PET/ITO -> RL/Si blank)
transfer print source-drain electrode pattern from silicon transfer substrate #1 to
    PET device substrate (Nanonex 2500 imprint machine, 500 PSI, 180 C, 3 min)
sandwich PET device substrate between quartz transfer substrate and a blank Si
    piece with a release layer (Qu/CNT/RL -> Au/PET/ITO -> RL/ Si blank)
transfer print CNTs from quartz transfer substrate to PET device substrate
    (Nanonex 2500 imprint machine, 500 PSI, 100 C, 3 min)
align Si transfer substrate #2 to PET device substrate in Nanonex contact aligner
add blank Si piece with a release layer to the top PET device substrate (Si
    2/RL/Au/PMMA/ Al_2O_3/PMMA -> CNT/Au/PET/ITO -> RL/Si Blank)
transfer print gate electrodes, interconnects, and dielectric layers from Si transfer
    substrate #2 to the PET device substrate (Nanonex 2500 imprint machine, 500
    PSI, 100 C, 3 min)

Appendix C: Fabrication Procedure for Top Local Gated CNT FET on Quartz

These instructions produce a top-gate aligned CNT FET on a quartz substrate. The typical device geometries are: 500 um quartz substrate, aligned CNT channel, 50 nm Ti/Au source-drain, 75 nm Al_2O_3 dielectric, 100 nm Ti/Au gate. If the metallic CNTs are to be removed by joule heating, that should be done after patterning the CNTs and before depositing the Al_2O_3 dielectric.
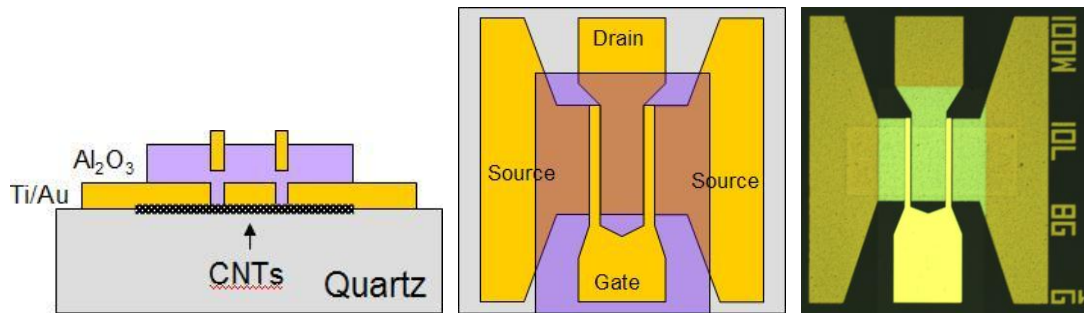
Figure C.1 a) side-view and b) top-view diagram of a completed CNT FET on quartz. c) Optical image of completed device.

Purchase Wafers:
3" diameter, single crystal quartz wafers, 0.5mm thick, ST-cut 42°45', single side polished (SSP), Hoffman Materials

Dicing:
CNTs align themselves perpendicular to the wafer flat, so either mark the back side of the wafer with a diamond scribe to indicate the alignment direction or dice into shapes which allow one to identify the alignment direction.
Cover wafers with photoresist to protect surface during dicing. Many photoresists would do.
    spin HMDS at 4000 rpm for 60 sec
    spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
    bake on hotplate at 90 C for 60 sec
    dice with diamond saw, both sides of wafers covered by tape
    remove tape
    soak and sonicate in Acetone for 10 minutes
    rinse with acetone, methanol, and isopropanol (IPA)
    blow dry with nitrogen

Annealing: necessary for CNT alignment. To prevent cracking, heating and cooling rates should be < 10 C/min.
   heat quartz pieces in open tube furnace (air) to 900 C
   hold for 12 hours
   cool to room temperature

Alignment Marks: (only needed for iron catalyst)
Many photoresists would do.
   spin negative photoresist, NR7-1500 PY at 4000 rpm for 60 sec
   bake on hotplate at 90 C for 60 sec
   expose alignment mark mask pattern in contact aligner, 16 sec
   bake on hotplate at 120 C for 60 sec
   develop in RD6 for 15 sec
   rinse with DI for 30 sec
   e-beam evaporate 30nm Ti (CHA Mark IV)
   liftoff photoresist in RR2, 85 C
   rinse in acetone, do not let dry
   rinse in photostripper (Microstrip 2001) for 3 minutes
   rinse in acetone, methanol, IPA
   blow dry with nitrogen

Catalyst Deposition: Ferritin - for medium density and partial alignment over whole sample surface.
   dilute ferritin solution with DI to 1 mg/mL
   soak quartz pieces in solution for 20 min in refrigerator, 3 C
   rinse with DI
   blow dry with nitrogen
   keep ferritin refrigerated - do not let freeze

Catalyst Deposition: Iron - for patterned high density and alignment. The same patterning could be done with ferritin, with a small reduction in density.
To evaporate the thin film of iron, use a slow deposition rate (0.1 A/s). Use a new single iron pellet in a clean crucible and focus the beam on the pellet before depositing.
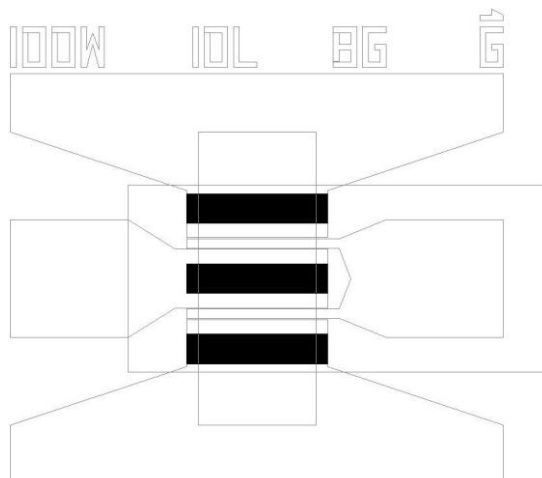
Figure C.2 Diagram of the CNT FET device geometry with the iron catalyst lithography mask filled in.

    spin positive photoresist OIR 908-35 at 4000 rpm for 60 sec
    bake on hotplate at 90 C for 60 sec
    align catalyst mask to sample alignment marks in contact aligner
    expose in contact aligner, 13 sec
    develop in OPD 4262 for 60 sec
    rinse with DI for 30 sec
    e-beam evaporate 0.5 nm Fe (CHE Mark IV)
    expose sample surface without mask in contact aligner, 13 sec
    soak in OPD 4262 for 3 min
    soak in photostripper, Microstrip 2001 for 3 min
    soak in acetone for 3 min
    rinse with DI
    blow dry with nitrogen

CVD: Hydrogen Anneal - to clean the quartz surface of residual photoresist.[101] To prevent cracking, heating and cooling rates should be < 10 C/min.
We use a three-zone tube furnace from Lindberg Blue, 2 in quartz tube, mass flow controllers, and quartz boats from Glass Tech. All three zones are set to the same temperature.
    insert samples in boats into the center of the tube
    flush with 200 sccm argon for five minutes
    flow 1700 sccm argon and 1900 sccm hydrogen
    heat to 400 C
    hold temperature and flow rates for 1 hour
    cool to room temperature
    stop hydrogen flow
    stop argon flow after 5 minutes
    remove samples

CVD: CNT Growth

Many papers report using different gases: methane, ethylene, methanol and ethanol bubblers, water bubblers, etc. No significant difference in density was found from these other sources. To prevent cracking, heating and cooling rates should be < 10 C/min.

   insert samples in boats into the center of the tube
   heat in air to 700 C - to burn away the organics in ferritin and make isolated iron
        oxide nanoparticles from iron films
   hold for 10 min (oxidizing step)
   cool to room temperature
   seal tube ends
   flush with 1000 sccm argon, hydrogen, and methane for 5 min
   stop argon and methane flow
   set hydrogen flow to 250 sccm
   heat to 925 C
   hold for 10 min (reducing step)
   introduce methane flow 1000 sccm
   hold for 20 min
   stop methane flow
   cool to room temperature
   stop hydrogen flow
   flush with 1000 sccm argon for 5 min
   remove samples

Photolithography: Source-Drain Electrodes
For the high frequency CNT devices, some channel lengths are < 1um, so a stepper was used instead of a contact aligner. The procedure would be very similar if using a contact aligner.
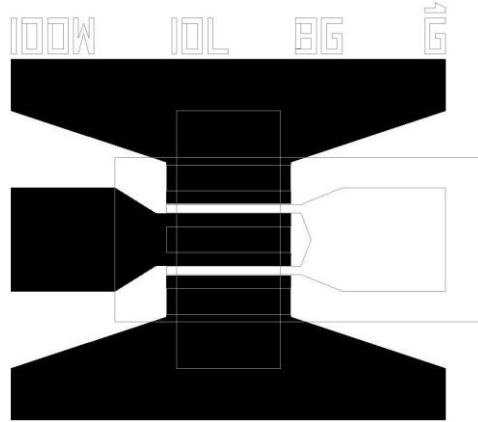

Figure C.3 Diagram of the CNT FET device geometry with the source-drain lithography mask filled in.

   spin HMDS at 4000 rpm for 60 sec
   spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
   bake on hotplate at 90 C for 60 sec
   align source-drain mask pattern to sample alignment marks in stepper (if used)
   expose pattern in stepper (400um chuck, 0.24s exposure)

bake on hotplate at 120 C for 60 sec
develop in OPD 4262 for 60 sec
e-beam evaporate 5 nm Ti and 45 nm Au (CHA Mark IV)
liftoff in acetone for 1 hr
use tweezers to remove large flakes of metal weakly sticking to the sample
use strong acetone sprayer to ensure liftoff of small features
rinse in acetone, methanol, IPA
blow dry with nitrogen

Photolithography: Pattern CNTs

This step defines the channel width for each FET and prevents separate devices from being shorted together.

Figure C.4 Diagram of the CNT FET device geometry with the nanotube channel lithography mask filled in.

spin OIR 908-35 at 4000 rpm for 60 sec
bake at 90 C for 60 sec
align the CNT pattern mask to the sample alignment marks or source-drain electrodes
expose mask pattern in contact aligner for 13 sec
develop in OIR 4262 for 60 sec
rinse in DI for 30 sec
run 10 sec oxygen plasma (100 W, 200 mTorr, 16 sccm O2) in reactive ion etcher
expose full sample in contact aligner for 13 sec
develop in OIR 4262 for 60 sec
soak in acentone for 3 min
rinse with acetone, methanol, IPA
blow dry with nitrogen

CVD: Hydrogen Anneal - best if done immediately before the next ALD step.

Included in ensuring a clean surface, this process encourages p-type devices.[101] To prevent cracking, heating and cooling rates should be < 10 C/min.
insert samples in boats into the center of the tube
flush with 200 sccm argon for five minutes

flow 1700 sccm argon and 1900 sccm hydrogen
heat to 400 C
hold temperature and flow rates for 1 hour
cool to room temperature
stop hydrogen flow
stop argon flow after 5 minutes
remove samples

Atomic Layer Deposition: Dielectric Layer
As is discussed in Chapter 3, the deposition temperature will have an effect on the dielectric quality and the charge traps in the sample. There is no procedural difference when using different temperatures. We use a Beneq TFS 500 system.
place quartz samples on a clean silicon wafer (the wafer will be used to determine an etch rate later)
load growth recipe (Al_2O_3 baseline, 220 C)
vent system and insert sample
pump system and wait until it reaches temperature
run recipe - set target for 75 nm
vent lines
vent system and remove sample
pump system
log run

Photolithography: Determining Etch Rate:
dice the silicon wafer that held the quartz pieces in the ALD into a few pieces
spin OIR 908-35 at 4000 rpm for 60 sec on silicon pieces
bake at 90 C for 60 sec
expose any mask pattern in contact aligner for 13 sec
develop in OIR 4262 for 60 sec
rinse in DI for 30 sec
dilute buffered oxide etch (BOE) with DI to be 1:3, giving a total molarity of:
rinse a silicon piece in dilute BOE for 60 sec
soak in DI for 2 min
soak in acetone for 2 min
rinse with acetone, methanol, IPA
determine etch depth with profilometer
using that rate, predict the length or time needed to etch 90% of the total dielectric thickness (67.5 nm in our case)
rinse a different silicon piece in the dilute BOE for that length of time
soak in DI for 2 min
soak in acetone for 2 min
rinse with acetone, methanol, IPA
determine etch depth with profilometer
use the new depth and time to predict a more accurate etch rate
continue trial etching in BOE with different silicon pieces if necessary

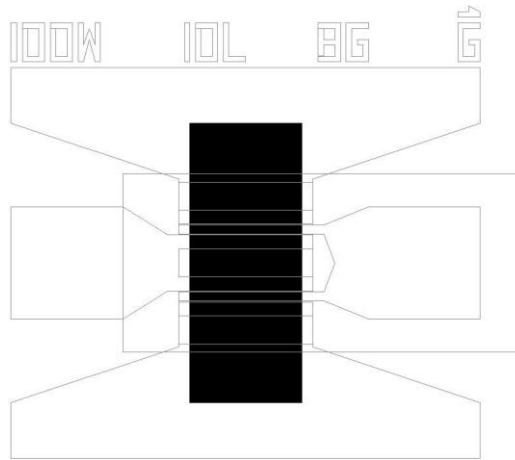**Photolithography: Dielectric Etching**

Figure C.5 Diagram of the CNT FET device geometry with the dielectric layer lithography mask filled in.

　　spin OIR 908-35 at 4000 rpm for 60 sec
　　bake at 90 C for 60 sec
　　align the dielectric pattern mask to the sample alignment marks or source-drain
　　electrodes
　　expose in contact aligner for 13 sec
　　develop in OIR 4262 for 60 sec
　　rinse in DI for 30 sec
　　use the same dilute BOE as when determining the etch rate
　　add 5% to the total etch time, as it is worse to etch too little than too much
　　rinse the quartz samples in dilute BOE for the new etch time
　　soak in DI for 2 min
　　soak in acetone for 2 min
　　rinse with acetone, methanol, IPA

Photolithography: Gate
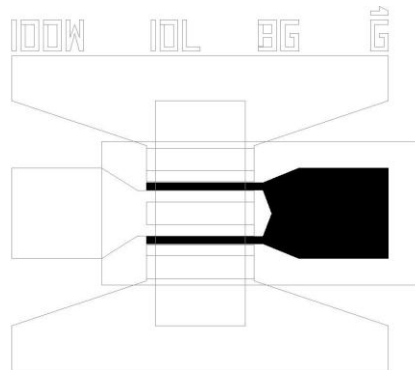
Figure C.6 Diagram of the CNT FET device geometry with the gate lithography mask filled in.

　　spin HMDS at 4000 rpm for 60 sec
　　spin positive photoresist, OIR 908-35 at 4000 rpm for 60 sec
　　bake on hotplate at 90 C for 60 sec
　　align gate mask pattern to sample alignment marks in stepper

expose pattern in stepper (400um chuck, 0.24s exposure)
develop in OPD 4262 for 60 sec
rinse with DI for 30 sec
blow dry with nitrogen
e-beam evaporate 5 nm Ti and 95 nm Au (CHA Mark IV)
liftoff in acetone for 1 hr
use tweezers to remove large flakes of metal weakly sticking to the sample
use strong acetone sprayer to ensure liftoff of small features
rinse in acetone, methanol, IPA
blow dry with nitrogen

Appendix D: Capacitance Calculations

The capacitances of the parallel plate capacitors introduced in Chapter 2 were extracted in several ways. First, the capacitance equation for parallel plate arrangements was used based on the electrode geometries. This equation is given in EQ D.1, where k is the dielectric constant, ε_0 is the permittivity of free space, A is the area of overlap, and d is the separation of the plates.

$$C = \frac{k\varepsilon_0 A}{d}$$ EQ D.1

The AC capacitance was also measured using an LCR meter at 100 kHz (HP 4275A Multi-Frequency LCR Meter). The third method used scattering (S) parameters taken from VNA measurements from 100 kHz to 20 GHz. The impedance of an ideal capacitor should be inversely related to frequency and capacitance, as shown in EQ D.2. Using the input impedance calculated from S_{11} (EQ D.3), the capacitance for each parallel plate capacitor was calculated in this high frequency regime. The results of each of the three techniques is given in Table D.1. The parallel plate calculation and LCR meter measurement correspond well. The results from the VNA measurements at higher frequencies are of the same order of magnitude.

$$Z_{cap} = \frac{1}{j2\pi fC}$$ EQ D.2

$$Z_{in} = 50\frac{S_{11}-1}{S_{11}+1}$$ EQ D.3

	C1	C2	C3	C4	C5
Parallel Plate Calculation	44.0 pF	15.9 pF	2.75 pF	440 fF	27.5 fF
LCR Meter (100 kHz)	43.5 pF	15.5 pF	2.61 pF	381 fF	15.5 fF
S Parameter Extraction	20 pF	8 pF	2 pF	250 pF	30 fF

Table D.1 The calculated capacitances for five fabricated parallel plate capacitors using a parallel plate calculation, an LCR meter, and S Parameters taken with a vector network analyzer.

It is also useful to know the different capacitances in our CNT FETs, the capacitance between the gate and the CNTs (C_{GCNT}), the capacitance between the gate and the sources (C_{GS}), and the capacitance between the gate and the drain (C_{GD}). The capacitance between the gate and the CNTs can be approximated as the capacitance between a cylinder and an infinite plane, given in EQ D.4, where h is the distance between the cylinder and the plane, and d is the cylinder diameter.

$$\frac{C_{GCNT}}{L} \approx \frac{2\pi k \varepsilon_0}{\ln(h/d)} \qquad\qquad \text{EQ D.4}$$

Using a dielectric constant of 8, a dielectric thickness of 65 nm, a CNT diameter of 1.5 μm, and the channel length of 10 μm, the approximate gate-CNT capacitance is 1.2 pF per CNT. The capacitance of a CNT FET was also taken from VNA measurements as described earlier. A plot of C_{GCNT} extracted from S Parameters is given in Figure D.1. It calculates C_{GCNT} to be between 100 and 250 fF, which corresponds to 80 to 210 CNTs, which is consistent with our growth density in a 100 μm wide channel.
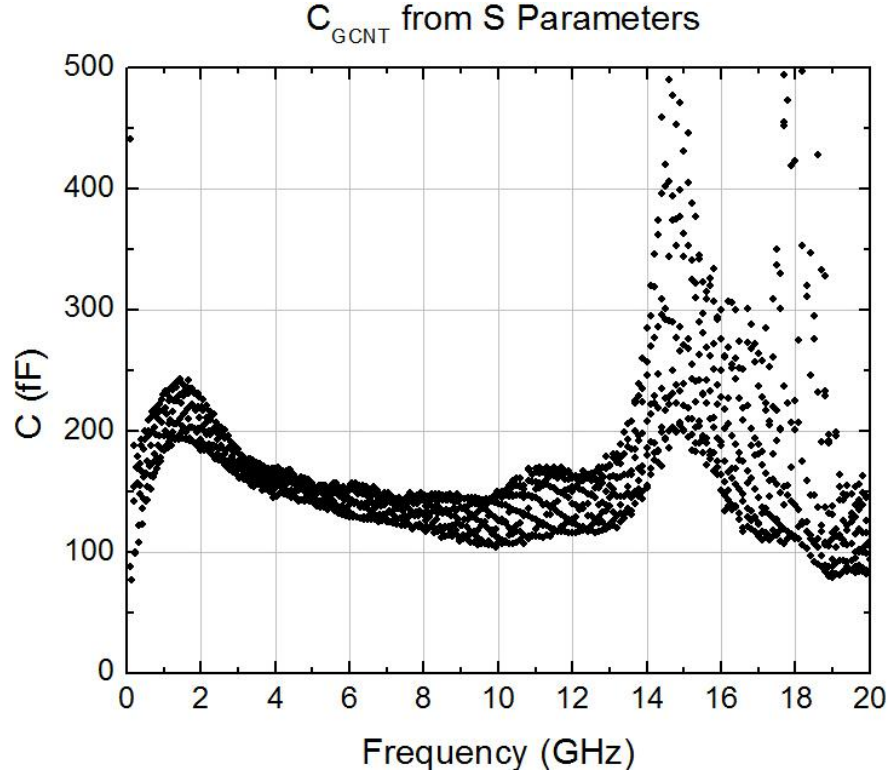
Figure D.1 Gate-CNT capacitance (C_{GCNT}) plotted as a function of frequency extracted from scattering parameters taken on a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm).

To estimate the gate capacitance to the drain and source, S Parameters were taken on an FET electrode geometry without any CNTs in the channel ($W = 0$). The capacitance associated with that measurement should give the gate-drain capacitance. Since the source electrodes cannot be probed in a GSG configuration, their capacitance cannot be measured directly. However, the electrode proximity to the gate is similar for both the sources and the drain, so $C_{GS} \approx C_{GD}$. In addition to device measurements, a simulation of the FET geometry without CNTs was made with Microwave Office, which produces theoretical scattering parameters. The resulting capacitances from both the VNA measurements and the Microwave Office Simulation are plotted in Figure D.2.
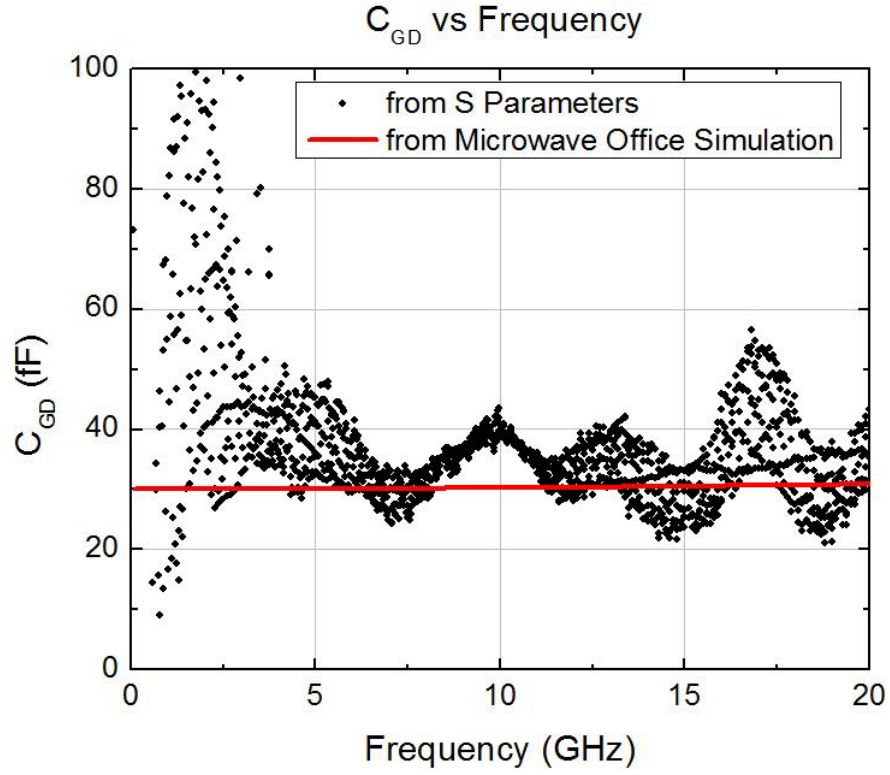
Figure D.2 Gate-drain capacitance (C_{GD}) plotted as a function of frequency extracted from scattering parameters taken on an FET electrode geometry without CNTs in the channel ($W = 0$, $L = 10$ μm, $G = 8$ μm). The same capacitance from a Microwave Office simulation using the same device geometry is plotted in red.

The theory and the data plots overlap, giving a gate-drain capacitance near 30 fF. When referenced in this dissertation, the gate capacitance values used are $C_{GCNT} = 100$ fF, $C_{GS} = C_{GD} = 30$ fF.

Appendix E: Preisach Hysteresis Model Matlab Script

```matlab
clear all; close all;
n=100;                  % n is the of vertical divisions
N=n*(n+1)/2;            % N is the total number of hysterons
h=2/(n+1);              % h is the separation between
hysterons
a0=-1+h/2;              % a0 is the first alpha value
b0=-1+3*h/2;            % bo is the first beta value

% The locations of each hysteron (a, b) are filled in.

i=1;
for i1=1:n
    for i2=1:i1
        a(i,1)=a0 + (i2-1)*h;
        b(i,1)=b0;
        i=i+1;
    end
    b0=b0+h;
end

% The initial default hysteron occupation (R0) is set by
sweeping waveform D.

Osc=100;
for i1=1:Osc+1
    VgsMax(i1,1)=1-(i1-1)/Osc;
end

for i1=1:Osc
    x=VgsMax(i1,1);
    for i2=1:N
         if x>b(i2,1);
            R0(i2,1)=1;
        end
        if x<a(i2,1);
            R0(i2,1)=0;
        end
    end

    x=-VgsMax(i1+1,1);
    for i2=1:N
        if x>b(i2,1);
            R0(i2,1)=1;
        end
        if x<a(i2,1);
```

```
                R0(i2,1)=0;
        end
    end
end

% The current hysteron occupation (R) is set to the
default.

for i1=1:N
    R(i1,1)=R0(i1,1);
end

% Sweeps - Only one is executed at a time.



                            % Waveform A
t=1;
for x=0:0.01:1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;
end

for x=1:-0.01:-1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
```

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```
        y(t,1)=sum(R)/N;
        t=t+1;
end

for x=-1:0.01:1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;
end




                        % Waveform B
t=1; j=1;
for x=0:0.01:1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
```

```
        end
    end
    x2(j,1)=x;
    y2(j,1)=sum(R)/N;
    j=j+1;
end


for x=1:-0.01:-1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
    end
    x2(j,1)=x;
    y2(j,1)=sum(R)/N;
    j=j+1;
end


for x=-1:0.01:1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
```

```matlab
                R(i1,1)=0;
            end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
    end
    x2(j,1)=x;
    y2(j,1)=sum(R)/N;
    j=j+1;
end



                                % Waveform C
t=1; j=1;
for x=0:0.01:1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
```

```
        end
    x2(j,1)=x;
    y2(j,1)=sum(R)/N;
    j=j+1;
%-Vgs
    xx(t,1)=-x;
    time(t,1)=t;

    for i1=1:N
        if -x>b(i1);
            R(i1,1)=1;
        end
        if -x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
    end
    x2(j,1)=-x;
    y2(j,1)=sum(R)/N;
    j=j+1;
end


for x=1:-0.01:-1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
```

```
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
    end
    x2(j,1)=x;
    y2(j,1)=sum(R)/N;
    j=j+1;
%-Vgs
    xx(t,1)=-x;
    time(t,1)=t;

    for i1=1:N
        if -x>b(i1);
            R(i1,1)=1;
        end
        if -x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
    end
    x2(j,1)=-x;
    y2(j,1)=sum(R)/N;
    j=j+1;
end


for x=-1:0.01:1
    xx(t,1)=x;
    time(t,1)=t;
```

```
    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
    end
    x2(j,1)=x;
    y2(j,1)=sum(R)/N;
    j=j+1;
%-Vgs
    xx(t,1)=-x;
    time(t,1)=t;

    for i1=1:N
        if -x>b(i1);
            R(i1,1)=1;
        end
        if -x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Vgs=0
    for i1=1:N
        if 0>b(i1);
            R(i1,1)=1;
        end
        if 0<a(i1);
            R(i1,1)=0;
        end
```

```matlab
    end
    x2(j,1)=-x;
    y2(j,1)=sum(R)/N;
    j=j+1;
end


                            % Waveform D
t=1;
for x=0:0.01:1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Detrap
    Osc=2;
    for i1=1:Osc+1
        VgsMax(i1,1)=1-(i1-1)/Osc;
    end

    for i1=1:Osc
        x=VgsMax(i1,1);
        for i2=1:N
            if x>b(i2,1);
                R(i2,1)=1;
            end
            if x<a(i2,1);
                R(i2,1)=0;
            end
        end

        x=-VgsMax(i1+1,1);
        for i2=1:N
            if x>b(i2,1);
                R(i2,1)=1;
            end
            if x<a(i2,1);
```

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```matlab
                R(i2,1)=0;
            end
        end
    end
end

for x=1:-0.01:-1
    xx(t,1)=x;
    time(t,1)=t;

    for i1=1:N
        if x>b(i1);
            R(i1,1)=1;
        end
        if x<a(i1);
            R(i1,1)=0;
        end
    end
    y(t,1)=sum(R)/N;
    t=t+1;

% Detrap
    for i1=1:Osc
        x=VgsMax(i1,1);
        for i2=1:N
            if x>b(i2,1);
                R(i2,1)=1;
            end
            if x<a(i2,1);
                R(i2,1)=0;
            end
        end

        x=-VgsMax(i1+1,1);
        for i2=1:N
            if x>b(i2,1);
                R(i2,1)=1;
            end
            if x<a(i2,1);
                R(i2,1)=0;
            end
        end
    end
end

for x=-1:0.01:1
    xx(t,1)=x;
```

```
        time(t,1)=t;

        for i1=1:N
            if x>b(i1);
                R(i1,1)=1;
            end
            if x<a(i1);
                R(i1,1)=0;
            end
        end
        y(t,1)=sum(R)/N;
        t=t+1;

    % Detrap
        for i1=1:Osc
            x=VgsMax(i1,1);
            for i2=1:N
                if x>b(i2,1);
                    R(i2,1)=1;
                 end
                if x<a(i2,1);
                    R(i2,1)=0;
                end
            end

            x=-VgsMax(i1+1,1);
            for i2=1:N
                if x>b(i2,1);
                    R(i2,1)=1;
                end
                if x<a(i2,1);
                    R(i2,1)=0;
                end
            end
        end
end
```

```matlab
% data is exported to an Excel spreadsheet


filename='test.xls';

xlswrite(filename, 'n', 'Sheet1', 'A1');
xlswrite(filename, n, 'Sheet1', 'A2');

xlswrite(filename, 'N', 'Sheet1', 'A4');
xlswrite(filename, N, 'Sheet1', 'A5');

xlswrite(filename, 'h', 'Sheet1', 'A7');
xlswrite(filename, h, 'Sheet1', 'A8');


xlswrite(filename, 't', 'Sheet1', 'B1');
xlswrite(filename, time, 'Sheet1', 'B2');
xlswrite(filename, 'x', 'Sheet1', 'C1');
xlswrite(filename, xx, 'Sheet1', 'C2'); % xx is the input
xlswrite(filename, 'y', 'Sheet1', 'D1');
xlswrite(filename, y, 'Sheet1', 'D2');  % y is the output

xlswrite(filename, 'a', 'Sheet1', 'F1');
xlswrite(filename, a, 'Sheet1', 'F2');  % a are the
alphas
xlswrite(filename, 'b', 'Sheet1', 'G1');
xlswrite(filename, b, 'Sheet1', 'G2');  % b are the betas
xlswrite(filename, 'R', 'Sheet1', 'H1');
xlswrite(filename, R, 'Sheet1', 'H2');  % R is the final
occupation for each hysteron.

xlswrite(filename, 'y2', 'Sheet1', 'K1');
xlswrite(filename, y2, 'Sheet1', 'K2'); % y2 is the
output for x = 0 for Waveforms B, C, and D.
```

Appendix F: Recalibrating Two-Tone Input Power

In section 7.2.2.2, two-tone mixing experiments were performed at fixed frequencies in which one input power swept from -20 dBm to 20 dBm while the other remained fixed. The output mixing products showed some amplitudes dropping as the first input power increased, indicating that the power reaching the device from the second signal generator was not remaining constant as expected.

This behavior is not completely understood, but it is likely due to the power divider that is used to join the two input tones. It should operate by dividing the power at each terminal equally across the other two terminals, so the signal output to the device should include one half of the power from signal generator #1 and one half the power from signal generator #2. Since the input impedance of our CNT FET devices are larger than 50 Ω, part of the signal at the output terminal is reflected back into the power divider and when the input power is large enough (10 dBm or greater), unexpected behavior occurs. When reflected power is inserted back into the output terminal, it is divided across the two input terminals. The output of each signal generator is then divided by the total power at its terminal, which includes contributions from the other signal generator and the output. The end result is that as one input power is increased, the amount of power transmitted to the device from the other signal generator is reduced. This appears to be an input power limitation of the power divider used, as this reduction is similar for different input powers of the signal generator held at constant power, as shown in Figure F.1. No input power limitation was listed in the power divider's specifications. This unexpected behavior is a lesson

in why one should use a directional coupler instead of a power divider for this type of experiment.
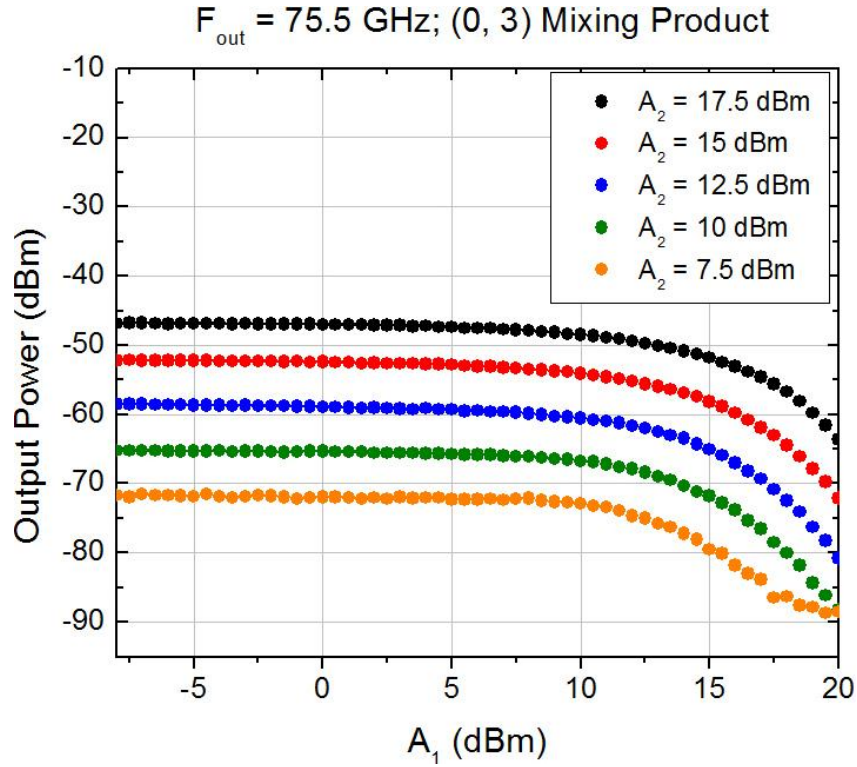

Figure F.1 Plot of the output power of the (0, 3) mixing product vs. the output power of one signal generator for different constant input powers of the second signal generator in a two-tone mixing setup performed on a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm). The other signal generator was held at a fixed output power of 15 dBm. The output frequency was 75.5 GHz, which is three times the input frequencies, which were separated by 100 kHz.

The mixing peak amplitudes could be analyzed at low input powers where the power divider behaves as expected, but fewer peaks are produced at those input powers. To consider the six main peaks observed, the powers produced by the signal generators are converted to the powers incident upon the device. When ignoring the 5th order and higher expansion terms, the 3rd order harmonics of the two fundamentals, (0, 3) and (3, 0), do not depend on the input power of the other tone, therefore their outputs should primarily only depend on one signal generator. The (3,

0) data are used to extract the signal power at the input of the device from signal generator #1 and the (0, 3) data are used to extract the same from signal generator #2. The extracted relationships will then be used to predict the output of cross mixing products which will be compared with the measured results. We will be using the convention of A to mean power in dBm, P is power in mW, and V is voltage in volts. Signals will be referenced at three different locations which are labeled in Figure F.2. The output of the signal generators will use the subscript "SG" (so A1 becomes $A_{SG}1$); the input on the gate of the device carries the subscript "in;" and the output of the device read at the spectrum analyzer is labeled "out." The labels 1 and 2 refer to the signals carrying F_1 and F_2. We will be determining A_{in} as a function of A_{SG}.
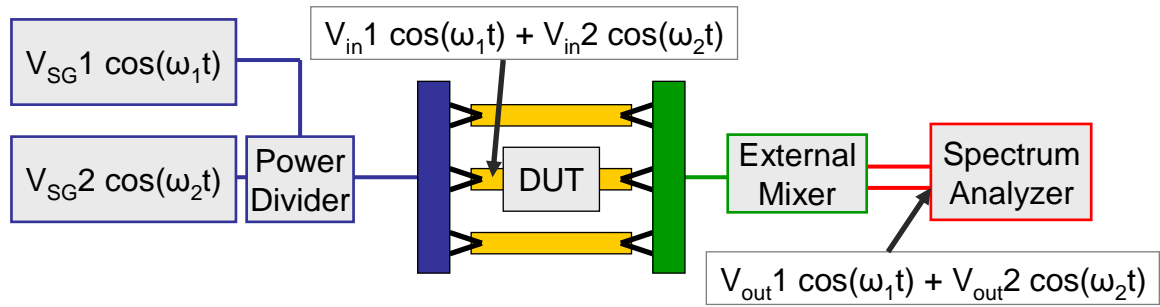

Figure F.2 Diagram of our HF two-tone mixing experimental setup showing the locations of the different signal amplitudes analyzed. V_{SG} is the voltage produced by the signal generator; V_{in} is the voltage incident upon the device; V_{out} is the voltage read by the spectrum analyzer.

First, the (3, 0) plot is used to find the linear relationship between $A_{SG}1$ and $A_{in}1$, shown in Figure F.3. The fit was made for the powers of $A_{SG}1$ where the (3, 0) peak is above the noise floor. If $A_{SG}1$ was equal to $A_{in}1$, the slope of this line should be 3 as shown in EQ F.2-5. The variables α and β will be used in this section to make the equations less messy as define in EQ F.1

$$\alpha_n = \frac{\partial^{n-1}G}{\partial V_{gs}^{n-1}} \frac{1}{n!} \qquad\qquad \beta_n = \alpha_n^2 R^4 \qquad\qquad \text{EQ F.1}$$

$$I_d\left(\delta V\right)\Big|_{(3,0)} \approx \alpha_3 \frac{1}{4}\left(V_{in}1\right)^3 \qquad \text{EQ F.2}$$

Squaring the current and multiplying by R puts EQ F.3 in terms of power.

$$\left(I_d\left(\delta V\right)\Big|_{(3,0)}\right)^2 R \approx \alpha_3^2 R\left(\frac{1}{4}\right)^2 \left(V_{in}1\right)^6 = \alpha_3^2 R^4\left(\frac{1}{4}\right)^2 \left[\frac{\left(V_{in}1\right)^2}{R}\right]^3 \qquad \text{EQ F.3}$$

$$P_{out}\Big|_{(3,0)} \approx \beta_3 \left(\frac{1}{4}\right)^2 \left(P_{in}1\right)^3 \qquad \text{EQ F.4}$$

Taking the logarithm of each side puts the powers in terms of dBm.

$$Log\left(P_{out}\Big|_{(3,0)}\right) \approx Log(\beta_3) + 2Log\left(\frac{1}{4}\right) + 3Log(P_{in}1)$$

$$A_{out}\Big|_{(3,0)} \approx 10Log(\beta_3) + 20Log\left(\frac{1}{4}\right) + 3A_{in}1 \qquad \text{EQ F.5}$$

Thus, the output power of the (3, 0) mixing product be proportional to 3 times the input power of signal generator #1. The (3, 0) plot in Figure F.3 provides us with the line:

$$A_{out}\Big|_{(3,0)} \propto 2.769 A_{SG}1 \qquad \text{EQ F.6}$$

Combining EQ F.5 and F.6 gives the relationship between $A_{in}1$ and $A_{SG}1$. From the observations of the fundamental amplitudes in Chapter 6, the attenuation at 15 dBm input powers near 25 GHz input signal was 30 dB, plus 1 extra dB because the cable on the first signal generator. Using that data point produces EQ F.7.

$$\boxed{A_{in}1 = 0.923 A_{SG}1 - 29.845 dBm} \qquad \text{EQ F.7}$$

Figure F.3 Plot of the output power of the (3, 0) mixing product peak vs. the output power of one signal generator in a two-tone mixing setup performed on a CNT FET (W = 100 μm, L = 10 μm, G = 8 μm). The other signal generator was held at a fixed output power of 15 dBm. The output frequency was 75.5 GHz + 300 kHz, which is three times the input frequency of the first signal generator.

Next, the (0, 3) plot is used to find the relationship between $A_{SG}2$ and $A_{in}2$. No simple fitting functions are obvious when plotted in terms of dBm, so the plot in mW is shown in Figure F.4. An exponential relationship is apparent and given in EQ F.8.

$$P_{out}\big|_{(0,3)} \propto \exp(-P_{SG}1/22.091) \qquad \text{EQ F.8}$$

Following the same steps shown in EQ F.2-4 for this peak produces:

$$P_{out}\big|_{(0,3)} \approx \beta_3 \left(\frac{1}{4}\right)^2 (P_{in}2)^3 \qquad \text{EQ F.9}$$

Combining EQ F.7 and EQ F.8 and fitting such that $P_{in}1 = P_{in}2$ where (3, 0) and (0, 3) intercept (A1 = 16 dBm, A2 = 15 dBm) produces EQ F.10.

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$$P_{in}2 = 0.05665 \exp(-P_{SG}1/66.2723) \quad \text{for } A2 = 15 \text{ dBm} \qquad\qquad \text{EQ F.10}$$
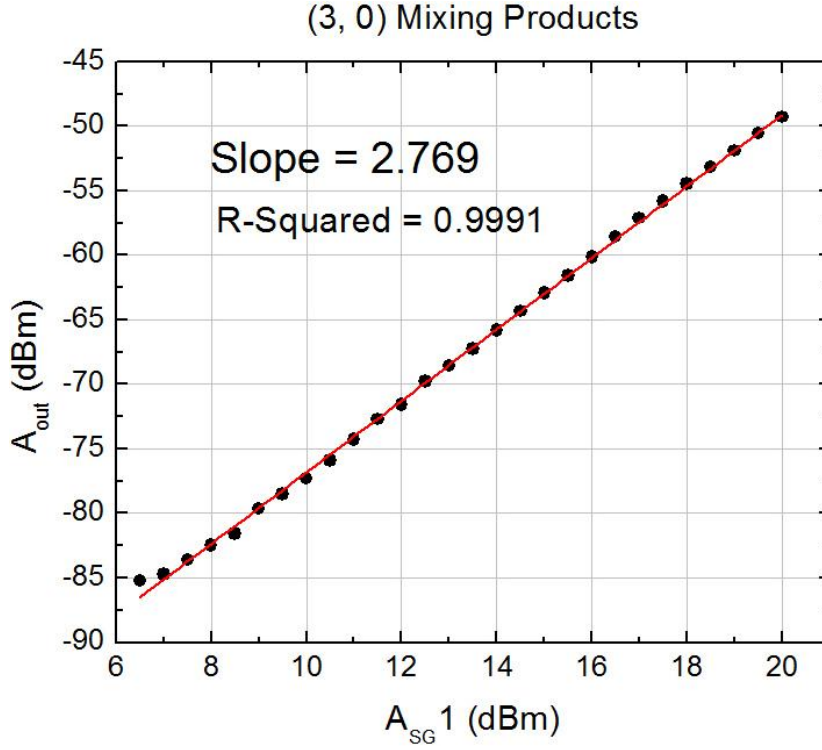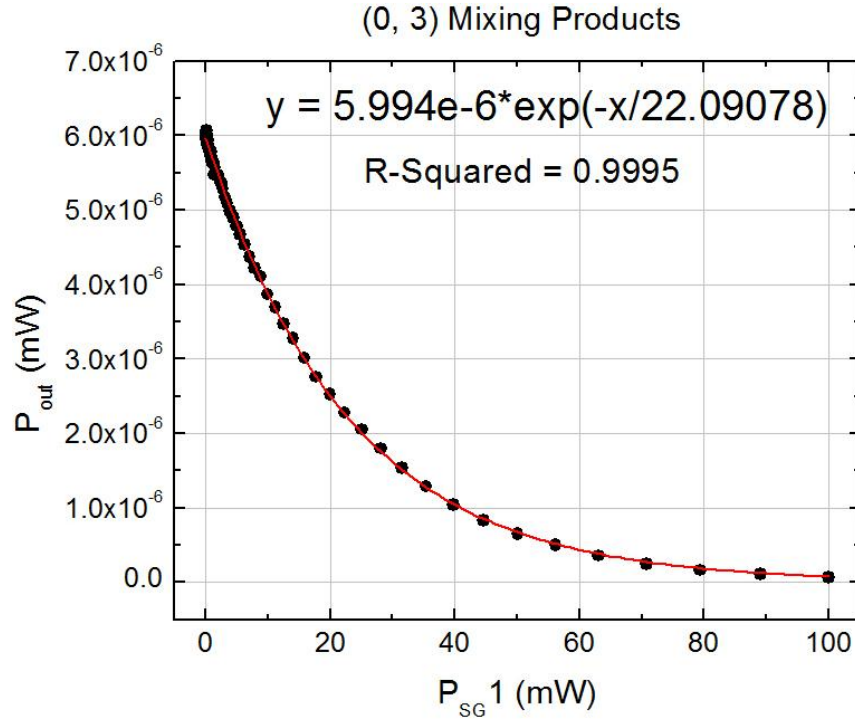

Figure F.4 Plot of the output power of the (0, 3) mixing product peak vs. the output power of one signal generator in a two-tone mixing setup performed on a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm). The other signal generator was held at a fixed output power of 15 dBm. The output frequency was 75.5 GHz – 300 kHz, which is three times the input frequency of the first signal generator.

EQ F.7 and F.10 are used to convert the powers displayed on the signal generators to the powers incident on the device. By using our Taylor expansion of drain current under mixing, the expected output amplitude dependence on input power is generated for the other four mixing peaks, which is compared with the measured data.

First considering only one term in each peak's expansion, the output power as a function of the input power for all six peaks is listed in EQ F.11.

$$P_{out}|_{(1,2)} \approx \beta_3 \left(\frac{3}{4}\right)^2 (P_{in}1)(P_{in}2)^2 \qquad A_{out}|_{(1,2)} \approx 10Log(\beta_3) + 20Log\left(\frac{3}{4}\right) + A_{in}1 + 2A_{in}2$$

$$P_{out}|_{(2,1)} \approx \beta_3 \left(\frac{3}{4}\right)^2 (P_{in}1)^2 (P_{in}2) \qquad A_{out}|_{(2,1)} \approx 10Log(\beta_3) + 20Log\left(\frac{3}{4}\right) + 2A_{in}1 + A_{in}2$$

$$P_{out}|_{(0,3)} \approx \beta_3 \left(\frac{1}{4}\right)^2 (P_{in}2)^3 \qquad A_{out}|_{(0,3)} \approx 10Log(\beta_3) + 20Log\left(\frac{1}{4}\right) + 3A_{in}2$$

$$P_{out}|_{(3,0)} \approx \beta_3 \left(\frac{1}{4}\right)^2 (P_{in}1)^3 \qquad A_{out}|_{(3,0)} \approx 10Log(\beta_3) + 20Log\left(\frac{1}{4}\right) + 3A_{in}1$$

$$P_{out}|_{(-1,4)} \approx \beta_5 \left(\frac{5}{16}\right)^2 (P_{in}1)(P_{in}2)^4 \qquad A_{out}|_{(-1,4)} \approx 10Log(\beta_5) + 20Log\left(\frac{5}{16}\right) + A_{in}1 + 4A_{in}2$$

$$P_{out}|_{(4,-1)} \approx \beta_5 \left(\frac{5}{16}\right)^2 (P_{in}1)^4 (P_{in}2) \qquad A_{out}|_{(4,-1)} \approx 10Log(\beta_5) + 20Log\left(\frac{5}{16}\right) + 4A_{in}1 + A_{in}2$$

EQ F.11

By matching the output to (0, 3) and (3, 0), $\beta_3 = 0.537$ mW and $\beta_5 = 20.0$ mW.

These values give: $\dfrac{\partial^2 G}{\partial V_{gs}^2} = 55.6 \ \mu S / V^2$ and $\dfrac{\partial^4 G}{\partial V_{gs}^4} = 6.78 \ \mu S / V^4$. Figure F.5 displays

the measured data for each mixing product plotted against the expected product

behavior using EQ F.11 and the expected input signal amplitudes from EQ F.7 and

F.10. The agreement for the (0, 3) and (3, 0) plots is nearly perfect. This may seem

inevitable since they were used to predict the input amplitudes, but they were not

transposed point by point. Simple functions (linear and exponential) fit their behavior

very well. The other four mixing product projections follow the same trends as the

data, falling short at large values of $A_{SG}1$. Including more terms in the expansion

would raise the projected output power in each plot.
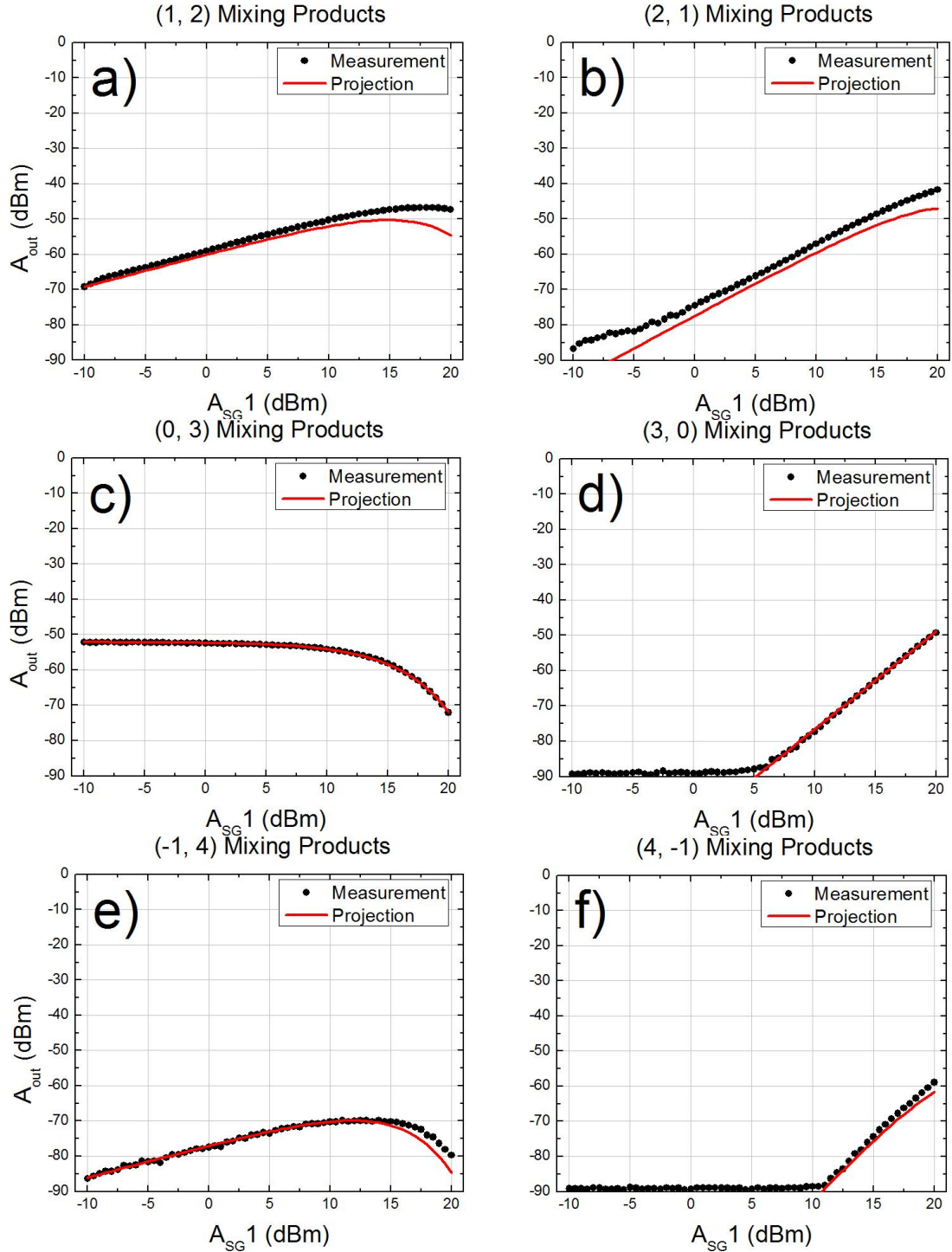
Figure F.5 Plots of the output power of six mixing product peaks vs. the output power of one signal generator in a two-tone mixing setup performed on a CNT FET ($W = 100$ μm, $L = 10$ μm, $G = 8$ μm). The black dots are the measurements taken and the red lines are the expected mixing product amplitudes based on a single expansion term per peak. The other signal generator was held at a fixed output power of 15 dBm. The output frequency was 75.5 GHz + 300 kHz, which is three times the input frequency of the first signal generator.

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