

ABSTRACT

Title of Thesis: A NOVEL COMPRESSING ANALOG-TO-DIGITAL CONVERTER

Keir Christian Lauritzen, Master of Science, 2005

Thesis Directed By: Professor Martin C. Peckerar, Electrical and Computer Engineering

Analog-to-digital converters form the backbone of many real world systems. A compression and expansion (companding) capability is a useful tool to increase the signal-to-noise ratio of many of these applications. Frequently, power-signal systems utilize analog compression to simplify signal processing. A novel compressing high-speed converter is presented in this thesis. The converter described here has a natural compressing transfer function of $f(x)=1-1/x$. The converter is a variation on Flash conversion, so it is high speed, with a sampling frequency of 80MHz. A four bit implementation of this converter was manufactured on a 0.5 μ m CMOS process with an area of 0.018mm². The power consumed was 50mW on a first pass design. The compressing converter will to scale with process improvements. The converter desensitizes the linear region to reference mismatch, and arbitrary compressing transfer functions can be obtained.

A NOVEL COMPRESSING ANALOG-TO-DIGITAL CONVERTER

by

Keir Christian Lauritzen

Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Master of Science
2005

Advisory Committee:

Professor Martin Peckerar, Chair
Professor Pamela Abshire
Professor Neil Goldsman

©Copyright by

Keir Christian Lauritzen

2005

Dedication

Dedicated to my family, Mom, Kjeld, and Dad who keep me going. Dedicated to my grandparents, Vernon and Catherine Gable, for providing me inspiration throughout my life.

Acknowledgements

The author would like to thank the support of his adviser Dr. Martin Peckerar, with his help throughout this project. In addition, a thank you goes to the thesis defense committee of Dr. Neil Goldsman and Dr. Pamela Abshire, as well as the entire ECE department. Seokjin Kim proved invaluable in his help with testing, as well as Dr. F. Keith Perkins at the Naval Research Lab. Tyler Onufert was a great help on the encoder work. Ji Luo answered many layout questions. The author would also like to thank Dr. Dan Radack the program manager at DARPA for on this project. The US Navy supported the author for much of the initial work and has filed the patents. Katherine Lauritzen helped with editing the paper.

Contents

1	Introduction	1
2	Background	4
2.1	Analog-to-Digital Converter Characteristics	4
2.1.1	Quantization Error	5
2.1.2	Dynamic Range	5
2.1.3	Signal-to-Noise Ratio (SNR)	7
2.1.4	Power Consumption	8
2.1.5	Propagation Delay	9
2.2	Appropriate Signals	9
2.3	Sample ADCs	11
2.3.1	Non-linear Architectures	11
2.3.2	Flash Analog-to-Digital Converter	12
3	A New Compressing Architecture Based on the “Flash” Principle	15
3.1	Description	15
3.2	Ideal Converter Characteristics	17

3.2.1	Transfer Function	17
3.2.2	Quantization Error (Qe)	18
3.2.3	Resolution	22
3.2.4	Signal-to-Noise Ratio (SNR)	24
3.2.5	Dynamic Range	28
3.2.6	Optimal Signal	30
3.2.7	Comparing Compressing and Linear Converters	31
3.2.8	Varying Parameters	33
3.2.9	Generating Arbitrary Transfer Functions	34
3.3	Device Characteristics	36
3.3.1	Static and Dynamic Power Consumption	36
3.3.2	Transient Delay	41
4	Implementation	43
4.1	Analog Circuit Design	43
4.1.1	Reference Ladder	43
4.1.2	Input Buffer	51
4.1.3	Sample/Hold	57
4.1.4	Comparators	59
4.2	Digital Circuit Design	75
4.2.1	Encoders	75
4.2.2	Error correction	87
4.2.3	Output Buffer and Flip-Flops	92

4.3	Final Mixed-Signal Circuit	95
5	Testing	111
5.1	Test setup	112
5.2	Measured Results	114
5.2.1	DC Transfer Function	114
5.2.2	Power Consumption	122
5.2.3	Propagation Delay	122
6	Architectural Analysis and Improvements	123
6.1	Division of Input Signal	123
6.2	Signal-Dependent Transient Characteristics	125
6.3	Other Optimizations	127
6.4	Applications	128
7	Conclusion	132
A	Derivation of V_{noise}	134

List of Figures

2.1	Quantization Error of an Ideal Linear ADC	6
2.2	Simple Flash ADC	14
3.1	Schematic Drawing of Compressing ADC	16
3.2	Transfer Function plotted for the continuous and digital outputs . .	19
3.3	Quantization Error	21
3.4	Q_e normalized to give each bit zero mean	22
3.5	Resolution of each bit	23
3.6	Derivation of the PDF of Q_e	25
3.7	Q_e Probability Density Function	26
3.8	Signal-to-Noise Ratio (dB) vs. V_{in} , the markers are the number of bits.	29
3.9	Signal vs. Noise for each bit	29
3.10	Optimally signal for the standard converter found using histogram equalization	30
3.11	Quantization Noise (Normalized) for a Linear and Compressing Converter for the Optimal Signal	31

3.12	Quantization Noise (Non-Normalized) for a Linear and Compressing Converter for the Optimal Signal	32
3.13	SNR for N=4,5,6	35
3.14	Transfer Function for N=4,5,6	35
3.15	Transfer Function if last resistor is 4R with all other R	36
3.16	Transfer Function of Logarithmic ADC using Compressing Architecture	37
3.17	Transfer Function of Linear ADC using Compressing Architecture	37
4.1	DC sweep resistive ladder	45
4.2	Layout of the Resistors	47
4.3	Cross Section of Poly-Poly Capacitor	48
4.4	A “DC” Sweep of the Capacitive Ladder	49
4.5	DC Sweep of Capacitive Ladder Zoomed In	49
4.6	Layout of the Capacitor	50
4.7	Input buffer schematic	52
4.8	Transfer Function of Input Buffer with an $8k\Omega$ Load	54
4.9	Currents of Input Buffer	56
4.10	Layout of Input Buffer	56
4.11	Transient Response of the Input Buffer	57
4.12	Sampling switch schematic	58
4.13	Layout of Sample Switch	60
4.14	Schematic of NMOS Comparator showing stages	61

4.15	Decision Circuit used in the Comparators	65
4.16	Decision Circuit biased to work with output buffer	66
4.17	Schematic of PMOS Comparators	67
4.18	DC Sweep of NMOS Comparator to find the gain	70
4.19	DC Sweep of PMOS Comparator to find the gain	70
4.20	Transient performance of NMOS Comparator	72
4.21	Transient performance of PMOS Comparator	73
4.22	Power Supply Current of NMOS Comparator during Transient Analysis	73
4.23	Layout of NMOS Comparator	74
4.24	Layout of PMOS Comparator	74
4.25	Layout of PMOS Comparator	75
4.26	ROM Structure	79
4.27	A 1-of-N Converter	80
4.28	Schematic of (a) a Binary Encoder and (b) the L-Encoder	86
4.29	Schematic of Encoder Used	88
4.30	Delay of Output Bits of the Encoder	88
4.31	Power of Encoder	89
4.32	Layout of the encoder	89
4.33	Schematic of the Error Correction	90
4.34	Layout of Error Correction	91
4.35	Schematic of a D Flip-Flop	92
4.36	Layout of a D Flip-Flop	93

4.37	Schematic of the Output Buffer	94
4.38	Layout of the Output Buffer	94
4.39	Schematic of Digital Backend	95
4.40	Schematic of Chip-B Analog Frontend	96
4.41	Schematic of Chip-D Analog Frontend	97
4.42	Bitwise Output of ADC A (Vref=100mV)	98
4.43	Lowest Bitwise Output of ADC A (Vref=100mV)	99
4.44	Bitwise Output of ADC A (Vref=150mV)	99
4.45	Bitwise Output of ADC A (Vref=500mV)	100
4.46	Transfer Function of Chip B	100
4.47	”DC” Analysis of Chip D	101
4.48	Transient Analysis of Chip B	102
4.49	Power Supply Current of Chip B	103
4.50	Capacitive Ladder Transient Response	104
4.51	Layout of Chip B Frontend	104
4.52	Layout of Chip D Frontend	105
4.53	Close-up Layout of Input of Chip B	105
4.54	Close-up Layout of Input of Chip D	106
4.55	Layout of the Digital Backend	106
4.56	Layout of the Complete Chip A	107
4.57	Layout of the Complete Chip B	107
4.58	Layout of the Complete Chip C	108
4.59	Layout of the Complete Chip D	108

4.60	Layout of Chip A showing Separate Power Lines	110
5.1	Pin-outs of ADC-A and ADC-B	112
5.2	Pin-outs of ADC-C and ADC-D	113
5.3	DC Sweep of Chip A, $V_{ref} = 1V$	115
5.4	DC Sweep of Chip A, $V_{ref} = 1V$, zoomed	115
5.5	DC Sweep of Chip A, $V_{ref} = 450mV$	116
5.6	DC Sweep of Chip B, $V_{ref} = 3.6V$, Latched outputs	116
5.7	DC Sweep of Chip B, $V_{ref} = 3.6V$, Unlatched outputs	117
5.8	1011 to 1100 Transition with Clock	118
5.9	Transfer Function at $V_{dd} = 2V$	119
5.10	Bitwise Output at $V_{dd} = 2V$	120
5.11	Bitwise Output at $V_{dd} = 3V$	120
5.12	Bitwise Output at $V_{dd} = 4V$	121
5.13	Bitwise Output at $V_{dd} = 5V$	121
6.1	Schematic of the Inverse DAC	130
A.1	Derivation of V_{noise}	135

List of Tables

3.1	Quantization Error	20
3.2	Summary of SNR Results	28
3.3	SNR Comparison for N=4,5,6	34
3.4	Resistor Values for Various Transfer Functions	38
3.5	Anticipated Device Characteristics	40
4.1	Summary of the Four Implementations Components	44
4.2	Comparison of Resistors Available	45
4.3	Comparison of Comparator Performance	71
4.4	Comparison of Encoder Characteristics	76
4.5	Truth Table of Encoder	78
4.6	Bubble Errors of a Standard Binary ROM	81
4.7	Comparison of Encodings Available	83
4.8	Comparison of the Encoding Scheme Conversion to Binary	87
4.9	Truth Table of the Manglesdorf Error Correction	90

Chapter 1

Introduction

The analog-to-digital converter is an integral part of many of today's most visible integrated systems. Applications range from audio recorders to satellite systems. The real world operates continuously in time and value. Analog components take their name from the fact that they have outputs which are analogous to the real world. Digital signals are discrete, or guaranteed values, and they are generally used by computers and processors of all sorts. Analog to digital converters (ADCs) form the boundary between the analog and digital worlds. ADCs convert a signal from the analog domain to the digital domain and are integral parts of any digital system wishing to take information from the real world.

A novel compressing ADC is presented here. It is based on Flash conversion, with a natural transfer function of $1 - 1/x$. This architecture has many applications for signal processing, such as speech and image signals. The compression lends itself to working with power signals such as radar and sonar. The small die size

and ability to use advanced power management techniques allows the design to be used in small smart sensors. The circuit is characterized by high speed and low power and shows great promise in the applications listed above.

In chapter 2, a background in ADCs is given with some analysis of linear converters. The use of compression in signal processing is discussed as a way to increase the signal to noise ratio over a large dynamic range. A brief overview of other nonlinear converters appearing in the literature is given and Flash conversion is discussed.

In chapter 3, the architecture is analyzed from a theoretical standpoint with calculations for important characteristics, including quantization error, signal-to-noise ratio, and dynamic range. Each of the design parameters are analyzed with regard to their effects on the transfer function and alternative reference ladders are shown to enable the generation of arbitrary compressing functions. The device characteristics are then analyzed from a high-level standpoint, to better understand the architecture. This analysis provides key insights into the fundamental design characteristics and helps to focus the optimization of the design.

In chapter 4, the physical implementations of the circuits are described. Four implementations were developed to test many of the permutations of the architecture, with the main differences being different reference ladders, input buffers, and comparators. Each subcomponent is described with data from simulation and layout. Several of the component circuits are developed in-depth, such as the encoder and comparators. These components were then brought together and simulated as a system. The encoder section includes a detailed description of many of the en-

coder circuits available, as part of on going work by the author.

In chapter 5, the test setup is described including the equipment available in the test facility. The physical devices were manufactured through MOSIS on the AMI $0.5\mu m$ process. The test results are shown with a focus on proving that the architecture is compressing. The power consumption was measured as well as preliminary speed results.

In chapter 6, many of the issues that were found in the device are discussed. Possible solutions are presented to each of these and future work outlined. Overall architectural enhancements and sample applications are also presented.

A novel compressing architecture has been fully developed from theoretical overview to a full physical implementation in submicron CMOS. Much of this theoretical analysis is appropriate for other nonlinear converters. This converter is the fastest integrated compressing ADC in the literature as known to the author. This is a proven member of a class of single reference ADCs, which has been investigated to eliminate common mode issues. Due to its small size and high bandwidth the converter is appropriate for integration with sensor systems.

Chapter 2

Background

The analog-to-digital converter described in this thesis is a nonlinear, compressing converter. This chapter seeks to provide background for this architecture, by discussing the use of compression in companding (compressing/expanding) signal processing. A discussion of previously designed non-linear converters is provided, as well as an overview of some of the characteristics and architectures of similar ADCs.

2.1 Analog-to-Digital Converter Characteristics

An analog-to-digital converter (ADC) takes an analog input and outputs a digital word, which represents the signal level of the input. An ADC can be viewed as a black box that performs this function. We will begin by discussing some of the black box characteristics, then discuss some of the silicon box characteristics.

The characteristics developed will be limited to those applicable to the compressing ADC. There are many excellent discussions of these characteristics in much greater detail [37, 38, 39].

2.1.1 Quantization Error

If the analog input signal is quantized using an ideal ADC and then converted back to an analog signal using an ideal DAC the output will look like a staircase as in Figure 2.1. The difference between the original and quantized signal is the quantization error. The more bits there are to represent the original signal, the lower the quantization error. Quantization error is a loss of information that can not be recovered or reconstructed.

From a signal processing standpoint, this quantization stage is simply considered as adding noise to the signal to be processed. This noise can be treated as random as long as Bennett's Criteria are satisfied [40]. This can be summarized as a signal, which is equally likely to be on any valid bit. In a linear ADC, the quantization is the same on all bits therefore it is straightforward to calculate the RMS value of $Q_{e,RMS} = \sqrt{\frac{V_{LSB}}{12}}$.

2.1.2 Dynamic Range

The dynamic range of an ADC is the range of signal values that the architecture can operate on (before saturation) divided by the smallest signal that the ADC can detect. The dynamic range for a linear converter is equal to the total voltage

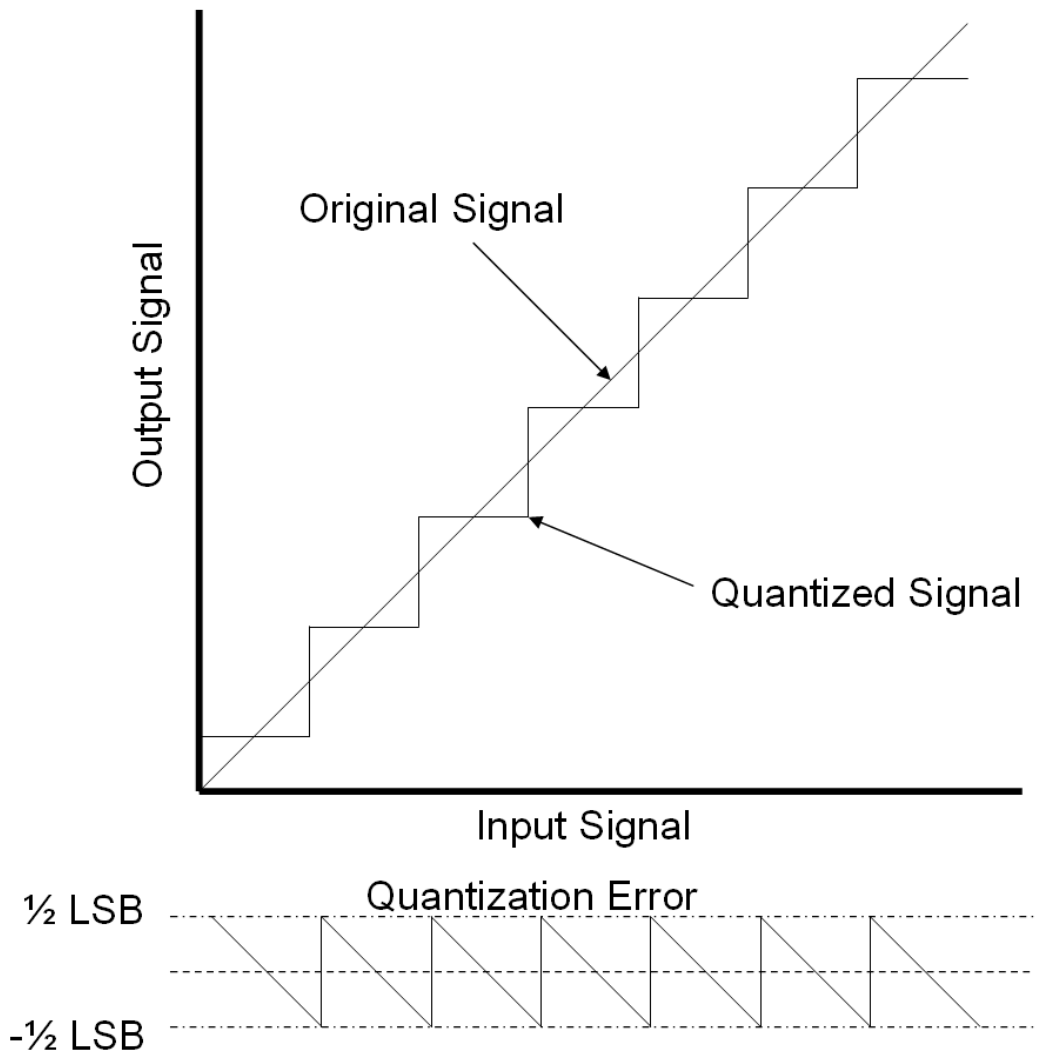


Figure 2.1: Quantization Error of an Ideal Linear ADC

range, $(2^N - 1) V_{LSB}$ divided by the smallest voltage it can resolve V_{LSB} , for a final dynamic range of $(2^N - 1)$. This is typically written in decibels.

2.1.3 Signal-to-Noise Ratio (SNR)

The SNR is a ratio of the maximum signal divided by the quantization noise. It must be noted that the only noise considered in this definition is quantization noise, not thermal noise or any other type of noise or distortion. These other factors are considered under signal-to-noise plus distortion ratio (SNDR). To calculate the SNR, first consider the RMS value of the maximum sinewave that could be fed into the ADC. The amplitude would be $\frac{V_{max}}{2}$, so the RMS value is $\frac{V_{max}}{2\sqrt{2}}$. V_{max} is the same as discussed in dynamic range, $(2^N - 1) V_{LSB}$. This makes the final RMS value $\frac{(2^N - 1)V_{LSB}}{2\sqrt{2}}$. In section 2.1.1, the RMS value of the quantization noise was found. Combining these two results yields the final SNR for a linear converter.

$$SNR = \frac{(2^N - 1) V_{LSB}}{2\sqrt{2}} \cdot \frac{\sqrt{12}}{V_{LSB}} = \frac{\sqrt{12}}{2\sqrt{2}} \cdot (2^N - 1) \quad (2.1)$$

One thing to notice from this derivation is that the quantization noise remains constant for any suitably-random signal. The signal strength, however is not a constant, so if the average signal strength is lower, then the actual SNR will be lower than this theoretical maximum.

The question naturally arises, Why not use a squarewave since the RMS value would increase the SNR? A sinewave is generally used since it is suitably random,

i.e. all output values are present, if it is fast enough. Waveforms that approach a squarewave are not random enough, since the likelihood of a squarewave being on a middle transition are much lower than at the flat parts of a square wave. The voltage probability density function (PDF) of a sinewave is not truly evenly distributed[41], but it will still work for this definition.

2.1.4 Power Consumption

Power consumption is defined as the power that the chip uses and dissipates as heat. In the case of analog-to-digital converters, unlike amplifiers that source a load, almost no power leaves the chip, so this can be found by measuring the power supply current and voltage. Typically, the current is measured since the voltage remains constant.

Static power consumption is measured when there is no input signal and is meant to find DC bias power and leakage power. Dynamic power consumption is found by inputting a large, wide bandwidth signal. The goal is to cause as many components to switch as fast as possible. This would represent the worst case average dynamic power consumption. In addition, with a sensitive enough power supply, through simulation or analysis, peak power consumption may be found which measures large transient spikes. Peak consumption is important for determining overload conditions as well as when designing power supplies.

2.1.5 Propagation Delay

Propagation delay is the maximum amount of time it takes for an input signal to be processed and show up at the output. This is typically measured using a known longest path. With the propagation delay found, the sampling clock can be determined by taking the reciprocal. If there is any pipelining, then the clock may be higher and will need to be determined by the designer.

It is crucial to remember the difference between sampling rate and analog bandwidth. Analog bandwidth is the maximum speed that the ADC can accurately digitize. For Nyquist rate devices, such as this, the analog input bandwidth must be less than half the sampling frequency, as required by Nyquist sampling theory [44]. If the design is pipelined, uses feedback, or is oversampled then the analog bandwidth goes down compared to the sampling rate.

2.2 Appropriate Signals

There are three potential uses for a compressing ADC. The first is from a signal processing standpoint and the use of companding. The second is for linearizing power signals, and the third use is to linearize arbitrarily non-linear sensors to simplify signal processing.

Companding is the process of compressing the analog input signal, performing signal processing, and then expanding the signal back to a linear form, in either digital or analog domain. Companding is useful when the probability of low amplitude signals is greater than that of large amplitude signals. In a linear

quantizer the signal-to-noise ratio (SNR) decreases as the signal level goes down, while it remains high over a large signal range with companding. Companding is a well-understood signal processing technique that the reader is encouraged to explore further [1, 43, 2, 46].

Speech processing is typically cited as an example, which benefits from companding. A large dynamic range is necessary to capture the nuance of the human voice, but most speech occurs at a low level resulting in a skewed signal PDF. This can be compensated for by using companding. In fact companding was used in many telephone systems. Two classes of compressors became common because of this, μ -law and A-law (Equations 2.2 and 2.3). V is the overload voltage of the converter, μ and A are parameters, which determine the amount of compression and x is the input signal.

$$F(x) = V \frac{\log(1 + \mu x/V)}{\log(1 + \mu)} \quad (2.2)$$

$$F(x) = \left\{ \frac{Ax}{1 + \log A}, 0 < x < V/A \right.$$

$$\left. \frac{V + V \log(Ax/V)}{1 + \log A}, V/A < x < V \right. \quad (2.3)$$

Power signals are where the signal strength rises as a square-law, exponential, or other higher order function. These signals have a large dynamic range, but the accuracy needed on upper bits is lower than on the lower bits. The most simple

case that can be discussed is the power through a resistor, which will rise as the square of the current. If the power is measured without compression, and current is the signal of interest, a change in power by a factor of 4 will have meant a change of signal strength of a factor of 2. The linear digitizer will have still have been required to have dynamic range capable of measuring the factor of 4 change, when there was only a factor of 2 change in the signal strength. With compression, the digitizer could have been limited to a factor of 2 range, which would reduce the complexity of the digitizer.

Sensors often have nonlinear characteristics where the electrical signal increases faster than the real world signal being measured, such as pressure. A compressing ADC can be used to reduce the dynamic range requirements of the digitizer and to linearize the device reducing the signal processing demands.

2.3 Sample ADCs

In this section, competing technologies for compression are described. Flash conversion is described since that architecture is closely related to the novel compressing converter presented in this thesis.

2.3.1 Non-linear Architectures

A compressing ADC is proposed in [3], which is a modification of a successive-approximation ADC. Successive-approximation works by calculating the MSB, then subtracting it from the original signal if it is a “1”. The second most signifi-

cant bit is calculated and then subtracting if necessary, and so on. The compressing version uses a R-2R ladder to calculate the bits to be compared against. The use of a successive-approximation architecture places the circuit into the medium accuracy, medium speed category. A further description of the successive-approximation ADC can be found in [42].

Lygouras developed a nonlinear converter with a digitally configurable transfer function[4]. The design converted the analog signal into pulse width modulation. The pulse width modulation was sent into a ROM that had been programmed with the nonlinear function. This technique is heavily dependent upon the speed capabilities of logic used. This design is very flexible with regard to the transfer function. Further enhancements could use FPGA structures to modify the design to morph the transfer function on the fly.

Another non-linear ADC has been developed which uses the exponential curve of bipolar transistor to scale the output currents from current mirrors[7]. The scaling is performed by increasing the emitter area and requires accurate current mirrors. This design could also be used in CMOS by using subthreshold operation. Other non-linear ADCs have been demonstrated[6, 5].

2.3.2 Flash Analog-to-Digital Converter

There are three broad categories of ADCs: low resolution, wide bandwidth ADCs, high resolution narrow bandwidth ADCs, and noise-shaping ADCs. The compressing converter is part of the wide bandwidth class. The fastest and one of the oldest converters is the Flash ADC. The Flash converter is composed of three

main sections: a reference ladder, quantizers, and an encoder. The reference ladder is typically a resistive ladder, which sets up the voltages that the input will be compared with. The quantizers, or comparators output a “1” if one input is larger and “0” if the other is larger.

The output of the comparators is thermometer code, a code such as 00000111111111, where the position of the 01 transition tells the output. To get the thermometer code to something more usable, such as binary, an encoder is used. The flash converter is fastest because the outputs are all processed in parallel. The downside is the number of comparators and the large input capacitance. The number of comparators increases the power consumption and the die area. The large input capacitance puts an upper limit on the analog bandwidth.

A compressing converter can be done if the reference ladder is changed. A scaled ladder can be achieved by doubling the resistance value of each additional resistor. This leads to very large resistance values quickly, which can be difficult to design with a higher tolerance. It could also be done by using an R-2R ladder. An R-2R ladder can have a larger power consumption since the ladder appears to the power supply as a resistance R.

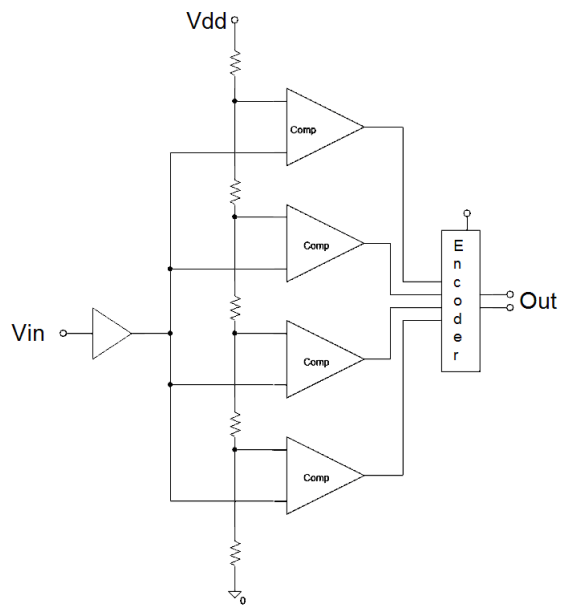


Figure 2.2: Simple Flash ADC

Chapter 3

A New Compressing Architecture Based on the “Flash” Principle

3.1 Description

The compressing converter described in this thesis is a variation on Flash conversion. In this variation the input signal is fed to the reference ladder and the other input of the comparators is connected to a single reference voltage. This difference alone makes the circuit compressing instead of linear. The topology is composed of the same three stages as Flash: the input stage and reference ladder, quantization stage, and encoder stage as shown in Figure 3.1.

The input stage includes a buffer, optional sample and hold, and the reference ladder. The input signal comes into the circuit through the buffer which is used to isolate the input from the rest of the circuit. The buffer drives the reference

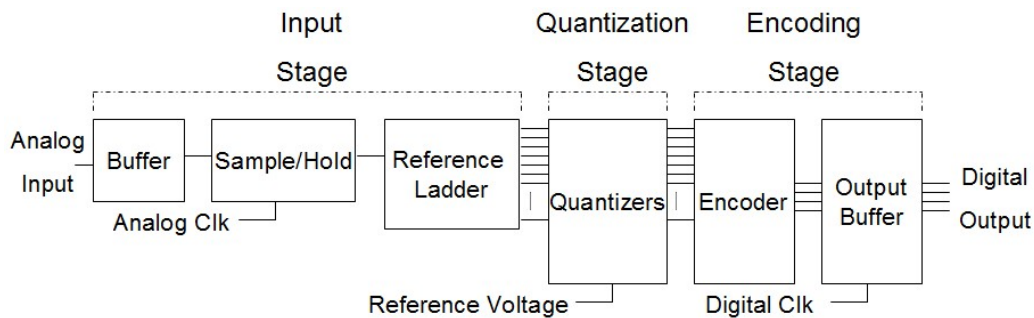


Figure 3.1: Schematic Drawing of Compressing ADC

ladder which is a low impedance load. The sample and hold stores the input signal allowing the rest of the circuit to operate on it. This increases the sampling speed of the circuit. This can be omitted in the early stages of development, if functionality is a driving factor, or if other techniques are pursued. The reference ladder is a series connection of impedance elements. The reference ladder divides the input signal into a set of node voltages which are a fraction of the original input signal.

Each node of the reference ladder is connected to one of the inputs of the quantizers. Each quantizer accepts two inputs and compares them, outputting a digital high or low depending on which value is greater. The two inputs are a node voltage and the reference voltage. $2^N - 1$ analog inputs become $2^N - 1$ digital outputs. The output of the quantization stage is thermometer code, which is a series of high and low bits (000000111111) where the important information is the 01 transition. This form of code is called thermometer code and is an inefficient method of encoding, requiring N bits for N number of outputs. These parallel outputs are passed to the encoding stage.

The encoding stage takes the 2^N inputs, finds the 01 transition, and outputs a binary number which indicates the bit location of the 01 transition. The binary encoding is a much more efficient encoding scheme than thermometer code. The encoding stage also includes output buffers and latches, to get the signal from the circuit to the outside world.

3.2 Ideal Converter Characteristics

The previous section gave a very high level description of the signal path. In this section, the discussion will focus on how the circuit operates on the signal, some general characteristics of the circuit, and the affects of the reference ladder on circuit output.

3.2.1 Transfer Function

To find the transfer function, the reference ladder must be defined. For the initial consideration, for both mathematical convenience and since it was the design implemented, the reference ladder will divide the input signal into equal fractions . This is a completely arbitrary condition and any fraction could be used.

The voltage at any output node is going to be equal to the number of the node subtracted from the total number of nodes divided by the number of nodes. This is shown in Equation 3.1. The output of the comparator switches when the node voltage equals the reference voltage. This switching increases the digital output by one as shown in Equation 3.3.

$$V_n = \frac{2^N - n}{2^N} \cdot V_{in} \quad (3.1)$$

$$V_n = V_{ref} \quad (3.2)$$

$$V_{ref} = \frac{2^N - n}{2^N} V_{in} \quad (3.3)$$

$$\frac{V_{ref}}{V_{in}} = \frac{2^N - n}{2^N} = 1 - \frac{n}{2^N} \quad (3.4)$$

$$\frac{n}{2^N} = 1 - \frac{V_{ref}}{V_{in}} \quad (3.5)$$

Equations 3.1 through 3.5 show the full transfer function. The $\frac{n}{2^N}$ is the digital output. A plot of this function is shown in Figure 3.2.

3.2.2 Quantization Error (Qe)

The quantization error of the linear converter is the same for each bit. With the nonlinear converter the quantization error increases with each increased bit. The maximum quantization error occurs immediately before each digital transition. Therefore the maximum quantization error of each bit is the difference between each switching voltage. This can be calculated using Equation 3.8. The switching voltages of a 4-bit encoder with a $V_{ref}=100\text{mV}$ is shown in Table 3.1.

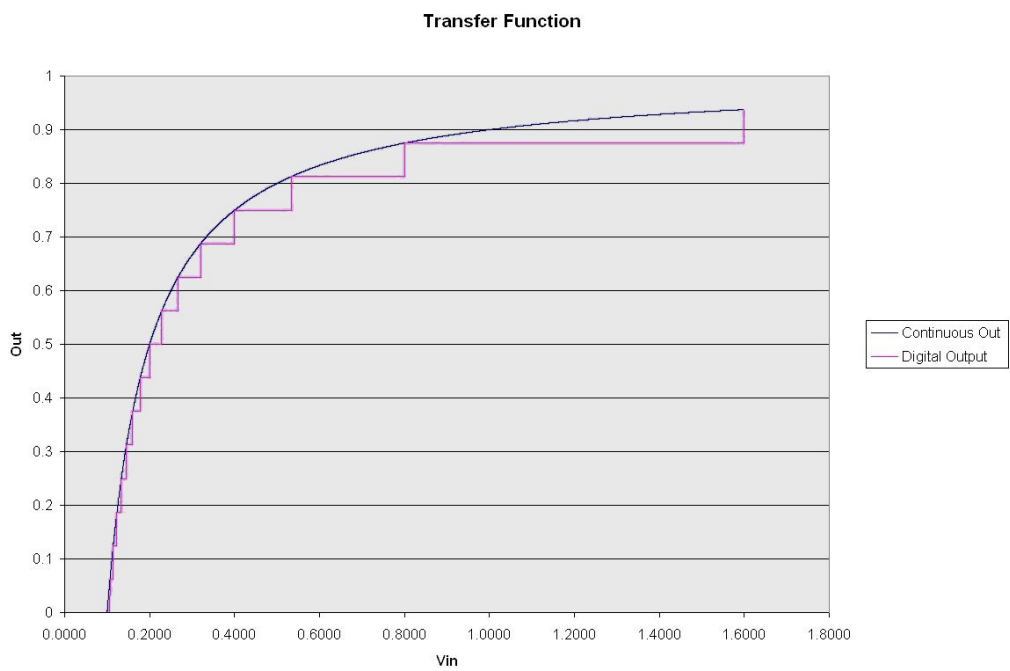


Figure 3.2: Transfer Function plotted for the continuous and digital outputs

Digital Bit	Vin	Vdelta	Qe
0	0	0	0
1	6.7	6.7	6.7
2	14.3	7.6	7.6
3	23.1	8.8	8.8
4	33.3	10.2	10.2
5	45.5	12.2	12.2
6	60	14.5	14.5
7	77.8	17.8	17.8
8	100	22.2	22.2
9	128.6	28.6	28.6
10	166.7	38.1	38.1
11	220	53.3	53.3
12	300	80.0	80.0
13	433.3	133.3	133.3
14	700	266.7	266.7
15	1500	800.0	800.0

Table 3.1: Quantization Error

$$\Delta V_{bn} = \frac{V_{ref}}{1 - \frac{n}{2^N}} - \frac{V_{ref}}{1 - \frac{n-1}{2^N}} \quad (3.6)$$

$$\frac{V_{ref}}{\frac{2^N-n}{2^N}} - \frac{V_{ref}}{\frac{2^N-n-1}{2^N}} = \frac{2^N \cdot V_{ref}}{2^N - n} - \frac{2^N \cdot V_{ref}}{2^N - n + 1} \quad (3.7)$$

$$\Delta V_{bn} = \frac{2^N \cdot V_{ref}}{(2^N - n)(2^N - n + 1)} \quad (3.8)$$

$$\Delta V_{b0} = V_{LSB} \cong \frac{V_{ref}}{2^N} \quad (3.9)$$

The continuous transfer function and the digital transfer function were cal-

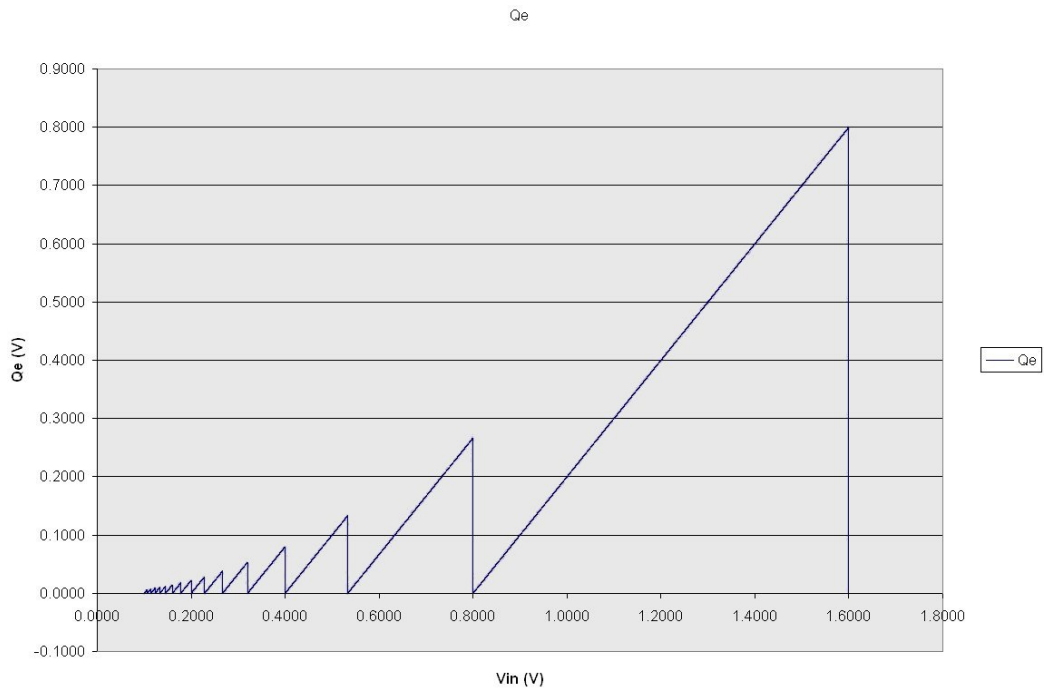


Figure 3.3: Quantization Error

culated and plotted previously. The difference at each step was calculated and plotted in Figure 3.3. There are two important characteristics that can be noticed from this plot; the Qe is nearly linear for each step and the Qe increases with each bit. Notice, the Qe increases very quickly after the 2^{N-1} bit, which will become very important when investigating SNR.

The Qe found in the previous step can be normalized around zero. This is equivalent to changing the continuous transfer function by a half-bit. This is a valid step since it does not change the shape or nature of the function. This normalized Qe is plotted in Figure 3.4.

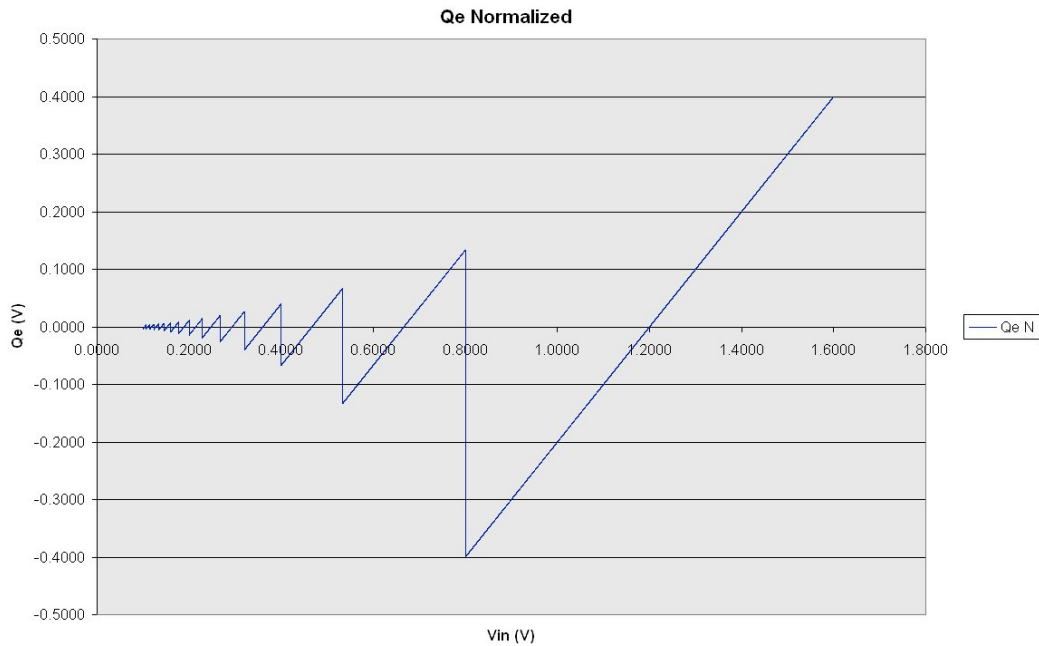


Figure 3.4: Q_e normalized to give each bit zero mean

3.2.3 Resolution

Quantization error, resolution, and SNR¹ are all interrelated and are often cited interchangeably. In the case on the compressing converter, SNR is separate from resolution. As Equation 3.9 shows, one of the characteristics of this architecture is the ability to resolve very small signals. Figure 3.5 shows the ratio of the bit step size over the least significant bit. Notice that the lowest bits all maintain a ratio near one with the LSB, which demonstrates the high resolution of the circuit on the lower bits.

¹Dynamic Range is also included in this group. This is due to the fact that for linear converter a bit increase results in a SNR and Dynamic Range increase of the dB, since they are both based on V_{total}/V_{LSB} .

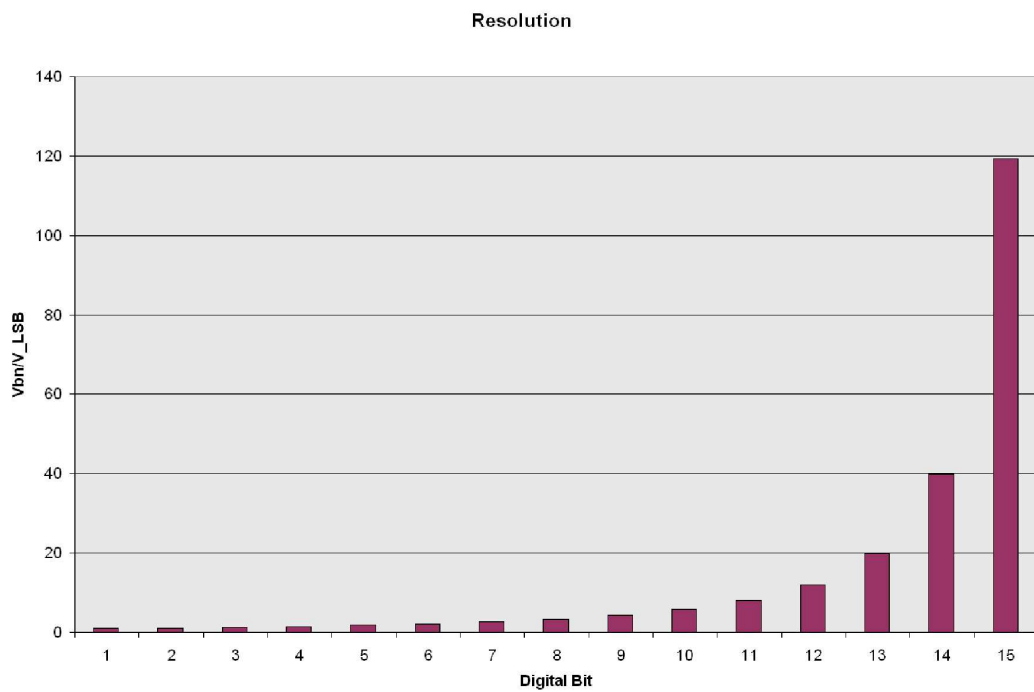


Figure 3.5: Resolution of each bit

This graph shows the factor that each bit is larger than the LSB. The first bits are all very close to 1 which leads to a high resolution.

3.2.4 Signal-to-Noise Ratio (SNR)

The calculation of signal to noise for the compressing converter follows the same procedure as for a linear converter. The noise and signal voltage are calculated separately.

Noise

To calculate the noise voltage we will begin by determining the probability density function (PDF) of the Q_e . For a linear converter the PDF is a uniform constant distribution. The PDF of the nonlinear converter will be a symmetric staircase. Looking at the normalized Q_e in Figure 3.4 we observed that the Q_e is increasing with each bit and that it is approximately linear. These two observations will be used to develop the PDF.

By using the linear observation, we can say that the probability of any error on bit is the same, i.e. if the output is a 2 the quantization error probability for all values for $-\frac{1}{2}V_{b2}$ to $\frac{1}{2}V_{b2}$. This yields a uniform distribution for each bit and the range is $-\frac{1}{2}V_{bn}$ to $\frac{1}{2}V_{bn}$. V_{bn} is less than V_{bn+1} , so PDF is narrower for the n bit than the $n + 1$ bit. Bennett's Criteria allows us to assume that the probability of any error is the same, so the height of each error bit will be the same. The PDF is generated by summing these individual bits. This procedure is illustrated in Figure 3.6.

Looking at Table 3.1 gives us the width of each step of the bit and the sum of all bit steps. Using these two pieces of information, it is possible to generate a

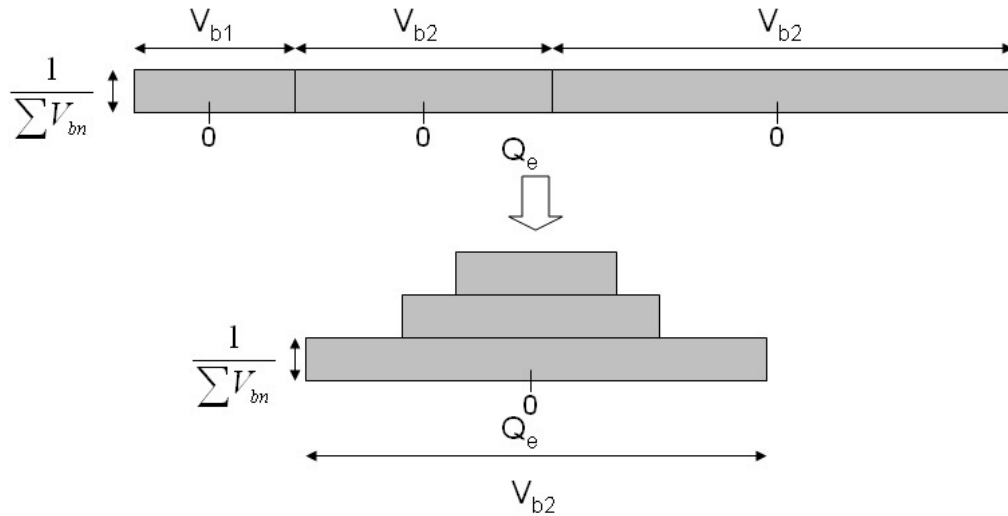


Figure 3.6: Derivation of the PDF of Q_e

graphical PDF of Q_e for the sample converter. The PDF is plotted in Figure 3.7.

Now that the PDF of Q_e has been calculated, it is straightforward (although tedious) to calculate the power of the signal. Once the power has been found the RMS noise voltage can be found simply by taking the square root. This calculation is performed in the Appendix in section A. The resulting noise voltage is Equation 3.10.

$$V_{noise,RMS} = \sqrt{\frac{1}{12} \frac{\sum V_{bn}^3}{\sum V_{bn}}} \quad (3.10)$$

Is this a reasonable result? If the circuit was linear and there was no variation over V_{bn} , the calculation would simplify to $\frac{V_{LSB}}{\sqrt{12}}$, which is the generally accepted expression for the noise voltage of a linear converter. This predicts our derivation is on the right track.

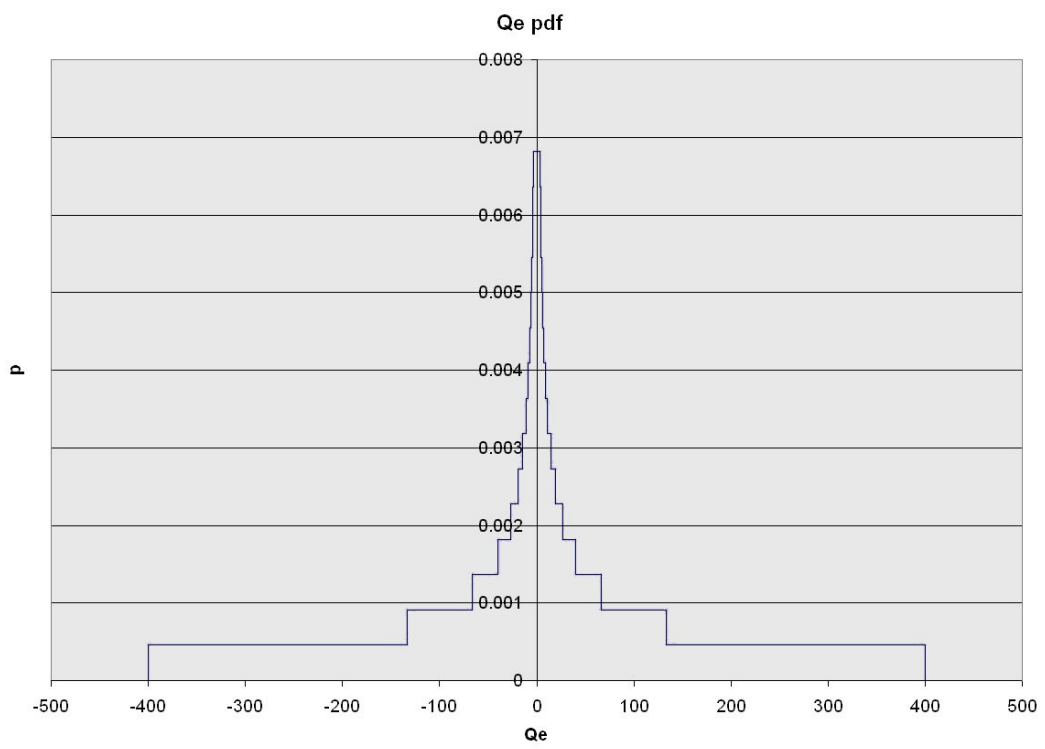


Figure 3.7: Q_e Probability Density Function

Signal

To calculate the signal voltage a sine wave will be assumed, with a $V_{p-p} = \sum V_{bn}$ to maximize the SNR. The signal therefore has a voltage of Equation. 3.11. This leads to a SNR of 3.13.

$$V_{sig,RMS} = \frac{V_{p-p}}{2\sqrt{2}} = \frac{\sum V_{bn}}{2\sqrt{2}} \quad (3.11)$$

$$SNR(n) = \frac{V_{sig,RMS}}{V_{noise,RMS}} = \frac{\frac{\sum V_{bn}}{2\sqrt{2}}}{\frac{\sum V_{bn}^3}{\sqrt{12} \sum V_{bn}}} \quad (3.12)$$

$$SNR(n) = \frac{\sqrt{12} (\sum V_{bn})^2}{2\sqrt{2} \sum V_{bn}^3} \quad (3.13)$$

The SNR has been found for signals that are input range limited. This derivation is the signal to noise ratio if the input range is limited to n-bits. That is SNR(3) has a signal amplitude of the voltage where the third transition occurs and is the average quantization noise over those 3 bits. This equation 3.13 can be used to find the full signal SNR, which is what is typically cited for linear converters, but is more interesting if we look at all bits. Values for the example converter are in Table 3.2. These values have been plotted in Figures 3.8 and 3.9. Figure 3.9 shows that the signal voltage increases faster than the noise voltage, which leads to a rapidly increasing SNR. The SNR increases very quickly from 0 to 8 bits, levels off and then slowly decreases. This calculation is equivalent, limiting the input signal to operating only over those bits. The SNR was also calculated by

Digital	V_{in} (mV)	ΔV (mV)	V_{noise} (mVrms)	V_{sig} (mVrms)	SNR	SNRdb
0	0	0	0	0	N/A	N/A
1	6.7	6.7	1.9	2.4	1.22	1.76
2	14.3	7.6	2.1	5.1	2.44	7.73
3	23.1	8.8	2.3	8.2	3.61	11.14
4	33.3	10.2	2.5	11.8	4.72	13.49
5	45.5	12.2	2.8	16.1	5.73	15.17
6	60	14.5	3.2	21.2	6.64	16.44
7	77.8	17.8	3.7	27.5	7.38	17.36
8	100	22.2	4.5	35.4	7.92	17.97
9	128.6	28.6	5.5	45.5	8.21	18.29
10	166.7	38.1	7.2	58.9	8.23	18.31
11	220	53.3	9.8	77.8	7.93	17.98
12	300	80	14.6	106.1	7.27	17.23
13	433.3	133.3	24.6	153.2	6.24	15.90
14	700	266.7	51.3	247.5	4.82	13.67
15	1500	800	172.3	530.3	3.08	9.77

Table 3.2: Summary of SNR Results

using a piecewise integration method and was found to be equivalent.

3.2.5 Dynamic Range

The dynamic range of ADC is the total voltage range the device can operate over divided by the smallest signal it can detect. The maximum voltage occurs when the device is at bit $2^N - 1$. This leads to a maximum voltage of $(2^N - 1) \cdot V_{ref}$. The minimum voltage is $\frac{V_{ref}}{2^N}$, the difference between the 0 and 1 transitions. This leads to a dynamic range of 3.14.

$$V_{DynamicRange} = \frac{V_{max} - V_{min}}{V_{LSB}} = \frac{(2^N - 1) \cdot V_{ref}}{\frac{V_{ref}}{2^N}} \approx 2^{2N} \quad (3.14)$$

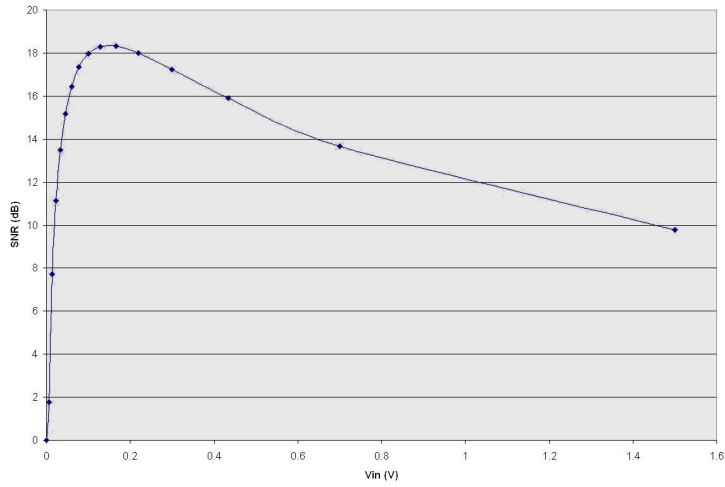


Figure 3.8: Signal-to-Noise Ratio (dB) vs. V_{in} , the markers are the number of bits.

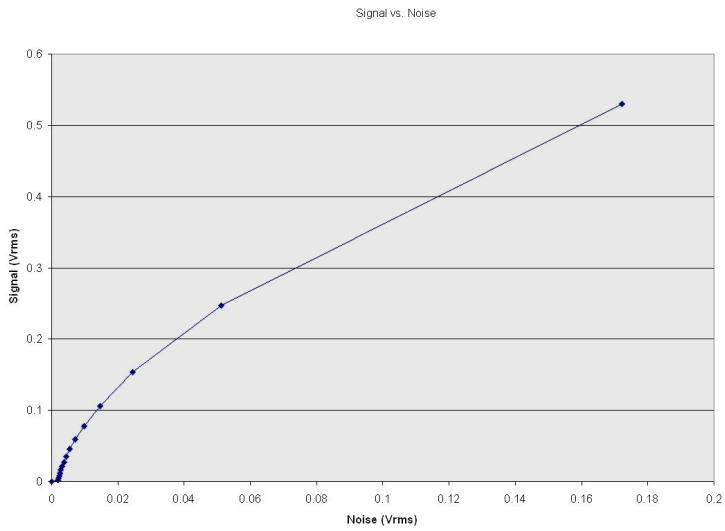


Figure 3.9: Signal vs. Noise for each bit

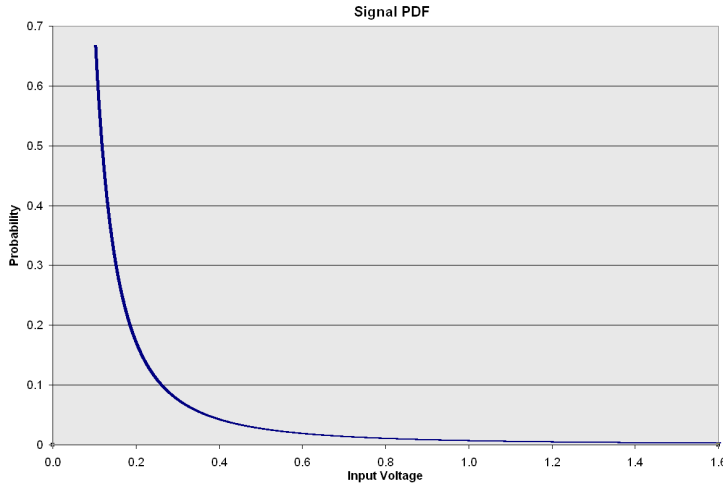


Figure 3.10: Optimally signal for the standard converter found using histogram equalization

3.2.6 Optimal Signal

It is clearly shown that this device works best for signals that spend most of the time around zero. It an attempt to quantify this optimal signal histogram equalization is used [47]. The basic idea is to have equal uses of each step of the transfer function. This is done by making the transfer function the cumulative density function (CDF) of the signal. This can then be differentiated and normalized to find the signal PDF, which is plotted in Figure 3.10.

$$CDF : 1 - \frac{V_{ref}}{V_{in}}, V_{ref} < V_{in} < 2^N V_{ref} \quad (3.15)$$

$$PDF : \frac{1}{2^N - 1} \frac{V_{ref}}{V_{in}^2} \quad (3.16)$$

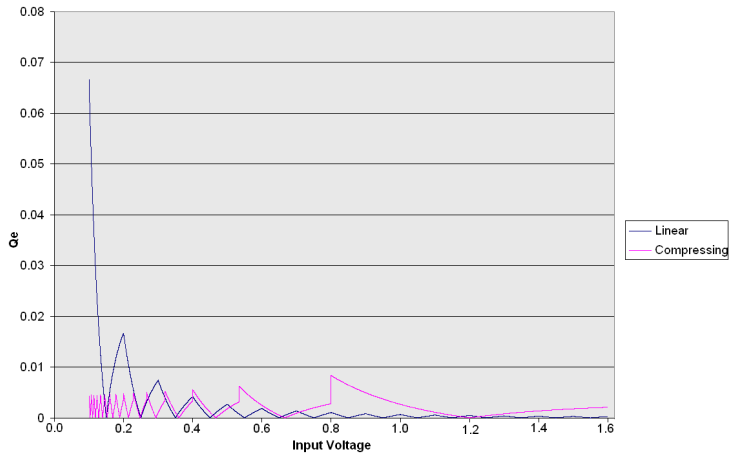


Figure 3.11: Quantization Noise (Normalized) for a Linear and Compressing Converter for the Optimal Signal

To calculate the SNR with this optimized signal, the average value of the signal was found, 42mV. The signal PDF was then multiplied by the Q_e and the RMS average of that was found, 1.08mV. The final SNR was 31.73dB, and was found to be the same as a linear converter with the same signal. However, inspection of the noise (Figures 3.11 and 3.12) shows that while the average maybe the same, the maximum noise is much lower for the compressing converter. This SNR is a substantial improvement over an equally distributed signal.

3.2.7 Comparing Compressing and Linear Converters

The calculated parameters allow us to make comparisons between the compressing converter and a linear converter based on criteria analyzed. Another characteristic that emerges is there are two main operating regimes; a nearly linear regime and a highly compressing regime. The transition occurs around bit 2^{N-1} and can

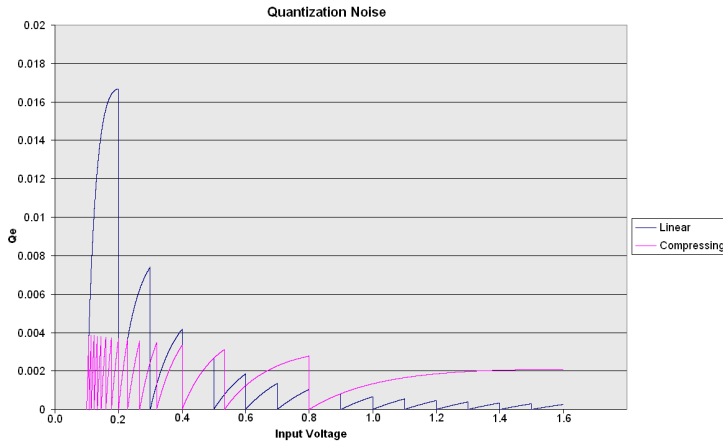


Figure 3.12: Quantization Noise (Non-Normalized) for a Linear and Compressing Converter for the Optimal Signal

readily be seen in Figures 3.2 and 3.13. The compressing regime covers about 2^N more input signal compared to the linear regime.

The transfer function shows how the first half maintains nearly a straight transfer function, before it quickly becomes compressing. A linear converter would continue in a straight line. The compressing converter increases the resolution in the linear region and reduces this in the compressing region. The compressing converter has a much higher resolution in the linear region than a linear converter with an equivalent dynamic range. The dynamic range of the compressing converter, $(2^{2N} - 1)$, is much better than a linear converter, $(2^N - 1)$. The dynamic range of a 4-bit compressing converter is equivalent to an 8-bit linear converter.

The SNR steadily increases until the linear-compressing transition point, just as a linear converter does. Around this bit the SNR levels off and eventually begins to decrease as the quantization noise begins to increase quickly. The maximum

SNR for the compressing converter is the same as a linear converter of one less bit, i.e. a 4-bit compressing converter has the equivalent SNR as a 3-bit linear converter. This makes sense since this is the linear regime of operation.

When the compressing converter is operated in the linear regime ($V_{in} < 2^{N-1}V_{LSB}$) the SNR remains high to accurately converting small signals. The device retains a large amount of dynamic range, equal to that of a linear converter with twice the number of bits, to capture and convert large signals.

3.2.8 Varying Parameters

If V_{ref} is increased the voltage range covered by each bit increases. Graphically, increasing V_{ref} causes the transfer function to spread out. The dynamic range increases by the factor that V_{ref} increased by. Equation 3.17 shows that if V_{ref} is decreased it acts as signal amplification with regard to the digital output.

$$\frac{n}{2^N} = 1 - \frac{\beta V_{ref}}{V_{in}} = 1 - \frac{V_{ref}}{\beta^{-1} \cdot V_{in}} \quad (3.17)$$

The reference ladder determines the shape of the transfer function and subsequently all of the other characteristics. The reference ladder divides the input signal into the proper fraction. The absolute values of the reference ladder do not matter for the purpose of signal characteristics, however they do matter in section 3.3.2. The number of bits was shown to determine the SNR, but does not have an effect on the overall transfer function. The maximum SNR of the 5-bit is 24.3dB compared to 18.3dB for the 4-bit converter. This difference of about

# of Bits	Maximum SNR (dB)	SNR (dB) at N
4	18.31	9.8
5	24.30	10.2
6	30.31	10.4

Table 3.3: SNR Comparison for N=4,5,6

6dB is the same as linear converters. The overall SNR, however, remains about the same. These values are compared in Table 3.3. The SNR plots are shown in Figure 3.13 and the transfer functions are shown in Figure 3.14. The transfer function is slightly different for each bit due to the actual voltages plotted. The transfer function of Equation. 3.5 is the same for all N.

3.2.9 Generating Arbitrary Transfer Functions

As was stated in the beginning of this section, the choice of equal fractions for the reference ladder was completely arbitrary, any other fraction could have been chosen. To illustrate this point several modifications have been made to the reference ladder and these have been simulated. The first potential change was done by making the final resistor in the chain 4 times the other resistors. This has the effect of making the transfer function “less compressing” as shown in Figure 3.15.

More traditional implementations can be realized with this approach. A logarithmic ADC, as shown in Figure 3.16, was made using very small variations from the basic compressing converter (about a factor of 2). A linear ADC (Figure 3.17) was implemented by making extreme variations to the base reference ladder. Not only does this show the flexibility of the architecture, but it also shows that

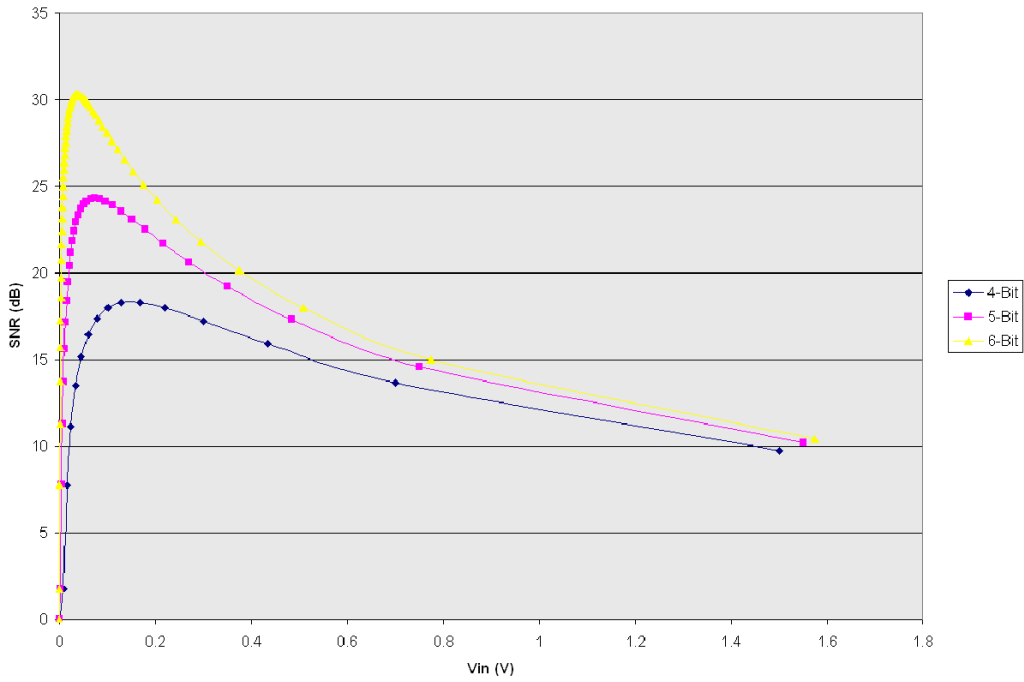


Figure 3.13: SNR for N=4,5,6

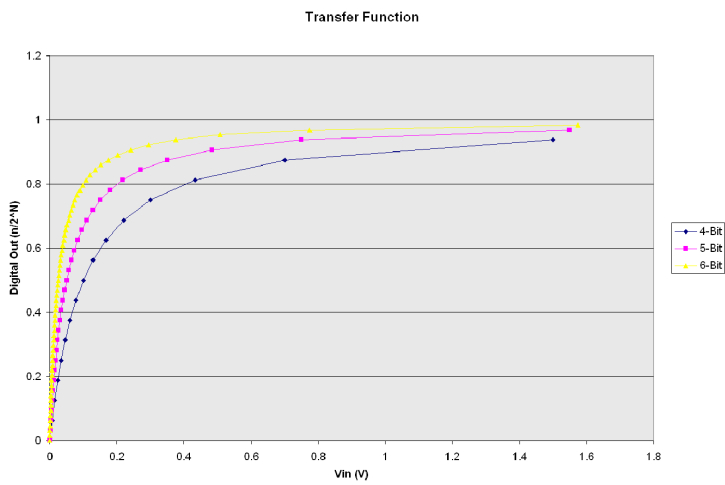


Figure 3.14: Transfer Function for N=4,5,6

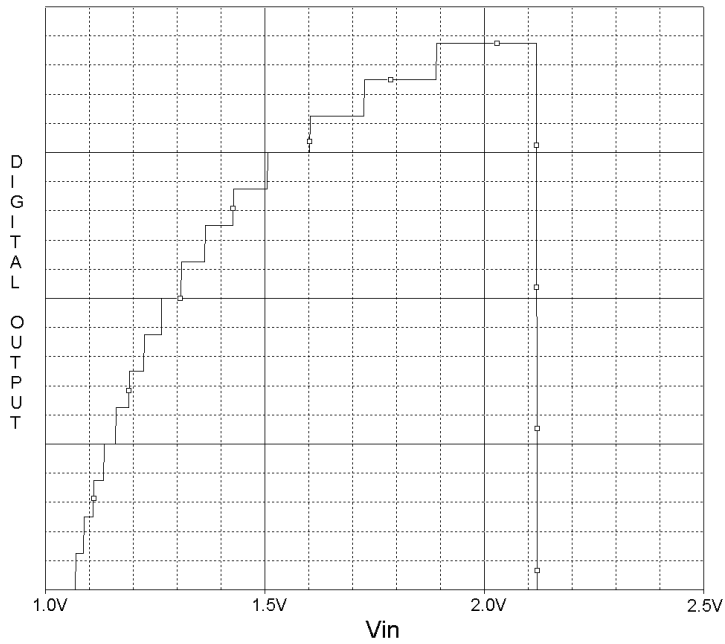


Figure 3.15: Transfer Function if last resistor is $4R$ with all other R

only compressing functions can be done “naturally”. The resistor values used are shown in Table 3.4.

To achieve a compressing function from a linear Flash architecture the same extreme changes need to be made to the reference ladder, as needed to be made to linearize the compressing converter.

3.3 Device Characteristics

3.3.1 Static and Dynamic Power Consumption

A good understanding of the expected power consumption is very important, for reasons of architectural comparison, judging the success of an actual device, and

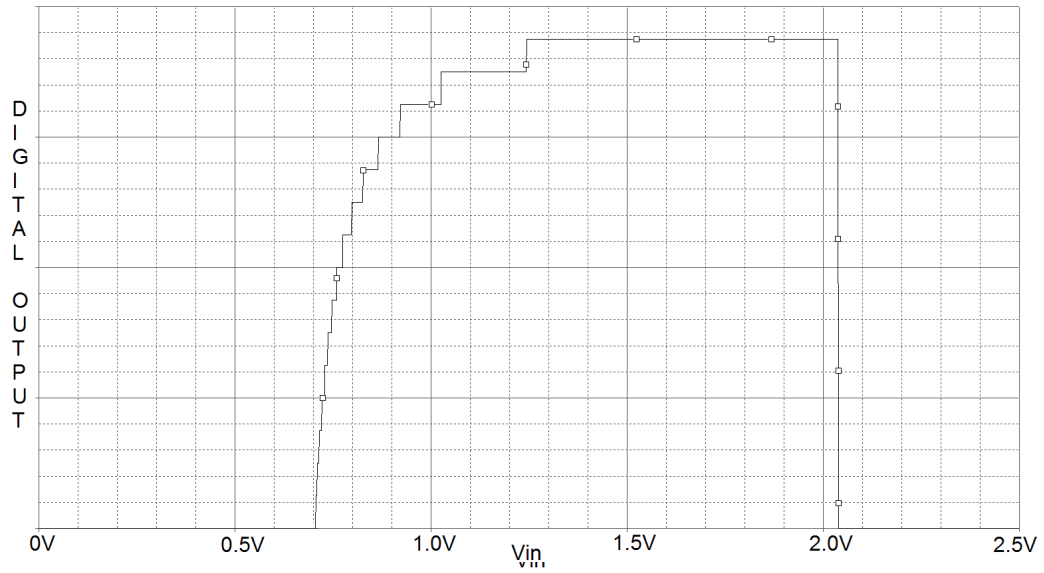


Figure 3.16: Transfer Function of Logarithmic ADC using Compressing Architecture

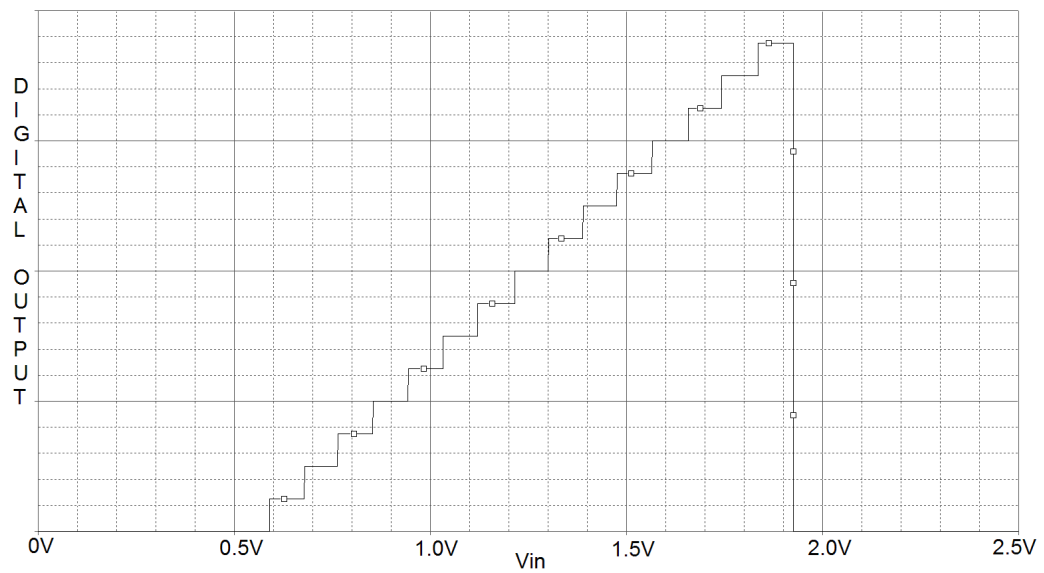


Figure 3.17: Transfer Function of Linear ADC using Compressing Architecture

Device	Base Design	Less Compressing	Logarithmic	Linear
Vsw	100	100	50	30
R1	1000	1000	500	120000
R2	1000	1000	500	32000
R3	1000	1000	600	13400
R4	1000	1000	600	6400
R5	1000	1000	700	3600
R6	1000	1000	700	2300
R7	1000	1000	800	1700
R8	1000	1000	800	1120
R9	1000	1000	1000	890
R10	1000	1000	1000	710
R11	1000	1000	1000	590
R12	1000	1000	1000	500
R13	1000	1000	1100	390
R14	1000	1000	1100	360
R15	1000	1000	1100	300
R16	1000	4000	800	4000

Table 3.4: Resistor Values for Various Transfer Functions
The linear ADC requires a variation over 3 orders of magnitude, while the logarithmic converter resistors where all of same order of magnitude.

for component optimization, despite power consumption being easily measured.

Analyzing Figure 3.1 we see that there are several stages and investigating each stage led to the conclusions summarized in Table 3.5 and will be highlighted in this section. This analysis is intended to provide a guide to optimization.

Since the architecture is based on Flash ADC, the static power consumption will be dominated by the quantizer stage. Each quantizer will generally consume a fixed amount of power (DC) regardless of operating conditions. This can be quite large per quantizer and when multiplied by $2^N - 1$ total quantizers, it becomes obvious why this is the dominant power consumer. The static to dynamic power ratio depends on the actual architecture. Many quantizers use a combination of DC biased components and clocked or unclocked latches. The latches have a high dynamic power consumption, but no static power consumption. Proper optimization of the quantizer stage can result in excellent power consumption.

The buffer is the other main source of DC power consumption. For many reasons discussed in section 4.1.2 buffers have a large bias current, so the circuits tend to consume large amounts of static power. This is generally less than the quantizer stage though. In addition, they have little dynamic power consumption.

The reference ladder presents an interesting advantage over Flash conversion. In Flash conversion the reference ladder is a fixed source of static power consumption $\frac{V_{dd}^2}{R_{reference,total}}$. For high speed designs $R_{reference,total}$ can become very small. With the compressing converter the power consumption is dependent upon the signal voltage. This leads to the conclusion that the total power consumption of the reference ladder will generally be pretty low. Since V_{in} will generally

Stage	Static Power	Dynamic Power	Transient Delay
Buffer	$I_{bias} \cdot V_{dd,Buffer}$	Little change from static	Unity gain circuit, based on load impedance as determined by reference ladder
Sample/Hold	Pass circuit, 0	Very small charge injection, single inverter, small capacitive loss	Charging and discharging inversion channels of large pass transistors
Reference Ladder	V_{in}^2 / R_{total}	Little change from static	Will be a different propagation delay depending on the bit, i.e bit 1 faster than bit 16
Quantizers	$(2^N - 1) \cdot I_{bias} \cdot V_{dd,comparators}$	Per quantizer- Generally contains high gain latch stages Total- requires quantizer to switch, so it will be signal dependent	Fixed delay to make switch
Encoder	Generally CMOS, so 0	Very high, depends on number of gates switching, so signal dependent	Delay encoder architecture dependent, longest delay will generally be on a single bit, often LSB.
Output Buffer	Generally CMOS, so 0	N number of drivers, only consume on switch	Fixed for all bits, single gate delay

Table 3.5: Anticipated Device Characteristics

be small, the total R can be made small, without power concerns. To bring the power consumption to a minimum, the input signal can be lowered to 0 after each sample.

The standard assumption is that the CMOS implementation leads to zero static power consumption and a relatively large dynamic power consumption. With CMOS, however, this power consumption is in the form of large peak power consumption. The encoder power consumption will be dependent on the number of gate transitions. The transition from n to $n+1$ will generally lead to less gate switching than the transition of n to $n+2$. This leads to a large signal dependence on the dynamic power. Using the same argument as established in previous paragraphs, the dynamic power consumption will be lower since there will be less full range transitions. In this paper, the full range switching will typically be reported.

What are the outcome of signal dependent effects? What is the most likely signal? In section 3.2.4 it was shown that the maximum SNR is in the lower signal voltages. It is therefore assumed that the device will generally operate under those conditions. This needs to be considered when judging the average effects of signal dependent characteristics throughout the device. Remember, in the compressing converter not all bits are created equal, the optimal signal is more likely to be on the lowest bits.

3.3.2 Transient Delay

Reference ladder presents itself as a distributed RC load to the buffer, where each R node is connected to a capacitance (quantizer input). Since the circuit is a

distributed RC, there is a (transmission line-like) delay associated with it, which will be different for each bit. The higher bits will have a much longer delay than the lower bits. R and C should be minimized to reduce this effect. This effect can be considered analytically, ignoring the effect of the capacitance of other quantizers. The pole associated with each quantizer will be determined by capacitance and the resistance between the quantizer and the buffer. This leads to the approximate pole being (3.18), which shows a significant delay at the upper bits. This will cause a signal dependent phase in the output spectrum. Hence, R and C need to be minimized. Using the logic discussed in section 3.3.1 the average transient delay due to this effect will be much lower than the discussion would assume.

$$\omega_{pm} = \frac{1}{nRC} \quad (3.18)$$

Both the comparators and buffer will largely present themselves as a fixed delay. The bandwidth of the device will generally be limited by other components (reference ladder).

The delay of the encoder will be architecturally dependent. The device will need to be clocked to work at the longest delay, which for most encoder implementations will be the LSB. The encoder is a band-limiting component, but there are many digital techniques to eliminate problems with the encoder.

Chapter 4

Implementation

There were four implementations of this circuit manufactured on the AMI Semiconductor $0.5\mu m$ process. This a robust digital CMOS process which was provided through MOSIS. The design was done using submicron scalable CMOS design rules[9]. Simulations and circuit checking were performed on Cadence Design Studio using the installed kits provided to the University of Maryland. For hand calculations parametric test results were used[8]. There were four implementations developed and a summary of their components are in Table 4.1.

4.1 Analog Circuit Design

4.1.1 Reference Ladder

The reference ladder will be discussed first even though it comes comes third in the signal chain. There are two reasons for this: one of the implementations

	A	B	C	D
Input buffer	None	PMOS Source Follower	None	PMOS SF
Sample/Hold	No	No	Yes	Yes
Reference Ladder	Resistive	Resistive	Capacitive	Capacitive
Reference Offset	None	PMOS DCT	None	None
Comparators	PMOS	NMOS	PMOS-2	PMOS-2
Encoder	Same	Same	Same	Same
Digital Output	Latched	Both	Both	Both
Part Number	T4AABP	T4BPBK	T4BPBL	T4BPBL

Table 4.1: Summary of the Four Implementations Components

did not have a buffer or sample/hold, and the design of the input buffer and the sample/hold depend on the reference ladder far more than the reference ladder depends on those components. As explained in section 3.2.9, the reference ladder determines the transfer function of the device by the variation in the reference elements. The reference ladder impedance determines many of the power and speed characteristics, as discussed in section 3.3.

Resistive Ladder

The first ladder used was a resistive ladder. The resistive ladder is composed of a series of 15 high resistance resistors. Figure 4.1 shows the output of the resistive ladder. There were two variables that needed to be chosen for the ladder: the type of resistor used and total resistance value. There are three resistors available in the process used: an Nwell resistor, a polysilicon (poly) resistor, and high-resistance poly resistor¹. Since this is a digital process, none of resistors are of exceptional accuracy. Table 4.2 gives a summary of the resistor characteristics. The choice of

¹It is assumed that the high-resistance polysilicon resistor is obtained by not using a silicide.

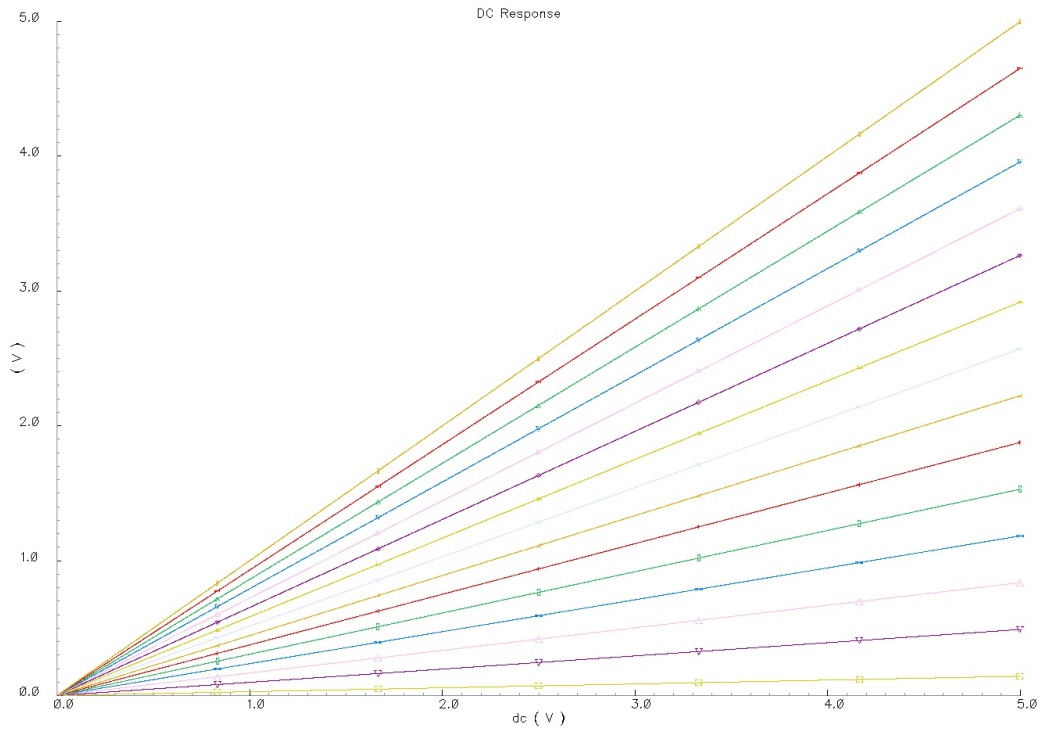


Figure 4.1: DC sweep resistive ladder

resistor depends on the final resistance value desired, but the high-res poly or poly resistor would be chosen over the Nwell resistor due to parasitic capacitances and total area.

The total resistance value determines the power consumption of the component, the speed of the component, and the demands on the input buffer. The power

Characteristic	Nwell	Poly	High-Res Poly
Resistance ($\Omega/sq.$)	~833	25	~1100
Area	Very Large	Small	Small
Accuracy	Low	High	Medium

Table 4.2: Comparison of Resistors Available

consumption will be $\frac{V_{in}^2}{R_{total}}$, so larger values of R reduce the power consumption. Section 3.3 argued that in general the power consumption will be low if the device is typically operated in the linear regime. The linear regime will also limit the effects of the resistance on speed. For most high speed devices the designer is willing to trade power for speed, and as such for this design favored making the resistance as small as possible. Small resistors also have lower noise than large resistors.

The limiting characteristic was generally determined by the demands placed on the input buffer. Driving large currents is difficult in CMOS. This loading effect will be analyzed in section 4.1.2. For the bufferless design, the resistance had no effect, other than to limit most speed tests. The final resistance value was chosen to about 1000Ω , for a total resistance of $15k\Omega$.

The layout of the resistor was performed using the poly resistor in a connection of 3 series resistors as shown in Figure 4.2. These were surrounded by a guard ring to reduce substrate noise coupling. Each resistor has parasitic capacitance to ground which would limit the speed and also allow noise to be coupled in. This parasitic capacitance can only be reduced by reducing the size of the resistors. This has two balancing factors: current limitation and accuracy. The minimum width is determined the maximum current drawn. The dominant variation in resistor values is process variation, so a larger area leads to more precise resistors. In analog and RF processes there are more accurate and lower parasitic resistors available.

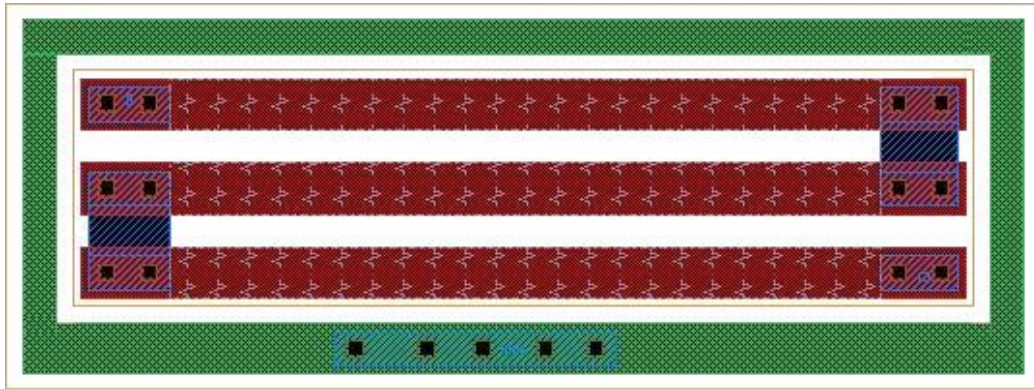


Figure 4.2: Layout of the Resistors

Capacitive Ladder

A capacitive network was implemented in two of the designs. The advantage of capacitive ladder is that there will be no static power dissipation. This becomes a major benefit for low power designs. However, since the impedance of a capacitor reduces as frequency increases dynamic power consumption can be very high, unlike the resistive ladder.

In CMOS designs capacitors are generally favored over resistive devices. Many CMOS circuits move charge around rather than working with current. CMOS capacitors typically have a much higher relative accuracy than resistors. Digital CMOS process typically have (at least) one high quality linear capacitor. In the process used this was a poly-poly capacitor, a cross section is shown in Figure 4.3. MOS gates can be used as well, but these are non-linear, and metal-insulator-metal (MIM) capacitors are rarely available². A poly-poly capacitor is made by using the

²MIM capacitors require at least one extra mask step so are often not added due to cost reasoning. These are the standard linear capacitor in RF processes. MIM have a very low parasitic capacitance.

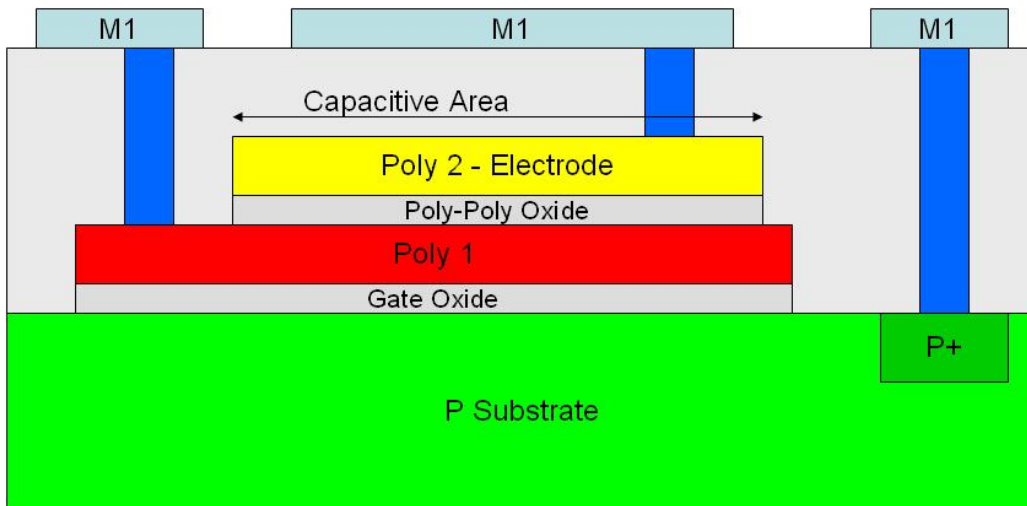


Figure 4.3: Cross Section of Poly-Poly Capacitor

gate poly with another growth of oxide followed by another layer of polysilicon. The polysilicon layers are connected up to first layer of metal through contacts. The cross section show that the capacitor has high capacitance per unit area, since the oxide is very thin.

The cross section also shows, however, that there is a very high parasitic capacitance to ground. This parasitic capacitance can lead to noise coupling into the reference ladder, however, the guard ring can prevent most of that. The main problem with the parasitic capacitance is that it affects the transfer function of the reference ladder. This can be remedied through the imposition of added design constraints. The parasitic capacitance is about 10% of the real capacitance. The designs here used uncompensated networks, so there is an additional non-linearity. A “DC” sweep is shown in Figure 4.4. Figure 4.5 shows a close-up of the non-linearity.

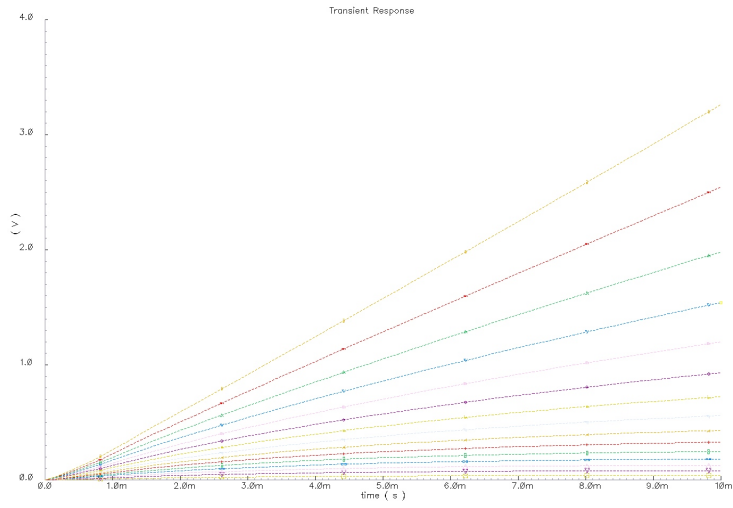


Figure 4.4: A “DC” Sweep of the Capacitive Ladder

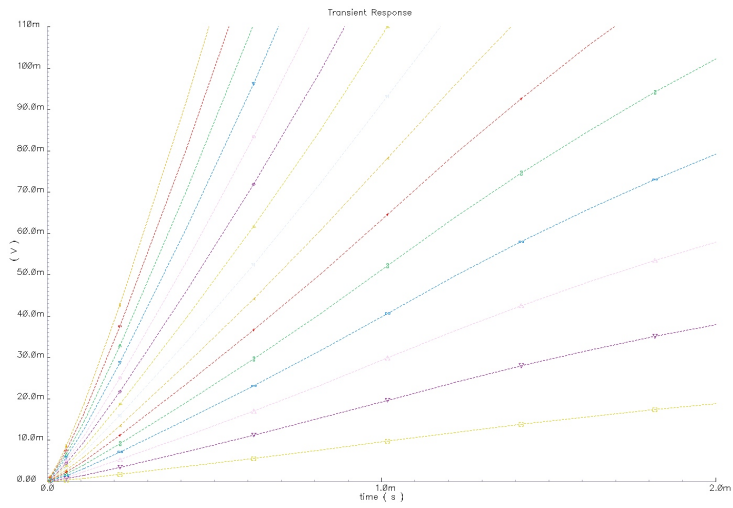


Figure 4.5: DC Sweep of Capacitive Ladder Zoomed In

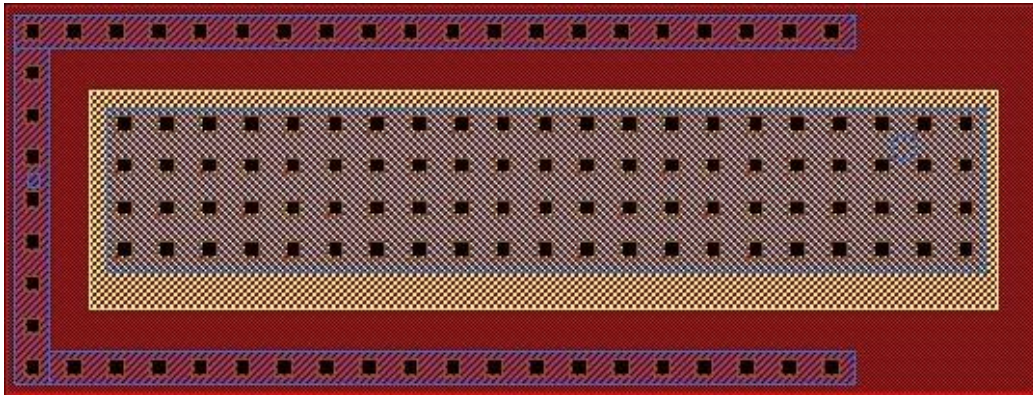


Figure 4.6: Layout of the Capacitor

Thermal noise is caused by the random variations in the current caused by thermal excitation and is white across all frequencies. The thermal noise voltage of capacitors goes as $1/C$ like the impedance. The transient speed of capacitive network increases as the input capacitance goes down. Since the capacitors are in series the input capacitance goes down as more capacitors are added. The thermal noise can be very small with large capacitors, but the series connection keeps the speed up. These characteristics lead to the design choice of making the capacitors large. The capacitors were chosen to be about $220 fF \times 2$ as shown in Figure 4.6.

Reference Ladder Error

The reference ladder will have a mismatch between the components. In a linear ladder, the effect of a ladder mismatch is easy to calculate since the total error is proportional to the error of each reference element. In this design the effect of the error is more complex. Equation 4.4 shows the final error of the n -th transition. The three components of the error are the original transition width, $\frac{n}{(2^N - n)}$, and the

relative error of the reference element. ΔV_{bn} goes as approximately exponential and dominates the equation leading to an increasing absolute error. $\frac{n}{(2^N-n)}$, however, reduces the relative error on the lowest bits, which is excellent on a design where the lowest bits are most important. The highest bits (above 2^{N-1}) get an increasing relative error compared to the relative error of the reference ladder.

$$Error_n = \Delta V_{b(n+\Delta n)} - \Delta V_{bn} = \frac{2^N \cdot V_{ref}}{(2^N - n \left(1 + \frac{\Delta n}{n}\right)) (2^N - n + 1)} - \frac{2^N \cdot V_{ref}}{(2^N - n) (2^N - n + 1)} \quad (4.1)$$

$$Error_n = \frac{2^N \cdot V_{ref}}{(2^N - n + 1)} \left[\frac{\Delta n}{(2^N - n \left(1 + \frac{\Delta n}{n}\right)) \cdot (2^N - n)} \right] \simeq \Delta V_{bn} \left[\frac{\Delta n}{(2^N - n)} \right] \quad (4.2)$$

$$n \Rightarrow nR, \Delta n = n \Delta R \quad (4.3)$$

$$Error_n = \Delta V_{bn} \left[\frac{n}{(2^N - n)} \cdot \frac{\Delta R}{R} \right] \quad (4.4)$$

4.1.2 Input Buffer

The purpose of the input buffer is to isolate the outside signal from the circuitry. Ideal voltage-voltage buffers are characterized by an infinite input impedance, zero output impedance, and unity gain. The circuit senses an input voltage and

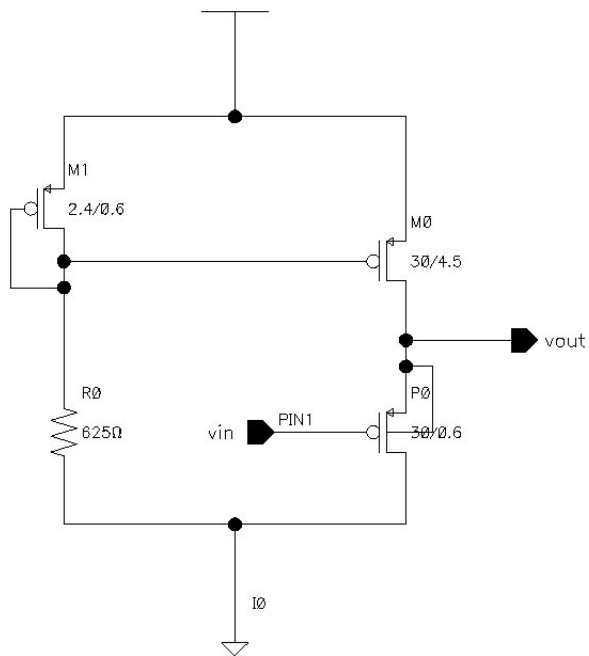


Figure 4.7: Input buffer schematic

generates an equal output voltage into an arbitrary load. The buffer prevents the circuitry from loading the signal generator or other input source. This is especially important because the reference ladder is a resistive low impedance.

The input buffer was a source follower. Additionally, a operational amplifier³ with a feedback network was considered. The two were compared analytically and the source follower was found to be the better option as it operates over a large input voltage range. This requires an op-amp with a large common mode range, a difficulty with a high gain amplifier.

The source follower input transistor is shown as P0 is Figure 4.7. The input transistor needs to be sized according to two competing needs: minimizing input

³An operational transconductance amplifier could be used with the capacitive reference ladder.

capacitance and minimizing the effects of the load reference ladder. The input capacitance of an amplifier is that of the gate and is proportional to the area of the gate. This signal source needs to be able to charge the gate to reach high speeds.

The gate-source voltage can be found in terms of current through the transistor. The current through the transistor is the bias current with no input, the change in the bias current due to finite output resistance of the current mirror, and the current output to the load. The change in voltage goes as the inverse square root of the current.

$$V_{GS} = \sqrt{\frac{I}{k_p} \cdot \frac{L}{W}} + V_{th} \quad (4.5)$$

$$I = I_{bias} + \Delta I_{bias} + I_{Load} = I_{bias} + \Delta I_{bias} + \frac{V_{out}}{R_{total}} \quad (4.6)$$

$$\frac{\partial V_{GS}}{\partial I} = \frac{1}{\sqrt{I \cdot k_p}} \cdot \sqrt{\frac{L}{W}} \quad (4.7)$$

Ideally $\frac{\partial V_{GS}}{\partial I}$ would be zero, but this solution gives us the change in gain and clues at how to minimize this change. As the load draws off more current, the gate-source voltage increases, reducing the gain below unity. The gate width to length ratio needs to be large to maintain near unity gain as shown in Equation 4.7. The larger load resistance can increase the gain by decreasing the current, which increases the V_{GS} . A higher output resistance on the current mirror has a similar effect by causing a decrease in ΔI_{bias} . Figure 4.8 shows the transfer

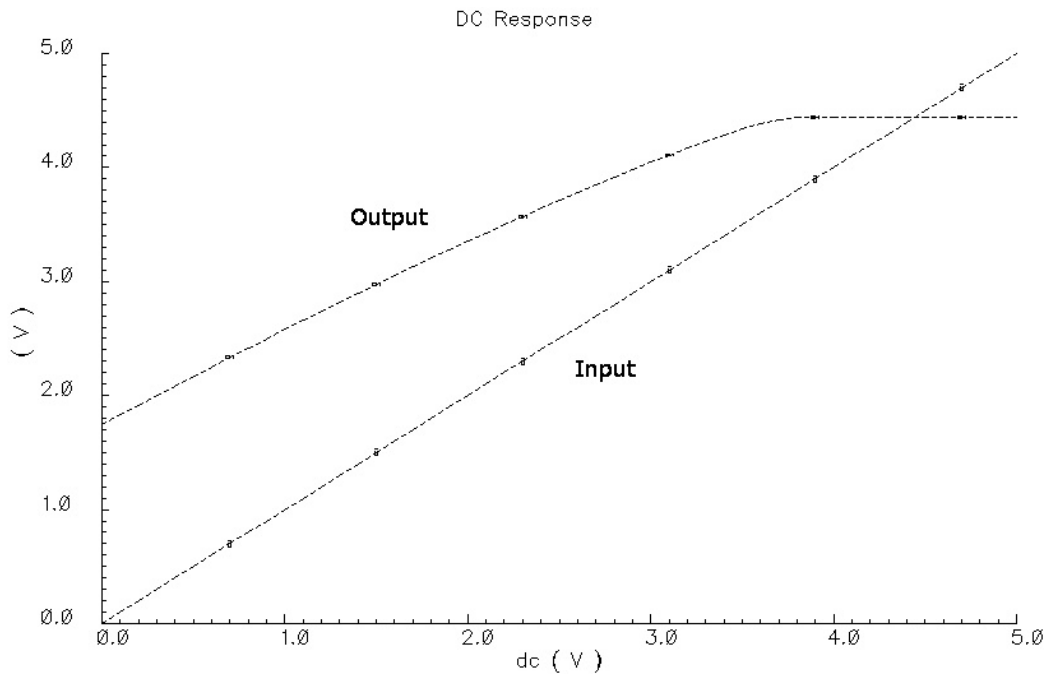


Figure 4.8: Transfer Function of Input Buffer with an $8k\Omega$ Load

function with the input buffer with a resistive reference ladder. The change in input-output voltage is proportional to inverse square root of the current, which leads to a non-linear change. This design is intentionally nonlinear, so all of these nonlinearities can all be dealt with in design.

The source follower circuit is in Figure 4.7. The circuit is a PMOS source follower circuit. A PMOS circuit was used instead of an NMOS circuit to eliminate the body effect, since the source of a PMOS circuit can be tied to the Nwell body. The source follower is biased with a simple current mirror.

The current mirror is set to have a current of $500\mu A$, as found using Equation 4.10. The output resistance of the current mirror was increased by increasing the

length. A high output resistance is very important in a circuit such as this which needs to operate over a large voltage range, since it increases the gain of the buffer. A different topology could have been used such as a cascoded current mirror to further increase the output resistance even more. Unfortunately, this would have reduced the voltage headroom of the circuit, which needs to be maximized in this design.

$$V_{dd} = I \cdot R_0 + V_{GS} \quad (4.8)$$

$$V_{dd} = I \cdot R_0 + \sqrt{\frac{I}{\beta}} + V_{th} \quad (4.9)$$

$$V_{dd} - V_{th} = I \cdot R_0 + \sqrt{\frac{I}{\beta}} \quad (4.10)$$

A layout of the input buffer is shown in Figure 4.10. The large PMOS transistor is the input transistor. The resistors were connected in the array to minimize the area. The performance of the circuit is not strongly affected by the absolute value of the resistors.

The buffer has a unity gain and as such is usually not speed limited. To test this the circuit was loaded with a resistive load and a pulse was applied. The result is shown in Figure 4.11 and shows that while there is a delay it is small relative to the other components.

Two of the implementations did not use a buffer in order to maximize DC⁴ test

⁴In case of the capacitive implementation, DC just means slow so the overall transfer function can be determined.

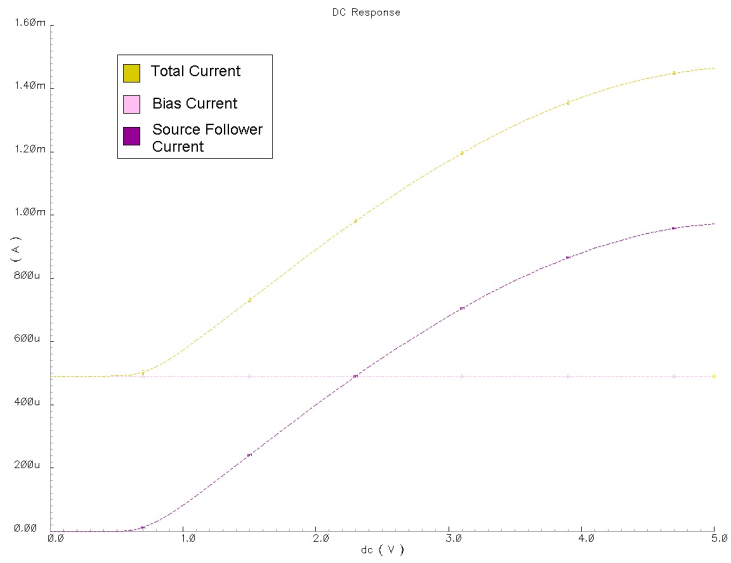


Figure 4.9: Currents of Input Buffer

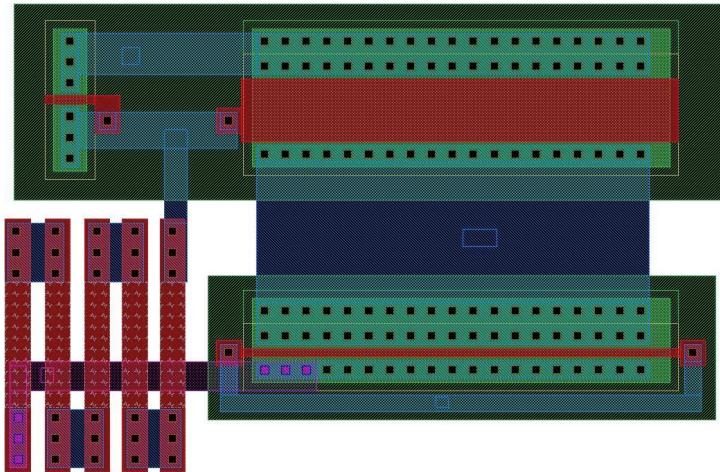


Figure 4.10: Layout of Input Buffer

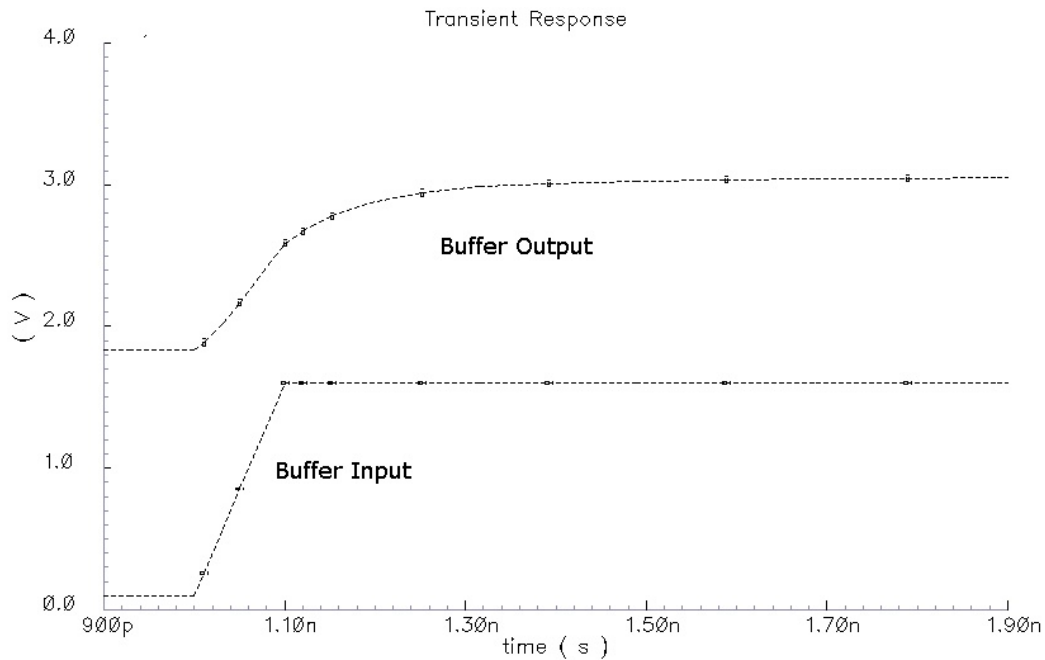


Figure 4.11: Transient Response of the Input Buffer

flexibility.

4.1.3 Sample/Hold

A sample/hold circuit was used to load the capacitive reference ladder. The sample/hold circuit utilized the capacitive ladder as the hold capacitor and the comparators as the buffer. The comparators may be used as buffers since they have infinite input resistance. The use of the capacitive ladder as the hold capacitor leads to a reduced noise and increased speed as described in section 4.1.1.

The circuit described here as a sample and hold would be better as the sampling switch as shown in Figure 4.12. The circuit is composed of a CMOS trans-

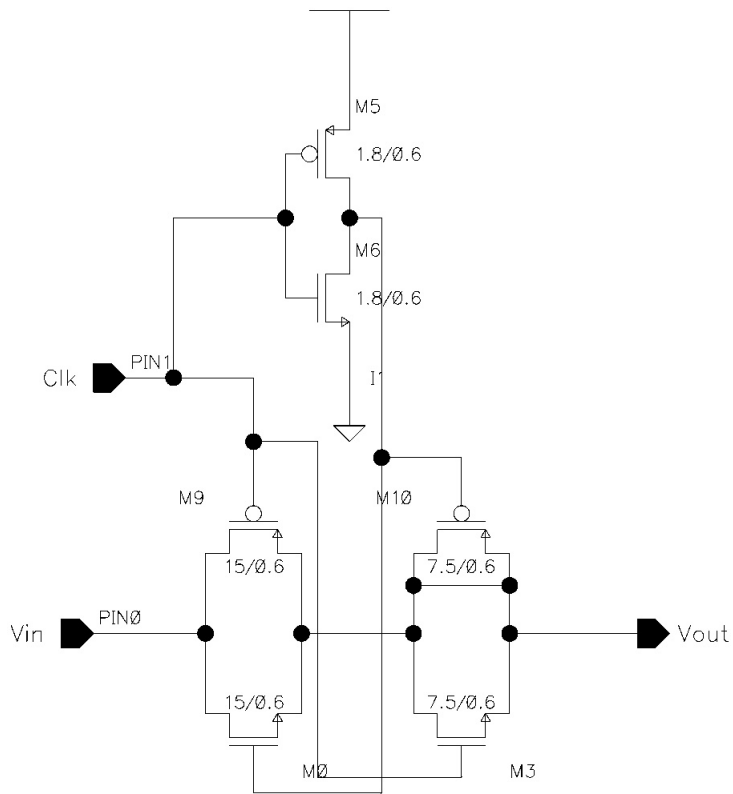


Figure 4.12: Sampling switch schematic

mission gate, a dummy switch and the clock inverter. The CMOS transmission gate was chosen to maintain a low resistance path over all input voltage ranges required by the device. This reduces signal dependent distortions among other things. The gates were sized to be fairly large in order to minimize the resistance, making the switch act more like an ideal switch. The layout of the sample switch is shown in Figure 4.13.

There are two main sources of error in sample and hold circuits, clock feedthrough and charge injection[36, 33]. Clock feedthrough is the result of the clock ca-

capacitively coupling into the signal. Clock feedthrough is a signal independent error, unlike charge injection. Clock feedthrough is best eliminated through a differential architecture⁵, since it appears as a common mode error. Since clock feedthrough is signal independent it can be compensated for in this architecture in the calibration step. Charge injection is more complex. When the switch is on, the MOSFET channel is in inversion and there is a layer of mobile charge in the channel. When the switch is turned off this charge needs to go somewhere. If the switch is operated fast enough the charge will split, with half going to the signal source and half into the signal path. This charge goes on to the capacitor and adds an additional voltage to the signal. This would be fine if the amount of charge were constant, but it is signal dependent. Charge injection results in input nonlinearities, which make it less of an issue with a nonlinear architecture. A dummy switch with half the width was used to absorb this charge. When the main clock turns off the inverter makes a complementary clock turning on the dummy switch. The source and drain of the dummy switch are shorted, but a channel is still formed absorbing the charge.

4.1.4 Comparators

Circuit Description

The comparator used was based on the design in Baker, Li, and Boyce [11].

Opamps can be used as comparators, but they have frequency compensation to

⁵A differential compressing architecture has yet to be developed. This could be done by using a complete sample/hold amplifier and having the amplifier be differential.

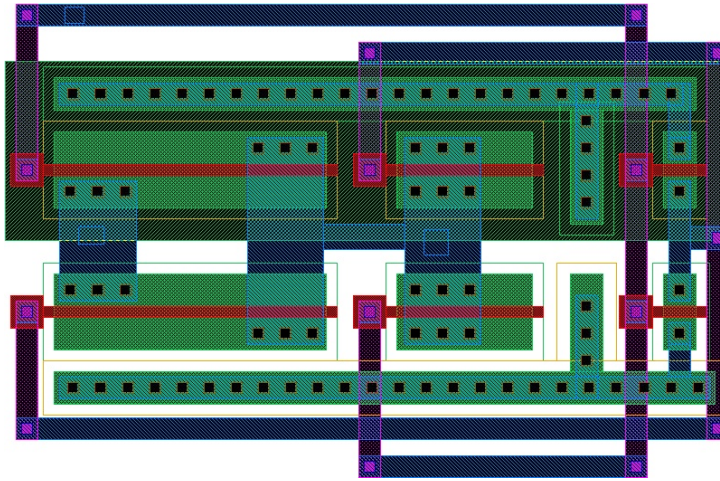


Figure 4.13: Layout of Sample Switch

prevent oscillation in feedback circuits, which limits their bandwidth. It is important to remember that comparator design is different than opamp design. The goal of comparators is to determine which input is larger and output “one” or a “zero”. The key parameters are offset, maximum operating frequency, and voltage level that can be discriminated at that frequency. Many comparators are clocked and some are even pipelined. The design described here used neither technique.

The design is composed of three stages: preamplifier, decision circuit, and output buffer as shown in Figure 4.14. The purpose of the preamplifier stage is to provide a small amount of gain in order to allow the decision circuit to full switch at the desired discrimination level. The preamplifier is an actively loaded differential pair with a simple current mirror biasing the differential pair. The load on each side of the differential pair is a diode coupled transistor. In addition there are two diode coupled transistors connected between the sides of the differential

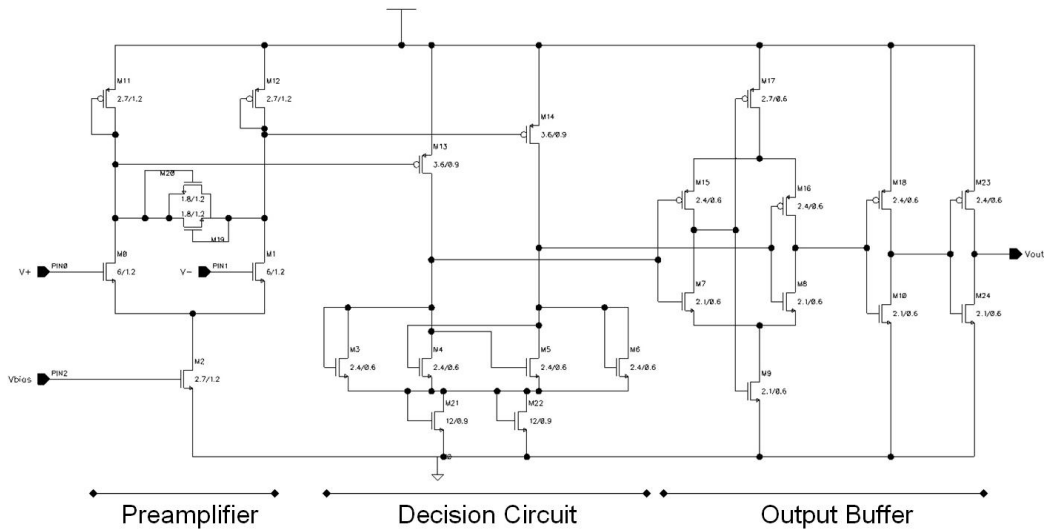


Figure 4.14: Schematic of NMOS Comparator showing stages

pair. The purpose of these transistors is to keep the differential output voltage with a V_t of each other, to increase the speed of the design. In hindsight, due to the bias conditions of this circuit, this is unnecessary. The current is then mirrored from M11 and M12 to M13 and M14, respectively.

One of the interesting characteristics of this architecture is that the comparators can be designed around a single input voltage⁶. This is what led to the discovery of this architecture. ADC architectures where the comparator operates at a single voltage have been investigated by the author⁷. The fact that all the comparators work at the same input voltage implies two things: the comparator circuit can be optimized for that input, and there is no common mode to consider. The optimization for these designs were limited. The single voltage input allows the

⁶Actually it needs to operate over a range, for example the NMOS convert needs to work from 3.5 to 4V. This is a very small range compared to the dynamic range of the device.

⁷Investigations continue with these.

designer to bias the amplifier for a specific voltage rather than a large input range. The lack of common mode means that each comparator operates the same and has the characteristics, i.e. no input dependent characteristics. The CMRR is an important characteristic of opamps. The CMRR is related to the output resistance of the current source. Since these designs do not need to work over a common-mode range, a simple current source is fine.

The offset of the comparator is largely determined by preamplifier, hence steps are taken for good matching. Much has been written on MOS matching[?, 13][?, ?], but in this circuit the dominant source of mismatch will be threshold mismatch. Threshold mismatch is inversely proportional to the square root of the gate area, therefore a large gate is beneficial to matching. This has been done in this design with a $W/L = 6.0/1.2 = 20\lambda/4\lambda$. A secondary factor will be process and geometry mismatch. A large W/L ratio, as used here, helps reduce both of these factors.

The effect of an error on the comparator⁸ was investigated further. Adjusting Equation 3.6, which is used to find the voltage difference between two bits, to take into account an offset in the comparator yields Equation 4.11. This equation was simplified, and it is shown that the difference between two bits is the original difference plus the offset voltage amplified by the inverse of the original bit division, β .

⁸This can be offset voltage between built into the comparator, noise on the reference ladder, or noise on the reference voltage and the analysis is the same.

$$\Delta V_{bn,offset} = \frac{V_{ref}}{1 - \frac{n}{2^N}} - \frac{V_{ref} + V_{offset}}{1 - \frac{n-1}{2^N}} \quad (4.11)$$

$$\frac{V_{ref}}{\frac{2^N-n}{2^N}} - \frac{V_{ref} + V_{offset}}{\frac{2^N-n-1}{2^N}} = \frac{2^N \cdot V_{ref}}{2^N - n} - \frac{2^N \cdot (V_{ref} + V_{offset})}{2^N - n + 1} \quad (4.12)$$

$$\Delta V_{bn,offset} = \Delta V_{bn} + V_{offset} \cdot \frac{2^N}{2^N - n + 1} = \Delta V_{bn} + V_{offset} \cdot \beta \quad (4.13)$$

The effect of comparator offset becomes more severe the higher the bits go. Therefore, highest bit will have the offset amplified by a factor of approximately 2^N or 16 in this circuit. This is a potentially serious problem, although as was discussed earlier, the accuracy at the higher bits is less important than the lower bits. The problem is caused by the division of the input signal and is related to the effect discussed in Section 4.1.4.

Does the division of the input signal affect the signal to noise ratio for the noise on the reference ladder, i.e. thermal noise? If the metastable region discussed in Section 4.1.4 is taken as a separate issue, the noise does seem to be β multiplied like the offset voltage. However, this needs to be taken with the metastable region, since that is the area of operation where noise is the largest problem. Further work will continue to analyze this and tests are being developed to verify the conclusions.

This large gate area leads to one major problem, a large input capacitance. As was discussed in section 3.3.2 the capacitance of the comparators has a large effect on the speed of the device. This determines the pole of the reference ladder and the speed of the circuit. This is one of the primary difficulties of CMOS ADC design, the input transistors need to be small to be fast but large to be accurate. The LSB of this device is of the same order as threshold voltage errors, the design erred on the side of offset correction by making the transistors large. Future designs will look to better balance these effects. Due to the large input capacitance multiple preamplifier stages are often used to get the desired gain at high speeds.

When designing Flash ADCs one of the major limiters of speed is capacitive feedthrough. This is when the input signal couples through the gate-source capacitance of both sides of the differential pair and the signal ends up on the reference ladder. This is not an issue with this design since the coupled input signal connects to a voltage source (V_{ref}). This will not be a speed-limiting issue.

The decision circuit (Figure 4.15) is a positive feedback circuit which is capable of discerning between very small signal differences. The decision circuit accepts two input currents, i_{o+} and i_{o-} , which are the drain currents from M13 and M14 (see Figure 4.14). The heart of the decision circuit is M4 and M5 a cross-coupled pair, i.e. the drain of M4 is connected to the gate of M5 and vice-versa. If i_{o+} increases, the drain voltage of M4 will increase. This in turn increases the gate voltage of M5, which reduces the drain voltage of M5. This decreases the gate voltage of M4 and further increases the drain voltage. As the drain voltage of M4 (v_{o+}) increases, M3 begins to pull off more current from i_{o+} until the feedback

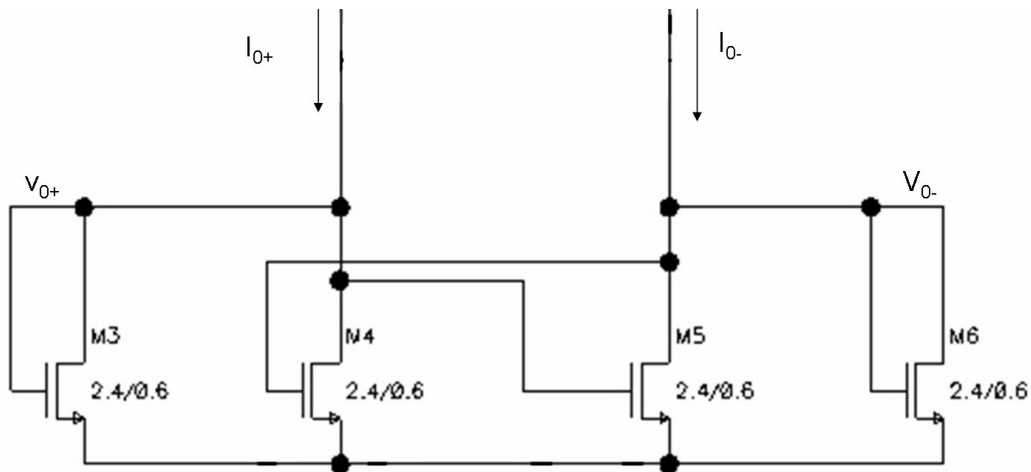


Figure 4.15: Decision Circuit used in the Comparators

cycle is stopped. This limits the output voltage range variations. M6 acts in a similar way by forcing more current into M5.

The circuit allows hysteresis to be built into the circuit, although none was used in this implementation. Hysteresis takes its name from ferromagnetics, and can best be explained by example. In a comparator with hysteresis, if the output is a zero, the input must go above the reference voltage by a margin to change to a one. If it does not go above this margin, but still goes above the reference voltage the output will remain a zero. Hysteresis can be used to reduce the effects of noise, by preventing the output from changing unless there is a significant signal change. This topic will be visited again in Sections 4.1.4 and 5.2.1.

The NMOS decision circuit required the output to be biased as shown in Figure 4.16. This changes the output voltages to values that properly are amplified by the output buffer.

The output buffer takes two output voltages from the decision circuit and am-

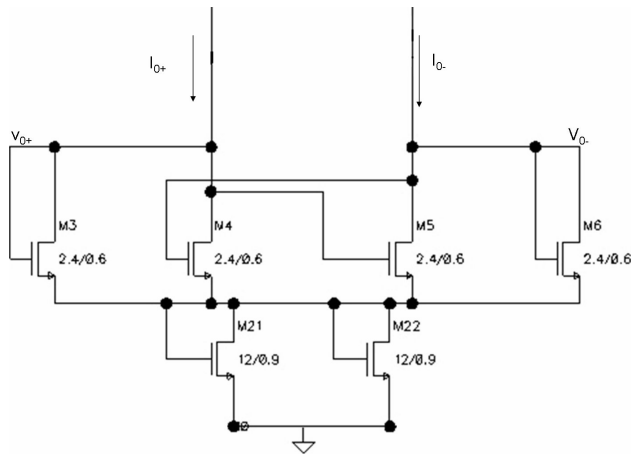


Figure 4.16: Decision Circuit biased to work with output buffer

plifies them to the digital levels required for the encoder. The output buffer is a self-biasing amplifier. Looking at the v_{o+} input, note that the voltage increases as the output decreases, since the circuit is basically a CMOS inverter. This causes the bias transistors to change as M9 turns off and M7 turns on hard. A similar effect happens as v_{o-} decreases, which increases the output voltage of the buffer. This output goes to a CMOS inverter to further increase the gain and bring the output levels to V_{dd} and Gnd . The NMOS comparator has an additional inverter to match the encoder design.

The PMOS circuit (Figure 4.17) is similar to the NMOS converter shown in Figure 4.14, only upside down. The main difference between the two schematics is that the decision circuit does not need the additional bias diodes. PMOS transistors are slower than NMOS transistors, often by a factor of 3. The PMOS comparator used PMOS transistors in the speed sensitive components, so the comparator was much slower than the NMOS comparator.

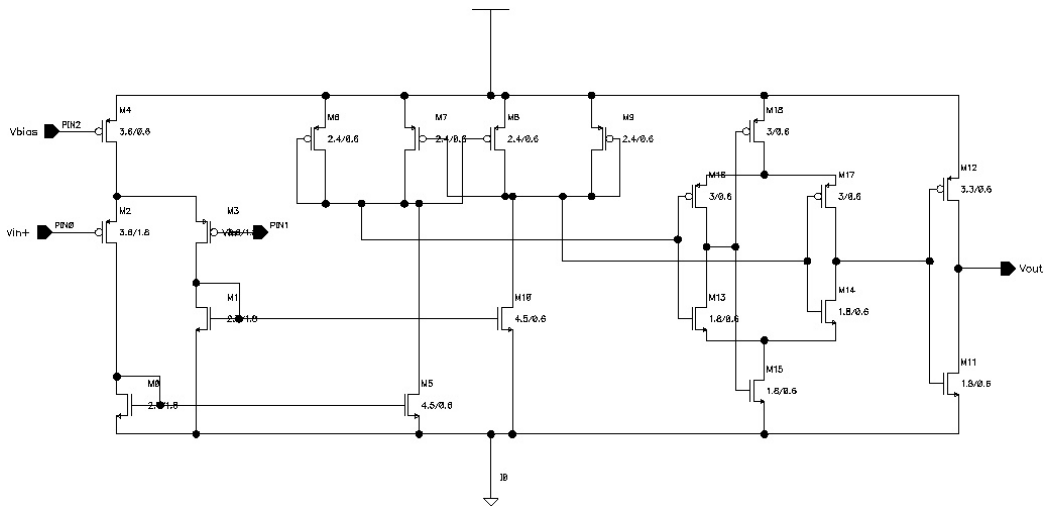


Figure 4.17: Schematic of PMOS Comparators

A PMOS buffer was used instead of an NMOS buffer to eliminate the body effect. This change forced the reference ladder to be tied to V_{dd} instead of Gnd . The input range of the PMOS comparator was designed to include ground, however it was not possible to get the NMOS comparator to have an input range including V_{dd} . This led to the requirement that the reference ladder must be biased down by a fixed voltage amount. This was accomplished through a PMOS diode-coupled transistor. Once the transistor turns on it is able to maintain a relatively constant voltage. The output resistance is approximated by $1/g_m$, so a large W/L was used. This transistor added another non-linearity in the reference ladder.

Metastable Region

In Section 5.2.1, it will be shown that there were significant glitches in the output transfer function. These glitches are the result of the comparator entering the

metastable region of operation, i.e. the output voltage was neither a “1” or a “0”. The size of the metastable region can be found using Equation 4.15. The metastable voltage margin is fixed by the supply voltage and the voltage range on the reference ladder that results in a metastable output is determined by the gain of the comparator. The range of node voltage is the same on each bit, but the node voltage is the input voltage divided by beta. This results in a input range into the circuit that causes a glitch to be beta-multiplied, i.e. increasing with each bit.

$$V_{margin} > A_{comp} \cdot \Delta V_n = A_{comp} \cdot \frac{2^N - n}{2^N} \Delta V_{in} = A_{comp} \cdot \frac{1}{\beta} \Delta V_{in} \quad (4.14)$$

$$\Delta V_{in,glitching} < \beta \cdot \frac{V_{margin}}{A_{comp}} \quad (4.15)$$

This shows the more input signal enters the metastable region on the higher bits, where there is a higher β , using the terminology established earlier. This increased glitch region can lead to significant issues and presents certain design challenges. The simplest way to reduce the effect is to increase the gain of the comparator. The gain is typically inversely proportional to the speed, and since the highest bits are already the slowest due to the reference ladder, this is not an ideal solution. This speed limit can be overcome by increasing the power used. A second option could involve a pipelined situation where these bits go through additional gain stages, while the other bits are passed. This has the effect of increasing the bandwidth while increasing the delay. The glitches are very

pronounced on the designs using the PMOS comparators since they have a lower gain than the NMOS comparators.

A third and most likely solution would be to use hysteresis to cover the entire metastable region. The hysteresis would keep the circuit out of the metastable region and improve noise immunity. The hysteresis would be the same on each bit, since the node voltage range that causes hysteresis is the same for each bit. The hysteresis will therefore be greater than if just noise were the issue.

The noise on the reference voltage should show up the same on all bits so this will not be β multiplied as in Equation 4.13. However, when those are coupled with the metastability region, it has the effect of causing more glitches and is worsened by the β multiplication of the metastability region.

Circuit Performance - Simulation

There are two main characteristics that can be found through simulation: gain and switching delay. To find the DC gain a sweep can be used placed at the $V+$ input and the reference voltage was placed on the $V-$ input. $V+$ was then swept and the transfer function investigated. The dc gain can be found by finding the slope of the transfer function. The zoomed-in transfer function for the NMOS comparator is shown in Figure 4.18 and the gain was found to be $4/.0008 = 5000V/V$.

Due to the lower transconductance of the PMOS gain stages and lower output resistance of the NMOS loads, the gain of the PMOS comparator was much lower at $4/.005 = 800V/V$. The transfer function is shown in Figure 4.19.

To find the switching delay of the comparators an input pulse was applied to

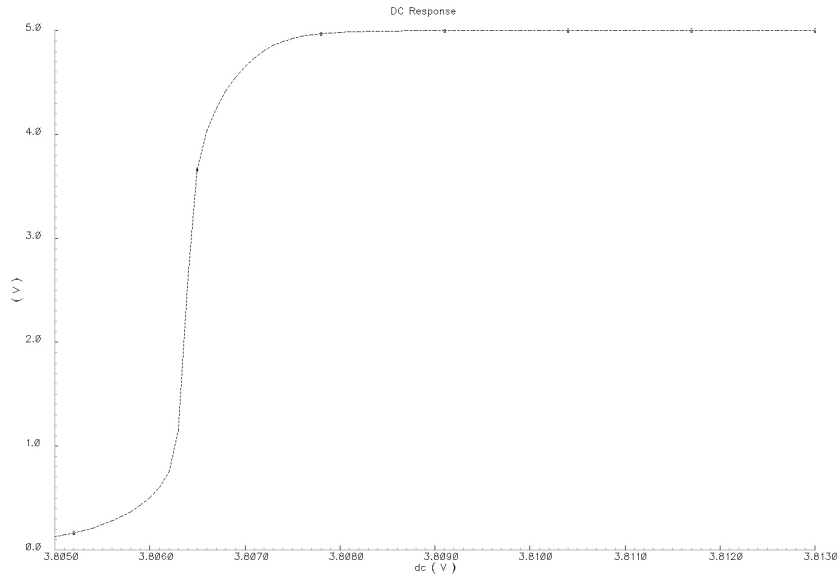


Figure 4.18: DC Sweep of NMOS Comparator to find the gain

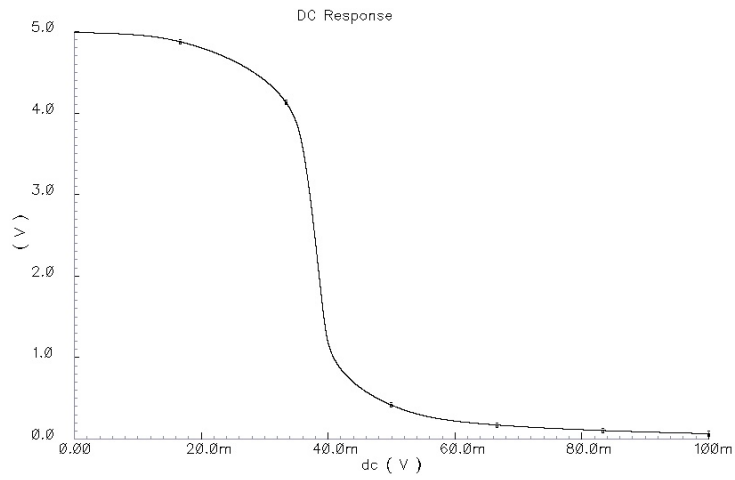


Figure 4.19: DC Sweep of PMOS Comparator to find the gain

	NMOS	PMOS	PMOS-2
Gain (V/V)	5000	800	800
Gain (dB)	74	58	58
Switching delay (ns)	2.2	3.0	3.0
Area (maximum dim.)	$4.0 \times 10^3 \mu m^2$	$2.0 \times 10^3 \mu m^2$	$2.3 \times 10^3 \mu m^2$

Table 4.3: Comparison of Comparator Performance

positive input at $V_{ref} \pm 10mV$ and the negative at V_{ref} and the delay between when the output switches was measured. The delay of the NMOS comparator is shown in Figure 4.20 and found to be $2.2ns$. The PMOS delay was found to be $3.0ns$ as shown in Figure 4.21. The power consumption was found by measuring the current out of the power supply during the the transient analysis and is found in Figure 4.22.

Circuit Layout

The comparators were drawn as shown in Figures 4.23, 4.24, and 4.25. Circuit-wise the PMOS-2 comparator is identical to the PMOS comparator. The preamplifier was placed in a separate well in the PMOS-2 design to reduce feed-through from the digital parts. The NMOS comparator used a guard ring to further reduce the noise in the preamplifier. This will also help minimize particle effects in satellite applications. The areas of the layouts are given in Table 4.3

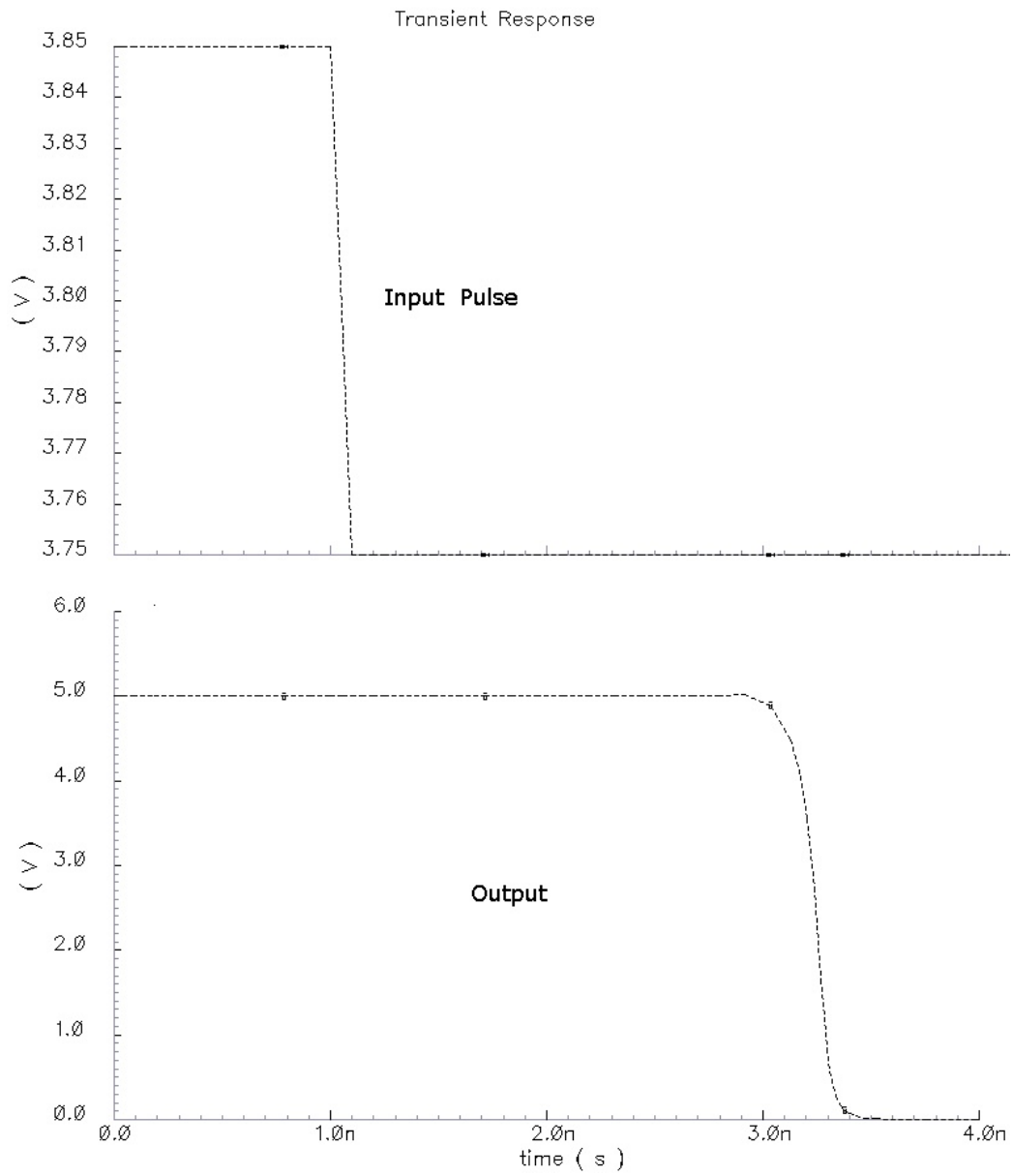


Figure 4.20: Transient performance of NMOS Comparator

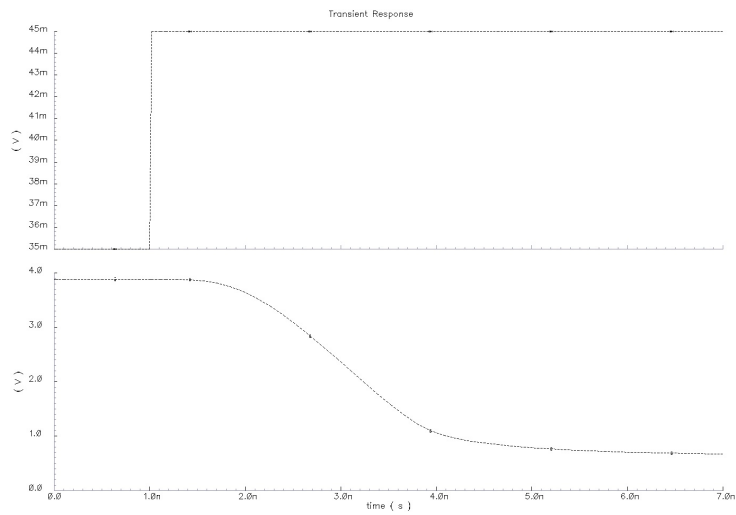


Figure 4.21: Transient performance of PMOS Comparator

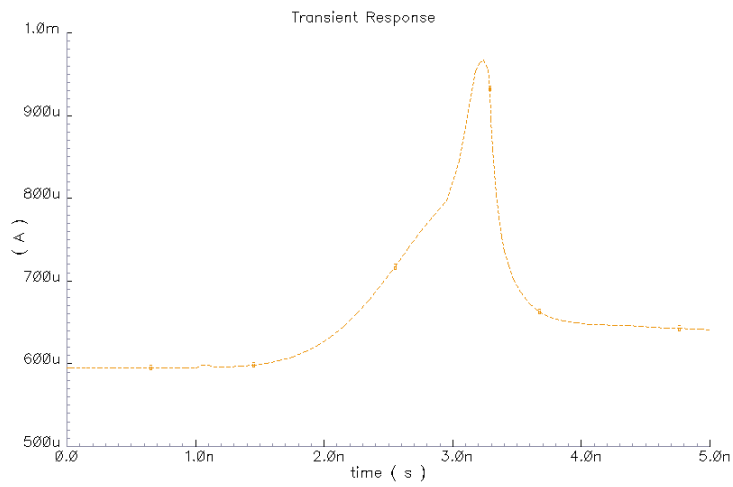


Figure 4.22: Power Supply Current of NMOS Comparator during Transient Analysis

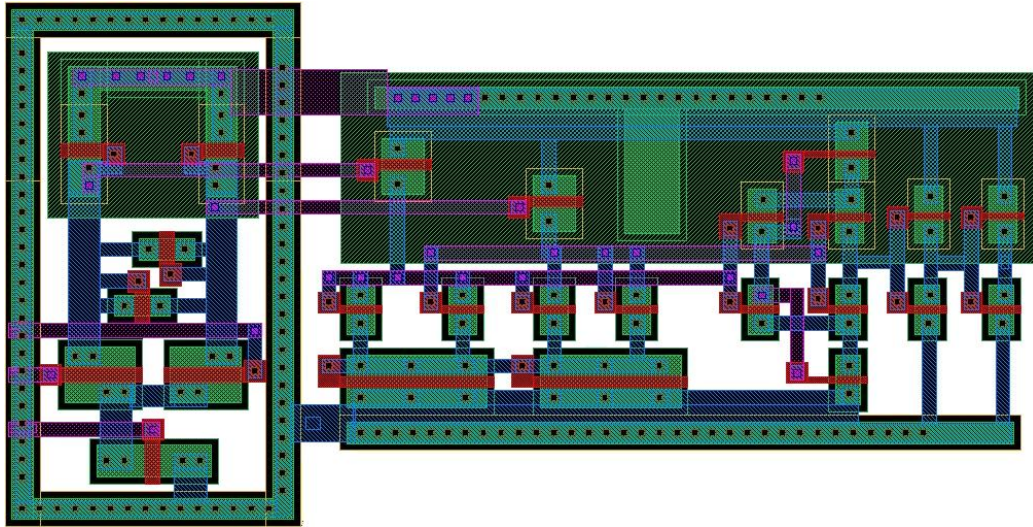


Figure 4.23: Layout of NMOS Comparator

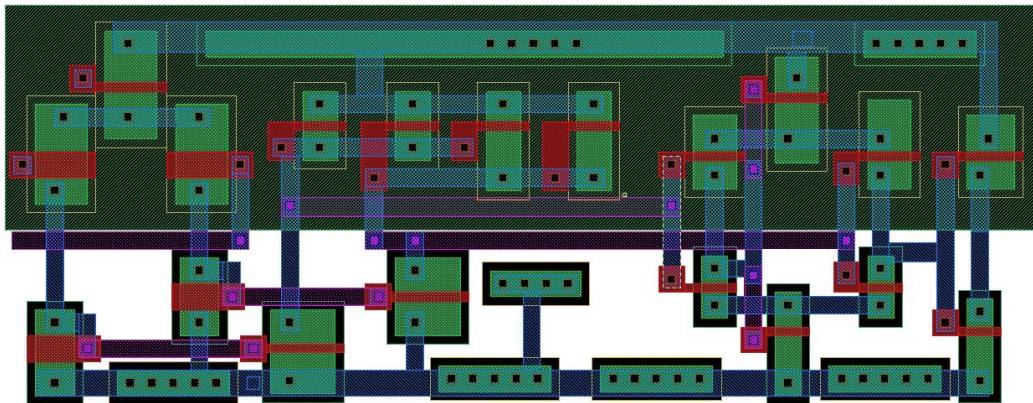


Figure 4.24: Layout of PMOS Comparator

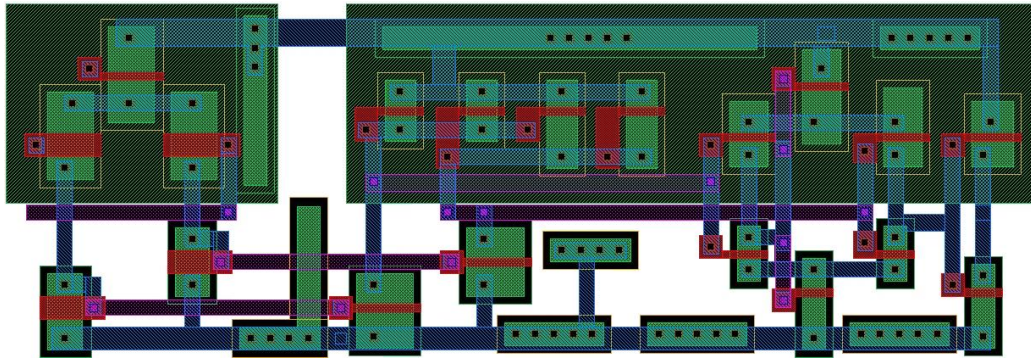


Figure 4.25: Layout of PMOS Comparator
Has added guard ring used with capacitive reference ladder

4.2 Digital Circuit Design

Analog-Digital Converters are mixed-signal circuits and as such must enter the digital realm at some point. This section deals with the three digital components in the circuit.

4.2.1 Encoders

The encoder converts the thermometer code output of the quantizer stage to binary numbers as shown in Table 4.5. Encoders are characterized by several parameters: power consumption, physical area, propagation delay, and error immunity. As part of ongoing work several designs were compared. 6-bit encoders were schematically drawn and evaluated for the above parameters. The three best performing designs were laid out to compare the area and extracted performance of the encoders. The results of this work are shown in Figure 4.4. Much of this schematic and layout work was done by Tyler Onufert [14] in addition to the author.

Design	$t_{longest}(ns)$	Transistors	Error Immunity
ROM	0.264	Max. 64x6	Quasi-Gray Code
ROM w/ 1ofN	1.642	668+Above	Rejection of First Order Bubble Errors
XOR Encoder	4.6	460	None
Wallace Tree	9.3	1938	Minimization of all bubble errors
Fat Tree	1.45	232	
Fat Tree w/ 1ofN	2.09	856	Rejection of FO Bubble Errors
L-Encoder	2.0	452	None
L-Encoder w/ Error Correction	2.5	1586	Rejection of All Single Bit Errors

Table 4.4: Comparison of Encoder Characteristics

Error Immunity

Error immunity is an important characteristic that can be used for comparison of the architectures and it is the ability to suppress or reduce the effects of bubble errors. There are two types of errors, bubble errors and metastability errors. Metastability errors occur when the digital signal is a voltage level in between the noise margin of the digital encoder. This results in neither a 1 or a 0 and this propagates through out the circuit. None of the architectures performs better than any other in so far as metastability errors are concerned. Circuits have been demonstrated to reduce metastability errors [19].

Encoders work by sensing the a 01 transition in the thermometer code, but what happens if there are two or more 01 transitions in the thermometer code. These are bubble errors and they are defined as having an order equal to the distance from the actual transition. 000101111 is a first order bubble error, while 0001001111 is a second order error⁹. First order errors are more common than second order, and second more common than third and so on. Rejection of first order errors is therefore more important than second order or higher errors. Some designs are capable of rejecting bubble errors and some also minimize the effects of a bubble error. This thesis explains the issues below.

Designs Considered

The standard encoder used in many Flash designs is a ROM-style encoder [27]. ROMs accept an input a single “1” as an address and then outputs the contents

⁹0001101111 is also a second order bubble error. Both zeros and ones can be bubble errors.

	Thermometer Code	1 of N	D3	D2	D1	D0
0	XXXXXXXXXXXXXXXXX1	0000000000000001	0	0	0	0
1	XXXXXXXXXXXXXXXXX10	0000000000000010	0	0	0	1
2	XXXXXXXXXXXXXXXX100	0000000000000100	0	0	1	0
3	XXXXXXXXXXXXX1000	0000000000001000	0	0	1	1
4	XXXXXXXXXXXX10000	0000000000010000	0	1	0	0
5	XXXXXXXXXX100000	0000000000100000	0	1	0	1
6	XXXXXXXXX1000000	0000000001000000	0	1	1	0
7	XXXXXXX10000000	0000000010000000	0	1	1	1
8	XXXXXX100000000	0000000100000000	1	0	0	0
9	XXXXX1000000000	0000001000000000	1	0	0	1
10	XXXX10000000000	0000010000000000	1	0	1	0
11	XXX100000000000	0000100000000000	1	0	1	1
12	XX1000000000000	0001000000000000	1	1	0	0
13	X10000000000000	0010000000000000	1	1	0	1
14	100000000000000	0100000000000000	1	1	1	0
15	000000000000000	1000000000000000	1	1	1	1

Table 4.5: Truth Table of Encoder

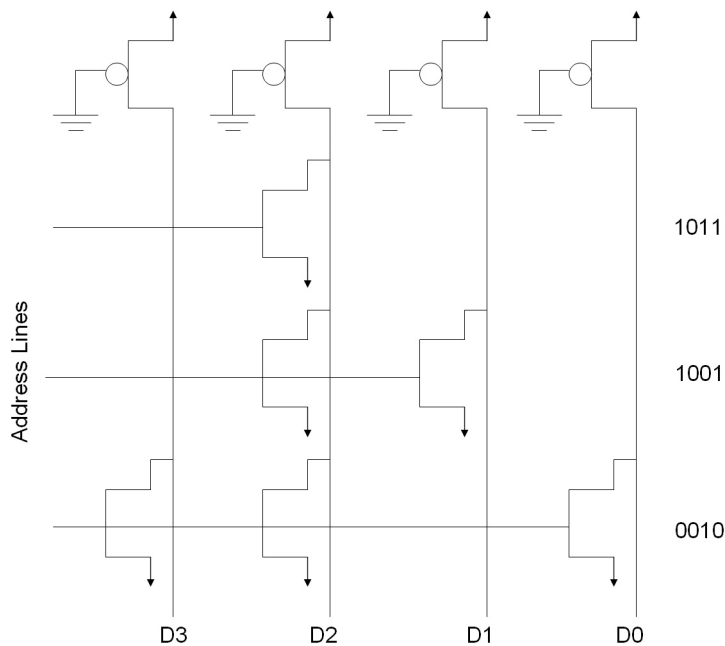


Figure 4.26: ROM Structure

of that address. The input is the 1-of-N and the output is $D_3D_2D_1D_0$ in Table 4.5. ROMs are small, fast, and accurate. A typical ROM structure is shown in Figure 4.26. Each bit D_n has a pull-up PMOS transistor and then each address has NMOS if the output will pull-down to low. When a high is put on an address line the output will be a “1” if there is no transistor and a “0” if there is a NMOS pull-down transistor. The power consumption of ROMs can be higher than other circuits because when the output goes low the circuit is still drawing power.

To generate the 1-of-N addresses, a 1-of-N converter is required (Figure 4.27). Since each bit requires an AND gate and an inverter¹⁰, this converter increases the size of the ROM encoder substantially. This leads to a significant increase in

¹⁰In practice NAND or NOR gates are used of course.

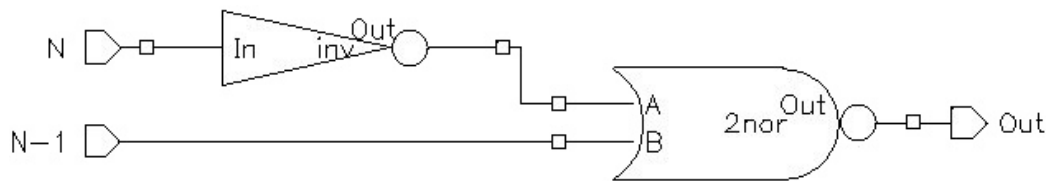


Figure 4.27: A 1-of-N Converter

size and delay, and begins to take away many of the advantages of the ROM. The 1-of-N converter of the test structures was a substantial portion of the final area.

A standard 1-of-N converter outputs a 1 at every 01 transition. If there are bubble errors, this can result in more than one high output. Looking at the structure this can lead to errors because the output bits will AND'ed together. For example in Figure 4.26 if inputs 2 and 3 are both high then the final output will be 0000 a significant error from either 1001 and 0010. The errors of a 4-bit binary encoder are shown in Table 4.6, and it can easily be seen that these errors can be quite large. The Up or Down notation refers to whether the correct bit is higher (Up) or lower (Down) than the bubble error.

The simplest form of error correction is by changing the two input AND to a three input AND and keeping the inverter on the lowest bit. This form of error correction turns 000101111 \Rightarrow 000001000 instead of 000101000 eliminating the bubble error. So it appears that this eliminates all first order bubble errors, however this assumes that the 1 is the error not the 0. A better method, which is a compromise is discussed in Section 4.2.2. This error correction has no effect on higher-order bubble errors, but since they are much lower in frequency than first order bubble errors this is still very effective.

Correct Output	FO Up	FO Up	FO Error	SO Up	SO Up	SO Down
0000	0000	0	-	0000	0	-
0001	0001	0	-	0000	1	-
0010	0000	2	2	0000	2	-
0011	0001	2	2	0010	1	3
0100	0100	0	4	0100	0	4
0101	0101	0	4	0000	5	5
0110	0000	6	2	0000	6	4
0111	0001	6	2	0010	5	3
1000	1000	0	8	1000	0	8
1001	1001	0	8	1000	1	9
1010	1000	2	2	1000	2	8
1011	1001	2	2	1010	1	3
1100	1100	0	4	1100	0	4
1101	1101	0	4	-	-	1
1110	-	-	8	-	-	4
1111	-	-	8	-	-	3

Table 4.6: Bubble Errors of a Standard Binary ROM

Since these errors can be large, alternate encoding schemes have been developed. Three encoding schemes will be discussed. Gray Code is a common encoding of binary information and has the best error suppression, since the maximum error is the same as the order of the bubble error (plus one)[16]. This minimizes the effect of the bubble errors. The conversion to binary, however is difficult resulting a series connection of $N - 1$ XOR gates. XOR gates are not well suited to CMOS logic families, so this dramatically increases the delay of the circuit. An encoding was proposed to reduce this delay down to a single XOR gate delay, by using Quasi-Gray encoding [15]. This encoding has good error minimization, not as good as Gray, but better than binary. With most designs this speed up is worth the reduced noise minimization, hence this is a very common encoding.

An interesting encoding scheme is the Flipped Brick encoding [17] named after the method with which the encoding is calculated. This encoding was found to have a noise power less than both the Gray and Quasi-Gray encodings. This reference also presents a method of calculating the noise power of any encoding scheme. Flipped Brick encoding conversion to binary encoding is longer than Quasi-Gray but shorter than Gray encoding ($N - 3$ delays). Flipped Brick is better than Gray code in all respects and is a powerful alternative to Quasi-Gray if error minimization is more important than speed¹¹. Table 4.7 shows 4-bit encodings of all the schemes discussed in addition to L-encoding, which was used in this design.

The next design considered after the ROM was an XOR encoder, which is

¹¹Or if effective pipelining can be used.

Decimal	Binary	Gray	Quasi-Gray	Flipped Brick	L-Encoding
0	0000	0000	0000	0100	0000
1	0001	0001	0001	0101	0001
2	0010	0011	0011	0110	0011
3	0011	0010	0010	0111	0010
4	0100	0110	0111	0000	0100
5	0101	0111	0110	0001	0101
6	0110	0101	0100	0010	0111
7	0111	0100	0101	0011	0110
8	1000	1100	1111	1011	1000
9	1001	1101	1110	1010	1001
10	1010	1111	1100	1001	1011
11	1011	1110	1101	1000	1010
12	1100	1010	1000	1111	1100
13	1101	1011	1001	1110	1101
14	1110	1001	1011	1101	1111
15	1111	1000	1010	1100	1110

Table 4.7: Comparison of Encodings Available

composed of a large array of XOR gates[21]. The XOR encoder was originally designed for bipolar logic where an XOR is a simple gate. In CMOS, XORs are large slow gates so this design is not appropriate, although the number of transistors is very low. The XOR encoder was very slow in CMOS.

The Wallace Tree Encoder is based upon Wallace Tree Multiplier [22], a fast method of doing binary multiplication, which is typically a slow process. The Wallace Tree uses a cascade of simple adders to perform the multiplication quickly. The basic premise of the Wallace Tree Encoder is that the binary output is the number of zeros¹² on the thermometer input code[24, 23]. This is accomplished by adding using a cascade of simple adders as described in the original paper. The advantage of the Wallace Tree is the noise minimization, since a bubble error results in an output change of the number of extra ones. This can minimize the effects of bubble errors and is the only circuit to minimize wide bubble errors such as 0011000011111111. The first two ones would result in an output change of two while all other error corrections would lead to an extra transition. The Wallace Tree has been evaluated and widely promoted [28], but our tests show that it is very large and slow in CMOS. For high speed Flash implementations, this is not an appropriate choice.

The Fat Tree encoder was proposed as an alternative to ROM encoders[26]. The structure is a bit symmetric tree of OR gates and requires a 1-of-N converter. The Fat Tree ORs together all the bits which result in an output of one, i.e.

¹²All of these designs are using active-low logic. There is little difference between a active-low and active-high logic.

$D_0 = T_1 + T_3 + T_5 + T_7 + T_9 + T_{11} + T_{13} + T_{15}$ and $D_1 = T_2 + T_3 + T_6 + T_7 + T_{10} + T_{11} + T_{14} + T_{15}$. One of the advantages of this design is that each bit has the same number of gates to go through, leading to an equal propagation delay. The design is very fast as well, but according to the simulations it was not as fast as the ROM.

A design for a priority encoder can be found using standard digital design techniques such as Karnaugh Maps and the truth table in Table 4.5 and one is shown in Figure 4.28a. A priority encoder of this form will have a lower level of complexity than a Fat-Tree encoder. The least significant bit will have the same number of gates, but the next bit will have half, and the third bit half the second, and so on. This reduces the total number of gates compared to a Fat Tree Encoder, but the design becomes irregular.

L-Encoder was Chosen

An improvement over the standard priority encoder is shown in Figure 4.28b. This design is based around a different encoding scheme referred to as L-Encoding in Figure 4.5. This scheme was developed by the author and is further developed in [14]. The basic difference between L-Encoding and binary is the LSB. The LSB has been changed to reduce the number of transitions on the bit. This reduces the number of gates on the LSB in half and reduces the total number of gates by 25%. This results in a similar reduction in power dissipation and reduction of a gate delay. The conversion from L-encoding to binary is achieved through XOR'ing the two least significant bits. This is a much easier conversion than the

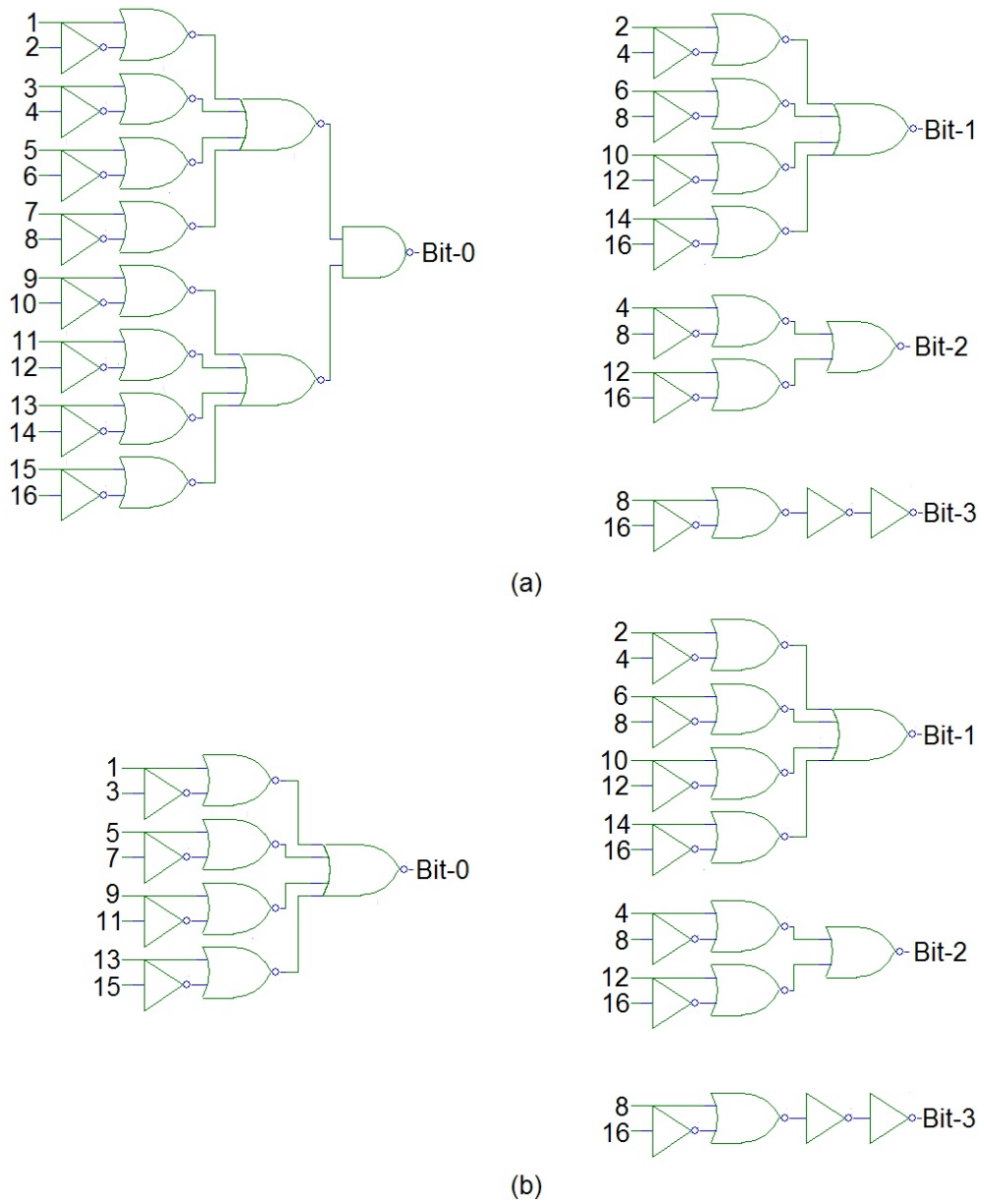


Figure 4.28: Schematic of (a) a Binary Encoder and (b) the L-Encoder

Encoding Scheme	# XORs	Gate Delays
Gray	N	N
Quasi-Gray	N	1
Flipped Brick	N	N-3
L-Encoding	1	1

Table 4.8: Comparison of the Encoding Scheme Conversion to Binary

other encoding schemes as shown in Table 4.8.

This design took the results of that study and used an L-Encoder, since it was high speed and low power. The other circuit that would have been used is the ROM, but the researchers also wanted to test the L-Encoder design. The schematic of the encoder is shown in Figure 4.29, which is slightly different than Figure 4.28b. The circuit was simulated to have a maximum delay of $2.7ns$ as shown in Figure 4.30. The maximum peak power consumption was found to be 30mW as shown in Figure 4.31. This was tested using the entire digital backend, not just the L-Encoder. The circuit was laid out using optimized gates for the process. These gates were laid out and the encoder is shown in Figure 4.32. The area of the encoder was $593 \times 62\mu m$.

4.2.2 Error correction

The error correction used was democratic error correction proposed by Mangelsdorf [18]. The output bit is chosen based on voting by the bit and its two neighbors, with the majority of them being output as in Table 4.9. The logic for this $B = AB + BC + AC$ and is simple to develop such as Figure 4.33. This must be done for each bit. This circuit adds a delay and increases size and power, but

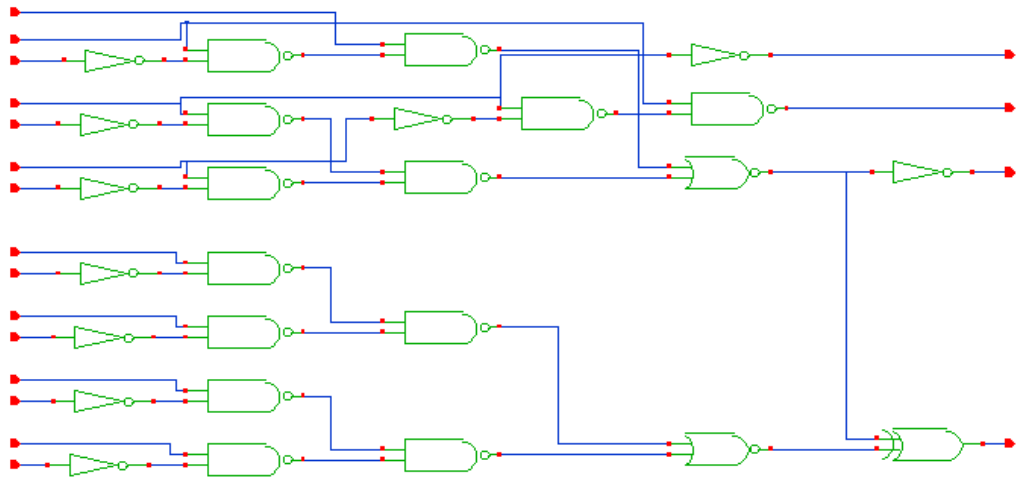


Figure 4.29: Schematic of Encoder Used

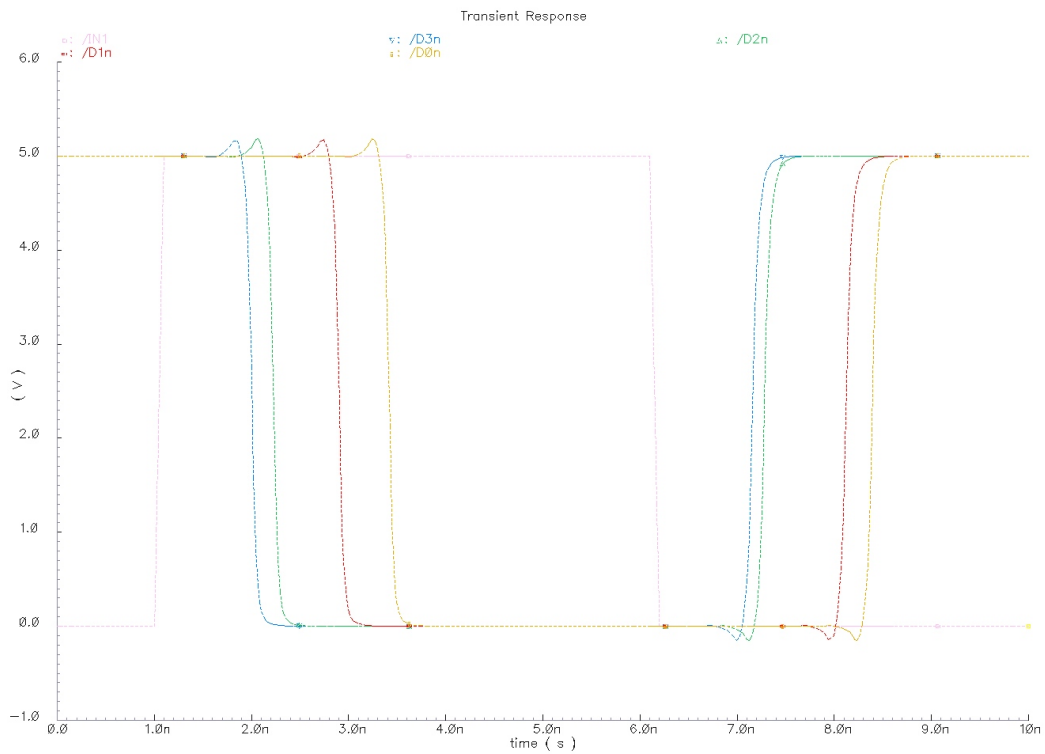


Figure 4.30: Delay of Output Bits of the Encoder

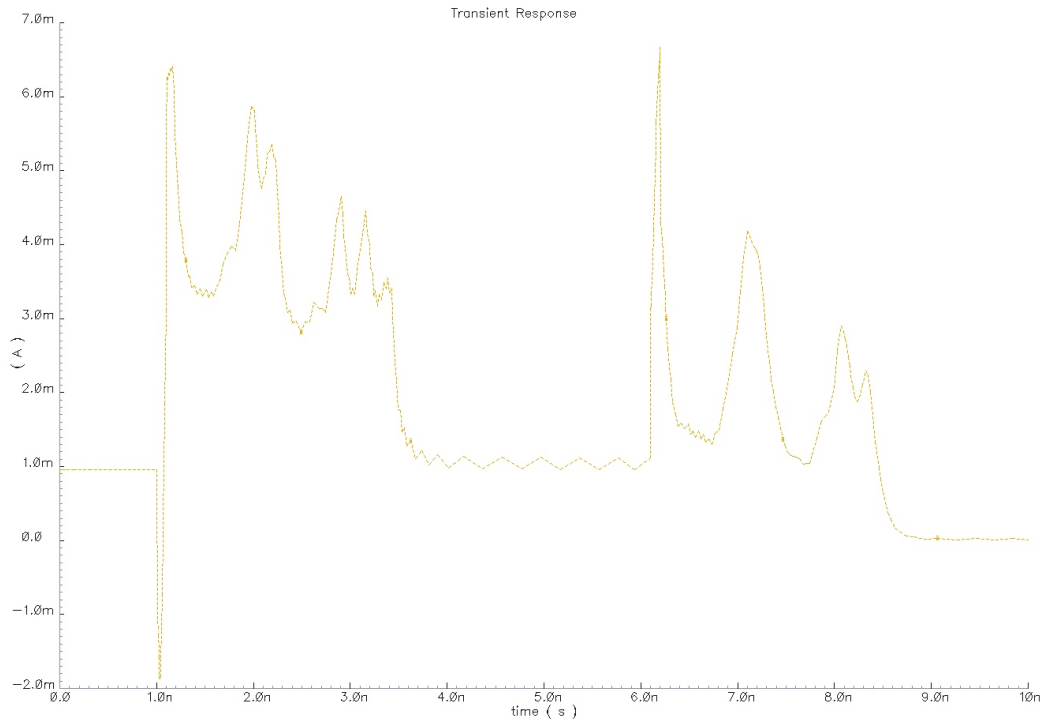


Figure 4.31: Power of Encoder

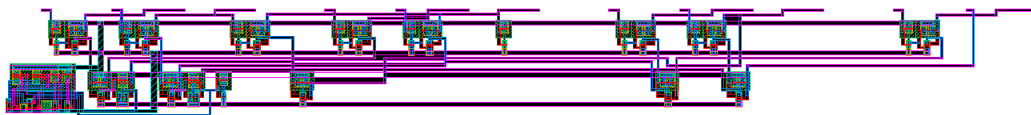


Figure 4.32: Layout of the encoder

Input	Output
000	0
001	0
010	0
011	1
100	0
101	1
110	1
111	1

Table 4.9: Truth Table of the Mangelsdorf Error Correction

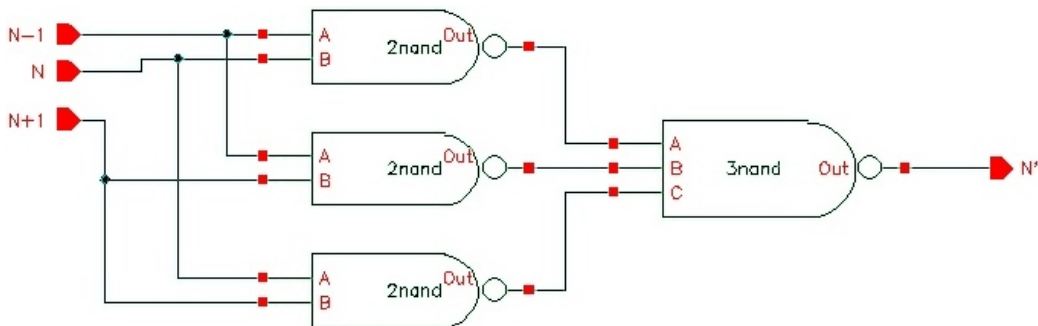


Figure 4.33: Schematic of the Error Correction

it eliminates all first order bubble errors. This is even better than basic error correction since it can do some averaging i.e. 0010111 \rightarrow 0001111 not 0000111 and the first is probably a better answer. Since there are a large number of signal-dependent transient issues, the design placed a heavy emphasis on the error correction. The error correction was used to eliminate the effects. The layout for the circuit is shown in Figure 4.34.

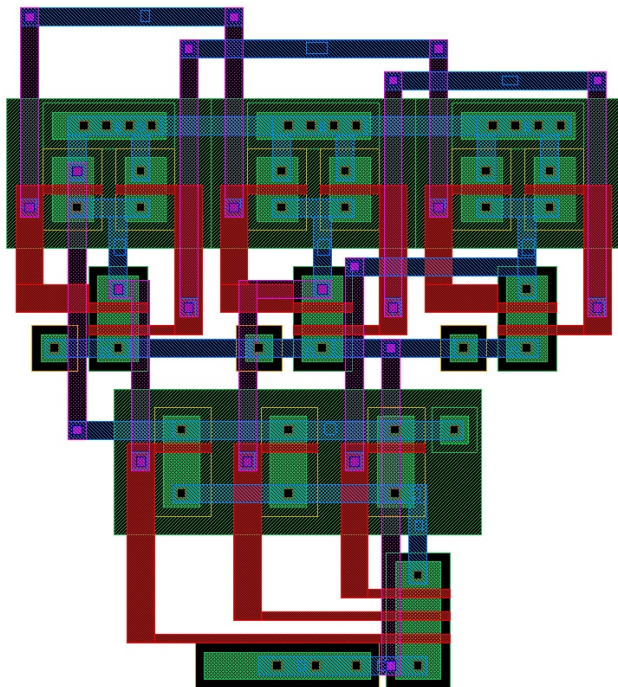


Figure 4.34: Layout of Error Correction

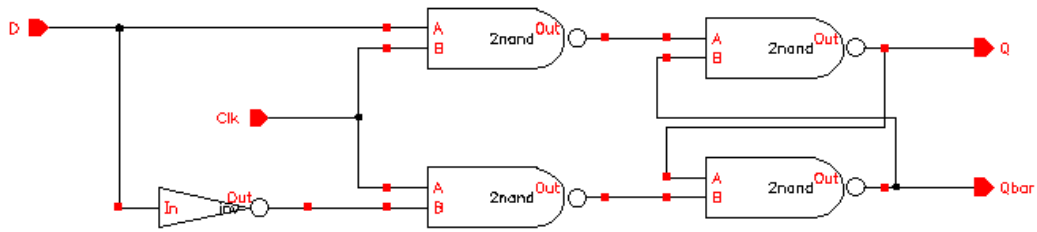


Figure 4.35: Schematic of a D Flip-Flop

4.2.3 Output Buffer and Flip-Flops

The output of the encoder is connected to D flip-flops. The D flip-flops are clocked by the digital clock line and are used to prevent a single output despite the different propagation times through the encoder. The unlatched outputs were included in the three of the designs previously discussed, to eliminate a signal required during testing. The schematic and layout of the flip-flops and output buffers are shown in Figures 4.35 and 4.36 and Figures 4.37 and 4.38, respectively.

Output buffers were used to drive the output pins. This was done by cascading a series of increasing inverters, until the proper driving ability was achieved as described in [32]. Four inverters with increased sizes were used to drive the capacitance of the output pins, which was extracted to be $2 \times 10^{-13} F$. The output buffers need to be increased, in order to drive the 10pF probes, and will be done in the next iteration.

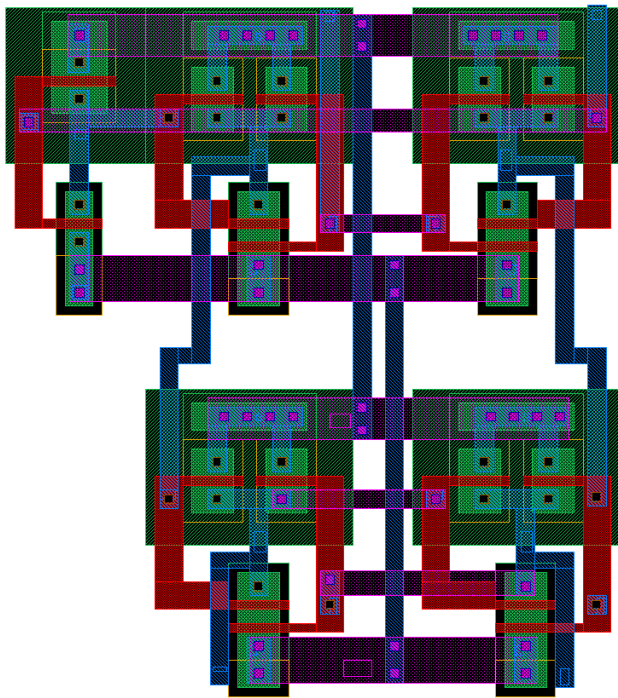


Figure 4.36: Layout of a D Flip-Flop

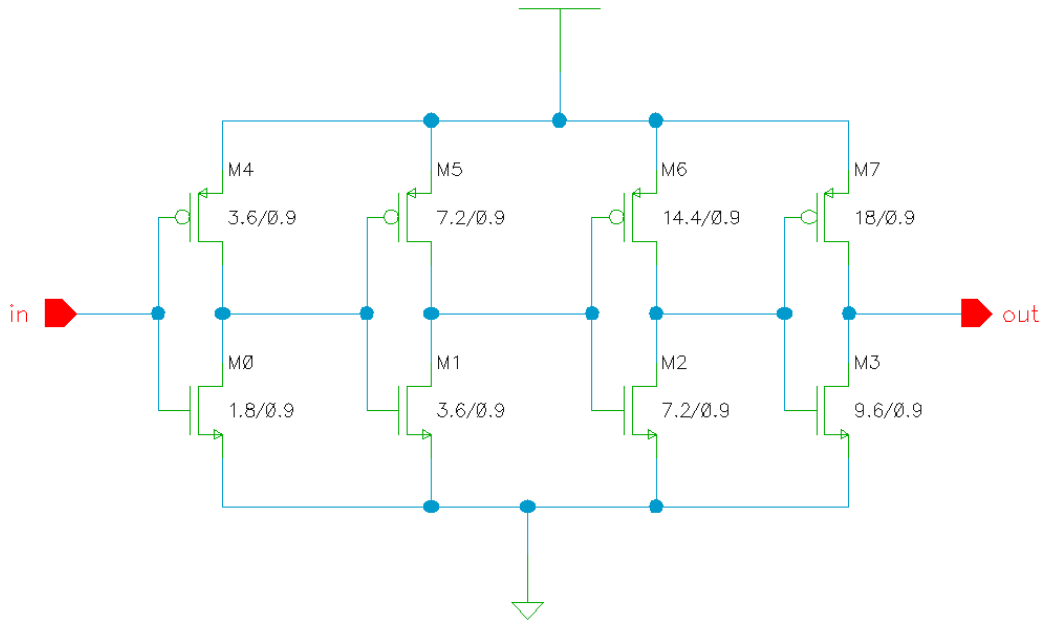


Figure 4.37: Schematic of the Output Buffer

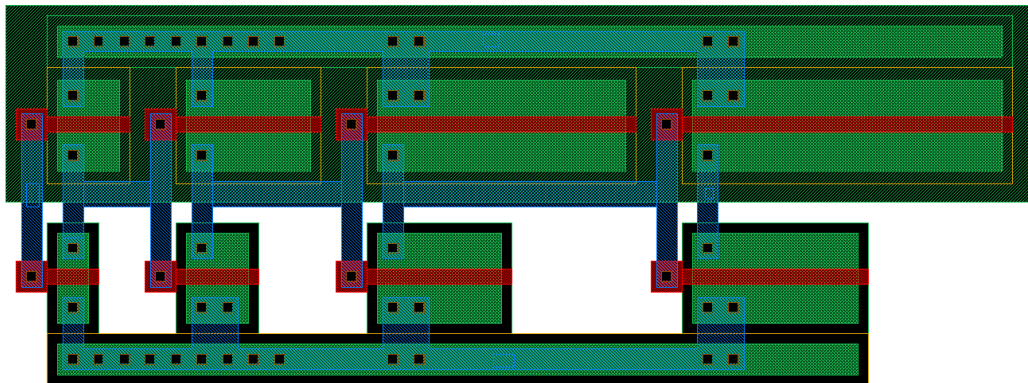


Figure 4.38: Layout of the Output Buffer

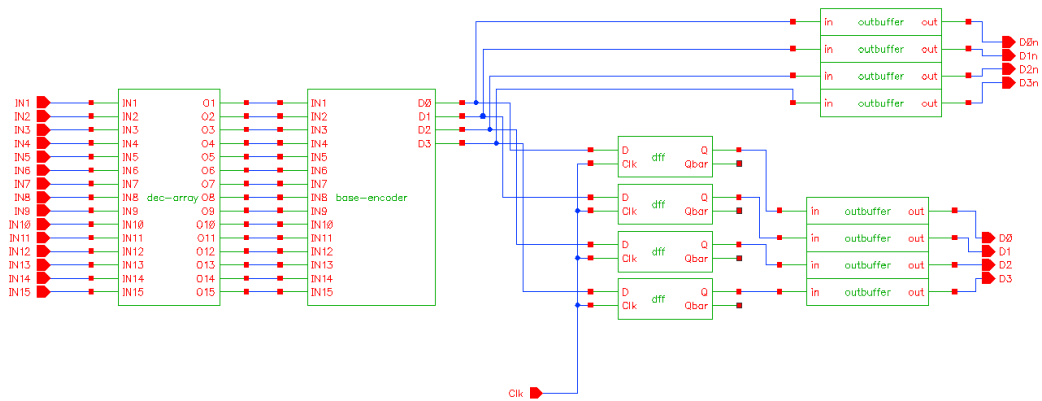


Figure 4.39: Schematic of Digital Backend

4.3 Final Mixed-Signal Circuit

The compressing ADC is composed of two distinct parts, analog and digital, as outlined in sections 4.1 and 4.2. In that way they could be brought together as two separate parts. This does not allow for further optimization, but it simplified the design. The same digital section was used in all chips, except the chip A did not have unlatched outputs. The digital circuit is shown in Figure 4.39. The analog frontend is different for each chip with the different components listed in Table 4.1. The schematics of some of the chips are shown Figures 4.40 and 4.41.

The results from the previous section should give us an accurate understanding of the characteristics of the design, however it is important to work with a circuit as a whole to ensure there are no unusual interactions. To understand and confirm the analytical results in Chapter 3, the first simulation was a DC sweep with different reference voltages. These were done on Chip-A and the results (Figures 4.42, 4.43, 4.44, and 4.45) confirm the the analytical results. Chip B was also tested

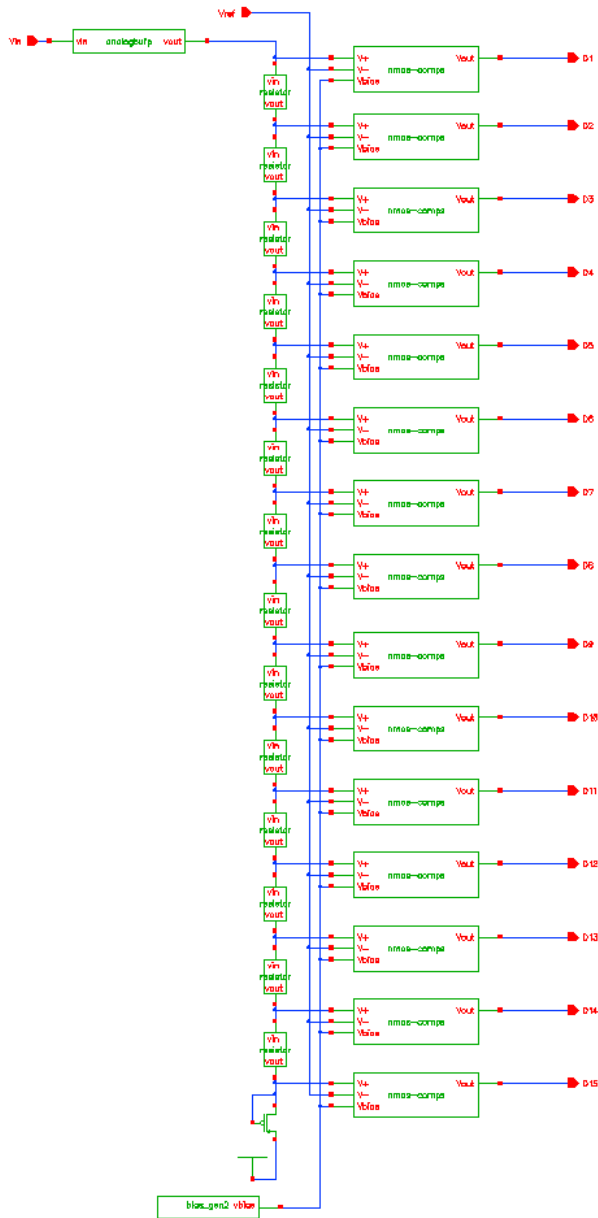


Figure 4.40: Schematic of Chip-B Analog Frontend

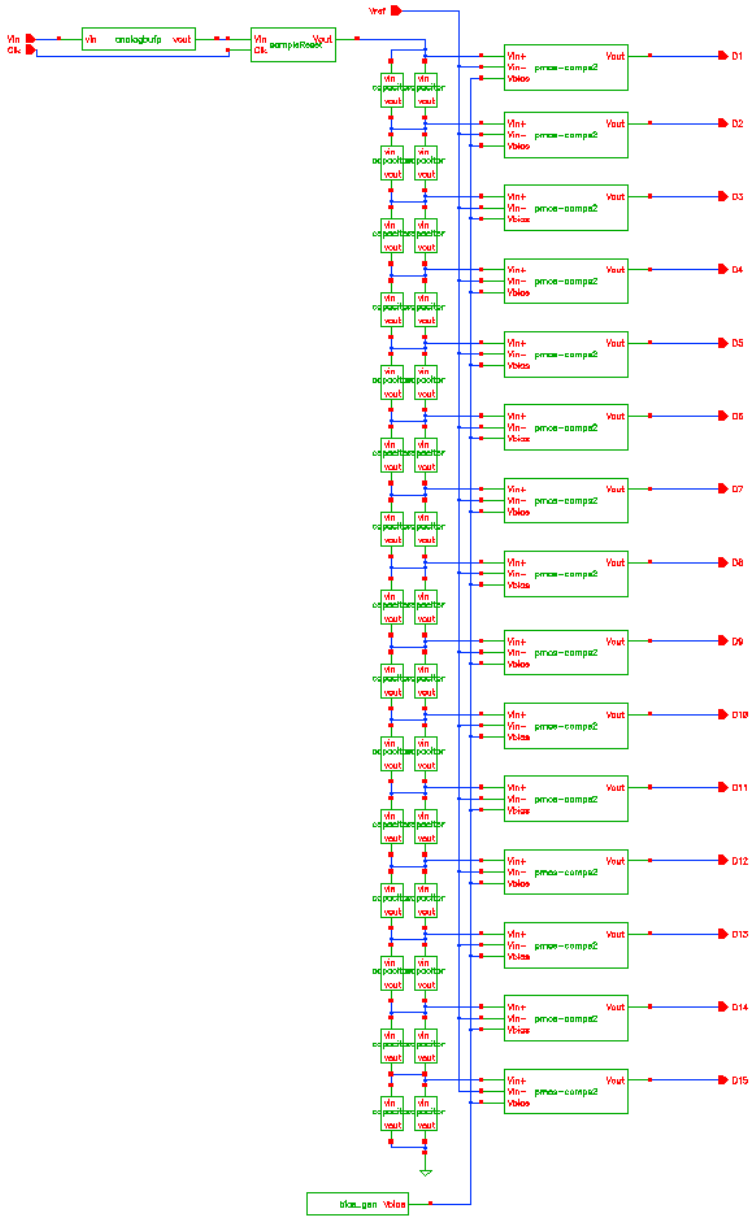


Figure 4.41: Schematic of Chip-D Analog Frontend

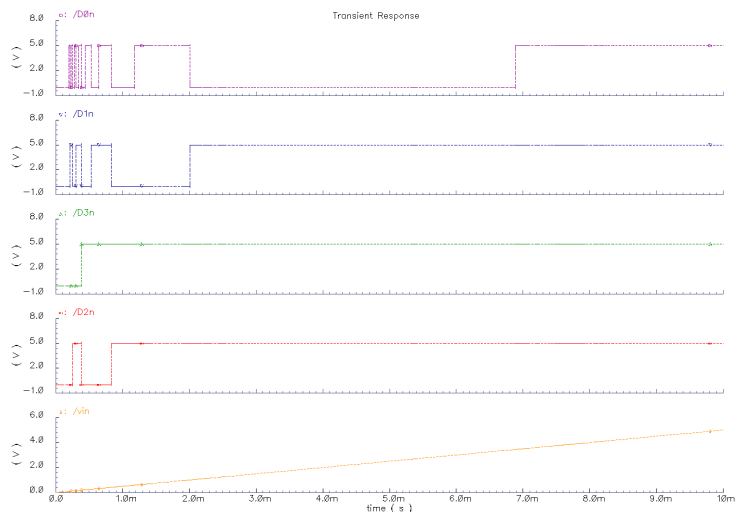


Figure 4.42: Bitwise Output of ADC A ($V_{ref}=100mV$)

with a $V_{ref} = V_{dd} - 1.05V$ and this is shown in Figure 4.46.

A very slow transient analysis was performed to try to capture the DC characteristics of the capacitive reference ladder, Chip D, and this was the first sign of concern. The “DC” sweep is shown in Figure 4.47 and this shows that the circuit appears to be working, except the last bit is missing. The conditions for this sweep were a $t_{rise} = 10ms$, $V_{pulse} = 0 - 5V$, and $V_{ref} = 10mV$.

The next step was to analyze the propagation delay of the entire chip. The maximum delay will occur on the analog side on the highest bits, and on the digital side will occur on the LSB output bit. Therefore the longest single bit delay should be on the LSB of $1110 \rightarrow 1111$, but the longest overall delay will be a $0000 \rightarrow 1111$. The transition from $0000 \rightarrow 1111$ will have the highest power consumption since the most number of gates are making transitions. It makes sense to test on this worst case transition, so a $V_{pulse} = 0 - 5V$, $t_{rise} = 100ps$, and

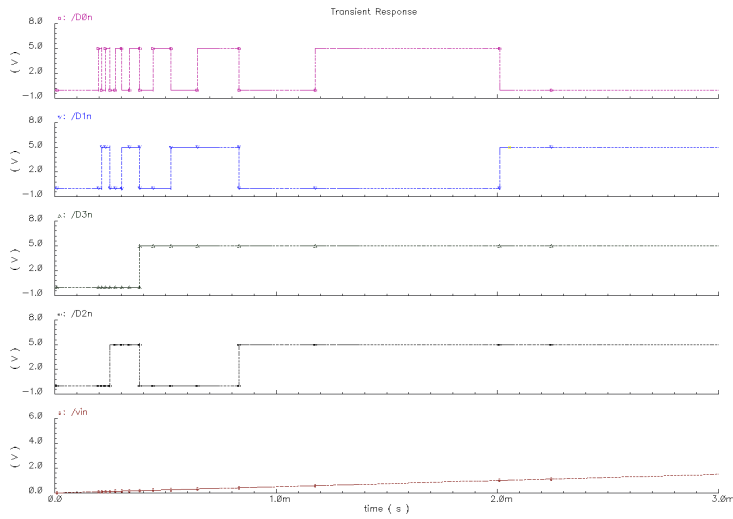


Figure 4.43: Lowest Bitwise Output of ADC A ($V_{ref}=100\text{mV}$)

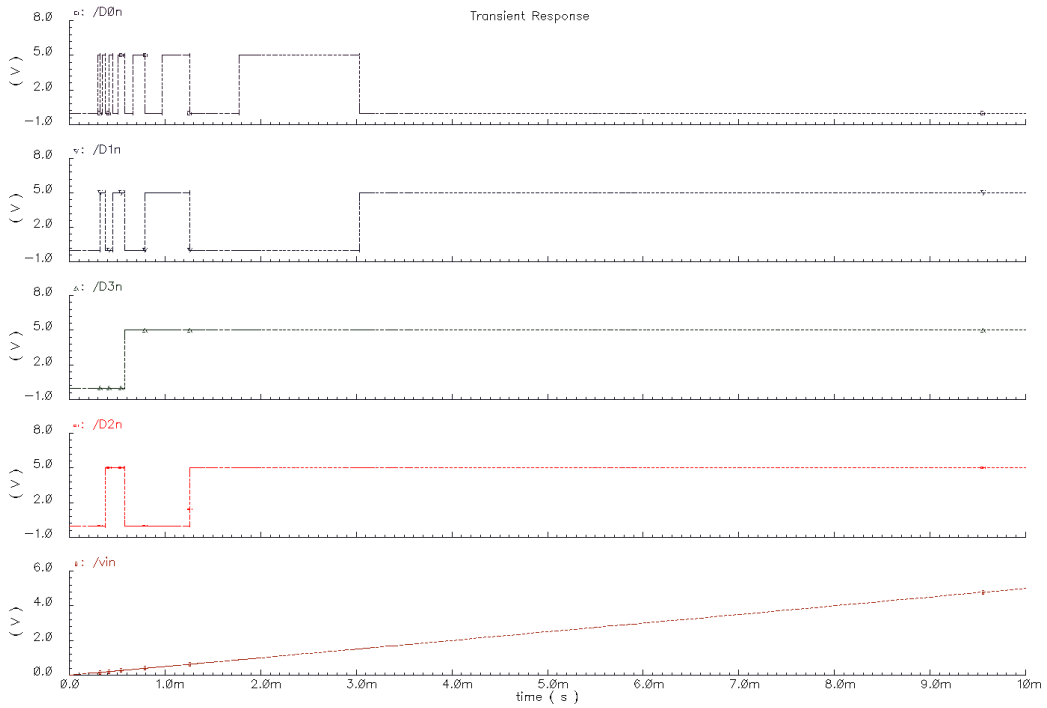


Figure 4.44: Bitwise Output of ADC A ($V_{ref}=150\text{mV}$)

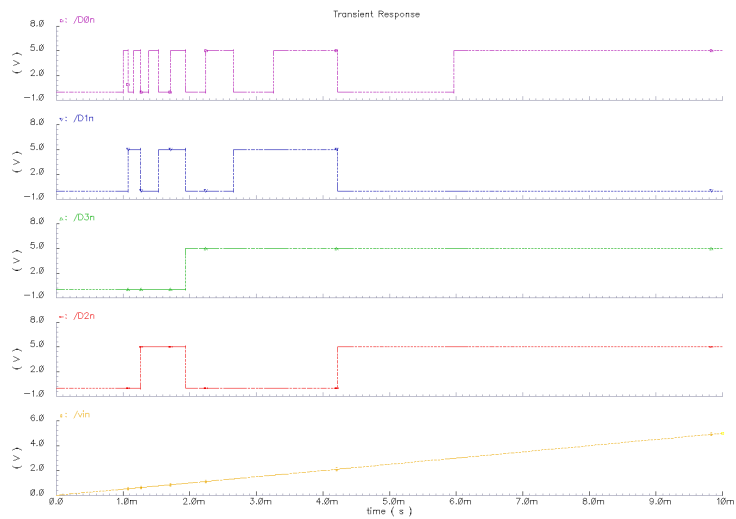


Figure 4.45: Bitwise Output of ADC A ($V_{ref}=500mV$)

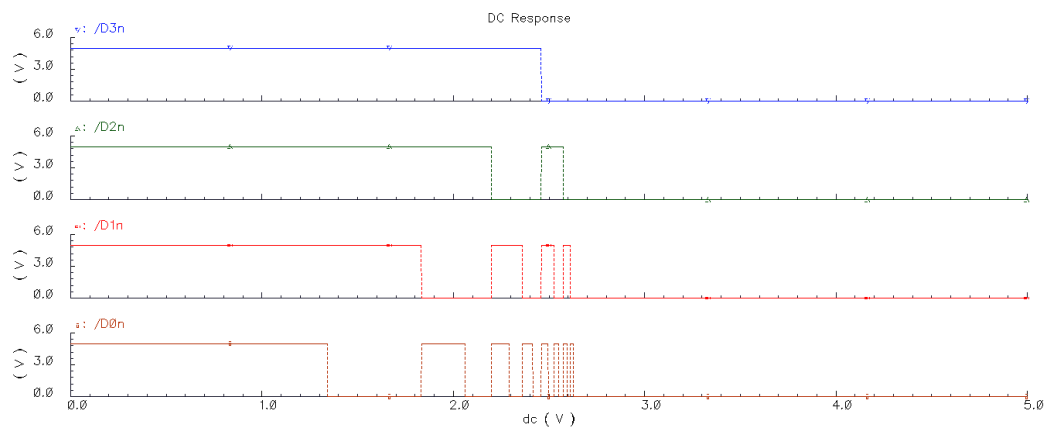


Figure 4.46: Transfer Function of Chip B

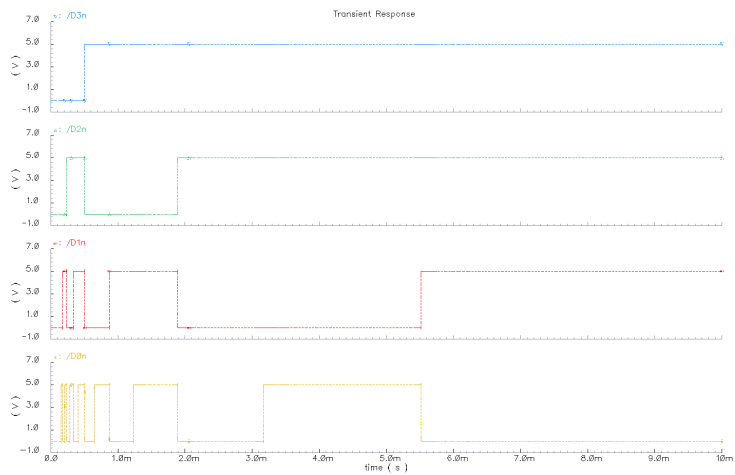


Figure 4.47: "DC" Analysis of Chip D

$V_{ref} = 100mV$ was used and the transition time and power consumption were measured (Figure 4.48 and 4.49). The longest delay was found to be about $12ns$ and the nominal and peak power are $46mW$ and $76mW$, respectively. This leads to maximum operating speed of about $80MHz$. Since the encoder delay was about $3ns$ and the total circuit delay was $12ns$, it can be inferred that the analog frontend is the dominant factor in determining circuit speed. Chip D was tested with a pulse to find the transient delay through the circuit. The delay through the comparators was found to be less than $3ns$ as shown in Figure 4.50. The signal will also begin to leak through the sample/hold and charge up the capacitive ladder in a matter of milliseconds. This sets a minimum frequency the chip convert. All simulations were post-extraction.

The frontends were connected in a standard frame. Any input sections, such as the buffer or sample and hold, were all in one area, and the reference ladders and the comparators in a single array. Chip B and Chip D are frontends and are shown

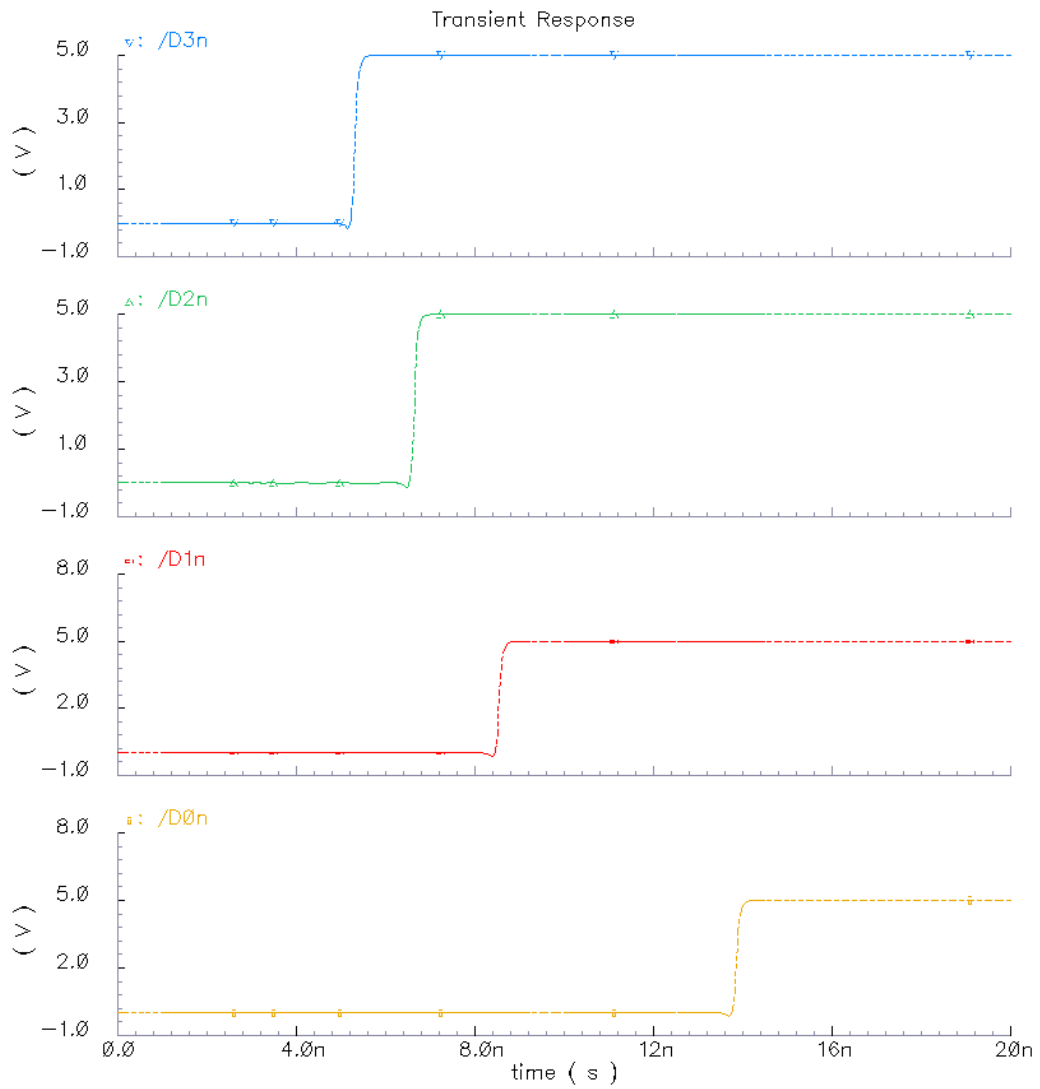


Figure 4.48: Transient Analysis of Chip B

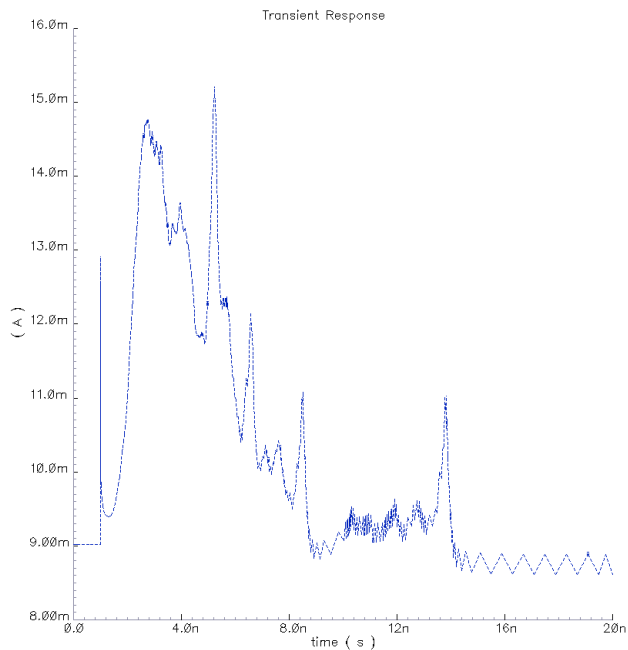


Figure 4.49: Power Supply Current of Chip B

in Figure 4.51 and 4.52. A close-up look at the input sections of these frontends is given in Figure 4.53 and 4.54. The layout of the digital backend is shown in Figure 4.55.

The final layouts of each chip are shown in Figures 4.56, 4.57, 4.58, and 4.59. Since the circuits all basically used a standard frame the area of all the chips is about the same at $680 \times 320 \mu m = 0.18 mm^2$.

Baker outlined some techniques that can be used to reduce noise coupling between the analog and digital circuits[32]. The main problem is that the large transient swings of the digital circuitry capacitively couples a lot of noise into the substrate and causes noticeable voltage dips in the power supply. To reduce substrate coupling the digital and analog sections are surrounded by guard rings.

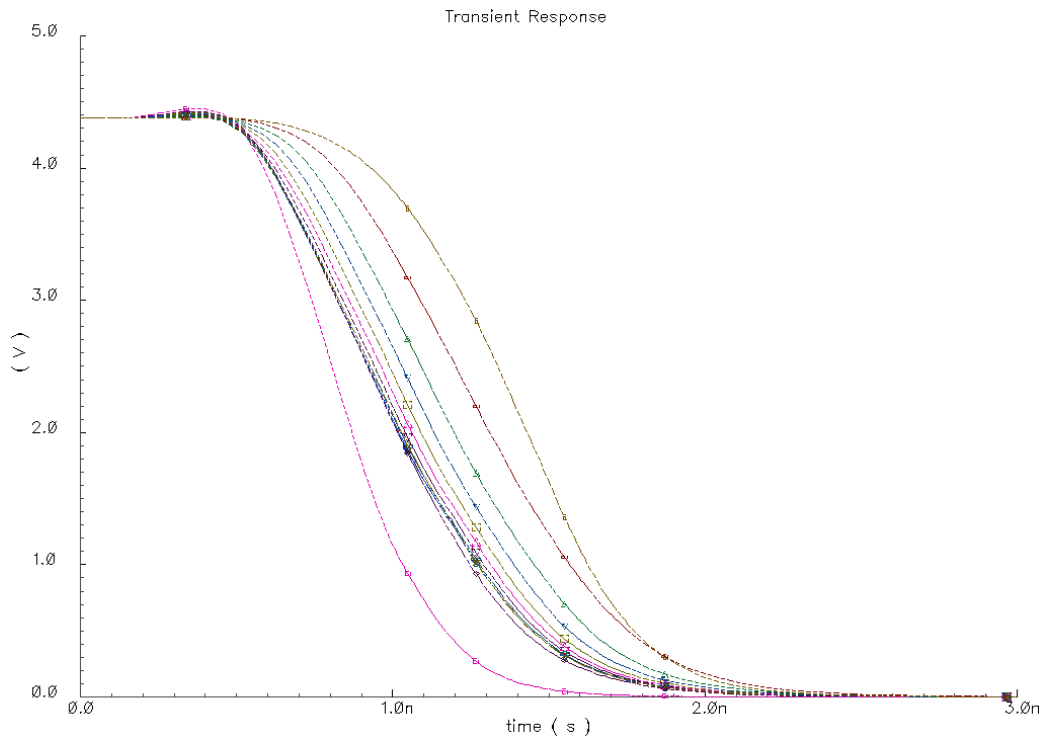


Figure 4.50: Capacitive Ladder Transient Response

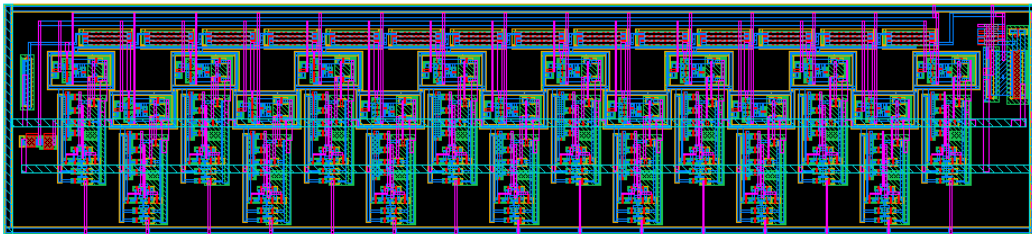


Figure 4.51: Layout of Chip B Frontend

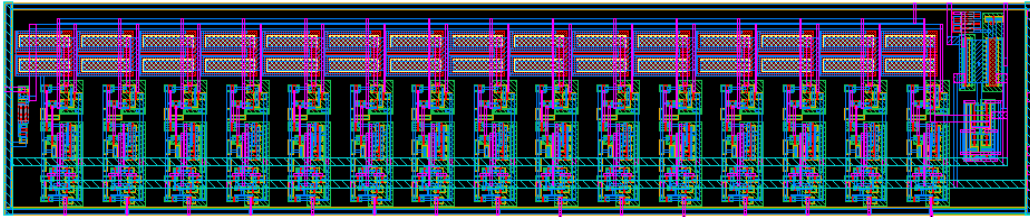


Figure 4.52: Layout of Chip D Frontend

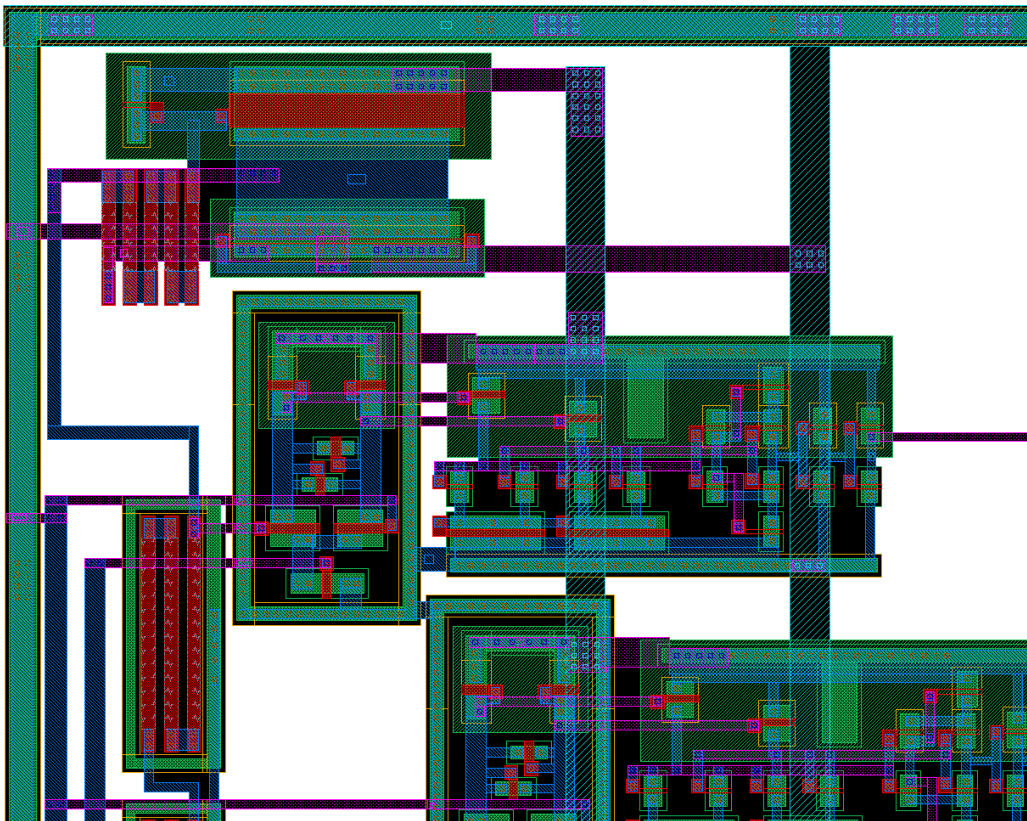


Figure 4.53: Close-up Layout of Input of Chip B

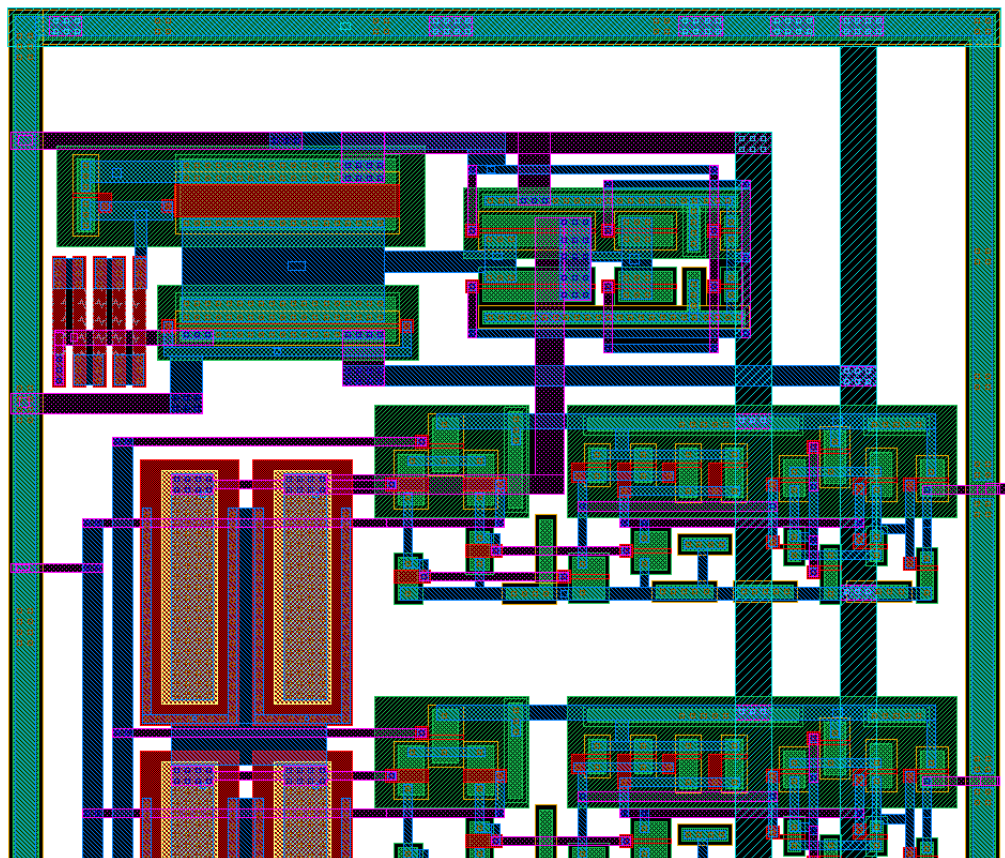


Figure 4.54: Close-up Layout of Input of Chip D

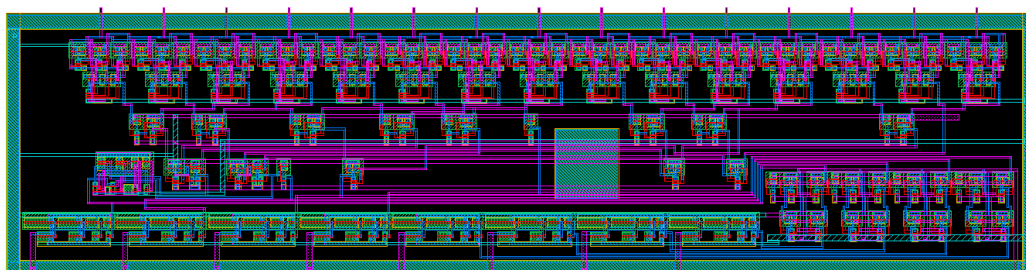


Figure 4.55: Layout of the Digital Backend

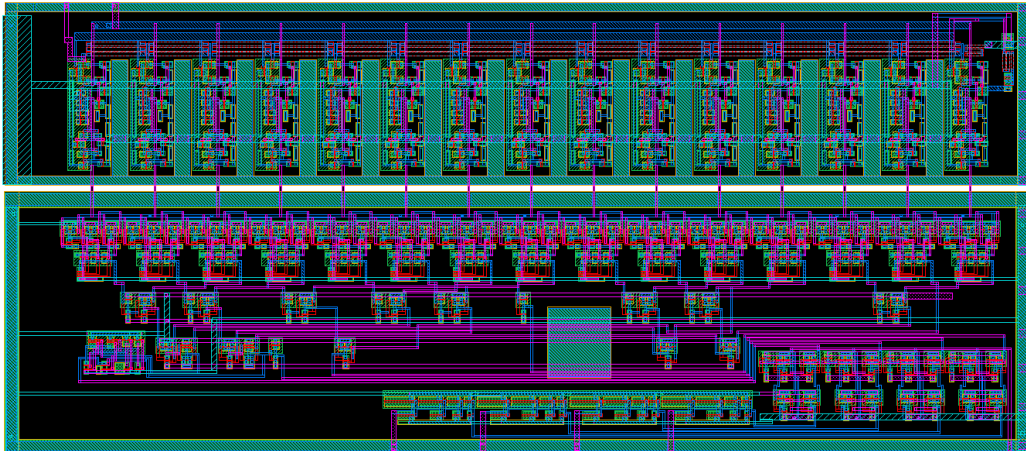


Figure 4.56: Layout of the Complete Chip A

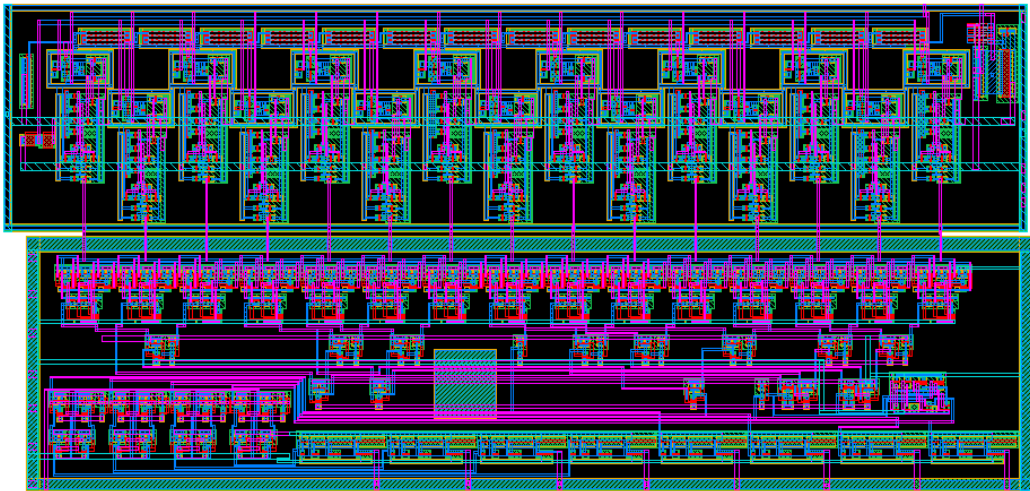


Figure 4.57: Layout of the Complete Chip B

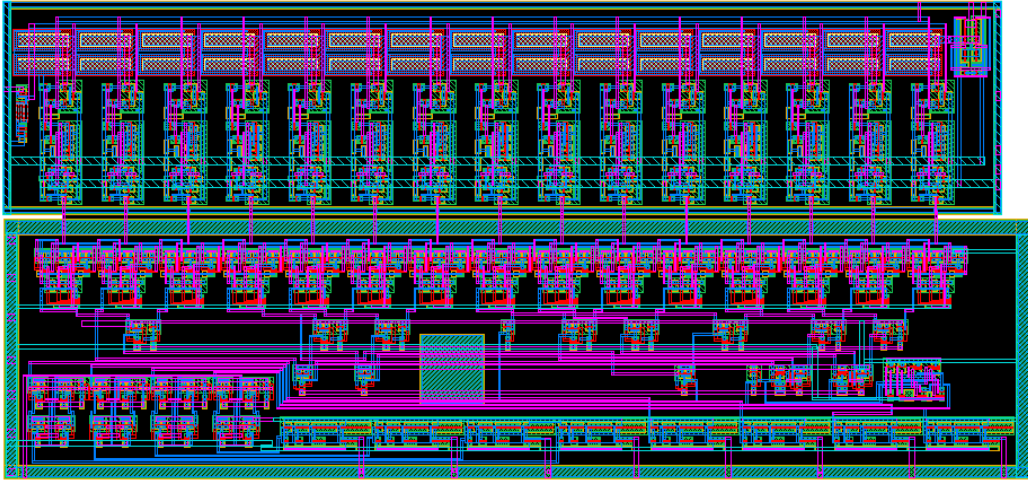


Figure 4.58: Layout of the Complete Chip C

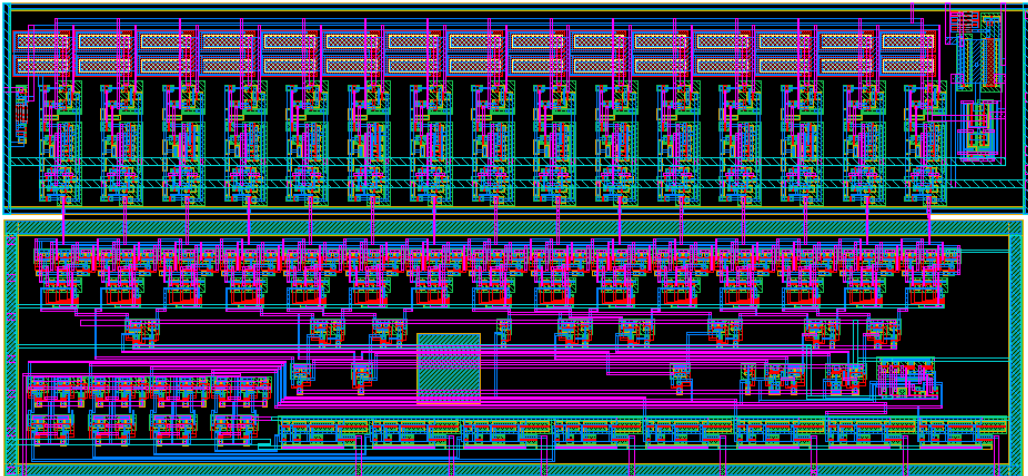


Figure 4.59: Layout of the Complete Chip D

These merely consist of p+ diffusions surrounding the circuits. The input circuitry is also kept physically far from the digital circuitry.

The circuit was designed to use only a single power supply. To reduce the coupling of the power signals between the digital and analog sections the power was brought off the rails using distinct metal lines for each. This is shown in the complete layout in Figure 4.60

Each layout went through LVS and extraction and passed both at the component level and the entire circuit.

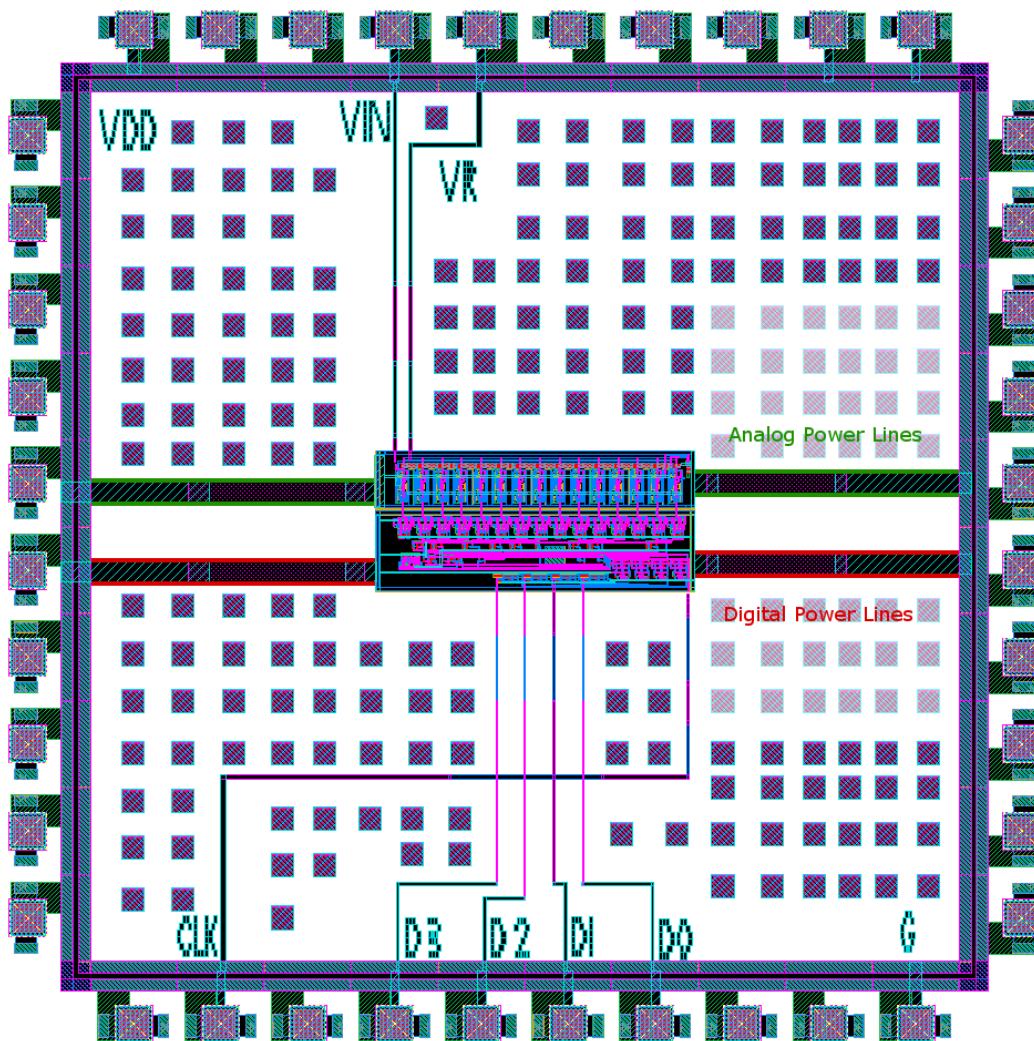


Figure 4.60: Layout of Chip A showing Separate Power Lines

Chapter 5

Testing

The compressing ADC is a novel design, so much needs to be proven. The non-linear design makes the characteristics harder to determine, since there is not a standard set of characteristics for nonlinear ADCs. The main characteristics that were tested were the transfer function, power consumption, and the propagation delay. Propagation delay was limited by the test equipment.

The converter testing was done at the Naval Research Lab in Washington, DC. Seokjin Kim did much of the lab work under the supervision of F. Keith Perkins. The tests were outlined by the designer and the tests were designed with the help of Mr. Kim.

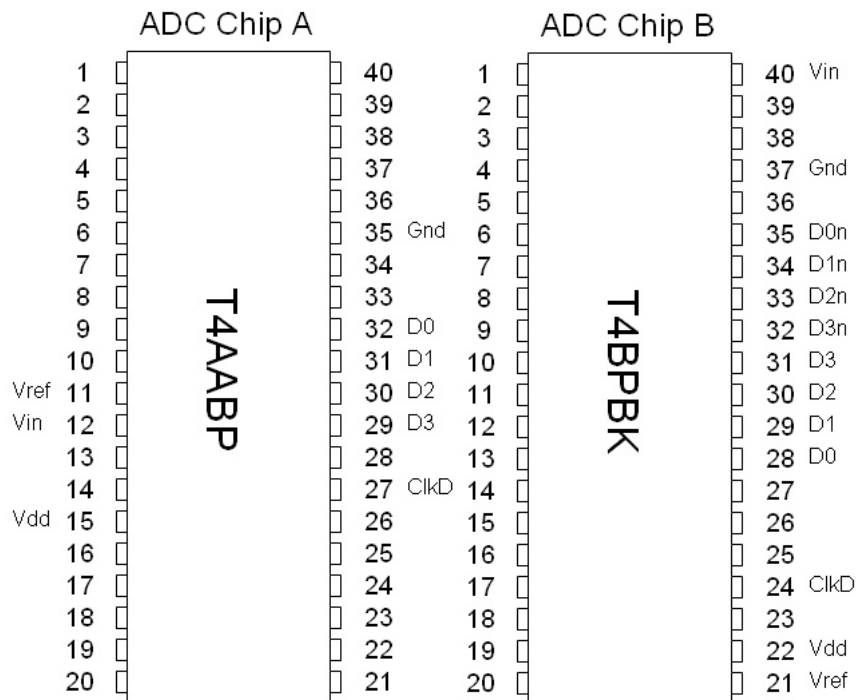


Figure 5.1: Pin-outs of ADC-A and ADC-B

5.1 Test setup

Four circuits were manufactured and packaged by MOSIS in DIP40 packages. The pinouts of these circuits and chips is shown in Figures 5.1 and 5.2. The standard connections are the same between these chips. The D*n pins are the unlatched digital outputs. ClkA is the clock signal for the sample and hold and ClkD is the clock for the D flip-flops.

The test equipment available is limited and has limited the tests run. The power supply is a Keithley 2400 at 5V. The reference voltage is from a Stanford lock-in amplifier. The lock-in amplifier also provides the digital clock and is limited to

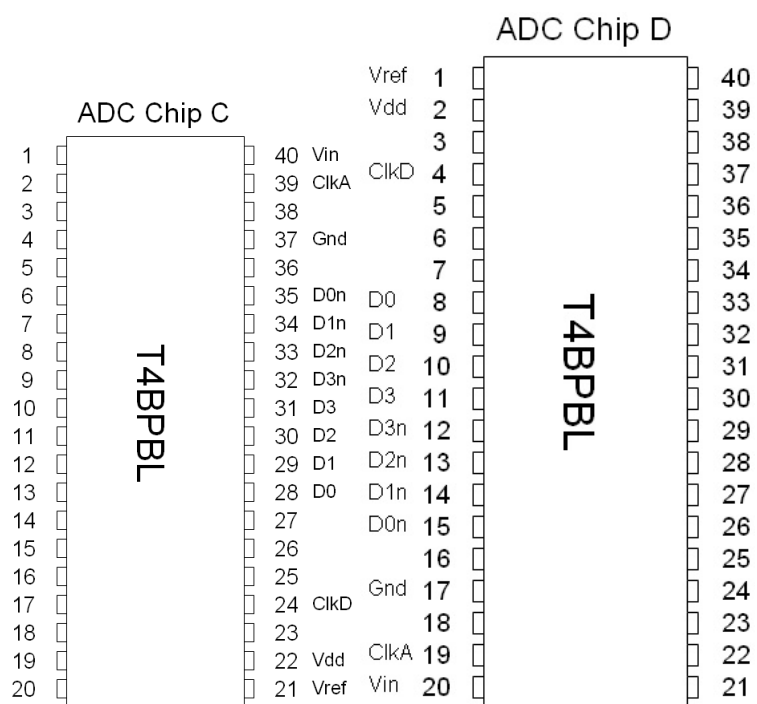


Figure 5.2: Pin-outs of ADC-C and ADC-D

100kHz. An Agilent 33250A is used to make the input signal and a Tektronix TD220 oscilloscope is capturing the output.

5.2 Measured Results

5.2.1 DC Transfer Function

Since this is a novel architecture, it is very important first and foremost to assure that the device operates the way that is supposed to, namely that the transfer function is compressing. The test was done using the first chip and with the chip properly biased. $V_{in} = 0 - 5V@10Hz$ sweep, $Clk = 0 - 5V@100kHz$ square wave, $V_{ref} = 1000mV$ and $V_{DD} = 5V$. The clock was set at a much higher rate than the input signal so the signal would be approximately DC. The full repeating DC ramp is shown in Figure 5.3 and a zoomed view of just a single ramp is shown in Figure 5.4.

These confirm that the chip was working. The circuit was also tested at $V_{ref} = 450mV$ and the results are shown in Figure 5.5

Chip B was also tested and it seems that the chip is too noisy and some bits are being lost to glitches. A similar test was done as before, but with $V_{ref} = 3.6V$ and the results as in Figure 5.6. In addition, the unlatched outputs were measured and are in Figure 5.7. With reduced noise and proper biasing this chip should work.

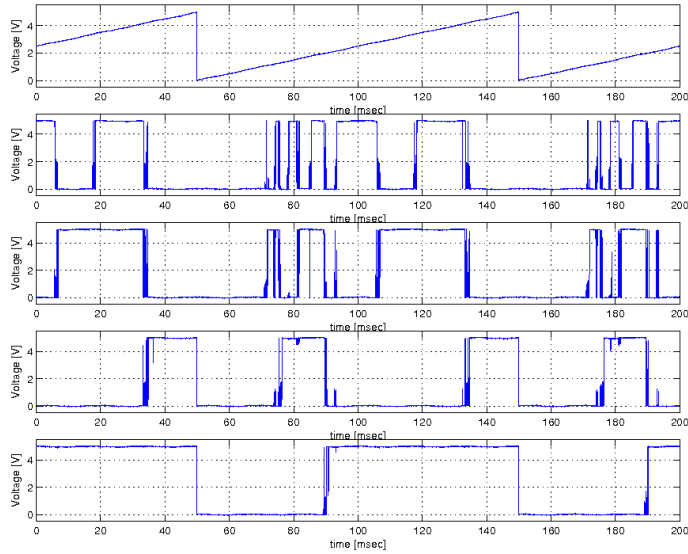


Figure 5.3: DC Sweep of Chip A, $V_{ref} = 1V$

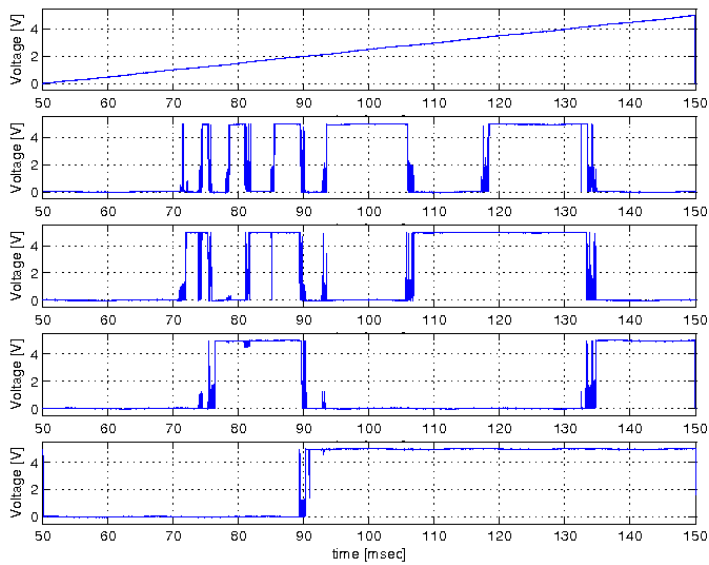


Figure 5.4: DC Sweep of Chip A, $V_{ref} = 1V$, zoomed

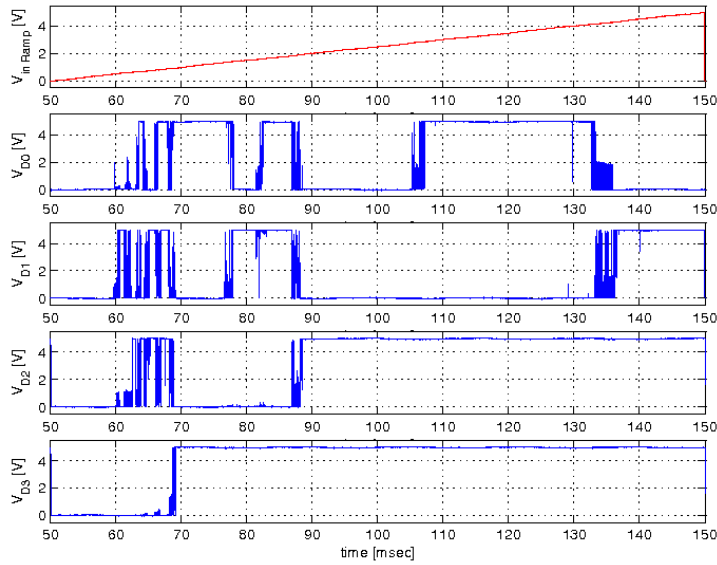


Figure 5.5: DC Sweep of Chip A, $V_{ref} = 450mV$

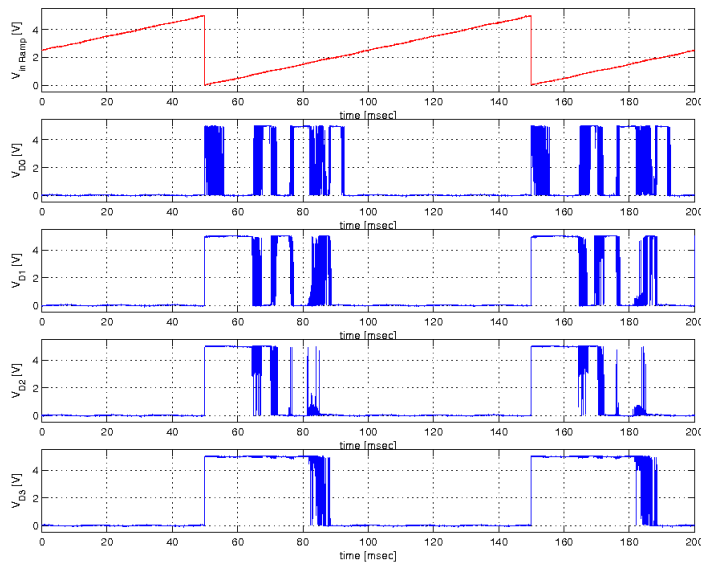


Figure 5.6: DC Sweep of Chip B, $V_{ref} = 3.6V$, Latched outputs

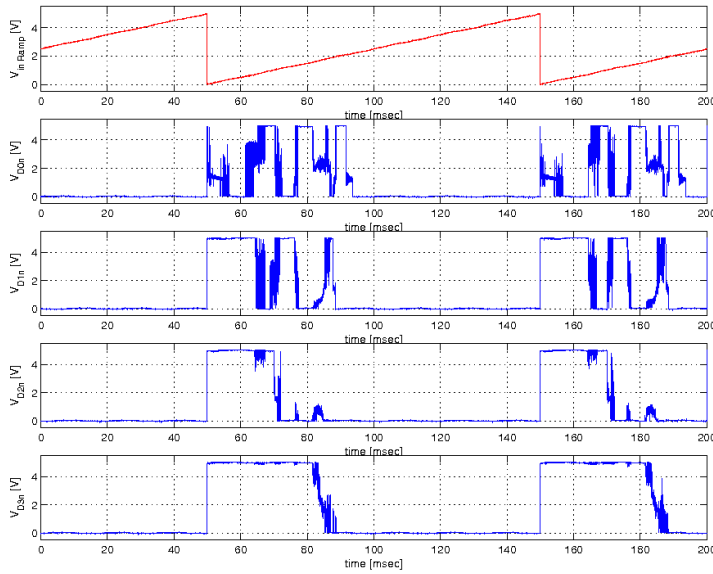


Figure 5.7: DC Sweep of Chip B, $V_{ref} = 3.6V$, Unlatched outputs

Glitches in Transfer Function

As stated earlier, there were issues with the output glitching and these are readily seen in the previous results. Figure 5.8 shows a close-up of the 1011 \rightarrow 1100 transition. This transition shown is one of the upper bits, was worse than the lower bits. Figure 5.4 shows that the glitches are worse on the upper bits. The figure here supports the conclusion that this is caused by metastable region. When the comparator enters the metastable region all the inputs of the encoder which are reading that comparator also become metastable. It is not until the comparator enters a stable region that the circuit settles into a stable operating position.

There are clearly ripples showing up on the output. These match the clock, which leads to the conclusion that the flip-flops are forced to a stable point by the

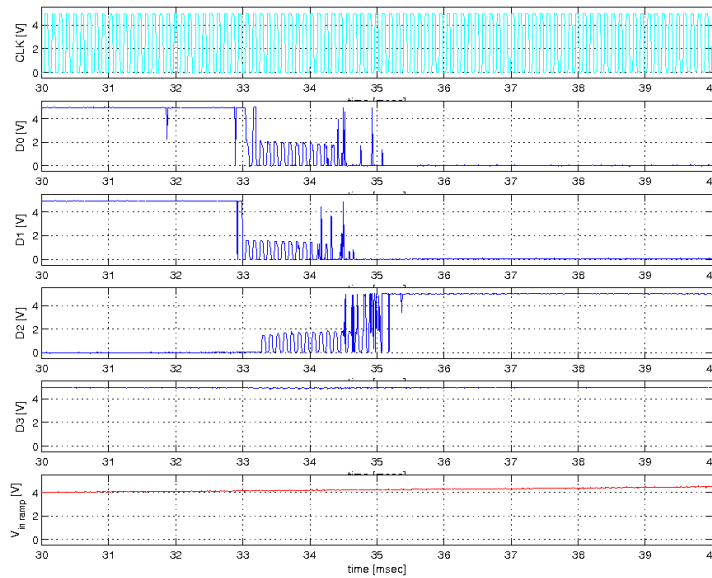


Figure 5.8: 1011 to 1100 Transition with Clock

clock, but when the flip-flop is in read mode it floats to the middle. D_2 at $t = 35\text{m}$ it is particularly revealing can be seen that the output goes high before going back to the metastable point. At this point the comparator is beginning to go past the threshold. D_0 and D_1 start latching hard to zero and much of their glitching goes away. This is supported by the results from Chip B, where the nature of the glitches changes between the latched and unlatched outputs. If Figures 5.6 and 5.7 are analyzed, the unlatched glitches stay around $\frac{V_{dd}}{2}$, while the latched glitches go to V_{dd} or Gnd .

To confirm that the glitches were the result of metastable outputs, the voltage supply was adjusted to change the gains of the circuit. Initially, it was thought that by increasing the supply voltage the current through the preamplifiers in the comparators the glitching would be reduced. The glitching actually become worse,

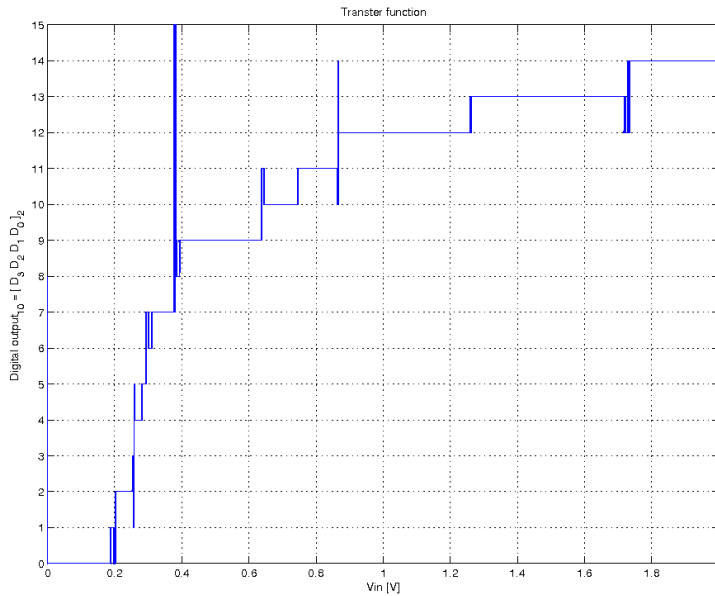


Figure 5.9: Transfer Function at $V_{dd} = 2V$

and reducing the voltage reduced the glitching. This is thought to be since the dominant gain elements are actually the digital components. The gain of a CMOS inverter can be crudely underestimated as $\frac{V_{dd}}{V_{dd} - V_{thn} - V_{thp}}$. As V_{dd} decreases the gain increases since the the threshold voltages remain the same. All output bits go through at least 4 CMOS gates. This gain increase can continue until the V_{dd} is equal to the sum of the threshold voltages. Figure 5.9 shows the transfer function with a 2V supply voltage. Notice glitching is gone, but there are offsets. The large spike is presumed to be a certain gate which stopped working at such a low voltage because the the thresholds were higher. Figures 5.10, 5.11, 5.12, and 5.13 show the glitching reduce for supply voltages of 2, 3, 4, and 5V, respectively.

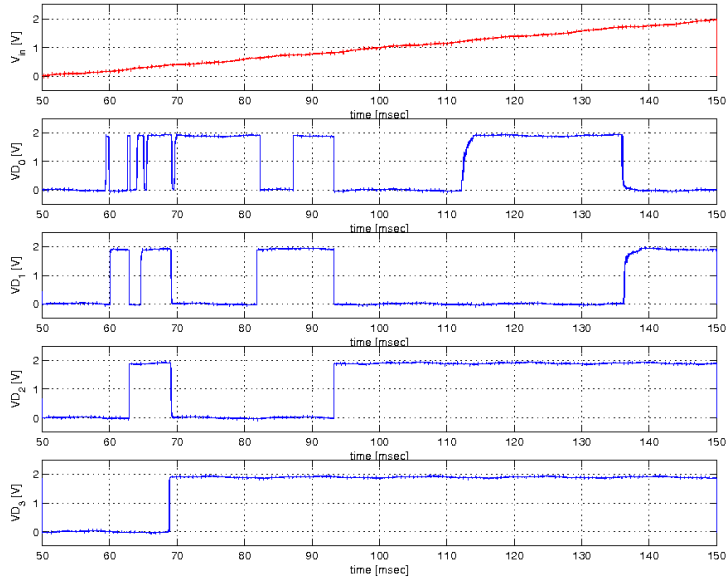


Figure 5.10: Bitwise Output at $V_{dd} = 2V$

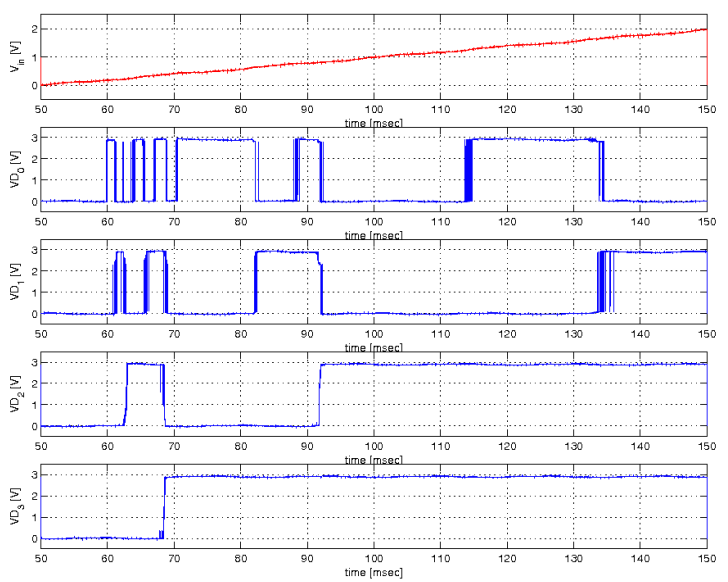


Figure 5.11: Bitwise Output at $V_{dd} = 3V$

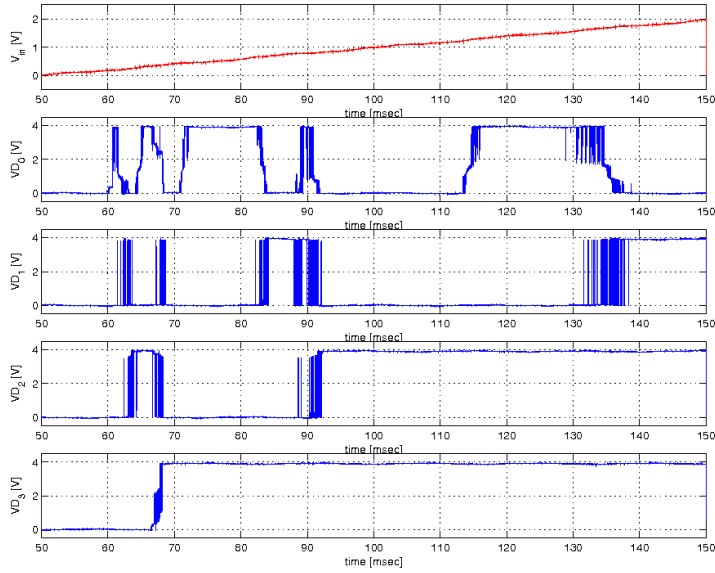


Figure 5.12: Bitwise Output at $V_{dd} = 4V$

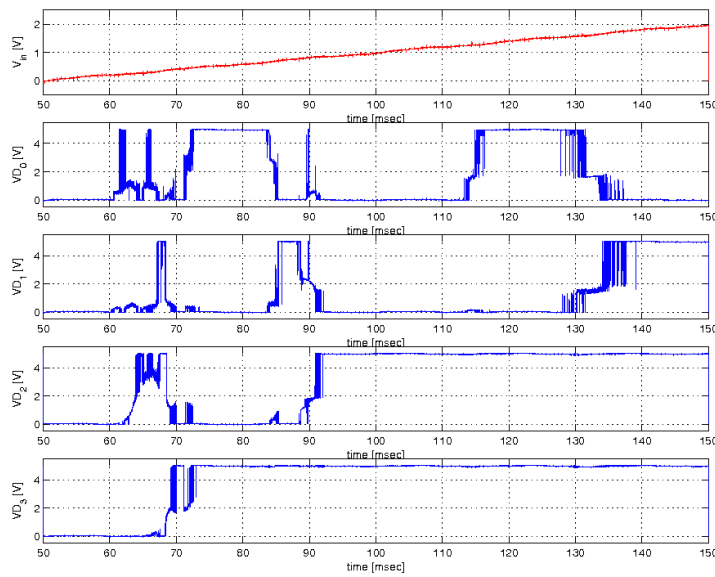


Figure 5.13: Bitwise Output at $V_{dd} = 5V$

5.2.2 Power Consumption

Power consumption is important characteristic to consider, both static and dynamic power consumption. To find the static power, the power out of the power supply was measured with no input signal, and with a 10MHz signal to find dynamic power. The static consumption was 41.7mW and the dynamic power was 49.5mW. The analog frontend is drawing the most power and should be the focus of future optimization.

5.2.3 Propagation Delay

The test equipment available limited the transient tests that were able to be run. The chips functioned properly at the maximum speed that the test setup could operate, which was a clock signal of 100kHz.

Chapter 6

Architectural Analysis and Improvements

No new design is perfect, and this design was no exception. There were two fundamental issues uncovered through the analytical work as well as in testing. The main issue relates to division of bits through a reference ladder. The second issue is signal-dependent delays found through the various components. A brief summary of each of the issues follows with potential solutions and that is followed by a section of other optimizations that could be made.

6.1 Division of Input Signal

The basic concept of the architecture is the division of the input signal. The input signal is divided and compared against a fixed reference voltage leading to

the compressing transfer function. This division of the input signal caused the glitches, which were not discovered until the chip was tested. The glitching was a manifestation of primarily the β -multiplied metastable region¹. This increased metastable region was made more noticeable by the β -multiplied noise on the reference ladder and the reference voltage. This was clearly the case since the noise on the reference source was reduced by using a low-pass filter. The glitching is also much larger on the upper bits than on the lower bits.

Several methods are being proposed to minimize the effects of the β -multiplication, as previously mentioned. Hysteresis could be implemented in the comparators to cover the entire metastable region. This seems to be the most reasonable solution. In addition, the gain of the upper bit comparators can be increased. This usually requires a reduction in speed, but it could be compensated with an increase in power. The extra gain could also be achieved through trading delay for gain through the use of additional latches. This would keep the bandwidth up, despite the increase in delay.

Upon noticing the β -multiplication of other effects, the offset mismatch was analyzed and found to be β -multiplied as well. This effect is less worrisome than the previous two issues. The offset can be reduced through many autozeroing techniques which would make the effect negligible. This seems to be a plausible option, especially if the device takes on a much more pipelined architecture such as through introduction of additional latches. Offset mainly effects the linearity of the device, or to phrase more broadly, the matching of the physically device

¹Where β you'll recall is $\frac{2^N}{2^N - n}$, which increases with each bit.

transfer function with the theoretical device transfer function. The offset gets worse on the upper bits, but the linearity is also less important, since the focus on accuracy is on the lower bits. In those bits, the β -multiplication of the offset remains near unity.

One of the benefits of the division is reduction of the effect of reference ladder error in the least significant bits. Again working from the argument of high accuracy in the linear region, this is highly beneficial. Matching between resistive elements is generally rather poor, and this increases the accuracy over a Flash architecture. The division also benefits the capacitive ladder, which has better matching to begin with, but suffers from the non-linearity issues.

All of these problems are caused by the use of division on the input signal. These effects may be mitigated by the use of a multiplication model, where the smallest bits are multiplied by the largest gain². This approach could lead to a hybrid model where some bits are multiplied and some divided to balance the issues created by both. In addition, a design where each bit is divided individually could also be investigated.

6.2 Signal-Dependent Transient Characteristics

The primary reason these designs began to be investigated was the thought that if the input signal were modulated against a single reference voltage the comparators could be better optimized. Many designs were investigated, but this design

²These ideas are completely untested and merely offered to the reader as a tool to expand their thinking on these architectures.

was continued due to the novel compressing effect. The comparators could be designed to operate at a single input voltage that would allow the bias conditions to be pushed. While this is true, the task of modulating the input signal has proven to be more detrimental than the compensation the optimized comparators provide. The reference ladder sets up an RC delay line that is different for each bit and increases in delay with each bit. This causes large signal-dependent transient variations.

In addition to the RC delay line of the reference ladder, there can be a g_m induced delay. If the gates of the differential input transistors are overdriven less, g_m will be lower on the comparator. The g_m dependence on input voltage gets worse as the devices become smaller, as devices scale and transconductance lowers. This lower transconductance results in lower speeds on the upper bits since they are less likely to be heavily overdriven. This can be overcome by switching to a preamplifier design which has a signal-independent g_m , such as BJTs or subthreshold MOS.

As different parts of the signal propagate with different path delays through the analog section, the encoder inputs change many different times. This prevents the error correction from working at maximum efficiency. One solution to this effect would be the use of latching comparators. Latches are not only a timing mechanism, but they are gain elements which reduce metastability. The design could also be pipelined to reduce the overall design of the circuit.

A way to reduce the effects is to use small reference elements, i.e. really small resistors. This makes the reference ladder faster than the other components,

which have lower signal-dependent delays. This approach increases the demands of input buffer, but it may be done with a different process.

6.3 Other Optimizations

As was discussed in the previous section, there are issues with g_m being voltage related causing signal-dependent delays. This could be eliminated by switching to subthreshold comparators, since they have a constant transconductance. Subthreshold design can be a challenging paradigm to design in since the bias conditions must remain carefully controlled to ensure the device remains in subthreshold. This design, by having a constant input range in the comparators, would simplify the design of subthreshold comparators.

If the subthreshold comparators are combined with a low-power encoder topology, the overall power consumption could be drastically reduced. This combined with the ability to eliminate the power consumption of the reference ladder, would make an overall low power design.

Bipolar design also has the constant g_m , so it is also better suited for the design. In addition, SiGe bipolar transistors are very fast, so it has the potential to dramatically increase the operating speed of the circuit[34]. These advantages of bipolar design are well understood, but the typical bipolar process is an RF process. RF processes, including many CMOS processes, have high accuracy, low-parasitic resistors and capacitors. The MIM capacitor of the process cited has very low parasitics, which would eliminate the “linearity” problems of the capaci-

tor ladders in the process used here. There are also very low parasitic capacitance resistors.

One possible power saving solution proposed is the use of multiple power supplies for the digital and analog sections, and the reference ladder. The reference ladder needs a voltage at least equal to the dynamic range. A large voltage on the reference ladder, would allow for a large dynamic range and number of bits. A low voltage on the comparators and digital components would reduce the total power consumption dramatically since the reference ladder is such a small part of the system. This architecture allows a low voltage on the comparators, since there is a single input voltage. A comparator input range is typically a bias voltage plus the input range, so this design can be limited to ranges imposed by the bias circuits, such as a current mirror and active load in a differential pair.

The reference voltage was observed to be noisy input source in this circuit. In addition, the capacitor seemed to destroy the chip, probably through discharging the capacitor onto the chip. An improvement on a future design will be larger ESD protection on this pin and integrated low-pass filter. This will dramatically reduce the reference noise.

6.4 Applications

A circuit without an application is merely an academic exercise. Two applications have been focused on. High-speed power signals, such as radar and sonar, and integrated sensors requiring a large dynamic range. These two applications will

be described here, as well as potential changes in the design that would be made in each application.

The first class of applications is high-speed power signals, focusing mainly on radar. These applications require high bandwidth, high resolution ADCs. Many radar signals first go through logarithmic amplifiers, which compress the power signal and then the ADC. This design integrates the compressing and conversion into one step offering a simplified design and potentially higher speeds. Commercial logarithmic amplifiers above 1GHz are very difficult to implement, so an architecture which can easily reach past that would be desirable[35]. These speed goals can be reached through the use of advanced processes, such as deep submicron CMOS or BiCMOS. Power becomes less of a concern for these applications.

A very interesting application would be for low-power integrated sensors. An example would be a remote ground sensor. It needs a large dynamic range to detect small things and vehicles, but the accuracy is important on the small-signal. This would allow the sensor to resolve the distance a person is from the sensor, but still allow it to detect a truck. The goal of these designs is minimum power-consumption, but to retain wide bandwidth signal capturing. Latched comparators and advanced power management techniques should be used. The sensor should turn on, capture the signal, then turn off. Submicron CMOS should be used to minimize the power consumption.

Companding is another application that has already been discussed in section 2.2. The expander transfer function is Equation 6.1. A digital-to-analog converter, which can approximate that transfer function is shown in Figure 6.1.

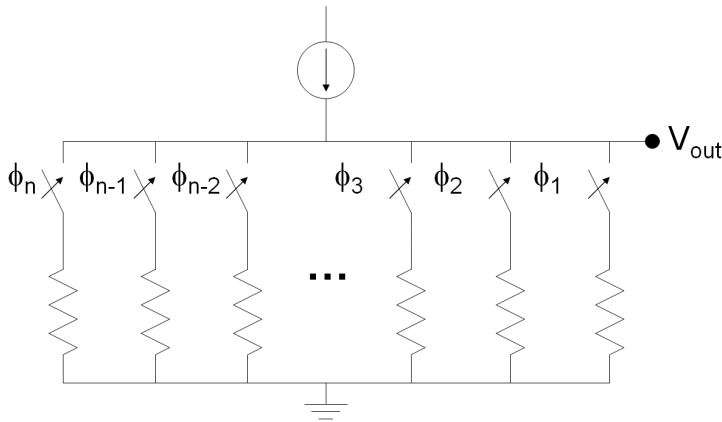


Figure 6.1: Schematic of the Inverse DAC

$$F^{-1} = \frac{V_{ref}}{1 - \frac{n}{2^N}} = \frac{2^N V_{ref}}{2^N - n} \quad (6.1)$$

When a switch turns “on” that resistance adds in parallel to the total resistance. Since all resistors are equal, this means the total resistance is that of a single resistor divided by the number “on” in parallel. When these are biased by the current source the voltage output can be found as in Equation 6.2. If n is changed to use inverse logic, and $IR = 2^N V_{ref}$, this equations matches that of the inverse function as in Equation 6.3. This design is proposed to show that this division technique has multiple uses³.

$$V_{out} = I \cdot R_{total} = I \cdot \frac{R}{n} \quad (6.2)$$

³This again is an untested idea.

$$V_{out} = \frac{I \cdot R}{2^N - n} = \frac{2^N V_{ref}}{2^N - n} \quad (6.3)$$

Chapter 7

Conclusion

A 4-bit compressing analog-to-digital converter architecture has been presented. The architecture is based on Flash ADCs with some modifications to the input signals. The architecture has been analyzed from a theoretical point of view. The circuit components have been described and analyzed. Physical chips were manufactured by MOSIS and have been tested. The architecture is well understood with the figures of interest being developed both theoretically and in actual measurement.

The architecture has a very large dynamic range, $2^{2N} - 1$, compared with a linear device, $2^N - 1$. The signal to noise ratio was found to be lower than a linear device, but the SNR is higher for small input signals compared to a linear device with the same dynamic range. A simple analytical solution was found for the quantization noise. The optimal signal density was found and the quantization noise was compared for a linear and compressing device with that signal.

The architecture also demonstrated the ability to generate arbitrary functions by changing the reference ladder. The natural transfer function is $1 - 1/x$ and $\log(x)$ is possible with only slight modifications.

The basic characteristics were found both in simulation and the physical device. The circuit is high bandwidth, with a sampling frequency of 80MHz, based on simulation, on a $0.5\mu m$ digital CMOS process. The speed tests have been limited by the equipment available. The static power consumption was found to be about 41.7mW and dynamic 49.5mW, which closely matched the simulated power 46mW static and 76mW dynamic. The 4-bit transfer function was indeed found to be compressing and the dependence of the transfer function on the reference voltage was confirmed. The final active die area was $0.18mm^2$, which is small for a converter with this dynamic range.

This was the first implementation of the new architecture. Four different physical chips were manufactured based on this architecture. The output signal was found to contain glitches, however these were examined in the circuit analysis and solutions have been presented. Many other architectural enhancements have been suggested and work continues to improve the design. Future plans include scaling the design into deep submicron CMOS and then conversion to BiCMOS. A search of the literature by the author concludes, that this is the highest bandwidth compressing converter.

Appendix A

Derivation of V_{noise}

$$\begin{aligned}
P_{Q_e} &= \int_{-\infty}^{\infty} \rho \cdot (Q_e)^2 dQ_e \\
P_{Q_e} &= \int_{-\frac{1}{2}V_{bN}}^{\frac{1}{2}V_{bN-1}} \rho \cdot (Q_e)^2 dQ_e + \int_{-\frac{1}{2}V_{bN-1}}^{\frac{1}{2}V_{bN-2}} \rho \cdot (Q_e)^2 dQ_e + \dots + \int_{-\frac{1}{2}V_{b1}}^{\frac{1}{2}V_{b1}} \rho \cdot (Q_e)^2 dQ_e + \dots \\
&\quad + \int_{\frac{1}{2}V_{bN-2}}^{\frac{1}{2}V_{bN-1}} \rho \cdot (Q_e)^2 dQ_e + \int_{\frac{1}{2}V_{bN-1}}^{\frac{1}{2}V_{bN}} \rho \cdot (Q_e)^2 dQ_e \\
P_{Q_e} &= \rho \cdot \frac{(Q_e)^3}{3} \Big|_{-\frac{1}{2}V_{bN}}^{\frac{1}{2}V_{bN-1}} + \rho \cdot \frac{(Q_e)^3}{3} \Big|_{-\frac{1}{2}V_{bN-1}}^{\frac{1}{2}V_{bN-2}} + \dots + \rho \cdot \frac{(Q_e)^3}{3} \Big|_{-\frac{1}{2}V_{b1}}^{\frac{1}{2}V_{b1}} + \dots + \rho \cdot \frac{(Q_e)^3}{3} \Big|_{\frac{1}{2}V_{bN-2}}^{\frac{1}{2}V_{bN-1}} + \rho \cdot \frac{(Q_e)^3}{3} \Big|_{\frac{1}{2}V_{bN-1}}^{\frac{1}{2}V_{bN}} \\
P_{Q_e} &= 2\rho \cdot \frac{(Q_e)^3}{3} \Big|_0^{\frac{1}{2}V_{b1}} + \dots + 2\rho \cdot \frac{(Q_e)^3}{3} \Big|_{\frac{1}{2}V_{bN-2}}^{\frac{1}{2}V_{bN-1}} + 2\rho \cdot \frac{(Q_e)^3}{3} \Big|_{\frac{1}{2}V_{bN-1}}^{\frac{1}{2}V_{bN}} \\
P_{Q_e} &= 2 \cdot \frac{(Q_e)^3}{3} \Big|_0^{\frac{1}{2}V_{b1}} \cdot \frac{1}{\sum V_{bn}} \cdot N + \dots + 2 \cdot \frac{(Q_e)^3}{3} \Big|_{\frac{1}{2}V_{bN-2}}^{\frac{1}{2}V_{bN-1}} \cdot \frac{1}{\sum V_{bn}} \cdot 2 + 2 \cdot \frac{(Q_e)^3}{3} \Big|_{\frac{1}{2}V_{bN-1}}^{\frac{1}{2}V_{bN}} \cdot \frac{1}{\sum V_{bn}} \cdot 1 \\
P_{Q_e} &= \frac{2}{3} \cdot \frac{1}{\sum V_{bn}} \cdot \left[N \cdot (Q_e)^3 \Big|_0^{\frac{1}{2}V_{b1}} + \dots + 2 \cdot (Q_e)^3 \Big|_{\frac{1}{2}V_{bN-2}}^{\frac{1}{2}V_{bN-1}} + 1 \cdot (Q_e)^3 \Big|_{\frac{1}{2}V_{bN-1}}^{\frac{1}{2}V_{bN}} \right] \\
P_{Q_e} &= \frac{2}{3} \cdot \frac{1}{\sum V_{bn}} \cdot \left\{ N \cdot \left[\left(\frac{V_{b1}}{2} \right)^3 - \left(\frac{0}{2} \right)^3 \right] + \dots + 2 \cdot \left[\left(\frac{V_{bN-1}}{2} \right)^3 - \left(\frac{V_{bN-2}}{2} \right)^3 \right] + 1 \cdot \left[\left(\frac{V_{bN-1}}{2} \right)^3 - \left(\frac{V_{bN-2}}{2} \right)^3 \right] \right\} \\
P_{Q_e} &= \frac{2}{8 \cdot 3} \cdot \frac{1}{\sum V_{bn}} \cdot \left\{ N \cdot [V_{b1}^3] + \dots + 2 \cdot [V_{bN-1}^3 - V_{bN-2}^3] + 1 \cdot [V_{bN-1}^3 - V_{bN-2}^3] \right\} \\
P_{Q_e} &= \frac{1}{12} \cdot \frac{1}{\sum V_{bn}} \cdot \sum_{n=1}^N V_{bn}^3
\end{aligned}$$

Figure A.1: Derivation of V_{noise}

Bibliography

- [1] Y. Tsvividis, "Externally Linear, Time-Invariant Systems and Their Application to Companding Signal Processors," *IEEE Trans. on Circuits and Systems-II. Analog and Digital Signal Processing*, vol. 44, pp. 65-85, Feb. 1997.
- [2] A. Gersho, "Principles of Quantization" *IEEE Trans. Circuits and Systems*, vol. CAS-25, no. 7, pp. 427-436, July 1978.
- [3] Lampinen, H. and O. Vainio, "A New Dual-Mode Data Compressing A/D Converter Circuits and Systems," in *Proc. ISCAS*, 1997, pp. 429-432.
- [4] J.N. Lygouras, "Nonlinear ADC with Digitally Selectable Quantizing Characteristic", *IEEE Trans. Nuclear Science*, vol. 35, iss. 5, pp. 1088-1091, Oct. 1988.
- [5] Harrison, D.C., "A quadratic A/D Converter", *IEEE Trans. Nuclear Science*, pp. 396-398, 1980.

- [6] B.A. Hafeth and M.A.H. Abdul-Karim, "Flexible Non-Linear Analogue-to-Digital Converter," *Int. Journal of Electronics*, vol. 58, pp. 111-115, 1985.
- [7] K.M. Mahmoud and R.F. Wolffenbuttel, "A Nonlinear A/D Converter for Smart Silicon Sensors," in *Proc ISCAS*, 1992, pp. 605-608.
- [8] "MOSIS Wafer Acceptance Tests", 30 Mar. 2005 <http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t4bp-params.txt>.
- [9] "MOSIS Scalable CMOS Rules", 30 Mar. 2005, <http://www.mosis.org/Technical/Designrules/scmos/scmos-main.html>.
- [10] A. Tangel and K. Choi, "The CMOS Inverter as a comparator in ADC designs," in *Proc. ICEEE*, 2001, pp. 1-5.
- [11] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. 3rd ed., New York: Wiley-IEEE Press, 1998, pp. 685-699.
- [12] A. Hastings, *The Art of Analog Layout*. New Jersey: Prentice Hall, 2001, pp. 426-430
- [13] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. 3rd ed., New York: Wiley-IEEE Press, 1998, pp. 594-595.
- [14] K.C. Lauritzen, T. Onufert, S. Kim, F.K. Perkins, and M.C. Peckerar, Unpublished

- [15] Y. Akazawa, A. Iwata, T. Wakimoto, T. Kamato, H. Nakamura, and H. Ikawa, "A 400MSPS 8b Flash AD Conversion LSI" in *Proc. ISSCC*, 1987, pp. 98-99, 356.
- [16] M.M. Mano, *Digital Design*, 3rd ed., Prentice Hall, 3rd ed., 2002, pp. 21-22.
- [17] S. Padoan, A. Boni, C. Morandi, and F. Venturi, "A Novel Coding Schemes for the ROM of Parallel ADCs, Featuring Reduced Conversion Noise in the Case of Single Bubbles in the Thermometer Code," in *IEEE ICECS*, 1998, pp. 271-274.
- [18] C.W. Mangelsdorf, "A 400-MHz Input Flash Converter with Error Correction," *IEEE J. Solid State Circuits*, vol. 25, no.1, pp. 184-191, Feb. 1990.
- [19] C.L. Portmann and T.H.Y. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1132-1140, Aug. 1996.
- [20] C.L. Portmann and T.H.Y. Meng, "Metastability in CMOS Library in Reduced Supply and Technology Scaled Applications," *IEEE J. Solid-State Circuits*, vol. 30, no. 1, pp. 39-46 Jan. 1995.
- [21] P. Xiao, K. Jenkins, M. Soyuer, H. Ainspan, J. Burghartz, H. Shin, M. Dolan, and D. Hareme, "A 4b 8GSample/s A/D Converter in SiGe Bipolar Technology" in *Proc. ISSCC*, 1997, pp. 124-125.
- [22] C.S. Wallace, "A suggestion for a fast multiplier," *IEEE Trans. on Electronic Computers*, pp. 14-17, Feb. 1964.

- [23] F. Kaess, R. Kanan, B. Hochetand M. Declercq, "New Encoding Scheme For High-Speed Flash ADC's" in *Proc. ISCAS*, 1997, pp. 5-8.
- [24] R. Kanan, F. Kaess, and M. Declercq, "A 640mW High Accuracy 8-bit 1GHz Flash ADC Encoder," in *Proc. ISCAS*, 1999, pp. II-420-423.
- [25] G. Yu-hua, W. Zhao-gang, R. Jun-yan, and L. Lian, "Error-Suppressing Encoding Structure of Competition in Flash A/D Converter," in *Proc. Int. Conf. ASIC*, 2001, pp. 296-298.
- [26] D. Lee, J. Yoo, K. Choi, and J. Ghaznavi, "Fat Tree Encoder Design for Ultra-High Speed Flash A/D Converters," in *MWSCAS*, 2002, pp. II-87-II-90.
- [27] M.M. Mano, *Digital Design*, 3rd ed., Prentice Hall, 3rd Ed., 2002, pp. 270-276.
- [28] P. Pereira and J.R. Fernandes, "Dynamic Performance of Parallel-Type ADCs with Different Encoders," *DCIS'01*, Nov. 2001.
- [29] P. Pereira and J.R. Fernandes, "Comparative Study of Encoders for Parallel-Type ADCs," in *Proc. Int. Workshop on ADC Modelling and Testing*, pp. 142-146, Sep. 2001.
- [30] P. Pereira, J.R. Fernandes, and M.M. Silva, "Wallace Tree Encoding in Folding and Interpolation ADCs," in *Proc. ISCAS*, 2002, pp. I-509-512.

- [31] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. 3rd ed., New York: Wiley-IEEE Press, 1998, pp. 216-221.
- [32] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. 3rd ed., New York: Wiley-IEEE Press, 1998, pp.783-788.
- [33] C. Enz and G.C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," in Proc. , 1996, pp. 1584-1614.
- [34] J.S. Dunn, et. al. "Foundation of RF CMOS and SiGe BiCMOS Technologies" *IBM J. Research and Development*, vol. 47, no. 2/3, pp. 101-138, March/May 2003.
- [35] Dave Shaver, Personal communication on November 12, 2004.
- [36] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. 3rd ed., New York: Wiley-IEEE Press, 1998, pp.719-724.
- [37] S.K. Tewksbury, F.C. Meyer, D.C. Rollenhagen, H.K. Schoenwetter, and T.S. Souders, "Terminology Related to the Performance of S/H, A/D, and D/A Circuits," *IEEE Trans. on Circuits and Systems*, vol. CAS-25, pp. 419-426, July 1978.
- [38] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. 3rd ed., New York: Wiley-IEEE Press, 1998, pp. 772-788.

- [39] R. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*. 2nd ed., Boston: Kluwer Academic Publishers, 2003, pp.7-21.
- [40] W.R. Bennett, "Spectra of quantized signals" *Bell System Technical Journal*, vol. 27, pp. 446-472, July 1948.
- [41] Matt Franklin, Personal Communication, February 22, 2005.
- [42] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. 3rd ed., New York: Wiley-IEEE Press, 1998, pp. 832-837.
- [43] Y.P. Tsividis, V. Gopinathan, and L. Toth, "Companing in Signal Processing," *Electronics Letters*, vol. 26, pp. 1331-1332, Aug. 1990.
- [44] H. Nyquist, "Regeneration Theory," *Bell System Technical Journal*, p. 126, Jan. 1932.
- [45] F. Serra-Graells, L. Gomez, and J.L. Huertas, "A True-1-V 300- μ W CMOS-Subthreshold Log-Domain Hearing-Aid-On-Chip," *J. Solid-State Circuits*, vol. 39, no. 8, pp. 1271-1281, Aug. 2004.
- [46] T.F. Shubert Jr., "Simulation of the Effects of Compadding on Quantization Noise in Digital Communication Systems," *IEEE Trans. on Education*, vol. 37, pp. 47-50, Feb. 1994.
- [47] S. Laughlin, "A Simple Coding Procedure Enhances a Neuron's Information Capacity," *Notizen*, pp. 910-912, 1981.