ABSTRACT

Title of dissertation: CAPACITANCE-TO-DIGITAL CONVERTERS FOR HIGH-SPEED HIGH-RESOLUTION READOUT OF CAPACITIVE SENSORS

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This work focuses on the design of a capacitance-to-digital converter (CDC) for high-speed high-resolution readout of capacitive sensors. Most previously reported CDCs show a tradeoff in resolution and conversion speed; In this work a two-step successive approximation register (SAR) CDC is proposed to improve resolution and conversion speed over state-of-the-art. First, the coarse conversion stage performs a capacitive offset compensation down to within 10fF. The fine conversion stage converts the amplified residue voltage with a resolution of 200aF. These bits are communicated off chip on an I^2C bus. The effective number of bits (ENOB) is compared under different measurement conditions. The circuit achieves 9.8 ENOB with a 28 µs conversion time. When overclocked, the circuit achieves 8.2 ENOB with a 14 µs conversion time. This equates to an overall figure of merit (ENOB throughput) of 350 kbits/s and 585 kbits/s, respectively, which is among the highest values reported in the literature. The interface circuit design is described, simulated, and measured to characterize performance.

CAPACITANCE-TO-DIGITAL CONVERTERS FOR HIGH-SPEED HIGH-RESOLUTION READOUT OF CAPACITIVE SENSORS

By

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Dedication

To my wife, daughter, and parents.

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I would like to thank my advisor, Dr. Pamela Abshire, for guiding me and my work. I thank her for always pushing me to grow as a researcher and a person. A special thanks to Dr. Timothy Horiuchi for the insightful discussions on research projects and getting me to think about problems in a different way.

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List of Abbreviations

ADC	analog-to-digital converter
AHS	artificial hair sensor
CBCM	charge-based capacitance measurement
CDAC	capacitive digital-to-analog converter
CDC	capacitance-to-digital converter
CDT	capacitive displacement transducer
CMOS	complementary metal-oxide semiconductor
COTS	commercial-off-the-shelf
DAC	digital-to-analog converter
DNL	differential nonlinearity
ENOB	effective number of bits
FEM	finite element model
FPGA	field-programmable gate array
HDL	hardware description language
I^2C	inter-integrated circuit
IC	integrated circuit
IMU	inertial measurement unit
INL	integral nonlinearity
LSB	least significant bit
MEMS	microelectromechanical sensor
MIM	metal-insulator-metal
MOM	metal-oxide-metal
NMOS	n-type metal-oxide semiconductor

PCB	printed circuit board
PDMS	polydimethylsiloxane
PLL	phase-locked loop
PM	period modulation
PMOS	p-type metal-oxide semiconductor
PSPI	photosensitive polyimide
PSRR	power supply rejection ratio
RF	radio frequency
RMS	root mean square
RTL	register transfer level
SAR	successive approximation register
SCL	serial clock line
SDA	serial data line
SNR	signal-to-noise ratio
SQNR	signal-to-quantization-noise ratio
UAV	unmanned aerial vehicle

Chapter 1

Introduction

1.1 Motivation

The sensing of various physical properties such as acceleration, rotation, pressure, flow, proximity, and touch have been possible by exploiting capacitance variations. Capacitive sensing has gained popularity due to its high sensitivity to small changes and low temperature sensitivity, making it a suitable choice for various industries, including industrial and medical applications. Additionally, it tends to consume less power than other sensor transducer types, making it ideal for use in portable battery-operated devices. Consequently, the design of capacitive interface circuits for readout has been critical to fully make use of these advantages. A capacitance-to-digital converter (CDC) takes a capacitance variation from the capacitive sensor and converts it into a digital representation that can be read out. Typically, a CDC is comprised of both an interface circuit and an ADC, although in certain instances, these components may be indiscernible.

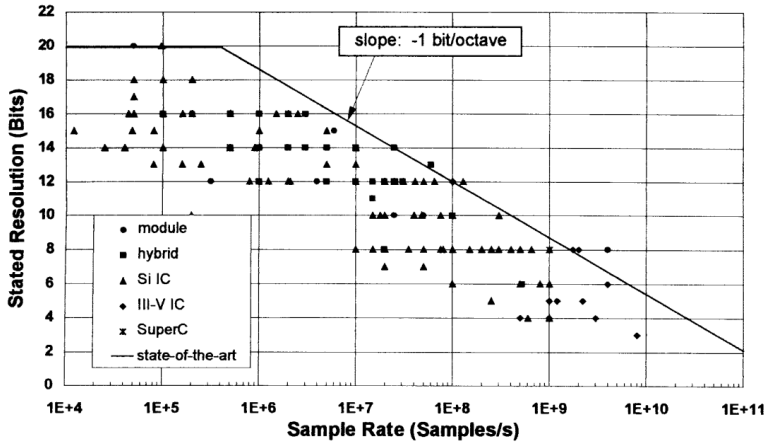


Figure 1.1. Survey of ADCs showing the trend of resolution decrease as sampling rate increases **[1]**. Copyright © 1999, IEEE

For ADCs, there have been thoroughly researched and established tradeoffs between resolution and sampling rate. Similarly, while many capacitive converters achieve attofarad resolutions, higher resolution tends to come at the cost of speed [2] [3] [4]. In emerging applications that aim at exploring high frequency effects in natural systems such as the resonant frequency of bat hairs and using distributed sensing to determine wing deformation in UAVs for fast attitude correction, both speed and resolution are critical. The goal of this work is to achieve high resolution while minimizing the conversion time for CDCs to support the strict requirements of these sensor systems.

1.2 Technical Contributions

The primary contributions of this work are as follows:

- **Design of two-step SAR capacitance-to-digital converter**

  The design of a two-step SAR CDC is presented. The relationship between the 16-bit digital output representation and the sensed capacitance is derived. Showed how a two-step architecture produces sub-femtofarad resolution. The use of non-uniform conversions is shown to improve speed capabilities. Explored noise and offset-limited achievable resolution.

- **Testing of two-step SAR capacitance-to-digital converter**

  The proposed design was fabricated and tested in a 0.5µm and 0.18µm technology. The DNL and INL figures were determined and effective resolution compared under different testing conditions. The design achieves 9.8 ENOB for 64µs/28µs conversion times (Near fastest reported conversion). When

overclocked, it achieves 8.2 ENOB for 32µs/14µs conversion times (Fastest reported conversion). This equates to a near highest ENOB throughput (FoM2) of 150/350 kbits/s (Nominal) and 256/585 kbits/s (Overclocked). The nonlinearity is explored with maximum average INL/DNL of 276 LSB/11.4 LSB.

- **Demonstrated sensor testing for higher input frequency sensors**

  Created a high frequency area changing capacitance sensor. The circuit was tested with high frequency sensors which is not reported by many published works considering their converter bandwidth capabilities. Demonstrated testing at 234Hz and 656Hz (Fastest reported testing speeds).

1.3 Thesis Organization

Chapter 2 provides background information on capacitance sensing and presents some examples. **Chapter 3** introduces capacitive interface circuits and discusses design considerations and potential sources of error. **Chapter 4** presents a novel design for capacitance-to-digital conversion. The relationship between sensed capacitance and the digital bits is derived. **Chapter 5** discusses measurement results and quantifies the performance of the proposed design. Finally, **Chapter 6** summarizes the work, compares it to the state-of-the-art, and suggests future improvements and applications.

Chapter 2

Capacitance Sensing

2.1 Introduction

By looking at the simplified model of a capacitor ($C=\varepsilon A/d$), we see that changes in capacitance can occur with a change in the permittivity ε, the overlap area A of the electrodes, or the distance d between electrodes. With these properties, capacitive sensors have been developed for various applications.

2.2 Permittivity Change

Variations in permittivity have been used in humidity sensors, chemical sensing, and biomedical applications (e.g. cell culture monitoring).

The concentration of a substance can be measured by monitoring the changes in permittivity. As higher concentrations of particles appear, the permittivity and, consequently, the capacitance changes. If the permittivity of the particle is greater than that of the medium, the capacitance increases. A simple example is depicted in Fig. 2.2.

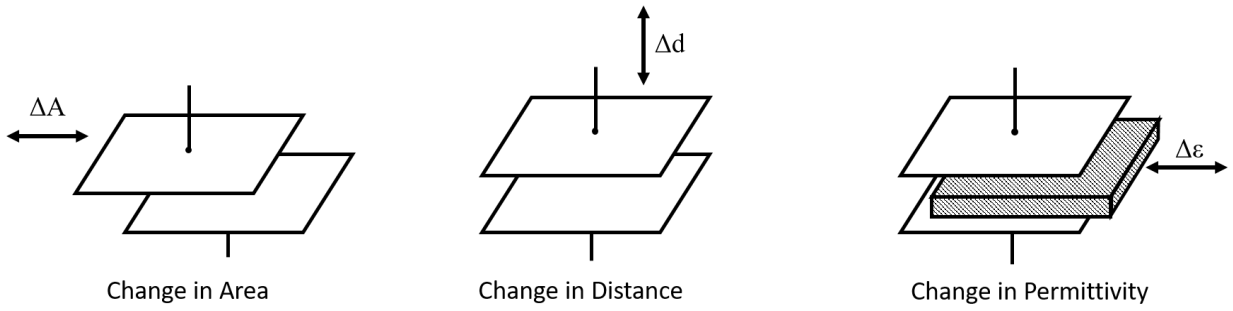
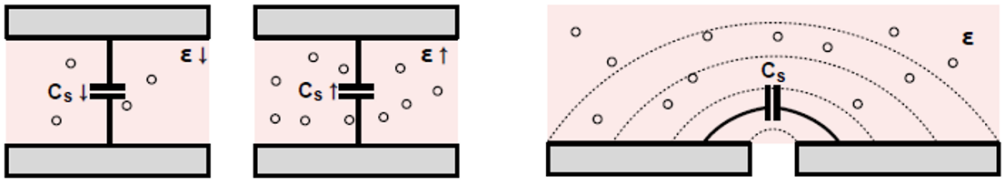


Figure 2.1. Capacitance variability types showing examples of change in area, distance, and permittivity.



(a) (b)

Figure 2.2. Concentration sensor examples showing particle concentration changing permittivity and consequently capacitance; (a) Vertical electrode configuration; (b) Horizontal electrode configuration. Source: **[5]**

Another example of using the dielectric property for sensing is cell culture monitoring in Lab-on-CMOS systems [6]. The dielectric properties at the interface are altered by adherent cells as they settle onto the surface, adhere, proliferate, and eventually detach due to various factors like cell death, forced detachment, or other morphological changes. The process of cell adhesion occurs in three stages. Initially, they descend and make initial contact with the surface. Then, they attach to the surface and finally flatten themselves until reaching stable adhesion [7]. Healthy cells remain firmly attached to the surface and spread out as they grow and proliferate, while compromised cells contract and may detach from the surface. The modifications in cell morphology influence the dielectric properties at the interface, which can be quantified by changes in surface capacitance.

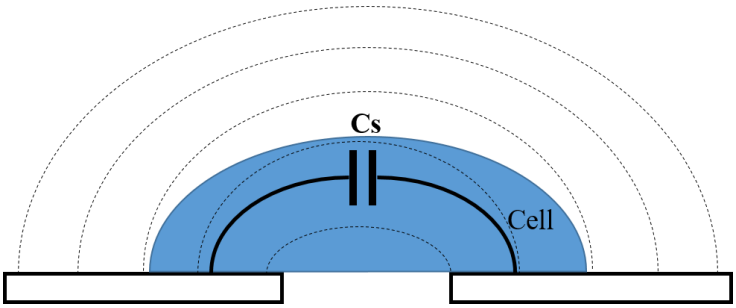


Figure 2.3. Cell culture monitoring example showing how an adhering cell contributes a change in permittivity between electrodes.

2.3 Area Change

Sensors that use a change in overlap area have been used to measure acceleration [8] [9] and displacement (linear and angular) [10] [11].

An example of a micro accelerometer using this principle is shown in Fig. 2.4. The spring-mass system is used to detect acceleration, where capacitive transducers are formed by movable electrodes on the proof mass and fixed electrodes on the top die. When the proof mass moves with respect to the frame and top die, a displacement in the electrode overlap occurs, which is then converted into capacitance variation. Finally, the interface circuit detects this variation.

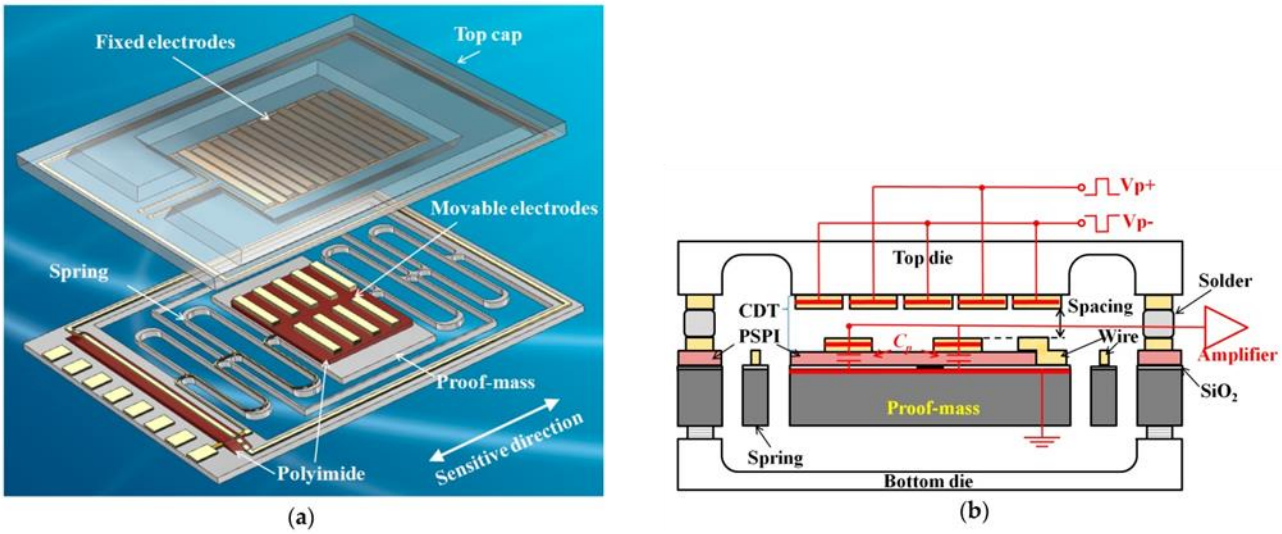


Figure 2.4. Schematic of the micro accelerometer using an encoder-like area-change transducer. (a) Structure of the capacitive accelerometer. The spring-mass system is also used as a micro position actuator for the calibration of the capacitive transducer; (b) Section view of the capacitive accelerometer, the electrodes on the top die and the proof-mass die form the capacitive displacement transducer (CDT); a photosensitive polyimide (PSPI) is inserted for reducing the parasitic capacitance. Source: **[8]**.

One of the earliest examples of the area changing capacitance principle is the rotary variable capacitor. Historically used in radio frequency (RF) tuning applications, the capacitor is formed by a fixed electrode and a moving electrode on a rotary axis. Maximum capacitance occurs when the electrodes are fully overlapped ($\theta = \pi$) and minimum when not overlapped at all ($\theta = 0$). In practice, a set of interlaced electrodes are used which scales the capacitance proportionally by 2N, where N is the number of moving electrodes.

$$C = \frac{\varepsilon \theta r^2}{2d} \tag{2. 1}$$

$$C_{int} = N \frac{\varepsilon \theta r^2}{d} \tag{2. 2}$$

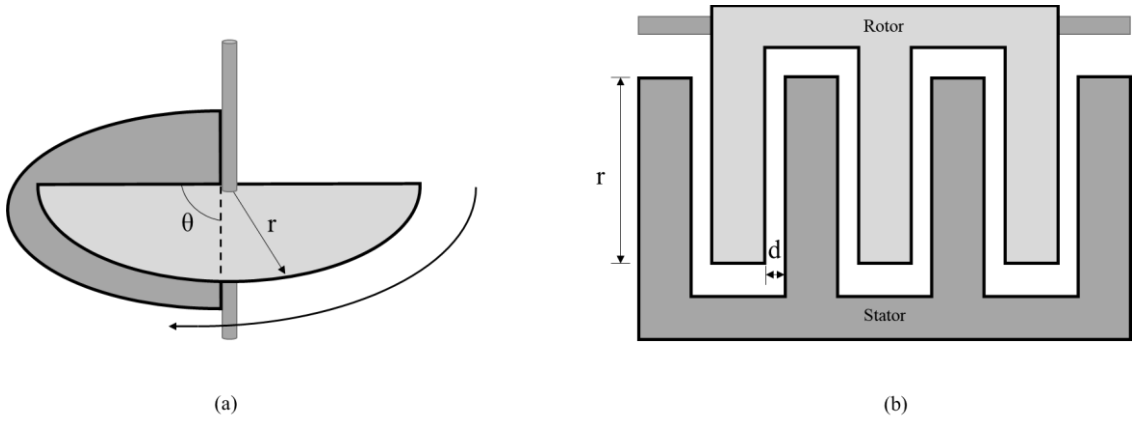


Figure 2.5. Rotary variable capacitor examples showing a rotating plate (rotor) passing over a stationary plate (stator) to create an area changing capacitor: (a) Single capacitor; (b) Interlaced multi-plate capacitor cross section.

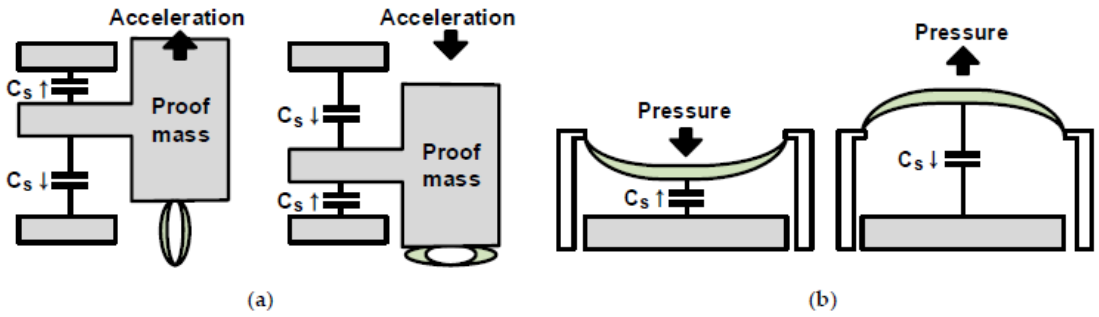


Figure 2.6. Distance-based capacitive sensor examples showing how a change in gap distance between electrodes influences the sensed capacitance: (a) accelerometer; (b) pressure sensor. Source: **[5]**

2.4 Distance Change

The most commonly used method of sensing capacitance is by looking at the variations in distance between electrodes. Sensing examples include acceleration, rotation, pressure, flow, proximity, touch, and strain.

Accelerometers and pressure sensors are commonly manufactured using a MEMS fabrication process. The micro machined accelerometer generally uses a spring-mass system where a proof mass moves in the event of sudden acceleration and the capacitance between electrodes changes due to the change in gap distance. The pressure sensor comprises a fixed electrode and a movable electrode in the form of a membrane, forming a capacitor. Physical forces, such as pressure or acceleration, alter the distance between the two electrodes. Examples of the principles are shown in Fig. 2.6.

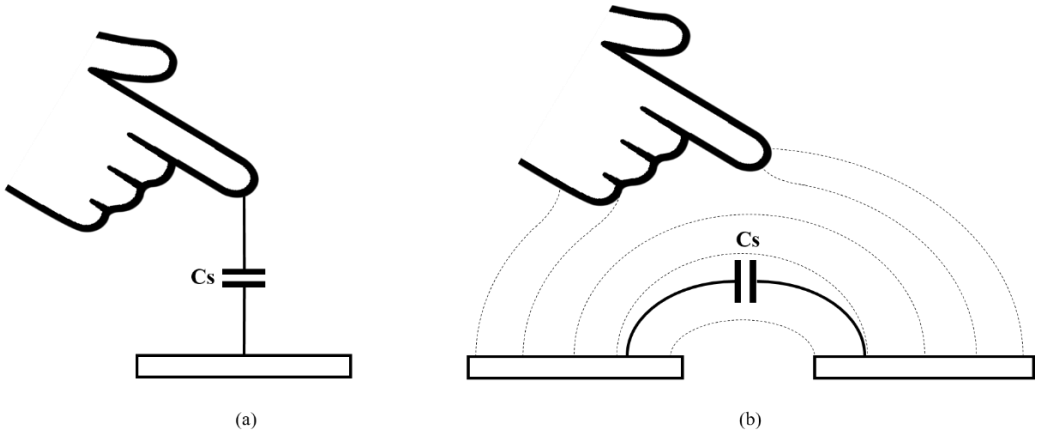


Figure 2.7. Capacitive touch sensor examples showing how an approaching finger interacts with the electrodes and influences the sensed capacitance: (a) self-capacitance; (b) mutual capacitance.

Touch sensors are categorized into two types, namely self-capacitance and mutual capacitance. The self-capacitive sensor detects the presence of a finger by measuring the capacitance change caused by the distance between the finger and the touch electrode. As the finger approaches, the sensed capacitance increases. In contrast, the mutual-capacitive sensor detects changes in capacitance between two electrodes due to fringe field interference. In this case, an approaching finger decreases the capacitance. We see that actual contact isn't necessary, which is why the sensor can also be used as a proximity sensor.

Artificial hair sensors (AHS) generally use a cantilever-like structure which extends out-of-plane and converts a mechanical deflection into an electrical signal. Applications include flow sensing in air and water, inertial, rotational, and acoustic sensing.

The sensor in Fig. 2.8 uses a hair structure on a polymer diaphragm membrane to convert lateral mechanical deflection of the hair into a change in capacitance at the base.

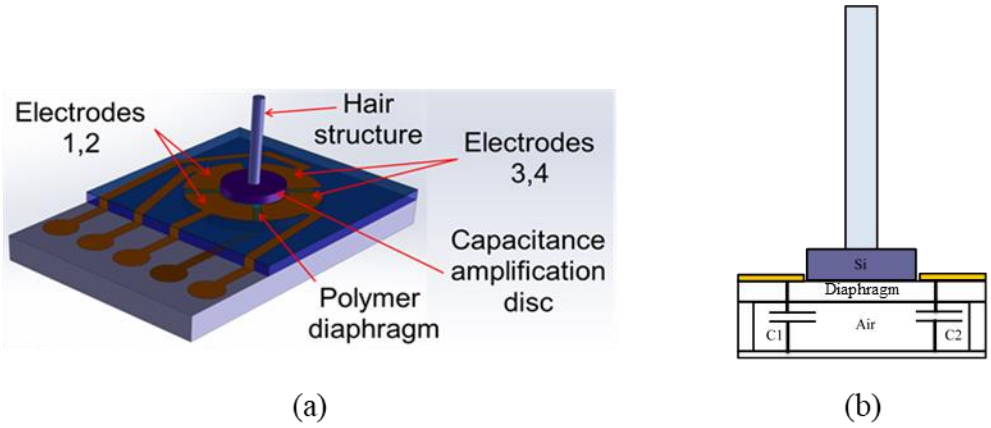


Figure 2.8. Capacitive airflow sensor showing hair-like structure on a diaphragm with pie-shaped electrodes for directional sensing: (a) MEMS hair structure; (b) Cross-sectional view. **[12]**

The electrodes effectively act as parallel plate capacitors that increase or decrease their capacitance as the distance between each electrode and an underlying electrode decreases or increases, respectively. When the hair deflects, electrodes opposite each other experience equal and opposite changes in capacitance. Therefore, a differential capacitance ($\Delta C = C1 - C2$) can be observed in both orthogonal directions, corresponding to the deflection of the vertical hair. Fig. 2.8 shows the structure and a cross-sectional view.

Soft capacitive strain sensors have been used in many applications such as motion detection, soft robotics, and tactile sensing. These sensors are highly stretchable and flexible allowing them to sustain high strains. The predominant variation in capacitance occurs when the gap distance between the interdigitated combs increases or decreases as the sensor is stretched. The sensors shown in Fig. 2.9 were fabricated using a conductive PDMS (cPDMS) to create the elastomer conductor.

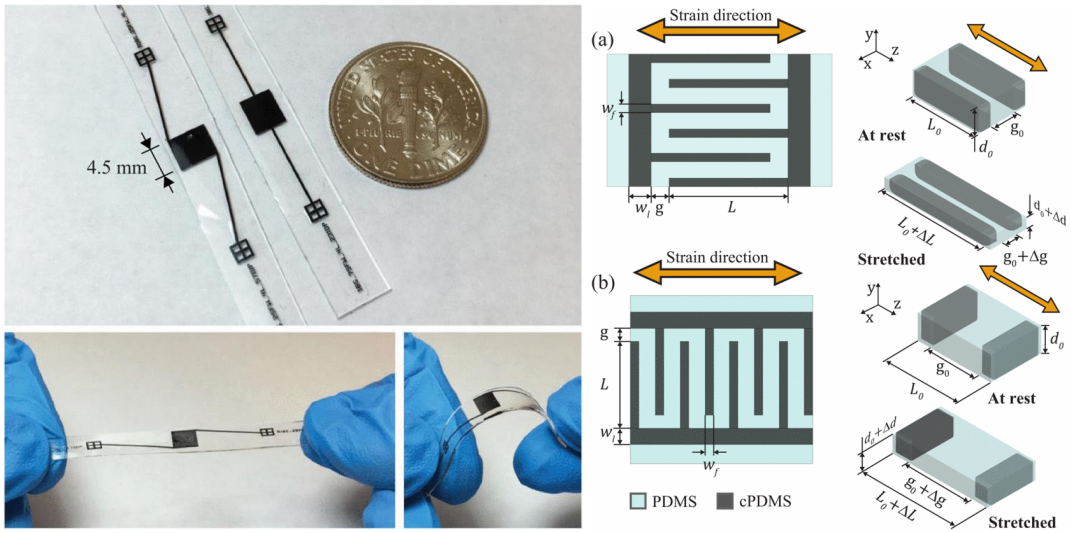


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Figure 2.9. Soft capacitive sensor samples (left) and working principle (right) of the proposed sensor: (a) Lateral comb (lc) and (b) transverse comb (tc). Source: **[13]**

Chapter 3

Capacitive Interface Circuits

3.1 Introduction

Generally, capacitive sensors use a change in capacitance to create an electrical signal which detection circuits process for readout. Detection circuits consist of a front-end interface circuit that turns this variation into a voltage, current, frequency, pulse width variation, or digital code. When the circuit converts a capacitance into a digital representation, it is considered a Capacitance-to-Digital Converter (CDC). Since detection circuits are commonly used to communicate with other devices, such as computers or microcontrollers, CDCs are the most popular way of sampling capacitance variations for easy readout.

In this chapter, design considerations and potential sources of error are discussed for capacitive interface circuits. Examples of front end interface circuits are presented and roughly grouped into charge-based, oscillator-based, and bridge-based approaches. Finally, a comparison of CDC architectures is discussed with respect to resolution and speed.

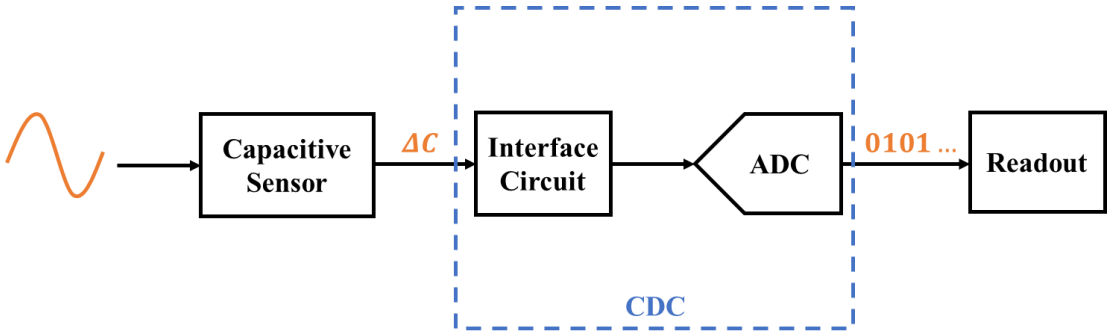

Figure 3.1. Signal chain from incoming signal to readout. The sensor converts a signal into a change in capacitance which the CDC converts into a digital code for readout.

3.2 Design Considerations

Designing interface circuits for capacitive sensors requires prior knowledge of the required sensor range, resolution, frequency characteristics of the sensors and intended application, number of sensors being interfaced to, and whether a differential reading is necessary.

Knowing the sensor range and resolution will determine whether offset compensation is necessary and how large on-chip capacitors need to be.

The frequency characteristics of the sensor and the application will determine the bandwidth of the circuit operation.

Large arrays of sensors can be utilized to improve sensitivity, selectivity, robustness, dynamic range, and functionality, which requires incorporating proper readout capabilities [14]. The number of sensors being interfaced and the desired conversion rate will determine the kind of readout and additional bandwidth necessary.

It is common for symmetrical devices to experience variations in opposing directions, in this case, a differential reading can be considered. A differential readout may be used to reduce or eliminate certain common mode variations. Additionally, a differential reading can create a linearized output, when the individual components vary nonlinearly, and double the sensitivity.

3.3 Sources of Error

Parasitic capacitance, external interference, and temperature/humidity are important factors to consider when designing capacitive sensors and systems. Parasitic capacitance can be attributed to traces and contacts between one end of the sensed

capacitor to another layer on chip or on a PCB. Environmental interference from an interfering body, radiated electromagnetic signal, or noise from nearby electronic devices can also affect the capacitance sensed. Shielding techniques can be used to mitigate these effects by driving a shield at the same potential as the sensor input.

Some other possible sources of error for the interface circuit include inaccurate or noisy reference potentials, unstable gain stages for a given bandwidth, and offsets in the comparators and sample-and-hold stages.

In many cases, the pivotal component of the circuit design is the physical on-chip capacitor itself. When an array of capacitors is used, the accuracy and linearity of the circuit depends on the capacitor tolerances of the process and how well the capacitors match the intended exponential scaling. Common approaches to reducing mismatch include using layout techniques such as unit elements in an interdigitated or common centroid configuration.

3.4 Charge-Based Capacitance Measurement

3.4.1 Rail-to-rail

This technique for capacitance measurement was first proposed in [15]. Originally proposed for measuring on-chip interconnect capacitance, the circuit uses two pseudo-inverters with non-overlapping clocks, V_1 and V_2, to charge and discharge the capacitors seen in Fig. 3.2.

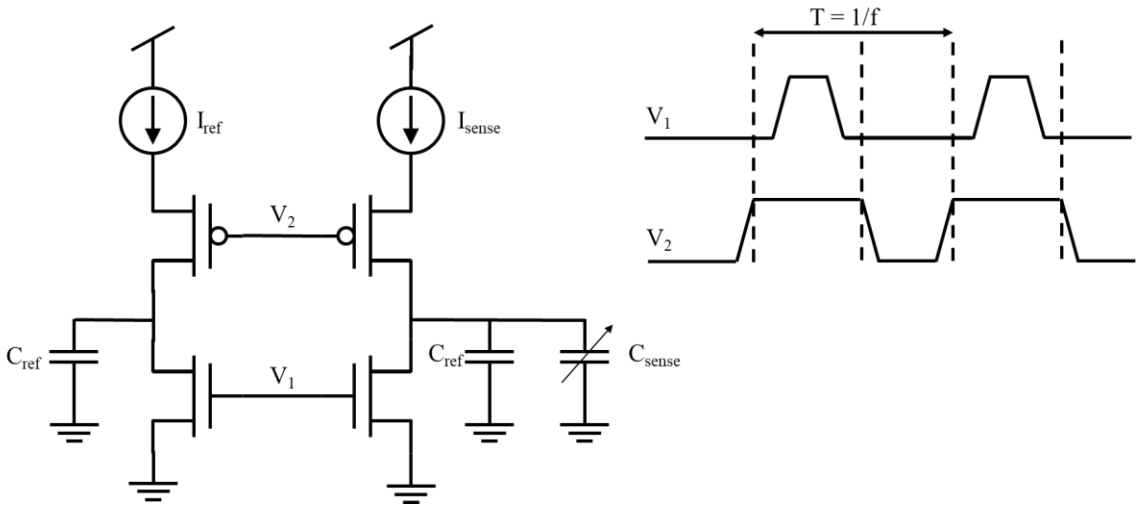

Figure 3.2. Charge-based capacitance measurement (CBCM) circuit where the sensed capacitance is determined by finding the difference in net average current between both branches.

The average current is measured for both branches,

$$I_{avg} = fV_{dd}C \tag{3. 1}$$

where f is the frequency of V_1 and V_2, V_{dd} is the supply voltage, and C is the capacitance being charged and discharged. Therefore, the sensed capacitance C_{sense} can be expressed in terms of the average net current.

$$I_{net} = I_{sense} - I_{ref} \tag{3. 2}$$

$$C_{sense} = \frac{I_{net}}{fV_{dd}} \tag{3. 3}$$

3.4.2 Charge Sharing/Balancing

A simplified circuit for capacitive sensing based on charge transfer is shown in Fig. 3.3. The circuit repeatedly charges the sense capacitor and dumps the charge onto the hold capacitor. The sensed capacitance can be found with two different approaches.

To sample the charge on the sensing capacitor, C_{sense}, switch φ_1 is closed and switches φ_2 and φ_3 are opened. After C_{sense} is charged, φ_1 will open and φ_2 will close allowing the accumulated charge to transfer to the holding capacitor C_{hold}. Once C_{hold} is charged, φ_2 will open and φ_3 will close which allows the now isolated sensing capacitor to be discharged and reset for the next sample. The sensed capacitance can be estimated immediately after φ_2 with Eq. 3.4.

$$C_{sense} = C_{hold} \frac{V_o}{V_{in} - V_o} \tag{3. 4}$$

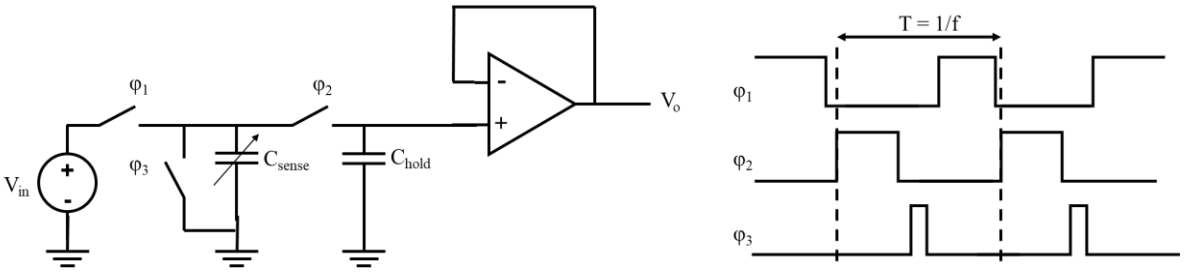

Figure 3.3. Switched capacitor charge sharing circuit showing how charge transfer from the sense capacitor to hold capacitor can be used to determine C_{sense} .

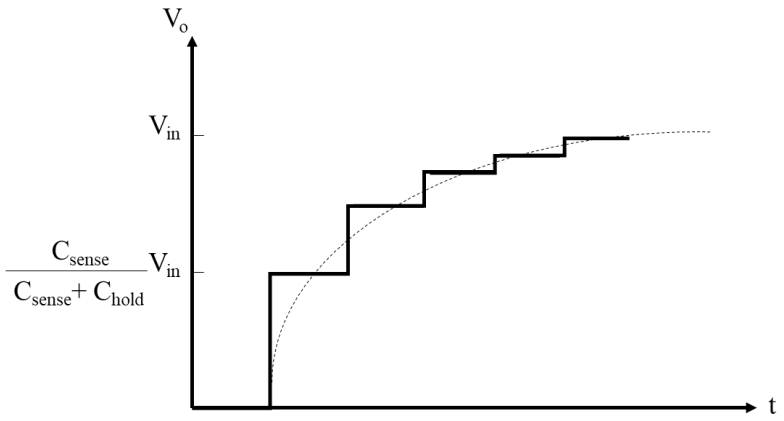

Figure 3.4. Output voltage of switched capacitor charge sharing circuit showing the RC charging characteristic.

Alternatively, by letting the output voltage approach the input voltage and using φ_3 to reset the output afterwards, the sensed capacitance can be estimated based on the RC time constant. The switches and C_{sense} act as a switched capacitor resistor with resistance depending on the switching frequency. The resistance and time constant are defined in Eq. 3.5 and 3.6.

$$R_{sc} = \frac{1}{f \cdot C_{sense}} \tag{3. 5}$$

$$\tau = R_{sc} C_{hold} = \frac{C_{hold}}{f \cdot C_{sense}} \tag{3. 6}$$

The sensed capacitance is therefore found by using Eq. 3.7.

$$C_{sense} = \frac{C_{hold}}{f \cdot \tau} \tag{3. 7}$$

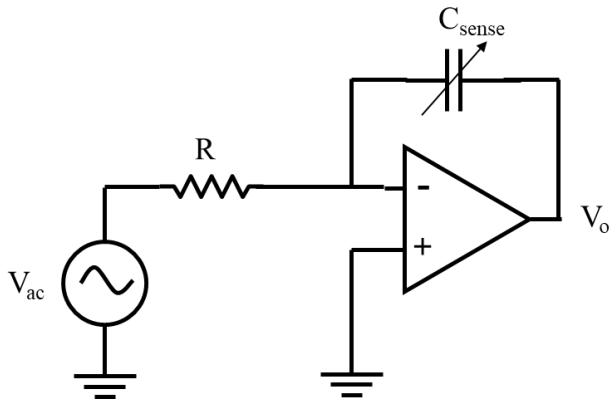

Figure 3.5. Integrator circuit for capacitive measurement where the sense capacitor is placed in the negative feedback path of the amplifier.

3.4.3 Charge/Discharge Rate

The capacitance can be measured by comparing the charge or discharge rate with an RC configuration. Typically, this approach uses an integrator and the rates are measured with a counter. Depending on how many slopes are being measured or compared, the approach will be referred to as a single-slope [16], dual-slope [17], or even triple-slope conversion [18].

$$V_o(t) = -\frac{1}{RC_{sense}} \int_0^t V_{ac}(t)dt \tag{3. 8}$$

$$C_{sense} = \frac{1}{\omega R} \left| \frac{V_{ac}(j\omega)}{V_o(j\omega)} \right| \tag{3. 9}$$

3.5 Oscillator-Based Capacitance Measurement

Measurement circuits using oscillators have been studied extensively in the past. This approach uses the sensing capacitor as a key element in an oscillator which creates a change in frequency with a change in capacitance. Examples of these types of circuits include relaxation oscillators, ring oscillators, and LC tank.

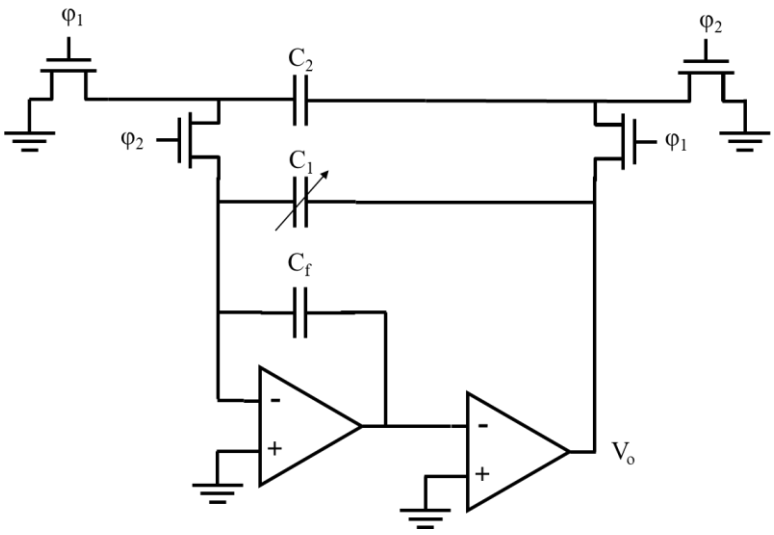

Figure 3.6. Switched capacitor relaxation oscillator circuit where C_2 is used as the switched capacitor and C_1 the sense capacitor which influences the integrated charge and frequency.

The switched capacitor relaxation oscillator presented in Fig. 3.6, was first proposed in [19].

The circuit works by using non-overlapping signals, φ_1 and φ_2, to switch and integrate the charge on capacitor C_2 and pass it to a comparator to create a square wave ouput signal. The frequency dependance is shown in Eq. 3.10.

$$f_0 = \frac{C_2}{C_1}\frac{f_{CLK}}{\left(2+\frac{V_{SS}}{V_{DD}}+\frac{V_{DD}}{V_{SS}}\right)} \tag{3. 10}$$

Here f_{CLK} is the frequency of φ_1 and φ_2, while V_{DD} and V_{SS} are defined with respect to the virtual ground of the first opamp (assumed to be 0V). This equation holds for $C_2 << C_1$.

The ring oscillator approach uses a change in the sensing capacitor across one inverter stage to produce a change in frequency.

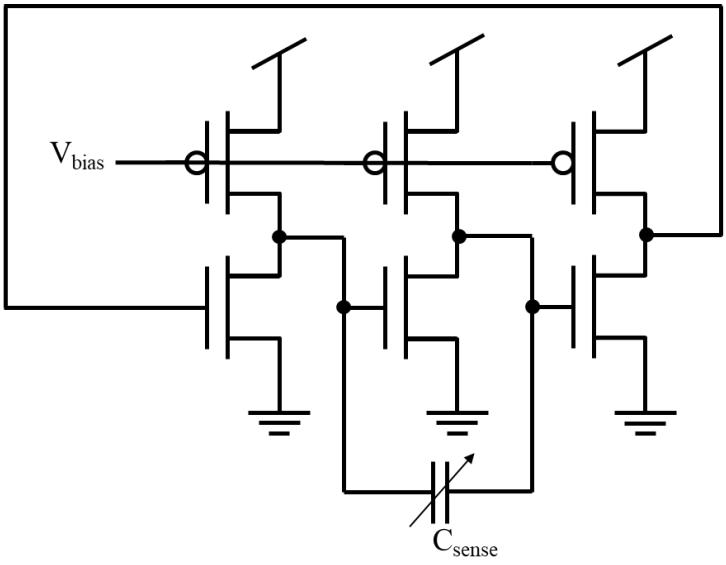

Figure 3.7. Ring oscillator circuit for capacitive measurement with sense capacitor across an inverter stage to produce a change in frequency.

The equation generally used for finding the oscillation frequency of a ring oscillator is:

$$f_{osc} = \frac{I_d}{2NV_{SW}C} \tag{3. 11}$$

Where I_d is the drain current supplied by the PMOS, N is the number of stages, V_{SW} is the switching voltage of each inverter stage, and C is the capacitance at the output of each inverter stage.

Alternatively, the Barkhausen criteria can be used for the following satisfied conditions:

$$|A_1(j\omega) \cdot A_2(j\omega) \cdot \cdots A_N(j\omega)| = 1 \tag{3. 12}$$

$$\angle A(j\omega) = \theta = tan^{-1}\, \omega RC = \frac{2k\pi}{N} \tag{3. 13}$$

Therefore, the oscillation frequency is given by:

$$\omega_{osc} = \frac{\tan\theta}{RC} \tag{3. 14}$$

For the ring oscillator circuit in Fig. 3.7, the capacitor C_{sense} can be separated into input and output Miller capacitors, C_{Mi} and C_{Mo}.

$$C_{Mi} = (1 + A)\, C_{sense} \tag{3. 15}$$

$$C_{Mo} = \left(1 + \frac{1}{A}\right) C_{sense} \tag{3. 16}$$

The frequency relationship for Eq. 3.11 becomes Eq. 3.17 and Eq. 3.14 becomes Eq. 3.18.

$$f_{osc} = \frac{I_d}{2V_{SW}(3C_o + C_{Mi} + C_{Mo})} \tag{3. 17}$$

$$\omega_{osc} = \frac{1}{R_o}\sqrt{\frac{3C_o + C_{Mi} + C_{Mo}}{C_o(C_o + C_{Mi})(C_o + C_{Mo})}} \tag{3. 18}$$

Where A is the gain of a single stage, R_o is the output resistance of each stage, and C_o is the output capacitance of each stage without contributions from C_{sense}.

3.6 Bridge-Based Capacitance Measurement

3.6.1 Voltage Amplifier

Full bridge and half bridge front-end structures have commonly been used for accurately measuring capacitance.

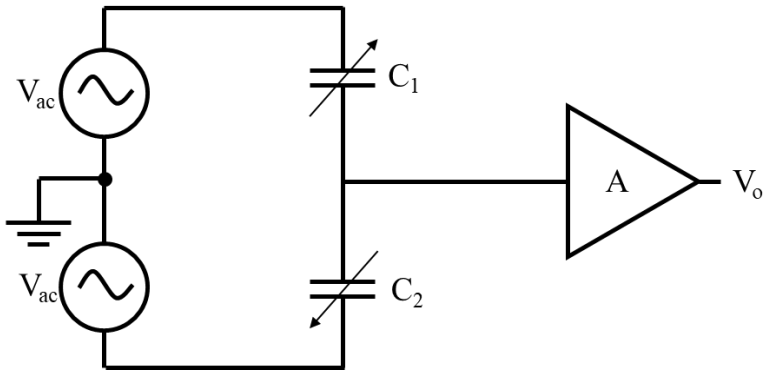

Figure 3.8. Half-bridge voltage amplifier circuit showing the voltage between varying capacitors C_1 and C_2 amplified by gain A.

In the voltage amplifier configuration, the sensing capacitor is placed in a half bridge and the voltage of the center node is amplified by an amplifier with a gain A.

The output in Fig. 3.8, for a half-bridge structure, can be expressed as:

$$V_o = \frac{C_1 - C_2}{C_1 + C_2} V_{ac} A \tag{3. 19}$$

If it is possible to arrange the sensor in a full bridge configuration, then the interface would look like the one in Fig. 3.9.

In this case the output is doubled due to the differential nature of the configuration and can be expressed as:

$$V_o = 2\frac{C_1 - C_2}{C_1 + C_2} V_{ac} A \tag{3. 20}$$

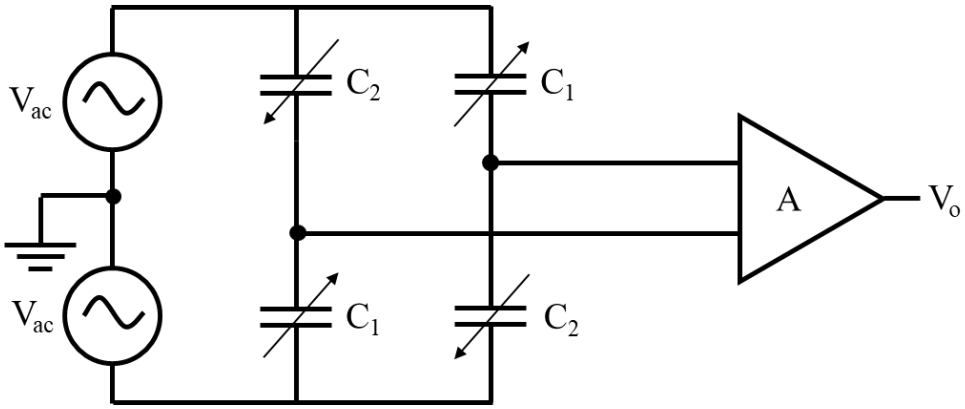

Figure 3.9. Full-bridge voltage amplifier circuit showing the difference voltage between varying capacitors C_1 and C_2 amplified by gain A.

3.6.2 Transimpedance Amplifier

The transimpedance amplifier interface uses the current created by the capacitive half-bridge and amplifies it through a feedback resistor.

The output in Fig. 3.10, can be expressed as:

$$|V_o(j\omega)| = \omega R_f (C_2 - C_1)|V_{ac}(j\omega)| \tag{3. 21}$$

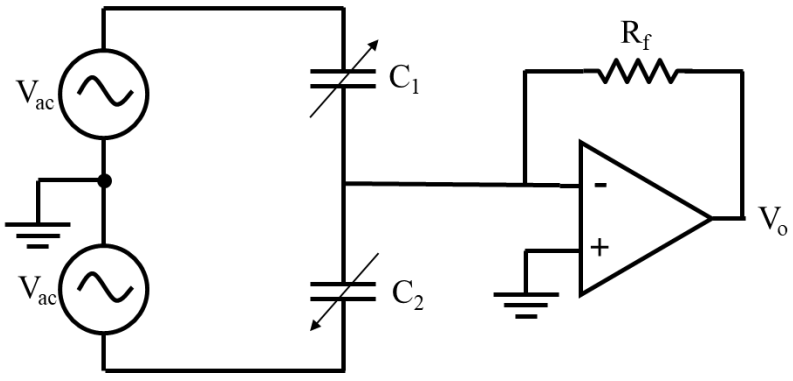

Figure 3.10. Half-bridge transimpedance amplifier circuit showing the amplifier with feedback resistor used to amplify current from varying capacitors C_1 and C_2.

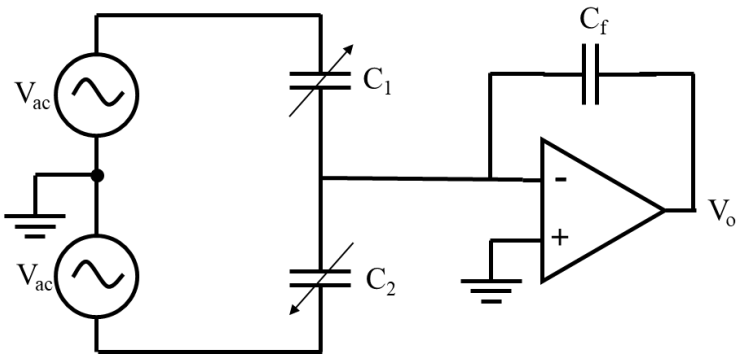

Figure 3.11. Half-bridge charge integration circuit showing the charge between varying capacitors C_1 and C_2 being integrated through feedback capacitor.

3.6.3 Charge Integration

The charge integration interface, as the name suggests, integrates the charge created by the capacitive half-bridge.

In this configuration the output can be expressed as:

$$V_o = \frac{C_1 - C_2}{C_f} V_{ac} \tag{3. 22}$$

3.7 Capacitance-to-Digital Converters

When considering data converters for any application, many performance metrics are used to determine which is the most suitable solution. Some important metrics include speed, resolution, and power.

ADC architectures have been extensively studied with the tradeoffs in resolution and sampling rate being well established. From Fig. 3.12 we see that the corner of maximum speed and resolution occurs for SAR architectures. Similarly, by comparing many CDC architectures reported in the literature for resolution and conversion rate, we see an identical trend occurs [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31].

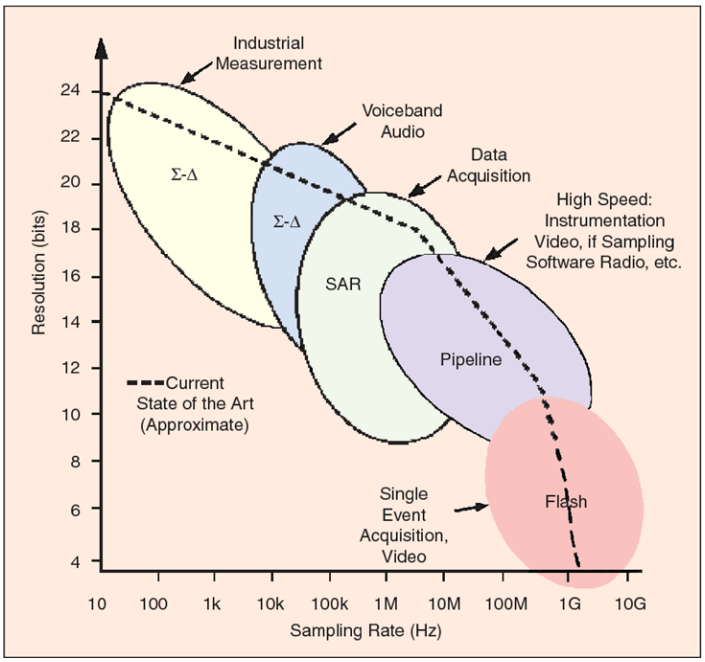

Figure 3.12. ADC architectures and applications for resolution versus sampling rate showing the approximate state of the art trend **[32]**. Copyright © 2005, IEEE

From Fig. 3.13, we find that sigma delta (ΣΔ) approaches have the highest resolution and slowest speeds whereas SAR approaches have the fastest speeds but lower resolution.

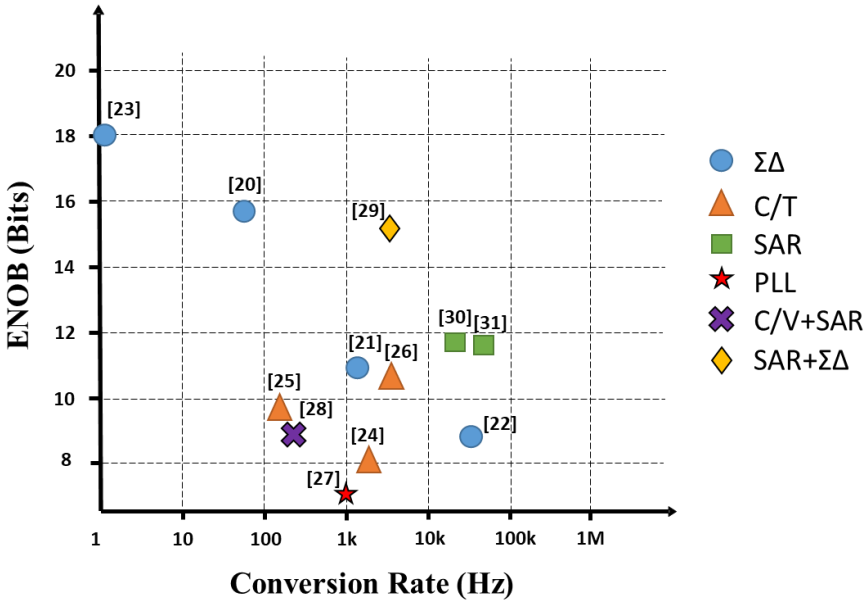

Figure 3.13. CDC resolution versus conversion rate comparison showing the state of the art for different architectures.

This is because ΣΔ architectures use high frequency oversampling techniques to achieve high resolution and low quantization noise. The output is a high frequency bitstream which is commonly passed through a filter and decimation stage to effectively downsample the signal and finally get a lower frequency representation of the capacitance. SAR architectures, on the other hand, perform a binary search to match the sensed capacitance to a bank of capacitors which directly becomes the output code representation. Hybrid architectures implement a combination of approaches such as SAR and ΣΔ. Usually, the SAR stage is used for offset cancellation while the ΣΔ stage handles the dynamic changes in capacitance. Oscillator based approaches use the change of capacitance to generate a change in frequency. The output generally uses a counter to estimate the number of pulses in a set time. Capacitance-to-time (C/T) approaches use the charge and/or discharge rate to determine capacitance. The output is commonly a count representing the time or a period modulated signal proportional to the sensed capacitance.

To meet our objective of high speed and high resolution, we further explore SAR architectures.

Chapter 4

A Two Step SAR Capacitance-to-Digital Converter

4.1 Introduction

The following design was originally tailored to meet the specifications of the flow sensor in our previous work [12]. As such, the biggest technical challenges are to retain sensitivity to relatively small changes while compensating for a large offset capacitance ($\Delta C/C \sim 10^{-4}$) and meeting bandwidth requirements ($f_s = 2*N*f_{nyquist}$, where N = number of sensors). The offset arises from the physical fabrication process and is not exactly known in advance. For a single sensor, the sampling frequency is double the resonant frequency of the AHS ($f_{resonant} \sim 10^4$ Hz). This upper limit was targeted to explore any potential effects the natural frequency of the bat hairs contribute to sensing, since they lie in the ultrasonic range [33].

The proposed capacitive sensor design uses a two-step SAR capacitance-to-digital conversion scheme shown in Fig. 4.1. This architecture was chosen for the following reasons. First, a bridge-based front-end lends itself easily for differential configurations. Second, a SAR approach digitizes the input capacitance with a bank of capacitors or capacitor DAC (CDAC) by balancing the bridge. Third, the sampling rate is only limited by how quickly the CDAC can be switched on or off (Typically ~10^4–10^7 Hz). Fourth, SAR approaches have been shown to be generally more energy efficient, even though, this is traded for better resolution. Finally, a two-step approach is used because physical attofarad capacitors are not feasible.

Two prototype designs are presented, the preliminary design is implemented in a 0.5µm CMOS process and the final design in a 0.18µm CMOS process. The features and

performance vary for both designs but the fundamental architecture is identical. The differences are described in sections 4.5 and 4.6.

4.2 Circuit Architecture

The design presented in Fig. 4.1 is a single ended configuration of the circuit. The coarse stage uses a SAR method where a CDAC is used to perform a binary search to match the sensed capacitance. The CDAC and the sensed capacitance are placed in a half bridge configuration where both ends are excited with periodic signals in anti-phase, creating a redistribution of charge on the V_X node between them. This value is sampled and compared to a reference voltage V_{Ref} to sequentially determine whether to keep or remove each capacitor in the CDAC array.

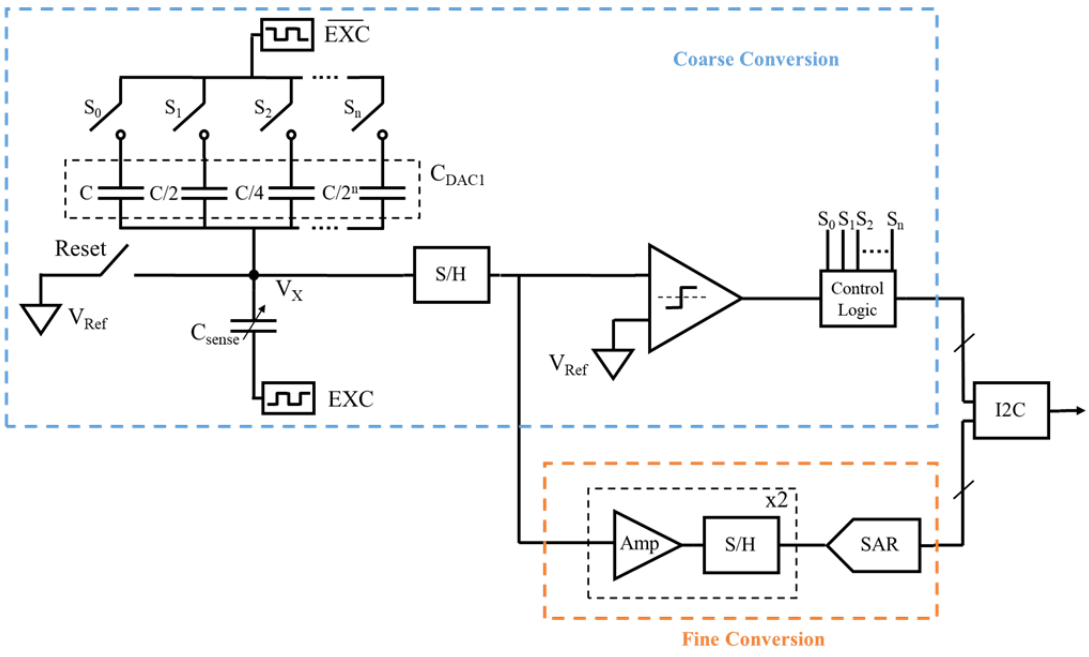

Figure 4.1. Two-step SAR capacitance-to-digital converter architecture showing the coarse conversion balancing the bridge in the front-end and the fine conversion performing a SAR conversion on the amplified residue.

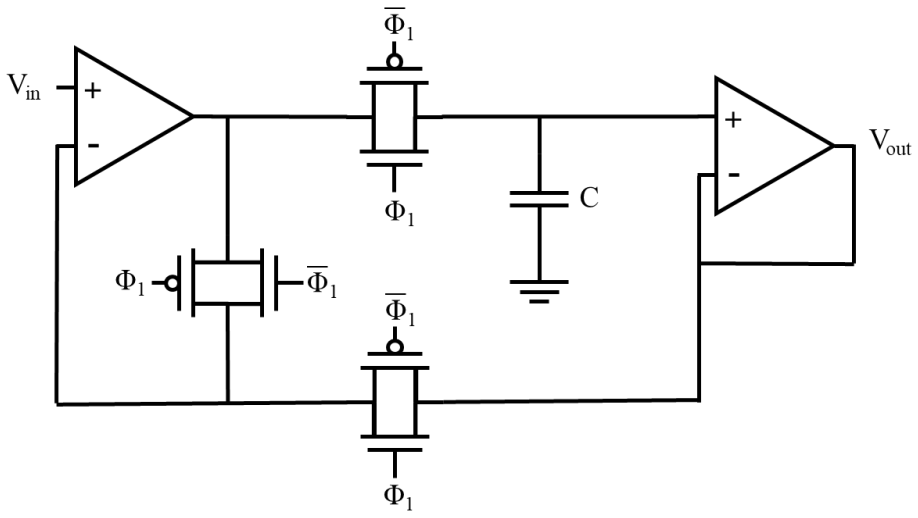

Figure 4.2. Sample-and-hold circuit using opamps as buffers around the hold capacitor and transmission gates to control the sampling.

The voltage at V_X approaches V_{Ref} as the CDAC matches the sensed capacitance. Once the best combination of capacitors is chosen, the bits are stored in a register waiting for the I^2C interface to read it out.

The sample-and-hold circuit uses a buffered input and output around the capacitor. A rail-to-rail opamp was used to adequately capture the range of voltages during the front end comparisons and the amplified residue voltages later on [34]. The circuit is shown in Fig. 4.2.

A total of 3 sample-and-hold stages and 2 amplifier stages are implemented. The amplifiers are placed between the sample-and-hold stages and use a switched capacitor design to amplify the residue voltage. The amplifier stage takes an input voltage and subtracts the reference voltage from it. It then amplifies the difference by the ratio C_1/C_2 and adds it back to a reference voltage.

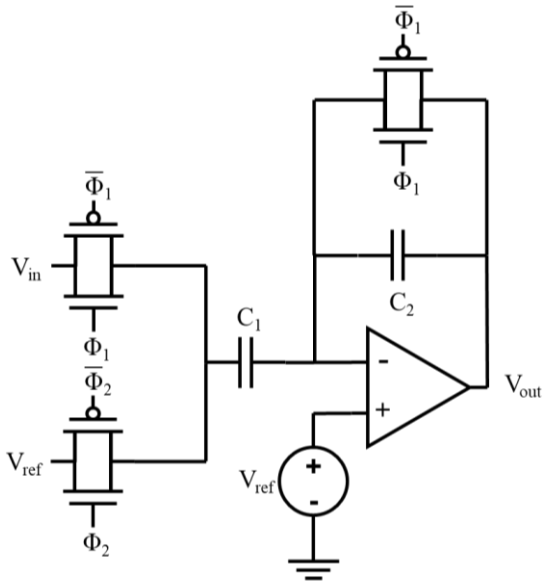

Figure 4.3. Switched capacitor amplifier circuit using the ratio of C_1 and C_2 to amplify the difference between input voltage and reference voltage with V_{ref} also setting the DC offset of the output.

$$V_{out} = \left(V_{in} - V_{Ref}\right)\frac{C_1}{C_2} + V_{Ref} \tag{4. 1}$$

The fine stage then takes the amplified residual voltage and performs a conversion with a charge redistribution SAR ADC. For the final design, an overall gain of 50 is achieved with the first amplifier using a C_1/C_2 ratio of 10 followed by a ratio of 5 in the second amplifier. The resolution of the fine conversion can be approximated as 1/50 times the smallest capacitor in the CDAC, or 200aF. Since the both stages use an 8 bit CDAC and the gain is less than 256, there will be an overlap in bits. This was done to reduce the strict requirements in comparator accuracy while still meeting a desired sub femtofarad resolution. The fine conversion then repeats until the value saturates, indicating the need to perform another coarse conversion for front end compensation. In the ideal case, where there is no parasitic capacitance and the second SAR stage matches

the input amplified residue voltage exactly, the sensed capacitance can simply be expressed as:

$$C_{sense} = \frac{1+B}{1-B} C_{DAC1} \quad (4.\ 2)$$

$$B = \frac{V_{DD}-V_{Ref}}{A\,V_{DD}} \frac{C_{DAC2}}{C_{FS}} \quad (4.\ 3)$$

Where A is the gain of the switched capacitor amplifier stages, C_{DAC1} is the coarse conversion capacitance, C_{DAC2} is the fine conversion capacitance, and C_{FS} is the full scale capacitance of one CDAC (i.e. 2.55pF for 8-bit DAC with 10fF LSB). Therefore, according to (2), the maximum sensed capacitance range is about 2.6pF.

4.3. Sensed Capacitance Derivation

4.3.1 Individual Configuration

The following steps were used to derive the relationship between the sensed capacitance with the coarse and fine bits.

The front-end of the sensor is a key aspect for understanding how compensation and capacitance-to-digital conversion can be achieved. It is best understood in two phases, ϕ_1 and ϕ_2. In ϕ_1, the middle node V_X is initialized to V_{Ref} while the other ends of C_{DAC1} and C_{Sense} are held at V_{DD} and ground, respectively. In ϕ_2, the ends of the capacitors are flipped in polarity while V_X is free to move. If both capacitors C_{DAC1} and C_{Sense} are matched exactly, then we can see that V_X stays at V_{Ref} since no charge would need to be redistributed.

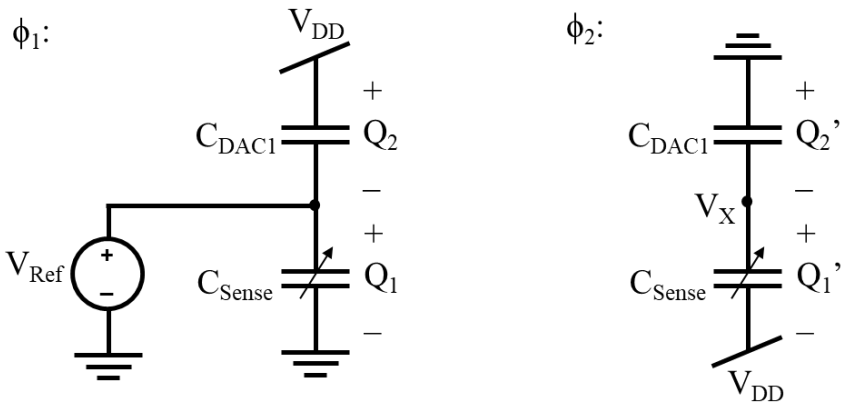

Figure 4.4. Front-end analysis showing the configuration in two phases. The first phase sets the initial conditions and the second phase allows charge to redistribute on V_X. C_{DAC1} is used to match C_{Sense}.

ϕ_1:

$$Q_1 = V_{Ref} C_{Sense} \tag{4. 4}$$

$$Q_2 = \left(V_{DD} - V_{Ref}\right) C_{DAC1} \tag{4. 5}$$

ϕ_2:

$$Q_1{}' = (V_X - V_{DD}) C_{Sense} \tag{4. 6}$$

$$Q_2{}' = -V_X C_{DAC1} \tag{4. 7}$$

Using conservation of charge, we can solve for Vx.

$$Q_1' - Q_1 = Q_2' - Q_2 \tag{4. 8}$$

$$(V_X - V_{DD}) C_{Sense} - V_{Ref} C_{Sense} = -V_X C_{DAC1} - \left(V_{DD} - V_{Ref}\right) C_{DAC1} \tag{4. 9}$$

$$V_X = V_{Ref} + \frac{C_{Sense} - C_{DAC1}}{C_{Sense} + C_{DAC1}} V_{DD} \tag{4. 10}$$

Having found V_X from the coarse conversion, we can now look at the fine conversion stage. The final amplified residue voltage appears as V_{oSH3} and the matched voltage V_{X2} from the fine conversion in Fig. 4.5.

$$V_{oSH3} = \left(V_X - V_{Ref}\right)A + V_{Ref} \tag{4. 11}$$

$$V_{X2} = V_{Ref} + \left(V_{DD} - V_{Ref}\right)\frac{2^{N-1}}{2^N - 1}\sum_{n=0}^{N-1}\frac{B_n}{2^n} \tag{4. 12}$$

Eq. 4.12 describes the voltage V_{X2} in terms of the sum of bits B_n from C_{DAC2}. However, the equation can simply be rewritten in terms of the C_{DAC2} capacitance divided by the full scale capacitance C_{FS} of the CDAC.

$$V_{X2} = V_{Ref} + \left(V_{DD} - V_{Ref}\right)\frac{C_{DAC2}}{C_{FS}} \tag{4. 13}$$

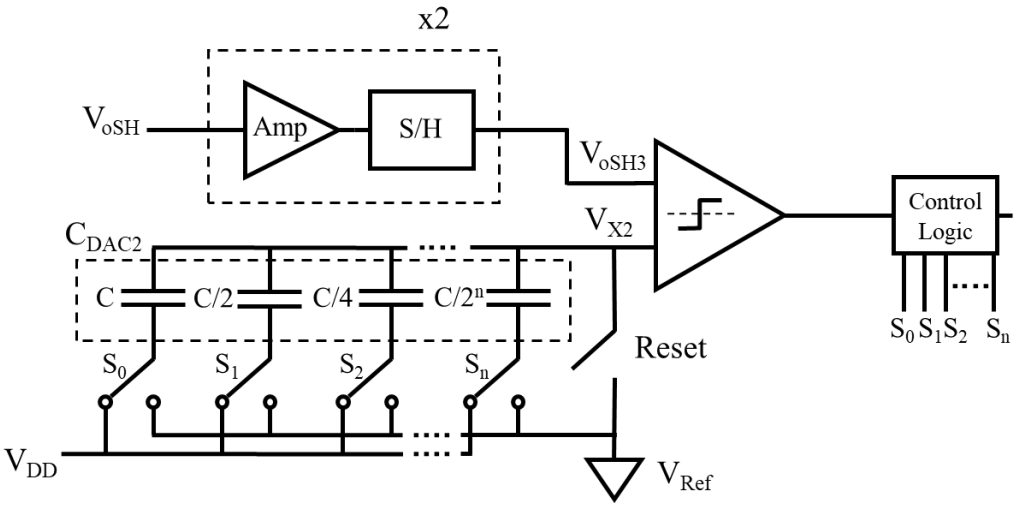

Figure 4.5. Fine conversion stage showing SAR charge redistribution circuit used to match the amplified residue voltage.

Now if we assume the fine conversion stage matches the amplified residue exactly (i.e. $V_{oSH3} = V_{X2}$), we can solve for V_X.

$$\left(V_X - V_{Ref}\right)A + V_{Ref} = V_{Ref} + \left(V_{DD} - V_{Ref}\right)\frac{C_{DAC2}}{C_{FS}} \tag{4. 14}$$

$$V_X = V_{Ref} + \frac{V_{DD}-V_{Ref}}{A}\frac{C_{DAC2}}{C_{FS}} \tag{4. 15}$$

Finally, by substituting Eq. 4.10 for V_X, we can solve for C_{Sense}

$$V_{Ref} + \frac{C_{Sense}-C_{DAC1}}{C_{Sense}+C_{DAC1}}V_{DD} = V_{Ref} + \frac{V_{DD}-V_{Ref}}{A}\frac{C_{DAC2}}{C_{FS}} \tag{4. 16}$$

$$C_{Sense} = \frac{\frac{V_{DD}}{V_{DD}-V_{Ref}}A + \frac{C_{DAC2}}{C_{FS}}}{\frac{V_{DD}}{V_{DD}-V_{Ref}}A - \frac{C_{DAC2}}{C_{FS}}}C_{DAC1} \tag{4. 17}$$

or

$$C_{Sense} = \frac{1+B}{1-B}C_{DAC1} \tag{4. 2}$$

Where

$$B = \frac{V_{DD}-V_{Ref}}{A\,V_{DD}}\frac{C_{DAC2}}{C_{FS}} \tag{4. 18}$$

If we include the effect of parasitic capacitance C_p from V_X to ground and error voltage V_{err} from the mismatch in V_{oSH3} and V_{X2}, the complete sensed capacitance relationship becomes

$$C_{Sense} = \frac{1+B+\frac{V_{err}}{A\,V_{DD}}}{1-B-\frac{V_{err}}{A\,V_{DD}}}C_{DAC1} + \frac{B+\frac{V_{err}}{A\,V_{DD}}}{1-B-\frac{V_{err}}{A\,V_{DD}}}C_p \tag{4. 19}$$

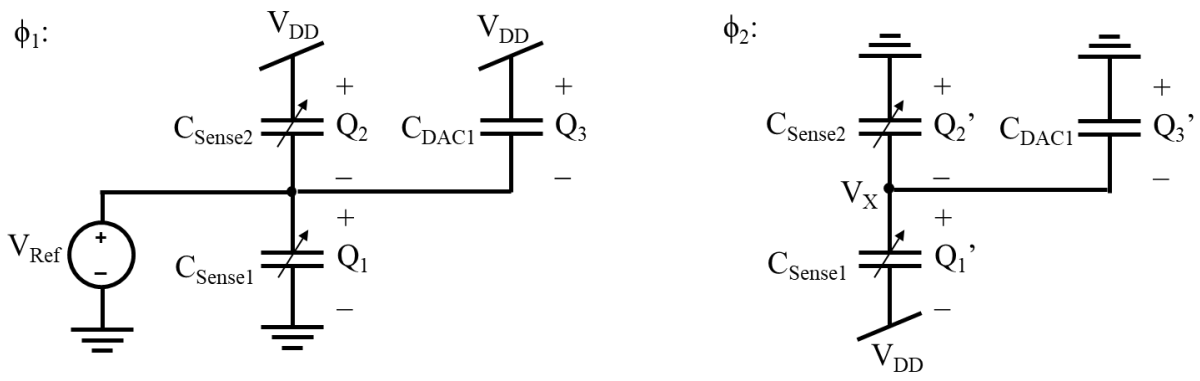

Figure 4.6. Front-end analysis of differential configuration in two phases. The first phase sets the initial conditions and the second phase allows charge to redistribute on V_X. C_{DAC1} is used to match the difference C_{Sense1} - C_{Sense2}.

4.3.2 Differential Configuration

The approach described up until now is for an individual capacitance configuration. However, the same analysis can be performed for the differential configuration.

In the differential case shown below, C_{DAC1} now matches the difference ΔC_{Sense} between sensing capacitors C_{Sense1} and C_{Sense2}. Since the only difference between the individual and differential configurations is what C_{DAC1} represents, the rest of the analysis after the front end stays the same. For C_{Sense2} smaller than C_{Sense1}, C_{DAC1} is set in parallel to C_{Sense2} to make up the difference and $\Delta C_{Sense} = C_{Sense1} - C_{Sense2}$.

ϕ_1:

$$Q_1 = V_{Ref} C_{Sense1} \tag{4. 20}$$

$$Q_2 = \left(V_{DD} - V_{Ref}\right) C_{Sense2} \tag{4. 21}$$

$$Q_3 = \left(V_{DD} - V_{Ref}\right) C_{DAC1} \tag{4. 22}$$

ϕ_2:

$$Q_1' = (V_X - V_{DD})C_{Sense1} \quad (4.\ 23)$$

$$Q_2' = -V_X C_{Sense2} \quad (4.\ 24)$$

$$Q_3' = -V_X C_{DAC1} \quad (4.\ 25)$$

$$\Delta C_{Sense} = \frac{1+B}{1-B} C_{DAC1} + \frac{2B}{1-B} C_{Sense2} \quad (4.\ 26)$$

Again, by including the non-ideal terms C_p and V_{err}, the complete relationship becomes:

$$\Delta C_{Sense} = \frac{1+B+\frac{V_{err}}{AV_{DD}}}{1-B-\frac{V_{err}}{AV_{DD}}} C_{DAC1} + \frac{2B+\frac{V_{err}}{AV_{DD}}}{1-B-\frac{V_{err}}{AV_{DD}}} C_{Sense2} + \frac{B+\frac{V_{err}}{AV_{DD}}}{1-B-\frac{V_{err}}{AV_{DD}}} C_p \quad (4.\ 27)$$

In the differential case, we see that knowing the capacitance C_{Sense2} becomes necessary for accurately determining the differential capacitance.

4.4. Resolution and ENOB

When referring to resolution in this work, an important distinction is made between the capacitance resolution and the ENOB resolution. The capacitance resolution is the capacitance value that the LSB in the converter represents and is expressed in units of Farads. By contrast, the ENOB resolution is an accuracy figure of merit relating the SNR performance to an ideal CDCs resolution with a certain number of bits (limited only by the quantization noise). The ENOB resolution is expressed in bits and is a practical way of determining overall measurement accuracy of the converter. Sources of error will affect a converters accuracy or precision which is reflected in the ENOB resolution. Some sources of error may affect accuracy which is how far the measured value is from the true value, while other sources affect the precision which is the repeatability of

measurements. As an example, parasitic capacitance introduces a fixed offset error which affects accuracy but not precision while thermal noise introduces variations during operation which affect both accuracy and precision.

To determine the theoretical resolution of the circuit, Eq. 4.19 can be used to find the change in C_{sense} when C_{DAC2} is incremented by a least significant bit (LSB) of 10fF (the smallest capacitor in the fine CDAC). The resolution and effective number of bits (ENOB) due to quantization noise is plotted for the converters input capacitance range. In addition, the effect of varying parasitic capacitance, gain, and fine conversion voltage error on the accuracy is presented. These cases reveal that gain variations affect the slope of the resolution curve, while parasitic capacitance presents itself as an offset.

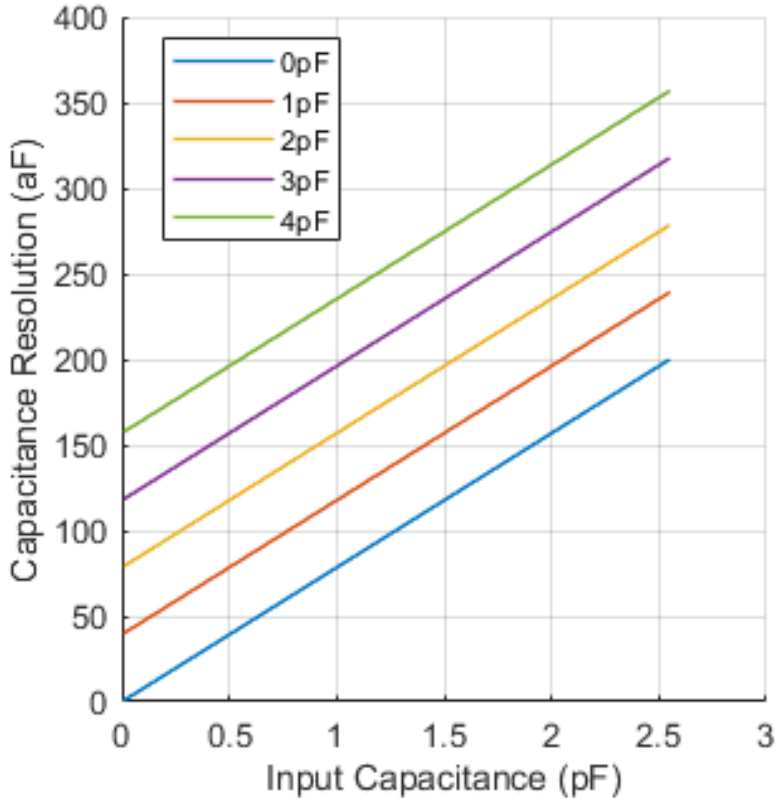

Figure 4.7. Capacitance resolution versus input capacitance determined by taking an LSB incremental difference of C_{sense} equation. The resolutions accuracy is shown for different parasitic capacitance values.

It is important to note that no other error sources were included for the following analysis which would reduce the achievable resolution. For this design, the two largest limiting factors of resolution are thermal noise and comparator offset. The achievable resolution due to these factors is explored in sections 4.4.1 and 4.4.2.

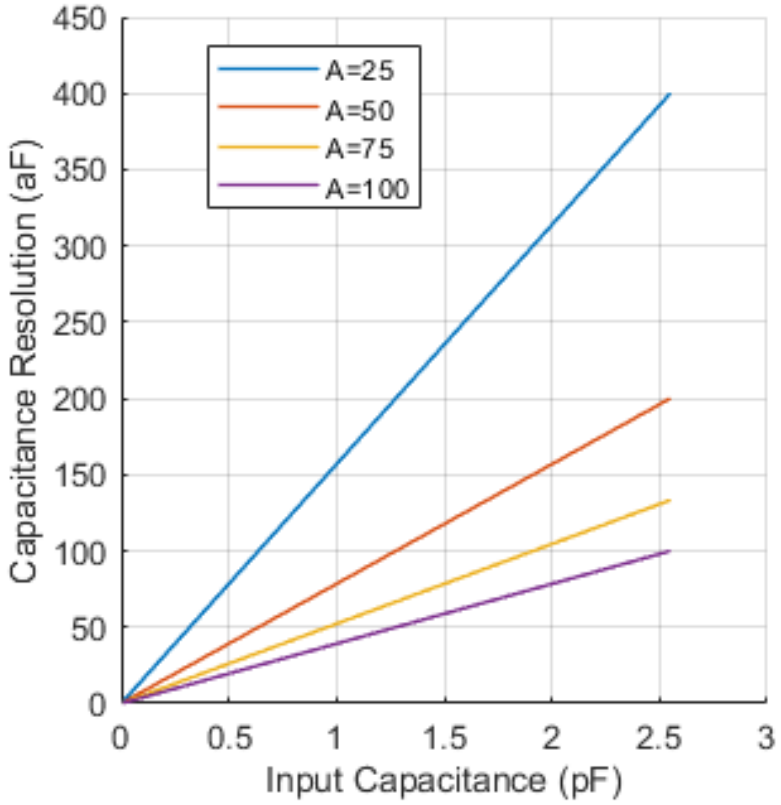

Figure 4.8. Capacitance resolution versus input capacitance determined by taking an LSB incremental difference of C_{sense} equation. The resolution is shown for different gain values.

Figures 4.7 and 4.8 reveal the resolution scales with input capacitance. Additionally, parasitic capacitance and gain change the offset and slope of the resolution, respectively. Finally, by looking at the effect of voltage mismatch for the fine conversion stage, we see that it makes very little difference to the resolution. Fig. 4.9 reveals even at 1 V difference, less than 2.5 aF error occurs in the accuracy.

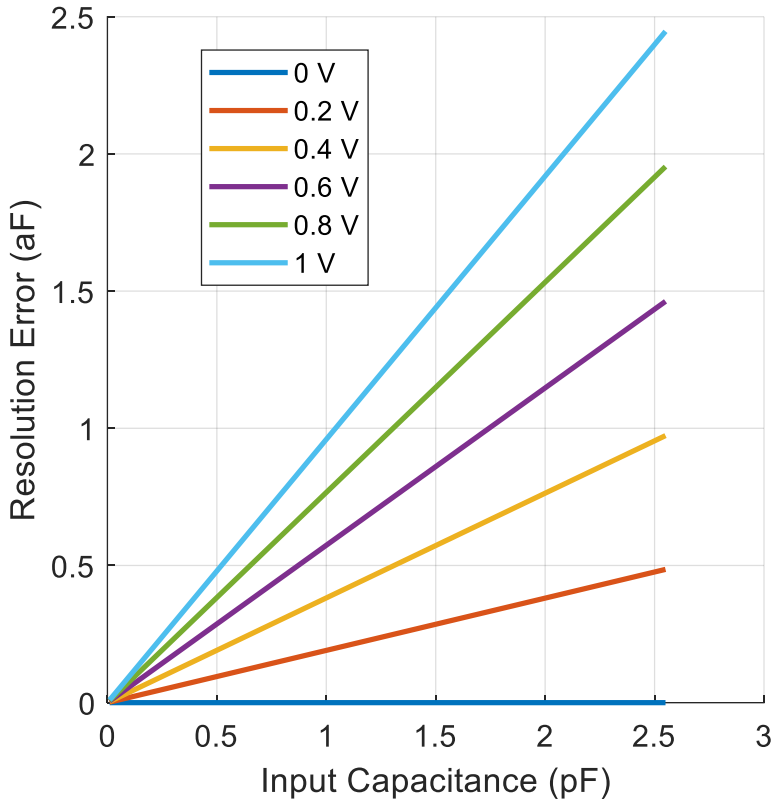

Figure 4.9. Capacitance resolution error versus input capacitance showing effect on resolutions accuracy for different fine conversion voltage errors.

To express the converters ideal performance, we consider the input capacitance and its corresponding resolution to define the ENOB as:

$$ENOB = \log_2\left(\frac{Input\ Capacitance}{Capacitance\ Resolution}\right) \quad (4.\ 28)$$

Using Eq. 4.28, the maximum theoretical ENOB is found to be 13.6 bits for an implemented gain of 50 with no parasitic capacitance. The coarse conversion and fine conversion ranges will necessarily be overlapping, reducing ENOB below 16 bits, due to the use of a gain less than 256 (the 8-bit fine conversion stage is scaled by this gain). Therefore, a gain of 50 leads to the maximum ENOB being 2.4 bits less than the 16 available bits and introduces redundancy between the coarse and fine bits.

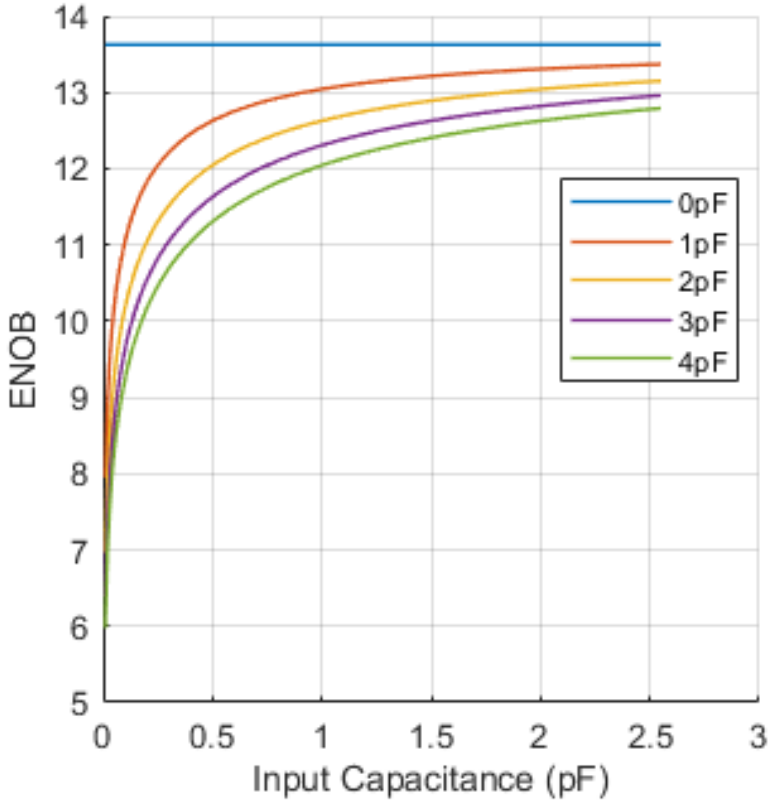

Figure 4.10. ENOB versus input capacitance showing how performance is limited across the converter range for increasing parasitic capacitance.

Fig. 4.10 shows the effect of parasitic capacitance on the ENOB. The increased parasitic capacitance introduces an error in accuracy to the sensed capacitance which can be accounted for as an offset in resolution. This decreases the input capacitance-to-resolution ratio and appears as a logarithmic curve when converted to ENOB using Eq. 4.28.

4.4.1 Noise Analysis

The noise analysis conducted focuses on the thermal noise and its effect on the achievable resolution. For this, the total noise in the fine conversion stage needs to be determined since it defines the resolution of the whole converter.

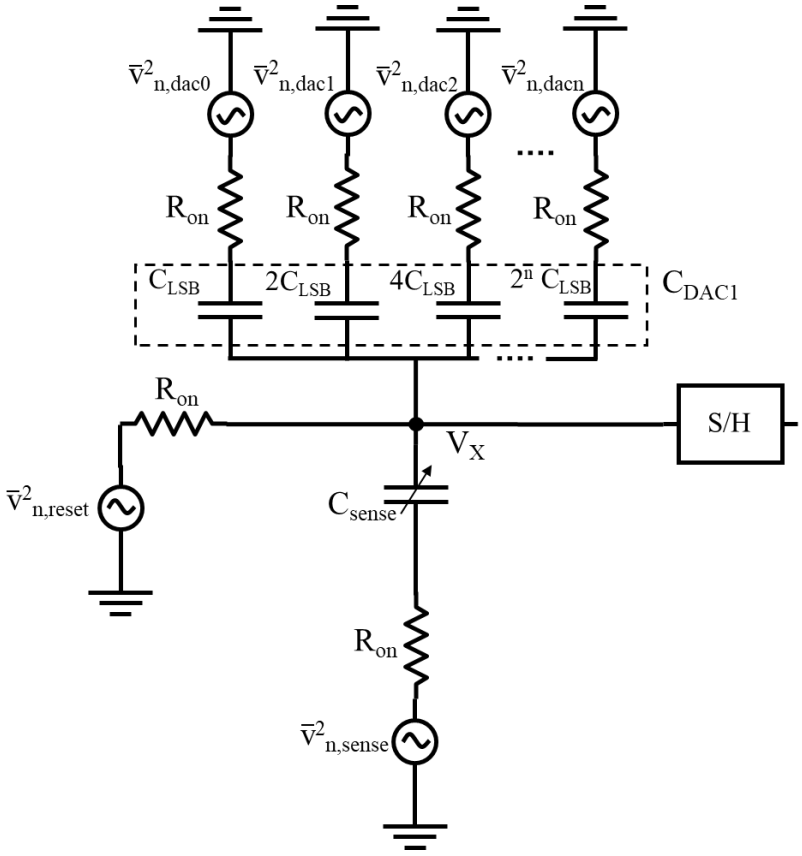

Figure 4.11. Noise contributions for front-end circuit showing the thermal noise sources from the CDAC, C_{sense}, and reset switches.

First, we begin by analyzing the noise contribution of the front-end circuit. The thermal noise contributions are due to the on resistance from the switches. The noise on the V_X node is found from three parts: the CDAC, the reset switch, and the sensed capacitor. Since these noise sources are assumed to be independent and linear, they can be found separately and summed at the end. Fig. 4.11 shows the noise contributions for the front-end circuit.

Beginning with the CDAC, we note that the noise from each bit can be found separately and summed up as well. Fig. 4.12 shows the contribution of a single bit. We define the full scale capacitance C_{FS} as the total capacitance from the capacitors in C_{DAC1}.

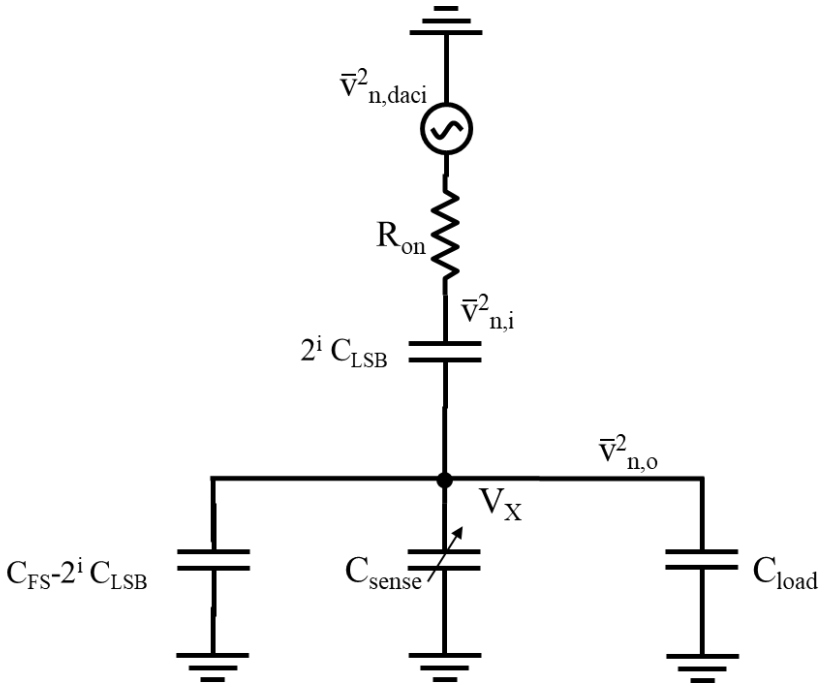

Figure 4.12. Noise contribution from switch of a single bit from C_{DAC1} where the output referred noise at V_X is a found from the capacitive voltage divider.

We also define the load capacitance on V_X as the parasitic capacitance due to the bond pad plus the capacitance from the input of the sample-and-hold stage.

$$C_{FS} = (2^N - 1)C_{LSB} \tag{4. 29}$$

$$C_{load} = C_p + C_{gsn} + C_{gsp} + C_{gdn} + C_{gdp} \tag{4. 30}$$

The thermal noise of the i-th capacitor is simply defined by the kT/C noise in Eq. 4.32, where Ci is the i-th capacitor in series with the combined capacitance at V_X. To find the output noise at V_X, we just do a voltage division of the noise calculated. The total noise from the CDAC is finally found by summing the noise contributions for every bit at V_X.

$$\bar{v}^2_{n,i} = \frac{kT}{C_i} \tag{4. 31}$$

$$C_i = \frac{2^i C_{LSB}\left(C_{FS} - 2^i C_{LSB} + C_{sense} + C_{load}\right)}{C_{FS} + C_{sense} + C_{load}} \quad (4.\ 32)$$

$$\bar{v}_{n,oi}^2 = \left(\frac{2^i C_{LSB}}{C_{FS} + C_{sense} + C_{load}}\right)^2 \bar{v}_{n,i}^2 \quad (4.\ 33)$$

$$\bar{v}_{n,o}^2 = \sum_{i=0}^{N-1} \bar{v}_{n,oi}^2 \quad (4.\ 34)$$

The noise contributions from the reset switch and the sense capacitor is defined in Eq. 4.36 and 4.38, respectively. The total noise at V_X is therefore defined as the summation from all three parts.

$$\bar{v}_{n,o2}^2 = \frac{kT}{C_{FS} + C_{sense} + C_{load}} \quad (4.\ 35)$$

$$\bar{v}_{n,sense}^2 = \frac{kT\left(C_{FS} + C_{sense} + C_{load}\right)}{C_{sense}\left(C_{FS} + C_{load}\right)} \quad (4.\ 36)$$

$$\bar{v}_{n,o3}^2 = \left(\frac{C_{sense}}{C_{FS} + C_{sense} + C_{load}}\right)^2 \bar{v}_{n,sense}^2 \quad (4.\ 37)$$

$$\bar{v}_{n,xtot}^2 = \bar{v}_{n,o}^2 + \bar{v}_{n,o2}^2 + \bar{v}_{n,o3}^2 \quad (4.\ 38)$$

For simplification purposes, the noise that reaches the fine conversion stage is defined as the total noise from the front-end amplified by the total gain of the amplification stages. As this noise is independent from the noise on the other input of the comparator, the noise can be modeled as being grouped at one input. The noise contributions in the fine conversion stage is shown in Fig. 4.13.

$$\bar{v}_{n,amp}^2 = A^2\, \bar{v}_{n,xtot}^2 \quad (4.\ 39)$$

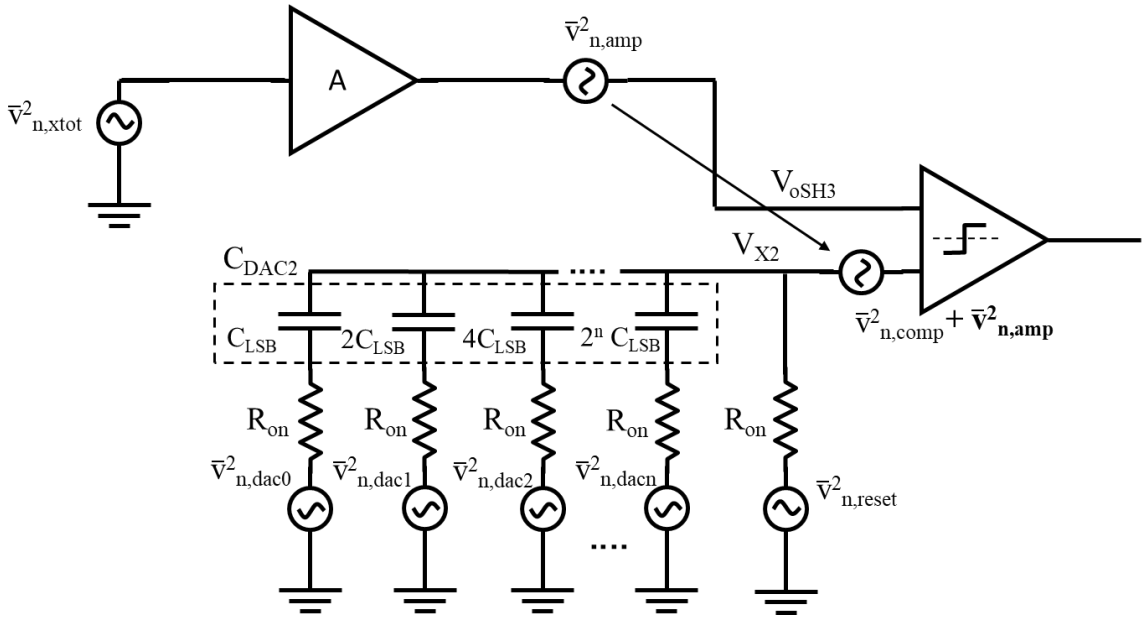

Figure 4.13. Noise contributions in fine conversion stage showing the thermal noise sources from CDAC2 and reset switches, as well as, the comparator input-referred noise added with the amplified noise from the front-end.

The noise contributions come from the CDAC, the reset switch, and the combined input-referred noise from the comparator and the amplified noise from the front-end. Just as before, the noise contribution from the CDAC is found by summing the noise from each bit. The difference here is that there is no sense capacitor and parasitic capacitance associated with a bond pad. Therefore, the load capacitance is just defined by the input of the comparator.

$$C_{load2} = C_{gsn} + C_{gdn} \tag{4. 40}$$

$$\bar{v}^2_{n,i} = \frac{kT(C_{FS}+C_{load2})}{2^i C_{LSB}(C_{FS}-2^i C_{LSB}+C_{load2})} \tag{4. 41}$$

$$\bar{v}^2_{n,oi} = \left(\frac{2^i C_{LSB}}{C_{FS}+C_{load2}}\right)^2 \bar{v}^2_{n,i} \tag{4. 42}$$

$$\bar{v}^2_{n,o} = \sum_{i=0}^{N-1} \bar{v}^2_{n,oi} \tag{4. 43}$$

The noise due to the reset switch is again identical to the front-end case and the total noise at V_{X2} is the summation of all these sources.

$$\bar{v}_{n,o2}^2 = \frac{kT}{C_{FS}+C_{load2}} \tag{4. 44}$$

$$\bar{v}_{n,x2tot}^2 = \bar{v}_{n,o}^2 + \bar{v}_{n,o2}^2 + \bar{v}_{n,comp}^2 + \bar{v}_{n,amp}^2 \tag{4. 45}$$

If we assume the case where C_{sense} and C_p are approximately equal to C_{FS}, then the total RMS voltage due to noise at V_{X2} is calculated to be 1.4mV. To compare this to the quantization noise, we convert the quantization noise capacitance found in Eq. 4.47 into a voltage by using Eq. 4.48. For a CLSB of 10fF and V_{Ref} of $V_{DD}/2$, the RMS voltage due to quantization noise is found to be 1.9mV. This means the thermal noise is comparable but the converter is not noise-limited.

$$C_q = \frac{C_{LSB}}{\sqrt[2]{12}} \tag{4. 46}$$

$$\bar{v}_q^2 = \left(C_q \cdot \frac{V_{DD}-V_{Ref}}{C_{FS}}\right)^2 \tag{4. 47}$$

To determine the achievable resolution including thermal noise, we combine it with the quantization noise and convert it into a capacitance. This capacitance represents the RMS resolution of the fine conversion stage. Since the fine conversion resolution is scaled by the gain, we can determine the ENOB for the whole two-step converter by using Eq. 4.51, where the RMS resolution is multiplied by square root of 12 to approximate an LSB quantization.

$$\bar{v}_{tot,x2}^2 = \bar{v}_{n,x2tot}^2 + \bar{v}_q^2 \tag{4. 48}$$

$$C_{tot,rms}^2 = \bar{v}_{tot,x2}^2 \left(\frac{C_{FS}}{V_{DD}-V_{Ref}}\right)^2 \tag{4. 49}$$

$$ENOB_{MAX} = log_2\left(\frac{C_{Range}}{\sqrt[2]{12}\, C_{tot,rms/A}}\right) = 13.3\ bits \qquad (4.\ 50)$$

The maximum achievable resolution due to thermal noise is now 13.3 bits. This is slightly smaller than what was shown in the ideal case. Fig. 4.14 shows this difference in terms of ENOB.

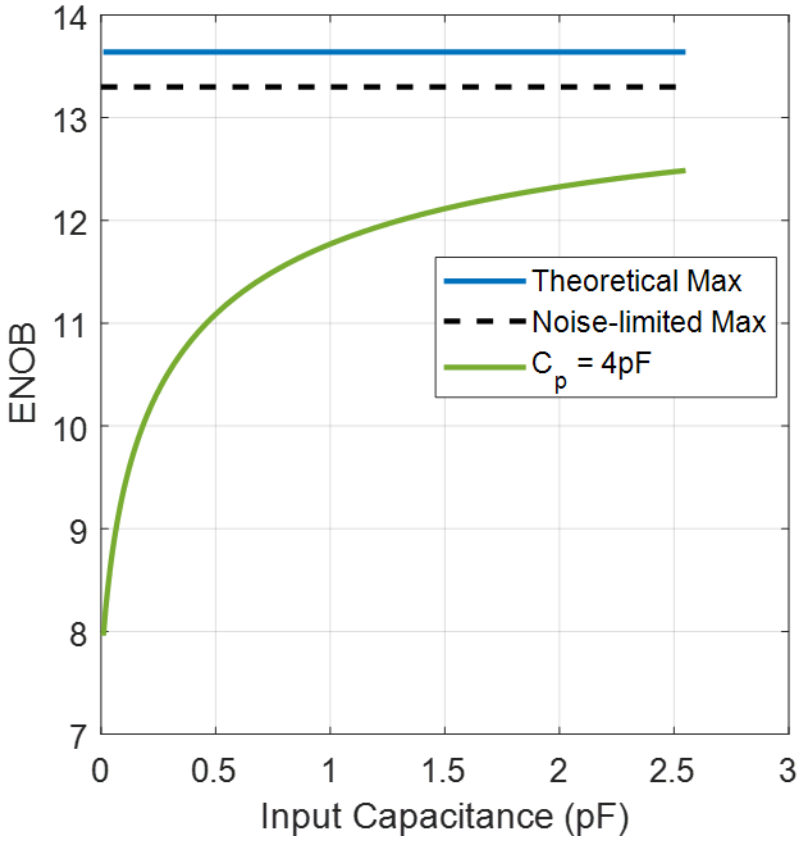

Figure 4.14. Noise-limited achievable resolution showing how the effect of thermal noise reduces the maximum ENOB and includes the further reduced performance from parasitic capacitance.

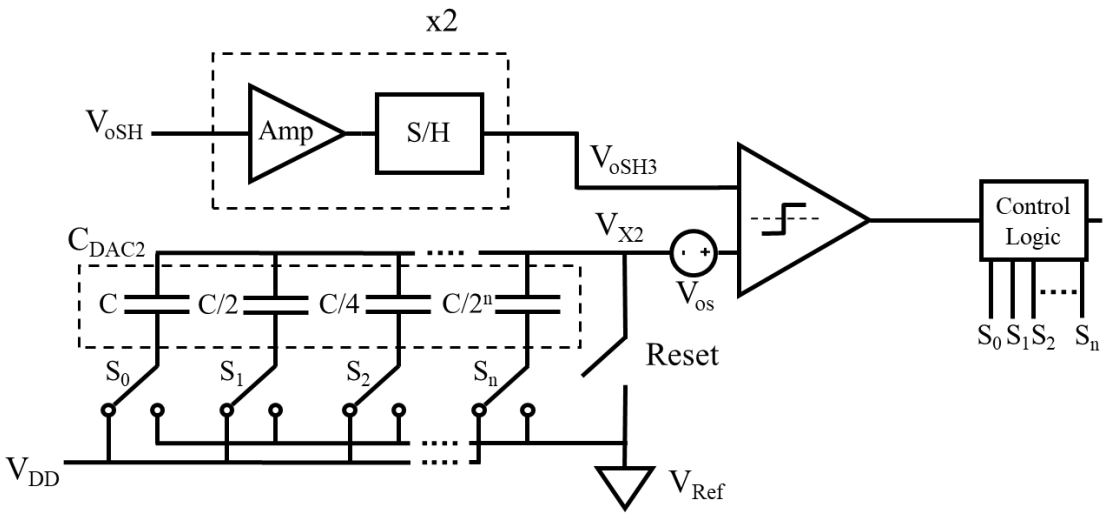

Figure 4.15. Offset voltage contribution in fine conversion stage showing the offset represented as a voltage source at the input of the comparator.

4.4.2 Offset Error

Another important limitation to achievable resolution for converters comes from the comparator offset error. A comparator offset voltage can arise from device mismatch and cause the output to change for a zero input voltage difference. If we include an offset voltage at the input of the comparator (seen in Fig. 4.15), then we can write the new relationship for voltage at V_{X2} with Eq. 4.53. We can then reinterpret the offset voltage as an error capacitance C_{err}, defined in Eq. 4.55.

$$V_{X2} = V_{OS} + V_{Ref} + \left(V_{DD} - V_{Ref}\right)\frac{C_{DAC2}}{C_{FS}} \tag{4. 51}$$

$$V_{X2} = V_{Ref} + \left(V_{DD} - V_{Ref}\right)\frac{C_{DAC2}+C_{err}}{C_{FS}} \tag{4. 52}$$

$$C_{err} = V_{OS}\frac{C_{FS}}{V_{DD}-V_{Ref}} \tag{4. 53}$$

Since the offset voltage is considered to be a statistical variable, we can rewrite the error capacitance in terms of the RMS offset voltage, and note that the RMS resolution must be greater than C_{err} to limit conversion error to one LSB.

$$C_{LSB,rms} > V_{OS,rms} \frac{C_{FS}}{V_{DD} - V_{Ref}} \tag{4. 54}$$

To approximate the RMS offset voltage, the standard deviation of threshold voltage corner values was used. This was calculated to be about 17.9mV. Following the same approach as the previous section, we can determine the worst case achievable resolution due to offset error. This value is calculated to be about 10.4 ENOB, which is a significantly more impactful effect than the thermal noise. Fig. 4.16 shows the offset voltage-limited achievable resolution compared to the ideal case.

$$ENOB_{MAX} = log_2 \left(\frac{C_{Range}}{\sqrt[2]{12}\, C_{LSB,rms}/A} \right) = 10.4\ bits \tag{4. 55}$$

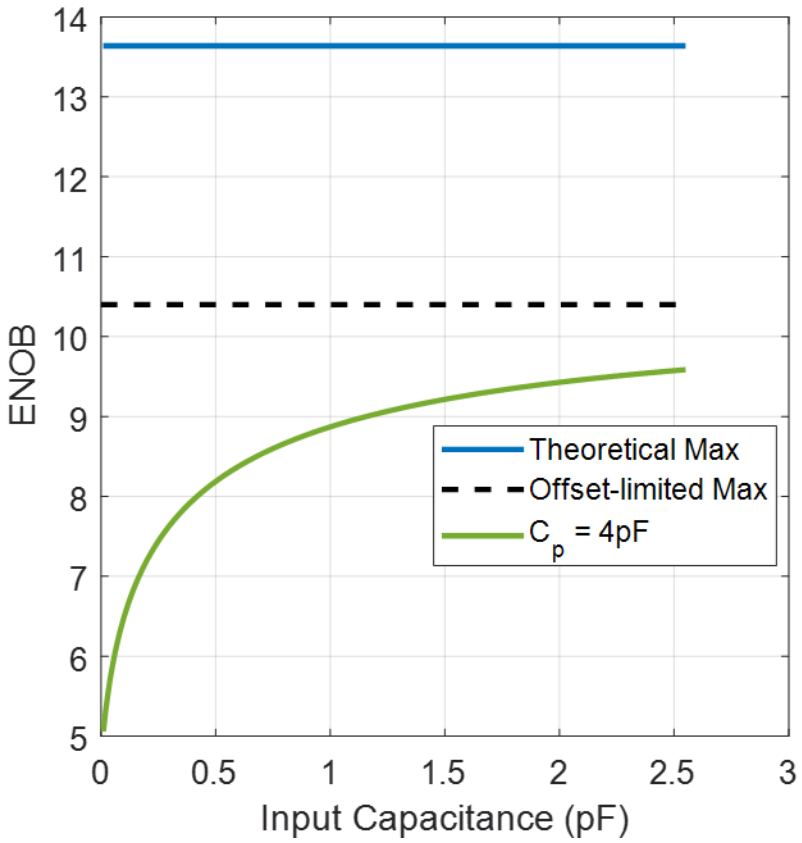

Figure 4.16. Offset-limited achievable resolution showing how the effect of comparator offset voltage reduces the maximum ENOB and includes the further reduced performance from parasitic capacitance.

4.5 Preliminary Design

4.5.1 Digital Circuits and Timing

The only digital circuit implemented in the preliminary design is the control logic. Both the coarse and fine conversion stages had their own dedicated control logic. The control logic circuit is essentially a shift register that controls the CDAC switches while simultaneously acting as the output bit encoder. The circuit is shown in Fig. 4.17.

When initialized, the first bit Q_0 is set high while Q_1-Q_n are set low. If the first bit being high, which corresponds to the first capacitor in the capacitor bank being connected, does not exceed the sensed capacitor, then we choose to keep it and shift the high bit to Q_1 on the next clock cycle. If this bit does exceed the sensed capacitor, then the SR latch for Q_1 is reset. The setting and resetting of the SR latches is controlled by the output of the comparator V_{comp}. The circuit continues to switch on and off the capacitors in the capacitor bank until reaching Q_n and holds the bit combination until being reset by the Reset signal. In this way, a binary search is accomplished to match the sensed capacitor.

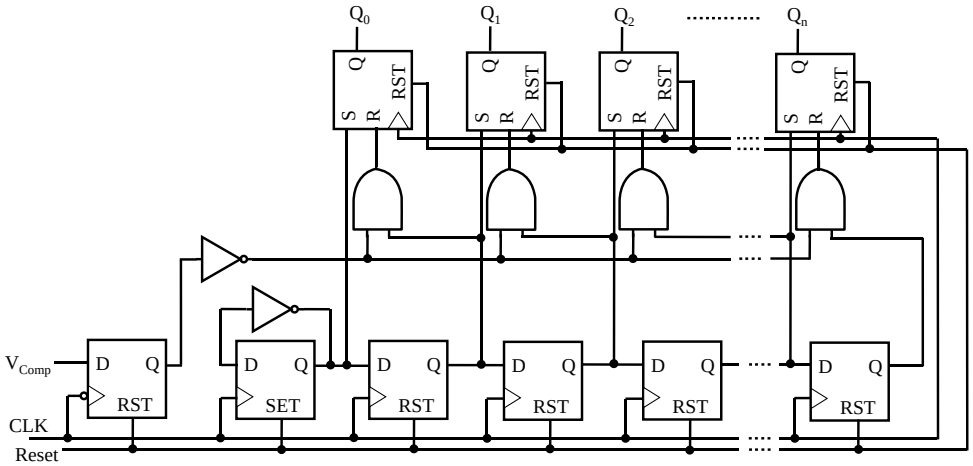

Figure 4.17. Control logic circuit made by using D flip flops as a shift register and SR flip flops to latch the bits.

All the clock, reset, excitation, and control signals were generated off-chip using a MOJO V3 Field Programmable Gate Array (FPGA). Additionally, the I^2C interface was created on the FPGA which accepted all 16 bits directly wired as inputs.

The circuit constantly performed a coarse and fine conversion which would then be read out on the I^2C bus and reset. During a conversion, the control signals triggered the sample and hold and switched capacitor amplifier stages regularly. This meant that the stages were constantly being updated even when a coarse conversion hadn't completed yet. This inevitably led to a waste in power since the residue voltage had not been properly defined yet. The final design uses the control signals efficiently by modifying the timing scheme.

4.5.2 Simulation

The following simulation results show how the preliminary design works step-by-step by showing the waveforms. Additionally, we show that by knowing the non-ideal values of gain and parasitic capacitance, we can improve the accuracy. The simulation is tested with a sensing capacitor of 1pF and an 8-bit capacitor bank with the largest capacitor being 1.28pF and the smallest 10fF. Both the coarse and fine conversion stages use identical capacitor banks and the amplification stage uses a gain of 100. Therefore, the coarse conversion stage has a sensing range of 10fF – 2.55pF while the fine conversion stage has a range of 0 – 25.628fF. The final output is expressed with 16 bits and has a total sensing range of 10fF – 2.5756pF.

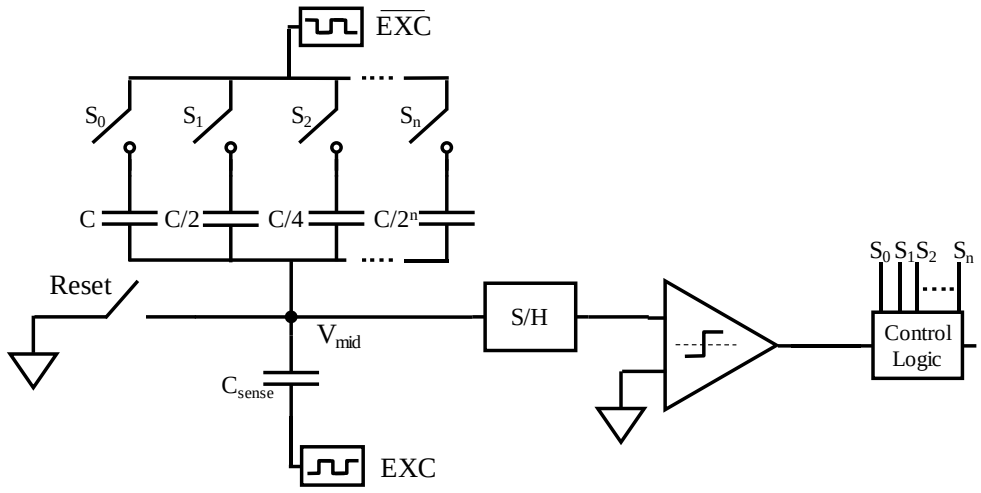

Figure 4.18. Coarse conversion circuit architecture showing CDAC used to balance the half bridge with Csense.

Beginning with the front end of the circuit, shown in Fig. 4.18, the ends of the CDAC and the sensed capacitor are excited with an excitation signal and its complement. The node V_{mid}, between the sensed capacitor and the CDAC, then changes as described in the front-end sensor analysis. If V_{mid} falls below V_{ref}, then that means the capacitor from the CDAC is too large so it is switched off and the next one is turned on. Fig. 4.19 shows V_{mid} during the coarse conversion accompanied by the excitation signals and the first 8 output bits Q. For C_{sense} = 1pF, the capacitor bank settles on the output Q=01100011 or 0.99pF.

The sample and hold circuit samples V_{mid} during the second phase of the excitation. This output, V_{oSH}, is compared with V_{ref} using a comparator and its output V_{Comp} is used as an input to the contol logic circuit.

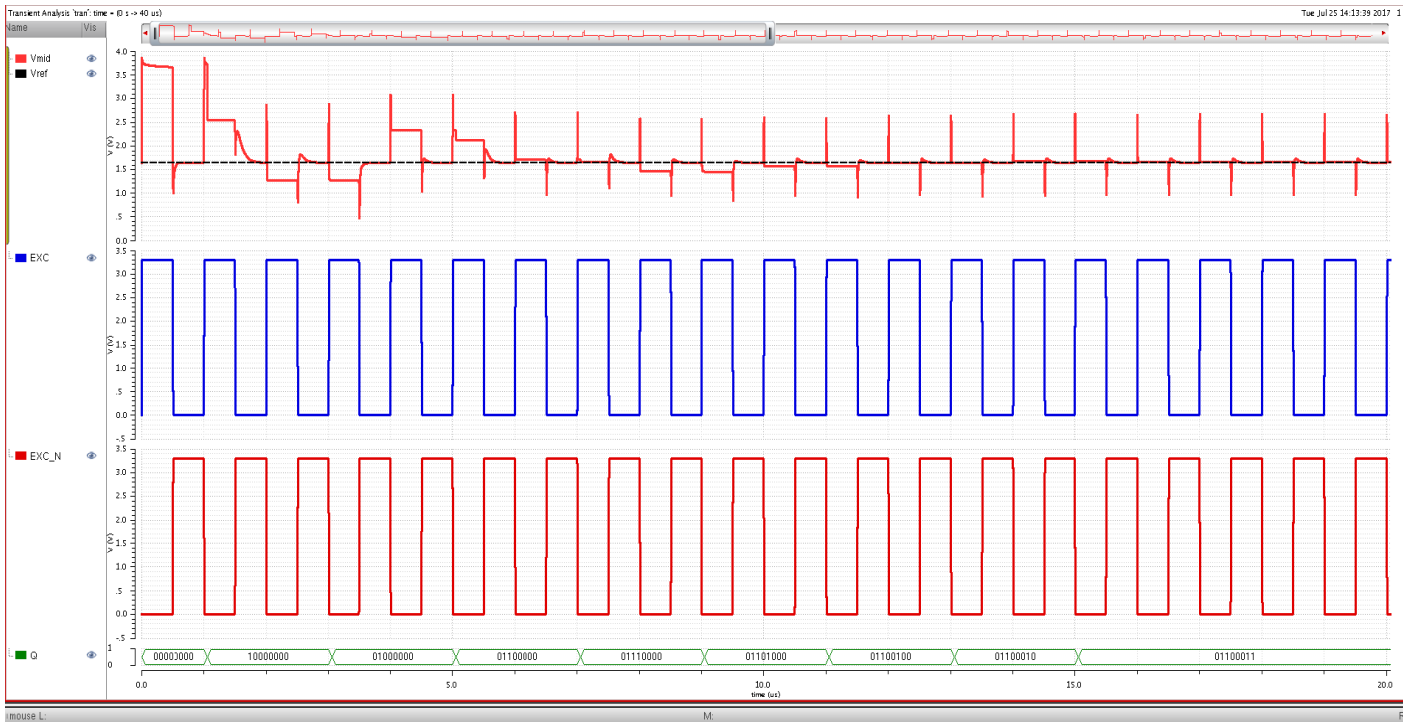

Figure 4.19. Coarse conversion simulation showing how Vmid changes as each bit in the CDAC is tested and chosen (represented as Q).

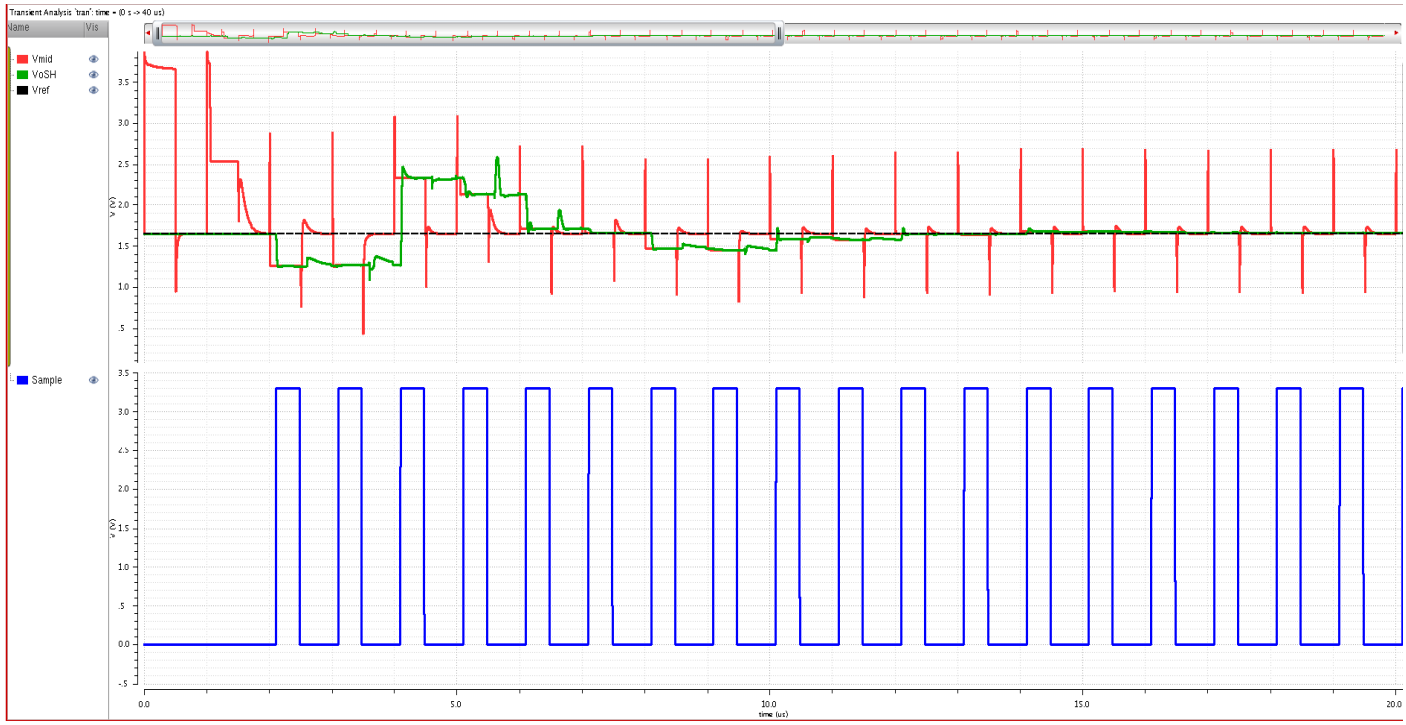

Figure 4.20. 1st stage sample-and-hold simulation showing how Vmid is sampled during a coarse conversion.

Once the coarse conversion is completed, the fine conversion can be found. The output of the first sample and hold stage will hold the residue voltage after the coarse conversion is completed. This voltage is then fed into a switched capacitor amplifier stage, a second sample and hold stage, a second amplifier stage, and a third sample and hold stage.

The amplifier circuit uses two phases, Φ_1 and Φ_2, to amplify the difference in voltage between V_{in} and V_{ref} such that $V_{out} = C_1/C_2*(V_{in} - V_{ref}) + V_{ref}$. For this design C_2= 900fF and C_1 = 9pF for the gain to be 10. Using two amplification stages, an overall gain of 100 can be achieved.

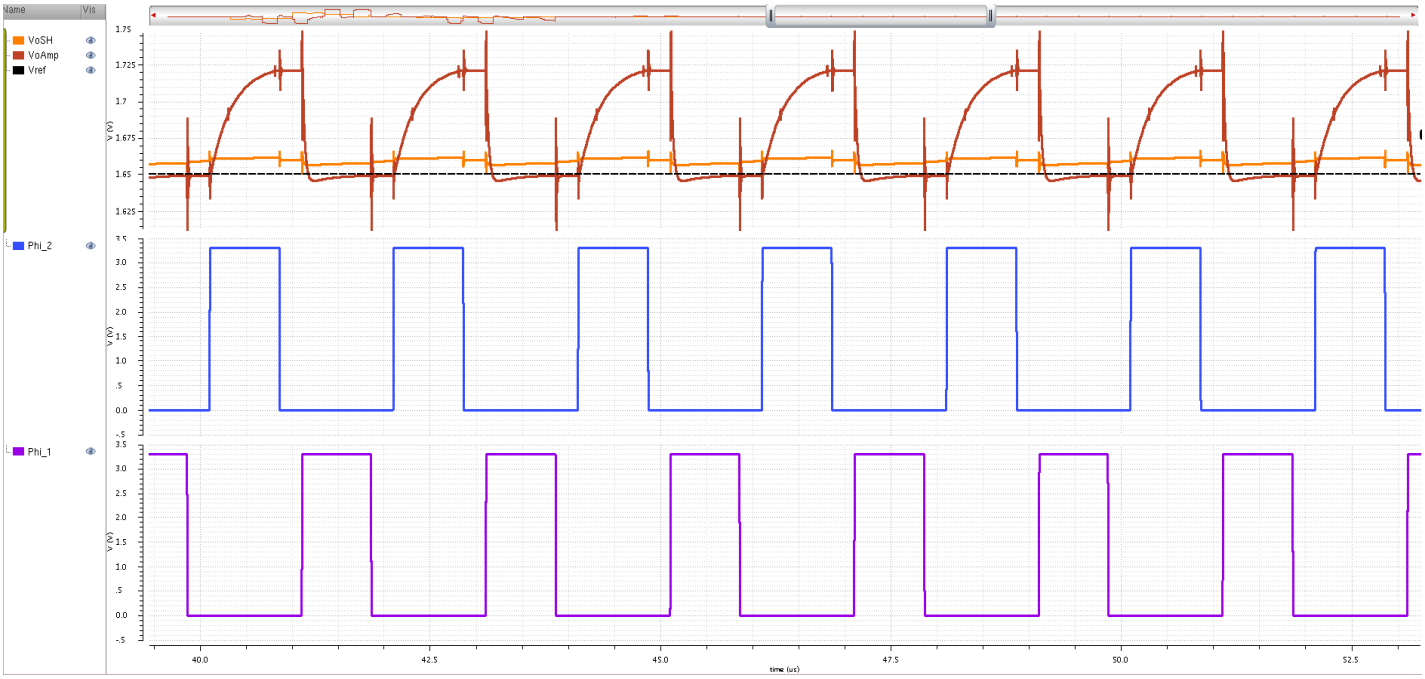

Figure 4.21. 1st stage switched capacitor amplifier simulation showing how the sample-and-hold output is sampled and amplified.

Fig. 4.21 shows the amplifier output V_{oAmp} in red, the sampled residue voltage V_{oSH} in orange, the reference voltage V_{ref} in black, and the two phase pulses Φ_1 and Φ_2 in purple and blue. V_{oSH} is sampled at 1.6578V and V_{oAmp} settles on 1.7213V. This means the residue voltage is amplified with a gain of 9.14 for this stage.

Fig. 4.22 shows the second stage amplifier output V_{oAmp2} in green, the sampled output from the previous amplifier stage V_{oSH2} in red, the reference voltage V_{ref} in black, and the two phase pulses Φ_1 and Φ_2 in purple and blue. V_{oSH2} is sampled at 1.7169V and V_{oAmp2} settles on 2.252V. This means the voltage is amplified with a gain of 9.00 for this stage.

After the two amplifier and sampling stages, the output is held and compared with a comparator and the fine CDAC. Both inputs, V_{ref2} and V_{oSH3}, are shown in Fig. 4.23 while the fine conversion output Q_f changes below.

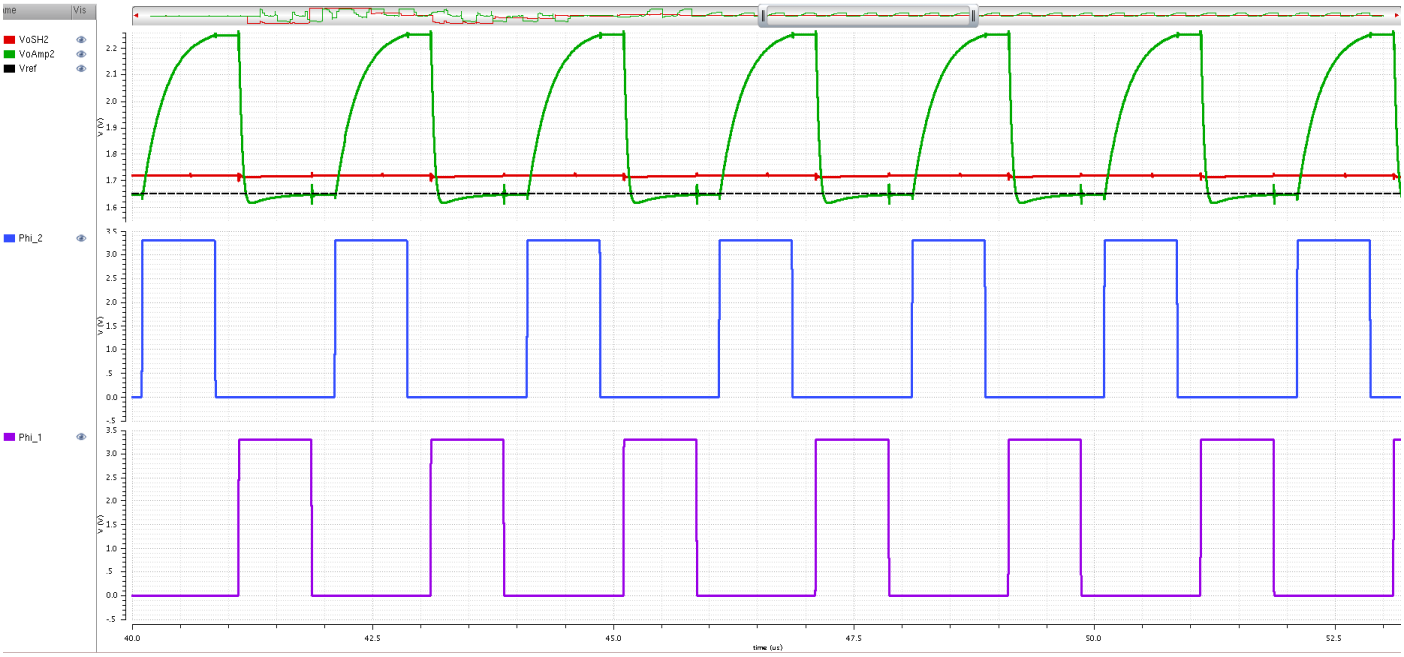

Figure 4.22. 2nd stage switched capacitor amplifier simulation how the output of the first amplification stage is sampled and amplified again.

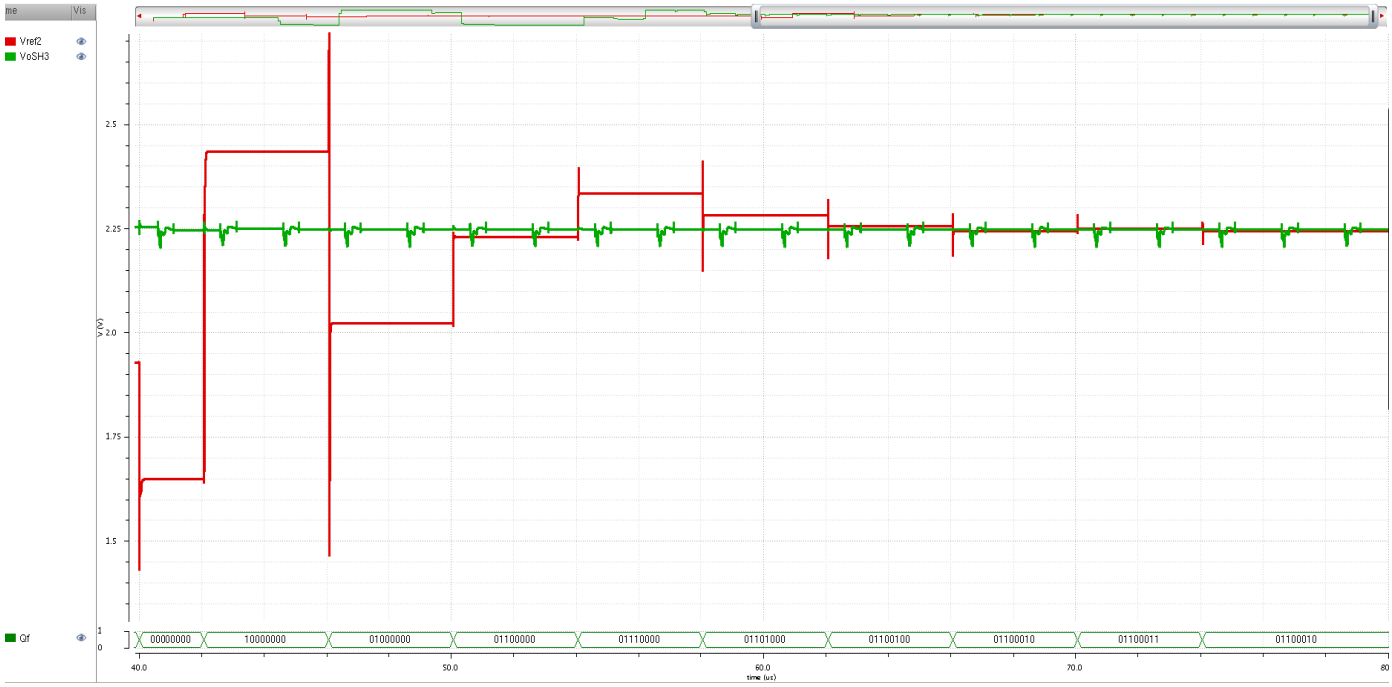

Figure 4.23. Fine conversion with the output of the final sample-and-hold stage being used as a reference for Vref2 to match with each bit in the CDAC tested and chosen (represented as Qf).

The fine conversion capacitor bank settles on the output Q_f = 01100010 or 0.98pF. The sensed capacitance can be found by using the derived equation with the coarse and fine conversion values as inputs. In this case the estimated sensed capacitance is 0.9938pF, only 6.2fF off from the actual C_{sense}. However, by taking into account an actual gain of 82.26, the final conversion becomes 0.9947pF, which is 5.4fF off. If the parasitic capacitance on V_{mid} is also taken into account, then the final conversion becomes 0.9999pF, which is approximately 100aF off. This shows that the accuracy can be improved with calibration.

4.6 Final Design

4.6.1 Individual and Differential Capable Front-end

The front end was designed to interface with 4 of the capacitor electrodes and a common electrode to perform both differential and single ended capacitance conversions. The CDAC is always connected to $\overline{\text{EXC}}$ while the electrode switches S_E and direction switches S_D are set depending on the conversion mode. For single ended conversions, the capacitor selected for conversion is set to EXC to complete the half bridge, while the other electrodes are disconnected via the corresponding S_E switches. For differential conversions, C_{Sense1} and C_{Sense2} form a half bridge together, while C_{Sense3} and C_{Sense4} form another half bridge together. This means either S_{E1} and S_{E2} or S_{E3} and S_{E4} can be on at a time. During the coarse conversion, the very first clock period is used to check which capacitor of the pair is larger and sets S_D such that the smaller capacitor is in parallel with the CDAC. In this way the coarse conversion attempts to make up the difference between the capacitors and the code output represents ΔC with S_D representing the direction. This configuration allows using the same back end circuitry for all conversion modes. The front-end circuit is shown in Fig. 4.24.

4.6.2 Non-uniform Conversion Time

The time for one conversion depends on a number of factors. The very first conversion is both a coarse and fine conversion. After, as long as the input capacitance does not exceed the fine conversion range, the next conversion performed is only a fine conversion. As such, repeated fine conversions are performed until the input changes enough to require a full coarse and fine conversion.

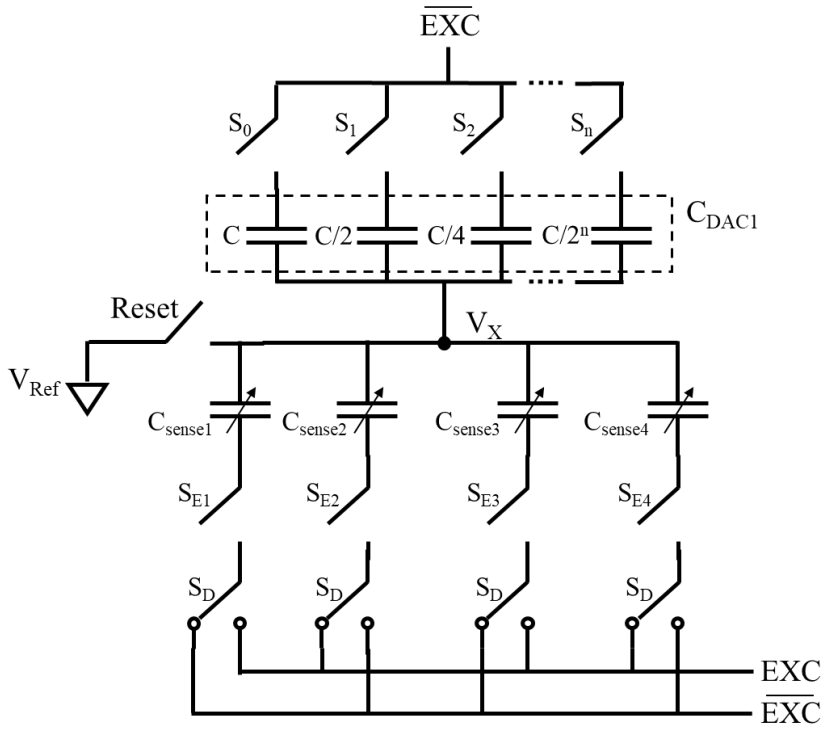

Figure 4.24. Front-end circuit showing the capability to match 4 different individual sense capacitors or differentially match either C_{sense1}-C_{sense2} or C_{sense3}-C_{sense4}.

Fig. 4.25 shows the timing diagram of a full conversion followed by just a fine conversion. The input clock is divided by 4 to generate the excitation signal. The same SAR control logic is used for the coarse and fine bits to reduce area and power. To do this, the SAR input clock, comparator output, and bit selection gets multiplexed depending on whether a coarse or fine conversion occurs. As a result, the coarse and fine bits are stored in separate registers to avoid being overwritten. The SAR clock is identical to the excitation signal during the coarse conversion and after 9 clock periods (1 period for direction check and 8 periods for CDAC comparison), the clock waits for the residue to be amplified and then switches to a faster clock speed for the fine conversion (identical to the input clock for 8 periods).

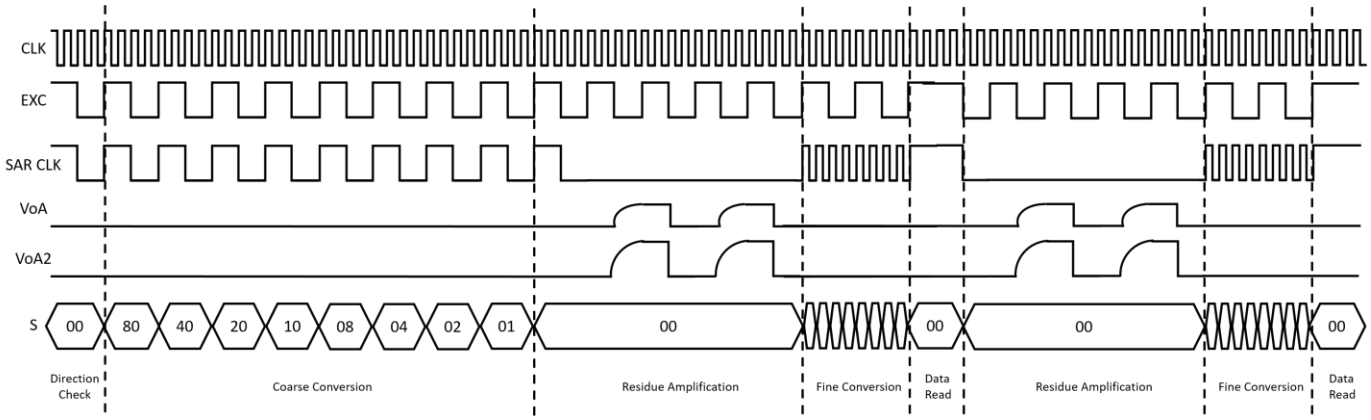

Figure 4.25. Timing diagram showing a full coarse and fine conversion followed by only a fine conversion.

All signals are then held until the data is read and acknowledged by the I^2C bus. If the fine bits are 0x00 or 0xFF, then that signals a potential out-of-range and the converter attempts another full conversion, otherwise, fine conversions are repeated. V_{oA} and V_{oA2} represent the output voltage of the first and second amplification stages, respectively.

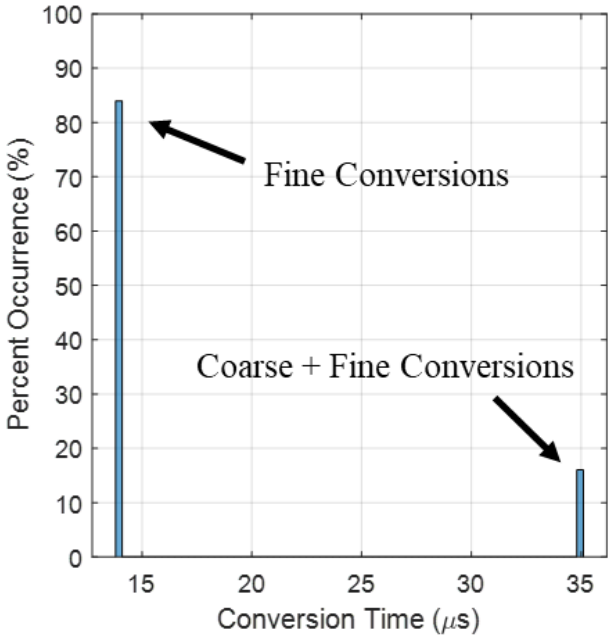

Figure 4.26. Histogram of conversion time test data showing percent occurrence of full coarse and fine conversions and just fine conversions.

4.6.3 Digital Circuits and Features

The digital circuits were implemented by synthesizing Verilog HDL code using an RTL compiler. Then, the layout was created by using Cadence Encounter Place & Route software. The digital circuit block is in charge of four main functions: I^2C readout, SAR control logic, clock signal generation, and mode select.

4.6.3.1 I^2C Readout

The I^2C readout was implemented by modifying an I^2C slave core written in Verilog [35]. It is used to read from and write to the chip and reduce the pins needed for communication to just two (SDA and SCL). This two wire bus supports up to 128 unique 7-bit addresses. The code was modified to allow the I^2C address to be defined by wires off-chip. For this implementation, the 7-bit address was defined as 00011XX, where XX are the last 2 bits pinned out. This allows for 4 separate addresses to be defined. Additionally, separate registers were created for the read data and the write data. The write data is stored as the mode select value, while the read data is the converter data to be read. The last change was detecting and passing an acknowledge flag when the first byte of data is read so that the second byte can be selected.

Using this design allows the readout speed to be set by however fast the SCL line can be driven. This was important since slower communication speed would limit the speed that conversions could be read out. The SCL line speed was set to 2.2MHz by a Teensy 4.0 microcontroller. Since this is not a standard selectable speed, the Wire library was modified to allow for the higher communication rate. With the higher speed, smaller pullup resistors had to be used to reset the line fast enough.

4.6.3.2 SAR Logic

The SAR control logic determines which capacitors of the CDAC to keep during a conversion by checking each bit. The SAR logic was written in such a way to use a single control logic block and simply multiplex the conversion bits depending on the conversion phase. When a coarse conversion is occurring, signal S stays low to allow the comparator from the coarse stage to reach the control logic. When the coarse conversion is complete, S goes high and the faster clock Clock2 is passed to the control logic. This approach reduces area since each conversion phase no longer has its own dedicated control logic, like in the preliminary design.

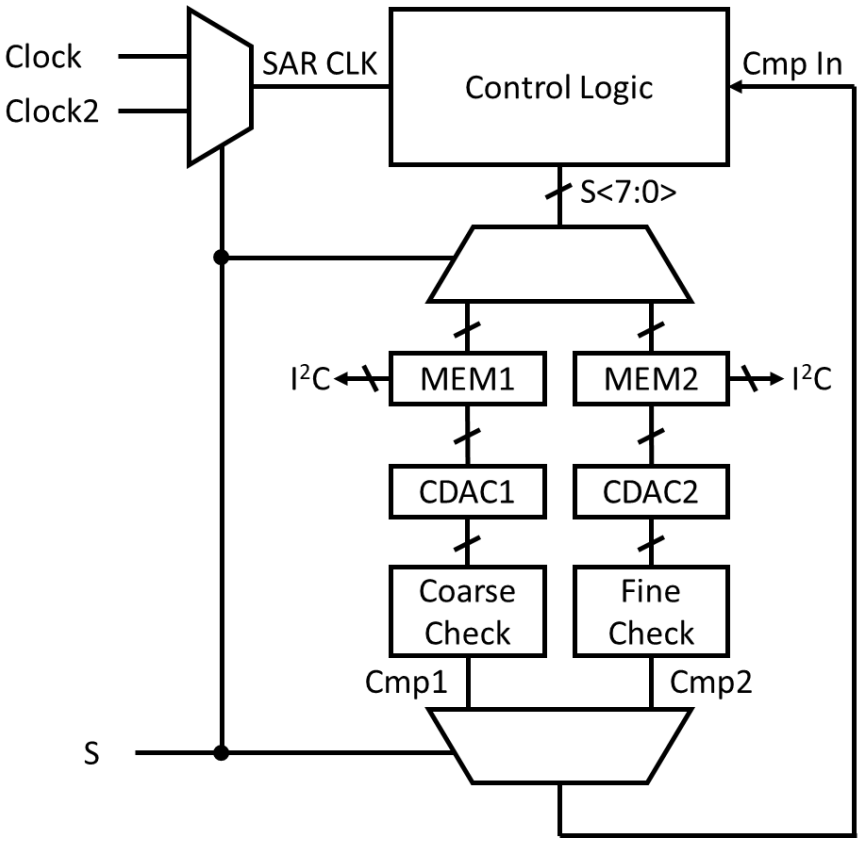

Figure 4.27. SAR logic representation showing how only one control logic circuit is necessary if multiplexed between coarse and fine conversions.

4.6.3.3 Clock Signals

The clock signals generated set the timing for the sample and hold, switched capacitor amplifiers, reset, SAR coarse and fine clocks, and excitation signals. The control signals for the switched capacitor amplifiers were passed through a non-overlapping clock circuit presented in Fig. 4.28. The circuit works by generating two complementary clock signals that have a time delay between them. The delay was created by placing a capacitor to charge/discharge between logic gates. Having non-overlapping signals ensure that glitches don't occur when the amplifier switches between phases.

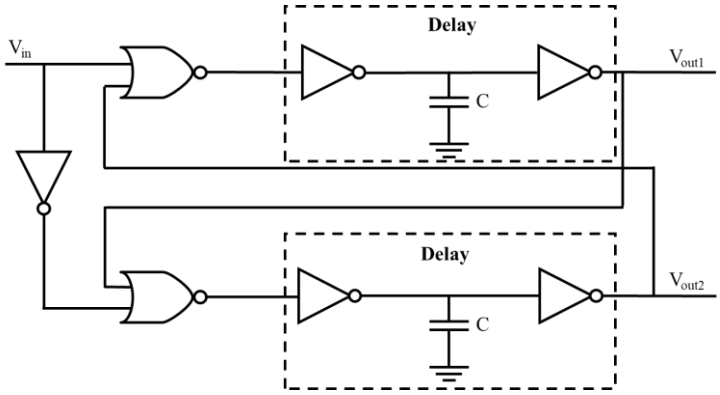

Figure 4.28. Non-overlapping clock circuit using a latch with delays to ensure the logic transitions at Vout1 and Vout2 do not coincide.

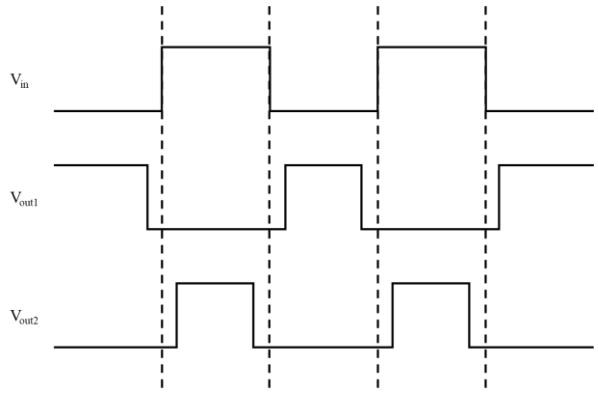

Figure 4.29. Non-overlapping clock signals showing an example of the edge transitions for Vout1 and Vout2 with a given Vin signal.

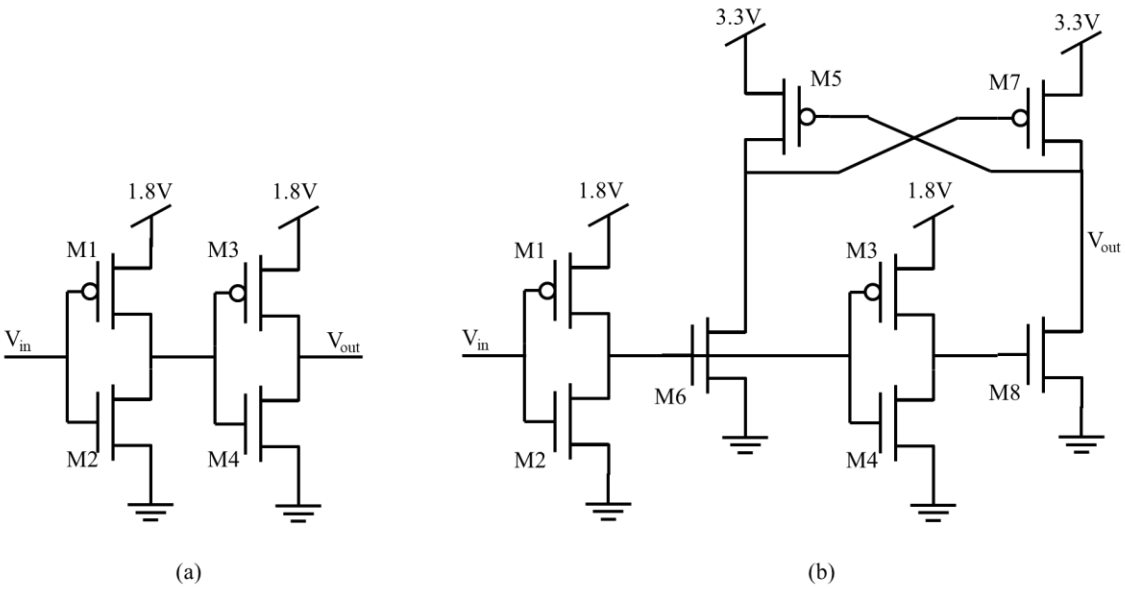

Figure 4.30. Level shift circuit showing the two inverters with lower voltage rail to shift down and two inverters with intermediate pullup structures at higher voltage rail to shift up: (a) Shift down circuit; (b) Shift up circuit.

TABLE I

LEVEL SHIFT TRANSISTOR SIZING

Device	M1, M3	M2, M4	M5, M7	M6, M8
W/L	3.6/0.3	1.4/0.35	2.0/0.3	4.0/0.35

The analog and digital circuits operate at different voltages on-chip. As such, level shifting circuits are necessary for any signals that communicate between the digital block and the rest of the circuit. For example, the output from the comparators need to be shifted down before being input to the SAR logic. Also, all control signals from the digital block need to be shifted up before controlling any transmission gates in the rest of the circuit. The circuits are shown in Fig. 4.30.

The down shifting circuit simply uses two inverters with the source of the PMOS transistors connected to 1.8V. This allows the output to follow the input signal with a maximum value of 1.8V for safe interaction with the digital circuits. The up shifting circuit uses a cross coupled pair of PMOS transistors connected to 3.3V and NMOS transistors driven by the lower voltage signal through inverter buffers to create an adequate driving signal at the output.

4.6.3.4 Mode Select

The mode select allows for eight different conversion options and two test options and is selected by writing to the device via I^2C. The test options use an on-chip 9-bit test DAC as an input to the converter. The test DAC can also be set to ground for measurement and calibration. The test DAC was designed with a 6.3fF LSB and a full-scale capacitance of 3.22pF.

TABLE II

MODE SELECT OPTIONS

Mode	Description
0	Switch between differential E1/E2 and differential E3/E4
1	Cycle through single-ended E1-E4
2 (default)	Differential E1/E2
3	Differential E3/E4
4	Single-ended E1
5	Single-ended E2
6	Single-ended E3
7	Single-ended E4
8-13	Not Used
14	Test DAC input
15	Test DAC measurement

Chapter 5

Measurement Results

5.1 Introduction

The performance was characterized with a few different approaches. The first approach uses an on-chip test DAC to perform a linear capacitance sweep. Then, to be able to more carefully see output code transitions, a refined sweep is performed using an applied voltage emulating a change in capacitance. Finally, these two measured results were compared to the simulation results of a sweeping input capacitance. Additionally, the effect of applying off chip offset capacitors is investigated.

To analyze the performance under dynamic conditions, the test DAC was used to create a sinusoidal input signal with varying signal amplitude and frequencies. A heat map was created for these results at 1MHz and overclocked at 2MHz input clock frequencies.

The final testing examples show the preliminary and final designs tested with actual capacitance sensors. The preliminary design was tested with a capacitance strain sensor while the final design is tested at high speeds with a propeller variable capacitor device.

5.2 Input Sweep

Before using the test DAC as an input device to the converter, it needed to be characterized. The test DAC was put in measurement mode and each capacitor in the DAC was measured individually. The measurement was performed by applying a step voltage through a known resistor in series with the test DAC in an RC configuration and measuring the rise time to infer the capacitance.

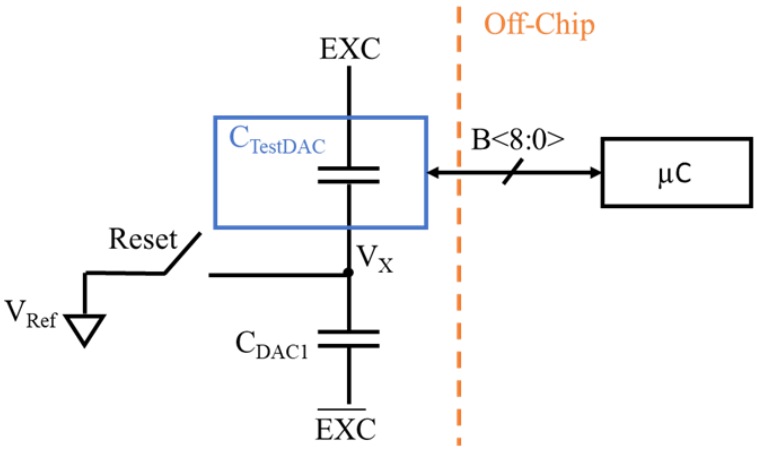

Figure 5.1. Test DAC setup internally as input to converter front-end with switches being driven by off-chip microcontroller.

Once measured, the test DAC was used to apply a sweeping input to the converter with each bit of the DAC being controlled by a Teensy 3.2 microcontroller. The test DAC uses 9 bits with a designed LSB capacitance of 6.3fF and full scale capacitance of 3.22pF. An example of the output is shown in Fig. 5.2.

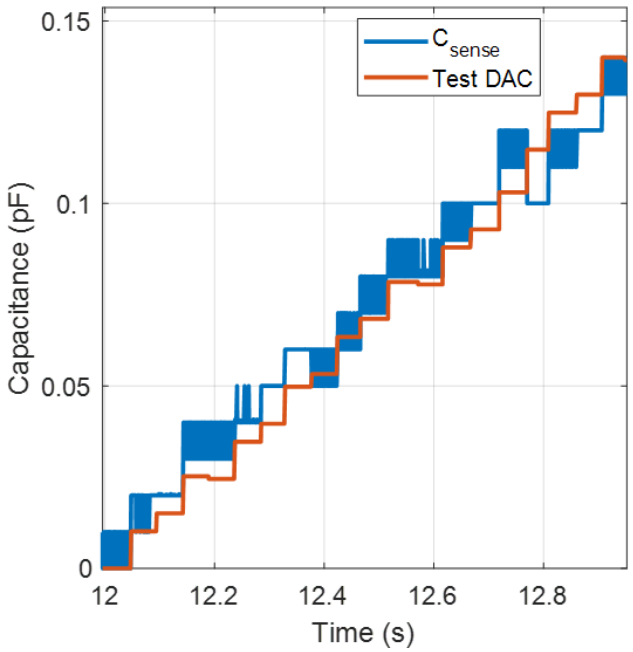

Figure 5.2. Example data of test DAC input and sensed capacitance output during linear sweep.

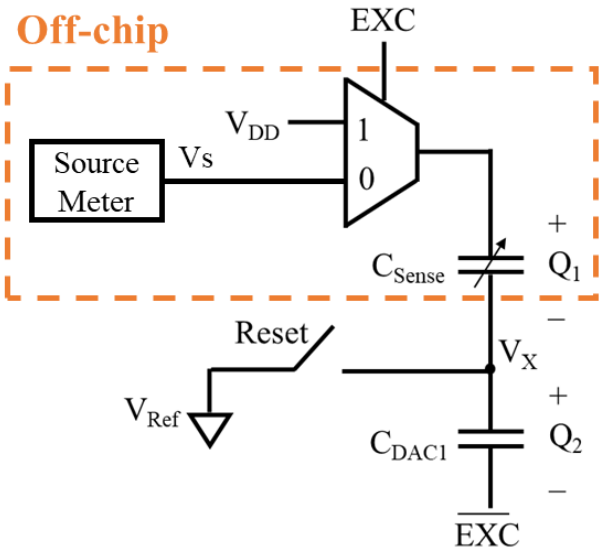

Figure 5.3. Front-end circuit for voltage sweep input capacitance emulation showing the off-chip setup using an analog multiplexer to switch between the source meter voltage and VDD. The excitation signal controls the multiplexer instead of driving the sense capacitor directly.

To emulate a more refined changing capacitance input, a sweep voltage is applied to a 2pF capacitor. The voltage was swept from 0 to 3.3V at 40uV steps which translates to approximately 24aF steps. The sweep voltage was supplied by a Keithley 2400 source meter and passed through a CD4051B analog multiplexer. Fig. 5.3 shows the circuit and how this was implemented for the single ended case.

$$V_X = V_{Ref} + \frac{C_{Sense0} - C_{DAC1}}{C_{Sense0} + C_{DAC1}} V_{DD} - \frac{C_{Sense0}}{C_{Sense0} + C_{DAC1}} V_S \quad (5.1)$$

Where the input capacitor C_{Sense0} = 2pF and the emulated capacitance C_{Sense} is found with Eq. 5.2.

$$C_{Sense} = \frac{V_{DD} - V_{Ref} + V_X}{V_{DD} + V_{Ref} - V_X} C_{DAC1} \quad (5.2)$$

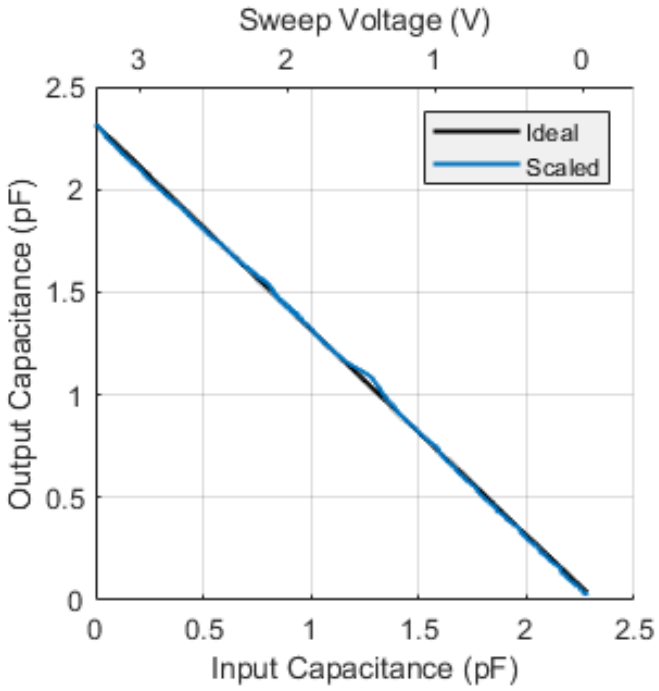

Figure 5.4. Output capacitance versus emulated input capacitance showing the linearity across the voltage sweep range compared to the expected line. The output is scaled by removing offset and gain errors.

The following data was collected with the converter in differential mode which is similar to the approach shown in Fig. 5.3. Fig. 5.4 shows the emulated capacitance for an applied sweep voltage and corresponding output capacitance.

The output is scaled to follow along the ideal or expected relationship curve before determining the DNL and INL performance. Since multiple conversions occur during each voltage step, the average is used to compare to the expected value. The maximum DNL and INL, using this approach, is found to be 11.4 LSB and 276 LSB, respectively. The mean and standard deviation of the DNL is 0.02 LSB and 2.1 LSB. The mean and standard deviation of the INL is 1.5 LSB and 73 LSB. The linearity for this design is influenced by physical mismatches in the CDAC and variations in gain that scales the fine bits.

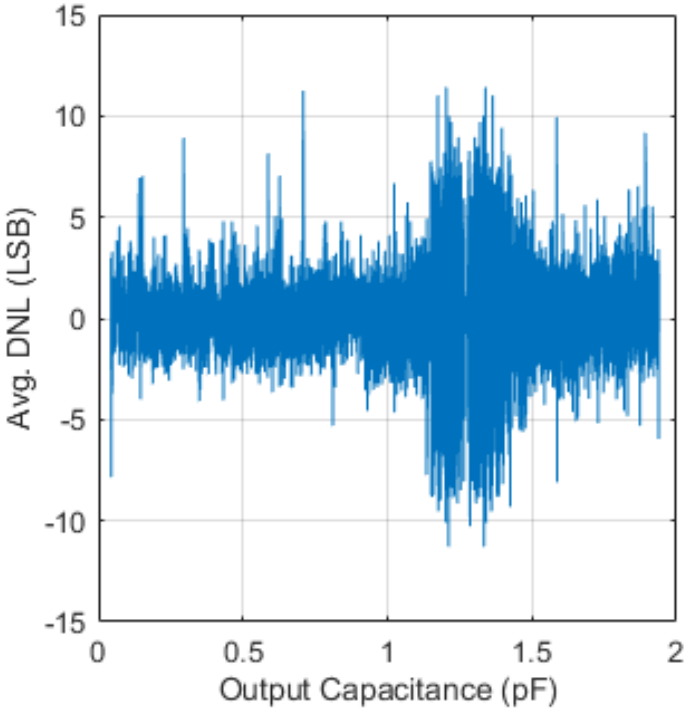

Figure 5.5. Average DNL for emulated input capacitance sweep showing the difference between the measured step width and the ideal value of 1LSB.

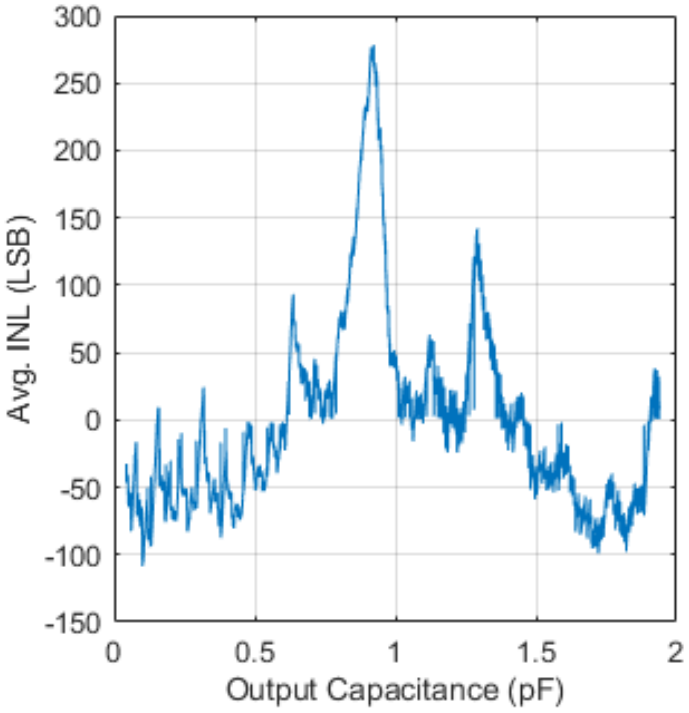

Figure 5.6. Average INL for emulated input capacitance sweep showing the deviation, in LSB, of the measured conversion from the ideal or expected line.

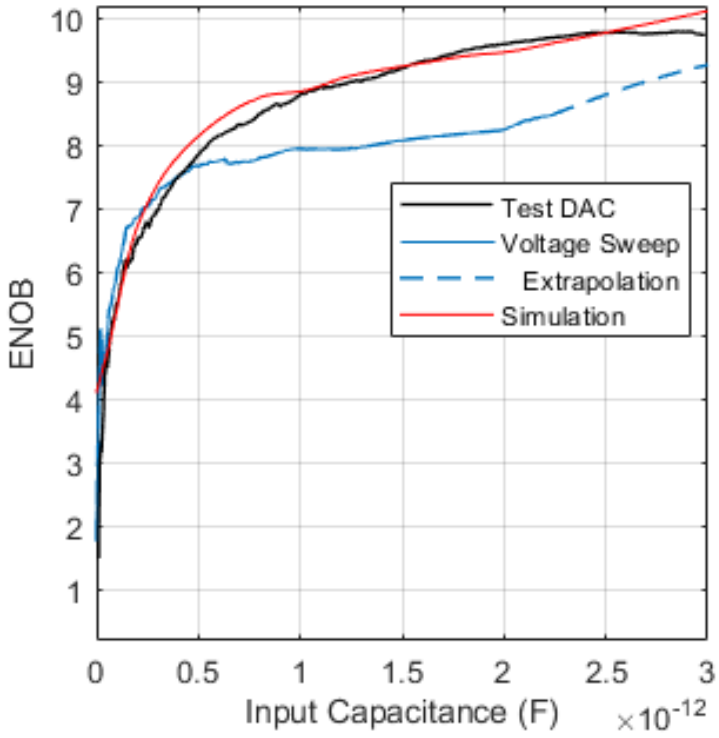

Figure 5.7. ENOB versus input capacitance comparing test DAC, voltage sweep, and simulation data. The voltage sweep does not cover the whole converter range and is extrapolated.

The results of the test DAC input is compared to the emulated capacitance approach and the simulation results in Fig. 5.7. A maximum of 9.8 ENOB occurs for the test DAC input and 9.2 ENOB for the voltage sweep input at 2.92pF input capacitance. The simulation results indicate a predicted 10 ENOB for the same input capacitance. The resolution was defined by looking at the standard deviation at each capacitance input and multiplying it by square root of 12 which approximates an LSB quantization.

$$ENOB = log_2\left(\frac{Cin}{\sqrt[2]{12}\,\sigma}\right) \quad (5.\ 3)$$

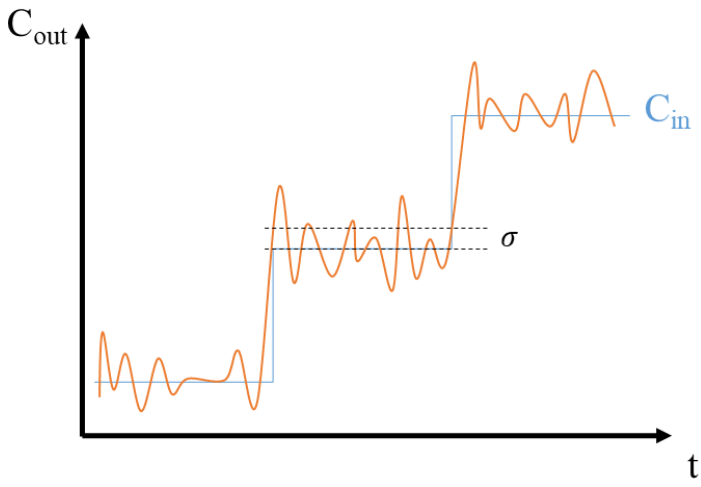

Figure 5.8. Example of how the capacitance resolution is measured for linear sweep experiments. The standard deviation is found at each input capacitance value during the sweep.

5.3 Offset Capability

Although the input range is limited to about 3pF, we look at the effect of offsetting this range by using off-chip capacitors. Fig. 5.9 shows how the ENOB is affected by 1pF, 2pF, and 10pF off-chip capacitor offsets. The capacitance resolution was again found by looking at the standard deviation at different points along the converter input range described in Fig. 5.8. The performance is degraded mainly due to slew rate limitations of the front-end at the designed operating speed.

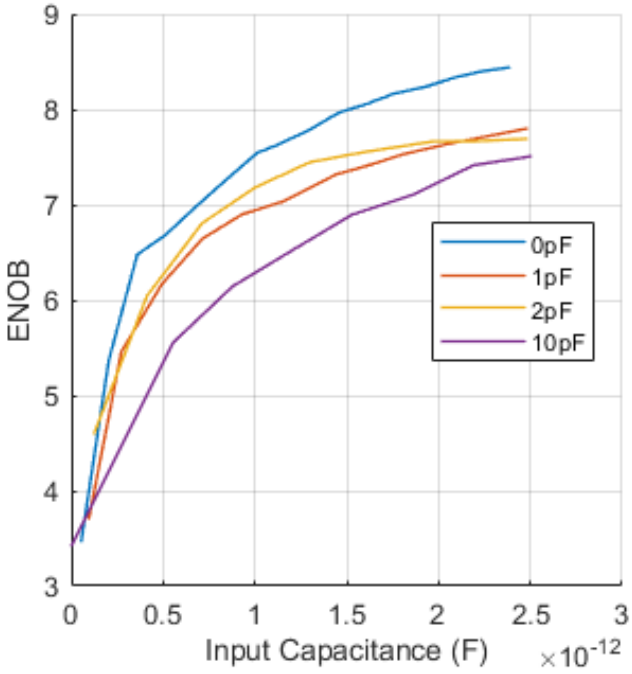

Figure 5.9. ENOB versus input capacitance showing the reduction in performance for different off-chip capacitor offsets.

5.4 Dynamic Testing

The test DAC was used to generate a sinusoidal input capacitance. The SNR for a sinusoidal input is defined below. A heat map was created for varying input signal frequencies and amplitudes at two different input clock frequencies. The ENOB definition is adjusted to account for the varying amplitude. The results indicate better performance at smaller amplitudes and lower input frequencies. Additionally, Fig. 5.11 reveals the tradeoff in performance for overclocking the input clock frequency to 2MHz.

$$SNR = 20\log_{10}\left(\frac{Input\ Amplitude/\sqrt{2}}{RMS\ Resolution}\right) \tag{5. 4}$$

$$ENOB = \frac{SNR - 1.76 + 20\log_{10}\left(\frac{Maximum\ Amplitude}{Input\ Amplitude}\right)}{6.02} \tag{5. 5}$$

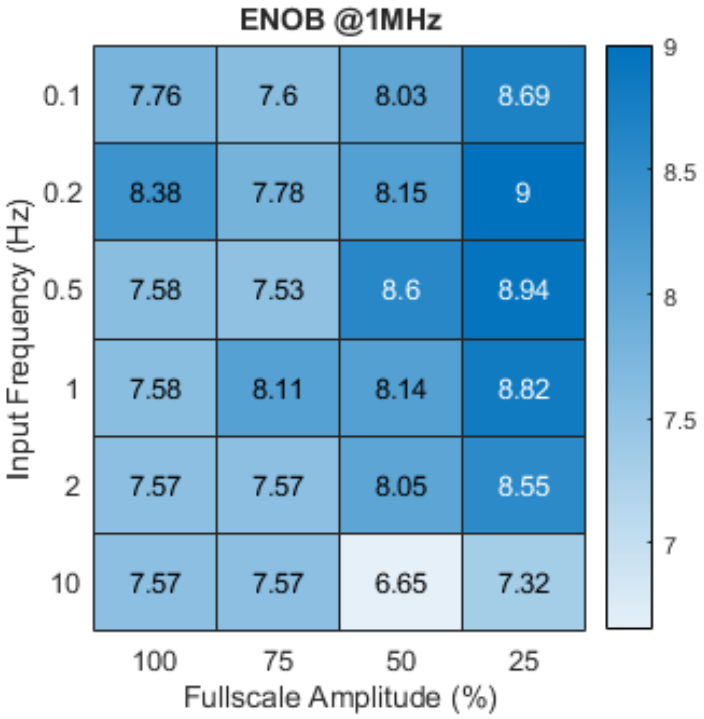

Figure 5.10. ENOB heat map for sine wave input at 1MHz input clock frequency showing best performance occurring at smaller input signal amplitudes and frequencies.

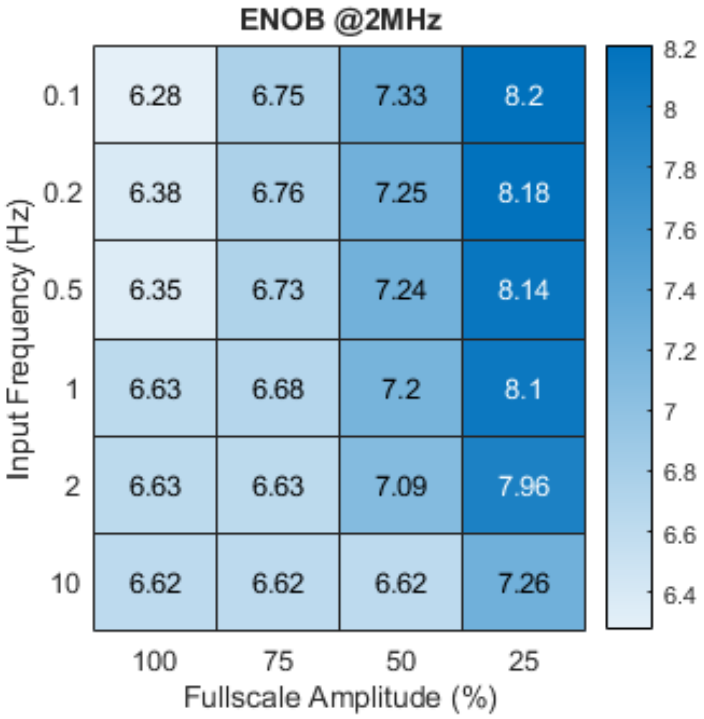

Figure 5.11. ENOB heat map for sine wave input overclocked at 2MHz input clock frequency showing best performance occurring at smaller input signal amplitudes and frequencies.

5.5 Sensor Testing

5.5.1 Preliminary Design

The preliminary design was tested with a capacitive strain sensor shown in Fig. 5.12. The sensor was provided by the same group who designed and fabricated it in [13]. For this test, the sensor was stretched and released, by hand, multiple times under a microscope. When the sensor is at rest (t = 0s), the sensed capacitance is stable at about 1.9pF. Then, when the sensor is stretched (t = 8.4s), the sensed capacitance decreases to about 1.2pF.

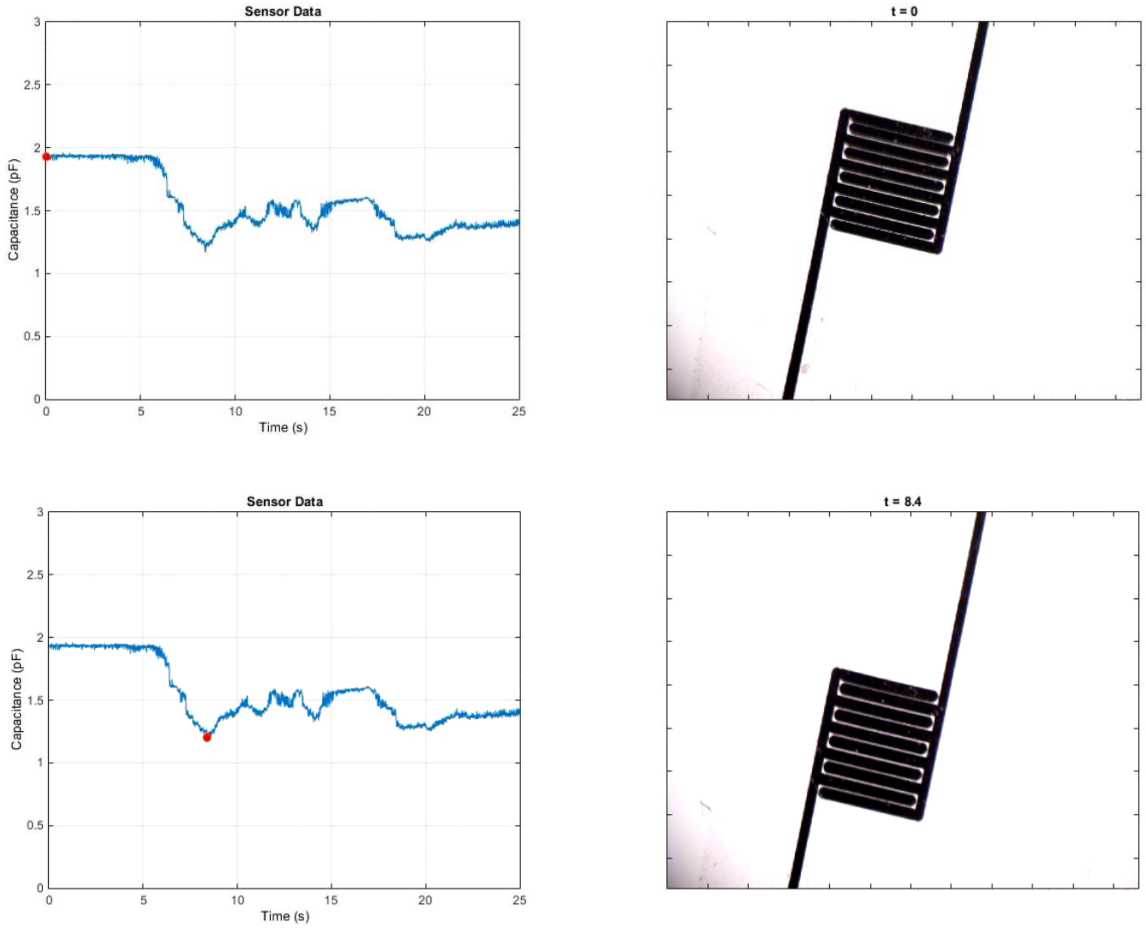

Figure 5.12. Capacitance output with capacitive strain sensor manually stretched showing how an increase in gap distance between the comb fingers reduces the overall capacitance.

5.5.2 Final Design

While many CDCs boast high conversion rates, all reported test results have been done using devices operating at 100Hz or slower. To test the converter with a device that varies at higher speeds, a variable capacitor was created using a 7mm DC coreless motor. An aluminum foil sleeve was placed around the motor and propeller with a threaded wire brushing against it to form one of the electrodes. The other electrode was fixed 1cm away and formed a 5mm gap with the propeller. The result is an area changing variable capacitor.

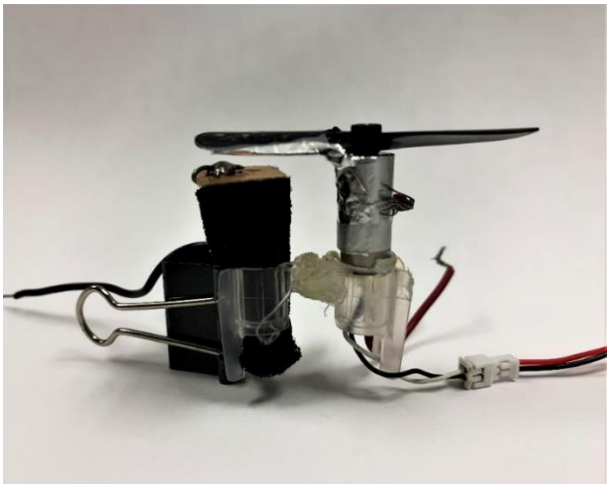

Figure 5.13. Photo of assembled propeller variable capacitor prototype with aluminum foil sleeve electrode over propeller and motor.

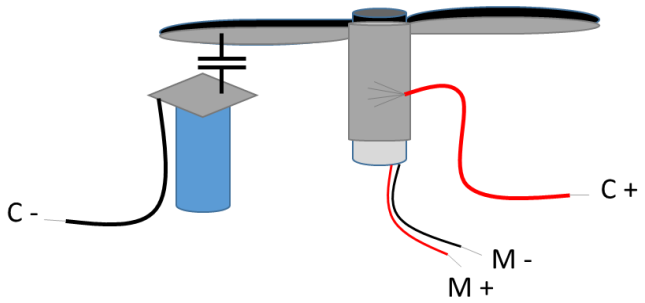

Figure 5.14. Illustration of propeller variable capacitance device with aluminum foil sleeve electrode over propeller and motor. A threaded wire makes contact with the foil over the motor.

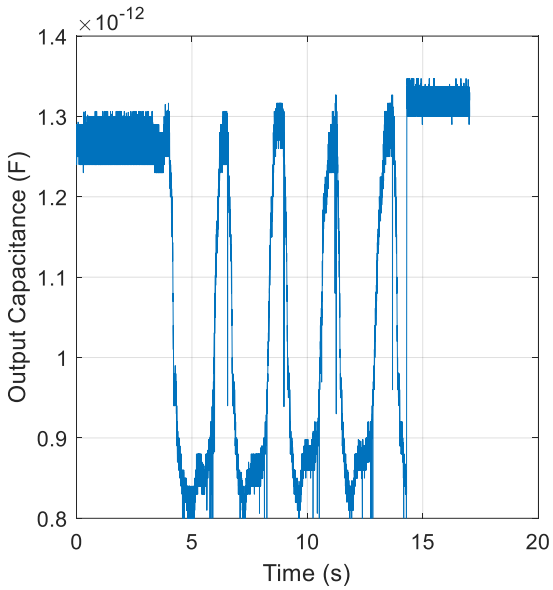

Figure 5.15. Control experiment where propeller is manually rotated to ensure capacitance variation is a result of electrode overlap and not a confounding factor.

Fig. 5.15 shows the control experiment where propeller is manually rotated so as to demonstrate the capacitance shift without the potential of EM interference caused by actuating the motor. In both the control experiment and the dynamic experiments, the peak-to-peak amplitude of the capacitance is approximately 500fF.

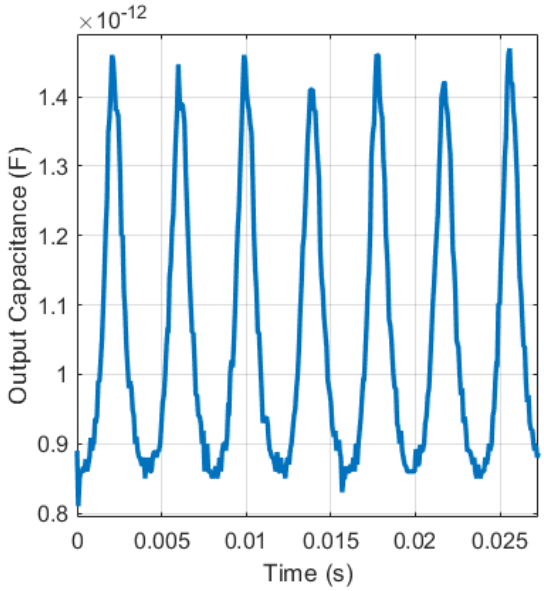

Figure 5.16. Output capacitance of propeller variable capacitor rotating at 234Hz. The continuous contact with foil produces a sinusoidal output.

Above around 400Hz, the aluminum sleeve fails due to the friction of the brushing wire. A modified design was created with the wire making contact with the propeller as it rotates. The advantage is now the speed could be increased. The disadvantage is there no longer is continuous contact, but instead brief contact as the propeller passes over the other electrode. The result is a more pulse-like behavior.

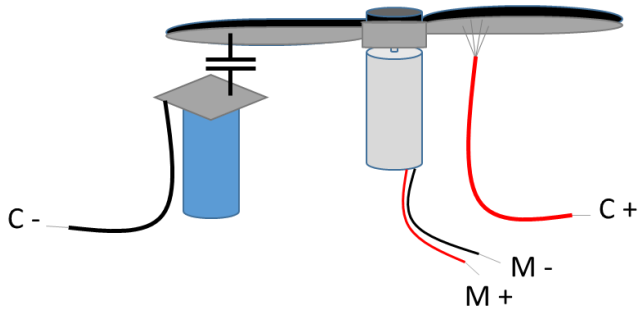

Figure 5.17. Illustration of propeller variable capacitance device with aluminum foil sleeve electrode only over propeller. A threaded wire makes contact with the foil over the propeller.

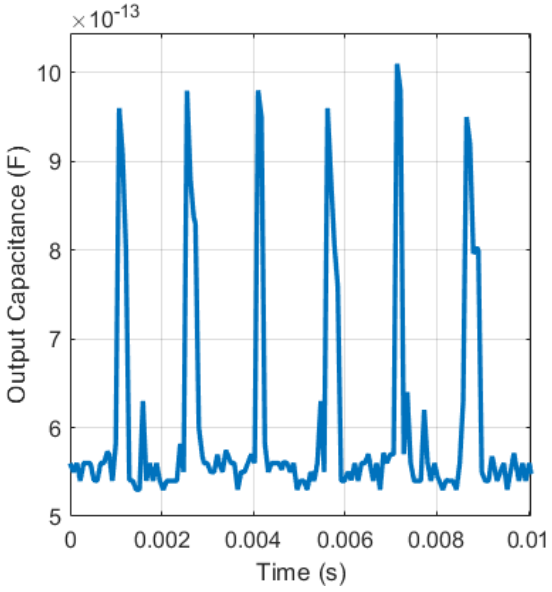

Figure 5.18. Output capacitance of propeller variable capacitor rotating at 656Hz. The non-continuous contact with foil produces a pulsed output.

The results of the propeller variable capacitor are compared with the few reported test results. Also, the test DAC results from section 5.4 were added. From Fig. 5.19, we see a drop in performance for increasing sensor input frequency.

TABLE III

DEMONSTRATED TEST PERFORMANCE SUMMARY

	[22]	[23]	[26]	[28]	**TestDAC**			**Propeller**	
ENOB (bits)	8.8	18.1	10.6	8.9	9	8.8	7.3	6.7	5.2
Input Frequency (Hz)	100	0.015	0.004	0.0016	0.2	1	10	234	656

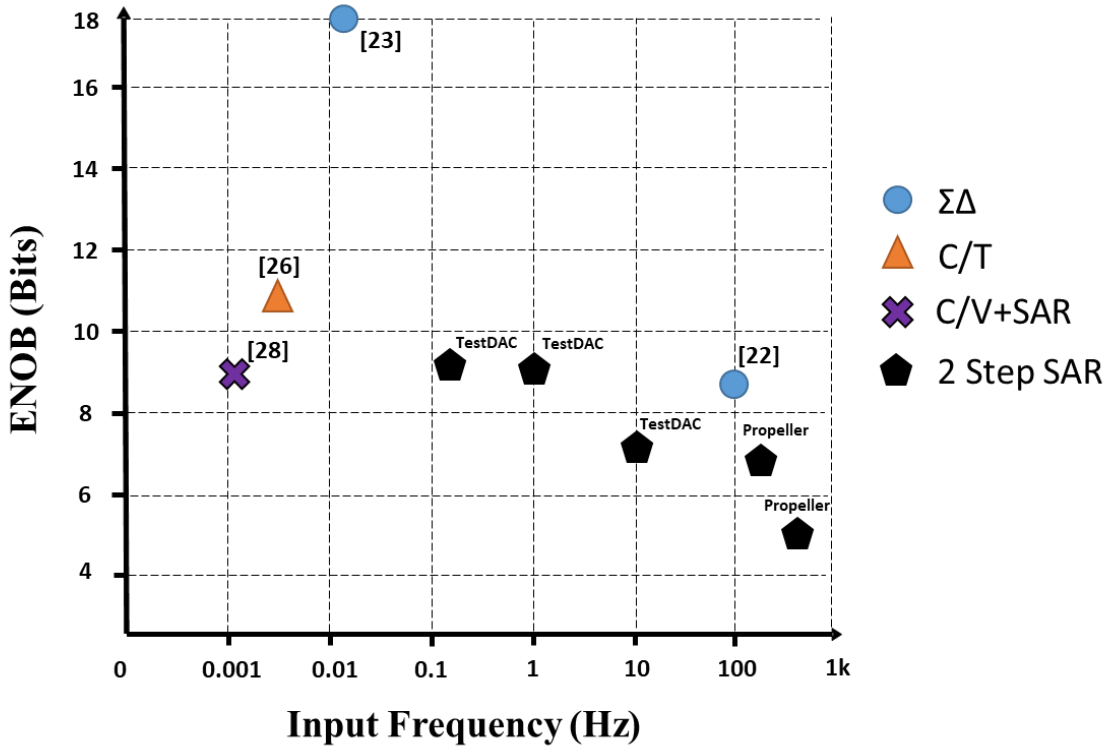

Figure 5.19. Tested sensor resolution versus input frequency summary including test DAC and propeller device results. The reduction in performance is shown as the input frequency increases.

Chapter 6

Conclusion

6.1 Summary

SAR CDCs have the fastest conversion speeds, but their resolution is limited by the smallest physical capacitor in the CDAC. A two-step SAR approach is presented which increases the effective resolution while maintaining speed capability with repeated fine conversions. A non-uniform timing scheme is implemented to improve conversion rates and not waste time and power on redundancy. Finally, the I^2C interface was included on the chip along with the clock signals and reference voltages that drive the different stages, to reduce the number of off-chip wires and signals.

The preliminary design was proposed and implemented as a proof of concept which resulted in a 9.2 ENOB and 6.25kHz conversion speed. The final design further improved this to 9.8 ENOB and 15.6kHz conversion speed for full conversions or 35.7kHz for repeated fine conversions. When overclocked, this results in 8.2 ENOB and 31.2kHz conversion speed for full conversions or 71.4kHz for repeated fine conversions.

6.2 Comparison to State of the Art

The testing results for the fabricated chips are compared to other CDC architectures. Table IV summarizes the preliminary and final results compared to the state-of-the-art, while Fig. 6.1 visually compares the effective resolution and conversion rate.

From this comparison we see that this work outperforms all but two other works in ENOB throughput (FoM2). It should be noted that having a large capacitance range is

an important factor for a larger calculated SNR and this work has among the smallest reported ranges. If the range were increased by two bits in the coarse conversion, then the input range would increase to about 11.6pF and the effective resolution to 11.8 ENOB. With two additional bits, the conversion time would increase to 72μs for full conversions but stay at 28μs for repeated fine conversions.

The figure-of-merit (FoM) is calculated using Eq. 6.1, where P is the power consumption, T_{conv} is the conversion time, and R_{eff} is the effective resolution in bits.

$$FoM = \frac{P \times T_{conv}}{2^{R_{eff}}} \tag{6. 1}$$

The effective resolution is found using the signal-to-noise ratio (SNR) calculated by Eq. 6.3, where the absolute resolution is the root-mean square capacitance resolution.

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{6. 2}$$

$$SNR = 20 \log_{10} \left(\frac{Capacitance\ Range / 2\sqrt{2}}{RMS\ Resolution} \right) \tag{6. 3}$$

For comparison of resolution and speed, we define another figure of merit also referred to as ENOB throughput.

$$FoM2 = \frac{ENOB}{Conversion\ Time} \tag{6. 4}$$

TABLE IV

PERFORMANCE SUMMARY AND COMPARISON

	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	**Prelim. Work**	**Final Work**
Architecture	ΣΔ	ΣΔ	ΣΔ	ΣΔ	C/T	C/T	C/T	PLL	C/V+ SAR	SAR+ΣΔ	SAR	SAR	2 Step SAR	2 Step SAR
Output format	Digital code	Bit stream	Bit stream	Bit stream	Digital code	Digital code	PM	Digital code	Digital code	Digital code	Digital code	Digital code	Digital code	Digital code
Technology (nm)	N/R	160	350	350	90	180	160	130	180	180	180	180	500	180
Area (mm^2)	N/R	0.28	2.6	0.65	0.3	0.1	0.05	0.0725	0.49	0.46	0.1	0.2	0.9	0.43
Supply Voltage (V)	3.3	1.2	3.3	3	0.6 & 1	0.6 & 1.2	1	0.3	0.9 & 1.2	1.4	0.9 & 1	0.8 & 1.2	3.3	1.8 & 3.3
Power (µW)	2,300	10.3	14,900	60,000	5.5	0.11	14	270,000	0.16	33.7	3.84	6.44	9,830	15,129
Conv. Time (µs)	11,000	800	20	1,000,000	640	6,400	210	1,000	4,000	230	42.5	16	160	64/28[a] (32/14)[b]
Cap. Range (pF)	8.19	0.52	0.1	1	4	25.4	8	0.3	10	24	16.14	12.66	2.57	2.9
RMS Resolution (fFrms)	0.04	0.07	0.065	0.001	4.5	8.7	1.4	3.57	6	0.16	1.3	1.2	1.3	0.93
ENOB (bit)	15.8	11.1	8.8	18.1	8	9.7	10.6	6.1	8.9	15.4	11.8	11.6	9.2	9.8 (8.2)[b]
FoM (pJ/step)	428	3.76	670	207,000	13.8	0.846	1.87	3.936	1.33	0.179	0.046	0.033	2,700	475
FoM2 (kbit/s)	1.4	13.8	440	18.1	12.5	1.5	50	6.1	2.2	67	277	725	57.5	150/350[a] (256/585)[b]

C/V: Capacitance-to-voltage, C/T: Capacitance-to-time, PM: Period modulation, PLL: Phase-locked loop, N/R: Not reported.
a Full Conversion/Only Fine Conversion
b Overclocked

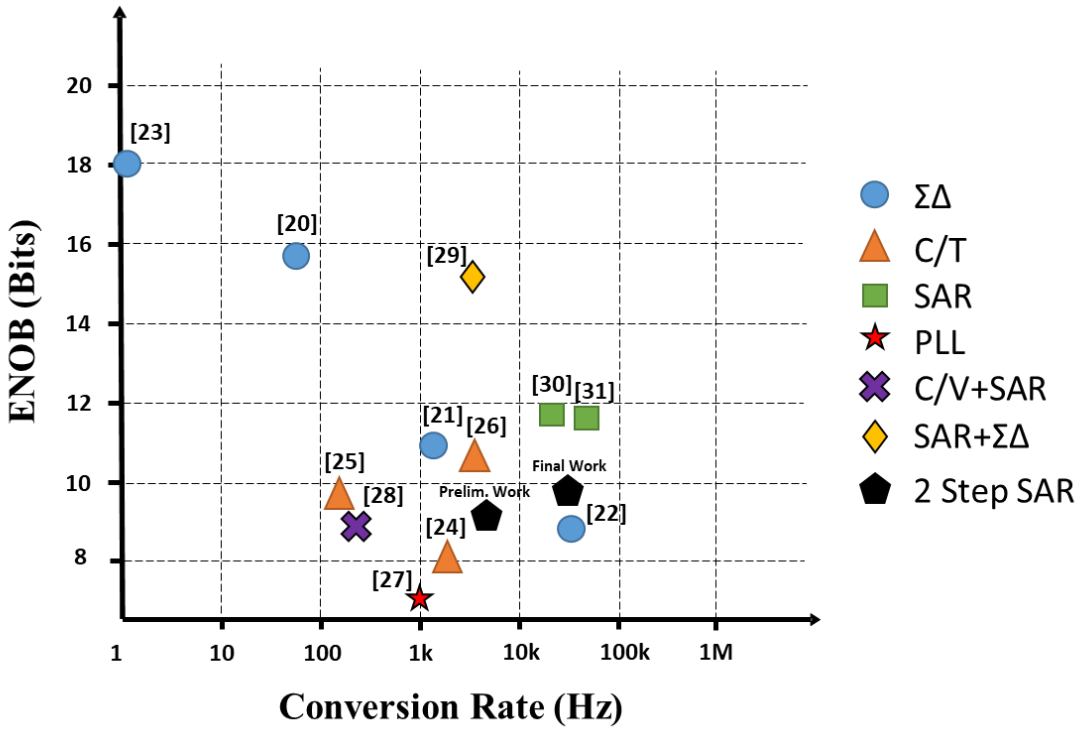

Figure 6.1. CDC resolution versus conversion rate comparison showing the state of the art for different architectures including this work.

6.3 Future Work

The design presented leaves room for further improvement by implementing offset cancelation techniques.

As previously demonstrated, the offset voltage significantly reduces the achievable resolution when left unrestrained. Offset cancellation techniques have shown to reduce offset voltage to values on the order of µV and even remove 1/f noise [36] [37]. A simple passive technique to reduce offset is by using trimming. Trimming involves measuring the offset and using simple circuitry such as a resistor divider to adjust the offset. More complex dynamic techniques include autozeroing and chopper stabilization. Autozeroing samples the offset during one clock phase and then subtracts it for input

signal in the following phase. Chopper stabilization is a modulation technique which translates the signal to an out-of-band frequency and then demodulates back to DC. The noise and offset are modulated to harmonics of the chopping frequency which can be filtered out by a low pass filter.

Additionally, interfacing and testing the circuit with other capacitive sensors for applications where both speed and resolution is critical can be explored. Examples of such applications are described in the next section.

6.4 Applications

6.4.1 Distributed Airflow Sensing on a Batwing

Biological sensory systems are often exquisitely sensitive and robust, and many researchers have developed successful artificial sensors by mimicking natural systems [38] [39]. One class of such sensors is the hair sensor. The field has been inspired by examples in biology, such as the lateral line system of fish and cercal system of crickets. The motivation of developing an artificial equivalent is to gain further understanding of the function these sensor systems serve from a biological perspective and to further improve manmade systems and technologies from an engineering perspective. The challenge, however, is to replicate the properties of these sophisticated mechanical sensors and incorporate them easily for applications such as inertial or flow sensing on small unmanned aerial vehicles (UAVs) to support flight control.

Bats are uniquely the only known mammals capable of sustained flight. They are exceptionally agile flyers and have developed specialized sensors that provide aerodynamic feedback for flight control. In particular, hair sensors are implemented as microscopic hairs distributed over the bat's wing with each one surrounded by a ring of

tactile receptors. This allows them to measure airflow as slow as 2-3cm/s in a directionally sensitive manner. It is believed that these bat hair sensors are specialized to monitor flight speed and airflow conditions that indicate stall [40]. This allows them to fly at slower airspeeds, thereby allowing for tighter turns and increased maneuverability. This work could be applied to learn from natural sensors, such as those found on bats, by designing a sensor system that can collect airflow information in flight. This information can further our understanding on the role hair sensors play in a biological system, such as the bat's, and may also be able to support flight control on small unmanned aerial vehicles (UAVs), particularly on flapping UAV platforms [41].

The proposed system design uses the hair structure to transduce airflow into a change in capacitance which is measured and converted to a digital value. This data is communicated on an I^2C bus to a microcontroller. Although, in initial prototypes a commercial-off-the-shelf (COTS) chip (AD7746) can be used to establish proof of concept, this part lacks the speed to support multiple sensors. The part provides an RMS resolution of 40aF and conversion rate of 90Hz [20]. In order to achieve the required sensitivity, speed, and area specifications, a custom capacitance readout chip would be designed and implemented. Additionally, a reduction of the physical dimensions of the sensor would allow it to be distributed and placed in more locations.

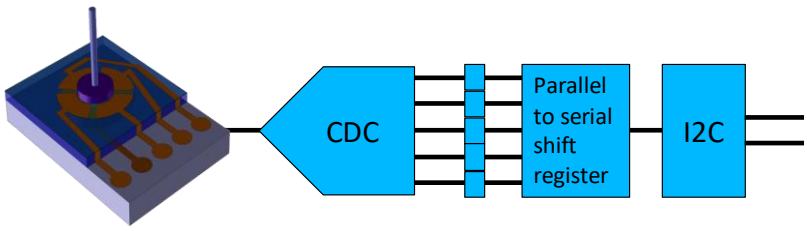

Figure 6.2. System architecture showing airflow sensor interfaced to CDC and output bits conditioned for I2C readout **[12]**. Copyright © 2016, IEEE

The sensor and readout chip could be placed on a flexible PCB, which would be attached to a bat's wing as illustrated in Fig. 6.3. The COTS chip provides sensing and readout but requires a relatively large area and wire-bonding from the hair structure to the PCB. A custom design could replace this scheme, with the potential for the hair sensor to be fabricated directly on the IC. The overall system is intended to transduce *in situ* airflow data during free flight under laboratory conditions.

The goal would be to ultimately place multiple sensors on a bat's wing, at locations illustrated in Fig. 6.4. These could be single hair sensors or arrays of sensors per site. The bat can carry a backpack with battery and microcontroller to communicate with the sensors. In this implementation the I^2C bus has been selected for the ability for multiple devices to share the same 4 lines (Power, Ground, Serial Data, and Serial Clock).

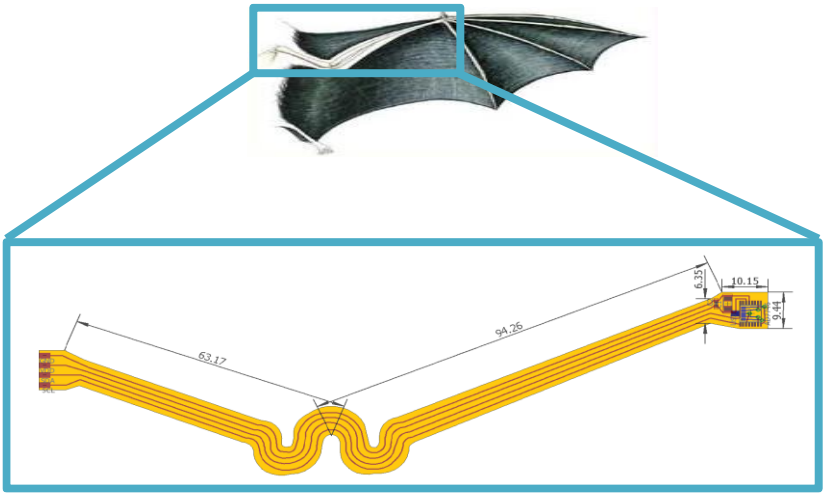

Figure 6.3. FlexPCB design showing traces running across bats arm to sensor on bats knuckle (measurements in mm) **[12]**. Copyright © 2016, IEEE

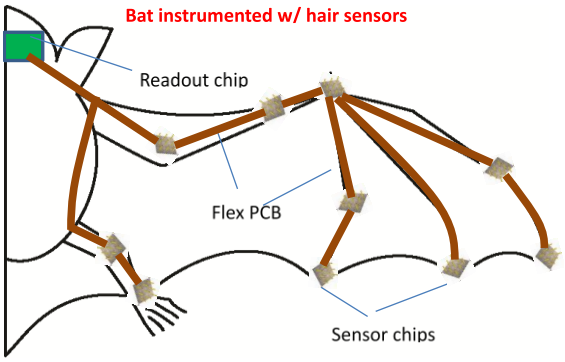

Figure 6.4. Instrumented bat concept showing sensor locations along bats wing interconnected by flexPCB traces **[12]**. Copyright © 2016, IEEE

As more devices are added, they could be programmed with unique addresses using non-volatile memory such as poly fuses, floating gates or hardwiring.

There are foreseeable challenges to overcome or account for with a system such as the one presented. From an overall system perspective, for example, delamination of the flex PCB from the bat when it bends and flaps its wings could be a problem. The PCB should not be too rigid and designed to bend appropriately at different joints. Braided wires could be an alternative if they are small and light enough.

6.4.2 Distributed Strain Sensing on Airfoil

Animals such as birds, bats, and insects have extensive sensor arrays in their wings that give them information about air flow and force distribution, helping them deal with windy conditions. Small unmanned air vehicles (UAVs), on the other hand, can experience strong disturbances in roll due to changes in wind angle over their wings, which current attitude control systems using inertial measurement units (IMU) may not be able to stabilize fast enough. Consequently, previous studies have shown that sensing wing deformation in UAVs and arm deflection in rotorcraft can provide faster flight control than centrally mounted inertial sensors, similar to the mechanosensory system in

insects [42] [43]. Therefore, incorporating force and flow measurements into small UAV attitude control systems can offer potential benefits, with strain sensors showing promise for total moment measurement [42].

Engineered strain sensors can be used to measure UAV wing deformations, but the task of embedding hundreds of these sensors on a UAV wing is not easy. The sensing system needs to minimize flow perturbation, tolerate collisions, and be able to measure larger strains without constraining wing deflection. Larger numbers of sensors can provide numerous benefits, including better disturbance classification and noise reduction [44]. A number of studies have proposed distributed strain sensing systems which can sense wing deformation during flight, but significant challenges remain [45] [46]. These include maintaining high sensitivity while distributing sensors across a larger area and dealing with tradeoffs between number of sensors, sample rate, and noise when collecting and processing data from a large array of sensors in real-time.

Although current commercially available ICs have been used for real-time data collection in these systems, their bandwidth is severely limited. Incorporating the capacitance to digital converter proposed could allow the ability to fully capture the dynamic motion of the airfoil without having to subsample the system and populate the wing with more sensors. Additionally, the addresses are customizable removing the need to multiplex commercial chips that may not offer the option. Example of strain sensing system is shown in Fig. 6.5.

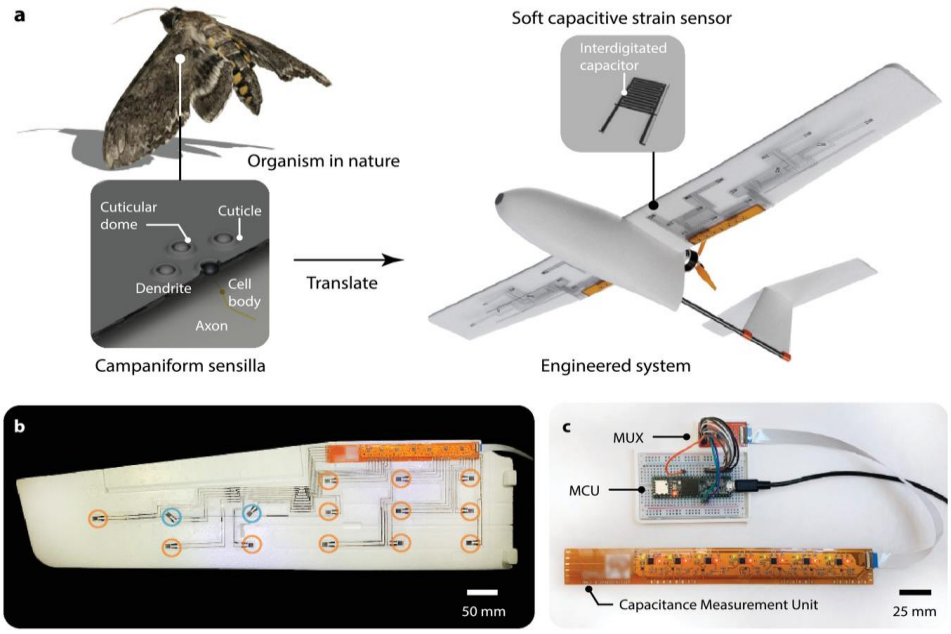

Figure 6.5. A large-area soft sensing skin to measure wing deformations in small UAVs. a) Illustration of a hawkmoth's wing with embedded strain sensors (campaniform sensilla) on its forewings and their reflection in the engineered small UAV wings used in this work. b) Photograph of a single UAV wing integrated with the large-area soft sensing skin and a flexible PCB for capacitance measurements. Most of the sensors were embedded to detect normal strains (orange circles) with two shear strain sensors tilted at ± 45° (blue circles). c) Image of the measurement electronics in the sensing skin system including a capacitance measurement unit, a multiplexer, and a microcontroller unit. Figure used with permission from **[45]**.

6.5 Technical Contributions

The primary contributions of this work are as follows:

- **Design of two-step SAR capacitance-to-digital converter**

  The design of a two-step SAR CDC is presented. The relationship between the 16-bit digital output representation and the sensed capacitance is derived. Showed how a two-step architecture produces sub-femtofarad resolution. The use of non-uniform conversions is shown to improve speed capabilities. Explored noise and offset-limited achievable resolution.

- **Testing of two-step SAR capacitance-to-digital converter**

  The proposed design was fabricated and tested in a 0.5µm and 0.18µm technology. The DNL and INL figures were determined and effective resolution compared under different testing conditions. The design achieves 9.8 ENOB for 64µs/28µs conversion times (Near fastest reported conversion). When overclocked, it achieves 8.2 ENOB for 32µs/14µs conversion times (Fastest reported conversion). This equates to a near highest ENOB throughput (FoM2) of 150/350 kbits/s (Nominal) and 256/585 kbits/s (Overclocked). The nonlinearity is explored with maximum average INL/DNL of 276 LSB/11.4 LSB.

- **Demonstrated sensor testing for higher input frequency sensors**

  Created a high frequency area changing capacitance sensor. The circuit was tested with high frequency sensors which is not reported by many published works considering their converter bandwidth capabilities. Demonstrated testing at 234Hz and 656Hz (Fastest reported testing speeds).

6.6 Publication Record

6.6.1 Journal Articles in Preparation

1. **A. Castro**, and P. Abshire, "A Two Step SAR Capacitance to Digital Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2023. [In preparation]

6.6.2 Refereed Conference Proceedings

1. **A. Castro**, and P. Abshire, "A Two-step SAR Capacitance-to-Digital Converter," *2023 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2023. [In preparation]

2. **A. Castro**, H. Bae, M. Yu and P. Abshire, "Bat-inspired hair sensor," *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Shanghai, 2016, pp. 556-559.

3. **A. Castro**, L. Peckerar, T. Horiuchi and P. Abshire, "Rotor-induced Airflow for Odor Source Detection on Nano-Quadcopters," *2020 IEEE SENSORS*, 2020, pp. 1-4.

4. **A. Castro**, N. Magnezi, B. Sintayehu, A. Quinto and P. Abshire, "Odor Source Localization on a Nano Quadcopter," *2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Cleveland, OH, 2018, pp. 1-4.

5. B. Senevirathna, **A. Castro**, M. Dandin, E. Smela and P. Abshire, "Lab-on-CMOS capacitance sensor array for real-time cell viability measurements with I2C readout," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, QC, 2016, pp. 2863-2866.

6. B. Senevirathna, **A. Castro**, T. Datta-Chaudhuri, E. Smela and P. Abshire, "Characterization of an active micro-electrode array with spike detection and asynchronous readout," *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, MA, 2017, pp. 627-630.

7. A. Berkovich, **A. Castro**, M. Islam, F. Choa, G. Barrows and P. Abshire, "Dark current reduction by an adaptive CTIA photocircuit for room temperature SWIR sensing," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, 2017, pp. 1-4.

8. T. Datta-Chaudhuri, B. Senevirathna, **A. Castro**, E. Smela and P. Abshire, "An active micro-electrode array with spike detection and asynchronous readout," *2014 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings*, Lausanne, 2014, pp. 588-591.

Appendix A

A.1 Bat-inspired Hair Sensor

The following design of a directional airflow sensor is inspired by the hair sensors on the bat wing [40].

Various designs of artificial hair sensors were considered and simulated for the proposed application. Ultimately, a capacitive hair sensor design was chosen because they can generally offer directionality, high sensitivity, good frequency response, low temperature sensitivity, and low power consumption. The hair structure presented is derived from the work in [12].

In order to achieve the necessary directionality and sensitivity, the structure in Fig. A.1 was originally designed.

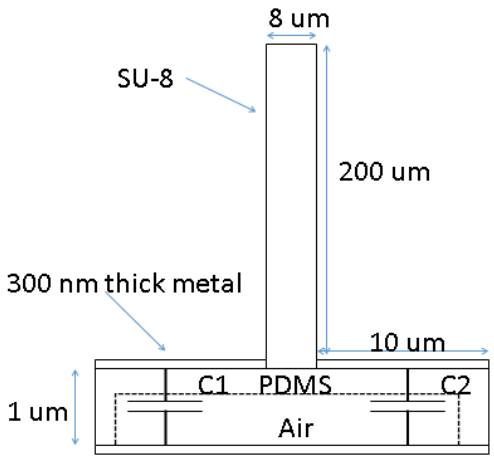

Figure A.1. MEMS hair structure cross-section showing the air cavity and PDMS diaphragm that form the base with dimensions.

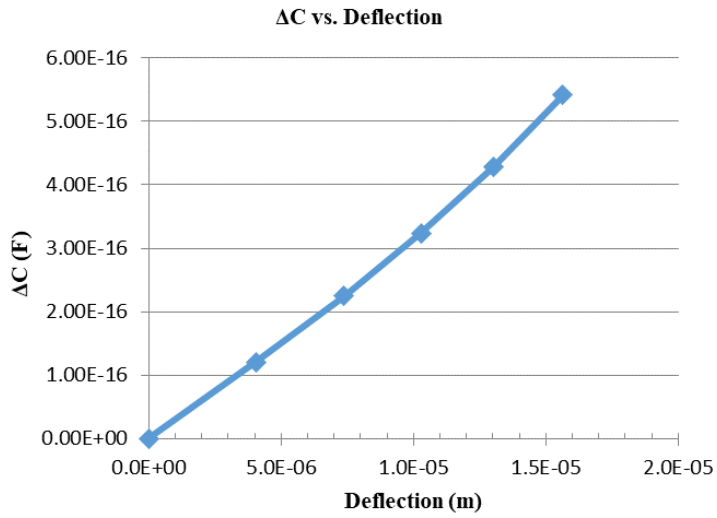

Figure A.2. Differential capacitance change with increasing deflection of MEMS structure showing capacitive range.

For a deflection of 8μm, the differential capacitance ΔC = 250aF. The designed structure achieves directional sensing with the use of 4 electrodes on a flexible membrane.

To achieve similar sensitivity with less aggressive sizing, the cavity height and diameter are scaled up accordingly. Also, a silicon disc is placed on the flexible diaphragm to serve as a base for the vertical hair while providing mechanical amplification for high sensitivity.

Multiphysics Finite Element Model (FEM) simulations were performed to characterize and optimize the structural design. Fig. A.3 shows the velocity magnitude as air deflects the hair.

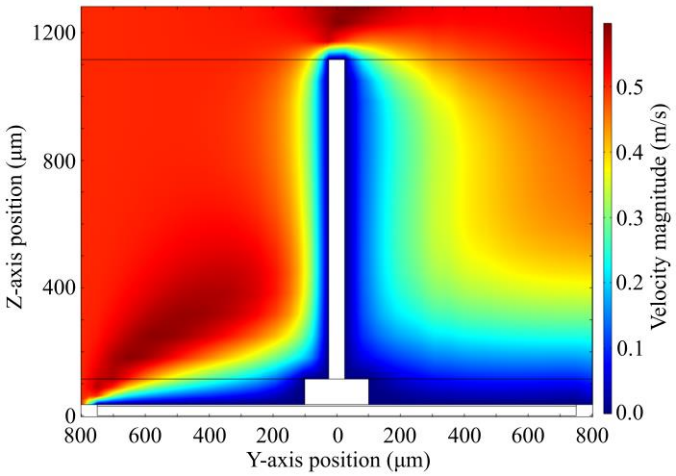

Figure A.3. FEM velocity field simulation for airflow speed of 0.5 m/s showing the fluid-structure interaction with the sensor **[12]**. Copyright © 2016, IEEE

The structure has been designed so that it exhibits 225aF of differential capacitance (Fig. A.4) for an airflow speed of 0.5m/s. The expected bat flight speed ranges from 0.5–8m/s. The sensitivity of the structure can be adjusted by changing the height and/or diameter of the cavity, and the hair length.

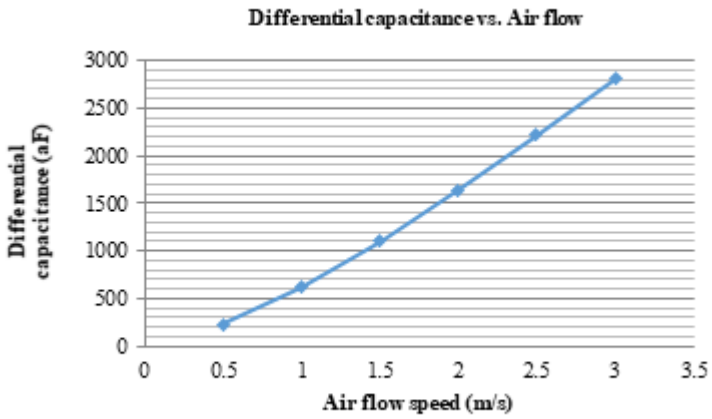

Figure A.4. Differential capacitance change with increasing airflow of MEMS structure showing capacitive range for typical bat flight speeds. **[12]**. Copyright © 2016, IEEE

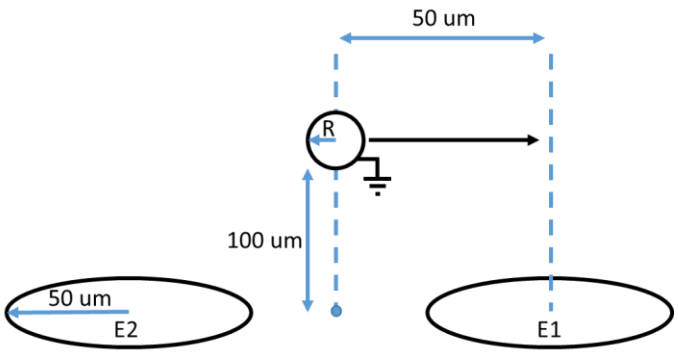

Figure A.5. Interference model for differential capacitance with grounded sphere displaced from center of both electrodes.

The benefit of using a differential capacitance reading is its high tolerance to noise. Additionally, offset capacitances can almost completely be eliminated as the common mode capacitance should approximately be equal.

To analyze how much of an effect an interfering body makes on the differential capacitance, the following model was also simulated.

A grounded sphere is displaced from the center of circular electrodes E1 and E2. The capacitance C1 and C2 corresponds to the capacitance between each electrode and the sphere. The differential capacitance in Fig. A.6 refers to $\Delta C = C1-C2$ for different sphere radii R.

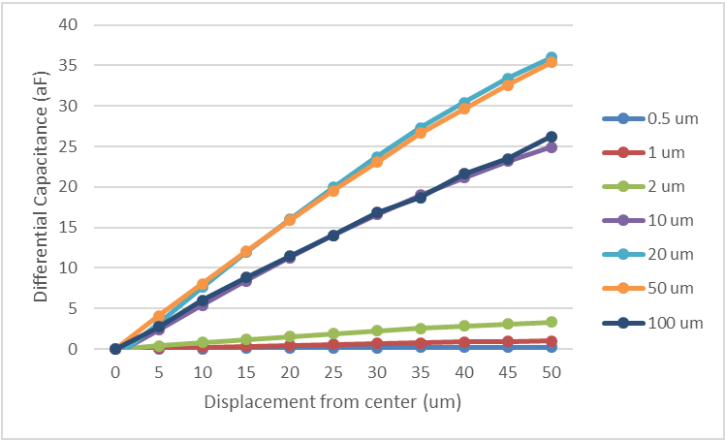

Figure A.6. FEM simulation of interference model for differential capacitance with grounded sphere displaced from center of both electrodes at different heights.

The results show that the biggest change in capacitance seen is on the order of tens of attofarads. This simulation was performed at a fixed height of 100 um, which is considerably close to the electrodes. As the interfering body gets further away, the added differential capacitance becomes even more negligible.

A.2 Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) was also simulated for the switched capacitor amplifier of the preliminary design and shown in Fig. A.7. The PSRR is greater than 77dB for frequencies below 100kHz and has a minimum of about 14dB at around 150MHz.

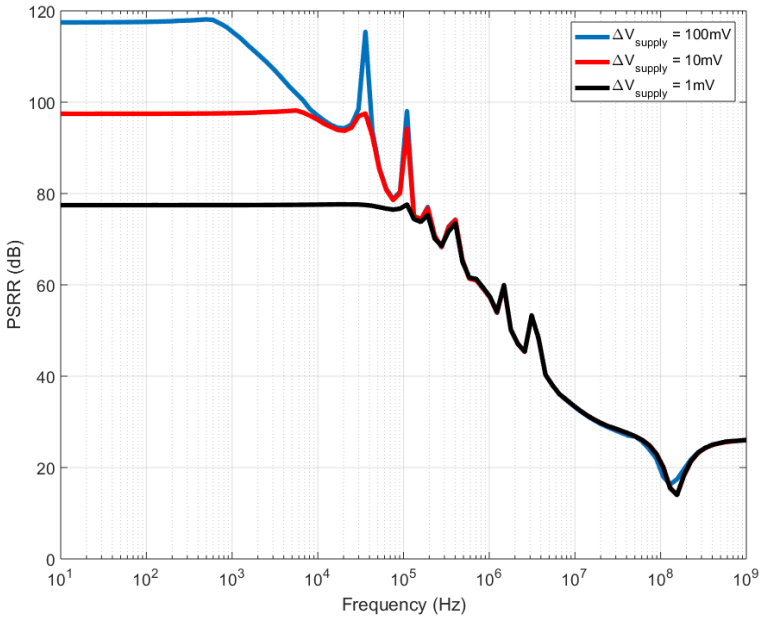

Figure A.7. Frequency sweep of PSRR showing higher noise rejection in the power supply at lower frequencies for different supply voltage peak-peak variations.

A.3 Circuit Details and Layout

A.3.1 On-chip Bias Generator Circuit

The bias circuit implemented on-chip was a Beta-multiplier, self-referenced bias circuit [47]. It consists of three main parts: a start-up circuit, Beta-multiplier circuit, and current mirror circuit. The output of the circuit generates three bias voltages (Vn, Vp, and Va). Bias voltages Vn and Vp connect to the NMOS and PMOS transistors setting the tail currents of the rail-to-rail opamp circuit, respectively. While, bias voltage Va sets the tail current for the opamp in the switched capacitor amplifier circuit and the comparator. A 3.7kΩ resistor is used and the other device sizes are listed below.

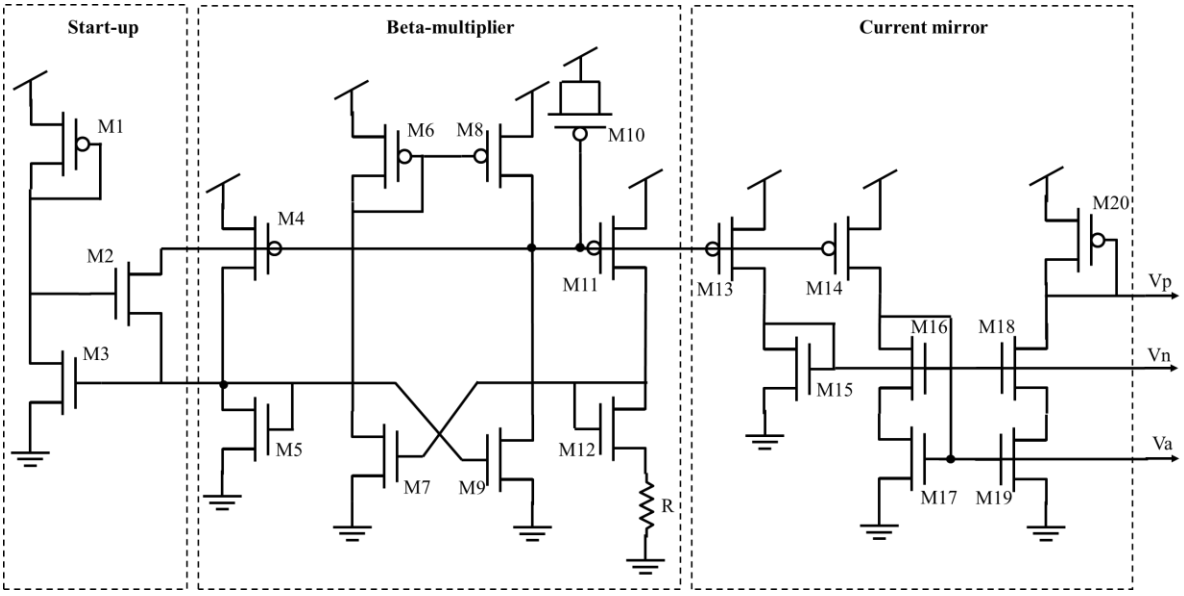

Figure A.8. On-chip bias generator circuit consisting of a startup, beta multiplier, and current mirror circuit to generate the required voltages.

TABLE V

BIAS GENERATOR TRANSISTOR SIZING

Device	M1	M2	M3, M5, M7, M9	M4, M6, M8, M11, M14	M10	M12	M13	M15	M16-M19	M20
W/L	1.2/2.4	0.35/0.35	7.0/0.35	12/0.3	6.0/6.0	28/0.35	24/0.3	0.7/0.7	1.0/0.35	0.6/0.3

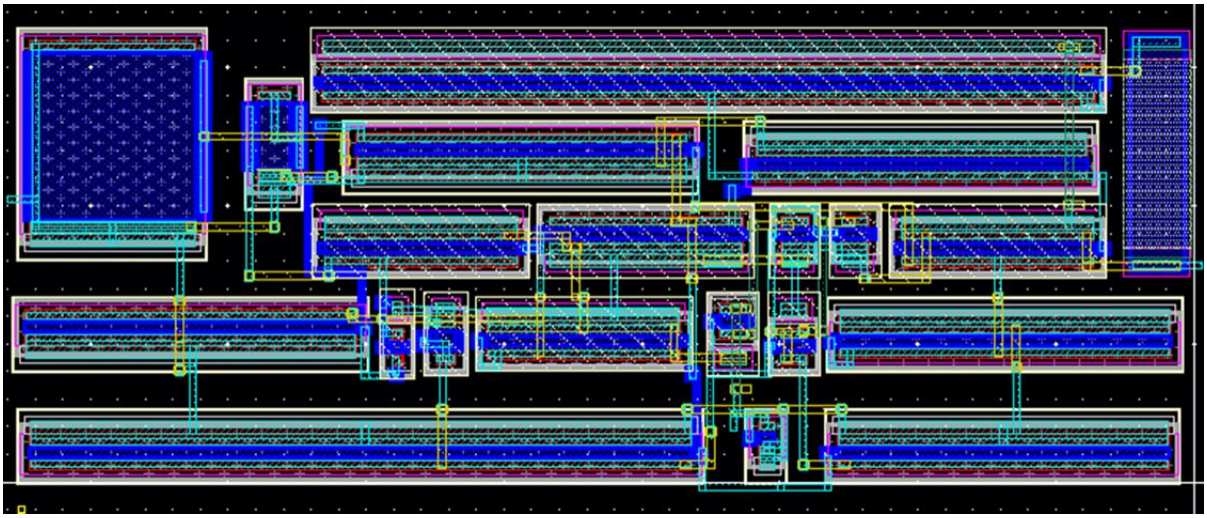

Figure A.9. Bias generator circuit layout.

A.3.2 Sample-and-Hold Circuit

The sample-and-hold circuit is shown in more detail below. The transmission gates (M1-M6) have dummy devices (MD1-MD12) around them to reduce charge injection. The dummy devices are half the size of the size of the transmission gates and are driven by antiphase signals. A 500fF MIM capacitor is used for the sampling capacitor.

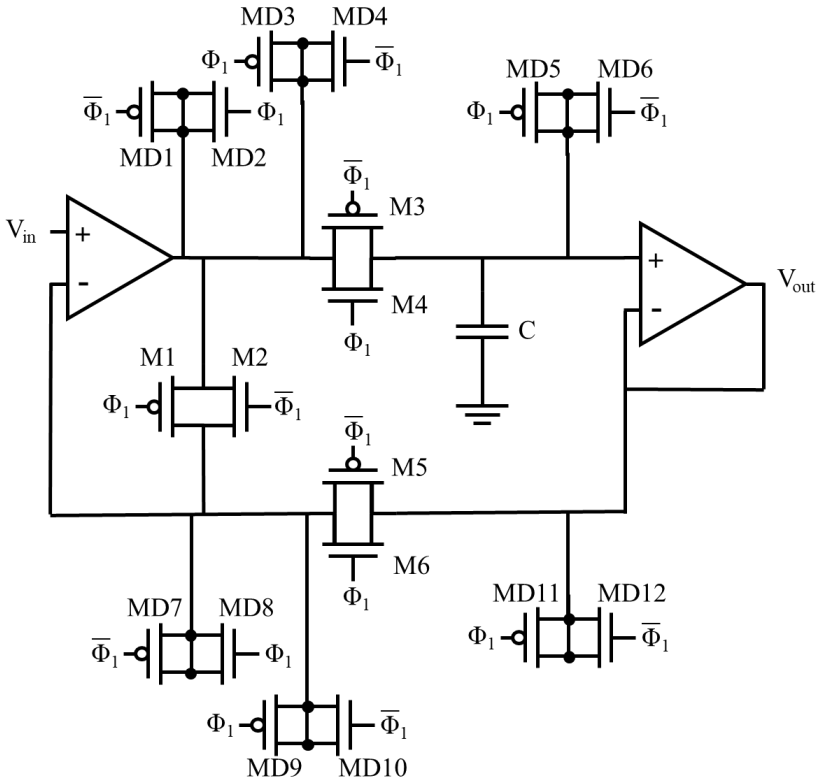

Figure A.10. Sample-and-hold circuit with dummy switches for charge injection reduction and opamp buffers around the hold capacitor.

TABLE VI

SAMPLE-AND-HOLD TRANSISTOR SIZING

Device	M1, M3, M5	M2, M4, M6	MD1, MD3, MD5, MD7, MD9, MD11	MD2, MD4, MD6, MD8, MD10, MD12
W/L	1.05/0.35	1.2/2.4	0.525/0.35	0.6/2.4

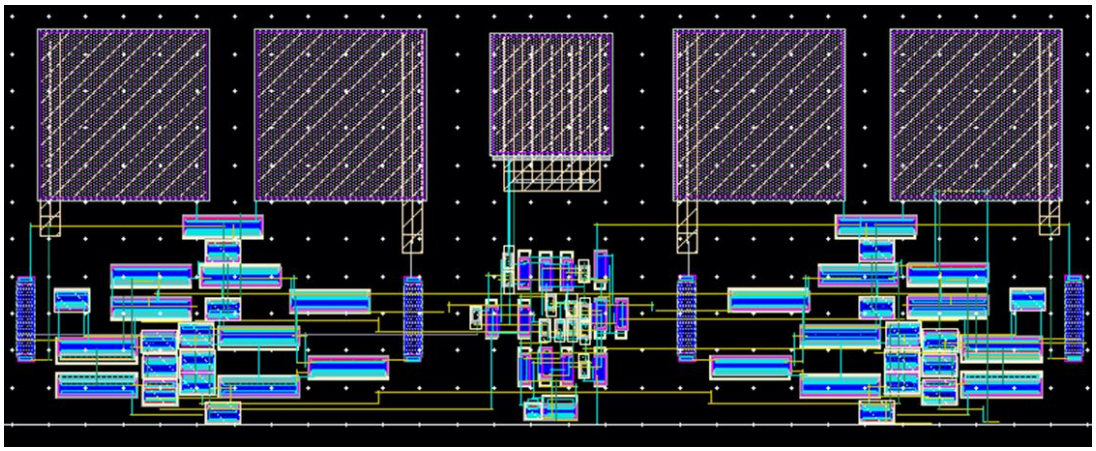

Figure A.11. Sample-and-hold circuit layout.

The opamps were implemented with a cross-coupled rail-to-rail design shown below. A resistor value of 5kΩ and compensating capacitance of 1pF was used for the first two sample-and-hold stage opamps, while 10kΩ and 2pF was used for the last sample-and-hold stage.

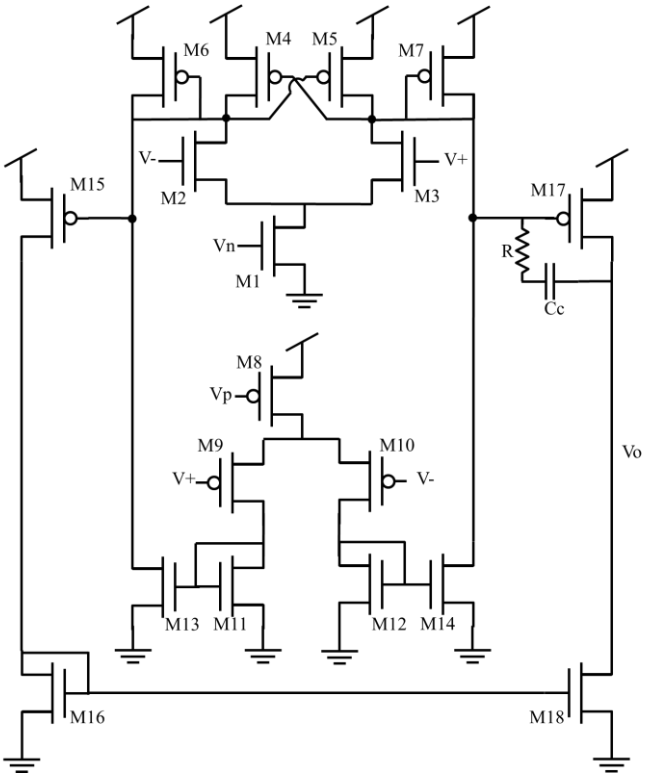

Figure A.12. Cross-coupled rail-to-rail opamp circuit for wide input and output swing implemented in the sample-and-hold circuit **[34]**.

TABLE VII

RAIL-TO-RAIL OPAMP TRANSISTOR SIZING

Device	M1	M2-M3, M11-M14, M16, M18	M4-M7, M9-M10, M15, M17	M8
W/L	7.7/0.7	3.85/0.7	9.78/0.6	19.56/0.6

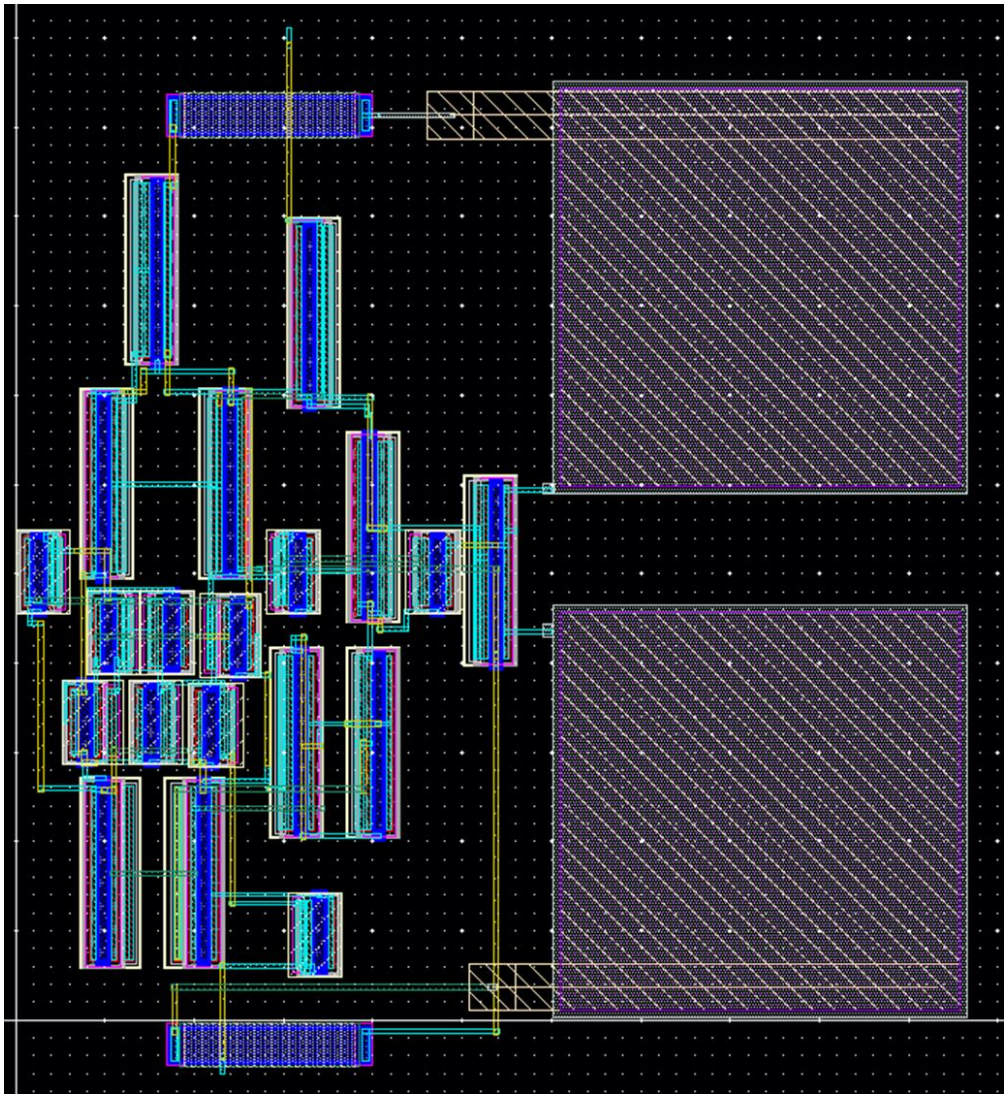

Figure A.13. Rail-to-rail opamp circuit layout with 5kΩ resistor and 1pF compensating capacitance.

A.3.3 Switched Capacitor Amplifier Circuit

The switched capacitor amplifier circuit is shown in more detail below. The transmission gates (M1-M6) have dummy devices (MD1-MD12) around them to reduce charge injection. The dummy devices are half the size of the size of the transmission gates and are driven by antiphase signals. Capacitor C2 is implemented with a 340fF MIM capacitor and C1 with 1.7pF or 3.4pF MIM capacitor depending on the gain stage.

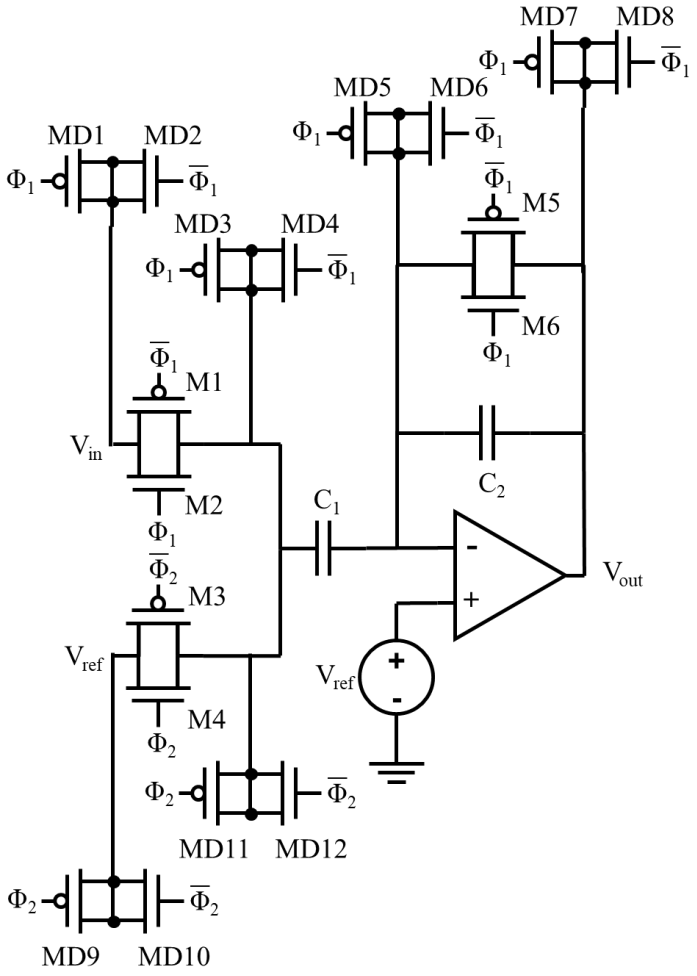

Figure A.14. Switched capacitor amplifier circuit with dummy switches to reduce charge injection errors.

TABLE VIII

SWITCHED CAPACITOR AMPLIFIER TRANSISTOR SIZING

Device	M1, M3, M5	M2, M4, M6	MD1, MD3, MD5, MD7, MD9, MD11	MD2, MD4, MD6, MD8, MD10, MD12
W/L	1.2/2.7	1.05/0.525	0.6/2.7	0.525/0.525

The opamp in the amplifier circuit is presented below. A two stage opamp is used with a resistor value of 5kΩ and compensating capacitance of 500fF.

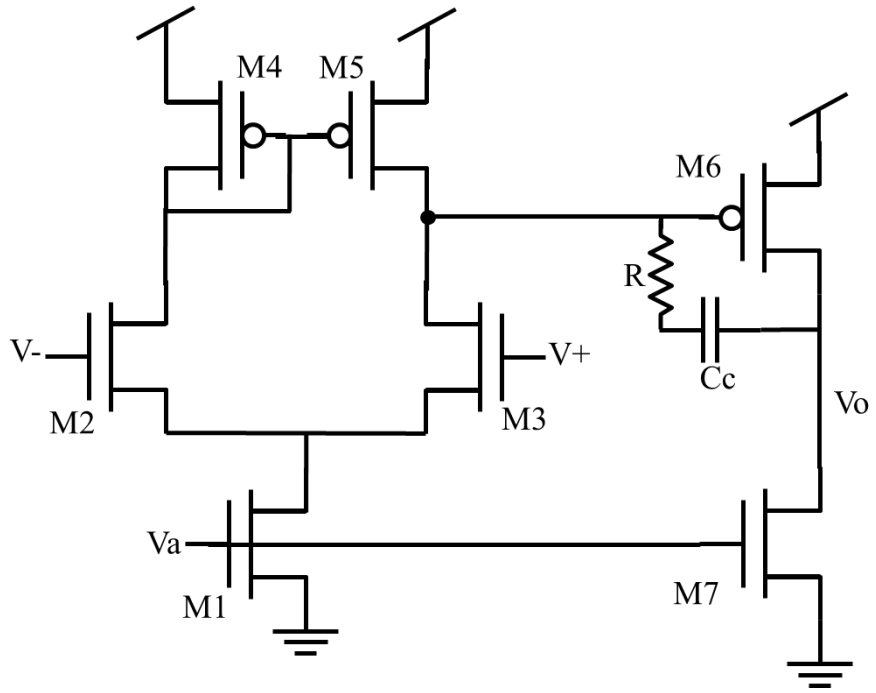

Figure A.15. Two stage opamp circuit used in switched capacitor amplifier.

TABLE IX

SWITCHED CAPACITOR OPAMP TRANSISTOR SIZING

Device	M1-M3, M7	M4-M5	M6
W/L	5.6/0.7	4.8/0.6	9.6/0.6

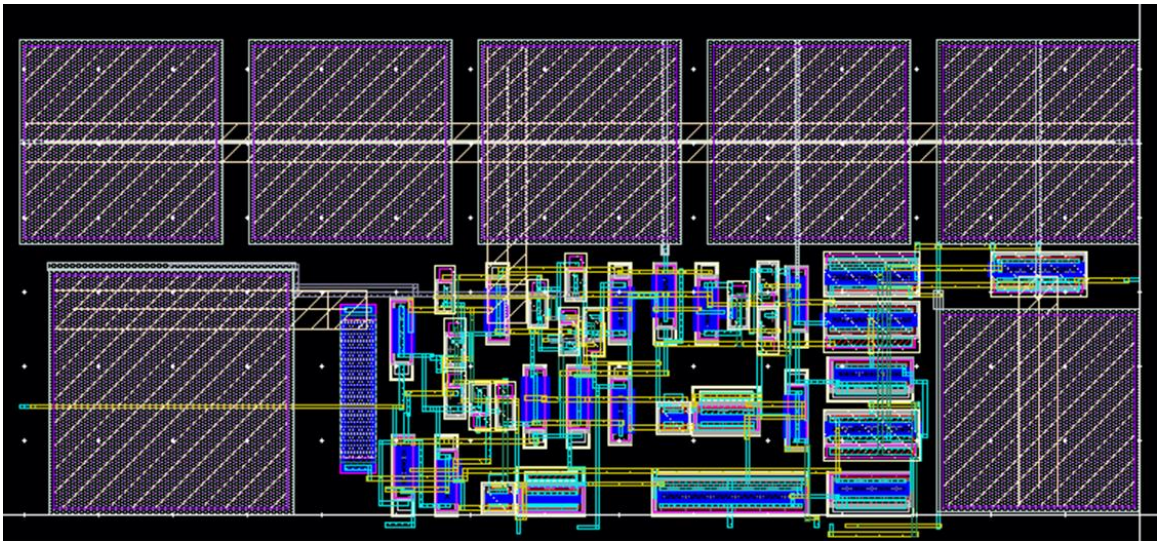

Figure A.16. Switched capacitor amplifier circuit layout.

A.3.4 Comparator Circuit

The comparator circuit was implemented using a two stage opamp. A resistor value of 10kΩ and compensating capacitance of 500fF was used. The layout is presented with the resistor and capacitor implemented with a poly resistor and MIM capacitor, respectively.

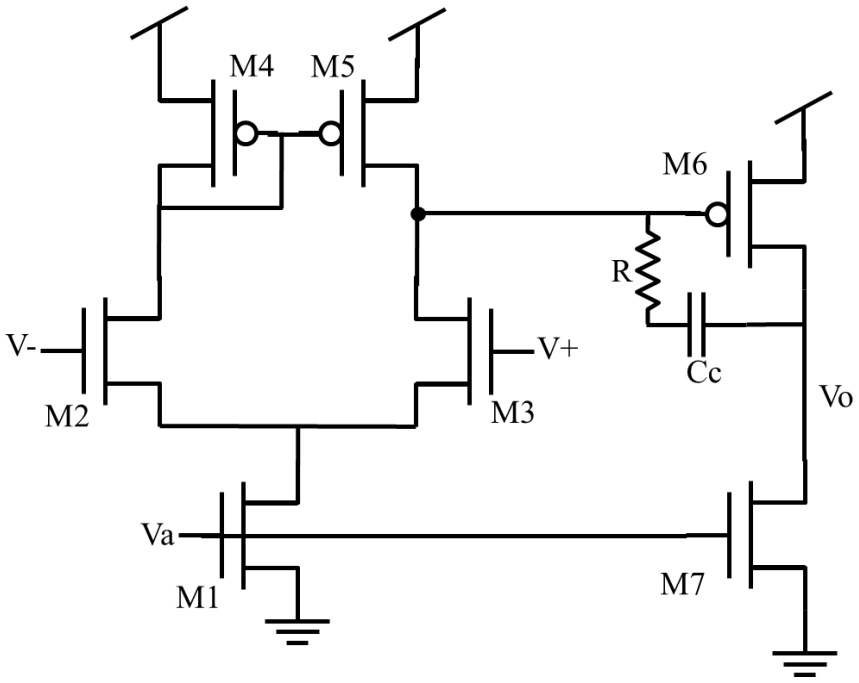

Figure A.17. Two stage opamp circuit used as comparator for coarse and fine conversions.

TABLE X

COMPARATOR TRANSISTOR SIZING

Device	M1	M2-M3, M7	M4-M5	M6
W/L	11.2/0.35	5.6/0.35	4.8/0.6	9.6/0.6

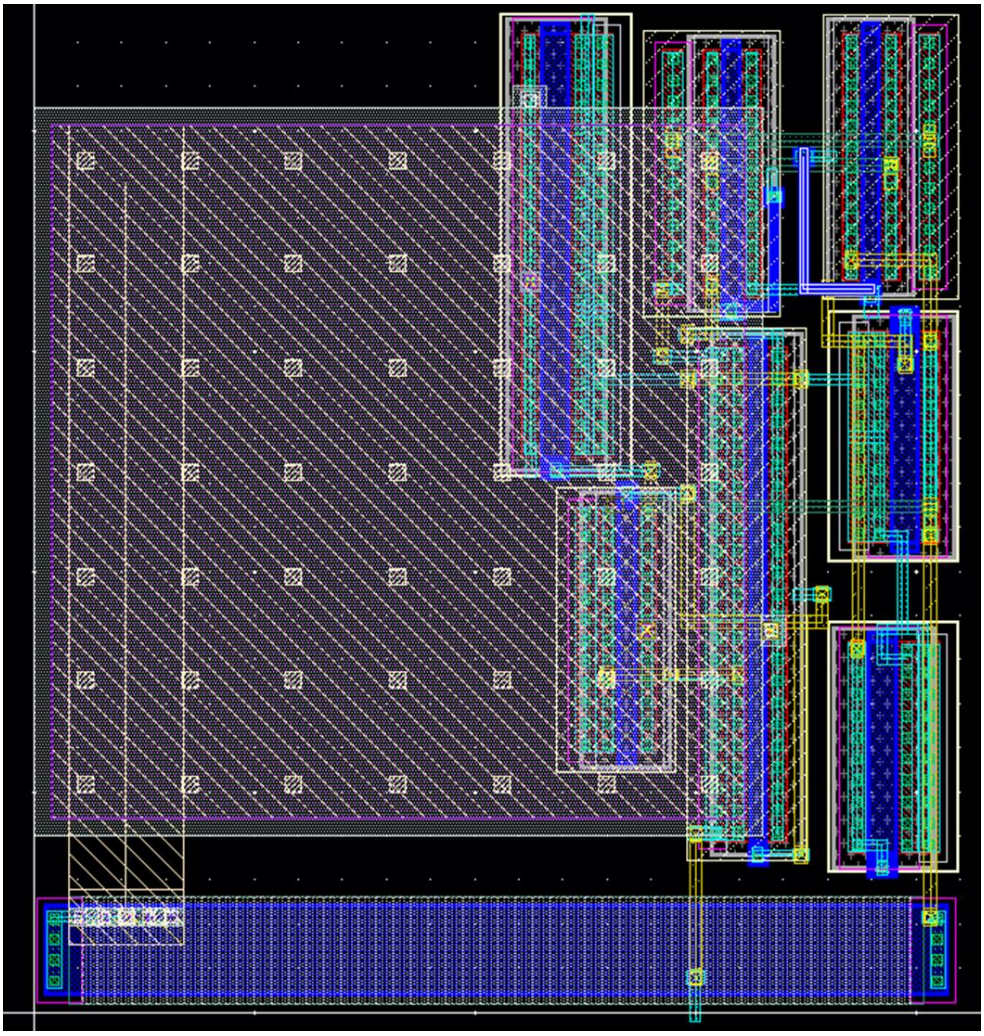

Figure A.18. Two stage opamp comparator circuit layout.

A.3.5 CDAC Layout

The capacitor DACs for the coarse conversion, fine conversion, and test DAC are shown below with transmission gate sizes listed. To reduce mismatch, unit capacitors were placed in a common centroid configuration surrounded by dummy devices around the outside. The Modgen tool in Cadence was used to generate the CDACs with a guard ring surrounding the structure. The unit capacitors for the coarse and fine CDACs use 10.3fF MOM capacitors while the test DAC uses a 6.3fF MOM unit capacitor.

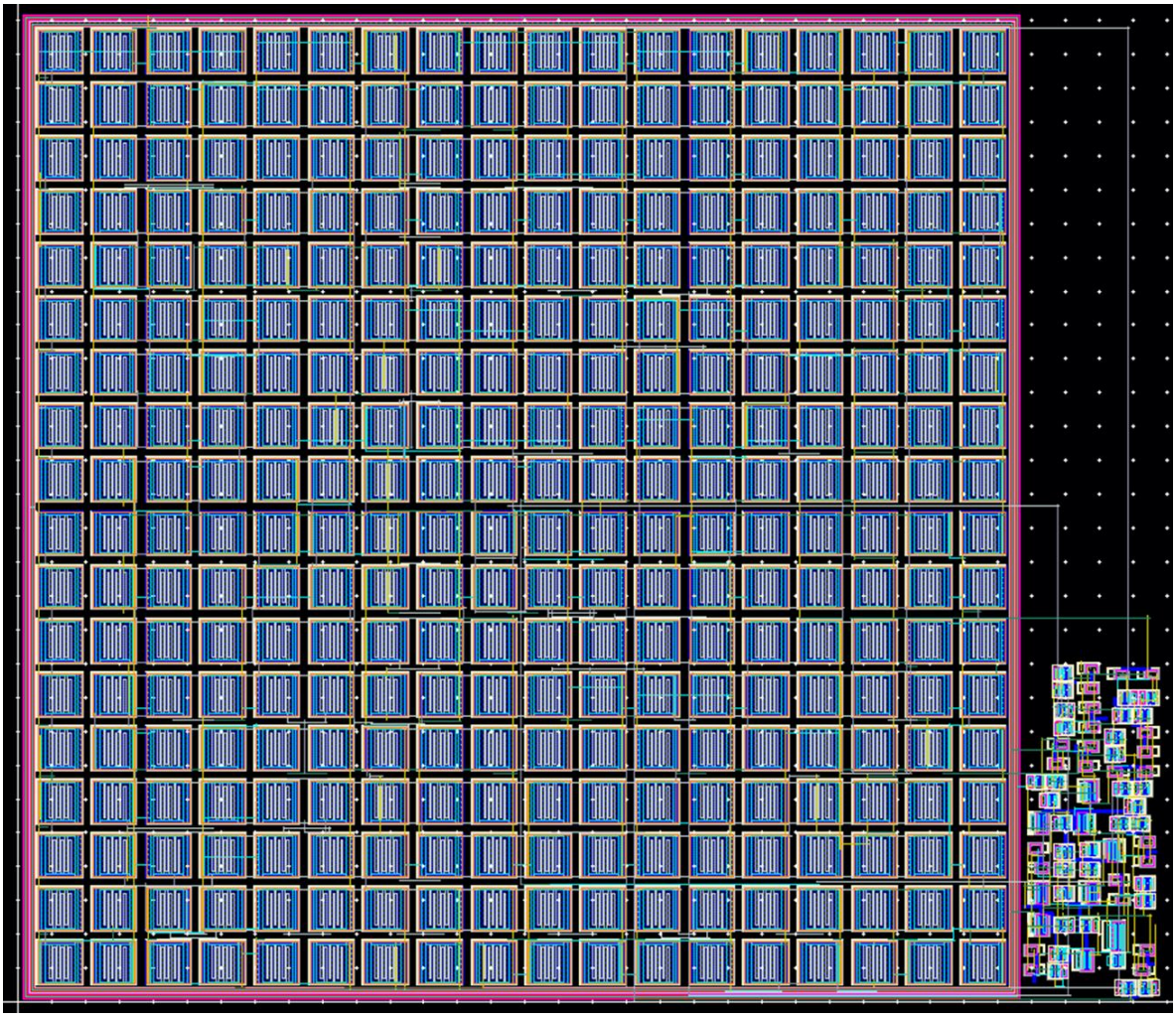

Figure A.19. Coarse CDAC with common centroid configuration, dummy devices, and guard ring.

TABLE XI

COARSE CDAC TRANSMISSION GATE TRANSISTOR SIZING

Device	S_0-S_7		S_{E1}-S_{E4}		S_D		Reset	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
W/L	2.8/0.35	1.2/0.3	2.8/0.35	1.2/0.3	1.4/0.35	2.4/0.3	0.525/0.35	6.0/0.3

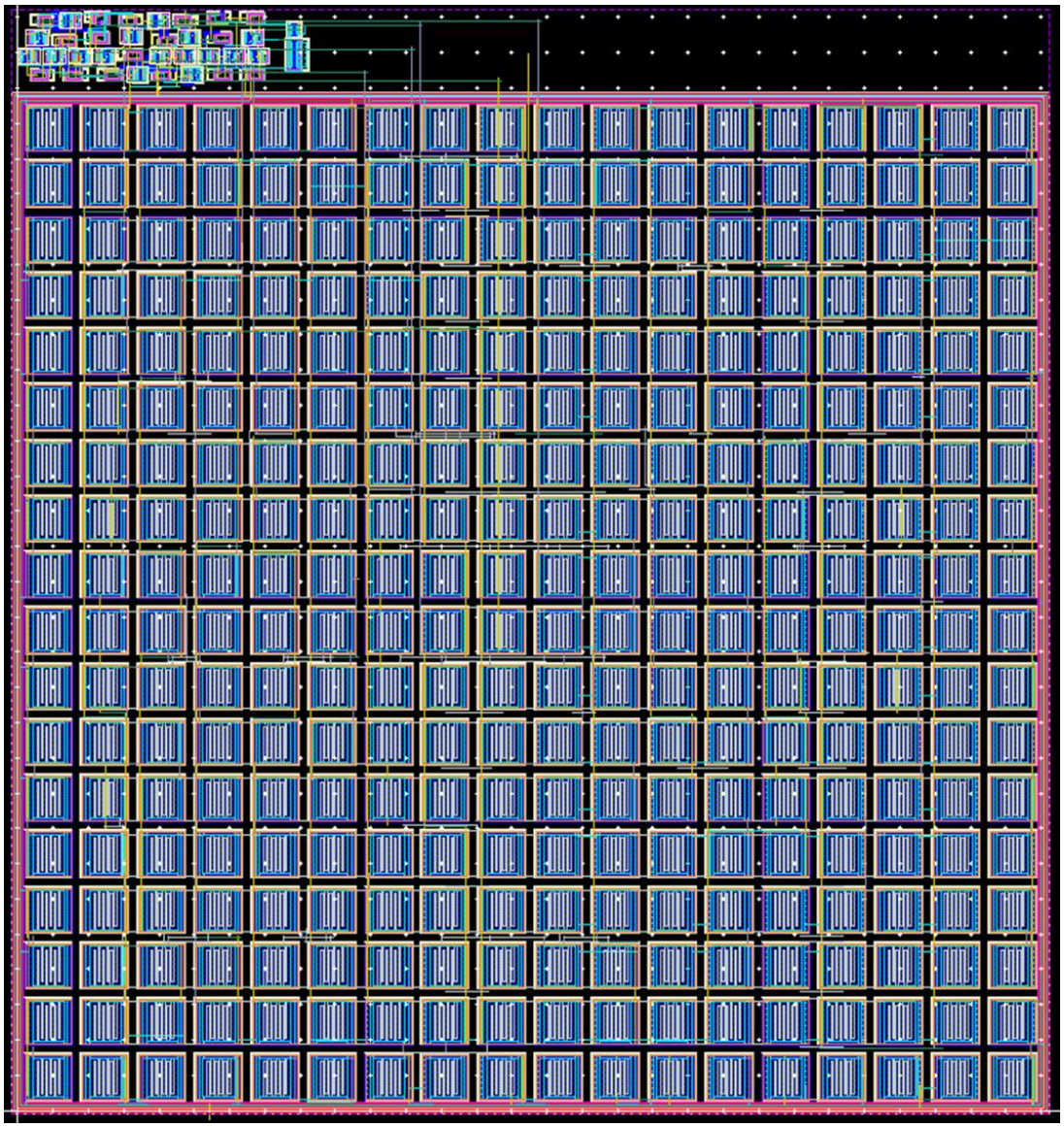

Figure A.20. Fine CDAC with common centroid configuration, dummy devices, and guard ring.

TABLE XII

FINE CDAC TRANSMISSION GATE TRANSISTOR SIZING

Device	S_0-S_7		Reset	
	NMOS	PMOS	NMOS	PMOS
W/L	1.4/0.35	0.6/0.6	1.4/0.35	0.6/0.6

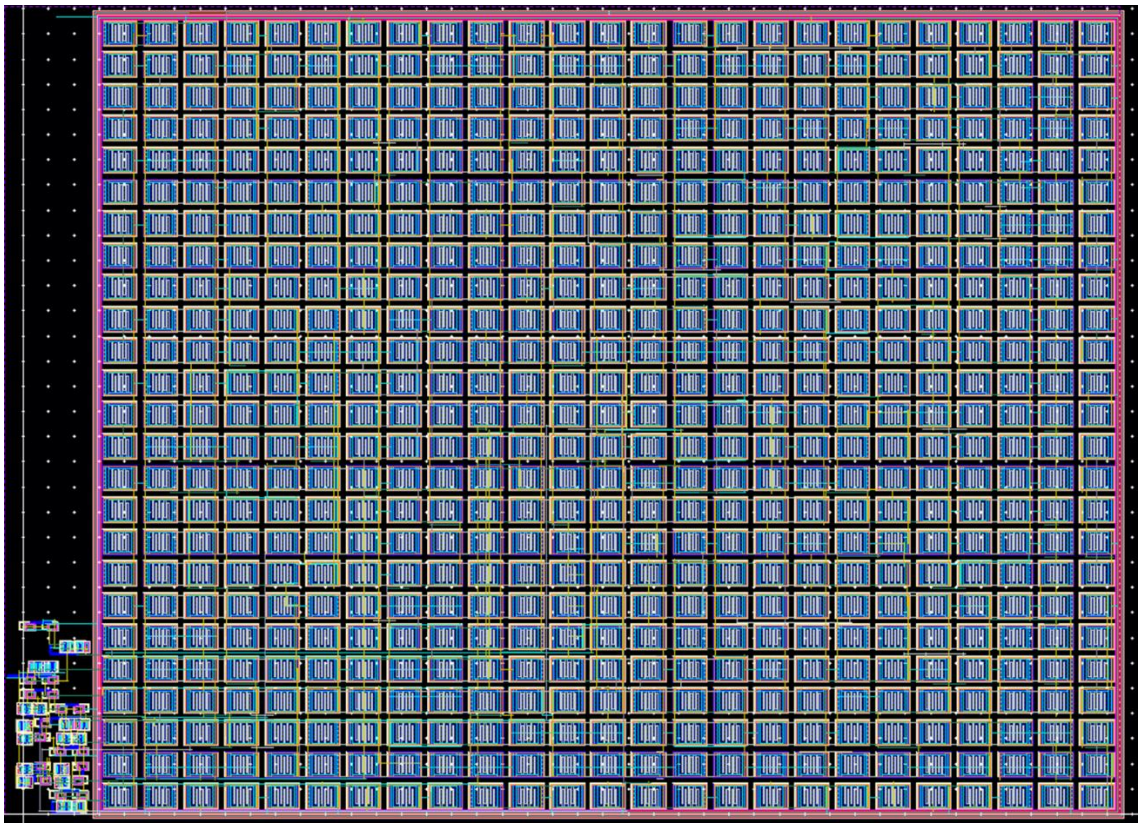

Figure A.21. Test DAC with common centroid configuration, dummy, devices, and guard ring.

TABLE XIII

TEST DAC TRANSMISSION GATE TRANSISTOR SIZING

Device	S_0-S_8	
	NMOS	PMOS
W/L	2.8/0.35	1.2/0.3

A.4 Die Photos of Fabricated Designs

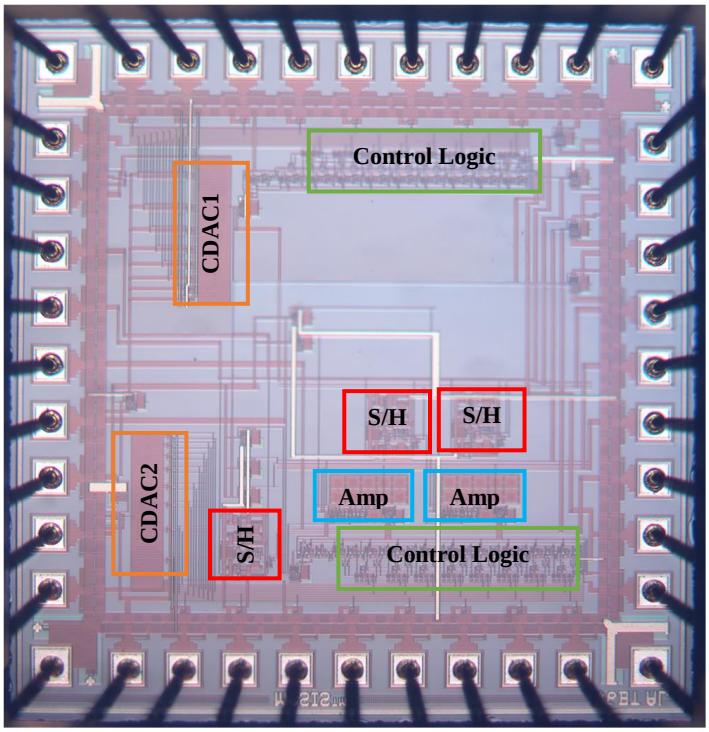

Figure A.22. Die photo of preliminary design (1.5 x 1.5 mm^2)

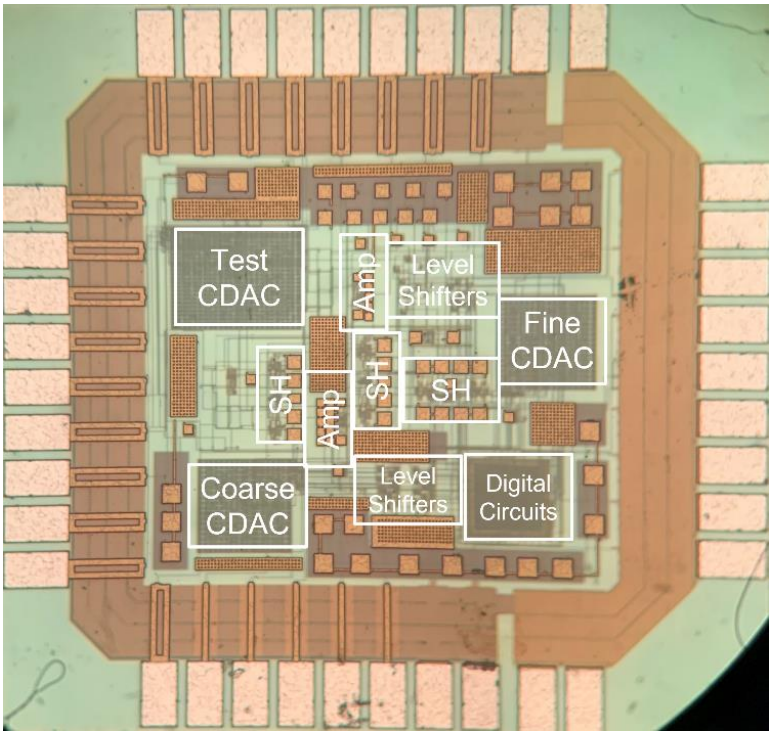

Figure A.23. Die photo of final design (1.1 x 1.15 mm^2)

A.5 Implemented Verilog Code for Digital Circuit Synthesis

The verilog code was synthesized and implemented with the following summarized steps. First, the RTL compiler was run where the Verilog top level is specified and additional attributes are set such as the clock timing constraints. This synthesizes the code into a gate level netlist. Then, the logic gates from this file is imported into Cadence Encounter to place and route the digital circuit block. During this step the power and ground rings are setup and the standard cells are placed to fit in the area and routed. Once completed, the design is exported as a GDS file and the final netlist. Finally, these files are imported into Cadence Virtuoso to be implemented with the rest of the design.

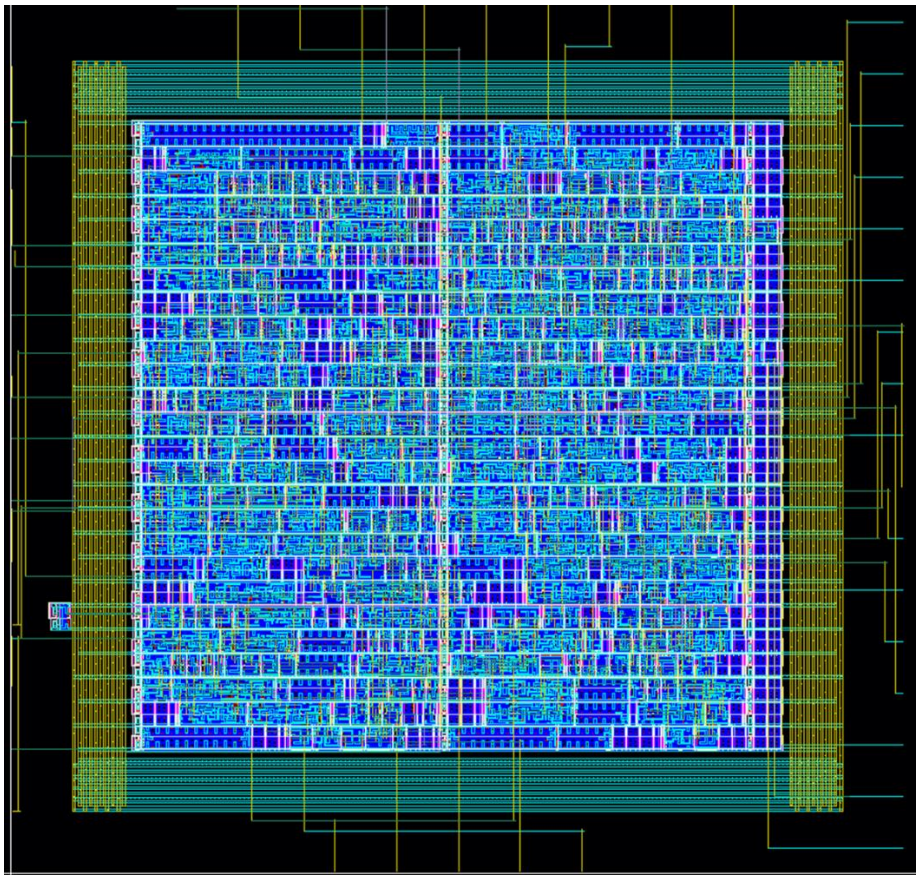

Figure A. 24. Synthesized Verilog digital circuit layout

```
module ClockSignals(
       input clk,
       input rst,
       input hold,
       input Ack,
       output EXC,
       output EXCN,
       output T1,
       output T2,
       output T3,
       output T4,
       output Qfr,
       output Clock,
       output RESET,
       output RESET2,
       output Clock2,
       output S
       );
reg exc;
reg excn;
reg t1;
reg t2;
reg t4;
reg qfr;
reg clock;
reg reset;
reg reset2;
reg [3:0] count;
reg fine;
reg clk2;
reg count2;
reg count3;
reg count4;
reg [1:0] count5;
reg th;

always @(posedge clk) begin
    if (hold) th <= 1'b1;
    if (Ack) begin
        th <= 1'b0;
        qfr <= 1'b0;
        reset <= 1'b0;
        count4 <= 1'b0;
    end
    if (rst) begin
        exc <= 1'b1;
        excn <= 1'b0;
        t1 <= 1'b0;
        t2 <= 1'b1;
        t4 <= 1'b0;
        qfr <= 1'b0;
        clock <= 1'b0;
        reset <= 1'b1;
        reset2 <= 1'b1;
        count <= 4'b0;
        fine <= 1'b0;
        clk2 <= 1'b0;
        count2 <= 1'b0;
        count3 <= 1'b0;
        count4 <= 1'b0;
        th <= 1'b0;
        count5 <= 2'b0;
    end
```

```
    else begin
        clk2 <= ~clk2;
        count3 <= ~count3;

        if (clk2 & ~th & count3) begin
            exc <= ~exc;
            excn <= ~excn;
            if (fine & reset2) begin
                t1 <= excn;
                if (count5 == 2'b01 || count5 == 2'b11) t2 <= ~t2;
                count5 <= count5 + 1;
            end
            else t1 <= t1;
        end
        if (count3 & exc) begin
            if (count == 4'b0 && count2 == 1) begin
                count <= 4'b1010;
            end
            else if (count == 4'b1001) begin
                qfr <= 1'b1;
                fine <= 1'b1;
                count2 <= 1'b1;
                t2 <= ~t2;
                count <= count + 1'b1;
            end
            else if (count == 4'b1101) begin
                reset2 <= 1'b0;
                count <= count + 1'b1;
            end
            else if (count == 4'b1111) begin
                clock <= ~clock;
                reset <= 1'b1;
                reset2 <= 1'b1;
                qfr <= 1'b1;
                t2 <= 1'b1;
                count4 <= 1'b1;
                count <= count + 1'b1;
            end
            else begin
                qfr <= 1'b0;
                reset <= 1'b0;
                count4 <= 1'b0;
                count <= count + 1'b1;
            end
        end
    end
end

assign EXC = exc;
assign EXCN = excn;
assign T1 = t1;
assign T2 = t2;
assign T3 = ~t2;
assign T4 = t1 & t2;
assign Qfr = qfr;
assign Clock = clock;
assign RESET = reset;
assign RESET2 = reset2;
assign Clock2 = (clk & ~th & ~reset2)|count4;
assign S = count2;
endmodule
```

```
module ModeSelect(
       input clk,
       input rst,
       input [7:0] S,
       output [3:0] QE,
       output St,
       output Qt
       );
reg [3:0] qe;
reg [1:0] count;
reg [3:0] mode;
reg st;
reg qt;

always @(posedge clk) begin
    if (rst) begin
        count = 2'b0;
        mode = 4'b0;
        st = 0;
        qt = 0;
    end
    else begin
        mode = S[3:0];
        case (mode)
            4'b0000:
                begin
                    if (count%2 == 0) begin
                        qe = 4'b1100;
                    end
                    else begin
                        qe = 4'b0011;
                    end
                    count = count + 1'b1;
                    st = 0;
                    qt = 0;
                end
            4'b0001:
                begin
                    qe = 4'b1000 >> count;
                    count = count + 1'b1;
                    st = 0;
                    qt = 0;
                end
            4'b0010:
                begin
                    qe = 4'b1100;
                    st = 0;
                    qt = 0;
                end
            4'b0011:
                begin
                    qe = 4'b0011;
                    st = 0;
                    qt = 0;
                end
            4'b0100:
                begin
                    qe = 4'b1000;
                    st = 0;
                    qt = 0;
                end
            4'b0101:
                begin
```

```
                    qe = 4'b0100;
                    st = 0;
                    qt = 0;
                end
            4'b0110:
                begin
                    qe = 4'b0010;
                    st = 0;
                    qt = 0;
                end
            4'b0111:
                begin
                    qe = 4'b0001;
                    st = 0;
                    qt = 0;
                end
            4'b1110:
                begin
                    qe = 4'b0000;
                    qt = 1;
                    st = 0;
                end
            4'b1111:
                begin
                    qe = 4'b0000;
                    qt = 1;
                    st = 1;
                end
            default:
                begin
                    qe = 4'b1100;
                    st = 0;
                    qt = 0;
                end
        endcase
    end
end
assign QE = qe;
assign Qt = qt;
assign St = st;
endmodule
```

```
module SARLogic(
       input   clk,   // clock input
       input   rst,   //reset
       input   go,   // go=1 to perform conversion / like EN signal
       output   valid,   // valid=1 when conversion finished
       output  [7:0]  result,  // 8 bit result output
       output  [7:0]  value,   // to DAC
       input   cmp   // comparator output
       );

 reg  [7:0]  result;  // hold partially converted result
 reg  [3:0]  c;
 reg    c2;


always @(posedge clk or posedge rst) begin
    if (rst) begin
        result = 8'b00000000;
        c = 4'b1001;
        c2 <= 0;
    end
    else if (go) begin
        result = 8'b10000000;
        c = 4'b1000;
        c2 <= 0;
    end
    else begin
        if (~cmp) result[c-1] = 0;
        if (c2) begin
            result = 8'b10000000;
            c = 4'b1000;
            c2 <= 0;
        end
        else if (c == 4'b0001) begin
            c2 <= 1;
        end
        else begin
            c = c - 1;
            result[c-1] = 1;
        end
    end
end
assign valid = c2;
endmodule
```

```
module I2C_slave(
       input [6:0] I2C_ADR,
       inout SDA,
       input SCL,
       input [7:0] IOin,
       output [7:0] IOout,
       output ACK
       );
wire SDA_shadow;
wire start_or_stop;

// I2C start and stop conditions detection logic
`ifdef Xilinx
    BUF mybuf(.O(SDA_shadow), .I((~SCL | start_or_stop) ? SDA : SDA_shadow));
    BUF SOS_BUF(.O(start_or_stop), .I(~SCL ? 1'b0 : (SDA ^ SDA_shadow)));
`else
    assign SDA_shadow = (~SCL | start_or_stop) ? SDA : SDA_shadow;
    assign start_or_stop = ~SCL ? 1'b0 : (SDA ^ SDA_shadow);
`endif
reg incycle;
always @(negedge SCL or posedge start_or_stop)
if(start_or_stop) incycle <= 1'b0;
else if(~SDA) incycle <= 1'b1;

// Count the I2C bits coming in
reg [3:0] bitcnt;  // Counts the I2C bits from 7 down to 0, plus an ACK bit
wire bit_DATA = ~bitcnt[3];  // DATA bits are the first 8 bits sent
wire bit_ACK = bitcnt[3];  // ACK bit is the 9th bit sent
reg data_phase;

always @(negedge SCL or negedge incycle)
if(~incycle) begin
    bitcnt <= 4'h7;  // bit 7 is received first
    data_phase <= 1'b0;
end
else begin
    if(bit_ACK) begin
        bitcnt <= 4'h7;
        data_phase <= 1'b1;
    end
    else
        bitcnt <= bitcnt - 4'h1;
end

// Detect if the I2C address matches
wire adr_phase = ~data_phase;
reg adr_match, op_read, got_ACK;
reg SDAr;
always @(posedge SCL) SDAr <= SDA;  // sample SDA on posedge
reg [7:0] mem;
wire [7:0] mem2;
wire op_write = ~op_read;

always @(negedge SCL or negedge incycle)
if(~incycle) begin
    got_ACK <= 1'b0;
    adr_match <= 1'b1;
    op_read <= 1'b0;
end
else begin
    if(adr_phase & bitcnt==7 & SDAr!=I2C_ADR[6]) adr_match <= 1'b0;
    if(adr_phase & bitcnt==6 & SDAr!=I2C_ADR[5]) adr_match <= 1'b0;
    if(adr_phase & bitcnt==5 & SDAr!=I2C_ADR[4]) adr_match <= 1'b0;
```

```
    if(adr_phase & bitcnt==4 & SDAr!=I2C_ADR[3]) adr_match <= 1'b0;
    if(adr_phase & bitcnt==3 & SDAr!=I2C_ADR[2]) adr_match <= 1'b0;
    if(adr_phase & bitcnt==2 & SDAr!=I2C_ADR[1]) adr_match <= 1'b0;
    if(adr_phase & bitcnt==1 & SDAr!=I2C_ADR[0]) adr_match <= 1'b0;
    if(adr_phase & bitcnt==0) op_read <= SDAr;
    if(bit_ACK) got_ACK <= ~SDAr;  // Monitor ACK to free bus when master doesn't ACK

    if(adr_match & bit_DATA & data_phase & op_write) mem[bitcnt] <= SDAr;//Memorywrite
end

// drive the SDA line when necessary.
wire mem_bit_low = ~mem2[bitcnt[2:0]];
wire SDA_assert_low = adr_match & bit_DATA & data_phase & op_read & mem_bit_low &
got_ACK;
wire SDA_assert_ACK = adr_match & bit_ACK & (adr_phase | op_write);
wire SDA_low = SDA_assert_low | SDA_assert_ACK;
assign SDA = SDA_low ? 1'b0 : 1'bz;

assign mem2 = IOin;
assign IOout = mem;
assign ACK = bit_ACK & op_read;
endmodule
```

```
module SAR_CDC_Digital2(
     input CLK,
     input rst,
     input Cmp_In,
     input Cmp_In2,
     input SCL,
     inout SDA,
     input [1:0] I2C_ADR_bits,
     output [7:0] Q,
     output [7:0] Qf,
     output [3:0] QE,
     output EXC,
     output EXCN,
     output T1,
     output T2,
     output T3,
     output T4,
     output Qfr,
     output Clock,
     output Clock2,
     output RESET,
     output RESET2,
     output VALID,
     output SS,
     output QS,
     output Qt,
     output St,
     output EXCt
    );
wire [6:0] I2C_ADR;
wire [7:0] data;
wire [7:0] MS;
wire valid;
wire Cmp;
wire clk;
wire rst_sar;
wire SQ;
wire S;
wire SQrst;
wire Qfrst;

reg [7:0] dataMUX;
reg [7:0] Qmem;
reg [7:0] Qfmem;
reg SD;
reg [3:0] QEc;
reg rst_ms;
reg rst_ms2;
reg rst_ms3;
reg rst_max;
reg rst_max2;
reg V;
reg V1;
reg [1:0] c;
reg [1:0] c1;
reg Ack;
reg QSreg;

ClockSignals ClockSignals(
            .clk(CLK),
            .rst(reset),
            .hold(VALID),
            .Ack(Ack),
```

```
            .EXC(EXC),
            .EXCN(EXCN),
            .T1(T1),
            .T2(T2),
            .T3(T3),
            .T4(T4),
            .Qfr(Qfr),
            .Clock(Clock),
            .RESET(RESET),
            .RESET2(RESET2),
            .Clock2(Clock2),
            .S(S)
);
ModeSelect ModeSelect(
            .clk(Clock|rst),
            .rst(rst),
            .S(MS),
            .QE(QE),
            .St(St),
            .Qt(Qt)
);
SARLogic SARLogic(
            .clk(clk),
            .rst(reset|rst_max2),
            .go(rst_sar),
            .valid(valid),
            .result(data),
            .value(),
            .cmp(Cmp)
);
I2C_slave I2C_slave(
            .I2C_ADR(I2C_ADR),
            .SDA(SDA),
            .SCL(SCL),
            .IOin(dataMUX),
            .IOout(MS),
            .ACK(SQ)
);
//Switch data to be read from Q to Qf on Ack
always @(posedge SQrst) begin
    if (rst) begin
        c <= 2'b0;
        SD <= 0;
    end
    else if (c ==2'b0) begin
        dataMUX <= Qmem;
        SD <= 0;
        c<=c+1;
    end
    else if (c ==2'b01) begin
        dataMUX <= Qfmem;
        SD <= 1;
        c<=c+1;
    end
    else if (c ==2'b10) begin
        dataMUX <= Qmem;
        SD <= 0;
        c <= 2'b0;
    end
    else begin
        dataMUX <= Qmem;
        SD <= 0;
        c<=2'b0;
```

```
    end

end
assign SS = SD;
//Assign data from SAR logic to Qmem or Qfmem depending on coarse or fine phase S
always @(posedge CLK) begin
    if (rst) begin
        Qmem = 8'b0;
        Qfmem = 8'b0;
    end
    else begin
        if (S == 0) Qmem = data;
        if (S == 1) Qfmem = data;
    end
end
//Check if fine conversion is out of range
always @(posedge CLK) begin
    if ((dataMUX == 8'hFF|dataMUX == 8'h00) & (SS == 1) ) rst_max <= 1;
    else rst_max <= 0;
end
always @(negedge clk) begin
    if ((data == 8'hFF|data == 8'h00) & (Qf == data) & (c[1] == 1) ) rst_max2 <= 1;
    else rst_max2 <= 0;
end
assign Cmp = S ? Cmp_In2 : Cmp_In;//Switch comparator input depending on phase
assign clk = S ? Clock2 : EXC;//Switch clock to SAR logic depending on phase
assign rst_sar = S ? RESET2 : RESET;//Switch SAR logic enable depending on phase
//Check if mode select has changed
always @(posedge CLK) begin
    if (QE!=QEc) begin
        rst_ms <= 1;
        QEc <= QE;
    end
    else begin
        rst_ms <= 0;
        QEc <= QE;
    end
end
always @(posedge CLK) begin
    if (~SS) begin
        if (rst_ms & ~rst_ms2) rst_ms2 = 1;
    end
    else rst_ms2 = 0;
    if (rst_ms2) rst_ms3 = 1;
    if (rst|Ack) rst_ms3 = 0;
end
//Send Ack to ClockSignals when done reading data
always @(posedge CLK) begin
    if(rst) Ack = 0;
    else begin
        if(c[1] & V) Ack = 1;
        else Ack = 0;
    end
end
always @(Qfrst) begin
    if (rst) V = 0;
    else begin
        if(Qfr & Clock2) V = 1;
        else V = 0;
    end
end
always @(posedge CLK) begin
    if (rst|~RESET) V1 = 0;
```

```
    else if (Ack) V1 = 1;
end
//Switch position of coarse conversion capDAC depending on electrodes enabled
always @(posedge CLK) begin
    if (rst) QSreg = 0;
    if (data == 8'b0 && S == 0 && EXCN == 1) begin
        case (QE)
            4'b1100: if (~Cmp_In) QSreg = ~QSreg;
            4'b0011: if (~Cmp_In) QSreg = ~QSreg;
            4'b1000: QSreg = 1;
            4'b0100: QSreg = 0;
            4'b0010: QSreg = 1;
            4'b0001: QSreg = 0;
            default: QSreg = 0;
        endcase
    end
end
assign reset = rst|(rst_ms3 & SS)|rst_max;
assign Q = S ? Qmem : data;
assign Qf = ~S ? Qfmem : data;
assign VALID = valid & ~Ack & V & ~V1;
assign I2C_ADR = {5'b00011,I2C_ADR_bits};
assign SQrst = SQ|rst;
assign Qfrst = Qfr|rst;
assign QS = QSreg;
assign EXCt = St ? EXC : 0;//Excitation signal for test DAC
endmodule
```

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