ABSTRACT

Title of dissertation: NOVEL TUNNELING DIODES FOR A HIGH PERFORMANCE INFRARED RECTENNA

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Since the 1960s, metal-insulator-metal (MIM) tunneling diodes have been used for detecting and mixing electromagnetic waves up to infrared frequencies. To improve the wave coupling efficiency, an antenna is usually integrated with a MIM diode, and this integrated structure is known as a "rectenna" which can rectify incident waves. Although antenna coupled MIM diodes can detect and rectify infrared waves, the energy conversion efficiency of these structures is usually very low largely because of the response time of the tunnel junction. This thesis summarizes an attempt to improve the power conversion efficiency of the rectenna. As a result, novel tunneling diodes have been developed using a geometric field enhancement (GFE) technique, which takes advantage of the "lightning rod" effect. The GFE technique is implemented by using a pointed electrode, creating an asymmetric electric field in the region of the tunnel barrier. Thus, the tunneling current in this system can be asymmetric with respect to the sign of the applied bias. Furthermore, the geo-

metric structure of these novel optical rectennas provides the appropriate conditions for the excitation of surface plasmon resonances. These resonances further enhance the junction's electric field, allowing for larger current flow, effectively lowering the diodes tunneling resistance.

Three different types of tunneling diodes are developed and explored in this research: a perfect planar type tunneling diode, an asymmetric tunneling diode (ATD), and a focused asymmetric metal-oxide-metal (FAMIM) tunneling diode. The fabrication processes for each new tunneling diode have been successfully developed. The degree of performance improvement achieved by each process is summarized. This thesis documents the highest MIM detection sensitivities of 31 V^{-1} and 22 V^{-1} reported in open literature for planar type tunneling diodes and ATDs, respectively. Improvements in tunneling current nonlinearity (curvature of the current-voltage plot) of 350 % and 33 % are achieved for ATDs and FAMIM diodes, respectively.

NOVEL TUNNELING DIODES FOR A HIGH PERFORMANCE INFRARED RECTENNA

by

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Dissertation submitted to the Faculty of the Graduate School of the
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Dedication

To my loving wife and parents.

To my beautiful daughter.

To my wise brother and sister.

Acknowledgments

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Sincerely,

Kwangsik Choi

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Chapter 1

Introduction

1.1 A History of the MIM Diode

Metal-Insulator-Metal (MIM) tunneling diode research started in the 1960s [1]. Early MIM tunneling diodes consisted of a sharp metal tip on a planar metal surface with a thin insulation layer or air gap between the two metal electrodes. This was a variant of the "cat's whisker" or point-contact diode. The early MIM tunneling diodes showed good performance for detecting and mixing high frequency waves up to infrared (IR) range [2, 3, 4, 5, 6]. However, there were some drawbacks: it was not easy to reproduce devices, and diodes were mechanically fragile.

A new type of MIM diode was developed to overcome those limitations using thin film technologies. The initial thin film MIM diodes were developed by Gustafson and Bachner in 1974 [7, 8]. Compared with the earlier point-contact diodes, thin film techniques, such as thin metal or oxide deposition, provided some degree of process reproducibility. The two dimensional structure of a thin film MIM diode makes integration with popular CMOS technologies easy. Furthermore, control over oxide thickness allows for enhanced reliability.

The main research issues in thin film MIM tunneling diode research revolve around reducing tunnel junction size, integrating a properly coupled antenna with a tunnel junction, developing and optimizing a tunneling diode manufacturing pro-

cess, and developing techniques to improve the performance of the tunnel junctions. The requirements for successful junction scaling, though, were contradictory. For example, it is very important to achieve a small junction area, because the junction area defines the junction capacitance. Junction area also defines diode tunneling resistance (larger area, lower resistance). The capacitance and resistance limit the operation speed of a tunneling diode. Heiblum's tunneling diode was a model, showing how researchers had to handle the scaling issue [9]. We need small junction capacitance (small junction area) and low junction tunneling resistance (large junction area). The problem of making small junction area has been dramatically solved by using e-beam lithography [10, 11]. Most MIM tunneling diodes are fabricated using by e-beam lithography to achieve a small junction size. But we must find techniques for decoupling junction capacitance from junction tunneling resistance. This decoupling is the subject of this thesis. In addition, other factors affect our ability to rectify high frequency electromagnetic radiation. Specifically, the diode current-voltage (I-V) relationship must be asymmetric. That is, it must resemble an ideal diode with ultra-low turn on voltage to the maximum extent possible.

One popular approach to achieve this is using dissimilar electrodes materials. The related theory has been established in 1960s by Simmons [12]. Dissimilar electrodes create different tunneling barrier height at each electrode due to the work-function difference. As a result, a built-in potential is created in a tunneling barrier without any external bias supply. This material asymmetry leads to I-V asymmetry. As we shall show, this improves the demodulation efficiency of the MIM diodes. Furthermore, an ideal MIM diode will be highly nonlinear in the forward bias case.

Of course, in addition to the materials issues just described, antenna design and matching considerations are important as well. Hobbs and et. al. have stressed the importance of these design issues. They have used a wave guide for shorter wave detection, 1.6 um [13]. In this approach, the coupling efficiency could be improved through the wave guide instead of improving diode performances. Except these two cases, there are no other developed techniques. That is, the absence of proper techniques in thin film tunneling diodes is retarding their progress.

Three different types of antenna (dipole, bowtie, and spiral) have been integrated and tested with MIM diodes [11, 10, 14]. It now appears that there are no other choices but these three antenna types. In addition to the antenna type, some researchers have focused on geometric antenna design at infrared frequencies. The fundamental issue related to the integrated antenna is the validity of classic antenna theory at infrared frequencies. Some practical research results about such antenna design have come from the optical antenna area [15, 16].

1.2 Thesis Outline

This thesis is composed of seven chapters, and various topics related to thin film tunneling didoes are covered mostly based on the rectifying operation aspects. Chapter 1 is the introduction of this thesis and includes the history of MIM diodes, the motivation and objective of this research, the thesis outline, and the contribution.

Chapter 2 covers the physics of tunneling diodes. It starts with the tunneling

current through a tunneling barrier and leads to the rectifying mechanism of tunneling diodes. Fundamental characteristics of tunneling diodes are described based on the physics and the equivalent circuit model, and conventional infrared rectenna implemented with a thin film MIM tunneling diode and an integrated antenna is introduced. Other important issues such as tunneling time and energy conversion efficiency are also discussed in this chapter.

In chapter 3, after reviewing the structure of conventional thin film tunneling diodes, a new technique is introduced, the geometric field enhancement (GFE) technique, to provide a MIM tunneling diode with unique asymmetric current characteristics and superior performance. The advantages obtained are explored.

Chapter 4 describes the mechanism of near field enhancement through surface plasmon resonance in tunneling diodes. This near field enhancement is one of the advantages derived from the GFE technique. This chapter includes the basic concepts of surface plasmon (SP) generation and surface plasmon resonance (SPR). Furthermore, optical antennas are introduced as an example of a practical application of SPRs, and it is explained how the near field enhancement can be applied to enhance the performance of tunneling diodes.

Chapter 5 covers the fabrication processes of novel tunneling diodes developed in this research. Three different types of new tunneling diodes are developed. The first diode is called a planar type tunneling diode. This diode has significant importance in that a perfect planar tunneling structure has been established in thin film tunneling diodes for the first time. The diode is designed to have the structure of optical antenna so that very strong near field enhancement is expected inside

the tunneling barrier. During the process development, a boiling water oxidation process was developed and used for this diodes.

As the second type of diode, asymmetric tunneling diodes are presented in chapter 5. This diode is implemented by applying the GFE technique to a poly-Si electrode to achieve asymmetric tunnel current. The tunneling barrier is implemented by the boiling water oxidation process again. Simple overlap tunneling diode fabrication is also explained here. It is prepared to verify the origin of asymmetric tunneling current.

The third type of diode is described in the last part of chapter 5. This diode is referred to as a focused asymmetric metal-insulator-metal (FAMIM) tunneling diode and developed by applying the GFE technique to achieve an asymmetric tunneling diode. Besides to the FAMIM diode fabrication, various process techniques, tested and applied to the FAMIM diodes to improve diode performances, are explored such as electrode patterning, metal oxidation process, and plasmon grating integration.

Chapter 6 provides the characteristics and performances of the new diodes introduced in chapter 5. The diode characterization is performed through DC current-voltage measurements at room (300K) and low (77K) temperature and RF(radio frequency) rectification tests. The benefits or effects of the GFE technique on tunneling didoes are demonstrated based on data analysis and parameter extraction, and other basic characteristics of tunneling diodes are explored in this section.

Chapter 7 concludes this new tunneling diode research. This chapter summarizes the research work and achievements of the developed novel tunneling diodes study. Future works are also addressed, so that further research can be extended

based on this thesis.

Appendix A includes the process descriptions for each tunneling diode developed in this research.

1.3 Contributions of This Thesis

The invention of the GFE technique is the most critical and significant contribution of this research because it helps to remove the inherent barriers which are induced by material properties and by the absence of applicable techniques. The representative characteristic of the GFE technique is generating asymmetric tunneling current in a symmetric metal-insulator structure. This asymmetric current is the first demonstration in thin film tunneling diodes with the same metal electrodes. The details of benefits from the GFE technique are listed below.

- reducing tunneling resistance
- increasing nonlinearity
- enhancing the effective amplitude of the AC signal
- improving zero bias performance
- merging with dissimilar electrodes method
- using near field enhancement by surface plasmon resonances

Furthermore, a perfect planar type of tunneling diode has been demonstrated. This diode might be the best choice to maximally use the near field enhancement through surface plasmon resonances. The perfect planar tunneling structure is also the first implementation in thin film tunneling diodes.

The last contribution of this research is developing a new oxidation process using a boiling water process. This process is not only simple, easy, and cheap, but also it provides a robust tunneling barrier between tunneling electrodes.

Chapter 2

MIM Tunneling Diode Physics

2.1 Tunneling Current

The main mechanism responsible for current transport in the MIM diode is tunneling. Energy band diagrams provide a simple and useful way to describe the current characteristics in a MIM structure. Figure 2.1 shows the energy band diagram of a MIM diode with the same metals used for the two electrodes, E_F is the Fermi level of metal, φ is the barrier height, and "d' is the tunneling barrier thickness. The Fermi levels are located at same position without external bias, as shown in Figure 2.1(a), so that there is no net current flow between two electrodes. The current flow in this structure can be achieved in two ways: thermionic emission over the barrier and tunneling through the barrier. These are described more fully, below.

When a high electric field is applied across the insulator, as shown in Figure 2.1(d), the potential barrier height is reduced by the Schottky effect through an image-force [17]. This lowering creates a net current flow, called Schottky emission. Furthermore, carriers can obtain enough thermal energy to surmount the barrier without considering barrier lowering. This is called thermionic emission, which exhibits a strong dependence on temperature. So, such thermionic emission always exists in a tunneling barrier having thin oxides and low barrier height.

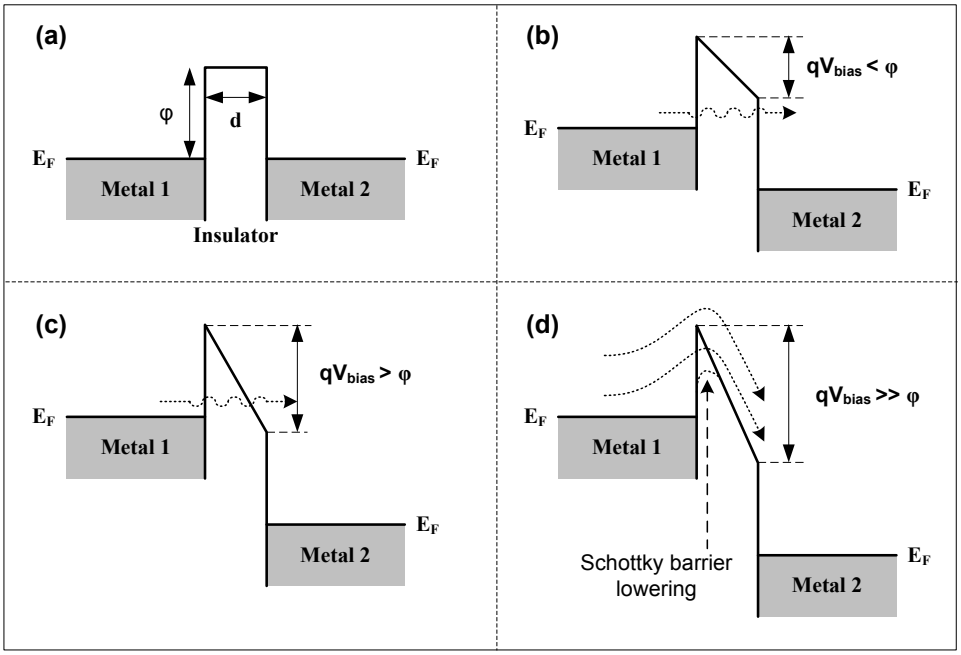

Figure 2.1: Energy band diagram of a MIM diode with same metal electrodes (Metal1 = Metal2 . (a) Zero bias condition, (b) Direct tunneling at small positive bias, (c) Fowler-Nordheim (FN) tunneling at intermediate positive bias. (d) Thermionic emission over the barrier including Schottky effect at high positive bias.

Tunneling through a potential barrier is described by quantum mechanics. When the barrier thickness is very thin (usually below 4 nm), there are tunneling currents between two electrodes in both directions at equilibrium condition (Vbias = 0). These currents, of course, cancel yielding zero net current. At low-biases, shown in Figure 2.1(b), electron tunneling from metal 1 to metal 2 is dominant, creating net current flow. The current is increased at a higher bias condition because the tunneling probability is proportional to applied potential. This tunneling current does not have a strong temperature dependence [12]. We should note that tunneling current is seriously decreased when the barrier thickness exceeds 4nm [18]. The

insulation layer needs to be thinner than 4 nm for proper device operation. As the applied bias is higher than the barrier height, the effective tunneling barrier thickness starts decreasing, as shown in Figure 2.1(c). This situation is called Fowler-Nordheim Tunneling [19].

Under light illumination, another process of tunneling current at MIM diodes is known as photo-assisted tunneling. Electrons absorbing photon energy near the tunnel junction can surmount the potential barrier, generating current flow. However, this photo-assisted current is usually much weaker than the other previous processes mainly due to tiny tunnel junction area. Therefore, it can be ignored for the net current of MIM tunneling diodes.

The current-voltage relation in a MIM diode is described by the Simmons's formula [18],

$$J = \frac{6.2 \cdot 10^{10}}{\beta \Delta s} \cdot \{\bar{\varphi} \cdot \exp[-1.025\beta\Delta s\bar{\varphi}^{1/2}] - (\bar{\varphi}+V) \cdot \exp[-1.025\beta\Delta s(\bar{\varphi}+V)^{1/2}]\} \quad (2.1)$$

where $\bar{\varphi}$ is the mean barrier height of the insulator, V is the voltage across the barrier, β is a correction factor, and Δs is the barrier thickness. This formula may be modified to include image force barrier lowering. These modifications are derived in [18]. For very high voltage, V > (φ_0+E_F/q) , Eq. (2-1) reduces to the Fowler-Nordheim equation [17].

Using Eq. (2-1), for a rectangular potential barrier including image force effect, a simple polysilicon-SiO_2-polysilicon tunneling current is simulated with 15 Å oxide thickness and 60 nm^2 junction area at room temperature. With these simulation conditions, thermal current is also derived using data supplied in [12]. Figure 2.2

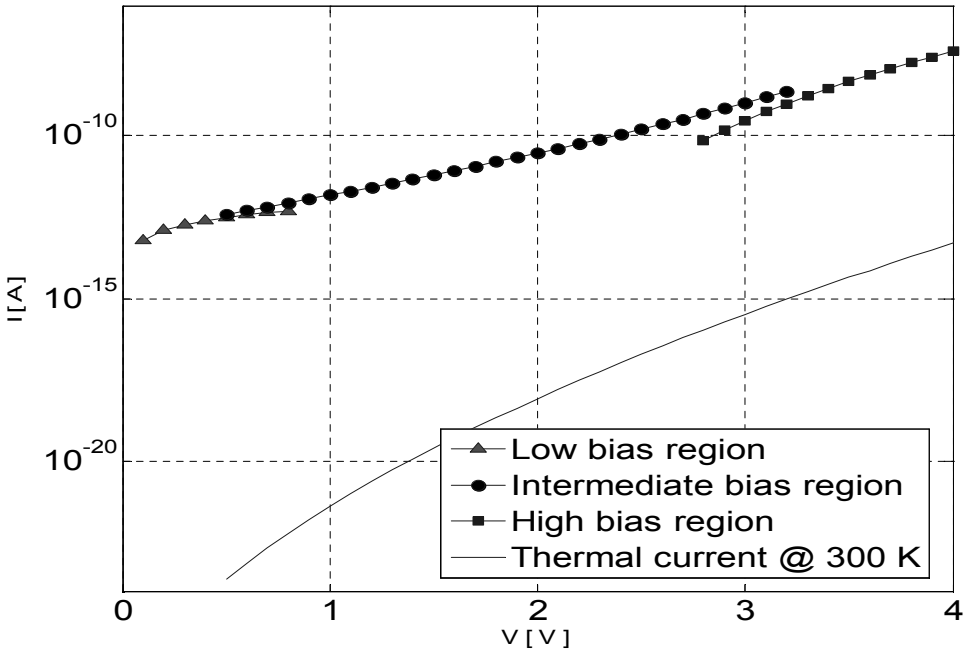

Figure 2.2: Simulated tunneling and thermal current for a polysilicon-SiO_2-polysilicon tunneling structure of 15 Å barrier thickness and 60 nm^2 tunneling junction area. Tunneling currents are extracted using Eq. (2.1) for low, intermediate, and high bias region.

shows the result for the tunneling and thermal current of the tunneling structure at 300 K. As the barrier thickness is increased, the tunneling current is decreased and the thermal current is increased. Also, the tunneling and thermal currents reach almost the same level at around 40 Å barrier thickness.

2.2 Rectifying Operation

Rectification in MIM diodes is the result of the nonlinearity of tunneling current. The relationship between AC voltage signal ($|v_{ac}|$) in a tunnel junction and rectified DC voltage (V_{rect}) and current (I_{rect}) are expressed by [20]

$$V_{rect} = \frac{1}{4} \cdot \frac{I''(V_{BIAS})}{I'(V_{BIAS})} \cdot |v_{ac}|^2 = \frac{1}{4} \cdot S \cdot |v_{ac}|^2 \tag{2.2}$$

$$I_{rect} = \frac{1}{4} \cdot I''(V_{BIAS}) \cdot |v_{ac}|^2 \tag{2.3}$$

where $\mathrm{I}'(V_{BIAS})$ and $\mathrm{I}''(V_{BIAS})$ are the first and second derivatives of tunneling current at a certain DC bias point (V_{BIAS}), respectively, $|v_{ac}|$ is the magnitude of the AC voltage signal in a tunneling diode, and the S is the sensitivity defined as the ratio of $\mathrm{I}''(V_{BIAS})$ to $\mathrm{I}'(V_{BIAS})$. These voltage and current parameters are two of the main quality factors for rectifying diode performance. They are derived from a Taylor-expansion of the static current-voltage relationship of a tunneling diode. As explicitly shown in Eq. (2.2) and (2.3), to improve rectifying performance of a MIM tunneling diode, one must increase AC voltage signal ($|v_{ac}|$), nonlinearity or curvature of tunneling current-voltage curve (I''), and differential resistance ($1/\mathrm{I}'$) of a MIM diode.

2.3 MIM Diode Model

Consider a simple MIM diode equivalent circuit model, consisting of a junction capacitance, C_D, and a diode tunneling resistance, R_D. The cutoff frequency of such a single pole MIM rectifier is expressed by,

$$f_c = \frac{1}{2\pi R_D C_D} \tag{2.4}$$

where the junction capacitance (C_D). This can be derived using

$$C_D = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{2.5}$$

where ε_0 is the free space permittivity, ε_r is the relative permittivity of insulator, "d" is the barrier thickness, and A is the junction area. The diode resistance can be extracted by a simple DC I-V measurement. Assuming the diode resistance is linearly proportional to the ratio of barrier thickness to junction area (d/A), the cutoff frequency of MIM diodes is defined by tunneling resistivity only. Therefore, high conductivity at given frequency is essential for MIM diodes. This explanation is based on an assumption that the entire junction area conducts uniformly. In real diodes, sharp corners or edges transfer most currents, and a relative permittivity of a ultra thin oxide film can be different from the relative permittivity of a bulk oxide. Besides, a relative permittivity is a function of frequency. So, the exact diode resistance and capacitance cannot be calculated using only simple geometric parameters. More details about contact resistance can be found in reference [21]. However, simple I-V extraction methods could provide a reasonable initial value for each parameter.

2.4 Tunneling Time

Tunneling time is the mean time that an electron takes to tunnel through a barrier. When it is not much shorter than the MIM diode's RC time constant, it must be considered to describe the device operation speed of the diode. Although

there were many attempts to derive a meaningful formula for the tunneling time, this "simple" problem has not been fully solved yet [22, 23]. However, the tunneling time can be estimated to be below 10^{-15} s (through experiments and theoretical approaches [9, 24, 25]). Considering an infrared wave of 20 μm wavelength, the wave periode is about 5.6×10^{-15} sec in a vacuum. Therefore, it can be concluded that the entire response time of the MIM tunneling junction is limited not by the tunneling time itself but by other external factors such as a RC delay time. Based on this tunnel-time estimate, it appears that MIM diodes can operate at near infrared frequencies before the tunneling time limits set in.

2.5 Antenna Coupled MIM Diode

An antenna is a transducer designed to transmit or receive electromagnetic waves effectively, and it can be used for coupling incident waves into a detector, such as bolometer or MIM diode [11, 26, 27, 28]. Generally, a bowtie or dipole antenna is integrated with MIM diodes to couple incident waves. Figure 2.3 shows the two different types of antenna integrated with a MIM tunneling diode [11, 29]. It appears that a bowtie antenna is the more attractive option to be integrated with a tunnel junction diode. The triangle shape not only provides a geometric field enhancement effect, but it also makes use of field enhancement from surface plasmon resonances (as discussed in the Introduction). The surface plasmon aspect is to be discussed further in chapter 3. Also, bowtie antennas provide a broad bandwidth, and the fabrication process is also simple.

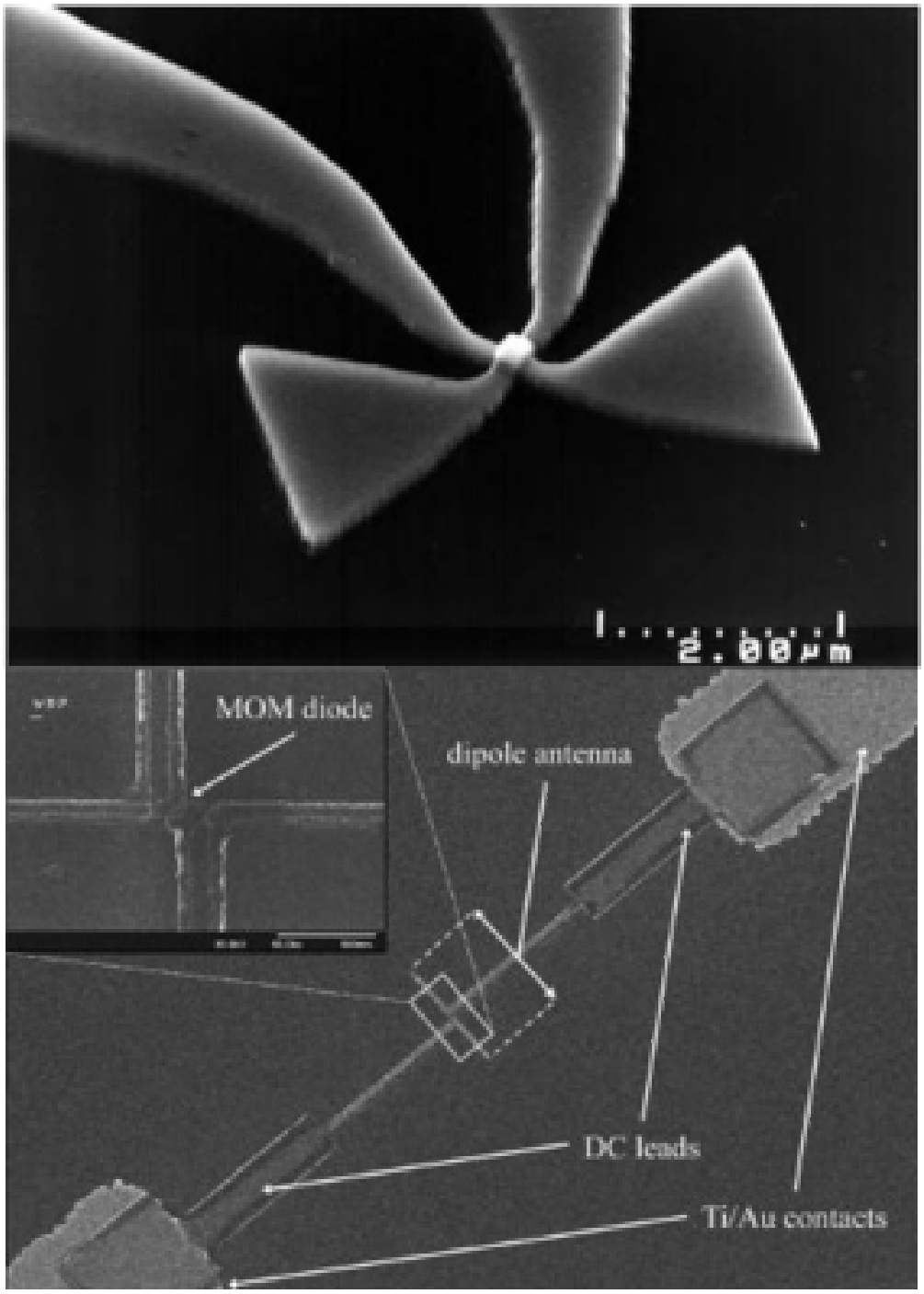

Figure 2.3: Antenna coupled MIM tunneling diodes: a bowtie antenna is integrated into a MIM tunneling diode (top) [11], and a dipole antenna is integrated into a MIM tunneling diode (bottom) [32].

The impedance of an infinite bowtie antenna is derived using a conformal mapping method, which transforms a two-dimensional boundary problem into a simpler equivalent problem [30]. In such analysis, the bowtie shape is converted to coplanar strips. The impedance of a coplanar strip is expressed as

$$Z = \frac{\eta_0}{\sqrt{\varepsilon_{eff}(f)}} \cdot \frac{K(k)}{K'(k)} \tag{2.6}$$

where ε_{eff} is the effective permittivity, $K'(k)$ is an elliptic integral of the first kind, and k is the bowtie flare angle [31]. To get the numerical impedance value of an infinite bowtie antenna, we need to know the effective permittivity (ε_{eff}) of the antenna. At low frequency, the permittivity of a conductor on a substrate usually has a constant value. However, conductivity increases up to the value of the substrate as the frequency goes up. Generally, this phenomenon is continued in the infrared range. The effective permittivity for coplanar strips is to be obtained by a useful empirical formula, verified through experiments,

$$\sqrt{\varepsilon_{eff}(f)} = \sqrt{\varepsilon_q} + \frac{\sqrt{\varepsilon_r} - \sqrt{\varepsilon_q}}{1 + a(\frac{f}{f_{TE}})^{-b}} \tag{2.7}$$

where ε_q is the quasi-static effective permittivity expressed by ε_q=(ε_r+1)/2, a is a geometry parameter of the transmission line, b is a fixed constant of 1.8, and f_{TE} is the surface wave TE1 mode cutoff frequency, expressed as

$$f_{TE} = \frac{c}{4d\sqrt{\varepsilon_r - 1}} \tag{2.8}$$

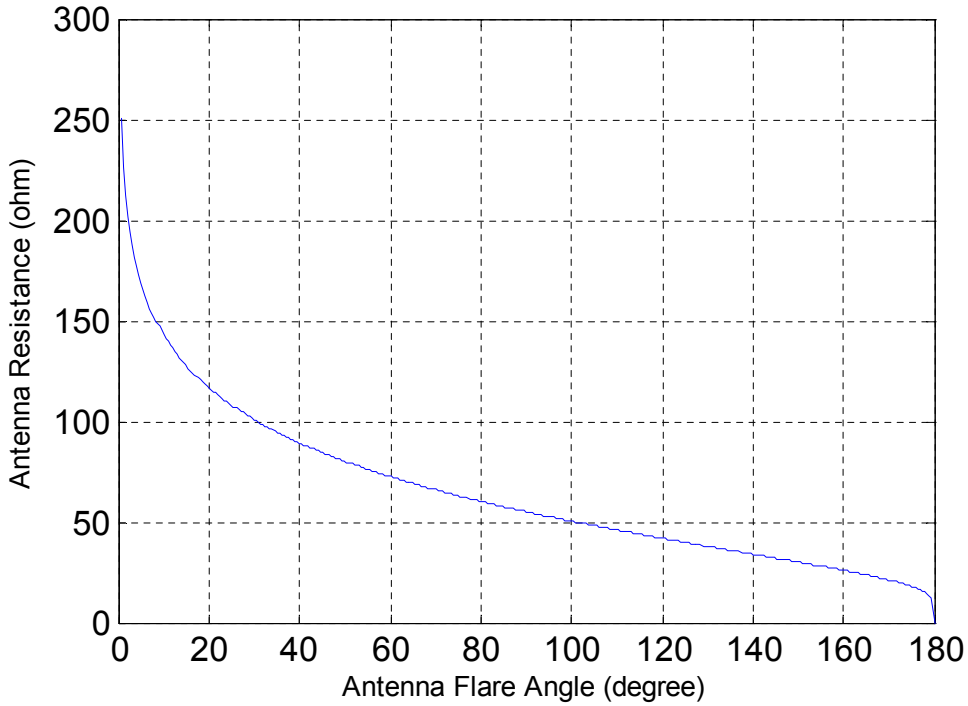

Figure 2.4: Antenna resistance vs. flare angel of polysilicon bowtie antenna at wavelength 10.6 μm.

with the substrate or dielectric thickness of d [31, 32].

Eq. (2.6) is plotted with a variable of flare angle in Figure 2.4 using specific parameter values from the references assuming that effective permittivity of a poly-Si at 28 THz is same of its quasi-static value of Si. Therefore, we use $\varepsilon_{eff,Si}$=$\varepsilon_{r,Si}$=11.7 for 10.6um wavelength. The impedance is about 80 Ω for a bowtie antenna with 45° flare angle on a 430 um thick Silicon substrate at 10.6 um wavelength, 28 THz. This antenna impedance should be considered during impedance matching between an antenna and a tunneling junction diode.

2.6 Energy Conversion Efficiency

Kale described the conversion efficiency of tunneling diodes [33], and Hobbs restated the efficiency factors using recent developed MIM tunneling diodes [13]. The conversion efficiency (η) is conceptually expressed by

$$\eta = \eta_a \eta_c \eta_m \eta_q \tag{2.9}$$

where η_a is the antenna efficiency, η_c is the another antenna efficiency related to the antenna material, η_m is the matching efficiency between antenna and tunneling diode impedance, and η_q is the quantum efficiency of tunneling diode [13, 33]. The antenna efficiency (η_a) is the ratio of the collected power to intercepted power by an antenna. Antenna efficiency is related to antenna resonances at the given wavelengths. The efficiency η_c is related to the conductance of the antenna material. At low frequency, metals can usually be considered to be perfect conductors. However, as the frequency increases, the perfect conductor devolves to a lossy medium. The loss is more serious as frequency increases. A low loss metal must be selected to achieve high η_c. The matching efficiency (η_m) can be maximized when the antenna resistance equals to the tunneling junction resistance. The quantum efficiency (η_q) is defined by a ratio of generated electrical power to incident optical power. In MIM diodes, the quantum efficiency is directly related with current responsivity or sensitivity, and expressed by

$$\eta_q = \frac{h\nu}{q}\beta_i \tag{2.10}$$

where h is Plancks constant, ν is angular frequency, q is electron charge, and β_i is the current responsivity of MIM diodes. The current responsivity can be expressed by

$$\beta_i = \frac{rectified\ current}{input\ power} = \frac{I''}{2I'} = S/2 \tag{2.11}$$

where I' and I'' are the first and second derivative of a MIM tunneling diode at a given bias point respectively, and S is the sensitivity of a MIM diode. Therefore, high sensitivity is necessary for the high quantum efficiency. Hobbs reported a quantum efficiency of 6 %, which is the highest quantum efficiency ever reported for MIM diodes [13].

For high energy conversion efficiency, two fundamental design requirements must be satisfied in a tunneling diode: thin tunneling barrier thickness and low tunneling barrier height. As addressed above, increasing tunneling conductivity is the most important factor. First, high tunneling conductance or current improves current curvature, and this results in higher sensitivity. Considering the small radiation resistance of bowtie antenna simulated before, better impedance matching condition can be achieved through the low tunneling resistance. That is, more power can be transferred from antenna to tunnel junction.

Chapter 3

Geometric Field Enhancement (GFE) Technique

3.1 Conventional Diodes and Dissimilar Metal Electrodes

Conventional thin film MIM tunneling diodes have a simple overlap structure consisting of two metal lines[10, 11, 34]. Specific examples of this configuration are shown in chapter 2. Row A in Figure 3.1 shows the schematic of a tunnel junction structure employed for "conventional" MIM diodes, and their associated energy band diagrams under different bias conditions are shown again. Here, even if the two electrodes are implemented using the same metal, there is some work-function difference on either side of the insulator, as shown in Figure 3.1 (A-2). Hobbs explained this tunneling barrier lowering as a result of a more abrupt junction at the interface of the 2nd electrode side [35] induced by processing differences for the two electrodes. Due to the inherent work-function difference, the forward tunneling current becomes bigger than the reverse one. The thicker arrow line in Figure 1 (A-3) describes this situation. (**Note, the bias polarity and the current transport direction in this research are defined as shown in the Figure 3.1. So, forward tunneling current means that electrons are tunneling from the second electrode to the first electrode, and reverse tunneling current means the opposite. Therefore, the reverse biasing condition is able to generate higher currents compared to the forward biasing condition.**)

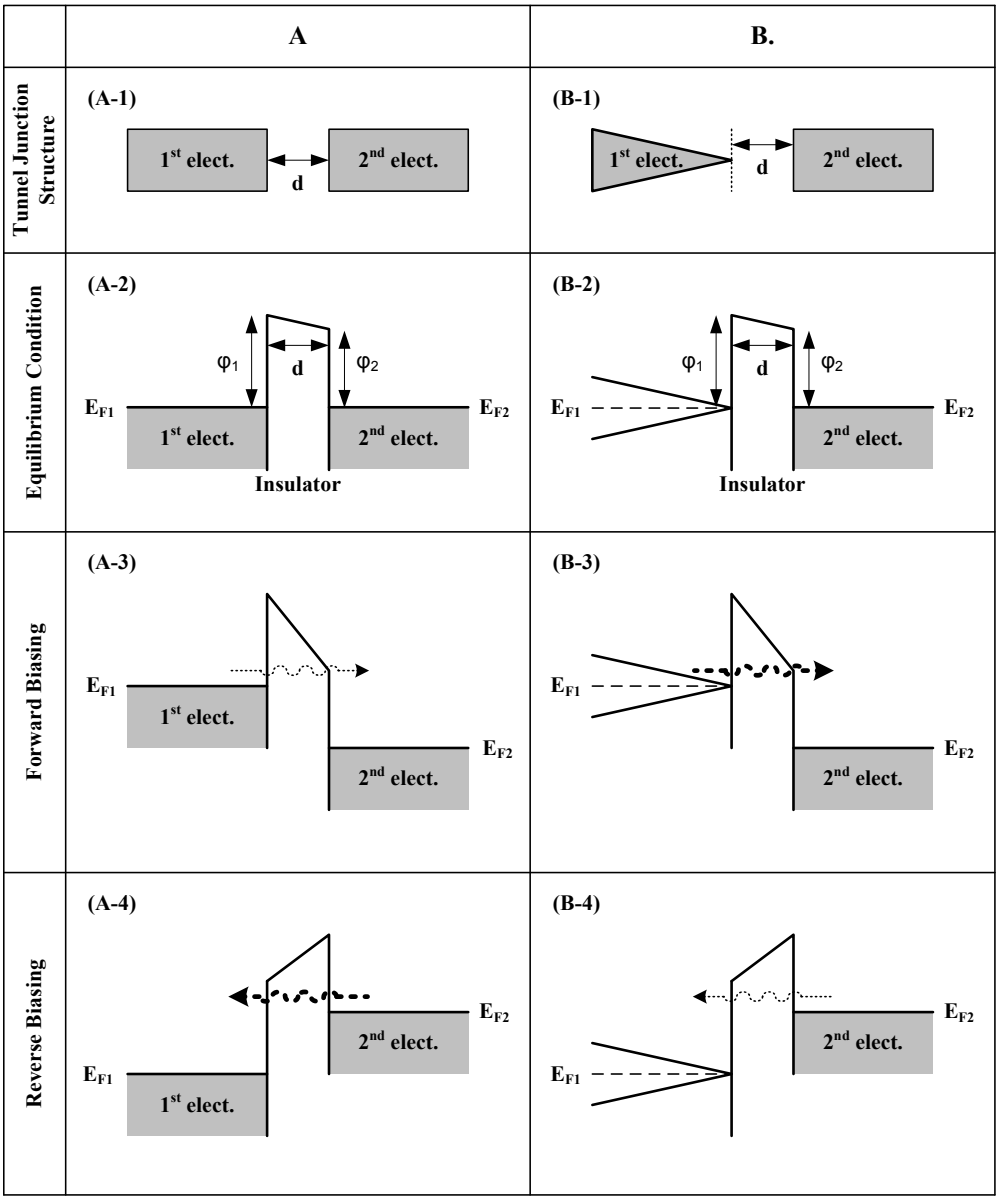

Figure 3.1: Two tunneling junction structures and corresponding energy band diagrams for zero, forward, and reverse bias condition. Row A is for a conventional MIM diode, and row B is for a diode to which the GFE technique is applied.

Here, it is found that the electrical characteristics of this conventional tunnel junction is defined by the material properties of metal and insulator for electrodes and a tunnel barrier, respectively. Any kind of metal can be used for electrodes in

MIM tunneling diodes. However, when the main concern is to obtain the highest tunneling current through a metal-insulator-metal tunneling structure, Ni becomes the most attractive option because of the smallest band off-set energy in a Ni-NiO interface as 0.3 eV [13, 35]. Hobbs asserts that the smallest RC time constant possible for a high-yield Ni/NiO/Ni MIM diode is 30 $f$sec based on material properties [13]. Other metal/metal-oxide combinations should have bigger RC time constants due to the large band-edge offset at the interface and concurrent high tunneling resistance. The figure of merit of MIM tunneling diodes, such as sensitivity and tunneling resistance, are tied to this parameter as well.

Dissimilar metal electrodes can partially overcome the problem of achieving asymmetry in the tunneling I-V characteristics [34, 36]. It is to generate such a built-in potential in a tunneling barrier that asymmetric tunneling current can be obtained through the tunnel junction. Our main method of achieving current asymmetry is described in the next section.

3.2 What is the GFE Technique?

The geometric field enhancement (GFE) technique locally enhances the electric field and creates a natural I-V asymmetry through field-line concentration at a sharp tip. This technique is implemented using a sharply pointed electrode facing a second planar electrode with a tunneling barrier. A schematic of this structure is shown in Figure 3.1 (B-1). Asymmetric electric field can be generated in the tunneling barrier due to the pointed electrode under a biased condition. Comparing equal magnitudes

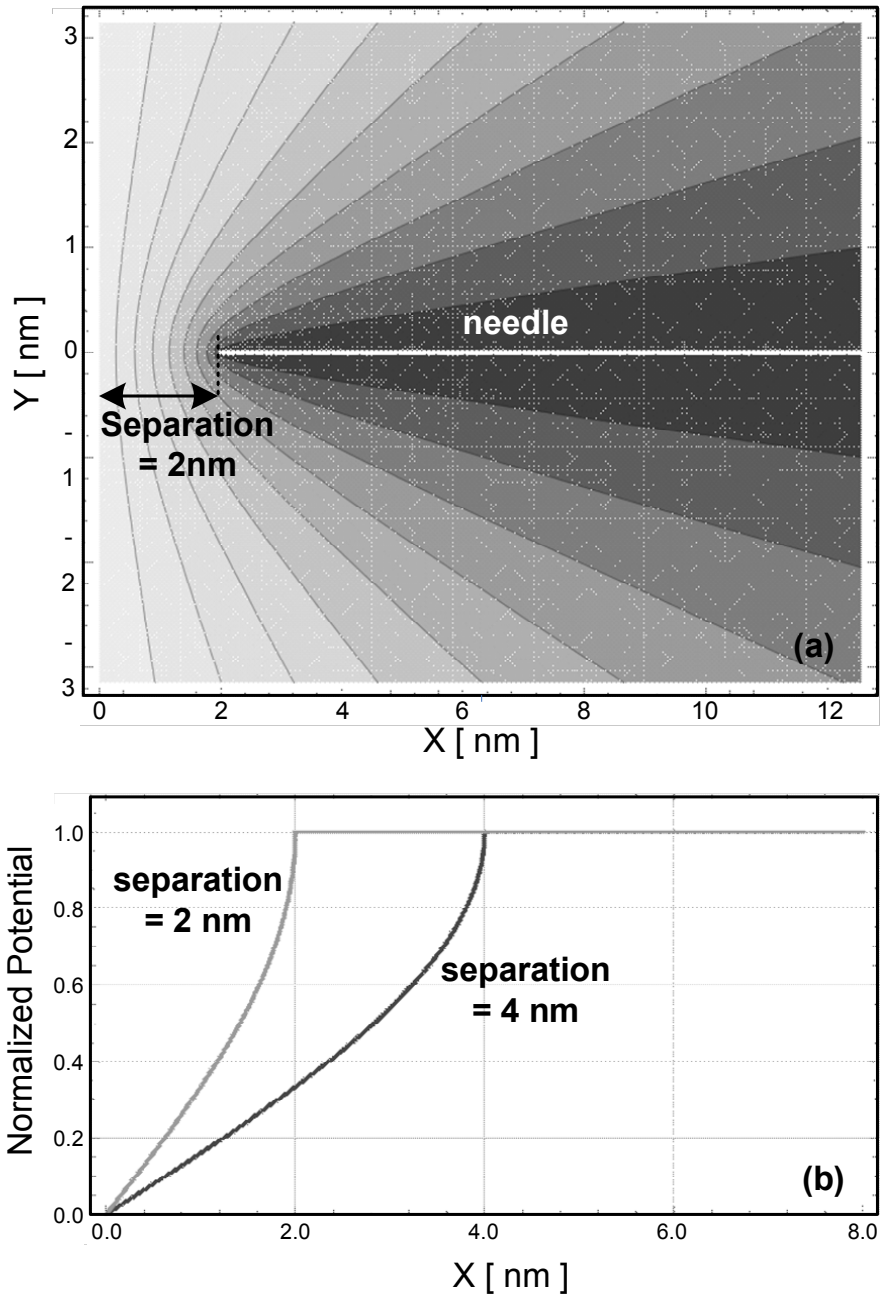

Figure 3.2: (a) Equipotential surfaces obtained by conformal mapping for the needle-on-plane problem. The needle is on the right. The plane is on the left. (b) Potential vs. distance for the needle-on-plane problem. The potential is normalized to that on the needle tip.

of forward and reverse bias condition for these different electrode geometries, as appearing in Figure 1 (B-3) and (B-4), a higher electric field is created near the pointed electrode under the reverse bias condition than the plane electrode side under the forward bias condition. This, of course, is due to "lightning rod" effect (bunching of field lines at sharp points.)

Assuming that the gap (d) between the two electrodes in Figure 1 is small enough for electron tunneling, the asymmetric electric field affects tunneling probability. As a result, asymmetric tunneling current, higher reverse tunneling current, can be generated through the tunnel junction by the GFE technique (assuming the GFE effect is stronger than the tunneling barrier lowering effect).

Our initial modeling work [37] was done using conformal mapping solution to the Poisson equation to check an asymmetric electric field intensity which is created by a geometric effect [38]. The simulation results for the two different separations, 2 nm and 4 nm, were just provided to show asymmetric electric field or potential under certain specific simulation conditions.

In Figure 3.2(a), the equipotentials are shown around an ultra sharp tip named as a needle to the right. The lightning rod effect causes a sharp bunching of the surfaces and an attendant high field at the needle tip. The plane spreads the equipotentials, lowering the field. In Figure 3.2 (b), the potential is plotted as a function of position, normalized to the bias at the needle tip. Also, it shows what happens when the tip-to-plane separation is changed from 2 to 4 nm. In both cases, the electric field (the slope of the potential versus position plot) increases at the tip. By taking a ratio of the field (calculated as the potential versus position slope) at

nine-tenths of the way to the needle tip to the field at the planar surface, the ratio is close to 2.3 for both cases shown in Figure 3.2(b). The electric field is more than double on the tip with respect to the plane. Therefore, the tunneling current in this structure can be asymmetric due to the geometric field enhancement.

3.3 Benefits of the GFE Technique

The most clear and conspicuous characteristic of the GFE technique is that it generates asymmetric tunneling currents through a tunneling barrier. But the GFE technique provides other unique advantages:

- Reducing tunneling resistance (DC lightning rod effect)
- Increasing nonlinearity (DC lightning rod effect)
- Enhancing the effective amplitude of the AC signal (AC lightning rod effect)
- Improving zero bias performance
- Merging with dissimilar electrodes method
- Using near field enhancement by surface plasmon resonances

First, the GFE technique increases tunneling current level directly. Especially for the configuration shown in Figure 3.1, the reverse tunneling current becomes bigger than the forward current due to the asymmetric electric field induced by the GFE technique. This is a practical result of lightning rod effect under DC biased condition. This asymmetric tunneling current is significant, as this characteristic is achieved with the same metal used on both electrodes. This increased tunneling current helps eliminate material limitations as it reduces tunneling resistance.

Therefore, a smaller RC time constant can be achieved, and the power transfer efficiency can be improved because the matching condition is more closely satisfied.

The current curvature or nonlinearity (the second bullet) can be improved by the GFE approach as well. A higher current level leads to a rapid change of resistance and increases current curvature. Also, the current level dependency of I″can be found in the MIM diode comparison table in Wilke's paper [10].

Both AC and DC electric fields are enhanced by lightening rod effect. The AC signals coupled to the antenna surface travel and then form fields at the tunnel junction. The traveling signals appear to be focused at the pointed electrode tip by the pointed electrode geometry: AC lightning rod effect. Accordingly, stronger signals can be injected into the tunnel junction. This phenomenon is demonstrated by Grober et, al. at RF frequencies [39]. Considering this situation, bowtie antenna must be the best choice as integrated antenna type. Due to the geometry of a bowtie antenna, the AC lightning rod effect can be maximized compared to other antenna types [40, 41]. This AC lightning rod effect can increase the magnitude of AC coupled signal, $|v_{ac}|$, in Eq. (2.2) and (2.3).

The performance improvement at zero bias is an extension of the previously outlined benefits of the GFE technique. Of course, in the absolute zero bias state, there may be no GFE effect. (No field lines are present to "bunch up.") However, as soon as the AC field is incident, there is a field-line concentration. The geometric asymmetry yields unidirectional current flow (rectification.) And furthermore, the tunneling resistance during negative phase is smaller than positive phase due to this asymmetric field generated by the oscillating signal. This asymmetric conductance

increases current nonlinearity even at zero bias. (Sensitivity increases also due to the improved I''.) This additional I$''$ improvement is considered a secondary enhancement distinguished from the main I$''$ improvement brought by increased current level due to the DC lighting rod effect. This secondary effect should be effective for entire bias range.

In addition to the previously described benefits of the GFE technique, this technique can be merged with the dissimilar electrodes method without any performance or characteristic trade-off. Therefore, further performance improvement is possible through higher tunneling current asymmetry for MIM tunneling diodes.

As mentioned before, the GFE technique is implemented by using a pointed electrode shape. This electrode shape enables tunneling diodes to use the near field enhancement created by surface plasmon and surface plasmon resonances. This benefit of the GFE technique is discussed in the next chapter.

Chapter 4

Surface Plasmon Resonance Applied to Tunneling Diodes

4.1 The Surface Plasmon

In the text below, we describe the physics of plasmon generation and how these excitations can improve MIM diode performances.

4.1.1 Dielectric Constant (Relative Permittivity ε_r)

Metals are usually considered to be good conductors up to near infrared frequencies. As a result, electromagnetic waves can't propagate into the metals and are easily reflected from the surface. At higher frequencies, such as far-infrared, visible, or ultra violet, metals exhibit dielectric properties, so they allow such high frequency waves to propagate as through a waveguide. These essentially optical characteristics of metals are described by the dielectric constant or relative permittivity. In other words, permittivity relates to a material's ability to guide electromagnetic waves. The frequency dependency of permittivity is called dispersion, and it works as a key concept for optical properties of a material.

In an isotropic media, the relative permittivity is a scalar and can be expressed by

$$\varepsilon_r = 1 + \chi \tag{4.1}$$

where χ is the electric susceptibility due to polarization. Permittivity is defined by $\varepsilon = \varepsilon_r \varepsilon_0$, where ε_0 is the permittivity of free space. When the frequency response of a medium includes phase differences, permittivity has a complex form:

$$\varepsilon(\omega) = \varepsilon'(\omega) + i\varepsilon''(\omega) \tag{4.2}$$

where ε' is the real part of the permittivity related to the stored energy within the medium, and ε'' is the imaginary part of the permittivity related to the dissipation or loss of energy within the medium.

In a lossy medium, the total current density is expressed by

$$J_{Tot} = J_c + J_d = \sigma E - i\omega\varepsilon' E = -i\omega\varepsilon E \tag{4.3}$$

where J_c is the Ohm's law field driven current, J_d is the displacement current, σ is the conductivity, E is the electric field, ω is the angular frequency, ε' is the real part of the permittivity, and ε is the complex permittivity. So, the complex permittivity can be expressed by

$$\varepsilon(\omega) = \varepsilon'(\omega) - i\frac{\sigma}{\omega} \tag{4.4}$$

If we just focus on metals, then a more useful form of Eq. (4.4) can be derived using the Drude Model for a wide frequency range [31, 32]. Simply, the Drude Model gives

$$\varepsilon(\omega) = 1 - \frac{{\omega_p}^2}{\omega^2 + i\gamma\omega} \tag{4.5}$$

where ${\omega_p}^2$ is the plasma frequency of the free electron gas, γ=$1/\tau$ is a characteristic collision frequency according to applied electromagnetic field on a metal medium, and τ is the relaxation time of the free electron gas. The plasma frequency is the natural frequency of a free oscillation for the electron gas, and it is expressed by

$${\omega_p}^2 = \frac{ne^2}{\varepsilon_0 m^*} \tag{4.6}$$

where n is the electron density, and e is the electron charge, and m^* is the effective optical mass.

From Eq. (4.2) and Eq. (4.5), the real and imaginary components of the complex permittivity are given by

$$\varepsilon'(\omega) = 1 - \frac{\omega_p^2\tau^2}{1 + \omega^2\tau^2} \tag{4.7}$$

$$\varepsilon''(\omega) = \frac{\omega_p^2\tau^2}{\omega(1 + \omega^2\tau^2)} \tag{4.8}$$

Usually, the Drude model is applicable up to a specific frequency where inter-band transitions can occur by high photon energy.

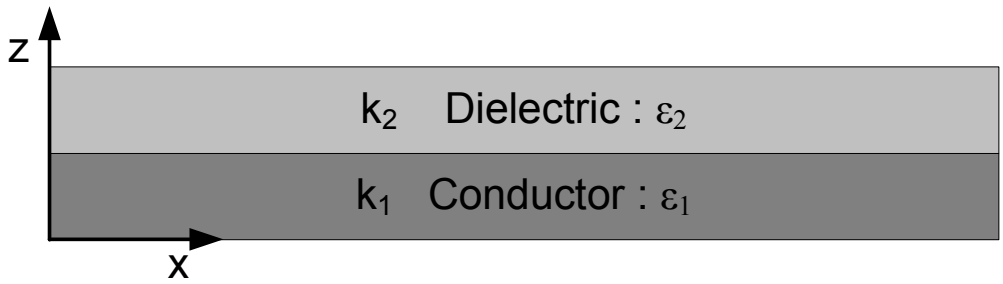

Figure 4.1: A simple dielectric-conductor configuration

4.1.2 Surface Plasmon

Surface plasmon (SP) or surface plasmon polariton (SPP) is electron fluctuation at the boundary between a conductor and a dielectric. These waves (or quasi particles) are confined to the interface and propagate along the surface of conductor, and the characteristics are explained using Maxwell's equations. For a simple conductor and dielectric configuration, shown in Figure 4.1, the solutions of Maxwell's equations exist only for TM mode especially for confined waves to the interface with only x direction of wave propagation, not TE mode. Mathematical derivations solving Maxwell's equations for the trapped surface wave can be found in many references [42, 43]. From the solutions, two useful relations can be derived using boundary conditions at the interface,

$$\frac{k_2}{k_1} = -\frac{\varepsilon_2}{\varepsilon_1} \tag{4.9}$$

$$k_1{}^2 = \beta^2 - k_0{}^2\varepsilon_1, k_2{}^2 = \beta^2 - k_0{}^2\varepsilon_2 \tag{4.10}$$

where k_1 and k_2 are the wave vectors, ε_1 and ε_2 are the relative permittivities for each region, k_0 is the free space wave vector, and β is the complex propagation constant. Because the dielectric's permittivity is usually positive, Eq. (4.9) implies that the real part of ε_1 must take on a negative value. Finally, the dispersion relation is given by using Eq. (4.9) and Eq. (4.10)

$$\beta = k_0 \sqrt{\frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2}} \tag{4.11}$$

The dispersion relation, Eq. (4.11), is plotted in Figure 4.2 for metal/air and metal/silica configurations [42]. When the propagation constant is increased, the frequency is saturated at the surface plasmon frequency, ω_{sp} , which is expressed as:

$$\omega_{sp} = \frac{\omega_p}{\sqrt{1 + \varepsilon_2}} \tag{4.12}$$

As shown in Figure 4.2, the propagation constant of the surface plasmon wave is greater than the wave vector of the incident wave. This means a special method, compensating the phase difference between the incident wave and the induced surface plasmon wave, is necessary to generate surface plasmon waves. There are several techniques for the phase matching. These include prism coupling, grating coupling, focused optical beams, near-field excitation, and end-fire coupling [44, 45, 46, 47, 48, 49]. Through anyone of these coupling processes, an incident wave can excite a surface plasmon wave at the interface of a conductor and a dielectric material.

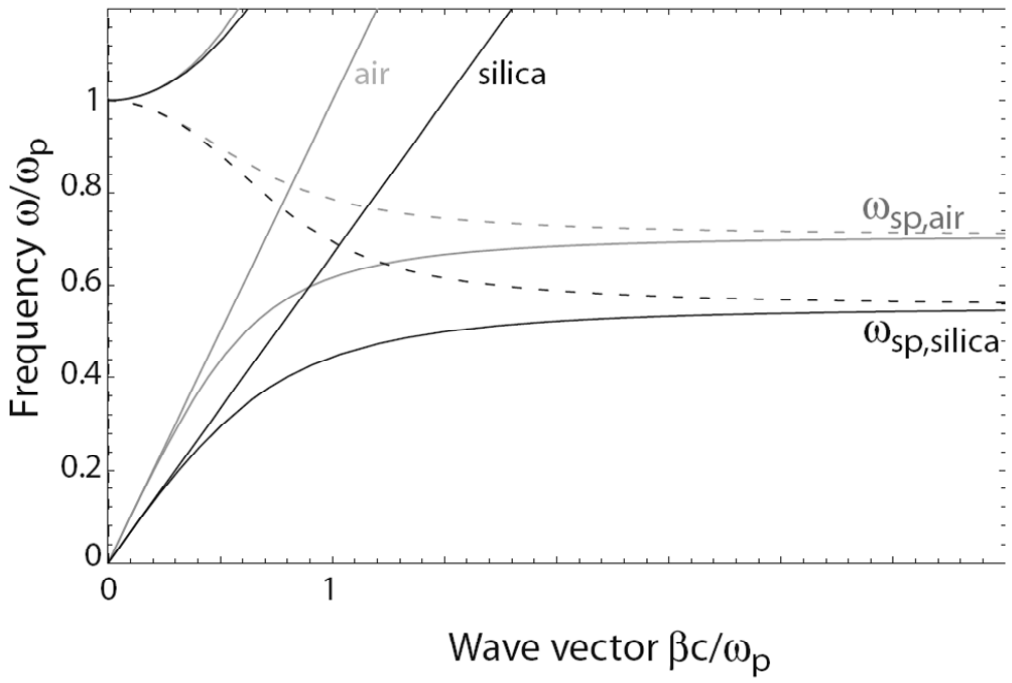

Figure 4.2: Dispersion relation of surface plasmon wave at the interface between a metal and air (gray) & silica (black). Dash lines are for imaginary part of the propagation constant [45].

4.2 Surface Plasmon Resonance & Optical Antenna

The term "surface plasmon resonance (SPR)" is used for describing localized surface plasmons, especially for metallic nanostructures. Contrary to the propagation of surface plasmon waves discussed in the previous section, the surface plasmon resonances can be excited through direct light illumination on nanometer size particles without a specific coupling technique when the particle size is much smaller than the incident wavelength. Intuitively, incident waves cause a collective displacement of electrons at surface of a metal pattern, and this charge displacement creates a restoring force. Therefore, a resonance can arise on a metal particle. The most important property of surface plasmon resonance is the field enhancement near the

particle. Many researchers have observed the field enhancement effect on nano-size metal patterns, illuminated at the resonant wavelength [15, 50, 51, 52, 53, 54, 55]. The field enhancement is exploited for implementing optical antennas. It leads to confine intense optical fields in a small gap, which has subwavelength dimensions, at the SPR resonance frequency.

For the case at hand, in the infrared region, the antenna length (L) and resonance wavelength (λ) seem to follow a common antenna theory with little deviation caused by substrate screening and conductivity change [15, 50, 56]:

$$L = \frac{\lambda}{2n_{eff}} = \frac{\lambda_{eff}}{2} \tag{4.13}$$

where n_{eff} is the effective refractive index of surrounding materials. In the visible region, however, the deviation of resonance wavelengths from general antenna concept is much more serious than it is in the infrared region. To compensate for this, Novotny et, al. derived a theoretical scaling formula for effective wavelengths from near-infrared to visible [16]. Another possible approach is using simulations such as finite-difference time-domain (FDTD) simulation for optical antenna design [54]. Simple shapes, such as bar, triangle, and circle, are very common patterns for SPR and optical antenna research.For most case, a coupled configuration is used to implement a dipole and a bowtie optical antenna.

The resonance wavelength of a coupled antenna shows different characteristics compared with a single pattern. While the resonance wavelength of a single pattern is determined by pattern's geometric parameters and material properties, the gap

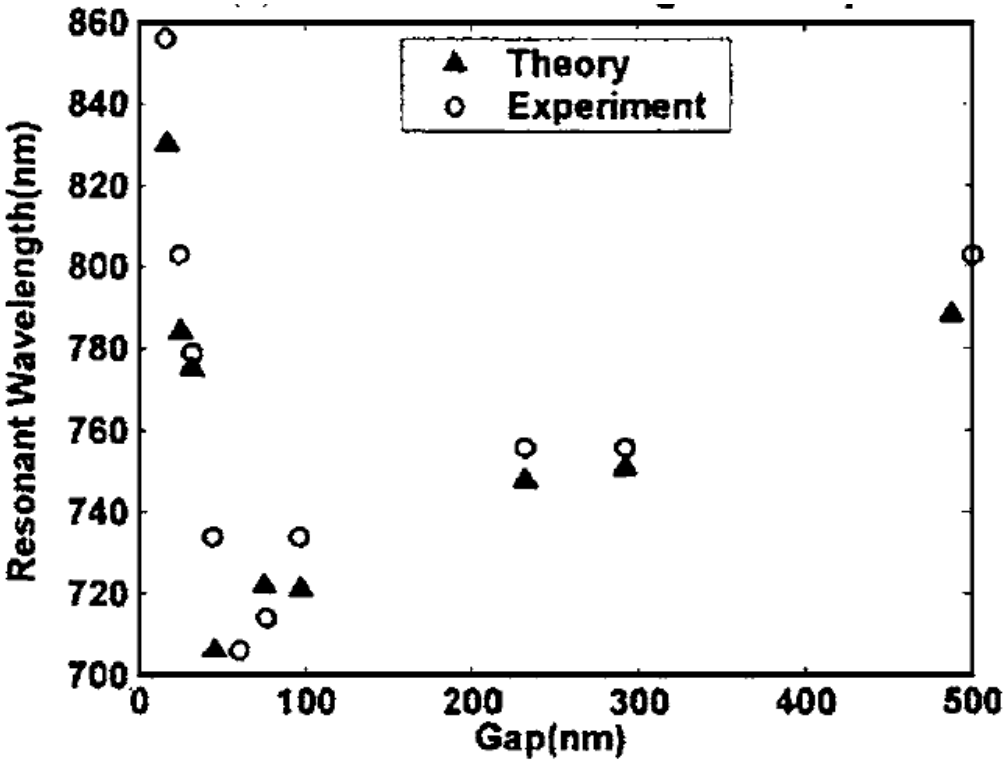

Figure 4.3: Experimental measurements (cricles) and FDTD simulations (triangles) of the peak resonant wavelength versus gap size for bowtie optical antennas [57].

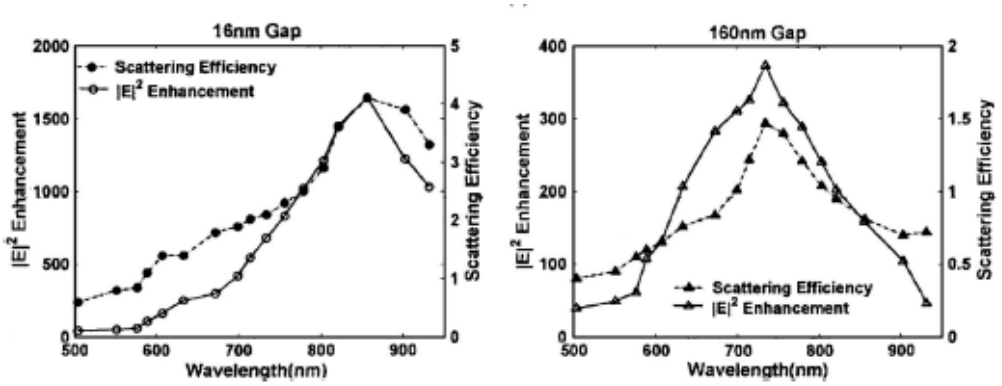

Figure 4.4: Field intensity for bowtie optical antennas with different gap size, 16 nm and 160 nm [57].

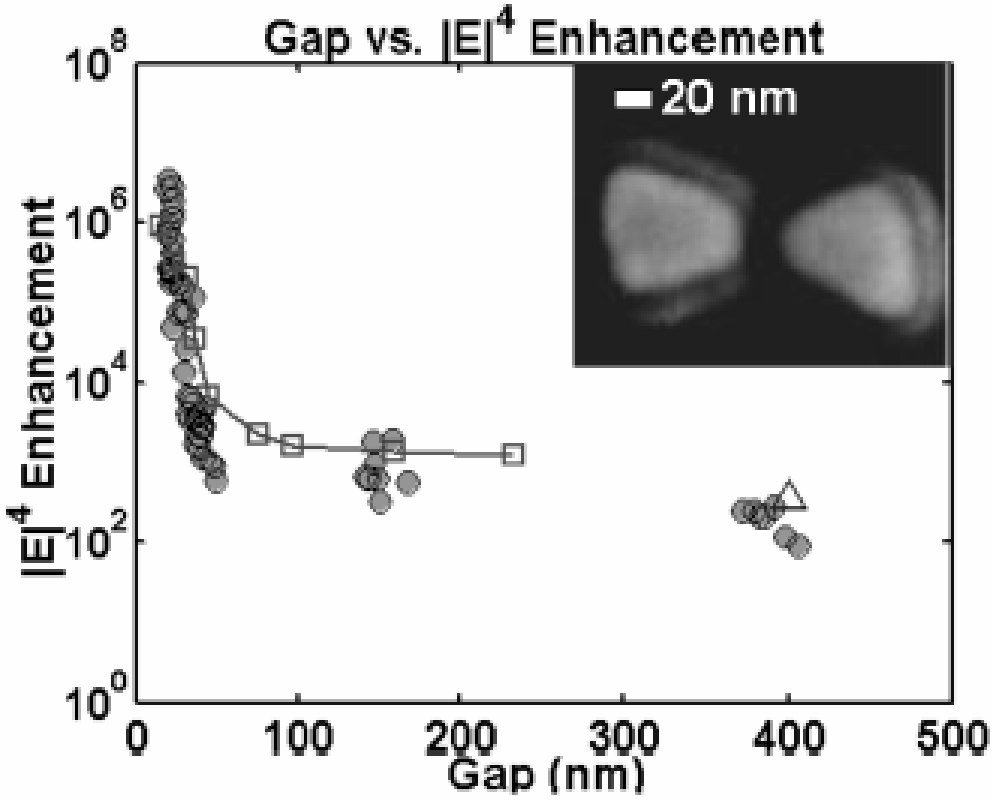

Figure 4.5: Electric field enhancement depending on the gap size: experimental data (circles) and FDTD simulation data (open squares) [61].

size of a coupled antenna plays as another key factor, which determines the resonance wavelength. As the gap size decreases, the resonance wavelength is also decreased for a coupled configuration. However, the resonance wavelength begins increasing after a certain gap size [54, 57, 53]. Figure 4.3 shows the relationship between antenna gap and resonant wavelength of optical bowtie antennas [54]. Another interesting point is that the resonance wavelengths of a single pattern and a coupled one are different in experiments and simulations. The resonance wavelength of a coupled structure was longer than one of a single pattern.

Figure 4.4 shows a FDTD simulation result of a optical bowtie antenna illu-

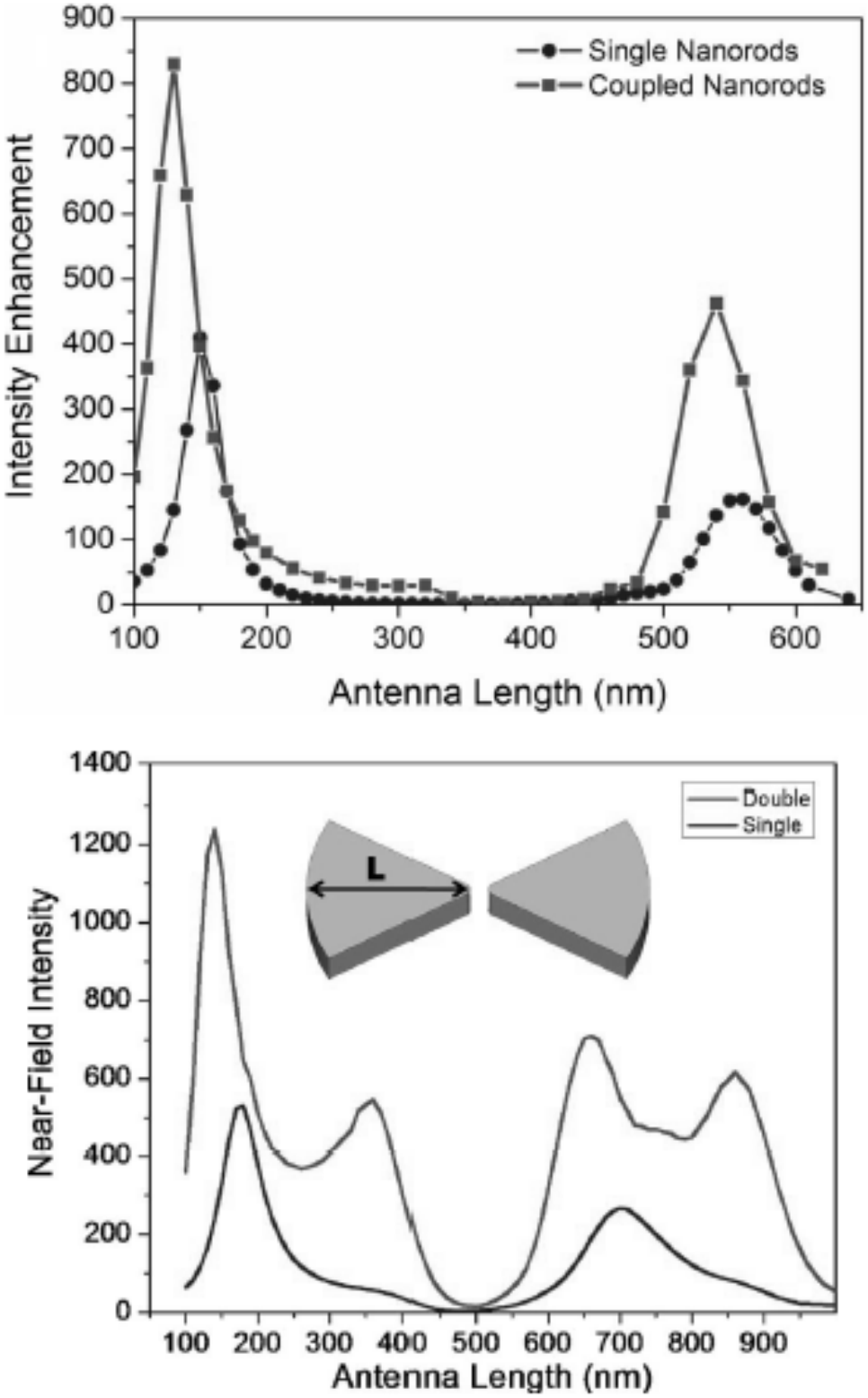

Figure 4.6: Field intensity comparison: between a single nanorod and dipole antenna (top) and between a triangle and bowtie antenna (bottom) under 830 nm wavelength illumination [62].

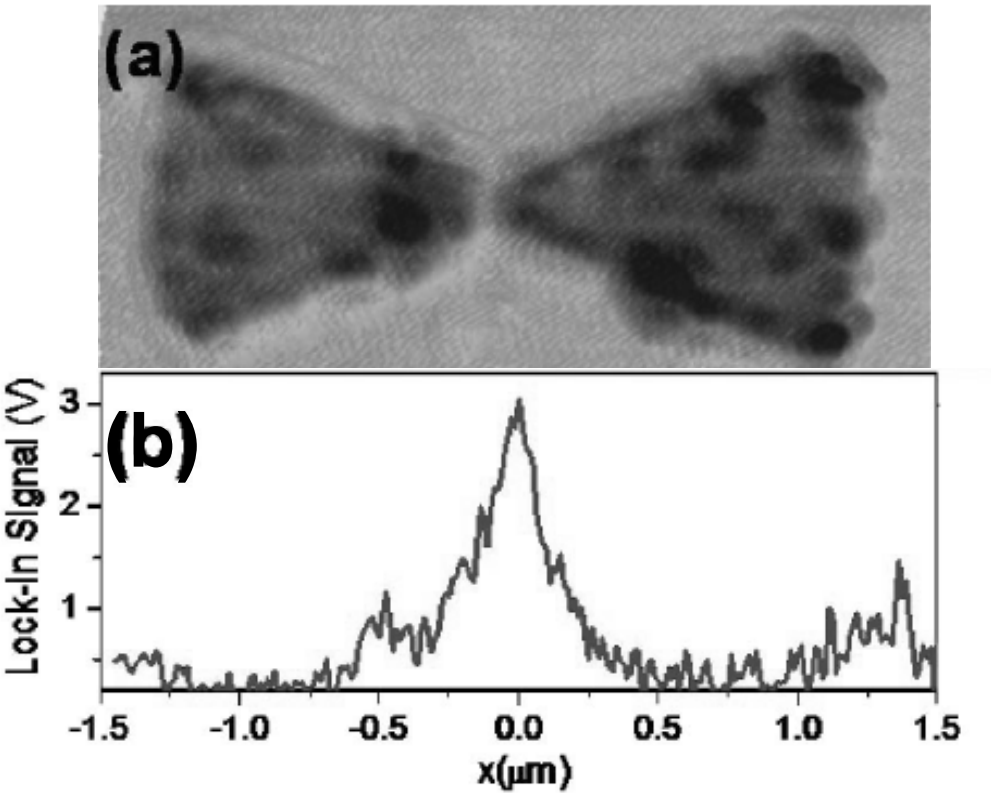

Figure 4.7: Field intensity experiment results of a bowtie antenna under 7 um infrared wave: (a) AFM scanning image and (b) measured signal in the gap of bowtie antenna [62].

minated by visible waves [54]. The field intensity is calculated at the middle of the gap. For the coupled antennas, the gap size is the most critical parameter with antenna length again. Contrary to the resonant wavelength, the field intensity always increases as the gap size is decreasing, shown in Figure 4.5 [58].

The coupled antenna's field intensity is higher than a single pattern [59]. In Figure 4.6, FDTD simulation results show the higher field intensity of coupled antenna than a single pattern at the same antenna length under 830nm plane wave illumination [59]. In the simulations, the coupled antennas have a 20 nm gap. For

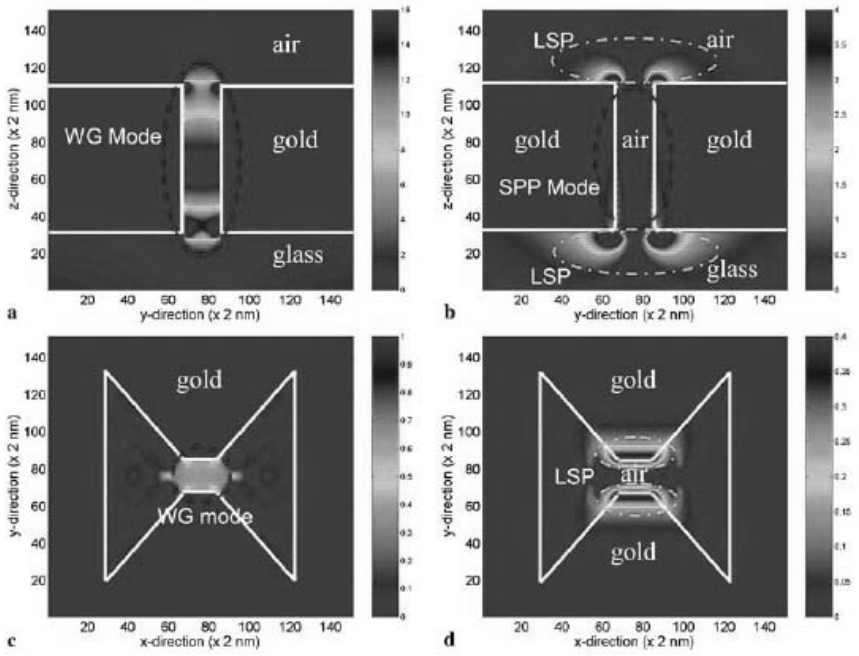

Figure 4.8: Time-averaged (a), (c) $|E_y|^2$ and (b), (d) $|E_y|^2$ distributions of the bowtie aperture in a 160 nm gold film on quartz substrate computed by the FDTD method. The y-polarized plane wave at 633 nm wavelength is incident from the substrate side. (a), (b) show the middle yz plane across the bowtie gap, and (c), (d) show the xy plane cutting through the middle of the gold film (where WG means LSP means localized surface plasmon) [64].

a bowtie antenna, the field intensity effect is broadened over much wide wavelength range compared with a dipole antenna, shown in Figure 4.6. This can be explained with quadrupole modes of bowtie antenna [60]. One of the most important results is the higher field intensity of the bowtie antenna compared to the dipole antenna in Figure 4.6. In the reference, the author explains this higher intensity due to the "lightning rod" effect [59]. Figure 4.7 shows an infrared experimental result of the same reference [59]. The antenna length is around 1.2 um and placed on a quantum-cascade laser facet, which has a 7 um wavelength.

Special field intensity information can be obtained from FDTD simulations. Figure 4.8 shows FDTD simulation results for a gold bowtie pattern simulated in [61]. The maximum field intensity occurs inside the gap for $|E_y|^2$ component. As shown in Figure 4.8, the most high electric fields are confined in the gap.

4.3 Surface Plasmon Resonance in Tunneling Diode

In chapter 3, surface plasmon resonance is mentioned as the last benefit of using the GFE technique in MIM tunneling diodes. One of the main goals of developing the GFE technique is to exploit such a field enhancement mechanism in an antenna/MIM integrated structure. This section explain how the field enhancement by SPRs is achieved in the GFE technique as the last benefit.

At first, it needs to be checked the structural difference between conventional thin film MIM diodes and optical antennas which both have a bowtie antenna structure. The main difference is having a focused launching structure or not. Optical

antenna have a focused structure composed of two sharpened and faced antenna arms. As a result of the focused structure, strong electric field enhancement is established in the gap through the "lightning rod" effect. On the other hand, conventional MIM tunneling diodes, for example shown in Figure 2.3, have a simple overlap structure between bias lead lines which are connected to each antennae arm. Therefore, conventional tunneling diodes are not "shaped" right to take full advantage of plasmonic field enhancement. Because the GFE technique is implemented by a pointed electrode, the field enhancement can be achieved by the "lightning rod" effect.

Surface plasmons can be excited through a proper grating structure satisfying a required momentum matching condition [62, 63]. By implementing a focused waveguide to the grating structure, the propagating surface plasmons can be launched and enhanced at the end of the waveguide. For the localized surface plasmons (=surface plasmon resonances), SPRs on a isolated particle can be coupled to the next particle in a properly distributed array. Like propagating surface plasmons, this SPRs also can propagate through a proper particle array and be launched through a pointed waveguide. In antenna coupled MIM tunneling diodes or optical antennas, each antenna flare can be used as a pointed waveguide as a plasmon launcher for electric field enhancement.

Considering the structure of conventional MIM diodes, even if surface plasmons are excited on the antenna surface, the surface plasmons cannot be launched into the tunneling junction. Instead of focusing and launching into the junction, the excited surface plasmons would simply travel from the antenna to the bias lines.

In this case, the propagating direction of the surface plasmon is orthogonal to the tunnel junction. The near field enhancement may not appear, or it would be very weak. The GFE technique uses a pointed tip which is encapsulated by another electrode. Therefore, the generated SPs or SPRs can be confined into a tunneling barrier without any geometric loss.

If the near field enhancement by surface plasmon resonance is demonstrated on MIM tunneling diodes, the consequent effect should be similar to the previous AC lightning rod effect. Therefore, we could achieve additional improvement in the tunneling diode rectifying operation [41].

4.4 Field Enhancement Simulation by Surface Plasmon Resonance

This section introduces the simulation results of electric field enhancement induced by SPRs. Using COMSOL Multiphysics, the field enhancement is simulated based on the FDTD method. (All simulation results in this section are provided by Filiz Yesilkoy.) First, a 2-D simulation is performed to check the resonance antenna length by SPRs at 9.6 μm incident wavelength. For this simulation, a Ni bowtie antenna on SiO2 substrate is used, and the entire model structure is surrounded by a PML (Perfect Matched Layer). The gap size of the bowtie antenna is 10 nm, and it is filled by air. Figure 4.9 shows the 2-D model. In the simulation, the electric field intensity at the middle of the gap is monitored to find the antenna's resonance by changing the antenna length from 0.5 μm to 5 μm. The highest resonance is observed at antenna length of 2.3 μm, as shown in Figure 4.10. (The E-field enhancement

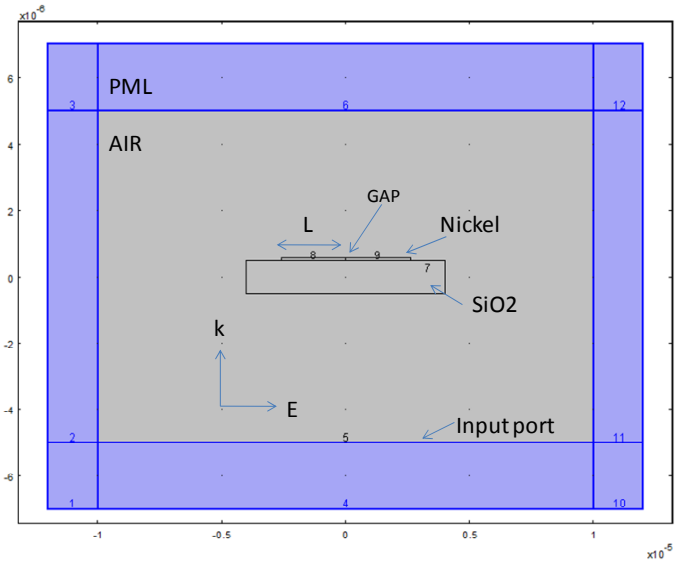

Figure 4.9: 2-D model for checking the resonance length of a bowtie antenna.

factor is a relative value compared to the intensity of the incident electric field.)

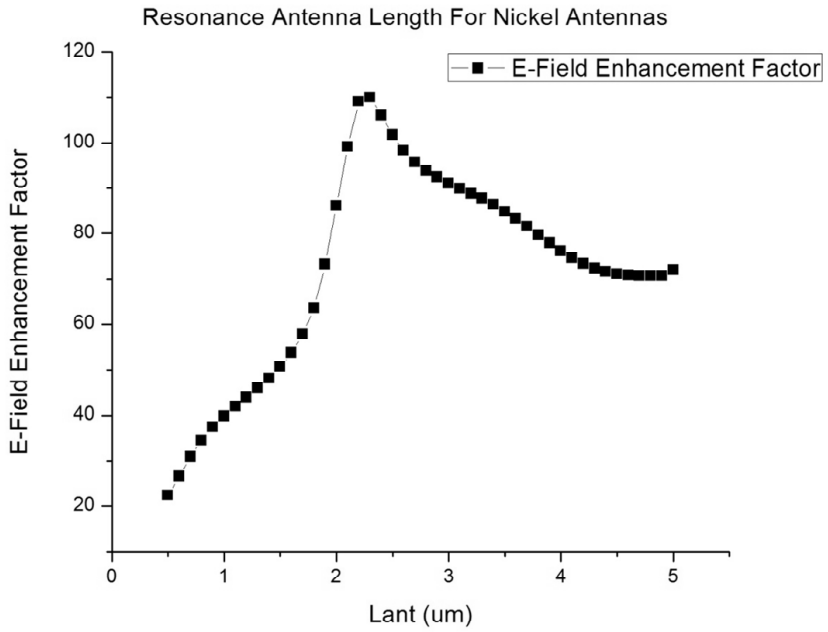

Figure 4.10: Simulation result of a Ni bowtie antenna for 9.6 um infrared wave.

Though a strong resonance and electric field enhancement are achieved with antenna length of 2.3 μm, it could be occurred due to antenna resonance, not due to SPRs. However, the antenna resonance at 9.6 μm incident wavelength is at 3.3 μm, calculated by using Eq. (4.13). This antenna resonance length shows a large deviation from the simulation result. Furthermore, the wavelength of the SP, which can be excited on Ni surface under 9.6 μm incident wave, is 2.46 μm and almost matched to the simulation result, 2.3 μm. (Here, the wavelength of SP is calculated using Eq. (4.11) with ε_{Ni} = -1599 and ε_{SiO_2} = 3.9 at 9.6 μm wavelength [64].) Therefore, this supports the condition that the strong resonance in the simulation is mainly the result of SPRs.

In Chapter 3, the proper structure to implement the GFE technique is described as a pointed tip facing a metal plane. The tunneling diode structure is designed as a 3-D modeling for simulation as shown in Figure 4.11. The tunneling diode consists of a triangular electrode and a plane electrode with a 10 nm air gap. Ni of 100 nm thickness is used for both electrodes, and entire diode structure is placed on SiO_2 substrate. The pointed tip is designed to have 20 nm radius curvature and 60 degree tip angle. PML layers are used at the top and bottom of the simulated space.

To excite surface plasmon resonance at the air gap, the incident wave of 9.6 μm is launched from the bottom. Figure 4.12 shows the special distribution of electric field between two Ni electrodes. In Figure 4.12, the electric field intensity is normalized to incident electric field magnitude and shown with a scale bar. An asymmetric field characteristic is observed in this SPR simulation: the highest field

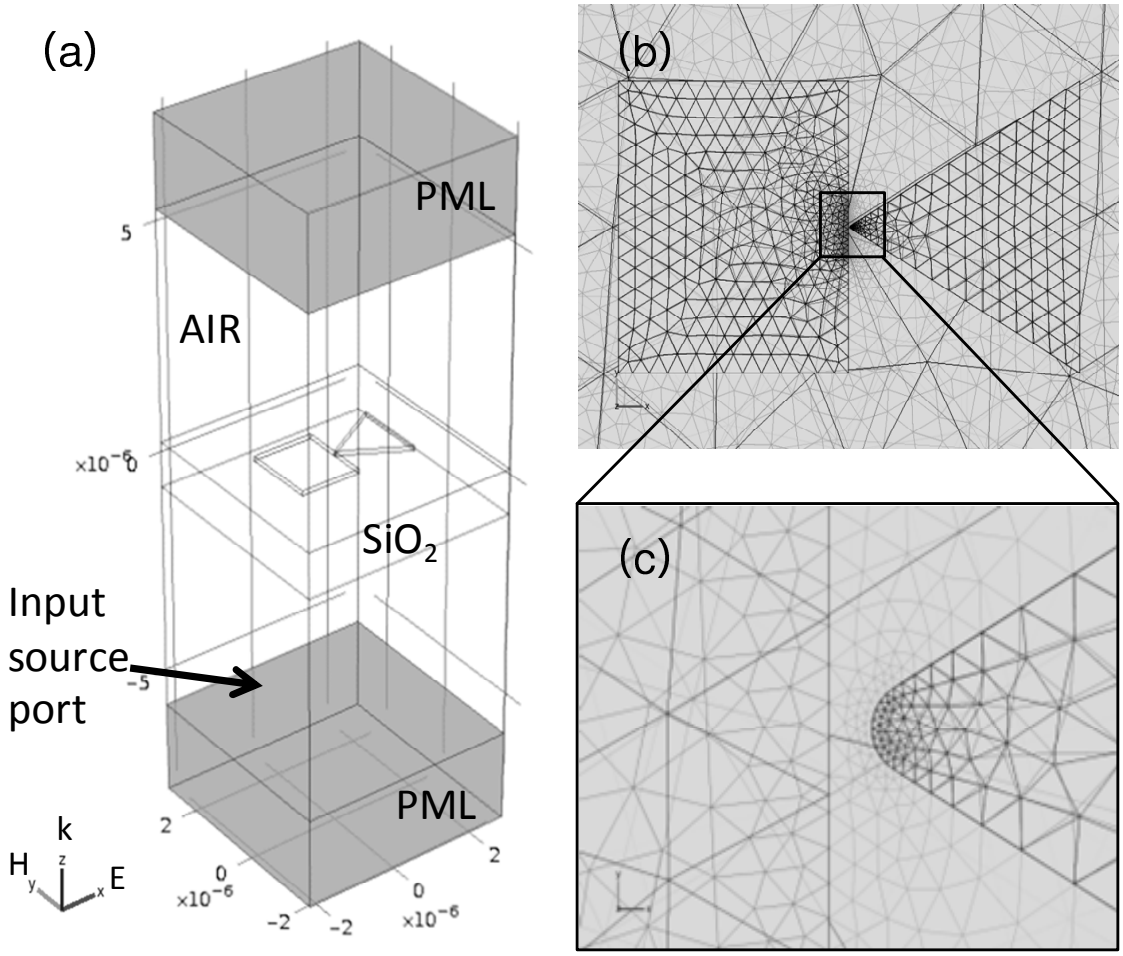

Figure 4.11: 3-D simulation model for an asymmetric tunneling diode structure: (a) overall model structure, (b) top view of an asymmetric tunneling structure using simulation mesh lines, (c) a Ni tip with 20 nm radius curvature, 10 nm air gap, 100 nm thickness, and 60 degree tip angle.

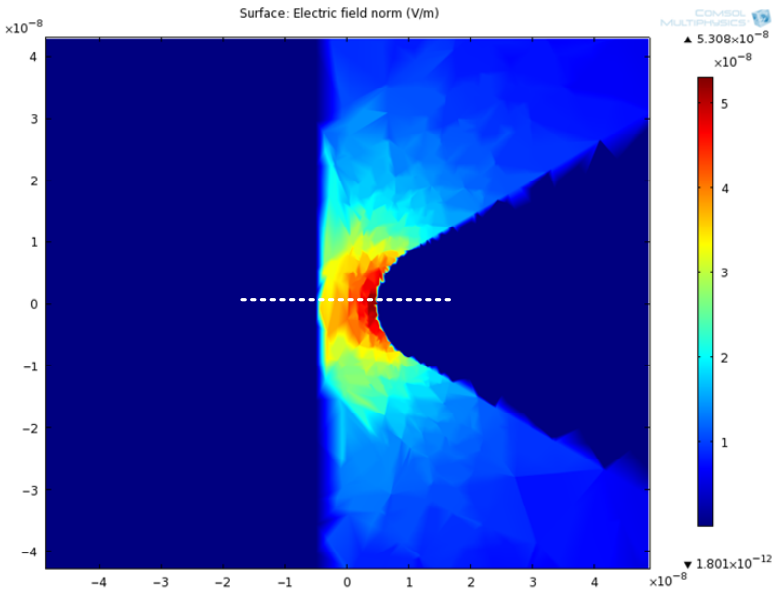

Figure 4.12: Electric field enhancement induced by surface plasmon resonances inside the air gap between a pointed electrode and a plane electrode.

is obtained at the tip side, and the intensity reduces to the plane electrode direction. Figure 4.13 shows the distribution of the electric field intensity through the dash line in Figure 4.12. As mentioned, an asymmetric field distribution is obtained, and the highest electric field intensity is almost eight times higher than the incident electric field. When the electrode shape is changed to a bar, the highest electric field intensity is only double the incident intensity. The asymmetric characteristic of the field distribution disappears.

Another 2-D simulation is performed with a bowtie antenna and SP grating structures. The bowtie antenna model is the same as the first simulation. The grating structures are implemented with three Ni metal lines. Each metal line has a width of 2.3 μm and is placed at each antenna arm with 4.6 μm period. This time,

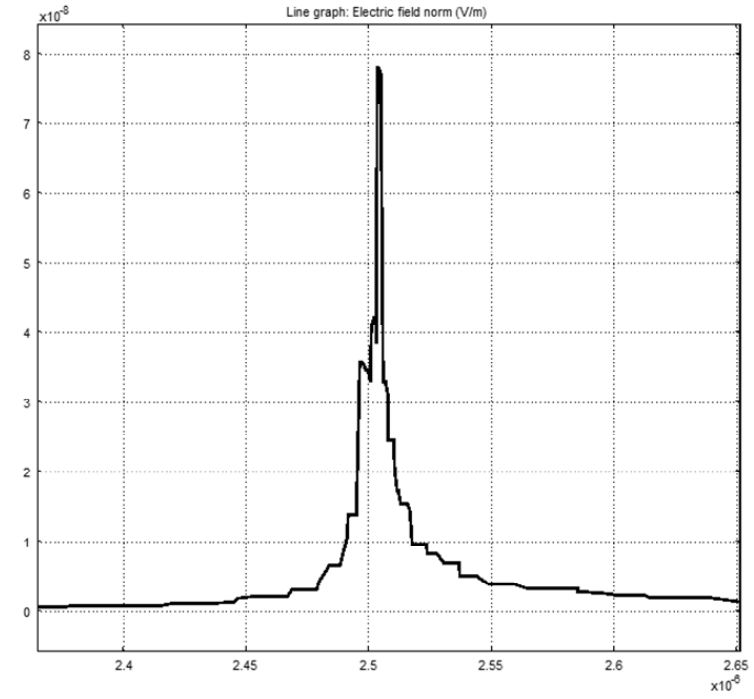

Figure 4.13: Electric field intensity through the dash line in Figure 4.13.

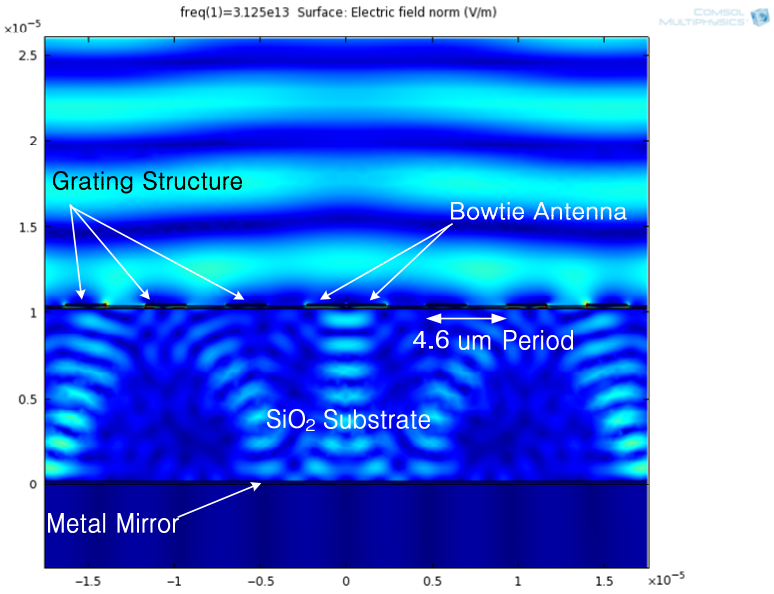

Figure 4.14: Simulation result of a bowtie antenna with grating structures.

the incident wave is launched from the top, and a metal mirror is placed at the bottom of the SiO_2 substrate. Figure 4.14 shows the simulation result. Comparing to an antenna only model, the electric field intensity with grating structures is as high as 15 %. These simulation results show that SPRs can create a strong electric field inside the tunneling barrier. By integrating grating structures, much stronger electric field can be obtained. Therefore, SPRs can be used to improve the rectifying performance of tunneling diodes.

Chapter 5

Tunneling Diode Fabrication

5.1 Fully Planar Type Tunneling Diode

First, we focus on our attempts to develop a perfect planar tunneling structure for the maximal use of the near field enhancement created by GFE and SRPs. In other words, implementing a tunnel junction in an optical bowtie antenna is the main target. As shown in chapter 4, the smallest gap size of reported optical antenna is 16 nm [54]. Tunneling current cannot be supported in such a thick tunneling barrier [18]. The required barrier thickness is below 4 nm thickness. This section shows how perfect planar type tunneling diodes are developed with a proper thickness of the tunneling barrier.

5.1.1 Planar Type Tunneling Diode Fabrication

The prototype devices were implemented with a bowtie antenna with 60° regular triangles of 4.3um each side length. A doped poly-Si layer is used for antenna and electrodes. The fabrication procedure is listed below, and each process step is explained after the list.

1. *Si_3N_4 deposition*
2. *Poly-Si deposition*

3. Poly-Si Doing

4. E-beam patterning

5. Reactive ion etching (RIE)

6. Applying boiling water oxidation process

1. *Si_3N_4 deposition* : A Si_3N_4 layer of 800 Å thickness is used as an insulation layer for device isolation from the conductive silicon substrate. For this Si_3N_4 layer is deposited by using a PECVD (Plasma-enhanced Chemical Vapor Deposition) is used.

2. *Poly-Si deposition* : A poly-Si layer of 600 Å thickness is deposited on the Si_3N_4 using a LPCVD (Low Pressure Chemical Vapor Deposition) to create the active device material.

3. *Poly-Si Doping* : Poly-Si doping is performed using a Spin-on-Dopant (SOD) with phosphorus dopants, followed by a RTA (Rapid Thermal Annealing) process to diffuse dopants. After SOD coating, the sample is baked at 200 $°C$ for 20 minute on a hot plate. A simple RTA process at 1000 $°C$ during 30 second transfers the dopants into the deposited poly-Si layer. Finally, the SOD is removed using a buffered oxide etch. A TLM (Transmission Line Method) pattern measurement shows the poly-Si sheet resistance to be 348 $\Omega/\square$ is obtained, and the doping concentration is about 10^{-21} cm^{-3} with the mobility of 100 cm^2/Vs.

4. *E-beam patterning* : For device patterning, e-beam writing instead of optical

lithography is used for poly-Si electrodes because of its higher resolution. First, Hydrogen Silsesquioxane (HSQ: e-beam resist) is coated to a sample. After baking at 150°C during 15 minute on a hotplate, the sample is loaded into the chamber of e-beam writer. For the specific writing condition, a 10 kV acceleration voltage and a 10 μm aperture size result in 12 pA current for a Raith e-LiNE writer. The 160 $\mu C/cm^{-3}$ writing dose gives almost perfect dose clearance for the bowtie electrode patterns. Finally, HSQ (Buffered Oxide Etch) patterns are formed after developing the sample in CD-26 developer.

5. *Reactive ion etching (RIE)* : RIE etching is applied using SF_6 and O_2 to etch out the poly-Si layer. Electron exposed HSQ patterns work as etch stop layer during RIE etching and is removed using BOE after dry etching. Figure 5.2 shows a pattern after RIE etching.

6. *Applying boiling water oxidation process* : Right after the RIE etching, the two flares of the bowtie pattern are connected by a thin poly-Si knot, shown in Figure 5.3. A boiling water process is applied to the poly-Si patterns to implement a insulator layer for tunneling barrier between two poly-Si electrodes. The details of boiling water oxidation process is discussed in the next section.

Figure 5.1 shows a schematic of the process flow described above. A more detailed process flow for the perfect planar tunneling diode fabrication is added in Appendix A.

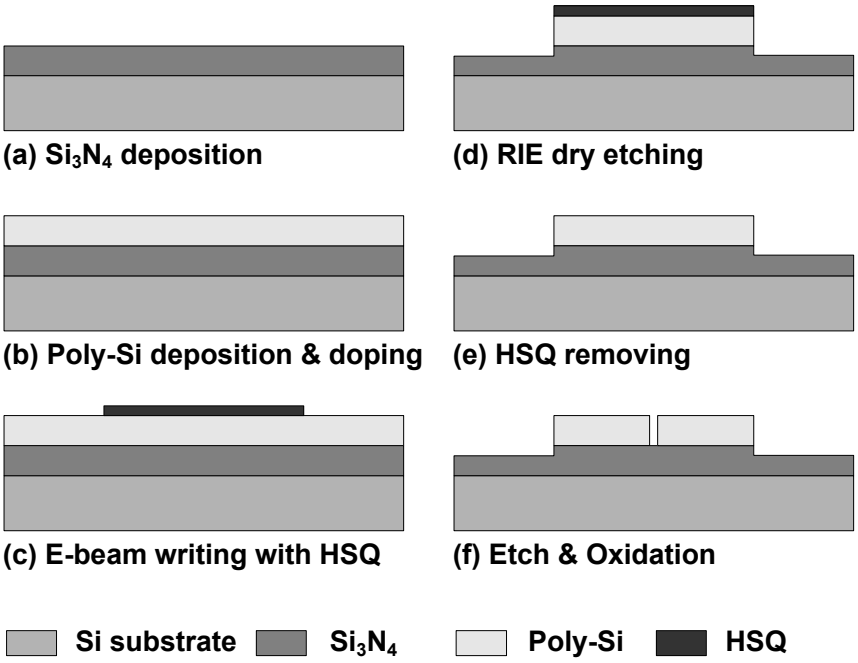

Figure 5.1: A schematic of process flow of polysilicon tunneling diode.

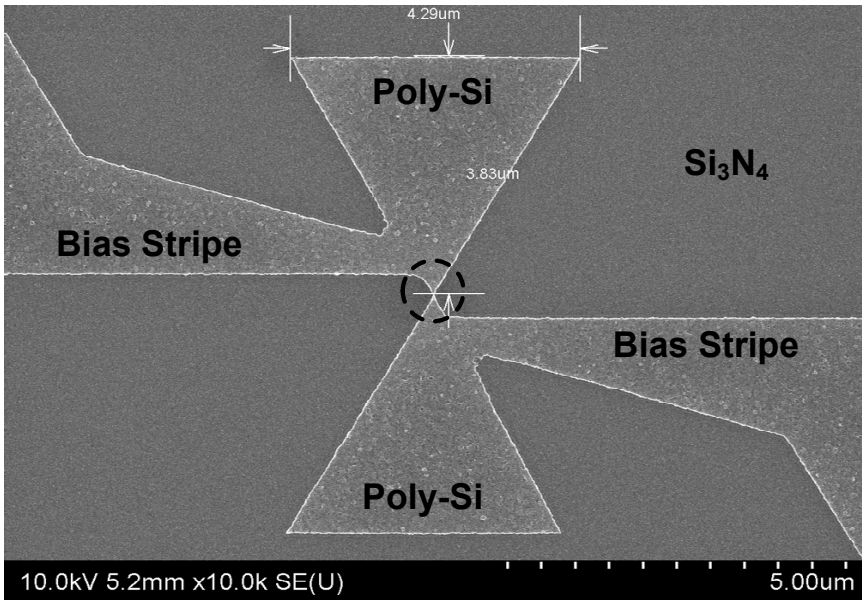

Figure 5.2: A SEM image after RIE etching of a poly-Si antenna coupled tunneling diode.

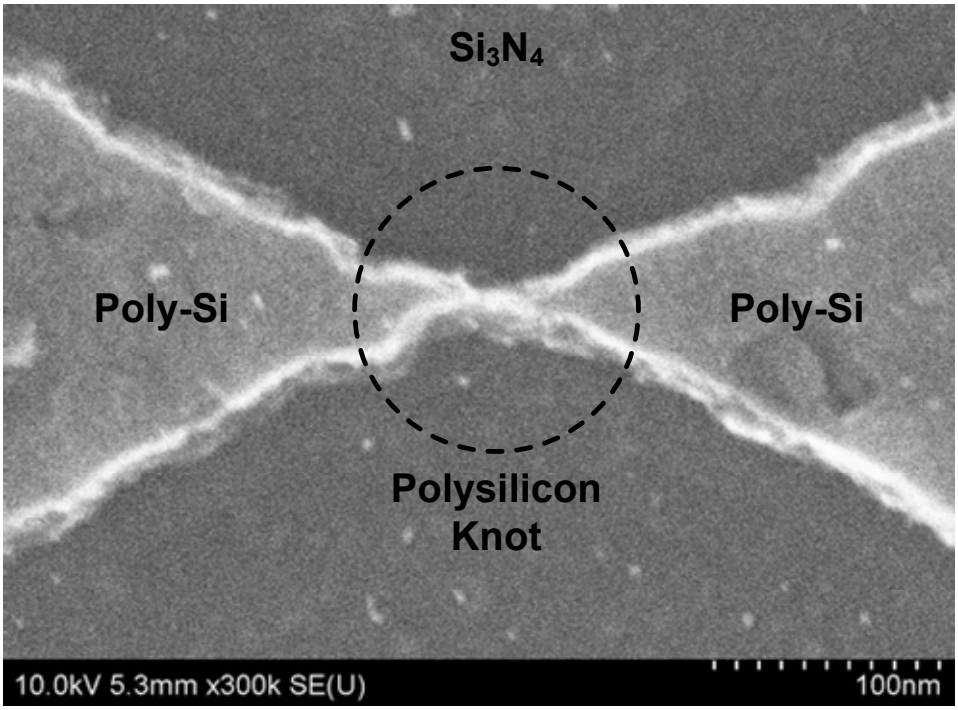

Figure 5.3: A SEM image of poly-Si knot after poly-Si RIE etching process.

5.1.2 Boiling Water Oxidation

As stated above, tunneling diodes require a very thin tunneling barrier. As implemented in a planar structure such as an optical antenna, these tunnel layers are very hard to achieve. To solve this technical issue, we first developed a boiling water oxidation process applied to patterned poly-Si.

The boiling water oxidation process accelerates growth of the native oxide on the surface [65]. By repeatedly applying this oxidation process and oxide etching process to the poly-Si knot shown in Figure 5.3, a thin SiO_2 tunneling barrier is implemented between two poly-Si electrodes.

To check the poly-Si etch rate by the boiling water oxidation and the BOE

etching process, an experimental cycle is set as a 20 second etching in BOE and 1 minute oxidation in boiling water. The etch rate is monitored by a SEM (Scanning Electron Microscope) for different number of cycles on different samples. Figure 5.4 shows the etching and oxidation result of 16 separated samples and the associated linear fit to the data. The controllable and repeatable nature of the process is shown by the degree to which the data conform to the "best-fit" line. Similar data has appeared in the literature [65].

Through the linear fit, we got a slope of 0.71 and an intercept of 4.78. This means that the average lateral poly-Si etching rate is 0.71 nm per cycle and the initial thickness of surface oxide layer on poly-Si in our process is 4.78 nm. Based on these results, the average etch rate is determined as 7 Å/cycle.

This etch and boiling process is applied to a real device, which have really tiny knot size as shown in Figure 5.3. Before the first oxidation, the native oxide layer is etched out using BOE. Then, the sample is oxidized in boiling water for 1 minute. The etch and oxidation processes are repeated until an oxide barrier is formed at the bowtie. At each step, the process is monitored by DC current-voltage (I-V) measurement. Finally, when a nonlinear current-voltage characteristic is achieved through the measurement, the device is checked with a SEM. The process in steps needed to make a tunneling barrier are described below.

STEP 1. Initial device is checked using a SEM.

STEP 2. DC I-V measurement using a probe station and a parameter analyzer.

STEP 3. Applying one cycle of oxide etching & boiling water oxidation process.

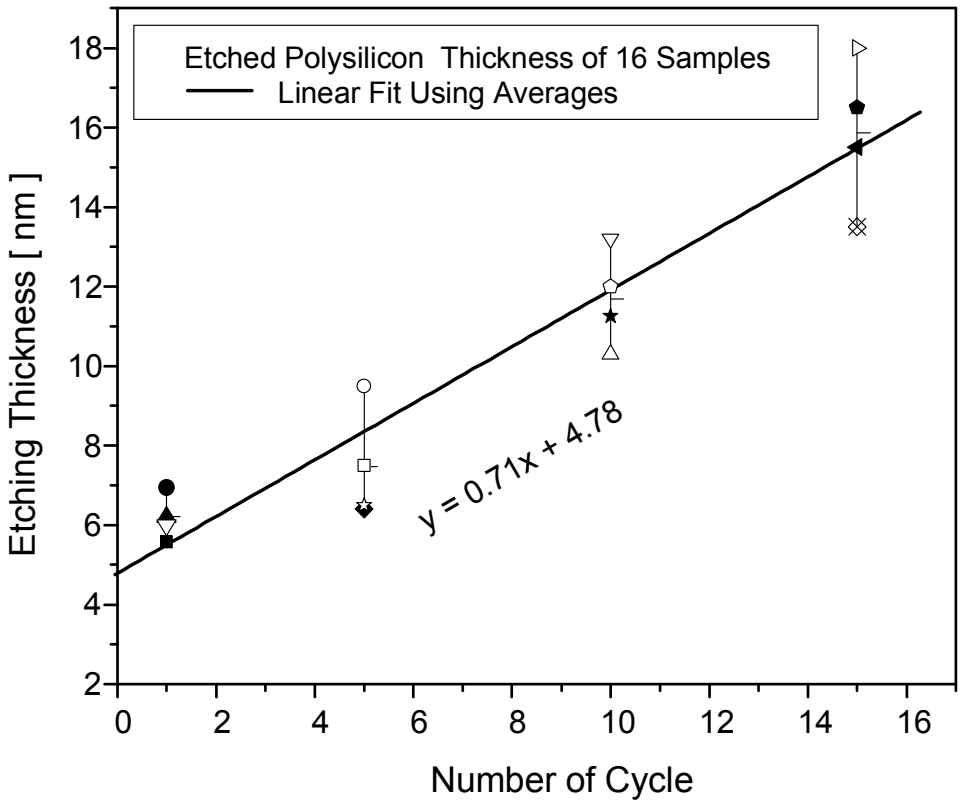

Figure 5.4: Boiling water oxidation data.

STEP 4. DC I-V measurement.

STEP 5. Repeating STEP 3 & STEP 4.

STEP 6. Checking the device using a SEM.

STEP 5 is conducted until the DC I-V property is changed from linear to nonlinear. This creates an in-situ probe of tunnel layer growth. Figure 5.5 shows two SEM images of a poly-Si bowtie device before and after one cycle of the etching/oxidation process. The SEM images show that the poly-Si knot is clearly etched out after one cycle etching and oxidation process for this diode. Figure 5.6 shows

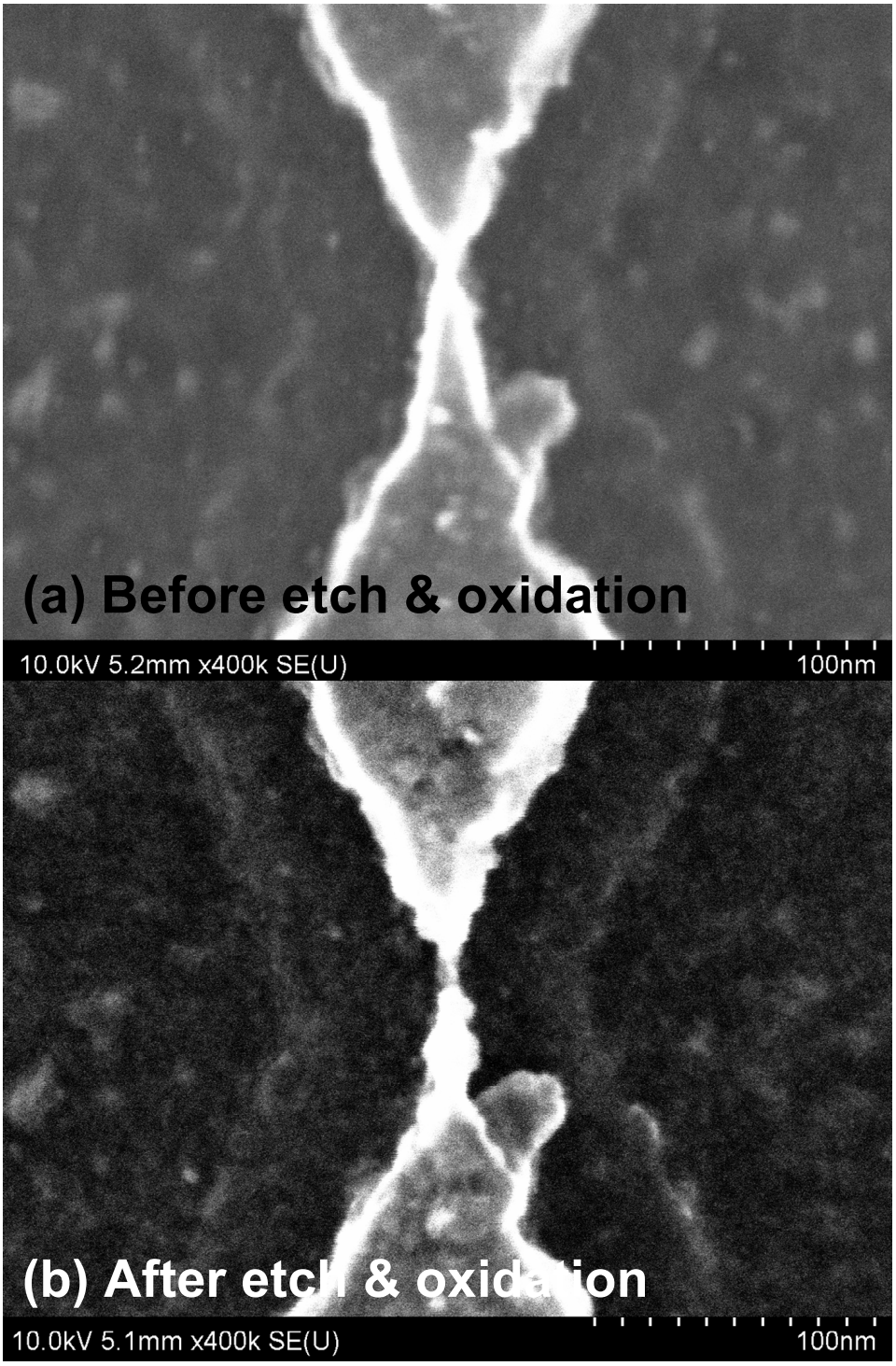

Figure 5.5: Before (a) and after (b) boiling water oxidation.

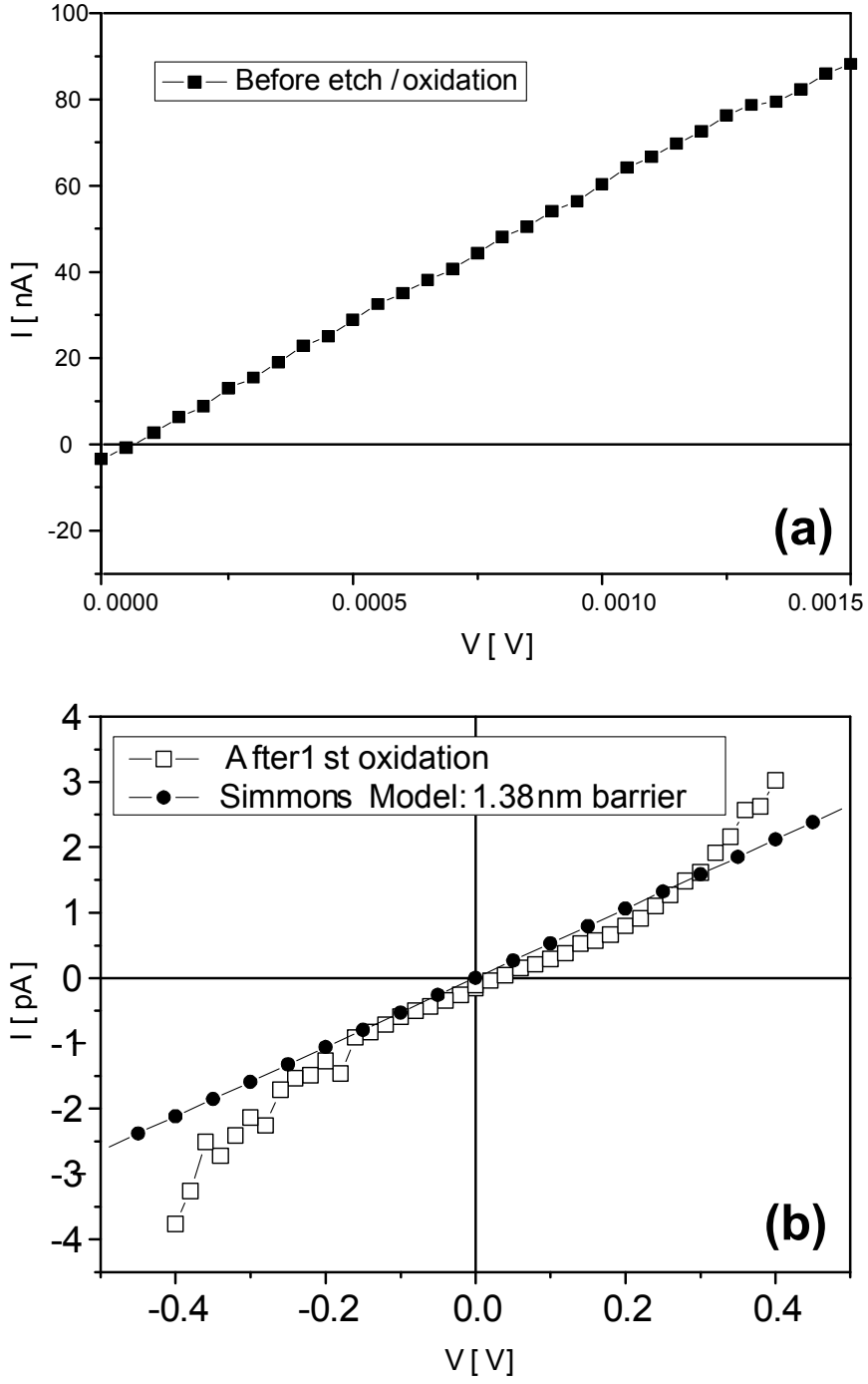

Figure 5.6: DC current measurement resutls: (a) before the etching & boiling water oxidation process, and (b) after one cycle process of the etching & boiling water oxidation process.

measured DC I-V data. For this specific case, only one cycle of etching and oxidation process is enough to implement a SiO_2 tunneling barrier between poly-Si patterns, and the conduction property change from linear to nonlinear verify the tunneling barrier. In the Figure 5.6(b), the filed circle line is a theoretical fit using Simmons's tunneling current model [18]. For the fit, the junction area is assumed as 60 nm^2. The theoretical fit yields 1.38 nm oxide thickness.

5.2 Asymmetric Tunneling Diode (ATD)

A second type of tunneling diode has been developed using the GFE technique in order to improve nonlinearity and asymmetry characteristics of tunneling currents. That is, the main target is demonstrating the GFE technique through asymmetric tunneling currents in a tunneling diode. The details and benefits of the GFE technique are discussed in chapter 2. In this approach, a single triangular electrode shape is chosen for the first electrode. It is blanked with a second metal patch, shown in Figure 5.8. The motivation for the second design is discussed below.

5.2.1 Asymmetric Tunneling Diode (ATD) Fabrication

The critical issue in developing an ATD using the GFE technique is the sharpness of the first electrode tip. In this 2nd type diode development, a poly-Si layer is used for a pointed electrode mainly because a sharper electrode tip can be obtained compared to a metal electrode. Two common methods for metal patterning are tested: metal lift-off and wet metal etching. The patterning resolution of both

processes is degraded, as compared to the acuity achieved by the reactive ion etching of poly-Si. As the required unit processes for a point electrode have been fully developed and optimized through the previous planar tunneling diode development, a poly-Si electrode is used in the ATD development. The fabrication procedure of ATDs is listed below.

1. *Si_3N_4 deposition*
2. *Poly-Si deposition*
3. *Poly-Si Doing*
4. *1st pointed electrode E-beam patterning*
5. *Reactive ion etching (RIE)*
6. *Applying boiling water oxidation process*
7. *Surface oxide etching for metal contact*
8. *2nd plane electrode patterning*

The substrate preparation and poly-Si electrode patterning steps from step 1 to 5 are the same as the first planar tunneling diode process disclosed. But only a single poly-Si electrode is made first using e-beam writing and RIE etching process in step 4 and 6. Figure 5.7 shows the result of a sharp poly-Si electrode.

For implementing a thin tunnel barrier on the first pointed poly-Si electrode, the boiling water oxidation process is used. Before the oxidation, native oxide is removed using BOE. Then, the sample is oxidized in boiling water for 5 minute.

The next step is the oxide etching process, to open a contact to the poly-Si

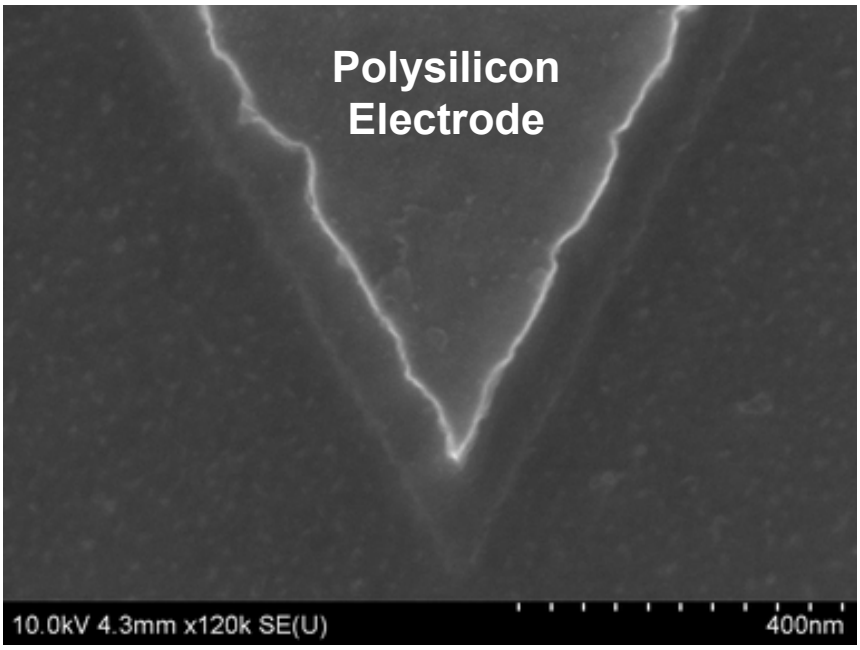

Figure 5.7: A pointed poly-Si electrode shape after RIE etching process.

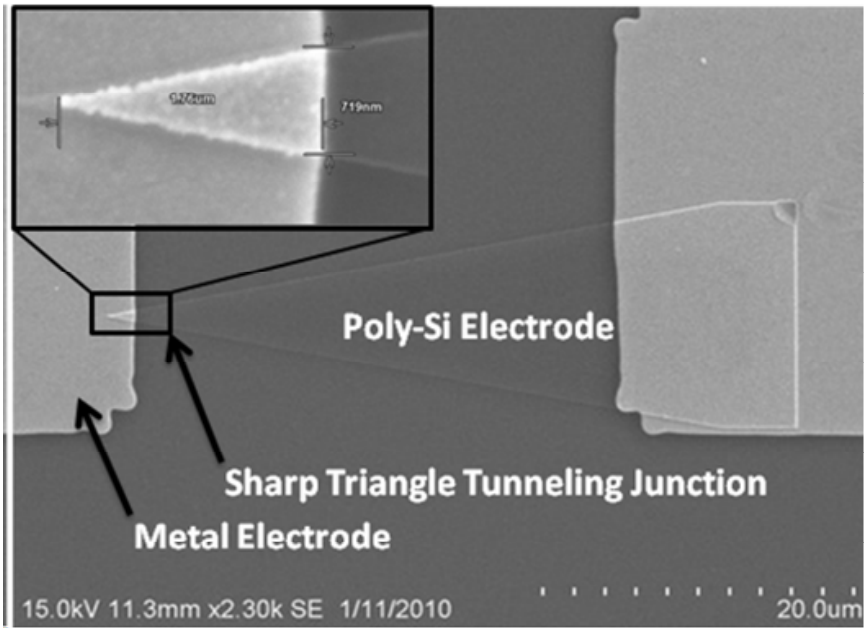

Figure 5.8: A completed asymmetric tunneling diode.

electrode. This is necessary since the entire surface is oxidized during the oxidation process. For this oxide etching process, a common photo-lithography and BOE etching is performed. The photo-lithography is performed using PR-1813 positive photo resist and a contact aligner.

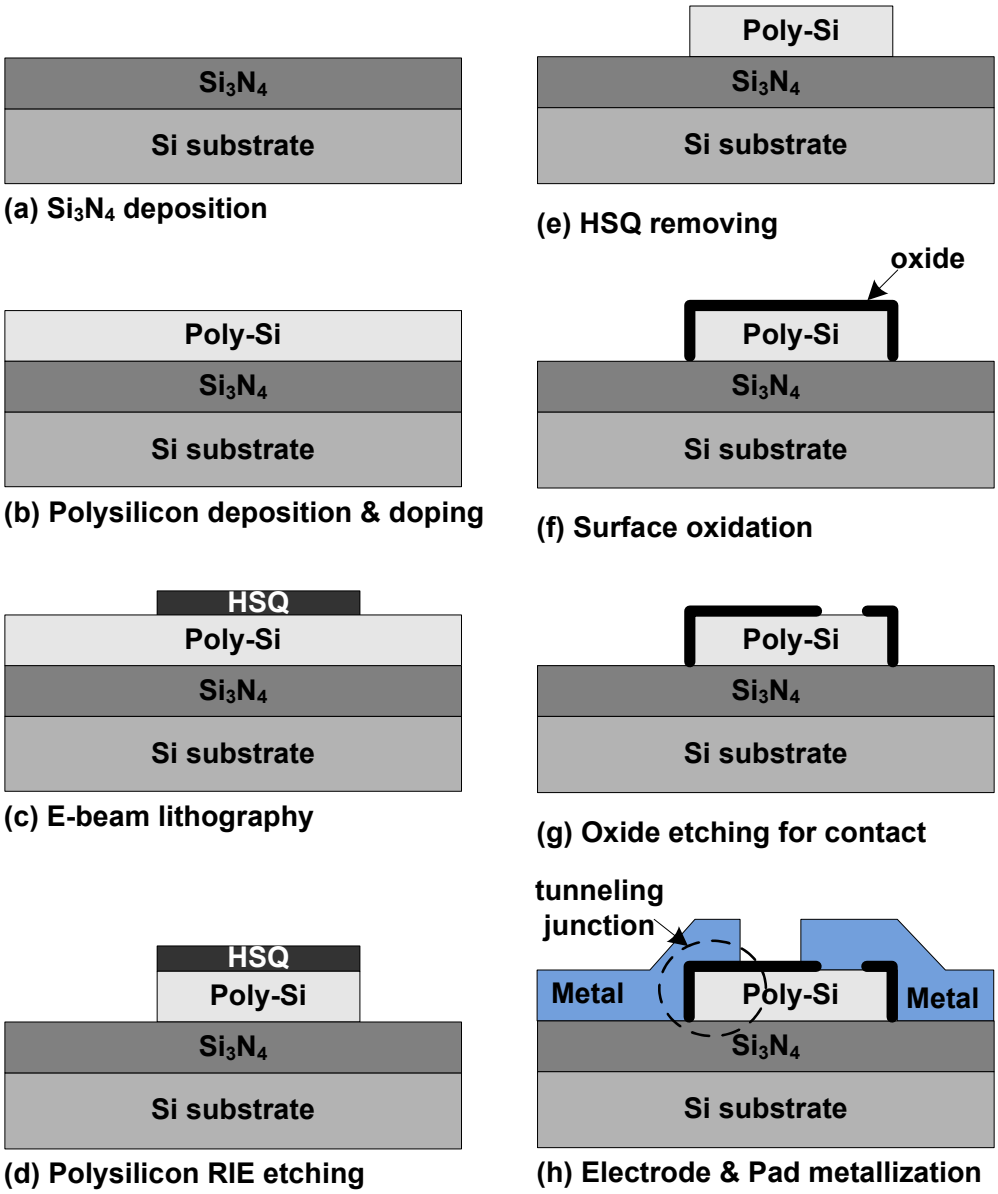

Figure 5.9: Asymmetric tunneling diode process flow.

Finally, a metal pad on the poly-Si electrode and another plane metal electrode, covering the sharpened tip of the poly-Si triangle, are made by photo-lithography and Ti/Au metal lift-off process. A e-beam metal evaporator is used for the late metallization, and the evaporated thickness of Ti and Au is 100 Å and 1500 Å , respectively. Figure 5.8 shows a completed asymmetric tunneling diode, and the inset figure shows the overlapped tunnel junction area between a bottom poly-Si electrode and a top Ti/Au electrode. A schematic representation of the entire process flow is shown in Figure 5.9. The detailed process recipe of the ATD fabrication is added in Appendix A.

5.2.2 Crossbar Tunneling Diode Fabrication

For the asymmetric tunneling diodes described above, the tunneling structure consists of a doped poly-Si, SiO_2, and Ti. The work-function of the poly-Si and Ti is not same so that asymmetric tunneling current can be generated from the work-function difference, not from the effect of the GFE technique. To verify geometric effects on tunneling current, we compared the asymmetric structures to another tunneling devices prepared by using crossbar patterns.

The crossbar devices, which do not have such a sharp corner, are fabricated using exactly same procedures with the triangle tunneling diodes at the same time. Instead of a triangular poly-Si electrode, a rectangular poly-Si bar is crossed over by another Ti/Au metal bar, separated by a thin SiO_2 tunneling barrier using the boiling water oxidation process. This crossbar diode is similar to the basic "edge-

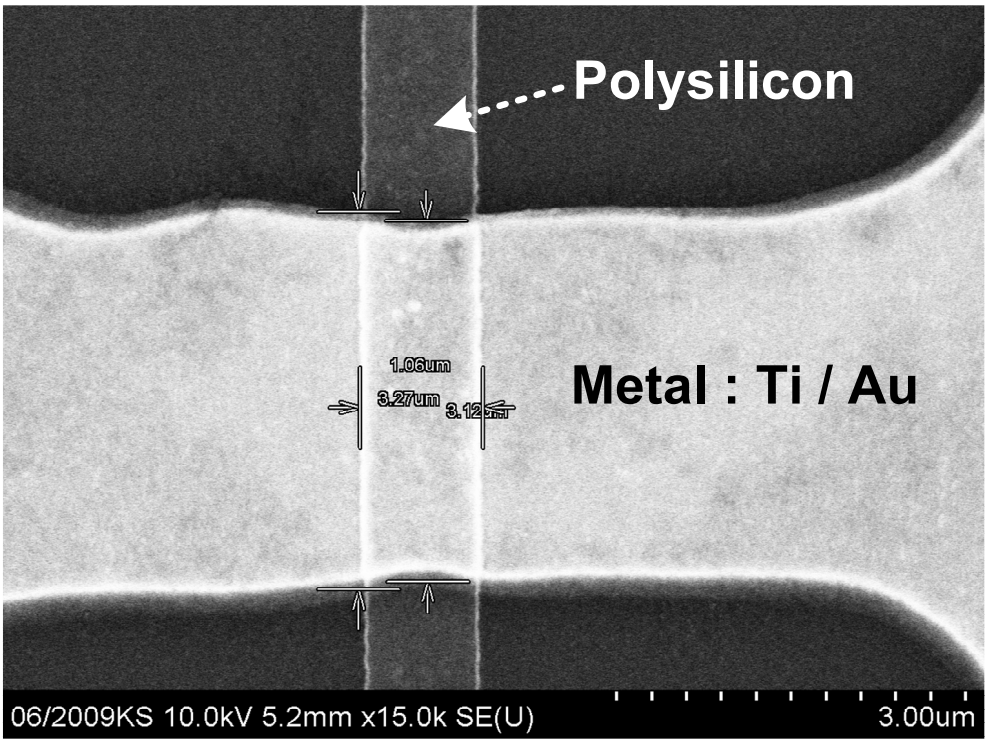

Figure 5.10: A completed crossbar tunneling diode.

MOM" structure originally presented by Heiblum and Gustafson [9]. Figure 5.10 shows a completed crossbar tunneling diode.

5.2.3 An Asymmetric Tunneling Diode with Low Junction Capacitance

This section describes a simple and effective technique to reduce junction overlap capacitance by installing a sacrificial insulator between the two electrodes. A thin Si_3N_4 layer is deposited on poly-Si after the doping process, and the same diode fabrication processes are applied. Figure 5.11 shows a completed ATD with a Si_3N_4 sacrificial layer on the top of the 1st poly-Si electrode. The Si_3N_4 is deposited

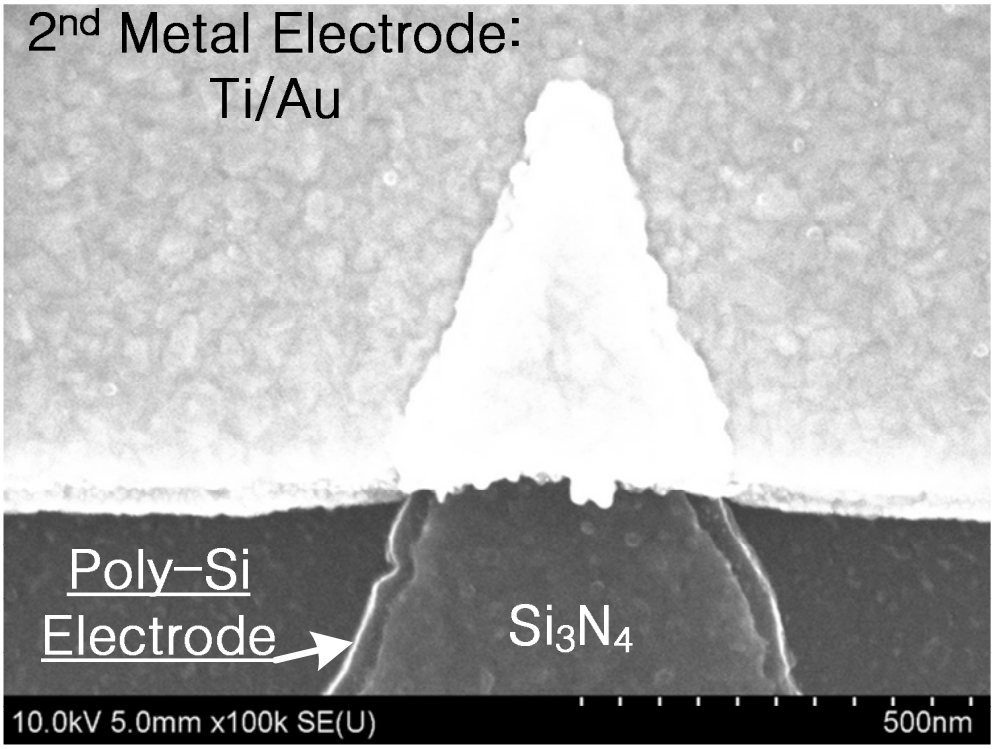

Figure 5.11: A completed asymmetric tunneling diode with a Si_3N_4 sacrificial layer.

using PECVD. The nitride thickness is targeted as 300 Å . Because the deposited Si_3N_4 is completely etched away during the RIE etching process (as shown in Figure 5.11), the critical boundary and tip of the point poly-Si electrode can be maintained, allowing for geometric field enhancement.

5.3 Focused Asymmetric MIM Tunneling Diode

The tunneling current level of the previous asymmetric tunneling diodes could be significantly improved by lowering the relatively large tunnel junction area and by using a metal electrode which has higher conductance than a doped poly-Si.

However, the increased current level still does not provide an RC response time short enough for infrared operation. More improvement of tunneling current is clearly required. We begin by replacing the first poly-Si electrode with a metal to lower parasitic resistance.

5.3.1 Ni-NiO-Ni Tunneling Diode Fabrication

In previous work, the geometric field enhancement(GFE) technique is demonstrated using poly-Si asymmetric tunneling diodes. The same scheme is applied to a metal electrode, and the developed asymmetric MIM tunneling diodes are referred to as Focused Asymmetric Metal-Insulator-Metal (FAMIM) tunneling diodes. To maximize tunneling current, Ni and NiO is selected for the electrode and the tunneling barrier material, respectively. The process flow of the FAMIM diodes is listed below.

1. *Si_3N_4 deposition*
2. *1st pointed electrode E-beam patterning*
3. *Ni metallization & liftoff*
4. *Surface oxidation using oxygen plasma*
5. *2nd electrode E-beam patterning*
6. *Ni metallization & liftoff*
7. *Wire bonding pad metallization*

In order to isolate the diodes from the substrate and lower the pad-to-substrate

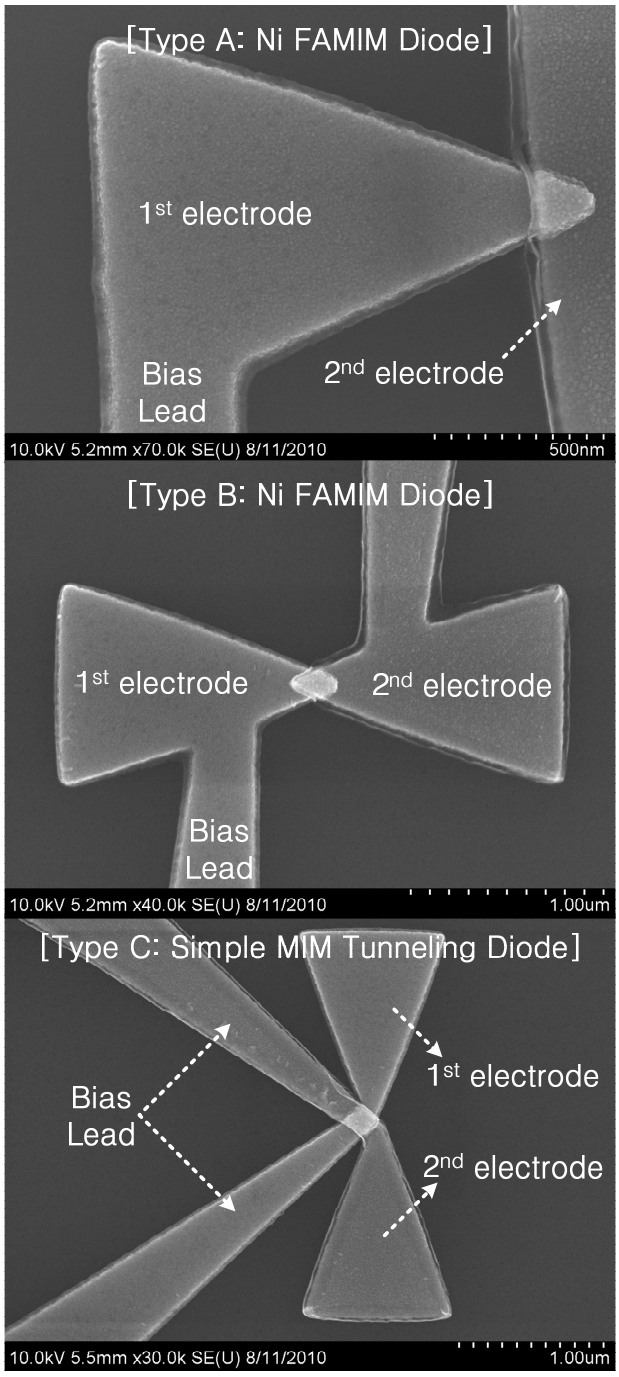

Figure 5.12: SEM images of completed MIM diodes. Type-A and Type-B diodes are two different FAMIM didoes, and Type-C diodes are prepared to use reference MIM diodes for performance comparison. All diodes have a Ni-NiO-Ni structure.

capacitive coupling, dry oxidation was used to create an SiO_2 layer. This was followed by nitride deposition using PECVD on SiO_2. For electrode patterning, e-beam writing is used on a PMMA e-beam resist. A 10 KV acceleration voltage and 10 μm aperture size result in 32 pA current, and 160 $\mu C/cm^2$ electron dose is used for pattern writing. A Ni layer of 700 Å is evaporated using an e-beam evaporator for the 1st electrode. After the metal lift-off step, a surface oxidation process is performed using RIE with oxygen plasma for the 1st electrode. For the final step, the second electrode is formed using the same e-beam patterning and a metal lift-off process with the same thickness of the first Ni layer. In the case a thick metal pad is required, thick Ti/Au metal pads are fabricated using an image-reversal process with AZ5214 photo resist and metal evaporation process.

Three different tunneling diodes, Types-A, B, and C, have been designed and fabricated to demonstrate the GFE effect in MIM tunneling didoes. The fully fabricated Ni-NiO-Ni diodes are shown in Figure 5.12. A triangular electrode shape is chosen to maximize "lightning rod" effect by implementing a bowtie antenna geometry again. The Type-A diode design, consisting of a pointed electrode and a planar electrode, is the same structure as the previous poly-Si asymmetric tunneling diodes. The Type-B diode is designed to achieve a symmetric bowtie antenna with two pointed triangular electrodes, and Type-C is prepared as a conventional MIM tunneling diode with a simple overlapped structure for comparison. The process details of Ni-NiO-Ni tunneling diodes are described in Appendix A.

Angle	Dose (μC/cm^2)				
(°)	100	120	140	160	180
18	20 nm	20 nm	20 $\sim$ 30 nm	20 nm	20 nm
30	30 nm	25 nm	15 $\sim$ 25 nm	20 nm	20 nm
45	30 $\sim$ 40 nm	30 nm	20 nm	20 nm	40 nm
60	50 $\sim$ 60 nm	30 $\sim$ 40 nm	40 nm	40 nm	50 nm

Table 5.1: Tip diameter of Ni triangular electrode.

5.3.1.1 E-beam Patterning Optimization

As same as poly-Si ATM fabrication, the critical issue in the FAMIM diode fabrication is the sharpness of the first electrode tip. Initially, three common methods are explored to find the best process for a pointed metal electrode: metal lift-off, metal wet-etching, ion-milling process. Among the processes, metal lift-off shows the best patterning resolution. However, the tip sharpness is degraded compared to a poly-Si electrode when it is fabricated by a lift-off process.

To optimize the tip sharpness, e-beam patterning resolution is investigated for various tip angles and electron doses. Test patterns are prepared and followed by a Ni evaporation, and lift-off process. Using the SEM, the tip diameter of each triangular electrode is measured and listed in Table 5.1. The sharpness of the triangular tip creates the angle and electron dose dependency, as shown in Table 5.1. This dependency seems to be saturated below a certain tip angle. Based on this e-beam patterning test, a tip angle and electron dose of 45° and 160 μC/cm^2,

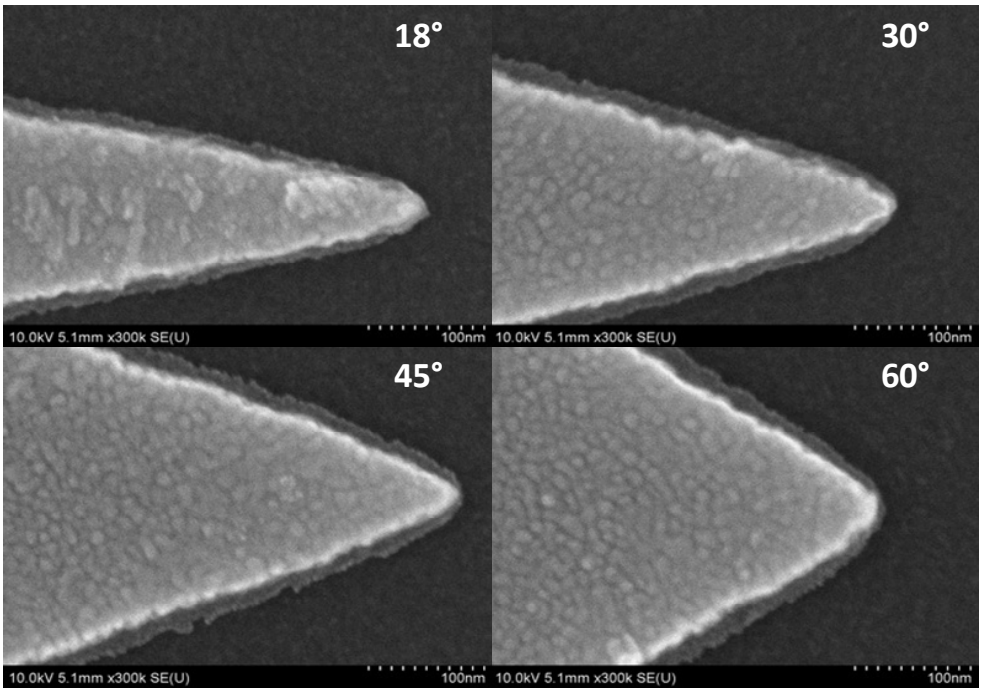

Figure 5.13: SEM images for e-beam patterning optimization. A 160 μC/cm^2 electron dose is used for all patterns in this figure. For the 160 μC/cm^2 electron dose, three patterns of 18°, 30°, and 45° have almost same tip sharpness as 20 nm diameter.

respectively, is selected for a basic diode patterning process. Figure 5.13 shows the tested patterns for four different angles with a 160 μC/cm^2 electron dose.

5.3.1.2 NiO Surface Oxidation

The quality of the tunnel barrier dominates in determining ultimate rectifying performance. Simmons claims that the thickness of a tunneling barrier should be kept below 40 Å to sustain tunneling current as the main transport mechanism in a MIM tunnel junction [12]. Above 40 Å, thermionic currents become dominant. If thermionic current is dominant, the junction cannot respond to infrared waves be-

cause the thermionic transition process is too slow to respond at infrared frequencies [9]. Thus, a thin oxidation barrier is necessary for MIM tunneling diodes.

In the FAMIM diode process, we used an RIE oxygen plasma process to form the tunnel oxide. By measuring the tunneling resistance at zero bias for the Type A FAMIM diodes, the controllability and repeatability of the plasma oxidation process is verified. In the oxidation process, the exposure time to oxygen plasma is controlled and the other process conditions are kept constant. An RF power of 50 W and an oxygen pressure of 150 mTorr are used throughout.

Table 5.2 shows the measured tunneling resistances for three Type-A FAMIM diodes. The barrier thickness is extracted using a theoretical equation derived by Simmons [18] (Eq. (43) in the reference). For the extraction, a nickel work-function of 5.15 eV and a barrier height of 0.3 eV are used. The barrier lowering effect at the second electrode side is ignored in the extraction. As listed in Table 5.2, the tunneling resistance increased as the exposure time is extended. For three different oxidation times, a thin oxide layer below 40 Å is obtained. However, the tunnel junction resistances are relatively high compared to other reported diodes [10]. The high resistance is thought due to two factors: relatively thick tunneling barrier and thin metal thickness. Such high resistance reduces power transfer efficiency from an integrated antenna to a tunnel junction. Therefore, further process optimization for oxidation is required for lowering the tunneling resistance in the FAMIM diode fabrication.

Time (second)	Junction Area (μm^2)	$1/I'$ (Ω)	Barrier Thick. (Å)
20	0.04	360K	23
40	0.04	16M	33
60	0.039	100M	35

Table 5.2: Differential tunneling resistance at zero bias.

5.3.2 Low Tunneling Resistance by Boiling Water Oxidation

For thin film MIM tunneling diodes, various metal oxidation processes are available such as oxide sputtering and oxide evaporation. In the FAMIM diode fabrication, oxygen plasma is used to form a thin metal oxide layer using RIE. The details are described in the previous section. However, the obtained oxide thickness is not very thin as shown in Table 5.2. A thinner oxide layer might be achieved on a Ni surface by reducing the oxygen pressure and exposure time.

On the other hand, the boiling water oxidation which is used for poly-Si electrodes is easy to execute testing the process for Ni electrodes. Thus, the boiling water oxidation is applied with two different solutions: one is using pure de-ionized (DI) water, and the other is using a ZnCl solution. The purpose of using ZnCl solution is to provide traps in a tunneling barrier to increase tunneling current by implementing Frenkel-Pool emission. For both oxidation processes, 1 minute boiling is applied. Figure 5.14 shows the measured tunneling resistance (R0) at zero-bias condition. Compared to oxygen plasma oxidation, very small tunneling resistances are obtained through boiling oxidation process. For example, a tunneling diode of

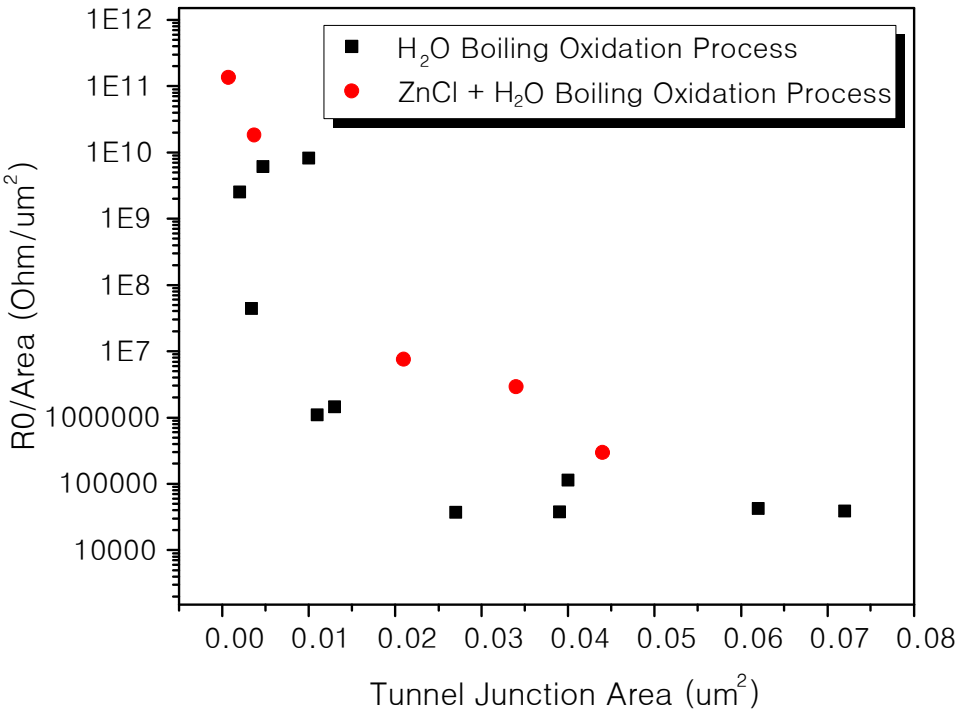

Figure 5.14: Boiling water oxidation results for MIM tunneling diodes. ZnCl solution for surface oxidation

0.04 μm^2 junction area has a tunneling resistance of 1.45 KΩ at zero bias. However, for the same junction size diode oxidized by the oxygen plasma process, the zero bias resistance is 360 KΩ as listed in Table 5.2.

Surprisingly, the ZnCl solution gives higher tunneling resistance compared to the pure water oxidation process. This might be explained by a longer transition time through traps inside a tunneling barrier. More work is necessary to optimize the oxide doping effect on MIM tunneling resistance.

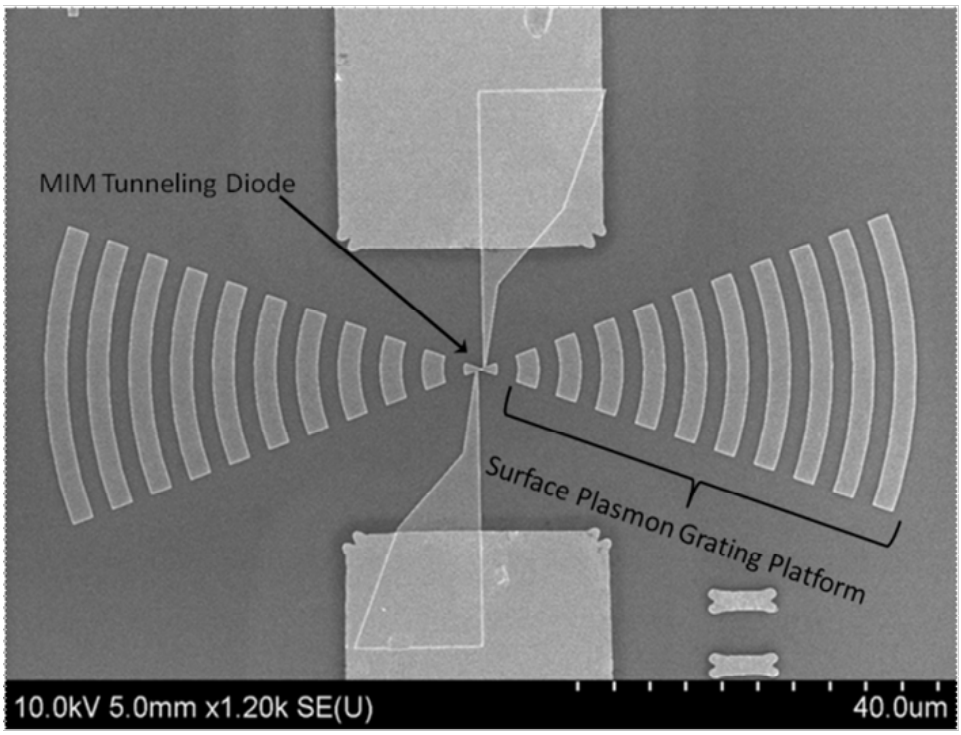

Figure 5.15: A FAMIM diode with a surface plasmon grating platform

5.3.3 Plasmon Grating Platform

In chapter 4, a grating scheme is introduced as a way to further use of surface plasmon or surface plasmon resonances in tunneling diodes. Figure 5.15 shows a FAMIM diode which has a fan-shaped ring grating platforms at each side. The grating period is 2.4 μm and obtained from infrared frequency simulations using the RF module of COMSOL simulator. There are many types of different grating structures for generating surface plasmons [62, 63, 66]. Finite difference wave simulations can be used to find the proper grating scheme for IR rectification.

5.4 Discussion

Perfect planar tunneling diodes have been demonstrated using poly-Si electrodes. This has a significant meaning because such a planar type tunnel junction is a very rare structure in tunneling diodes. Another achievement is developing the boiling water oxidation process. A thin tunneling barrier is successfully implemented using the boiling water oxidation process. The measured nonlinear DC current demonstrates the tunneling current through the barrier. This oxidation process can provide another option to make a tunneling barrier in tunneling diodes. Furthermore, if the developed planar tunneling diode thus developed is used as an optical antenna, it should provide a large electric field enhancement due to the extremely small gap size.

In planar type tunneling didoes, one of the critical geometric parameters is the knot size, which is defined by e-beam writing and RIE dry etching. When the knot is not very small, the poly-Si patterns all are etched out after repeating the etching and oxidation process several times. Usually, a 10 - 20 nm knot thickness is achievable for the etching and oxidation process. Such a small knot size can be achieved based on optimized e-beam writing and REI etching conditions. All successfully fabricated devices have such small knots.

However, the planar type diodes have some drawbacks. The first thing we observe is a large tunnel junction resistance. This causes the impedance matching problem when the tunnel junction is coupled with an antenna. Also, the current level is so low that the current non-linearity (or I-V curvature) would be very small.

Therefore, it is difficult to achieve good rectifying performance in the planar type tunneling diodes. The second issue is that devices are prone to electro-static discharge (ESD) overstress. Careless sample handling caused serious damages to the devices through ESD. For example, many devices are burnt-out during gold wire bonding on metal pads. It is believed that the low current conductance of the tunneling diode is the main reason for ESD susceptibility. A final drawback is process control. The new process is not complex itself. But all devices could not be processed in parallel due to process variations of diodes, especially for the e-beam patterning process. More specifically, each bowtie pattern, after RIE dry etching, has a different knot thickness. To make a thin oxide barrier, each knot needs a different number of etch/oxidation cycles. Therefore, only a single device could be processed at a time.

The most important achievement of the ATD process is developing an overall process to implement the GFE technique using a pointed poly-Si electrode. The ATD process solves the process difficulties in the asymmetric tunneling diode process. Tunnel junction size is controlled by changing the overlap size of the two electrodes. Again, we aim to have higher tunneling current capacity. This higher current capacity improves the ESD robustness of the ATDs, and increases process yield (compared to the planar type diodes). The ATD fabrication process is simple, and parallel fabrication processing is possible.

Through the ATD process, it is again emphasized that the e-beam patterning and RIE etching conditions are optimized to generated the sharpest electrode possible, and we have verified the practical use of the boiling water process. Another

Diode Type	Planar Diode	ATD	FAMIM Diode
1st Electrode	Poly-Si	Poly-Si	Ni
Tunneling Barrier	SiO_2	SiO_2	NiO
2nd Electrode	Poly-Si	Ti/Au	Ni
Oxidation Process	Boiling Water	Boiling Water	Boiling water Oxygen Plasma
Pattering	E-beam	E-beam	E-beam
Junction Size	Nonadjustable	Adjustable	Adjustable
Process Yield	Very Low	Very High	Moderate
Current Symmetry	Symmetric	Asymmetric	Asymmetric

Table 5.3: Summary of novel tunneling diode fabrication process.

technique, which can reduce a junction overlap capacitance, has been developed by using a sacrificial Si_3N_4 layer on a poly-Si electrode. When a lower junction capacitance is required, this technique can be useful.

The FAMIM diode process is developed to achieve higher tunneling current in an asymmetric tunneling diodes. The GFE technique is applied to a Ni electrode instead of a poly-Si one of a ATD. Both structurally symmetric and asymmetric FAMIM diodes have been developed. E-beam patterning optimization is performed to obtain a sharp Ni electrode, and a tip diameter of 20 nm is achieved. Through oxygen plasma treatment, a thin tunneling barrier is formed on Ni electrodes. The thinner oxide layer is achieved using the boiling water oxidation. By integrating grating structures to a FAMIM diode, it is possible to generate SPs or SPRs to en-

hance the junction field and lower the MIM tunneling resistance without increasing junction capacitance. Table 5.3 is listed the process details of each tunneling diode developed in this research.

Chapter 6

Tunneling Diode Characterization & Discussion

Diode characterization has been performed on completed tunneling diodes in various tests such as DC current-voltage (I-V) measurements (at room temperature and at 77K), RF rectifying tests, and infrared wave detection tests. The characteristics of each diode type are described and discussed separately, and the benefits of the GFE technique are verified using FAMIM diodes. It will be shown how the performance improvements at DC due to GFE techniques are related to MIM rectifying performance in this chapter.

6.1 Test Setup

6.1.1 DC I-V Test

DC measurement setup is prepared with a parameter analyzer, HP 4156B, and a probe station, HP REL-4800. Figure 6.1 shows the DC I-V measurement setup. This setup is used for room temperature DC I-V tests.

For low temperature tests, diodes are tested in liquid nitrogen to operate diodes at 77 K. Instead of probing, diode's pads are wire-bonded to the pads on a common dip IC package using a gold wire bonder. The bonded IC package is mounted on a IC package socket where the electrical connections between the package and a parameter analyzer are made.

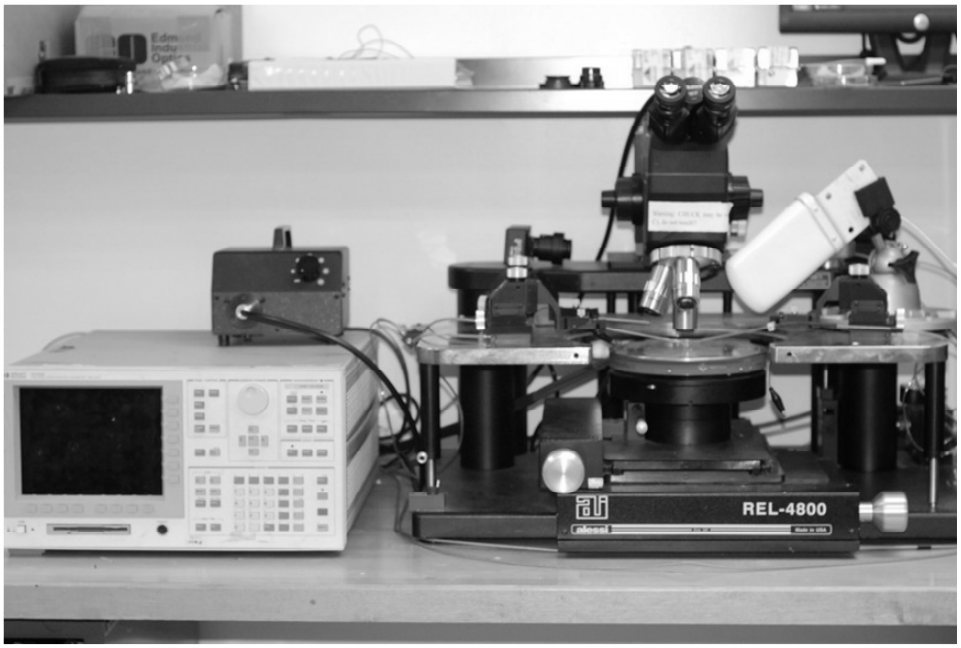

Figure 6.1: Room temperature DC I-V test setup.

6.1.2 RF Rectification Test

For RF rectification tests, a RF source, HP 8350B sweep oscillator, is connected to a commercial RF log-periodic antenna, HG2458-08LP. The RF response is measured using needle-probes contacting the DC bias lines of the tunnel device. These probe tips work as a "rabbit ear" antenna, coupling the RF waves from the transmission antenna to the tunneling diodes. The distance between the transmission antenna and a diode is fixed as 14 cm. During the RF tests, the parameter analyzer and the probe station of DC setup are used to supply DC bias and monitor rectified DC current.

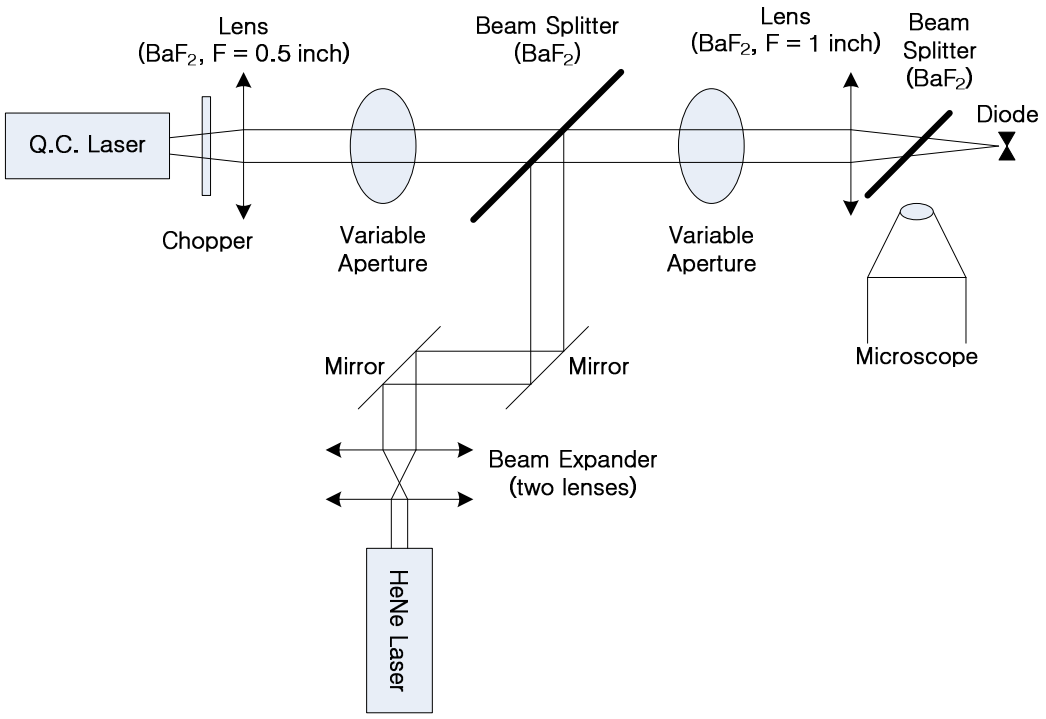

Figure 6.2: Schematic of IR test setup.

6.1.3 IR Rectification Test

The infrared wave testing setup is illustrated in Figure 6.2. In this setup, a quantum cascade laser (QCL) of 9.6 um wavelength is used as the infrared radiation source, and a Helium Neon (HeNe) laser is used as an aligning beam.

First, the QCL is placed at the focal distance (f=0.5) of the first barium fluoride (BaF2) lens so that laser beam is collimated after the lens. A chopper is installed between the laser and the first lens in order to provide a reference frequency to a lock-in amplifier. Two variable apertures are placed in the optical path before the second BaF2 focusing lens (f=1) to align the IR beams to a diode. Second, the aligning beam from the HeNe laser is expanded and collimated by using two

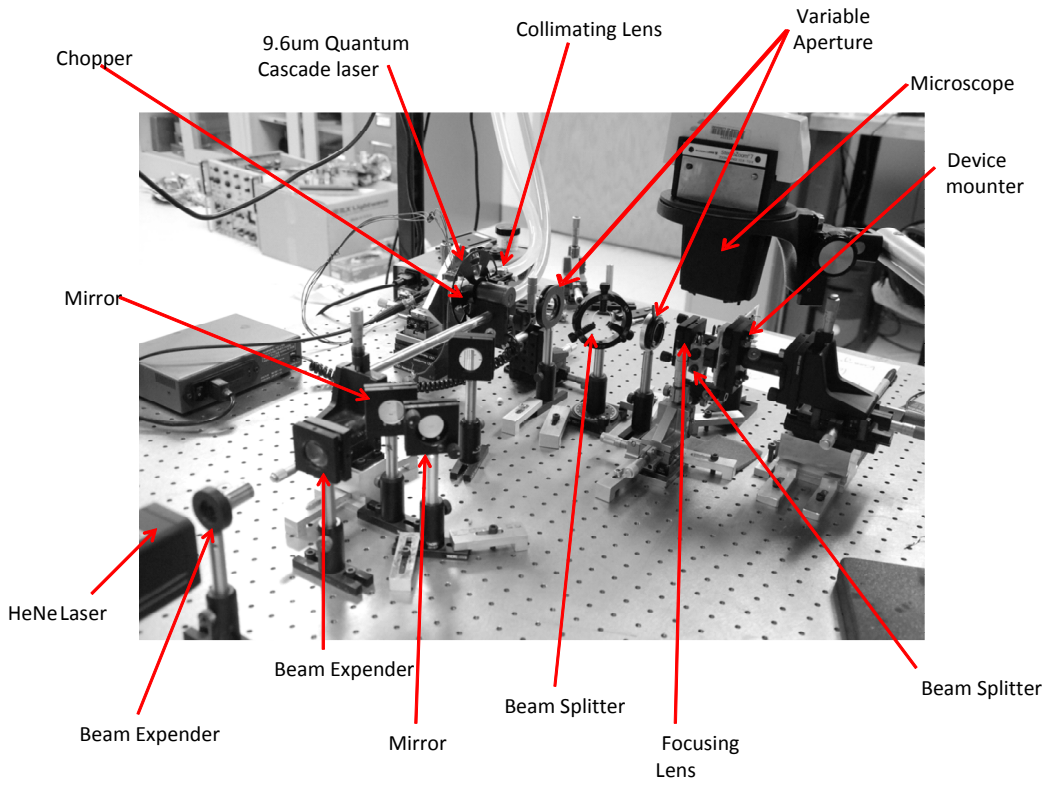

Figure 6.3: IR test setup.

lenses (beam expander). After the beam expander, HeNe laser beam is guided by two mirrors, and the guided beam is split and aligned with the IR beam through the beam splitter. This aligned HeNe laser beam reflects from the sample, and the reflected beam is guided to a microscope through a beam splitter. By aligning the QCL with the HeNe, we can monitor where the QCL is focused on the sample.

Three measuring equipments, a parameter analyzer, a locking amplifier, and a DC power supplier, are used for IR rectifying tests. The rectified DC signal can be monitored using the parameter analyzer or the locking amplifier with a chopper. A sample mount is designed to rotate the sample on an x-y-z stage. Using this IR test setup, the maximum IR power density of 191 W/cm2 is obtained with 10um

spot size on the sample surface. Figure 6.3 shows the completed IR test setup on an optical table. During IR rectifying test, the QCL laser is cooled using both a thermoelectric cooler and water circulation.

6.2 Perfect Planar Type Tunneling Diode

6.2.1 DC Test

The fabrication process and design of planar type tunneing diodes are introduced in chapter 5.1. After DC current-voltage relationship is checked using the DC measurement setup at room temperature, the related DC analysis is conducted as follows. First, a fifth order polynomial fitting is applied to the measured I-V data. Using the polynomial fit, I' and I'' are extracted. The sensitivity is calculated as I''/I', and the tunneling resistance is obtained as a reciprocal of I'. Figure 6.4(a) shows the measured DC I-V data and a fifth order fit for a perfect planar type tunneling diode. Using the polynomial fit, the I' and I'' are extracted and plotted in Figure 6.4(b) and (c), respectively. Figure 6.4(d) shows the calculated sensitivity using the extracted I' and I''. The highest sensitivity of this diode was reached to 6 V^{-1} at 0.35 V. Most fabricated devices had very low current level because of a small tunnel junction area, and the sensitivity is below 10.

The highest sensitivity result is shown in Figure 6.5. The highest sensitivity is 31 V^{-1} at 80 mV, which is the highest ever reported for thin film MIM tunneling diodes. Also, it gives more asymmetric current. The closest reported value is listed in a reference [34] : 13 V^{-1}. Table 6.1 lists sensitivities reported recently from other

groups [67].

6.3 Asymmetric Tunneling Diode

Asymmetric tunneling diode (ATD) is developed to overcome the drawbacks of the previous planar type tunneling diodes. The characteristics of ATDs are introduced and discussed in this section. For all tests, the metal electrode is grounded,

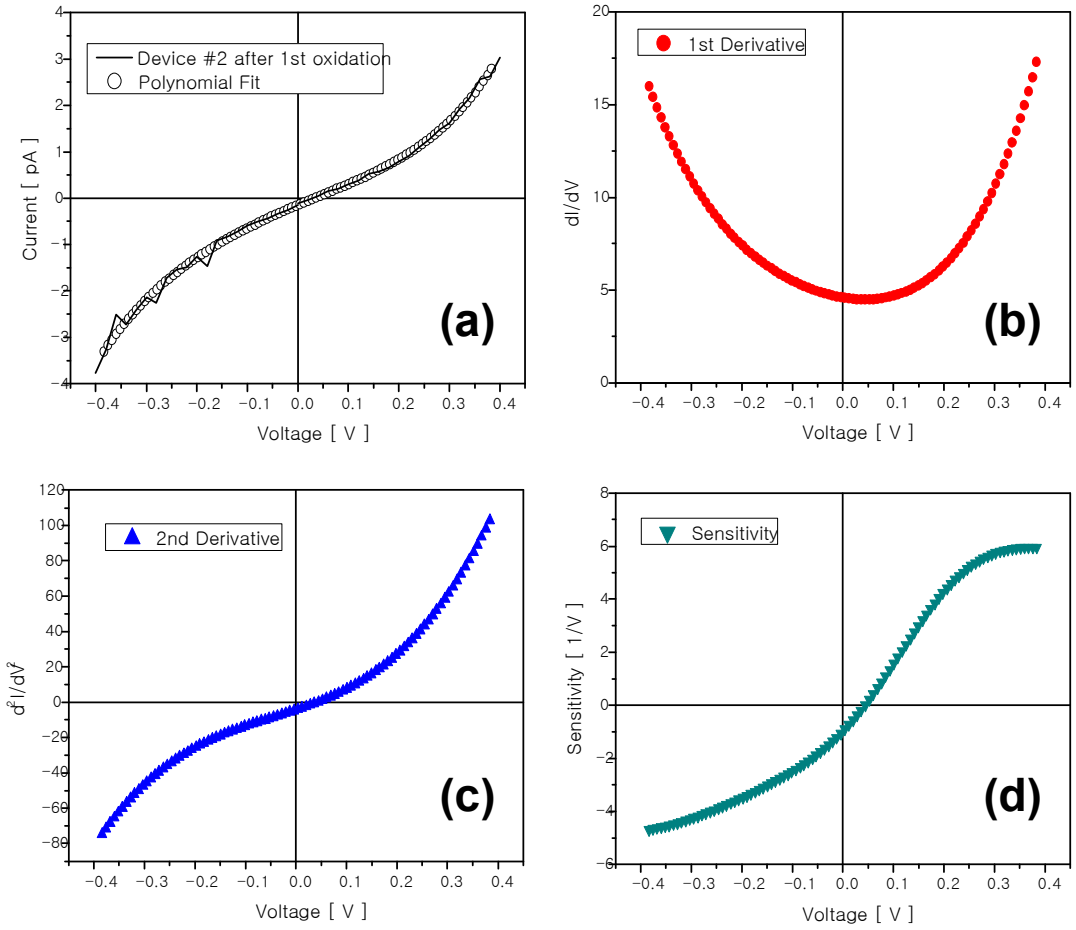

Figure 6.4: (a) DC I-V measured data (solid line) and a 5th order polynomial fit (circles), (b) the 1st derivative of current, (c) the 2nd derivative of current, and (d) device sensitivity.

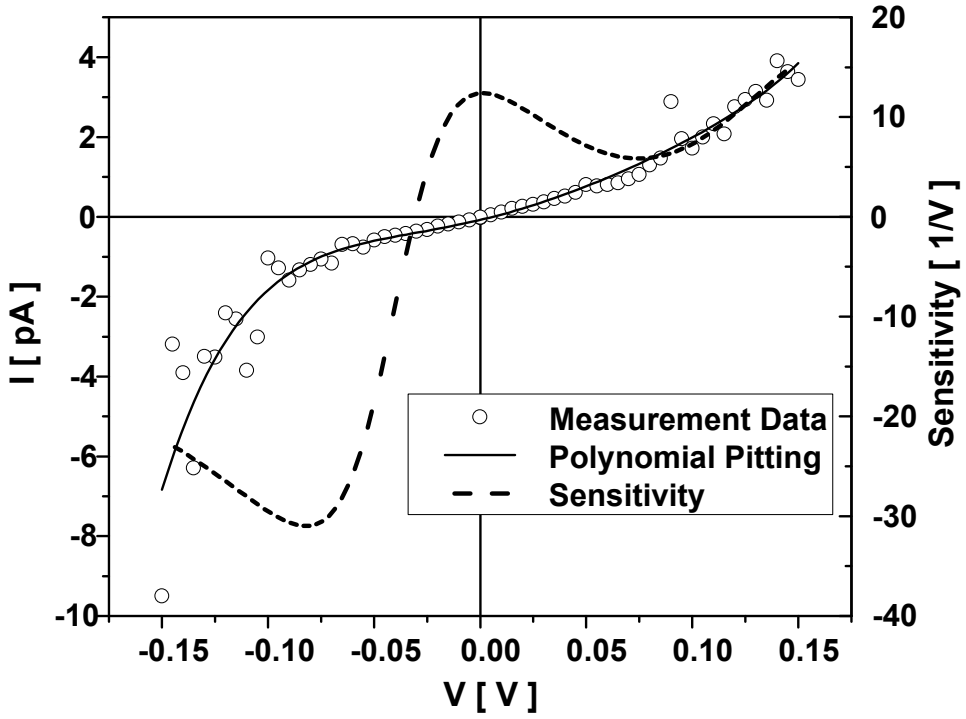

Figure 6.5: I-V measurement data (open circles) and polynomial fit (solid line) of a CIC diode are shown. The sensitivity (dashed line) is calculated and plotted by I''/I' using the polynomial fit.

Authors	Type of Tunneling Diode	Sensitivity (1/V)
A.B. Hoofring	Thin-film Ni-NiO-Au ($0.64\mu m^2$)	4.55
M.R. Abdel-Rahman	Thin-film Ni-NiO-Ni ($0.075\mu m^2$)	2.75
	Thin-film Ni-NiO-Ni ($0.0014\mu m^2$)	1.65
P. Esfandiari	Thin-film Ni-NiO-Pt ($0.0025\mu m^2$)	13
S. Krishnan	Thin-film Ni-NiO-Cr ($1.45\mu m^2$)	5
This Result	Planar-type polysilicon CIC	**31**

Table 6.1: Sensitivity Comparison.

and bias voltage is applied on the poly-Si electrode as defined in chapter 3.

6.3.1 Room Temperature DC Test

The measured DC current-voltage result of an asymmetric tunneling diode is shown in Figure 6.6. As expected, the result shows a manifest asymmetry characteristic of the ATD. The asymmetry factor is calculated as a magnitude ratio of reverse to forward current, shown with a solid line in Figure 6.6. Through the nonlinear I-V relation shown in Figure 6.6, it is demonstrated that the boiling water process makes a proper surface oxide layer on the poly-Si pattern for a tunneling barrier.

Although asymmetric tunneling currents are obtained as expected, the origin of such asymmetric currents is most likely due to the dissimilar electrode materials,

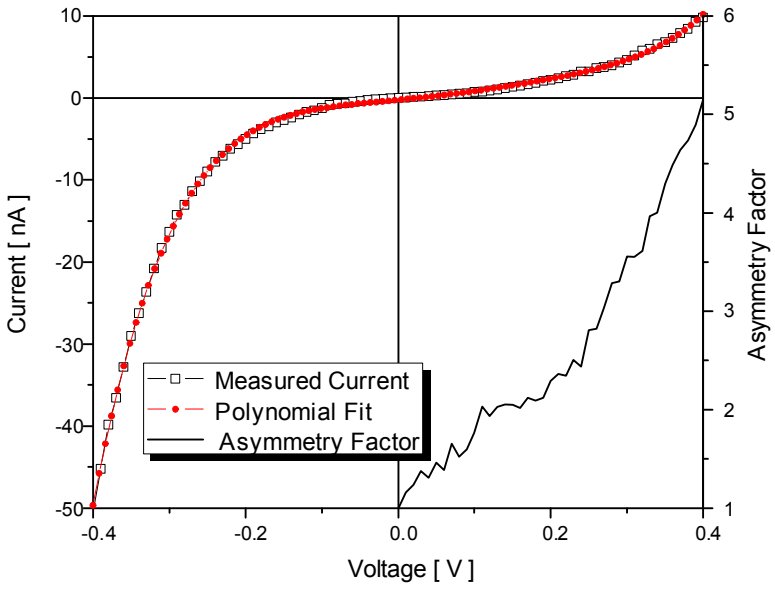

Figure 6.6: Measured asymmetric tunneling current of an asymmetric tunneling diode which has a pointed poly-Si electrode for the GFE technique. The solid line is the calculated asymmetric factor defined as a ratio of reverse to forward current.

a poly-Si and Ti. Therefore, a work-function difference exists between the two electrodes. This difference is about 0.28 eV, and it might create the asymmetric tunneling current.

To verify the origin of the asymmetric tunneling current, crossbar patterns tunneling diodes, shown in Figure 5.10, are prepared and tested. Figure 6.7 shows measured DC I-V data for a crossbar diode, and the inset is a SEM image of the diode with 3.4 um2 junction area. The tunneling current of the crossbar diode shows very weak asymmetry. The asymmetry factor is below 1.2 for entire bias range. This weak current asymmetry is due to the different work functions and density of states between the doped poly-Si layer and Ti. By comparison of the two different devices, it is verified that the strong current asymmetry is derived from the geometric field enhancement of the pointed tip. That is, the GFE technique is

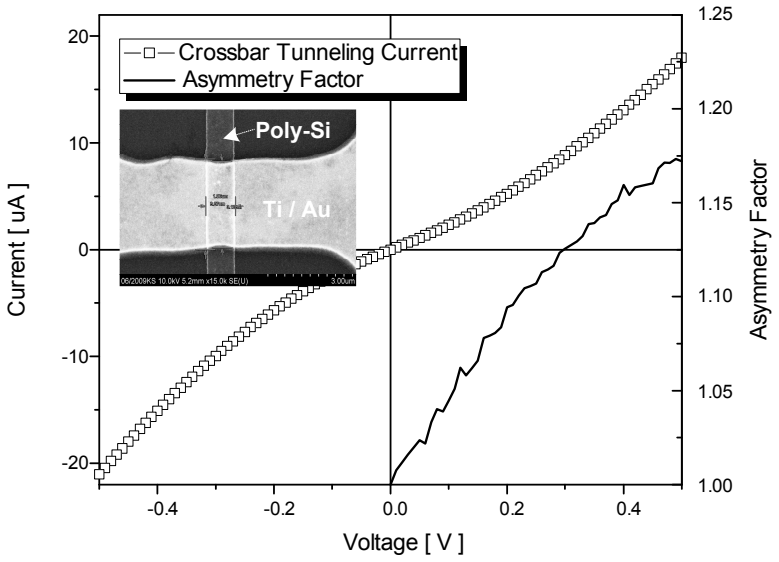

Figure 6.7: Measured DC I-V data of a cross-bar tunneling diode.

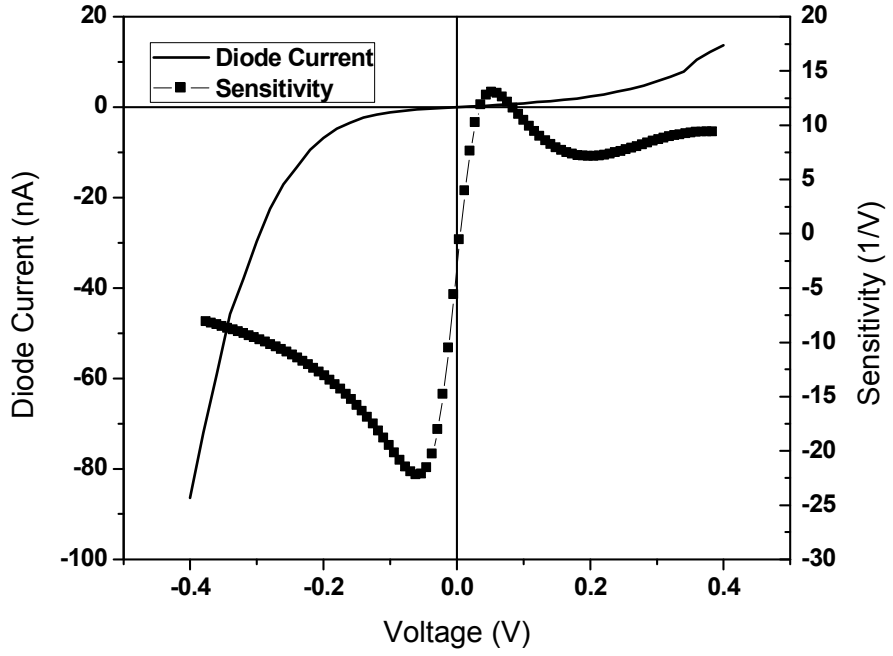

Figure 6.8: Best sensitivity result of a ATD with 0.6 μm^2 junction area. Measured DC current-voltage relationship and extracted sensitivity for a poly-Si ATD. The reverse tunneling current level was much higher than the forward level due to the geometric field enhancement from the sharp tip. The filled square line is the calculated sensitivity.

demonstrated through poly-Si asymmetric tunneling diodes.

Figure 6.8 shows the measured tunneling current and extracted sensitivity of an ATD with the highest sensitivity. The tunneling current plot shows very strong asymmetry in Figure 6.8. The tunneling current at -0.4 V is 6.3 times of the forward current at the same forward bias voltage. The sensitivity plot shows clear improvement under the reverse bias conditions. Generally, the sensitivity of a tunneling diode is proportional to the tunneling resistance, so it is not easy to achieve a high sensitivity from a diode which has a small tunneling resistance or large tunnel junction area. However, comparing with other thin film tunneling diodes listed in

Table 6.1, the ATD shown in Figure 6.8 has a large tunneling junction area and very high sensitivity. The maximum sensitivity is reached at -22 V^{-1} for a -60 mV terminal bias. On the other hand, the maximum sensitivity obtained under forward bias conditions is 13 V^{-1} at +60 mV. The 71 % of sensitivity improvement and the 4.5 times higher current curvature in the reverse bias region demonstrate the superior benefit of the GFE technique.

For performance comparison, specific parameters of an ATD and a crossbar diode are listed in Table 6.2. The nonlinearity improvement reaches to 350 % for the ATD. However, the calculated percentage improvements of sensitivity and nonlinearity in the crossbar tunneling diode is much lower than that obtained for the ATD. The superior performance of the ATD demonstrates the effectiveness of the GFE technique.

6.3.2 77K DC measurement

Low temperature measurements were performed to ascertain the degree to which thermal processes affect MIM current flow. After wire bonding, ATDs were tested at 77 K using liquid nitrogen. Figure 6.9 shows the measured DC I-V data at room and 77K for a ATD of 0.54 um^2 tunnel junction area. At 77 K, the current level is decreased, but it still shows asymmetric and nonlinear current behavior. The nonlinear property at 77 K supports that the current is from a tunneling mechanism. The reduction of tunneling current may be mainly due to a small decrease of the conductance of the doped poly-Si electrode. As shown in measured data,

Diode Type		ATD	Crossbar
Junction Area		0.6 μm^2	3.4 μm^2
Asymmetric Ratio* @ ±0.3 V		5.12	1.13
Max. S (1/V)	Forward Bias	13.01	2.78
	Reverse Bias	22.25	3.22
	Impro.**	71 %	16 %
Max. I″ (A/V^2)	Forward Bias	0.36×10^{-6}	1.62×10^{-6}
	Reverse Bias	8.82×10^{-5}	1.15×10^{-4}
	Impro.**	350 %	30 %

*Asy. Ratio=abs((reverse current)/(forward current))

**Impro.=((reverse factor)-(forward factor))/(forward factor)×100 %

Table 6.2: Performance summary of an ATD and a crossbar tunneling diode.

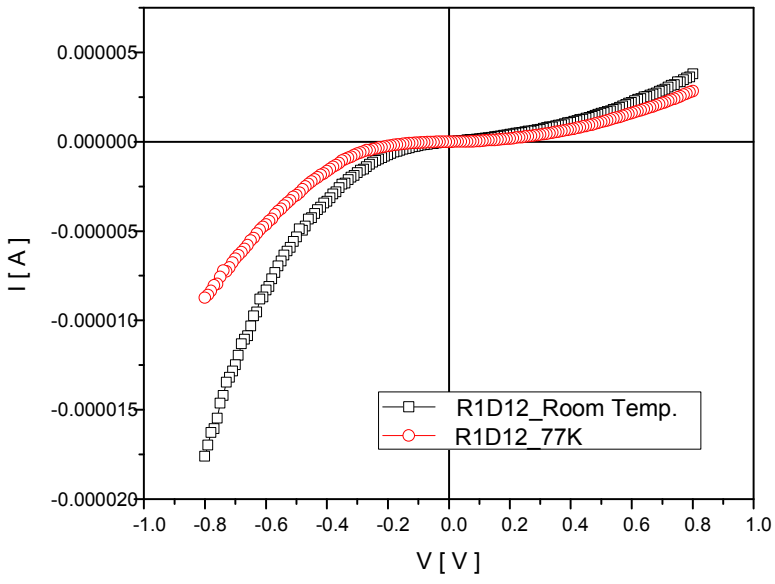

Figure 6.9: DC I-V measurement data for a 0.54 μ4m2 tunneling junction device at room temperature and 77K using liquid nitrogen.

the reverse current shows much higher current reduction compared to the forward current. This different temperature dependency may be induced by the geometric field enhancement. Also, the device shows significant improvement of the sensitivity at low temperature, as shown in Figure 6.10. In this case, the sensitivity at 77 K is almost twice of the one at room temperature. This kind sensitivity improvement at low temperature is a very common characteristics in tunneling diodes [9].

6.3.3 RF Rectification Test

An interesting experiment has been performed using the asymmetric tunneling diodes. Using the same test setup for DC IV measurements, incident wave detection tests were executed. For this test, a commercial walkie-talkie, which operates at

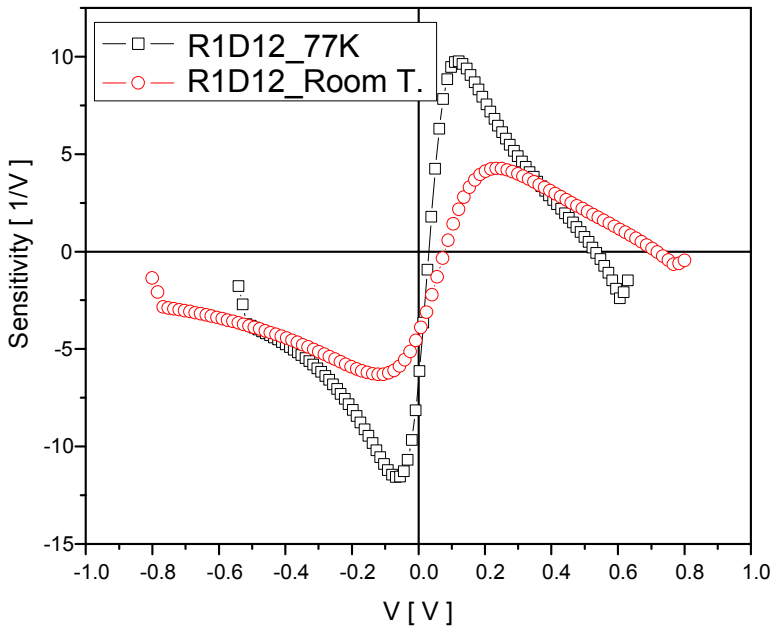

Figure 6.10: Sensitivities at room temperature and 77K of the same device in Figure 5.7

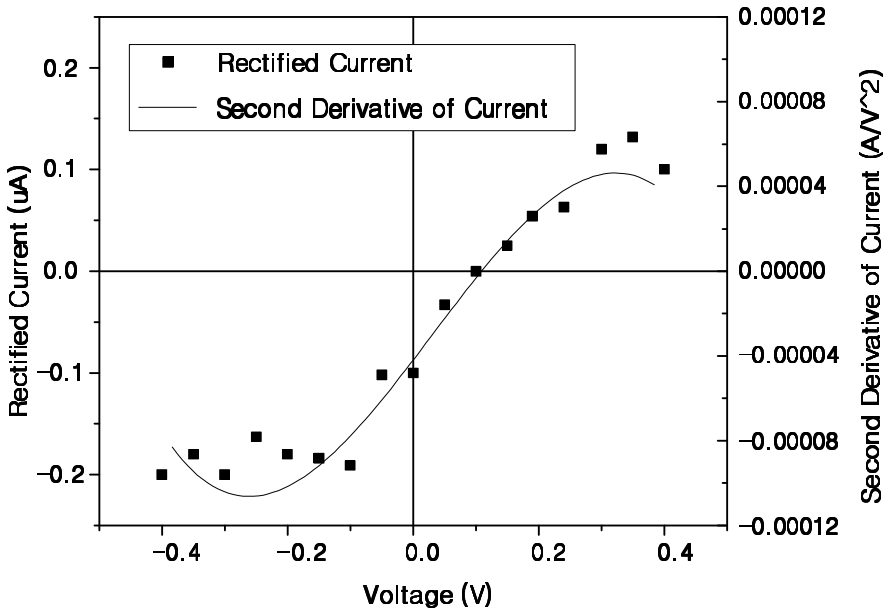

Figure 6.11: RF rectification test results of a poly-Si ATD at 900 MHz with 30 dBm power. The second derivative of diode current is plotted with a solid line, and the rectified DC currents are plotted with square-dots. The maximum sensitivity of this ATD is -7 V_{-1}.

900 MHz, is used as an RF wave transmitter. A tunneling device was placed on a probe station and connected to parameter analyzer for biasing. The RF response was measured using needle-probes contacting the output pads of the tunnel device. These probe tips work as a "rabbit ear" antenna, coupling the RF waves from the transmission antenna to the ATD. During the tests, the walkie-talkie is placed and fixed near the device measurement set-up, 30 cm distance away from a tunneling device.

Figure 6.11 shows the rectified DC current at each bias point and the second derivative of a ATD I-V curve. As predicted by Eq.(2.3), the rectified DC currents follow the current curvature (I''). The diode gives higher (by roughly a factor of 2)

rectified DC currents at the reverse bias side of the current-voltage plot due to the higher I'' at the reverse bias region as an effect of the GFE technique.

6.4 FAMIM Tunneling Diode

This section includes the details of DC and RF testing of FAMIM diodes, and it includes a performance comparison between FAMIM diodes and conventional MIM diodes. The specific benefits of the GFE technique, mentioned in chapter 3, are explored based on the body of data presented and its interpretation.

6.4.1 DC Test Results

Asymmetric Tunneling Current: Using the DC IV test set-up, asymmetric tunneling current characteristics of completed diodes are obtained at room temperature. For Type-C diodes, the current asymmetry shows a random distribution at ±0.025 V DC bias conditions. There are two factors creating two random response: the unintended sharp edge of the 1st electrode and the barrier lowering effect at the 2nd electrode in Type-C diodes. However, Type-A and Type-B diodes show clear tunneling current asymmetry under all bias conditions. We find that 75 % and 96 % of Type-A and Type-B diodes (respectively) show higher reverse tunneling current compared to forward tunneling currents at ±0.025 V. The two electrodes of Type-A and Type-B diodes are implemented with Ni, and the asymmetric polarity is opposite to the polarity induced by the barrier lowering effect described in chapter 3. Therefore, this asymmetric tunneling current must be a result of the GFE effect. This asymmetry is the main characteristic of FAMIM diodes (Type-A and Type-B) compared to conventional MIM tunneling diodes (Type-C)

The measured DC tunneling currents for a Type-B FAMIM diode and a Type-

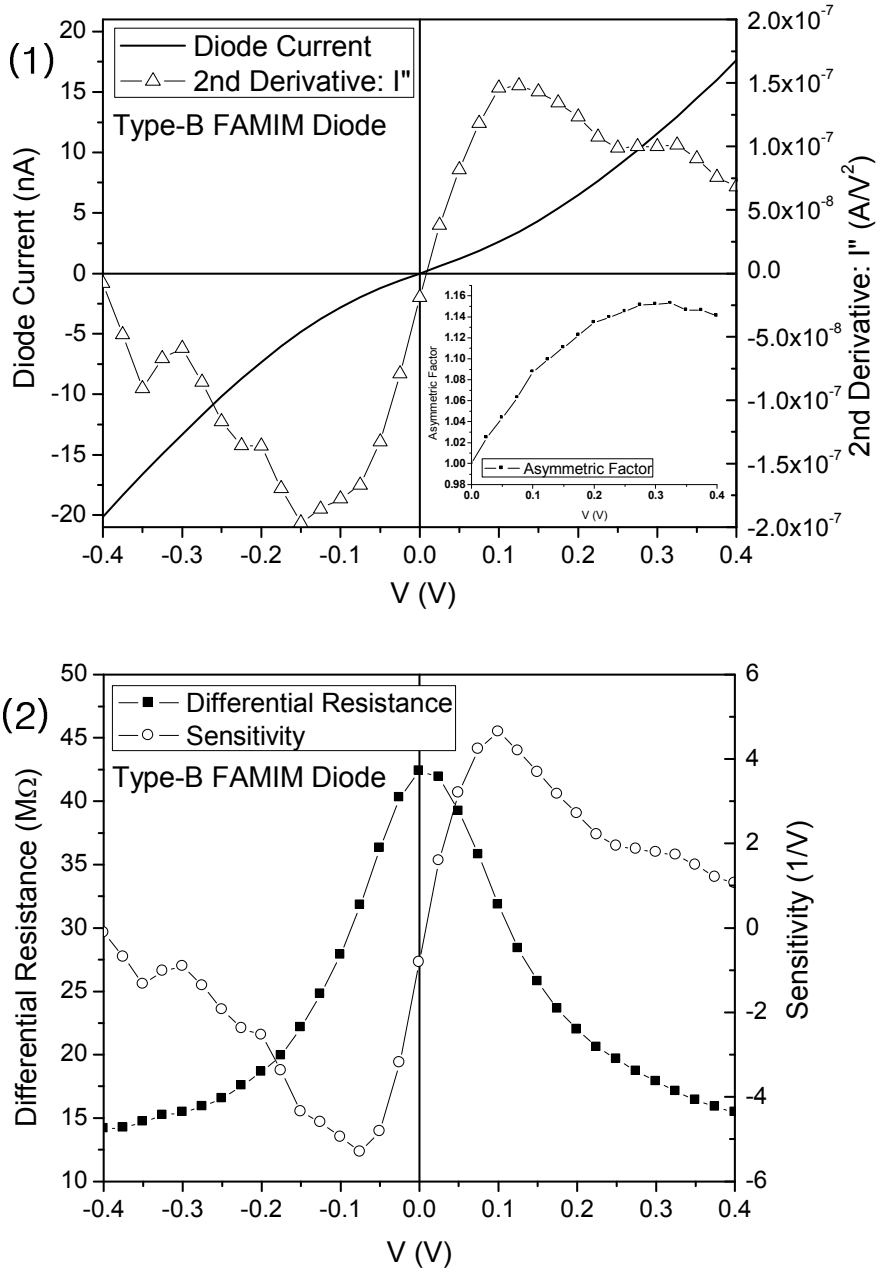

Figure 6.12: DC current-voltage measurement data for a Type-B FAMIM diode. (1) The solid line is the measured tunneling current under DC bias sweep, and the triangle line is the extracted current curvature of a Type-B FAMIM diode. (2) The filled square line is the extracted differential resistance of the diode in (1), and the circle line is the extracted sensitivity of the diode in (1).

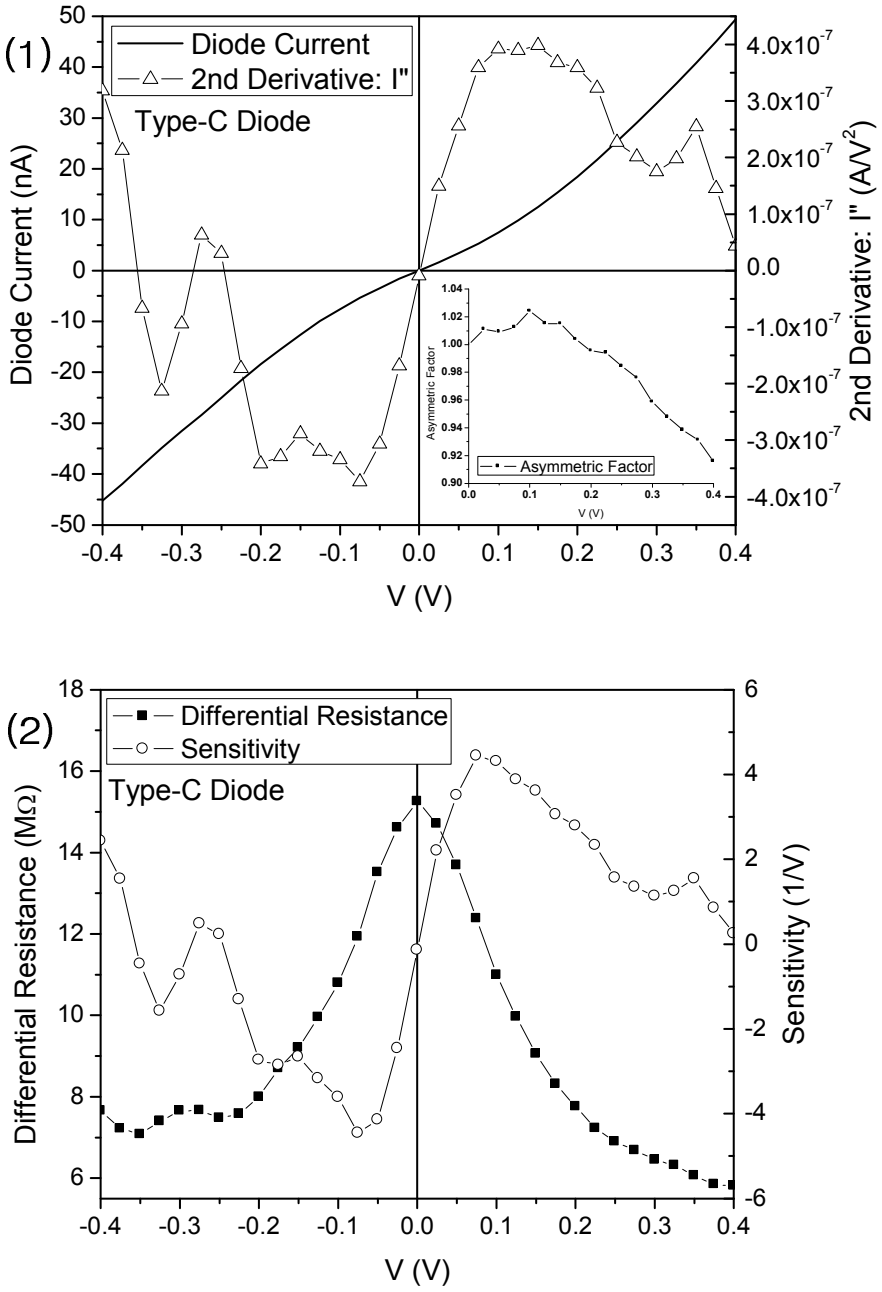

Figure 6.13: DC current-voltage measurement data for a Type-C conventional tunneling diode. (1) The solid line is the measured tunneling current under DC bias sweep, and the triangle line is the extracted current curvature of a Type-C conventional diode. (2) The filled square line is the extracted differential resistance of the diode in (1), and the circle line is the extracted sensitivity of the diode in (1).

Diode Type		Type-B FAMIM	Type-C Conventional
Junction Area		0.018 μm^2	0.029 μm^2
Zero Bias	$1/I^{'}$	42.38 MΩ	15.25 MΩ
	S	-0.81 V^{-1}	-0.14 V^{-1}
	$I^{''}$	-1.91E-8 A/V^2	-9.08E-9 A/V^2
Forward Bias	Max. S	4.65 V^{-1} @ 0.10 V	4.44 V^{-1} @ 0.075 V
	Max. $I^{''}$	1.48E-7 A/V^2 @ 0.125 V	3.92E-7 A/V^2 @ 0.10 V
Reverse Bias	Max. S	-5.30 V^{-1} @ -0.075 V	-4.46 V^{-1} @ -0.075 V
	Max. $I^{''}$	-1.97E-7 A/V^2 @ -0.15 V	-3.74e-7 A/V^2 @ -0.075 V

Table 6.3: Performance summary of the two diodes shown in Figure 6.12 and 6.13.

C diode are plotted in Figure 6.12 and 6.13 respectively. The differential resistance ($1/I^{'}$), second derivative of tunneling current ($I^{''}$), and sensitivity (S) of each diodes are extracted from the measured DC currents and plotted in the figures. The specific characteristics of the two diodes are listed in Table 6.3. Commonly, a 5th order polynomial fit is used to extract $I^{'}$ and $I^{''}$ from measured DC tunneling currents of a MIM diode. There are issues relating to the validity of polynomial fitting described more fully in the next section. But here $I^{'}$ and $I^{''}$ are extracted from the measured currents directly without a polynomial fitting procedure because of the extraction accuracy issue. The extracted plots are somewhat noisy, but they do not suffer from numerical problems described below.

As shown in Figure 6.12(1), asymmetric tunneling current is obtained from the Type-B diode. This asymmetric current demonstrates the successful implementation

of the FAMIM diode process using the GFE technique. This asymmetric tunneling current is a unique achievement in MIM diodes with the same metal electrodes. Furthermore, tunneling current asymmetry can be achieved not only in geometrically asymmetric design, Type-A diodes, but also in geometrically the symmetric design, Type-B diodes. The inset figures in Figure 6.12(1) and Figure 6.13(1) show the asymmetry factors. The asymmetry factor of the FAMIM diode reaches 1.153 at the ±0.325 DC bias point. Seven diodes (15 %) of the Type-A and Type-B (total 48 diodes) groups show more than 10 % higher reverse current compared to forward current at ±0.3 V. On the other hand, the asymmetry factor of the Type-C group decreases almost monotonically in the low bias range. The reversed asymmetry of this diode can be explained by the barrier lowering at the second electrode side.

Curvature (I''), Sensitivity (S) and Small Signal Resistance ($1/I'$): The improvement of I'' and S is critical for good rectifying performance. This improvement is the ultimate goal of developing FAMIM diodes. To check I'' improvement, simple comparison between a FAMIM and a conventional MIM diode would be proper. Such comparison, however, is not easy because I'' depends on driving point courrent. Thus, carefully selected diodes, which have almost same current conductance, should be compared. Or the performance parameters can be compared at forward and reverse bias condition in a single diode. Table 6.3 shows that the maximum I'' and S values for each bias direction are almost same for the Type-C diodes. However, the Type-B FAMIM diode shows a significant improvement of maximum I'' and S in the reverse bias condition: 33 % and 14 % improvement compared to the forward bias results, respectively. As shown in Figure 6.12(2), the slope of the

differential resistance of the FAMIM diode at a reverse bias direction is steeper than the slope of the conventional diode in Figure 6.13(2). This rapid resistance change reflects the higher current non-linearity created by the DC lightning rod effect under reverse bias conditions. In contrast, the Type-C diode shows little difference in I'' and S when comparing forward and reverse bias result. and the tunneling resistance seems almost symmetric up to ± 0.2 V, shown in Figure 6.13(2).

Another improvement realized by the FAMIM structure is the reduced tunneling resistance in the reverse bias direction, as compared to the forward bias direction. As shown in Figure 6.12(2), the tunneling resistance in reverse bias is smaller than the forward bias resistance for the entire bias range. However, this resistance reduction is not clear in the conventional tunneling diode shown in Figure 6.13(2). For a specific example, the differential resistances at +0.1V and -0.1V of the FAMIM diode of Figure 6.12(2) are 31.83MΩ and 27.87MΩ, respectively. For the Type-C diode of Figure 6.13(2), the differential resistances at +0.1V and -0.1V are 10.99MΩ and 10.79MΩ, respectively. This reduced resistance in the FAMIM diode appears to have a negative effect on the diode sensitivity. Therefore, the sensitivity improvement (14 %) is much smaller than the improvement due to increased curvature. But, this reduced tunneling resistance is another advantage of FAMIM diode because it will allow more signal energy to couple into the tunnel junction due to impedance matching. This is demonstrated in the RF rectifying test section.

Zero Bias Performance: The rectifying performance of a MIM diode can be maximized by operating the diode at a bias condition that maximize I'' or S. However, the rectified DC current or voltage are usually small even at the maximum

Diode #	Diode Type	Junction Area (um^2)	DC Current (A)	R_0 (MΩ)	I"$_0$ (AV2)	S_0 (1/V)	Rectified DC current (A)
1	B	0.037	-7.0E-12	13.6	-8.27E-8	-1.12	-4.7E-11
2	B	0.018	-2.03E-12	42.4	-1.91E-8	-0.81	-1.65E-11
3	C	0.029	-4.21E-12	15.3	-0.91E-8	-0.14	-2E-12
4	C	0.012	2.05E-12	23.4	1.32E-8	0.31	1.15E-11
5	A	0.035	-2.4E-13	282	-2.74E-9	-0.77	-2.15E-12
6	B	0.038	-3.9E-13	221	-3.28E-9	-0.73	-2.3E-12
7	B	0.024	-2.1E-13	342	-1.39E-9	-0.48	-1.35E-12
8	C	0.011	-5.7E-13	138	-1.34E-9	-0.18	-2.6E-12
9	C	0.030	-2.1E-13	181	-0.82E-9	-0.15	-8E-13
10	C	0.017	-1.6E-13	495	-0.10E-9	-0.05	-1.6E-13

Table 6.4: Diode characteristics at zero bias.

I$''$ or S at the bias point due to originally small I$''$. (Until now, the highest published I$''$ is close to 10^{-2} range for thin film MIM diodes [10].) In energy harvesting, this situation leads to higher power consumption compared to the harvested power. Zero bias is a "sweet spot" for energy harvesting applications, as there is no power dissipated in the absence of signal. The I$''$ improvement at zero bias is explored using experimental data.

The operating parameters of ten diodes at zero bias are listed in Table 6.4. In order to achieve meaningful comparisons, diodes which have similar tunneling resistances at zero bias must be compared to minimize the current level dependency

of I''. First, the current level dependency of I'' is found in the Table. For the same type of diodes, a diode of smaller resistance or higher current has higher curvature at zero bias. By comparing diode #1 with diode #3, (two diodes with nearly the same resistance and tunnel junction size), I'' and S of diode #1 are nine and eight times higher than diode #3, respectively. For high resistance diodes, (from diode #5 to diode #10, for example) a clear improvement is found again: I'' and S of diode #6 is four and five times higher than diode #9. A similar result is observed by comparing diode #2 with diode #4 and diode #7 with diode #9 based on current level.

Among the diodes tested, the FAMIM diode #1 has the highest zero bias sensitivity (-1.12 1/V) and current curvature (-4.7E-8 A/V^2). This sensitivity result is comparable with the MIM sensitivity value reported by Bean, et al.[29], implemented using a dissimilar electrodes method with a Al-Al2O3-Pt structure. The rectified DC current result summarized in Table 6.4 is discussed in the next section. Based on this comparison between different types of diodes, FAMIM diodes show better performance for zero bias operation as evidenced by increased I'' and S.

6.4.2 RF Rectification Test

Although infrared frequency operation is the major application area of MIM tunneling diodes, the inherent rectification characteristics of MIM diodes can be checked at RF frequency. It has been shown that the RF response of a MIM diode can be sustained in infrared frequencies [7]. In this section a discussion of the

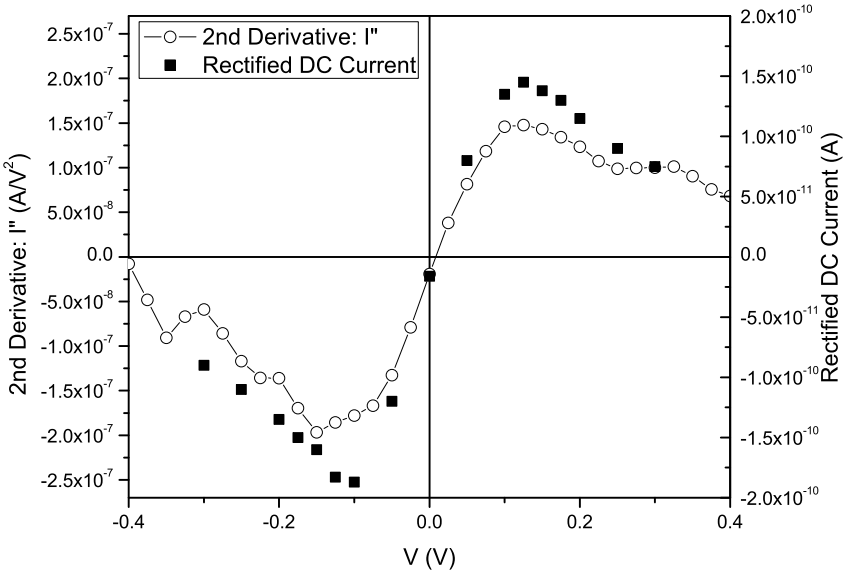

Figure 6.14: RF rectifying result. RF rectifying is performed using transmission antenna and a RF source with 12 dBm RF power and the FAMIM diode shown in Figure 6.12.

RF performance of the FAMIM diodes and conventional MIM tunneling diodes is provided. RF rectifying result will clearly show how the performance improvement at DC affects to rectifying operation, and the AC lightning rod effect is verified based on experiment data. Additionally, the extraction accuracy issue in MIM diode parameter extraction is covered.

RF rectification tests have been performed at 6.4 GHz with 12 dBm RF power (RF output power from a RF source) using the RF test set-up introduced in chapter 6.1. The rectified DC current is monitored at different DC bias points. Figure 6.14 shows rectified DC currents result (filled squares) at different bias points together with I'' of the FAMIM diode in Figure 6.12. As indicated in Eq. (2.3), the rectified

DC current is proportional to the second derivative of the DC tunneling current. This characteristic is clearly shown in Figure 6.14. The rectified DC currents follow I'' over the entire bias range. The bias points of each peak rectified current are matched to the maximum points of I'' in both the forward and reverse bias direction. The rectified current at zero bias has the same polarity as I''.

In Table 6.4 the rectified current of diode #1 is much higher than that of diode #3. The difference is almost 24 times. Compared to the I'' improvement, much higher rectified DC current is obtained. This can be explained by the lower tunneling resistance of diode #1. Due to the lower resistance of diode #1, the coupled signal power from the antenna into the tunnel junction is higher than the diode #3. This rectifying results show the superior performance of the FAMIM diode at zero bias.

Parameter Extraction Accuracy Issue: The core parameters, such as I'', S, and $1/I'$, are extracted from measured DC current using a fifth polynomial fit. The fitting procedure gives clean and smooth results for the extracted parameters, as verified elsewhere in the literature [34, 35, 13, 29, 67, 68].

In Figure 6.15, the measured DC I-V data of a FAMIM diode is plotted with circles. In addition, a fifth and a seventh order polynomial fit are plotted with squares and a solid line, respectively. The two fit curves seem to be well matched to the measured data. The seventh order fit is added for comparison with the fifth order fit. For each polynomial fit, the fitting residuals are distributed in $\pm 1 \times 10^{-8}$ and $\pm 3 \times 10^{-9}$, respectively. In Fig. 6.16, three current curvatures are overlapped with the rectified DC current result. Really clean and smooth current curvature

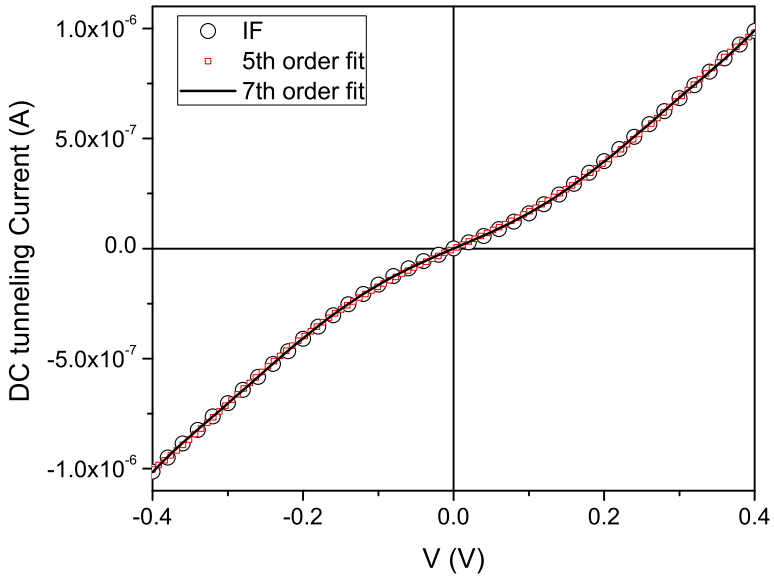

Figure 6.15: Measured DC tunneling current and polynomial fits. Measured current, a 5th, and a 7th order polynomial fit are plotted with circles, squares, and a solid line, respectively.

curves are extracted from the fifth and the seventh order polynomial fits compared to the current curvature using the raw data, directly extracted from the measured raw data without any fitting procedure. First, the maximum points of the rectified DC currents are matched to the peak points of the curvature using the raw data at ± 0.1 V. Second, the rectified DC currents show a local minimum at each bias direction. The curvature from raw data shows the same behavior at higher bias levels.

There are serious deviations between the rectified DC current and what would be expected for the two current curvatures obtained from the polynomial fits. The peak points of the curvature using fifth order fit are not matched to the rectified DC

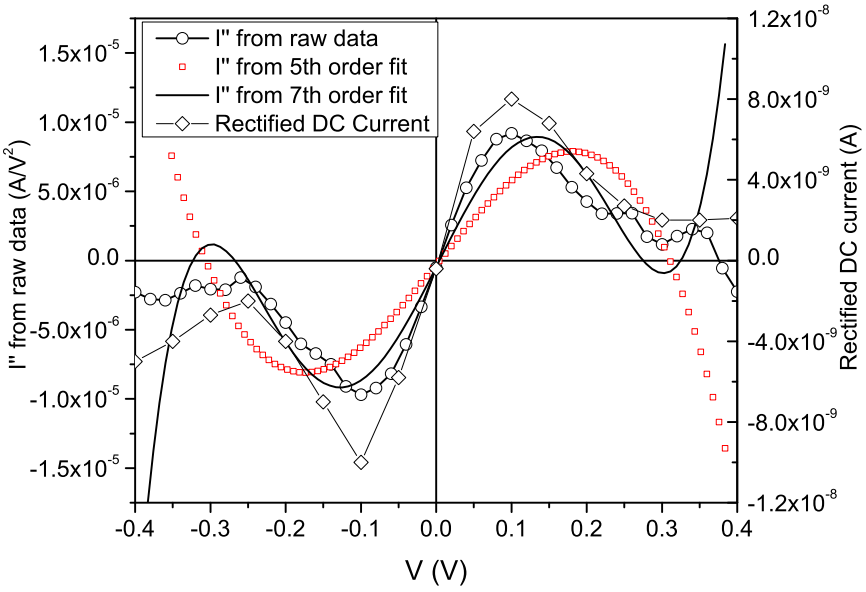

Figure 6.16: Current curvature and rectified DC current. The circle line is for the I'' extracted using raw data, the squares are for the I'' extracted by the 5th order polynomial fit shown in Figure 6.15, the solid line is the I'' extracted by the 7th order polynomial fit shown in Figure 6.15, and the diamond line is rectified DC current data of the FAMIM diode in Figure 6.15.

currents, and the high bias behavior is much different from the rectified DC current. The seventh order fit shows better result compared to the fifth order case: the peak points of curvature are closer to the peaks of rectified DC current and the high bias trend is more similar to the rectified DC current. But, the extraction accuracy between the rectified DC current and extracted curvature using the seventh order fit is still in disagreement with the raw data. The same accuracy errors are found in $1/I''$ and S. Based on this observation, it appears that the polynomial fitting procedures are not truly indicative of the actual operating parameter trends. Thus, it appears that high density data curves must be used for accurate assessment of

MIM diode performance. (Note that the rectified current behavior at high bias condition may be from thermally generated current [9].)

Reduced Resistance Effect: Using a rudimentary equivalent circuit model of an antenna coupled MIM diode [69], the coupled power (P_c) in the tunnel junction or dissipated power by the tunnel junction can be expressed as

$$P_c = \frac{1}{2} \cdot \frac{1}{R_D} \cdot |v_{ac}|^2 \tag{6.1}$$

where the R_D is the tunnel junction resistance. Using Eq. (2.2) and Eq. (2.3) and replacing R_D with the differential resistance, Eq. (6.1) can be rewritten using the rectified DC current (I_{rect}),

$$P_c = 2 \cdot \frac{I_{rect}}{S} \tag{6.2}$$

Using Eq. (6.2), the coupled power of the FAMIM diode used in Figure 6.16 is calculated and plotted in Figure 6.17. The coupled power calculated by using the fifth order polynomial fit data is decreased as the bias voltage goes high at both forward and reverse bias direction, squares in Figure 6.17. For the seventh order case, the coupled power seems flatter over the various bias conditions (circles in Figure 6.17). However, the coupled power using the raw data shows a continuous increase as the bias is increasing from zero to higher bias for each bias direction. This behavior is reasonable because the differential resistance of the diode decreases as the bias voltage increases. This resistance reduction helps to satisfy impedance matching condition. Therefore, more power can be coupled into the tunnel junction

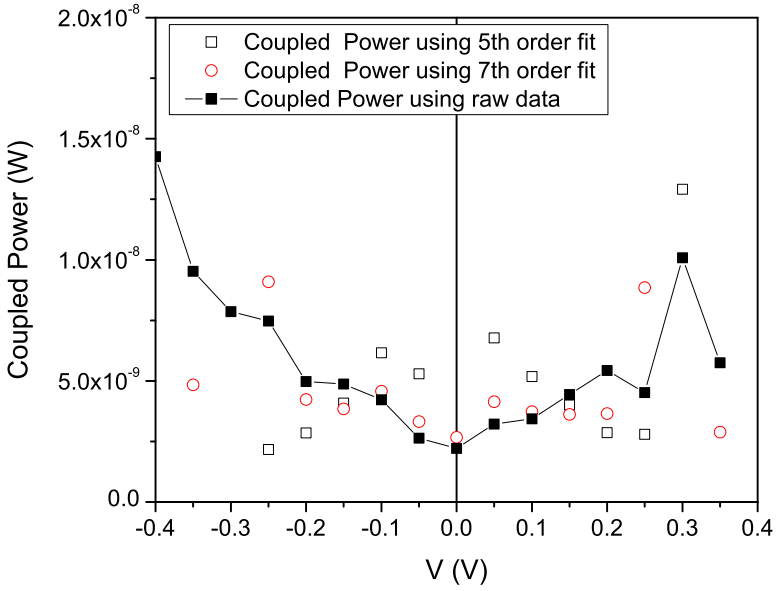

Figure 6.17: Coupled power in a FAMIM diode. Empty squares are for coupled power calculated using the S from the 5th order fit in Figure 6.15. Circles are for coupled power calculated using the S from the 7th order fit in Figure 6.16. Filled squares are for coupled power calculated using raw data.

at lower resistance. (Note: the basic assumption is that the tunneling resistance is much larger than the radiation resistance of the rabbit ear antenna.) Once again, the coupled power result show the inaccuracy of the polynomial fitting procedure again.

To provide sound data supporting improvement of coupled power by reduced resistance in MIM didoes, RF rectifying tests were performed for every diode in each lot prepared (25 Type-A diodes, 23 Type-B diodes, and 16 Type-C diodes) at ±50 mV and at the zero DC bias condition. Figure 6.18 shows the coupled power, extracted by using eq. (6.2), under +50 mV DC bias for thirteen Type-B diodes

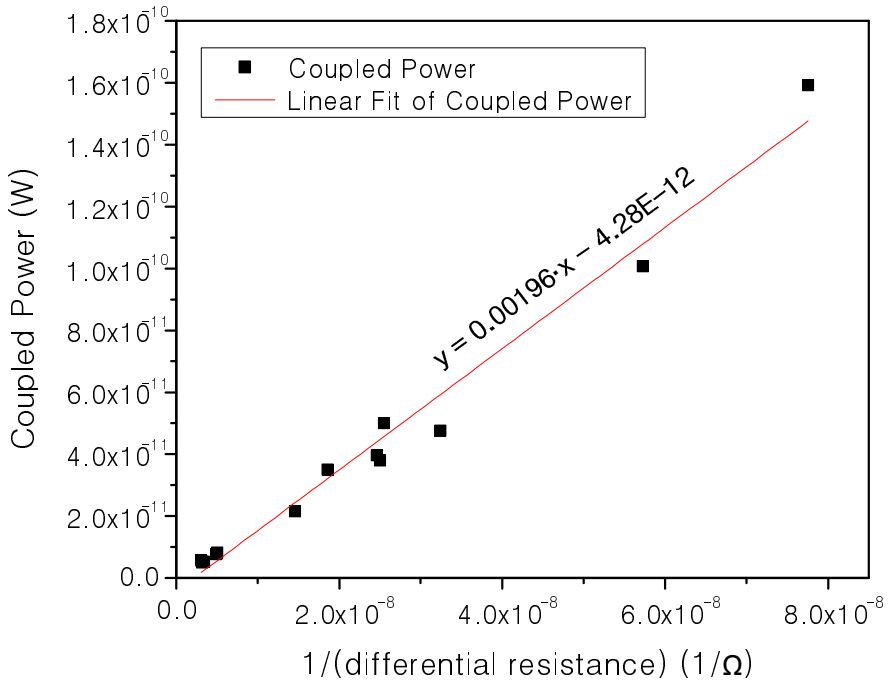

Figure 6.18: Coupled power at multiple Type-B FAMIM diodes. Each square indicates the coupled power for a diode at +50 mV DC bias condition. Total thirteen Type-B diodes of a 40 second oxidized sample are used in this figure. Solid line is for a linear fit of coupled power of thirteen diodes.

where a 40 second oxidation process is used. Similar to the single diode case shown in Figure 6.17, as more power is coupled into a tunneling diode, the diode appears to have a smaller tunneling resistance. This trend is common in other tests for different types of diodes at -50 mV and at zero bias.

As expressed in Eq. (6.2), $|v_{ac}|^2/\ 2$ becomes the slope in the P_c vs. $1/R_D$ plot. Using this relationship, the magnitude of the coupled ac voltage signal is extracted using a linear fit according to each sample, diode type, and bias condition. Each fit result and the calculated magnitude of the AC voltage signal are listed in Table 6.5. The slope of Type-A and Type-B diodes are higher than Type-C diodes at

Oxidation Time [sec]	Diode Type	@ +50 mV		@ -50 mV	
		Slope [V^2]	$\|v_{ac}\|$ [mV]	Slope [V^2]	$\|v_{ac}\|$ [mV]
20	A	0.00160	56.57	0.00169	58.14
	B	0.00163	57.10	0.00159	56.39
	C	0.00147	54.22	0.00142	53.29
40	A	0.00172	58.65	0.00167	57.79
	B	0.00196	62.61	0.00171	58.48
	C	0.00163	57.10	0.00165	57.45

Table 6.5: Linear fit results of coupled power.

both ±50 mV DC bias condition for both samples. This result means that more signal is coupled into the tunnel junction of FAMIM diodes compared to Type-C general MIM diodes. This is the result of AC lightning rod effect induced by the GFE technique. A higher magnitude of AC voltage in the 40 second oxidation sample is observed compared to the 20 second oxidation sample due to the higher tunneling resistance of the 40 second oxidation sample. This can be understood by considering a voltage divider configuration of an antenna resistance and a diode resistance. (Although higher voltage signals can be transferred on diodes which have higher tunneling resistance, this does not guarantee higher power transfer efficiency.)

6.5 Discussion

DC I-V measurements demonstrate successful fabrication of the fully planar type tunneling diodes. For these diodes, the highest sensitivity reached is 31 V^{-1}, and this is the highest sensitivity achieved in any thin film tunneling diodes appearing in open literature.

The performance of ATDs has been improved in many aspects compared to the planar type tunneling diodes: tunneling current level, zero-bias resistance, sensitivity, and reduced process complexity. The most impressive result is the strongly asymmetric tunneling current created by a pointed electrode implementing the GFE technique. The current asymmetry is verified through comparison with crossbar tunneling diodes. This ATD is the first thin film tunneling diode in which an asymmetric tunneling characteristic is achieved by exploiting geometric field enhancement rather than work function difference effects. Through DC I-V measurement at 77 K, the tunneling current is demonstrated. For the best performance ATD, the highest sensitivity is reached to 22 V^{-1}, and the 350 % of nonlinearity improvement is obtained at reverse bias direction as a result of the GFE technique. RF rectification tests show the proper rectifying operation of ATD diodes and support the effect of the GFE technique.

The FAMIM diodes are developed by applying the GFE technique to a metal electrode instead of a poly-Si electrode. This increases tunneling current level by reducing band edge offset. Although the current asymmetry of FAMIM diodes is weaker than the asymmetry of poly-Si ATDs, a current asymmetry is maintained in

FAMIM diodes. Similar to ATDs, the origin of such current asymmetry is verified by comparing with conventional MIM tunneling diodes.

To summarizing, FAMIM diodes show superior characteristics inherent in GFE: asymmetric tunneling current, higher absolute tunneling current capability at a given bias, lower tunneling resistance, higher current curvature, enhanced AC signal coupling ability, and improved zero bias performance. Even with a weaker current asymmetry of FAMIM diodes(compared to ATDs), the improvement of S and I'' is as high as 33 % and 14 %, respectively, and such result clearly show the effectiveness of the GFE technique.

RF rectification tests performed using FAMIM diodes show the proper rectifying operation of the diodes and make it clear the relationship between the performance improvements at DC and RF rectification results. Furthermore, the AC lightning effect is demonstrated, the power transfer issue related on a impedance matching is studied, and parameter extraction issue is discussed.

Infrared wave rectification tests were performed with ATDs and FAMIM diodes at 9.6 μm wavelength. However, rectification result was not obtained. It may be due to the higher RC time constants of the prepared diodes. So further research is required to achieve a tunneling diode with a smaller RC time constant for infrared rectification tests.

Chapter 7

Conclusion

7.1 Summary

This research is focused on developing novel tunneling diodes for infrared wave rectifier development. Although previous research demonstrated that MIM diodes can work properly as rectifiers for infrared waves, the energy conversion efficiency from incident optical power to electrical power is usually very low because of poor rectifying performance of MIM tunneling diodes. The insufficient performance could be a serious problem (especially for infrared wave energy harvesting application). To improve the limited performance of tunneling diodes, two main ideas are proposed: using the surface plasmon resonances and using the GFE technique. Based on the two ideas, three different tunneling diodes have been developed and studied in this research.

First, a fully planar type tunneling diode process is developed and tested using polys-Si electrodes. The main goal is implementing a perfect planar type device to use surface plasmon resonances. The idea is captured from optical antenna concepts and applied for this tunneling diode fabrication. In the process development, the most critical issue is implementing a planar tunneling structure, and it is solved by using boiling water oxidation process. The process reproducibility and controllability of the boiling water oxidation technique is tested and demonstrated successfully.

Through DC I-V measurement tests, nonlinear tunneling currents are achieved in perfect planar type tunneling diodes.

The asymmetric tunneling diode (ATD) is developed for further improvement of the planar type tunneling diodes and implemented using the GFE technique. In ATDs, the GFE technique is achieved by a pointed poly-Si electrode, and the boiling water oxidation process is used to form a thin SiO_2 tunneling barrier on a the electrode. As a direct result of the GFE technique, very strong asymmetric tunneling currents are obtained through ATDs. This asymmetric tunneling currents are verified by comparing with crossbar tunneling didoes. Through DC I-V tests at room temperature and 77 K and RF rectification tests, the various diode's properties are characterized. Performance improvements, such as increased tunneling current density, nonlinearity, and sensitivity, are achieved in ATDs as the derivative effects of the GFE technique.

To increase tunneling current level, the GFE technique is applied to such a metal electrode instead of a poly-Si electrode that FAMIM diodes are developed. As ATDs, asymmetric tunneling currents are obtained in both structurally asymmetric and symmetric FAMIM diodes. Although the degree of current asymmetry is lower than ATDs due to a relatively blunt metal tip, performance improvements in sensitivity, nonlinearity, and current level are verified through DC I-V tests. The RF rectification test results show how the improvement at DC can affect the rectifying operation of FAMIM diodes. Using multiple diodes, it is demonstrated that the reduced tunneling resistance improves the power coupling between the antenna and the integrated tunnel junction and that the AC voltage signal is enhanced by AC

lightning rod effect. The accuracy issue of polynomial fitting procedures is covered. It is concluded that high-density data plots must be used for proper analysis of device performance, rather than curve fitting.

The various benefits of the GFE technique are explored and verified using FAMIM diodes and conventional MIM tunneling diodes. Specifically, asymmetric tunneling current characteristic, tunneling resistance reduction, nonlinearity improvement, injected signal enhancement, and zero bias performance improvement are demonstrated based on experimental data.

7.2 Achievements

As introduced in the beginning of this dissertation, most performance parameters are limited by the properties of the materials that are used to fabricate thin film tunneling diodes. Only one technique, a dissimilar electrode method, has been developed and made available to improve the limited rectifying performance of thin film tunneling diodes until now. Therefore, the most critical contribution of this research is the development of the GFE technique and its demonstration that enhances the performance and breaks the material limitations of thin film tunneling diodes. Other meaningful achievements are accomplished through this novel tunneling diode development. These include:

- Demonstration of the success of two fundamental ideas to improve the rectifying performance of thin film tunneling diodes: using surface plasmon resonances and applying the GFE technique

- Developing a new fully planar type tunneling diode using poly-Si/SiO_2/poly-Si structure
- Developing a new ATD using poly-Si/SiO_2/Ti structure
- Developing a new FAMIM diode using Ni/NiO/Ni structure
- Utilizing boiling water oxidation process for implementing a tunneling barrier
- Demonstrating asymmetric tunneling current by using GFE technique not by using dissimilar electrodes
- Demonstrating performance improvements, such as increasing tunneling current, reducing tunneling resistance, and increasing nonlinearity, derived from applying the GFE technique
- Demonstrating performance improvements at zero bias operation of FAMIM diodes
- Proposing a prototype tunneling diode design including a surface plasmon grating platform

7.3 Future Work

The further works in this novel tunneling diode research need to be conducted in four main directions: optimizing diode fabrication process, testing higher frequency rectification up to infrared frequencies, executing an optical simulation to

optimize diode and antenna design, and devising a proper process and design for a diode array.

The most critical issue we face is lowering MIM tunneling resistance without increasing junction capacitance. Lower tunneling resistance leads to the higher I-V non-linearity (I''). Therefore, it is necessary to find a proper oxidation process which can make a really thin and uniform tunneling barrier. From this point of view, the boiling water oxidation process is a good candidate for achieving such a thin and uniform oxide barrier. Frenkel-Pool emission may be achieved through the boiling oxidation process with other solutions instead of pure water. This introduces mid gap defects in the tunnel insulator, lowering tunnel injection barriers, lowering diode tunneling resistance.

Increasing the sharpness of a metal electrode is also important to enhance tunneling current asymmetry. In this dissertation, all metal electrodes are prepared by using a metal lift-off process. The tip sharpness of such electrodes are not as sharp as poly-Si electrodes which is implemented by a RIE dry etching process. Metal dry etching processes, such as ion-milling and focused ion-milling process, may give a sharper metal electrode. Further current asymmetry can be achieved by using dissimilar electrodes method with the GFE technique.

Most fabricated diodes respond to RF waves up to 6.4 GHz. However, the diodes did not respond to a infrared wave of 9.6 μm wavelength, due to a large RC time constant of the didoes. Thus, it requires to check the correct pole location in a frequency domain. For this, a higher frequency sweeping test is required to provide a feedback to the diode design and fabrication.

Antenna geometry is also important to couple incident waves into a tunnel junction. In this research, the antenna geometry, especially for the antenna length, is designed by using a simple RF antenna based theory and emperical simulations using COMSOL. However, considering the target operating frequency range, infrared frequencies, more sophisticated approaches are necessary. That is, precise optical simulations can provide useful feedbacks for the antenna design. Especially, surface plasmon resonances are mentioned as one of main ideas to improve the rectification performances of tunneling diodes. Optical simulations can be used to optimize new tunneling diodes, integrated antenna, and surface plasmon grating platform.

Finally, we must consider establishing a diode array for a infrared energy harvesting panel. The proper and optimized diode array design and required fabrication process must be devised in future work.

Appendix A

Tunneling Diode Process Procedure

This appendix describes the details of each tunneling diode fabrication process

A.1 Perfect Planar Type Tunneling Diode

1. *Bare Si wafer cleaning*
   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Surface oxide etching: BOE(10:1) for 60 seconds
   - Wafer rinse: DI water washing → N_2 blowing

2. *Dry oxidation*
   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Wafer loading into oxidation furnace
   - Dry oxidation condition
     - Gas: O_2 2000 sccm
     - Furnace temperature: 1000 $^{\circ}C$
     - Oxidation rate: 9 Å/min
   - Total SiO_2 500 Å oxidation

3. *Si_3N_4 deposition using PECVD*
   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Wafer loading into PECVD chamber

- Si_3N_4 deposition receipt
  - Gas flow: 5 % SiH_4 + 95 % N_2 (400 sccm), NH_3 (20 sccm)
  - Chamber pressure: 1000 mTorr
  - RF condition: high frequency process (13.56 MHz, 20 W, for 13 seconds) → low frequency process (20 W, for 7 seconds)
  - Deposition temperature: 300 $°C$
  - Deposition rate: 145 Å/min
- Total Si_3N_4 800 Å deposition

4. *Poly-Si deposition*

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $°C$ hotplate for 60 seconds
- Wafer loading into LPCVD chamber
- Poly-Si deposition receipt
  - Gas: SiH_4 100 %
  - Deposition temperature: 850 $°C$
  - Deposition rate: 150 Å/min
- Total Si_3N_4 600 Å deposition

5. *Poly-Si Doing*

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $°C$ hotplate for 60 seconds
- Spin-on-Dopant(SOD) (dopant: Phosphorus) coating: 3000 rpm for 60 seconds
- Baking: 200 $°C$ hotplate for 20 minutes
- Wafer loading into RTA (RTA 410) chamber
- Phosphorus doing receipt
  - Gas: N_2 20 sccm
  - Process temperature: 1000 $°C$ for 35 seconds
  - Temperature rising time: 8 seconds
  - Temperature falling time: 12 seconds
- SOD removing: BOE(10:1) for 60 seconds
- Wafer rinse: DI water washing → N_2 blowing

6. *E-beam patterning*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - E-beam resist (HSQ) coating: 2000 rpm for 60 seconds
   - Baking: 150 $^{\circ}C$ hotplate for 15 minutes
   - Gold particle: Drop gold particles on the seample → 90 $^{\circ}C$ hotplate baking for 30 seconds
   - Wafer loading into e-beam chamber
   - E-beam writing condition
     - Acceleration voltage: 10 KV
     - Aperture size: 10 μm
     - Beam step size (X & Y): 2 nm
     - Working distance: 8 mm
     - Resulting beam current: 12 pA
     - Total electron dose: 160 $\mu C/cm^{-3}$
   - Pattern develop: CD-26 for 3 minutes

7. *Reactive ion etching (RIE)*

   - Sample baking: 150 $^{\circ}C$ hotplate for 5 minutes
   - Sample loading into RIE chamber
   - RIE etching condition
     - Gas: SF_6 40 sccm, O_2 13 sccm
     - RF power: 80 W
     - Chamber pressure: 80 mTorr
     - Poly-Si etching rate: 60 Å/sec
     - Total etching time: 15 seconds
   - Stripping HSQ: BOE (10:1) for 20 seconds

8. *Applying boiling water oxidation process*

   - Native surface oxide etching: BOE(10:1) for 20 seconds
   - Boiling water oxidation: boiling DI water using a hotplate
   - Oxidation in the boiling water for 1 minute
   - Sample dry using N_2 blowing

A.2 Asymmetric Tunneling Diode (ATD)

1. *Bare Si wafer cleaning*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Surface oxide etching: BOE(10:1) for 60 seconds
   - Wafer rinse: DI water washing → N_2 blowing

2. *Dry oxidation*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Wafer loading into oxidation furnace
   - Dry oxidation condition
     - Gas: O_2 2000 sccm
     - Furnace temperature: 1000 $^{\circ}C$
     - Oxidation rate: 9 Å/min
   - Total SiO_2 500 Å oxidation

3. *Si_3N_4 deposition using PECVD*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Wafer loading into PECVD chamber
   - Si_3N_4 deposition receipt
     - Gas flow: 5 % SiH_4 + 95 % N_2 (400 sccm), NH_3 (20 sccm)
     - Chamber pressure: 1000 mTorr
     - RF condition: high frequency process (13.56 MHz, 20 W, for 13 seconds) → low frequency process (20 W, for 7 seconds)
     - Deposition temperature: 300 $^{\circ}C$
     - Deposition rate: 145 Å/min
   - Total Si_3N_4 800 Å deposition

4. *Poly-Si deposition*

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $°C$ hotplate for 60 seconds
- Wafer loading into LPCVD chamber
- Poly-Si deposition receipt
  - Gas: SiH_4 100 %
  - Deposition temperature: 850 $°C$
  - Deposition rate: 150 Å/min
- Total Si_3N_4 600 Å deposition

5. *Poly-Si Doing* :

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $°C$ hotplate for 60 seconds
- Spin-on-Dopant(SOD) (dopant: Phosphorus) coating: 3000 rpm for 60 seconds
- Baking: 200 $°C$ hotplate for 20 minutes
- Wafer loading into RTA (RTA 410) chamber
- Phosphorus doing receipt
  - Gas: N_2 20 sccm
  - Process temperature: 1000 $°C$ for 35 seconds
  - Temperature rising time: 8 seconds
  - Temperature falling time: 12 seconds
- SOD removing: BOE(10:1) for 60 seconds
- Wafer rinse: DI water washing → N_2 blowing

6. *E-beam patterning*

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $°C$ hotplate for 60 seconds
- E-beam resist (HSQ) coating: 2000 rpm for 60 seconds
- Baking: 150 $°C$ hotplate for 15 minutes
- Gold particle: Drop gold particles on the seample → 90 $°C$ hotplate baking for 30 seconds
- Wafer loading into e-beam chamber

- E-beam writing condition
  - Acceleration voltage: 10 KV
  - Aperture size: 10 μm
  - Beam step size (X & Y): 2 nm
  - Working distance: 5 mm
  - Resulting beam current: 12 pA
  - Total electron dose: 160 $\mu C/cm^{-3}$
- Pattern develop: CD-26 for 3 minutes

7. *1st poly-Si electrode RIE etching*

- Sample baking: 150 $^{\circ}C$ hotplate for 5 minutes
- Sample loading into RIE chamber
- RIE etching condition
  - Gas: SF_6 40 sccm, O_2 13 sccm
  - RF power: 80 W
  - Chamber pressure: 80 mTorr
  - Poly-Si etching rate: 60 Å/sec
  - Total etching time: 15 seconds
- Stripping HSQ: BOE (10:1) for 20 seconds

8. *Surface oxidation using the boiling water oxidation process*

- Boiling water oxidation: boiling DI water using a hotplate
- Oxidation in the boiling water for 1 minute
- Sample dry using N_2 blowing

9. *Surface oxide (on a poly-Si electrode) etching*

- Wafer cleaning: Acetone $\rightarrow$ Methanol $\rightarrow$ N_2 blowing
- Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
- Photo resist (S1813) coating: 4000 rpm for 60 seconds
- Sample baking: 90 $^{\circ}C$ hotplate for 2 minutes
- Expose: 8 mW/cm^2 of 365 nm for 11 seconds
- Pattern develop: 352 for around 25 seconds

- Oxide etching: BOE (10:1) for 10 seconds
- Sample rinse and dry
- Sample cleaning: Acetone → Methanol → N_2 blowing

10. *2st electrode patterning: using a image reversal process*

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
- Photo resist (AZ5214) coating: 5000 rpm for 60 seconds
- Sample baking: 90 $^{\circ}C$ hotplate for 3 minutes
- Expose: 8 mW/cm^2 of 365 nm for 5 seconds
- Sample baking: 120 $^{\circ}C$ hotplate for 1 minute
- Sample cooling: for 3 minutes
- Flood expose: 8 mW/cm^2 of 365 nm for 30 seconds
- Pattern develop: 400K + DI water (1:3 ratio) for around 20 seconds

11. *2st electrode patterning: using e-beam writing*

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
- E-beam resist (PMMA 495A4) coating: 4000 rpm for 60 seconds
- Baking: 180 $^{\circ}C$ hotplate for 90 seconds
- Gold particle: Drop gold particles on the seample → 90 $^{\circ}C$ hotplate baking for 30 seconds
- Wafer loading into e-beam chamber
- E-beam writing condition
  - Acceleration voltage: 10 KV
  - Aperture size: 10 μm
  - Beam step size (X & Y): 2 nm
  - Working distance: 5 mm
  - Resulting beam current: 12 pA
  - Total electron dose: 160 μC/cm^{-3}
- Pattern develop: MIBK+IPA for 1 minute

12. *Ti/Au metal evaporation for 2nd electrode*

    - Sample loading into the chamber of e-beam evaporator
    - Metal evaporation: Ti 100 Å and Au 1500 Å
    - Metal lift-off using acetone
    - Wafer cleaning: Acetone → Methanol → N_2 blowing

A.3 Focused Asymmetric MIM (FAMIM) Tunneling Diode

1. *Bare Si wafer cleaning*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Surface oxide etching: BOE(10:1) for 60 seconds
   - Wafer rinse: DI water washing → N_2 blowing

2. *Dry oxidation*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Wafer loading into oxidation furnace
   - Dry oxidation condition
     - Gas: O_2 2000 sccm
     - Furnace temperature: 1000 $^{\circ}C$
     - Oxidation rate: 9 Å/min
   - Total SiO_2 500 Å oxidation

3. *Si_3N_4 deposition using PECVD*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Wafer loading into PECVD chamber
   - Si_3N_4 deposition receipt
     - Gas flow: 5 % SiH_4 + 95 % N_2 (400 sccm), NH_3 (20 sccm)
     - Chamber pressure: 1000 mTorr
     - RF condition: high frequency process (13.56 MHz, 20 W, for 13 seconds) → low frequency process (20 W, for 7 seconds)
     - Deposition temperature: 300 $^{\circ}C$
     - Deposition rate: 145 Å/min
   - Total Si_3N_4 800 Å deposition

4. *1st electrode patterning: using e-beam writing*

- Wafer cleaning: Acetone → Methanol → N_2 blowing
- Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
- E-beam resist (PMMA 495A4) coating: 4000 rpm for 60 seconds
- Baking: 180 $^{\circ}C$ hotplate for 90 seconds
- Gold particle: Drop gold particles on the seample → 90 $^{\circ}C$ hotplate baking for 30 seconds
- Wafer loading into e-beam chamber
- E-beam writing condition
  - Acceleration voltage: 10 KV
  - Aperture size: 10 μm
  - Beam step size (X & Y): 2 nm
  - Working distance: 5 mm
  - Resulting beam current: 12 pA
  - Total electron dose: 160 $\mu C/cm^{-3}$
- Pattern develop: MIBK+IPA for 1 minute

5. *Ni metal evaporation for the 1nd electrode*

- Sample loading into the chamber of e-beam evaporator
- Metal evaporation: Ni 700 Å
- Metal lift-off using acetone
- Wafer cleaning: Acetone → Methanol → N_2 blowing

6. *Oxygen plasma cleaning*

- Sample loading into the chamber of plasma cleaner
- Cleaning condition
  - Gas: O_2
  - Pressure: 0.6 Torr
  - RF power: 75 W
  - Cleaning time: 60 seconds
- Wafer cleaning: Acetone → Methanol → N_2 blowing

7. *Surface oxidation using oxygen plasma*

- Removing surface oxide: BOE (10:1) for 5 seconds
- Ni surface oxidation using RIE
  - Loading the sample into RIE
  - Gas: O_2 60 sccm
  - Chamber pressure: 150 mTorr
  - RF power: 50 W
- Wafer cleaning: Acetone → Methanol → N_2 blowing

8. *2st electrode patterning: using e-beam writing*

   - Wafer cleaning: Acetone → Methanol → N_2 blowing
   - Wafer baking: 90 $^{\circ}C$ hotplate for 60 seconds
   - Copolymer (MMA-MAA EL6) coating: 2500 rpm for 60 seconds
   - Baking: 180 $^{\circ}C$ hotplate for 4 minutes
   - E-beam resist (PMMA 495A4) coating: 2000 rpm for 60 seconds
   - Baking: 180 $^{\circ}C$ hotplate for 90 seconds
   - Gold particle: Drop gold particles on the seample → 90 $^{\circ}C$ hotplate baking for 30 seconds
   - Wafer loading into e-beam chamber
   - E-beam writing condition
     - Acceleration voltage: 10 KV
     - Aperture size: 10 μm
     - Beam step size (X & Y): 2 nm
     - Working distance: 5 mm
     - Resulting beam current: 12 pA
     - Total electron dose: 160 μC/cm^{-3}
   - Pattern develop: MIBK+IPA for 1 minute

9. *Ni metal evaporation for the 2nd electrode*

   - Sample loading into the chamber of e-beam evaporator
   - Metal evaporation: Ni 700 Å
   - Metal lift-off using acetone
   - Wafer cleaning: Acetone → Methanol → N_2 blowing

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