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2D Materials

PAPER

RECEIVED
15 December 2023

REVISED
14 February 2024

ACCEPTED FOR PUBLICATION
10 April 2024

PUBLISHED
18 April 2024

Emission current enhancement from quasi-freestanding epitaxial graphene microstructure electron emitters through surface layered silicon dioxide

Daniel Lewis[1,2,*], **Jason Swart**[3], **Michael Pedowitz**[1,2], **Jennifer DeMell**[4], **Brendan Jordan**[1,2], **Rachael L Myers-Ward**[5], **Daniel J Pennachio**[5], **Jenifer R Hajzus**[5] and **Kevin M Daniels**[1,2,*]

[1] Department of Electrical and Computer Engineering, University of Maryland, College Park, MD 20742, United States of America
[2] Institute for Research in Electronics and Applied Physics, University of Maryland, College Park, MD 20742, United States of America
[3] School of Mathematical and Statistical Sciences, Arizona State University, Tempe, AZ 85281, United States of America
[4] Laboratory for Physical Sciences, College Park, MD 20740, United States of America
[5] US Naval Research Laboratory, Washington, DC 23075, United States of America
[*] Authors to whom any correspondence should be addressed.

E-mail: dlewis17@umd.edu and danielkm@umd.edu

Keywords: quasi-freestanding, phonon assisted, electron emission, bilayer graphene, epitaxial graphene, microstructures, secondary electron emission

Supplementary material for this article is available online

Abstract

Enhanced electron emission from oxide-encapsulated quasi-freestanding bilayer epitaxial graphene devices is reported, including one emission current of 9.4 μA and successful emission even with oxide thicknesses of up to 1.25 μm. The low operating temperature (215 °C), and applied electric fields under which the devices operate indicate electron emission is due to phonon-assisted electron emission, wherein forward-scattering hot phonons impart the necessary energy for the electrons to escape the graphene as an emission current. A suite of device structures and behaviors are cataloged, and various emission behaviors are demonstrated through encapsulating oxide layers. Emission current enhancement due to electron multiplication in the oxide layers is observed across multiple devices and oxide thicknesses.

1. Introduction

Primary electron emission sources that function through thermionic, cold field, and Schottky emission, share basic design aspects. These devices are typically 3-dimensional structures aligned with their intended emission path and have their emission points operated in moderate to high vacuum [1]. The primary electrons, which are not a result of electron-electron collisions specifically, are released by these systems and are then free to traverse the intervening space to the target uninhibited, often while being directed by externally applied electric or magnetic fields along the way. While vacuum containment is not strictly a requirement to achieve primary electron emission, allowing the electrons to travel to the target through vacuum ensures that they can interact with the target surface at predictable incidence angles and expected initial energies, such as in vacuum-contained designs that are commonly used in microscopy and x-ray generation [2–4]. Additionally, these primary electron sources typically do not require an electron multiplication mechanism, such as photomultiplier tubes (PMTs) [5–7], custom dynode arrays [7, 8], Townsend discharge arrangements [9], or microchannel plates (MCPs) [10], as the primary source is engineered to provide all of the necessary emission current for the given application. Electron multiplication strategies are more commonly employed in detection systems, where otherwise undetectable events can be amplified into identifiable currents.

Electron emission sources synthesized from quasi-freestanding bilayer epitaxial graphene (QFEG) on semi-insulating silicon carbide have previously been demonstrated [11], which operate in a planar 2D configuration without the need for the emission structure to be aligned with the intended electron

travel path. These graphene electron emitters, synthesized using a simple, scalable fabrication process, were evaluated for their emission current based on their size and shape, ultimately demonstrating a measurable correlation between performance and shape and a strong correlation between emission current output and device temperature [11].

Here, we present graphene microstructure electron sources, where instead of directing emitted electrons through a vacuum, direct their emission currents immediately into and through oxide layers deposited on the device surface. Whereas our previously demonstrated electron sources in vacuum depends on primary electron emission, devices presented in this work demonstrate the addition of secondary electron emission (SEE) as observed from the transmitted emission current through the encapsulating oxide layers. An increase in the total measured current is observed, suggesting that electron multiplication is occurring through the encapsulating oxide layers. Emission currents as high as 9.4 μA are reported with encapsulating oxides, and clear patterns of device behavior are identified, allowing for a direct path for future efforts at optimization or increasing performance. All thicknesses of the e-beam deposited oxide layers survive repeated use of the devices, including heating cycles, without suffering dielectric breakdown, or observable physical change from their initial condition from the fabrication process.

2. Methods and materials

The QFEG used for the devices was formed on a cleaned wafer of 6H-SiC (0001) in an Aixtron/Epigress VP508 horizontal hot-wall reactor [12, 13]. The wafer was first etched by ramping the temperature to 1570 °C in 5 slm of high-purity H_2 at 200 mbar. Then the gas flow was switched to 100 mbar high-purity Ar and the temperature was held at 1580 °C for 20 min to synthesize monolayer graphene via silicon sublimation from the SiC lattice. The temperature was reduced to 1050 °C in the flow of Ar, then switched to 80 slm of high-purity H_2 at 900 mbar for 60 min. The H_2 passivates the silicon dangling bonds remaining on the SiC surface, releasing the $6\sqrt{3}$ buffer layer and forming the full structure of the QFEG.

A layer of LOR 5B and Shipley 1813 photoresist were applied to protect the graphene while the wafer was diced into 8 mm squares, as the use of a lift-off resist in conjunction with a photoresist has been shown to leave the graphene surface cleaner than when a photoresist is used alone [14]. The sample surface was sprayed clean of any particulate debris, and the photoresists were removed in acetone without sonication, followed by an IPA rinse, DI rinse, HF bath, DI rinse, and dry N_2.

Each device, and its integrated heating elements, was fabricated on its own dedicated 8 mm square sample, to simplify the fabrication process. Once the devices were fabricated, they were mounted in our standardized dedicated test housing: an Al_2O_3 ceramic dual in-line package (DIP) which consists of a depressed central cavity, pads for wire bonding the device contacts to the package pins, and a conductive ring around the top; a thin metal pad is evaporated onto the surface of the center of the cavity, away from the contact pins, to act as an electrode during device testing (figure 1). This arrangement allows for quick and seamless changes between devices under test, and eliminates any test variability that would result from the physical arrangement of the apparatus, as the dimensions of the DIPs are standardized for each package.

An example of a completed device package is illustrated in figure 1. A compound layer of LOR 5B and Shipley 1813 photoresist was applied to a cleaned QFEG sample, and a Heidelberg Maskless Aligner was used to pattern the device shape into the center of the sample. The resist was developed in an MF-319 bath for 1 min, then cleaned with DI and dry N_2. The sample was plasma etched with 100 sccm CF_4 at 25 mW for 30 s, then the resists are removed, and the sample is cleaned and dried, in the same manner as described above. The result is a SiC square with the only graphene present in the shape of the device and a 1 mm wide section of its contact pads. Simple shadow masks were used to pattern e-beam evaporated Al onto the device contact pads at the center edges, and along the sample's perpendicular edges to form the integrated resistive heaters (figure 1).

The aluminum of the contact pads makes direct contact with the plasma-etched SiC surface, providing ample adhesion to receive ball-and-wedge wire bonds with 50 μm Au wire, while overlapping the graphene of the device's contact pads to make low-input-resistance conductive contact to power the device. The resistive heating elements are entirely on the plasma-etched surface, again providing adhesion for the wire bonding, and also electrical isolation from the device. Wire bonding is done from the device to its dedicated test housing to enable remote activation of the heaters and the device.

A hole was drilled through the DIP that holds the device packages, to accommodate the K-type thermocouple probe of the Fluke T3000 FC module used for temperature measurements (figure 1). The metal layer deposited on the bottom of the DIP acted as the negative electrode of the applied accelerating field during device testing. The sample was secured to the test package with a thermally conductive, electrically insulating glue so that accurate temperature readings can be taken without risking electrical shorts from the temperature probe or the test housing. The device was positioned in such a way that the K-type

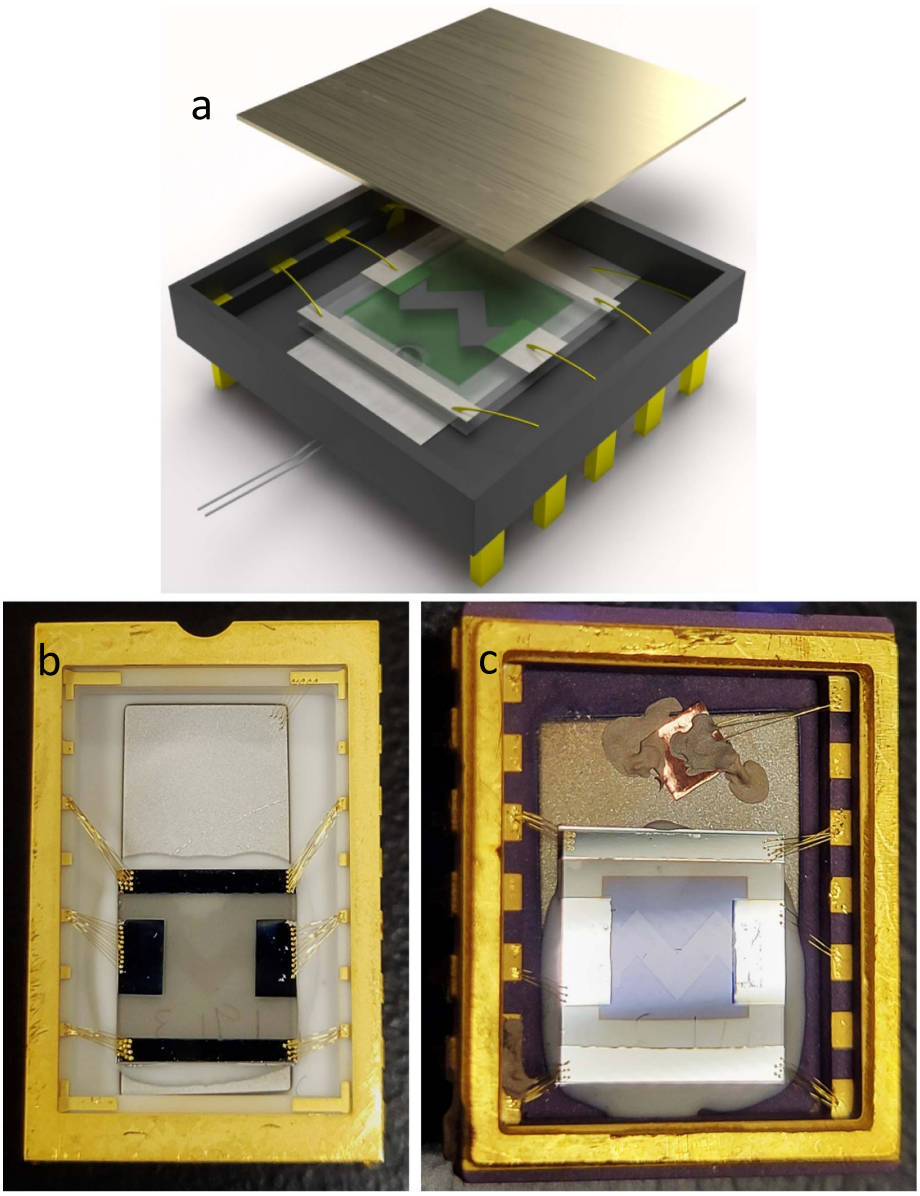

Figure 1. Devices and their packaging. (a) The conceptual layout of a completed package. The graphene device (grey) is on top of the SiC substrate (clear), with the contact pads and resistive heaters (silver) wired to the DIP pins (gold), and the oxide layer (green) is overlayed on the entire device area. A metal skin inside the DIP cavity (silver) forms the negative electrode of the enclosure, with the top collection plate (brass, cut-away) as the positive. A hole drilled through the DIP allows positioning of the K-type thermocouple probe (sphere) for direct temperature readings. (b) A completed device with no oxide layer. The graphene microstructure is faintly visible between the contact pads. A multitude of wire bonds reduces the thermal and current loads on each individual wire bond, to avoid degradation over multiple use cycles. (c) A completed device with 500 nm of oxide. Refraction at an oblique viewing angle reveals the graphene structure. Internal stress from the oxide layer partially delaminated one metal-graphene contact pad, but did not alter device performance. The wire bonds to the metal-coated-ceramic of this DIP were reinforced to prevent shorting.

thermocouple probe could make direct, electrically isolated contact with the sample, but the graphene device itself was situated entirely over the metal of the negative electrode, so the device is immersed in the applied electric field without gaps.

The package was plugged into to a purpose-built testing structure which both allowed the control wires to be connected to the device package via a feed-through in the vacuum chamber, and secured the thermocouple probe in position to ensure accurate measurements. The scroll pump in an Agilent Technologies IDP-15 Helium Leak Checker generated a low vacuum (∼7–9 mTorr) for device testing, while the integrated resistive heaters and a dedicated feedback action maintained the device package at 215 °C for the duration of all tests to ensure consistency.

Power was supplied to the device and the accelerating field, and the emission current was measured, by a combination of units depending on the test being conducted. For low voltage/high precision measurements we used a Keysight B2902a precision source/measure unit, and for high voltage/low

precision data we used a Keithley 2290-10 power supply. Power was supplied to the integrated heaters with a PRR48-22M Kepco power supply, and a dedicated external feedback mechanism, to maintain temperature. Measurements for all systems, including temperature readings, were at synchronized 1 s intervals for the duration of all tests.

Devices were subjected to a standardized battery of four tests, repeated at each increment of applied oxide thickness, in order to identify performance patterns and evaluate the foundations of device behavior. Devices of various sizes and morphologies were compared in order to establish an optimal design on which to base future permutations.

3. Results and discussion

3.1. Device fabrication and test conditions

Devices were made in six configurations, as illustrated in figure 2. The default device (figure 2(b)) is a right-angle zig-zag pattern with a 45° pitch (the best performing device configuration from the previous study [11]). The High Pitch device (figure 2(c)) is a more pronounced zig-zag pattern with a 60° pitch, and the extreme pitch device (figure 2(d)) is sharper still at 80°. The rectangular device (figure 2(e)) is a straight-line pattern 1 mm wide, and the large rectangular device (figure 2(f)) is the same but 2 mm wide. Finally, there is the nothing device (figure 2(a)), which is identical in all ways to the other constructed devices except it has no graphene, only bare SiC with aluminum depositions at the normal positions for the contact pads and heating elements. All devices have the same 4 mm space laterally between contacts, and their widths and geometries are individually tailored such that all devices present a uniform total of 4 mm^2 of graphene as their electron emission surface (except the Large Rectangular at 8 mm^2).

Each device was subjected to a standardized set of 4 tests, conducted over the same length of time for each device, all at a steady device temperature of 215 °C, and with a constant current through the device of only 10 mA to avoid self-joule heating. In Test 1, the applied accelerating electric field is ramped from 0 V cm^{-1} to 1 kV cm^{-1} in 50 V cm^{-1} increments, and in test 2 the accelerating field is taken from 1 kV cm^{-1} back down to 0 V cm^{-1}, with an intervening 0 V cm^{-1} between each incremental step of the sequence. Tests 3 and 4 are the same as tests 1 and 2, respectively, but with maximum applied fields of 10 kV cm^{-1} and 500 V cm^{-1} increments.

Between each set of tests, SiO_2 was e-beam evaporated (Angstrom NexDep) onto the operating surface of all devices, encapsulating the entire device in the oxide layer. The oxide was deposited in multiple stages to avoid any overheating that could have risked introducing additional unwanted strain in the deposited oxide layers. A thickness of 250 nm of oxide was deposited at 2 Å s^{-1}, then the e-beam evaporator was brought up to atmospheric pressure and the devices were removed and left to equilibrate in air at STP for 5 min. The devices were then loaded back into the deposition chamber, and another layer of 250 nm of oxide was deposited at 2 Å s^{-1}, and so on until the desired thickness was reached. The SiO_2 in the source crucible was replaced between each deposition, to limit non-oxide debris from infiltrating the oxide layers. After each deposition, a non-device sample included in the chamber was used to verify that layer's thickness with a Tencor Alpha-step 200 profilometer, as shown in the Supporting Information.

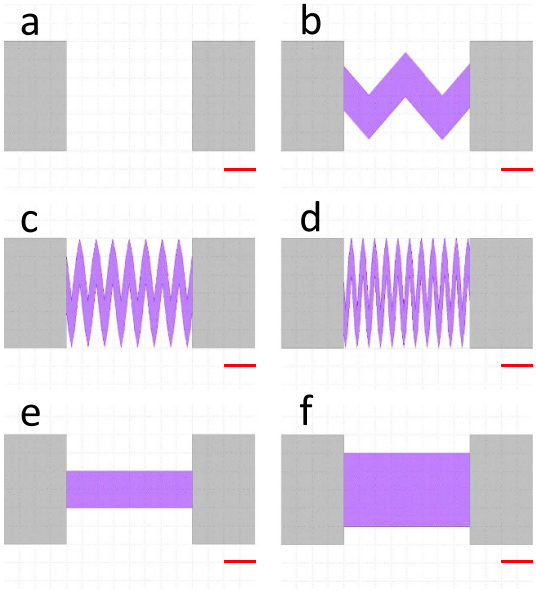

Figure 2. A schematic detailing the 6 fabricated device designs. (a) The nothing device, (b) the default, (c) high pitch, (d) extreme pitch, (e) rectangular, and (f) large rectangular. Purple represents exposed graphene, grey is aluminum. Scale bars (red) are 1 mm.

The first oxide layer's total thickness was 250 nm, and the second layer was twice as thick, totaling 500 nm of oxide. For the third stage of the oxide cap, it was decided to increase the total thickness by a larger margin, in order to look for significant deviations in device behavior. As such, the third layer of oxide added 750 nm more, bringing the total oxide covering the devices in the last round of tests to a final thickness of 1.25 μm. All depositions were conducted with every device simultaneously, to eliminate any variability that would be due to deposition techniques, and tests were repeated under matching conditions immediately following each oxide deposition.

The surface morphology of the oxide after deposition, both before and after device testing, is shown in figure 3. The authors credit the poor adhesion of materials to graphene for the buckled appearance of the oxide, but note that it appears otherwise intact and contiguous, and also that it shows no

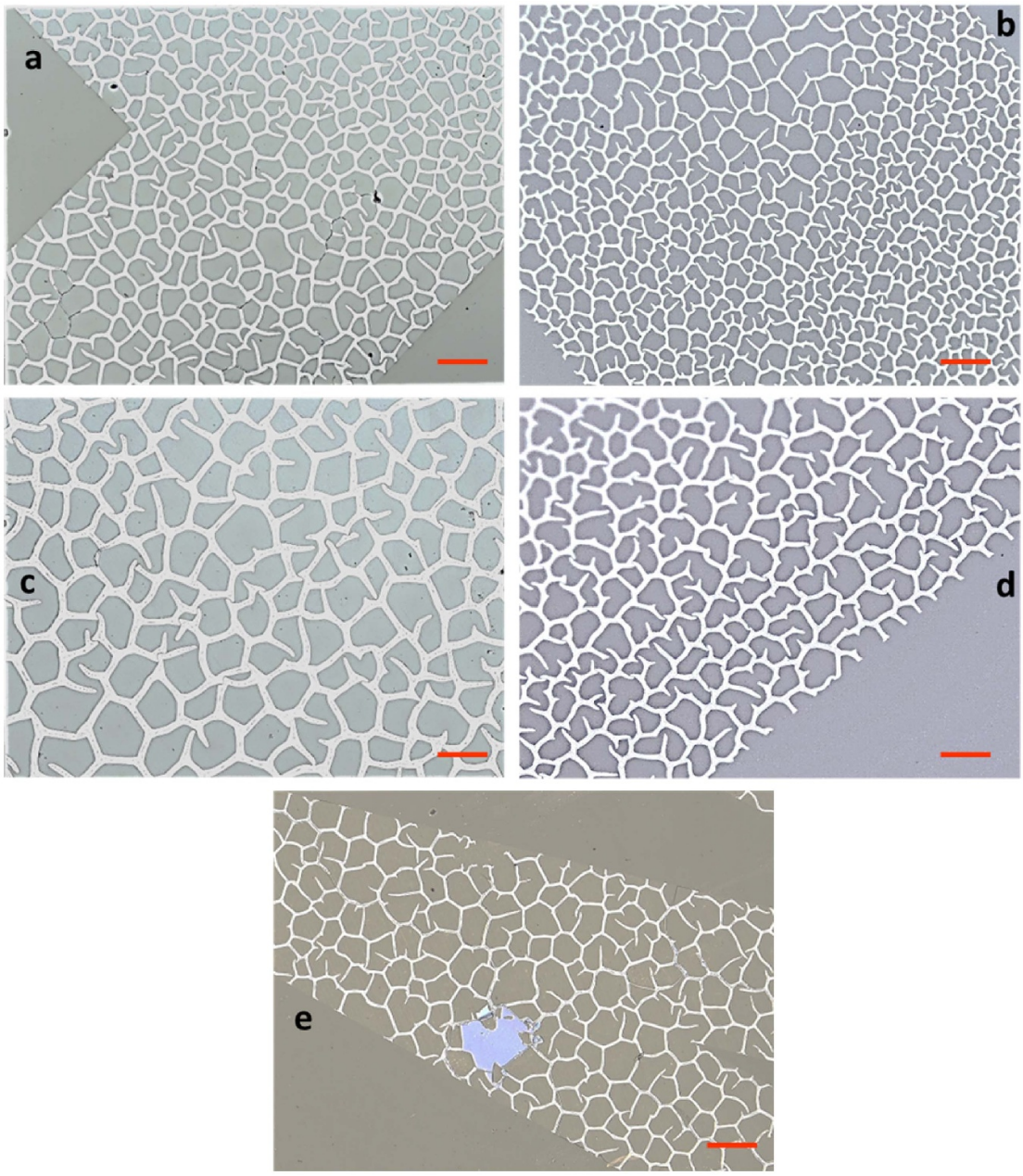

Figure 3. Keyence optical images of deposited oxide layers on device surfaces. The oxide buckled (lighter traces) due to internal stress and low adhesion to the graphene, but nonetheless remains continuous across the device surface. Oxide thickness was 1,250 nm in all images. Scale bars are 100 μm. (a) Default device before testing and (b) after. (c) High pitch device before testing and (d) after. Images taken after device tests experienced lower light conditions, but were otherwise identical. (e) Extreme Pitch device after testing, with a chip taken out of the oxide by a probe station micromanipulator, revealing the graphene surface beneath. Using a color filter to enhance image contrast, the exposed graphene can be seen as a light blue area, against the tan of the oxide where it conforms to the surface, and the buckled traces in white.

signs of change following repeated device testing. In figure 3(e), the graphene surface is only visible when the oxide is chipped away, while it is not visible in the traces of the buckled oxide, indicating that although the oxide is not conformal everywhere, it is continuous. The stark difference in adhesion between the oxide on the graphene surface and on the SiC is clear as well, along the edges of the devices, and even at the sharp internal corner of the extreme pitch design, at the bottom right of figure 3(e).

3.2. Device tests

Four standardized tests, two each at both high and low applied accelerating fields and with different application patterns, were used to evaluate device behavior and performance. Figure 4 shows the results from test 1, where the accelerating field is ramped from 0 V cm^{-1} to 1 kV cm^{-1} in 50 V cm^{-1} increments every 30 s. The emission currents seen in this show linear behavior across the test's entire range, and rise above the noise threshold at accelerating field values

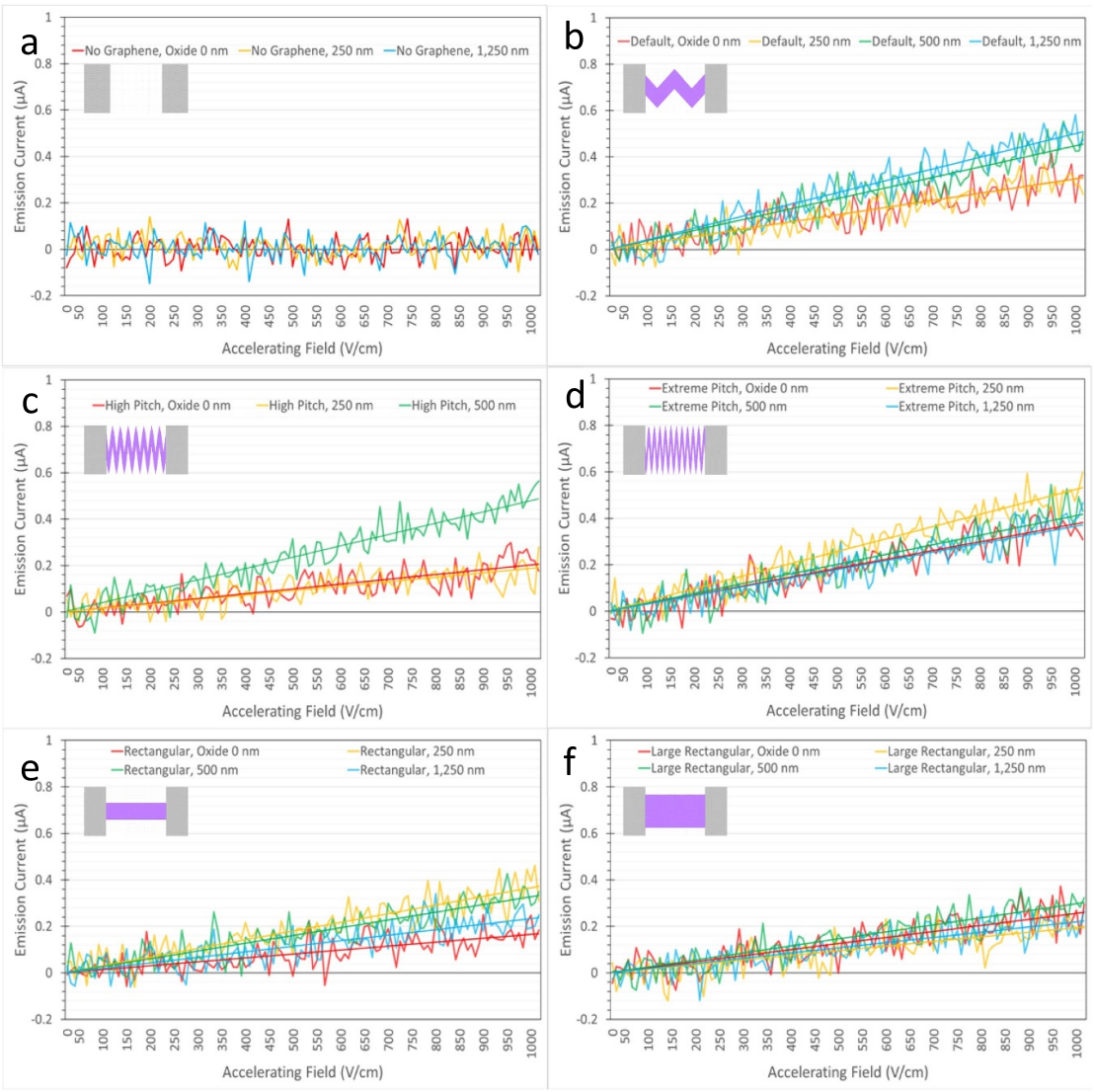

Figure 4. Test 1: the accelerating field is ramped from 0 V cm^{-1} to 1 kV cm^{-1} in 50 V cm^{-1} increments at 30 s intervals. Device names include oxide thicknesses in nm for each test.

as low as 300 V cm^{-1}, a value not readily identifiable in test 3. These results suggest that field emission should not be considered a significant contributing mechanism to the emission current, as discussed below.

Figure 5 shows the results from test 2, where the accelerating field starts at 1 kV cm^{-1} and is stepped down to 0 V cm^{-1} in increments of 50 V cm^{-1} every 30 s, with a 10-second gap of 0 V cm^{-1} in between each increment. Emission currents seen in this test follow the reverse of the linear path seen in test 1, while also immediately dropping below the noise threshold every time the accelerating field is set to 0 V cm^{-1}. These results highlight the necessity of an applied accelerating field for collecting the emission current, and also suggest that the emission current is isotropic, as discussed below.

Figure 6 shows the results from test 3, where the accelerating field is ramped from 0 V cm^{-1} to 10 kV cm^{-1} in 500 V cm^{-1} increments every 30 s. Figure 7 shows the results from Test 4, where the accelerating field starts at 10 kV cm^{-1} and is stepped down to 0 V cm^{-1} in increments of 500 V cm^{-1} every 30 s, with a 10-second gap of 0 V cm^{-1} in between each increment. Tests 3 and 4 are procedurally identical to tests 1 and 2, respectively, but the higher accelerating fields and measurement limits reduce the impact of noise on the results, while device behaviors remain the same.

The collective results from all Tests support the conclusion that the emission current observed from the devices is driven primarily by the mechanism of PAEE. During the tests, devices were held at a static temperature of 215 °C, well below the predicted values of ∼600 °C–1300 °C that would be required to obtain a measurable thermionic emission current from graphene [15–17]. Field emission from planar graphene has been reported, but at applied

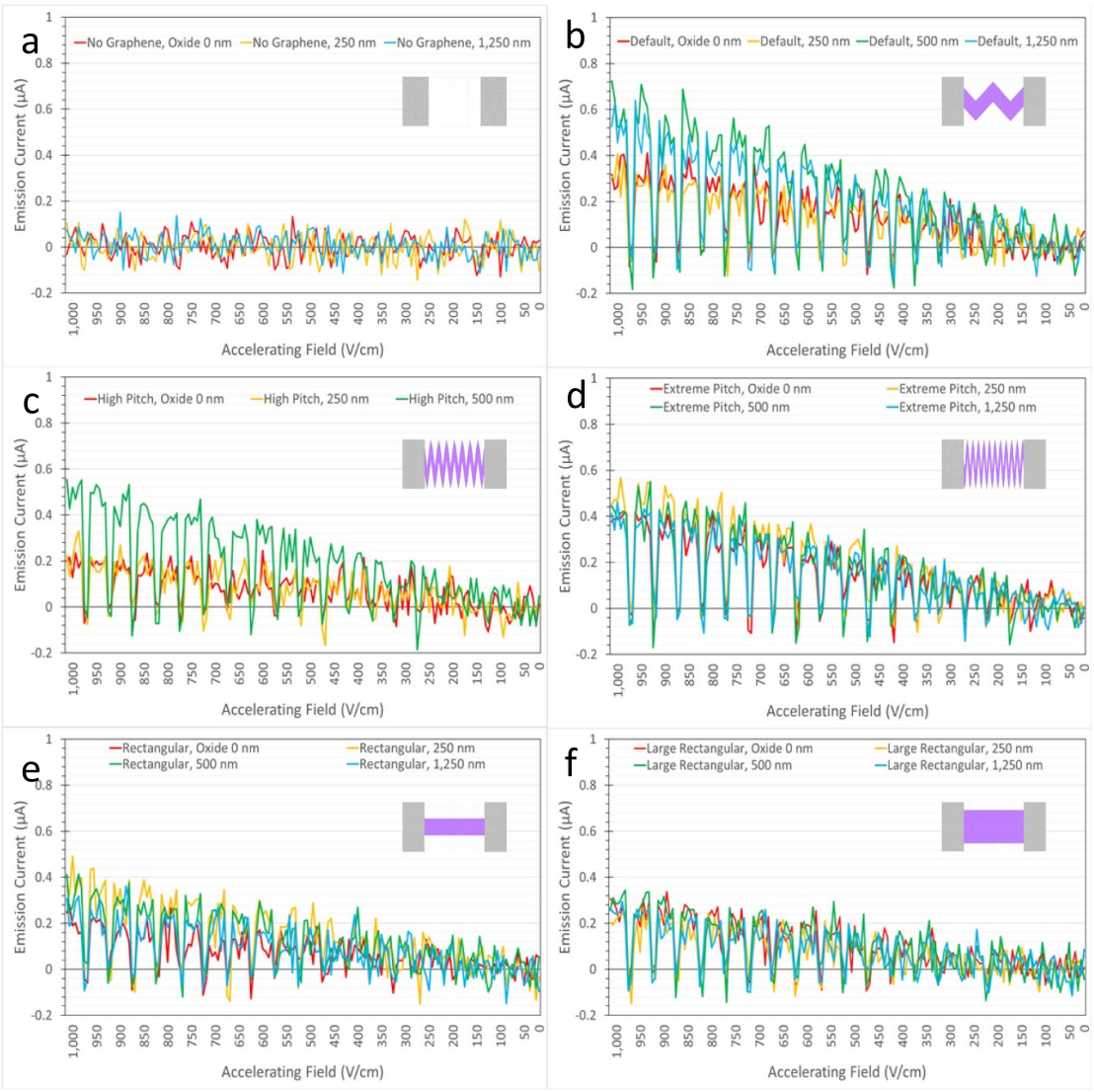

Figure 5. Test 2: the accelerating field is stepped down from 1 kV cm^{-1} to 0 V cm^{-1} in 50 V cm^{-1} increments at 30 sec intervals, with 10 sec of 0 V cm^{-1} between each increment. Oxide thickness is listed in nm.

fields of 50 kV cm^{-1} or more [18–20], while the devices presented here displayed output above the noise threshold at applied fields as low as 300 V cm^{-1}, and the Tests stopped at 10 kV cm^{-1}.

When shown graphically, both thermionic and field emission I vs. E curves take on a kind of 'bent knee' shape, reminiscent of a forward-biased diode, showing little appreciable emission activity until a turn-on point, followed by a sharp rise. Our devices, though, show a linear relationship between output and applied field at all times, indicating that they do not experience the 'turn-on point' that would be characteristic of other emission methods. As was previously shown [11], with the operating parameters of the Tests we conducted here, both thermionic and field emission currents would be far too low to be relevant contributors to the output currents measured, and so cannot be credited with the device activity, so PAEE remains the primary mechanism.

The linear relationship between the emission currents of the devices and the applied fields of the Tests furthermore suggests that the electron emission from the graphene surface, or ultimately from the outermost layered oxide surface, is isotropic. If the QFEG devices were emitting preferentially towards non-conductive elements of the containment package, we would expect the emission currents to either grow logistically with increasing applied fields (starting low, growing gradually, and then saturating), or exponentially decay with decreasing applied fields (starting high, and rapidly dropping). If the devices were emitting preferentially towards the collection plate, we would expect exponential growth with increasing field, or logarithmic decay with decreasing field (staying high for longer, and only slowing dropping off). These behaviors are not shown, all the curves show clear linear dependence throughout the Tests. Isotropic electron emission is consistent with

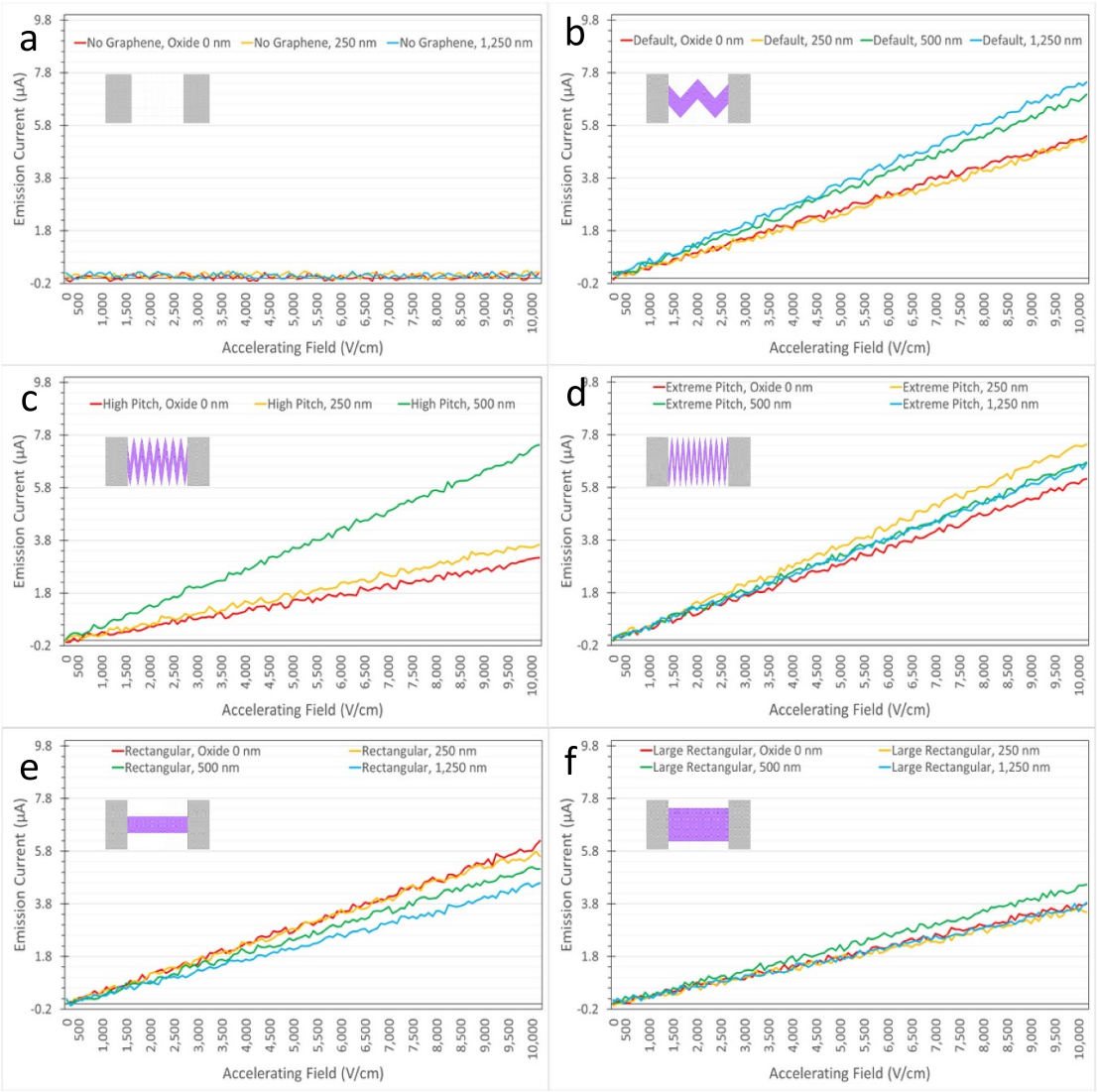

Figure 6. Test 3: the accelerating field is ramped from 0 V cm^{-1} to 10 kV cm^{-1} in 500 V cm^{-1} increments at 30 s intervals. Device names include the oxide thickness in nm for each test.

conventional electron sources, which use a Wehnelt structure to selectively filter out emitted electrons that are not aligned along the emitter's central axis [21]—a structure which the devices presented here do not currently employ. Due to the unconventional nature of the emitters presented here, and the limitations of the equipment and measurement methods the authors have access to, it was determined that incorporating a Wehnelt-type structure could result in the emission currents being artificially and inconsistently reduced below measurement thresholds, rendering test results unreliable, and as such it was determined to omit such a structure from the entirety of the testing arrangement.

Unfortunately, all test data for the Nothing device at the 500 nm oxide step, and the High Pitch device at the 1250 nm oxide step, are unavailable for this publication. An unknown error corrupted the data from the Nothing device with 500 nm of oxide, rendering it unreadable, and the error was not detected until after the third oxide layer deposition was completed. Prior to the third oxide deposition, an unrelated equipment failure resulted in the physical destruction of the high pitch device. In both cases, a shortage of time, equipment availability, and necessary materials precluded the devices being reconstituted and retested. The authors propose that the absence of these data sets, though unfortunate, does not compromise the observations or conclusions presented herein.

3.3. Device morphologies

The differences in device behaviors at equal stages of each test can be attributed to the varying shapes of the graphene that comprises the electron emission surface, as it is the only remaining variable. It was previously shown that the zig-zag patterned device outperformed other shapes of equal dimensions, and the tests performed here serve to further refine and evaluate that initial finding.

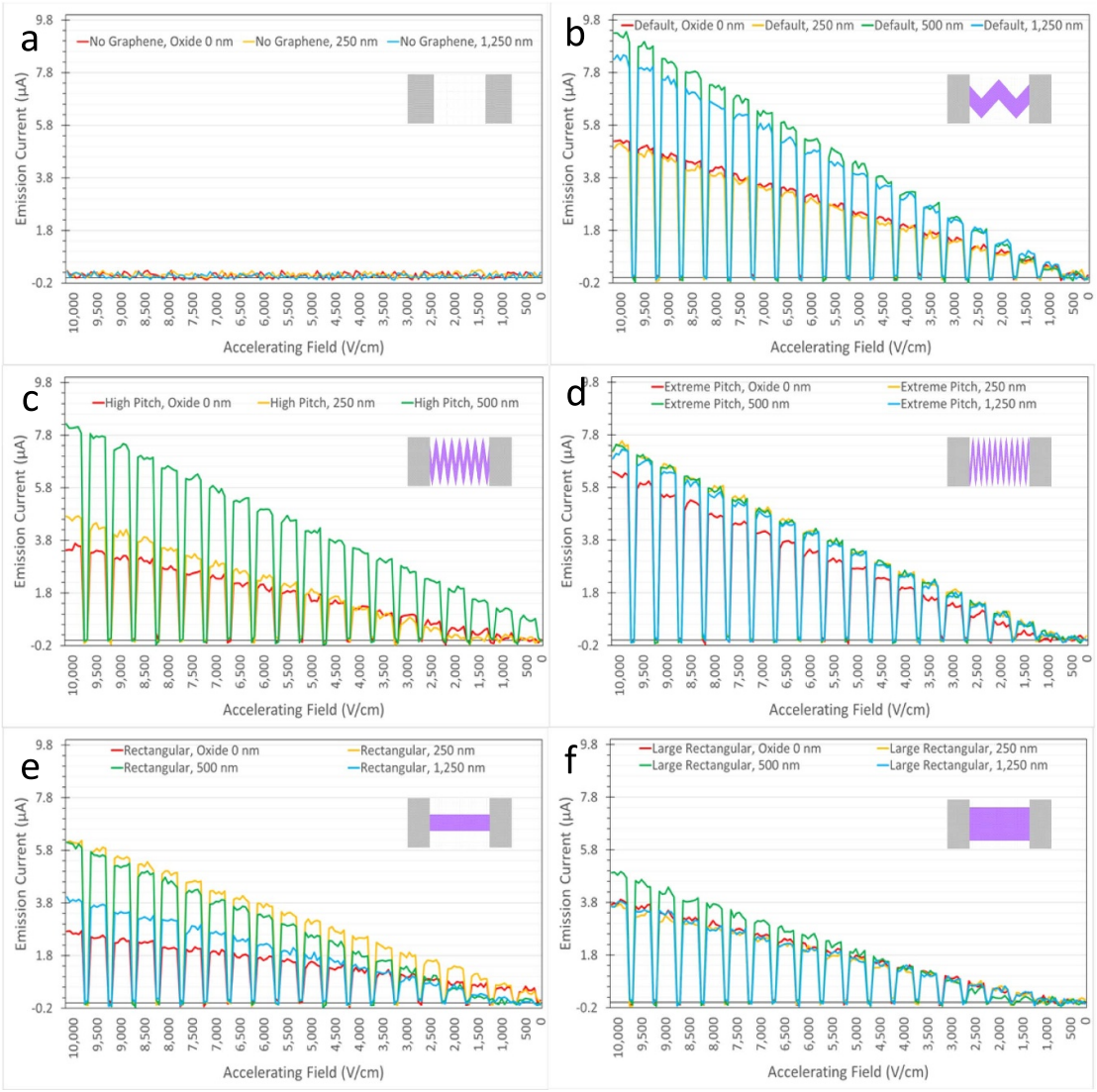

Figure 7. Test 4: the accelerating field is stepped down from 10 kV cm^{-1} to 0 V cm^{-1} in 500 V cm^{-1} increments at 30 s intervals, with 10 s of 0 V cm^{-1} between each increment. Oxide thickness is listed in nm.

The 'Nothing' device (bare SiC) clearly illustrates that the QFEG structure alone is responsible for the observed emission currents. The high-profile shapes of the wire bonds, the bare metal of the resistive heating elements, and every other conductive source in the device package are exposed to the same applied electric field, with an unobstructed path to the current collection electrode, and yet no results beyond the background noise are found at any point. The Nothing device also demonstrates that the oxide layers are not an electron source in and of themselves, and any electron interactions the oxide experiences must therefore originate from the graphene emitters they are deposited on.

Similar to what was shown in our earlier work, the Rectangular device shape—a straight-line path on the graphene between the contacts—underperforms in every test, compared to the zig-zag patterns. Additionally, though it might at first seem unintuitive, the Large Rectangular device—the same shape as the Rectangular, only twice as big—consistently exhibits *less* emission current. We credit both of these performance patterns to the mechanism of PAEE as well, in that for electrons to be emitted in this regime, they must interact with hot forward-scattering (FS) phonons.

As Wei *et al* found, only FS electron-phonon interactions actually contribute to a PAEE-driven emission current [22, 23]. The specific shapes of the Rectangular, and Large Rectangular, devices might actually be interfering with that mechanism, though, by allowing a greater accessible graphene area. This increased graphene area would dilute the current density through the device, as the applied current

of 10 mA was constant for all cases. The Bose-Einstein phonon distribution is dependent on lattice temperature [23]:

$$g_n(T) = \frac{1}{\left(e^{\frac{E_n}{k_b T}} - 1\right)}$$

where g_n is the phonon distribution at temperature T (kelvin), w_n is the phonon frequency, k_b the Boltzmann constant, and $\hbar$ the normalized Planck constant so that an individual phonon's energy is given by $E_n = \hbar w_n$.

As device temperatures were all held constant, we must conclude that having a greater graphene area would also decrease the phonon density across that area. With decreased densities of both electrons and phonons, it logically follows that the frequency of their energetic interactions would decrease, and by the PAEE mechanism, the emission current would decrease. And this is the behavior we see in the large rectangular device when compared to the normal rectangular one, with all other test variables matched between them. This conclusion is also illustrated by the performance of both Rectangular devices in comparison to the other device morphologies: the rectangular devices underperformed compared to all the others, despite having the same total area as the emission surface.

However, the effects of having constraints on the freedom of movement of the electrons and phonons appears to also have an upper limit, as illustrated by the three different varieties of zig-zag pattern devices. In tests 1 and 3, the extreme pitch device seems to have the strongest performance, while in tests 2 and 4 it is the default device, with the high pitch device falling somewhere in between in all cases. This pattern appears to indicate two points: (1) the devices' performance can be consistently enhanced by forming the graphene into a circuitous shape in order to increase the likelihood of electron-FS phonon interactions by restricting their available paths, and (2) that an optimization of this design is possible. Such an optimization may require numerous additional tests and fabrications with incremental changes, and is beyond the scope of this work.

3.4. Oxide layers

Device performance shows distinct changes when the layers of SiO_2 are added, in most cases being enhanced beyond the results of the devices without oxide on them. The results from the nothing device highlight that when the devices are tested with the oxide layers present, the emission current solely results from the electrons being emitted from the graphene, as the oxide produces no emission current on its own. Since the devices are entirely encapsulated by the oxide, the most likely way for this electron multiplication effect (measured as an increase in total current overall) to be manifested would be through SEE, as the electrons released from the graphene energetically interact with electrons in the oxide, granting them enough energy to enter the conduction band and ultimately to surmount the vacuum barrier and escape the structure.

Across all four tests, most of the devices follow a similar pattern with regards to the oxide: at 250 nm thick, the total emission current from the devices is higher than that of the devices with no oxide at all. At 500 nm, total emission current tends to increase a little more, then at 1250 nm, the emission current appears to come back down. This pattern suggests that for thinner oxide layers, more electrons are generated through SEE than are lost to recombination, but for thicker layers, the kinetic energy loss from the interactions overwhelms the secondary electron production, leading to a lesser total of free electrons overall.

The authors surmise, then, that an optimal oxide thickness must exist wherein the generation of secondary electrons and recombination of interacting electrons balances, and the emission current finds a local maximum, but the current data set is insufficient to identify that value. The performance pattern of the devices is not completely uniform, indicating that the emission current behavior is likely not governed by the single factor of the oxide thickness, though speculation on the additional mechanisms contributing to this behavior is beyond the scope of this work.

It is also worth noting that the resultant device behaviors were not precisely mirrored between tests 3 and 4, when the accelerating field is ramped up and stepped down, respectively. The authors posit that this may be due, at least in part, to both the differences in behavior of the devices due to their morphology and also to irregular charging and discharging of the oxide layer between these tests. In test 3, as the accelerating field is ramped up, charges may become trapped in the oxide and remain there when the test is terminated, only to then be released when test 4 is performed.

3.5. Oxide layers—structure and transmission current

When the deposition method is e-beam evaporation, it is common for SiO_2 to sublimate and contact the surface in roughly spherical shapes of various size [24–27]. These shapes inevitably coalesce into the amorphous structure SiO_2 is well known to form, and on our devices it was found that the uppermost surface of the oxide retained a rough topography consisting of these deformed spherical shapes, ranging in size from roughly 100–300 nm, as shown in figure 8.

In a substance with a regular crystalline structure, it is possible that the emitted electrons could experience channeling, wherein the crystallographic alignment forms an unimpeded path through the component atoms, as is seen during the ion implantation

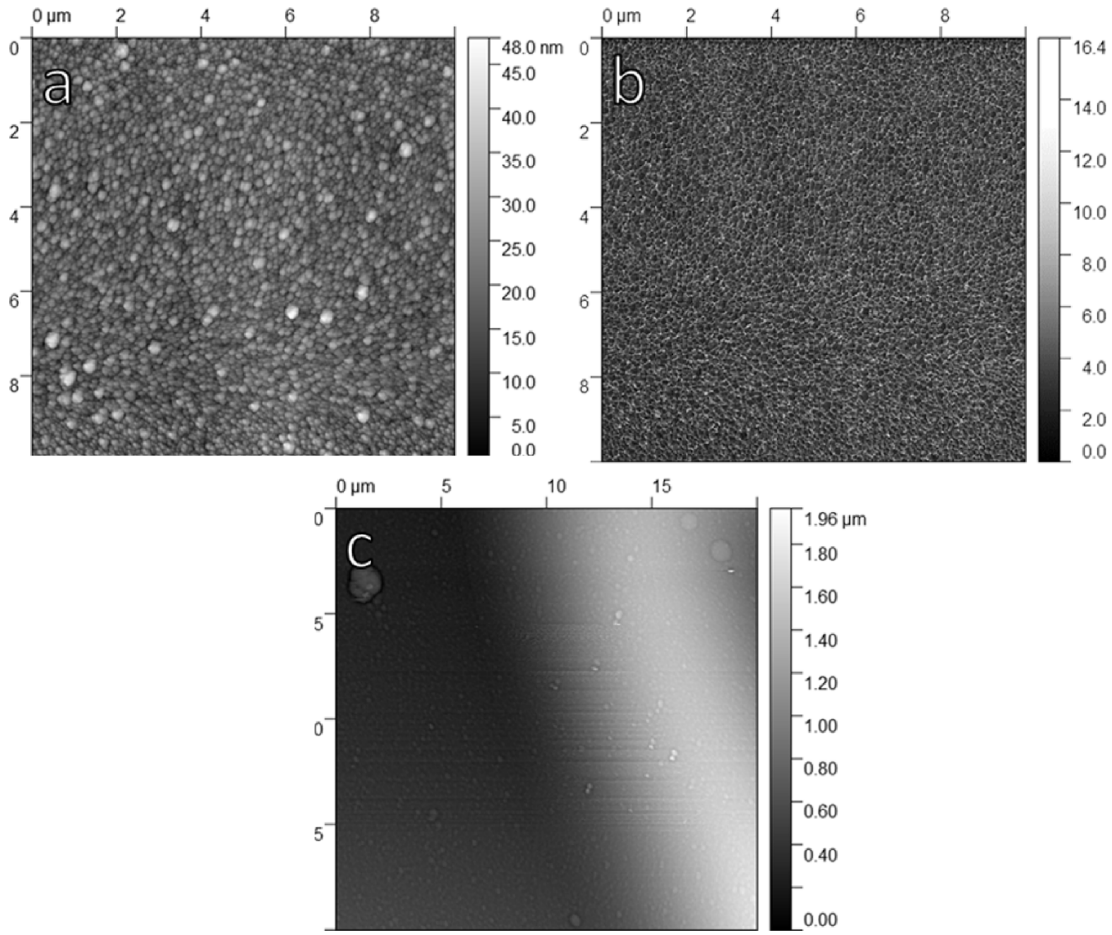

Figure 8. AFM height (a) and phase retrace (b) of the 1250 nm oxide layer. The surface appears rough and amorphous, as expected for SiO_2, with grain sizes between ∼50–300 nm. Height retrace max displacement is 50 nm, indicating that the oxide layer is continuous across the area, with no pinholes reaching the graphene layer below. (c) Height retrace of the edge of a blistered trace in the oxide layer. The buckled ridge of the oxide nearly doubles the total height from the graphene surface, but still appears continuous over the area, with no breaks or pinholes to the graphene.

method of semiconductor doping [28–30]. However, SiO_2 is amorphous, rendering this behavior unlikely, especially across the numerous grain boundaries that would inevitably arise from this deposition method.

Simulations performed with the CASINO (monte CArlo SImulation of electroN trajectory in sOlids) [31] package suggest that the electrons originating from the graphene are unlikely to traverse the full thickness of the oxide at any stage aside from the thinnest oxide layers at the higher accelerating voltages; this is broadly not in agreement with the actual measurements that were observed. Although some electrons could potentially pass through the oxide layers, as shown in the Supporting Information, they cannot account for the total emission currents observed, nor could they account for the increase in emission currents observed in the presence of the oxide layers compared to the devices when they were tested without the oxide. We must conclude, then, that the electrons emitted from the graphene and transiting the oxide cannot be the dominant mechanism at work, nor can it account for the emission current *increases* in later tests, and SEE must be the dominant mechanism.

3.6. Oxide layers—electron multiplication

In the case of SEE from the oxide layer, electrons emitted from the graphene, and accelerated by the applied external electric field, interact with electrons in the oxide, imparting enough energy to these (secondary) electrons to allow them to escape the material entirely. Some primary electrons may be incident with enough energy for multiple such interactions, and some secondary electrons may gain enough energy to free additional electrons themselves, and so the total number of released electrons is greater than the incident number (electron multiplication). Charge neutrality of the oxide is maintained due to the oxide being in direct contact with the rest of the device, all of which is itself conductive, between the graphene and its contact pads on either side.

The secondary electron yield (SEY) of a material describes how many secondary electrons are released per incident particle. To be released to the vacuum level, an electron must have energy in excess of the electron affinity (EA) of a material (usually about 10 eV more than the EA is enough to ensure the electron does not get attracted back to the surface it was

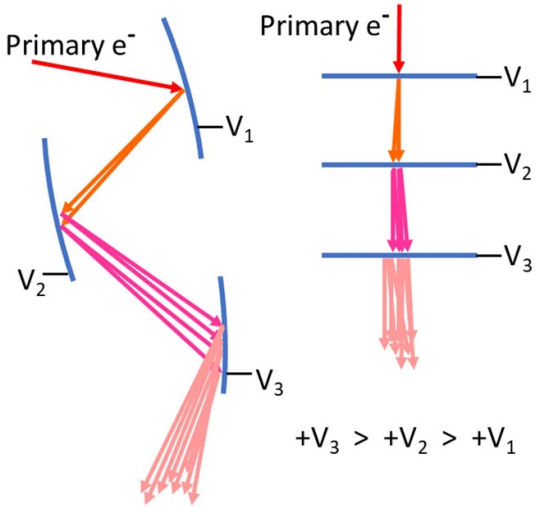

Figure 9. Electron multiplication via reflective and transmissive dynodes.

just released from) [32–35]. Additionally, electron-electron interactions in the conduction band result in high energy loss, so a lower conduction band occupation is advantageous; secondary electrons in insulators tend to interact with lattice phonons, thereby losing less energy in each event, and can promote valence band electrons [34]. Wider band gap oxides have lower EAs than metals, allowing a greater proportion of secondary electrons to have the energy needed to escape. For example, SiO_2 has an SEY of ~4.3, compared to 1.4 for Cu (with some surface oxide), 1.8 for Pt, 0.5 for Li, or 0.95 for pure aluminum (increasing to 2.5 after some oxidation) [36–38].

As previously stated, translating a material's SEY into an electron multiplication effect can be accomplished with a series of dynodes. A dynode array consists of discrete elements of a material with a significant SEY, arranged in such a way that electrons impacting each stage of the dynode will be amplified, then the amplified electrons will strike more dynodes and be amplified again, and so on. A typical arrangement can be as a series of reflective surfaces with ever-increasing potentials, to draw in the electrons, as shown in figure 9 [39].

Alternatively, it can be set up as a series of interaction surfaces, where the incident electrons enter one side of a thin surface, multiply due to interactions, and emerge from the far side of the surface and continue on, as a transmission rather than a reflection, in this case referred to as a tynode (transmission dynode), as shown in figure 9 [39]. Continuous thin film tynode stacks for electron multiplication have been implemented with different materials and geometries [8, 40–42], including a stack of TiN/Al_2O_3 membranes wherein the membranes are curved in order to focus each tynode layer's resulting electrons into the next tynode layer [43].

While it is unlikely that the electrons are experiencing any kind of focusing within the amorphous structure of the evaporated SiO_2, we propose that it is possible the electrons could be interacting with the oxide in a kind of tynode format regardless. The graphene device and its oxide layer are immersed in the applied electric field, which is set between the upper and lower electrodes that are physically separated from the structure of the device itself.

As an emitted electron leaves the graphene and passes upward through the oxide, it moves closer to the anode, experiencing the higher bias as it moves through the equipotential lines. In the tynode format, as illustrated in figure 9, an electron encounters a material at a higher potential, gains energy from the traversal, and interacts with the surface, releasing secondary electrons that are then also accelerated by the field to experience more interactions, and so on. This behavior could allow the entire oxide layer to act as a series of tynodes stacked on top of each other, and could account for the increase in emission current when the oxide is present vs. when it is not. The end result being that the emission current increases for thinner oxide layers, then decreases when the electrons lost to collisions outnumbers the electrons gained thanks to the SiO_2's SEY, which matches the behavior that was observed during the tests.

The test results from the nothing device clearly demonstrate both that the only thing actually producing electrons to be emitted is the graphene microstructure itself, and also that merely the presence of the oxide layer is not sufficient to result in electron emission. Thus, the only mechanism that could result in more electrons being generated *with* the oxide layers than without is the interaction between the electrons emitted from the graphene and the atoms of the oxide, i.e. SEE.

4. Conclusions

Electron emission is demonstrated from planar microstructures fabricated from quasi-freestanding epitaxial graphene on a semi-insulating silicon carbide substrate, achieving emission currents as high as 9.4 μA via phonon-assisted electron emission (PAEE). The essential role of graphene in device operation is demonstrated, and variations in device performance based on intentional design are catalogued in greater detail than in previous work.

Furthermore, it is shown that the devices can produce measurable emission current even when fully encapsulated in a silicon dioxide layer, and that such a layered structure can even see an increase in total

output attributed to SEE from the oxide itself. Not all device morphologies follow the same exact performance pattern relative to the oxide, however, nor do they all experience the same magnitude of changes. The authors feel that there is insufficient data as of yet to identify or evaluate a potential link between both variables simultaneously, but the experimental results suggest such a link could be possible and worthy of investigation.

The implications of this design would ultimately represent a combined electron emission source and electron multiplication method without needing to operate in vacuum. Paired with an anode material layered on top of the oxide, to allow for electrical isolation and interaction emission, could produce a layered material heterostructure that operates as an x-ray emission source without the need for vacuum containment.

Future efforts will include an investigation into the device behaviors when the oxide layer is included, with the intent of formulating an electron emission heterostructure stack and an optimized device design. Such a stack, when combined with a layered interaction anode, may allow for a structure that can generate low energy x-rays without the need for vacuum containment.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

The authors would like to thank the staff of the University of Maryland Fabrication Laboratory for providing essential facilities support. Mr Bryan Quinn and Dr Don Schmadel of the University of Maryland, Institute for Research in Electronics and Applied Physics, and Dr Francis P McCluskey, University of Maryland Department of Mechanical Engineering, for critical equipment. Dr Sean Horan of Boston Scientific, Marlborough, MA, provided essential insight and consultation. Work at the US Naval Research Laboratory was supported by the Office of Naval Research. This research was performed while Dr Daniel Pennachio held an NRC Research Associateship award at NRL. Dr Jenifer Hajzus acknowledges the American Society for Engineering Education Naval Research Laboratory Post-doctoral Fellow program. This work was supported by NSF under the Award CBET-2145549. Funding for the AFM shared facility used in this research was provided by NSF under the Award CHE-1626288.

ORCID iDs

Daniel Lewis https://orcid.org/0000-0002-8379-6731
Daniel J Pennachio https://orcid.org/0000-0002-0797-5076
Jenifer R Hajzus https://orcid.org/0000-0002-2227-4868

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