ABSTRACT

Title of Document: END-OF-LIFE AND CONSTANT RATE RE-
                        LIABILITY MODELING FOR SEMICON-
                        DUCTOR PACKAGES USING KNOWLEDGE-
                        BASED TEST APPROACHES

                        LIYU YANG, Doctor of Philosophy, 2009

Directed By: Professor Joseph B. Bernstein, Reliability Engi-
                        neering, Department of Mechanical Engineering,
                        University of Maryland at College Park.

End-of-life and constant rate reliability modeling for semiconductor packages are the focuses of this dissertation. Knowledge-based testing approaches are applied and the test-to-failure approach is approved to be a reliable approach. First of all, the end-of-life AF models for solder joint reliability are studied. The research results show using one universal AF model for all packages is flawed approach. An assessment matrix is generated to guide the application of AF models. The AF models chosen should be either assessed based on available data or validated through accelerated stress tests. A common model can be applied if the packages have similar structures and materials. The studies show that different AF models will be required for SnPb solder joints and SAC lead-free solder joints. Second, solder bumps under power

cycling conditions are found to follow constant rate reliability models due to variations of the operating conditions. Case studies demonstrate that a constant rate reliability model is appropriate to describe non solder joint related semiconductor package failures as well. Third, the dissertation describes the rate models using Chi-square approach cannot correlate well with the expected failure mechanisms in field applications. The estimation of the upper bound using a Chi-square value from zero failure is flawed. The dissertation emphasizes that the failure data is required for the failure rate estimation. A simple but tighter approach is proposed and provides much tighter bounds in comparison of other approaches available. Last, the reliability of solder bumps in flip chip packages under power cycling conditions is studied. The bump materials and underfill materials will significantly influence the reliability of the solder bumps. A set of comparable bump materials and the underfill materials will dramatically improve the end-of-life solder bumps under power cycling loads, and bump materials are one of the most significant factors. Comparing to the field failure data obtained, the end-of-life model does not predict the failures in the field, which is more close to an approximately constant failure rate. In addition, the studies find an improper underfill material could change the failure location from solder bump cracking to ILD cracking or BGA solder joint failures.

END-OF-LIFE AND CONSTANT RATE RELIABILITY MODELING FOR SEMI-

CONDUCTOR PACKAGES USING KNOWLEDGE-BASED TEST APPROACHES

By

LIYU YANG

Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
2009

Advisory Committee:
Associate Professor Joseph B. Bernstein, Chair/Advisor
Associate Professor Hugh Bruck
Associate Professor Patrick F. McCluskey
Professor Peter Sandborn
Professor Peter Kofinas, Deans Representative

Dedication

To my parents, my wife, my brother, and my kids.

Acknowledgements

Table of Contents

List of Tables

List of Figures

xxii

List of Illustrations

$\lambda(T)$	failure rate as a function of temperature
$\lambda(V)$	failure rate as a function of voltage
λ_s	system failure rate
γ_0, γ_1	constant
ε_f	the fatigue ductile coefficient in shear
a	constant
b	constant
c	constant
d	constant
dL_c/dN_c	crack growth rate
k	Boltzmann constant, 8.617343x10-5 eV/K
t	time
t_a	dwell time at use conditions
t_t	the dwell time at test conditions
t_f	time to failures
X	thickness of the diffusion layers
$\Delta\varepsilon$	inelastic strain range

$\Delta\varepsilon_p$	plastic strain
$\Phi(T_{max})$	function in N-L equation, related to the maximum temperature
ΔK	intensity factor
ΔK_{eff}	the effective stress intensity factor range
ΔT	temperature interval or temperature range
ΔT_{use}	temperature range/interval at use or field conditions
ΔT_{test}	temperature range /interval at test conditions
ΔW	viscoplastic strain energy density accumulated per cycle
ΔW_{avg}	average viscoplastic strain energy density accumulated per cycle
A	constant
AATC	air-to-air thermal cycling
AF	acceleration factor
AF_1	acceleration factor for failure mechanism I
AF_2	acceleration factor for failure mechanism II
$AF_{\Delta T}$	acceleration factor due to temperature interval/range
AF_{base}	Acceleration factor value from N-L format
AF_f	acceleration factor due to cycling frequency

AF_{RH}	acceleration factor due to RH stress acceleration
AF_s	acceleration factor for the system
AF_T	acceleration factor due to temperature acceleration
$AF_{(T, RH)}$	acceleration factor due to temperature and relative humidity
$AF_{(T,V)}$	acceleration factor due to temperature and voltage acceleration
AF_V	acceleration factor due to voltage acceleration
B	a value dependent on thermal profiles (average temperature of the solder and the half dwell time
C	constant
C4	controlled collapse chip connections
$Corr(\Delta T_{use})$	temperature excursion range dependent correction factor for use
$Corr(\Delta T_{test})$	temperature excursion range dependent correction factor for test
CSAM	c-mode scanning acoustic microscopy
CTE	coefficient of thermal expansion
dL_c / dN_c	crack propagation rate per thermal cycle
DNP	distant neutral point
E_a	activation energy

EM	electromigration
ENIG	electroless Ni immersion Au
EOS	electrical overstress
ESD	electron static discharge
f	cycle frequency
f_{use} or f_a	cycle frequency at use or field applications
f_{test} or f_t	cycle frequency at test conditions
$F(t,T)$	cumulative distribution function related to time t and stress factor T
$F(t,U)$	cumulative distribution function related to time t and stress factor U
FCBGA	flip chip ball grid array
FIB	focus ion beam
FP	failure percentage
FP_1	failure percentage due to failure mechanism I
FP_2	failure percentage due to failure mechanism II
g	the growth rate of the corrosion
G	a function of geometry
H	constant

H_{use}	stress factor of H at use conditions
H_{test}	stress factor of H at test conditions
HAST	highly accelerated stress test
HDI	high density interconnect
HTOL	high temperature operating life
ILD	inner layer dielectric
IMC	intermetallic compound
IPL	Inverse power law
J	the current density
K_0	constant
K_1	constant
K_2	constant
K_3	constant
K_4	constant
L_c	crack length
L_{eff}	the effective length between conductors
LGA	land grid array

M	the percentage moisture contents
M_t	the percentage of the threshold moisture content
m	constant for cycle frequency term in N-L model
MTTF	mean- time- to- failure
$MTTF(T_{use})$	mean- time- to- failure at use condition temperature
$MTTF(T_{test})$	mean- time- to- failure at test condition temperature
n	constant for temperature range term in N-L model
n_i	fractional sub-population for each failure mechanism i
NF	number of failure mechanisms
N_0	initial number of cycles to crack initiation
N_f	number of cycles to failures
$N_{test}\ or\ N_t$	number of cycles at test conditions
$N_{use}\ or\ N_a$	number of cycles at use conditions
OLGA	organic land grid array
OSP	organic solderability preservatives
PBGA	plastic ball grid array
PC	power cycling

PCB	printed circuit board
PCT	pressure cooker test
PQFP	plastic qual flat package
PTH	plated through hole
QFP	quad flat package
QFN	quad flat no-lead
$R(t)$	reliability at time t
RH	relative humidity, %
RH_{use}	relative humidity at use or field conditions
RH_{test}	relative humidity at test conditions
s	constant related to temperature
SAC	Sn-Ag-Cu solder alloy
SAC105	Sn-1Ag-0.5Cu solder alloy
SAC205	Sn-2Ag-0.5Cu solder alloy
SAC305	Sn-3Ag-0.5Cu solder alloy
SAC405	Sn-4Ag-0.5Cu solder alloy
SOIC	small outline integrated circuit
SnPb	eutectic Sn and Pb solder

t	time
t_d	half dwell time
T	temperature, K^o
T_{max}	Max temperature of the thermal profiles
T_s	cycle temperature of solder
T_{sj}	the average temperature of the solder
T_{use}	temperature at use or field conditions
T_{test}	temperature at test conditions
T_{use_max}	maximum temperature at use conditions
T_{test_max}	maximum temperature at test conditions
TC	thermal cycling or temperature cycling
TEBGA	thermally enhanced ball grid array
TH	temperature and humidity
T_g	glass transition temperature
TS	thermal shock
U	stress factor
UBM	under bump metrology

V	voltage stress, v
V_{use}	voltage at use or field conditions
V_{test}	voltage at test conditions
WB	wire bond
x_{tk}	thickness of the diffusion layer
z	constant related to temperature

1. INTRODUCTION

1.1 Semiconductor packages and systems

Semiconductor packages contain electrical circuits and interconnect which form desirable functional entities. In order to have reliable and robust package systems in the application, mechanical structures and enhancements / protections are required. In addition, the packages must provide adequate means for heat removal, since all circuits operate best at lower temperatures. Moreover, the packages must meet the required reliability performance under the specified conditions. The package design, assembly/ packaging processes, and packaging materials all contribute to the final reliability performance of the products.

Semiconductor packages can be categorized into two types of platforms, lead-frame based or substrate based. Small Outline Integrated Circuits (SOIC), Quad Flat Package (QFP) and Quad Flat No-Lead (QFN) packages are all lead frame based packages. The substrate based packages include Plastic Ball Grid Array (PBGA) packages, Thermally Enhanced Ball Grid Array (TEBGA) packages and Flip Chip Ball Grid Array (FCBGA) packages. The multiple interfaces in the package present a great challenge to manufacturing processes and reliability performance.

Figure 1-1 shows an example of a FCBGA package with a heat spreader, while Figure 1-2 shows a cross-section view of the package. The package consists of an organic substrate, a die, underfill materials to protect the die, flip chip bumps and solder balls for interconnects, a large copper heat spreader and some capacitors. In addition,

1

a layer of thermal interface materials provides a thermal pathway between the heat spreader and the die. The periphery of the heat spreader is affixed to the substrate.

Ball side view   Heat spreader side view
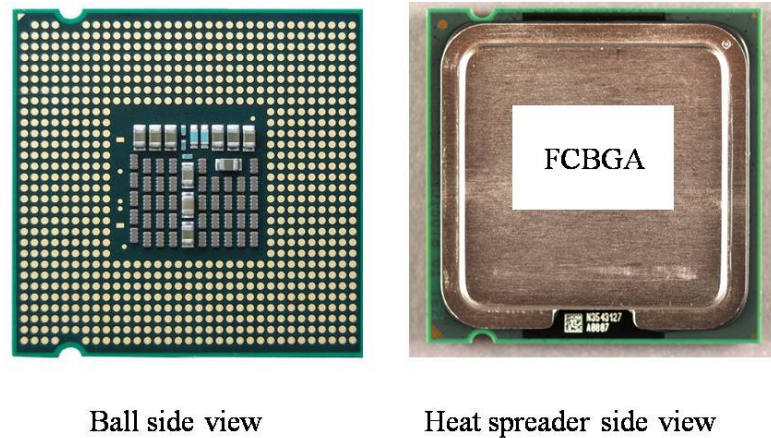
Figure 1-1 Images of a FCBGA package [Prismark, 2007]
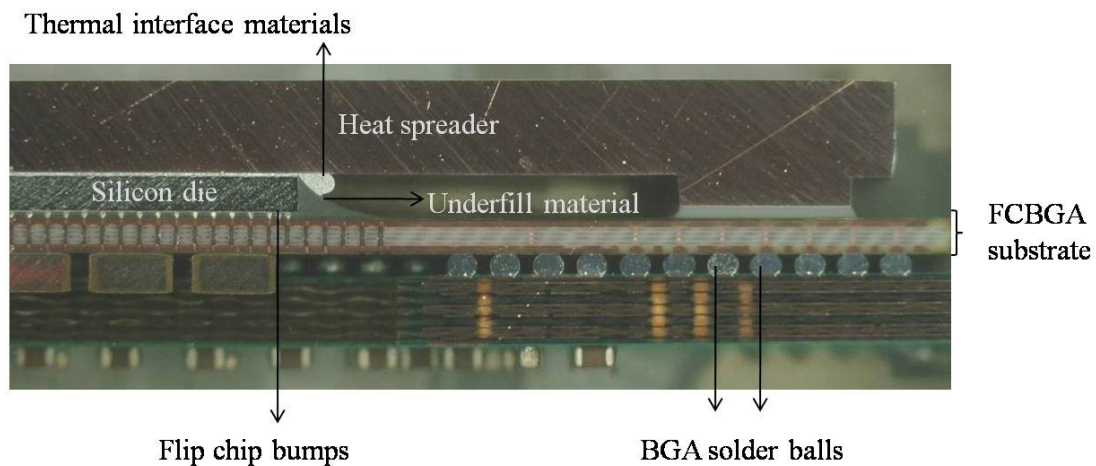
Figure 1-2 A cross section view of the package [Prismark, 2007]

Besides FCBGA packages, other technologies have been widely used, including various BGA packaging technologies using wire bond interconnects. Figure 1-3 shows a simple wire bond Land Grid Array (LGA) package, while Figure 1-4 shows a more complicated stack-up BGA package
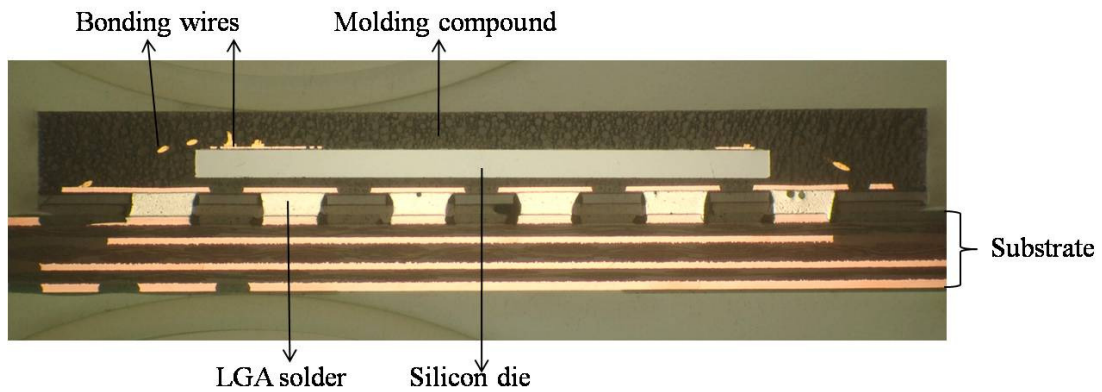
Figure 1-3 A cross section of a wire bond LGA package [Prismark, 2008]
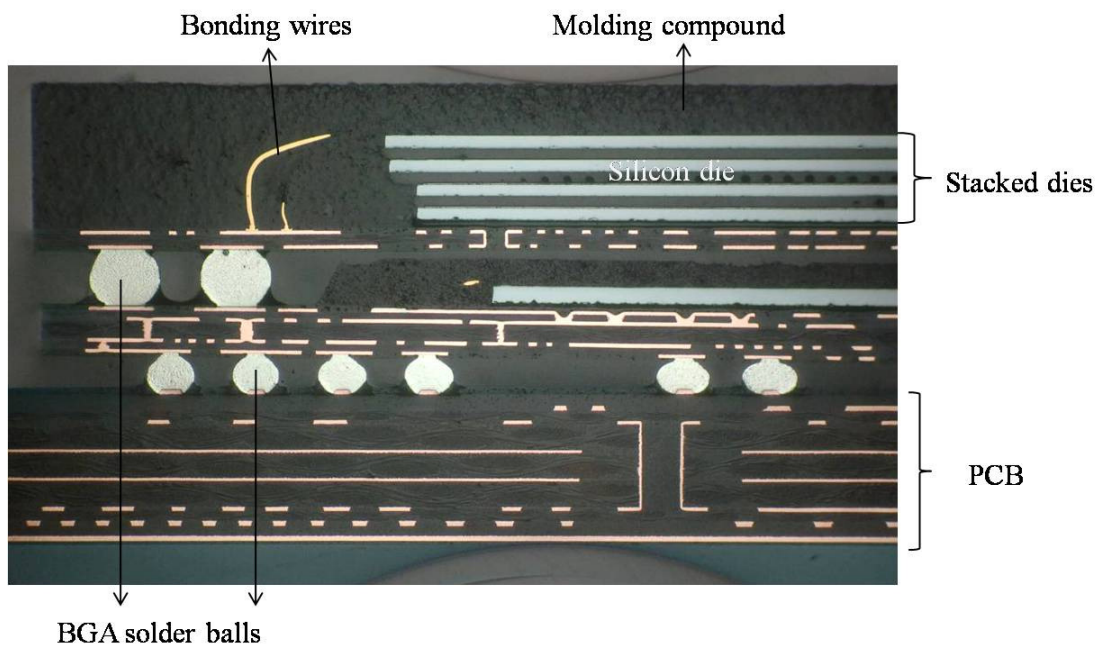
Figure 1-4 A cross section of a stacked BGA package [Prismark, 2008]

It is obvious that package technologies can be complicated. Moreover, their associated assembly processes and application conditions can post many reliability challenges. For example, the flip chip bumps can fail due to fatigue-induced cracking, the

3

silicon die can fail due to the inner layer dielectric (ILD) layer delamination, and there can be interface delamination and package cracking failures. In addition, the advancement in packaging processes and materials will require new approaches for the reliability enhancement or characterization of reliability models.   In the following section, key factors in the structures will be described:

1.1.1   Interconnects

Interconnections in package systems include bonding wires, flip chip bumps and the solder balls/leads. Obviously, interconnection failures will cause loss of function.

There are many variables influencing the interconnect reliability, such as interconnect materials, interconnect geometry and dimensions, process defects and other packaging materials that surround the interconnect.   For example, flip chip bumps can be made of high lead solder, eutectic solder or copper. Different bump materials will demonstrate different reliability performance with the same packaging materials set. In addition, different bump materials might require comparable Under Bump Metrology (UBM) structures and stack-up to achieve desired bump reliability.

Figure 1-5 shows a C-mode Scanning Acoustic Microscopy (CSAM) image of solder bumps Figure 1-6 showed a close-up bump structure.
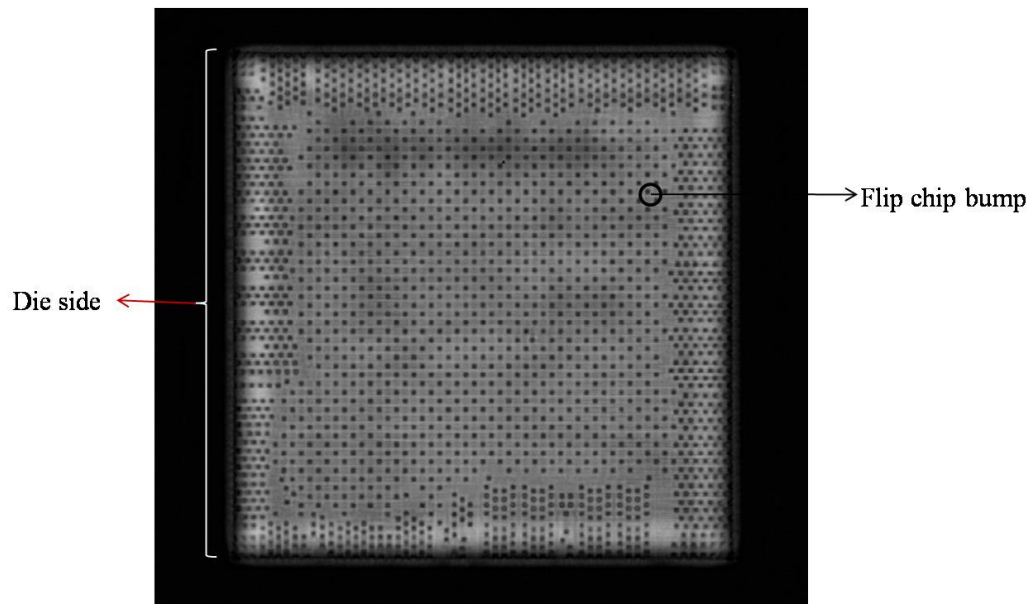
Figure 1-5 A CSAM image of the solder bumps
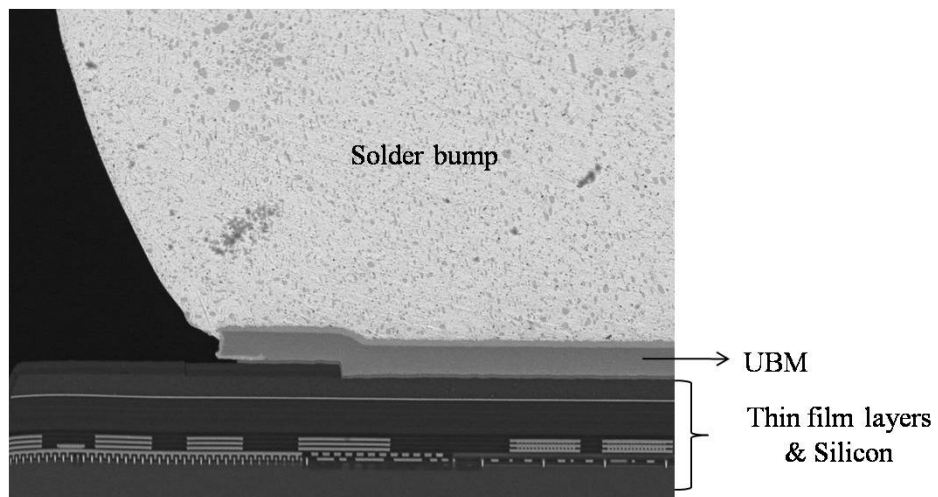
Figure 1-6 A close-up view of bump/UBM interfaces

1.1.2 Lead frames and substrates

Lead frames and substrates can be used as carriers to connect the die to the PCBs. However, they will add new challenges to the reliability of the package, due to their material variations, the surface finishes of the contacts and dimensions/geometries. In addition, the trends for high density substrates and high performance will aggregate the challenges.

1.1.3 Low-k / Cu silicon technology

With the demand for high performance and small form factor products, most advanced products are moving to low-k Cu silicon. The tradeoff for adopting low-k Cu silicon is the reliability challenges associated with low-k materials and the scale down of the gate length and other critical dimensions. For example, in low-k Cu silicon, low–k dielectric cracking and thin film delamination failures are dominant new failure mechanisms. The adoption of low-k Cu silicon will challenge the materials suppliers to come out with a compatible set of packaging materials to mitigate the risks in the package structure, such as the optimization of underfill materials in FCBGA packages. Figure 1-7 shows the ILD cracking failures due to the interaction between the silicon and packaging materials.
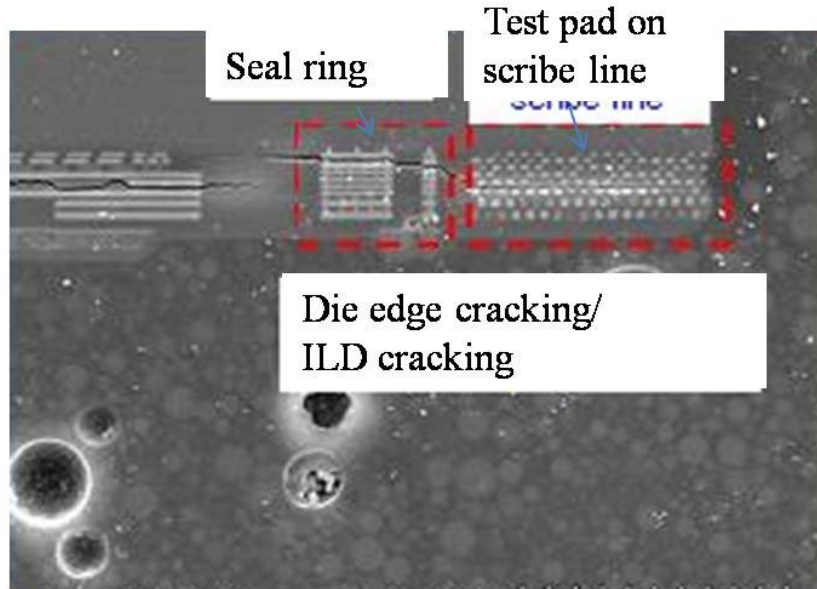
Figure 1-7 Low-k dielectric cracking in silicon [Yang and Walls, 2007]

1.1.4   Power dissipation and thermal profiles

Since the number of transistors packaged in a die is now higher, the power dissipation

has dramatically increased. In addition, the use conditions in thermal profiling are

more complex. As a result, the junction temperature and reliability performance of

the devices are affected.

1.1.5   Package reliability prediction and the failure rate estimation

In general, when package reliability has been discussed, it often refers to conducting

tests such as thermal cycling (TC), Highly Accelerated Stress Test (HAST) and High

Temperature Operating Life (HTOL), etc., for the packages. The expectation is that

tests will be passed based on pre-determined test conditions and durations. Little

knowledge has been obtained on the reliability life in the field, or on the estimation of failure rate. However, with more and more focus on reliability prediction, there is a need to understand the reliability life in the field, as well as the failure rate. Therefore, more reliability studies will be carried out in order to collect failure data and develop prediction models. The reliability assessment described in this dissertation will focus on the failure data collected and then, estimate the failure rate or reliability life under the use conditions.

1.2   Reliability considerations in semiconductor packages

1.2.1   Reliability concepts

The reliability of semiconductor packages is defined as the probability of a package to perform its function for a given time period, under specified conditions, without failures.

However, in industrial practices, the package reliability is usually judged by passing or failing required tests. The activities are usually limited to conducting stress tests and then attempting to identify and understand the failure mechanisms, if there are any failures. If necessary, changes are made to the packaging materials, assembly processes and package designs, in order to improve reliability performance.

1.2.2   Package failure categories

The package failures can be classified as solder joint failures and non-solder joint related failures. There are different ways to process the data from different failure cat-

egories. However, in field applications it is possible to analyze all of them with a similar approach.

Solder joint failures are often, worn-out fatigue failures and usually, these are associated with an increased failure rate. Various life prediction models for solder joint reliability are developed based on simulation or empirical data. However, there is a need to characterize those models, especially when there are new advancements in packaging materials, manufacturing processes and package designs. Additionally, the accuracy of the acceleration models for the life prediction of solder joints shall be validated.

Non-solder related package failures refer to failures not associated with solder joint failures. They account for the majority of the field failures but, are not well modeled. Table 1-1 lists results of studies concerning common field-return failures from company A, while Table 1-2 shows the failure percentage breakdown related to the packages. Indeed, the study shows solder joint fatigue failure is not one of the dominant failure model/mechanisms observed.

Table 1-1 Research data based on field-return failures from Company A between

2006 to 2007 (Yang et al., 2007)

Failure Mechanism Categories	Descriptions	# of Returns	% of Returns
Troubles not identified	No root causes identified.	3219	27.58%
ESD/EOS	Failures due to ESD and EOS failures.	2323	19.91%
Unsuccessful analysis	Cannot find out what is wrong and/or parts damaged.	1955	16.75%
Test (including software)	Failures due to insufficient test coverage or gaps in software.	1181	10.12%
Customer	Failures due to customer application set-ups or handlings.	1178	10.09%
Wafer	Failures related to wafer fabrication processes.	1092	9.36%
Assembly	Failures related to packages (reliability or quality, manufacturing etc.)	352	3.02%
Other failure mechanisms	Other than those identified	152	1.30%
Lab services	Failures due to lab analysis.	100	0.86%
Design	Failures due to product design issues.	53	0.45%
Distribution	Failures due to logistics issues.	38	0.33%
Customer services	Returns due to customer service errors.	24	0.21%
Product software	Failures due to product software application.	3	0.03%
Total returns = 11670			100%

Table 1-2 Package assembly related field-return failures [Yang et al., 2007]

Items	Failure Mechanisms	Description
Broken wires/bonds and lifted wires	32.2%	Failures seen at the second stitch bonds on the lead frame or substrates.
Die cracking	15.54%	Die chipping, passivation cracking or metal traces cracking in the die.
Delamination	12.71%	Any interface delamination, such as mold/die interface.
Die damage/wafer defects	12.15%	Die surface damage or scratch.
Package/substrate cracking	10.17%	Organic substrate cracks and solder mask cracks.
Others	17.23%	Other failures including solderability, foreign materials.

It should be reminded that the field failure data can be skewed, depending on the mainstream package types used by the companies.

1.2.3   Reliability assessment, prediction and failure rate modeling

One of the objectives of the reliability assessment is to understand the weakest links of the package and improve the reliability performance by eliminating the weakest links. The reliability studies will help with the collection of failure data in the accelerated stress tests to predict the time-to-failure, as well as the failure rates in the field based on the reliability models developed.

One of the difficulties in reliability prediction is the rarity of failure data from the stress-based approach. Instead of collecting the failure data, the intention is to pass the tests with zero failures. In order to validate or develop the models for reliability

11

prediction, a test-to-fail approach shall be adopted. The failure data observed in the stress tests will be required to understand the failure mechanism and predict the failure rate.

The reliability and failure rate models developed can be used to; (1) understand the life margin of the packages in the field application; and (2) predict the failure rate in the field. If necessary, the process will help reduce the failure returns in the field by screening out early failures. Reliability prediction and the modeling approach will help save time and reduce the cost of the package and production qualification process. .

1.3   Accelerated stress tests and acceleration factors (AF)

In accelerated stress tests, high stress stimuli are applied to a package to turn latent defects into observable failures within a short time period. The benefit of amplifying the occurrence of failures due to product deficiencies in accelerated stress testing is that product deficiencies become more apparent earlier in the process. However, the stress applied in these acceleration tests shall not introduce failure mechanisms which will not normally be seen in the field applications. In order to use the knowledge gained in accelerated stress testing, the failure mechanism shall be the same under both the stress conditions and the use conditions.

The common stress stimuli used in accelerated stress tests are listed below:

1. Elevated temperature. Testing a product for an extended period of time at an elevated temperature is probably the most common form of stress testing.

Marginal product designs often exhibit a temperature threshold beyond which the product will not function satisfactorily, and failure modes that involve chemical or diffusion processes can often be effectively accelerated at elevated temperature.

2. Temperature cycling. A number of interconnection and packaging failures modes are stimulated by temperature cycling. Faulty surface mount solder joints or weak interfaces, for example, tend to fail intermittently and will fail during temperature cycling.

3. Power cycling. Turning a product on and off is a common form of stress testing and is often done with or without other stress loads. The temperature transients that occur during power-up can stimulate thermo-mechanical defects, similar to the thermal cycling test. For semiconductor systems involving possible variable conditions resulting from an abrupt shutdown, on/off powering may also reveal design deficiencies associated with ill-defined start-up conditions. Power cycling can also detect certain failures which will not be detectable under thermal cycling test conditions, especially the thermal cycling tests without in-situ reading monitoring.

4. Voltage variations. Varying the voltage supplied to an semiconductor system can reveal design margin problems and marginal performance of specific components. It is often combined with testing at temperature limits to increase the detection of marginal conditions.

5. Vibration and mechanical shock. Vibration and mechanical shock stressing
   has traditionally been used to reveal structural support problems. In addition,
   problems with surface mount solder joints, has also increasingly been ad-
   dressed using vibration testing. Another form of mechanical impact tests is
   drop testing.

6. Elevated humidity. Elevated humidity testing is usually done in conjunction
   with high temperature testing to reveal problems with corrosion or high vol-
   tage isolation breakdown.

In general, the industry has adopted established test types and conditions defined in
JEDEC test standards [JEDEC, 2004]. Examples of the reliability test conditions are
shown in Table 1-3. During the reliability study, the test conditions and durations
can be selected based on the package material and use conditions. Table 1-4 demon-
strates the tests, the failure mechanisms detected by the tests, and the associated relia-
bility models.

Table 1-3 Standard stress tests used in semiconductor package studies

Test	Conditions	Target failure mechanisms
Preconditioning	JESD 22A 113	Cracking, delamination , interconnect damage failures
Unbiased and biased highly accelerated stress testing (HAST)	JESD22A118	Corrosion, delamination , contamination and migration , polymer aging failures
High temperature storage	JESD22A103	Diffusion, oxidation, degradation of materials properties, IMC, creep failures.
Temperature humidity bias (or no bias) (THB)	JESD22A101	Corrosion, contamination and migration failures
Temperature cycling (TC)	JESD22A104	Cracking, deamiantion, fatigue failures.
Power thermal cycling	JESDA105	Cracking and delamination, fatigue, material degradation failures
Mechanical shock (drop test)	JESD22B104	Cracking and delamination and fatigue, brittle fracture failures
Vibration	JESD22-B103B	Solder joint failures. Cracking and impact failures.
Bending (monotonic and cyclic)	JESD22B113; JS9702	Package, solder joint failures, cracking, and delamination.
Thermal shock (TS)	JESD22A106	Cracking, delamination and fatigue, brittle fracture failures
Autoclave (PCT)	JESD22A102	Corrosion, delamination and migration, interface contamination failures
Drop Test	JESD22-B111	Failures in the solder joints.
Cyclic Bending Test	JESD22-B114 and IPC/JEDEC 9702	Failures in the solder joints.
Board level SJR	IPC/JEDEC 9701	Thermo-mechanical solder joint failures.

Table 1-4 Stress tests and associated failure mechanisms and models

Test Types	Stress	Mechanisms	Accelerating Variables	Typical Models
Bake	high temperature	Diffusion; oxidation; dielectric breakdown; degradation of material properties; intermetallic formation; chemical reactions.	temperature	Arrhenius
Thermal cycle	Temperature range and max temperature.	Fatigue, delamination or brittle fracture.	Temperature range, temperature	Coffin-Manson or Norris – Landzberg
Thermal shock	Temperature range	Fatigue; delamination; brittle fracture	Temperature and time	Coffin-Manson or Norris – Landzberg
Power cycling	Temperature range, max temperature; profiles	Fatigue; generating large thermal gradients; thermal interface material pump out; material degradation; thermal solution wear-out	N/A	Coffin-Manson or Norris – Landzberg
Mechanical shock and vibration	Mechanical impacts	Fatigue; brittle fracture	NA	Coffin-Manson
Temperature and moisture (with or without bias)	High temperature, moisture	Corrosion; metal migration; dielectric material degradation; polymer aging	Temperature; humidity; voltage	Peck's or generalized Eyring

There is a misconception that test durations are usually fixed and that the purpose of

stress testing is to pass the test. In contrast, the knowledge-based package reliability

studies [Intel, 2000] [Sematech, 2000] focus on collecting failure data. The test dura-

tion for the qualification shall be determined based on the reliability life needs, the reliability models and use conditions. The failure data collected shall be used to predict the reliability life or failure rate for similar packages in the field application.

By definition, the acceleration factor for a given failure mechanism is the ratio of time or cycles it takes for a certain fraction of the population to fail, following the application of stresses or use conditions, to the corresponding time or cycles with more severe stresses or use conditions. The acceleration factor for a combination of stress factors can be the combination of AFs of the individual stress factor, as long as the same failure mechanisms are observed under the stress factors. It is clear that AF shall be associated with certain failure mechanisms. That is required in order to predict the reliability life and failure rate in the field condition, based on the failures observed in the accelerated stress tests.

1.4   Failure rate modeling

With a constant failure rate, the failures are not depend on time under the use conditions; those failures can be predicted by collecting the failure data from accelerated stress testing using random samples.

In industrial practice, the high temperature operating life (HTOL) test is usually applied during the qualification tests to estimate the failure rate in the field, with the assumption of expected failure mechanisms associated with temperature and voltage. Chi-square value, based on the number of failures observed from the stress tests, is used replace the number of failures observed. The acceleration factor models be-

17

tween the test conditions and the field application conditions are critical for the reliability life and failure rate estimation in the application conditions, as well.

When there are zero failures, the Chi-square value used in the failure rate estimation can still help estimate the failure rate. The hypotheses used in the failure rate estimation are:

(1) Field failures will be created by the operation voltage and temperature; nothing else.

(2) If there is no failure observed in the stress testing, then a Chi-square value of 5.99/2 can represent the upper bound of the expected number of failures. The failure rate can then be estimated using the value. Clearly, there are questions raised about the approach.

Moreover, field failures can be introduced by many stress factors besides temperature and voltage stresses. There are requests from the industry to provide a failure rate model to reflect the field applications.

1.5   Objectives, motivation and scope

This dissertation will assess the reliability performance of the packages, develop and validate the acceleration models used in reliability prediction, and establish the failure rate models. A proper approach for the component failure rate modeling will be proposed. In addition, the reliability performance and prediction for flip chip bump reliability under power cycling conditions will be presented. The results of the study

will help guide the test strategies and predict the life time and the failure rate of semi-conductor packages and assemblies in the field applications.

2. REVIEW OF FAILURE MECHANISMS IN SEMICON-

   DUCTOR PACKAGES

2.1   Introduction

A failure mechanism is described as a physical process resulting from the application of chemical, mechanical or electrical loads and leading to failures in semiconductor packages.

Failure mechanisms can be divided into two categories; overstress failures and wear-out failures. Overstress failures include structural overloads that might cause structural collapse, e.g. dielectric breakdown. Wear-out failures include failures which cause degradation in packages over time, e.g. solder joint fatigue failures. The failure mode is how the failure mechanism manifests itself. It is the symptom and not the root causes. A failure mode might be associated with many failure mechanisms.

Table 2-1 summarizes common known failure mechanisms observed in the semiconductor packages. The failure mechanisms are categorized into several key groups and while some are defect driven, others are simply overstressed or worn-out.

Table 2-1 Categories of failure mechanisms observed in semiconductor packages

Failure Mechanisms	Failure Mechanism Descriptions	Driving Forces	Notable References
Die cracking; thin film or dielectric cracking; passivation cracking.	Failures are shown to be open/short failures or functional failures. Failure mechanisms can be due to manufacturing defects, package design issues or materials used.	Temperature cycling; power cycling; moisture and temperature testing.	[Merrett et al., 1983]; [Shirley and Blish, 1987]; [Blish and Vaney, 1991]; [Zelenka, 1991];[Omi et al., 1991];[Hong, 1992];[Hu et al., 1995];];[Wu et al., 1995]; [Cory, 2000]; [Chou et al., 2001];[Nguyen et al., 2002];[Tsai et al., 2004]
Interface delamination	Delamination of any interfaces in the package structure. Interface delamination can happen at interfaces between the die and molding compound, the die and underfill materials, or between the metallization and dielectric materials in the silicon or in substrates.	Temperature cycling; power cycling; temperature and humidity testing; mechanical bending test.	[Doorselaer and Zeeuw, 1990]; [Gestel et al., 1992]; [Emerson et al., 1992]; [Nguyen, 1995]; [Amagi et al., 1995] ;[Tanaka et. al., 1999];[Aihara et al., 2001];[Harvey et al., 2001];[Davitt et al., 2001] ; [Chung et al., 2002]; [Lin et al., 2003];[Saitoh et al., 2003];[Wei et al., 2003];[Kwon et al., 2004];[Tsao et al., 2004]; [Kwon et al., 2005];[Braun et al., 2006] ; [Son et al., 2007]
Package cracking including substrate cracking, underfill cracking, solder mask cracking, mold compound cracking.	The cracks can be observed in the package body or internal "elements". Package cracking might be induced by interface delamination failures.	Temperature cycling; power cycles; temperature and humidity testing; mechanical bending.	[Zelenka, 1991]; [Amagai, 1995]; [Dias et al., 1997];[Ahn et al., 2000]; [lin, 2005]; [Cui, 2005];

Solder joint fatigue failures	Solder interconnects in semiconductor packages , e.g. solder bumps in flip chip packages or solder balls in BGAs or lead frame solder joints. The failure can be seen at the joint interfaces or in the bulk solders.	Temperature cycling; power cycling; vibration shock, other fatigue tests.	[Zelenka, 1991]; [Tu et al., 1997];[Ghaffarian, 2000];];[Davitt et al., 2001]; [Lau et al., 2001]; [Zeng and Tu, 2002]; [Choi et al., 2003]; [Pucha et al., 2004] ;[Suhling, 2004]; [Yoon et al., 2004]; [Wang et al., 2004];[Lau and Dauksher, 2005] ; [zeng et al., 2005]; [Birzer et al., 2006] ;[Braun et al., 2006]; [Pei et al., 2006]; [Davis et al., 2007];[Lee et al., 2007]
Wire bond failures, e.g.	Any failures related to the wire bonding such as IMC voids and cracks, lifting/broken bond/heel broken of stitch bonds.	High temperature storage (150 ^{o}C, 170 ^{o}C); power cycling and thermal cycling.	[Uebbing, 1981]; [Hund and Plunkett, 1988]; [Wu et al., 1995];[Cory, 2000]; [Park et al., 2004];
Corrosion failures	Failures associated with moisture and contaminants.	High temperature; temperature and humidity test;	[Striny and Schelling, 1981]; [Emerson et. al., 1992]; [Emerson et al., 1994];[Pecht and Dasgupta, 1996];[Tran et al., 2000];
Electromigration failures	Damages seen at interconnects in the silicon or solder bumps due to high current density, current crowding or high temperature applications	Current density; temperature	[Wu et al., 2004];[Balkan, 2004]; [Shao et al., 2004]; [Basaran et al., 2005];[Ding et al., 2005]

It shall be reminded that multiple failure mechanisms can happen to one type of package technologies. Typically, only a couple of them will be dominant. Examples of failure mechanisms observed in BGA packages under the same stress factors is shown in Table 2-2.

Table 2-2 Failure mechanisms possible seen in BGA packages

Failure Mechanisms	Root causes	Possible areas
Thermal mechanical stresses	CTE mismatch among different materials; temperature changes.	Flip chip joints, e.g. bumps
		Flip chip underfill interfaces.
		Die attach, mold compound, substrate interfaces.
		2nd level BGA solder joints
	Delamination and loss of adhesion at interfaces	Device to underfill to substrates
		Solder masks to substrate
		Overmold or glob top to device
		Heat spreader interfaces
	Metal circuit fatigue	Substrate metallization lines; PTHs and micro-vias
		Bonds, e.g. wire bonds
	Device cracking	die and passivation; ILD
Temperature and humidity failure mechanisms	Corrosion and loss of adhesion strength	die, bond pads, circuits, and bumps
		Dendrite, corrosion product growth
		Metal depletion into solution
		Oxide film growth
		Loss of interfacial adhesion
Thermal aging failure mechanisms	Material breakdown, interconnect degradation	Material oxidation
		Electrical and thermal degradation
		Intermetallic growth and degradation

2.2 Key failure mechanisms of semiconductor packages

Semiconductor packages have evolved for years in design, form factors, materials and manufacturing processes. However, not all of the developments improve the reliability performance of the packages. In contrast, many of them raise significant reliability challenges.

For example, low-k dielectric materials used in silicon devices are mechanically weak and post risks of dielectric cracking failures. Lead-free solder alloys require higher processing temperatures, which will affect the package reliability requirements as well. The selection of underfill materials will affect the solder bump failures and then, possibly, ILD cracking failures. New failure mechanisms will emerge with the new design and materials. The manufacturing processes for the new technologies will always raise defects and reliability issues.

Several key failure mechanisms observed in packages will be described in this section.

2.2.1   Wire bonding failures

Figure 2-1 shows an image of wire bond interconnects used in a lead frame based package. The close-up ball bond and wedge bond are shown in Figures 2-2 and 2-3. The diameter of Au bonding wires is approximately 0.8 mil for a pitch of 25-30 μ m. When a wire or a bond is subjected to repetitive stresses, it will eventually fail. For

example, thermal cycling stress will flex the wires and introduce the damages on the

wires and the area where the bonding process occurs.
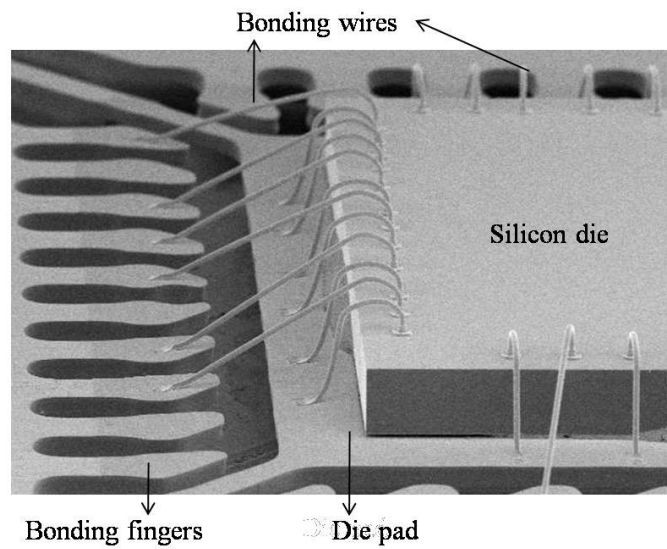
Figure 2-1 An image of wire bond interconnects [Yang, 2007]
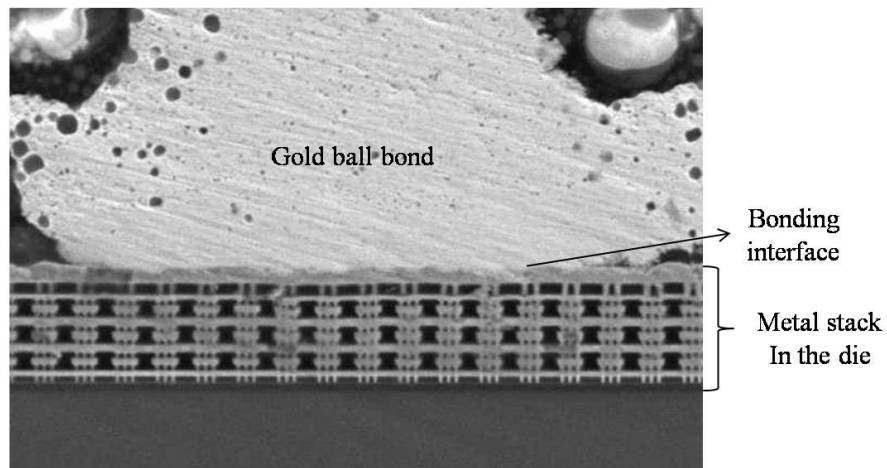
Figure 2-2 Ball bond in wire bonding [Yang, 2007]
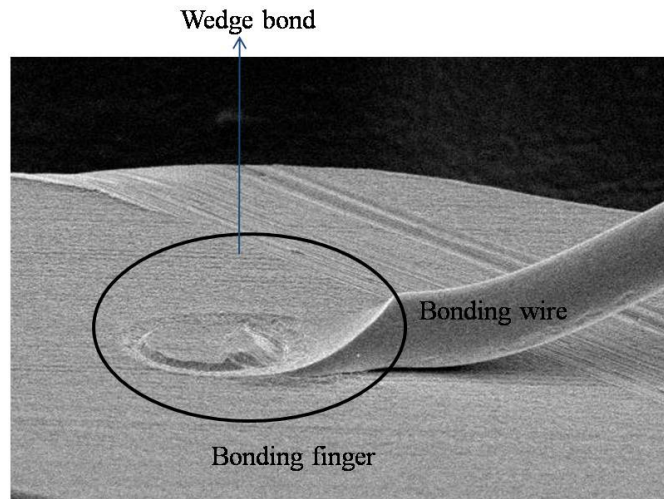
Figure 2-3Wedge bond in wire bonding [Yang, 2007]

The failure mechanisms associated with the wire bonding interconnects include broken bonds, lifting-off bonds, broken wires and heel fracture failures. A crack prorogation at the wedge bonding heel is shown in Figure 2-4, which can lead to an electrical open failures. The ball bond fracture is a result of either tensile or shear forces induced by thermal stress and will cause lift-off bond failure (as shown in Figure 2-5).

[Heleine et al., 1991] reports that the weakest link in wire interconnects is usually at the heel of the bond. [Uebbing, 1981] observes that the interface delamination between the molding compound and the die in the package will induce wire failures. The degradation of the bonding strength due to excessive intermetallic compound (IMC) formation is key to some of the wire bond failures. [Khan et al., 1988] reports that the presence of halogenated organic residues in the molding compound, will

cause increased gold-aluminum wire bond failures through the degradation of the intermetallic compound. [Park et al., 2004] shows that the lifetime of Au-Al bonding will be affected by contamination from other packaging materials, as well.
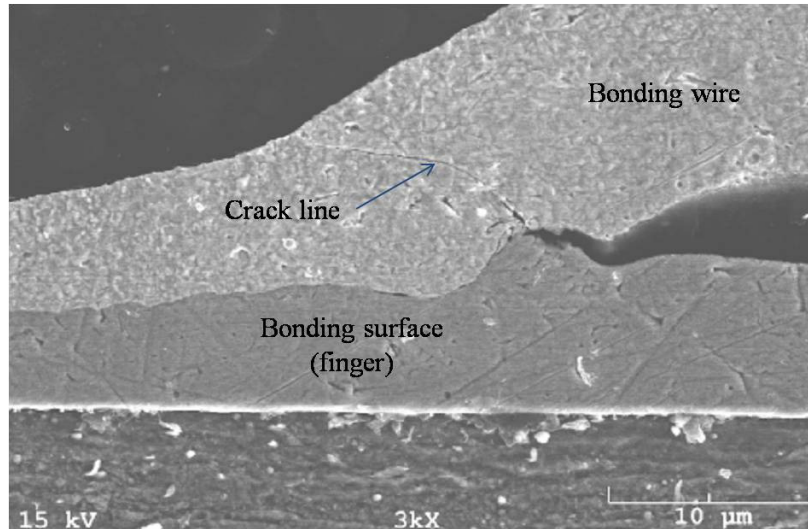
Figure 2-4 Wedge bonding failure (fracture failure seen in the heel) [Yang, 2007]
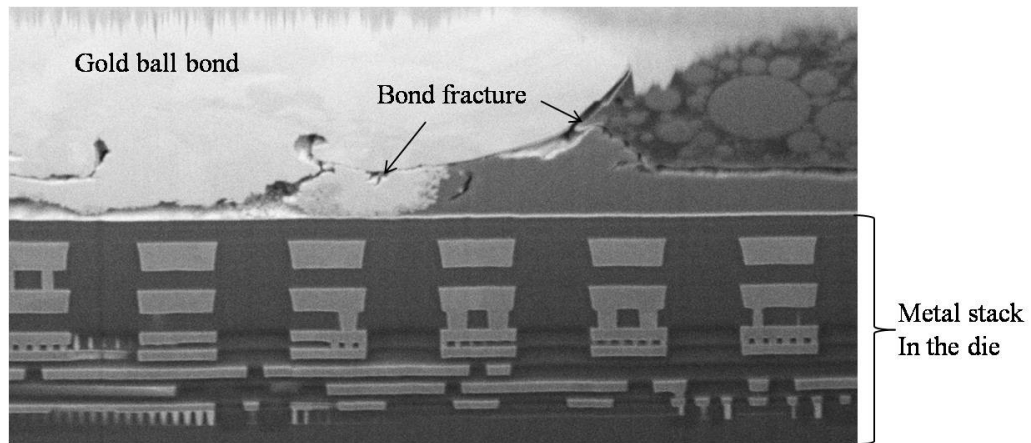
Figure 2-5 Ball bond interface cracking (failure at TC 1000 cycles) [Yang, 2007]

2.2.2 Die cracking failures (e.g. passivation cracking, ILD cracking)

Die cracking failures are commonly reported failure mechanisms in packages. A high percentage of die cracking failures is due to the defects in the silicon, coupled with the high stresses generated during the application or testing. The defects, usually introduced during wafer manufacturing, wafer back grinding and wafer sawing, can act as starting points for die cracking failures. [Chou, 2001] discusses silicon design and layout schemes such as the metal densities, the passivation and low-k materials used will aggregate the cracking risks. The pre-existing cracks can cause a catastrophic event. For example, micro-cracks at the die top surface can propagate vertically to cause active circuit damages. Edge cracks induced from the wafer sawing process are most likely to propagate at the corners of the die or arrive at inner layer dielectric or thin film layers inside the silicon.

The die-attach fillet height or the underfill fillet height will generate high stresses, which will cause die cracking failures under thermal cycling conditions. The package material selection will contribute to the die cracking failures as well. [Michaelides and Sitaraman, 1999] emphasize that the underfill materials do transfer the thermal stress from the solder bumps to the chip, substrates and other components in the packages. Die cracking (including metal deformation and ILD cracking) failures are also associated with the encapsulation and underfill materials and silicon technologies used. For example, high Tg underfill materials in flip chip assembly will cause low-k die cracking failures, due to their higher modulus and high warpage generation. In

contrast, a low Tg underfill material will have lower modulus and will thereby, re-

duce the risks for die cracking failures.

Figures 2-6 depicts a die cracking failure observed in the die surface. Figures 2-7 and

2-8 show low-k dielectric cracking in the silicon.
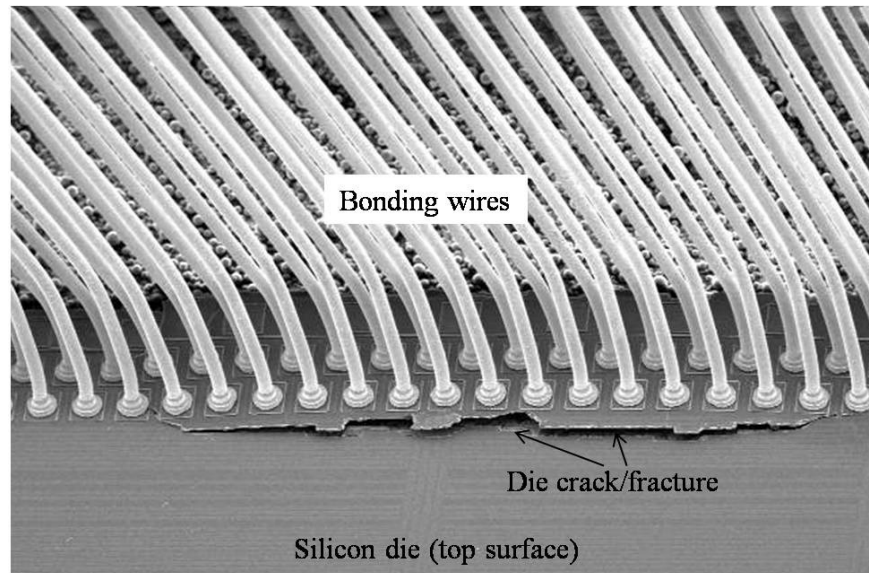
Figure 2-6 die cracking failure seen at the die surface [Yang & Bernstein, 2008]
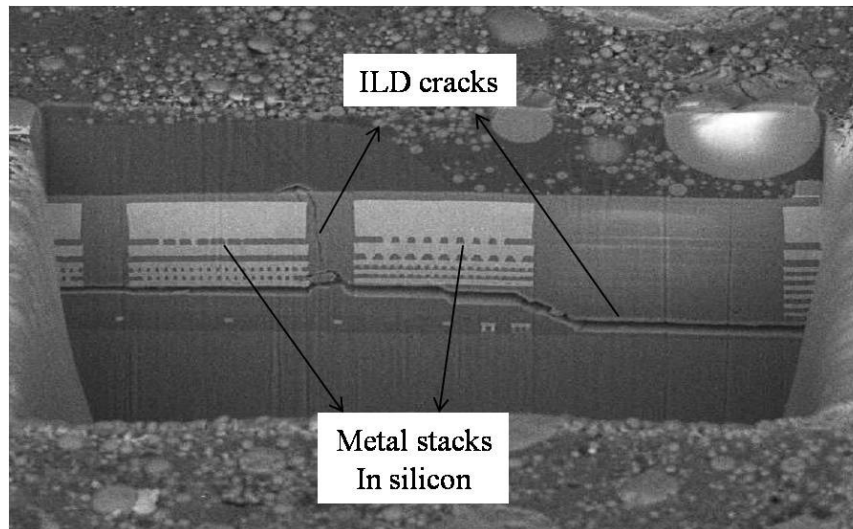
Figure 2-7 Inner layer dielectric and thin film cracking failure [Yang & Bernstein, 2008]
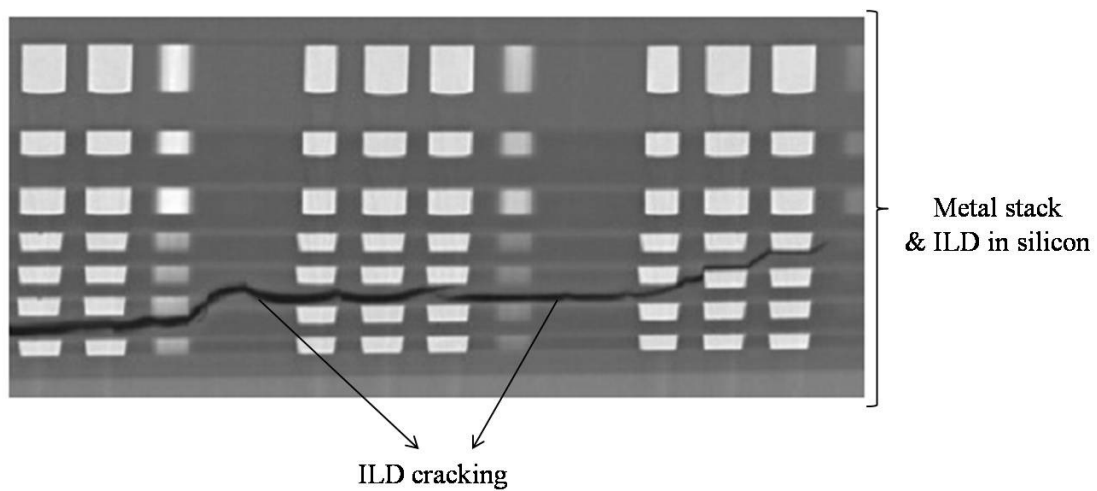
Figure 2-8A close-up view of low-k dielectric cracking [Yang, 2007]

[Merrett et al., 1983; Marcyk and Kudva, 1989] mention localized passivation tracks on the die, which are associated with passivation defects from the wafer manufactur-

ing process and are the primary reason for early product failures. In this case, optimization of die thinning and die polishing processes is recommended, in order to reduce the chance of die cracking. [Kessel et al., 1984] emphasizes that an un-optimized die attach process can introduce die cracking failures. [Yang and Bernstein, 2008] describe the die-edge defects induced during the wafer sawing process, as one of the reasons for product early failures. [Amagai et al., 1995] finds chip backside contamination is found to be a primary driving force for cracking/ interface delamination failures after 85 ^{o}C/85%RH testing. In addition, the height of die attach fillets significantly influences the stresses on the die edge and is found to help extend initial cracks at the edges of the silicon. [Hu, 1995] provides a good tolerance of defects by limiting the board thickness to less than twice of the die, in order to prevent die cracking failures.

Hydrostatic stress is known to be the driving force for stress voiding and the Von Mises stress is the force for plastic deformation. The voiding influences the occurrence of cracking, however, the cracking does not influence stresses induced voiding failure. If the void growth occurs close to the potential crack failure area, the probability for crack nucleation will be increased. Voiding changes stresses in all directions, especially inside the potential crack nucleation area, whereas crack propagation due to a planar like shape does not relax in potential void location [Orain et al., 2006]. Temperature cycling will accelerate the interlayer dielectric cracking failures. [Nguyen et al., 2002] describes the thin film cracking as due to the thermal expansion mismatch between silicon substrates and thin films under the loads of fast tempera-

ture cycling. [Syndergaard and Young, 1994] observe metallization cracks near the die corner under the temperature cycling testing. The damages start to occur when the plastic starts to delaminate from the surface of the die. [Tsai, 2004] concludes that cracks initiated at the edges, from bending stresses on the die are due to CTE mismatch between the die and the substrates, can cause the die cracking failures. In addition, increasing substrate thickness and /or reducing die thickness, is one of the most effective approaches to prevent die from cracking [Han, 2001].

2.2.3 Package cracking failures

Package cracking failures include the fracture failures in the package body, excluding the die and the solder joints. The failures can be introduced from stresses generated during the package assembly processes, from a defect in the substrates, from the packaging materials used, and from application conditions. The thermal mismatch of packaging materials can be large enough to make the interfaces package susceptible to the cracking. The cracks can start at various interfaces, including die top surface and molding compound interfaces and die attach/lead frame or substrate interfaces, including interfacial layers in the substrates. The cracked package is susceptible to corrosion and contamination failures from the migration of external ions along the surface of cracks, which are also the direct cause of package and product failure. In many cases, the package cracking is closely associated with interface delamination failures.

Figure 2-9 demonstrates a package cracking failure after temperature cycling tests. The delamination will generate stress at the die corner and initiate the crack at that corner. The picture on the left shows a CSAM image picking up the die corner failure, while the FIB picture on the right shows the thin film delamination and the package cracking at the corner. Figure 2-10 shows a typical molding cracking failure in the package.
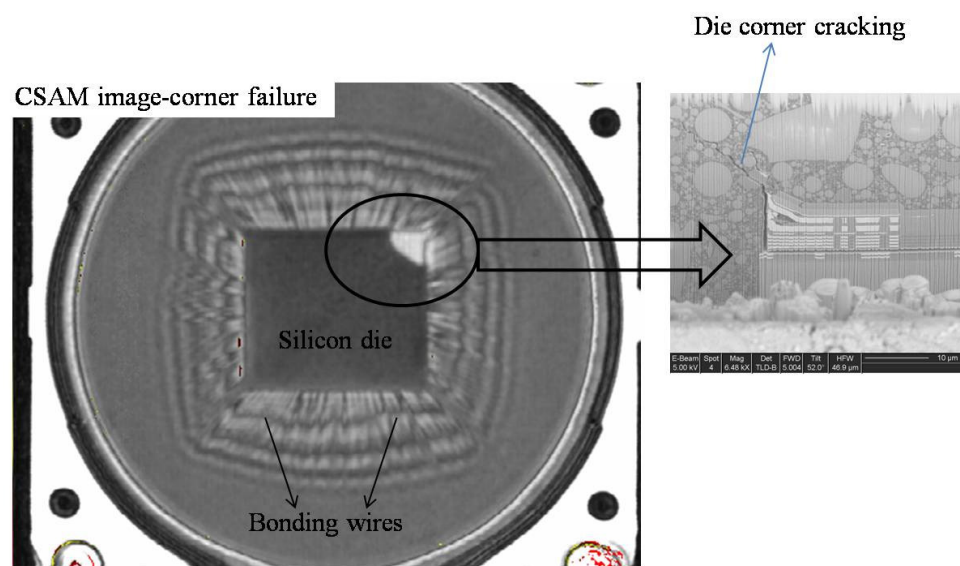
Figure 2-9 Package cracking failure after TC 600 cycles (die corner delamination)

[Yang, 2007]
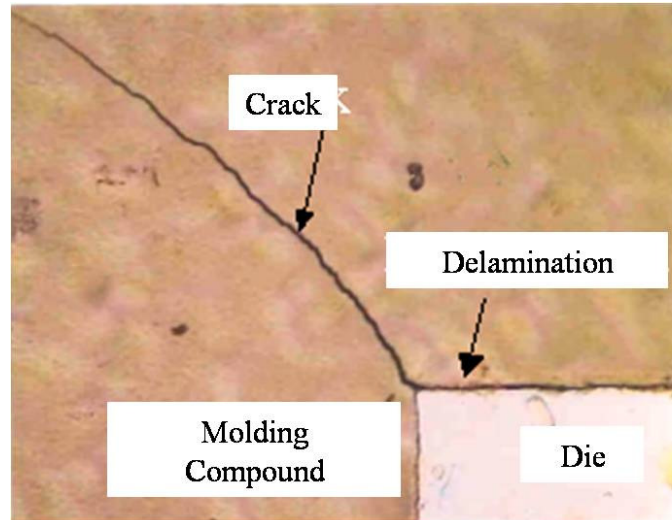
Figure 2-10 Package cracking (molding cound cracking) [Yang, 2007]

[Azimi, 1997] observes that package cracks most often originate under the die, near the corners of traces and under solder bump pads on the C4 side of the OLGA package. [Dias et al., 1997] reports metal line breaks due to cracks in the flip chip organic substrates layers under the temperature cycling test. [Saitoh et al., 2003] reports package resin cracking, induced by the interface delamination at the interface of the die pad. The cracking direction tends to become perpendicular to the bottom surface of the package as the interface delamination extends. [Ray et al., 2003] describes that the cracks in the resin layers can propagated to damage the traces underneath the BC4 layers of FCBGAs.

The curing of the mold compound is one of the most stringent processes for the reliability of the packages. The large stresses initiated from the bottom corner of the pad, with a max distance from the neutral point (DNP), drive the cracks to propagate to-

ward the middle of the substrate. The high stress is induced by high CTE mismatch and cure shrinkage of the molding compound.

Cracks in most materials tend to be tensile driven and the high tensile stress will lead to fracturing in areas of high stress concentration. Reducing the stress concentration points and improving the interface adhesion will help prevent cracking failures, as will process and design modifications.

2.2.4 Interface delamination failures

Because package structures involve many interfaces, interface delamination failures are always one of the primary failure mechanisms observed. Interface delamination failures can be described as the separation of any interfaces in the packages, due to loss of interface adhesion strength, voids and other damage to interface structures. Interface delamination failures can elevate package cracking, as well as die cracking and wire bonding failures [Chee et al., 2006; Doorselaer, 1990; Saitoh et al., 1997; Kwon et al, 2004].

There are many driving forces that cause interface delamination failure including moisture, hydro-thermo-mechanical stresses and tensile stress loads. High temperature, higher thermal mismatch and higher shear forces at the interface, combined with a loss of interface adhesion strength, all lead to an increased delamination rate. With the adoption of low-k dielectrics, the interface delamination failure has become a major reliability concern. Figure 2-11 shows an example of delamination failure between the molding compound and the substrate surface in a BGA package. The sepa-

ration interface is between the die attach adhesives and the substrate. Figure 2-12

shows the delamination at the thin film interfaces inside the silicon. The delamina-

tion interface is at the layers of metal 1, in the silicon metallization stack-ups.
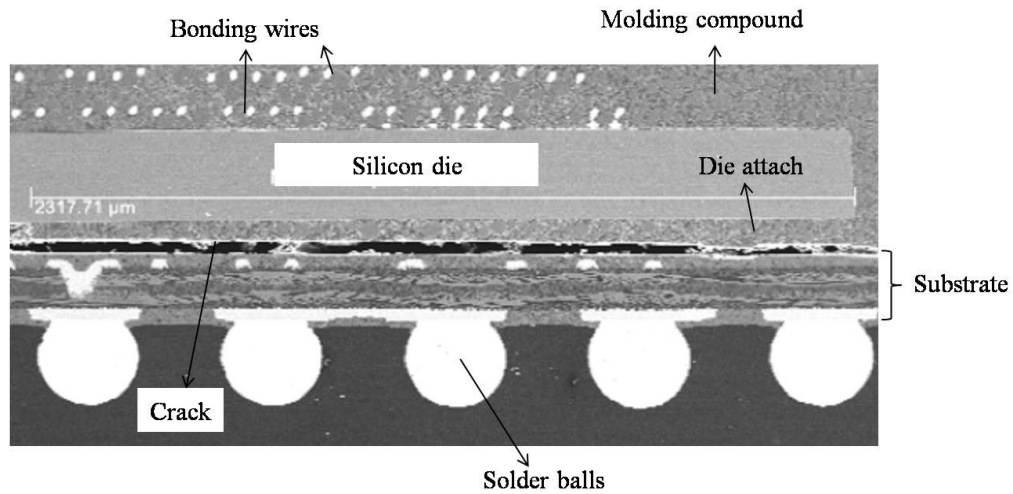
Figure 2-11 An example of a interface delamination failure seen in the package[Yang,

2007]
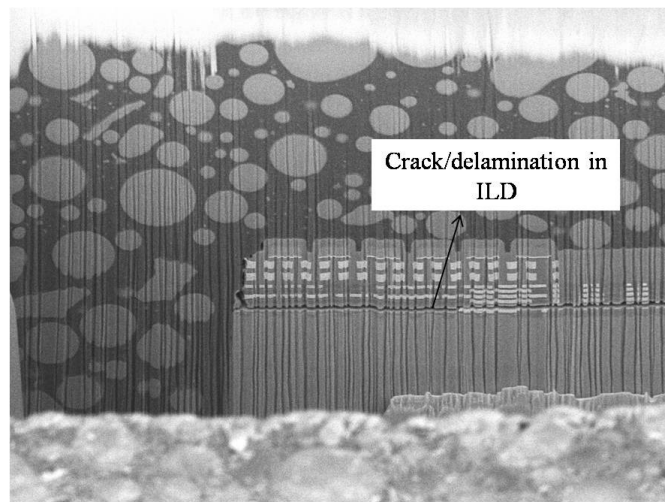
Figure 2-12 Delamination at ILD after moisture sensitivity tests [Yang, 2007]

Moisture and temperature conditions strongly influence interfacial adhesion. [Merrett et al., 1983] reports that the dependence of interface delamination failures on the relative humidity (RH) and temperature. [Ferguson & Qu, 2002; Aihara et al., 2001] mention that the resistance to delamination and subsequent cracking failures will be improved by lowering moisture absorption and improving interface adhesion. [Chung et al., 2002] indicates that a compound system with higher moisture uptake will result in poor reliability. [Tanaka et al., 1999] describes that the change in delamination-occurrence temperature in the package is corresponded to the change in the true adhesion strength due to the moisture absorption, so do the residual stress and the stress intensity factor. [Li et al., 2007] describes that delamination in the dielectric film stacks is associated with the moisture absorbed which will weaken the chemical bonds within the dielectric film and reduce the interfacial strength and the hygroscopic stresses.

[Braun et al., 2006] finds that temperature cycles conditions with higher upper and delta temperatures lead to an increased area of the interface delaminated for the flip chip packages at the chip/underfill interface, and introduce the cracking of solder bumps and electrical failures. Larger thermal stresses at the die surface for the lead-free solder package is observed, as compared with the high lead and leaded eutectic solder package. [Kwon et al., 2005] discovers that underfill materials with high CTE and low modulus, exhibit significant interface delamination failures, which initiate at the edge of silicon die under thermal cycling conditions. [Chen et al., 2006] reports delamination

37

failures, caused by poor interface adhesion and high low-k shear stress on a multi-layer Cu silicon of a build-up substrate structure. Underfill materials can dramatically affect the interface delamination. Low-k cracking is found to be associated with underfill materials. [Wang et al., 2005] proves that increasing the CTE of the underfill materials enhances the thermal mismatch between the underfill and solder bumps however, it also increases the crack driving force for low-k interfacial delamination under the critical solder bumps. [Zhai et al., 2006] showed in his study that the presence of the underfill fillet formed at the die periphery plays an important role in the delamination at the die corner or the die edge.

[Tsao et al., 2004] presents the results that a molding compound with the right CTE and modulus combination can help eliminate the delamination failures for the low-k ILD failing at the chip corners. The metal peeling found at the die edge is the initial point of delamination. The lower modulus of low-k dielectrics will result in a higher crack driving force. The corner delamination is less sensitive to the modulus of the ILD materials, than the near-bump delamination.

[Lin et al., 2003] finds the die attach voids make it easier to introduce the delamination initiation at the edge of the die attach paste, due to a high stress concentration and low adhesion strength. However, the delamination failures can be controlled by reducing the die-attach voids and enhancing the interface adhesion strength [Lin et al., 2003]. [Lee et al., 2007] reports a tall die attach fillet height is sighted in the region of delamination between metal 1 and via 1 in the low-k die layers under thermal cycling.

[Wang et al., 2004] describes the interfacial delamination failures of low-k structures as associated with increasing die size in a package. Packaging effects are varied when different low-k materials are used, as the high modulus of low-k materials is less dependent on the packaging materials.

Figures 2-13 shows additional interface delamination failures observed in the flip chip packages.
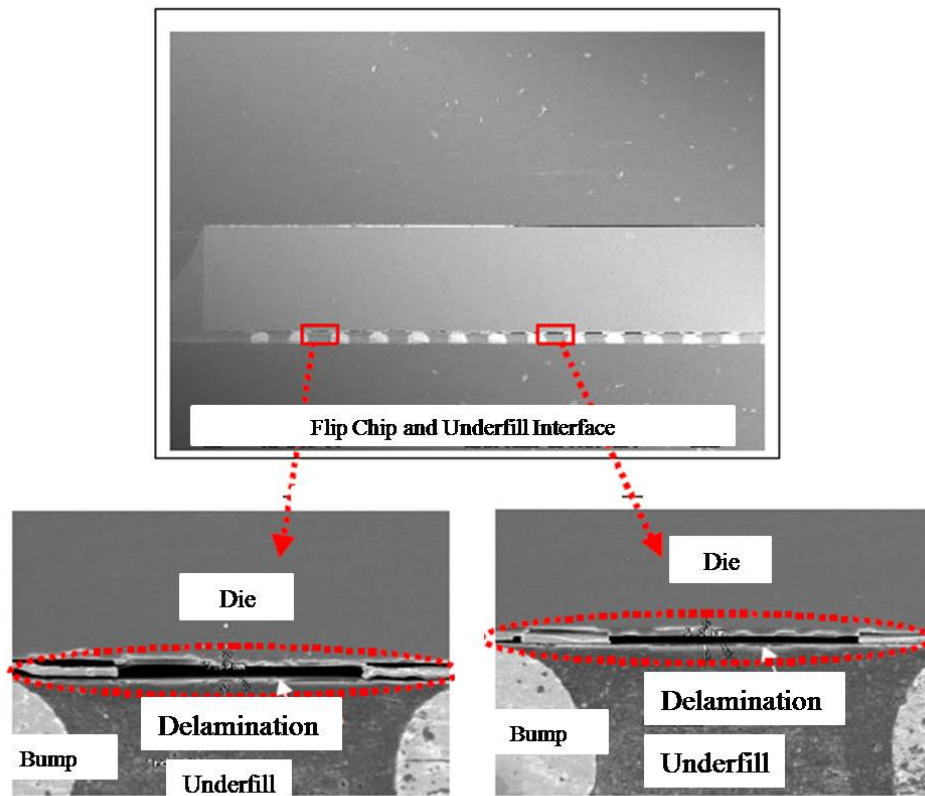
Figure 2-13 Delamination between the underfill and the die after 100 hours HAST [Freescale, 2008]

2.2.5 Solder interconnect failures

Solder connections are everywhere in semiconductor packages and assemblies. Solder interconnects are typically formed by tin-lead solder alloys, with or without small additives such as Cu, Ag or In between the die and substrates or between the substrates and PCBs. Figure 2-14 shows the solder bump connections at flip chip level and the BGA joints at the second level of interconnections.
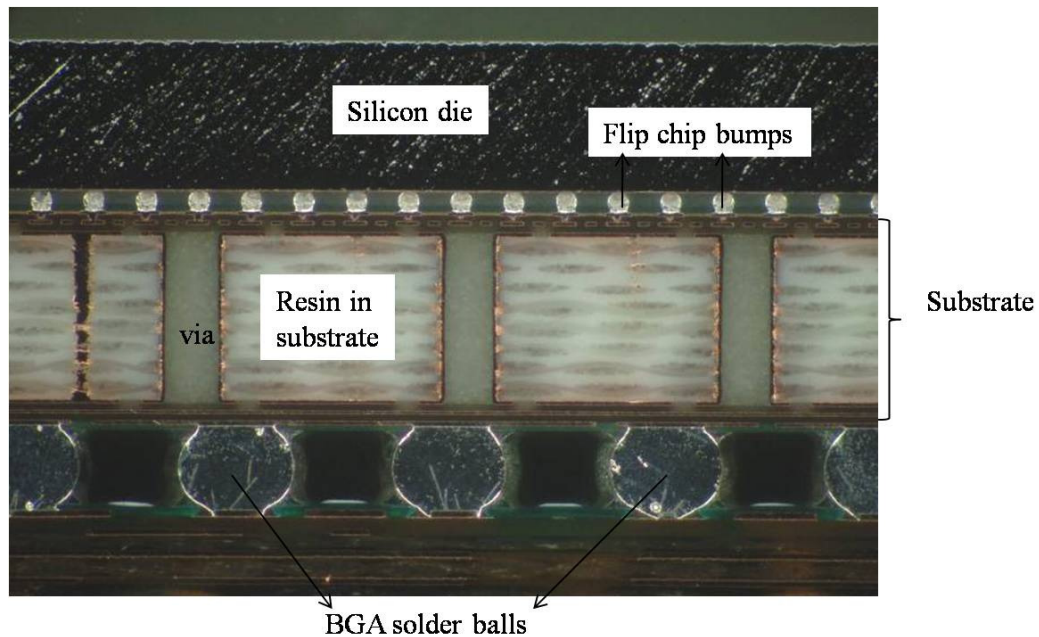
Figure 2-14 Solder interconnections in semiconductor packages [Prismark, 2007]

The stress and strain in the solder joint are a result of the global mismatch of the coefficient of thermal expansion (CTE) between package and substrates and the total CTE mismatch between solder and copper pads/leads. The thermal mismatch during thermal cycling causes fatigue failures in solder joints.

The thermal fatigue performance of solder joints will depend on a number of parameters related to solder materials, pad surface finishes, interface compound thickness and microstructures, the geometry of the solder joints, key design rules, and the manufacturing e.g., cooling rate or ramp rate during reflowing process. [Qi et al., 2004] reports that solder joints with the highest cooling rate showed the worst reliability in fatigue life for lead-free solders. Besides the thermal-mechanical fatigue failures, the mechanical impact on the solder joint becomes a major issue for the semiconductor industry, due to the ever increasing popularity of portable electronics and the transition to lead-free solders. Figure 2-15 shows a solder bump failure structure and Figure 2-16 shows a solder ball connection failure.
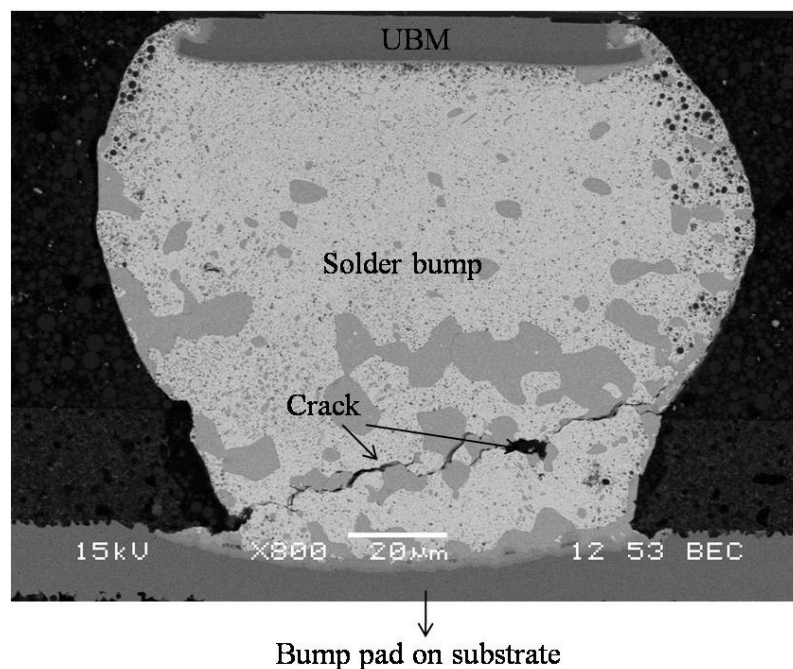
Figure 2-15 A bump cracking failure

41
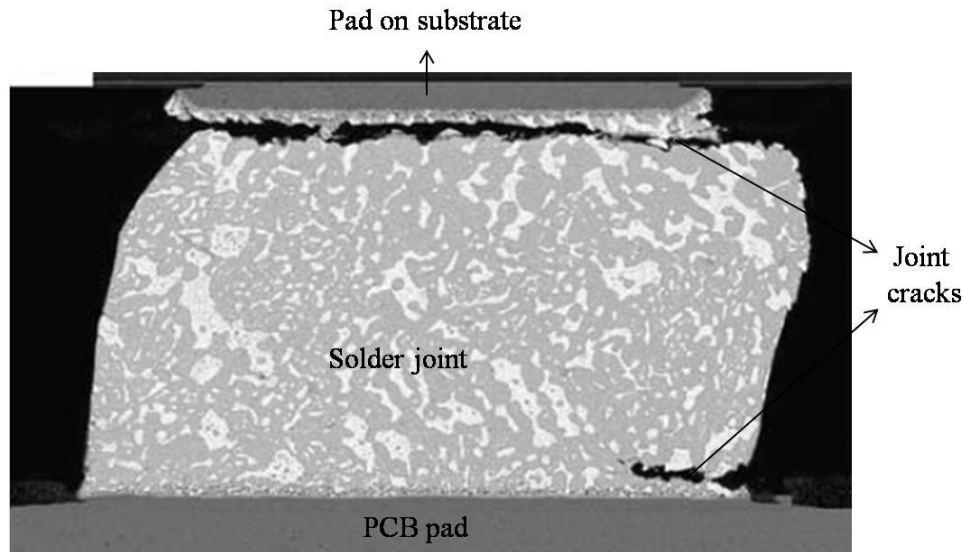
Figure 2-16 A second level solder joint failure [Freescale, 2004]

[Chan et al., 1997; Tu et al., 1997; Gupta, 2004; Kim et al., 2005] observe that the solder cracks formed during cycling testing, were initiated and propagated along the IMC and solder joint interface. Thicker intermetallic layers in the joint will result in shorter fatigue lifetime. It is obvious that the presence of an IMC layer will help initiate cracks and affect the fatigue lifetime of solder joints. A thicker IMC layer will also provide void sites for crack initiation and paths of the cracks. However, [Arulvannan and Chong, 2006] indicate that IMC thickness under control can have no impact on the reliability of the solder joints. In addition, the peak reflow temperature has little impact on solder joint life. Rather, intermetallic layer thickness is sensitive to the reflow profiles employed.

[Chen et al., 2007] reports that smaller solder mask openings, when compared to a larger solder mask opening design, can change the thermal fatigue failure site, from the package size to the board side. [Lin et al., 2002] reports that under a high cycle vibration load, the BGA solder joint cracks always start at the inner corner of the component side, while secondary cracks always start at the outer corner of the joint and show up at the solder/Ni interface at component sides. The delamination between the solder mask and solder joint gives impetus to the development of the cracking. [Adamson, 2000] presents that the number of cycles to failures drops significantly as the package size increases. In addition, large ball sizes or solder joints with a higher aspect ratio, survive a large number of thermal cycles. [Toisishiraporn et al., 2007] reports that solder joint failures are related to the location of the joints on substrates or on the PCBs. The sacrificed solder joints (redundant interconnections placed in the vicinity of high stress areas) will accelerate stress in material and cause early failure of the live solder joints. When the corner solder joints are removed, the reliability of the package is increased. [Li et al., 2009] discloses that diagonal solder interconnections beneath the die edge, are the most critical. Both thermal shock and power cycling will accelerate the same failure mechanisms, but power cycling has an absolute fatigue life that is 2-3 times longer than that of thermal shock.

[Xia et al., 2007] describes research results showing that assemblies with OSP finishes outperform their ENIG counterparts under temperature cycling conditions. However, under drop tests, ENIG assemblies reveal better reliability performance, than those with OSP finishes. Under drop test, solder joint fractures in the IMC layer in-

itiate in the bulk solder and under temperature cycling, initiate near the interface. In

the case of the ENIG, the propagation of crack is along the device/solder interface,

while in the case of OSP, the crack extends parallel to the solder /PWB interfaces.

When two levels of solder joints are available, as seen in flip chip packages, a tra-

deoff between the reliability of the 1st and 2nd level interconnects is moderated by the

thermo-mechanical properties of the underfill material. Interface adhesion is the rele-

vant parameter determining the solder bump life. In addition, assembly warpage is a

potentially limiting reliability design factor. The considerations of the underfill prop-

erties are listed in Table 2-3.

Table 2-3 Critical properties for underfill materials

Property	Preferred direction	Comments
CTE	Generally matching the solder bump	Mismatch to the solder CTE will impose axial strains during cyclic stress
Tg	Generally higher is better	While higher Tg generally improved thermo-mechanical stability, however, it also tends to impose a higher warpage strain.
E (modulus)	Generally lower is better	Higher modulus improves mechanical coupling between chip and carrier, it will also tend to impose a higher warpage strain and cause low-k cracking.
Adhesion	Higher is better	Adhesion fracture toughness of both chip to underfill and underfill to carrier need to be high.

With more and more components classified for portable applications, dynamic loads

will have a significant effect on the fatigue life of solder connects. The cracks in-

duced by vibration fatigue are created in metal compound layers or nearby solder ma-

terial. [H. Wang et al., 2004] observes the solder joints' fatigue life in mechanical load is connected with the mass of the chips, the stiffness of the chips and the shape and number of solder joints. Under drop impact conditions, [Jang et al., 2007] reports that while intermetallic thickness, itself, is not a critical factor, it can affect adhesion, due to the different solder reaction rates.

Reliability performance and failure mechanisms of lead-free package, under temperature cycling conditions and drop testing loads show different failure trends than leaded counter parts. [Cavasin et al., 2007] observes that the board level performance of eutectic Sn-Ag(Sn-3.5Ag) solder under thermal cycling conditions is better than that of eutectic SnPb solder.

[Chen et al., 2007] reports that SAC305 solder alloys are found to have the best durability during the cyclic bend test, while the SnPb solder is the strongest during monotonic bend tests. [Wang et al., 2007] observes that the high-cycle fatigue performance of the SAC solder system under vibration loading is much better than the SnPb solder system. [Pandher et al., 2007] shows a negative effect of a Bi addition to SAC 305 and SAC205, in terms of drop test performance. A combination of Ni and Cr offers high drop shock reliability and excellent tarnish resistance. The best combination of properties is demonstrated for modified SAC105 with 0.05%Ni +0.03%Cr. [Mattila et al., 2007] concludes that the drop reliability decreases with increasing temperature, and that the joints on a Cu/OSP PWB finish are more reliable than those on NiAu surface. In addition, at elevated temperature, SAC solder alloys are is the most reliable alloys. [Kim et al., 2007] performed a detailed study to compare the performance of

various SAC alloys. The results show SAC 105 alloy performs better under drop load, as compared to SAC405 alloys. However, the failure modes are different. For SAC 405, the majority of the failures occur through IMC layer and minor failures occur at bulk solder. For SAC105 solders, cracks propagate through bulk solder more often than through a brittle IMC layer.

Regarding solder joint reliability performance, both board and package interface cracking failures can be observed with increasing number of cycles. Failure mechanism differences can be explained either by global or local stress conditions.

2.2.6 Electromigration failures

Electromigration is an open-circuit failure mechanism precipitated by metal transports in an interconnection metallurgy. The electro-transport rate increases as the current density increases. Traditionally, electromigration is a very low risk failure mechanism for semiconductor packages due to the large dimension scale involved, as compared to metallization in silicon technology.   However, with the current requirement for high performance devices and small form factor packages dimensions of interconnects in packages are becoming smaller and power and current density are increasing. As a result, there is a high potential for electromigration failures in solder bumps.

Another immerging failure mechanism associated with electromigration is thermo-migration, which is thought to be a more benign mechanism, much rarer than electromigration. Thermo-migration coupled with electromigration failures will cause

serious reliability issues. Whenever the direction of thermo-migration and the elec-

tromigration are the same, the damages will be very severe. When the direction of

the thermo-migration and electromigration are opposite, less damage will occur.

For the package level electromigration study, special test structures are usually de-

signed to generate electromigration stress failures. Figure 2-17 shows a test structure

consisting of a flip chip solder bump and high density interconnect (HDI) boards,

containing at least one sense bump and stress bump in the circuit.

Figure 2-18 shows the degradation of the solder bumps/joints under electromigration.

Depending on the direction of the current flow, cracks formed due to electromigration

can be observed on different interfaces.
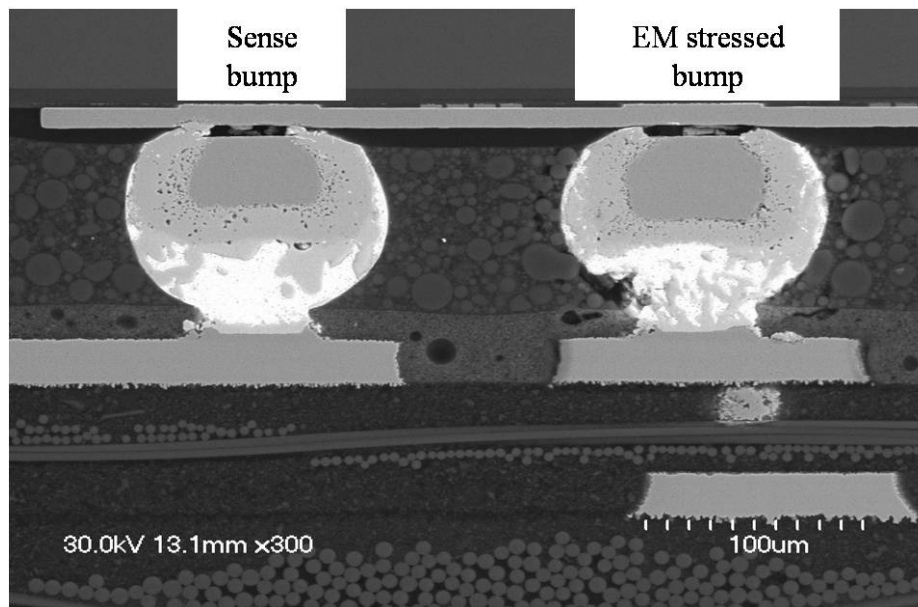
Figure 2-17 Bump structures under electromigration testing [Gajewski, 2006]
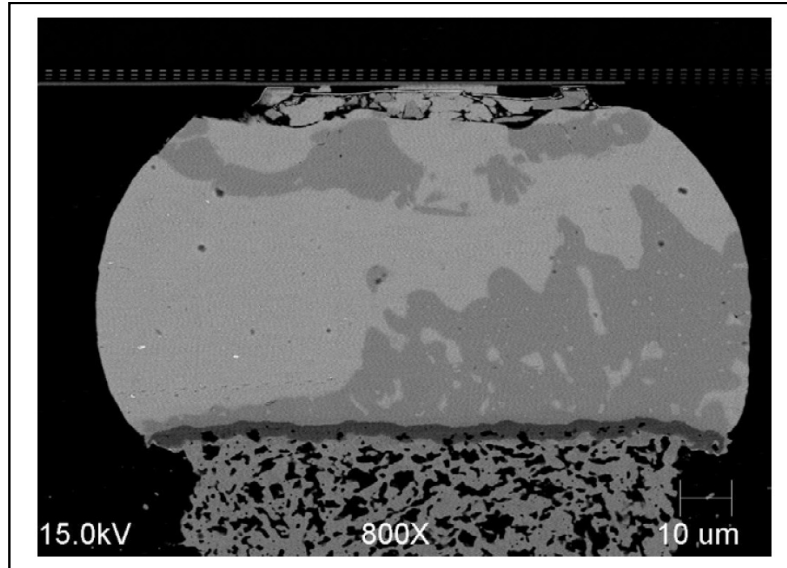
Figure 2-18 Solder joint cracking due to electromigration [Su et al., 2005]

[Basaran et al., 2005] studies the void nucleation and growth in solder joint interfaces during current stressing. The Ni UBM –solder joint interface is the preferred site of void nucleation and growth. The contaminants in the interface help accelerate the void nucleation process. The structural damage at the region of UBM and UBM/bump interfaces is shown in the form of solder cracking or delamination.

Two key factors to note when observing the electromigration behaviors of flip ship packages are the current crowding and Joule heating. Damages that initiate in the bump fracture or solder voiding at solder/UBM interface are a result of a current crowding, which is also the primary failure mechanism of flip chip interconnects. Bump temperature has more significant influence on bump failures than current density. [Lee et al., 2007] confirms that very high current density conditions lead to severe Joule heating evolution inside the flip chip solder bumps.

[Wu et al., 2004; Wu et al., 2006; Ha et al., 2009] demonstrate that Sn5Pb95 solder bumps are observed to have higher failure resistance than eutectic Sn63Pb37. SAC solder alloys have higher resistance to failures, as compared to eutectic solder alloys. Pb is found to be the dominant diffusion species and migrates along the electron flow. Cu doped SnPb bumps show an improved electromigration resistance over eutectic SnPb interconnects.

[Ding et al., 2005] studied the impact of UBM structures on the electromigration. He finds that Ni-UBM has more resistance to EM failures than Cu-UBM. The Cu UBMs' failure mechanism is temperature dependent. At high temperature, the Cu UBM dissolves continuously, while at low temperature, open failures are caused by a crack formation at the Cu_3Sn/Cu_6Sn_5 interface, with little damage to the UBM. The electromigration life of Pb-free solder is found to be much better than that of the eutectic solder, but worse than that of the high lead solder at the same temperature. Also, [Kwon and Paik, 2007; Wu et al., 2004; Nah et al., 2007] show that Ni-P UBM thickness is effective to enhance electromigration reliability; a thicker UBM layer will delay an EM failure and prolong the MTTF. The failure mechanism is described as the formation of IMC layers (Cu_6Sn_5) with increased current stressing, and the dissolution of Cu_6Sn_5 IMC into the solder region under increased current stressing.

[Shao et al., 2004] finds that electromigration failures on anode/chip side and large $(Cu/Ni)_6Sn_5$ IMC are mostly observed on the interface of the UBM and the solder bump. Nickel atoms are migrated by a electron flow from the substrate side to the chip side to form the $(Cu, Ni)_6Sn_5$ IMCs. [Jen et al., 2009] studies the void formation

49

of the lead free solder bump connections in flip chip packages under current crowding and high temperature environments. The voids, which are due to current crowding, initiate at the corner and are located at the interfaces of UBM/IMC and IMC/solder interfaces. All failures are attributed to the propagation of voids along those interfaces at the cathode chip side of bumps with downward electron flow. [Lai and Chiu, 2007] report that the solder joint with a greater Cu weight has a longer electromigration life under low current stressing with Ti/Ni(V)/Cu UBM structures.

2.2.7 Corrosion failures

Corrosion failures can be defined as the reaction of a metallic material with its environment; the process of chemical or electrochemical degradation of metallic interconnects. The rate of corrosion depends on the component materials, the availability of an electrolyte, and concentration of the ionic, the geometry, the environmental conditions and the local electric field.

For semiconductor packages, corrosion failures occur when the devices are in the presence of moisture and contaminants. Bond pad corrosion is most common when the die passivation does not cover the metallization in the bond pad locations, while internal corrosion is attributed to weakness or damage in the die passivation, permitting moisture to reach the metallization.

Three industry standard tests are used to accelerate corrosion failure mechanisms, including 85 ^{o}C/85%RH (TB), autoclave (PCT) (120 ^{o}C/100%RH) and HAST (130 ^{o}C/85%RH).

50

[McGarvey, 1979] reveals that process defects are one of the key reasons that failures occur under corrosive environment. [Gestel et al., 1992] reports the adhesion between die surface and mold tends to diminish in environments with higher temperature and humidity. Moisture which penetrates in the interconnection layers of the delaminated area causes corrosion on the pads. As a result, bond pad corrosion failures and bond lift failures are observed under HAST test conditions. [Emerson et al., 1992; Tran et al., 2000] report that passivation materials are critical for the prevention of HAST corrosion failures. [Tan, C.W., et al, 2002] observes stress corrosion cracking failures at the interface of Cu-Al under PCT test conditions.

2.3 Summary

In this section, several key categories of failure mechanisms observed in semiconductor packages are discussed. The failure mechanisms are not independent; they might interact with each other or be introduced by one another. For example, interface delamination failures can introduce die or package cracks failures. In addition, failure mechanisms can be induced by the same stress stimulus.

As mentioned previously, some failure mechanisms occur in accelerating stress conditions, which might not show up under use conditions. Those failure mechanisms will be invalid as predictors of failure rate in the use conditions. One of the most important factors considered in reliability study is to understand the use conditions and evaluate if the failure mechanism is possible in the field.

3. FAILURE/LIFE MODELS USED IN SEMICONDUCTOR PACKAGES

The purposes of reliability assessments include (1) understanding the physical or chemical phenomena causing the failures. (2) improving the design and optimize the materials to improve reliability performance, (3) collecting failure data to describe the statistical distribution of failures and, (4) predicting the reliability and failure rates in the field applications. In order to predict the reliability performance under various conditions, failure/life models are required.

Different failure mechanisms might need different models to describe the failure characteristics and for reliability prediction. For example, the models describing failure distributions with a constant failure rate will be different from those describing wear-out failures, which are inherently related to the materials, the design of the package and its manner of application. Wear-out failures generally will demonstrate an increasing failure rate and are dependent on time in the field.

Two different stress models are often used in calculating the reliability and the time-to-failure of semiconductor packages. One, is the inverse power law model and the other, is the Arrhenius model.

3.1 Introduction

3.1.1 Inverse power law (IPL) model

IPL model is a flexible model for the expected number of failures in the first t hours,
$t_f(t)$, shown as

$$t_f(t) = at^b \quad for \ a, b > 0 \tag{3.1}$$

Coffin –Manson model is an example of IPL models. The unknown parameters in the IPL model are the constants (a and b). A summary of the constant b in the literature is summarized in Table 3-1. The parameters vary with the materials used and the dominant failure mechanisms detected.

Table 3-1 Exponent parameters b used in IPL models

Authors/Sources	Mechanism/materials	Exponent b
Norris & Landzberg, 1969	Solder (95Pb5Sn)	1.9
Kotlowicz, 1989	Solder (37Pb63Sn)	2.27
Li et al., 1991; Hall, 1991; Ju et al., 1994	Solder (37Pb63Sn)	1.2 to 2.7
Scharr,1991	Cu and lead frame alloys	2.7
Dittmer et al., 1995	Al Wire bonds	3.5
Dunn & Mcpherson,1990	Au4Al fracture in WB	4.0
Peddada & Blish, 1993	Delamination/bond failure	4.2
Blish, 1997	Au wire down bond heel crack	5.1
Zelenka, 1991	Interlayer dielectric cracking	5.5+/- 0.7
Hagge, 1989	Silicon fracture	5.5
Cui, 2005	Substrate via cracking	4.2
Chen and Mencinger, 2000	cracking in substrates	1.25
Dunn and Mcpherson, 1990	Si fracture	7.1
Blish, Vaney [1997]; Chen and Mencinger, 2000	Thin film cracking	8.4 6.0
Intel, 2000	NA	3.0-10: Brittle materials 1.5-2.5: Ductile 1-2: Hard metal

3.1.2 Arrhenius models

The Arrhenius model is used to model the impacts from temperature on failure me-

chanisms. The time-to-failure can be expressed as

$$t_f = ae^{-E_a/kT} \qquad\qquad\qquad\qquad (3.2)$$

It is obvious that the activation energy E_a has significant effects on the time-to-failure estimation. However, there are risks using the typical E_a value, which might not represent the devices of interest [Lall, 1996]. Instead, the activation energy E_a shall be calculated based on the experimental data.

Through the years, a large amount of experimental data has been accumulated for the activation energy E_a of various failure mechanisms, as shown in Table 3-2.

Table 3-2 Activation energy (Ea) values [Blish et al., 1991, 1997, 2000]

Failure Mechanisms		Activation energy, Ea	Stress factors
Wire bonds and their interfaces	Neck broken	0.70 eV	Temperature; Δt
	Lifted bonds	1.26 eV	Temperature; Δt
	Intermetallic degradation	0.8eV	Temperature
Corrosion of bond pads and metal traces		0.53-0.7eV; 0.6-1.0 eV	RH, temperature
Passivation defect failure		0.79eV; 0.56eV	Temperature, RH
Solder electromigration		0.64 eV-0.72eV (Cu UBM); 1.03 eV-1.11 eV(Ni-UBM).	Current and temperature
Inter layer dielectric (ILD)		0.68eV	Δt
Micro cracking		0.4 eV-0.95 eV	Δt
Thermal interface degradation		0.45eV	Temperature and humidity
Oxidation		1.3 eV to 2.0 eV	Temperature

3.2 Description of reliability models

An accelerated test model is usually developed entirely based on curve fitting of failure data. The models typically associate the reliability performance with the stress factors, such as temperature, voltage or temperature gradient. Failure data will be characterized by Weibull, lognormal or exponential distributions.

3.2.1 Arrhenius-Weibull models

If the product life data had a Weibull distribution at an absolute temperature T, an Arrhenius-Weibull model can be developed. The Weibull shape parameter β in the model is a constant (independent of temperature). The natural Log of the Weibull characteristic life $\eta(T)$ is a linear function of the inverse of an absolute temperature T, shown as

$$Ln[\eta(T)] = \gamma_0 + \frac{\gamma_1}{T} \tag{3.3}$$

The parameters γ_0, γ_1, and β are the characteristics of the packages and test methods, and are estimated from the test failure data.

The cumulative distribution function can be expressed as

$$F(t,T) = 1 - \exp\left[-\left(\frac{t}{\eta(T)}\right)^{\beta}\right] = 1 - \exp\left\{-\left[t\exp\left[-\gamma_0 - \left(\frac{\gamma_1^{'}}{T}\right)\right]\right]^{\beta}\right\} \tag{3.4}$$

A high β value corresponds to a narrow distribution of Ln life and a low β value corresponds to a wide distribution of Ln life.

3.2.2 IPL-Weibull model

If the life time of the package has a Weibull life distribution whose characteristic life

is a power function of stress, an IPL-Weibull model can be used. The model will as-

sume that,

     a. at stress level U, the product life has a Weibull distribution

     b. the Weibull shape parameter β is a constant

     c. The Weibull characteristic life follows an IPL of stress factor U

$$\eta(U) = e^{\frac{\gamma_0}{\gamma_1}} \tag{3.5}$$

    The parameters γ_0, γ_1, and β are characteristics of the packages and test me-

thods, and are estimated from the failure data.

The cumulative life distribution can be expressed as

$$F(t,U) = 1 - \exp\left[-\left(\frac{t}{\eta(U)}\right)^{\beta}\right] = 1 - \exp\left\{-\left[t\exp\left[-\gamma_0/U^{\gamma_1}\right]\right]^{\beta}\right\} \tag{3.6}$$

3.2.3 Arrhenius-Exponential models

The Arrhenius –Exponential mode is a special case of the Arrhenius-Weibull model

with a shape parameter of $\beta = 1$, with the assumptions below

    a. at any absolute temperature T, the lifetime has an exponential distribution

    b. the natural log of the mean life θ is a linear function of the inverse of T,

The model can be expressed as

$$Ln[\theta(T)] = \gamma_0 + (\gamma_1/T) \tag{3.7}$$

57

Model parameters γ_0 and γ_1 are characteristics of the product and test methods and

are estimated from the data.

At absolute temperature T, the cumulative distribution function is

$$F(t;T) = 1 - \exp[-t/\theta(T)] = 1 - \exp\{-t\exp[-\gamma_0 - (\gamma_1/T)]\} \quad (3.8)$$

3.2.4 IPL-Exponential models

The assumptions of the IPL- exponential model include

       (1) at any stress level U, the lifetime has an exponential distribution and

       (2) the mean life θ is an inverse power function of U.

The model can be expressed as

$$\theta(U) = e^{\gamma_0}/U^{\gamma_1} \quad (3.9)$$

Model parameters γ_0 and γ_1 are characteristic of the product and test method. $\theta(U)$

can be plotted as a straight line on log-log paper.

The failure rate $\lambda = 1/\theta$ is a power function of U, and can be shown as

$$\lambda(U) = e^{-\gamma_0}U^{\gamma_1} \quad (3.10)$$

At stress level U, the cumulative distribution function can be expressed as

$$F(t;U) = 1 - \exp[-t/\theta(U)] = 1 - \exp[-te^{-\gamma_0}U^{\gamma_1}] \quad (3.11)$$

3.3 Acceleration factor (AF) models

The acceleration factor (AF) is defined as a ratio of a degradation rate at an elevated stress level relative to that at a lower stress level, or as the ratio of times to failure. It can be described as

$$AF = \frac{MTTF_{use}}{MTTF_{test}} = \frac{Failure\ life\ in\ use\ conditons}{Failure\ life\ in\ test\ conditions} \qquad (3.12)$$

Typically, the AF is failure mechanism specific. For one specific failure mechanism, the acceleration factor is the product of the acceleration factor for individual stress factors, shown in the following format,

$$AF = AF_T \times AF_V ...... \qquad (3.13)$$

For an AF with multiple failure mechanisms, every failure mechanism will be identified and its unique AF will be calculated for each mechanism at given stress factors, using Eq(3.13). The overall AF can be expressed based on the failure rate models. The details will be discussed in later chapters.

The true task of the reliability modeling is to estimate an appropriate value of the AF based on the expected /observed failure mechanisms that will occur in the field. In the following section, some examples of AF models are shown.

(a) AF due to temperature stress

$$AF_T = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)\right] \qquad (3.14)$$

(b) AF due to voltage stress

$$AF_V = \exp\left[\psi(V_{use} - V_{test})\right] \tag{3.15}$$

(c) AF due to temperature range

$$AF_{\Delta T} = \left(\frac{\Delta T_{test}}{\Delta T_{use}}\right)^n \tag{3.16}$$

(e) AF due to humidity

$$AF_{RH} = \left(\frac{RH_{test}}{RH_{use}}\right)^c \tag{3.17}$$

As mentioned above, the acceleration factor of a single failure mechanism, under various stress factors can be the product of the acceleration factor for individual stress factors, as described in Table 3-3. This is only true when there is one common failure mechanism.

The accuracy of the AF models depends on the model parameters. However, in many applications, the AF models adopt historical data, which might not be accurate, especially with advancements in the material development processes. In many conditions, new characterization shall be done to verify the model parameters.

Table 3-3 Acceleration factor under various stress factors [JESD91A, 2003][JEP122C, 2006]

Stress Tests	Acceleration factor model
Temperature and voltage (Eyring Model)	$AF(T,V) = AF(T) \times AF(V) =$ $\exp\left(\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)\right) \times \exp(\psi(V_{test} - V_{use}))$
Temperature and relative humidity (Peck-model)	$AF(T,RH) = AF(T) \times AF(RH) =$ $\exp\left(\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)\right) \times \left(\frac{RH_{test}}{RH_{use}}\right)^c$
Temperature cycling (Coffin-Manson or its modification)	$AF = AF(\Delta T) \times AF(T) \times AF(f) =$ $\left(\frac{\Delta T_{test}}{\Delta T_{use}}\right)^n \times \left(\exp\left(\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)\right)\right) \times \left(\frac{f_{use}}{f_{test}}\right)^m$

3.4 Acceleration factors for multiple failure mechanisms

[Qin and Bernstein, 2005] discusses the needs for total acceleration factors of multiple failure mechanisms and proposes an acceleration factor for multiple failure mechanisms in the following format

$$AF_s = FP_1 AF_1 + FP_2 AF_2 + ... \qquad (3.18)$$

Where FP_1 and FP_2 are failure percentages of various failure mechanisms, and AF_1 and AF_2 are the individual acceleration factors.

[Moura, 1992] proposes a similar approach, which does not need the assumed constant failure rate of the system. An average failure rate is used in certain time intervals of the interest. The average failure rate in the exact time interval of the interest is estimated for each component at the use conditions, where,

$$\lambda_T = \sum_{i=1}^{m} n_i \lambda_i \tag{3.19}$$

n_i is the quantity of components of type I and λ_i is the average failure rate of component type i.

$$AF = \sum_{i=1}^{m} n_i \lambda_i AF_i / \sum_{i=1}^{m} n_i \lambda_{ui} \tag{3.20}$$

The equivalent AF is a weighted average of the AF of each technology type in the subassembly.

3.5 Package failure models

3.5.1 IMC diffusion model

The formation and growth of IMC layers has a significant impact on bonding interface failures. The growth rate of the IMC at a given temperature usually follows a parabolic relationship,

$$x = \xi t^{1/d} \tag{3.21}$$

62

where x is the IMC thickness, and t is the time, d is the constants, ξ is the diffusion

rate constant at the selected temperature, and $\xi = He^{-\frac{E_a}{kT}}$ where Ea is the activation

energy.

[Li et al., 2006] reports the activation energy of $(Cu,Ni)_6 Sn_5$ IMC growth is about

0.59eV when d=2. [Kim et al., 2003] reports an IMC growth rate of copper wires on

aluminum pads described as

$$x = 0.004658t \times \exp\left(\frac{-13046.179}{T}\right) \tag{3.22}$$

[Chen and Chen, 2009] obtains d=4.1(EP-Ni) and 3.7 (EL-Ni) for different sold-

er/UBM systems. The activation energy for EP-Ni UBM is 51 Kj/mol and 48kJ/mol

for El-Ni UBM systems.

The rate of formation of intermetallic phases might be described by a single, activa-

tion energy over the entire temperature range [Braunovic and Alexandrov, 1994]. In

other cases, the rate can be a variable. [Uno and Tatsumi, 2000] reports the activation

energy for bonding under various molding compound composition including Bi-

Phenyl Epoxy Resin (BP) and Ocresol Novolac Epoxy (OCN), concluded as the fol-

lowing

For BP (<450k), $\xi = 2.0 \times 10^{15} \exp\left(\frac{-2.0eV}{kT}\right)$

For BP (>450k), $\xi = 5.1 \times 10^{19} \exp\left(\frac{-1.5eV}{kT}\right)$

For OCN (>430k), $\xi = 5.5 \times 10^{19} \exp\left(\frac{-2.3eV}{kT}\right)$

[Liao and Wei, 2004] uses the following equation to model the thickness/growth of the Cu-Sn compound,

$$x = \left(\frac{T^2}{R_{ramp}} \right) \frac{k}{E_a} K_0 e^{-E_a / k T} \tag{3.23}$$

where K0,and R_{ramp} represented reaction rate constant and temperature ramping rate. The activation energy for Cu6Sn5 compound formation is found to be 0.97 +/- 0.06 eV.

3.5.2 Thermal-mechanical fatigue models

In assessing the reliability of solder joints under thermal-mechanical stresses, the fatigue models, including Coffin-Manson model and its modifications, are usually applied to describe the time to failure characteristics. The Coffin-Manson model can be described as

$$N_f = C \left(\frac{\Delta \varepsilon}{2 \varepsilon_f} \right)^n \tag{3.24}$$

Where N_f is the mean number of cycles to failure and $\Delta \varepsilon$ is the inelastic strain range, and $\Delta \varepsilon = F \dfrac{L_D}{h} \Delta \alpha \Delta T$, ε_f is the fatigue ductile coefficient in shear, e.g. solder constant is 0.325 and C is the fatigue strength coefficient,

$C = -0.442 - 6 \times 10^{-4} T_s + 1.74 \times 10^{-2} Ln \left(1 + \dfrac{1}{t_0} \right)$, where T_s is the mean cycle temperature of the solder in C, t_0 is the dwell time in minutes at max temperature.

[Sumikawa et al., 2001] uses a simplified model to describe the relationship between the median of the number of cycles to failures and the equivalent inelastic strain as

$$N_f = \left(\frac{\Delta\varepsilon}{0.25}\right)^{-2} \tag{3.25}$$

[John Lau, 1997simply adopts the following format

$$N_f = C(\Delta\varepsilon)^n \tag{3.26}$$

where C is noted to be 2.37 and n=-2.564 for 63Sn37Pb eutectic solders.

[Chen et al., 2005] describes the relationship between strain and number of cycles differently, by considering the cycle frequency,

$$\left[N_f f^{(s-1)}\right]^z \Delta\varepsilon = C \tag{3.27}$$

where f is the frequency factor, k is the frequency exponent

and
$$s = 0.919 - 1.765 \times 10^{-4} T - 8.634 \times 10^{-7} T^2$$

$$z = 0.731 - 1.63 \times 10^{-4} T + 1.392 \times 10^{-6} T^2 - 1.151 \times 10^{-8} T^3$$

$$C = 2.122 - 3.57 \times 10^{-3} T + 1.329 \times 10^{-5} T^2 - 2.502 \times 10^{-7} T^3$$

[Yu and Shiratori, 1997] omits the effect of frequency and assume the strain rate of the solder related to the following equation,

$$\varepsilon = A.\sigma^\zeta \exp\left(\frac{-E_a}{kT}\right) \tag{3.28}$$

It reports A=3.29e+11 and $\zeta = 5.66 \times 10^{-0.00288(T-273)}$ and Ea/k=13180.0.

ς is the steady state strain rate and σ is applied stress.

[Norris and Landzberg, 1969] first reports a model considering the cyclic frequency, and the maximum temperature and temperature range all together, shown as

$$\frac{N_{use}}{N_{test}} = \left(\frac{f_{use}}{f_{test}}\right)^m \left(\frac{\Delta T_{test}}{\Delta T_{use}}\right)^n \Phi(T_{max}),$$ (3.29)

where $\Phi(T\,max) = \exp\left(\gamma\left(\dfrac{1}{T_{use\_max}} - \dfrac{1}{T_{tets\_max}}\right)\right)$ (3.30)

For high lead solders, n=2 and m=1/3, and γ is 1616. For lead free solders (e.g. SnAgCu(SAC)), [Pan et al., 2005] finds a new set of model parameters with n= 2.65 and m = 0.136, and γ is approximately 2185.

[Salmela,2007] describes a modified Norris-Landzberg's model by adding the correction term Corr(ΔT) (Temperature –excursion-range-dependent correction factor). The acceleration factor is then expressed as

$$AF = AF_{base}\frac{(Corr\,(\Delta T_{use}))^{(-1/B_{use})}}{(Corr\,(\Delta T_{test}))^{-(1/B_{test})}}$$ (3.31)

(AF$_{base}$) is calculated from Norris-Landzberg's equation

Where B is depend on the thermal cycling profile

$$B = -0.442 - 6.10^{-4}T_{sj} + 1.74.10^{-2}\ln\left(1 + \frac{360}{t_d}\right)$$ (3.32)

Where T_{sj} is the average temperature of the solder and t_d is the half dwell-time (in minutes). $Corr(\Delta T)$ can be determined. The described formula can better explain the observed the differences between the acceleration factor values recorded for different solder materials.

66

3.5.3 Fracture failure models

For fracture failures, the Paris-Erdogan equation is established to describe the relationship between the die crack growth rate and the variation in the cyclic stress intensity factor, expressed as

$$\frac{dL_c}{dN} = A(\Delta K)^{m_p} \tag{3.33}$$

Where dL/dN is the crack growth rate, A and m_p are material constants,

$K = G\sigma\sqrt{2\pi L}_c$ is the new intensity factor, L_c is the crack length, σ is the nominal stress and the factor G is a function of geometry, $\Delta K = G\sigma_r\sqrt{2\pi L_c}$. σ_r is the nominal stress range.

[Strifas et al., 2002] investigates the crack growth in the solder joints under cycling conditions and computes the characteristic joint fatigue life as

$$t_f = N_0 + \frac{L_c}{dL_c / dN} \tag{3.34}$$

$$\frac{dL_c}{dN} = K_3 \Delta W_{acg}^{K_4} \tag{3.35}$$

L_c is the crack length and t_f is the number of cycles to 63.2% population failure. K3 and K4 are constant.

N_o is cycles to crack initiation. da/dN is the crack growth rate per cycle.

$$N_0 = K_1 \Delta W_{avg}^{K_2}, \tag{3.36}$$

where K1 and K2 are the constant.

ΔW_{avg} is the volume average visco-plastic strain energy density accumulated through the third thermal cycle

$$\Delta W_{avg} = \left[\frac{\sum\limits_{n=1}^{\# \, of \; elements} \Delta W_n V_n}{\left[\sum\limits_{n=1}^{\# \, of \; elements} V_n \right]} \right] \Bigg/ \left[\sum\limits_{n=1}^{\# \, of \; elements} V_n \right] \tag{3.37}$$

Where ΔW_n is the average strain energy density of the element numbered n, and Vn is the volume of this element.

[Darveaux et al., 1994] publishes the damage relationship used for correlating damage-to-the life as

$$N_f = 7860(\Delta W)^{-1.00} \tag{3.38}$$

$$\frac{dL_c}{dN} = 4.96e - 8(\Delta W)^{1.13} \tag{3.39}$$

[Luo et al, 2005] finds that the solder joints in the corners of the package suffer much higher plastic strain and are more susceptible to failure. The main failure mechanism in board level drop tests is the plastic strain-induced crack at the interface between the solder balls and the pads in the packages. The failure models can be obtained as

$$N_f = 10.959 \times \Delta W_{avg}^{-0.45196} + \frac{L_c}{0.0699 \times \Delta W_{avg}^{0.660}} \tag{3.40}$$

68

3.5.4 Electromigration models

The electromigration failures discussed in this section are only related to flip chip solder bumps in the packages. The critical factors influencing the electromigration performance of solder bumps are the bump dimension, bump materials and UBM structures.

Electromigration failures can be described using the well known Black's equation. The typical time-to-failure due to the electromigration can be expressed as

$$t_f = \frac{A}{J^n} e^{\left(\frac{E_a}{kT} \right)} \tag{3.41}$$

A, Ea and n can be determined by experimental results.

[Ding et al., 2005] determines the Ea is 0.64 eV to 0.72eV for Cu UBM structure and 1.03-1.11 eV for Ni UBM structure. [Lee et al., 2007] calculates Ea and n of Sn-3.5Ag solder to be 1.63eV and 4.6, respectively. [Ramanathan et al., 2007] obtains Ea=0.84eV and n=10.1 for Sn0.7Cu solder bump on a plated Cu UBM. The n value is significantly higher than the value of 2 due to the Joule heating presented.

3.5.5 Corrosion/temperature & humidity models

The basic corrosion reliability models still remain tied to a few key variables, such as the relative humidity, the temperature, the voltage across conductors, contaminants and catalysts. In most cases, an Arrhenius exponential form is sufficient to represent the corrosion rate dependence on the temperature, except that the strength of such a

dependence is dictated by the activation energy characteristic of the rate controlling mechanism responsible for the failure.

[Uno and Tatsumi, 2000] mention the growth of corrosion layers on the bonding interface, where the width of corrosion layer W is given as gt, where

$g = g_0 \exp\left(-\dfrac{E_a}{kT}\right)$. The growth rate of the corrosion g is found to be related to the molding compound materials. Considering the Au_4Al alloy, the activation energy is 1.6eV for BP resin and 2.3eV for OCN resin.

[Shirley and Hong, 1991] develop a model for moisture penetration through passivation micro-cracks. The models applied in the study are a combination of Arrhenius model and power models, shown as

$$t_f = A\exp\left(\dfrac{-E_a}{kT}\right)(RH)^c \tag{3.42}$$

where Ea =0.79eV and c=4.64 for passivation cracking failures.
[Merrett et al., 1983] describes the life model as

$$t_f \propto \exp\left(0.00044RH^2 + \dfrac{E_a}{kT}\right) \tag{3.43}$$

where $E_a = 0.56eV$ for the temperature range of 85-110 $^\circ$C. [Li et al., 2007] determines the Ea=0.796eV and m=2.815 for delamination failures under temperature and humidity testing. The equation for reliability life at temperature and moisture conditions can be written as

$$t_f = \frac{85^3}{RH^3} \exp\left[\frac{0.9eV}{k}\left(\frac{1}{T+273} - \frac{1}{358}\right)\right] \qquad (3.44)$$

where n=-3.0 and Ea=0.9eV.

Relative humidity is one of the strongest factors in the corrosion process. [Osenbach et al., 1997; Peck, 1986; Striny and Schelling, 1981] fit the temperature and humidity biased accelerated life test data in the form of

$$t_f = Ae^{(-E_a/kT)}e^{-B(RH)^2} \qquad (3.45)$$

or

$$t_f = A\exp\left(\frac{E_a}{kT} + \frac{B}{RH}\right) \qquad (3.46)$$

or

$$t_f = A(RH)^c\left(\frac{E_a}{kT}\right) \qquad (3.47)$$

Moreover, [Striny, 1981] develops a reliability model for aluminum corrosion failure data, shown as

$$AF = \exp\left(\frac{E_a}{K}\left(\frac{1}{T_u} - \frac{1}{T_s}\right) + E_b\left(\frac{1}{H_u} - \frac{1}{H_s}\right)\right) \qquad (3.48)$$

[Giacomo et al., 1996] depicts the time to failure expression of common metallization used in thin-film circuitries, as well as thick films and interconnects as,

$$t_f = A\frac{(1-RH)[1+(B-1)RH}{RH} \qquad (3.49)$$

For b<<1 (most of cases), the time to failure due to corrosion can be written as

$$t_f = A\frac{(1-RH)^2}{RH}$$
(3.50)

where A and B are constants and the RH is the relative humidity. A and B can be determined by experimental results.

[Rudra et al., 1994] discusses the growth of filaments due to temperature, humidity, voltage loads and the time to failure, shown as

$$t_f = \frac{\alpha p(1000L_{eff})^\mu}{V^\omega(M-M_t)} \quad \text{when M>M}_t$$
(3.51)

$$t_f = \infty \qquad \text{when M<M}_t$$
(3.52)

L_{eff} is the effective length between conductors. $L_{eff} = yL$, y is the shape factor, from 0.5 to 2.

3.6 Summary

This chapter discusses available failure models and describes various failure mechanisms, including life and acceleration factor models. Additionally, the concepts of differentiating AFs based on specific failure mechanisms and generating the overall system AFs based on expected failure mechanisms, are reviewed.

For solder joint related failures, the models are constructed based on the Coffin-Manson model or its modification; e.g. Norris-Landzberg model, where there are huge variations on the model parameters used. The models are usually based on a increasing failure rate. Since few models of non-solder jointed related failures are

72

available, it is difficult to describe failure mechanisms such as interface delamination, and even when models are available, their accuracy cannot be determined, as little work has been done in that area.

Moreover, the majority of available failure models focus on a single failure mechanism when, in reality, multiple failure mechanisms can be observed. Therefore, the models shall describe a situation to illustrate multiple failure mechanisms, and there will be additional discussions in later chapters.

4. END-OF-LIFE AF MODELS FOR RELIABILITY PRE-DICTION OF SOLDER JOINTS

Solder joint reliability is one of the most studied areas in terms of the reliability of semiconductor packages. It is often on the top of the list when discussing package reliability. Solder joint reliability can be categorized as 1st level (e.g. flip chip bumps) and 2nd level.

In general, acceleration models will be used to predict solder joint fatigue life under use conditions based on the fatigue life estimation under stress conditions. However, the accuracy of the model is difficult to validate and is often not validated. As a result, the fatigue life of the solder joints can be over-designed with added cost or time, or under-estimated with a compromised reliability performance. It is an important goal for engineers to use valid and accurate life models to predict the field life of the solder joints and reduce development cost and time.

Most empirical AF models including the Norris-Landzberg model [1969] and its modifications usually consider the effects of temperature range, cycle frequency, and the maximum temperature of the AF value, regardless of the package types, types of substrates, or package materials used. This approach is widely adopted and little is done to validate the models for modern packages structures and materials.

In this chapter, AF models used in solder joint reliability prediction are studied based on the test results from a variety of packages. The results show that the available model parameters used in the industry are not appropriate, in many cases, the predic-

tion does not agree with the test results at all. The industry's use of a common model should be reevaluated.

The studies suggest that a new set of model parameters might be required for new package technologies or new materials. The research shows the acceleration factor models will depend on the solder joint materials and microstructures at the joint interfaces. The solder joint fatigue life performance is too complicated to be assumed as a fixed empirical model.

The methodology to develop an acceleration factor model and the demonstration of their weakness will help achieve reliable solder connections in the future.

4.1 Introduction

Solder joints play an important role in overall package reliability performance. The solder joints can be formed between the pads of printed circuit boards and the leads or solder balls using solder pastes. They can also refer to the connection between solder bumps in the flip chip systems and the substrates. Figures 4-1 to 4-5 show several diagrams of solder joints in the packaging systems. The focus of this study is on the ball grid array packages and assemblies.
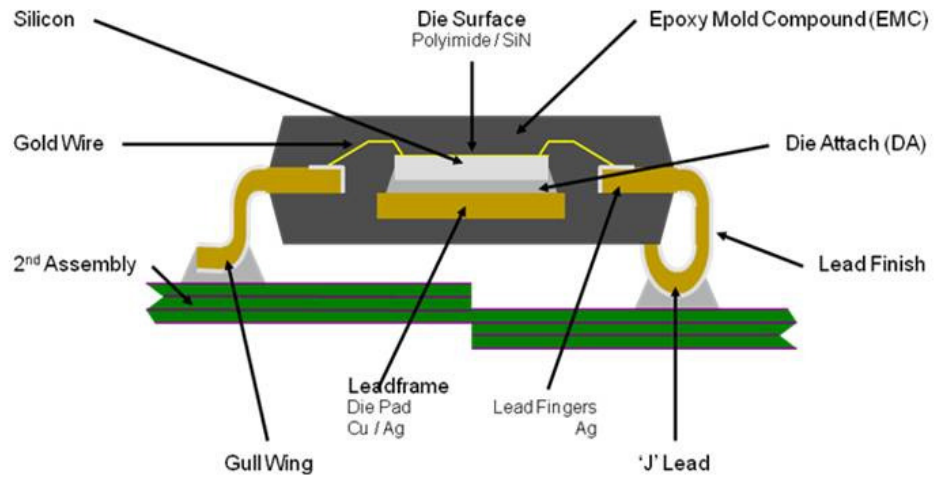
Figure 4-1 Lead frame based packages and the solder joints
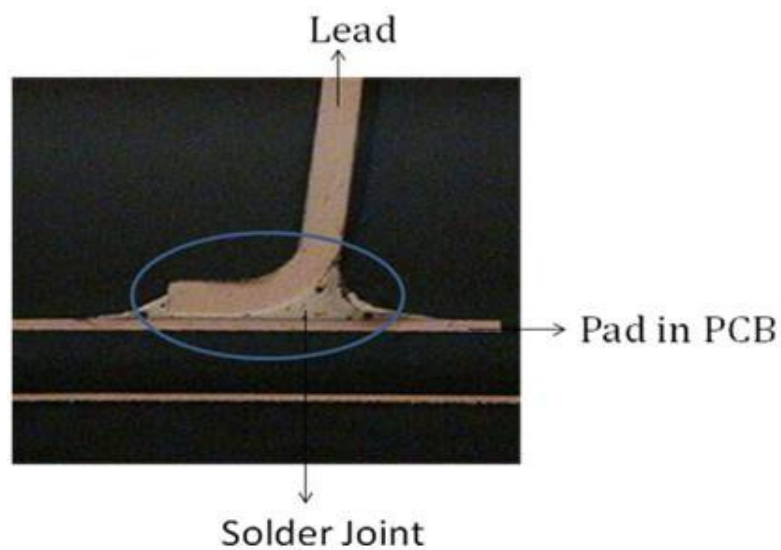
Figure 4-2 A close-up view of the solder joints in lead frame based packages
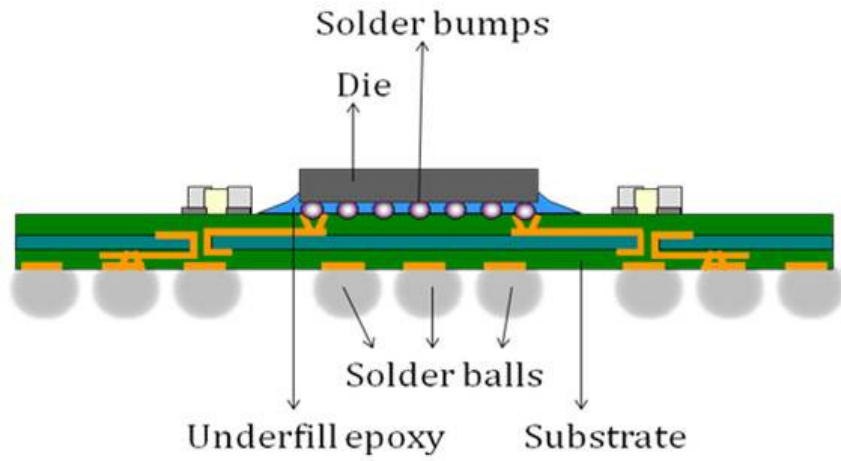
Figure 4-3 A diagram of a flip chip BGA package and solder connects
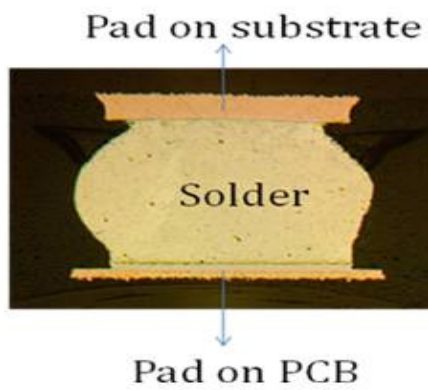
Figure 4-4 Solder joint (2nd level) between the PCB and the substrate
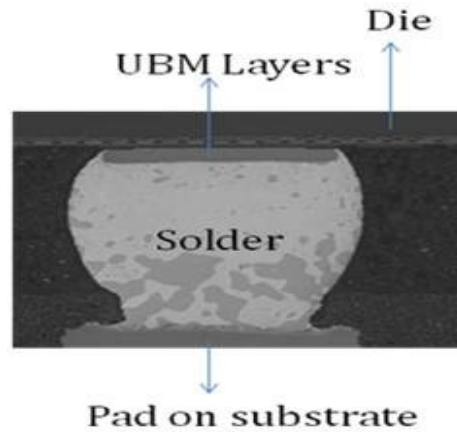
Figure 4-5 Solder joint between the substrates and the silicon die (bumps)

The solder joint reliability is usually assessed by collecting failure data of the solder joints from accelerated stress tests. The fatigue life under stress test conditions will be converted into the reliability life under use conditions through acceleration factor (AF) models.

Historically, the emphasis of solder joint reliability studies is to reduce solder interconnect related failures and meet package qualification criteria by improving the materials and optimizing interface microstructures and the geometry of the joints. Tremendous amounts of data are generated for various solder alloys, interface metal finishes, and package structures. However, few studies focus on the prediction of the fatigue life of solder joints under use conditions. The characteristics of solder joint reliability based on previous studies can be summarized as follows:

(1) The solder joint failures are fatigue failures, which can be accurately described by a Weibull or Lognormal distribution. The tests are in general car-

ried out under thermal cycling (e.g. air-to-air thermal cycle or liquid-to-liquid thermal shock) tests. The mean-time-to-failure (MTTF) and/or characterization life value (η) from the Lognormal or Weibull distributions are used for the reliability analysis.

(2) There are no clear definitions of what the passing criteria are for solder joint life tests. However, there are specifications available to describe how many MTTF cycles the solder joints shall endure under certain conditions in order to assess the reliability of solder joints. Indeed, few studies are trying to correlate the life from the accelerated stress testing with the lifetime of the solder joints in the field conditions.

(3) The Coffin-Manson model is the choice for the life prediction of solder joints when using simulation data, and modified Norris-Landzberg models are the choice for the lifetime prediction using experimental failure data. Using modified Norris-Landzberg models, the model parameters are usually fixed and independent of the package structures and bill of materials used. Additionally, little information is available about the accuracy of the models for today's new packages.

The failures of the solder joints can be presented in a probability paper such as a lognormal paper (shown in Figure 4-6) which will tell the mean-time-to-failure (MTTF) of the failure data plotted. The reliability life of the solder joints under use condi-

tions will be induced based on the acceleration factor models and the MTTF values from the acceleration stress tests.

However, a common problem encountered by reliability or packaging engineers is the accuracy of the acceleration factor models. There is little confidence with the MTTF or failure rate estimated based on the available AF model parameters.
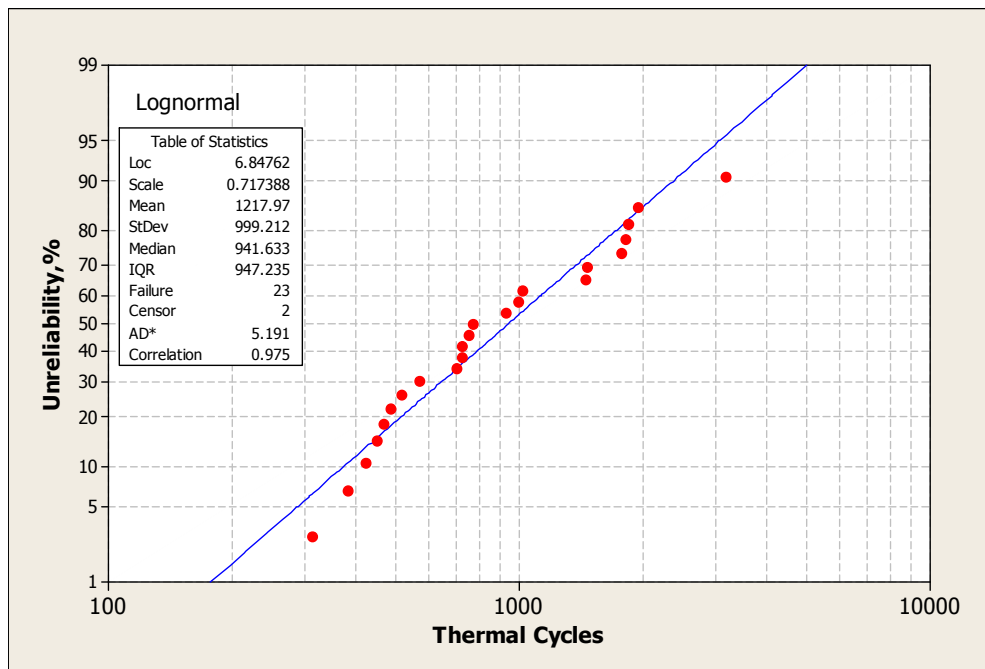
Figure 4-6 An example of a Log-normal plot for solder joint failures

This chapter will examine modified Norris-Landzberg models by studying the reliability performance of various organic packages, which are popular in the industry. In addition, the impacts of several key factors on the model parameters are discussed. Nonetheless, it should be kept in mind that the acceleration factor model is generated

through the failure data fitting. The models cannot be expected to precisely predict

the AF values and there will be acceptable errors.

4.2 The acceleration factor models for solder interconnects reliability

The acceleration factor for the solder joint reliability between any two stress condi-

tions can be expressed as Eq. [4.1] which is first described by Norris and Landzberg

[1969].

$$AF = \frac{N_a}{N_t} = \left(\frac{\Delta T_t}{\Delta T_a}\right)^2 \left(\frac{f_a}{f_t}\right)^{1/3} \Phi(T_{max}) \tag{4.1}$$

Where $\Phi(T_{max}) = \dfrac{life\left(T_{max\_a}\right)}{life\left(T_{max\_t}\right)}$

The model is assumed to take into account the ramp time and dwell time, temperature

factors as well as thermal strains that have been thought significant for the solder joint

fatigue failures.   Additionally, there are following assumptions for the model.

   (1) The relationship between plastic strain, $\Delta \varepsilon_p$ and the cycles to failure, Nf, is

       shown as $N_f \left(\Delta \varepsilon_p\right)^2 = Cons\tan t$ for nearly all metals.

   (2) The thermal fatigue failures occur at a cross section of common $\Delta \varepsilon_p$. Most of

       the fractures happen at or near the chip-to-solder interface, which is the case

       of maximum shear strain. The plastic strain amplitude and the fatigue life are

       closely linked to dimensional considerations.

81

(3) The cycle frequency is assumed to have profound effects on the fatigue life of lead alloys. A hold period or dwell time in creep fatigue will be regarded as a frequency adjustment. The relationship between the cycles-to-failures and the cycle frequency can be expressed as $N_f / f^{\frac{1}{3}} = cons\tan t$. All such effects as time-dependent properties upon fatigue life are contained in the empirical frequency factor.

(4) When strain is applied at a continuously changing temperature, it is antic- ipated that fatigue life will be decreased in the upper temperature region of the cycle due to temperature related effects, such as an increased grain boundary sliding. $\Phi(T_{max})$ is not constant but a ratio of fatigue life under different ex- treme temperatures.

Pan et al. [2005] describes a modified the Norris-Landzberg model for lead-free sold- er joints, shown as

$$AF = \frac{N_a}{N_t} = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{2.65} \left(\frac{t_a}{t_t}\right)^{0.136} \exp\left[2185\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right] \tag{4.2}$$

The term $\Phi(T_{max})$ in the Norris-Landzberg model is replaced with

$\exp\left[2185\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right]$. The cycle frequency term is slightly modified to focus on

the dwell time only.

W. Dauksher [2008] summarizes published testing data and come out a different set

of model parameters using the familiar model as N. Pan et al.'s format, described as

$$AF = \frac{N_a}{N_t} = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{1.75} \left(\frac{t_a}{t_t}\right)^{0.25} \exp\left[1600\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right]$$
(4.3)

O. Salmela [2007] modifies the Norris-Landzberg model parameters to predict their

experimental results, shown as

$$AF = \frac{N_a}{N_t} = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{1.662} \left(\frac{f_a}{f_t}\right)^{1/3} \exp\left[1267\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right]$$
(4.4)

For the Norris-Landzberg model, based on the original data described, if using the

term $\exp\left(\gamma\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right)$ to replace the term $\Phi(T_{max})$, the model will be modified

as Eq.[4.5]. Table 4-1 lists different γ value discussed in the model proposed by

Norris and Landzberg [1969].

$$AF = \frac{N_a}{N_t} = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{n} \left(\frac{f_a}{f_t}\right)^{m} \exp\left[\gamma\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right]$$
(4.5)

Table 4-1 the value of r [Norris and Landzberg, 1969]

$\Phi(T_{max})$ value in N-L model	γ value in N-L modification	Note
2	1616	For 5Sn95Pb high lead solder, two extreme temperatures are 85 ^{o}C and 150 ^{o}C.
1.82	1392	Solder volume to form the joints is 60 mils; two thermal cycling conditions, 25 ^{o}C-85 ^{o}C @ 3 cycles/h and 0 ^{o}C-150 ^{o}C @ 2 cycles/h.
1.45	1063	The maximum temperatures used are 110 ^{o}C and 150 ^{o}C.

It is obvious the model parameters are not constant and shall be validated when being used for any reliability prediction. In some of the literature, the term γ is described as E_a, the activation energy related to the maximum temperature in the stress conditions.

In this Chapter, the acceleration factor models using the Norris-Landzberg format are evaluated by examining the reliability performance of various package types under different thermal cycling conditions. The key factors in the thermal cycling profiles include cycle frequency, temperature range, and maximum temperature—assuming they are independent. Additionally the validation tests are presented to validate the observation and conclusions.

4.3 Assessment of AF models

4.3.1 Test vehicles and experiment descriptions

4.3.1.1 Test samples

Table 4-2 lists test vehicles studied. The size of the packages ranges from 10 mm to 33 mm, and the package types cover fcCSPs, MAPBGAs, CBGAs, TEBGAs and FCBGAs. All of the test samples are daisy chain devices where the resistance can be monitored during the test duration insitu. The failure data is analyzed using Weibull or Lognormal distribution, whichever are more appropriate to the failure data.

(1) fcCSP packages

FcCSPs are one type of chip scale package (CSP) using bumps on the die to connect the device to the organic substrates. The die attachment process is called flip chip bonding. The underfill materials are usually applied around the bumps to protect the solder joints and improve the reliability performance of the packages. The package is usually is in a small form factor comparable to FCBGA packages. In addition, the package is molded and looks like a MAPBGA in appearance.

(2) MAPBGA packages

MAPBGA is a form of CSP package with area array solder ball patterns. They are called "mold array process ball grid arrays" packages because of the manufacturing process used. They have various package sizes but typically smaller than 17 mm x 17 mm. The interconnects inside the packages are typically bonding wires, but can be flip chip bumps too.

85

(3) CBGA packages

CBGAs refer to FCBGA packages using ceramic substrates, which are very different from FCBGA packages using organic substrates. The silicon is mounted to the ceramic substrates using flip chip interconnects, however no underfill materials are required during the die attachment. There is a large CTE mismatch between the ceramic substrates and the PCBs, so the reliability of second level BGA solder joints is a concern.

(4) PBGA packages and TEBGA packages

In general, PBGAs are BGA packages which use organic or plastic materials, the substrates can be supported with enhanced thermal plane or embedded stiffeners. PBGAs have many variations and usually use wire bond interconnects and molding compounds. TEBGAs are one type of PBGAs with enhanced thermal capabilities.

(5) FCBGA packages

FCBGAs refer to flip chip BGA packages which use organic substrates, and an underfill process is required to protect the first level interconnects (bumps). The biggest difference between FCBGA and fcCSP is the size of the package. In addition, FCBGAs can come with two versions, with a heat spreader or without. There will be no overmolding materials to protect the die. The biggest differences between FCBGA and CBGA are the substrate material and the underfill processes.

Table 4-2 Test vehicles used in solder joint reliability study

Package Types	Package Size, mm×mm	Die Size, mm×mm	Other Important Attributes
fcCSPs	16×16, 280-ball	10.6×10.1	0.11 mm thick substrate; 0.8 mm pitch
MAPBGAs	13×13, 144-ball	6×6 & 8×8	0.32 mm thick substrate; 1 mm pitch
	10×10, 144-ball	6×6	0.32 mm thick substrate; 0.8 mm pitch
	12×12, 179-ball	6.6×6.7	0.36 mm thick substrate; 0.8 mm pitch;
	13×13, 225-ball	9.65×9.3	0.24 mm thick substrate; 0.8 mm pitch;
	14×22, 209-ball	8×13	0.36 mm thick substrate; 1.0 mm pitch;
	17×17, 208-ball	6×6 & 8×8	0.36 mm thick substrate; 1.0 mm pitch
	13×13, 216-ball	7×6.5	0.26 mm substrate thick; 0.8 mm pitch
	15×15, 196-ball	10.2×9.6	0.36 mm thick substrate; 1.0 mm pitch.
CBGAs	15 ×15, 148-ball	7×7.4	0.6 mm thick substrate; 1 mm pitch.
	20 × 20, 431-ball	14×13	1.0 mm substrate thick; 0.8 mm pitch.
TEBGAs	27 × 27, 516-ball	8.5×8.8	1.5 mm substrate thick; 1.0 mm pitch.
FCBGAs	17 × 17, 332-ball	10.5×9.33	0.94 mm thick substrate; 0.8 mm pitch;
	25 × 25, 360-ball	8×7	1.2 mm thick substrate; 1.27 mm pitch.
	33 × 33, 820-ball	12.5× 12.5	1.17 mm thick substrate; 1.0 mm pitch
PBGAs	27 × 27, 388-ball	10×10	0.56 mm thick substrate; 1.0 mm pitch.

4.3.1.2 Thermal cycling conditions

The key profile elements affecting the solder fatigue life include the temperature range, the ramp rate, and dwell time at the extreme temperature, and the maximum temperature. The impact of those factors on solder fatigue life is different. For instance, the dwell time affects the creep of the materials, and the ramp rate changes the formation of solder microstructure which then influences the solder joint performance. If a ramp rate is too fast, there will be significant shock effects on the fatigue life of the solder joints. However, the most significant element is still attributed to be the temperature range in the thermal cycling profile.

The temperature cycling conditions applied in the studies include air-to-air thermal cycling (AATC) and liquid-to-liquid thermal shock (LLTS), as shown in Table 4-3.

Table 4-3 Thermal cycling conditions and cycle frequencies

TC Conditions	Temperature Range, ΔT (^{o}C)	Cycle Frequency, cycle/hour	T_{max} , ^{o}K
0 ^{o}C/100 ^{o}C (AATC)	100	1	373.15
0 ^{o}C /100 ^{o}C (AATC)	100	2	373.15
0C/125C (AATC)	125	1.65	398.25
-40 ^{o}C/125 ^{o}C (AATC)	165	1 & 6	398.25
-55 ^{o}C/125 ^{o}C (LLTS)	180	6	398.15
-50 ^{o}C/150 ^{o}C (AATC)	200	1	423.15

4.3.1.3 Failure criteria and failure data collection

The resistance in the test vehicles will be monitored in-situ during the tests. The sample size for each test vehicle is 16 or 32. The exact cycles-to-failures will be recorded by event detectors. Failure analysis will be carried out to confirm the failure mechanisms. A Weibull distribution or a log-normal distribution is found to be the most appropriate for the fatigue failures seen in the solder joint reliability analysis. Commercial statistical software MINITAB is used for the failure data distribution analysis.

4.3.2 Results and discussions

Using the AF model formula described in Eq. [4.5], three model parameters need to be determined: the power exponent n for the range of cycle temperature, m for the cycle frequency, and γ in terms of maximum temperature.

4.3.2.1 Impacts of various factors on solder joint reliability

(1) The impact of surface finishes of PCB pads

Three types of surface finishes are studied for 12 mm $\times$ 12mm fcCSP packages under the thermal cycling condition of -40 ^{o}C to 125 ^{o}C. The failure data are shown in Table 4-4 and plotted in a lognormal paper (shown in Figure 4-7). The distribution analysis demonstrates that Ni/Au finish will help achieve a much longer MTTF life comparing to those using ENIG and IT (immersion Sn) finishes with a maximum

89

improvement of 17%. However, the difference of MTTF life between ENIG and IT

finishes is not significant statistically (P-value is 0.057).

Table 4-4 Cycles to failure of fcCSPs solder joints with various surface finishes

No. of Samples	Cycles-to-Failures		
	ENIG	IT	Ni/Au
1	4076	3040	3928
2	4289	3934	4212
3	3793	3620	3204
4	3512	3741	3936
5	3498	3913	3557
6	3338	3801	4067
7	3584	3936	3661
8	3318	4149	4273
9	3764	3687	4442
10	4223	3016	4324
11	3726	3931	4196
12	4162	3525	4323
13	3930	3286	Censored
14	3624	3497	Censored
15	3975	3776	Censored
16	4248	3181	Censored
17	3916	3189	Censored
18	4447	3736	Censored
19	Censored	Censored	Censored
20	Censored	Censored	Censored
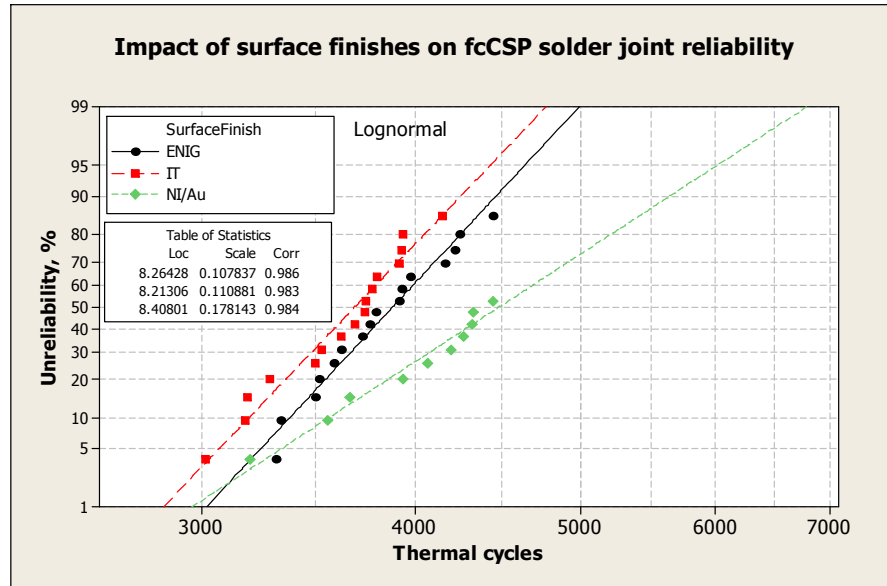
Figure 4-7 Impact of surface finishes of PCB pads

However, if the cycles-to-1% failures are used for the analysis, the difference be-

tween NiAu and ENIG is less than 3% (as shown in Table 4-5), and there is no differ-

ence statistically. It contradicts with the conclusions using the cycles-to- 63.2% fail-

ures, so the conclusion regarding the effectiveness of the surface finishes on the sold-

er joint life depends on the cycles to failures used in the distribution plot.   Ideally, the

plot lines should be in parallel and the conclusion should not be dependent on the

cumulated failure percentage. However, in practical testing the plotted lines are often

not in parallel even for the same failure mechanisms.

Table 4-5 Cycles to failures at different cumulated failure percentages

BGA Pad Finishes	Cycles-to-% Failure			
	1% Failure	5% Failure	10% Failure	MTTF
ENIG	3021	3251	3381	3905
NI/Au	2961	3344	3567	4554
% change	-2%	2.9%	5.5%	16.7%

(2) The impact of solder pastes

To form the solder joints, the solder paste must be applied. This will determine the assembly peak reflow temperature as well as the interface microstructures, and ultimately affect the solder joint reliability.

The cycles to failures for 13 mm × 13 mm 144-ball MAPBGAs using SAC405 solder balls and various solder pastes are compiled in Table 4-6. The data are plotted in a Weibull paper (shown in Figure 4-8). The distribution analysis suggests the performance of eutectic SnPb paste on the PCB pads is much better than that of SAC 405 pastes. Pair-tests on the failure data show the change between SnPb pastes and SAC405 pastes is significant.

Table 4-6 Cycles of failures using SnPb and SAC405 pastes

No of samples	Cycles-to-failures (AATC: -40 ℃/125 ℃)	
	SnPb pastes	SAC405 pastes
1	5480	3904
2	6287	4575
3	4565	4648
4	6227	5356
5	6249	4282
6	5172	4343
7	5728	4784
8	6287	4548
9	5254	3320
10	4965	4388
11	censored	4957
12	5217	4659
13	4585	3352
14	6074	3483
15	5938	4570
16	censored	5501
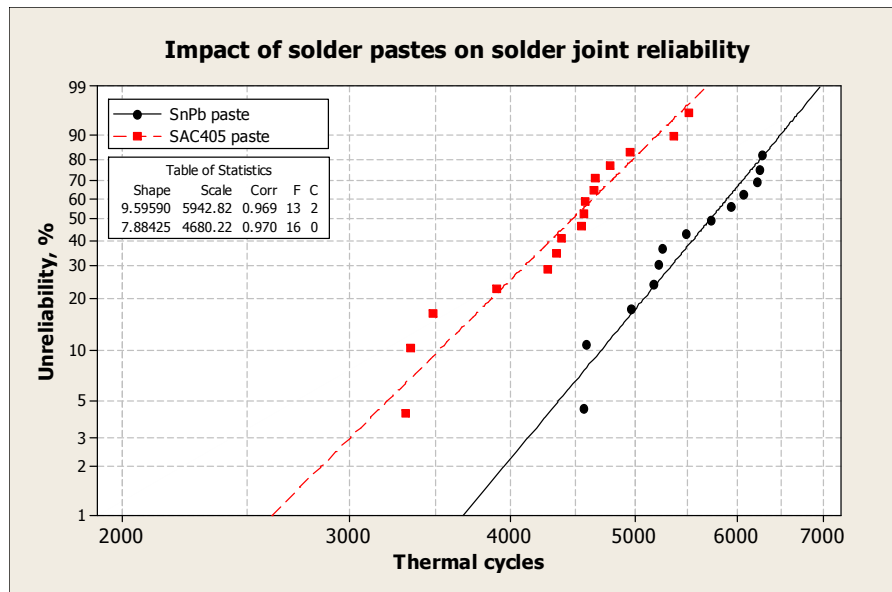
Figure 4-8 Impact of solder pastes on solder joint reliability of 144-

ball MAPBGAs

For a similar13 mm × 13mm 225-ball MAPBGA packages using SAC405/SnPb and

SAC405/SAC405 pastes, the cycles to failures data is listed in Table 4-7 and the

Weibull plot is shown in Figure 4-9, the devices with SnPb pastes perform about

30% better than the units with SAC405 paste in terms of the MTTF life.

Table 4-7 Cycles to failure data observed for 225 BGA packages

# of Samples	Cycles-to-Failures (AATC: -40 °C/125 °C)	
	SnPb Paste	SAC405 Paste
1	3082	2683
2	3691	2947
3	Censored	2677
4	3965	2975
5	3921	2430
6	3481	2499
7	Censored	3168
8	2910	2874
9	2791	3273
10	Censored	3100
11	3794	2648
12	Censored	2495
13	3675	2493
14	3537	2628
15	Censored	2507
16	Censored	2890
17	Censored	NA
18	Censored	NA
19	3137	NA
20	Censored	NA
21	3732	NA
22	3721	NA
23	Censored	NA
24	Censored	NA
25	3507	NA

26	3440	NA
27	Censored	NA
28	3828	NA
29	3520	NA
30	3749	NA
31	3652	NA
32	3512	NA
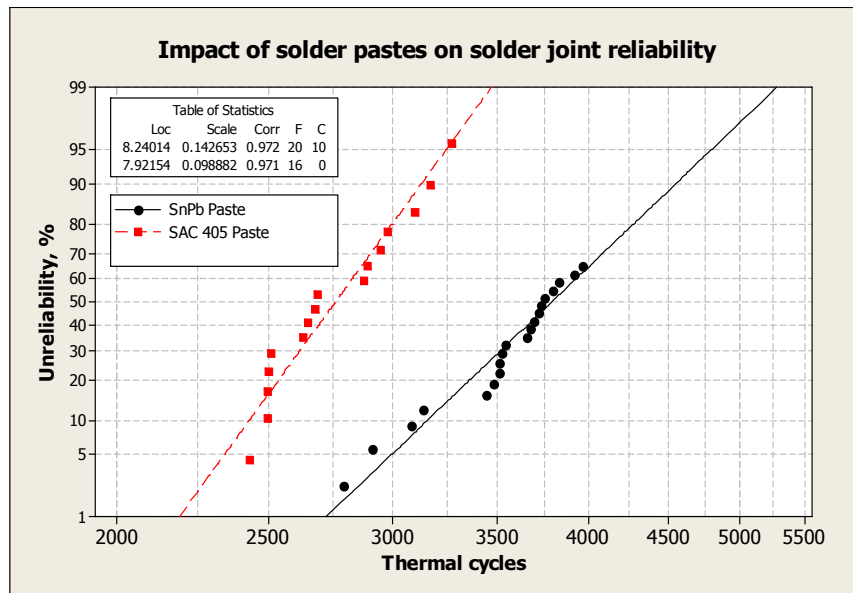
Figure 4-9 Impacts of solder pastes on solder joint reliability of 225 MAPBGAs

However, a conclusion shall not be drawn that SnPb paste will outperform the

SAC405 paste at any conditions. In some of the studies, the SAC solder alloys will

perform equivalently, or even outperform the SnPb solder pastes. There are many

other factors involved in for good solder joint reliability performance.

Table 4-8 shows results of 25 mm × 25 mm 360-ball FCBGAs with 7 mm × 9 mm

die size. It is obvious that the variation of the solder paste composition does not sig-

nificantly affect the solder joint fatigue life. In this case, the SnPb solder balls per-

form equally well as the SAC 405 solder balls using the SAC405 paste.

Table 4-8 Weibull analysis for 360-ball FCBGAs

Solder Composition	TC conditions	Cycles-to-63.2% failure	AF	Cycles-to-1% failure	AF
SnPb/SnPb	-40 ^{o}C/125 ^{o}C	3390	0.97	2498	1.05
	-55 ^{o}C /125 ^{o}C	3498		2372	
SnPb/SAC405	-40 ^{o}C /125 ^{o}C	3317	0.97	2644	1.14
	-55 ^{o}C /125 ^{o}C	3413		2325	
SAC405/SAC405	-40 ^{o}C /125 ^{o}C	3212	X	1971	X

Another case shows totally different results. 431-ball CBGAs are studied to see the

impact of the solder ball materials on the lifetime of the solder joint. Table 4-9 sum-

marizes the Weibull analysis results

Table 4-9 Weibull analysis data summary for 20 mm x 20 mm 431-ball CBGAs

Solder Alloy	TC Conditions	Cycles-to-63.2% failure	Cycles-to-1% failure
SnPb	0 ^{o}C/100 ^{o}C	3639	2190
SnPb	-40 ^{o}C/125 ^{o}C	1675	1055
SAC405	0 ^{o}C/100 ^{o}C	13348	5052
SAC405	-40 ^{o}C/125 ^{o}C	2230	883

Contrary to what is described above; SAC405 solder pastes outperform the samples

using SnPb solder paste if not equal.

The influence of the solder paste on the solder joint life is complicated due to many factors, e.g. soldering processing conditions, the interaction between solder ball alloys and solder paste alloys, and the interface microstructure. It should be careful when we try to make a decision. SnPb and SAC405 alloys are indeed very competitive pair.

4.3.2.2 The development of AF model parameters

In Equation [4.5), three model parameters need to be determined. The power exponent n for the temperature range, m for the cycle frequency and Φ in the exp(Tmax) term.

4.3.2.2.1 The effects of the cycle frequency (f)

At low cycling conditions, the cycle frequency is assumed to contribute significantly to the fatigue life of solder joints. The cycle frequency term in Eq. [4.5] includes the ramp time and the dwell time in the temperature profile. The value of m varies based on which models are used. For instance, the values of 1/3, 0.136, 0.25 and 0.67 (E.qs. [4.2], [4.3], [4.4] and [4.5]) have been used in various acceleration factor models. In this section, two different thermal cycling profiles with different cycle frequencies are evaluated. Table 4-10 shows the conditions and test vehicles used. Cases B and C are using the same materials but different reflowing peak temperature during the board assembly.

Table 4-10 Test conditions and test vehicles for the evaluation of cycle frequency

Case No.	Thermal cycling conditions and cycle frequency	Package assembly
A	0 ^{o}C/100 ^{o}C, 1 cph & 2 cph	13 mm × 13 mm 225-ball MAPB-GA; SAC405 solder balls/SnPb paste
B	0 ^{o}C/100 ^{o}C, 1 cph & 2 cph	12 mm × 12 mm 179-ball MAPB-GA; SAC405 solder balls/SnPb paste
C	0 ^{o}C/100 ^{o}C, 1 cph & 2 cph	12 mm × 12 mm 179-ball MAPB-GA; SAC405 solder balls/SnPb paste
D	0 ^{o}C/100 ^{o}C, 1 cph & 2 cph	12 mm × 12 mm 179-ball MAPB-GA; SAC405 solder balls/SAC405 paste
E	0 ^{o}C/100 ^{o}C, 1 cph & 2 cph	15 mm × 15 mm 148-ball CBGA; SAC405 balls/SnPb pastes
F	-40 ^{o}C/125 ^{o}C, 1 cph & 6 cph	16 mm × 16 mm 280-ball fcCSP;SAC405 balls/SnPb solder paste.

The exponent value of m is summarized in Table 4-11. The results show the value m will change significantly depending on the type of solder pastes and types of thermal cycling (TC Vs TS) conditions.   For example, in case F, the AATC and TS results only provide an m of 0.05 and in case D where SAC405 pastes are used, m is obtained as 0.1. For the same thermal cycling conditions, similar solder materials and package types, the variation of m is acceptable and considered consistent.

Table 4-11 Estimation of *m* value

Test Legs	Solder Paste Alloys	Cycle time, minutes/cycle	Cycle-to-failure, cycles	m value
A: 0 ^{o}C/100 ^{o}C	SnPb	60	3865	0.61
		30	5885	
B: 0 ^{o}C/100 ^{o}C	SnPb	60	5816	0.53
		30	8403	
C:0 ^{o}C/100 ^{o}C	SnPb	60	6542	0.61
		30	9985	
D: 0 ^{o}C/100 ^{o}C	SAC405	60	12937	0.1
		30	13819	
E: 0 ^{o}C/100 ^{o}C	SnPb	60	738	0.67
		30	1174	
F:-40 ^{o}C/125 ^{o}C	SnPb	60	833	0.05
		10	910	

In general, the lower cycle frequency will give more time for the fatigue damage to develop in the solder joints, however, fewer cycles will be applied on the solder joints as a result. The effect of the cycle frequency can affect the influences of the temperature range on the final solder fatigue life as well. If considering the air-to-air thermal cycling for SnPb pastes only, the m value is estimated to be around 0.6.

There is not enough data to generate a universal m value for all the factors. However, it can be assumed that a constant m value will provide a very good estimation for the majority of the packages in similar structures, assuming the same solder joint materials/microstructures.

4.3.2.2.2 The impact of cycle temperature ranges (ΔT) and the maximum temperature (T_{max})

The empirical Coffin-Manson model directly accounts for the differences in fatigue life resulting from differences in the range of the temperature. The thermal strain developed during the thermal cycling is directly proportional to the magnitude of the temperature change. Additionally, depending on the types of the solder alloys used, the dependence of the fatigue life with the extreme temperature might be more complicated than assumed. In the following study, considering only one cycle frequency, the effects of the temperature range (ΔT) and the maximum temperature (T_{max}) on the solder joint fatigue life are evaluated.

(1) Impact of temperature range

33 mm x 33 mm 820-ball FCBGAs are tested under two thermal cycling conditions with the same maximum temperature and similar cycle frequency. The solder joint alloy is SAC405 solder. Under AATC 0 ^{o}C-125 ^{o}C with a 1.85 cycle frequency, the characteristic life is calculated to be 4253 cycles. Under AATC -40 ^{o}C-125 ^{o}C with 1.65 cycle frequency, the character life is estimated to be around 2766 cycles. The acceleration between the two conditions due to the temperature range is 1.54. Since both the maximum temperature and cycle frequency are similar, the acceleration is due to the temperature delta, then the power exponent n for the ΔT term in the model can be estimated to be 1.56, which is much smaller than the typical n=2 or n=2.65 used in other models. Figure 4-10 shows the Weibull plot.
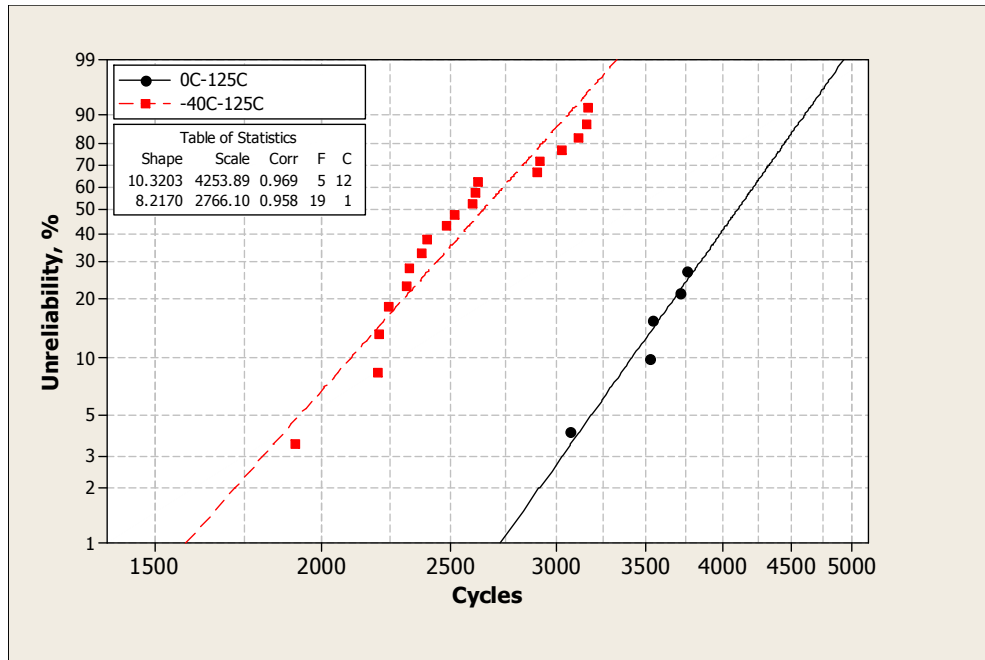
Figure 4-10 Weibull plots of 33 mm FCBGA solder joint failures

However, the AF value should be affected by f and ΔT terms as well.

(2) Combination of temperature range (ΔT) and the maximum temperature (T_{max})

Two groups of studies are conducted to consider the effects of the temperature range and the maximum temperature in the thermal cycling profiles. The assumption is one set of empirical model parameters will be available for all the packages and assemblies. The analysis ignores the influences from package structures, substrates and other factors on the acceleration, instead focusing the thermal cycling conditions and the estimated mean-time-to-failure data.

Table 4-12 summarizes the experimental data between thermal cycling 0 °C/100 °C and -40 °C/125 °C with the same cycle frequency (1 cph) using SnPb solder joints.

Table 4-13 summarizes the experimental data between -40 ^{o}C/125 ^{o}C and -50 ^{o}C/150 ^{o}C using 1 cph cycle frequency for SnPb solder joints.

Table 4-12 Cycles to failure and AF estimation

Package Type	Temperature cycling conditions	Cycles to 63.2% failure, cycles	Estimated AF
208 MAPBGA	0 ^{o}C/100 ^{o}C	4846	2.489
	-40 ^{o}C/125 ^{o}C	1947	
216MAPBGA	0 ^{o}C/100 ^{o}C	10298	2.898
	-40 ^{o}C/125 ^{o}C	3554	
516 TEBGA	0 ^{o}C/100 ^{o}C	11315	2.685
	-40 ^{o}C/125 ^{o}C	4215	
431 CBGA	0 ^{o}C/100 ^{o}C	3639	2.173
	-40 ^{o}C/125 ^{o}C	1675	
332 FCBGA	0 ^{o}C/100 ^{o}C	15925	3.119
	-40 ^{o}C/125 ^{o}C	5106	
332 FCBGA	0 ^{o}C/100 ^{o}C	9003	2.663
	-40 ^{o}C/125 ^{o}C	3381	
360 FCBGA	0 ^{o}C/100 ^{o}C	4753	3.03
	-40 ^{o}C/125 ^{o}C	1568	

Table 4-13 Cycles to failures and AF estimations

Package Type	Temperature cycling conditions	Cycles to 63.2% failure, cycles	Estimated AF
144 MAPBGA	-40 ^{o}C/125 ^{o}C	1679	1.338
	-50 ^{o}C/150 ^{o}C	1255	
144 MAPBGA	-40 ^{o}C/125 ^{o}C	2741	1.224
	-50 ^{o}C/150 ^{o}C	2240	
144 MAPBGA	-40 ^{o}C/125 ^{o}C	2616	1.102
	-50 ^{o}C/150 ^{o}C	2373	
144 MAPBGA	-40 ^{o}C/125 ^{o}C	2487	1.38
	-50 ^{o}C/150 ^{o}C	1802	
208MAPBGA	-40 ^{o}C/125 ^{o}C	3812	2.044
	-50 ^{o}C/150 ^{o}C	1865	
225 MAPBGA	-40 ^{o}C/125 ^{o}C	3372	2.16
	-50 ^{o}C/150 ^{o}C	1561	
388PBGA	-40 ^{o}C/125 ^{o}C	4601	1.565
	-50 ^{o}C/150 ^{o}C	2940	

Based on the data in Table 4-12, the impact of maximum temperature and the temperature range can be expressed as

$$2.722 = (1.65)^n \exp[0.000168\gamma] \tag{4.6}$$

Similarly, the distribution data in Table 4.13 can be processed and then obtain

$$1.545 = (1.212)^n \exp[0.000148\gamma] \tag{4.7}$$

Then it can obtained that $n = 1.79$ and $\gamma = 600$, so the acceleration factor model can be expressed as

$$AF = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{1.79} \left(\frac{f_a}{f_t}\right)^{0.6} \exp\left[600\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right]$$

(4.8)

Additional tests for BGA packages using SAC405 solder joints are conducted and the test results are summarized in Table 4-14.

Table 4-14 Cycles to failures and AF estimation

Package Type	Temperature cycling condi-tions	Cycles-to-63.2% failure	Estimated AF
431 CBGA	0 ^{o}C/100 ^{o}C	13348	5.986
	-45 ^{o}C/125 ^{o}C	2230	
322 FCBGA	0 ^{o}C/100 ^{o}C	21044	5.222
	-45 ^{o}C/125 ^{o}C	4030	
360 FCBGA	0 ^{o}C/100 ^{o}C	11343	4.175
	-45 ^{o}C/125 ^{o}C	2717	

It is obvious that the acceleration factors calculated from failure data listed in Table 4.14 do not fit well with the model shown in Equation [4.9], as well many available models listed in Section 2. However, there is an agreement with the estimation from Pan's model (Equation [4.2]). Considering a similar m value for cycle frequency and an n value, the N. Pan's modification can work well for the failure data in Table 4-14 where the SAC405 solder joints are used.   It confirms that a new model will be needed if the solder joint are made of SAC405 solders instead of eutectic SnPb solders.

4.3.2.2.3 Verification of the AF model

12 mm x 12 mm 179-ball MAPBGAs are studied under air-to-air thermal cycling conditions and a liquid-to-liquid thermal shock condition in order to collect appropriate data and evaluate the models parameters. The failure data from each test conditions is plotted in the Weibull paper and summarized in Table 4-15. The solder ball alloy used in the packages is SAC405 solder with SAC405 solder pastes on the PCB pads to form the solder joints.

Table 4-15 Thermal cycling conditions and characterization life (η)

Types of Solder Pastes used in assembly	TC Conditions	Cycles-to-63.2%-failure (η)
12 mm x 12 mm 179-ball MAPBGAs using SAC405 solder balls and SAC405 (Lead free) paste	0 ^{o}C/100 ^{o}C, 30 minutes/cycle, AATC	13819
	0 ^{o}C/100 ^{o}C, 60 minutes/cycle, AATC	12937
	-40 ^{o}C/125 ^{o}C, 60 minutes/cycle, AATC	4175
	-55 ^{o}C/125 ^{o}C, 10 minutes/cycle, LLTS	4434

The acceleration factor can be experienced as

$$AF = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{1.36} \left(\frac{f_a}{f_t}\right)^{0.1} \exp\left(2651\left(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}}\right)\right)$$

(4.9)

The acceleration factors calculated from modified Norris-Landzberg models is compared to the values from Equations [4.2],[4.3], [4.4] and [4.5] and presented in Table 4-16. It is obvious that some models might work well in certain cases, but it is not possible to predict the acceleration factors using a unified set of model parameters.

Table 4-16 The comparison of estimated AF value from various models

Thermal cycling conditions	n	m	γ	AF model	AF measured
0 ^{o}C to 100 ^{o}C & -40 ^{o}C to 125 ^{o}C	1.79	0.6	600	2.71	2.10 (SAC405/SnPb); 3.09(SAC405/SAC405)
	1.36	0.1	2651	3.09	
	2	0.33	1392	3.44	
	2.65	0.136	2185	5.45	
	1.75	0.25	1600	3.14	
	1.662	0.33	1267	2.85	
-40 ^{o}C to 125 ^{o}C & -55 ^{o}C to 125 ^{o}C	1.79	0.6	600	0.40	0.98 (SAC405/SnPb); 0.94 (SAC405/SAC405)
	1.36	0.1	2651	0.94	
	2	0.33	1392	0.66	
	2.65	0.136	2185	0.99	
	1.75	0.25	1600	0.74	
	1.662	0.33	1267	0.64	

In order to confirm the results from the studies above (mixed AATC and LLTS results), 14 mm x 22 mm 209-ball MAPBGAs using a combination of joints with SnPb solder balls and SnPb solder pastes are tested under three thermal cycling conditions.

The failure data observed in the tests is then plotted in a Weibull probability paper, as shown in Figure 4-11.

	Eta	Beta	r^2	n/s
	2847	8.903	0.961	32/0
	2386	11.31	0.885	32/7
	6730	8.803	0.939	31`/0
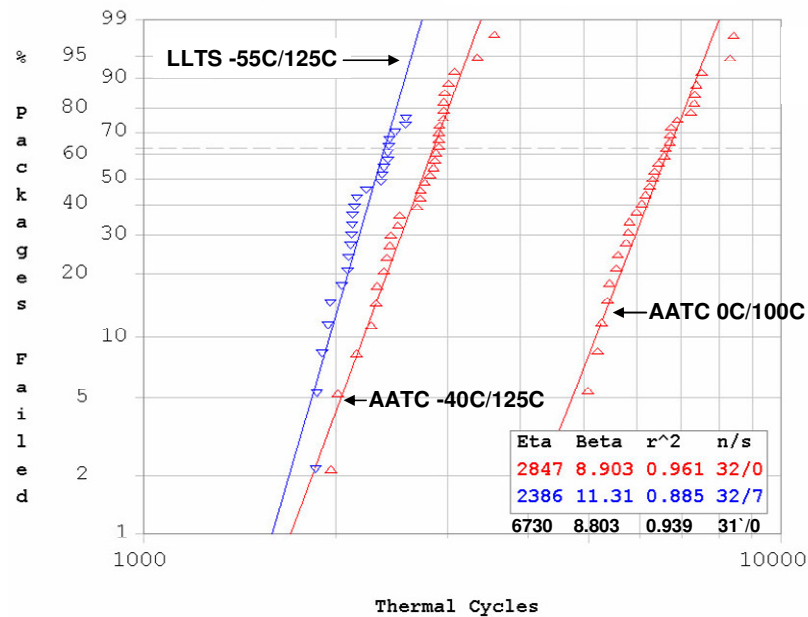
Figure 4-11 Weibull plot of failure data of 209-ball MAPBGAs

The acceleration factor is calculated to be 2.36 between condition A and B, and 1.19 between the condition B and C. For both cases, the model parameters developed for 179-ball MAPBGAs can predict the results well.

Based on the multiple case studies, it can be concluded that the prediction of the acceleration factor is complex. There are too many factors should be considered to decide the model to use. It is important to be cautious in using any models for the prediction of acceleration factors.

4.3.4 Discussions and conclusions

Experimental results in this study show the model parameters developed for certain samples might work for some packages, but cannot be used to predict the acceleration factors for all packages. There are too many factors involved to influence the strain levels the solder joints will endure.

However, the model parameters can be shared for similar package structures and solder joint materials. The solder joint materials are confirmed to be one of the significant factors in the acceleration factor models. Under the same air-to-air thermal cycling conditions, the SAC405 solder joints will produce a higher acceleration factor than eutectic SnPb solder joints. The purpose of this article is not to conclude that the model parameters available in the literature is wrong, instead, the article supports that they can be used to predict some experimental data very well, but are not universal for all BGA packages.

The studies demonstrate that:

(1) There are no universal empirical models for the acceleration factor of solder joints. The available Norris-Landzberg models and its modifications can work in some cases, but in other cases, the same model can give totally wrong results.

(2) The acceleration factor model developed from a similar package structure and a material set can be adopted for similar packages and materials. For instance,

the model parameters presented in this article (Equation [4.9]) are based on failure data observed from various BGA types, sizes, thickness of substrates as well as the variation of board configurations. The model can be used to predict the acceleration factors for similar package structures and materials within an acceptable tolerance (organic substrates with SAC405/SnPb solder composition, preferred package size is less than 27 mm x 27 mm).

(3) If the material set is different, especially the solder joint materials, a large difference among the model prediction and the test results will likely be seen. The SAC405 solder joints will need a different acceleration model from that for eutectic SnPb solders.

(4) The variation of failure data collected and associated distribution analysis results make it more difficult to produce a universal model to predict the acceleration factor.

Future work will need to confirm some of the observations and provides a more precise AF model.

4.4 Summary

This Chapter discusses acceleration factor models used in solder joint reliability life prediction. The original model was developed by Norris-Landzberg in 1969. Although there are some adjustments through the years, the three stress factors considered in the model are still the same: temperature range, cycle frequency and the

maximum temperature respectively. The hypothesis is that the AF model is only affected by three stress factors associated with thermal cycling profiles.

However, there are few data available to validate the prediction results. In practice, most engineers conveniently use the traditional Norris Landzberg models even the parameters were developed many decades ago. So it is confusing what empirical models can be used to accurately predict the solder joint life in the use conditions.

Tremendous amount of data are collected using various package types and under many thermal cycle profiles. The experiment results clearly demonstrate that a huge error can be introduced if a model is used to predict all the solder joint fatigue life in the use conditions. AF models will vary if the package material changes and if the structure changes.

The AF models shall be validated and characterized for certain types of packages and materials set used in order to provide accurate life prediction.

5. FAILURE BOUND ESTIMATION AND FAILURE RATE MODELING

Semiconductor packages can fail in various stages of applications due to various failure mechanisms even they pass all required tests. A constant failure rate usually describes a majority of non-solder joint related package failures observed in accelerated tests or use applications. The failure rate is usually estimated by using a specific Chi-square value or the expected number of failures.

The focus of this Chapter is to discuss the statistical characteristics of the failures observed in tests or applications and estimate their confidence bounds. First, several methods used to estimate the failure bounds will be described, second, a new approach for the failure bound estimation will be proposed and then validated through case studies. The failure rate estimation based on the new approach will have physical meanings and will provide more meaningful information than that obtained using the specific Chi-square value. The conclusion will help with the understanding of the statistical meaning of the failures observed in stress tests or in the field applications. The methods will help correlate the failure rate obtained in tests with the field returns under use conditions.

5. 1 Introduction

5.1.1 Failure trends

The reliability of a semiconductor package is associated with many factors, including designs and structures, materials properties, processes, and use conditions. A standard stress-based testing approach is usually adopted to assess the reliability of the packages in the field. Different types of stress tests might be applied to activate different failure mechanisms, such as interface failures, fatigue failures, electromigration failures and corrosion failures.

In general, the number of failures encountered in qualification tests is few and even zero, the failure data in the field is not correlated with the failure rate estimation calculated based on a zero-failure approach using Chi-square values at specific confidence levels. Figure 5-1 shows examples of the field failures from Company A in a year. In addition, most field failures in the summary are not related to wear-out failures, instead they are random failures. It is appropriate to assume a constant failure rate when analyzing the failures in the field. The question is if a constant failure rate can be estimated for failures observed in accelerated stress tests. A Poisson process [Yang et.al, 2007; Shahrzad et al., 2008; Intel, 1999] can describe the number of failures in the field or in the accelerated stress tests.
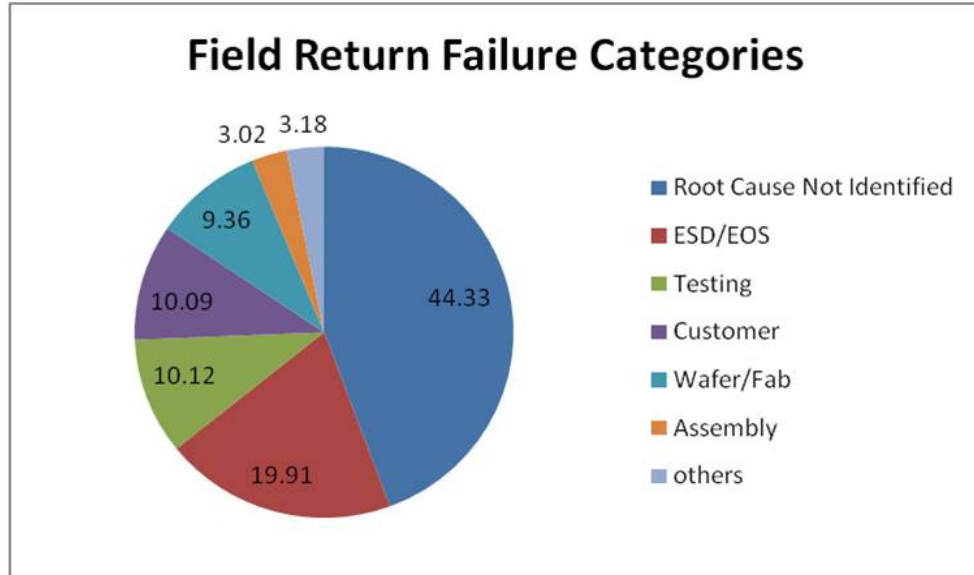
Figure 5-1 Field return failure distribution of Company A in a year [Yang et al.,

2007]

5.1.2 Failure rate modeling

The observation of failures is critical for reliability prediction and the failure rate pre-

diction. For random failures, the failure rate can be described by failure-in-time

(FIT), shown as

$$FIT = \frac{n_f}{N \cdot t \cdot AF} \times 10^9 \qquad\qquad (5.1)$$

Where n_f: the number of failures observed or expected. It can be the mean of the

Poisson distribution or the confidence bounds of the mean.

N: the total sample size;

t: the total test time or cycles;

AF : the acceleration factor for the failure mechanism.

It is obvious that a number of failures will be required to estimate the failure rate. However, there is a certain amount of risk brought about by the observation of one or more failures. Zero failure brings about a sense of security, but it is flawed to have an estimation of the failure rate when there is zero failure. There is also a risk drawing conclusions about a product when there are no failures observed.

To make a convenient case for a zero failure, the industry uses a half of the Chi-square values with a degree of freedom of $2n_f+2$ to calculate the failure rate, shown as

$$FIT = \frac{\chi^2_{(2n_f+2,1-\alpha)}}{2 \cdot N \cdot t \cdot AF} \times 10^9 \qquad (5.2)$$

Where α : the confidence level.

$\chi^2_{(2n_f+2,1-\alpha)}$: Chi-square value with a degree of freedom of $2n_f+2$ at a confidence level of α.

However, if there is zero failure, it is flawed to calculate the failure rate using a Chi-square value of degree of freedom of 2, because nothing is known about the failure distribution or failure mechanism with zero failures.

In order to assess the failure rate in the field application, the expected number of failures observed from the testing conditions must be estimated, and only then can the acceleration factors for the expected failure mechanisms be obtained.   Furthermore,

115

the estimation of the failure bounds then be estimated. The confidence bounds will help us evaluate the characteristics of the failure data as well as the trends of the failure rate and select the right approach for the reliability studies.

5.2 Theory

5.2.1. Poisson distribution and the confidence bounds of its mean

The number of failures can be analyzed by a Poisson distribution, which is used to deal with the occurrence of some random events in the continuous dimension of time and space, it can be expressed as Equation [5.3]

$$P(n_f, \lambda) = \frac{\lambda^{n_f} \exp^{-\lambda}}{n_f!}, \quad n_f = 0, 1, 2, 3..., \tag{5.3}$$

Where n_f: the number of failures

λ: The mean (rate) of the Poisson distribution, which represented the average rate of occurrence of the event of interest.

 A common inferential problem dealing with the Poisson distribution is the determination of the confidence bounds for λ. Several approaches are discussed below.

5.2.1.1 The exact method

Based on the definition, the lower and upper bounds of the mean of the Poisson distribution can be estimated as [Sahai and Khurshid, 1993]

For λ_L:

116

$$P(X \geq x | \lambda = \lambda_L) = \sum_{i=x}^{\infty} e^{-\lambda_L} \lambda_L^i / i! \leq \alpha / 2 \qquad (5.4)$$

For λ_U :

$$P(X \leq x | \lambda = \lambda_U) = \sum_{i=0}^{x} e^{-\lambda_U} \lambda_U^i / i! \leq \alpha / 2 \qquad (5.5)$$

Where λ_L : the lower bound λ

λ_U : The upper bound of λ ;

The problem with this method is the difficulty in computing the cumulative Poisson probability expression.

5.2.1.2 Shortcut approaches

In general, the shortcut methods are based on the square root transformation of a Poisson distributed variable, which is assumed to be a normally distributed variable.

The estimation of confidence bounds at a 95% confidence level can be expressed as [Vandenbroucke, 1982]

$$\left[\sqrt{n_f} \pm 1.96(0.50) \right]^2 \quad or \quad \left[\sqrt{n_f} \pm 1 \right]^2 \qquad (5.6)$$

A proposal to add one to the lower limit and two to the upper is shown as [Ury, 1985]

$$\left(n_f - 1.96\sqrt{n_f} + 1, n_f + 1.96\sqrt{n_f} + 2 \right) \qquad (5.7)$$

5.2.1.3 Chi-square method (χ^2)

A simple way to calculate the confidence bounds for the mean based on the relation between the Poisson distribution and the Chi-square distribution is shown as [Ulm 1990; Pearson et al., 1970]

$$\sum_{i=0}^{M-1} e^{-\lambda} \lambda^i / i! = 1 - \Pr\{\chi_{2n_f}^2 \leq 2\lambda\} = \Pr\{\chi_{2n_f}^2 > 2\lambda\} \tag{5.8}$$

and

$$\lambda_L = \frac{\chi_{(2n_f, \alpha/2)}^2}{2} \text{ and } \lambda_U = \frac{\chi_{(2n_f+2, 1-\alpha/2)}^2}{2} \tag{5.9}$$

A one-sided bound can be obtained by replacing $\alpha/2$ by α, which is most widely used in the failure rate calculation.

5.2.1.4 Normal distribution assumption

For a normal distribution, the 95% confidence bounds for the mean can be calculated in the following Equation [5.10]

$$\bar{X} \pm Z_{\alpha/2} \frac{s}{\sqrt{N}} \tag{5.10}$$

Where $\bar{X}$: the sample mean;

N: the sample size

s: the sample standard deviation

$Z_{\alpha/2}$: The standard normal value with an area of $\alpha/2$ to its right.

118

When the number of failures is very large (>100), the confidence bounds can be defined as

$$\left(n_f \pm Z_{1-\alpha/2} \sqrt{n_f} \right) \tag{5.11}$$

If the sample size is less than 30, the confidence bounds is calculated by

$$\bar{X} \pm t_{\alpha/2, N-1} \frac{s}{N}. \tag{5.12}$$

Where $t_{N-1,\alpha/2}$ is the t-distribution value with a degree of freedom of N-1.

It is necessary to collect the failure data in order to estimate the confidence bounds of the failures. If no failure were observed, there would be no knowledge of the failure mechanisms and accurate representation of the AFs. Therefore, any failure rates based on zero failures are questionable.

5.2.2 A proposal for confidence bounds for the number of failures observed

For the unknown population mean from a random sample drawn from the population, neither the normal nor the t-distribution statistical analyses can be used to estimate the bounds, instead the confidence bounds can be calculated using the Tchebycheff theorem [Papoulis, 1984], which states that regardless of the sample of the distribution used, the proportion of observations (or areas falling within m_z standard deviations of the mean) is at least $1 - \dfrac{1}{m_z^2}$, then

$$P\left\{ \bar{n}_f - m_z \frac{\sigma}{\sqrt{N}} < n_f < \bar{n}_f + m_z \frac{\sigma}{\sqrt{N}} \right\} \geq 1 - \frac{1}{m_z^2} \tag{5.13}$$

119

Where n_f : the number of failures.

$\bar{n}_f$: The average of number of failures.

σ : Standard deviation

N: total sample size

With more knowledge about the distribution, the tighter bounds can be attained.

Adopting the concept and reference from [Bartlett, 1955], the failure bounds for the number of failures can be described as

$$n_f \pm \frac{n_f}{\sqrt{n_f - 1}} \tag{5.14}$$

The Equation [5.14] can be used as another simplified option to estimate the confidence bounds for the number of failures.

5.3 Acceleration factor and failure rate modeling

5. 3.1 The acceleration factor estimation

It is impossible to test semiconductor packages in a real application due to the generic higher reliability of the packages; instead, the accelerated stress tests should be used in order to generate failures earlier. If the failure mechanism is consistent between field application conditions and the accelerated test conditions, then the acceleration factor models can be developed to estimate the reliability life and the failure rate of the packages in the field.

The acceleration factor of combined stress factors can be the product of the acceleration factor for individual test stress factor, as described in Chapter 4, as long as the failures can be attributed to the same failure mechanism.

In many applications, the acceleration factors calculated are often based on the historical data for the E_a and other parameters, which might not be accurate especially with advancements in the material development processes. In many conditions, new characterization should be done to verify the model parameters.

5.3.2 AF modeling for multiple failure mechanisms

It is well documented that the acceleration factors for a single failure mechanism can be the product of individual acceleration factors under specific stress factors, e.g. the total acceleration factor under temperature and voltage stresses can be expressed as

$$AF = AF_v . AF_t \qquad (5.15)$$

Where AF_t is the acceleration factor for temperature stress;

AF_v is the acceleration factor for voltage stress.

In reality, if there are two or more failure mechanisms, the calculation for the total AF will not be straightforward.

Assume FM_1 and FM_2 are two failure mechanisms observed in an accelerated stress test. For failure mechanism I, the number of failures observed is n_{f1}; for failure mechanism II, the number of failures observed is n_{f2}, the acceleration factors are calculated for the two failure mechanisms, assuming AF_1 for FM_1 and AF_2 for FM_2

The total AF can be expressed as

$$AF = \frac{AF_1 \cdot AF_2 \chi^2_{(2(n_{f_1}+n_{f_2})+2,1-\alpha)}}{AF_1 \cdot \chi^2_{(2n_{f_2}+2,1-\alpha)} + AF_2 \cdot \chi^2_{(2n_{f_1}+2,1-\alpha)}}$$

$$\text{Or} \quad AF = \frac{AF_1 \cdot AF_2 \cdot (n_{f_1}+n_{f_2})}{AF_1 \cdot n_{f_2} + AF_2 \cdot n_{f_1}} \tag{5.16}$$

Where n_{f_1} and n_{f_2} can be the number of failures observed or expected.

If $n_{f_1} = n_{f_2} = 0$, then there is no failures observed. There is no meaning to calculate the AF. Mathematically, it can be expressed as (using Chi-square expression)

$$AF = \frac{AF_1 \cdot AF_2}{AF_1 + AF_2} \tag{5.17}$$

If $n_{f_1} = 0; n_{f_2} \neq 0$ or $n_{f_2} = 0; n_{f_1} \neq 0$, then there is only one failure mechanism, so

$$AF = AF_1 \quad or \quad AF_2.$$

If $n_{f_1} \gg n_{f_2}$ or $n_{f_2} \gg n_{f_1}$, it can be assumed there is one dominant failure mechanism, then $AF = AF_1 \quad or \quad AF_2$

If $n_{f_1} = n_{f_2}$, then

$$AF = \frac{2AF_1 \cdot AF_2}{AF_1 + AF_2} \quad \text{Or} \quad AF = \frac{AF_1 AF_2 \cdot \chi^2_{(4n_{f_1}+2,1-\alpha)}}{(AF_1 + AF_2) \cdot \chi^2_{(2n_{f_1}+2,1-\alpha)}} \tag{5.18}$$

The number of failures observed from the accelerated stress testing or its bounds can replace the Chi-square value.

In many cases, there is only one dominant failure mechanism even if there are multiple failure mechanisms observed, in which case the calculation can be simplified to serve as a model for single failure mechanisms.

5.4 Case studies

In order to estimate the failure rate at random failures, first, the number of failures shall be available or their bounds must be estimated. As discussed, there are some issues with the Chi-square approach. Second, the acceleration factors between the stress test conditions and the use conditions must be determined. The acceleration factor is usually calculated from either an empirical formula. If the uncertainty of the acceleration factor is large, the failure rate calculated will be meaningless. It is important to obtain an accurate acceleration factor between the test conditions and the use conditions.

In order to obtain enough failure data under the test conditions, the test intervals must be selected to allow for an accurate mathematical representation of the failures through the entire stress period. Large number of samples must be selected to represent the population. A minimum of 3 to 5 test intervals must be defined for each test condition over the stress period. During the test, within each test interval, at least 1 to 3 failures are preferable to be obtained; the more failures that are observed, the better the estimation of the failure rate will be. In the following sessions, several case studies are discussed. All the tests are done on the package level, which means the

studies do not focus on the second level solder joint failures that are well-known for their wear-out fatigue failures.

5.4.1 Reliability and failure rate estimation of RCPs

Figures 5-2 and 5-3 show the schematic diagram and bottom view of the RCPs used in the test. The experiments are conducted using a test-to-failure approach under thermal cycling conditions. The units are taken out for functional testing at an interval of 250 cycles. The functional failures detected will be analyzed to determine the failure mechanism. The conditions of temperature cycling tests are -40 ^{o}C to 125 ^{o}C, and -65 ^{o}C to 150 ^{o}C. The number of failures observed is listed in Table 5-1. The key failure mechanism is Cu trace cracking (Figure 5-43) in the dielectric layers, there can be multiple cracks in each sample, the number of failures is counted by the number of samples failed, not the number of the cracks. Sometimes the cracking can even go deeper into the silicon to cause further damage (Figure 5-5).
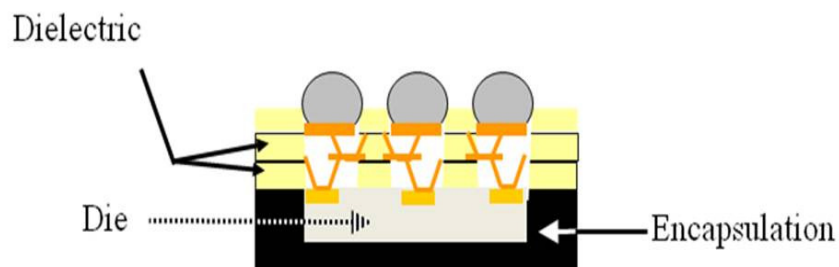
Figure 5-2 Schematic stack-up structure of RCPs
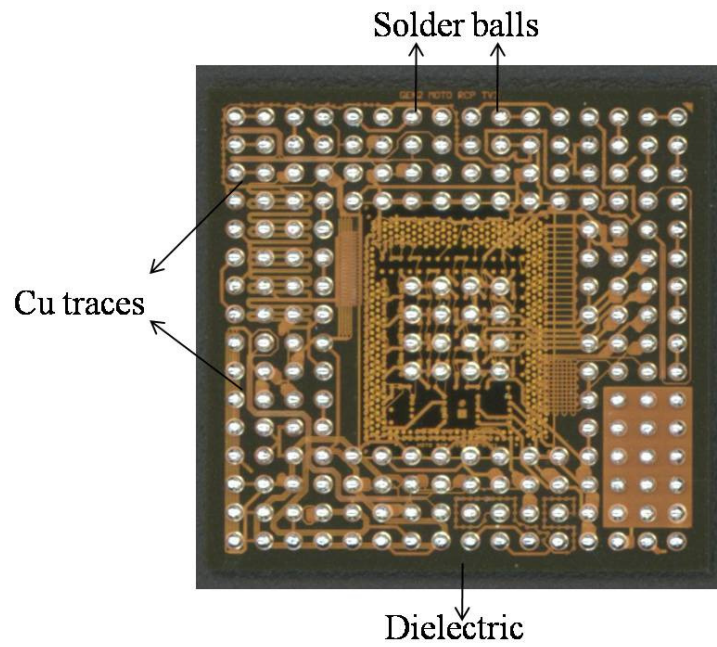
Figure 5-3 Bottom view of the RCP package
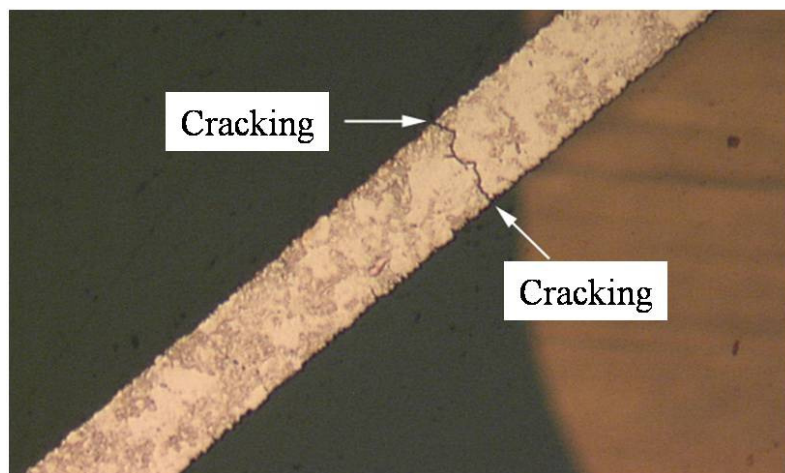
Figure 5-4 Cracking trace in the dielectric
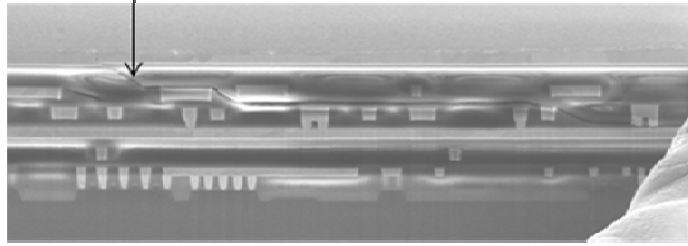
Figure 5-5 Cracks cutting into the die (Focus-ion-beam image)

Table 5-1 Reliability testing results of RCPs

Temperature Cycling Intervals	Number of Failures	
	-40 ^{o}C/125 ^{o}C	-65 ^{o}C/150 ^{o}C
0-250 cycles	0	0
250-500 cycles	0	3
500-750 cycles	2	2
750-1000 cycles	1	1
1000-1250 cycles	3	4
1250 -1500 cycles	0	3
1500-1750 cycles	1	1
1750 -2000 cycles	2	2
2000 cycles+ (censored)	410	390

5.4.1.1 Failure characteristics

Using MINITAB, the failure data is plotted in the Weibull and exponential distributions, (Figures 5-6 and 5-7). The Weibull plot typically can fit well with any kinds of failure data, however, it is not a specific distribution to describe a particular failure

rate. For instance, exponential distribution is best fit for a constant failure rate and

lognormal distribution is best fit for wear-out fatigue failures.
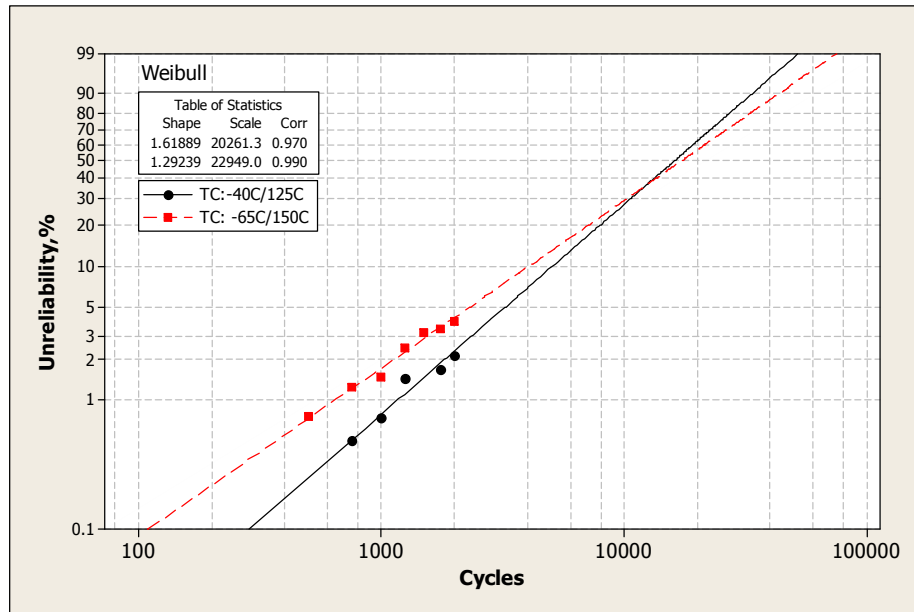
Figure 5-6 Weibull distribution plot of the failure data observed in RCPs
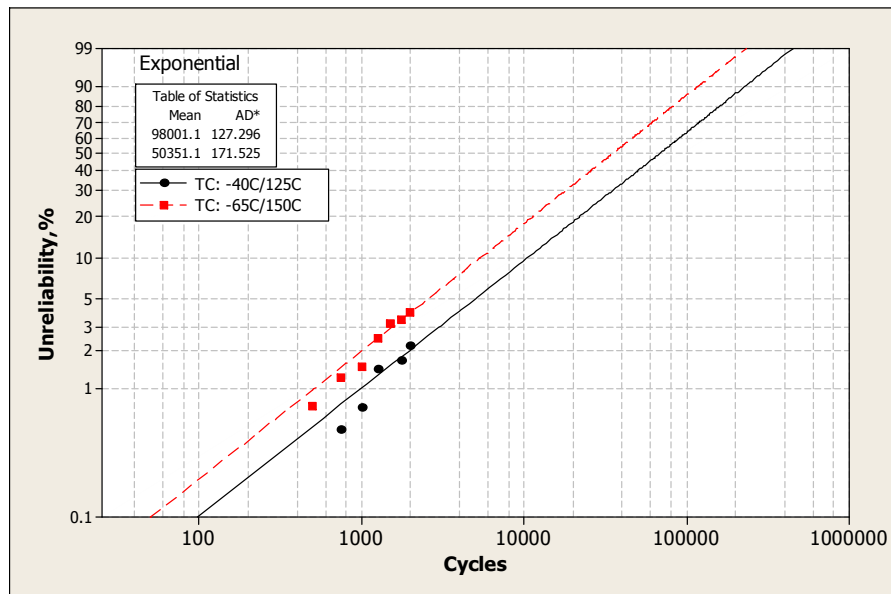
Figure 5-7 Exponential distribution plot of the failure data observed in RCPs

127

The failure data under -40 ^{o}C/125 ^{o}C and -65 ^{o}C/150 ^{o}C fit well in both Weibull and

Exponential distributions. The shape parameter β in the Weibull plot is around 1-

1.6, showing a weak trend of an increasing failure rate. The failure data can be

processed as a constant failure rate indeed since the exponential distribution can de-

scribe the failure data very well, the Mean-Time-to-Failure (MTTFs) under the two

test conditions (in exponential distribution) are 98001 cycles and 50350 cycles re-

spectively.

5.4.1.2: AF and failure rate estimation

The acceleration factor between the thermal cycling conditions of -40 ^{o}C/125 ^{o}C and

-65 ^{o}C/150 ^{o}C is expressed as

$$AF = \frac{98001}{50350} = \left(\frac{215}{165}\right)^{n}, \text{ so the constant } n = 2.52$$

The acceleration factor model will be written as

$$AF = \left(\frac{\Delta T_{test}}{\Delta T_{use}}\right)^{2.52} \tag{5.19}$$

Assuming a constant failure rate, Table 5-2 lists the comparison of the failure rate

calculated from Chi-square, the number of failures observed, and the bound estima-

tion using the $n_f \pm n_f / \sqrt{n_f - 1}$ approach.

Table 5-2 Failure rate estimation

TC conditions	Total # of Failures, n_f	Failure Rate Calculation, FIT		
		Average Failure Rate using n_f	Failure rate by χ^2 (upper limit)	Failure rate limits $\left(n_f \pm n_f / \sqrt{n_f - 1}\right)$
-40 $^{\circ}$C/125 $^{\circ}$C	9	10817	18876	(7000, 14640)
-65 $^{\circ}$C/150 $^{\circ}$C	16	20018	30380	(14850, 25200)

Apparently, the Chi-square approach gives a higher failure rate estimation in comparison to other approaches. The $\left(n_f \pm n_f / \sqrt{n_f - 1}\right)$ approach provides a much tighter

bound estimation of the failure rate. Additionally, if one uses the qualification test

conditions and durations, e.g. under -40 $^{\circ}$C /125 $^{\circ}$C thermal cycling conditions for

1000 cycles, the failure rate using $n_f = 3$ is calculated to be 7317 FIT; and 37805 FIT

using Chi-square value with degree of freedom of 8 and 12491 FIT using the new

$\left(n_f \pm n_f / \sqrt{n_f - 1}\right)$ approach. The failure rate estimation is different from the results

after 2000 cycles (Table 5-2). It demonstrates that a test-to-failure approach will help

provide a tighter interval since there are more failures observed over time. The more

failure data that is collected, the more accurate the estimation of the failure rate will

be.

Table 5-3 demonstrates the bounds for the number of the failures observed. Obvious-

ly, the approach using $\left(n_f \pm n_f / \sqrt{n_f - 1}\right)$ is much tighter than other approaches.

Table 5-3 Confidence bounds estimation using various approaches

TC & n_f	Confidence Limit for n_f				
	$n_f - 1.96\sqrt{n_f} + 1,$ $n_f + 1.96\sqrt{n_f} + 2$	$\left(\sqrt{n_f} \pm 1\right)^2$	$\left(\sqrt{n_f} \pm 1.96/2\right)^2$	$\chi^2_{(2n_f,\alpha/2)},$ $\chi^2_{(2n_f+2,1-\alpha/2)}$	$\left(n_f \pm n_f / \sqrt{n_f - 1}\right)$
-40 °C/125 °C, 9	4,16	4,16	4,16	4,17	6,12
-65 °C/150 °C, 16	9,25	9,25	9,25	10,25	12,20

5.4.2 Reliability and failure rate analysis of FCMMAP modules

The FCMMAP package studied in this case is one type of system-in-package (SiP) module, the device is designed as a daisy chain device in order to monitor the integrity of the package structure during the accelerated stress testing. The package cross-section is shown in Figure 5-8. Temperature cycling tests are conducted to study the reliability performance of the module, and Table 5-4 summarizes the failure data collected. The dominant failure mechanisms are an interface delamination failure seen in the silicon (Figure 5-9) and the bump failures. The failure mode is open failures.
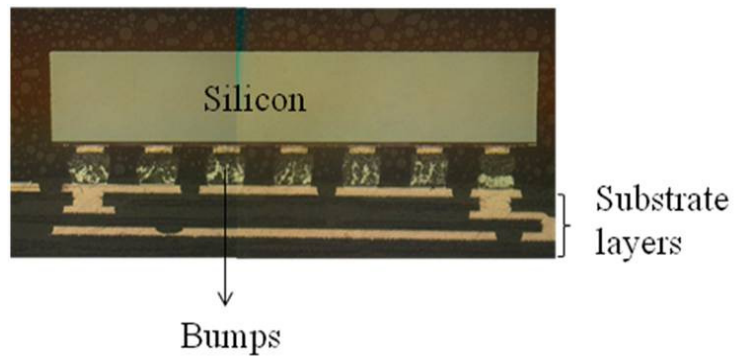
Figure 5-8 FCMMAP module cross section
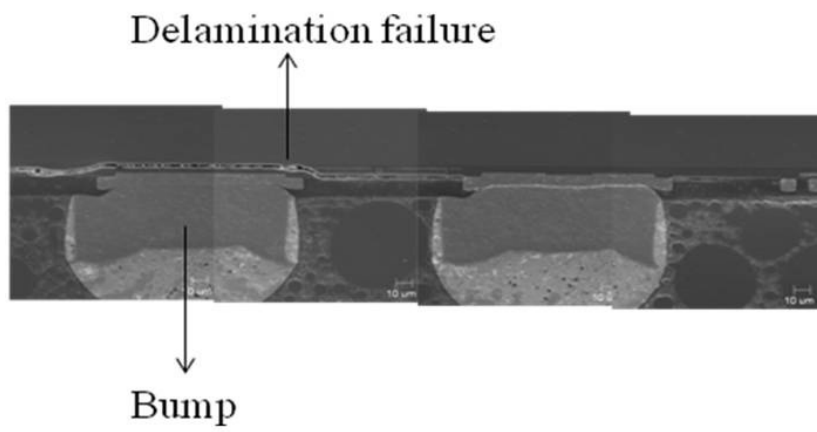
Figure 5-9 Delamination failures seen in silicon

Table 5-4 Failure data for FCMMAP modules

Temperature Cycling Intervals	Number of Failures	
	-40 ^{o}C /125 ^{o}C	-65 ^{o}C/150 ^{o}C
0-250 cycles	0	0
250-500 cycles	0	0
500-750 cycles	1	11
750-1000 cycles	2	7
1000-1250 cycles	0	0
1250-1500 cycles	2	0
1500-1750 cycles	3	4
1750-2000 cycles	1	5
2000 cycles + (censored)	119	180

5.4.2.1 Failure distributions

The failure distribution analysis of Weibull and exponential distributions are shown in Figures 5-10 and 5-11. From the Weibull plot, clearly two different failure rate trends are observed. The failure data observed under -40 ^{o}C/125 ^{o}C shows an increasing failure rate where the shape parameter $\beta > 1$, however an approximate constant failure rate is shown for the failure data under -65 ^{o}C/150 ^{o}C conditions, where $\beta \approx 1$. The failure data under -40 ^{o}C/125 ^{o}C does not fit very well in the exponential distribution.
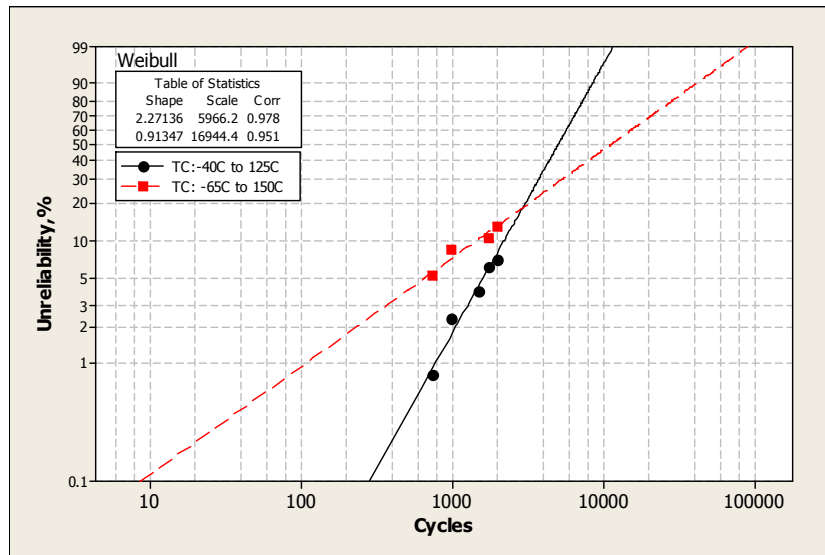
Figure 5-10 Weibull plot of the failure data (FCMMAP)
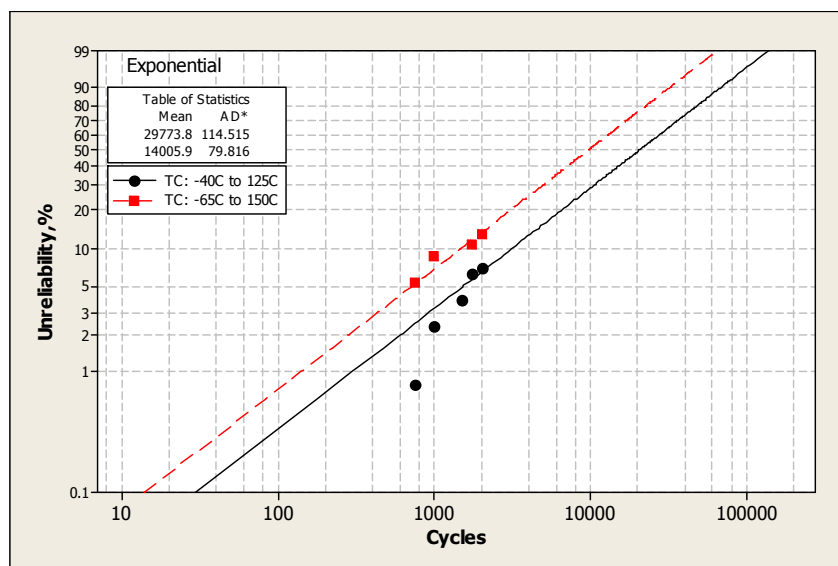
Figure 5-11 Exponential plot of the failure data (FCMMAP)

5.4.2.2 Failure bound estimation

The failure rates are the reverse of the MTTF value of exponential distribution and are summarized in Table 5-5.

Table 5-5 Failure rate estimation

TC Conditions	Total # of failures, n_f	Failure Rate Calculation, FIT		
		Average Failure Rate Using n_f	Failure Rate by χ^2	Failure Rate Intervals $\left(n_f \pm n_f / \sqrt{n_f - 1}\right),$
-40 ^{o}C/125 ^{o}C	9	35156	61328	(22726, 47586)
-65 ^{o}C/150 ^{o}C	27	65217	89928	(52427,78007)

As shown in previous section, the calculation based on the Chi-square estimation

gives a high failure rate which means that the bounds are wider,   as shown in Table

5-6, Chi-square gives the widest bounds, and $\left(n_f \pm n_f / \sqrt{n_f - 1}\right)$ provides the tightest

bounds, which is better.

Table 5-6 Failure bound estimation for FCMMAPs

TC & n_f	Bounds l for n_f				
	$n_f - 1.96\sqrt{n_f} + 1,$ $n_f + 1.96\sqrt{n_f} + 2$	$\left(\sqrt{n_f} \pm 1\right)^2$	$\left(\sqrt{n_f} \pm 1.96/2\right)^2$	$\chi^2_{(2n_f, \alpha/2)},$ $\chi^2_{(2n_f+2, 1-\alpha/2)}$	$\left(n_f \pm n_f / \sqrt{n_f - 1}\right)$
-40 ^{o}C/125 ^{o}C, 9	4,16	4,16	4,17	4,16	6,12
-65 ^{o}C/150 ^{o}C, 27	18,38	18,38	18,39	16,39	22,32

5.4.3 Reliability testing on Power Quad Flat Non-lead (PQFN) packages

A different package technology, PQFN packages (Figures 5-12 and 5-13), is tested to evaluate the reliability. The package technology has been qualified using the standard qualification tests and the results are clean (Table 5-7).

Table 5-7 PQFN product qualification summary

Stress Tests	Test Conditions	Results (#Rej/SS)
Highly Accelerated Stress Test	130 ^{o}C/85%RH; 96 hrs	0/231 (3 lots)
Temperature Cycling	-65 ^{o}C to 150 ^{o}C; 500 cycles	0/231 (3 lots)
High Temperature Storage	175 ^{o}C; 504 hrs	0/144 (2 lots)
High Temperature Life Operating	Ta=150 ^{o}C; 408 hrs	0/231 (3 lots)
Early Life Failure Rate	Ta=150 ^{o}C; 24 hrs	0/2400 (3 lots)
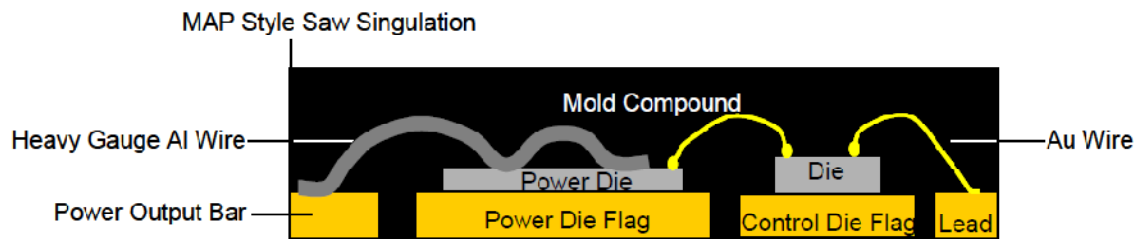
Figure 5-12 PQFN cross section diagram
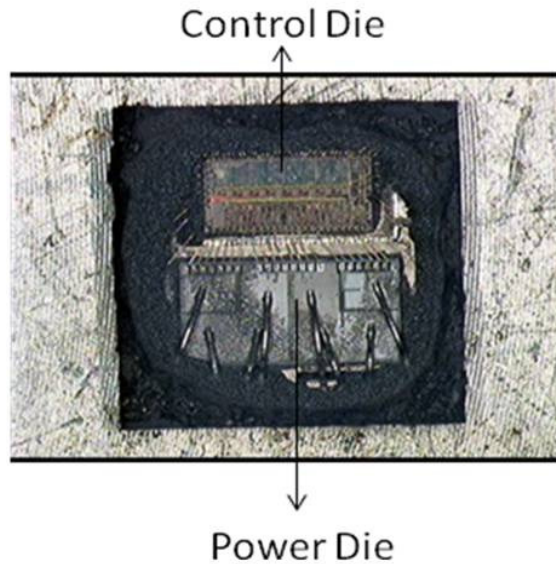
Figure 5-13 Top view of PQFN packages

Temperature cycling tests of two test conditions are applied to the samples. Table 5-8 shows the failure data summary. Interestingly and not surprisingly, many failures show up after 1000 cycles.

All of the failures are due to current sense failure (a functional failure), which is caused by the silicon degradation. The failure data is analyzed and fit into the Weibull plot (where the shape parameter β *is* > 7), which shows a very strong, worn-out failure mechanism (Figure 5-14).

Table 5-8 Failure data for PQFN package (current sense failure)

Temperature Cycling Intervals	Number of Failures	
	-50 ^{o}C/150 ^{o}C	-65 ^{o}C/150 ^{o}C
0-250 cycles	0	0
250-500 cycles	0	0
500-750 cycles	0	0
750-1000 cycles	0	0
1000-1250 cycles	1	4
1250-1500 cycles	2	16
1500-1750 cycles	8	18
1750-2000 cycles	13	11
2000 cycles + (censored)	25	0
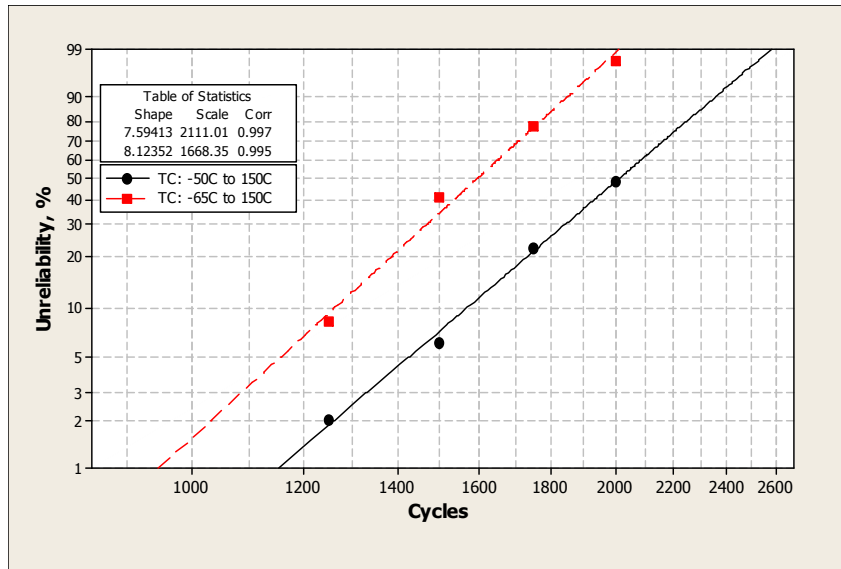
Figure 5-14 Weibull plot for the PQFN failures during thermal cycling test

The failure distribution analysis is summarized in Table 5-9. The Weibull plots under the two test conditions are in parallel which means the same failure mechanism in this case.

Table 5-9 Weibull plot data summaries for the PQFNs

TC Condi-tions	Cycles-to-Failures (CI @ 95% CL)				
	1% Failure	2% Failure	5% Failure	MTTF	Characteristic life, η
-50 ^{o}C /150 ^{o}C	1152 (929-1429)	1263 (1054-1513)	1428 (1247-1634)	1983 (1878-2094)	2111 (1985-2244)
-65 ^{o}C to 150 ^{o}C	969 (839-1119)	1051 (928-1190)	1170 (1060-1292)	1559 (1497-1624)	1649 (1589-1710)

The acceleration factor will be estimated based on the Coffin Manson model, where

$$AF_{\Delta T} = \left(\frac{\Delta T_t}{\Delta T_a} \right)^n$$. Here $\Delta T_t = 215\ ^oC$ and $\Delta T_a = 200\ ^oC$. If using the η value (63.2%

fail) as the criterion, then the power exponent n is calculated to be 3.25. Similarly, when the cycles to 1% cumulative failure percentage (CFP) are used, $n = 2.39$. The dependence of the n value on the CFP percentage is summarized in Table 5-10 and is not significant.

Table 5-10 n value using various CFP percentage

Parameters	AF Parameters (Coffin-Manson Model)			
	1% Failure	2% Failure	5% Failure	η (63.2% fail)
AF	1.19	1.2	1.22	1.27
n value	2.39	2.54	2.76	3.25

During the qualification tests of the PQFN packages, the passing condition is 500 cycles @ -65 °C/150 °C with zero failure. Assuming the failure data follows a constant failure rate and if we use a Chi-square approach, where $\chi^2_{(2,0.05)} = 5.99$, then the failure rate can be calculated as 26043 FIT. If we assume that a reasonable AF is 14, then the failure rate in the field is about 1929 FIT. However, by using the test-to-failures approach, it is obvious that the failure is increasing and that the assumption of using a constant failure rate is not appropriate, then the failure rate at 500 cycles using a Weibull analysis will be around 910 FIT under testing conditions and approximately 65 FIT at use conditions. There is a large difference in the failure rate estimation between using a constant failure rate approach and using the actual increasing failure rate approach.

A different product is packaged in a similar PQFN platform. Some of the data observed under isothermal air-to-air thermal cycling is shown in Table 5-11.

Table 5-11 Isothermal cycling results of PQFN parts

Test Types	Test Duration	Fail/Pass	Failure Mode
Thermal Cycling (-65 °C to 150 °C)	200 cls	1/239	IGSS failure
	500 cls	2/237	IGSS failures
	1000 cls	1/236	IGSS failure

The failure analysis has concluded that a silicon manufacturing defect (poor PHV implant) led to IGSS and IDSS leakage. The failures are randomly distributed and can

be expressed as exponential distributions $(\beta \approx 1)$ (Figure 5-15). CSE failures are also

plotted in Figure 5-15 (@-65 ^{o}C/150 ^{o}C) for comparison.
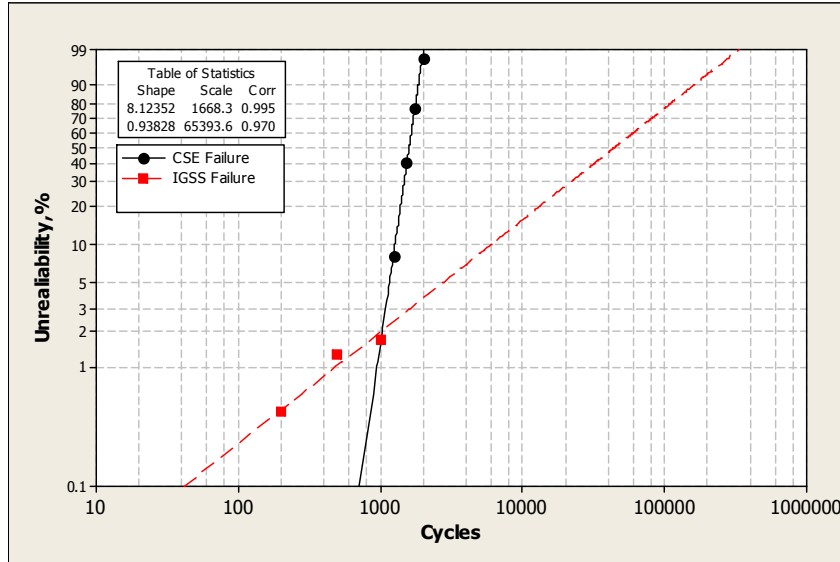
Figure 5-15 Failure data probability plot (two failure mechanisms)

Figure 5-15 clearly shows two failure mechanisms. The shape parameter β of the

Weibull distribution is 0.94 for IGSS failures, showing an approximate constant fail-

ure rate.   The failure rate is estimated to be $4 \times 10^9 / N \cdot t$ =16800 FIT under the stress

conditions. The exponential distribution fitting gives a FIT value of 19140. Howev-

er, the Chi-square estimation will give a failure rate of 38284 FIT which is much

higher than expected.

 5.4.4 Field failures of products (PLCC packages)

Field failures of PLCC packages are studied in this section. The number of failures

from two lots is summarized in Table 5-12. There are a total of eight failures in Lot 1

and five failures in Lot 2, and the maximum life data available in the field is ten

140

months. The failure analysis is completed with the returned parts and all of them showed voids at the interface of the metallization contacts in the silicon, a stress migration failure phenomenon due to defects in silicon manufacturing. The total samples in the field are 30,000.

Table 5-12 Field failure summaries for PLCC packages

Months in the field	Number of Failures		Note
	Lot1	Lot2	
1	1	0	Failure Mechanism is stress induced voiding.
2	0	0	
3	0	0	
4	1	0	
5	3	0	
6	0	1	
7	1	0	
8	1	2	
9	1	1	
10		1	
Total units shipped	5000	25000	Total units:30,000

A thermal cycling test was conducted and the same failure mechanism was observed with respect to the field failures. Under a thermal cycling condition of -65 ^{o}C to 150 ^{o}C, there are two failures observed out of a total of160 units tested. The use condition is assumed to be from 0 ^{o}C to55 ^{o}C.

5. 4.4.1 Failure distribution

The failure data from the field is plotted in the Weibull and Exponential papers (Figures 5-16 and 5-17). When analyzing the data using a Weibull analysis, the shape parameter β is around 1.2 which is very close to 1(showing a good fit in the exponential plot). The characterization life η is estimated to be 5862 months. When using exponential distribution analysis, the failure data fit well with the straight line, with a failure rate of 61 FIT (/unit.hr) from the distribution.
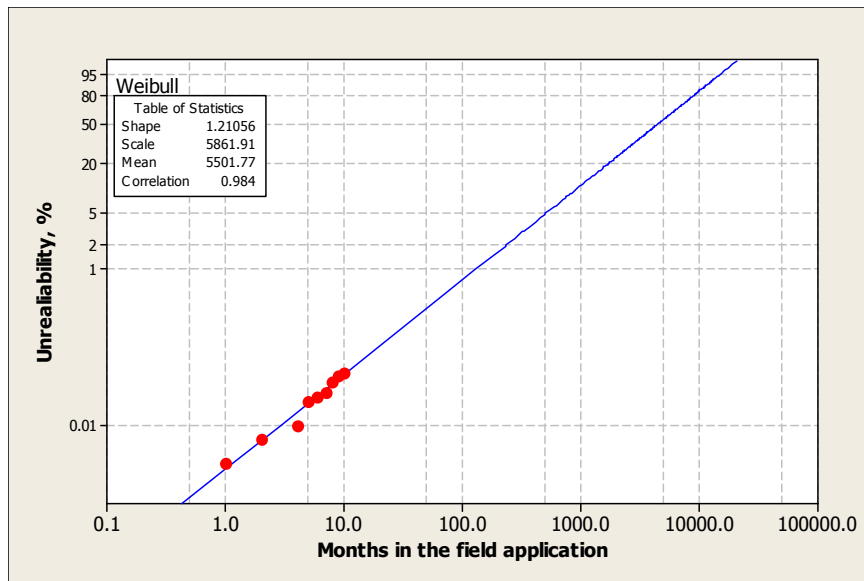
Figure 5-16 Weibull distribution of the failures of PLCC packages
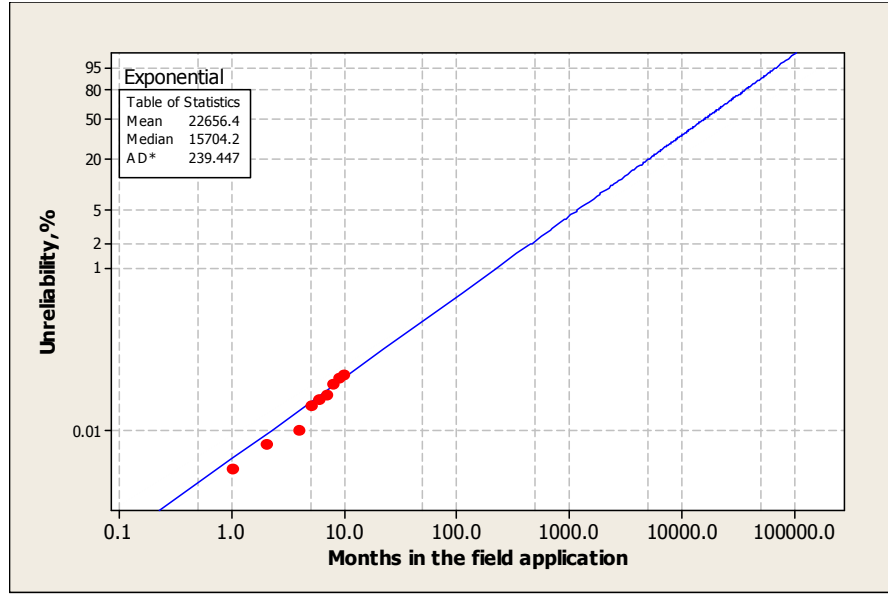
Figure 5-17 Exponential distribution of failures of PLCC packages

5.4.4.2 Failure rate estimation

For a Weibull analysis, the failure rate will be dependent on the time in the field application and can be expressed as.

$$Failure\ Rate(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} \tag{5.21}$$

When t=10 months,

$$Failure\ rate(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} = 75FIT$$

Assuming the failure follows an exponential distribution, and using a standard failure rate definition, the number of failures is 13, the total unit time can be estimated at

143

30000*10*30*24 for 10 months of field life, and the failure rate can be estimated to be

$$FIT = \frac{Number\ of\ Failures}{Total\ unit\ time} = \frac{13}{30000 \times 10 \times 30 \times 24} \times 10^9 = 60.2$$

Using the half of the Chi-square value, the failure rate can be expressed as

$$FIT = \frac{\chi^2_{(26+2,0.05)}}{2 \times Total\ unit\ time} = \frac{41.34}{2 \times 30000 \times 10 \times 30 \times 24} \times 10^9 = 95.7$$

Obviously, using the failure rate calculated from the Chi-square value always overestimates the failure rate in comparison to the expected failure rate. The approach using the proposed approach gives a 78 FIT, which is closer to the measured mean data.

5.5 Discussions and summary

Semiconductor components can fail for many reasons. In some cases, the failures can be due to the defects in design or materials used, in other cases, the failures can be due to the defects in manufacturing and the environmental conditions. Typically, the majority of the field failures are defect driven and largely due to design, whereby structure and materials are often eliminated or reduced through design for reliability (DFR) practices or relentless reliability tests. Case studies demonstrate that exponential distribution is appropriate for analyzing the failure data from field applications or stress tests.

It is easy to plot any failure data in certain probability plots, like Weibull and Exponential distributions. However, it is important to review the failure data and decide what failure distribution will be used for the analysis. A shoot-from-the-hip approach will produce confusing results. It is necessary to obtain the failure trend or failure rate analysis.

In the industry, failure rate estimation typically will be done even without failures observed, by adopting the $\chi^2_{(2n_f+2,1-\alpha)}/2$ method to replace the observed or expected number of failures. However, it is impossible to start any distribution analysis when there is zero failures observed. There will be no knowledge about the failure mechanism and failure trends with zero failures. In order to have reasonable prediction of the failure rate, it is important to have at least 2-3 failures to start with. Moreover, the confidence bounds of the number of the failures can be estimated using the $n_f \pm n_f/\sqrt{n_f-1}$ approach. Testing and field results show that the new approach provides the tightest confidence bound based on the number of failures observed. It can provide better interval estimation for the failure rate as well. In addition, the estimation of the confidence bounds will provide us with a more realistic estimation for the failure rate, instead of the point estimation or the upper bound using the Chi-square value.

6. RELIABILITY ASSESSMENTS USING A KNOWLEDGE-BASED TEST APPROACHES

6.1 Introduction

During accelerated stress tests, the types of stress tests are chosen based on expected failure mechanisms, use conditions and package materials. The test conditions are usually based on JEDEC standards or the lifetime required of the package in the field.

Typically, the objectives of reliability studies are to assess the reliability, understand the failure mechanisms, fix the design/material/process issues if there are any, and improve the overall reliability performance of the package. It is preferred that qualification tests are completed with zero failures.

If there are zero failures at the end of the qualification tests, it does not demonstrate there will be zero failures in the field. Indeed, with zero failures, it is impossible to gain much knowledge about the failure mechanisms in field applications, let alone estimate acceleration factors and predict the failure rate. The worst scenario is using reliability models based on zero failures to predict the use life in the field with no knowledge of the actual failure mechanisms.

The disadvantage for the stress-based package reliability approach is that the tests are not designed to collect failure data and develop reliability models associated with the failure mechanisms. In reality, the same tests will be conducted again and again

when new packages are developed. However, little knowledge will be obtained about the lifetime of the applications in the field.

In order to assess and predict the reliability and failure rate in field conditions, the reliability studies shall focus on testing the packages to the point of failures. The failure information can then be used to evaluate the reliability life margin, and predict the failure rate characteristics.

In this Chapter, the test-to-failure approaches will be applied to the package development activities. One case will focus on a high density thermally enhanced BGA (TEBGA) package development, another case will focus on the reliability assessments of RCP packages. The studies will demonstrate that the test-to-failure approach provided much more information than the traditional approaches. In addition, the data will help us to fully characterize the reliability performance of the package technologies.

6.2 Reliability assessment and prediction of TEBGA packages

6.2.1 Introduction

The TEBGA package technology utilizes a build-up substrate in which the circuitry is built on the top of a copper heat spreader. High density micro-vias are manufactured to connect different layers in the substrate. The stiffness of the copper heat spreader will reduce the substrate warpage, then improve the yield and board level reliability. A strong interface adhesion is presented among the dielectric layers, copper metallization and the heat spreader. The majority of the substrate thickness is copper heat

147

spreader. The silicon processes used in the test vehicles are Cu interconnects and low-k dielectrics.

The package and the cross section views of a TEBGA package using the wire bonding technology are shown in Figures 6-1 and 6-2.   The packages possess a high thermal dissipation capability and can dissipate upto fifteen watts at a case temperature of 115 ^{o}C.   The complexity of the silicon device (8-layer metallization) and substrate structures (up to four layers) present many challenges for the package to meet the designed reliability performance.   With little knowledge about the interactions between the new substrate technology and the complex silicon technology available, the package posts a high level of reliability risks. Table 6-1 shows the comparison of different cavity down substrates. The inner layer dielectric (ILD) delamination and cracking failures are shown in Figures 6-3 to 6-6. A large number of failures is observed during the pre-certification tests, as shown in Table 6-2. All of the failures are due to die cracking and inner layer dielectric cracking. Table 6-3 listed the possible failure mechanisms in the TEBGA technology.
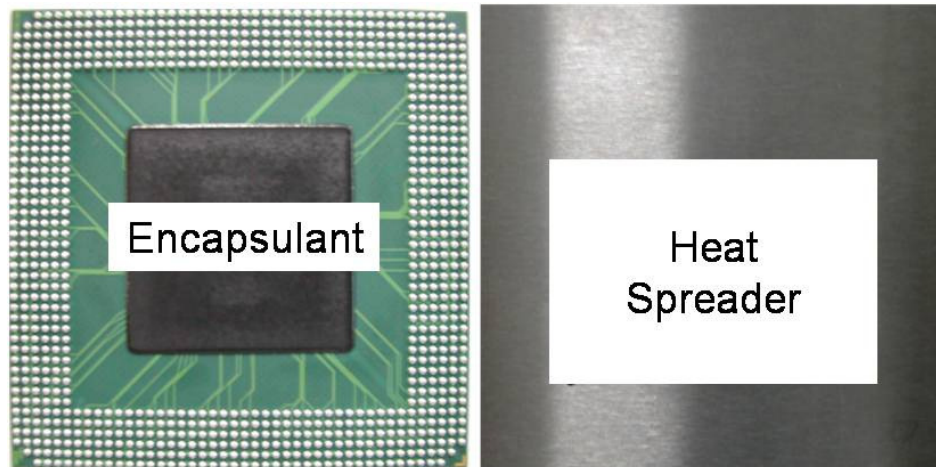
Figure 6-1 Top and bottom view of TEBGA packages
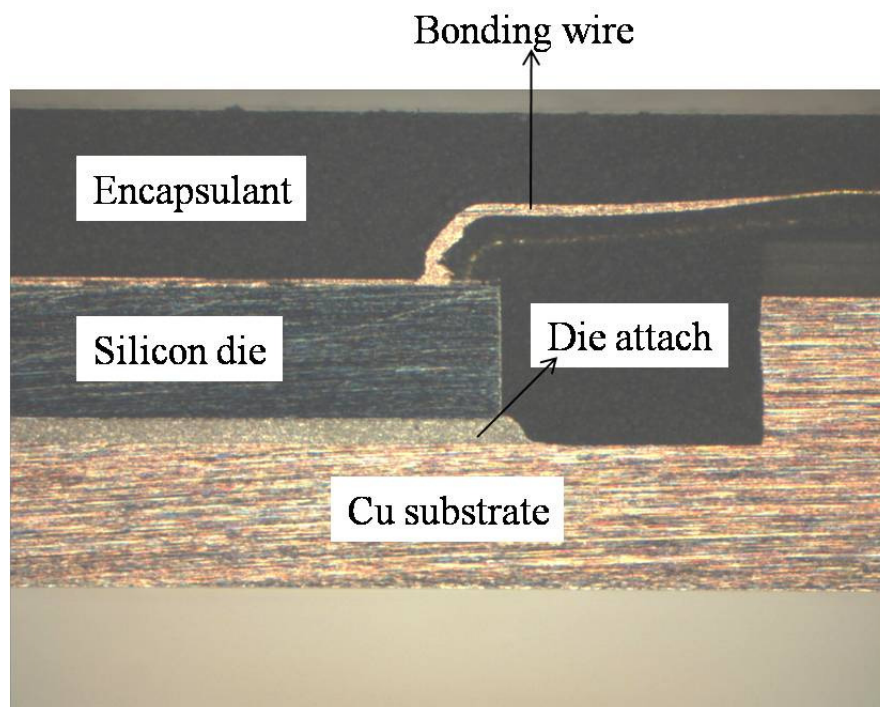
Figure 6-2 A cross section image of a TEBGA package [Yang and Bernstein, 2008]

Table 6-1 Comparison of various types of TEBGA packages

Category	Laminate (BT Pre-preg) TEBGA	Tape TEBGA	Build-up TEBGA
Concept	Multi-layer Circuits laminated to stiffening ring, then to a heat spreader	Single or two metal layer tape laminated to a heat spreader	Multi-layer build-ups on a heat spreader
Dielectric Tg, ° C	180	375	175
Moisture absorption, %	0.4	2.4	1.6
Dielectric thickness, µm	50	50	32
Circuit adhesive	Required	Not required	Not required
Stiffener	Not required	Required	Not required
Via diameter, µm	250	50	100
Via capture pad, µm	400	165	200
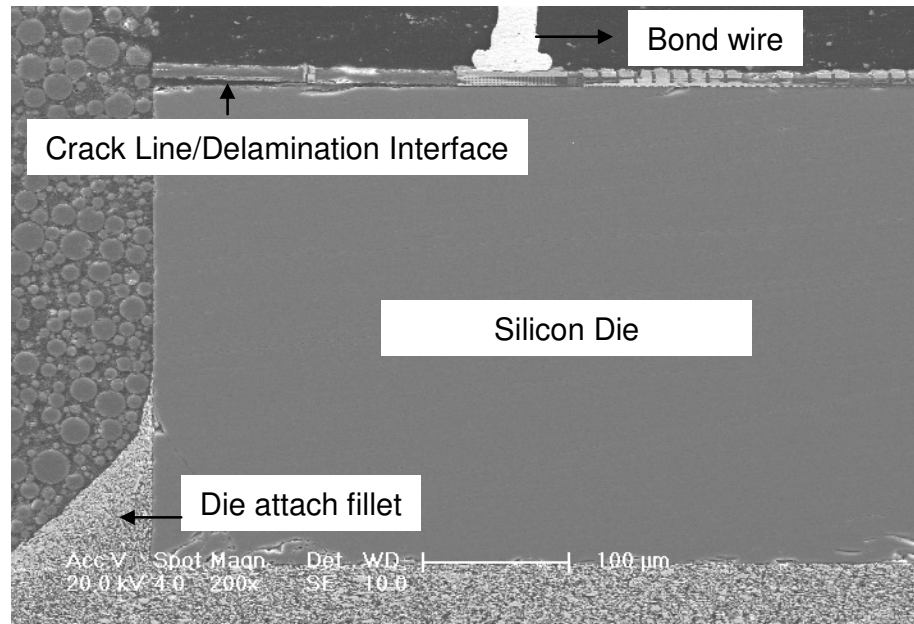
Figure 6-3 A cross section view of thin film cracking/delamination

Table 6-2 Die/thin film cracking failures observed in pre-qual tests

Test	No. of Failures	Failure Description	Note
TC "B" (-55 ^{o}C/125 ^{o}C)	7 failures	Opens and shorts.	250 Cycles
	4 failures	Opens and shorts.	500 cycles
UHAST 130 ^{o}C/85% RH	2 failures	opens	96 hours
	1 failure	Short to VCC/GND	168 hours
HTS 150 ^{o}C	1 failure	open	250 hours
	2 failures	Open and short	500 hours
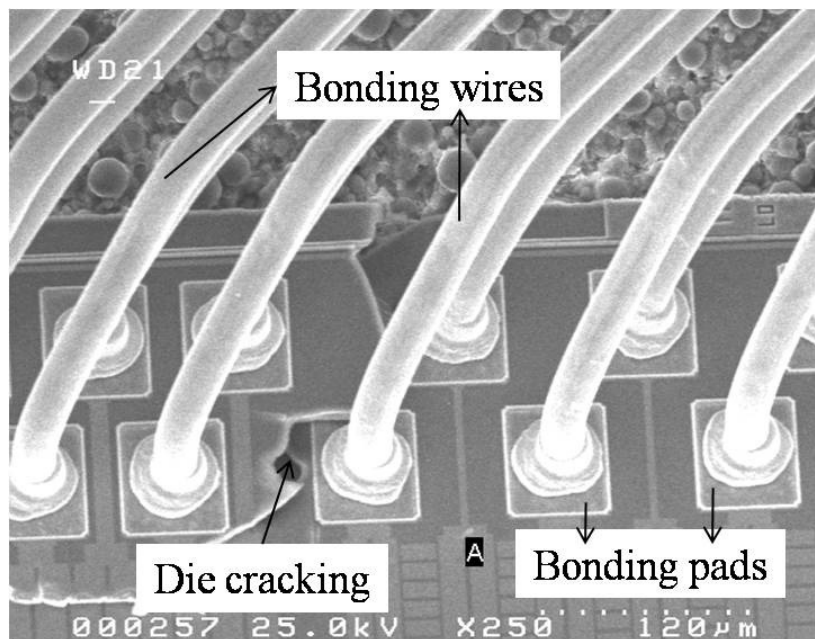
Figure 6-4 Die surface cracks after the thermal cycling tests
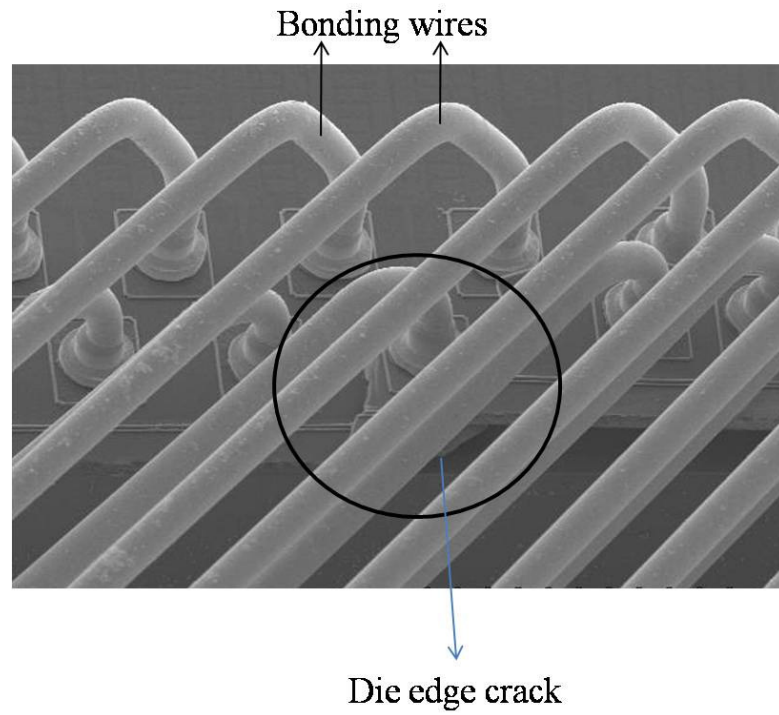
Figure 6-5 Die edge cracks and chipping
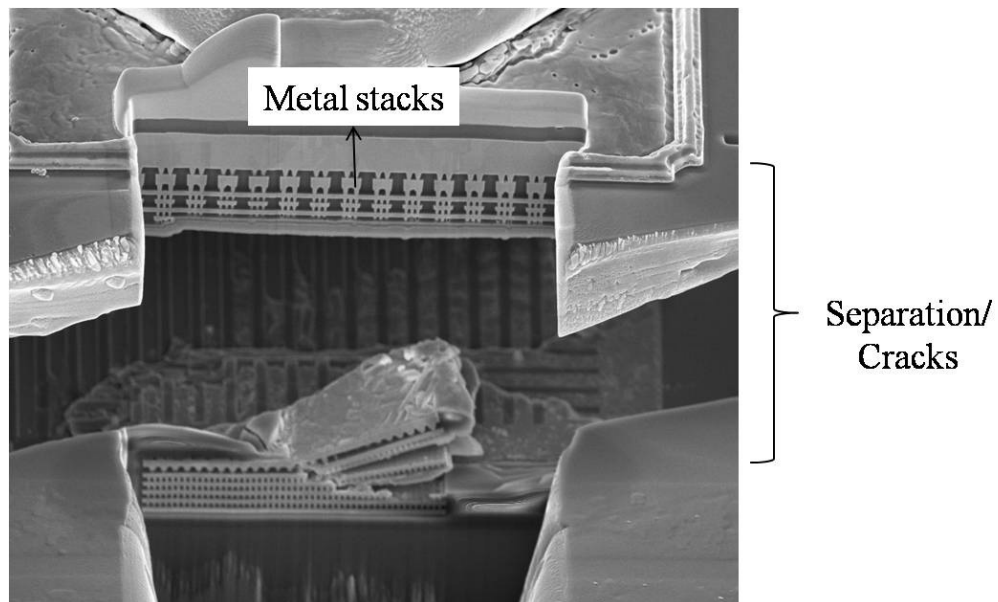
Figure 6-6 FIB image showing the inner layer cracking/delamination

Table 6-3 Possible failure mechanisms expected from the TEBGA package reliability tests [Yang & Bernstein, 2008]

Failure Category	Failure Mechanism	Driving Forces
Die	Inner layer dielectric and thin-film cracking and delamination	CTE mismatch; passivation materials; die sizes; edge micro-cracks from the wafer sawing; thermal mechanical stresses.
	Die cracking/ passivation cracking	Mechanical loads during the processing; defects induced in wafer saw processing; thermo-mechanical stresses.
Die attach	Interface delamination	Surface contaminations; oxidation and moisture absorption; voids at the interfaces; thermal mechanical stresses.
Wire bonding	Broken wires/lift wires	Thermal mechanical stresses; wire bonding loop profiles; bonding parameters; stress conditions; bonding pad metal contaminations; die surface delamination.
	Bonding pad cratering	Wire bonding defects; CTE mismatch and pad metallization/stack-ups; Wire bonding parameters.
Substrates	Via cracking	Substrate Tg; CTE mismatch; stress concentrations; moisture ingression; adhesion strength degradation.
	Interface delamination	Substrate Tg; material CTE mismatch; poor substrate process controls; moisture absorption; Interface adhesion strengths; stress loads.
	Solder mask cracking	Surface flaws and stress concentration; mechanical damages and CTE mismatch.
	Dielectric cracking	Copper trace layouts; copper surface roughness; dielectric material properties; CTE mismatch and stress loads.

Failure Category	Failure Mechanism	Driving Forces
Encapsulation	Encapsulant cracking	CTE mismatch; stress concentration; stress loads and material properties.
	Encapsulant interface delamination	CTE mismatch; stress concentration due to defects; material properties; moisture absorption; interface adhesion degradation; interface contaminations; passivation materials.
Solder joint	Solder joint fatigue cracking	CTE mismatch; pad surface finishes; solder materials and test conditions.
	Missing solder balls	Handling; CTE mismatch; pad surface finishes and contaminants; mechanical impacts during ATE testing; trays.

As proved, one of the dominant failure mechanisms for the low-k Cu die is ILD or thin film cracking. The failures can happen during the wafer preparing processes or the package assembly [Yang et al., 2006; Scherban et al., 2001; Fan et al., 2005 and 2008]. The inner layer thin film cracking or die cracking is mainly caused by the edge chipping and micro-cracks. These failures are highly dependent on the die sizes and package types [Hong, 1992]. There is a dependence of the die edge cracking seen in FCBGA packages on wafer sawing processes. It is found that the energy release rate increased significantly when the initial die edge defect sizes increases. However, the size of initial die edge defects can be tolerated if the right packaging materials are applied [Mercado and Sarihan, 2003]. Moreover, the rigidness of the substrate used in the package will significantly influence the stress magnitude and distribution on the die. Although Cu interconnects are increasingly favored over aluminum interconnects for the performance improvement of the devices, the technology is more likely to have reliability risks and to cause failures [Stolarska and Chopp, 2003]. A large amount of reliability test data is collected for TEBGA packages using 0.18 μm Al metallization silicon where there are no catastrophic failures observed [Yang et al., 2004]. However, The silicon devices built with Cu low-k metallization processes posted unexpected challenges because of

(1) Eight-layer Cu metallization in the silicon. The top metal layer is much thicker than the typical layers underneath to reduce the IR-drop. Also, Cu had a tendency to cause issues during wafer sawing. The test pads

155

and metal structures in the scribe street are prone to introduce the chipping during the sawing.

(2) The large package size and die size. Higher stresses are associated with large die sizes and package sizes.

(3) Substrate technology with thick Cu layers, including the variation of dielectric materials and the substrate cavity machining processes, can affect the evenness of the die attachment surfaces and stresses on the die

6.2.2 Key failure mechanisms

A high failure rate due to die-edge cracking or ILD and thin film cracking are observed during the package reliability studies. Extensive failure analyses reveal the cracking starts at die edges, then extends into the thin film interfaces. Figures 6-7 and 6-8 show the die cracks seen on the die surface and the thin film cracking (from FIB analysis). The key driving forces that influence the die cracking failures are investigated in this section, including the wafer sawing, assembly processes and materials, and thermal mechanical stresses due to the mismatch of the CTEs of the package materials.
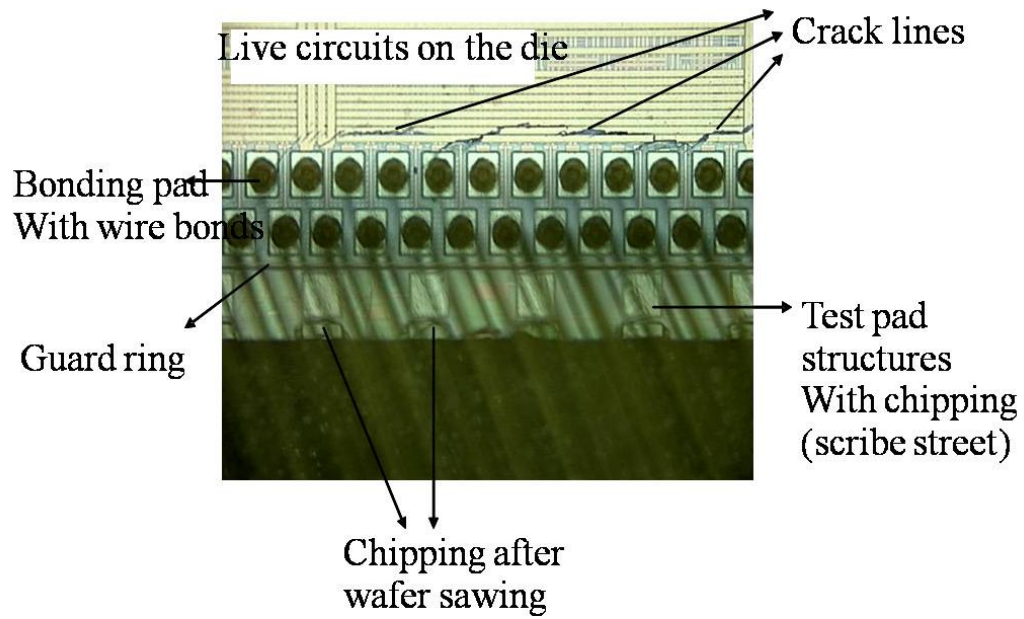
Figure 6-7 Die cracks seen on the die surface
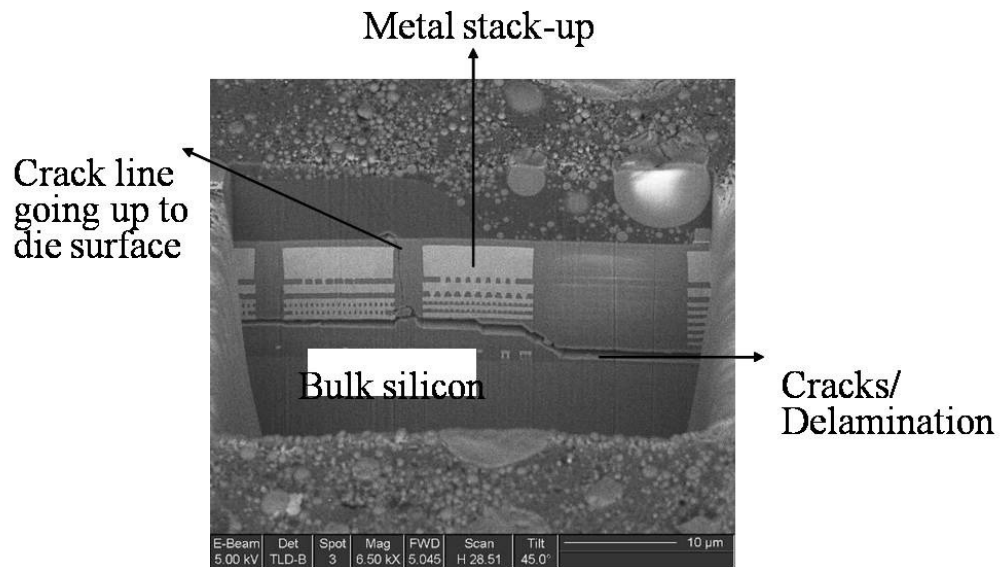
Figure 6-8 A cross section view of thin film delamination at interfaces

6.2.3 Materials and methods

6.2.3.1 Package and silicon attributes

The substrates under tests are unique in terms of their structure and manufacturing

processes. A machined cavity in the substrate is milled for the die placement.

Built-up circuit layers and dielectric layers are about 0.2 mm in thickness compared

to a 0.8 mm thickness of the metal heat spreader. The CTE of the substrate is not

far different from that of Cu (e.g. 16 ppm/ ^{o}C). However, the impact of the CTE

mismatch between the die and the substrate will be significant on the package war-

page and the stress distribution during the assembly process and the subsequent

stress tests.

Two different package sizes are investigated in this study, one is 35 mm $\times$ 35 mm

and the other is 45 mm $\times$ 45 mm. The thickness of the packages is about 1.49 mm

for both package sizes. The test devices had an 80 µm minimum width of the scribe

street. The bonding pad structure is an Al cap on the Cu metallization. The bonding

pad pitch is 40 µm /80 µm.   Figure 6-9 shows the bond pad layout and Figure 6-10

shows the cross-section of the bonding interfaces.   A combination of maximum of

layers of Cu in the silicon, a high copper density at the scribe street and a large

package / die size will present many challenges to the reliability performance of the

packages. Table 6-4 lists the attributes of the test samples. Figure 6-11 shows a

stack-up diagram of the substrate technology.

Figure 6-9 Bond pad layout and pitch rules

Figure 6-10 Bond pad structure (Al cap above Cu stack-up)

Table 6-4 Package and device attributes

Type	Item	Attributes	
Packages	Type	EBGA	
	Size & Thickness	45x45 mm^2 1.49 mm thick	35x35 mm^2 1.49 mm thick
	1st level inter-connects	Au bonding wires	
	Ball count	1140	672
	Ball size	0.65 mm in diameter	
	Solder mask opening	400 μm	
	Substrate layer count & thickness	4 layers & 0.99 mm	
Silicon	Die size	15×15 mm^2	12.5×12.5 mm^2
	No. of bonding pads	1400	900
	Die thickness	15 mil (381 μm)	
	Pad structure	Al cap on Cu	
	Metallization	Cu	
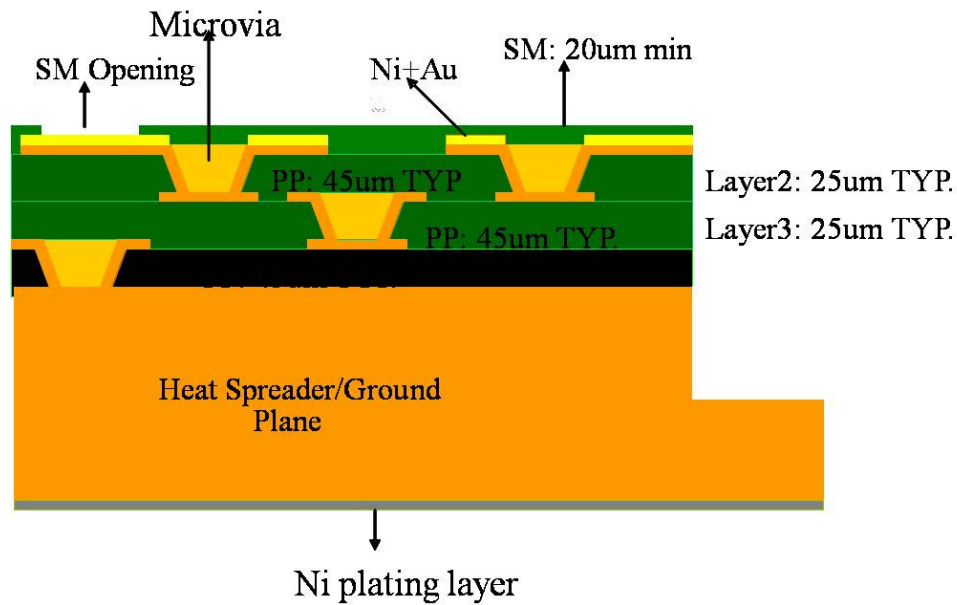
Figure 6-11 The stack-up diagram of the substrate technology

As mentioned, the dielectric layers and metallization layers are much thinner than
the Cu heat spreader in the substrate. The thick Cu heat spreader will influence the
stresses on the die surface or the die edge significantly. In addition, a large stress
will be experienced on the die surface and die edges due to the CTE mismatch of the
packaging materials.

6.2.3.2 Assembly modules of the assembly process

Figures 6-12 and 6-13 show the complete assembly process flow. Some of the key
processes are described below.

161
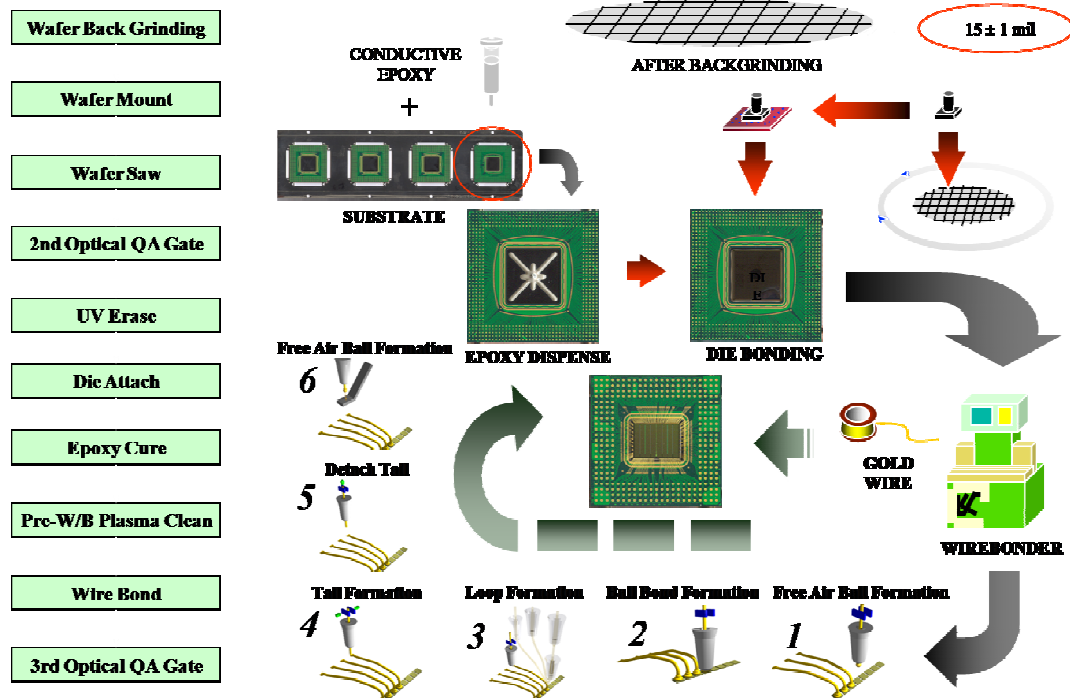
Figure 6-12 TEBGA package assembly process flow-Part I [ASE, 2004]

Pre-L/E Baking	
Pre-L/E Plasma Clean	
Liquid Encapsulation	
Post Mold Cure	
Solder Ball Mount	
IR Reflow	
Flux Clean	
Pre-T/M Plasma Clean	
Pad Topside Marking	
Mark Cure	
FVI QA Gate	
Packing	
Packing QA Gate	

FINISHED WIRE BOND

+

LIQUID COMPOUND

=

DAM APPLICATION

FILL APPLICATION

BALL ATTACH   REFLOW   OUTPUT MAGAZINE LOADER

SOLDER FLUX

BEFORE BALL ATTACH

FLUX APPLICATION

SOLDER BALL

AFTER BALL ATTACH

BALL MOUNTED

REFLOW

Ink Marking

TOPSIDE MARKING

+

Figure 6-13 TEBGA package assembly process flow-Part II [ASE, 2004]

(1) Wafer back grinding and sawing

The wafer sawing process can introduce serious defects to the die edges as well as the die itself. The defects, such as chipping and micro-cracks, will act as stress concentration points for future package failures. The presence of test structures at scribe streets will increase the possibility of peeling and chipping defects on the die edges during the wafer sawing process.   Examples of chipping defects at the die edge from the wafer sawing process are shown in Figures 6-14 and 6-15.

163

Figure 6-14 Chipping touching the guard ring
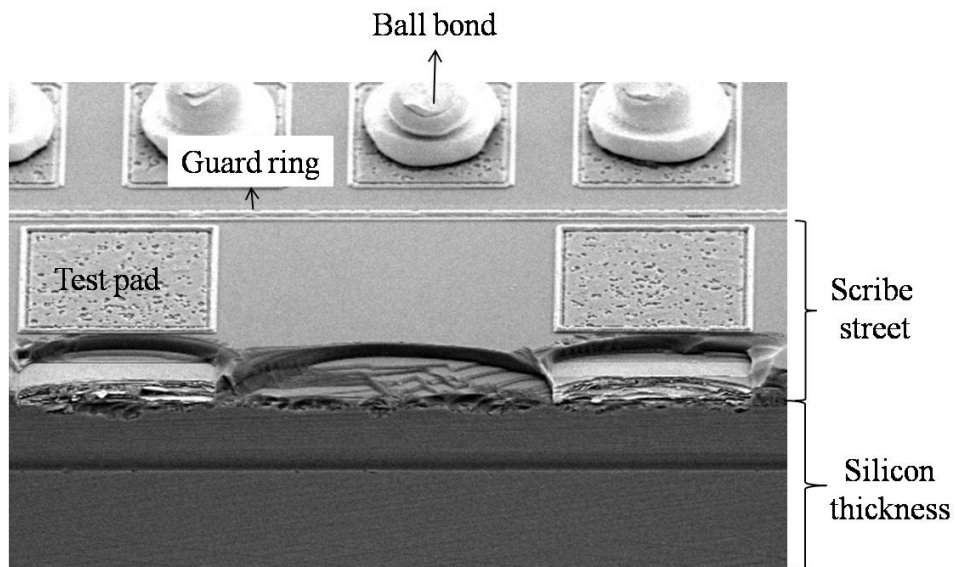
Figure 6-15 Test pads and the chipping at the scribe street

(2) Die attachment

The die attachment materials and their curing process are important to the levels of the stress on the die. The key process control factors include the bonding line thickness, the voids of die attachment adhesives, and the fillet height.   The surface flatness of the substrate cavity will also affect the overall bonding line thickness, the die tilting angle as well as the fillet height. The surface of the cavity shall be flat but with a certain roughness to have a strong bond with the die. Figure 6-16 highlights the die and die attachment elements.
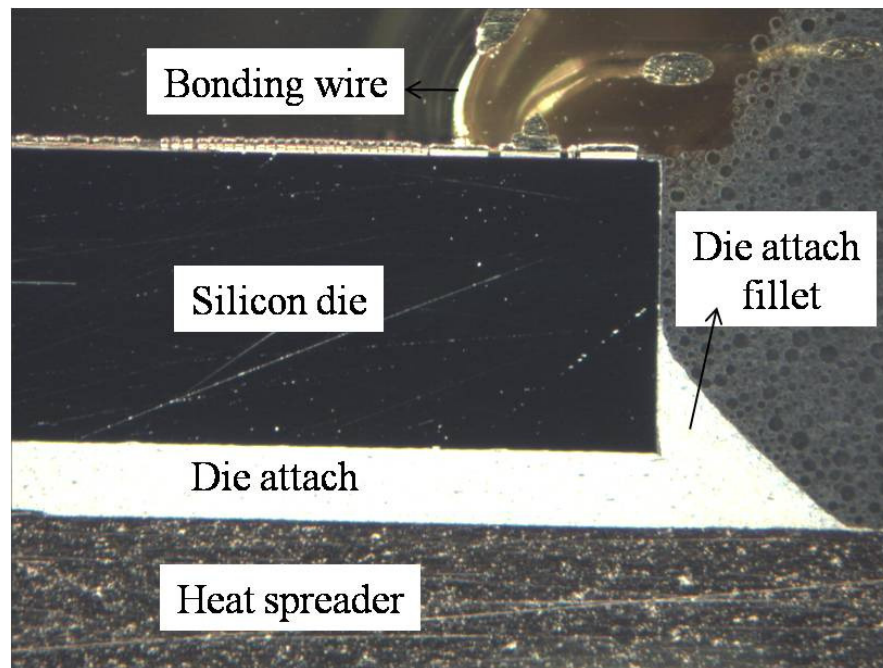
Figure 6-16 Demonstration of die attach elements

(3) Wire bonding

During the package assembly, three different loop profiles are designed to meet the bonding wire density needs and the specification of the solder ball stand-off height after reflowing [JEDEC, 2005]. Because of the single tier structure of the substrates, there is a great challenge to balance reliable wire bond contacts and the overall package specification, e.g. solder ball stand-offs. Wire sweep failures can be a factor to consider too. The bonding parameters can introduce cracking or damages on the die.

(4) Liquid encapsulation

Encapsulation materials have very different CTE and Young's modulus values compared to the silicon. As a result, a large thermal mechanical stress can be generated on the silicon, during the encapsulant curing process and stress tests. Low stress encapsulation materials are generally preferred to reduce the stress on the die and prevent failures such as die cracking.

(5) Solder ball attachment and reflowing

During the solder ball attachment process, the packages will need to go through a peak temperature shock as high as 245-260 ^{o}C during the solder reflowing process. Thermal stress generated during the reflowing process can introduce various failures.

6.2.3.3 Experimental set-up and descriptions

To fully characterize the failure mechanism mentioned above, first of all, a fishbone diagram is studied (Figure 6-17) and second, a hypothesis study is conducted and the critical factors suspicious of causing die-edge cracking are shown in Table 6-5. Top suspects are associated with local damages on the die edge, as well as the stress generated during assembly. Moreover, assembly materials and geometry variations in the die attach process can affect the stress distribution on the die significantly. A series of studies are conducted to validate the hypothesis listed. In addition, the board level solder joint reliability is proceeded to understand if missing ball failures are a long term threat to the package reliability performance.
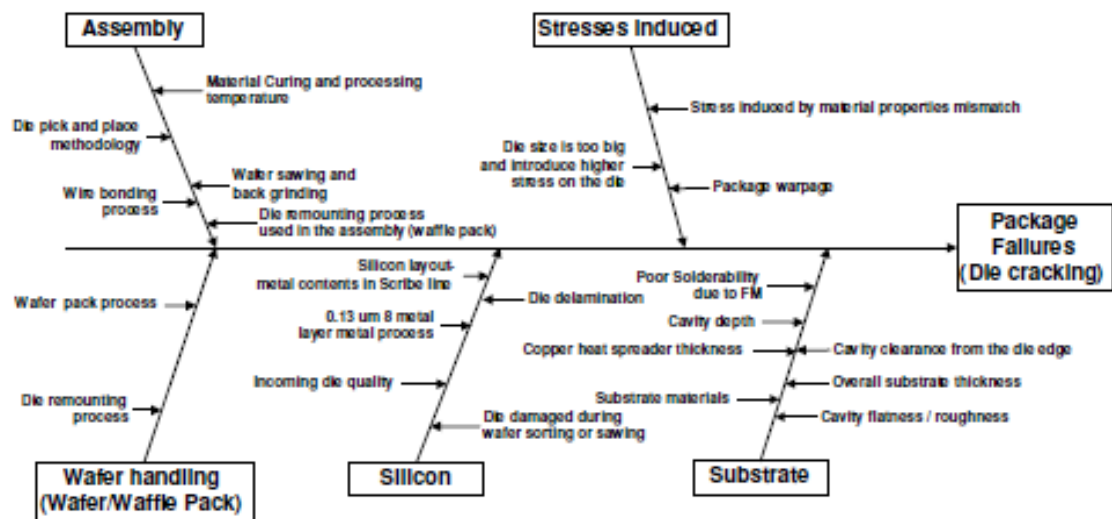
Figure 6-17 Fishbone diagram for the root cause analysis of die cracking failures

Table 6-5 A hypothesis summary for the die cracking and thin film cracking failures

Category	Potential causes	Data to support	Data to refute
Substrate	cavity flatness is not meeting specification	die cracking; the substrate cavity surface not flat	no die backside cracking seen. BLT is within specification.
	cavity wall is too close to the die edge	cracking on the die edges	Clearance meet design rules
	Substrate stack-up structures	TEBGA is observed with cracking and UBGA not shown die cracking.	Similar substrates are not seen issues with other silicon products. FEA results showed similar stress distribution for TEBGA and UBGA.
Assembly	Assembly materials-mismatch (die, encapsulation, adhesive, copper)	die cracking right after assembly and after preconditioning test.	the cracks are not seen at corners but at the die edges where defects are visible.
	Manufacturing and process control	Die cracking before any stress testing. Excessive chipping is seen.	All manufacturing data are under control.
	die back grinding damage	die cracking/damage.	No die backside cracking seen.
	wafer sawing damage	damages on the die edges; die edge cracking; thin film delamination failures.	Standard wafer sawing process used. Single or dual process.
	Wire bonding (temp, force, pressure, tool	Die edge cracking and ILD delamination failures.	No visual defects or cracks seen in the assembly in-

Category	Potential causes	Data to support	Data to refute
	touching etc.)		line control. No wire bonding damages.
	Die attach curing temperature	die cracking.	curing parameters are within spec.
	Encapsulation cure temperature and process damage.	die cracking seen at the end of line	curing parameters are within spec.
Test stress	die size/die thickness ratio concerns	die cracking.	Not all the packages seen failures.
	material mismatch during stressing	die cracking.	Not all the packages seen failures.
Silicon	Silicon top metal layers changes	die cracking and thin film delamination	Film delamination seen at the bottom metal layers other than top layers.
	Incoming wafer quality issues	Die cracking	No issues with incoming check and handling.
	Die size is too large	Die cracking	Not all of the packages seen failures.

(1) Wafer sawing studies

Failure analysis demonstrates that chipping defects from the wafer sawing are the

initiation points of the die cracking and the inner layer dielectrics cracking. The

cracks will extend with the help of the die-edge tensile stress associated with the

CTE mismatch between the packaging materials and the process control, such as

the fillet height of the die attach adhesives. In order to reduce the damages from the wafer sawing process, a dual step sawing approach is evaluated. During the process, the first step is to cut into the scribe street at a desired depth instead of cutting through the silicon, then followed by cutting through the wafer using a narrower blade. The theory is to reduce the impacts of cutting through the metallization in the scribe streets on the edge of the die. A narrow blade in the first cut will significantly reduce the impacts. Figure 6-18 illustrates the top view of the die surface with information of the scribe width and test structures in the scribe street. Test structures are seen on both 80 μm and 240 μm scribe streets. The guard ring is applied to prevent the peeling or the cracking of the live die area. Key sawing factors including blade grit sizes, cutting kerf widths, feed speeds, blade RPMs and first step cutting depths are shown in Table 6-6.
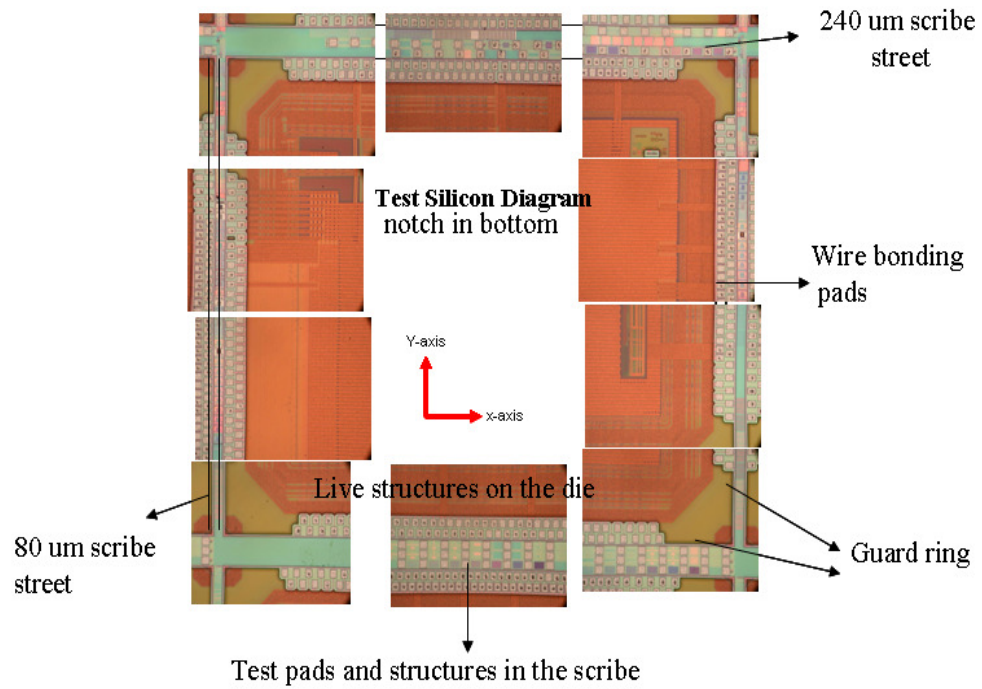
Figure 6-18 Schematic diagram of the test chip showing the scribe street

Table 6-6 Factors and parameters of the dual step wafer sawing processes

Items	1st Blade	2nd blade
Blade type	A	B
Blade Grit size	2-4 μm	2-4 μm
Kerf width	25~30 μm	20~25 μm
Feed Spreed	35 mm/s	35 mm/s
RPM	45k	45k
Cutting Depth	10 mil (254 μm)	5 mil (127 μm)

Additionally, several studies focusing on wafer sawing schemes are carried out to understand the mechanics of the die-edge cracking and find the solutions to prevent the failures. The studies are described below.

> (1) A wider scribe street study. By simulating a wider scribe street, the buffer distance between the guard ring and the die edge will be larger, and the assumption is that there will be higher levels of tolerances to die edge damages during the wafer sawing processes.

> (2) A study of sawing using resin blades.   Resin blades are soft and compliant compared with diamond blades in the wafer sawing process. In theory, the stress on the die edge will be smaller if using resin blades, then less damages on the die edges will be introduced during the sawing process.

Temperature cycling tests are one of the methods to activate the die edge cracking and inner layer dielectric cracking failures.   Besides the functional tests, CSAM is able to detect the cracking/delamination failures (sample images shown in Figures 6-19 and 6-20), even for very fine cracks underneath the die surface.   However, the functional test often showed few failures compared with the CSAM analysis.   It means the die cracking and inner layer dielectric cracking will not necessarily translate to functional failures.
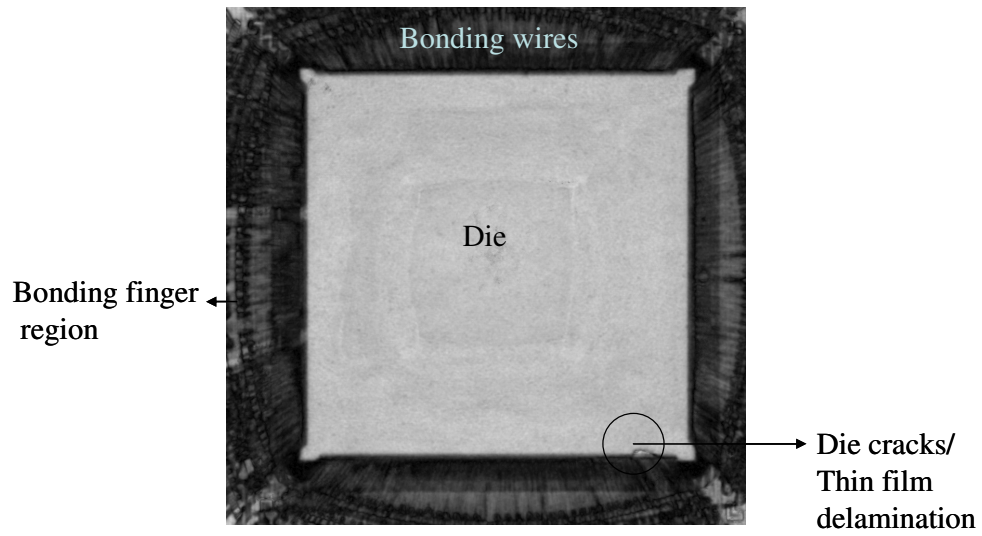
Figure 6-19 A CSAM showing the die cracking/thin film delamination at the die edge

(small)
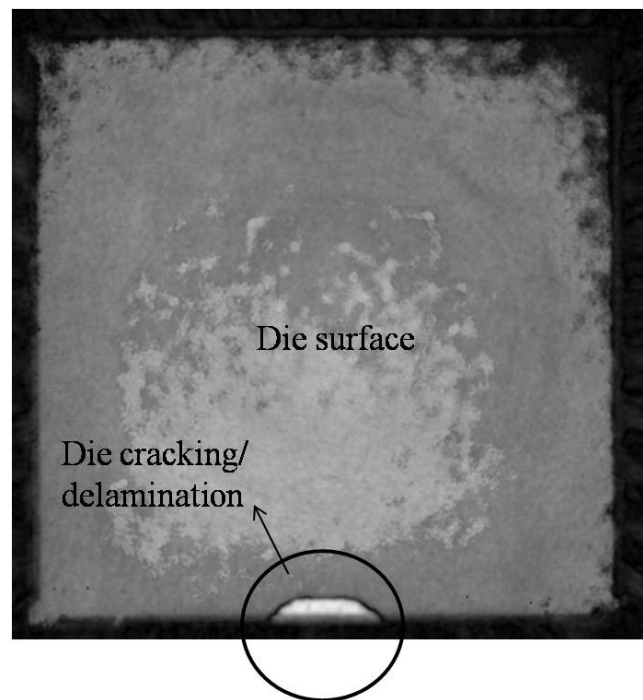
Figure 6-20 A CSAM showing the die cracking/thin film delamination at the die

173

(2) The impacts of encapsulation and die attach materials

Referring to the package structures, one of the significant factors affecting the stress on the die is packaging materials, including the encapsulant and the die attach materials. There is a significant CTE between the silicon and those assembly materials. As a result, the thermo-mechanical stresses will be generated on the die during the assembly processes and subsequent stress tests. Low stress encapsulation materials and die attach materials are evaluated through FEA simulation.   An example of the FEA model is shown in Figure 6-21.
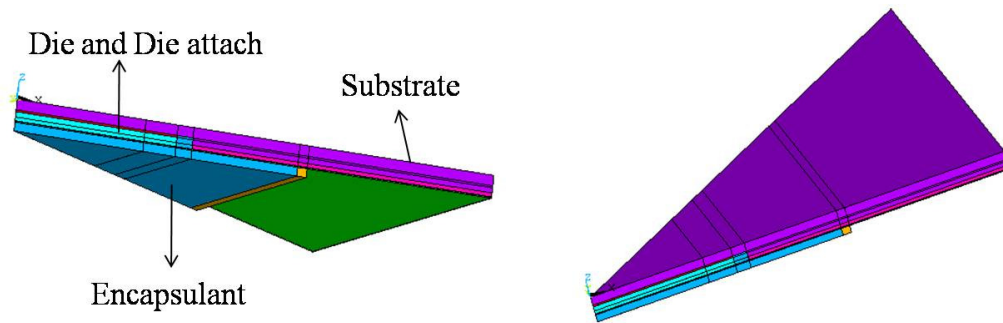
Figure 6-21 A 1/8 FEA model of the package

(3) The impact of package substrate variations

A variation of the substrate stack-up is studied using the FEA approach and empirical studies. The key structures and dimensions are described in Table 6-7. Besides the dimension variations, the biggest differences between the structures are

174

the manufacturing processes of the cavity where the die will sit. The assembly

materials and parameters are exactly the same.

Table 6-7 Package dimensions for the simulation study

Components	Package Attributes
Package size, mm × mm	45×45 and 35× 35
Die size, mm × mm	12.5 to 15.4
Cavity size, mm × mm	14 to 16.7
Cu thickness under the die, mm	0.387 to 0.466
Cu heat spreader thickness, mm	0.786
Solder mask thickness, mm	0.023 to 0.046
Cu/Dielectric thickness, mm	0.141 to 0.186

6.2.4. Experimental results and discussions

The reliability testing results from the package qualification tests is shown in Table

6-8. The temperature cycling test is effective to pick up the failures and in seeing

that die cracking is the root cause of the failures.

Table 6-8 Test results of package qualification

Stress Types	Conditions	Test Results (# of failures /total sample size)
Preconditioning	JEDEC MSL 4 (peak Temp: 220 ^{o}C)	0/450
Temperature cycling	1000 cycles at condition "B" (-55 ^{o}C +125 ^{o}C)	12/230. Die edge cracking is the failure mechanism.
Unbias HAST	100 hrs at 130 ^{o}C/85% RH	0/119.
High temperature bake	1000 hrs at 150 ^{o}C	0/231.
Board level temperature cycling test	TC 'X': 1000 cycles (-40 ^{o}C to 85 ^{o}C)	0/38 after 1000 cycles.
	TC 'J': 3500 cycles (0-100 ^{o}C)	0/30 after 7000 cycles.

In this section, the results from various studies to understand the failure mechanisms

and root causes will be discussed.

6.2.4.1 Impacts of dual-step wafer sawing approach

A high die cracking failure rate (over 10% @ 90% CL) is seen with TEBGA pack-

ages using a single step wafer sawing scheme during the pre-qualification study.

By converting to a dual-step wafer sawing process, which cut through the first

depth of 5-10 mils on the scribe street and then finish the cut using a narrow blade, a

much lower failure rate (in the range of 2-3% @ 90% confidence level) is reported.

Although the improvement is obvious, it demonstrated that sawing damages and die

cracking failures cannot be eliminated by only optimizing the sawing schemes and

parameters.   Figures 6-22 and 6-23 show the die edge cracking observed after a

temperature cycling test. In some cases, the cracks existed before the encapsulation

process in the assembly (encapsulant is seen inside the crack lines).

Guard ring

Bonding Au wire

Cracking line seen after wafer sawing

Chipping due to wafer sawing
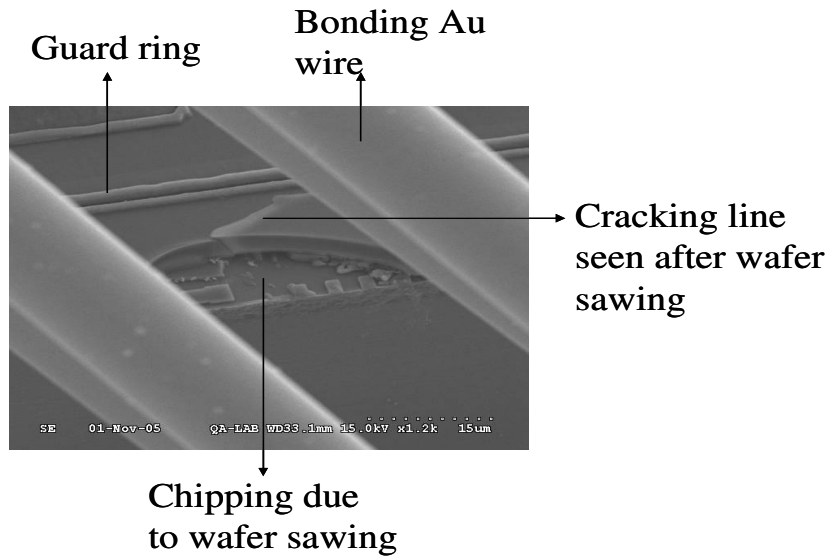
Figure 6-22 Die edge cracking seen after decapping

Metal stack-up Of pad structure

M8
M7

Metal in the Scribe street Showed peeling.

Bulk Silicon
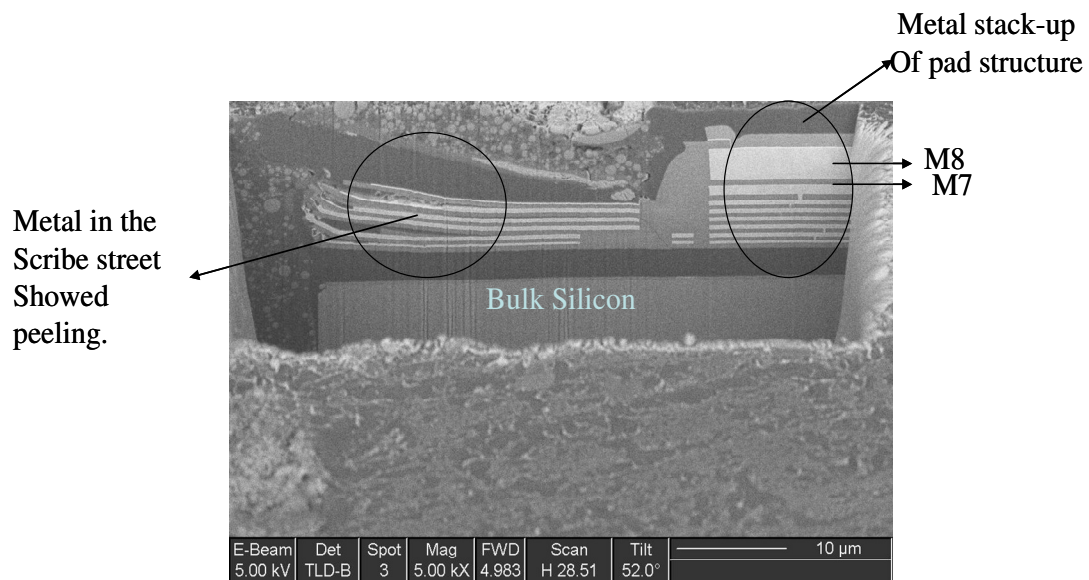
Figure 6-23 Chipping and metal peeling at the die edge

Besides the sawing schemes, the blade dressing process is found to be critical to maintain clean and controlled cutting edges. Experimental results demonstrate that a blade dressing is required to be done every twenty five wafers.

6.2.4.2 The influence of increasing the width of the scribe street

The majority of the die cracking failures is seen in the narrow scribe street (80 μm). A proposal to increase the scribes from 80 μm to 160 μm is evaluated. The implementation is carried out by sacrificing one column of dice adjacent to an 80 μm street in the wafer to make a 160 μm scribe street. The scribe of finished dice will have a 160 μm width on one side and a 240 μm scribe width on the other. As a result, the dead silicon area between the die edge and the guard ring is about 70 μm and 110 μm respectively. A total of 205 units are assembled and sent for reliability testing. Fifteen units from 205 sample units are seen die cracking right after 250 cycles of the temperature cycling test, and another twelve units fail after 500 cycles of the temperature cycling test, an additional two units fail after 1000 cycles.

The error bound for the number of failures at each of the test intervals can be calculated based on Eq. [5.14]. Taking a 250-cycle period as a time interval, 15 failures are observed in the first interval. Using the Eq. [5.14], the bounds for the failures observed are 11 to19 failures for the same time interval. In the second 250 cycles interval, 12 failures are observed within the estimated bounds and the failure rate is considered to be constant. However, the number of failures drops significantly after 500 cycles of thermal cycling. The majority of the failures is seen before 500 cycles

178

with a constant failure and a very low number of failure numbers is seen between 500 and 1000 cycles.   It is possible that the failures can be screened.

6.2.4.3 Study of resin blades

The wafer sawing using the resin blade presents the best sawing quality in terms of the kerf width control, the size and the number of chippings on the die edges (Figure 6-24), , especially in the area where metal structures are presented.   In this study, a total of 113 samples are built with the dice cut using resin blades and sent through the temperature cycling test. There are total four failures after 1000 cycles and the bounds for the number of failure at 1000 cycles intervals is 2 to 6. The reliability of the package is significantly improved with a failure rate of 2400 FIT based on an acceleration factor of 7.3 of a 0-70 $^{\circ}$C use conditions.

The dominant failures are due to the initial defects of micro-cracks after the wafer sawing process. The wafers sawed using the resin blade show a higher reliability after the temperature cycling test. It demonstrated, with the right type of sawing blades and optimized dual step sawing parameters, die cracking and inner layer thin film dielectric cracking failures can be reduced or eliminated. The resin blades used in the wafer sawing process present robust results. Table 6-9 summarizes the failure rate calculated from resin blade study and wide scribe study, resin blades perform the best.

Guard ring

Bonding pads

Guard ring

Test pads

Kerf width

Edge chipping

Edge chipping

80 um scribe street

240 um scribe street
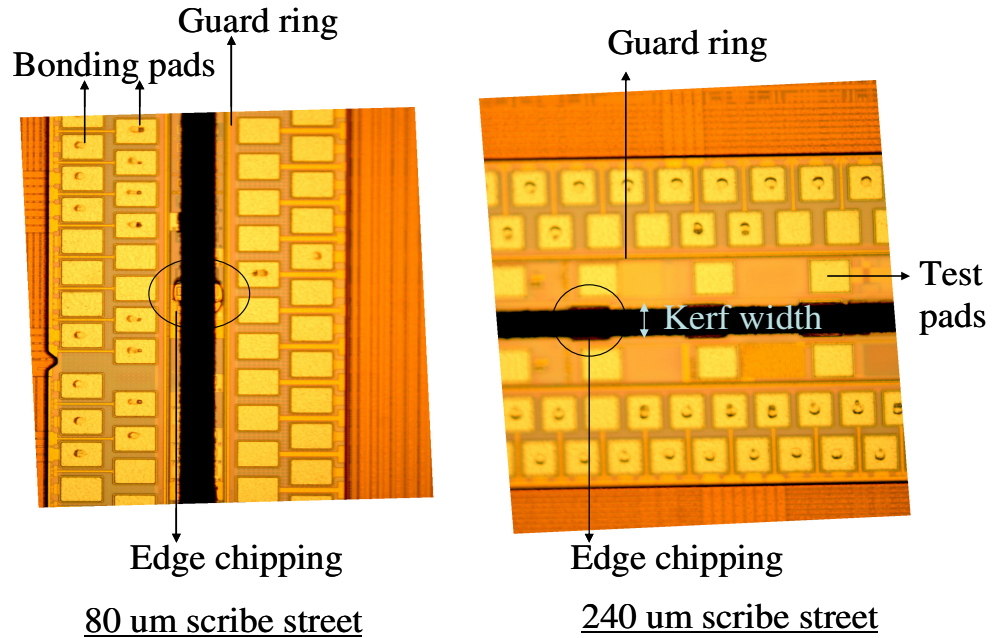
Figure 6-24 Visual images of the defects after the wafer sawing using resin blades

Table 6-9 Summaries of the dual step wafer sawing studies

Studies (Dual step sawing)	Failure Rate	Reliability bounds
Diamond blade study	9.417E-5	0.9243-0.9621
Resin blade study	5.213e-5	0.9561-0.9826
Wide scribe study	0.0003	0.8585-0.9268

6.2.4.4 Impacts of package attributes

FEA results validate that the large tensile stress is located at the edges of the die for both 35 mm and 45 mm TEBGA packages. Similar die principle stresses are shown on the die surface during thermal cycling tests. It also demonstrates that the impact

180

of the substrate size on the stress distribution on the die is minimal. However, an alternative TEBGA package with different dielectric materials and thinner copper heat spreader thickness and different cavity milling process generates smaller tensile stress on the die. Experimental results of the revised TEBGA substrate show a much lower failure rates due to the die cracking and ILD failures. The difference on the die surface stress distribution is due to the change of Cu heat spreader thickness and the cavity features of the substrates. Figure 6-25 shows an example of the stress distribution on the die for TEBGA packages with thick Cu heat spreader.
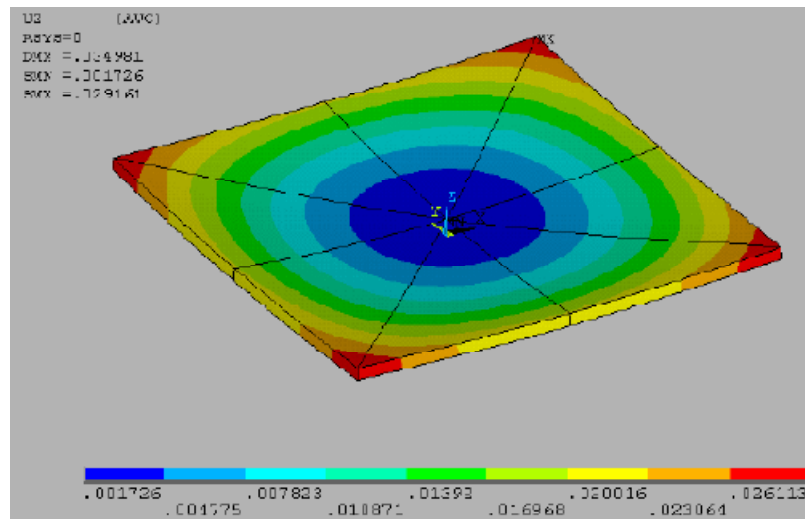
Figure 6-25 Die placement contour under thermal cycling tests

It should be pointed out that the stress obtained in all cases is no way large enough to break a perfect silicon unless the silicon is flawed and micro cracks pre-existed before the stress applied. The presence of the die edge chippings and peelings helped introduce the failures, the higher stress generated did not help either. It

181

should be mentioned that the die cracking failures are not observed in similar parts

using an Al metallization silicon. Instead, it shows a very stable and a clean sawing

edge and there is no subsequent die cracking failures found after the assembly and

after the stress tests.

6.2.4.5 Impacts of assembly materials for encapsulation and die attachment

In theory, low stress die attach and encapsulation materials will reduce the stresses

on the die and then reduce the possibility of die cracking failures. Table 6-10 shows

three types of die attach and encapsulation material studied.

Table 6-10 Low stress die attach and encapsulation material properties

Encapsulant	Categories	Material properties
A	Modulus, Mpa	$-0.1174T^2 + 53.221T + 4231.9$
	CTE, ppm/C	$3E-06T^3 - 0.0022T^2 + 0.4323T$
B	Modulus, Mpa	$0.0013T^3 - 1.2176T^2 + 282.64T$
	CTE, ppm/C	$-5E-06T^3 + 0.004T^2 - 0.6616T$
C	Modulus, Mpa	$0.002T^3 - 1.8653T^2 + 438.78T$
	CTE, ppm/C	$-2E-06T^3 + 0.0019T^2 - 0.3233T$
Die Attach Adhesive		
E	Modulus, Mpa	$0.0006T^3 - 0.572T^2 + 128.01T$
	CTE, ppm/C	$-7E-06T^3 + 0.0054T^2 - 0.6717T$
F	Modulus, Mpa	$65200 \ e^{-0.0153 \ T}$
	CTE, ppm/C	138
G	Modulus, Mpa	$4E-05T^3 - 0.0402T^2 + 9.4209T$
	CTE, ppm/C	$2E-06T^3 - 0.0018T^2 + 0.9052T$

The finite element study shows the low stress encapsulation materials will help reduce the substrate warpage and then the stress on the die significantly. Type C die attach materials generated the smallest warpage on the packages. The combination of the type A encapsulant and the type C die attach material generated the smallest stress on the die surface. The application of low stress materials will reduce the risks of the die cracking and thin film cracking failures. The accurate stress analysis with corner/biomaterial interfaces involved can use a fracture mechanics based approach to predict the failures [Fan et al., 2001].

6.2.4.6 Impacts of the assembly process

The fillet height of the die attach materials as well as the substrate cavity flatness are identified as two key process factors which can introduce the failures. The cavity milling process during substrate manufacturing creates cavity surfaces with a high peak area in the center and the pin-wheel like effects, as shown in Figures 6-26 and 6-27. The potential risk of the cavity flatness variation is interfacial delamination and bonding line thickness variations, and the variation of the fillet height. Finite element analysis shows if the fillet height is over 95% of the die thickness, the tensile stress will be significantly increased (Figure 6-28). Failure analysis demonstrates that several failed units have fillet heights over 93%-100% of the die thickness. The recommended fillet height criteria are 50% and no higher than 75% of the die thickness.

The limitation of the die cavity flatness is controlled at ~2 mil to reduce their impacts on the process variations.   The cavity profile /flatness with a large die size results in a much poorer die attach control.
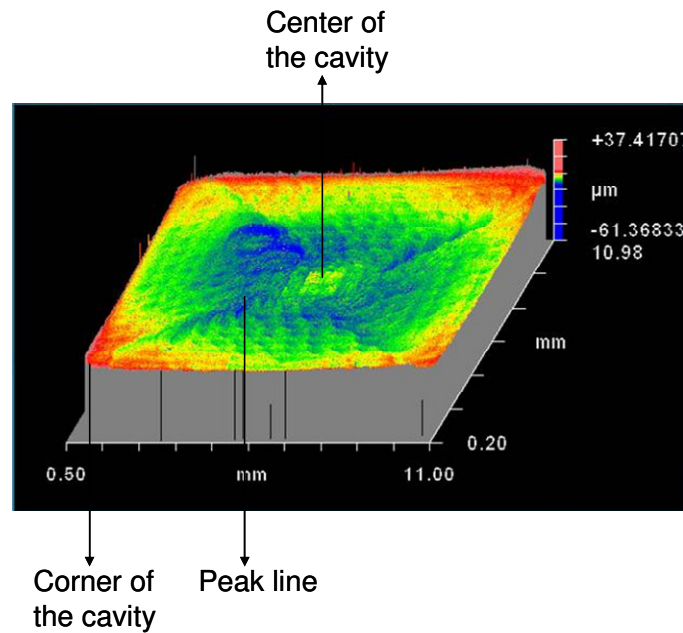
Figure 6-26 A scanning contour showing the substrate cavity

flatness (example flatness: ~95 um)
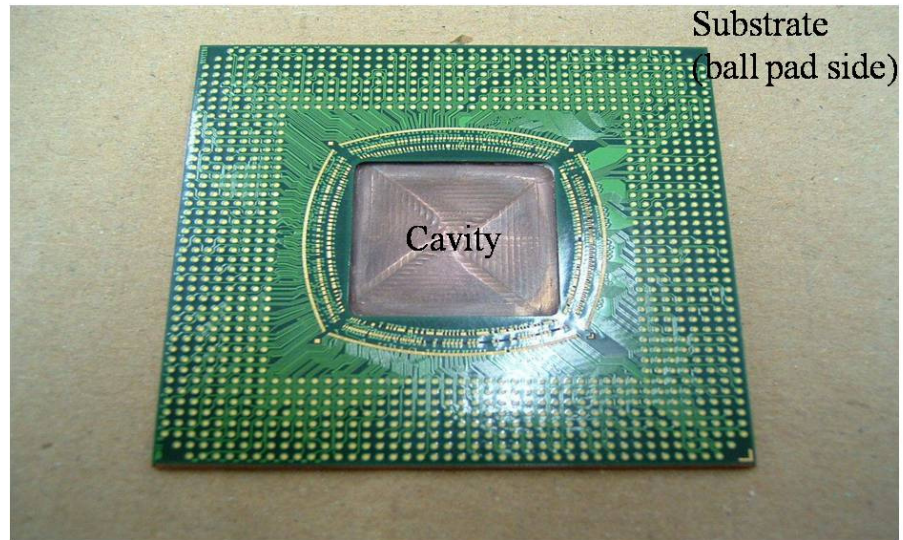
Figure 6-27 Cavity surfaces of TEBGA substrates
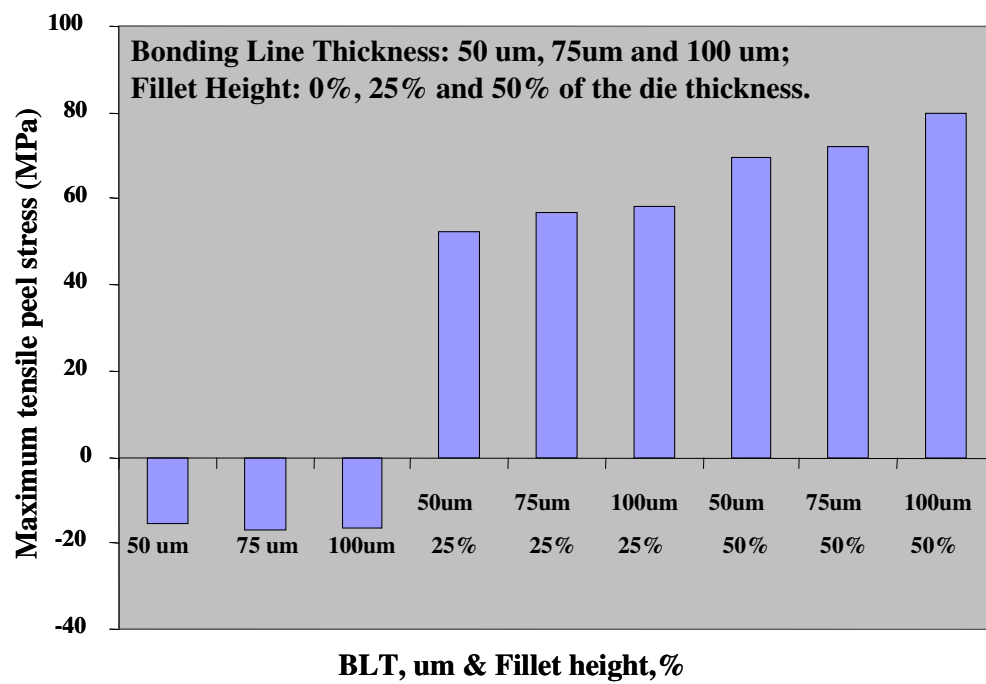
Figure 6-28 Impact of the die fillet height on the die stress of TEBGAs

185

6.4.4.7 Solder joint reliability assessment

The ball shear or pull tests are usually used to measure the quality of the solder joints in BGA packages.   However, the ball shear and pull tests will not guarantee good solder joints.

In order to demonstrate the solder joint reliability of the packages, especially the observation of missing balls during the assembly and test processes, the packages were cycled at a condition of 0 ^{o}C-100 ^{o}C.   The life at the accelerated conditions can be extrapolated to the use conditions by using a reasonable acceleration factor. Table 6-11 lists detailed information of test vehicles used in board level thermal cycling.

The cycles to failure data is listed in Table 6-12. There are total 24 samples failed and 8 units suspended at the end of 10000 cycles. The failure mechanisms are confirmed as cracking at the ball sides of the joints.

Table 6-11 Test packages, boards and conditions used in SJR study

Test Packages	
Package Body Size	45 mm-TEBGA
Die Dimensions	10mm × 10mm
Solder Ball Diameter	650 um
Solder Resist Opening (SRO)	400 um
Solder Ball Land Type (SMD, NSMD)	SMD
Solder Ball Pitch	1.00 mm
Solder Ball Metallurgy	Eutectic – 63Sn/37Pb
Substrate Number of Layers	4 (3 + 1 Grounded Heat Spreader)
Substrate Thickness	0.99mm
Solder Resist Opening Surface Finish	ENIG
Test Board Information	
Board Dimensions	298 × 216 × 2.4mm thick
Dielectric Material	FR-4
Board Stack-up	6-layer (1.0 oz Copper layer)
Solder Pad Diameter	18mils +/- 2mils everywhere
Solder Pad Type	Metal Defined
Board Solder Pad Surface Finish	HASL
TEST CONDITIONS	
Sample Size	32 packages / 4 boards

Temp Cycle Range	0 to 100 ^{o}C
Temp Cycle Duration	10-min ramp; 15-min dwell
Failure Criteria Method	Event Detection: 1000-ohm per IPC9701 Resistance Measurement: 15% net increase

Table 6-12 Solder joint failure data for TEBGA packages (45 mm x 45 mm)

Number of Devices	Cycles to failure	Censor
24	9965. 8891, 8965, 9121, 9347, 9280, 9275, 8060,9482, 9546, 8154, 9371, 9033, 9845, 9758, 8438,9740,9875,9518,7838,9694,9508,8564,8595,	Fail
8	10000 (8)	Not fail

Both Weibull plots and lognormal plots of the solder joint failure test data are shown in Figures 6-29 and -30. The failure data fit both distributions very well. The shape parameters of the Weibull distribution is over 15 which means that the failures happen in a short time duration and distribute close to each other.   The MTTF of the distribution is about 9500 cycles. Overall, the solder joint reliability is robust.
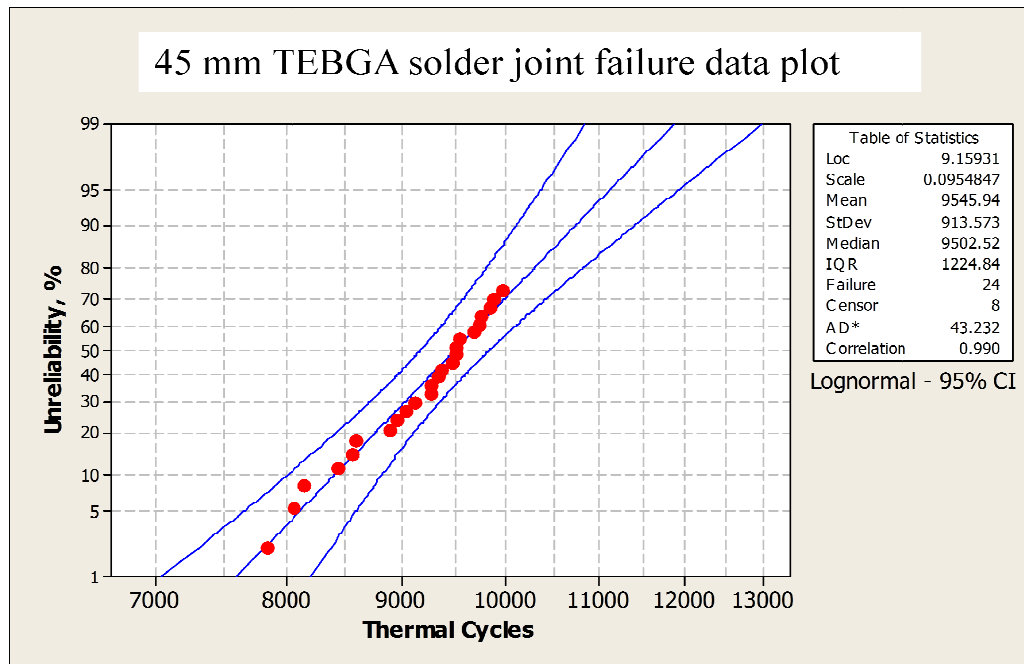
Figure 6-29 Log-normal plot of the solder joint failure data for TEBGAs
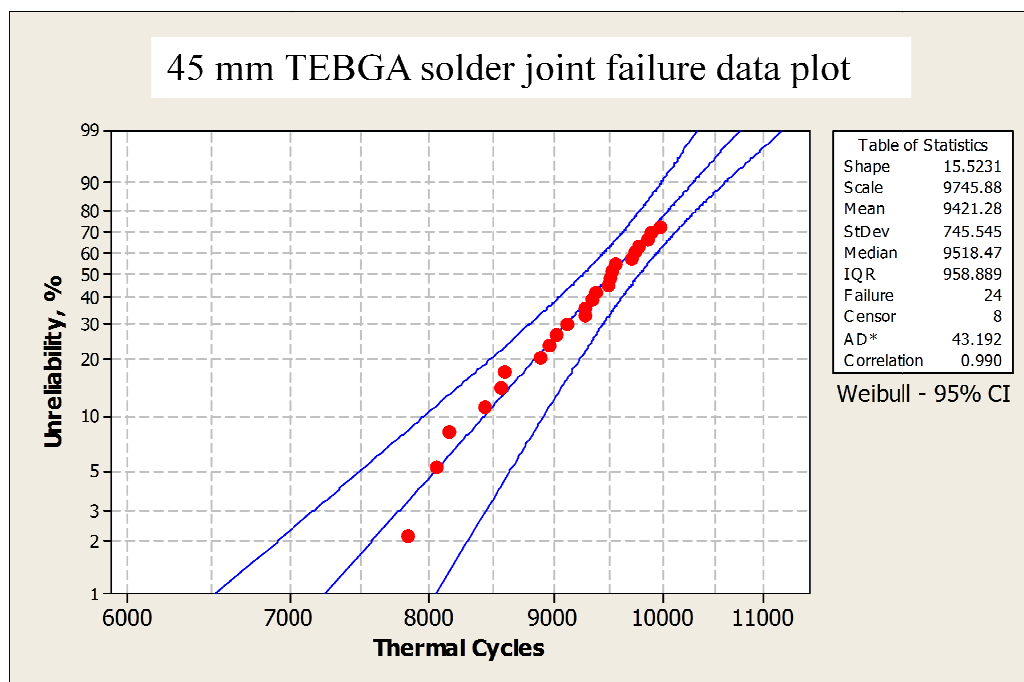
Figure 6-30 Weibull plot of the solder joint failure data for TEBGAs

189

The failure data can be collected at interval readings and analyzed as well. The question is if there are any differences in comparison to the exact number of failures. Figure 6-31 plots the original data in a different plot using the periodic failure data at fixed test intervals, from which a similar conclusion can be drawn. Based on the discussions in chapter 4, in comparison to similar package technologies, the field life of the package can be predicted using the AF models.
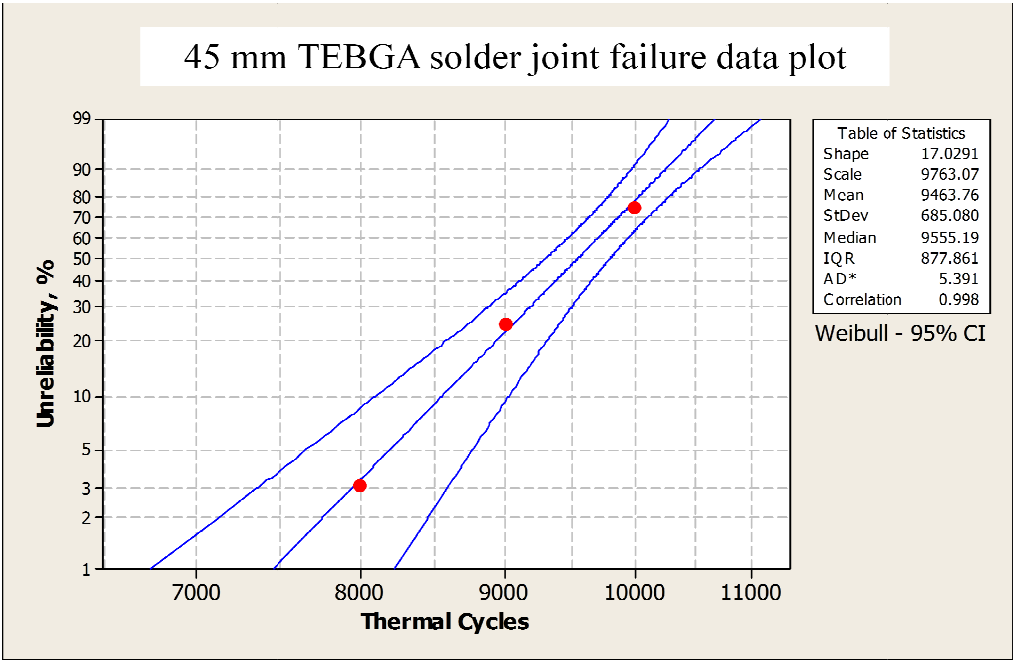
Figure 6-31 Reliability analysis using periodic resistance data (every 1000 cycles)

6.4.4.8 Failure rate estimation

As discussed in Chapter 5, package reliability failure rate can be measured by a failure unit (FIT), which is defined as the number of expected device failures per billion parts of hours/cycles. The failure rate for the die cracking and the thin film crack-

ing failures under use conditions (0 °C to 70 °C) is calculated and listed in Table 6-14 using an acceleration factor of 7.3. The results demonstrate that there is a clear decreasing failure rate of the data under both conditions. The failures caused by wafer sawing is screenable.

Table 6-13 Failure rate estimation from TEBGA test results

Number of cycles	Failure Rates (per 1000 cycles)	
	Resin blade	Diamond blade
250	0.937	2.163
500	0.238	0.488
1000	0.24	0.29

6.2.5 Discussions

The root causes of the die cracking/ILD cracking failures are initiated by the defects induced from the wafer sawing. Through the adoption of low impact wafer sawing, coupled with the issues from the die attach fillet height control and application of low stress materials, the impact of the defects can be controlled and reduced. New samples build using the improvement plan pass all the required reliability requests and provided customers a low failure rate for the lifetime of the product in the field. The estimation of the failure rate in the field applications provides confidence for reliability performance in the field.

The failure rate trend for the die cracking and ILD delamination is random and a constant failure rate can be demonstrated. The prediction of failure rate in the field applications will be estimated based on the reliability assessment results.

6.3 Reliability assessment of RCPs

6.3.1 Introduction

The package technology studied in this session is one type of WLCSPs which is constructed using singulated die instead of a wafer. The technology eliminates wire bonds or flip chips bumps, with simplified assembly processes. The key advantages of the packaging technology include:

- Package size reduction.

- Integrated package substrates

- No bonding wires or flip chip bumps needed

- Technology flexibility

The assembly process started by placing large number of singulated die on a panel (e.g. 200 mm circle plate) using pick-and-place equipment. The encapsulant is then screen printed to hold the die motionless on the panel so the alignment can be made during the I/O build-up process. The dielectric layers and thin film Cu metallization will be developed above the encapsulant to construct the circuits.

Figure 6-32 shows multiple packages in a panel carrier. Figure 6-33 shows the sche-

matic diagram of a package.
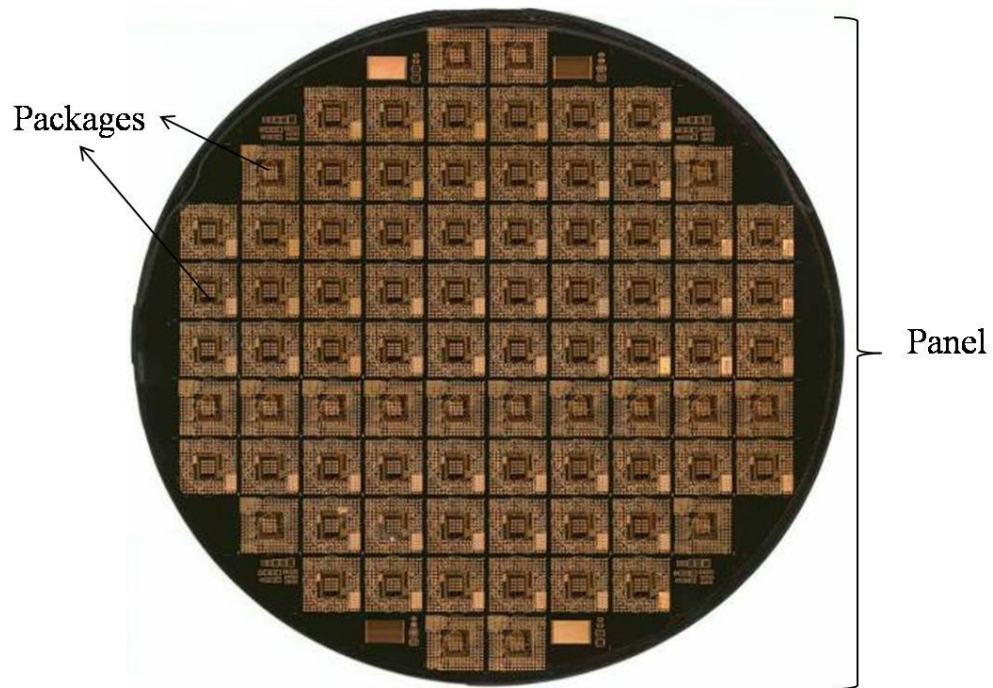
Figure 6-32 A panel with CSP packages
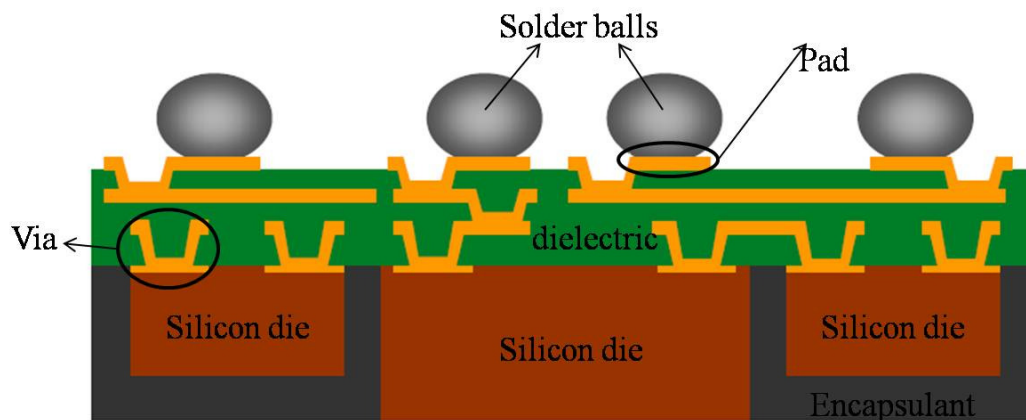
Figure 6-33 Stack-up view of the CSP package structure

193

6.3.2 Key failure mechanisms

During the package development, three key failure mechanisms are identified, including dielectric cracking failures, Cu trace cracking and the interface delamination between the EGP and encapsulant.

6.3.2.1 Dielectric cracking

The dielectric cracking seen in the build-up layers is shown in Figures 6-34 and 6-35. The cracking line is seen along the Cu traces underneath.   In many cases, the dielectric cracking on the surfaces are only cosmetic issues and might not be detectable by functional testing.
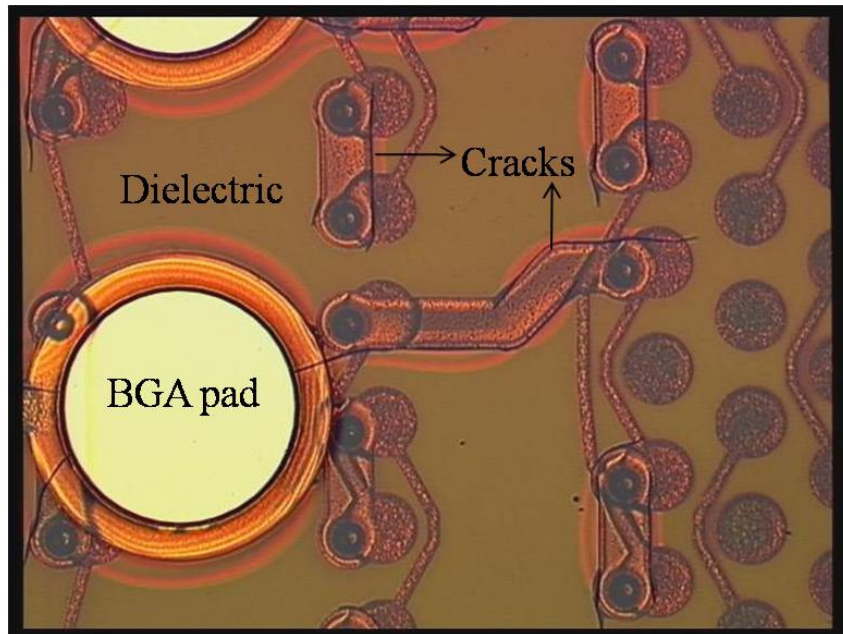
Figure 6-34 Dielectric cracking on the surface
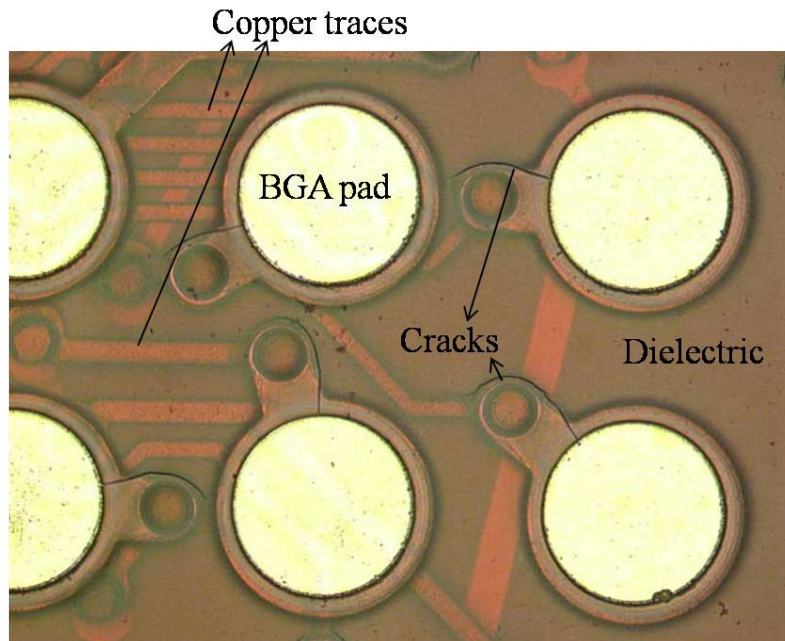
Figure 6-35 Dielectric cracking near the ball pads

6.3.2.2 Cu trace cracking

Cu trace cracking failures are the dominant failure mechanism observed from thermal cycling tests.   One of the examples related to the Cu traces cracking failures is shown in Figure 6-36.

The Cu trace cracking failures are related to the package design and layout, e.g. the trace density, the turning angle of the traces, and the structure of the embedded ground plane (EGP). The failure site of the Cu trace cracking is always near the edge of the EGP. A straight angle (depicted in Figure 6-37) can prevent the Cu trace cracking failures. The layouts of the Cu traces in the dielectric layers are critical to prevent the Cu trace from cracking.
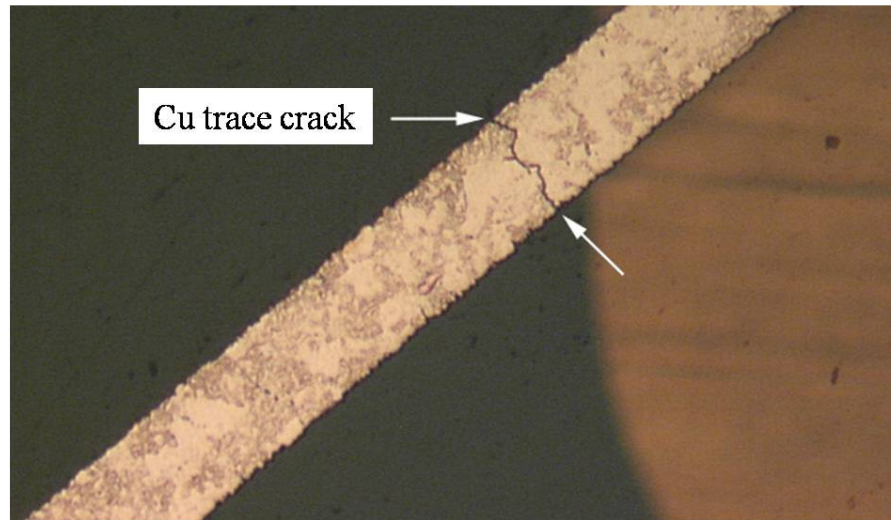
Figure 6-36 Cu trace cracking in build-up layers
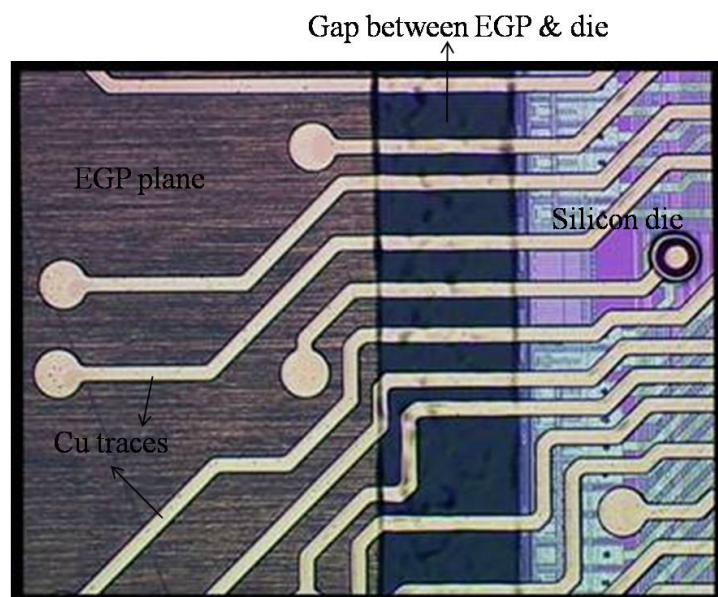
Figure 6-37 Layout optimization of the Cu traces in the package

6.3.2.3 Interface delamination

One of the unique structures in packaging technology is the EGP (an example show-

ing in Figure 6-38). The EGP is made of etched Cu and embedded in the dielectric

materials to improve the stiffness of the package, reduce the package warpage as well

as enhance thermal dissipation capability.   The   interface adhesion between the

EGP, the dielectric/encapsulation materials and EGP designed are critical to prevent

the delamination failures. Figure 6-39 shows a CSAM image with the interface de-

lamination observed.
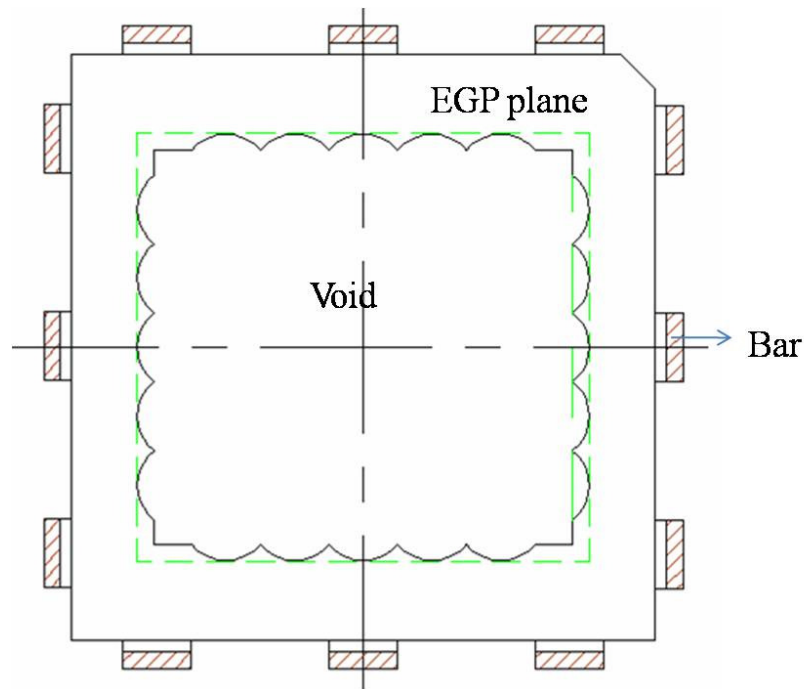
Figure 6-38 An example of an EGP design
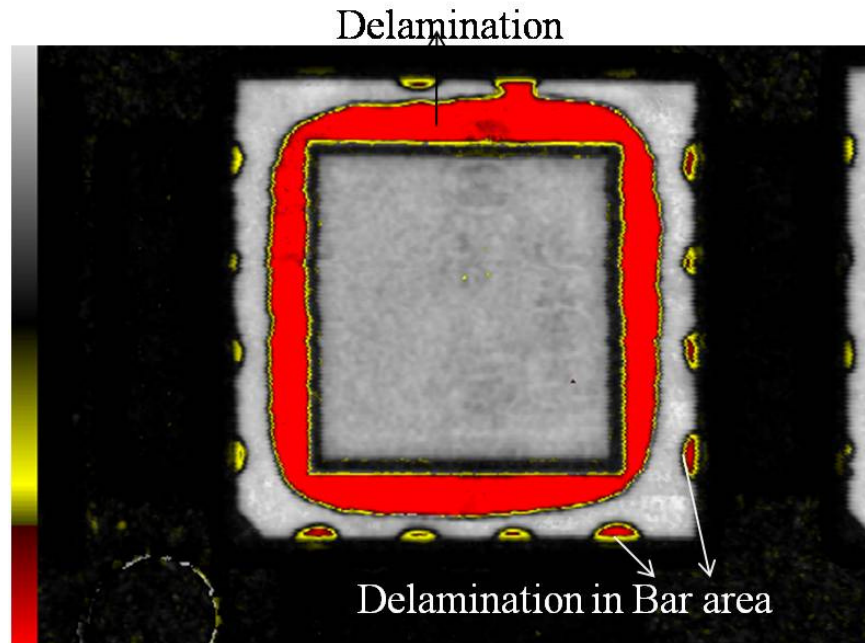
Figure 6-39 EGP layer delamination failure (CSAM)

EGP interface delamination failures might not show up as functional failures, but it is considered to be a high risk factor for the package reliability. The focuses of the failure mechanisms in this assessment are the Cu trace cracking and interface delamination. These two failure mechanisms are usually correlated with each other.

6.3.3 Materials and methods

6.3.3.1 Test vehicles

For component reliability studies, two different package sizes with similar structures are studied. One is 9 mm × 9 mm 2-layer package and the other is the 17 mm × 17 mm with a similar 2-layer structure. Table 6-14 lists the attributes of the test vehicles.

Table 6-14 Package attributes of RCPs

Categories	Test vehicles	
Package size	9 mm × 9 mm	17 mm × 17 mm
No. of metal layers	2 layers	2 layers
Die size	110 μ m bond pad and 130 μ m pitch	150 μ m bond pad and 225 μ m pitch.
Package thickness	0.65 mm	0.65 mm
Solder alloys	0.5 mm pitch	1.0 mm pitch.

Table 6-15 Assembly information for the board level reliability study

Category	Attributes
Package size	17 mm × 17 mm
Ball count and pitch	208, 1.0 mm pitch
Die thickness & die size	360 μ m & 6.81 mm × 9.2 mm
Solder sphere and solder paste	SnPbAg (63/35/2) & SnPb
Dielectric thickness	90 μ m
Package pad information	0.65 mm pad diameter/0.5 mm pad opening
Board pad information	0.5 mm pad diameter/0.625 pad opening
PCB thickness	0.62"

For the board level reliability study, specially designed daisy chain packages with 1.0 mm ball pitch are studied when mounted on boards. The board information is shown in Table 6-15. During the board level testing, the daisy chain resistance will be monitored in-situ so the failures will be detected real time. The failure criteria are 90%

199

increase in the daisy chain resistance value. In addition, the finishes of two different board pad surfaces are studied. One is Cu OSP finish and the other is NiAu surface finish.

6.3.3.2 Experiments set-up and descriptions

Thermal cycling tests are effective methods to activate the failure mechanisms mentioned in the previous section. In this study, the samples are sent through an MSL3 preconditioning test with a reflow peak temperature of 260 ^{o}C, then followed by air-to-air-thermal-cycling (AATC) tests. Two different thermal cycling conditions will be applied, one is -40 ^{o}C/125 ^{o}C and the other is -55 ^{o}C/125 ^{o}C. The units will be periodically taken out for electrical tests in order to evaluate their reliability. The stress testing approach is test-to-failures. For the component level reliability study, the samples are from three lots with 77 units per lot.

6.3.4 Experimental results discussions

6.3.4.1 The acceleration factors

Cu cracking failure is identified as the dominant failure mechanism during the thermal cycling tests. Tables 6-16 and 6-17 show the failure data collected for 9 mm × 9 mm packages. The number of failures observed under both thermal cycling conditions can be described in an exponential distribution, as shown in Figure 6-40. The test duration is 250 cycles beyond the qualification duration in order to generate more failures.

Table 6-16 Failure data for 9 mm x 9 mm packages under -40 $^{\circ}$C/125 $^{\circ}$C condition

Cycle interval	# Failure/# Pass
0-250 cycles	2
250-500 cycles	0
500-750 cycles	6
750-1000 cycles	1
1000-1250 cycles	1
1250 cycles + (suspended)	223

Table 6-17 Failure data for 9 mm x 9 mm package under -55 $^{\circ}$C/125 $^{\circ}$C condition

Cycle interval	# Failure/# Pass
0-200 cycles	1
200-400 cycles	4
400-600 cycles	2
600-800 cycles	1
800-1000 cycles	3
1000 cycles + (suspended)	226

In Figure 6-40, the distribution plots of the failure data clearly demonstrate a constant failure rate under both AATC conditions. Using the MTTF value (shown in Figure 6-40), the acceleration factor for the Cu cracking failure mechanisms under the two test conditions can be described as a function of the temperature range of the thermal cycling tests.
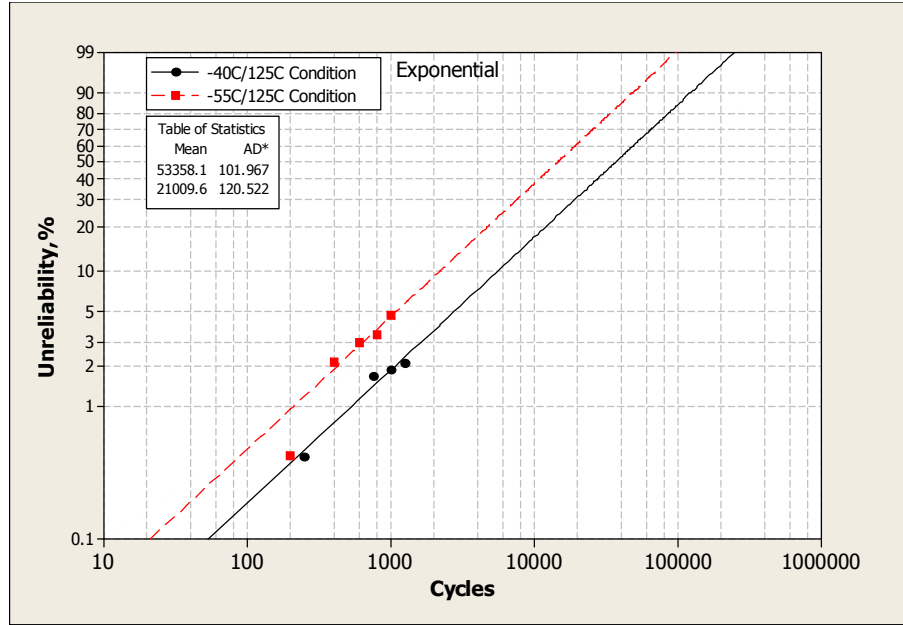
Figure 6-40 Exponential plot of failure data under two TC conditions

The acceleration factor for the Cu cracking failure mechanism without considering

the effect of cycle frequency can be expressed as $AF = \left(\dfrac{\Delta T_1}{\Delta T_2}\right)^n = \left(\dfrac{180}{165}\right)^n = 2.54$, n is

estimated to be 10.7.

The AF model for Cu trace cracking failures can be written as

$$AF = \left(\frac{\Delta T_1}{\Delta T_2}\right)^{10.7} \tag{6.1}$$

which might not be the best choice to predict the MTTF life at use conditions if assuming the same Cu trace failure mechanism expected in the field. It is a model developed based on the data from AATC and LLTS. In reality, LLTS environment is not typically present.

6.3.4.2 Failure rate estimation

Two lots of 9 mm × 9 mm packages are tested under -40 $^\circ$C/125 $^\circ$C AATC condi-tions. The failure data is recorded in Table 6-18. The tests are suspended after 1250 cycles instead of 1000 cycles for qualification needs. There are a total of 3 failures observed in Lot A and 3 failures in Lot B. The overall number of failures is 6 units after 1250 cycles. Total sample sizes are 236 and 239 respectively for Lot A and Lot B.

Table 6-18 Failure data for 9 mm × 9 mm packages under thermal cycling tests

Cycle Intervals	Lot A	Lot B
0-250 cycles	1	1
250-500 cycles	0	0
500-750 cycles	1	1
750-1000 cycles	1	0
1000-1250 cycles	0	1
1250 cycles+ (suspended)	233	236

When the failure data is plotted in both Weibull and exponential paper, a good fit is shown for both types. It shows that the exponential distribution can describe the fail-ure data trends very well. The Exponential plot is shown in Figure 6-41. A constant failure rate can be used for the failure data analysis.

Assuming a constant failure rate and using the Eq. [5.14], the upper bound of the number of failures is estimated to be 9, then the failure rate at -40 $^\circ$C/125 $^\circ$C AATC conditions is estimated to be 15300 FIT using the upper bound value. Based on the

AF formula calculated in the previous section, assuming the use condition is 25 $^{\circ}$C-70 $^{\circ}$C, the FIT value in the use condition is estimated to be about 580 FIT.
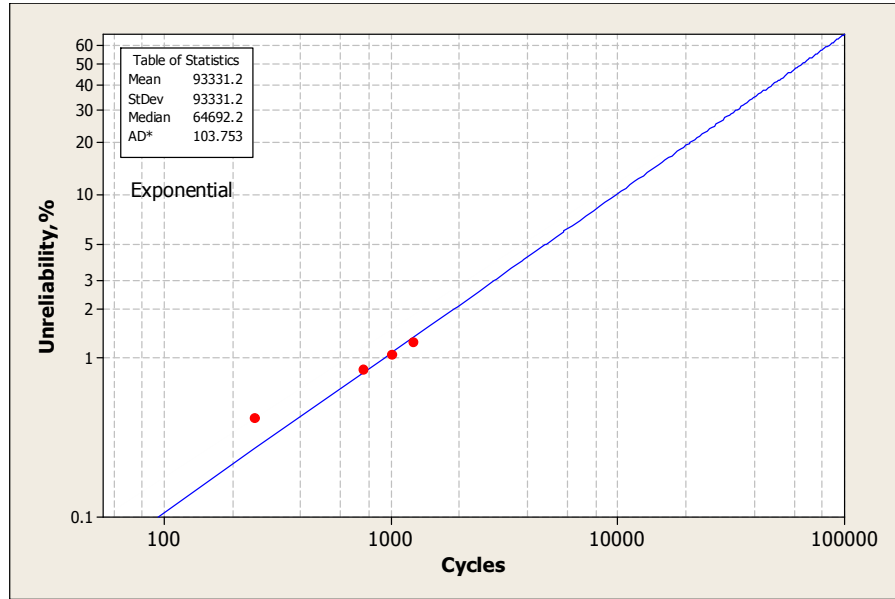
Figure 6-41Exponential plot for the failures under thermal cycling test

6.3.4.3 Comparison of the reliability performance between WLCSPs and FCMMAPs

A 9 mm × 9 mm flip chip FCMMAP package is studied under the -40 $^{\circ}$C to 125 $^{\circ}$C. AATC condition and the failure data is summarized in Table 6-19.

Table 6-19 Failure data for FCMMAP packages under AATC condition

Cycle interval	# Failure
0-250 cycles	0
250-500 cycles	0
500-750 cycles	0
750-1000 cycles	0
1000-1250 cycles	2
1250 cycles + (suspended)	173

Considering the test result within the interval (1250 cycles), the estimated upper limit of the number of failures is 4 using the Eq. [5.14], and the failure rate can be estimated to be around 18300 FIT, which is close to the estimation for RCPs under the test conditions (690 FIT at use conditions).

Considering only the qualification specification which required that 1000 cycles have zero failures, then the FIT can be estimated to be 650 FIT. The failure rate will be lower than it really should be. The technology has a similar predictive failure rate.

6.3.4.4 Solder joint reliability performance

6.3.4.4.1 The acceleration models

To study the solder joint reliability performance under thermal cycling conditions, 9 mm × 9 mm redistributed chip packages are mounted on PCBs. All the devices are tested to failure during the study. The number of failures is presented at equivalent time intervals, e.g. 200 cycle intervals. The cycles to failure data are shown in Table 6-20. The Weibull plot of the failure data is shown in Figure 6-42. Using estimated characteristic life data from the Weibull plot, the acceleration factor between 0 ^oC/100 ^oC and -55 ^oC/125 ^oC for the solder joint failures is calculated to be 2652/1361=1.95. Assuming the influences from cycle frequency and the maximum temperature follows the assumption used in lead free solders, then the power exponent n can be calculated as 0.94. So the acceleration models for the redistributed chip packages can be expressed as

$$AF = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{0.94} \left(\frac{f_a}{f_t}\right)^{0.136} \exp\left(2185\left(\frac{1}{T_{\max\_a}} - \frac{1}{T_{\max\_t}}\right)\right) \tag{6.2}$$

If using the models developed in Chapter 4 for lead free solders, the model can be expressed as

$$AF = \left(\frac{\Delta T_t}{\Delta T_a}\right)^{2.11} \left(\frac{f_a}{f_t}\right)^{0.6} \exp\left(2952\left(\frac{1}{T_{\max\_a}} - \frac{1}{T_{\max\_t}}\right)\right) \tag{6.3}$$

Table 6-20 Failure data observed from BLR study

Cycles Interval, cycles	Thermal Cycling (NiAu finish)	
	0C/100C (ss=42)	LLTS (-55C/125C) (ss=16)
0-400	0	0
400-800	0	0
800-1200	0	5
1200-1600	1	10
1600-2000	7	1
2000-2400	10	NA
2400-2800	13	NA
2800-3200	9	NA
3200-3600	2	NA
3600+	0	0
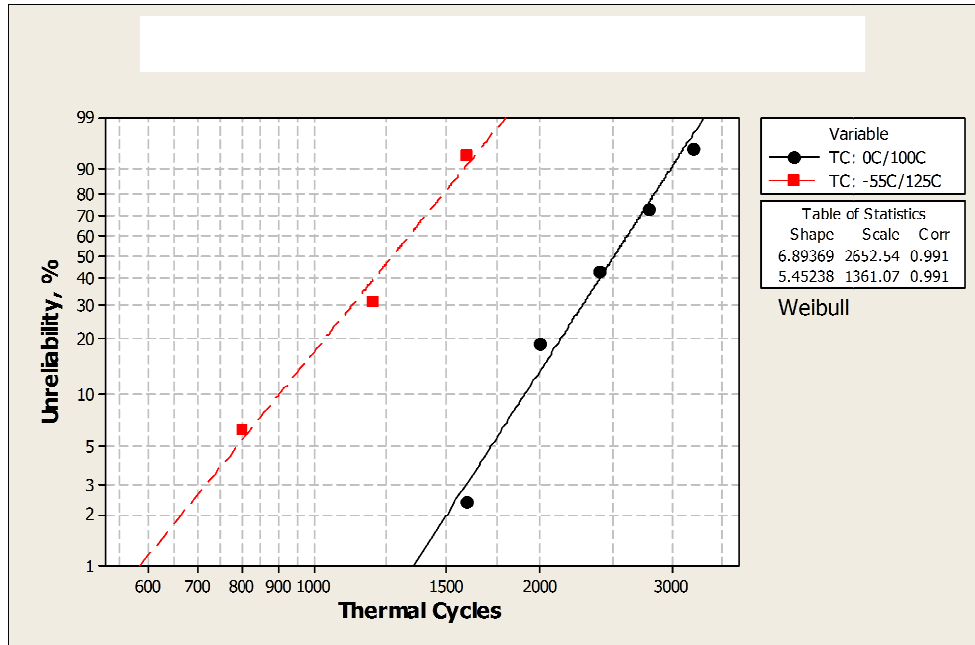
Figure 6-42 Weibull plot of cycles to failures from 9 mm RCPs

In order to confirm if the same model can be applied to other similar packages, 17 ×
17 mm redistributed chip packages with similar package structures and BOMs are
studied. Using the Weibull tools, the analysis results are summarized in Table 6-21.

Using the characterization life, the acceleration between A and C is 5787/2000=2.9,
which is much bigger than the AF of the same conditions for the 9mm × 9 mm RCP
packages. It is obvious that the same models can have issues to be applied to these
two different-sized packages even if they use the same BOMs and structures.

Table 6-21 17 mm x 17 mm WLCSPs with 7 mm x 9 mm die size

TC conditions		Cycles to 1% failure	Characteristic life, cycles
A	0 °C to 100 °C	4320	5787
B	-40 °C to 125 °C	1245	2860

The acceleration models can be expressed as

$$AF_{RCP} = \left(\frac{\Delta T_a}{\Delta T_t}\right)^{0.68} \left(\frac{f_a}{f_t}\right)^{0.136} \exp\left(2185(\frac{1}{T_{max\_a}} - \frac{1}{T_{max\_t}})\right)$$ (6.4)

6.3.4.4.2 The effect of the surface finish of the pads in the solder joint

The number of cycles of the packages (9 mm × 9mm) are obtained when mounted on the PCBs with different pad surface finishes. The details of the failures are listed in Table 6-22.

The failure data is then plotted in the Weibull paper and shown in Figure 6-43. Although there appears to be some reliability life improvement from NiAu finish to Cu OSP, the improvement of the NiAu pad surface finish over the Cu OSP finish is about 1.12x, which is not statistically significant. More data might be needed to assess the impact of the pad surface finishes.   In addition, when evaluating the impact on the solder joint reliability, there are more factors to be considered instead of pure cycles to failures.

Table 6-22 SJR failures data on two pad surface finishes

Cycles Interval, cycles	Air to Air Thermal Cycling (0 °C-100 °C)	
	Cu OSP	NiAu
0-400	0	0
400-800	0	0
800-1200	0	0
1200-1600	1	1
1600-2000	7	0
2000-2400	10	7
2400-2800	13	13
2800-3200	9	14
3200-3600	2	8
3600-4000	0	1
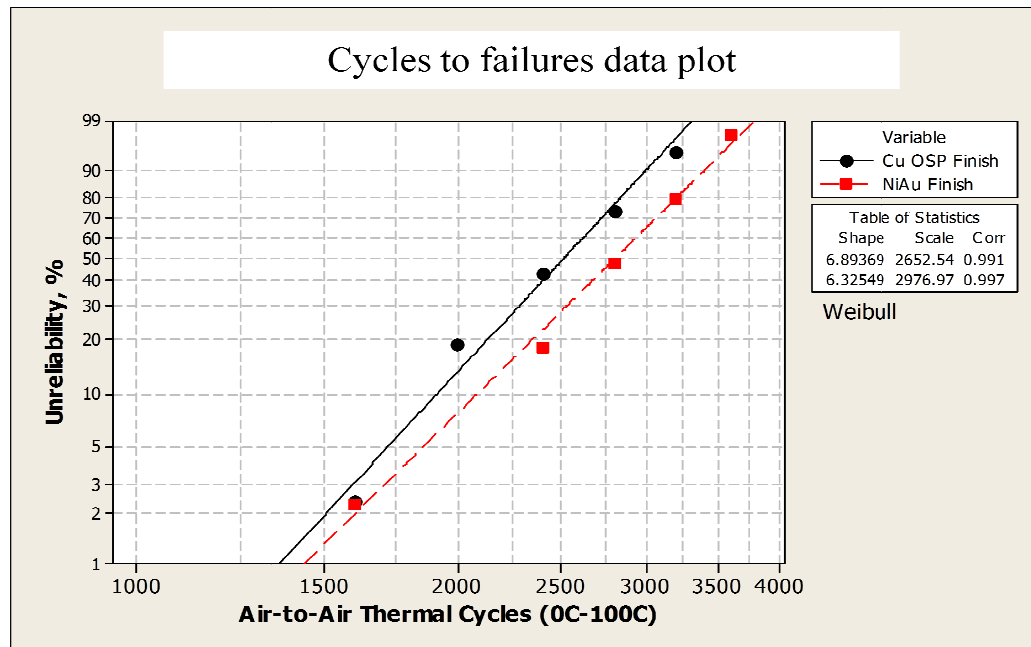
Figure 6-43 Impact of surface finish on the solder joint reliability performance

6.3.5 Discussions

The test-to-failure approach is applied in order to understand the failure characteristics and failure rate trends. Both component level and board level reliability performance are investigated.

Cu trace cracking is the dominant failure mechanism observed in the study of component reliability, its failure rate is described as a constant failure rate. In addition, the AF model for the failure mechanism can be described as a function of the ratio of the temperature range. Using this model, the number of cycles to failures can be estimated for the various parts under the use conditions.

The AF model for the solder joint reliability confirms the findings described in Chapter 5.

In addition, the test-to-failure approach demonstrated its efficiency and will be adopted in future package reliability assessments.

6. 4 Summary

In the field of semiconductor packaging, reliability assessment is always important for understanding failure mechanisms and fixing issues. Most importantly, it helps generate data to predict the reliability performance of packages under use conditions. However, in many cases, reliability testing does not fulfill the tasks of predicting reliability performance and failure rate estimation.

In this Chapter, the reliability assessment for two packaging technologies is discussed. To go beyond the qualification conditions, the focus is the test-to-failure method so that we can predict reliability and failure rates in field conditions.

Although the ultimate goal is to have zero failures at the end of the qualification tests, it is valuable in research to actually have failures, even if it is only two or three failures. Failure data provides knowledge about failure mechanisms and failure rate. If enough test conditions are applied, then AF models will be obtained for future reliability prediction.

The traditional test-to-pass approach does not have the advantages mentioned above. In addition, the failure rate based on zero failure tests does not provide accurate failure rate data or reliability prediction.

7. END-OF-LIFE RELIABILITY STUDIES OF FLIP CHIP BUMPS UNDER POWER CYCLING CONDITIONS

7.1 Introduction

Flip chip technology is one of the most advanced and high performance packaging technologies used today.   Figure 7-1 describes a schematic diagram for a flip chip BGA package.   Inside a FCBGA package, the solder bumps are the interconnects between the die and the substrates and are the key element for a robust package. In order to protect the bumps from fatigue failures, underfill materials are applied to fill in the gap between the die and substrate in order to protect the bumps by absorbing the thermal mechanical stresses generated during testing or field applications.
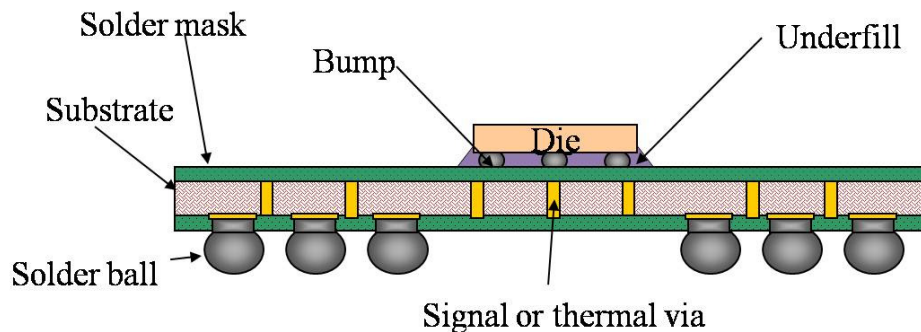
Figure 7-1 A diagram showing a flip chip package

The flip chip bumps are formed through a very complicated process, and will vary if different bump materials are used.   Figure 7-2 shows an example of the bumping process by which the solder bumps are plated on the UBM layers.
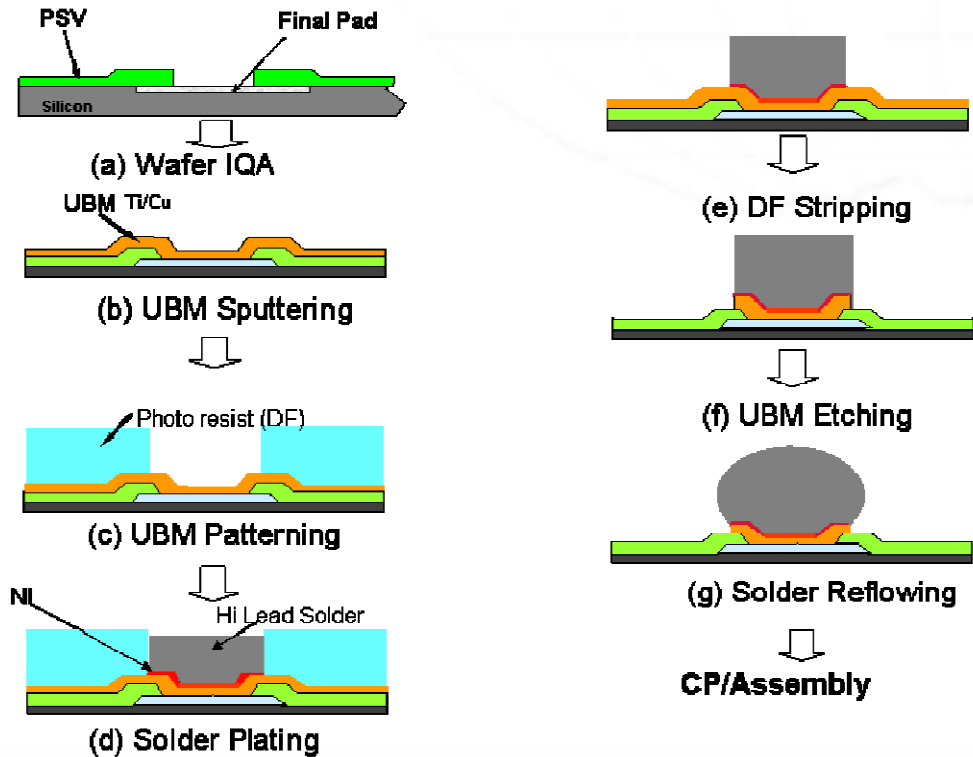
Figure 7-2 An example of bumping processes (plating processes)

Both UBM structures and bump materials will affect the interface material reaction and the interface microstructures, and will influence the bump reliability. The UBM usually consists of the seed layer (Ti), the adhesion layer (Cu) and the barrier layer (Ni). During the bumping process and subsequent assembly processes later on, the Ni and Cu contents in the UBM structure will react with the solder alloys to form the (Cu,Ni)Sn intermetallic compounds (IMC) which are necessary for good and strong bonds between the solder and the UBM layers [D. Li et al., 2006; H. Lu et al., 2006; R. S. Sidhu et al., 2007]. However, much thicker IMC layers will degrade the interface strength [H. W. Chiang et al., 2006; G. Y. Jang et al., 2005; M. H. Lu et al., 2007; J. O. Amistoso and A. V. Amorsolo, 2008] as well. On the substrate side of

the bump joint, eutectic solders on the Cu pads of the substrates will form the solder joints with the bump materials Figure 7-3 showed a typical solder joint between the die and the substrate.
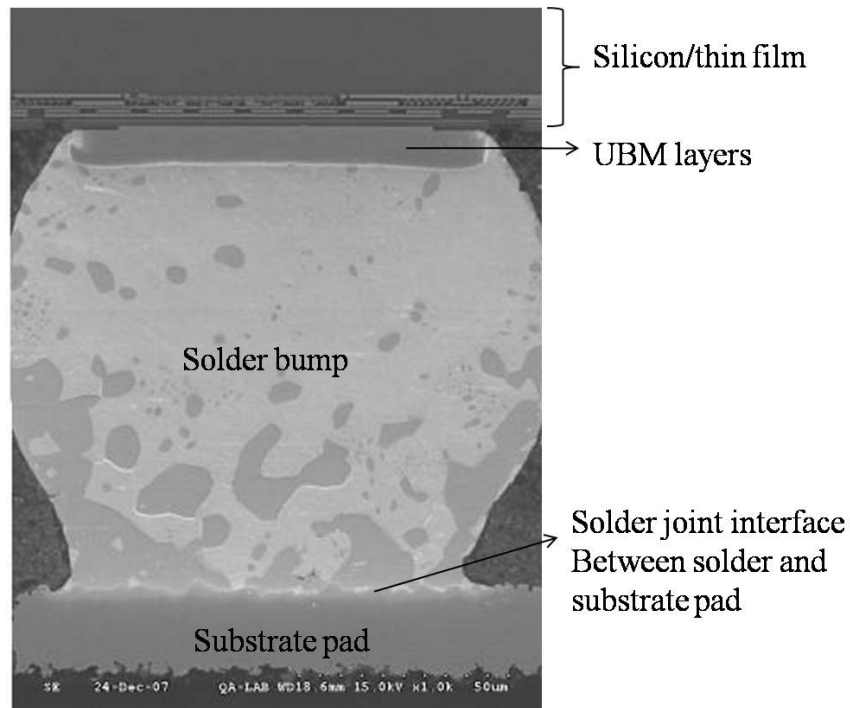
Figure 7-3 An example of a solder joint between the die and the substrate

Underfill materials, as expected, significantly improve the bump reliability under thermal mechanical cyclic conditions. However, underfill materials can transfer the stress to the die and significantly increase the risks of die and passivation failures, even the low-k dielectric materials in the silicon. Improper underfill materials will introduce other critical failure mechanisms in the die and low k dielectrics.

In addition, there are tremendous challenges to achieve highly reliable solder bump interconnects, especially with the following:

(1) the scale down trend for bump dimension, bump pitch and height

(2) the changes of types of bump UBM structures and bump materials

(3) the adoption of the extra low-k Cu die

(4) the complexity and thickness of the substrates

7.2 Review of solder bump reliability

A majority of the bumps in clip chip packages are made of solder alloys, either eutectic SnPb solders, high lead solders or lead free solders. Different bump materials will require unique UBM structures and dimensions, and even the underfill materials will be different too.

The reliability performance of the flip chip solder joints involve many unknown risks due to the small dimension and weak structures involved.

[Kim et al., 2005] describes that the formation of the IMC layers at the interfaces of solder bumps are critical and the grain coarsening does a major role to the crack growth of the solder bumps. [Wang et al., 2004] describes that the strength of Sn(Cu) bumps will depend on the microstructures at the interfaces and that the Sn (Cu) solder joints performed better than the eutectic solder in terms of shear strength. [Zhang et al., 2009] shows kirkendall voids will attribute to further IMC growth at the joints and the thickness of the IMC layers will degrade the interface strength of the bumps. [Yoon et al., 2004] reports that more reliable UBM stability can be achieved with a thicker Cu adhesion layer at the UBM structure. The shear strength will increase as well. [W. Chen et al., 2007] shows that the UBM thickness and dimension had im-

portant effects on the solder bump shear strength and reliability performances under the thermal cycling conditions. However, larger UBM and thicker UBM tend to introduce higher stresses. [Lu and Plumbridge, 2007] study the solder bump performance under thermal cycling and aging conditions and observe that repeated cycles will cause crack initiation on the surface of the solder bumps, and later the cracks will penetrate into the interior of the bumps. A higher cooling rate and a lower temperature peak of the profile will help reduce the cracks on the other hand. In addition, prolonged isothermal exposure will only result in micro structural coarsening and no cracking in the solder bumps. The typical bump reliability studies focus on the performance of thermal cycling. However, few studies are focusing on the reliability life and the prediction models of the bump joint reliability.

In this Chapter, the reliability performance of flip chip solder bumps will be studied through power cycling tests. Iso-thermal cycling tests (or thermal cycling) are tradiitionally used to detect any failures related to the CTE mismatches among the packaging materials. However, there will be no thermal gradient inside the packages during the test, including the solder bumps. Power cycling test, on the other hand, will see thermal gradients inside the packages during the tests. Most importantly, power cycling tests are the closest tests which simulate field applications.

Because of the failure, detection for flip chip bump joints are not as straightforward as expected. Traditional component level thermal cycling test combined with periodic automated test engineering (ATE) test will not be able to detect the bump failures

216

effectively. In the studies, the performance of the package/devices under tests will be monitored in-situ.

7.3 Test vehicles and experimental descriptions

7.3.1 Packages under testing

Three different package sizes are evaluated and the detail package attributes are summarized in Table 7-1.

Table 7-1 FCBGA package attributes

Attributes Items	FCBGA I	FCBGA II	FCBGA III
Package size (mm x mm)	25×25	33×33	27×27
Package ball count	468	820	1588
Die size (mm x mm)	6.7×8.3	12.8×12.8	14.8×10.8
Sub layer structure	6L (2/2/2)	8L (3/2/3)	8 L (3/2/3)
Underfill materials	UF_L1	UF_L1	UF_L1
UBM size (μm)	~95	~95	~95
UBM structure & materials	Sn5Pb95& Sn63Pb37	Sn5Pb95 & Sn63Pb37	Sn5Pb95 & Sn63Pb37
Bump diameter and height, μm	116 μm; 90 μm.	118 μm; 90 μm.	120 μm; 95 μm
Substrate thickness, μm	1.1	1.1	1.2
Min. bump pitch, μm	180	180	180
Substrate core thickness, μm	800	800	800
UBM structure	Ti/Cu/Ni	Ti/Cu/Ni	Ti/Cu/Ni
BGA solder alloy	SAC405	SAC405	SAC405

In addition, a variation of underfill materials is applied to evaluate the impacts on the bump performance. The assembly processes are the same for all the test vehicles.

7.3.2 Test set-up & descriptions

Temperature profiles are one of the most important factors for power cycling tests. Similar to typical thermal cycling profiles, the temperature profiles in power cycling will define the temperature range, the peak temperature the devices will operate, the ramp rate and the dwell time at peak and low temperatures. Table 7-2 shows an example of power cycling profiles.   Two maximum temperature values are studied in the evaluation, one is around 105 ^{o}C -110 ^{o}C which is the maximum temperature the package will be operating and the other is 65 ^{o}C-70 ^{o}C which is close to the Tg of the underfill materials.

In power cycling tests, FCBGA packages are mounted in the application boards which are then inserted into the testing systems. Each card will operate individually. The thermal profiles will be controlled by running program scripts constantly. The specially designed program scripts can power on and off the devices in order to achieve desired temperature profiles.   An example of the application board with the package mounted is shown in Figure 7-4. An example of temperature profile in a power cycling test is shown in Figure 7-5 with a test cycle time of ~15-17 minutes per cycle, where the dwell time at the peak temperature is around 5 -7 minutes.   The failure will be recorded when the system cannot execute the desired performance. For any failure, failure analysis will be carried out to validate the failure mechanisms.

FCBGA package mounted on the card

Figure 7-4 An image of the application board used in power cycling tests
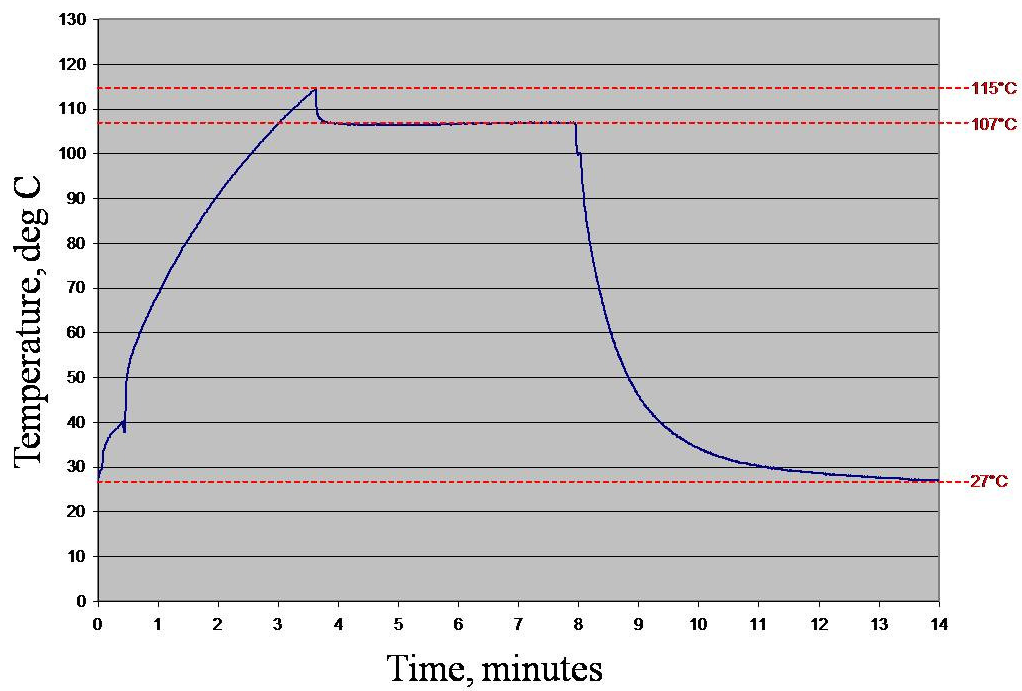
Figure 7-5 An example of the power cycling profile

219

Table 7-2 Power cycling conditions

Package sizes	Power cycling profiles	Remarks
	Condition 1	Condition 2
25 mm × 25 mm packages	Cycle time: 15 minutes; Peak temperature: 95 ^{o}C; Low temperature: 35 ^{o}C Dwell at peak temperature: 5-7 minutes; Ramp up rate: 0.4-0.5 ^{o}C/sec.	Cycle time: 15 minutes; Peak temperature: 70 ^{o}C; Low temperature: 45 ^{o}C Dwell at peak temperature: 5-7 minutes; Ramp up rate: 0.4-0.5 ^{o}C/sec.
33 mm × 33 mm packages	Cycle time: 15 minutes; Peak temperature: 107 ^{o}C; Low temperature: 27 ^{o}C Dwell at peak temperature: 5-7 minutes; Ramp up rate: 1.05 ^{o}C/sec.	Cycle time: 15 minutes; Peak temperature: 60 ^{o}C; Low temperature: 25 ^{o}C Dwell at peak temperature: 5-7 minutes; Ramp up rate: 1.05 ^{o}C/sec.
35 mm × 35 mm	Cycle time: 15 minutes; Peak temperature: 105 ^{o}C; Low temperature: 25 ^{o}C Dwell at peak temperature: 5-7 minutes; Ramp up rate: 1.05 ^{o}C/sec.	NA

CSAM techniques are used to help detect any bump failures only when the crack failures are significant (as shown in Figure 7-6).   However, a cross section analysis shall be done to validate CSAM observations. Figure 7-7 shows a cracked bump near the substrate side after cross section analysis. Usually the bump cracks are hair line cracks.

White bump
(bump cracks)

White bump
(bump cracks)
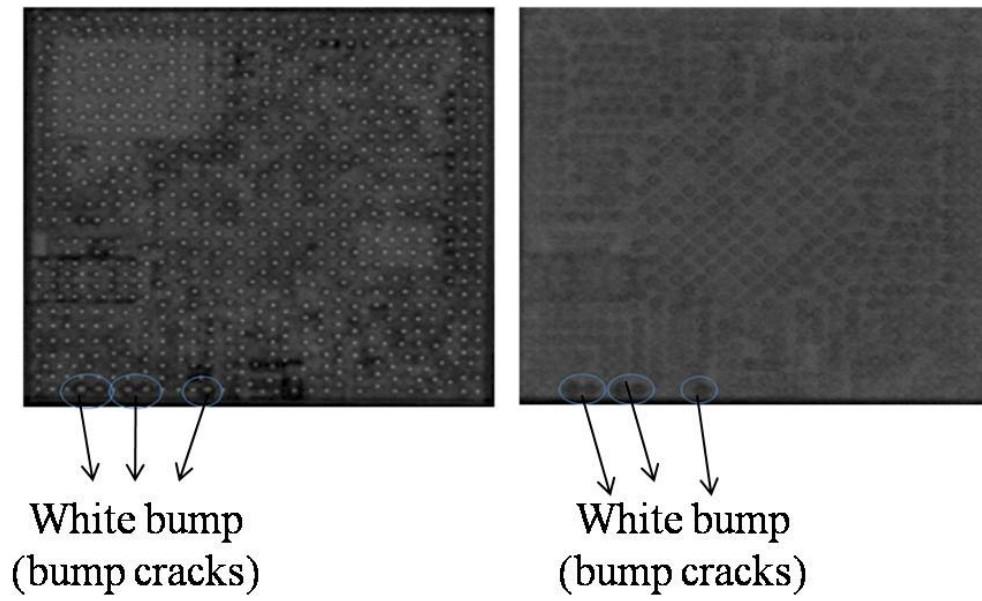
Figure 7-6 Bump failure detection through CSAM

Silicon/
thin film

UBM

Solder bump

crack

Substrate pad
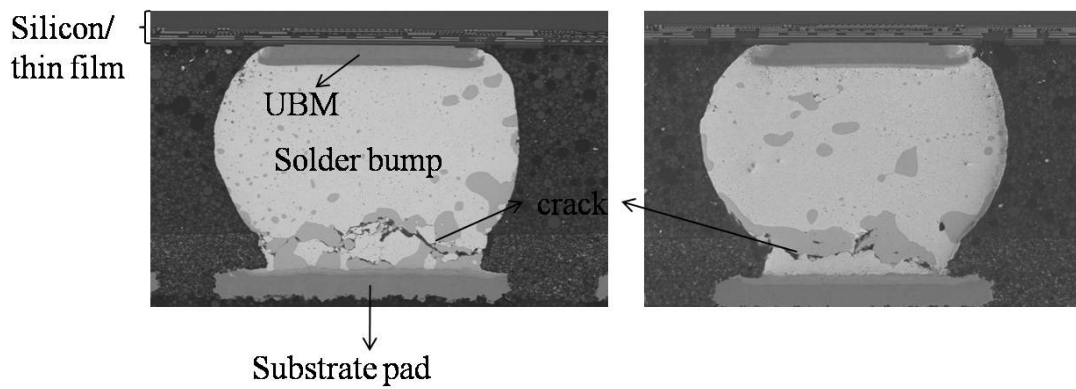
Figure 7-7 Bump cracking failures after 1650 cycles

7.4 Data analysis and discussions

7.4.1 Field failure data assessment

Intermittent flip chip solder bump failures are reported in the field applications (shown in Table 7-3). The failure analysis confirms the root cause is bump cracks as shown in Figures 7-8.

The time-to-failure data for the first 10 months from Table 7-3 is plotted in Figure 7-9. Clearly, the failure data fits the Weibull plot well with a estimated shape parameter of 1.25. Based on the failure distribution analysis,   the estimated 1% cumulated fail time is 5 months, 2% cumulated failure time is 7 months, 5% cumulated failure time is 14 months.

Table 7-3 Field failure summaries of Company B

Months in field	Number of failures of Product Lots, x1000								
	A	B	C	D	E	F	G	H	I
0		5					1		7
1	9	12		4	4	10	1	8	22
2	18	12		10	12	19	6	10	41
3	12	10	1	20	28	8	10	21	35
4	11	8	3	17	11	24	11	9	24
5	11	37	0	11	20	8	20	7	28
6	11	35	1	12	15	4	13	7	36
7	8	33	3	20	15	24	17	9	25
8	13	46	3	22	12	22	22	22	52
9	9	33	3	21	14	24	39	18	58
10	15	54	6	20	30	27	42	16	68
11	31	79	14	59	24	49	59	17	19
12	45	80	10	56	31	65	66	10	
13	33	137	10	62	31	78	18		
14	69	185	17	69	40	28			
15	65	238	18	65	13				
16	89	263	17	24					
17	95	270	7						
18	84	52							
19	25								
# of Fail	653	1589	113	492	300	390	325	154	415
Total	6065	14469	899	7539	5002	9208	7018	3107	11626
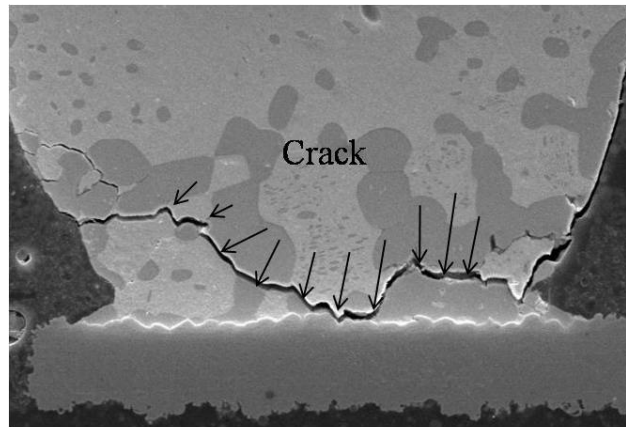
Figure 7-8 Bump cracking seen infield failures
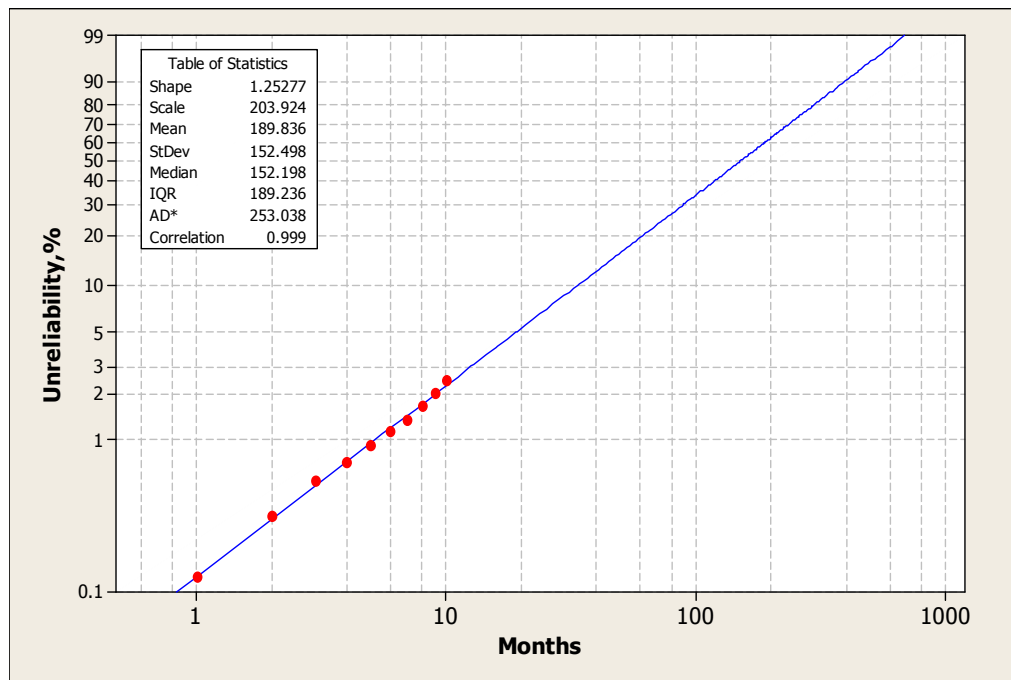
Figure 7-9 Weibull plot for field failures in 10 months

The distribution analysis for each individual lot is analyzed and the results are summarized in Table 7-4.

Table 7-4 Weibull analysis summary for lots listed in Table 7-3

Lots	Life at Certain CDF %, Months				
	1%	2%	5%	10%	MTTF
Lot A (β=1.51)	4.76	7.57	14.1	22.66	91
Lot B (β=2.07)	6.9	9.68	15.17	21.46	56.24
Lot C (β=2.8)	6.83	8.76	12.2	15.8	31.4
Lot D (β=1.7)	5.6	8.44	14.6	22.3	74.4
Lot E (β=1.52)	4.32	6.84	12.6	20.23	80
Lot F (β=1.75)	6.07	9.06	15.45	23.3	75.3
Lot G(β=2.1)	6.2	8.65	13.5	19.02	49.3
Lot H (β=1.17)	3.02	5.48	12.1	22.3	139
Lot I (β=1.18)	3.8	6.86	15.1	27.9	179
Average	5.3	6.9	13.9	21.7	86.2

Obviously, the shape parameters of the failure data from each lot are larger than 1,

indicating a wear-out failure mechanism for most of them. However, a couple of

lots did show shape parameters close to 1 (Lots H and I), which can fit well in an ex-

ponential distribution and be described as a constant failure rate. The possible reason

for that phenomenon is that the variation of the use conditions in the field made the

failure trends shown up as a constant failure rate even though individual bump fail-

ures are fatigue induced. For instance, each failure unit might go through different

temperature profiles, e.g. peak temperature history and dwell time. When the number

of the failures is analyzed altogether, the results show a constant failure rate. This

observation supports the constant failure approach even for solder bump failures in

the field application. During lab tests, in general, wear-out failures will be observed due to the well controlled test conditions, which mean an increasing failure rate.

7.4.2 Power cycling test results discussions

It is found that the solder bump failures are difficult to validate during the traditional qualification tests. In many cases, the failed parts will pass ATE tests unless there are significant permanent failures. However, power cycling tests with in-situ performance monitoring is effective for picking up the failures, even the early intermittent ones.

7.4.2.1 Power cycling failure data characterization and acceleration models

(1) FCBGA I packages

Two power cycling conditions are conducted with FCBGA I packages and Table 7-5 lists the cycles-to-failure data. Under power cycling condition of 35 ^{o}C to 95 ^{o}C, there are total 22 failures observed and 3 units are suspended. Under power cycling condition of 45 ^{o}C to 70 ^{o}C, there were a total of16 failures and 9 units were suspended. Failure analysis confirms bump cracking failures.

Table 7-5 Cycles to failures (bump crack) for FCBGA I packages

Failure Cycles @ (35 ^{o}C-95 ^{o}C)	Failure Cycles @ (45 ^{o}C-70 ^{o}C)
Failing cycles:	Failing cycles:
313, 381, 422, 449, 468, 485, 514, 571, 703, 722, 724, 752, 768, 929, 995, 1018, 1446, 1455, 1767, 1806, 1836, 1939.	4512, 5318, 5854, 6992, 7300, 8478, 8519, 8697, 10203, 11518, 11638, 11642, 13937, 13941.
Suspended:	Suspended:
1018, 3057, 3174, 4804.	14753, 15046, 15221, 15251, 15263, 15526, 15527, 15533, 15548.

Both Weibull and Log-normal distributions are applied to the failure data (Figures 7-10 and 7-11) and the results are summarized in Table 7-6. Obviously, the MTTF life increases dramatically when the operating temperature range changes from 35 ^{o}C /95 ^{o}C to 45 ^{o}C-70 ^{o}C conditions.   The acceleration factor is more than 12 between the two power cycling conditions. In addition, both Log-normal distribution and Weibull distribution can describe the failure data well, but the difference is not large.   Table 7-7 shows cycles to 1%, 5% and 10% failures from the Log-normal distribution analysis.

Table 7-6 Failure distribution parameter summary

Test Vehicle	Distribution Parameters		
	Distribution types	Power Cycling: 35-95C	Power Cycling: 45-70C
FCBGA I packages	Weibull	β = 2.08 η = 1154 cycles	β = 2.69 η = 13046 cycles
	Lognormal	Loc = 6.83 MTTF = 1170cycles	Loc = 9.37 MTTF = 13982cycles

Table 7-7 Break-down cycles to failures data using Log0normal distribution

% fail, cycles	Temperature range, 35 ^{o}C-95 ^{o}C	Temperature range, 45 ^{o}C -70 ^{o}C
MTTF	1170	13982
1% fail	187	2949
5% fail	299	4419
10% fail	383	5482
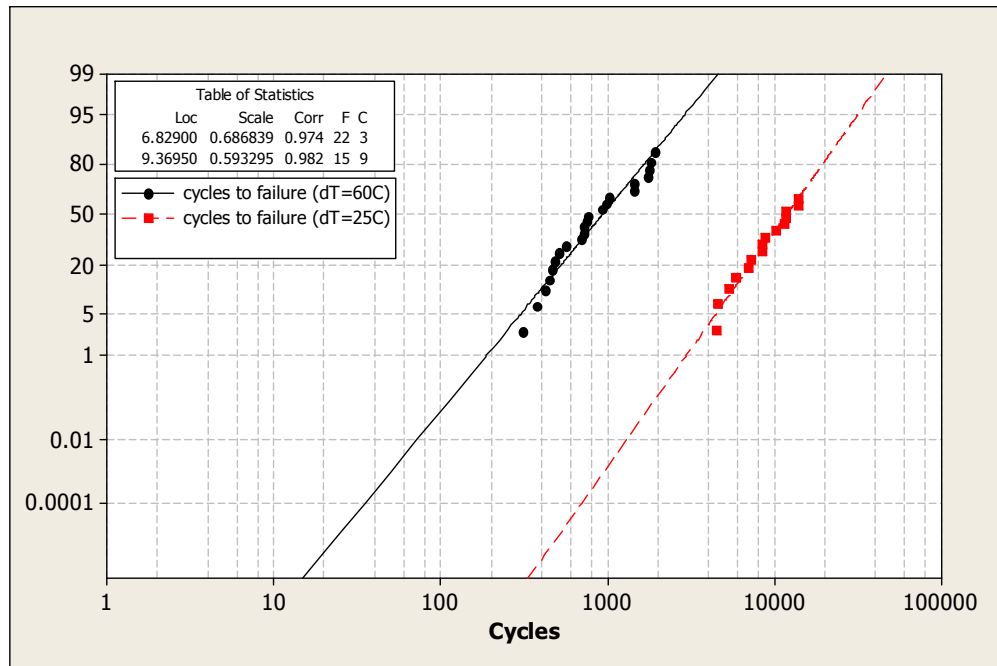
Figure 7-10 Log-normal plot of power cycling failures
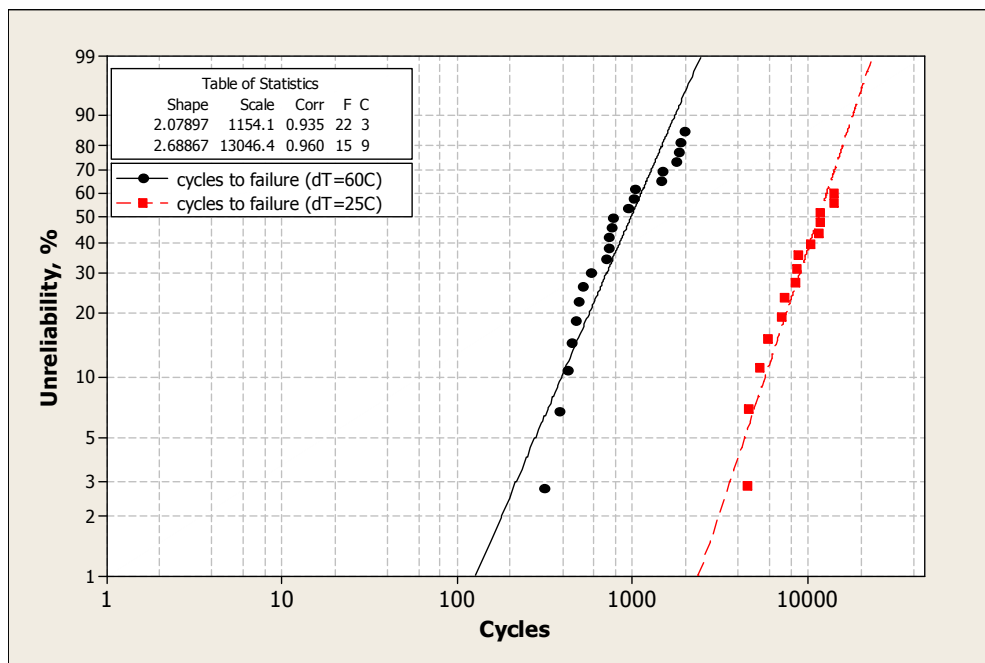
Figure 7-11 Weibull plot of power cycling failures

Applying a modified Norris-Landzberg model (E.q. [4.5]), if using the original model parameters (n=2 and γ=1616), the AF will be calculated around 8, which is about 34% less than the estimated AF value from the experiment. Table 7-8 lists the power exponent n estimation using Norris-Landzberg model. It is obvious that the parameter is much larger than the typical n=2 value used. It is much higher than the value estimated for BGA solder joints as well (discussed in Chapter 4).

The temperature range of the power cycling tests played an important role on the bump life time estimation, however, more importantly, a large impact of the glass transition temperature (Tg) of the underfill materials is observed too.   If the maximum temperature is above the Tg of underfill materials, the protection of the underfill on the bumps will be reduced and the bumps will be operating un-protected, which will lead to quick solder bump failures. It can be one of the reasons for the higher AF value observed. The influence of underfill materials on bump reliability will be discussed later.

Table 7-8 Power exponent n estimation from N-L models

N-L Model Parameter, n			
MTTF	10%	5%	1%
2.5	2.72	2.76	2.83

(2) FCBGA II packages

In case 2, 33 mm x 33 mm FCBGA II packages are tested under conditions of 27 ^{o}C - 107 ^{o}C and 25 ^{o}C-60 ^{o}C respectively.   The cycles to failure data is shown in Table

7.9. Both Log-normal distribution and Weibull distributions are shown in Figures 7-12 and 7-13).   The distribution parameters are summarized in Table 7-10.

Table 7-9 Cycles to failures data of FCBGA II packages

Cycles to Failures @ $27\ ^{o}C$-$107\ ^{o}C$	Cycles to Failures @ $25\ ^{o}C$-$60\ ^{o}C$
Failure cycles: 729, 968, 1000, 1061, 1132, 1382, 1582, 1596, 1654, 1687, 1742, 1871, 1885, 1999, 2001, 2049, 2158, 2375, 2469, 2526, 2550, 2561, 2780, 2803, 3299, 3444, 3988, 4151, 4435, 7290 Suspended at: 4054, 6665, 7415, 7642, 9222.	Failure Cycles: 25617,28696,24119,28929 28056,21089,30706,30070 30797,31449,32066,28848,31523 32748,32564, Suspended at: 33240,32860,32944,33214 33299,33645,32830,33329 33480,33736

Based on the data in Table 7-10, the acceleration factor for FCBGA II packages is calculated to be around 11-12, which is similar to the AF value obtained for 25 mm FCBGA I packages. Using the Norris-Landzberg model approach, the power exponent n is estimated to be 2.23 in terms of MTTF life, which is a little bit different from the value estimated for 25 mm FCBGA I packages.   Although there are some differences, the change of the package size does not dramatically affect the AF models. Similarly, the life is dramatically improved when the maximum operating temperature is below Tg of the underfill material.
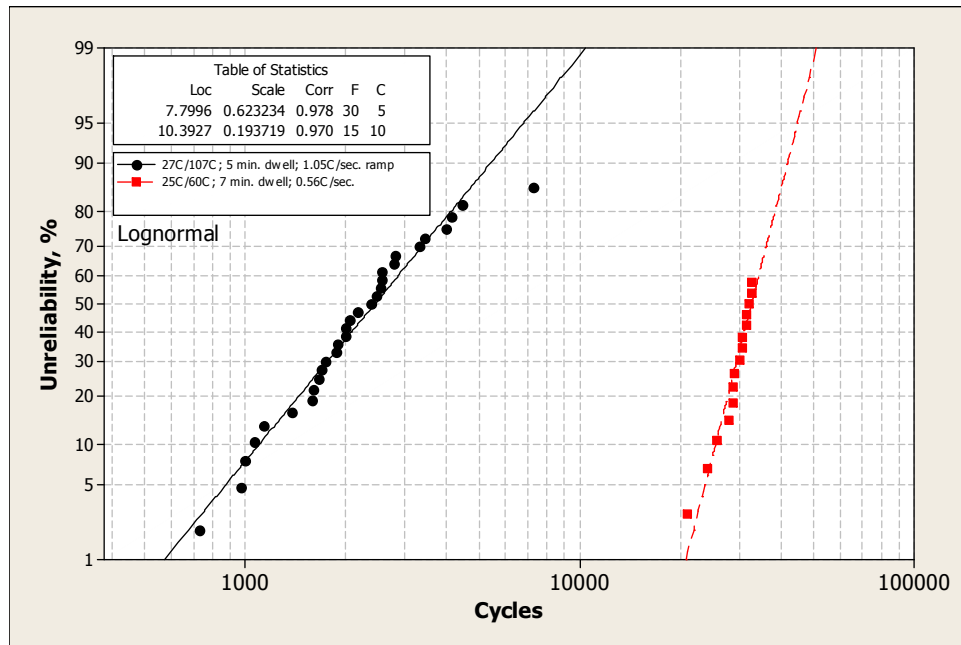
Figure 7-12 Log-normal plot of FCBGA II failures
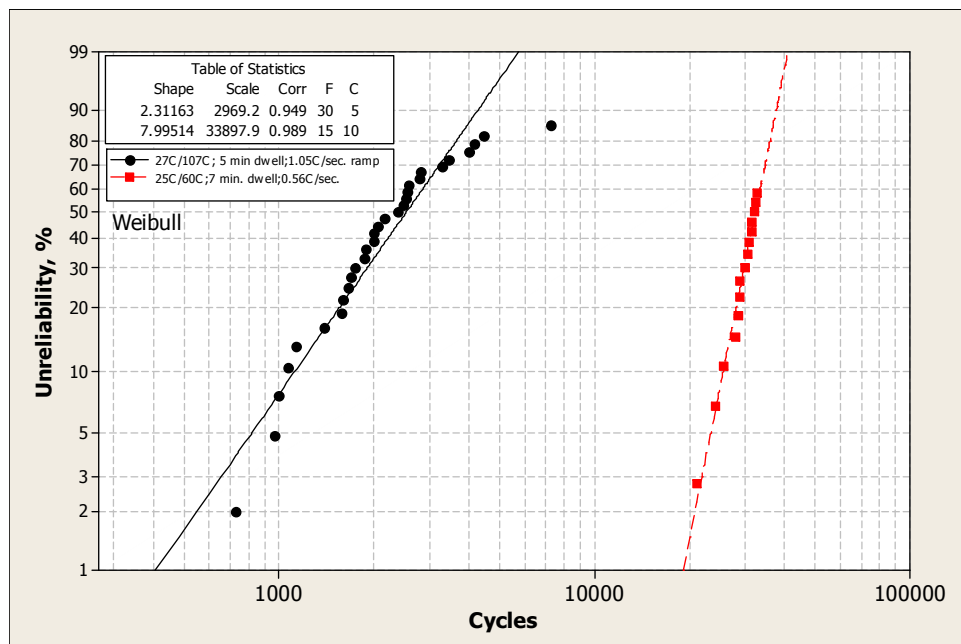
Figure 7-13 Weibull plot of FCBGA II failures

Table 7-10 Failure data analysis results

Temperature Range	Distribution	MTTF, cls
27 ^{o}C-107 ^{o}C	Weibull	2969
	Lognormal	2962
25 ^{o}C-60 ^{o}C	Weibull	33900
	Lognormal	32968

The analysis data from power cycling studies are compared with the field failure data. The comparison is shown in Table 7-11.

Table 7-11 Comparison of field failure data and modeling results

CPF, %	Test Results (35C-95C)	Test Results (45C-70C)	Field Data, months	Modeling Data @ use conditions (25C-70C; 5 cls/day), months
1%	187 cls	2949 cls	5	3
5%	299 cls	4419 cls	14	4.5
MTTF	1170 cls	13982 cls	86	14

It shows a large difference when the CPF% is increasing. The reason could be the assumption of the use conditions, or the field failure is following a different distribution. The modeling indeed is close to the field data when the CPF% is low.

7.4.2.2 Influences of underfill materials

As mentioned earlier, the purpose of the underfill materials is to protect the bumps from fatigue failures under thermal-mechanical cycling loads. However, the impacts

of the material properties (e.g. Tg and modulus) on the overall package reliability performance is not clear.

In this section, two types of underfill materials with different Tg and modulus are evaluated. Table 7-12 listed the key underfill material properties used in the test packages.

Table 7-12 Low Tg and high Tg underfill material properties

Underfill Materials	
Low Tg: 75 ^{o}C	High Tg: 130 ^{o}C
CTE: 32 ppm/^{o}C (<Tg); 120 ppm/^{o}C (>Tg); Young's Modulus: 7 Gpa	CTE: 27 ppm/^{o}C (<Tg); 95 ppm/^{o}C (>Tg); Young's Modulus: 9.2 Gpa

When the operating temperature is above the Tg, the underfill materials will exhibit a higher CTE and not be able to protect the bumps from the cyclic stresses. However, the advantage for low Tg underfill materials is that little stress will be generated on the die and it provides a better protection on the die. On the other hand, if the Tg of underfill materials is high, the bumps will be protected well at elevated temperatures. High risks will be present and there will be a high possibility to introduce die and passivation cracking failures, especially for low-k or ultra low-k dielectric materials. Figures 7-14 and 7-15 show low-k cracks in the silicon due to the use of high Tg underfill materials.
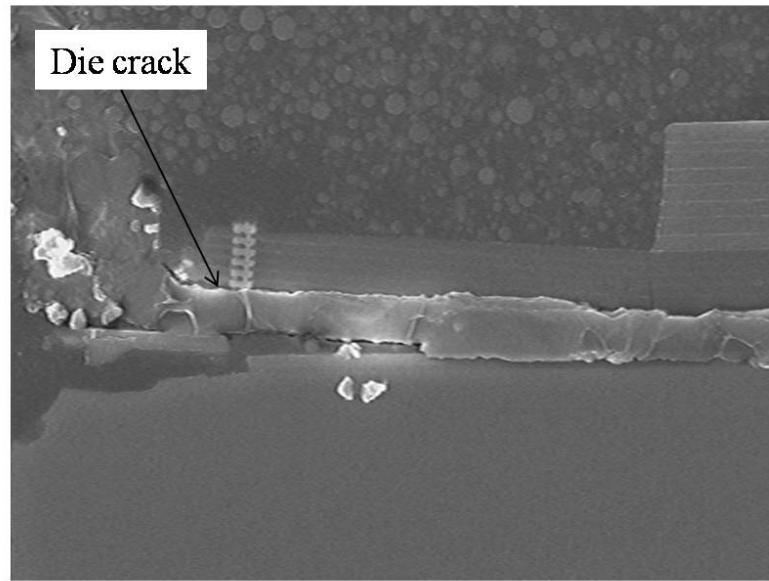
Figure 7-14 Low-k dielectric / die cracking failures
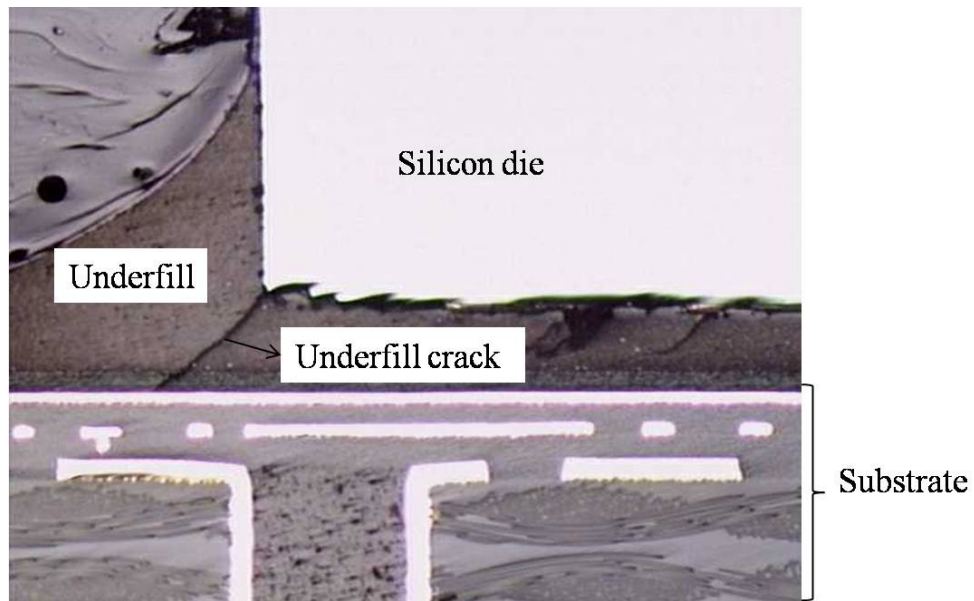
Figure 7-15 Underfill cracking in flip chip packages

33 mm FCBGA II packages are assembled using two types of underfill materials with high and low Tg respectively. The cycles to failures data are recorded in Table 7-13. The solder bumps are high lead solder alloys. The ramp rate is 1.05 $^{\circ}$C/sec. and the peak temperature is about 110 $^{\circ}$C in the power cycling profiles. The total cycle time is around 15-16 minutes per cycle.

Table 7-13 Cycles of failure data of FCBGAs using different underfill materials

Underfill Materials	Failure cycles
Low Tg (70 $^{\circ}$C) NL	Failing cycles: 501, 729, 916, 968, 1000, 1061, 1132, 1232, 1299, 1382, 1141, 1439, 1582, 1590, 1596, 1596, 1654, 1687, 1688, 1742, 1794, 1871, 1885, 1936, 1989, 1999, 2001, 2049, 2158, 2209,2375, 2469, 2487, 2515, 2516, 2526, 2550, 2561, 2780, 2803, 2846, 2988, 3299, 3385, 3444, 3988, 4089, 4151, 4435, 7290 Suspended @: 4054, 6665, 7415, 7551, 7642, 8225, 8385, 9222, 10998, 17010
Low Tg (102 $^{\circ}$C) NH	Failing cycles: 9593,10654,10677,10957,10995,11046,11932,12214,12258,12433,12617,12638,12793, 13192, 13256, 13452. Suspended @:12954,13003,13247,13315,13316,13455,13590, 13720, 13726.
High Tg (130 $^{\circ}$C) HH	Failing cycles: 10175, 10975, 11000, 11029, 11093, 11188, 11235, 11469, 11492, 11830, 11908, 11949. Suspended @: 8635, 10201,10414, 11273, 11786, 11909, 11914, 11965, 11988, 12022, 12157, 12179, 12334.

The Log-normal plots of the failure data listed in Table 7-13 are presented in Figure 7.16. Obviously, the MTTF life of FCBGA II packages using high Tg underfill materials is dramatically improved. In addition, the failure mechanism of FCBGA II packages when using high Tg underfill materials is that of the second level solder joint failures instead of the bump fatigue failures observed in FCBGA II packages when using low Tg underfill materials. The transition of failure mechanisms transition shows up as the obvious difference of the slope for the two distributions.

The hypothesis is that high Tg underfill materials will be able to protect the bump better, but post a high warpage of the substrates during the power cycling test. The warpage will apply higher stresses on the second level BGA solder joints, and ultimately cause the failures.

The effect of underfill materials on Eu solder bumps are studied using a large die and substrate structures. Figure 7-17 shows the Weibull plot of the study. For the specific package and die configuration, the life of the solder bumps are extended at least 9 times when the underfill materials are changed from low Tg to high Tg.
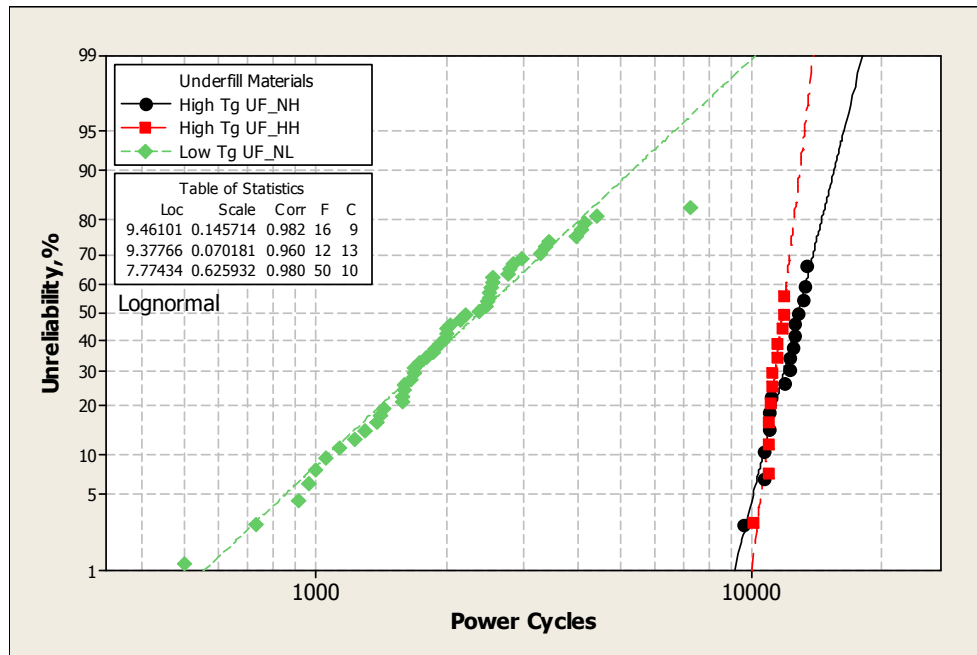
Figure 7-16 Distribution plot using low and high Tg underfill materials
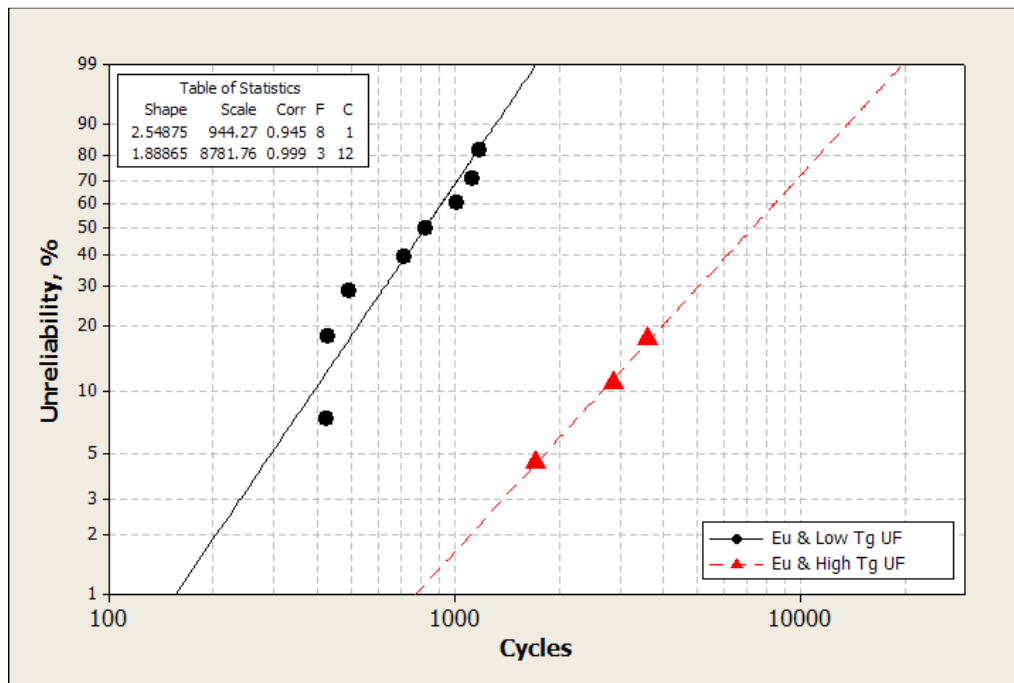
Figure 7-17 Impact of underfill materials using eutectic solder bumps

7.4.2.3 Influences of bump materials

When discussing the reliability of solder bumps, the performance of different bump materials have to be evaluated. Bump materials will demonstrate different creep rate, strength, and in addition, affect the interface microstructures and the solder joint life ultimately.

Two most popular bump materials are studied in this section, high lead bumps (95Pb5Sn) and eutectic bumps (37Pb63Sn). Figure 7-18 and Figure 7-19 show the microstructures of the high lead bumps and Eutectic solder bumps at time zero and Figures 7-20 and 7-21 show samples after certain stress cycles. It is obvious that the microstructure of both types of materials have dramatically changed after stress tests. The grain size grows in both structures. The high lead bumps show non uniform structures but eutectic bumps show more uniform microstructures even after cycling stresses. The high lead bumps show obvious Sn rich regions close to the joint interface after cycling stress which can be the starting point for cracking failures.

UBM

Solder bump
(high lead)

Substrate pad
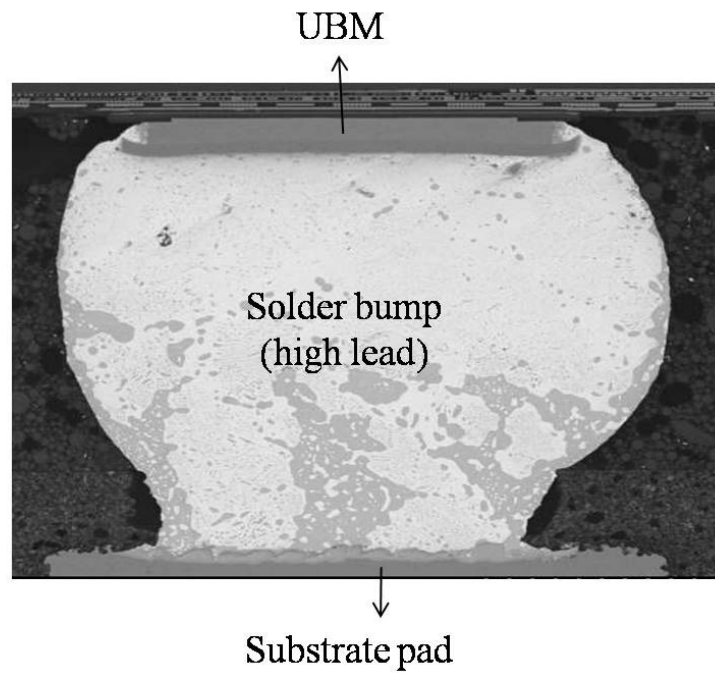
Figure 7-18 High lead solder bump /joints

Solder bump
(Eutectic)
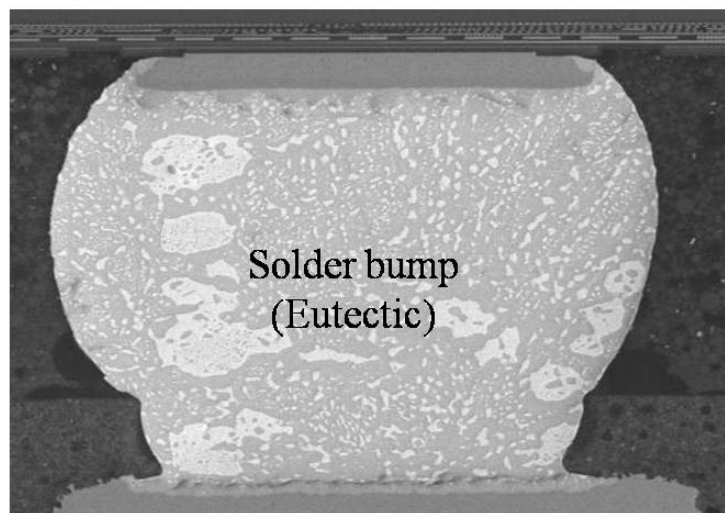
Figure 7-19 Eutectic solder bump joints
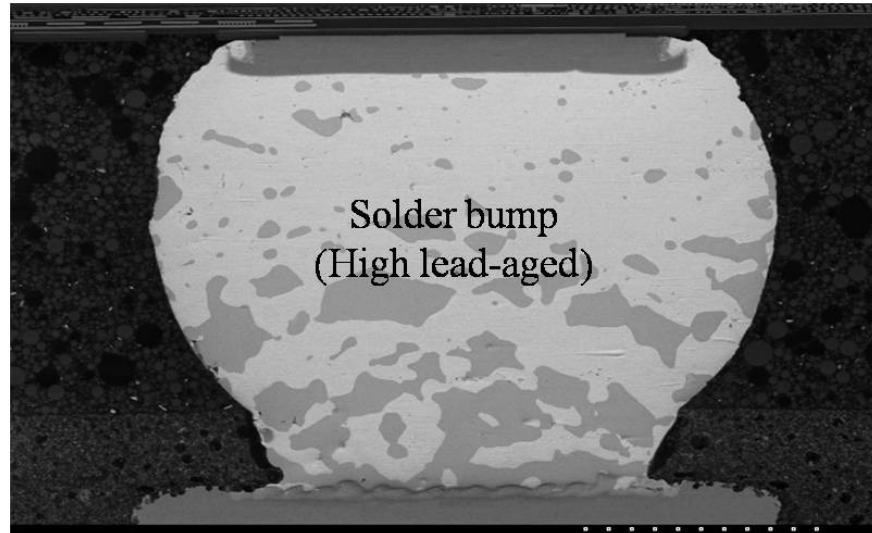
Figure 7-20 High lead solder bump after 4500 cycles
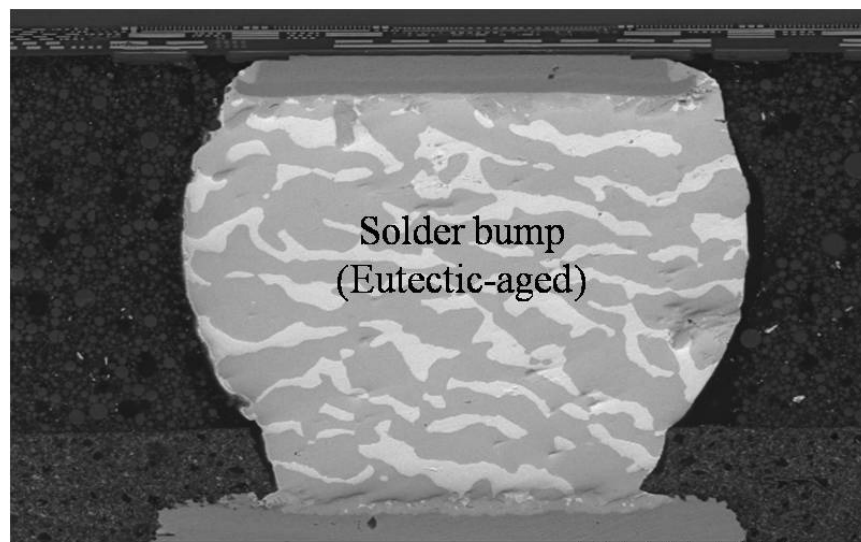
Figure 7-21 Eutectic solder bump after 4500 cycles

33 mm FCBGA II packages using eutectic bumps and low Tg underfill materials are studied under power cycling test with a temperature range of 27 ^{o}C to 107 ^{o}C. The

241

cycles to failures data is recorded in Table 7-14. No bump failures are observed and the current cycle counts are well beyond 25000 cycles. Experimental data shows Eutectic solder bumps will significantly extend the cycles to failures where high lead solder bumps will fail much earlier, regardless of what underfill materials used in the packages.

Table 7-14 Cycles to failure data of FCBGA II packages using eutectic bumps

Cycles to Failures @ 27 ^{o}C to 107 ^{o}C
Failure cycles: 11154 (substrate cracking), 28056,24881, 27038, 25413, 28943, 25060, 23913, 29819
Current cycles:
22692, 25187, 31089, 23945, 31729, 31993, 23615, 23748, 30874, 31757, 31493, 31452, 24345, 25010, 24360, 24325.

For a small die and package structure, there is no valid failure observed using eutectic solder bumps. While using a large package and die size structure, the failures are collected, then plotted in Weibull paper, as shown in Figure 7-22. It obviously shows that eutectic solder bumps outperform HL solder bumps at least 5 times using low Tg underfill materials. In addition, the maximum operating temperature dramatically impacts the fatigue life of the bumps in the similar configuration.
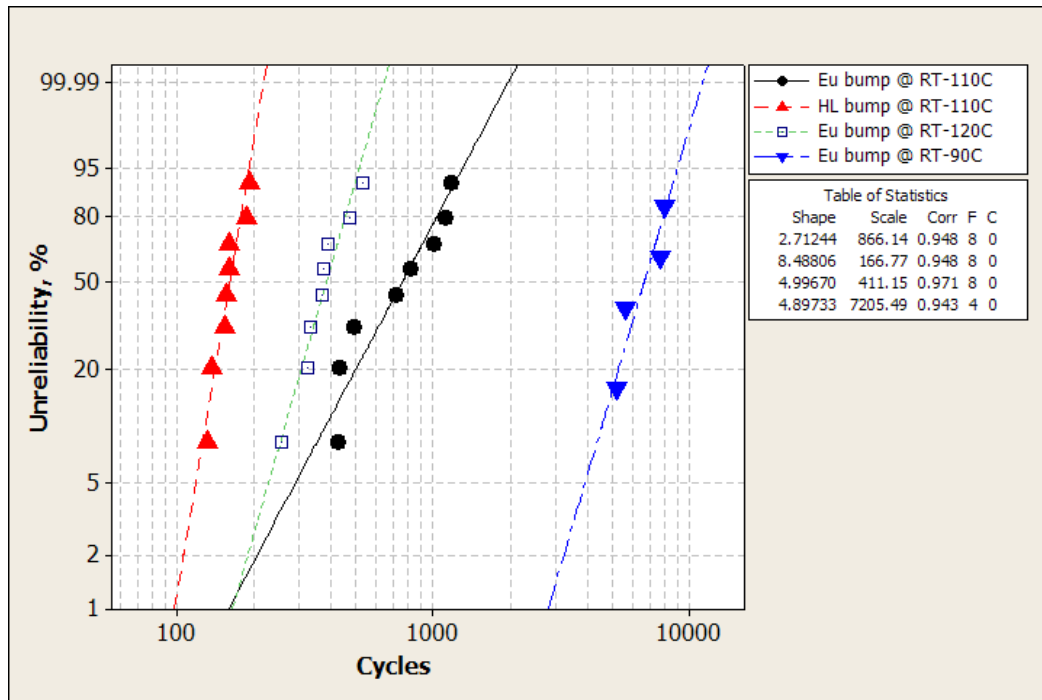
Figure 7-22 Reliability of eutectic solder bumps in a large package/die

7.4.3 Failure rate estimation

In general, solder bump failures are described as worn-out failures, which means the failures can be plotted in a Weibull paper and the shape parameters of Weibull distribution will be much larger than 1. Under controlled isothermal cycling conditions, this is absolutely true.

However, the failure data collected from power cycling tests do not always demonstrate this assumption. For example, the estimated shape parameters for both Lots H and I in Table 7-4 are close to 1. As expected, the failure data fit well in an exponential distribution instead of a Log-Normal distribution, which is different from traditional worn-out failures.

One of the reasons for a good exponential distribution fitting are the large variations in the field application conditions. This means that there can be differences in peak temperatures that the parts will experience, including user environments, as well as the programs run by the customers which will influence the thermal profiles. These variables will let the parts experience different power cycling conditions in the field.

In order to assess the hypothesis, studies are carried out using 35 mm × 35 mm FCBGA III packages under power cycling conditions. Table 7-15 summarizes the failure data collected and Figures 7-23, 7-24 and 7-25 show various distribution plots, including the Weibull plot and Exponential plots.

Table 7-15 Cycles to failure data for 35 mm x 35 mm FCBGA III packages

Cycles	Peak temperature, ºC	Fail/Suspension
3640	99	1 Fail
926	106	1 Fail
1753	103	1 Fail
4596	101	1 Fail
1220	109	1 Fail
8190	104	1 Fail
2783	102	1 Fail
11659	99	1 Fail
11350	100	1 Fail
12775	106	1 Fail
12784	93-101	10 Suspended
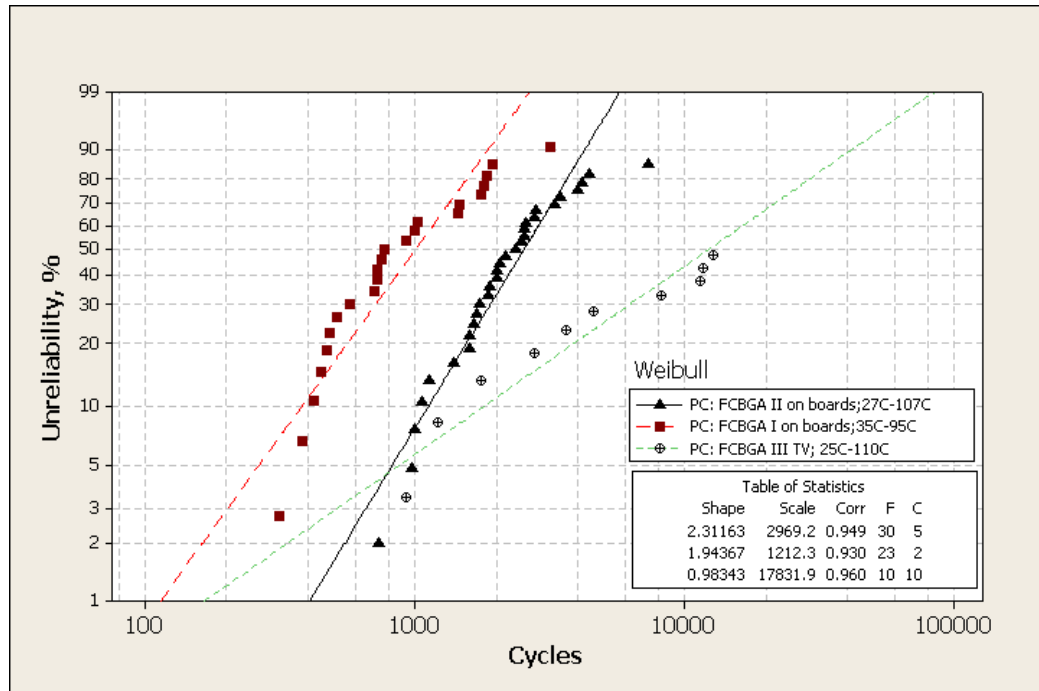
Figure 7-23Weibull distribution of FCBGA III power cycling failures
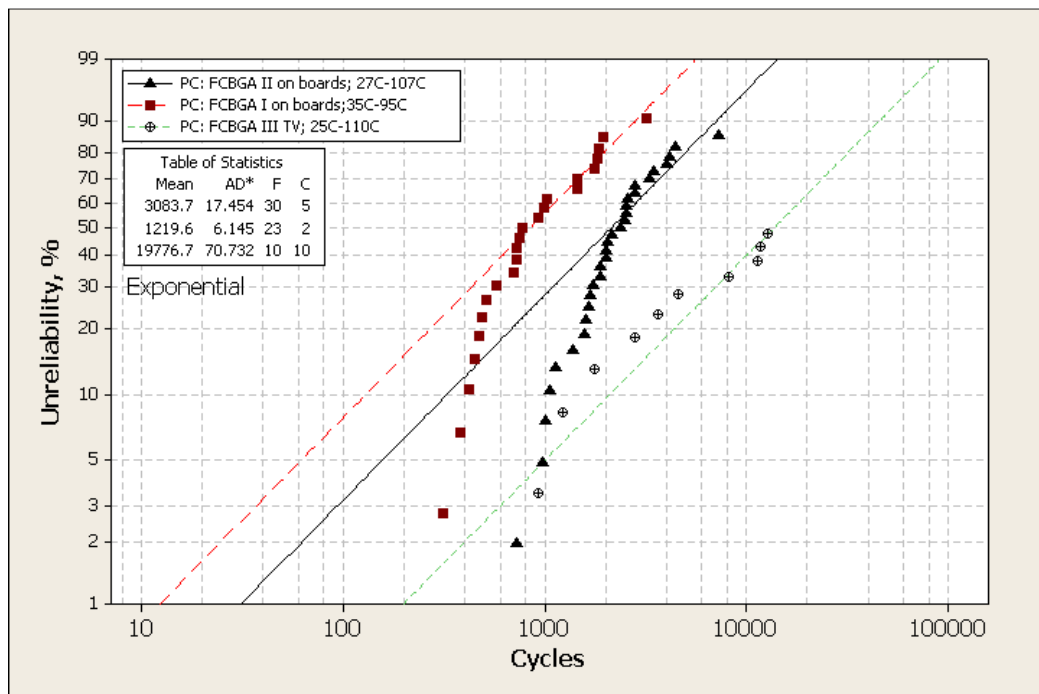
Figure 7-24 Exponential distribution of FCBGA III power cycling failures

245
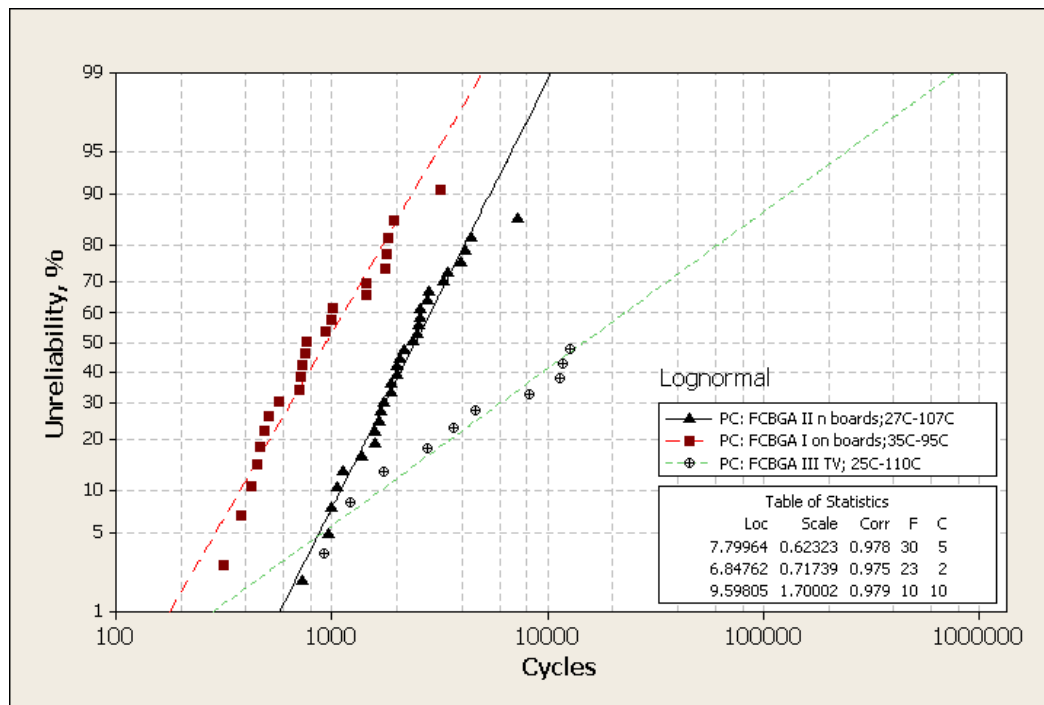
Figure 7-25 Log-normal distribution of FCBGA III power cycling failures

For each plot, three fit lines of the failures are presented for FCBGAI, FCBGAII and
FCBGA III packages. The targeted power cycling conditions for all three packages
are similar, however, due to the heating mechanism used, FCBGA III packages are
tested using a much wider peak temperature range. However, both FCBGA I and
FCBGA II packages are studied with a very tightly controlled peak temperature. The
distribution plot for FCBGA III packages is significantly different from those for
FCBGA I and FCBGA II packages. The failure rate from all three tests fit the Wei-
bull plot very well. However, the failure rate for FCBGA II and FCBGA I does not
fit well with exponential distribution.

However, the failure data from FCBGA III packages shows a very good fit in exponential distribution, which usually describes the failure data in a constant failure rate. The large variation of the peak temperature for FCBGA III failures is thought to be the reason for the random failures.

It is possible that a constant failure rate can be used for the field failures, even for solder bump failures, traditionally considered as a wear-out failure mechanism, based on the failure data collected in the lab testing.

7.5 Summary and discussions

Solder bump joint reliability is one of the key areas where tremendous efforts have been made during package development and qualification. However, traditional thermal cycling tests with periodic ATE testing cannot effectively detect the bump failures, instead, the bump joint failures are often first observed in field applications. The purpose of the research is to evaluate the effectiveness of power cycling by the detection of bump failures in the field, moreover, to develop a model which can be applied to estimate the field failures.

In addition, the influence of the underfill properties and bump materials are studied too. The failure data from power cycling testing demonstrates that a constant failure rate for bump failures can be obtained due to the variation of the power cycling peak temperature variations. Thermal profiles are critical for any conclusions drawn from power cycling studies.

The study results presented in this chapter show

1. Power cycling can detect intermittent failures much earlier than any traditional approach. Intermittent failures are often real failures shown in the field applications.

2. Underfill materials will dramatically influence the fatigue life of solder bumps. The study shows low Tg underfill materials will lose the protection on the bumps when the operating temperature is over the Tg. Although high Tg underfill materials can protect the bumps better at elevated temperatures, they will, however, change the failure mechanisms, but with a much longer fatigue life. High Tg underfill materials will also introduce low-k or ultra low-k dielectric cracking.

3. Eutectic solder alloys demonstrate a much better fatigue performance than high lead solder alloys under power cycling conditions, even with low Tg underfill materials.

4. The acceleration factors estimated based on failure data of FCBGAII and FCBGA I packages are very similar. The model for larger packages provided a conservative AF value. The effects of underfill materials and bump materials on the AF are not clear since not enough data has been collected. However, the AF models could not correlate well with the field data, especially when CPF% is high.

One advantage for power cycling tests is that the test itself simulated the field applications. In field applications or power cycling tests, each system can experience different temperature ranges and peak temperatures, and so the failure distribution might

not show up as an obvious worn out failure mechanism, instead closing to a constant failure rate with the shape parameter in a Weibull distribution close to 1. In thermal cycling tests of solder bumps, there will always be a uniform temperature profile and the failures are always worn-out failure rates.

8. CONTRIBUTIONS AND FUTURE WORK

8.1 Contributions of the dissertation

The focuses of the dissertation are to study the end-of-life models and constant failure rate modeling for semiconductor packages using knowledge-based testing methodologies. To start the dissertation, the key failure mechanisms and the failure models associated with those failure mechanisms are introduced and reviewed, then followed by research works in the end-of-life AF models and constant failure rate modeling for the packages. Additionally, the reliability studies are carried out for flip chip solder bumps under power cycling conditions in order to model the failures and correlate with the field failures.

8.1.1 End-of-life AF models for the prediction of solder joint reliability

Historically, the reliability prediction of solder joints is based on Coffin-Manson or its modifications, such as Norris-Landzberg model. However, there is no indication of how accurate the prediction will be. The dissertation studies the AF models widely used and develop an application matrix based on extensive experimental data. The research demonstrates that:

(1) End-of-life AF models for leaded and lead free solder joints are different. The AF values for SAC405 lead free solder joints are normally much larger than that of eutectic solder joints.

(2) End-of-life AF models for the solder joint reliability prediction are not universal, as typically assumed. AF models will be affected by many factors, including package types, and materials used.

(3) If necessary, in order to provide accurate reliability predictions, the AF model parameters should be characterized for packages interested, using at one conditions. Traditional model parameters, e.g. those used in Norris-Landzberg model can be misleading at times.

(4) Similar package structures and materials set can share the same end-of-life models based on the study.

Based on the research work on the end-of-life reliability models in the research, the following assessment matrix/flow chart is recommended. If the product have different with the materials and structures used, then additional test should be done.
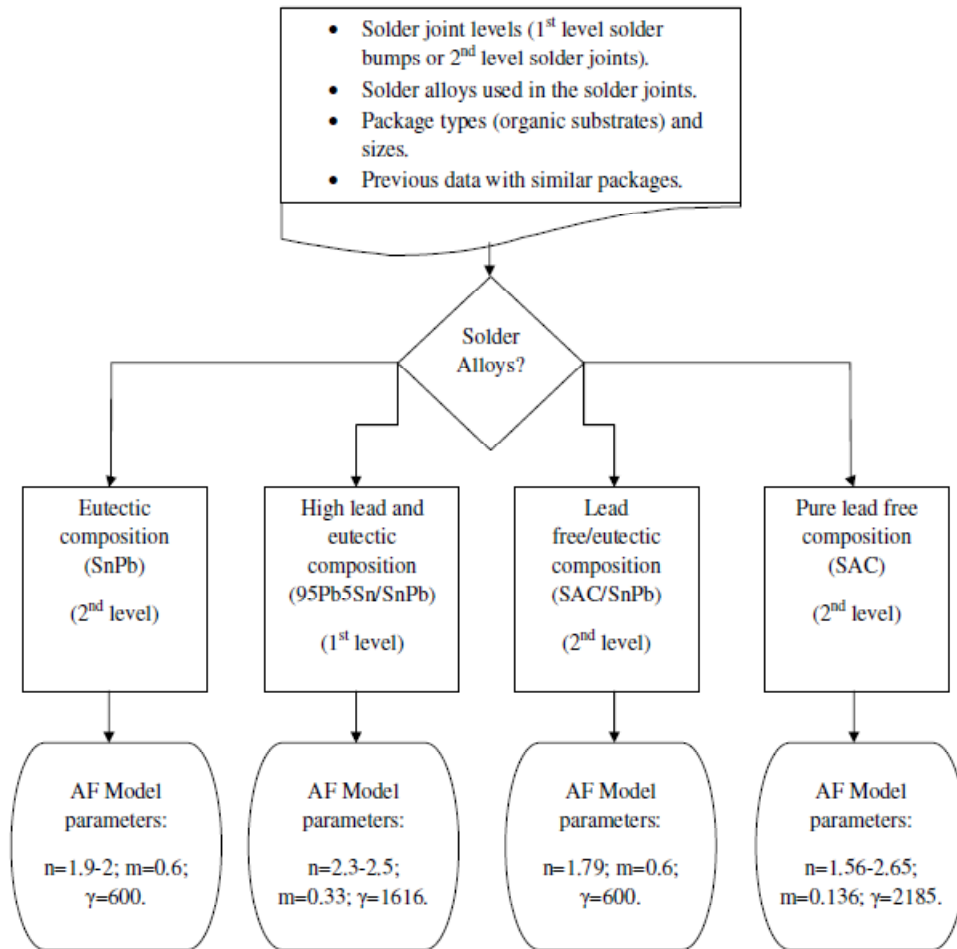
Figure 8-1 End-of-life AF model determination for semiconductor packages

8.1.2 Constant failure rate modeling for semiconductor packages using knowledge-based test-to--failure approach

In reality, the field failures often demonstrate very different failure trends comparing to the end-of-life failures. In order to predict the reliability and failure rate in field applications, failure data is required to be collected during the stress testing in order to understand the failure trends for expected failure mechanisms. The dissertation

studied the failure rate models using knowledge-based test-to-failure approach instead of traditional test–to-pass approaches. The contribution of the research work can be listed below

(1) The estimation of the failure bounds used in failure rate models is studied and a new formula is proposed and validated. The popular estimation of bounds based on the Chi-square distribution is found to be flawed, especially when the number of failure is small. The proposal approach provides easier and tighter bounds than what are used today.

(2) Non-solder joints package failures are following a constant failure rate, instead of end-of-life increasing failure rate. The observation is confirmed through stress testing data and available field failure data. In the field application, even solder bump failures can be analyzed using a constant failure rate approach, which is very different from any research data published under thermal cycling conditions.

8.1.3 Reliability assessment for TEBGA and RCPs using knowledge-based test approaches

Chapter 6 discusses the reliability assessments and failure models for TEBGA packages and RCP packages using knowledge-based test approach. Besides the understanding of the failure mechanisms and the reliability improvements, the focus is put on understanding the failure data trends and failure rate estimation. The studies validated the achievements in this dissertation and will be instructive for future reliability

and failure predictions of semiconductor packages. OEMS and system manufacturers have been pushing for the failure data and then use them to predict the system failures.

8.1.4 End-of-life and Constant failure rate estimation for solder bumps reliability under power cycling conditions

The end-of-life models of solder bumps formed between the die and flip chip substrates is assessed in the dissertation. In addition, the study shows the models based on the end-of-life failure data collected through power cycling conditions did not predict the field failure data well. Moreover, the studies find the variation of the power cycling profiles will demonstrate the expected end-of-life bump failures to follow an approximate constant failure rate, which is not observed in typical thermal cycling conditions. This observation suggests a constant failure rate of bump failures in field applications. The finding is in an agreement with the field failure trends.

In addition, the end-of-life model development study demonstrates that a similar AF model can be used for similar FCBGAs (similar underfill materials and package structures). The model developed for the larger FCBGA packages will provide a more conservative estimation of reliability.

The dissertation studies the impact of underfill materials and bump materials as well. Low Tg underfill materials show a limitation in protecting the bumps and that high Tg underfill materials can achieve the protection of bumps at elevated thermal cycling ranges. However, the change of the Tg of the underfill materials can change the fail-

ure mechanisms from bumps to BGA joints as shown in this study. An optimization shall be done for the combination of underfill materials, the bump types, and dielectric materials in FCBGA packages in order to achieve a robust design and reliability. The study also demonstrates that eutectic solder bump materials show much robust reliability under low-Tg underfill packages compared to the packages which use high lead solder bumps.

8.2 Suggestions for future work

8.2.1 The correlation of constant failure rate estimation and the trends of field failures

In the industry, tremendous testing has been done to evaluate the performance of the packages under defined stress test conditions. However, there is a poor understanding of the correlation between the failure data collected in the stress testing and the field failures. It will be very meaningful if a failure rate model can be developed considering the failures observed during development, the qualification test, manufacturing defects and other results.

8.2.2 End-of-life acceleration factor model development and verification

For empirical AF models, it is not clear how the package structures and materials will influence the acceleration. The current AF models mainly consider the factors associated with thermal cycling profiles or other stress factors. The future work shall focus on the influences of other factors, such as underfill materials, dwell time and peak temperatures.

Appendices

Key Paper Published

❑ Liyu Yang and Joseph Bernstein, "Failure rate estimation of known failure mechanisms of electronic packages," Microelectronics Reliability, Vol. 39, Issue 12, 2009, pp.1563-1572 .

❑ Liyu Yang, Joseph Bernstein, T. Koschmieder, "Assessment of acceleration models used for BGA solder joint reliability studies," Microelectronics Reliability, Vol. 39, issue 12, 2009, pp. 1546-1554.

❑ Shahrzad Salemi, Liyu Yang, Jun Dai, Jin Qin, Joseph B. Bernstein, Physics-of-Failure Based Handbook of Microelectronic Systems, RIAC, 2008.

❑ Liyu Yang and Joseph Bernstein, "Reliability Study of High-Density EBGA Packages Using the Cu Metalized Silicon," IEEE Transactions on Components and Packaging Technology, Vol. 31, No.3, Sep 2008, pp. 702-711.

❑ Liyu Yang, Joseph Bernstein and James Walls, "Predictive Reliability Assessment and Failure Rate Models for Electronic Packages," 40th IMAPS Symposium, San Jose, 2007.

Bibliography

25-GS0003, Procedure for Failure Mechanism Based Certifications of New Package Technologies, Intel, 2000.

25-GS0906, Assembly/Package Certification Methodology Governing Specification, Intel, 2000.

25-GS3000, Intel Product Qualification Specification, Intel, 2000.

Abernethy, R. B., the New Weibull Handbook, 2nd Edition, 1996.

Adeyemi, O., "Confidence Bounds on Failure Probability Estimates," JPL Deep Space Network Progress Report 42-46, pp. 155-167.

Ahmad, S. S., Blish, R. C., Corbett, T., et al, "Effect of Bromine in Molding Compounds on Gold-Aluminum Bonds," IEEE Trans. on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-9, N0.4, Dec. 1986, pp. 379-385.

Ahn, E. C., Cho, T.J., Shim, J.B., Moon, H.J., et al, "Reliability of Flip Chip BGA Package on Organic Substrate," IEEE Electronic Components and Technology Conference, 2000, pp. 1215-1220.

Aihara, T., Ito, S., Sasajima, H. and Oota, K., "Development of Reliability and Moldability on Fine Pitch Ball Grid Array by Optimizing Materials," Trans. of the ASME Journal of Electronic Packaging, Vol. 123, Mar. 2001, pp. 88-94.

Akay, H.U., Liu, Y. and Rassaian, M., "Simplification of Finite Element Models for Thermal Fatigue Life Prediction of PBGA Packages," Trans. of the ASME Journal of Electronic Packages, Sep. 2003, Vol. 125, pp. 347-353.

Alpem, P. and Lee, K. C., "A Simple Model for the Mode II Popcorn Effect in Thin Plastic IC," IEEE 41st Annual International Reliability Physics Symposium, Dallas, Texas, 2003, pp. 452-457.

Amagai, M., Seno, H. and Ebe, K., "Cracking Failures in Lead-on-Chip Packages Induced by Chip Backside Contamination," IEEE Trans. on Components, Packaging, and Manufacturing Technology- Part B, Vol. 18, No.1, Feb. 1995, pp. 119-126.

Amagai, M., "The Effect of Polymer Die Attach Material on Solder Joint Reliability," EEP-Vol 25, 1998 Workshop on Mechanical Reliability of Polymer Materials and Plastic Packages of IC Devices, ASME 1998, pp. 223-230.

Amagai, M., "Chip Scale Package Solder Joint Reliability and Modeling," Microelectronics Reliability, Vol. 39, 1999, pp. 463-477.

Aoki, Y., Tsujie, I. and Nagai, T., "The Effect of Ramp Rate on Temperature Cycle Fatigue in Solder Joints," ESPEC Technology Report No. 25, 2007, pp. 4-13.

Aoki, Y., Tsujie, I. and Nagai, T., "The Effect of Ramp Rate on Thermal Fatigue Testing of Solder Joints," ESPEC Technology Report No. 27, 2009, pp. 1-13.

Arulvanan, P. and Zhong, Z. W., "Assembly and Reliability of PBGA Packages on FR-4 PCBs with SnAgCu Solder," Microelectronic Engineering, Vol. 83, 2005, pp. 2462-2468.

ASE Ltd., Internal Report: EBGA assembly flow and qualification report, 2005.

Bailey, R., "Estimation from Zero-Failure Data," Risk Analysis, Vol. 17, N0.3, 1997, pp. 375-380.

Balkan, H., "Flip Chip Electromigration: Impact of Test Conditions in Product Life Predictions," IEEE ECTC, 2004, pp. 983-987.

Barnard, G. A., "An Analogue of Tchebycheff's Inequality in Terms of Range," Technometrics, Vol. 4, No.1, Feb. 1962, pp. 133-134.

Barney, M. M., and Morris, J. W., "Observation of Microstructural Coarsening in Micro Flip-Chip Solder Joints," Journal of Electronic Materials, Vol. 30, No.9, 2001, pp. 1088-1092.

Bartlett, M. S., "Approximate Confidence Intervals: III. A Bias Correction," Biometrika, Vol. 42, No. 1-2, Jun. 1955, pp. 201-204.

Basaran, C., Ye, H., Hopkins, D. C., Frear, D. and Lin, J. K., "Failure Modes of Flip Chip Solder Joints under High Electric Current Density," Trans. of the ASME Journal of Electronic Packaging, Vol. 127, Jun. 2005, pp. 157-163.

Benoit, J. T., Chin, S., Jain, R. and McCluskey, P., "Wire Bond Metallurgy for High Temperature Electronics," IEEE, 1998, pp. 109-113.

Bailey, C., "Modeling the Effect of Temperature on Product Reliability," IEEE SEMI-THERM Symposium, 2003, pp. 324-331.

Barrett, J. J., Hayes, T. F., Mathuna, R.S. C., "Reliability Evaluation of High Pin Count Hermetic Ceramic IC Packages for Space Applications," IEEE Trans. on Components, Hybrids and Manufacturing Technology, Vol. 15, No.6, Dec. 1992, pp. 1093-1104.

Bartlett, M.S., "Approximate Confidence Intervals: III. A Bias Correction," Biometrika, Vol. 42, No. 1-2, Jun. 1955, pp. 201-204.

Bernstein, J., Gurfinkel, M., Li, X., Walters, J., Shapira, Y., Talmor, M., "Electronic Circuit Reliability Modeling," Microelectronics Reliability, Vol. 46, Issue 12, Dec. 2006, pp. 1957-1979.

Bernstein, J. B., Tutorial: Physics based product qualification, IRPS, 2007.

Birzer, C., Stoeckl, S., Schuetz, G. and Fink, M., "Reliability Investigations of Lead-less QFN Packages until End-of-life with Application-Specific Board-Level Stress Tests," IEEE ECTC, 2006, San Diego, pp. 594-600.

Blish, R. C. and Vaney, P. R., "Failure Rate Model for Thin Film Cracking in Plastic ICs," IEEE/IRPS Proceedings, 1991, pp. 22-29.

Blish, R.C., "Temperature Cycling and Thermal Shock Failure Rate Modeling," IEEE IRPS Proceedings, 1997, PP. 110.

Blish, R. and Durrant,P., "Semiconductor Device Reliability Failure Models," Technology Transfer # 00053955A-XFR, SEMATECH, May 31, 2000.

Bojta, P., Nemeth, P., Harsanyi, G., "Searching for Appropriate Humidity Accelerated Migration Reliability Test Methods," Microelectronics Reliability, Vol.42, 2002, pp.1213-1218.

Braun, T., Becker, K. F., Koch, M., Bader, V., Aschenbrenner, R., Reichl, H., "High-Temperature Reliability of Flip Chip Assemblies," Microelectronics Reliability, Vol. 46, pp. 144-154.

Braunovic, M. and Alexandrov, N., "Intermetallic Compounds at Aluminum-to-Copper Electrical Interfaces: Effects of Temperature and Electric Current," IEEE

Trans. on Components, Packaging, and Manufacturing Technology, Part A, Vol. 17, No.1, March 1994, pp. 78-85.

Brown, B. and Hollander, M., Statistics: A Biomedical Introduction, 1977.

Brunk, H.D., An Introduction to Mathematical Statistics, Blaisdell Publishing Company, 1965.

Burnette, T., Johnson, Z., Koschmieder, T. and Oyler, W., "Underfilled BGAs for a Variety of Plastic BGA Package Types and the Impact on Board-Level Reliability," Freescale internal report, 2004.

Carulli, J. M. and Anderson, T. J., "The Impact of Multiple Failure Modes on Estimating Product Field Reliability," IEEE Design and Test of Computers, 2006, pp. 118-126.

Cassanelli, G., Mura, G., Cesaretti, F., Vanzi, M. and Fantini, F., "Reliability Predictions in Electronic Industrial Applications," Microelectronics Reliability, Vol. 45, 2005, pp. 1321-1326.

Cavasin, D., Anani, M., Rittman, G. and Casto, J., "Board Level Characterization of Pb-free Sn-3.5Ag Versus Eutectic Pb-Sn BGA Solder Joint Reliability," IEEE ECTC, 2007, pp. 129-135.

Chang, H. S., Hsieh, K. C., Martens, T. and Yang, A., "Wire-Bond Void Formation During High Temperature Aging," IEEE Trans. on Component and Packaging Technologies, Vol. 27, No.1, Mar. 2004, pp. 155-160.

Chan, Y. C., Alam, M. O., Hung, K. C., Lu, H. and Bailey, C., "Effect of Underfill Entrapment on the Reliability of Flip Chip Solder Joint," Trans. of the ASME Journal of Electronic Packaging, Vol. 126, Dec. 2004, pp. 541-545.

Chen, B. L., Shi, X. Q., Li, G. Y., Ang, K. H. and Pickering, J. P., "Rapid Temperature Cycling Methodology for Reliability Assessment of Solder Interconnection in Tape Ball Grid Array Assembly," Trans. of the ASME Journal of Electronic Packaging, Vol. 127, Dec. 2005, pp. 466-473.

Chen, C. K., Cheah, S. L., et al, "Failure Mechanism of Smaller Substrate Bond Pad Size in Flip Chip Technology," IEEE Proceedings of 11th IPFA, 2004, Taiwan, pp. 235-238.

Chen, H. Y. and Chen, C., "Interfacial Reaction between Eutectic SnPb Solder and Electroplated Ni as well as Electroless-Ni Metallization During Reflow," Journal of Electronic Materials, Vol. 38, No.2, 2009, pp. 338-344.

Chen, K. M., Jiang, D. S., Kao, N. H. and Lai, J. Y., "Effects of Underfill Materials on the Reliability of Low-K Flip Chip Packaging," Microelectronics Reliability, Vol. 46, 2006, pp. 155-163.

Chen, W., McCloskey, P., Rohan, J. F., Byrne, P. and McNally, P. J., "Preparation and Temperature Cycling Reliability of Electroless Ni (P) Under Bump Metallization," IEEE Trans on Components and Packaging Technologies, Vol. 30, No.1, Mar. 2007, pp. 144-151.

Chen, Y. S, et al., "Solder Joint Reliability Assessment for Flip Chip Ball Grid Array Components with Various Designs in Lead Free Solder Materials and Solder Mask Dimensions," Journal of Electronic Materials, Vol. 36, No.1, 2007, pp. 6-16.

Chen, Y. T and Mencinger, N., Intel Statistical and Reliability Courses: Reliability Statistics, Jul. 2000.

Choi, W. J., Yeh, E. C. C. and Tu, K. N., "Mean-Time-to-Failure Study of Flip Chip Solder Joints on Cu/Ni(V)/Al Thin Film Under Bump Metallization," Journal of Applied Physics, Vol. 94, No. 9, pp. 5665-5671.

Chou, K. Y., Chen, M. J., et.al., "Die Cracking Evaluation and Improvement in ULSI Plastic Packages," Proceedings IEEE 2001 Int. Conference on Microelectronics Test Structure, Vol. 14, March 2001, pp. 239-244.

Chilamakuri, S. and Gupta, B. K., "Failure-in-time Estimates Reliability Life of Passive Devices," Laser Focus World, Jul. 2002,

http://www.laserfocusworld.com/display_articl/147848/62/none/none/Feat/-Failure-in-time-estimates-reliability-life-of-passive-device.

Choubey, A., Osterman, M. and Pecht, M., "Microstructure and Intermetallic Formation in SnAgCu BGA Components Attached with SnPb Solder Under Isothermal Aging," IEEE Trans. on Device and Materials Reliability, Vol. 8, No.1, Mar. 2008, pp. 160-167.

Chung, C. L., Fun, J., Huang, M. L. and Tsai, F. J., "Study on Failure Mechanism of PCT Reliability for BT Substrate Based CSP (Chip Scale Packages)," Trans. of the ASME, Vol. 124, Dec. 2002, pp. 334-339.

Chung, C. C., Yang, T. F., and Juang, J. Y., et al., "Influence of Underfill Materials on the Reliability of Coreless Flip Chip Package," Microelectronics Reliability, Vol. 48, 2008, pp. 1875-1881.

Ciappa, M., Carbognani, F., Cova, P. and Fichtner, W., "Lifetime Prediction and Design of Reliability Tests for High-Power Devices in Automotive Applications", 41st Annual International Reliability Physics Symposium, Dallas, 2003, pp. 523-528.

Cooper, M. S., "Investigation of Arrhenius Acceleration Factor for Integrated Circuit Early Life Failure Region with Several Failure Mechanisms," IEEE Trans. on Components and Packaging Technologies, 2004, pp. 1-3.

Condra, Lloyd, O'Rear, S., Freeman, T., Flancia, L., Pecht, M. and Barker, D., "Comparison of Plastic and Hermetic Microcircuits Under Temperature Cycling and Temperature Humidity Bias," IEEE Trans. on Components, Hybrids and Manufacturing Technology, Vol. 15, N0.5, Oct. 1992, pp. 640-650.

Cory, A. R., "Improved Reliability Prediction Through Reduced –Stress Temperature Cycling," IEEE 38th Annual International Reliability Physics Symposium, San Jose, California, 2000, pp. 231-236.

Cui, H., "Accelerated Temperature Cycle Test and Coffin-Manson Model for Electronic Packaging," IEEE RAMS, 2005, pp. 556-560.

Cushing, M. J., "Another Perspective on the Temperature Dependence of Microelectronic-Device Reliability," Proceedings Annual Reliability and Maintainability Symposium, 1993, pp. 333-337.

Danielson, D., Marcyk, G., Babb, E. and Kudva, S., "HAST Applications: Acceleration Factors and Results for VLSI Components," IEEE/IRPS Proceeding, 1989, pp. 114-121.

Dauksher, W., "A Second-Level SAC Solder Joint Fatigue Life Prediction Methodology," IEEE Transaction on Device and Materials Reliability, Vol. 8, No.1, Mar. 2008, pp. 168-173.

Davis, J. A., Bozack, M. J., and Evans, J. L., "Effect of (Au, Ni)Sn$_4$ Evolution on Sn-37Pb/ENIG Solder Joint Reliability Under Isothermal and Temperature-Cycled Conditions," IEEE Trans. on Components and Packaging Technologies, Vol. 30, No.1, Mar. 2007, pp. 32-41.

Davuluri, P., Shetty, S., Dasgupta, A. and Young, S., "Thermomechanical Durability of High I/O BGA Packages," Trans. of the ASME Journal of Electronic Packaging, Vol. 124, Sep. 2002, pp. 266-270.

DeBusk, B. M., "Managing the Reliability of COTS-based Military Systems," 1998 Proceedings Annual Reliability and Maintainability Symposium, pp. 394-399.

Dias, R., Lucero, A., Niemeyer, S. and Myers, S., "Failure Mechanisms in C4 Organic Packages," Intel Q&R Conference, 1997, pp. 57-68.

Ding, M., Wang, G., Chao, B. and Ho, P. S., Su, P., Uehling, T. and Wontor, D., "A Study of Electromigration Failure in Pb-free Solder Joints", IEEE 43th Annual IRPS Proceeding, San Jose, 2005, pp. 518-523.

Doorselaer, K. V. and Zeeuw, K. D., "Relation Between Delamination and Temperature Cycling Induced Failures in Plastic Packaged Devices," IEEE Trans. on Compo-

nents, Hybrids and Manufacturing Technology, Vol. 13, No.4, Dec. 1990, pp. 879-882.

Driel, W. D. V., Gils, M. A. J. V., Silfhout, R. B. R. V., Zhang, G. Q., "Prediction of Delamination Related IC and Packaging Reliability Problems," Microelectronics Reliability, Vol. 45, 2005, pp. 1633-1638.

Dudek, R., Doring, R. and Michel, B., "Reliability Prediction of Area Array Solder Joints," Journal of Electronic Packaging, Trans. of ASME, Vol. 125, Dec. 2003, pp. 562-568.

Dunn, C. F. and McPherson, J. W., "Temperature Cycling Acceleration Factors for Aluminum Metallization Failure in VLSI Applications," 28th Annual Proc. of the Intl. Rel. Phys. Symp., 1990, pp. 252-258.

Ebeling, C. E., an Introduction to Reliability and Maintainability Engineering, McGraw-Hill International Editions, Singapore, 1997.

Ebersberger, B. and Lee, C., "Cu Pillar Bump as a Lead-Free Drop-in Replacement for Solder –Bumped Flip Chip Interconnects," IEEE ECTC, 2008, pp. 59-66.

Emerson, J. A., Peterson, D. W., Sweet, J. N., "HAST Evaluation of Organic Liquid IC Encapsulant Using Sandia's Assembly Test Chips," IEEE IRPS Proceeding, 1992, pp. 951-956.

Emerson, J., Sweet, J. N. and Peterson, D. W., "Evaluating Plastic Assembly Processes for High Reliability Applications Using HAST and Assembly Test Chips," IEEE IRPS Proceeding, 1994, pp. 191-195.

Epstein, B., "Estimation from Life Test Data," Technometrics, Vol. 2, No.4, Nov. 1960, pp. 447-454.

Ersland, P., Jen, H. R. and Yang, X. , "Lifetime Acceleration Model for HAST Tests of a pHEMT Process," Microelectronics Reliability, Vol. 44, 2004, pp. 1039-1045.

Fan, X. J., Raiser, G. and Vasudevan, V. S., "Effects of Dwell Time and Ramp Rate on Lead-Free Solder Joints in FCBGA Packages," IEEE Electronic Components and Technology Conference, 2005, pp. 901-906.

Ferguson, T. and Qu, J., "Effect of Moisture on the Interfacial Adhesion of the Underfill/Solder Mask Interface," ASME Journal of Electronic Packaging, Vol. 124, Jun. 2002, pp. 106-110.

Filippi, R. G., McGraph, J. F., Shaw, T. M. et al, "Thermal Cycle Reliability of Stacked Via Structures with Copper Metallization and an Organic Low-k Dielectric," 42nd IEEE Annual International Reliability Physics Symposium, Phoenix, 2004, pp. 61-67.

Foucher, B., Tomas, J., Mounsi, F., Jeremias, M., "Life Margin Assessment with Physics of Failure Tools Application to BGA Packages," Microelectronics Reliability, Vol. 46, 2006, pp.1013-1018.

Frear, D., Morgan, H., Burchett, S. and Lau, J., The Mechanics of Solder Alloy Interconnects, Van Nostrand Reinhold, New York, 1994.

Freund, J. E., Livermore, P. E. and Miller, I., Manual of Experimental Statistics, Prentice-Hall, 1960.

Freescale Semiconductor Inc., Internal report: Qualification study report of 35 mm x 35 mm FCBGAs, 2008.

Freescale Semiconductor Inc., Solder Joint Reliability Study of 179-ball LGA Packages, Internal Report, 2004.

Gain, A. K., Chan, Y.C., Sharif, A. and Yung, W. K. C., "Effect of Small Sn-3.5Ag-0.5Cu Addition on The Structure and Properties of Sn-9Zn Solder in Ball Grid Array Packages," Microelectronic Engineering (2009),doi:10.1016/J.mee.2009.04.015.

Gajewski, D., Internal Report: Electromigration Study of Cu Bumps in RF Modules, 2006.

Ganesan, S., Pecht, M., and Ling, S., "Use of High Temperature Operating Life Data to Mitigate Risks in Long-duration Space Applications That Deploy Commercial-Grade Plastic Encapsulated Semiconductor Devices," Microelectronics Reliability, Vol. 46, 2006, pp. 360-366.

Gektin, V., Bar-Cohen, A. and Ames, J., "Coffin-Manson Fatigue Model of Under-filled Flip-chips," IEEE Trans. on Components, Packaging, and Manufacturing-Part A, Vol. 20, No.3, September 1997, pp. 317-326.

Gestel, R. V., Zeeuw, K. D., Gemert, L. and Bagerman, E., "Comparison of Delamination Effects Between Temperature Cycling Test and Highly Accelerated Stress Test in Plastic Packaged Devices," IEEE/IRPS Proceeding, 1992, pp. 177-181.

Ghaffarian, R., "Impact of CSP Assembly Underfill on Reliability," APEX, 2001, Session P-AD2/3, pp. 1-7.

Ghaffarian, R., "Accelerated Thermal Cycling and Failure Mechanisms for BGA and CSP Assemblies," Trans. of the ASME Journal of Electronic Packaging, Vol. 122, Dec. 2002, pp. 335-340.

Giacomo, G. D., Reliability of Electronic Packages and Semiconductor Devices, the McGraw Hill Companies, 1997.

Goroll, M., Pufall, R., Kanert, W., Plikat, B., "Semiconductor in High Temperature Applications-A Future Trend in Automotive Industry," Microelectronics Reliability, Vol. 44, 2004, pp. 1413-1417.

Graves, S., Bisgaard, S., et.al., "Accelerated Testing of on-Board Diagnostics," Quality and Reliability Engineering International, 2009, Vol. 23, pp. 189-201.

Gracia, A. G., Woirgard, E. and Zardini, C., "Correlation between Experimental Results and FE Simulations to Evaluate Lead-Free BGA Assembly Reliability," Microelectronics Reliability, Vol. 45, 2005, pp. 1652-1657.

Gunn, J. E., Malik, S. K., "Highly Accelerated Temperature and Humidity Stress Test Techniques," IEEE/IRPS Proceeding, 1981, pp. 48-51.

Guterman, H. E., "An Upper Bound for the Sample Standard Deviation," Technometrics, Vol. 4, No.1, Feb. 1962, pp. 134-135.

Ha, S. S., et al., "Electromigration Behavior in Sn-37Pb and Sn-3.0Ag-0.5Cu Flip Chip Solder Joints under High Current Density," Journal of Electronic Materials, Vol. 38, No. 1, 2009, pp. 70-77.

Hagge, J. K., "Mechanical Considerations for Reliable Interfaces in Next Generation Electronics Packaging," Proc. IEEE Nat'l Aerospace and Electronics Conference-NEPCON, 1989, pp. 2021-2026.

Hahn, G. J. and Meeker, W. Q., "Statistical Intervals: A Guide for Practitioners," A Wiley-Interscience Publication, John Wiley & Sons, 1991.

Hall, P. M., "Creep and Stress Relaxation in Solder Joints," Solder Joint Reliability, Theory and Applications, Ed. J. H Lau, 1991, pp. 306-332.

Hallberg, O., "Recent Humidity Accelerations, A Base for Testing Standards," Quality and Reliability Engineering International, Vol. 7, pp. 169-180, 1991.

Hartfield, C. D., et al., "Interface Reliability Assessments for Copper low k Products," IEEE Trans. On Device and Materials Reliability, Vol. 4, No.2, Jun. 2004, pp. 129-141.

Halford, G. R., et al., "Temperature Effects on the Strain Range Partitioning Approach for Creep Fatigue Analysis," Fatigue at Elevated Temperatures, Philadelphia, ASTM, 1972, pp. 658-669.

Han, H., Sohn, Y.C. and Yu, J., "Interfacial Reactions between Cu_xNi_y Alloy Under Bump Metallurgy and $Sn-Ag-_z$ Cu Solders," Journal of Electronic Materials, Vol. 36, No. 5, 2007, pp. 578-586.

Han, J. B., "Flip Chip BGA Design to Avert Die Cracking," Trans. of the ASME Journal of Electronic Packaging, Vol. 123, Mar. 2001, pp. 58-63.

Harry, C. C. and Mathiowetz, C. H., "ASIC Reliability and Qualification: A User's Perspective," Proceedings of the IEEE, Vol. 81, N0.5, May 1993, pp. 759-767.

Harvey, I. R., Turner, D., Ortowski, J. and Herbert, C., "Optimization Case Study of CSP Temperature Cycle and Board Bending Reliability," IPC SMEMA Council APEX, 2001, RE1-3, PP. 1-8.

Heleine, T. L., Murcko, R. M., Wang, S. C., "A Wire Bond Reliability Model," IEEE /IRPS Proceeding, 1991, pp. 378-381.

Hillman, D., Wells, M., Cho, K., "The Impact of Reflowing a Pb-free Solder Alloy Using a Tin/Lead Solder Alloy Reflow Profile on Solder Joint Integrity," Rockwell Collins Internal Report, 2008.

Ho, P. S., Wang, G., Ding, M., Zhao, J. H and Dai, X., "Reliability Issues for Flip Chip Packages," Microelectronics Reliability, Vol. 44, 2004, pp. 719-737.

Hong, C., "Thin Film Cracking/Delamination Evaluation Using Assembly Test Chip," WLR Final Report, 1992, pp. 163-166.

Howard, R. T., "Packaging Reliability-How to Define and Measure It," IEEE Trans. on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-5, No.4, Dec. 1982, pp. 454-462.

Hu, K. X., Yeh, C. P., Doot, B., Skiper, A. F. and Wyatt, K. W., "Die Cracking in Flip Chip-on-Board Assembly," IEEE Proceeding, 1995, pp. 293-299.

Huang, M. L., et al., "Morphology and Growth Kinetics of Intermetallic Compounds in Solid-State Interfacial Reaction of Electroless Ni-P with Sn-Based Lead Free Solders," Journal of Electronic Materials, Vol. 35, No. 1, 2006, pp. 181-188.

Hund, T. D. and Plunkett, P. V., "Improving Thermosonic Gold Ball Bond Reliability," IEEE Trans. on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-8, No.4, Dec. 1985, pp. 446-456.

Intel, Knowledge Based Reliability Evaluation of New Package Technologies Utilizing Use Conditions, March 1999.

Jang, G. Y., et.al., "Mechanism of Interfacial Reaction for the Sn-Pb Solder Bump with Ni/Cu Under-Bump Metallization in flip chip Technology," Journal of Electronic Materials, Vol. 33, No.10, 2004, pp. 1118-1129.

Jang, G. Y. and Duh, J. G., "The Effect of Intermetallic Compound Morthology on Cu Diffusion in Sn-Ag and Sn-Pb Solder Bump on the Ni/Cu under Bump Metallization," Journal of Electronic Materials, Vol. 34, No.1, 2005, pp. 68-79.

Jang, G. Y., et al., "Influence of Cu Content on Compound Formation near the Chip Side for the Flip Chip Sn-3.0Ag-(0.5 or 1.5) Cu Solder Bump During Aging," Journal of Electronic Materials, Vol. 35, No. 9, 2006, pp. 1745-1754.

Jang, J.W., Lin, J. K. and Frear, D.R., "Fatigue Morphology after the Drop Impact Test of the Ball Grid Array Package with Lead-Free Sn3.8Ag0.7Cu and Ni under Bump Metallization," Journal of Electronic Materials, Vol. 36, N0.3, 2007, pp. 207-213.

Jen, M. H. R., Liu, L. C. and Lai, Y.S., "Electromigration on Void Formation of Sn3Ag1.5Cu FCBGA Solder Joints," Microelectronics Reliability, Vol.49, 2009, pp. 734-745.

Jeng, S. T., Chang, H. H., Lai, Y. S. and Tsai, T. Y., "High Strain Rate Compression Behavior for Sn-37Pb Eutectic Alloy, Lead Free Sn-1Ag-0.5Cu and Sn-3Ag-0.5Cu Alloys," Microelectronics Reliability, Vol. 49, 2009, pp. 310-317.

JESD74, Early Life Failure Rate Calculation Procedure for Electronic Components, April 2000.

JEDEC Standard, JESD91A, Method for Developing Acceleration Models for Electronic Component Failure Mechanisms, August 2003.

JEDEC Standards, JESD94 Application Specific Qualification Using Knowledge Based Test Methodology, January 2004.

JEDEC Standards, JESD47D, Stress-Test-Driven Qualification of Integrated Circuits, JEDEC Standards, November, 2004.

Jen, M. H. R., Liu, L. C. and Wu, J., "Flip Chip Ball Grid Array Lead-Free Solder Joint Under Reliability Test," Trans. of the ASME Journal of Electronic Packaging, Vol. 127, Dec. 2005, pp. 446-451.

Jeon, Y. D., Paik, K. W, Ostmann, A. and Reichl, H., "Effects of Cu Contents in Pb-free Solder Alloys on Interfacial Reactions and Bump Reliability of Pb-free Solder Bumps on Electroless Ni-P Under-Bump Metallurgy," Journal of Electronic Materials, Vol. 34, No.1, 2005, pp. 80-90.

Jeon, Y. D, Lee, Y. B. and Choi, Y. S, "Thin Electroless Cu/OSP on Electroless Ni as a Novel Surface Finish for Flip Chip Solder Joints," IEEE ECTC, 2006, San Diego, pp. 119-124.

JEP122C, Failure Mechanisms and Models for Semiconductor Devices, JEDEC Publication, March 2006.

JEP 148, Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment, JEDEC Publications, April 2004.

JEP 150, Stress-Test-Driven Qualification and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components, JEDEC Publication, May 2005.

Johnson, M. E., Lu, H. Y., et al., "Using High Speed Shear and Cold Ball Pull to Characterize Lead Free Solder Alloys and Predict Board Level Drop Test Performance", IEEE ECTC, 2007, pp. 536-542.

Jones, J. and Hayes, J., "Estimation of System Reliability Using a "Non-Constant Failure Rate" Model," IEEE Trans. on Reliability, Vol. 50, No.3, Sep. 2001, pp. 286-288.

Joyce, W. B. and Anthony, P. J., "Failure Rate of a Cold –or Hot – Spared Component with a Lognormal Lifetime," IEEE Trans. on Reliability, Vol. 37, No.3, 1988 August, pp. 299-307.

Ju, T. H., Lin, W., Lee, Y. C. and Liu, J. J., "Effects of Ceramic Ball Grid Array Package's Manufacturing Variations on Solder Joint Reliability," Proc. 3rd Int. Conf. Multichip Modules, 1994, Vol. 2256, pp. 514-519.

Khan, M., Fatemi, H., Romero, J. and Delenia, E., "Effect of High Thermal Stability Mold Material on the Gold-Aluminum Bond Reliability in Epoxy Encapsulated VLSI Devices," IEEE/IRPS Proceeding, 1988, pp. 40-49.

Kim, D. G., Kim, J. W. and Jung, S. B., "Reliability Evaluations of Flip Chip package under Thermal Shock Test," Microelectronic Engineering, Vol. 82, 2005, pp. 575-580.

Kim, H. J., Lee, J. Y., Paik, K. W., et al., "Effects of Cu/Al Intermetallic Compound (IMC) on Copper Wire and Aluminum Pad Bondability," IEEE Trans. on Components and Packaging Technologies, Vol. 26, No.2, Jun. 2003, pp. 367-374.

Kim, H., Zhang, M., Kumar, C. M., et al., " Improved Drop Reliability Performance with Lead Free Solders of Low Ag Content and Their Failure Modes," IEEE ECTC 2007, pp. 962-967.

Kim, I. and Lee, S. B., "Fatigue Life Evaluation of Lead-Free Solder under Thermal and Mechanical Loads," IEEE ECTC, 2007, pp. 95-104.

Kim, J. W., Kim, D. G., Hong, W. S., Jung, S. B., "Evaluating of Solder Joint Reliability in Flip Chip Packages During Accelerated Testing," Journal of Electronic Materails, Vol. 34, No. 12, 2005, pp. 1550-1557.

Kim, J. W., Kim, D. G., Lee, Y. C. and Jung, S. B. , "Analysis of Failure Mechanism in Anisotropic Conductive and Non-Conductive Film Interconnections," IEEE Trans. on Components and Packaging Technologies, Vol. 31, No.1, Mar. 2008, pp. 65-.

Kirschman, R. K., Sokolowski, W. M. and Kolawa, E. A., "Die Attachment for – 120 $^{\circ}$C to +20 $^{\circ}$C Thermal Cycling of Microelectronics for Future Mars Rovers-An Overview," Trans. of the ASME Journal of Electronic Packaging, Vol. 123, Jun. 2001, pp. 105-111.

Kitagawa, H., Maeda, T., Murata, S., Maki, T., et al., "Plastic Packaging Stress Induced Failures in TiW/Al-Si Metal to Silicide Contacts," IEEE/IRPS, 1988, pp. 71-75.

Koh, J. H. and Kim, T. G., "Reliability of Pb (Mg, Nb) O3-Pb (Zr, Ti) O3 Multilayer Ceramic Piezoelectric Actuators by Weibull Method," Microelectronics Reliability, Vol. 46, 2006, pp. 183-188.

Kotlowicz, R. W., "Comparative Compliance of Representative Lead Designs for Surface Mounted Components," 39th Annual Proc. Electronic Components Conference, 1989, pp. 791-831.

Kripesh, V., Zhang, X., Khan, N., Rotaru, M. and Chong, C. T., "Design and Development of a Large Die and Fine Pitch Wafer Level Package for Mobile Applications," IEEE ECTC, 2006, San Diego, pp. 570-576.

Kuan, W. C., Liang, S. W. and Chen, C., "Effect of Bump Size on Current Density and Temperature Distributions in Flip Chip Solder Joints," Microelectronics Reliability, Vol. 49, 2009, pp. 544-550.

Kwon, Y. M. and Paik, K. W., "Electromigration of Pb-free Solder Flip Chip Using Electroless Ni-P/Au UBM," IEEE ECTC, 2007, pp. 1472-1477.

Kwon, W. S., Kim, H. J., Paik, K. W., Jang, S. Y. and Hong, S. M., "Mechanical Reliability and Bump Degradation of ACF Flip Chip Packages Using BCB Bumping Dielectrics Under Temperature Cycling," Trans. of the ASME Journal of Electronic Packaging, Vol. 126, Jun. 2004, pp. 202-207.

Kwon, W.S., et al., "Thermal Cycling Reliability and Delamination of Anisotropic Conductive Adhesives Flip Chip on Organic Substrate with Emphasis on the Thermal Deformation," ASME Trans. of Journal of Electronic Packaging, Vol. 127, Jun. 2005, pp. 86-90.

Lai, Y. S. and Chiu, Y. T., "Failure Mechanism of Sn-Ag-Cu Flip Chip Solder Joints with Different Cu Weight Contents Under Comparatively Low Current Stressing," IEEE ECTC, 2007, pp. 1462-1466.

Lakshminarayanan, V., "Environmental-Stress Screening Improves Electronic-Design Reliability," EDN, Sep. 20, 2001, pp. 73-84.

Lall, P., "Tutorial: Temperature as an Input to Microelectronics-Reliability Models," IEEE Trans. on Reliability, Vol. 45, No.1, Mar. 1996, pp. 3-9.

Moura, E. C., "A Method to Estimate the Acceleration Factor for Subassemblies," IEEE, 1992, pp. 396-399.

Lall, P., Panchagade, D., Iyengar, D., "High Speed Digital Image Correlation for Transient-Shock Reliability of Electronics," IEEE ECTC, 2007, pp. 924-939.

Lau, J. and Dauksher, W., "Reliability of a 1657 CCGA Package with 95.5Sn3.9Ag0.6Cu Lead-free Solder Paste on PCBs," Trans. of the ASME Journal of Electronic Packaging, Vol. 127, Jun. 2005, pp. 96-105.

Lee, C. C., Liu, H. C. and Chiang, K. N., "3-D Structure Design and Reliability Analysis of Wafer Level Package with Stress Buffer Mechanism," IEEE Trans on Components and Packaging Technologies, Vol. 30, No.1, Mar. 2007, pp. 110-118.

Lee, C. C., Tran, T. A., Yuan, Y., et al., "Challenges in Temperature Cycling Test for Electronic Packages Containing Low-k/Cu Silicon," IEEE ECTC, 2007, pp. 1186-1192.

Lee, J.-H., Lee, Y.-D., Park, Y.-B., Yang, S.-T., Suh, M.-S., et al., "Joule Heating Effect on the Electromigration Lifetime and Failure Mechanisms of Sn-3.5Ag Solder Bump," IEEE ECTC, 2007, pp. 1436-1441.

Lewis, E. E., Introduction to Reliability Engineering, second edition, John Wiley & Sons, Inc., 1996.

Li, C. Y., et al., "Damage Integral Methodology for Thermal and Mechanical Fatigue of Solder Joints," Solder Joint Reliability, Theory and Applications, ed. John H Lau, 1991, pp. 261-288.

Li, D., Liu, C. and Conway, P., "Microstructure and Shear Strength Evolution of Sn-Ag-Cu Solder Bumps during Aging at Different Temperatures," Journal of Electronic Materials, Vol. 35, No.3, 2006, pp. 388-398.

Li, J., Karppinen, J., Laurila, T. and Kivilahti, J. K., "Reliability of Lead-Free Solder Interconnections in Thermal and Power Cycling Tests," IEEE Trans. on Components and Packaging Technologies, Vol. 32, No. 2 Jun. 2009, pp. 302-308.

Li, L., Xie, J., Ahmad, M. and Brillhart, M., "Environmental Effects on Dielectric Films in Plastic Encapsulated Silicon Devices," IEEE ECTC, 2007, pp. 755-760.

Lin, K. L. and Lin, G.-P., "The Electromigration Investigation on the Newly Developed Pb-Free Sn-Zn-Ag-Al-Ga Solder Ball Interconnect," IEEE ECTC, 2007, pp. 1467-1471.

Lin, T. Y., Xiong, Z. P., Yao, Y. F., Tok, L., Yu, Z. Y., Njoman, B., Hua, K. H. and Lin, Y. C., Duh, J. G. and Chiou, B. S., "Wettability of Electroplated Ni-P in Under Bump Metallurgy with Sn-Ag-Cu Solder," Journal of Electronic Materials, Vol. 35, No.1, 2006, pp. 7-14.

Lin, Y. T., Peng, C.T., and Chiang, K. N., "Parametric Design and Reliability Analysis of Wire Interconnect Technology Wafer Level Packaging," ASME Journal of Electronic Packaging, Vol. 124, Sep. 2002, pp. 234-239.

Lin, Y., Liu, W., Guo, Y. and Shi, F. G., "Reliability Issues of Low-Cost Overmolded Flip Chip Packages," IEEE Trans. on Advanced Packaging, Vol. 28, No.1, Feb 2005, pp. 79-88.

Liu, J., Gao, L., Xie, M., et.al., "A General Weibull Model for Reliability Analysis Under Different Failure Criteria-Application on Anisotropic Conductive Adhesive Joining Technology," IEEE Trans. on Electronics Packaging Manufacturing, Vol. 28, No.4, Oct. 2005, pp. 322-327.

Liu, X., Sooklal, V. K., Verges, M. A., Larson, M. C., "Experimental Study and Life Prediction on High Cycle Vibration Fatigue in BGA Packages," Microelectronics Reliability, Vol. 46, 2006, pp. 1128-1138.

Liu, X. W. and Plumbridge, W. J., "Damage Produced in Solder Alloys during Thermal Cycling," Journal of Electronic Materials, Vol. 36, No. 9, 2007, pp. 1111-1120.

Lou, H., Qu, X., Chen, Z., Wang, J., "Lifetime Assessment of Solder Joints of BGA Package in Board Level Drop Test," IEEE 6th International Conference on Electronic Packaging Technology, 2005, pp. --.

Ma, H., Suhling, J. C., et. al., "The Influence of Elevated Temperature Aging on Reliability of Lead Free Solder Joints," IEEE ECTC, 2007, pp. 653-668.

Ma, Y. Y., "Failure Analysis of Full Delamination on the Stacked Die Leaded Packages," Trans. of the ASME Journal of Electronic Packaging, Vol. 125, Sep. 2003, pp. 392-399.

Mathew, R., Hasan, A., Yang, L., Chen, C.-T., Tran, H. and Abhyankar, R., "IXE 7000 Ethernet Switch Package Development," 55th IEEE Electronic Components & Technology Conference, May 2005 , Orlando, pp. 1-8.

Mattila, T. T., Kaloinen, E., Syed, A. and Kivilahti, J. K., "Reliability of SnAgCu Interconnects with Minor Additions of Ni or Bi under Mechanical Shock loading at Different Temperatures," IEEE ECTC, 2007, pp. 381-390.

McCluskey, F. P. , Hakim, E. B., Fink, J., Fowler, A., and Pecht, M., "Reliability Assessment of Electronic Components Exposed to Long-Term Non-Operating Conditions," IEEE Trans. on Components, Packaging and Manufacturing Technology-Part A, Vol. 21, No.2, Jun. 1998, pp. 352-359.

McGarvey, W. J., "Autoclave vs. 85c/85%RH Testing- A Comparison," IEEE , 1979, pp. 136-142.

McMahon, T. J. and Jorgensen, G. J., "Progress Toward a CdTe Cell Life Prediction," CP462, NCPV Photovoltacies Program Review, The American Institute of Physics, 1999, pp. 54-61.

Memis, I., "Testing to Eliminate Reliability Defects from Electronic Packages," 43rd Annual International Reliability Physics Symposium, San Jose, 2005, pp. 462-465.

Merrett, R. P., Bryant, J. P. and Studd, R., "An Appraisal of High Temperature Humidity Stress Tests for Assessing Plastic Encapsulated Semiconductor Components," IEEE IRPS Proceeding, 1983, pp. 73-82.

Monlevade, E. F. D. and Peng, W., "Failure Mechanisms and Crack Propagation Paths in Thermally Aged Pb-Free Solder Interconnects," Journal of Electronic Materials, Vol. 36, No. 7, 2007, pp. 783-797.

Moore, D. S. and McCabe, G. P., Introduction to the Practice of Statistics, fourth edition, W. H. Freeman and Company, New York, 1996.

Moreau, S., Lequeu, T. and Jerisian, R., "Comparative Study of Thermal Cycling and Thermal Shock Tests on Electronic Component Reliability," Microelectronics Reliability, Vol. 44, 2004, pp. 1343-1347.

Nah, J.-W., Chen, K., Suh, J. O. and Tu, K. N., "Electromigration Study in Flip Chip Solder Joints," IEEE ECTC, 2007, pp. 1450-1455.

Nelson, W., Accelerated Testing-Statistical Models, Test Plans, and Analyses, Wiley Series in Probability and Mathematical Statistics, New York, 1990.

Nguyen, H. V., Salm, C., Vroemen, J., Voets, Krabbenborg, J., B., et al., "Test Chip for Detecting Thin Film Cracking Induced by Fast Temperature Cycling and Electromigration in Multilevel Interconnect Systems," Proceedings of 9th IPFA, Singapore, 2002, pp. 135-139.

Nir, N., Dudderar, T. D., Wong, C. C. and Storm, A. R., "Fatigue Properties of Microelectronics Solder Joints," Trans. of the ASME Journal of Electronic Packaging, Vol. 113, Jun. 1991, pp. 92-101.

Nishikawa, H., Piao, J. Y. and Takemoto, T., "Interfacial Reaction between Sn-0.7Cu (Ni) Solder and Cu Substrate," Journal of Electronic Materials, Vol. 35, No.5, 2006, pp. 1127-1132.

Noctor, D. M., Bader, F. E., Viera, A. P., Boysan, P., Golwalkar, S., and Foehringer, R., "Attachment Reliability Evaluation and Failure Analysis of Thin Small Outline Packages (TSOP's) with Alloy 42 Lead frames," IEEE Trans. on Components, Hybrids and Manufacturing Technology, Vol. 16, No.8, Dec. 1993, pp. 961-971.

Norris, K. C. and Landzberg, A. H., "Reliability of Controlled Collapse Interconnections," IBM J. R & D Vol. 13, 1969, pp. 266-271.

Ohring, M., Reliability and Failure of Electronic Materials and Devices, Academic Press, 1998.

Oldervoll, F. and Strisland, F., "Wire Bond Failure Mechanisms in Plastic Encapsulated Microcircuits and Ceramic Hybrids at High Temperatures," Microelectronics Reliability, Vol. 44, 2004, pp. 1009-1015.

Omi, S., Fujita, K., Tsuda, T., and Maeda, T., "Causes of Cracks in SMD and Type Specific Remedies," IEEE Trans. on Components, Hybrids and Manufacturing Technology, Vol. 14, No.4, Dec. 1991, pp. 818-823.

Orain, S., Fuchsmann, A., Fiori, V. and Federapiel, X., "Reliability Issues in Cu/low-k Structures Regarding the Initiation of Stress –Voiding or Crack Failures," Microelectronic Engineering, Vol. 83, 2006, pp. 2402-2406.

Osenbach, J. W., Evanosky, T. L., Chand, N., Comizzoli, R. B. and Krautter, H. W., "Temperature-Humidity-Bias Behavior and Acceleration Factors for Nonhermetic Uncooled InP-Based Lasers," Journal of Light Wave Technology, Vol. 15, No.5, May 1997, pp. 861-873.

Pan, N., et. al., "An Acceleration Model for Sn-Ag-Cu Solder Joint Reliability Under Various Thermal Cycle Conditions," SMTA International, 2005, pp. 876-883.

Papoulis, A. , Probability, random variables and Stochastic Processes, McGraw-Hill Book Company, Second Edition, 1984.

Papoulis, A. , Probability & Statistics, Prentice Hall, 1990.

Pandher, R. S., Lewis, B. G., Vangavcti, R., Singh, B., "Drop Chock Reliability of Lead-Free Alloys-Effect of Micro-Additives," IEEE ECTC, 2007, pp. 669-676.

Park, J., Kim, B.-S., Cha, H.-J., Jo, Y.-B., Shin, S.-C., et.al., "Interfacial Degradation Mechanism of Au-Al Bonding in Quad Flat Package," IEEE 42nd Annual International Reliability Physics Symposium, Phoenix, 2004, pp. 569-570.

Park, S., Dhakal, R., Lehman, L. and Cotts, E. J., "Grain Deformation and Strain In Board Level SnAgCu Solder Interconnects Under Deep Thermal Cycling," IEEE Trans. on Components and Packaging Technologies, Vol. 30, No.1, Mar. 2007, pp. 178-185.

Park, S., Shah, C., Kwak, J., Jang, C., et al., "Transient Dynamic Simulation and Full Field Test/Validation for a Slim-PCB of Mobile Phone under Drop/Impact," IEEE ECTC, 2007, pp. 914-922.

Parker, T. P. and Webb, C. W., "A Study of Failures Identified during Board Level Environmental Stress Testing," IEEE Trans. on Components, Hybrids, and Manufacturing Technology, Vol. 15, No.6, Dec. 1992, pp. 1086-1092.

Partel, J. K., "Confidence Intervals Using Censored Data," Technometrics, Vol. 18, No.2, May 1976, pp. 221-225.

Pearson, E. S., Hartley, H. O., eds., Biometrica Tables for Statisticians, Vol.1, Cambridge: Cambridge University Press, 1970.

Pecht, M., Dasgupta, A. and Barker, D., "The Reliability Physics Approach to Failure Prediction Modeling," Quality and Reliability Engineering International, Vol.6, 1990, pp. 267-273.

Pecht, M. and Dasgupta, A., "Physics of Failure: An Approach to Reliable Product Development," IEEE IRW Final Report, 1995, pp. 1-4.

Pecht, M., Nguyen, L. T., Hakim, E. B., Plastic Encapsulated Microelectronics, John and Wiley & Sons, 1995.

Peck, D. S., "Comprehensive Model for Humidity Testing Correlation", 1986 IEEE IRPS, pp. 44-50.

Peddada, S. R. and Blish, R. C., "Modeling of Down Bond Failure Rates in 196 Lead MM Packages," Intel Q&R Conference, 1993, pp. 61-71.

M. Pei, Fan, X. and Bhatti, P. K., "Field Condition Reliability Assessment for SnPb and SnAgCu Solder Joints in Power Cycling Including Mini Cycles," IEEE Electronic Components and Technology Conference, 2006, pp. 899-905.

Prismark, Workshop of Advanced Packaging, July, 2004.

Prismark, Workshop of Flip Chip and Low-k Update and Challenges, Winter, 2006.

Prismark, Workshop on Flip Chip packages and CSP packages, June 2007.

Prismark, Workshop of Advanced Packages Trend and Challenges, June and July, 2008.

Pucha, R. V., Tunga, K., Pyland, J. and Sitaraman, S. K., "Accelerated Thermal Cycling Guidelines for Electronic Packages in Military Avionics Thermal Environment," Trans. of the ASME Journal of Electronic Packaging, Vol. 126, Jun. 2004, pp. 256-264.

Qi, Y., et. al., "Accelerated Thermal Fatigue of Lead-Free Solder Joints as a Function of Reflow Cooling Rate," Journal of Electronic Materials, Vol. 33, No. 12, 2004, pp. 1497-1506.

Qin, J., Huang, B., Walter, J., Bernstein, J. B., and Talmor, M., "Reliability Analysis of Avionics in the Commercial Aerospace Industry," The Journal of the RAC, First quarter, 2005, pp. 1-5.

Raghunathan, R. and Sitaraman, S. K., "Qualification Guidelines for Automotive Packaging Devices," Inter Society Conference on Thermal Phenomena, 2000, pp. 385-389.

Ramanathan, L., Yu, T. Lee, T., Jang, J.-W., Chae, S.-H. and Ho, P. S., "Current Carrying Capacity of Sn0.7Cu Solder Bumps in Flip Chip Modules for High Power Applications," IEEE ECTC, 2007, pp. 1456-1461.

Ray, S., Kiyono, S., Waite, K. and Nicholls, L., "Qualification of Low-k 90 nm Technology Die with Pb-free Bumps on a Build-up Laminate Package (PBGA) with Pb-free Assembly Processes," IEEE ECTC, 2006, San Diego, pp. 139-144.

Roesch, W. J. and Jittinorasett, S., "Cycling Copper Flip Chip Interconnects," Micro-electronics Reliability, Vol.44, 2004, pp. 1047-1054.

Romeu, J. L., "Statistical Analysis of Reliability Data, Part 2: on Estimation and Testing," The Journal of the Reliability Analysis Center, Third Quarter, 2001, pp. 4-9.

Ryu, D. and Chang, S., "Novel Concepts for Reliability Technology," Microelectronics Reliability 45, 2006, pp. 611-622.

Sadegh, P., Thompson, A., Luo, X., et. al., "A Methodology for Predicting Service Life and Design of Reliability Experiments," IEEE Trans. on Reliability, Vol. 55, No.1, Mar. 2006, pp. 75-85.

Sahai, H. and Khurshid, A., "Confidence Intervals for the Mean of a Poisson distribution: a Review," Biom. J. 35, 1993, 7, pp. 857-867.

Saitoh, T. and Toya, M., "Numerical Stress Analysis of Resin Cracking in LSI Plastic Package under Temperature Cyclic Loading-Part II: Using Alloy 42 as Lead-Frame

Material," IEEE Trans. on Components, Packaging, and Manufacturing Technology-Part B, Vol. 20, No.2, May 1997, pp. 176-183.

Saitoh, T., Matsuyama, H. and Toya, M., "Delamination and Encapsulant Resin Cracking in LSI Plastic Packages Subjected to Temperature Cycling," Trans. of the ASME Journal of Electronic Packaging, Vol. 125, Sep. 2003, pp. 420-425.

Salemi, S. and Bernstein, J. B., Reliability Prediction for Electronic Devices- the Paradigm Formation – Three phases in Electronic System Prediction, 2006.

Salemi, S., Yang, L., Dai, J., Qin, J. and Bernstein, J., Physics of Failure Based Handbook of Microelectronic Systems, RIAC, 2008.

Salmela, O., "Comments on the IPC Surface Mount Attachment Reliability Guidelines," Quality and Reliability Engineering International, Vo. 21, 2005, pp. 345-354.

Salmela, O., "Acceleration Factors for Lead-Free Solder Materials," IEEE Trans. On Components and Packaging Technologies, Vol. 30, No.4, Dec. 2007, pp. 700-707.

Sematech International, Knowledge based Reliability Qualification Testing of Silicon Devices, Technology Transfer # 00053958A-XFR, May 31 2000.

Scalise, J., "Plastic Encapsulated Microcircuits (PEM) Qualification Testing," IEEE ECTC, 1996, pp. 392-397.

Scharr, T. A., "Fatigue Properties of Base Copper Materials Used in the Fabrication of TAB Leads," 41st Annual Proc. Electronic Comp. and Tech. Conference, 1991, pp. 848-853.

Shao, T. L., Chen, I. H. and Chen, C., "Electromigration Failure Mechanism of Sn96.5Ag3.5 Flip Chip Solder Bumps," IEEE ECTC, 2004, pp. 979-982.

Shen, Y. L., "Analysis of Thermal Stresses in Copper Interconnect/low-k Dielectric Structures," Journal of Electronic Materials, Vol. 34, No. 5, 2005, pp. 497-505.

Shetty, S., Reinikainen, T., "Three and Four Point Bend Testing for Electronic Packages," Trans. of the ASME Journal of Electronic Packaging, Vol. 125, Dec. 2003, pp. 556-561.

Shi, X. Q., Pang, H. L. J. and Zhang, X. R., "Investigation of Long-term Reliability and Failure Mechanism of Solder Interconnects with Multifunctional Micro-Moire Interferometry System," Microelectronics Reliability, Vol. 44, 2004, pp. 841-852.

Sinkovics, B. and Krammer, O., "Board Level Investigation of BGA Solder Joint Deformation Strength," Microelectronics Reliability, Vol. 49, 2009, pp. 573-578.

Shirley, C. G. and Blish, R.C., " Thin-Film Cracking and Wire Ball Shear In Plastic DIPS Due to Temperature and Thermal Shock," IEEE/IRPS Proceeding, 1987, pp. 238-249.

Shirley, C. G. and Hong, C. E. C., "Optimal Acceleration of Cyclic THB Tests for Plastic-Packaged Devices," IEEE/IRPS Proceeding, 1991, pp. 12-21.

Shohji, I., Mori, H. and Orii, Y., "Solder Joint Reliability Evaluation of Chip Scale Package Using a Modified Coffin-Manson Equation," Microelectronics Reliability, Vol. 44, 2004, pp. 269-274.

Snook, I., Marshall, J. M. and Newman, R. M., "Physics of Failure As an Integrated Part of Design for Reliability," Proceedings Annual Reliability and Maintainability Symposium, 2003, pp. 46-54.

Solomon, H. D., "The Solder Joint Fatigue Life Acceleration Factor," Trans. of the ASME Journal of Electronic Packaging, Vol. 113, Jun. 1991, pp. 186-190.

Son, H.-Y., Jung, G.-J., Lee, J.-K., Choi, J.-Y. and Paik, K.-W., "Cu/SnAg Double Bump Flip Chip Assembly as An Alternative of Solder Flip Chip on Organic Substrates for Fine Pitch Applications," IEEE ECTC, 2007, pp. 864-871.

Son, H. Y., Jung, G. J., Park, B. J. and Paik, K. W, "A Study on the Thermal Reliability of Cu/SnAg Double Bump Flip Chip Assemblies on Organic Substrates," Journal of Electronic Materials, Vol. 37, No. 12, 2008, pp. 1832-1842.

START, Reliability Estimations for the Exponential Life, A Publication of the DOD Reliability Analysis Center, Volume 10, No. 7,

http://src.alionscience.com/pdf/R_EXP.pdf.

Stepniak, F., "Conversion of the Under Bump Metallurgy into Intermetallics: the Impact on Flip Chip Reliability," Microelectronic Reliability, Vol. 41, 2001, pp. 735-744.

Stepniak, F., "Failure Criteria of Flip Chip Joints during Accelerated Testing," Microelectronics Reliability, Vol. 42, 2002, pp. 1921-1930.

Stepniak, F., "Mechanical Loading of Flip Chip Joints before Underfill: The Impact on Yield and Reliability," Microelectronics Reliability, Vol.44, 2004, pp. 805-814.

Strifas, N., Vaughan, C. and Ruzzene, M., "Accelerated Reliability-Thermal and Mechanical Fatigue Solder Joints Methodologies," IEEE 40th Annual International Reliability Physics Symposium, Dallas, Texas, 2002, pp. 144-147.

Striny, K. M. and Schelling, A. W., "Reliability Evaluation of Aluminum-Metallized MOS Dynamic RAM's in Plastic Packages in High Humidity and Temperature Environments," IEEE Trans. on Components, Htbrids, and Manufacturing Technology, Vol. CHMT-4, N0.4, Dec. 1981, pp. 476-481.

Suhir, E., "Accelerated Life Testing in Microelectronics and Photonics: Its role, Attributes, Challenges, Pitfalls, and Interaction with Qualification Tests," ASME Trans. of Journal of Electronic Packaging, September 2002, Vol. 124, pp. 281-291.

Suhling, J. C., Gale, H. S., Johnson, R. W., et.al., "Thermal Cycling Reliability of Lead-free Solders for Automotive Applications," IEEE Inter. Society Conference on Thermal Phenomena, 2004, pp. 350-357.

Syndergaard, P. and Young, J. , "A Model of Temperature Cycling Performance in Plastic Encapsulated Packages," IEEE IRW Final Report, 1994, pp. 37-41.

Tan, C.W., Daud, A. R., Yarmo, M. A., "Corrosion Study at Cu-Al Interface in Microelectronics Packaging," Applied Surface Science, Vol. 191, 2002, pp. 67-73.

Tanaka, N., Kitano, M., Kumazawa, T. and Nishimura, A., "Evaluating IC-Package Interface Delamination by Considering Moisture-Induced Molding-Compound Swelling," IEEE Trans. On Component and Packaging Technology, Vol. 22, N0.3, Sep. 1999, pp. 426-432.

Tee, T. Y., Ng, H. S., Lim, C. T., Pek, E. and Zhong, Z., "Impact Life Prediction Modeling of TFBGA Packages Under Board Level Drop Test," Microelectronics Reliability, Vol. 44, 2004, pp. 1131-1142.

Teverovsky, A., "Effect of Environments on Degradation of Molding Compound and Wire Bonds in PEMs," IEEE Electronic Components and Technology Conference, 2006, pp. 1415-1424.

Thomson, G. W., "Bounds for the Ratio of Range to Standard Deviation," Biometrika, Vol. 42, No.1/2, Jun. 1955, pp. 268-269.

Tiplitz, C., "Approximations to the Mean and Standard Deviation of Recreation of Reciprocals of Observations," Technometrics, Vol. 5, No.4, Nov. 1963, pp. 522-524.

Toishiraporn, P., Subbarayan, G., et al., "Predictive Reliability Models Through Validated Correlation Between Power Cycling and Thermal Cycling Accelerated Life Tests," Soldering and Surface Mount Technology, Vol. 14, No.3, 2002, pp. 51-60.

Toishiraporn, P., Crosbie, P., et. al., "Dynamic Crack Propagation Prediction of Solder Joints under Impact Conditions," IEEE ECTC, 2007, pp. 689-694.

Tran, T. A., Yong, L., Williams, B., Chen, S. and Chen, A., "Fine Pitch Probing and Wire Bonding and Reliability of Aluminum Capped Copper Bond Pads," IEEE Electronic Components and Technology Conference, 2000, pp. 1674-1680.

Tsai, M.-Y., Hsu, C. H. J. and Wang, C. T. O., "Investigation of Thermomechanical Behaviors of Flip Chip BGA Packages During Manufacturing Process and Thermal Cycling," IEEE Trans. on Components and Packaging Technologies, Vol. 27, No.3, Sep. 2004, pp. 568-576.

Tsao, P.-H., Huang, C., Lin, A., Li, M.-J., Perng, D. J. and Tsai, N., "Cavity-down Thermal-Enhanced Package Reliability Evaluation for Low-k Dielectric/Cu Intercon-

nects," IEEE Electronic Component and Technology Conference, 2004, pp. 1191-1193.

Tsao, P.-H., Kiang, B., Wu, K., et al., "Low-k Flip Chip Board Level Reliability on 65 nm Technology," IEEE ECTC, 2007, pp. 110-115.

Tseng, A., et al., "BGA Assembly Process Development for 45 nm ELK Devices," International Conference on Electronic Packaging Technology & High Density Packaging, 2008.

Tu, P. L., Chan, Y. C., Lai, J. K. L., "Effect of Intermetallic Compounds on the Thermal Fatigue of Surface Mount Solder Joints," IEEE Trans. on Components, Packaging, and Manufacturing Technology-Part B, Vol. 20, No.1, Feb. 1997, pp. 87-93.

Tummala, R. R., Rymaszewski, E. J. and Klopfenstein, A. G., Microelectronics Packaging Handbook, Second edition, Chapman & Hall, 1996.

Uchida, M., Ito, H., Yabui, K., Nishiuchi, H., et al., "Low-Stress Interconnection for Flip Chip BGA Employing Lead-Free Solder Bump," IEEE ECTC, 2007, pp. 885-891.

Uebbing, J., "Mechanisms of Temperature Cycle Failure in Encapsulated Optoelectronic Devices," IEEE IRPS Proceeding, 1981, pp. 149-156.

Ulm, K., "A Simple Method to Calculate the Confidence Interval of a Standardized Mortality Ratio," American Journal of Epidemiology, 1990, 131(2), pp. 373-375.

Uno, T. and Tatsumi, K., "Thermal Reliability of Gold-Aluminum Bonds Encapsulated in Bi-Phenyl Epoxy Resin," Microelectronics Reliability, Vol. 40, 2002, pp. 145-153.

Ury, H. K. and Wiggins, A. D., "Another Shortcut Method for Calculating the Confidence Interval of a Poisson Variable," Am. J. Epidemiol, 1985, Vol. 122, pp. 197-198.

Vairagar, A. V., Mhaisalkar, S. G. and Krishnamoorthy, A., "Electromigration Behavior of Dual-Damascene Cu Interconnects- Structure, Width, and Length Dependences," Microelectronics Reliability, Vol. 44, 2004, pp. 747-754.

Vandenbroucke, J. P., "A Shortcut method for calculating the 95% confidence interval of the Standardized Mortality Ratio," Am. J. Epidemiol, 1982; Vol. 115, pp. 303-304.

Vasudevan, V. and Fan, X., "An Acceleration Model for Lead Free Solder Joint Reliability under Thermal Cycling," IEEE ECTC, 2008, pp. 139-145.

Vries, J. D., Jansen, M. and Driel, W. V., "Solder Joint Reliability of HVQFN-Packages Subjected to Thermal Cycling," Microelectronics Reliability, Vol. 49, 2009, pp. 331-339.

Wang, H., Zhao, M. and Guo, Q., "Vibration Fatigue Experiments of SMT Solder Joint", Microelectronics Reliability, Vol. 44, 2004, pp. 1143-1156.

Wang, G., Groothuis, S. and Ho, P. S., "Packaging Effect on Reliability for Cu/Low-k Structure," IEEE 42nd Annual International Reliability Physics Symposium, Phoenix, 2004, pp. 557-562.

Wang, G., Ho, P. S., Groothuis, S., "Chip-Packaging Interaction: A Critical Concern for Cu/Low k Packaging," Microelectronics Reliability, Vol. 45 2005, pp. 1079-1093.

Wang, J., Lim, H. K., Lew, H. S., Saw, W. T. and Tan, C. H., "A Testing Method for Assessing Solder Joint Reliability of FCBGA Packages," Microelectronics Reliability, Vol. 44, 2004, pp. 833-840.

Wang, K. Z. and Chen, C. M., "Intermetallic Compound Formation and Morphology Evolution in the 95Pb5Sn flip chip Solder Joint with Ti/Cu/Ni Under Bump Metallization During Reflow Soldering," Journal of Electronic Materials, Vol. 34, No. 12, 2005, pp. 1543-1549.

Wang, S. J., Kao, H. J. and Liu, C. Y., "Correlation between Interfacial Reactions and Mechanical Strengths of SnCu/NiP Solder Bumps," Journal of Electronic Materials, Vol. 33, No. 10, 2004, pp. 1130-1136.

Wang, S. N., Liang, L., et al., "Solder Joint Reliability under Electromigration and Thermal-Mechanical Load," IEEE ECTC, 2007, pp. 1074-1083.

Wang, T. H., et al., "Optimization of Board Level Thermo-mechanical Reliability of High Performance Flip Chip Package Assembly," Microelectronic Engineering, Vol. 85, 2008, pp. 659-664.

Wei, J., Wang, Q., Luo, W., Xiao, G., Chan, P. C. H., "Highly Accelerated Stress Test (HAST) for Low-Cost Flip Chip on Board Technology," IEEE ICEPT, 2003, pp. 386-388.

White, M., Cooper, M., Chen, Y. and Bernstein, J. B., "Impact of Junction Temperature on Microelectronics Device Reliability and Considerations for Space Applications," IEEE IRW Final Report, 2003, pp. 133-136.

Wong, E. H., Seah, S. K. W., and Shim, V. P. W., "A Review of Board Level Solder Joints for Mobile Applications," Microelectronics Reliability, Vol. 48, 2008, pp. 1747-1758.

Wong, S. S. K. , Wong, E. H., Mai, Y. W., Rajoo, R., Lim, C. T., "Failure Mechanisms of Interconnections in Drop Impact," IEEE Electronic Components and Technology Conference, 2006, pp. 1484-1492.

Wong, S. F., Malatkar, P., Rick, C., Kulkarni, V. and Chin, I., "Vibration Testing and Analysis of Ball Grid Array Package Solder Joints," IEEE ECTC, 2007, pp. 373-380.

Wu, J. D., Zheng, P. J., Lee, C. W., Hung, S. C. and Lee, J. J., "A Study in Flip Chip UBM/Bump Reliability With Effects of Sn/Pb Solder Composition," IEEE 41st Annual International Reliability Physics Symposium, Dallas, Texas, 2003, pp. 132-139.

Wu, J. D., Lee, C. W., Zheng, P J., et al., "Electromigration Reliability of $SnAg_xCu_y$ Flip Chip Interconnects," IEEE Electronic Components and Technology Conference, 2004, pp. 961-967.

Wu, J. D., Lee, C. W, Wu, S. Y. and Li, S., "Electromigration Reliability Enhancement of Flip Chip Interconnects Using Cu-Doped SnPb Solder," 42nd Annual International Reliability Physics Symposium, Phoenix, 2004, pp. 565-566.

Wu, J. D., Zheng, P. J., Lee, C. W., Hung, S. C. and Lee, J. J., "A Study in Flip Chip UBM/Bump Reliability With Effects of SnPb Solder Composition," Microelectronics Reliability, Vol. 46, 2006, pp. 41-52.

Wu, W., Held, M., Jacob, P., Scacco, P., and Birolini, A., "Investigation on the Long Term Reliability of Power Modules," Proceedings of 1995 International on Power Semiconductor Devices & ICs, 1995, pp. 443-448.

Xiong, Z., Osenbach, J. W., Chua, K. H., "Eutectic SnPb Solder Bump Cracking Issue of Large –die Flip Chip Ball Grid Array (FCBGA) Package with Electroless Ni/Immersion Au (ENIG) Build-up Substrate," IEEE Electronics Packaging Technology Conference, 2006, pp. 196-202.

Wu, Y., Zhang, J., Wu, F., et al., "Effects of UBM on Electromigration in Pb-free Solder Joints," IEEE ECTC, 2004, pp. 998-1002.

Yang, L., and Walls, J., Customer Field Failure Data Analysis for Future Product and Technology Reliability Improvement, Freescale Semiconductor Internal Report, 2007.

Yang, L., Bernstein, J. B., and Chung, K., "The Impact of Lead-free Soldering on Electronics Packages," Microelectronics International, Vol. 18, No.3, 2001, pp. 20-26.

Yang, L. , Bernstein, J. B., and Leong, K.C., "Effect of the Plasma Cleaning Process on Plastic Ball Grid Array Package Assembly Reliability," IEEE Trans. on Electronics Packaging Manufacturing, Vol. 25, Issue 2, Apr. 2002, pp. 91-99.

Yang, L. and Bernstein, J. B., "Encapsulation Process Development for Flexible-Circuit Based Chip Scale Packages," IEEE Trans. on Electronic Packaging Manufacturing, Vol. 25, No.4, Oct. 2002, Pp. 344-354.

Yang, L. , King, C. K., Bernstein, J. B., "Liquid dispensing encapsulation in semiconductor packaging," Microelectronics International, Vol. 20, Issue 3, Dec. 2003, pp. 29-35.

Yang, L. , King, C. and Doe, R., "Qualification of an Enhanced Ball Grid Array Package using Build-up Layers on a Metal Heat Spreader," 54rd IEEE ECTC, Las Vegas, Jun. 2004, pp. 1187-1190.

Yang, L. , King, C., Peng, R., and Gelvin, E., "Reliability Improvement Study of a Build-up Wire Bonding EBGA Package Using 8-layer 0.13 um Copper Silicon Technology," IEEE ECTC, 2006, pp. 1893-1898.

Yang, L. , Bernstein, J. B., and Walls, J., "Physics Based Predictive Reliability Study for Electronic Packages," WA5-1, 40th IMAPS Symposium, 2007, San Jose, CA.

Yang, L. and Bernstein, J. B., "Reliability Study of EBGA Packages," IEEE Trans. on Components and Packaging Technology-Part A, Vol.31, No.3, Sep. 2008, pp.702-711 .

Yang, L., Bernstein, J. B., "Failure rate estimation of known failure mechanisms of electronic packages," Microelectronics Reliability, Available online, 22 July 2009.

Yang, L., Bernstein, J. B., Koschmieder, T. , "Assessment of acceleration models used for BGA solder joint reliability studies," Microelectronics Reliability, Available online, 1 September 2009.

Yoon, J.-W., Moon, W.-C. and Jung, S.-B., "Interfacial Reaction of ENIG/Sn-Ag-Cu/ENIG Sandwich Solder Joint during Isothermal Aging," Microelectronic Engineering, Vol. 83, 2006, pp. 2329-2334.

Yoon, J. W., Kim, S. W. and Jung, S. B., "IMC Morphology, Interfacial Reaction and Joint Reliability of Pb-free Sn-Ag-Cu Solder on Electrolytic Ni BGA Substrate," Journal of Alloys and Compounds, Vol. 392, 2005, pp. 247-252.

Yoon, S. W., et al., "Under Bump Metallurgy Study on Copper Low-k Dielectrics for Fine Pitch Flip Chip Packaging," Journal of Electronic Materials, Vol. 33, No. 10, 2004, pp. 1144-1155.

Yu, C. H., et al., "Influence of Interfacial Reaction Layer on Reliability of Chi- Scale Package Joint from Using Sn-37Pb and Sn-8Zn-3Bi Solder," Journal of Electronic Materials, Vol. 34, No.2, 2005, pp. 161-167.

Yu, H., Vuorinen, V. and Kivilahti, J. K., "Solder Substrate Interfacial Reactions in the Sn-Cu-Ni Interconnection System," Journal of Electronic Materials, Vol. 36, No. 2, 2007, pp. 136-146.

Yu, Q. and Shiratori, M., "Fatigue-Strength Prediction of Microelectronics Solder Joints under Thermal Cycling Loading," IEEE Trans on Components, Packaging and Manufacturing Technology, Part A, Vol. 20, No.3, Sep. 1997.

Yeoh, A., Chang, M., Pelto, C., Huang, T.-L., Balakrishnan, S., "Copper Die Bumps and Low-k Dielectrics in 65 nm High Volume Manufacturing," IEEE Electronic Components and Technology Conference, 2006, pp. 1611-1615.

Yoon, S. W., Witarsa, D., Lim, S. Y. L., et al., "Reliability Studies of a Through Via Silicon Stacked Module for 3D Microsystem Packaging," IEEE Electronic Components and Technology Conference, 2006, pp. 1449-145.

Zakaria, M. and Kassim, Z., "Reducing Burn-in Time Through High-Voltage Stress test and Weibull Statistical Analysis," IEEE Design and test of Computers, March-April 2006, pp. 88-98.

Zelenka, R. L., "A Reliability Model for Interlayer Dielectric Cracking During Temperature Cycling," 29th Annual Proc. of the Intl. Rel. Phys. Symp., 1991, pp. 30-34.

Zeng, K., Stierman, R., Chiu, T. C., Edwards, D., Ano, K. and Tu, K. N., "Kirkendall Void Formation in Eutectic SnPb Solder Joints on Bare Cu and its Effect on Joint Reliability," Journal of Applied Physics, Vol. 97 024508, 2005, pp. 1-8.

Zhai, C. J., Sidharth, A. and Blish, R. , "Board Level Solder Reliability Vs. Ramp Rate & Dwell Time During Temperature Cycling," IEEE 41st Annual International Reliability Physics Symposium, Dalls, Texas, 2003., pp. 447-451.

Zhai, C. J. , Ozkan, U., Sidharth, A., Blish, R. and Master, R. N., "Investigation of Cu/Low-k Film Delamination in Flip Chip Packages," IEEE ECTC, 2006, San Diego, pp. 709-717.

Zhai, C. J. , Too, S. S. and Master, R. N., "Reliability Modeling of Lidded Flip Chip Packages," IEEE Electronic Components and Technology Conference, 2007, pp. 1091-1096.

Zhang, B., Ding, H. and Sheng, X., "Reliability Study of Board Level Lead Free Interconnects under Sequential Thermal Cycling and Drop Impact," Microelectronics Reliability, Vol. 49, 2009, pp. 530-536.

Zhao, X. J., Caers, J.F.J.M, Vries, J. W. C. D., Wong, E. H. and Rajoo, R., "A Component Level Test Method for Evaluating the Resistance of Pb-free BGA Solder Joints to Brittle Fracture under Shock Impact," IEEE ECTC, 2007, pp. 1522-1529.

Zhao, S. and Pang, X., "Investigation of Delamination Control in Plastic Package," Microelectronic Reliability, vol. 49, 2009, pp. 350-356.

Zhu, X., Baumann, R., Pilch, C., Zhou, J., Jones, J. and Cirba, C., "Comparison of Product Failure Rate to The Component Soft Error Rates in A Multi-Core Digital Signal Processor," 43rd IEEE Annual International Reliability Physics Symposium, San Jose, 2005, pp. 209-214.

Sahai, H. and Khurshid, A., "Confidence Intervals for the Mean of a Poisson Distribution: a Review," Biom. J. 35, 1993, 7, pp. 857-867.