ABSTRACT

Title of Document: LOW POWER SMARTDUST RECEIVER WITH NOVEL APPLICATIONS AND IMPROVEMENTS OF AN RF POWER HARVESTING CIRCUIT.

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Smartdust is the evolution of wireless sensor networks to cubic centimeter dimensions or less. Smartdust systems have advantages in cost, flexibility, and rapid deployment that make them ideal for many military, medical, and industrial applications. This work addresses the limitations of prior works of research to provide sufficient lifetime and performance for Smartdust sensor networks through the design, fabrication and testing of a novel low power receiver for use in a Smartdust transceiver. Through the novel optimization of a multi-stage LNA design and novel application of a power matched Villard voltage doubler circuit, a 1.0 V, 1.6 mW low power On-Off Key (OOK) receiver operating at 2.2 GHz is fabricated using 0.13 um CMOS technology. To facilitate data transfer in adverse RF propagation environments ($1/r^3$ loss), the chip receives a 1 Mbps data signal with a sensitivity of -90 dBm while consuming just 1.6 nJ/bit. The receiver operates without the addition

of any external passives facilitating its application in Smartdust scale (cm^3) wireless sensor networks. This represents an order of magnitude decrease in power consumption over receiver designs of comparable sensitivity.

In an effort to further extend the lifetime of the Smartdust transceiver, RF power harvesting is explored as a power source. The small scale of Smartdust sensor networks poses unique challenges in the design of RF power scavenging systems. To meet these challenges, novel design improvements to an RF power scavenging circuit integrated directly onto CMOS are presented. These improvements include a reduction in the threshold voltage of diode connected MOSFET and sources of circuit parasitics that are unique to integrated circuits. Utilizing these improvements, the voltage necessary to drive Smartdust circuitry (1 V) with a greater than 20% RF to DC conversion efficiency was generated from RF energy levels measured in the environment (66 uW). This represents better than double the RF to DC conversion efficiency of the conventional power matched RF energy harvesting circuit. The circuit is integrated directly onto a 130 nm CMOS process with no external passives and measures only 300 um by 600 um, meeting the strict form factor requirement of Smartdust systems.

LOW POWER SMARTDUST RECEIVER WITH NOVEL APPLICATIONS AND IMPROVEMENTS OF AN RF POWER HARVESTING CIRCUIT.

By

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Dedication

This thesis would be incomplete without a mention of the support given to me by my wife, Toni, to whom this thesis is dedicated. More than once, obstacles appearing too great to overcome challenged my resolve. Without her unwavering love and support, I doubt this thesis would ever have been completed.

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Chapter 1: Literature Survey

Introduction

A topic of intense interest in radio frequency (RF) wireless research is that of wireless sensor networks. Wireless sensor networks are characterized by the ad-hoc distribution of many tiny sensor devices in an area. These devices are capable of sensing data, performing data processing, and wireless transmission to other sensor nodes. When distributed in a random fashion in an area, these sensor nodes organize themselves into a network capable of routing data back to a central access point.

Unlike existing wireless networks, wireless sensor networks have minimal bit rate requirements. These requirements are typically on the order of bits per day [1]. Because these networks often must operate in areas without pre-existing infrastructure, they are typically required to operate for extended periods of time on a single battery charge. Thus, low power design and techniques for extracting energy from the environment are important technologies for wireless sensor networks.

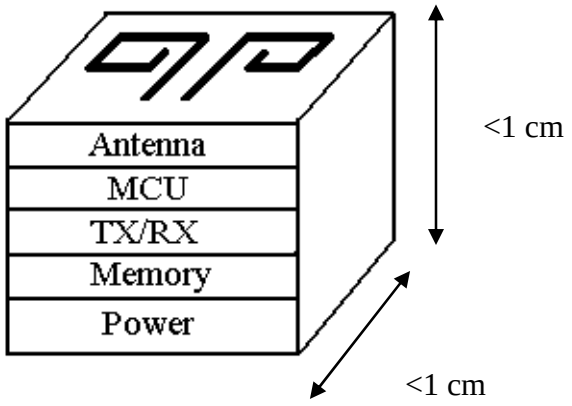


Fig. 1 Smartdust sensor node.

Smartdust systems are the evolution of wireless sensor networks to cubic centimeter dimensions or less (Fig. 1). Such small scale integration of the various subcomponents (transceiver, microcontroller, memory, etc.) poses unique challenges in the design of Smartdust systems. One of the most difficult challenges in the implementation of Smartdust systems is the difficulty in realizing long term operation given the limited availability for on-system energy storage.

This work seeks to help resolve this issue in two ways; first through the development of a low power receiver design compatible with the form factor of Smartdust systems; and second through the novel improvement of RF energy scavenging circuitry to extend the operational lifetime of Smartdust sensor nodes. Towards this goal, this work first assess the availability of RF energy in the environment, then identifies the performance limitations of RF energy scavenging, and lastly, through various means, improves and applies RF energy scavenging technology to enhance the performance of Smartdust sensor networks.

The first aspect of this work, summarized in Chapter 2 is a comprehensive survey of the RF energy present in the environment due to the cellular and ultra-high frequency (UHF) TV infrastructure. The goal is to characterize the availability of RF energy in the environment that can be scavenged to recharge the battery of a Smartdust sensor node.

Chapter 3 summarizes the development of an analytical model by which the performance of the power matched Villard voltage doubler circuit as an RF energy scavenger can be examined. The model is applied as a tool to study the effect of various parasitic sources on scavenging performance. Subsequently, a determination is made of the dominant parasitic losses under different operational conditions. Furthermore, this model has the novel ability to enable swift optimization of a multi-stage power matched Villard voltage doubler over multiple design parameters including transistor width and number of stacked stages.

Novel modifications to the power matched Villard voltage doubler are presented in Chapter 4 to reduce the performance degradation of the parasitics that were identified in Chapter 3. Techniques to reduce the body effect, threshold voltage losses, and parasitic input losses are examined. These design improvements enable the fabrication of an RF energy scavenging circuit that is more than twice as efficient as the conventional RF power harvesting circuit. This represents sufficient RF scavenging performance to recharge the battery of a Smartdust sensor node by

beaming power from an RF source or even from scavenging RF energy levels detected in the environment as reported in the survey presented in Chapter 2.

The last topic of this work presents a novel receiver design that implements the power matched Villard voltage doubler as a non-coherent demodulator to realize an ultra low power on-off key receiver compatible with the cubic centimeter form factor of Smartdust systems. Furthermore, to meet the link range requirements of Smartdust sensor nodes, a novel methodology is presented for optimizing a multi-stage low noise amplifier (LNA) to achieve a desired sensitivity at the minimum possible power consumption. This work culminates in the fabrication and verification of a low power receiver requiring an order of magnitude less power per bit than receivers of comparable sensitivity.

The contributions to the field of wireless sensor networks include:

- (Chapter 2) RF energy survey of the environment
  - Study received variation in received RF energy as function of time
  - Survey RF energy received in environment as a function of location
- (Chapter 3) Identify and study the effect of parasitic sources on performance of RF energy harvesting circuits through the development

and application of an analytical model of the RF energy harvesting circuit.

- Identify dominant parasitic loss mechanisms in the Villard voltage doubler as an RF energy scavenging circuit.
- Model and quantify the effects of stacking multiple Villard voltage doublers in series.
- Utilize model to optimize design parameters of a Villard voltage doubler.

- (Chapter 4) Study novel enhancements to RF power harvesting circuits to improve power harvesting efficiency, generate sufficient voltage at lower RF power levels to power a Smartdust node, and more efficiently demodulate RF signals.
  - Reducing body effect
  - Novel sacrificial current biasing
  - Novel parasitic resistant matching
  - Design and layout circuits that meet performance goals while meeting DRC/Antenna/Floating Gate rules
- (Chapter 5) The novel implementation and performance analysis of an RF power harvesting circuit as the demodulating element in an on-off keyed (OOK) receiver.
  - Studied and quantified the gain improvement of the power matched Villard voltage doubler as opposed to the conventional voltage rectifier.

        - Study and quantify the novel gain control characteristics of a RF power harvesting circuit as a receiver demodulator.
        - Study and quantify improved RF filtering resulting from a RF power harvester as the demodulating element in a receiver.
    - (Chapter 5) Optimize LNA and RF amplification stages of an OOK receiver for low power operation through determination of optimal number of stages and proper biasing between weak and strong inversion operation.
        - Development of a novel methodology from optimizing bias point and number of stages in a multistage LNA to achieve desired receiver sensitivity at minimal power cost.
        - Study improved RF filtering of multi-stage LNA design.
    - (Chapter 5) Integrate complimentary metal on silicon (CMOS) RF receiver circuits (low noise amplifier, RF power harvester, base band amplifier and comparator) under ultra low power constraints
        - 1 V supply
        - ~ 1 mW power draw

To better illustrate how this work is the necessary evolution of wireless sensor networks, the remainder of this chapter will begin with a brief history of wireless sensor networks. In addition, to properly motivate this work, the economic outlook and market applications for this technology will be reviewed. Finally, this chapter will present the characteristic and challenges of wireless sensor networks along with a

comprehensive survey of prior work in the fields of wireless sensor networks and energy scavenging to illustrate how this work addresses existing problems in the development of Smartdust sensor networks.

Brief History of Wireless Sensor Networks

The origins of the modern wireless data networks can be traced back to the ALOHA system. Developed in 1970 at the University of Hawaii, ALOHA was the first system to employ random access control. It spanned four of the Hawaii islands utilizing a 24 kbaud link operating at 400 MHz [2].

Research continued in the 1970s, thanks largely to support from the U.S. federal government. In 1972, the U.S. Defense Advanced Research Projects Agency (DARPA) initiated a program called the DARPA Packet Radio Network (PRNET) [1]. PRNET showed significant advancement over prior wireless digital networks such as the ALOHA system. It utilized direct sequence spread spectrum to enhance its performance in the presence of multi-path interference. Support for wireless sensor networks continued in 1980 when DARPA initiated the Distributed Sensor Networks (DSN) program [3]. Support for wireless data networks by DARPA has continued through the 1990's. As an example, the SensIT program founded in 1998 by DARPA has funded twenty-nine wireless network programs [1].

Support for wireless data networks in the commercial sector began to materialize in 1997, with the establishment of the 802.11 Wireless LAN (WLAN) standard by the Institute for Electronics Engineers [1]. These networks represented a major leap in wireless performance and at 54 Mbps rivaled the data rates of wired connections at the time [3].

More recently, there has been a trend towards smaller, low power networks called wireless personal area networks (WPANs) based on the 802.15 standard [1][3]. These networks are typically characterized by wireless links of a few meters. While there are several examples of WPANs, Bluetooth is the most common and successful standard for personal area networks [1]. At only 1 Mbps, data rates are significantly lower than those of WLANs.

Initiated in 1993 at University of Los Angeles and Rockwell Science Center, the Wireless Integrated Network Sensors (WINS) system was the first wireless network to sacrifice data rate and range to extend operational lifetime. In this manner it became the first example of the modern wireless sensor network. Data rates were limited to less than 100 kbps and multi hop protocols were used to limit the power used during transmission. In addition, time division multiple access (TDMA) was used for media access and a spread spectrum radio was utilized to enhance the performance of nodes in the presence of multi-path interference [4].

Development of wireless sensor nodes has continued with Picoradio, uAMPS and the Smart-Dust project. Picoradio, under development at Berkley, is a system on a chip approach to wireless sensor networks utilizing a spread spectrum transceiver [5]. This approach offers the potential for very low cost manufacture and is a continuation of the trend for smaller, lower power designs. uAMPS is an MIT project with the principal goal of lowering node power consumption [6]. A defining characteristic of the system is the LEACH protocol, which spreads cluster formation responsibility among varying nodes in the network to enhance node lifetime [1]. Smart-Dust is another MIT project with the goal to create a sensor node so small that it can be suspended in air. This requires a system volume on the order of a cubic millimeter. Towards this goal, optical communication is being pursued [7].

Motivation for Research

The market for wireless sensor networks is projected to experience rapid growth in the next few years. In 2005, there were 200,000 deployments of wireless sensor nodes worth 100 million dollars [8]. By 2011 the wireless sensor network market is expected to be worth 1.6 trillion dollars [9]. That represents growth by four orders of magnitude in market value.

Such large growth projections are largely a function of the broad spectrum of potential applications for wireless sensor networks. Among the most common applications are [1][5][7][10][11][12]:

- Security and Military Sensing
- Industrial Monitoring
- Asset Tracking
- Environmental Sensing
- Health Monitoring

The application of wireless sensor networks in these industries promises to change the way we live. Low cost, miniature sensor nodes could be sprayed or painted onto roads, walls, and machines; flooding human perception with a wealth of environmental knowledge ranging from traffic patterns to supply chains [13]. Even the human body could have wireless sensor nodes literally swallowed to provide critical information on the condition of the human body. Access would be a gained to a database of current environmental data that would never be outdated or require refreshing [13].

All of these applications have distinct requirements that make them highly suitable for the application of wireless sensor networks.

The first is that these applications require deployment into areas where a networking infrastructure does not currently exist. For example, in security sensing, possible deployment scenarios involve rapid deployment after a natural disaster. In a natural disaster such as a hurricane, the traditional networking infrastructure may be inoperative. Wireless sensor networks could provide a fast means to gather real time data on conditions shortly after such a disaster.

In addition, these applications share the need for wireless nodes with a very small system form factor. Health monitoring could utilize "dust size" systems on the order of a few millimeters cubed to deploy wireless sensor networks directly into the human body. Such systems could provide real-time feedback to surgeons and doctors on a patient's condition without the use of more invasive procedures.

A third characteristic shared by these applications, is the need for networks that organize themselves in an ad-hoc fashion. Asset tracking involves the creation of a network of nodes that are constantly being moved spatially. The spatial movement of the nodes translates into an ever-changing link configuration between nodes and network routing must be able to dynamically adjust routing to changes in the network topology.

The ability to operate for long periods of time unassisted is a fourth characteristic desired by the applications. Environmental sensing is generally characterized by the ability to deploy wireless sensor nodes into remote locations. Such a location

requires a network node that can last for long periods of time without access to a power infrastructure, maintenance or recharge [12].

Given the scale of possible deployments of wireless sensor nodes, all of the example applications require that individual nodes be very low cost. Given the desire to maximize profit, asset tracking and industrial monitoring require that wireless sensor networks cost be minimized such that the there is a net overall profit from their use. In addition, military and health monitoring requires that node cost be minimized to prevent large deployments of wireless sensor networks from becoming prohibitively expensive.

Defining Characteristics of a Sensor Network

Wireless sensor networks represent a major research challenge. To better understand the scope of that challenge, one should look at the defining characteristics of a wireless sensor network:

- Sensor networks are made of tiny sensor nodes [4][14] – Target sizes for nodes are on the order of a centimeter cubed. Among the components that need to be

incorporated into this confined space are the microprocessor, memory, sensors, transceiver and power sufficient to perform sensing and networking.

- Sensor nodes will be randomly distributed [13][14] - Sensor nodes will also be expected to operate efficiently no matter how they are oriented. Environmental obstruction may be common and ideal orientation of the antenna or transmit and receive structures cannot be guaranteed.

- Sensor nodes are self-contained [1][13][14] – Sensor nodes will be required to maintain operation for long periods of time (> 1 month). Due to the size restrictions on sensor nodes, extremely small batteries must be used. Therefore, power consumption must be kept to a minimum to allow for adequate battery life. Power harvesting from the environment may be possible to extend node life. Solar power, kinetic energy, radio frequency, and thermal power are among the possible external power sources under study.

- Network topology changes frequently [12][14] – Sensor nodes will be prone to failure due to a variety of reasons. Changing environmental conditions can weaken transceiver links. Power restrictions can require motes to go off-line either temporarily or permanently. In addition, network topology can change due to the actual movement of sensor nodes.

- Sensor nodes will be deployed in large numbers [12][14] – Sensor networks may be deployed with nodes numbering in the hundreds to thousands. As a result, sensor networks need to be highly scalable.

- Sensor networks broadcast information [12] – A sensor network's primary function is to move information from the sensors back to the access point. Traditional networking protocols use global identification to enable point-to-point communication. Due to the sheer volume of sensor nodes deployed in a network, global identification is impractical. Therefore, access points will make requests for data types to the network, and the nodes that can address that requirement will respond.

Challenges in Physical Layer Implementation

The characteristics of wireless sensor networks have implications at the physical layer of the network. For example, wireless sensor networks must have a long lifetime. This facilitates the need for a physical layer that is very low power. The modulation format must be carefully chosen to minimize the energy necessary to transmit and receive each bit of data. Furthermore, given that data rates are low, and it is desirable to minimize the time spent broadcasting, data is best broadcast in short bursts [15].

Another characteristic with important implications to physical layer design is the need for small size. Dimensions of less than a cubic centimeter severely limit the amount of energy that can be stored on a system's battery. This again facilitates the need for low power transceiver design, but also makes the use of energy scavenging from the environment attractive. In addition, the small size requirement of wireless sensor networks translates into a small antenna. Smaller antennas generally require the use of a higher carrier frequency for transmission. Higher carrier frequencies require higher power requirements; therefore, a system optimization is necessary to balance the requirement for small size and low power.

Given that sensor nodes will be deployed in large numbers, the cost of individual nodes is an important consideration. To drive down the price, is it desirable to implement the design directly onto CMOS. This is also consistent with the desire for a small system size.

Lastly, since sensor nodes are randomly distributed, the physical layer must be able to cope with the possibility of a non-optimal orientation or placement. Under ideal conditions, signal power degrades as the inverse square of the distance, r, from the transmitting source ($1/r^2$). Given that sensor nodes could be located behind obstructions or directly on the ground, $1/r^2$ free space path loss is unlikely. Therefore, the physical layer implementation of the transceiver must have a sensitivity sufficient to bridge air gaps even when $1/r^3$ or even $1/r^4$ path loss is encountered [4][16]-[20].

Current Research in Wireless Sensor Network Transceiver Design

A literature survey in the fields of low power wireless transceiver design and RF power harvesting provides the context for contrasting this work with prior works in wireless sensor networks and energy scavenging.

Coherent Modulation

Given that low power operation is a critical requirement for wireless sensor networks, it is important to choose a modulation technique that is optimal for low power consumption. Typically transmission systems are designed to be spectrally efficient utilizing coherent modulation and demodulation techniques. Coherent demodulation and modulations refers to mixing an RF data signal with a synthesized frequency of known phase. In this manner, data can either be stored or extracted from and combination of the phase, amplitude and frequency of an RF signal.

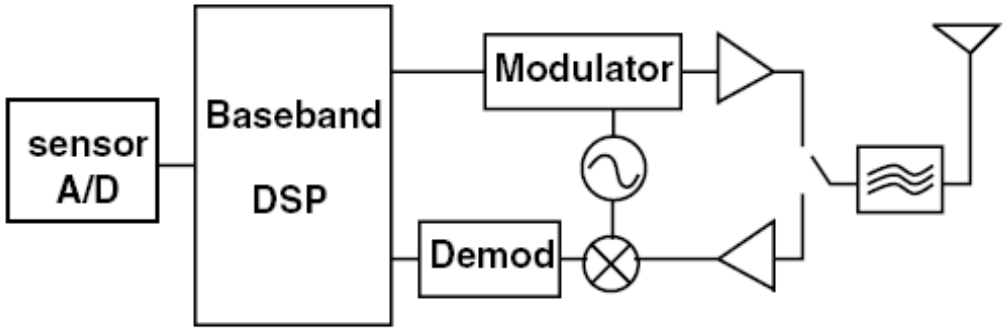


Fig. 2 Typical transceiver design [21].

The coherent architecture in Fig. 2 is necessary for spectrally efficient phase shift keying (PSK) and quadrature amplitude modulation (QAM) transceivers. PSK and QAM are very popular modulation techniques. PSK stores the transmitted information in the phase of the RF signal, while QAM stores information in both the phase and amplitude of the transmitted RF signal.

However, this system architecture requires the use of RF mixers, phase locked loops (PLL) and voltage controlled oscillators (VCO). These components dominate the power consumption of the transceiver due to long turn on times [22]. Given that sensor node communication is characterized by short bursts of data, long transient start up times result in a large amount of wasted energy to start up the transceiver [21]. The importance of minimizing start up time can be further illustrated by plotting energy consumption per bit versus transient start up time for the transmission of a single data packet.

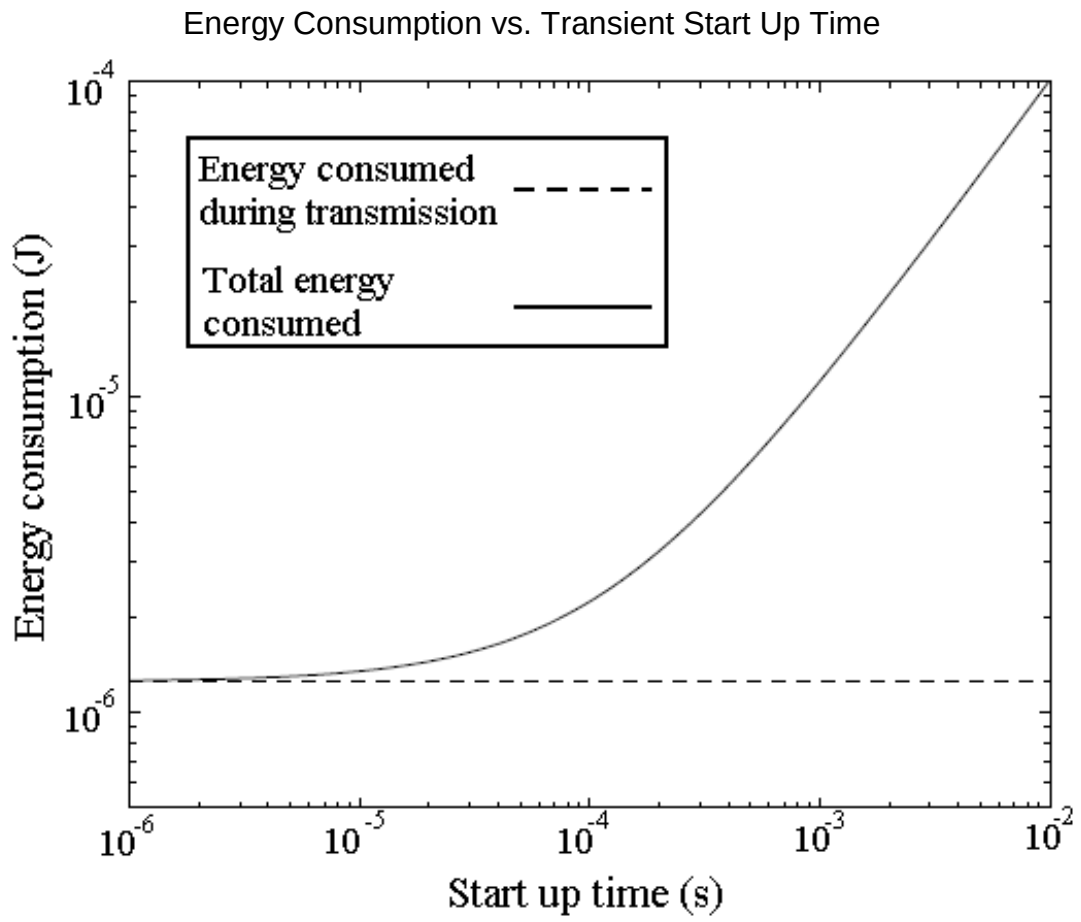


Fig. 3 Energy consumption vs transient start up time for a 100 bit packet transmitted at 1 Mbps [23]

Several efforts in wireless sensor node transceiver design have championed the use of spread spectrum as the digital modulation scheme [4][5][24]. Spread spectrum shows strong performance in the presence of multi-path [25]. Spread spectrum refers to the practice of mixing an RF data signal with a chipping signal from a pseudo-orthogonal set that is faster than the symbol rate of the RF signal. The signal's spectrum in the frequency domain becomes flat and spread out resulting in a signal that can be difficult to distinguish from the thermal noise. The spread signal offers an inherent immunity to narrowband interference sources. The original RF data signal can be

retrieved by remixing the spread signal with the original chipping code. Like PSK and QAM modulation, spread spectrum has a start up time limited by the transient turn on time of the frequency synthesizer [24]. Therefore, it is not optimal for low power communication.

Non-Coherent Modulation

The need for a transceiver system with a fast transient turn on time favors non-coherent modulation and demodulation techniques. Non-coherent modulation refers to the addition or recovery of data from an RF signal without knowledge of the phase of the RF signal. Work has been proposed that favors the use of non-coherent frequency shift keying (FSK) modulation [26]. FSK modulation stores the transmitted data as the instantaneous frequency of the RF signal. The simplest binary implementation of FSK modulation refers to indicating a binary one by transmitting at a given frequency during the bit period, or indicating a binary zero by transmitting at another tone during the bit period.

Through the use of a fractional N synthesizer with sigma delta modulation, transient turn on times as low as 10 us can be realized for an FSK transmitter. However, such a design requires an estimated transmit power on the order of 12 mW. 10 mW of the transmit power is required to operate the fractional N frequency synthesizer. Given that the design is estimated to transmit 0 dBm, the system achieves a power out to DC power draw efficiency of only 8.3%. Although this design minimizes energy

consumption from a transient turn on time perspective, it clearly does not achieve a high power efficiency.

On-off keying (OOK) modulation is another technique that can be implemented in a non-coherent manner of reception. OOK modulation stores the transmitted data as the amplitude of the RF signal. The simplest form of OOK modulation is binary OOK and indicates the state of digital data through the presence or absence of RF energy during a bit period.

A criticism of OOK modulation has been the perception of poor performance compared to FSK [27]. This assumption is not entirely valid. The probability of a bit error for non-coherent OOK and FSK can be expressed as:

$$P_{error,OOK} = \frac{1}{2}\left(1+\sqrt{\frac{1}{\pi \cdot SNR}}\right)\cdot e^{-\frac{SNR}{4}}$$

Eqn. 1. Probability of error for an OOK signal [28].

$$P_{error,FSK} = \frac{1}{2}\cdot e^{-\frac{SNR}{4}}$$

Eqn. 2. Probability of error for an FSK signal [28].

Where signal to noise ratio (SNR) is the power of the desired data signal to the power of the noise in the RF signal. The Nyquest theorem can be utilized to determine the relation between SNR and the ratio of the total signal energy to noise energy in a bit period (E_b/N_0) assuming non return to zero (NRZ) signaling.

$$SNR = \frac{f_b \cdot E_b}{B \cdot N_0}$$

Eqn. 3. Relation of SNR to the energy per bit (E_b), noise per bit (N_0), channel data rate (f_b), and bandwidth (B).

By plotting the two equations (Eqn. 1) and (Eqn. 2) against E_b/N_0, it can be concluded that there is very little difference between the probability of a bit error (BER) for non-coherent FSK and non-coherent OOK modulation (Fig. 4).

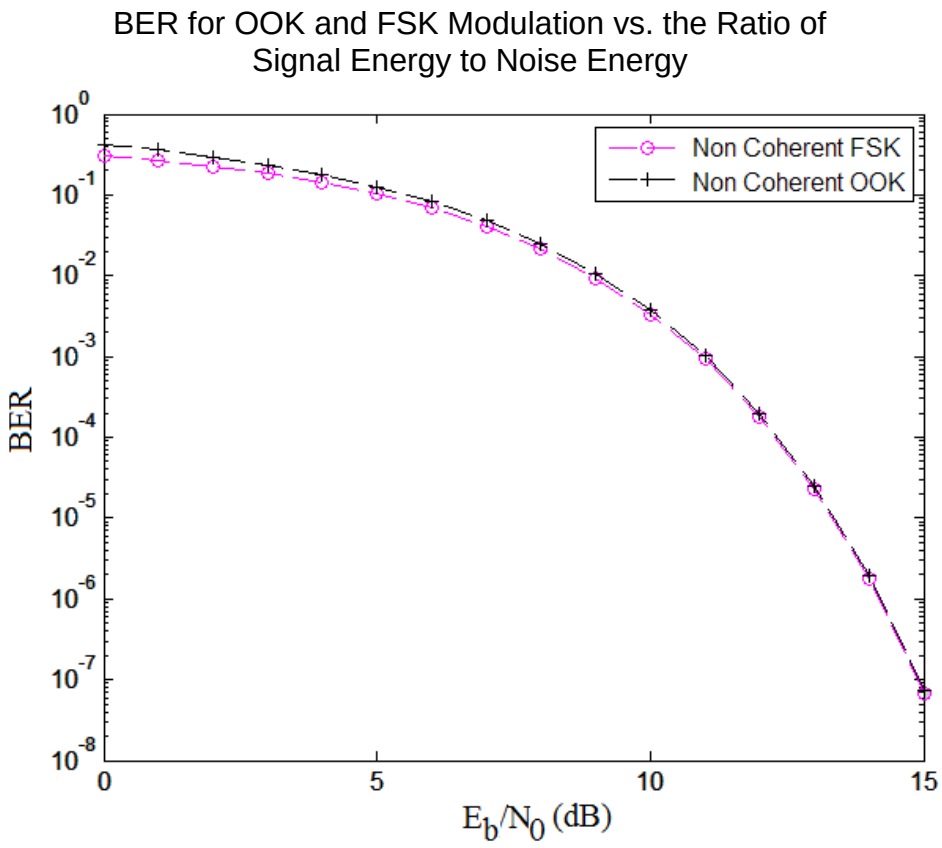


Fig. 4 Plot of Bit Error Rate (BER) for OOK and FSK modulation vs the ratio of signal energy per bit to noise energy per bit ($E_b/N_{0)}$.

Another criticism of OOK transmission has been its performance in the presence of co-channel interference. To refute that criticism, the probability of error for a signal of interest in the presence of an interfering signal in an OOK transceiver is derived in the work by Anthes [29].

$$P_{err} = \frac{1}{2}P_{miss} + \frac{1}{4}P_{false\_alarm} + \frac{1}{4}P_{jam}$$

Eqn. 4. Probability of error from co-channel interference of an OOK signal

Where P_{miss} is the probability of error when a one is present for the desired signal. P_{false_alarm} is probability of error when both desired signal and interfering signal transmit a 0. And P_{jam} is the probability of error when the desired signal is a 0 and the interfering signal is a one.

The probability of each error condition is expressed as:

$$P_{miss} = \frac{1}{\sqrt{2 \cdot \pi}} \int_{-\infty}^{\frac{V_t - Sd_1}{\sigma}} e^{-\frac{z^2}{2}} dz$$

Eqn. 5. Probability of error when the symbol "1" was transmitted given a decision threshold of V_t, received signal level of Sd_1 and standard deviation of σ [29].

$$P_{false\_alarm} = \frac{1}{\sqrt{2 \cdot \pi}} \int_{\frac{V_t}{\sigma}}^{\infty_1} e^{-\frac{z^2}{2}} dz$$

Eqn. 6. Probability of an error when a zero is transmitted and the interfering signal transmits a zero given a decision threshold of V_t and standard deviation of σ [29].

$$P_{jam} = \frac{1}{\sqrt{2 \cdot \pi}} \int_{\frac{V_t - Si_1}{\sigma}}^{\infty_1} e^{-\frac{z^2}{2}} dz$$

Eqn. 7. Probability of an error when a zero is transmitted and the interfering signal transmits a one given a decision threshold of V_t, received signal level of Si_1 and standard deviation of σ [29].

When the probability of error (P_{err}) is plotted versus the difference between desired signal and interfering signal in decibels, it can be seen that for 15 dB of SNR, a

minimum delta between the desired signal and interfering signal of 13 dB is needed to prevent a significant increase in BER (Fig. 5).

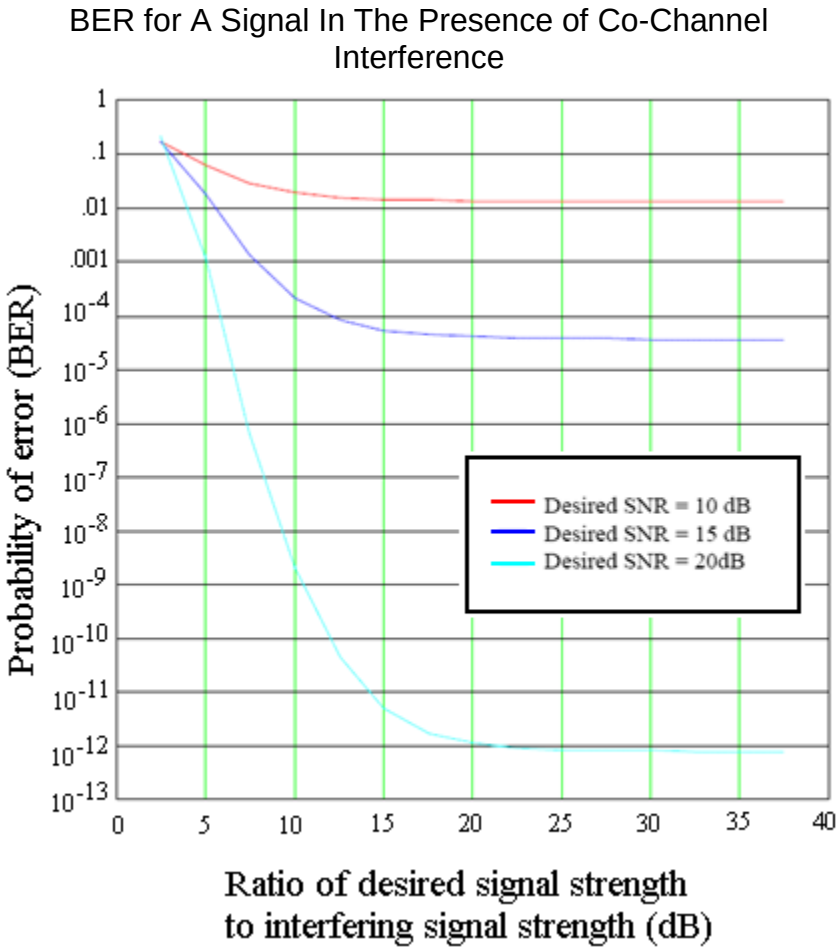


Fig. 5 BER versus the ratio of the desired signal to interfering signal (in dB) for the indicated desired signal SNRs of 10 dB, 15 dB and 20 dB. [29]

In contrast, FSK should theoretically be immune to an interfering signal, until the interfering signal strength is larger than the desired signal. For this reason, FSK clearly demonstrates superior performance in the presence of co-channel interference. However, wireless sensor networks must be able to operate in the presence of

unreliable link communications [12]. Therefore, a certain susceptibility to channel interference may be acceptable.

Given that rejection of channel interference is not a critical design parameter and that a non-coherent OOK transceiver is the simplest and thus, has the least components to draw power, non-coherent OOK modulation is an attractive option for wireless sensor networks. Daly and Chandrakasan propose the use of a non-coherent OOK transceiver for wireless sensor networks [30]. The transmitter is a simple surface acoustic wave (SAW) resonator connected to a power amplifier. The receiver consists of an LNA, followed by a series of differential RF amplifiers. The signal is then fed into a differential voltage rectifier and then amplified using a base band amplification circuit. Operating at 916.5 MHz, the system consumes only 2.6 mW when receiving a 1 Mbps signal. This is a significant reduction in the power requirements compared to other works in the field [4][5][6].

However, the system Daly and Chandrakasan is not without its limitations. Receiver sensitivity is limited to only -65 dBm [30]. This translates to about 20 m of transmission range using the ideal free space path loss model. Given that typically path losses on the order of r^3 and even r^4 can be expected, -65 dBm is not sufficient to meet the 10 m goal of wireless sensor networks [4][16]-[20]. In addition, transmitter efficiency is poor due to a transmitter that requires over 9 mW but transmits only -2.2 dBm. Furthermore, due to the SAW oscillator having a turn on time greater than a bit

period, the transmitter cannot be turned off during the transmission of a zero bit. This effectively doubles the average power requirement of the transmitter.

M-ary vs Binary Modulation

A reduction in transmit time to send a packet could directly lead to energy savings and extend the operational life time of a sensor node. It then stands to reason that m-ary modulation which transmits more than one bit per symbol could reduce power consumption. However, the m-ary transmitter is significantly more complex and as a result requires more power than a binary modulated transmitter.

$$\alpha < n\left(1+\frac{P_{FS-B}\left[\left(1-\frac{\beta}{n}\right)T_{on}+(1-\beta)T_{st}\right]}{P_{\mathrm{mod}-B}\cdot T_{on}}\right)$$

Eqn. 8. α is the ratio of energy required for m-ary modulation to the energy required for binary modulation.

Through the derivation and analysis of Eqn. 8, the work by Shih et al. concludes that the transient start up time must be less than the packet transmit time for m-ary modulation to operate at lower power than binary modulation [22]. α is the ratio of energy required for m-ary modulation to the energy required for binary modulation and is a function of the power draw of the frequency synthesizer ($P_{FS-B)}$ and modulator (P_{mod-B}) of a binary transceiver; the ratio of power draw for a m-ary frequency synthesizer versus binary frequency synthesizer, β; the transmission time (T_{on}) and startup time (T_{st}); and n is the number of bits per symbol. The paper

admits that this analysis is only valid if the output power of the transmitter is very small compared to the DC power draw of the transmitter. In other words, the power of the transmitter must be dominated by the modulation circuitry power requirement, not the power amplifier power requirement. This is not desirable in a power efficient transmitter.

Weak Inversion

Up to this point, alternative system architectures and modulation formats have been explored to improve the power efficiency of a Smartdust receiver. However, the circuit design and physical implementation of a receiver is also important design criteria for low power receiver design. For example, work by Enz et al. on the EKV model (named after the authors Enz, Krummenacher, and Vittoz) suggests that the operation of RF circuits in weak inversion represents an effective means to lower the power consumption of receiver designs regardless of the system architecture or modulation format used [31].

The operation of a transceiver in weak inversion has been examined by researchers at the Swiss Federal Institute of Technology [32][33][34]. Given a supply voltage of only 1 V in the .5 um AMI process, the best inversion coefficient (IC) achievable was 10. The inversion coefficient is a measure of the level of inversion of the metal on silicon field effect transistor (MOSFET) channel and is defined as:

$$I_c = \frac{I_d}{I_s}$$

Eqn. 9. Inversion coefficient of a MOSFET as defined by EKV model [31].

Where I_d is the drain current and I_s is the specific current which is defined as a function of the thermal voltage (V_T), gate oxide capacitance (C_{ox}), gate dimensions (W, L), electron mobility (u_n), and transconductance of the gate (gm_g) and source (gm_s):

$$I_s = 2 \cdot \left(\frac{gm_s}{gm_g} \right) \cdot u_n \cdot C_{ox} \cdot \frac{W}{L} \cdot V_T^{\,2}$$

Eqn. 10. Specific current of a MOSFET as defined by the EKV model [31].

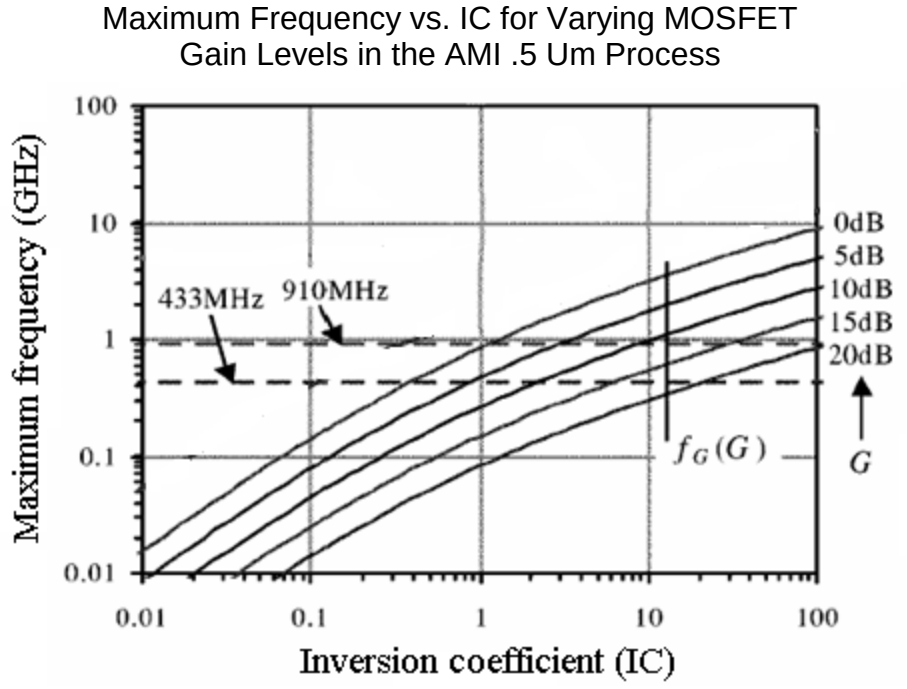


Fig. 6 Maximum frequency (f) versus inversion coefficient (IC) for the indicated current gains (G) in the AMI .5 um process [32].

Fig. 6 above illustrates that with an IC of only 10, a gain of 18 dB was still achievable at 433 MHz. Although weak to moderate inversion has a negative impact on the bandwidth gain product of the MOSFET, it offers a better trans-conductance to DC current draw ratio [31]. The system achieved the impressive feat of transmitting 24 kbps with a -95 dBm sensitivity and the transmitter was forty percent efficient with 10 dBm output power. However, limiting the carrier frequency to 433 MHz, places constraints on the minimum antenna size. In addition, the system relied upon external passives, which also places constraints on minimal system size.

Optics

The use of optical communication has been proposed in the Smart-Dust program at MIT. The goal is to create a sensor node so small that it can be suspended in air. This requires a system volume on the order of a cubic millimeter [7]. Optical communication is well suited for small form factors since an antenna is unnecessary. In addition, the power necessary to transmit and receive over millimeter distance is small (sub milliwatt) [7]. However, optical free space communication requires line of sight. Akyildiz et al. indicate that line of sight may not be dependable in wireless sensor network communication [12].

Passive Tags/RFID

Low power transceivers have been proposed that utilize RF power harvesting to directly power the system. These designs, which are often referred to as passive radio frequency identification (RFID) tags, rely on a capacitor for energy storage and do not carry a battery. Therefore, they must receive enough input RF energy to supply the instantaneous current demands of the transceiver. Facen and Boni propose a system that utilizes a full wave rectifier and charge pump to power the transceiver from the 895.5 MHz received data signal. This system has a predicted operational range of only 5.3 m [35]. Gregori et al. propose an alternative design that utilizes a power matched half wave rectifier circuit [36]. This design requires 250 uW of energy to correctly function. These designs illustrate the primary disadvantage of passive tags. They typically only operate at close range (<10 m) to strong power sources.

Current Research in Energy Harvesting

As the demodulating element in the low power receiver and energy source for the system, RF energy harvesting is a critical component of the research presented in this work.

Alternative Sources for Energy Harvesting

Many works in the literature have proposed alternative sources for energy harvesting. By reviewing the work done on these alternative techniques, distinct advantages of RF power harvesting become apparent.

Vibrational energy has been a popular topic for energy harvesting research. The three techniques for converting vibrational energy to electrical energy are piezoelectric, electrostatic and electromagnetic. Roundy et al. report that up to 300 uW/cm^2 of electrical power could be generated form vibrational energy in the environment [37]. Measurements on fabricated systems in the same work report 180 uW/cm^2 of electrical power generated when exposed directly to the vibrating case of an operating microwave oven.

There has been additional work in vibrational energy harvesting. Work by Shearwood and Yates, and Williams et al. reports .3 uW generated form a 4.4 kHz source using electro-magnetics and MEMS [38][39]. Meninger et al. model a system that could generate 8.6 uW [40][41]. Work by Kulah and Najafi reports 2.5 uW at 150 mW theoretical output [42].

The human gait has been examined extensively as a source of energy for vibrational energy scavenging [43][44]. Amirtharajah and Chandrakasan theorize as much as 400 uW could be generated from the human gait [43].

All of these works share one common problem. They all require that the vibrational energy-scavenging device be connected to specific environmental sources that are known to have high densities of vibrational energy. Useful environmental sources seem to be limited by close proximity to microwaves, milling machines, kitchen blenders, etc [37].

Solar cell efficiencies of twenty five to twenty seven percent have been realized in recent works [45][46]. Theoretical modeling predicts efficiencies as high at 46.6% but this has not yet been measured experimentally [47]. Solar power density ranges from about 100 mW/cm^2 outdoors on a sunny day to 100 uW/cm^2 for office light conditions. This ranges from a generated power density of 27 mW/cm^2 to 27 uW/cm^2. Solar energy is currently under investigation as the power source for the Smart-Dust program at the University of California at Berkeley [48][49].

Solar energy shows significant potential for outdoor environments, but as indicated by the lower power density for office lighting conditions, has limited value for indoor conditions. In addition, the orientation of the solar cell is a critical parameter in the use of solar power and may not be controllable in a wireless sensor network.

Several works have investigated the generation of electrical energy from thermal temperature gradients. The efficiency of converting thermal power to electrical power is limited by the Carnot efficiency [50].

$$N = \frac{T_{high} - T_{low}}{T_{high}}$$

Eqn. 11. Carnot efficiency of electrical to thermal conversion defined as a function of the high (T_{high}) and low (T_{low}) temperatures of the thermal gradient.

Useful energy levels are reported for temperature gradients of a few degrees over short distances (millimeters). One work reported the generation of 40 uW from only a 5 degree (Celsius) temperature gradient [51] . The device was .5 cm^2 by a few millimeters thick. Other groups have reported similar successes. Thermolife is a device measuring only 1.4 mm thick and 9.3 mm in diameter and is able to generate up to 100 uW from a 10 degree (Celsius) temperature gradient [52]. Stordeur and Stark report 20 uW generated from a 20 degree Celsius temperature gradient [53] while Strasser et al. have successfully generated 1 uW from a 5 degree Celsius temperature gradient [54].

Thermo electrics haven't been confined to low power. Ono et al. report 7.6 mW generated from 64 degree Celsius temperature gradient [55]. Unfortunately, system performance degraded to 5.6 mW after 10 days due to increase resistivity of the $Na_{.7}CoO_2$.

Techniques are also being developed to improve the performance of thermal scavenging. V-VI materials as well as nano wires are among the device improvements being investigated [56][57]. A system improvement under investigation is the use of pulsed outputs to generate a higher average output power [58].

Novel applications and structures for thermal energy harvesting are also under investigation. Work by Rahman and Shuttleworth has demonstrated a working system to operate a computer off of thermoelectrically-generated energy [59]. Fleurial at al. have proposed a battery hybrid that can be recharged thermally [60]. Among the more novel structures under investigation, Hasebe et al. have successfully fabricated flexible devices for scavenging thermal energy that can generate 15.4 uV per degree Kelvin [61].

The human body has been proposed as a source of thermal energy for energy scavenging. Jacqout et al, theorize that 60 uW could be generated from the waste heat of the body [62]. However, this has not yet been realized experimentally.

Unfortunately, little information is available on how common 5 to 10 degree (Celsius) temperature gradients over short distances are in the environment. Anatychul and Mikityuk report that thermal differences in soil are highly seasonal [63]. At 25 to 30 cm under the surface, temperature gradients of 15 to 30 degree Celsius are common in the summer but only 5 to 8 degrees is typical in the winter. Therefore, the ability to use thermal energy as a source of energy for wireless sensor networks is questionable.

RF Energy Harvesting

The environment is full of radiated emissions. Even at a kilometer away from an FM radio tower, peak indoor power densities better than .5 uW/cm^2 can be detected [64]. Similar power densities can be detected at higher frequencies (including cellular bands) both domestically and internationally [65][66].

Given a radiated frequency of 900 MHz from a cell tower and a simple quarter wavelength antenna at the RF power harvesting circuit, .5 uW/cm^2 equates to approximately 60 uW of received power (Eqn. 12 and Eqn. 13). This power level is consistent with the expected received RF energy 150 meters from a cell tower transmitting at 100 W.

$$A_{eff} \sim \frac{1}{8}\lambda^2 = \frac{1}{8}\cdot\left(\frac{c}{f}\right)^2 = 134\,cm^2$$

Eqn. 12. Effective area of quarter wavelength antenna as a function of the signal wavelength (λ) or the speed of light (c) and the signal frequency (f).

$$P_{received} = A_{eff} \cdot .5\frac{uW}{cm^2} \sim 66\,uW$$

Eqn. 13. Power received from a 900 MHz source on a quarter wavelength antenna from an electric field intensity of .5 uW/cm^2.

Fundamentally, approximately 60 uW of power is available to recharge a battery or power a system from the radiated RF power from a cell tower signal at a distance of over a 100 m.

Roundy et al. questions the usefulness of the expected power densities for RF energy when applied to wireless sensor networks [37]. However, the reported power densities for RF are for the average amount of RF energy found anywhere in the environment as compared to energy densities right next to a strong vibrational or thermal source. If one was to place the RF energy harvesting device within .1 m of an RF energy source commonly found in the environment, as is done in the case of reported vibrational and thermal power harvesting experiments [37]-[41][52][52], one could easily achieve power densities of greater than 450 uW/cm^2 from a 250 mW transmitter such as cell phone. This compares favorably with reported energy densities for thermal and vibrational energy scavenging.

Voltage Doubler

To generate voltages sufficient for powering wireless sensor nodes from ultra low power levels, the voltage doubler has been a popular topic for RF energy harvesting research.

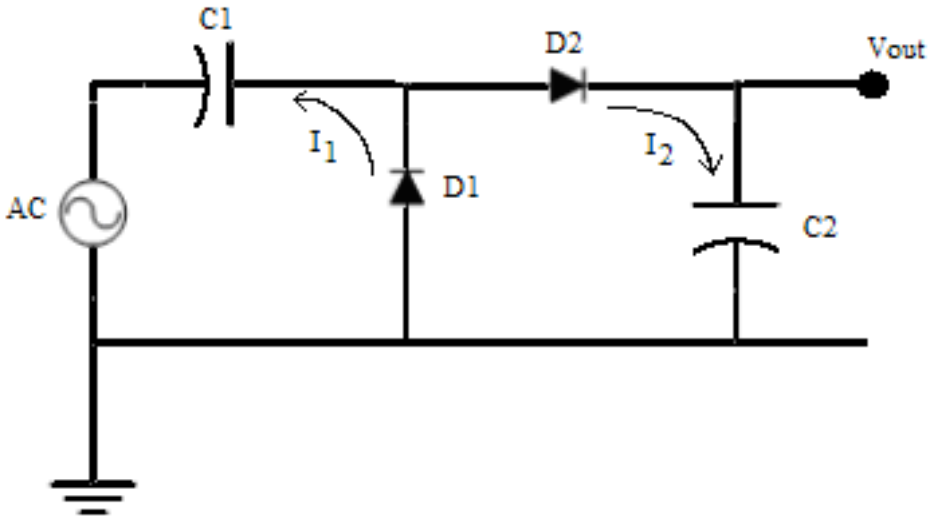


Fig. 7 Single stage of a voltage doubler circuit.

Fig. 7 illustrates the basic voltage doubler circuit. An intuitive understanding of this circuit can be gained by first examining what occurs when current flows in the direction of I_1 (the down swing of the AC current). D_2 blocks the flow of current through C_2. As a result, all the current goes across C_1. This charges C_1 up to roughly the same level as the peak of the AC voltage. Once, the upswing of the AC cycle (I_2) is reached, the voltage across both the AC source and C_1 drop across C_2, charging it to approximately twice the peak voltage of the AC signal [67].

Joe and Chia propose a more rigorous analysis that is based on the diode equivalent model [68]. The analysis relates the input power to the voltage at the input of the voltage doubler through a matching circuit as:

$$V_1 = \sqrt{2 \cdot R_d \cdot P_{in}}$$

Eqn. 14. Voltage at input to energy harvesting circuit from Joe and Chia model.

R_d is the real part of the diode equivalent model impedance and P_{in} is the input RF power. V_1 is then related to the output voltage of the AC model as:

$$V'_{out} = \frac{i \cdot V_1}{\omega \cdot R_d \cdot C_d}$$

Eqn. 15. Voltage at output of RF energy harvesting circuit from Joe and Chia model.

Where C_d is the effective capacitance of the diode equivalent model at the desired angular frequency, ω. Finally, the output DC voltage is defined as the AC output voltage in series with an internal resistance. The internal resistance is defined as the inverse of the slope of the diode characteristic curve when the DC current approaches zero. This is an approximation that assumes the diode acts as a linear junction when forward biased.

In the case where the diodes are replaced by diode connected NMOS, Yao et al. provides for an analysis of the expected efficiency of the voltage doubling circuit [69]. The power lost in a diode connected MOSFET is derived to be:

$$P_{nmos,loss} = \frac{1}{2} V_i^2 \left(\frac{1}{R_c} + R_c \cdot \omega^2 \cdot C_p{}^2 \right)$$

Eqn. 16. Power loss in NMOS of RF energy harvesting circuit.

Where R_c and C_p are the junction resistance and capacitance in the diode equivalent model for a diode connected MOSFET, ω is the angular frequency, and V_i is the incident AC voltage to the voltage doubler. Yao et al. use this analysis to show that the efficiency is maximized at a single distinct load resistance [69]. This result is supported by the analysis in Joe and Chia [68].

Resonant Voltage Boosting

The work by Yan et al. provides a methodology for boosting output voltage from a voltage doubler utilizing a resonant tank [70]. A resonant tank is illustrated in Fig. 8.

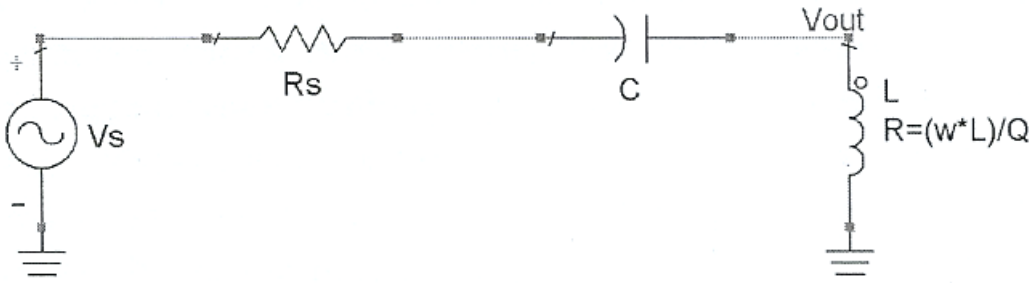


Fig. 8 Resonant tank boosting circuit.

From the circuit parameters presented in Fig. 8, the output voltage of the resonant tank which is the source voltage for the voltage doubler is derived by Yan et al. to be:

$$V_{out} = V_s \cdot \left| \frac{j\omega L + \frac{\omega L}{Q}}{j\omega L + \frac{\omega L}{Q} + \frac{1}{j\omega C} + R_s} \right|$$

Eqn. 17. Output voltage from resonant tank circuit and voltage doubler as a function of the circuit parameters defined in Fig. 8.

In the ideal case where Q is extremely high, this can simplify to:

$$Vout = \frac{1}{R_s} \cdot \sqrt{L/C} \cdot V_s$$

Eqn. 18. High Q approximation of output voltage form resonant tank circuit.

The analysis assumes that the input impedance to the voltage doubler is orders of magnitude larger than the inductance used in the resonant tank. Given typical junction capacitances for diodes, this may not be true for large inductances.

Energy Harvesting with Multiple Antennas

Mi et al. propose the use of multiple antennas in the same space (Fig. 9) to increase the energy generated through RF power harvesting [71].

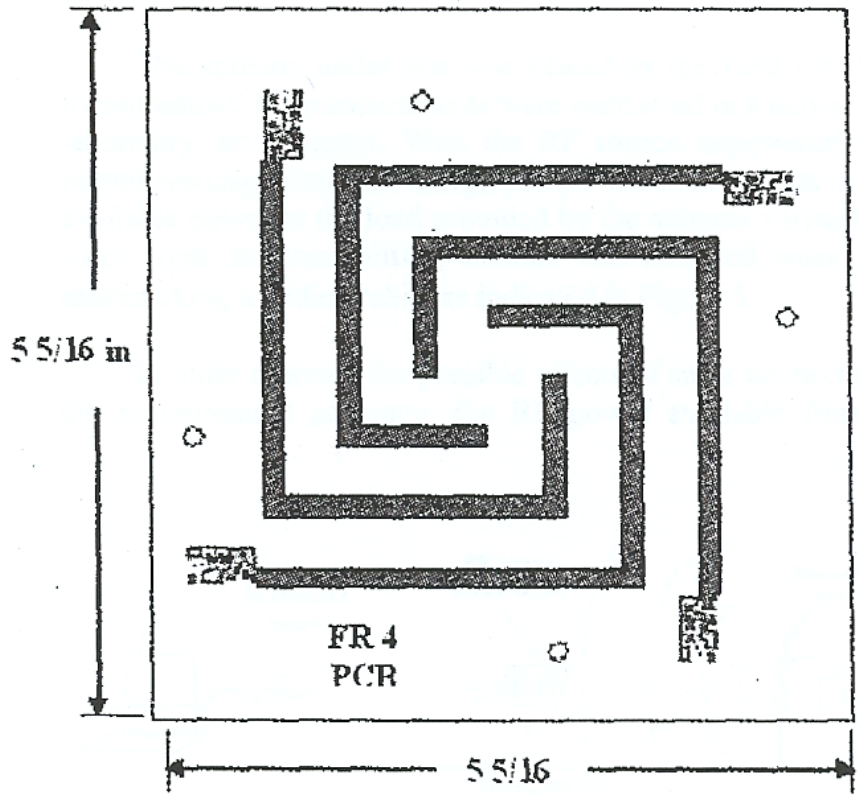


Fig. 9 RF Energy harvesting utilizing multiple antennas in the same space.

The proposed multi antenna design is impedance matched to a voltage doubling circuit with each antenna connected to its own voltage doubling circuit. Circuit topologies for connecting the RF energy scavenging antennas in series and parallel are presented and analyzed.

RF Power Harvested vs. Distance from an RF Source for Various Multi-antenna RF Energy Harvesting Designs

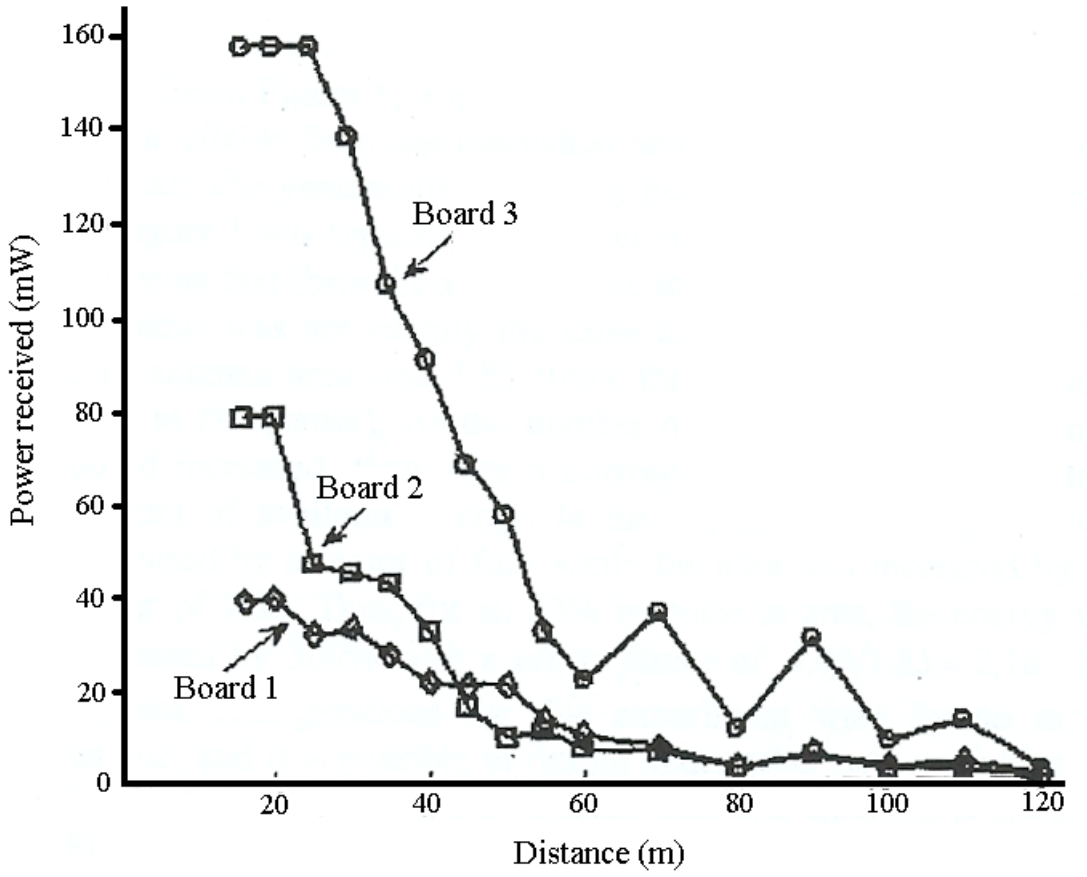


Fig. 10 Power generated from board 1 (single antenna), board 2 (two antennas), and board 3 (four antenns) at various distances form an RF energy source.

A parallel circuit is chosen and experimental measurement (Fig. 10) confirms that the combined RF power scavenged from a multi-antenna design is four times greater than the RF power scavenged from a single antenna design. The factor of four power increase is obtained at an increase in form factor of only 1.83 times the single antenna area. Thus, the work demonstrates a 300% increase in power while utilizing only 83% more space.

Substrate Losses

The work by Heikkinen et al. studies the effect of substrate loss on surface mount voltage doubler circuits used for RF power harvesting [72]. Surface mount substrates were modeled and compared including RT 5870, RT 6010 and FR4. RT 5870 was shown both through simulation and through measurement to provide the best performance. The work supports that the substrate for surface mount designs must be chosen to minimize parasitic losses.

Alternative Designs

Inductive coupling utilizes the flux from an electromagnetic field (B), through a loop of area A, and resistance R_{loop}, to generate current.

$$I = \frac{-\frac{d\left(\oint B \cdot da\right)}{dt}}{R_{loop}} = \frac{-\frac{\Delta\left(B \cdot A \cdot \cos(\phi)\right)}{\Delta t}}{R_{loop}}$$

Eqn. 19. Current generated on wire loop from electromagnetic flux.

Inductive coupling is a near field technique and as such has limited range. Work in the literature has reported maximum ranges of 28 mm from an RF signal described only as high power operating at 4 MHz [73].

The full wave rectifier depicted in Fig. 11 is another alternative to the voltage doubler circuit.

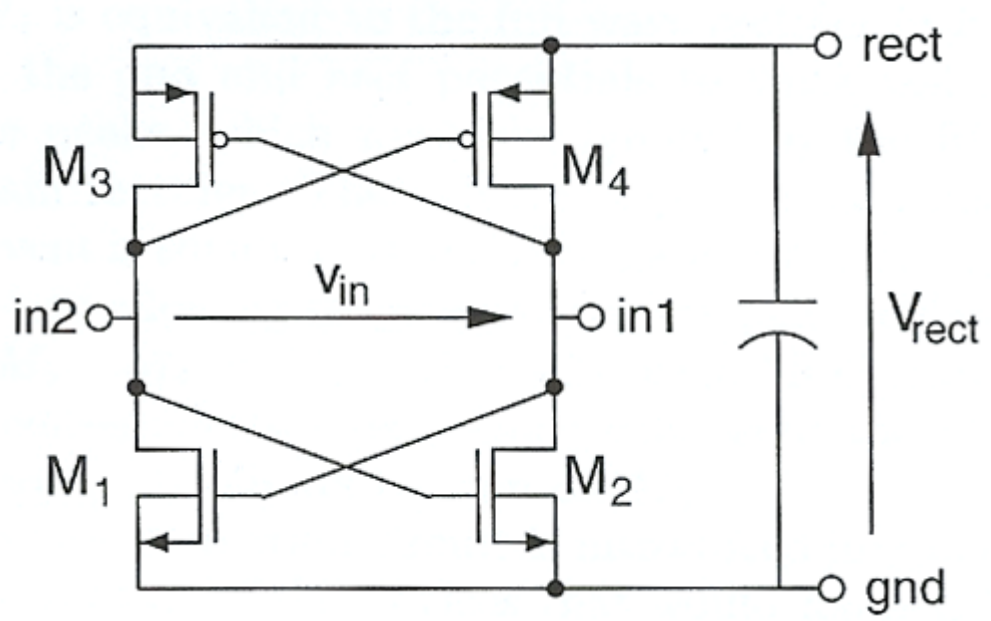


Fig. 11 Full wave rectifier circuit.

However, each swing of the input voltage must overcome two diode threshold voltages. This is in contrast to the voltage doubler, which only attenuates each swing of the input voltage through one diode threshold voltage. Therefore, the characteristics of the full wave rectifier are less favorable for RF power harvesting. In addition, the maximum voltage out of the full wave rectifier is the voltage at the input of the rectifier as opposed to twice the input voltage as is the case with the voltage doubler circuit.

Pseudo-Schottky Diode

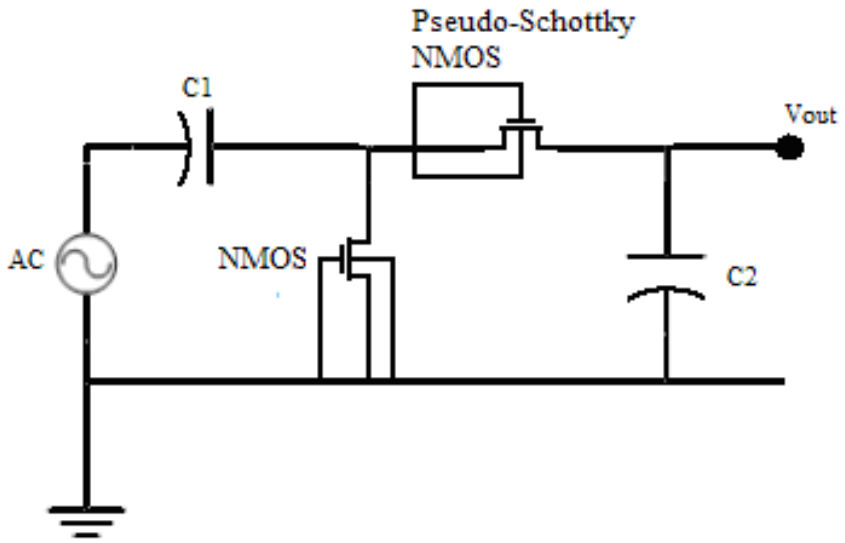


Fig. 12 Pseudo Schottky RF power harvesting circuit design.

A new approach under investigation is the use of body driven NMOS FETs to reduce threshold voltage (Fig. 12) [74]. These devices are sometimes referred to as Pseudo-Schottky diodes. The Pseudo-Schottky diode is an NMOS diode with the body connected to the gate. Such a device does reduce the body effect and thereby increase efficiency. However, since one of the MOSFET bulk terminals is connected to ground and one terminal is connected to a voltage other than ground, isolation must be provided between bulk terminals. This can be achieved by using a CMOS process with an n doped substrate and placing the NMOS devices in p doped wells. However, given that the body of the Pseudo-Schottky diode is driven by an RF signal, such a device would result in lost efficiency due to excess capacitance between the n doped bulk and p doped well. Another alternative is to use a silicon-on-insulator process.

However, such processes are not as well characterized as bulk CMOS processes resulting in longer development times and added expense.

Voltage Doubler Stacking

These circuits can be stacked to repeatedly double the initial input peak AC voltage (minus any parasitic losses) to achieve the desired output voltage. Fig. 13 shows a chain of four of these circuits stacked together.

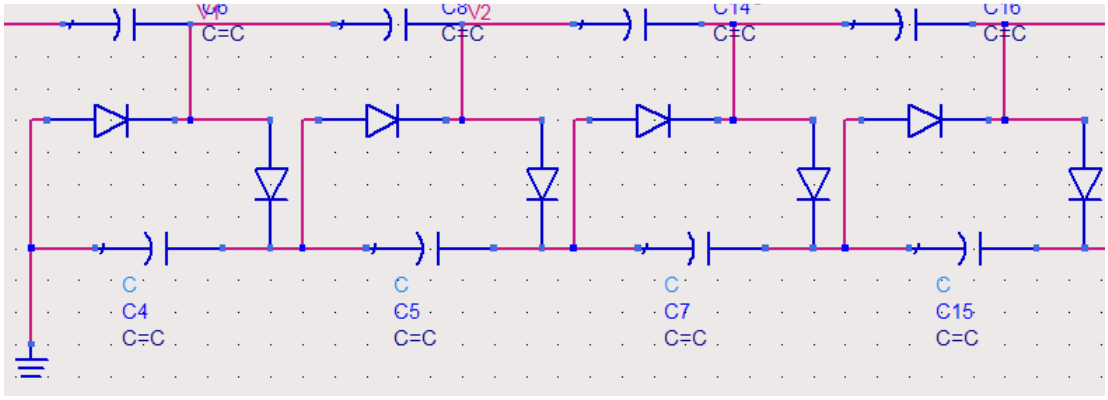


Fig. 13 Stacked stages of voltage doubler circuits.

Yao et al. proposes a treatment of the voltage doubler for determining the output voltage of the voltage doubling circuit [69]. Through recursion, the voltage at the output of a stacked voltage doubling circuit consisting of n stages is defined as:

$$V_n = 2 \cdot n \cdot (V_i - V_d)$$

Eqn. 20. Output voltage at nth stage of stacked voltage doublers.

Where V_i is the voltage incident at the input of the first voltage doubler stage and V_d is the threshold voltage of the diode or diode connected MOSFET. Harrist proposes an alternative treatment that defines output voltage as a function of the DC output voltage and internal resistance of a single voltage doubler stage [67]. Under this treatment, V_{out} for an n stage voltage doubler is defined as:

$$V_{out} = \frac{n \cdot V_0}{n \cdot R_0 + R_L} \cdot R_L = V_0 \frac{1}{\frac{R_0}{R_L} + \frac{1}{n}}$$

Eqn. 21. Output voltage of stacked voltage doublers as a function of the output voltage from a single stage with an open load, the load resistance, and the internal DC resistance of the diode.

Where R_L is the load impedance, R_0 is the internal DC resistance and V_0 is open load voltage of the output of the voltage doubler. A central figure of merit for power harvesting circuits is the ability to convert input power to an output voltage. Neither treatment models this effect. Thus, a more comprehensive analysis is desirable.

Conclusions

Given the limitations of the prior works of research to properly address the design challenges in providing sufficient lifetimes and performance for Smartdust sensor networks, the purpose of this research is to design, fabricate and test a novel low power receiver for use in a Smartdust transceiver. Among the performance goals of the Smartdust receiver are to demonstrate adequate sensitivity for reliable transmission over 10 m from a 1 mW source in poor propagation environments (close

to ground plane, walls, etc.), a receiver power draw on the order of 1 mW, and integration directly onto CMOS without any external passives. Towards this goal, several techniques and novel ideas are proposed for improving sensitivity. Among them is the use of a RF power harvesting circuit for demodulation and development of an analytical methodology for optimizing a multistage LNA to meet sensitivity requirements at minimal power draw. In addition several other benefits of the proposed ideas will be explored including Automatic Gain Control (AGC) and increased RF pass band filtering.

In an effort to further extend out the lifetime of the Smartdust transceiver, RF power harvesting is explored as a power source. Work by Roundy et al. has reported that there is not enough ambient RF energy in the environment to effectively act as a power source for wireless sensor networks [37]. This work seeks to disprove the conclusion of Roundy et al. through a careful survey of the RF energy in the environment and through the application of novel improvements to RF power harvesting circuits that will improve RF power harvesting efficiency over what has previously been reported in the literature. To better understand the performance limitations of power harvesting circuitry, an analytical model is developed by which the dominant parasitics can be identified under various regimes of operation. The goal of this work is to generate sufficient voltage to drive analog and digital electronics (> 1 V) from RF energy levels that can be detected from RF sources such as cell towers. This is in contrast to previous works that have required close proximity to an RF energy source (<15 m).

Chapter 2: Survey of Ambient RF Energy Sources

Introduction

RF wireless electronics play a crucial role in collecting and relaying information in modern society. To support the wireless transfer of data, an extensive wireless infrastructure has been established across the country. Examples of this infrastructure range from the radio and television networks established in the 1920's and 1940's respectively [75] to the more recently established GSM and CDMAone cellular networks.

As a result of wireless networks, significant RF energy can be detected in the environment. Even at a kilometer away from an FM radio tower, indoor power densities better than .5 uW/cm^2 can be detected [64]. Comparable power densities can be detected at higher frequencies both domestically and internationally [65][66] including the cellular bands near 900 MHz.

Through efficient conversion of this RF energy to DC power, the wireless infrastructure could serve not only as a communication source, but also as a source of power. This power source would require no physical tether to utilize. In addition, the cost of utilizing this source of power represents no additional cost to the wireless network providers, as RF power harvesting effectively reclaims RF power that would be absorbed by the environment.

The major reluctance in implementing RF energy scavenging from the wireless infrastructure is whether sufficient RF power to operate portable electronics can reliably be received. This work seeks to answer that question through an examination of the amount of RF energy present in the environment.

Survey Methodology

The goal of this research is to perform a comprehensive survey of ambient RF energy in the environment due to cellular and UHF TV band emissions. This work studies the RF energy present in the urban and suburban environments (as opposed to rural areas), because of the abundance of RF wireless sources present to facilitate communications for the higher population densities characteristic of these areas. This work will be used to better predict the RF energy levels that can be expected in urban and suburban areas from RF energy sources common in the environment.

The survey methodology was divided into a spatial and time domain survey. The spatial survey was conducted by driving through various urban and suburban areas recording periodic samples of the received RF signal strength from a ¼ whip antenna. The origin of the survey measurements was identified as urban or suburban to indicate the effect of population density on RF energy levels.

Urban areas are defined as areas characterized by dense population and large commercial development. Environmental features are characterized by roads

typically laid out in a grid structure between large multi-story buildings. Urban areas are located in areas that have been incorporated as a city and represent focal points of trade and commerce for the region [76].

Suburbs are commonly defined as residential areas near a city or large town. Suburbs are characterized as a collage of large residential zones consisting of single family homes or multifamily dwellings and commercial zones primarily consisting of single story buildings [77].

In addition, measurements in suburban areas were subdivided into five additional categories to compare the effect of different districting types, commercial densities, and road types on expected RF energy levels.

Highway - *Highways are major multi-lane roads with controlled access for entering and exiting traffic. Highways often pass through both commercial and non-commercial zones [78]*.

Commercial Road - *Commercials Roads are characterized as roads populated by retail stores including strip malls, shopping malls, chain restaurants, and retail parks. These areas are characterized by retail buildings and automobile parking [79]*.

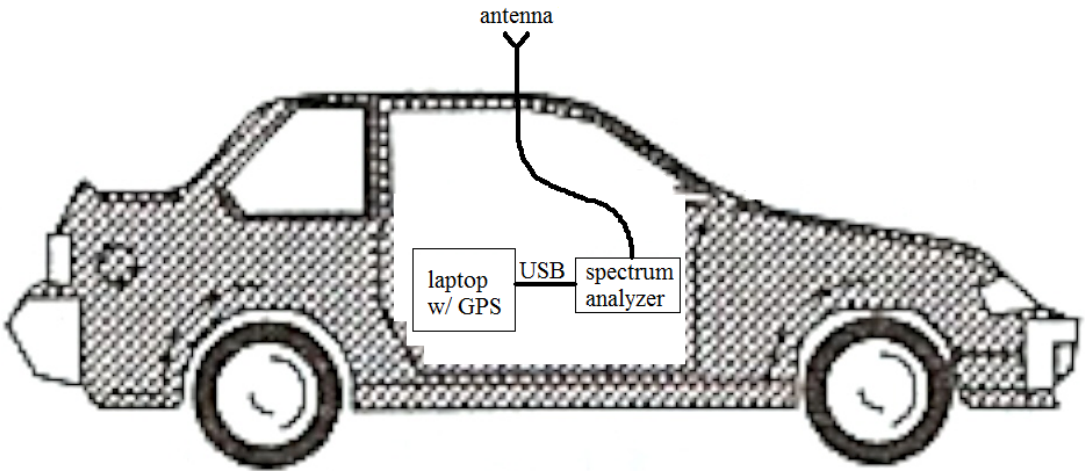
Non-Commercial Road - *Non-commercial roads are characterized by the absence of commercial or residential buildings. They are often smaller roads that provide access between commercial and residential areas along paths of lighter traffic density.*

Residential - *Residential areas consist of small plots of land populated by single family or multi-family homes, or larger plots of land populated by apartment buildings with residual parking lots in between them. Some subdivisions are isolated form retails areas, offices and other subdivisions by artificial walls and natural barriers. Most subdivisions are surrounded on all sides by large, multi lane roads to handle large concentrations of traffic due to the lack of through streets inside the subdivision itself [80].*

Campus - *Campus designs are common for public buildings and consist of complexes of two or more religious, commercial, industrial, governmental, or educational buildings grouped on a plot of land. Instead of the traditional front yard and backyard design, the land area is laid out in a more complex system of spaces between buildings. The spaces between buildings often consist of courtyards and quadrangles. Colleges are typically laid out in a campus arrangement [81].*

The survey required the ability to log both absolute position and record RF energy levels at regular intervals. To meet this requirement the RF measurement system depicted in Fig. 14 was designed.

(a)



(b)

Fig. 14 Photo of RF energy survey system (a) and illustration of a car mounted survey system (b).

The system consisted of a ruggedized laptop with built in GPS and an Agilent Technologies N9340A Handheld Spectrum Analyzer connected to a RE1903U-SM magnetic mount omni-directional antenna. MATLAB scripting was executed on the laptop utilizing the Instrument Control Toolbox to remotely interrogate the handheld spectrum analyzer through a USB port and laptop GPS through a serial port. The Instrument Control Toolbox provides access to USB and serial ports through the VISA IO standard. A VISA device driver provides a generic interface by which MATLAB can communicate with various IO devices including USB and serial ports.

For surveys of spatial fluctuations in received RF energy, the position and signal strength of the six strongest signal peaks was averaged over two samples and recorded on the spectrum analyzer every six seconds. Signal peaks were identified by remotely triggering a marker peak search on the spectrum analyzer remotely from the MATLAB script running on the laptop. Each RF measurement was associated with a spatial position measurement obtained through serial interrogation of the internal GPS in the laptop. The GPS data acquired from the laptop is presented in the industry standard NMEA format. When measuring fluctuations in received RF signal strength over time, time stamp data was logged in addition to the position, strength and frequency of RF measurements. The full set of data was saved to a tab delimited ASCII text file. In addition, for spatial surveys of RF energy the data was saved to a KML script with color coded pictorial representation of signal strength for easy import into Google Earth. An illustration of the algorithm implemented by the

MATLAB code to acquire spatial and temporal data is presented in Fig. 15, and the full code utilized to acquire and process data is presented in Appendix B.

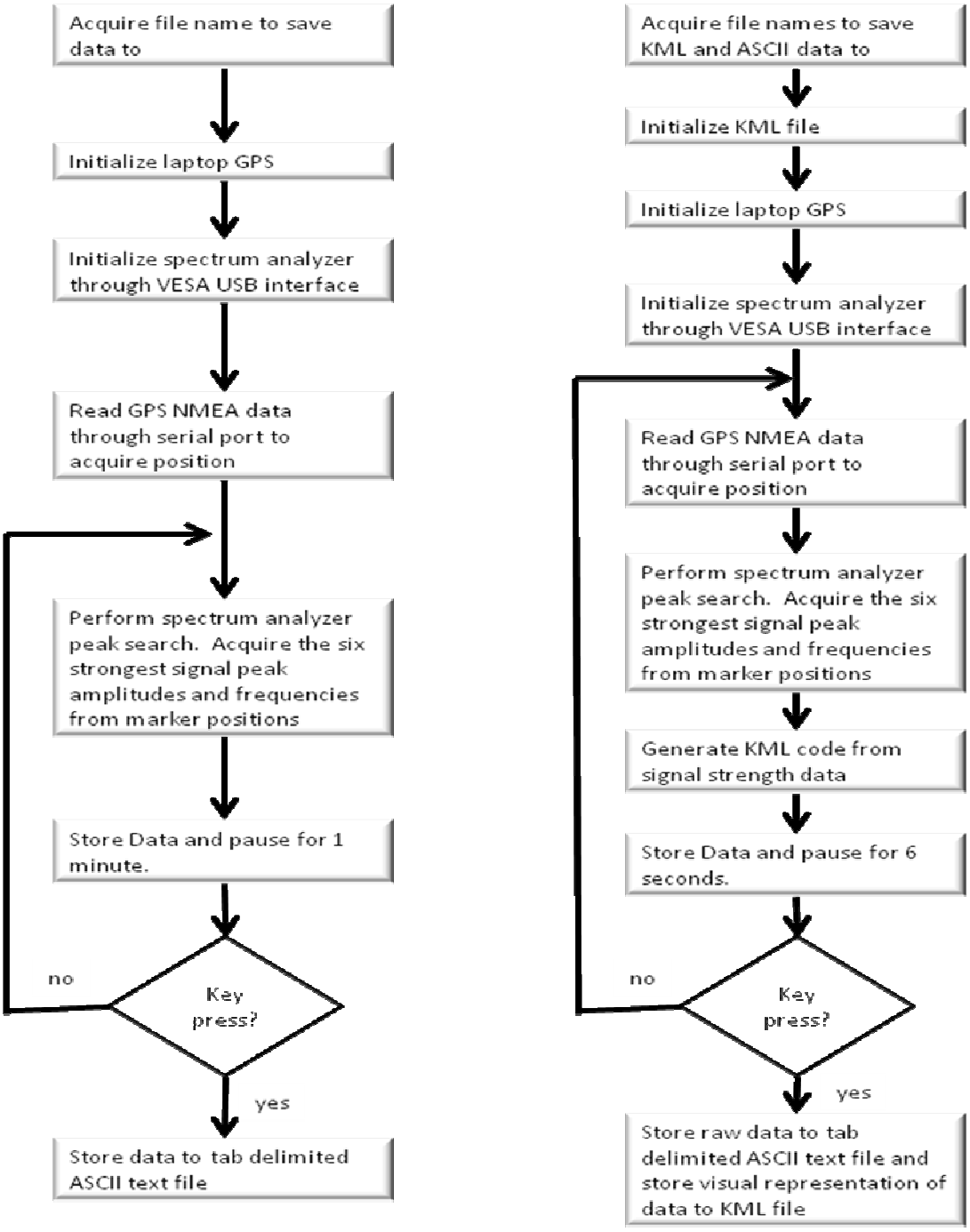


Fig. 15 Algorithm utilized in monitoring temporal fluctuations in received RF energy (a) and spatial fluctuations in received RF energy (b).

The RF energy survey targeted RF frequency bands commonly utilized throughout the country. The UHF TV band located between 470 and 806 MHz and the cellular CDMAone/GSM bands located in the frequency bands of 824-849 MHz, 869-894 MHz, 896-901 MHz, and 935-940 MHz are utilized in communications infrastructure where very broad coverage is required. This coverage is achieved for the UHF TV band through a high power source (up to 1 MW) centralized to one tower. These systems utilize one tower to cover areas greater than 50 miles [82]. Cellular systems, on the other hand, utilize many lower power (< 500 W) broadcast towers to cover an area. The area that each cellular tower covers varies greatly, but is typically limited to a few miles [83]. Thus, given the wide coverage of the UHF TV and cellular bands, the RF frequency band between 500 MHz and 1 GHz was monitored. This range was large enough to sample the RF bands of interest, but small enough to allow a new sample every six seconds.

The antenna used for measurement was the RE1903U-SM 900/1800/1900 MHz tri-band 3 dBi magnetic mount omni-directional antenna. To calibrate the antenna measurements to a 0 dBi monopole, the signal strength received by the antenna from a known power source was measured from 100 MHz to 2.5 GHz over a known distance of 1.25 meters. The gain of the antenna could then be calculated from Eqn. 22 [84].

$$G_{antenna} = \frac{P_{received} - P_{transmited} + 20 \cdot \log_{10}\left(\frac{4 \cdot \pi \cdot d}{\lambda}\right)}{2}$$

Eqn. 22. Gain as determined from two matching antennas place a distance d from each other.

Fig. 16 presents the resulting gain as a function of frequency for the collection antenna.

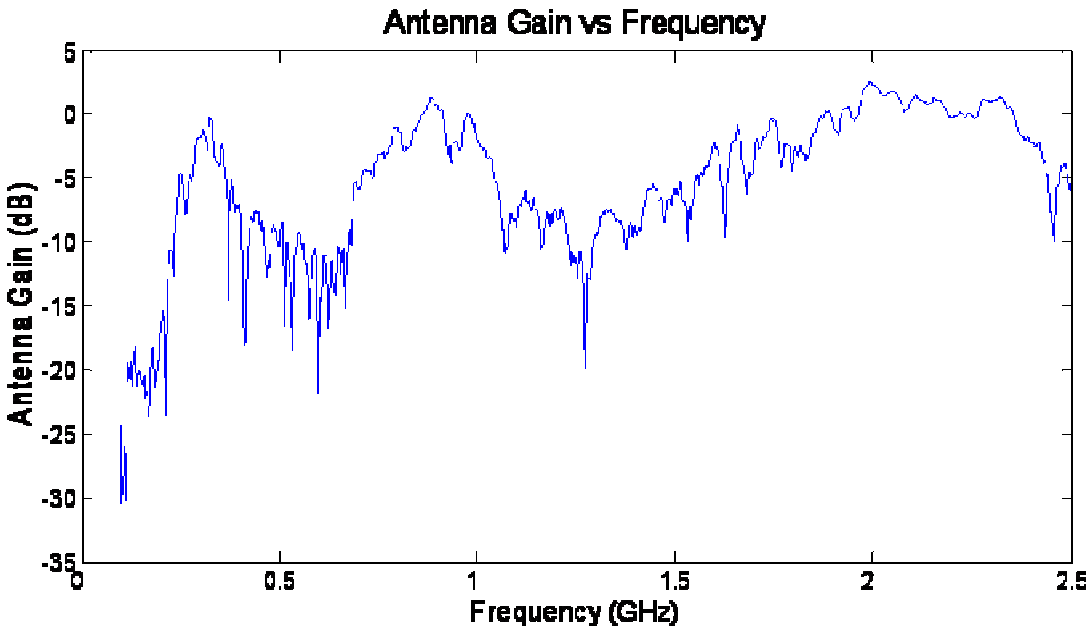


Fig. 16 Antenna gain of RE1903U anetnna versus frequency.

By subtracting the antenna gain from the measured signal strength, the received signal incident on a 0 dBi monopole could be calculated. The lowest antenna gain detected in the survey range (500 MHz to 1GHz) was about -21 dBm. Therefore the scope sample bandwidth was set to enable a scope sensitivity of -85 dBm. This enables a measurement sensitivity of -65 dBm after calibrating to the theoretical unity gain monopole antenna.

Spatial Survey Measurements

A spatial survey was conducted of the RF energy levels present in the environment. The test was conducted between the hours of 9 am to 4 pm on weekdays between the dates of April 15th, 2008 and June 15th, 2008 in the greater Baltimore-Washington area. The survey was conducted in both urban and suburban environments allowing for analysis on the effect of population density and land use on expected RF signal strength.

Suburban

Measurements for RF energy levels present in suburban areas were carried out in the I-295/95 corridor between Baltimore, Maryland and Washington, D.C. As described in the previous section on survey methodology, measurements were taken in a variety of settings ranging from residential and campus areas to commercial roads and highways. Received RF power was normalized to the unity gain monopole antenna and then converted to KML format with RF strength indicated by color coded circles at measurement locations. Fig. 17 and Fig. 18 give example images of RF signal strength measurements in suburban settings.

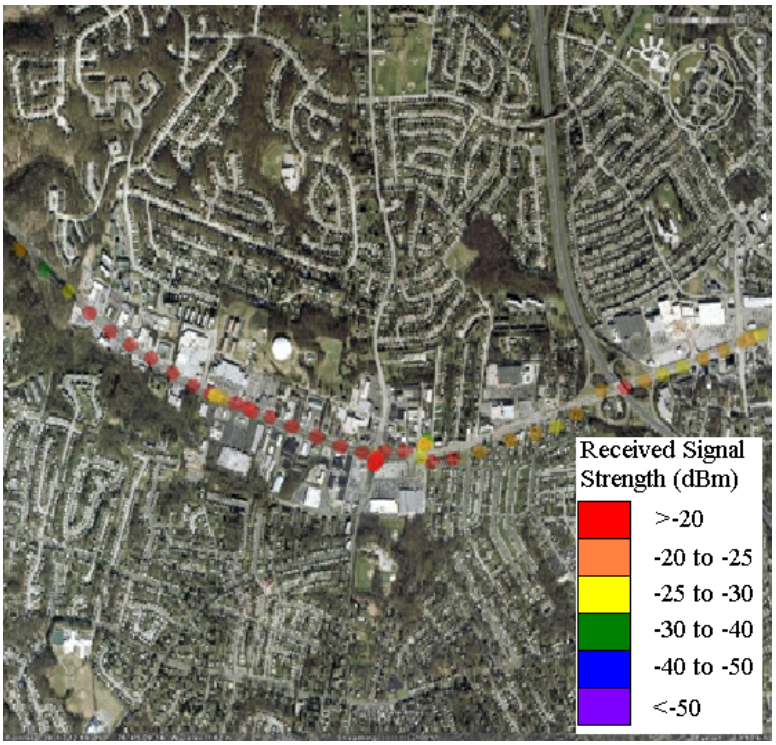


Fig. 17 Overhead views of RF signal strength for commercial area.

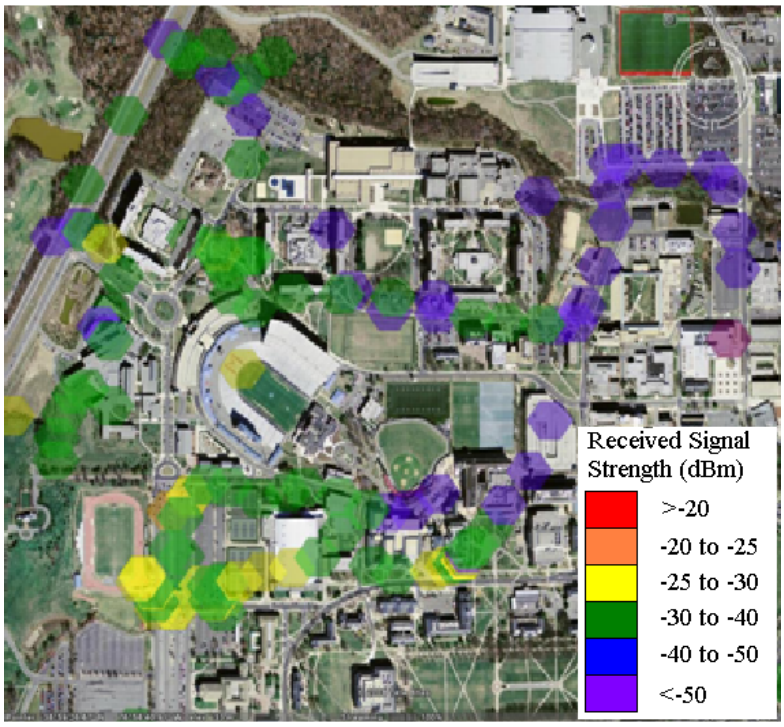


Fig. 18 Overhead views of RF signal strength for campus area.

The first metric by which the suburban areas was evaluated by was the peak RF signal strength detected during the survey.

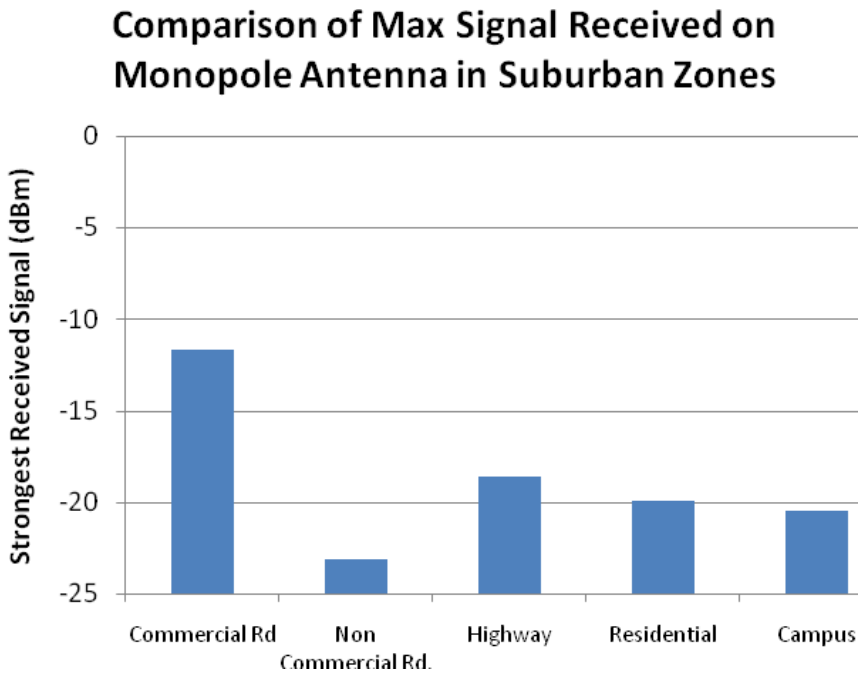


Fig. 19 Peak RF signal strength received by survey system for each suburban landscape type.

As indicated by Fig. 19, RF energy levels as high as -11.7 dBm can be detected on the commercial roadways of the suburban environment by a monopole antenna. The peak signal levels detected in the other four regions were not quite as high but still represented significant energy levels at ~-20 dBm. Even in the absence of antenna gain, this represents tens of microwatts of available RF energy.

To better understand the likely hood of receiving such strong RF levels, distribution curves of the RF power received by the strongest RF source (narrowband) were plotted in Fig. 20.

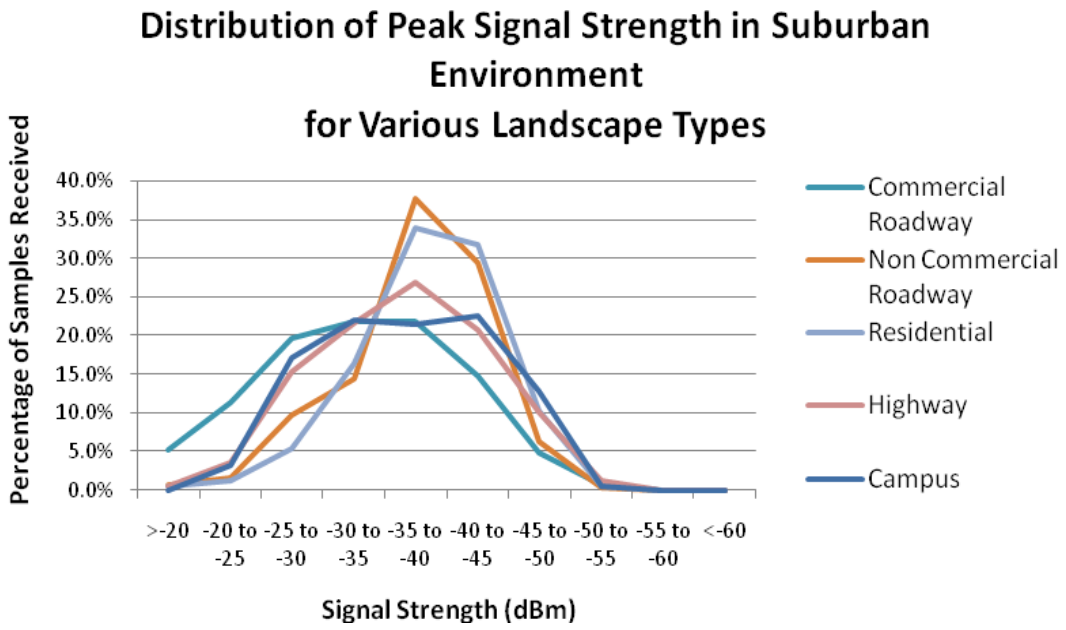


Fig. 20 Distribution of peak RF signal strength received by survey system for each suburban landscape type.

Fig. 20 shows that strong peak RF levels on the order of -20 dBm or better are only available in significant quantity along commercial roadways. In the other regions, RF levels were generally limited to -25 dBm or lower. RF levels were particularly weak in residential areas and along non commercial roads with over 97% of the samples detected at RF levels of -25 dBm or less.

Broadband collection of RF energy has been proposed as a way to increase the amount of energy collected from the environment [85]. Fig. 21 presents the average increase in RF energy detected by summing the six strongest RF sources collected (broadband) collection over narrowband peak collection for each suburban setting.

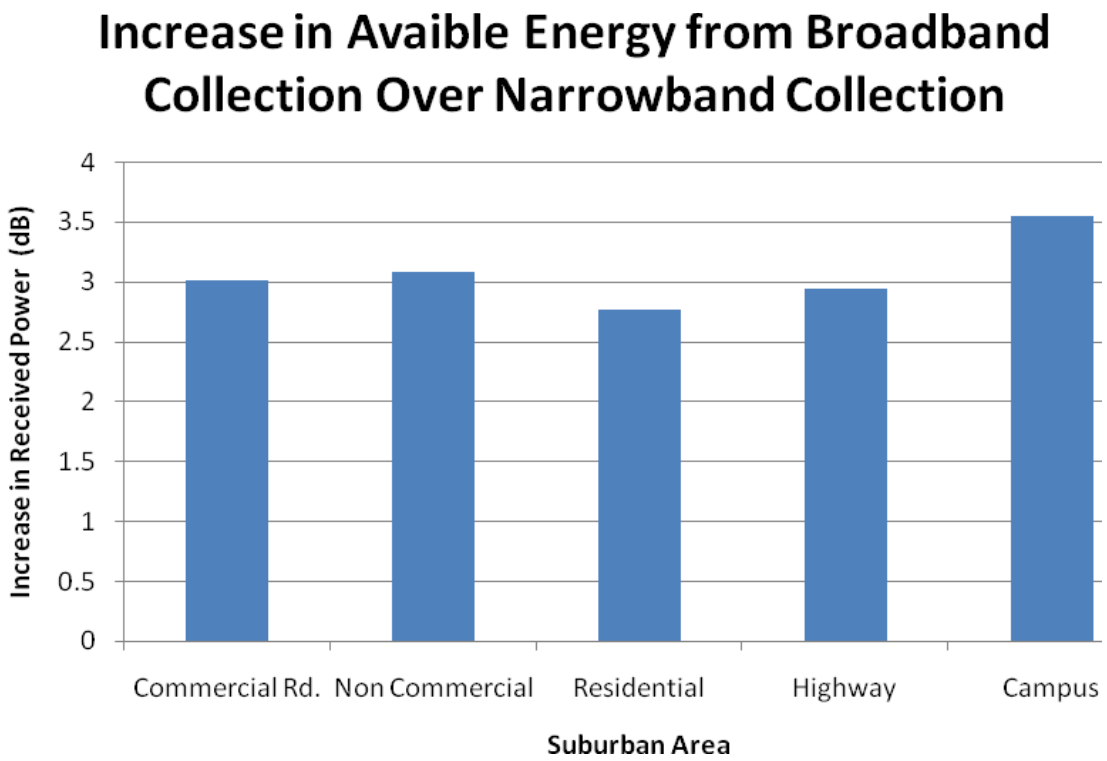


Fig. 21 Increase in avaible energy from broadband collection over narrowband collection.

This demonstrates that integration over a broad energy spectrum does increase total received RF energy. However, the increase is only about 3 dB as opposed to the order of magnitude increase one might hope for. This is a result of the large variation in the strength of RF energy received by various sources. The strongest RF signal source tends to dominate received RF energy. However, in the case of commercial roadways, this represents RF levels of -25 dBm or higher present during almost one third of the measurements (Fig. 22).

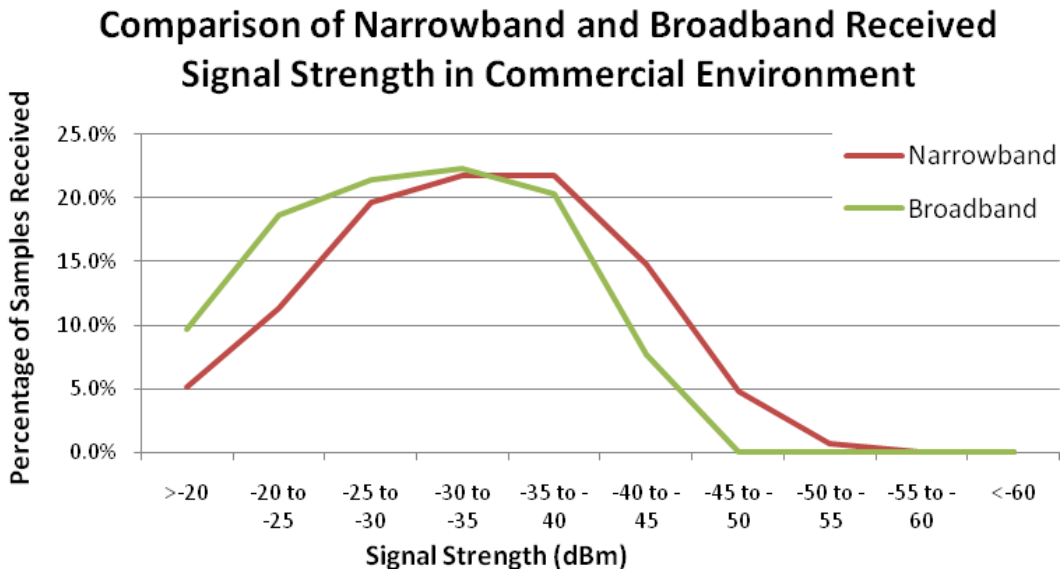


Fig. 22 Comparison of the distribution of received RF signal strength for narrowband collection and broadband collection in a commercial setting

UHF TV broadcast and cellular signals are known sources of RF power in suburban communities. The data indicates that there is significantly more power in the UHF TV band than in the cellular band in suburban areas. This result is particularly pronounced in the residential areas and non-commercial roadways and appears to be the result of poorer cellular coverage in those areas. To illustrate the difference in received energy in the UHF TV and cellular bands, Fig. 23 plots the increase in peak RF signal detected in the UHF TV band over that detected in the cellular band in each type of suburban setting.

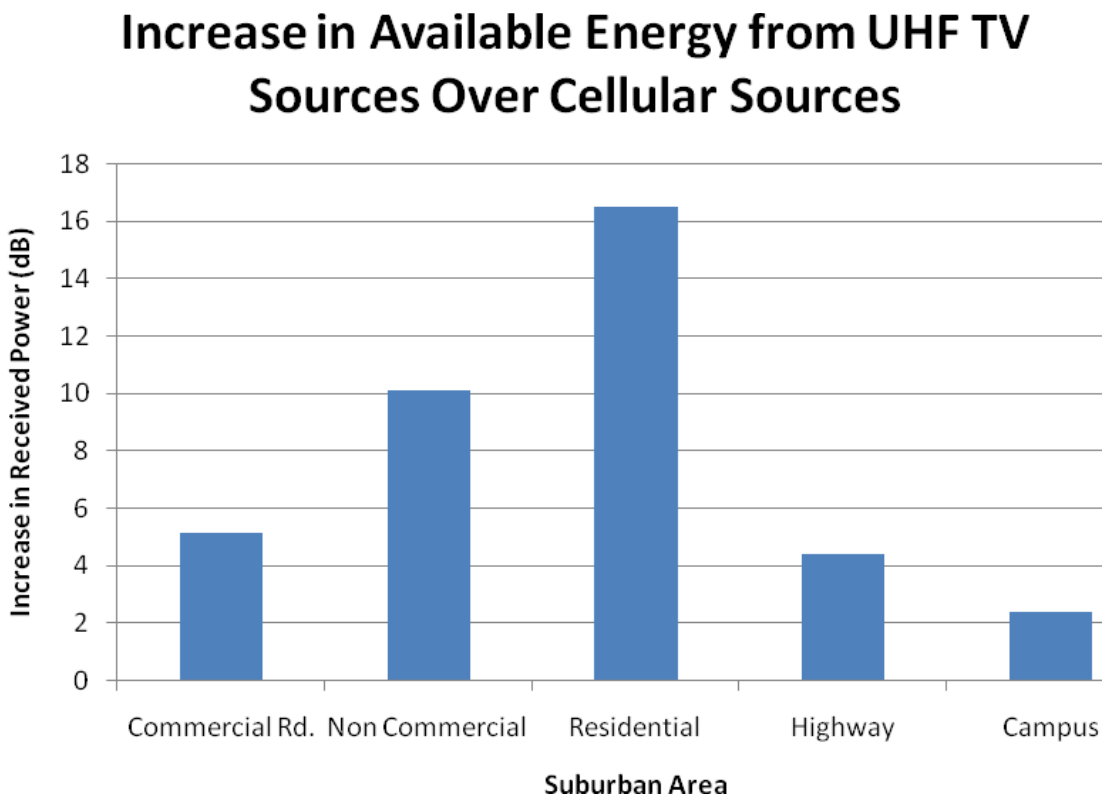


Fig. 23 Increase in received RF signal strength for UHF narrowband collection over cellular narrowband collection in a various suburban areas.

On average, over 16 dB more power was detected in the UHF TV band than in the cellular band in residential suburban settings. However, the amount of RF energy present in the UHF TV and cellular bands is more equitable in the commercial roadways, highways and campus settings. This is likely due to the increased call volume resulting from the higher population density of these areas over non commercial and residential areas. The increased demand necessitates the use of more cellular channels [86], and as a result, more RF energy is present in the environment.

In summary, a link was demonstrated between the availability of RF energy and population density. A greater average RF energy was obtainable in more densely populated areas such as campuses and commercial roadways than in the more lightly populated residential and non-commercial roadways. In addition broadband collection of RF energy showed only a limited 3 dB increase in RF energy collected. This is likely a result of the low number of carrier channels necessary to meet the call demand requirements of areas with lower population density.

Distinctions were also present in the availability of RF energy between UHF TV bands and cellular bands. The suburban environment demonstrated that RF energy present in the UHF TV band is on average stronger than that found in the cellular band. In residential and non-commercial roadways, the difference in energy available in the two bands was dramatic, resulting in up to 16 dB difference in average energy received.

Urban

The measurements for an urban environment were conducted in Baltimore, MD and in Washington, DC. As was done with the suburban measurements, the measured data normalized to the gain of a unity gain monopole antenna was saved in KML format enabling the data to be plotted using Google earth. Color coding was used to indicate RF signal strength at the indicated positions. Fig. 24 and Fig. 25 illustrate the data that was measured in both Baltimore, MD and Washington, DC.

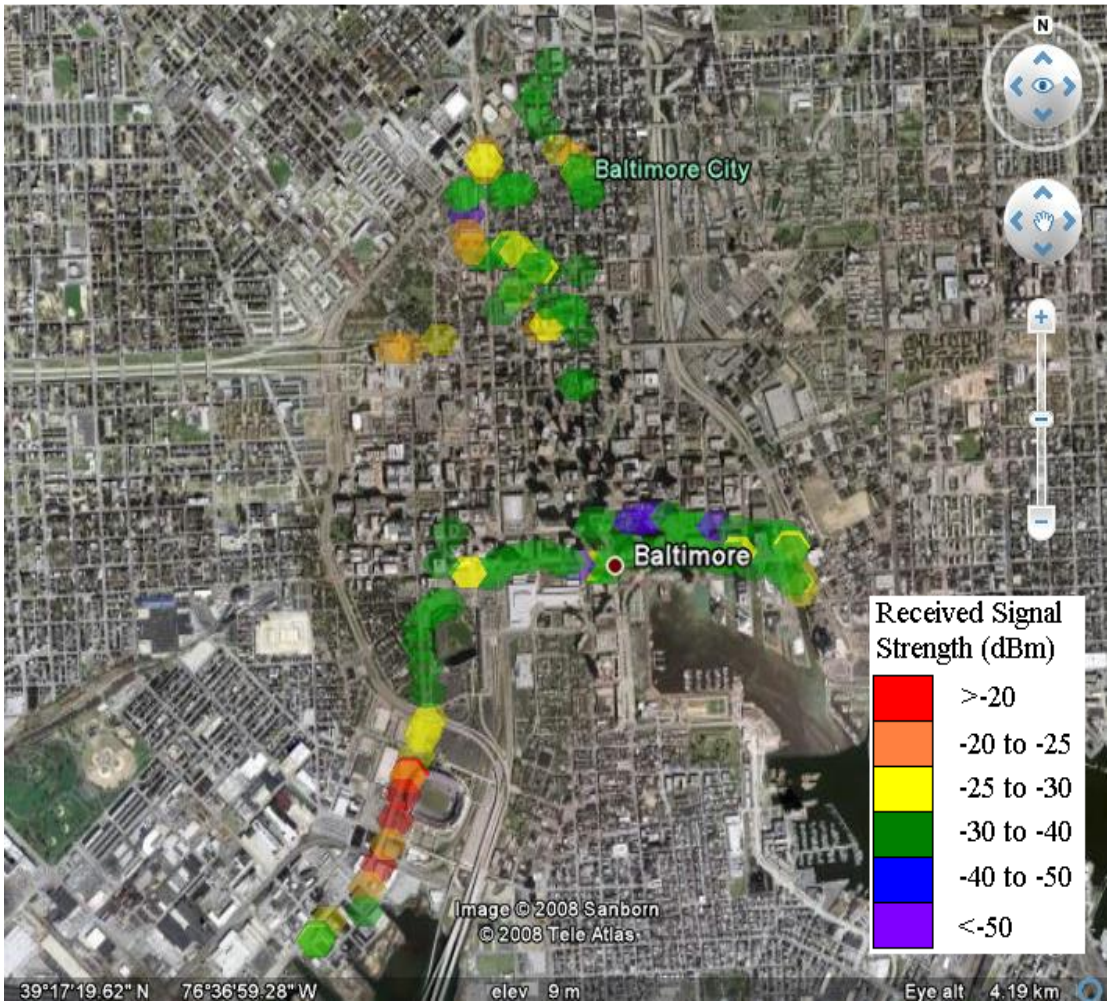


Fig. 24 Overhead view of RF energy measurements in Baltimore, MD.

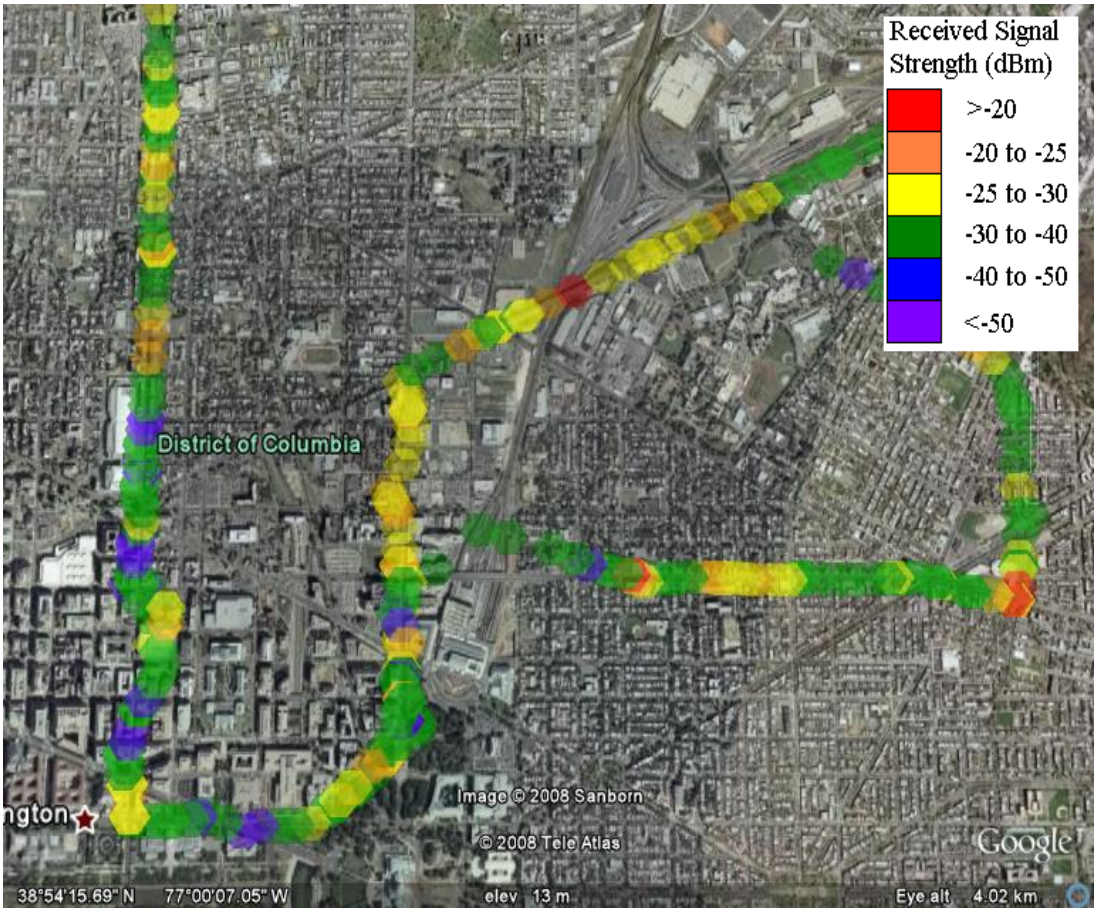


Fig. 25 Overhead view of RF energy measurements in Washington, DC.

Although the peak RF signal level measured in the urban environment of -15.2 dBm is lower than the peak signal received in the commercial area of a suburban environment, it is apparent after conducting the survey that overall the urban environments host significantly higher RF energy levels than suburban regions. This is supported in Fig. 26 which compares the distribution curves of the strongest received narrowband signal in an urban environment to the narrowband signal strength in the suburban environment.

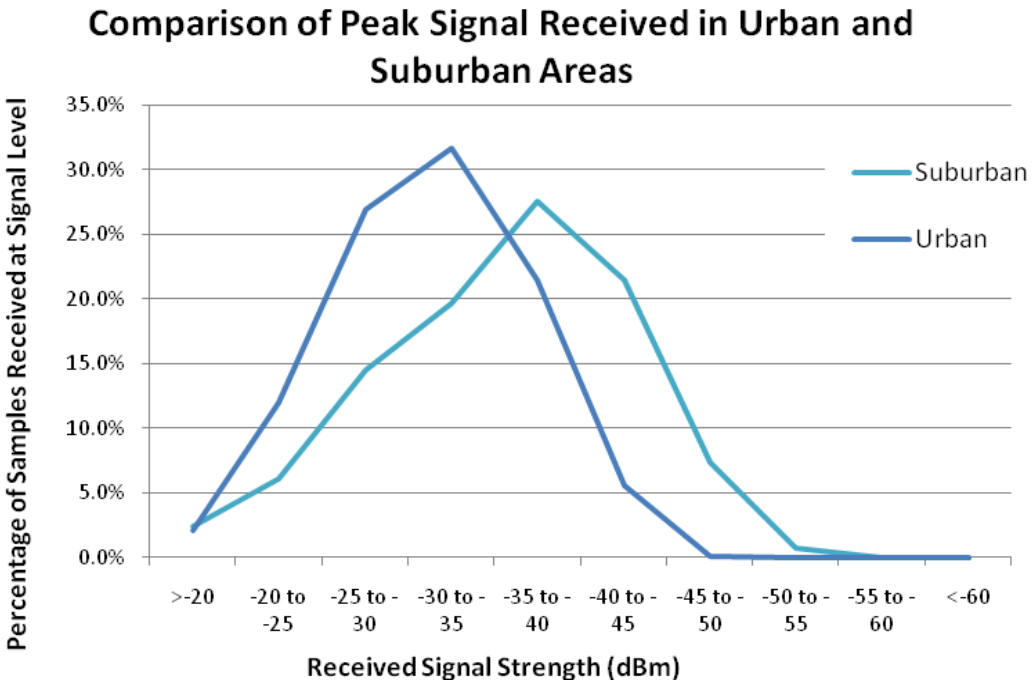


Fig. 26 Comparison of the distribution of peak received RF signal strength in an urban and suburban setting.

Urban environments have on average over 4 dB more energy than suburban environments. However, as was the case in suburban environments, broadband collection yields only about a 3 dB increase in collected RF energy. Therefore, despite the presence of more RF energy, the total energy collected is still dominated by the presence of one or two particularly strong sources in any one spot.

In suburban areas it was apparent that UHF TV was the strongest source of RF energy. However, in urban areas, the level of power available from cellular and UHF TV is considerably more equitable (Fig. 27). This would appear to be the result of much stronger cellular coverage and is likely due to the use of many cell sites within a smaller coverage range to meet call demand requirements in urban areas.

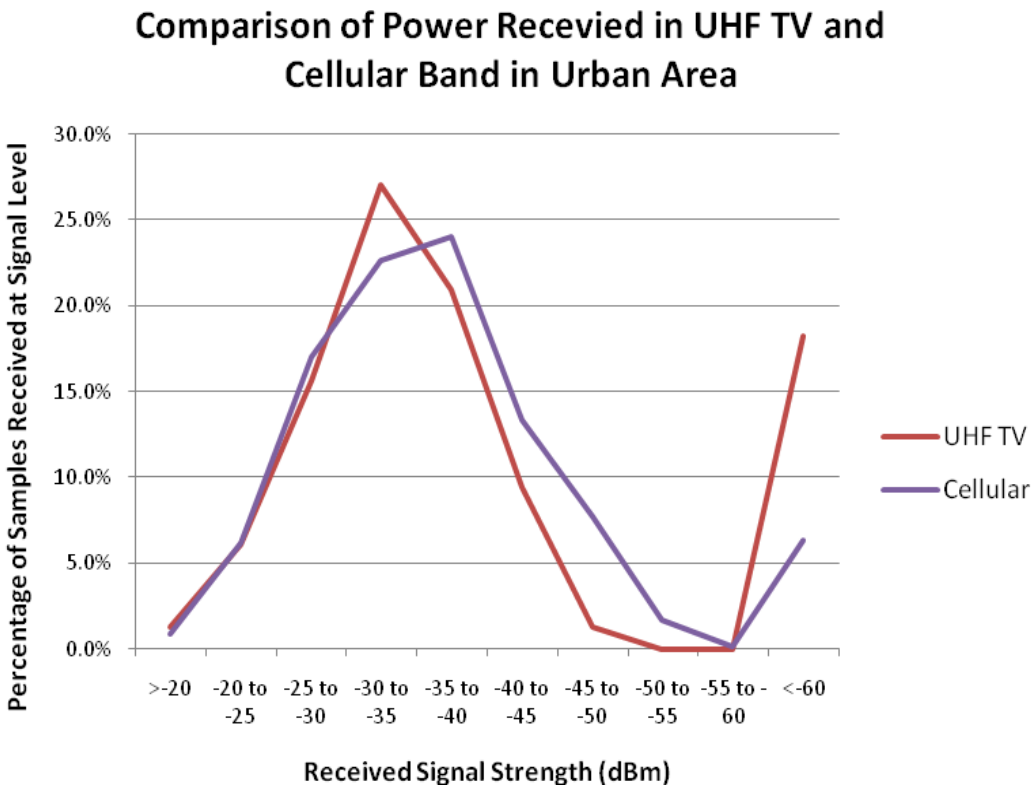


Fig. 27 Comparison of the distribution of peak received RF signal strength in the UHF and cellular bands of an urban setting.

In summary, the urban environment demonstrated more RF energy available from cellular and UHF TV sources than its suburban counterpart. RF energy was equally abundant in both the cellular and UHF bands. However, as with the suburban environment, in an urban environment the ability to conduct broadband RF energy scavenging showed only a 3 dB improvement in collected energy over the energy available from narrowband collection of the peak carrier. Thus, available RF energy in the environment in the cellular and UHF TV bands appears to be dominated by one or two strong RF sources.

Time Domain Survey Measurements

The energy received from cellular and UHF TV sources vary with time [86]. To determine the extent of this power fluctuation, the RF signal strength received at two different locations was monitored over a week long period. As was done with the spatial measurements, the frequency and amplitude of the top six RF signal levels were recorded. Samples were recorded every minute and the received signal strength was averaged over two samples. The spectrum was monitored from 50 MHz to 2.95 GHz. Both cellular and UHF band data was gathered at location 1. At location 2, while cellular data was gathered, the UHF signal was below -80 dBm and therefore no measurement was obtainable.

TABLE I STATISTICAL MEASUREMENTS OF THE RECEIVED SIGNAL STRENGTH OF CELLULAR AND UHF SIGNALS OVER TIME.

	UHF TV Location 1	Cellular Location 1	Cellular Location 2
Maximum	-21.19	-47.20	-38.37
Minimum	-32.08	-59.36	-48.83
Mean	-27.71	-56.81	-43.48
Median	-27.85	-56.90	-43.17
Standard Deviation	1.356	.878	1.528
Range	10.89	12.16	10.45

TABLE I presents a statistical summary of the data gathered. As expected, the power received varied greatly. The range over which the RF energy was received varied for both the cellular and UHF TV measurements was approximately 10 dB. This

represents a variation of up to an order of magnitude in received RF energy. Such large variation in received energy suggests that the availability of sufficient RF energy for RF energy scavenging may be intermittent. Thus energy storage will be necessary to allow the energy received to be integrated over time. This variation over time is illustrated in Fig. 28 through Fig. 31 below.

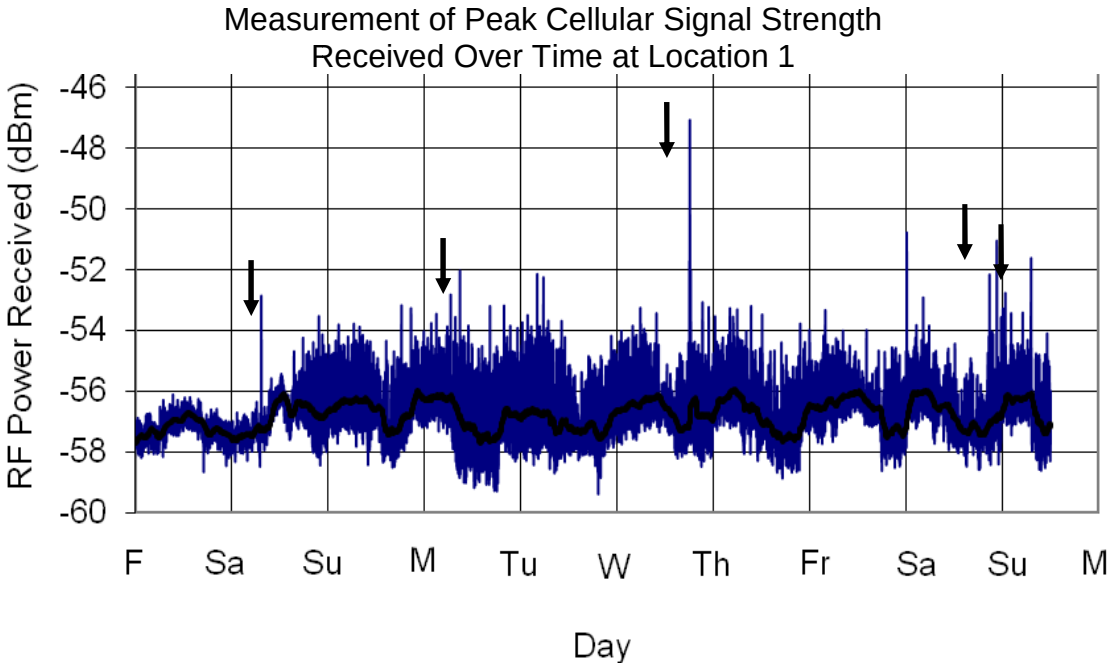


Fig. 28 Measurement of peak signal strength received over time in the cellular band at location 1.

The arrows indicated in Fig. 28 illustrate the increase in received RF emanations due to close proximity to a cellular handset engaged in an active call. This demonstrates that proximity to an active handset presents a significant but short lived source of RF energy. The RF energy received as a result of close proximity to a hand set is up to 10 dB greater than the average strength of the received signal from the cell tower.

An additional feature of interest found in Fig. 28 is that the variation in received RF energy is significantly lower during the first several days than during the following days. The first two days represent the fourth of July weekend and would suggest that major holidays represent a period of lower cell phone use and consequentially lower levels of RF energy present from cellular communications.

In addition, Fig. 28 seems to show a periodic pattern as the average amount of RF energy rises and falls during the course of each day. To better illustrate this behavior, Fig. 29 plots the received RF measurements as a function of the time of day.

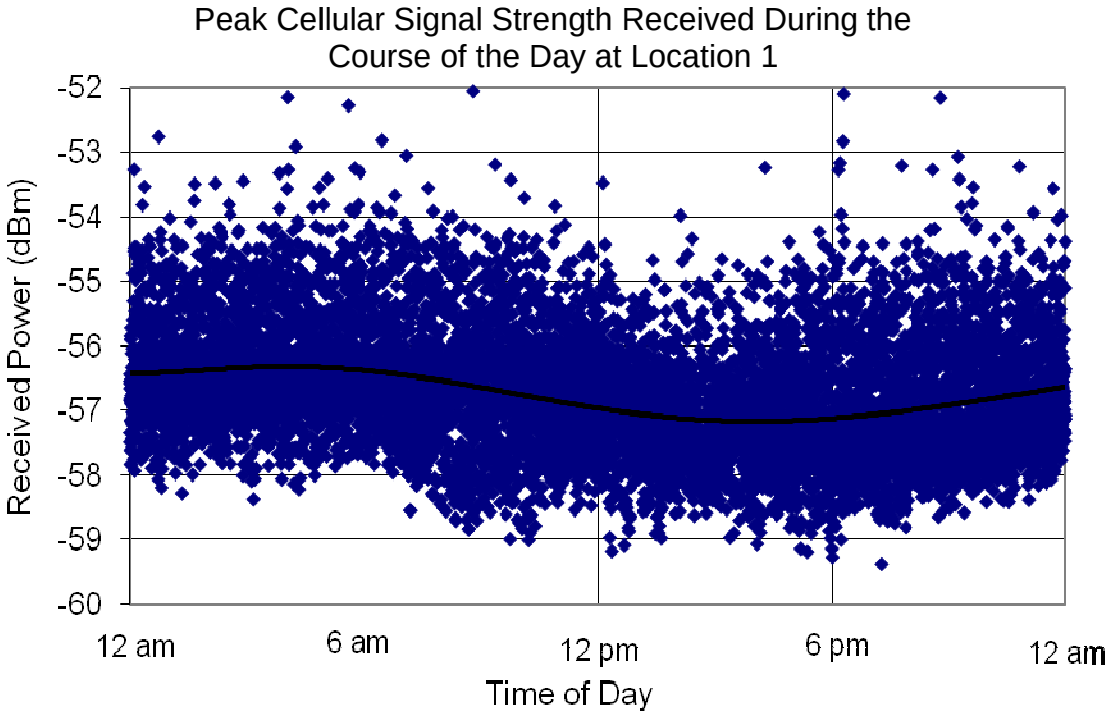


Fig. 29 Measurement of peak signal strength received over time in the cellular band at location 1 as a function of time of day.

Fig. 29 clearly indicates that on average, received RF energy is greatest during the morning period and decreases trough the afternoon until reaching a minimum during the early evening. However, the periodic nature of the received RF energy from a cell tower during the course of a day results in less than a 1 dB variation in average received RF energy.

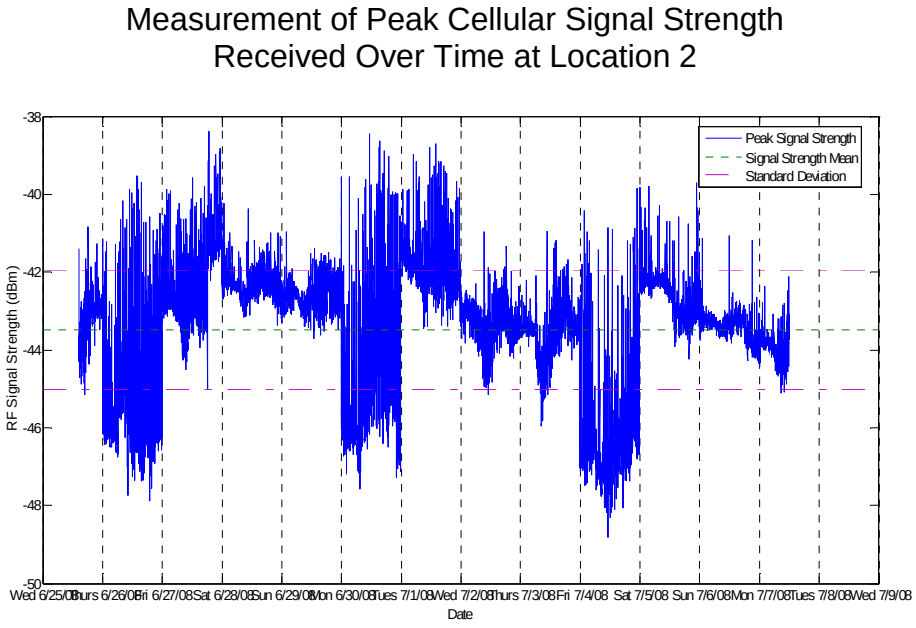


Fig. 30 Measurement of peak signal strength received over time in the cellular band at location 2.

Like the measurements of received RF signal strength in the cellular band in Fig. 28, Fig. 30 clearly indicates a periodic structure in transmitted RF energy by the cell tower near location 2. However, unlike the measurements in Fig. 28, the periodic structure in RF energy manifests itself as a reduction in minimum RF energy received by the cell tower for 24 hours every fourth day. The RF energy clearly drops at midnight before returning to normal levels 24 hours later. This behavior appears to

be intended by the operators of the monitored cell tower. However, during these periods of low minimum power, peak signal levels comparable to that detected during periods of higher minimum power were still detected.

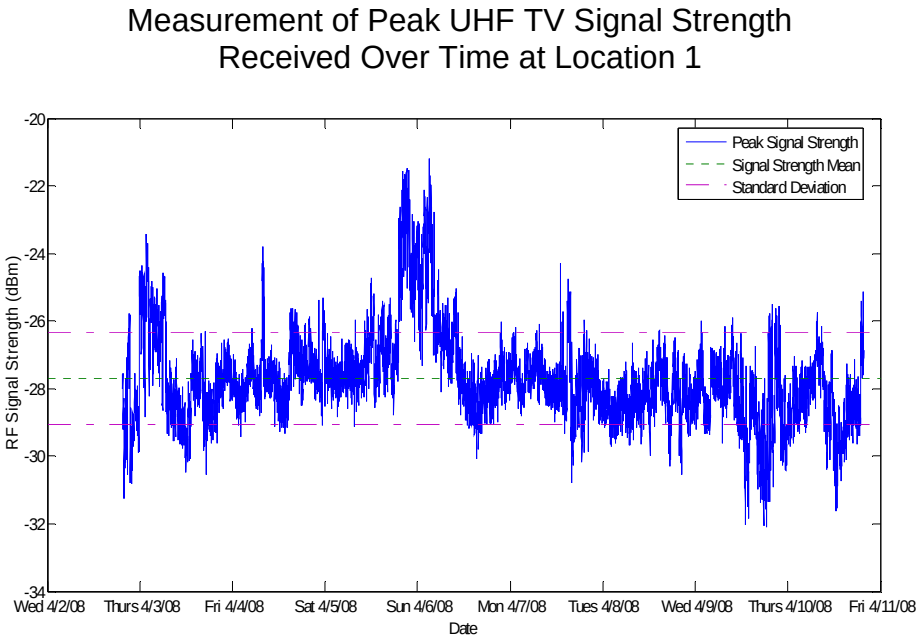


Fig. 31 Measurement of peak signal strength received over time in the UHF TV band at location 1.

The received RF signal strength from the UHF TV tower near location 1 showed no periodic structure as indicated in Fig. 31. Significant variations in received RF energy did occur as illustrated by the rise in RF energy received on 4/6/08. Given that UHF TV does not implement power management, these variations in signal strength are likely the result of environmental conditions.

In summary, fluctuations in received RF energy of up to 10 dB were observed during the measurement period. In addition, close proximity to active cellular handsets

represents an increase of up to 10 dB over the average power available from the cell tower, but is available for only brief durations (minutes). A periodic structure in the received RF energy received from a cell tower was observed at two measurement locations while the received RF energy from UHF TV transmissions demonstrated no periodic structure. This suggests that daily variations in network demand and power management techniques implemented by cellular systems have a modest but predictable impact on the average RF energy levels detected in the environment.

Conclusions

The RF energy survey presented in this work represents a major investment in time with over thirty thousand samples collected and two hundred miles driven over a two month period. This data provides a tool by which the probability of receiving a given RF power level can be predicted under a variety or suburban and urban landscapes. In addition, time domain analysis has resulted in a clearer picture of how signal power received from both UHF TV and cellular sources can fluctuate with time.

The strongest signal measured during the course of this work was -11.7 dBm, supporting the result of prior works that RF energy levels as high as -12 dBm can be detected in the environment from UHF and cellular sources. In addition, by examining the distribution of energy levels present in the environment, this work reveals that RF signal levels on the order of -20 dBm are consistently detected in

close proximity (< 200 meters) to cell towers and are encountered about five to ten percent of the time during travel in urban and commercial areas.

In addition, this work has revealed some of the properties and characteristics of RF energy present in the environment from cellular and suburban sources including:

1. RF energy levels are on average higher in urban areas than suburban areas.
2. Cellular towers are typically placed at the intersections of major roads resulting in stronger RF energy levels.
3. RF energy present in the environment from UHF TV signals is on average stronger than that of cellular signals in suburban areas.
4. In urban areas, power present form UHF TV and cellular communications are comparable.
5. Over time, signal levels received from both UHF TV and cellular communications vary by an order of magnitude or greater.
6. Close proximity to cellular handsets presents opportunities for significant increases in RF energy received over short durations.
7. Holidays can significantly affect the peak available RF energy from cellular networks.
8. Fluctuations in the demand for cellular networks over the course of a day result in a modest periodic change in average received RF energy.

9. Power management techniques implemented by cellular providers can result in periodic variation over the course of several days in expected received RF energy from a cell tower.
10. Broadband collection of RF energy represents, on average, a 3 dB increase in received RF energy over narrowband reception.

The RF to DC conversion efficiency of RF energy scavenging systems is highly dependent upon the power of the RF signal received. By gathering expected signal strength data over time and for various landscapes, this work presents the necessary information by which the ability of past, current, and future research in RF energy scavenging systems to provide efficient conversion of RF to DC power can be measured. Thus, the suitability of an RF energy scavenging technology for a given deployment can be more effectively predicted.

Chapter 3: Modeling the Power Matched Villard Voltage Doubler

Introduction

A common approach to RF energy scavenging employs the power matched Villard voltage doubler circuit. In solid state circuits, the diodes used for rectification are typically replaced with diode connected MOSFETs. This approach facilitates the integration of these circuits directly onto CMOS by using diode structures that are easily realized on most CMOS processes. The difficulty in the design of Villard voltage doublers that employ diode connected MOSFETs is that of determining proper sizing for the MOS transistors.

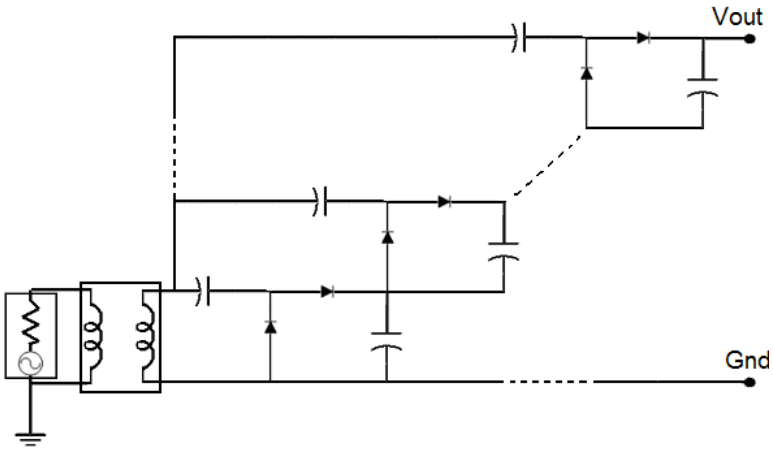


Fig. 32 Illustration of a cascaded multi-stage Villard voltage doubler.

The core cell of the Villard voltage doubler can be stacked sequentially to repeat the doubling effect of the input voltage (Fig. 32). Several systems have demonstrated this technique to good effect and realized improved RF to DC conversion efficiency at lower input power levels [67],[69]. However, as is the case with transistor sizing,

determining the number of stages for optimal RF to DC conversion presents a challenging problem in the design of multi-stage Villard voltage doubler systems.

The most common technique used to optimize transistor sizing and the number of stages in Villard voltage doubler system is an iterative approach that relies on harmonic balance or time domain circuit simulations. This approach is both time consuming, difficult to optimize for multiple design variables, and fails to provide a tool by which the effects of device parasitics can easily be explored.

An alternative solution is to develop an analytical model by which the relevant system variables including transistor size, number of stacked stages, and threshold voltage for an energy scavenging circuit can be optimized. Previous works in modeling RF energy scavenging circuits predict performance over a fairly narrow region of operation and often fail to analytically relate the physical design parameters (transistor width, number of cascaded stages, parasitics) to the performance of the circuit [69],[68]. These restrictions limit their suitability for performing design optimizations of the Villard voltage doubler circuit.

This work expands upon these previous works through the development of a model of the Villard voltage doubler that is derived directly from its physical realization and design parameters. This model provides a unique tool to examine the complete design space of the Villard voltage doubler and quickly determine the single most efficient design to meet the output voltage and load requirements at the minimum

possible input RF power. In addition, this model allows identification of the fundamental limits of RF to DC conversion efficiency as circuit parameters are changed and parasitics are added or removed.

Design Methodology

TABLE II MODEL PARAMETERS

Process Variables	
V_{th}	MOSFET threshold voltage
W_{single}	Width of a single finger of the MOSFET gate
L_{eff}	Effective length of MOSFET gate
n	MOSFET capacitance ratio
V_t	Thermal voltage
FC	Forward-bias depletion capacitance coefficient
M	Bottom junction capacitance grading coefficient
E_{ox}	Permittivity of gate oxide
T_{ox}	MOSFET gate oxide thickness
R_{res}	Sheet resistance of MOSFET gate
n_f	Number of fingers for MOSFET gate
I_{vth}	drain-source current at threshold voltage
R_s	Contact and metal resistance of gate
$C_{j,area}$	Depletion region capacitance per unit area
$C_{j,per}$	Depletion region capacitance per unit length
γ	Channel length modulation parameter
u_n	Mobility
R_{sx}	Source resistance due to velocity saturation
Y	Junction potential
A_{junc}	Area of PN junction
P_{junc}	Perimeter of PN junction
Circuit Variables	
V_{out},V_{inc}	input AC voltage or DC output voltage
f	RF frequency
R_{out}	Impedance of output load
n_s	number of stacked voltage doubler stages
Dependant Variables	
C_{ox}	E_{ox}/T_{ox}
K	$(u_n*Cox*W_{eff}/L_{eff})/2$;
W_{eff}	n_f*W_{single}

The development of an analytical methodology for solving the power matched Villard voltage doubler begins with the derivation of an analytical model for the diode. The variables necessary for this model are presented under process variables in TABLE II. This diode model is used to determine the performance of the rectifying element when inserted into the Villard voltage doubler circuit. Upon completion of the diode model, proper analysis of the Villard voltage doubler circuit involves DC loop analysis and AC nodal analysis. The DC loop analysis serves as the tool by which an output DC voltage can be related to the incident AC voltage. The AC nodal analysis provides the means by which the input RF energy necessary to generate a given incident AC voltage can be determined.

Modeling the Rectification Structure

Due to the popularity of integrating RF scavenging circuits directly onto CMOS, the diode connected MOSFET is a common choice as the rectification element in a Villard voltage doubler (Fig. 33).

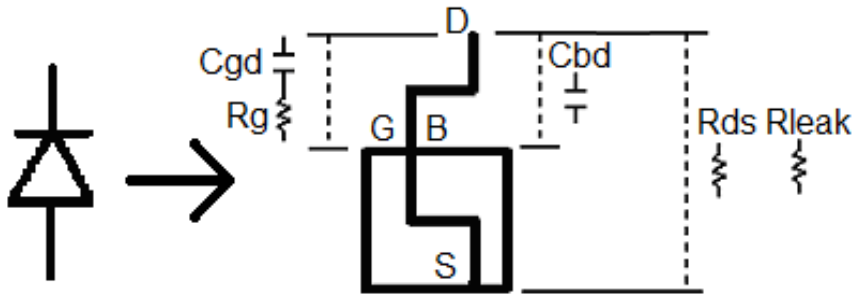


Fig. 33 Illustration of diode connected MOSFET

To determine a large signal model, it is necessary to identify the resistance of the rectifying structure, as well as any sources of parasitic impedance.

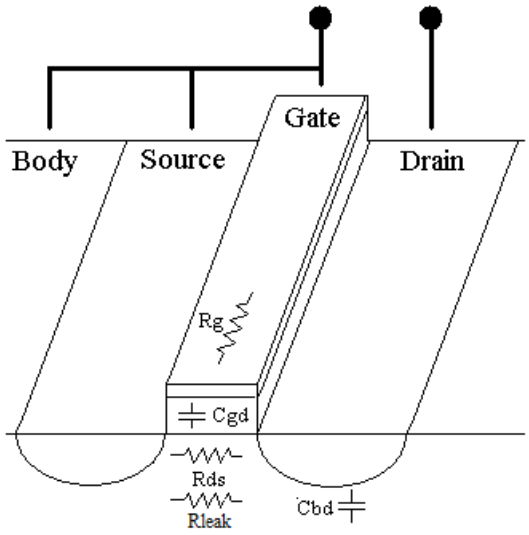
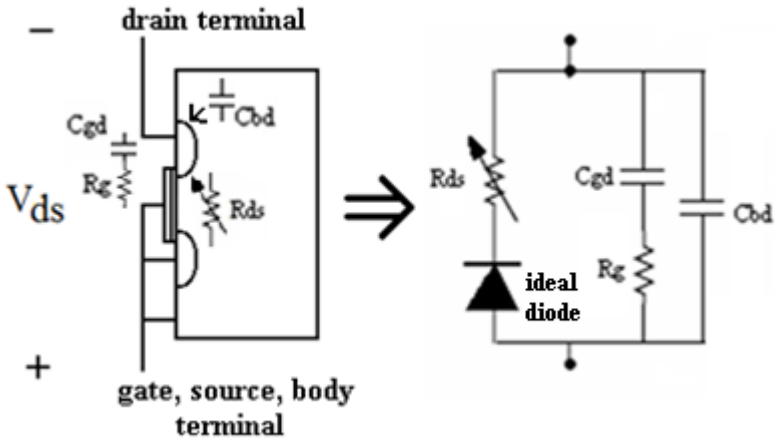
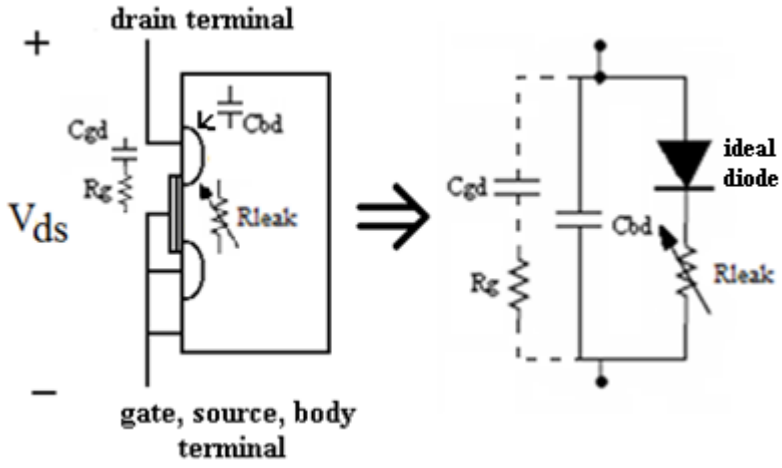


Fig. 34 Illustration of substrate connections for diode connected MOSFET and the associated sources of parasitic.

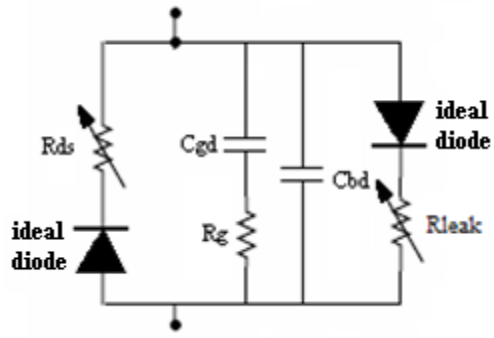
Fig. 34 illustrates the physical realization of the diode connected MOSFET and identifies the MOSFET elements and parasitics that contribute to modeling the diode connected MOSFET.



(a)



(b)



(c)

Fig. 35 Large signal model of diode connected MOSFET that is forward biased (a), reverse biased (b) and general case (c) .

The resulting large signal model for the diode connected MOSFET that has been forward biased, reverse biased and a general model that is valid in either regime of operation is presented in Fig. 35. In Fig. 35b, the path for the gate parasitics is dashed to indicate that although present, C_{gd} is approximately zero when the diode connected MOSFET is reverse biased, effectively negating any contribution to the impedance presented by the diode connected MOSFET. The total impedance presented by the diode connected MOSFET is the cumulative result of the rectifying channel resistance when forward biased, $R_{ds}(t)$; the gate parasitics, $C_{gd}(t)$ and $R_{gd}(t)$; the parasitic capacitance due to the PN junction at the drain, $C_{bd}(t)$; and finally the leakage current across the MOSFET channel when reverse biased, $R_{leak}(t)$.

The channel resistance, $R_{ds}(t)$ due to the rectifying path is derived from the channel current for the MOSFET. As indicated in Eqn. 23, the channel current for a diode connected MOSFET that is forward biased is modeled by the transconductance equations for a MOSFET in three separate regions based on the level of inversion of the channel between the drain and source where $V_{ds}(t)$ is equal to $V_{gd}(t)$ [87].

$$I_{ds}(t) = 0 \qquad V_{ds}(t) < 0$$

$$I_{ds}(t) = \frac{W_{eff}}{L_{eff}} \cdot I_{vth} \cdot \exp\left(\frac{V_{ds}(t) - V_{th}}{n \cdot V_T}\right)\left[1 - \exp\left(-\frac{V_{ds}(t)}{V_T}\right)\right] \qquad 0 < V_{ds}(t) < V_{th}$$

$$I_{ds}(t) = K \cdot \frac{\left(V_{ds}(t) - V_{th}\right)^2 \cdot \left(1 + \gamma \cdot V_{ds}(t)\right)}{1 + 2 \cdot K \cdot R_{sx} \cdot \left(V_{ds}(t) - V_{th}\right)} \qquad V_{ds}(t) > V_{th}$$

Eqn. 23. Channel current of a diode connected MOSFET.

The parameters used in Eqn. 23 include the dimensions of the MOSFET (W_{eff}, L_{eff}), channel length modulation parameter (γ), source resistance due to velocity saturation (R_{sx}), MOSFET capacitance ratio (n), thermal voltage (V_T), drain source current at threshold (I_{vth}), and parameter K defined in TABLE II.

It's important to note that the PN junction formed between the body and drain is forward biased at the same time that V_{ds} is greater than V_{th} allowing current to flow across the channel of the MOSFET. However, current lost to the PN junction (I_{pn}) is very small compared to the channel current, I_{ds} and can be modeled simply as a reduction in threshold voltage [88]. I_{ds} dominates I_{pn} because the MOSFET threshold voltage is less than the junction potential of the PN junction and thus turns on more quickly.

Given that $V_{ds}(t)$ and $I_{ds}(t)$ are a function of time, and the performance of the circuit is governed by the average resistance over a period of the input RF signal presented between the drain and source, R_{ds} is derived to be:

$$R_{ds} = \frac{\left(V_{ds}^{\ rms}\right)^2}{\left(\overline{V_{ds}(t) \cdot I_{ds}(t)}\right)}$$

Eqn. 24. Effective large signal channel resistance of a diode connected MOSFET.

Where $V_{ds}^{\ rms}$ is equal to the rms value of $V_{ds}(t)$ while forward biasing the rectification structure.

The second path is a result of the AC coupled path between the gate and the drain and is a product of the combined contribution of the gate capacitance and the gate resistance derived in Eqn. 25 and Eqn. 26. Fig. 34 presents a simplified view of the gate resistance as the sheet resistance of the polysilicon gate. A more complex view of the gate resistance used in this analysis is presented by the work in [89] and models the gate resistance as a function of the polysilicon sheet resistance and the channel resistance.

$$C_{gd} = \frac{2}{3} \cdot C_{ox} \cdot W_{eff} \cdot L_{eff} \qquad V_{ds}(t) \le 0$$
$$C_{gd} = 0 \qquad V_{ds}(t) > 0$$

Eqn. 25. Gate capacitance of a diode connected MOSFET.

$$R_g = \left(\frac{1}{12} \cdot \frac{R_{res} \cdot W_{eff}}{{n_f}^2 \cdot L_{eff}} \right) + R_s + \left(\frac{1}{12} \cdot \frac{L_{eff}}{n \cdot W_{eff} \cdot u_n \cdot C_{ox} \cdot V_t} \right)$$

Eqn. 26. Gate resistance of a diode connected MOSFET [89].

The gate resistance, R_g is a function of the sheet resistance of the gate (R_{res}), transistor size (W_{eff}, L_{eff}), number of gate fingers (n_f), mobility (u_n), oxide capacitance per unit area (C_{ox}), thermal voltage (V_T), and total resistive losses due to layout connections to the gate (R_s). The quantity 1/12 is a fitting parameter.

The third path is formed at the PN junction between the drain and the body indicated in Fig. 34. This path contributes to the parasitic capacitance of the junction. The resulting expressions for C_{bd} is a time average of the junction capacitance ($C_j(t)$) over a single period of the RF signal.

$$C_{bd} = \overline{C_j(t)}$$

Eqn. 27. Large signal capacitance of the PN junction formed between the body and drain.

Where $C_j(t)$ is the time dependant instantaneous capacitance of the PN junction as modeled under the BSIM 3.3 model [90].

$$C_j(t) = \frac{C_{j,area} \cdot A_{junc} + C_{j,per} \cdot P_{junc}}{\left(1 - \frac{V_{ds}(t)}{Y}\right)^M} \qquad V_{ds}(t) \le FC \cdot Y$$

$$Cj(t) = \frac{C_{j,area} \cdot A_{junc} + C_{j,per} \cdot P_{junc}}{(1 - FC)^M} \cdot \left(1 + \frac{M}{Y \times (1 - FC)} \times (V_{ds}(t) - FC \cdot Y)\right) \qquad V_{ds}(t) > FC \cdot Y$$

Eqn. 28. Instantaneous capacitance of the PN junction formed between the body and drain [90].

The instantaneous capacitance of the PN junction ($C_j(t)$) is a function of the per unit area junction capacitance ($C_{j,area}$), per unit perimeter junction perimeter ($C_{j,per}$), area of

the junction (A_{junc}), perimeter of the junction (P_{junc}), junction potential (Y), grading coefficient (M), and forward bias depletion capacitance coefficient (FC).

The final path is a result of the leakage current through the MOSFET that is reverse biased. An ideal MOSFET allows no current to flow when off, but in practice small amounts of current flow when in the off state. This effect can cause minor impedance changes for a voltage doubler under low power operation and is modeled by R_{leak}.

$$R_{leak} = \frac{V_{ds,reverse}}{I_{ds}\left(V_{gs}=0, V_{ds,reverse}=2\cdot\left|V_{inc}\right|\right)} = \frac{2\cdot\left|V_{inc}\right|}{\frac{W_{eff}}{L_{eff}}\cdot I_{vth}\cdot\exp\left(\frac{-V_{th}}{n\cdot V_T}\right)\left[1-\exp\left(-\frac{\left|V_{inc}\right|}{V_T}\right)\right]}$$

Eqn. 29. Leakage current through the reverse bias diode connected MOSFET.

Eqn. 29 approximates R_{leak} as the current and voltage drop across the diode connected MOSFET at the maximum reverse bias voltage, $V_{ds,reverse}$. As will be seen in the next section on DC loop equations, the maximum point of reverse bias is approximately equal to $2*V_{inc}$, where V_{inc} is the magnitude of the voltage incident on the Villard voltage doubler.

At this point, a model and analytical expressions for the behavior of the diode connected MOSFET have been established. This model serves as the basis for the DC loop analysis and AC nodal analysis to follow.

The DC Loop Equations

The DC solution is derived through the application of Kirchhoff's loop analysis and provides a means to relate the voltage incident on a series of stacked voltage doublers to the resulting output voltage.

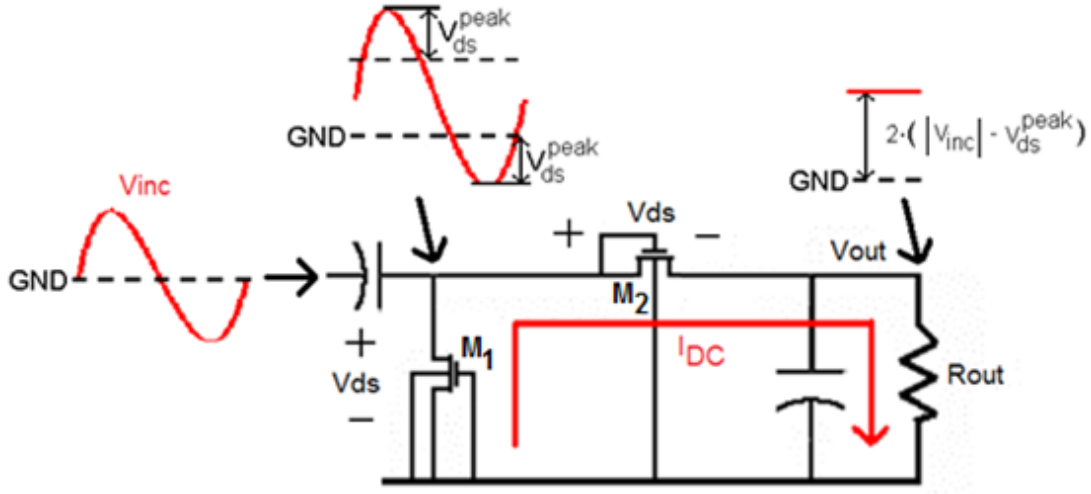


Fig. 36 Illustration of the operating voltage levels and current through the DC loop of a single stage of the Villard voltage doubler.

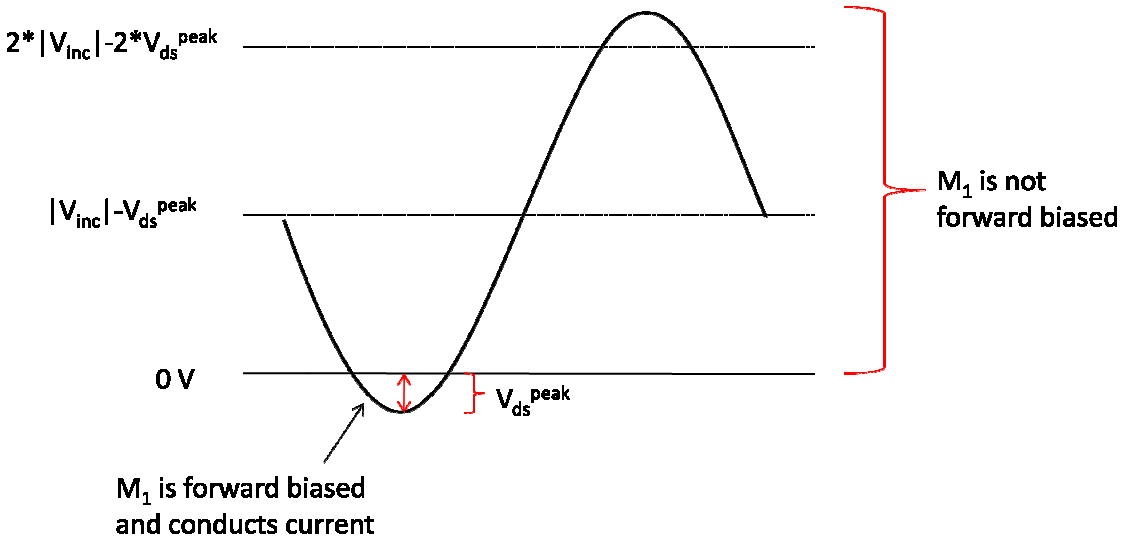
Fig. 36 presents an illustration of the DC loop for a single stage Villard voltage doubler.

The periodic incident voltage gives rise to a current across each rectifying MOSFET (M_1 and M_2). The rectifying diodes are in series in the DC loop and parallel to the charge storing capacitors. Therefore, Eqn. 24 is modified resulting in an R_{DC} of:

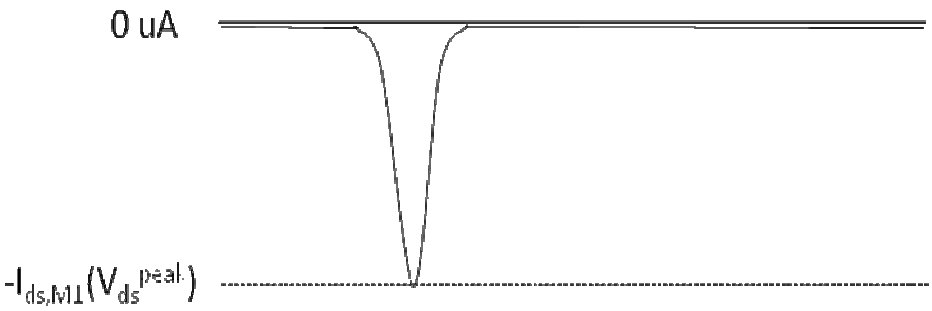
$$R_{DC} = \frac{\left(V_{ds}^{\ peak}\right)^2}{\left(\overline{P_{ds,Mn}(t)}\right)} = \frac{\left(V_{ds}^{\ peak}\right)^2}{\left(\overline{V_{ds,Mn}(t) \cdot I_{ds,Mn}(t)}\right)}$$

Eqn. 30. Effective DC resistance of a diode connected MOSFET in the Villard voltage doubler.

Where $\overline{P_{ds,Mn}(t)}$ is the average power over one period through the diode connected MOSFET, $I_{ds,Mn}(t)$ is the current through the diode connected MOSFET, and $V_{ds,Mn}(t)$ is the time domain voltage drop across the diode connected MOSFET, M_n where n equals 1 or 2 (M_1 or M_2). V_{ds}^{peak} is the maximum forward bias across the diode connected MOSFET as depicted in Fig. 36 for diode M_1, resulting from the voltage incident on the rectifying diodes following the DC blocking capacitor.



(a)



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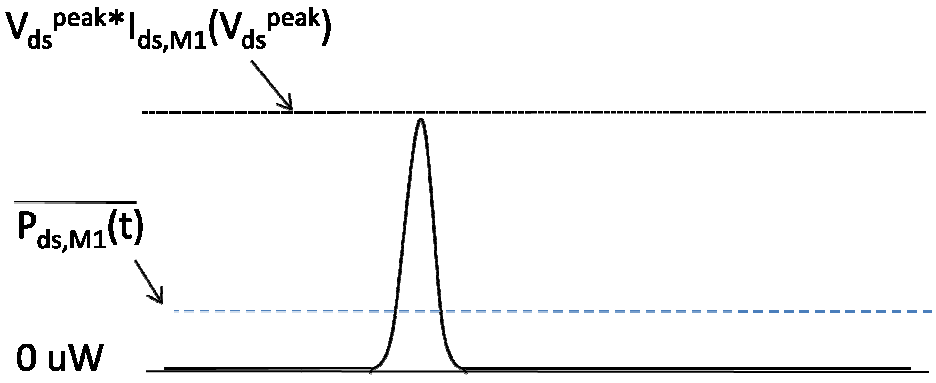
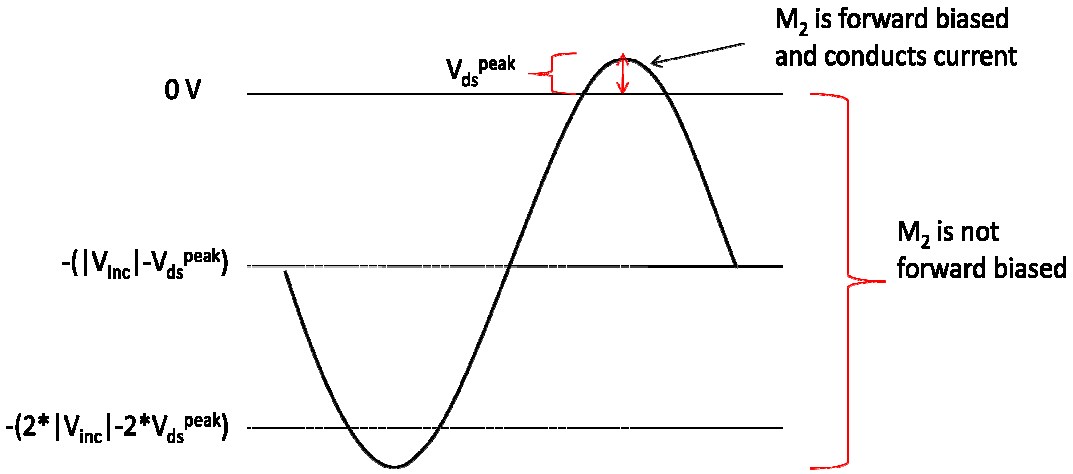
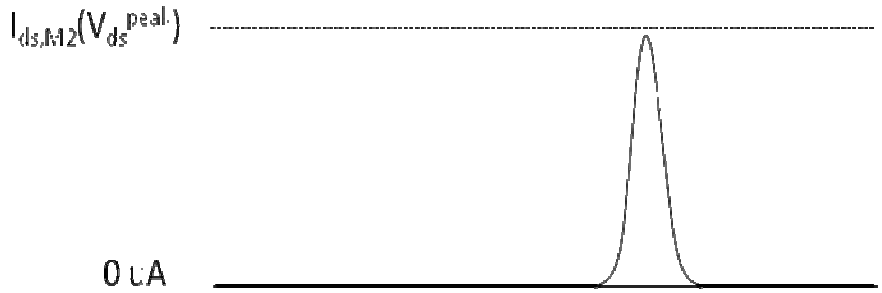


(c)

Fig. 37 The voltage drop, $V_{ds,M1(t)}$ (a), current, $I_{ds,M1}(t)$ (b), and power dissipated, $P_{ds,M1}(t)$ (c) across diode connected MOSFET, M_1.



(a)



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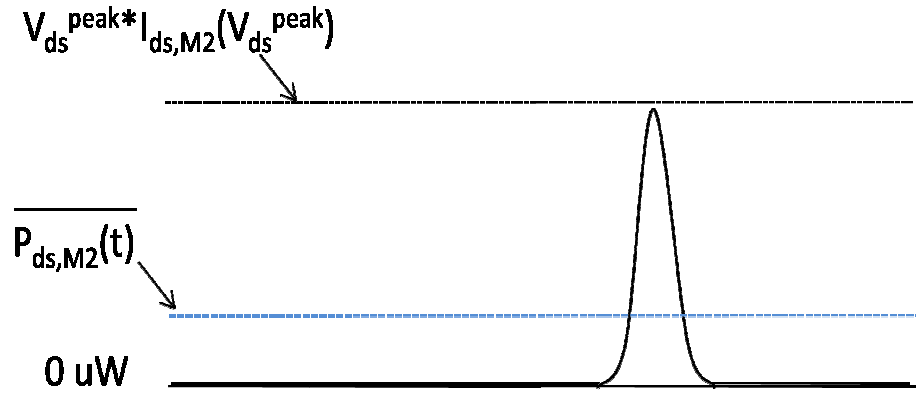


(c)

Fig. 38 The voltage drop, $V_{ds,M2(t)}$ (a), current, $I_{ds,M2}(t)$ (b), and power dissipated, $P_{ds,M2}(t)$ (c) across diode connected MOSFET, M_2.

The voltage, resulting current, and power dissipated across M_1 ($V_{ds,M1}(t)$, $I_{ds,M1}(t)$, $P_{ds,M1}(t)$) and M2 ($V_{ds,M2}(t)$, $I_{ds,M2}(t)$, $P_{ds,M2}(t)$) over one period are illustrated in Fig. 37 and Fig. 38. Peak forward bias across the diode connected MOSFETs, V_{ds}^{peak} and the mean power dissipated across each diode connected mosfet ($\overline{P_{ds,M1(t)}}$ and $\overline{P_{ds,M2(t)}}$) are also indicated in Fig. 37 and Fig. 38.

From Fig. 37a and Fig. 38a, it can be seen that for the voltage doubler circuit, $V_{ds,M1}(t)$ is:

$$V_{ds,M1}(t) = -\left(|V_{inc}| \cdot \sin(2\pi ft) + |V_{inc}| - V_{ds}^{peak}\right).$$

Eqn. 31. Voltage difference between the drain and source terminals of a diode connected MOSFET in the Villard voltage doubler.

And $V_{ds,M2}(t)$ is:

$$V_{ds,M2}(t) = \left(|V_{inc}| \cdot \sin(2\pi ft) - |V_{inc}| + V_{ds}^{peak}\right).$$

Eqn. 32. Voltage difference between the drain and source terminals of a diode connected MOSFET in the Villard voltage doubler.

Since, both $I_{ds,M1}(t)$ and $I_{ds,M2}(t)$ are approximately equal to zero while the respective diodes M_1 and M_2 are reverse biased, when calculating power dissipation across the diode connected MOSFETs (M_1 and M_2), $V_{ds,approx}(t)$ can be used as an approximation of $V_{ds,M1}(t)$ and $V_{ds,M2}(t)$.

$$V_{ds,Mn(t)} \approx V_{ds,approx}(t) = V_{ds}^{peak} \cdot \sin(2 \cdot \pi \cdot f \cdot t)$$

Eqn. 33. Approximation of the incident voltage across the drain and source terminals of a MOSFET valid when solving the DC loop equations.

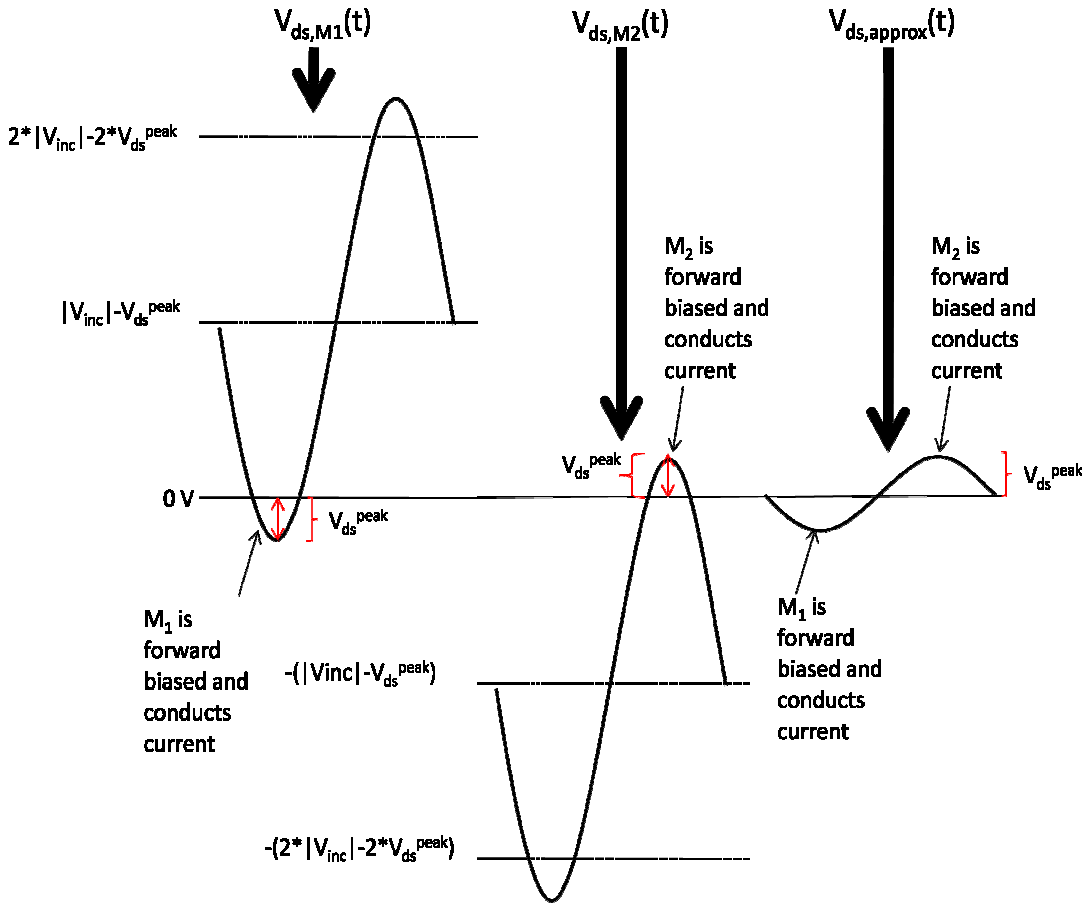


Fig. 39 The voltage drop across M1 and M2 ($V_{ds,M1}(t)$ and $V_{ds,M2}(t)$) and $V_{ds,approx}(t)$ which is a valid approximation for both $V_{ds,M1}(t)$ and $V_{ds,M2}(t)$.

The waveforms $V_{ds,M1}(t)$, $V_{ds,M2}(t)$ and the resulting approximation, $V_{ds,approx}(t)$ are illustrated in Fig. 39. $V_{ds,approx}(t)$ provides an approximation of the conductive region ($I_{ds,Mn}(t) \neq 0$, were n =1 or 2) for both $V_{ds,M1}(t)$ and $V_{ds,M2}(t)$.

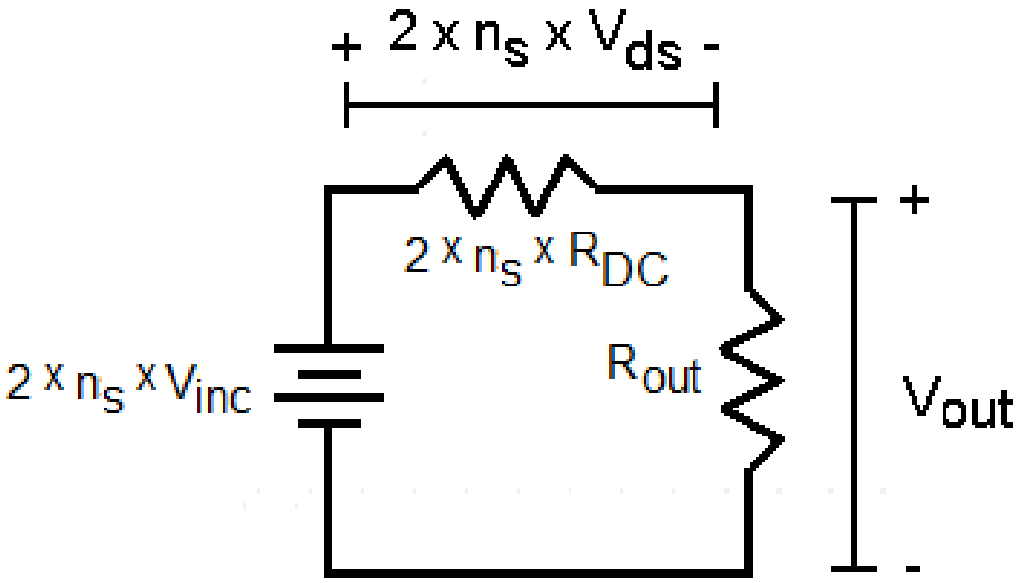


Fig. 40 Model of the multi-stage Villard voltage doubler as a DC power source.

With the capacitive elements acting as charge storage devices for the rectifying elements, a Villard voltage doubler of n_s DC loops can be modeled as indicated in Fig. 40 [91]. From this model, utilizing the simple relationship, V=I*R, the DC current across the output load (R_{out}) and DC current across the effective MOSFET resistance (R_{DC}) can be derived.

$$I_{DC,R_{out}} = \frac{n_s \cdot \left(2 \cdot |V_{inc}| - 2 \cdot V_{ds}^{\ peak}\right)}{R_{out}}$$

Eqn. 34. DC current across output load, R_{out}.

$$I_{DC,R_{DC}} = \frac{V_{ds}^{peak}}{R_{DC}}$$

Eqn. 35. DC current across effective MOSFET resistance, R_{DC}.

By equating these two currents and algebraic manipulation, the second equation for R_{DC} presented in Eqn. 36 can be extracted where n_s is the number of stacked stages.

$$R_{DC} = \frac{V_{ds}^{peak} \cdot R_{out}}{n_s \cdot \left(2 \cdot \left|V_{inc}\right| - 2 \cdot V_{ds}^{peak}\right)}$$

Eqn. 36. DC resistance of the diode connected MOSFET derived from the model depicted in Fig. 40.

By setting Eqn. 30 and Eqn. 36 equal, V_{ds}^{peak} can be solved for. This equality is best solved through numeric methods. Once V_{ds}^{peak} has been determined, V_{out} can be evaluated from:

$$V_{out} = n_s \cdot \left(2 \cdot \left|V_{inc}\right| - 2 \cdot V_{ds}^{peak}\right)$$

Eqn. 37. Output DC voltage of a multistage Villard voltage doubler.

Alternatively, one can determine $|V_{inc}|$ from a given V_{out}, by expressing R_{DC} as:

$$R_{DC} = \frac{V_{ds}^{peak} \cdot R_{out}}{V_{out}}$$

Eqn. 38. Effective DC resistance of diode connected MOSFET derived from Fig. 40 arranged as a function of V_{out}.

Once again V_{ds}^{peak} can be determined from Eqn. 30 and Eqn. 38 while Eqn. 37 can be rearranged to express $|V_{inc}|$ as a function of V_{out}.

$$|V_{inc}| = \frac{\frac{V_{out}}{n_s} + 2 \cdot V_{ds}^{peak}}{2}$$

Eqn. 39. Input incident voltage for a multi-stage Villard voltage doubler as a function of output voltage.

Thereby, one can determine V_{out} as a function of $|V_{inc}|$ or $|V_{inc}|$ as a function of V_{out}.

The AC Nodal Equations

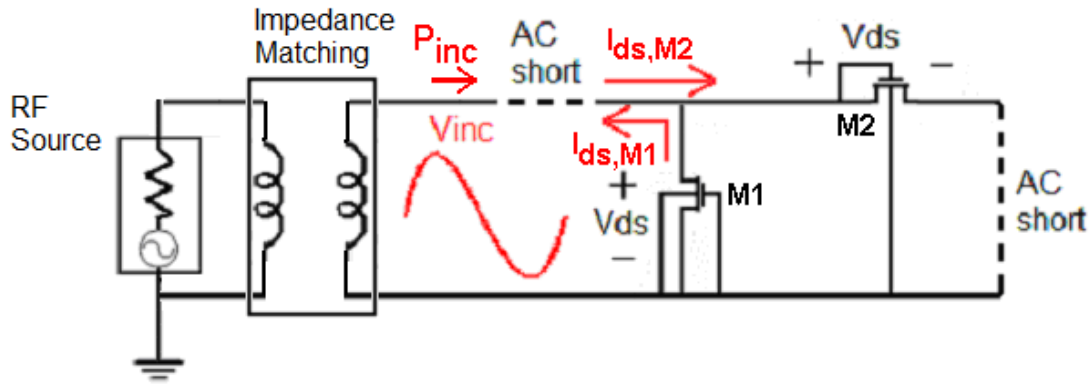


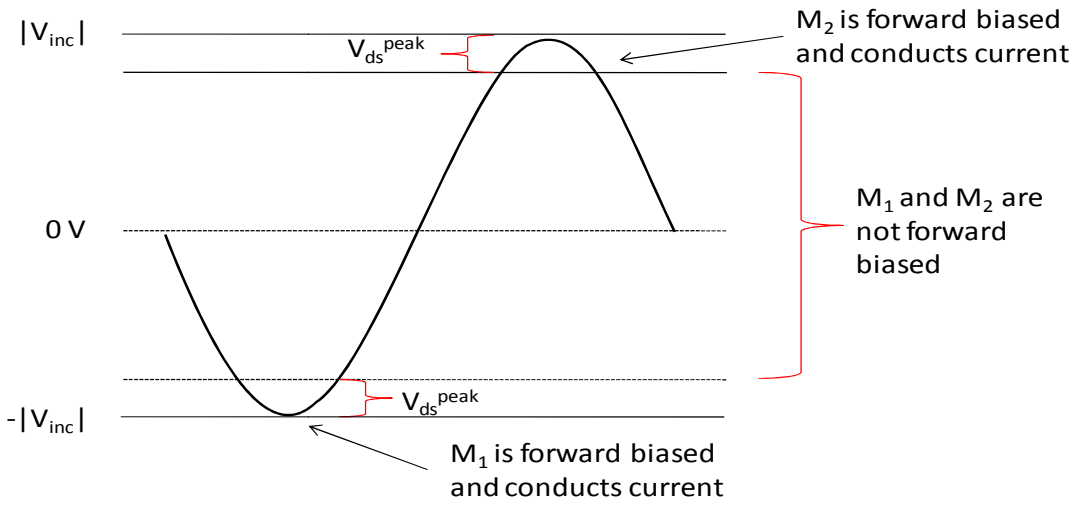
Fig. 41 Illustration of the Villard Voltage doubler with incident voltage and resulting AC current.

The AC analysis of the diode connected MOSFET is more complex than the DC analysis. Fundamentally, the AC input equations are an application of Kirchhoff's Current Law. Therefore, as illustrated in Fig. 41, the AC current incident on the voltage doubler is the summation of the currents through both diodes, $I_{ds,M1}(t)$ and $I_{ds,M2}(t)$. $I_{ds,M1}(t)$ and $I_{ds,M2}(t)$ are functions of $V_{ds,M1}(t)$ and $V_{ds,M2}(t)$, respectively, (or $V_{ds,approx}(t)$ as previously discussed) as illustrated during the DC loop analysis in Fig. 37 and Fig. 38. The current draw of a single stage of the Villard voltage doubler represents a real resistance equal to:

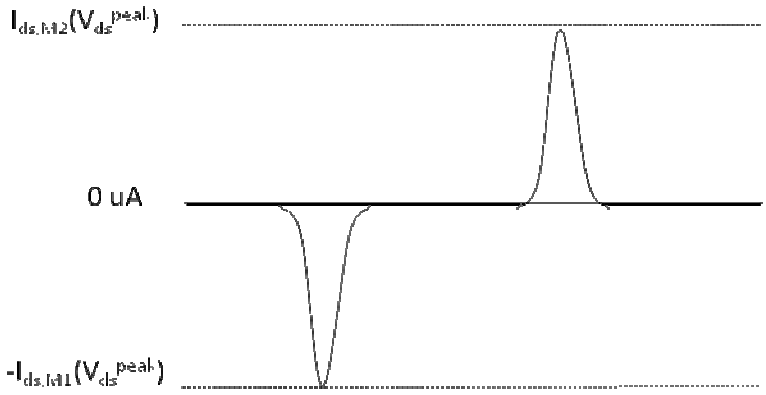
$$R_{AC} = \frac{\left(\left|V_{inc}(t)\right|\right)^2}{2 \cdot \overline{P_{inc}(t)}} = \frac{\left(\left|V_{inc}(t)\right|\right)^2}{2 \cdot \overline{\left(V_{inc}(t) \cdot \left(I_{ds,M1}(t) + I_{ds,M2}(t)\right)\right)}}$$

Eqn. 40. Effective AC resistance of the drain source channel for a diode connected MOSFET in a Villard voltage doubler.

R_{AC} represents a diode structure with no parasitics except the threshold voltage. As illustrated in Fig. 41, $V_{inc}(t)$ is the time domain voltage incident on the Villard voltage doubler; $\overline{P_{inc}(t)}$ is the average power draw of the Villard voltage doubler; and $I_{ds,M1}(t)$ and $I_{ds,M2}(t)$ are the time domain current through the diode connected MOSFETs, M_1 and M_2.



(a)



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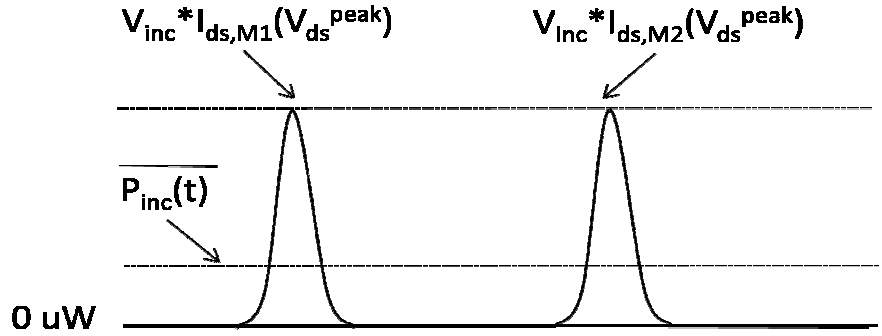


(c)

Fig. 42 The input voltage to the Villard voltage doubler, $V_{inc}(t)$ (a), sum of current, $I_{ds,M1}(t)$ and $I_{ds,M2}(t)$ (b), and power input to the Villard voltage doubler, $P_{inc}(t)$ (c).

Fig. 42 plots example waveforms for $V_{inc}(t)$, the sum of $I_{ds,M1}(t)$ and $I_{ds,M2}(t)$, and $P_{inc}(t)$. The average power entering the Villard voltage doubler, $\overline{P_{inc}(t)}$ is also indicated.

It is assumed that a matching circuit is used, as in Fig. 41, to match the input power source to the impedance presented by the cascaded voltage doubler of n_s stages. Therefore, the power necessary to generate the incident voltage from the DC loop equations when no additional parasitic are present would be expressed as:

$$P_{in} = \frac{n_s \cdot \left(\left|V_{inc}\right|\right)^2}{2 \cdot R_{AC}}$$

Eqn. 41. Input AC power draw of a multi-stage Villard voltage doubler without the presence of parasitic losses.

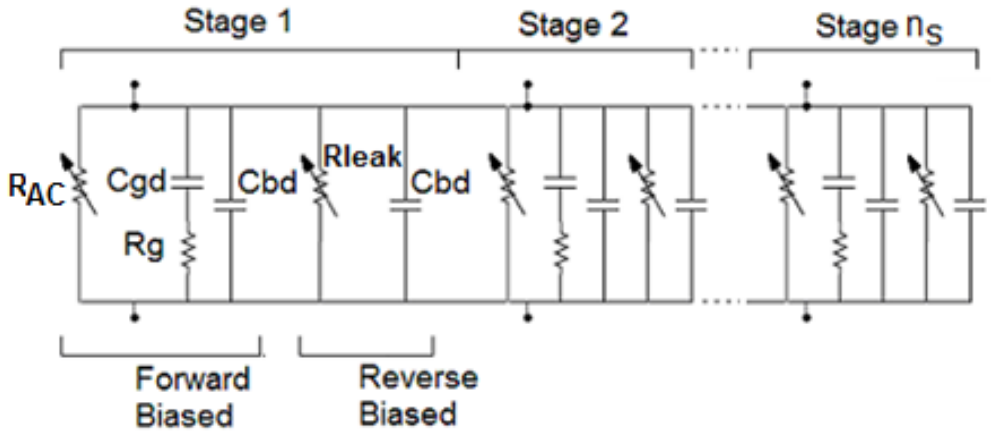


Fig. 43 The AC impedance model of a Villard voltage doubler consisting of n_s stages including the parasitics of CMOS integration.

However, as indicated previously, while determining the model for the diode connected MOSFET, there are parasitics that affect the impedance presented at the input to the Villard voltage doubler. Given that the DC bypass capacitors are sufficiently large to appear as shorts at the RF operating frequency, a Villard voltage doubler can be modeled as in Fig. 43 and the total impedance can be expressed as:

$$Z_{in} = \frac{R_{AC} \parallel Z_{gate} \parallel X_{pn} \parallel R_{leak}}{n_s}$$

Eqn. 42. Input AC impedance of a multi-stage Villard voltage doubler in the presence of parasitic losses.

Where R_{leak} was defined in Eqn. 29, while Z_{gate} and $X_{pn,}$ can be expressed as:

$$Z_{gate} = \left(R_g + \frac{-j}{2 \cdot \pi \cdot f \cdot C_{gate}} \right)$$

Eqn. 43. Parasitic impedance of MOSFET gate.

C_{gate} refers to the gate capacitance, C_{gd} when the diode connected MOSFET is forward biased. Therefore, C_{gate} is equal to C_{gd} when V_{ds} is less than zero from Eqn. 25.

$$X_{pn} = \left(\frac{-j}{2 \cdot \pi \cdot f \cdot C_{bd}} \right)$$

Eqn. 44. Parasitic impedance of the PN junction formed between the body and drain of the diode connected MOSFET.

The power transferred to a cascaded Villard voltage doubler of n_s stages to generate $|V_{inc}|$ at the input to the Villard voltage doubler becomes:

$$P_{in} = real\left(\frac{|V_{inc}|^2}{2 \cdot Z_{in}}\right)$$

Eqn. 45. Input AC power draw including parasitic losses.

While the DC loop analysis provides the means to relate the DC output voltage to the input AC voltage, the AC nodal analysis provides the tool to relate input AC voltage to input RF energy. Thus, the input RF energy incident on the power matched Villard voltage doubler can be related to the resulting output voltage.

Model Validation

From the analysis presented, a model has been developed for the diode connected MOSFET. The DC loop equations were presented for relating the AC voltage incident on the Villard voltage doubler to the DC voltage generated at the output and AC nodal analysis was used to determine the power necessary to generate the voltage incident on the voltage doubler due to matching both with and without parasitic effects. To validate this model, the output voltage, as predicted by this model from a 900 MHz RF power source, was compared to harmonic balance simulations using the BSIM 4.0 model provided by a 130 nm IBM process. All required performance metrics for the model were either obtained from published values or were experimentally determined.

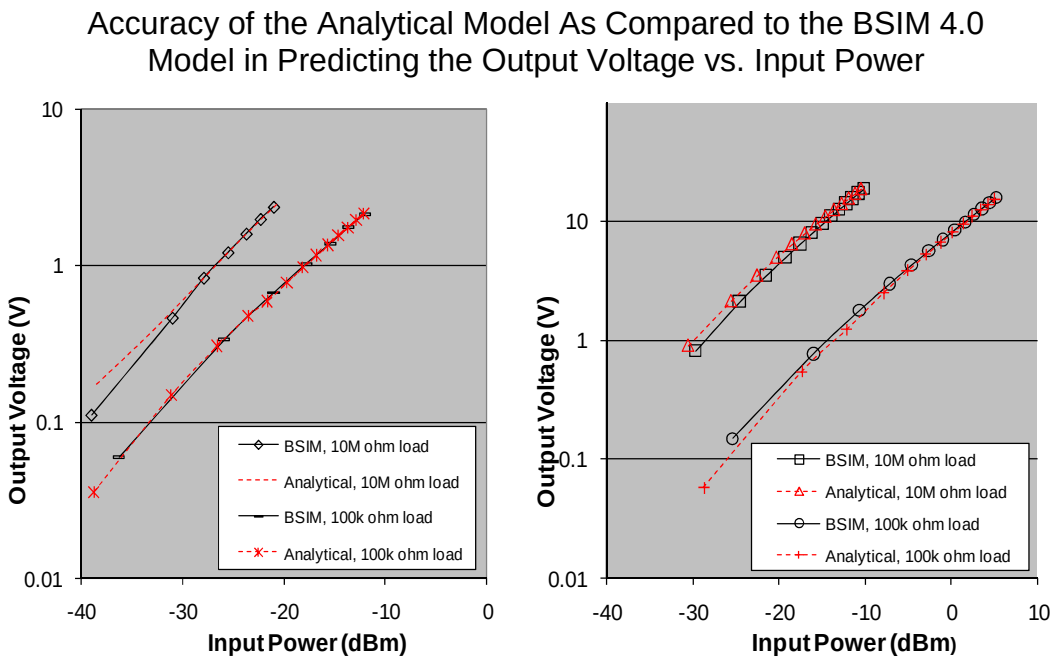


Fig. 44 Input power vs output voltage as determined by the analytical model presented and a harmonic balance simulation using the BSIM 4.0 model for a single stage power matched Villard voltage doubler (a) and eight stage power matched Villard voltage doubler (b).

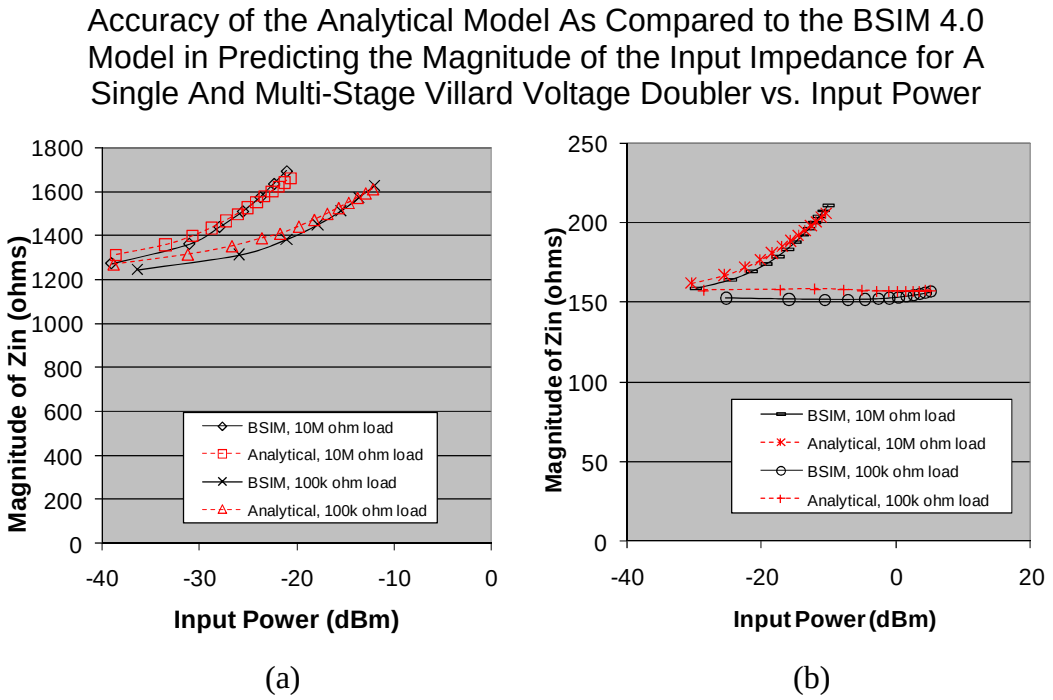


Fig. 45 Magnitude of the input impedance vs input power as determined by the presented analytical model and a harmonic balance simulation using the BSIM 4.0 model for a single stage power matched Villard voltage doubler (a) and eight stage power matched Villard voltage doubler (b).

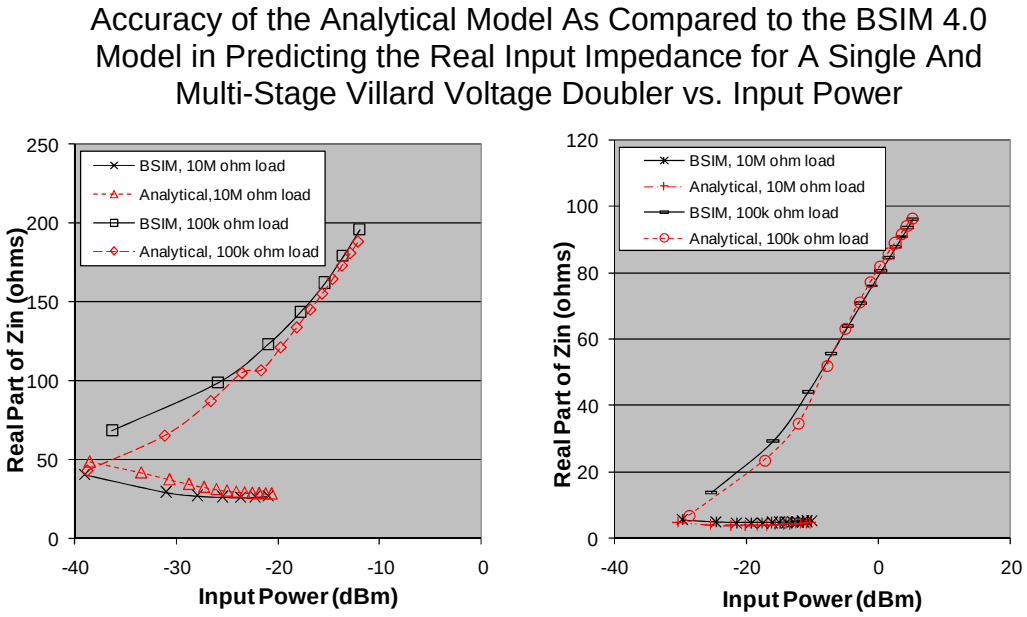


Fig. 46 Real component of the input impedance vs input power as determined by the presented analytical model and a harmonic balance simulation using the BSIM 4.0 model for a single stage power matched Villard voltage doubler (a) and eight stage power matched Villard voltage doubler (b).

Fig. 44 through Fig. 46 demonstrate the accuracy by which this model matches the results of the more complex and time consuming harmonic balance simulation with the BSIM 4.0 model under a variety of load conditions, input powers, and number of stacked voltage doubler stages.

Further validation of the analytical model was achieved through its application in fabricating the optimal RF energy scavenging circuit in a 130 nm IBM process designed to generate 1 V across a 50 kΩ load from a 2.2 GHz RF power source. The matching circuit was assumed to be an L circuit consisting of an inductor and capacitor in either a series or shunt configuration. From previous experimental

measurement, the power loss at 2.2 GHz from the finite Q of the inductors was determined to be ~6 dB in the 130 nm IBM process used for fabrication.

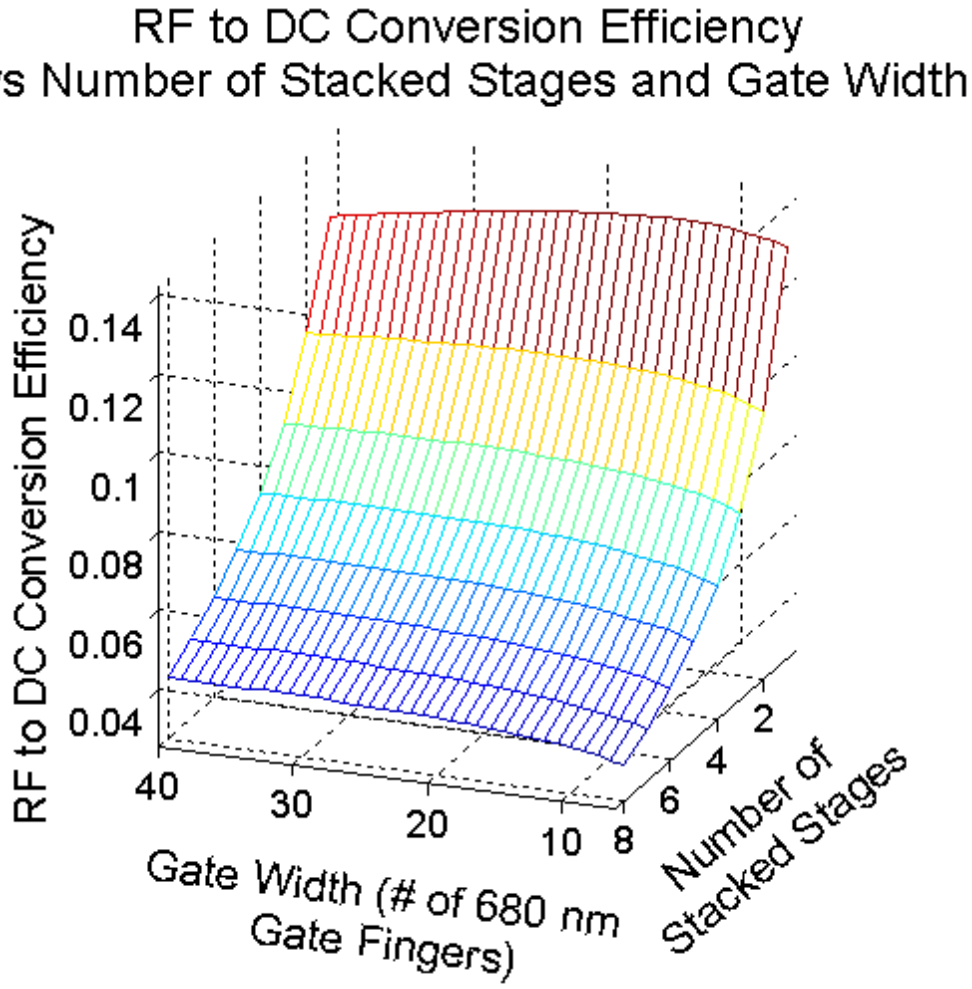


Fig. 47 Conversion efficiency vs. gate width and number of stacked voltage doubler stages

Fig. 47 illustrates that the peak efficiency occurs using one voltage doubler stage and a total gate width of 13.6 um. To validate the model, the optimal circuit design as predicted by this model was fabricated using the IBM 130 nm process.

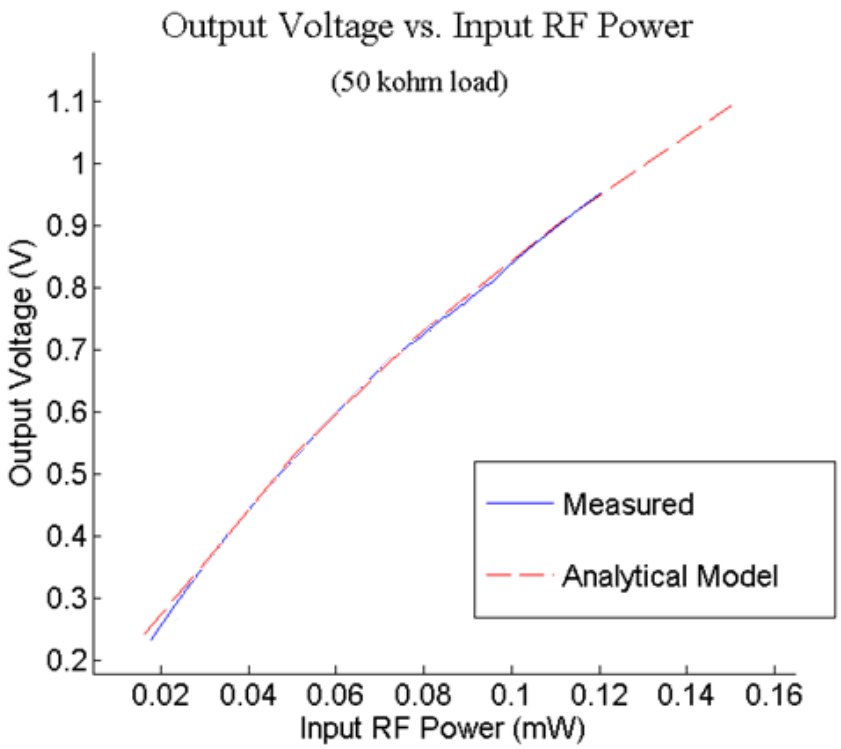


Fig. 48 Modeled and measured input power vs output voltage of RF energy scavenger design.

Fig. 48 shows very good agreement between the output voltage versus input RF power predicted by the analytical model and the measured data. The optimal design yielded an output voltage of 1 V representing an RF to DC conversion efficiency of ~14% with only -8.5 dBm of input RF energy.

Thus the analytical model has been validated through comparison to harmonic balance simulation of the BSIM 4.0 model and through optimization and measurement from a chip fabricated in the modeled 130 nm IBM process.

Effects of Parasitics on Energy Scavenging Performance

Having been validated against the BSIM 4.0 model and against measurements from a fabricated chip, the analytical model presented in this paper provides a useful tool by which the effect of performance degrading parasitics can be examined under different regimes of operation. The two types of parasitics degrading the performance of the power matched Villard voltage doubler are the losses due to the threshold voltage and parasitic capacitances and resistance formed from the gate of the rectifying diodes. The different sources of parasitics dominate the performance of the circuit in different regimes of operation. By plotting RF to DC conversion efficiency from a 900 MHz RF power source versus output load resistance and magnitude of the parasitic effect, Fig. 49 through Fig. 51 illustrate when the two parasitic sources, threshold voltage and parasitic gate impedance, will limit the performance of the power scavenging circuit.

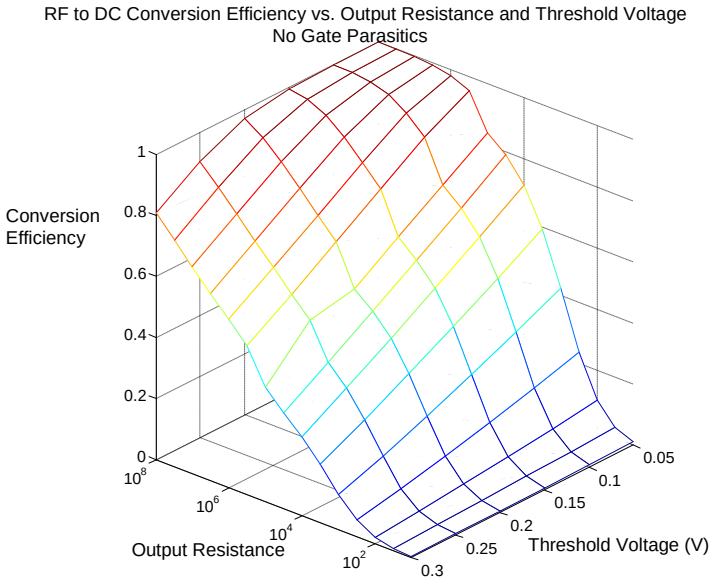


Fig. 49 RF to DC conversion efficiency versus output load impedance and threshold voltage without losses due to parasitic gate impedance.

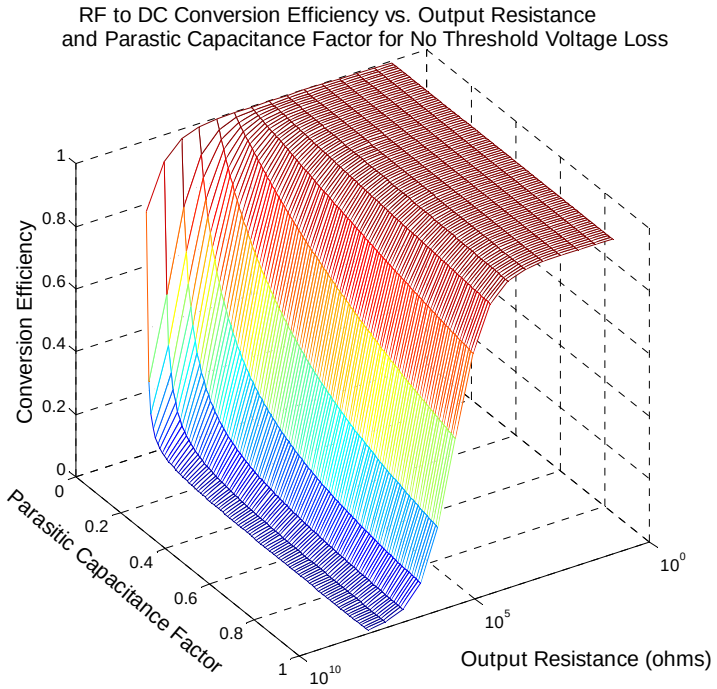


Fig. 50 RF to DC conversion efficiency versus parasitics capacitance (defined as parasitic capacitance factor times modeled parasitic capacitances) of gate impedance without threshold voltage losses.

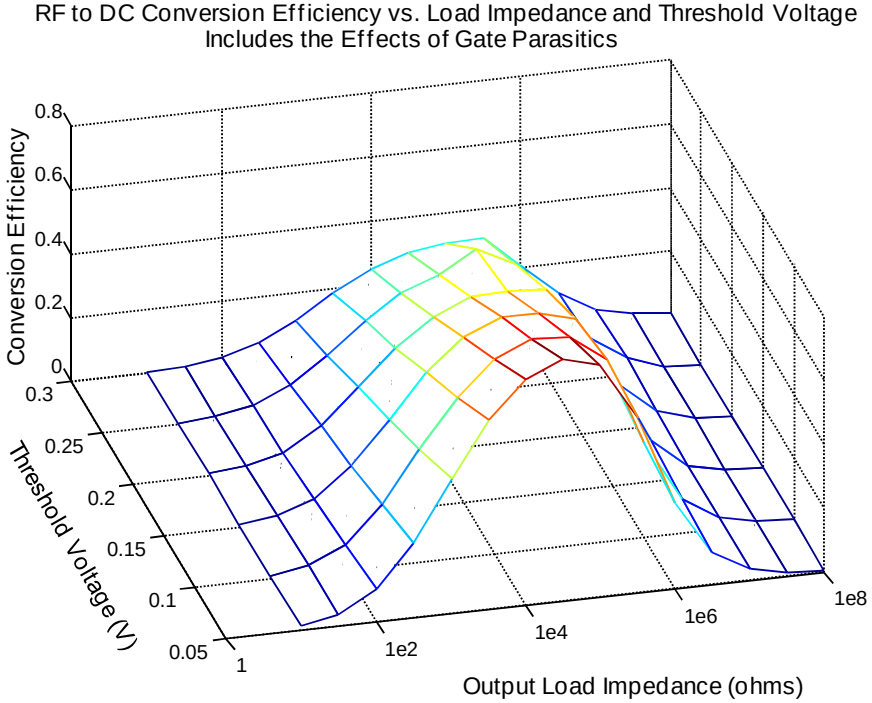


Fig. 51 RF to DC conversion efficiency versus threshold voltage with parasitic gate impedance losses.

Fig. 49 examines the effect of threshold voltage on power scavenging efficiency for a single stage power matched Villard voltage doubler. As illustrated, given a constant incident voltage (.5 V) in the presence of a threshold voltage, as output load decreases (load current increases) the conversion efficiency is reduced. As threshold voltage increases, the reduction in conversion efficiency occurs more swiftly than the reduction in output load impedance. Therefore, a reduction in the threshold voltage improves performance when high output load currents are expected. The power loss due to the threshold voltage is modeled as R_{DC} in Fig. 40.

Alternatively, increasing the parasitic capacitance portion of the gate impedance (R_g and C_{gd} in Fig. 35) decrease RF scavenging efficiency as the output load increases in magnitude (load current reduces). This is illustrated in Fig. 50 by plotting RF to DC conversion efficiency versus output resistance and parasitic capacitance factor. The parasitic capacitance factor is a constant by which the expected parasitic capacitance of the gate is scaled while the parasitic resistance of the gate remains unchanged. In this way, the power lost to the resistive gate impedance is increased or decreased as the gate capacitance is increased or decreased, respectively. In addition, to remove the effect of the threshold voltage it was necessary that K and I_{vth} defined in TABLE II approach infinity and V_{th} approaches zero. The power loss due to gate parasitics is modeled in Fig. 40 as a reduction in the resulting V_{inc} for a given input RF power level.

As a result of the threshold voltage dominating power loss when the load current is high, and the parasitic gate impedance dominating power loss when the load current is low, for a defined incident voltage there is an optimal load resistance. By plotting RF to DC conversion efficiency as a function of threshold voltage and load impedance, Fig. 51 illustrates that there is optimal load resistance when the capacitive parasitics are included in the modeling. In this case, the optimal load resistance is about 50 kΩ's.

This is an important result. Previous works in the field have targeted reducing the threshold voltage of the rectifying element to improve power scavenging performance [69],[74],[92]. This work supports that approach to improving system performance as the load resistance is lowered. However, considerable new research is aimed at very low power RF energy scavenging for trickle charging a battery. Trickle charging presents a high load impedance. As a result, this work indicates that for low power RF scavenging systems, the dominate power loss mechanism is due to parasitic gate impedance in the rectification structure.

Effect of Number of Voltage Doubler Stages on RF Energy Scavenging Performance

As discussed previously, Villard voltage doubler stages can be stacked to increase the output DC voltage. This effect can be thought of as increasing the resulting source voltage of the DC power supply created at the output of the RF energy harvesting circuit as depicted in Fig. 40. However, as also indicated in Fig. 40, additional

stacked Villard voltage doubler stages result in an increased source resistance for the output DC power source created from the RF energy harvesting circuit. This reduces the ability of stacked voltage doubler stages to drive lower output load impedances (high load currents) and necessitates the stacking of voltage doubler stages be used only when driving high output load resistances.

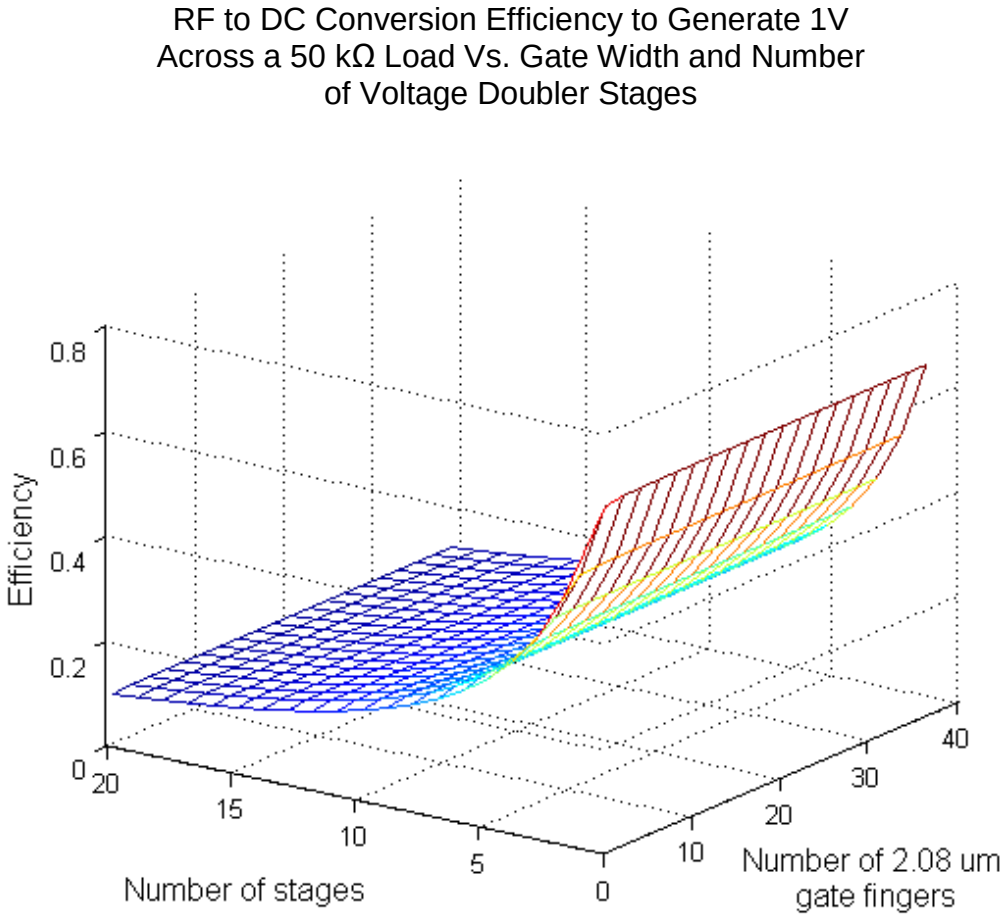


Fig. 52 RF to DC conversion efficiency to generate 1V across a 50 kΩ load versus gate width (number of 2.08 um fingers) and number of voltage doubler stages.

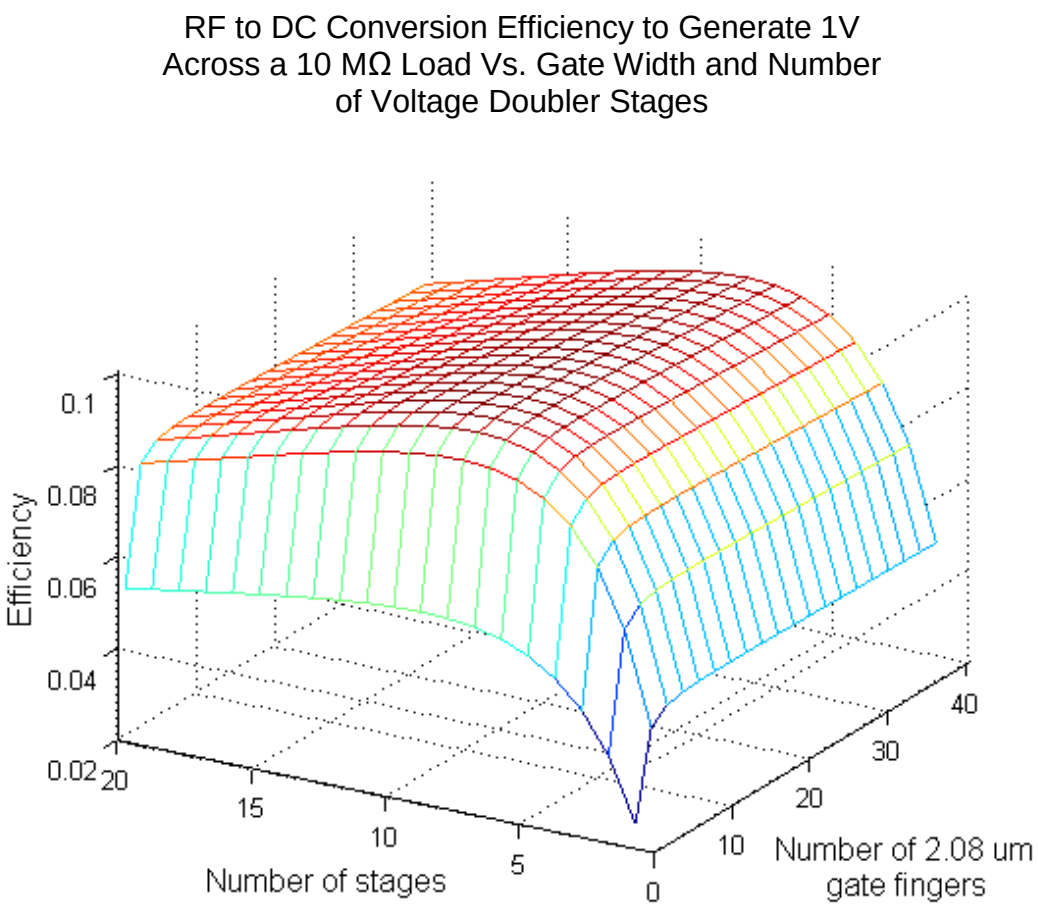


Fig. 53 RF to DC conversion efficiency to generate 1V across a 10 MΩ load versus gate width (number of 2.08 um fingers) and number of voltage doubler stages.

This effect is illustrated by Fig. 52 and Fig. 53, which depicts RF to DC conversion efficiency when generating 1 V across a high output load (10 MΩ) and low output load (50 kΩ) versus gate width (number of 2.08 um gate fingers) and number of voltage doubler stages. The model assumes that the IBM 130 nm process is used and the RF energy scavenging circuit is power matched to a 900 MHz RF source. In Fig. 52, one can see that the maximum RF to DC conversion efficiency is achieved for a gate width of 41.6 µm and only one voltage doubler stage. However, once output

load impedance is increased to 10 MΩ, maximum RF to DC conversion efficiency is achieved by stacking 8 voltage doubler stages and utilizing a gate width of 20.8 µm.

Optimization example

A significant benefit of the analytical model presented and validated, is its application to predict the optimal design of an RF energy scavenging circuit. To illustrate, the analytical model developed was used to determine the optimal transistor width and number of stacked stages for an RF energy scavenging circuit designed to generate 1 V across a 1 MΩ load from a 900 MHz RF power source.

The matching circuit was assumed to be an L Circuit consisting of an inductor and capacitor in either a series or shunt configuration. The value of the inductor and capacitor, as well as, the choice of a series or shunt L circuit was governed by the input impedance to the multi stage Villard voltage doubler. As the width of the transistor and the number of cascaded voltage doubler stages was varied, solutions that required unusually large inductors, small capacitors, or had a real component to their impedance nearing the parasitic resistance of the circuit were discarded. To this end, the inductor was limited to 30 nH or smaller, the capacitor was limited to .1 pF or larger, and the real component of the input impedance of the Villard voltage doubler was limited to larger than 5 Ω.

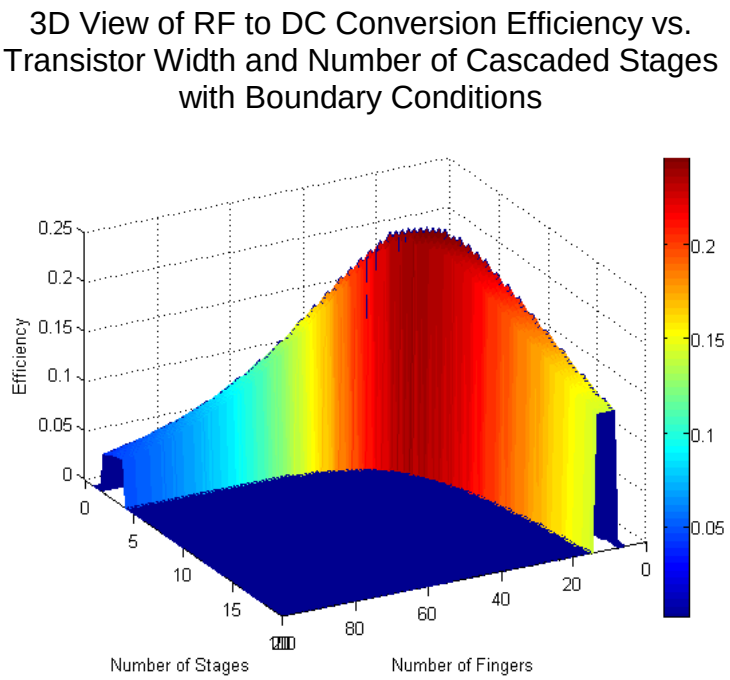


Fig. 54 3-dimensional view of the efficiency of an RF scavenging circuit as a function of the number of 2.08 um fingers and the number of cascaded voltage doubler stages.

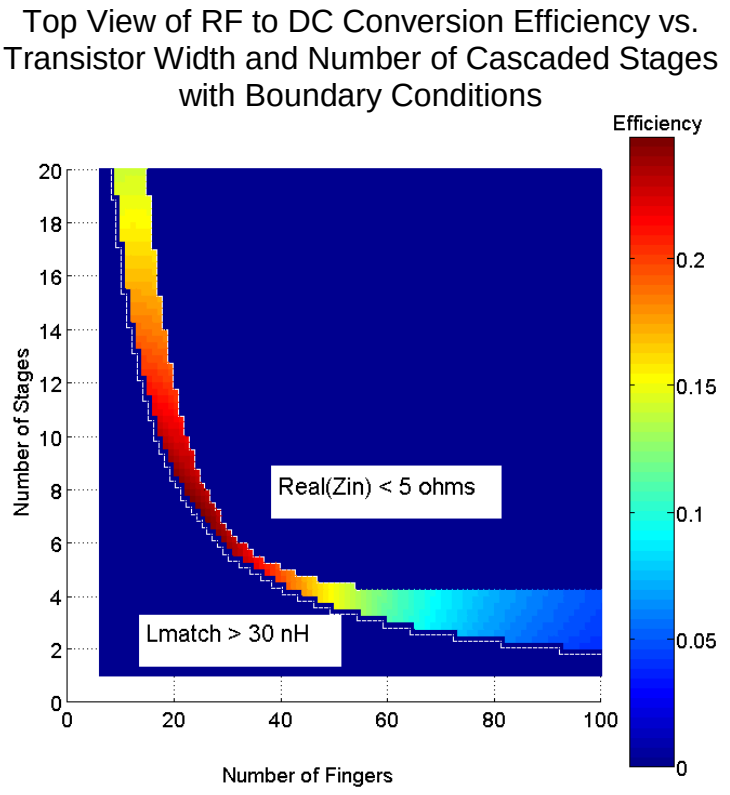


Fig. 55 Top view of the efficiency of an RF scavenging circuit as a function of the number of 2.08 um fingers and the number of cascaded voltage doubler stages.

Fig. 54 and Fig. 55 illustrate the efficiency of the design over the sample space and clearly demonstrate that there is an optimal solution consisting of 30 fingers resulting in a transistor 62.4 um wide and with six voltage doubler stages cascaded together. This results in a total efficiency of approximately 25% while requiring only about –25 dBm of input RF energy. This assumes an ideal L match circuit. Thus, a physical realization of such a design would require a larger input RF energy due to the finite Q of the inductor and capacitor used for the matching circuit.

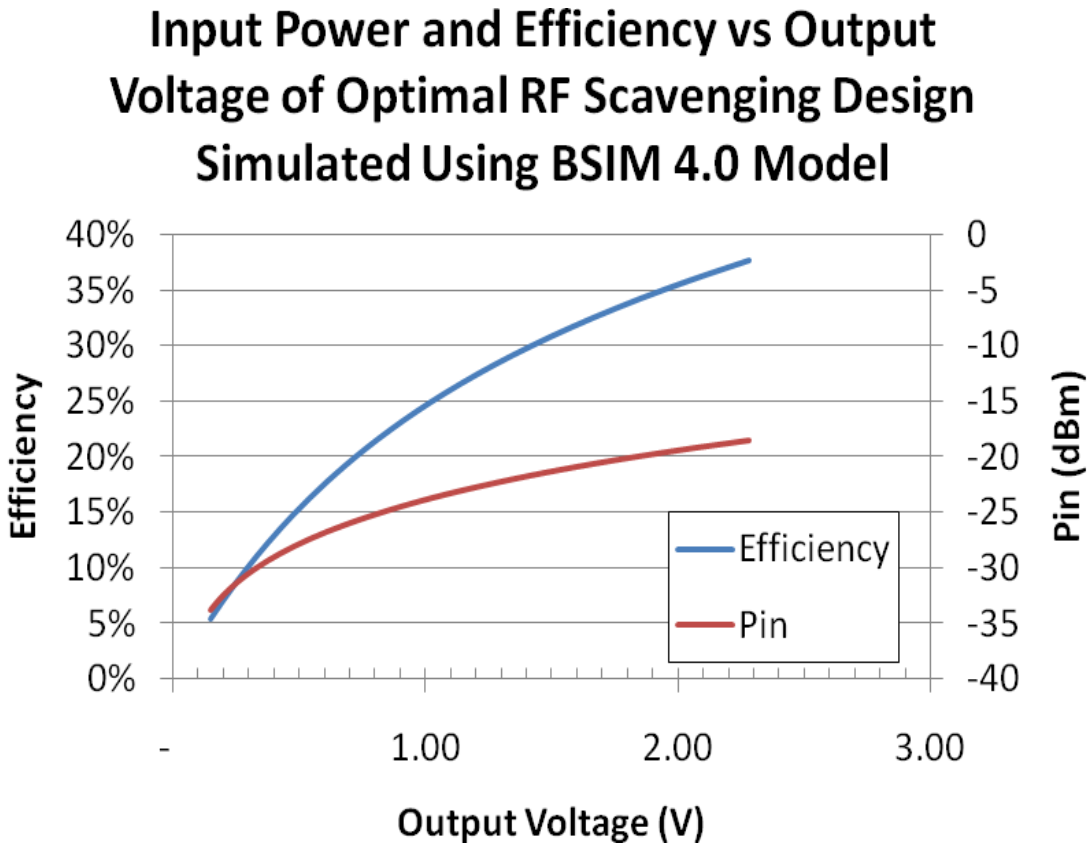


Fig. 56 Harmonic balance simulation of RF to DC conversion efficiency and incident input power versus output voltage for the optimal design determined by the analytical model using the BSIM 4.0 model.

This result was validated by performing a harmonic balance simulation using the BSIM 4.0 model. As indicated in Fig. 56, the BIM 4.0 based simulation yielded an output voltage of 1 V with an RF to DC conversion efficiency of 25% with only -25 dBm of input RF energy. This agrees very closely with the optimal design predicted by the analytical model.

Conclusions

A model has been presented for the analytical modeling of a multistage Villard voltage doubler for RF energy scavenging. The model presented is completely analytical and relies only on twenty-five parameters, of which most model a physical effect (TABLE II). This is in contrast to simulations base on the BSIM 4.0 model, which have over 250 parameters, of which a significant number are empirically derived fitting parameters [93].

The model has been validated and shows excellent agreement with the harmonic balance simulations using the BSIM 4.0 model over a wide range of simulation parameters including transistor width, number of cascaded stages, and load impedance. In addition, the model presented accurately predicted the performance of an RF energy scavenging circuit fabricated in the IBM 130 nm CMOS process. While this work utilized the diode connected MOSFET as the rectification structure in the voltage doubler, any diode structure including PN junctions and Schottky diodes could be modeled and applied to the analytical method presented.

Furthermore, the analytical model was used to explore the effect of circuit parasitics on system performance. This analysis indicates that under low power conditions (< mW), threshold voltage is the performance limiting parasitic when the load resistance on the DC output is low (< 10 kΩ). However, when the output load resistance is high (>10 kΩ), as is the case under trickle charge conditions, the gate parasitics of the diode connected MOSFETs are the performance limiting parasitics.

Lastly, the analytical model presented was used to determine the most efficient RF energy scavenging circuit design for generating 1 V across a 1 MΩ load at the minimal RF input energy. The optimization was limited to solutions that presented an input impedance which can be matched using L circuits realizable in the typical CMOS processes. The analytical model developed in this work predicted an optimal design with six stacked stages and transistors 62.4 um wide resulting in an efficiency of 25% at an input RF energy of -25 dBm. This is in agreement with the 25% RF to DC conversion efficiency at -25 dBm input RF energy predicted by a harmonic balance simulation using the BSIM 4.0 model of the predicted optimal design.

Chapter 4: Improved RF Energy Harvesting Circuit

Introduction

The ability to harvest energy from the environment could greatly extend the operational lifetime of wireless sensor networks and reduce their size. The small scale of Smartdust sensor nodes (cubic centimeter) necessitates the integration of RF energy scavenging systems directly onto CMOS. However, parasitic sources and physical effects inherent to on chip CMOS integration pose performance limitations and present significant challenges in the design of efficient RF energy scavenging circuits.

Efficient RF scavenging technologies reported in the literature make use of very low loss, high quality surface mount passives and stub tuning networks for external matching to the rectification circuitry [70][92]. However, the aggressive form factor of Smartdust systems makes the use of external impedance matching techniques difficult, facilitating the need for on-chip impedance matching. Given the lossy nature of CMOS passives, on chip integration of the complete RF energy scavenging network poses unique challenges and opportunities for improvement in the design of such systems.

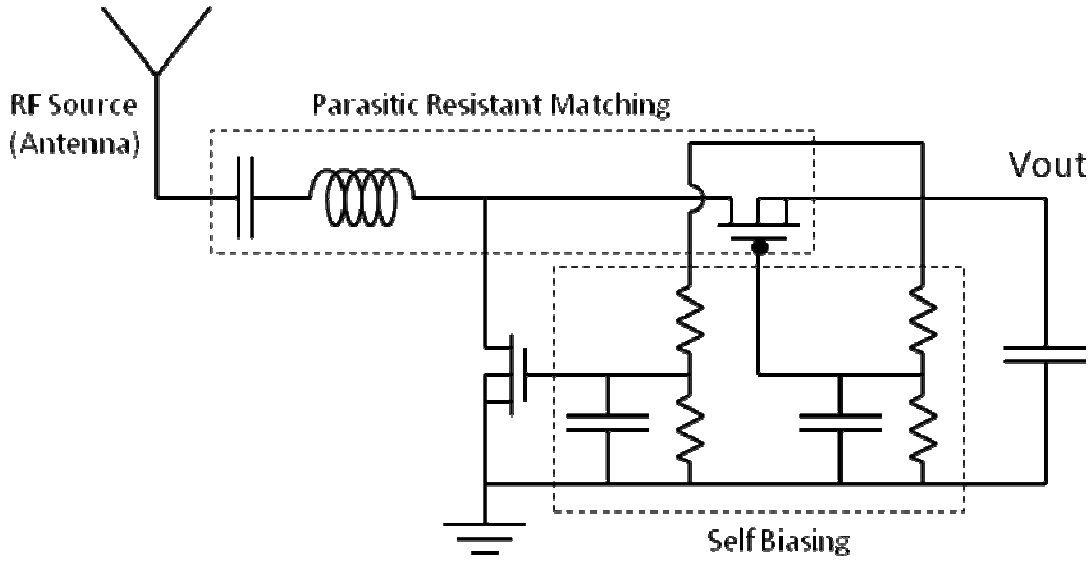


Fig. 57 Improved RF power harvesting circuit

This work presents a modified power matched Villard voltage doubler circuit (Fig. 57) compatible with modern CMOS processes that demonstrates an inherent resistance to the parasitics and performance degrading effects that plague the traditional CMOS implementation of the RF energy scavenging circuit. The modifications presented in this work can be implemented in a typical CMOS fabrication process without any additional mask layers or feature sets. Given the economies of scale in the mass deployment of Smartdust sensor networks, the ability to rely only on features standard to an analog CMOS process would result in significant cost savings.

Design Methodology

The design goal is to generate sufficient voltage and power to operate a wireless sensor node from RF energy levels measured in the environment (66 uW) in a form

factor compatible with Smartdust systems. To meet this requirement, the complete RF scavenging network including matching will be placed on chip. Design consideration will be necessary for the increased parasitics inherent in on-chip inductor and capacitor structures.

Several low power transceiver architectures are available that operate from a supply rail at or below 1 V [15][30][32][33][34][94][95]. Therefore, DC power must be efficiently coupled to a load at 1 V from a source RF energy level as low as 66 uW received due to ambient sources (GSM, FM, ISM, UHF TV bands). The RF to DC conversion design goal was defined as >20% efficiency. At this point, sufficient RF energy is delivered to the out load that a 1 mW transceiver architecture could be operated with a 1% duty cycle. Thus, the RF energy harvesting design could facilitate sustained operations of a Smartdust sensor node near a cell tower, UHF TV source, or dedicated RF power source over an indefinite period of time.

To prevent the RF energy source form interfering with ISM band electronics during testing, 2.2 GHz was chosen as the initial design frequency for the RF energy harvesting circuits. This frequency is also compatible with related research works in Smartdust technology. Parasitics at this frequency are greater than those experienced at 900 MHz and 1.8 GHz, and are comparable to those at 2.4 GHz ISM band. Once RF energy harvesting from ambient RF energy levels is demonstrated, the designs can easily be re-tuned to UHF TV, cellular or ISM bands.

To accomplish this goal, power matched Villard voltage doubler circuits are employed utilizing diode connected MOSFETs [69][92]. Three circuit modifications compatible with CMOS technology are presented for improving the efficiency of the Villard voltage doubler and meeting the required 1 V output voltage at 20% conversion efficiency from 66 uW of received RF energy.

Design Improvements to RF Power Harvesting Circuit

The modified power matched Villard voltage doubler demonstrates a resistance to several key problems that plague the traditional implementation of the Villard voltage doubler. The primary means by which the circuit improves upon the traditional design is through the implementation of a matching network resistant to parasitic losses, through a form of self-biasing to reduce the threshold voltage inherent in diode connected CMOS, and by floating the body of a PMOS to reduce body effect losses.

PMOS with Floating Body to Reduce Body Affect

The traditional implementation of the Villard voltage doubler is implemented with diode connected NMOS (Fig. 58).

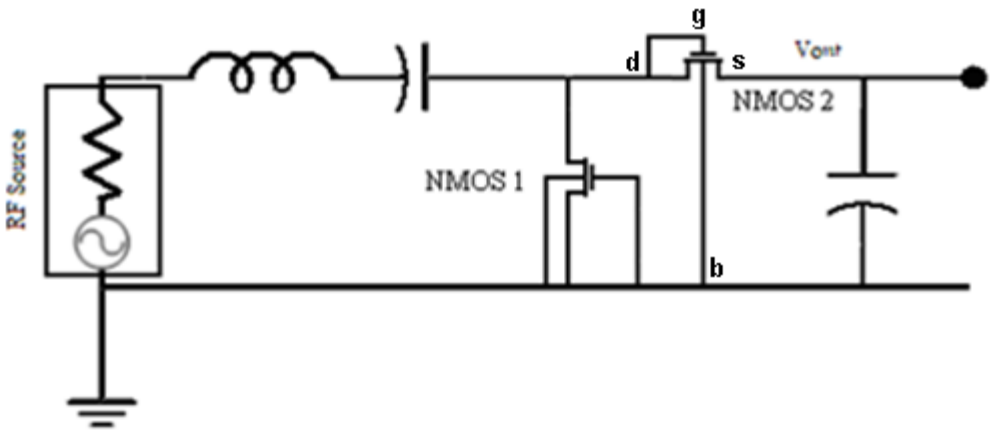


Fig. 58 Conventional RF power harvesting circuit.

Under normal operation, the source of the output diode connected NMOS will float at a voltage higher than the bulk potential. This gives rise to an increase in the threshold voltage of the diode connected MOSFET due to the body effect that is expressed in Eqn. 46 where V_{th0} is the 0 V_{SB} threshold voltage, γ is the body effect parameter, V_{SB} is the potential difference between the source and body, and ϕ is the surface potential of the bulk substrate.

$$V_{th} = V_{th0} + \gamma\left(\sqrt{V_{SB} + 2\cdot\phi} - \sqrt{2\cdot\phi}\right)$$

Eqn. 46. Threshold voltage of a diode connected MOSFET resulting from the body effect.

Therefore, for a conventional Villard voltage doubler implemented in CMOS, higher output voltages cannot be achieved without increasing parasitic losses.

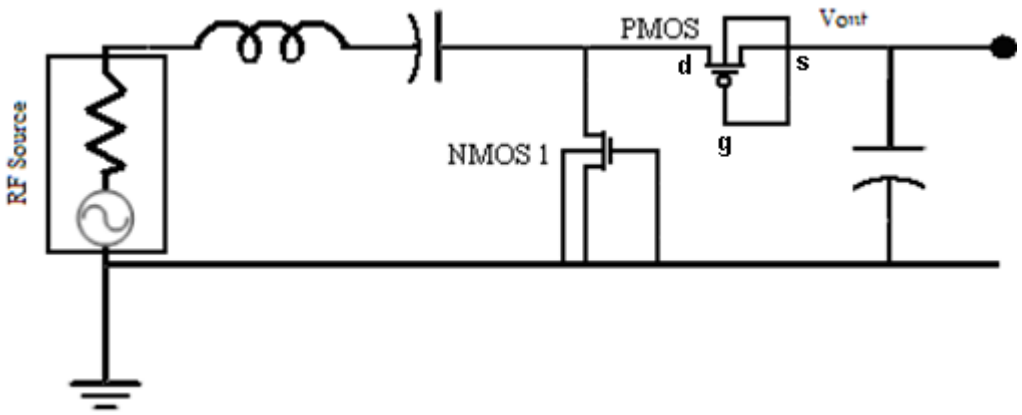


Fig. 59 Power harvesting circuit with NMOS 2 replaced by a PMOS with floating body.

To minimize the body effect, NMOS 2 can be replaced with a diode connected PMOS (Fig. 59). The PMOS has the body, gate, and drain node connected to V_{out} and the source node connected to the voltage at the drain of the diode connected NMOS. The body effect of NMOS 1 is already minimized and is treated exactly as in the previous circuit. The PMOS only conducts when the gate is below the source. Since the gate has been connected to V_{out}, this occurs when the AC voltage at the input is positive with respect to ground. Since both the body and the source of the PMOS are connected to V_{out} there is no increase in the threshold voltage due to the body effect.

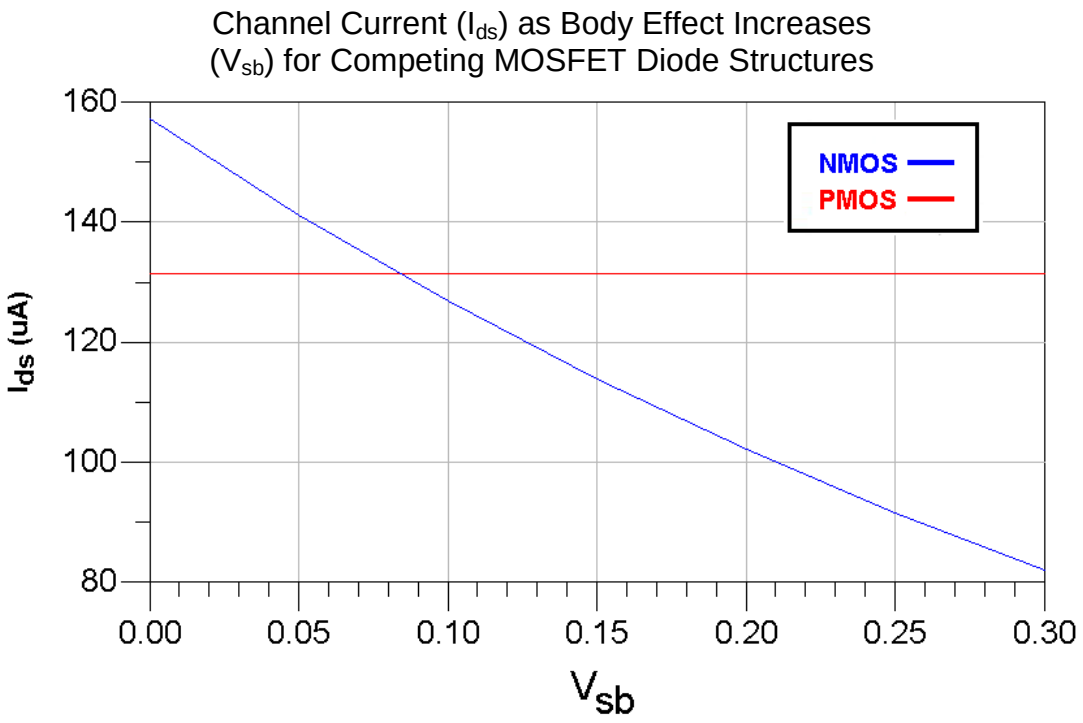


Fig. 60 Improvement to drain current (I_{ds}) for a given V_{ds} (.3V) as V_{bs} is varied for a diode connected PMOS (27.2 um/.25 um) and diode connected NMOS 2 (13.6um / .25um) as depicted in Fig. 58 and Fig. 59.

Fig. 60 illustrates that when the body effect is minimal (V_{sb} < .08 V), the diode connected NMOS (13.6 um / .25 um) demonstrates superior I_{ds} (stronger turn on) for a given V_{ds} (.3 V). However, as the body effect is increased (V_{sb} > .08V), the diode connected PMOS (27.2 um / .25 um) demonstrates superior I_{ds} (turn on current) for a given V_{ds} (.3V). V_{sb} is the potential difference between the source of the MOSFET and the bulk silicon substrate. In the case of the diode connected NMOS, the bulk is also the body of the device.

In order for this design to work, it is critical that there is sufficient isolation that the body of the PMOS can be connected to V_{out} without any current flowing from the

PMOS body to the bulk substrate. The body of a diode connected PMOS can be connected to V_{out} due to the fact that PMOS FETs are placed in an n-type doped well inside of the p-type substrate.

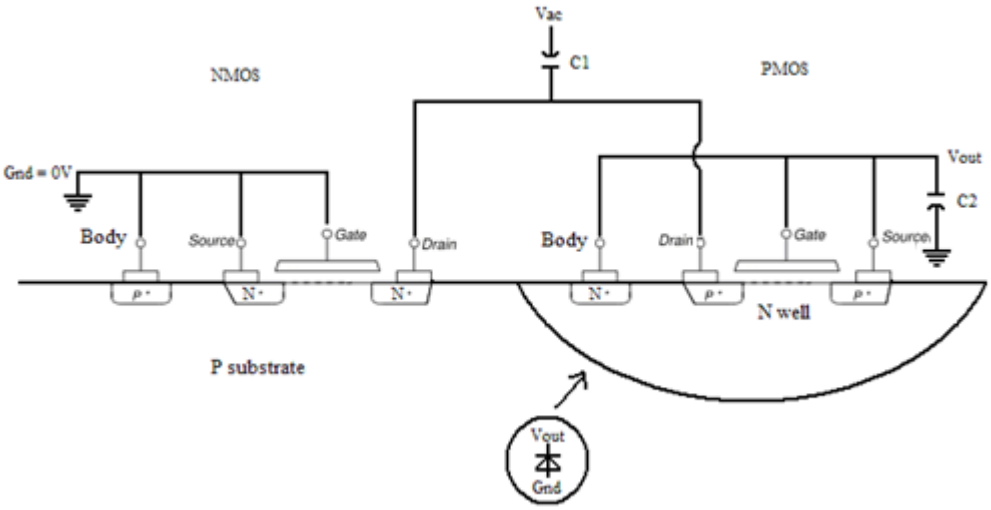


Fig. 61 Layout of NMOS and PMOS device with appropriate connections for RF power harvesting circuit indicated. The voltage across the PN junction is labeled to show how diode is reverse biased and current will not flow under operating conditions since V_{out} is always greater than the circuit ground.

As seen in Fig. 61, PMOS is built in an N well. Since the junction from the N well to p substrate acts as a diode, if the voltage potential in the N well is higher than the voltage potential in the P substrate, current will not flow. Generally, proper biasing of the n type well is achieved by connecting to a positive externally applied supply voltage. Such a source does not exist in this application. However, for the proposed Villard voltage doubler, V_{out} is at an inherently greater potential than the substrate voltage since the output voltage is a result of the positive rectification of the incident AC signal and as a result satisfies the biasing requirements of the n type well. The junction capacitance between the n type well and the substrate is parallel to and is

several orders of magnitude lower than output capacitance (C_2) of the Villard voltage doubler. Therefore, it has no significant effect on the circuit performance.

Parasitic Resistant Matching Network.

Power matching is an important step in maximizing the conversion efficiency of an RF energy harvesting circuit.

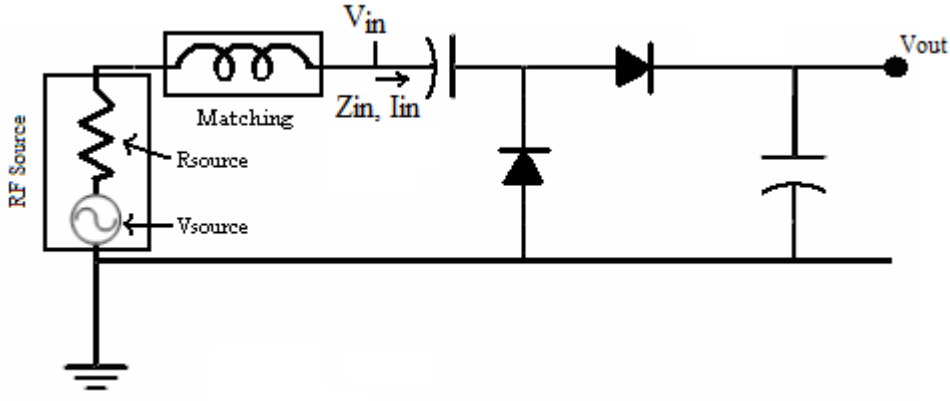


Fig. 62 Villard voltage doubler power matched to RF source.

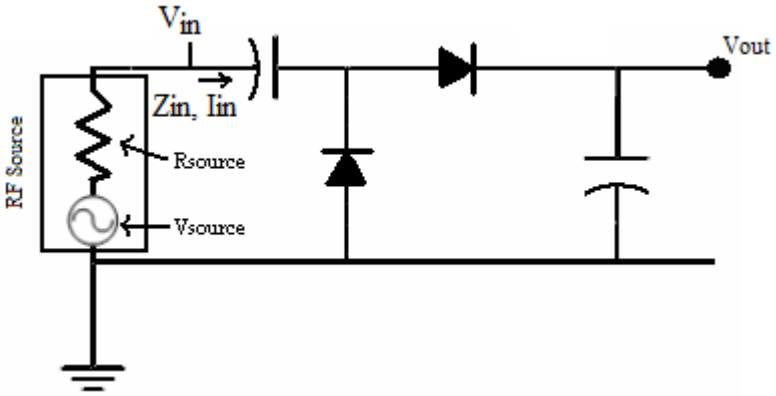


Fig. 63 Villard voltage doubler not power matched to RF source.

To illustrate, the output voltage resulting from the power matched Villard voltage doubler presented in Fig. 62 is derived in Eqn. 47 and the output voltage resulting from an unmatched Villard voltage doubler as presented in Fig. 63 is derived in Eqn. 48.

$$V_{output} = V_{source}\sqrt{\frac{|Z_{in}|}{R_{source}\cdot\cos(\phi)}} - 2\cdot V_{th}$$

Eqn. 47. Output voltage of the Villard voltage doubler resulting from the RF power source depicted in Fig. 62 (Derivation Appendix A).

$$V_{output} = 2\cdot V_{source} - 2\cdot V_{th}$$

Eqn. 48. Output voltage of the Villard voltage doubler unmatched to the RF power source depicted in Fig. 63.

Eqn. 48 assumes $|Z_{in}| >> R_{source}$ which is true when the diode connected MOSFETs in a Villard voltage doubler circuit are not strongly forward biased. This is common under low incident power conditions (sub milliwatt). From Eqn. 47 and Eqn. 48, relationship Eqn. 49 can be derived, indicating under what conditions the output voltage will be greater when power matching is applied.

$$\sqrt{\frac{|Z_{in}|}{R_{source}\cdot\cos(\phi)}} > 2$$

Eqn. 49. Conditions under which the power matched Villard voltage doubler will outperform a non power matched Villard voltage doubler (Derivation Appendix A).

This relationship demonstrates the necessity of impedance matching to the RF power source (generally an antenna) as $|Z_{in}|$ increases and ϕ, the phase difference between the real and imaginary components of the input impedance, approaches 90 degrees. The input impedance of a Villard voltage doubler (Z_{in}) operating at RF frequencies with a low incident power represents a large and reactive impedance that is orders of magnitude larger than the source impedance of a typical power source such as an antenna. Thus, power matching is a critical element in the design of an RF energy harvesting circuit.

Given the importance of power matching to maximize RF to DC conversion efficiency, care must be applied in the design of the power matching circuit to minimize parasitic losses. Fig. 64 illustrates a typical impedance matching design and the resulting parasitics.

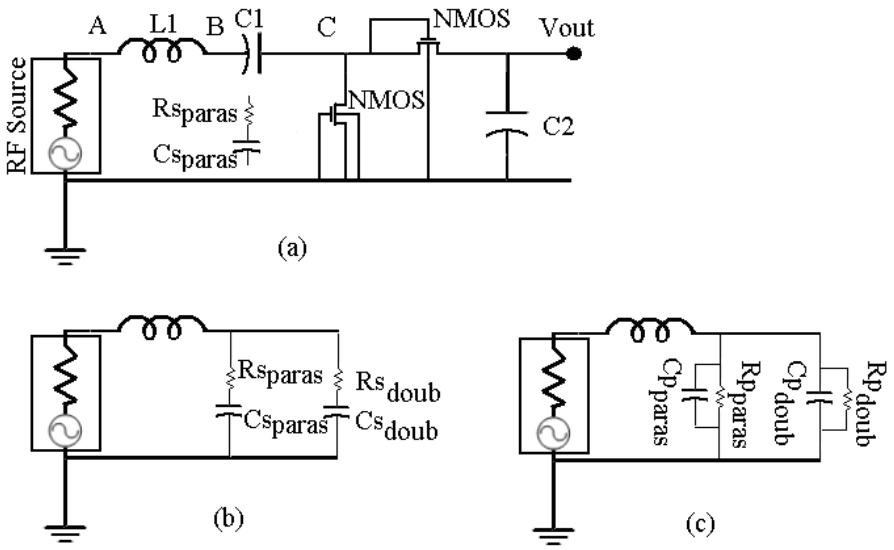


Fig. 64 Step-by-step simplification of equivalent effective circuit impedance of conventional matching circuit.

In the presence of the parasitics inherent in CMOS design, a significant performance enhancement can be achieved by moving the impedance matching inductor into the Villard voltage doubler as illustrated in Fig. 65. While theoretically these two schematics are equivalent, it becomes apparent after examination of the parasitics incurred during layout that the schematic in Fig. 65 is inherently less sensitive to the parasitics associated with the capacitor C1.

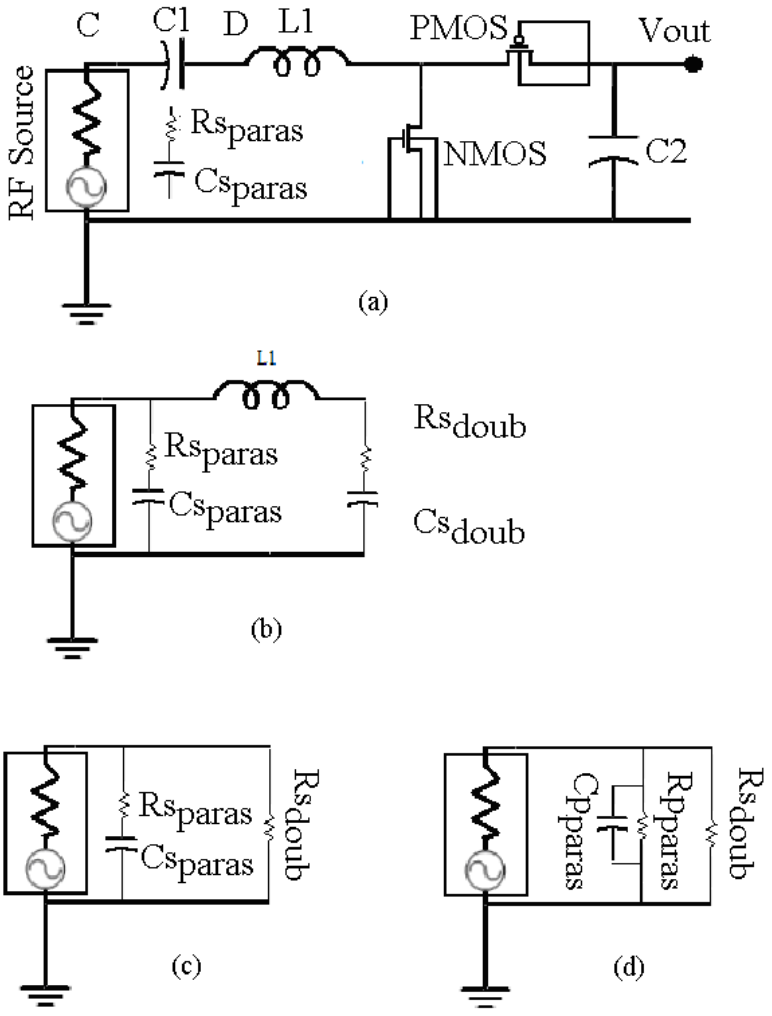


Fig. 65 Step-by-step simplification of equivelent effective circuit impedance of parasitic resistant matching circuit.

The impedance of the voltage doubler at point C in Fig. 64a is dominated by the junction capacitance of the diode and is highly reactive. C1 is orders of magnitude higher than the junction capacitance, therefore, it appears as a short at the RF frequency. The impedance at point B is also large and reactive. The parasitic resistance and capacitance of C1 results in a complex impedance parallel to the input impedance at point B (Fig. 64b). Both the parasitic complex impedance of C1 (Rs_{para}, Cs_{para}) and the complex impedance of the voltage doubler (Rs_{doub}, Cs_{doub}) presented at point B can be converted to the equivalent parallel resistive and capacitive components as is done in Fig. 64c. The parallel resistance of the Villard voltage doubler (Rp_{doub}) is comprised primarily of the effective source to drain resistance of the diode connected MOSFETs. Under low power conditions, the diode connected MOSFETs are only weakly forward biased and the channel resistance which comprises Rp_{doub} is greater than the equivalent parallel impedance of the parasitic resistance (Rp_{para}). Thus, significant current flows across the parasitic resistance representing a power loss and results in a reduction in RF to DC conversion efficiency.

Alternatively, this work proposes a parasitic resistant matching network by implementing the DC block capacitor, the source of the parasitic losses, prior to the power matching circuitry as indicated in Fig. 65a. Compatibility with gate tie down requirements and antenna rules are preserved through the application of a PMOS with a floating body.

For the parasitic resistant matching network proposed in Fig. 65a, it can be seen that the reactive part of the impedance at points C and D has been tuned out, putting the series resistance (Rs_{doub}) presented by the voltage doubler in parallel with the parasitic impedance (Rp_{para},Cp_{para}) of capacitor C1 (Fig. 65d). The relationship between Rs_{doub} and Rp_{doub} can be derived as a function of the series capacitance of the Villard voltage doubler (Eqn. 50).

$$Rp_{doub} = Rs_{doub} \cdot \left(1 + \left(\frac{1}{\omega \cdot Rs_{doub} \cdot Cs_{doub}}\right)^2\right)$$

Eqn. 50. Effective parallel resistance of the Villard voltage doubler.

At RF frequencies (> 100 MHz), typical values for the real (Rs_{doub}) and capacitive impedance (Cs_{doub}) of the voltage doubler result in $Rp_{doub} >> Rs_{doub}$. As a result, even under low power conditions where the diode connected MOSFETs are not strongly forward biased, Rs_{doub} is orders of magnitude smaller than Rp_{para}. Thus, very little power is lost to current flow across Rp_{para} and the parasitic resistant matching network proposed in Fig. 65 shows superior performance to the conventional power matched Villard voltage doubler in Fig. 64.

It should also be noted that modern CMOS fabrication processes require that a certain ratio of gate tie downs to metal area be maintained. Connecting the inductor directly to the gate of an NMOS in a Villard voltage doubler would require an unrealistic number of tie down contacts. Therefore, this technique is only suitable for designs

that use a PMOS with gate and body tied to the output as opposed to a NMOS which would result in the inductor tied directly to the gate.

Sacrificial Biasing

In the typical implementation of the Villard voltage doubler, the gate threshold voltage of the diode connected MOSFET limits the conversion efficiency of the RF power harvesting circuit. Work by Mandal and Sarpeshkar utilizes floating gates to reduce the threshold voltage of diode connected MOSFETs [92]. This technique relies on the availability of a second polysilicon layer which is not a feature commonly found in CMOS processes, and when available, incurs additional cost. Thus, this approach is not economical for wireless sensor networks consisting of a large number of nodes in which the cost of individual nodes must be kept to a minimum.

In addition, previous works have attempted to improve RF power harvesting efficiency by using special MOSFETS with reduced gate threshold voltages [69],[74]. However, as is the case with a second polysilicon layer, low threshold voltage MOSFETs are a feature available only at additional cost during fabrication.

The solution proposed by this work achieves the performance gains of threshold reduction techniques without the additional expense of costly fabrication options. To achieve this, the work presented reduces gate threshold voltage through the sacrifice

of minimal amounts of output current to generate a bias at the gates of the diode connected MOSFETs. This technique is immune to the reliability concerns and requirement for a second polysilicon layer that plague biasing implementations utilizing floating gates [92].

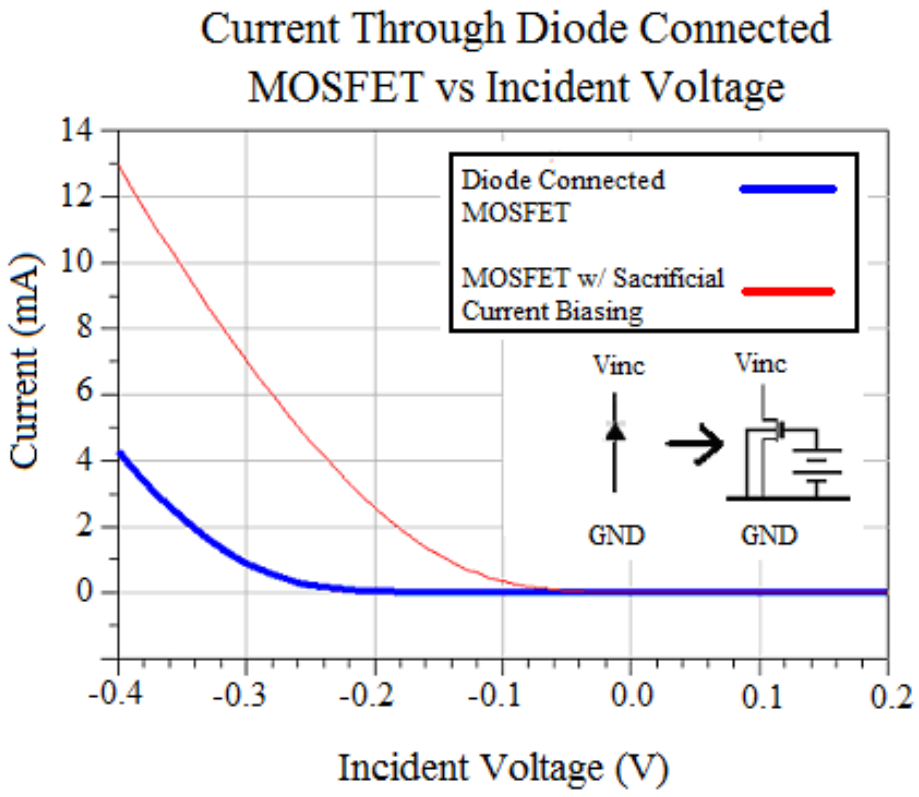


Fig. 66 Plot illustrating the reduction in turn on voltage for diode connected MOSFET with gate biasing versus a standard diode connected MOSFET.

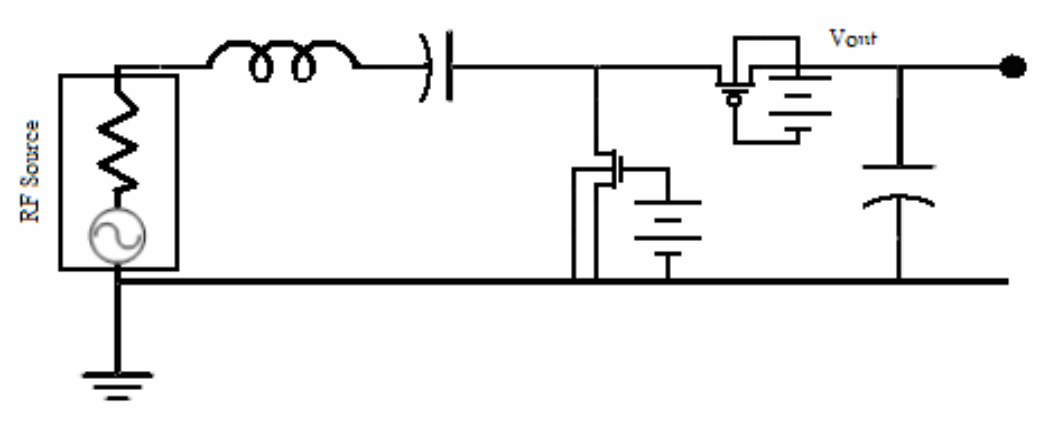


Fig. 67 Biasing the gate of diode connected MOSFETs to reduce the threshold voltage.

Fig. 66 illustrates the concept by plotting current through the diode connected MOSFET when the diode structure is forward biased as V_{inc} falls below the circuit ground. By applying a DC bias to the gates of both diode connected MOSFETs (Fig. 67), the turn on threshold voltage can be reduced. Since a PMOS with floating body has been implemented, both gates are connected to DC nodes. The gates act as an open load at DC and no power is lost to the parasitics of the gate.

This approach does increase the leakage current while the diode connected MOSFET is reverse biased, but this current is orders of magnitude lower than the forward biased current. Therefore, the MOSFET that is forward biased dominates the current flow.

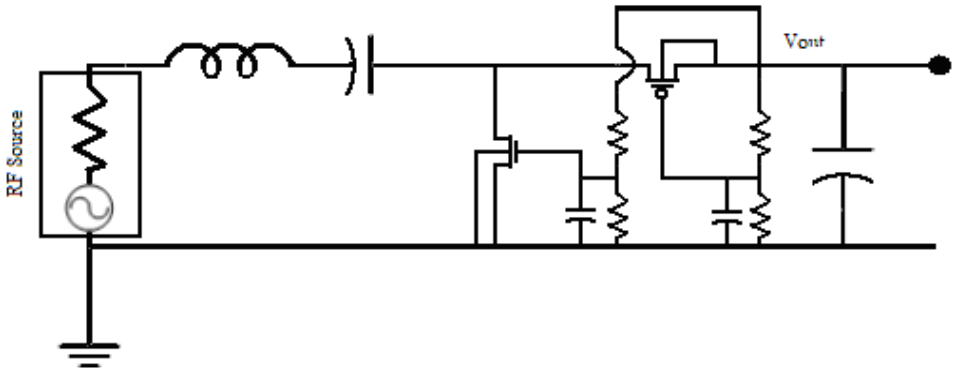


Fig. 68 Circuit design illustrating the use of sacrificial current biasing to reduce the threshold voltage of diode connected MOSFETs.

Although possible, in practice it is not suitable to hang voltage sources off of the gates of the diode connected MOSFETs in the RF power harvesting circuit. A more practical approach is to use the desired output voltage to create the bias voltages through a voltage divider network (Fig. 68). This technique sacrifices some current to create an overall improvement to system efficiency. Again, it is necessary to replace one of the diode connected NMOS with a floating body PMOS for two reasons. The first is that the threshold voltage of the output diode connected MOSFET must be below V_{out} to be obtainable through a voltage divider network. The second reason is so that the gate is connected to a DC node in the circuit.

Sufficiently larger resistors are used in the divider network to reduce power dissipated due to the bias current. This power dissipated can be designed to be orders of magnitude below the increase in output power due to the application of a bias voltage. Practical limitations are placed on the size of the resistors used in the divider network due to an increase in the time necessary to achieve steady state. This is a direct result

of the RC time constant of the voltage divider network and gate capacitance. This approach does increase the leakage current while the diode connected MOSFET is reverse biased, but the bias point is chosen to keep the power lost to leakage currents less than the power gained through a reduction in threshold losses.

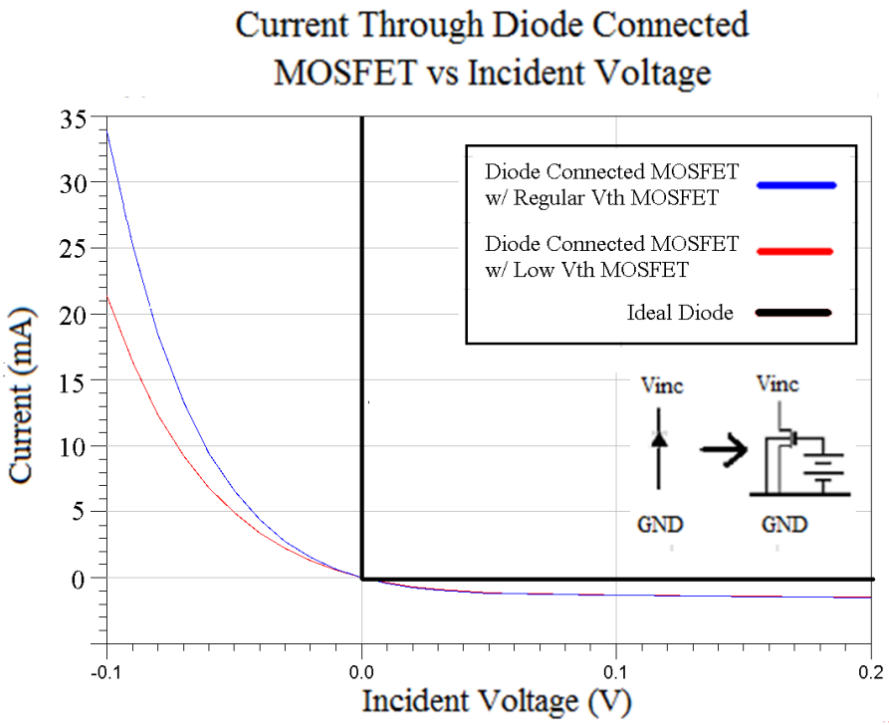


Fig. 69 Ideal diode response vs diode connected MOSFET with regular FETs and diode connected MOSFET using low threshold voltage FETs.

Previous work in the literature has concluded that the use of low threshold voltage MOSFETs provides the best performance for RF power harvesting [69]. This work challenges that assertion by demonstrating that the proposed technique enables traditional MOSFETs to outperform low threshold voltage MOSFETs. This is because the ability of sacrificial current biasing to reduce the threshold voltage of a MOSFET is limited due to the finite slope of the I-V curve resulting from the non-

ideal transition of the diode connected MOSFET from an open to a closed circuit. This is illustrated in Fig. 69. Regular MOSFETs have a sharper transition than low threshold voltage MOSFETs, resulting in a faster turn on when transitioning to the open state, and therefore, show better RF conversion efficiency since propoer biasing can effectively remove most of the threshold voltage.

Design and Simulation

RF power harvesting circuits were designed and simulated using the IBM 130 nm CMOS process. The circuit was designed to be capable of powering a low power transceiver indicative of that found in a Smartdust system [33][94][95]. Given this goal, the systems were designed to generate 1 V across a 70 kΩ load from less than 66 uW of input RF power at 2.2 GHz. Due to the presence of minimal RF energy from consumer electronics, 2.2 GHz was chosen so that the amount of RF energy received could easily be controlled. This is important for testing due to the flood of RF energy in the environment at 900 MHz, 1.8 GHz and 2.4 GHz from wireless electronics.

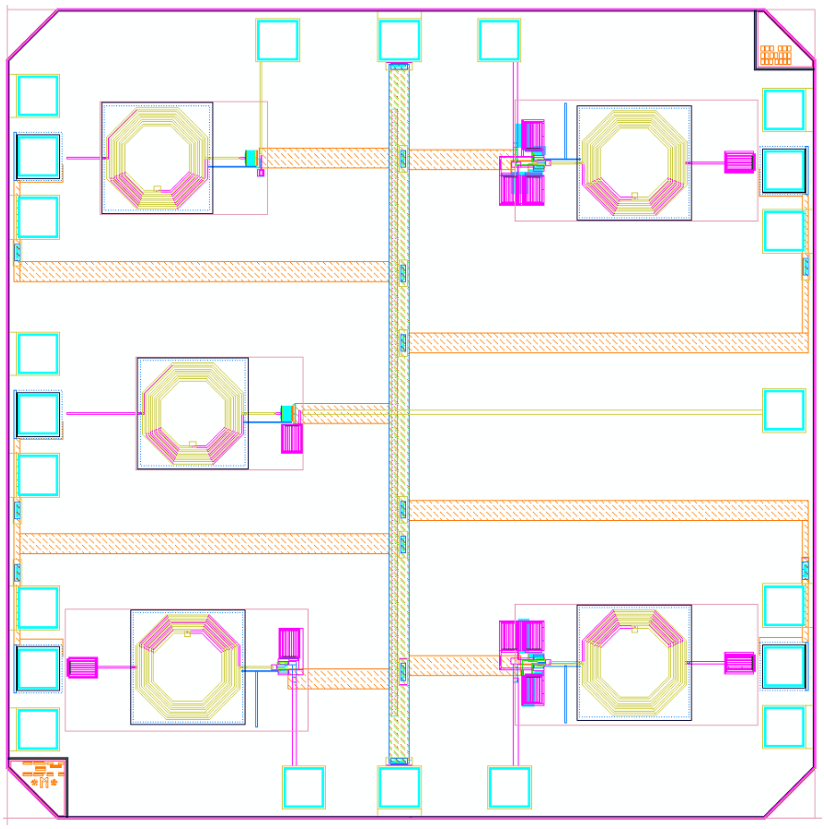


Fig. 70 Image of test chip layout with RF power harvesting circuits comprised of various combinations of the design improvements discussed in this work. Design was implemented in a 130 nm IBM process.

Four RF power-harvesting circuits were designed, simulated, and laid out for comparison. The reference design utilized a vertical natural capacitor at the input of the voltage doubler to meet layout requirements and prevent forward biasing of the tie down diodes that are required for Metal-Insulator-Metal (MIM) capacitors. MIM Caps were used for all other designs since forward biasing of the required tie down diodes would not occur for these designs. Low threshold voltage MOSFETs were utilized unless otherwise noted. The largest design utilizing all three design improvements took up only 600 um by 300 um of total chip space.

RF Energy Harvesting Circuits Tested:

1. Reference design with no improvements.
2. Design utilizing a PMOS with floating body and the parasitic resistant matching network.
3. Design utilizing all three improvements with low threshold voltage MOSFETs
4. Design utilizing all three improvements with normal threshold voltage MOSFETs

All designs utilized an on chip impedance matching network to match to the imaginary and real components of the voltage doubler impedance. The predicted results from simulation are given in TABLE III. A combined improvement of 113% was predicted over the reference design of a conventional RF power harvesting circuit.

TABLE III OUTPUT VOLTAGE AND EFFICIENCY OF PROPOSED RF POWER HARVESTING CIRCUITS.

Improvement	Matched Impedance (ohms)	Vout	Pin (uW)	Pout (uW)	Efficiency	Percent Increase Over Reference
Reference	72	0.707	66	7.14	10.8%	
PMOS+ Matching	94	0.943	66	12.7	19.24%	80%
PMOS + Match + Bias	110	1.007	66	14.49	21.95%	103%
PMOS + Match + Bias + Regular Vth FET	104	1.03	66	15.16	22.97%	113%

Measurements

These circuits were taped out and fabricated in an IBM 130nm run utilizing the 3-2 DM metal stack (Fig. 71).

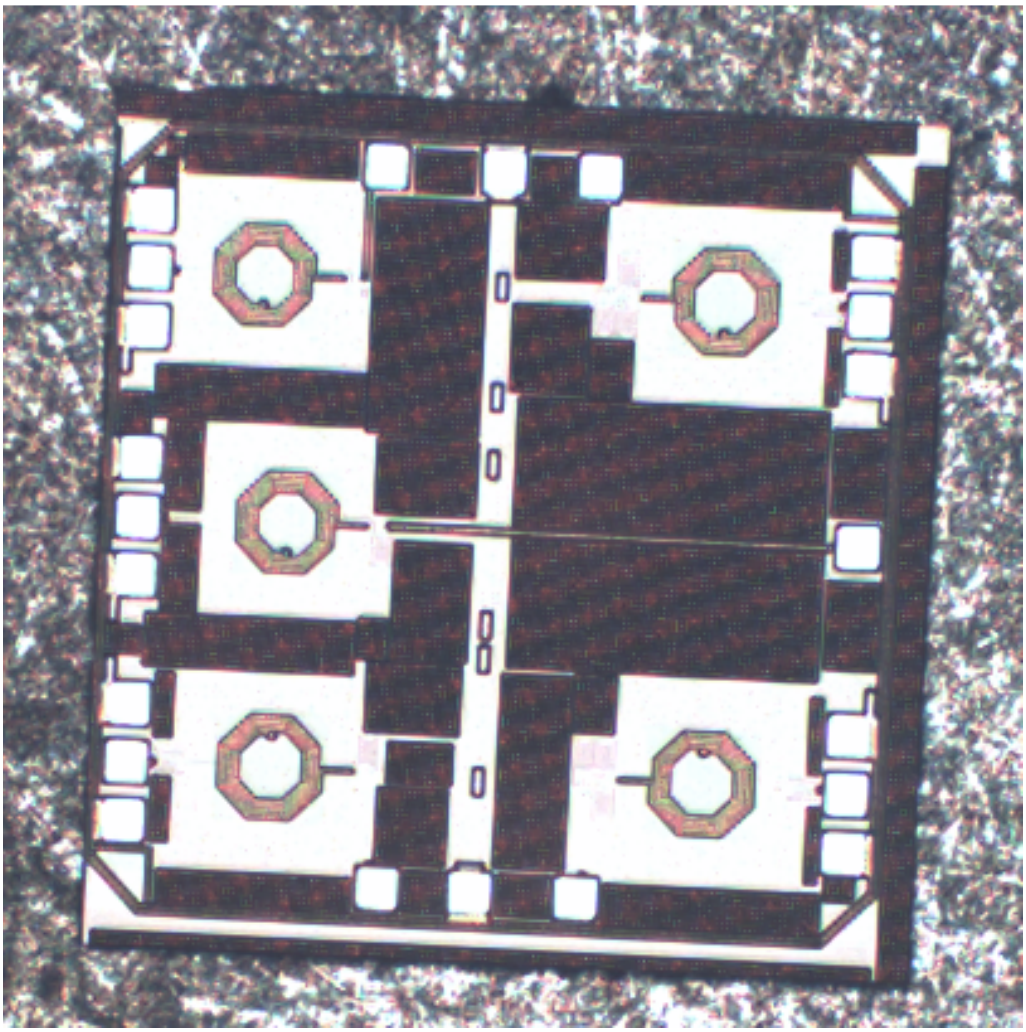


Fig. 71 Image of test chip with RF power harvesting circuits comprised of various combinations of the design improvements discussed in this paper. Design was fabricated in a 130 nm IBM process.

This process provides for higher performance inductors and metal-insulator-metal capacitors. Careful attention was paid towards meeting metal fill requirements without adding unnecessary parasitics in the presence of the inductors. Gate tie down

requirements were met at DC nodes to prevent losses due to parasitic capacitive losses from the tie down diodes.

TABLE IV COMPARISON OF MEASURED AND SIMULATED RESULTS OF RF POWER HARVESTING CIRCUIT TESTING.

Improvement	Unmatched Pin (uW)	Sim. Vout	Measured Vout	Simulated Efficiency	Measured Efficiency	Percent Increase Over Measured Reference
Reference	61.6	.672	0.658	10.5%	10.0%	
PMOS+ Matching	56.2	.844	0.82	18.1%	17.1%	71%
PMOS + Match + Bias	54	.888	.889	20.9%	20.9%	109%
PMOS + Match + Bias + Regular Vth FET	55.6	.930	.938	22.2%	22.6%	126%

TABLE IV shows that at 2.2 GHz, the output voltage and RF to DC power conversion efficiency show excellent agreement between simulation and measured results. The measurements verified that the input impedances were within 3 Ωs of the impedance predicted by simulation. The input power ranged from 54 uW to 61.6 uW and was a function of the RF source power (66 uW) minus the cable loss and impedance mismatch loss between the RF energy scavenging network and the 50 Ω power source.

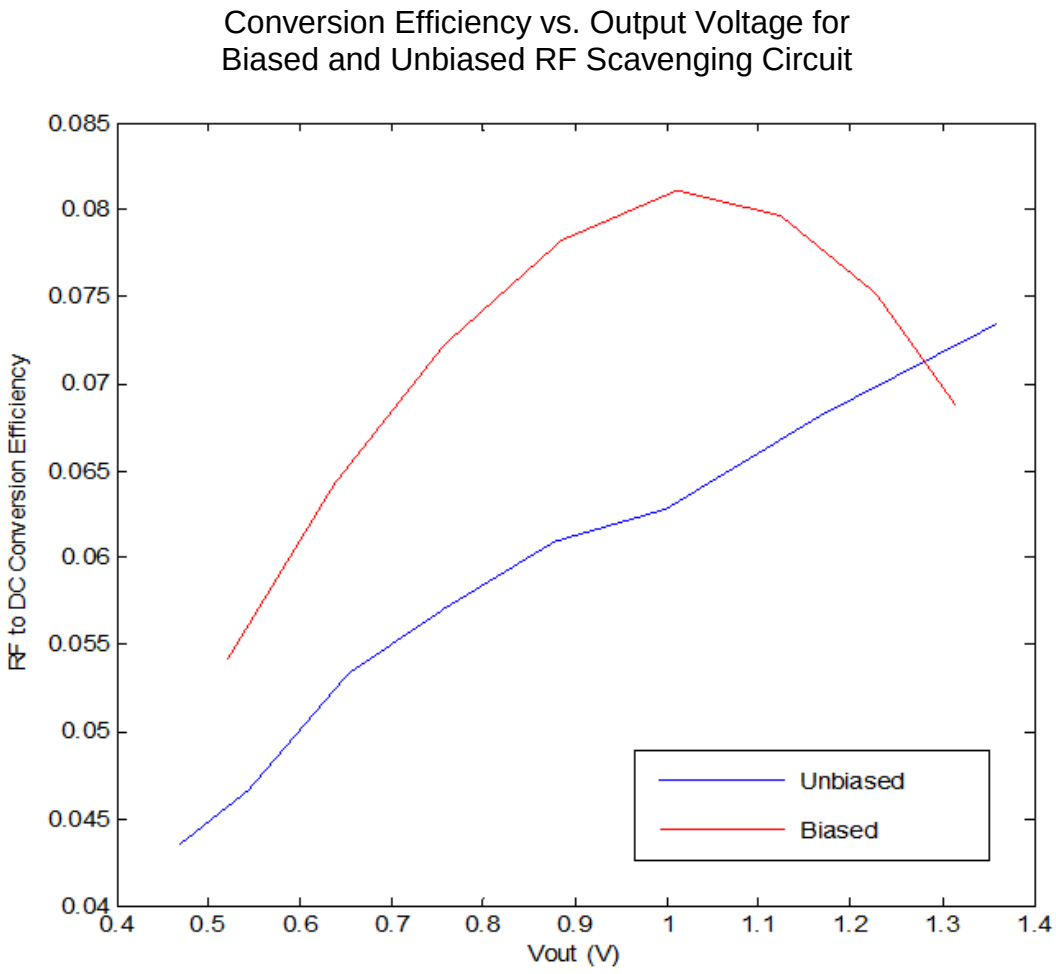


Fig. 72 Comparison of measured RF to DC conversion efficiency vs output voltage across a 200 kΩ load for both an RF energy harvesting circuit with biasing and without biasing.

It's worth noting that unlike the improvements to reduce the body effect and matching circuit parasitics, sacrificial current biasing is optimized for a given output voltage. As increased input RF energy results in an output voltage higher than the optimal output voltage, the diode connected MOSFET's leakage current increases.

This is a consequence of larger output voltages resulting in larger bias voltages on the gate preventing the diode connected MOSFET's from ever fully turning off. Fig. 72 shows that efficiency is at a peak at the optimal output voltage of 1 V. The optimal output voltage is the output voltage that the biasing network was designed to operate at.

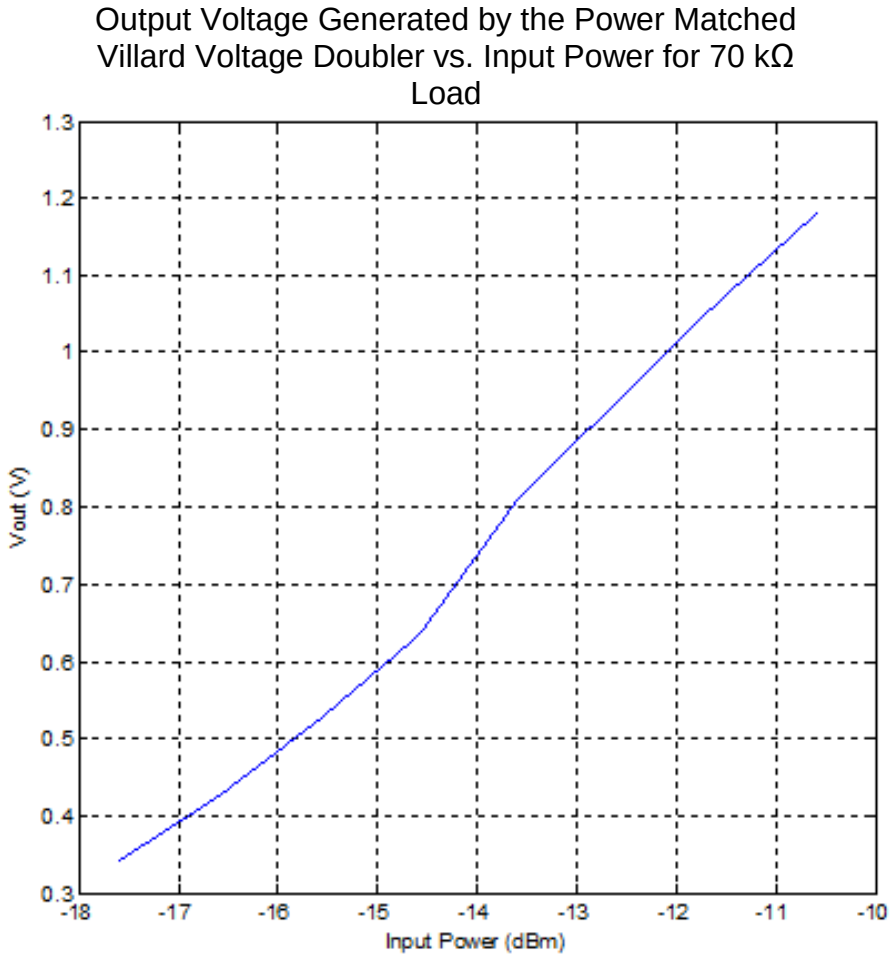


Fig. 73 Measurement of V_{out} vs input power for the RF energy harvesting circuit utilizing all design improvements with a 70 kΩ load.

The design goal was to generate 1 V across a 70 kΩ load from 66 uW (-11.8 dBm) of input RF energy. As indicated in Fig. 73, that design goal was met with 1.02 V generated from a 66 uW source resulting in 22.5% RF to DC conversion efficiency.

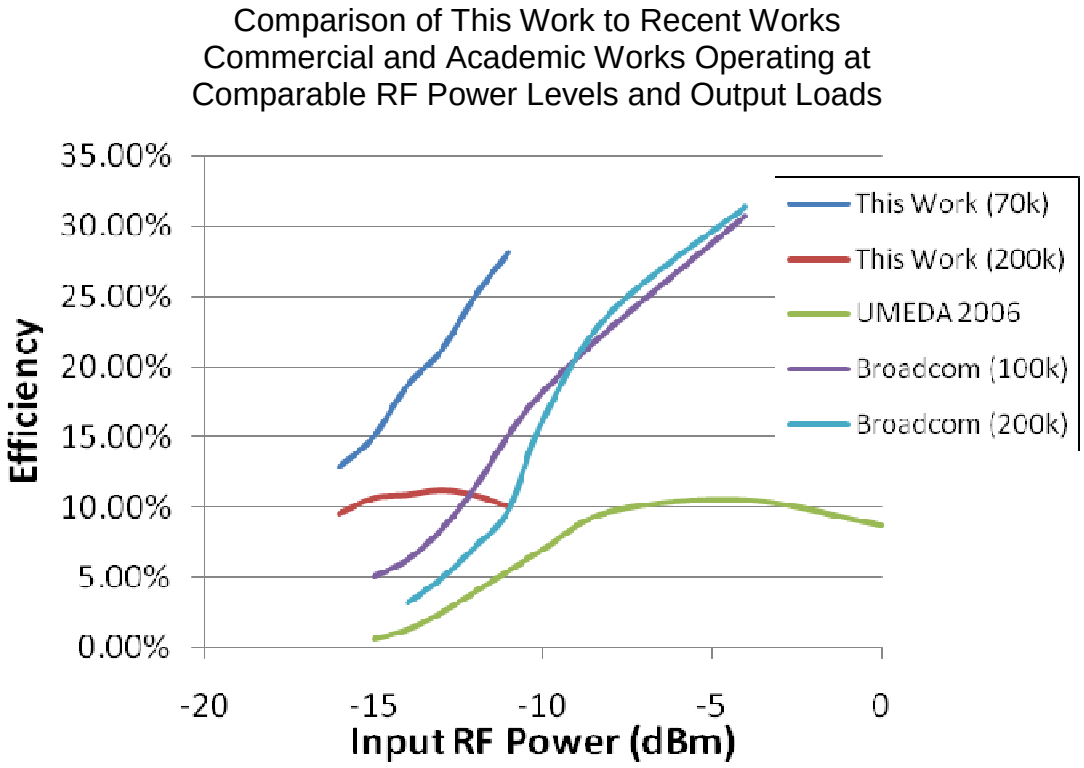


Fig. 74 Comparison of this work to recent works commercial and academic works operating at comparable RF power levels and output loads

As demonstrated by Fig. 74, this work compares well with other recent works both in the academic and commercial communities designed to operate at comparable RF energy levels and output loads. This work demonstrates two to three times the RF to DC conversion effieincy of the RF energy scavenging system by the commercial RF wireless IC design company, Broadcom [96] and about ten times the performance of the academic work reported by Umeda et al [97].

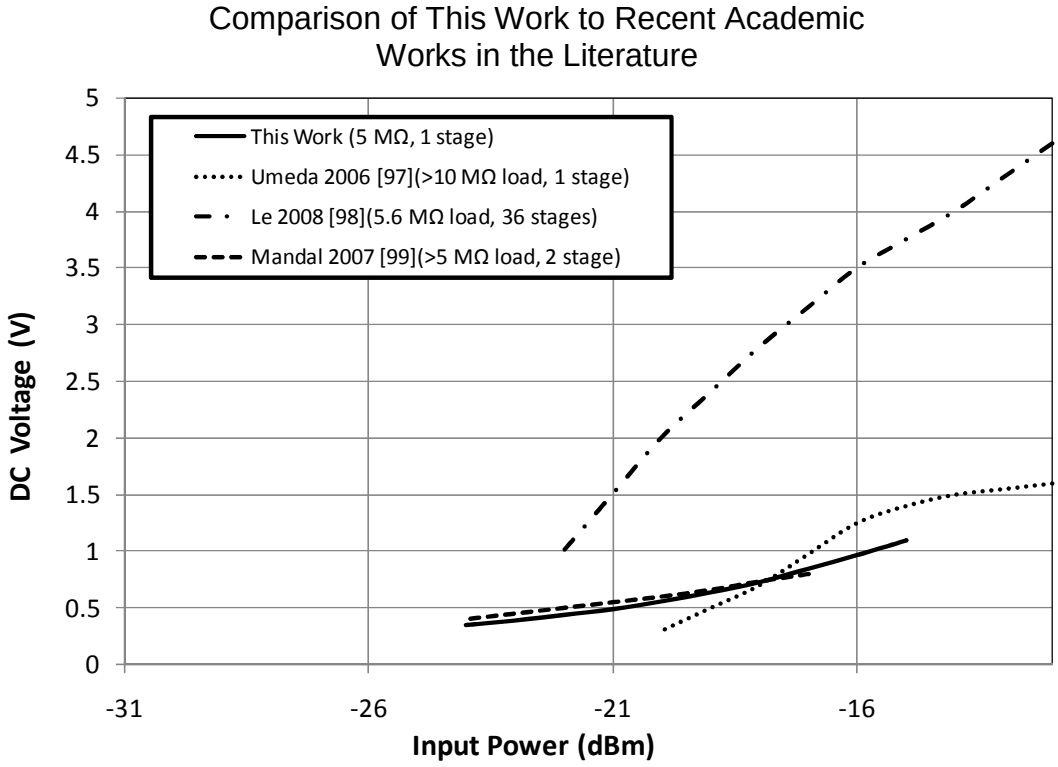


Fig. 75 Comparison of this work to recent works tested under similar output loads and input power conditions.

Comparisons to prior work in the field can be difficult since performance is often measured at different input power and output load conditions. However, despite the fact that this work was optimized for operation at about -12 dBm input RF power, and operates at over twice the RF frequency (2.2 GHz vs 900 MHz) which results in more parasitic loss, this work compares well with prior recent academic works that were optimized for very low input RF power levels (Fig. 75).

Conclusions

This work successfully demonstrates that despite restrictions inherent in the aggressively small form factor of Smartdust systems, the voltage and power levels necessary to operate Smartdust sensor nodes can be generated from RF energy scavenging. Several improvements to the standard power matched Villard voltage doubler enable 1 V to be generated with greater than 22% efficiency from RF energy levels as low as -12 dBm while utilizing all on chip components. This is twice the efficiency of the reference power matched Villard voltage doubler RF energy harvesting circuit. The system consumes only .18 mm^2 of chip space while integrating all necessary impedance matching circuitry directly onto the CMOS chip. Furthermore, the improvements presented in this paper can be implemented with the features standard in any CMOS process, reducing the cost of large scale deployments of RF energy scavenging technology.

This research demonstrates significant increases in the performance of RF power harvesting integrated completely onto CMOS. With these performance increases, a Smartdust system could potentially operate off of the ambient RF energy in the environment due to cellular/television networks and wireless consumer electronics. With recent advancements in on-chip antenna design [100][101], coupling this RF energy harvesting system to a novel 1 V battery chemistry [102] would enable a Smartdust node to self recharge from received RF emissions and provide continuous, sustained operations for an indefinite period of time while occupying less than a cubic centimeter of space.

Chapter 5: Improved Low Power Receiver Architecture

Introduction

Smartdust networks are characterized by the ad-hoc distribution in an area of many dust size sensor devices. Ad-hoc distribution results in the non-optimal orientations and placements of wireless nodes. Therefore, the physical layer implementation of the transceiver must have a link margin sufficient to bridge air gaps even when $1/r^3$ path loss is encountered [16]-[20]. Given the 10 m transmission distance characteristic of sensor networks [30], this results in up to 90 dB of path loss for transmission in the ISM bands. Despite efficient power amplifier designs (>30%) [32],[103], the limited power delivery capability of miniature battery technology places an upper boundary on the output power of the transmitter to a few mW [34]. Furthermore, the random orientation of the transceiver necessitates a monopole antenna design, limiting antenna gain. Thus, the ability to meet a 90 dB link margin to overcome $1/r^3$ path loss over ten meters is largely a function of the receiver sensitivity.

Because these networks must often operate in areas without any pre existing infrastructure, they are typically required to operate for extended periods of time on single battery charge. Unlike existing wireless networks, wireless sensor networks have minimal bit rate requirements. These requirements are typically on the order of bits per day [1]. Therefore, wireless sensor nodes spend the majority of time ready to receive data as opposed to actively transmitting data [34]. Such low channel

utilization results in a transceiver dominated by the average power consumption of the receiver architecture.

Given that average transceiver power consumption and link margin is largely dominated by the performance of the receiver, careful design and optimization of the receive architecture will have the most impact on the performance of a wireless sensor network. For this reason, this work identifies the performance limiting features of the non-coherent OOK receiver, proposes a receiver architecture to reduce these performance limitations, and presents a methodology for optimizing the multistage LNA of the receiver to meet a sensitivity requirement with minimal total power consumption.

Design Methodology and System Architecture

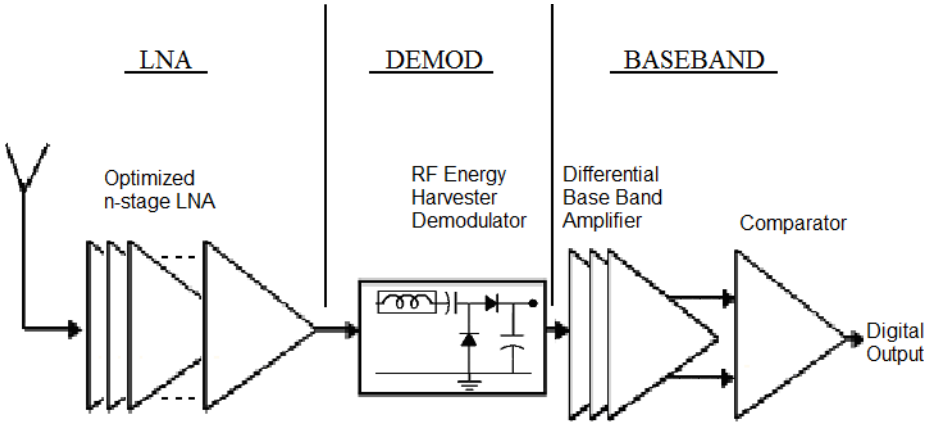


Fig. 76 Proposed low power receiver architecture implementing RF energy scavenging circuit for demodulation and an optimized multi-stage LNA.

To meet sensitivity requirements at the lowest possible power consumption, the non-coherent on-off keying (OOK) receiver architecture in Fig. 76 is proposed. OOK is less spectrally efficient than the more common phase-shift keying (PSK). However, OOK can be implemented in a non-coherent architecture. Therefore, it provides opportunities to reduce power consumption [94].

To provide reliable communications over 10 m distances in the presence of $1/r^3$ path loss, the receiver must meet a -90 dBm sensitivity at 1 Mbps. A BER of 10^{-3} necessitates a peak SNR of better than 17 dB for a non coherent OOK receiver, and thus, a receiver noise figure (NF) of 7 dB is necessary to meet the performance goal (Eqn. 51).

$$NFreceiver = Sensitivity_{dBm} + 174\,dBm - BW_{dB} - S/N_{dB}$$
$$NFreceiver = -90 + 174 - 60 - 17 = 7\ dB$$

Eqn. 51. Required NF of the reciever to meet the -90 dBm sensitivity requirement for OOK receiver operating with a 10^{-3} BER. 1 MHz receiver bandwidth is assumed.

The receiver was implemented at a carrier frequency of 2.2 GHz to maintain compatibility with several Smartdust related research works [101][104][105], but could easily be implemented at the 2.4 GHz ISM band. To enable operation from ultra small batteries and minimize power consumption, the receiver was designed to operate from a 1 V supply rail. In addition, to meet the mm^3 scale dimensions required for Smartdust systems, no external passives were used.

Eqn. 52 applies the Friis formula to determine the noise figure of the receiver for the proposed non-coherent OOK receiver architecture.

$$NF_{receiver} = NF_{LNA} + \frac{NF_{BB}}{G_{DEMOD} \cdot G_{LNA}}$$

Eqn. 52. Noise figure (NF) of the non-coherent OOK receiver depicted in Fig. 76 (Derivation Appendix A).

Given that the power loss of a conventional voltage rectifier used for non-coherent demodulation results in a gain of approximately -50 dB for a weak input signal, the receiver NF is dominated by the second term of Eqn. 52.

There are two primary means by which the receiver noise figure can be improved. The first option is to reduce the loss incurred form the rectifying demodulator. The second option is to increase the gain of the LNA stage without significant degradation to the LNA noise figure. Since, the proposed application is for power limited Smartdust systems, the improvement to gain must be accomplished at minimal additional power consumption.

Power Matched Voltage Doubler for Demodulation

As stated previously, the sensitivity of an OOK receiver is degraded significantly due to the lossy nature of the rectifying demodulator proposed in Fig. 76. To reduce signal power loss and improve S/N ratio, a power matched Villard voltage doubler implemented utilizing diode connected CMOS is proposed as the non-coherent

rectifying element in the receiver architecture (Fig. 77). Improvements to the lossy nature of the rectifying demodulator directly results in less RF loss and, hence, less supply power required to meet the receiver sensitivity requirement.

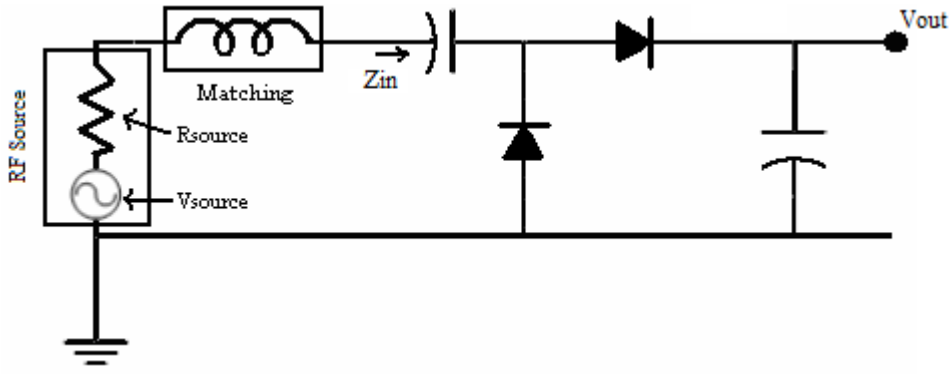


Fig. 77 Villard voltage doubler power matched to RF source.

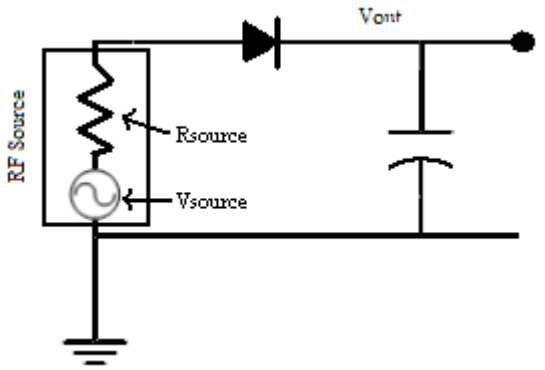


Fig. 78 Conventional envelope detector connected to RF power source.

The Villard voltage doubler rectifies the full wave to deliver twice the voltage to the base band circuitry than the more common half wave rectifier (Fig. 78). In addition, power matching increases the voltage incident to the rectification circuitry, which more strongly forward biases the diode connected MOSFETs. Stronger forward biasing results in less power lost to the channel resistance of the diode connected MOSFETs. Eqn. 53 presents an analytically derived expression for the gain of a

power matched Villard voltage doubler over a traditional half wave voltage rectifier in terms of the input impedance, source resistance, phase angle between the real and imaginary components of the input impedance, and loss from the power matching circuit.

$$Power\ Gain_{dB} = 10 \cdot \log\left(\frac{|Z_{in}|}{R_{source} \cdot \cos(\phi)}\right) - Loss_{matching}$$

Eqn. 53. Power gain of RF energy harvesting circuit over conventional envelope detector.

The input impedance of the Villard voltage doubler (Z_{in}) with a low incident RF signal power represents a large and reactive impedance that is orders of magnitude larger than the source impedance at the output of an LNA. Typical values of Z_{in}, R_{source}, $Loss_{matching}$ and φ represent a 17.6 dB gain over the traditional envelope detector.

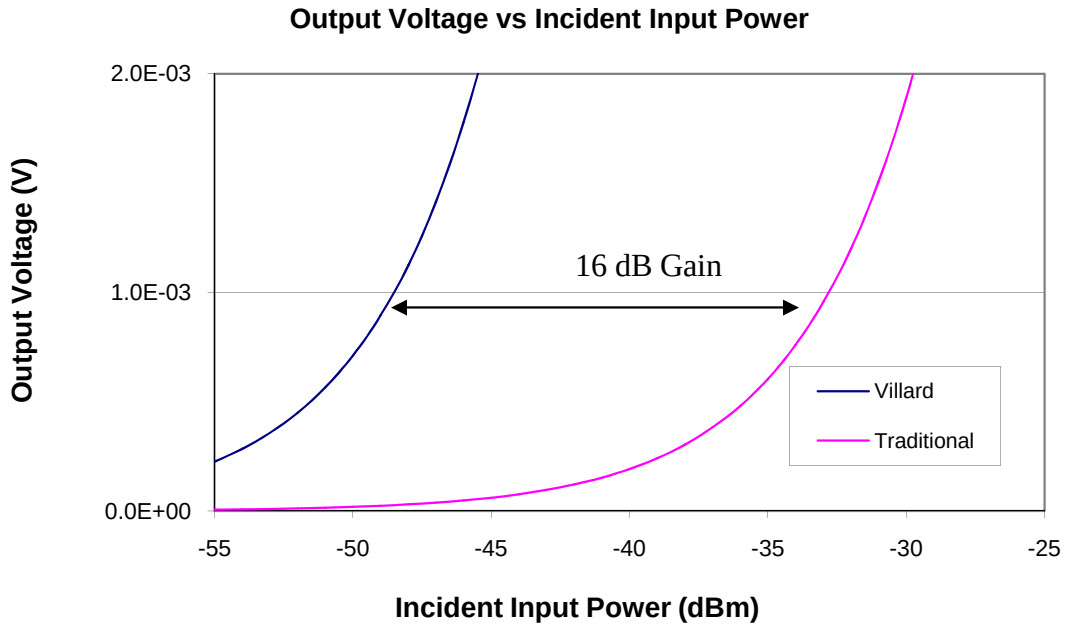


Fig. 79 BSIM 4.0 simulation of power gain of Villard voltage doubler over a conventional envelope detector.

Fig. 79 presents a BSIM 4.0 simulation of the output voltage generated from a given input power level for a power matched Villard voltage doubler and for a traditional half wave envelope detection circuit. By identifying the input power levels points at which each circuit achieves a given output voltage, the gain can be calculated. In this case, by choosing 1 mV as the target output voltage, the simulations result in a gain of approximately 16 dB. This compares well with the 17.6 dB theoretical predicted gain and validates the analysis represented by Eqn. 53. As previously demonstrated from Eqn. 52, a 16 dB reduction in the loss factor of the envelope detector corresponds directly to 16 dB less gain required by the power hungry LNA section of the OOK receiver to meet the desired sensitivity.

The use of an RF power harvesting circuit for demodulation also provides for additional benefits beyond demodulation gain. RF power harvesting circuits have the interesting property of attenuating large signals while allowing small signals to pass unaffected. This effect is illustrated in Fig. 80 and Fig. 81.

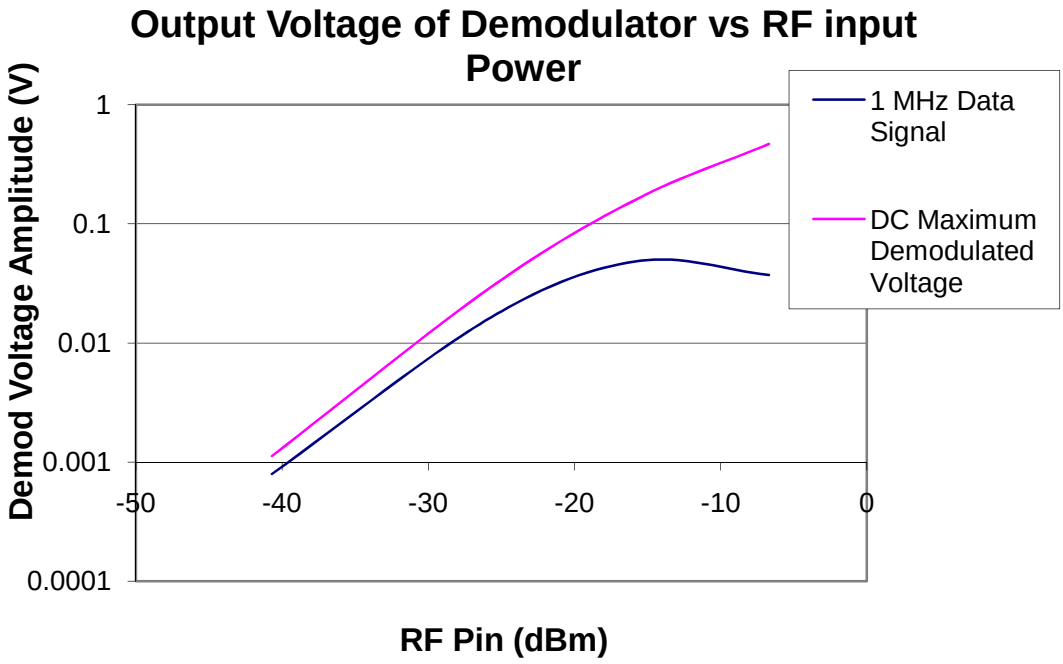


Fig. 80 Normalized transient response of the Villard voltage doubler to a strong input signal (-13 dBm) and weak input signal (-43 dBm) modulated at 1 MHz.

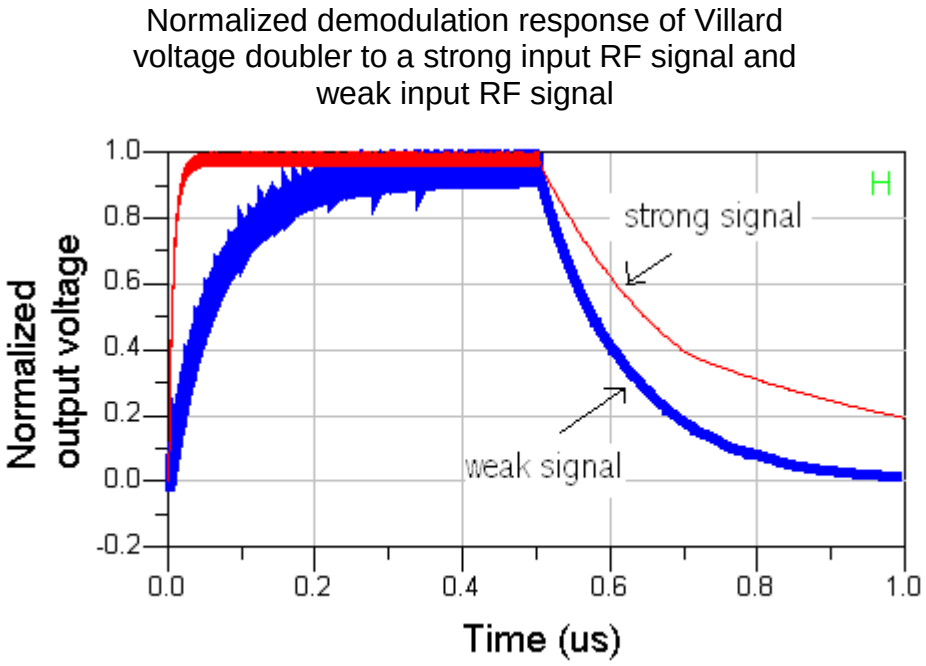


Fig. 81 Normalized transient response of the Villard voltage doubler to a strong input signal (-13 dBm) and weak input signal (-43 dBm) modulated at 1 MHz.

As expected, strong signals show a faster charge time as the junction resistance of the diode decreases. However, as the incident RF energy increases, the discharge time increases. The longer discharge time corresponds to a larger RC time constant and thus dominates the frequency response of the circuit resulting in a lower bandwidth. By decreasing gain as signal strength increases, this effect can be used as a form of automatic gain control and thus, increase the dynamic range of the system.

This effect can better by understood by examination of the equivalent circuit modeling the demodulator and load at time t=0 after removal of the incident RF power (Fig. 82).

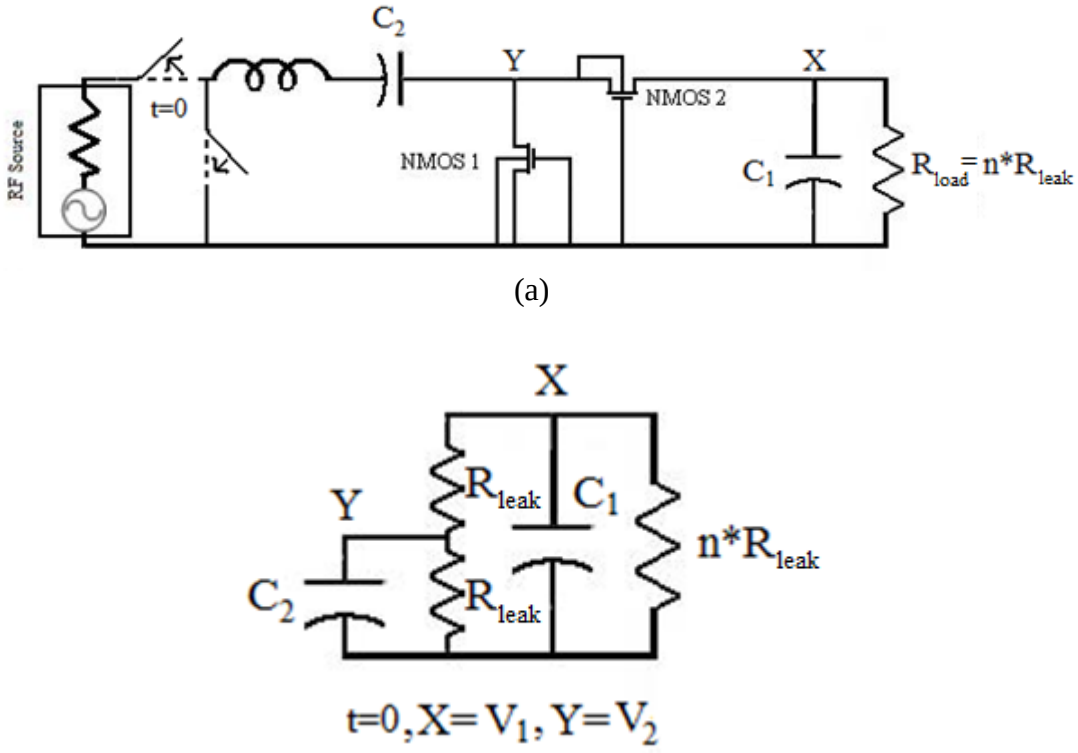


Fig. 82 Power matched Villard voltage doubler acting as demodulator of on-off keyed RF sigal (a) and equivalent impedance presented to the demodulated signal after the RF signal has been removed(b).

In the absence of an RF signal, NMOS1 and NMOS2 result in a leakage current as demonstrated by the equation for the drain current of a MOSFET when V_{GS}=0:

$$I_{ds}(t) = \frac{W_{eff}}{L_{eff}} \cdot I_{vth} \cdot \exp\left(\frac{-V_{th}}{n \cdot V_T}\right)\left[1 - \exp\left(-\frac{V_{ds}(t)}{V_T}\right)\right]$$

Eqn. 54. Leakage current of diode connected MOSFET when no RF signal is present

By approximating the resistance due to the leakage current as:

$$R_{leak} \sim \frac{V_{ds}(t=0)}{I_{ds}(t=0)}$$

Eqn. 55. Approximation of MOSFET resistance due to leakage current and amplitude of demodulated signal.

And Expressing R_{load} as a multiple of R_{leak}:

$$R_{load} = n \cdot R_{leak}$$

Eqn. 56. Representation of load resistance as a multiple of the leakage resistance from the diode connected MOSFETs.

The output voltage as a function of time at point X can be derived as:

$$X = K_1 \cdot e^{r^+ t} + K_2 \cdot e^{r^- t}$$

Eqn. 57. General solution to transient response of discharging voltage on Capacitor C_1 (Derivation Appendix A).

Where:

$$r^{+} = \frac{-\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) + \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1+\frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2 \cdot C_1}}}{R_{leak} \cdot 2}$$

Eqn. 58. First root of the auxiliary equation to the differential equation describing the circuit presented in Fig. 82b (Derivation Appendix A).

$$r^{-} = \frac{-\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) - \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1+\frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2 \cdot C_1}}}{R_{leak} \cdot 2}$$

Eqn. 59. Second root of the auxiliary equation to the differential equation describing the circuit presented in Fig. 82b (Derivation Appendix A).

And

$$K_1 = V_1 - \frac{\left(R_{leak} \cdot C_1 \cdot r^{+} + \left(1+\frac{1}{n}\right)\cdot\right)\cdot V_1 - V_2}{R_{leak} \cdot C_1 \cdot \left(+r^{+} - r^{-}\right)}$$

Eqn. 60. First constant to Eqn. 57 derived from the boundary conditions (Derivation Appendix A).

$$K_2 = \frac{\left(R_{leak} \cdot C_1 \cdot r^{+} + \left(1+\frac{1}{n}\right)\cdot\right)\cdot V_1 - V_2}{R_{leak} \cdot C_1 \cdot \left(+r^{+} - r^{-}\right)}$$

Eqn. 61. Second constant to Eqn. 57 derived from the boundary conditions (Derivation Appendix A).

A quick plot of the discharge after time t at point X for a starting output voltage of 1V and .001 V in Fig. 83 corresponds well with the discharge rate of the BSIM model in Fig. 81.

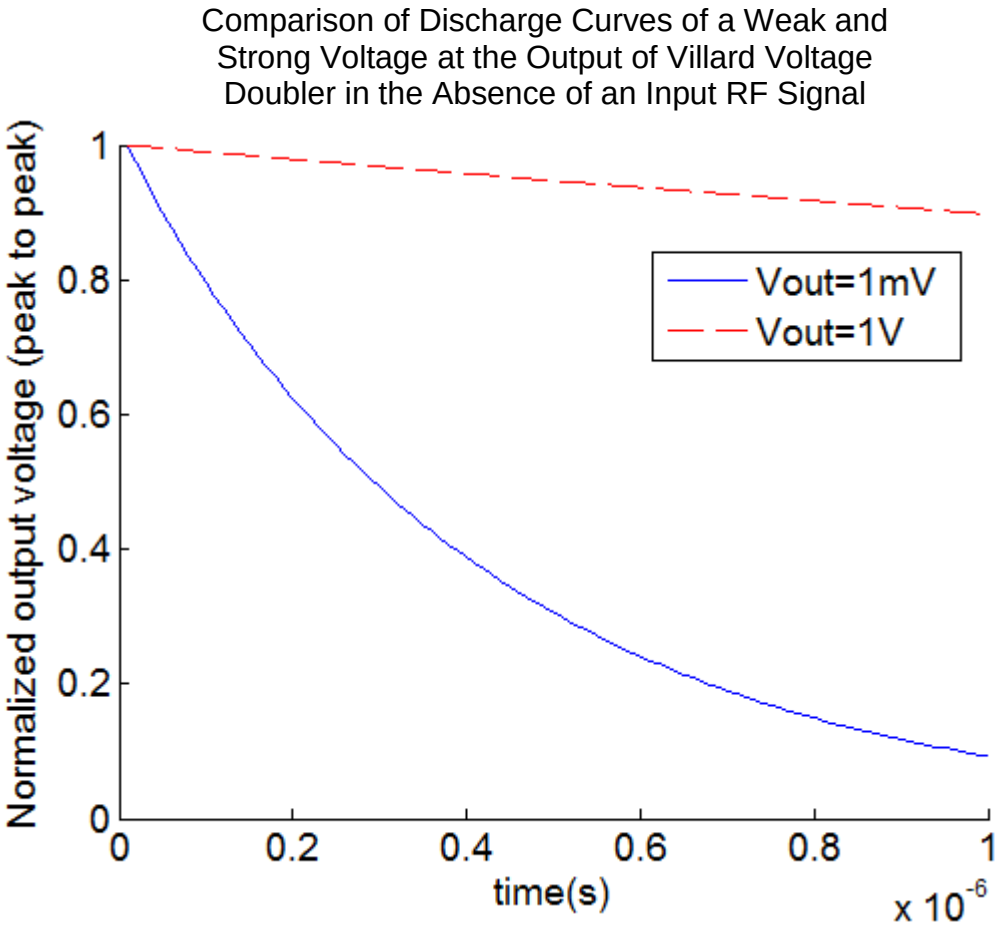


Fig. 83 Normalized discharge curve of strong and weak demodulated signal from the Villard voltage doubler.

In addition, given that r^+ (Eqn. 59) represents the largest RC time constant of the demodulator, the bandwidth of an AC signal applied at node X from the demodulated signal can be derived as:

$$BW = \frac{\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) - \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1+\frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2 \cdot C_1}}}{R_{leak} \cdot 2}$$

Eqn. 62. Demodulation bandwidth of the Villard voltage doubler (Derivation Appendix A).

As expected, the bandwidth (BW) of the demodulator is a function of the demodulated voltage.

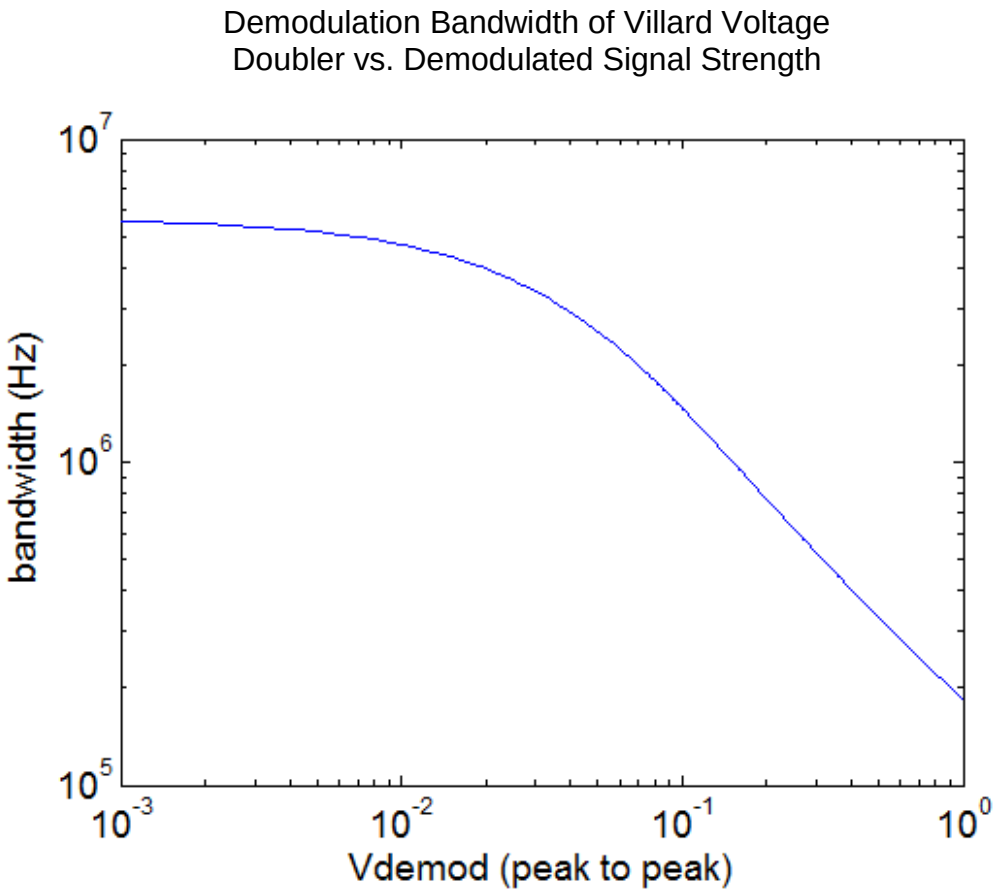


Fig. 84 Demodulation bandwidth of the Villard voltage doubler as a function of demodulated signal amplitude.

For typical values of n, C_1, C_2 and MOSFET parameters, sufficient bandwidth is present to pass a weak demodulated signal at 1 MHZ while the limited bandwidth of the demodulator passing a strong 1 MHz signal will result in significant attenuation (Fig. 84).

Another advantage of the RF power harvesting circuit over the traditional voltage rectifier utilized as an envelope detector is the frequency selectivity of the RF power harvesting circuit. This frequency selectivity, illustrated in Fig. 86, can be compared to the frequency response of a traditional envelope detector in Fig. 85.

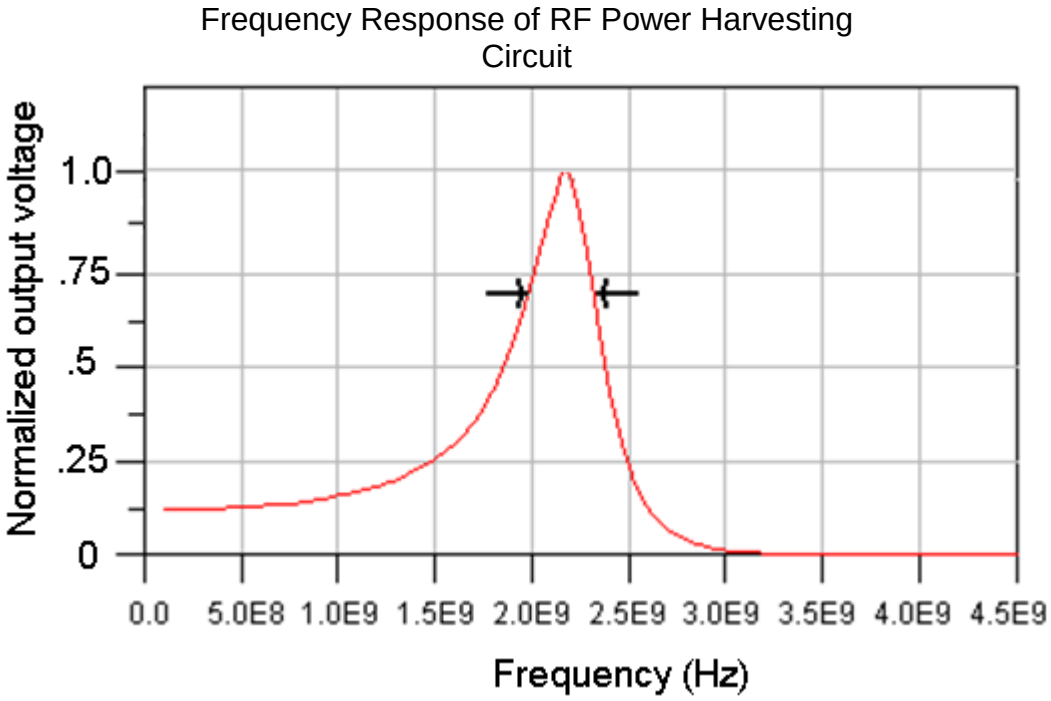


Fig. 85 Normalized output voltage vs frequency for an RF power harvesting circuit with 3dB bandwidth points indicated by arrows.

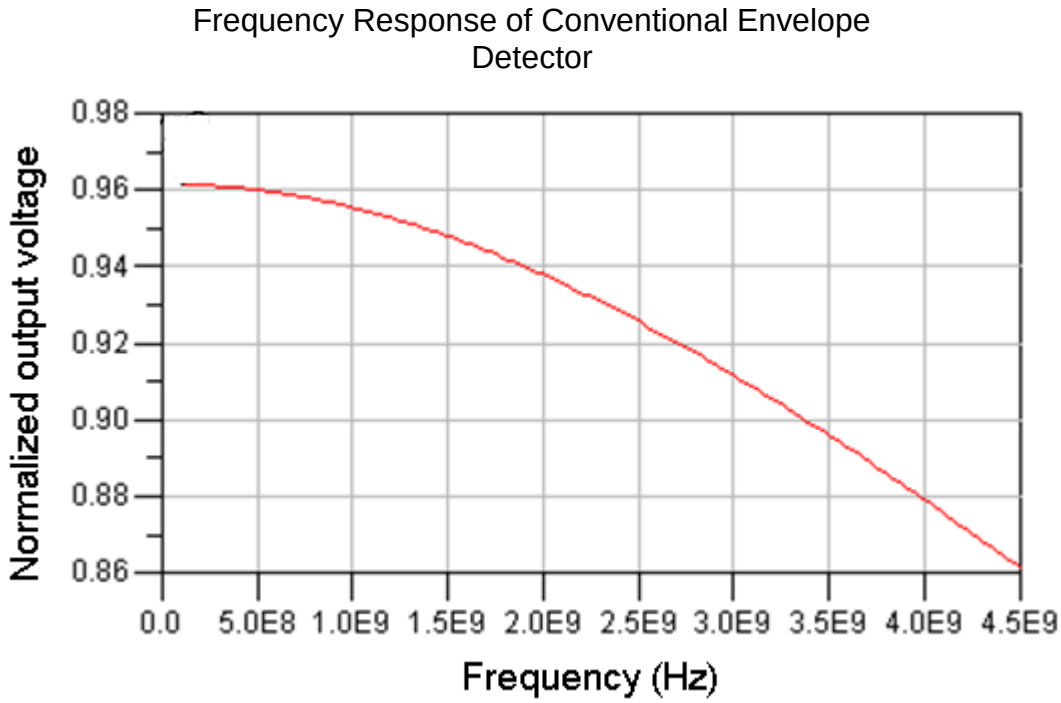


Fig. 86 Normalized output voltage vs frequency for an unmatched rectifier circuit.

An approximation to the 3 dB bandwidth of the RF power scavenging circuit implemented in Fig. 77 can be derived by assuming the RF scavenger acts as a square law detector when demodulating the RF signal:

$$BW_{3dB} = \sqrt{\sqrt{2}-1} \cdot \left(R_{source} + R_{scavenger} + R_{paras}\right) \cdot \pi \cdot f_0^{\,2} \cdot C_{scavenger}$$

Eqn. 63. 3 dB bandwidth of the power matched Villard voltage doubler (Derivation Appendix A).

Where

$$Z_{in} = R_{scavenger} - \frac{j}{\omega \cdot C_{scavenger}}$$

Eqn. 64. Input impedance of the Villard voltage doubler depicted in Fig. 77 as a function of its real and capacitive elements.

f_0 is the frequency at which the RF power scavenger has been power matched to RF source and R_{paras} represents the resistive losses resulting from the finite Q of the matching inductor .

Typical values for the sum of R_{source}, $R_{scavenger}$, and R_{paras} are 100 Ω, and $C_{scavenger}$ is about .2 pF resulting in a bandwidth of 390 MHz. This is consistent with the 3 dB points indicated on Fig. 85 where the voltage is $1/\sqrt{2}$ of the peak value.

This bandwidth reduction serves to help filter the received signal from interference sources, reducing the need for additional RF filtering. Given that power loss must be minimized in the circuit, $R_{scavenger}$ must be approximately equal to R_{source}, and R_{paras} must be very small compared to $R_{scavenger}$ and R_{source}. Therefore, inspection of Eqn. 63 reveals that to minimize bandwidth and thus interference rejection while preserving the sensitivity of the demodulator, it is important to minimize the capacitive component of the RF power scavenger impedance and the parasitic resistances in the network.

This reduction in bandwidth reduces the maximum system data rate, but given that high-speed communication is not important for wireless sensor networks, the reduction in bandwidth is less important than the improved performance in the presence of interference.

Optimization of a Multi-Stage LNA

A reduction in the lossy nature of the non-coherent rectification circuitry alone is not enough to meet the sensitivity requirement to reliably communicate over 10 m in a high loss environment. As shown previously in Eqn. 52, a strong LNA gain can affectively negate the increase in noise figure due to the lossy nature of the rectification circuitry. The challenge is to realize a large RF gain in the multi-stage LNA while consuming the minimal DC supply power.

Work by Meindl and Hudson studies how gain and power scale as a function of the number of stages in various multi-stage amplifier designs with emphasis on bipolar technologies [106]. In continuation of that work, Daly and Chandrakasan build upon this approach through the efficiency metric:

$$Efficiency = \frac{\log(G_{LNA})}{P_{LNA}}$$

Eqn. 65. Efficiency metric utilized by Daly and Chandrakasan.

This metric defines efficiency as a function of gain and power consumption of an LNA and is used by Daly and Chandrakasan to optimize an untuned RF amplifier topology (Eqn. 66). The contribution of NF and number of amplification stages on the efficiency of a multistage is neglected [94].

$$0 = \frac{\partial}{\partial_X} \frac{\log(G_{LNA})}{P_{LNA}} \tag{4}$$

Eqn. 66. Optimization of efficiency metric for variable X.

The methodology presented in this work expands upon these previous works by recognizing that in addition to the gain and power consumption of each LNA stage, the efficiency of an LNA design for a receiver is dependent upon the noise figure and the number of RF amplification stages cascaded together in the receiver. Under these constraints, an analytical methodology for meeting receiver noise figure requirements at the minimum total power consumption of a multi-stage power constrained common source LNA design is derived.

Through application of the Friis formula (Eqn. 67), the total NF of a receiver can be divided into an equation defining the NF of a multi-stage LNA as a function of the gain and noise figure of the individual LNA stages (Eqn. 68) and an equation defining the NF of the receiver in terms of the NF from the baseband circuitry, NF of the multi stage LNA, and gain of each LNA stages (Eqn. 69).

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 \cdot G_2} + \frac{NF_4 - 1}{G_1 \cdot G_2 \cdot G_3} \mathrm{K}$$

Eqn. 67. Friis formula. Determines total NF or a receiver as a function of each stage's noise figure and gain.

$$NF_{n\_LNA\_stages} = \sum_{i=1}^{n} \frac{NF_{LNA} - 1}{G_{LNA}^{\ i-1}} + 1$$

Eqn. 68. NF of multi-stage LNA.

$$NF_{receiver} = NF_{n\_LNA\_stages} + \frac{NF_{BB\&DEMOD} - 1}{G_{LNA}{}^{n}}$$

Eqn. 69. NF of the receiver depicted in Fig. 76 comprised of multi-stage LNA, demodulator, and baseband circuitry.

The summation in Eqn. 68 can be recognized as a geometric series and simplified to:

$$NF_{n\_LNA\_stages} = \frac{NF_{LNA} - 1}{1/G_{LNA} - 1} \cdot \left(\frac{1}{G_{LNA}{}^{n}} - 1 \right) + 1 \qquad n \in [1, \infty]$$

Eqn. 70. Simplification of Eqn. 68 as a geometric sequence.

Eqn. 69 and Eqn. 70 can be combined to determine the required number of stages as a function of the NF of the non LNA stages, desired NF for the receiver, and performance parameters (NF and gain) of the individual stages of the multi-stage LNA (Eqn. 71).

$$n = \frac{\log\left(\dfrac{NFreq - 1 + \dfrac{NF_{LNA} - 1}{1/G_{LNA} - 1}}{NF_{BB} - 1 + \dfrac{NF_{LNA} - 1}{1/G_{LNA} - 1}} \right)}{\log\left(1/G_{LNA} \right)}$$

Eqn. 71. Minimum number of LNA stages to meet receiver noise figure requirement.

By assuming power consumed by the baseband stage is very small compared to the power required by the RF amplifier stages, the total power consumed by the receiver is approximately equal to the sum total of the power consumed in each LNA stage.

$$P_{receiver} = n \cdot P_{LNA}$$

Eqn. 72. Power consumption of optimized multi-stage LNA.

By performing an optimization of the total power draw of the multi-stage LNA as the NF_{LNA} goes to zero, this analysis converges to the less accurate power and gain analysis of previous works in the field represented by Eqn. 65 and Eqn. 66. This result demonstrates this work to be a more complete and comprehensive analysis than the analysis of prior works.

$$P_{draw\_total} = n \cdot P_{LNA} = \lim_{NF_{LNA} \to 0} \frac{\log\left(\frac{NFreq - 1 + \frac{NF_{LNA} - 1}{1/G_{LNA} - 1}}{NF_{rest} - 1 + \frac{NF_{LNA} - 1}{1/G_{LNA} - 1}} \right)}{\log\left(1/G_{LNA}\right)} \cdot P_{LNA}$$

$$P_{draw\_total} = \frac{\log\left(\frac{NFreq - 1}{NF_{rest} - 1}\right)}{\log\left(1/G_{LNA}\right)} \cdot P_{LNA} = \frac{C \cdot P_{LNA}}{\log\left(1/G_{LNA}\right)} = \frac{-C \cdot P_{LNA}}{\log\left(G_{LNA}\right)}$$

Eqn. 73. Convergence of the optimization methodology proposed by this work to the inverse of the metric utilized by Daly and Chandrakasan as NF of the LNA converges to zero.

$$0 = \frac{\partial}{\partial_X} Pdraw\_total = -C \cdot \frac{\partial}{\partial_X} \frac{P_{LNA}}{\log\left(G_{LNA}\right)} = \frac{\partial}{\partial_X} \frac{\log\left(G_{LNA}\right)}{P_{LNA}}$$

$$0 = \frac{\partial}{\partial_X} \frac{\log\left(G_{LNA}\right)}{P_{LNA}}$$

Eqn. 74. Equivalency of an optimization performed on the methodology proposed by this work to an optimization of the metric utilized by Daly and Chandrakasan as NF of the LNA converges to zero.

We now have the total power consumption of the receiver as a function of the gain, NF, and power consumption of a single stage of the multistage LNA; noise figure of the baseband of the receiver; and required receiver noise figure (Eqn. 71 and Eqn. 72).

Up to this point, the treatment presented is a generalization that applies to a receiver utilizing a multi-stage LNA comprised of any RF amplifier topology. In this work, the power restricted common source cascode LNA depicted in Fig. 87 was implemented due to its good noise performance and narrow band operation.

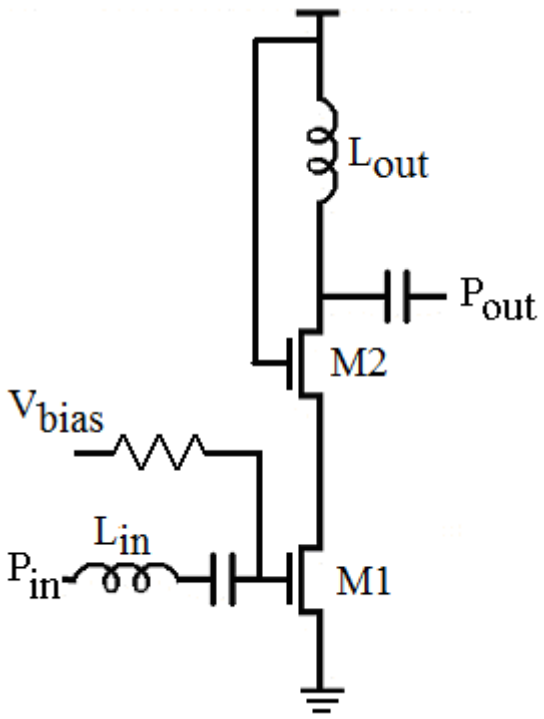


Fig. 87 Common source cascode low noise amplifier implemeted in the multi-stage LNA design of this work

For the common source LNA, all three performance parameters (supply power, gain, and noise figure) are determined by the level of channel inversion of the MOSFET, M1, in Fig. 87. Proper optimization between weak and strong inversion is necessary to optimize between the superior g_m of sub-threshold operation and the larger f_t of a MOSFET operating in strong inversion. The level of inversion is a function of the bias voltage (V_{bias}) indicated in Fig. 87. Therefore, V_{bias} is the variable over which the gain, noise figure and supply current must be optimized over.

There are several methods for determining the performance parameters of the LNA as a function of V_{bias} including the application of a spice based simulator or direct measurement through fabrication. The method chosen in this work is to analytically model the power supply consumption, gain, and noise figure of the LNA as a function of the performance limitations of the common source cascode LNA topology implemented in CMOS. This methodology will be validated against both simulated and measured data.

Power consumption for the common source LNA can be defined as the supply voltage times the channel current of the MOSFET.

$$P_{LNA} = I_{ds} \cdot V_{Supply}$$

Eqn. 75. Power supply consumption of a single common source cascode LNA stage.

Where I_{ds} is modeled as an exponential function (Eqn. 76) for sub-threshold operation and quadratic function (Eqn. 77) when operating in strong inversion [87].

$$I_{strong} = \frac{u_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \frac{(V_{bias} - V_{th})^2 \cdot (1 + \lambda \cdot V_{sup\ ply})}{1 + u_n \cdot C_{ox} \cdot \frac{W}{L} \cdot Rsx \cdot (V_{bias} - V_{th})}$$

Eqn. 76. Supply current of LNA biased in strong inversion.

$$I_{weak} = \frac{W}{L} I_t \exp\left(\frac{V_{bias} - V_{th}}{n \cdot V_t}\right)\left[1 - \exp\left(-\frac{V_{sup\ ply}}{V_t}\right)\right]$$

Eqn. 77. Supply current of LNA biased in weak inversion.

Where transistor gate length is the minimum supported by the process and optimal transistor width can be approximated for a power restricted common source LNA operating at 2.2 GHz as 114 um [107].

$$W_{opt} = \frac{250\ um \cdot GHz}{freq_{GHz}}$$

Eqn. 78. Optimal transistor width for power restricted common source cascode LNA.

The transition between these two modes of operation is modeled as a weighted average.

$$I_{ds} = I_{weak} \cdot M + I_{strong} \cdot (1 - M)$$

Eqn. 79. Supply current of common source cascode LNA as a weighted average of the drain current modeled by weak and strong inversion.

Where the weight factor, M, is defined as:

$$\begin{aligned} M &= 1 && V_{bias} \le V_{th} \\ M &= \left(\frac{1-(V_{bias}-V_{th})}{2 \cdot n \cdot V_t} \right) && V_{th} < V_{bias} < (V_{th} + 2 \cdot n \cdot V_t) \\ M &= 0 && V_{bias} \ge (V_{th} + 2 \cdot n \cdot V_t) \end{aligned}$$

Eqn. 80. Weight factor used to properly model the drain current of a common source cascode LNA.

Assuming the LNA has been power matched at both input and output, circuit analysis of a cascode LNA implemented in CMOS and associated parasitic sources reveals an analytical expression for the gain of the LNA as:

$$P_{gain}(dB) = 10 \cdot \log\left(\left| Q_{in} \cdot g_m \right|^2 \cdot \frac{R_{load}}{2} \cdot R_{source} \right)$$

Eqn. 81. Power gain common source cascode LNA (Derivation Appendix A).

Where R_{source} is the impedance of the RF source driving the LNA and R_{load} is the output resistance at the output of the LNA. Q_{in} is the voltage gain due to the input matching circuit and is expressed as:

$$Q_{in} = \frac{1}{2 \cdot \pi \cdot f \cdot C_{gate} \cdot (R_{source} + R_{gate})}$$

Eqn. 82. Voltage gain of input power matching circuit for common source cascode LNA.

Where C_{gate} is derived from the gate dimensions and the oxide capacitance:

$$C_{gate} = \frac{2}{3} \cdot C_{ox} \cdot W_{eff} \cdot L_{eff}$$

Eqn. 83. Parasitic gate capacitance of common source cascode LNA.

And the work by Jin et al. provides an analytical model for the gate resistance [89].

$$R_{gate} = \left(\frac{1}{12} \cdot \frac{R_{res} \cdot W_{eff}}{n_f{}^2 \cdot L_{eff}} \right) + R_s + \left(\frac{1}{12} \cdot \frac{L_{eff}}{n \cdot W_{eff} \cdot u_n \cdot C_{ox} \cdot V_t} \right)$$

Eqn. 84. Parasitic gate resistance of common source cascode LNA.

Finally, by recognizing that the input matching inductor is resonantly matched to the gate capacitance of M1, the noise figure can be modeled from the analysis in [108].

$$NF_{LNA} = 1 + \frac{R_{gate}}{R_{source}} + \lambda f^2 \frac{R_{source} + R_{gate}}{f_T{}^2} \cdot \frac{g_{d0}}{R_{source}}$$

Eqn. 85. Noise figure (NF) of common source cascode LNA.

Where the parameter g_{d0} represents g_{ds} evaluated when V_{ds} is equal to 0 V, and λ is a fitting parameter.

We have now developed completely analytical expressions to predict the performance parameters of an individual LNA stage. To validate the model, the power restricted common source cascode LNA was fabricated in a 130 nm process. Fig. 89 through Fig. 91 illustrate the strong agreement between the analytical models and measured performance of the common source cascode LNA as a function of bias voltage.

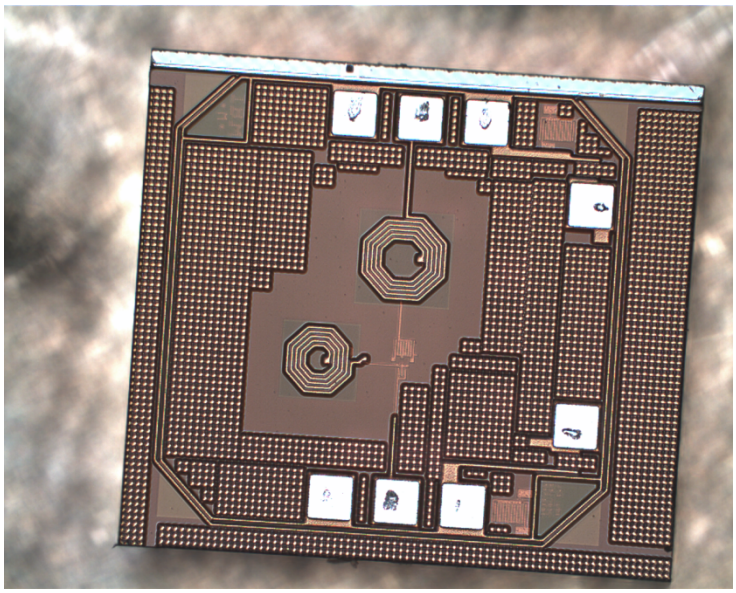


Fig. 88 Image of fabricated common source cascode LNA.

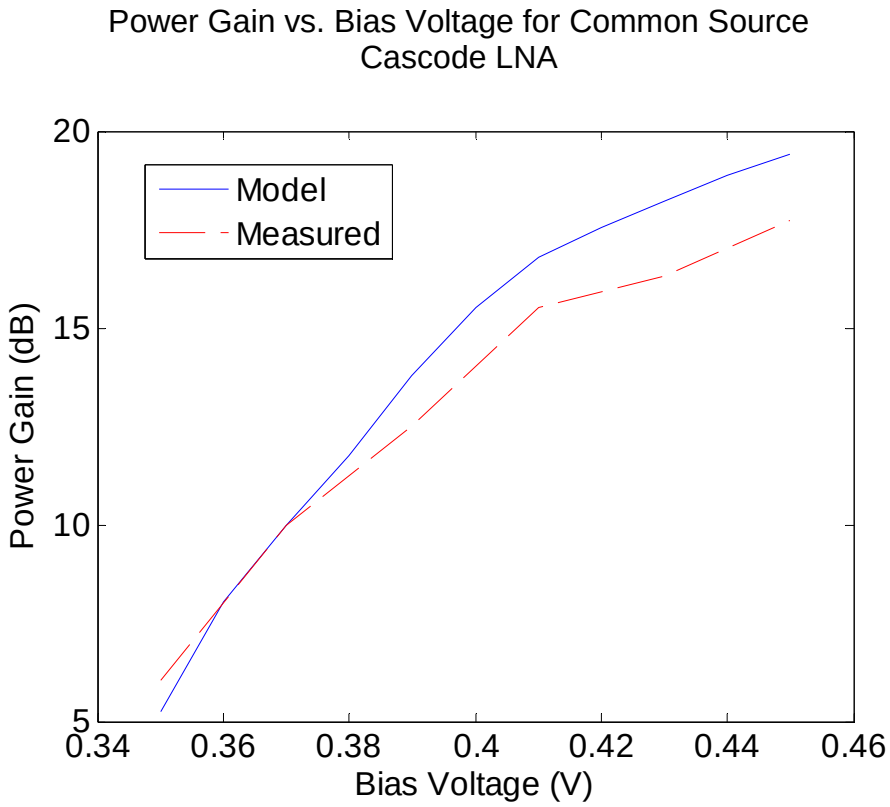


Fig. 89 Comparison of measured and analytically modeled power gain of common source cascode LNA as a function of bias voltage.

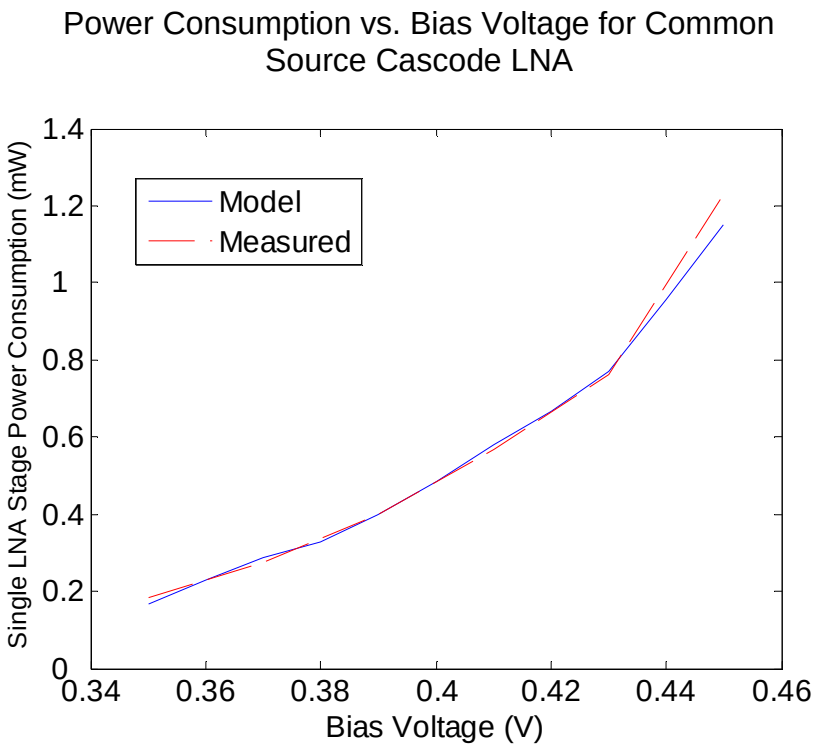


Fig. 90 Comparison of measured and analytically modeled DC supply power consumption of common source cascode LNA as a function of bias voltage.

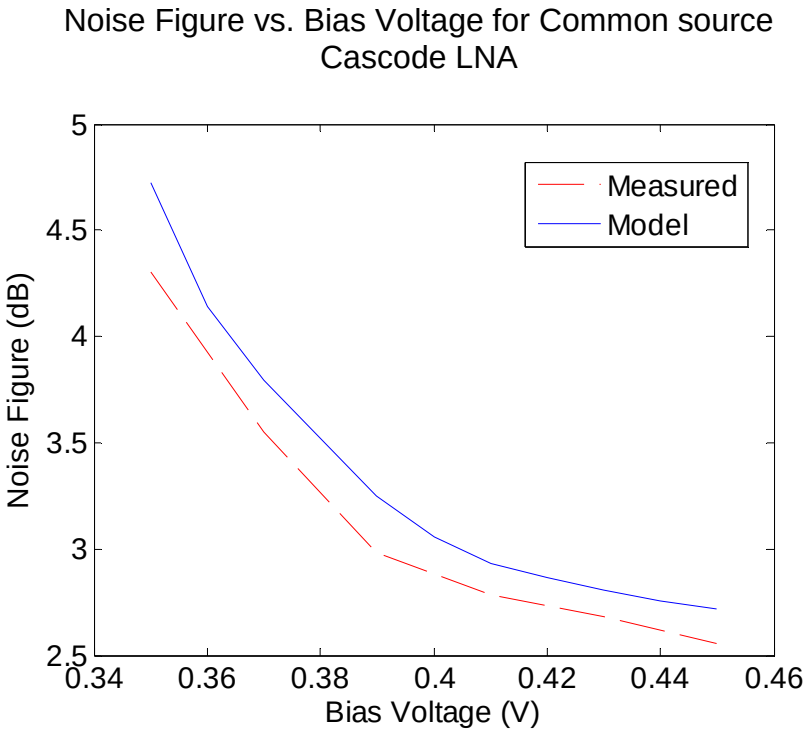


Fig. 91 Comparison of measured and analytically modeled noise figure of common source cascode LNA as a function of bias voltage.

As stated, the design goal was to achieve a sensitivity of -90 dBm at a data rate of 1 Mbps. Thus, a receiver NF of 7 dB is necessary to meet the performance goal. Given the LNA performance metrics provided by Eqn. 75, Eqn. 81 and Eqn. 85, in addition to the baseband NF, the required number of stages and total power consumption can be plotted as a function of V_{bias} from Eqn. 71 and Eqn. 72.

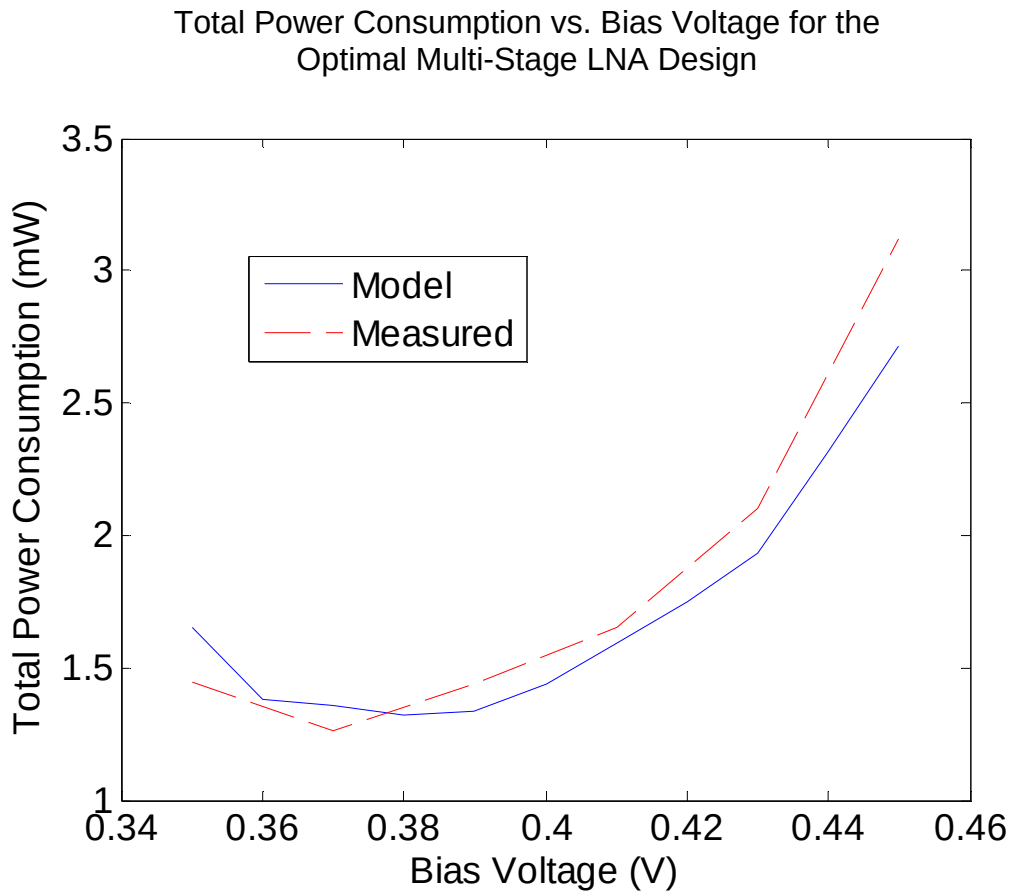


Fig. 92 Comparison of measured and analytically modeled total power consumption of optimized multi-stage LNA as a function of bias voltage.

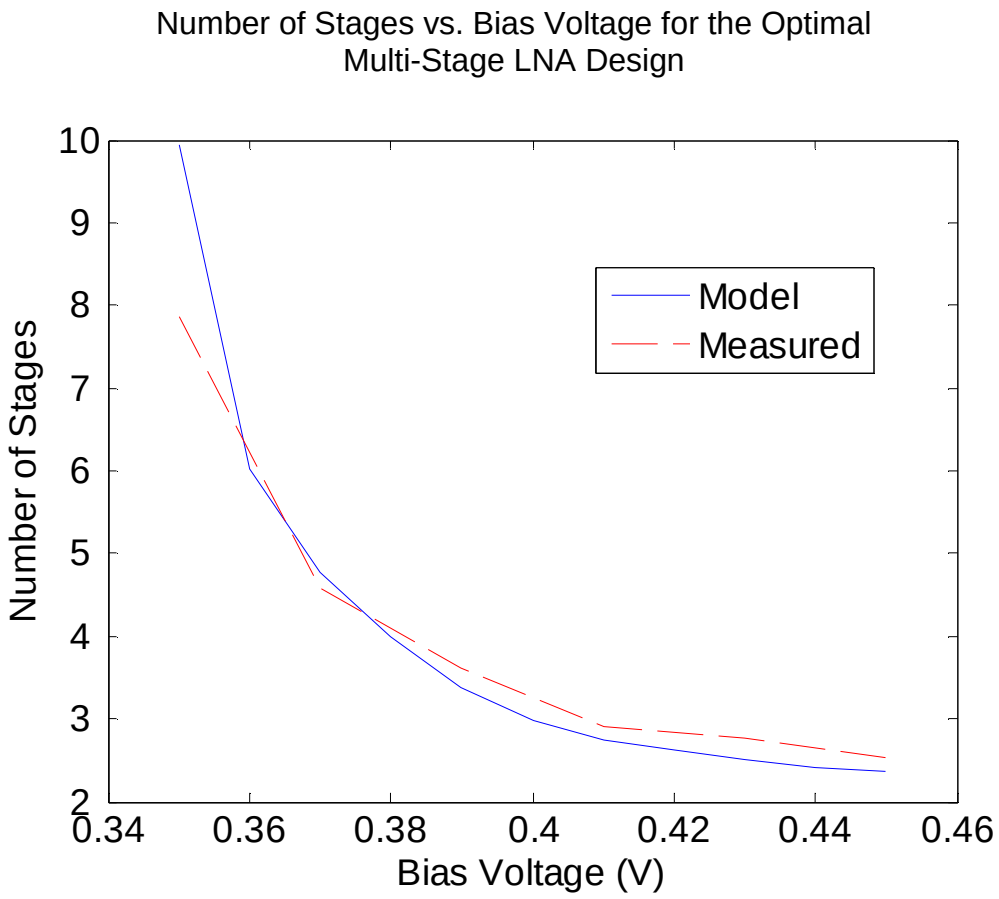


Fig. 93 Comparison of measured and analytically modeled number of LNA stages necessary to meet receiver noise figure requirement as a function of bias voltage.

As shown in Fig. 92, the analytical model and the measured data predict that the required receiver noise figure of 7 dB can be met with only 1.32 mW of total supply power by electing a bias voltage of .38 V. This result requires four stages of amplification to meet the –90 dBm sensitivity (Fig. 93).

Receiver design is often a series of trade offs and optimization between design parameters. Chip die area is an important design parameter. Four stages of RF amplification consumed a prohibitive amount of die space. For this reason,

minimizing the number of amplification stages is an important design goal. Towards that goal, through an examination of Fig. 92 and Fig. 93, we can see that reductions in the number of RF amplification stages can be realized through minor increases in supply power draw. Therefore, the bias point was set at .41 V, requiring only three stages of RF amplification and 1.6 mW of total power draw as predicted from measured performance parameters. This results in a multi-stage LNA with 46 dB of power gain and a noise figure of 2.85 dB.

Lastly, to complete the characterization of the individual LNA stages, the third order intermodulation product and 1 dB compression point were determined.

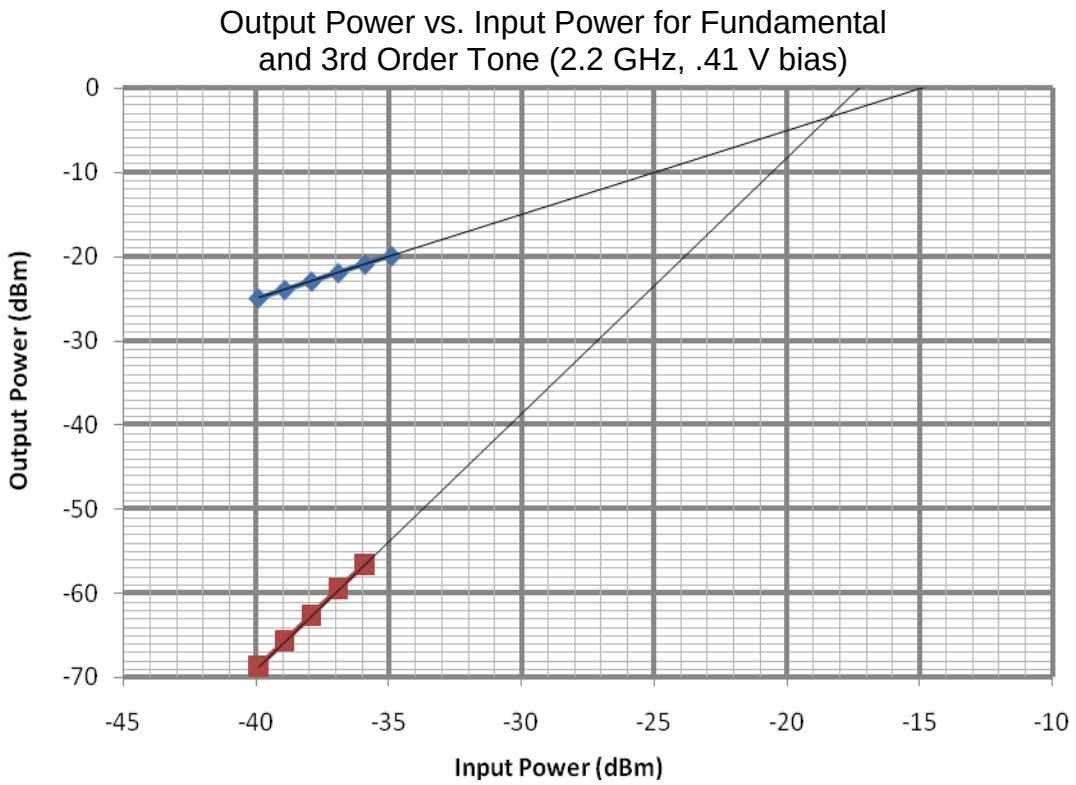


Fig. 94 Output power vs. input power for fundamental (blue data pts) and 3rd order tone (red data pts). The intersection of these two lines determines the third order intermodulation point (IIP3 and OIP3).

Because the LNA is a narrowband device the two tone test was used. This test requires two closely spaced balanced tones to be injected into the LNA at the operational frequency. By plotting the intersection of the output power level of the fundamental tones with the third order tones versus the input power, we can determine the third order intermodulation point (IIP3). This measurement and the resulting IIM3 for the LNA operating at a .41 V bias voltage are plotted in Fig. 94. The resulting IIP3 and output third order intercept point (OIP3) are -18.5 dBm and -3.5 dBm, respectively.

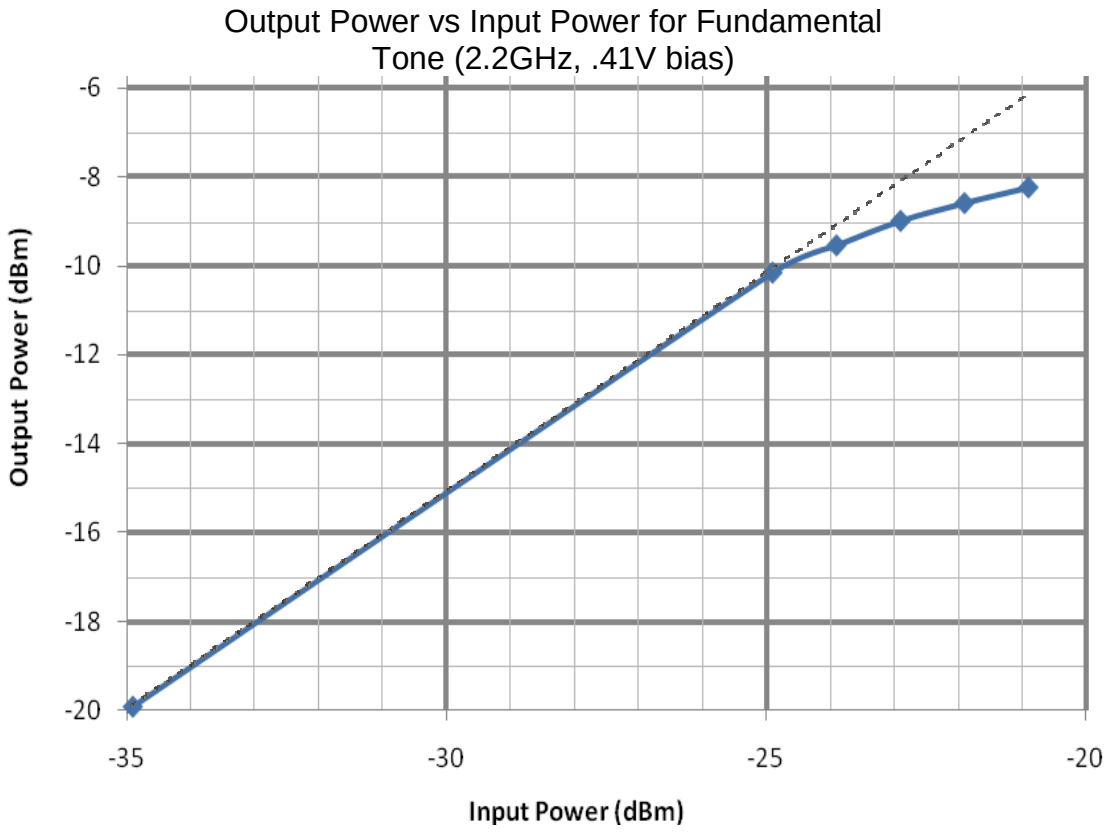


Fig. 95 Output power vs input power for fundamental tone (2.2GHz, .41V bias). This plot is used to determine the 1 dB compression point.

By plotting the output power level of the fundamental tone versus the input power, we can determine the 1 dB compression point. The point where the measured gain is 1 dB less than the expected linear interpolation of the gain at lower input RF power levels, is the 1 dB compression point. This measurement and the resulting 1 dB compression point for the LNA operating at a .41 V bias voltage are plotted in Fig. 95. The resulting input 1 dB compression point and output 1 dB compression point are -23 dBm and -9 dBm, respectively.

Baseband

The base band consists of a sequence of four differential amplifiers followed by an op-amp comparator to provide digital output levels. To reject supply rail and substrate noise generated by the RF amplification stages and any digital electronics incorporated on-chip, a differential design was adopted for the base band amplification circuitry (Fig. 96).

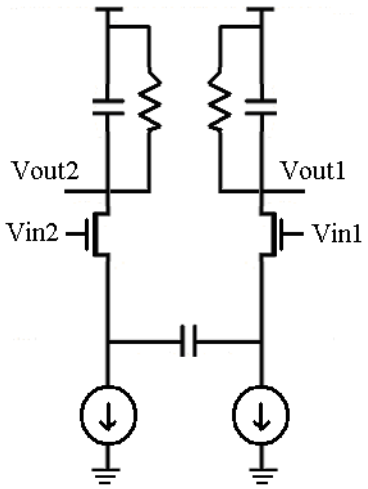


Fig. 96 Single stage of multi-stage baseband differential amplification circuit.

Although differential base band circuitry draws approximately 3 dB more power than the common mode counterpart, given the low power consumption relative to the RF amplification stages, differential amplification does not significantly increase total receiver power draw.

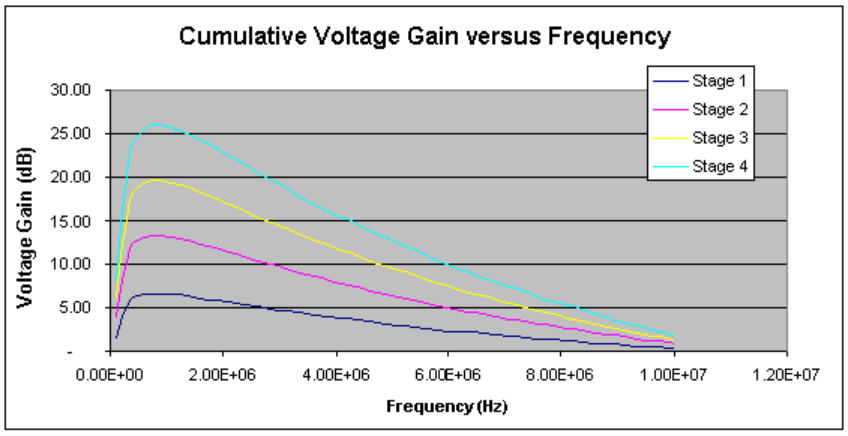


Fig. 97 Cumulative voltage gain after each stage of baseband amplification versus frequency.

In addition, to reject the DC offset introduced by transistor mismatch and minimize noise to improve the S/N ratio, band pass filtering is provided utilizing capacitors C_1, C_2 and C_3 (Fig. 97).

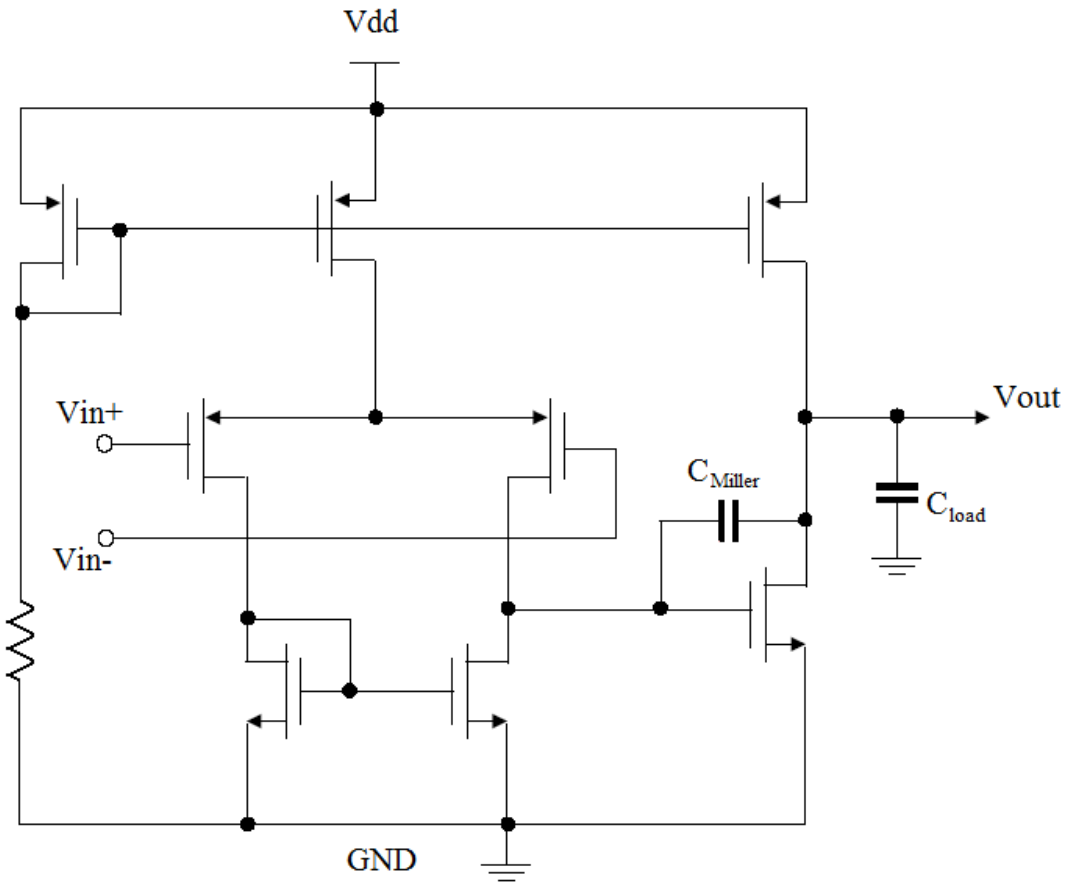


Fig. 98 Comparator design implementing Miller capacitor to increase stability.

The comparator was designed as an op-amp depicted in Fig. 98 utilizing the Miller effect (C_{Miller}) to increase phase margin and prevent ringing [109]. Each stage of baseband amplification draws less than 8 uA, while the comparator draws less than 20 uA for a total base band current draw of approximately 52 uA.

Given the AC coupled nature of the base band circuitry, an encoding scheme that minimizes the DC component of the base band signal is required. A popular option is Manchester encoding.

Measurements

An experimental prototype of the receiver was fabricated utilizing an IBM 130 nm CMOS process (Fig. 99). The design was realized on a die measuring 2 mm by 2 mm while the space consumed by the receiver measured approximately 1.0 mm^2. Particular attention was paid towards minimizing parasitic capacitance between the RF lines and the substrate.

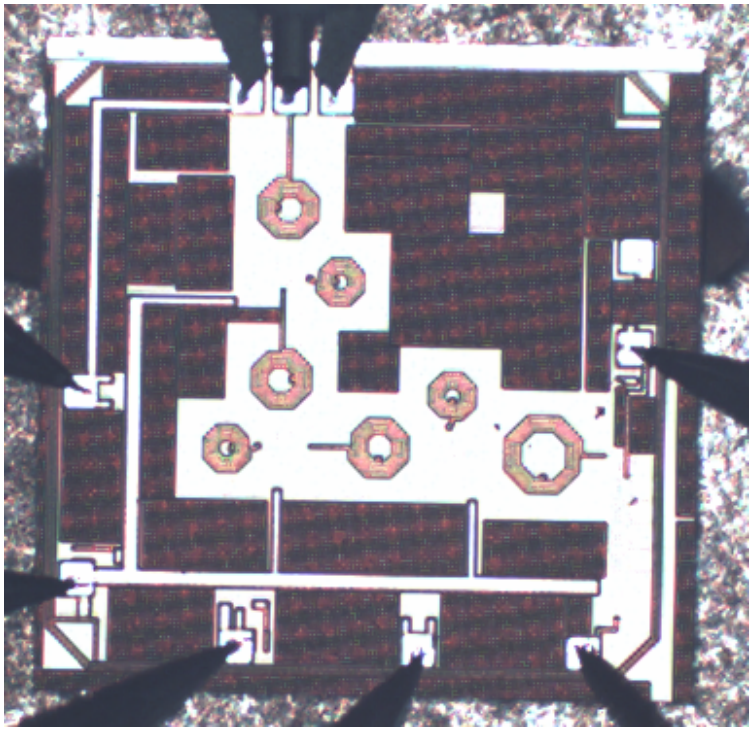


Fig. 99 Image of fabricated low power receiver

Validating the analytical model, a BER of 10^{-3} was measured at the predicted .41 V multi-stage LNA biasing voltage. The total power consumption is only 1.6 mW from the 1 V supply rail. In addition, the receiver shows good performance up to the measured input RF power level of –20 dBm providing good dynamic range. TABLE V summarizes the measured performance metrics.

TABLE V PERFORMANCE METRICS OF LOW POWER RECEIVER AND SUBCOMPONENTS

Specifications			
Receiver Performance		*Implementation*	
Sensitivity (BER=10^{-3})	-90 dBm	Transmission Frequency	2.2 GHz
Power Consumption	1.6 mW	Technology	.13 um CMOS
Energy per Bit	1.6 nJ/bit	Die Area Used	1 mm^2
Data Rate	1 Mbps	Supply Voltage	1 V
Single-Stage LNA Performance		*Multi-Stage LNA Performance*	
Gain	15.5 dB	Gain	46 dB
Power Consumption	.5 mW	Power Consumption	1.6 mW
Noise Figure	2.8 dB	Noise Figure	2.85 dB
IIP3	-18.5 dBm		
Output 1 dB Comp. Pt.	-9 dBm		
RF Scavenging Demodulator			
Gain vs Voltage Rectifier	17.6 dB		
Power Consumption	0 mW		
Baseband			
Voltage Gain	30 dB		
Filter Bandwidth (3dB)	1 MHz		
Power Consumption	.05 mW		

Conclusions

An ultra low power OOK receiver with a link margin suitable for challenging transmission environments has been presented. Among the notable design attributes are a completely analytical methodology for optimizing a multi-stage LNA and use of a RF power harvesting circuit for passive demodulation. To meet the -90 dBm desired receiver sensitivity, application of the optimization methodology presented

results in an LNA design with 46 dB of gain and a 2.85 dB noise figure that consumes only 1.6 mW of total power.

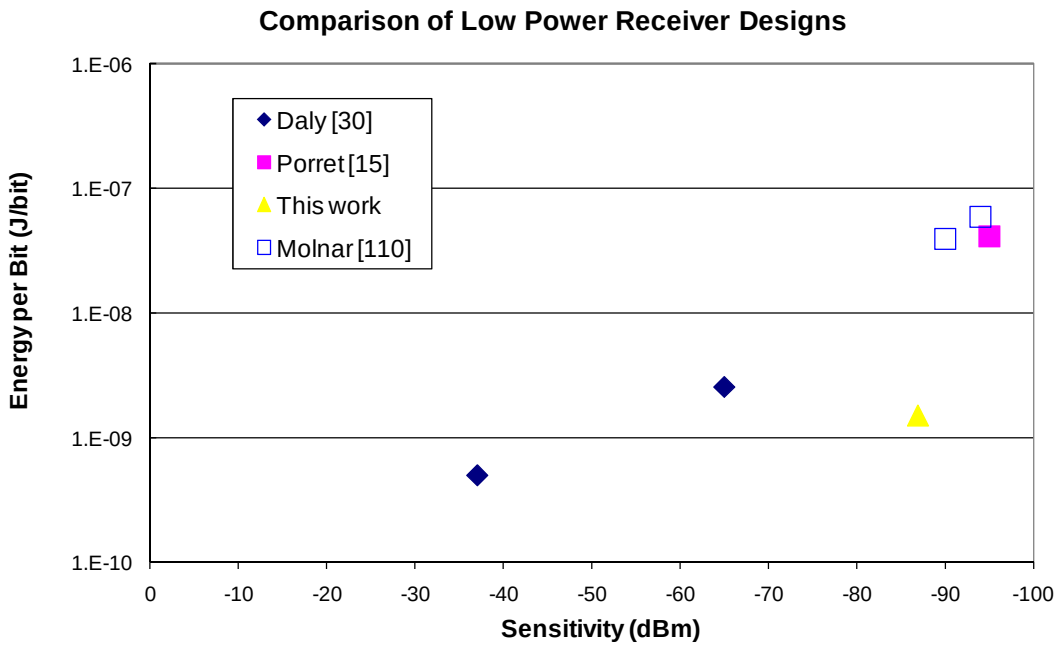


Fig. 100 Comparison of the energy effiency of the low power receiver design resulting from this work to other low power receiver designs in the literature.

Good agreement has been demonstrated between predicted performance and measured receiver performance. The 2.2 GHz OOK receiver meets the design requirement of –90 dBm sensitivity at 1 Mbps while drawing only 1.6 mW of power from a 1 V supply rail. In addition, the receiver architecture consumes just 1 mm^2 of die space and requires no external passives, thus preserving the cm^3 scale form factor necessary for Smartdust sensor networks. These results compare favorably with prior work in the field (Fig. 100) and demonstrate that significant improvements in sensitivity can be achieved with minimal additional power consumption.

Chapter 6: Conclusions

Smartdust is the realization of wireless sensor networks in a sub-cubic centimeter form factor. Through the random distribution of Smartdust nodes, sensor networks can quickly be established to remotely monitor large regions of area. To minimize deployment costs, individual nodes will be fabricated in CMOS taking advantage of economies of scale. The advantages of sensor networks to assist in disaster relief, the military, health care, and business activities have resulted in their being the subject of significant research in recent years.

The development of Smartdust sensor networks is not without considerable research and design challenges. The aggressive form factor of Smartdust sensor networks limits the ability of on system energy storage to meet system life time requirements that can measure in months to years. As demonstrated in Chapter 1, various research efforts are under way to extend the operation life time of Smartdust sensor networks through energy scavenging from energy sources commonly available in the environment. In addition, previous works have demonstrated that Smartdust sensor networks transmit little data and thus life time is dominated by power consumption of the receiver. Works in the literature have proposed various approaches to lowering receiver power consumption. However, to extend system life time, it is desirable that the energy required to receive a bit of data be minimized. Towards this goal, 1 nJ of energy consumption per bit represents the state of the art for low power receiver

design. However, the random distribution of Smartdust sensor networks results in a difficult transmission environment that can be characterized by $1/r^3$ path loss. As a result, work in the literature that achieves the 1 nJ energy consumed per bit of data received, are not sensitive enough to provide sufficient link margin to provide communication over 10 meter distances, and receivers that demonstrate sufficient link margin to communicate over 10 meters, reduce system life time by at least an order of magnitude.

This work is resolving some of the issues associated with Smartdust networks by addressing the challenges resulting from such a small form factor, limited power supply and difficult transmission environment.

As demonstrated through a comprehensive RF energy survey reported in Chapter 2, this work confirms that sufficient RF energy levels are available in the environment from the cellular and UHF TV communications infrastructure to supply power to a Smartdust sensor node. Thus, this work demonstrates the exciting potential of the cellular and UHF TV wireless networks deployed throughout the country to provide a cheap and abundant source of energy for Smartdust sensor networks.

To assist in achieving the RF to DC power conversion efficiencies necessary to power Smartdust nodes from RF energies found in the environment, a parasitic aware analytical model of the power matched Villard voltage doubler implemented in CMOS was derived and validated against simulated and measured data. This model

represents the most comprehensive and accurate analytically derived model of a power matched Villard voltage doubler integrated onto CMOS to date. Through the study of this model, under incident power level conditions representative of RF power levels present in the environment, the dominate sources of parasitic loss were identified as the threshold voltage loss of the diode connected MOSFETs and the parasitic gate losses at the input to the Villard voltage doubler. The need to lower threshold voltages is a well known mechanism for improving power harvesting performance, however, the need to lower parasitic gate losses is a result newly reported in this work. In addition, this model was used to characterize the effect of stacking multiple Villard voltage doubler stages on RF to DC conversion efficiency. Finally, this model is used as a rapid optimization tool for predicting optimal design parameters in a power matched Villard Voltage doubler.

Modifications of the power matched Villard voltage doublers to reduce parasitic losses are developed in Chapter 4. To reduce losses incurred from parasitic losses at the input of the Villard voltage doubler, a parasitic resistant matching network is presented and analyzed. Subsequent fabrication and measurement demonstrate a 70 percent improvement over the conventional design of a power matched Villard voltage doubler. In addition, threshold voltage losses are minimized through the novel modification of the Villard voltage doubler through a PMOS with floating body to enable sacrificial current biasing resulting in an additional 50 percent RF to DC conversion efficiency. The cumulative effect of these design improvements is a more than doubling (126% improvement) in RF to DC power conversion efficiency. A

newly reported result of this work identified that when implementing techniques to remove threshold voltage, the slope of the diode connected MOSFET's I-V curve limits RF scavenging performance. In the IBM 130 nm process utilized in this work, the standard MOSFET displays a larger slope to the I-V curve than MOSFET options that implement doping techniques to lower the threshold voltage. Thus, the conclusion of prior work in the literature that low threshold voltage MOSFETs are preferable is not correct. The design improvements presented in this work result in an RF energy scavenging system that demonstrates superior performance to current commercial products.

To further enhance the operational lifetime of Smartdust sensor nodes, in Chapter 5 this work presents a Smartdust receiver topology compatible with voltage levels produced by the RF energy scavenging work in chapter 4 (1 V), that lowers power consumption through the novel use of an RF power harvesting circuit to improve sensitivity. This technique is demonstrated to improve sensitivity by over 17 dB at no additional power consumption. In addition, the novel ability of this technique to reduce bandwidth and thereby improve rejection of interfering signals, as well as improve dynamic range, is studied and validated. Given the poor propagation environment of Smartdust sensor networks, to meet the sensitivity requirement necessary to transmit data over 10 meters, RF gain is necessary in the LNA of the non-coherent OOK receiver architecture presented in this work. To achieve sufficient gain to meet the required receiver sensitivity, this work presents a novel methodology to optimize a multi-stage low noise amplifier to meet receiver NF requirements at

minimal supply power consumption. Through the application of this methodology, an LNA generating 46 dB of gain with a NF of 2.85 dB while consuming just 1.6 mW of power has been fabricated and measured. Utilizing these design improvements, a full RF to digital level non-coherent OOK receiver has been fabricated and tested that demonstrates a -90 dBm sensitivity while consuming just 1.6 nJ/bit received. This represents a 30 dB increase in sensitivity over receiver designs of comparable energy draw and an order of magnitude decrease in power consumption versus receiver designs of comparable sensitivity.

The realization of Smartdust sensor networks is a project of considerable ambition and challenge. The success achieved by this work in RF energy scavenging and ultra-low power received design, represent major contributions towards the completion of a Smartdust sensor node. Given a modest duty cycle of ~1%, the research presented by this work could enable the design of a sensor node unconstrained by operational life time limitations. The work presented by this research is implemented completely in CMOS with very modest die space requirements, therefore the cost of implementation of a Smartdust node can be measured in pennies per node resulting from economies of scale in CMOS fabrication. Such a system would have advantages in cost, flexibility, rapid deployment and robustness that could lead to the application of Smartdust sensor networks in all aspects of life.

Appendix A – Derivation of Select Results

This appendix presents derivations of equations novel to this work that have not been previously derived in the main text.

Output voltage of the Villard voltage doubler resulting from the RF power source depicted in Fig. 62 (Derivation Appendix A). (Eqn. 47 p. 128)

The real power transferred to a Villard voltage doubler as represented by the load Z_{in} in Fig. 62 can be expressed as:

$$P_{in} = \mathrm{Re}\left\{V_{in} \cdot {I_{in}}^{*}\right\} = \mathrm{Re}\left\{V_{in} \cdot \left(\frac{V_{in}}{Z_{in}}\right)^{*}\right\} \tag{1}$$

$$P_{in} = \left|V_{in}\right|^{2} \mathrm{Re}\left\{\left(\frac{1}{Z_{in}}\right)^{*}\right\} \tag{2}$$

$$P_{in} = \left|V_{in}\right|^{2} \mathrm{Re}\left\{\frac{Z_{in}}{\left|Z_{in}\right|^{2}}\right\} \tag{3}$$

$$P_{in} = \frac{\left|V_{in}\right|^{2}}{\left|Z_{in}\right|} \mathrm{Re}\left\{\frac{Z_{in}}{\left|Z_{in}\right|}\right\} \tag{4}$$

$$P_{in} = \frac{\left|V_{in}\right|^{2}}{\left|Z_{in}\right|} \cos(\varphi) \tag{5}$$

Where φ is the phase angle between the real and imaginary components of the voltage doubler impedance. In addition for a power matched source of impedance R_{source}, the real power transferred must equal:

$$P_{in} = \frac{\left(\frac{V_{source}}{2}\right)^2}{R_{source}} \tag{6}$$

These two expressions for P_{in} can be equated and solved for V_{in}:

$$V_{in} = \frac{V_{source}}{2}\sqrt{\frac{|Z_{in}|}{R_{source}\cdot\cos(\phi)}} \tag{7}$$

Given that a Villard voltage doubler doubles the voltage incident at its input minus a threshold voltage, the output voltage can be expressed as:

$$V_{out} = 2\cdot V_{in} - 2\cdot V_{th} \tag{7}$$

Insertion of V_{in} above into the equation for V_{out} results in the final equation:

$$V_{output} = V_{source}\sqrt{\frac{|Z_{in}|}{R_{source}\cdot\cos(\phi)}} - 2\cdot V_{th} \tag{9}$$

Conditions under which the power matched Villard voltage doubler will outperform a non power matched Villard voltage doubler (Derivation Appendix A). (Eqn. 49 p. 128)

Power matching improves the power output of a Villard voltage doubler when:

$$Pout_{matched} > Pout_{unmatched} \quad (1)$$

Which can be simplified to:

$$\frac{Vout_{matched}^{2}}{R_{out}} > \frac{Vout_{unmatched}^{2}}{R_{out}} \quad (2)$$

And, finally:

$$Vout_{matched} > Vout_{unmatched} \quad (3)$$

The previously derived Eqn. 47 presents an expression for $Vout_{matched}$:

$$Vout_{matched} = V_{source}\sqrt{\frac{|Z_{in}|}{R_{source}\cdot\cos(\phi)}} - 2\cdot V_{th} \quad (4)$$

Furthermore, for an unmatched RF power harvesting circuit as depicted in Fig. 63, at RF frequencies the capacitive element of the RF power harvesting circuit results in a highly reactive load where:

$$R_{source} << |Z_{in}| \quad (5)$$

Thus, $Vin_{unmatched}$ can be expressed as:

$$Vin_{matched} = V_{source} \quad (6)$$

And the voltage doubling nature of the Villard voltage doubler results in a $Vout_{unmatched}$ of:

$$Vin_{matched} = 2 \cdot V_{source} - 2 \cdot V_{th} \tag{7}$$

The expressions for $Vout_{matched}$ and $Vout_{unmatched}$ can now be applied to (6) resulting in:

$$V_{source}\sqrt{\frac{|Z_{in}|}{R_{source} \cdot \cos(\phi)}} - 2 \cdot V_{th} > 2 \cdot V_{source} - 2 \cdot V_{th} \tag{8}$$

And simplifies to:

$$V_{source}\sqrt{\frac{|Z_{in}|}{R_{source} \cdot \cos(\phi)}} > 2 \cdot V_{source} \tag{9}$$

$$\sqrt{\frac{|Z_{in}|}{R_{source} \cdot \cos(\phi)}} > 2 \tag{10}$$

Thus, deriving the inequality of Eqn. 49 for the condition under which power matching out performs a non power matched system.

Noise figure (NF) of the non-coherent OOK receiver depicted in Fig. 76 (Derivation Appendix A). (Eqn. 52 p. 152)

The Friis formula states that for a receiver of n stages:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 \cdot G_2} + \frac{NF_4 - 1}{G_1 \cdot G_2 \cdot G_3} + \ldots \quad (1)$$

Thus application of the Friis formula to the non-coherent OOK receiver depicted in Fig. 76 yields:

$$NF_{receiver} = NF_{n\_stage\_LNA} + \frac{NF_{DEMOD} - 1}{G_{n\_stage\_LNA}} + \frac{NF_{BB} - 1}{G_{DEMOD} \cdot G_{n\_stage\_LNA}} \quad (2)$$

For a passive demodulator that attenuates the signal as is the case with any type of envelope detector or RF energy scavenger then the noise figure of the demodulator is equivalent to the signal attenuation. Signal attenuation is defines as the inverse of gain. Thus:

$$NF_{DEMOD} = \frac{1}{G_{DEMOD}} \quad (3)$$

Which allows the expression for the noise figure of the receiver to be simplified to:

$$NF_{receiver} = NF_{n\_stage\_LNA} + \frac{\frac{1}{G_{DEMOD}} - 1}{G_{n\_stage\_LNA}} + \frac{NF_{BB} - 1}{G_{DEMOD} \cdot G_{n\_stage\_LNA}} \quad (4)$$

$$NF_{receiver} = NF_{n\_stage\_LNA} + \frac{NF_{DEMOD} - 1}{G_{n\_stage\_LNA}} + \frac{NF_{DEMOD} \cdot (NF_{BB} - 1)}{G_{n\_stage\_LNA}} \quad (5)$$

$$NF_{receiver} = NF_{n\_stage\_LNA} + \frac{NF_{DEMOD} - 1 + NF_{DEMOD} \cdot NF_{BB} - NF_{DEMOD}}{G_{n\_stage\_LNA}} \quad (6)$$

$$NF_{receiver} = NF_{n\_stage\_LNA} + \frac{NF_{DEMOD} \cdot NF_{BB} - 1}{G_{n\_stage\_LNA}} \quad (7)$$

The noise figure of the demodulator is highly lossy and as a result $NF_{DEMOD} >> 1$ simplifying the expression for the noise figure to:

$$NF_{receiver} = NF_{n\_stage\_LNA} + \frac{NF_{DEMOD} \cdot NF_{BB}}{G_{n\_stage\_LNA}} \quad (8)$$

And finally given the relationship between the noise figure and gain of a non coherent envelope detector or RF energy harvesting circuit, the noise figure of the receiver can be expressed as:

$$NF_{receiver} = NF_{n\_stage\_LNA} + \frac{NF_{BB}}{G_{DEMOD} \cdot G_{n\_stage\_LNA}} \quad (9)$$

Demodulation Response of a Villard Voltage Doubler to an AC signal

(Eqn. 57-Eqn. 62 p. 158-161)

Equations (1) and (2) can be derived through the application of Kirchhoff's current law at the nodes corresponding to voltage levels X and Y in Fig. 82.

$$\frac{X-Y}{R_{leak}} = \frac{Y}{R_{leak}} + C_2 \frac{d}{dt} Y \tag{1}$$

$$-C_1 \frac{d}{dt} X = \frac{X-Y}{R_{leak}} + \frac{X}{n \cdot R_{leak}} \tag{2}$$

Through algebraic manipulation and differentiation (2) becomes

$$Y = R_{leak} \cdot C_1 \frac{d}{dt} X + X \cdot \left(1 + \frac{1}{n}\right) \tag{3}$$

$$\frac{d}{dt} Y = R_{leak} \cdot C_1 \frac{d^2}{dt^2} X + \frac{d}{dt} X \cdot \left(1 + \frac{1}{n}\right) \tag{4}$$

By plugging (3) and (4) into (1)

$$\frac{X - R_{leak} \cdot C_1 \frac{d}{dt} X - X \cdot \left(1 + \frac{1}{n}\right)}{R_{leak}} = \frac{R_{leak} \cdot C_1 \frac{d}{dt} X + X \cdot \left(1 + \frac{1}{n}\right)}{R_{leak}} + C_2 \left(R_{leak} \cdot C_1 \frac{d^2}{dt^2} X + \frac{d}{dt} X \cdot \left(1 + \frac{1}{n}\right)\right) \tag{5}$$

$$\frac{X - 2 \cdot R_{leak} \cdot C_1 \frac{d}{dt} X - 2 \cdot X \cdot \left(1 + \frac{1}{n}\right)}{R_{leak}} = C_2 \left(R_{leak} \cdot C_1 \frac{d^2}{dt^2} X + \frac{d}{dt} X \cdot \left(1 + \frac{1}{n}\right)\right) \tag{6}$$

$$\frac{-X \cdot \left(1 + \frac{2}{n}\right) - 2 \cdot R_{leak} \cdot C_1 \frac{d}{dt} X}{R_{leak}} = C_2 \left(R_{leak} \cdot C_1 \frac{d^2}{dt^2} X + \frac{d}{dt} X \cdot \left(1 + \frac{1}{n}\right)\right) \tag{7}$$

$$-\frac{X \cdot \left(1 + \frac{2}{n}\right)}{R_{leak}} - 2 \cdot C_1 \frac{d}{dt} X = C_2 \cdot R_{leak} \cdot C_1 \frac{d^2}{dt^2} X + C_2 \cdot \frac{d}{dt} X \cdot \left(1 + \frac{1}{n}\right) \tag{8}$$

$$0 = C_2 \cdot R_{leak} \cdot C_1 \frac{d^2}{dt^2} X + \left(2 \cdot C_1 + C_2 \cdot \left(1 + \frac{1}{n} \right) \right) \frac{d}{dt} X + \frac{X \cdot \left(1 + \frac{2}{n} \right)}{R_{leak}} \tag{9}$$

$$0 = \frac{d^2}{dt^2} X + \frac{\left(2 \cdot C_1 + C_2 \cdot \left(1 + \frac{1}{n} \right) \right)}{C_2 \cdot R_{leak} \cdot C_1} \frac{d}{dt} X + \frac{X \cdot \left(1 + \frac{2}{n} \right)}{R_{leak} \cdot C_2 \cdot R_{leak} \cdot C_1} \tag{10}$$

And to simplify (10) we define the constants A, B and C resulting in (12):

$$A = 1 \qquad B = \frac{\left(2 \cdot C_1 + C_2 \cdot \left(1 + \frac{1}{n} \right) \right)}{C_2 \cdot R_{leak} \cdot C_1} \qquad C = \frac{\left(1 + \frac{2}{n} \right)}{C_2 \cdot {R_{leak}}^2 \cdot C_1} \tag{11}$$

$$0 = A \cdot \frac{d^2}{dt^2} X + B \cdot \frac{d}{dt} X + C \cdot X \tag{12}$$

(12) is a second order differential equation and results in the auxiliary equation:

$$0 = A \cdot r^2 + B \cdot r + C \tag{13}$$

Using the quadratic formula we get:

$$r = \frac{-B \pm \sqrt{B^2 - 4 \cdot A \cdot C}}{2 \cdot A} \tag{14}$$

And by plugging (11) into (14), we get:

$$r = \frac{-\frac{\left(2 \cdot C_1 + C_2 \cdot \left(1 + \frac{1}{n} \right) \right)}{C_2 \cdot R_{leak} \cdot C_1} \pm \sqrt{\left(\frac{\left(2 \cdot C_1 + C_2 \cdot \left(1 + \frac{1}{n} \right) \right)}{C_2 \cdot R_{leak} \cdot C_1} \right)^2 - 4 \cdot \frac{\left(1 + \frac{2}{n} \right)}{R_{leak} \cdot C_2 \cdot R_{leak} \cdot C_1}}}{2} \tag{15}$$

Which simplifies to:

$$r = \frac{-\frac{\left(2\cdot C_1 + C_2\cdot\left(1+\frac{1}{n}\right)\right)}{C_2\cdot C_1} \pm \sqrt{\left(\frac{\left(2\cdot C_1 + C_2\cdot\left(1+\frac{1}{n}\right)\right)}{C_2\cdot C_1}\right)^2 - 4\cdot\frac{\left(1+\frac{2}{n}\right)}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \tag{16}$$

$$r = \frac{-\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) \pm \sqrt{\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right)^2 - 4\cdot\frac{\left(1+\frac{2}{n}\right)}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \tag{17}$$

$$r = \frac{-\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) \pm \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1+\frac{1}{n}\right)^2}{C_1^{\,2}} + \frac{4\left(1+\frac{1}{n}\right)}{C_2\cdot C_1} - 4\cdot\frac{\left(1+\frac{2}{n}\right)}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \tag{18}$$

$$r = \frac{-\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) \pm \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1+\frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \tag{19}$$

We explicitly define each solution of r:

$$r^{+} = \frac{-\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) + \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1+\frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \tag{20}$$

$$r^{-} = \frac{-\left(\frac{2}{C_2} + \frac{\left(1+\frac{1}{n}\right)}{C_1}\right) - \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1+\frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \tag{21}$$

Given that (20 and (21) must always be positive, the auxiliary equation in (13) has a general solution of the form:

$$X = K_1 \cdot e^{r^+ t} + K_2 \cdot e^{r^- t} \tag{22}$$

Boundary condition that the voltage equals V_1 at t = 0 give us:

$$K_1 + K_2 = V_1 \tag{23}$$

A second boundary condition is obtained by plugging (22) into (2):

$$-C_1 \tfrac{d}{dt}\left(K_1 \cdot e^{r^+ t} + K_2 \cdot e^{r^- t}\right) = \frac{\left(1+\frac{1}{n}\right)\cdot K_1 \cdot e^{r^+ t} + \left(1+\frac{1}{n}\right)\cdot K_2 \cdot e^{r^- t} - Y}{R_{leak}} \tag{24}$$

Which simplifies to:

$$-R \cdot C_1 \cdot \left(K_1 \cdot r^+ \cdot e^{r^+ t} + K_2 \cdot r^- \cdot e^{r^- t}\right) = \left(1+\frac{1}{n}\right)\cdot K_1 \cdot e^{r^+ t} + \left(1+\frac{1}{n}\right)\cdot K_2 \cdot e^{r^- t} - Y \tag{25}$$

And has a boundary condition of $Y=V_2$ at t=0, resulting in:

$$-R_{leak} \cdot C_1 \cdot \left(K_1 \cdot r^+ + K_2 \cdot r^-\right) = \left(1+\frac{1}{n}\right)\cdot K_1 + \left(1+\frac{1}{n}\right)\cdot K_2 - V_2 \tag{26}$$

And simplifies to:

$$\left(R_{leak} \cdot C_1 \cdot K_1 \cdot r^+ + \left(1+\frac{1}{n}\right)\cdot K_1\right) + \left(R_{leak} \cdot C_1 \cdot K_2 \cdot r^- + \left(1+\frac{1}{n}\right)\cdot K_2\right) = V_2 \tag{27}$$

$$\left(R_{leak} \cdot C_1 \cdot r^+ + \left(1+\frac{1}{n}\right)\right)\cdot K_1 + \left(R_{leak} \cdot C_1 \cdot r^- + \left(1+\frac{1}{n}\right)\right)\cdot K_2 = V_2 \tag{28}$$

Solving (23) for K_1, we get:

$$K_1 = V_1 - K_2 \tag{29}$$

And can plug (29) into (28) resulting in:

$$\left(R_{leak} \cdot C_1 \cdot r^+ + \left(1+\frac{1}{n}\right)\right)\cdot \left(V_1 - K_2\right) + \left(R_{leak} \cdot C_1 \cdot r^- + \left(1+\frac{1}{n}\right)\right)\cdot K_2 = V_2 \tag{30}$$

Which can be solved for K_2:

$$-\left(R_{leak}\cdot C_1\cdot r^{+}+\left(1+\frac{1}{n}\right)\right)\cdot K_2+\left(R_{leak}\cdot C_1\cdot r^{-}+\left(1+\frac{1}{n}\right)\right)\cdot K_2=V_2-\left(R_{leak}\cdot C_1\cdot r^{+}+\left(1+\frac{1}{n}\right)\right)\cdot V_1 \quad (31)$$

$$\left(-R_{leak}\cdot C_1\cdot r^{+}+R_{leak}\cdot C_1\cdot r^{-}\right)\cdot K_2=V_2-\left(R_{leak}\cdot C_1\cdot r^{+}+\left(1+\frac{1}{n}\right)\cdot\right)\cdot V_1 \quad (32)$$

$$R_{leak}\cdot C_1\cdot\left(-r^{+}+r^{-}\right)\cdot K_2=V_2-\left(R_{leak}\cdot C_1\cdot r^{+}+\left(1+\frac{1}{n}\right)\right)\cdot V_1 \quad (33)$$

$$K_2=\frac{\left(R_{leak}\cdot C_1\cdot r^{+}+\left(1+\frac{1}{n}\right)\right)\cdot V_1-V_2}{R_{leak}\cdot C_1\cdot\left(+r^{+}-r^{-}\right)} \quad (34)$$

And then (34) can be plugged into (29) to get K_1:

$$K_1=V_1-\frac{\left(R_{leak}\cdot C_1\cdot r^{+}+\left(1+\frac{1}{n}\right)\right)\cdot V_1-V_2}{R_{leak}\cdot C_1\cdot\left(+r^{+}-r^{-}\right)} \quad (35)$$

So to Summarize, the Voltage at location X as a function of time is:

$$X=K_1\cdot e^{r^{+}t}+K_2\cdot e^{r^{-}t} \quad (36)$$

Where:

$$r^{+}=\frac{-\left(\frac{2}{C_2}+\frac{\left(1+\frac{1}{n}\right)}{C_1}\right)+\sqrt{\frac{4}{{C_2}^2}+\frac{\left(1+\frac{1}{n}\right)^2}{{C_1}^2}-\frac{4/n}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \quad (37)$$

$$r^{-}=\frac{-\left(\frac{2}{C_2}+\frac{\left(1+\frac{1}{n}\right)}{C_1}\right)-\sqrt{\frac{4}{{C_2}^2}+\frac{\left(1+\frac{1}{n}\right)^2}{{C_1}^2}-\frac{4/n}{C_2\cdot C_1}}}{R_{leak}\cdot 2} \quad (38)$$

and

$$K_1 = V_1 - \frac{\left(R_{leak} \cdot C_1 \cdot r^+ + \left(1 + \frac{1}{n}\right)\right) \cdot V_1 - V_2}{R_{leak} \cdot C_1 \cdot \left(+r^+ - r^-\right)} \tag{39}$$

$$K_2 = \frac{\left(R_{leak} \cdot C_1 \cdot r^+ + \left(1 + \frac{1}{n}\right)\right) \cdot V_1 - V_2}{R_{leak} \cdot C_1 \cdot \left(+r^+ - r^-\right)} \tag{40}$$

r+ and r- result in two RC time constants of:

$$RC_1 = \frac{R_{leak} \cdot 2}{\left(\frac{2}{C_2} + \frac{\left(1 + \frac{1}{n}\right)}{C_1}\right) - \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1 + \frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2 \cdot C_1}}} \tag{41}$$

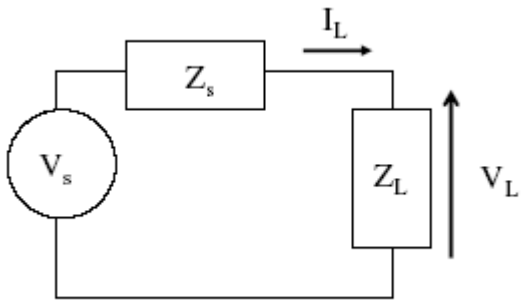
$$RC_2 = \frac{R_{leak} \cdot 2}{\left(\frac{2}{C_2} + \frac{\left(1 + \frac{1}{n}\right)}{C_1}\right) + \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1 + \frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2 \cdot C_1}}} \tag{42}$$

The bandwidth of the demodulator will be limited by the larger of the two RC time constants which corresponds to RC_1 resulting in a bandwidth of:

$$BW = \frac{\left(\frac{2}{C_2} + \frac{\left(1 + \frac{1}{n}\right)}{C_1}\right) - \sqrt{\frac{4}{C_2^{\,2}} + \frac{\left(1 + \frac{1}{n}\right)^2}{C_1^{\,2}} - \frac{4/n}{C_2 \cdot C_1}}}{R_{leak} \cdot 2} \tag{44}$$

3 dB bandwidth of the power matched Villard voltage doubler (Derivation Appendix A). (Eqn. 63 p. 163)

The resonant matching circuit of a power matched Villard voltage doubler can be modeled as:



Where

$$Z_s = R_{source} + R_{paras} + j \cdot \omega \cdot L_{matching}$$

$$Z_L = R_{scavenger} - \frac{j}{\omega \cdot C_{scavenger}}$$

The time averaged power dissipated across Z_L is:

$$P_L = \frac{1}{2} \cdot \mathrm{Re}\left\{V_L \cdot I_L{}^*\right\} \tag{1}$$

Where

$$V_L = V_s \cdot \frac{Z_L}{Z_s + Z_L} \tag{2}$$

$$I_L = \frac{V_s}{Z_s + Z_L} \tag{3}$$

Thus

$$P_L = \frac{1}{2} \cdot \mathrm{Re}\left\{V_s \cdot \frac{Z_L}{Z_s + Z_L} \cdot \left(\frac{V_s}{Z_s + Z_L}\right)^*\right\}$$

$$= \frac{1}{2} \cdot \frac{\left|V_s\right|^2 \cdot R_{scavenger}}{\left(R_{source} + R_{paras} + R_{scavenger}\right)^2 + \left(j \cdot \omega \cdot L_{matching} - \frac{j}{\omega \cdot C_{scavenger}}\right)^2} \tag{4}$$

We know from the theory of maximum power transfer that maximum power is transferred when

$$j \cdot \omega \cdot L_{matching} = \frac{j}{\omega \cdot C_{scavenger}} \tag{5}$$

Resulting in

$$P_{MAX} = \frac{1}{2} \cdot \frac{\left|V_s\right|^2 \cdot R_{scavenger}}{\left(R_{source} + R_{paras} + R_{scavenger}\right)^2} \tag{6}$$

Given that the Villard voltage doubler acts as a square law detector, the 3db bandwidth can be derived from:

$$\frac{1}{\sqrt{2}} = \frac{P_L}{P_{MAX}} \tag{7}$$

And solving for ω we get

$$\frac{1}{\sqrt{2}} = \frac{\frac{1}{2} \cdot \frac{\left|V_s\right|^2 \cdot R_{scavenger}}{\left(R_{source} + R_{paras} + R_{scavenger}\right)^2 + \left(j \cdot \omega \cdot L_{matching} - \frac{j}{\omega \cdot C_{scavenger}}\right)^2}}{\frac{1}{2} \cdot \frac{\left|V_s\right|^2 \cdot R_{scavenger}}{\left(R_{source} + R_{paras} + R_{scavenger}\right)^2}} \tag{8}$$

$$\frac{1}{\sqrt{2}} = \frac{\left(R_{source} + R_{paras} + R_{scavenger}\right)^2}{\left(R_{source} + R_{paras} + R_{scavenger}\right)^2 + \left(j \cdot \omega \cdot L_{matching} - \frac{j}{\omega \cdot C_{scavenger}}\right)^2} \tag{9}$$

$$j \cdot \omega \cdot L_{matching} - \frac{j}{\omega \cdot C_{scavenger}} = \pm\sqrt{\sqrt{2} - 1}\left(R_{source} + R_{paras} + R_{scavenger}\right) \tag{10}$$

$$0 = L_{matching} \cdot \omega^2 \pm \sqrt{\sqrt{2} - 1}\left(R_{source} + R_{paras} + R_{scavenger}\right) \cdot \omega - \frac{1}{C_{scavenger}} \tag{11}$$

Application of the quadratic formula yields two positive roots:

$$\omega = \pm \frac{\sqrt{\sqrt{2}-1}\cdot\left(R_{source}+R_{paras}+R_{scavenger}\right)}{2\cdot L_{matching}} \mu \frac{\sqrt{\left(\sqrt{2}-1\right)\cdot\left(R_{source}+R_{paras}+R_{scavenger}\right)^2+4\cdot\frac{L_{matching}}{C_{scavenge}}}}{2\cdot L_{matching}} \quad (12)$$

Finally the bandwidth is equal to:

$$BW_{3dB} = \omega^{+} - \omega^{-} = \frac{\sqrt{\sqrt{2}-1}\cdot\left(R_{source}+R_{paras}+R_{scavenger}\right)}{L_{matching}} \quad (13)$$

And given that in a resonant network

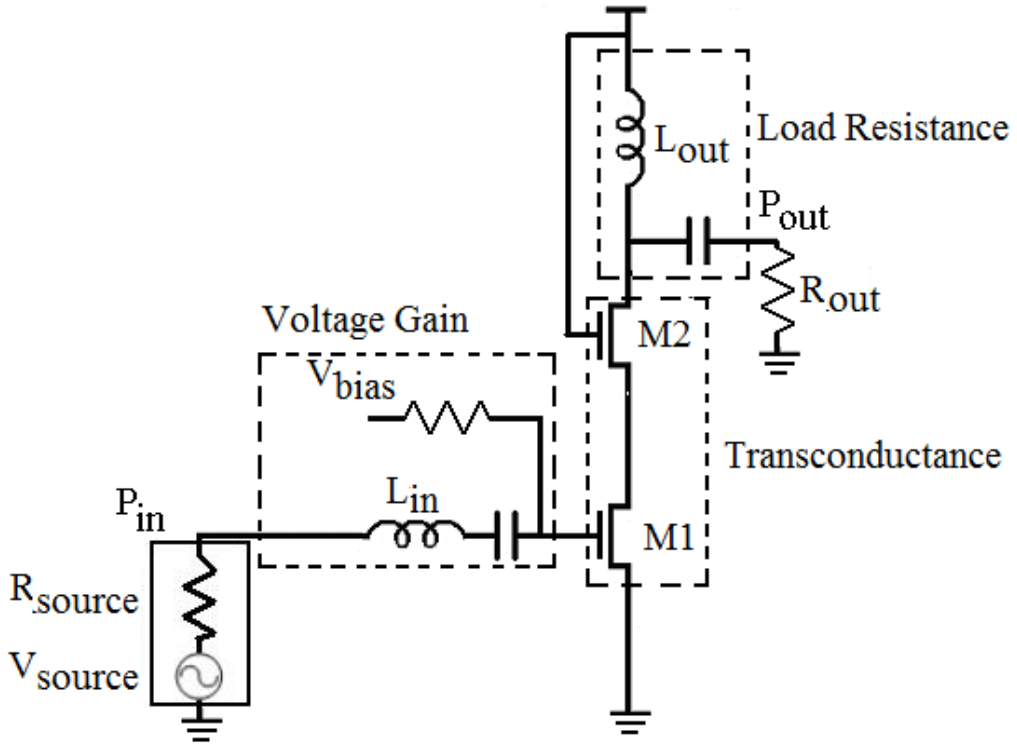
$$L_{matching} = \frac{1}{\omega_0^{\,2}\cdot C_{scavenger}} \quad (14)$$

BW_{3dB} can also be expressed as:

$$BW_{3dB} = \sqrt{\sqrt{2}-1}\cdot\left(R_{source}+R_{paras}+R_{scavenger}\right)\cdot 2\cdot\pi\cdot f_0^{\,2}\cdot C_{scavenger} \quad (15)$$

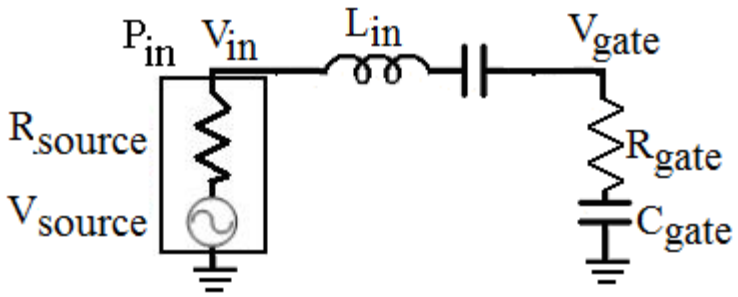
Power gain common source cascode LNA (Derivation Appendix A).

(Eqn. 81 p. 172)



The gain from a power matched Common source cascode LNA can be derived as a function of the input voltage gain, the transconductance of M_1 and M_2, and the load resistance.

The Voltage gain is derived through recognition that the voltage at the gate of M_1 is the result of a series resonant circuit as depicted below.



The voltage gain (V_{gate}/V_{in}) for a series resonant circuit is:

$$Q_{in} = \frac{1}{2 \cdot \pi \cdot f \cdot C_{gate} \cdot \left(R_{source} + R_{gate}\right)} \tag{1}$$

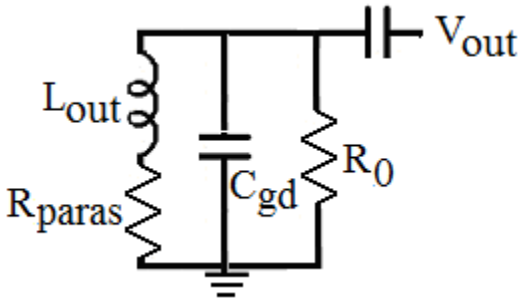
The total transconductance from M_1 and M_2 is dominated by the transconductance of M_1 [Gray]. Thus, the transconductance in strong inversion is:

$$g_m = \frac{2 \cdot I_{ds}}{V_{GS} - V_{th}} \tag{2}$$

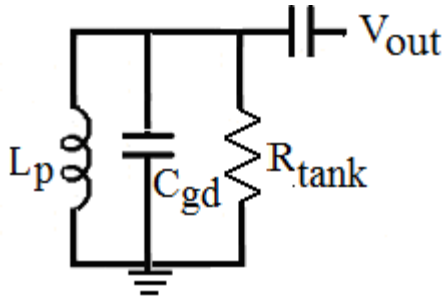
And in weak inversion the transconductance is:

$$g_m = \frac{I_{ds}}{n \cdot V_t} \tag{3}$$

The load resistance including parasitics can be depicted as:



These parasitics can be simplified as a parallel RLC circuit of:



Where

$$R_{\tan k} = \frac{R_{paras} \cdot \left(1 + \left(\frac{\omega \cdot L_{out}}{R_{paras}}\right)^2\right) \cdot R_0}{R_{paras} \cdot \left(1 + \left(\frac{\omega \cdot L_{out}}{R_{paras}}\right)^2\right) + R_0} \tag{4}$$

And

$$L_p = \frac{\left(\frac{\omega \cdot L_{out}}{R_{paras}}\right) \cdot R_{\tan k}}{\omega} \tag{5}$$

Assuming the load has been impedance matched to the output impedance of the LNA, the real power transferred to the load can be derived as in (8). A proof that power matching to the output load, improves power transfer is presented in the next derivation.

$$P_{load} = \left(g_m \cdot V_{gate}\right)^2 \cdot \frac{R_{\tan k}}{2} \tag{6}$$

$$P_{load} = \left(g_m \cdot \frac{1}{2 \cdot \pi \cdot f \cdot C_{gate} \cdot \left(R_{source} + R_{gate}\right)} \cdot V_{in}\right)^2 \cdot \frac{R_{\tan k}}{2} \tag{7}$$

The total power gain is the ratio of input power to power applied to the load:

$$G_{power} = \frac{\left(g_m \cdot \frac{1}{2 \cdot \pi \cdot f \cdot C_{gate} \cdot \left(R_{source} + R_{gate} \right)} \cdot V_{in} \right)^2 \cdot \frac{R_{\tan k}}{2}}{\frac{{V_{in}}^2}{R_{source}}} \tag{8}$$

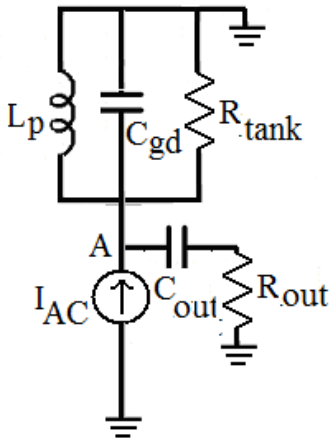
$$P_{gain} = \left(g_m \cdot Q_{in} \right)^2 \cdot \frac{R_{\tan k}}{2} \cdot R_{source} \tag{9}$$

$$P_{gain}(dB) = 10 \cdot \log\left(\left(g_m \cdot Q_{in} \right)^2 \cdot \frac{R_{\tan k}}{2} \cdot R_{source} \right) \tag{10}$$

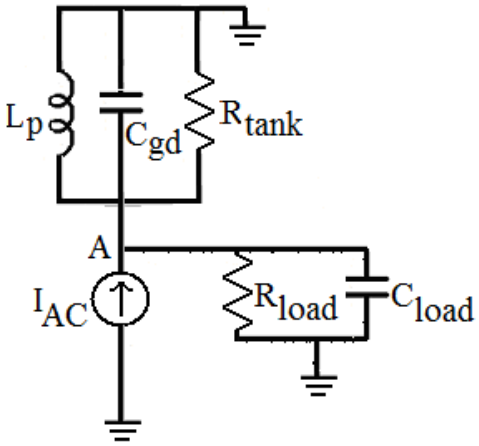
Thus, the power gain of the common source cascode LNA has been derived.

Proof that impedance matching the output impedance of an LNA maximizes power transfer to the load (p. 172)

The decision to power match to the output of the LNA can be justified by modeling the output circuit, MOSFET current source, and output load that power is delivered to:



The circuit can be modified such that the output impedance R_{out} and C_{out} can be converted to the equivalent parallel elements R_{load} and C_{load}.



By applying Kirchhoff's current law, we can equate the currents at point A:

$$I_{AC} = \frac{V_A}{X_p} + \frac{V_A}{X_{gd}} + \frac{V_A}{X_{load}} + \frac{V_A}{R_{tank}} + \frac{V_A}{R_{load}} \quad (1)$$

$$I_{AC} = V_A \cdot \left(\frac{1}{X_p} + \frac{1}{X_{gd}} + \frac{1}{R_{\tan k}} + \frac{1}{X_{load}} + \frac{1}{R_{load}} \right) \tag{2}$$

$$I_{AC} = V_A \cdot \left(\frac{1}{j \cdot \omega \cdot L_p} - \frac{\omega \cdot C_{gd}}{j} + \frac{1}{R_{\tan k}} - \frac{\omega \cdot C_{load}}{j} + \frac{1}{R_{load}} \right) \tag{3}$$

$$I_{AC} = V_A \cdot \left(\frac{1}{j \cdot \omega \cdot L_p} - \frac{\omega \cdot \left(C_{gd} + C_{load} \right)}{j} + \frac{1}{R_{\tan k}} + \frac{1}{R_{load}} \right) \tag{4}$$

$$I_{AC} = V_A \cdot \left(\frac{1}{j} \left(\frac{1}{\omega \cdot L_p} - \omega \cdot \left(C_{gd} + C_{load} \right) \right) + \left(\frac{R_{\tan k} + R_{load}}{R_{\tan k} \cdot R_{load}} \right) \right) \tag{5}$$

Now, by solving for the voltage at point A we get:

$$V_A = \frac{I_{AC}}{\left(\left(\frac{R_{\tan k} + R_{load}}{R_{\tan k} \cdot R_{load}} \right) - j \left(\frac{1}{\omega \cdot L_p} - \omega \cdot \left(C_{gd} + C_{load} \right) \right) \right)} \tag{6}$$

The power across R_{load} represents the output power and is expressed as:

$$P_{out} = \frac{\left(\frac{I_{AC}}{\left(\left(\frac{R_{\tan k} + R_{load}}{R_{\tan k} \cdot R_{load}} \right) - j \left(\frac{1}{\omega \cdot L_p} - \omega \cdot \left(C_{gd} + C_{load} \right) \right) \right)} \right)^2}{R_{load}} \tag{7}$$

It's clear upon inspection of (7) that P_{out} is maximal when

$$0 = \frac{1}{\omega \cdot L_p} - \omega \cdot \left(C_{gd} + C_{load} \right) \tag{8}$$

Allowing the simplification of (7) to:

$$P_{out} = \frac{\left(I_{AC} \cdot \left(\frac{R_{\tan k} \cdot R_{load}}{R_{\tan k} + R_{load}} \right) \right)^2}{R_{load}} = \left({I_{AC}}^2 \cdot \left(\frac{R_{\tan k} \cdot R_{load}}{R_{\tan k} + R_{load}} \right) \cdot \left(\frac{R_{\tan k}}{R_{load} + R_{\tan k}} \right) \right) \tag{9}$$

The quantity P_{out} is maximal by setting R_{tank} as high as circuit parasitics will allow and then by power matching R_{load} to R_{tank}. Therefore maximal power transfer to a load is obtained by impedance matching the output resistance R_{load} to the highest realizable R_{tank} and setting the reactance resulting from L_p, C_{gd}, and C_{load} such that they sum to zero.

Appendix B – Source Code

This appendix presents MATLAB code that implements novel algorithms and models developed from the research presented in this work.

Chapter 2 Code

RFsurvey_TIME.M: Code to acquire temporal survey data of RF energy present in the environment.

```
tic
RADIUS=.0005;
MAX_SAMPLES=30000;
VARS2STORE=6;

x=zeros(1,6);
y=zeros(1,6);

%%%% DETERMINE FILENAME FOR DATA SAVE%%%%%%%%%%%%%%%
 [filename,path]=uiputfile('*.kml','Save KML data','default.kml');
if(filename==0) break; end;

BACKUP_NAME=strread(filename,'%s','delimiter','.');

BACKUP_DATA=zeros(MAX_SAMPLES,(2+2*VARS2STORE+1));


%%%%%%%%%%%%%%%%% INIT HARDWARE%%%%%%%%%%%%%%%%%
s1=INIT_GPS();
S2=INIT_Scope();
j=1;

query_Scope(S2,'*IDN?')
write_Scope(S2,':FREQ:SPAN 2900000000');
write_Scope(S2,':FREQ:CENTER 1500000000');
write_Scope(S2,':CALCulate:MARKer:ALL');
write_Scope(S2,':AVER:TRACe1:STAT ON');
write_Scope(S2,':AVER:TRACe1:COUNT 2');

%%%%%%%%%%%%%%%%% ACQUIRE GPS DATA %%%%%%%%%%%%%%%
   DATA=read_GPS(s1);
   LOCy=DATA(2);
   LOCx=DATA(4);

%%% CONVERT NMEA GPS DATA TO LATTITUDE/LONGITUDE%%%%%%%%
```

```
    LOCx=floor(LOCx/100)+((mod(LOCx,100))/60);
    LOCy=floor(LOCy/100)+((mod(LOCy,100))/60);


    if(char(DATA(5))=='W')
       LOCx=LOCx*-1;
    end
    if(char(DATA(3))=='S')
       LOCy=LOCy*-1;
    end

%%%%%%%%%%%%% REPEATE UNTIL KEYSTROKE %%%%%%%%%%%%%
while j<(MAX_SAMPLES)+1

%%%%%%%%%%%% ACQUIRE RF SURVEY DATA %%%%%%%%%%%%%%%%

    write_Scope(S2,':CALCulate:MARKer:ALL')

    x(1)=str2num(query_Scope(S2,':CALCulate:MARK1:X?'));
    y(1)=str2num(query_Scope(S2,':CALCulate:MARK1:Y?'));
    x(2)=str2num(query_Scope(S2,':CALCulate:MARK2:X?'));
    y(2)=str2num(query_Scope(S2,':CALCulate:MARK2:Y?'));
    x(3)=str2num(query_Scope(S2,':CALCulate:MARK3:X?'));
    y(3)=str2num(query_Scope(S2,':CALCulate:MARK3:Y?'));
    x(4)=str2num(query_Scope(S2,':CALCulate:MARK4:X?'));
    y(4)=str2num(query_Scope(S2,':CALCulate:MARK4:Y?'));
    x(5)=str2num(query_Scope(S2,':CALCulate:MARK5:X?'));
    y(5)=str2num(query_Scope(S2,':CALCulate:MARK5:Y?'));
    x(6)=str2num(query_Scope(S2,':CALCulate:MARK6:X?'));
    y(6)=str2num(query_Scope(S2,':CALCulate:MARK6:Y?'));

    biggest=1;
    big_val=y(1)

    for p=2:6
       if (y(p)>big_val)
          biggest=p;
          big_val=y(p)
       end
    end



%%%% STORE RAW DATA IN ARRAY FOR LATER FILE SAVE %%%%
    time_store=toc
    format long
    BACKUP_DATA(j,1)=LOCx;
    BACKUP_DATA(j,2)=LOCy;
    BACKUP_DATA(j,3)=x(1);
    BACKUP_DATA(j,4)=y(1);
    BACKUP_DATA(j,5)=x(2);
    BACKUP_DATA(j,6)=y(2);
    BACKUP_DATA(j,7)=x(3);
    BACKUP_DATA(j,8)=y(3);
    BACKUP_DATA(j,9)=x(4);
    BACKUP_DATA(j,10)=y(4);
```

```
    BACKUP_DATA(j,11)=x(5);
    BACKUP_DATA(j,12)=y(5);
    BACKUP_DATA(j,13)=x(6);
    BACKUP_DATA(j,14)=y(6);
    BACKUP_DATA(j,15)=time_store;


%%%%% PAUSE AND END DATA SURVEY ON KEY STROKE %%%%%%%%%
    j=j+1;
    if(getkeywait(60) ~= -1)
        j=MAX_SAMPLES+1;
    end

end
 %%%%%%%%%%%%% SAVE RAW ASCII DATA %%%%%%%%%%%%%%%%%


save( [path [char(BACKUP_NAME(1)) '.txt']], 'BACKUP_DATA','-ASCII', '-DOUBLE');

fclose(s1);
fclose(S2);
```

RFsurvey_SPATIAL.M: Code to acquire spatial survey data of RF energy present in the environment.

```
RADIUS=.0005;
MAX_SAMPLES=10000;
COLORS={'red','orange','yellow','green','blue','purple'};
VARS2STORE=6;

x=zeros(1,6);
y=zeros(1,6);

%%%% DETERMINE FILENAME FOR DATA SAVE%%%%%%%%%%%%%%%
[filename,path]=uiputfile('*.kml','Save KML data','default.kml');
if(filename==0) break; end;
GPS_fid=fopen([path,filename],'w');

BACKUP_NAME=strread(filename,'%s','delimiter','.');

BACKUP_DATA=zeros(MAX_SAMPLES,(2+2*VARS2STORE));

%%%% KML HEADER AND COLORS %%%%%%%%%%%%%%%%%%%%%%%%
LINE='<?xml version="1.0" encoding="UTF-8"?>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='<kml xmlns="http://earth.google.com/kml/2.2">';
fprintf(GPS_fid,'%s\n',LINE);
LINE='<Document>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='  <name>My Places.kml</name>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sh_blue">';
fprintf(GPS_fid,'%s\n',LINE);
```

```
LINE='		<IconStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<scale>1.3</scale>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<Icon>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			</Icon>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='		</IconStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='		<PolyStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<color>7fff0055</color>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='			<outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='		</PolyStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='	</Style>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='	<Style id="sh_green">';
fprintf(GPS_fid,'%s\n',LINE);
LINE='		<IconStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<scale>1.3</scale>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<Icon>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			</Icon>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='		</IconStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='		<PolyStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<color>7f00aa00</color>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='			<outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='		</PolyStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='	</Style>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='	<StyleMap id="msn_red">';
fprintf(GPS_fid,'%s\n',LINE);
LINE='		<Pair>';
fprintf(GPS_fid,'%s\n',LINE);
```

```
LINE='                        <key>normal</key>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sn_red</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>highlight</key>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sh_red</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  </StyleMap>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sn_purple">';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <IconStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <scale>1.1</scale>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <Icon>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        </Icon>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </IconStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <PolyStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <color>7f7f00aa</color>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </PolyStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='  <StyleMap id="msn_purple">';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                <Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>normal</key>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sn_purple</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>highlight</key>';
```

```
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sh_purple</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  </StyleMap>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sn_red">';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <IconStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <scale>1.1</scale>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <Icon>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        </Icon>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </IconStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <PolyStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <color>7f0000ff</color>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </PolyStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  <StyleMap id="msn_blue">';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>normal</key>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sn_blue</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>highlight</key>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sh_blue</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  </StyleMap>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  <StyleMap id="msn_green">';
 fprintf(GPS_fid,'%s\n',LINE);
```

```
LINE='              <Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <key>normal</key>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <styleUrl>#sn_green</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              <Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <key>highlight</key>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <styleUrl>#sh_green</styleUrl>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              </Pair>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  </StyleMap>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sn_blue">';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              <IconStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <scale>1.1</scale>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <Icon>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      </Icon>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              </IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              <PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <color>7fff0055</color>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              </PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sn_yellow">';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              <IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <scale>1.1</scale>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <Icon>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
  fprintf(GPS_fid,'%s\n',LINE);
```

```
LINE='                        </Icon>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                </IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                <PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <color>7f00ffff</color>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sn_green">';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                <IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <scale>1.1</scale>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <Icon>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        </Icon>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                </IconStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                <PolyStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <color>7f00aa00</color>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                </PolyStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  <StyleMap id="msn_orange">';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                <Pair>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>normal</key>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sn_orange</styleUrl>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                </Pair>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                <Pair>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>highlight</key>';
```

```
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sh_orange</styleUrl>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='              </Pair>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='  </StyleMap>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  <StyleMap id="msn_yellow">';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              <Pair>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>normal</key>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sn_yellow</styleUrl>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              </Pair>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              <Pair>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <key>highlight</key>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <styleUrl>#sh_yellow</styleUrl>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='              </Pair>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='  </StyleMap>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sh_orange">';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              <IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <scale>1.3</scale>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <Icon>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        </Icon>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              </IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              <PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <color>7f00aaff</color>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              </PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sh_red">';
  fprintf(GPS_fid,'%s\n',LINE);
```

```
LINE='              <IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <scale>1.3</scale>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <Icon>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                      </Icon>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              </IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='              <PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <color>7f0000ff</color>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              </PolyStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sn_orange">';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              <IconStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <scale>1.1</scale>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <Icon>';
    fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
    fprintf(GPS_fid,'%s\n',LINE);
LINE='                      </Icon>';
    fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='              </IconStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='              <PolyStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <color>7f00aaff</color>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                      <outline>0</outline>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='              </PolyStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sh_purple">';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='              <IconStyle>';
    fprintf(GPS_fid,'%s\n',LINE);
```

```
LINE='                        <scale>1.3</scale>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <Icon>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        </Icon>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
    fprintf(GPS_fid,'%s\n',LINE);
LINE='                </IconStyle>';
    fprintf(GPS_fid,'%s\n',LINE);
LINE='                <PolyStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <color>7f7f00aa</color>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <outline>0</outline>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                </PolyStyle>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Style id="sh_yellow">';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <IconStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <scale>1.3</scale>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <Icon>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='
<href>http://maps.google.com/mapfiles/kml/pushpin/ylw-pushpin.png</href>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        </Icon>';
   fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <hotSpot x="20" y="2" xunits="pixels" yunits="pixels"/>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                </IconStyle>';
  fprintf(GPS_fid,'%s\n',LINE);
LINE='                <PolyStyle>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <color>7f00ffff</color>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                        <outline>0</outline>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                </PolyStyle>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='  </Style>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='  <Folder>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                <name>My Places</name>';
 fprintf(GPS_fid,'%s\n',LINE);
LINE='                <open>1</open>';
  fprintf(GPS_fid,'%s\n',LINE);
```

```
        LINE='              <Style>';
           fprintf(GPS_fid,'%s\n',LINE);
        LINE='                    <ListStyle>';
          fprintf(GPS_fid,'%s\n',LINE);
        LINE='                              <listItemType>check</listItemType>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                              <ItemIcon>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                                        <state>open</state>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                                        <href>C:/Program Files/Google/Google
Earth/res/mysavedplaces_open.png</href>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                              </ItemIcon>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                              <ItemIcon>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                                        <state>closed</state>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                                        <href>C:/Program Files/Google/Google
Earth/res/mysavedplaces_closed.png</href>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                              </ItemIcon>';
         fprintf(GPS_fid,'%s\n',LINE);
        LINE='                              <bgColor>00ffffff</bgColor>';
          fprintf(GPS_fid,'%s\n',LINE);
        LINE='                    </ListStyle>';
          fprintf(GPS_fid,'%s\n',LINE);
        LINE='              </Style>';
        fprintf(GPS_fid,'%s\n',LINE);

        %%%%%%%%%%%%%%%%% INIT HARDWARE%%%%%%%%%%%%%%%%%
        s1=INIT_GPS();
        S2=INIT_Scope();
        j=1;

        query_Scope(S2,'*IDN?');
        write_Scope(S2,':FREQ:SPAN 500000000');
        write_Scope(S2,':FREQ:CENTER 720000000');
        write_Scope(S2,':CALCulate:MARKer:ALL');
        write_Scope(S2,':AVER:TRACe1:STAT ON');
        write_Scope(S2,':AVER:TRACe1:COUNT 2');

        %%%%%%%%%%%%% REPEATE UNTIL KEYSTROKE %%%%%%%%%%%%
        while j<(MAX_SAMPLES)+1
        %%%%%%%%%%%%%%%%% ACQUIRE DATA%%%%%%%%%%%%%%%%%
           DATA=read_GPS(s1);
           LOCy=DATA(2)
           LOCx=DATA(4)

           write_Scope(S2,':CALCulate:MARKer:ALL')

           x(1)=str2num(query_Scope(S2,':CALCulate:MARK1:X?'));
           y(1)=str2num(query_Scope(S2,':CALCulate:MARK1:Y?'));
           x(2)=str2num(query_Scope(S2,':CALCulate:MARK2:X?'));
           y(2)=str2num(query_Scope(S2,':CALCulate:MARK2:Y?'));
```

```
x(3)=str2num(query_Scope(S2,':CALCulate:MARK3:X?'));
y(3)=str2num(query_Scope(S2,':CALCulate:MARK3:Y?'));
x(4)=str2num(query_Scope(S2,':CALCulate:MARK4:X?'));
y(4)=str2num(query_Scope(S2,':CALCulate:MARK4:Y?'));
x(5)=str2num(query_Scope(S2,':CALCulate:MARK5:X?'));
y(5)=str2num(query_Scope(S2,':CALCulate:MARK5:Y?'));
x(6)=str2num(query_Scope(S2,':CALCulate:MARK6:X?'));
y(6)=str2num(query_Scope(S2,':CALCulate:MARK6:Y?'));


% DETERMINE KML COLOR CODING FOR MEASURED RF SIGNAL STRENGHT
biggest=1;
   big_val=y(1);

   for p=2:6
      if (y(p)>big_val)
         biggest=p
         big_val=y(p)
      end
   end

   color_choice=6

   if (big_val>-50)
      color_choice=5
   end
   if (big_val>-40)
      color_choice=4
   end
   if (big_val>-30)
      color_choice=3
   end
   if (big_val>-25)
      color_choice=2
   end
   if (big_val>-20)
      color_choice=1
   end

%%% CONVERT NMEA GPS DATA TO LATTITUDE/LONGITUDE%%%%%%%%
   LOCx=floor(LOCx/100)+((mod(LOCx,100))/60);
   LOCy=floor(LOCy/100)+((mod(LOCy,100))/60);


   if(char(DATA(5))=='W')
      LOCx=LOCx*-1;
   end
   if(char(DATA(3))=='S')
      LOCy=LOCy*-1;
   end
   %%%% STORE RAW DATA IN ARRAY FOR LATER FILE SAVE %%%%
   format long
   BACKUP_DATA(j,1)=LOCx;
   BACKUP_DATA(j,2)=LOCy;
   BACKUP_DATA(j,3)=x(1);
   BACKUP_DATA(j,4)=y(1);
```

```
BACKUP_DATA(j,5)=x(2);
BACKUP_DATA(j,6)=y(2);
BACKUP_DATA(j,7)=x(3);
BACKUP_DATA(j,8)=y(3);
BACKUP_DATA(j,9)=x(4);
BACKUP_DATA(j,10)=y(4);
BACKUP_DATA(j,11)=x(5);
BACKUP_DATA(j,12)=y(5);
BACKUP_DATA(j,13)=x(6);
BACKUP_DATA(j,14)=y(6);


%%%%%% CREATE COLORED POLYGON FOR KML FILE%%%%%%
Ax=LOCx+RADIUS;
Ay=LOCy;
Bx=LOCx+(2.2/5)*RADIUS;
By=LOCy+(1.15/2)*RADIUS;
Cx=LOCx-(2.2/5)*RADIUS;
Cy=LOCy+(1.15/2)*RADIUS;
Dx=LOCx-RADIUS;
Dy=LOCy;
Ex=LOCx-(2.2/5)*RADIUS;
Ey=LOCy-(1.15/2)*RADIUS;
Fx=LOCx+(2.2/5)*RADIUS;
Fy=LOCy-(1.15/2)*RADIUS;

LINE='                                          <Placemark>';
fprintf(GPS_fid,'%s\n',LINE);
LINE=['                                                 <name>'
char(COLORS(color_choice)) '</name>'];
fprintf(GPS_fid,'%s\n',LINE);
LINE=['                                                 <styleUrl>#msn_'
char(COLORS(color_choice)) '</styleUrl>'];
fprintf(GPS_fid,'%s\n',LINE);
LINE='                                                  <Polygon>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                                                          <tessellate>1</tessellate>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                                                          <outerBoundaryIs>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='                                                                  <LinearRing>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='
        <coordinates>';
fprintf(GPS_fid,'%s\n',LINE);
%LINE=['                ',num2str(Ax,'%f'), ',', num2str(Ay,'%f'), ',', '0
',num2str(Bx,'%f'), ',', num2str(By,'%f'), ',', '0 ', num2str(Cx,'%f'), ',', num2str(Cy,'%f'), ',', '0 ',
num2str(Dx,'%f'), ',' ,num2str(Dy,'%f'), ',' ,'0 ' ,num2str(Ax,'%f'), ',' ,num2str(Ay,'%f'), ',' ,'0
</coordinates>'];
LINE=['                ',num2str(Ax,'%f'), ',', num2str(Ay,'%f'), ',', '0
',num2str(Bx,'%f'), ',', num2str(By,'%f'), ',', '0 ', num2str(Cx,'%f'), ',', num2str(Cy,'%f'), ',', '0 ',
num2str(Dx,'%f'), ',' ,num2str(Dy,'%f'), ',' ,'0 ' ,num2str(Ex,'%f'), ',' ,num2str(Ey,'%f'), ',','0 '
,num2str(Fx,'%f'), ',' ,num2str(Fy,'%f'), ',','0 ' ,num2str(Ax,'%f'), ',' ,num2str(Ay,'%f'), ',' ,'0
</coordinates>'];
fprintf(GPS_fid,'%s\n',LINE);
LINE='                                                                  </LinearRing>';
```

```
    fprintf(GPS_fid,'%s\n',LINE);
    LINE='                                                  </outerBoundaryIs>';
    fprintf(GPS_fid,'%s\n',LINE);
    LINE='                                              </Polygon>';
    fprintf(GPS_fid,'%s\n',LINE);
    LINE='                                          </Placemark>';
    fprintf(GPS_fid,'%s\n',LINE);


%%%%% PAUSE AND END DATA SURVEY ON KEY STROKE %%%%%%%%%%
    j=j+1;
    if(getkeywait(6) ~= -1)
        j=MAX_SAMPLES+1;
    end

end

%%%%%%%%%% SAVE KML DATA AND RAW ASCII DATA %%%%%%%%%%%%
LINE='              </Folder>';
    fprintf(GPS_fid,'%s\n',LINE);
LINE='</Document>';
fprintf(GPS_fid,'%s\n',LINE);
LINE='</kml>';
fprintf(GPS_fid,'%s\n',LINE);

save( [path [char(BACKUP_NAME(1)) '.txt']], 'BACKUP_DATA','-ASCII', '-DOUBLE');

fclose(GPS_fid);
fclose(s1);
fclose(S2);
```

RFharv_MODEL.M: Code to Model Power Matched Villard Voltage Doubler Integrated onto CMOS

```
warning off all
clear

% Variables to solve over a range
Vth=.179;
Vth_length=length(Vth);
Vinc=.1:.1:1.3;
H=length(Vinc);
ns=8

% Results Storage Variables
VGS_final=zeros(Vth_length,H);
Vout=zeros(Vth_length,H);
Zload=zeros(Vth_length,H);
PinDB=zeros(Vth_length,H);
Efficiency=zeros(Vth_length,H);
RjAC_final=zeros(Vth_length,H);
RjDC_final=zeros(Vth_length,H);
ratio=zeros(Vth_length,H);
ratio_true=zeros(Vth_length,H);

% Circuit/Sim Variables
f=900e6;
Rout=1e7;
NOPARARISITICS=0;
FFTandI=1;
FC=.5;
M=.55;

%Layout/Process Variables
L=.25; % um
W=41.6; % um
n=1.1;
Vt=.026;
Eox=3.9*8.85e-14*1e-4;
Tox=3.03e-9*1e6;
Rresistivity=7;
nf=20; %number of fingers
Ivth=300e-9;
Rs_sub=30; %metal impedance and substrate
Rs_source_back=200;
CjArea=1.05e-15;
CjPer=.05e-15;
CjPerPoly=.38e-15;
gamma=.05;
un=500*.01*.01;
```

```
Rsx=20;
Y=.6;

%Dependant Variables
Weff=W-0;
Leff=L-.028;
Cox=Eox/Tox;
Cj=Cox*Weff*Leff*(.6);
Area=(.44+2*.028)*W;
Per=(.44+2*.028)*2*nf;
PerPoly=W;
ID0=(Weff/Leff)*Ivth;
K=(un*Cox*(1e6*1e6)*Weff/Leff)/2;
Rs_g=((1/12)*((Weff/nf)/Leff)*Rresistivity)/nf+Rs_sub;
Rs_channel=Leff/(n*W*un*Cox*(1e6*1e6)*Vt)
Rs_gate=(Rs_g+(1/12)*Rs_channel)



for vthl=1:Vth_length

   vthl % progress counter

   for UI=1:H

      VGS=[1e-99 mean([1e-99 Vinc(UI)]) Vinc(UI)];
      k=3;
      RjDC=zeros(1,k);
      Rj_DC2=zeros(1,k);
      I_DC_half=zeros(1,k);

      for temp=1:30
         for t=1:k
            period=1/f;
            oversample=800;
            time=0:(period/oversample):period;
            Vgs_points=VGS(t)*sin(2*pi*f*time);

            Itot1A=ID0.*exp((Vgs_points-Vth(vthl))./(n.*Vt)).*(1-exp(-Vgs_points./Vt));
            Itot1B=K.*((Vgs_points-
Vth(vthl)).^2).*(1+gamma*Vgs_points)./(1+2*K*Rsx*(Vgs_points-Vth(vthl)));
            Itot1 =
Itot1A.*(Vgs_points<Vth(vthl)).*(Itot1A>0)+Itot1B.*(Vgs_points>Vth(vthl)).*(Itot1B>0);
            PDC=Vgs_points.*Itot1;
            PDC=mean(PDC);
            I_DC_half(t)=PDC/VGS(t);

            RjDC(t)=VGS(t)/I_DC_half(t);
            Rj_DC2(t)=VGS(t)*Rout/(ns*(2*Vinc(UI)-2*VGS(t)));
         end
      %%% new faster solver
         if ((Rj_DC2(2)-RjDC(2))*(Rj_DC2(3)-RjDC(3))>0)
            VGS=[VGS(1) mean([VGS(1) VGS(2)]) VGS(2)];
         else
            VGS=[VGS(2) mean([VGS(2) VGS(3)]) VGS(3)];
         end
```

```
            end

            Itot2=1*(Itot1-circshift(Itot1,[0 (oversample/2)]));
            Vinc_points=Vinc(UI)*sin(2*pi*f*time);
            Pin=Vinc_points.*Itot2;
            PinRMStrueAC=mean(Pin);
            IACtrue=2*PinRMStrueAC/Vinc(UI);
            Rj_AC=Vinc(UI)./IACtrue;
            index=2;
            ratio(vthl,UI)=IACtrue/I_DC_half(t);

            %calculate additional results for this run
            VGS_final(vthl,UI)=VGS(index);
            Vout(vthl,UI)=ns*(2*Vinc(UI)-2*VGS(index));
            j=sqrt(-1);

            %Gate Cap
            Xj1=Rs_gate(1)-j/(2*pi*(Cj)*f);
            ZloadA=(Rj_AC.*Xj1./(Rj_AC+Xj1))

            %Cap from pn junction
            Vd=-(Vinc(UI)*sin(2*pi*f*time)+Vinc(UI)-VGS(index));
            Cj_AVGA=(CjArea*Area+CjPer*Per+CjPerPoly*PerPoly)./((1-Vd/Y).^(M));
            Cj_AVGB=((CjArea*Area+CjPer*Per+CjPerPoly*PerPoly)./((1-
FC).^(M))).*(1+(M./(Y.*(1-FC))).*(Vd-FC*Y));
            Cjd1=Cj_AVGA.*(Vd<=(FC*Y))+Cj_AVGB.*(Vd>(FC*Y));
            figure(6)
            plot(Cjd1) % Instantaneous Capacitance across PN junction
            Xj3=mean(-j./(2*pi*(Cjd1)*f))

            %Leakage Current
            Vtemp=2*Vinc(UI)-2*VGS(index)
            Rleak=((Vtemp)./(ID0*(exp(-Vth./(n*Vt))).*(1-exp(-Vtemp./Vt))))
            Xj2=Rleak;

            % Store Results for each run
            ZloadB=(ZloadA.*Xj3)./(ZloadA+Xj3);
            ZloadB=(ZloadB.*Xj3)./(ZloadB+Xj3);
            Zload(vthl,UI)=((ZloadB.*Xj2)./(ZloadB+Xj2))/ns;

            if (NOPARARISITICS)
               Rj_AC
               Zload(vthl,UI)=Rj_AC/ns;
            end
            PinTOTAL=real((Vinc(UI)^2)./Zload(vthl,UI))/2;
            ratio_true(vthl,UI)=(2*PinTOTAL/Vinc(UI))/I_DC_half(t);
            PinDB(vthl,UI)=10*log10(PinTOTAL/.001);
            Pout(vthl,UI)=Vout(vthl,UI).*Vout(vthl,UI)./Rout;
            Efficiency(vthl,UI)=Pout(vthl,UI)./PinTOTAL;
            RjAC_final(vthl,UI)=Rj_AC;
            RjDC_final(vthl,UI)=RjDC(index);
         end
      end

      %Display results
      VGS_final'
```

```
Vin=(Vout'+ns*2*VGS_final')./(ns*2)
Vout'
2*ns*Vin
abs(Zload')
real(Zload')
PinDB'
Efficiency'
2*ns*RjDC_final

if(length(Vinc) ~= 1 && length(Vth) ~= 1)
   figure(1)
   mesh(PinDB',ones(H,1)*Vth,Efficiency')
   figure(2)
   mesh(PinDB',ones(H,1)*Vth,Vout')

   figure(6)
   mesh(PinDB',ones(H,1)*Vth,RjAC_final'/Rout)
   figure(7)
   mesh(PinDB',ones(H,1)*Vth,RjDC_final'/Rout)
   figure(8)
   mesh(PinDB',ones(H,1)*Vth,RjAC_final'./RjDC_final')
   figure(9)
   mesh(PinDB',ones(H,1)*Vth,ratio_true')
end
```

Chapter 5 Code

LNA_OPT.m: Code Implementing Optimization Methodology of Multi-stage LNA

```
warning off all
clear
i=sqrt(-1);
Vb=.35:.01:.45;
Vbias=Vb-.01; % Model ground bounce
Weakweight=zeros(1,length(Vbias));

% Circuit/Sim Variables
Vds=1;
f=2200e6;
w=2*pi*f;
Rs=50;
Rs_gate=30;
Rout=50/2;
NF_REST=100000;
required_NF=10^(7/10)


%Layout/Process Variables
Vth=.355;
L=.12; % um
W=107.38; % um
n=1.2;
Vt=.026;
Eox=(3.9)*8.85e-14*1e-4;
Tox=3.03e-9*1e6;
Rresistivity=7;
nf=59; %number of fingers
Ivth=300e-9;
gamma=.05;
un=500*.01*.01;
Rsx=20


%Dependant Variables
Weff=W-0;
Leff=L-.028;
Cox=Eox/Tox;
Cg=1*Cox*Weff*Leff*(.66)
ID0=(Weff/L)*Ivth;
K=(un*Cox*(1e6*1e6)*Weff/Leff)/2;


%Modelling inversion point
```

```
ItotWEAK=ID0.*exp((Vbias-Vth)./(n.*Vt)).*(1-exp(-Vds./Vt))
ItotSTRONG=K.*((Vbias-Vth).^2).*(1+gamma*Vbias)./(1+2*K*Rsx*(Vbias-Vth))
for t=1:length(Vbias)
   if Vbias(t)>Vth
      if Vbias(t)<(Vth+2*n*Vt)
         WeakWeight(t)=(1-(Vbias(t)-Vth)/(2*n*Vt)).^1.2;
      else
         WeakWeight(t)=0;
      end
   end

   if Vbias(t)<=Vth
      WeakWeight(t)=1;
   end
end


gms=ItotSTRONG.*(2.0./(Vbias-Vth));
gmw=ItotWEAK./(n*Vt);
gm=gmw.*(WeakWeight).^1.2+gms.*(1-WeakWeight).^1.2

Itot=ItotWEAK.*WeakWeight+ItotSTRONG.*(1-WeakWeight)

% Supply Current
PDC=1.*Itot;
Vbias2=.35:.02:.45;
measSupply=[0.184 0.275 0.397 0.567 0.76 1.23]*.001

figure(8)
plot(Vb,PDC)

hold on
plot(Vbias2,measSupply)
hold off


%Power Gain
Qinalt=(1)./(2*pi*f*Cg*(Rs+Rs_gate))
Vgain_in=Qinalt
Vgain=sqrt(Rs_gate.*(gm.*Rout.*Qinalt).^2./Rout)
Pgain=20*log10(Vgain)
measGain=([6.05 10 12.5 15.5 16.3 17.7]);
figure(9)
plot(Vb,Pgain)
hold on
plot(Vbias2,measGain)
hold off


% Noise figure
ft=gm./(Cg*(2*pi));
Ym=6;
R1=Rs_gate;
gd0=gm*9;
NF=1+R1./Rs+(Ym*(f.^2).*((Rs+R1).^2)./(ft.^2)).*(gd0./Rs)
NFdb=10*log10(NF)
```

```
figure(10)
measNF=[4.30E+00 3.55E+00 2.98095 2.78474 2.684 2.55705];
plot(Vbias2,measNF)
hold on
plot(Vb,NFdb)
hold off


% Methodology utilizing analytical approximations of performance parameters
number_stages_required=zeros(1,length(Vbias));
Gain=10.^(Pgain/10);
Supply=PDC
n_eqn=zeros(1,length(Vbias));
for t=1:length(Vbias)
   NFrec=NF_REST;
   number_stages_required(t)=0;
   if NF(t) < required_NF
      while NFrec > required_NF && number_stages_required(t)<21
         NFrec=NF(t)+(NFrec-1)/Gain(t);
         number_stages_required(t)=number_stages_required(t)+1;
         n=number_stages_required(t);
         NFLNAeqn=((NF(t)-1)/((1/Gain(t))-1))*((1/Gain(t))^n-1)+1;
         eqn_NFrec=NFLNAeqn+(NF_REST-1)/(Gain(t)^n);
      end
      PowerDRAW=number_stages_required.*(Supply);
      n_eqn(t)=log((required_NF-1+(NF(t)-1)/(1/Gain(t)-1))/(NF_REST-1+((NF(t)-
1)/(1/Gain(t)-1))))/log(1/Gain(t));
   end
end

% Methodology utilizing measured performance parameters
n_eqn_real=zeros(1,length(Vbias2));
NF=10.^(measNF/10)
Gain=10.^(measGain/10)
for t=1:length(Vbias2)
   NFrec=NF_REST;
   if (10.^(measNF(t)/10)) < required_NF
      n_eqn_real(t)=log((required_NF-1+(NF(t)-1)/(1/Gain(t)-1))/(NF_REST-1+((NF(t)-
1)/(1/Gain(t)-1))))/log(1/Gain(t));
   end
end

% Optimal Supply Consumption for analytical approx and meas. performance data
P_eqn=n_eqn.*PDC;
P_eqn_meas=n_eqn_real.*measSupply;

% Plot Optimization based on Analytical and Measured LNA performance Data
figure(1)
plot(Vb,P_eqn)
hold on
plot(Vbias2,P_eqn_meas)
hold off
figure(2)
plot(Vb,n_eqn)
hold on
```

```
plot(Vbias2,n_eqn_real)
hold off
```

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