ABSTRACT

Title of Dissertation:	GALLIUM NITRIDE BASED ONBOARD CHARGER FOR ELECTRIC VEHICLES
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Next generation of electric vehicles will be equipped with high power density and high efficiency onboard charging systems with bi-directional power flow. These benefits can be achieved by utilizing the emerging Wide Bandgap devices, planar magnetic solutions, innovative circuit topologies, and advanced control methods to enable MHz switching frequencies without sacrificing efficiency. However, the advantage of higher switching speed is gained at the expense of higher switching losses in both the semiconductors and the magnetics. Conventional circuit topologies, operation modes and control algorithms would no longer be effective in such conditions. Furthermore, the practical implementation of the system has shown more stringent requirements on the controller speed, layout parasitic and the thermal management. In this Ph.D. dissertation work, aforementioned challenges have been addressed, and the proposed innovations have been validated through design and development of a new bi-directional onboard charger using Gallium Nitride devices. The first part of this work

has been focused on a thorough characterization of the front-end AC-DC power factor correction and rectification stage of an onboard charger, utilizing advanced planar magnetics and newly proposed soft-switching control methods. The second part of this work is focused on developing a CLLC DC-DC converter, to interface the AC-DC stage and the high-voltage traction battery. Extended Harmonic Approximation method has been developed and a novel "$f - \varphi$" control scheme is proposed to enhance the efficiency at high switching speed. This system allows insights into the practical implementation and evaluation of utilizing Wide Bandgap semiconductors to achieve high power density and efficiency for the transportation industry.

GALLIUM NITRIDE BASED ONBOARD CHARGER FOR ELECTRIC VEHICLES

by

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List of Abbreviations

ICE	internal combustion engine
EV	electric vehicle
HEV	hybrid electric vehicle
PHEV	plug-in hybrid electric vehicle
BEV	battery electric vehicle
WBG	wide bandgap
SiC	silicon carbide
EVSE	electric vehicle supply equipment
BAT	battery
OBC	onboard charger
GaN	gallium nitride
PFC	power factor correction
PCB	printed circuit board
ZVS	zero-voltage switching
CRM	critical conduction mode
FPGA	field-programmable gate array
PWM	pulse width modulation
EMI	electromagnetic interference
RMS	root mean square
PFM	pulse frequency modulation

FHA	first harmonic approximation
EHA	extended harmonic approximation
FEA	finite element analysis
DM	differential mode
SoC	state of charge
CC	constant current
CV	constant voltage
DAB	dual active bridge
TPS	triple-phase-shift
SR	synchronous rectification
HEMT	high electron mobility transistor

Chapter 1: Introduction

1.1 Background and Incentives

1.1.1 Development of Battery Electric Vehicles

The total number of vehicles running on roads has already crossed 1 billion in 2010 [1] and it is estimated to be doubled by 2040 [2]. Despite their great enhancement to human lives, some major side effects have now become universal concerns. Environmental impacts, such as air pollution and carbon emissions, are the foremost problems. In 2017, over 99% of vehicles owned in the United States are powered by the internal combustion engine (ICE), which burn gasoline or diesel for propulsion [3]. It is reported that vehicles have become the largest greenhouse gas pollution source in both 2016 and 2017, exceeding the emissions from industries and buildings for the first time [4], [5]. On the other hand, transportation alone has consumed 75% of all petroleum products in the United States [6]. It is estimated that petroleum has only 50 years reservation on earth based on its production rate of 2017, and the actual ending date could come earlier considering the 55% higher growing global needs compared to the past 10 years average [7]. Thus, from both environmental and sustainable point of view, vehicles need a substantial change to become both cleaner and more efficient.

To date, the automotive industry is undergoing a significant transformation, which is marked by the development of electric vehicles (EVs). The burning of fossil fuels is reduced or replaced with the help of more electrified propulsion systems. The change was firstly marked by a growing number of Hybrid Electric Vehicles (HEVs) and Plug-In Hybrid Electric Vehicles (PHEVs). They are driven by a combination of a gasoline

engine and an electric machine to get more cost savings in fuels and to reduce emissions at the same time. Battery electric vehicles (BEVs), which are purely driven by the electricity stored inside propulsion batteries, have revealed the greatest advantages in overcoming the aforementioned challenges, but they were traditionally discarded as a useful way of transportation due to limited battery capacity and high cost, low propulsion power and lack of charging facilities. However, efforts have been already devoted so far, with constant developments in the following areas.

(a) Energy storage system

With improved battery chemistry technologies, such as the lithium-ion (Li-Ion) and the nickel metal hydride (NiMH), propulsion batteries are demonstrating much larger energy density, longer lifespan, higher reliability, and can be also charged more quickly. For instance, an industry standard, the 18650B battery cell produced by Panasonic and later applied in Tesla Model S and X, has a proven record high energy density of 676 Wh/L (or 243 Wh/kg) and 1925 mA charging current [8]. A recently announced new battery cell, the 2170 cell utilized in Tesla Model 3, is reported to be more energy dense and has a much higher charging current close to 6000 mA [9], which leads to even more compact size, longer mileage and can be charged faster. As a comparison, in 1997 Toyota Prius (the world first mass production HEV), the energy density of the battery cell was only 30 Wh/kg [10]. On the other hand, the cost of the battery pack has also experienced a dramatic decrease of more than 70% (from $1000/kWh to $200/kWh) over the past six years [11], and it is believed that the price will further drop to $100/kWh in the near future [12]. With the enhanced performance and the reduced cost of the battery, BEVs have shown a larger potential to be driven at

a higher propulsion power and through a longer distance. Currently, an increased number of long-range BEVs have been developed to fulfill the promise of approaching the mileage of typical gasoline engine vehicles, represented by the 2018 Chevy Bolt (60 kWh battery, 238 miles range) [13] and the Tesla Model 3 (50 kWh battery, 220 miles range) [14].

(b) Electric drive system

The electric drive system, which includes the traction motor and its affiliated controller module, is an important constitute for an electric vehicle. It determines the amount of power transmitted to the wheels and thus the torque and the speed of the vehicle. The main developing goals are to achieve greater torque density, wider speed range, lower noise, smaller size, and lower cost [15]. In early HEVs and PHEVs (such as 2010 Nissan Leaf and 2010 Chevy Volt), their traction motors were designed at a peak power around 100 kW with "0 to 60 mph" acceleration times of around 9 seconds [16], [17]. Currently, with larger battery capacity and improved motor technologies, more compact and powerful motors have been designed and applied in the newest BEVs. The 2018 Chevy Bolt is equipped with a 150kW, 96% efficiency permanent magnet motor with less than 7 seconds "0 to 60 mph" acceleration time [18]. The Tesla Model S utilizes dual AC induction motors with 581 kW combined power and 2.8 seconds "0 to 60 mph" acceleration time [19]. As the vehicle market is also being extended towards trucks and SUVs [20], large power density motors would be of even higher demand in the future. As a result, the motor drive module needs to support much larger current to deliver the rising power to the motor. Wide Bandgap (WBG) Devices, especially silicon carbide (SiC) MOSFETs, have been recently utilized in such motor

drive systems [21]. The 650V SiC based power modules manufactured by ST Microelectronics are integrated in Tesla Model 3 inverter, with around 100A current rating per each module [22]. The smaller conduction loss and higher operation temperature of these devices make them suitable for motor drive applications.

(c) Battery charging facilities

One of the continuing requirements with BEVs is to make charging more accessible and much faster. Accompanying the increase of BEV sales, the number of electric vehicle supply equipment (EVSE) has also shown significant growth, which is currently around 3,500,000 worldwide including both public and private ones, compared to only 200,000 in 2012. In the United States, it is estimated that each electric car is now coupled with 1.1 private suppliers [3]. It should be noted that private EVSEs are usually operating at a power level less than 10 kW, which typically charge the vehicle at a rate of 25 miles/hour. They are designed for use at home or work places, where vehicles are parked still for the most of the time [23]. As an alternative charging method, public DC fast charging infrastructure, analogous to gas stations for ICE vehicles, has been deployed with about 100,000 units worldwide. With much higher power compared to private EVSEs, they can charge most BEVs up to 80% capacity in 30 minutes, and it is expected that the charging time can be further reduced to 15 minutes by 2028 [24]. Future deployment of the charging facilities would be even more extensive to accommodate the rapid growth of EVs. For instance, ABB will provide 900 fast charging stations to the United States highways as part of Electrify America project by 2030 [25]. Tesla is deploying their superchargers at the speed of six new locations opening every week [14]. By 2020, China will install 4.3 million private

suppliers and 500,000 public charging units [3]. UK is considering turning 5% of its parking spaces into EV charging bays by 2020, and further increasing to 20% by 2025 [26].

1.1.2 Status of Development and Future Prospects

Based on higher energy density batteries, more powerful electric drive systems, and more accessible and convenient charging facilities, new EV sales worldwide grew rapidly and has firstly exceeded 1 million in 2017, which is 54% increase than 2016, and the total number of global EVs has exceeded 3 million with 65% share of BEVs [3]. While this is clearly a good start, there is still a long way to go since the market share of EVs in the total vehicle stock is pretty low (less than 1% for most countries) [3]. To accomplish the promise of driving EVs into a zero-emission future, both governments and car manufacturers have accelerated the automotive revolution and proposed more ambitious plans. The United States has announced that new EV sales should meet 20% market share by 2020 and 50% by 2025 [3]. As for China and India, the number is 40% by the year of 2030 [27]. In addition, China, with currently 30% share of global vehicle sales, is currently considering legalizing a ban for the production and sales of gasoline vehicles [28]. Norway already has a relatively high EV stock share of 6% and the nation already announced that vehicles producing emissions will be completely banned by 2025 [29], which was later joined by Germany, France and Britain that announced similar bans that will put the end for gasoline cars by 2040 [30]. As a response, the world top car manufactures including Volkswagen, Toyota, GM, and Ford have promised to stop manufacturing ICE vehicles by 2030 [29]. On the other hand, Volkswagen will plan to build 2 to 3 million BEVs a year by 2025 [31], and GM

will offer at least 20 new BEVs also by 2023 [32]. Volvo and Jaguar Land Rover also announced that all of their new models from 2020 will be either hybrid or electric [28]. Through joint efforts, it is estimated that global stock of EVs will reach 13 million by 2020, when the sales per year would be 4 million with 24% annual growth rate. By 2030, the global stock would become 228 million, which would reduce 121 mega tons CO_2 emissions (63% less) compared to same number of ICE vehicles [3]. The EV mileage share is also expected to reach 20% by 2030 [33].

1.1.3 Challenges of Battery Electric Vehicles

The consistently growing investment and production will combine to spur the automotive industry into a period of an intense development, which will put forward the requirement for effective solutions to the most prominent challenges of BEVs these days, covering multiple fields of study including engineering, city planning, politics and economics. Due to the scope of this research, only challenges with a special focus on battery charging techniques are analyzed in this section.

Electric vehicle battery charging is normally divided into three categories based on the power level: level 1, 2, and 3 (shown in Fig. 1-1). In the figure, HV BAT represents the high voltage battery, which is also the propulsion battery of the vehicle to drive the inverter and the motor. LV BAT stands for the low voltage battery that supplies electric power other than the propulsion, such as air conditioner, vehicle controller, head lights, etc. APM stands for the auxiliary power module which charges LV BAT from HV BAT. OBC represents the onboard charger, which transmits power from AC grid to HV BAT especially for Level 1 and 2 charging. The charging power is usually 1 to 3 kW in level 1, 3 to 20 kW in level 2 and over 20 kW in level 3 (also known as DC fast

charging), while the charging time is reduced at higher power levels. Although faster charging rate of 90 miles / 30 minutes is more preferred for customers with urgent needs than 25 miles/hour, DC fast charging pumps enormous amount of currents (hundreds of amperes) into the battery in a short time, which could affect the battery health and lifespan. Also, the high charging power is usually imported through a three-phase utility grid interface, which is usually not accessible at residential houses especially in the United States. Thus, a more practical pattern of BEV battery charging would be using the onboard charger to charge the vehicle at level 2 at homes or workplaces for most of the time, while using DC fast charging at commercial charging stations for quick charging needs. Therefore, improving the performances of level 2 OBCs is of high importance, which is the main target of this research.

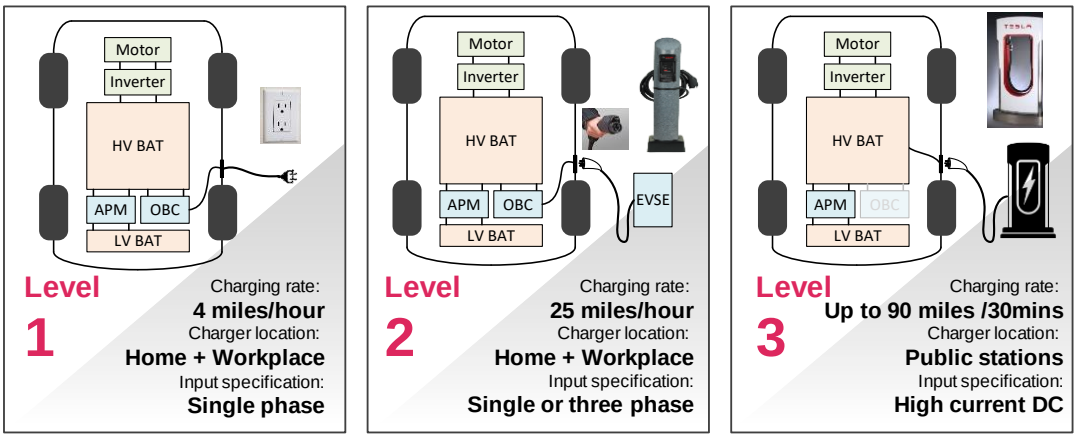

Fig. 1-1. Different charging levels for BEVs.

The most prominent challenges for onboard battery chargers are size, weight, and efficiency. For long-range BEVs, a compact and lighter onboard charger would provide additional space for a larger battery pack. Several state-of-the-art onboard charger products from the market are listed in Table 1-1. Most of them have shown power densities around 0.6 kW/L (or 0.5 W/kg). However, the US Department of Energy

(DOE) has ambitious power density targets of 3.5 kW/L (or 3 kW/kg) by 2020 and 4.6 kW/L (or 4 kW/kg) by 2025 [34] for onboard chargers. Passive components, such as power inductors, transformers and capacitors, consume the largest portion of volume and weight in conventional onboard chargers. Their sizes would be even larger at higher power levels (between 6.6 to 22 kW) due to the higher voltage or current ratings. On the other hand, power losses, which come from the non-ideal properties of electric components, would also increase at higher power levels. Efficiency is a critical metric to evaluate the performance of the charger, since higher power losses lead to more generation of heat and a need for effective cooling, which sacrifices the power density.

Table 1-1. Specifications of selected commercial on-board chargers for BEVs.

Manufacturer	**Input (V_{AC})**	**Output (V_{DC})**	**Power Rating (kW)**	**Efficiency**	**Cooling System**	**Size (L)**	**Weight (kg)**
Brusa	100-264	200-520	7.36 (two in parallel)	93%	Air /Liquid	11.3	12.4
Delphi	85-265	170-440	6.6 (two in parallel)	94%	Liquid	11.2	10
Delta-Q	85-265	200-450	6.6 (two in parallel)	94%	Liquid	10.9	12.4
Current ways	110-240	112-450	6.6	96%	Liquid	10.9	11
Bel	120/240	250-435	15	90%	Liquid	33.3	36
Bel	460-575 (three phase)	500-800	25	93%	Liquid	15	19.4
Brusa	360-440 (three phase)	200-450	20.75	94%	Liquid	11	12

1.2 State-of-the-Art

To increase the power density as well as the efficiency of the onboard chargers, substantial improvement has been achieved over the past few years. They are

represented by the emergence of WBG devices, the application of ultra-high switching speed, and the shift towards planar magnetics.

1.2.1 Wide Bandgap Devices

WBG materials, including SiC and Gallium Nitride (GaN), possess a larger critical electric field (>2MV/cm), which could be utilized to achieve high breakdown voltage while reducing the on-resistance on a large scale compared to silicon devices. The reduced capacitance also allows for much higher switching frequency, especially for GaN semiconductors [35]. Thus, WBG devices could be promising to both reduce the size and increase the efficiency of the charger.

Currently, there are already a few successful demonstrations of using WBG power electronics in EV onboard chargers. In 2014, Arkansas Power Electronics International (APEI), Toyota, and other partners designed a highly compact onboard charger for Prius Plug-in Hybrid model using SiC power modules, which achieved more than twice power level than the old unit with less than quarter of the volume [36]. After a few years, GaN devices have begun showing better performance in terms of the switching frequency than SiC devices. A joint team led by the Center for Power Electronics Systems (CPES) at Virginia Polytechnic Institute and State University and the Delta Products Corporation has developed a 6.6 kW bi-directional onboard charger based on both SiC and GaN devices, which achieved a power density of 2.3 kW/ L and over 96% efficiency [37]. In 2018, a team led by the University of Texas at Austin has firstly reported an all-GaN power rectifier unit working at 3.2 kW with the power density of 4.5 kW/L (without housing/fan) [38]. The PFC unit operated at MHz switching frequency can achieve as high as 8 kW/L power density [39]. At the University of

Maryland, College Park, our team has successfully developed the first 3.3kW GaN-based bi-directional DC-DC converter working at MHz frequency range with a 9.2 kW/L power density (without housing/fan) [40].

1.2.2 High Frequency Power Electronics

Conventional power electronics converters are usually operated at a switching frequency between 20 kHz to 200 kHz. With higher switching speed (especially into MHz region), the size of the passive components would be minimized, and the power density of the converter could be largely increased. However, challenges in terms of higher switching losses in switches, limited controller and sensor speed, Printed Circuit Board (PCB) circuit parasitic components, and the magnetic design are more prominent than before. One of the very first demonstration of MHz switching on GaN devices was implemented on a 300W boost converter with 97.8% efficiency [41]. It was later implemented on a Totem-pole PFC rectifier at 1 kW based on digital control [42]. Zero-voltage switching (ZVS) can be guaranteed by operating the PFC rectifier in Critical Conduction Mode (CRM) [43]–[47]. In order to improve the controller response time, a Field-Programmable Gate Array (FPGA) controller was firstly used in a 1MHz, 10 kW three-phase VIENNA rectifier with a 25 MHz data sampling rate and an increased PWM resolution of 4 ns [48]. Furthermore, adaptive continuous current source drivers are designed and verified on a 1 MHz, 300 W boost PFC circuit to further reduce the switching losses by sensing the drain-to-source current and adaptively tuning the driving currents [49]. In addition, an integrated current sensor with 10MHz bandwidth was developed recently for ultra-fast current sensing in high frequency power electronic converters [50]. Magnetic materials that can work at MHz frequency range

have also been developed, represented by the L material (500kHz to 1MHz) from Magnetics [51] and 3F36 material (500kHz to 1MHz) from Ferroxcube [52]. Thus, the trend for high frequency power electronics has been well recognized in both academia and industry, and advanced semiconductors, low-latency affiliated hardware, and enhanced circuit control algorithms should be developed at the same time to support such variation.

1.2.3 Planar Magnetics

Planar magnetics is a technology to build inductors or transformers as an integral part of the PCB board. It utilizes the PCB traces as the windings, which surround the planer magnetic core. Different turns are sandwiched in different layers with proper insulation. Compared with the conventional wire-wound magnetic components, the inductance values of planar magnetic components are easier to control; they are simpler for mass-market manufacturing; and their utilization significantly reduces height of the power circuit (due to the flat geometry) [53]. Furthermore, heat dissipation would be much easier with a larger surface, which can be attached to a larger heatsink (or cold plate). Plus, the cross-section area is increased compared to the conventional hand-wound magnetics, which could lead to a reduced number of turns at the same flux density requirement. Furthermore, the large width-to-height ratio of the PCB traces could help to alleviate the skin effect and the proximity effect, which are the two major factors that contribute to the copper loss. The ratio of the cross-section area to the core volume of a planer magnetic core is also larger than the conventional competitive, which could help reduce the core loss. Hence, planar magnetics has been widely applied in different power electronic applications [36], [37] and [40].

1.3 Limitations of Current High Frequency Onboard Chargers

It has been shown that by operating WBG devices at high frequency range and combining the planer magnetics into the onboard charger, the power density and the efficiency could be largely increased. However, there are various significant challenges that need to be addressed to show full advantages of such technologies. For example, the SiC based charger shown in [36] doesn't support bi-directional power flow. In order to reduce the size, the DC-link capacitor is selected at a very low value (300 μF) which brings a large voltage ripple on the input side of the DC-DC stage. Also, soft-switching is not guaranteed through the entire operation range which could affect the light load efficiency. As shown in another design [37], a variable DC-link voltage control method was introduced and 1.2kV SiC MOSFETs are applied in the PFC stage to accommodate the wide drain-to-source voltage range. The drawback of using SiC MOSFETs, however, is that the switching frequency cannot reach MHz (In this case it is 300 kHz). Although the DC-DC stage is implemented by all GaN switches, the switching frequency is limited to 500 kHz. The high switching frequency feature of the WBG devices were not exploited thoroughly and thus the power density of the entire system could be further optimized. In [40], a MHz DC-DC converter was developed at 3.3 kW level with a planar transformer. However, the controlling of the system is open-loop and the converter efficiency at lighter load (lower battery voltage) has not been addressed thoroughly. Based on the limitations existed in previous designs, the objectives of this research are discussed as follows.

1.4 Synopsis of the dissertation

In this dissertation, a single phase two-stage onboard charger based on all-GaN devices operating at MHz frequency is proposed. It is consisted by a power factor correction (PFC) rectifier and a DC-DC converter to interface the vehicle battery. Research addresses novel circuit components and structure, advanced control methods, and comprehensive system level optimization. The proposed target was on the investigation, modelling, optimization, simulation and verification of the first all-GaN onboard charger operated at MHz frequency with a high power density and efficiency. Novel operation and controlling methods were analyzed in the high switching speed scenario. Planar coupled inductor and transformer were developed for size reduction and efficiency improvement. Systematic optimization was conducted to enhance the overall performance. The analysis was finally verified on a thermally stable system developed on a well-designed PCB board with extremely low parasitic coefficients. The rest of this dissertation is organized as follows.

In Chapter 2, an interleaved Totem-Pole PFC rectifier working at CRM is introduced. The modelling of a coupled inductor is given, and the effect of the coupling factor on the switching frequency range, current ripples, current Root Mean Square (RMS) values and soft-switching region is analyzed thoroughly. Limitations of conventional open-loop interleaved phase control is shown, and a closed-loop phase control is demonstrated.

In Chapter 3, a CLLC-type resonant DC-DC converter controlled with Pulse Frequency Modulation (PFM) is introduced. Operation principles and design considerations based on a battery charging profile are presented. Limitations of

conventional First Harmonic Approximation (FHA) method are explained, and a more accurate Extended Harmonic Approximation (EHA) modelling method based on numerical approach is proposed. Based on the new model, reactive power flow and major voltage/current stress of the converter can be projected more accurately, which could be further utilized to generate optimized design parameters.

In Chapter 4, disadvantages of PFM mode at higher switching frequency are explained and a new "$f-\varphi$" modulation scheme is proposed for the CLLC converter. Circuit modelling and power loss analysis based on EHA are developed, and a systematic approach to design and optimize the converter coefficients is presented. Comparison of the new modulation scheme and the conventional PFM control is shown. Based on the proposed control method and optimization results, a laboratory prototype is designed and tested at 3.3 kW peak power to verify the analysis. Three different operation points corresponding to the light-load (1.65kW), medium-load (2.48kW), and heavy-load (3.3kW) conditions are independently tested and high conversion efficiencies are demonstrated through the entire charging process.

In Chapter 5, theoretical analysis and Finite Element Analysis (FEA) simulation are presented for a novel unsymmetrical planar magnetic winding structure. In this approach, primary and secondary windings are interleaved to reduce the AC resistance. Unsymmetrical structure offers more flexibility to control the leakage inductance. Considerations to reduce the intra-winding capacitance are also explained, which is critical in high frequency applications.

Finally, conclusions of the dissertation and research contributions are summarized in Chapter 6. Future work to further develop the proposed techniques are also included.

For the ease of the readers, the major contributions of this research are listed here:

- Modelling, characterization and control of a Totem-Pole interleaved Power Factor Correction (PFC) rectifier
    1. Modelling and characterization of the coupled effect
    2. Extension of soft-switching region
    3. Closed-loop control of 180º phase shift and hardware verification
    4. Design of interleaved coupled inductor
- Optimization and development of a CLLC resonant DC-DC converter
    1. Modelling based on Extended Harmonic Approximation
    2. Novel “frequency-phase” control method
    3. Systematic optimization
    4. Design, test and verification on a 3.3kW prototype

Chapter 2: Interleaved Critical Conduction Mode Totem-Pole PFC Rectifier

2.1 Introduction

In this chapter, theoretical analysis and modeling of the PFC rectifier working in CRM is presented. The circuit topology and its operation principles are introduced. Provided that one coupled inductor is adopted to form two inductance values, its equivalent model is derived and the effects on the switching currents are exemplified. A special emphasis is placed on the coupling factor of the inductor and its influence on multiple variables, such as the input current ripple, current stress on the semiconductors, and the switching frequency variation. Furthermore, the advantage of using coupled inductor to extend the ZVS properties of the switches to full voltage range is shown for the first time and compared to conventional designs. In contrast to existing prototypes, a closed-loop phase shift control will be implemented in this work, considering the limitations revealed by the open-loop control systems. As will be introduced next, the switching frequency will be varied following a pattern determined by the input voltage. Consequently, the Differential Mode (DM) noise spectrum would be more sophisticated than the fixed frequency design, and considerations on the design of the Electromagnetic Interference (EMI) filter are presented. Noticing that the size reduction of the DC-link would not be benefited from high frequency switching, initial analysis on the active buffer techniques is introduced in this chapter as well.

To begin with, the electrical specifications of the PFC stage are first shown in Table 2-1. The input AC voltage could vary from 85Vrms to 265Vrms, which is universal in

different countries, but the nominal point is taken at 240Vrms input voltage when the input power can reach the maximum value. The power level would be reduced at lower input voltages to limit the current flowing through the components. The DC-link voltage, which is also the output voltage of the PFC stage, is taking the value of 400V with 5% ripple. It is a common voltage level well adopted by most GaN devices which are designed at the maximum drain-to-source voltage of 650V.

Table 2-1. Electrical specifications of the PFC stage.

Parameters	**Values**
Input AC voltage	85Vrms to 265Vrms
Nominal input voltage	240Vrms
Input line frequency	50 to 60 Hz
Peak power	6.6 kW (when input voltage is 240Vrms)
DC-link voltage	~ 400V

2.2 Circuit topology and operation principles

In this project, the totem-pole PFC with interleaved input configuration and coupled inductor is chosen as the circuit topology, which is shown in Fig. 2-2(a). The interleaved structure is adopted to minimize the current stress on the devices and to reduce the input current ripples. Other topologies applied in the EV charging applications are the boost PFC and the bridgeless PFC [54], which are shown in their interleaved versions in Fig. 2-2(b) and (c) respectively. Notice that totem-pole PFC has the simplest structure and less count of the components, but it was traditionally discarded as a promising circuit in the application due to the large reverse-recovery losses (especially when the circuit works in CCM) and conduction losses of the silicon MOSFETs [55]. In the case of utilizing GaN devices as power switches, the reverse

recovery current is cut down to zero due to its unique structure and its low on-resistance could largely reduce the conduction losses as well, making the totem-pole topology very attracting in the high frequency application.

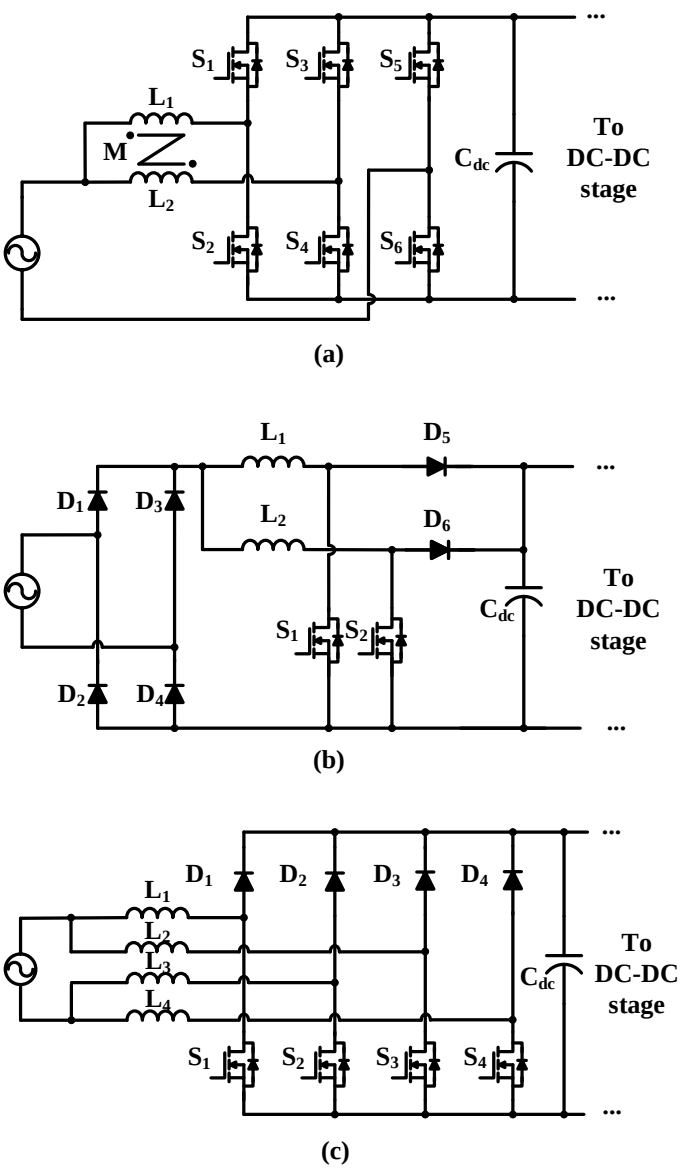

Fig. 2-1. Different interleaved topologies of PFC rectifier applied in EV charging applications. (a) Totem-pole PFC with coupled inductor. (b) Interleaved boost rectifier. (c) Bridgeless interleaved boost topology.

The detailed PFC stage structure is shown in Fig. 2-2. In switching circuits, noises would be generated by the high frequency ripples and the parasitic capacitors between different components. An EMI filter is usually placed at the input side to prevent affecting other surroundings electronics. Following the EMI stage, the coupled inductor is represented by its "self-inductance" (L_1 and L_2) and "mutual-inductance" (M). Detailed modeling and operation of the coupled inductor would be discussed in section 2.2, and the EMI filter design would be presented in section 2.5. S_1 to S_4, usually referred as "fast switches", are operating at high switching frequency. Specifically, the switches on the same leg (S_1, S_2 from primary leg or S_3, S_4 from secondary leg) are driven complementarily with a deadtime, and the gate driving signals of S_2 and S_4 (or S_1 and S_3) have a 180° phase difference. S_5 and S_6 (both are implemented by a pair of two parallel switches to split the current, represented by a subscript of a and b), usually referred as "slow switches", are also driven complementarily but are controlled by a low frequency signal. Their switching status is inverted only when the input voltage changes its polarity, meaning that S_6 will be turned on if the input voltage is at its positive half line cycle, and S_5 will be turned on if the input voltage is at the other negative half line cycle. In conclusion, the driving signals of different switches are shown explicitly in Fig. 2-3. In addition, a relatively large capacitor C_{dc} is usually placed at the output of the PFC stage (referred as the "DC-link) to absorb the AC power caused by the single-phase input and maintain a stable DC-link voltage.

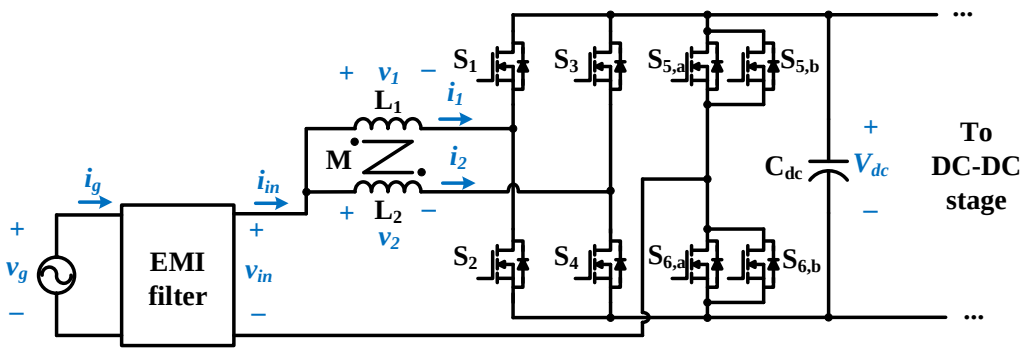

Fig. 2-2. Circuit topology of the totem pole PFC with coupled inductor.

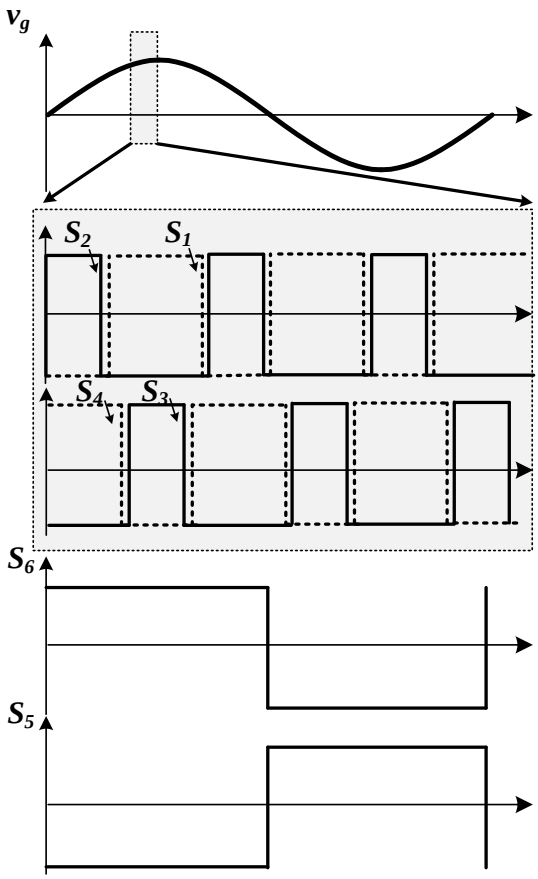

Fig. 2-3. Driving signals of different switches during the input line cycle.

2.3 Coupled Inductor Modelling and Circuit Operation Principles

In a coupled inductor, the voltage across one winding is not only related to the current through itself, but also affected by the current through the other winding. The coupling effect can be analytically expressed by Eq. 2-1 and Eq. 2-2:

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \quad \text{Eq. 2-1}$$

$$v_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \quad \text{Eq. 2-2}$$

where v_x, i_x are the respective voltages and currents on the primary ($x = 1$) and the secondary ($x = 2$) windings. Based on the direction each winding is wounded on the core, the coupling effect can be divided into two categories: direct coupling ($M > 0$) and inverse coupling ($M < 0$), which are depicted respectively in Fig. 2-4.

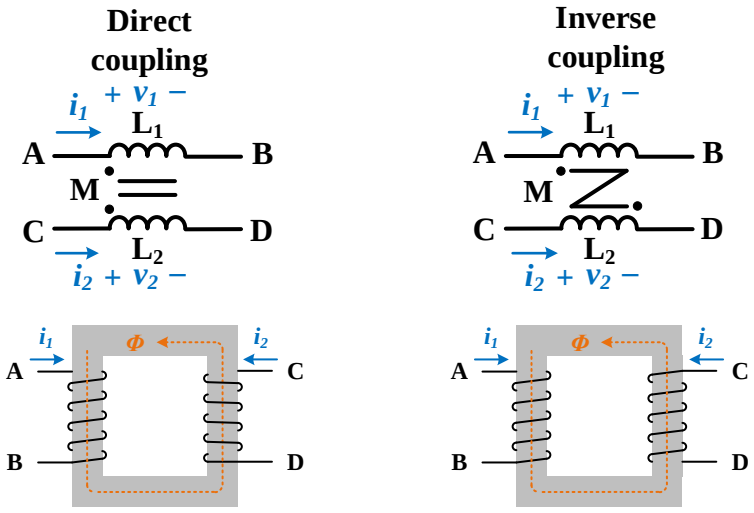

Fig. 2-4. Theoretical model and physical implementation of different coupled inductors.

For the ease of the analysis, symmetric structure is assumed in both windings that L_1 and L_2 would have the same value of L:

$$L_1 = L_2 = L \quad \text{Eq. 2-3}$$

Next the coupling factor (α) is defined to quantify the relationship between the self and mutual inductance:

$$\alpha = \frac{M}{L} \qquad \text{Eq. 2-4}$$

where larger value of α represents a stronger coupling between the windings. In order to cancel the variable of i_2 from the equation, an operation of (Eq. 2-1)− (Eq. 2-2)× α is conducted and the simplified expression is shown as:

$$L\frac{di_1}{dt} = \frac{v_1 - \alpha v_2}{1 - \alpha^2} \qquad \text{Eq. 2-5}$$

v_1 and v_2 are the voltages across each winding, which are directly determined by the states of different switches. Here, the equivalent circuits at different switching states are depicted in Fig. 2-5. To simplify the analysis, only the positive line cycle is considered here, when S_6 is kept on and S_5 is kept off.

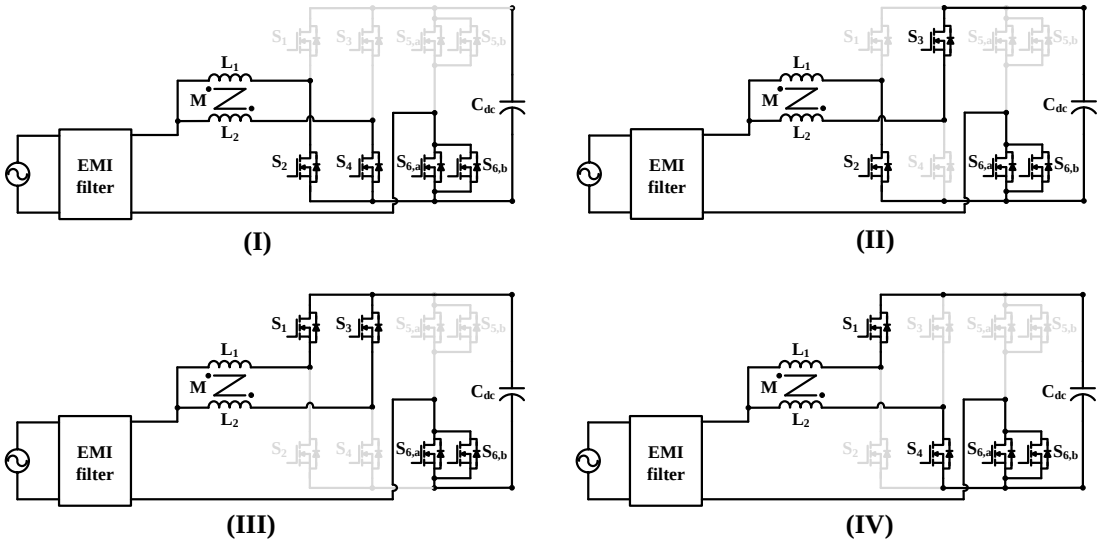

Fig. 2-5. Operation principles of the PFC stage.

State (I): S_2 is ON and S_4 is ON. At this phase, $v_1 = v_{in}$ and $v_2 = v_{in}$.

State (II): S_2 is ON and S_4 is OFF. At this phase, $v_1 = v_{in}$ and $v_2 = v_{in} - v_{DC}$.

State (III): S_2 is OFF and S_4 is ON. At this phase, $v_1 = v_{in} - v_{DC}$ and $v_2 = v_{in} - v_{DC}$.

State (IV): S_2 is OFF and S_4 is OFF. At this phase, $v_1 = v_{in} - v_{DC}$ and $v_2 = v_{in}$.

v_{in} denotes input voltage and v_{DC} represents the DC-link voltage during the positive half line cycle. As can be seen, the total number of different combinations of $(v_1 - \alpha v_2)$ from is four. Next, the ratio between v_1 and v_2 is defined as A_x:

$$\frac{v_1}{v_2} = A_x \qquad \text{Eq. 2-6}$$

where x denotes different switching states ranging from I to IV. By applying A_x into Eq. 2-5, a more simplified expression can be derived:

$$v_1 = \left(\frac{1 - \alpha^2}{1 - \frac{\alpha}{A_x}} \cdot L \right) \frac{di_1}{dt} = L_{eqx} \frac{di_1}{dt} \qquad \text{Eq. 2-7}$$

Here, an equivalent inductance of the first winding at the switching stage x is defined as L_{eqx}, which is sensitive to the voltage across the winding. The purpose of this process is to "cancel" the coupling effect in the expression and to equate the coupled inductor to an independent inductor. Assume the duty ratio of the bottom switch (S_2 and S_4) is defined as d, the steady state voltage relationship can be expressed as:

$$v_{in} = (1 - d) v_{DC} \qquad \text{Eq. 2-8}$$

Based on Eq. 2-7 and Eq. 2-8, the values of v_1, v_2, A_x and L_{eqx} in different switching states are listed in Table 2-2 and Table 2-3 for $v_{in} < 0.5 v_{DC}$ and $v_{in} > 0.5 v_{DC}$, respectively.

Table 2-2. Values of voltages on each winding and their ratio. ($v_{in} < 0.5v_{DC}$)

	State I	**State II**	**State III**	**State IV**
v_1	v_{in}	v_{in}	v_{in}	$v_{in} - v_{DC}$
v_2	v_{in}	$v_{in} - v_{DC}$	v_{in}	v_{in}
A_x	1	$\frac{v_{in}}{v_{in}-v_{DC}} = \frac{1-d}{-d}$	1	$\frac{v_{in}-v_{DC}}{v_{in}} = \frac{-d}{1-d}$
L_{eqx}	$(1+\alpha)L$	$\frac{(1-\alpha^2)(1-d)}{1-d+d\alpha}L$	$(1+\alpha)L$	$\frac{(1-\alpha^2)d}{d+\alpha(1-d)}L$

Table 2-3. Values of voltages on each winding and their ratio. ($v_{in} > 0.5v_{DC}$)

	State I	**State II**	**State III**	**State IV**
v_1	v_{in}	$v_{in} - v_{DC}$	$v_{in} - v_{DC}$	$v_{in} - v_{DC}$
v_2	$v_{in} - v_{DC}$	$v_{in} - v_{DC}$	v_{in}	$v_{in} - v_{DC}$
A_x	$\frac{v_{in}}{v_{in}-v_{DC}} = \frac{1-d}{-d}$	1	$\frac{v_{in}-v_{DC}}{v_{in}} = \frac{-d}{1-d}$	1
L_{eqx}	$\frac{(1-\alpha^2)(1-d)}{1-d+d\alpha}L$	$(1+\alpha)L$	$\frac{(1-\alpha^2)d}{d+\alpha(1-d)}L$	$(1+\alpha)L$

In both cases, there are only three different forms of expression for the equivalent inductance L_{eqx}. For the ease of reference, the following inductance variables are defined:

$$L_a = \frac{(1-\alpha^2)(1-d)}{1-d+d\alpha}L \quad \text{Eq. 2-9}$$

$$L_b = (1+\alpha)L \quad \text{Eq. 2-10}$$

$$L_c = \frac{(1-\alpha^2)d}{d+\alpha(1-d)}L \quad \text{Eq. 2-11}$$

It is worth mentioning that despite the limited number of expressions, the actual values of the equivalent inductance are still varying with the duty ratio, which is determined by the input and output voltage relationship. The inductance values can be used to calculate the current changing rates in different switching states, and the

theoretical current waveforms of each winding (i_1 and i_2) as well as the combined input (i_{in}) can be then depicted, which is shown in Fig. 2-6. As can be noticed, although the current through each winding is divided into four segments, the total input current has shown two repetitive patterns in one switching cycle due to the 180° phase shift. Also, the current ripple of the input current is smaller than the current through individual windings, which is one of the advantages of the interleaved structure and will be discussed in the next section.

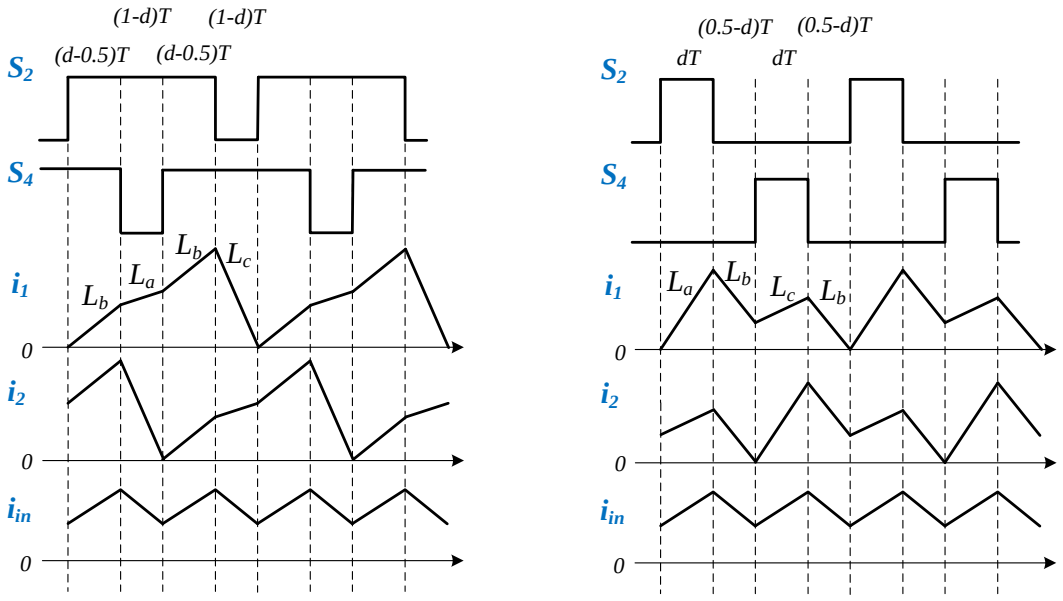

Fig. 2-6. Theoretical currents through each winding of the coupled inductor and the total input current with relative switching signals. (Left: $v_{in} < 0.5v_{DC}$. Right: $v_{in} > 0.5v_{DC}$)

2.4 Critical Conduction Mode and Soft Switching

2.4.1 Switching frequency variation

In CRM, the current through each winding would reach zero before the next switching cycle starts. Unlike the Continuous Conduction Mode (CCM), the switching frequency in CRM is always changing, which can be determined by calculating the

turning-on time of the bottom switch (S_2 or S_4) when $d < 0.5$ or the turning-off time when $d > 0.5$. To maintain the unity power factor requirement, the average current in each switching period of each interleaved leg should be half of the input current ($i_g/2$) seen from the grid side, expressed as:

$$\frac{1}{T(t)} \cdot \int_{t}^{t+T(t)} i_1(\tau) d\tau = \frac{i_g}{2} \qquad \text{Eq. 2-12}$$

where $T(t)$ denotes the period of the selected switching cycle starting from time t. If the input power (P_{in}) is known, the right side of Eq. 2-12 can be written as:

$$\frac{i_g}{2} = \frac{v_g I_r}{2V_r} = \frac{V_p P_{in}}{2V_r^2} \sin(2\pi f_{line} t) = \frac{P_{in}}{\sqrt{2}V_r} \sin(2\pi f_{line} t) \qquad \text{Eq. 2-13}$$

where V_p and V_r are the input voltage peak and RMS value, respectively, and f_{line} represents the line voltage frequency. The average current is calculated by finding the enclosed area by the current waveform. Since the equivalent inductance during two of the switching states has the same value, the ramp rate of the current would also be identical. Therefore, the enclosed area would be equivalent to a triangle area as we connect the peak current point to zero at the end of the switching period, as shown in Fig. 2-7.

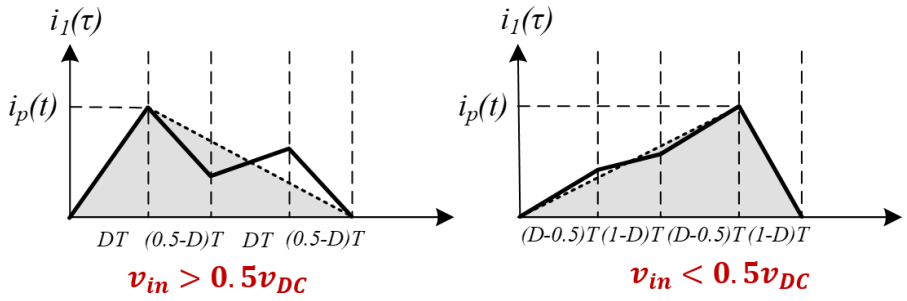

Fig. 2-7. Calculation of the average current in one switching cycle.

Since the average value of the triangle is half of the peak value, Eq. 2-12 can be written as

$$i_p(t) = i_g = \frac{\sqrt{2}P_{in}}{V_r}\sin(2\pi f_{line}t) \quad \text{Eq. 2-14}$$

From t to $t + dT(t)$, the current of the first winding is linearly increasing, represented by:

$$\frac{L_a i_p(t)}{T_{on}} = v_i = V_p\sin(2\pi f_{line}t) \quad \text{Eq. 2-15}$$

The turning-on time of the bottom switch can be then found as:

$$T_{on} = \frac{L_a P_{in}}{V_r^2}, d < 0.5 \quad \text{Eq. 2-16}$$

Similarly, the turning-off time of the bottom switch when $d > 0.5$ can be calculated as:

$$T_{off} = \frac{(1-d)L_c P_{in}}{dV_r^2}, d > 0.5 \quad \text{Eq. 2-17}$$

Considering the turning-on time over the complete cycle period is exactly the duty ratio if $d < 0.5$ and the turning-off time over the cycle period is one minus the duty ratio if $d > 0.5$, the expression of the switching cycle can be easily calculated by:

$$T_{on} = \frac{d}{f(t)}, d < 0.5 \quad \text{Eq. 2-18}$$

$$T_{off} = \frac{1-d}{f(t)}, d > 0.5 \quad \text{Eq. 2-19}$$

Thus, the final expression for the switching frequency at time t is shown as follows:

$$f(t) = \begin{cases} \dfrac{V_r^2\left(1 - \dfrac{V_p sin(2\pi f_{line} t)}{v_{DC}}\right)}{L_a P_{in}}, d < 0.5 \\ \dfrac{V_r^2\left(1 - \dfrac{V_p sin(2\pi f_{line} t)}{v_{DC}}\right)}{L_c P_{in}}, d > 0.5 \end{cases} \quad \text{Eq. 2-20}$$

As one can notice, the switching frequency is not affected by the L_b value. Suppose $L = 10\mu H$, $V_r = 240V$, $f_{line} = 60Hz$, $v_{DC} = 400V$ and $P_{in} = 6.6kW$. Combining Eq. 2-9, Eq. 2-11 and Eq. 2-20, the variation of the switching frequency through the entire half line cycle can be depicted, as shown in Fig. 2-8. It is shown that with stronger coupling, the frequency range would be expanded. Such effect is even more evident for direct coupling case than the inverse coupling case. Operation in a frequency that is much higher than 1MHz is not preferred, due to the limitation of the processing time of the controller and the delayed response of sensors and gate drivers.

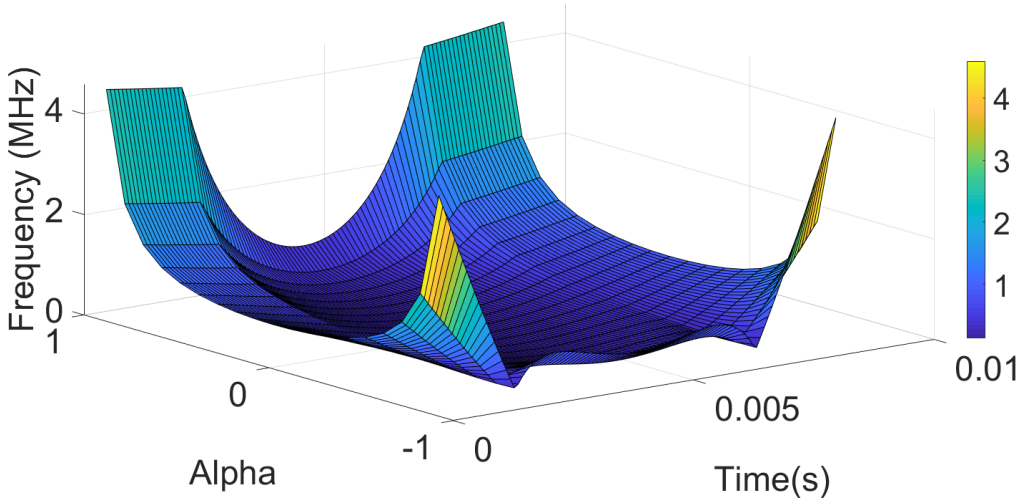

Fig. 2-8. Switching frequency variation in the positive half line cycle with related with different coupling factor values ($-1 < \alpha < 1$).

2.4.2 Input current ripple and inductor current stress

The analysis of the input current ripple would be used for the EMI filter design, and the calculation of the inductor current stress is related with the conduction losses of both the inductor and the switches. The peak (I_{peak}) and bottom (I_{bottom}) point of the input side current can be found from Fig. 2-6. For $d > 0.5$, they can be calculated by:

$$I_{bottom} = \frac{v_{in}(d-0.5)T(t)}{L_b} + \frac{v_{in}(1-d)T(t)}{L_a} \quad \text{Eq. 2-21}$$

$$I_{peak} = I_{bottom} + \frac{2v_{in}(d-0.5)T(t)}{L_b} \quad \text{Eq. 2-22}$$

For $d < 0.5$, they can be calculated by:

$$I_{bottom} = \frac{v_{in}dT(t)}{L_a} + \frac{(v_{in}-v_{DC})(0.5-d)T(t)}{L_b} \quad \text{Eq. 2-23}$$

$$I_{peak} = I_{bottom} - \frac{2(v_{in}-v_{DC})(0.5-d)T(t)}{L_b} \quad \text{Eq. 2-24}$$

By importing the expression into MATLAB, the peak and bottom current can be depicted in Fig. 2-9 and Fig. 2-10. One conclusion can be drawn from the results that negative coupling factor leads to higher current ripple and positive coupling factor leads to lower current ripple.

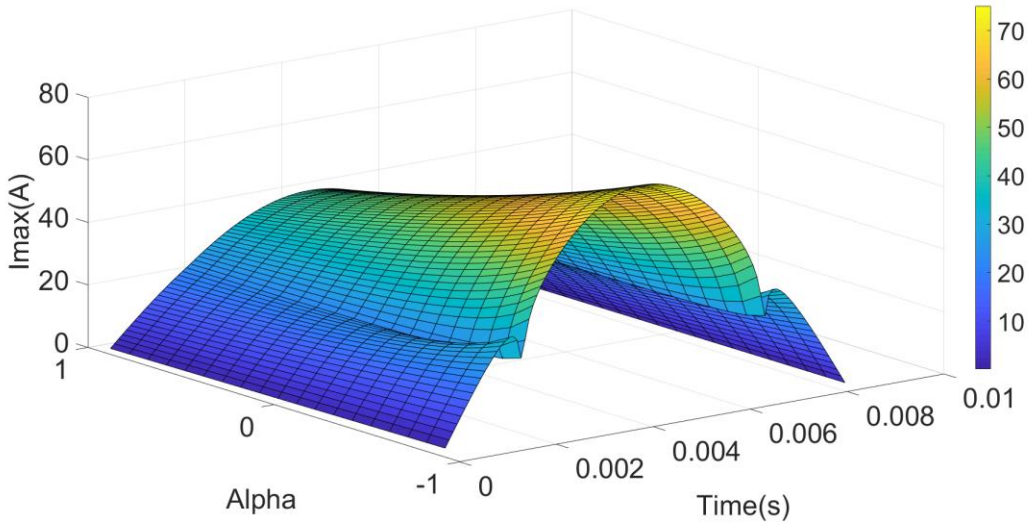

Fig. 2-9. Current envelope of input grid current peak points.

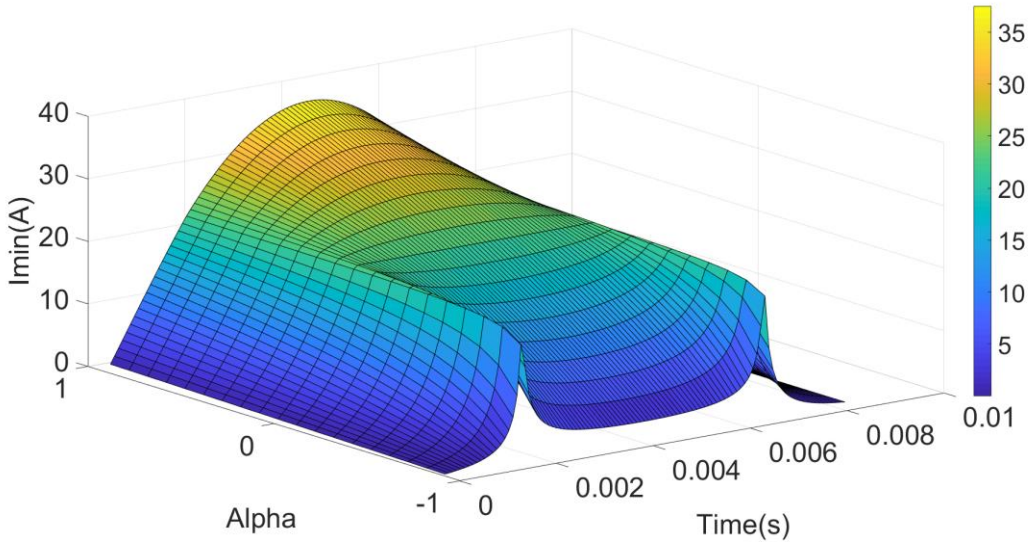

Fig. 2-10. Current envelope of input grid current bottom points.

Due to the varying switching frequency and different current ramp rate at different input line voltage, the calculation of the single interleaved leg current RMS value is more complicated than the input current ripple. The basic idea is to calculate the integration of the current square during each switching phase and sum up for four phases. Then the same process is conducted for the remaining switching cycles and

integrate for the whole line cycle. For each switching phase, the current through the inductor can be generalized as a linear segment, as shown in Fig. 2-11.

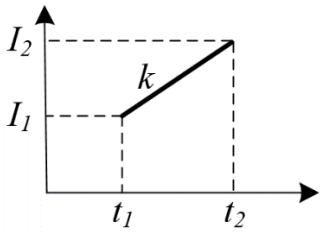

Fig. 2-11. Generalized current waveform during one switching phase.

The RMS current from t_1 to t_2 can be found by definition and later simplified as:

$$I_{rms,t_1\ to\ t_2} = \sqrt{\frac{1}{t_2 - t_1} \cdot \int_{t_1}^{t_2} \left(I_1 + \frac{I_2 - I_1}{t_2 - t_1} t\right)^2 dt} = \sqrt{\frac{I_1^2 + I_2^2 + I_1 I_2}{3}} \quad \text{Eq. 2-25}$$

Since in each switching frequency, the current at different phase transition can be found by the equivalent inductance and the duty ratio, the RMS current can be calculated, and as mentioned before, the RMS current in the complete line cycle can be found by integrating the results in each switching cycle. The method is implemented in MATLAB and the result is shown in Fig. 2-12.

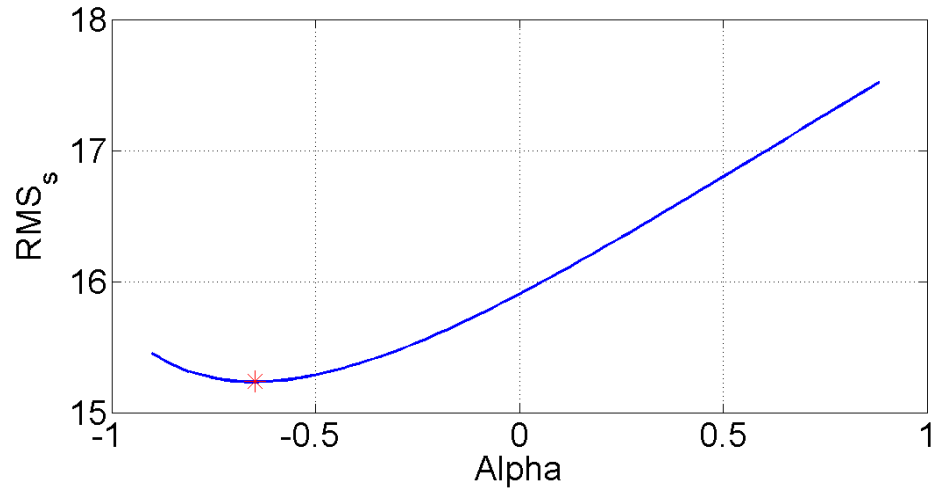

Fig. 2-12. RMS current value through one interleaved leg.

When $\alpha = -0.64$, the RMS current in each interleaved leg is at its minimum value. The other conclusion is that positive coupling factor has shown larger current stress than the negative coupling factor.

Based on the previous analysis, a generalized input current waveform is next shown in Fig. 2-13, where only one switching cycle (from t_0 to $t_o + T$) is presented. The spectrum of the DM noise can be calculated analytically and consideration for the filter design is discussed afterwards. Since the input current has doubled line frequency due to interleaving, a specific pattern of current is repeated twice in the figure. Assume the current starts from x_0, and increase with the ramp rate of k_1. When it reaches the peak value after t_1, it begins to decrease with the ramp rate of k_2 until it goes back to x_0 again.

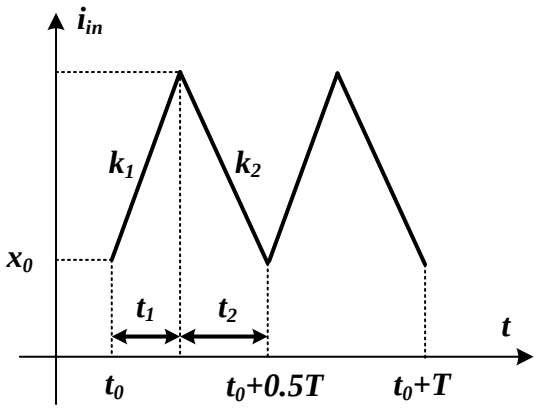

Fig. 2-13. CRM mode PFC input current waveforms.

Each linear segment of the current can be expressed by:

$$i_{in}(t) = x_0 + k_1(t - t_0), t_0 < t < t_o + t_1$$
$$i_{in}(t) = x_1 + k_2(t - t_1 - t_0), t_0 + t_1 < t < t_o + 0.5T \quad \text{Eq. 2-26}$$

The Fourier Transform of the waveform shown in Fig. 2-13 can be formulated as:

$$\begin{aligned} I(j\omega) &= \cdots + \int_{t_0}^{t_o+t_1} (x_0 + k_1(t - t_0))e^{-j\omega t}dt + \cdots \\ &= \cdots + \left(e^{-j\omega(t_0+t_1)} - e^{-j\omega t_0}\right)\left(\frac{jx_0}{\omega} + \frac{k}{\omega^2}\right) + \frac{jkt_1}{\omega}e^{-j\omega(t_0+t_1)} + \cdots \\ &= \ldots + e^{-j\omega(t_0+t_1)}\left(\frac{jx_1}{\omega} + \frac{k_1}{\omega^2}\right) - e^{-j\omega t_0}\left(\frac{jx_0}{\omega} + \frac{k_1}{\omega^2}\right) + \cdots \end{aligned} \quad \text{Eq. 2-27}$$

Note that there are identical terms in the expression which will be cancelled by each other, Eq. 2-27 can be further simplified as (with variables defined in Fig. 2-14):

$$I(j\omega) = \frac{1}{\omega^2}\left(\sum e^{-j\omega t_k}(k_{l,k} - k_{r,k}) + \sum e^{-j\omega\tau_k}(k_{r,k} - k_{l,k+1})\right) \quad \text{Eq. 2-28}$$

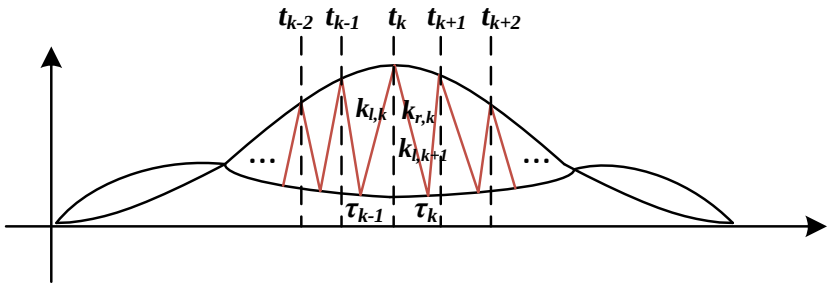

Fig. 2-14 CRM mode PFC input current waveforms. (shown for half line cycle).

where $k_{l,k}$ denotes the ramp rate of the left segment of the current at t_k and $k_{r,k}$ denotes the ramp rate of the right segment of the current. Based on the discussion in section 3.3, the relationship between the ramp rates can be calculated as:

$$k_{l,k} - k_{r,k} = \frac{V_o}{(1+\alpha)L} \qquad \text{Eq. 2-29}$$

Since the input voltage between two switching cycles are the pretty close, we assume them to be the same. Then we would have:

$$k_{r,k} - k_{l,k+1} = \frac{-V_o}{(1+\alpha)L} \qquad \text{Eq. 2-30}$$

Thus, the noise spectrum can be simplified as:

$$I(j\omega) = \frac{1}{\omega^2}\frac{V_o}{(1+\alpha)L}\sum(e^{-j\omega t_k} - e^{-j\omega\tau_k}) \qquad \text{Eq. 2-31}$$

When conducting the EMI noise measurement, the current ripple is measured from a 50Ω resistor via the Line Impedance Stabilization Network (LISN) device. Thus, the noise signal expressed in $dB\mu V$ unit is as follows:

$$V(j\omega) = 20 \cdot \log_{10}(I(j\omega) \cdot 50 \cdot 10^6) \qquad \text{Eq. 2-32}$$

The noise spectrum measured across the resistor can be then drawn by MATLAB, which is shown in Fig. 2-15. One can notice that the peak noise point is happening at 400 kHz. This frequency is exactly twice as 200 kHz, which is the frequency on one

leg when the input is at its peak voltage. Also, frequencies near 200 kHz is lasting longer than frequencies near MHz. The second observation is that the spectrum has a large amplitude drop at around 700 kHz, which happens when the duty ratio is 0.5 and the current ripple is perfectly cancelled.

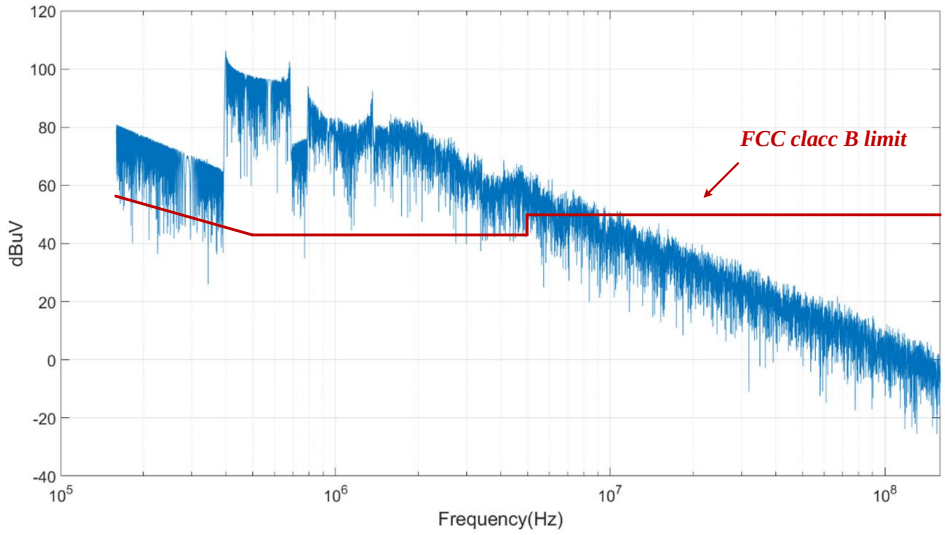

Fig. 2-15. Differential mode noise spectrum (in blue) and FCC class B limit (in red).

A second-order DM filter topology can be utilized in the proposed design, as shown in Fig. 2-16. Two pairs of filter inductor and capacitor is cascaded to enhance the filtering effect.

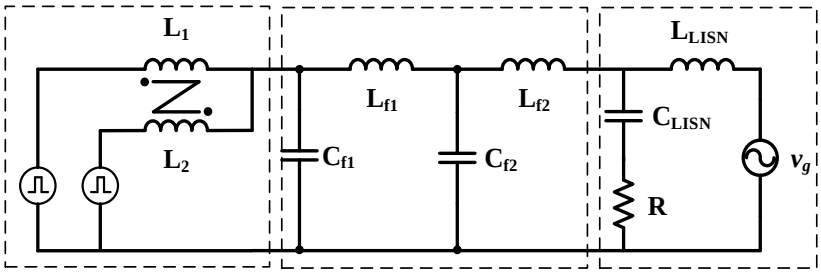

Fig. 2-16. DM filter circuit.

FCC class B is chosen as the EMI standard, whose average limit is shown by the red curve in Fig. 2-15 [57]. Based on the worst case scenario, an attenuation of around

50dB at 400 kHz is required. By setting the cross-frequency at 30kHz with 40dB/dec ramp rate, the filter inductor has the value of $L_{f1} = L_{f2} = 3.6\mu H$, and the filter capacitor has the value of $C_{f1} = C_{f2} = 3.3\mu F$. A damping resistor of 15Ω is added in parallel to the inductor for better performance. As a result, the simulated filtered signal sensed by the LISN is shown in Fig. 2-17.

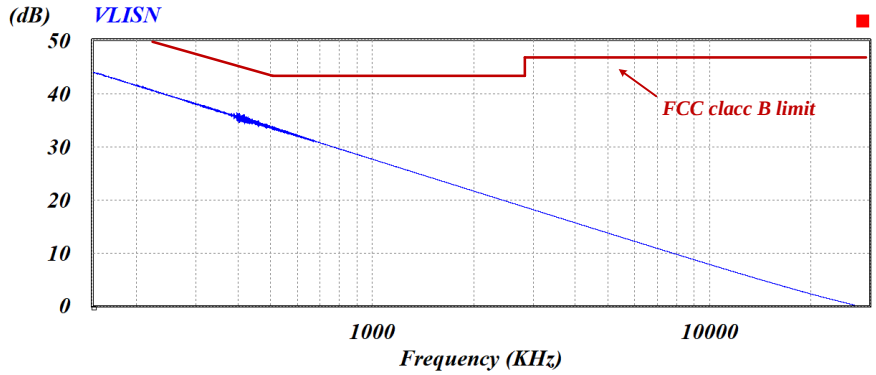

Fig. 2-17. DM filter simulation.

2.4.3 Extra turning-on time and soft switching capability

Zero current in CRM could help reduce the switching losses for the bottom switch (S_2 or S_4 during positive half cycle). With well-controlled deadtime (when one switch is turned off and the other switch is waiting to be turned on), the drain-to-source voltages could reach zero before the actual turn-on, realizing ZVS and further reducing the power losses. As for the top switch (S_1 or S_3), ZVS would always be maintained since the current through the inductor is at its peak value and their output capacitors can be discharged quickly before turned on. Also, they would be turned off at zero current given by CRM, but the bottom switches would still be turned off with hard switching. With GaN devices, the turning off process is extremely fast, leading to relatively small turning off losses. Therefore, the overall switching losses in CRM

operation would be largely reduced, and the efficiency of the PFC rectifier would be improved a lot.

A specific emphasis is given to the analysis of the ZVS of bottom switches, which can be illustrated with Fig. 2-18. It shows different current and voltage values when the bottom switch is about to be turned on. The drain-to-source voltages of S_1 and S_2 are 0V and v_{DC}, respectively. The current of i_1 just reaches 0A at the time.

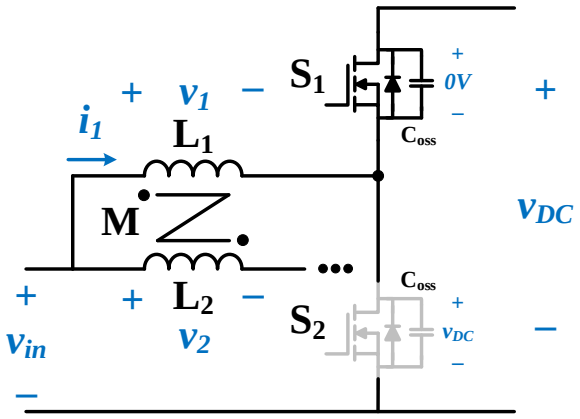

Fig. 2-18. LC resonance circuit during deadtime. (The second interleaved leg is neglected for simplicity).

During the deadtime, an LC resonance would happen among the winding inductance and the two output capacitors of the switches. The change of the voltage on the winding could result in a change of the equivalent inductance, adding more complexity to the analysis than the two independent inductor case. Based on Eq. 2-5, the current variation in the winding can be modelled as:

$$\frac{di_1}{dt} = \frac{v_1 - \alpha(v_{in} - v_{DC})}{(1-\alpha^2)L} \qquad \text{Eq. 2-33}$$

Other relative relationship can be found as:

$$v_1 = v_{in} - v_{low} \qquad \text{Eq. 2-34}$$

$$C_{out}\frac{dv_{low}}{dt} = i_1 + C_{out}\frac{dv_{high}}{dt} \quad \text{Eq. 2-35}$$

$$v_{low} + v_{high} = v_{DC} \quad \text{Eq. 2-36}$$

Combing Eq. 2-33 to Eq. 2-36, the following relationship can be found:

$$2(1-\alpha^2)LC_{out}\cdot\frac{d^2v_{low}}{dt^2} + v_{low} + \alpha(v_{in} - v_{DC}) - v_{in} = 0 \quad \text{Eq. 2-37}$$

Eq. 2-37 is a second order linear coefficient differential equation, whose solution can be easily calculated in Eq. 2-38 with the initial condition of $v_{low,0} = v_{DC}$ and $i_{1,0} = 0$.

$$v_{low} = (v_{in} - v_{DC})(\alpha - 1)cos\omega_r t + v_{in} - \alpha(v_{in} - v_{DC}) \quad \text{Eq. 2-38}$$

where ω_r denotes the resonance frequency and it is expressed as:

$$\omega_r = \sqrt{\frac{1}{2(1-\alpha^2)LC_{oss}}} \quad \text{Eq. 2-39}$$

The current through the winding can be also found as:

$$i_1 = -2(v_i - v_o)(\alpha - 1)C_{oss}\omega_r sin\omega_r t \quad \text{Eq. 2-40}$$

Here, we are interested in whether the bottom switch drain-to-source voltage can be reduced to zero during the resonance, where ZVS turning-on can be achieved for the bottom switch. It can be found by calculating the minimum value of v_{low}, which happens after half resonance cycle ($cos\omega_r t = -1$).

$$v_{low,min} = 2(1-\alpha)v_{in} - (1-2\alpha)v_{DC} \quad \text{Eq. 2-41}$$

Thus, if $v_{low,min} < 0$, we have:

$$v_{in} < \frac{1-2\alpha}{2(1-\alpha)}v_{DC} \quad \text{Eq. 2-42}$$

On the other hand, if $v_{in} > \frac{1-2\alpha}{2(1-\alpha)} v_{DC}$ holds true, the bottom switch would be turned on with hard-switching, increasing more power losses (Valley switching). The voltage waveforms in this case can be found in Fig. 2-19.

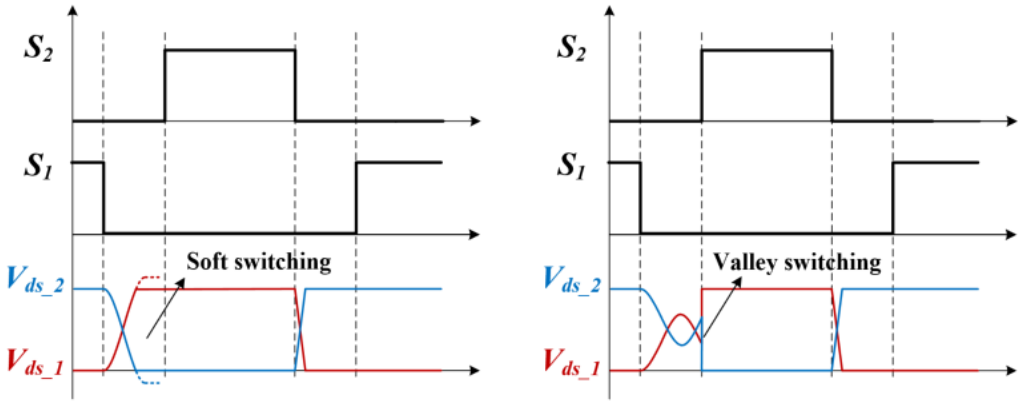

Fig. 2-19. Drain-to-source voltage variation during the deadtime. (Left: with soft switching. Right: without soft switching.)

To minimize this effect, we can introduce an extra turn-on time of the top switch (t_{extra}) to let the inductor current drop a bit below zero. The negative current (defined as I_o) could help the bottom switch drain-to-source voltage drop even more, until it reaches zero. However, at different line voltages, the actual value of t_{extra} also varies, which needs to be carefully calculated and tuned. Too large t_{extra} could impact the input power factor and cause more current distortion.

In this situation, the initial current in Eq. 2-38 should be changed to $i_{1,0} = I_o$ and the expression for the bottom switch drain-to-source voltage would become:

$$v_{low} = \frac{I_0}{2C_{oss}\omega_r} sin\omega_r t + (v_{in} - v_{DC})(\alpha - 1)cos\omega_r t + v_{in} - \alpha(v_{in} - v_{DC}) \quad \text{Eq. 2-43}$$

To ensure exact ZVS operation, the inductor initial current can be then calculated as:

$$I_0 = -\sqrt{\frac{C_{osss}}{L(1-\alpha^2)}(2(2\alpha-1)v_{DC}^2 + 4(1-\alpha)v_{in}v_{DC})} \qquad \text{Eq. 2-44}$$

Next, the extra turn-on time can be found as:

$$t_{extra} = \frac{L_b I_o}{v_{in} - v_{DC}} = \frac{(1+\alpha)LI_o}{v_{in} - v_{DC}}$$
$$= \frac{\sqrt{\frac{C_{oss}L(1+\alpha)}{1-\alpha}[(4\alpha-2)v_{DC}^2 + 4(1-\alpha)v_{in}v_{DC}]}}{v_{DC} - v_{in}} \qquad \text{Eq. 2-45}$$

With different coupling factor values, the extra turn-on time during half line cycle can then be depicted in Fig. 2-20. It shows that direct coupling would need extra turning-on time on a wider input voltage range with a larger value of it, comparing to inverse coupling. On the other hand, inverse coupling would offer advantages of smaller extra turning-on time, and for most time it is even not required. Therefore, the current distortion is expected to be smaller.

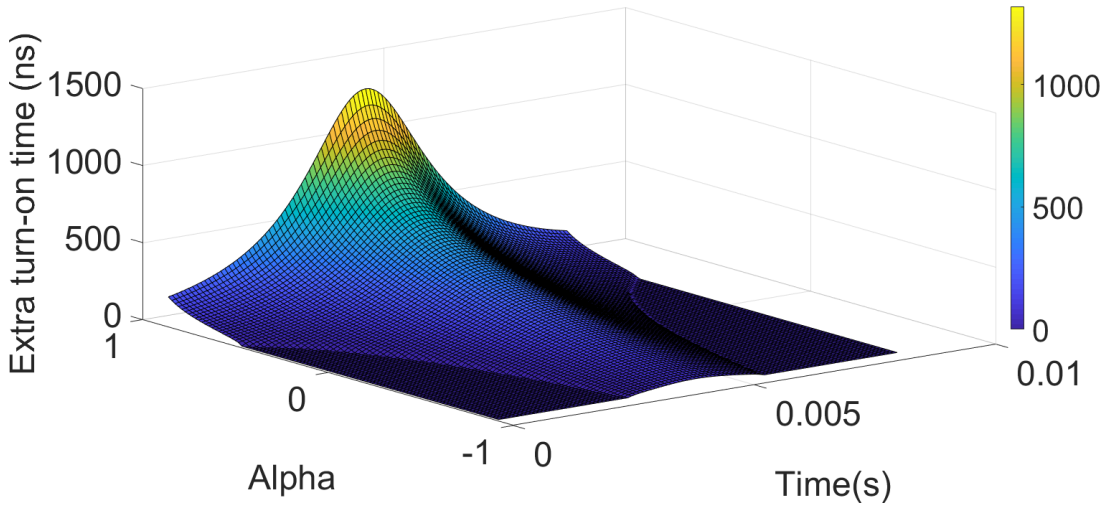

Fig. 2-20. Extra turn-on time variation during a half line cycle.

Based on the consideration of extra turn-on time and the current stress, inverse coupling is applied in this design with $\alpha = -0.64$, and the EMI filter is then designed based on that.

2.5 Closed-loop Phase Shift Control of the Interleaved Switches

2.5.1 Limitations of the open-loop phase control method

One of the most commonly used open-loop phase control scheme in the interleaved structure is the “master-slave” method, where the turning-on time of one leg (master) is controlled actively by sensing the zero-crossing of the current while the other leg (slave) is manually given a time delay of half switching period. As for the turning-off time, it can be conducted in two ways: current-mode or voltage-mode, as shown in Fig. 2-21.

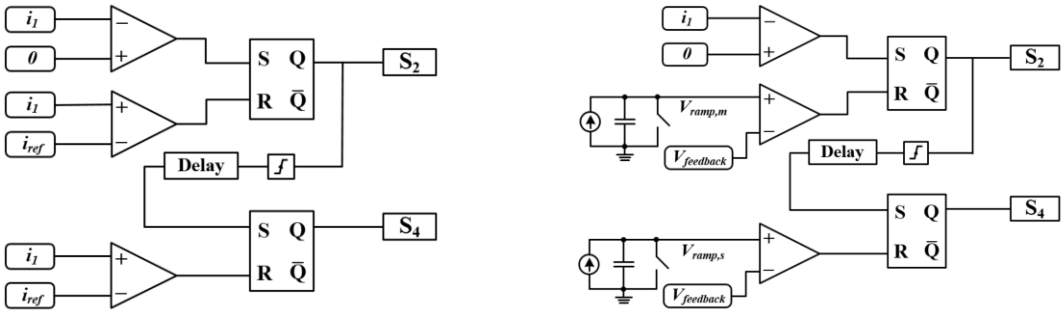

Fig. 2-21. Diagram of current-mode and voltage-mode control.

It can be noted that in current-mode control, the master bottom switch would be turned off when the inductor current reached the preset reference current i_{ref}, and will be turned on again when the current is reduced to zero. The rising-edge of the turning-on signal of the master switch would go through a delay module, which can postpone the signal by half of the last master switching period, and then trigger the turning on time of the slave switch. The turning off moment of the slave switch is also controlled by the current reference. Relative inductor current and switching signal can be found in Fig. 2-22.

As for voltage-mode control, the master turning-on time is still triggered by the zero current crossing point, but the turning-off time is controlled by a voltage feedback signal $V_{feedback}$. It comes from the voltage loop of the converter to stabilize the output voltage. Here, two sets of fixed ramp-rate analog counters (composed of a fixed value current source, a capacitor and a reset switch connected in parallel) are applied. When the voltage on the capacitor reaches $V_{feedback}$ for both the master and slave switch, they should be turned off, and the reset switch would be turned on at the same time to pull the capacitor voltage back to zero. The turning-on moment of the slave switch also comes from a delay module, that will be postponed half of the last switching period of

the master switch. Relative inductor current and switching signal can be found in Fig. 2-22.

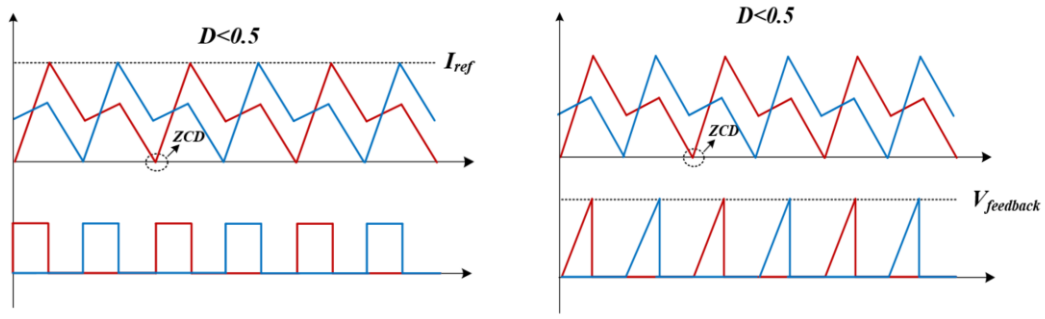

Fig. 2-22. Theoretical waveforms of current-mode and voltage-mode control.

The open-loop control method would work fine if all the design parameters are as expected and no errors would happen during the operation. In fact, the real coefficients and the working condition are not ideal, which could impact the performance of the PFC rectifier. Relative problems were discussed in [56] previously based on two independent inductors. Here, we extend the scope to the coupled inductor and mainly analyze two possible factors: Mismatch inductance and turning-on time disturbance.

a. Mismatch inductance

In previous analysis, we already assumed $L_1 = L_2$. However, their values may not be the same in reality. If a mismatch happens, the current waveform, especially the one on the slave leg would experience distortions. We analyze this by first looking into the change in the equivalent inductance caused by the mismatch.

First, we define the mismatch coefficient $m = \frac{L_1}{L_2}$. The coupling factor is then defined as $\alpha = \frac{M}{L_1}$. By referring to Eq. 2-7, we can calculate the equivalent inductance of the first ($L_{eqx,fst}$) and second ($L_{eqx,sec}$) winding:

$$L_{eqx,fst} = \frac{L_1(1-m\alpha^2)}{1-\frac{\alpha m}{A_x}} \quad \text{Eq. 2-46}$$

$$L_{eqx,sec} = \frac{L_2(m\alpha^2-1)}{\alpha A_x - 1} \quad \text{Eq. 2-47}$$

With the known values of A_x, the inductance values can be listed in Table 2-4 and Table 2-5 for different input line voltages.

Table 2-4. Equivalent inductance values in different switching phases. (D > 0.5)

	State I	**State II**	**State III**	**State IV**
v_1	v_{in}	v_{in}	v_{in}	$v_{in}-v_{DC}$
v_2	v_{in}	$v_{in}-v_{DC}$	v_{in}	v_{in}
A_x	1	$\frac{v_{in}}{v_{in}-v_{DC}}=\frac{1-d}{-d}$	1	$\frac{v_{in}-v_{DC}}{v_{in}}=\frac{-d}{1-d}$
$L_{eqx,fst}$	$\frac{1-m\alpha^2}{1-m\alpha}L_1$	$\frac{(1-m\alpha^2)(1-d)}{1-d+dm\alpha}L_1$	$\frac{1-m\alpha^2}{1-m\alpha}L_1$	$\frac{(1-m\alpha^2)d}{d+(1-d)m\alpha}L_1$
$L_{eqx,sec}$	$\frac{m\alpha^2-1}{\alpha-1}L_2$	$\frac{d(1-m\alpha^2)}{\alpha(1-d)+d}L_2$	$\frac{m\alpha^2-1}{\alpha-1}L_2$	$\frac{(1-d)(m\alpha^2-1)}{(1-\alpha)d-1}L_2$

Table 2-5. Equivalent inductance values in different switching phases. (D < 0.5)

	State I	**State II**	**State III**	**State IV**
v_1	v_{in}	$v_{in}-v_{DC}$	$v_{in}-v_{DC}$	$v_{in}-v_{DC}$
v_2	$v_{in}-v_{DC}$	$v_{in}-v_{DC}$	v_{in}	$v_{in}-v_{DC}$
A_x	$\frac{v_{in}}{v_{in}-v_{DC}}=\frac{1-d}{-d}$	1	$\frac{v_{in}-v_{DC}}{v_{in}}=\frac{-d}{1-d}$	1
$L_{eqx,fst}$	$\frac{(1-m\alpha^2)(1-d)}{1-d+dm\alpha}L_1$	$\frac{1-m\alpha^2}{1-m\alpha}L_1$	$\frac{(1-m\alpha^2)d}{d+(1-d)m\alpha}L_1$	$\frac{1-m\alpha^2}{1-m\alpha}L_1$
$L_{eqx,sec}$	$\frac{d(1-m\alpha^2)}{\alpha(1-d)+d}L_2$	$\frac{m\alpha^2-1}{\alpha-1}L_2$	$\frac{(1-d)(m\alpha^2-1)}{(1-\alpha)d-1}L_2$	$\frac{m\alpha^2-1}{\alpha-1}L_2$

Likewise, we can define the following expression for simplicity:

$$L_{a,fst} = \frac{(1-m\alpha^2)(1-d)}{1-d+dm\alpha}L_1, L_{a,sec} = \frac{(1-d)(m\alpha^2-1)}{(1-\alpha)d-1}L_2 \quad \text{Eq. 2-48}$$

$$L_{b,fst} = \frac{1-m\alpha^2}{1-m\alpha}L_1, L_{b,sec} = \frac{m\alpha^2-1}{\alpha-1}L_2 \quad \text{Eq. 2-49}$$

$$L_{c,fst} = \frac{(1-m\alpha^2)d}{d+(1-d)m\alpha}L_1, L_{c,sec} = \frac{d(1-m\alpha^2)}{\alpha(1-d)+d}L_2 \quad \text{Eq. 2-50}$$

As a comparison, the equivalent inductance when the two windings are matched are referred as $L_{a,nom}, L_{b,nom}$ and $L_{c,nom}$. If $\alpha = -0.64$, the inductance variation in half line cycle can be depicted in Fig. 2-23 and Fig. 2-24.

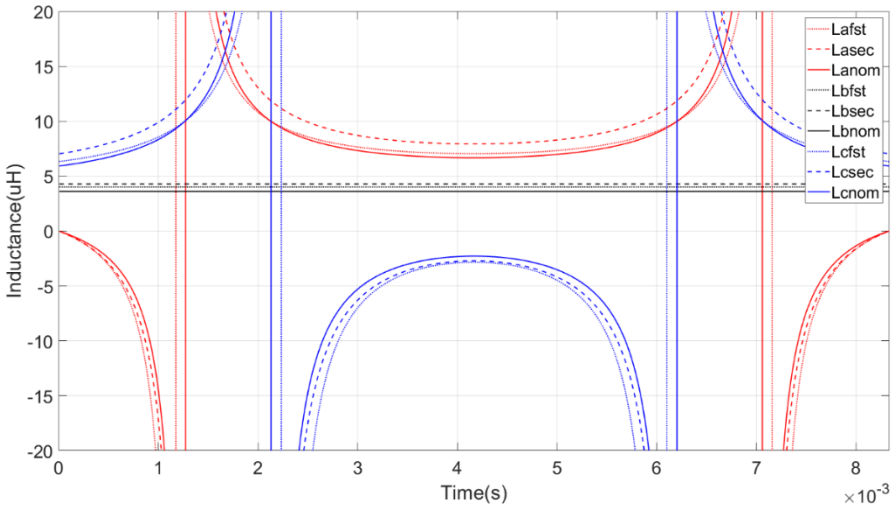

Fig. 2-23. Equivalent inductance variation in half line cycle ($L_2 > L_1$).

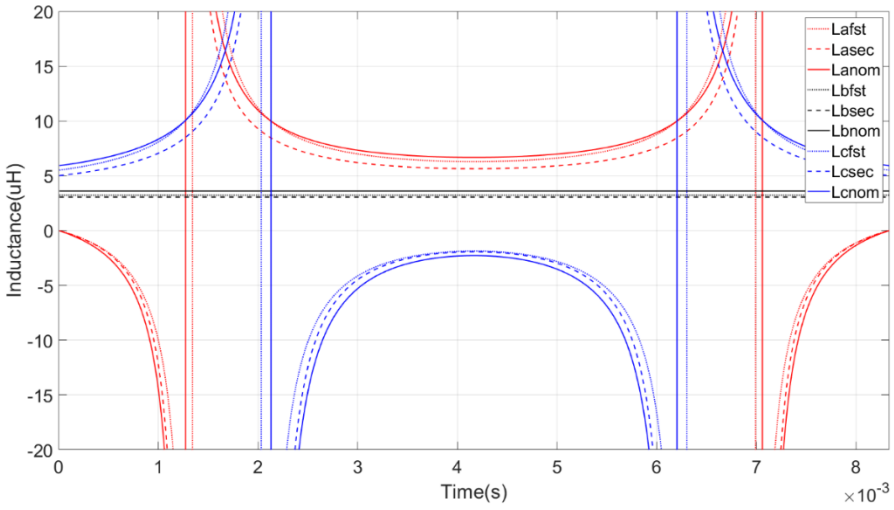

Fig. 2-24. Equivalent inductance variation in half line cycle ($L_2 < L_1$).

The following analysis would take $D < 0.5$ as an example. As can be seen, we have $L_{a,sec} > L_{a,fst} > L_{a,nom}$, $L_{b,sec} > L_{b,fst} > L_{b,nom}$ and $|L_{c,fst}| > |L_{c,sec}| > |L_{c,nom}|$when $L_2 > L_1$. On the other hand, the relationship would become $L_{a,nom} > L_{a,fst} > L_{a,sec}$, $L_{b,nom} > L_{b,fst} > L_{b,sec}$ and $|L_{c,nom}| > |L_{c,sec}| > |L_{c,fst}|$ when $L_2 < L_1$. Their impacts on the current waveforms in both current-mode and voltage-mode control are shown in Fig. 2-25.

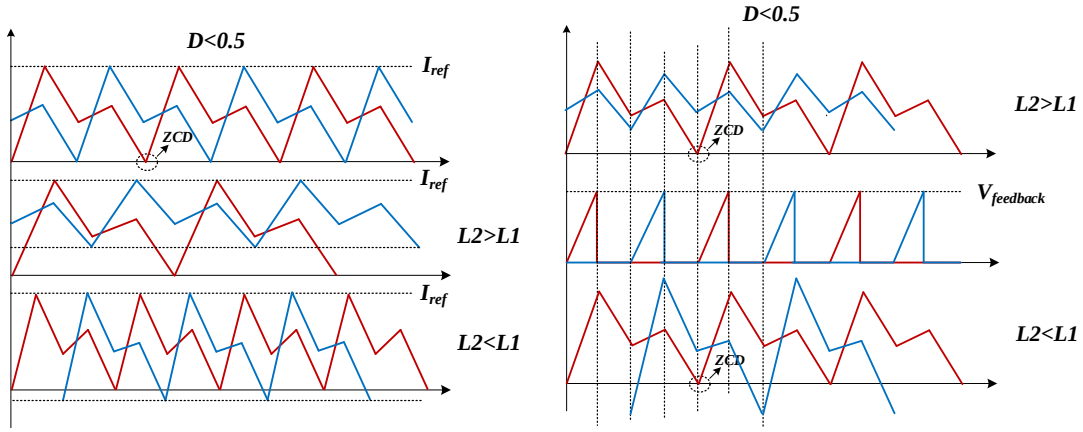

Fig. 2-25. Impacts of mismatch winding on the current waveforms.

In current-mode control, due to the inductance relationship and fact that current must reach I_{ref}, the slave leg current would start from a positive value when $L_2 > L_1$ and from a negative value when $L_2 < L_1$. Two problems can be seen from here. For the case of $L_2 > L_1$, the slave switch would lose ZVS and become hard-switching, increasing the power losses. Second effect is that the average current of the slave inductor would not be equal to the master leg. Since there is no control on the output voltage, the actual transmitted power would exceed the rated number if $L_2 > L_1$ or below it when $L_2 < L_1$.

In voltage-mode control, the waveforms under mismatch windings are similar to current-mode control, except that the slave current would not necessarily reach the same peak current as the master current. With the ability to control the output voltage, the actual transmitted power is still under control, and thus the average current of the slave is still the same as the master leg. However, the hard-switching problem when $L_2 > L_1$ still exists.

b. Turn-on time perturbation

In open-loop control, the turn-on instant of the bottom switch is managed manually. If perturbation happens in the controller, the current waveforms would also be affected. It can be illustrated in Fig. 2-26 (shown for the case when $D < 0.5$).

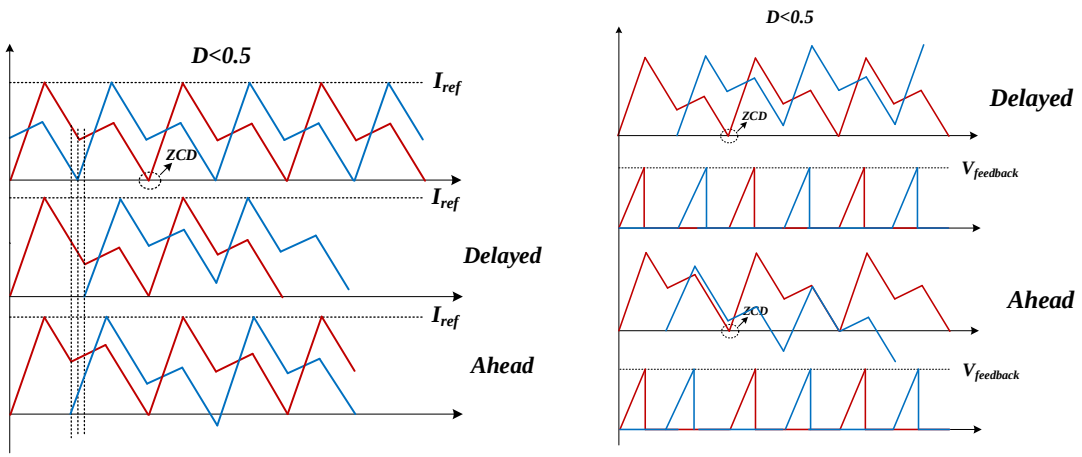

Fig. 2-26. Impacts of turning-on time perturbation on the current waveforms. (Left: current-mode control. Right: voltage-mode control)

In current-mode control, non-ZVS operation would happen for the delayed perturbation and negative current would occur for ahead perturbation. In voltage-mode control, both delayed and ahead perturbation would cause the slave leg-current unstable.

2.5.2 Implementation of the closed-loop phase shift control

In closed-loop control, the master-leg switches are controlled in the same way as in open-loop, but the slave-leg switches turn-on instants are controlled by a loop composed of sensing, filtering, comparing and compensating modules. The complete control diagram together with the circuit structure is shown in Fig. 2-27. The upper block illustrates the typical CRM control in voltage-mode for the master-leg switches, where ZCD and voltage control are both maintained. The bottom block illustrates the closed-loop algorithm for the slave-leg switches. The turn-on instants of the two bottom switches are captured and compared. The average value of the output, which is given by a low-pass filter, would reflect the phase difference information. 180° phase

difference would result in zero output, which will be passed to a PI compensator to generate the modulation signal. It will be added with the voltage loop feedback signal and will be fed into the slave leg control loop. In this way, ZCD is also maintained at the slave-leg unlike the case in open-loop control, and the phase difference can be also managed.

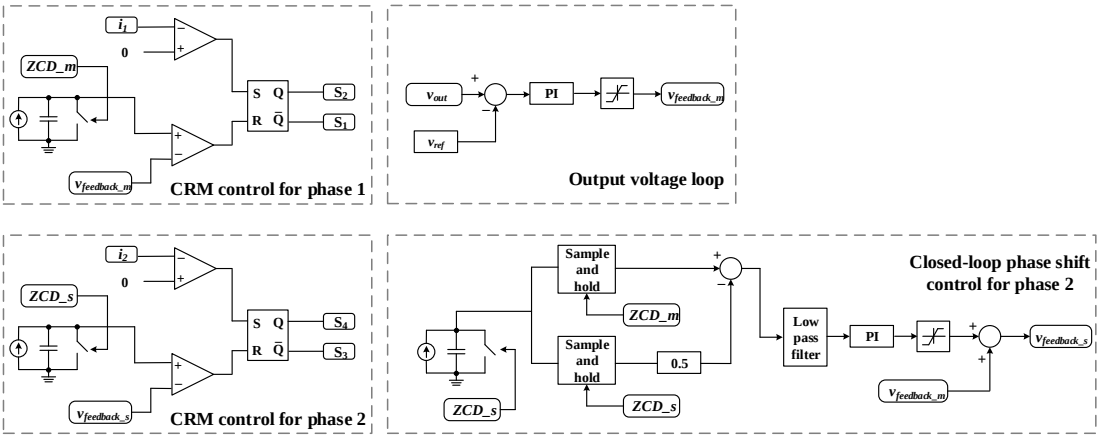

Fig. 2-27. Diagram of the closed-loop control algorithm.

In order to verify the aforementioned control algorithm, simulation is carried out in PSIM 11.1.6. For simplicity, the first simulation is conducted for the case of two independent inductors, with relative parameters listed in Table 2-6.

Table 2-6. Simulation parameters for two independent inductors.

Parameters	**Values**
Inductor (μH)	16
Peak power (W)	1000
Input voltage RMS (V)	240
Load (Ω)	160

The gain and the time constant of the PI controller is chosen as 0.001 and 0.005. The simulated waveform of the two inductors are shown in both line cycles and switching cycles (Fig. 2-28 and Fig. 2-29). As can be seen, their phase difference is controlled well at 180°, which proves effectiveness of the control algorithm.

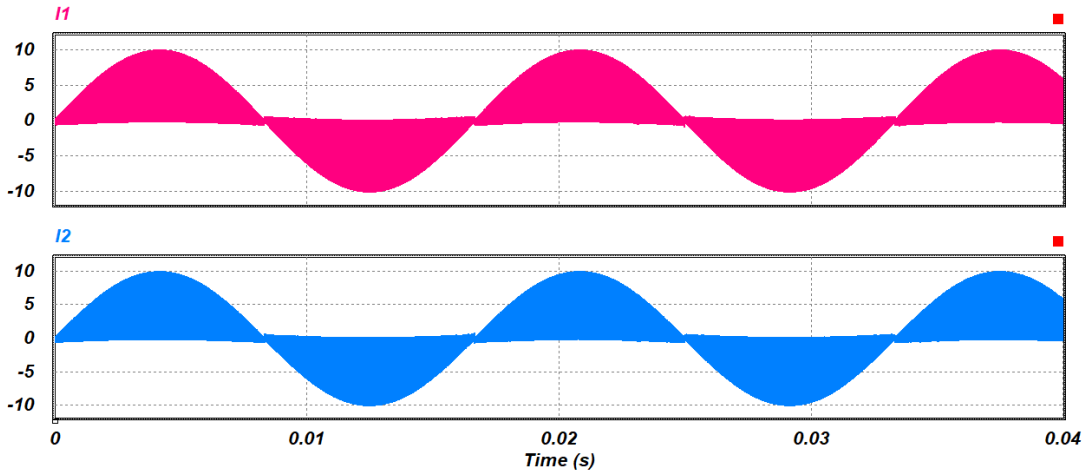

Fig. 2-28. Simulated current in line cycles.

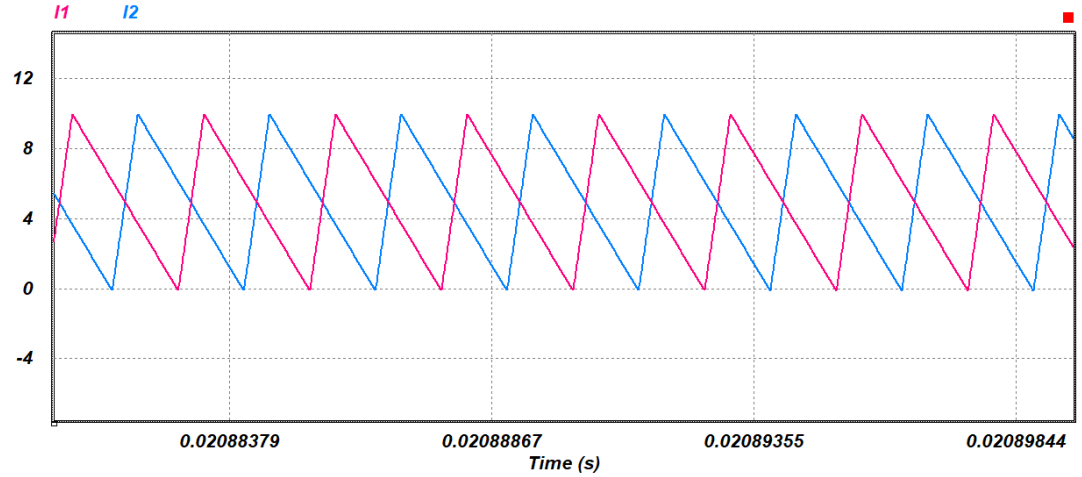

Fig. 2-29. Simulated current in switching cycles.

For the coupled inductor, the simulation is based on current-mode control and it is conducted with the following coefficients.

Table 2-7. Simulation parameters for coupled inductor.

Parameters	Values
Self inductance (μH)	10
Mutual inductance (μH)	-6.4
Peak power (W)	6600
Input voltage RMS (V)	240
Load (Ω)	24.24

The current waveforms of each interleaved leg (I_1 and I_2) and the total input current (I_{in}) are shown respectively in Fig. 2-30.

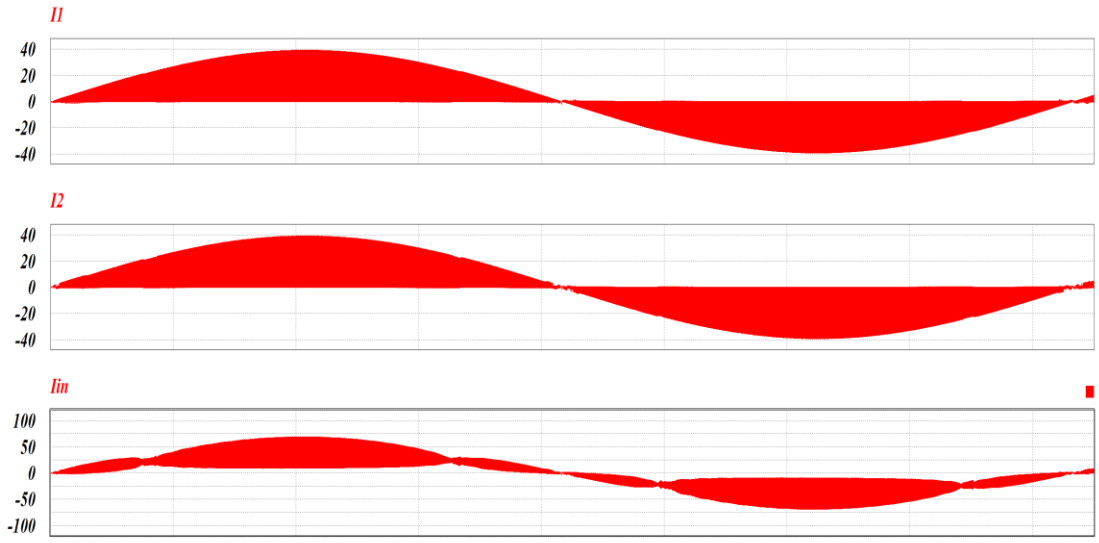

Fig. 2-30. Simulated waveforms.

It can be noted that the current of each interleaved leg would return to zero after each switching cycle. The average of the current would approach a sinusoidal wave, which is in phase with the input voltage. The input current is the summation of the two currents on both legs, and due to the 180 degree phase shift, the current ripple is shown to be reduced. Especially when the input voltage is half as the output voltage, the ripple

current would be zero. The simulated result is in agreement with the analysis in Chapter 3. Next, the RMS current value, input current power factor and the total harmonic distortion (THD) can be automatically calculated by the software and are shown in Table 2-8. As can be seen, the RMS current is well matched with the result calculated from Fig. 2-12, and the power factor, as well as the THD, are in reasonable range.

Table 2-8. Simulation results.

Parameters	**Values**
First leg current RMS value	15.3 A
Second leg current RMS value	15.4 A
Input current RMS value	29.6 A
Input power factor	99.68%
Total harmonic distortion	4.3%

An enlarged view of the currents is shown respectively in Fig. 2-31 (for duty ratio larger than 0.5) and Fig. 2-32 (for duty ratio smaller than 0.5). As can be seen, the schemes of the current in two legs are identical and well matched with the theoretical waveforms. In addition, the 180 degree phase shift is well maintained between the two winding currents. Doubled switching frequency is also shown in the input current waveform.

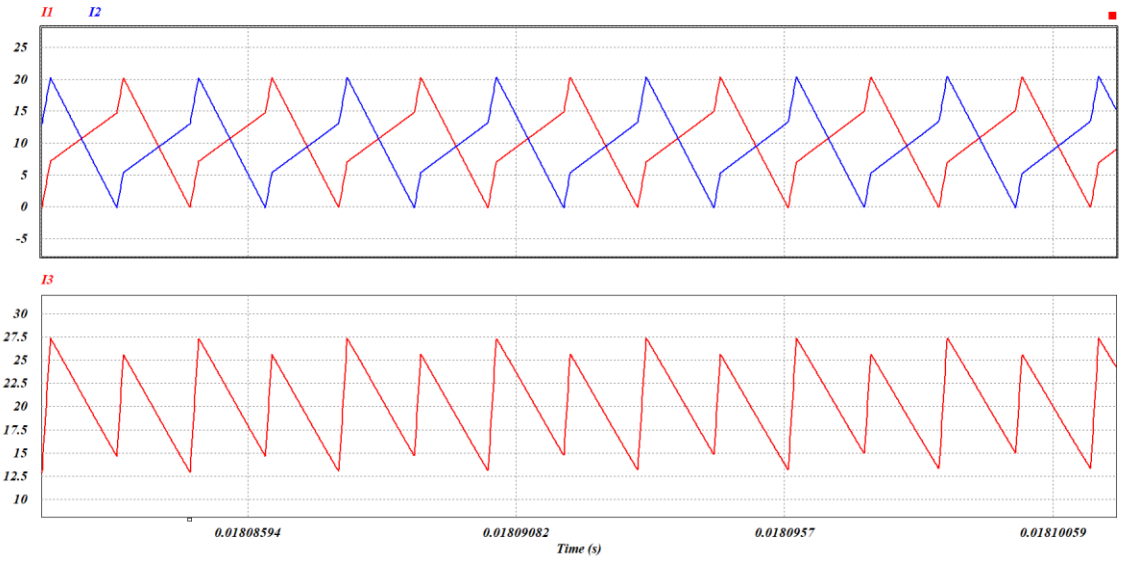

Fig. 2-31. Current waveforms for D > 0.5.

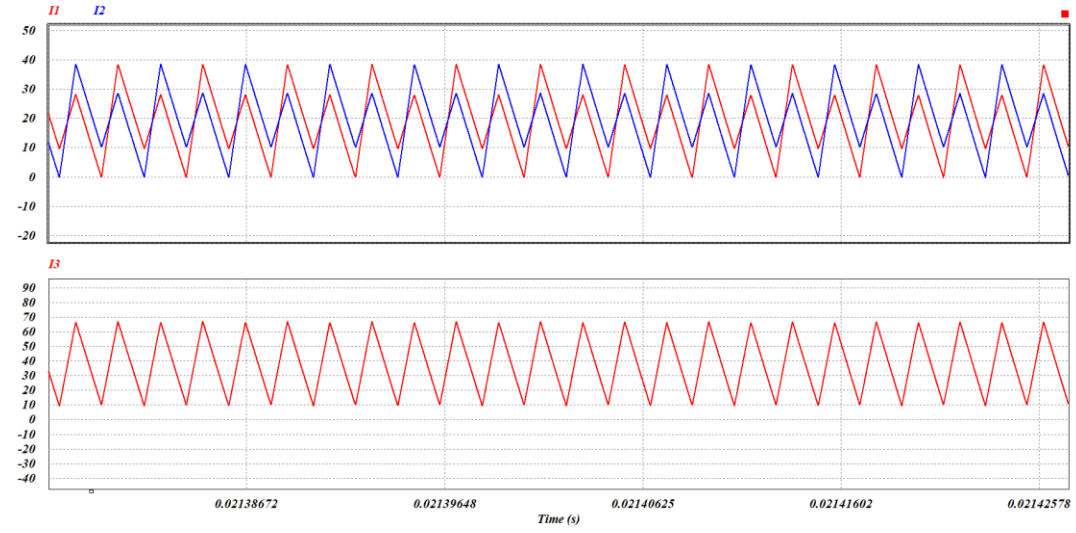

Fig. 2-32. Current waveforms for D < 0.5.

2.6 Hardware considerations

In the PFC stage, the zero crossing of the current through each interleaved leg is critical since it can be used to determine the turn-on time of the corresponding switch, and also to measure the phase difference between the two legs. Two common types of the current sensing technology are based on hall-effect components and current sensing

resistors. Due to the MHz frequency current ripple, hall-effect sensors cannot be applied, since their bandwidth are usually limited to 1MHz, which would lead to serious errors in the results. Thus, sensing resistors are utilized in this design, which are placed in series with the corresponding inductor winding (Fig. 2-33). To explain the working principle, only the sensing resistor in the first leg is drawn in the figure. The winding current is transferred to the voltage across the resistor, which is then connected to the inputs of a high-speed comparator. Zero-crossing can be sensed by detecting the voltage change on the output port of the comparator. Since the resistor ground is different from the controller ground, an isolated dc-dc power supply is applied to generate an isolated supply voltage to the comparator. To receive the sensed signal, a digital isolator is used to convert the signal back to the controller ground domain, and further sensed by the ADC input of the controller. Relative component selection is shown in Table 2-9.

Table 2-9. Component selection of the current sensing circuits.

Component	**Part number**	**Note**
Current sensing resistor	CRA2512-FZ-R010ELF	0.01 OHM 1% 3W , current sense
Comparator	LTC6754	High Speed Rail-to-Rail
Comparator decoupling cap	C0805C102K8RACTU	1000PF 10V
Comparator decoupling cap	C0805C103K8RAC7800	10000PF 10V
Isolated power supply	MEU1S0303ZC	DC DC CONVERTER 3.3V 1W
High speed digital isolator	ADUM1100ARZ-RL7	DGTL ISO 2.5KV GEN PURP 8SOIC

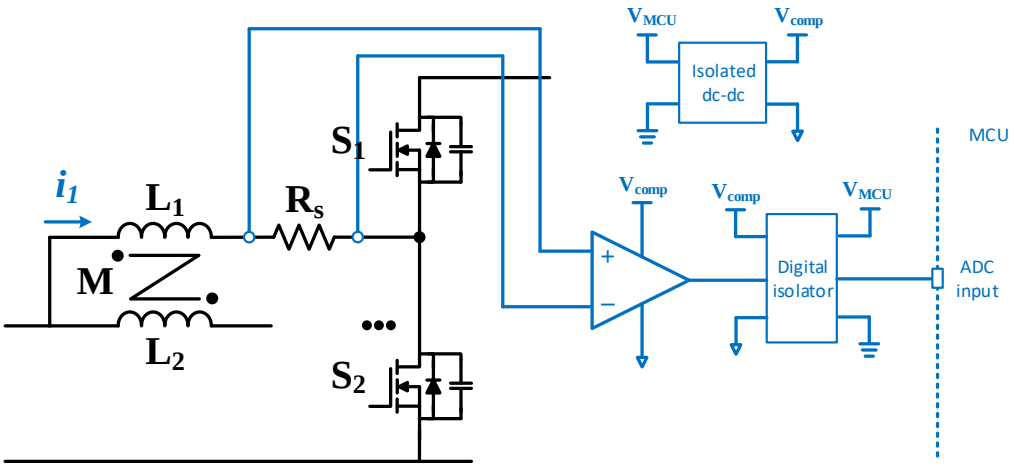

Fig. 2-33. Current sensing circuit.

Voltage sensing in the PFC stage is more straightforward compared to the current sensing. Both the input voltage and the DC-link voltage are required to be sensed for proper control. Since the DC-link shares the same ground with the MCU, its voltage can be sensed directly by scaling using a voltage divider. The input terminals, however, are not directly referred to the MCU ground. In addition, the input voltage is a bipolar signal which cannot be directly sensed by the ADC. Its value can be derived instead by two separate voltage dividers connected to each terminal, which is shown in Fig. 2-34.

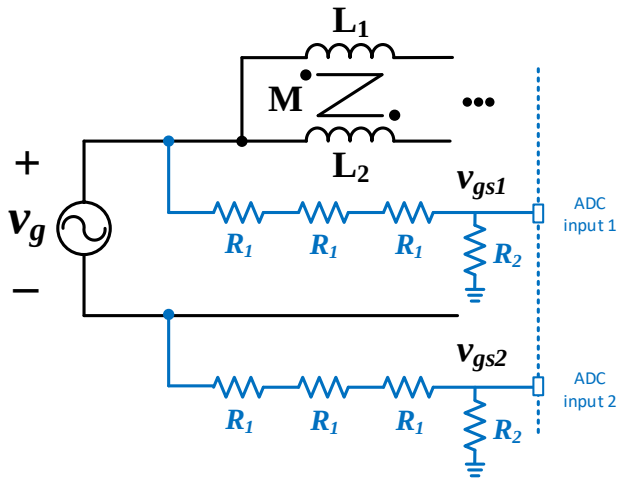

Fig. 2-34. Voltage sensing circuit.

The sensed voltage waveforms are depicted in Fig. 2-35. The sensing ratio is expressed as:

$$A_v = \frac{R_2}{3R_1 + R_2} \qquad \text{Eq. 2-51}$$

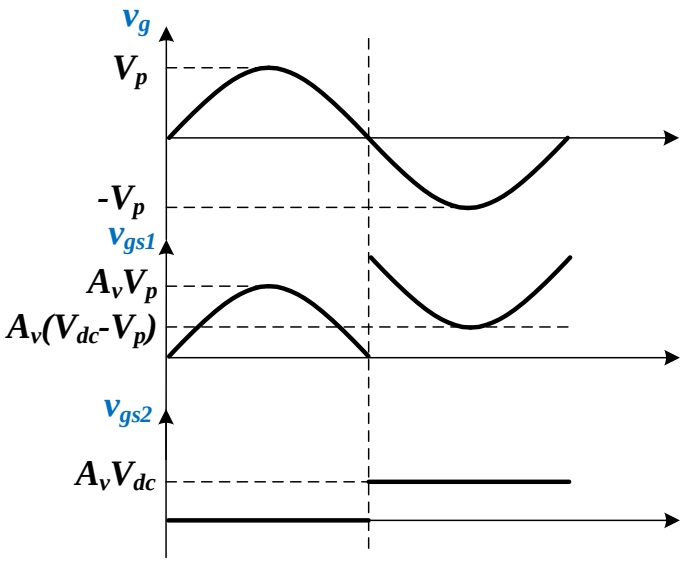

Fig. 2-35. Sensed voltage waveforms.

By subtracting v_{gs1} with v_{gs2}, we could have the sensed input voltage as:

$$v_{gs} = v_{gs1} - v_{gs2} = A_v v_g \qquad \text{Eq. 2-52}$$

The two resistance values are chosen as $R_1 = 178k\Omega$ and $R_2 = 4.7k\Omega$. The sensing ratio is calculated as $A_v = 0.0088$. Detailed selection of the components are shown in Table 2-10.

Table 2-10. Component selection of the voltage divider at the input side.

Symbol	Part number	Description
R1	RN73C2A178KBTDF	178K OHM 0.1% 1/10W
R2	ERA-6ARW472V	RES SMD 4.7K OHM 0.05% 1/8W 0805

Furthermore, the component selection of the DC-link voltage divider is shown in Table 2-11.

Table 2-11. Component selection of the voltage divider at the DC-link.

Symbol	Part number	Description
R1	RN73C2A261KBTDF	261K OHM 0.1%
R2	ERA-6ARW512V	5.1K OHM 0.05%

To generate the required CRM mode gating signals, the Pulse Width Modulation (PWM) module needs to work at the External PWM Reset Mode, where the ZCD signal works as an external trigger to reset the PWM counter and pull up the output voltage (Fig. 2-36). A comparison value (COMP) is coming from the voltage closed-loop compensator to control the correct turn-off time, and further control the power factor. Deadtime module helps generate proper deadtime between the high-side and low-side switches. Extra turn-on time can be pre-programmed into the MCU and manually adds a delay to the ZCD signal.

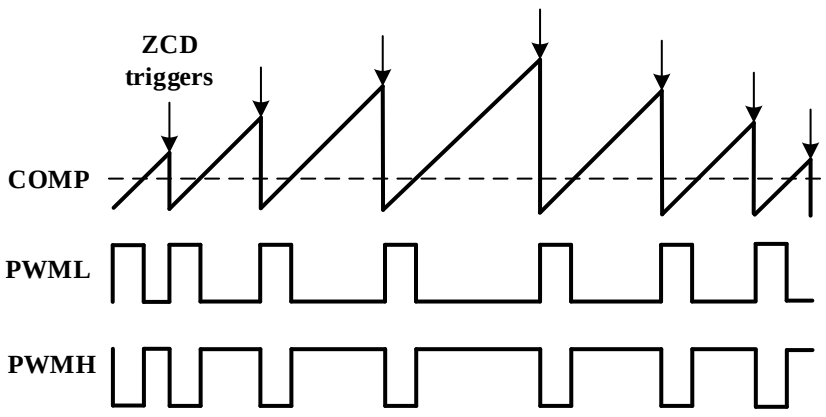

Fig. 2-36. PWM signal generation in the controller.

2.7 Active buffer

In a conventional two-stage onboard CHARGER, a large capacitor must be placed at the DC-link to absorb the reactive power caused by the single-phase input. For example, if 5% ripple is allowed at 400V average value, the capacitance value would exceed 1mF. Considering both the voltage level and the capacitance, multiple capacitors connecting in series and parallel are often applied, which would consume a large portion of the volume. Although high-frequency switching could help reduce the volume of most passive components, it could not help with the reduction of the DC-link capacitors, since the reactive power is happening at the line frequency. Here, we applied a technology known as "active buffer" [58], [59], to replace the large DC-link capacitors with a sub-circuit that actively absorb the reactive power. The topology is referred from [59] and is shown in Fig. 2-37. The only two large value capacitors are C_1 and C_2, where the first one takes a portion of the reactive power and the second one helps to keep the DC-link voltage stable by modulating the switching duty ratio. Since the voltage ripple across each capacitor is not restricted but the overall voltage is required, the capacitance of C_1 and C_2 can be made smaller than 1mF, which could help reduce the volume.

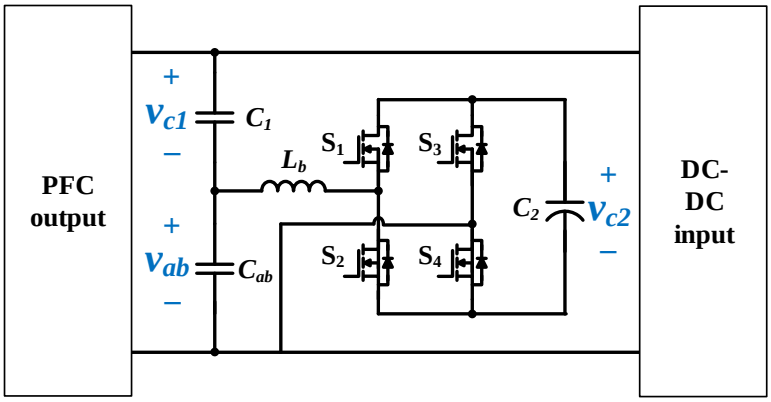

Fig. 2-37. Active buffer topology between the PFC stage and the DC-DC stage.

The operation principle of the above circuit could be shown in Fig. 2-38. In the first half line cycle, the positive reactive power would flow into the active buffer and C_1 and C_2 would be charged to store the energy. Assume the average voltage of C_1 and C_2 are V_{c1} and V_{c2} respectively. The Differences between the peak voltage and the average are defined as ΔV_1 and ΔV_2. Since the DC-link voltage is kept relatively stable, thus we could assume it to be constant as $V_{DC} = 400\text{V}$. Then we have the average value of the voltage across C_{ab} as: $v_{ab} = V_{DC} - v_{C1}$.

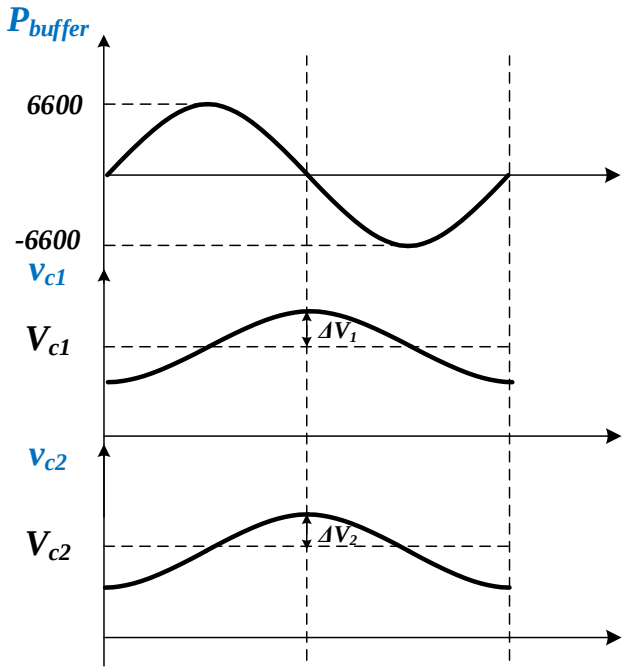

Fig. 2-38. Operation waveforms of the applied active buffer circuit.

Seen from the side of C_{ab}, the switching part can be regarded as a boost circuit, where S_1, S_4 are switching simultaneously with a duty ratio of d, and S_2, S_3 are switching complementarily compared to S_1, S_4. By doing the cycle average, the following relationship between the input and output voltages can be formulated:

$$v_{ab} = (2d - 1)v_{C2} \quad \text{Eq. 2-53}$$

By taking the average and ripple values into Eq. 2-53, the following equations could be derived:

$$V_{ab} - \Delta V_{ab} = (2(D - \Delta d) - 1) \cdot (V_{C2} + \Delta V_2) \quad \text{Eq. 2-54}$$

$$V_{ab} + \Delta V_{ab} = (2(D + \Delta d) - 1) \cdot (V_{C2} - \Delta V_2) \quad \text{Eq. 2-55}$$

Since $\Delta V_{ab} = \Delta V_1$, we have:

$$\Delta V_1 = 2V_{C2}\Delta d - (2D - 1)\Delta V_2 \quad \text{Eq. 2-56}$$

To ensure the right operation of the active buffer circuit, there are several constraints of the parameters. The first one is that the variation of the duty ratio should also be less than 0.5, or the actual duty ratio would exceed 1 or below 0, which is given by:

$$\Delta d = \frac{\Delta V_{C1} + (2D-1)\Delta V_2}{2V_{C2}} < 0.5 \qquad \text{Eq. 2-57}$$

The second constraint is that the input voltage should also be less than the output voltage, due to the boost operation of the circuit:

$$v_{ab} < v_{C2} \qquad \text{Eq. 2-58}$$

It can also be written as:

$$V_{ab} + \Delta V_{ab} < V_{C2} - \Delta V_{C2} \qquad \text{Eq. 2-59}$$

Since the reactive power is mostly received by C_1 and C_2, the energy stored in these two capacitors should equal the input energy in half line cycle:

$$0.5C_1[(V_{C1} + \Delta V_1)^2 - (V_{C1} - \Delta V_1)^2] + 0.5C_2[(V_{C2} + \Delta V_2)^2 - (V_{C2} - \Delta V_2)^2] = \int_{\frac{T}{2}} P(t)dt \qquad \text{Eq. 2-60}$$

After simplification, Eq. 2-60 can be written as:

$$2C_1\Delta V_1 V_{C1} + 2C_2 V_{C2}\Delta V_2 = 19.45 \qquad \text{Eq. 2-61}$$

Suppose $v_{ab} > 0$, then $D = \frac{\frac{V_{ab}}{V_{C2}}+1}{2} > 0.5$. The first constraint can be made more precise as:

$$\Delta d = \frac{\Delta V_{C1} + (2D-1)\Delta V_2}{2V_{C2}} < 1 - \frac{\frac{V_{ab}}{V_{C2}} + 1}{2} \qquad \text{Eq. 2-62}$$

Assume $V_{ab} = 100V$, $C_1 = 250\mu F$, $\Delta V_1 = 100V$, $V_{C1} = 300V$. From Eq. 2-61 we could have:

$$C_2 V_{C2} \Delta V_2 = 2.225 \quad \text{Eq. 2-63}$$

We further assume $V_{C2} = 250V$, then Eq. 2-63 becomes:

$$C_2 \Delta V_2 = 0.0089 \quad \text{Eq. 2-64}$$

Based on the above assumption, the first constraint can be simplified as:

$$\Delta V_2 < 125V \quad \text{Eq. 2-65}$$

And the second constraint would be:

$$\Delta V_2 < 50V \quad \text{Eq. 2-66}$$

Thus, if we choose $C_2 = 400\mu F$, ΔV_2 can be calculated as 22.25V, which satisfy both Eq. 2-65 and Eq. 2-66. A complete list of parameters is shown in Table 2-12.

Table 2-12. Active buffer component parameters.

Parameters	**Values**
C_1	$250\mu F$
V_{C1}	$300V$
ΔV_1	$100V$
C_2	$400\mu F$
V_{C2}	$250V$
ΔV_2	$22.25V$
D	0.7
V_{ab}	$100V$

Chapter 3: Resonant DC-DC Converter with Extended Harmonic Approximation

3.1 Introduction

In this chapter, circuit operation principles and control methods will be introduced for the DC-DC stage. Since the output of the DC-DC stage is the battery, which could show various voltages at different state of charge (SoC), the converter itself should be able to operate efficiently at different loading conditions. A simplified charging process of a battery could be illustrated by the charging profile (Fig. 3-1), which explicitly clarifies the charging currents during different times through the charging process. Definitions of different variables shown in the figure are explained here: $V_{out,min}$ is minimal battery voltage; $V_{out,nom}$ is nominal battery voltage at the peak power point; $V_{out,max}$ is maximum battery voltage at full capacity; $I_{out,max}$ is battery charging current at CC region; $I_{out,min}$ is battery charging current at the end of process; t_{CC} is Constant Current (CC) region duration; t_{CV} is Constant Voltage (CV) region duration. When the battery voltage is low (could be as low as 200V), the charging current is at its peak value (16.5A for a 6.6 kW prototype for example) and is kept constant afterwards. As the battery is getting charged, the voltage increases at the same time and the peak power is reached 400V nominal voltage. The above process is referred as the Constant Current (CC) charging, which should take most of the time in one charging process. After CC charging is finished, the current is reduced gradually to charge the battery to its full capacity. The battery voltage would still increase but much slower

and finally reaches 450V when SoC is 100%. This process is usually referred as Constant Voltage (CV) charging.

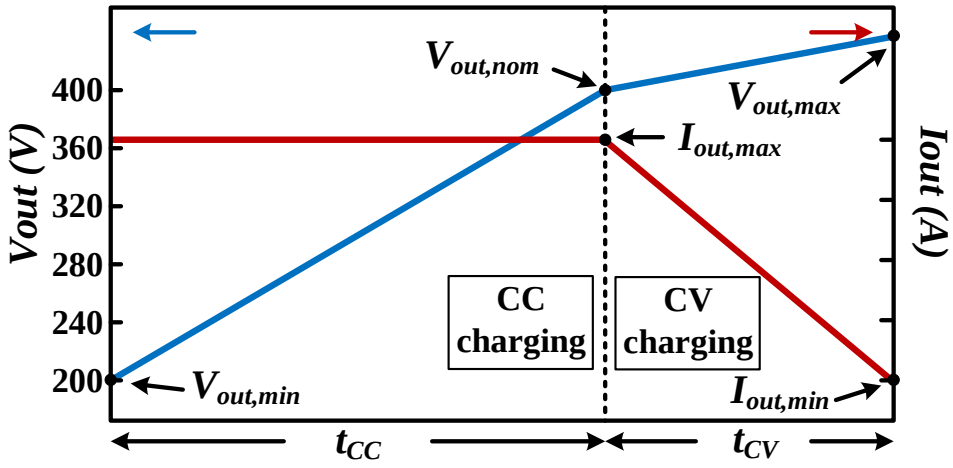

Fig. 3-1. Battery voltage and current values during a complete charging process.

The above mentioned electrical specifications are then listed in Table 3-1. It should be noted that the power level of the DC-DC stage and the PFC stage are closely related, which means the full power operation is guaranteed only if the AC input comes from the level-2 EVSE (240Vrms), otherwise the power level would be reduced due to the current rating of different power components.

Table 3-1. Electrical specifications of the DC-DC stage.

Parameters	Values
DC-link voltage	380V to 420V
Minimum battery voltage	200V
Maximum battery voltage	450V
Nominal battery voltage	400V
Nominal charging power	6.6 kW
Peak charging current	16.5A

There has been many varieties and variations of DC-DC converter topologies over the years. However, due to the requirements of galvanic isolation and bi-directional power flow for the onboard charger application, two types of DC-DC converter topologies are mostly applied in existing products and prototypes: Dual Active Bridge (DAB) converter (Fig. 3-2) and CLLC resonant converter (Fig. 3-3).

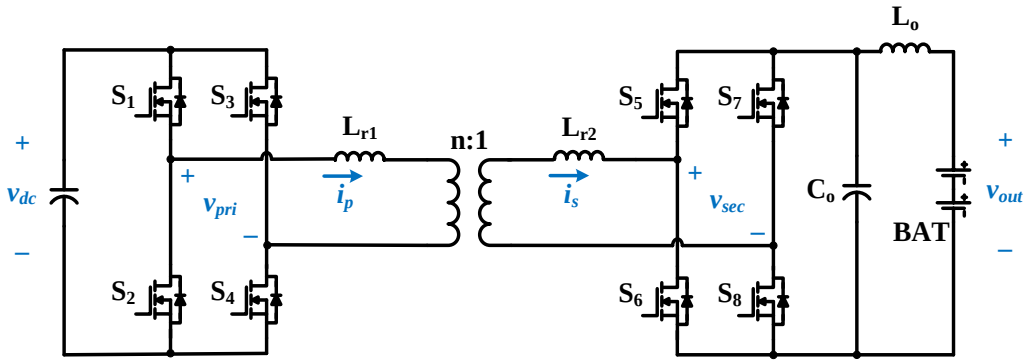

Fig. 3-2. DAB converter topology.

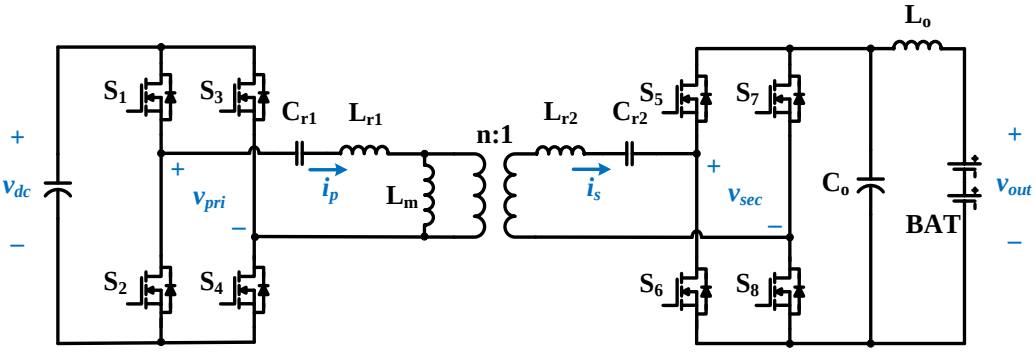

Fig. 3-3. CLLC resonant converter topology.

Both converters can achieve a wide output voltage range, but they are based on different control methods. The DAB converter keeps a constant switching frequency but changes duty ratio of the primary side voltage v_{pri}, while CLLC converter varies the switching frequency but keeps constant 0.5 duty ratio of v_{pri}. As shown in our previous work [60], full bridge CLLC converter has shown more advantages in

achieving higher power density and lower cost. The DAB converter was discarded in that work mainly due to non-ZVS operation at light load conditions. However, with the recent introduction of Triple-Phase-Shift (TPS) control, ZVS can be extended to the full power range [61], [62]. On the other hand, conventional CLLC resonant converter has shown limitations such as higher reactive power at light load conditions, which contributes to higher turning-off losses especially at high switching frequency. Inspired by the phase shift control in DAB converter, a "frequency-phase" ("$f-\varphi$") dual control algorithm is proposed in this work to improve the light load efficiency of CLLC converter. In this chapter, more focus would be put on the conventional CLLC converter design and the proposed control method will be introduced in the next chapter.

3.2 Conventional CLLC Converter with Pulse Frequency Modulation (PFM)

3.2.1 Operation Principles of Conventional CLLC Converter

As depicted in Fig. 3-3, the battery is isolated from the input side by the n:1 high-frequency transformer. In this way, the circuit can be divided into the primary side and the secondary side. On each side there exists a full bridge composed of four switches. The switches on the diagonal of the full bridge, such as S_1 and S_4, would be turned on and off at the same time, and the switches on the same leg, such as S_1 and S_2, would be driven complementarily with a deadband. The components between the two full bridges compose the resonant network. C_{r1} and C_{r2} are referred as the primary side and secondary side resonant capacitors. Likewise, L_{r1} and L_{r2} are referred as the primary side and secondary side resonant inductors, which are implemented by the leakage

inductance of the transformer. In addition, the magnetizing inductance is defined as L_m.

Conventionally, the voltage conversion ratio is controlled by the switching frequency of the primary side switches, while operating the secondary side switches equivalent to a diode rectifier. Under the First Harmonic Approximation (FHA) shown in Fig. 3-4, the equivalent circuit can be depicted in Fig. 3-5. As can be noted, the components in the secondary side are transferred to the primary side. Their expressions can be easily found and shown in Eq. 3-1 and Eq. 3-2.

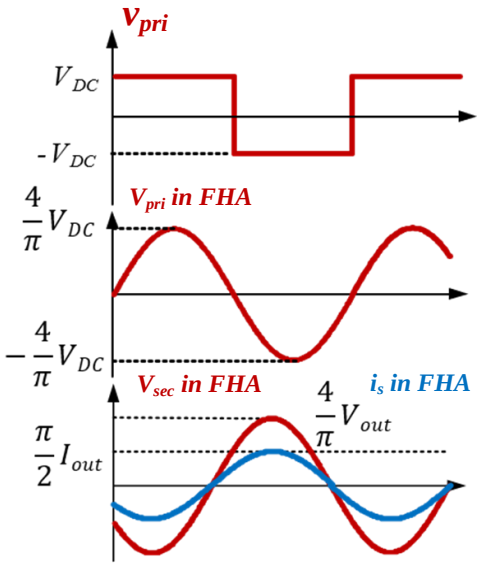

Fig. 3-4. First Harmonic Approximation (FHA) principles.

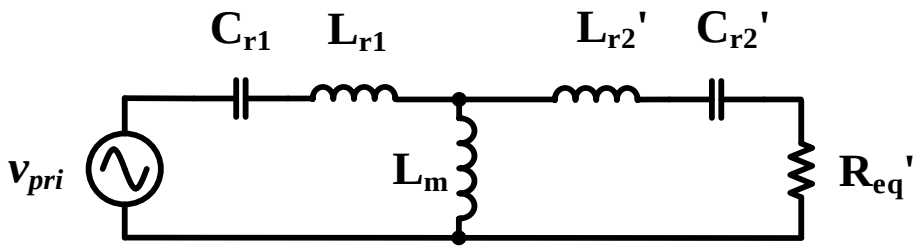

Fig. 3-5. Equivalent circuit of CLLC converter under conventional modulation scheme.

$$L'_{r2} = L_{r2}n^2 \quad \text{Eq. 3-1}$$

$$C'_{r2} = \frac{C_{r2}}{n^2} \quad \text{Eq. 3-2}$$

$$R_{eq}{}' = \frac{\frac{4}{\pi}V_{out}}{\frac{\pi}{2}I_{out}} \cdot n^2 = \frac{8n^2}{\pi^2} \cdot R_{eq} \quad \text{Eq. 3-3}$$

Based on the equivalent model, the voltage gain in the frequency domain could be expressed as

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{1}{n}\frac{R_{eq}{}'}{Z_{in}} = \frac{1}{n}\frac{R_{eq}{}'}{(Z(L'_{r2}) + Z(C'_{r2}) + R'_{eq})//Z(L_m) + Z(C_{r1}) + Z(L_{r1})} \quad \text{Eq. 3-4}$$

where the symbol "//" denotes the impedance of two parallel components.

The expression in Eq. 3-4 contains too many variables, which would be complicated for the designer to determine the parameters. Here, we defined several more coefficients to simplify the equation, which are referred as resonant frequency ω_o, quality factor Q, and the inductance ratio k.

$$\omega_o = \frac{1}{\sqrt{L_{r1}C_{r1}}} \quad \text{Eq. 3-5}$$

$$Q = \frac{\sqrt{\frac{L_{r1}}{C_{r1}}}}{R_{eq}{}'} \quad \text{Eq. 3-6}$$

$$L_m = kL_{r1} \quad \text{Eq. 3-7}$$

Since L_{r1} and L_{r2} are the leakage inductance of the transformer, they inherently have the following relationship $L_{r1} = n^2L_{r2}$. To further simplify the analysis, we assume the resonant capacitors also have a similar relationship: $C_{r1} = \frac{C_{r2}}{n^2}$. Under this

condition, the converted inductance and capacitance values can be written as: $L'_{r2} = n^2 L_{r2} = L_{r1}$, $C'_{r2} = \frac{C_{r2}}{n^2} = C_{r1}$. Thus, the impedance composed by L_{r1}, C_{r1} and L_{r2}', C_{r2}' would be the same: $Z(C_{r1}) + Z(L_{r1}) = Z(L'_{r2}) + Z(C'_{r2})$. The simplified expression of the voltage gain can be then written as:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{1}{n} \cdot \frac{1}{\sqrt{a^2 + b^2}} \quad \text{Eq. 3-8}$$

where

$$a = \frac{1}{k} + 1 - \frac{1}{k\omega_n^2} \quad \text{Eq. 3-9}$$

$$b = 2\left(\frac{1}{k} + 1\right) \cdot \frac{Q}{\omega_n} - \left(\frac{1}{k} + 2\right) Q\omega_n - \frac{Q}{k\omega_n^2} \quad \text{Eq. 3-10}$$

$$\omega_n = \frac{\omega_s}{\omega_o} \quad \text{Eq. 3-11}$$

The voltage gain expression contains two information: amplitude and phase. The amplitude represents the actual output voltage value over the input voltage, which can be used to derive the gain curve and determine the switching frequency at different load conditions. Unlike uni-directional topology where diode rectifier is applied at the secondary side, the turn-on time of the secondary switches have to be manually controlled. The phase of the voltage gain also represents the phase difference of the driving signal between the primary and secondary switches. For example, if $k = 5$, $n = 1$, $\omega_o = 1MHz \times 2\pi$, the gain curves at different load conditions can be depicted as Fig. 3-6. Based on the charging profile, at different time during the CC region, the operation points can be marked in the figure as well. The blue triangles correspond to the operation points at the minimum input voltage (380V), and the red squares correspond to the operation points at the maximum input voltage (420V). At the same

frequency, the phase angle of the resonant tank impedance can be also marked in Fig. 3-7. Several conclusions can be drawn from the figures: 1. At low battery voltages, the switching frequency would be higher than the case in high battery voltages. 2. Lower switching frequency leads to smaller phase angle, which also corresponds to higher power level. 3. The phase angle should be kept positive and higher than a minimum value to ensure ZVS property.

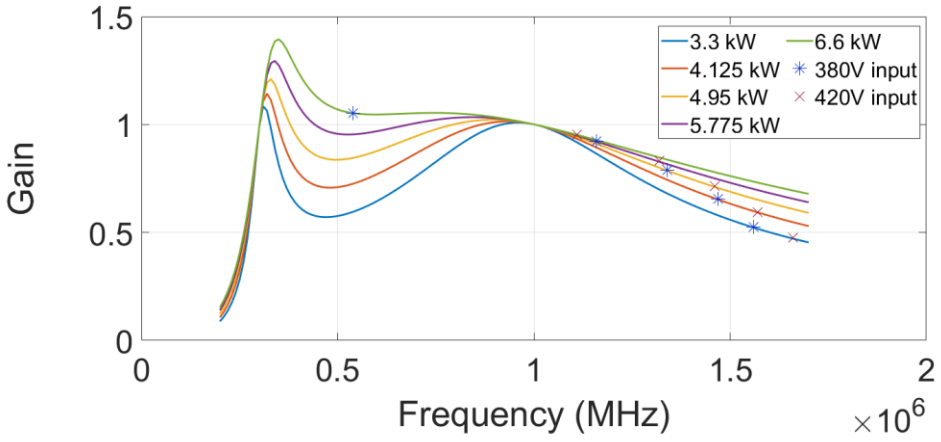

Fig. 3-6. Gain curves with the operation points.

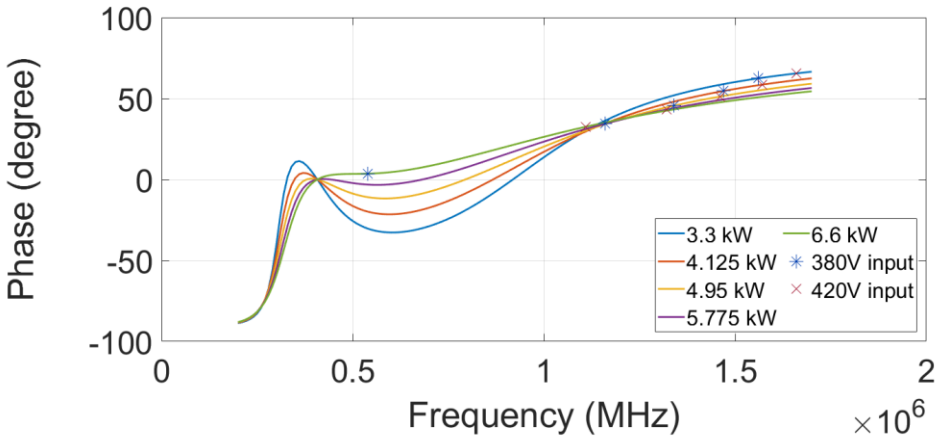

Fig. 3-7. Resonant network input impedance phase.

In resonant converters, the phase angle of the tank impedance carries much information. By using FHA method, the input voltage and current could be expressed in phasor diagram, shown in Fig. 3-8.

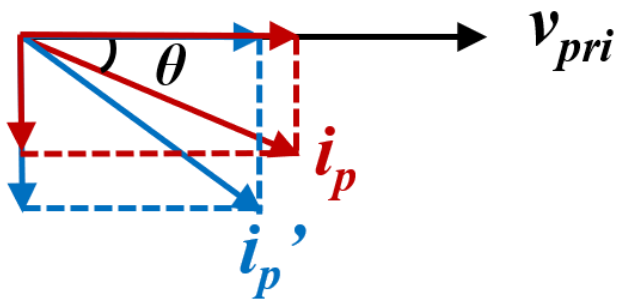

Fig. 3-8. Phasor diagram to model the phase angle.

The lagging current i_p has a phase difference of θ ($\theta < 0$) compared with the primary side voltage v_{pri}. Assume the projected current of i_p on the real axis is i_{px} and on the imaginary axis is i_{py}. The real power and reactive power can be expressed as:

$$P_{real} = i_{px} \cdot v_{pri} = i_p \cdot v_{pri} \cdot cos\theta \quad \text{Eq. 3-12}$$

$$P_{reactive} = i_{py} \cdot v_{pri} = i_p \cdot v_{pri} \cdot sin\theta \quad \text{Eq. 3-13}$$

The real power is the actual power received by the load, which could be found out from the battery charging profile. The reactive power doesn't help with the power transmission, but it is useful to maintain ZVS at full power range. As can be seen from Fig. 3-8, when the power level is lower (represented by the blue arrows), the projected current on the real axis would be reduced. According to Fig. 3-7, the phase angle would be increased at lighter loads, which could lead to larger projected current on the imaginary axis and larger reactive power. However, too much reactive power could

lead to a large primary side current stress since $i_p = \sqrt{i_{px}^2 + i_{py}^2}$. Also, it is directly related with the switch turning-off losses, where

$$P_{off} \propto V_{dc} \cdot |i_{py}| \cdot f_{sw} \quad \text{Eq. 3-14}$$

As shown in [60], switching losses would be the dominant loss in MHz converter, thus controlling the reactive power to be just enough for the ZVS is a better solution to improve the efficiency.

3.2.2 Limitations of Conventional CLLC Converter

As shown before, the switching frequency of S_1 to S_4 (known as primary switches) are controlled actively by Pulse Frequency Modulation (PFM) to regulate the output charging current I_o, while S_5 to S_8 (known as secondary switches) are controlled as equivalent to a full-bridge diode rectifier. The diode-like operation of the secondary switches can be simply achieved by keeping them in "OFF" states and utilizing their intrinsic body diodes to conduct the current. However, due to the high and almost constant voltage drop (~1.4V) across the body diode, it would generate really high conduction loss and decrease the energy conversion efficiency on a large scale. Another similar solution is to connect fast Schottky diodes in parallel to the secondary switches to reduce the voltage drop to ~0.7V and improve the reverse recovery behaviors [63], but it would increase the overall output capacitance between the drain and source, which degrades the switching performance. It also increases the size and cost of the overall system. As an alternative solution, this problem could be alleviated by introducing synchronous rectification (SR) control [64], [65]. However, there is no commercially available SR chip that works at the battery voltage level (200V to 450V).

Although analog sensing circuits could be utilized to detect the zero-crossing moments of the voltage, phase synchronization errors are usually inevitable due to the limited sampling frequency and the inheritably added turn-on delays (to tolerant the voltage oscillation during switching) [66].

In another approach, the switching time of the secondary switches can be estimated using approximation methods [66]–[69]. FHA method was firstly applied to model the converter and calculate the phase difference, where only the first order harmonic components of voltage and current are analyzed [63], [67]. The converter can be simplified to a resonant network with a sinusoidal voltage excitation, as shown in Fig. 2 from [67]. However, FHA method is only accurate if the switching frequency is near the resonant tank frequency ($f_o = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}}$), which is usually not the case considering a wide output range from the battery charging profile (shown in Fig. 3-1). It was later refined by the Extended Harmonic Approximation (EHA) method [66], [69], where higher harmonics are also included in the model to improve the estimation accuracy. Nevertheless, the model established in [66] relies on the assumption that the load equivalent resistance is identical at different harmonic orders, which over-simplifies the problem and its accuracy relies much on the selection of converter parameters. A more generalized model is proposed in [69], but it is only shown for a fixed-frequency control and its accuracy is not validated by either simulation or experiments. In reality, PFM control would lead to varying impedance values of the resonant components and add more complexity to the EHA model. Currently there is no effective solution proposed to address the issue, which is one of the contributions of this work.

Various limitations of CLLC converter itself with PFM control have also been reported. Firstly, the gain variation at higher switching frequencies is usually much slower than points near the resonant frequency. It means that the converter needs to sweep the frequency on a large range at the beginning of the charging process, in which case the design of the EMI filter and the transformer is much more complicated. Secondly, larger reactive power at lighter load conditions is usually unavoidable. It is due to the increase of the input impedance phase angle at higher switching frequencies. It should be noted that a good amount of reactive power could help with the soft-switching behavior, but excessive reactive power results in higher current stress on the components and thus generate more power losses. In reality, the converter works at light load for the most of time, thus increasing light load efficiency is crucial to improve the overall energy loss and also would reduce the complexity of the thermal solution. Currently, there are two major trends to solve the aforementioned problems, which are discussed as below.

a. Maximum Efficiency Tracking Method

"Maximum Efficiency Tracking" or "Variable DC-link Control" was widely applied in various CLLC prototypes [70]–[72]. In this control algorithm, the DC-link voltage (which is also the input voltage to the DC-DC converter) is controlled by the front-end PFC rectifier to accommodate the gain requirement and the switching frequency of the CLLC converter is varied in a small range only to compensate the double line frequency ripples across the DC-link. However, due to the wide changing range of the DC-link voltage (500V to 840V in [72]), the primary side switches should have a larger breakdown voltage ratings, such as 1.2 kV of SiC MOSFETs. Thus, the

application is restricted to specific series of the devices. The emerging 650V GaN devices with even lower on-resistance and higher operation frequency could not fit in with this control scheme. In addition, the large variation on the DC-link voltage could also deviate the PFC stage from the optimal operation point and the overall efficiency of the system would be decreased as a consequence.

b. Dual-Variable Control Method

Another series of solution utilizes an additional control variable into the resonant converters, such as phase shift [73] and duty ratio [74]–[76], to help narrow the frequency range and improve the soft-switching performance. However, additional circuit components need to be added to either primary or secondary side. For uni-directional circuit topologies, such as LLC converter with a diode bridge on the secondary side, it is acceptable to some extent, but it would not be appropriate for bi-directional topology such as CLLC converter, since the same copy of components need to be added to both sides, which adds too much complexity or even disables normal operation. On the other hand, the term “Dual-Variable” usually means different variable joins the control algorithm at different working conditions, such as light and heavy loads. In each condition, there is only one control variable that is actually being tuned, which does not fully discover the potential of using dual-variable control.

3.3 Extended Harmonic Approximation (EHA) modelling

3.3.1 Equivalent Circuit Model and Phasor Diagram of currents and voltages

EHA modelling is based on the theory of Fourier Series Expansion, that a square shape voltage can be divided into various harmonic components, as shown in Eq. 3-15 and Eq. 3-16.

$$v_p = \frac{4}{\pi} V_i \sum_{k=1,3,5\ldots} \frac{1}{k} \sin(k\omega t) = \sum_{k=1,3,5\ldots} v_{p,k} \qquad \text{Eq. 3-15}$$

$$v_s = \frac{4}{\pi} V_o \sum_{k=1,3,5\ldots} \frac{1}{k} \sin[k(\omega t + \varphi)] = \sum_{k=1,3,5\ldots} v_{s,k} \qquad \text{Eq. 3-16}$$

Here, k denotes the harmonic order and ω represents the switching frequency in rad/s ($\omega = 2\pi f$). The k_{th} harmonic component of v_p and v_s is represented by $v_{p,k}$ and $v_{s,k}$, respectively. At the k_{th} harmonic order, the converter topology could be further simplified to the circuit shown in Eq. 3-9.

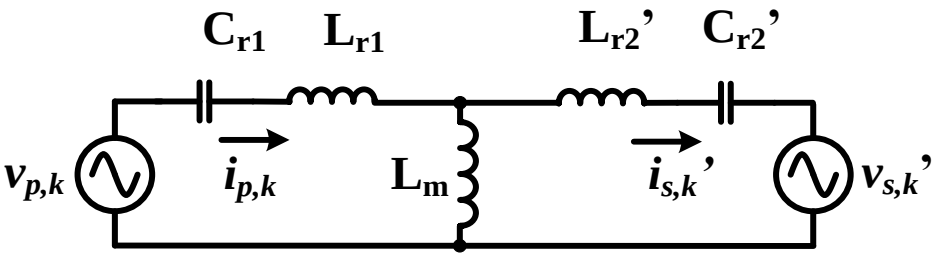

Fig. 3-9. Equivalent circuit of the CLLC converter based on EHA modelling.

The transformer is removed for clearer demonstration and the secondary side components can be transferred to the primary side with the conversion ratio of n^2: ${L_{r2}}' = L_{r2} \cdot n^2$ and ${C_{r2}}' = C_{r2}/n^2$. The current and voltage at the secondary side would also been converted to ${i_{s,k}}' = i_{s,k}/n$ and ${v_{s,k}}' = n \cdot v_{s,k}$. In the following analysis, we assume the impedance composed by L_{r1} and C_{r1} and the impedance

composed by $L_{r2}{}'$ and $C_{r2}{}'$ are the same for simplicity, so that $Z(L_{r1}) + Z(C_{r1}) = Z(L_{r2}{}') + Z(C_{r2}{}')$. Definitions of other relative coefficients are listed in Table 3-2.

Table 3-2. Definition of coefficients.

Coefficients	Definition
$Z_{LC} = Z(L_{r1}) + Z(C_{r1}) = j\omega L_{r1} + \frac{1}{j\omega C_{r1}}$	Impedance of the LC resonant tank
$Z(L_m) = j\omega L_m$	Impedance of the magnetizing inductance
$m = \frac{L_m}{L_{r1}}$	Inductance ratio
$\omega_o = \frac{1}{\sqrt{L_{r1}C_{r1}}}$	Resonant frequency in rad/s

In order to better demonstrate the relationship of different variables, $v_{p,k}$ and $v_{s,k}{}'$ are expressed in the form of vectors: $\hat{v}_{p,k} = \frac{4V_i}{k\pi}$ and $\hat{v}_{s,k}{}' = \frac{4nV_o}{k\pi}[\cos(k\varphi) + jsin(k\varphi)]$. $\hat{\imath}_{p,k}$ and $\hat{\imath}_{s,k}{}'$ can be found by applying superposition to both voltage excitations, which are shown as follows.

$$\hat{\imath}_{p,k} = \frac{\hat{v}_{p,k}}{Z_{LC}//Z(L_m) + Z_{LC}} - \frac{\hat{v}_{s,k}{}'}{Z_{LC}//Z(L_m) + Z_{LC}} \cdot \frac{Z(L_m)}{Z(L_m) + Z_{LC}} \quad \text{Eq. 3-17}$$

$$\hat{\imath}_{s,k}{}' = -\left(\frac{\hat{v}_{s,k}{}'}{Z_{LC}//Z(L_m) + Z_{LC}} - \frac{\hat{v}_{p,k}}{Z_{LC}//Z(L_m) + Z_{LC}} \cdot \frac{Z(L_m)}{Z(L_m) + Z_{LC}}\right) \quad \text{Eq. 3-18}$$

Next, both current vectors $\hat{\imath}_{p,k}$ and $\hat{\imath}_{s,k}{}'$ together with $\hat{v}_{p,k}$ and $\hat{v}_{s,k}{}'$ can be drawn in a phasor diagram shown in Fig. 3-10.

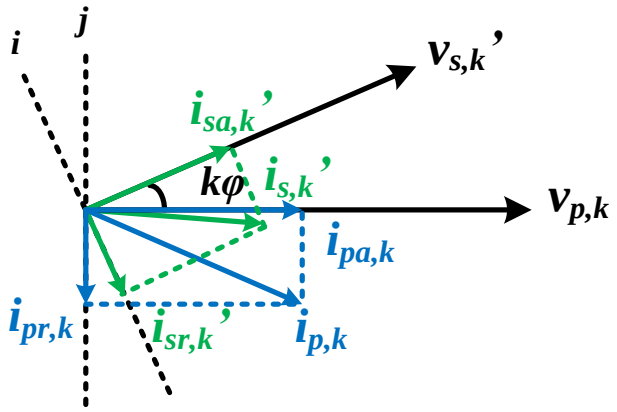

Fig. 3-10. Phasor diagram of selected voltages and currents on both sides of the converter.

It should be noted that the position of the vector corresponds to $t = 0$ and the projection of the vector on the "*j*" axis represents the voltage or current value directly measured from the circuit. During the operation, the vectors would be rotating counter-clockwise at an angle-frequency of $k\omega$. Each current vector is divided into two orthogonal components, with one aligned on the voltage vector from the same side and the other on the perpendicular direction ("*j*" axis for the primary side and "*i*" axis for the secondary side). The subscript "a" and "r" stand for "active" and "reactive", since they contribute to the active and reactive power flow in the system. Based on Eq. 3-17 and Eq. 3-18, active and reactive currents can be calculated, as shown in Eq. 3-19 to Eq. 3-22.

$$\hat{\imath}_{pa,k} = \frac{-4mnV_o}{L_{r1}\pi} \cdot \frac{\omega \sin(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 3-19}$$

$$\hat{\imath}_{pr,k} = j \cdot \frac{-4}{L_{r1}\pi} \cdot \frac{\frac{V_i}{k^2\omega}[(m+1)k^2\omega^2 - \omega_o^2] - \omega mnV_o\cos(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 3-20}$$

$$\hat{\imath}_{sa,k}{}' = -\frac{4mV_i}{L_{r1}\pi} \cdot \frac{\omega \sin(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 3-21}$$

$$\hat{\imath}_{sr,k}{}' = i \cdot \frac{-4}{L_{r1}\pi} \cdot \frac{\frac{nV_o}{k^2\omega}[(m+1)k^2\omega^2 - \omega_o^2] - \omega m V_i \cos(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 3-22}$$

The total active power P_{active} measured from the primary side can be found by calculating the average value of $v_p \cdot i_p$ in one switching period (T), which could be expressed by different harmonic components

$$P_{active} = \frac{1}{T}\int_T \left[\sum_{1,3,5\ldots} \left(|\hat{v}_{p,k}|\sin(k\omega t)\right)\right] \cdot \left[\sum_{1,3,5\ldots} \left(|\hat{\imath}_{p,k}|\sin(k\omega t + angle(\hat{\imath}_{p,k}))\right)\right] dt \quad \text{Eq. 3-23}$$

Here, $angle(\hat{\imath}_{p,k}) = \arctan(-\frac{|\hat{\imath}_{pa,k}|}{|\hat{\imath}_{pr,k}|})$ represents the phase difference between $\hat{v}_{p,k}$ and $\hat{\imath}_{p,k}$. Since the integration of two sine functions at different frequencies over one fundamental period is zero, only the product of voltage and current at the same frequency would result in non-zero values. Thus Eq. 3-23 can be further simplified as

$$P_{active} = \frac{1}{T}\int_T \left[\sum_{1,3,5\ldots} \left(|\hat{v}_{p,k}|\sin(k\omega t)\right) \cdot \left(|\hat{\imath}_{p,k}|\sin(k\omega t + angle(\hat{\imath}_{p,k}))\right)\right] dt \quad \text{Eq. 3-24}$$

With the definition of $\hat{\imath}_{pa,k}$, it could be expressed as

$$P_{active} = 0.5 \sum_{k=1,3,5\ldots} \left|\hat{v}_{p,k}\right| \cdot \left|\hat{\imath}_{pa,k}\right|$$

$$= \frac{8V_i V_o mn}{L_{r1}\pi^2} \sum_{k=1,3,5\ldots} \frac{\omega \cdot \sin(k\varphi)}{k(\omega_o^2 - k^2\omega^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 3-25}$$

Assuming 100% power conversion efficiency, the active power would be equal to the power measured from the load (P_o).

$$P_{active} = P_o = V_o I_o \quad \text{Eq. 3-26}$$

Combining Eq. 3-25 and Eq. 3-26, the relationship between the switching frequency ω and the phase shift φ can be formulated as

$$\sum_{k=1,3,5\ldots} \frac{\omega \cdot \sin(k\varphi)}{k(\omega_o^2 - k^2\omega^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} = \frac{I_o L_{r1}\pi^2}{8V_i mn} \quad \text{Eq. 3-27}$$

Since i_s has the same phase as v_s in SR, they would cross zero values at the same moments. It will be shown later in Section III that the summation of all the reactive current components ($\hat{\imath}_{sr,k}{}'$) represents the current value during the zero-crossing of $v_s{}'$. Thus the following equation can be formulated

$$\sum_{k=1,3,5\ldots} \hat{\imath}_{sr,k}{}' = \sum_{k=1,3,5\ldots} i \cdot \frac{-4}{L_{r1}\pi}$$

$$\cdot \frac{\frac{nV_o}{k^2\omega}[(m+1)k^2\omega^2 - \omega_o^2] - \omega m V_i \cos(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} = 0 \quad \text{Eq. 3-28}$$

Eq. 3-28 can be further simplified as

$$\sum_{k=1,3,5\ldots} \frac{\frac{nV_o}{k^2\omega}[(m+1)k^2\omega^2 - \omega_o^2] - \omega m V_i \cos(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} = 0 \quad \text{Eq. 3-29}$$

3.3.2 Numerical Method to Estimate the Phase Difference

Here, Eq. 3-27 and Eq. 3-29 are two important equations to determine the value of the switching frequency ω and the phase difference φ at a certain output voltage V_o. It should be noted that a closed-form expressions of ω and φ cannot been found, and the calculation should be conducted in a numerical way, which is shown by a flow diagram in Fig. 3-11.

To start with, suppose the component values of the converter are already determined, the mapping of the switching frequency and the phase difference will firstly be calculated by Eq. 3-27. Note that there is no output voltage variable V_o in Eq. 3-27, it can be solved by sweeping various values of switching frequency and phase difference in two "for" loops, and those pairs of (ω, φ) which satisfy the equation are left and stored. The final results can be depicted in Fig. 3-12.

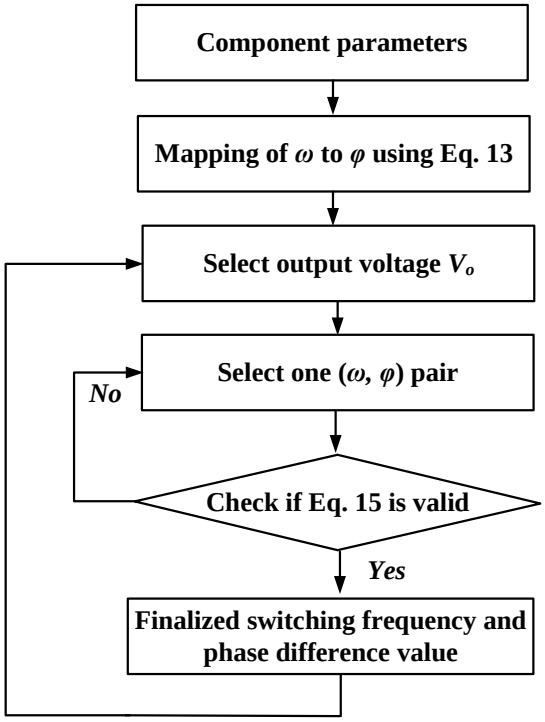

Fig. 3-11. Numerical method to estimate switching frequency and phase difference at different output voltages based on the EHA model.

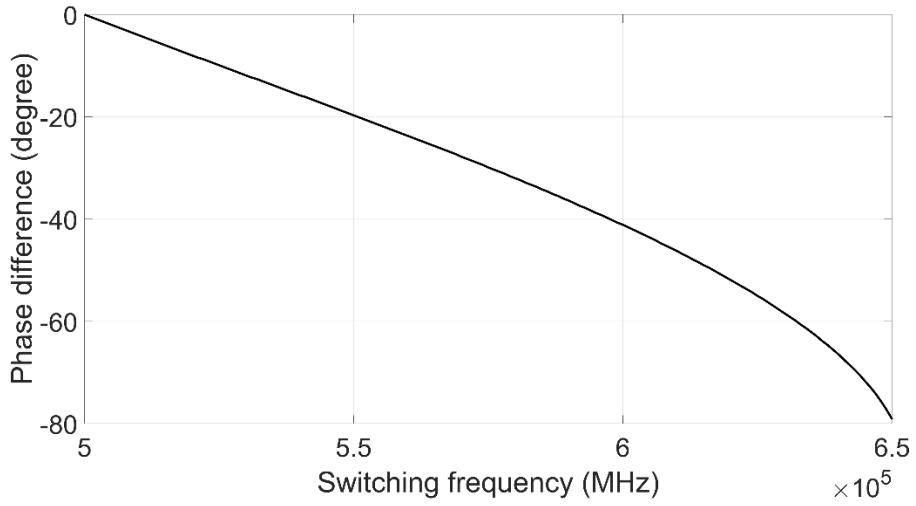

Fig. 3-12. Relationship between phase difference and switching. ($n = 0.84$, $L_{r1} = 4.7\mu H$, $C_{r1} = 21.6nF$, $L_{r2} = 6.6\mu H$, $C_{r1} = 15.3nF$, $L_m = 37.6\mu H$)

Although the relationship of ω and φ is found, the exact switching frequency at a specific output voltage condition is still not known. In the next step, all the selected

pairs of (ω, φ) are taken into Eq. 3-29 to find the unique value of ω and φ at different output voltages. The voltage values are taken from the CC region and the results are shown in Fig. 3-13 and Fig. 3-14, respectively. To solve Eq. 3-27 and Eq. 3-29, the highest harmonic order is chosen to be 21, which guarantees enough accuracy within reasonable computation time.

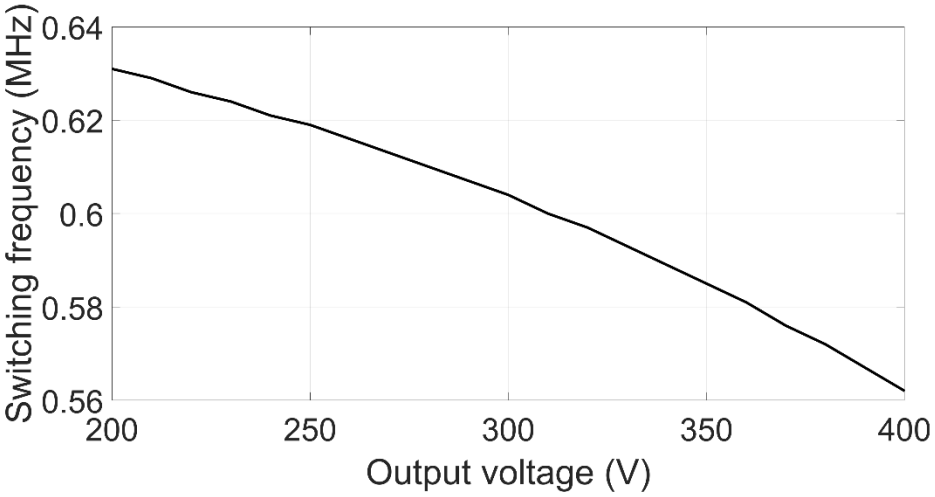

Fig. 3-13. Switching frequencies (in MHz) at different output voltages.

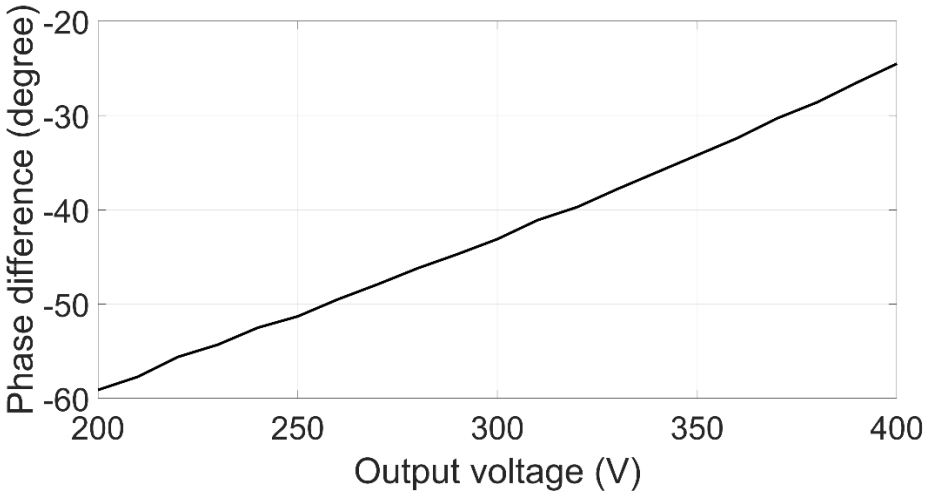

Fig. 3-14. Phase difference values (in degree) at different output voltages.

As can be seen, the switching frequency decreases at higher output voltages, and v_s would also be less lagging than v_p. The accuracy of the above EHA modelling can be proved by simulation, where exact phase differences of the diode bridge are measured and shown in Fig. 3-15.

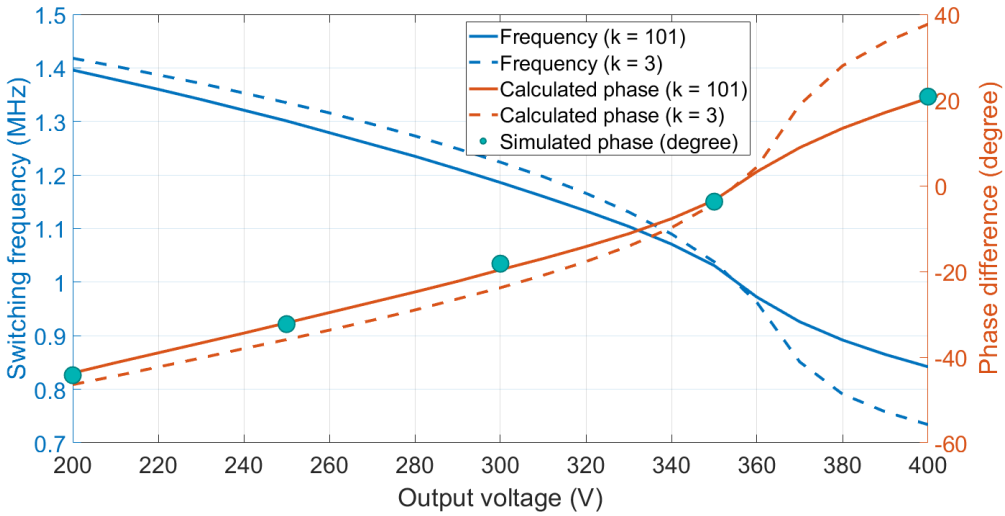

Fig. 3-15. Estimated and simulated phase difference values.

As can be noticed, the estimated phase difference values are really close to the simulated results (less than 1°), which shows even higher estimation accuracy than the results reported in [66]. Based on the proposed model, the current harmonic components could also be found, and reactive power could be analyzed afterwards.

3.3.3 Reactive Power and Power Losses

In this section, the relationship of reactive power and the power losses are analyzed based on the EHA model introduced before, and the increase of power losses at lighter loads (also lower output voltages in CC region) is demonstrated. Active power is not considered here since it is preset by the battery charging profile and is not dependent on the component parameters, thus the associated power losses are fixed and not

controllable. On the other hand, reactive power and its associate power losses are sensitive to the component parameters and the control method. Based on the loss breakdown shown in [77], two main power losses are analyzed: turning-off loss of switches and extra conduction loss.

a. Turning-off loss

Although the primary side switches could achieve ZVS during turning-on time, the turn-off behavior is still hard switching. As can be seen from Fig. 3-16, the turning-off current is equal to the summation of all the reactive current harmonics, which is defined as i_{pr}.

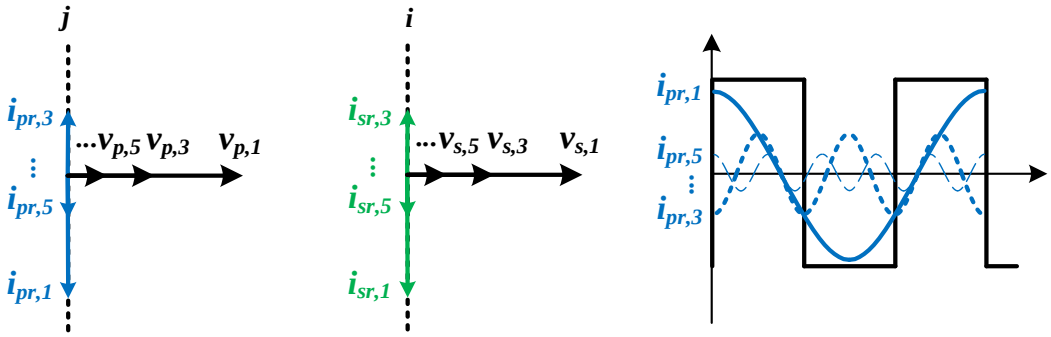

Fig. 3-16. Turning-off current and reactive current components.

$$i_{pr} = \sum_{k=1,3,5\ldots} \hat{i}_{pr,k}$$

$$= \sum_{k=1,3,5\ldots} \frac{-4}{L_{r1}\pi} \cdot \frac{\frac{V_i}{k^2\omega}[(m+1)k^2\omega^2 - \omega_o^2] - \omega mnV_o\cos(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m+1-\frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 3-30}$$

Thus, the turning-off losses of four switches could be expressed as follows.

$$P_{off} = -4 \cdot \frac{V_i i_{pr}}{2} t_{off} f \quad \text{Eq. 3-31}$$

where t_{off} denotes the turn-off time of the switches. Since i_{pr} has a negative value due to the lagging current effect, there is a negative sign in the front to convert into positive power loss value.

b. Extra conduction loss

The conduction losses contributed by $i_{pa,k}$ and $i_{sa,k}$ are dependent on the active power, and their values would not be affected by the control method. Thus, the contribution of $i_{pr,k}$ and $i_{sr,k}$ to the conduction loss is referred as "extra conduction loss", which can be expressed as

$$P_{con,extra} = \frac{1}{T}\int_T \left(\sum_{k=1,3,5\ldots} \left|\hat{i}_{pr,k}\right| \cos(k\omega t) \right)^2 dt \cdot (2R_{on} + R_{pri}) + \frac{1}{T}\int_T \left(\sum_{k=1,3,5\ldots} \left|\hat{i}_{sr,k}\right| \cos(k\omega t) \right)^2 dt \cdot (2R_{on} + R_{sec}) \quad \text{Eq. 3-32}$$

Since the integration of the multiple of two cosine functions at different frequencies over the fundamental period is zero, the expression could be simplified as

$$P_{con,extra} = \frac{1}{T}\int_T \sum_{k=1,3,5\ldots} \left(\left|\hat{i}_{pr,k}\right| \cos(k\omega t)\right)^2 dt \cdot (2R_{on} + R_{pri}) + \frac{1}{T}\int_T \sum_{k=1,3,5\ldots} \left(\left|\hat{i}_{sr,k}\right| \cos(k\omega t)\right)^2 dt \cdot (2R_{on} + R_{sec}) \quad \text{Eq. 3-33}$$

Based on the RMS current expression, the final result is shown as follows

$$P_{con,extra} = \frac{2R_{on} + R_{pri}}{2} \sum_{k=1,3,5\ldots} \left|\hat{i}_{pr,k}\right|^2 + \frac{2R_{on} + R_{sec}}{2} \sum_{k=1,3,5\ldots} \left|\hat{i}_{sr,k}\right|^2 \quad \text{Eq. 3-34}$$

where R_{on} denotes the on-resistance of the switch and R_{pri}, R_{sec} represent the transformer primary and secondary side winding AC resistance. Suppose $R_{pri} = 100m\Omega$, $R_{sec} = 100m\Omega$, $R_{on} = 50m\Omega$ and $t_{off} = 5ns$, the two power losses can be calculated based on the aforementioned EHA model, as shown in Fig. 3-17. As can been seen, the power losses at lighter loads (or lower output voltages) are higher than heavier loads, and the efficiencies would also drop significantly at the same time.

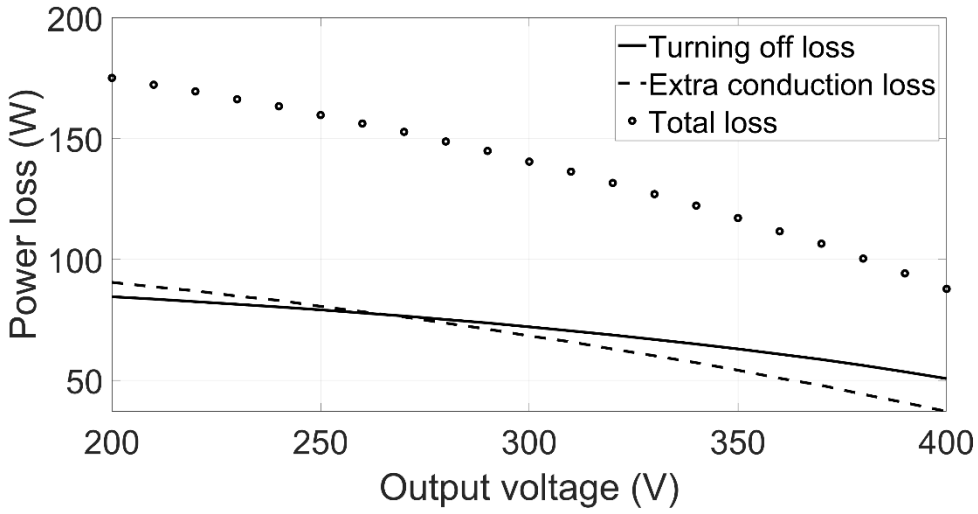

Fig. 3-17. Power loss estimation for a 6.6kW CLLC converter based on the EHA model.

Chapter 4: “ $f-\varphi$ ” Control and Optimization for CLLC Converter

4.1 Introduction

In this section, a novel “$f-\varphi$” control method is proposed to limit the reactive power at light loads and improve the overall power conversion efficiency. In PFM control, once the component parameters are determined, the switching frequency at specific output voltage is also fixed. In “$f-\varphi$”, the phase difference of the secondary bridge is not controlled in SR scheme anymore but acts as an additional control variable. With the flexibility to select φ, switching frequency can be located literally in any range, as long as the pair of (f,φ) outputs the required active power. This enlarges the room for parameter optimization and also helps with the reactive power management. Several key contributions of this chapter are listed as below.

1. A generalized EHA modelling of the CLLC converter is presented, which is validated by simulation and has shown higher accuracy in terms of current stress, switching frequency, and phase shift values than other proposed analysis models. The relationship between the “reactive current” and the power loss is clarified for the first time.

2. Based on the proposed EHA model, the relationship between the switching frequency and the phase shift is analyzed at different load conditions. With the additional control variable, frequency range is no longer restricted by the converter parameters and the operation conditions but could be initiated by designers with more

flexibility. The mapping from frequency to voltage gain could also become linear, which simplifies the controller on a large scale.

3. Based on the loss model, a numerical approach is proposed to optimize the component parameters and the frequency range to ensure ZVS operation for all the switches and also reduce the current stress over the entire charging process. Comparison of the optimized results with the conventional CLLC converter is presented to demonstrate much lower power losses at lighter load conditions and relatively same power losses at heavy load conditions.

4.2 Proposed "$f-\varphi$" Modulation Scheme

4.2.1 "$f-\varphi$" modulation principles

To find the mapping of f and φ, similar numerical method based on Eq. 3-27 introduced before could be applied. However, since switching frequency is selected manually, conducting the numerical process would be impractical for each frequency range. Thus, proper approximation should be applied for simple implementation. Firstly, several key assumptions are made in the first place:

(1) Switching frequency ω is selected less than the resonant frequency ω_o, so that the size of resonant components could be smaller within the same frequency range of the PFM scheme.

(2) The inductance ratio m is larger than 5.

(3) The switching frequency is assumed to be linearly changing (increasing or decreasing) with the output voltage.

In Eq. 3-27, the following approximation could be assumed: $2m+1-\frac{\omega_o^2}{k^2\omega^2} \approx 2m+1$ and $k^2\omega^2-\omega_o^2 \approx k^2\omega^2$ for $k \geq 3$. Thus, the active power can be expressed as the summation of the first harmonic component and the rest approximated higher order components.

$$P_{active} \approx \frac{8V_iV_omn}{L_{r1}\pi^2}\left[\frac{\omega\cdot\sin\varphi}{(\omega_o^2-\omega^2)(2m+1-\frac{\omega_o^2}{\omega^2})} - \frac{1}{(2m+1)\omega}\sum_{k=3,5\ldots}\frac{\sin(k\varphi)}{k^3}\right] \quad \text{Eq. 4-1}$$

Here we define the amount of power contributed by the first harmonic is $P_1 = \frac{8V_iV_on}{L_{r1}\pi^2}\cdot\frac{m}{2m+1-\frac{\omega_o^2}{\omega^2}}\cdot\frac{\omega\cdot\sin\varphi}{\omega_0^2-\omega^2}$, and the amount of power contributed by higher harmonics is $P_{3,5\ldots} = -\frac{8V_iV_omn}{L_{r1}\pi^2(2m+1)\omega}\cdot\sum_{k=3,5\ldots}\frac{\sin(k\varphi)}{k^3}$. Based on the initial assumption of $\omega > \frac{1}{\sqrt{2}}\omega_o$, we have $\frac{\omega}{\omega_0^2-\omega^2} > \frac{1}{\omega}$. Thus,

$$P_1 > \frac{8V_iV_on}{L_{r1}\pi^2}\cdot\frac{m}{2m}\cdot\frac{\sin\varphi}{\omega} > -\frac{8V_iV_omn}{L_{r1}\pi^2(2m+1)\omega}\cdot\sin\varphi \quad \text{Eq. 4-2}$$

Next, we will prove that the active power is mostly contributed by the first harmonic component by comparing the value of $\sin\varphi$ and $\sum_{k=3,5\ldots}\frac{\sin(k\varphi)}{k^3}$. The value of $\frac{\sin(k\varphi)}{k^3}$ at different values of k is shown in Fig. 4-1, and $\sin\varphi$ especially corresponds to the case of $k=1$.

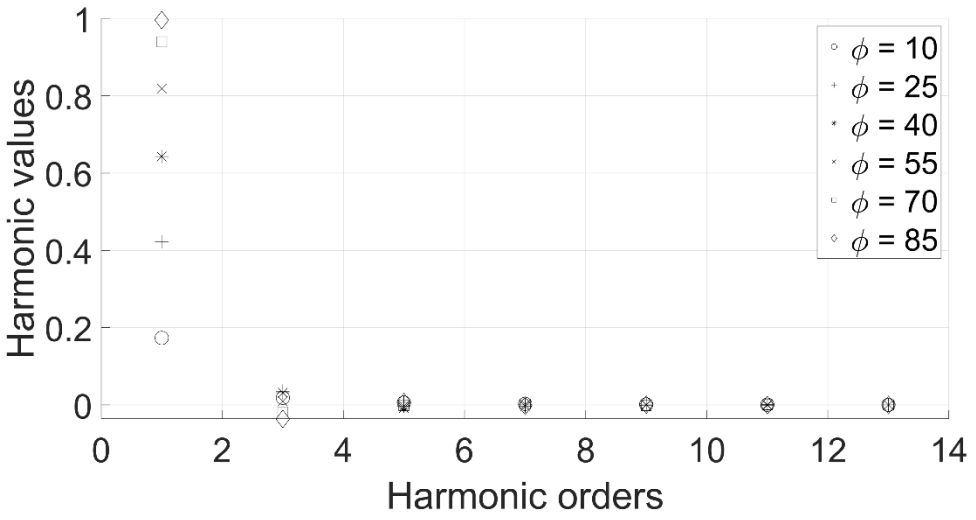

Fig. 4-1. Different harmonic values of $\frac{\sin(k\varphi)}{k^3}$.

As can be seen, for $\varphi > 25°$, first harmonic values would be at least x10 times larger than the other harmonic total. Thus, the active power could be regarded to be contributed by only the first harmonic component, which is expressed by

$$P_{active} \approx P_1 \text{ if } \varphi > 25° \qquad \text{Eq. 4-3}$$

Using the assumption shown in Eq. 3-26, the relationship between frequency and phase shift can be simply formulated as

$$\sin\varphi \approx \frac{I_o L_{r1} \pi^2}{8 V_i m n} \cdot \frac{(\omega_o^2 - \omega^2)(2m + 1 - \frac{\omega_o^2}{\omega^2})}{\omega} \qquad \text{Eq. 4-4}$$

which does not rely on numerical computation.

4.2.2 Power loss analysis for "$f - \varphi$" control

Based on Section III, reactive current components are firstly calculated and summed up for both primary and secondary side.

$$i_{pr} = \sum_{k=1,3,5\ldots} \frac{-4}{L_{r1}\pi} \cdot \frac{\frac{V_i}{k^2\omega}[(m+1)k^2\omega^2 - \omega_o^2] - \omega m n V_o \cos(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 4-5}$$

$$i_{sr} = \sum_{k=1,3,5\ldots} \frac{-4}{L_{r1}\pi} \cdot \frac{\frac{nV_o}{k^2\omega}[(m+1)k^2\omega^2 - \omega_o^2] - \omega m V_i \cos(k\varphi)}{(k^2\omega^2 - \omega_o^2)(2m + 1 - \frac{\omega_o^2}{k^2\omega^2})} \quad \text{Eq. 4-6}$$

Since the secondary side switches are not controlled in SR, they could lose the soft-switching property. When selecting the optimal converter components and the switching frequency range, the following constraint needs to be maintained to ensure ZVS for both sides

$$i_{pr} < 0, i_{sr} < 0 \quad \text{Eq. 4-7}$$

However, the secondary side switches would lose the ZCS property and thus the addition turning-off loss should be taken into account.

$$P_{off} = -4 \cdot (\frac{V_i i_{pr}}{2} + \frac{V_o i_{sr}}{2}) t_{off} f \quad \text{Eq. 4-8}$$

Likewise, the extra conduction losses could be expressed as follows.

$$P_{extra,con} = \frac{2R_{on} + R_{pri}}{2} \sum_{k=1,3,5\ldots} \left|\hat{i}_{pr,k}\right|^2 + \frac{2R_{on} + R_{sec}}{2} \sum_{k=1,3,5\ldots} \left|\hat{i}_{sr,k}\right|^2 \quad \text{Eq. 4-9}$$

The power loss value is the key criteria to find the optimized component parameters and the switching frequency range, which will be introduced in the next section.

4.2.3 Optimization methods

In "$f - \varphi$" modulation, different selection of switching frequency would lead to different loss values, and thus an optimized frequency range should be found out. Here,

the optimization process is also generalized to find out the optimized component parameters as well, which is conducted in a numerical way as shown in Fig. 4-2.

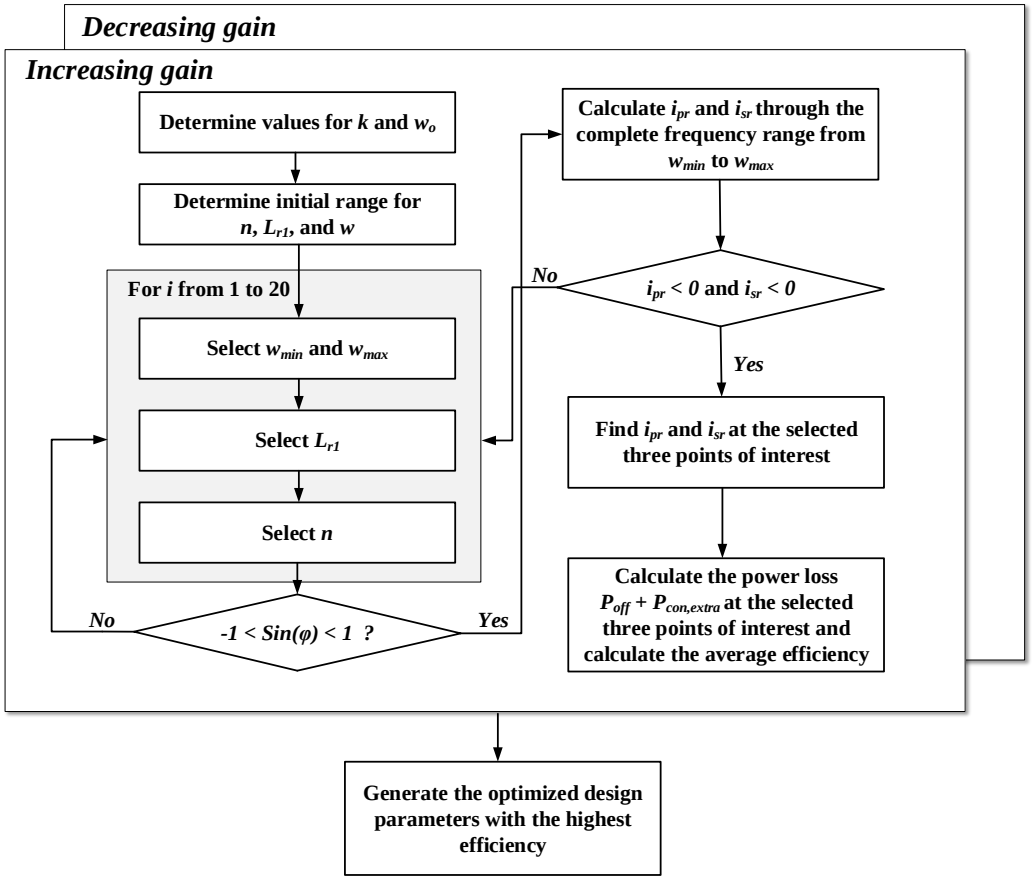

Fig. 4-2. Optimization process for the "$f-\varphi$" control.

The inductance ratio m and the resonant frequency ω_o were selected in the first place. Next, an initial range of the transformer turns ratio n, resonant inductance value L_{r1}, and the switching frequency ω are determined. The algorithm would enter three "for" loops to sweep the values of the above variables. Increasing gain with increasing frequency is analyzed first, and the complete process would be conducted for decreasing gain. Based on Eq. 4-4, the value of $sin\varphi$ can then be calculated at different output voltages. Improper selection of the initial parameters would result in impractical values for $sin\varphi$, thus a check on whether $-1 < sin\varphi < 1$ should be taken at this step.

If the condition holds true for all output voltages, the reactive currents (i_{pr} and i_{sr}) at both sides are calculated next. Then, ZVS property is checked by Eq. 4-7. If it holds true, power loss P_{off} and $P_{extra,con}$ are calculated and averaged at three different voltages: 200V (light load), 300V (mid load) and 400V (peak load), which aims to ensure an overall high efficiency over the entire charging period. Once it is finished, other initial values of k and ω_o can be selected and the same process is conducted. The lowest average power loss scenario is selected, and the corresponding design parameters are finalized.

Based on the electric specifications of a 6.6 kW converter as an example, the optimized component parameters and the switching frequency range are listed in Table 4-1 and Table 4-2.

Table 4-1. Optimized component parameters for the "$f-\varphi$" control.

Parameters	**Values**
Transformer turns ratio n	1.45
Resonant frequency ω_o (MHz)	1.5
Resonant inductance L_{r1} (μH)	1.68
Resonant capacitor C_{r1} (nF)	6.68
Inductance ratio m	5

Table 4-2. Switching frequency range and the phase difference value.

Output voltage (V)	**Switching frequency (MHz)**	**Phase difference (degree)**
200	0.915	72.6
300	0.958	62.3
400	1	54.5

The simulation results are next shown. The purpose of simulation (6.6 kW peak power as an example) is to verify the accuracy of the calculation. Based on the

component parameters and the control variables, simulation at three different load conditions could be conducted. The currents (i_p and i_s) and voltages (v_p and v_s) are shown as follows.

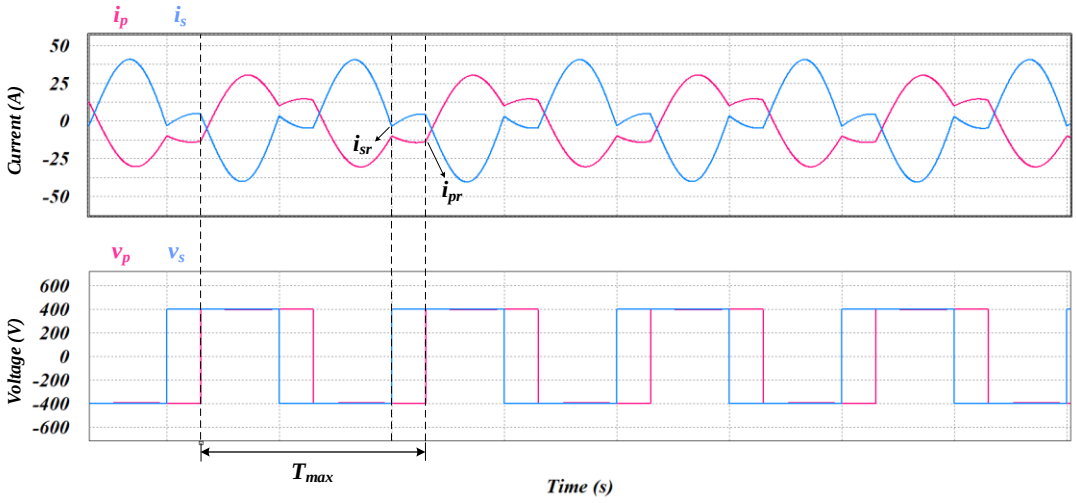

Fig. 4-3. Simulation results for 400V output voltage.

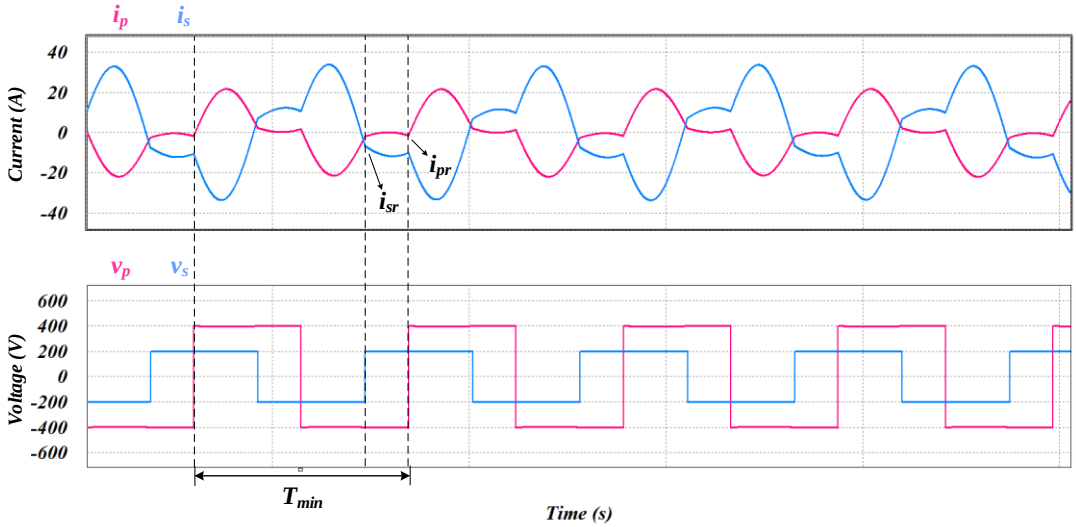

Fig. 4-4. Simulation results for 200V output voltage.

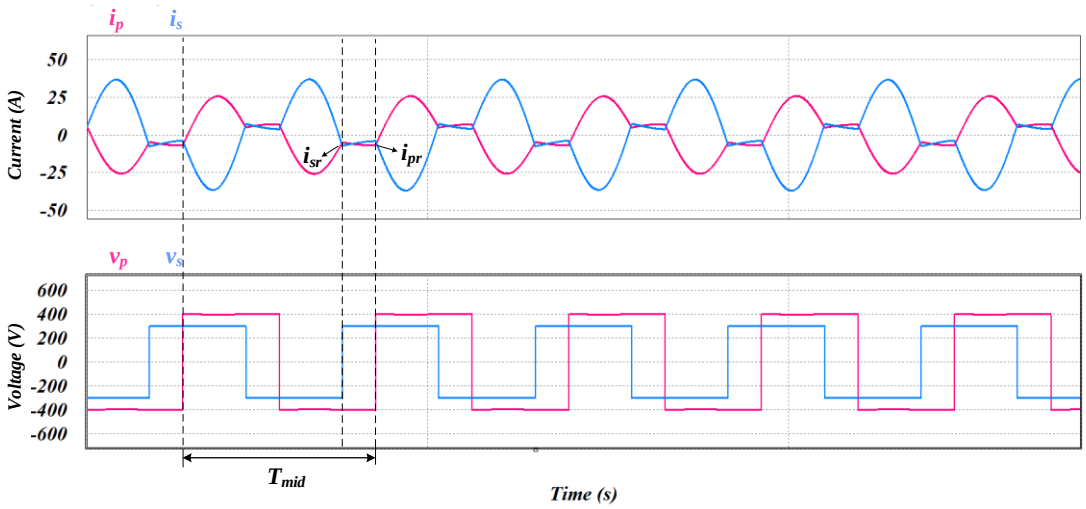

Fig. 4-5. Simulation results for 300V output voltage.

The turning-off current measured from the simulation is compared with the estimation, which is shown in Table 4-3. It can be noted that the estimated values have shown same trend of variation and are close to the simulation results within small errors.

Table 4-3. Estimated and simulated current values at different loading conditions.

Variables	Estimation	Simulation
Primary reactive current at 400V output voltage (A)	-12.3	-13.5
Secondary reactive current at 400V output voltage (A)	-1.10	-2.74
Primary reactive current at 200V output voltage (A)	-0.45	-0.99
Secondary reactive current at 200V output voltage (A)	-6.00	-6.66
Primary reactive current at 300V output voltage (A)	-5.63	-6.72
Secondary reactive current at 300V output voltage (A)	-5.66	-7.11

Based on the EHA modeling introduced in Chapter 3, a set of optimized coefficients for a conventional CLLC converter is also determined for comparison purpose. The

values are listed in Table 4-4. As can be seen, due to the fact that the switching frequency is lower than the resonant frequency in the "$f-\varphi$" control, the values of the passive components could be even smaller than the conventional case, which is one major benefits of the proposed method.

Table 4-4. Optimized component parameters for the PFM control.

Parameters	**Values**
Transformer turns ratio n	0.84
Resonant frequency ω_o (MHz)	0.5
Resonant inductance L_{r1} (μH)	4.7
Resonant capacitor C_{r1} (nF)	21.6
Inductance ratio m	8

The power loss distribution could then be calculated and compared with the PFM scheme based on Eq. 4-8 and Eq. 4-9. As seen from Fig. 4-6, the total power loss at the peak power in "$f-\varphi$" control is close to the value in PFM control, with slightly higher value of ~10 W. However, the light load and mid load power loss is reduced a lot (more than 50%), which demonstrates the effectiveness of the control algorithm. The reduction of the loss at lighter loads not only save the energy during the entire charging process, but also relax the thermal requirements at the worst case scenario.

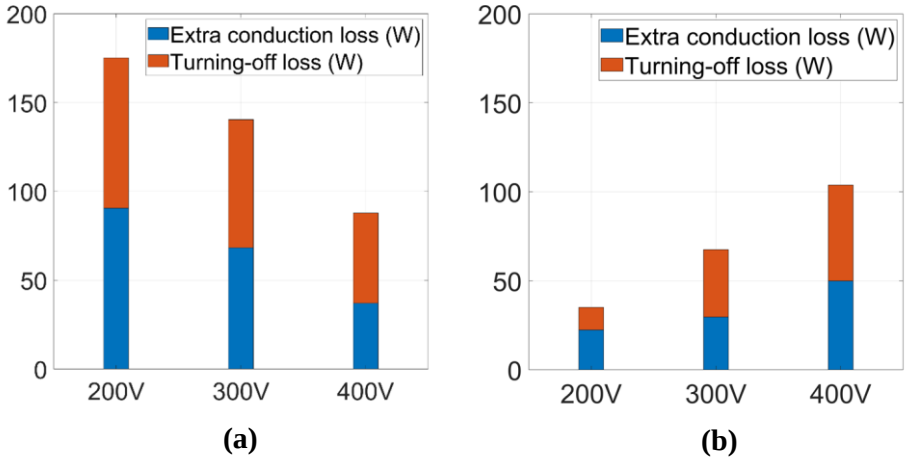

Fig. 4-6. Comparison of power loss values between (a) PFM control and (b) "$f-\varphi$" control.

4.3 Hardware consideration

4.3.1 Switches

Rapid development of the WBG technology has led to an increased number of GaN devices available from the market. Specifically, the GaN High Electron Mobility Transistor (HEMT) is utilized for the fast switch due to its ultra-low gate charge and low drain-to-source turn-on resistance (R_{ds_on}). Several major manufacturers have released their 650V products for automotive industry, which are shown in Table 4-5.

Table 4-5. Selected GaN HEMTs from different manufactures.

	GaN System	**Transphorm**	**GANPOWER**	**Infineon**
Part number	GS66508T	TP65H035WS	GPI65030DFO (Preliminary)	IGT60R070D1
Vdss (V)	650	650	650	600
Rds_on (mΩ) at 25 ℃	50	35	55	55
Rds_on (mΩ) at 120 ℃	129	60	140	100
Id (A)	30	46.5	30	31
Gate charge (nC)	5.8	24	N/A	5.8
Package	GaN_{PX}	TO-247	DFN	PG-HSOF-8-3
Dimension (mm)	7 × 4.5	15.9 × 20.85	6 × 8	10 × 11.6

Here GS66508T is chosen as the switch in this application. To incorporate with future development into even higher power level, two GS66508T are connected in parallel to increase the current level. TP65H035WS with the cascode structure is previously applied in [37], but the through-hole package type is not very suitable for high frequency application due to the additional parasitic inductance on the pins.

4.3.2 Gate driver

Since GaN HEMTs would be turned on at a lower gate voltage (5 to 6V) than silicon MOSFETs (15 to 20V), adding a negative voltage to turn the switch off is suggested to avoid fault trigger. For this purpose, isolated gate driver circuit is applied and shown in Fig. 4-7. An isolated DC-DC power supply (15V to 9V) along with a 5.8V Zener diode is utilized to convert the bus voltage (15V) to +6V/-3V voltage levels, which are

connected to the secondary side of the gate driver. The turn-on and turn-off path are separate in the driver IC, which has a 10Ω and 2Ω resistor respectively.

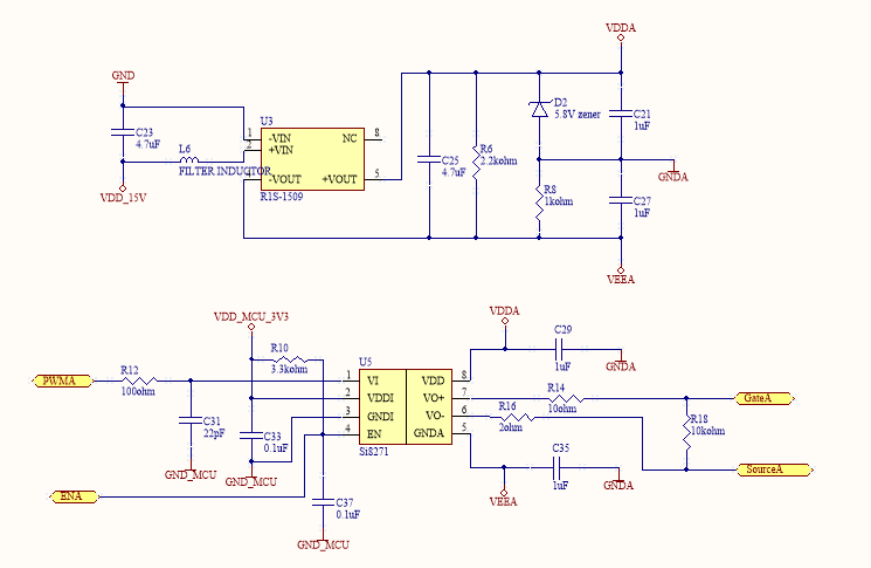

Fig. 4-7. Gate driver circuit.

Designing the gate drive circuit for two parallel switches is critical, since it should not only maintain good noise immunity against high frequency noise (especially in high frequency applications), but also should guarantee a same turn-on time for both switches to equally distribute the current. The first requirement is achieved by minimizing the loop inductance, where the turn-on path and the return path could be implemented on two PCB layers with one sitting right on the top of the other. The second requirement could be achieved by making the driving path of two switches as symmetric as possible. The PCB layout for one pair of the switches is shown in Fig. 4-8.

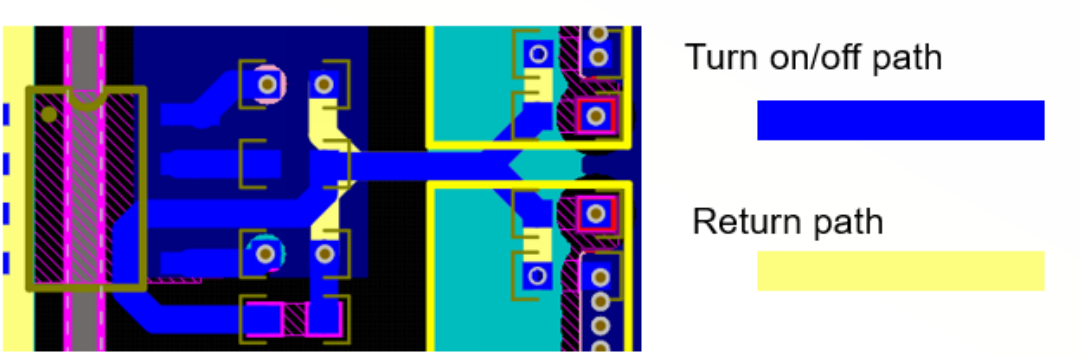

Fig. 4-8. PCB layout of the gate drive circuit for two parallel switches.

4.3.3 System Overview

To verify the aforementioned analysis, an onboard charging system is implemented on a PCB shown in Fig. 4-9. This circuit board consists of the switching circuit including the PFC stage, DC-DC stage, DC-link capacitors, and controller interface. To find out the optimized magnetic winding structure, magnetic components are implemented on separate boards. After soldering all the components, pictures of the top and bottom side of the system are shown in Fig. 4-10 and Fig. 4-11. As can be seen, only GaN HEMTs are placed on the bottom side where heatsink or cold plate could be attached. All other components are soldered on the top side.

TMS320F28377D Delfino dual core 32-bit MCU is chosen as the controller in this design for its high main clock frequency (200 MHz), fast data processing capability and adequate peripherals.

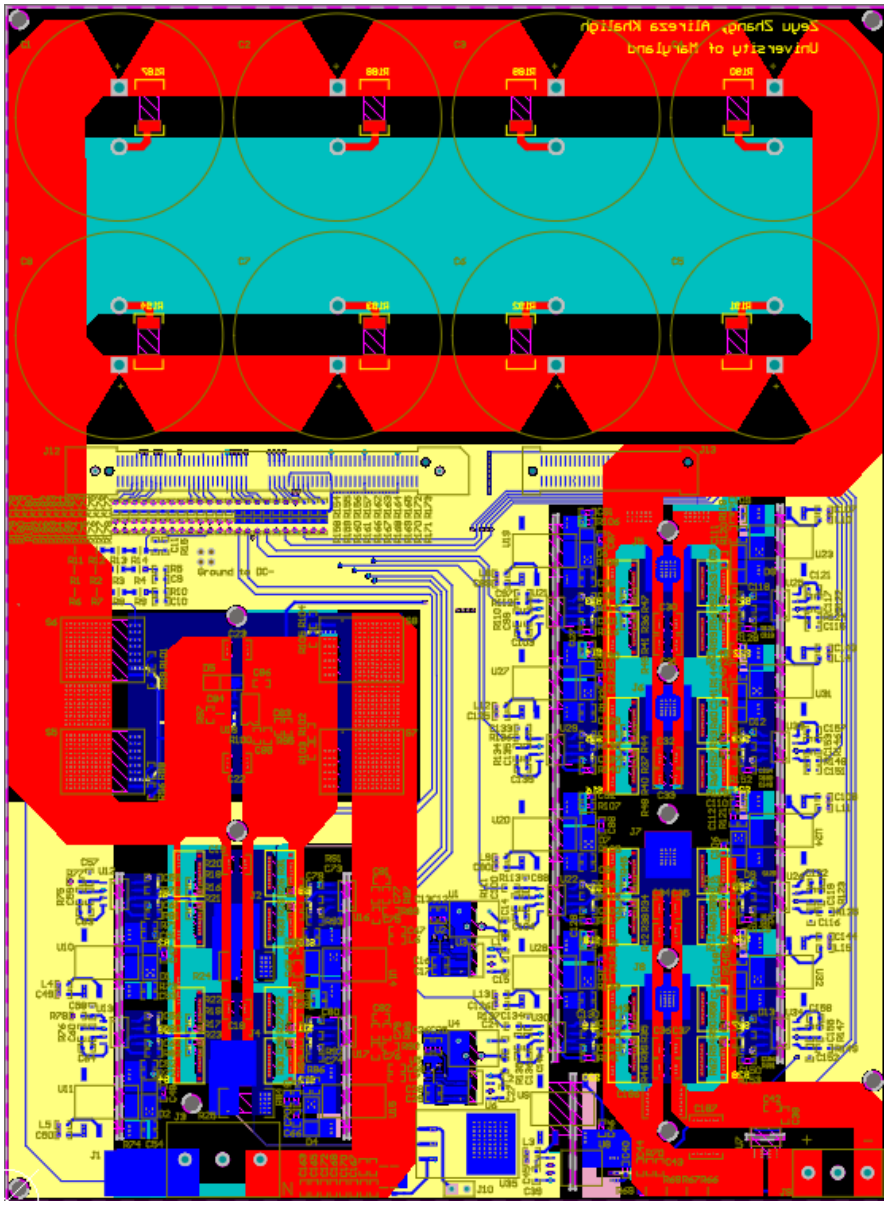

Fig. 4-9. PCB layout for the switching board.



Fig. 4-10. Top side of the PCB.

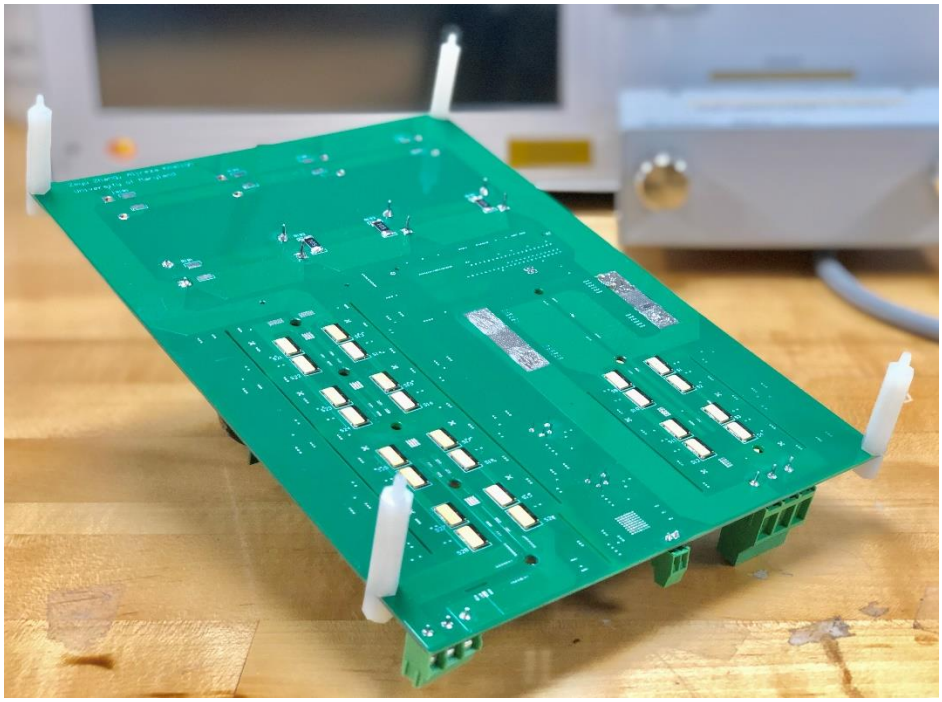

Fig. 4-11. Bottom side of the PCB.

4.4 Experimental Results

A 3.3 kW peak power CLLC converter based on "$f-\varphi$" control is tested with the calculated and optimized component coefficients, which are measured and listed in Table 4-6.

Table 4-6. Optimized component parameters for the "$f-\varphi$" control (3.3kW peak power).

Parameters	**Values**
Transformer turns ratio n	8 to 9
Resonant frequency ω_o (MHz)	1
Resonant inductance L_{r1} (μH)	3
Resonant capacitor C_{r1} (nF)	10.1
Resonant capacitor C_{r2} (nF)	6.8
Inductance ratio m	4.6

The tested switching frequency and phase shift values are listed in Table 4-7.

Table 4-7. Testing coefficients for the 3.3kW prototype.

Condition	**Frequency**	**Phase shift**
400V to 400V, 3.3kW	562 kHz	55.6°
400V to 300V, 2.48kW	549 kHz	59.3°
400V to 200V, 1.65kW	534 kHz	48.1°

The tested waveforms at three operation conditions are shown in Fig. 4-12 to Fig. 4-14. From top to bottom are the output voltage (purple), primary current (green) and primary bridge voltage (blue), respectively.

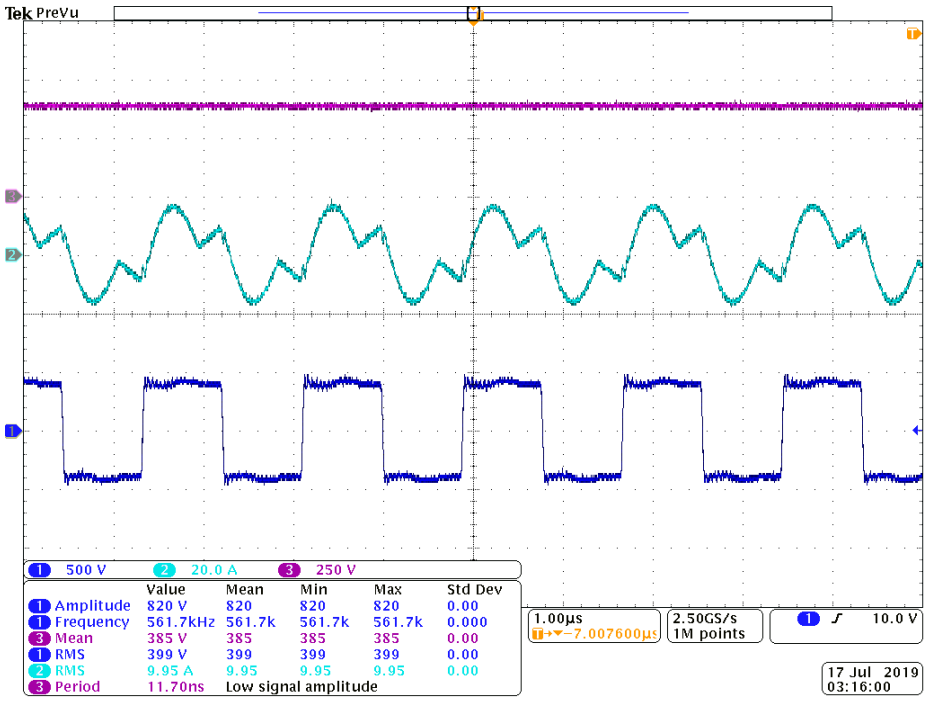

Fig. 4-12. 400V to 400V condition waveform.

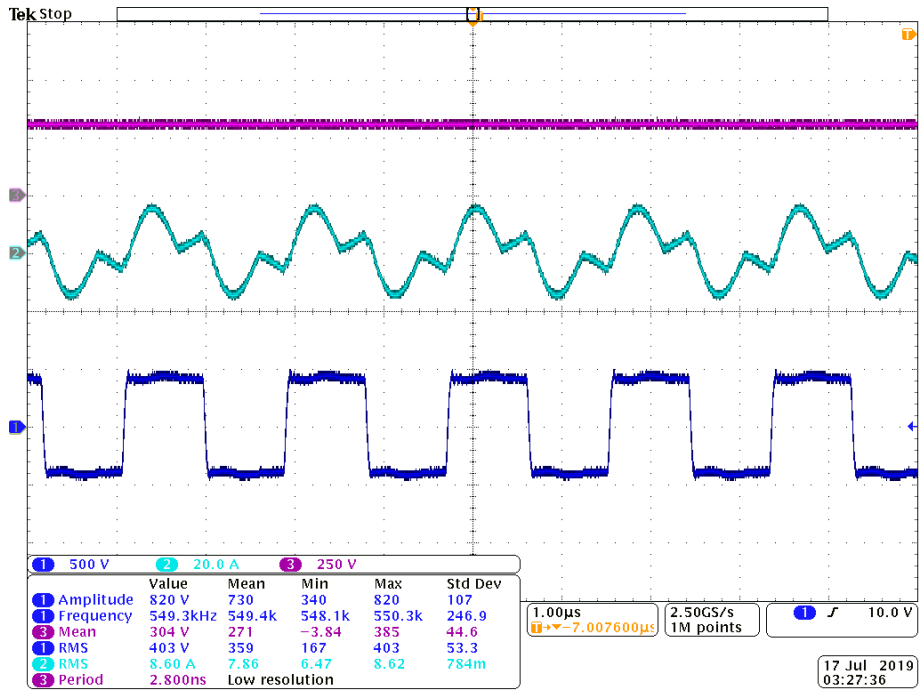

Fig. 4-13. 400V to 300V condition waveform.

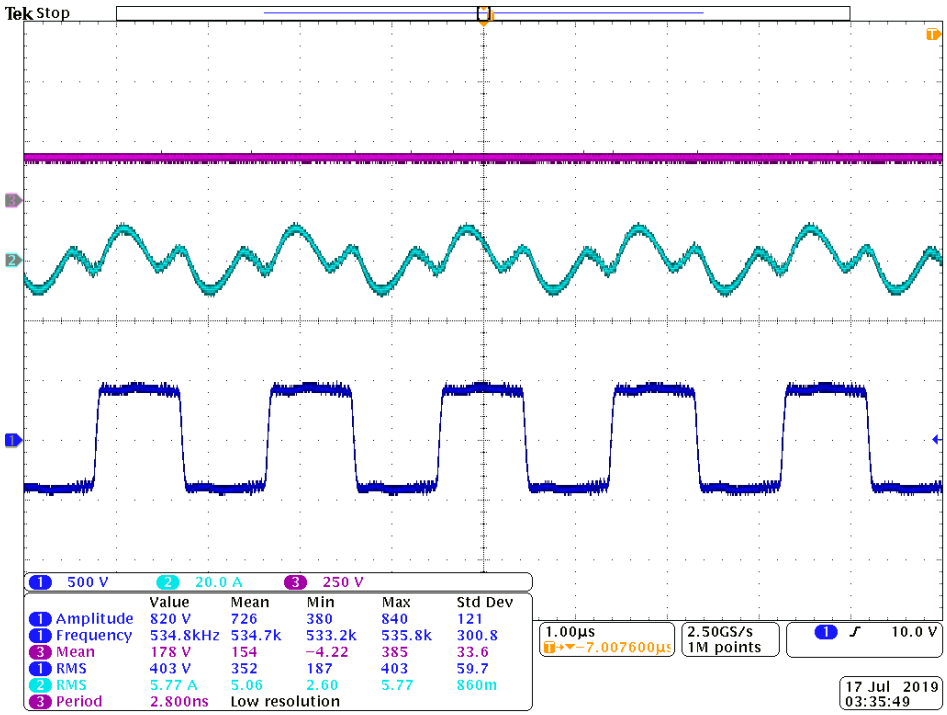

Fig. 4-14. 400V to 200V condition waveform.

The tested efficiency curve is shown next in Fig. 4-15. It can be seen that the peak power efficiency is 96.4%, 96.4%, and 94.2% respectively at three working conditions, which validates the high efficiency operation proposed in the first place.

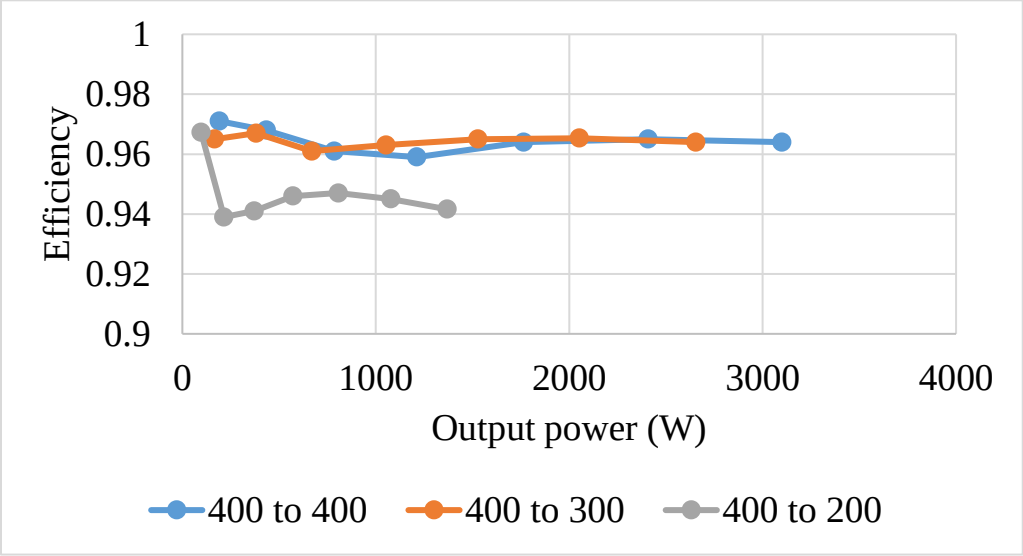

Fig. 4-15. Efficiency curve at different operation conditions.

Chapter 5: Planar Magnetics with Interleaved Winding Structure

5.1 Introduction

As discussed before, the magnetic components (inductors and transformers) in the proposed design are achieved using planar magnetics, where the windings are implemented by the PCB traces. In the PFC stage, the coupled inductor is implemented on an EI core where the first and second winding can be individually wounded on the two side legs of the core. The side view of the inductor is depicted in Fig. 5-1, where the winding turns are represented by the blue (first winding) and red (second winding) blocks. Here, a twelve-turn structure with two turns on the same layer is shown in this figure. The cross-section area of the side leg and the center leg are defined as A_{e1} and A_{e2}, respectively. Since the inductance value applied in the design is relatively small, an air gap is inserted between the E core and the I core, whose values are l_{g1} for the side leg and l_{g2} for the center leg. It is already known that by tuning the cross-section area and the air gaps, one can directly control the inductance value and the coupling factor, but limitations may apply. For one thing, the air gaps (l_{g1} and l_{g2}) are preferred to be made the same, or it will add much complexity into mass production and manufacturing, adding the costs at the same time. In addition, off-the-shelf magnetic cores are selected in this design for better availability, whose center leg cross-section area is usually doubled compared to the side leg's ($A_{e2} = 2A_{e1}$). As will be shown later, the resulted coupling factor would only have one possible value ($\alpha = -0.33$ calculated by Eq. 5-10). It is necessary to add one more control variable to change the inductance, where the interleaved winding structure is utilized shown in Fig. 5-2 [43].

In this structure, a portion of the first winding turns (referred as standard turns whose number is denoted by N_1) is implemented on the left leg, and the remaining turns (referred as interleaved turns whose number is denoted by N_2) are winded on the right leg. The same winding strategy is applied for the second winding as well. It should be noted that the direction of the interleaved turns is opposite to the standard turns to generate reverse direction of the magnetic flux.

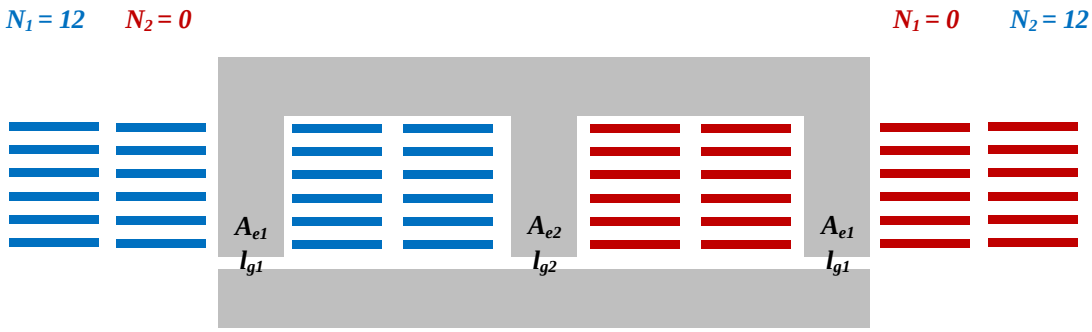

Fig. 5-1 Structure of conventional coupled inductor ($N_1 = 12, N_2 = 0$ on the left leg).

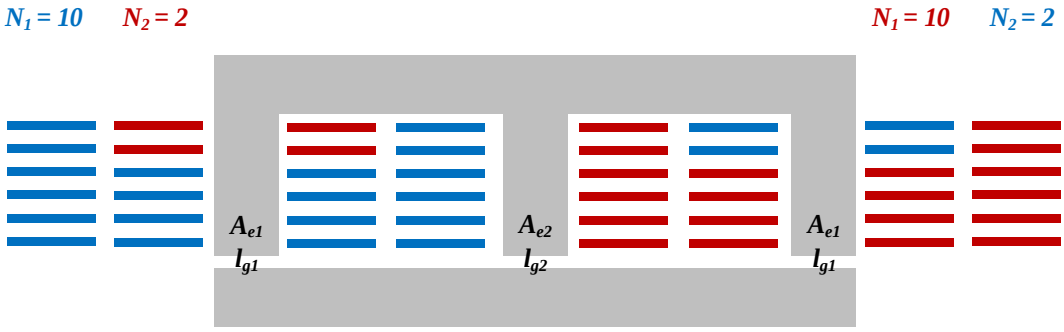

Fig. 5-2. Structure of the interleaved coupled inductor ($N_1 = 10, N_2 = 2$ on the left leg).

5.2 Coupled inductor magnetic structure

To calculate the coupled inductance value, an equivalent circuit to model the magnetic paths and flux density are shown in Fig. 5-3. The magnetomotive force (MMF), represented by the product of the winding turns and the winding current, is

shown on each side leg as equivalent to a voltage source. Since the standard and interleaved turns have opposite direction, the polarity of the equivalent voltage source is also different. The air gaps are depicted as resistors whose values are equivalent to their reluctance: $R_{g1} = \frac{l_{g1}}{A_{e1}\mu_0}$, $R_{g2} = \frac{l_{g2}}{A_{e2}\mu_0}$ (R_{g1} for side leg and R_{g2} for center leg), where μ_0 denotes the electromagnetism permeability of the air. Usually, the reluctance of the air gap is much larger than the reluctance of the magnetic core, thus only the air gap reluctances are included in the model. Besides, the magnetic flux through the first and second winding are denoted as ϕ_1 and ϕ_2, which can be regarded as two current flows in the equivalent model. Note that a portion of the magnetic flux will go through the center leg, so that the effect of the interleaved turns is not completely added on the standard turns. As can be shown later, the existence of the center leg could give more flexibility to control the inductance value, which can also explain that the EI core is a better solution than the UI core to form a coupled inductor.

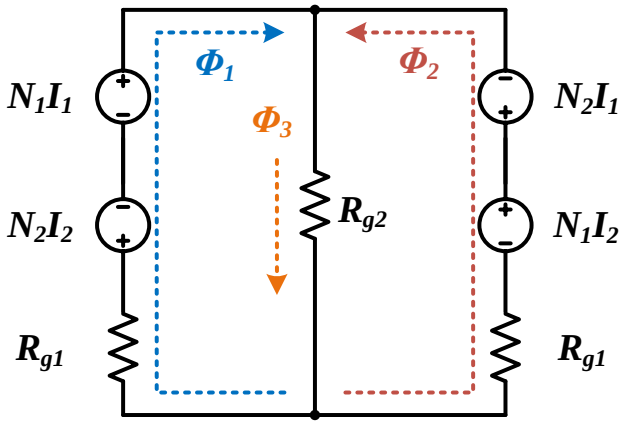

Fig. 5-3. Equivalent circuit modelling for the coupled inductor.

By using superposition, the magnetic flux through the left leg can be expressed by:

$$\phi_1 = \frac{N_1 I_1 - N_2 I_2}{R_{g1} + R_{g2}//R_{g1}} - \frac{N_1 I_2 - N_2 I_1}{R_{g1} + R_{g1}//R_{g2}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}} \quad \text{Eq. 5-1}$$

Similarly, the magnetic flux through the right leg can be expressed by:

$$\phi_2 = \frac{N_1 I_2 - N_2 I_1}{R_{g1} + R_{g2}//R_{g1}} - \frac{N_1 I_1 - N_2 I_2}{R_{g1} + R_{g1}//R_{g2}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}} \quad \text{Eq. 5-2}$$

Thus, the magnetic flux in the center leg (ϕ_3) can be expressed as:

$$\phi_3 = \phi_1 + \phi_2 = \frac{(N_1 - N_2)(I_1 + I_2)}{R_{g1} + R_{g2}//R_{g1}} \cdot \frac{R_{g1}}{R_{g1} + R_{g2}} \quad \text{Eq. 5-3}$$

Next, we are going to find the relationship between the winding structure and the inductance values. As shown in Fig. 5-4, the coupled inductor can be equivalently considered as a 1:1 transformer with the magnetizing inductance of L_m and the leakage inductance of L_s. The relationship between self and mutual inductance, and leakage and magnetizing inductance can be easily found as:

$$L = L_s + L_m \quad \text{Eq. 5-4}$$

$$M = -L_m \quad \text{Eq. 5-5}$$

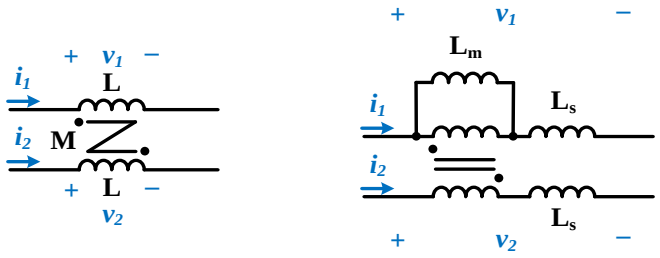

Fig. 5-4. Coupled inductor and equivalent model.

If we directly measure the first winding inductance and set the second winding current to be zero, the result would reflect the summation of L_m and L_s (shown in Fig. 5-5 (a)). If we still measure the first winding inductance and set the first winding current

to be zero, the second winding current would be reflected only on the magnetizing inductance and thus the measurement result would represent L_m (Fig. 5-5 (b)).

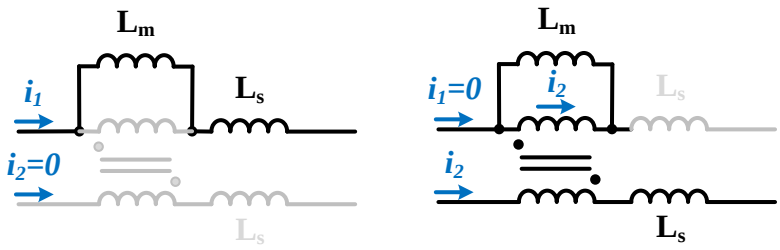

Fig. 5-5. Equivalent circuit under two test conditions.

Based on Eq. 5-1 to Eq. 5-3 and the relationship between magnetic flux and inductance, the value of L and M can be expressed as:

$$L = L_m + L_s = \frac{N_1\phi_1 - N_2\phi_2}{I_1}|_{I_2=0} = \frac{N_1^2 + N_2^2}{R_{g1} + R_{g1}//R_{g2}} + \frac{2N_1N_2}{R_{g1} + R_{g1}//R_{g2}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}}$$
$$= \frac{N_1^2 + N_2^2}{R_{g1} + 2R_{g2}} + \frac{(N_1 + N_2)^2 R_{g2}}{R_{g1}^2 + 2R_{g1}R_{g2}} \quad \text{Eq. 5-6}$$

$$M = -L_m = -\frac{N_1\phi_1 - N_2\phi_2}{-I_2}|_{I_1=0} = -\frac{2N_1N_2}{R_{g1} + R_{g1}//R_{g2}} - \frac{N_1^2 + N_2^2}{R_{g1} + R_{g1}//R_{g2}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}}$$
$$= \frac{-2N_1N_2}{R_{g1} + 2R_{g2}} - \frac{(N_1 + N_2)^2 R_{g2}}{R_{g1}^2 + 2R_{g1}R_{g2}} \quad \text{Eq. 5-7}$$

Since we also have the following assumption: $A_{e2} = 2A_{e1}, l_{g1} = l_{g2}$, which leads to $R_{g1} = 2R_{g2}$, the expression for the self and mutual inductance can be further simplified as:

$$L = \frac{3N_1^2 + 2N_1N_2 + 3N_2^2}{8R_{g2}} \quad \text{Eq. 5-8}$$

$$M = -\frac{N_1^2 + 6N_1N_2 + N_2^2}{8R_{g2}} \quad \text{Eq. 5-9}$$

The coupling factor can be then expressed as:

$$\alpha = \frac{M}{L} = -\frac{N_1^2 + 6N_1N_2 + N_2^2}{3N_1^2 + 2N_1N_2 + 3N_2^2} \quad \text{Eq. 5-10}$$

Therefore, by controlling the standard and the interleaved turns number, one can directly control the coupling factor, which is much easier than controlling the air gaps or the cross-section areas. For example, if $N_1 = 10$, $N_2 = 2$, the coupling factor can be calculated as $\alpha = -0.64$, which corresponds to the lowest RMS current case based on Fig. 2-12. Since $L = 10\mu H$ and $M = -6.4\mu H$, the reluctance of the air gaps can be also calculated: $R_{g1} = 8.8 \times 10^6 H^{-1}$, $R_{g2} = 4.4 \times 10^6 H^{-1}$. The magnetic flux density values at different parts of the core can be calculated:

$$B_1 = \frac{\phi_1}{A_{e1}} = \frac{4I_1 - 2I_2}{A_{e1}R_{g2}} \quad \text{Eq. 5-11}$$

$$B_2 = \frac{\phi_2}{A_{e2}} = \frac{4I_2 - 2I_1}{A_{e2}R_{g2}} \quad \text{Eq. 5-12}$$

$$B_3 = \frac{\phi_3}{A_{e3}} = \frac{2I_1 + 2I_2}{A_{e3}R_{g2}} \quad \text{Eq. 5-13}$$

Next, we will investigate the physical implementation of the coupled inductor. Suppose E64 planer E core from Ferroxcube is chosen with the center leg cross-section area of $A_{e2} = 519mm^2$. The air gap can be then calculated as: $l_{g1} = l_{g2} = 2.87mm$. Under the above conditions and the current waveform shown in Chapter 2, the flux density maximum and minimum values through the side leg and center leg can be calculated, which are depicted in Fig. 5-6. Several insights can be drawn from the plots. First, the flux density in the center leg is much smaller than the side leg due to the current cancellation effect offered by the interleaved legs. Second, based on the core material 3F36 (suitable for high frequency application with saturated flux density of

420mT at 100℃), the calculated flux density is maintained at a reasonable region without causing saturation.

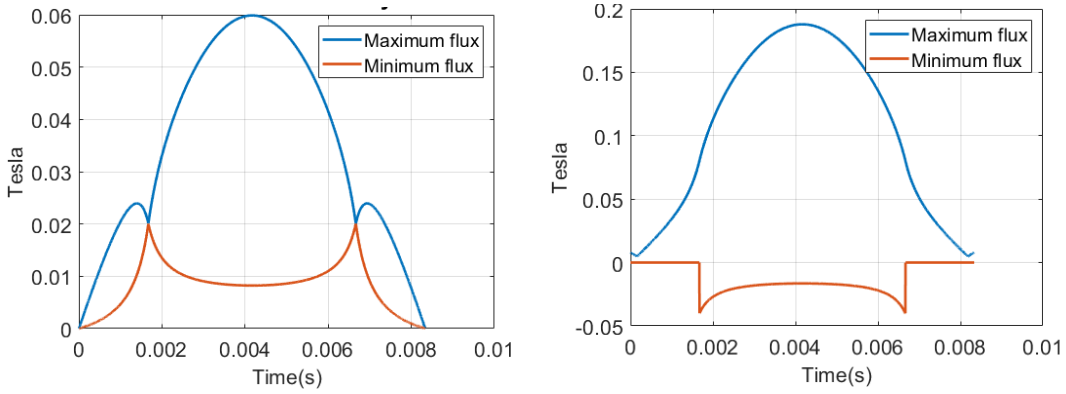

Fig. 5-6. Maximum and minimum flux density in center leg (left) and side leg (right).

We further investigate the flux density variation ($\frac{\Delta B}{2}$) in both side leg and center leg for the core loss calculation, as shown in Fig. 5-7.

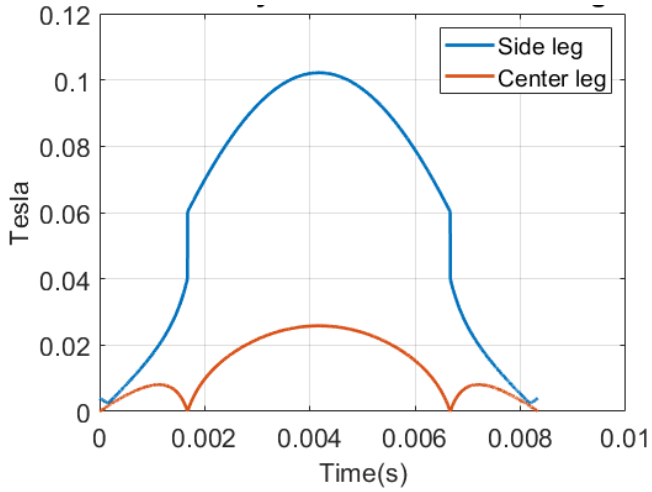

Fig. 5-7. Flux density variation in side leg and center leg.

Note that the switching frequency is always changing in this application, the flux density variation ($\frac{\Delta B}{2}$) is smaller at higher frequency due to smaller current and vice versa. In a conventional fixed-frequency PFC rectifier, the core loss calculation is based on the following equation:

$$P_{core} = \alpha f^{x} (\frac{\Delta B}{2})^{y} L(T) V_{core} \quad \text{Eq. 5-14}$$

where α, x, y are constants that are related with the core material, f denotes the switching frequency, $L(T)$ is a temperature dependent coefficient and V_{core} represents the volume of the core. In the proposed design, the method to calculate the core loss is to divide the input line period into various small time segments, find out the frequency and flux density in each time segment, and finally integrate the core loss over the entire line period, which can be explained by:

$$P_{core} = \int \alpha f(t)^{x} (\frac{\Delta B(t)}{2})^{y} L(T) V_{core} dt \quad \text{Eq. 5-15}$$

Based on the algorithm, the core loss is estimated to be 11.4W. Better analysis of the coupled inductor can be conducted by 3D FEA simulation in ANSYS Maxwell. Fig. 5-8 shows the physical structure of the core and the winding. The interleaved structure is not shown explicitly, but the excitation currents in the interleaved turns are already inverted 180 degree than the standard turns. Magnetic flux density distribution is simulated at the peak current condition, which corresponds to peak input voltage ($240\sqrt{2}V$) and minimum switching frequency (200 kHz). The flux density at most parts of the core is less than 100mT, which is in agreement with the calculation.

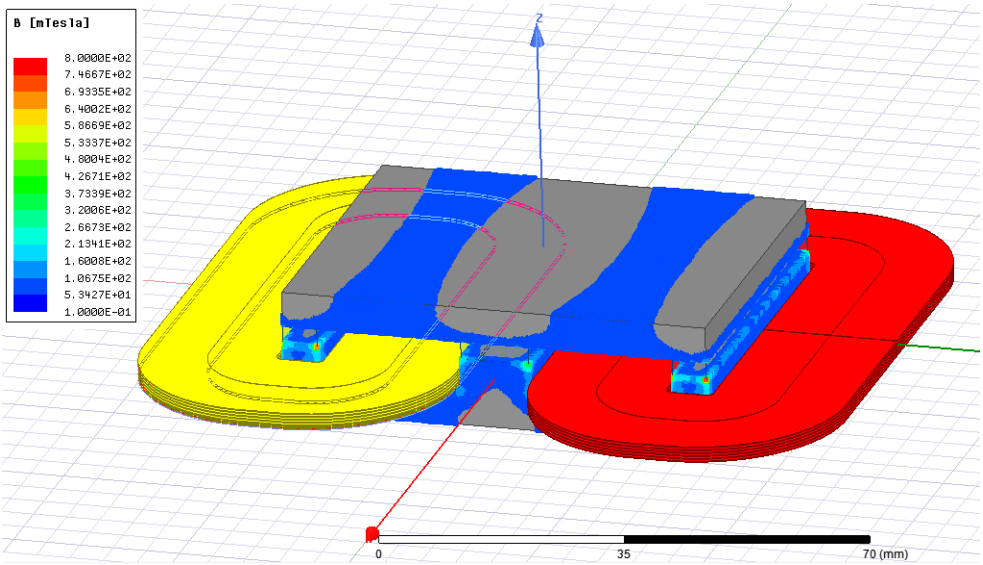

Fig. 5-8. Magnetic flux density simulation.

5.3 Transformer magnetic structure

Unlike the coupled inductor from last section which has the same turns number on both sides, the planar transformer applied in the DC-DC stage could have non-unity turns ratio. Thus, the equivalent magnetic model should contain more generality, which is shown in Fig. 5-9. $n_{1,a}$ and $n_{1,b}$ correspond to the turns number of the primary winding on the left and right leg of the core, and $n_{2,a}$ and $n_{2,b}$ correspond to the turns number of the secondary winding on the left and right leg of the core.

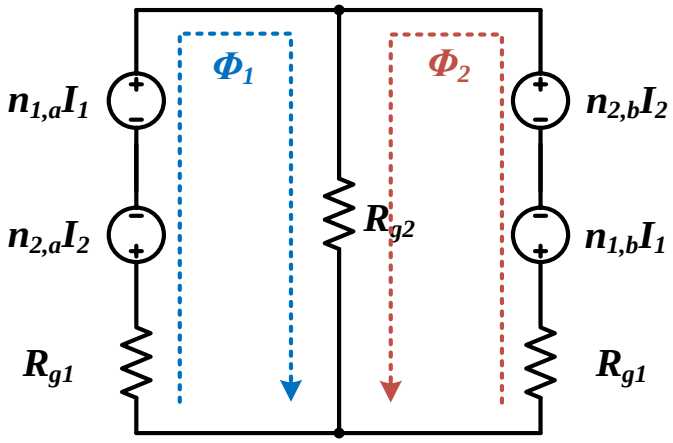

Fig. 5-9. Equivalent circuit modelling for the planar transformer.

Next, the leakage L_s and magnetizing inductance L_m of the transformer can be calculated using a similar method. Their relationship is expressed as follows.

$$L_m = \frac{n_1}{n_2} \cdot \frac{3n_{1,a}n_{2,a} + n_{1,a}n_{2,b} + n_{1,b}n_{2,a} + 3n_{1,b}n_{2,b}}{8R_{g2}} \quad \text{Eq. 5-16}$$

$$L_s + L_m = \frac{3n_{1,a}^2 + 2n_{1,a}n_{2,b} + 3n_{1,b}^2}{8R_{g2}} \quad \text{Eq. 5-17}$$

Based on the inductance expression, different winding structure and the resulting coefficients could be listed in Table 5-1. The winding structures are represented in the form of "$n_{1,a}Pn_{2,a}S$" on the left leg and "$n_{1,b}Pn_{2,b}S$" on the right leg.

Table 5-1. Different winding structure of the planar transformer.

Winding structure	Turns ratio	Inductance ratio
4P3S 1P4S	5 to 7	4.3
4P2S 2P5S	6 to 7	7.3
5P3S 1P4S	6 to 7	3.5
5P3S 2P4S	7 to 7	8
5P1S 2P6S	7 to 7	3.46

The designed winding structures are implemented on an 8-layer PCB shown in Fig. 5-10. Different structures are tested in experiment to find out the optimized result.

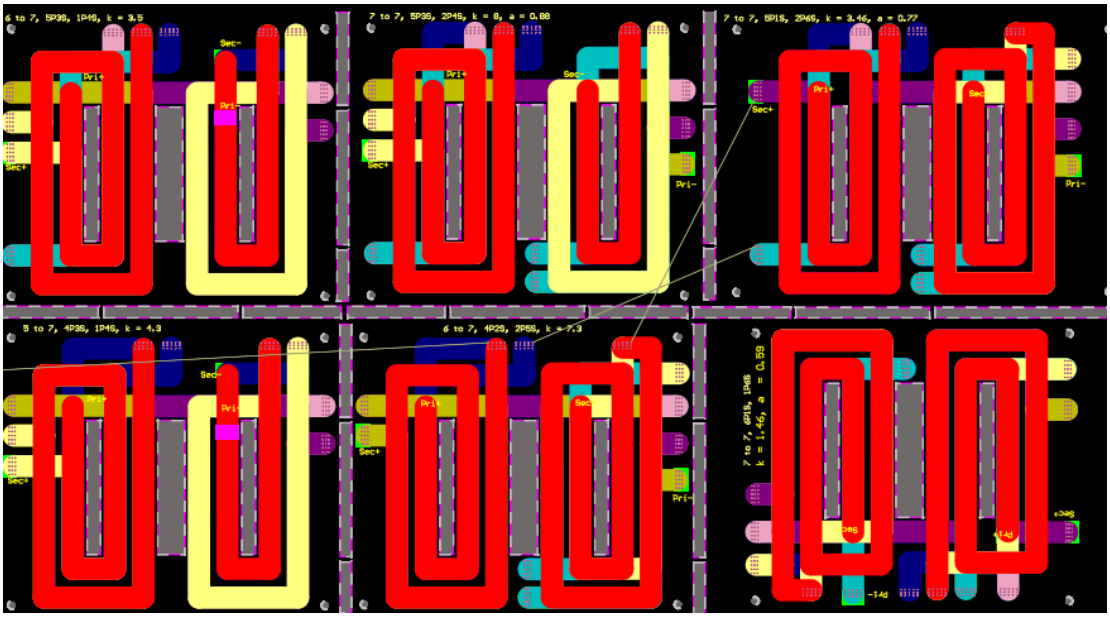

Fig. 5-10. Different winding structures in PCB.

5.4 Considerations to reduce intra-winding capacitance

One major drawback of planar magnetics is that the windings are too close to each other, insulated by a thin FR4 material of the PCB. In order to conduct high current at high power, the width of the winding is also very large. These effects could result in a large intra-winding capacitance, which is defined as the capacitance between the windings on the same side (primary or secondary) of the transformer (C_p in Fig. 5-11). In conventional converters working at 100 to 200 kHz, the resonant capacitor is usually ten times bigger than the parasitic capacitor. However, in higher frequency designs, the resonant capacitor values are smaller. The parasitic capacitor could affect the normal operation of the converter on a large scale. The effect is usually revealed as the distortion on the current waveforms, such as an example shown in Fig. 5-12. The

current could carry high frequency ripples, which would further affect the bridge voltage waveform.

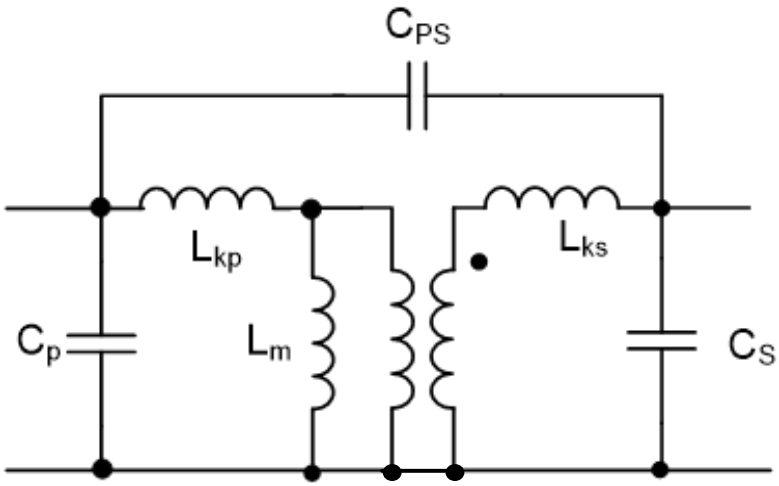

Fig. 5-11. Transformer model with parasitic capacitance.

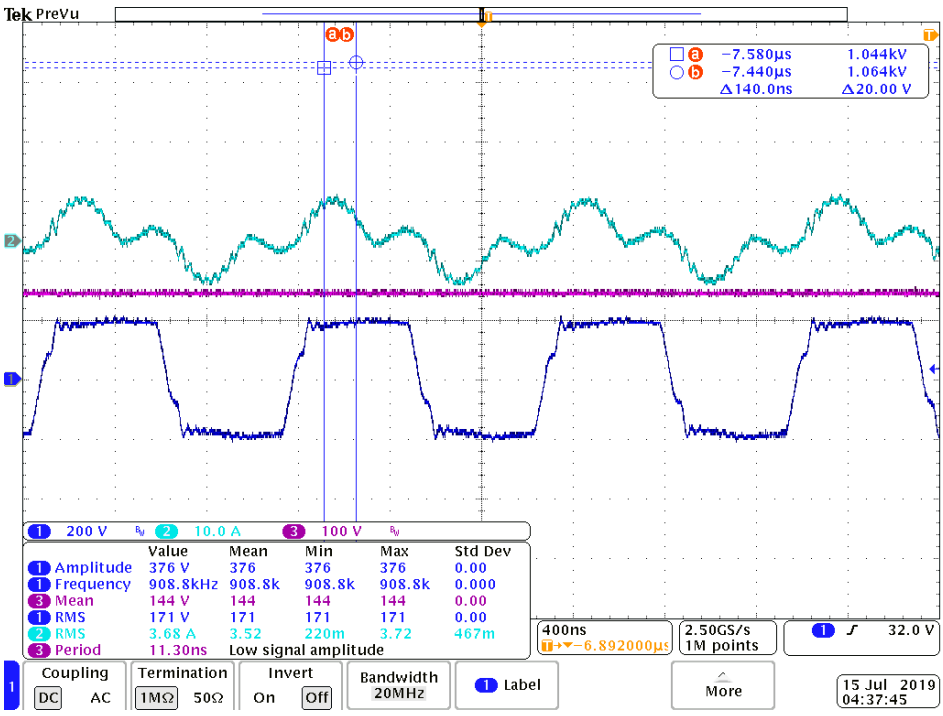

Fig. 5-12. Current waveform distortion due to intra-winding capacitance.

From the capacitance expression shown in Eq. 5-18, two major methods to mitigate the parasitic effect are to increase the thickness of FR4 (defined by t), and reduce the

overlapping area (defined by A) of different windings. Also, trying to interleave the primary and secondary windings as much as possible could also help in this regard.

$$C_p = \varepsilon \cdot \frac{A}{t} \qquad \text{Eq. 5-18}$$

As shown in Fig. 5-13, a concept design would have smaller width trace, and windings in different layer are separated with an overlapping distance of d.

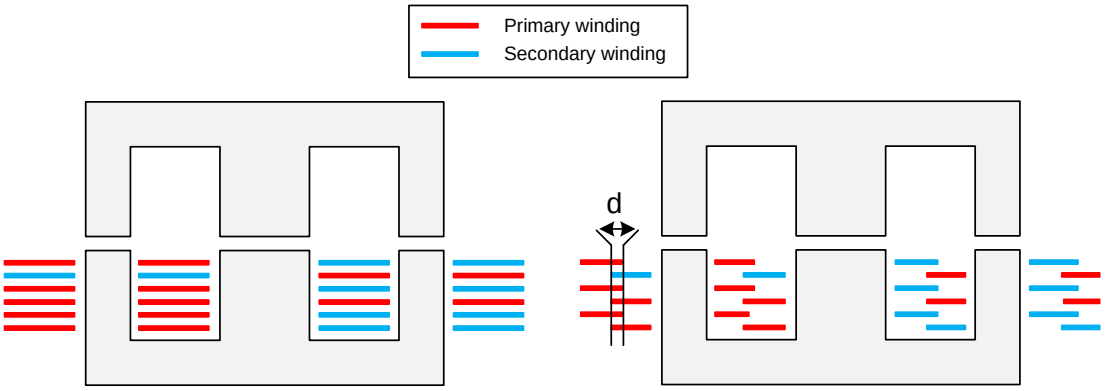

Fig. 5-13. Methods to reduce intra-winding capacitance.

Based on this idea, the planar transformer is depicted in Fig. 5-14and simulated by q3d engine from Ansys, which is shown in Fig. 5-15.

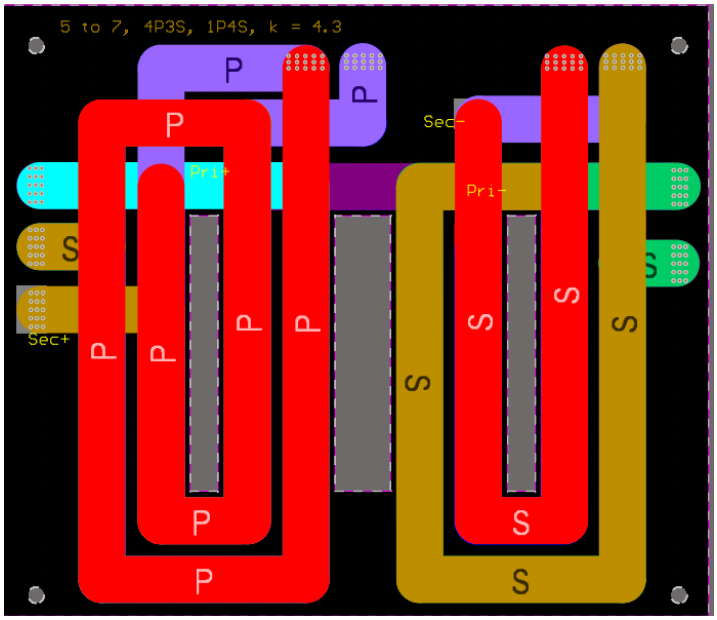

Fig. 5-14. Planar transformer with reduced parasitic capacitance.

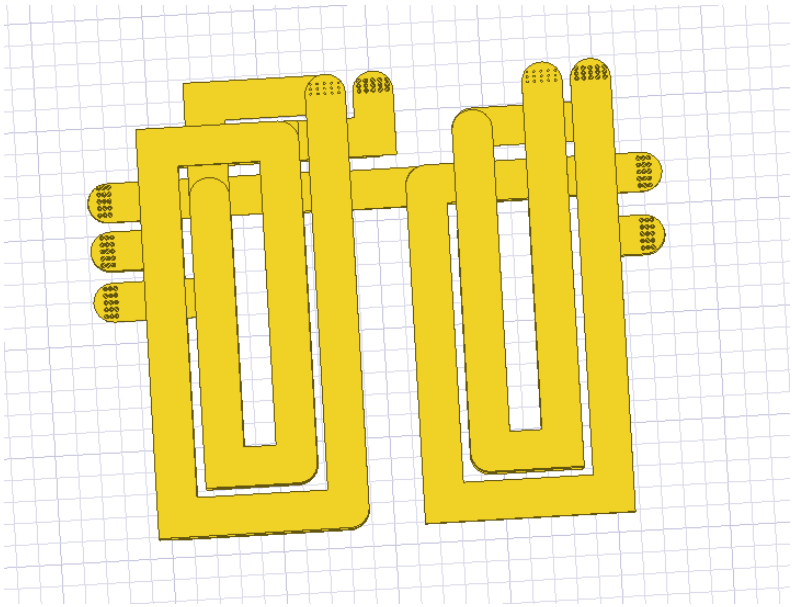

Fig. 5-15. Q3D simulation model of the designed planar transformer.

The simulated results are listed in Table 5-2. As can be seen, the parasitic capacitance values are controlled below 1nF, which is acceptable based on the design parameters of the CLLC converter presented in Chapter 4.

Table 5-2. Simulated results of the planar transformer.

Parameters	Values
Intra-winding capacitance	673 pF
Inter-winding capacitance	677 pF

It should be noted that larger separation of the winding could result in higher AC resistance, since the current interleaving effect is less in this condition. Thus, different values of d is also tested to find out the relationship of capacitance values and the power loss, which are shown in Fig. 5-16 and Fig. 5-17.

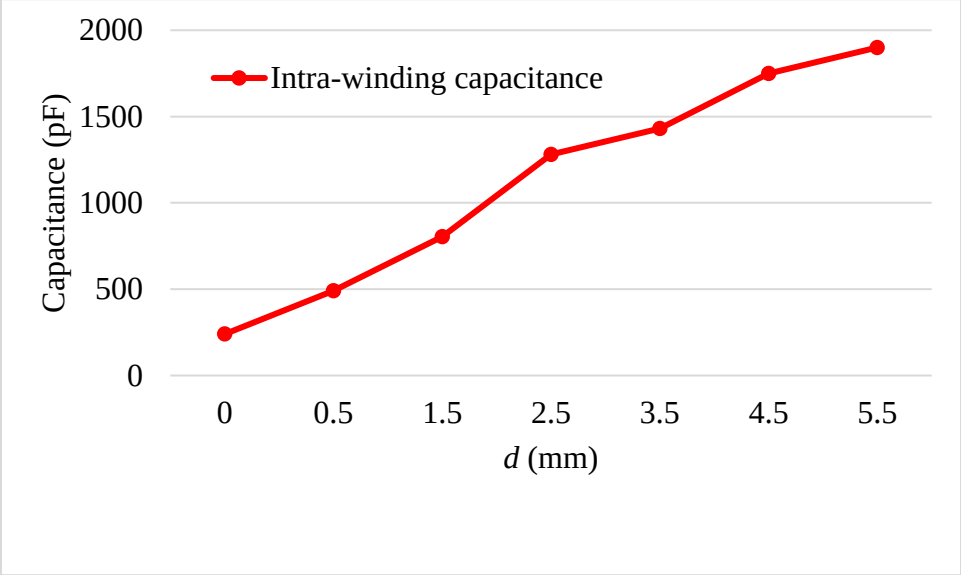

Fig. 5-16. Relationship between intra-winding capacitance and overlapping distance.

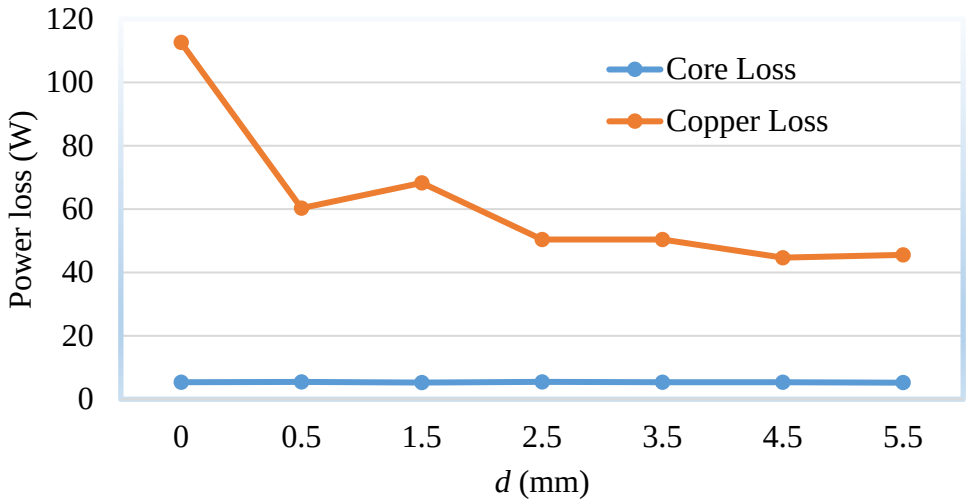

Fig. 5-17. Relationship between power loss and overlapping distance.

The picture of the designed winding structure is shown in Fig. 5-18. By using the impedance analyzer E4990A from Keysight, the intra-winding capacitor is measured for both the coupled inductor and the transformer, shown in Fig. 5-20. As can be seen, the parasitic capacitor is well controlled in pF range, which would not seriously affect the normal operation of the high frequency circuit.

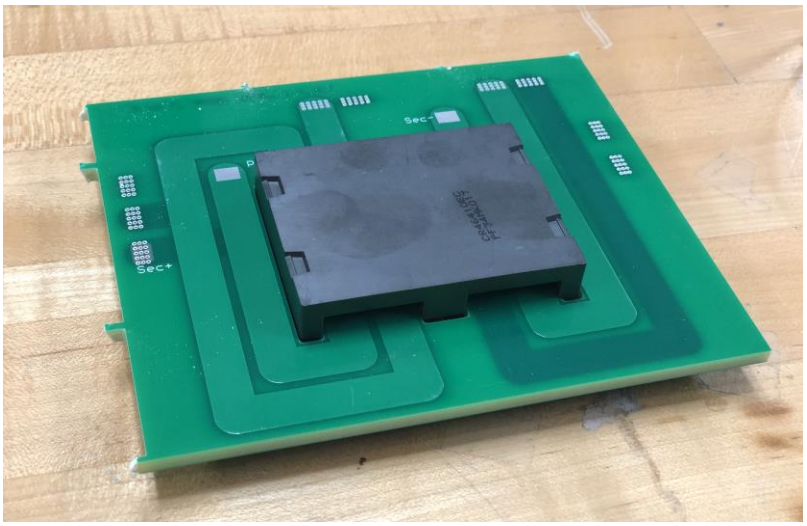

Fig. 5-18. Designed winding structure of the planar magnetics.

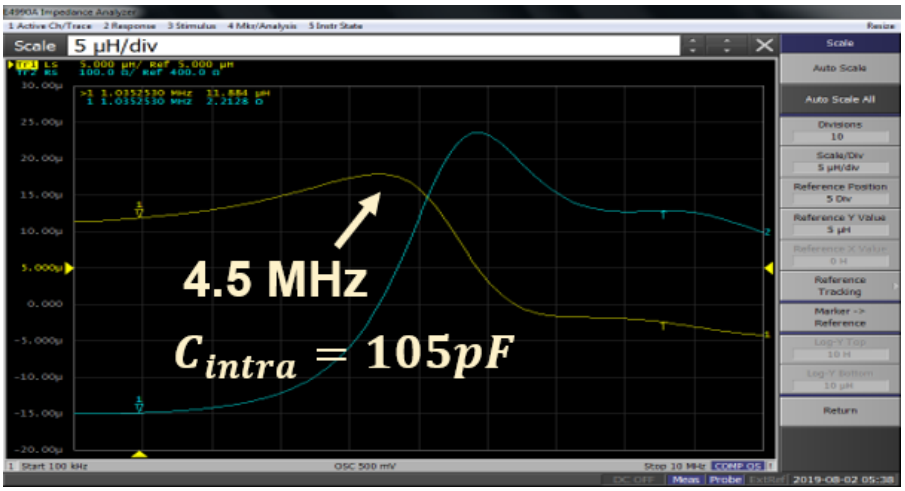

Fig. 5-19. Measuring results of the transformer with 4P3S, 1P4S structure.

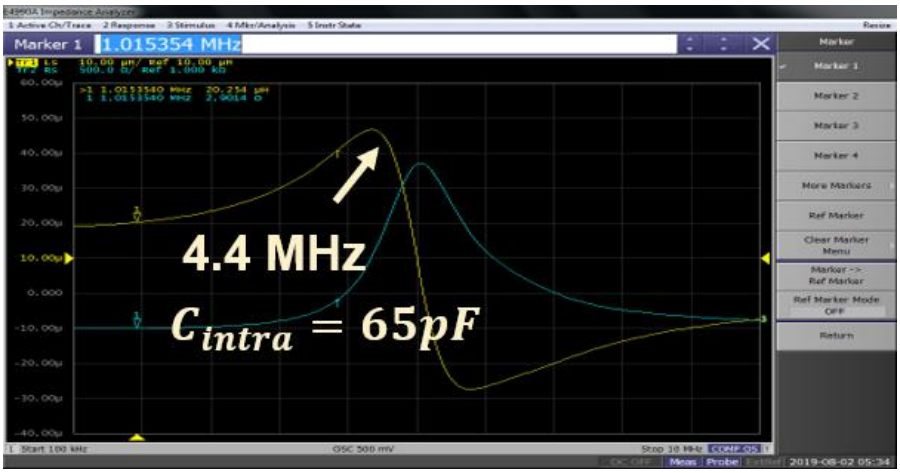

Fig. 5-20. Measuring results of the coupled inductor with 5P1S, 2P6S structure.

Chapter 6: Conclusions and Future Work

In this dissertation, a bi-directional onboard charger for electric vehicles based on GaN devices is introduced. By utilizing highly efficient GaN switches, operating the power electronics at MHz frequency, and implementing planar magnetics, the power density and the efficiency of the charger can be largely enhanced.

A totem-pole interleaved CRM PFC rectifier based on coupled inductor was firstly introduced in this work. With different coupling factors, the switching frequency variation range, input current ripple, and the current stress on the switches can be controlled. In addition, an extra turn-on time control is proposed to extend the ZVS operation to full input line cycle. A closed-loop control algorithm is designed to stabilize the phase difference between the two interleaved legs. Furthermore, the EMI filter design based on a varying frequency noise signal is analyzed. To exploit the size reduction, inclusion of an active buffer at the DC-link is investigated.

Next, a CLLC DC-DC converter is considered for the second stage of the charger, and a new "f-φ" control algorithm was proposed to reduce power loss at light load conditions and minimize the frequency range. An optimization design flow was introduced to determine the design parameters. Finally, a preliminary design and implementation of the proposed onboard charger is shown, with magnetic design, component selection and circuit simulation. Experimental results have shown 96.4% efficiency in heavy-load (3.3kW) and medium-load condition (2.48kW), and 94.2% efficiency in light-load condition (1.65kW).

This work extends the knowledge in high frequency, high power, and high density onboard charger design. The proposed design methodology and control strategy will

be a reference for future applications. Several future work could be done to further exploit the potential of the proposed system.

(1) An enhanced thermal management should be designed to extend the verification of the proposed prototype in higher power levels. Specifically, comprehensive thermal simulations and liquid cooling solutions should be exploited to efficiently dissipate the heat.

(2) Analysis can be extended on the relationship between the input current ripple and the size of the EMI filter. Based on the selected devices, an optimized PFC stage with small size and high efficiency could be further developed.

(3) Furthermore, this work presents the results of the DC-DC stage using open loop. A closed-loop control of the proposed "$f-\varphi$" control needs to be investigated and implemented. This could be challenging due to the existence of two variables and simultaneously maintaining stable operation.

Bibliography

[1] “It’s Official: We Now Have One Billion Vehicles On The Planet,” *Green Car Reports*. [Online]. Available: https://www.greencarreports.com/news/1065070_its-official-we-now-have-one-billion-vehicles-on-the-planet. [Accessed: 26-Jul-2018].

[2] “The number of cars worldwide is set to double by 2040,” *World Economic Forum*. [Online]. Available: https://www.weforum.org/agenda/2016/04/the-number-of-cars-worldwide-is-set-to-double-by-2040/. [Accessed: 26-Jul-2018].

[3] “Global EV Outlook 2018,” [Online]. Available: https://webstore.iea.org/global-ev-outlook-2018. [Accessed: 27-Jul-2018].

[4] O. Milman, “Vehicles are now America’s biggest CO2 source but EPA is tearing up regulations,” *The Guardian*, 01-Jan-2018.

[5] “Cars and trucks are America’s biggest climate problem for the 2nd year in a row - Vox.” [Online]. Available: https://www.vox.com/energy-and-environment/2018/1/11/16874696/greenhouse-gas-co2-target-2017-paris-trump. [Accessed: 27-Jul-2018].

[6] “transportation-white-paper-feb2018.pdf.” .

[7] “BP Statistical Review of World Energy.” [Online]. Available: https://www.bp.com/content/dam/bp/business-sites/en/global/corporate/pdfs/energy-economics/statistical-review/bp-stats-review-2018-full-report.pdf. [Accessed: 24-Jul-2019]

[8] “Lithium Ion NCR18650.” [Online]. Available: https://engineering.tamu.edu/media/4247819/ds-battery-panasonic-18650ncr.pdf. [Accessed: 24-Jul-2019]

[9] “Tesla 2170 Battery Cells: Greater Power At Comparable Cost.” [Online]. Available: https://insideevs.com/tesla-2170-battery-cells-greater-power-comparable-cost/. [Accessed: 02-Aug-2018].

[10] “Toyota Prius - Wikibooks, open books for an open world.” [Online]. Available: https://en.wikibooks.org/wiki/Toyota_Prius. [Accessed: 06-Aug-2018].

[11] “Electric Vehicle Battery: Materials, Cost, Lifespan,” *Union of Concerned Scientists*. [Online]. Available: https://www.ucsusa.org/clean-vehicles/electric-vehicles/electric-cars-battery-life-materials-cost. [Accessed: 02-Aug-2018].

[12] “Batteries 2017 Annual Progress Report,” p. 1145, 2017.

[13] “2018 Bolt EV: Electric Car | Electric Vehicle,” *Chevrolet*. [Online]. Available: www.chevrolet.com/index/vehicles/2018/cars/bolt-ev/overview.html. [Accessed: 05-Aug-2018].

[14] “Model 3 | Tesla.” [Online]. Available: https://www.tesla.com/model3. [Accessed: 05-Aug-2018].

[15] “GRIN - A Summary of Electric Vehicle Propulsion Technologies.” [Online]. Available: https://www.grin.com/document/277317. [Accessed: 05-Aug-2018].

[16] “Nissan Leaf - Wikiwand.” [Online]. Available: https://www.wikiwand.com/en/Nissan_Leaf. [Accessed: 05-Aug-2018].

[17] “Chevrolet Volt - Wikiwand.” [Online]. Available: https://www.wikiwand.com/en/Chevrolet_Volt. [Accessed: 05-Aug-2018].

[18] “2018 Bolt EV: Electric Car | Electric Vehicle,” *Chevrolet*. [Online]. Available: www.chevrolet.com/index/vehicles/2018/cars/bolt-ev/overview.html. [Accessed: 05-Aug-2018].
[19] “Tesla Model S - Wikiwand.” [Online]. Available: https://www.wikiwand.com/en/Tesla_Model_S. [Accessed: 06-Aug-2018].
[20] “The American Sedan Is Dying. Long Live the SUV,” *Bloomberg.com*, 16-Jan-2018.
[21] “ST targets Electric Vehicles with SiC power devices,” *eeNews Power*, 17-May-2016. [Online]. Available: http://www.eenewspower.com/news/st-targets-electric-vehicles-sic-power-devices. [Accessed: 06-Aug-2018].
[22] A. Avron, “About the SiC MOSFETs modules in Tesla Model 3,” *PntPower*, 27-Jun-2018. .
[23] “Chevy EV Life: Bolt EV Charging Guide | Chevrolet,” *Chevy EV Life: Bolt EV Charging Guide | Chevrolet*. [Online]. Available: https://www.chevyevlife.com/bolt-ev-charging-guide. [Accessed: 06-Aug-2018].
[24] “15 minute charge for a 300 mile range? DOE moves to boost EVs,” *Utility Dive*. [Online]. Available: https://www.utilitydive.com/news/15-minute-charge-for-a-300-mile-range-doe-moves-to-boost-evs/522653/. [Accessed: 06-Aug-2018].
[25] “ABB selected by Electrify America to provide high power electric vehicle chargers across the United States.” [Online]. Available: https://new.abb.com/news/detail/4283/abb-selected-by-electrify-america-to-provide-high-power-electric-vehicle-chargers-across-the-united-states?utm_source=social-media. [Accessed: 06-Aug-2018].
[26] “UK Study Says 20% Of Parking Spots Need Charging Points.” [Online]. Available: https://insideevs.com/uk-study-says-20-of-parking-spots-need-charging-points/. [Accessed: 26-Jul-2018].
[27] “China wants 40% of new car sales to be electric by 2030.” [Online]. Available: https://www.motor1.com/news/127872/china-ev-autonomous-forecast-2030/. [Accessed: 07-Aug-2018].
[28] D. Roberts, “The world’s largest car market just announced an imminent end to gas and diesel cars,” *Vox*, 13-Sep-2017. [Online]. Available: https://www.vox.com/energy-and-environment/2017/9/13/16293258/ev-revolution. [Accessed: 07-Aug-2018].
[29] W. M. Business, “The death of the internal combustion engine,” *Huffington Post*, 09-Dec-2016. .
[30] S. Castle, “Britain to Ban New Diesel and Gas Cars by 2040,” *The New York Times*, 22-Dec-2017.
[31] F. Lambert, “VW announces new plan to build 2 to 3 million all-electric cars a year by 2025,” *Electrek*, 16-Jun-2016. .
[32] “GM’s Path to an All-Electric, Zero Emissions Future.” [Online]. Available: https://www.gm.com/mol/m-2018-mar-0307-barra-speech.html. [Accessed: 06-Aug-2018].
[33] “Electric Car Mileage Share Expected To Hit 20% By 2030.” [Online]. Available: https://insideevs.com/electric-car-mileage-share/. [Accessed: 13-Aug-2018].

[34] “Electrical and Electronics Technical Team Roadmap.”[Online]. Available: https://www.energy.gov/sites/prod/files/2017/11/f39/EETT%20Roadmap%2010-27-17.pdf. [Accessed: 13-Aug-2018].
[35] I. C. Kizilyalli, Y. A. Xu, E. Carlson, J. Manser, and D. W. Cunningham, “Current and future directions in power electronic devices and circuits based on wide band-gap semiconductors,” in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 417–417.
[36] B. Whitaker *et al.*, “A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2606–2617, May 2014.
[37] B. Li, Q. Li, F. C. Lee, Z. Liu, and Y. Yang, “A High-Efficiency High-Density Wide-Bandgap Device-Based Bidirectional On-Board Charger,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1627–1636, Sep. 2018.
[38] R. Yu, Q. Huang, T. Chen, A. Q. Huang, and T. Ribarich, “High-Frequency and High-Density Design of all GaN Power Supply Unit,” in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–5.
[39] Q. Huang and A. Q. Huang, “Review of GaN totem-pole bridgeless PFC,” *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 187–196, Sep. 2017.
[40] P. He, A. Mallik, A. Sankar, and A. Khaligh, “Design of a 1-MHz High-Efficiency High-Power-Density Bidirectional GaN-Based CLLC Converter for Electric Vehicles,” *IEEE Transactions on Vehicular Technology*, pp. 1–1, 2018.
[41] Y. Wu, M. Jacob-Mitos, M. L. Moore, and S. Heikman, “A 97.8% Efficient GaN HEMT Boost Converter With 300-W Output Power at 1 MHz,” *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 824–826, Aug. 2008.
[42] Z. Liu, Z. Huang, F. C. Lee, Q. Li, and Y. Yang, “Operation analysis of digital control based MHz totem-pole PFC with GaN device,” in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, USA, 2015, pp. 281–286.
[43] M. Fu, C. Fei, Y. Yang, Q. Li, and F. Lee, “Optimal Design of Planar Magnetic Components for A Two-Stage GaN-Based DC/DC Converter,” *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.
[44] X. Xu and A. Q. Huang, “A novel closed loop interleaving strategy of multiphase critical mode boost PFC converters,” in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, 2008, pp. 1033–1038.
[45] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, “Design of GaN-Based MHz Totem-Pole PFC Rectifier,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 799–807, Sep. 2016.
[46] F. Yang, X. Ruan, M. Xu, and Q. Ji, “Designing of coupled inductor in interleaved critical conduction mode boost PFC converter,” in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 1876–1882.
[47] J. Zhang, J. Shao, P. Xu, F. C. Lee, and M. M. Jovanovic, “Evaluation of input current in the critical mode boost PFC converter for distributed power systems,”

in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, 2001, vol. 1, pp. 130–136 vol.1.
[48] M. Hartmann, S. D. Round, H. Ertl, and J. W. Kolar, "Digital Current Controller for a 1 MHz, 10 kW Three-Phase VIENNA Rectifier," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2496–2508, Nov. 2009.
[49] Z. Zhang, P. Xu, and Y. Liu, "Adaptive Continuous Current Source Drivers for 1-MHz Boost PFC Converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2457–2467, May 2013.
[50] S. Nibir, M. Biglarbegian, and B. Parkhideh, "A Non-Invasive DC-10MHz Wideband Current Sensor for Ultra-Fast Current Sensing in High Frequency Power Electronic Converters," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.
[51] "Magnetics - L Material." [Online]. Available: https://www.mag-inc.com/Products/Ferrite-Cores/L-Material. [Accessed: 10-Dec-2018].
[52] "3F36 Material specification." [Online]. Available: https://www.ferroxcube.com/upload/media/product/file/MDS/3f36.pdf. [Accessed: 10-Dec-2018].
[53] "Benefits of Planar." [Online]. Available: http://www.paytongroup.com/webfiles/files/Benefits%20of%20Planar.pdf. [Accessed: 10-Dec-2018].
[54] F. Musavi, W. Eberle, and W. G. Dunford, "A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1833–1843, Jul. 2011.
[55] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 799–807, Sep. 2016.
[56] L. Huber, B. T. Irving, and M. M. Jovanovic, "Open-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1649–1657, Jul. 2008.
[57] "SIM800_FCC_Part15.pdf." .
[58] M. Mellincovsky, V. Yuhimenko, Q. Zhong, M. M. Peretz, and A. Kuperman, "Active DC Link Capacitance Reduction in Grid-Connected Power Conversion Systems by Direct Voltage Regulation," *IEEE Access*, vol. 6, pp. 18163–18173, 2018.
[59] M. Mellincovsky, V. Yuhimenko, M. M. Peretz, and A. Kuperman, "Analysis and Control of Direct Voltage Regulated Active DC-Link Capacitance Reduction Circuit," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6318–6332, Jul. 2018.
[60] P. He, "High-Frequency Bidirectional DC-DC Converters for Electric Vehicle Applications," 2018.
[61] "Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters - IEEE Journals & Magazine." [Online]. Available: https://ieeexplore.ieee.org/document/5776689. [Accessed: 05-Dec-2018].
[62] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified Triple-Phase-Shift Control to Minimize Current Stress and Achieve Full Soft-Switching of Isolated

Bidirectional DC–DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.
[63] Y. Tang, J. Lu, B. Wu, S. Zou, W. Ding, and A. Khaligh, "An Integrated Dual-Output Isolated Converter for Plug-in Electric Vehicles," *IEEE Transactions on Vehicular Technology*, vol. 67, no. 2, pp. 966–976, Feb. 2018.
[64] C. Fei, Q. Li, and F. C. Lee, "Digital Implementation of Adaptive Synchronous Rectifier (SR) Driving Scheme for High-Frequency LLC Converters With Microcontroller," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5351–5361, Jun. 2018.
[65] C. Zhao, M. Chen, G. Zhang, X. Wu, and Z. Qian, "A Novel Symmetrical Rectifier Configuration With Low Voltage Stress and Ultralow Output-Current Ripple," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1820–1831, Jul. 2010.
[66] A. Sankar, A. Mallik, and A. Khaligh, "Extended Harmonics Based Phase Tracking for Synchronous Rectification in CLLC converters," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2018.
[67] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "Bi-Directional CLLC Converter With Synchronous Rectification for Plug-In Electric Vehicles," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 998–1005, Mar. 2018.
[68] C. Duan, H. Bai, W. Guo, and Z. Nie, "Design of a 2.5-kW 400/12-V High-Efficiency DC/DC Converter Using a Novel Synchronous Rectification Control for Electric Vehicles," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 106–114, Jun. 2015.
[69] A. K. S. Bhat, "A generalized steady-state analysis of resonant converters using two-port model and Fourier-series approach," *IEEE Transactions on Power Electronics*, vol. 13, no. 1, pp. 142–151, Jan. 1998.
[70] and, K. Colombage, C. Gould, and B. Sen, "A CLLC resonant converter based bidirectional EV charger with maximum efficiency tracking," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, 2016, pp. 1–6.
[71] H. Wang, S. Dusmez, and A. Khaligh, "Maximum Efficiency Point Tracking Technique forLLC-Based PEV Chargers Through Variable DC Link Control," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 11, pp. 6041–6049, Nov. 2014.
[72] B. Li, Q. Li, F. C. Lee, Z. Liu, and Y. Yang, "A High-Efficiency High-Density Wide-Bandgap Device-Based Bidirectional On-Board Charger," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1627–1636, Sep. 2018.
[73] Q. Cao, Z. Li, B. Xue, and H. Wang, "Fixed Frequency Phase Shift Modulated LLC Resonant Converter Adapted to Ultra Wide Output Voltage Range," p. 6.
[74] M. Shang and H. Wang, "A LLC type resonant converter based on PWM voltage quadrupler rectifier with wide output voltage," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1720–1726.
[75] H. Wang and Z. Li, "A PWM LLC Type Resonant Converter Adapted to Wide Output Range in PEV Charging Applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3791–3801, May 2018.

[76] Z. Li and H. Wang, “Design of a secondary side regulated LLC based integrated PEV onboard charger with full ZVS range,” in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1394–1400.
[77] P. He, A. Mallik, A. Sankar, and A. Khaligh, “Design of a 1-MHz High-Efficiency High-Power-Density Bidirectional GaN-Based CLLC Converter for Electric Vehicles,” *IEEE Transactions on Vehicular Technology*, vol. 68, no. 1, pp. 213–223, Jan. 2019.