# ABSTRACT

Title of dissertation: NOVEL MATERIALS AND STRUCTURES FOR WIDE AND ULTRA-WIDE BANDGAP SEMICONDUCTOR SWITCHES

David Issa Shahin, Doctor of Philosophy, 2018

Dissertation directed by: Professor Aristos Christou
Materials Science and Engineering

Semiconductor power switches are necessary for the deployment of next-generation electrical systems, including renewable energy generators, electric vehicle drivetrains, and high-power communications systems. Current silicon-based technologies are limited by insufficient blocking voltages due to bandgap limitations and processing-induced defects, undesirably high on-state resistances due to gate charge trapping at poorly understood dielectric/semiconductor interfaces, and limited reliability due to electrical and thermal failure under aggressive operating conditions. As such, new materials and device architectures are required to achieve previously unattained power, efficiency, and reliability.

This dissertation identifies and investigates material candidates and demonstrates their incorporation into new device architectures for power switches. Wide bandgap (WBG) semiconductors such as GaN, and ultra-wide bandgap (UWBG) semiconductors such as $\beta$-$Ga_2O_3$ and diamond are employed to address the previously stated limitations. Gate charge trapping in these systems is addressed through use of high-k dielectrics not previously employed for WBG and UWBG switches. $ZrO_2$ and $HfO_2$ dielectrics are presented as candidates for dielectric and interface charge tuning on GaN and $Ga_2O_3$, thereby allowing

the possibility of threshold voltage manipulation and normally-off behavior in WBG and UWBG switches.

Fabrication technologies for WBG and UWBG switches are also reported. Normally-on and -off AlGaN/GaN MOS-HEMTs with threshold voltages between -3 to +4 V are demonstrated through a combination of $ZrO_2$ dielectric selection and AlGaN recess etching. Design and processing for normally-off vertical GaN MOSFETs are also developed, with emphasis on critical challenges in fabricating these devices. Additionally, the fabrication and stability of hydrogen-terminated diamond switches with $Al_2O_3$ surface transfer dopants are reported.

Finally, new materials and processes for improved electrical and thermal stability in power switches are demonstrated. TiN is presented as a reliable gate electrode for AlGaN/GaN HEMTs, imparting superior resistance to reverse gate bias electrical stress and temperatures up to 800 °C that otherwise destroyed conventional Ni/Au-gated HEMTs. A novel process for plasma-free selective area etching of nanocrystalline diamond heat spreading films is also presented, which promises to avoid plasma damage to the underlying semiconductor and enables etching of diamond films along features inaccessible to a typical plasma-based process.

# NOVEL MATERIALS AND STRUCTURES FOR WIDE AND ULTRA-WIDE BANDGAP SEMICONDUCTOR SWITCHES

by

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# Dedication

To my beloved wife Katie, and our Baby Kat.

And to The Count.

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Lastly, I thank my wife, Katie, for accompanying me on this journey. She has been my steadfast companion through it all, sharing in my successes, and helping me regain my footing after my failures. It is for her and our future that I chose to embark on my doctoral education, and because of her that I have completed it. I owe her and thank her for everything.

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# List of Abbreviations

| | |
|---|---|
| **2DEG** | two-dimensional electron gas |
| **2DHG** | two-dimensional hole gas |
| **AC** | alternating current |
| **AFM** | atomic force microscopy |
| **ALD** | atomic layer deposition |
| **BFOM** | Baliga's Figure of Merit |
| **C-V** | capacitance-voltage |
| **CAD** | computer-aided design |
| **CAVET** | current aperture vertical electron transistor |
| **CBO** | conduction band offset |
| **CL** | cathodoluminescense |
| **CTLM** | circular transfer length method |
| **CVD** | chemical vapor deposition |
| **CZ** | Czochralski |
| **DC** | direct current |
| **DLTS** | deep-level transient spectroscopy |
| **EFG** | edge-defined film-fed growth |
| **F-N** | Fowler-Nordheim |
| **FET** | field effect transistor |
| **FIB** | focused ion beam |
| **FWHM** | full width at half maximum |
| **HEMT** | high electron mobility transistor |
| **HPHT** | high pressure high temperature |
| **HVPE** | hydride vapor phase epitaxy |
| **I-V** | current-voltage |
| **ICP** | inductively-coupled plasma |
| **LED** | light emitting diode |
| **MBE** | molecular beam epitaxy |
| **MIS** | metal-insulator-semiconductor |
| **MOCVD** | metal-organic chemical vapor deposition |
| **MOS** | metal-oxide-semiconductor |
| **MW-CVD** | microwave plasma chemical vapor deposition |
| **NCD** | nanocrystalline diamond |
| **NEA** | negative electron affinity |

| | |
|---|---|
| **P-F** | Poole-Frenkel |
| **PECVD** | plasma-enhanced chemical vapor deposition |
| **PL** | photoluminescense |
| **RF** | radio frequency |
| **RIE** | reactive ion etching |
| **RMS** | root-mean-square |
| **RTA** | rapid thermal annealing |
| **SBD** | Schottky barrier diode |
| **SCLC** | space charge limited current |
| **SEM** | scanning electron microscopy |
| **TAT** | trap-assisted tunneling |
| **TDMAZ** | tetrakis(dimethylamido)-zirconium(IV) |
| **TLM** | transfer length method |
| **TMAH** | tetramethylammonium hydroxide |
| **UV** | ultraviolet |
| **UWBG** | ultra-wide bandgap |
| **VdP** | Van der Pauw |
| **WBG** | wide bandgap |
| **XPS** | x-ray photoelectron spectroscopy |
| **ZTB** | zirconium(IV) *tert*-butoxide |

# PART I
# INTRODUCTION

# Chapter 1: Introduction

## 1.1 Problem Statement and Summary of Contributions

Modern society has come to depend on the effective and efficient control of electricity. Many current and future electrical systems, including grid-scale energy generation, storage, and transmission systems, electric vehicle drivetrains, and high-power communications systems, depend on the development of innovative and reliable solid-state semiconductor power switches. Current power switch technologies suffer from (1) insufficient off-state blocking voltages due to bandgap limitations, material and processing defects, and normally-on behavior, (2) high on-resistances due to charge trapping effects, and (3) premature failure due to electrical and thermal degradation. To enable power switches with previously unattainable power, efficiency, and reliability characteristics, new materials, device architectures, and fabrication processes are required.

The scholarly contribution of this dissertation is to identify and investigate novel materials for incorporation into power switches based on technologically important wide bandgap (WBG) semiconductors such as GaN, and ultra-wide bandgap (UWBG) semiconductors such as $\beta$-$Ga_2O_3$ and diamond. These semiconductors exhibit increasingly larger bandgaps and critical electric field strengths, leading to drastically higher values of Baliga's Figure of Merit (BFOM) for power devices, and thus enabling switches with lower on-state resistances and higher off-state blocking voltages than other semiconductors such as Si and SiC.

This dissertation addresses charge trapping and other gate dielectric effects in

WBG/UWBG systems through study of new dielectric systems not previously employed for high voltage switches. Specifically, $ZrO_2$ and $HfO_2$ high-k dielectrics deposited by atomic layer deposition (ALD) are presented. Two $ZrO_2$ precursor systems, zirconium(IV) *tert*-butoxide (ZTB) and tetrakis(dimethylamido)-zirconium(IV) (TDMAZ), are compared for integration with device-relevant crystal planes of n-type GaN and $Ga_2O_3$ using metal-oxide-semiconductor (MOS) capacitors. On both GaN and $Ga_2O_3$, ZTB-$ZrO_2$ films exhibited positive flatband voltage shifts, indicative of negative fixed oxide or interfacial charge, while TDMAZ-$ZrO_2$ films had much less fixed charge. These characteristics allow gate charge tuning for normally-off power switches through appropriate materials selection, as discussed later in this work. In addition, $HfO_2$ films have been produced on $(\bar{2}01)$ $\beta$-$Ga_2O_3$ with superior electrical interface characteristics, including one of the lowest measures of interface trapped charge of any oxide dielectric on $Ga_2O_3$ reported to date. This indicates that $HfO_2$ is an attractive candidate gate oxide for emerging high performance UWBG power switches.

Device architectures and fabrication technologies for WBG switches are also reported in this dissertation. These include demonstration of AlGaN/GaN MOS-high electron mobility transistors (HEMTs) with tunable threshold voltages between $V_t$ = -3 to +4 V achieved through a combination of $ZrO_2$ dielectric selection and AlGaN barrier recess etching. These technologies stand to enable normally-off AlGaN/GaN HEMTs, a critical characteristic for fail-safe WBG power switches. For higher power switching capabilities, critical design and processing challenges for normally-off vertical GaN MOSfield effect transistors (FETs) on a custom vertical $n^+/p^+/n^-$ epitaxial structure are also reported.

Additionally, UWBG power switch technology based on diamond is demonstrated through formation of two-dimensional conducting channels through surface transfer doping

of hydrogen terminated diamond surfaces. These technologies are used to produce p-channel transistors on ultra-smooth, low defectivity diamond substrates. Switches on hydrogen-terminated diamond with $Al_2O_3$ as a surface transfer dopant exhibited normally-on behavior and relatively stable current output over the course of one week.

The final part of this dissertation demonstrates novel materials and processes for improved electrical and thermal stability, as next-generation power switches will require new strategies for controlling the tremendous electrical and thermal stresses encountered during operation. ALD-deposited TiN is presented as an electrically and thermally stable gate electrode for AlGaN/GaN HEMTs. TiN-gated devices exhibited improved output and superior resistance to electrical gate stresses and high temperatures that destroyed conventional Ni/Au-gated HEMTs. Additionally, a novel process is presented for plasma-free selective area patterning and etching of nanocrystalline diamond (NCD) heat spreading films for power devices. Through use of an oxygen atmosphere at elevated temperatures (700–800 °C), this process enables selective etching of diamond films without plasma damage and thus without performance degradation in the underlying semiconductor, while also enabling the possibility of etching along vias and other features inaccessible to a typical plasma etch.

The significance of the research presented hereafter has been recognized through multiple scholarly works produced as part of the author's doctoral research program. This dissertation contains material adapted from papers accepted by *Applied Physics Letters*, *ECS Transactions*, *ECS Journal of Solid State Science and Technology*, *Diamond and Related Materials*, and extended abstracts at the International Conference on Compound Semiconductor Manufacturing Technology (CS-MANTECH), with additional manuscripts

currently in preparation [1–9]. In total, the author has made significant contributions to 16 journal publications, 29 conference presentations, and one U.S. Patent. A complete listing of all scholarly publications, presentations, and patents authored or co-authored as part of this work can be found in Appendix A.

## 1.2 Background on Power Electronics

Next-generation power semiconductor switches are critical to disruptive advances in grid-scale switching, renewable energy generation and storage, electric vehicle drivetrains, high speed wireless communications, and defense applications [10–14]. These switches, especially power FETs, must be capable of withstanding high off-state blocking voltages and high on-state currents with minimal switching and on-state losses in order to maximize efficiency. Normally-off behavior (i.e. the switch is in the off-state at zero gate bias) is strongly desired to make power switches fail-safe. Low gate and off-state leakage is also needed in order to reduce inefficiency from off-state losses. Power switches must also function for extended durations under extreme conditions, including in elevated temperature and high radiation environments [15–17]. Si-based electronics, arguably the workhorses of semiconductor devices, cannot adequately address these requirements due to high on-resistances ($R_{on}$), slow switching speeds, and junction temperature limitations. To address these limitations, WBG semiconductors such as GaN, and UWBG semiconductors such as $Ga_2O_3$ and diamond must be employed, due to their large bandgaps ($E_g$), large critical electric field strenghts ($E_c$), and high carrier mobilities ($\mu$). Representative values of important electrical properties for these WBG and UWBG materials are shown in Table 1.1, along

with those of Si and SiC for comparison. The listed material properties render the WBG and UWBG semiconductors superior to competing Si and SiC when assessed using the BFOM (normalized to Si) value for power device materials [18, 19]. Other figures of merit for high power, high frequency, and high temperature electronics detailed elsewhere also find the WBG and UWBG materials to be superior for these applications [20]. Theoretically, then, these materials are ideal for withstanding the high voltage, high current, and high temperature conditions required by the current and future power switching applications, while also supporting higher efficiencies and smaller device footprints [21].

Table 1.1. Important properties of wide and ultra-wide bandgap semiconductors. (Data from [22–24].)

| Material | $E_g$ (eV) | $\mu$ ($cm^2V^{-1}s^{-1}$) | $E_c$ (MV/cm) | BFOM ($\epsilon_r\mu_n E_c^3$) | $k_{Thermal}$ (W/cm·K) |
|---|---|---|---|---|---|
| Si | 1.1 | 1350 (n) | 0.3 | 1 | 1.5 |
| SiC | 3.3 | 700 (n) | 2.0 | 130 | 4.5 |
| GaN | 3.4 | >900 (n) | 3.3 | >714 | 1.3 |
| $Ga_2O_3$ | 4.8 | <300 (n) | 8 | 3571 | 0.3 |
| Diamond | 5.5 | 3800 (p) | 10 | 48592 | 22 |

The superior properties of the WBG and UWBG semiconductors are demonstrated for practical power switch designs by plotting the ideal on-resistance ($R_{on,ideal}$) as a function of breakdown (blocking) voltage ($V_{br}$), given by Eqn. 1.1:

$$R_{on,ideal} = \frac{4 \cdot {V_{br}}^2}{\mu \cdot \epsilon_{sc} \cdot {E_c}^3} \tag{1.1}$$

where $\mu$ is the majority carrier mobility, $\epsilon_{sc}$ is the permittivity of the semiconductor, and the other values are as defined earlier in this section. Fig. 1.1 shows the relationship in Eqn. 1.1

on a plot of $R_{on,ideal}$ versus $V_{br}$ for the WBG and UWBG semiconductors discussed in this dissertation, along with Si and SiC for comparison. Note that the denominator term is the BFOM. Thus, power switches produced from the WBG and UWBG semiconductors can (in theory) attain higher $V_{br}$ and lower $R_{on}$, thereby achieving higher power and efficiency levels than are possible with the current generation of semiconductor power switches.

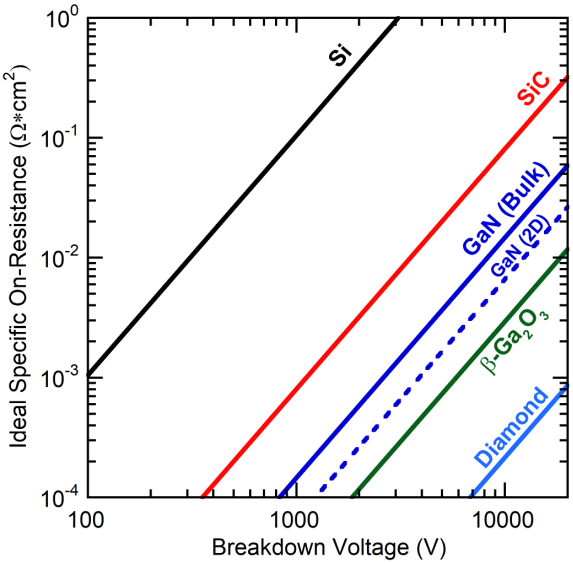


Fig. 1.1. Theoretical $R_{on}$–$V_{br}$ relationships for important power semiconductor materials.

## 1.3 Wide Bandgap GaN Power Switches: Current Status and Critical Issues

### 1.3.1 GaN Background

Of the three semiconductor technologies addressed in this dissertation, GaN materials and device technology are by far the most mature, with commercial production and use of GaN switches in both power and radio frequency (RF) systems. Combined with GaN-based light emitting diodes (LEDs), the global market for GaN devices is projected to grow to over

$3.4 billion by the year 2024 [25]. Useful GaN semiconductor devices are produced with the wurtzite (hexagonal) GaN polytype, as shown in Fig. 1.2.

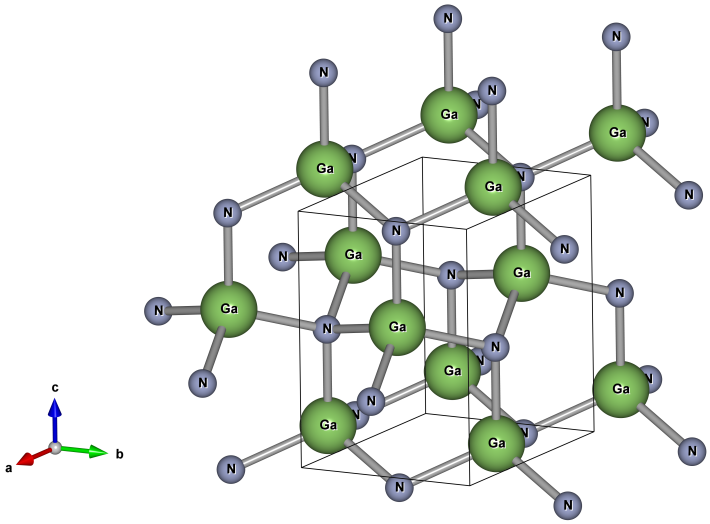


Fig. 1.2. Ball-and-stick model of the primitive unit cell for wurtzite (2H) GaN. (Model created using VESTA software [26] and data from [27].

Device-quality GaN thin films are commonly grown by metal-organic chemical vapor deposition (MOCVD) on foreign substrates with similar crystal structures, such as sapphire, SiC, or (111) Si. Mature production technology for these foreign substrates enabling the manufacture of low-cost, large-area GaN films (up to 8" diameter on Si) that are compatible with standard Si foundry hardware [28]. However, lattice and thermal expansion mismatches between these foreign substrates and the GaN epitaxial films can be significant, and even with the incorporation of complex nucleation layer schemes, still yield threading dislocation densities between $10^6$–$10^9$ dislocations/cm$^2$ [29]. These dislocations have been shown to act as charge traps and leakage pathways that can degrade device performance and contribute to premature failure [30–32]. More recently, bulk GaN substrates grown by hydride vapor phase epitaxy (HVPE) or ammonothermal growth have become commercially

available. Use of native GaN substrates allows growth of GaN epitaxial films with much lower dislocation densities ($<10^4$ cm$^{-2}$) and demonstrated improvements in on- and off-state device characteristics [33–35]. However, additional complexities are introduced by use of bulk GaN substrates. Chief among these issues is material size and cost. While 6" SiC and 8" Si wafers are commonly used as substrates for epitaxial GaN films, currently only 2–3" diameter bulk GaN wafers are commercially available due to the relative complexity of GaN bulk growth processes. These small bulk GaN wafers are also very expensive ($1000s for a 2" substrate). Larger bulk substrates (4–6" diameter) are currently being developed and should drive costs downward as production technology and adoption rate improves [36]. Thermal conductivity of bulk GaN relative to foreign substrates is also an issue for efficient and reliable GaN power switches of any geometry: GaN exhibits a thermal conductivity nearly equivalent to Si, but over three times less than that of SiC [22]. Additionally, the thermal conductivity of GaN substrates and films varies based on the quality and defectivity of the material [36]. Development of methods for effective heat dissipation is thus a paramount concern for all GaN switch architectures, with integration of NCD heat spreading films [37], backside vias/cooling channels [38], heatsink design [39], and transfer or growth of GaN films onto high thermal conductivity substrates (diamond) [40,41] all under investigation. In addition, the HVPE and ammonothermal processes use radically different growth conditions which may impact GaN epilayer quality and defectivity during subsequent MOCVD growth or other high temperature processes [42,43].

### 1.3.2 GaN Switches: High Electron Mobility Transistors

The most common GaN power switch architecture commercially available is the lateral AlGaN/GaN HEMT. The HEMT structure, shown schematically in Fig. 1.3, was first demonstrated by Asif Khan et al. in 1993 [44]. AlGaN/GaN HEMTs are well-suited for low- to moderate-power switches (<650 V) due to extremely low $R_{on}$ values, achieved through the two-dimensional electron gas (2DEG) formed in the quantum well at the c-plane AlGaN/GaN interface [45, 46]. As such, electron conduction along the 2DEG does not suffer from impurity scattering effects, allowing excellent device output and rapid switching characteristics [47].

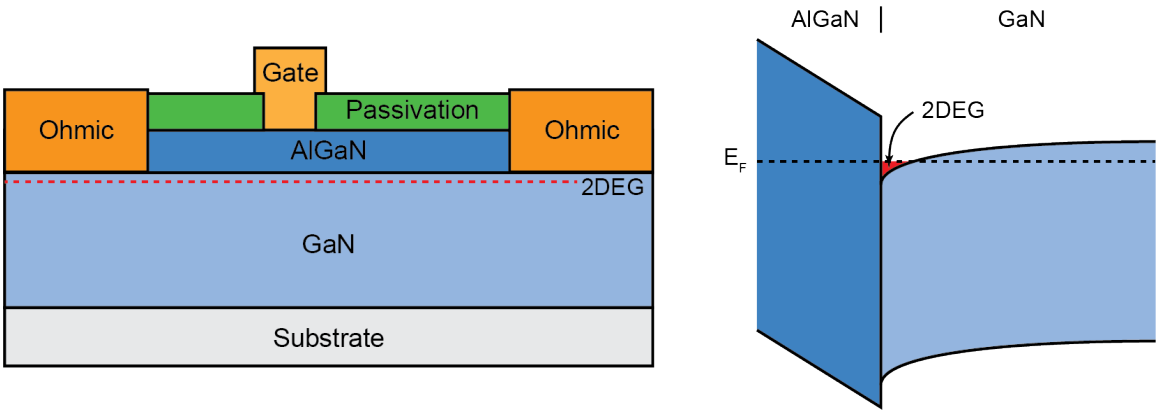


Fig. 1.3. Schematic of a standard AlGaN/GaN HEMT device with associated band diagram.

Despite reports of excellent device characteristics and relatively simple fabrication processes (to be described later in this dissertation), HEMTs suffer from several key limitations that must be addressed for high power switches:

- First, the natural existence of the 2DEG in the absence of any gate bias means that these devices are typically normally-on (depletion-mode), which is an undesirable

characteristic for fail-safe power switches [14]. Normally-off (enhancement-mode) GaN HEMTs have been realized in various ways, including local recess etching of the AlGaN barrier layer underneath the gate, incorporation of p-doped GaN or charged dielectric layers as part of the gate stack, and combination of GaN HEMTs and Si MOSFETs in a cascode-type device arrangement [48–52]. Several companies have recently brought normally-off GaN HEMTs to market based on these technologies, including EPC and TransPhorm [46]. Still, development of new technologies in this area is a key priority for fail-safe and reliable power switches.

- The prototypical GaN HEMT relies on a Schottky metal gate structure (i.e. Ni metal) to the AlGaN barrier layer. While metal-semiconductor gates are good for fast and effective channel modulation, they suffer from high gate leakage effects, especially when forward biased (gate-source voltage $>$ +1 V). Incorporation of insulating gate dielectrics significantly reduces leakage current, but also tend to make the devices even more normally-on (negative threshold voltage shift) due to the effective increase in barrier thickness between the gate electrode and the 2DEG channel [53–55]. Additionally, Schottky metal gates have been shown to degrade under intense electrical and thermal stresses, presenting a reliability concern in AlGaN/GaN HEMTs [56–59].

- Lateral near-surface conduction requires tradeoffs between breakdown voltage, device size, and on-resistance. Effective surface state passivation schemes are also required for optimal performance, as electron trapping in the gate-drain access region leads to the formation of a "virtual gate" over the 2DEG that reduces device output and can

contribute to reduced reliability [60–62].

### 1.3.3 GaN Switches: Vertical Metal-Oxide-Semiconductor Field Effect Transistors

To achieve higher power switching in GaN devices, vertical architectures must be employed. Vertical GaN switches incorporate thick, low-doped drift layers buried in the structure to stands off high drain biases in the off state. The blocking region is thus moved below the surface, allowing for maximum performance, alleviating the need for complex passivation schemes, and allowing for a reduced device footprint over a comparable lateral device. A variety of vertical switch geometries are being explored, including MOSFETs [63], finFETs [64], and current aperture vertical electron transistors (CAVETs) [65]. Of these, the ideal high power switch structure for achieving both normally-off behavior and high $V_{br}$ is the trench-gate MOSFET, shown in Fig. 1.4.

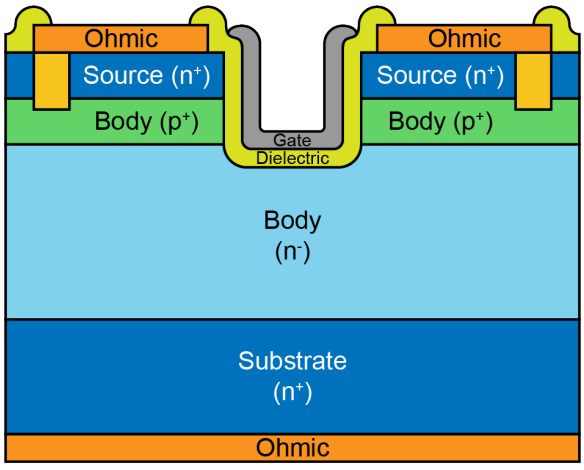


Fig. 1.4. Cross-section of a vertical trench-gate GaN MOSFET.

The trench-gate MOSFET structure benefits from the buried gate, lack of a parasitic

junction FET (JFET) in the middle of the device, and the ability to create the necessary device regions with only doped epilayers. The first trench-gate vertical GaN MOSFET was demonstrated in 2007 [66]. Since then, breakdown voltages up to 1600 V and on-resistances of 1–2 $m\Omega \cdot cm^2$ have been achieved in state-of-the-art vertical GaN MOSFETs, which while impressive for GaN still fall short of the theoretical performance limits [63, 67–69]. Simpler devices such as vertical p-n diodes have achieved performance characteristics much closer to the theoretical limits, suggesting that with appropriate optimizations, further improvements in vertical GaN switches can be achieved [70, 71]. Selected issues in vertical GaN MOSFETs relevant to this dissertation research are discussed below:

- Cl-based plasma etching is required to create the trench gate feature due to the lack of isotropic wet etchants for GaN. Plasma etching for these features (on the order of hundreds to thousands of nm) can create electrically-active defects such as N vacancies that cause charge trapping and increased $R_{on}$ in the on-state, and increased leakage currents and reduced $V_{br}$ in the off-state [72–74]. This damage must be reduced to increase the performance and reliability of vertical MOSFETs switches. Some studies have focused on reducing this damage through adjustments to the plasma etch process itself (gas flow rates, plasma powers, pre-etch processes, mask selection, etc.) and assessment of the resulting etched surfaces with scanning electron microscopy (SEM), atomic force microscopy (AFM), and photoluminescense (PL) or cathodoluminescense (CL) measurements [75–78]. Other work has focused on use of wet treatments to remove damaged GaN after etching. Chemicals such as tetramethylammonium hydroxide (TMAH) have shown promise for selective sidewall

etching/cleanup. TMAH rapidly attacks non-c- and non-m-plane GaN, leading to the formation of vertical m-plane facets along etched features [78, 79]. However, damage cleanup with TMAH unfortunately preculdes the option of comparing m- and a-plane oriented trench MOSFETs.

- Many dielectrics have been studied or at least suggested for GaN devices, including $SiO_2$, $Al_2O_3$, $HfO_2$, and $ZrO_2$ [80]. These dielectrics have been studied in a variety of device architectures (MOSFETs, HEMTs, MOS-capacitors) on polar c-plane (0001) GaN surfaces, as c-plane GaN far and away the most common substrate orientation available. In a vertical trench-gate MOSFET, however, the MOS interface along the n-channel will be formed with etched nonpolar a- and m-planes (the $(11\bar{2}0)$ and $(1\bar{1}00)$ planes, respectively), as shown in Fig. 1.5. These interfaces have a significant effect on $R_{on}$ of the resulting device [72]. Almost no study of dielectric interfaces with these planes has been performed due to the difficulty in obtaining high quality large area substrates of these orientations, which must be cut from a thick c-plane GaN wafer [81, 82]. Furthermore, few studies have been undertaken to characterize and optimize the dielectric interface with the etched c-plane GaN at the bottom of the trench gate [83]. Understanding these interfaces is essential for improved vertical GaN MOSFETs.

- Dopant control and the ability to fabricate and maintain regions of controlled carrier concentration is essential for vertical GaN MOSFETs. Dopants must either be incorporated during material growth or using ion implantation due to the difficulty in diffusion-doping GaN [84]. p-type doping is particularly difficult, as GaN typically

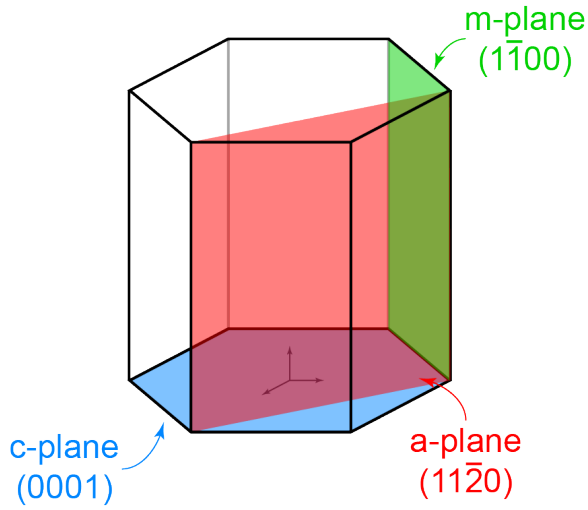


Fig. 1.5. Orientation of polar c- and nonpolar a- and m-planes in the hexagonal GaN crystal structure.

contains some level of unintentional n-type dopants (Si and O, recently traced to contamination from quartz reactor parts during growth [85]) and the most commonly used p-dopant, Mg, occupies a deep acceptor level 160 meV from the valence band [86]. MOCVD-grown p-GaN suffers from formation of H-Mg complexes that passivate the acceptors [87, 88]. Selectively implanted Mg activation is also low ($< 10\%$) even after complex annealing processes at temperatures above 1300 °C [86, 89]. Making Ohmic contacts to p-GaN layers is accordingly difficult and contact schemes vary widely [87].

- Epitaxial material quality for the low-doped blocking region has a strong influence on the breakdown voltage and measured critical field sustained by real devices. A theoretical $E_c$ value of 3.3 MV/cm is typically assumed for calculations based on $V_{br}$. However, the measured $E_c$ for vertical FETs and diodes is highly variable, with values between 1.5–3.75 MV/cm having been reported in the literature[90–93]. Material

quality factors such as dislocation density and epitaxial growth conditions, and device design factors such as field plating or edge termination structures all factor into the $E_c$ extracted from device $V_{br}$ values. These factors must be thoroughly understood in GaN to achieve superior MOSFET performance.

## 1.4 Critical Issues for Ultra-Wide Bandgap $Ga_2O_3$ and Diamond Switches

UWBG semiconductors such as $Ga_2O_3$ and diamond represent emerging technologies that are candidates for extremely high power switching. With bandgaps of 4.8-5.5 eV and projected critical field strengths exceeding 8 MV/cm, these materials are positioned to deliver superior high voltage and high temperature switching characteristics.

### 1.4.1 $Ga_2O_3$ Materials and Devices

The (010) and ($\bar{2}$01) planes of monoclinic $\beta$-phase $Ga_2O_3$, shown in Fig. 1.6 [26,27], have become the subject of significant attention for the next generation of power devices beyond GaN [94]. Not only does $Ga_2O_3$ exhibit large bandgap and critical field values, it is also the only WBG or UWBG semiconductor that can be produced via conventional melt-growth techniques. Application of common melt-growth techniques such as the Czochralski (CZ) and edge-defined film-fed growth (EFG) technique has allowed $Ga_2O_3$ substrate technology and size to advance rapidly, with bulk 4" diameter wafers already demonstrated [94,95].

$Ga_2O_3$ switches are primarily targeted for ultra-high power, lower frequency switching due to low electron mobilities ($\approx$ 150–200 $cm^2/V{\cdot}sec$ at room temperature) [78,96,97].

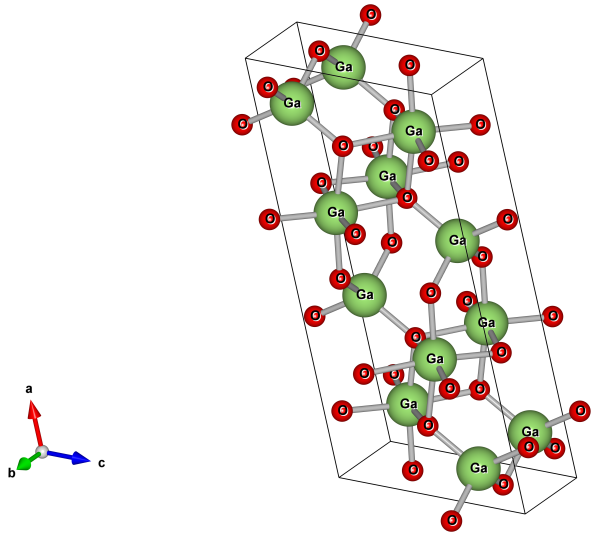


Fig. 1.6. Ball-and-stick model of monoclinic $\beta$-$Ga_2O_3$ [26, 27].

Good device performance has been achieved with normally-on n-channel device technology, with FETs exhibiting current output above 80 mA/mm and breakdown voltages up to 1 kV [23, 98–100]. Critical fields as high as 3.8 MV/cm have demonstrated experimentally in $Ga_2O_3$ switches, already surpassing the theoretical limit for GaN [101]. Despite these performance characteristics, several critical issues have been identified for $Ga_2O_3$ power switches:

- The lack of p-dopants precludes the typical normally-off npn-type MOSFET structure [94]. As such, the majority of lateral and vertical $Ga_2O_3$ switches demonstrated to date are normally-on n-channel devices (a representative example of a lateral $Ga_2O_3$ MOSFET is shown in Fig. 1.7), with highly doped source/drain regions and low/unintentionally doped gate/body regions [23, 102]. These devices have the same issues for fail-safe operation as GaN HEMTs. Positive threshold voltages and normally-off behavior have been reported in unique FET structures such as FETs thin exfoliated

flakes of $Ga_2O_3$ [98, 103]. While interesting, these device architectures are unlikely to result in mass-producible devices for use in real-world applications. Development of $(Al,Ga)_2O_3/Ga_2O_3$ heterostructure devices or thin conducting layer devices may present opportunities to port technologies from normally-off GaN HEMTs into the $Ga_2O_3$ world [104].

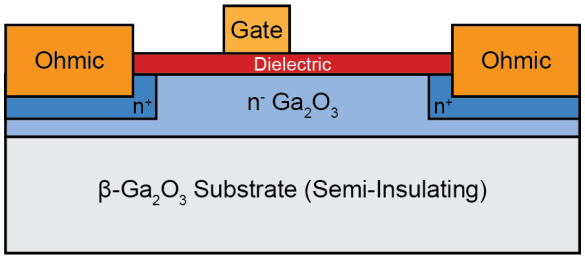


Fig. 1.7. Generic schematic of a depletion-mode lateral $Ga_2O_3$ MOSFET.

- Materials and processes for achieving high-quality dielectric interfaces to $Ga_2O_3$ is important for minimizing off-state leakage and defect-related trapping effects [105]. Lower-k dielectrics such as $SiO_2$ and $Al_2O_2$ have been commonly studied due to their wide bandgaps [106, 107]; integration of higher-k dielectrics has been much less common [103]. High-k dielectrics such as $HfO_2$ and $ZrO_2$ (discussed later in this dissertation) have been the subject of little attention because their bandgaps differ from that of $Ga_2O_3$ by less than 1 eV. However, Wheeler and Shahin, et al. recently demonstrated that these high-k dielectrics exhibit Type II staggered band alignments, with conduction band offsets to $Ga_2O_3$ of around 1.2 eV suitable for use with n-channel devices [108]. Analysis of the electrical quality of these dielectrics and their interfaces with $Ga_2O_3$ is an essential research task for the development of improved power devices.

- Thermal management is even more critical for $Ga_2O_3$ power devices than for GaN. As shown in Table 1.1, the thermal conductivity of $Ga_2O_3$ (0.3 W/cm·K) is less than 1/4$^{th}$ that of GaN (1.3 W/cm·K), and roughly 1/15$^{th}$ that of SiC (4.5 W/cm·K). For $Ga_2O_3$ devices to handle switching at even higher power levels than competing WBG devices, reduction of device self-heating must be addressed [105]. Potential mitigation options could be similar to those in GaN, including integration of high thermal conductivity layers, backside and topside cooling schemes, and reliable contact materials that can withstand higher temperatures in the device active regions, but these have yet to be thoroughly investigated.

### 1.4.2 Diamond Materials and Devices

Cubic-phase diamond (Fig. 1.8) is another UWBG material under consideration for next-generation ultra-high power switches. Diamond is theoretically a perfect candidate for these switches, as the values listed in Table 1.1 position diamond devices to deliver both higher power and higher frequency switching than is possible with any of the other WBG or UWBG semiconductors [24]. Additionally, the extremely high thermal conductivity allows for reduced self-heating and simpler thermal management.

Diamond switches typically rely on conductive channels generated by unconventional means due to very deep acceptor (B, 0.37 eV) and donor (P, 0.5 eV and N, 1.7 eV) dopant levels [109, 110]. One such technique is the formation of a two-dimensional hole gas (2DHG) by hydrogen surface termination of diamond. C-H bonds are formed on a clean diamond surface by exposure to a pure hydrogen plasma at temperatures above 700 °C.

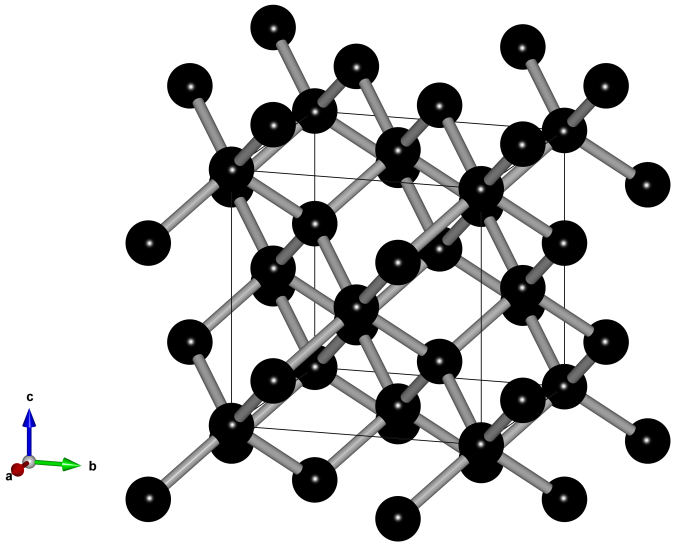


Fig. 1.8. Ball-and-stick model of the diamond cubic phase of carbon [26, 27].

The C-H dipoles create a negative electron affinity (NEA) at the H:diamond surface such that the surface will readily give up electrons [111]. Through adsorption or deposition of various so-called "surface transfer dopants", such as atmospheric $H_2O$ vapor, $NO_2$ gas, or dielectrics such as $Al_2O_3$, $V_2O_5$, $MoO_3$, etc., the 2DHG is formed just below the H:diamond surface with carrier densities of $10^{12}$–$10^{14}$ holes/cm$^2$ [112–114]. The 2DHG is analgous to the 2DEG exhibited by AlGaN/GaN heterostructures, except with opposite charge polarity, and can form the basis for H:diamond switches, shown schematically in Fig. 1.9. The sheet resistance of these 2DHGs is typically an order of magnitude higher than the 2DEGs in AlGaN/GaN structures, due to a roughly order of magnitude lower mobility [115]. A number of different so-called "surface transfer dopants" and passivation schemes have been reported in hydrogen-terminated diamond FETs [115–121], with standout examples of current output up to 1300 mA/mm [122], breakdown voltages up to 500 V, and thermal stability up to 400 °C [123]. Challenges for these surface channel devices include:

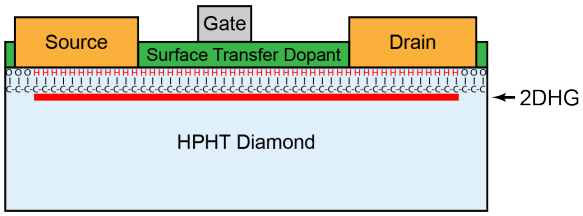


Fig. 1.9. Simple schematic of an H:diamond FET with a surface transfer dopant as passivation and gate dielectric.

- The long term stability of these devices must be well-characterized, as a variety of instabilities have been noted in H:diamond FETs. Since the 2DHG depends on C-H bonds at the diamond surface, H:diamond FETs are sensitive to any process or environment that damages that surface. Dielectric deposition processes involving ozone or oxygen plasmas (i.e. plasma-enhanced ALD) can readily destroy the hydrogen termination and should be avoided in processing. Storage and operation atmosphere can have a significant effect on device performance, with open air leading to degraded performance relative to dry $N_2$ or vacuum [24, 113]. Gate dielectric degradation and/or hydrogen desorption can also be an issue due to hot carrier effects, resulting in blistering underneath contact pads and dielectric layers under high bias conditions [24]

- Cost-effective, large-area, low-defectivity single crystal diamond substrates are not widely available, complicating processing. Substrate production technologies for diamond include chemical vapor deposition (CVD) and high pressure high temperature (HPHT) synthesis [124, 125]. In either case, commercially available device-quality substrates are limited to between 3–10 mm in size, with substate cost growing rapidly with progressively larger single crystal area. Explorations of CVD epilayer growth

over an array of smaller diamond substrates have achieved up to 1–2" square ubstrates, but these technologies are still relatively immature and have not yet translated into commercially available substrates [126, 127]. Alternatively, simulatneous processing of multiple smaller substrates in place of a single large substrate could allow comparable device production rates [105].

## 1.5 Chapter Summary

This review of WBG and UWBG technologies for power switching reveals several overarching technical challenges for GaN, $Ga_2O_3$, and diamond devices. These include processes for high quality dielectric/semiconductor interfaces to achieve reduced gate leakage and charge trapping, novel device architectures for normally-off behavior and high breakdown voltage, and new materials and processes for enhanced electrical and thermal stability. This dissertation presents novel approaches to address these challenges. By achieving advances in these critical areas, this work contributes to higher performance and higher reliability WBG and UWBG switches, thereby enhancing their utility in real-world applications.

# Chapter 2: Research Approach

This dissertation reports novel strategies for addressing the key challenges for WBG/UWBG power switches discussed in Chapter 1. A brief description of the approaches and contributions of this work is provided below, divided into three topic areas of research.

## 2.1 High-k Dielectric Integration with WBG and UWBG Semiconductors

Chapters 3 and 4 report novel ALD $ZrO_2$ and $HfO_2$ high-k dielectrics as candidates for integration with n-type GaN and $Ga_2O_3$ to address the issue of high quality dielectric/semiconductor interfaces. These high-k dielectrics are appealing not just for their excellent material characteristics (summarized in Table 2.1), but also because integration of these dielectrics allows for flexibility in controlling the tradeoffs between maximum drain current, gate leakage, and gate capacitance by changing the dielectric thickness [128]. Additionally, varying amounts of charge can be created in these dielectrics through appropriate ALD precursor selection, specifically through $ZrO_2$ grown with ZTB (negative charge) or TDMAZ (much less charge) precursors, thereby offering opportunities for threshold voltage manipulation in n-channel GaN and $Ga_2O_3$ devices.

Table 2.1. Comparison of dielectric parameters for low-k and high-k dielectrics. (Data from [80, 108, 129–135].)

| Dielectric | k | $E_g$ (eV) | $E_{br}$ (MV/cm) | GaN CBO (eV) | $Ga_2O_3$ CBO (eV) |
|---|---|---|---|---|---|
| $SiO_2$ | 3.9 | 8.6 | 10 | 2.5 | 3.6 |
| $Al_2O_3$ | 9 | 6.8 | 10 | 2.1 | 1.5 |
| $HfO_2$ | $\geq$14 | 5.7 | 7 | 1.1 | 1.3 |
| $ZrO_2$ | 25 | 5.8 | 9 | 1.1 | 1.2 |

Electrical characterization of these dielectrics in GaN and $Ga_2O_3$ MOS systems was performed through capacitance-voltage (C-V) and current-voltage (I-V) measurements on MOS capacitor structures. Data from these measurements allowed extraction of fixed oxide charge quantities, interface trap state densities, and leakage current mechanisms for dielectrics deposited on device-relevant crystal planes of GaN and $Ga_2O_3$. Based on the measurements presented, effective pre-deposition surface treatments were developed, and the electrical quality of these dielectrics was determined to evaluate their potential as gate dielectrics in functional WBG/UWBG switches. For GaN, substrates included the bulk c-plane GaN substrates encountered in lateral AlGaN/GaN HEMT structures, as well as the much-less studied non-polar a- and m-planes important for trench-gate GaN MOSFETs. The effects of different substrate etch conditions and pre-ALD surface cleans on the resulting interface quality were also assessed using these measurements. $ZrO_2$ dielectrics deposited using the ZTB precursor were found to exhibit a roughly +1–2 V positive C-V curve shift on all GaN substrates, regardless of surface condition or cleaning process. This indicated the presence of negative charge in the dielectric, which was also linked to a frequency-dependent loss mechanism. Meanwhile, TDMAZ-derived $ZrO_2$ typically exhibited a much smaller amount of oxide charge, depending on the pre-deposition surface cleaning employed, and was frequency-stable. For $Ga_2O_3$, $(\bar{2}01)$-plane bulk substrates were used in the as-grown condition and subjected to similar characterization techniques. In all cases, $HfO_2$ and $ZrO_2$ deposited with both ZTB and TDMAZ precursors exhibited comparable positive threshold voltage shifts, with $HfO_2$ exhibiting outstanding electrical interface qualities on $Ga_2O_3$.

## 2.2 Novel Devices and Processing for WBG and UWBG Switches

The design, processing, and characterization of WBG and UWBG power devices and materials are reported next, with emphasis on normally-off device architectures critical for fail-safe power switching. The $ZrO_2$ dielectrics derived from the ZTB and TDMAZ precursors characterized in Chapter 3 were successfully integrated as gate dielectrics into both planar and recessed-gate AlGaN/GaN HEMTs. Chapter 5 details the fabrication and characterization of these $ZrO_2$ MOS-HEMTs and their comparison to reference Schottky metal-gated HEMTs. HEMTs were characterised under direct current (DC) and switching conditions using both static and pulsed I-V measurements of drain current as a function of gate and drain bias; gate leakage current was also measured. In comparison to the reference HEMTs, $ZrO_2$ integration, when combined with gate recess etching, allowed threshold voltage control over a nearly 7 V range, enabling both normally-on and normally-off MOS-HEMTs with appropriate dielectric and recess selection. Dielectric integration significantly suppressed gate leakage current relative to the Schottky gates, allowing improved current output by driving the gate into higher forward bias. Charge trapping in the $ZrO_2$ dielectrics was also evaluated from comparison of the change in dynamic on-resistance, with the negatively-charged ZTB dielectrics exhibiting significantly more charge trapping than the uncharged TDMAZ dielectrics.

Design and process development for normally-off vertical trench-gate GaN MOS-FETs is also presented in Chapter 6. Epistructure design and device fabrication processes are not yet well understood for these devices, as evidenced by the widely varying reports of epistructure doping levels, thicknesses, and “optimized” processes to satisfy the issues

noted in Chapter 1. Furthermore, the capability to fabricate and characterize such devices is limited to only a small number of research groups worldwide; the development of similar capability at the University of Maryland represents an important contribution from this work. A photolithographic mask set was designed specifically for this process, with a number of features to facilitate study of trench gates aligned to different crystallographic planes. In addition, a three-layer epitaxial layer structure was designed for growth by a commercial vendor on a 2" GaN substrate; the design considerations for this structure (doping density and layer thickness) are described in the context of achieving a target 1200–1500 V blocking voltage. Characterization of the wafer and its various epilayers was performed to determine important parameters such as sheet resistivity, contact resistivity, and doping density of each layer using I-V and C-V measurements on planar Ohmic contact structures and diodes. Trench fabrication process considerations for trench-gate MOSFETs are also reported, including plasma etch process selection, mask selection for these etches, TMAH wet treatments to create vertical sidewalls, and gate metallization within the gate trench. Understanding of these considerations, combined with the dielectric processing studies from Chapter 3, are together expected to enable future improvements in vertical GaN MOSFETs.

Additionally, Chapter 7 reports the fabrication and characterization of H:diamond switches on ultra-smooth type IIa HPHT diamond substrates. These substrates were selected for use due to their low dislocation density compared to CVD-grown substrates and low impurity incorporation to minimize the effects of scattering and electrically-active unintentional dopants [136–139]. Processes to create ultra-smooth (surface roughness $<3$ Å) diamond substrates prior to hydrogen-termination are described. Due to the very small

diamond substrate sizes and square substrate geometries, a unique process for photoresist spincoating also was developed. This process, involving surrounding a diamond substrate with multiple pieces of silicon wafers or other material, was required to mitigate photoresist nonuniformities that negatively affected contact lithography pattern fidelity during fabrication. p-channel $Al_2O_3$/H:diamond MOS switches fabricated on these substrates are also reported using standard static I-V measurements. Normally-on behavior ($V_t$ = +4 V) and good current output (up to 60 mA/mm) were observed. Factors influencing device stability and uniformity are also reported through I-V measurements taken over the course of one week.

## 2.3 Novel Materials and Processes for Electrical and Thermal Stability

Finally, advanced materials and processes for improved electrical and thermal reliability in WBG and UWBG switches are reported. One such advance is detailed in Chapter 8, where ALD TiN transition metal nitride films are presented as an electrically and thermally stable gate electrode for WBG/UWBG power devices. Conventional Schottky metal gates such as Ni degrade due to metal migration under electrical and thermal stresses, whereas transition metal nitrides such as TiN do not because of non-metallic bonds in the material [56–59]. The thermal stability of TiN, along with good electrical properties on GaN and AlGaN, position it as a viable substitute for electrically and thermally stable power switches [140–143]. ALD was used to deposit TiN gates for AlGaN/GaN HEMTs. As-fabricated TiN-gated HEMTs were compared to reference Ni-gated HEMTs using static and pulsed I-V testing. After determining the initial performance of each device variety, the electrical

stability of TiN gates was assessed using reverse bias gate sweeping from a gate-source voltage of 0 V until breakdown. Thermal stability was evaluated by annealing the fabricated HEMTs at progressively higher temperatures up to 1000 °C, and comparing gate leakage and device operation after each anneal. Significant improvements in electrical and thermal stability were realized by implementing the TiN gates in place of conventional Ni metal, making TiN gate technology an important contribution for reliable power switches.

Additionally, a novel process is presented for plasma-free selective area patterning and etching of NCD heat spreading films for power devices. NCD films have found use in power devices such as AlGaN/GaN HEMTs to reduce self-heating [37]. Selective patterning capability is necessary for integration of NCD films into useful device architectures, but selective etching using an $O_2$ plasma risks plasma damage to underlying semiconductor layers. Chapter 9 presents a plasma-free process for selective of NCD films grown on Si for simplicity and cost purposes. Etching was achieved through use of a patterned oxide hardmask on top of the NCD and exposure to an oxygen atmosphere at 700–800 °C. Optical microscopy, scanning electron microscopy, and Raman microscopy were used to monitor etch progression. Etching was found to proceed both laterally and vertically with controlled etch rates in a semi-isotropic process (i.e. less anisotropic than in a conventional plasma etch). Not only does this process allow etching wtihout plasma damage effects, it also enables NCD etching along backside vias and other features inaccessible to a typical plasma etch.

# PART II
## CHARACTERIZATION OF NOVEL DIELECTRICS FOR WBG AND UWBG POWER SWITCHES

# Chapter 3: Characterization of ALD $ZrO_2$ High-k Dielectrics in GaN MOS Systems

## 3.1 Introduction

High quality MOS gate structures are essential for GaN power transistors with low on-state resistance and gate leakage. High-k dielectrics such as $ZrO_2$ are appealing for GaN device integration, with a dielectric constant as high as k $\approx$ 29, breakdown strength up to 9 MV/cm, and valence and conduction conduction band offsets to GaN greater than 1 eV, respectively [80, 131, 133–135]. $ZrO_2$ can also be deposited by ALD for uniform, conformal deposition on planar and vertically etched gate features such as those found in a MOS-HEMT or vertical MOSFET. Multiple ALD precursor systems can be employed for $ZrO_2$ deposition, with TDMAZ being the most commonly studied on GaN [144, 145]. $ZrO_2$ dielectrics deposited using ZTB are novel to GaN MOS systems and devices. ZTB is an oxygen-containing precursor, while TDMAZ has no oxygen, as shown in Fig. 3.1.

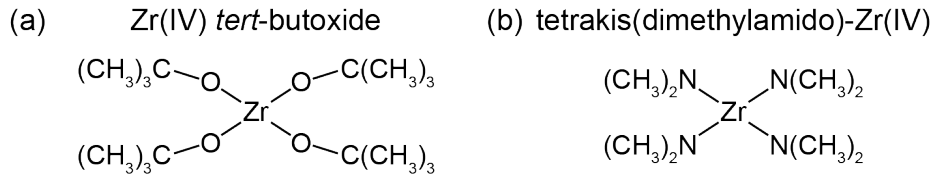


Fig. 3.1. Structural formulas for ZTB ($Zr[OC(CH_3)_3]_4$) and TDMAZ ($[(CH_3)_2N]_4Zr$) precursors.

Appropriate precursor selection may allow tuning of the oxygen stoichiometry in $ZrO_2$ dielectrics on GaN, which affords the opportunity for gate charge engineering in WBG devices. As such, study of these dielectrics in GaN MOS systems is an important undertaking for production of high performance devices. This chapter reports the first characterization

and comparison of novel ZTB- and TDMAZ-derived $ZrO_2$ films in MOS capacitors on bulk GaN substrates. Device-relevant orientations (polar c-plane, and non-polar a- and m-planes) and surface conditions (as-grown and Cl-plasma etched) for GaN are explored in this work. Understanding of dielectric/GaN interface along these other planes and surface conditions is extremely relevant to the performance of recessed-gate AlGaN/GaN HEMTs and trench-gate GaN MOSFETs, and very few studies have been undertaken in this regard [22, 81].

## 3.2 MOS Capacitor Fabrication and Measurement

Simple MOS capacitor structures were used to characterize ALD high-k dielectrics on as-grown and etched n-type GaN. Bulk c-plane (polar) GaN substrates grown by HVPE were used in either the as-grown condition or after etching approximately 100 nm into the sample using a $Cl_2$/Ar plasma. Separate nonpolar m- and a-plane GaN substrates were also used in the as-grown condition; these substrates were designated as "rider" grade, with a minimum usable surface area of 60% due to cracks and defects. All substrates were procured from a commercial vendor (Kyma Technologies) and were unintentionally or lightly n-doped, with carrier concentrations on the order of n = $10^{16}$–$10^{17}$ $cm^{-3}$. Prior to dielectric deposition, GaN samples were cleaned using a variety of surface pretreatments previously found to give high quality interfaces with $Al_2O_3$ and $HfO_2$, including piranha ($3H_2SO_4$:$1H_2O_2$) etching at 80 °C followed by rapid thermal annealing in flowing $O_2$ at 700 °C for 10 min [146, 147]. $ZrO_2$ films were deposited directly on the substrate surfaces (no GaN epilayers) by thermal ALD at 200 °C using either ZTB or TDMAZ and deionized water precursors in an Ultratech Savannah 200 ALD reactor, with growth rates of ≈0.8 Å/cycle

for both precursors. Ozone oxidation under the same deposition conditions were attempted but not reported in this work, due to a very low growth rate (0.3 Å/cycle) and detectable levels of carbon contamination in the film by x-ray photoelectron spectroscopy (XPS). MOS capacitors were then fabricated by standard e-beam metal evaporation and liftoff processes to create topside and backside Ti/Au contacts. C-V measurements were performed using a Keithley 4200 semiconductor characterization system. Two contact arrangements were used, as shown in Fig. 3.2. The primary arrangement was used for most C-V measurements, taken between small circular top-side contacts (bias) and the blanket back-side contact (ground). The secondary arrangement was used for trapping/detrapping studies using ultraviolet (UV), where measurements were taken between small circular contacts (bias) and a surrounding large-area contact (ground) on top of the $ZrO_2$ film. This forms a series capacitor setup such that the reciprocal of the large-area capacitor drops out of the series combination, leaving the measured capacitance as that of the small capacitor only.

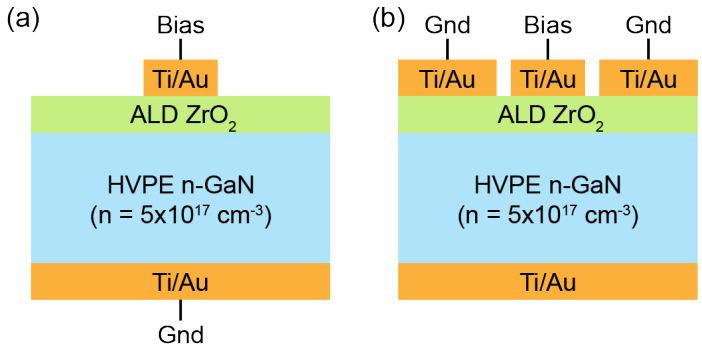


Fig. 3.2. MOS capacitor structures fabricated for this work. The top-to-bottom arrangement in (a) was used for general C-V measurements, while the arrangement in (b) was used in the UV detrapping experiments.

## 3.3 Capacitance-Voltage Measurements on $ZrO_2$/GaN MOS Capacitors

### 3.3.1 As-Grown c-Plane GaN

The frequency response of the $ZrO_2$ films from each precursor, shown in Fig. 3.3, was extracted by measuring the capacitance as a function of frequency in accumulation at a fixed bias of +5 V. The ZTB film exhibited a significant frequency dependence of accumulation capacitance and thus dielectric constant, with k decreasing from 27 at 1 kHz to 17 at 1 MHz. The TDMAZ-grown films, however, showed stable capacitance values leading to a dielectric constant of k = 24 across the entire measured frequency range. While these values are all within the range of reported dielectric constants for $ZrO_2$ [131, 133], the sensitivity to increasing measurement frequencies indicates that a loss mechanism is dominant at high measurement frequencies in the ZTB films. The cause has been identified as oxygen nonstoichiometry in the ZTB films, as XPS measurements indicated a O:Zr ratio of 2.2:1 for the ZTB films [108], while the TDMAZ films were nearly stoichiometric with an O:Zr ratio of 2.0:1. Other residual contaminants (e.g. carbon) from the ALD precursors were not detected. Previous work has linked these loss effects to residual water-based species (e.g. $H_2O$, $OH^-$, etc.) left over from the $H_2O$ oxidation steps in thermal ALD films [148]. In this case, however, the excess oxygen and the frequency dispersion is observed only in the ZTB films, meaning that the source must be the oxygen-containing ZTB precursor itself. Future work will explore whether post-deposition annealing processes can mitigate this frequency dependence in the ZTB films; however, Niinisto et al. previously reported that post-deposition annealing in forming gas ($N_2/H_2$) did not significantly improve the

accumulation capacitance in $ZrO_2$ films on Si with lower than desired dielectric constants [133].

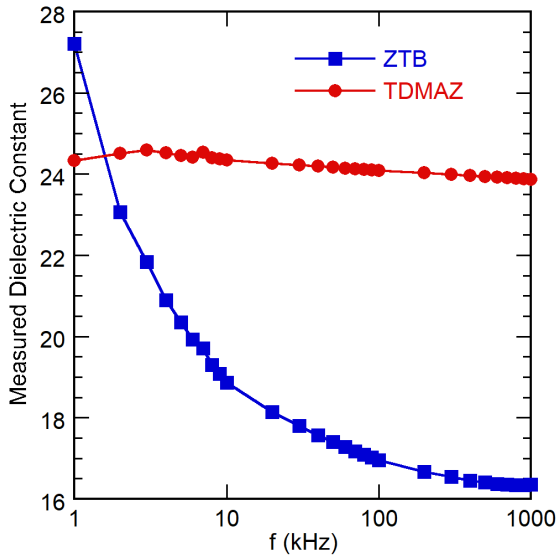


Fig. 3.3. Frequency dependence of the $ZrO_2$ dielectric constant, as extracted from the accumulation capacitance when measured from 1 kHz to 1 MHz. The ZTB shows a significant decrease in dielectric constant with increasing frequency, while the TDMAZ dielectric constant is stable over the measurement frequency range.

1 MHz dual-sweep C-V measurements were performed on the $ZrO_2$/GaN MOS capacitors shown in Fig. 3.2(a) to compare the effects of the different surface pretreatments (reference acetone and isopropanol rinse, 80 °C piranha clean for 10 min, and piranha clean followed by 700 °C thermal oxidation for 10 min) on the C-V characteristics of films from each precursor. Additional surface treatments based on an Ar/$H_2$ anneal at 850 °C and a soak in 80 °C TMAH were performed but are not included here, as these treatments resulted in severe dislocation etching and surface damage. C-V curves are shown graphically in Fig. 3.4. The ideal flatband voltage, $V_{fb}$, for these MOS structures (assuming no fixed or

trapped charge) was calculated as 0.12 V using Eqn. 3.1:

$$V_{fb} = \phi_{ms} = \phi_m - (\chi_{GaN} + \phi_n) \tag{3.1}$$

where $\phi_{ms}$ = metal-semiconductor work function difference, $\phi_m$ = metal work function, $\chi_{GaN}$ = GaN electron affinity, and $\phi_n$ = difference between the conduction band and Fermi level ($E_C - E_F$) in the semiconductor. The measured flatband voltage was determined by finding the total flatband capacitance ($C_{fb}$) according to Eqn. 3.2 along the C-V sweep direction closest to $V_{fb,ideal}$:

$$C_{fb} = \frac{\epsilon_{ox}\epsilon_{GaN}}{\epsilon_{GaN}d + \epsilon_{GaN}\sqrt{k_B T \epsilon_{GaN}/N_D q^2}} \tag{3.2}$$

where $\epsilon_{ox}$ and $\epsilon_{GaN}$ = absolute permittivity of $ZrO_2$ and GaN, respectively (= $\epsilon_0 \cdot$k), d = $ZrO_2$ thickness, $k_B$ = Boltzmann's constant, T = ambient temperature (assumed to be 298 K), and $N_D$ = apparent donor/carrier density as extracted from $1/C^2$ –V plots of the C-V data. The ZTB C-V curves were uniformly shifted to positive voltages, regardless of the pre-ALD surface treatment employed. These shifts are indicative of an overriding negative fixed charge of $5–7\times10^{12}$ $cm^{-2}$, as extracted from the difference between the difference between the ideal and measured $V_{fb}$ from the C-V curve closest to ideal. The excess oxygen in the ZTB films is expected to be negatively charged, possibly in the form of excess oxygen or $OH^-$. Negative charge in the ZTB-derived $ZrO_2$ may therefore be useful in producing positive threshold voltage shifts in normally-on GaN devices. Meanwhile, surface treatments before TDMAZ-$ZrO_2$ deposition produced negative shifts in the measured C-V curves compared to

the reference, yielding $V_{fb}$ values much closer to ideal, and a corresponding reduction in fixed charge density to as low as $4\times10^{11}$ cm$^{-2}$. TDMAZ-$ZrO_2$ is therefore not expected to be as effective as ZTB-$ZrO_2$ in producing positive threshold voltage shifts due to the lack of significant negative oxide charge to deplete the device channel. In any case, control over this oxygen excess through ALD precursor selection presents interesting opportunities for gate charge engineering in normally-off GaN MOS devices, as will be discussed later in Chapter 5.

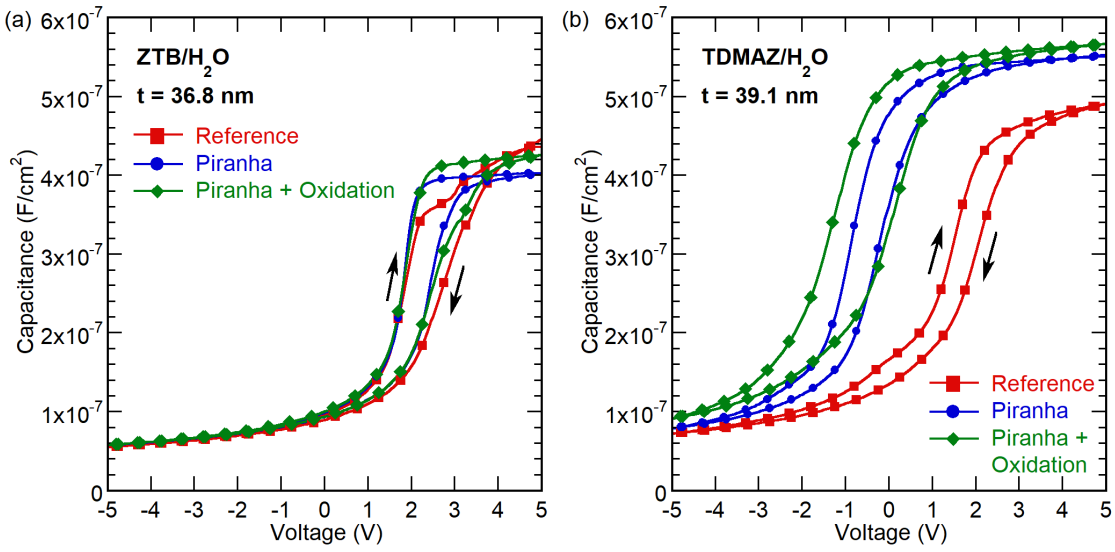


Fig. 3.4. 1 MHz dual-sweep capacitance-voltage measurements on $ZrO_2$/GaN MOS capacitors from (a) ZTB (36.8 nm film thickness) and (b) TDMAZ (39.1 nm film thickness) precursors with various pre-ALD surface treatments.

The hysteresis ($\Delta V_{fb}$) between each sweep direction was used to quantify the total oxide and interface trapped charge (from slow traps that respond to the measurement sweep) according to Eqn. 3.3 [133, 146]:

$$Q_{trap} = C_{ox}\Delta V_{fb} \tag{3.3}$$

Trapped charge estimates were between 2–5$\times 10^{12}$ cm$^{-2}$, depending on the surface treatment used. In all cases, the measured hysteresis was much wider ($0.7 \leq \Delta V_{fb} \leq 1.5$ V) than previously observed when employing these surface treatments before deposition of $Al_2O_3$ and $HfO_2$ on GaN ($\Delta V_{fb} \leq 0.5$ V) [147]. These values are in part due to capacitor fabrication directly on lower quality bulk HVPE GaN substrates without MOCVD GaN epitaxial layers, but also indicate a generally higher interface trap density associated with $ZrO_2$ films. For both the ZTB and TDMAZ dielectrics, the pre-ALD piranha treatment yielded low hysteresis and corresponding trapped charge, while the post-piranha thermal oxidation worsened the hysteresis. The piranha treatment by itself is thus preferred for preparing as-grown GaN surfaces for $ZrO_2$ ALD, as long as the device structures (contacts, passivation layers, etc.) can withstand the attack of piranha etching [149].

The trapped charge stability in the ZTB dielectric was explored through repeated C-V measurements on samples exposed to a broadband UV light source, as shown in Fig. 3.5a. After a 20 min UV exposure, the high-to-low C-V sweep shifted negative by nearly 2 V (closer to the ideal $V_{fb}$), indicating that a large quantity of trapped and oxide charge (up to 5$\times 10^{12}$ cm$^{-2}$) had been removed by the UV exposure. Additional C-V measurements showed gradual charge retrapping, up to a total of 68 hours when the final C-V curve had returned to the initial state. The same procedure was performed on the TDMAZ films, which were insensitive to the UV exposure shown in Fig. 3.5b. This indicated that the trapping/detrapping behavior observed only in the ZTB films must again be linked to the excess oxygen and any resulting oxide and interface defect states.

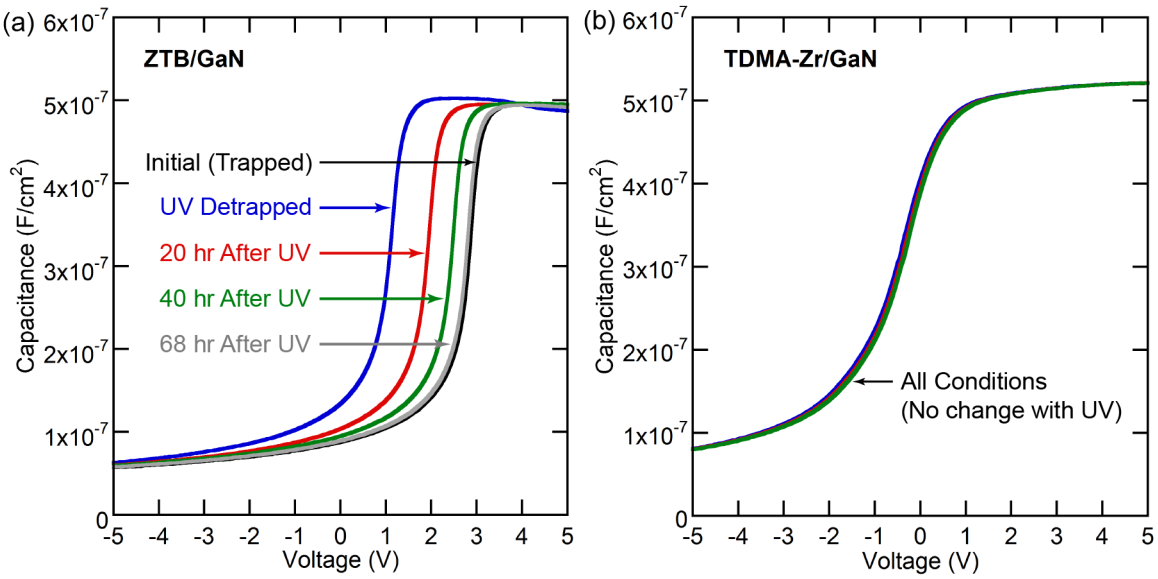


Fig. 3.5. (a) High-to-low C-V sweeps on ZTB/GaN MOS capacitors. A 20 min UV exposure discharged a large amount of slow interface traps observed previously, and gradually recharged over the course of 3 days. (b) C-V sweeps on TDMAZ/GaN MOS capacitors indicated no trap state alteration from the UV exposure.

### 3.3.2 Etched c-Plane GaN

C-V measurements performed on etched c-plane GaN MOS capacitors are shown in Fig. 3.6. Dielectrics on the as-etched (reference solvent clean) GaN surfaces exhibited reduced accumulation capacitance, likely due to physical and electrical defects created by the plasma etching. This capacitance was recovered by the piranha-based cleaning processes, possibly due to removal of a small amount of etch-damaged GaN [78]. Positive shifts in the ZTB C-V (Fig. 3.6a) curves were again observed regardless of surface treatment. The TDMAZ C-V behavior (Fig. 3.6b) showed an even stronger dependence on the surface preparation for the etched c-plane GaN, with the thermal oxidation step leading to a nearly 4 V negative shift in the C-V curves relative to the sample cleaned with piranha only, which exhibited a flatband voltage close to ideal. The piranha treatment by itself is therefore

again preferred for GaN surface cleanup prior to ALD for its closest-to-ideal electrical parameters. No defect "bumps" or other features are observed in the depletion regime for either oxide, indicating that the piranha-based pre-ALD surface treatments give higher quality dielectric interfaces with etched GaN as well as on as-grown GaN. This finding fits well with observations from Zhang et al. that a piranha etch can round the corners of etched gate trenches for vertical GaN devices, thereby reducing the electric field [78].

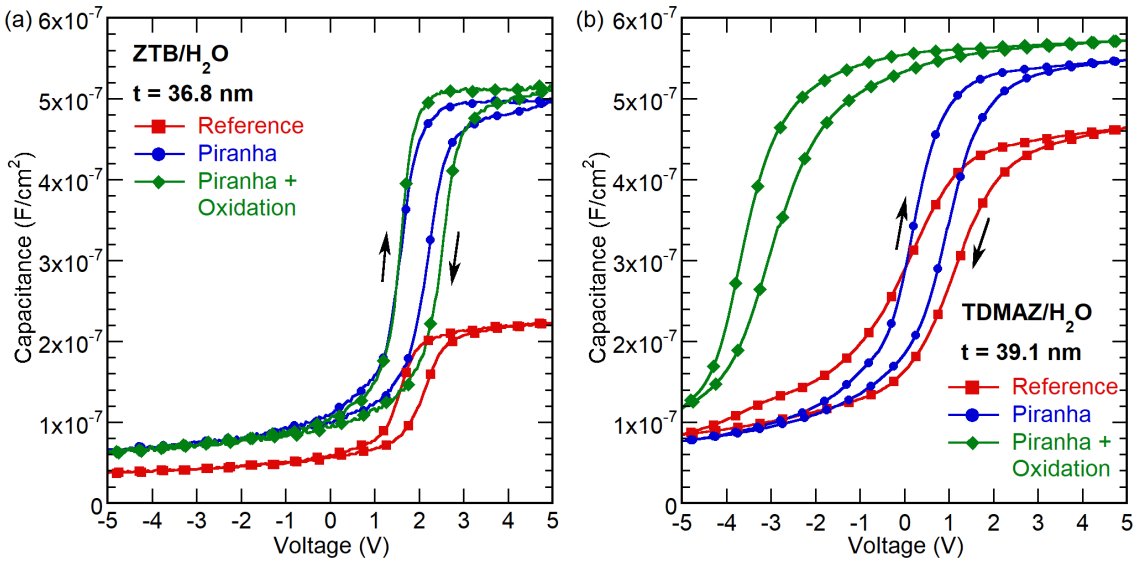


Fig. 3.6. C-V measurements for (a) ZTB and (b) TDMAZ films on GaN etched with $Cl_2$/Ar plasma. As with the as-grown GaN substrates, piranha cleaning by itself yielded superior C-V characteristics over the other treatments explored in this work.

### 3.3.3 Non-Polar (a- and m-Plane) GaN

A limited number of small (5×10 mm) non-polar a- and m-plane GaN substrates were available in this work; as such, only the 80 °C piranha clean was used for surface preparation prior to $ZrO_2$ deposition. The C-V characteristics of $ZrO_2$ films on piranha-cleaned non-polar a- and m-plane substrates are shown in Fig. 3.7. Very low capacitance

values were measured for $ZrO_2$ on the m-plane substrates, which is surprising given that the m-plane has typically been preferred for vertical trench-gate GaN devices. The inability to obtain a useful C-V curve was linked to the poor quality of these substrates, which were produced by cutting and polishing rectangular wafers out of a thick c-plane GaN wafer [82]. Both microscopic (dislocations) and macroscopic (cracks, pits, chips) are observable in the non-polar samples that consume roughly 40% of the sample surface area, shown in Fig. 3.8; these defects affected the C-V measurements by contributing to high leakage/loss in the semiconductor that prevents adequate carrier accumulation at the dielectric/semiconductor interface. Meanwhile, for the a-plane samples, C-V curves very similar to those of piranha-cleaned c-plane GaN were collected. The ZTB dielectric still exhibited a slightly smaller positive shift in the C-V curves, while the TDMAZ dielectric C-V curve was very close to the ideal $V_{fb}$. The dual-sweep hysteresis from the $ZrO_2$/a-plane GaN samples were also comparable those on the c-plane GaN.

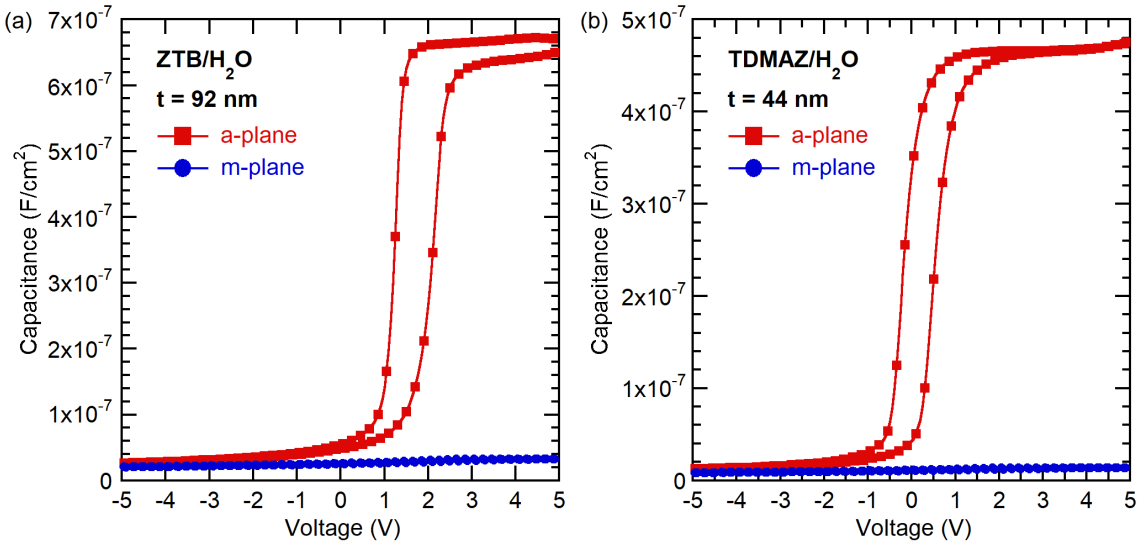


Fig. 3.7. C-V measurements for (a) ZTB and (b) TDMAZ films on non-polar a- and m-plane GaN bulk substrates.

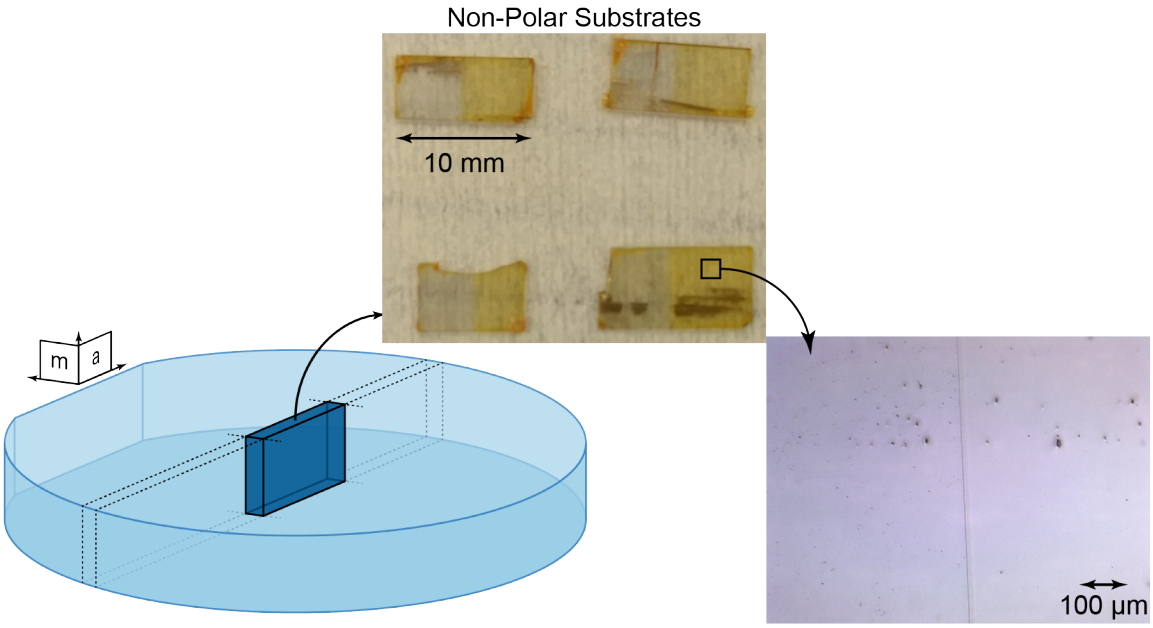


Fig. 3.8. Schematic and optical images of non-polar GaN substrates (5×10 mm), showing macroscopic and microscopic defects in the samples.

## 3.4 Chapter Summary

MOS capacitors with $ZrO_2$ and $HfO_2$ high-k dielectrics were fabricated on bulk GaN substrates. On both substrate materials, the dielectric constant of $ZrO_2$ grown by thermal ALD using ZTB and deionized water was found to decrease significantly when measured at increasing frequencies between 1 kHz (k = 27) and 1 MHz (k = 17), while $ZrO_2$ grown using TDMAZ and deionized water exhibited a frequency-independent dielectric constant of k = 24. The consistently positive $V_{fb}$ shift observed with ZTB-$ZrO_2$ films were consistent with negative charge due to excess oxygen in the dielectric. C-V curve shifts in the TDMAZ-$ZrO_2$ films were more sensitive to the pre-ALD surface cleaning employed, with piranha cleaning yielding $V_{fb}$ values much closer to the ideal case on both as-grown

and etched GaN. The hysteresis between the positive-to-negative and negative-to-positive sweep directions for these $ZrO_2$ films on both as-grown and etched c-plane GaN ($0.7\ V \leq \Delta V_{fb} \leq 1.5\ V$) were used in Eqn. 3.3 to estimate trapped charge quantities. For both ZTB and TDMAZ films, trapped charge densities were on the order of $10^{12}$ $cm^{-2}$, with pre-ALD piranha cleaning typically giving the lowest trapped charge numbers, regardless of substrate condition. Charge in the ZTB dielectrics was sensitive to broadband UV, with most traps discharged after 20 min exposure and recharged within three days of repeat measurements, while the TDMAZ dielectrics were not sensitive to the exposure.

This work shows that the amount of dielectric charge can be controlled based on the ALD precursor and surface treatments employed, which will ultimately prove useful in manipulating threshold voltage in normally-on, n-channel WBG switches shown later in Chapter 5. However, further work is needed to determine if the frequency-dependent capacitance observed in the ZTB-$ZrO_2$ can be mitigated while still maintaining the negative fixed charge. Potential mitigation strategies include annealing in a reducing atmosphere, changes to the precursor initiation sequence at the beginning of ALD growth, or stacking of alternating layers of TDMAZ and ZTB $ZrO_2$.

# Chapter 4: $HfO_2$ and $ZrO_2$ High-k Dielectric Interfaces with $\beta$-$Ga_2O_3$

## 4.1 Introduction

With the surge of interest $\beta$-$Ga_2O_3$ for ultra-high power devices, increasing attention has been paid to normally-on MOSFETs for power and RF switching [99, 101, 150–152]. Just as with GaN power switches, high dielectric/$Ga_2O_3$ interface quality is required to minimize off-state gate leakage and achieve optimum on-state performance. Dielectrics such as $SiO_2$ and $Al_2O_3$ deposited by ALD have typically been used for these MOSFETs and have been thoroughly characterized on $\beta$-$Ga_2O_3$ [106, 107, 129, 130]. In comparison, little study has been performed on high-k dielectrics such as $HfO_2$ and $ZrO_2$, in large part due to the narrower bandgaps assicated with these dielectrics. Despite having bandgaps approximately 0.9 eV greater than that of $Ga_2O_3$, both ALD $HfO_2$ and $ZrO_2$ were recently found to exhibit Type II staggered band alignments on $(\bar{2}01)$ $\beta$-$Ga_2O_3$ and conduction band offset (CBO) of 1.3 eV and 1.2 eV, respectively, as determined by XPS [108]. These values are close to the 1.5–1.6 eV CBO for the $Al_2O_3$/$Ga_2O_3$ MOS structure [130], and recent reports suggest that $HfO_2$ is a useful insulator for n-channel $Ga_2O_3$ MOS devices [102, 152]. Additionally, $HfO_2$ and $ZrO_2$ may afford opportunities to achieve normally-off transistor behavior through gate charge engineering at the dielectric/$Ga_2O_3$ interface [152]. Detailed study of the electrical characteristics of these systems and interfaces has not yet been undertaken. This chapter addresses the need for high quality MOS structures by investigating the electrical properties of ALD $HfO_2$ and $ZrO_2$ films on $(\bar{2}01)$ $Ga_2O_3$ through C-V and I-V measurements on MOS capacitors.

## 4.2 Processing for High-k/$Ga_2O_3$ Capacitor Fabrication

$HfO_2$ and $ZrO_2$ films were deposited by ALD on 680 $\mu$m thick, 5×10 mm bulk n-type ($\bar{2}01$) $\beta$-$Ga_2O_3$ grown by the EFG method, with a manufacturer specified carrier concentration of $\approx 2\times10^{17}$ $cm^{-3}$ from unintentional doping. The capacitor structure and associated band diagrams are shown in Fig. 4.1. Immediately prior to ALD growth, the substrates were cleaned with a 10 min room temperature UV/$O_3$ exposure followed by a 30 sec soak in 10:1 buffered oxide etch ($NH_4F$:HF). $HfO_2$ films were deposited by thermal ALD at 175 °C in an Oxford FlexAL reactor using tetrakis(ethylmethylamino)hafnium and $H_2O$ precursors (1.0 Å/cycle). $ZrO_2$ films were deposited at 200 °C in an Ultratech Savannah 200 ALD reactor using either ZTB or TDMAZ as precursors and deionized $H_2O$ as the oxidant (1.3 Å/cycle) [108]. These films were not subjected to post-deposition annealing prior to capacitor fabrication. Circular Au topside contacts were deposited by electron-beam evaporation, while blanket Ti/Au was deposited for the backside contact (without contact annealing). Dual-sweep C-V measurements using a standard parallel capacitance and resistor/conductor model and I-V measurements were made on a Keithley 4200 parameter analyzer.

## 4.3 $HfO_2$/$Ga_2O_3$ MOS System

### 4.3.1 Capacitance-Voltage Measurements

The capacitance behavior of 40 nm $HfO_2$ under dual sweeps from 3.5 V to -5 V at 10 kHz, 100 kHz, and 1 MHz is shown in Fig. 4.2a. Also shown is the ideal C-V curve

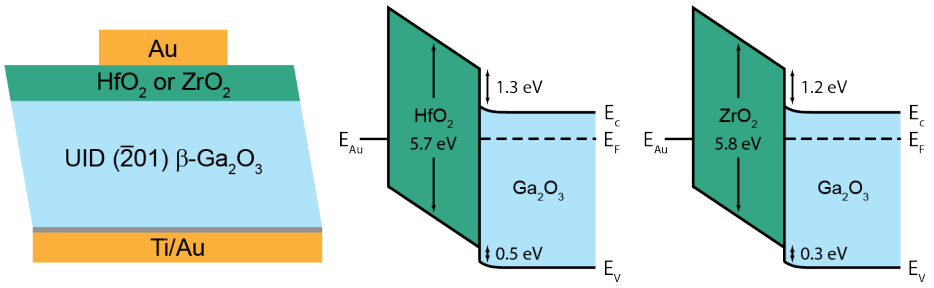


Fig. 4.1. Example MOS capacitor structure and associated band diagrams for $ZrO_2$ and $HfO_2$ on $Ga_2O_3$.

calculated from theory using a standard series capacitance model for the dielectric and semiconductor depletion capacitances, with the latter given by Eqn. 4.1 (and $V_{fb}$ calculated using previously reported Au metal work function values on $Ga_2O_3$) [153, 154]:

$$C_D = \frac{\epsilon_{SC}}{\sqrt{2}L_D}\left[\frac{\exp\left(\frac{q\phi_s}{k_BT}\right) - 1 - \left(\frac{n_i}{N_D}\right)^2 \exp\left(\frac{-q\phi_s}{k_BT}\right)}{\left[\frac{-q\phi_s}{k_BT} + \exp\left(\frac{q\phi_s}{k_BT}\right) - 1 + \left(\frac{n_i}{N_D}\right)^2\left[\exp\left(\frac{-q\phi_s}{k_BT}\right) - 1\right]\right]^{\frac{1}{2}}}\right] \tag{4.1}$$

where $\epsilon_{SC}$ = permittivity of the semiconductor, $\phi_s$ = surface potential, $n_i$ = semiconductor intrinsic carrier concentration, $N_D$ = semiconductor doping/carrier density, and $L_D$ = Debye length. $\phi_s$ can be related to the voltage, V, for an n-type semiconductor through Eqn. 4.2:

$$V - V_{fb} = \pm\frac{1}{C_{ox}}\left[\sqrt{2}\epsilon_{SC}\left(\frac{k_BT}{qL_D}\right)\left[-\frac{q\phi_s}{k_BT} + \exp\left(\frac{q\phi_s}{k_BT}\right) - 1 + \left(\frac{n_i}{N_D}\right)^2\left[\exp\left(\frac{-q\phi_s}{k_BT}\right) - 1\right]\right]^{\frac{1}{2}}\right] + q\phi_s \tag{4.2}$$

with $V_{fb}$ = theoretical flatband voltage and $C_{ox}$ = dielectric capacitance.

A dielectric constant of k = 14 was extracted from the maximum accumulation capacitance for the as-deposited films; this value is on the lower end of dielectric constant

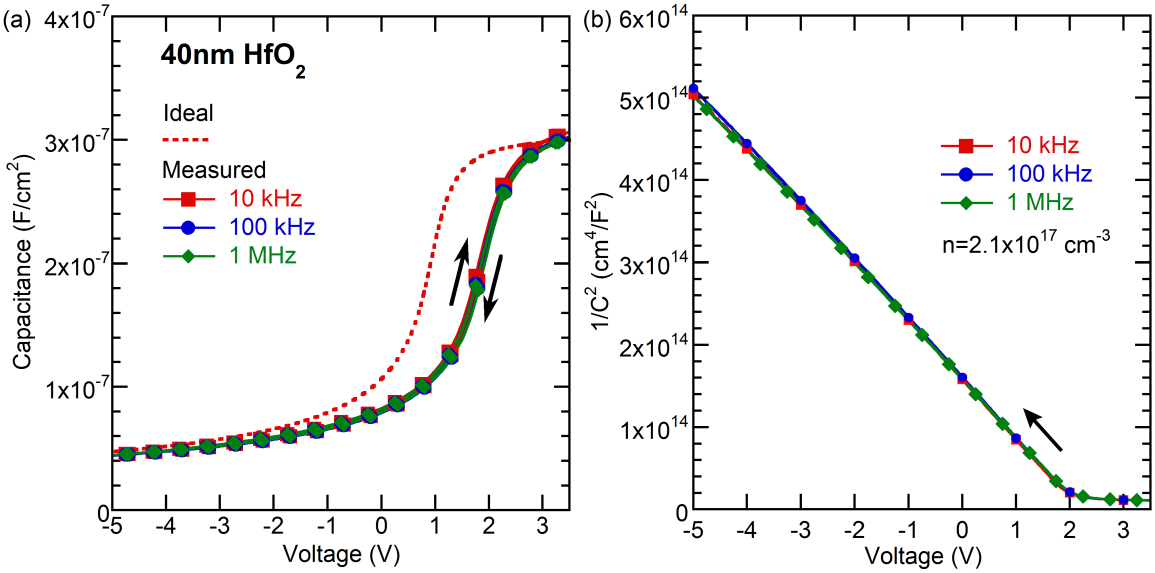


Fig. 4.2. (a) Measured and calculated ideal C-V curves for 40nm $HfO_2$ on $(\bar{2}01)$ $\beta$-$Ga_2O_3$, indicating positive shifts and extremely low hysteresis and stretch-out. (b) The corresponding $1/C^2$-V plot for C-V sweeps from 3.5 V to -5 V, yielding an apparent carrier density of $2.1\times10^{17}$ $cm^{-3}$ (very close to the manufacturer specified $2\times10^{17}$ $cm^{-3}$ carrier concentration).

values for ALD $HfO_2$, with k values between 12–24 having been reported elsewhere [131, 132, 147, 155–157]. The $HfO_2$ films were found to be amorphous and slightly oxygen deficient, with an O:Hf ratio of 1.9:1 from XPS [108]. These factors, combined with any residual impurities from the ALD process, are likely responsible for the lower dielectric constant. Post-deposition annealing is expected to increase the dielectric constant [155]. The measured capacitance response was highly stable as a function of alternating current (AC) measurement frequency in the 10–1000 kHz range, as negligible frequency dispersion was observed. The dual-sweep hysteresis was extremely low ($\leq$ 0.15 V), independent of the measurement frequency. These measurements were stable and repeatable after multiple sweeps over selected bias conditions ranging from a few seconds to a few days apart, suggesting that slow border traps observed with other ALD oxide/$Ga_2O_3$ MOS systems

were not significantly affecting the measurements reported presently [130].

Comparison to the ideal C-V curve indicated a ≈1 V positive shift in the measured C-V curves ($V_{fb}$ of 1.1 V and 2.15 V for the ideal and measured cases, respectively), leading to an estimated negative fixed/oxide charge density of $3\times10^{-7}$ C/cm$^2$. Sweeps to +5 V forward bias (not shown) resulted in further shifting of up to an additional 1.5 V. The positive shift in the C-V curves, along with an average extracted threshold voltage $V_t$ of +1.05 V, suggest that the Au/$HfO_2$/$Ga_2O_3$ structure could be useful for achieving normally-off behavior for n-channel $Ga_2O_3$ MOSFETs. However, the exact origin of these shifts is still a topic of investigation. A similar shift was recently reported in enhancement-mode $Al_2O_3$/$Ga_2O_3$ finFETs and was speculated to arise from interface trap states and/or Fermi level pinning [158]. Furthermore, Moser, et al. observed a strong dependence of C-V shifts on $Ga_2O_3$ doping density in $HfO_2$/$Ga_2O_3$ MOSFETs, with more positive shifting for reduced $Ga_2O_3$ doping density down to a level ($7\times10^{17}$ cm$^{-3}$) that is comparable to those used in this chapter ($\approx2\times10^{17}$ cm$^{-3}$) [159].

Various methods have been reported for quantifying interface trap density ($D_{it}$) for high quality ALD oxides on $Ga_2O_3$ [106, 107]. True quasi-static/low frequency methods are very difficult to perform in this case, given the lack of minority carriers in doped n-type $Ga_2O_3$. This leaves high frequency methods, such as the Terman method, which compares the gate voltages for the calculated ideal high-frequency C-V curves to those of the "stretched out" real high-frequency C-V curves at a given surface potential $\phi_s$ in weak depletion to find $D_{it}$ using Eqn. 4.3 [160]:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{dV_g}{d\phi_s} - 1\right) - \frac{C_s}{q} = \frac{C_{ox}}{q^2}\frac{d\Delta V_g}{d\phi_s} \tag{4.3}$$

wherein $C_{ox}$ = oxide capacitance, $V_g$ = measured gate voltage, $C_s$ = semiconductor depletion capacitance, and $\Delta V_g = V_{g,\,measured} - V_{g,\,ideal}$. Terman calculations can be used to easily probe interface trap states near the conduction band, with the interface trap energy $E_{trap}$ being determined through Eqn. 4.4:

$$E_{trap} = \frac{E_g}{2} + \phi_s + \left(\frac{k_B T}{q}\right) \ln\left(\frac{N_D}{n_i}\right) \tag{4.4}$$

The $1/C^2$–V curves (shown in Fig. 4.2b) extracted from the measured C-V data are highly linear at voltages below flatband, indicating a constant apparent carrier density of $2.1\times10^{17}$ $cm^{-3}$ that closely matched specifications from the substrate manufacturer ($2\times10^{17}$ $cm^{-3}$) and separate Hall effect measurements. Therefore, Eqns. 4.2 and 4.3 were readily applicable to estimate $D_{it}$, with the extracted values shown in Fig. 4.3. Averaging the extracted values gives $D_{it} = 1.3\times10^{11}$ $cm^{-2}\cdot eV^{-1}$ for the $HfO_2/Ga_2O_3$ MOS system at trap energies of $E_c$-0.6 V $\leq E_{trap} \leq$ $E_c$-0.2 V. This value is indicative of a high quality $HfO_2/Ga_2O_3$ interface, and compares very favorably to other ALD gate oxides on bulk $Ga_2O_3$, including $SiO_2$ ($D_{it} \geq 6\times10^{11}$ $cm^{-2}\cdot eV^{-1}$) and $Al_2O_3$ ($D_{it} \geq 2.3\times10^{11}$ $cm^{-2}\cdot eV^{-1}$). Results in those studies were obtained using the Terman, conductance, hi-lo, and UV-assisted methods, and were among the first reported for a $Ga_2O_3$ device. The Terman method has well-reported complications due to inaccuracies in calculation of the ideal C-V curve, e.g. due to nonuniformity in semiconductor doping density [128,160]. However, Zeng et al. have demonstrated reasonable agreement between the Terman and the conductance methods when applied to $Ga_2O_3$ MOS capacitors [106]. Furthermore, the Terman method is primarily applicable to shallow trap states near the conduction band edge; it is likely that

high-temperature methods (e.g. Gray-Brown) will be required to provide insight into deep traps ($E_{trap} \leq E_c$-0.6 V) in future studies of ultra-wide bandgap semiconductors [128, 160].

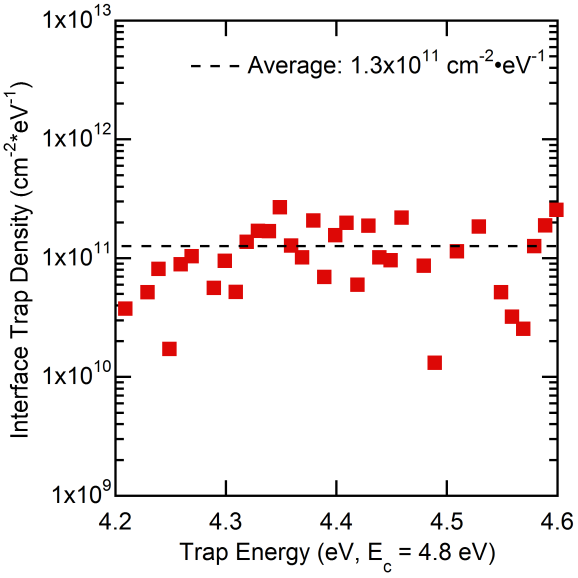


Fig. 4.3. Interface trap density estimations using the Terman method for representative $HfO_2/Ga_2O_3$ C-V curves, with an average $D_{it}$ from all data points shown of $1.3\times10^{11}$ $cm^{-2}\cdot eV^{-1}$ for $E_c$-0.6 V $\leq E_{trap} \leq E_c$-0.2 V.

### 4.3.2 Current-Voltage Measurements

The measured MOS capacitor leakage current under negative bias was about $10^{-8}$ A/cm$^2$ at -5 V. The forward leakage current measured under bias from 0 to +20 V is shown in Fig. 4.4a; the $HfO_2$ supported an electric field strength up to 5 MV/cm (+20 V, assuming the field drop occurs only within the oxide for simplicity) without sharp increases in leakage current. This data was fit to the Fowler-Nordheim (F-N) model for tunneling through a partial barrier under forward bias, as given by Eqn. 4.5 [128]:

$$J_{FN} = \frac{q^2 E_{ox}^2}{16\pi^2 \hbar \phi_{ox}} \exp\left(\frac{-4\sqrt{2m^*}\,(q\phi_{ox})^{\frac{3}{2}}}{3\hbar q E_{ox}}\right) \tag{4.5}$$

where $E_{ox}$ = electric field in the oxide, m* = effective mass of electrons in the $HfO_2$ (taken to be 0.11 times the electron rest mass) [161], and $\phi_{ox}$ = barrier height between the oxide and $Ga_2O_3$ conduction bands (aka CBO). The barrier height can thus be extracted from the slope of the $\ln(J/E_{ox}^2)$ vs. $1/E_{ox}$ plot near the highest forward bias/field strength, as shown in Fig. 4.4b. From this slope, the CBO was calculated as $\phi_{ox}$ = 1.30 eV, which was identical to the CBO previously determined from XPS (1.3 eV) for $HfO_2$ on $Ga_2O_3$ [108]. The excellent fit to the F-N model also indicates that the forward leakage is not controlled by bulk or interfacial defects in the $HfO_2$ or $Ga_2O_3$, another sign of a high quality $HfO_2/Ga_2O_3$ interface.

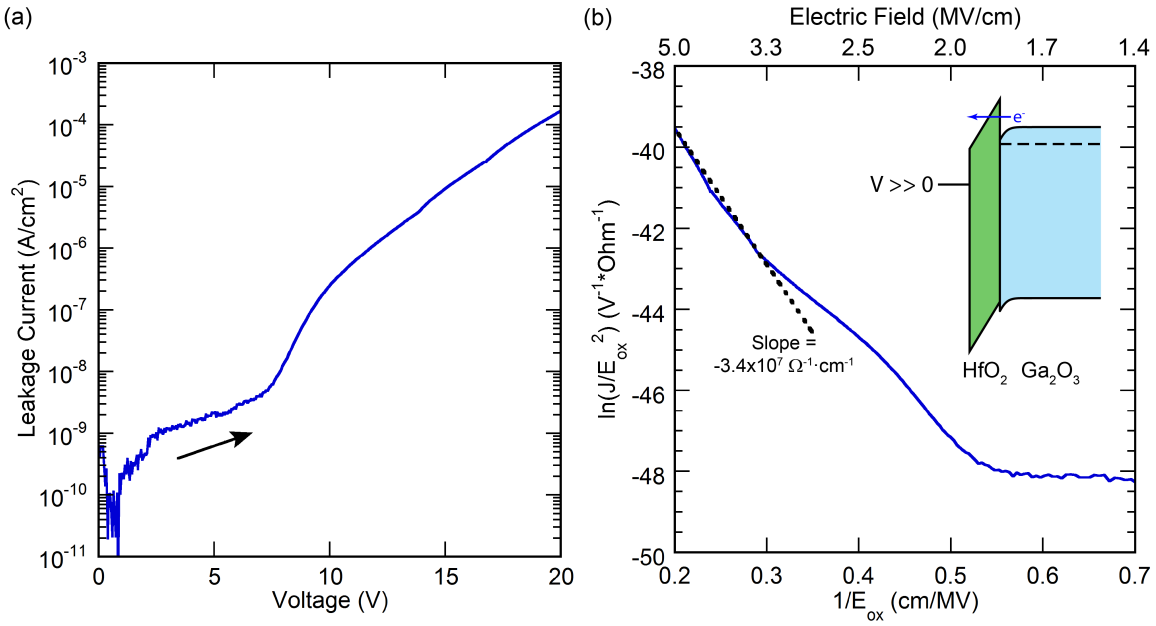


Fig. 4.4. (a) Forward bias leakage current measurement and (b) corresponding F-N plot for 40 nm $HfO_2$ on $Ga_2O_3$. The slope of the $\ln(J/E_{ox}^2)$-$1/E_{ox}$ plot was used to extract a 1.3 eV CBO for the $HfO_2/Ga_2O_3$ that closely matches the value determined from XPS [108]. This slope was extracted at the highest field (5 MV/cm) to ensure that the leakage current was due to true F-N tunneling through a triangular potential barrier.

## 4.4 $ZrO_2/Ga_2O_3$ MOS Systems

### 4.4.1 Capacitance-Voltage Measurements

The capacitance behavior of the ZTB- and TDMAZ-$ZrO_2$ films is shown in Fig. 4.5. Dielectric constants of k = 24 (ZTB) and k = 18 (TDMAZ) were extracted from the 10 kHz C-V measurements. As in the case of $ZrO_2$ films on GaN discussed in Chapter 3, C-V sweeps again highlighted an anomalous frequency dispersion in the $ZrO_2$ accumulation capacitance. The dispersion in the ZTB films, with k decreased from 23.6 at 10 kHz to 16.5 at 1 MHz, was expected given similar observations in the GaN MOS systems. Unlike before, however, the TDMAZ film dielectric constant also showed a slight decrease from k = 18 to k = 16 across the same frequency range. While the ZTB dispersion has been linked to the presence of excess oxygen and negative oxide charge, the dispersion in the TDMAZ-$ZrO_2$ may be a result of residual oxidant species or contamination in the film. Frequency dispersion has been reported elsewhere for $ZrO_2$ grown by thermal ALD using $H_2O$ as the oxidant and arises from residual oxidant species creating defects in the film [145, 148]. Post-measurement corrections for C-V curves on lossy dielectrics have been reported elsewhere, but were not applied to the data presented here [162, 163].

Comparison to the ideal C-V curves indicated a +0.9 V positive shift in the measured $V_{fb}$. As similar observations were made for the $HfO_2/Ga_2O_3$ MOS capacitors discussed earlier in this chapter, the fixed charge may be due to a substrate effect or some product of the thermal ALD process on $Ga_2O_3$ substrates, rather than a characteristic unique to one of the dielectrics. The positive C-V curve shifts were again repeatable over multiple

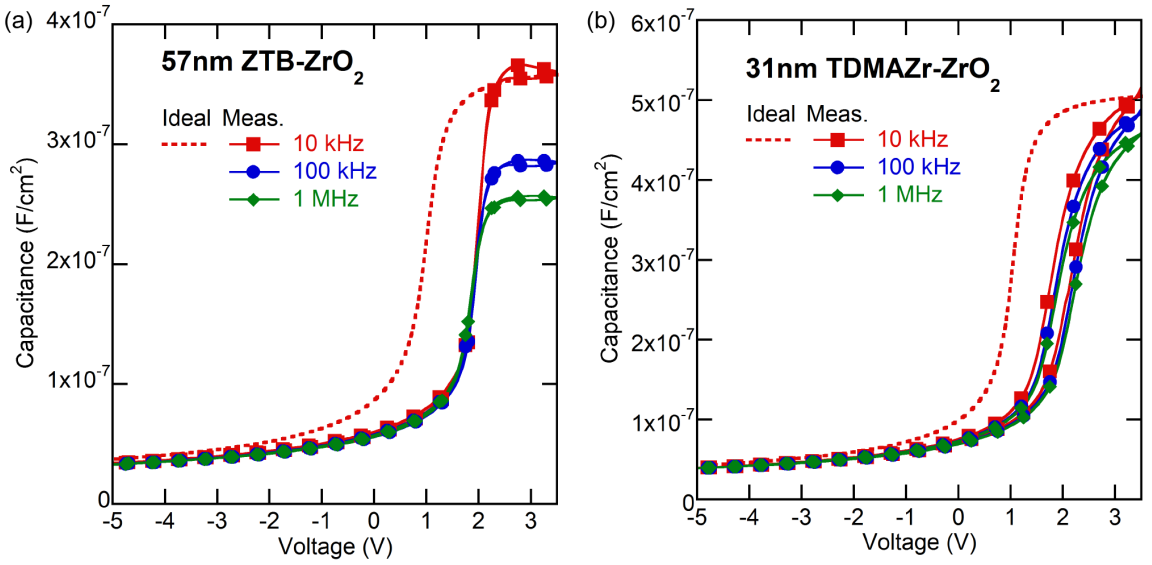


Fig. 4.5. Measured and ideal C-V curves for (a) 57 nm ZTB-$ZrO_2$ and (b) 31 nm TDMAZ-$ZrO_2$ on $(\bar{2}01)$ $\beta$-$Ga_2O_3$.

measurements and therefore not due to the border trapping observed in other $Ga_2O_3$ MOS systems [130].

Comparison of the calculated and measured cases indicated a "compression" of the measured ZTB C-V curves rather than the stretch-out expected from interface trapping effects. This can be explained through extraction of the $1/C^2$–V relationship from the measured C-V curves, shown in Fig. 4.6. The ideal curves shown in Fig. 4.5 assume a constant carrier density, as extracted from the slope of the linear (depletion) region of the $1/C^2$–V data for each dielectric. This assumption does not hold true for the ZTB films excess oxygen defects. At voltages just below flatband and into weak depletion, the measured data for the ZTB deviates from linearity (the dashed black line in Fig. 4.6 serves as a visual guide). As the slope of the $1/C^2$–V plot gives an "apparent" carrier density in the semiconductor, this deviation suggests non-uniform carrier depletion close to the ZTB/$Ga_2O_3$ interface due

to negative dielectric charge. Furthermore, a lower apparent carrier density was extracted from the linear region of the ZTB curve, which may also be related to carrier depletion from the negatively charged excess oxygen. In contrast, the TDMAZ does not exhibit non-linear $1/C^2$–V curves in weak depletion, and the carrier density extracted for the TDMAZ sample closely matched the value extracted from a reference $Au/Ga_2O_3$ Schottky diode.

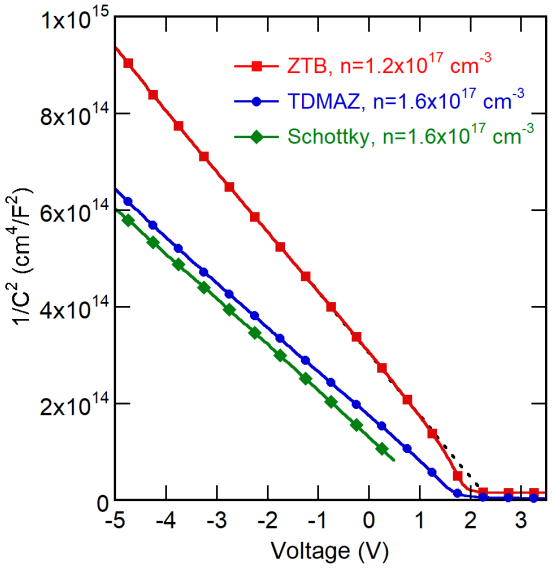


Fig. 4.6. $1/C^2$–V plots and average apparent carrier densities for $ZrO_2/Ga_2O_3$ MOS capacitors. The deviation from linearity in the ZTB capacitor can be observed between +1 V and +2 V where the ZTB data diverges from the dashed guide line. The extracted carrier density is also lower than of the TDMAZ capacitors and reference $Au/Ga_2O_3$ Schottky diodes.

Dual-sweep hysteresis was lower for both dielectrics on $Ga_2O_3$ than on GaN ($\delta V_{fb}$ $\leq$ 0.05 V for ZTB and $\leq$ 0.40 V for TDMAZ), indicating that the oxide-oxide interfaces in this case have fewer trap states than the oxide-nitride interfaces in Chapter 3. These values were used in simple interface trapped charge estimations using the hysteresis method shown previously in Eqn. 3.3 [133, 146]. These values yield estimated $D_{it}$ values of $1.4\times10^{11}$ and $1.3\times10^{12}$ $cm^{-2}$ for the ZTB and TDMAZ dielectrics, respectively, using the maximum

measured $C_{ox}$ values at 10 kHz and assuming each defect state is singly charged. These values are in the range reported elsewhere for $Ga_2O_3$ MOS systems with lower-k dielectrics such as $SiO_2$ and $Al_2O_3$ [106, 107]. However, the hysteresis method is best suited for estimations of MOS interface trap densities, while more accurate determination of $D_{it}$ requires more rigorous techniques such as the Terman or conductance methods. The Terman method used earlier in this chapter could not be successfully applied to the $ZrO_2/Ga_2O_3$ MOS systems described here due to complications arising from the observed frequency dispersion. As such, true determination of the quantity and energy distributions of $D_{it}$ in these films will require other defect spectroscopy techniques such as conductance spectroscopy, high temperature methods, or spectroscopy methods such as deep-level transient spectroscopy (DLTS) [160].

### 4.4.2 Current-Voltage Measurements

Forward bias leakage for both $ZrO_2$ dielectrics are shown in Fig. 4.7. Reverse bias leakage was very low ($\leq$10 nA/cm$^2$ at -5V); the forward bias leakage increased rapidly. Forward leakage through $ZrO_2$ films has been previously described using trap-assisted tunneling (TAT) mechanisms [148, 164]. TAT models of varying complexity have been reported [148, 164–167]. The leakage current density was replotted in terms of ln(J) versus $1/E_{ox}$ and fit to the single-energy TAT model in Eqn. 4.6 [164]:

$$J_{TAT} = A \exp\left(\frac{-4\sqrt{2m^*}\,(q\phi_t)^{\frac{3}{2}}}{3\hbar q E_{ox}}\right) \tag{4.6}$$

Where A = a constant, $E_{ox}$ = electric field in the $ZrO_2$, m* = effective mass of electrons in the $ZrO_2$ (taken to be 0.27 times the electron rest mass) [168], and $\phi_t$ = trap state energy relative to the $ZrO_2$ conduction band. At high forward bias, the leakage current has both F-N and TAT contributions (shown schematically in Fig. 4.9). As such, the exponential argument in the simple TAT model is the same as in the F-N tunneling model, except applied to ln(J) instead of $\ln(J/E_{ox}^2)$ and with the $\phi_t$ term being the energy difference between the trap state and dielectric conduction band instead of between the dielectric and semiconductor conduction bands. The single-energy TAT model fits the ZTB leakage data quite well, which at high forward bias yields the nearly linear $\ln(J)$–$1/E_{ox}$ plot shown in Fig. 4.9, and gives $\phi_t$ = 0.4 V. This value fits well with the trap energies determined by Seo et al. for $ZrO_2$/Si MOS capacitors [164].

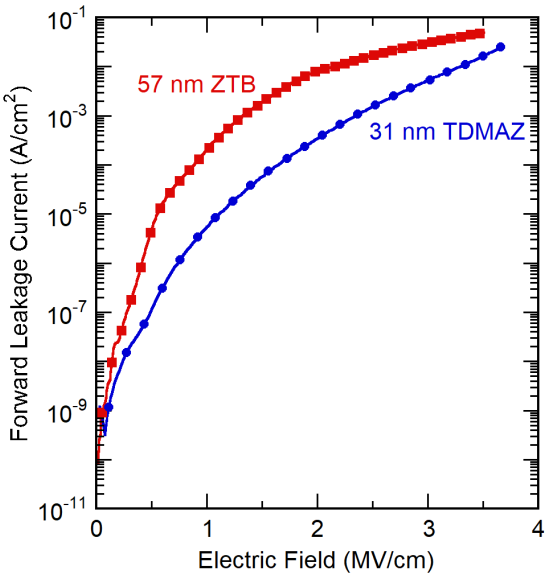


Fig. 4.7. Forward bias leakage current measurements for 57 nm ZTB and 31 nm TDMAZ-$ZrO_2$ films on $Ga_2O_3$.

Similar fitting for the TDMAZ leakage did not produce a linear TAT plot at high

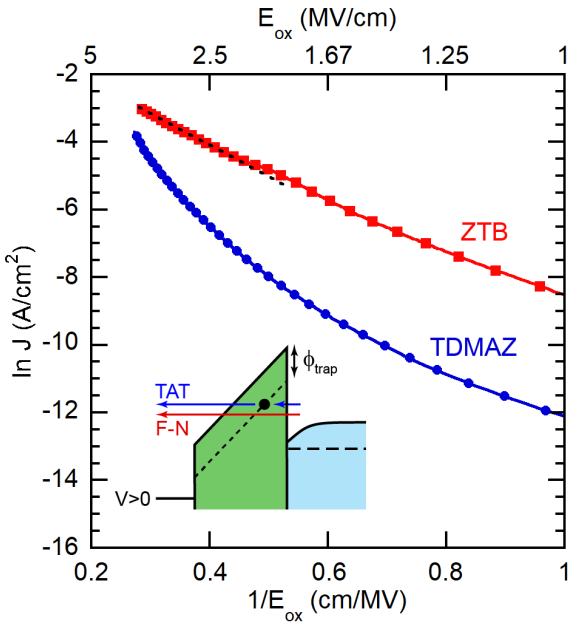


Fig. 4.8. High forward bias leakage plotted as ln(J) versus $1/E_{ox}$ for ZTB and TDMAZ dielectrics, with an inset schematic of the TAT process at high forward bias. A suitable linear fit was obtained for the ZTB data (with the black dashed line serving as a visual guide, with $\phi_t$ = 0.4 eV. A linear fit to the TDMAZ data was not obtained, indicating the need for a different model to describe the leakage data.

forward bias, indicating the need for a different leakage model. Both Poole-Frenkel (P-F) and space charge limited current (SCLC) models were thus considered, as the respective plots for each leakage model shown in Fig. 4.9 exhibited linear regions of the TDMAZ data. P-F emission current occurs when charge can migrate into the dielectric and subsequently jump into the conduction band due to thermal fluctuations, according to the model in Eqn. 4.7 [128]:

$$J_{PF} = E_{ox} \exp\left(\frac{-q\left(\phi_t - \sqrt{\frac{qE_{ox}}{\pi\epsilon_0 k}}\right)}{k_B T}\right) \tag{4.7}$$

Where in this case $\phi_t$ = barrier height between the trap state and the dielectric conduction band. By plotting $\ln(J_{PF}/E_{ox})$ versus $E_{ox}^{0.5}$ (Fig. 4.9a) and finding the intercept at $E_{ox}^{0.5} = 0$, a $\phi_t$ value of 0.61 eV can be extracted for the TDMAZ system. Furthermore, the slope gives

a dielectric constant value of k = 16.5, which closely matches the high frequency (1 MHz) dielectric constant determined from C-V measurements. However, confirmation of P-F conduction requires confirmation that the dielectric constant extracted from these electrical measurements matches the value found from optical measurements such as spectroscopic ellipsometry [164]. Temperature-dependent I-V measurements would also be useful in fully characterizing the leakage behavior.

The SCLC leakage model describes a condition where large amounts of charge in high forward bias limits the current leaking through the dielectric, and has been reported previously for the $ZrO_2$/Si MOS system [164]. The large leakage current present in high forward bias suggest that SCLC may also affect the TDMAZ leakage observed. This phenomenon is described in terms of Eqn. 4.8:

$$J_{SCLC} = \left(\frac{9}{8}\right) \frac{\epsilon_0 k(\mu\theta)V^2}{d^3} \tag{4.8}$$

Where $\mu$ = electron mobility, and $\theta$ = a parameter related to trap state density and energy. Fitting the linear portion of the J–$V^2$ plot (Fig. 4.9c) to Eqn. 4.8 allows determination of a $\mu\theta$ value of $2.4\times10^{-9}$ $cm^2/V\cdot sec$ for the TDMAZ. Small values of $\mu\theta$ ($<10^{-9}$ $cm^2/V\cdot sec$) indicate an SCLC mechanism [169], which may be caused in this case by both the accumulation charge in the $Ga_2O_3$, the oxide and interface charge observed from the C-V measurements, and the large current density leaking through the dielectric. The $\mu \cdot \theta$ product can be further refined to determine carrier mobility, trap density, and trap energy [164], but the temperature-dependent I-V measurements have not been performed at this time.

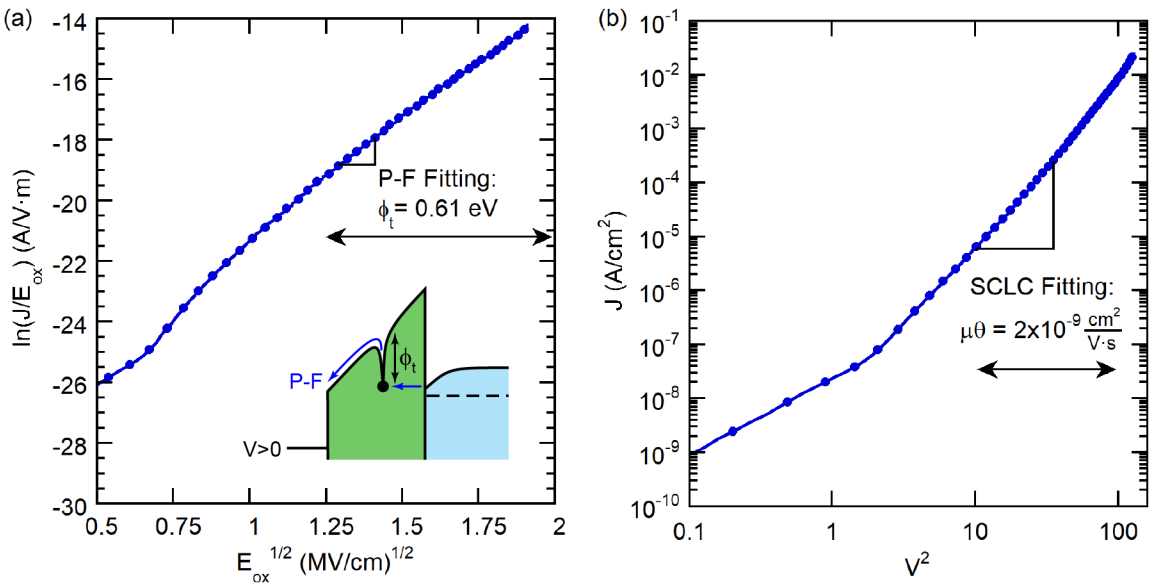


Fig. 4.9. TDMAZ-$ZrO_2$ forward bias leakage plotted as (a) $\ln(J/E_{ox})$–$E_{ox}^{1/2}$ for the P-F model, and (b) J–$V^2$ for the SCLC model.

## 4.5 Chapter Summary

ALD $HfO_2$ and $ZrO_2$ are appealing dielectrics for integration with $\beta$-$Ga_2O_3$. $HfO_2$/$Ga_2O_3$ and $ZrO_2$/$Ga_2O_3$ MOS capacitors have been characterized electrically using C-V and I-V measurements. Measurements of positive flatband and threshold voltages for these dielectrics suggest that $HfO_2$ and $ZrO_2$ are potential candidates for use in normally-off $Ga_2O_3$ transistors. However, all three dielectrics exhibited comparable positive shifts; this indicates that the origin of these shifts may be related to substrate- or ALD-related effects, rather than the fixed oxide charge observed in the GaN MOS systems studied in Chapter 3. Excellent C-V characteristics were observed for $HfO_2$ films, which exhibited C-V curves with minimal hysteresis, stretch-out, and frequency dispersion. Application of the Terman method indicated an average $D_{it}$ of $1.3\times10^{11}$ $cm^{-2}\cdot eV^{-1}$ in the $E_c$-0.6 V $\leq E_{trap} \leq$ $E_c$-0.2

V range. This result is competitive with trap densities reported for ALD $SiO_2$ and $Al_2O_3$ on $\beta$-$Ga_2O_3$. $ZrO_2$ deposited using the ZTB and TDMAZ precursors exhibited frequency dispersion in their C-V curves, along with other nonuniformities in the measured data that complicated detailed determinations of interface trap density. Estimation of total $D_{it}$ using the hysteresis method yielded total interface trap density values of $1.4\times10^{11}$ and $1.3\times10^{12}$ $cm^{-2}$, without regard to the energy distribution of the traps. Application of other methods to probe interface traps, such as the conductance method or elevated-temperature methods, will allow more detailed characterization of the energy distribution of these trap states.

The forward bias I-V characteristics for each dielectric were fit to several leakage current models at room temperature. For the $HfO_2$ dielectrics, good fitting was obtained with the F-N tunneling model, and a CBO of 1.3 eV was extracted that matched the value determined by XPS in [108]. ZTB-$ZrO_2$ I-V characteristics were fit to a single energy TAT model, with a trap state energy of 0.4 eV below the conduction band, while TDMAZ-$ZrO_2$ I-V characteristics were better fit to the P-F (trap energy of 0.61 eV) and SCLC models. Future characterization of these dielectrics with temperature-dependent I-V measurements will allow more detailed understanding of the leakage mechanisms in these dielectrics.

# PART III
# PROCESSING AND CHARACTERIZATION OF WBG AND UWBG SWITCHES

# Chapter 5: $ZrO_2$ Gate Dielectrics for Threshold Voltage Tuning and Low Gate Leakage in AlGaN/GaN MOS-HEMT Switches

## 5.1 Introduction

AlGaN/GaN HEMTs exhibit many advantageous characteristics for advanced power and RF switching [14, 170]. While these devices benefit from the low on-state resistance and high switching speed afforded by the 2DEG formed at the AlGaN/GaN interface, they are limited by normally-on (depletion-mode) behavior and high Schottky gate leakage. A variety of approaches have been undertaken to establish normally-off (enhancement-mode) behavior, including local recessing of the AlGaN barrier to eliminate the 2DEG under the gate [48, 49], thin AlGaN barriers [171], $F^-$ treatment/implantation [172–174], and/or the integration of charged gate layers [50] or p-n junctions [51] to deplete the 2DEG without gate bias. Normally-off behavior typically comes at the expense of reduced current output, higher on-state resistance, and increased current collapse due to charge trapping near the gate. The latter problem of Schottky gate leakage can be solved by integration of a gate dielectric to create a metal-insulator-semiconductor (MIS) or MOS-HEMT, such as AlN, SiN, $Al_2O_3$, $HfO_2$, and $ZrO_2$, with improved reliability and reduced off-state power usage [53–55, 175–177]. Gate dielectric integration also allows increased device output, since the gate can be driven further into forward bias than would be possible with a conventional Schottky gate. However, the incorporation of a MIS/MOS gate structure often results in a negative threshold voltage shift due to the increased effective barrier thickness between the gate and 2DEG. This makes achieving low gate leakage and normally-off behavior in a single device a non-trivial accomplishment.

As part of this dissertation work, AlGaN/GaN MOS-HEMTs with extremely positive threshold voltages (+4 V) and low gate leakage were produced through a combination of AlGaN barrier recess etching and incorporation of the negatively-charged ZTB-$ZrO_2$ as the gate dielectric [178]. $ZrO_2$ is an appealing dielectric for GaN HEMTs, and the multiple precursor systems available for $ZrO_2$ ALD allow incorporation of gate dielectrics with varying amounts of negative fixed oxide charge, as indicated by the C-V results in Chapter 3. Appropriate dielectric selection thus enables gate charge engineering and threshold voltage tuning in functional AlGaN/GaN HEMTs.

This chapter reports novel AlGaN/GaN HEMTs with combinations of AlGaN barrier recess etching and $ZrO_2$ dielectrics with varying amounts of negative oxide charge using the ZTB and TDMAZ precursors reported in Chapter 3. These techniques enable threshold voltage control over an extremely wide range of 7 V for a given AlGaN/GaN HEMT structure. Furthermore, $SiN_x$ passivation outside of the gate has been introduced to achieve improved current collapse in the device access regions.

## 5.2 MOS-HEMT Device Fabrication

MOS-HEMTs and reference Schottky-gated HEMTs were fabricated from a commercial MOCVD-grown AlGaN/GaN structure (20 nm AlGaN thickness) on a highly resistive Si substrate, as shown schematically in Fig. 5.1. The original structure had a sheet resistance ($R_{sh}$) of 572 Ω/square, mobility ($\mu_n$) of 1618 $cm^2/V{\cdot}sec$, and sheet carrier density of $6.7\times10^{12}$ $cm^{-2}$ as indicated by Hall Effect measurements on Van der Pauw (VdP) structures fabricated in parallel with the HEMTs. Isolated device mesas were defined with a $Cl_2$/Ar

inductively-coupled plasma (ICP) etch. Ohmic contacts were produced by e-beam evaporation and lift-off of Ti/Al/Ni/Au, followed by rapid thermal annealing (RTA) at 850 °C for 30 sec in flowing $N_2$. Additional Ti/Au overlay metal was evaporated onto the Ohmics for easier electrical probing. An optimized bi-layer $SiN_x$ passivation stack was deposited by plasma-enhanced chemical vapor deposition (PECVD) [62]. Contact and gate recess windows were etched through the $SiN_x$ with $SF_6$-based reactive ion etching (RIE). AlGaN recess etching was performed on some devices using a $BCl_3/Cl_2/Ar$ ICP process, timed to etch just through the barrier layer with minimal etching of the GaN buffer layer underneath. Etching increased $R_{sh}$ to 80 k$\omega$/square on corresponding recessed VdP structures, indicating that the 2DEG had been eliminated by the etch. Samples were cleaned with a 10 min $UV/O_3$ exposure, followed by a 30 sec soak in 10:1 $H_2O$:HCl, and a very short ($<$1 sec) soak in 10:1 buffered oxide etch ($NH_4F$:HF). 40 nm $ZrO_2$ gate dielectrics were deposited by thermal ALD at 200 °C using either ZTB or TDMAZ and deionized $H_2O$ precursors by the processes described in Chapter 3. Dielectric thickness was determined from ellipsometry measurements. Based on the MOS capacitor data presented in Chapter 3, both dielectrics are expected to a low-frequency dielectric constant of k $\approx$ 25. Negative oxide charge on the order of $10^{12}$ $cm^{-2}$ is expected for the ZTB-$ZrO_2$ dielectric, while much less oxide charge is expected for the TDMAZ-$ZrO_2$. Finally, metal gates were deposited by evaporation and lift-off of Ni/Au. The final devices had a gate-source length ($L_{gs}$) of 2.5 $\mu$m, gate length ($L_g$) of 3 $\mu$m and gate width ($W_g$) of 75 $\mu$m, and gate-drain length ($L_{gd}$) of 10 $\mu$m.

Fabricated devices were characterized using static I-V measurements on a Keithley 4200 semiconductor parameter analyzer. Pulsed I-V measurements were also performed using an Accent DiVA analyzer to determine dynamic on-resistance under switching con-

ditions. Measurements were performed under off-state quiescent bias conditions, with an off-state gate bias of $V_{gs,q} = V_t$–2 V, quiescent drain bias varying between $V_{ds,q}$ = 0–50 V, and a pulse width of 200 ns.

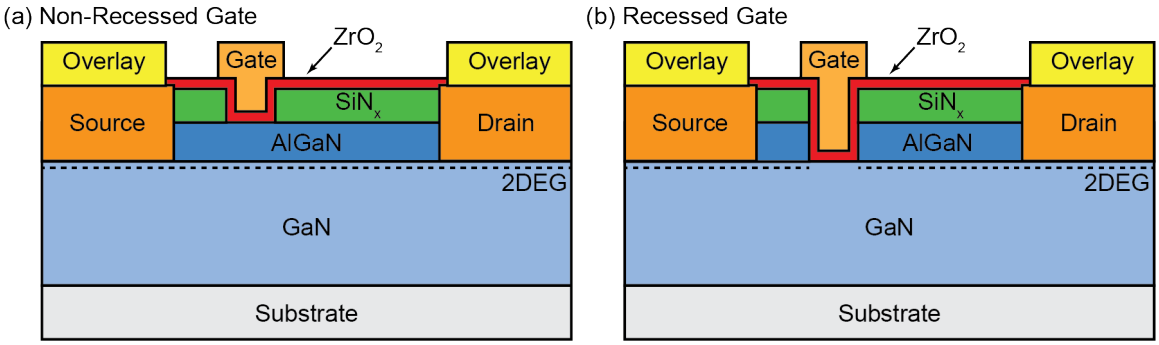


Fig. 5.1. Schematics of $ZrO_2$ MOS-HEMTs with (a) non-recessed and (b) recessed gates.

## 5.3 $ZrO_2$ MOS-HEMT Operation Characteristics

Relevant device parameters for the $ZrO_2$ MOS-gated and reference Schottky-gated HEMTs are shown in Table 5.1. The effect of $ZrO_2$ dielectric integration on the non-recessed structures is readily apparent from the transfer characteristics ($I_d$-$V_g$ curves) in Fig. 5.2. Up to +10 V gate bias was applied to the $ZrO_2$ MOS-HEMTs due to the lower gate leakage associated with a MOS gate compared to the reference Schottky gates. For the non-recessed MOS-HEMTs, the negative oxide charge associated with the ZTB-grown $ZrO_2$ led to a $V_t$ shift of +1.85 V compared to the reference HEMT. This value is comparable to the positive $\Delta V_{fb}$ observed in the ZTB-$ZrO_2$/GaN MOS capacitors reported in Chapter 3. Meanwhile, incorporation of the TDMAZ-grown dielectric (with comparatively little oxide charge) caused a negative $V_t$ shift of -1.04 V. This is expected due to the increased effective barrier thickness between the gate metal and 2DEG in the un-charged $ZrO_2$.

Table 5.1. Representative characteristics for $ZrO_2$ MOS-gated and reference Schottky-gated HEMTs.

| Parameter | Reference | ZTB No Recess | TDMAZ No Recess | ZTB Recess | TDMAZ Recess |
|---|---|---|---|---|---|
| $V_t$ ($V_{ds}$ = 1 V, V) | -2.11 | -0.26 | -3.15 | +3.92 | +0.11 |
| $g_{m,max}$ ($V_{ds}$ = 10 V, mS/mm) | 122 | 150 | 112 | 53.9 | 39.7 |
| $\mu_{n,FE}$ ($cm^2/V{\cdot}sec$) | 1687 | 1916 | 1450 | 519 | 74 |
| $I_{ds,max}$ @ $V_{gs,max}$ (mA/mm) | 565 | 592 | 551 | 198 | 285 |
| $R_{on}$ ($\Omega{\cdot}mm$) | 17.1 | 9.93 | 10.9 | 22.7 | 24.5 |
| $\Delta R_{on,dyn}$ ($V_{dsq}$ = 50 V, %) | 28 | 412 | 511 | 21 | 1 |

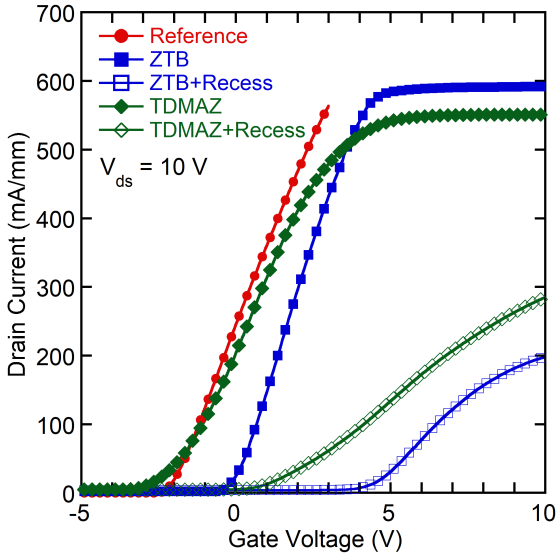


Fig. 5.2. Transfer characteristics ($I_d$-$V_g$) at $V_{ds}$ = +10 V for $ZrO_2$ MOS-HEMTs and Schottky-gated reference HEMTs.

Gate recess etching led to positive shifts for both MOS-HEMT structures compared to their non-recessed counterparts, with the recessed ZTB MOS-HEMTs exhibiting very strong enhancement-mode operation ($V_t$ = +3.92 V) and the recessed TDMAZ MOS-HEMTs just barely reaching a positive $V_t$ ($V_t$ = +0.11 V). These shifts (+4.18 V for the ZTB and +3.26 V for the TDMAZ dielectrics, respectively) are in line with theory for recess etching on

typical HEMT structures (no MOS gates). Saito et al. previously showed that a maximum $V_t$ of roughly +1.5–2 V is theoretically achievable with a full barrier recess in an AlGaN/GaN heterostructure [179]. For the non-recessed reference HEMTs ($V_t$ = -2.11 V), a full recess etch should result in a positive $V_t$ shift of ≈ +4 V, which agrees well with the positive shifts observed in the recessed $ZrO_2$ MOS-HEMTs. Therefore, the combination of recess etching and $ZrO_2$ integration offers threshold voltage control over a nearly 7 V range, up to a maximum of +3.92 V for the recessed ZTB MOS-HEMTs. The maximum value is very close to the previous result from devices with ZTB-$ZrO_2$ as the gate dielectric and without $SiN_x$ passivation [178] and is among the highest positive $V_t$ values observed for any AlGaN/GaN HEMT [177]. Addition of the $SiN_x$ passivation layer therefore did not have a significant effect on $V_t$, but is expected to improve charge trapping under static and dynamic I-V conditions.

Conventional methods for extracting carrier field-effect mobility ($\mu_{n,FE}$) from the device transfer characteristics at low drain bias ($V_{ds}$ = 0.1 V) cannot be reliably used for a conventional power HEMT, as contact resistance and other parasitic resistance effects from the relatively large source-gate and gate-drain access regions outside the gate are ignored [180–182]. A method of correcting for these effects was developed by Aminbeidokhti et al. to allow extraction of the field-effect mobility in the 2DEG via Eqn. 5.1: [183]

$$\mu_{n,FE} = \frac{n_{gate} V_{ds}}{C_{gate}\left(\frac{1}{g_m} - R_{sh} n_s\right)\left(V_{ds} - (R_{sh} n_s + R_{sh} n_d + R_{s,c} n_c) I_{ds}\right)^2} \tag{5.1}$$

where the $n_{gate}$, $n_s$, and $n_d$ account for the relative geometries of the gate and access regions ($n_{gate}$ = $L_g/W_g$, $n_s$ = $L_{gs}/W_g$, $n_d$ = $L_{gd}/W_g$), $R_{sh}$ is the sheet resistivity of the 2DEG channel,

and $R_{s,c}n_c$ is the combined source and drain contact resistance $R_c$ obtained from transfer length method (TLM) measurements [160]. For these HEMTs, $R_{sh}$ was taken from the Hall effect measurements reported in the device fabrication section. $R_c$ was not directly measured, but was assumed to be 30 Ω based on TLM measurements on similar samples that underwent identical contact processing. The peak values of $\mu_{n,FE}$ determined from these calculations are reported in Table 5.1, using maximum transconductance values ($g_{m,max}$) at $V_{ds}$ = 0.1 V and appropriate gate capacitance values ($C_{gate}$), assuming dielectric constants of k = 9.3 for the 20 nm AlGaN and k = 25 for the 40 nm $ZrO_2$. For the reference HEMTs, the peak $\mu_{n,FE}$ of 1687 $cm^2/V{\cdot}sec$ was in good agreement with the Hall mobility of 1618 $cm^2/V{\cdot}sec$. $ZrO_2$ incorporation in the non-recessed MOS-HEMT structure yielded mobility values on the same order of magnitude as the reference HEMTs. The highest mobility was achieved using the ZTB dielectric, which is likely due to the negative dielectric charge causing a reduction in 2DEG carrier density. Channel mobility was significantly reduced in the recessed MOS-HEMTs due to recess etch-induced plasma damage and destruction of the 2DEG underneath the gate [178], with higher mobility again observed in the ZTB-gated devices. These trends show the same order of magnitude change observed in gated-Hall Effect measurements reported previously in Anderson et al., with +8 V biasing returning the sheet carrier density in recessed VdP structures close to original values while showing an order of magnitude reduction in mobility [178]. However, the accuracy of these extractions could be further improved by use of measured rather than assumed values for the gate capacitances and contact resistances on each device structure, but the necessary measurements have not been performed at the time of this work.

Device output characteristics are shown in Fig. 5.3. The ability to drive the MOS-

gated HEMTs to much higher forward bias conditions (up to +10 V, versus +2 V for the Schottky gates) allowed comparable or even superior output current ($I_{ds,max}$) and on-resistance ($R_{on}$) to be achieved in the non-recessed devices. Enhancement-mode operation in the recessed MOS-HEMTs unsurprisingly came at the expense of degraded $I_{ds,max}$ and increased $R_{on}$, again due to plasma damage and 2DEG removal under the gate. Recovery of $I_{ds,max}$ and $R_{on}$ may be possible through annealing or TMAH soaking to heal or remove plasma damage, but this has not yet been explored in these MOS-HEMTs [184].

Fig. 5.4 shows the dynamic on-resistance ($R_{on,dyn}$) extracted from pulsed I-V measurements between $V_{ds,q}$ = 0–50 V. The condition $V_{ds,q}$ = 0 V represents the same testing condition as the static I-V measurements shown earlier, and the initial $R_{on,dyn}$ values reflect the same trends as $R_{on}$ extracted from the static I-V sweeps in Fig. 5.3. Dynamic switching at higher $V_{ds,q}$ values revealed increased $R_{on,dyn}$ and degraded current collapse behavior in the ZTB MOS-HEMTs. This was expected from enhanced charge trapping in the negatively charged ZTB dielectric, despite integration of $SiN_x$ passivation in the device access regions. $R_{on,dyn}$ was further degraded by recess etching, as the trap states in the dielectric were moved physically closer to the GaN layer. Meanwhile, both non-recessed and recessed MOS-HEMTs with the TDMAZ dielectrics exhibited good current collapse, with non-recessed devices exhibiting a smaller $R_{on,dyn}$ increase than even the reference Schottky-gated HEMTs. This indicates a high quality TDMAZ dielectric with very little charge and trap states compared to the ZTB.

$ZrO_2$ integration successfully reduced gate leakage by at least five orders of magnitude compared to Ni/Au Schottky gating under both forward and reverse gate bias (Fig. 5.5). Extremely low leakage currents were observed under reverse bias for the ZTB and TDMAZ

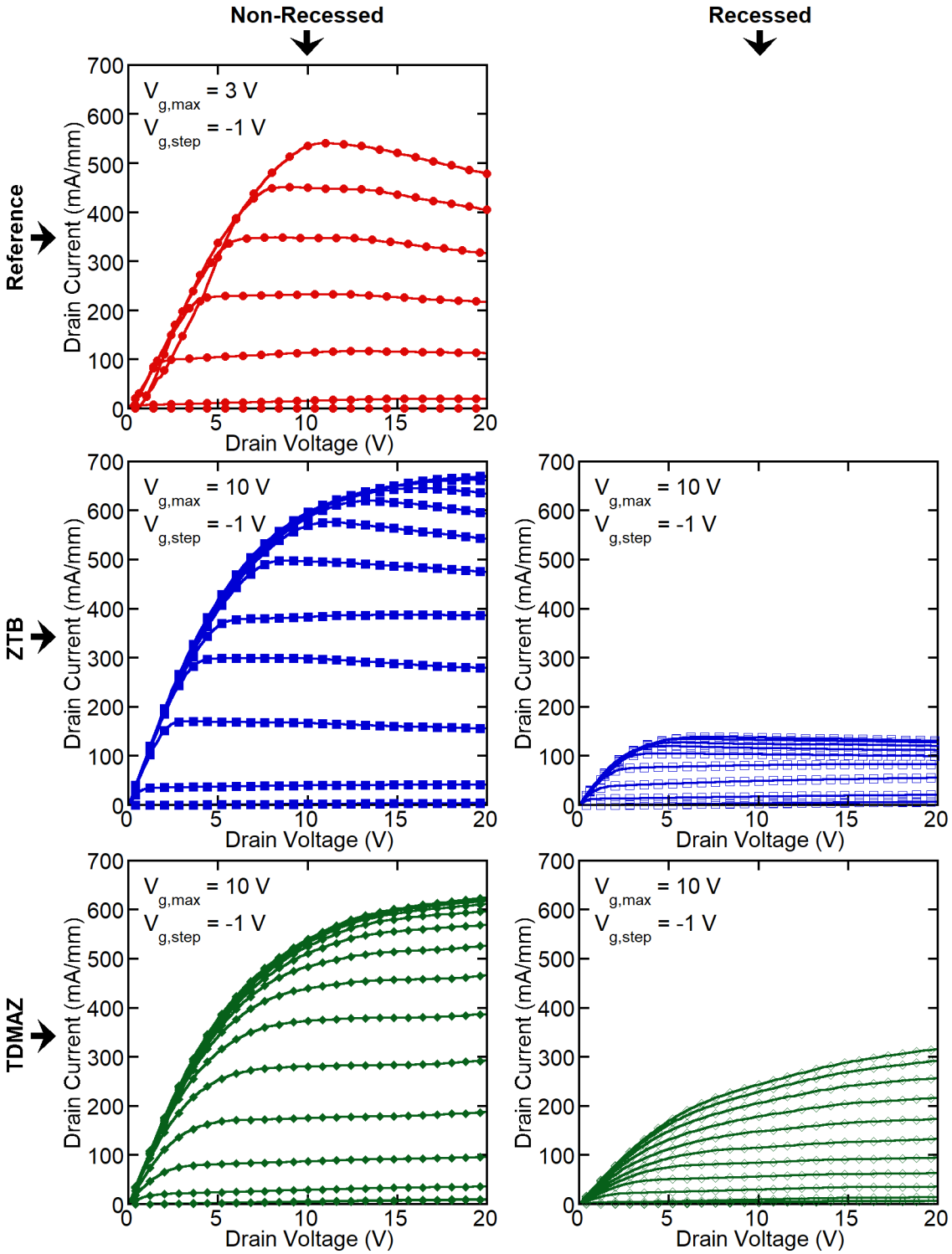


Fig. 5.3. Output characteristics ($I_d$-$V_d$) for $ZrO_2$ MOS-HEMTs and Schottky-gated reference HEMTs.

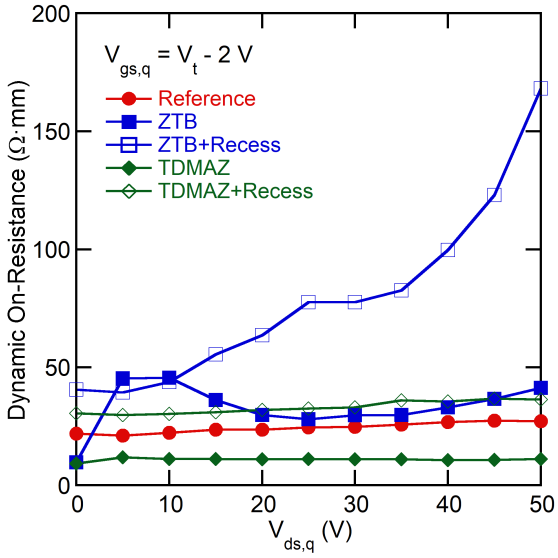


Fig. 5.4. Dynamic on-resistance of $ZrO_2$ MOS-HEMTs and reference HEMTs as a function of quiescent drain-source voltage under off-state conditions.

MOS-HEMTs. Under forward bias, gate leakage was higher for the ZTB MOS-HEMTs than their TDMAZ counterparts by 2–5 orders of magnitude. This was an expected consequence of the negative oxide charge and other trap states in the ZTB dielectric, as trap-assisted forward-bias leakage mechanisms have been observed in $ZrO_2$ dielectrics [148, 164]. Despite this, leakage for the ZTB MOS-HEMTs at $V_{gs}$ = +10 V was still lower than the Schottky gate leakage for the reference HEMTs when operated at or above the typical gate bias of $V_{gs}$ = +1V. Recess etching did not significantly change the forward gate leakage behavior of either dielectric, indicating that etch damage contributions to the recessed gate leakage were minimal. Both non-recessed and recessed MOS gates with $ZrO_2$ dielectrics are thus viable options for reduced gate leakage compared to standard Schottky metallization. This reduced leakage, combined with the demonstration of both enhancement- and depletion-mode operation, demonstrates that $ZrO_2$ dielectrics and gate recessing offer a route to overcome key

limitations for AlGaN/GaN HEMTs mentioned previously.

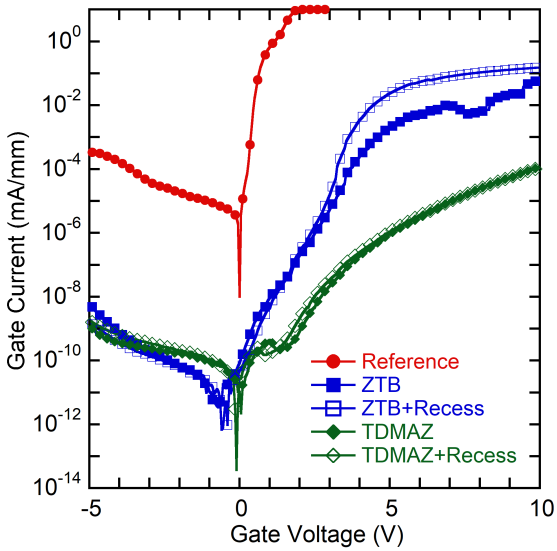


Fig. 5.5. Gate leakage comparison between $ZrO_2$ MOS-HEMTs and Schottky gated HEMTs.

## 5.4 Chapter Summary

AlGaN/GaN MOS-HEMTs were fabricated with ALD-$ZrO_2$ gate dielectrics and AlGaN barrier recesses. Through use of two different Zr-precursors in the ALD process (ZTB and TDMAZ), different amounts of negative charge can be produced in the gate dielectric. Combining these dielectrics with barrier recess etching allows threshold voltage control in AlGaN/GaN HEMTs over an extremely wide range of 7 V. A maximum positive $V_t$ of +3.92 V was achieved through integration of the negatively charged ZTB-$ZrO_2$ dielectric with barrier recessing. MOS gates could be driven to gate-source biases up to +10 V to achieve good output current levels while maintaining around 5 orders of magnitude lower leakage than conventional Schottky gates. Thus, both enhancement-mode operation and low gate leakage can be achieved in a $ZrO_2$ MOS-HEMT, which represents a critical advance in

AlGaN/GaN HEMT technology. However, current collapse under dynamic I-V conditions was significantly worse for ZTB-gated MOS-HEMTs, while the TDMAZ-gated MOS-HEMTs were comparable to or better than Schottky-gated devices. Mitigation schemes for the poor current collapse behavior must be developed, potentially including alternating layers of the low-trapping TDMAZ and negatively-charged ZTB.

# Chapter 6: Design and Process Development to Enable Vertical Trench-Gate GaN MOSFETs

## 6.1 Introduction

Vertical GaN switch architectures, such as the trench-gate MOSFET, are necessary to achieve high voltage power switches ($\geq$1 kV). These devices have advantages over lateral conventional AlGaN/GaN HEMTs, including normally-off behavior, sub-surface conduction, reduced gate leakage currents, and high areal power density [68]. However, even the highest performance devices demonstrated to date still fail to reach these theoretical limits due to a number of complex challenges related to material growth and device fabrication. One such challenge is the characterization of the MOS interfaces with novel high-k dielectrics along etched c-, a-, and m-planes of GaN addressed in Chapter 3 of this dissertation. Additional challenges include development of plasma etching and damage cleanup processes to create and metallize highly vertical gate trenches with minimal plasma damage to the semiconductor, as well as dopant control and Ohmic contact formation to both the n- and p-type GaN layers involved in the required epitaxial layer structure. Activated doping and Ohmic contact formation to the buried p-type body layer is particularly important to allow effective gate biasing and n-channel formation. This chapter reports epitaxial structure design and processing to enable vertical trench-gate GaN MOSFETs, elements that are somewhat inconsistently detailed in literature reports on these devices. Systematic study will highlight key fabrication bottlenecks that must be overcome for this switch technology to become more widely adopted. The ability to fabricate these structures represents an entirely new capability for the University of Maryland that will enable additional opportunities for

research into enhanced vertical GaN switches.

## 6.2 Photolithography Mask Design for Vertical GaN MOSFETs

An entirely new photolithography mask set was designed to support fabrication and study of vertical MOSFET epitaxial layer structures and devices. The photomask set was designed using free photomask computer-aided design (CAD) software (KLayout) and is shown in Fig. 6.1. Key features of the mask set include:

- A central crystallographic alignment mark scheme to allow rotational alignment of the mask layers to GaN non-polar m-planes. The details of this process are detailed in a subsequent section.

- A variety of MOSFET architectures with gates along mesa or trench gate sidewalls at angles ranging from 0° to 90° (in 15° increments) off of the m-planes highlighted with the central crystallographic alignment mark. The various trench angles will allow characterization and comparison of devices oriented along the non-polar m-planes, a-planes, and at mixed angles halfway between. Various contact schemes to the p-body layer are also employed for each architecture, including no body contact, a body contact with n-type Ohmic metals (Ti-based), and a body contact with p-type Ohmic metals (Pd, Ni).

- Circular transfer length method (CTLM) measurement structures on the source ($n^+$), body (p), and drift ($n^-$) epilayers for determination of contact and sheet resistivity on each layer.

- Schottky barrier diode (SBD) and p-n junction diodes on each epilayer for extraction of doping density and other diode characteristics through C-V and I-V measurements.

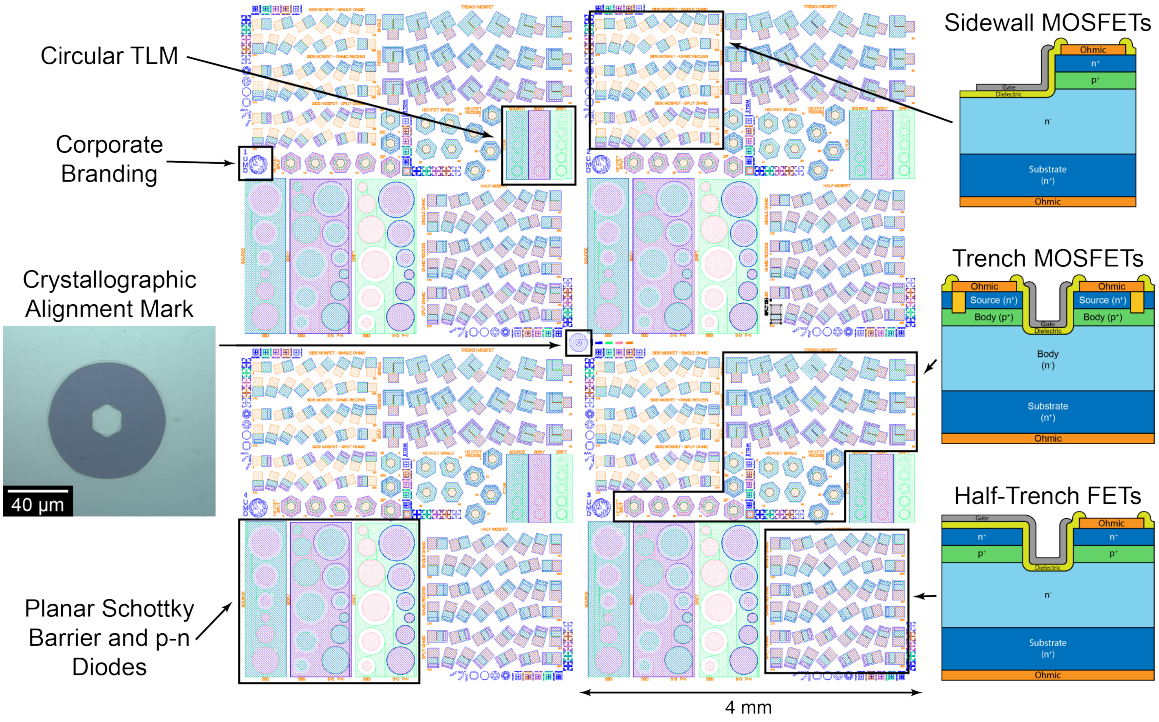


Fig. 6.1. Custom photolithographic mask structures designed for fabrication and characterization of devices and epilayers for vertical trench-gate GaN MOSFETs, with important design features marked in boxes.

## 6.3 Epitaxial Layer Design for Vertical GaN MOSFETs

A four layer structure was designed for MOCVD growth by a commercial vendor to support high voltage vertical GaN MOSFETs as follows:

- Source ($n^+$): $2\times10^{18}$ $cm^{-3}$ Si doped, 500 nm thick
- Body ($p^-$): $>1\times10^{19}$ $cm^{-3}$ Mg doped, 500 nm thick
- Drift ($n^-$): $<1\times10^{16}$ $cm^{-3}$ unintentionally doped, 10 $\mu$m thick

- Bulk GaN Drain/Substrate ($n^+$): $>10^{18}$ $cm^{-3}$ Si doped, $\approx$ 500 $\mu$m thick

This structure creates a vertical npn MOSFET structure. Inclusion of the low-doped drift layer forms a one-sided p-n junction with the p-body layer that becomes reverse biased when standing off high off-state drain bias. Specifications for this drift layer must be designed to balance competing effects between the off- and on-states. In general, having a thick, low-doped drift layer is desirable for high off-state blocking voltages, as the electric field can be spread over the entire drift layer to avoid breakdown. However, these two factors (drift layer thickness and doping density) also affect the resistivity of the drift layer and thus play a major role in the on-resistance of the MOSFET. The effect of drift layer doping density ($N_d$) on blocking voltage ($V_{br}$) can be determined using Eqn. 6.1 [185]:

$$V_{br} = \frac{\epsilon_0 k_{GaN} E_c^2}{2qN_d} \tag{6.1}$$

where $\epsilon_0$ = permittivity of free space, k = relative permittivity of GaN (9.5), $E_c$ = critical electric field for GaN, and q = elementary charge. (Note that the above equation neglects the built-in voltage ($V_{bi}$) from the p-body/n-drift diode; for a power MOSFET $V_{bi}$ is only a few volts and thus negligible compared to the critical field and doping density term.) The minimum drift layer thickness ($W_d$) needed to support the depletion region in reverse bias can then be determined as a function of the desired blocking voltage using Eqn. 6.2 [185]:

$$W_d = \sqrt{\frac{2\epsilon_0 k_{GaN}(V_{bi} - V)}{qN_d}} \tag{6.2}$$

The relationships described by these two equations are shown graphically for a vertical GaN

device in Fig. 6.2, assuming a value of $E_c$ for GaN of 3 MV/cm.

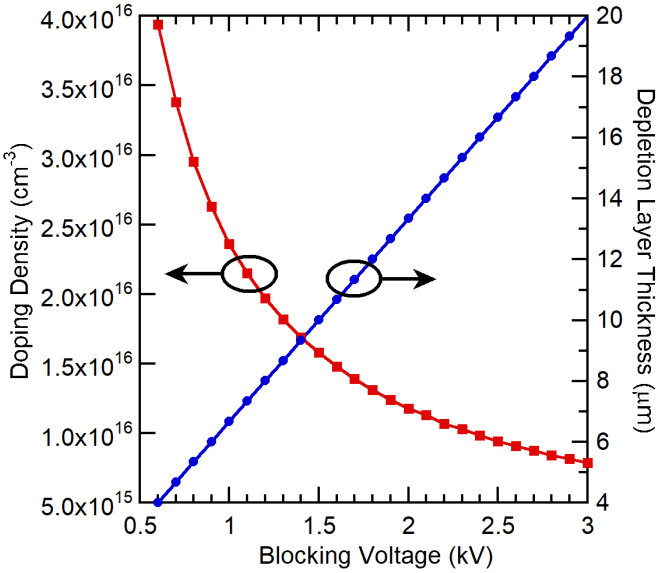


Fig. 6.2. Theoretical plot of drift layer doping density and thickness as a function of blocking voltage for a vertical GaN MOSFET.

Aside from theory, the maximum drift layer thickness and minimum unintentional doping density are also constrained by more practical considerations. Growth time and thermal stresses limit the drift layer thickness to around 10 $\mu$m during MOCVD or HVPE growth, and unintentional impurity incorporation (Si, O, and C) limits the unintentional doping to around $1\times10^{16}$ cm$^{-3}$ [87, 186, 187]. Recent work points to solutions for these issues, with demonstrations of MOCVD doping densities as low as $2\times10^{15}$ cm$^{-3}$ achieved through optimization of growth process conditions, and HVPE doping densities as low as $2\times10^{14}$ cm$^{-3}$ achieved by removal of contamination sources such as quartz reactor parts [85, 187]. As these capabilities are relatively recent developments, they are not necessarily expected to be widely available among commercial vendors at this time and may not be achievable in the commercial wafer commissioned as part of this work. In this case, a drift

layer 10 $\mu$m thick with an unintentional doping densty of $1\times10^{16}$ cm$^{-3}$ or less was specified, with a target $V_{br}$ of 1500 V. The resistance of the specified drift layer (in $\Omega\cdot$cm$^2$) can be estimated using Eqn. 6.3:

$$R_{drift} = \frac{4V_{br}^2}{\mu_n \epsilon_0 k_{GaN} E_c^3} \tag{6.3}$$

where $\mu_n$ = electron mobility, assumed to be around 900 cm$^2$/V·s [188], and the denominator of $R_{drift}$ is the BFOM for power devices. For a 1500 V blocking structure, then, $R_{drift}$ is expected to be 0.44 m$\Omega\cdot$cm$^2$.

A critical note should be made on the value of $E_c$, as mentioned in Chapter 1. A theoretical value of 3.0–3.3 MV/cm is often quoted for GaN; however, the critical field determined from breakdown of actual devices can be aw low as half of this value due to defects in the material. Device design considerations such as field plates or implanted field termination layers can reduce the peak electric field at typical points of failure, allowing for increased breakdown fields [90–93]. As such, the actual blocking voltage and drift resistivity of a commercially grown epistructure may vary significantly.

Additional consideration was given to the n$^+$-source and p-body design. High doping density in both layers is necessary to minimize the electrical resistance and facilitate production of good Ohmic contacts. For the intentionally doped n$^+$ source, Si doping by MOCVD growth is relatively straightforward, as Si is a shallow donor (activation energy of 0.02-0.03 eV) [189]. An Si doping concentration of $2\times10^{18}$ cm$^{-3}$ was specified. The source epilayer thickness was determined by Ohmic contact considerations. Low resistance Ohmic contacts to n-type GaN can be produced by elevated temperature alloying of Ti-based contacts, such as the 850 °C annealing of Ti/Al/Ni/Au used for the AlGaN/GaN HEMTs

produced in Chapters 5 and 8 of this dissertation. In this process, Ti metal reacts with and "spikes" downward into the GaN epilayer. While this behavior produces excellent Ohmic contact, the $n^+$ source must be sufficiently thick to prevent the contacts from consuming the entire layer into the underlying p-body. Spike depths ranging from 25–130 nm have been reported on GaN epilayers and AlGaN/GaN heterostructures, so 500 nm is more than adequately thick for the source layer [190].

Production of high quality p-GaN body layers is more difficult, for the reasons discussed previously in Chapter 1. Mg is a deep acceptor in GaN (activation energy 0.16 eV) [86] Mg doping in MOCVD-grown GaN layers is further complicated by formation of Mg-H complexes with residual H from the growth process that passivates the Mg acceptors. For both reasons, activation annealing must be performed to activate the acceptors and remove the residual hydrogen [87, 191]. Even with this annealing, residual C from the MOCVD growth can remain as a compensation dopant to the Mg, further reducing carrier concentrations [192]. The Mg doping concentration was specified at $1\times10^{19}$ $cm^{-3}$, with the assumption that a $\leq$ 10% activation efficiency would produce a comparable carrier density in both the body and source layers [86, 89]. A 500 nm body layer thickness was selected to provide processing leeway and prevent over-etching through the p-body layer, as Cl-based plasma is required to etch through the $n^+$ source layer to make electrical contact to the p-body. Also, these specifications are sufficient to ensure that neither the source or body layers will become fully depleted under any bias conditions on the body-source or body-drift p-n junctions.

According to the previous specifications, a $n^+/p/n^-$ epilayer stack was produced by MOCVD (growths coordinated by Kyma Technologies) on a commercially available

2” diameter HVPE bulk GaN substrate (Sumitomo Electric). The substrate was selected based on specifications for vertically-threading screw dislocation density less than $10^7$ $cm^{-2}$. Dislocations in the substrate had a random distribution across the substrate area, with large dislocations appearing as visible hexagonal features (Fig. 6.3). MOCVD epistructure growth included a p-GaN activation anneal for the Mg-doped body layer, but the specifics of this anneal were manufacturer proprietary and can only be surmised from publications on the subject [191]. AFM imaging of the upper surface of the MOCVD-grown epistructure indicated a smooth surface (root-mean-square (RMS) roughness 1.5 Å) with the step-flow growth pattern expected for GaN as shown in Fig. 6.4. Wafer bowing was not readily apparent on visual inspection, such that residual thermal stress from MOCVD growth were expected to be low.

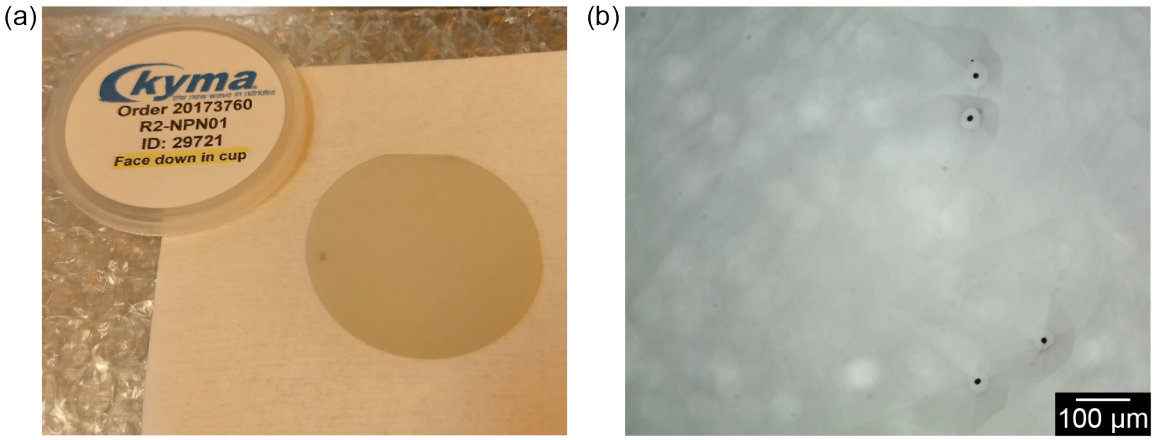


Fig. 6.3. (a) Photo of the 2” GaN substrate/epilayer structure as received from the vendor, and (b) optical micrograph showing hexagonal defect/dislocation pits randomly scattered around the sample area.

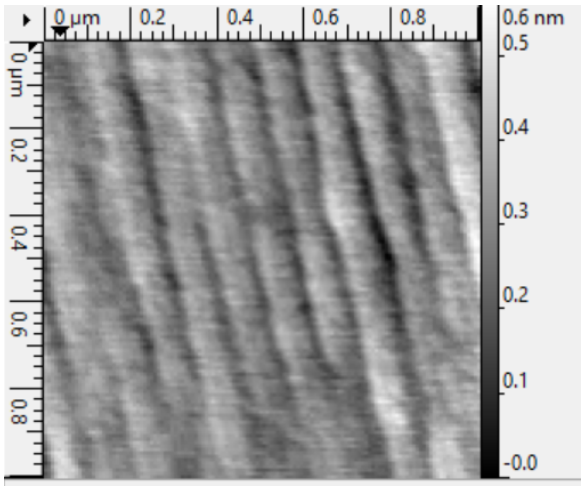


Fig. 6.4. $1\times1$ $\mu$m AFM scan of the MOCVD GaN epilayer surface with the expected step-flow growth.

## 6.4 Contact Fabrication and Epilayer Characterization

Planar CTLM and SBD test structures were fabricated on the source, body, and drift epilayers to allow characterization of contact resistance, sheet resistance, and doping density in each layer. The top source layer was immediately accessible for contact deposition; however, to access the buried p-body and drift layers, $Cl_2$/Ar ICP etching was performed to etch down to each subsequent layer. (Etch process parameters are listed in Appendix B.) Etching was performed to a depth of 700–800 nm for access to the p-body, while a 1300–1400 nm total etch was performed to reach the $n^-$-drift layer. Ti/Al/Ni/Au metal stacks were deposited by e-beam evaporation and liftoff for Ohmic contacts to the n-type layers (source and drift), and as Schottky contacts to the p-body layer. These contacts were alloyed by RTA at 850 °C for 30 sec in flowing $N_2$. Pd/Au metal was deposited by evaporation and liftoff for Ohmic contacts to the p-body layer and Schottky contacts to the source and drift layers. Alloying was again performed by RTA, this time at 450 °C for 1 min in flowing $N_2$.

As expected, good Ohmic contact was made to the $n^+$-source layer with the alloyed Ti/Al/Ni/Au contacts. A low specific contact resistance ($\rho_c$) of $2.2\times10^{-5}$ $\Omega\cdot cm^2$ and sheet resistance ($R_{sh}$) of 2015 $\Omega$/square were extracted from I-V measurements on the CTLM structures, as shown in Fig 6.5. Reverse bias C-V profiling on the source SBDs yielded a majority carrier density of n = $5.2\times10^{17}$ $cm^{-3}$; this is only one-quarter of the expected carrier concentration based on the specified doping density of $N_d = 2\times10^{18}$ $cm^{-3}$. The reduced carrier density is likely due to Mg intermixing from the underlying p-body layer. Mg dopants from MOCVD growth have been previously reported to "ride" along the growth surface during p-layer growth [193, 194]. Subsequent layer growths incorporate this Mg as a contaminant; in this case, the n-doped source layer was likely contaminated with Mg which reduced the measured carrier concentration.

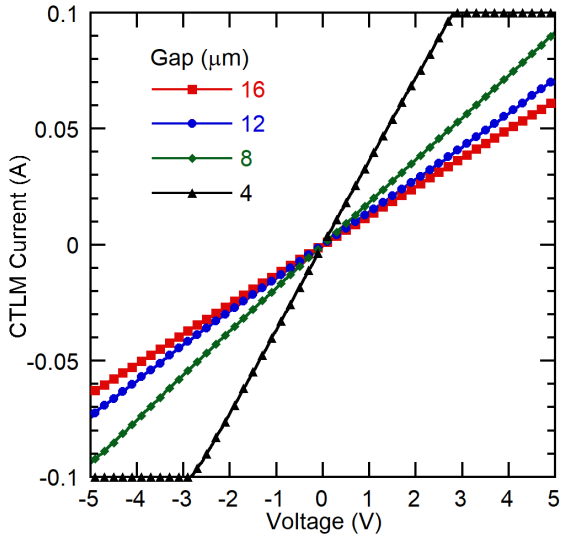


Fig. 6.5. I-V measurements from CTLM contact structures on the $n^+$ source layer, showing high current output and Ohmic (linear) behavior.

The Pd/Au contacts deposited on the p-body did not exhibit Ohmic characteristics, as shown in Fig 6.6. Instead, the I-V behavior observed with the CTLM structures resembled

back-to-back Schottky contacts, which prevented extraction of $\rho_c$ and $R_{sh}$ for the body layer. Reverse-bias C-V on the body SBDs indicated an active carrier concentration on the order of only $p = 0.8\times10^{15}$ cm$^{-3}$; this value may indicate very poor Mg activation or carrier reduction due to n-type defect formation [195], but should be treated with some skepticism due to the poor Ohmic contacts for the SBD ground connection. Non-linear I-V behavior is not atypical for contact structures to p-GaN. Many literature reports have been devoted to development of Ohmic contacts to p-type GaN [87, 196]. In general, high work function metals such as Ni and Pd were utilized, but the successfulness of these contact fabrication processes is as much dependent on p-GaN quality as on the contact scheme used. Additionally, etching through the $n^+$-source and into the p-body layer likely further degraded the carrier concentration and resistivity in the p-body layer due to vacancy formation and other damage effects [73, 74, 195]. These combined effects were all likely responsible for low CTLM currents and extracted doping densities. In any case, process development for low resistivity Ohmic contacts to this specific p-GaN layer must be developed for accurate epilayer characterization and eventual vertical device fabrication.

Ti/Al/Ni/Au contacts to the $n^-$-drift layer were nominally linear, as shown in Fig. 6.7, but due to the lack of carriers in the unintentionally-doped drift layer, both $\rho_c$ and $R_{sh}$ were extremely high. SBD C-V profiling yielded a drift layer carrier concentration of $n = 2.5\times10^{15}$ cm$^{-3}$, which was lower than was expected from the manufacturer's quoted minimum unintentional doping specification of around $1\times10^{15}$ cm$^{-3}$. I-V sweeps on these SBDs were used to probe the breakdown characteristics of the drift layer; both lateral (along the etched drift layer surface) and vertical (from the drift layer surface to the substrate backside) diode arrangements could withstand voltages up to the parameter analyzer's -200

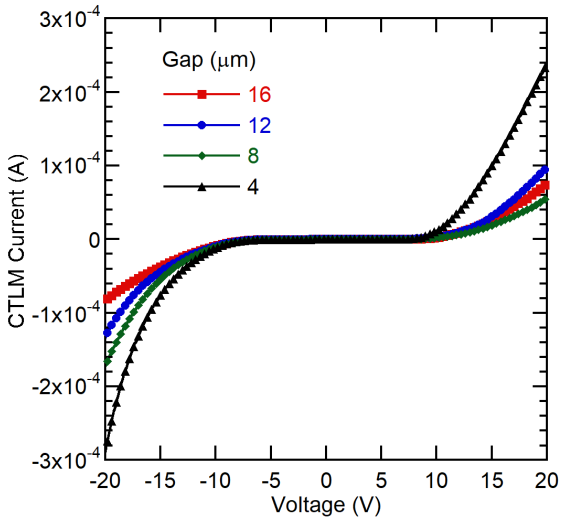


Fig. 6.6. I-V measurements from CTLM contact structures on the etched p-body layer. (Note the different axis scaling compared to Fig. 6.5.)

V limit without breakdown. This indicates that the low-doped drift layer has promise for blocking high voltages, but additional testing is needed with a higher voltage source to determine the ultimate breakdown voltage.

## 6.5 Process Development and Challenges for Vertical GaN MOSFETs

### 6.5.1 Crystallographic Alignment Mark Design and Processing

A simple method is required to align the mask set designed previously to the non-polar crystallographic planes of GaN. While the flats in the bulk GaN substrate can be used for alignment, research-scale processing will take place on smaller samples cut from a bulk wafer; in this work, the 2" wafer was diced as needed into $\sim$1 cm$^2$ coupons. Any misalignment in these cuts relative to the wafer flats would translate into further error when used for mask alignment. Instead, this dissertation reports the development of a

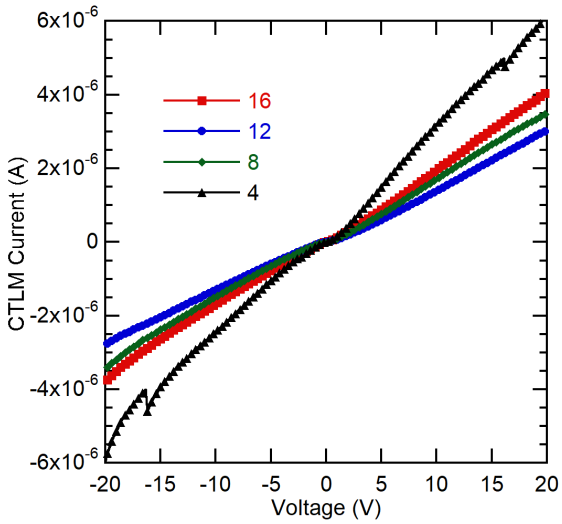


Fig. 6.7. I-V measurements from CTLM contact structures on the etched $n^-$-drift layer. These Ti/Al/Ni/Au contacts were processed at the same time as the source Ohmic contacts, indicating that the low current/high contact and sheet resistances were due to the low carrier density in the drift layer.

crystallographic alignment mark that simply indicates the orientation of the non-polar GaN m-planes by taking advantage of crystallographic wet etching with TMAH [79]. Before exposing the sample to TMAH, which selectively etches defective GaN, a 500 nm $SiO_2$ protective hardmask was deposited by PECVD at 300 °C on the sample surface. Circular crystallographic alignment marks were created by etching through the $SiO_2$ and into the GaN (500 nm deep) in the center of each coupon using a positive photoresist mask (Shipley S1800 series) for the respective F- and Cl-plasma processes detailed in Appendix B. The coupons were then soaked in a bath of 25% TMAH in water at 80–90 °C for up to 4 hours. Wet etching selectively etched the non-m-planes of GaN and formed large facets oriented parallel to the m-planes, as shown in Fig. 6.8. These m-plane facets were visible by optical microscopy, and were used as alignment marks the mesa/trench mask level in the next step.

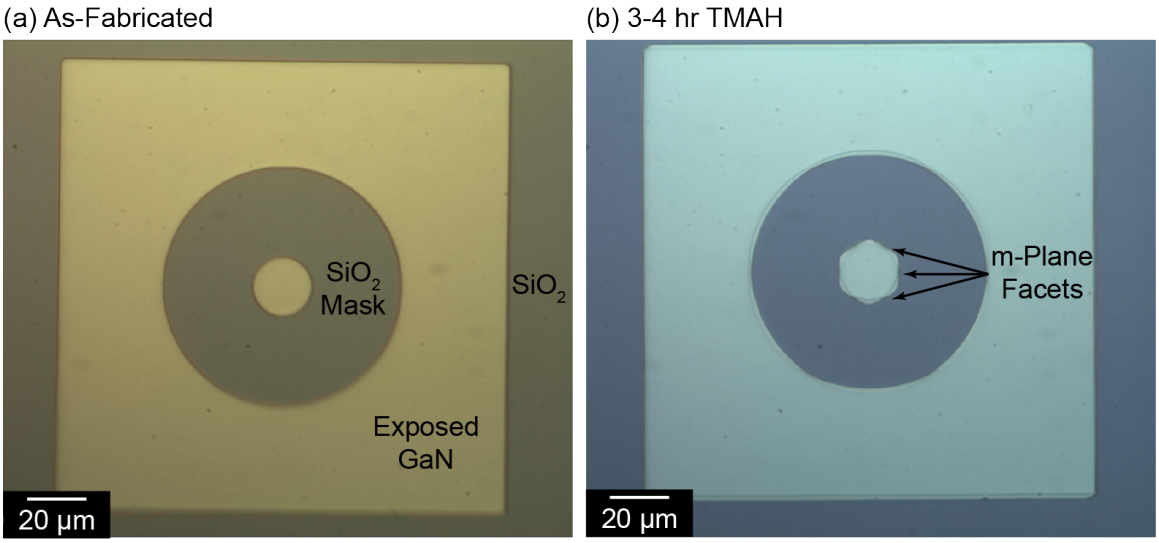


Fig. 6.8. Optical micrographs of the ring-shaped crystallographic alignment mark (a) as-fabricated and (b) after soaking in TMAH. m-plane facets are easily visible after TMAH exposure and can be used to align the remainder of the mask set in a contact lithography tool.

### 6.5.2 Trench Gate Etch Process Development

Several Cl-based plasma etches were considered for use in this study, including the $Cl_2$/Ar ICP/RIE etch used elsewhere in this dissertation, a $BCl_3/Cl_2$ ICP/RIE etch [78], and a low power $BCl_3/Cl_2$ RIE-only etch [67]. Etch rates were measured on test GaN samples using a Tencor stylus profilometer, with the average etch rates over three separate measurements detailed in Table 6.1. Since the mesa and trench etching would be performed as a single step through both the $n^+$-source and p-body (target depth 1200–1400 nm), the $Cl_2$/Ar process was selected for further use as it was the only process to yield a suitably fast etch rate. Trench etch profiles with both $SiO_2$ (500 nm) and $SiO_2$/Ni (500/100 nm) etch masks for the $Cl_2$/Ar GaN etching process were explored. The $SiO_2$ hardmask was patterned using photoresist as a mask for $SiO_2$ plasma etching prior to GaN trench etching. For the

$SiO_2$/Ni hardmask combination, Ni was deposited by e-beam evaporation and lift-off with a bi-layer lift-off resist/photoresist stack, which was then used as an etch mask for both the $SiO_2$ and GaN plasma etches.

Table 6.1. GaN etch rates for Cl-based plasma etches explored in this dissertation. (Additional process details can be found in Appendix B.)

| Etch Chemistry | Avg. Etch Rate (nm/min) |
|---|---|
| $Cl_2$/Ar ICP/RIE | 160 |
| $BCl_3/Cl_2$ ICP/RIE | 70 |
| $BCl_3/Cl_2$ RIE-only | 11 |

Cross-sections of trenches produced with both mask schemes are shown in Fig. 6.9. Smooth sidewalls were obtained for etching using both masks. The sidewall angle for trenches masked with only $SiO_2$ was 19° off-vertical, while an 9° angle was obtained for the $SiO_2$/Ni-masked trenches. The etch selectivity between the GaN and $SiO_2$ mask for the $Cl_2$/Ar plasma etch was measured at approximately 6:1 (i.e. GaN etches 6x faster than $SiO_2$), while the GaN-to-Ni selectivity was at least 13:1 based on the Ni still being visible after 1300 nm GaN etching. The shallower sidewalls for the $SiO_2$-masked trenches likely arose from taper and erosion in the photoresist mask that carried over to the $SiO_2$ mask during the $SiO_2$ plasma etch. Small microtrenching features (small divots/grooves) were apparent at the base of the $SiO_2$-masked trench walls. Microtrenching arises from plasma species reflecting off the non-vertical sidewalls and attacking the bottom wall edge more aggressively [197, 198]. A much steeper sidewall was obtained using the Ni hardmask, which was at least 10 times thinner than the photoresist mask and much more resilient to both the $SiO_2$ and GaN etches (as indicated by the etch selectivity). Microtrenching was not

apparent for the $SiO_2$/Ni masked trenches due to the steeper sidewalls. The $SiO_2$/Ni mask combination was thus selected for further processing.

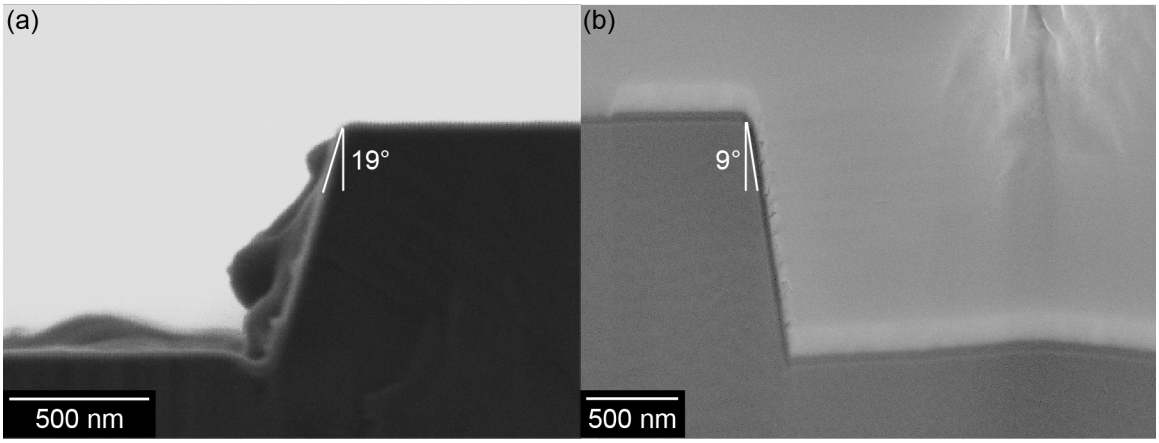


Fig. 6.9. GaN trenches etched by $Cl_2$/Ar plasma with (a) $SiO_2$ and (b) $SiO_2$/Ni hardmasks. Note the different scale markers due to different trench etching depths. The rounded features seen on the sidewall in (a) due to organic contamination behind the cross-sectioned surface.

## 6.6 Trench Faceting with TMAH Wet Etching

A heated TMAH soak (25% in water, 80–90 °C bath temperature, up to 30 min) was employed to selectively etch away plasma damaged GaN and form the trench sidewalls into vertical m-plane oriented facets. Plan-view SEM images comparing the as-etched and TMAH-faceted trenches are shown in Fig. 6.10. The as-etched trenches were uniform in appearance, without any regard to the crystallographic orientation of the trench. Once exposed to the TMAH treatment, clear differences between the m- (Fig. 6.10a) and a-plane (Fig. 6.10b) oriented trenches emerged. The m-plane oriented trenches had smooth, single-facet sidewalls, while the a-plane sidewalls were etched into numerous m-plane facets, creating a zig-zag appearance. Additionally, dislocation pits were observed along the trench

bottoms after TMAH etching. These presence of these pits and dislocations is expected; assuming a maximum dislocation density of $10^7$ cm$^{-2}$, these 100 $\times$ 3.5 $\mu$m trenches could contain up to 35 dislocations each. Dislocations in the trench are undesirable, as they will contribute to leakage and premature failure, but are unavoidable given the random dislocation distribution in this substrate.

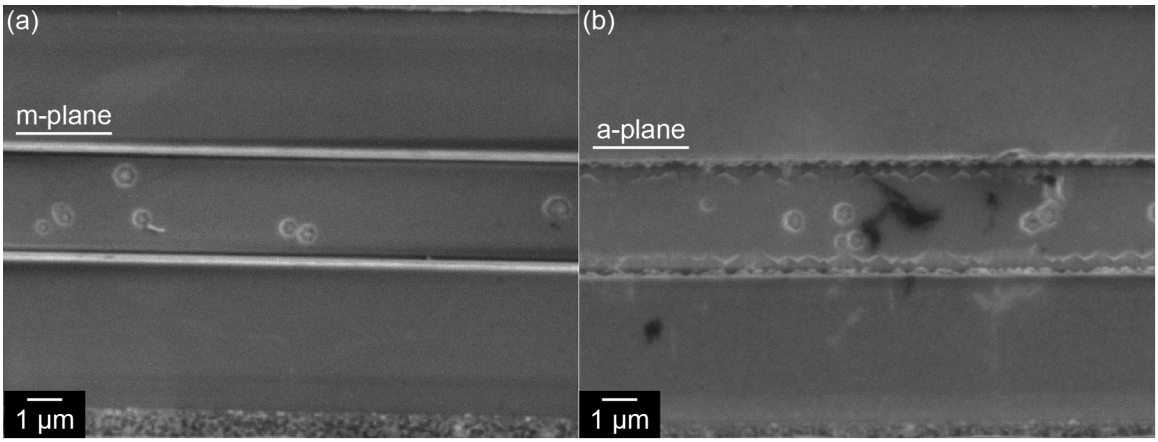


Fig. 6.10. Effects of TMAH faceting on trenches oriented parallel to (a) m-planes and (b) a-planes of GaN. m-plane oriented trenches show smooth sidewalls after TMAH exposure, while the a-plane oriented trenches exhibit many small m-plane facets instead of smooth sidewalls and bottom. Hexagonal dislocation pits are highlighted on the bottom surface of the trenches.

In keeping with the optimum pre-ALD surface treatments identified in for GaN in Chapter 3, a 10 min piranha clean (3:1 $H_2SO_4$:$H_2O_2$, 80 °C) was performed on as-etched and TMAH-faceted trench structures. Then, Ni/Au metal was deposited by e-beam evaporation and liftoff to observe metal coverage along the trench sidewalls, as would be required in a trench-gate MOSFET. Cross-sectional SEM images of the as-etched and TMAH-faceted trenches after Ni/Au deposition are shown in Fig. 6.11. These images reveal a key complication for vertical MOSFET fabrication: metallization of steep sidewalls along deep and narrow trenches. On the as-etched trenches (Fig. 6.11a), the metallization is

clearly thinner along the sidewalls; black features in the images may indicate the presence of voiding or other nonuniformities in the metal deposited on these sidewalls. This difficulty arose not only from the trench geometries, but also from the e-beam evaporator deposition geometry. The evaporators used in this study (Angstrom NexDep) rely on a rotating turret geometry, as shown in Fig. 6.12a. Under these conditions, evaporation occurs in a conical pattern, and the turret rotates the sample so that deposition is nominally perpendicular to the sample surface. This means that the deposition thickness listed previously was the deposition thickness along the bottom and top of the trench, while the sidewall metallization was thinner.

An attempt to improve the gate metallization along the trench sidewalls was employed with the TMAH-faceted sample. In this case, a "flip-stage" was utilized in the evaporator, where the sample was fixed to a plate directly over the evaporation crucible, as shown in Fig. 6.12b. This plate was manually rotated along one axis, thereby changing the direction of the sample surface relative to the incoming evaporated metal. More metal (up to 300 nm total) was also deposited. Inspection of the TMAH-faceted trench cross-sections (Fig. 6.11b and c) indicated that neither modification improved the sidewall metallization; discontinuities and non-uniformities can easily be observed along the trench sidewalls due to the m-plane facets produced by the TMAH treatment. At present, only the rotating turret and flip-stage deposition geometries are available in the University of Maryland FabLab, and simply depositing sufficient metal quantities to completely fill the trenches using these deposition methods is prohibitively expensive and time-consuming. Alternate metallization techniques are thus required to allow gating of a trench MOSFET, such as electroplating/electroless deposition of metals (e.g. Ni) or ALD of conductive metal nitrides like the

TiN used previously in this program for AlGaN/GaN HEMTs [4]. Additionally, the TMAH aggressively attacked the microtrenching at the base of the sidewalls, leading to abnormal sidewall shapes that further hindered metallization of the trench sidewalls and bottom. This type of defect is significant and has not been observed in other reports of TMAH-faceted GaN trenches [78]. Mitigation of this defect must be a top priority, as the electric field in a functioning MOSFET is highest at the bottom corners of the gate trench. These irregular features at the bottom of the trench sidewall will likely contribute to premature device failure. Trench etching and faceting may thus require the use of $SiO_2$-only hardmasks, since the 19° sidewall angle would move the microtrenched regions closer to the trench centers and away from what would eventually become the vertical trench sidewalls.

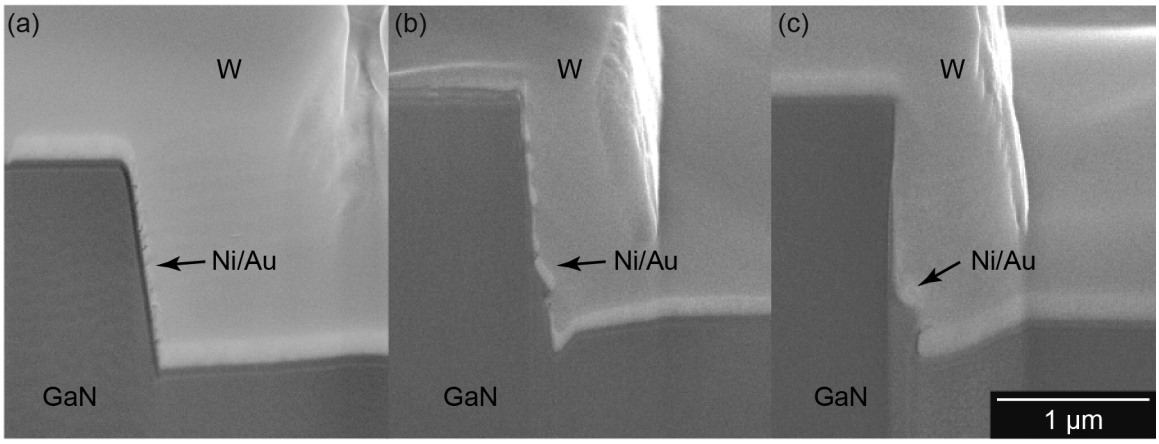


Fig. 6.11. Cross-sections of (a) as-etched, (b) TMAH-faceted m-plane, and (c) TMAH-faceted a-plane trench sidewalls, showing issues with gate metal continuity along the highly vertical trench walls.

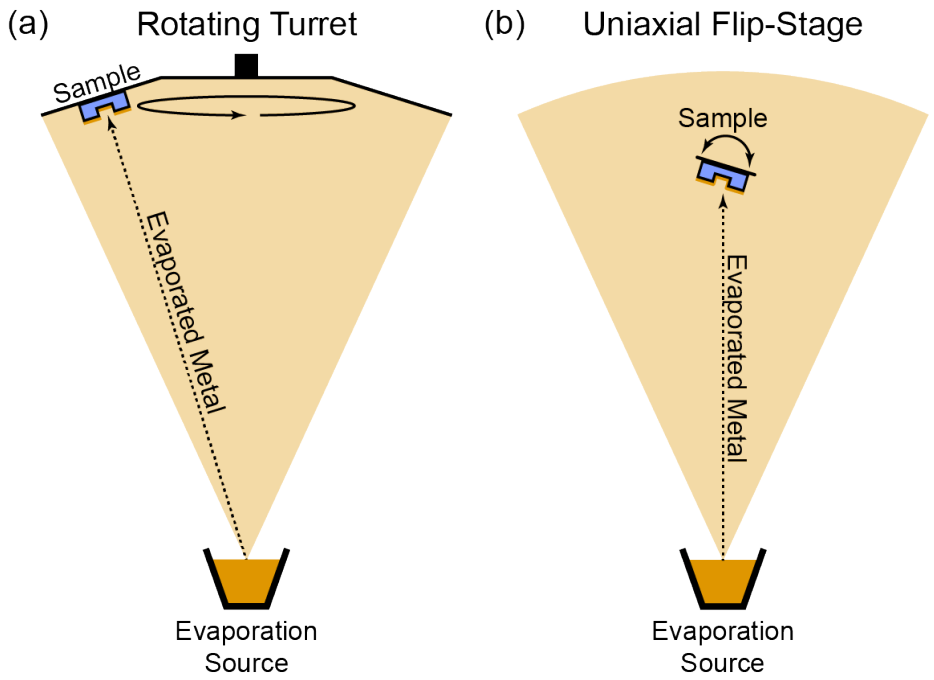


Fig. 6.12. Schematics of the two deposition arrangements possible in the UMD e-beam evaporators for gate deposition. The standard arrangement using a rotating turret is shown in (a), and the flip-stage arrangement for uniaxial rotation is shown in (b).

## 6.7 Chapter Summary

Fabrication of vertical trench-gate GaN MOSFETs is a difficult task in comparison to the simplicity of fabrication for AlGaN/GaN HEMTs and other lateral WBG and UWBG switches. This complexity is, in large part, the reason why vertical MOSFET performance has not approached theoretical limits for on-resistance and breakdown voltage. This chapter details a number of important and often underreported considerations relevant to the fabrication of these devices, including photlithographic mask design; design and characterization of epilayer thicknesses, doping densities, and contacts; and trench crystallographic alignment, etching and metallization. Several key challenges still remain that must be resolved to allow future fabrication of high performance vertical trench-gate MOSFETs:

- Low-resistivity Ohmic contacts must be developed to the buried and etched p-body layer to allow gate biasing and channel formation in a vertical MOSFET. Producing Ohmic contacts to p-layers is difficult and varies widely with the p-doping technique, dopant concentration, contact metals, annealing techniques, etc. Additionally, the p-body layer can only be accessed by plasma etching, which raises the possibility of increased sheet resistance and even p-type to n-type conversion. Addressing these issues will likely require more than just experimentation with annealing of different high work function metals. TMAH treatment to remove etch-damaged GaN, Mg implantation underneath the body contacts to create $p_+$ regions, and annealing or MOCVD p-layer regrowth after etching may be required as the subject of future work.

- Microtrenching at the base of the trench sidewalls must be mitigated to prevent device failure where the electric field is highest in a vertical MOSFET. Use of mask materials that allow for shallower sidewall angles, followed by TMAH treatment, or use of lower power plasma etches may provide the solution to this issue.

- Gate metallization thickness and quality must be improved along the trench sidewalls where the gate bias is most important. As mentioned previously, the available evaporator deposition techniques are not ideal for the trench geometries employed in this work, especially in the case of vertical TMAH-faceted sidewalls. Additional techniques must be accessed elsewhere or developed in-house, potentially including Ni electrodeposition techniques or ALD of conductive metal nitrides like TiN, to form a continuous conductive gate.

Consistent solutions to these challenges, combined with the other developments

reported in this chapter, will allow fabrication of vertical GaN switches at the University of Maryland and in the broader power electronics community. Successful device fabrication based on this work is expected to yield future contributions to understanding of device fabrication and reliability. For example, functional vertical switches can be subjected to reliability studies to determine the primary failure mechanisms in these systems. The effect of dislocations on device performance and failure can also be studied.

# Chapter 7: Hydrogen-Terminated Diamond Switches with $Al_2O_3$ Surface Transfer Doping

## 7.1 Introduction to Diamond Power Switches

Diamond-based electronics are an emerging UWBG switch technology projected to enable novel ultra-high power, high frequency applications. Deep dopant levels in diamond require the use of 2D conducting channels, such as those generated by hydrogen surface termination of diamond, to achieve operational power switches [109, 110]. Exposing diamond to a hydrogen plasma at elevated temperatures (>700 °C) produces a surface C-H dipole layer that significantly reduces the ionization energy of valence band electrons to as low as 0.05 eV [111]. Contact between this dipole layer and high electron affinity surface transfer dopants leads to electron transfer, leaving behind a near-surface 2DHG with carrier densities up to $10^{14}$ $cm^{-2}$ [112–114]. A number of promising surface transfer dopants and passivation schemes have been reported for H:diamond FETs [115–121], but their long-term stability and reliability requires further assessment. In this chapter, the fabrication, characterization, and stability of H:terminated diamond switches with $Al_2O_3$ as the surface transfer dopant are reported. Innovative processing developed to allow contact photolithography on these small HPHT samples is also reported.

## 7.2 Hydrogen-Terminated Diamond Device Fabrication

### 7.2.1 Preparation of Smooth Hydrogen-Terminated Diamond Surfaces

Undoped (100) type IIa single crystal HPHT substrates (New Diamond Technology Co.) were selected for use in this work due low dislocation density and impurity concentrations [138]. Substrates ranged in size from 3×3×0.5 mm to 5×5×0.5 mm (L×W×H). In order to minimize carrier scattering within the 2DHG due to surface roughness, substrates were polished and etched with a low power plasma [199] by research collaboartors at Euclid TechLabs to less than 3 Å RMS roughness, as indicated by AFM imaging shown in Fig. 7.1.

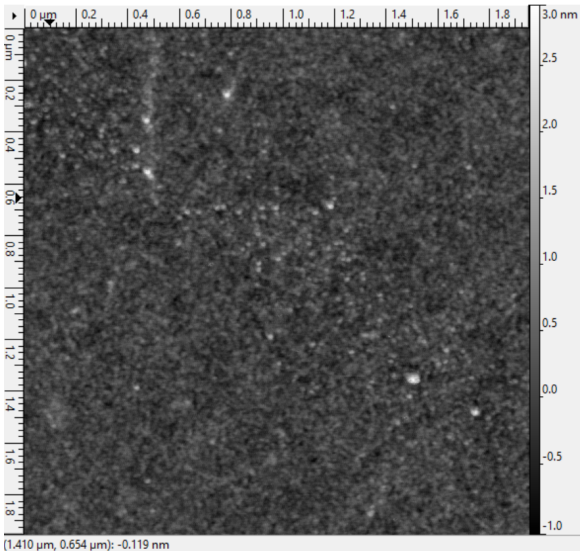


Fig. 7.1. AFM image of a typical polished and etched diamond substrate with <3 Åsurface roughness.

Hydrogen termination of the surface was achieved by exposing the polished surface to a hydrogen plasma at temperatures above 700 °C. The resulting surface exhibited p-type conductivity when contacted by an adsorbed or intentionally deposited surface transfer

dopant. This was observed with I-V measurements between two Au contact pads on the hydrogenated sample surface, as shown in Fig. 7.2. Open atmosphere testing allowed adsorption of atmospheric humidity and contaminants that act as simple transfer dopants and provide some current output. Intentional exposure to $NO_2$ (created by reacting Cu metal with $HNO_3$ [200]) improved the current output by nearly an order of magnitude. However, this effect was transient, as the $NO_2$ desorbs from the surface or reacts with atmospheric water to reform $HNO_3$; as a result, the current output decreased by 23% just 30 minutes after initial $NO_2$ exposure. Intentional oxidation of the surface with an $O_2$ plasma effectively destroyed the hydrogen termination and reduces the current output accordingly. $H_2O$ and $NO_2$ were thus inherently unstable transfer dopants. Passivation with high electron affinity dielectrics is of tremendous interest for stable and reliable hydrogen-terminated FETs.

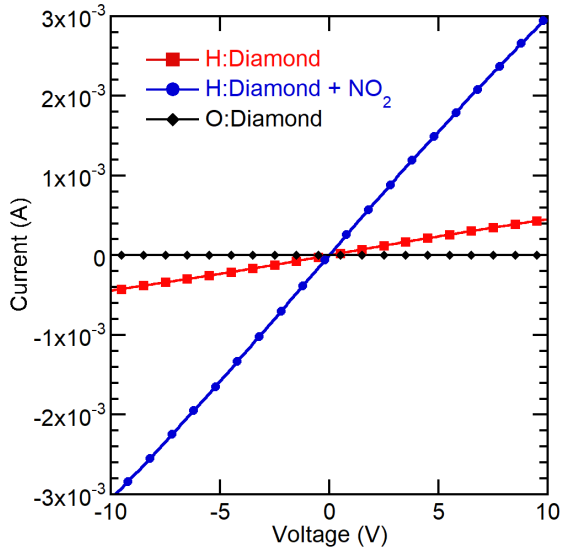


Fig. 7.2. Two-point I-V measurements between Au contacts $\approx$ 25 $\mu$m apart, showing conduction along the H-terminated surface with unintentional atmospheric adsorbates and intentional $NO_2$ adsorbates. Oxygen plasma exposure destroyed the hydrogen termination and thus the surface conductivity.

### 7.2.2 H:Diamond Switch Fabrication

$Al_2O_3$-passivated FETs, shown schematically in Fig. 7.4, were fabricated on these ultra-smooth hydrogen-terminated HPHT substrates. Substrates were received for processing already hydrogen terminated and stored in ethanol to avoid contamination of the diamond surface. Processing was performed using standard contact photolithography techniques. Due to the small sample geometries employed in this work, spincoating of photoresist resulted in formation of thick edge beads at the sample corners that significantly limited the usable area on these substrates and otherwise degraded feature resolution. To combat this effect, an innovative sample mounting geometry was developed. This mounting scheme, shown in Fig. 7.3, involved positioning the diamond in the center of a Si wafer, followed by securing additional straight-edged Si pieces up against each side of the diamond substrate. This effectively creates a much larger surface area for the photoresist to spread over, thereby mitigating the edge beading.

A typical device process sequence was followed for these H:diamond FETs. First, blanket deposition of 100–150 nm layer of Au by e-beam evaporation was performed on the entire sample to protect the surface termination during subsequent processing steps. Photoresist mesas were patterned on the blanket Au layer, followed by wet etching in $KI/I_2$ (Au Etchant TFA, Transene Co.) to form discreet Au device mesas. A brief $O_2$ plasma etch was used to destroy the hydrogen termination and achieve device isolation. Discrete Ohmic contacts were then formed from the Au mesas by photolithography and $KI/I_2$ wet etchback. A blanket 25 nm $Al_2O_3$ film was used as the surface transfer dopant and gate dielectric, deposited by ALD at 175 °C with trimethylaluminum and water precursors. Windows were

etched through the $Al_2O_3$ over the Ohmic contacts. Finally, 100 nm Al was deposited by e-beam evaporation and liftoff to form the gates.

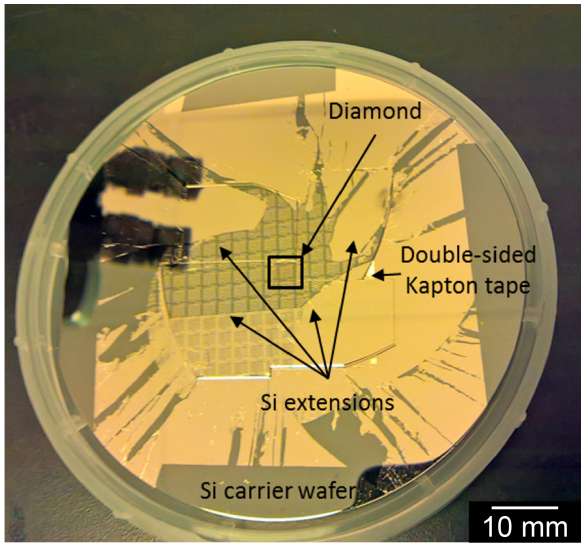


Fig. 7.3. Mounting scheme for small diamond substrates. Si wafer pieces were cut and mounted next to the diamond sample sides to allow photoresist to flow off the diamond edges and corners, thereby mitigating edge bead issues.

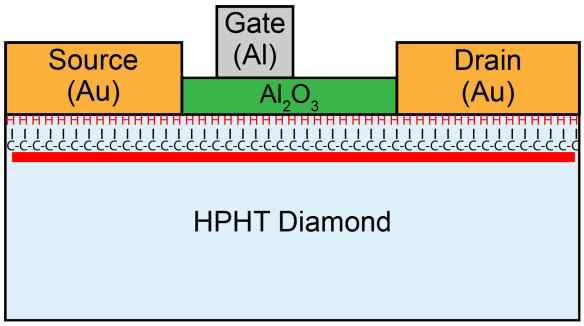


Fig. 7.4. Hydrogen-terminated diamond FET schematic with $Al_2O_3$ as both the surface transfer dopant and gate dielectric.

## 7.3 Operating Characteristics of $Al_2O_3$/H:Diamond MOSFETs

Transfer and output characteristics for these $Al_2O_3$/H:diamond MOSFETs with 3 $\mu$m gate length are shown in Fig. 7.5 below, with useful extracted device parameters in Table 7.1. The transfer characteristics shown were representative of these H:diamond FETs, while the output characteristics were among the better examples of devices fabricated for this work. As expected from the presence of a 2DHG, these $Al_2O_3$/H:diamond switches were normally-on, with a threshold voltage ($V_t$) of around 4 V. A channel mobility of approximately 50 $cm^2/V{\cdot}sec$ was extracted from the maximum transconductance value, assuming an $Al_2O_3$ dielectric constant of 9. This value is toward the lower end of the mobility ranges expected for an H:diamond surface with dielectric passivation (i.e. no $NO_2$ passivation)[115]. Output current was comparable to other reports of $Al_2O_3$/diamond FETs without $NO_2$ passivation under the dielectric layer [123]. However, it should be noted that current output is significantly lower than that of state-of-the-art AlGaN/GaN HEMTs including those reported elsewhere in this dissertation. Even though comparable sheet carrier densities can be developed in H:diamond 2DHG layers, the channel mobility extracted earlier is significantly lower than in AlGaN/GaN 2DEG layers, resulting in higher resistivity channels.

## 7.4 Stability and Reliability Considerations for H:Diamond MOSFETs

Operational stability is a concern for hydrogen-terminated diamond devices. Several studies have reported degraded conductivity or FET output from unpassivated H:diamond

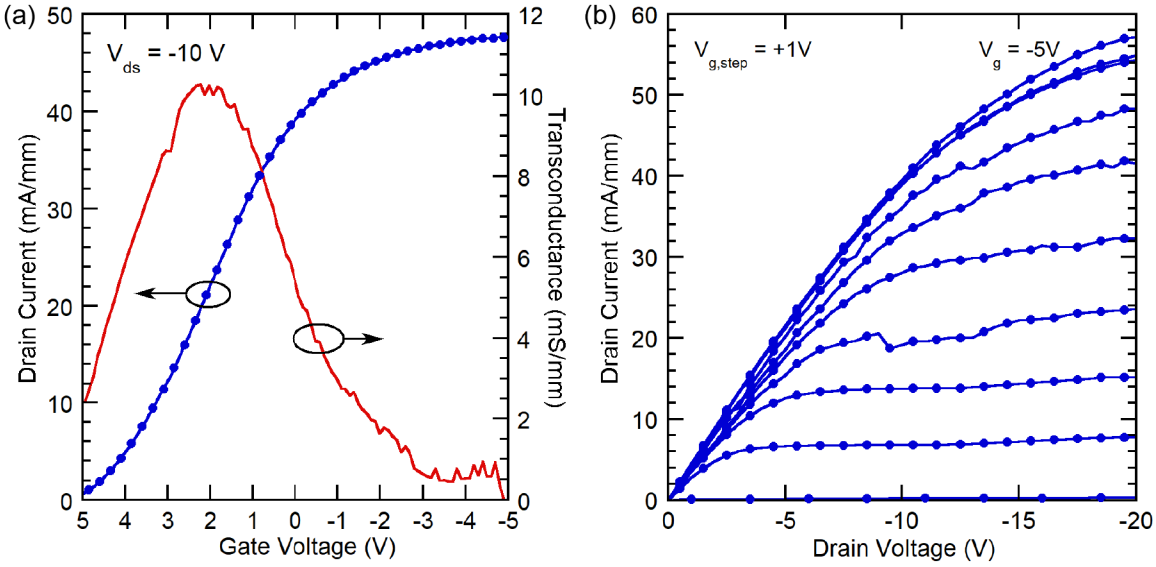


Fig. 7.5. (a) Transfer and (b) output characteristics of an $Al_2O_3$/H:diamond FET (source-gate spacing $L_{gs}$ = 3 $\mu$m, gate length $L_g$ = 3 $\mu$m, gate-drain spacing $L_{gs}$ = 10 $\mu$m).

Table 7.1. $Al_2O_3$/H:diamond FET operating characteristics for the device shown in Fig. 7.5.

| Parameter | Value |
|---|---|
| $V_t$ (V) | 4.04 |
| $g_{m,max}$ (mS/mm) | 10.3 |
| $I_{ds,max}$ ($V_{gs}$ = -5 V, mA/mm) | 57.2 |
| $R_{on}$ (Ohm·mm) | 224 |
| $I_{g,max}$ (mA/mm) | $6.43\times10^{-7}$ |
| $I_{off,max}$ ($V_{gs}$ = -5 V, $V_{ds}$ = -20 V) | 0.229 |

surfaces during testing in ambient atmosphere, as opposed to vacuum or dry $N_2$ atmosphere [24, 201]. While the use of dielectrics as surface transfer dopants should stabilize the 2DHG and the resulting device performance, thin or low-quality dielectrics may be insufficient to shield the hydrogenated surface from ambient atmosphere effects. Passivated devices have shown some relatively minor instabilities (<10% over a period of 15 hours) [113]. Thicker and denser dielectrics have been shown to provide more complete surface protection and stability of H:diamond surfaces [123, 202].

In order to assess the stability of the $Al_2O_3$/H:diamond MOSFETs produced in this work, multiple device measurements were taken on a single device over the course of one week. These measurements are shown in Fig. 7.6. Slight degradation in output characteristics were observed; on-resistance increased by 54 Ω·mm (27%) between the initial and final measurements, while output current decreased by 4 mA/mm (11%). Dielectric degradation was ruled out, as changes in $V_t$, $g_{m,max}$, and gate leakage current through were negligible during all measurements ($<10^{-7}$ mA/mm). Therefore, inconsistent electrical contact to the Au Ohmic pads over repeated measurements was the most likely cause. Due to the very weak adhesion of the Au to the ultra-smooth H:diamond surfaces used in this work, repeated measurements using tungsten probes resulted in severe scratching of the Au contacts. This led to reduction in contact area and provided for inconsistent contact between the probes and Au pads that resulted in the reductions observed. Implementation of contacts with increased adhesion and mechanical integrity will allow for improved measurement consistency. The preferred contact scheme for mechanical reliability would be an alloyed structure such as Ti/Au [123]; however, alloyed contacts would likely need to be fabricated prior to hydrogen termination and disallows the use of Au as a protective layer for the H:diamond surface before surface passivation with ALD. Adjacent contact pads with Ti or another adhesion layer that overlap the Au Ohmics are also be an option, but would require production of a new photolithography mask.

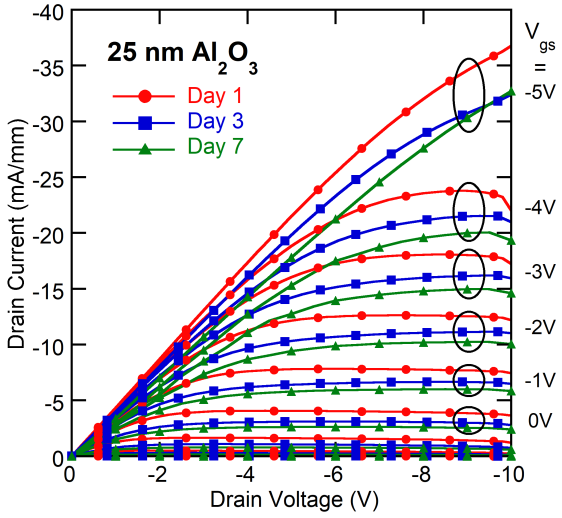


Fig. 7.6. Repeated $I_d$-$V_d$ measurements on an $Al_2O_3$/H:diamond FET over the course of one week. (Device $L_{sg}$ = 3 $\mu$m, $L_g$ = 3 $\mu$m, and $L_{gd}$ = 2.5 $\mu$m.) Relatively minor degradation in output current and on-resistance were observed, which has been linked to contact damage during repeated probing.

## 7.5 Chapter Summary

UWBG switches based on H:diamond conducting channels have been fabricated on smooth HPHT diamond substrates. Surfaces with <3 Åroughness were obtained prior to hydrogen termination. Hydrogen termination was then achieved by exposing the substrates to a pure hydrogen plasma at 700 °C. FETs fabricated on the hydrogen-terminated surface utilized a blanket $Al_2O_3$ dielectric as the surface transfer dopant and exhibited normally-on behavior and well-behaved transistor characteristics, with $V_t$ of approximately 4 V and $I_{ds,max}$ of 57.2 mA/mm, and an estimated maximum channel mobility of 50 $cm^2/V{\cdot}sec$. Device stability was assessed through repeated measurements in laboratory air over the course of one week. Negligible changes in $V_t$ or $g_{m,max}$ were observed, but a slight degradation in output current was observed that is due to probe damage to the weakly adhered Au Ohmic

contacts. Reliability of these devices can thus be easily improved by changing to a more robust contact scheme, such as alloyed contacts or overlay pads with an adhesion layer.

# PART IV
# MATERIALS AND PROCESSES FOR ELECTRICALLY AND THERMALLY STABLE POWER SWITCHES

# Chapter 8: TiN Schottky Gates for Electrically and Thermally Stable AlGaN/GaN HEMTs

## 8.1 Introduction

Electrically and thermally stable device structures are essential for reaching the maximum potential of WBG and UWBG switches. Ni/Au-based Schottky gate metallizations have been commonly employed in these both GaN and $Ga_2O_3$ switches, but at least in AlGaN/GaN HEMTs, their reliability is limited by gate degradation from Ni migration into nearby metal and semiconductor layers when subjected to electrical and thermal stresses [56–59, 94]. As such, development of alternative gate schemes resistant to these degradation mechanisms is highly desirable for fabrication of reliable HEMTs and other power switches. Conductive transition metal nitrides, such as TiN, are particularly promising, due to near-metallic conductivity, suitable Schottky barrier heights to AlGaN and GaN, and high temperature stability to at least 750 °C [140–143]. TiN can also be deposited by versatile methods such as ALD, reactive sputtering, and molecular beam epitaxy (MBE) that can be easily integrated into conventional HEMT process flows [142, 203, 204]. Despite this promise, limited work has been done to assess the effects of a TiN gate on HEMT reliability under extended electrical or thermal stress, and previous studies have exclusively focused on sputtered TiN rather than ALD TiN [142, 205–207]. In this chapter, the superior reliability of ALD TiN gates for AlGaN/GaN HEMTs is demonstrated in comparison to conventional Ni/Au gates through reverse bias electrical stressing and elevated temperature annealing. TiN gates may also be useful for highly stable gates for other n-type WBG/UWBG semiconductor devices such as $Ga_2O_3$.

## 8.2 TiN and Reference HEMT Device Fabrication

Ni/Au- and TiN-gated HEMTs were fabricated from AlGaN/GaN HEMT structures grown by MOCVD on a SiC substrate, as shown in Fig. 8.1.

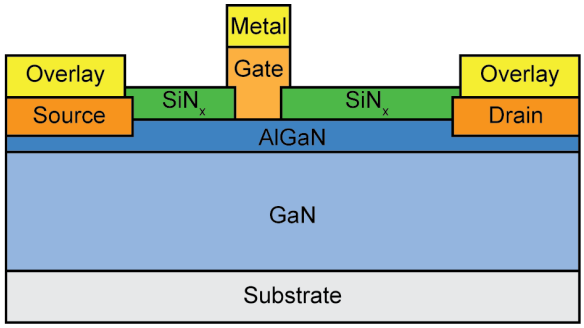


Fig. 8.1. Device schematic of the HEMTs fabricated in this work (gate/metal stack consisted of either Ni/Au or TiN/Ti/Au).

All devices had a gate-source spacing of 2 $\mu$m, gate length of 3 $\mu$m, gate-drain spacing of 10 $\mu$m, and gate width of 75 $\mu$m. The HEMT structure consisted of an AlN nucleation layer, Fe-doped GaN buffer layer, AlN interlayer, and an undoped $Al_{0.22}Ga_{0.78}N$ barrier layer, with 2DEG carrier density and mobility of $9.4\times10^{12}$ $cm^{-2}$ and 2070 $cm^2/(V\cdot sec)$ respectively, as indicated by Hall effect measurements.[208] Device were fabricated using a standard HEMT processing sequence. Mesa isolation was performed using $Cl_2$/Ar-based ICP etching. Ohmic metallization was performed by lift-off of e-beam evaporated Ti/Al/Ni/Au metal, followed by RTA at 850 °C for 30 sec in flowing $N_2$. Overlay metallization was deposited by lift-off of e-beam evaporated Ti/Au. The devices were subsequently passivated with PECVD $SiN_x$, and contact windows were etched using $SF_6$-based RIE conducted with calibration witness $SiN_x$ films to minimize plasma damage to the underlying AlGaN [152]. Ni/Au gates were fabricated on the reference sample by e-beam evaporation and lift-off.

TiN gates were fabricated by blanket ALD using tetrakis(dimethylamido)-titanium(IV) and $N_2/H_2$ plasma at 350 °C for 1000 cycles (approximately 5.5 hour growth time), resulting in stable ALD growth at a rate of 0.7 Å/cycle. TiN films produced through this process exhibited decreasing sheet resistivity with increased TiN thickness; as such, 75 nm TiN was deposited to obtain a sheet resistivity of 27 Ω/square, as determined by contactless resistivity measurements [203]. No residual precursor/carbon contamination was detectable via XPS. Ti/Au top gate contacts were then fabricated by E-beam deposition and liftoff, and were used as an etch mask for self-aligned $SF_6$-RIE etching to remove the TiN outside the gate regions. Calibration witness samples were again utilized to minimize over-etching the TiN into the underlying $SiN_x$ layer.

As-fabricated HEMTs and corresponding VdP structures were initially tested using standard static I-V measurements to assess device performance and process effects on the HEMT structure itself. Pulsed I-V measurements were also performed to compare dynamic on-resistance ($R_{on,dyn}$) for devices with each gate material; testing was conducted from quiescent drain voltages ($V_{dsq}$) between 0–50 V, with a quiescent gate voltage $V_{gsq}$ = -6 V, pulse width 500 ns and 1 ms pulse spacing for a duty cycle of 0.05%. Electrical stress stability was conducted through reverse bias sweep, step-stress, and constant bias timed stressing in a normal air atmosphere. Thermal stability was evaluated through sequential device annealing in flowing $N_2$ at temperatures between 400–1000 °C in 100 °C increments for 10 minutes at a time, with device characteristics compared after each anneal.

## 8.3 Comparison of As-Fabricated Devices

Static I-V measurements were used to evaluate the performance of the TiN- and Ni/Au-gated HEMTs after fabrication. Relevant device parameters are shown in Table 8.1, and graphically in Fig. 8.2. The TiN-gated devices exhibited improved on-state characteristics, in the form of greater maximum transconductance ($g_{m,max}$) and on-state drain current ($I_{ds,max}$) while having lower static on-resistance ($R_{on}$) than the Ni/Au-gated devices. Performance improvements came at the expense of greater off-state leakage in the TiN devices. The increased reverse leakage may be due to the lower TiN barrier height with the AlGaN (0.5 eV for TiN versus 0.7 eV for Ni, as calculated from temperature-dependent gate I-V measurements), or to the formation of a leaky interfacial layer in the initial stages of TiN deposition [141, 142, 209–211]. The 2DEG density ($n_s$) and carrier mobility ($\mu_{2DEG}$) were found to be degraded more (relative to the as-grown structure) in the reference sample than in the sample subjected to the TiN ALD growth process. The degradation was largely attributed to fluorination of the AlGaN barrier under the gate during the $SiN_x$ recess etch process [212]. The TiN-gated devices were likely annealed during the TiN growth process, thereby partially recovering the carrier density and mobility relative to the unannealed Ni/Au-gated devices [212].

Dynamic current-voltage measurements were also performed to compare the effects of gate material on $R_{on,dyn}$ [213]. From the values listed in Table 8.1 and shown in Fig. 8.3, the TiN-gated devices exhibited drastically improved current collapse over the range of quiescent drain voltages ($V_{dsq}$) from 0 to 50 V, as evidenced by the 12% increase in $R_{on,dyn}$ compared to the 130% increase exhibited by the Ni/Au-gated HEMTs. The improved current

collapse was attributed to the increased off-state leakage current for the TiN-gated HEMTs. The higher leakage current allows for electrons to be collected rather than trapped near the AlGaN/GaN interface during the off-state quiescent voltage stress.

Table 8.1. Representative device parameters for as-fabricated Ni/Au- and TiN-gated HEMTs.

| Parameter | Units | Ni/Au Gate | TiN Gate |
|---|---|---|---|
| $V_t$ | V | -2.47 | -2.77 |
| $I_{off}$ ($V_{gs}$ = -10V) | mA/mm | 0.179 | 4.88 |
| $g_{m,max}$ | mS/mm | 140 | 159 |
| $I_{ds,max}$ ($V_{gs}$ = 1V) | mA/mm | 471 | 589 |
| $R_{on}$ | Ohm·mm | 8.61 | 8.10 |
| $q\phi_b$ | eV | 0.7 | 0.5 |
| $n_s$ | $cm^{-2}$ | $6.76\times10^{12}$ | $7.75\times10^{12}$ |
| $\mu_{2DEG}$ | $cm^2/(V\cdot s)$ | 1890 | 1950 |
| $R_{on,dyn}$ ($V_{dsq}$ = 0 V) | Ohm·mm | 8.3 | 8.1 |
| $R_{on,dyn}$ ($V_{dsq}$ = 50 V) | Ohm·mm | 19.4 | 9.0 |

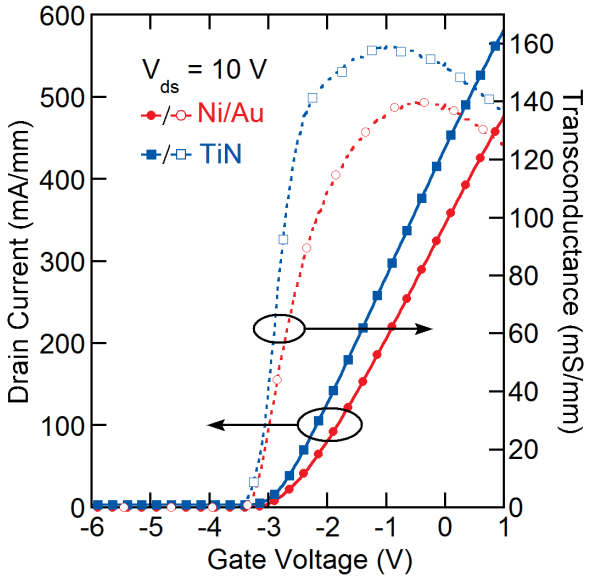


Fig. 8.2. Turn-on ($I_{ds}$ and $g_m$ versus $V_{gs}$) characteristics for Ni/Au- and TiN-gated HEMTs at $V_{ds}$ = 10 V.

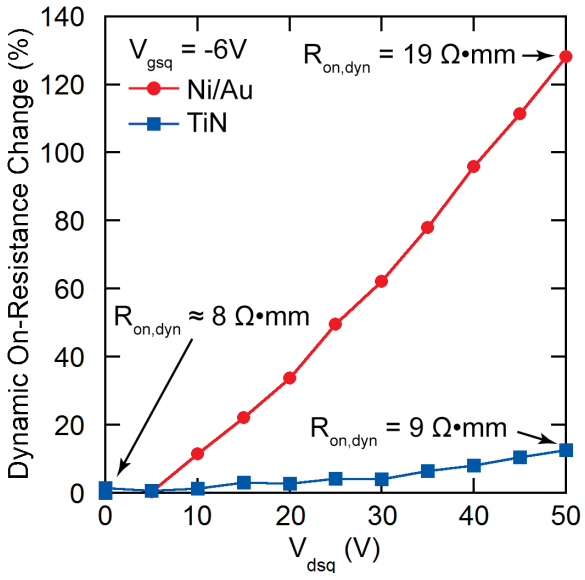


Fig. 8.3. Change in dynamic on-resistance as a function of quiescent drain-source voltage for Ni/Au- and TiN-gated HEMTs.

## 8.4 Electrical Stability of TiN Gates

Reverse bias gate voltage sweeps ($V_{ds}$ = 0) on the Ni/Au and TiN-gated HEMTs are shown in Fig. 8.4. Degradation in the Ni/Au gate current began at a critical voltage of approximately $V_{gs}$ = -120 V, indicated by the abrupt increase and subsequent instability in gate current beyond this critical voltage. This observation is consistent with previous reports of Ni/Au current instability under high reverse bias due to defect formation and subsequent metal migration in the AlGaN barrier caused by increased strain from the inverse piezoelectric effect [214–216]. The TiN-gated HEMTs exhibited instability at much higher critical voltage of $V_{gs}$ = -210 V, though with significantly higher overall leakage current levels in comparison to the Ni/Au gates. Since the TiN as a refractory metal nitride should be relatively immune to diffusion/migration effects, any current instability would likely

only become noticeable after more severe damage to the AlGaN as evidenced by the higher critical voltage.

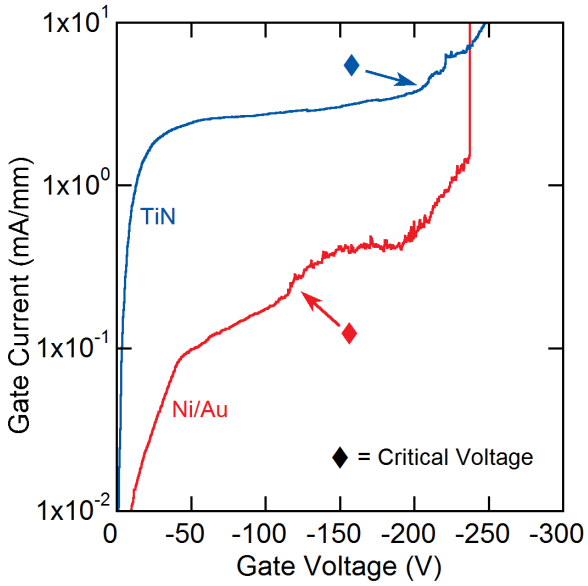


Fig. 8.4. Reverse bias gate sweeps from $V_{gs} = 0$ to breakdown for tested devices. The critical voltage for the onset of degradation is marked for each gate scheme.

To evaluate the breakdown characteristics of the gates, reverse bias gate-source step-stress measurements (-10 V steps) were used to test five devices with each gate scheme to breakdown. Under these conditions, the TiN-gated HEMTs failed catastrophically at higher and less variable reverse bias in comparison to the Ni/Au gates ($V_{gs} = -270 \pm 10$ V for the TiN, versus $-240 \pm 30$ V for Ni/Au), likely because of metal migration effects in the Ni/Au-gated HEMTs that exacerbated gate degradation.

Gate currents for both the Ni/Au- and TiN-gated HEMTs were compared before and after constant bias gate stressing at $V_{gs} = -140$ V ($V_{ds} = 0$) for one hour, as shown in Fig. 8.5. This stress condition was selected in order to evaluate the stability of the TiN gates just beyond the observed critical voltage that should degrade, but not destroy, the Ni/Au gates.

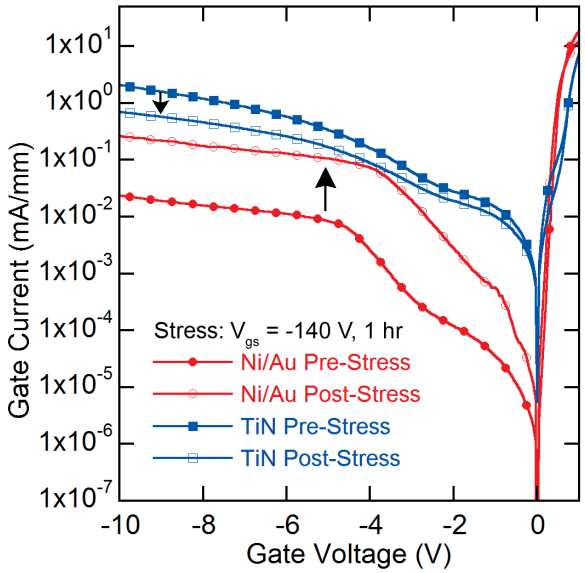


Fig. 8.5. Magnitude of gate current as a function of gate voltage for Ni/Au- and TiN-gated HEMTs before and after stressing at $V_{gs}$ = -140 V ($V_{ds}$ = 0).

The Ni/Au gates indeed degraded as a result of the constant bias stress test, as evidenced by the nearly order of magnitude increase in reverse leakage current after stressing. The TiN gates, however, exhibited a decrease in reverse leakage current after stressing, indicating that they were more stable under these reverse bias conditions than the usual Ni/Au gates. No change in Schottky barrier height was observed before and after TiN gate stressing; this suggested that the reduction in leakage current stemmed from localized heating effects, such as improvement in the AlGaN/TiN/Ti/Au interfaces due to sintering/burn-in, without significant change to the TiN itself.

## 8.5 Thermal Stability of TiN Gates

To assess the thermal stability of the Ni/Au- and TiN-gated HEMTs, four devices from each sample were sequentially annealed in flowing $N_2$ at temperatures between

400–1000 °C in 100 °C increments for 10 minutes at a time to allow comparison of the device output characteristics after each anneal. Fig. 8.6 shows the gate leakage current magnitude at $V_{gs}$ = -10 V ($V_{ds}$ = 0) for Ni/Au and TiN-gated HEMTs after annealing at each temperature.

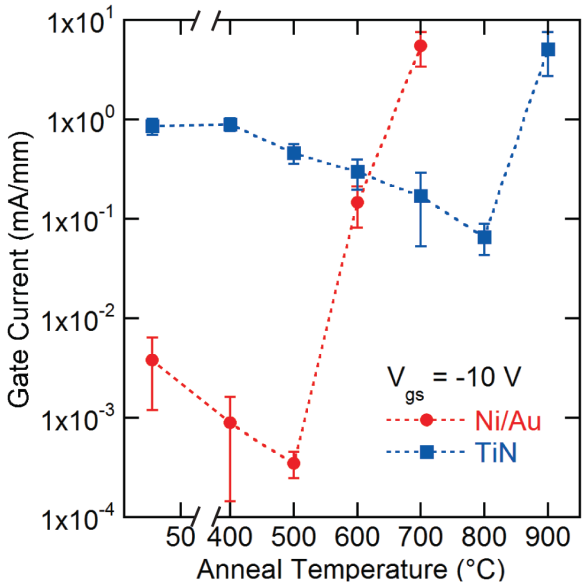


Fig. 8.6. Magnitude of gate current at $V_{gs}$ = -10 V for Ni/Au and TiN gates after sequential annealing up to 900 °C for 10 minutes.

Annealing at moderate temperatures up to 500 °C led to reductions in reverse leakage current for both the Ni/Au and TiN gates [143, 217, 218]. Higher temperature anneals led to substantial increases in Ni/Au gate leakage, with the leakage current becoming nearly equivalent to the forward on-state gate current after annealing at 700 °C, and device failure (open gate, always on) at 800 °C. Reverse leakage currents for the TiN, however, largely continued to decrease with annealing to temperatures as high as 800 °C, while maintaining high forward gate current levels. Large increases in gate leakage were observed after 900 °C annealing, indicating that this temperature was sufficient to degrade the devices. Devices

annealed at 1000 °C no longer exhibited high current in the on-state (always off). On-state device performance ($I_{ds}$-$V_{ds}$) curves are shown in Fig. 8.7 for as-fabricated HEMTs and HEMTs annealed at 800 °C. Corresponding optical images of the devices before and after 800 °C annealing are shown in Fig. 8.8. As expected from the $I_{gs}$-$V_{gs}$ measurements, the Ni/Au-gated HEMTs no longer modulated after annealing at 800 °C, as the devices were always in the on-state for $V_{gs}$ between -10 V and 1 V. Optical imaging (Fig. 8.8b) indicated severe damage to the Ni/Au gate metallization, resulting in loss of gate control over the device. The TiN-gated HEMTs were still functional after the 800 °C anneal, which agrees with other results for sputtered TiN-gated HEMTs [207]. $I_{ds,max}$ was degraded by approximately 29% relative to the as-fabricated device, which was likely due to thermal degradation of the Ohmic contacts and alloying of the Ti/Au overlay metal after extended durations above 600 °C [219]. This degradation was observed in Fig. 8.8c, while the gates appeared intact and functional. This demonstrated improvement in thermal stability over Ni/Au gates should allow TiN to be integrated with other high temperature HEMT processing steps, such as diamond heat spreader growth/etching after gate deposition, or Ohmic contact annealing with TiN grown in situ during the AlGaN/GaN growth process [5, 37, 220].

## 8.6 Chapter Summary

ALD TiN-gated HEMTs were successfully shown to yield improved performance over Ni/Au-gated HEMTs. As-fabricated device characterization indicated improved static electrical performance from the TiN-gated HEMTs, at the expense of higher off-state gate

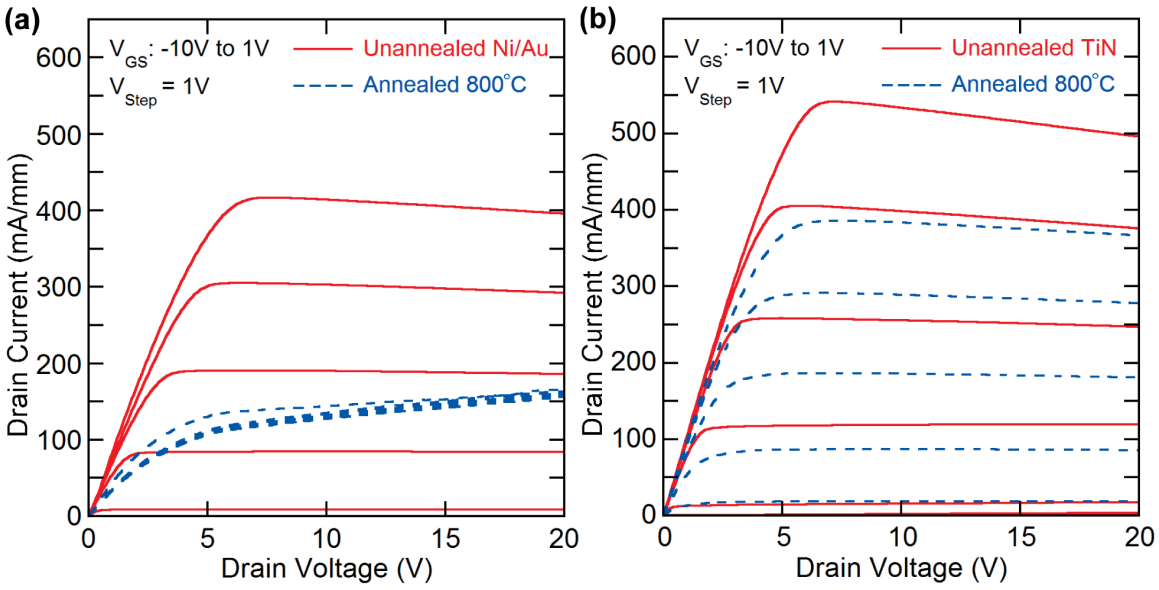


Fig. 8.7. Drain current-drain voltage ($I_{ds}$-$V_{ds}$) characteristics of (a) Ni/Au- and (b) TiN-gated HEMTs as-fabricated and after annealing at 800 °C for 10 minutes.

leakage currents attributed in part to a lower Schottky barrier with the AlGaN/GaN structure. The TiN gates exhibited improved tolerance to reverse bias electrical stressing relative to the reference Ni/Au gates, as evidenced by a higher critical voltage ($V_{gs}$ = -210 V for TiN, versus -120 V for Ni/Au) and a higher, less variable breakdown voltage ($V_{gs}$ = -270 ± 10 V for TiN, compared to -240 ± 30 V for Ni/Au). Constant bias gate stressing at $V_{gs}$ = -140 V (just above the Ni/Au critical voltage) for one hour caused the Ni/Au to degrade, with leakage currents increasing by nearly an order of magnitude, while the TiN leakage was reduced by the stressing. Annealing experiments revealed that the Ni/Au gates degraded after annealing above 500 °C for 10 minutes, as evidenced by dramatically increased leakage current, while the TiN did not severely degrade until being annealed at temperatures above 800 °C. These assessments indicate that ALD of TiN is a strong candidate technique for fabrication of electrothermally reliable HEMTs with transition metal nitride gates. The advances presented

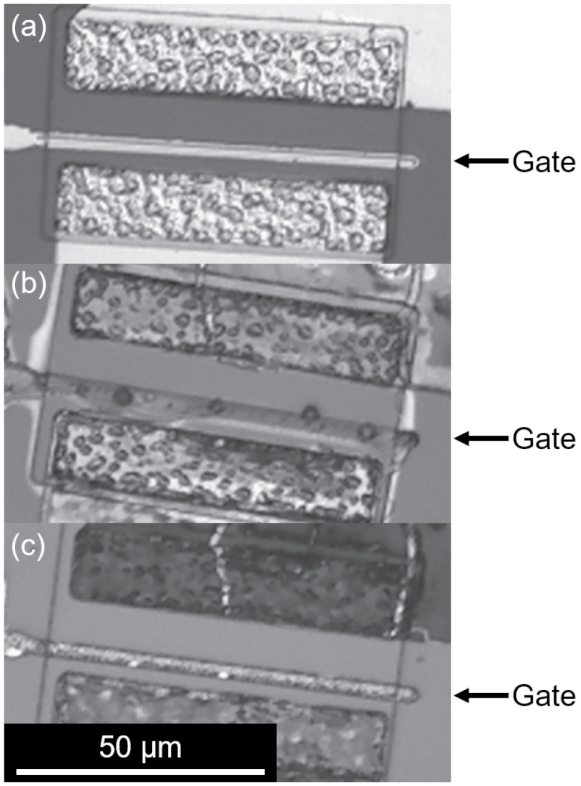


Fig. 8.8. Optical micrographs showing (a) as-fabricated HEMTs, (b) Ni/Au-gated HEMTs after 800 °C annealing, and (c) TiN-gated HEMTs after 800 °C annealing.

here also stand to benefit $Ga_2O_3$ switch technology. Promising investigations into ALD TiN integration with $Ga_2O_3$ have been performed on simple diode structures by Tadjer et al., but TiN gates for $Ga_2O_3$ switches have not yet been thoroughly investigated [221].

# Chapter 9: Plasma-Free Thermal Etch for Nanocrystalline Diamond Heat Spreading Films

## 9.1 Introduction

NCD thin films are of great interest for thermal management and passivation of electronic devices due to a high thermal conductivity and high electrical resistivity in undoped films [222, 223]. Thermal management is particularly important for WBG/UWBG semiconductors, some of which, such as $Ga_2O_3$, are very poor thermal conductors and are thus subject to thermal degradation during high power switching. In order to effectively integrate these films into device fabrication processes, selective patterning techniques for creation of NCD features must be developed. At present, two major avenues exist for patterning NCD: selective-area CVD or $O_2$-plasma etching of blanket films. A variety of selective-area deposition processes have been reported; however, the additional processing steps required to generate NCD features while simultaneously avoiding spontaneous nucleation of diamond outside the regions of interest greatly increase process complexity [224–226]. Plasma-based etching processes represent a much simpler alternative to selective-area deposition, and can be used to selectively remove portions of blanket films of NCD [37, 227, 228]. However, the energetic nature of these etching processes can create defects in device layers sensitive to $O_2$-plasma underneath the NCD films during the final stages of etching [222, 229–231]. In the case of GaN devices, surfaces exposed to $O_2$ plasma prior to gate insulator deposition exhibit higher MOS leakage current than surfaces processed by thermal oxidation [147]. Plasma etching of diamond is also extremely anisotropic, and an isotropic etch for diamond is not readily available. Development of an isotropic etch would aid in fabrication of dia-

mond films into complex geometries that cannot easily be performed by plasma etching, such as thinning of diamond films on cooling vias and vertical channels, or fabrication of conical diamond structures for electron emitters and atomic force microscope probes [232–234].

In this work, a dry thermal oxidation process for selective etching of NCD films has been developed. A number of studies have examined oxidation processes of diamond crystals and films in oxygen or air atmospheres, wherein the diamond and any graphite or amorphous carbon formed during the growth process are oxidized into volatile CO/$CO_2$ compounds [52, 235–240]. However, this knowledge has yet to be developed into a selective etching process for NCD films. The process detailed in this work is advantageous for NCD integration into electronic devices, as NCD films can be etched on both lateral and vertical features without plasma-induced damage to the host semiconductor regions.

## 9.2 Process Development for Diamond Thermal Etching

Samples were fabricated according to the process flow shown schematically in Fig. 9.1. NCD films with thicknesses of 0.9 $\mu$m and grain size of approximately 190 nm were prepared on Si substrates by microwave plasma chemical vapor deposition (MW-CVD) [241]. These films were then covered with a blanket mask of $SiO_2$ (PECVD, 100 nm or 1000 nm), $SiN_x$ (PECVD, 100 nm or 1000 nm), or $Al_2O_3$ (ALD, 50 nm). Prior to patterning, one set of masked samples was heated to 700 °C at a ramp rate of 600 °C/min and held for 15 min under 100 sccm of flowing $O_2$ in an AnnealSys AS-One RTA to assess the integrity of the mask materials under etching conditions. A second set of samples was subjected

to a vacuum anneal (pressure below $1.5\times10^{-4}$ Torr) in the AS-One at 750 °C for 10 min prior to mask deposition in order to remove volatile products from the NCD film that could compromise the mask integrity during etching. These films were observed post-annealing using an Olympus BX51 optical microscope with Nomarski contrast filters and a JEOL JSM-7600F scanning electron microscope to search for etch pits due to pinholes or film delamination.

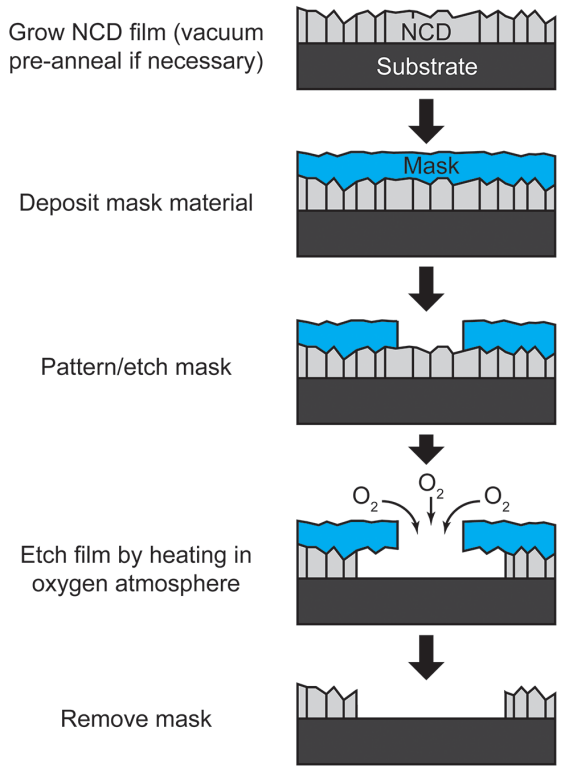


Fig. 9.1. General process flow for fabrication and etching of masked NCD films.

Masked samples were then patterned using conventional photolithography techniques to selectively expose 1–100 $\mu$m features in the NCD films. Features were defined in the $SiN_x$ masks using $SF_6$ ICP-RIE etching. $SiO_2$ and $Al_2O_3$ masks were patterned using buffered HF wet etching. Initial process demonstration was performed using a Neytech Qex furnace at

650–900 °C with a ramp rate of 50 °C/min under approximately 500 sccm of continuously flowing $O_2$ at atmospheric pressure, in order to assess suitable etching temperatures and times. These studies indicated that etching at temperatures below 700 °C was too slow for efficient processing, while etching at temperatures above 800 °C occurred so quickly that the etch could not be easily controlled. As such, process temperatures of 700, 750, and 800 °C and times of 4–20 min were selected for more precise determination of the NCD lateral and vertical etching rates. $SiO_2$ was selected as the mask material, based on the mask integrity results detailed later in this work. The AnnealSys AS-One RTA was employed for the etch rate studies using the process profile shown in Fig. 9.2, as the RTA allowed better control over the sample temperature and process atmosphere than could be achieved in the Neytech furnace. As the NCD samples exhibited no change during annealing in nitrogen at the selected temperatures, flowing $N_2$ atmospheres were employed during heating and cooling to prevent unwanted etching and allow precise control over the oxygen etch time. Masked NCD samples were heated to temperature at a ramp rate of 600 °C/min under 100 sccm of flowing $N_2$ after an initial 1000 sccm flowing $N_2$ purge at room temperature. A 100 sccm flowing $O_2$ atmosphere (chamber pressure of $9\times10^{-2}$ Torr) was maintained while at temperature to etch the NCD films, while cooling was performed under a 1000 sccm $N_2$ purge atmosphere. Following the etching process, lateral etch rates were measured using optical imaging of the mask undercut regions. Vertical etch rates were measured using a Tencor AlphaStep 500 stylus profilometer after stripping the etch mask. Raman spectroscopy and focused ion beam (FIB)/SEM were used to evaluate NCD decomposition in/near exposed features, using a Thermo Scientific DXR Raman Microscope (4 mW laser at a wavelength of 532 nm, and 100× objective lens with numerical aperture of 0.90 and

working distance of 210 $\mu$m) and an FEI Nova 600 NanoLab, respectively.

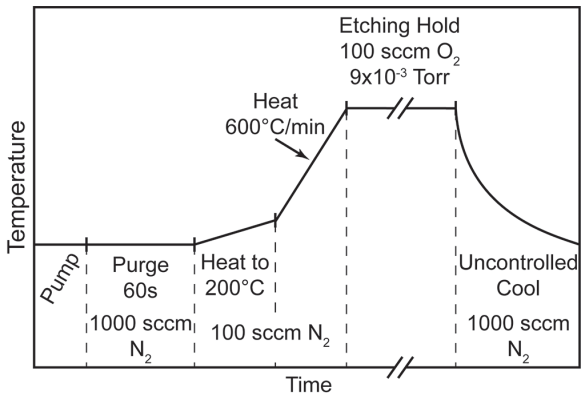


Fig. 9.2. General process profile for NCD thermal etch rate studies performed in the AnnealSys AS-One RTA. (Etching hold temperature and time were varied between 700–800 C and 4–20 min, respectively).

## 9.3 Masking and Etching Process Evaluation

### 9.3.1 Mask Material Comparison

Evaluation of the masks on non-outgassed NCD after annealing at 700 °C for 15 min indicated that thick (1000 nm) PECVD $SiO_2$ was suitable for use on as-grown NCD films, with minimal pinholes observed ($<$10 cm$^{-2}$). However, the thin (100 nm) PECVD $SiO_2$ developed a large number of pinholes and near-surface blisters ($\sim$10$^3$ cm$^2$), as shown in Fig. 9.3a. The ALD $Al_2O_3$ masks (Fig. 9.3c) also formed numerous blisters ($\sim$10$^5$ cm$^{-2}$), while both the thin and thick PECVD $SiN_x$ masks completely delaminated from the as-grown NCD (Fig. 9.3b).

The mask defects introduced by annealing were suspected to be at least partially due to the release of residual gases trapped in or on the NCD film, possibly hydrogen or

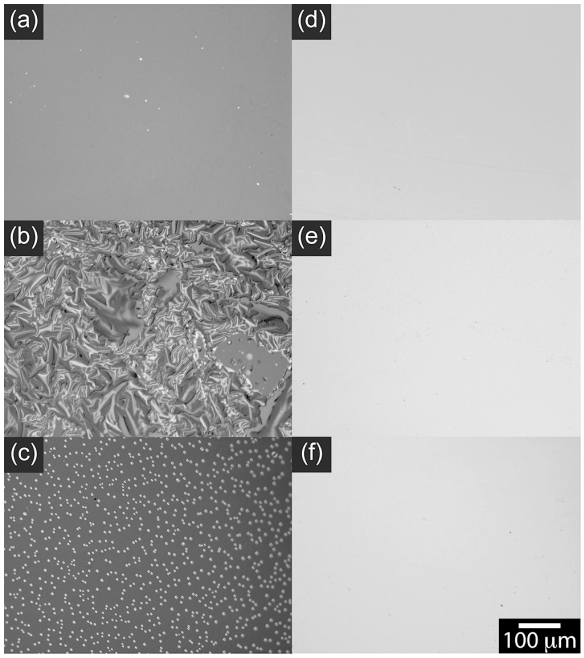


Fig. 9.3. Representative Nomarski contrast optical images of NCD films annealed at 700 °C for 15 min, masked with (a) 100 nm $SiO_2$ without NCD pre-anneal, (b) 100 nm $SiN_x$ without NCD pre-anneal, (c) 50 nm $Al_2O_3$ without NCD pre-anneal, (d) 1000 nm $SiO_2$ with NCD pre-anneal, (e) 100 nm $SiN_x$ with NCD pre-anneal, and (f) 50 nm $Al_2O_3$ with NCD preanneal.

residual hydrocarbons from the diamond growth process [242, 243]. As such, a second set of NCD films was pre-annealed under vacuum (pressure $<1.5\times10^4$ Torr) at 750 °C for 10 min prior to mask deposition. This outgas pre-anneal corrected the delamination and blistering issues initially observed with the thin $SiO_2$, thin $SiN_x$, and $Al_2O_3$ films, as shown in Fig. 9.3d–f. However, the thick $SiN_x$ film still completely delaminated; outgassing of the nitride mask itself during heating is suspected to be responsible for the catastrophic mask damage. For the remainder of the study, thick (1000 nm) $SiO_2$ films were chosen as the mask material, as they could be used on either outgassed or non-outgassed NCD films without defect formation or film delamination. These results also suggest that 100 nm $SiO_2$, 100 nm $SiN_x$, and 50 nm ALD $Al_2O_3$ films were suitable mask materials, provided that the

underlying NCD film was annealed in vacuum prior to mask deposition.

### 9.3.2 Etch Profile Evaluation

Upon annealing in an oxygen atmosphere at temperatures of 700 °C and above, the masked NCD filmswere found to decompose both vertically and laterally, undercutting the mask material. The lateral etching was visible via optical imaging, as shown in Fig. 9.4 for 0.9 $\mu$m thick NCD films masked with 1000 nm $SiO_2$ and annealed at 750 °C under flowing $O_2$ for various times. Before etching (Fig. 9.4a), NCD was optically observable in the exposed features and underneath the mask. A slight lateral undercut was observed after a 5 min etch, with incomplete decomposition of the NCD within the exposed feature (residual carbon/NCD appears as the dark material in Fig. 9.4b). Longer etches allowed for complete clearing of the NCD film inside the feature, as well as easily visible lateral mask undercutting (Fig. 9.4c and d). Complete clearing of the features etched in the AS-One RTA occurred after 20 min at 700 °C, after 10 min at 750 °C, and just after 5 min at 800 °C.

Cross-sections of partially and completely etched features, shown in Fig. 9.5, were prepared via FIB milling to allow observation of the etch progression. Initial etching was found to occur primarily through diamond decomposition along grain boundaries, leading to roughening of the NCD film (Fig. 9.5b). Continued etching led to oxygen penetration into the highly defective nucleation layer and initiation of lateral etching along the underside of the NCD film (Fig. 9.5c) [244]. Lateral etching then progressed along the nucleation layer underneath the mask while the NCD grains completely decomposed with further etching, leading to the observed undercutting in cleared features (Fig. 9.5d).

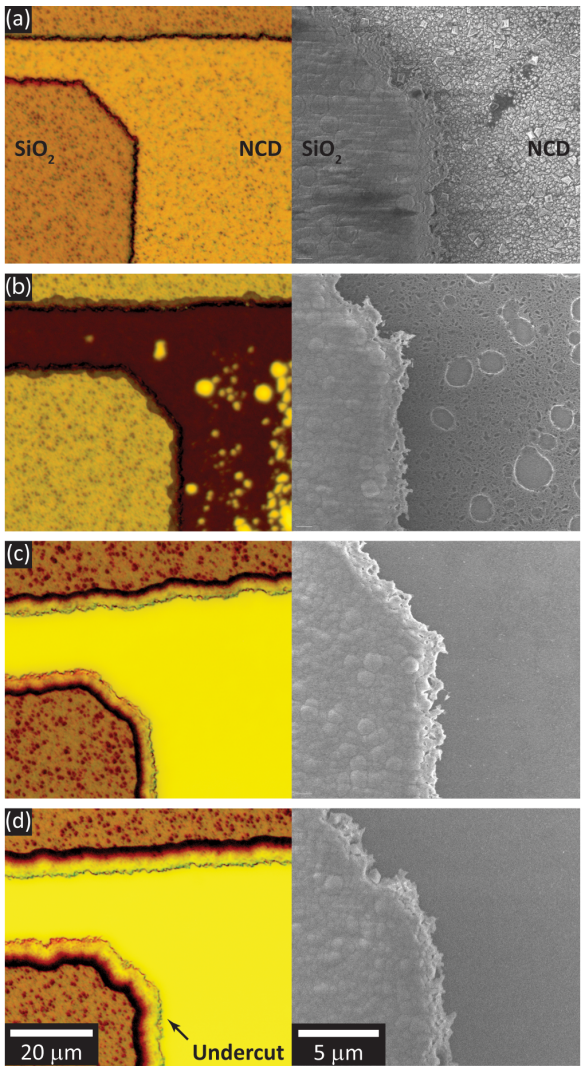


Fig. 9.4. Nomarski contrast optical images (left) and corresponding SEM images (right) of NCD films masked with 1 $\mu$m thick $SiO_2$, etched in $O_2$ at 750 °C for (a) 0 min, (b) 5 min, (c) 10 min, and (d) 15 min. Optical images show comparable undercutting of the mask along both straight and angled patterns.

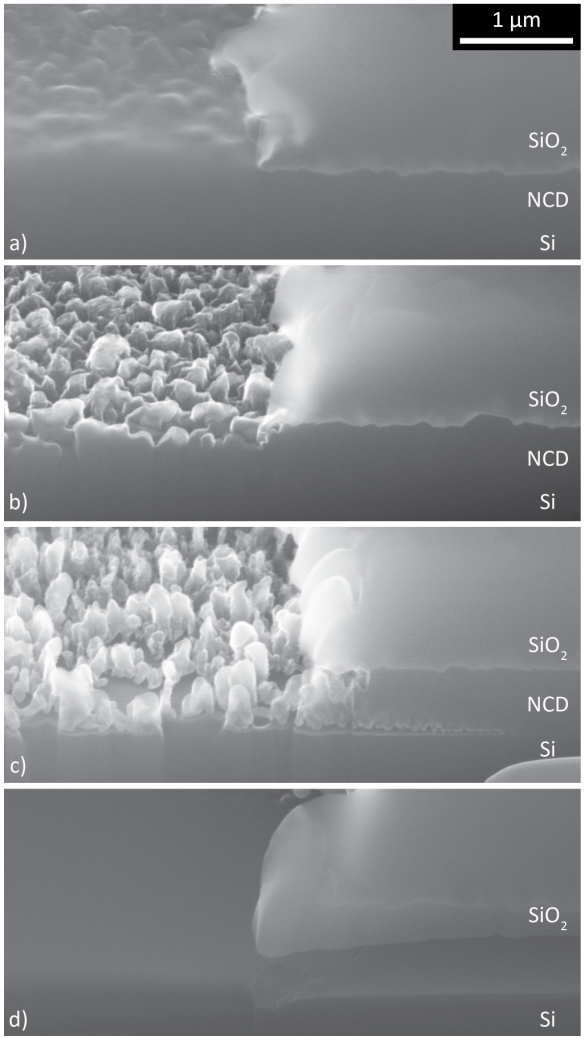


Fig. 9.5. Cross-sections of (a) unetched, (b–c) partially etched, and (d) fully etched features after etching at 700 °C. Etching progressed by oxygen penetration into the NCD grain boundaries and underlying nucleation layer, leading to lateral etching under the mask.

Raman spectroscopy was used to monitor the NCD decomposition after etching through observation of the characteristic peak of $sp^3$-bonded diamond (1333 $cm^{-1}$) and the broader peaks from disordered, non-$sp^3$ carbon (1400–1700 $cm^{-1}$) [245,246]. Fig. 9.6 shows a map of the full width at half maximum (FWHM) of the 1333 $cm^{-1}$ $sp^3$ peak overlaid on an optical image of a feature etched at 750 °C for 15 min. Full Raman spectra collected at the labeled points 1–5 are shown in Fig. 9.7. In both figures, the exposed area of the feature (Point 1) was free of diamond and any residual carbon. Near the mask edge (Point 2), very disordered carbon was observed, as evidenced by the very low intensity of the $sp^3$ and non-diamond carbon peaks in the Raman spectra. Further into the undercut zone (Point 3), broad carbon peaks appeared, indicating the presence of more disordered carbon remnants from the original NCD film. In the dark band observed underneath the mask (Point 4), both peaks were again observed, but with increasing sharpness of the 1333 $cm^{-1}$ peak, indicative of an increased diamond component to the underlying carbon. Finally, the masked NCD far away from the feature (Point 5) was adequately protected from etching, as evidenced by the narrow and sharp 1333 $cm^{-1}$ peak.

Cross-sectional imaging of the feature etched at 750 °C for 15 min, shown in Fig. 9.8, indicate an etching profile consistent with the Raman mapping. The exposed feature area (Point 1) was found to be clear of NCD and carbon residue. Etching progressed most rapidly along the bottom of the film, again indicating that oxygen penetrated and decomposed the defective nucleation layer more rapidly than the columnar growth section of the film [244]. Residual carbonaceous material was found adhered to the bottom side of the oxide mask, accounting for the carbon signals observed in the Raman spectra (Points 2 and 3). The

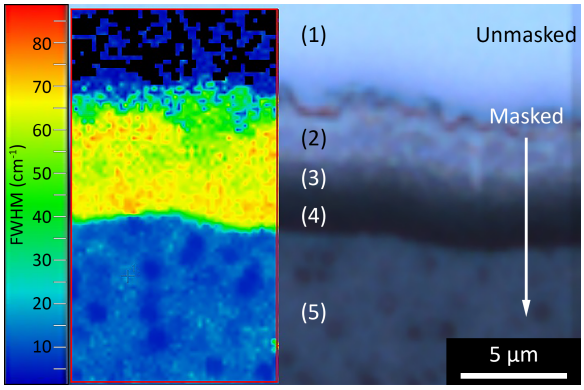


Fig. 9.6. Raman spectral map (left) of the FWHM of the 1333 $cm^{-1}$ peak overlaid on an optical image (right) of a masked etched feature. Numbered points in the optical image correspond to the positions at which full Raman spectra were captured.

damaged carbon zone immediately beyond the furthest undercut point (>4.4 $\mu$m from the mask edge) corresponded to the dark zone (Point 4) of partially decomposed NCD in the optical images and Raman maps.

### 9.3.3 Nanocrystalline Diamond Etch Rates

Lateral etching was measured with optical microscopy by measuring the distance from themask edge to the inner edge of the dark zone (between Points 3 and 4), as the previous Raman/FIB analyses indicated that NCD etching proceeded up to the edge of that zone. As shown in Fig. 9.9, lateral etching between 700–800 °C proceeded linearly with respect to time, with faster etching occurring at higher temperatures.

Vertical etch depths/rates are shown in Fig. 9.10. As with the lateral etching, faster vertical etching occurred at higher temperatures. Precise vertical etch depths became increasingly difficult to measure with increasing temperature, due to the rapid decomposition of the NCD films and preferential etching of the NCD along grain boundaries. Grain

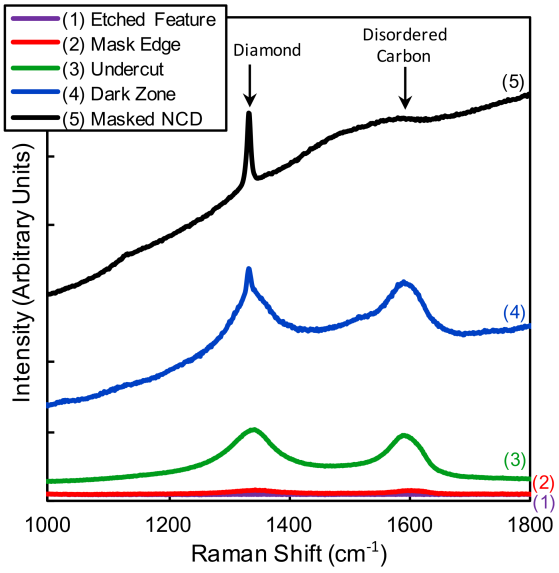


Fig. 9.7. Raman spectra collected at points along a masked and etched NCD feature. The sharp peak at 1333 $cm^{-1}$ indicates the presence of diamond, while the broad peak near 1333 $cm^{-1}$ and 1600 $cm^{-1}$ indicates residual non-diamond carbon remaining from decomposition during etching.

boundary etching resulted in roughened NCD surfaces within a given sample/feature area, leading to the large measurement uncertainty for the 4 min etch at 800 °C. This roughening, along with the vertical etch rate being approximately half of the lateral etch rate at any given temperature, indicated that oxygen decomposition through the disordered grain boundaries proceeded at a higher rate than on the columnar grains. This preferential etching is likely responsible for the initial delay in the onset of vertical etching evident in the etch rate data, as more time is required for decomposition of the crystalline diamond grains themselves than for the grain boundaries.

The lateral and vertical etch rates were fitted to an Arrhenius model to determine an activation energy ($E_a$) for etching, as shown in Fig. 9.11. $E_a$ was found to be very similar for both lateral and vertical etching (≈136–140 kJ/mol), suggesting that the decomposition process was similar in both cases. However, these activation energies are significantly

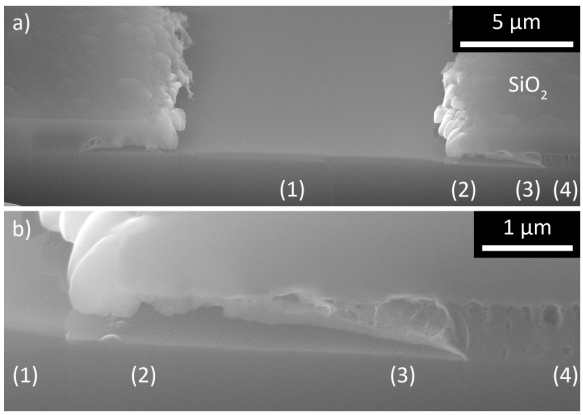


Fig. 9.8. Cross-sectional images of an NCD feature etched at 750 °C for 15 min at (a) lower and (b) higher magnification, with the marked points corresponding to the previous Raman spectra.

lower than the activation energies of 303–318 kJ/mol reported by Joshi, et al. obtained by thermogravimetric analysis of diamond films [247, 248]. The lower activation energy likely stemmed from the use of finer-grained and thinner NCD (grain size of approximately 190 nm and thickness of 0.9 $\mu$m) in the present study, as the smaller NCD grains would exhibit more surface and grain boundary area susceptible to oxygen attack.

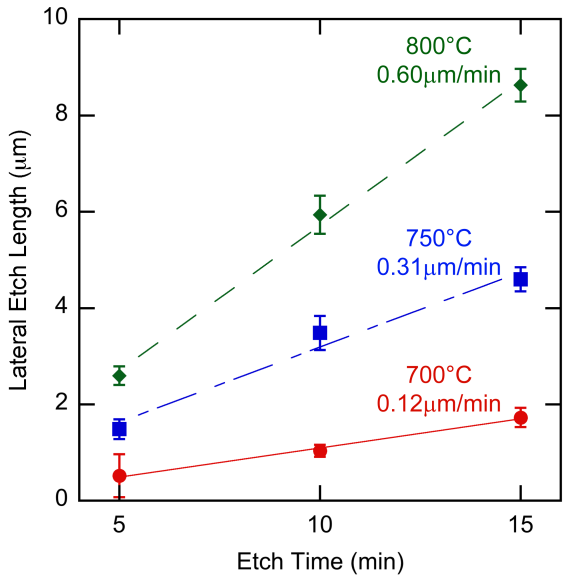


Fig. 9.9. Lateral etch distances and etch rates for thermal etching at 700–800 °C.

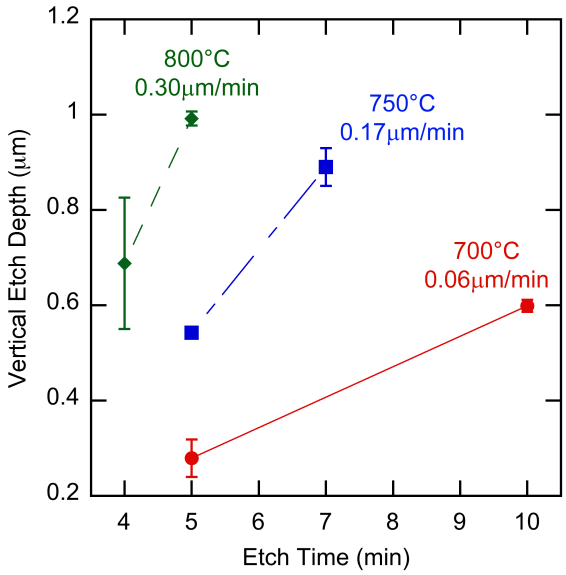


Fig. 9.10. Vertical etch distances and associated etching rates measured for thermal etching at 700 °C, 750 °C, and 800 °C.

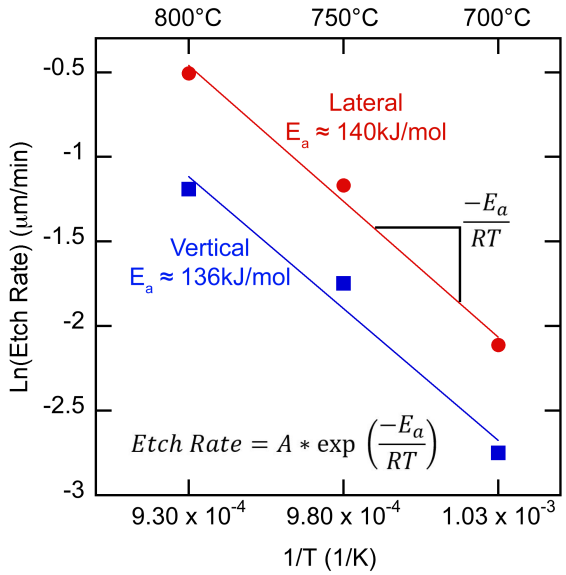


Fig. 9.11. Arrhenius plot used in determination of activation energy for lateral etching.

## 9.4 Chapter Summary

Dry, non-plasma oxygen thermal etching has been demonstrated for selective removal of NCD films. Hard mask materials such as $SiO_2$, $Si_3N_4$, and $Al_2O_3$ were evaluated for compatibility with this high temperature process. Thin (50–100 nm) films of all three materials were compatible with the process, provided that the underlying NCD film was vacuum annealed to remove residual volatiles from the growth process. Thick (1000 nm) $SiO_2$ was compatible with both as-grown and vacuum-annealed NCD. Temperatures above 700 °C were effective for this etching process, with 0.9 $\mu$m thick NCD films being completely removed from patterned features as indicated by Raman spectroscopy and cross-sectional SEM imaging. Lateral etching proceeded more rapidly at higher temperatures, as evidenced by larger mask undercuts appearing after etching for a given time at higher temperatures. The vertical etch rate also increased with temperature, and was roughly half the rate of

the corresponding lateral etch rate at each temperature. This difference was attributed to more rapid etching through the disordered NCD grain boundaries and underlying nucleation layer. Despite the difference in etching rates, both vertical and lateral etching exhibited comparable activation energies, suggesting that the underlying oxidation mechanism is the same in both cases. As a plasma-free, less-anisotropic dry etch, this process stands to benefit NCD integration into WBG/UWBG power devices sensitive to $O_2$-plasma damage and with complex geometries.

# PART V
# CONCLUSIONS AND FUTURE WORK

# Chapter 10: Conclusions and Recommendations for Future Work

## 10.1 Conclusions

Power switches based on WBG and UWBG seimiconductors are positioned to have a significant impact on society by enabling more efficient and reliable systems for energy harvesting and control, communications, navigation, and transportation. This dissertation reports novel approaches to solving operational and reliability issues in these power switches. First, ALD high-k $ZrO_2$ and $HfO_2$ dielectrics were evaluated for integration with device-relevant GaN orientations using C-V and I-V measurements on MOS capacitors. $ZrO_2$ films grown using ZTB, an oxygen-containing ALD precursor novel to these WBG and UWBG systems, uniformly exhibited positive C-V curve shifts due to negative oxide charge related to excess oxygen in the dielectric. This came at the expense of a noticeable sensitivity of the accumulation capacitance to AC measurement frequency, indicating a loss mechanism related to the trapped oxygen that must be mitigated for stable use in power switches. Dielectrics grown using a more conventional Zr-precursor, TDMAZ, did not exhibit this negative charge or frequency dispersion with appropriate pre-ALD surface cleaning. With these two dielectric processes, $ZrO_2$ films can be deposited with varying amounts of negative charge that proved useful for $V_t$ manipulation in normally-on, n-channel GaN HEMTs. When integrated with $(\bar{2}01)$ $\beta$-$Ga_2O_3$, both dielectrics exhibited positive C-V curve shifts. Dominant forward bias leakage mechanisms were identified for both dielectrics related to trap states in the dielectrics commonly observed in $ZrO_2$ on other semiconductors. Additionally, $HfO_2$ dielectrics exhibited outstanding electrical interface

characteristics on $Ga_2O_3$ and are thus strong candidates for WBG and UWBG power switches. C-V measurements revealed high frequency stability, extremely low hysteresis and stretch-out for the $HfO_2/Ga_2O_3$ system, with one of the lowest measures of interface trap states for any dielectric on $Ga_2O_3$ to date. I-V measurements fit very well to the F-N tunneling model with an $HfO_2$-$Ga_2O_3$ conduction band offset of 1.3 eV that closely matched the value determined by XPS.

Innovative designs and processing for WBG and UWBG switches were then developed and characterized for this dissertation program. The two $ZrO_2$ variants used previously were integrated as gate dielectrics with $SiN_x$-passivated AlGaN/GaN MOS-HEMTs. Combination of different levels of negative dielectric charge, combined with AlGaN barrier recess etch processes under the HEMT gate, allowed $V_t$ to be manipulated to make the devices normally-on or normally-off over a total range of -3 to +4 V. Gate leakage was significantly reduced by dielectric incorporation relative to HEMTs with Ni-metal Schottky gates, allowing the MOS gates to be forward biased by an additional 8 V and useful current output to be achieved. Charge trapping associated with recess etching and negative charge in the ZTB-$ZrO_2$ dielectric contributed to poor current collapse under pulsed switching conditions, while devices with the TDMAZ dielectric exhibited comparable or even improved current collapse relative to Schottky-gated HEMTs. These dielectrics thus grant appealing capabilities in AlGaN/GaN HEMTs, though further work is needed to reduce charge trapping and current collapse in the ZTB/recessed gate HEMTs while still maintaining the negative oxide charge responsible for the strong normally-on behavior.

Critical design and process considerations for vertical GaN MOSFETs were presented. The design of a new photolithographic mask set for trench-gate MOSFETs was

described, along with a process for crystallographically aligning the mask set to specific non-polar GaN planes using TMAH faceting of a centrally located etched feature. Doping density and thickness specifications for a three-layer npn epitaxial layer structure were then presented, with a target blocking voltage of 1200–1500 V. This epilayer design was then sent to a commercial vendor for material growth on a 2" bulk GaN substrate, which was then characterized for use in trench-gate MOSFET fabrication. Several key challenges were presented that must be resolved for device fabrication, including good Ohmic contact to the buried p-body layer after etching access windows through the source layer, trench processing to create uniform interfaces between the trench sidewalls and bottoms without microtrenching defects, and gate contact deposition along highly vertical sidewalls without discontinuities.

UWBG switch architectures based on H:diamond with 2D p-channels were also reported. Switches with an $Al_2O_3$ gate dielectric and surface transfer dopant were fabricated directly onto the substrate surface after hydrogen termination. An innovative mounting scheme was developed to allow photoresist processing and contact lithography while reducing edge beads and other photoresist defects that arose from the small substrate geometry. Standard device testing indicated normally-on behavior ($V_t$ = 4 V), current output up to approximately 60 mA/mm and low gate leakage. The peak hole mobility was estimated to be 50 $cm^2/V{\cdot}sec$ from the maximum transconductance extracted from $I_d$-$V_g$ measurements. Devices exhibited relatively stable current output over the course of one week, with slightly reduced current output and increased on-resistance due to probing damage in the weakly-adhered Au Ohmic contacts.

Finally, novel materials and processes were developed for improved electrical and

thermal stability in power switches. TiN transition metal nitride gates for AlGaN/GaN HEMTs were demonstrated as a more stable and reliable alternative to conventional Ni-based Schottky metal gates. TiN-gated HEMTs exhibited improved current output, lower on-resistance, and reduced current collapse compared to the Ni gates, albeit at the expense of a lower Schottky barrier height and increased gate leakage current. Using high reverse bias gate sweeping as a form of accelerated life test, TiN gates exhibited higher critical voltages for the onset of gate degradation and higher breakdown voltages than the Ni gates. Rapid thermal annealing was also used to determine the thermal stability of TiN-gated HEMTs, which retained functionality after annealing to temperatures as high as 800 °C. This represents an 300 °C improvement over the conventional Ni-gated HEMTs. A novel process for plasma-free selective area patterning and etching of NCD heat spreading films was also presented. After patterning an $SiO_2$ hardmask on top of blanket-grown NCD films, exposure to an oxygen atmosphere at 700–800 °C was used to selectively oxidize and etch away the NCD without use of an oxygen plasma that can damage semiconductor device structures underneath the NCD film. Etching was monitored using optical microscopy, FIB cross-sectioning and SEM imaging, and Raman microscopy. Lateral and vertical etching was observed, making this process less-anisotropic than a conventional oxygen plasma etch. Additionally, as a plasma-free process, etching can be achieved without line-of-sight, such that NCD films along backside vias and other complex geometries can be achieved.

The contributions reported in this dissertation are expected to benefit the power electronics community by providing new understanding of materials integration and fabrication processes for WBG and UWBG switches. The significance of the work reported herein, and additional work performed under this research program that was not expressly detailed here,

has been recognized by its inclusion in 16 journal publications, 29 conference presentations, and one U.S. Patent. A complete listing of these scholarly outputs is given in Appendix A.

## 10.2 Future Work

Continuing study of several promising topics is recommended based on the results reported in this dissertation:

- *Defect quantification and control in $ZrO_2$ high-k dielectrics for WBG and UWBG MOS systems* – Changes in threshold voltage in WBG/UWBG switches through Zr-precursor selection is an appealing capability. However, the stability and control of the negative charge responsible for these changes must be further explored. A primary concern is whether the frequency dispersion observed in the ZTB dielectrics can be mitigated while still preserving the negative charge. Annealing experiments and other adjustments to the ALD process sequence could present routes for mitigation or stabilization of the negative charge, but were not attempted as part of this work. Temperature-dependent C-V and I-V measurements, along with more intensive methods of quantifying interface trap densities would assist in these studies. Combining the ZTB and TDMAZ-grown $ZrO_2$ in a multilayer composite $ZrO_2$ film might offer a combination of the best of both dielectrics, with the negative charge of the ZTB and the higher interface quality, lower trapping, and frequency stability of the TDMAZ dielectrics.

- *Vertical GaN switch fabrication* – The complexities for fabricating vertical GaN devices highlighted in this work must be addressed in the future. Particular attention

must be paid to achieving consistent Ohmic contact to commercially-grown p-GaN epilayers, fabrication of trench gates without microtrenching effects, and integration of the promising high-k dielectrics studied in this dissertation. The last point represents a truly novel contribution, as $ZrO_2$ and $HfO_2$ have not yet been demonstrated in a vertical MOSFET. To achieve these goals, consistent sources of semiconductor and dielectric material must be established, since these capabilities either do not currently exist or are not widely available at UMD. This requires that close collaborations between the device fabricators at UMD and commercial vendors or national laboratory providers be established or continued, with the teams working to achieve disruptive advances for vertical GaN switch technology.

- *Diamond switch sample consistency* – Consistency in device performance will be beneficial for diamond device studies. A more mechanically reliable contact scheme should be implemented, either through addition of overlay pads with adhesion layers, or through implementation of alloyed contact processing. Device fabrication on undoped epilayers, rather than directly on the HPHT substrates, may further improve device-to-device and substrate-to-substrate consistency.

- *NCD thermal management integration with $Ga_2O_3$* – The feasibility of integrating nanocrystalline diamond heat-spreading thin films with $Ga_2O_3$ and other cooling schemes should be determined. Due to the low thermal conductivity of $Ga_2O_3$, this element of future work stands to greatly benefit $Ga_2O_3$ switch technology if successful. If so, the plasma-free NCD etch process developed in this dissertation may also be applicable.

# Appendix A: Publications, Presentations, and Patents

## A.1 Publications

The following scholarly publications have been authored or co-authored as part of this dissertation work:

1. **D.I. Shahin**, M.J. Tadjer, V.D. Wheeler, A.D. Koehler, T.J. Anderson, C.R. Eddy, Jr., A. Christou, "Electrical Characterization of ALD $HfO_2$ High-k Dielectrics on $(\bar{2}01)$ $\beta$-$Ga_2O_3$," *Applied Physics Letters* 112, 042107 (2018). DOI: 10.1063/1.5006276.

2. V.D. Wheeler, T.J. Anderson, S. Ahn, **D.I. Shahin**, M.J. Tadjer, A.D. Koehler, K.D. Hobart, F. Ren, F.J. Kub, A. Christou, C.R. Eddy, Jr., "ALD TiN Schottky Gates for Improved Electrical and Thermal Stability in III-N Devices," *ECS Transactions* 80 [3], 17-25 (2017). DOI: 10.1149/08003.0017ecst.

3. **D.I. Shahin**, T.J. Anderson, A. Christou, "Achieving Vertical Trench-Gate GaN MOSFETs Via Process Optimization," *ECS Transactions* 80 [7], 139-145 (2017). DOI: 10.1149/08007.0139ecst.

4. **D.I. Shahin**, A. Christou, J.E. Butler, "High Power Diamond Devices with 2-D Transport Channels," *ECS Transactions* 80 [7], 197-201 (2017). DOI: 10.1149/08007.0197ecst.

5. M.J. Tadjer, V.D. Wheeler, **D.I. Shahin**, C.R. Eddy, Jr., F.J. Kub, "Thermionic Emission Analysis of TiN and Pt Schottky Contacts to $\beta$-$Ga_2O_3$," *ECS Journal of Solid State Science and Technology* 6 [4], P165-P168 (2017). DOI: 10.1149/2.0291704jss.

6. V.D. Wheeler, **D.I. Shahin**, M.J. Tadjer, C.R. Eddy, Jr., "Band Alignments of Atomic Layer Deposited $ZrO_2$ and $HfO_2$ High-k Dielectrics with $(\bar{2}01)$ $\beta$-$Ga_2O_3$," *ECS Journal of Solid State Science and Technology* 6 [2], Q3052-Q3055 (2017). DOI: 10.1149/2.0131702jss.

7. A.D. Koehler, T.J. Anderson, M.J. Tadjer, A. Nath, B.N. Feigelson, **D.I. Shahin**, K.D. Hobart, F.J. Kub, "Vertical GaN Junction Barrier Schottky Diodes," *ECS Journal of Solid State Science and Technology* 6 [1], Q10-Q12 (2017). DOI: 10.1149/2.0041701jss.

8. M.J. Tadjer, T.J. Anderson, A.D. Koehler, C.R. Eddy, Jr., **D.I. Shahin**, K.D. Hobart, F.J. Kub, "A Tri-Layer PECVD SiN Passivation Process for Improved AlGaN/GaN HEMT Performance," *ECS Journal of Solid State Science and Technology* 6 [1], P58-P61 (2017). DOI: 10.1149/2.0231701jss.

9. T.J. Anderson, V.D. Wheeler, **D.I. Shahin**, M.J. Tadjer, A.D. Koehler, K.D. Hobart, A. Christou, F.J. Kub, C.R. Eddy, Jr., "Enhancement Mode AlGaN/GaN MOS High-Electron-Mobility Transistors with $ZrO_2$ Gate Dielectric Deposited by Atomic Layer

Deposition," *Applied Physics Express* 9 [7], 071003 (2016). DOI: 10.7567/APEX.9.071003.

10. (Editors' Choice) B.D. Weaver, T.J. Anderson, A.D. Koehler, J.D. Greenlee, J.K. Hite, **D.I. Shahin**, F.J. Kub, K.D. Hobart, "On the Radiation Tolerance of AlGaN/GaN HEMTs," *ECS Journal of Solid State Science and Technology* 5 [7], Q208-Q212 (2016). DOI: 10.1149/2.0281607jss.

11. **D.I. Shahin**, T.J. Anderson, V.D. Wheeler, M.J. Tadjer, A.D. Koehler, K.D. Hobart, C.R. Eddy, Jr., F.J. Kub, A. Christou, "Electrical and Thermal Stability of ALD-Deposited TiN Transition Metal Nitride Schottky Gates for AlGaN/GaN HEMTs," *ECS Journal of Solid State Science and Technology* 5 [7], Q204-Q207 (2016). DOI: 10.1149/2.0211607jss.

12. A.D. Koehler, T.J. Anderson, M.J. Tadjer, B.D. Weaver, J.D. Greenlee, **D.I. Shahin**, K.D. Hobart, F.J. Kub "Impact of Surface Passivation on the Dynamic ON-Resistance in Proton Irradiated AlGaN/GaN HEMTs," *IEEE Electron Device Letters* 37 [5], 545-548 (2016). DOI: 10.1109/LED.2016.2537050.

13. **D.I. Shahin**, T.J. Anderson, T.I. Feygelson, B.B Pate, V.D. Wheeler, J.D. Greenlee, J.K. Hite, M.J. Tadjer, A. Christou, K.D. Hobart, "Thermal etching of nanocrystalline diamond films," *Diamond and Related Materials* 59, 116-121 (2015). DOI: 10.1016/j.diamond.2015.09.017.

14. A.D. Koehler, T.J. Anderson, P. Specht, B.D. Weaver, J.D. Greenlee, **D.I. Shahin**, K.D. Hobart, F.J. Kub, M.J. Tadjer, "Radiation-Induced Defect Mechanisms in GaN HEMTs," *ECS Transactions* 69, 57-63 (2015). DOI: 10.1149/06911.0057ecst.

15. T.J. Anderson, K.D. Hobart, J.D. Greenlee, **D.I. Shahin**, A.D. Koehler, M.J. Tadjer, E.A. Imhoff, R.L. Myers-Ward, A. Christou, F.J. Kub, "UV detectors based on the graphene/SiC heterojunction," *Applied Physics Express* 8 [4], 041301 (2015). DOI: 10.7567/APEX.8.041301.

16. A. Christou, **D.I. Shahin**, "GaN/Si(111) Device Defects and Degradation Mechanisms," *ECS Transactions* 64 [7] 203 (2014). DOI: 10.1149/06407.0203ecst.

## A.2 Presentations

The following conference presentations were given in conjunction with this dissertation work:

1. **D.I. Shahin**, K.K. Kovi, A. Thapa, Y. Lu, I. Ponomarev, J.E. Butler, A. Christou, "Fabrication and Characterization of Diamond FETs with 2D Conducting Channels," 2018 International Workshop on Compound Semiconductor Manufacturing Technology, May 6-11, 2018, Austin, TX.

2. (Invited Presentation) **D.I. Shahin**, K.K. Kovi, A. Thapa, Y. Lu, I. Ponomarev, J.E. Butler, A. Christou, "Diamond Electronics with 2-D Transport Channel," 2018 Lawrence Symposium on Epitaxy, February 18-21, 2018, Scottsdale, AZ.

3. **D.I. Shahin**, K.K. Kovi, M. Yung, Y. Lu, A. Yuan, A. Auerbach, A. Thapa, I. Ponomarev, J.E. Butler, A. Christou, "Radiation Hardness of Hydrogen-Terminated Diamond Transistor and Diode Structures," 2017 Materials Research Society Fall Meeting and Exhibit, November 26-December 1, 2017, Boston, MA.

4. A.D. Koehler, T.J. Anderson, M.J. Tadjer, **D.I. Shahin**, V.D. Wheeler, K.D. Hobart, F.J. Kub, "Passivation and Gate Dielectrics to Enable High Performance AlGaN/GaN HEMTs with Low Dynamic On-Resistance, High Breakdown Voltage, and Enhancement Mode Operation," 2017 Materials Research Society Fall Meeting and Exhibit, November 26-December 1, 2017, Boston, MA.

5. (Invited Presentation) **D.I. Shahin**, T.J. Anderson, A. Christou, "Achieving Vertical Trench-Gate GaN MOSFETs Via Process Optimization," 232nd Electrochemical Society Meeting, October 1-6, 2017, National Harbor, MD.

6. V.D. Wheeler, T.J. Anderson, S. Ahn, **D.I. Shahin**, M.J. Tadjer, A.D. Koehler, K.D. Hobart, F. Ren, F.J. Kub, A. Christou, C.R. Eddy, Jr., "ALD TiN Schottky Gates for Improved Electrical and Thermal Stability in III-N Devices," 232nd Electrochemical Society Meeting, October 1-6, 2017, National Harbor, MD.

7. (Invited Presentation) **D.I. Shahin**, A. Christou, J.E. Butler, "High Power Diamond Devices with 2-D Transport Channels," 232nd Electrochemical Society Meeting, October 1-6, 2017, National Harbor, MD.

8. **D.I. Shahin**, M.J. Tadjer, V.D. Wheeler, A.D. Koehler, A. Christou, "Characterization of $ZrO_2$ and $HfO_2$ Dielectrics Deposited by Thermal ALD on $\beta$-$Ga_2O_3$ Substrates," 2nd International Workshop on Gallium Oxide and Related Materials, September 12-15, 2017, Parma, Italy.

9. **D.I. Shahin**, M.J. Tadjer, V.D. Wheeler, T.J. Anderson, A.D. Koehler, K.D. Hobart, C.R. Eddy, Jr., F.J. Kub, A. Christou, "Characterization of $ZrO_2$ and $HfO_2$ MOS Capacitors Deposited by ALD on (-201) $\beta$-$Ga_2O_3$ Substrates," 59th Electronic Materials Conference, June 28-30, 2017, South Bend, IN.

10. T.J. Anderson, V.D. Wheeler, **D.I. Shahin**, M.J. Tadjer, L.E. Luna, A.D. Koehler, K.D. Hobart, F.J. Kub, C.R. Eddy, Jr., "Normally-Off AlGaN/GaN MOS-HEMTs Using $ZrO_2$ Gate Dielectric with Tunable Charge," 231st Electrochemical Society Meeting, May 28-June 1, 2017, New Orleans, LA.

11. **D.I. Shahin**, T.J. Anderson, V.D. Wheeler, M.J. Tadjer, A. Christou, "ALD High-k $ZrO_2$ Dielectrics for Wide and Ultra-Wide Bandgap Semiconductor Devices," 2017 Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe, May 21-24, 2017, Las Palmas de Gran Canaria, Spain.

12. **D.I. Shahin**, T.J. Anderson, V.D. Wheeler. M.J. Tadjer, L.E. Luna, A.D. Koehler, K.D. Hobart, C.R. Eddy, Jr., F.J. Kub, A. Christou, "Characterization of ALD High-k Dielectrics in GaN and $Ga_2O_3$ Metal-Oxide-Semiconductor Systems," 2017 International Conf. on Compound Semiconductor Manufacturing Technology, May 22-25, 2017, Indian Wells, CA.

13. T.J. Anderson, V.D. Wheeler, **D.I. Shahin**, M.J. Tadjer, L.E. Luna, A.D. Koehler, K.D. Hobart, C.R. Eddy, Jr., F.J. Kub, "Threshold Voltage Control by Tuning Charge in $ZrO_2$ Gate Dielectrics for Normally-Off AlGaN/GaN MOS-HEMTs," 2017 International Conference on Compound Semiconductor Manufacturing Technology, May 22-25, 2017, Indian Wells, CA.

14. T. Anderson, V. Wheeler, M. Tadjer, A. Koehler, L. Luna, K. Hobart, F. Kub, C. Eddy, Jr., **D.I. Shahin**, "Enhancement Mode AlGaN/GaN MOS-HEMTs with $ZrO_2$ Gate Dielectric Deposited by Atomic Layer Deposition," GOMACTech 2017, March 20-23, 2017, Reno, NV.

15. A. Koehler, T. Anderson, M. Tadjer, B. Feigelson, K. Hobart, F. Kub, A. Nath, **D.I. Shahin**, "Mg-Implanted Vertical GaN Junction Barrier Schottky Diodes," GOMACTech 2017, March 20-23, 2017, Reno, NV.

16. M. Tadjer, T. Anderson, A. Koehler, C. Eddy, Jr., K. Hobart, F. Kub, **D.I. Shahin**, "An Optimized Tri-layer PECVD SiN Passivation Process for AlGaN/GaN HEMTs," GOMACTech 2017, March 20-23, 2017, Reno, NV.

17. C. Eddy, Jr., V. Wheeler, **D.I. Shahin**, T. Anderson, M. Tadjer, A. Koehler, K. Hobart, A. Christou, F. Kub, "$ZrO_2$ as a High-k Gate Dielectric for Enhancement-mode AlGaN/GaN MOS HEMTs," 44th Conference on the Physics and Chemistry of Surfaces, January 15-19, 2017, Santa Fe, NM.

18. **D.I. Shahin**, T.J. Anderson, V.D. Wheeler, M.J. Tadjer, L.E. Luna, A.D. Koehler, K.D. Hobart, C.R. Eddy, Jr., F.J. Kub, A. Christou, "Integration of $ZrO_2$ Dielectrics with Wide and Ultrawide Bandgap Semiconductors and Devices," 2016 International Semiconductor Device Research Symposium, December 7-9, 2016, Bethesda, MD.

19. A.D. Koehler, T.J. Anderson, M.J. Tadjer, B.N. Feigelson, K.D. Hobart, F.J. Kub, A. Nath, **D.I. Shahin**, "Vertical GaN Junction Barrier Schottky Diodes by Mg Implantation and Activation Annealing," 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications, November 7-9, 2016, Fayetteville, AR.

20. **D.I. Shahin**, T. Anderson, V. Wheeler, M. Tadjer, A. Koehler, K. Hobart, C. Eddy, Jr., F. Kub, A. Christou, "Electrical and Thermal Stability of ALD-TiN Schottky Gates for AlGaN/GaN HEMTs," American Vacuum Society 63rd International Symposium and Exhibition, November 6-11, 2016, Nashville, TN.

21. C. Eddy, Jr., C. English, V. Wheeler, **D.I. Shahin**, N. Garces, A. Nath, J. Hite, M. Mastro, T. Anderson, "Advances in High-k Dielectric Integration with Ga-polar and N-polar GaN," American Vacuum Society 63rd International Symposium and Exhibition, November 6-11, 2016, Nashville, TN.

22. (Invited Presentation) A. Christou, **D.I. Shahin**, "Vertical GaN High Voltage Transistors: Comparison with SiC Switches," 2016 Pacific Rim Meeting on Electrochemical and Solid-State Science, October 2-7, 2016, Honolulu, HI.

23. **D.I. Shahin**, T.J. Anderson, J.D. Greenlee, A.D. Koehler, V.D. Wheeler, M.J. Tadjer, T.I. Feygelson, B.B. Pate, J.K. Hite, K.D. Hobart, C.R. Eddy, Jr., F.J. Kub, A. Christou, "Reliability Assessment of Thermally-Stable Gate Materials for AlGaN/GaN HEMTs," 2016 International Conference on Compound Semiconductor Manufacturing Technology, May 16-19, 2016, Miami, FL.

24. A.D. Koehler, T.J. Anderson, M.J. Tadjer, B.D. Weaver, J.D. Greenlee, **D.I. Shahin**, K.D. Hobart, F.J. Kub, "Effect of Surface Passivation on Current Collapse of Proton-Irradiated AlGaN/GaN HEMTs," 2016 International Conference on Compound Semiconductor Manufacturing Technology, May 16-19, 2016, Miami, FL.

25. **D.I. Shahin**, T.J. Anderson, A. Christou, "Control of Surfaces and Interfaces for Achieving Vertically Integrated Power Electronics," 2016 Lawrence Symposium on Epitaxy, February 21-24, 2016.

26. **D.I. Shahin**, A. Christou, "Graphene Interconnects for Flexible Displays and High Voltage Power Devices/Components," Fall 2015 Center for Advanced Life Cycle Engineering Technical Review, October 20, 2015, College Park, MD.

27. (Invited Presentation) A.D. Koehler, T.J. Anderson, P. Specht, B.D. Weaver, J.D. Greenlee, **D.I. Shahin**, K.D. Hobart, F.J. Kub, M.J. Tadjer, "Radiation-Induced Defect Mechanisms in GaN HEMTs," 228th Electrochemical Society Meeting, October 11-16, 2015, Phoenix, AZ.

28. K. Shenai, A. Christou, **D.I. Shahin**, B. Raghothamachar, M. Dudley, "Material Defects and Reliability Issues in High Voltage 4H-SiC Power Devices," 2015 Reliability of Compound Semiconductors Workshop, May 18, 2015, Scottsdale, AZ.

29. A. Christou, **D.I. Shahin**, "GaN/Si(111) Device Defects and HFET Degradation Mechanisms," 2014 ECS and SMEQ Joint International Meeting, October 5-9, 2014, Cancun, Mexico.

## A.3 Patent Filings

The following patent has been awarded based on work contained in this dissertation:

1. T.J. Anderson, V.D. Wheeler, **D.I. Shahin**, A.D. Koehler, M.J. Tadjer, K.D. Hobart, F.J. Kub, "Metal Nitride Alloy Contact for Semiconductor," U.S. Patent No. 9,991,354 B2, June 5, 2018.

# Appendix B: Plasma Etch Recipes for GaN Trench-Gate Processing

The following processes were utilized for trench-gate etch experimentation on GaN epilayers, as detailed in Chapter 6.

Table B.1. Cl-based plasma process parameters for GaN etching in an Oxford PlasmaLab 100 system.

| Process | Gas Flow Rates | RIE/ICP Power | Pressure | Temperature |
|---|---|---|---|---|
| $Cl_2$/Ar ICP/RIE | 10 sccm/5 sccm | 40 W/150 W | 5 mTorr | 30 °C |
| $BCl_3/Cl_2$ ICP/RIE | 5 sccm/20 sccm | 20 W/100 W | 5 mTorr | 30 °C |
| $BCl_3/Cl_2$ RIE Only | 6 sccm/6 sccm | 15 W/0 W | 5 mTorr | 30 °C |

Table B.2. F-based photoresist-masked $SiO_2$ etch process in an Oxford PlasmaLab 100 system.

| Process | Gas Flow Rates | RIE/ICP Power | Pressure | Temperature |
|---|---|---|---|---|
| $C_4F_8$/He ICP/RIE | 10 sccm/10 sccm | 50 W/1400 W | 1 mTorr | 20 °C |

# Bibliography


[1] D. I. Shahin, M. J. Tadjer, V. D. Wheeler, A. D. Koehler, T. J. Anderson, C. R. Eddy, Jr., and A. Christou, "Electrical characterization of ALD $HfO_2$ high-k dielectrics on $(\bar{2}01)$ $\beta$-$Ga_2O_3$," *Applied Physics Letters*, vol. 112, p. 042107, 2018.

[2] D. I. Shahin, T. J. Anderson, and A. Christou, "(Invited) Achieving Vertical Trench-Gate GaN MOSFETs via Process Optimization," *ECS Transactions*, vol. 80, no. 7, pp. 139–145, 2017.

[3] D. I. Shahin, A. Christou, and J. E. Butler, "High Power Diamond Devices with 2-D Transport Channels," *ECS Transactions*, vol. 80, no. 7, pp. 197–201, 2017.

[4] D. I. Shahin, T. J. Anderson, V. D. Wheeler, M. J. Tadjer, A. D. Koehler, K. D. Hobart, C. R. Eddy, Jr., F. J. Kub, and A. Christou, "Electrical and Thermal Stability of ALD-Deposited TiN Transition Metal Nitride Schottky Gates for AlGaN/GaN HEMTs," *ECS Journal of Solid State Science and Technology*, vol. 5, no. 7, pp. Q204–Q207, 2016.

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