

ABSTRACT

Title of dissertation: **FUNDAMENTAL STUDIES OF TIN WHISKERING
IN MICROELECTRONICS FINISHES**

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Common electronics materials, such as tin, copper, steel, and brass, are ambient reactive under common use conditions, and as such are prone to corrosion. During the early 1940s, reports of failures due to electrical shorting of components caused by ‘whisker’ (i.e., filamentary surface protrusion) growth on many surface types – including the aforementioned metals – began to emerge. Lead alloying of tin (3-10% by weight, typically in the eutectic proportion) eliminated whiskering risk for decades, until the July 2006 adoption of the Restriction of Hazardous Substances (RoHS) directive was issued by the European Union. This directive, which has since been adopted by California and parts of China, severely restricted the use of lead (<1000 ppm) in all electrical and electronics equipment being placed on the EU market, imposing the need for developing reliable new “lead-free” alternatives to SnPb. In spite of the abundance of modern-day anecdotes chronicling whisker-related failures in satellites, nuclear power stations, missiles, pacemakers, and spacecraft navigation equipment, pure tin finishes are still increasingly being employed today, and the root cause(s) of tin whiskering remains elusive.

This work describes a series of structured experiments exploring the fundamental relationships between the incidence of tin whiskering (as dependent variable) and

numerous independent variables. These variables included deposition method (electroplating, electroless plating, template-based electrochemical synthesis, and various physical vapor deposition techniques, including resistive evaporation, electron beam evaporation, and sputtering), the inclusion of microparticles and organic contamination, the effects of sample geometry, and nanostructuring. Key findings pertain to correlations between sample geometry and whisker propensity, and also to the stress evolution across a series of 4"-diameter silicon wafers of varying thicknesses with respect to the degree of post-metallization whiskering. Regarding sample geometry, it was found that smaller, thinner substrates displayed a more rapid onset of whiskering immediately following metallization. Changes in wafer-level stress were not found to correlate with whiskering morphology (number, density, length) after 6 weeks of aging. This result points either to the irrelevance of macrostress in the substrate/film composite, or to a difference in whiskering mechanism for rigid substrates (whose stress gradient over time is significant) when compared with thinner, flexible substrates (whose stress is less variable with time). Organic contamination was found to have no appreciable effect when explicitly introduced. Furthermore, electron-beam evaporated films whiskered more readily than films deposited via electroplating from baths containing organic "brighteners." Beyond such findings, novel in themselves, our work is also unique in that we emphasize the "clean" deposition of tin (with chromium adhesion layers and copper underlayers) by vacuum-based physical vapor deposition, to circumvent the question of contamination entirely. By employing silicon substrates exclusively, we have distinguished ourselves from other works (which, for example, use copper coupons fabricated from rolled shim stock) because we have better sample-to-sample consistency in terms of material properties, machinability, and orientation.

**FUNDAMENTAL STUDIES OF TIN WHISKERING IN
MICROELECTRONICS FINISHES**

by

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DEDICATION

All of my life's achievements, including this dissertation, are dedicated principally to my father (my hero), Les, my mother, Althea, and my brother, John. Harry Charles has been my tireless mentor, co-advisor, and friend – I owe the completion of this project, and my character as a professional engineer, to his encouragement and support. Al Genis remains the inspiration behind all of my pursuits in this field, and his appraisal of my abilities has been the greatest gift of all to my career. Finally, I devote this work to Jose Gustavo Piñol Montañez, the love of my life, who holds equal share in all that I achieve.

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CHAPTER 1: INTRODUCTION

Problem Statement

“Tin (Sn) whiskers” are crystalline metallic ‘tendrils,’ or filamentary outgrowths, of tin which originate from electroplated or physical vapor deposited tin-containing surfaces (see Figure 1).

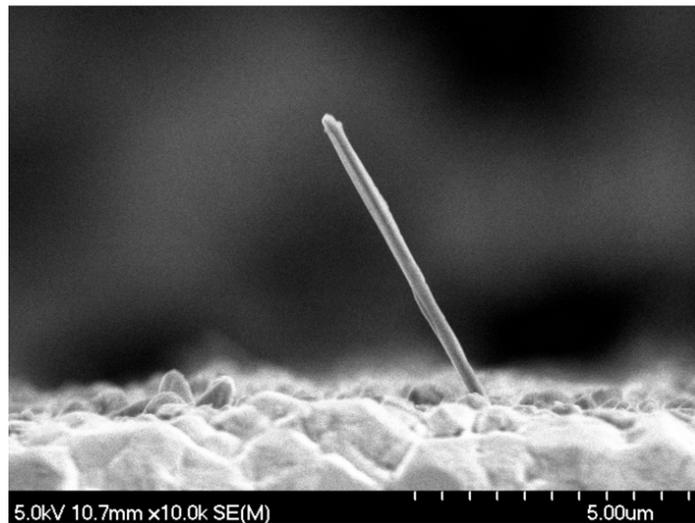


Figure 1: Tin Whisker on electron-beam evaporated Cu-Sn thin film (10,000x magnified)

Their reported sizes, growth rates, proliferation conditions, and morphologies have a wide range of reported values and properties, making them difficult to predict and, as a result, rather perplexing to study. Given that they are conductive, and also that they are capable of piercing through protective/conformal overcoats (nevermind that encapsulation is not always practical), tin whiskers pose a significant reliability problem to the electronics industry⁸³. For years, such risks were unimportant, given the almost exclusive use of tin-lead solder. The RoHS-driven resurgence of pure tin plating (and the corresponding certain, though gradual, elimination of lead as an option) has

renewed the commercial and scientific communities' interest in discovering the root cause of tin whisker growth, how best to prevent it, and/or how to minimize the risk of shorting if whiskers are inevitable.

Outreach & Collaboration

During the course of this research, I attended multiple conferences and workshops related to whiskering and RoHS transitioning, including:

- “Lead-Free Track” at the International Microelectronics and Packaging Symposium (IMAPS) in 2006
- “Lead-Free Solder Joint Reliability Workshop” by Jean-Paul Clech in May 2007
- NIST Workshop: Measurement of Stress in Sn and Sn Alloy Electrodeposits in April 2008
- CALCE Symposium on Part Reprocessing, Tin Whisker Mitigations, and Printed Wiring Assembly Rework/Repair in November 2008
- “Achieving High Reliability of Lead-Free Soldering – Materials Consideration” Professional Development Course by Ning-Cheng Lee (Indium Corporation of America) at ECTC 2009

Reports detailing what I learned at these events are also included in Appendices C, D, E, and F. I consulted with members of NIST's Metallurgical Division during several phases of this dissertation, including Maureen Williams, Bill Boettinger, Kil-Won Moon, Daniel Josell, and Gery Stafford. Each of these scientists have been very active in the area of tin whiskering, and were very

accommodating in offering me their advice and suggestions. I have also enjoyed a standing invitation to listen in on and/or participate in the recurring iNEMI Tin Whisker Team conference call, allowing me to regularly interface with several of the field's most recognized experts, including Richard Parker (Delphi), Tom Woodrow (Boeing), and Carol Handwerker (Purdue).

Review of Literature and Concepts

A thorough review of scholarly publications on the subject of tin whiskers leads to the following categorization: Fundamentals of Growth and Metallurgy, Anthologies and Case Studies, Theory/Modelling, and Mitigation. A discussion of each category is included in the following sections, with emphasis placed on the more significant papers and their contributions to the general understanding of tin whisker formation physics. It should be noted that, while much of the fundamental information presented therein is widely agreed upon and/or currently being researched, there exists in the field a resounding lack of consensus when it comes to a comprehensive picture of the tin whiskering phenomenon, its causes, and its remedies. This fact, coupled with the strong economic impetus for firms to successfully transition into RoHS adoption, makes the understanding and mitigation of tin whiskers critically important to the global electronics industry.

Fundamentals of Growth and Metallurgy

Whiskers (especially but not exclusively tin whiskers) pose risks to microelectronics reliability from multiple standpoints. They can cause soft and

hard electrical shorts, debris contamination, and ‘metal vapor arcing,’ a process by which high power conditions result in the vaporization of tin whiskers into a massively conductive and long-sustaining plasma. The emergence of one or more of these deleterious effects has in numerous documented cases been shown to destroy small electronics, medical devices, communications systems, munitions, and spacecraft. Public sources of fundamental and/or background information on tin whiskering are largely in agreement when it comes to generalized characteristics of whiskering, and also employ common language while describing those characteristics. To begin with, whiskers are widely defined as being “filamentary” protrusions, or “outgrowths” of crystalline metal emerging from a surface having that same metal within its composition (this is often presumed to be an *electroplated* surface, though not in every case). Distinct from dendrites, whose growth proceeds via metal ion dissolution in water and the subsequent application of an electric field, whiskers are believed to require *neither* such condition in order to form. Whiskers have been observed on tin, zinc, cadmium, iron, antimony, silver, indium, gold, lead, palladium, and nickel, individually, taking on a variety of trajectories, shapes, and surface textures. Their growth has been shown to commence after an “incubation period” which has been shown to last minutes, weeks, or decades, and to display rates ranging from <0.03 to 0.9 mm/year⁸¹. They may contain striations (see Figure 2) and/or kinks, and may be solid, hollow, or ‘perforated’⁵².

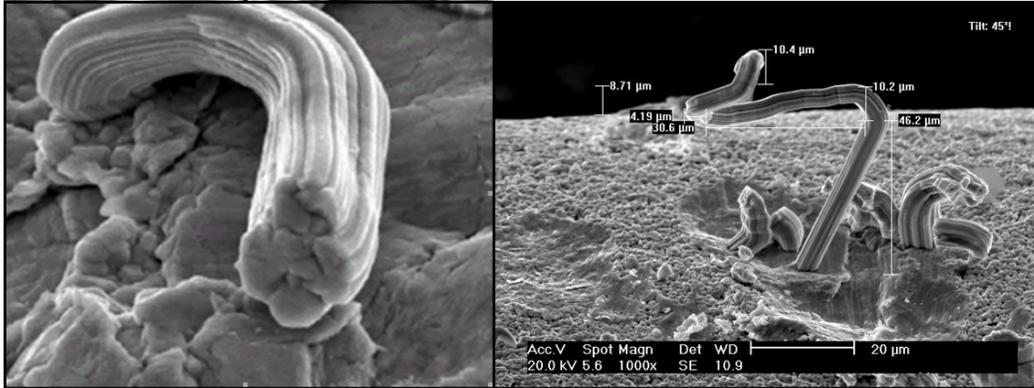


Figure 2: Striated and Bent Whiskers [SEM micrograph from Reference 87]

It is universally believed that stress (usually compressive stress) is the driving force behind whisker formation, and many sources elaborate that stress to be comprised of residual stresses due to plating, mechanically and thermally induced stresses, and the stress caused by solid state diffusion. Although a more complete examination of contending theories will be presented in the Theory and Modelling section, the bulleted list below provides a sampling of the more confident (and/or implied) claims encountered in the literature:

Whiskers DO grow...

- ◆ Spontaneously from pure electroplated Cd, Zn, Fe, Ni, and Sn.
- ◆ After incubation periods from seconds to decades.
- ◆ At accelerated rates with applied compressive force/stress.
- ◆ At higher incidence with applied compressive force/stress.
- ◆ Up to several millimeters in length.
- ◆ With diameters ranging from 6nm to 70 μm (1-5 μm typical).
- ◆ More readily from a 'bright' plating surface than from a 'matte' one.
- ◆ More readily when stress and/or diffusion is augmented.

- ◆ At typical growth rates of 0.1 angstrom/second (ambient, tin).
- ◆ At accelerated rates with Zn present in Cu substrates.
- ◆ From Sn on quartz with Cu underlay.
- ◆ From Al/Ag films when exposed to hydrogen sulfide (H₂S).
- ◆ Due to material being added at the *base* of the whisker
(not the tip).
- ◆ When an intermetallic compound (IMC) has formed between tin and the
substrate metal (though some research suggests that this is not a necessary
condition).
- ◆ From plated finishes whose grain structure is columnar.

Whiskers usually DO NOT grow...

- ◆ From Sn when alloyed with Pb (at 5% or greater).
- ◆ From Sn on quartz (*without* Cu underlay).
- ◆ When the ambient temperature exceeds 150°C.

Accepting as valid the premise that whisker formation is a stress relief mechanism^{13,29,31,39,42}, one may infer that the corresponding redistribution which is imposed upon the local lattice will effectively alter aspects of that material. When considering the role of crystallographic transformations leading to and/or occurring during whisker growth, it is critically important to identify and understand all of the germane materials science concepts. Although tin whiskers have been confirmed by x-ray diffraction to display single crystal ordering (tin

has a tetragonal structure), in practice the films from which whiskers grow may be polycrystalline and contain imperfections³⁷.

Disruptions to crystalline ordering are known as crystallographic defects, and they can manifest themselves as points (such as impurities, interstitials, and vacancies), lines (such as ‘dislocations’), planes (such as stacking faults), and three-dimensional groupings (known as ‘bulk’ defects). The presence of crystallographic defects necessarily implies that strength-related properties of the material have been altered. Dislocations, arising for example due to plastic deformation, may be of the ‘edge,’ ‘screw,’ or ‘mixed’ (i.e., both ‘edge’ and ‘screw’) type, and may in turn result in ‘slip’ (or ‘glide’), defined⁸⁵ as the “process by which plastic deformation is produced by a dislocation motion.” Slip is one of several processes by which a lattice may become further distorted, and it is most likely to occur “between planes containing the smallest Burgers vector.” The burgers vector is the vector signifying the magnitude and direction of the dislocation causing the relevant lattice deformation, and its orientation relative to that dislocation indicates the dislocation *type* (i.e., it will be *parallel* to a screw dislocation, but *orthogonal* to an edge dislocation). Naturally, a burgers vector will be a multiple of one of the translation vectors of the host lattice unless it corresponds to a *partial* dislocation. ‘Creep’ is the general term used to describe the irreversible migration of material in response to a stress, imposing a time-dependent deformation. ‘Climbing,’ a special case of creep, occurs when a lattice vacancy diffuses into the vicinity of a dislocation, allowing that dislocation to

move to another slip plane, thereby propagating through the crystal matrix and imparting additional deformations.

Stacking fault energy (SFE), or the energy associated with a two-dimensional discontinuity in crystalline ordering, is an influential factor relating to the motion of dislocations. SFE values for many materials have been experimentally determined using weak-beam transmission electron microscopy as well as x-ray diffraction. If a host material has sufficient stacking fault energy, the corresponding dislocation mobility will enable the spontaneous onset of a thermodynamically driven 'recrystallization' event. In such a circumstance, dislocations glide onto nearby slip planes and are able to traverse the lattice. They do so because sustainment of deformations is energetically inferior to recrystallization. During a recrystallization process, new grains nucleate from existing subgrains, incubate, and grow/merge until they have entirely replaced the deformed grains. An analogous process associated more specifically with the subgrains themselves, known as 'recovery,' also involves energy minimization, in this case via defect rearrangement or annihilation. In cases where full equilibration has not been achieved upon completion of both recovery and recrystallization, further evolution of the matrix can proceed via 'grain growth,' a lateral augmentation of grain size (and reduction in the number of grains), occurring most appreciably at "high temperatures." It should be noted that for some materials, including pure tin, room temperature is significant enough a fraction of the melting point that mechanisms such as creep and grain growth may

be observed. At room temperature, the homologous temperature of tin is 0.59, slightly lower than the SnPb value of 0.6535. (The homologous temperature is defined as the ratio of the ambient temperature to the melting point, both in Kelvin.)

Grain boundaries are the interfaces between metallic grains in a film or bulk material. The average (or local) grain size (i.e., distance between neighboring grain boundaries), a property which can be modified in terms of the plating conditions or of the deposition technique itself (explored in greater detail later), relates directly to the strength of a material via the yield stress, as defined by the Hall-Petch relationship:

$$\sigma_{\text{yield}} = \sigma_0 + \frac{k_y}{\sqrt{d}} \quad (\text{Equation 1.1})$$

where σ_{yield} is the yield stress, σ_0 is the starting stress, d is the average grain diameter, and k_y is a “fitting parameter”⁸⁷. It is partly the movement of high angle grain boundaries through a material which enables the recrystallization process to take place. Grain boundaries may be assigned mobilities which are dependent upon, among other things, their *degree* of misorientation (i.e., ‘high angle’ or ‘low angle’ boundaries, with the former having a generally higher mobility) and the temperature (likely because bulk diffusion plays a role). Because of its

temperature-dependent nature, boundary mobility (μ) is often described as having an Arrhenius-type behavior, i.e.:

$$\mu = \mu_0 \exp(-Q/RT) \text{ (Equation 1.2)}$$

where the prefactor (μ_0) and activation energies (Q) are often experimentally determined, R is the universal gas constant, and T is the temperature in Kelvin. There is also an energy associated with each boundary, as defined by the Read-Shockley equation:

$$\gamma_s = \gamma_0 \theta (A - \ln \theta) \text{ (Equation 1.3)}$$

where γ_s is boundary energy, θ is the degree of misorientation (ratio of Burgers vector to dislocation spacing), and:

$$\gamma_0 = G \cdot b / 4\pi(1-\nu) \text{ (Equation 1.4)}$$

and

$$A = 1 + \ln(b / 2\pi r_0) \text{ (Equation 1.5)}$$

where ν is Poisson's ratio, G is shear modulus, b is Burgers vector, and r_0 is the radius of dislocation concentration. The boundary energy, together with the

subgrain size (d_s), relates to the driving force approximation for metallurgical recrystallization as follows:

$$\Delta E \approx 3\gamma_s / d_s \text{ (Equation 1.6)}$$

All grain boundaries can become ‘Zener pinned’ by point defects and/or disruptions to the boundary plane, thereby preventing further lattice motion (other than localized bowing which results from forces exerted on uncompromised portions of the plane). If these particulates are widely distributed, however, they can actually lead to accelerated recrystallization instead; in fact, there is a transition from retardation to acceleration depending on the “f/d” ratio, i.e. the ratio of the volume fraction of particles to the average particle diameter²².

Anthologies and Case Studies

George Galyon of IBM has compiled several review articles on the chronology and theory of tin whiskering²⁸⁻³², which serve as excellent, systematic primers on the subject. In a comprehensive work²⁸ presented at SMTAI (Surface Mount Technology Association’s International Conference) in 2004, he characterized each decade between 1946 and 2004 in terms of its major relevant technological breakthroughs, as well as of the general climate of tin whisker inquiry during that period. The 1940s brought reports of some of the first known observances of whisker growth, on electroplatings of both cadmium and tin. The following decade saw a proliferation of fundamental research and publications, as

well as the implementation of many whisker “mitigation” practices still in use today. It was during this period that whiskers were first grown as single crystals, with augmentation occurring at the base/root, rather than the tip, an observation which gave rise to the publication of multiple dislocation-based explanations. The first of these came from J.D. Eshelby¹⁸, who supposed that a Frank-Read Source was involved, a type of dislocation amplification in which two ends of said dislocation have been pinned, leading to the emission of stress relief seeking dislocation ‘loops’ which emanate to slip planes and cause atomic migration along grain boundaries up to the surface. Other theories included mixed (i.e., edge and screw) and helical dislocations, in the latter case with climb playing a role as well. Galyon asserts in his anthology that all subsequent works on the subject are essentially offshoots of these few initial works. The prevailing modern-day opinion, he tells us, is that whisker growth is unrelated to lattice dislocations, an opinion first voiced by W.C. Ellis¹⁷, also in the 1950’s. He was the first to argue that ‘recrystallization’ might play a significant role, and that since whisker cross-sections have revealed some to be neither coherent with their base materials, nor coincident with expected glide directions, they cannot at all be explained by dislocations. Rounding out the 1950’s discussion was the seminal Fisher-Darken-Carroll²³ paper, in which tin-on-steel substrates were subjected to very large clamping forces, and *highly* accelerated whisker growth rates were observed. This work, verified in the subsequent literature by others, led to the widespread belief that compressive stress is what drives whisker growth.

During the 1960's, Russian experimenters found that zinc, when present in copper substrates (as in *brass* substrates), causes tin whiskers to grow more readily²⁸. They also expressed their concurrence with the Fisher-Darken Carroll results, as well as with the recrystallization hypothesis, and they were first to introduce the notion of annealing for whisker mitigation. Also active during this decade were S.C. Britton and M. Clarke of the International Tin Research Institute (ITRI), who published data on the effectiveness of underlayers of nickel and copper on brass substrates, as a means for mitigating the migration of zinc into the superficial tin matrix. Their findings were mixed, depending on the brightness of the tin electrodeposits. When Cu and/or Zn atoms were able to migrate to the tin surface, whiskering would occur. Though they were, at the time, many years from having the capability to image such a phenomenon, they *were* able to electrochemically measure (correctly) that the intermetallic incidence at the substrate surface was 'island'-like, rather than contiguous²⁸. The 1970's brought at least two particularly notable works which continue to influence tin whisker research today, namely U. Lindborg's zinc study⁵⁰ which concluded, via x-ray stress analysis, that micro-stresses (i.e., those due to dislocations and impurities) are unrelated the incidence of zinc whisker growth, and K.N. Tu's first paper (of many) in which he found whiskers to grow from tin on quartz *only* with an intermediate copper layer. In the latter work, Tu postulated that IMC formation is critical to whisker growth.

In Reference 27, Galyon combines the accomplishments of the 1980's and 1990's into a single section, as they are few in number. An interesting European

Space Center paper, published in 1987, asserted that mechanical stresses did **not** accelerate whisker growth in their samples. The experimental setup did not involve macro-compression (i.e., the pressing of two surfaces together), but rather investigated the whiskering impact of a thin tin film which had been electroplated onto a surface and was bent into tension and/or compression (via a C-shaped ring). Galyon interjects that this result may be due to their configuration, i.e. their technique does not lead to a direct ‘extrusion’ of tin. Rather, he says, their experiment involved relatively small (‘micro’) stresses, without assisting recrystallization (as had been surmised in Fisher, et al.). In 1998, Tu became the first to propose that whiskers may grow through cracks in weak oxide, a premise which is still being explored today. Lee & Lee⁴⁷ published groundbreaking data on cantilever beam stress measurements, employing the Complex Stoney’s equation (the application of which requires that the non-alloyed tin be etched away) to demonstrate that annealed films were stress-free. They also presented electron beam diffraction results which demonstrated that whisker orientations differed from those of their host grain(s).

Not surprisingly, the present decade has produced an extremely high volume of scholarly publications on the subject of whiskering, to a degree which dwarfs the previous six. Motivations for such a dramatic increase naturally stem from the electronics industry’s need to respond to the RoHS directive, and such modern research efforts are enhanced by the comparatively high level of technological sophistication which is reasonably accessible to industry players. Chief among these technologies is certainly focused ion beam (FIB) milling;

when coupled with scanning electron beam (SEM) imaging, FIB provides a highly controlled and informative means by which to planarize surfaces of interest (i.e., cross-sections of whiskered films) and to make morphological observations at a snapshot in the film's evolutionary life. Dr. Galyon mentions the first FIB work in 2001, by Zhang et al., which led the authors to agree that nickel underlays were an effective means of whisker mitigation, perhaps due to the fact that Sn diffuses more readily into nickel, while in the absence of nickel, copper will diffuse unimpeded into tin. Also described in Galyon's anthology were the developments of various research groups and consortia dedicated to the cause of ending whiskers, and also to the emergence of a discussion on the role of stress *gradients* in as-plated films (i.e., as measured by micro-x-ray analysis). Galyon closes with an overview of his own "Integrated Theory" of whiskering, in which he provides the following (summarized) criteria:

"1. Whiskers do not grow from as-plated microstructures...

a "different" whisker grain must be formed.

2. Whisker grains are formed by recrystallization events.

Recrystallization events are driven by macro - and/or
micro -stresses within the film.

3. Tin atoms are transported to the whisker grain through a

grain boundary network that connects the whisker grain
with the film / substrate interface region.

4. The driving force for tin transport is a positive stress gradient...not a compressive stress state.

5. Intermetallic formation at the substrate interface generates very high compressive stresses in the intermetallic region.
The intermetallic region is always a combination of intermetallic and unreacted/displaced tin atoms.

6. The unbalanced inter-diffusion of copper and tin results in a Kirkendall effect with a vacancy-rich zone within the copper substrate in the vicinity of the film/substrate interface.

7. The Kirkendall zone within the copper substrate results in a shrinkage effect that establishes a tensile stress state in the Kirkendall zone.

8. Dislocation mechanisms are probably not relevant to whisker growth. Tin atoms can move into the whisker grain from the whisker grain boundaries by diffusion and thereby lift the whisker grain surface so as to grow a filamentary whisker.”²⁸

In a 1993 work featured at the IEEE Aerospace Applications Conference, CPT Mark E. McDowell related the U.S. Air Force’s understanding of the tin whisker problem as well as their rationale when making reliability-based decisions about plating finishes⁵². He reported that, at the time, there were ~50

military specification (MIL-SPEC) documents which still permitted the use of pure tin. It was the Air Force's belief that whiskers primarily emerged from surface "nodules," in keeping with the published opinion that the shape and/or proximity of such nodules is a deciding factor in the morphology of the coincident whiskers. CPT McDowell's paper speculates that whiskers must form due to a long-distance diffusion process, since there is no observable localized thinning of the tin beneath heavily whiskered regions. He also observed the lack of agreement in the literature regarding the strength of whiskers (i.e., whether they are difficult to break or whether they are prone to breaking), as well as whether slower growth or faster growth correlates with higher dormancy.

Theory/Modelling

As evidenced by the proliferation of academic inquiry into tin whiskering over the past several decades, there has been a sustained effort within industrial and academic venues to identify a comprehensive theory to explain the phenomenon. Many such attempts can be described as including at least one of the following factors: plating stresses, applied stresses (microscale and macroscale), intermetallic growth, CTE mismatch, crystallographic defects, recrystallization, grain growth, creep, the presence of a native oxide and/or imperfections therein, and mechanical deformations. The claims presented in Table 1 below illustrate the widespread lack of agreement on any single given theory.

Primary Theory	Counter Claim
Whiskers grow when dislocations migrate to the film surface, dropping off atoms. -Dislocation loops emitted from a Frank-Read source -Edge dislocations stuck to screw dislocations -Helical "climbing" dislocations ^{47,23,17}	Dislocation Theory cannot be correct since: -Whisker roots aren't always coherent with the film grains -"Kinking" would not occur with dislocated atoms -Not all whisker growth directions match up with possible dislocation glide planes ¹⁷
Whisker Growth is a special case of recrystallization ¹⁷	No counter-claim exists
Whisker growth is independent of micro-stresses (which are due to crystallographic defects) in Zn on steel ⁵⁰	Lindborg's x-ray stress mapping has never been repeated, and so this result has never been confirmed.
Whiskers grow due to stresses which arise when copper-tin intermetallics form ^{11,42,64}	Whisker growth can be prevented by copper as an interlayer between matte Sn and brass (Cu + Zn). ⁸
Whisker formation is accelerated when a Sn sample is mechanically stressed (direct clamp). ³³	European Space Agency says that stress has no effect (C-clamp). ²⁸
Aluminum electromigration can cause hillock and whisker growth at grain boundaries. ²⁸	Electromigration is irrelevant to tin whiskering, as whiskering has been observed to occur in the absence of both current and moisture. ²
Whiskers grow through cracks in a weak or compromised surface oxide layer. ^{37,47}	Whiskers grow in the absence of SnO _x . ²
Whisker growth occurs via simple mass transport (i.e., diffusion). ²³	Whisker growth occurs via a combination of mechanisms, which may or may not include ordinary diffusion.
Whisker growth relieves biaxial (i.e., at grain boundaries) compressive stresses built up in a film due to excessive intermetallic (Cu ₆ Sn ₅) formation through a large number of grain boundaries (i.e., smaller grains are worse). ⁴⁴	A NIST study revealed hillock formation in films where a tungsten diffusion barrier separates the copper layer from the tin layer, suggesting that intermetallic compounds are not required for whisker formation. ⁷³
Whiskers grow when the following three conditions are present: 1. Fast atomic diffusion at room temperature 2. Compressive stress driving force (mechanical, thermal, and chemical) 3. Protective surface oxide (to confine, and also to induce a stress gradient)	Mechanical compressive stresses have been ruled out by some, micro-stresses by others, and surface oxides by still others!

Table 1: A Summary of Popular Whiskering Theories and Counter Claims

Mitigation

Whisker mitigation practices approved by the International Electronics manufacturing Initiative (iNEMI) Tin Whisker User Group can be viewed at: http://www.inemi.org/cms/projects/ese/tin_whisker_usergroup.html. As of January 25th, 2010, the approved technologies were described as follows:

“Mitigation practices recommended by the User Group include: use of nickel-palladium or nickel-palladium-gold instead of tin; use of a nickel underlay; annealing/heat treatment (150°C for one hour) of matte tin within a short time after plating; use of a hot dip tin or tin alloy finish rather than plating (SnAgCu is the preferred alloy); and fusing (reflow above 232°C) by the tin plating supplier within a short time after plating.”

Common techniques advocated and/or employed for mitigating tin whisker growth, as reported in the literature, include one or more of the following:

- ◆ ALLOYING WITH LEAD (3-10% by weight)²
- ◆ FUSING/REFLOW⁷
- ◆ HOT-DIPPING⁵²
- ◆ ANNEALING (150-200°C, in nitrogen)⁸¹
- ◆ UNDERLAYING (i.e., for tin on brass: Cu for matte Sn and Ni for bright Sn are suggested)⁶⁰
- ◆ ORGANIC ENCAPSULATION/CONFORMAL COATING (mitigates shorting, not formation of whiskers)⁷

- ◆ INCREASING Sn THICKNESS (8 μ m or greater if not flow melted)¹⁵
- ◆ USE OF ALTERNATIVE MATERIALS:

Criteria	Sn	SnBi	SnCu	SnAg	Au flash/PdNi	Au flash/Pd
Solderability	OK	OK	OK	OK	OK	OK
Solder Joint Reliability	OK	SnPbBi reliability ³	OK	Not tested	OK	OK
Tin Whisker Susceptibility	Slightly higher risk ¹	Slightly higher risk ¹	Significant Risk ²	Slightly higher risk ¹	No whisker risk	No whisker risk
SnPb and Pb-free Process	OK	SnPbBi reliability ³	OK	Not tested	OK	OK
Contact Resistance	OK	OK	OK	Not tested	OK	OK
Fretting Resistance	OK	OK	OK	Not tested	Better than SnPb	Better than SnPb
Coefficient of Friction	OK	OK	OK	Not tested	OK	OK
Plating Process	Easier than SnPb	Difficult ⁴	Difficult ⁴	Very Difficult ⁵	OK	OK
Scrap Value	OK	Bismuth content ⁶	OK	OK	OK	OK
Cost	OK	OK	OK	Expensive	Very Expensive	Very Expensive

Table 2: Comparison of SnPb ‘Alternative’ Plating Materials⁹⁰

It is the preliminary opinion of this author that whisker growth occurs due to a combination of recrystallization and grain growth. The former is believed likely to play a dominant role in whisker formation, particularly when considering that (upon completion of an initial nucleation stage) recrystallization proceeds as a site-specific, *saturation* type growth process. The relatively weak driving force behind recrystallization, which can be accelerated or slowed based on the prevalence and geometry of foreign particulates, may help to explain the occasional ‘unusually long’ incubation periods. Furthermore, the grain boundary ‘pinning’ which results from higher particulate densities may have the effect of

translating what might have been lateral grain growth into vertical grain growth, once the recrystallization and recovery mechanisms have been fully realized. On the other hand, a specific means of grain boundary pinning, known to metallurgists as ‘Zener pinning,’ involves incorporation of a fine dispersion of particulates into a material for purposes of *retarding* the recrystallization process. Incorporating foreign particles of a properly engineered morphology might also prolong the crystallization step (an effect known as “continuous recrystallization”) and/or contribute additional relaxation surfaces to the end of relieving the stress precursors to whiskers. Investigating the consequences of such a treatment on a variety of substrates, and for a variety of *types* of tin plating finishes (including SnZn and potentially other alloys) may aid in proving or disproving the recrystallization hypothesis.

CHAPTER 2: EXPERIMENTATION

PHASE I: Substrate Preparation

Early in this work, it was presumed (based on numerous reports in the literature as well as on iNEMI endorsement) that substrates chemically machined from rolled copper shim stock, in the geometry outlined below, would be ideal test structures for tin whisker studies, given that (as in most solderable electronics applications) the metallization underlayer would be comprised of copper, and also that cantilevered structures were widely believed to be useful gauges of “as-plated” film stresses, via the uncompensated Stoney equation. In preparation for the test coupon fabrication, samples of several thicknesses of copper shim stock were submitted to the JHUAPL sheet metal shop for rolling/flattening. Artwork for the production of the flexure beam stress testing coupons was generated by W. Johnston in the Board Fabrication area at the Applied Physics Laboratory, and a checkplot rendering of the geometry is presented in Figure 3 below:

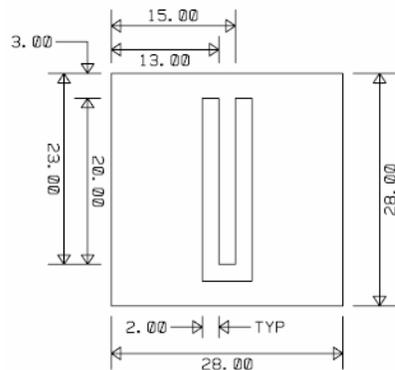


Figure 3: Flexure Beam Coupon Geometry

Dry-film photolithographic processing was carried out according to the following process steps:

1. Hand cleaning of copper surfaces with Microscrub cleanser
2. Deionized water rinse
3. Heated solvent soaks (5 minutes in acetone, 3 minutes in isopropyl alcohol)
4. Deionized water rinse, dry nitrogen blowoff
5. Oven pre-heating of copper shim stock to 90°C (~5 minutes)
6. Lamination of dry film onto shim stock
7. Exposure of cantilever beam pattern in double-sided UV table
8. Tank develop
9. Deionized water rinse, dry nitrogen blowoff
10. Double-sided pattern etch in ferric chloride
11. Deionized water rinse, dry nitrogen blowoff



Figure 4: Flex Beam Structure Etching



Figure 5: Completed Flex Beams (detail)

Numerous issues arose pertaining to the viability of these larger copper cantilevered structures, particularly the difficulty in achieving an acceptable

tradeoff between how “thin” the coupons could be while retaining planarity (indeed, achieving planarity *prior* to micromachining was also impractical for the lower thickness range) and the ability to obtain flexure in the central beam. Furthermore, discussions with colleagues at NIST, including Bill Boettinger and Maureen Williams, suggested that any attempts to employ the Stoney equation for stress calculations using rolled copper stock would be error-prone if the “roll *direction*” (or absolute orientation to it) was not also taken into consideration. Based on these manufacturing and analytical complications, we chose to migrate our experiments to an alternative substrate material and geometry. We selected silicon for our new base material, based on its maturity (from a materials science standpoint), the availability of supplies, and the ease of machining. We scaled down the geometry of the test sample to allow for the higher throughput of samples, as well as to enhance the sensitivity of the flexure beam appendages. A checkplot illustrating the dimensions of our modified, smaller test die, along with photographs of the microfabricated die, are shown in Figures 6 and 7 below. The microfabrication was accomplished using deep reactive ion etching of the arrayed pattern shown (emulsion photoplotted artwork and negative-working Futurrex NR5-8000 resist were used).

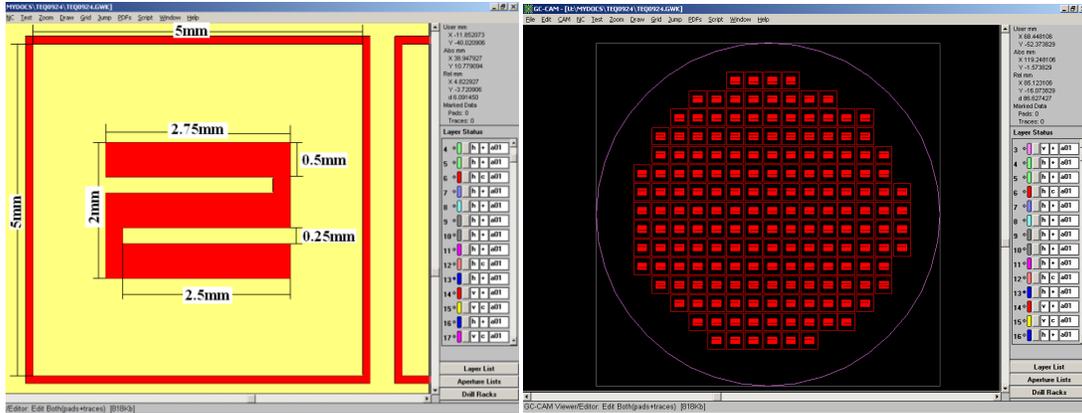


Figure 6: Modified Silicon Test Die Geometry



Figure 7: Microfabricated Silicon Test Die

PHASE II: Substrate Metallization (Thin Film Deposition)

A. Plating

All plating experiments were performed on the 100-micron thick silicon test die structures described above, with an electron-beam evaporated seed layer of 300 angstroms of chromium (to aid in adhesion) followed by 2,500 angstroms of copper. The silicon parameters for all plating experiments are included in Table 3 below.

(1) Techni-Matte Tin Sulfate 89T

Electroplating of tin was performed using the Techni-Matte Tin Sulfate 89T formulation, a bath containing stannous sulfate and sulfuric acid. Samples were solvent rinsed prior to plating, and dipped

in ammonium hydroxide for 30 seconds afterwards. One sample was plated for 10 minutes, another for around 96 minutes.

(2) Datak Tinnit Electroless

Electroless plating of tin was performed using Datak “Tinnit” acid-based plating solution. Samples were solvent rinsed prior to deposition, and dipped in ammonium hydroxide for 30 seconds afterwards. The sample received 20 minutes of deposition (with agitation every 5 minutes) at a bath temperature of 55°C.

(3) Techni Bright Acid Tin

Electroplating of tin was performed using the Techni Bright Acid Tin formulation, a bath containing stannous sulfate, sulfuric acid, a proprietary brightener, and an antioxidant. Samples were acid pre-cleaned in LAC-81 for 5 minutes at 60°C and then dipped in sulfuric acid prior to plating. No post-plating treatment was performed. One sample was plated for 10 minutes, another for around 96 minutes.

Sample Name	Sample Shape	Substrate	Type	Resistivity	Thick or Thin Si?	Big or Small Die?	Deposition Type	Surface Prep	Plating Composition (if applicable)	Deposition End	Deposition Conditions	Post Processing	Aging Temperature	RESULTS
LE1	Beam Pattern	100um Si • 300A Cr • 2500A Cu	N	"0.005-0.02"	Thin	Small	Electroplating	solvent rinse	Techni Matte Tin Sulfate 89T (stannous sulfate • H2SO4)	10 minutes	RT, agitation	Ammonium Hydroxide dip, 30 seconds	32	whiskers
LE2	Beam Pattern	100um Si • 300A Cr • 2500A Cu	N	"0.005-0.02"	Thin	Small	Electroless Plating	solvent rinse	Datak Tinnit Electroless (acid-based)	20 minutes	55C, agitation every 5 minutes	Ammonium Hydroxide dip, 30 seconds	32	whiskers
LE3	Beam Pattern	100um Si • 300A Cr • 2500A Cu	N	"0.005-0.02"	Thin	Small	Electroplating	solvent rinse	Techni Matte Tin Sulfate 89T (stannous sulfate • H2SO4)	96.14 min (7.98 A*min)	RT, agitation	Ammonium Hydroxide dip, 30 seconds	32	no whiskers
LE4	Beam Pattern	100um Si • 300A Cr • 2500A Cu	N	"0.005-0.02"	Thin	Small	Electroplating	LAC-81, 10% sulfuric dip	Techni Bright Acid Tin (stannous sulfate • H2SO4 • brightener • antioxidant)	33.85 min (2.81 A*min)	RT, agitation	Ammonium Hydroxide dip, 30 seconds	32	no whiskers
LE5	Beam Pattern	100um Si • 300A Cr • 2500A Cu	N	"0.005-0.02"	Thin	Small	Electroplating	LAC-81, 10% sulfuric dip	Techni Bright Acid Tin (stannous sulfate • H2SO4 • brightener • antioxidant)	96 minutes	RT, agitation	Ammonium Hydroxide dip, 30 seconds	32	no whiskers
LE6	Beam Pattern	100um Si, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	HF dip	NA	~2.7 microns QCM	P=6.9e-7T, 33% Power, 5 A/sec, -8.09kV, -0.046A emission current	none	32	no whiskers
LE7	Beam Pattern	100um Si	N	"0.005-0.02"	Thin	Small	Resistive Evaporation	HF dip	NA	600nm QCM	P=5.0e-8MB, 37% Power, ~0.94nm/sec	none	32	no whiskers
LE8	Beam Pattern	100um Si	N	"0.005-0.02"	Thin	Small	DC Sputtering	HF dip	NA	31 minutes	P=2.3e-7T, prep 30sec @ 500V, sputter 31min @ 800V (1.2A, 613TV, 25.7sccm Ar)	none	32	no whiskers
LE9	Beam Pattern	100um Si • 300A Cr • 2500A Cu	N	"0.005-0.02"	Thin	Small	Electroplating	LAC-81, 10% sulfuric dip	NA				32	no whiskers

Table 3: Deposition Experiments Datalog

B. Physical Vapor Deposition (PVD)

All PVD experiments were performed on the 100-micron thick silicon test die structures described above, with an electron-beam evaporated seed layer of 300 angstroms of chromium (to aid in adhesion) followed by 2,500 angstroms of copper. The silicon parameters for all PVD experiments are included in Table 3 below.

(1) Electron Beam Evaporation

E-beam evaporation was carried out in a CHA evaporation system, with cryogenic pumping. Typical vacuum levels at the start of depositions were $\sim 2.5 \times 10^{-6}$ Torr or better. Deposition rate and thickness were determined using a quartz crystal monitor located in the bell jar center, directly above the substrate planetary.

(2) Resistive/Thermal Evaporation

Resistive evaporation was carried out in a BOC/Edwards Auto 306 resistive evaporator system, with oil diffusion pumping. Typical vacuum levels at the start of depositions were $\sim 4.0 \times 10^{-6}$ Torr. Deposition rate and thickness were determined using a quartz crystal monitor located in the bell jar, oblique to the evaporant path.

(3) DC Sputtering

Direct current sputtering was carried out in a Denton Discovery confocal sputtering system, with cryogenic pumping. Typical vacuum levels at the start of depositions were $\sim 2.5 \times 10^{-6}$ Torr. Deposition rate

and thickness were empirically determined via a series of calibration runs.

PHASE III: Experimental Subsets

A. Deposition Type

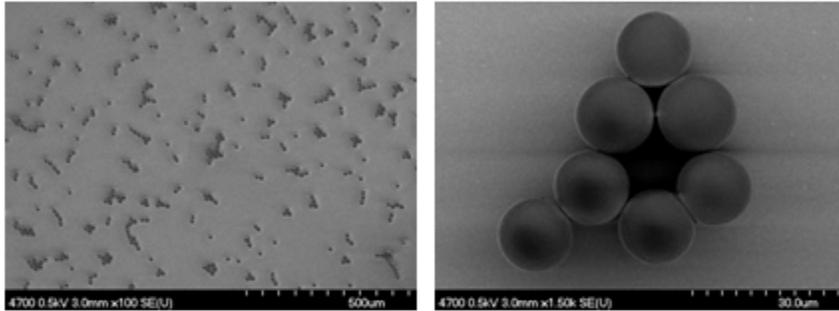
In consideration of the pervasive argument that plating bath contamination may contribute to the incidence of whiskers, we elected to evaluate the effects of deposition type on the morphology and whiskering propensity of as-fabricated, as well as “aged,” films. The processing parameters involved with each deposition technique were described and tabulated in the Phase II subsection above. In each case, a chromium ‘adhesion’ layer was applied to the bare silicon surface, followed by a copper interlayer (to mimic standard printed wiring board metallurgy, and to allow for the creation of the notorious copper-tin “intermetallic” compound widely believed to contribute stresses which are critical to tin whisker formation), and finally by a top surface of pure tin. By including a series of high-vacuum, high-purity deposition processes (i.e., electron beam evaporation, resistive evaporation, and sputtering), we were able to make whisker character comparisons between “clean” (contaminant-free) samples and those which had been plated (including some with proprietary, though assuredly organic, ‘brightener’ components). Several authors in this field have made claims regarding the whiskering propensity of “matte” tin compared with “bright” tin (divergence of opinion exists here as well), however we are aware of no other work that so fully considers the means of tin deposition within the context of lead-free reliability, nor have we found any study on PVD tin whiskering.

B. Microparticles

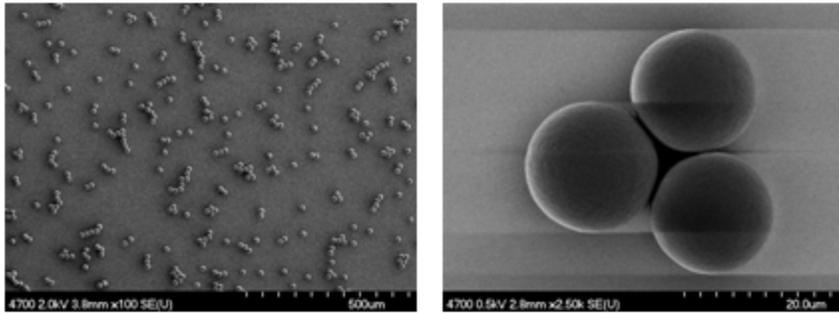
In an effort to explore the mitigation approach described earlier, in which stress “relaxation surfaces” are presented to the tin film matrix in the form of chemically inert particles, two particle types were selected. The first was a cross-linked polystyrene (carboxyl type) microbead, having a mean diameter of 15.2 microns, and the second was a cross-linked polystyrene (amino type) microbead, having a mean diameter of 2.48 microns. Both particle types are commercially available from Spherotech, Inc. (Lake Forest, IL, part numbers CPX-150-10 and APX-20-10, respectively). Cross-linked polystyrene was selected because of its inertness, its ability to be adhered onto smooth surfaces, and its ability to withstand elevated temperatures and flow “in place” without permanently deforming. The figures below show SEM images of the results of various attempts at adhering the particles to bare silicon surfaces by:

- Spincoating (20 seconds spread at 1krpm, 40 seconds spin at 2krpm)
- Spincoating + hotplate baking at 100°C for 60 seconds
- Spincoating + dipping in boiling water for 60 seconds.

P1: Carboxyl Polystyrene, 15.2 microns in diameter
Spincoated (20s at 1krpm, 40s at 2krpm)



P2: Carboxyl Polystyrene, 15.2 microns in diameter
Spincoated (20s at 1krpm, 40s at 2krpm), Hotplate Bake at 100°C for 60s



P3: Carboxyl Polystyrene, 15.2 microns in diameter
Spincoated (20s at 1krpm, 40s at 2krpm), Dipped in Boiling DI Water for 60s

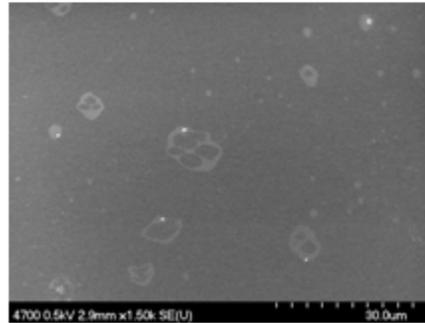
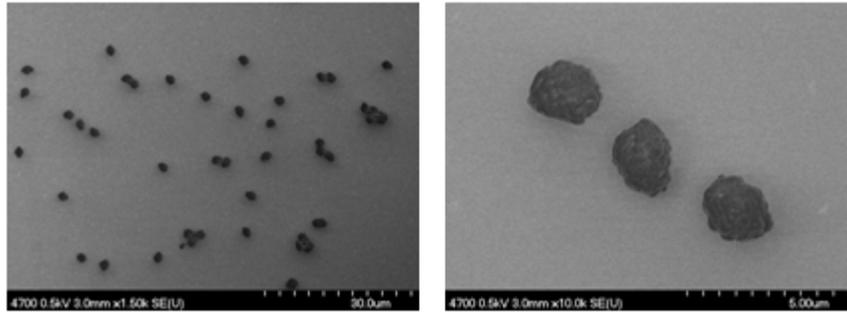
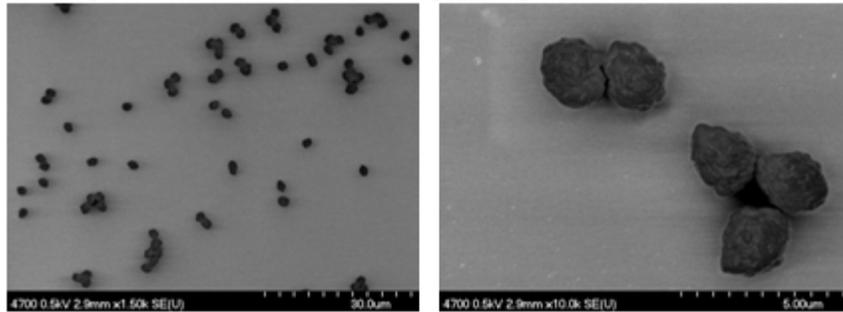


Figure 8: Carboxyl Polystyrene Microparticle Adhesion Tests

P4: Amino Polystyrene, 2.48 microns in diameter
Spincoated (20s at 1krpm, 40s at 2krpm)



P5: Amino Polystyrene, 2.48 microns in diameter
Spincoated (20s at 1krpm, 40s at 2krpm), Hotplate Bake at 100°C for 60s



P6: Amino Polystyrene, 2.48 microns in diameter
Spincoated (20s at 1krpm, 40s at 2krpm), Dipped in Boiling DI Water for 60s

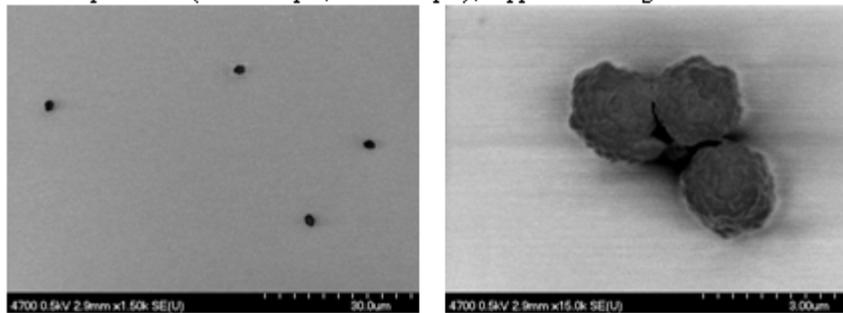


Figure 9: Amino Polystyrene Microparticle Adhesion Tests

C. Organic Contamination (Surface, Buried)

To study the question of organic contamination's role in tin whiskering, certain samples were "treated" with AZ9240 photopolymer (diluted with acetone to aid with application), applied with a fine-bristled paintbrush either prior to metallization or afterwards (to the plated surface).

D. Geometric Studies

Over the course of experimentation and inspection related to experimental trials A through C, we began to suspect a general relationship between sample geometry (size and/or shape) and the whiskering result, both with and without aging. As such, a new experimental trial was conceived in which we sought to compare a vast array of die sizes and silicon host wafer thicknesses. A costly assortment of custom-prepared silicon wafers were acquired for this purpose, and careful DRIE-based die fabrication was performed (sample handling was particularly emphasized during this phase, given the fragility and short supply of expensive materials).

E. Tin Nanowires

In the spirit of experimental subset D, we became interested in investigating the effect of tin nanostructuring on its tendency to spontaneously whisker. An electrochemical, template-based synthesis of tin nanowires was performed using Whatman “Anodisc” filter membranes with nominal pore diameters of ~200 nanometers. The plating solution was Techni Bright Acid Tin (stannous sulfate + sulfuric acid + brightener + antioxidant). Electrochemical analysis was performed on a CHI760 (CH Instruments) analyzer. Cyclic voltammogram (CV) and chronocoulombetric (CC) plots for the tin nanowire electrodeposition are presented in Figure 10 below. Characteristic deposition and dissolution peaks were observed at -60mV and +90mV, respectively. The

potential sweep covered a range from -75mV to -60mV over the course of the deposition, and the total accumulated charge transferred was 1.658 coulombs.

This corresponds to an expected nanowire length of ~2.22 microns, as calculated in Figure 11 below.

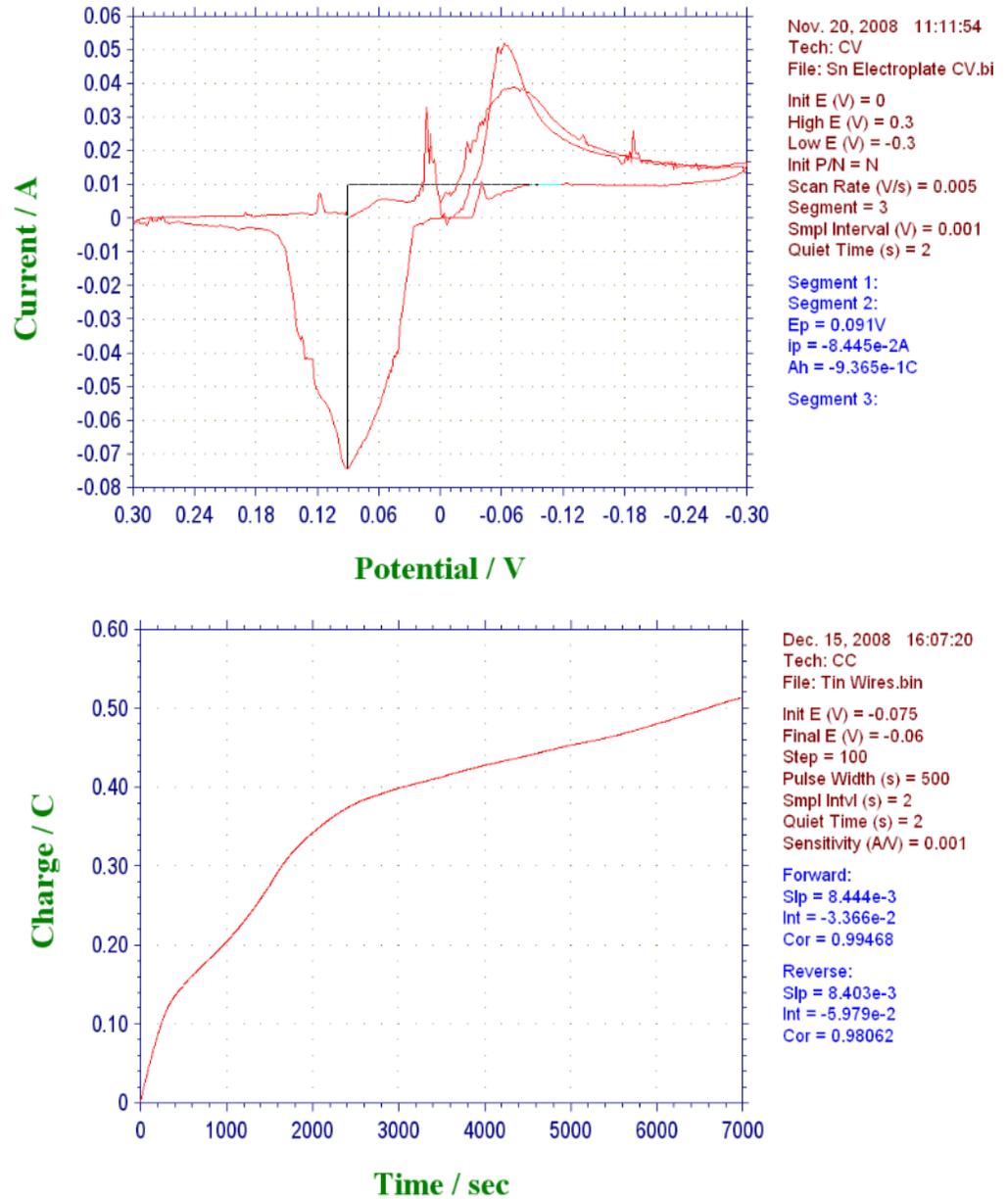


Figure 10: Cyclic Voltammetry and Chronocoulombetric Plots for Tin Nanowire Electrodeposition

CALCULATION	RESULT
Single Pore Volume (200nm pore diameter)	6.28e-12 cm ³
Total Volume, 50% Porosity across 1.267cm ² area	6.3e-3 cm ³
Mass of Tin Needed to completely fill membrane	0.045913633 grams
Mass of Tin Needed for 1.5-micron length	0.001377409 grams
Molar Mass of Tin	118.69 g/mol
Number of Moles of Tin Needed	1.1605e-5 moles
Amount of Charge Transfer Needed (Faraday's Constant * Number of Moles of Tin Needed)	1.119721774 Coulombs

Figure 11: Charge Calculations for Tin Nanowire Electrodeposition in Anodisc Membranes (200nm pore diameter, 1.5um length)

PHASE IV: Whisker Documentation (Microscopy)

A. Deposition Type

There are marked differences among the samples whose deposition technique was varied. Whiskering results immediately following the initial tin deposit were included in Table 3 above. At age “zero,” only the thin matte electroplated and electroless plated samples had grown whiskers. After 61 weeks of aging, whisker onset “ages” (see Table 4 below) have been determined for several of the samples. Whiskering has yet to occur on the thin bright electroplated sample, nor has any whiskering occurred on the e-beam evaporated, resistively evaporated, and sputtered tin films on bare silicon (no underlayers of Cr or Cu).

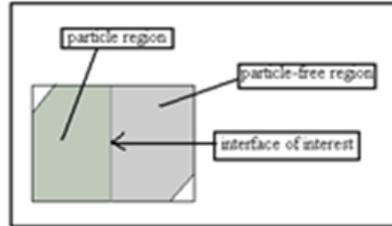
Sample Name	Sample Shape	Substrate	Thick or Thin Si?	Big or Small Die?	Deposition Type	Surface Prep	Plating Composition (if applicable)	Deposition End	Deposition Conditions	Post Processing	Aging Temperature	RESULTS
LE1	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	Electroplating	solvent rinse	Techni Matte Tin Sulfate 89T (stannous sulfate + H2SO4)	10 minutes	RT, agitation	Ammonium Hydroxide dp, 30 seconds	32	whiskers at 9 weeks
LE2	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	Electroless Plating	solvent rinse	Durak Tinnit Electroless (acid-based)	20 minutes	55C, agitation every 5 minutes	Ammonium Hydroxide dp, 30 seconds	32	whiskers at 9 weeks
LE3	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	Electroplating	solvent rinse	Techni Matte Tin Sulfate 89T (stannous sulfate + H2SO4)	96.14 min (7.98 Amp*min)	RT, agitation	Ammonium Hydroxide dp, 30 seconds	32	whiskers at 2 weeks
LE4	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	Electroplating	LAC-81, 10% sulfuric dip	Techni Bright Acid Tin (stannous sulfate + H2SO4 + brightener + antioxidant)	33.85 min (2.81 Amp*min)	RT, agitation	Ammonium Hydroxide dp, 30 seconds	32	no whiskers
LE5	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	Electroplating	LAC-81, 10% sulfuric dip	Techni Bright Acid Tin (stannous sulfate + H2SO4 + brightener + antioxidant)	96 minutes	RT, agitation	Ammonium Hydroxide dp, 30 seconds	32	whiskers at 44 weeks
LE6	Beam Pattern	100um Si	Thin	Small	Electron Beam Evaporation	HF dp	NA	~2.7 microns QCM	P=6.9e-7T, 33% Power, ~5 A/Sec	none	32	no whiskers
LE7	Beam Pattern	100um Si	Thin	Small	Resistive Evaporation	HF dp	NA	600nm QCM	P=5.0e-8MB, 37% Power, ~0.94nm/Sec	none	32	no whiskers
LE7b	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	Resistive Evaporation	HF dp	NA	600nm QCM		none	32	no whiskers
LE8	Beam Pattern	100um Si	Thin	Small	DC Sputtering	HF dp	NA	31 minutes	P=2.3e-7T, presp 30sec @ 500V, sputter 31min @ 800V (1.2A, 613.1V, 25.7sccm Ar)	none	32	no whiskers
LE8b	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	DC Sputtering	HF dp	NA	31 minutes	P=2.3e-7T, presp 30sec @ 500V, sputter 31min @ 800V (1.2A, 613.1V, 25.7sccm Ar)	none	32	no whiskers
LE10a	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thin	Small	Electron Beam Evaporation	HF dp	NA	~1 micron QCM	P=6.9e-7T, 33% Power, ~5 A/Sec	none	32	whiskers at 0 weeks
LE10a	Beam Pattern	100um Si + 300A Cr + 2500A Cu	Thick	Small	Electron Beam Evaporation	HF dp	NA	~1 micron QCM	P=6.9e-7T, 33% Power, ~5 A/Sec	none	32	whiskers at 0 weeks

Table 4: Description of "LE" Sample Preparation and Subsequent Whiskering Results

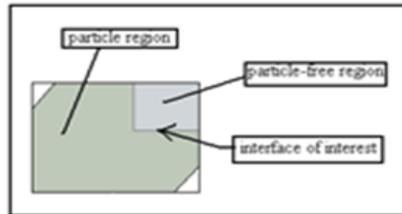
B. Microparticles

Side-by-side samples, wherein half of a ~1” scribed silicon square had been masked during the microparticle spincoating step prior to deposition, were analyzed (along with untreated control samples) in the Microanalysis lab at JHUAPL. Samples were named “A” or “C” (for “amino” or “carboxyl” type cross-linked polystyrene) followed by a sequential number. Figure 12 below shows the analytical reference sheets used during SEM imaging. No whisker activity was observed on any particle-treated sample, regardless of sample geometry (size, shape, and die thickness) employed, particle type/treatment used, thermal aging, or silicon wafer type (the latter, however, was not expected to have any impact). By contrast, both particle-free control samples whiskered despite there being no thermal treatment (ambient storage only).

Sample(s): A1 & C1
Description: Previously imaged "side by side" samples (tape was used to mask the particle-free regions)
Analysis Desired: Top view of interface, to see if additional aging has caused whisker ring to occur on one or both sides.



Sample(s): A2 & C2
Description: New "side by side" samples (this time, used clip-on mask to minimize residue left behind in whisker-free regions)
Analysis Desired: Top view of interface, to see if aging has caused whiskers to grow on either side.



Sample : CTRL2
Description: New, 'control' sample with no particles anywhere.
Analysis Desired: Top view of surface, to see if aging was sufficient to cause whisker ring on a non-particle samples.

Sample : Sn Wires
Description: Previously imaged "Sn nanowires" sample
Analysis Desired: Cross-section views, to see if aging has caused whiskers to grow from any of the surfaces of the nanowires.

Figure 12: SEM Analysis Reference Instructions (example)

Sample Name	Sample Shape	Substrate	Type	Resistivity	Thick or Thin Si?	Big or Small Die?	Deposition Type	Surface Prep	Plating Composition (if applicable)	Deposition End	Deposition Conditions	Post Processing	Aging Temperature	RESULTS
thinSS_C	1H WAFER	100um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Big	Electron Beam Evaporation	clean	NA	NA	NA	Carboxyl PS, 200C HP, 5.1 Days, petrie covered	200	no whiskers
thinSS_A	1H WAFER	100um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Big	Electron Beam Evaporation	clean	NA	NA	NA	Amino PS, 200C HP, 5.1 Days, petrie covered	200	no whiskers
C1	1" square	525um Si - 400A Cr, 2500A Cu, 1um Sn	P	"5-40"	Thick	Big	Electron Beam Evaporation	clean	NA	NA	NA	Carboxyl PS, 200C HP, 4.3 Days, petrie covered + 5 Days 200C Oven	200	no whiskers
C2	1" square	525um Si - 400A Cr, 2500A Cu, 1um Sn	P	"5-40"	Thick	Big	Electron Beam Evaporation	clean	NA	NA	NA	Carboxyl PS, 200C HP, 4.8 Days 200C Oven	200	no whiskers
A1	1" square	525um Si - 400A Cr, 2500A Cu, 1um Sn	P	"5-40"	Thick	Big	Electron Beam Evaporation	clean	NA	NA	NA	Amino PS, 200C HP, 4.3 Days, petrie covered + 5 Days 200C Oven	200	no whiskers
A2	1" square	525um Si - 400A Cr, 2500A Cu, 1um Sn	P	"5-40"	Thick	Big	Electron Beam Evaporation	clean	NA	NA	NA	Amino PS, 200C HP, 4.8 Days 200C Oven	200	no whiskers
CONTROL	1" square	525um Si - 400A Cr, 2500A Cu, 1um Sn	P	"5-40"	Thick	Big	Electron Beam Evaporation	clean	NA	NA	NA	200C HP, 4.8 Days 200C Oven	200	no whiskers
TH10_thick	Beam Pattern	525um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	200C HP, 16 hours	200	no whiskers
TH10_thin	Beam Pattern	100um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	200C HP, 16 hours	200	no whiskers
TH11_thick	Beam Pattern	525um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	200C HP, 16 hours, particles	200	no whiskers
TH11_thin	Beam Pattern	100um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	200C HP, 16 hours, particles	200	no whiskers
L10_thick	Beam Pattern	525um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	none	32	whiskers at 3 days
L10_thin	Beam Pattern	100um Si - 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	none	32	whiskers at 3 days

Table 5: Description of Particle and "TH" Sample Preparation and Subsequent Whiskering Results

C. Organic Contamination (Surface, Buried)

Whiskering occurred on all samples within experimental subset C, including the control samples. No appreciable differences in whisker lengths or densities were observed when comparing post-processing thermal aging conditions and the situation of the contaminant (surface or buried) within the sample stackup. After 61 weeks of aging, samples TH1 through TH8 contain an average (per $100\mu\text{m} \times 100\mu\text{m}$ area) of ~45 'short whiskers' (length = 2-4 μm), ~5 'medium length whiskers' (length = ~10 μm), and approximately 1 'long whisker' (length = 20-50 μm).

Sample Name	Sample Shape	Substrate	Type	Resistivity	Thick or Thin Si?	Big or Small Die?	Deposition Type	Surface Prep	Plating Composition (if applicable)	Deposition End	Deposition Conditions	Post Processing	Aging Temperature	RESULTS
TH1	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	200C Oven, 5 Days, uncovered	200	whiskers
TH2	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	organic contamination AZ9240 • acetone	NA	NA	NA	200C Oven, 5 Days, uncovered	200	whiskers
TH3	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	200C Oven, 3 Days, uncovered	200	whiskers
TH4	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	organic contamination buried AZ9240 • acetone	NA	NA	NA	200C Oven, 3 Days, uncovered	200	whiskers
TH5	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	organic contamination surface AZ9240 • acetone	NA	NA	NA	200C Oven, 3 Days, uncovered	200	whiskers
TH6	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	clean	NA	NA	NA	200C HP, 7 Days, petrie covered	200	whiskers
TH7	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	organic contamination buried AZ9240 • acetone	NA	NA	NA	200C HP, 7 Days, petrie covered	200	whiskers
TH8	Beam Pattern	100um Si • 400A Cr, 2500A Cu, 1um Sn	N	"0.005-0.02"	Thin	Small	Electron Beam Evaporation	organic contamination surface AZ9240 • acetone	NA	NA	NA	200C HP, 7 Days, petrie covered	200	whiskers

Table 6: Description of "TH" Sample Preparation and Subsequent Whiskering Results

D. Geometric Studies

Due to the volume of datapoints associated with experimental subset D, bivariate graphical representation (bubble charts) of tabulated whisker frequencies were employed as a convenient means of making qualitative assessments. A number of trends can be observed within Figures 13-15 below. Whiskering frequency (or “density”) immediately following tin deposition (within 2 hours of venting the evaporator and removing the samples for inspection) appears to trend lower as the silicon thickness increases (along the x-axis), and to a lesser extent appears to trend lower as the length of the sample side increases. After 12 weeks of ambient aging, there was much more uniform whiskering character across all samples, as evidenced by the second, “fuller” bubble chart shown in Figure 14.

Si Thickness (um)	X-Y Dimension (mm)	Date	Largest Mag Recorded	Grain Size (um)	Whiskers?	Average Whisker Length	#/area (at 1,000x)	Date	Largest Mag	Grain Size (um)	Whiskers ?	Average Whisker	#/area (at 1,000x)
20	3	7/8/09	20000	1	yes	2	7	7/21/09	8000	1	yes	5	55
20	4	7/8/09	25000	1	yes	1.5	2	7/21/09	-	1	yes	3	34
20	5	7/8/09	20000	1	yes	2	3	7/21/09	5000	1	yes	2	21
20	5 (beam)	7/8/09	30000	1	yes	1.5	3	7/21/09	20000	1	yes	3	38
20	6	7/8/09	30000	1	yes	1.5	1	7/21/09	11800	1	yes	3	27
20	7	7/8/09	25000	1	yes	1.5	3	7/21/09	9020	1	yes	3	35
20	10	7/8/09	20000	1	yes	3	1	7/21/09	20000	1	yes	3	25
20	12	7/8/09	15000	1	yes	3	1	7/21/09	11000	1	yes	3	32
50	3	7/8/09	25000	1	yes	2	6	7/21/09	8000	1	yes	2	26
50	4	7/8/09	25000	1	yes	2	6	7/21/09	15000	1	yes	3	36
50	5	7/8/09	30000	1	yes	2	5	7/21/09	10000	1	yes	2	40
50	5 (beam)	7/8/09	30000	1	yes	2	5	7/21/09	20000	1	yes	2	38
50	6	7/8/09	20000	1	yes	2	5	7/21/09	20000	1	yes	2	34
50	7	7/8/09	25000	1	yes	2	8	7/21/09	20000	1	yes	2	30
50	10	7/8/09	25000	1	yes	2	3	7/21/09	25000	1	yes	2	30
50	12	7/8/09	15000	1	yes	2	7	7/21/09	8000	1	yes	2	28
75	3	7/8/09	20000	1	yes	2	3	7/21/09	6000	1	yes	3	34
75	4	7/8/09	25000	1	yes	2	3	7/21/09	20000	1	yes	2	23
75	5	7/8/09	1000	1	no	N/A	N/A	7/21/09	13000	1	yes	4	35
75	5 (beam)	7/8/09	1000	1	no	N/A	N/A	7/21/09	15000	1	yes	3	39
75	6	7/8/09	1000	1	no	N/A	N/A	7/21/09	15000	1	yes	3	27
75	7	7/8/09	15000	1	yes	2	1	7/21/09	20000	1	yes	3	30
75	10	7/8/09	15000	1	yes	2.5	2	7/21/09	11000	1	yes	3	28
75	12	7/8/09	20000	1	yes	2.5	4	7/23/09	8010	1	yes	2	35
90	3	7/9/09	15000	1	yes	1	2	7/23/09	18000	1	yes	2	59
90	4	7/9/09	20000	1	yes	1	2	7/23/09	5000	1	yes	2	64
90	5	7/9/09	20000	1	yes	1.25	2	7/23/09	8010	1	yes	2	70
90	5 (beam)	7/9/09	20000	1	yes	1	1	7/23/09	15000	1	yes	2	57
90	6	7/9/09	15000	1	yes	1	2	7/23/09	20000	1	yes	2	51
90	7	7/9/09	30000	1	yes	1.5	1	7/23/09	15000	1	yes	2	58
90	10	7/9/09	1000	1	no	N/A	N/A	7/23/09	15000	1	yes	2	50
90	12	7/9/09	25000	1	yes	1.5	5	7/23/09	18000	1	yes	2	45
125	3	7/9/09	15000	1	yes	2	2	7/23/09	18000	1	yes	2	74
125	4	7/9/09	20000	1	yes	1	4	7/23/09	9000	1	yes	2	68
125	5	7/9/09	20000	1	yes	1	4	7/23/09	10000	1	yes	2	59
125	5 (beam)	7/9/09	15000	1	yes	2		7/23/09	5000	1	yes	2	63
125	6	7/9/09	15000	1	yes	1	1	7/23/09	11000	1	yes	2	58
125	7	7/9/09	15000	1	yes	2	2	7/23/09	7000	1	yes	2	55
125	10	7/9/09	20000	1	yes	1	1	7/23/09	2500	1	yes	2	59
125	12	7/9/09	15000	1	yes	2	3	7/23/09	20000	1	yes	2	51

Table 7: SEM Analysis Results of Geometry-Based Experimental Trials

Si Thickness (um)	X-Y Dimension (mm)	Date	Largest Mag Recorded	Grain Size (um)	Whiskers?	Average Whisker Length	#/area (at 1,000x)	Date	Largest Mag	Grain Size (um)	Whiskers ?	Average Whisker	#/area (at 1,000x)
150	3	7/9/09	15000	1	yes	2	2	7/23/09	6000	1	yes	2	53
150	4	7/9/09	20000	1	yes	2	2	7/23/09	13000	1	yes	2	61
150	5	7/9/09	20000	1	yes	1.5	2	7/23/09	10000	1	yes	2	51
150	5 (beam)	7/9/09	1000	1	yes	2	3	7/23/09	5010	1	yes	2	51
150	6	7/9/09	20000	1	yes	1.5	1	7/23/09	9000	1	yes	2	48
150	7	7/9/09	20000	1	yes	2	1	7/23/09	13000	1	yes	2	54
150	10	7/9/09	20000	1	yes	1.5	1	7/23/09	15000	1	yes	2	50
150	12	7/9/09	20000	1	yes	1.5	1	7/23/09	15000	1	yes	2	60
175	3	7/9/09	20000	1	yes	3	1	7/23/09	13000	1	yes	3	57
175	4	7/9/09	20000	1	yes	2	3	7/23/09	2500	1	yes	2	56
175	5	7/9/09	25000	1	yes	2	4	7/23/09	25000	1	yes	2	57
175	5 (beam)	7/9/09	1000	1	no	N/A	N/A	7/23/09	7000	1	yes	2	71
175	6	7/9/09	30000	1	yes	1	1	7/23/09	8010	1	yes	2	60
175	7	7/9/09	20000	1	yes	1	1	7/23/09	11000	1	yes	2	65
175	10	7/9/09	15000	1	no	N/A	N/A	7/23/09	15000	1	yes	2	55
175	12	7/9/09	20000	1	yes	1.5	3	7/23/09	13000	1	yes	2	44
190	3	7/8/09	20000	1	yes	2.5	8	7/21/09	20000	1	yes	2	37
190	4	7/8/09	30000	1	yes	2	8	7/21/09	15000	1	yes	2	31
190	5	7/8/09	25000	1	yes	2	5	7/21/09	9000	1	yes	2	30
190	5 (beam)	7/8/09	25000	1	yes	2	5	7/21/09	8000	1	yes	3	36
190	6	7/8/09	35000	1	yes	1.5	9	7/21/09	4000	1	yes	2	27
190	7	7/8/09	30000	1	yes	1.5	4	7/21/09	10000	1	yes	2	26
190	10	7/8/09	20000	1	yes	1.5	4	7/21/09	18000	1	yes	3	26
190	12	7/8/09	20000	1	yes	2	5	7/21/09	20000	1	yes	2	28
225	3	7/8/09	20000	1	yes	2	2	7/21/09	11000	1	yes	2	22
225	4	7/8/09	25000	1	yes	2	1	7/21/09	20000	1	yes	5	35
225	5	7/8/09	1000	1	no	N/A	N/A	7/21/09	18000	1	yes	5	31
225	5 (beam)	7/8/09	1000	1	no	N/A	N/A	7/21/09	3000	1	yes	4	25
225	6	7/8/09	1000	1	no	N/A	N/A	7/21/09	11000	1	yes	3	28
225	7	7/8/09	1000	1	no	N/A	N/A	7/21/09	20000	1	yes	3	37
225	10	7/8/09	1000	1	no	N/A	N/A	7/21/09	5000	1	yes	3	27
225	12	7/8/09	15000	1	yes	2	5	7/21/09	8010	1	yes	2	36
250	3	7/8/09	1000	1	no	N/A	N/A	7/21/09	13000	1	yes	2	34
250	4	7/8/09	1000	1	no	N/A	N/A	7/21/09	9000	1	yes	5	27
250	5	7/8/09	1000	1	no	N/A	N/A	7/21/09	8000	1	yes	5	26
250	5 (beam)	7/8/09	1000	1	no	N/A	N/A	7/21/09	20000	1	yes	5	36
250	6	7/8/09	1000	1	no	N/A	N/A	7/21/09	20000	1	yes	4	26
250	7	7/8/09	1000	1	no	N/A	N/A	7/21/09	5000	1	yes	3	31
250	10	7/8/09	1000	1	no	N/A	N/A	7/21/09	7000	1	yes	3	25
250	12	7/8/09	20000	1	yes	3	8	7/21/09	10000	1	yes	2	34

Table 7 (cont'd): SEM Analysis of Geometry-Based Experimental Trials

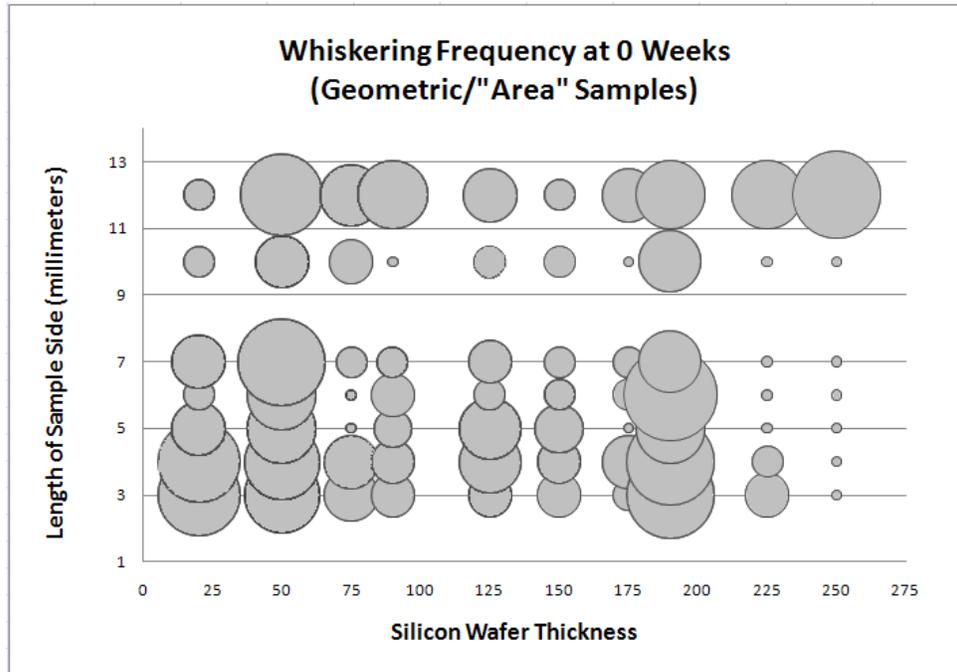


Figure 13: Whiskering at 0 Weeks, Sample Thickness vs. Side Length

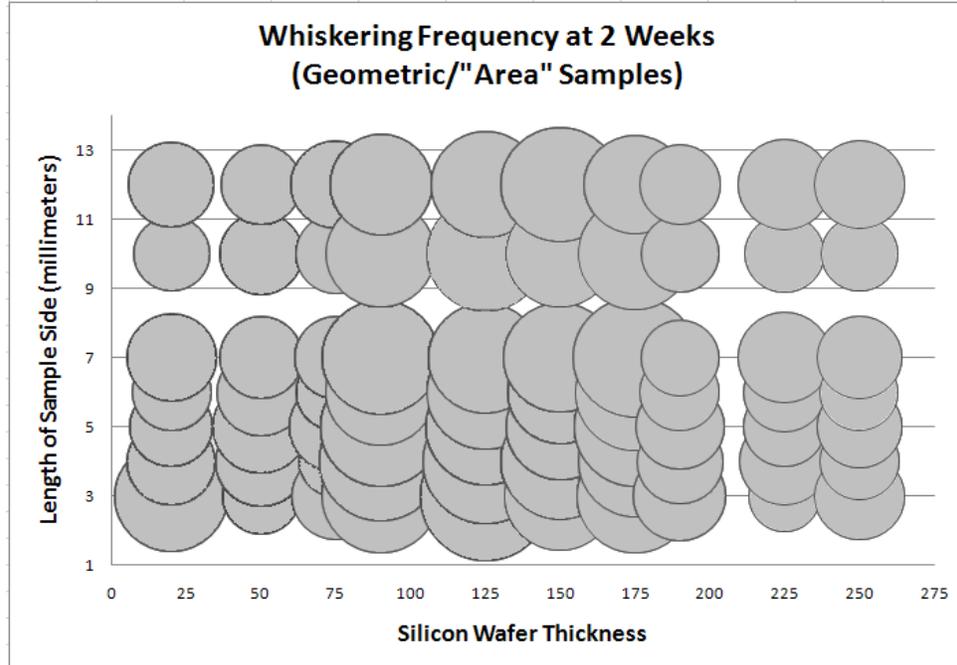


Figure 14: Whiskering at 2 Weeks, Sample Thickness vs. Side Length

The coefficient of determination for a 6th-order polynomial trendline in the case of the smallest sample geometry (3mm x 3mm) is 0.6608 when the 200 μ m die thickness value (8 whiskers) is included, but improves to a near-perfect 0.9988 when that datapoint is removed. In either case, there is a downtrend that is reasonably suggestive of a delayed whiskering onset in the case of the thicker dies, for a given x-y geometry. There is also an unexplained, but consistent “inflection” in whiskering frequency on the 190-micron thick samples.

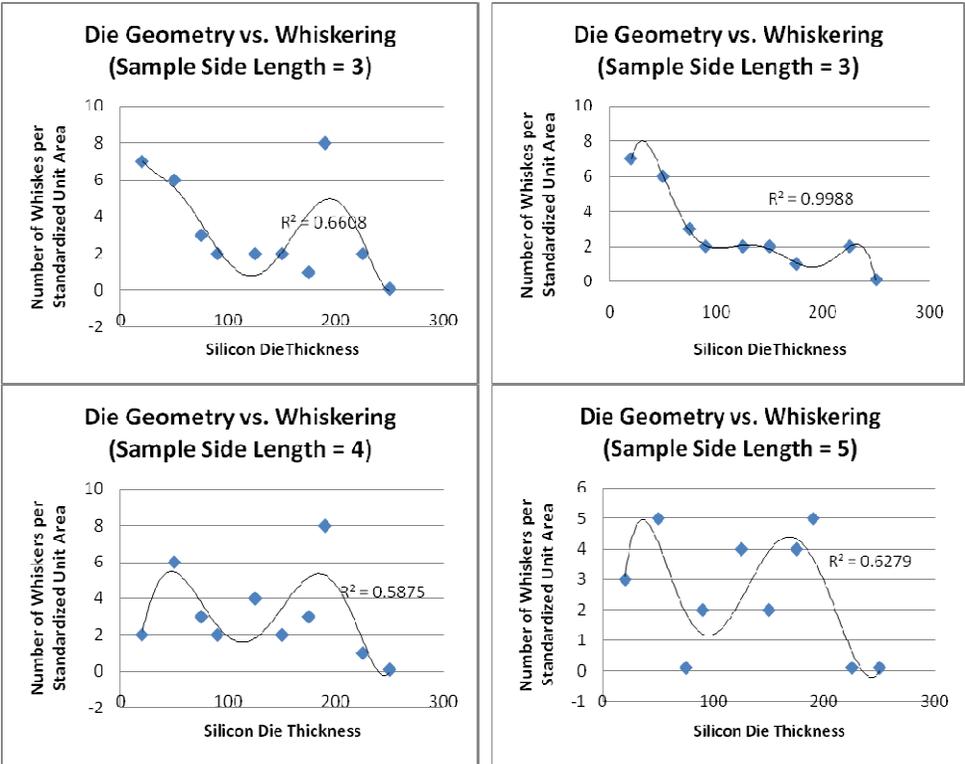


Figure 15: Sample Thickness vs. Whisker Density for Various Side Lengths (6th Order Polynomial Trendline Fitting)

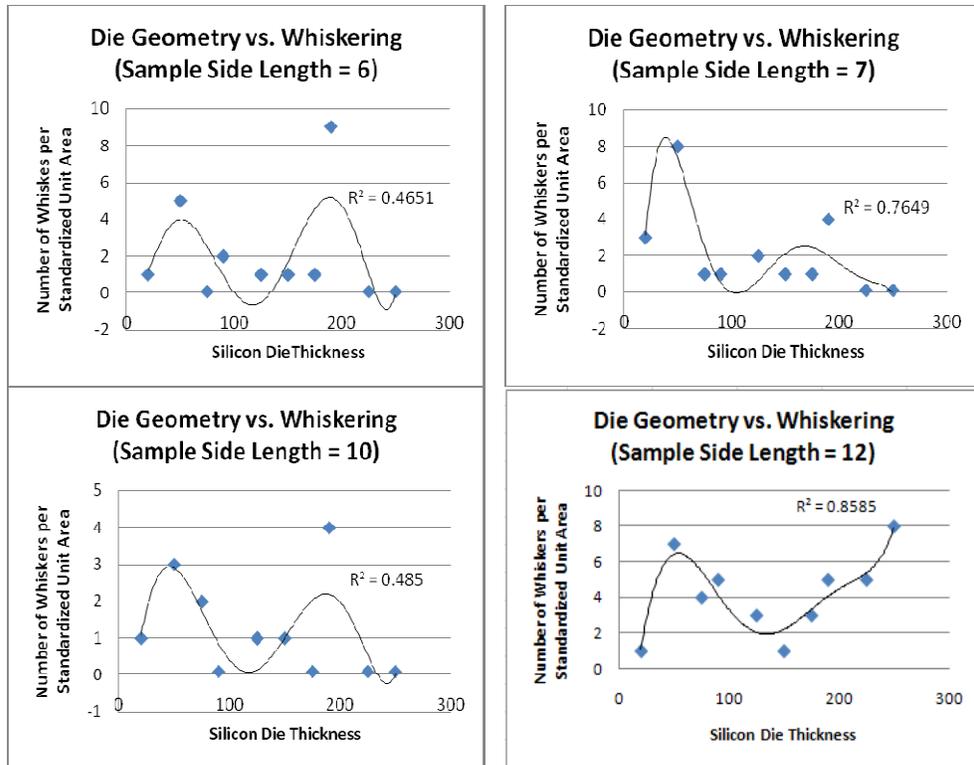


Figure 15 (cont'd) : Sample Thickness vs. Whisker Density for Various Side Lengths (6th Order Polynomial Trendline Fitting)

The effect of including the 190- μ m thick samples on the statistical significance of the downtrend curves generated by polynomial fitting is large.

Sample Side Length (in mm.)	Polynomial Curve Fitting			
	With 190- μ m Sample		Without 190- μ m Sample	
	Coefficient of Determination (R^2)	Correlation Coefficient ('R')	Coefficient of Determination (R^2)	Correlation Coefficient ('R')
3	0.6608	0.812896057	0.9988	0.99939982
4	0.5875	0.766485486	0.8633	0.929139387
5	0.3998	0.632297398	0.9415	0.970309229
6	0.4651	0.681982404	0.7601	0.871837141
7	0.7649	0.874585616	0.938	0.968504001
10	0.485	0.696419414	0.8856	0.941063228
12	0.8585	0.926552751	0.9017	0.949578854

Table 8: Curve-Fitting Statistics for 3mm-12mm Side Lengths, With and Without the 190- μ m Thickness Samples

E. Tin Nanowires

Despite thermal aging (200°C hotplate for 5 days) following the initial electrodeposition, along with an aging period of more than 7 months under ambient conditions, no whiskers can be found growing on the template-synthesized tin nanowires. Cross-sectional scans of the aged wires are shown in Figure 16 below.

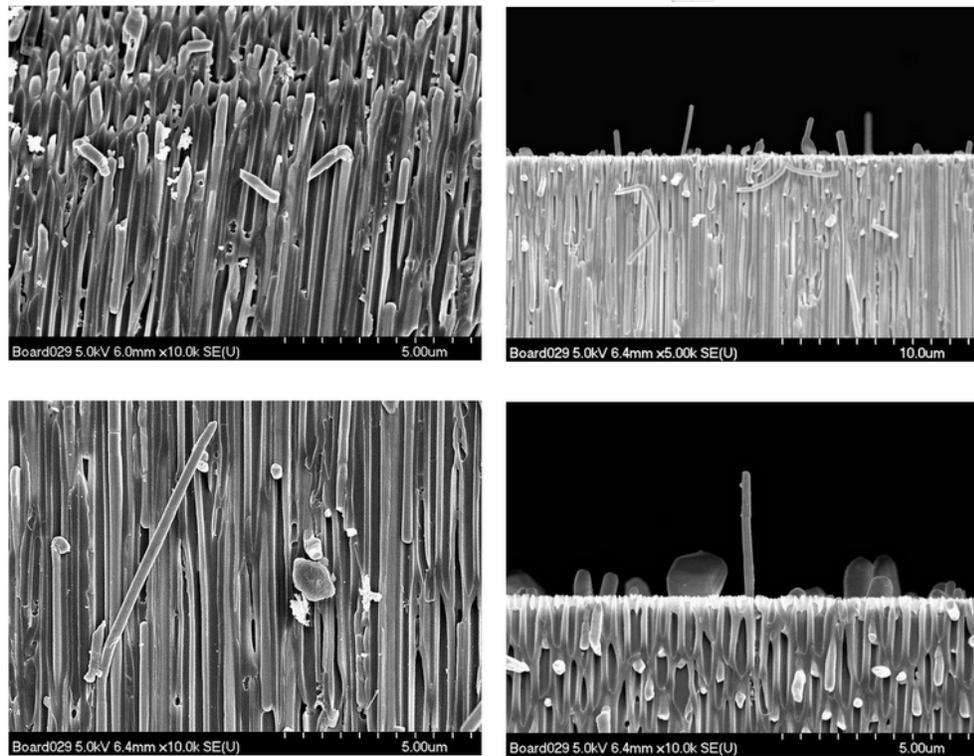


Figure 16: Tin Nanowires, Hotplate Aged for 5 Days (Whisker-Free)

PHASE V: Wafer-Level Stress Study

A custom batch of 100mm-diameter <100>-oriented silicon wafers of assorted thicknesses, ranging from 20 to 250 microns were employed in a stress study to determine the effect of ambient aging on the magnitude of the composite sample stress. A laser-based (670nm and 750nm) KLA-Tencor FLX-2908 Thin

Film Stress Measurement system was used for this purpose. First, background “radius of curvature” and “bow” measurements were taken of the as-received (fab cleaned) wafers. Next, electron beam evaporation of 400Å of chromium, followed by 2,690Å of copper, followed by 1µm of tin were deposited at an ultimate vacuum of 6.8×10^{-7} Torr. The chromium was deposited at 24% power at a rate of $\sim 3.3\text{Å}/\text{sec}$. The chamber pressure prior to the copper step read 3.1×10^{-7} Torr. The copper was deposited at 38% power at a rate of $\sim 4.7\text{Å}/\text{sec}$. The chamber pressure prior to the tin step read 1.2×10^{-6} Torr. The tin was deposited at 32% power at a rate of $\sim 4.4\text{Å}/\text{sec}$. Samples were allowed to cool for a period of approximately 10 minutes prior to atmospheric venting, after which immediate radius, bow, and stress measurements were taken. Post-metallization radius, bow, and stress measurements were again recorded after 43 days of ambient aging. Microstrain (strain multiplied by 10^6) values, computed using the Young’s Modulus for isotropic tin, are also provided for both sets of stress values. The numerical data from these experiments are tabulated in the figure below and presented graphically in the scatterplots that follow.

Sample Name	Thickness (um)	Tolerance (+/-) (um)	Type	Dopant	First Measurement		Second Measurement				Third Measurement			
					Radius (m)	Bow (um)	Radius (m)	Bow (um)	Stress (Mpa, Compressive)	Microstrain (unitless)	Radius (m)	Bow (um)	Stress (Mpa, Compressive)	Microstrain (unitless)
WW20a	20	10	P	B	-8.595	105.01	-13.218	60.57	-110.8	2,216	NM	NM	NM	NA
WW20b	20	10	P	B										
WW50a	50	10	N	Ph	17.182	-44.11	166.303	-32.11	-3	60	-63.293	26.61	-4.3	86
WW50b	50	10	N	Ph										
WW50c	50	10	N	Ph										
WW50d	50	10	N	Ph										
WW75a	75	10	P	B	52.674	-15.19	-8.731	120.48	-17.9	358	-8.14	103.63	-18.3	366
WW75b	75	10	P	B										
WW90a	90	10	P	B	130.641	-6.52	-7.496	130.61	-26.3	526	-7.16	143.23	-27.4	548
WW90b	90	10	P	B										
WW125a	125	10	P	B	345.193	-3.33	-8.598	99.81	-42.8	856	-7.905	101.64	-46.5	930
WW125b	125	10	P	B										
WW150a	150	10	N	Ph	134.277	-6.54	-6.087	129.2	-88.8	1,776	-10.086	78.15	-55.1	1,102
WW150b	150	10	N	Ph										
WW175a	175	10	P	B	86.166	-9.08	-7.42	105.49	-103	2,060	-13.476	59.29	-60.4	1,208
WW175b	175	10	P	B										
WW190a	190	10	N	Ph	-919.432	2.13	-7.27	105.72	-113.2	2,264	-12.06	63.52	-67.9	1,358
WW190b	190	10	N	Ph										
WW225a	225	25	P	B	93.219	-8.85	-10.389	75.92	-124.5	2,490	-23.327	33.96	-62.4	1,248
WW225b	225	25	P	B										
WW250a	250	25	N	Ph	570.398	-1.12	-13.218	60.57	-110.8	2,216	-36.34	23.28	-41.7	834
WW250b	250	25	N	Ph										

Table 9: Wafer-Level Stress Study, Assorted Thicknesses (custom wafer set from Wafer World, West Palm Beach, FL)

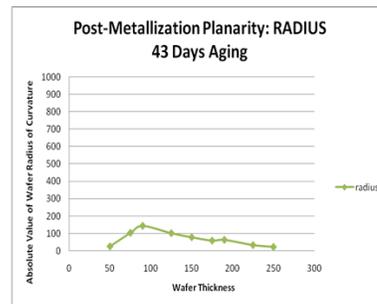
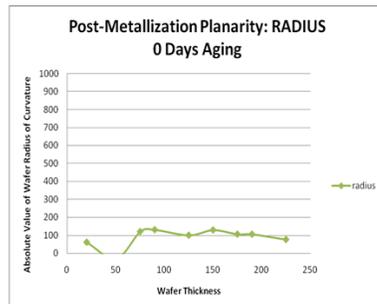
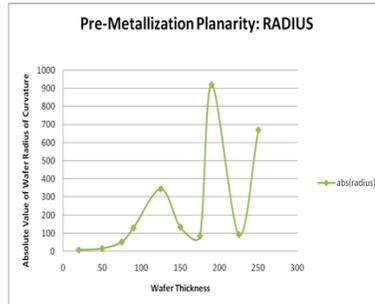


Figure 17: Wafer-Level Radius, Pre- and Post-Metallization/Aging

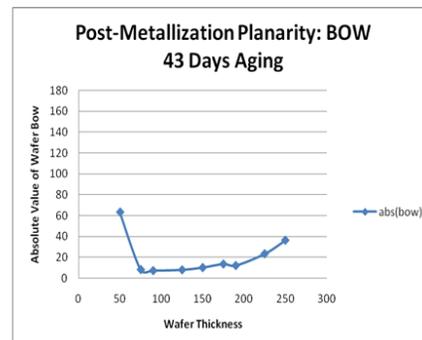
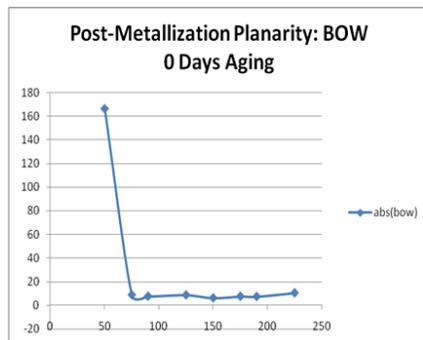
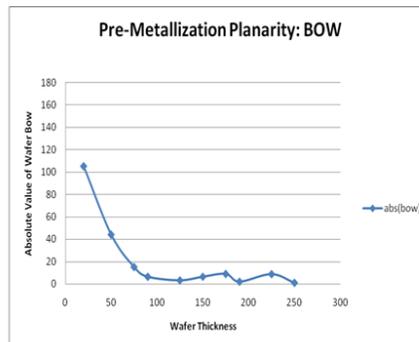


Figure 18: Wafer-Level Bow, Pre- and Post-Metallization/Aging

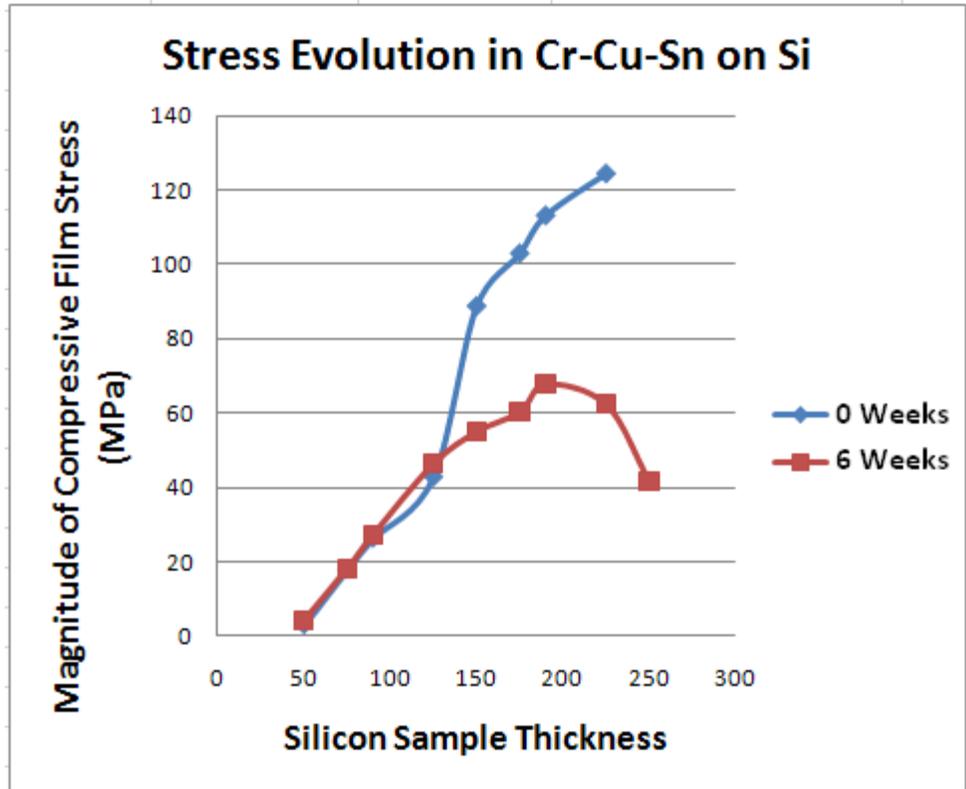


Figure 19: Film Stress vs. Sample Thicknesses, Aged 0 and 6 Weeks

SEM inspection of all ten wafers (loaded intact into the chamber, one by one) after 6 weeks of ambient aging revealed *indistinguishable* results in terms of whiskers. All specimens contained an average density of 20 whiskers per $100 \mu\text{m} \times 100 \mu\text{m}$ area, with lengths of 2-4 μm .

CHAPTER 3: SUMMARY, CONCLUSIONS, & FUTURE WORK

This work has described a series of empirical studies exploring the fundamental relationships between the incidence of tin whiskering (as dependent variable) and such independent variables as deposition method (electroplating, electroless plating, template-based electrochemical synthesis, and various physical vapor deposition techniques, including resistive evaporation, electron beam evaporation, and sputtering), the inclusion of microparticles, organic contamination, the effects of sample geometry, and the aging of tin nanowires. Several of the trends that have been observed/identified by this study are summarized in the diagram of Figure 20 (below).

Our most significant and novel findings pertain to the relevance of sample geometry to the whiskering character of samples, particularly early in their evolutionary stages. Bivariate graphical analysis revealed a trending toward lower whisker densities for thicker silicon substrates, and a less pronounced (but still observable) trending toward lower whisker densities for larger sample side lengths. The impacts of sample *thickness* on tin whiskering propensity, with respect to the changes over time in stress for a series of wafer-level stress measurements, were also observed. Despite the fact that all stress samples whiskered, there was no time-induced stress shift (at the macroscale) among the thinnest samples after 43 days. Downtrending in whiskering propensity curves, as shown in Phase IV, Section D, was found to be statistically significant, at p-values ranging from 0.63-0.92. Removing the presumed anomalous datapoints from the

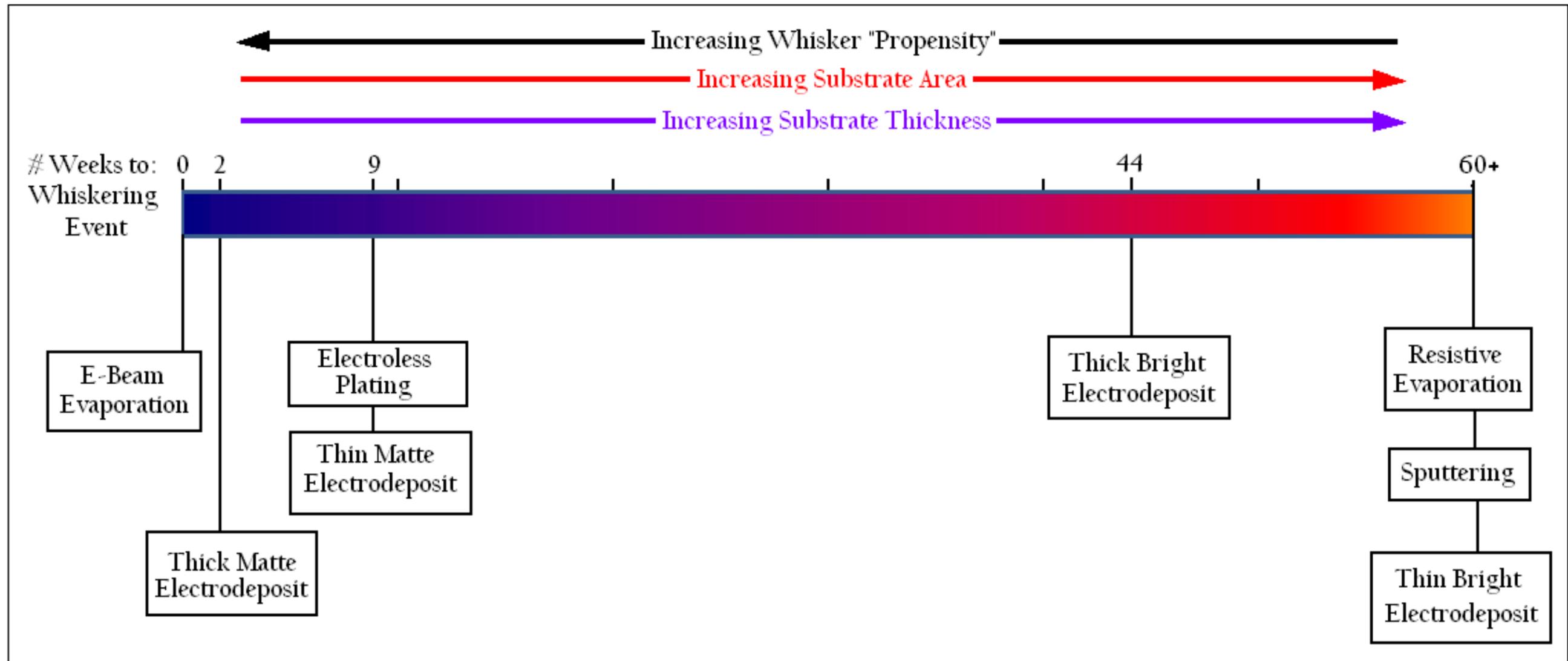


Figure 20: Summary of Observed Whiskering Trends

190- μm thick sample resulted in improved p-values, ranging from 0.87-0.999, across all data subsets. These results suggest that thicker silicon, more rigid and therefore less able to compensate for stress through intrinsic deformation, is undergoing a slower stress relief mechanism (such as whisker growth), while the films on thinner silicon die are accomplishing this stress relief over a significantly shorter period.

We found differences in whiskering onset ages depending on the deposition techniques employed, with thin “bright” electroplated films showing no whiskers after 61 weeks of ambient aging. We determined that even high-vacuum physical vapor deposition techniques, ostensibly “clean” and “contaminant free,” produce whisker-prone films. Organic contamination, when intentionally introduced either beneath or atop Cr-Cu-Sn films, appeared to have no significant impact on whisker character, and showed comparable morphology to untreated “control” samples which were otherwise identically processed.

Results from the inclusion of inert microscale particles (cross-linked amino and carboxyl terminated polystyrene) in tin films were inconclusive, since although whiskering did not occur in any “particled” samples, we were unable to induce whiskering on the control side of side-by-side samples either. Additionally, tin nanowires did not display whiskering after an ambient aging period of more than 7 months.

This work contributes to the general body of tin whisker inquiry in several respects. First, no prior studies could be found in which deposition method was explicitly evaluated with respect to the whiskering its films would (or would not) produce. Second, a unique observation about the influence of sample geometry was made, which led to an extensive and costly study involving a matrix of over 70 permutations of X, Y, and Z substrate dimensions. Third, “clean” specimen preparation was stressed during several phases of this research, a characteristic which contrasts with the majority of tin whisker literature, which tend to focus on plated films. Finally, the use of silicon as our substrate of choice provided better sample-to-sample consistency, in terms of surface inertness and flatness, and also by virtue of its clean, reproducible micromachinability.

It is the opinion of the author that tin whisker growth originates from **localized strain** which has not been compensated for once a tin film’s internal recovery and recrystallization processes have ceased. Within this theoretical framework, variation among whiskering ‘incubation periods’ should be explained by differences in recovery & recrystallization time. More specifically, the sooner a transition to the ‘grain growth’ regime of metallographic transformation can take place, the sooner tin whiskers will begin to emerge. The localized strain which leads to tin whiskering does not necessarily correlate with the summated ‘macro’-stress in the overall thin film. Organic residue contamination does not have an appreciable impact on the whiskering strain. Conversely, Cu_6Sn_5 intermetallic compound (IMC) formation is a critical precursor to whiskering, and as such is likely one of the primary sources of whiskering strain. This IMC forms

at the Sn-Cu interface, and is illustrated graphically in Figure 21 below.

Augmenting the susceptibility of tin to form whiskers via abnormal grain growth (i.e., in distributed locations where grains are incapable of expanding in-plane, due to grain boundary pinning) is the grain structure itself. Unlike SnPb, intrinsically whisker-immune and having an equiaxed, mosaic-type cross-sectional morphology (see Figure 21 below), pure Sn films are characteristically columnar when viewed in cross-section. As such, pinned grains will naturally expand in the only unconstrained direction; normal to the film surface.

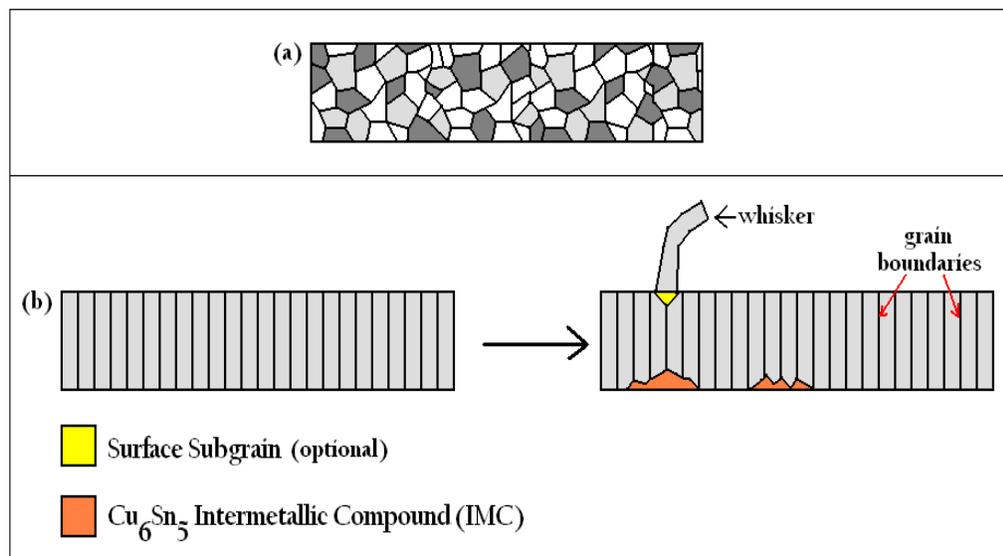


Figure 21: Cross-Sectional Diagrams of Grain Morphology for (a) SnPb and (b) Pure Sn

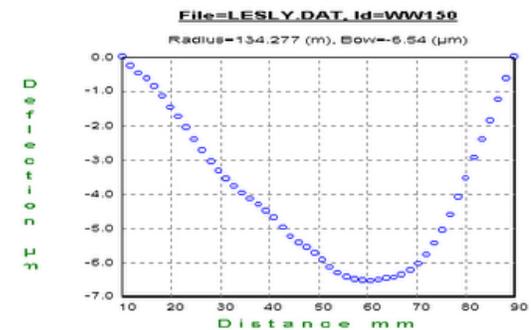
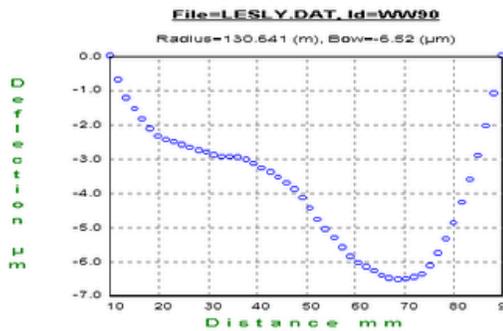
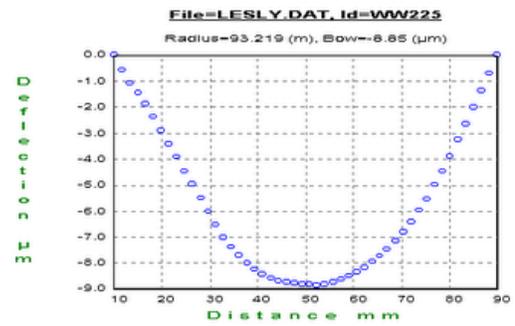
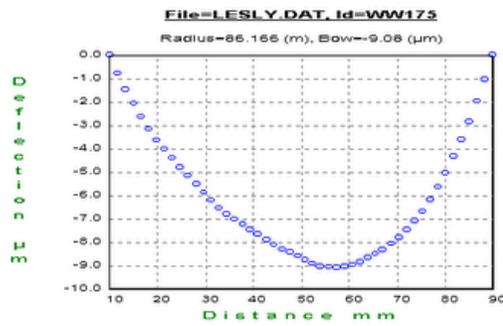
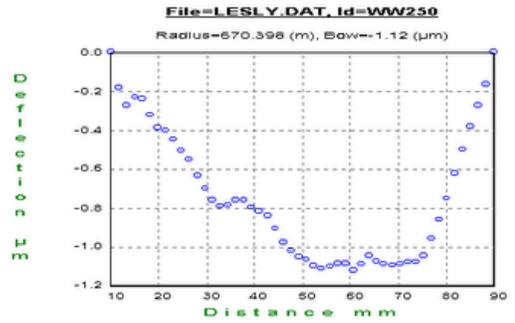
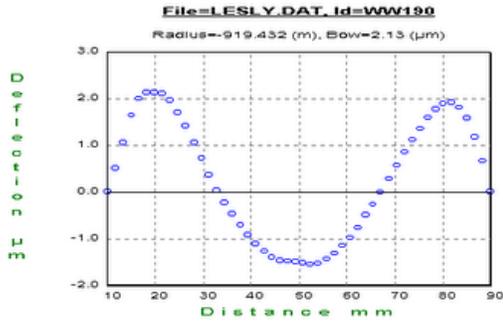
Future work should include further investigation into the concept of tin whisker mitigation through particle introduction. The mechanism through which this mitigation is expected to work is either by artificial extension of the recrystallization process (“continuous recrystallization”), thereby staving off the

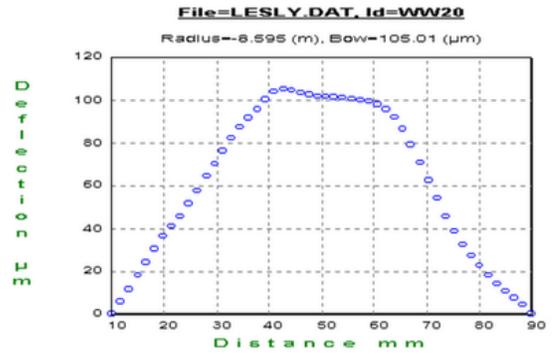
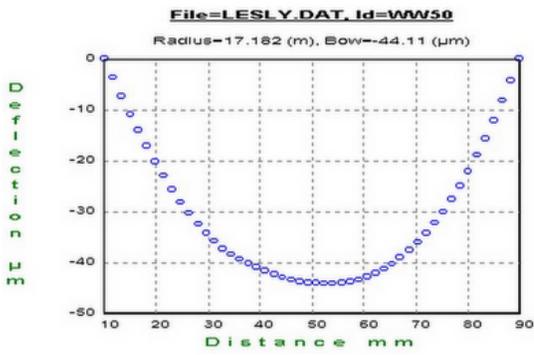
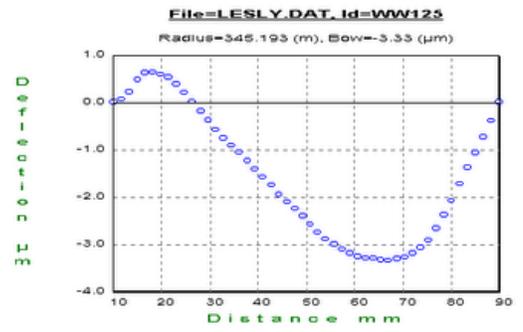
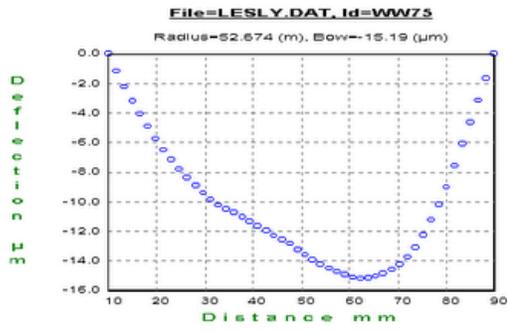
onset of grain growth, or through the provision of strain relaxation surfaces. Experimentation should involve the introduction of dispersions of fine particles, of varying mean diameters and volume densities, into tin thin films on copper surfaces. Particle introduction should be attempted through additional avenues not explored within this text, as well, including incorporation through a combination of electroplating and agitation. Additional particle 'types' should be explored as well, provided that the criteria of temperature resistance (at 200° C), shape permanence, and inertness within the context of the film stackup and substrate, are adhered to.

APPENDIX A

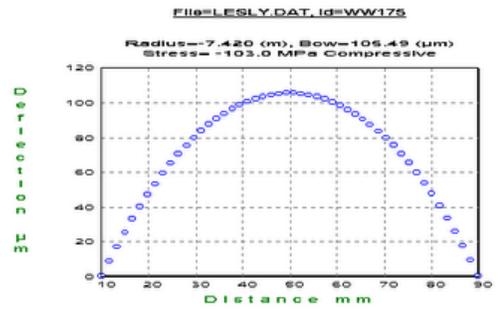
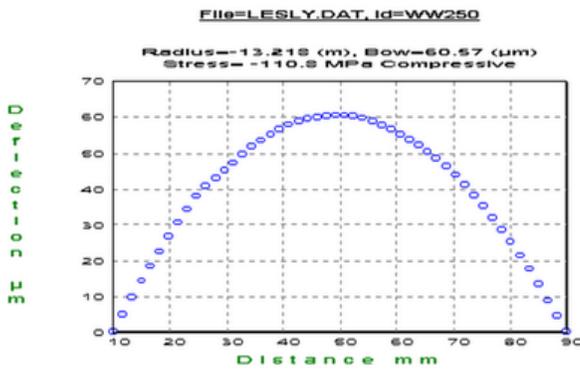
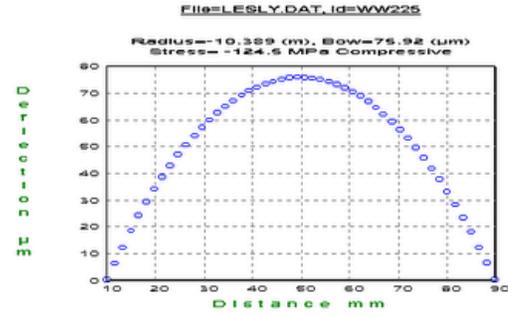
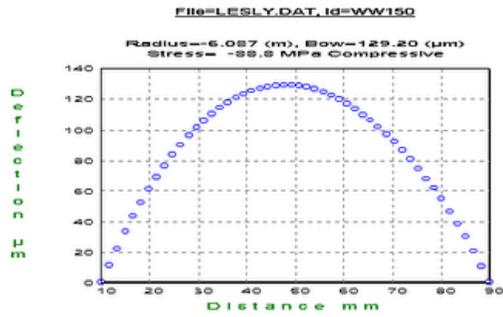
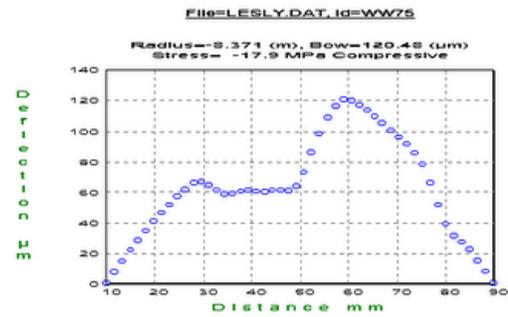
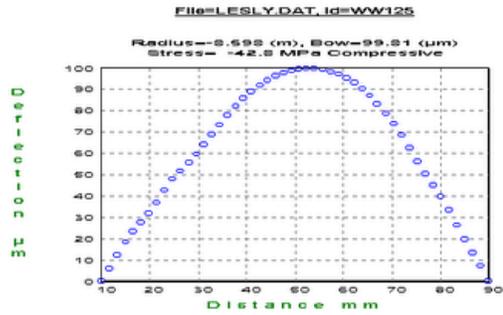
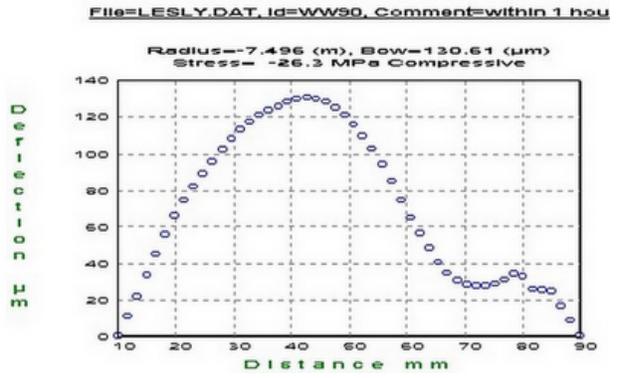
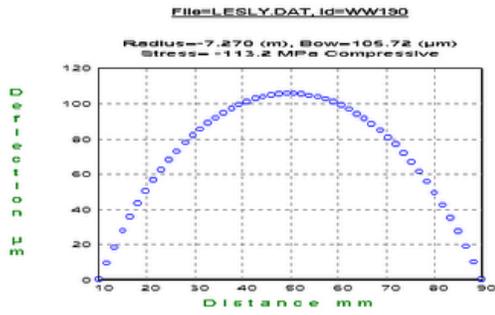
Phase V: Wafer-Level Stress Plots

Pre-Metallization



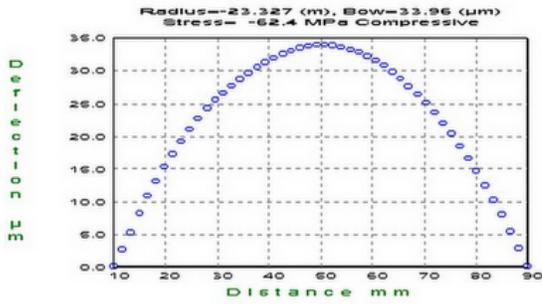


Post-Metallization (0 Days Aging)

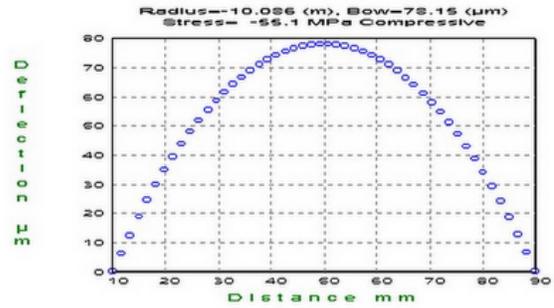


Post-Metallization (43 Days Ambient Aging)

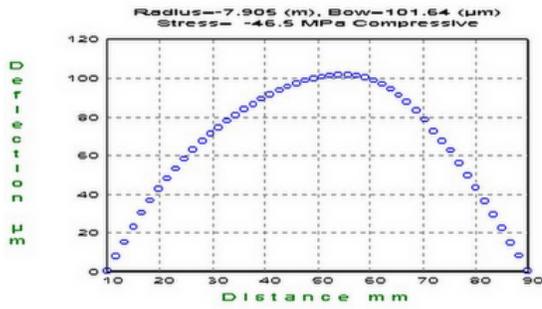
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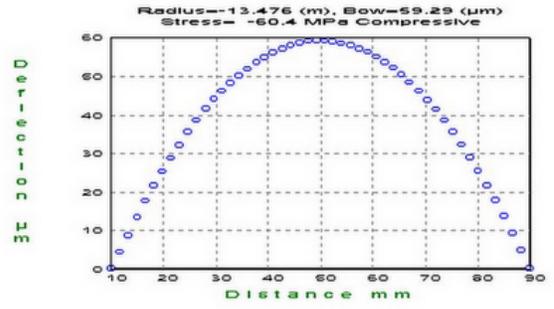
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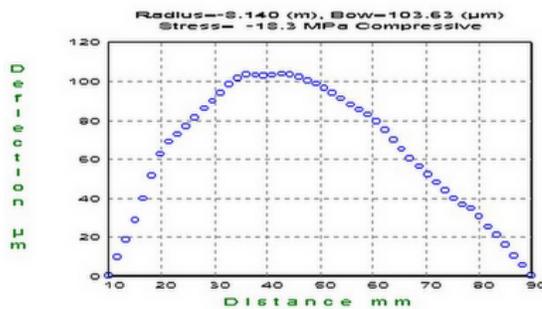
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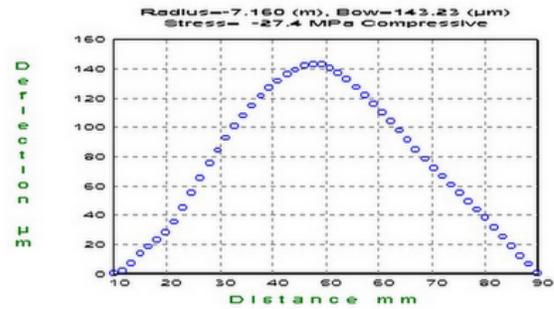
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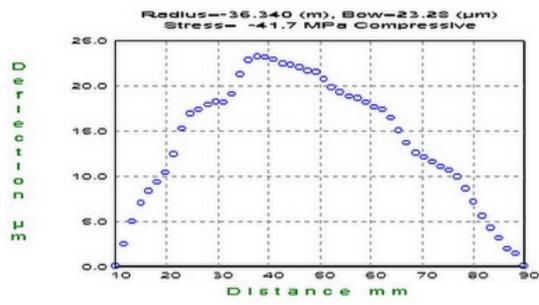
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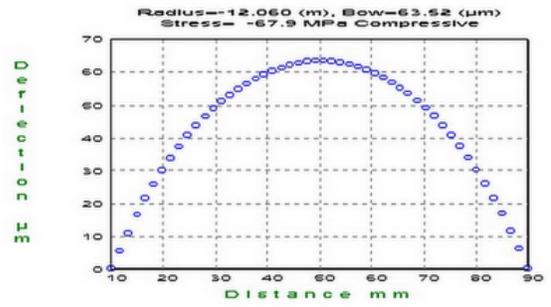
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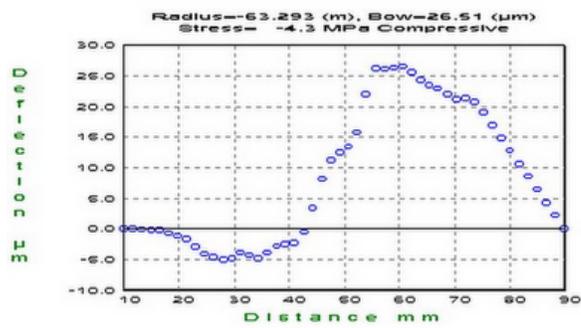
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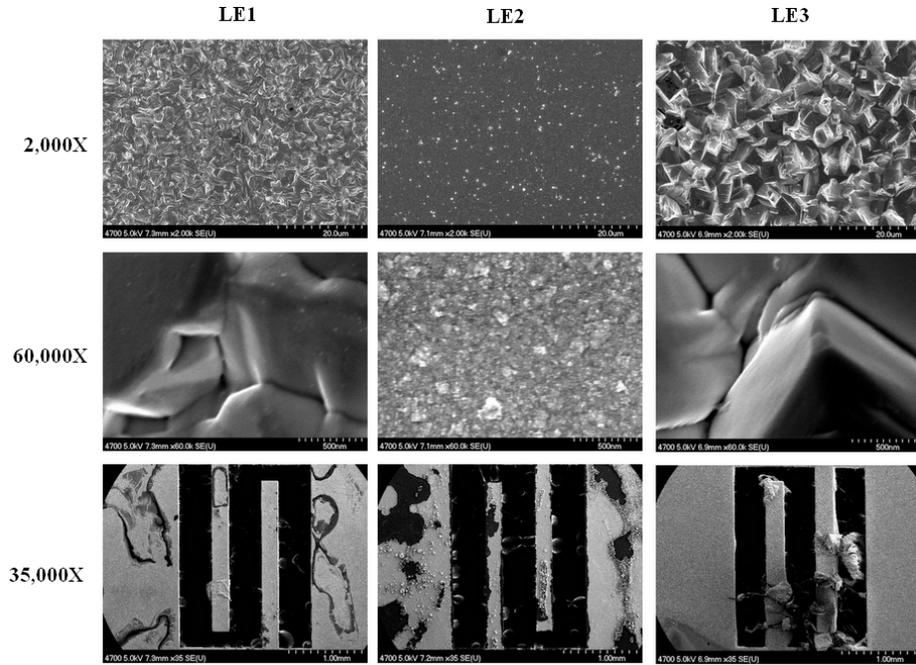
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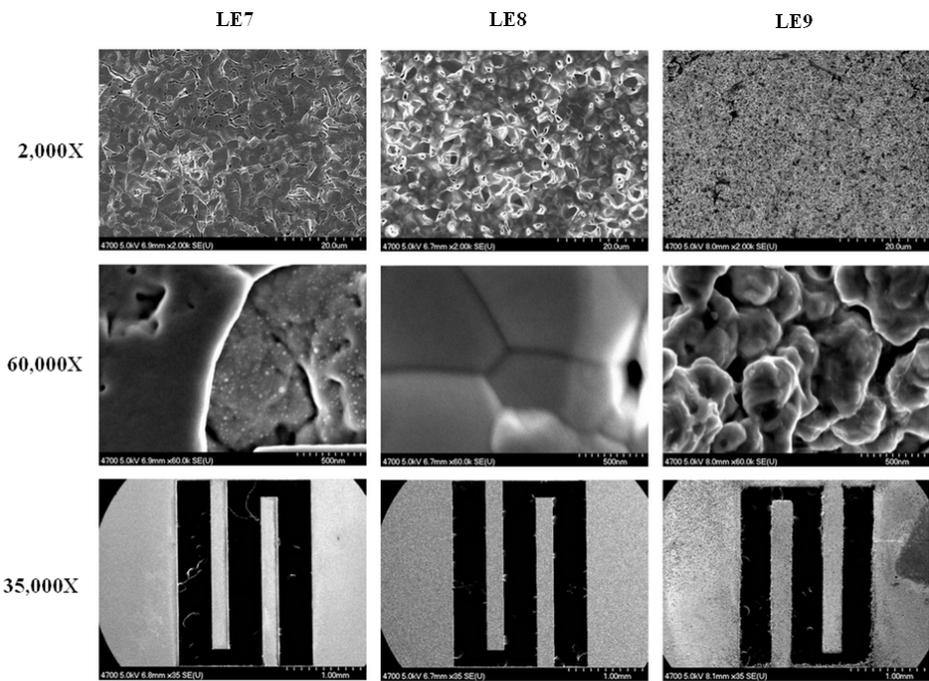
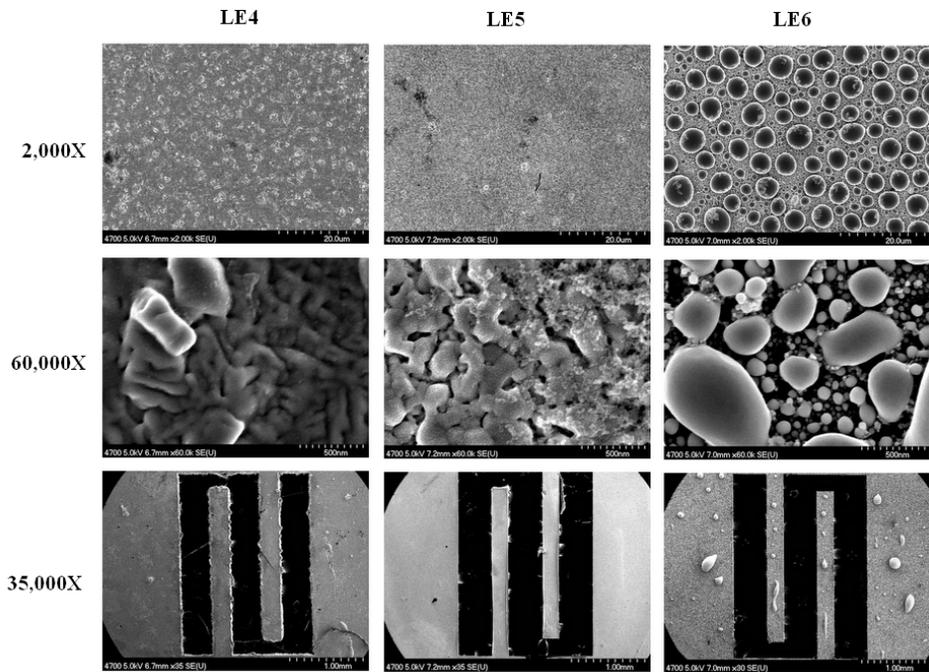


APPENDIX B

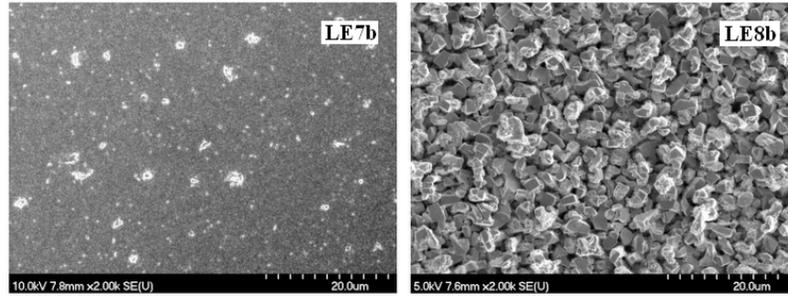
Scanning Electron Microscope (SEM) Images - Complete Catalog

LE Samples – 0 Weeks Old

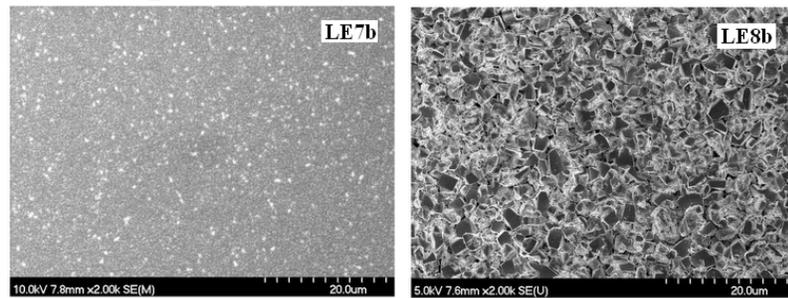




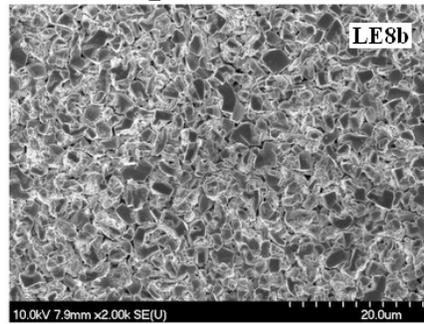
LE Samples 7b & 8b – 0 Weeks Old



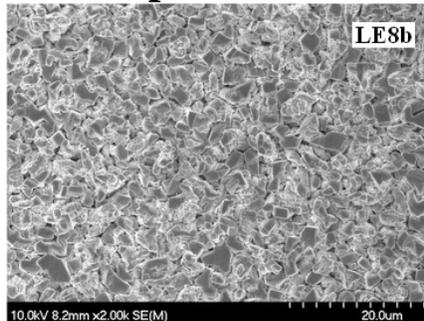
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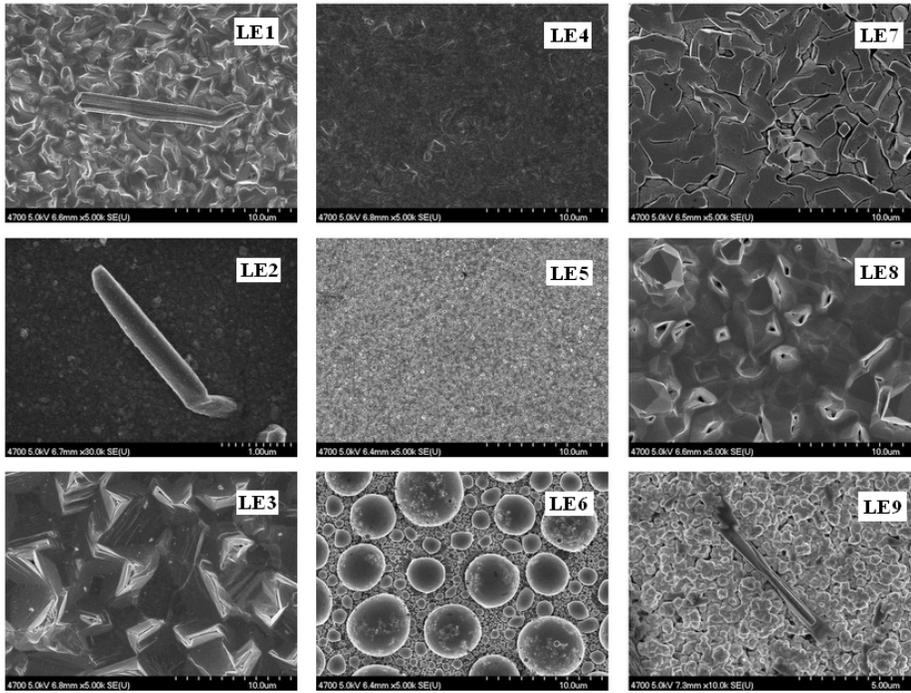
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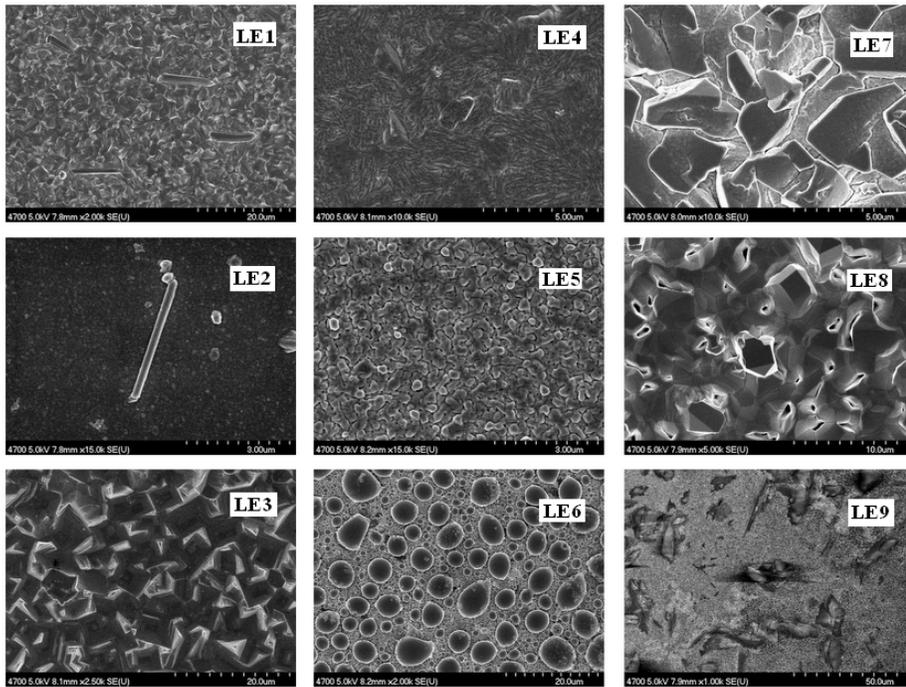
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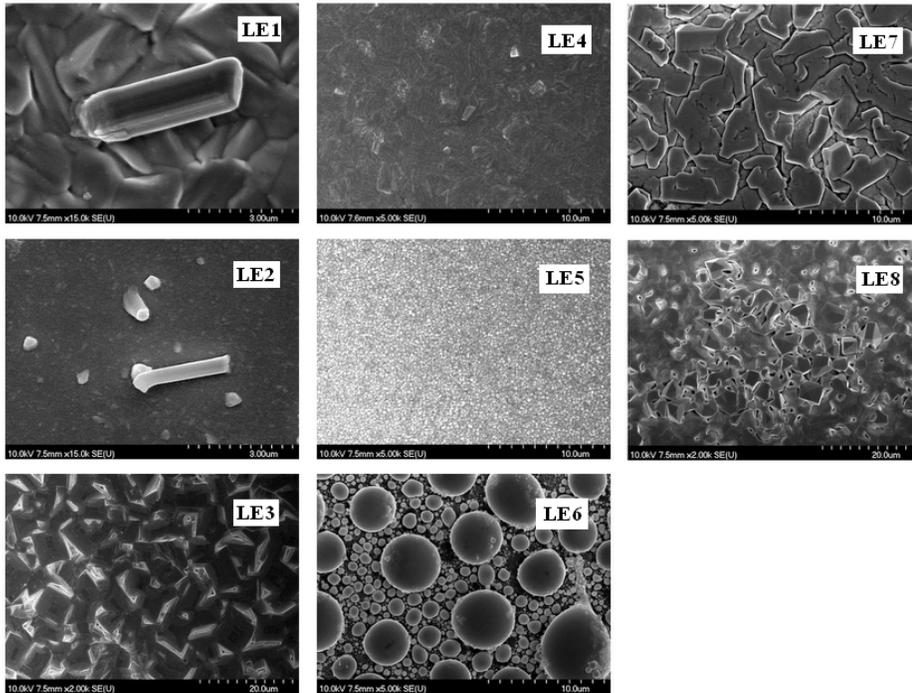
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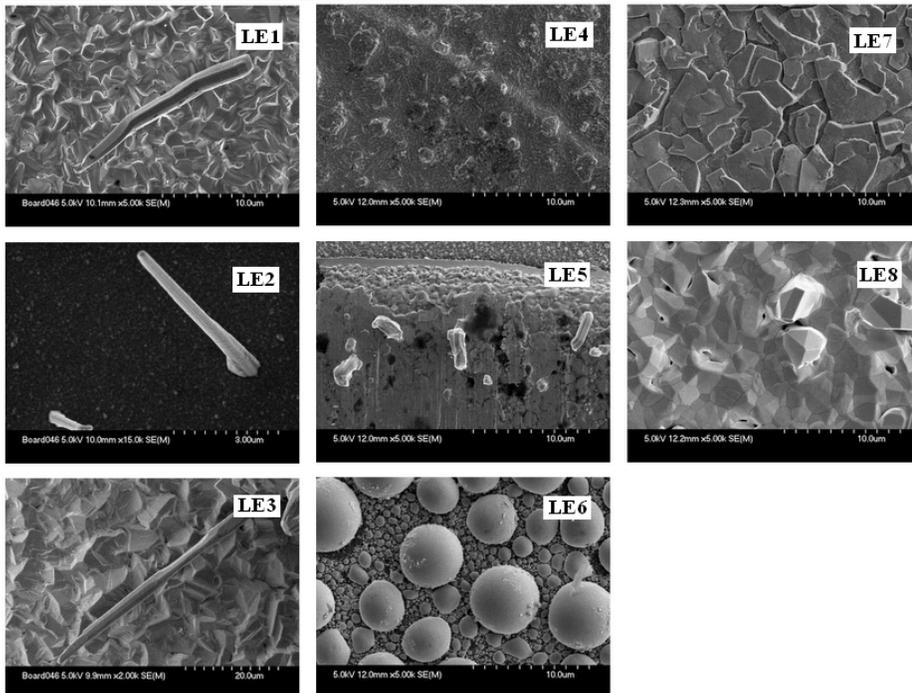
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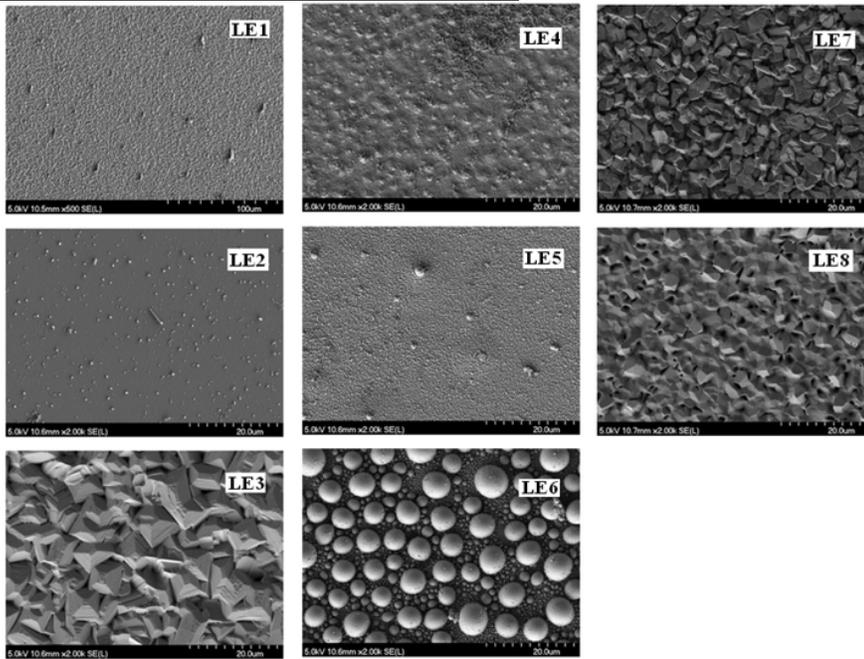
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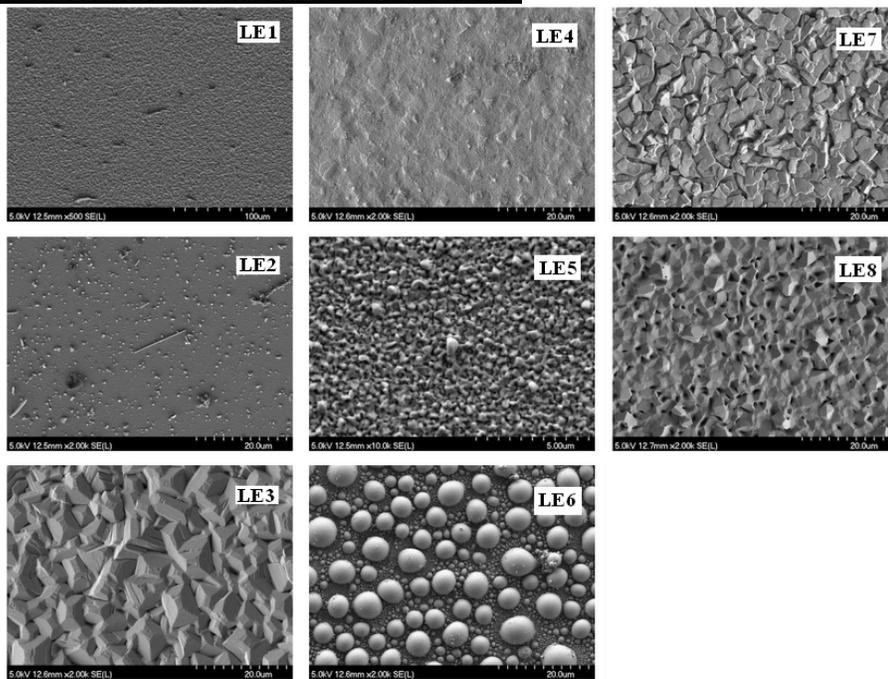
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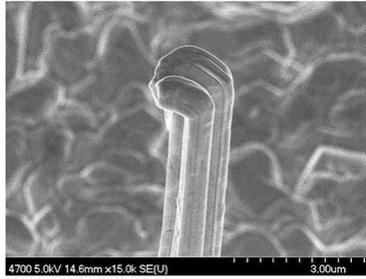
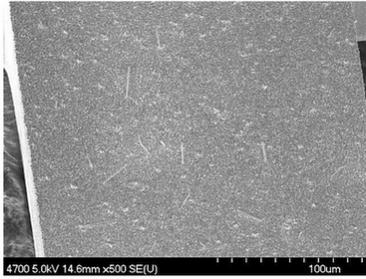
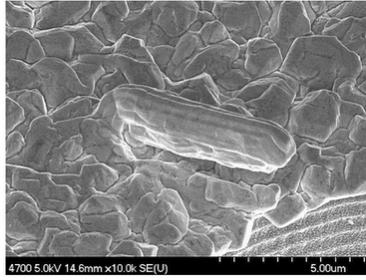
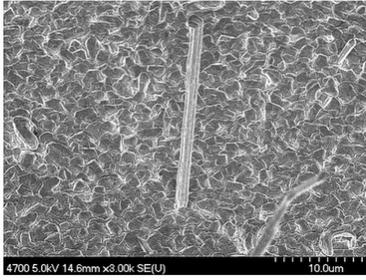
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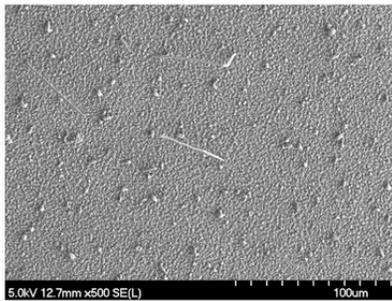
LE Samples – 50 Weeks Old



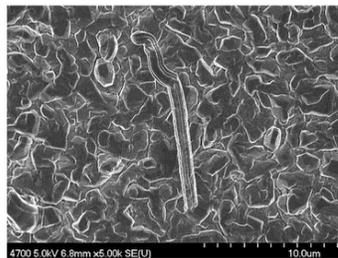
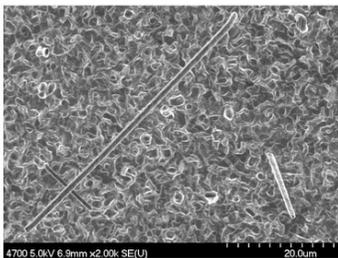
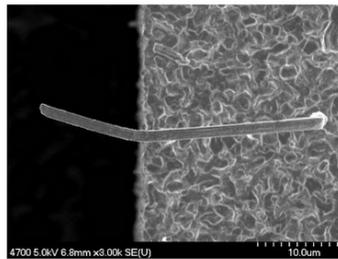
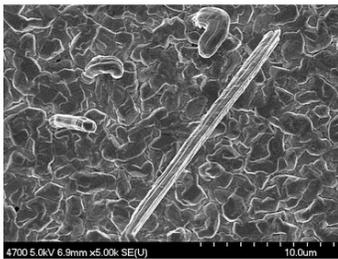
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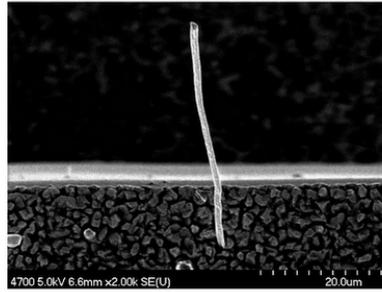
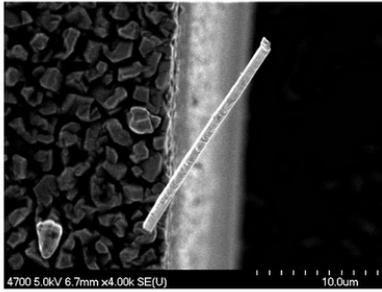
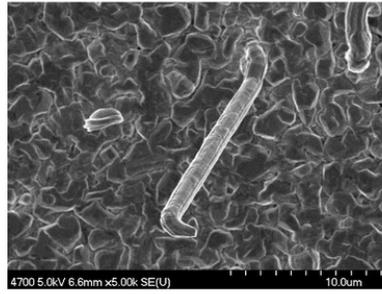
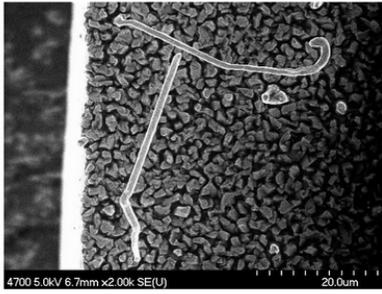
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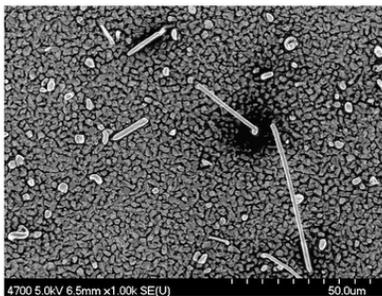
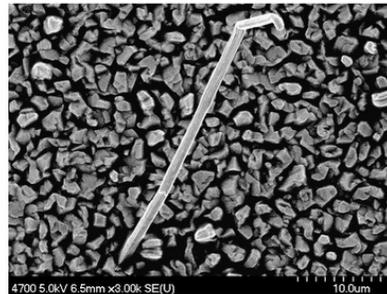
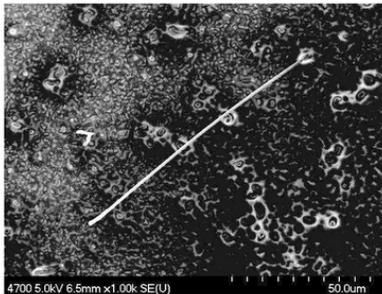
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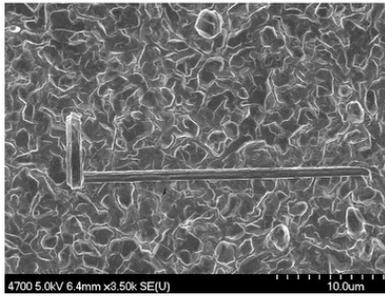
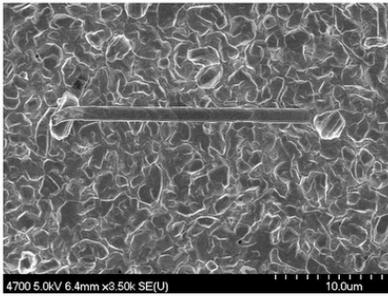
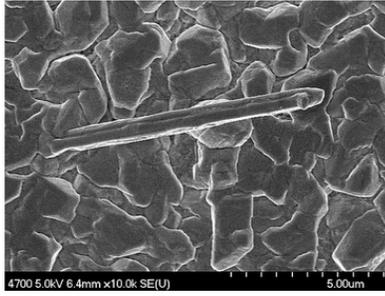
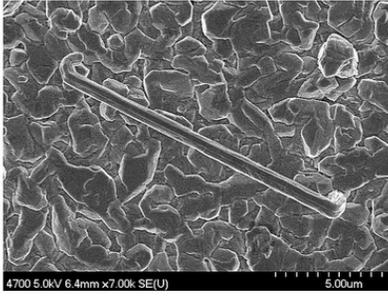
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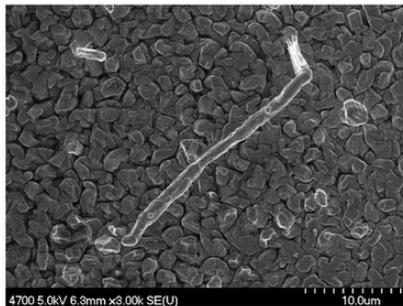
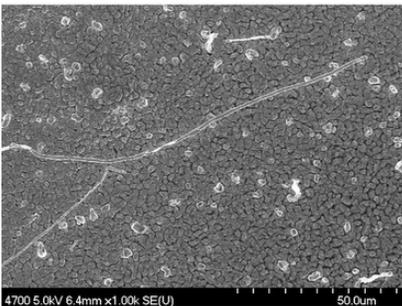
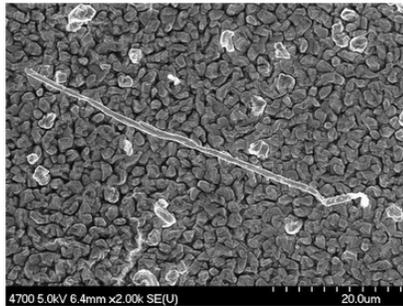
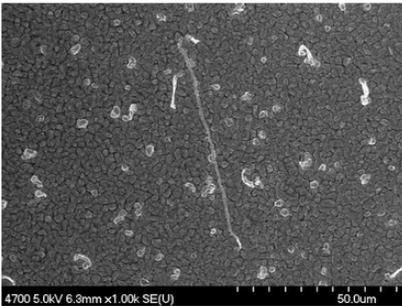
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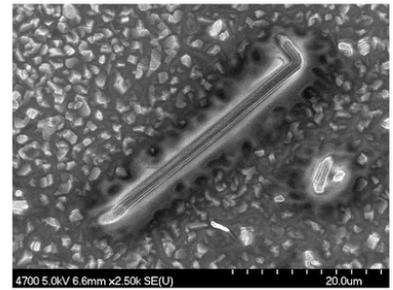
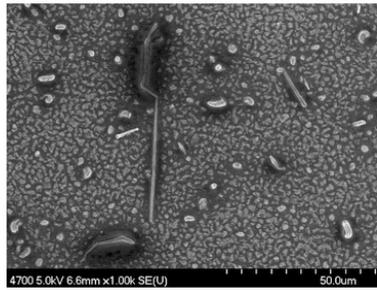
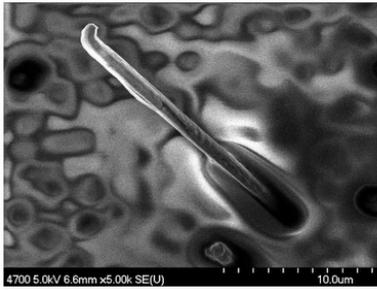
TH6



TH7



TH8



APPENDIX C

39th IMAPS SYMPOSIUM TRIP REPORT

Subject: Trip Report, IMAPS 39th International Symposium on Microelectronics,
San Diego Convention Center, San Diego, CA

Dates of Attendance: October 7-11, 2006

Introduction

The International Microelectronics and Packaging Society annual symposium provides the opportunity for its industrial and academic members (as well as other interested parties) to meet, exchange ideas, and conspire for continued success in an ever-changing climate of international redistribution and consumer demand. This year's conference, held at the San Diego Convention Center in California, featured 16 Professional Development Courses (PDCs), 6 technical tracks, and 180 vendor exhibitions. The symposium also included keynote speeches by Dr. Irwin Jacobs of Qualcomm and Col. Danny McKnight, retired former First Army Chief of Staff. I was originally scheduled to attend a workshop which focused specifically on Lead-Free Solder process implementation, however due to its last-minute cancellation I was instead moved into a 'Practical Electronics Reliability' workshop. Summaries of this workshop, along with overviews of the talks I attended within the Reliability Track technical program session, are provided below.

Professional Development Course S3

Practical Electronics Reliability – An Overview

This workshop, led by Andrew Kostic, PhD, provided a large body of background information and techniques pertaining to microelectronics reliability testing and statistical organization of test data. Our discussion began with an extensive listing of terminology and definitions meant to put everyone on the same ‘page’ for the remainder of the course. Distinctions were then made between the electronic and mechanical reliability life curves, and the basic computations of failure rates and identification of failure distributions (normal, lognormal, exponential, gamma, Weibull, and extreme value) were presented. Emphasis was placed on the notion that a thorough understanding must be achieved of the physics of failure (POF) for your device or application - for each given set of test conditions - before *valid* reliability testing can take place. The empirical relationship between activation energy (for a specific failure mechanism within a specific application), temperature, and failure rate, known as the Arrhenius equation, was described in detail, followed by a presentation of several common failure types in microelectronics testing, along with their background and causes, images, and relevant governing equations. A brief discussion was included regarding the implications of lead-free solder process implementation and the associated reliability concerns. It was asserted that there is an inherent reduction in a product’s mean time between failures (MTBF) when switching to lead-free materials. Furthermore, the claim was made that the existing models for leaded solder testing (or any other conceivable test paradigm, for that matter) are neither sufficient nor appropriate for computing valid reliability numbers,

primarily because our understanding of the POF (particularly of tin whiskering) is incomplete. The remainder of the workshop focused on the determination of confidence intervals, the modeling of system reliability (including how to project failure rates when taking into account multiple failure mechanisms), the choice of screening level (i.e., part level vs. system level, etc.), and the cost-benefit analysis of reliability testing as a practice. This workshop provided a good foundation for understanding how to approach reliability testing in microelectronics, and included a wide variety of useful reference materials.

Technical Program Papers

Session TA4

“Reliability and Microstructural Assessment of Hybrid CBGA Assemblies,” *Mark K. Hoffmeyer, Mukta Farooq, IBM Corporation.*

This work explored the reliability implications of using a mixture of, or ‘hybridized’, Pb-free (SAC) and Sn-Pb assembly technologies. The SAC alloy used in this work was the 95.5Sn-3.8Ag-0.7Cu composition, and was in ball form. Arrays of such solder balls were attached to FR4 test board using a Sn-Pb eutectic solder paste and subjected to a range of reflow profiles. The assembled modules were then thermally cycled and evaluated for failure behavior, microstructural integrity, etc. It was found that higher than normal reflow temperatures were needed for adequate homogenization of the SAC-SnPb junction (i.e., such that the mechanical stability at the interface was comparable to non-hybridized assemblies). Increased performance was also observed with longer dwell times at temperatures elevated beyond the liquidus-forming point. The metallurgy of the

assembled joints post-process (full interdissolution, pad plating dissolution, and IMC formation) was also described.

“Effect of Thermal Aging on Electrical Resistance of SnAgCu/Cu Joints,” *M. E.*

Marques, E. Monlevade, Nokia Institute of Technology.

This aim of this work was to investigate the correlation between electrical resistance and thermal aging of a circuit with daisy-chained CSPs attached using lead-free solder (Sn-3.7Ag-0.5Cu). Stress testing was done at 100°C and 125°C, for up to 1000 hours, and at 150°C, for up to 200 hours. Comparison measurements of the electrical resistance were made using a four-point technique on an LCR meter. Microstructure and intermetallic thicknesses were observed. Strangely, a near-perfect (~0.96) correlation was found between the incidence of the Cu₃Sn intermetallic and the decrease in electrical resistance (R), though the resistivity of Cu₃Sn is lower than any of the Cu- or Sn-containing elements of the starting solder material. Of the three known age-induced inhibitors of R, solder resistivity changes, IMC thickness changes, and Kirkendall voiding, the latter is said to have the greatest impact on electrical performance degradation.

“Lead-Free Die-Attachment with High-Temperature Capability by Low-Temperature Nanosilver Paste Sintering,” *J.G. Bai, J.N. Calata, et al., Virginia Polytechnic Institute and State University.*

A suspension containing nanoparticles of silver was used as an experimental means for high-temperature stable die attachment (desirable, for instance, for high-power silicon carbide devices). Naturally, this means of attachment is also ‘lead-free’. The

metallization sequence began with a direct-bond copper (DBC) layer, was then followed by electroless nickel (to protect the copper), a silver or gold plating (for adhesion), and the stencil application of the nanosilver paste. A 'low-temperature' sintering step was then performed (maximum temperature was 300°C), followed by an extensive battery of physical characterization tests. In most respects, the nanosilver paste (whose fired Ag density is >80%) performed comparably or better than common reflowed solders. In particular, its electrical and thermal conductivities and maximum use temperature were far superior.

“Board Level Reliability of High Density Flip Chip BGA with Large Die and Large Package,” *R. Chaware, L. Zhang, L. Hoang, Xilinx Inc.*

'Large' die (19 and 26mm) ball grid array (BGA) package assemblies were tested for reliability based on variability in lid/heat spreader adhesive choice, solder ball composition, lid shape, number and type of stacked layers, and board pad finish. Finite element modeling was used to generate a model for predicting the performance (bump stress and ball stress) of 'flat' and 'hat' lid configurations prior to stress testing of the actual devices. Thermal cycling for all samples was performed in air up to 100°C, and Weibull plots (cumulative failure % versus cycles to failure) were generated. Results indicated that, despite modeling evidence to the contrary, lid shape had no experimentally observed effect on the package reliability (nor did board pad finish). Lower t_g lid adhesives were found to delay failures (i.e., adhesive choice had an observable impact on the solder ball reliability within the FCBGA). Also, arrays which were lead-free were found to be more reliable than those which contained lead.

“Some Factors Affecting Voiding in Lead-free Solder Joints,” *G.J. Jackson, H.A.H. Steen, Henkel Technologies.*

In this study, several BGAs were constructed and their voiding levels compared based on variations in bond surface metallization (bare copper, organic surface protectant (OSP) coated Cu, immersion silver, and electroless nickel/gold (ENIG), and on variation in reflow profile. The solder used in this work was SAC387 (Sn-3.8Ag-0.7Cu), however two levels of flux composition (one containing SAC387, the other Sn-3.6Ag) were also investigated. Void quantification was performed using x-ray images of the reflowed ball arrays. The findings, common both to the surface metallization study as well as to the flux formulation study, revealed that when no copper was present, voiding was negligible, and as the level of copper increased (regardless of origin, and to a similar degree), so did the voiding. The proposed reason given for this was that SnAg aggregates are larger in the presence of Cu (in the form of ‘platelets’), thereby preventing trapped gases from escaping.

Session TP4

“Thermal and Mechanical Characterization of Lead Free Package with Organic Carrier for Server Applications,” *A. Sinha, IBM Server Development Group.*

This paper primarily documented an Ansys FEM simulation of the thermal and mechanical stresses experienced by a fully assembled lead-free package. The process flow involved soldering a processor chip onto an organic substrate using a lead-free BGA, underfilling at two attach levels, and mechanically leveling the package by fastening down the corners. Carrier deformations after underfill were modeled, as was

the load distribution across the package for a no-underfill assembly. A small experiment was also performed in which the failure rates for packages with and without underfill, after thermal cycling at 100°C, were compared. The findings were that underfill is beneficial from a mechanical and thermal reliability standpoint, and that better planarity (i.e., reduced warpage) results when the organic starting substrate is concave, rather than convex, in shape.

“Study of Ni-P/Pd/Au as a Final Finish for Packaging,” *D. Gudczauskas, UIC Technical Center, S. Hashimoto et al., C. Uyemura and Corporation, Ltd.*

As suggested in the title, the authors plated various NiP-Pd-Au finishes onto copper-clad laminate substrates either by purely electroless, by “electroless nickel electroless palladium immersion gold” (ENEPIG), or by ENEPIG with autocatalytic gold (ENEPIG-AG, or simply ENEPAG) means, in order to study the effectiveness of palladium as an intermediate blocking layer between nickel and gold (which interdiffuse readily) and the effect on reliability on SnPb and lead-free solder joints. Plating process and thicknesses, wire bond pull strength, location, and speed, and solder type were varied. Heat treatments were conducted in order to accelerate the occurrence of diffusion, and transmission electron microscopy (TEM), Auger spectroscopy, and scanning electron microscopy (SEM) data were gathered. The thickness value which agrees both with the requirement for good bond reliability as well as with the requirement for inhibiting nickel diffusion is 60nm. It was also found that the gold bond pad plating thickness (particularly with ENEPAG) must be adjusted based on the application specifications in order to achieve optimal reliability.

“Drop Test and Failure Mechanism of Sn-3.8Ag-0.7Cu and Sn-37Pb Solders in BGA Package,” *J.W. Jang, A.P. DeSilva, et al., Freescale Semiconductor, Ltd.*

This work compared failure modes based on drop tests for packages assembled using SnPb solder or using SAC (Sn-3.8Sg-0.7Cu) solder exclusively. Both solder-type BGAs were built using 200-micron balls on gold-plated nickel pads, however a comparison between nickel and copper under-bump metallizations (UBMs) was also made. Initial drop tests indicated that the SAC joints had significantly higher incidence of failure and joint compromise than the SnPb eutectic solder did. One explanation offered by this group was that, in instances of higher strain rates (as in drop testing), SAC becomes brittle rather than ductile (as it is at low strain rates). Its inability to elongate may be based on the formation of less-compliant Ag_3Sn IMC crystallites. Furthermore, the body-centered tetragonal crystallinity of Ag does not allow glide movement of dislocations (as does the face-centered cubic structure of lead). Copper UBM was shown to have a higher drop-impact resistance than that of nickel.

Conclusion

This was my fourth trip to an IMAPS symposium, and my third as a full member (non-student). I feel that attendance at such functions can benefit all professionals working in the broadly-defined electronics field, at any level, through exposure to the latest innovations and the reinforcement of industry standard practices. I continue to appreciate this organization’s priority of making opportunities available for, as well as promoting professional growth in, its professional members. I would be happy to loan

the proceedings on CD-ROM to any interested person. More information about the IMAPS organization and its events can be obtained at www.imaps.org.

APPENDIX D

CALCE TIN WHISKER SYMPOSIUM TRIP REPORT

Subject: Trip Report, Center for Advanced Life Cycle Engineering (CALCE)
International Symposium on Tin Whiskers, University of Maryland
College Park, MD.

Dates of Attendance: 24-25 April 2007

Introduction

The Center for Advanced Life Cycle Engineering (CALCE) held an International Symposium on Tin Whiskers on April 24th & 25th, 2007 at the Samuel Riggs IV Alumni Center, University of Maryland, College Park, MD. The symposium hosted 150 attendees, with representation from 6 universities, 80 corporations, 11 government agencies, and 15 different countries. Several highly regarded experts in the area of microelectronics reliability, including George Galyon of IBM, Tom Woodrow of Boeing, Bill Boettinger of NIST, Carol Handwerker of Purdue University, and Henning Leidecker of NASA GSFC, offered their perspectives on the status of lead-free viability, and presented their most recent work regarding tin whisker physics of failure. In all, 27 talks were given and 2 panel discussions were held. Highlights from several of them are presented below, followed by a brief discussion of the many calls for participation.

Metal Whiskering: Tin, Zinc, and Cadmium by Henning Leidecker GSFC/NASA

Dr. Leidecker began his talk with an historical overview of tin whisker awareness. He explained that common electronics materials, such as copper, steel, and brass, are reactive to ambient conditions and prone to corrosion. To combat such effects, beginning around the early 1940s, ‘protective,’ solderable surfaces of cadmium, tin, and/or zinc were commonly applied. Reports of failures due to electrical shorting of components caused by whisker (i.e., filamentary metallic surface protrusion) growth on many surface types – including the three already mentioned - began to emerge in 1946. These reports continued until the publication of Bell Labs’ S.M. Arnold’s 1959 paper extolling effective whisker mitigation by lead alloying (3-10% w/w), which gave way to decades of use of SnPb solders and finishes. The July 2006 adoption of the Restriction of Hazardous Substances (RoHS) directive by the European Union has brought about a renewed interest throughout the field in developing new alternatives to SnPb whose reliability can be established. Being that the mechanisms behind the process of whiskering have not, to date, been completely uncovered, many assembly facilities are reverting to finishes which remain potentially problematic. Despite the numerous early accounts of shorting failures caused by whiskering on pure Sn and Zn finishes, among others, as well as the abundance of modern-day catastrophes (i.e., NASA space shuttle transistor failure) whose root causes have been traced back to whisker shorts, these very finishes are still increasingly being employed today. Dr. Leidecker offered a number of possible explanations for the general lack of urgency in solving the tin whisker problem, including the persistent belief that whiskers are merely theoretical, or that the statistical incidence is low enough not to be of concern. In spite of the microelectronics

community's indifference, he maintained as imperative the need to continue its whisker research.

Prior to closing, Dr. Leidecker provided some information regarding certain statistical properties of whiskering (i.e., whisker density takes a Poisson distribution, while whisker length is lognormally distributed) as well as some data and formulae on the average melting temperatures of whiskers of various composition. He mentioned that dielectric breakdown of a whisker's native oxide (a necessary condition for establishing electrical contact) has been confirmed to occur within the range of 0.2V – 15V, and he also warned of the risk of generating ionized metal vapor – capable of sustaining very high electrical currents - within very small conductor gaps.

NIST Sn Whisker Research by W. J. Boettinger, et al, NIST

This talk began with a brief recounting of prior NIST works pertaining to tin whiskering as well as of current related efforts being pursued by NIST's Metallurgy Division. Several key material properties of electrodeposits were then discussed, in terms of their impact on the formation of tin whiskers, including intrinsic plating stress, interdiffusivity of Cu and Sn, intermetallic (IMC) formation and location, volume/compositional changes, creep tendency, and grain shape. A generalized theory for whisker formation was also presented.

Boettinger's group strongly advocates the use of the cantilever beam approach for stress measurement, and showed data suggesting that thicker deposits of bright Sn (1 micron thick or greater) contained greater compressive stress (while reminding us that '*intrinsic*' plating stresses can be either tensile or compressive). Deflection versus time

curves were presented, as a result of beam flexure experiments, for a range of deposit thicknesses and compositions, and approximate models for the behavior were also given. A positive relationship between copper content and both whisker incidence and maximum whisker length was claimed. Metallurgical data coupled with FIB cross-section images showed that the Cu_6Sn_5 intermetallic thickness which forms as a result of electrodeposition of pure Sn onto Cu is approximately proportional to $t^{1/2}$, with no intrusion into the tin grains or grain boundaries. Based on published data regarding the Cu/Sn and Cu/Cu-Sn diffusion couples and interdiffusion coefficients, Cu is purported as being a “fast diffuser” in pure Sn, however within the Cu_6Sn_5 IMC grains, Sn diffuses slightly more readily than does Cu. As such, it is theorized that a faster reaction takes place at the Cu/IMC interface, with a negative heat of mixing when compared to simple Sn/Cu mixing.

Microstructure information obtained from cross-sectional images of as-plated deposits of pure Sn, Sn with 2% Pb, and Sn with 3% Cu, revealed that for instances where hillocks and/or whiskers grew, columnar grains were present, while in the case of the lead-compensated alloy, there was an ‘equiaxed,’ small sized grain distribution. It was argued that, for an “equiaxed polycrystal,” stress relaxation would occur via grain shape modification rather than via forced filamentary outgrowth. On the other hand, creep (specifically, “diffusion creep,” or Nabarro-Herring-Coble creep) was mentioned as being an eligible contributor to whisker formation, when considering that a higher chemical potential is present on the grain boundaries *normal* to the stress than on those parallel to it.

Tracer Diffusion in Whisker-Prone Tin Platings by Tom Woodrow, Boeing

The objective of the work presented by Dr. Woodrow was to utilize non-radioactive isotopes of tin in order to track their diffusion with aging. Two different isotopes (Sn^{120} and Sn^{118}) were deposited, in single and double layers and having both bright and matte finishes, onto brass test coupons. After various incubation periods, FIB Microsection and Auger analyses were performed. 'Nodules' formed in bright finishes within 30 minutes of sectioning, while whiskers (allowed to grow for several days) were shown 'perched atop' grains along the matte plating surfaces. Secondary ion mass spectrometry (SIMS) depth profiles were performed on the double layers themselves (i.e., 'spot checks') as well as on their whiskers. A clear time-dependent interdiffusion was evident, along with the suggestion that the diffusion rate eventually slows to pseudo-equilibrium (i.e., only 1-2 time snapshots were provided). In all cases, it was found that the ratio of isotopes along the whiskers, from base to tip, was relatively constant. It was, however, also claimed that there is a gradient in the same ratio when measuring along the radial direction of the whisker (i.e., the core composition differs from that of the surface).

Tin Whisker Stress Measurement and Analysis by George Galyon, IBM

As perhaps the most published contributor to modern tin whisker inquiry, Dr. Galyon gave a thorough and engaging talk on the flexure beam (FB) thin film stress measurement technique. He opened the discussion by mentioning that the area of stress measurement is of particular interest to the Whisker “User” Group of the International Electronics Manufacturing Initiative (iNEMI), and listed cost, ease of implementation, access to high volume data, and a lack of publications using the technique (<5), as being among the benefits of using flexure beams. The basic assumptions involved with using FB methodology, as described by Dr. Galyon, are that your stresses reside in a two-dimensional plane, that the film strain is uniform along the normal direction, and that the Stoney stress equation accurately approximates the stress (by definition, Stoney’s equation is valid only for “thin film approximations,” in which the film thickness is <1% that of the substrate). Since FB analysis inherently results in some degree of experimental error, one may wish to consider finding ways to separate out the effects of IMC formation, stress gradients (both positive and negative), etc. As an example, Dr. Galyon has suggested that one might vary the film thickness across a number of experiments, in order to test the uniformity of film strain, or perform selective etches to determine the contribution of individual layers to the overall flexure. A “Complex Stoney’s” approach was also described, in which the flexure differential with and without tin would be used to determine the plating stress. Dr. Galyon went on to say that, were it possible to etch off the intermetallic without etching the underlying copper substrate, one could also make observations about IMC contributions to stress. He explained that certain material alternatives to copper, such as Alloy42 and tungsten, may enable such

analysis. Furthermore, it would be desirable to take into account Kirkendall effects (the temperature-driven movement of an interfacial marker, indicating the onset of diffusion) in FB testing.

To supplement his talk, Dr. Galyon handed out a small publication entitled “Residual Stresses in Thick and Thin Surface Coatings,” by T.W. Clyne, from the “Encyclopedia of Materials: Science and Technology,” Elsevier 2001.

Stress Relaxation in Sn, Sn-Cu, and Sn-Pb Films by Carol Handwerker and Aaron

Pedigo, Purdue University

Dr. Handwerker did an excellent job of summing up the prevailing presumptions regarding the variables involved in, and the necessary conditions for, tin whiskering. She enumerated several current and recent whisker study findings from Purdue, NIST, and Foresite, and also proposed a wide variety of possible directions for future inquiry. The following bulleted list provides an overview of her main points:

- It is generally held that increasing compressive stress contributes in a positive way to whisker formation.
- Creep is less prevalent than whisker formation as a stress-relief mechanism in thin films of Sn-3% Cu.

- Compressive stress does not increase with film thickness in SnPb, increases at a medium rate in pure Sn (forming hillocks), and increases at a fast rate in SnCu (forming whiskers).
- Intermetallic compounds, though commonly present in whisker-ridden parts, are not required for whiskers to grow (i.e., whiskers have been observed growing in the absence of an IMC layer).
- Hillocks and whiskers have been shown to form in spite of the existence of a Pt surface layer.
- The number, length, and type(s) of asperity formations on a SnCu surface change as a function of copper concentration.
- Contrary to prior belief, both bright *and* matte tin finishes can whisker.
- SAC305 solder can whisker.
- CTE mismatch, 'irregular' growth of IMCs, and oxidation/corrosion of Sn have all been shown to contribute to whiskering.

Dr. Handwerker's approach to solving the tin whisker problem gravitated consistently towards attempts to minimize the differences in material properties between SnPb and Pb-free solders.

Opportunities for Future Work

Despite the impressive quality and number of active research efforts focusing on the physics of formation of tin whiskers, there is widespread controversy and outright disagreement on a number of fundamental questions. Boettinger, et al, of NIST, for example, provided experimental evidence that a layer of oxide atop a tin plating surface is *not* required for whisker formation, however Chason, et al, of Brown, contends that it is in fact *critical*. Other points of contention include whether or not a finish must be bright (as opposed to matte), exhibit a columnar grain structure, have single-crystalline domains, or contain copper, in order to whisker. Because the tin whisker problem is far from resolved, there is a vast and diverse landscape of possible future directions for research. To this end, the CALCE symposium served a dual purpose, in terms of providing a forum for many of today's researchers to plead for greater involvement. Boettinger, et al, made note of a possible relationship between microstructure in plated films and the growths which subsequently form on their surfaces. Hence, it may be worth investigating ways to 'break up' an electrodeposit's grain structure as a whisker mitigation strategy. Dr. Galyon believes that more flexure beam experiment studies are badly needed. Dr. Handwerker posed the question "is there anything we can add to Sn to minimize its contact angle, thereby improving the solid-liquid interface segregation?" She also proposed comparing cantilever-based stress measurements with variation in Sn/Cu composition, and finding a way to 'disrupt' native oxide layers without using an

FIB (since Ga implantation, an unavoidable side-effect under normal circumstances, is problematic).

Conclusions

This was my first attendance at a CALCE event, and I was impressed to see such a high level of participation. In my opinion, attendance at such functions can benefit all professionals working in the broadly-defined electronics field, at any level, through exposure to the latest innovations and the reinforcement of industry standard practices. I feel that the information conveyed over the course of the 2-day symposium will be valuable to my dissertation work, and that the thin film testing and sample preparation techniques presented may prove useful in the context of my job. I would be happy to loan the proceedings (hard copy) to any interested person. More information about the CALCE organization and its events can be obtained at www.calce.umd.edu.

APPENDIX E

LEAD-FREE SOLDER WORKSHOP TRIP REPORT

Subject: Trip Report, Lead Free Solder Joint Reliability Workshop, instructed by Jean-Paul Clech, hosted by Hobbs Engineering, Boston, MA.

Dates of Attendance: 23-24 May 2007

Introduction

The purpose of this workshop, led by Jean-Paul Clech, was to discuss methods and considerations related to the determination of lead-free solder joint performance. Dr. Clech is an internationally recognized expert in the modeling of solder alloy systems, and has also done considerable legal and corporate consulting in electronics reliability. In his opening remarks, he informed us that the legally accepted definition of reliability is “the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels.” The implications of this definition were elaborated on throughout the twelve-part course. The first few segments focused on modern trends in microelectronics reliability, motivations for studying the physics of solder joint failure, and the overall subject of lead-free materials. The next few sections discussed matters specific to each of an assortment of package types (surface mount leadless, surface mount leaded, ball grid array, flip-chip, and chip scale packages), followed by two sections on the material properties of solder, two on experimentation and

modeling, and one section devoted to case studies. The following report provides a summary of the key lessons shared by Dr. Clech during this seminar.

Course Summary

To introduce the course, Dr. Clech provided us with a background on the composition of microelectronics solders prior to the European Union's adoption (in February of 2003) of the Reduction of Hazardous Substances Directive, which "restricts the use of six hazardous materials in the manufacture of various types of electronic and electrical equipment¹," among them lead (Pb). As is commonly known, 'near-eutectic' and eutectic tin-lead (SnPb) have been the most widely used solders for many years. As the movement towards "green" electronics progresses, however, there is renewed interest in lead-free alternatives, typically involving tin and/or tin alloys with silver, copper, bismuth, nickel, zinc, etc. The tin/silver/copper family (coined "SAC" solders) is perhaps the most popular of the alloy schemes, and a wide variety of ratios have been proposed thereof. Significantly challenging the institution of these replacement technologies is the limited degree to which their reliability has been characterized. Additionally, firm methodologies do not yet exist for testing such solders, as their properties vary too greatly from SnPb for the same tests to apply. Dr. Clech is of the opinion that for SAC387 and SAC 396 solders, which he considers to be the most heavily investigated of the SACs, we are no better than "18 to 30% up the learning curve," and worse that we have only a 5% understanding of SAC305. Failure mode acceleration factors (AFs), for example, are not available for many formulations of lead-free solder. Clech himself spent a full 5 years compiling AF

models for thermal cycling and vibration in SAC 387/396. In addition to time, cost is a major impediment to progress in these areas, particularly considering that a “good” creep test runs about \$150k.

Because temperature is the leading cause of electronic failures, followed by vibration, Dr. Clech stressed to us that thermal cycling tests are extremely important in reliability determination. He mentioned a useful relationship in appraising the nature of thermally-induced solder fatigue, which states that for materials operated at less than 0.4 times their melting temperature, the dominant deformation mode is reversible, elastic stretching, while those materials which operate at or above 40% of their melting temperature under load will deform via non-reversible creep. The ratio of operating temperature to melting temperature is also known as the ‘homologous’ temperature, and both SnPb and SAC solders have homologous temperatures greater than 0.6. Both solders are therefore susceptible to metallurgical creep at ambient temperatures. Interestingly, Dr. Clech explained that thermal cycling tests and beam flexure mechanical tests are in fact *equivalent* by the following expression, with the latter test being considerably faster and simpler to perform:

$$R = \frac{h}{\Delta\alpha \times \Delta T}$$

, and where R is the radius of curvature, h is the beam thickness, $\Delta\alpha$ is the CTE mismatch (i.e., finish/substrate or component/substrate), and ΔT is the change in temperature

(modeled, in this case). Similarly, equivalence exists between thermal cycling tests and power cycling tests when it comes to high-power integrated circuit assemblies.

It is clear that endeavors in solder joint reliability evaluation, a “semi-empirical science,” should attempt to take into account a wide variety of factors, enumerated by Dr. Clech to include three-dimensional and time-dependent stress and strain histories, non-linear, temperature, and time-dependent mechanical properties of solder, metallurgical considerations (such as intermetallic compounds, grain size, and aging), failure mechanisms (such as coarsening, matrix creep, and grain boundary sliding), and the intermittent nature of solder joint failures. *Global* CTE mismatch is important when evaluating leadless assemblies, while *local* CTE mismatch is a more legitimate concern for leaded assemblies. From a materials standpoint, CTE are better matched between SnPb and Cu substrates than for SnPb and Kovar or SnPb and ‘Alloy 42’ (Ni/Fe). It was noted that, despite the “standardized” manufacture of FR4 circuit boards, the *actual* CTE of a vendor supplied board may differ from its specified value, and can vary over a rather large range (9-24 ppm/°C). Furthermore, specially treated FR4 boards capable of withstanding the elevated temperatures required for SAC solder processing are now available, and the variability among their CTE is not well established. Irrespective of die size, as packages have scaled down to occupy smaller footprints, assembly Safety Factors (the ratio of ‘time to failure’ to ‘design life’) have diminished. While plated through-hole (PTH) technologies have typically allowed for an SF of ~10, modern chip-scale packages (CSPs) have SFs around 1.5.

A number of comparisons between SnPb, SAC, and SnCu solders were made throughout the course, often in terms of their ‘characteristic lifetimes’ with respect to various external factors. SnPb displayed a longer expected life when subjected to high shear strain, high temperature conditions, and/or longer dwell times during thermal cycling, when compared to SAC. The two solder types were found to be comparable, in terms of pull strength versus number of thermal cycles, in quad flat packs with either NiAu or organic solderability preservative (OSP) finishes. The general statement was made that “SAC is stiffer (higher E),” “has higher yield stress (σ_e) and strength (max. stress),” and is “more creep resistant” than its SnPb predecessor. Also, unlike SnPb, the coefficient of thermal expansion (CTE) of SAC is somewhat temperature dependent, although at ambient temperatures the two are roughly equal (~23-24 ppm/°C).

When advising us on how to perform predictive reliability work, Dr. Clech stressed the importance of in-house determination of the material properties (i.e., CTE, Poisson Ratio, etc.) and strain data for *all* components of the assembly under scrutiny (i.e., the board material, solder mask, package, solder joints, metallizations and coatings, etc.). The list of suitable inputs to a design of experiment (DOE) for such purposes is similarly long, and includes aspects of the assembly process itself, the volume of solder used, geometry and orientation of pads, traces, components, and die, and part vendors. Because one is generally interested in streamlining reliability test efforts as well as in making good lifetime predictions and pinpointing accurate test AFs, it is viewed an economical choice to develop experimental models along the way. Clech indicated

particular confidence in those life prediction models which are based on a “strain-energy criterion,” since they have correlation values similar to those of SnPb models, and he also provided formulae and descriptions of the Norris-Landzberg, Pan/HP, and Solder Reliability Solutions models. Strain energy is defined as the amount of energy absorbed by an item under load prior to fracture, and corresponds to the area under the stress-strain curve (also known as the ‘toughness’). The practice of validating models is strongly encouraged, by way of making comparisons to internally-generated datasets. In order to fully develop a reliability model, Dr. Clech feels that around 4 dozen such datasets are required, in addition to detailed test vehicle information, a constitutive model for solder joints, and wide-range failure distributions from accelerated testing (“covering 2-3 orders of magnitude in life”). To help maximize the efficiency of our reliability tests, he also provided optimal ramp rates and dwell times for SAC and SnPb solder thermal cycling tests.

Conclusion

In his Lead-Free Solder Joint Reliability workshop, Dr. Clech provides the background knowledge, insight, and fundamental modeling principles necessary for informing the formulation and launch of an independent series of reliability tests. Much of the information conveyed was germane to TSD’s in-house lead-free solder initiative, and is likely to directly and positively impact our progress. I would be happy to loan the proceedings (hard copy) to any interested person. More information about Jean Paul Clech and his company, Electronics Packaging Solutions International, Inc. (EPSI), can

be accessed at <http://www.jpclench.com/ClechBio.html> and
<http://www.jpclench.com/index.html>, respectively.

APPENDIX F

PART REPROCESSING SYMPOSIUM TRIP REPORT

Subject: Trip Report, CALCE Symposium on Part Reprocessing, Tin Whisker Mitigations, and Printed Wiring Assembly Rework/Repair

Dates of Attendance: 11-12 November 2008

Introduction

The Restriction of Hazardous Substances Directive (RoHS) adopted by the European Union in 2003 mandates the elimination of six toxic substances from electronics: **lead**, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, and polybrominated diphenyl ether. Removing lead from plated finishes and solders inevitably leads to the pervasive and unpredictable problem of spontaneous “tin whisker” growth, a plague of microscopic metal protrusions which can cause – indeed has caused – catastrophic failures across a breadth of applications. Of particular note is the fact that military, space, and medical industries no longer enjoy market dominance when compared with consumer electronics, and as such, despite RoHS “exemptions” allowing them to use lead in many cases, the availability of lead-containing components from suppliers has become increasingly difficult or even impossible. Firms are attempting to “stopgap” their parts supply by purchasing whatever remaining available lead-containing components they can find, but this is clearly only a temporary fix.

The Center for Advanced Life Cycle Engineering at the University of Maryland held a symposium in College Park, MD on November 11th and 12th devoted to “Part Reprocessing, Tin Whisker Mitigations, and Printed Wiring Assembly Rework/Repair.” This two-day meeting, which hosted over 100 attendees from 55 agencies, corporations, and universities, sought to address a number of concerns relating to the lead-free push and implications affecting all tiers and supply chain elements within the electronics industry. Presentations addressed whisker risk assessment, whisker mitigation techniques, physics of failure studies, rework of lead-free assemblies, ‘counterfeit’ part detection, and/or conversion of lead-free parts back to lead-containing parts (e.g., BGA reballing, component lead refinishing, etc.). This report summarizes the salient communications from this event.

Notable Papers

“GEIA Standardization Activities Related to Lead-Free Materials,” Anduin Touw

(Boeing)

A classification system has been developed by the Government Electronics and Information Technology Association (GEIA), which aids high-reliability industries in defining application-specific risk control mechanisms regarding tin whiskers. Each classification level (1, 2A, 2B, 2C, and 3, in order of increasing tin avoidance) specifies the level of tin documentation, detection and control, mitigation, and risk analysis required for a given task. Several audience members make remarks relating to their own implementation and use of these GEIA designations. GEIA also works with JEDEC in developing lead-free related standards and guidances.

“CALCE Study on BGA Reballing,” Lei Nie (CALCE)

Two reballing techniques were studied (solder wick ball removal followed by preform ball application, and low temperature wave solder ball removal followed by preform ball application), in which lead-free tin-silver-copper (SAC) solder balls were removed and tin-lead (SnPb) solder balls were placed onto plastic ball grid arrays (BGAs). Reballed assemblies were compared with non-reballed (SAC) assemblies, where both types were aged under 3 different sets of conditions, and then failure tested by ball shear, cold bump pull, and four-point bend. Results indicated that solder ball strength and overall assembly durability is similar in lead-free and mixed solder assemblies, with both outperforming reballed assemblies by a large margin. Ball strength was not significantly affected by the ball removal method selected, assembly durability (based on bend tests) was higher when the solder wick ball removal process had been used, rather than the low-temperature solder wave method.

“BGA Reballing Reliability,” Ray Cirimele (BEST)

In this study, control (non-reballed) BGAs were compared with otherwise identical single-reballed and double-reballed assemblies, the latter intended to simulate additional rework. Extensive electrical tests, including base loopback, memory, flash, script, SRAM and top loopback, were performed, revealing that the reballing process does not have an appreciable effect on the BGA integrity. It was also stated that, while the extra thermal exposures associated with second reballing events did not appear to

detriment the assembly's operation, temperature profiles showed that solder wicking subjects BGAs to less cumulative heat than using a solder fountain.

“An OEM Perspective on BGA Reballing,” Michael Davisson (Agilent)

Agilent, formerly HP Test & Measurement, performed 1000 thermal cycles on reballed video adaptor BGAs, periodically inspecting and testing them alongside a set of lead-containing control samples. The study found that ball shear, coefficient of thermal expansion (CTE) perforation, vibrational cracks and shock-induced failures were comparable in both sample groups. The only noted physical difference between the reballed and leaded BGAs was the thickness of the intermetallic layer (~50% higher when reballed). The company plans to use reballing as their primary means of tin whisker mitigation, and may also consider “mixed metal soldering” – the combining of lead-free and leaded chemistries, as available - in the future, contingent upon more research into its reliability.

“Manual Pretinning of COTS Components,” James Lake (Lockheed Martin)

“Retinning” refers to the process of dipping the plated terminations of a component into a molten solder (having a different composition than the original finish), in order to replace the original tinned layer with a new tinned layer. A method for manually retinning lead-free “commercial off-the-shelf” (COTS) parts into SnPb solder - with better depth control and prevention of bridging - was described. The process modifications discussed included utilizing a smaller-than-normal solder pot beneath a

microscope (for better viewing of smaller parts and the depth of the dip) and floating a ~50-mil thick layer of water-soluble flux atop the molten solder, since “dipping through flux was found to decrease solder bridges between leads.” As of the presentation date, Lockheed Martin Systems Integration Oswego had already used this reflowing technique on ~3500 piece parts.

“Tin Whisker Containment with Flexible Ceramic Conformal Coatings,” Ofer Sneh
(Sundew Technologies)

This paper was, in my opinion, the most remarkable of this conference, and seemed to have been largely overlooked by those in attendance! Sundew Technologies specializes in atomic-layer deposition (ALD) based conformal coatings which they believe can be 100% effective at containing tin whiskers. Their coatings are “tunable” in terms of flexibility, corrosion-resistance, % elongation to failure, and hermeticity, and can form tensile layers with extremely strong bonds to tin surfaces, providing an advantage over traditional encapsulants like Parylene C and Uralane 5750. Extensive accelerated aging tests on whisker-free and already whiskered surfaces were performed, and perfect mitigation was demonstrated over 24 weeks. The cost for “ALD-capping” is currently \$30-50 per square foot of printed circuit board, and Sundew anticipates a reduction in cost to \$10-15/sq ft in the near future.

Conclusions

The CALCE Symposium on Part Reprocessing, Tin Whisker Mitigations, and Printed Wiring Assembly Rework/Repair was a productive success. It was both encouraging and reassuring to see such a high level of active participation in this important field, and to confirm that the challenges faced by lead-free researchers are very much “shared” challenges. I feel that the information conveyed over the course of the 2-day symposium will be valuable to my work on the “Lead-Free Reliability” technical initiative. I would be happy to loan the proceedings (hard copy) to any interested person. More information about the CALCE organization and its events can be obtained at www.calce.umd.edu.

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CURRICULUM VITAE

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EDUCATION

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The Carey Business School, Johns Hopkins
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M.S. Electrical Engineering, August 2004.
Northern Illinois University, DeKalb, IL.

B.S. Electrical Engineering, August 2004.
Northern Illinois University, DeKalb, IL

B.S. Operations Management and Information Systems,
Magna Cum Laude, May 2001. Northern Illinois
University, DeKalb, IL.

U.S. Army Aircraft Electrician School, October 2002.
Fort Eustis, VA.

U.S. Army Primary Leadership Development Course,
Commandant's List, July 2004. Camp Cook, LA.

CURRENT INVOLVEMENT

Currently involved in microelectronics process engineering and related research & development. Responsible for the execution of fabrication standard processes and procedures (FSPP's) within the Engineering, Design, and Fabrication branch of the Technical Services Department at JHUAPL. Proficient in deep reactive ion etching, reactive ion etching, resistive evaporation, electron-beam evaporation, DC,

pulsed DC and RF sputtering, surface profilometry, optical interferometry, photolithography, wet etching of metals and dielectrics, ellipsometry, thermal oxidation of silicon, electrochemical analysis and synthesis, carbon dioxide lasing, wafer sawing, and laser stress measurement of silicon. Current research relates to nanoporous anodized aluminum, thin film appliqué, tin whisker physics of failure, and microtoroidal calcium fluoride optical structures. Past activities have included the development of an in-house process for growing metallic and multicomponent nanowires, processes for deep reactive ion etching (DRIE) based fabrication of Bradbury-Nielsen particle gates, the electrochemistry-based fabrication of freestanding nanoporous silicon dioxide, alkaline-based anisotropic etching for silicon texturization, and the handling and characterization of silica aerogel membranes.

ACADEMIC EXPERIENCE

2003-2004. Graduate Research Assistant, Northern Illinois University, DeKalb, IL.

2002 (Fall). Graduate Assistant/Supervisor, Northern Illinois University, DeKalb, IL.

MEMBERSHIPS AND HONORS

- National Merit Scholars (Commended Student)
- Johns Hopkins Women's Network Leadership Award Nominee
- MENSA (Member)
- Illinois State Scholar
- Golden Key Honor Society (Invitee)
- Toastmasters (Member)

RESEARCH INTERESTS

Lead-Free Process Development, Nanoscale Materials, Microelectronics Reliability, Semiconductor Device Physics

PUBLICATIONS

"Process Optimization for the Pulsed Laser Deposition of Perovskite Thin Films," L. A. McAnelly, M.S. Thesis (2004).

"Advanced Materials Development, Processing, and Analysis: Applications in Microelectronics and Electronic Packaging," H. K. Charles, Jr., and L. A. McAnelly, IMAPS Symposium Proceedings (2005).

“Contribution of Oxygen Partial Pressures Over a Wide Range to SrRuO₃ Thin Film Properties in Laser Deposition Processing,” Y. Z. Yoo, L. A. McAnelly, et al., Journal of Applied Physics, 97 (2005).

“Effects of Ru Vacancies and Oxygen Synthesis Pressures on the Formation of Nanodomain Structures in SrRuO₃ Thin Films,” Y. Z. Yoo, L. A. McAnelly, et al., MRS (March 2005).

"Electrochemical, Template-Based Synthesis of Metallic and Multicomponent Nanowires," McAnelly, L., Srinivasan, R., Lennon, A., presented at the IMAPS (International Microelectronics and Packaging Society) Emerging Technology Workshop: Nanotechnology for Microelectronics (December 2006).

"In-Situ Generation of Nanowires of Active Chemicals Within Nanopores of Membrane Electrodes for Paper-Thin Micro Battery Applications," L. A. McAnelly, A. Lennon, R. Srinivasan, presented at the IMAPS (International Microelectronics and Packaging Society) Emerging Technology Workshop: Nanotechnology for Microelectronics (December 2006).

“Self-Assembly Based on Chromium/Copper Bilayers,” P. Tyagi, N. Bassik, T. G. Leong, J. H. Cho, B. R. Benson and D. H. Gracias, IEEE/ASME Journal of Microelectromechanical Systems (JMEMS) (2009) accepted.

“Physical Vapor Deposition and Patterning of Calcium Fluoride Films,” L. McAnelly, K. Rebello, K. Caruso, A. S. Francomacaro, G. L. Coles (2009, pending publication).

“Effects of Tin Deposition Method on Tin Whiskering,” L. McAnelly, J. Melngailis, H.K. Charles, D. Lee, R. Deacon, G. Coles (2009, pending publication).

**CONFERENCE
PROCEEDINGS**

● “Advanced Materials Development, Processing, and Analysis: Applications in Microelectronics and Electronic Packaging,” H. K. Charles, Jr., and L. A. McAnelly, IMAPS Symposium Proceedings (2005).

- "Electrochemical, Template-Based Synthesis of Metallic and Multicomponent Nanowires," McAnelly, L., Srinivasan, R., Lennon, A., presented at the IMAPS (International Microelectronics and Packaging Society) Emerging Technology Workshop: Nanotechnology for Microelectronics (December 2006).
- "In-Situ Generation of Nanowires of Active Chemicals Within Nanopores of Membrane Electrodes for Paper-Thin Micro Battery Applications," L. A. McAnelly, A. Lennon, R. Srinivasan, presented at the IMAPS (International Microelectronics and Packaging Society) Emerging Technology Workshop: Nanotechnology for Microelectronics (December 2006).
- "Electrodeposited Bismuth-Gold Heterojunction Nanowires for Gamma Radiation Spectroscopy," Hoffmann, J., Monica, A., Papadakis, S., McAnelly, L., Nanoelectronic Devices for Defense & Security Proceedings (September 2009).
- "Template-Assisted Electrodeposition of Bismuth Nanowires for Electronic Applications," Monica, A.H., McAnelly, L.A., Baird, L.M., Deacon, R.M., Papadakis, S.J., Hoffman, J.A., Proceedings of the Materials Research Society Spring Meeting (accepted for Spring 2010).

REVIEWED JOURNALS

Microelectronics Journal
Microelectronic Engineering

SERVICES

- Tutor for special needs student (2003)

OTHER PROFESSIONAL EXPERIENCE

- Sergeant, *US Army Aviation (A. Co., 1/224 AVN, Edgewood, MD)*

PERSONAL AND HOBBIES

Enjoy art (painting, sketching, photography), endurance athletics, films, and international travel.