ABSTRACT

Title of dissertation: CORRELATION OF SIGNALS, NOISE, AND HARMONICS IN PARALLEL ANALOG-TO-DIGITAL CONVERTER ARRAYS

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Combining M analog-to-digital converters (ADC) in parallel increases the maximum signal-to-noise ratio (SNR) by a factor of M, assuming the noise is uncorrelated from one channel to the next. This allows for a significant increase in SNR over a single ADC; however, noise and harmonic correlation degrade this improvement. ADCs have three sources of noise: thermal (and other random physical processes), sampling, and quantization noise. There are two system components creating harmonics: the sampler and the quantizer. In this thesis, I determine, analytically and experimentally, the degree of correlation between signals, noise, and harmonics in a parallel ADC array.

To test the analysis experimentally, I developed a 16-channel test-bed using

16-bit, state-of-the-art ADCs and 16 direct-digital synthesizers as low-noise signal sources. The test bed provides excellent signal isolation between channels and minimal digital noise to enable the measurement of very low levels of correlation. I investigated the feasibility of measuring the very high levels of signal correlation in the presence of channel nonlinearities with different measurement signals. For a completely linear channel, the channel matching is limited by noise. With nonlinearities, the ability to measure the signal correlation depends on the measurement signal. I verified that the thermal noise is uncorrelated across 16 channels as expected. I also demonstrated that sampling noise is fully correlated from channel-to-channel when a common clock drives the ADCs. Efforts to reduce the correlation using two previously developed de-correlation techniques-phase randomization and frequency offsets-successfully reduced the correlated noise by a factor of two. I then demonstrated analytically and experimentally that harmonics from quantizers are largely uncorrelated; however, harmonics from the sampler are largely correlated confirming the need for decorrelation techniques. I demonstrated the impact of the previously developed decorrelation techniques to reduce harmonic correlation and developed two new decorrelation techniques: phase cancellation and clock offsets, which offer significant advantages over phase randomization and frequency offsets. Each technique offers different levels of dynamic range improvement and complexity, allowing for a range of techniques to target the optimal level of decorrelation.

Correlation of Signals, Noise, and Harmonics in Parallel Analog-to-Digital Converter Arrays

by

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Dedication

I dedicate this dissertation to all my C(K)atherine's for all their support.

Foreword

The student made substantial contributions to the relevant aspects of the jointly authored work included in the dissertation.

Acknowledgments

I want to acknowledge the following efforts: George Vetticad, Al Wu, and Joe Sluz for helping design, assemble, and troubleshoot the various test beds; Cesar Lugo and Laura Ruppalt for helping me with my writing; Salvador Talisa for reviewing all of my writing; Ken O'Haver, my business area, and JHU Applied Physics Laboratory for support; and my advisor Martin Peckerar for supporting this collaboration.

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List of Abbreviations

ADC	Analog-to-digital converter
SNR	Signal-to-noise ratio
RSS	Root-sum-square
DDS	Direct-digital synthesizer
CPCR	Channel-pair cancellation ratio
IF	Intermediate frequency
RMS	Root-mean-square
SFDR	Spur-free dynamic range
PSD	Power Spectral Density
DFT	Discrete Fourier transform
IDFT	Inverse discrete Fourier transform
LO	Local oscillator
PDF	Probability density function
LSB	Least significant bit
AAF	Anti-aliasing filters
MSPS	Millions of samples per second
FPGA	Field-programmable gate array
DAC	Digital-to-analog converter
NF	Noise figure
EMI	Electromagnetic interference
EIRN	Equivalent input referred noise
INL	Integral Nonlinearity
DNL	Differential Nonlinearity
LFM	Linear frequency modulation
BLGN	Band-limited Gaussian Noise
ITOI	Input third order intercept
RF	Radio frequency
MOSFET	Metal-oxide semiconductor field effect transistor
AWGN	Additive white Gaussian noise

Chapter 1

Introduction

Analog-to-digital converters (ADC) limit the dynamic range of many sensor, test and measurement, and communication systems [3, 4, 5, 6, 7]. Despite increases in ADC dynamic range over time [8], many of these systems would benefit from greater dynamic range capabilities. Since ADC performance gains arise from advances in underlying circuit techniques and semiconductor process advances, improvements in ADC performance are likely to plateau as silicon's limits are reached, much as microprocessor clock speed has stagnated [9]. Both of these concerns necessitate moving toward parallel ADC array architectures for performance gains, as microprocessors have. Parallel ADC arrays allow a substantial increase in the dynamic range relative to a single ADC; however, the impact of signal, harmonic, and noise correlation on a parallel systems has been little studied and may potentially limit the system dynamic range with many channels. It is an interesting and surprising result emerging from this study that the impact of noise and distortion correlation on multi-channel dynamic range is only fully manifest when the channel count is large (> 4).

In this work, I determined analytically and experimentally the degree of correlation between signals, noise, and harmonics in a parallel ADC array. Fig. 1.1 shows a parallel ADC system composed of M ADCs (not to be confused with

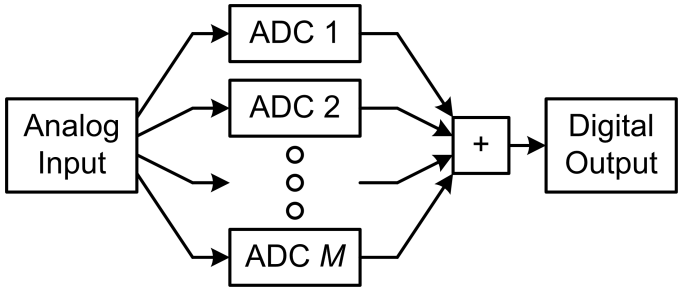

Figure 1.1: Combining multiple ADCs in parallel increases the SNR by a factor M, if all noise is uncorrelated across ADC channels.

a time-interleaved ADC array [10]). In this system, the same analog signal is applied to all M ADCs and the output is digitally summed. The dynamic range, as measured by the maximum signal-to-noise ratio (SNR), increases because the signal is correlated from channel to channel while the noise is not. When summed, the voltage of the M correlated (or coherent) signals increase over a single channel by a factor M (power increases by M^2), while the uncorrelated (or independent) noise from each channel combines as root-sum-square (RSS), which increases the voltage by $\sqrt{M}$ (power increases by M). The maximum power into the ADC array increases by M while the noise averages lower. In a parallel array, the SNR, therefore, increases by a factor of M assuming the noise is uncorrelated from channel-to-channel [11, 12, 13, 14].

In Chapter 2, I will develop a mathematical framework to discuss the correlation between channels. Additionally, I will discuss the limited literature in this area of multi-channel ADC arrays. I will discuss the decorrelation techniques previously discussed in the literature.

To investigate the correlation of noise and distortion experimentally, I devel-

oped a 16-channel testbed using 16-bit state-of-the-art ADCs and 16 direct-digital synthesizers (DDS) as low-noise signal sources. I will describe the test bed and its characterization in Chapter 3. The goal of the test bed is the capability to measure low levels of correlation. To achieve this, the test bed is composed of a large number of channels, provides excellent isolation from channel to channel, excellent source correlation, and has minimal source and digital noise.

While the signal power increases by M^2 when the channels are reasonably well matched, many communication and sensor applications of parallel ADC arrays, such as interference mitigation, require the extremely high matching between channels [15, 16]. Though hardware variations between channels limit the intrinsic channel response match, digital equalization techniques improve channel-to-channel matching. Channel nonlinearities, however, limit the level of matching achievable, as measured by the channel-pair cancellation ratio (CPCR). I investigated the challenge of measuring the very high levels of signal correlation in the presence of channel non-linearities with different measurement signals. For a completely linear channel, the channel matching is limited by noise. With nonlinearities, the ability to measure the signal correlation depends on the measurement signal, with linear frequency modulated signals performing better than band-limited Gaussian noise on an experimental receiver. I will discuss this further in Chapter 4.

In Chapters 5 and 6, I will address five sources of noise and distortion within ADCs— thermal noise (and other random physical processes), sampling noise, quantization noise, sampler distortion, and quantizer distortion. Thermal noise

is assumed to be always independent between ADCs and is the largest source of noise in modern ADCs. In Chapter 5, I will verify this experimentally. Ideally, quantization noise is correlated between channels, but previous investigations in the literature determined that it may be decorrelated using dithering [17].

Continuing in Chapter 5, I will demonstrate the sampling noise due to a common clock is fully correlated from channel-to-channel. Efforts to reduce the correlation using two previously developed decorrelation techniques—phase randomization [18, 19] and frequency offsets [20, 21]—successfully reduced the correlated noise in half.

In addition to noise, real ADCs generate spurious harmonics that may limit the dynamic range and degrade system performance. The undesired harmonics may alias into the passband of the signal. The extent of spurious harmonic generation by an ADC is characterized by the spur-free dynamic range (SFDR), which is the ratio of the signal to the largest harmonic, while the SNR is the ratio of the signal to the integrated noise power. Generally, you would like a SFDR greater than your SNR within a given bandwidth. Fig. 1.2 shows the spectrum from of a single DDS input to single ADC. The largest ADC harmonic is about -90 dBFS, so by our definition the SFDR is 90 dB (the higher spurious tones are not ADC harmonics, and I assume they are generated by the DDS). These harmonics may be correlated across ADCs (I show later that they largely are), in which case their power increases by M^2 like the signal, resulting in no net increase in SFDR from parallelization, as illustrated in Fig. 1.3. Various methods have been proposed to improve the SFDR of a single channel ADC [22, 23, 24].

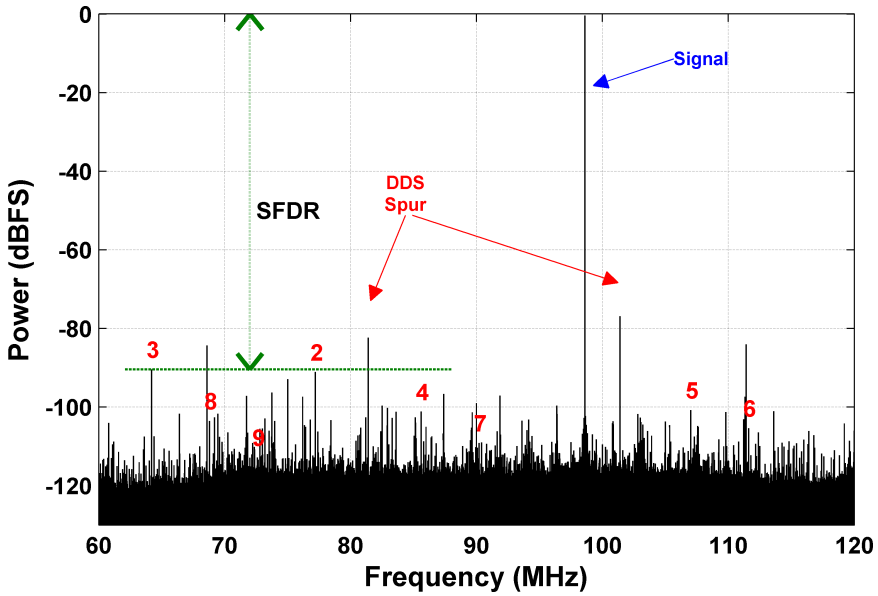

Figure 1.2: Measured spectrum of single tone with many harmonic spurs and SFDR of 90 dB. The first nine ADC harmonics are numbered. Many of the non-numbered spurs are generated by the DDS, including the largest spurs. While these spurious harmonics are larger than the ADC harmonics, they occur at different frequencies from the ADC harmonics, so they can be ignored.

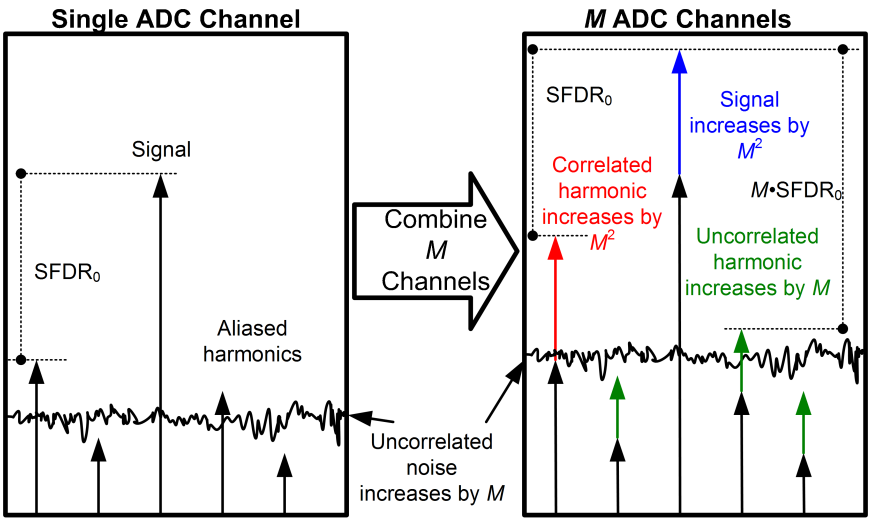

Figure 1.3: For an M channel ADC array, correlated signals and harmonics increase in power by M^2, while uncorrelated harmonics and noise increase by M. As a result, for completely correlated harmonics, the total SFDR does not increase, while for uncorrelated harmonics an increase in SFDR of M would be achieved.

In Chapter 6, I will demonstrate analytically and experimentally that harmonics from quantizers are largely uncorrelated (with some partial correlation); however, harmonics from the sampler are largely correlated. This large correlation necessitates the need for decorrelation techniques. I will demonstrate the impact of the previously developed decorrelation techniques to reduce harmonic correlation and discuss two new decorrelation techniques—phase cancellation and clock offsets—that offer significant advantages over the other two. Phase cancellation increases the system SFDR by adjusting the input phase in such a way as to cancel the largest harmonics. Clock offset decorrelation applies unique sampling frequencies to each channel causing aliased harmonics to alias to different frequencies, which increases the SFDR by about M^2. Together the four techniques provide a complete "toolbox" to improve the SFDR by up to M^2. Each technique offers different levels of dynamic range and complexity increases, allowing a system design a range of techniques to target the optimal level of decorrelation. Finally in Chapter 7, I summarize the results and make suggestions for future work.

To conclude, a succinct statement of the problems addressed in this thesis is:

1. What are the major noise and distortion sources in large (> 4 channel) parallel ADC arrays?
2. To what extent are these noise and distortion sources correlated from channel to channel?

3. To what extend can existing (and proposed) decorrelation techniques minimize output noise and distortion?

The unique contributions of this thesis to the field of multi-channel ADC array technology are:

1. I have built the largest channel-count multi-channel ADC array useful for studying noise averaging effects in such systems.
2. I have found that sampling noise and sampler distortion are the major correlated noise and distortion sources.
3. I have found that thermal noise and quantization noise (with dithering) are the major uncorrelated noise sources.
4. I have found that distortion from quantizer nonlinearities are partially correlated.
5. I have investigated the following techniques for decorrelation:
    a Phase randomization
    b Frequency offsets
6. Of these techniques, I have found frequency offsets to be most effective (as discussed in the body of this thesis).
7. I have developed the following two decorrelation techniques:
    a Phase cancellation
    b Clock offsets
8. I have shown that the advantages of phase cancellation relative to phase randomization are:

a Reduced peak harmonics levels, increasing SFDR by up to 8 dB

b Reduced impact of a “bad draw” in phase randomization

9. I have shown the advantages of clock offsets relative to frequency offsets are that clock offsets do not require mixers and are therefore appropriate in direct-sampling systems.
10. Of all the techniques, frequency offsets and clock offsets are most effective, improving the SFDR by M^2
11. Phase randomization, phase cancellation, and frequency offsets reduced the sampling noise by 50% - the maximum theoretical limit, while clock offsets use independent clocks and produce independent sampling noise.

These findings are substantiated in theory and in experiment as described below.

Chapter 2

Background

In this chapter, I will discuss the relevant background research from the literature. In the first section, I mathematically describe the correlation between channels and associated correlation metrics. Next, I will describe the analytical models for sampling noise, sampler distortion, and quantizer nonlinearities from the literature. I will then discuss *prewhitening*, which is the intellectual foundation of the decorrelation techniques used in this dissertation. Finally, I discuss the previous literature on harmonic correlation and decorrelation techniques.

2.1 Combining Multiple Channels

In this section, I outline the mathematical foundation of correlation, describe correlation across many channels, and discuss various metrics to characterize correlation across many channels. It is important to note that, while the mathematics are the same, the discussion here focuses on the correlation between two sequences or signals, not between random variables.

Fig. 1.1 showed a parallel ADC array, where the output sequences x_m of M channels are digitally summed,

$$\sum_{m=1}^{M} x_m.$$

The power of the combined signal P_x is the *expectation* of the magnitude squared

of sum of the sequences x_m,

$$P_x = \mathrm{E}\left[\left|\sum_{m=1}^{M} x_m\right|^2\right], \tag{2.1}$$

where $\mathrm{E}[x]$ denotes the expectation of x. The expectation is defined as

$$\mathrm{E}[x] \triangleq \frac{1}{t_1 - t_0}\int_{t_0}^{t_1} x(t)dx$$

for continuous signals and

$$\mathrm{E}[x] \triangleq \frac{1}{N}\sum_{n=1}^{N} x[n]$$

for discrete signals, if the signals are wide-sense stationary. Expanding the magnitude squared operation of (2.1), P_x becomes

$$P_x = \mathrm{E}\left[\left(\sum_{m=1}^{M} x_m\right)\left(\sum_{l=1}^{M} x_l\right)^*\right] \tag{2.2}$$

where * denotes complex conjugation. Summation and expectation are linear operations, so (2.2) may be rewritten as

$$P_x = \sum_{m=1}^{M}\sum_{l=1}^{M} \mathrm{E}\left[x_m x_l^*\right]. \tag{2.3}$$

$\mathrm{E}\left[x_m x_l^*\right]$ is the *correlation*, or first *joint moment*, between the sequences x_m and x_l [25]. The elements of (2.3) form the $M \times M$ *correlation matrix* $\mathbf{C_x}$,

$$\mathbf{C_x} = \begin{bmatrix} \mathrm{E}[x_1x_1^*] & \mathrm{E}[x_1x_2^*] & \cdots & \mathrm{E}[x_1x_M^*] \\ \mathrm{E}[x_2x_1^*] & \mathrm{E}[x_2x_2^*] & \cdots & \mathrm{E}[x_2x_M^*] \\ \cdots & \cdots & \cdots & \cdots \\ \mathrm{E}[x_Mx_1^*] & \mathrm{E}[x_Mx_2^*] & \cdots & \mathrm{E}[x_Mx_M^*] \end{bmatrix} \tag{2.4}$$

where m is the row number and l is the column number. The mth diagonal entry of the correlation matrix is the power, or *second moment*, of the mth channel. The

correlation matrix is Hermitian because $\mathbf{C_x}$ is the conjugate transpose of itself, $\mathrm{E}[x_m x_l^*] = \mathrm{E}[x_m^* x_l]$.

The total power P_x of the sum of channels x_m is the sum of all the entries of $\mathbf{C_x}$, which in matrix notation is

$$P_x = \mathbf{1}^T \mathbf{C_x} \mathbf{1}, \tag{2.5}$$

where $\mathbf{1}$ is a M-dimensional vector with a value of 1 for every entry,

$$\mathbf{1} = \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}_M . \tag{2.6}$$

P_x is always real (as it should be, since you can't have imaginary power!) because $\mathbf{C_x}$ is Hermitian, therefore,

$$P_x = \mathbf{1}^T \mathbf{C_x} \mathbf{1} = \mathbf{1}^T \Re(\mathbf{C_x}) \mathbf{1}. \tag{2.7}$$

The *correlation coefficient*, defined as

$$\rho_{ml} \triangleq \frac{\mathrm{E}[x_m x_l^*]}{\sqrt{\mathrm{E}[|x_m|^2]\,\mathrm{E}[|x_l|^2]}}, \tag{2.8}$$

characterizes the degree of correlation between two channels, irrespective of the sequence power. Correlation has units of power, while the correlation coefficient is unit less.

The correlation coefficient may be measured for harmonics, signals, or noise in the frequency domain or the time domain. If $\rho_{ml} = 1$, then x_m is fully correlated

with x_l. If $\rho_{ml} = 0$, then x_m is uncorrelated with x_l. If $\rho_{ml} = -1$, then the sequences are anti-correlated and $x_m = -x_l$. The correlation coefficient ρ_{ml} varies from -1 to 1.

The correlation coefficient matrix $\mathbf{R_x}$ is composed of pairwise correlation coefficients, in the same way as the correlation matrix $\mathbf{C_x}$,

$$\mathbf{R_x} = \begin{bmatrix} 1 & \rho_{1,2} & \cdots & \rho_{1,M} \\ \rho_{2,1} & 1 & \cdots & \rho_{2,M} \\ \cdots & \cdots & \cdots & \cdots \\ \rho_{M,1} & \rho_{M,2} & \cdots & 1 \end{bmatrix}. \tag{2.9}$$

The *total correlation coefficient* R_x is the sum of the entires of the correlation coefficient matrix $\mathbf{R_x}$,

$$R_x = \mathbf{1}^T \mathbf{R_x} \mathbf{1}. \tag{2.10}$$

The maximum value of R_x is M^2 when all channels are correlated ($\rho_{ml} = 1$). The correlation coefficient matrix, like the correlation matrix, is Hermitian ($\rho_{ml} = \rho_{lm}^*$). Therefore, like the P_x, when calculating the total correlation coefficient R_x only the real parts of $\mathbf{R_x}$ are required, since the complex parts cancel.

2.1.1 Signal Correlation

Throughout this dissertation, the focus is on the correlation difference between the signal s and the error ε. The error ε may be thermal noise, sampling noise, spurious harmonics, or some other error source. The recorded sequence x_m

is separated into a signal s_m and a signal-dependent additive error $\varepsilon_m(s_m)$,

$$x_m = s_m + \varepsilon_m(s_m). \tag{2.11}$$

(The additive error may also be signal independent, such as thermal noise, but the formulation is the same.) The signals are typically about the same, that is $s_m \approx s_l \approx s_0$. The correlation matrix $\mathbf{C_s}$ is then approximately

$$\mathbf{C_s} \approx \begin{bmatrix} \mathrm{E}[s_0 s_0^*] & \mathrm{E}[s_0 s_0^*] & \cdots & \mathrm{E}[s_0 s_0^*] \\ \mathrm{E}[s_0 s_0^*] & \mathrm{E}[s_0 s_0^*] & \cdots & \mathrm{E}[s_0 s_0^*] \\ \cdots & \cdots & \cdots & \cdots \\ \mathrm{E}[s_0 s_0^*] & \mathrm{E}[s_0 s_0^*] & \cdots & \mathrm{E}[s_0 s_0^*] \end{bmatrix}, \tag{2.12}$$

and $P_s \approx M^2 \mathrm{E}[|s_0|^2]$. The total correlation coefficient R_s is about M^2.

While the above approximation is generally true, it does not provide sufficient information of exactly how well matched two channels are. Very high levels of matching are required for many interference mitigation techniques used in communications [15]. Consider two signals s_1 and s_2, where s_2 the amplitude is different by a factor of 1.01 and the phase offset from s_1 by 170 μrad [1], $s_2 = 1.01 s_1 e^{j0.000\,17}$. The correlation coefficient is, therefore,

$$\rho_{1,2} = \frac{\mathrm{E}[s_1 s_2^*]}{\sqrt{\mathrm{E}[|s_1|^2]\,\mathrm{E}[|s_2|^2]}} = 0.999\,999\,99 - 0.000\,17\,j. \tag{2.13}$$

Clearly, the signals are very well correlated, although they are not identical as such a high correlation coefficient would suggest. Retaining eight significant digits is not only unwieldy, but it violates standard scientific notation.

[1] This is the measured RMS phase error and amplitude error of the IF testbed discussed later.

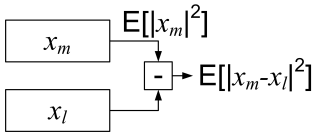

Figure 2.1: Simple block diagram of CPCR measurement.

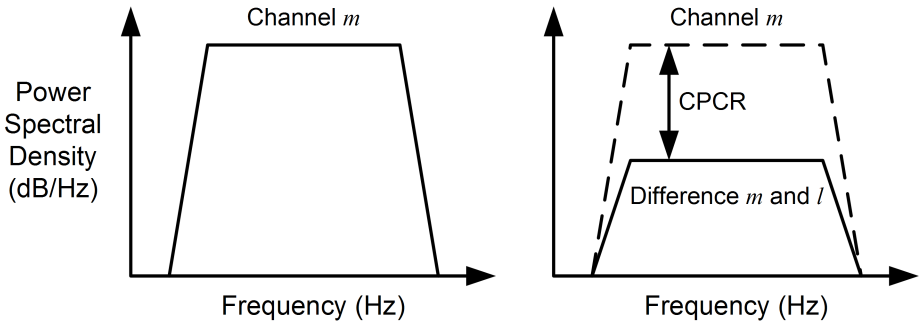

Figure 2.2: The CPCR is the reduction in power between a single channel and the difference between two signals.

CPCR provides a much better metric of matching between any two channels. CPCR quantifies the matching of two signals x_m and x_l by comparing the signal power of one channel to power of the difference between the two signals,

$$\text{CPCR} = \frac{\text{E}[|x_m|^2]}{\text{E}[|x_m - x_l|^2]} = \frac{\text{E}[|x_m|^2]}{\text{E}[|x_m|^2] + \text{E}[|x_l|^2] - 2\rho_{ml}\sqrt{\text{E}[|x_m|^2]\,\text{E}[|x_l|^2]}}, \quad (2.14)$$

as shown in Fig. 2.1. Fig. 2.2 shows a qualitative description of CPCR. The signal x_m has a particular power spectral density (PSD) and after cancellation it is reduced by the CPCR.

The CPCR from the example (2.13) is

$$\text{CPCR} = \frac{\text{E}[|s_1|^2]}{\text{E}[|s_1 - s_2|^2]} = \frac{\text{E}[|s_1|^2]}{\text{E}[|s_1 - 1.01 s_1 e^{j0.000\,17}|^2]} = \frac{1}{1.0 \times 10^{-4}} = 40.0 \text{ dB}, \quad (2.15)$$

which demonstrates that the CPCR is far more readable than the correlation coef-

ficient when the signals are well matched.

2.1.2 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is defined as

$$\mathrm{SNR} \triangleq \frac{P_s}{P_\varepsilon} = \frac{M^2\,\mathrm{E}[|s_0|^2]}{\mathbf{1}^T\mathbf{C}_\varepsilon\mathbf{1}} \tag{2.16}$$

where ε is the noise. If I assume that the noise power is about the same in every channel,

$$\mathrm{E}[\varepsilon_m\varepsilon_m^*] \approx \mathrm{E}[\varepsilon_l\varepsilon_l^*] \approx \mathrm{E}[|\varepsilon_0|^2],$$

then $\mathbf{C}_\varepsilon \approx \mathbf{R}_\varepsilon\,\mathrm{E}[|\varepsilon_0|^2]$. In that case, (2.16) becomes

$$\mathrm{SNR} = \frac{M^2\,\mathrm{E}[|s_0|^2]}{R_\varepsilon\,\mathrm{E}[|\varepsilon_0|^2]}. \tag{2.17}$$

The SNR improvement relative to a single channel from combining M channels is then

$$\mathrm{SNR}_{\mathrm{improvement}} = \mathrm{SNR}/\frac{\mathrm{E}[|s_0|^2]}{\mathrm{E}[|\varepsilon_0|^2]} = \frac{M^2}{R_\varepsilon}. \tag{2.18}$$

Since R_ε varies from 0 to M^2, the SNR improvement varies from a factor ∞ to 1, although an improvement of ∞ is unlikely.

In addition, I define the average non-diagonal correlation coefficient $\bar{\rho}$,

$$\bar{\rho} \triangleq \frac{1}{M^2-M}\sum_{m=1}^{M}\sum_{l\neq m=1}^{M}\rho_{ml} = \frac{R_\varepsilon - M}{M^2-M}. \tag{2.19}$$

It is often possible to calculate $\bar{\rho}$ between any two pairs of channels, such as sampling noise. In these cases, (2.17) is written as

$$\mathrm{SNR} = \frac{M^2}{(M+(M^2-M)\bar{\rho})}\frac{\mathrm{E}[|s_0|^2]}{\mathrm{E}[|\varepsilon_0|^2]}. \tag{2.20}$$

and the SNR improvement from (2.18) is then

$$\mathrm{SNR}_{\mathrm{improvement}} = \frac{P_s}{P_\varepsilon} \Big/ \frac{\mathrm{E}[|s_0|^2]}{\mathrm{E}[|\varepsilon_0|^2]} = \frac{M^2}{(M + (M^2 - M)\bar{\rho})}. \tag{2.21}$$

When $\bar{\rho} = 0$ (as in the case of thermal noise), then the SNR improvement is M.

I will now introduce the ratio of the actual SNDR increase to the ideal SNDR increase I. The actual SNDR increase is

$$\frac{\mathrm{SNDR}_{\mathrm{sum}}}{\mathrm{SNDR}_{\mathrm{single\ channel}}} = \frac{M^2 S}{P_R} \Big/ \frac{S}{P_r} = \frac{M^2 P_r}{P_R}, \tag{2.22}$$

while the ideal SNDR increase is M. Therefore, I is

$$D = \frac{M^2 P_r}{P_R} / M = \frac{M P_r}{P_R}. \tag{2.23}$$

Some challenges exist in measuring the correlation of the noise. In some instances, it is beneficial to measure the correlation in frequency domain, such as when the input signal is a tone. The signal may be transformed into the frequency domain using the discrete Fourier transform (DFT) [26]. The DFT transforms the sequence $x_m[n]$ to the discrete frequency domain $X[\tilde{n}]$,

$$X[\tilde{n}] \triangleq \sum_{n=0}^{N-1} x[n] W_N^{n\tilde{n}} \tag{2.24}$$

where $W_N = e^{2\pi j/N}$. The inverse DFT (IDFT) is defined as

$$x[n] \triangleq \frac{1}{N} \sum_{\tilde{n}=0}^{N-1} X[\tilde{n}] W_N^{-n\tilde{n}}. \tag{2.25}$$

The correlation between x_m and x_l in the discrete frequency domain is

$$\mathrm{E}\left[x_m[n] x_l^*[n]\right] = \frac{1}{N} \sum_{n=0}^{N-1} \left(\frac{1}{N} \sum_{\tilde{n}_m=0}^{N-1} X_m[\tilde{n}_m] W_N^{-n\tilde{n}_m} \right) \left(\frac{1}{N} \sum_{\tilde{n}_l=0}^{N-1} X_l[\tilde{n}_l] W_N^{-n\tilde{n}_l} \right)^*,$$

which may be rewritten as

$$\mathrm{E}\left[x_m[n]x_l^*[n]\right] = \frac{1}{N^2}\sum_{\tilde{n}_m=0}^{N-1}\sum_{\tilde{n}_l=0}^{N-1} X_m[\tilde{n}_m]X_l^*[\tilde{n}_l]\left(\frac{1}{N}\sum_{n=0}^{N-1} W_N^{n(\tilde{n}_l-\tilde{n}_m)}\right). \tag{2.26}$$

As discussed earlier, I generally only require the real part of the correlation. Taking the real part of the correlation, (2.26) becomes

$$\Re\left(\mathrm{E}\left[x_m[n]x_l^*[n]\right]\right) = \frac{1}{N^2}\sum_{\tilde{n}_1=0}^{N-1}\sum_{\tilde{n}_2=0}^{N-1} \Re\left(X_m[\tilde{n}_1]X_l^*[\tilde{n}_2]\right)\left(\frac{1}{N}\sum_{n=0}^{N-1}\cos(2\pi n(\tilde{n}_2-\tilde{n}_1)/N)\right). \tag{2.27}$$

The summation of cosines equals

$$\frac{1}{N}\sum_{n=0}^{N-1}\cos(2\pi n(\tilde{n}_2-\tilde{n}_1)/N) = \begin{cases} 1 & \text{if } \tilde{n}_1 = \tilde{n}_2 \\ & \\ 0 & \text{if } \tilde{n}_1 \neq \tilde{n}_2 \end{cases},$$

so (2.27) becomes

$$\Re\left(\mathrm{E}\left[x_m[n]x_l^*[n]\right]\right) = \frac{1}{N^2}\sum_{\tilde{n}=0}^{N-1}\Re\left(X_m[\tilde{n}]X_l^*[\tilde{n}]\right). \tag{2.28}$$

The real part of the correlation may be found with a single summation.

Alternately, the real part of the correlation may be found by adding the two signals and measuring the power. The real part of the correlation is

$$\Re\left(\mathrm{E}\left[x_m x_l^*\right]\right) = (1/2)\,\mathrm{E}\left[x_m x_l^*\right] + (1/2)\,\mathrm{E}\left[x_m x_l^*\right]^*. \tag{2.29}$$

Using (2.3) for two channels,

$$\mathrm{E}\left[x_m + x_l\right] = \mathrm{E}[|x_m|^2] + \mathrm{E}[|x_l|^2] + \mathrm{E}[x_m x_l^*] + \mathrm{E}[x_m x_l^*]^*, \tag{2.30}$$

the real part of the correlation becomes

$$\Re\left(\mathrm{E}\left[x_m x_l^*\right]\right) = \frac{1}{2}\left(\mathrm{E}\left[x_m + x_l\right] - \mathrm{E}[|x_m|^2] - \mathrm{E}[|x_l|^2]\right). \tag{2.31}$$

By measuring the power of each channel individually and then the sum, I can measure the correlation. This is especially powerful when the voltage signal is not directly available, such as when using a spectrum analyzer. I implemented this technique when I measured the correlation of the sampling noise.

2.1.3 Spur-Free Dynamic Range

Throughout this dissertation, I only consider harmonics of sinusoidal input tones, although harmonics are generated for all input signals. The kth harmonic of an input tone at frequency f is also a tone, which is at frequency $k \cdot f_{\text{in}}$. The tone may then be analyzed using the DFT. If I consider only the positive frequencies of the Fourier spectrum, since the harmonic is real, then the harmonic is fully described by the Fourier coefficient a_{km} of the bin containing the harmonic frequency $k \cdot f_{\text{in}}$, where m is the channel number.

In the time domain (again, only considering the positive frequencies), the harmonics $\varepsilon_{km}(t)$ are

$$\varepsilon_{km}(t) = a_{km} e^{j2\pi kft}. \tag{2.32}$$

When the signal input frequencies are the same, then the correlation is

$$\mathrm{E}[\varepsilon_{km}\varepsilon_{kl}^*] = \mathrm{E}\left[a_{km} e^{j2\pi kft} a_{kl}^* e^{-j2\pi kft}\right] = a_{km} a_{kl}^*. \tag{2.33}$$

If the harmonics may be manipulated in such a way, that $k \cdot f$ of channel m is different from channel l, then the correlation is zero.

Applying (2.33) to (2.8), the correlation coefficient between the kth har-

monic of any two channels m and l is

$$\begin{aligned}\rho_{ml} &= \frac{a_{km}a_{kl}^*}{|a_{km}||a_{kl}|} = \frac{|a_{km}|e^{j\angle a_{km}}|a_{kl}|e^{-j\angle a_{kl}}}{|a_{km}||a_{kl}|} \\ &= e^{j\angle a_{km} - j\angle a_{kl}}. \end{aligned} \tag{2.34}$$

While the magnitude of ρ_{ml} is always 1, I are only concerned with the real part of

$$\Re(\rho_{ml}) = \cos(\angle a_{km} - \angle a_{kl}),$$

which equals zero when the difference between the angles of the harmonics is $\pi/2$. The harmonics are fully correlated when the difference between the angles is 0, and they harmonics are anti-correlated when the angle are π out of phase.

The total kth harmonic output power P_k of M combined channels is

$$\begin{aligned} P_k &= \left| \sum_{m=1}^{M} a_{km} \right|^2 \\ &= \sum_{m=1}^{M} \sum_{l=1}^{M} a_{km}a_{kl}^* \\ &= \sum_{m=1}^{M} \sum_{l=1}^{M} |a_{km}||a_{kl}|\rho_{ml}. \end{aligned} \tag{2.35}$$

The total harmonic power depends on both the magnitude and phase of each harmonic. If the phases are all equal ($\rho_{ml} = 1$), their amplitudes add coherently, and the maximum total harmonic power $P_{k,\max}$ is achieved,

$$P_{k,\max} = \left(\sum_{m=1}^{M} |a_{km}| \right)^2. \tag{2.36}$$

Ideally, a single metric is desired to describe the correlation of harmonics between a set of M channels; however, since $|a_{km}|$ may vary significantly between channels, I instead use a trio of metrics to describe the performance. The first

metric is the *decorrelation value* I_k,

$$I_k \triangleq \frac{P_k}{P_{k,\max}}. \tag{2.37}$$

I_k measures the ratio of the actual harmonic power over the fully correlated harmonic power for a given harmonic k. For example, $I_k = 1/4$ indicates that the actual harmonic power is four times lower than the fully correlated case. When the average value of the real part of $\rho_{ml} = 0$ when $m \neq l$, then the harmonics are "fully decorrelated" and $I_k \approx M^{-1}$. The harmonics powers from each channel add instead of their voltages.

The second metric is the *total correlation coefficient* defined in (2.10). R_k is closely related to P_k; P_k is R_k weighted by the amplitude of the harmonics. I_k provides a better understanding of the actual performance of a parallel array; however, it is sensitive to harmonic power and a single large amplitude harmonic may significantly impact its value. R_k, on the other hand, is independent of harmonic amplitude and, therefore, provides a better measure of the harmonic correlation. Both metrics are useful for evaluating the correlation and performance of parallel ADC arrays.

The third metric is the SFDR, which maintains the same definition whether for an individual ADC or ADC array: the ratio of the maximum signal over the maximum harmonic,

$$\text{SFDR} \triangleq \frac{M^2 P_{\text{FS}}}{\max(P_k)}. \tag{2.38}$$

where P_{FS} is the full-scale power of the ADC, which is 0 dBFS. SFDR provides a single metric to underscore the correlation and the effectiveness of decorrelation

techniques, and enables a direct comparison to single ADC performance.

2.2 Prewhitening and Decorrelation Techniques

Prewhitening is a common technique within the communications community. Prewhitening involves applying linear filtering to a signal, such that, after filtering, the power spectral density appears white (flat spectrum) [27]. The autocorrelation of the signal is made more like a delta function.

Prewhitening allows for more efficient use of the available spectrum in a communications system. The noise added within the communications channel has a white spectrum. By reducing peaks and increasing the troughs in the spectrum, the signal-to-noise ratio is maximized across all frequencies for the available signal power. When the signal is received, the opposite linear filter is applied to recover the original signal.

The decorrelation techniques presented here are a variation on prewhitening, where instead of attempting whiten the signal, the decorrelation technique attempts to whiten the errors introduced by the hardware. Then, when the channels are combined the errors add as though they are independent.

The challenge of combining many ADCs in parallel is relatively new and, as such, the literature record is very sparse. Table 2.1 shows the significant literature for each ADC error source and decorrelation technique. Several papers and application notes discussed combining 2 to 4 ADC in parallel [11, 12, 13, 14]. An array of that size is unlikely to be limited by the correlated noise sources.

Table 2.1: Prior work on decorrelation techniques for different error sources.

Decorrelation Technique	Quantization Noise	Sampling Noise	Harmonics
Dithering	[20, 17]	No effect	-
Phase Randomization	-	This Work	[18, 19]
Frequency Offsets	-	This Work	[20, 21]
Phase Cancellation	-	This Work	This Work
Clock Offsets	-	-	This Work

Rabideau, Howard and their colleagues at MIT Lincoln Laboratory published a series of conference papers beginning in 2001 on the decorrelation technique for very large arrays of both ADCs and other analog components [20, 21, 18, 19]. Their papers described the linear transform technique and outlined five methods to decorrelate the errors. In addition, a paper by Skartlien and Oyehaug discussed the decorrelation of quantization noise in large arrays using additive dithering [17]. In this section, I describe prior research on correlation of errors in parallel ADC arrays. The literature record is sparse.

2.2.1 Phase Randomization

In a previous report, Howard *et al.* proposed and demonstrated a method to decorrelate mixer spurs and harmonics in parallel receiver arrays [18]. Further measurements of this technique were performed by Rabideau using four receivers

[19]. The technique involved applying a phase shift to the input signal of each channel by adjusting the local oscillator (LO) phase driving each mixer in the parallel array. The phase shift is then removed digitally at the output, resulting in a decrease in the harmonic correlation.

The phase randomization technique seeks to reduce the correlation between harmonics by randomizing the harmonic phases, which should reduce the total correlation coefficient R_k. Fig. 2.3 schematically shows how the phase randomization technique is implemented. In this approach, the signal phase of each channel is offset by a random phase using a flexible LO $L_m(t)$ and mixer. An ADC then digitizes the signal, which generates sampler and quantizer harmonics. A digital multiplier then removes the previously introduced phase shift and recorrelates the signal across channels. Since the harmonic phase is a multiple of the input signal phase, even after signal recorrelation, the harmonic phases are still randomly distributed across channels. If the harmonics of each channel are of equal magnitude (they are not) and randomly distributed in phase around the unit circle with a uniform distribution, then their sum approaches the Rayleigh distribution and the average total correlation coefficient R_k is M.

Consider a phase and amplitude modulated signal

$$w(t) = A(t)\cos\left(\omega_{\mathrm{RF}}t - p(t)\right) \tag{2.39}$$

where $A(t)$ is the amplitude modulation, $p(t)$ is the phase modulation, and ω_{RF} is the carrier frequency. The signal is mixed with an LO

$$L_m(t) = 2\cos\left(\omega_{\mathrm{LO}}t + \theta_m(t)\right) \tag{2.40}$$

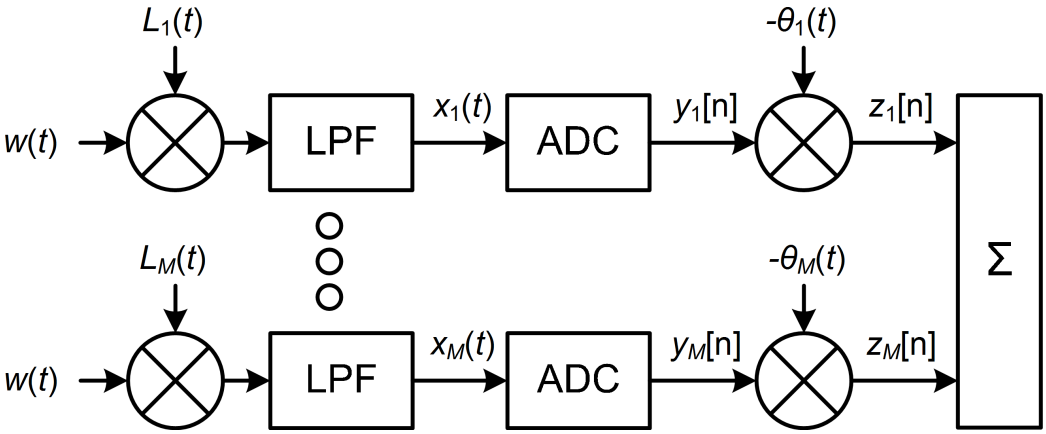

Figure 2.3: Schematic diagram of phase randomization and frequency offset decorrelation techniques.

where $\theta_m(t)$ is the introduced phase offset. The resulting output from each channel m is

$$x_m(t) = A(t)\cos\left(\omega t + p(t) + \theta_m(t)\right) \tag{2.41}$$

where $\omega_{\mathrm{LO}} - \omega_{\mathrm{RF}} = \omega$. Next, the ADC digitizes the mixed signal x_m and introduces harmonic distortion ε_m. The digitized signal with distortion $\varepsilon_m(nT)$ is

$$y_m[n] = x_m(nT) + \varepsilon_m(nT). \tag{2.42}$$

where n is the sample index and T is sampling period. Finally, the Hilbert transform $\mathcal{H}(x)$ is applied to the digitized signal to extract only the positive frequencies [28] and the phase offset is removed, by multiplying by a complex exponential, $e^{-j\theta_m(nT)}$

$$\begin{aligned} z_m[n] &= \mathcal{H}(y_m[n])e^{-j\theta_m(nT)} \\ &= A(nT)e^{j(\omega nT + p(nT))} + \mathcal{H}(\varepsilon_m(nT))e^{-j\theta_m(nT)}. \end{aligned} \tag{2.43}$$

When analyzing harmonics, I consider a sinusoidal input with $A(t) = A$ and

$p(t) = 0$. In that case, the positive frequencies of the harmonic distortion $\varepsilon_m(nT)$ are

$$\mathcal{H}(\varepsilon_m(nT))e^{-j\theta_m(nT)} = a_{km}e^{jk\omega nT - j\theta_m(nT)}, \tag{2.44}$$

which using (6.1) becomes

$$\begin{aligned} a_{km}e^{jk\omega nT - j\theta_m(nT)} &= |a_{km}|e^{j\angle a_{km}}e^{jk\omega nT - j\theta_m(nT)} \\ &= |a_{km}|e^{j(k\omega nT + (k-1)\theta_m(nT) + \phi_{km})}. \end{aligned} \tag{2.45}$$

For the phase randomization technique, I set $\theta_m(t) = \theta_m$ and (2.45) simplifies to

$$|a_{km}|e^{j(k\omega nT + (k-1)\theta_m + \phi_{km})}. \tag{2.46}$$

The phase of the kth harmonic is, therefore, $(k-1)\theta_m + \phi_{km}$.

The goal of the phase randomization approach is to randomize the input signal phase θ_m and cause the harmonic phase to be randomly distributed around the unit circle with a uniform distribution. To begin, I define the *harmonic voltage gain*

$$\nu \triangleq \sqrt{\sum_{m=1}^{M}\sum_{l=1}^{M}\rho_{ml}}. \tag{2.47}$$

If the harmonics are successfully distributed around the unit circle, then ν may be described by the Rayleigh distribution, assuming the harmonic amplitudes is equal across all channels. The exact probability distribution function of the voltage sum ν of M tones uniformly distributed on the unit circle is

$$f_\nu(\nu) = \nu\int_0^\infty \gamma J_0(\nu\gamma)[J_0(\gamma)]^M d\gamma \tag{2.48}$$

where J_0 is the zeroth order Bessel function [29, 18]. For large M, and assuming that approximately $M/2$ phases are on each half of the unit circle [30, 31], the distribution approaches the Rayleigh distribution

$$f_\nu(\nu) \approx \frac{2\nu}{M} e^{-\nu^2/M}. \tag{2.49}$$

The expected value of I_k becomes

$$I_k \approx \mathrm{E}[f_\nu(\nu)\nu^2 d\nu]/M^2 = 1/M, \tag{2.50}$$

which, in our 16-channel system is

$$10\log_{10}(16^{-1}) = -12.0\mathrm{dB}.$$

2.2.2 Frequency Offsets

In addition to using phase offsets to decorrelate spurs, Howard *et al.* suggested an implementation using frequency offsets [20, 21]. Howard's method causes the harmonics to be offset in frequency from channel to channel, so that when the channels are combined the harmonics do not add, resulting a SFDR improvement of M^2. I discuss Howard's method as a way to introduce our extension of this technique. In our extension, I apply frequency offsets to each sampling clock, which causes aliased harmonics to occur at different frequencies. This extension removes the need for a mixer, making it more appropriate for a wider range of systems.

2.2.2.1 Frequency Offsets on ADC Harmonics

By applying different frequency offsets to the input signal of each channel using independent local oscillators, I can cause the harmonics to appear at different frequencies for each channel. A frequency offset is simply a time-varying phase offset, and, as a result, the phase offset analysis from Section 2.2.1 may be applied using the appropriate $\theta_m(t) = \omega_m t + \theta_m$ for each channel. The phase error term θ_m accounts for the unknown starting phase of the signals at a particular time (for instance, $t = 0$). From (2.45), I find that the harmonic, after realignment, is

$$a_{km} e^{jk\omega nT - j\theta_m(nT)} = |a_{km}| e^{j(k\omega nT + (k-1)(\omega_m nT + \theta_m) + \phi_{km})}. \tag{2.51}$$

After realignment of the signal frequency, each harmonic is offset in frequency from the original harmonics by $(k-1)\omega_m$. The harmonics are not at the same frequency and, therefore, do not add. I_k is approximately M^2, which is M times larger than expected from phase randomization.

The harmonics are no longer at the same frequency and do not combine. Depending on the Nyquist zone of the harmonic and signal, (2.51) may need to be adjusted slightly, so that the final frequency offset is $(k \pm 1)\omega_m$. If both harmonic and signal are in either even or odd Nyquist zones, then the frequency offset is $(k-1)\omega_m$; otherwise, the offset is $(k+1)\omega_m$.

2.2.3 Dithering on Quantization Noise

Dithering is the addition of an independent signal to the input of the ADC to randomize the ADC input. The dither signal randomizes the input to reduce spurs

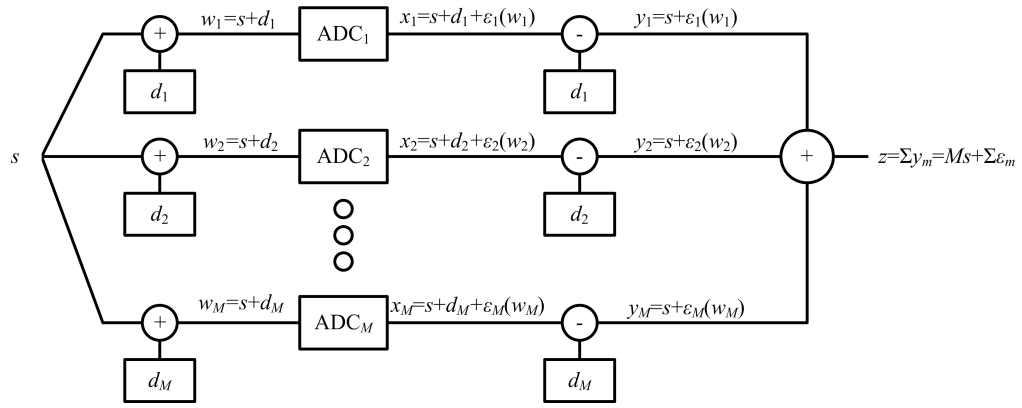

Figure 2.4: Subtractive dither in a parallel ADC array.

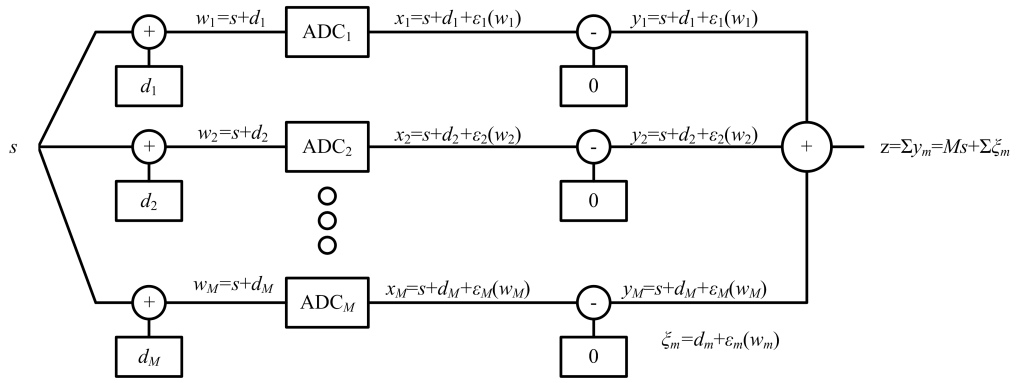

Figure 2.5: Additive dither in a parallel ADC array.

and whiten the quantization noise. The dither signal is typically random noise or a tone. Common noise probability density functions (PDF) for the random noise are Gaussian or normal, uniform, triangular, digital, and sinusoidal [32].

Dithering is either subtractive, where the dither signal is subtracted from output, or additive, where the dither signal is not subtracted. Figures 2.4 and 2.5 show subtractive and additive dither systems in a parallel ADC system.

The correlated input signal $s(t)$ is added to a unique independent dither signal $d_m(t)$ for each channel m. The linear transform is $g_m(x) = x + d_m$. The

transformed input signal $w_m(t) = s(t) + d_m(t)$ is quantized and sampled and the ADC output signal is

$$x_m[n] = s(nT) + d_m(nT) + \varepsilon_m(w_m(nT)). \tag{2.52}$$

The inverse transform is $g_m^{-1}(x) = x - d_m$ for subtractive dither and $g_m^{-1}(x) = x$ for additive dither. The output for subtractive dither is

$$y_m[n] = s(nT) + \varepsilon_m(w_m(nT)) \tag{2.53}$$

and

$$y[n] = s(nT) + d_m(nT) + \varepsilon_m(w_m(nT)) \tag{2.54}$$

for additive dither.

Quantization noise is a mapped error sequence; for every input voltage there is a single error voltage. If the ADCs are identical and if the input signals are correlated, then the quantization noise is fully correlated between channels. Dithering reduces the correlation between the input signals and, therefore, reduces the correlation of quantization noise between channels. The correlation of quantization noise and the input signal is well-known [33].

In Bennett's seminal paper on quantization noise [39], he observed that quantization noise is approximately uniform and white if four conditions hold. Bennett's conditions (quoted from [40]) are:

- The quantizer does not overload
- The quantizer has a large number of levels
- The bin width or distance between levels is small

- The PDF of the pairs of input samples is given by a smooth PDF

Many common signals, including some sinusoids, do not meet Bennett's conditions. The quantization noise of signals that meet Bennett's conditions appears to be white, uniformly distributed with a variance $\Delta^2/12$, and independent of the input signal. Δ is the voltage of one least significant bit (LSB).

Bennett's results are only approximately true. Widrow's *Statistical Theory of Quantization* provides an exact condition for independence of quantization noise from the signal [41]. For an input signal s with a particular PDF $f_s(s)$ and characteristic function

$$\Phi_s(u) = \int_{-\infty}^{\infty} f_s(s) e^{jus} ds, \tag{2.55}$$

the quantization noise and signal are independent if the signal is *band limited*, such that

$$\Phi_s(u) = 0 \quad \text{for} \quad |u| > \frac{\pi}{\Delta}. \tag{2.56}$$

Most signals do not meet the band limited condition; however, I could add an independent dither signal that meets the band limited condition and ensure independence, since the sum of two independent signals is the multiplication of their characteristic functions.

Few dither signal of practical interest exists that meets the above band limited condition [42]. The necessary and sufficient condition for independence and whiteness of a signal with added dither d is

$$\Phi_d\left(\frac{i}{\Delta}\right) = 0 \quad \text{for all} \quad i = \pm 1, \pm 2, \ldots, \tag{2.57}$$

Table 2.2: PDF of common dither distributions. M is number of digital bits and $K = 1,2,...,M$.

Distribution	Probability Density Function
Uniform	$f_d(d) = 1/D \quad \text{for} \quad \{-\frac{D}{2} \leq d \leq \frac{D}{2}\}$
Triangular	$f_d(d) = \frac{d}{D^2} + \frac{1}{D} \quad \{-D \leq d \leq 0\}$ $f_d(d) = -\frac{d}{D^2} + \frac{1}{D} \quad \{0 \leq d \leq D\}$
Gaussian	$f_d(d) = \frac{1}{\sqrt{2\pi}\sigma_d} e^{-d^2/2\sigma}$
Sine	$f_d(d) = \frac{1}{\pi\frac{D}{2}\sqrt{1-\left(\frac{2d}{D}\right)^2}} \left\{-\frac{D}{2} \leq d \leq \frac{D}{2}\right\}$
Digital	$f_d(d) = \frac{1}{M} \sum_{k \in K} \left(d - \frac{k}{M}D\right)$

which is a more relaxed condition than (2.56) [42, 43]. A uniformly distributed random variable with a width of $i \cdot \Delta$ meets the condition of 2.57. In addition, any arbitrary dither signal added to another dither signal that meets the condition for whiteness, such as triangular dither signal, also meets the conditions. Gaussian noise does not meet the condition for independence. Table 2.3 lists the characteristic function of five common dither distributions and when they meet the conditions of (2.57).

As Table 2.3 shows, most common dither signals do not make the quantization noise independent from the signal. In [42], the authors suggest using the

Table 2.3: Characteristic functions of common dither distributions. Only Uniform and Triangular distributions are the only distributions that can meet the conditions of (2.57). J_0 is a Bessel function. M is number of digital bits. $K = 1, 2, ..., M$.

Distribution	Characteristic Function	Meet (2.57)
Uniform	$\Phi_d(u) = \text{sinc}(uD)$	$D = \Delta$
Triangular	$\Phi(u) = \text{sinc}^2(uD)$	$D = 2\Delta$
Gaussian	$\Phi_d(u) = e^{-2\pi^2 u^2 \sigma_d^2}$	Never
Sine	$\Phi_d(u) = J_0(\pi u D)$	Never
Digital	$\Phi_d(u) = \frac{1}{M} \sum_{k \in K} e^{-j2\pi u(k/M)D}$	Never

deviation factor, or "D" factor,

$$D_F = \int [E(\varepsilon|s)]^2 f_s(s) ds, \tag{2.58}$$

to calculate the dependence of the quantization noise on the input signal [44]. The "D" factor is the expected value of the quantization noise conditional on the input signal. If the deviation factor is zero, then the quantization noise power remains approximately $\Delta^2/12$ but the quantization noise is completely independent of the signal. D_F is zero only if $E(e|s) = 0$ or $f_s(s) = 0$, but the latter is a trivial case. Given the characteristic function of the dither signal, the expectation in (2.58) is

$$E(\varepsilon|s) = -\sum_{i\neq 1}^{\infty} \Phi_d\left(\frac{i}{\Delta}\right) e^{j\pi(i/\Delta)s} \frac{\Delta}{i} \cos(\pi i) \quad \text{for} \quad i = \pm 1, \pm 2, \ldots \quad [42]. \tag{2.59}$$

It is clear that if $\Phi_d(k/\Delta) = 0$ — which are the necessary and sufficient conditions for independence — then D_F is zero. D_F may be evaluated for other dither functions and the appropriate signal s. If Bennett's conditions hold then a reasonable approximation of s is a uniform distribution from $\pm\Delta/2$.

D_F is signal-dependent noise power, so in a parallel ADC system, D_F is the correlated quantization noise [32]. Without dither, D_F is equal to $\Delta^2/12$ and goes to zero if conditions of (2.57) are met.

Independent Gaussian dither has been discussed as a method to decorrelate quantization noise in simulation [20] and analytically [17]. Both results show that additive Gaussian noise reduces the correlation of quantization noise. Skartlien and Oyehaug analytically determined total correlated and uncorrelated noise in an additive dithered array [17]. They found the optimal dither power to minimize to

total noise power (including dither) is

$$\sigma_{d,opt}^2 = \frac{\Delta^2}{(2\pi)^2} \ln(2(M-1)). \tag{2.60}$$

These results were not confirmed experimentally.

2.3 Summary of Chapter

In summary, I have discussed the mathematical background of correlation and developed a set of metrics to evaluate parallel ADC array performance. I then discussed the previously developed decorrelation techniques, phase randomization and frequency offsets. Finally, I discussed the previous results from the literature that demonstrated quantization noise is decorrelated from the signal using dithering.

Chapter 3

Development of Experimental Test Bed

3.1 Test Bed Description

The 16-channel test bed is composed of 16 ADCs, 16 DDSs as signal sources, amplifiers, anti-aliasing filters (AAF), clocks, and trigger sources, as shown in Fig. 3.1. Fig. 3.2 shows a photograph of the test bed, which required two 19 inch half height racks. The DDSs generate tones (as well as other modulated signals), which are amplified to full-scale of the ADC and filtered to remove out-of-band noise and harmonics. The ADC then samples the resulting signal at 120 MHz using by one of eight low-noise crystal oscillators. I designed the test bed to operate at a nominal intermediate frequency of 90 MHz, which is in the center of the second Nyquist zone. This is a common frequency location in radio applications.

The ADCs chosen were 16-bit Linear Technology LTC2208 capable of sampling at 130 MSPS. An RF transformer performs the single-to-differential conversion; I used the example input circuit from the datasheet [45]. Digital buffers can store up to 4 million samples before transferring them to a personal computer over 100 Mbit Ethernet. The large buffer length allows for long integration time to reduce the noise floor and expose many harmonics, while using a low data rate interface. The LTC2208 includes two gain settings (I use both depending on the experiment), a digital randomizer (which I generally used), and an internal sub-

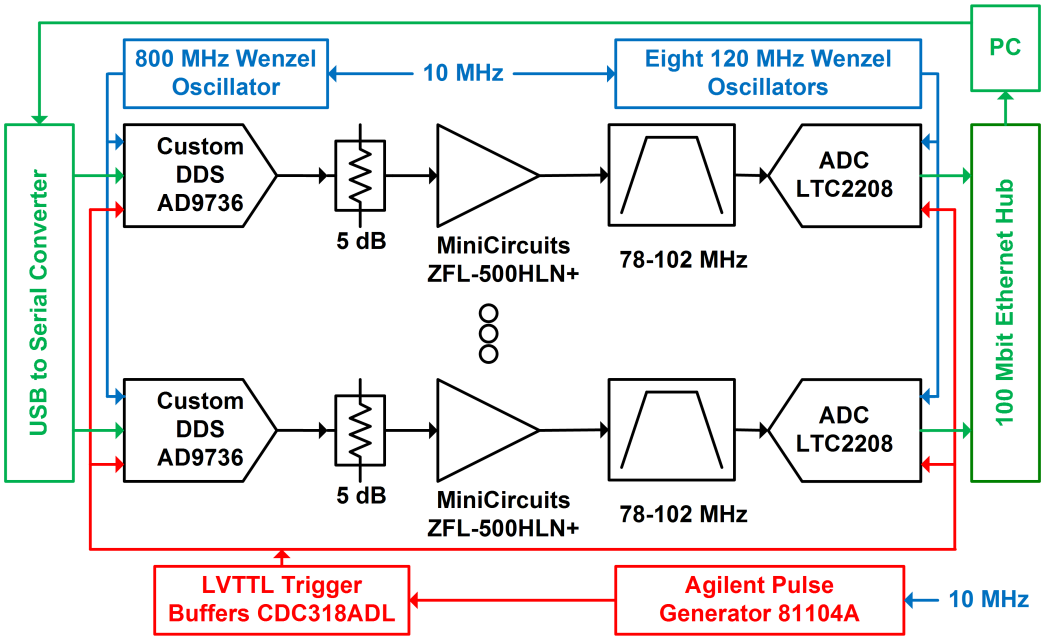

Figure 3.1: Block diagram of experimental test bed consisting of 16 ADCs, 16 DDS, eight 120 MHz oscillators, an 800 MHz oscillator, amplifiers, and assorted buffers and distribution networks.

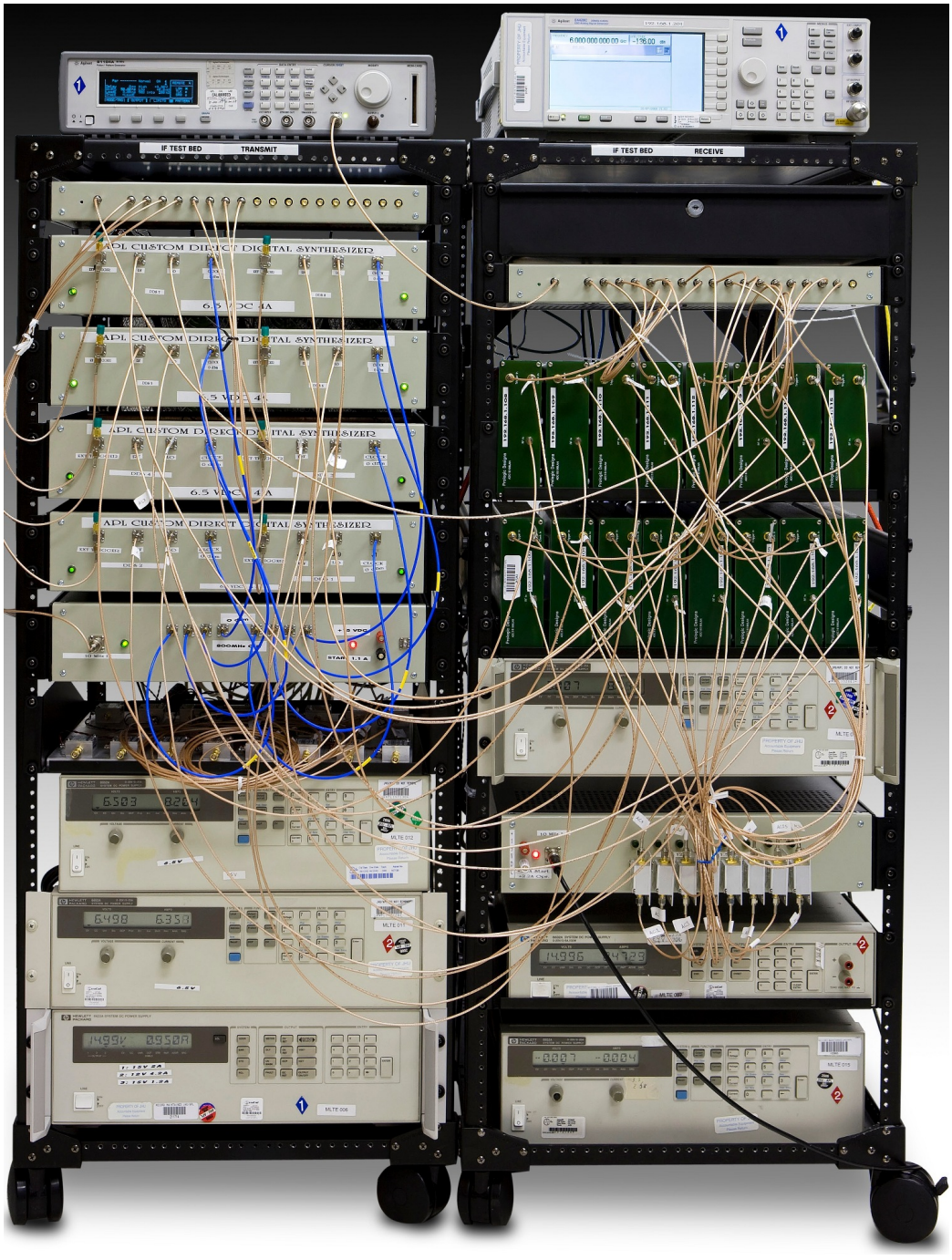

Figure 3.2: Photograph of the test bed composed of 16 ADCs, 16 DDSs, and supporting hardware. Test bed designed and assembled by myself.

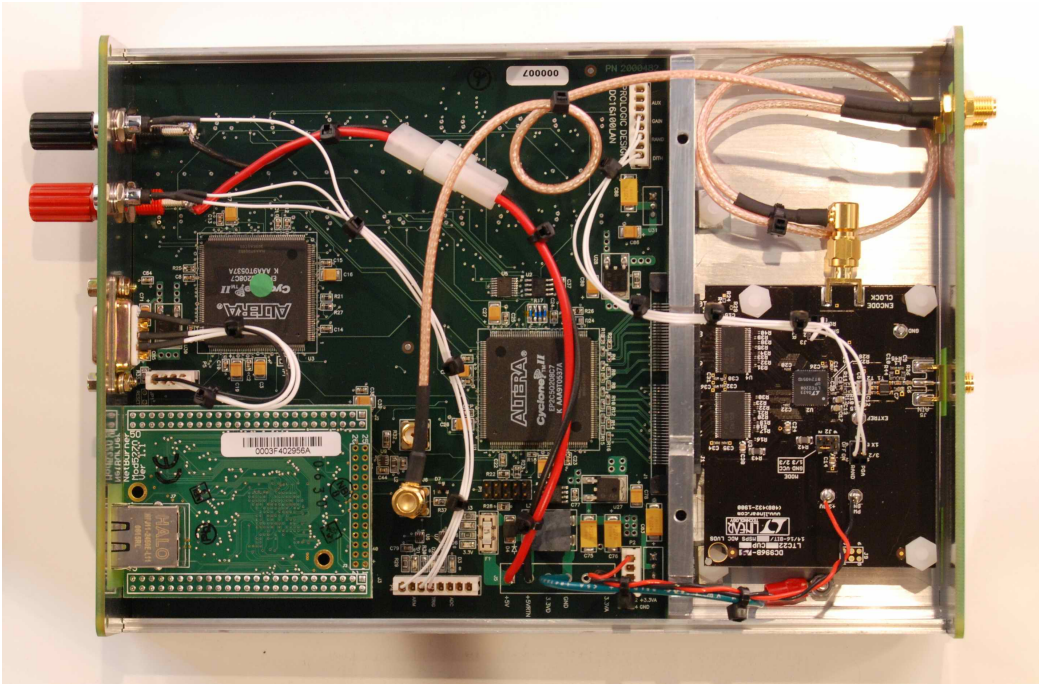

Figure 3.3: Photograph of the ADC board. ADC board designed by Prologic Designs with guidance and troubleshoot by myself.

tractive dither circuit (which I generally did not use). The buffer circuit accepted either an external LVTTL trigger or an internal trigger.

The DDSs are composed of a Xilinx Virtex 4 field-programmable gate array (FPGA) that controls two Analog Devices AD9736 digital-to-analog converters (DAC) (each FPGA controls two channels). The DACs are 14-bit and capable

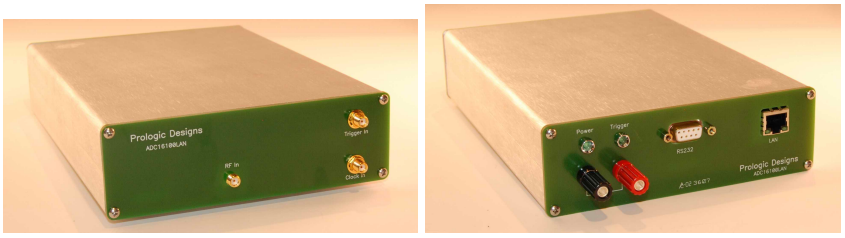

Figure 3.4: Photograph of the front and back of the ADC board.

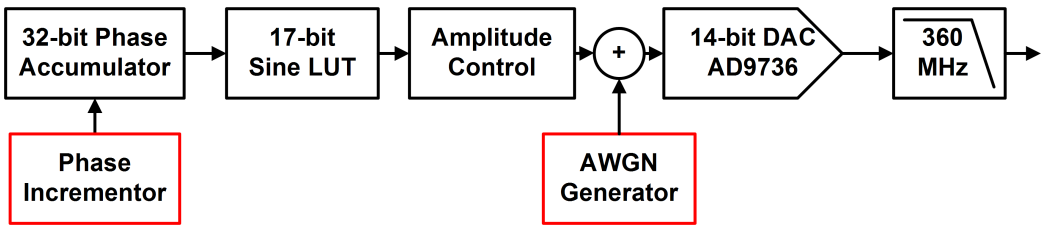

Figure 3.5: Simplified block diagram of custom DDS highlighting key enhancements for this work: phase "incrementor" and additive white Gaussian noise generator.

of operating at 1.2 GHz; however, our FPGA code was only able to run at 400 MHz with a double-data rate output resulting in a DDS clock frequency of 800 MHz. I implemented a standard DDS architecture [46]: the phase accumulator length is 32 bits and the phase-to-amplitude conversion look-up table is 17 bits, as shown in Fig. 3.5. The DDSs are capable of generating tones, pulsed tones, and pulsed linear frequency modulated waveforms. A seventh-order 360-MHz output reconstruction filter followed the DAC output. The maximum output power of each DDS is -3 dBm. I used a RS-232 serial connection to interface with the DDSs, which was chosen due to its low cost.

I implemented two key features in DDSs for this work. First, I developed a simplified additive white Gaussian noise generator using a Ziggurat method similar to [47, 48]. This allowed us to raise the noise floor of the DDSs as high as -100 dBc/Hz to act as a dither source. Second, I added a phase "incrementor" to phase align the channels, as described in Section 3.2.3.

The Mini-Circuits ZFL-500HLN+ amplifiers increase the -3 dBm signal to greater than the ADC full-scale power of +12 dBm. The amplifiers are a significant source of harmonic distortion (-45 dBFS maximum); however, the anti-

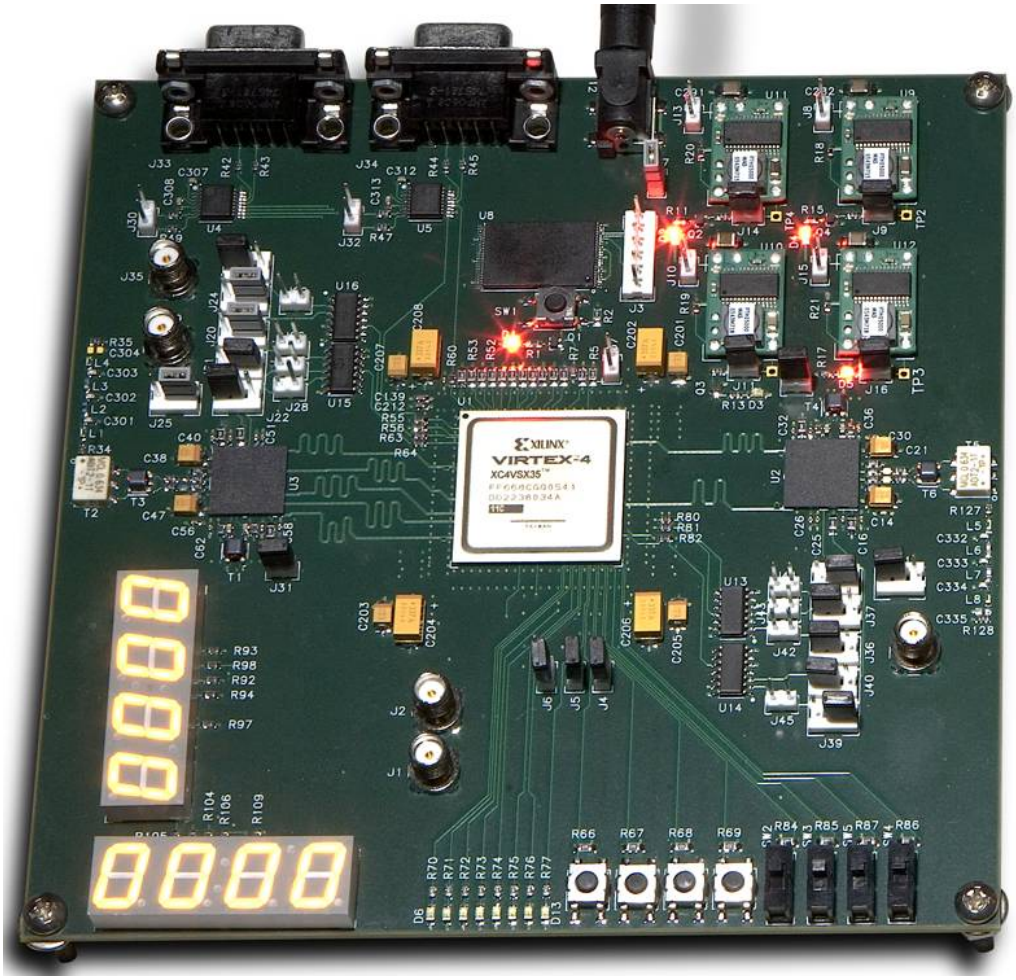

Figure 3.6: Dual DDS board using Xilinx Virtex 4 FPGA and Analog Devices AD9736.

DDS board designed by Matt Gerwell

aliasing provide greater than -75 dB of attenuation to the second and higher harmonics, resulting in harmonics powers of -120 dBFS at most. The anti-aliasing filters have a nominal bandwidth of 24 MHz centered at 90 MHz. The 800 MHz clock is generated by multiplying 100 MHz ultra-low noise oscillator from Wenzel Associates by eight. The 800 MHz is phase locked to a master 10 MHz oscillator. The final 800 MHz signal is divided eight ways and connected to each DDS board. Each of the eight 120 MHz oscillators from Wenzel Associates clocked two ADCs resulting in independent sampling noise in each pair of channels. Each independent oscillator was phase locked to the master 10 MHz signal. Finally, the LVTTL trigger was generated by an Agilent 81104A pulse generator. The trigger was divided 24 ways and buffered with two Texas Instruments CDC318ADL clock drivers resulting in a trigger rise time of approximately 3 ns.

The test bed includes a low noise 120 MHz clock array and an 800 MHz clock. Fig. 3.7 shows the configuration of the 120 MHz clock array. A 10 MHz reference is multiplied to 120 MHz using $\times 4$ and $\times 3$ multipliers. Eight individual oscillators are then phase locked to the common 120 MHz reference. Figs. 3.8 and 3.9 show the top and front of the clock array. George Vetticad assembled the clocks.

Fig. 3.10 shows the 800 MHz clock configuration. A 10 MHz reference clock is multiplied by 10 to 100 MHz and phase locked to a low noise 100 MHz oscillator. The output of the 100 MHz oscillator is then multiplied by 8 in two steps, split 8 ways and filtered. One clock signal is fed to each DDS board, which has two output channels.

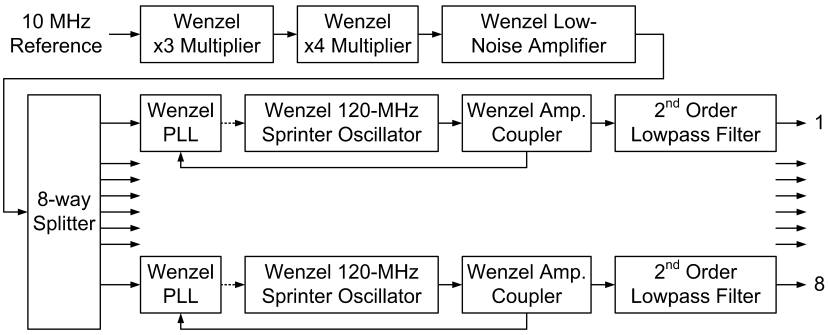

Figure 3.7: Block diagram of 120 MHz clock array.

Figure 3.8: Front panel of 120 MHz clock array.

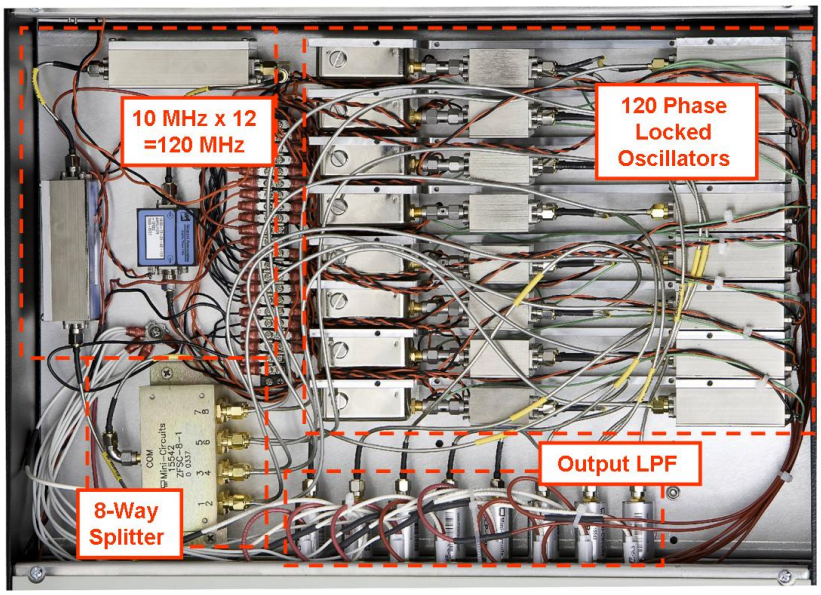

Figure 3.9: Top down view of 120 MHz clock array. Clock assembly designed by myself and assembled by George Vetticad.

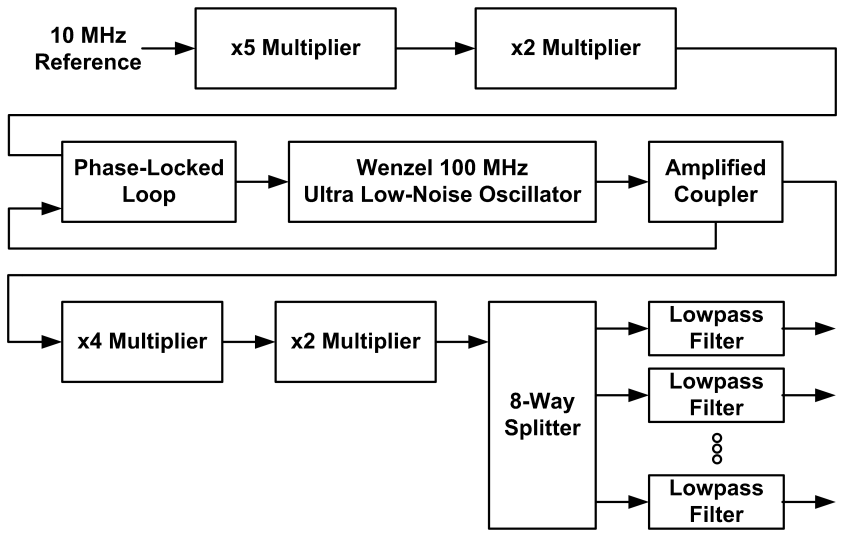

Figure 3.10: Block diagram of the 800 MHz clock. Clock assembly designed by myself and assembled by George Vetticad.

3.2 Design Goals

The goal of the 16-channel ADC test bed is to determine the performance capability of large parallel arrays that may be limited by noise and distortion correlation. To achieve this goal, I identified four design goals of the test bed: (1) the test bed must be able to measure low levels of partial correlation and provide significant statistical variation; (2) the measurement system—the signal sources and digital buffers—must be clean with low noise and spurs; (3) the signal sources must be well correlated from channel to channel; (4) the ADC channels must have excellent isolation between them. The section outlines the reason for each, steps I took to implement these goals, and any challenges I encountered.

3.2.1 Large Number of Channels

When the number of channels is small the impact of correlation is small compared to a large number of channels. This impacts both the total parallel array performance and our ability to measure the correlation.

Consider the error sequence r_m generated in each channel $m = 1, \ldots, M$, with M being the total number of channels. In our parallel array, I directly sum the error sequence digitally to form the total output error sequence R

$$R = \sum_{m=1}^{M} r_m.$$

I find the total output error power P_R by taking the expectation of R^2

$$P_R = \mathrm{E}[R^2] = \mathrm{E}\left[\left(\sum_{m=1}^{M} r_m\right)\left(\sum_{n=1}^{M} r_n\right)\right],$$

which, since expectation and summation are both linear operations, can be expanded as

$$P_R = \sum_{m=1}^{M}\sum_{n=1}^{M} \mathrm{E}[r_m r_n]. \tag{3.1}$$

The total power is the sum of M^2 pair-wise correlations $\mathrm{E}[r_m r_n]$.

The correlation coefficient is defined as

$$\rho_{mn} = \frac{\mathrm{E}[r_m r_n]}{\sqrt{\mathrm{E}[r_m^2]\,\mathrm{E}[r_n^2]}}.$$

The correlation coefficient is one when the sequences are fully correlated, zero with no correlation, and minus one when the sequences are anti-correlated. If I assume that the single channel power, which I will denote as $P_r = \mathrm{E}[r_m^2]$, is the same for all channels then the total power (3.1) becomes

$$P_R = \sum_{m=1}^{M}\sum_{n=1}^{M} \rho_{mn} P_r. \tag{3.2}$$

I further simplify (3.2) by recognizing that $\rho = 1$ when $m = n$, and by defining the average correlation coefficient $\bar{\rho}$ as

$$\bar{\rho} = \frac{1}{M^2 - M} \sum_{m=1}^{M} \sum_{n=1}^{M} \rho_{mn},$$

in which case, (3.2) becomes

$$P_R = P_r \left(M + (M^2 - M)\bar{\rho} \right) \tag{3.3}$$

Table 3.1 shows the error power increase due to correlation $P_R/(MP_r)$

$$\frac{P_R}{MP_r} = (1 + (M-1)\bar{\rho}) \tag{3.4}$$

for several values of $\bar{\rho}$ and M. The larger the number of channels, the greater the impact of partial correlation on limiting the performance of the parallel array. For example, a large average correlation coefficient of 0.5 increases the total error power by 1.76 dB for a two-channel ADC array, while it increase the total error power of a 16-channel ADC array by 9.29 dB. This impacts both performance of the ADC array and our ability to measure partial correlation; therefore, I designed the test bed with a large number of channels.

In addition to improving our ability to measure low levels of partial correlation, the 16 channels provides a large sample set to draw statistical behavior on harmonics and noise. This is particularly important for quantizer nonlinearities, which can vary significantly from ADC to ADC. Having a large number of channels prevents statistical outliers from impacting the overall performance measurements

Table 3.1: Error power increase due to correlation $P_R/(MP_r)$ for several values of $\bar{\rho}$ and M. The larger the number of channels the greater the impact of partial correlation and the greater our ability to measure the partial correlation. Our test bed enables us to observe average correlation coefficients $\bar{\rho}$ approaching 0.01.

M	$\bar{\rho} = 0$	$\bar{\rho} = 0.01$	$\bar{\rho} = 0.10$	$\bar{\rho} = 0.50$	$\bar{\rho} = 1.00$
2	0.00 dB	0.04 dB	0.41 dB	1.76 dB	3.01 dB
4	0.00 dB	0.13 dB	1.14 dB	3.98 dB	6.02 dB
8	0.00 dB	0.29 dB	2.30 dB	6.53 dB	9.03 dB
16	0.00 dB	0.61 dB	3.98 dB	9.29 dB	12.04 dB
32	0.00 dB	1.17 dB	6.13 dB	12.17 dB	15.05 dB
64	0.00 dB	2.12 dB	8.63 dB	15.12 dB	18.06 dB

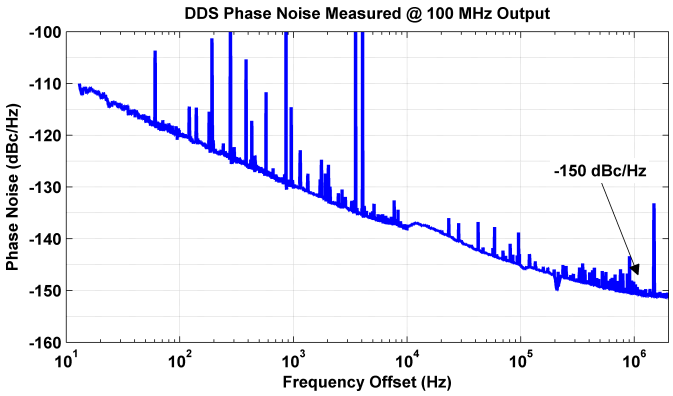

Figure 3.11: Measured phase noise from DDS at 100 MHz output frequency using 800 MHz clock. The DDS phase noise from each channel is comparable to commercial signal generators.

3.2.2 Low Noise and Spur Measurement System

As with most measurements, it is desirable that the measurement system's—signal sources and digital buffers, in this case—noise and spurious signals (spurs) be below that of the device under test (parallel ADCs). In particular, I am concerned about the signal source phase noise [49]. I chose to use DDSs because their phase noise is comparable to commercial signal generators and independent from channel to channel, so the resulting total noise is much lower than most commercial signal generators [50, 51]. Fig. 3.11 shows the measured phase noise of a single channel, measured with a DDS output frequency of 100 MHz. The phase noise was measured using a cross-correlation phase noise measurement system similar to [52].

The DDSs generate harmonics that alias into the anti-aliasing filter passband that are large relative to the ADC harmonics (-75 dBFS or less for the DDSs com-

pared to -85 dBc for the ADCs). The normal AAFs limit the signal bandwidth to 24 MHz centered at 90 MHz. The filters have greater than 60 dB of rejection at 138 MHz, which is the lowest frequency in the third Nyquist zone that aliases into the passband of the filter,

$$(120 - 102) + 120 = 138 \text{ MHz}.$$

Fig. 3.12 shows the first 100 ADC and DDS harmonics for an input frequency of 97.599 792 48 MHz. The ADC harmonics are plotted in the first, second, and third Nyquist zones. While the in-band DDS harmonics from 78 to 102 MHz may be large, only the fiftieth harmonic coincides between the ADC and DDS, demonstrating that I can separate the ADC and DDS harmonics in the frequency domain. The anti-aliasing filter removes the other coincident harmonics. The number of coincident harmonics is a small fraction of the first 100 harmonics, since the ADC and DDS clocks (120 and 800 MHz, respectively) are not closely related.

The second significant source of noise and spurs is the digital buffer that collects the digital data from the analog-to-digital converter. I sought to minimize the noise contribution of the digital circuitry isolating the components as much as possible. I electrically isolated the two analog and digital boards using a 3/8" piece of aluminum. In addition, I isolated the input, clock, and Ethernet connections from the chassis.

To verify that the digital buffer added minimal noise, I measured the noise figure (NF) of the ADC using the Y-factor method [53]. Fig. 3.13 shows the block

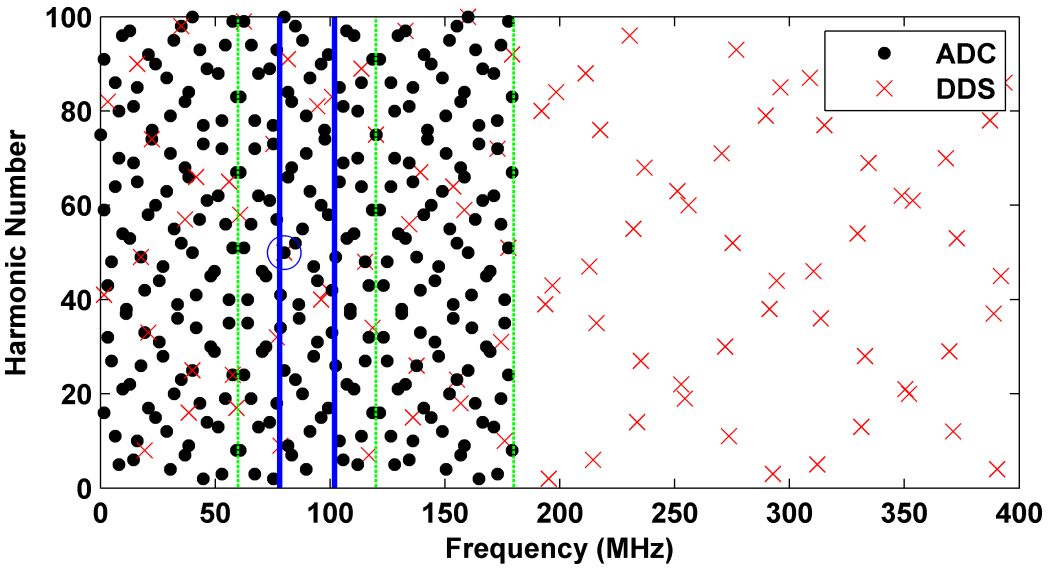

Figure 3.12: Plot of first 100 ADC harmonics in the first, second, and third Nyquist zones and the first 100 DDS harmonics for a frequency of 97.599792 48 MHz. Only the fiftieth harmonic of both the ADC and DDS occur at the same frequency within the passband of the anti-aliasing filter. The blue lines mark the passband of our bandpass anti-aliasing filter, and the green lines mark the boundaries of the first, second, and third Nyquist zones.

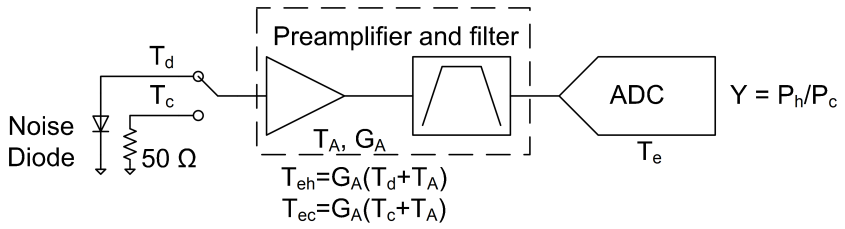

Figure 3.13: Y-factor noise figure measurement technique uses two calibrated noise sources to measure the noise figure of the ADC. The measurement required a preamplifier due to the high noise figure of the ADC.

diagram of the Y-factor method. In the Y-factor method, the ADC noise figure is measured applying two calibrated noise sources with known noise temperatures T_{ec} and T_{eh} to the ADC input and measuring the two output noise powers P_h and P_c. The noise temperature of the ADC T_e is then calculated using

$$T_e = (T_{eh} - Y \cdot T_{ec})/(Y-1) \tag{3.5}$$

where $Y = P_h/P_c$. The noise figure is

$$\mathrm{NF} = 10\log_{10}(1 + T_e/290). \tag{3.6}$$

I used a calibrated noise diode and 50 Ω termination as the noise sources. I measured the preamplifier and filter gain and noise figure using a noise figure capability of an Agilent E4440A. Fig. 3.14 shows the measured noise figure for 16 ADCs, which match the specification of 30.6 dB with gain "off" and 29.6 with gain "on" when the RF transformer loss is included. From this match, I conclude that the digital buffer adds minimal noise to the ADC.

In addition to white noise, the digital buffers could generate spurs. I measured the ADC noise floor spectrum shown in Fig. 3.15 by connecting a 50 Ω

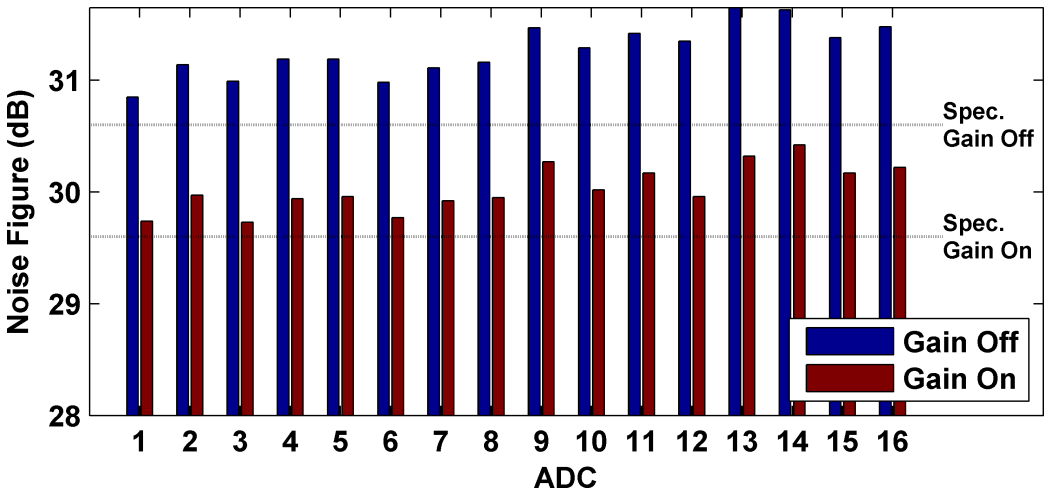

Figure 3.14: Measured noise figure matches the specification when RF transformer loss is included.

termination to an ADC, collecting 100 records with 2^{21} samples in each, and averaging the power of each spectrum. The ADC noise floor is composed of many spurs; however, all are below -105 dBFS, which is well below most of our harmonic measurements.

3.2.3 Excellent Signal Correlation Between Channels

Signal-dependent noise and distortion is potentially correlated; however, to see this correlation the signals must be highly correlated. The DDSs allow us to achieve very high levels of correlation between channels with the addition of the phase "incrementor" shown in Fig. 3.5 and mentioned earlier.

Each DDS receives a common 800 MHz clock and trigger. Unfortunately, the rise time of the trigger was too long (3 ns rise time versus 1.25 ns clock period), such that the trigger did not reliably occur on same clock period for all

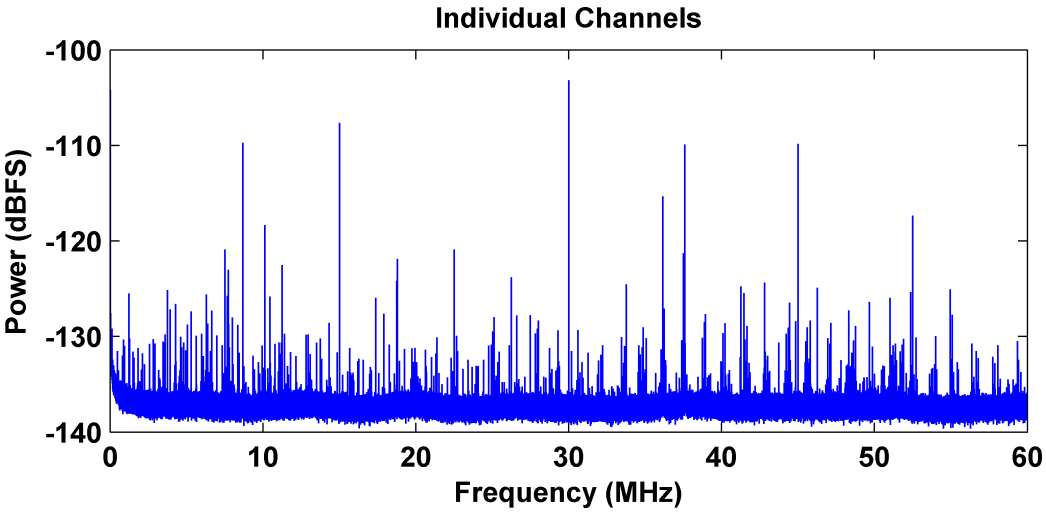

Figure 3.15: ADC noise floor.

DDSs. This was a flaw in our DDS design. To synchronize the channels, I started all the DDSs running with the arbitrary starting phase. Then I would measure the phase using the ADCs and increment the phase accumulator using the phase "incrementor" until the channels were phase aligned. Fig. 3.16 shows excellent phase (standard deviation of 170 μrad) and amplitude matching from the 16 DDSs using this closed-loop calibration technique.

3.2.4 Excellent Isolation Between Channels

I designed the test bed to provide excellent isolation between channels by housing each ADC in a separate enclosure, as shown in Fig. 3.2. Even in separate enclosures, however, I found that there was insufficient isolation between channels for some harmonic measurements.

I observed the insufficient isolation when measuring the amplitude stability of the second harmonic over a set of different captures. For the first set of 10 cap-

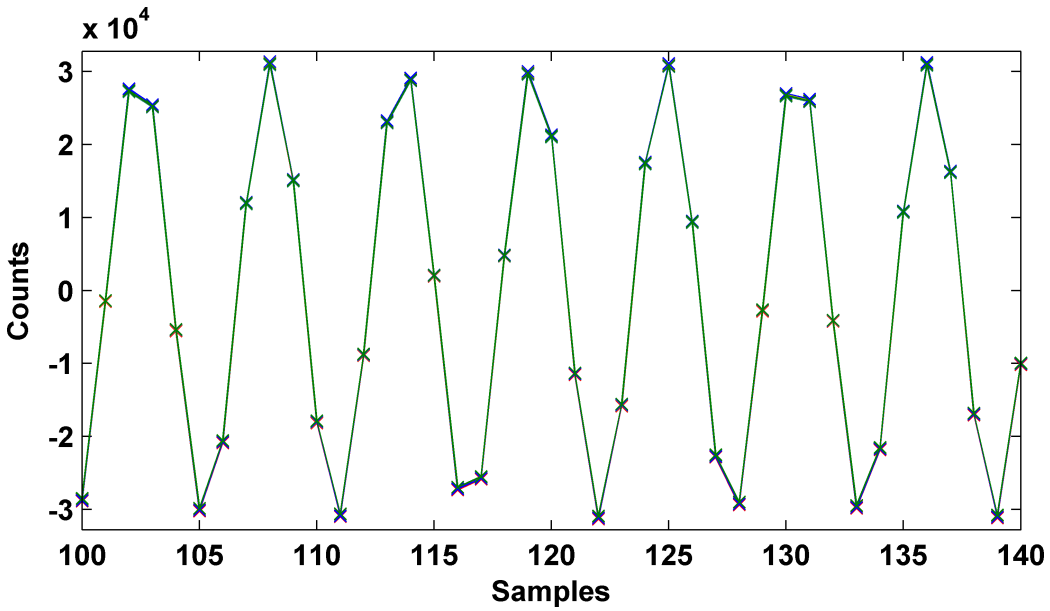

Figure 3.16: Output of 16 ADC channels demonstrating phase incrementation alignment technique.

tures, the input signal phase of each channel was kept constant and the measured second harmonic power was constant as expected. For the second set of 10 captures, the input signals phase were all adjusted by the same amount between each capture and the second harmonic remained constant as expected. On the third set of 10 captures, the input signal phase of each channel was adjusted by a random amount and the amount was *different* for each channel. Fig. 3.17a shows the second harmonic power for this third set of 10 captures for each ADC channel. Each line is one of 10 captures. The variation was as large as 20 dB from capture to capture for any given ADC.

This second harmonic power variation was unexpected. Our hypothesis is that there was insufficient isolation from channel to channel, and that the signal from the adjacent channels was leaking into the clock line. This unwanted clock

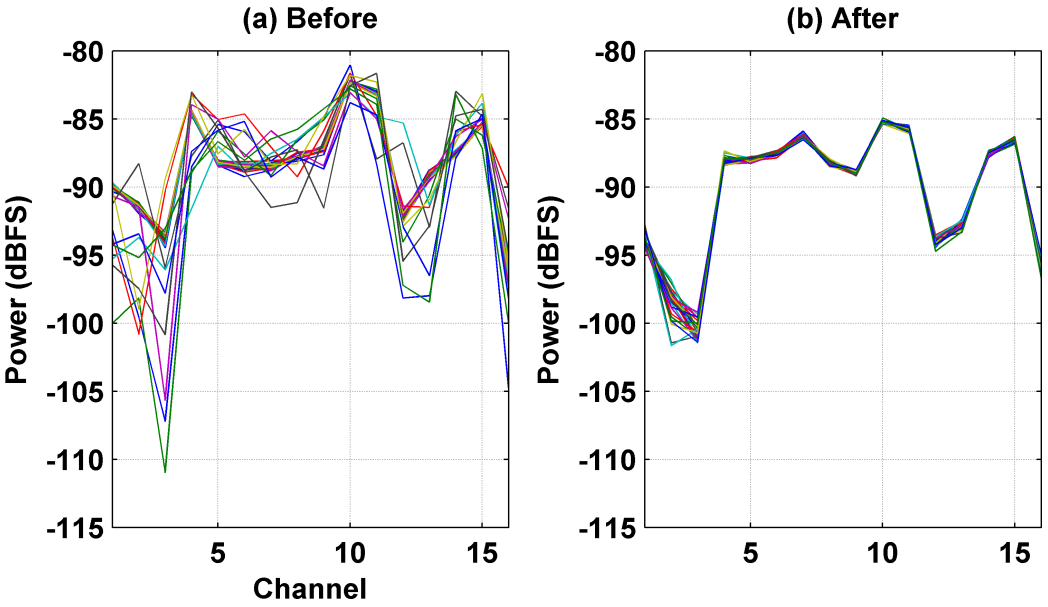

Figure 3.17: (a) When the input signal phases were adjusted randomly across channels the power of the second harmonic varied significantly. (b) After hardware modifications to increase isolation, the variation was dramatically reduced.

signal at the signal frequency also sampled the input signal, resulting in a spur at the same frequency as the second harmonic. The spurious clock signal was the sum of multiple channels, so that when all the phases were changed randomly the spurious clock signal phase also changed randomly. When all the input phases were changed by the same amount then the combined spurious clock phase did not change from channel to channel. The resulting spurious "second harmonic" then either destructively or constructively combined with the ADC generated second harmonic. A reasonable estimate for power of the spurious "second harmonic" was about -92 dBFS for most channels, since the measured second harmonics below this level showed greater variation from more complete destructive interference. Comparing high-power Channel 10 to low-power Channels 3 and 16, the

lower power harmonics vary more.

I made several modifications to the test bed to reduce the crosstalk. To reduce RF leakage on the power lines, I added additional bypass capacitors to the ADCs and amplifiers. I implemented a *star ground* to reduce signal leakage via the ground [54]. I also added additional grounds to the chassis holding the ADCs. Finally, I replaced all the single-shielded signal and clock cables with double-shielded cables to reduce radiated electromagnetic interference (EMI). Single-shielded cables only provide about -55 dB of attenuation, while double-shielded cable provides -110 dB of attenuation [55]. This reduced the ambient electric fields near the cables when measured with a small monopole antenna connected to a spectrum analyzer.

I then repeated the earlier experiments, where I changed the input signal phase randomly from channel to channel and record to record. Fig. 3.17b shows that the resulting power of the second harmonic was far more stable. The changes to the test bed significantly improved the isolation between channels and eliminated the variation between captures.

3.3 Test Bed Characterization

Each ADC was fully characterized to ensure it meets specifications in the following areas:

- Equivalent Input Referred Noise (EIRN)
- DC Offset
- Full-Scale Power
- Frequency Response
- Noise Figure
- Signal-to-Noise Ratio
- Spur-Free Dynamic Range
- Integral and Differential Nonlinearities (INL and DNL)

3.3.1 Equivalent Input Referred Noise and DC Offset

The EIRN is a measure of the internal noise of the ADC without an input signal, which adds sampling noise. EIRN was measured by terminating the input of the ADC and measuring the standard deviation of the resulting noise [1]. Several captures were taken to reduce any fluctuations in the measurement. The DC offset is found by calculating the mean output for the same data. The data sheet specifies a 78 dBFS noise power, which is about $10\,\Delta^2$ with gain off and $17\,\Delta^2$ with gain on [45]. The DC offset is specified as ± 2 mV, which is $60\,\Delta$ with gain off and $90\,\Delta$ with gain on.

Fig. 3.18 shows that the measured EIRN for all 16 ADCs meet specification.

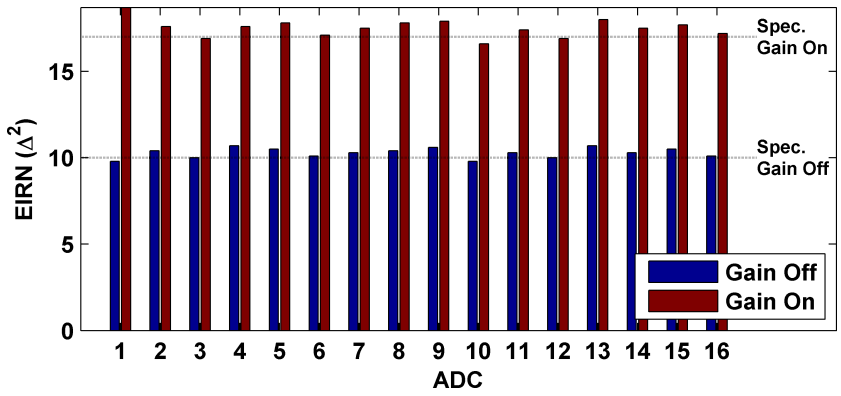

Figure 3.18: ADCs meet EIRN specification.

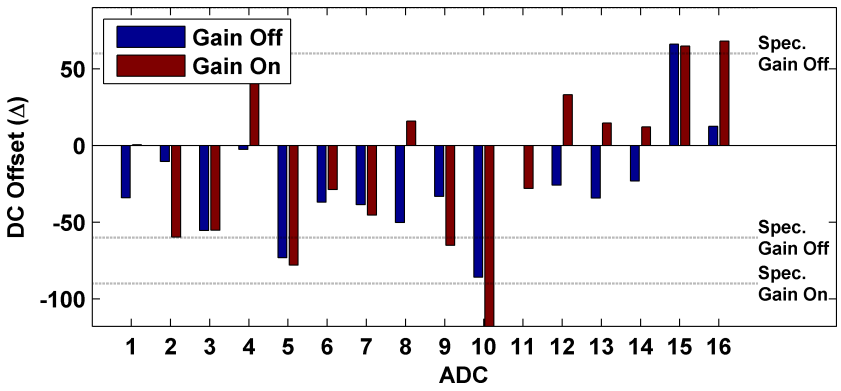

Figure 3.19: The DC offset of some ADCs are out of specification, but this does not impact correlation measurements.

Fig. 3.19 shows that the DC of some of the ADCs is out of specification; however, this does not impact the performance on these experiments.

3.3.2 Full-Scale Power and Frequency Response

The full-scale voltage of the LTC2208 is 2.25 V with the gain off and 1.5 with the gain on. The full-scale power in a 50 Ω system is 11.0 and 7.5 dBm with gain off and on. The measured full-scale power differs from the expected power due to gain errors in the ADC and loss from the input RF transformer.

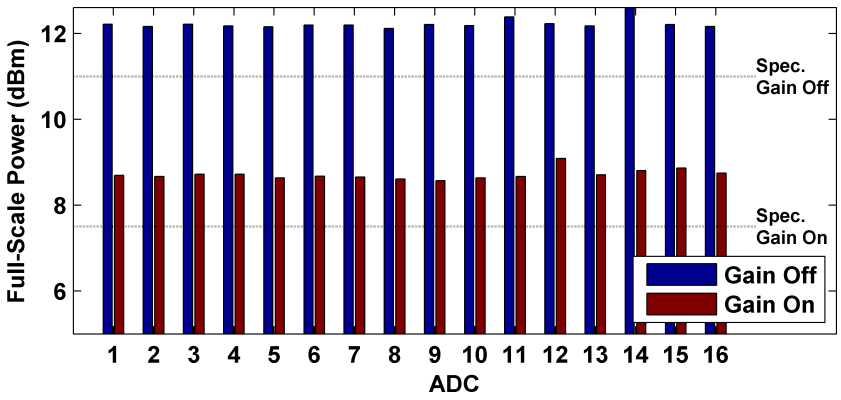

Figure 3.20: Measured full scale power shows good matching between channels and RF transformer loss of about 1 dB.

I measured the full-scale power by connecting a sinusoidal signal (from a signal generator) to the input of the ADC and capturing the output. I increased the input power in 0.01 dB increments in an automated loop until a sample on the ADC output was at full-scale. The input frequency must be chosen to excited many different output bits [1]. I then measured the signal that caused saturation on the spectrum analyzer. Fig. 3.20 shows the measured results. The RF transformer loss is about 1 dB.

3.3.3 Frequency Response

I measured the magnitude frequency response by applying a 75 MHz sinusoidal signal to the ADC and measuring the input power at the ADC. Then, using an automated loop, I changed the frequency in small increments and measured the power of the ADC data. Fig. 3.21 shows the frequency response is basically flat over the frequency bands of the anti-aliasing filters. Fig. 3.22 shows that the 1 dB

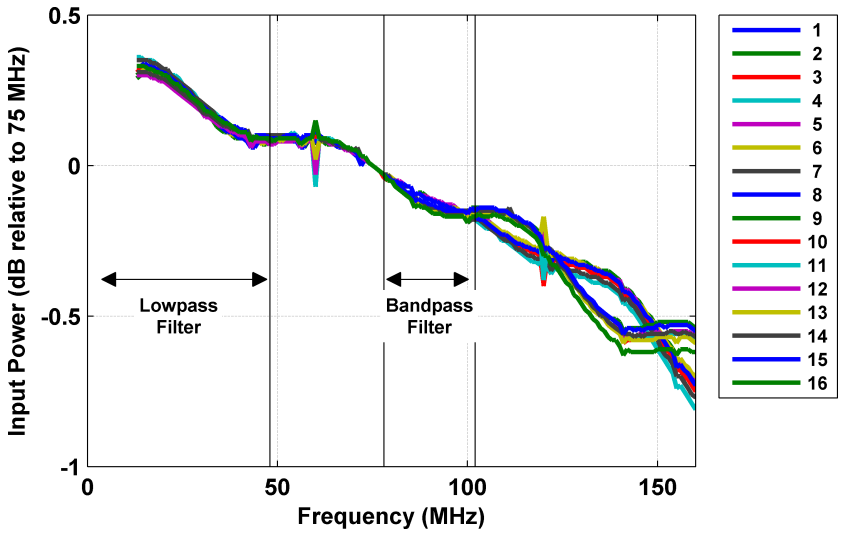

Figure 3.21: Measured frequency response shows increasing loss as frequency increases and excellent matching from channel to channel (small gain error).

and 3 dB (relative to a 75 MHz input) bandwidths are about 180 MHz and 280 MHz for each ADC.

3.3.4 SNR

I did not directly measure the maximum SNR, since the noise of the signal generators is well above the noise of the ADC. The SNR is inferred through

$$\mathrm{SNR(dB)} = P_{\mathrm{FS}} - (-174 + \mathrm{NF} + 10\log_{10}(f_s/2). \tag{3.7}$$

Fig. 3.23 the SNR matches the data sheet specification when RF transformer loss is included.

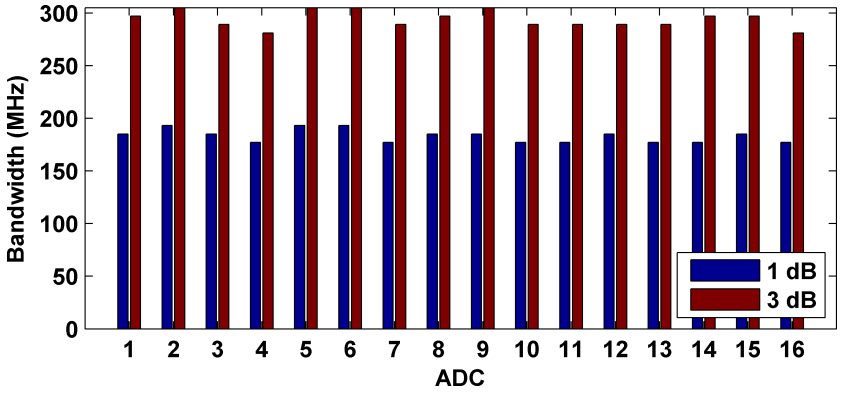

Figure 3.22: The 1 dB and 3 dB bandwidths are about 180 MHz and 280 MHz for all ADCs.

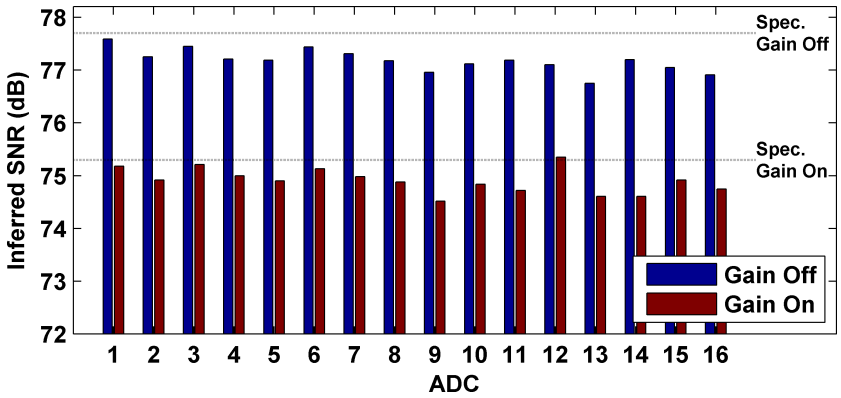

Figure 3.23: Measured SNR matches the specification when RF transformer loss is included.

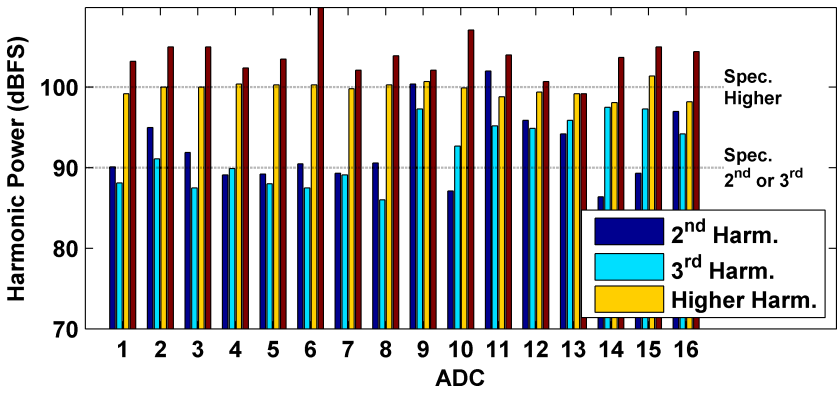

Figure 3.24: Measured SFDR with gain off.

3.3.5 Spur-Free Dynamic Range

SFDR is the ratio of the full-scale signal over the highest spur. The highest spur is usually the second or third harmonic of the input signal. I measured the SFDR by applying a nearly full-scale signal at 98.5 MHz from a signal generator to the ADC through an anti-aliasing filter. I measured the power of the ten largest spurs after filtering known signal generator spurs. Figures 3.24 and 3.25 show the measured SFDR with gain off and on. The data sheet specification is 90 dBc and the second and third harmonics do not always meet this, but all higher order harmonics do. With gain on, the third order harmonic power seems to decrease.

3.3.6 Integral and Differential Nonlinearities

To characterize our ADCs, I measured the performance metrics differential and integral nonlinearities (DNL and INL) of each channel [1]. DNL is the difference in the measured step size between each ADC output bit from the ideal step size Δ. INL is the deviation of the transfer function from the ideal transfer

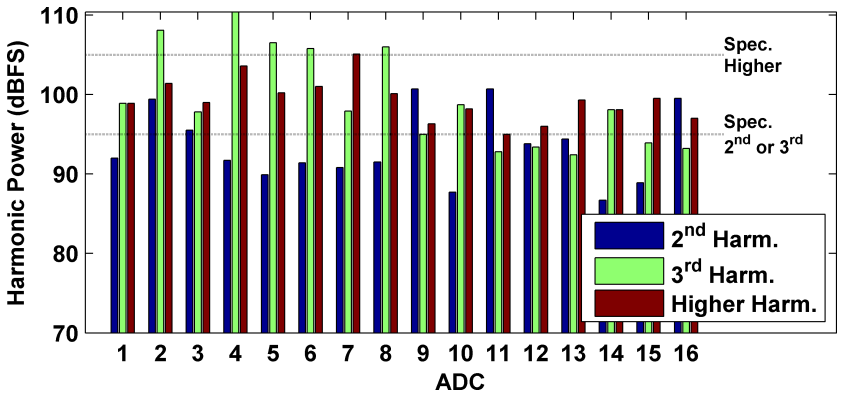

Figure 3.25: Measured SFDR with gain on, which, in general, improves the third order harmonic performance.

function, and is also the cumulative sum of the DNL.

I measured the DNL and INL of the 16 ADCs using a sine histogram test described in IEEE Standard 1241-2000 [56]. In the sine histogram test, I collect many samples of a high purity signal to form a large histogram. I then determine the DNL and INL from the deviation of the histogram from the ideal case. The test requires a large number of samples for each ADC output bit to reduce the measurement error. For each ADC, I recorded 91 000 different captures each with a length of 65 536 samples. Fig. 3.26 shows a block diagram of the sine histogram measurement setup. I overdrove the input about 0.5 dB, which is more than enough according to the standard. The frequency 30 503 540.04 Hz was selected, such that the number of cycles per record 16 659 is relatively prime with the record length 65 536. The 1 MHz narrowband filter is included to suppress signal generator spurs and reduce source noise, both of which are necessary to achieve the required spectral purity.

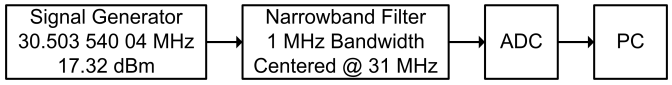

Figure 3.26: Block diagram of INL measurement setup. The signal frequency was chosen such that the number of cycles per record 16 659 is relatively prime with the record length 65 536. The filter improves the purity of the test signal, reduces spurs and noise.

Fig. 3.27 shows the measured INL for all 16 channels. Each subplot shows four ADC channels. Ideally, the INL would be 0 for all output bits of the ADC, but this is clearly not the case. For most ADCs, the INL is within $\pm 2\Delta$. The INL measurements show a large scale "sinusoidal" or "polynomial" structure and a small scale "jagged" structure. The large scale structure of the INL measurements is similar among some channels, but not others. I, therefore, expect the errors due to these transfer functions to be at least partially correlated.

The measured INL meets the manufacturer's specifications of a typical error of $\pm 1.2\Delta$ and a maximum INL error of $\pm 4.0\Delta$ [45]. Furthermore, to verify the fidelity and repeatability of our measurements over multiple runs, I took 3 INL measurements of the same ADC. Fig. 3.28 shows excellent matching between measurements of the same ADC, which provides confidence that our measurement technique is accurate and consistent. The count by count RMS difference of the INL between Run 1 and Run 2 is 0.0198Δ, between Run 1 and Run 3 is 0.0237Δ, and between Run 1 and Run 3 is 0.0183Δ showing excellent reproducibility.

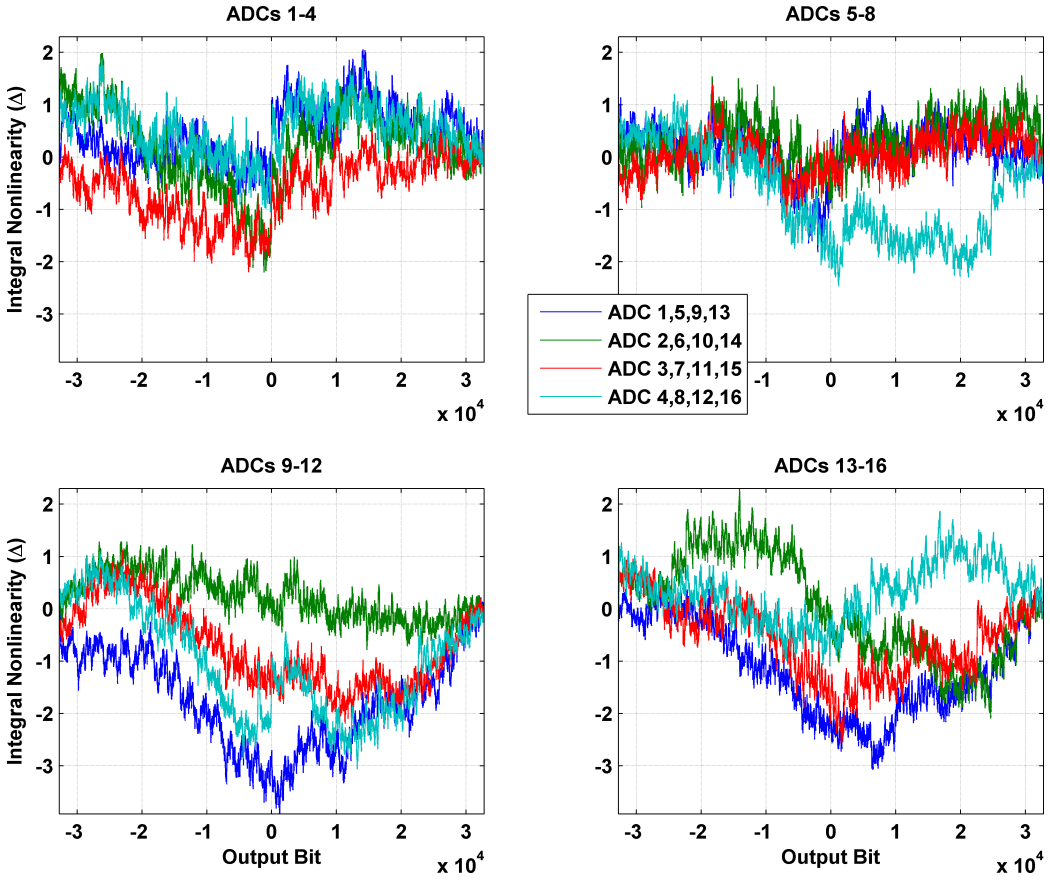

Figure 3.27: Measured INL from all 16 ADCs show complexity of quantizer transfer function errors. The large scale structure exhibits similarities from channel to channel, implying some level of correlation.

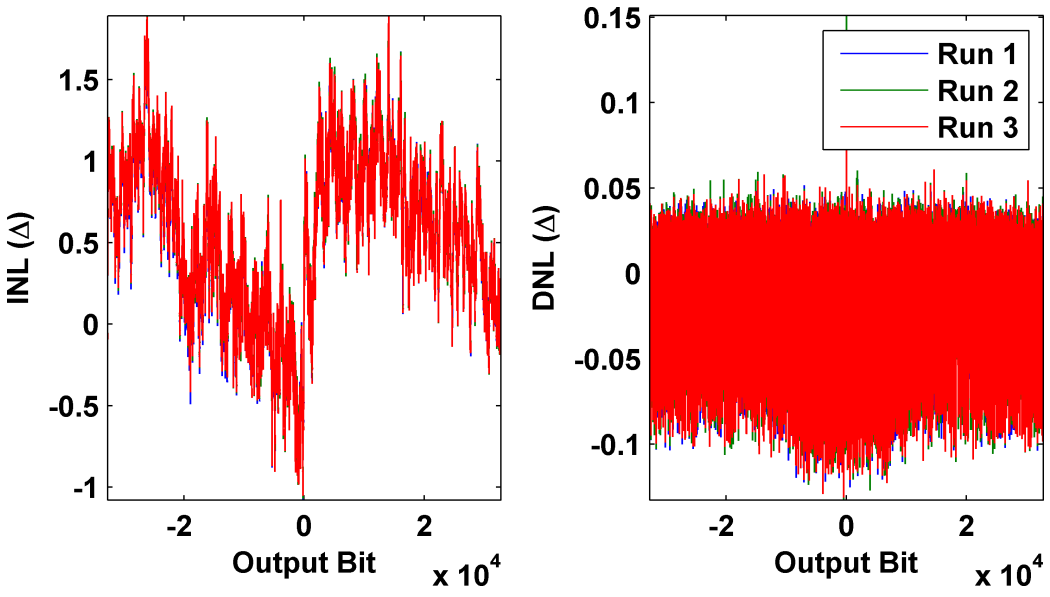

Figure 3.28: Three measurements of INL and DNL from the same ADC prove the excellent reproducibility of the measurements.

3.3.7 Characterization of DDSs

The DDS noise is dominated by phase noise. Fig. 3.29 shows a plot of the phase noise profile. For these experiments the white noise region $>$ 1 MHz is more important than lower offset frequencies. The phase noise in the white region is -150 dBc/Hz. The phase noise was measured using a in-house phase noise measurement test set. The inherent phase noise of the measurement system is well below the phase noise of the DDS.

The DDS includes a low pass reconstruction filter, which cause a non-uniform frequency response. The cutoff frequency of the 7-pole Chebyshev filter is 360 MHz.

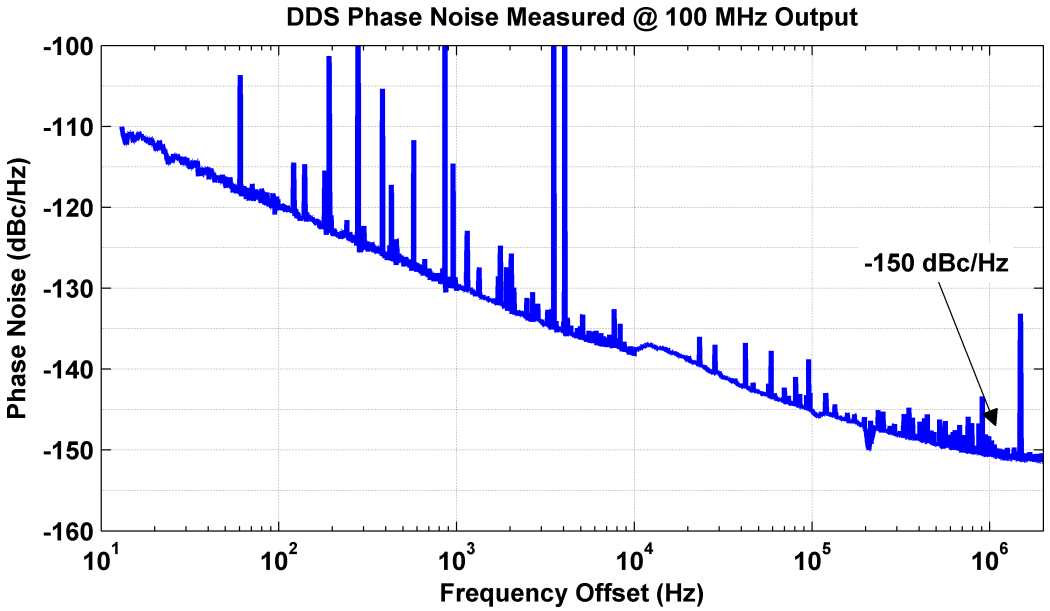

Figure 3.29: DDS phase noise at 100 MHz output frequency with 800 MHz clock.

3.3.8 Characterization of 120 MHz Clocks

The power output of each channel is 11.5 dBm. Each channel connects to two ADCs through a RF splitter and the power at the ADC is about 8 dBm. The recommended power is 12 dBm, but this should have negligible performance impact and it is impractical to increase the gain by only 3 dB.

The oscillators in clock array are very low noise. All of the oscillator components are from Wenzel Associates, Inc. The measured phase noise is about -170 dBc/Hz for frequencies greater than 10 kHz. This exceeds the specification of -165 dB/Hz.

The clock phase noise is low enough that it does not increase the ADC noise floor significantly. The phase noise PN is converted to timing jitter through

$$\mu = \frac{\sqrt{2 \cdot 10^{(\mathrm{PN}+10\log_{10}(B))/10}}}{2\pi \cdot 120 \times 10^6}, \tag{3.8}$$

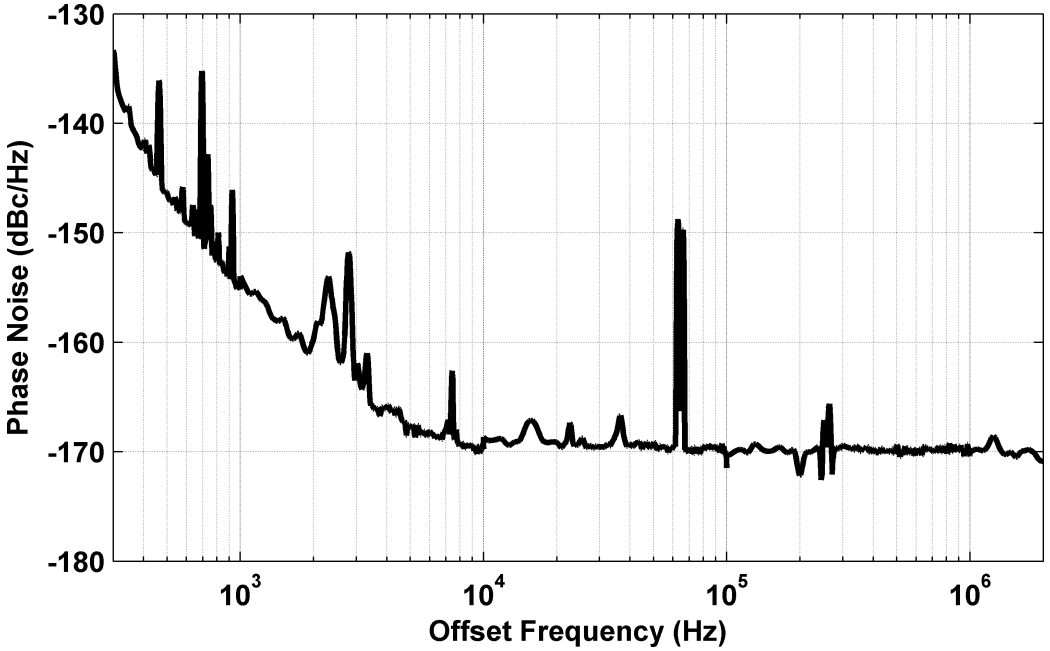

Figure 3.30: Measure phase noise is below white floor specification of -165 dBc/Hz.

where B is the clock input bandwidth of the ADC [1]. I estimated the clock input bandwidth as about 150 MHz based on the equivalent circuit in the data sheet [45]. The timing jitter μ, based on estimated bandwidth and the measured phase noise, is 73 fs. Fig. 3.31 shows the SNR reduction at the maximum frequency of interest is about 2 dB. This is insignificant relative to the phase noise of the DDSs.

3.3.9 Characterization of 800 MHz Clock

The 800 MHz clock is also very low noise. The 100 MHz oscillator has lower noise than the 120 MHz oscillators; it is -174 dBc/Hz. I was not able to measure the phase noise, but Fig. 3.32 shows the specified phase noise from components. The clock phase noise at the output of the DDS is reduced by the ratio of the output frequency over the clock frequency. The clock phase noise contribution

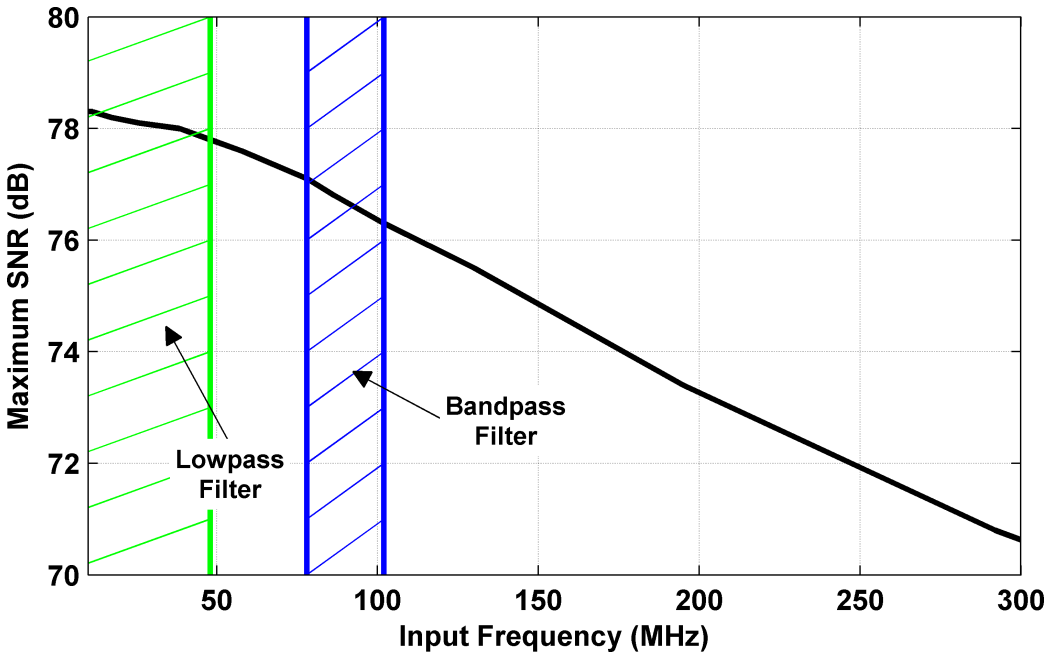

Figure 3.31: The SNR is reduced by 2 dB at the highest frequency of interest.

to the DDS phase noise at 90 MHz is

$$20\log_{10}\left(\frac{f_{\text{out}}}{f_{\text{clock}}}\right) = 20\log_{10}\left(\frac{90}{800}\right) = -19 \text{ dB} \tag{3.9}$$

lower than the specified clock noise.

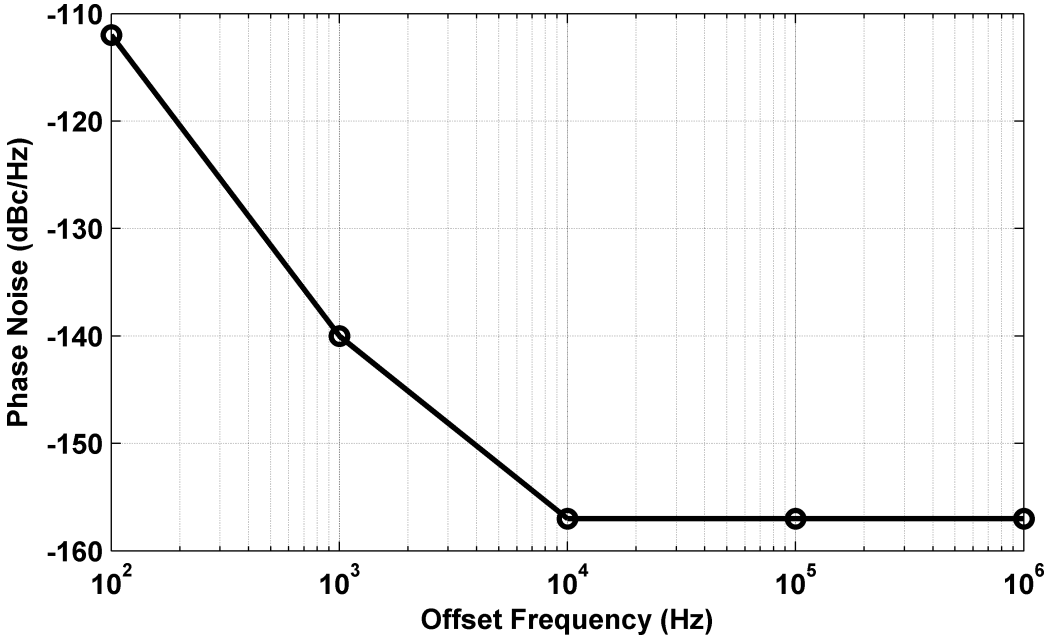

Figure 3.32: The phase noise of the 800 MHz clock is very low.

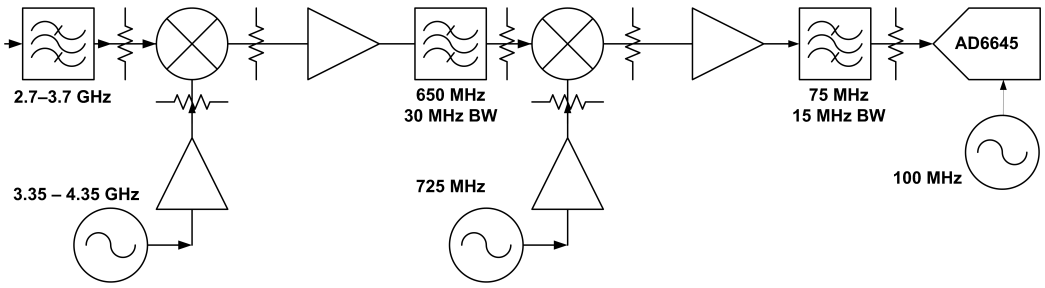

Figure 3.33: Block diagram of S-band receiver.

3.4 Design and Characterization of S-Band Receiver for CPCR Measurements

The S-Band receiver used to make CPCR measurements was designed by Joe Sluz, Matt Gerwell, and Al Wu [6]. The receiver has an RF bandwidth from 2.7-3.7 GHz and an instantaneous bandwidth of 15 MHz. The receiver uses two downconversion stages with the first LO variable from 3.35 to 4.35 GHz, and the second LO fixed at 725 MHz. The ADC is an Analog Devices AD6645, which is 14 bits and sampled at 100 MHz. The receiver parameters are listed in Table 4.1.

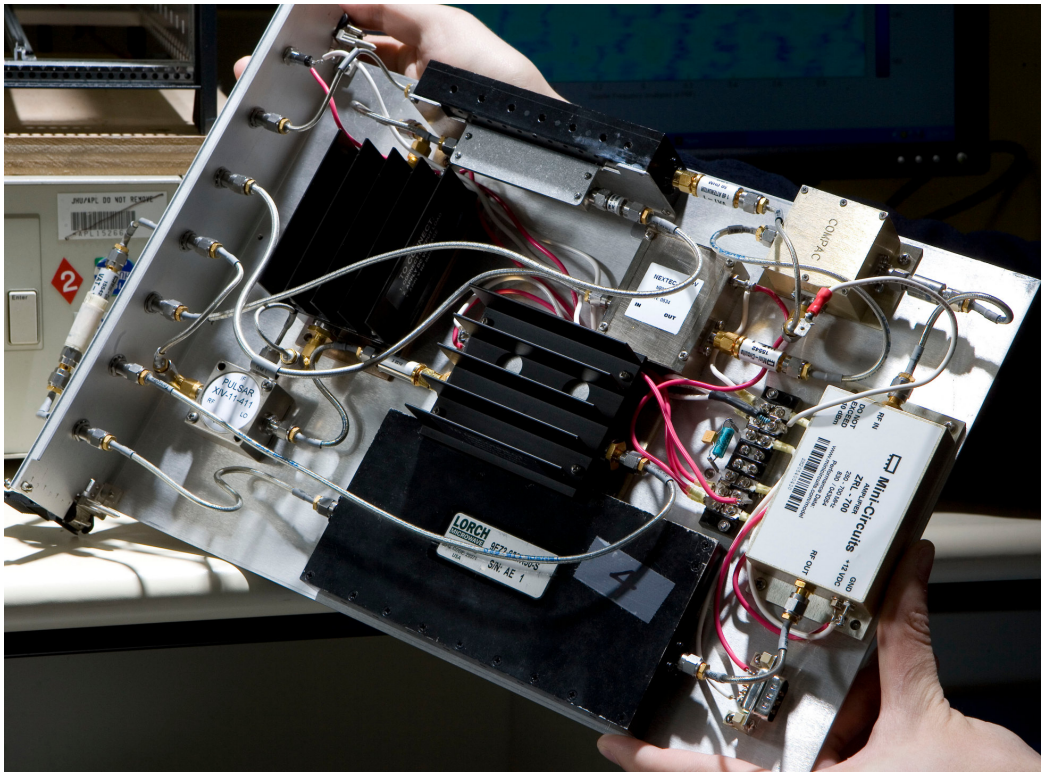

Figure 3.34: Photo of S-band receiver.

3.5 Summary of Chapter

In summary, I have developed a unique test bed using 16 state-of-the-art ADCs to investigate noise and distortion correlation. The test bed was designed around four design goals:

- Large number of channels
- Low noise and spur measurement system
- Excellent signal correlation
- Excellent isolation between channels

Each design goal was met. In addition, the test bed was throughly characterized.

Chapter 4

Correlation of Signals

Interference cancellation techniques in multi-channel radar and communications system, such as adaptive beamforming, are only effective if the response of each channel used is well matched [15, 16]. Though hardware variations between channels limit the intrinsic channel response match, digital equalization techniques improve channel-to-channel matching. Receiver channel nonlinearities, however, limit the level of channel matching achievable.

CPCR is a measure of the matching between two channels, which I define as the ratio of the output power of a reference channel P_{out} to the output power of the difference of the output signals (residue) P_r,

$$\text{CPCR} \triangleq \frac{P_{\text{out}}}{P_r}. \tag{4.1}$$

CPCR may be defined either as (4.1) or its reciprocal; I use (4.1) so that the CPCR is greater than 1 and a maximum CPCR describes the highest degree of channel matching instead of a minimum. CPCR measures the digital equalizer performance. In addition, CPCR may be used to infer higher level system parameters, such as *null depth* in an interference cancellation system, although, CPCR is not a direct measure of these characteristics [57, 58].

Experimentally, CPCR is measured by applying the same input signal to the two channels under test, either with or without digital equalization, and subtract-

ing the two outputs to find P_r. In order to reveal any mismatch within the channel bandwidth, the CPCR measurement signal should excite all frequencies within the bandwidth. The most desirable input signals will equally excite all frequencies within the channel bandwidth. Among the choices of excitation signals, linear frequency modulation (LFM) and band-limited Gaussian noise (BLGN) waveforms satisfy this requirement, as they both exhibit uniform power spectral densities within the channel bandwidth [57]. They differ, however, in their temporal characteristics: LFM sequentially excites each frequency, while BLGN excites all frequencies simultaneously.

In this paper, I compare the effect of the use of LFM and BLGN measurement signals on CPCR, and seek to determine the effect of hardware nonlinearities, including ADC saturation and analog-component third-order nonlinearities, on the measurement of CPCR. I do not directly evaluate the advantages or disadvantages of either signal for training purposes to generate equalization coefficients. In Section 4.1, I describe the hardware model used and determine the impact of noise on the CPCR. In Section 4.2, I determine the impact of ADC saturation on LFM and BLGN, and, in Section 4.3, I determine the impact of third-order nonlinearities. Finally, in Section 4.4, I experimentally confirm the results using a pair of S-band receivers. I show that the maximum achievable CPCR is lower for BLGN than LFM measurement signals due to ADC saturation and third-order nonlinearities.

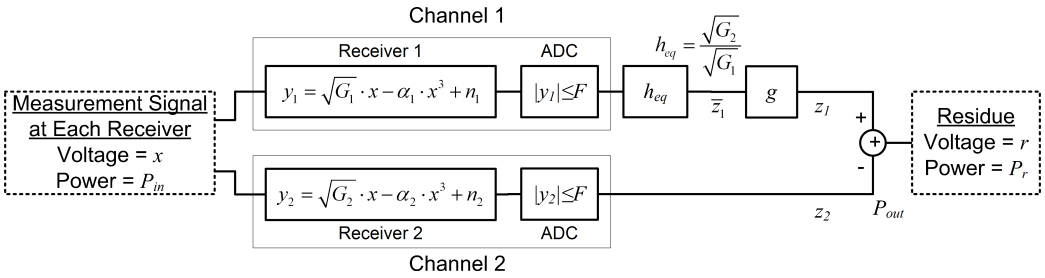

Figure 4.1: Block diagram of the CPCR measurement. Each channel contains a single receiver, and one of the legs possesses a digital equalizer h_{eq} and a single-tap equalizer g. Our receiver model includes both third-order nonlinearities and noise contributions, and the ADC model specifies the ADC full-scale voltage, F.

4.1 CPCR Measurement Technique and Receiver Model

Fig. 4.1 shows a detailed block diagram of our CPCR measurement setup. In this approach, CPCR is measured by applying a common input signal, denoted "measurement signal," to both channels under test. The equalizer is trained to match Channel 1 to Channel 2. The outputs are digitally captured and the difference is taken. The residual power P_r and CPCR are then measured.

Channel 1 consists of a receiver, modeled to include third-order nonlinearities and thermal noise, an ADC, a digital equalizer h_{eq}, and a single-tap adaptive equalizer g. Channel 2 consists of a similar receiver, again modeled with third-order nonlinearities and noise, and an ADC. As Channel 2 is considered the "reference" channel, no equalizer is included in that leg. The noise of the ADC is assumed to be included in the receiver noise and the ADC clips signal voltages with magnitudes greater than the full-scale voltage F. Throughout the analysis,

I assume a uniform magnitude frequency response and no phase error, such that the channel gain completely accounts for all differences between channels. I also assume the equalizer is perfectly calibrated and completely cancels the measurement signal when the receiver is operating linearly; the adaptive equalizer g only corrects for nonlinearities. I make these assumptions for mathematical simplicity and to address more effectively the effects of nonlinearities. A complete listing of parameters from Fig. 4.1 follows:

- x is the common measurement signal.
- y_i is the output voltage of receiver i,

$$y_i = \sqrt{G_i}x - \alpha_i x^3 + n_i. \tag{4.2}$$

- z_i is the output voltage of channel i. For Channel 1, z_1 is the output after the single-tap equalizer g, and $\bar{z}_1$ is the output before g.
- G_i is power gain of receiver i, $G_1 > G_2$.
- α_i is third-order voltage gain of receiver i and is related to the input third-order intercept (ITOI) by [59]

$$\alpha_i = \frac{2}{3}\frac{\sqrt{G_i}}{\mathrm{ITOI}_i R}. \tag{4.3}$$

  Note that ITOI is in Watts, α_i has units V^{-2}, and R is the impedance of the system. I use $R = 1\Omega$ for simplicity.
- n_i is output noise voltage of receiver i, including ADC noise.
- F is the full-scale voltage of the ADC and is the same for both receivers.
- h_{eq} is the equalizer gain, which, if I assume a uniform frequency response

in both channels, is

$$h_{eq} = \sqrt{\frac{G_2}{G_1}}.$$

- P_{in} is the measurement signal power, $\mathrm{E}[x^2]$.
- r is the residue voltage.
- P_r is the residue power, $\mathrm{E}[r^2]$.
- P_{out} is the output power of the reference channel, $\mathrm{E}[z_2^2]$
- g is an adaptive single-tap equalizer that minimizes the residue, and $g = 1$ if the equalizer is ideal.

The single-tap equalizer g is often included in digital equalization to correct for less than optimal equalizer weights h_{eq}. The adaptive equalizer is recalculated on shorter time intervals than the standard equalizer h_{eq}. For this work, I wish to understand the impact of the single-tap equalizer, if any, on the maximum CPCR.

The single-tap equalizer g minimizes the residue power over a collection of samples,

$$\frac{\partial}{\partial g} P_r = \frac{\partial}{\partial g} \mathrm{E}\left[(g_{opt}\bar{z}_1 - z_2)\right] = 0.$$

I solve the previous equation and find that the optimal g is

$$g_{opt} = \frac{\mathrm{E}\left[z_2 \bar{z}_1^*\right]}{\mathrm{E}\left[\bar{z}_1^2\right]}.$$

If the signals are well matched, such that $z_2 \approx \bar{z}_1$, as is the case for linear ADC operation, then $g \approx 1$ and the single-tap equalizer has no effect on the CPCR. When the signals differ, g adjusts the gain and phase to minimize the residue.

4.1.1 CPCR of Linear Channels

In this section, I determine the CPCR of two channels in the case of ADC linearity (no saturation, infinite F) and no third-order nonlinearities ($\alpha_1 = \alpha_2 = 0$). Assuming the equalizer perfectly matches the channels, such that $g = 1$, the input signal is fully canceled and the residue is simply the difference between the noise of each channel

$$r = \sqrt{\frac{G_2}{G_1}} n_1 - n_2.$$

The noise in each channel is independent and, as a result, the power of the residue is the sum of the two noise powers

$$\begin{aligned} P_r &= \mathrm{E}\left[r^2\right] = \mathrm{E}\left[\left(\sqrt{\frac{G_2}{G_1}} n_1\right)^2\right] + \mathrm{E}\left[(n_2)^2\right] \\ &= \frac{G_2}{G_1} P_{n,1} + P_{n,2} = N_t. \end{aligned} \tag{4.4}$$

N_t is about twice the noise power of a single channel, in other words, $N_t \approx 2P_{n,2}$ assuming that $G_2 \approx G_1$. I apply the residue power to (4.1) and find that the CPCR is

$$\mathrm{CPCR} = \frac{G_2 P_{\mathrm{in}}}{N_t} = \frac{P_{\mathrm{out}}}{2P_{n,2}}. \tag{4.5}$$

Therefore, the CPCR without nonlinearities is approximately half the output signal-to-noise ratio (SNR) of one receiver regardless of the type of measurement signal used. In practice, the CPCR increases linearly with increasing input power, until nonlinearities increase the residue and limit the maximum CPCR.

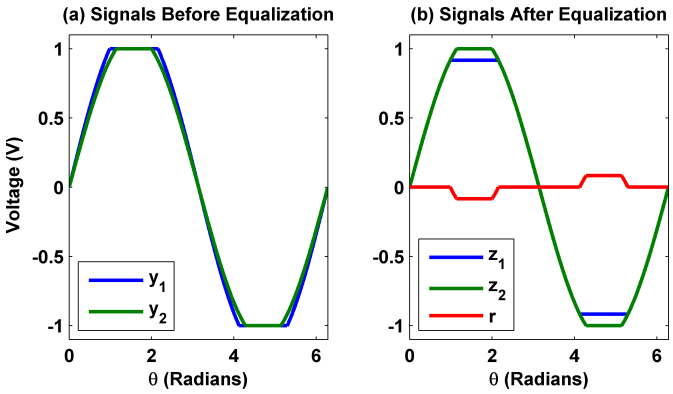

Figure 4.2: Demonstration of clipping on a sinusoidal input. The residue of saturated signals is increased relative to the unsaturated case.

4.2 CPCR Limitations Due to ADC Saturation

In the following analysis, I assume there are no third-order nonlinearities ($\alpha_1 = \alpha_2 = 0$). I also assume $g = 1$ for the analysis, although I allowed $g \neq 1$ in the simulations performed. ADC saturation results in the "hard" clipping of the receiver output signal y_i. Any signal voltage greater than F is limited to F, and any voltage less than $-F$ is limited to $-F$. After equalization, the output voltage z_i at saturation is different between channels due to the gain difference; therefore, when one (or both) signals saturate the ADC, the output voltages differ and the residue increases above zero (excluding noise), as depicted in Fig. 4.2. Fig. 4.2a shows the output of two channels with slightly different gains prior to equalization when both signals are saturated. Before equalization, the maximum voltage of each signal is $F = 1$ V. After equalization, shown in Fig. 4.2b, the maximum voltage of Channel 2 remains at F, but the maximum voltage of Channel 1 is $F\sqrt{G_2/G_1}$ and therefore the residue increases above zero (excluding noise).

The saturated transfer function of each channel is

$$z_i(x) = \begin{cases} F\sqrt{\frac{G_2}{G_i}}, & \frac{F}{\sqrt{G_i}} \leq x \\ \sqrt{G_2}x, & -\frac{F}{\sqrt{G_i}} < x < \frac{F}{\sqrt{G_i}} \\ -F\sqrt{\frac{G_2}{G_i}}, & x \leq -\frac{F}{\sqrt{G_i}} \end{cases}$$

assuming $\alpha_1 = \alpha_2 = 0$ and $g = 1$. As a result, the residue $r(x) = z_1(x) - z_2(x)$ is

$$r(x) = \begin{cases} F\sqrt{\frac{G_2}{G_1}} - F, & \frac{F}{\sqrt{G_2}} \leq x \\ F\sqrt{\frac{G_2}{G_1}} - \sqrt{G_2}x, & \frac{F}{\sqrt{G_1}} < x \leq \frac{F}{\sqrt{G_2}} \\ 0, & -\frac{F}{\sqrt{G_1}} \leq x \leq \frac{F}{\sqrt{G_1}} \\ -F\sqrt{\frac{G_2}{G_1}} + \sqrt{G_2}x, & -\frac{F}{\sqrt{G_2}} \leq x < -\frac{F}{\sqrt{G_1}} \\ -F\sqrt{\frac{G_2}{G_1}} + F, & x \leq -\frac{F}{\sqrt{G_2}} \end{cases} \tag{4.6}$$

As can be seen from (4.6), the residue power due to saturation depends intimately upon the likelihood that the input signal voltage saturates the ADC, and, as a result, the CPCR will vary depending on the specific input measurement signal used. By evaluating the variance of r for a given measurement input signal, the residue power due to saturation (including the noise) is

$$P_r = \int_{-\infty}^{\infty} r^2(x) \cdot f(x) dx + N_t$$

where $f(x)$ is the PDF of the measurement signal voltage x. The PDFs of both the LFM and BLGN measurement signals are symmetric about zero, so, from (4.6),

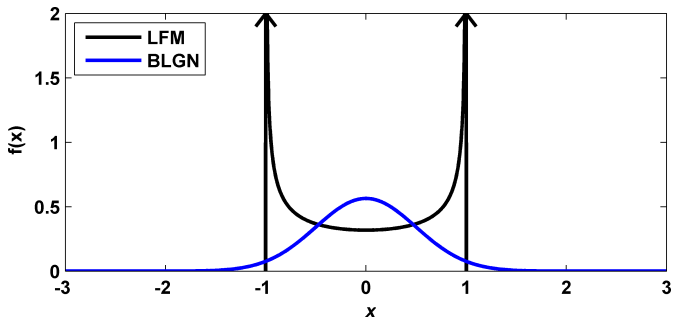

Figure 4.3: Comparison of LFM and BLGN probability density functions at the same power (LFM amplitude $A = 1$ and BLGN variance $\sigma^2 = \frac{1}{2}$).

the residue power simplifies to

$$P_r = 2 \int_{F/\sqrt{G_2}}^{\infty} \left(F\sqrt{\frac{G_2}{G_1}} - F \right)^2 f(x)dx + 2 \int_{F/\sqrt{G_1}}^{F/\sqrt{G_2}} \left(F\sqrt{\frac{G_2}{G_1}} - \sqrt{G_2}x \right)^2 f(x)dx + N_t. \tag{4.7}$$

With this relation, I can calculate the effect of saturation on residue power for an LFM and BLGN input signal. Note that (4.7) reduces to (4.4) when x does not saturate the ADC, in other words, when $|x| < F/\sqrt{G_1}$. Fig. 4.3 shows the PDF of the LFM (black) and BLGN (blue) measurement signals with the same power. Though both measurement signals have the same total power, the PDF varies significantly, with the peak-to-peak voltage variation much greater for BLGN than LFM. As a result, the saturated CPCR is expected to differ depending upon which measurement signal is used.

4.2.1 Effect of ADC Saturation on CPCR with LFM Measurement Signal

The PDF of an LFM measurement signal $x = A\sin(\theta(t))$ with amplitude A is [60]

$$f(x) = \begin{cases} (\pi\sqrt{A^2 - x^2})^{-1}, & x < |A| \\ 0, & \text{else} \end{cases} \tag{4.8}$$

Although LFM measurement signals are deterministic, the signal may still be represented as a PDF if I assume uniform random phase [60].

I find the residue power by substituting (4.8) into (4.7) and the result is

$$P_r(A) = \begin{cases} N_t, & A < \frac{F}{\sqrt{G_1}} \\ N_t + 2G_2 \int\limits_{\frac{F}{\sqrt{G_1}}}^{A} \frac{\left(F/\sqrt{G_1} - x\right)^2}{\pi\sqrt{A^2 - x^2}} dx, & \frac{F}{\sqrt{G_1}} < A < \frac{F}{\sqrt{G_2}} \\ N_t + 2G_2 \int\limits_{\frac{F}{\sqrt{G_1}}}^{\frac{F}{\sqrt{G_2}}} \frac{\left(F/\sqrt{G_1} - x\right)^2}{\pi\sqrt{A^2 - x^2}} dx & \\ \quad + 2F^2 \int\limits_{\frac{F}{\sqrt{G_2}}}^{A} \frac{\left(\sqrt{G_2/G_1} - 1\right)^2}{\pi\sqrt{A^2 - x^2}} dx, & \frac{F}{\sqrt{G_2}} < A \end{cases} \tag{4.9}$$

The resulting CPCR, using (4.1), is

$$\text{CPCR}(A) = \frac{G_2 A^2}{2P_r(A)}. \tag{4.10}$$

The maximum CPCR occurs when the residue power increases faster than the signal power. From (4.6), it can be concluded that, the residue power will increase dramatically when the signal saturates the ADC in Channel 1, that is, in the second interval, when $A > F/\sqrt{G_1}$. Referring to (4.9), the closed form

solution of the second interval is

$$P_r(A) = N_t + \frac{2}{\pi} G_2 \left(\frac{A}{2} - \frac{2F}{\sqrt{G_1}} \right) \sqrt{A^2 - \frac{F^2}{G_1}} + G_2 \left(\frac{A^2}{2} + \frac{F^2}{G_1} \right) \left(1 - \frac{2}{\pi} \sin^{-1} \frac{F}{A\sqrt{G_1}} \right). \quad (4.11)$$

From (4.11), I see that P_r increases quickly when A is greater than but near $F/\sqrt{G_1}$ since the derivatives the arcsine and square root functions are very large. A sample case that shows how the maximum CPCR is reached as a function of measurement signal power is in Section 4.2.3 below.

4.2.2 Effect of ADC Saturation on CPCR with BLGN Measurement Signal

I determine the CPCR with a BLGN measurement signal in the same manner, but substituting the PDF of BLGN,

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{x^2}{\sigma^2}} \quad (4.12)$$

into (4.7). The integrals may be solved analytically using error functions; however, I chose to evaluate them numerically, as shown below. The resulting CPCR is

$$\mathrm{CPCR}(\sigma) = \frac{G_2 \sigma^2}{P_r(\sigma)}. \quad (4.13)$$

4.2.3 Discussion of Maximum Saturation-Limited CPCR

Fig. 4.4 shows the CPCR as a function of the input measurement power for both LFM (black) and BLGN (blue) signals calculated by substituting (4.11) into

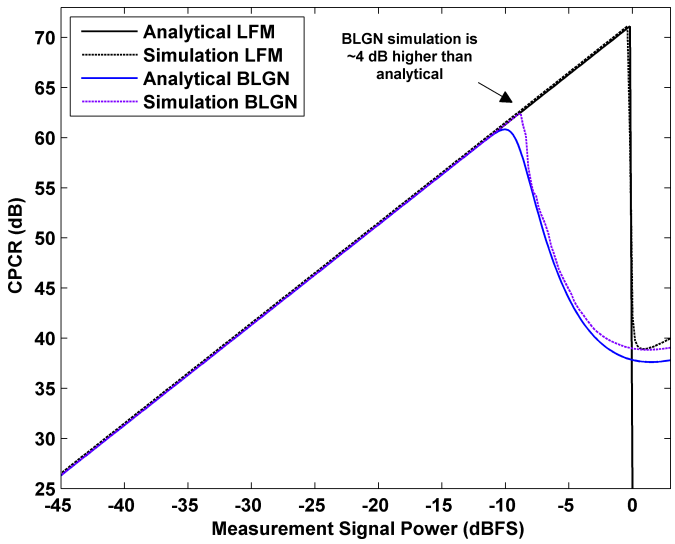

Figure 4.4: Analytical and simulated saturation-limited CPCR versus measurement signal power for the receiver parameters shown in Table 4.1. The maximum CPCR for BLGN measurement signal is 8 to 10 dB below that of the LFM measurement signal. For both measurement signals, the simulations closely match the analytical results.

(4.10) for LFM and (4.12) into (4.7) and (4.7) into (4.13) for BLGN using the receiver parameters in Table 4.1. The measurement signal power is in units of dBFS, which is dB relative to the full scale of the Channel 2 ADC (Fig. 4.1). In addition, Fig. 4.4 shows a numerically simulated CPCR (dotted) for each case. In the LFM simulation, I swept an ideal LFM measurement signal with 2^{15} samples through the system in Fig. 1 with $\alpha_1 = \alpha_2 = 0$ and receiver characteristics described in Table 4.1. I then calculated the residue and CPCR. The BLGN case was simulated similarly, using a 2^{15}-sample pseudorandom BLGN waveform as the measurement signal. In addition, the simulation included the adaptive equalizer g, although the analysis assumed $g = 1$.

Table 4.1: Measured Receiver Characteristics. The large difference in ITOI limits the CPCR for BLGN due to third-order nonlinearities.

Channel	Gain	Output Thermal Noise in 15 MHz	ITOI	ADC Saturation at ADC Input
1	7.8 dB	-70.7 dBm	22.0 dBm	5.5 dBm
2	7.6 dB	-67.4 dBm	18.6 dBm	5.5 dBm

As shown in Fig. 4.4, the CPCR increases linearly (it is noise limited) until about -10 dBFS for BLGN and about 0 dBFS for LFM, at which point the CPCR peaks. The maximum CPCR is lower for a BLGN measurement signal because the BLGN signal has a much larger peak-to-peak voltage for the same input power and, therefore, begins to saturate at much lower input powers. Fig. 4.3 clearly shows this large difference between the two types of signals.

For the LFM signal, the CPCR decreases rapidly once either channel saturates. The CPCR of the BLGN degrades at a much lower rate with increasing power, dropping off at about 5 dB per dB from -8 to -4 dBFS. Qualitatively the reason is that, though the BLGN signal has a large peak-to-peak voltage variation, at any given time the voltage is most likely to be closer to zero (Fig. 4.3). In contrast, the voltage of the LFM signal is most likely to occur at the peak voltage. Because of this characteristic, there is a sharp reduction of CPCR at saturation for the LFM waveform.

From Fig. 4.4, I note that for both the LFM and BLGN cases, the numerically simulated curves are in good agreement with the analytically calculated values. For LFM waveforms, the analytical and simulated maximum CPCRs match, while for the BLGN case, the simulated data possesses a maximum CPCR approximately 1.5 dB higher than the analytical calculation. This increase in CPCR is likely due to the limited number of samples in the simulation and the use of the adaptive g in the simulation. Recall the g was set to 1 in the analysis. The analytical solution includes the residue from the long tail of the BLGN PDF, while the simulation only includes a finite number of samples that tends to ignore the long tail contribution. The inclusion of the long tail causes a gentle peaking compared to the simulation, but the discrepancy is not large and the curves match at higher input powers. It is not clear whether the adaptive g increases the CPCR by better matching the saturated signals.

The maximum CPCR for both LFM and BLGN depends on the gain difference between channels. In theory, if both channels were perfectly matched before equalization, the maximum CPCR would be infinite since the saturation residues would exactly match. Recall from Fig. 4.2 that after equalization the saturation voltages are different. The maximum saturation-limited CPCR for the LFM signal occurs when the input signal A is just greater than $F/\sqrt{G_1}$, in other words, when Channel 1 saturates. Applying $A = F/\sqrt{G_1}$ to (4.5), the resulting maximum CPCR is

$$\mathrm{CPCR}_{\mathrm{max,LFM}} = \frac{F^2}{2N_t}\frac{G_2}{G_1} \approx \frac{\mathrm{SNR}_2}{2}\frac{G_2}{G_1} \tag{4.14}$$

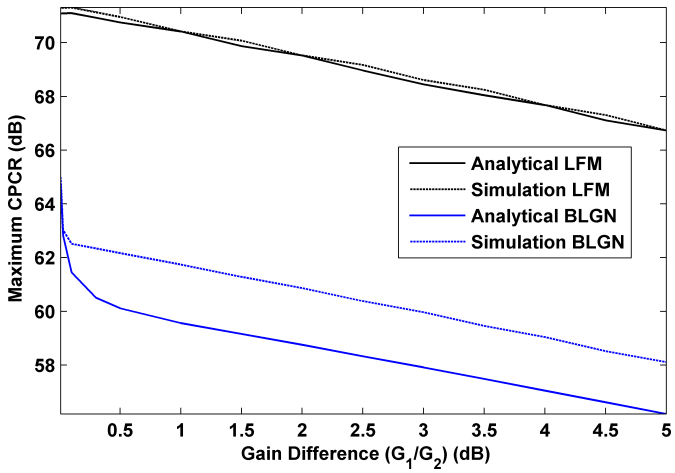

Figure 4.5: Saturation-limited maximum CPCR versus channel gain difference for both measurement signals. For both measurement signals, the maximum CPCR decreases approximately linearly with increasing gain difference.

where SNR_2 is the output signal-to-noise ratio of Channel 2. Fig. 4.5 shows the dependence of the saturation-limited maximum CPCR on the gain difference between channels for both LFM and BLGN. The simulated LFM line clearly matches (4.14).

The analytical solution (calculated numerically from (4.13)), shown in Fig. 4.5, is lower than the the simulation results. Since I earlier decided that the simulation is more accurate, I empirically determined that the maximum saturation-limited CPCR for a BLGN measurement signal from the simulation. I approximated the dotted blue line as

$$\mathrm{CPCR}_{\mathrm{max,BLGN}} \approx \frac{1}{6}\frac{F^2}{2N_t}\frac{G_2}{G_1} \approx \frac{\mathrm{SNR}_2}{12}\frac{G_2}{G_1}. \tag{4.15}$$

The maximum CPCR decreases linearly with increasing gain difference, with a slope of approximately 0.9 (due to the change in N_t with changing gain).

Fig. 4.5 also shows that if the gain is very well matched (< 0.1 dB) then the BLGN CPCR increases by several dB, although this behavior is not captured in (4.15). The maximum CPCR for channels with a 1 dB gain difference, which in our experience is representative of a typical system, is about $\mathrm{SNR}_{2,\mathrm{dB}} - 4$ dB for LFM and $\mathrm{SNR}_{2,\mathrm{dB}} - 12$ dB for BLGN, so the maximum CPCR is about 8 dB higher for LFM measurement signals, which is consistent with Fig. 4.4.

I can achieve the highest maximum CPCR through excellent analog gain matching before equalization. The maximum CPCR between different pairs of a larger set of receivers may vary substantially due to analog gain differences. Variations due to gain differences may be a significant source of CPCR variation in an otherwise identical set of receivers.

4.3 CPCR Limitations Due to Third-Order Nonlinearities

The analog components of any receiver are slightly nonlinear. Third-order nonlinearities generate intermodulation products of the measurement signals, which can increase the residue and limit CPCR. In this section, I will determine the impact of third-order nonlinearities on the maximum CPCR for LFM and BLGN measurement signals. Throughout this section I assume the channel is not saturated, such that $F \gg \sqrt{G_i}x$, and the $g \neq 1$.

4.3.1 Effect of Third-Order Nonlinearities on CPCR with LFM Measurement Signal

The LFM measurement signal is $x = A\sin(\theta(t))$, where $\theta(t)$ is the quadratic phase term of an LFM. The output voltage through Channel 1 of Fig. 4.1 is

$$z_1 = g\sqrt{G_2}A\sin\theta - g\sqrt{\frac{G_2}{G_1}}\alpha_1 A^3\sin^3\theta + g\sqrt{\frac{G_2}{G_1}}n_1.$$

I apply a trigonometric identity for $\sin^3\theta$ and the output voltage becomes

$$z_1 = g\sqrt{G_2}A\sin\theta - g\sqrt{\frac{G_2}{G_1}}\alpha_1 A^3\left(-\frac{1}{4}\sin 3\theta + \frac{3}{4}\sin\theta\right) + g\sqrt{\frac{G_2}{G_1}}n_1.$$

The third harmonic term $\sin 3\theta$ is filtered out prior to analog-to-digital conversion.

The filtered output voltage of Channel 1 is

$$z_1 = g\sqrt{G_2}A\left(1 - \frac{3}{4}\frac{\alpha_1 A^2}{\sqrt{G_1}}\right)\sin\theta + g\sqrt{\frac{G_2}{G_1}}n_1$$

and the similarly filtered output voltage of Channel 2 is

$$z_2 = \sqrt{G_2}A\left(1 - \frac{3}{4}\frac{\alpha_2}{\sqrt{G_2}}A^2\right)\sin\theta + n_2.$$

The residue using an LFM measurement signal is

$$r = \sqrt{G_2}A\left[g\left(1 - \frac{3}{4}\frac{\alpha_1 A^2}{\sqrt{G_1}}\right) - \left(1 - \frac{3}{4}\frac{\alpha_2}{\sqrt{G_2}}A^2\right)\right]\sin\theta + g\sqrt{\frac{G_2}{G_1}}n_1 - n_2. \tag{4.16}$$

The single-tap equalizer g completely cancels the $\sin\theta$ term and minimizes the residue when

$$g_{\min} = \left(1 - \frac{3}{4}\frac{\alpha_2}{\sqrt{G_2}}A^2\right) / \left(1 - \frac{3}{4}\frac{\alpha_1 A^2}{\sqrt{G_1}}\right). \tag{4.17}$$

Because the $\sin\theta$ term, which includes the effects of the third-order nonlinearity, can be fully removed with proper choice of g, third-order effects do not limit the maximum CPCR for LFM measurement signals. With $g = g_{\min}$, the CPCR is the same as the linear case (4.5).

4.3.2 Effect of Third-Order Nonlinearities on CPCR with BLGN Measurement Signal

The residue using a BLGN measurement signal is

$$r = \left(g\sqrt{G_2} - \sqrt{G_2}\right)x + \left(g\sqrt{\frac{G_2}{G_1}}\alpha_1 - \alpha_2\right)x^3 + \left(g\sqrt{\frac{G_2}{G_1}}n_1 - n_2\right). \tag{4.18}$$

I consider first the case $g = 1$ for which the linear term is fully canceled. To simplify the notation, let δ be the residual third-order voltage gain

$$\delta \triangleq \sqrt{\frac{G_2}{G_1}}\alpha_1 - \alpha_2. \tag{4.19}$$

The residue is

$$r = \delta x^3 + \left(\sqrt{\frac{G_2}{G_1}}n_1 - n_2\right) \tag{4.20}$$

and the power of the residue (after bandpass filtering) is

$$P_r = \delta^2 \,\mathrm{E}\left[\left(x^3\right)^2\right] + N_t = 12\delta^2 P_{\text{in}}^3 + N_t \tag{4.21}$$

where the power of the third-order term is derived in the Appendix.

The CPCR is then calculated to be

$$\text{CPCR} = \frac{P_{\text{out}}}{P_r} = \frac{G_2 P_{\text{in}}}{12\delta^2 P_{\text{in}}^3 + N_t}. \tag{4.22}$$

The optimal input power to maximize the CPCR is $P_{\text{in,opt}} = \sqrt[3]{N_t/24\delta^2}$. If the measurement signal power is greater than $P_{\text{in,opt}}$, the third-order nonlinearities dominate the residue and the CPCR decreases with increasing measurement power. As a result, the maximum CPCR limited by third-order nonlinearities with a BLGN signal is found by setting $P_{\text{in}} = P_{\text{in,opt}}$ and is

$$\text{CPCR}_{\text{max}} = G_2(9N_t\delta)^{-2/3}. \tag{4.23}$$

As seen above, unlike the LFM measurement signal case, third-order nonlinearities may limit the CPCR for BLGN measurement signals.

When I allow $g \neq 1$, I expect g to increase the CPCR slightly due to better matching of the third-order nonlinearity. This, however, decreases the linear matching, so the increase is expected to be small. This is explored further using simulations below.

In the same way gain differences between channels impact saturation-limited CPCR, ITOI differences impact nonlinearity-limited CPCR. High ITOI matching results in lower residue from third-order nonlinearities and a higher CPCR. From (4.3) and (4.19), I find the relationship between δ and the ITOI of each channel,

$$\begin{aligned}\delta &= \sqrt{\frac{G_2}{G_1}}\frac{2}{3}\frac{\sqrt{G_1}}{\text{ITOI}_1} - \frac{2}{3}\frac{\sqrt{G_2}}{\text{ITOI}_2} \\ &= \frac{2}{3}\frac{\sqrt{G_2}}{\text{ITOI}_2}\left(\frac{\text{ITOI}_2}{\text{ITOI}_1} - 1\right)\end{aligned} \tag{4.24}$$

Substituting (4.24) into (4.23)

$$\text{CPCR}_{\text{max}} = \left(\frac{G_2}{6N_t}\frac{\text{ITOI}_1 \cdot \text{ITOI}_2}{\text{ITOI}_2 - \text{ITOI}_1}\right)^{2/3} \tag{4.25}$$

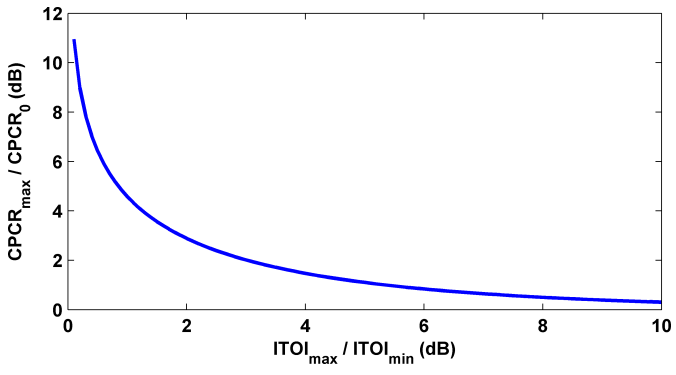

Figure 4.6: Maximum CPCR versus channel ITOI difference. Maximum CPCR increases above the worst-case maximum CPCR as the difference between ITOI decreases (in other words, as $\mathrm{ITOI_{max}}/\mathrm{ITOI_{min}}$ approaches 0 dB).

Because of the $2/3$ exponent, the sign of the denominator may be ignored and (4.25) may be written as

$$\mathrm{CPCR_{max}} = \mathrm{CPCR_0}\left(\frac{\mathrm{ITOI_{max}}/\mathrm{ITOI_{min}}}{\mathrm{ITOI_{max}} - \mathrm{ITOI_{min}} - 1}\right)^{2/3} \tag{4.26}$$

with

$$\mathrm{CPCR_0} = \left(\frac{G_2}{6N_t}\mathrm{ITOI_{min}}\right)^{2/3} \tag{4.27}$$

where $\mathrm{ITOI_{min}}$ and $\mathrm{ITOI_{max}}$ are the minimum and maximum ITOI of Channels 1 and 2.

Fig. 4.6 shows a plot of (4.26) over (4.27). Note that $\mathrm{CPCR_{max}} > \mathrm{CPCR_0}$ and that when $\mathrm{ITOI_{max}} \gg \mathrm{ITOI_{min}}$, then $\mathrm{CPCR_{max}} \approx \mathrm{CPCR_0}$. That is, $\mathrm{CPCR_0}$ is the worst-case $\mathrm{CPCR_{max}}$.

Since the CPCR varies for different channel pairs, when measuring the maximum CPCR using a BLGN measurement signal, it is best to measure many different channel pairs and analyze the CPCR statistically. The maximum CPCR

variation is larger due to third-order nonlinearities than ADC saturation.

4.3.3 Discussion of Maximum Third-Order Nonlinearity-Limited CPCR

In Section 4.3.1 I showed that, as long as a single-tap equalizer is available, the CPCR, when measured with an LFM measurement signal, is not limited by third-order linearities. On the other hand, in Section 4.3.2, I showed that nonlinearities do limit the CPCR measured using a BLGN signal, and argued that even with the single-tap equalizer in place the increase would be small. The maximum CPCR in the BLGN case was shown to be dependent on the residual third-order voltage gain δ.

Fig. 4.7 plots analytical and simulated CPCR for both LFM and BLGN as a function of the measurement power assuming $F \gg y_i$. The simulation was executed in a manner similar to that presented in Section 4.2.3, with the receiver model modified to include third-order nonlinearities and exclude saturation for the parameters in Table 4.1

Both the analytical and simulated results for LFM show no dependence on the third-order nonlinearities if I include g. When I exclude g, the CPCR is limited by third order nonlinearities.

Third-order nonlinearities clearly limit the maximum CPCR for BLGN measurement signals as expected from (4.23). The simulated results without g match the analytical results. With g included, the maximum CPCR increases by about

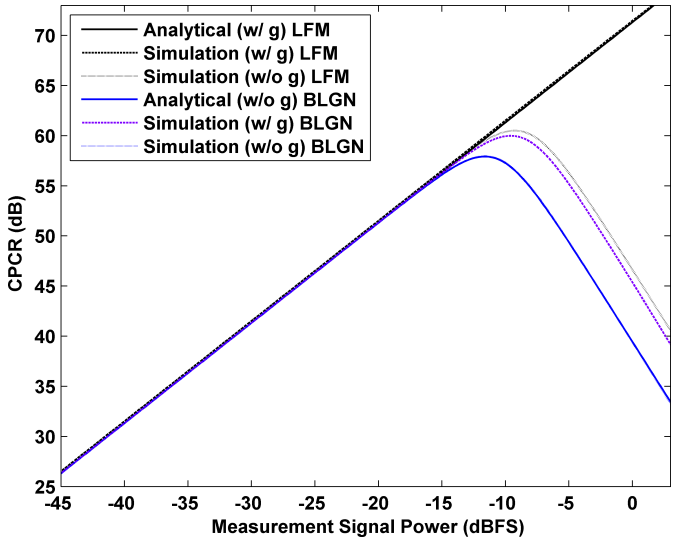

Figure 4.7: Maximum CPCR in the presence of third-order nonlinearities versus measurement signal power using the parameters in Table 4.1. With g, the maximum CPCR of the LFM measurement signal is not limited. For BLGN, the CPCR remains limited, but the inclusion of g increases the maximum CPCR by a few dB as predicted.

4 dB due to better matching between channels. The single tap equalizer g is not able to completely cancel the impact of third order nonlinearities like it does for LFM.

4.4 CPCR Limitations Due to Both ADC Saturation and Third-Order Nonlinearities

In Sections 4.2 and 4.3, I studied the effects of ADC saturation and analog third-order nonlinearities on CPCR, with each effect in the absence of the other. I now consider both effects together, analytically, experimentally and through simulation.

For our experiments, I used two S-band receivers with 15 MHz of instantaneous bandwidth and an RF bandwidth from 2.7 to 3.7 GHz [6]. The receivers have two down conversion stages and include analog-to-digital conversion. Table 4.1 lists the measured characteristics of the receivers. I reduced the LO drive power of the receivers from the previously published levels to increase the difference in ITOI and reduce the absolute ITOI level. This increases the residual third-order voltage gain and reduces the maximum CPCR due to third-order nonlinearities.

The equalizer is a finite-impulse response, deterministic least squares implementation [61]. I examined filter length, causal versus non-causal filters, and training length, and it was determined that 65 taps and 3000 training samples provide excellent performance over 15 MHz of bandwidth.

To assess the input power levels required to reach saturation, I measured the full scale power of Channel 2 by applying a sinusoid to the input and measuring the ADC output, increasing the input power until full scale was reached.

4.4.1 CPCR with LFM measurement signal

The CPCR when measured with an LFM measurement signal is only limited by saturation, not third-order nonlinearities, so long as the single-tap equalizer g is allowed to vary. The maximum CPCR is, therefore, (4.14).

To verify our analysis and simulations, I applied the same 15 MHz LFM waveform with a pulse duration of 100 μs to the input of the two receivers through a microwave power divider. I increased the power from -45 dBFS to +3 dBFS in 0.2 dB increments, which sweeps through the linear regime into Channel 1 saturation first and then Channel 1 and 2 saturation. New equalizer coefficients were calculated for each measurement and trained on the first 3000 samples. The equalizer was then applied to the captured data and the CPCR was measured using all 65 536 (2^{16}) samples taken. I included g to minimize the total residue. All measurements were made at 3.2 GHz.

The experimentally measured LFM CPCR is plotted as the black line in Fig. 4.8, along with the expected CPCR performance according to (4.14) in solid black. The measured CPCR does not go as high as analysis predicts, although the CPCR matches far from saturation and after saturation has been reached, demonstrating that ADC saturation provides an absolute limit on the measure CPCR.

The lower-than-expected CPCR in the near-saturation region appears to stem from uncorrelated spurs in the receivers, which originate from EMI, not third-order nonlinearities, and limit the total channel matching. Fig. 4.9 shows the LFM spectra recorded from both channels, as well as the residue between the channels. The sideband spurs are clearly evident (at 10 and 33 kHz offsets from the signal) in the Channel 1; however, the sideband spurs are either not present or are lower in the Channel 2 spectrum. These uncorrelated spurs do not cancel to the noise floor, and as a result, limit the degree to which the channels are matched (maximum achievable CPCR) and raise the noise floor.

The uncorrelated spurs are not due to nonlinearities, but are caused by some unknown EMI arising from isolation and grounding issues within the receiver rack, resulting in low frequency oscillations modulating the signal. The spur power is partially signal dependent, and I observe the same behavior when inputting a single tone. Without these spurs, the LFM CPCR would continue to increase until saturation is reached, verifying that, with the inclusion of the single-tap filter, the LFM CPCR is not limited by third-order nonlinearities.

4.4.2 CPCR with BLGN measurement signal

The CPCR, when measured with a BLGN measurement signal, is limited by both ADC saturation and third-order nonlinearities, although, normally only one determine limit the maximum CPCR. The total CPCR is found by substituting (4.12) into (4.7) to find $P_r(\sigma)$, and including $P_r(\sigma)$ in (4.22) (although including

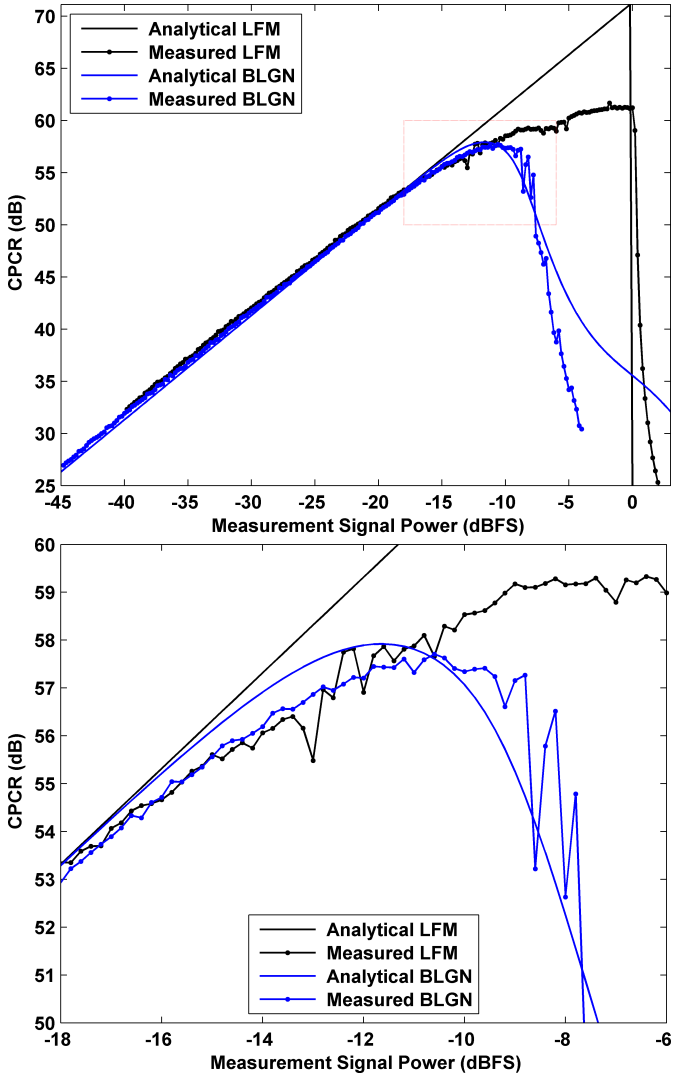

Figure 4.8: Experimentally measured CPCR versus measurement signal power for both LFM and BLGN measurement signals. The right hand plot is a close-up corresponding to the dotted region indicated on the left hand plot. For the BLGN case, the experimentally obtained data closely matches the expected CPCR; however, electromagnetic interference limited the CPCR measurement for the LFM case.

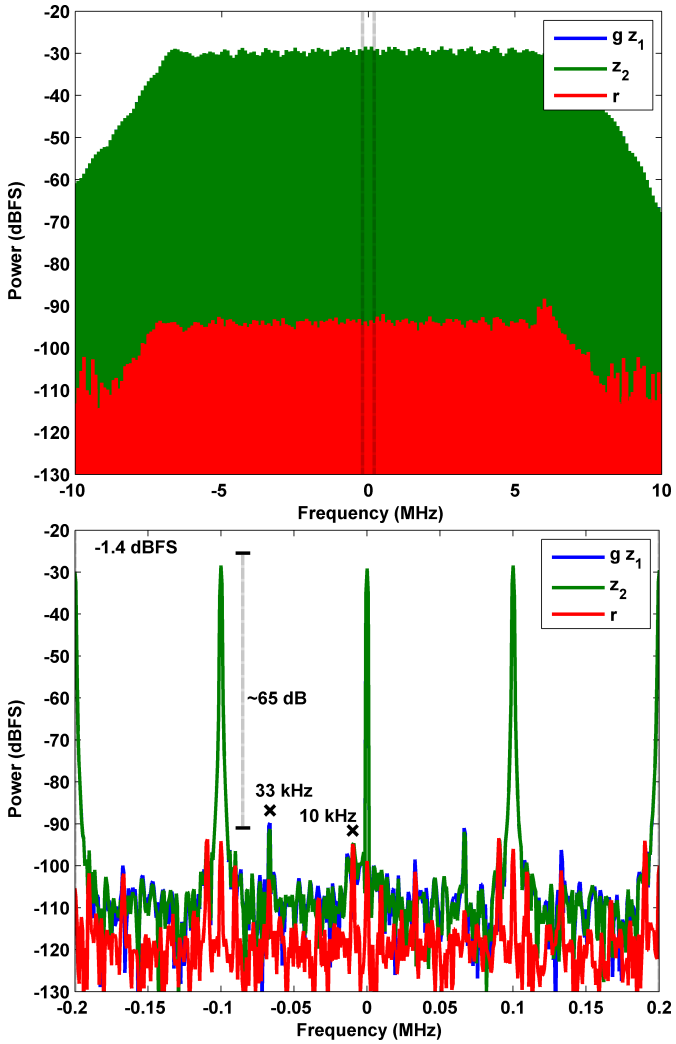

Figure 4.9: Output signal power of the equalized channel gz_1, reference channel z_2, and residue r versus frequency. The left hand figure shows the total 15 MHz LFM waveform and the right hand figure shows a narrow region of 400 kHz. Uncorrelated spurs in the equalized and reference channels limit channel matching and CPCR. Signals are canceled by over 65 dB, but sideband spurs limit total CPCR compared to ideal CPCR of about 70 dB.

only one N_t) to find the total CPCR

$$\text{CPCR} = \frac{G_2 P_{\text{in}}}{12\delta^2 P_{\text{in}}^3 + N_t + P_r(\sigma)}. \tag{4.28}$$

The maximum CPCR depends on δ: if δ is small, the maximum CPCR is ADC saturation limited; if δ is large, then the maximum CPCR is third-order nonlinearity limited and lower than the saturation-limited CPCR (4.15).

In order to experimentally measure the CPCR using a BLGN measurement signal, I applied a 15 MHz pseudorandom BLGN to the same two receivers and swept the power from -40 to -4 dBFS in 0.2 dB steps using the same equalization procedure described above. The pseudorandom noise sequence was longer than the capture time of the ADC, so the sequence did not repeat within a single capture.

The experimentally measured BLGN CPCR is plotted in blue in Fig. 4.8, with the analytically expected results in solid blue. There is excellent agreement between the expected and observed CPCR behavior. The measured curve shows the CPCR roll-off due to third-order intermodulation and the sharp drop-off near -9 dBFS as saturation begins. The measured CPCR is somewhat lower than the ADC saturation-limited predicted value in (4.15) when the channels enter saturation. This may be due, in part, to the same spurs that reduce the maximum CPCR of the LFM measurement, but may also be because the predicted value considers saturation of only one channel, not both channels, as is the case in our measurement.

4.5 Discussion

Our work has shown that the maximum CPCR of a pair of receivers is dramatically impacted by the measurement signal chosen. Particularly in the presence of saturation and third-order nonlinearities, the CPCR response can vary greatly depending upon whether an LFM or BLGN measurement signal is used. Even if the TOI of the receiver is very large such that the third-order nonlinearities are negligible, the maximum CPCR achievable with a BLGN measurement signal is approximately 8 dB below that obtained with an LFM measurement signal. The maximum CPCR in both cases is dependent upon the gain difference between channels, with the CPCR decreasing for increasing gain disparity. If third-order nonlinearity effects are significant, the BLGN CPCR may be further reduced, although the actual degradation depends on the ITOI difference between channels. If an adaptive single-tap equalizer is included in one of the channels, the CPCR of the LFM measurement signal is not affected by third-order nonlinearities. I verified the analytically-derived results with both simulated and experimentally obtained data.

Given the sensitivity of CPCR measurements to the properties of the measurement signal and the characteristics of the receiver pair used, any discussion of CPCR must include a specification of the measurement signal type and a discussion of the receiver gain and ITOI difference. In particular, for CPCR measurements made with BLGN, precise matching between a pairs of receivers may inflate the maximum CPCR relative to the average of many other receivers pairs.

In most cases, LFM is likely preferable to BLGN to measure the effectiveness of the equalization, since the maximum CPCR is higher by at least 8 dB. This gives a larger measurement dynamic range to see imperfections in the equalization (or, as in our case, EMI). CPCR also allows indirect inference of the performance of interference mitigation techniques. When CPCR is measured for these purposes, it may be more useful to use a waveform representing the typical interference, so that the effect of nonlinearities would be included.

Chapter 5

Correlation of Noise

There are three sources of noise in an ADC: thermal (and other random noise processes, such as shot noise), quantization, and sampling noise. Thermal noise is always independent between ADCs and is the largest source of noise in many modern ADCs. Quantization noise may be correlated between channels, but is typically below the thermal noise in modern ADCs and may be decorrelated using dithering [17]. Sampling noise (from clock or aperture jitter) is correlated when a common clock is used on all the ADC channels, and its magnitude depends on the input signal frequency and amplitude and the clock jitter.

5.1 Correlation of Thermal Noise

I designed the test bed to determine the dynamic range improvement due to combining many ADC channels in parallel. When the noise and distortion is uncorrelated then the SNR increase by a factor M. The signal power, which is correlated, increases by M^2, while the uncorrelated noise and distortion increases by M. Of the sources of noise in the test bed, I assumed that the white noise, usually dominated by the thermal noise, was uncorrelated from channel to channel. Fig. 5.1a shows the spectrum of the 16 channels with an input power of -28 dBFS and input signal near 97.6 MHz. I chose an input power well below full scale, so

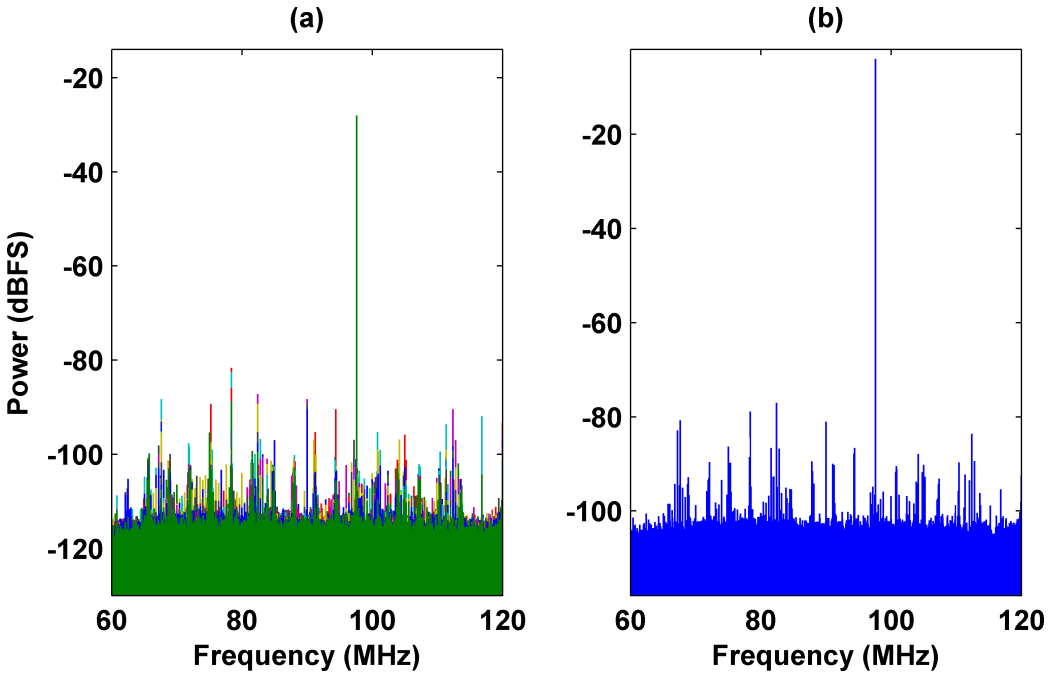

Figure 5.1: (a) Overlay of the spectrum of 16 channels with input signal of -60 dBFS. (b) Spectrum of 16 channels added in the voltage domain. The axis of (b) is offset by $10\log_{10}16$ = 12 dB, so that noise may be directly compared. At this input power, noise is uncorrelated and SNR is increased by 12 dB.

that the potentially correlated sampling was minimal. Fig. 5.1b shows the spectrum of the same signals added in the time domain. The y-axis of Fig. 5.1b is offset by 12 dB, such that uncorrelated noise is at the same level.

The noise appears uncorrelated in the plots. I measured the SNDR using the power spectra. I calculated the noise and distortion power by summing all the bins in the power spectrum and subtracting the power in the signal bin. The SNDR is the ratio of the power in the signal bin over the noise and distortion power. I calculated the SNDR for each channel and the combined signal and found that the SNDR increased by an average of 11.98 dB, which demonstrates the expected

SNDR improvement.

I conducted the same measurement using a single correlated tone across all channels for input powers from -52 dBFS to -0.1 dBFS. A signal offset from 98.1 MHz was applied to each channel and the phase and amplitude differences were removed using the calibration described earlier. I then captured 2^17 samples for each input power and converted the signal to the frequency domain using an FFT. I then measured the SNDR using by summing all bins except those containing the signal. I then measured the signal power bins.

Fig. 5.2 shows the measured noise and distortion power from the 16 channels and the combined channel. Below -15 dBFS, the noise and distortion remains constant around -74 dBFS. Above -15 dBFS, the noise and distortion power gradually increases to about -70 dBFS. The increase in noise and distortion power is likely due to increases in both distortion and sampling noise. The DDS noise power is < -75 within the 24 MHz filter bandwidth, so it is not likely to be the cause of the noise power increase.

Using the same data, I calculated D using (2.23) as across the same input powers, as shown in Fig. 5.3. Above -10 dBFS, I begins to degrade from 0 reaching a low value of -2.5 dB near full scale. This value of I indicates would result from a $\bar{\rho} \approx 0.05$.

For signals well below full scale, thermal noise is the dominate noise and distortion source and remains white and uncorrelated between channels regardless of the input signal. Near the full scale of the ADC the noise and distortion power increases significantly due to sampling noise and distortion from the ADC. These

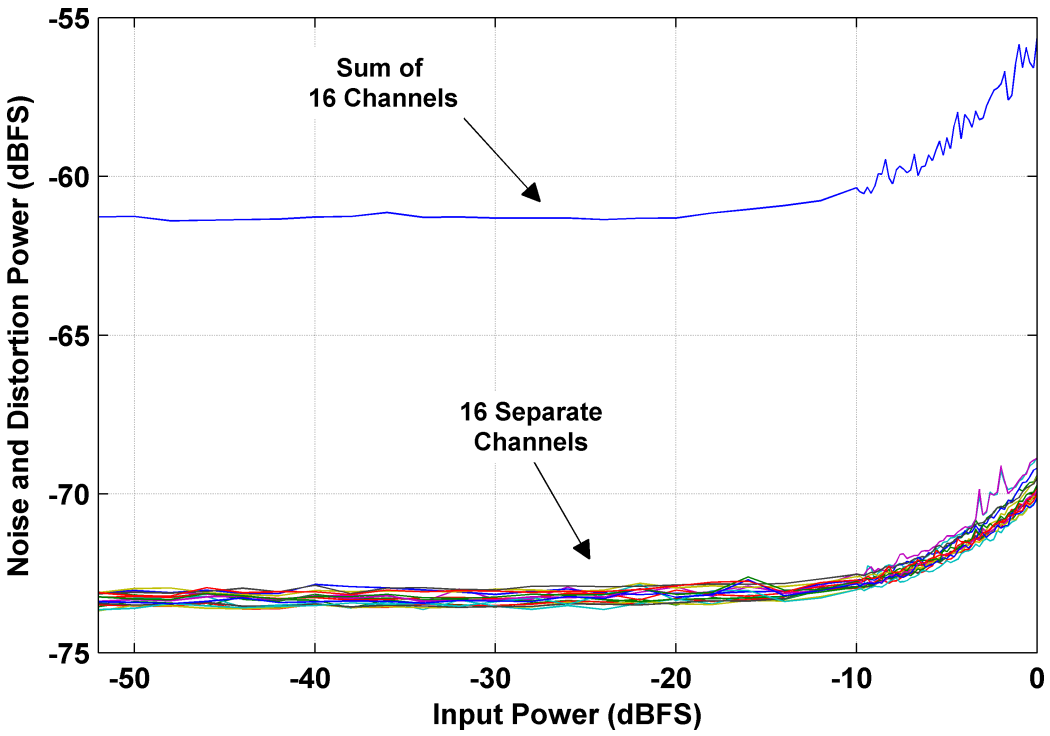

Figure 5.2: Plots of the noise and distortion power from the 16 channels as well as the combined channel. The noise and distortion power increases significantly near the full scale of the ADC. This is likely the result of increases in both distortion and sampling noise. The DDS signal source noise is < -75 dBc within the filter bandwidth.

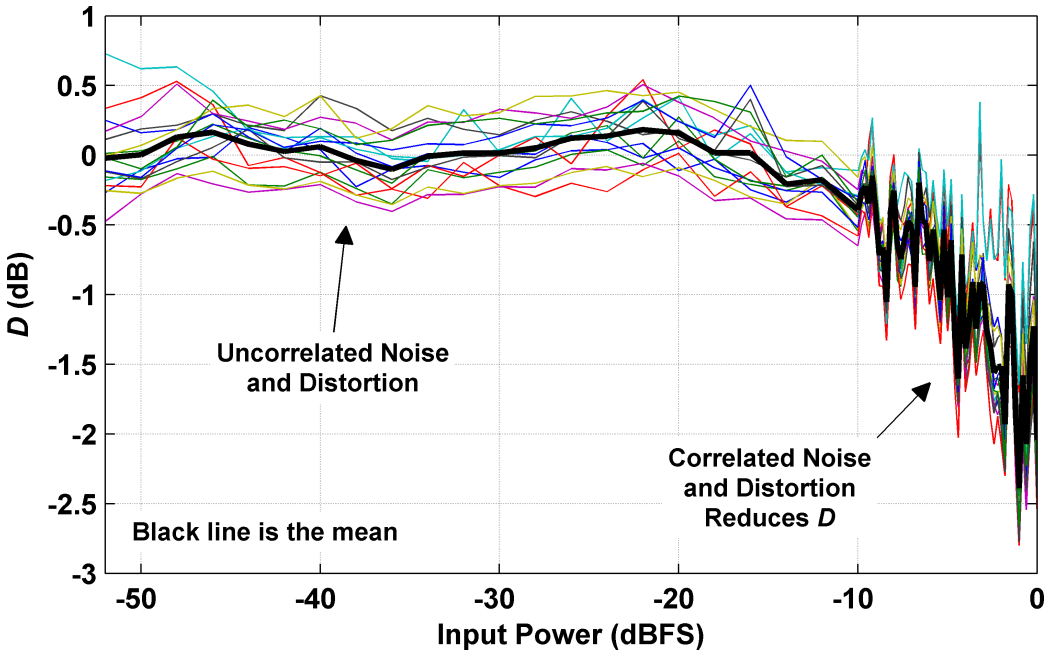

Figure 5.3: Plot of D for many different input powers. Below -10 dBFS, the noise and distortion is uncorrelated and $I \approx 0$ dB. Above -10 dBFS, the noise and distortion is partially correlated with D decreasing to a minimum values of about -2.7 dBFS.

noise and distortion sources are a partially correlated. In the rest of this chapter, I will further discuss the correlation of sampling noise and attempts to decorrelate it. Further, in the next chapter, I will discuss the correlation of harmonics.

5.2 Correlation of Sampling Noise

For many single channel systems, sampling noise (from clock or aperture jitter) does not the limit the SNR [65, 66, 67, 68]; however, improvements in ADCs and the drive towards higher intermediate frequencies (IF) in RF applications increases the impact of sampling noise [69]. Many modern ADCs have 3 dB bandwidths much greater than their sampling rate enabling higher IF frequencies; for instance, the Linear Technology LTC2208 used in these experiments has a 3 dB bandwidth of 700 MHz and a maximum sampling rate of 130 MHz [45]. Fig. 5.4 shows the maximum SNR of parallel ADC arrays with 1, 4, 8, and 16 channels as a function of IF frequency. In this calculation, the uncorrelated thermal noise-limited SNR of each individual ADC is taken as 78 dB, the correlated root-mean-square (RMS) clock jitter σ_μ is 60 fs, and the uncorrelated RMS aperture jitter σ_m is 85 fs [45]; all three values are near the state of the art for their frequencies. The SNR contribution as a function of frequency is [70]

$$\mathrm{SNR} = M \cdot \mathrm{SNR}_{\mathrm{thermal}} + \frac{M}{(\omega\sigma_m)^2} + \frac{1}{(\omega\sigma_\mu)^2}. \tag{5.1}$$

For a single channel, the SNR is thermal limited below about 100 MHz, while at higher frequencies the correlated sampling severely limits the maximum SNR. The onset frequency of clock-induced SNR degradation decreases for lower per-

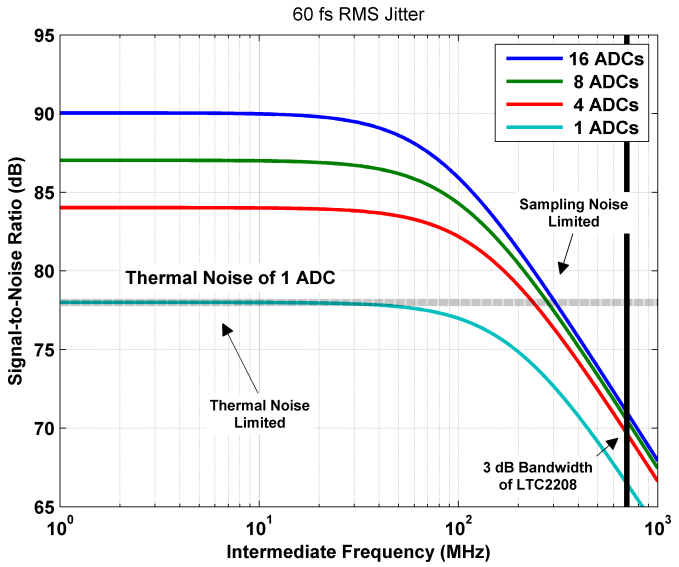

Figure 5.4: Maximum SNR of parallel ADC arrays as a function of IF frequency. The SNR (excluding sampling noise) of a single ADC is 78 dB and the RMS clock jitter is 60 fs; both values are near the state of the art. The impact of sampling noise on a single channel is low for IFs below 100 MHz; however, as the number of channels increases the SNR limitation due to correlated sampling noise becomes very significant. The 700 MHz 3 dB bandwidth of the LTC2208 is also marked.

formance clocks and high numbers of ADC channels. Dedicated state-of-the-art crystal oscillators, which can cost over a thousand dollars are required to achieve the 60 fs jitter assumed here [1], hence any techniques which would enable improved system SNR with lower performance clocks are desirable. Fig. 5.5 shows the impact of a 200 fs RMS jitter source. For a single channel, the impact is small; however any multi-channel system is severely limited for IFs $>$ 30 MHz.

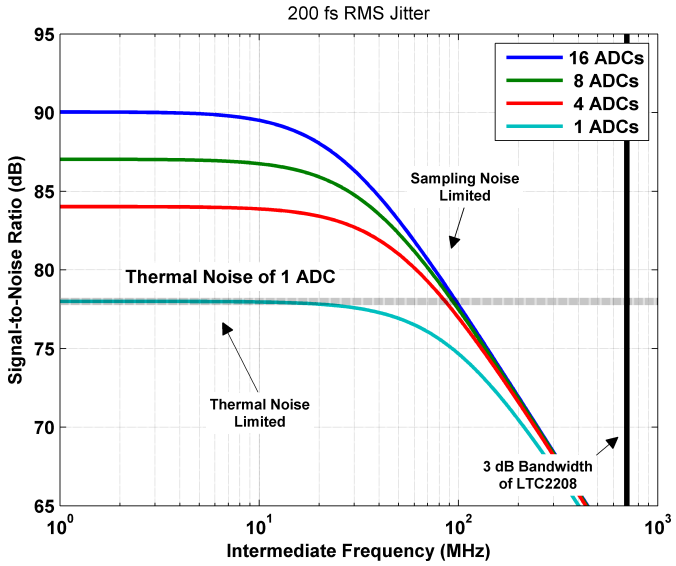

Figure 5.5: Maximum SNR of parallel ADC arrays as a function of IF frequency. The SNR (excluding sampling noise) of a single ADC is 78 dB and the RMS clock jitter is 200 fs; the RMS clock jitter is common for PLL clock sources [1]. The impact of sampling noise on a single channel is significant for IFs above 50 MHz.

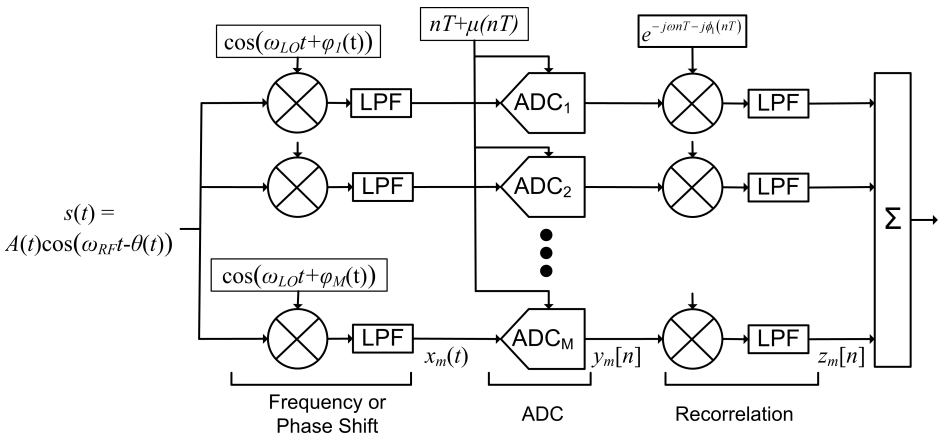

Figure 5.6: Downconversion block diagram with phase and frequency decorrelation.

5.3 Sampling Noise Model

The clock jitter noise model I present here is based on several previous derivations [70, 71, 72]. The sampling clock period is T and the clock jitter is $\mu(nT)$ on the nth sample. The input signal to the ADC $x(t)$ is sampled at time $nT+\mu(nT)$ yielding an output $y[n]=x(nT+\mu(nT))$. I approximate this output as

$$y[n]=x(nT+\mu(nT))\approx x(nT)+\mu(nT)x'(nT) \tag{5.2}$$

where $x'(nT)$ is the sampled time derivative of the input signal $x(t)$.

5.4 Impact of Phase and Frequency Shifts on Sampling Noise

As Fig. 5.6 shows, consider an initial modulated radio frequency (RF) input signal to an array of M ADCs

$$s(t)=A(t)\cos(\omega_{RF}t-\theta(t)) \tag{5.3}$$

where $A(t)$ and $\theta(t)$ are the amplitude and phase modulation. The RF input signal mixes with a phase or frequency shifted local oscillator, $\cos(\omega_{LO}t + \phi_m(t))$, and the output is lowpass filtered. Ignoring conversion loss, the downconverted intermediate frequency (IF) signal in each channel is

$$x_m(t) = A(t)\cos\big(\omega t + \theta(t) + \phi_m(t)\big) \tag{5.4}$$

where $\omega_{LO} - \omega_{RF} = \omega$. The ADC then samples the intermediate frequency signal with a jittery clock and the digital output is

$$\begin{aligned} y_m[n] = & A(nT)\cos\big(\omega nT + \theta(nT) + \phi_m(nT)\big) \\ & -\mu(nT)\omega A(nT)\sin\big(\omega nT + \theta(nT) + \phi_m(nT)\big) \end{aligned} \tag{5.5}$$

where it was assumed that $A'(t)$, $\theta'(t)$, and $\phi'_m(t)$ are small compared to $\omega A(t)$. The second term in (5.5) is the sampling noise of the IF signal.

Finally, I digitally multiply the sampled output $y_m[n]$ by $e^{-j\omega nT - j\phi_m(nT)}$ to frequency shift the signal to baseband and remove the excess phase. The final baseband signal $z_m[n]$ is composed of the desired baseband signal and the baseband sampling noise $z_m[n] = z_{sig}[n] + \varepsilon_m[n]$. The desired baseband signal, after lowpass filtering, is

$$z_{sig}[n] = A(nT)e^{j\theta(nT)} \tag{5.6}$$

where I again ignore conversion loss. I can downconvert simply using Euler's identity because $A(t)$ and $\theta(t)$ are narrowband relative to the Nyquist bandwidth.

Conversely, the clock jitter bandwidth considered here is wider than the Nyquist bandwidth, so Euler's Identity cannot be used without accounting for

both the positive and negative frequencies and their aliases. The sampling noise after downconversion, but before filtering, is

$$\begin{aligned}\varepsilon_m[n] = &-\mu(nT)A(nT)\omega e^{-j\omega nT - j\phi_m(nT)} \\ &\times \sin(\omega nT + \theta(nT) + \phi_m(nT)).\end{aligned} \tag{5.7}$$

I will ignore the filter when calculating the correlation between channels since there is no frequency dependence in the correlation coefficient assuming $\mu(nT)$ is white and wideband and taking into account both positive and negative frequencies and aliasing.

5.4.1 Determining the Correlation Coefficient

The total sampling noise is the sum of the correlation coefficient matrix times the sampling noise in a single channel

$$\begin{aligned}\mathrm{E}\left[\left(\sum_{m=1}^{M}\varepsilon_m\right)^2\right] &= \sum_{k=1}^{M}\sum_{l=1}^{M}\mathrm{E}\left[\varepsilon_k\varepsilon_l^*\right] \\ &= \sigma_\varepsilon^2\sum_{k=1}^{M}\sum_{l=1}^{M}\rho_{k,l}\end{aligned} \tag{5.8}$$

where $\mathrm{E}[x]$ is the expectation of x, $\sigma_\varepsilon^2 = \mathrm{E}[\varepsilon_m\varepsilon_m^*]$ for all m, and the correlation coefficient is

$$\rho_{k,l} = \frac{\mathrm{E}[\varepsilon_k\varepsilon_l^*]}{\sqrt{\mathrm{E}[\varepsilon_k\varepsilon_k^*]\,\mathrm{E}[\varepsilon_l\varepsilon_l^*]}} = \rho_{l,k}^*. \tag{5.9}$$

The correlation coefficient matrix is Hermitian and, therefore, the imaginary parts cancel in the summation, so I only need to consider the real part of the correlation coefficient matrix

$$\hat{\rho}_{k,l} = \Re(\rho_{k,l}) = \frac{\Re(\mathrm{E}[\varepsilon_k\varepsilon_l^*])}{\sqrt{\mathrm{E}[\varepsilon_k\varepsilon_k^*]\,\mathrm{E}[\varepsilon_l\varepsilon_l^*]}}. \tag{5.10}$$

Therefore, only the real part of the correlation coefficient $\hat{\rho}_{k,l}$ is considered throughout the rest of this paper.

For any channels k and l, the expected value of the sampling noise product is

$$\begin{aligned}\mathrm{E}[\varepsilon_k[n]\varepsilon_l[n]^*] = &-(1/2)\,\mathrm{E}\left[\mu(nT)^2 A(nT)^2 \omega^2\right] \\ &\times \mathrm{E}\left[\cos(\Delta\phi_{kl}(nT))e^{-j\Delta\phi_{kl}(nT)}\right].\end{aligned} \tag{5.11}$$

where $\Delta\phi_{kl}(nT) = \phi_k(nT) - \phi_l(nT)$ and, therefore, the real correlation coefficient is

$$\begin{aligned}\hat{\rho}_{k,l} &= \mathrm{E}\left[\frac{e^{j\Delta\phi_{kl}(nT)} + e^{-j\Delta\phi_{kl}(nT)}}{2}\cos(\Delta\phi_{kl}(nT))\right] \\ &= \mathrm{E}\left[\cos^2(\Delta\phi_{kl}(nT))\right]\end{aligned} \tag{5.12}$$

5.4.2 Constant Phase Offsets

For a constant phase offset, $\phi_m(nT) = \phi_m$, the real part of the correlation coefficient is

$$\hat{\rho}_{k,l} = \cos^2(\Delta\phi_{kl}). \tag{5.13}$$

The sampling noise between two channels is fully correlated ($\rho_{kl} = 1$) when $\Delta\phi_{kl} = 0, \pi, \ldots$ and uncorrelated ($\rho_{kl} = 0$) when $\Delta\phi_{kl} = \pi/2, 3\pi/2, \ldots$. It is possible to reduce the sampling noise correlation between any two channels to zero by placing them in quadrature, which reduces the total sampling noise by 3 dB compared to the fully correlated case. However, if a third ADC is added with its phase $\pi/2$ offset from ADC 1 (or 2), then the newly added ADC is fully correlated with ADC 2 (or 1) and the total sampling noise reduction is less than 3 dB.

To achieve a maximum reduction in total sampling noise of 3 dB, the phase should be either randomly or deterministically distributed around the unit circle, or half the channels should be placed in quadrature with the other half of the channels.

5.4.3 Frequency Offsets

For a linearly time varying phase offset, $\phi_m(nT) = \omega_m t$, the real part of the correlation coefficient is always

$$\hat{\rho}_{k,l} = \mathrm{E}[\cos^2(\omega_k t - \omega_l t)] = \begin{cases} 1/2 & \text{if } k \neq l \\ 1 & \text{if } k = l \end{cases} \tag{5.14}$$

regardless of the frequency chosen. The sampling noise is always partially correlated and cannot be fully decorrelated; however, no particular care needs to be taken to ensure partial correlation using frequency offsets. Frequency offsets reduce the total sampling by 3 dB for a large array.

5.5 Measurements of Sampling Noise Correlation

I verified the theoretical correlation coefficient by measuring the sampling noise correlation across a set of eight of the 16 ADCs described in Chapter 3, as shown in the block diagram of Fig. 5.7.

An Agilent E8267D signal generator produced the 120 MHz ADC clock signal, which was subsequently divided by a microwave power splitter yielding a clock power at the ADC of about 12 dBm. The pulse generator, 800 MHz DDS

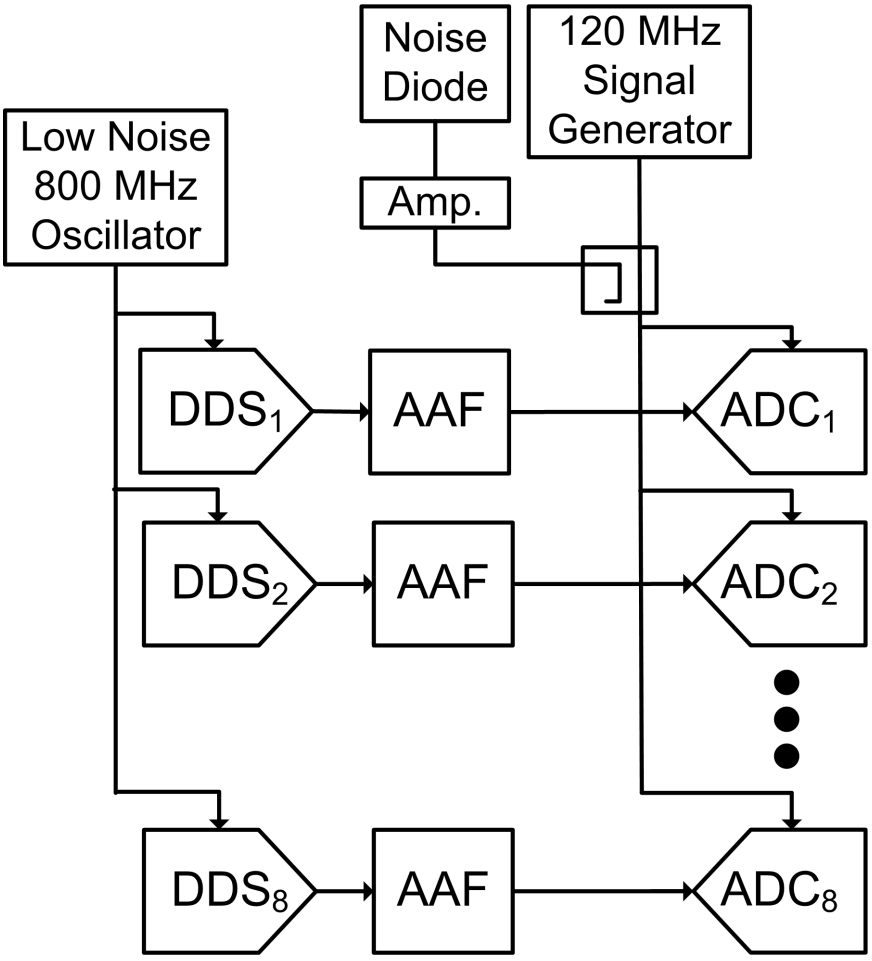

Figure 5.7: Block diagram of sampling noise measurement using 8 ADCs and DDSs. The measured phase noise of the 120 MHz signal generator and noise diode was -123 dBc/Hz at 1 MHz, Ill above the internal noise of the ADC (-157 dBc/Hz) and the DDS (-150 dBc/Hz at 1 MHz).

clock, and signal generator Ire all phase-locked to a common 10 MHz source. The phase noise of the signal generator was about -150 dBc/Hz) at the 1 MHz corner frequency (about 1 ps jitter in 200 MHz bandwidth [1]), as measured using the phase noise measurement setting of an Agilent spectrum analyzer. This phase noise level was comparable to the white ADC noise of -157 dBc/Hz at ADC full scale and to the DDS phase noise of about -150 dBc/Hz at 1 MHz offset. The common signal generator clock jitter was large enough to yield a noise correlation coefficient of about 0.7 between all channels; the total measured noise—sampling, ADC thermal, and DDS source noise—was largely correlated across channels due to the influence of the common sampling noise.

To better illustrate the impact of decorrelation techniques on sampling noise, I ensured that the clock jitter dominated our noise measurements by applying an amplified noise diode through a directional coupler to the clock signal before splitting. This raised the ADC clock's measured phase noise to about -123 dBc/Hz, ensuring that all measured noise was from sampling noise, as verified in Section 5.5.2.

I eliminated phase and amplitude differences between channels by using a closed loop calibration procedure to equalize each DDS source signal. The DDSs Ire set to generate the same IF ($\approx$90 MHz) with an initial unknown phase and an arbitrary amplitude below full scale. The ADCs measured the absolute amplitude using a fast Fourier transform (FFT) with a flat-top window. The DDS amplitudes Ire then adjusted until all signals measured about -0.1 dBFS, resulting in an amplitude variation across all channels of less than 0.1 dB. The ADCs then

measured the phase using an FFT and each DDS phase was adjusted to match the reference channel, resulting in a phase match of about 1 mrad. This calibration procedure yielded phase and amplitude alignment tighter than achievable with a typical microwave power splitter.

5.5.1 Measurement Approach

To measure the real part of the correlation coefficient, I applied

$$\mathrm{E}[|(\varepsilon_k+\varepsilon_l)|^2] = \mathrm{E}[|\varepsilon_k|^2]+\mathrm{E}[|\varepsilon_l|^2]+2\Re(\mathrm{E}[\varepsilon_k\varepsilon_l^*]) \tag{5.15}$$

to (5.10), so the the real part of the correlation coefficient becomes

$$\hat{\rho}_{k,l} = \frac{\mathrm{E}[|(\varepsilon_k+\varepsilon_l)|^2]-\mathrm{E}[|\varepsilon_k|^2]-\mathrm{E}[|\varepsilon_l|^2]}{2\sqrt{\mathrm{E}[\varepsilon_k\varepsilon_k^*]\,\mathrm{E}[\varepsilon_l\varepsilon_l^*]}} \tag{5.16}$$

Therefore, I can calculate the correlation coefficient by measuring three noise powers, that of channel k, channel l, and the sum of channels k and l. This technique measures only the real part of the correlation coefficient.

The sampling noise power is proportional to the input power, so all measurements Ire made with input powers of about -1 dBFS to maximize the noise. To measure the noise correlation coefficient, I applied a single tone with a frequency near 98 MHz to the ADCs and captured a sequence of 32768 samples. I then measured the noise power over a particular bandwidth away from the signal, for instance 85 to 95 MHz, by applying an FFT to the sequence and summing the magnitude squared of the FFT bins. In this way, I measured $\mathrm{E}[|\varepsilon_k|^2]$ and $\mathrm{E}[|\varepsilon_l|^2]$ from (5.16). To find the remaining term, $\mathrm{E}[|(\varepsilon_k+\varepsilon_l)|^2]$, I added the two voltage

sequences, applied an FFT, and summed the magnitude squared over the same set of FFT bins. Since the correlation coefficient is a ratio, the actual bandwidths over which the measurements are made are irrelevant, so long as there are a sufficient number of samples and the bandwidths are equal.

5.5.2 Verifying Sampling Noise

To confirm that the measured noise was actually sampling noise and not ADC or DDS noise, I first modified the configuration shown in Fig. 5.7 to include two independent noise diodes (one on ADCs 1-4 and one on ADCs 5-8) coupled to the same signal generator. Fig. 5.8a shows the -0.8 dBFS signal with the sampling noise in the frequency domain, and Fig. 5.8b shows the noise over a 100 kHz bandwidth offset from the signal by 15 MHz. As described earlier, channel to channel phase and amplitude differences Ire calibrated out in the analog domain prior to measurement. Clearly from Fig. 5.8b, the noise of channels 1-4 and 5-8 match each other within a set and appear independent between sets, indicating correlation due to clock noise. The sampling noise power on ADCs 5-8 is about 3 dB lower than on ADCs 1-4 due to the different diode noise powers, and helping to distinguish between the two sets. All of the correlation coefficients between channels with a common clock (ADCs 1-4 and 5-8) Ire greater than 0.999 and the magnitude of all of the correlation coefficients between channels with different noises Ire less than 0.03. From our experience, signals with correlation coefficients less than 0.03 are within our measurement error bounds and can be

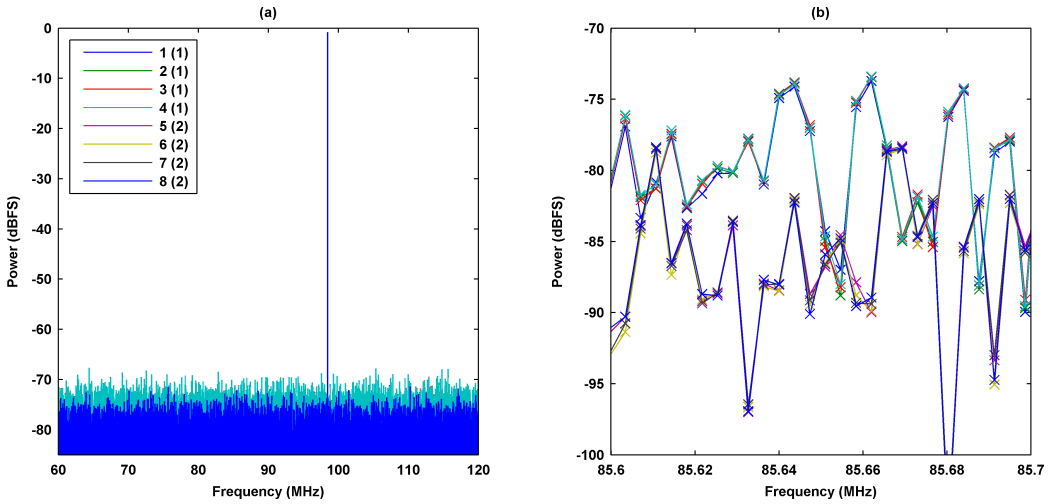

Figure 5.8: (a) Plot of the generated signal in the frequency domain. The relatively high noise floors are due to the imposed sampling noise. (b) Frequency domain plot of the noise of each channel over a 100 kHz bandwidth offset 15 MHz from the signal. There is strong correlation within each set of ADCs 1-4 and 5-8, and no correlation between sets with different diodes. DDS and ADC noise was much lower at about -101 dBFS per FFT bin from prior measurements.

considered independent, leading us to conclude that the noise present in our experimental configuration arise primarily from clock-induced sampling noise, not independent thermal noise.

5.5.3 Constant Phase Offsets

To experimentally assess the impact of our decorrelation techniques on sampling noise, I reverted to the single amplified noise diode configuration shown in Fig. 5.7, where a single noisy clock is common to all 8 ADCs. I phase and amplitude aligned the signals using the close-loop calibration procedure described

earlier. I then purposely adjusted the phase of DDSs 5-8 by $\Delta\phi_{kl}$ (the phase shift was the same on all four channels) and measured the correlation coefficient of the sampling noise between all pairs of channels (64 total) using (5.16). Fig. 5.9 plots the average measured correlation coefficient $\bar{\rho}$ between all phase offset channels for many phase offsets from 0 to 2π. Here, $\bar{\rho}$ is calculated by

$$\bar{\rho} = \frac{\sum_{m=1}^{4}\sum_{l=5}^{8}\hat{\rho}_{ml}}{4^2}. \tag{5.17}$$

The average measured two-channel correlation coefficient clearly follows the squared-cosine relationship predicted by (5.13), and complete decorrelation ($\hat{\rho}_{k,l} \approx 0$) was achieved for channels with a $\pi/2$ phase offset.

The maximum decorrelation between two channels occurs when the phase difference is $\pi/2$ between channels. When a third channel is added with a $\pi/2$ phase offset to channel 2, it is then offset from channel 1 by π and the sampling noise is again fully correlated $\rho = 1$. It is not possible to reduce the the average correlation coefficient $\bar{\rho}$ when $k \neq l$ below $1/2$. For systems with more than two channels, a distributed channel-dependent phase variation must be applied in order to achieve the maximum decorrelation. If the phase of M channels is either randomly or deterministically distributed from 0 to 2π, the average correlation coefficient $\bar{\rho}$ when $k \neq l$ may be reduced from 1 to $1/2$. This reduces the total sampling noise by 3 dB for large arrays.

I confirmed this result experimentally by uniformly distributing the phase of the signals from 0 to 2π (the phases Ire 0, $\pi/4$, $\pi/2$, $3\pi/4$, π, $5\pi/4$, $3\pi/2$, and $7\pi/4$) and measuring the correlation coefficient between all pairs of chan-

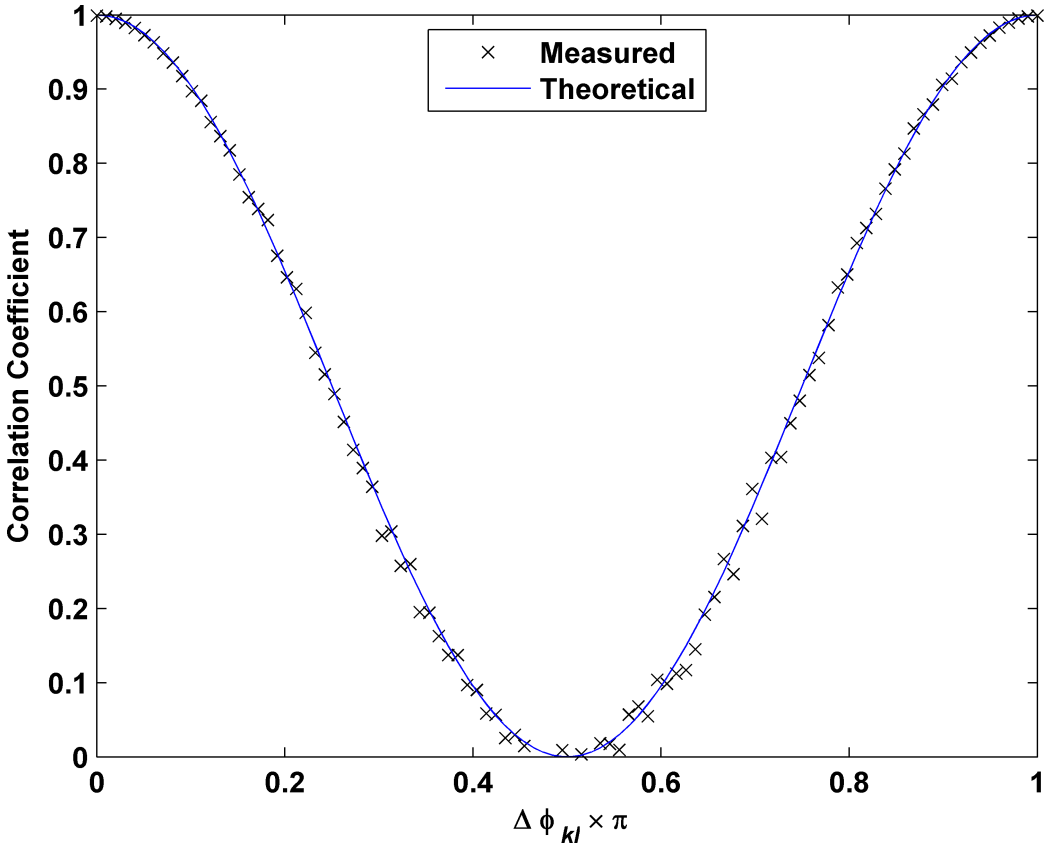

Figure 5.9: The measured correlation coefficient for phase shifted signals matches the prediction from (5.13).

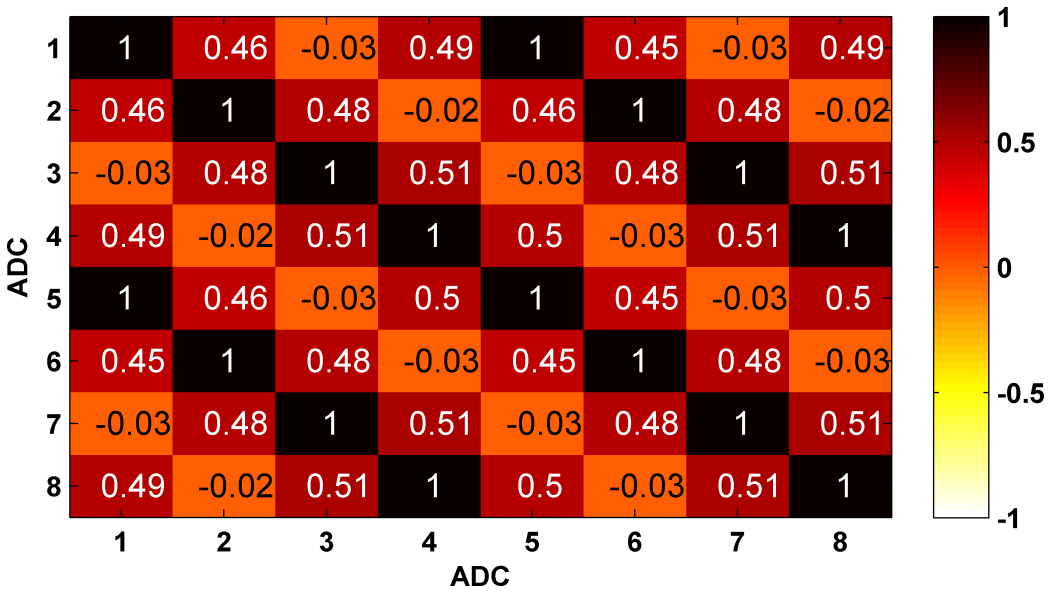

Figure 5.10: Color map of the measured correlation coefficient matrix between channels with phase uniformly distributed among all 8 channels between 0 and 2π.

nels. Fig. 5.10 shows the resulting phase correlation coefficient matrix as a color map. The sum of the sampling noise from all 8 channels is 3.14 dB below fully correlated noise, which matches the expected reduction of 3 dB.

Fig. 5.11a shows the fully correlated spectrum and the phase-decorrelated measured spectrum with the uniform phase distribution from 0 to 2π (both spectra were calculated from the same measurement). The fully correlated spectrum was calculated by adding the magnitude of the spectrum of each channel together. The phase-decorrelated combined spectrum was calculated by adding the 8 channels in the time domain then transforming to the frequency domain. The phase-decorrelated spectrum is always less than or equal to the fully correlated spectrum in every frequency bin.

Measurements with random phases produced similar results. In addition, I

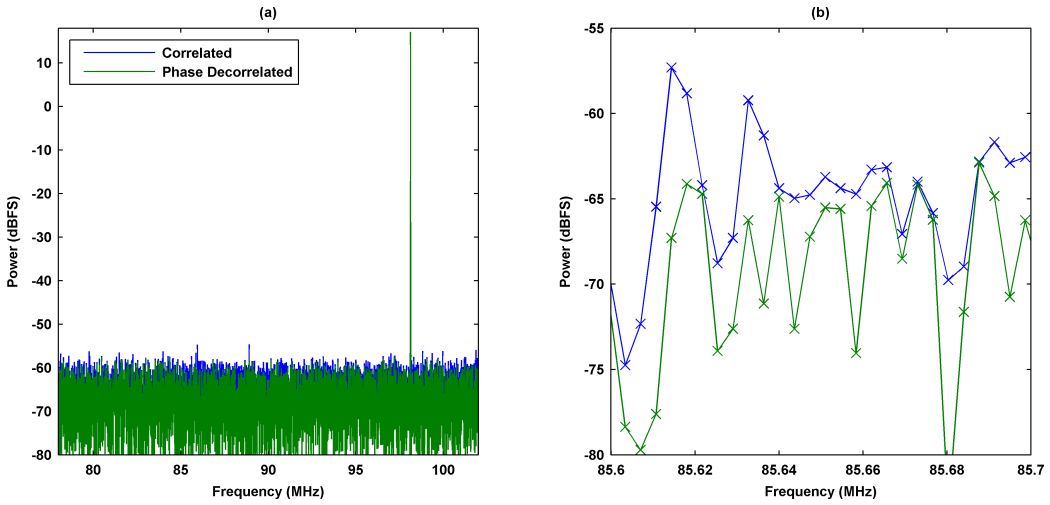

Figure 5.11: (a) The fully correlated and phase-decorrelated measured spectra for a uniform phase distribution from 0 to 2π over a 24 MHz bandwidth. Scale relative to the full scale of a single channel. (b) Close up of noise in 100 kHz bandwidth offset from the signal by 13 MHz. I calculated the correlated spectrum by summing the magnitude of each channel's spectrum. The phase-decorrelated noise is 3 dB below the correlated output due to the phase shifts; the actual spectrum is always less than or equal to the correlated spectrum.

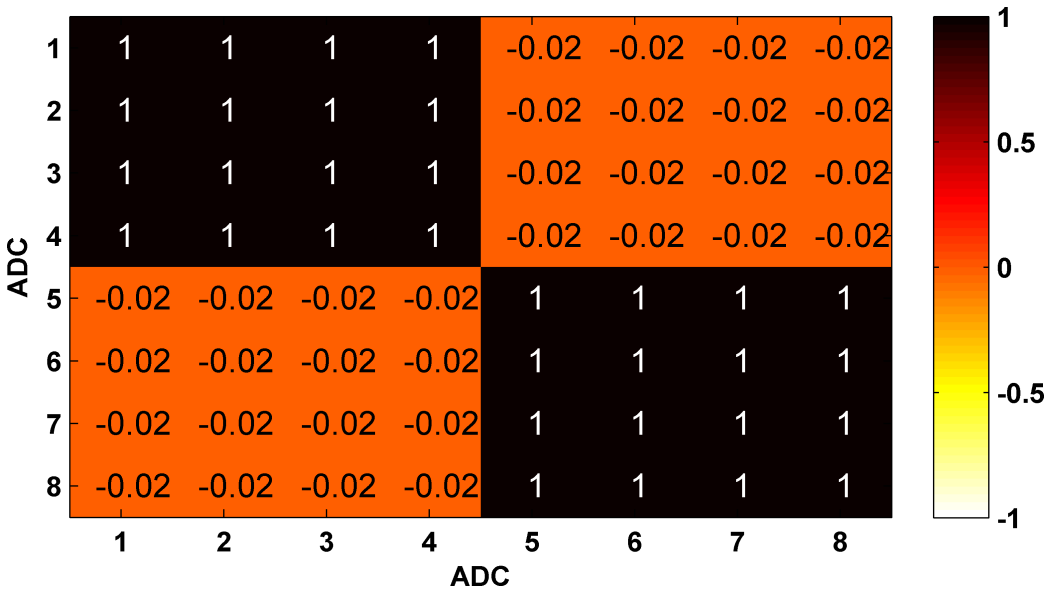

Figure 5.12: Color map of the measured correlation coefficient matrix when channels 1-4 are set in phase with each other but in quadrature with channels 5-8.

achieved the same result when the signals were in quadrature (the phases were 0, 0, 0, 0, $\pi/2$, $\pi/2$, $\pi/2$, and $\pi/2$), as shown in Fig. 5.12 The correlation coefficient between channels in quadrature is about zero and the total sampling noise is 2.43 dB below fully correlated noise.

5.5.4 Frequency Offsets

I measured the correlation coefficient of 8 ADCs where the input signal frequencies were separated by 1.8 kHz. Fig. 5.13 shows the 8 frequency shifted signals before downconversion and recorrelation. The spacing was chosen to be one bin width apart in the FFT to make the signals as similar as possible. Fig. 5.14 shows that the correlation coefficient between channels ranges from 0.42 to 0.50, confirming the coefficient of 0.5 predicted by (5.14). The total sampling noise is

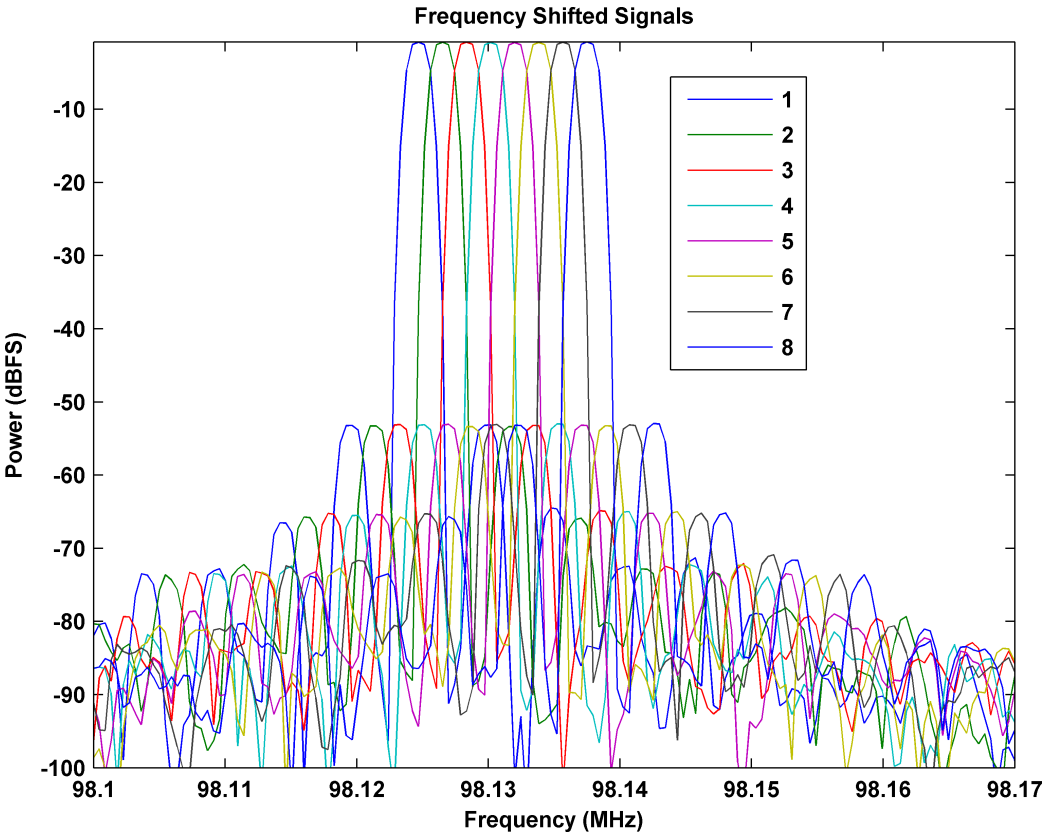

Figure 5.13: Input signals of 8 ADCs shifted 1.8 kHz before downconversion and recorrelation.

2.76 dB below full correlation, matching the expected 3 dB decrease. The same decrease is expected for any set of frequency separations, as the correlation coefficient of (5.14) is frequency-independent; this was verified with a second set of measurements with a frequency separation of 18 kHz (data not shown). Furthermore, the frequency separation need not be uniform, and randomly distributed frequency offsets are expected to have the same effect.

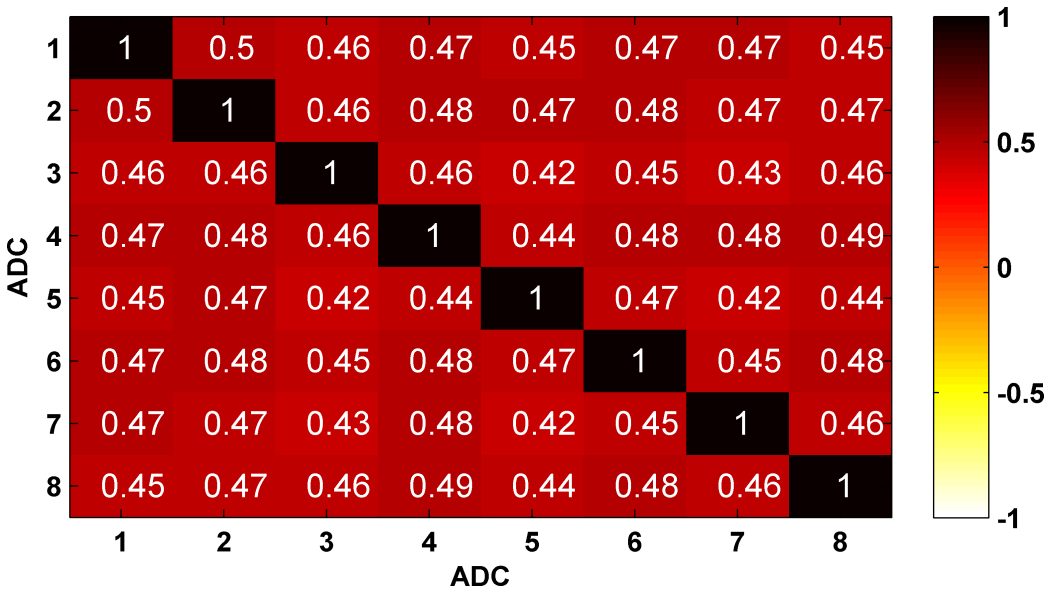

Figure 5.14: Measured correlation coefficient matrix is about 0.5 for all channels when input frequencies are offset by 1.8 kHz.

5.6 Summary and Conclusion of Chapter

I have experimentally demonstrated that thermal noise is uncorrelated from channel to channel, as expected.

I have shown theoretically and experimentally that applying phase and frequency offsets prior to digitization can reduce the correlation of sampling noise in a parallel ADC array with a common clock source. Specifically, by adjusting the frequency of each channel, by randomly or deterministically distributing the phase offset from 0 to 2π, or by placing half the channels in quadrature, I decrease the total sampling noise by about 3 dB. The 3 dB decrease in total sampling noise achieved in our work represents the maximum decrease possible using phase and frequency offsets as neither approach allows for negative correlation

coefficients, which would be required to cancel the noise further. I are not aware of any technique that enables negative correlation coefficients between sampling noise, I believe the phase and frequency offset approaches to be among the most effective methods of reducing the correlated sampling noise in fixed ADC arrays. As these techniques require mixers, they are most useful in RF applications. The phase offsets may even occur naturally in phased-array antenna.

Previously, frequency and phase offsets have been shown to effectively decorrelate mixer spurs and harmonic distortion, and our results show an additional benefit of these techniques. Fig. 5.4 showed that maximum SNR becomes severely limited by sampling noise for large arrays and high IFs, even with very low jitter clocks. Due to the cost of low jitter sources and the drive to higher IFs, a reduction of 3 dB is significant and welcome in many applications. Further performance improvement would require improved clock sources [50, 78, 79] or the use of independent clocks on each ADC or adequately small group of ADCs raising costs.

Chapter 6

Correlation of Harmonics

Unfortunately, real ADCs generate not only noise, but also spurious harmonics which may limit the dynamic range and degrade system performance. The undesired harmonics may alias into the passband of the signal. The extent of spurious harmonic generation by an ADC is characterized by the SFDR, which is the ratio of the maximum signal to the largest harmonic, while the SNR is the ratio of the signal to the integrated noise power. Generally, a SFDR greater than the SNR within a given bandwidth is desirable.

In this chapter, I use modeling and measurement to determine the potential inherent channel-to-channel correlation of harmonics in parallel ADC systems. All measurements were made on a specially designed 16-channel experimental test bed described in Chapter 3. In Section 6.1, I discuss the origins of ADC harmonics and present measurements of the inherent harmonic correlation of the ADC array. These measurements clearly establish the need for decorrelation techniques, if any significant increase in system SFDR is desired from parallelization. I also develop a set of metrics to evaluate the effectiveness of the decorrelation techniques. Finally, in Sections 6.3 and 6.4, I describe and experimentally demonstrate four phase and frequency decorrelation approaches, two of which are proposed here for the first time, and I add significant experimental results for the

other two. The phase decorrelation techniques of Section 6.3 yield an increase in system SFDR of a factor M or more, while the frequency decorrelation techniques of Section 6.4 increase system SFDR by a factor of M^2 over the correlated system. Though certain approaches may yield greater gains in SFDR, due to the varying complexity of implementations, the best choice of decorrelation technique for a given application will depend upon the required SFDR and system complexity.

6.1 Origin of ADC Harmonics

While some research has been performed on techniques to decorrelate ADC harmonics [20, 21, 18, 19], as far as I know no one has shown to what level harmonics in ADC arrays are inherently correlated. This is important, since any decorrelation technique deemed necessary increase the complexity of a parallel ADC array and should only be implemented if truly needed.

The primary mechanisms of ADC harmonic generation are related to sampling and quantization. Fig. 6.1 shows a simple block diagram of an ADC composed of a sampler (or sample and hold) and a quantizer. The sampler generates harmonics due to the finite time constant of the sampling capacitor and the finite fall time of the sampling clock. The quantizer generates harmonics due to errors in its transfer function, and, even for an ideal transfer function, the quantization noise is harmonically related to the signal [80].

Depending on the ADC architecture, sampler distortion may be more or less significant than quantizer distortion. At the signal frequencies I measured,

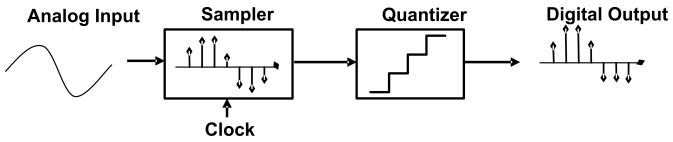

Figure 6.1: Simple block diagram of an ADC composed of a sampler and quantizer.

quantizer nonlinearities tend to dominate with our ADCs, but that should not be regarded as a general result.

In this section, I describe both sources of harmonic generation in isolation and determine the amplitude and phase relationship between the input signal and its harmonics. Using mathematical models and methods from the literature, I consider distortions arising from sampling and quantization mechanisms, verify these models, and predict the inherent harmonic correlation across ADCs in any array. I then evaluate these predictions and the inherent correlation of both sources of harmonics simultaneously at a particular input signal frequency, through measurements in our test bed.

6.1.1 Harmonics from the Sampler

To describe sampling-generated harmonics, I utilize a model from the literature to understand the characteristics of sampler distortion and then compare those characteristics with measurements to determine their applicability to our ADC [86]. This understanding of the distortion characteristics can then be used to predict the correlation of sampler harmonics.

Yu *et al.* analyzed the distortion of a simple metal-oxide-semiconductor field-effect transistor (MOSFET) sampler composed of only a single MOSFET

and sampling capacitor [86]. Similar analysis was also performed on a classic diode bridge sampler [74]. Yu *et al.* identified three sources of distortion depending on the clock fall time relative to the signal rise time or its frequency. *Continuous-time distortion* occurs due to the voltage dependent "on" resistance of the MOSFET switch. Continuous-time distortion dominates when the clock fall time is short enough that the clock is practically ideal. *Time-varying distortion* occurs when the clock fall time is longer, such that the changing voltage of the clock V_g also modulates the voltage-dependent "on" resistance of the switch. *Sampling distortion* occurs when the fall time is greater still, such that the actual time that the switch closes (when the signal is sampled) depends on the input signal. Yu *et al.* highlight that their model ignores high-order transistor effects such as the *body effect* and bias-dependent junction capacitance; however, their analytical model compares very well with SPICE simulations.

6.1.1.1 Amplitude and Phase of Sampler Harmonics

The Yu model overestimates the harmonic amplitudes because it does not take into account differential sampling and other linearization techniques [1, 89, 90]. For continuous-time distortion, the Yu model-predicted second and third harmonic coefficients are

$$a_2(A) = \frac{A}{2} \cdot \frac{j\omega C}{K(V_g - V_t)^2}$$

and

$$a_3(A) = \left(\frac{A}{2}\right)^2 \cdot \frac{j\omega C}{K(V_g - V_t)^3}$$

where K and V_t are MOSFET parameters, V_g is the clock voltage, C is sampling capacitor's capacitance, and A and ω are the input amplitude and frequency. For sampling distortion, the predicted harmonic coefficients are

$$a_2(A) = \frac{A}{4} \cdot \left(\frac{j\omega T_f}{V_g} \right)$$

and

$$a_3(A) = \frac{3A^2}{32} \cdot \left(\frac{\omega T_f}{V_g} \right)^2$$

where T_f is the fall time of the clock. No closed form solutions of the harmonic coefficients due to time-varying distortion are available; however, this is acceptable because continuous-time distortion and sampling distortion cover both limits of clock fall time and input signal frequency.

Yu *et al.* did not calculate higher order harmonic coefficients as these will increasingly be impacted by considerations like the body effect and the exact circuit models. Despite this, assuming the pattern established by the second and third harmonics holds generally true, several basic trends emerge: 1) both continuous-time and sampling distortion harmonic powers $|a_{km}|^2$ are proportional to $(A^2)^{k-1}$; 2) continuous-time distortion harmonic power is proportional to ω^2 while sampler distortion harmonic power is proportional to $\omega^{2(k-1)}$; 3) the harmonic phase is proportional to the input phase ϕ_m plus an offset ϕ_{km} that depends on the source of distortion:

$$\angle a_{km} = k\phi_m + \phi_{km} \tag{6.1}$$

The phase offset $\phi_{km} = \pi/2$ for continuous-time distortion and $\phi_{km} = (k-1)\pi/2$ for sampling distortion harmonics. It should be noted, though, that this is only a

simple analysis and higher-order effects may impact the harmonic phase.

6.1.1.2 Measured Sampler Distortion

Fig. 6.2 shows our measurement setup to investigate the sampler distortion. The measurement setup was composed of an Agilent E8267D signal generator, Mini-Circuits HELA-10B amplifier, filters to reduce source harmonics, and a single ADC. I chose this combination of signal source and amplifier to minimize the source harmonics. The second and third harmonic power from the signal generator and amplifier measured at the ADC full scale was ≤ -54 and ≤ -70 dBFS, respectively, for input signal frequencies from 80 to 250 MHz. Above 250 MHz, the second harmonic power increased to -35 dBFS and the third harmonic power to -65 dBFS. The harmonics were reduced using four filters, a bandpass filter from 78-102 MHz and three lowpass elliptical filters with cutoff frequencies of 150, 225, and 300 MHz. For all input frequency, I had a filter with at least 75 dB of attenuation at the second and higher harmonics, which I measured on a Hewlett Packard 8720C network analyzer. Therefore, the second harmonic was ≤ -120 from 80-250 MHz and ≤ -100 from 80-250 MHz, which was well below the measured harmonic power. The third harmonic power was at least 30 dB below these.

To measure the second through fifth harmonic power and phase, I applied the amplified and filtered tone to the input of each ADC—each ADC was measured separately—and adjusted the input power to -0.5 dBFS. I measured with

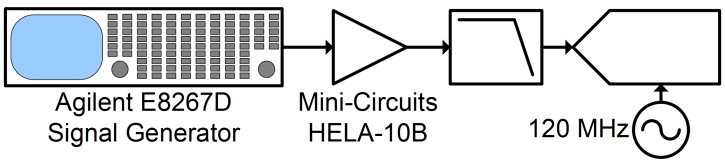

Figure 6.2: Measurement setup used to capture Fig. 6.3 composed of an Agilent E8267D signal generator, Mini-Circuits HELA-10B amplifier, lowpass filters, and a single ADC.

input signal frequencies from 80 to 300 MHz in 5 MHz intervals. The input signal was offset by 100 kHz and then adjusted so that the frequency was near the center of a frequency bin. I then captured the data, transformed the data to the frequency domain, and measured the phase offset ϕ_{km} and magnitude $|a_{km}|$.

Fig. 6.3 shows the measured values of ϕ_{km} and $|a_{km}|$ for $k = 2,3,4,5$. The power of the second, third, and fourth harmonics clearly increases with frequency as predicted from the analysis, indicating that they are sampler distortion limited. The fifth harmonic power does not increase with frequency, indicating that it is quantizer limited. The harmonic powers and trends are well matched across all channels.

The phase offset of the second and third harmonics trends toward $-\pi/2$ with increasing frequency from $-\pi$ for the second harmonic and π for the third. The fourth harmonic phase offset varies significantly with frequency, while the fifth harmonic varies from π toward 0. The harmonic phase offsets do not match the theory; however, the phase offsets match very closely from channel to channel.

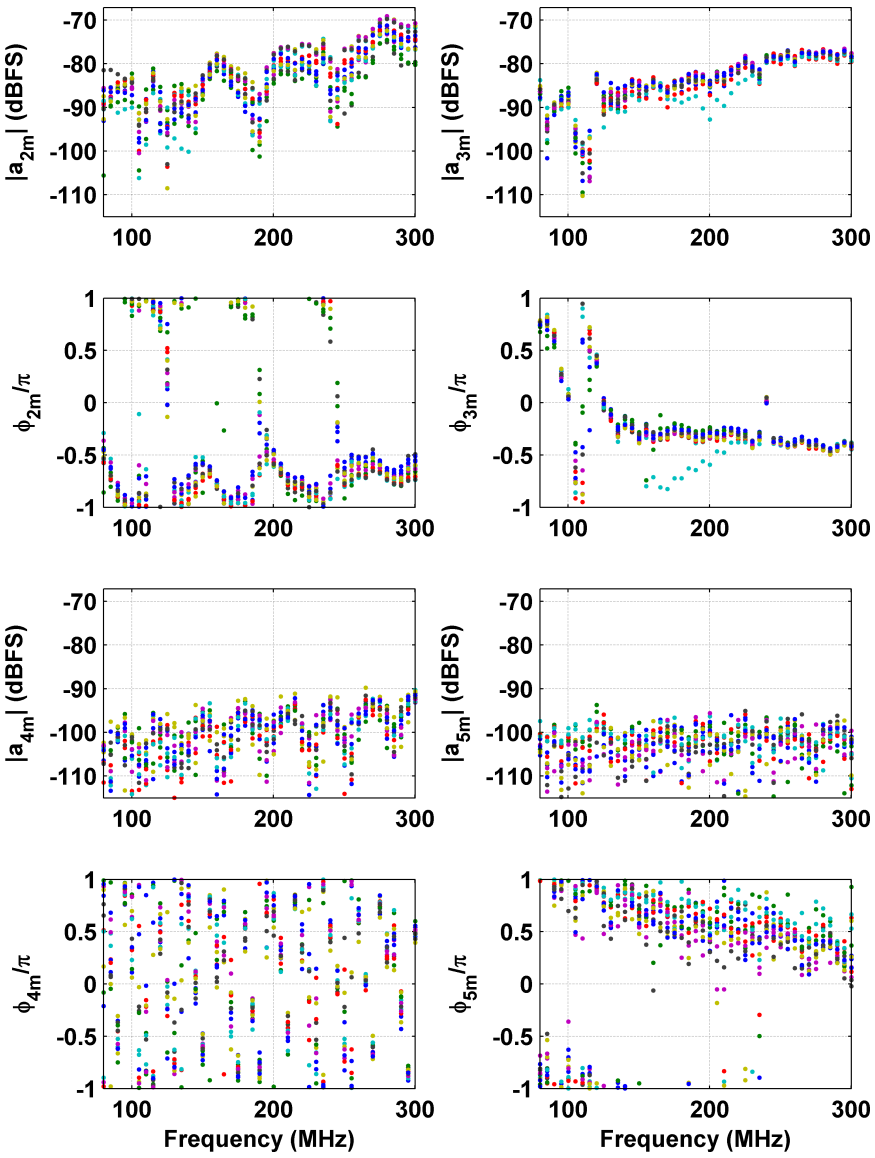

Figure 6.3: The second through fifth harmonic's magnitude and phase measured at different input frequencies near full scale of the ADCs. The second, third, and fourth harmonics all increase in power with frequency, although the second and fourth contain several troughs. The phase of the ADCs are largely consistent from channel to channel, suggesting strong correlation.

6.1.1.3 Predicted Sampler Harmonic Correlation

As discussed in Section 2.1.3, the phase matching between channels determines the correlation. Therefore, from the previous observation I expect the sampler distortion to be nearly fully correlated. The measured phase offset and power are well matched across channels, so that with common input signals, the harmonics should be correlated.

6.1.2 Harmonics from Quantizer

Quantization, even ideal quantization, generates harmonics of the input signal. The characteristics of harmonics arising from ideal quantization (more commonly called *quantization noise*) are well understood [40, 80]. The maximum harmonic from ideal quantization is $\leq$-9.03n dBFS (dB relative to ADC full scale) for an n-bit ADC [2]. The ADCs characterized in this paper have 16 bits, so the maximum harmonic due to ideal quantization is at most -144 dBFS. As I shall show, this is well below the measured harmonics and thermal noise by tens of dB. In addition, dithering effectively decorrelates ideal quantization noise [17], so I may disregard quantization noise as a significant source of harmonics.

Errors in the quantizer transfer function are a far more significant source of harmonics in ADCs than ideal quantization noise. To model the quantizer harmonics, I utilized a modeling method developed by Pan and Abidi [2]. In that method, they generated a digital signal and quantizer transfer function with errors. They applied the signal to the transfer function and measured the resulting

error sequence. Several quantizer transfer function models exist in the literature [91, 2, 92, 93, 94]; however, I chose to use measured transfer functions, since all models exhibit some deficiencies and to better validate the modeling method against measurements.

6.1.2.1 Simulated Amplitude and Phase of Quantization Harmonics

I simulated the effect of quantizer nonlinearities by digitally generating a sinusoidal input with a particular amplitude. To the signal, I added thermal and phase noise and a DC offset, and initialized the tone to a different starting phase. I based the simulations on the technique employed in [2]. I then quantized the signal with noise to 16-bit integers. Then, using the measured error sequence as a 16-bit error look-up table (LUT), I mapped the ideally quantized sinusoid to the error LUT yielding a quantizer error sequence. Finally, I transformed the simulated error sequence into the frequency domain and measured the complex Fourier coefficient a_{km} for the kth harmonic and mth channel.

Fig. 6.4a shows the simulated complex Fourier coefficients $|a_{km}|$ of the 16 channels for $k = 2,3,4,5$ using the measured transfer functions for input powers from -60 to -0.2 dBFS. The frequency of the test signal was exactly in the center of the fifth bin of a 524 288-bin DFT; this ensured no spectral leakage or scalloping loss [95]. Fig. 6.4b shows the phase offset ϕ_{km} of the same data.

From Fig. 6.4a, $|a_{km}|$ remains nearly constant over all input powers, except

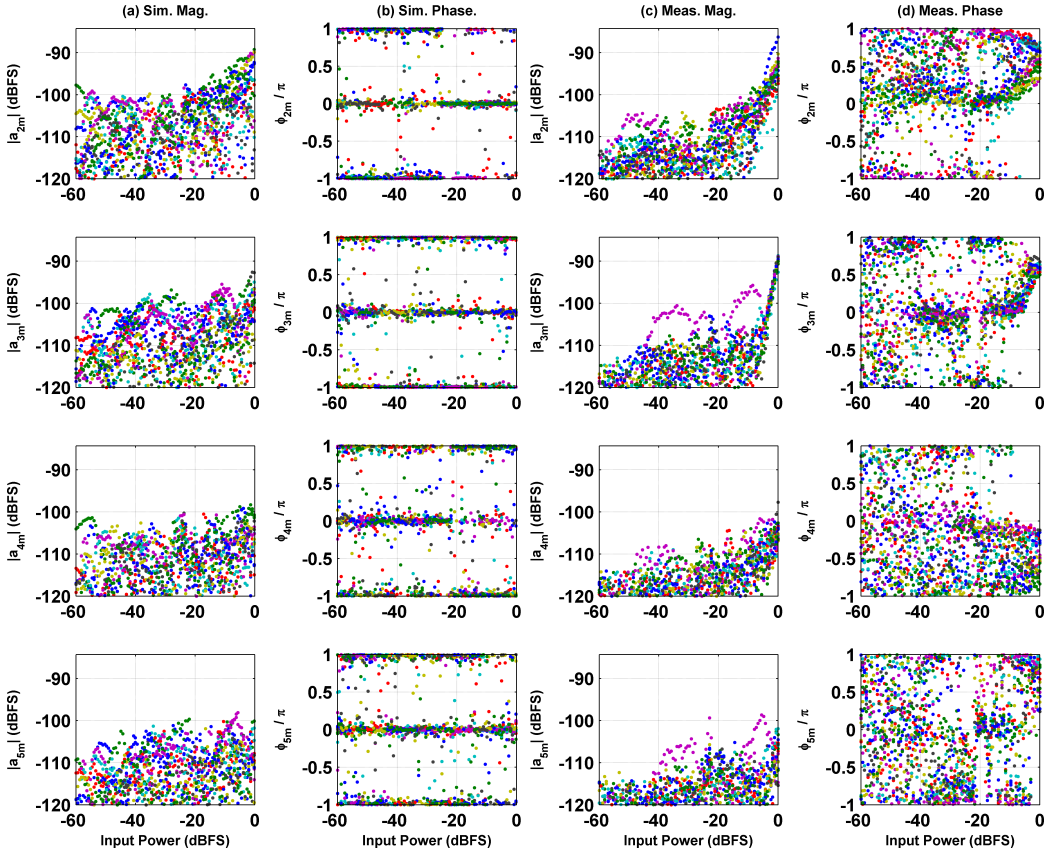

Figure 6.4: (a) Simulated $|a_{km}|$. (b) Simulated ϕ_{km}. (c) Measured $|a_{km}|$. (d) Measured ϕ_{km}. The simulated results used the measured INL with a noise signal as suggested in [2]. The measured results were measured at 38.6 MHz using the experimental test bed. The measured magnitudes show similar trends; the magnitude is nearly constant over most input powers with the second and third harmonics increasing near full scale. At lower powers, the simulated is higher than the measured. The simulated and measured phase offsets are vastly different.

for $k = 2,3$ at high input powers, which increase significantly. I believe the increase in second and third harmonic powers at higher input powers is due to the large-scale structure of the INL shown in Fig. 3.27. At large powers, the large-scale structure causes significant second and third harmonics, while higher-order harmonics are generated from the more random INL structure. In addition, at all input powers, the second and third harmonics are higher power than the fourth and higher harmonics.

The phase offset of the simulated data is generally around 0 or $\pm\pi$, with some deviation due to the noise, as shown in From Fig. 6.4b. In a second simulation, I subtracted the original noisy signal and found that the phase is either exactly 0 or exactly $\pm\pi$. There are no transient effects in the simulation to cause a phase offset other than 0 or $\pm\pi$. The phase offsets appear randomly and evenly distributed between 0 or $\pm\pi$.

6.1.2.2 Measured Amplitude and Phase of Quantizer Harmonics

I then measured the harmonic coefficients of each channel by applying a tone from each of the 16 DDSs to each of the ADCs through a lowpass AAF, using the test bed described in Section 3. The input signal frequency was slightly off of 38.6 MHz, so that the signal was near the center of a DFT bin. When the signal is near the center of the frequency bin, spectral leakage and scalloping loss are reduced; however, I still applied a Hann window to further reduce spectral leakage. I chose a signal in the first Nyquist zone to ensure that I measured

harmonics caused by the quantizer instead of the sampler, since the sampler harmonics are proportional to frequency; however, the measurements indicate that above -10 dBFS the sampler distortion is significant and impacts our ability to measure the quantizer nonlinearities. I chose an input signal frequency near 38.6 MHz to match our 48 MHz lowpass AAFs, which have a filter rejection of greater than 80 dB at the second harmonic frequency of 77.2 MHz; the second harmonic from the DDS and amplifier after filtering at the input of the ADC was approximately -140 dBc. I measured 100 input signal powers from -60 to -0.2 dBFS at the ADC. The differences in ADC input power between channels were calibrated out using a closed-loop calibration step. At each input power, the ADC captured 524 288 samples (the same as the simulation). I then transformed the signals to the frequency domain using a DFT and measured the harmonic coefficients a_{km}.

Fig. 6.4c and d show the measured $|a_{km}|$ and ϕ_{km} for $k = 2,3,4,5$ for input powers from -60 to -0.2 dBFS. The magnitude of the measured harmonics below -10 dBFS are below the simulated harmonics, but by a small amount. I think impact of dithering is underestimated in the simulated harmonics magnitudes, which results in a higher harmonic magnitude. The measured phase offsets below -10 dBFS appear largely random with some grouping around 0 and $\pm\pi$ like the simulation. Again, the increase in random phase can be attributed to the impact of dithering on low magnitude harmonics.

Above -10 dBFS, I think the sampler distortion began to impact the measured quantizer harmonics. The measured second and third harmonics increase like the simulation; however, all measured harmonic magnitudes increased above

zero, which was not predicted by the simulation. In addition, near full scale, the phase offsets begin to cluster towards the phase offset of the sampler distortion $\pi/2$. At full scale, third harmonic from the sampler distortion is larger than the quantizer distortion, while the second harmonic sampler distortion remains below the quantizer harmonics. The sampler distortion theory and quantizer model predicted the measured behavior very well.

6.1.2.3 Predicted Quantizer Harmonic Correlation

The simulations predict that the quantizer harmonic phases group around 0 and $\pm\pi$. Above -10 dBFS, the measured results indirectly match these results. Below -10 dBFS, the phase offsets are largely random with some grouping. From this, I predict the correlation that the quantizer harmonics will be largely uncorrelated; however, the tendency to group around 0 and $\pm\pi$ will result in significant correlation at times, as well as significant cancellation. Because of the possibility of strong correlation, it is important to attempt to decorrelate the harmonics even at low input frequencies.

6.1.2.4 Maximum Quantizer Harmonic Power

The previous analysis, simulation, and measurements led us to conclude that any decorrelation technique should focus on the lowest-order harmonics and ignore the higher-order harmonics. Unlike the sampler distortion harmonics, the quantizer harmonics show random amplitude characteristics. I want to ensure

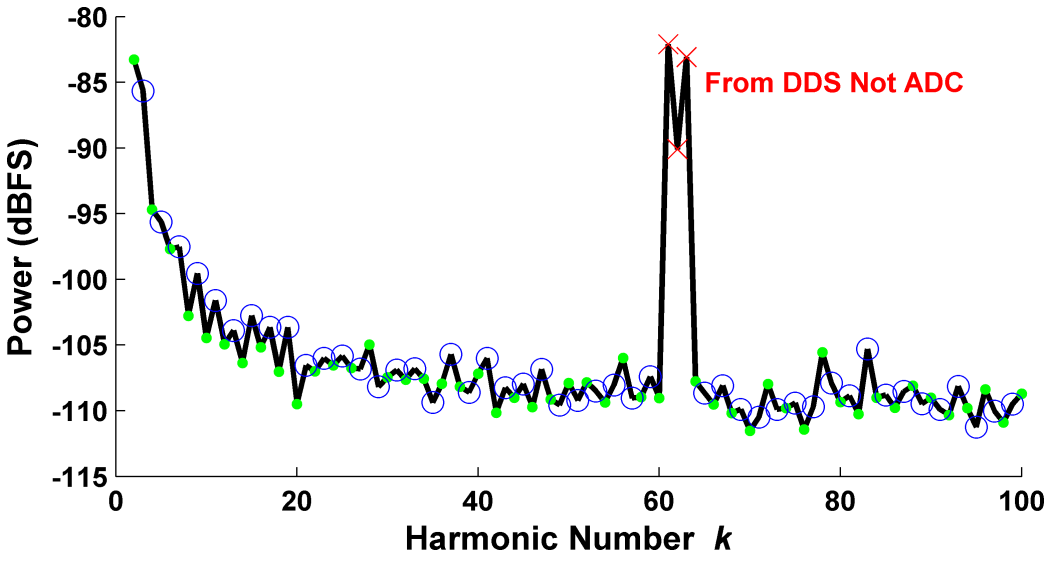

Figure 6.5: Maximum measured harmonics for $k = 2, ..., 100$ for 100 input powers from -60 to -0.2 dBFS at 38.6 MHz. The maximum powers for the tenth and higher ADC harmonics are below -100 dBFS.

that the higher-order harmonics at some arbitrary input power are not as larger as the lowest-order harmonics. Fig. 6.5 shows the maximum power for the first 100 harmonics for input powers from -60 to -0.2 dBFS collected at the same time as the previous quantizer harmonic measurements. The green dots are the even harmonics and the blue circles are the odd harmonics. Neglecting the peaks at $k = 61, 62, 63$, which are due to the DDS, the second and third harmonics are the highest. The maximum power for the tenth and higher harmonics is -100 dBFS, more than 15 dB below the maximum second harmonic, which confirms that higher-order harmonics remain much lower than the lowest-order harmonics. The noise per bin with the Hann window is about -123 dBFS/bin, which is about 12 dB below the lowest harmonic, ensuring that the results are not noise limited.

6.2 Inherent Harmonic Correlation in Parallel ADC Arrays

The previous sections evaluated the origins of harmonics in ADCs and provided qualitative predictions of the expected harmonic correlation in an ADC array. In this section, I investigate the inherent harmonic correlation without intentional decorrelation techniques.

6.2.1 Measured Inherent Harmonic Correlation

Using our 16 channel test bed, I measured the first 100 harmonic coefficients a_{km} for each channel for 120 input powers from -60 to -0.2 dBFS. I chose a signal frequency near 97.6 MHz so it would be near the center of a frequency bin in the DFT, although I still applied a Hann window. I performed a closed-loop phase calibration at each input power to ensure the input signals to each channel were coherent and recorded 262 144 samples per data set. The AAF reduced the second harmonic from the DDS and amplifier to approximately -135 dBc at full scale and the third harmonic to less than -150 dBc, which are well below the measured harmonics.

Fig. 6.6 shows P_k and $P_{k,\max}$ for $k = 2,3,4,5$. P_k and $P_{k,\max}$ were calculated from the measured harmonic coefficients according to (2.35) and (2.36). Above -8 dBFS input power, $P_{2,\max}$ and $P_{3,\max}$ are much larger than at lower input powers and increase linearly with input power. Both sampler and quantizer show this behavior at high input powers, so it is not possible to definitively determine the origin of those harmonics. Below -8 dBFS, $P_{k,\max}$ is nearly constant, with a slight

decrease with decreasing amplitude, for $k = 2,3,4,5$. This behavior matches the simulations and measurements of quantizer nonlinearities shown in the previous section.

For signal powers greater than -8 dBFS, the P_k of the second and fourth harmonics is closer to $P_{k,\max}$ than for the third and fifth harmonics. Above -8 dBFS, the second harmonic is both the most correlated and has the highest power. However, below -20 dBFS, the third and fifth harmonics are more correlated than the second and fourth harmonics. The SFDR of the complete system is 91.2 dB and is determined by the second harmonic magnitude.s is closer to $P_{k,\max}$ than for the third and fifth harmonics. Above -8 dBFS, the second harmonic is both the most correlated and has the highest power. However, below -20 dBFS, the third and fifth harmonics are more correlated than the second and fourth harmonics. The SFDR of the complete system is 91.2 dB and is determined by the second harmonic magnitude.

For any system full correlation yields $I_k = 1 = 0$ dB. Fig. 6.7 shows I_k for input signal powers -0.2, -5.2, -20.0, and -40.4 dBFS. At the highest input signal powers -0.2 and -5.2 dBFS, many harmonics approach full correlation with the same input signals. On the other hand, while many harmonics appear to be almost completely correlated, there are others that are significantly less correlated. For instance, at -0.2 dBFS, I_{93} is about -2 dB while I_{56} is < -20 dB. This is expected for higher order quantizer nonlinearities; some of the harmonic phases add coherently and others do not. For lower input signal powers, -20.0 and -40.4 dBFS, correlation decreases substantially across all harmonics. At these input powers,

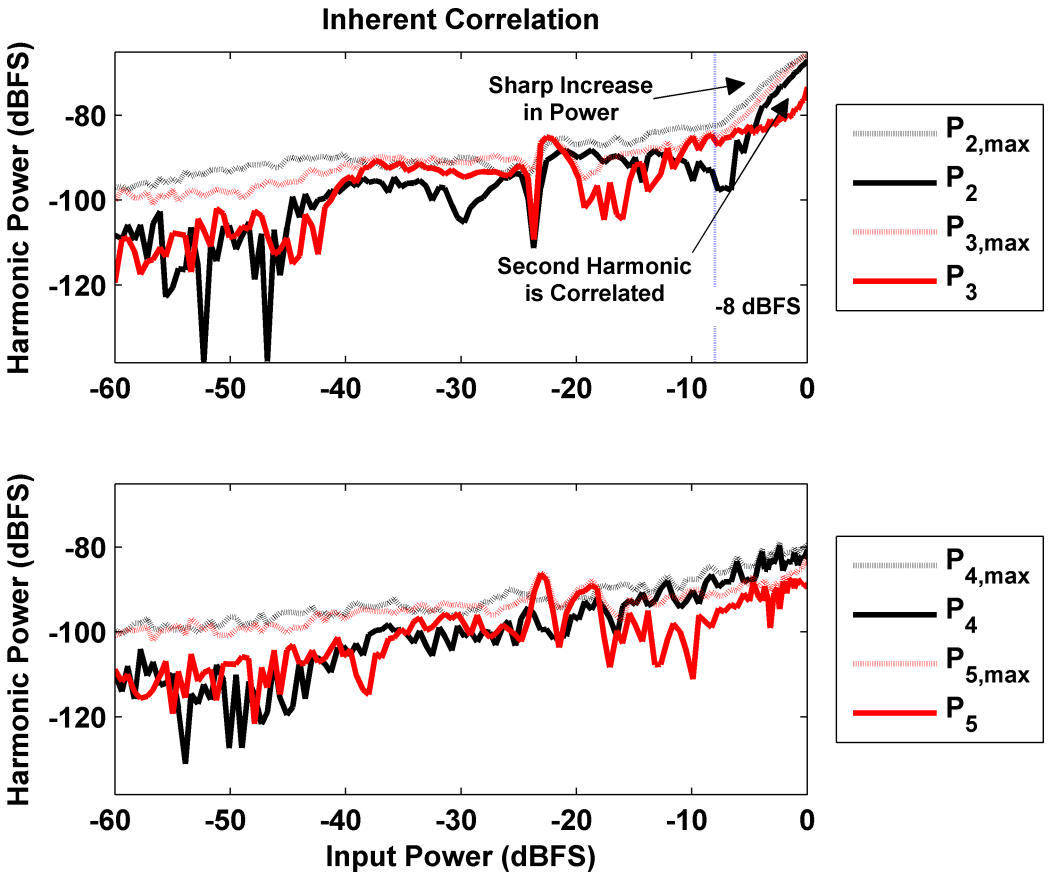

Figure 6.6: Comparison of $P_{k,\max}$ and P_k for $k = 2,3,4,5$ shows that second and fourth harmonics are more correlated at high powers (above -8 dBFS) and the third and fifth harmonics are more correlated at lower powers. The second harmonic is the largest harmonic. At some input powers, the harmonics destructively interfere and cancel.

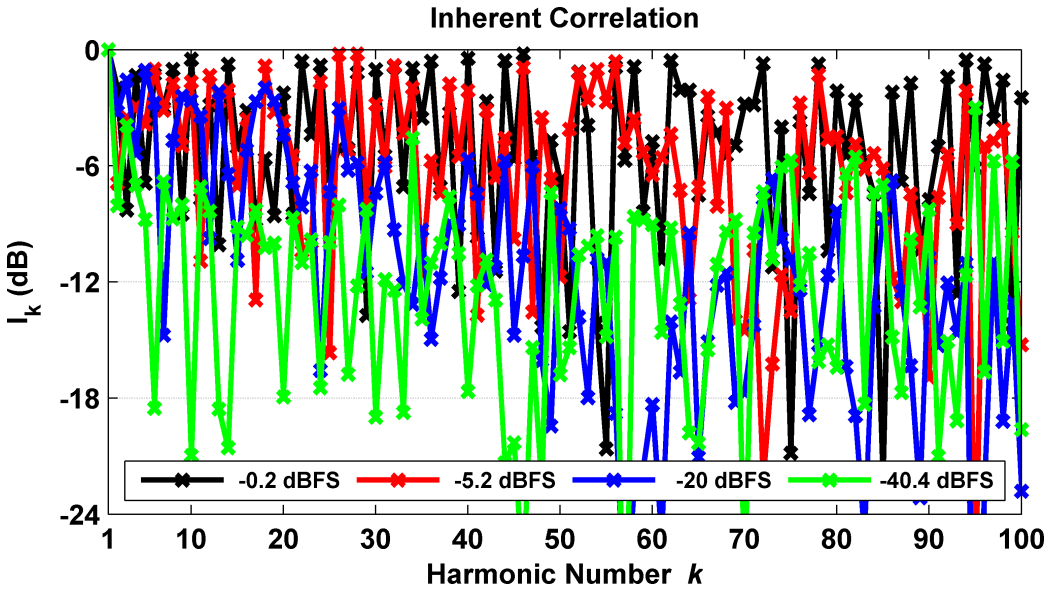

Figure 6.7: I_k and R_k at -0.2, -5.2, -20.0, and -40.4 dBFS. Many higher order harmonics are well correlated at higher input powers and less correlated at lower input powers.

the harmonics may be near the level of the noise, which is uncorrelated.

6.2.2 Inherent Correlation Summary

In the previous section, I discussed the two primary sources of harmonics in ADCs — sampler distortion and quantizer nonlinearities. I showed through modeling and measurements that the second and third harmonics exhibit the highest powers regardless of whether they arise from sampler distortion or quantizer nonlinearities.

I then demonstrated that many of the harmonics are strongly correlated. In particular, I showed (Fig. 6.6) that the second harmonic is well correlated from channel to channel, suggesting that it could significantly degrade dynamic range

improvements expected from parallelization. The focus of any decorrelation techniques should be decorrelation of the second and, to lesser extent, third harmonics.

The higher order harmonics were often correlated; however, since I showed that their maximum power is significantly below that of the lower order harmonics, these are far less of a concern. Recall that the maximum second harmonic power was about -85 dBFS, while the maximum harmonic power for the eleventh or higher harmonic was less than -100 dBFS.

6.3 Phase Decorrelation Techniques

In a previous report, Howard *et al.* proposed and demonstrated a method to decorrelate mixer spurs and harmonics in parallel receiver arrays [18]. Further measurements of this technique were performed by Rabideau using four receivers [19]. The technique involved applying a phase shift to the input signal of each channel by adjusting the LO phase driving each mixer in the parallel array. The phase shift is then removed digitally at the output, resulting in a decrease in the harmonic correlation, as described in Section 2.2.1

In this section, I apply their phase randomization approach to ADC arrays and evaluate its effectiveness at decorrelating ADC harmonics. In particular, I expand upon their investigation by confirming that harmonic correlation follows the Rayleigh distribution and demonstrate that the effectiveness of phase randomization of SFDR may be limited by the random phase offsets drawn. I then implement an improved phase cancellation approach which adjusts the input phase to cancel

the highest power harmonic. I will show that this improved technique significantly increases the resulting SFDR as compared to the phase randomization technique.

6.3.1 Phase Randomization Measurements

In order to evaluate the efficacy of the phase randomization approach, I collected two sets of data — Sets 1 and 2 — with different phase offsets in a very similar manner to that described in Section 6.2.1. I aligned the phase and amplitude of the signal into each channel at 97.6 MHz. I then adjusted the phase of the DDSs by θ_m; θ_m was different for each of the two sets, but was kept constant over all signal amplitudes. I recorded 262 144 samples per channel in the ADCs. Finally, I applied $-\theta_m$ to each channel to recorrelate the signals and measured the harmonic coefficients a_{km}. I repeated this procedure for 120 different amplitudes from -60 to 0.2 dBFS.

Fig. 6.8 shows the phase θ_m for Sets 1 and 2, plotted on the unit circle as red "x's" (the blue circles are the phases for phase cancellation discussed later). The phase sets were generated using a uniform pseudorandom number generator from 0 to 2π.

Figs. 6.9 and 6.10 show P_k and $P_{k,\max}$ for $k = 2,3,4,5$ for the phase randomization Sets 1 and 2. As expected, $P_{k,\max}$ for each case is similar to $P_{k,\max}$ from Fig. 6.6, since only the phase has changed and $P_{k,\max}$ ignores the phase of the harmonics. Looking first at Set 1, P_k is well below $P_{k,\max}$ for all harmonics plotted, indicating substantial decorrelation. The average values of I_2 and I_3 over

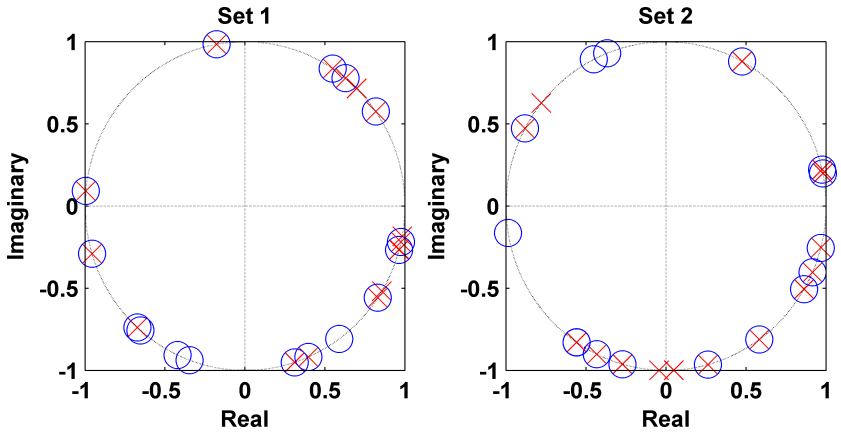

Figure 6.8: Distribution of phase randomization Sets 1 and 2 around the unit circle. Sets were generated using uniform pseudorandom number generator from 0 to 2π. Phase randomization used the red "x" phase offsets and phase cancellation used the adjusted blue circle phase offsets.

all amplitudes are -13.2 and -14.4 dB, slightly below (in other words, better than) the Rayleigh approximation. The SFDR is 101.5 dB.

Clearly, comparing Figs. 6.9 and 6.10, phase randomization was less effective for Set 2 than for Set 1. In particular, P_2 and P_3 are much higher (indicating more correlation) at high powers. The mean values of I_2 and I_3 over all input powers are only -7.7 and -9.6 dB, but are greater (worse) at higher input powers where P_k is largest, so that the SFDR is only 95.5 dB. Set 2 is less effective due to the particular phase offsets drawn. In Set 2, despite the input phases being random, the second and third harmonics, at higher input powers, tend to be on the same half of the unit circle, which invalidates the Rayleigh approximation and results in a high I_k. This demonstrates a weakness of this technique: while most of the harmonics may approach the Rayleigh distribution and be decorrelated, if the

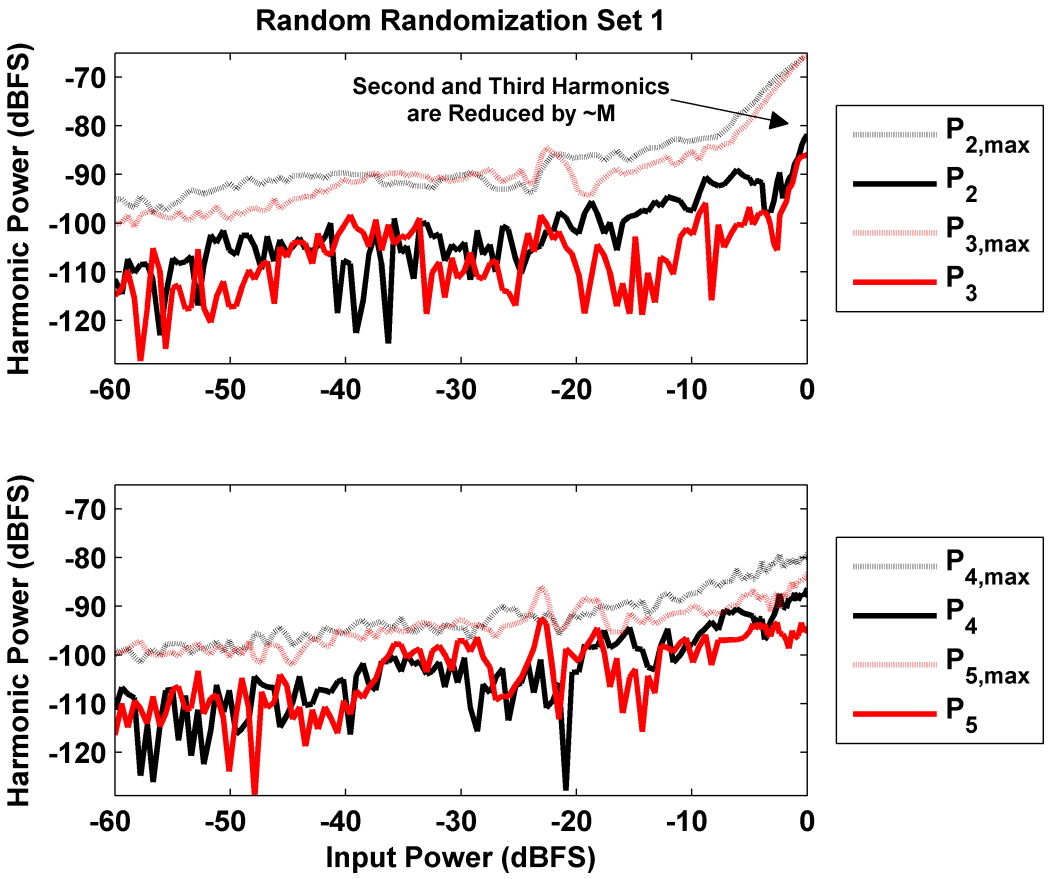

Figure 6.9: Phase randomization Set 1 effectively decorrelates the harmonics. The SFDR improves to 101.5 dB from 91.2 dB.

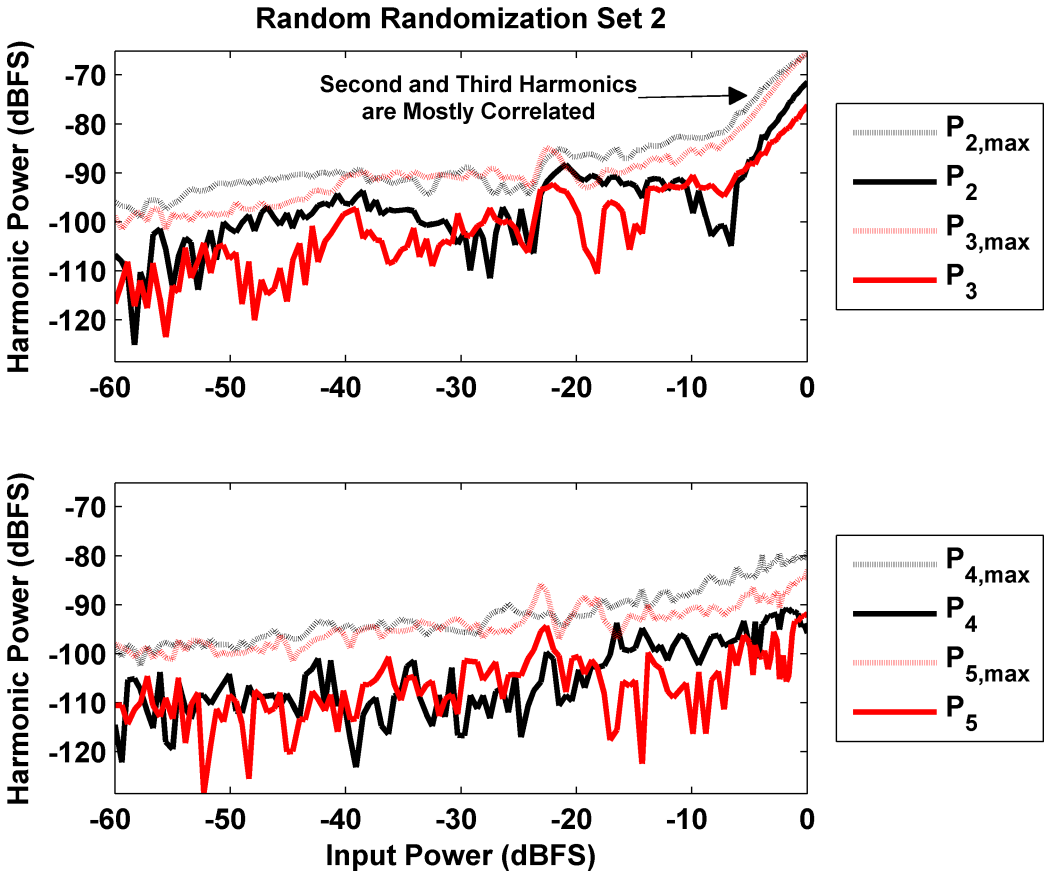

Figure 6.10: Phase randomization Set 2 is less effective than Set 1. Both the second and third harmonic are largely correlated at higher powers and the SFDR is only 95.5 dB compared to 101.5 dB for Set 1.

largest harmonics are well correlated (by chance) then the SFDR improvement is minimal.

Fig. 6.11 shows I_k for Sets 1 and 2 for $k = 2$ to 100. The difference between the two sets is small for $k \geq 6$, and both are more effective than no decorrelation technique.

Howard *et al.* predicted that phase randomization results in a Rayleigh distribution for the harmonic voltage gain ν. Fig. 6.12 shows twelve-point histograms

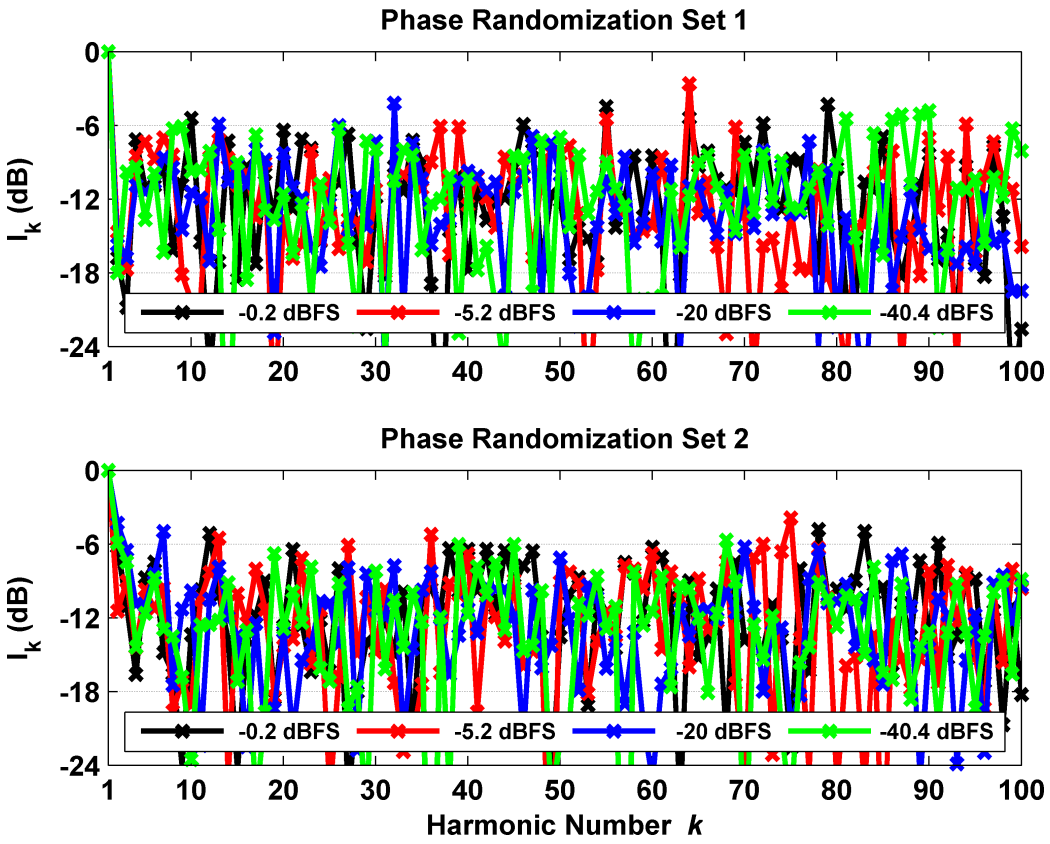

Figure 6.11: Measured I_k for phase randomization Sets 1 and 2 at -0.2, -5.2, -20.0, and -40.4 dBFS. I_k shows significant decorrelation for all harmonics unlike Fig. 6.7. The peak I_k is about -3 dB and the average is approximately M^{-1}.

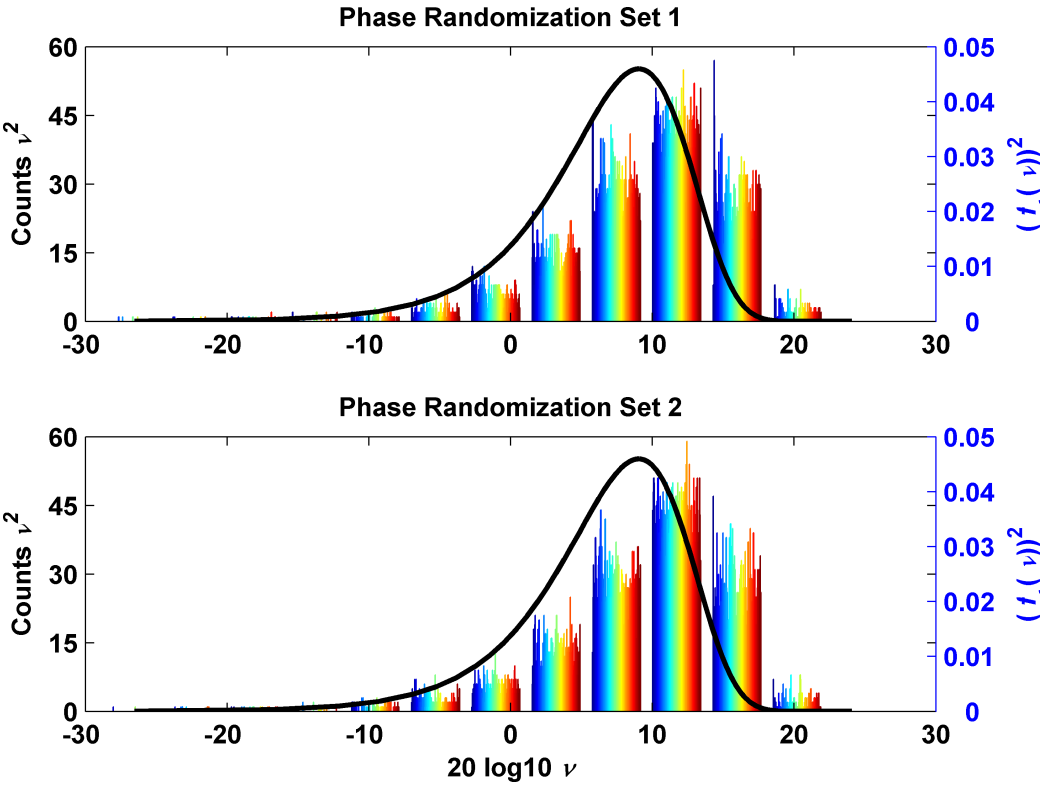

Figure 6.12: 12-point histograms of ν^2 across 120 input powers have a similar shape to the Rayleigh distribution $f_\nu(\nu)$.

of ν^2 for Sets 1 and 2 along with plots of the Rayleigh distribution $(f_\nu(\nu))^2$ for $M = 16$. The histograms show the first 100 harmonics across 120 input powers. Both histograms appear similar to Rayleigh distribution confirming this prediction. The expected value of ν^2 for Sets 1 and 2 are 16.1 and 16.5, which is very close to the predicted value of $M = 16$. Set 2 appears to be skewed higher than Set 1 resulting in a slightly higher expected value.

Phase randomization reduces the correlation of harmonics as predicted. I tested two sets and they showed different levels of decorrelation on the low order harmonics; the SFDR improved from 91.2 dB with no phase shifts to 101.5

and 95.5 dB. While the average I_k was about M^{-1}, the peak values of I_k were as high as -4 dB, which will impact SFDR. I confirmed that the harmonics follow the Rayleigh distribution. Parallel system designers must include this statistical behavior of the harmonics in their designs.

6.3.2 Phase Cancellation

As an extension to Howard *et al.*'s phase randomization technique, I propose an enhanced technique, in which I attempt to align the harmonic phases in such a way that the largest harmonic is canceled. Our approach arises from two observations: first, the phase of a harmonic at a particular input power level is predictable for both sampler distortion and quantizer nonlinearities; second, the low order harmonics dominate the total SFDR. For all the data sets observed so far, the second harmonic is always the highest, and it is always largest at the maximum input power. Therefore, by arranging the second harmonic phases in such a way that they cancel at the maximum input power the total system SFDR may be increased. Other harmonics could be chosen for optimization instead of the second harmonic, such as the third harmonic, depending of the specifics of the system, such as bandwidth and harmonic sources.

6.3.2.1 Theory of Operation

I randomly distribute the input phases, using the same distribution as the phase randomization technique. I then measure the complex Fourier coefficients

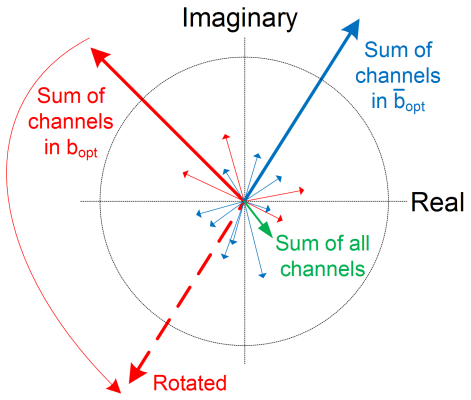

Figure 6.13: The vector formed by the sum of b_{opt} is rotated, so that it is π out of phase with the sum of the channels of $\bar{b}_{\text{opt}}$.

of the second harmonic $a_{2,m}$ for an input signal at full scale. I group the harmonics into two sets b_{opt} and $\bar{b}_{\text{opt}}$, such that the magnitude of sum of the second harmonics from the b_{opt} channels approximately equal the sum of the second harmonics of the $\bar{b}_{\text{opt}}$ channel harmonics,

$$\left| \sum_{i=b_{\text{opt}}} a_{2,i} \right| \approx \left| \sum_{i=\bar{b}_{\text{opt}}} a_{2,i} \right|. \tag{6.2}$$

Once I find b_{opt} and $\bar{b}_{\text{opt}}$, I adjust the phase of the sum of the channels in the set b_{opt} to be π out of phase with the channels in $\bar{b}_{\text{opt}}$,

$$\angle \left(\sum_{i=b_{\text{opt}}} a_{2,i} \right) - \angle \left(\sum_{i=\bar{b}_{\text{opt}}} a_{2,i} \right) = \pi \tag{6.3}$$

I adjust the phase of the harmonics by changing the input phases θ_m for $m = b_{\text{opt}}$.

I find b_{opt} by searching over all possible sets of channels b, where the size of b may vary from 1 to $M/2$. The number of possible combinations increases with the total number of channels Then, for all the possible sets of b, I attempt to

find the sets that meet the condition in (6.2) by calculating the following ratio:

$$\frac{\max\left(\left|\sum_{i=b} a_{2,i}\right|, \left|\sum_{i=\bar{b}} a_{2,i}\right|\right)}{\min\left(\left|\sum_{i=b} a_{2,i}\right|, \left|\sum_{i=\bar{b}} a_{2,i}\right|\right)}. \tag{6.4}$$

The set of b that minimizes the ratio is b_{opt}. Appendix B includes the Matlab code to determine b_{opt}.

6.3.2.2 Phase Cancellation Measurements

Starting with the two sets of phase randomization data presented previously, I determined the optimal second harmonic phase cancellation sets b_{opt} and $\bar{b}_{\text{opt}}$ using the method described above. To expedite the search, I limited the size of b to four or less (the size of $\bar{b}$ was 13 to 16). The adjusted phases θ_m that satisfy (6.3) are marked with blue circles in Fig. 6.8. Using the adjusted phase offsets, I remeasured the harmonic coefficients a_{km} at 97.6 MHz for input powers -60 to -0.2 dBFS. Figures 6.14 and 6.15 show P_k and $P_{k,\text{max}}$ for the second through fifth harmonics.

Figures 6.14 and 6.15 clearly show that the second harmonics cancel at full scale, with 42 dB of cancellation for Set 1. The third, fourth, and fifth harmonics of both sets are not canceled; however, these show the same level of decorrelation as the previous phase randomization data. The cancellation does not continue over the full input power range, but does reduce the maximum second harmonic power significantly. The SFDR increases from 101.5 to 103.9 dB for Set 1 and from 95.5 to 103.4 dB for Set 2. This is an improvement of 2.4 and 7.9 dB, respectively,

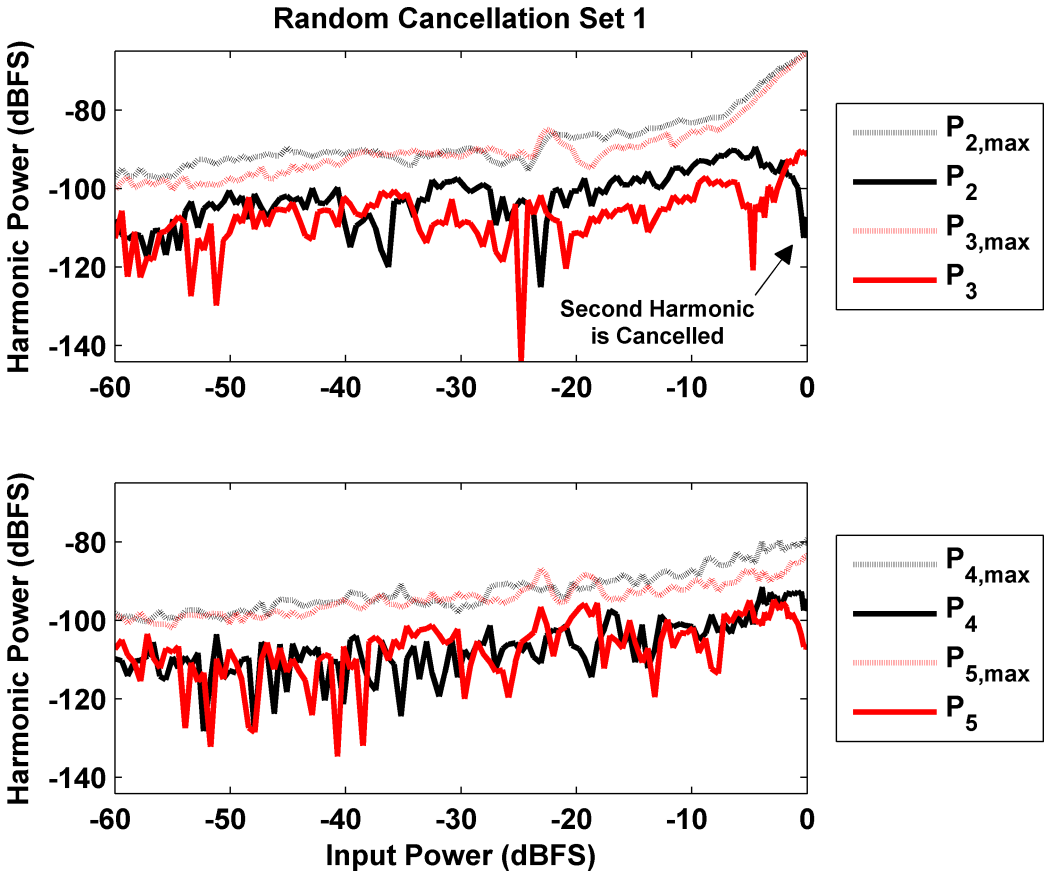

Figure 6.14: Measured P_k and $P_{k,\max}$ for $k = 2,3,4,5$ using phase cancellation technique for Set 1. The second harmonic is well canceled at full scale and improves the SFDR to 103.9 dB from 101.5 dB. The correlation of the other harmonics does not increase.

compared to phase randomization alone. I_k for $k \geq 6$ for both sets is similar to the results from phase randomization. The increase in SFDR is significant and is achieved with little additional complexity.

Since the harmonic phase offsets ϕ_{km} vary over frequency and amplitude, the cancellation degrades as I change the frequency and amplitude from 97.6 MHz and -0.5 dBFS. To determine the reduced effectiveness, I measured phase cancellation

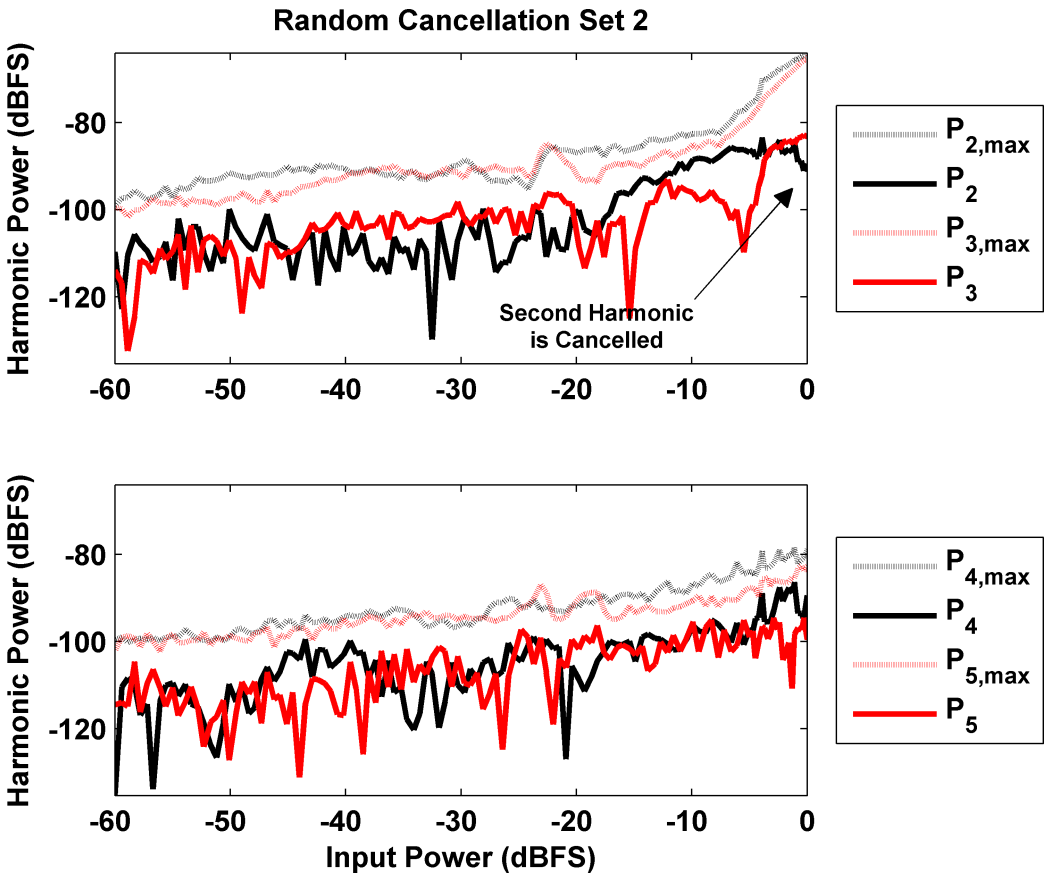

Figure 6.15: Measured P_k and $P_{k,\max}$ for $k = 2,3,4,5$ using phase cancellation technique for Set 2. The results are similar to Set 1 and the SFDR increases to 103.4 dB from 95.5 dB.

data sets using the same phase offsets trained at 97.6 MHz for input signal frequencies of 86.64 and 91.64 MHz. The second harmonic is in the fourth Nyquist zone at 91.64 and 97.6 MHz, while it is in the third Nyquist zone at 86.64 MHz. Because the Nyquist zone changes, the second harmonic phase changes sign, so I expect that phase cancellation will be less effective for a signal frequency of 86.64 than 91.64 MHz. The third harmonic does not undergo a phase change for these frequencies.

Fig. 6.16 shows the measured P_k for Set 1 at 91.64 and 86.64 MHz, and Fig. 6.17 shows the measured P_k for Set 2 at 91.64 and 86.64 MHz. At 91.64 MHz, the second harmonic is canceled in both sets, although the null is not quite as deep as at the training frequency 97.6 MHz. The SFDR is 104.0 and 99.3 dB for Set 1 and Set 2, respectively. On the other hand, at 86.64 MHz, the second harmonic does not cancel significantly for either set, with the second harmonic of Set 2 significantly more correlated. Although substantial improvements from phase cancellation were not achieved for 86.64 MHz, when using offsets calculated for 97.6 MHz, the SFDR is still 99.5 and 96.2 dB for Sets 1 and 2, respectively, which is comparable to SFDR achieved using phase randomization.

In summary, I have shown that phase randomization techniques reduce correlation of harmonics in ADC arrays; however, a particular set of phase offsets, such as phase randomization Set 2, may not provide a substantial increase in SFDR. Further, I extended this approach to include phase cancellation of the highest power harmonic, which results in a further increase in SFDR. The phase cancellation offsets are trained at a particular frequency, and if the harmonic phases

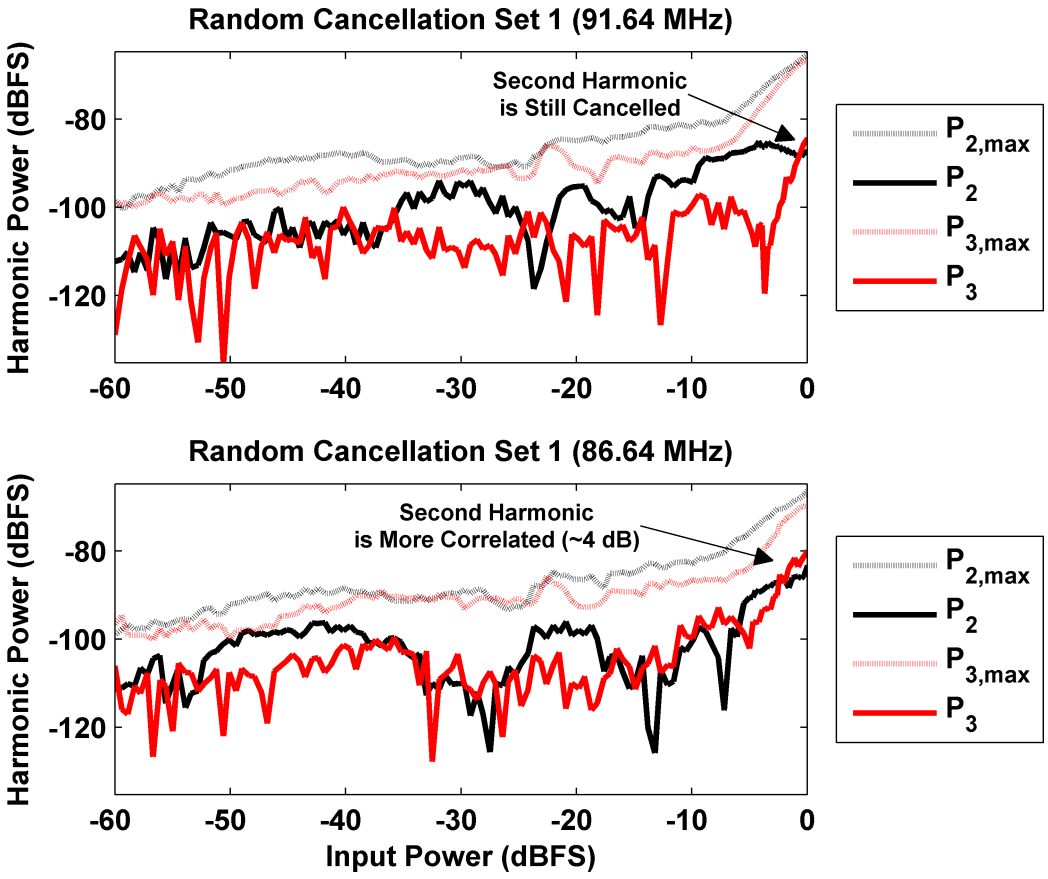

Figure 6.16: Measured P_k and $P_{k,\max}$ for $k = 2,3$ using phase cancellation Set 1 phases. At 86.64 MHz, the second harmonic is not canceled due to the Nyquist zone difference with the training data. At 91.64 MHz, the second harmonic is well canceled.

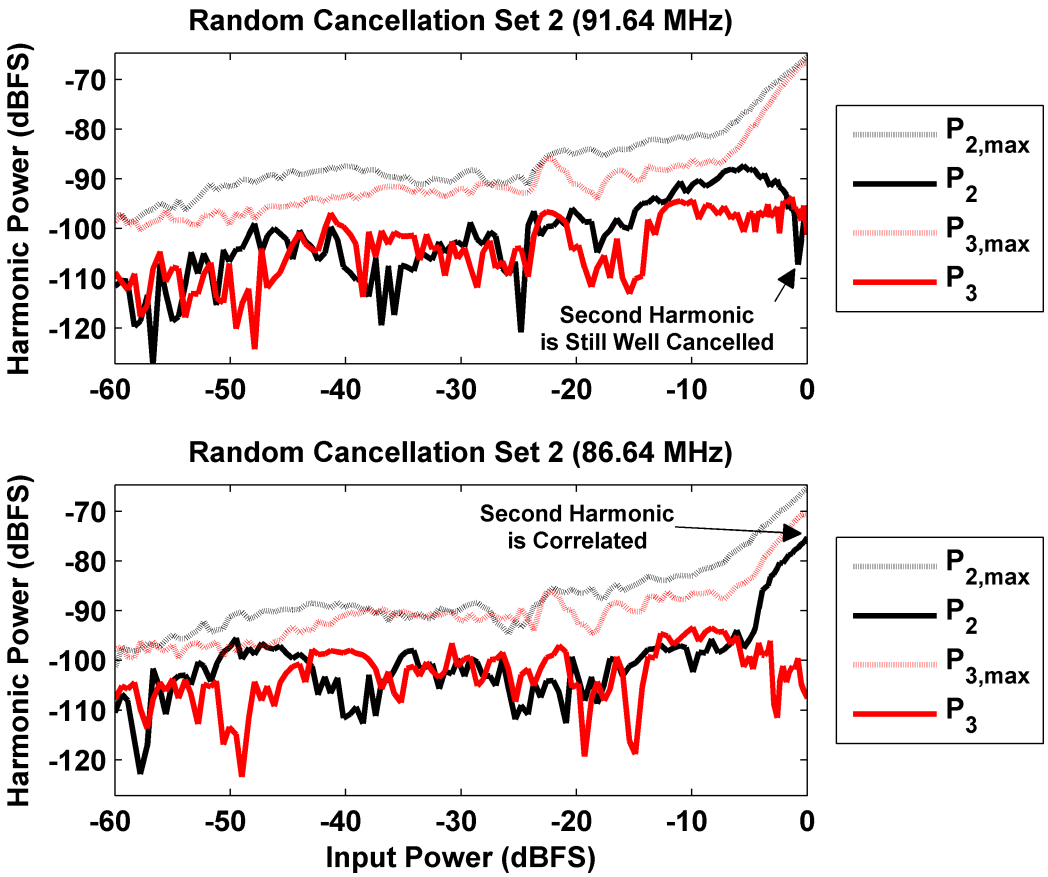

Figure 6.17: Measured P_k and $P_{k,\max}$ for $k = 2,3$ using phase cancellation Set 1 phases. At 86.64 MHz, the second harmonic is largely correlated and the SFDR is reduced. At 91.64 MHz, the second harmonic cancels as expected.

change significantly from the initial conditions, the cancellation may become less effective; however, the SFDR with this less effective cancellation is still comparable to that of the phase randomization techniques. Phase cancellation is an effective method to improve the total SFDR compared to phase randomization.

6.4 Frequency Decorrelation Techniques

Besides proposing the use of phase offsets to decorrelate spurs, Howard *et al.* suggested an implementation using frequency offsets [20, 21]. Howard's method causes the harmonics to be offset in frequency from channel to channel, so that when the channels are combined the harmonics do not add, resulting a SFDR improvement of M^2. I discuss Howard's method and introduce an extension of this technique. In our extension, I apply frequency offsets to each sampling clock, which causes aliased harmonics to occur at different frequencies. Our extension removes the need for the mixer (shown in Fig. 2.3) required for the phase decorrelation and frequency offset techniques, making it more appropriate for a wider range of systems.

6.4.1 Frequency Offset Measurements

In order to experimentally verify the expected decorrelation, I applied the frequency offset technique to our test bed. 16 full scale signals were applied to the 16 ADCs, each 10 kHz apart from the previous channel. I then converted the digitized signal to complex baseband using the Hilbert transform. Next, I

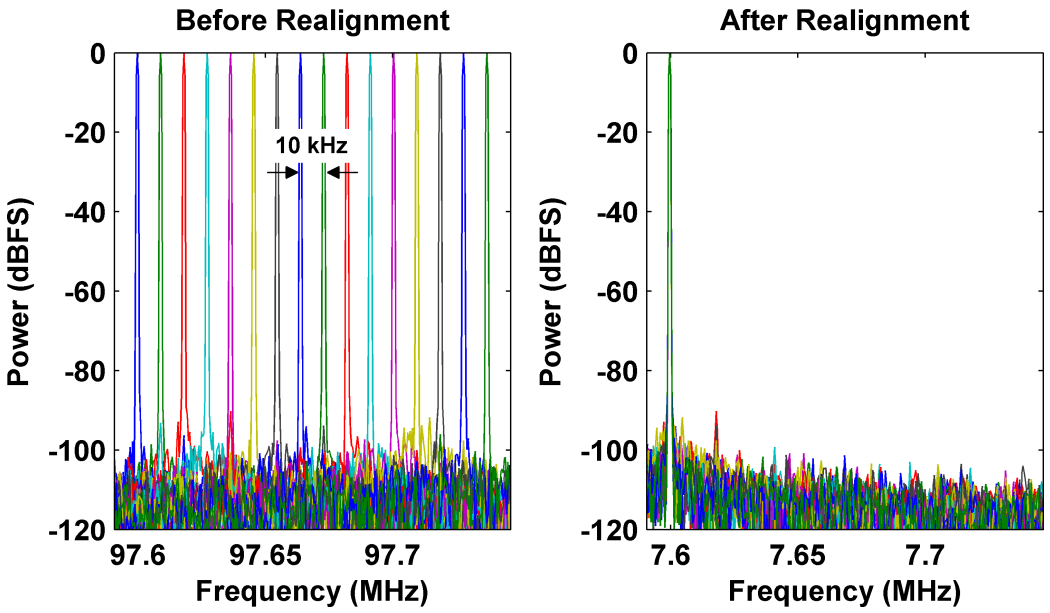

Figure 6.18: Before realignment, each channel is offset by 10 kHz from the previous channel. After downconversion and realignment, the signals coincide in frequency and are correlated.

multiplied each term by the opposite frequency offset to frequency align each channel. Finally, I measure and remove the constant phase error θ_m. Fig. 6.18 shows the input signal before and after frequency realignment, which verifies that before realignment the signals were offset by 10 kHz, and that after realignment they are realigned.

Figures 6.19 and 6.20 show the second and third harmonics before and after realignment. The signal and second harmonic are both in even Nyquist zones, and the offset is 10 kHz $(k-1)$, while the third harmonic is in an odd Nyquist zone and the offset is 40 kHz $(k+1)$. The highest harmonic of a single channel is about -84.2 dBFS, so the system SFDR is $10\log_{10}(16^2) = 24.1$ dB higher at about 108.2 dB. Frequency offsets provide a higher system SFDR than either phase

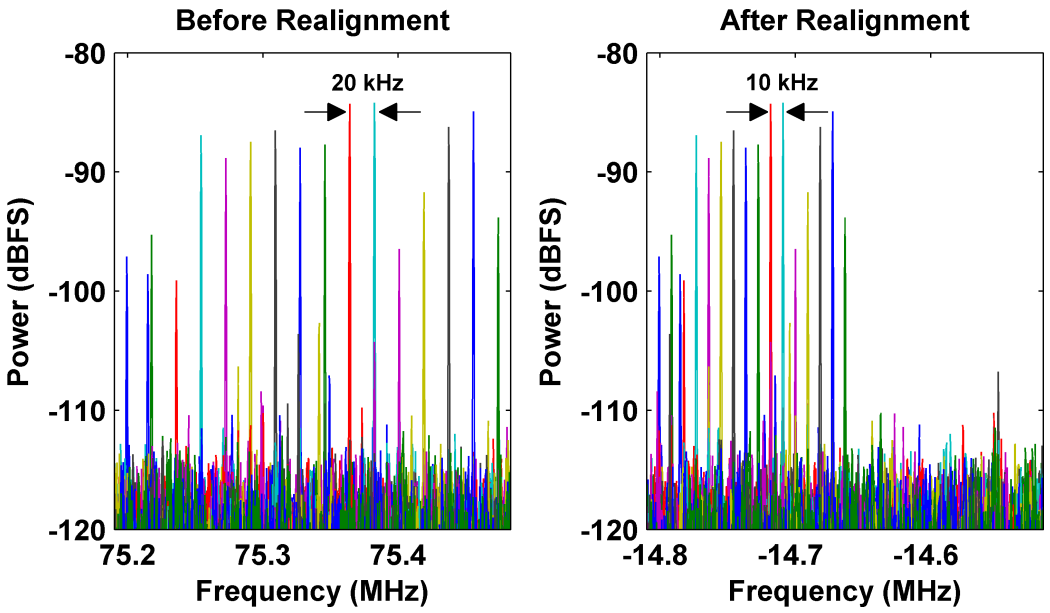

Figure 6.19: Prior to realignment, the second harmonics are spaced by 20 kHz. After realignment, though the fundamental signals coincide, the second harmonics remain offset by 10 kHz, and as a result do not sum.

randomization, where the best was 101.5 dB, or phase cancellation, where the best was 103.9 dB.

6.4.2 Clock Offsets

As an extension of the frequency offset approach, I also present an alternative method, in which I adjust the frequency of the ADC clock rather than the frequency of an LO. This technique has the advantage that no mixer is required, making it useful in a larger range of systems, such as direct RF sampling systems [96, 97].

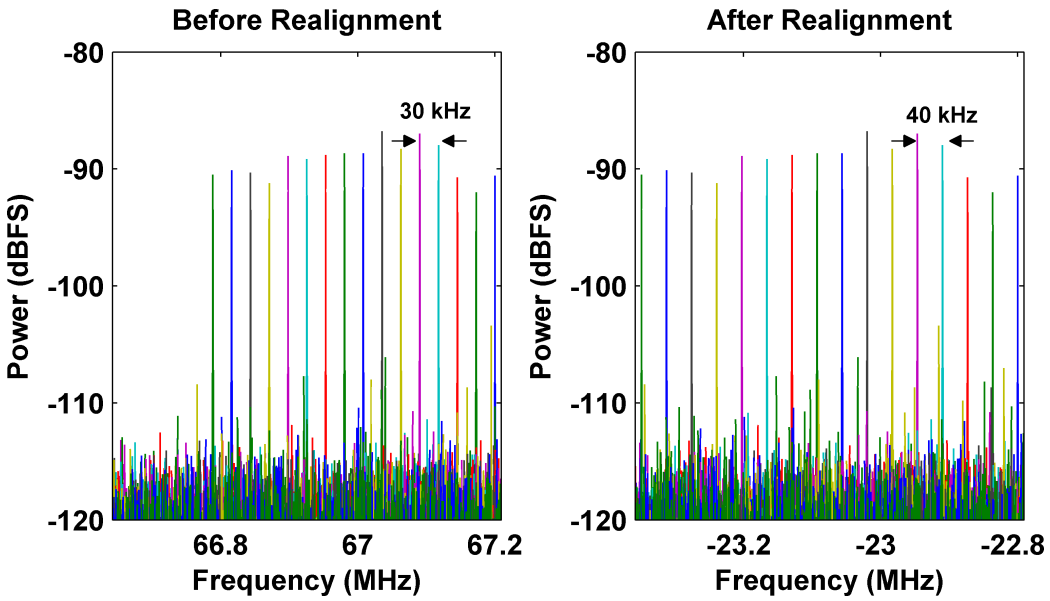

Figure 6.20: Before realignment, the third harmonics are spaced by 30 kHz. After realignment, they are spaced by 40 kHz ($k+1$).

6.4.2.1 Theory of Operation

Fig. 6.21 shows the clock offset technique. The basic concept is similar to frequency offsets; by driving each ADC clock at a slightly different frequency, the generated harmonics of each channel are offset in frequency, while the signal remains correlated. With this technique, all aliased harmonics and other spurious signals are offset in frequency. For illustration, consider a system with two clocks, 118 and 120 MHz, and a signal at 34 MHz. The second harmonic occurs at 68 MHz regardless of the sampling rate; however, the second harmonics alias to different frequencies, 50 and 52 MHz within the first Nyquist zone. This frequency separation occurs for all signals that alias. This has a side benefit that even harmonics from the signal source are offset in frequency, and the anti-aliasing filter requirements may be able to be relaxed. The signal must still satisfy the Nyquist

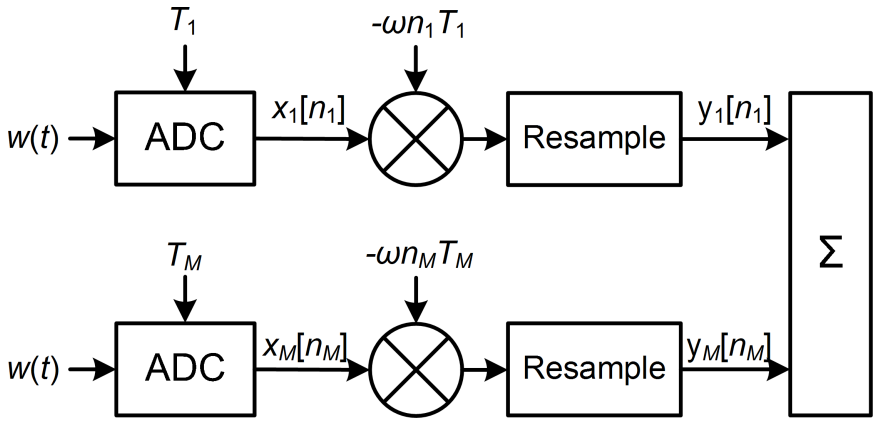

Figure 6.21: Schematic of the clock offset technique. Each channel is sampled by a different frequency and then digitally resampled to realign the signals.

conditions for all clock frequencies.

The signal $w(t)$ from (2.39) is sampled by M independent (but phase locked) oscillators with sampling periods of T_m and sampling frequency $f_m = 1/T_m$. The sampled signal is

$$x_m[n_m] = A(n_m T_m)\cos\left(\omega n_m T_m - p(n_m T_m)\right) + \varepsilon_m(w(n_m T_m)) \tag{6.5}$$

where n_m is a channel specific sample index, $A(t)$ and $p(t)$ are amplitude and phase modulation, and ε is the harmonic distortion, as before. The signal is digitally downconverted to baseband by applying the Hilbert transform and multiplying by $e^{-j\omega n_m T_m}$. The resulting complex signal component is

$$A(n_m T_m)e^{-jp(n_m T_m)} \tag{6.6}$$

and the harmonic component is

$$\mathcal{H}(\varepsilon_m(w(n_m T_m)))e^{-j\omega n_m T_m}. \tag{6.7}$$

Finally, the signals are realigned by digital resampling to nT_0.

I again assume that $A(t) = A$ and $p(t) = 0$. The harmonics are

$$a_{km} e^{jk\omega n_m T_m} e^{-j\omega n_m T_m} \tag{6.8}$$

which aliases to positive frequencies in the first Nyquist zone. The aliased frequency of the kth harmonic for an input frequency of f_{in} is

$$\min\left((k-1)f_{\text{in}} \mod f_m, f_m - (k-1)f_{\text{in}} \mod f_m\right). \tag{6.9}$$

The aliasing (mod operation) thus induces the frequency offset of the harmonics.

6.4.2.2 Clock Offset Measurements

In order to test the clock offset technique, I reconfigured the experimental test bed, such that eight DDSs and amplifiers were connected as clocks to eight ADCs. A fourth-order lowpass filter was connected to the output of each amplifier to reduces the clock spurs. I used a laboratory signal generator as the common signal source. The signal generator was filtered using a bandpass filter described in Section II and split using a Wilkinson power divider.

In order to first confirm the signal correlation of a complicated signal sampled at different rates, I applied a pseudorandom additive white Gaussian noise (AWGN) signal with 10 MHz of bandwidth centered at 91.6 MHz to the ADCs. I sampled the signal with the following clock frequencies, one on each channel: 118.6, 118.8, 119.0, 119.2, 119.4, 119.6, 119.8, and 120.0 MHz. Fig. 6.22 shows the sampled signal plotted in the second Nyquist zone. The white noise signal

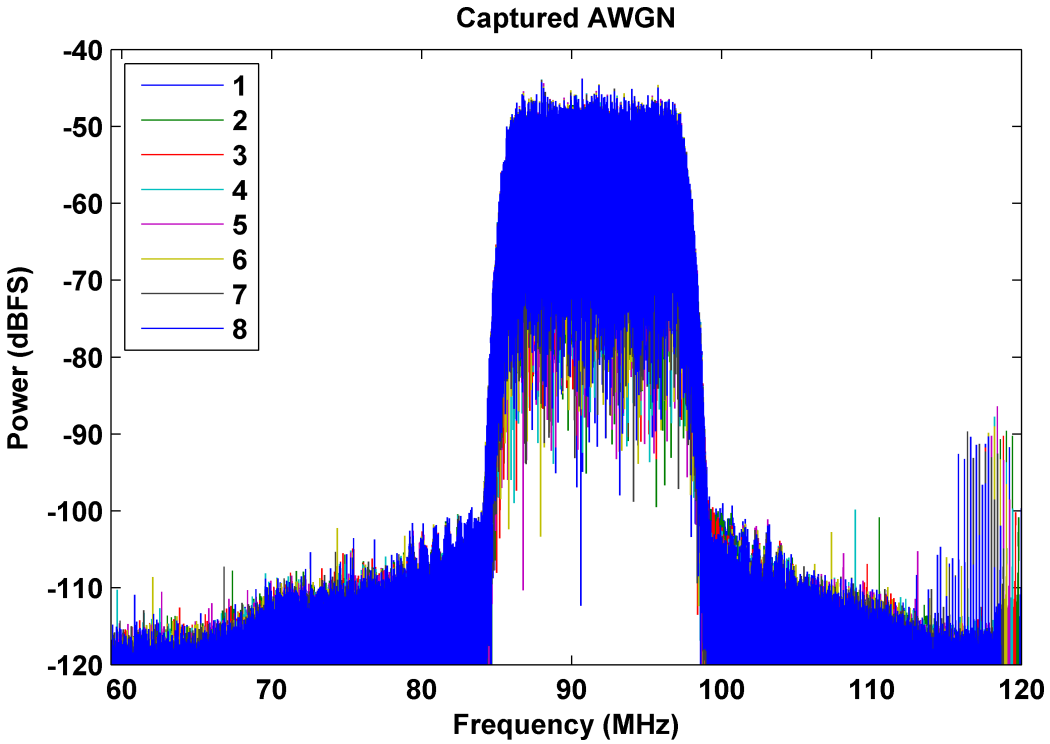

Figure 6.22: The sampled signal appears very similar when plotted in the second Nyquist zone as expected. Each clock is offset from the previous channel by 200 kHz. There is insufficient isolation between clocks, so large spurs occur on the right hand side of the spectrum.

in the center of the band appears similar between the eight channels, with small differences due to the different sampling rates.

The spurs in the frequency range 115-120 MHz of Fig. 6.22 arose due to insufficient isolation between the clock lines, which resulted in significant crosstalk between them. Harmonics of the clocks, which may be significant on clock signals, also appear in the spectrum due to insufficient isolation. The crosstalk is a limitation of our particular test bed and is not inherent in the decorrelation technique; however, future implementations of this technique must ensure sufficient

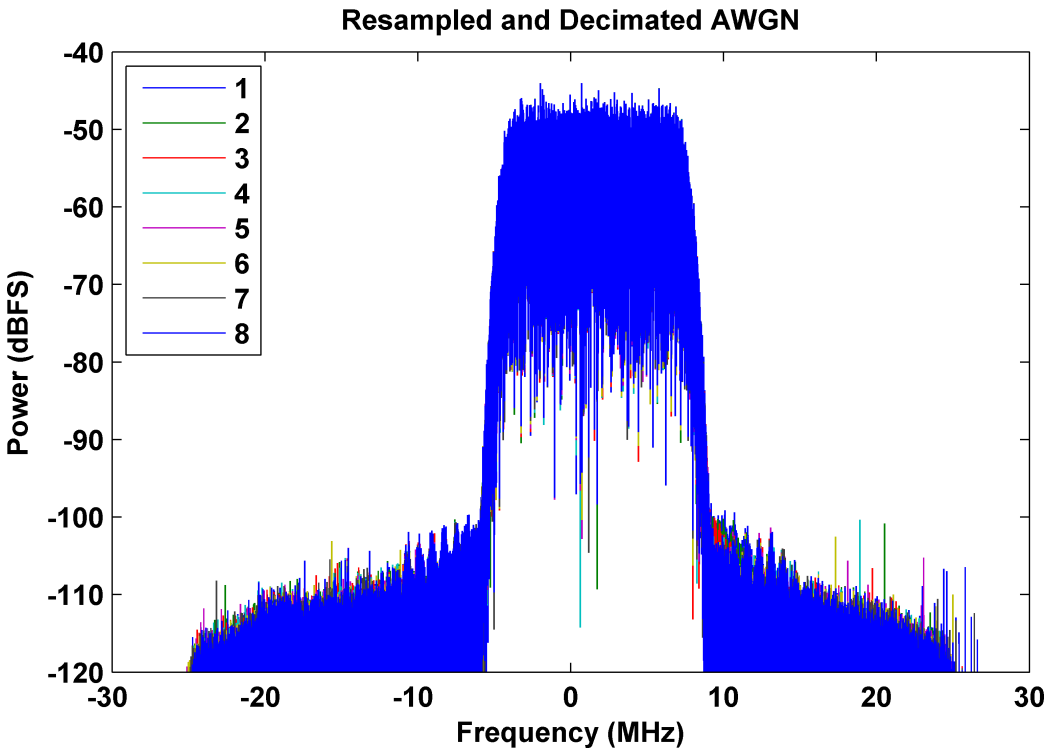

Figure 6.23: Captured signals after downconversion and resampling. The AWGN signals are well correlated in the frequency domain.

clock isolation.

Following data capture, I digitally downconverted the recorded signal to complex baseband (using 90 MHz as the center frequency). I resampled the signal to a common 60 MHz sampling rate. Finally, I multiplied each channel by a single complex number to remove the gain and phase differences caused by the Wilkinson power splitter. Figures 6.23 and 6.24 show that the AWGN is correlated across all eight channels in both the frequency and time domains. Clearly, the fundamental signal was correlated after sampling at different rates.

In order to assess the efficacy of clock offsets on harmonic decorrelation, I changed the input signal to a sinusoid with a frequency of about 94.6 MHz at full-

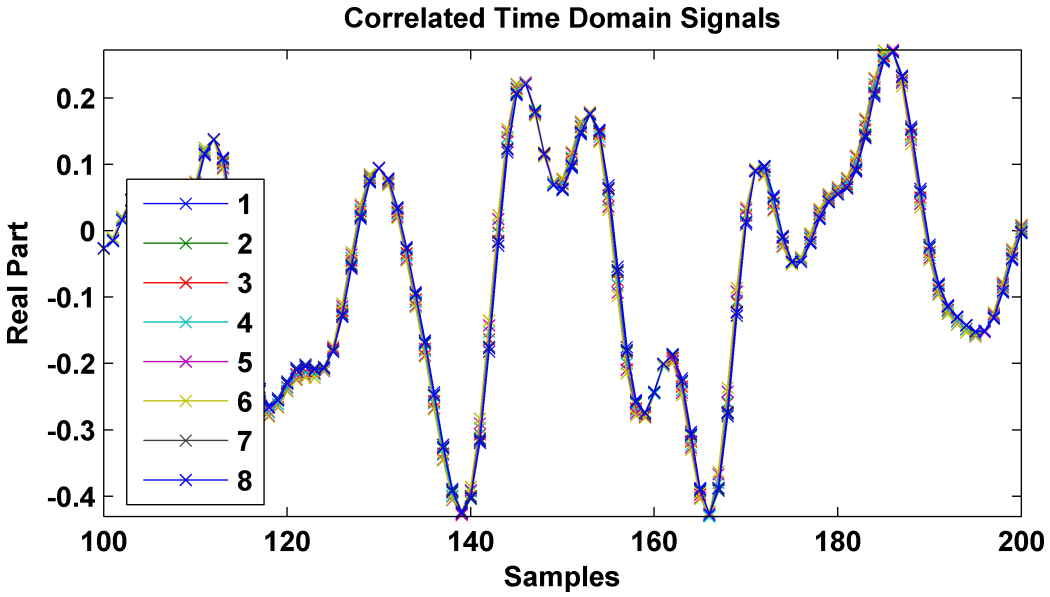

Figure 6.24: Real part of the eight captured signals after downconversion and resampling. The excellent overlap indicates that the signals are well correlated in the time domain.

scale power. I captured this signal on four channels, with sampling clock rates of 119.7, 119.8, 119.9, and 120.0 MHz. Fig. 6.25 shows the signals prior to realignment. The spurs induced by clock crosstalk are more noticeable with a sinusoidal input. The spurs are a limitation of the test bed and should be disregarded in this analysis.

After realignment, the harmonics are aliased to different frequencies. In this case, the aliased second harmonics are located, after digital downconversion, at -20.8, -20.7, -20.6, -20.5 MHz, as shown in Fig. 6.26.

Clock offsets cause aliased harmonics to appear at different frequencies and, therefore, do not sum. I_k is approximately M^2 and the same improvement is achieved as for the frequency offsets technique. The clock offset approach has

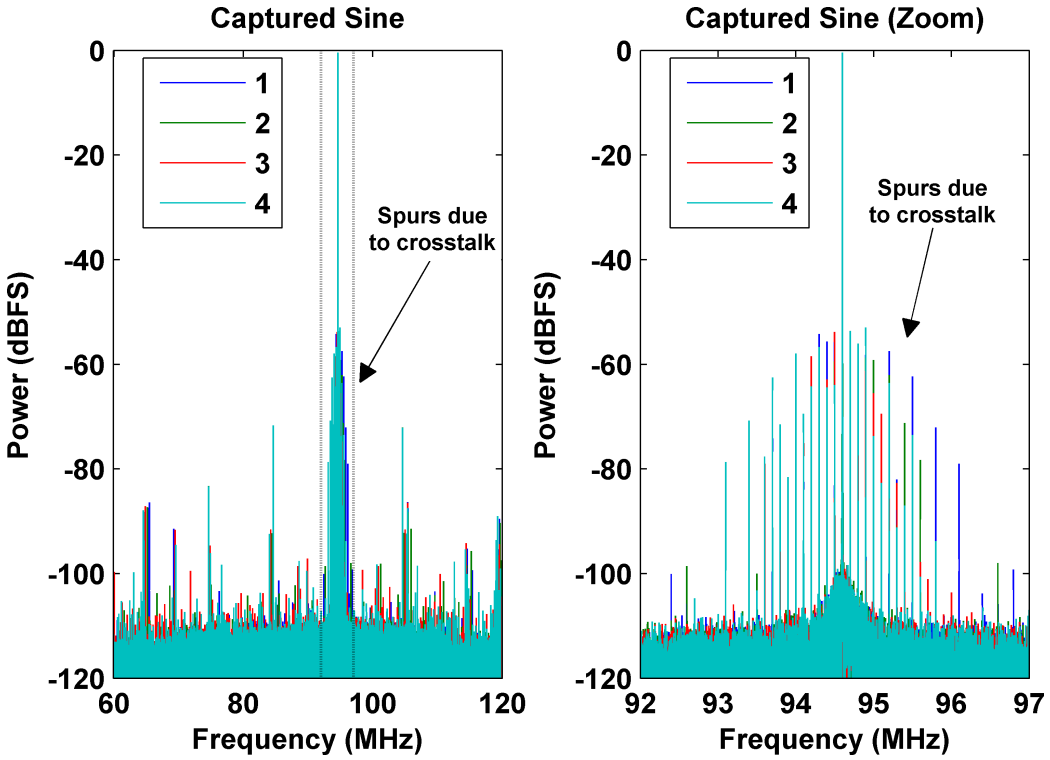

Figure 6.25: The captured sinusoidal input is correlated when plotted in the second Nyquist zone. Insufficient clock isolation cause the series of spurs around the signal.

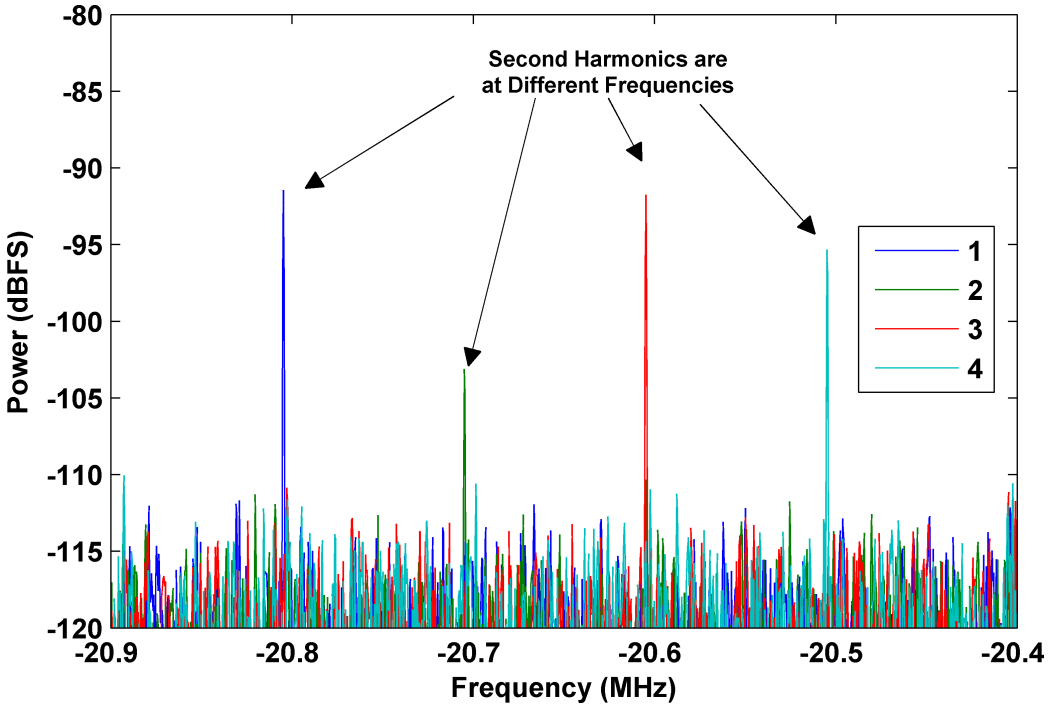

Figure 6.26: Plot of the second harmonics from each of the four channels following down-conversion and resampling. For the sampling frequencies chosen, the resulting second harmonics are offset by 100 kHz.

the benefit of not requiring a mixer and being appropriate for a wider range of systems. The technical challenges; however, lay in providing sufficient clock isolation and designing an appropriate resampler.

6.5 Summary and Conclusion

In this paper, I have identified the key sources of harmonic generation in an ADC and shown through modeling and measurements that the harmonics in a parallel ADC array are largely, although not fully, correlated. In addition, I determined that the second and third harmonics generally have the highest power and are more likely than other harmonics to be correlated, indicating that efforts to improve system performance through harmonic decorrelation should focus on low-order harmonics.

In order to decorrelate those harmonics, I first implemented the phase randomization approach first proposed by Howard *et al.* [18]. I confirmed that phase randomization reduces the correlation as expected, and that the harmonic voltage gain follows a Rayleigh distribution. This statistical behavior causes phase randomization to be less effective for small arrays than the other techniques. As discussed in [18], there is a reasonable probability of strong correlation between channels after applying phase randomization, which may increase the total correlation coefficient by about 8 dB above M for all array sizes. I measured a harmonic decorrelation value I_k as high as -4 dB, even though the mean was approximately -12 dB (M^{-1} for our 16-channel test bed). System designers must consider this

statistical behavior in a design that uses phase randomization or cancellation.

I then extended the phase randomization approach by introducing a phase cancellation technique to reduce the largest correlated harmonics. This improved the SFDR in both cases tested compared to phase randomization only. However, if the Nyquist zone of the harmonics changes compared to the training frequency, the effectiveness of the cancellation decreases. Phase cancellation provides a technique to overcome the strong correlation between channels for particular harmonics. Phase cancellation adds minimal complexity to phase randomization and yields significant improvements to SFDR compared to phase randomization, so there are few reasons not to implement this technique. As a result, I recommend using phase cancellation over phase randomization in all cases.

Future work in this area could investigate implementing phase randomization and phase cancellation techniques on the clock rather than the input signal via a local oscillator. I believe that these techniques should work when applied to the clock only and enable the application of phase decorrelation techniques to systems without mixers. The focus of this paper was ADC arrays; however, these techniques may be applied to many analog components in parallel.

Finally, I demonstrated that frequency and clock offsets induce frequency spreading of the channel harmonics, such that the spurs are no longer at the same frequency. As a result these harmonics do not sum, and the SFDR is increased by M^2 as opposed to an average of M for phase decorrelation techniques. Clock offsets do not require a mixer and are, therefore, more appropriate for a wider variety of systems, such as direct sampling systems. Frequency and clock offsets are

more complex and potentially costly than phase randomization and cancellation, since different LO and clock frequencies are required. While these techniques provide a further improvement in SFDR compared to phase decorrelation, they are most appropriate when harmonics are a significant concern and the improvements provided by the simpler phase-only techniques are insufficient.

Table 6.1 provides a summary of the measured SFDR for each decorrelation technique. All four techniques provide a clear SFDR improvement over that resulting from the inherent correlation of harmonics. The techniques may be combined to tailor the level of harmonic decorrelation. If a total SFDR improvement of $4M$ were required, for example, four unique frequency or clock offsets could be used in conjunction with phase randomization or cancellation to achieve the total improvement. The four techniques represent a "toolbox", giving system designers the ability to tailor their cost, complexity, and dynamic range improvement to suit system requirements.

Table 6.1: Measured SFDR for Each Technique

Decorrelation Technique	SFDR	Improvement over Fully Correlated
No Decorrelation (Fully Correlated)	89.1 dB	n/a
No Decorrelation	91.2 dB	2.1 dB
Phase Randomization Set 1	101.5 dB	12.4 dB
Phase Randomization Set 2	95.5 dB	6.4 dB
Phase Cancellation Set 1 (97.6 MHz) *	103.9 dB	14.8 dB
Phase Cancellation Set 1 (91.64 MHz)	104.0 dB	14.9 dB
Phase Cancellation Set 1 (86.64 MHz)	99.5 dB	10.4 dB
Phase Cancellation Set 2 (97.6 MHz) *	103.4 dB	14.3 dB
Phase Cancellation Set 2 (91.64 MHz)	99.3 dB	10.2 dB
Phase Cancellation Set 2 (86.64 MHz)	96.2 dB	7.1 dB
Frequency Offsets	$\approx 85 + 24.1$ dB	19 dB
Clock Offsets	$\approx 92 + 24.1$ dB	26.1 dB

* Training frequency

Chapter 7

Summary and Discussion

I developed a 16-channel testbed to investigate the partial correlation of noise and harmonics in parallel ADC arrays. I successfully achieved my four design goals.

- Large number of channels
- Low noise and spur measurement system
- Excellent signal correlation
- Excellent isolation between channels

The test bed had a large number of channels by design. I successfully measured an average correlation coefficient across 16 channels of 0.05. The signals were very well correlated between channels, allowing me to successfully investigate harmonic correlation with signals aligned to 170 μrad. The signal source noise was lower than the ADC noise by design and the DDS harmonics were mostly filtered from the ADC input. The remaining harmonics are separable from the ADC harmonics with only one of the first 100 harmonics overlapping. After several key hardware modifications, the ADC's digital buffers were brought to a very low level and the channels had excellent isolation.

I verified that the thermal noise is completely uncorrelated, as expected. I then demonstrated that the sampling noise from a common clock is completely

correlated. Phase randomization (phase cancellation is a variant of phase randomization) and frequency offsets are capable of reducing the correlated noise in half. This can lead to significant cost savings in many applications due to expense of high performance clocks.

Next, I have identified the key sources of harmonic generation in an ADC and shown through modeling and measurements quantizer harmonics are, at most, partially correlated; however, harmonics from the sampler are largely correlated. The sampler and quantizer harmonics are largest for the second and third harmonics. From these observations, I determined that efforts to improve system performance through harmonic decorrelation should focus on low order harmonics.

In order to decorrelate those harmonics, I implemented a phase randomization approach first proposed by Howard *et al.* I demonstrated that phase randomization reduces the correlation as expected, and I confirmed that the total correlation coefficient is consistent with Rayleigh distribution statistics. It is important to note that the Rayleigh distribution includes a finite probability of significant correlation. I measured I_k as high as -4 dB, even thought the mean was approximately 12 dB, or M^{-1}. System designers must consider this statistical behavior in a design that uses phase randomization or cancellation.

Furthermore, I extended the phase randomization approach by introducing a phase cancellation technique to reduce the largest correlated harmonics. This improved the SFDR in both cases tested compared to phase randomization. However, if the Nyquist zone of the harmonics changes compared to the training frequency,

the effectiveness of the cancellation is less effective. Phase cancellation adds minimal complexity and yields significant improvements to SFDR. As a result, phase cancellation should be chosen over phase randomization in actual implementation.

Finally, I demonstrated that frequency and clock offsets induce frequency spreading of the channel harmonics, such that the spurs are no longer at the same frequency. As a result, the harmonics do not sum, and the SFDR is increased by M^2. Clock offsets do not require a mixer and are, therefore, more appropriate for a wider variety of systems, such as direct sampling systems, although clock offsets may still be used in systems with mixers.

Table 6.1 provides a summary of the measured SFDR for each decorrelation technique. All four techniques provide a clear SFDR range improvement over no decorrelation. Phase cancellation has low overhead for implementation relative to randomization, so there are few reasons not to implement this technique. Frequency and clock offsets are more complex (and potentially costly), since different LO or clock frequencies must be generated. While they provide further improvement in SFDR, they are most appropriate when harmonics are a significant concern and the improvements provided by the simpler phase decorrelation approaches are not sufficient. The benefits increase for frequency and clock offsets as the number of channels increases, but the complexity increases at the same rate. The four decorrelation techniques described here all provide substantial SFDR improvement over implementations in which no decorrelation is attempted.

7.1 Suggestions for Future Work

This dissertation outlines a complete "toolbox", which enables the decorrelation of harmonics for various systems. This work did not address sources of other spurs and distortion, the worst of which is often intermodulation distortion. Rabideau and Howard discussed the use of frequency-dependent phase offsets (dispersion) to phase decorrelate the intermodulation distortion [18], but the required dispersion increases as the bandwidth decreases. They further investigate nonlinear correction to reduce intermodulation [19]. Many others have investigated this area as well [98, 99, 100, 101], but, as far as I know, no clear solution has been developed. This remains an interesting area of research.

There is a loose connection between sampling distortion and sampling noise. The sampling distortion is proportional to the clock fall time, which increases with bandwidth if the clock is harmonically rich. However, the sampling noise also increases with the bandwidth, so there is a trade-off in the design of sample-and-hold circuits. Little research has been conducted in this area. There is the potential for advanced filter designs to allow both rich harmonics and block the noise using comb filters.

More directly, there is a strong relationship between the thermal noise, input bandwidth, and sampler distortion. The thermal noise and input bandwidth are inversely proportional to the input sampling capacitance, while the sampler distortion is proportional to the input capacitance. More research is necessary to overcome these fundamental limitations. Finally, additional investigations should

be conducted on the modifications to the clock to provide phase cancellation and randomization.

Appendix A

Power of BLGN through Third-Order Nonlinearity

The power of a BLGN signal through a third-order nonlinearity $\mathrm{E}\left[(x^3)^2\right]$ has not previously been determined and is required for (4.21). In general, the power of an arbitrary cubed signal is not simply the signal power cubed, $\mathrm{E}\left[(x^3)^2\right] \neq \mathrm{E}\left[(x^2)\right]^3$. The power spectral density (PSD) for a Gaussian noise source filtered from DC to bandwidth B through a third-order nonlinearity x^3 in bandwidth B is [102]

$$PSD(f) = N^3\left(\frac{27}{2}B^2 - \frac{3}{2}f^2\right) \tag{A.1}$$

where N is the PSD of the input noise source. We refer to this as the "lowpass" case and it shown schematically in Fig. A.1a. We describe the "lowpass" case because it is known in the literature, while the "bandpass " case is not. The total noise power in bandwidth B is found by integrating the PSD from 0 to B. The resulting total output power is $13P_{\mathrm{in}}^3$ with $P_{\mathrm{in}} = NB$.

If the BLGN measurement signal is centered at a carrier frequency that is

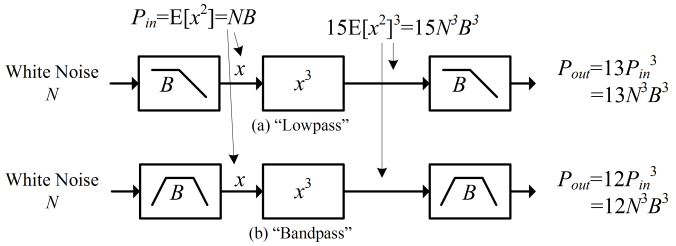

Figure A.1: "Lowpass" and "bandpass" Gaussian noise through a third-order nonlinearity.

much greater than B, as is the case here, then when the noise passes through the third-order nonlinearity, some of its energy occurs in the third harmonic. We refer to this as the "bandpass" case and depict it schematically in Fig. A.1b. Through numerical simulations, we determined that the total power for the BLGN measurement signal through a third-order nonlinearity is $12P_{\text{in}}^3$. The coefficient depends on the signal characteristics. For example, the power for an LFM signal through a third-order nonlinearity is $2.5P_{\text{in}}^3$.

Appendix B

Matlab Code to Determine b_{opt}

This appendix describes the Matlab code to determine b_{opt}. The basic algorithm forms N matrices, where the first matrix is one dimensional, the second is two dimensional, and so on, up to an N-dimensional matrix. The largest value of N is $M/2$, so for large ADC arrays this may be significant amount of data. In the code below, the maximum value of N is 4, although, clearly, it could be expanded to higher dimensions.

Each matrix is first initialized to ∞. Then, for each element of the matrix the ratio 6.4 is calculated, where the elements of b are the indices of the matrix. The diagonals, where one index is equal to another are ignored because the values have already been calculated in the previous array. From all M matrices, the minimum value is calculated and returned as b_{opt}.

```
function [best_channel total_min]= find_best_channel(a_km, N)

M = length(a_km);
```

```
if nargin < 2
    N = 1;
end

for n = 1:N
  switch n
    case 1
      for m = 1:M
        not_m = find_not_m(m,M);
        amp_m(m) = abs(a_km(m));
        amp_not_m(m) = abs(sum(a_km(not_m)));
      end
      ratio = max([amp_m;amp_not_m])./min([amp_m;amp_not_m]);
      [min_value(1) index1] = super_min(ratio);
    case 2
ratio = inf(M,M);
      for m1 = 1:M
       for m2 = 1:M
          m = [m1 m2];
          if length(unique(m)) == length(m)
         not_m = find_not_m(m,M);
            amp_m = abs(sum(a_km(m)));
            amp_not_m = abs(sum(a_km(not_m)));
            ratio(m1,m2) = max([amp_m;amp_not_m])./...
             min([amp_m;amp_not_m]);
          end
        end
      end
      [min_value(2) index2] = super_min(ratio);

case 3
     ratio = inf(M,M,M);
      for m1 = 1:M
       for m2 = 1:M
         for m3 = 1:M
           m = [m1 m2 m3];
            if length(unique(m)) == length(m)
             not_m = find_not_m(m,M);
              amp_m = abs(sum(a_km(m)));
              amp_not_m = abs(sum(a_km(not_m)));
              ratio(m1,m2,m3) = max([amp_m;amp_not_m])./...
               min([amp_m;amp_not_m]);
            end
          end
```

```
        end
       end
       [min_value(3) index3] = super_min(ratio);

case 4
     ratio = inf(M,M,M,M);
        for m1 = 1:M
          for m2 = 1:M
            for m3 = 1:M
              for m4 = 1:M
                m = [m1 m2 m3 m4];
                if length(unique(m)) == length(m)
                  not_m = find_not_m(m,M);
                  amp_m = abs(sum(a_km(m)));
                  amp_not_m = abs(sum(a_km(not_m)));
                  ratio(m1,m2,m3,m4) = max([amp_m;amp_not_m])./...
                   min([amp_m;amp_not_m]);
                end
              end
end
         end
        end
        [min_value(4) index4] = super_min(ratio);
  end
end

[total_min grouping] = min(min_value);
switch grouping
    case 1
        best_channel = index1;
    case 2
        best_channel = index2;
    case 3
        best_channel = index3;
    case 4
        best_channel = index4;
end
```

The function above, `find_best_channel`, calls two other functions, `find_not_m` and `super_min`. These functions are listed below for completeness.

```
function not_m = find_not_m(m,M)
% Returns the set of channels not in m
```

```
possible_m = 1:16;

N = length(m);

temp = m(1) == possible_m;
for n=2:N
temp2 = m(n) == possible_m;
    temp = or(temp, temp2);
end

not_m = sort(unique(possible_m.* ~temp));
not_m = not_m(2:end);
```

The function `super_min` is a recursive implementation of Matlab's built-in function `min` to work on multi-dimensional matrices at the same time instead of over a single dimension.

```
function [a r] = super_min(a)
% PROTOTYPE [minimum index] = super_min(a)
% Returns the minimum and index for
%   a multidimensional array, up to DIM =4;

N = length(size(a));

if N == 2
    temp = size(a);
    if temp(1) == 1
        N = 1;
        a = a';
    elseif temp(2) == 1
        N=1;
    end
end

for n = N:-1:1
    [a,I] = min(a,[],n);
    Index.(['I' num2str(n)]) = I;
end

r = Index.('I1');
for n = 2:N
```

```
    switch length(r)
        case 1
            r = [r Index.(['I' num2str(n)])(r)];
        case 2
            r = [r Index.(['I' num2str(n)])(r(1),r(2))];
        case 3
            r = [r Index.(['I' num2str(n)])(r(1),r(2),r(3))];
        case 4
            r = [r Index.(['I' num2str(n)])(r(1),r(2),r(3),r(4))];
    end
end
```

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