ABSTRACT

Title of dissertation: A NON-INVASIVE ELECTROSTATIC GATING METHOD FOR PROBING TWO-DIMENSIONAL ELECTRON SYSTEMS ON PRISTINE, CHEMICALLY-TERMINATED, INTRINSIC SI SURFACES

Luke Daniel Robertson, Doctor of Philosophy, 2021

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We have demonstrated a new and effective method for the non-invasive electrostatic gating of pristine, chemically-terminated, intrinsic Si surfaces. This was achieved using a silicon-on-insulator (SOI) device design in which two chips, an SOI gate chip and a pristine, Si chip, are Van der Waals bonded to one another. In this architecture, all harsh device processing is relegated to a single SOI chip which is host to all of the electrical components, including the ohmic contacts and the electrostatic gates. The pristine Si chip is bonded to the ohmic contacts on the SOI chip, while the electrostatic gates on the SOI chip are separated from the Si surface by vacuum. This novel design allows for the Si chip to remain free of dopants or metals that are traditionally fabricated directly onto the surface, thus enabling the Si chip to retain its native properties and remain compatible with a wide variety of existing surface preparation techniques, including wet chemical processing and dry ultra-high vacuum processing.

Using our non-invasive architecture, we were able to electrostatically gate a hydrogen-terminated Si(111) (H-Si(111)) surface. Transport measurements were performed on a

global-gate induced two-dimensional electron system (2DES) on the H-Si(111) surface via electrical access through the ohmic contacts, while the depletion gates confined the 2DES to a Van der Pauw geometry.

We also extended the reach of our devices to probe – for the first time – 2D electron transport on a pristine, intrinsic iodine-terminated Si(111) (I-Si(111)) surface. To date, no other 2D magnetotransport measurements have been realized on I-Si(111) surfaces due in large part to the difficulties surrounding the electrostatic gating of these fragile surfaces.

This novel architecture is not without its own set of challenges. In particular, the series contact resistance that arises at the SOI-Si bond edge, especially at low temperatures, is significant. The current injection across a Van der Waals bond is an inherent feature in our architecture due to the placement of the ohmic contacts on the SOI piece. I developed a mathematical framework for understanding this current injection in our devices, and presented device modifications for decreasing the contact resistance.

A NON-INVASIVE ELECTROSTATIC GATING METHOD FOR PROBING TWO-DIMENSIONAL ELECTRON SYSTEMS ON PRISTINE, CHEMICALLY-TERMINATED, INTRINSIC SI SURFACES

by

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Preface

This dissertation details two primary experiments that I conducted in the Kane Lab, and is intended to serve a two-fold purpose: first, to provide a full description of these experiments, and second, to equip the reader with all necessary tools and information to continue these experiments.

"Do. Or do not. There is no try."

-Yoda

Dedication

To Piyali, my muse.

Acknowledgments

There are myriad people deserving of my gratitude and appreciation, and indeed, too many to name here. My focus for this section is to show my appreciation for those who have had a direct impact on my research and the writing of this dissertation, and to those who have encouraged and inspired me along the way.

First, I want to thank Bruce for guiding my research during my time at LPS. It has been an honor and a privilege to have had the opportunity to work in your lab and to learn under your mentorship. Thank you for teaching me the discipline of experiment.

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To my parents, Dan and Susan, thank you for your unwavering love and support, not only during my time in graduate school but throughout my entire life. I'm truly grateful for all you do and I love you both! Mom – thank you for your thoughtful feedback on my thesis.

To my sister, Anna, and brother-in-law, John, you guys are awesome and an inspiration, and you have some pretty cool kids as well. To my niece, Katie, the world is your oyster, and to my newborn nephew, Alex, I look forward to watching you grow! Anna – thank you for your thoughtful feedback on my thesis.

To my brother, Ben, and sister-in-law, Clara, you guys are also awesome. Thank you both for your support and encouragement throughout my graduate adventures. Ben – thank you for your thoughtful feedback on my thesis.

Of course, I cannot forget my dear friends who actually trudged along side me in my graduate adventures. To Mina, Davy, Prasoon, Amit, John human, and John cat, thank you for helping me prepare for my defense and for making graduate school an unforgettable experience. I am truly grateful for our friendships, and I couldn't have done it without you

all!

To my LPS office mates, Joyce, Shavi, Wan-Ting, and Joe, thank you for all your help over the years and for always lending a listening ear.

To Raj and Kakali, I want to thank you for welcoming me into your family and for your constant support and encouragement throughout my time in graduate school. I cherish the memories I've made with the Das family over the years, and I look forward to making many more.

To Raj and Karishma, it's been awesome getting to know you both over the years, and I am honored to call you both my brother and sister. Thank you for your support and encouragement.

Getting back to my roots, I want to give a shout out to my 828 Boone crew. To Layla, David, Ben, and Chris, you all have been there since the beginning and I will always treasure our friendships. Layla – thank you for all your help and support over the years both here and abroad, and thank you for helping me prepare for my defense.

And lest I forget, none of my work could have gotten done without the help of the first-rate LPS cleanroom staff. To Toby, Doug, Jim, Paul, Steve, Jason, and Curt, I'm forever grateful for all of your assistance over the years and for the many chats we've had that were a welcome distraction from research.

To Warren, Dan, Basu, and other LPS crew members who've helped me along the way, thank you for sharing your wisdom with me. And to the machine shop, Don, Paul, and Ruben, thank you for always delivering quality and timely work.

To Jonas and Greg, you two are the powerhouses of LPS. Thank you both for running the facility like a well-oiled machine and always looking out for us graduate students.

Finally, I want to express my deepest appreciation and say an extra special thank to my best friend, Piyali. You've been there for me throughout this journey, and even during the toughest parts of graduate school you always encouraged me to keep going. You're the best person I know and you inspire me each day to be my best self, too. I love you always.

List of Symbols and Acronyms

Fundamental Constants

c	Speed of light in vacuum	$299\,792\,458\ \mathrm{m \cdot s^{-1}}$
e	Elementary charge	$1.602\,176\,634 \times 10^{-19}\ \mathrm{C}$
ε_0	Vacuum electric permittivity	$8.854\,187\,8128(13) \times 10^{-12}\ \mathrm{F \cdot m^{-1}}$
h	Planck's constant	$6.626\,070\,15 \times 10^{-34}\ \mathrm{J \cdot s}$
$\hbar$	Reduced Planck's constant	$1.054\,571\,817... \times 10^{-34}\ \mathrm{J \cdot s}$
k_B	Boltzmann's constant	$1.380\,649 \times 10^{-23}\ \mathrm{J \cdot K^{-1}}$
m_e	Electron rest mass	$9.109\,383\,7015(28) \times 10^{-31}\ \mathrm{kg}$
μ_B	Bohr magneton	$9.274\,010\,0783(28) \times 10^{-24}\ \mathrm{J \cdot T^{-1}}$

Acronyms

2DES Two-dimensional electron system

2DHS Two-dimensional hole system

AC Alternating current

AFM Atmoic-force microscopy

BOE Buffered oxide etch

BOX Buried oxide

DC Direct current

DIP Dual in-line package

DIW Deionized water

DoS Density of states

FCC Face-centered cubic

FE Field emission

FET Field-effect transistor

FQHE Fractional quantum Hall effect

FZ Float-zone

HF Hydrofluoric acid

HMET High-mobility electron transistor

H-Si(111) Hydrogen-terminated Si(111)

IPA Isopropyl alcohol

IQHE Integer quantum Hall effect

I-Si(111) Iodine-terminated Si(111)

IVC Inner vacuum can

MBE Molecular-beam epitaxy

MOSFET Metal-oxide-semiconductor field-effect transistor

PDG Proximity depletion gate

PEG Proximity enhancement gate

PPC Parallel-plate capacitor

QAHE Quatum anomolous Hall effect

QD Quantum dot

RCA Radio Corporation of America

RIE Reactive-ion etch

SB Schottky barrier

SEM Scanning-electron microscopy

SHE Spin Hall effect

SOI Silicon-on-insulator

SRD Spin-rinse-dry

STM Scanning-tunneling microscopy

TI Topological insulator

TMDC Transition metal dichalcogenide

UHV Ultra-high vacuum

VdP Van der Pauw

WKB Wentzel–Kramers–Brillouin

XPS X-ray photoelectron spectroscopy

X-Si(111) Halogen-terminated Si(111)

Table of Contents

Chapter 1: Introduction

This dissertation details the two main experiments that I conducted in the Kane lab. I intend to provide a full description of these experiments, and sufficiently equip the reader with all the necessary tools to continue these and similar experiments. The first experiment concerns the development of a fully non-invasive silicon-on-insulator (SOI) gating method for probing two-dimensional electron systems (2DESs) on hydrogen-terminated Si(111) (H-Si(111)) surfaces. This experiment involved the conception, design, fabrication, realization, and demonstration of a device comprising a pristine, intrinsic H-Si(111) chip, which hosted the 2DES, and a non-invasive SOI gate chip, which housed all electrical components. In the second experiment, I attempted to measure 2D electron transport on iodine-terminated Si(111) (I-Si(111)) surfaces using our non-invasive SOI gating architecture.

1.1 Background and motivation

The import of the 2DES cannot be overstated; it is the primary ingredient of the metal-oxide-semiconductor field-effect transistor (MOSFET), which permeates all modern electronics and microprocessors [1]. It has also been a test-bed for some of the most profound discoveries in condensed matter physics [2, 3]. Because of this, 2DESs are a rich playground not only for technological applications but also for the investigation of new and emergent physics. In the following sections, I will provide context for my research and highlight the central motivation for this work, which is to realize a new and productive way to probe 2D electron systems on chemically-passivated, intrinsic Si surfaces. Figure 1.1

illustrates a schematic diagram of the non-invasive SOI-based gating architecture that will be the centerpiece for the rest of the work described in this dissertation.

1.1.1 Silicon surface terminations

One of the remarkable properties of silicon is that its surface can be terminated in a number of ways that passivate the electronic surface states [4–9] and allow the surface to retain the band structure of the bulk [10–12]. Essentially, the bulk properties of Si are mapped onto the surface, and the 2DES can be described within this 3D projection onto the 2D surface (see Ch. 2). The most common surface passivation for Si is stoichiometric silicon-oxide, SiO_2, which can be grown thermally in a tube furnace [13, 14] or deposited using chemical vapor deposition (CVD) techniques [15]. Thermally grown SiO_2 is the primary passivating agent in MOSFETs due to its extraordinarily uniform characteristics. Indeed, this fortuitous ability to grow high-quality SiO_2 at scale is *the* primary reason why Si still dominates the microprocessor industry today [16, 17]. Of course, there exist other surface terminations for passivating the surface of Si, including hydrogen [18–24], halogens (Cl, Br, I) [25–29], various oxides [30–32], functional groups for complex chemistry [33–39], and even gold [40]. Furthermore, there exist many different methods for terminating these surfaces, including wet chemical treatments [41–46] and dry ultra-high vacuum (UHV) techniques [47, 48]. These aspects of Si are central to this thesis and will be discussed in greater detail in Ch. 3 (hydrogen, wet chemistry) and Ch. 6 (iodine, dry UHV). Indeed, because of the unique structure of our device architecture (see Ch. 3), it is of paramount importance to ensure that the Si surface is chemically passivated in order for a good 2DES to exist on the surface. For this work, I was primarily interested in the Si(111) surface, in which each Si atom on the crystal facet possesses one dangling bond that is monovalently passivated with either atomic hydrogen or atomic iodine (see Fig. 1.2). In Ch. 7, I will discuss going beyond the Si(111) surface and how our device architecture could be used to probe a variety of Si surfaces with different orientations and

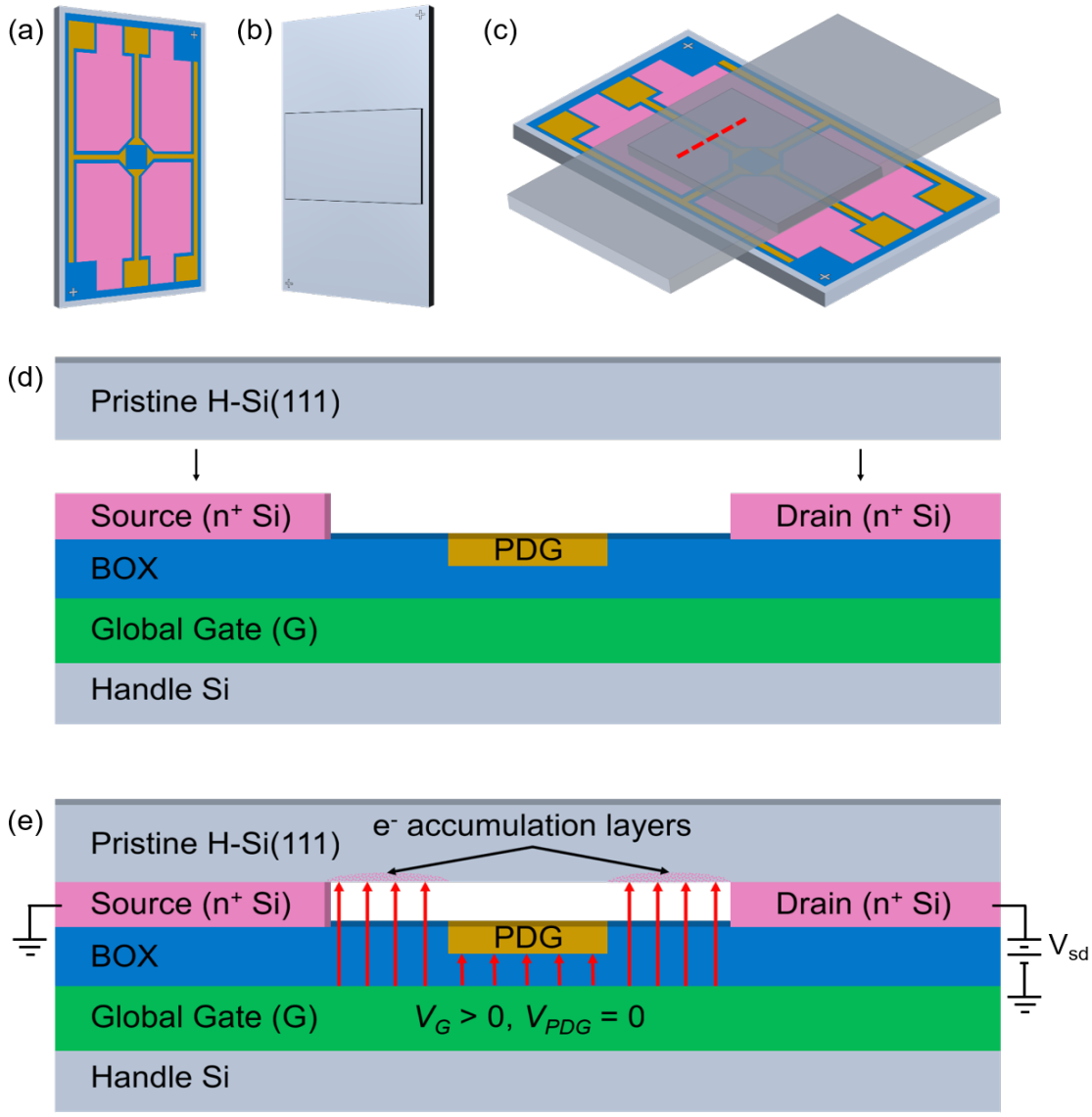

Figure 1.1: Illustration of the four-terminal device architecture central to this work: (a) the SOI piece housing all electrical components, (b) the pristine, chemically-terminated, intrinsic Si piece, (c) the Van der Waals bonded device, (d) a cross-sectional view of the unbonded device along the red dashed line in (c), (e) a cross-sectional view of the bonded device along the red dashed line in (c) with a crude wiring scheme. Ohmic contacts (n^+ Si) are shown in pink, buried oxide (BOX) in blue, global gate in green, PDGs in gold, and Si in gray. A forward bias applied to the global gate results in electron accumulation on the H-Si(111) surface, except where the grounded, vacuum-separated PDGs block the E-field (solid red arrows), depleting the local region.

different surface terminations.

Recent progress in surface preparation techniques make Si surfaces an attractive candidate for hosting 2DESs with exotic properties, especially those with enhanced spin-orbit interactions and topologically insulating behavior [49–54]. In particular, experiments have been successful in characterizing halogen (X: Cl, Br, I) terminated Si (X-Si) surfaces prepared with both established UHV techniques and novel wet chemical treatments [45]. These surface characterizations have to date been limited to topographical and spectroscopic analysis, as well as theoretical modeling. Some of these analyses have explored the electronic structure of X-Si surfaces [55, 56] while others have focused on halogen surface coverage and Si-X bond energies to understand the role of halogens as surface ligands for functional chemistry [57]. For example, Butera et al. have characterized X-Si surfaces prepared in both solution and UHV using scanning-tunneling microscopy (STM) and X-ray photoelectron spectroscopy (XPS). These analyses reveal partial and full monolayer coverage of the surface with minimal oxygen and carbon contamination [58]. Their primary efforts have been focused towards facilitating the selective adsorption of acceptor-dopant precursors, BCl_3 and $AlCl_3$, for acceptor-based devices, using halogens as effective mediators for wet chemistry surface functionalization [59, 60]. Additionally, they have reported progress in Cl-based STM lithography [61]; a natural extension of the established technique of hydrogen-based STM lithography [62–64].

Over the past year, the Kane group has partnered with the Butera group in order to consolidate their halogen surface preparation techniques with our non-invasive gating method. The goal of this collaboration is to extend the capabilities of our devices beyond H-Si(111) surfaces and provide a practical experimental procedure to measure 2D transport on these fragile, chemically-terminated Si surfaces. To this end, we have obtained I-Si(111) samples that were first terminated with hydrogen using a wet chemical treatment of ammonium fluoride (NH_4F), then terminated with iodine in UHV through thermally assisted H-I exchange, and then subsequently bonded with our SOI gate chips. In Ch. 6, I will discuss

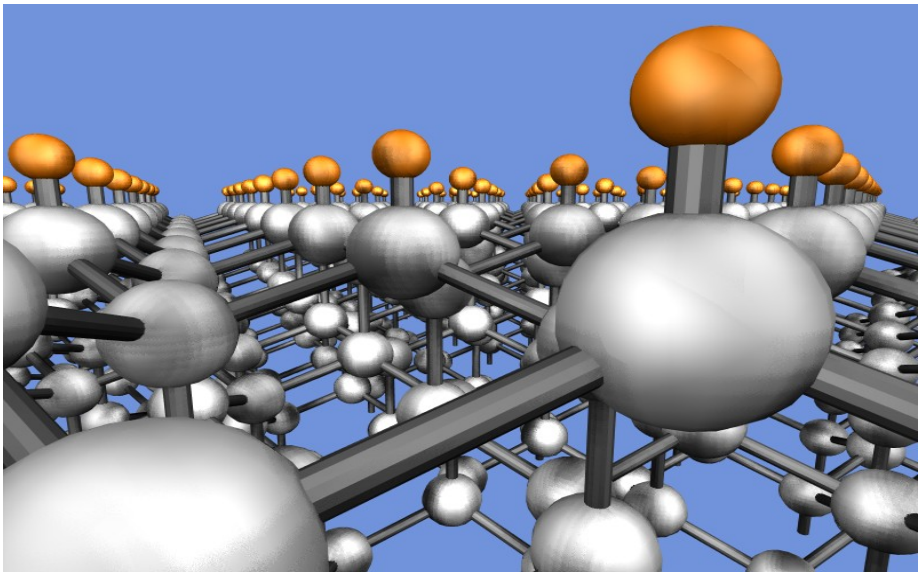

Figure 1.2: Ball-and-stick model of a hydrogen-terminated Si(111) surface. The Si atoms (gray) have a single dangling bond at the (111) surface that can be passivated by hydrogen (orange) or in general any halogen (Cl, Br, I) or univalent functional molecule.

in detail preliminary 2D transport measurements on these samples, as well as some STM and XPS surface analysis results from the Butera group.

1.1.2 Intrinsic silicon surfaces

Intrinsic materials are those which have very low levels of dopant impurities, and thus high carrier lifetimes [65, 66]. They are materials in their most pristine form, and while some impurities are always present, they can be treated as though they are completely undoped. Thanks to the float-zone (FZ) technique, Si processing has advanced to such a degree that intrinsic Si wafers can now be manufactured with residual impurity levels as low as 10^{13} cm^{-3} (or 1 part in 5 billion) [67] making Si a viable intrinsic material to work with. Mathematically, an ideal intrinsic semiconductor is one where the number of free electrons in the material equals the number of free holes, such that $n = p = n_i$, where n_i is

the intrinsic carrier concentration defined by:

$$n_i = \sqrt{N_C N_V} e^{-\frac{E_g}{2k_B T}} \tag{1.1}$$

where N_C and N_V are the density of states in the conduction band and valence band, respectively, and E_g is the band gap of the material. When doping is present (n-type or p-type) the Fermi energy E_F shifts from the intrinsic energy E_i, resulting in a deviation of the concentration of free carriers from the intrinsic value by:

$$n = n_i e^{\frac{E_F - E_i}{k_B T}} \text{ (for electrons)} \tag{1.2}$$

$$p = n_i e^{\frac{E_i - E_F}{k_B T}} \text{ (for holes)} \tag{1.3}$$

leading to the thermal-equilibrium mass action condition, $np = n_i^2$. For Si at 300 K, the intrinsic carrier concentration is $n_i \approx 10^{10}$ cm^{-3}, which means that Si manufacturers can produce Si that has impurity levels about one thousand times higher than the room temperature intrinsic level.

In the absence of surface roughness, the dominant scattering mechanism for electrons on the Si(111) surface at low temperature is due to charged impurity scattering caused by dopants [68]. Thus, the more pure the material, the more this effect is mitigated. Intrinsic Si is of interest not only due to its low defect density and desirable carrier lifetime properties [69], but also due to its compatibility with UHV processing, such as molecular-beam epitaxy (MBE) [70, 71]. UHV surface preparation techniques can take advantage of pristine materials that are free of dopants and other contamination, so intrinsic Si is ideal for the purposes of my work in this dissertation. We would like to keep our Si surfaces completely free of dopants and impurities, since this is the best way to ensure optimal conditions for 2D transport measurements. The caveat, however, is that undoped Si becomes an insulator at low temperature and thus requires some means by which to access

the electrostatically gated 2DES. Typically, this is achieved using dopants or metals fabricated into ohmic contacts. In our case we make electrical contact to the 2DES through the Van der Waals bonding of a pristine Si chip with an SOI gate chip, which hosts all of the electical components, including the ohmic contacts.

1.1.3 2D transport measurements

Despite the recent advances in Si surface termination techniques discussed in § 1.1.1, 2D electron transport measurements on these surfaces are lacking. This is in large part due to the difficulties involved in the electrostatic gating of these ambient-sensitive surfaces without destroying them. As has already been noted, 2DESs exhibit a wealth of physics that has been explored extensively in recent decades [68, 72–76]. Much interest has developed in systems with enhanced spin-orbit coupling [77–92] as well as strongly-correlated interactions [93–96]. Bulk Si and H-Si surfaces on their own possess very weak spin-orbit coupling to electrons, and so in this regard Si is typically not a very interesting material. However, with bulk or surface modification, spin-orbit interactions have been experimentally realized [49–54]. As such, it has been predicted that spin-orbit interactions can be greatly enhanced at the Si surface when it is terminated with heavy halogens. In particular, Si surfaces passivated with iodine [97, 98] are expected to exhibit strong spin-orbit interactions leading to topological phases including the spin Hall effect (SHE) [99] and the quantum anomalous Hall effect (QAHE) [100].

Using our unique, non-invasive SOI gating method, we have successfully gated Si surfaces terminated with iodine and report the first magnetotransport measurements of 2DESs on these surfaces. Our devices were originally conceived as a way to non-invasively gate pristine, intrinsic H-Si(111) surfaces, but we have extended their functionality to include Si surfaces of any chemical preparation, and in particular I-Si(111) surfaces. The key feature of our non-invasive SOI gating design, discussed in Ch. 3, is that the ohmic contacts are contained on the SOI gate chip, which allows for minimal processing of the pristine

Si(111) surface enabling it to retain its native properties. Unlike other non-invasive gating proposals for other pristine materials (e.g. GaAs by Kouwenhoven [101]), our architecture facilitates a method for the non-invasive study of Si surfaces without requiring the placement of dopants or metals on the surface of interest. As has been noted, this allows for broader compatibility with UHV processes in which pristine materials are required. Furthermore, our device architecture allows for the electrostatic gating of any chemically prepared Si surface because all of the gates (both accumulation and depletion gates) are also contained on the SOI gate chip and are separated from the surface by vacuum. Using this approach, I was able to measure 2D transport on intrinsic H-Si(111) surfaces, discussed in Ch. 4, and intrinsic I-Si(111) surfaces, discussed in Ch. 6.

1.1.4 Why silicon?

Silicon is a column IV element with atomic number 14 and a $1s^2 2s^2 2p^6 3s^2 3p^2$ electronic configuration. There are three naturally occurring stable isotopes of Si, ^{28}Si (92.23%), ^{29}Si (4.67%), and ^{30}Si (3.10%), with ^{29}Si being the only isotope with a non-zero nuclear spin, $I = \frac{1}{2}$. As a 3D solid, Si exists in only one stable allotrope and forms a diamond-cubic lattice structure with each atomic site contributing four covalent bonds to nearest neighbor Si atoms. Due to its cubic structure, Si has an isotropic coefficient of thermal expansion which plays a critical role in the ability of our devices to remain Van der Waals bonded during thermal cycling. Si is a semiconductor with an indirect band-gap of 1.1 eV. Thus, at zero Kelvin Si becomes an insulator with all electrons being bound to their respective lattice sites or covalent bonds. At non-zero temperatures, electrons in Si are thermally promoted to the conduction band with the assistance of phonons and contribute to conduction according to the Fermi-Dirac distribution.

The conduction properties of Si (and semiconductors in general) can be manipulated in a number of ways, most commonly through doping and electrostatic gating, which shift the Fermi level either closer to the conduction band (n-type doping) or closer to the valence

band (p-type doping), depending on the dopant species and applied voltages. Because Si is a column IV element, when it is doped with a column V element, such as phosphorous, the pentavalent P forms four covalent bonds with the neighboring Si atoms with one remaining electron occupying a shallow hydrogen-like orbital about the P dopant sitting just below the conduction band. These shallow electrons can be readily donated thermally to the conduction band, thus increasing the number of free negative charge carriers (n-type doping) – hence we call column V elements donors. Likewise, when Si is doped with a column III element, such as boron, the trivalent B forms three covalent bonds with the neighboring Si atoms with a remaining electron vacancy, or hole. The hole can also occupy a shallow hydrogen-like orbital about its B host just above the valence band. These shallow holes readily accept electrons from the valence band, thus increasing the number of free positive charge carriers (p-type doping) – hence we call column III elements acceptors. As a side note: In § 1.1.2, I emphasized the desire to keep dopants *out* of our devices, and while this is certainly true for the intrinsic Si surfaces, we do in fact introduce dopants in our SOI piece to form the ohmic contacts (see Ch. 3). This is indeed one of the great advantages of our device architecture, in that dopants, as well as other harsh processing, can be restricted to the SOI piece while the pristine Si piece remains unscathed.

The behavior I described above applies to other semiconductors as well, so why are we interested in Si in particular? In order for our devices to work, they must first be Van der Waals bonded to one another. This critical step requires that the bonding surfaces be large and atomically flat, thus Si is an excellent candidate for this approach due to the commercial availability of high-quality Si wafers. Not only do flat surfaces allow us to Van der Waals bond, but flatter surfaces typically have lower disorder – of paramount importance to the quality of the 2DES on the surface. Other compound semiconductors, such as GaAs for example, tend to have more disordered surfaces unless fabricated in UHV; commercially available GaAs does not have the flatness required for our devices. We also require high-quality surface terminations. As mentioned previously, Si surfaces

allow for an abundance of well-studied surface terminations, which make it an obvious choice for our purposes. From a physics perspective, Si is an interesting platform because it is a multi-valley material and has an anisotropic effective mass. The valley degrees of freedom have been explored extensively and have potential implications for future valleytronics technology [102] as well as quantum information processing [103, 104]. From the vantage point of a device engineer, Si is attractive because it has benefited from the development of a trillion dollar microprocessor industry and is an extremely well understood material. Many fabrication techniques from industry are also readily available and device realizations can be efficiently integrated into existing Si technology.

I would be remiss not to mention that the original proposal for a solid-state nuclear spin quantum computer by Kane in 1998 called for the implementation of donor-based spin qubits to be housed in Si [105]. This is in part due to the ability to produce isotopically enriched ^{28}Si ($I = 0$), which eliminates qubit decoherence due to the Overhauser field, but also because this approach would benefit from the success of the silicon industry.

Finally, over the past decade and a half, the Kane lab has developed Si vacuum-FET devices for investigating 2DESs and 2DHSs on hydrogen-terminated Si(111) surfaces that are encapsulated by remote gates in a vacuum cavity [106]. They have reported record mobilities in Si-based devices, with electron mobilities exceeding 300,000 cm^2/Vs [107], enabling the observation of a variety of phenomena including the integer and fractional quantum Hall effects (IQHE and FQHE), valley-valley interactions, and metallic behavior, among others [108–114]. These Si vacuum-FET devices are comprised of two individual pieces that are fabricated independently and then bonded together via Van der Waals forces. In these devices, the H-Si(111) chip hosts the 2DES and the implanted ohmic contacts, while the second piece, the remote vacuum chip, contains the global accumulation gate which induces the 2DES on the H-Si(111) surface. My work described in this dissertation is a natural extension of the ideas developed in the Kane lab by Eng, McFarland, Kott, and Hu.

This brief introduction has highlighted some of the interesting properties of Si, however, more comprehensive discussions of Si and Si device technology can be found in Yu and Cordona (2001) [65], Sze and Ng (2007) [66], and Streetman and Banerjee (2006) [115].

1.2 Summary of results

The following two sections briefly highlight the important results of my research, which are elaborated on in Chs. 3 and 4, and 6, respectively.

1.2.1 SOI-Si non-invasive devices

The primary goal of my research was to develop and demonstrate a fully non-invasive SOI-based gating architecture that allowed for the investigation of 2DES transport on pristine, chemically-terminated Si surfaces. I was able to avoid all harsh device processing on the intrinsic H-Si(111) surface, allowing it to remain in pristine condition, by relegating all harsh processing to a silicon-on-insulator (SOI) chip. Figure 1.3 shows an illustration of the four-terminal device design and a plot of the magnetotransport data from an H-Si(111) surface measured using our novel architecture. The SOI piece houses all of the electrical components, enabling myriad electrostatic gating schemes that confine electrons to a Van der Pauw (VdP) configuration at the micro- and nano-scale, all without the need to dope or gate the Si surface directly. Because the H-Si(111) piece has a pristine surface, it is compatible with a vast assortment of surface terminations that would not be possible with devices in which ohmic contacts are fabricated directly onto the surface. Furthermore, with reduced contact resistance to the 2DES, it will be possible to create and control scaled down 2D, 1D, and 0D structures.

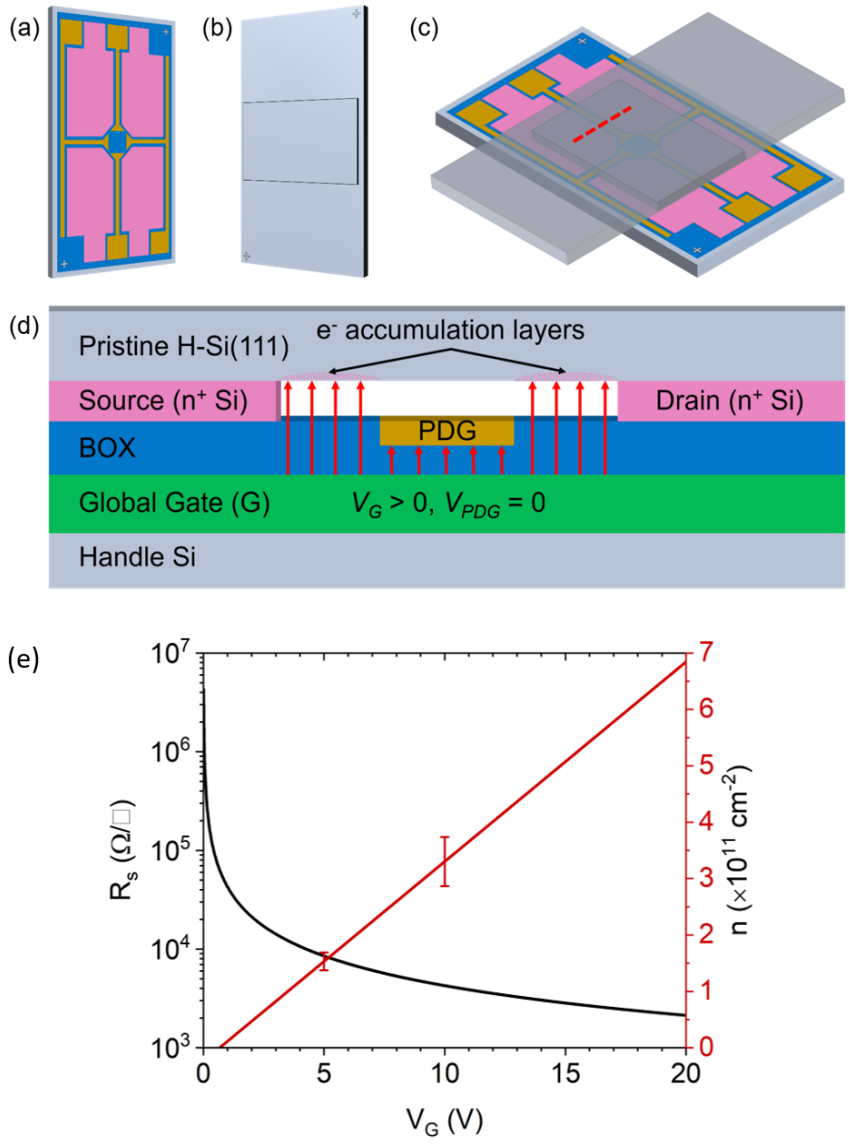

Figure 1.3: Illustration of the four-terminal device architecture: (a) the SOI piece housing all electrical components, (b) the pristine, intrinsic H-Si(111) piece, (c) the Van der Waals bonded device, and (d) a cross-sectional view of the bonded device along the red dashed line in (c). Ohmic contacts (n^+ Si) are shown in pink, buried oxide (BOX) in blue, global gate in green, proximity depletion gates (PDGs) in gold, and Si in gray. A forward bias applied to the global gate results in electron accumulation on the H-Si(111) surface, except where the grounded, vacuum-separated PDGs block the E-field (solid red arrows), depleting the local region. (e) shows the magnetotransport measurements obtained from a typical H-Si(111) surface using our novel architecture.

1.2.2 Iodine-terminated Si(111) surface transport

The second major aim of my research was to demonstrate that we can use our non-invasive SOI architecture to electrostatically gate ambient-sensitive Si surfaces other than the H-Si(111) surface. To this end, I was able to Van der Waals bond to an iodine-terminated Si(111) sample and measure magnetotransport on this fragile surface (see Fig. 1.4 and Table 1.1).

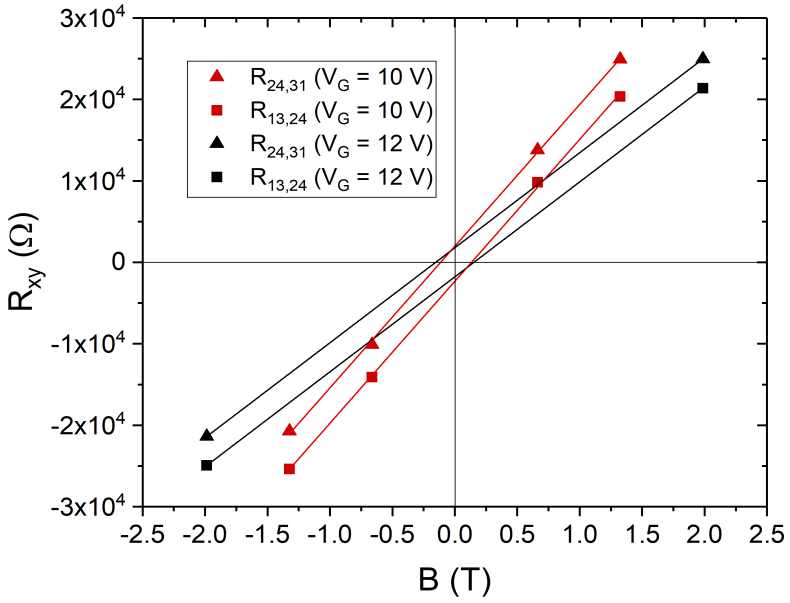

Figure 1.4: Hall resistance R_{xy} versus magnetic field B for two different carrier densities. These are the first reported magnetotransport measurements on a I-Si(111) surface.

Table 1.1: Sheet resistance data for the I-Si(111) sample measured at two different global gate voltages. Also listed are the extracted Hall densities, n, and the extracted carrier mobilities, μ.

Gate Voltage	$R_{horizontal}$	$R_{vertical}$	r	R_s	n	μ
$V_G = 10$ V	10.8 kΩ	8.9 kΩ	1.21	44.4 kΩ/□	3.6x10^{10} cm^{-2}	3900 cm^2/Vs
$V_G = 12$ V	8.7 kΩ	7.4 kΩ	1.18	36.4 kΩ/□	5.4x10^{10} cm^{-2}	3200 cm^2/Vs

This experiment was part of a collaboration between the Kane lab and the Butera lab at the Laboratory for Physical Sciences. While it is still in the early stages of development, I report significant experimental progress, including plots of the Hall resistance and a tabulation of the sheet resistance data obtained from transport measurements on a I-S(111) sample (see Fig. 1.4 and Table 1.1).

1.3 Overview of other 2D platforms

To understand the broader context of my work, it helps to take a step back and consider the different types of 2D systems and materials that are available to the experimentalist. While this is not exhaustive discussion of the literature on the subject, it will give a flavor of the different types of 2D materials and systems that exist, and help highlight some of their advantages and disadvantages. Here, I have broken up the 2DES platforms into one of three categories: surfaces, heterostructures, and 2D materials.

Surfaces — Perhaps the most straightforward type of 2D system one can consider engineering is on the surface of a 3D material. Surfaces are naturally two-dimensional and many 3D bulk materials can be configured to host a 2DES on their surface. Practically, some materials are more favorable hosts and easier to work with, such Si. However even the surface liquid helium has been examined [116–119]. Semiconductor surfaces passivated with an insulating oxide and configured into an FET can be used to confine the 2DES to an oxide-semiconductor interface. The most successful example of this is the Si MOSFET, where 2DESs have been studied extensively [120–130]. Additionally, Lu et al. have reported the fractional quantum Hall effect (FQHE) on an extremely high-mobility SiGe MOSFET [131]. In our device architecture, I used a vacuum-FET approach, where the insulating oxide was replaced by vacuum and the Si surface was chemically passivated with either hydrogen or iodine. Si(111) surfaces partially passivated with iodine are predicted to exhibit electronic behavior similar to that of 2D Dirac material such as graphene [132]. In the last decade, a new class of surface materials have emerged called topological insu-

lators (TIs) [133–137]. TIs are materials that have a gapped or insulating bulk but which possess dissipationless zero-energy edge modes on either the surface (in the 3D TI case) or the sample edges (in the 2D TI case). This "zoo" [138] of topological phases of matter are intimately connected to the integer quantum Hall effect (IQHE) and have potential implications for topological quantum computation [139, 140].

Heterostructures — Heterostructures provide yet another type of 2D system. In brief, a heterostructure is a stack where two or more dissimilar materials are brought together such that a band structure mismatch occurs, resulting in the formation of a 2D quantum well. Considerable effort has been put into the fabrication of heterostructures, both from a materials engineering standpoint [141], and from a materials composition standpoint [142]. Heterostructures have a high degree of tunablity not only in the material composition, but also the layer structure and quantum well thickness. One of the most important materials used for the investigation of 2DESs are GaAs/AlGaAs stacks. They are one of several materials used to fabricate what are known as high-mobility electron transistors (HMETs), with record electron mobilities exceeding 3.6×10^7 cm^2/Vs in samples produced by West and Pfeiffer [143–145]. Another common heterostructure is the Si/SiGe quantum well stack, which has high electron mobilities and excellent compatibility with Si based technology due to the similar lattice parameters [146]. More recently, functional oxide heterostructures [147] like ZnO/ZnMgO [148] and $LaAlO_3/SrTiO_3$ [149] have been investigated for their unique interfacial conductive states, where a 2DES can be confined at the interface despite both layers being insulators. Even more remarkable, it was discovered that the 2DES in the latter material, $LaAlO_3/SrTiO_3$, becomes superconducting at low temperatures [150].

2D materials — In 2004, Geim and Novoselov isolated the first sample of the carbon allotrope, graphene, and were awarded the Nobel Prize in physics in 2010 for their discovery [151]. This discovery led to a 2D material revolution in which significant theoretical and experimental effort went in to characterizing graphene [152–159] as well as other 2D

materials, now known as 2D Van der Waals materials [160–164]. Van der Waals materials are those which have strong covalent bonds with neighboring atoms in a plane, but which have weak Van der Waals attractions along the c-axis. This allows them to be readily separated into 2D sheets of material. Graphene was the first true 2D material to be isolated and studied, but soon afterwards 2D allotropes of other familiar materials began to be investigated, including silicene [165], germanene [166], phosphorene [167], borophene [168], and stanene [169]. These 2D -ene materials are attractive because they push the limits for confining a 2DES to a single monolayer. Their electronic properties can be tuned through doping, gating, and strain, and they exhibit a range of phenomena including massless Dirac fermions and topologically insulating behavior [165, 170, 171]. However, it can be quite difficult to decouple these materials from the substrates they are often bound to. Also, some films are easily oxidized in ambient conditions unless they are properly passivated, which can destroy their electronic properties. In particular, silicene terminated with heavy halogens like iodine is predicted to exhibit topological behavior [170, 171]. Our device architecture could be used as a substrate-decoupling host in an air-gap bridge configuration by using established lamination-transfer techniques (see Ch. 7) [172].

Another class of Van der Waals materials are transition metal dichalcogenides (TMDCs), with molecular composition MX_2, where M is a transition metal and X is a chalcogen [173]. 2D sheets of TMDCs are of particular interest because they lack inversion symmetry and possess enhanced spin-orbit interactions, making them ideal candidates for spintronics and valleytronics devices [174–177].

The last 2D material I will mention is hexagonal boron-nitride (h-BN), which has been studied recently due to its excellent insulating properties, wide band gap, and integration with other 2D materials as functional layers such as substrates for graphene [178–180].

1.4 Prospectus

The remainder of this dissertation is organized as follows. Chapter 2 begins with a survey of the basic physics of two-dimensional electron systems. I then give a brief discussion of some of the measurement techniques I used to investigate them, and conclude with a brief aside on topology.

In Ch. 3 I describe the design, fabrication, and realization of our fully non-invasive electrostatic gating method using an SOI-Si based architecture. Chapter 4 details my magnetotransport results on a pristine, intrinsic H-Si(111) surface using our novel architecture and compares these results to previous experiments. This chapter, as well as Ch. 3, constitutes the first of my two main experiments.

In Ch. 5, I discuss the technical challenges posed by the large series contact resistance, and present a viable solution that addresses this issue. I provide a physical model based on 1D Schottky barrier tunneling to explain our data, and find good agreement with our observations. The model highlights the central parameters that contribute to the large series contact resistance and provides insight into how we can decrease this resistance.

In Ch. 6 I describe the second main experiment of this thesis. Here, I report the first magnetotransport measurements made on an iodine-terminated Si(111) surface using our non-invasive SOI gating approach.

Finally, in Ch. 7 I conclude with a discussion of the over-arching implications of our new non-invasive device architecture and propose some possible experiments.

Supplemental information can be found in the appendices. Full device fabrication recipes can be found in Appendix A, and a repository of some older work on the fabrication of gallium nanowires using focused-ion beam lithography can be found in Appendix B.

Chapter 2: Two-dimensional electron systems: theory

Two-dimensional electron systems (2DESs) are a rich platform for the investigation of new physics. A wealth of intriguing physical phenomena have been discovered in 2DESs and many of these have led to deep insights into the physics of condensed matter systems. While not intended to be a comprehensive review of the properties of 2DESs, this chapter provides some basic background for understanding 2DESs. For a full treatment of the subject, I point the reader to the review by Ando, Fowler, and Stern [181], and the references therein.

My thesis research was primarily concerned with the fabrication of a non-invasive SOI gated device and proof-of-concept measurements of these devices from 4.2 K to 77 K. In this temperature range, I did not expect to see much if any interesting quantum effects seen in other 2DESs at lower temperatures. However, the theory presented in this chapter is still relevant for other possible 2DES experiments using our non-invasive architecture if the device performance (i.e. series resistance) can be improved at low temperatures. Furthermore, there is a trove of physics to be explored at low temperatures, not covered in this work, but covered in great detail by my predecessors McFarland and Kott working with earlier generation devices. I point the readers to their theses for a more in depth look at the low temperature physics of 2DESs on H-Si(111) surfaces [113, 114].

2.1 Solid state review

An ideal two-dimensional electron system (2DES) would have electrons electrons that are free to move in two of the three spatial dimensions, but which are confined to zero

width in the third dimension (the z-direction by convention). In reality, physical systems occupy finite volumes of space, thus in a real 2DES, the electrons are confined in the third dimension to a non-zero spatial extent, Δz, such that $\Delta z \sim 1/k_F$ where k_F is the Fermi wavevector. The Fermi wavevector is defined by the 2D electron density n and is given by $k_F = \sqrt{g_v g_s \pi n}$, where g_v and g_s are the valley and spin degeneracies, respectively. This spatial confinement leads to quantized motion of the electrons in the z-direction; thus it is this constraint on the third spatial coordinate that differentiates a real 2DES from a 3DES. In the following sections I develop some of the models of 2DESs used to understand their behavior. The discussions in the following sections are assisted with reference to Yu and Cordona (2001) [65], Sze and Ng (2007) [66], and Ibach and Lüth (1995) [182], unless otherwise noted. Bold characters represent vector or tensor quantities and Miller index notation is used to define crystallographic coordinates.

2.1.1 Lattice and reciprocal lattice vectors

In a three-dimensional crystal lattice, we can assign a real space coordinate $\mathbf{x} = (x_1, x_2, x_3)$ to each point in the lattice and provide instructions on how to move from one point in the lattice to any other point in the lattice. Those instructions come in the form of primitive vectors $\mathbf{a}_1$, $\mathbf{a}_2$, and $\mathbf{a}_3$, that form a real space basis and define a primitive cell (see Fig. 2.1). We can then define a lattice translation vector $\mathbf{R}$:

$$\mathbf{R} = n_1\mathbf{a}_1 + n_2\mathbf{a}_2 + n_3\mathbf{a}_3 \tag{2.1}$$

where $n_i = 0, \pm 1, \pm 2, \ldots$. Likewise, we can define a reciprocal space lattice (dual lattice) with coordinates $\mathbf{k} = (k_1, k_2, k_3)$ and that has a dual lattice translation vector, $\mathbf{G}$:

$$\mathbf{G} = m_1\mathbf{b}_1 + m_2\mathbf{b}_2 + m_3\mathbf{b}_3 \tag{2.2}$$

where $m_i = 0, \pm 1, \pm 2, ...$, and $\mathbf{b}_1$, $\mathbf{b}_2$, and $\mathbf{b}_3$ are the primitive vectors of the reciprocal space, and are formally related to the real space primitive vectors by:

$$[\mathbf{b}_1\mathbf{b}_2\mathbf{b}_3]^{\mathbf{T}} = 2\pi[\mathbf{a}_1\mathbf{a}_2\mathbf{a}_3]^{\mathbf{-1}} \tag{2.3}$$

Using **R** and **G**, we can now define each point in the real space (**x**) and reciprocal space (**k**) lattices.

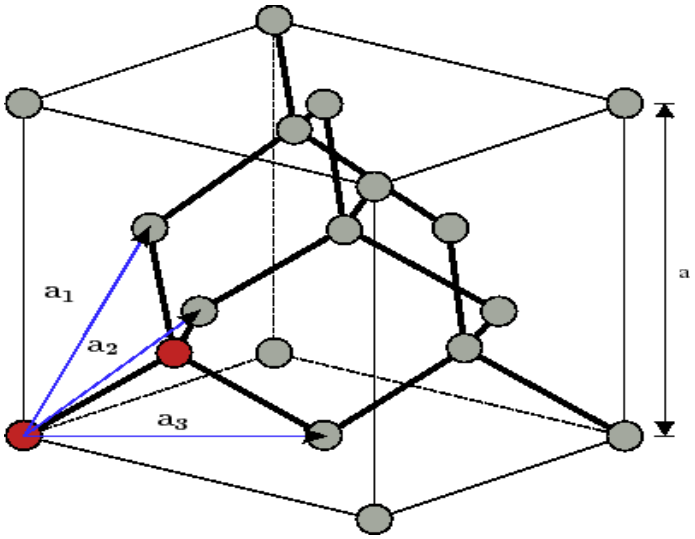

Figure 2.1: A 3D model of the face-centered diamond-cubic primitive cell for Si in real space, with primitive vectors $\mathbf{a}_1$, $\mathbf{a}_2$, and $\mathbf{a}_3$, which form a real space basis according to Eq. 2.1.

2.1.2 Periodic potentials and Bloch waves

In a crystalline solid, each point on the lattice represents the position of an atom which contributes its own Coulomb potential. Given that the lattice is periodic in **x**, the total Coulomb potential in the crystal will also be periodic in **x**, such that $V(\mathbf{x}) = V(\mathbf{x}+\mathbf{R})$. I note that periodicity in real space implies periodicity in reciprocal space. Now consider the time-independent Schrödinger equation for a single electron of mass m_e moving through this periodic potential in a lattice of infinite extent. Of course in real systems, we must

worry about boundaries and surfaces, but for now I will assume infinite spacial extent. Our task then becomes to solve the following:

$$\left[-\frac{\hbar^2}{2m_e}\nabla^2 + V(\mathbf{x})\right]\Psi_{\mathbf{k}}(\mathbf{x}) = E\Psi_{\mathbf{k}}(\mathbf{x}) \tag{2.4}$$

The unique solutions to this equation are given by Bloch's theorem and are called Bloch wavefunctions, which can be written in the form:

$$\Psi_{\mathbf{k}}(\mathbf{x}) = u_{\mathbf{k}}(\mathbf{x})e^{i\mathbf{k}\cdot\mathbf{x}} \tag{2.5}$$

where $u_{\mathbf{k}}(\mathbf{x})$ are envelope functions with the same periodicity as $V(\mathbf{x})$. The periodicity of the lattice potential and the envelope functions imply that both the energy eigenfunctions $\Psi_{\mathbf{k}}(\mathbf{x})$ and the energy eigenvalues $E(\mathbf{k})$ are periodic in $\mathbf{k}$, such that:

$$\Psi_{\mathbf{k}}(\mathbf{x}) = \Psi_{\mathbf{k}+\mathbf{G}}(\mathbf{x}) \tag{2.6}$$

$$E(\mathbf{k}) = E(\mathbf{k}+\mathbf{G}) \tag{2.7}$$

This means that Bloch waves with crystal momentum $\mathbf{k}$ that differ by a reciprocal lattice translation $\mathbf{G}$ are identical and have the same energy.

2.1.3 Nearly free electron model

If we assume that the potential is zero to begin with and is slowly turned on, while still demanding the periodicity in Eq. 2.7, we get a parabolic dispersion relation to lowest

order:

$$E(\mathbf{k}) = E(\mathbf{k}+\mathbf{G}) = \frac{\hbar^2}{2m_e}(\mathbf{k}+\mathbf{G})^2. \tag{2.8}$$

This means that there are infinitely many parabolas, shifted by integer multiples of $\mathbf{G}$, that describe the energy of the electronic states of our system. For simplicity, the one-dimensional case is shown in Fig. 2.2, where $\mathbf{G}$ simply becomes $G = 2\pi/a$ and a is the 1D lattice spacing.

Figure 2.2 shows an example. Note how the parabolas cross one another in multiple places. In reality, for a non-zero potential, the parabolas typically avoid each other, creating an avoided level crossing (red in Fig. 2.2). Two states which originally had the same energy (at a crossing point), split into symmetric and anti-symmetric states with lower and

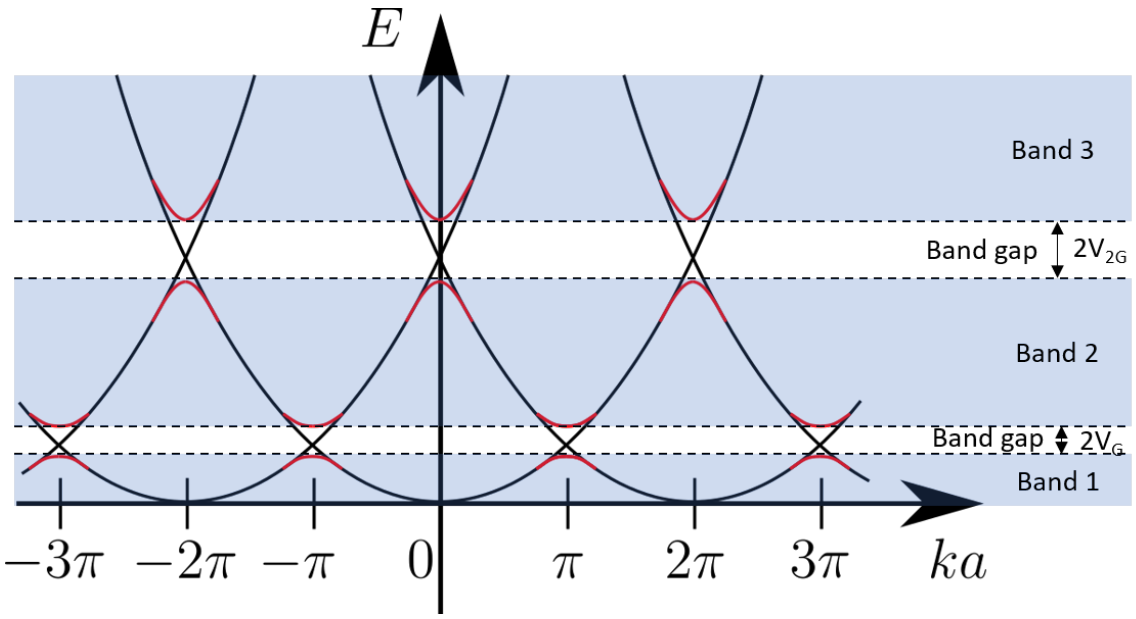

Figure 2.2: A 1D band diagram illustrating the infinitely many parabolas arising from the periodic dispersion relation in Eq. 2.8. The regions where the parabolas cross are split into higher and lower energy states, called avoided level crossings (in red). These avoided crossings lead to regions of allowed energy levels (bands) and disallowed energy regions (band gaps), where the band gap is proportional to the periodic potential.

higher energy, respectively. This level splitting creates forbidden energy regions called band gaps, whose height is proportional to the strength of the periodic potential, as well as bands of allowed energy regions. We can further reduce the complexity of the problem by only considering the region of k values between $\pm G/2$, known as the first Brillouin zone. From here on, we shall only consider $\mathbf{k}$ values in the first Brillouin zone.

Extension to a real three dimensional lattice is straightforward. In three dimensions, we can label our Brillouin zone with special points and $\mathbf{k}$-space paths that have high symmetry. Table 2.1 and Fig. 2.3 show examples for a face-centered cubic (FCC) lattice. One simply considers $E(\mathbf{k})$ along each path to different points of high symmetry, resulting in a series of 1D dispersion plots. When all of these 1D plots are stitched together at points of high symmetry, we get energy band diagrams (see Fig. 2.4).

Table 2.1: High symmetry points and high symmetry paths in the first Brillouin zone of an FCC lattice, as illustrated in Fig. 2.3. Also listed are the corresponding $\mathbf{k}$-space axes and their degeneracies.

Points of high symmetry	Path from Γ	Reciprocal lattice coordinate	Degeneracy
Γ	-	$\{000\}$	1
X	Δ	$\{100\}$	6
L	Λ	$\{111\}$	8
K	Σ	$\{110\}$	12
U	-	$\{121\}$	12
W	-	$\{120\}$	24

2.1.4 Silicon valleys

Silicon has a face-centered diamond-cubic lattice structure, as shown in Fig. 2.1, and contains six equivalent conduction band minima, called valleys, located about 85% of the way along the Δ-path near the X-points (see Fig. 2.4). We denote this valley degeneracy by $g_v = 6$ for the bulk as well as the Si(111) surface (when we project into two dimensions). However, the degeneracy g_v will in general depend on the orientation of the surface and

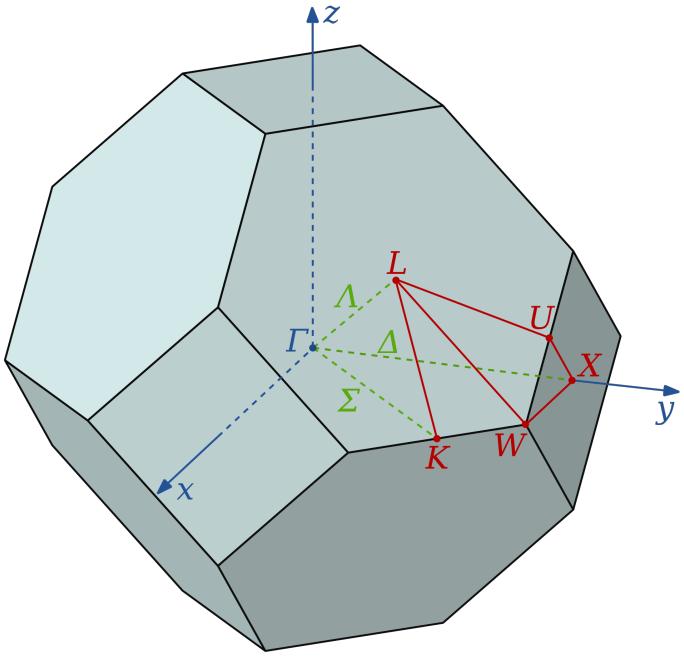

Figure 2.3: A 3D model for an FCC crystal illustrating the points and paths of high symmetry in the first Brillouin zone of Si.

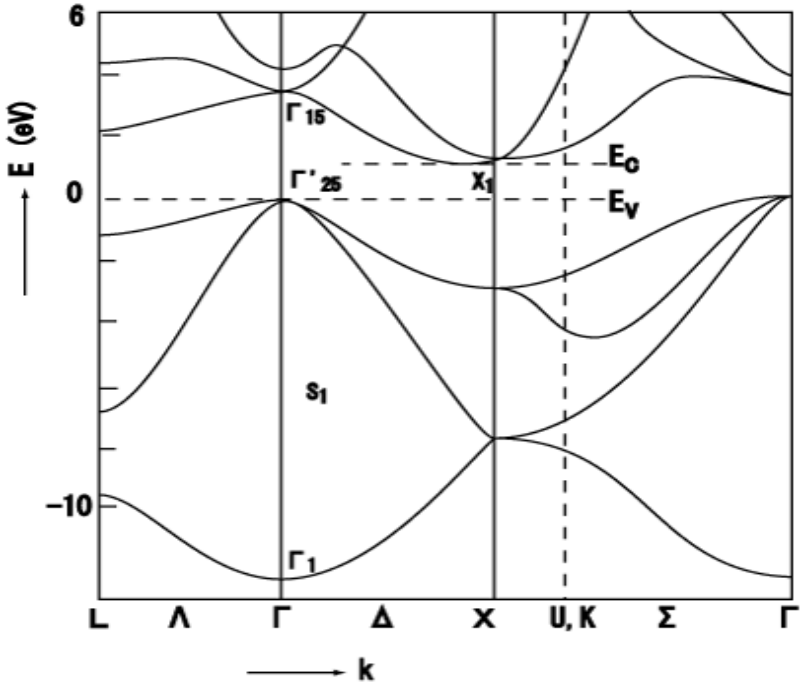

Figure 2.4: Dispersion relation in Si plotted along paths of high symmetry and stitched together at points of high symmetry. This is an energy band diagram.

whether or not any valley-splitting mechanisms are present (broken inversion symmetry). Likewise, the spin degeneracy is denoted by $g_s = 2$ in the absence of Zeeman spin-splitting and by $g_s = 1$ in the presence of broken time-reversal symmetry. The total degeneracy of our electron system in Si can then be written as $g = g_v g_s$.

Additionally, because Si is an indirect band-gap material (the conduction band minima are not at the Γ-point), the six valleys form six constant-energy ellipsoids centered at the valley minima along the Δ-path. An illustration of these constant energy surfaces can be seen in Fig. 2.5, as well as a projection of the six ellipsoids onto the (111) surface. The ellipsoidal nature of these surfaces give rise to an anisotropic effective mass, which we will see in the following sections is an important parameter that determines many of the properties of the electrons. Table 2.2 lists the valley degeneracies for some of the common surface orientations that are studied.

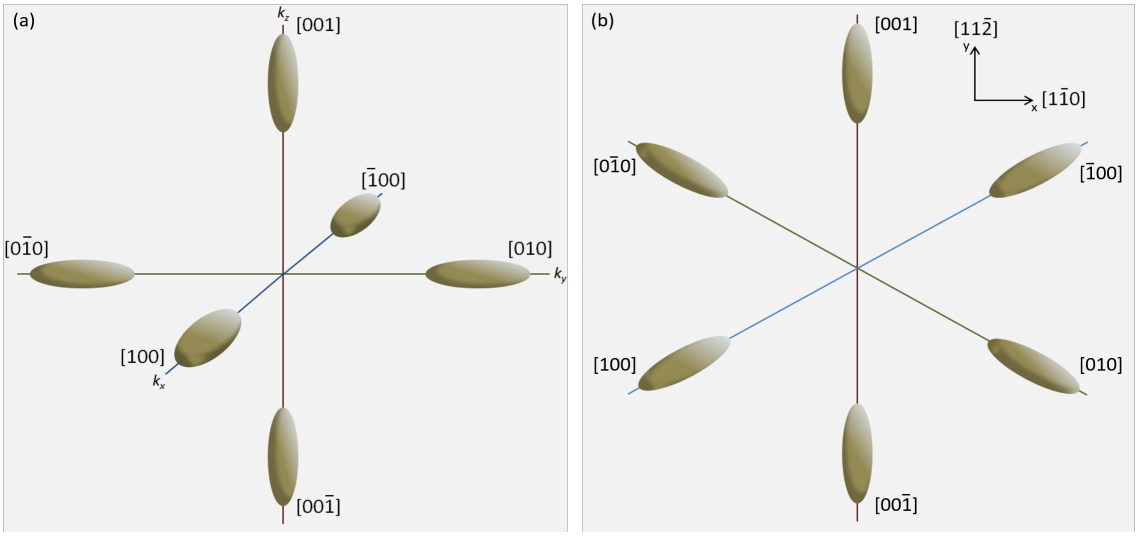

Figure 2.5: Illustration of the six equivalent constant-energy ellipsoids located ∼85% of the way to the X-point along the Δ-path. These ellipsoids represent the six degenerate valleys for (a) bulk Si and (b) the 2D projection onto the Si(111) surface. The ellipsoidal nature of the valleys leads to an effective mass anisotropy, with the major and minor axes of the ellipsoids representing the longitudinal and transverse effective masses, respectively. Our choice of rotation angles in Eq. 2.20 takes us from (a) to (b).

Table 2.2: The three most common surface orientations for Si samples along with their valley degeneracies and valley splitting.

Surface orientation	Valley pair	Valley degeneracy	Valley splitting
(100)	$\langle 001 \rangle$	$g_v = 2$	ground
	$\langle 100 \rangle$, $\langle 010 \rangle$	$g_v = 4$	excited
(110)	$\langle 100 \rangle$, $\langle 010 \rangle$	$g_v = 4$	ground
	$\langle 001 \rangle$	$g_v = 2$	excited
(111)	$\langle 100 \rangle$, $\langle 010 \rangle$, $\langle 001 \rangle$	$g_v = 6$	ground

2.1.5 Effective mass approximation

The effective mass approximation is a very useful single-electron model for interpreting the band structure of solid-state systems in the low energy regime. Using this model, we can approximate the motion of an electron of mass m_e in a periodic crystal potential as if it were an electron moving through free space but with a modified effective mass m^*. Because we are in the low energy limit, we can approximate the bottom of the conduction band as a parabola and arrive at the following dispersion relation:

$$E(\mathbf{k}) = \frac{\hbar^2}{2m^*}\mathbf{k}^2 = \frac{\hbar^2}{2m^*}(k_x^2 + k_y^2 + k_z^2) \tag{2.9}$$

The inverse of the effective mass, $1/m^*$, can then simply be expressed as the curvature of the conduction band. Taking the second derivative of $E(\mathbf{k})$ in Eq. 2.9 with respect to $\mathbf{k}$, we get:

$$\frac{1}{m^*} = \frac{1}{\hbar^2}\frac{d^2E}{d\mathbf{k}^2} \tag{2.10}$$

However, the expression in Eq. 2.9 is based on two assumptions that are not true for Si. First, Eq. 2.9 implies that the bottom of the conduction band is at the Γ-point, and second

it gives an effective mass that is a scalar, or isotropic throughout the Brillouin zone. Of course in Si the conduction band minima are not located at the Γ-point, but are instead located close to the X-points along the Δ-path. This leads to ellipsoidal constant energy surfaces (see Fig. 2.5) and an effective mass that is not isotropic. This requires that we express the effective mass of the electron not as a scalar, as in Eq. 2.10, but rather as a tensor $\mathbf{M}$ (or equivalently by its inverse $\mathbf{W} = \mathbf{M}^{-1}$). Let us drop the asterisks notation for the effective mass (which assumes isotropy), and instead express the effective mass in terms of matrix elements of effective mass tensors, $\mathbf{M}$ and $\mathbf{W}$, where:

$$w_{ij} = \frac{1}{m_{ij}} = \frac{1}{\hbar^2}\frac{\partial^2 E}{\partial k_i \partial k_j}. \tag{2.11}$$

We will use $\mathbf{M}$ and $\mathbf{W}$ interchangeably based on convenience going forward, and both will be referred to as the effective mass tensor unless clarification is required. In general, we can choose a basis aligned with the principal axes and express these effective mass tensors for an anisotropic system as:

$$\mathbf{W} = \mathbf{M}^{-1} = \begin{pmatrix} m_{xx} & 0 & 0 \\ 0 & m_{yy} & 0 \\ 0 & 0 & m_{zz} \end{pmatrix}^{-1} = \begin{pmatrix} \frac{1}{m_{xx}} & 0 & 0 \\ 0 & \frac{1}{m_{yy}} & 0 \\ 0 & 0 & \frac{1}{m_{zz}} \end{pmatrix} \tag{2.12}$$

This leads to a more general dispersion relation for the motion of an electron in an anisotropic system within the effective mass approximation:

$$E(\mathbf{k}) = \frac{\hbar^2}{2}(\mathbf{k}-\mathbf{k}_0)\cdot\mathbf{W}\cdot(\mathbf{k}-\mathbf{k}_0) \tag{2.13}$$

where $\mathbf{k}_0$ denotes the location in $\mathbf{k}$-space of the conduction band minima. For silicon, $k_0 \approx 0.85\pi/a$, where $a = 5.431\,\text{Å}$ is the lattice constant. Since ellipsoids are characterized

by one major axis and two equivalent minor axes, electrons in a given valley in Si will take on one of two effective masses along the principal directions, as seen in Fig. 2.5. Electrons travelling along the major, or longitudinal axis, will have an effective mass given by the curvature along the longitudinal axis, with $m_l = 0.98m_e$. Similarly, electrons travelling along the minor, or transverse axes, will have an effective mass given by the curvature of the transverse axis, with $m_t = 0.19m_e$.

I note that the effective mass tensor is a local description of electrons in each valley; however, opposite momentum valley pairs are equivalent within the effective mass approximation, meaning they are described by the same **M** and **W** tensors. We must therefore consider triplets of **M** and **W** for each problem. A list of some effective mass parameters is given in Table 2.3.

We can now perform arbitrary rotations on **W** to describe the motion of electrons along any crystalline direction, not just the principal axes. These rotations can be expressed in terms of Euler angles, α, β, and γ, and corresponding rotation matrices, $\mathbf{X}(\alpha)$, $\mathbf{Y}(\beta)$, and $\mathbf{Z}(\gamma)$, given by:

$$\mathbf{X}(\alpha) = \begin{pmatrix} 1 & 0 & 0 \\ 0 & cos(\alpha) & -sin(\alpha) \\ 0 & sin(\alpha) & cos(\alpha) \end{pmatrix} \tag{2.14}$$

$$\mathbf{Y}(\beta) = \begin{pmatrix} cos(\beta) & 0 & sin(\beta) \\ 0 & 1 & 0 \\ -sin(\beta) & 0 & cos(\beta) \end{pmatrix} \tag{2.15}$$

$$\mathbf{Z}(\gamma) = \begin{pmatrix} cos(\gamma) & -sin(\gamma) & 0 \\ sin(\gamma) & cos(\gamma) & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{2.16}$$

which can be combined more compactly to form a general rotation matrix $\mathbf{R}(\alpha,\beta,\gamma)$:

$$\mathbf{R}(\alpha,\beta,\gamma) = \mathbf{X}(\alpha)\mathbf{Y}(\beta)\mathbf{Z}(\gamma) \tag{2.17}$$

$$\mathbf{R}^{\mathbf{T}}(\alpha,\beta,\gamma) = \mathbf{Z}^{\mathbf{T}}(\gamma)\mathbf{Y}^{\mathbf{T}}(\beta)\mathbf{X}^{\mathbf{T}}(\alpha) \tag{2.18}$$

where $\mathbf{R}^{\mathbf{T}}(\alpha,\beta,\gamma)$ is the transpose of $\mathbf{R}(\alpha,\beta,\gamma)$. This allows us to express any arbitrary rotation of the effective mass tensor, with respect to a fixed coordinate system, as:

$$\mathbf{W}' = \mathbf{R}(\alpha,\beta,\gamma)\cdot\mathbf{W}\cdot\mathbf{R}^{\mathbf{T}}(\alpha,\beta,\gamma) \tag{2.19}$$

We now have all the necessary tools to find the effective mass tensors for each valley pair. To do this, we must first rotate $\mathbf{W}$ with respect to a fixed coordinate system, then pick out the principal axis masses for each valley pair, and finally assign each m_{xx}, m_{yy}, and m_{zz} with either m_l or m_t. As an example, let us find $\mathbf{W}$ for the $\langle 001\rangle$ valley pairs after a rotation into the $[111]_z$ basis since I was most interested in the (111) surface. By $[111]_z$ basis, I mean a rotation of $\mathbf{W}$ such that the [111] crystalline direction lies along the positive z-axis of our coordinate system. Although there are infinitely many ways to rotate into this frame, a convenient choice of rotation angles is to rotate $\mathbf{W}$ by $\gamma = 5\pi/4$ about the z-axis, then do no rotation about the y-axis, then finally rotate $\mathbf{W}$ by $\alpha = -\arccos(1/\sqrt{3})$ about the x-axis. We can write this as:

$$\mathbf{W}^{[111]_z} = \mathbf{R}(-\arccos(1/\sqrt{3}),0,5\pi/4)\cdot\mathbf{W}\cdot\mathbf{R}^{\mathbf{T}}(-\arccos(1/\sqrt{3}),0,5\pi/4) \tag{2.20}$$

which gives:

$$\mathbf{W}^{[111]_z} = \begin{pmatrix} \frac{m_{xx}+m_{yy}}{2m_{xx}m_{yy}} & \frac{m_{yy}-m_{xx}}{2\sqrt{3}m_{xx}m_{yy}} & \frac{m_{yy}-m_{xx}}{\sqrt{6}m_{xx}m_{yy}} \\ \frac{m_{yy}-m_{xx}}{2\sqrt{3}m_{xx}m_{yy}} & \frac{1}{6}\left(\frac{1}{m_{xx}}+\frac{1}{m_{yy}}+\frac{4}{m_{zz}}\right) & \frac{\sqrt{2}}{6}\left(\frac{1}{m_{xx}}+\frac{1}{m_{yy}}-\frac{2}{m_{zz}}\right) \\ \frac{m_{yy}-m_{xx}}{\sqrt{6}m_{xx}m_{yy}} & \frac{\sqrt{2}}{6}\left(\frac{1}{m_{xx}}+\frac{1}{m_{yy}}-\frac{2}{m_{zz}}\right) & \frac{1}{3}\left(\frac{1}{m_{xx}}+\frac{1}{m_{yy}}+\frac{1}{m_{zz}}\right) \end{pmatrix} \tag{2.21}$$

Next, we refer to Fig. 2.5 and Table 2.3 to build the specific rotated $\mathbf{W}$ for the $\langle 001 \rangle$ valley pair in the $[111]_z$ basis where we have $m_{zz} = m_l$, $m_{xx} = m_{yy} = m_t$, and we get:

$$\mathbf{W}^{[111]_z,\langle 001 \rangle} = \begin{pmatrix} \frac{1}{m_t} & 0 & 0 \\ 0 & \frac{1}{3}\left(\frac{m_l+2m_t}{m_l m_t}\right) & \frac{\sqrt{2}}{3}\left(\frac{m_l-m_t}{m_l m_t}\right) \\ 0 & \frac{\sqrt{2}}{3}\left(\frac{m_l-m_t}{m_l m_t}\right) & \frac{1}{3}\left(\frac{2m_l+m_t}{m_l m_t}\right) \end{pmatrix} \tag{2.22}$$

We can repeat this process for the $\langle 100 \rangle$ and $\langle 010 \rangle$ valley pairs, by choosing $m_{xx} = m_l$, $m_{yy} = m_{zz} = m_t$, and $m_{yy} = m_l$, $m_{xx} = m_{zz} = m_t$, respectively, or we can choose different rotation angles such that $\mathbf{W}$ is rotated into the $[111]_x$ or $[111]_y$ basis.

2.1.6 Projection into 2D

Up to this point I have described the motion of electrons in a three-dimensional bulk of a crystal. Here I consider a 2D electron system created by confining electrons to a Si surface accumulation layer by means of an electrostatic potential. If we confine the electron in one dimension, typically the z-direction by convention, we can map the 3D effective mass tensor to the Si surface to get a 2D effective mass tensor. Notice that for each valley pair, according to Eq. 2.21, $w_{zz}^{[111]_z}$ is identical. This means that a 2D projection of $\mathbf{W}$ onto the (111) surface in the $[111]_z$ basis results in a 6-fold valley degeneracy (neglecting

Table 2.3: List of some of the common effective mass parameters used in this chapter. Masses m_l and m_t are defined by the major and minor axes, respectively, of the constant energy ellipsoids in Fig. 2.5, the normal mass m_{zz} defines the ground state energy of the 2DES (E_0^z) on the Si(111) surface, m^* shows up in density of states (DoS) calculations as the isotropic, geometric mean of the principal masses, and $\bar{m}$ shows up in the 2D resistivity calculations as the arithmetic mean of the principal masses.

Effective mass name	Symbol	Expression
Free electron mass	m_e	$9.109 \times 10^{-31} kg$
Longitudinal mass	m_l	$0.98 m_e$
Transverse mass	m_t	$0.19 m_e$
Normal mass (111)	m_{zz}	$\left(\frac{3m_l m_t}{2m_l + m_t}\right)$
3D DoS mass	m^*	$\sqrt[3]{m_{xx} m_{yy} m_{zz}}$
2D DoS mass	m^*	$\sqrt{m_x m_y}$
Average in-plane mass	$\bar{m}$	$\frac{m_x + m_y}{2}$

spin), since the effective mass in the confined direction sets the ground state energies for each valley. Let us drop the $[111]_z$ superscript and now let w_{ij} refer to elements of our rotated $\mathbf{W}$ in Eq. 2.22. Following a derivation by Stern and Howard [183], one gets a new 2D dispersion relation:

$$E(\mathbf{k}) = E_0^z + \frac{\hbar^2}{2}\left[\left(w_{xx} - \frac{w_{xz}^2}{w_{zz}}\right)k_x^2 + 2\left(w_{xy} - \frac{w_{xz}w_{yz}}{w_{zz}}\right)k_x k_y + \left(w_{yy} - \frac{w_{yz}^2}{w_{zz}}\right)k_y^2\right] \quad (2.23)$$

where here, $\mathbf{k} = (k_x, k_y)$, and E_0^z is the ground state energy in the quantized z-direction. From this point forward, now that we have mapped our 3D electron system to two dimensions, I will use $\mathbf{k} = (k_x, k_y)$. In § 2.1.7 I will show that it is valid to assume our 2DES lives in the ground state of the z-component energy and that it is well-separated from the first excited state E_1^z. Eq. 2.23 can then be more compactly written as:

$$E(\mathbf{k}) = E_0 + \frac{\hbar^2}{2}\left(\frac{k_x^2}{m_x} + \frac{2k_x k_y}{m_{xy}} + \frac{k_y^2}{m_y}\right), \quad (2.24)$$

and the new 2D effective mass tensor elements become:

$$m_x = \left(w_{xx} - \frac{w_{xz}^2}{w_{zz}} \right)^{-1} \tag{2.25}$$

$$m_{xy} = m_{yx} = \left(w_{xy} - \frac{w_{xz} w_{yz}}{w_{zz}} \right)^{-1} \tag{2.26}$$

$$m_y = \left(w_{yy} - \frac{w_{yz}^2}{w_{zz}} \right)^{-1} \tag{2.27}$$

and:

$$\mathbf{M}_{2D} = \begin{pmatrix} m_x & m_{xy} \\ m_{yx} & m_y \end{pmatrix}. \tag{2.28}$$

Because we chose the specific rotation angles in Eq. 2.20, the 2D projection of the $\langle 001 \rangle$ valleys are now aligned along the y-axis of our coordinate system (see Fig. 2.5(b)). Continuing the example from § 2.1.5, we can write down the 2D effective mass tensor for electrons in the $\langle 001 \rangle$ valleys on the (111) surface:

$$\mathbf{M}_{2D}^{\langle 001 \rangle} = \begin{pmatrix} m_t & 0 \\ 0 & \frac{1}{3}(2m_l + m_t) \end{pmatrix} \tag{2.29}$$

$\mathbf{M}_{2D}$ for the other two valley pairs, $\langle 010 \rangle$ and $\langle 100 \rangle$, can be obtained through in-plane rotations of $\mathbf{M}_{2D}^{\langle 001 \rangle}$ by $\mathbf{Z}(2\pi/3)$ and $\mathbf{Z}(4\pi/3)$, respectively (see Fig. 2.5(b)). We now have a recipe to build the 2D effective mass tensor for any silicon surface to which we choose to confine our electrons. The procedure is as follows:

1. Perform a tensor rotation on general $\mathbf{W}$, choosing a convenient basis and corresponding rotation angles using Eq. 2.19.

2. Assign each principal axis effective mass with either m_l or m_t, depending on valley pair, by referring to Fig. 2.5 and Table 2.3.

3. Project the 3D effective mass tensor onto the 2D surface under study, according to Eqs. 2.25, 2.26, and 2.27, and build $\mathbf{M}_{2D}$.

4. If in (111) plane, perform in-plane $\mathbf{Z}(\gamma)$ rotations on $\mathbf{M}_{2D}^{\langle 001\rangle}$ of $2\pi/3$ and $4\pi/3$ to get $\mathbf{M}_{2D}^{\langle 010\rangle}$ and $\mathbf{M}_{2D}^{\langle 100\rangle}$, respectively (see Fig. 2.5(b)).

2.1.7 2D confinement

If we wish to confine our electron system to a 2D surface, we need to consider the nature of the confining potential $\Phi(z)$. For electrons in heterostructures and 2D materials, this confinement potential is built in by the band structure mismatch from the materials themselves, and the result is typically something resembling a 2D square well potential. For electrons confined to a surface, this is provided either through an image or surface potential balanced by an applied external field, most often provided by a gate electrode. In the parallel-plate capacitor (PPC) model, one assumes a triangular well potential $\Phi(z) = Fz$, which gives a constant effective electric field F provided A $\gg$ d, where A is the area of the plates and d is the separation between the plates. Here, $F = \frac{en}{\varepsilon_s}$ is the electric field and ε_s is the permittivity of the semiconductor. To simplify the problem, I will assume that the potential energy is infinite inside the insulator and triangular inside the semiconductor. The confining potential energy U as a function of z can then be written as:

$$U(z) = \begin{cases} \infty & z < 0 \\ eFz & z \geq 0 \end{cases} \tag{2.30}$$

The time-independent Schrödinger equation for a single electron in the semiconductor

well can then be written as:

$$\left[-\frac{\hbar^2}{2}\nabla\cdot(\mathbf{W}\cdot\nabla)+eFz\right]\Psi(\mathbf{x})=E\Psi(\mathbf{x}) \tag{2.31}$$

Separating out the z-component of the wavefunction, $\Psi(\mathbf{x})=\phi_{\mathbf{k}}(x,y)\psi(z)$, and recasting $\psi(z)=\sum_{j=1}^{\infty}c_j\zeta_j(z)$ as a linear combination of orthonormal basis functions, Eq. 2.31 can be rewritten as:

$$\left[\frac{\hbar^2}{2}\nabla\cdot(\mathbf{W}_{2D}\cdot\nabla)\phi_{\mathbf{k}}(x,y)+E(\mathbf{k})\phi_{\mathbf{k}}(x,y)\right]+\sum_{j=1}^{\infty}c_j\left[\frac{d^2}{ds_j^2}\zeta_j(z)-s_j\zeta_j(z)\right]=0 \tag{2.32}$$

where I have made the substitution $s_j=\frac{2m_{zz}}{\hbar^2}\left(eFz-E_j^z\right)$ and c_j are normalization constants. Here, E_j^z is the jth energy eigenvalue of the z-component wavefunction. The solution to Eq. 2.32 is well known. Because the confining potential is only a function of z, the x- and y-components of the wavefunction are the familiar Bloch waves with envelope functions $u_{\mathbf{k}}(x,y)$ due to the periodic lattice potential (contained in $\mathbf{W}_{2D}$), while the z-component is given by Airy functions of the first kind $\mathrm{Ai}(s_j)$. Thus I can write:

$$\Psi(\mathbf{x})=\phi_{\mathbf{k}}(x,y)\sum_{j=1}^{\infty}c_j\zeta_j(z)=u_{\mathbf{k}}(x,y)e^{ik_xx}e^{ik_yy}\sum_{j=1}^{\infty}c_j\mathrm{Ai}(s_j) \tag{2.33}$$

The Airy functions of the first kind, $\zeta_j(z)=\mathrm{Ai}(s_j)$, satisfy differential equations of the form $\zeta''-s\zeta=0$, and are defined by the improper Riemann integral:

$$\mathrm{Ai}(s_j)=\frac{1}{\pi}\int_0^{\infty}dt\,cos\left(\frac{t^3}{3}+s_jt\right) \tag{2.34}$$

While this integral equation does not have an analytic solution in terms of known functions, I am more interested in the energy spectrum. The approximate z-component energy eigenvalues are [181]:

$$E_j^z \approx \left(\frac{\hbar^2}{2m_{zz}}\right)^{1/3}\left(\frac{3\pi eF}{2}\left(j+\frac{3}{4}\right)\right)^{2/3} = \left(\frac{\hbar^2}{2m_{zz}}\right)^{1/3}\left(\frac{3\pi e^2 n}{2\varepsilon}\left(j+\frac{3}{4}\right)\right)^{2/3} \tag{2.35}$$

From this we find that the ground state energy E_0^z is well-separated from the first excited state E_1^z, with $\Delta_{10}^z = E_1^z - E_0^z \approx 5.786\left(n^{2/3}\right) \times 10^{-10}$ eV. For $n = 5 \times 10^{11}$ cm^{-2}, one finds $\Delta_{10}^z \approx 36.4$ meV ≈ 420 K, thus we can be confident that within the effective mass approximation we do not need to worry about occupancy of higher sub-bands from motion of electrons in the z-direction.

2.1.8 2D density of states

While the 2DES motion is quantized in the z-direction, and we have just shown that we can ignore sub-bands corresponding to motion in the z-direction, there are still transverse $\phi_{\mathbf{k}}(x,y)$ sub-band orbitals that form a quasi-continuum of states. It is natural then to see precisely how many states are available to electrons in the ground state sub-band. I have already solved the Schrödinger equation in § 2.1.7, so we can take the x- and y-components of the wavefunctions and derive the density of states (DoS) for a 2DES confined to an area, $A = L_x L_y$. The Bloch wave solutions for the transverse motion are:

$$\phi_{\mathbf{k}}(x,y) = u_{\mathbf{k}}(x,y)e^{ik_x x}e^{ik_y y}. \tag{2.36}$$

These give the familiar dispersion relation:

$$E(\mathbf{k}) = \frac{\hbar^2}{2m^*}\mathbf{k}^2 = \frac{\hbar^2}{2m^*}\left(k_x^2 + k_y^2\right) \tag{2.37}$$

I now impose Dirichlet boundary conditions by demanding that $\phi_{\mathbf{k}}(x,y)$ vanish at every point along all four edges of our rectangular well, $\phi_{\mathbf{k}}(x,0) = \phi_{\mathbf{k}}(x,L_y) = \phi_{\mathbf{k}}(0,y) = \phi_{\mathbf{k}}(L_x,y) = 0$ for $0 \leq x \leq L_x$ and $0 \leq y \leq L_y$. From this, we get the following constraints:

$$k_x = \frac{m_x \pi}{L_x}, \quad m_x = \pm 1, 2, 3, \ldots \tag{2.38}$$

$$k_y = \frac{m_y \pi}{L_y}, \quad m_y = \pm 1, 2, 3, \ldots \tag{2.39}$$

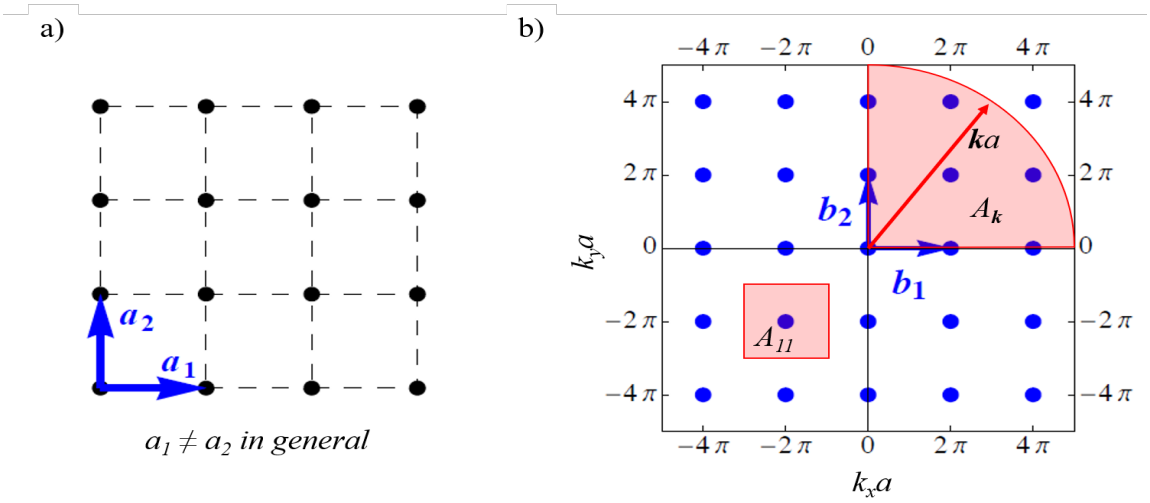

Figure 2.6: Illustration of (a) a 2D real space lattice and (b) a 2D reciprocal space lattice. In (b) the shaded quarter-circle represents the reduced $\mathbf{k}$-space area, $A_{\mathbf{k}}$, of filled states with crystal momentum less than $\mathbf{k}$, and the shaded square represents the area of a single-particle $\mathbf{k}$-space unit cell, A_{11}.

With this choice of boundary conditions we get standing wave solutions that are superpositions of states with $\pm\mathbf{k}$. Now, consider our two-dimensional $\mathbf{k}$-space as being separated into equal area cells, such as the one shown in Fig. 2.6, where each cell corresponds to a momentum pair (k_x, k_y) that the electron can have. But since opposite momentum states are equivalent, we only need to consider the first quadrant of the $\mathbf{k}$-space (red quarter-circle in Fig. 2.6). Given some energy $E(\mathbf{k})$ the area enclosed in the first quadrant is fixed by the wave vector $\mathbf{k}$, such that:

$$A_{\mathbf{k}} = \frac{\pi \mathbf{k}^2}{4} \tag{2.40}$$

We also know that electrons are fermions and must obey the Pauli exclusion principle. So, ignoring spin and valley degeneracies, each cell can only be occupied by a single electron. The area of a single-state $\mathbf{k}$-space unit cell A_{11} is given by ($m_x = m_y = 1$):

$$A_{11} = \left(\frac{\pi}{L_x}\right)\left(\frac{\pi}{L_y}\right) = \frac{\pi^2}{A} \tag{2.41}$$

Dividing Eq. 2.40 by Eq. 2.41, we get the total number of states available to the electron with wave vector less than $\mathbf{k}$:

$$N = \frac{A_{\mathbf{k}}}{A_{11}} = \frac{\mathbf{k}^2 A}{4\pi} = \frac{\left(\frac{2m^* E}{\hbar^2}\right) A}{4\pi} = \frac{m^* A}{2\pi\hbar^2} E \tag{2.42}$$

Differentiating N with respect to E, and dividing by the total area, A, gives us the number of states per unit area per unit energy. This is the DoS, and for a 2D system (in a

single valley and ignoring spin) is given by:

$$g_{2D}(E) = \frac{1}{A}\frac{dN}{dE} = \frac{m^*}{2\pi\hbar^2} \tag{2.43}$$

Remarkably, the 2D DoS does not depend on energy. Of course we know that we must account for spin and valley degeneracies, so to do this we simply multiply $g_{2D}(E)$ by the degeneracy factor $g = g_v g_s$. Furthermore, we can consider the z-component ground state energy E_0^z to be equal to the bottom of the conduction band E_c. Thus, $E \longrightarrow E - E_c$ and $g(E) \longrightarrow g(E - E_c)$. Since electronic states are forbidden inside the band gap, the DoS becomes:

$$g_{2D}(E - E_c) = \begin{cases} 0 & E < E_c \\ g_v g_s \frac{m^*}{2\pi\hbar^2} & E \geq E_c \end{cases} \tag{2.44}$$

Thus upon reaching the conduction band, there are a large number of states available to the 2D electron.

2.1.9 Landau levels

So far, I have discussed the physics of a non-interacting 2DES in the absence of external magnetic fields. Given a zero-field 2DES with a constant DoS (§ 2.1.8), when we turn on a magnetic field the electrons will organize themselves by filling Landau levels and the DoS will change. The Hamiltonian for a single electron confined to move freely in the x-y plane and in the presence of an external magnetic field is given by:

$$H = \frac{1}{2}(\hat{\mathbf{p}} - e\mathbf{A}) \cdot \mathbf{W} \cdot (\hat{\mathbf{p}} - e\mathbf{A}) + U(z) \tag{2.45}$$

where $\hat{\mathbf{p}}$ is the momentum operator, $\mathbf{A}$ is the vector potential, and $U(z)$ is the confining potential energy from Eq. 2.30. Since we are interested in what happens to electrons confined on the Si surface, let us choose a convenient gauge to work in, the Landau gauge, such that we have $\mathbf{A} = (0,\, B\hat{x},\, 0)$, where $\hat{x}$ is the x-position operator. This gives a magnetic field $\mathbf{B} = \nabla \times \mathbf{A} = (0,\, 0,\, B)$ which is perpendicular to the surface. Let us also take $\mathbf{W} \longrightarrow (m^*,\, m^*,\, m_{zz})$, so that the Hamiltonian then becomes:

$$H = \frac{\hat{p}_x^2}{2m^*} + \frac{(\hat{p}_y - eB\hat{x})^2}{2m^*} + \frac{\hat{p}_z^2}{2m_{zz}} + U(z) \tag{2.46}$$

We know classically that electrons subjected to a magnetic field follow cyclotron orbits with the cyclotron frequency given by $\omega_c = \frac{eB}{m^*}$. Additionally, because the y-position operator, $\hat{y}$, is absent from the Hamiltonian, we can replace $\hat{p}_y$ with its eigenvalue, $\hbar k_y$, which gives:

$$H = \frac{\hat{p}_x^2}{2m^*} + \frac{(\hbar k_y - m^*\omega_c\hat{x})^2}{2m^*} + \frac{\hat{p}_z^2}{2m_{zz}} + U(z) \tag{2.47}$$

Rearranging and letting $x_0 = \frac{\hbar k_y}{m^*\omega_c}$, where x_0 is the center of the cyclotron orbit, the final form of the Hamiltonian in the Landau gauge is:

$$H = \left[\frac{\hat{p}_x^2}{2m^*} + \frac{1}{2}m^*\omega_c^2(\hat{x} - x_0)^2\right] + \left[\frac{\hat{p}_z^2}{2m_{zz}} + U(z)\right] \tag{2.48}$$

The two terms in the first bracket of the Hamiltonian are that of a quantum harmonic oscillator, while the two terms in the second bracket are of the same form as the summation in Eq. 2.32. As expected, the z-component of the Hamiltonian is decoupled from the cyclotron motion and does not contribute to the Landau level energies, except for an overall

constant E_0^z (see Eq. 2.35). This is the ground state energy of the zero-field 2DES, or the bottom of the conduction band, E_c. Thus, the total energy of the Landau level system is given by:

$$E_m = E_c + \hbar\omega_c \left(m + \frac{1}{2}\right),\ m = 0, 1, 2... \tag{2.49}$$

Because of our choice of gauge, the x- and y-components are also decoupled from one another. Thus, the in-plane wavefunction for the Laudau level system can be written as a product of the two coordinate-separated components:

$$\phi_{LL}(x,y) = \psi_{m,k_y}(x - x_0)\psi_{k_y}(y) = \psi_{m,k_y}(x - x_0)e^{ik_y y} \tag{2.50}$$

where $\psi_{k_y}(y)$ is a plane wave modulated by an envelope function $\psi_{m,k_y}(x - x_0)$, which is a function describing the harmonic oscillation.

The Landau level system is characterized by quantum numbers m and k_y. However, because I am considering the non-interacting picture (E depends only on m), the Landau levels are highly degenerate. To see how degenerate, we must consider the constraints on k_y. The plane wave component of the wavefunction $\psi_{k_y}(y)$ must return to its original value after an in-plane 2π rotation, thus, $k_y = \frac{2\pi n}{L_y}$, where $n = 1, 2, ..., N$ is an integer. Each n represents an available state, thus for N electrons, the maximal value of k_y becomes $k_y = \frac{2\pi N}{L_y}$. For a 2DES confined to an area $A = L_x L_y$, we know that the cyclotron orbits must be physically contained in A, thus we have the following constraint on x_0 that $0 \leq x_0 \leq L_x$, which is essentially a constraint on N:

$$0 \leq N \leq \frac{m^* \omega_c L_x L_y}{2\pi\hbar}, \tag{2.51}$$

thus the number of electrons per maximally filled Landau level is:

$$N = g_v g_s \frac{m^* \omega_c A}{2\pi\hbar}, \tag{2.52}$$

where we have included the spin and valley degeneracy factors as we did before. Recalling from § 2.1.8 that the DoS is defined as the number of states per unit area per unit energy, we can write down the DoS for electrons in a magnetic field as, $g_{2D}(E - E_c, \omega_c > 0) = \frac{N}{A}$, and comparing to the zero-field DoS (Eq. 2.44), we get:

$$g_{2D}(E - E_c, \omega_c) = \begin{cases} 0 & E < E_c,\ \omega_c = 0 \\ g_v g_s \frac{m^*}{2\pi\hbar^2} & E \geq E_c,\ \omega_c = 0 \\ 0 & E \neq E_m,\ \omega_c > 0 \\ g_v g_s \hbar\omega_c \frac{m^*}{2\pi\hbar^2} & E = E_m,\ \omega_c > 0 \end{cases} \tag{2.53}$$

Because Landau levels are quantized, they form a type of band structure with discrete allowed energy states. Furthermore, at non-zero temperatures and in the presence of disorder, the Landau level degeneracy is lifted and the once discrete bands undergo level broadening given by $\Gamma = \frac{\hbar}{\tau}$, where τ is the average lifetime between electron scattering events. For $\Gamma << \hbar\omega_c$, the Landau levels remain separated but smeared symmetrically about each E_m. For $\Gamma \approx \hbar\omega_c$, the Landau levels are significantly mixed. When Γ increases above $\hbar\omega_c$, the Landau levels become broader, until the zero-field density of states is recovered in the limit $\frac{\Gamma}{\hbar\omega_c} \longrightarrow \infty$. Figure 2.7 illustrates the magnetic field dependence of the 2D DoS with and without the disorder parameter Γ.

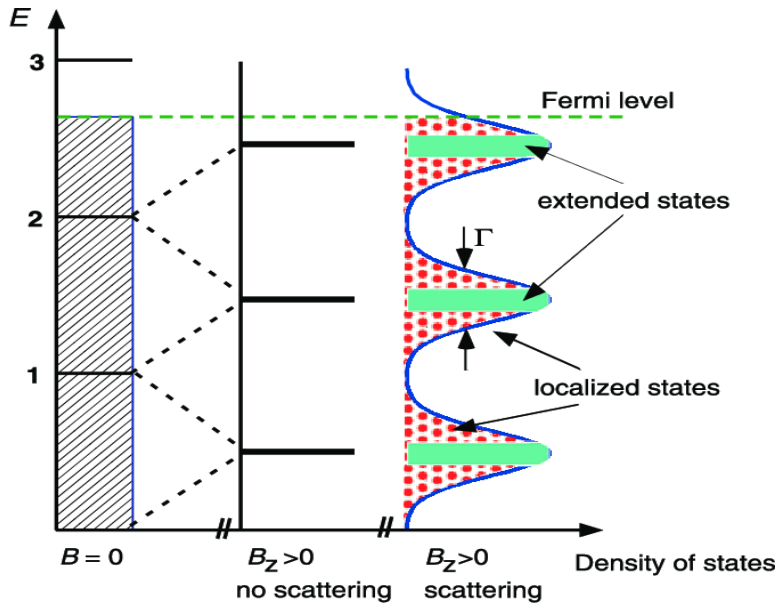

Figure 2.7: Density of states for a zero-field 2DES (**B** = 0) and a finite-field 2DES (**B** > 0). For the case $\Gamma = 0$, the Landau levels are localized at discrete levels. The introduction of disorder $\Gamma > 0$ causes the Landau levels to broaden.

2.1.10 2D carrier conductivity

Now finally, consider the collective motion of the electrons under the influence of electric field **E** parallel to the 2D surface. The current density **J** through a 2D material under the influence of an electric field **E** can be written as:

$$\mathbf{E} = \rho_{2D}\mathbf{J} \tag{2.54}$$

where ρ_{2D} is the resistivity tensor given by:

$$\rho_{2D} = \begin{pmatrix} \rho_{xx} & \rho_{xy} \\ \rho_{yx} & \rho_{yy} \end{pmatrix} \tag{2.55}$$

For $\hbar/\tau << E_F$, I can use the Drude model to find the equation of motion for a system

of non-interacting electrons [113]:

$$\mathbf{M}_j \mathbf{v}_j = e^2 \tau \mathbf{E} + e\tau(\mathbf{v}_j \times \mathbf{B}) \tag{2.56}$$

where v_j is the drift velocity of an electron in the j^{th} valley, and $\mathbf{B}$ is the magnetic field. This model has been found to be accurate for temperatures below 3 K. Following Ref. [113], if we let the current contributions from each valley be $J_j = n_j v_j$ and combine Eqs. 2.54 and 2.56, the 2D resistivity tensor for a 2DES on the Si(111) surface with all valleys equally occupied is given by:

$$\rho_{2D} = \frac{\eta}{en} \begin{pmatrix} \frac{\bar{m}}{e\tau} & B_z \\ B_z & \frac{\bar{m}}{e\tau} \end{pmatrix} \tag{2.57}$$

where η is an ideality factor given by:

$$\eta = \frac{1 + (\omega_c \tau)^2}{\Phi + (\omega_c \tau)^2} \tag{2.58}$$

and $\Phi = (\bar{m}/m^*)^2$, where $\bar{m} = \frac{m_x + m_y}{2}$. In the limit that $\omega_c \to 0$, $\eta < 1$ and for $\omega_c \to \infty$, $\eta \to 1$. In general, the valleys will not be equally occupied, due to valley splitting, which leads to anisotropy in the 2D resistivity, with $\rho_{xx}/\rho_{yy} \neq 1$. We do not see significant anisotropy in our 2DES resistivity measurements performed at 77 K, as the model breaks down above about 3 K. However, we would expect to see this behavior as we cool our devices down below 4.2 K. Finally, in the presence of a magnetic field, $\rho_{xy} = \rho_{yx} = \eta B_z/en$, gives the transverse, or Hall resistance which is discussed in § 2.2.2.

2.2 Measuring 2DES magnetotransport

At this point we have all the necessary information to understand the basic physics of a 2DES, but now we actually want to measure the 2DES and extract useful information, such as sheet resistance, carrier density, and mobility. In order to do this, we need to develop a measurement tool kit that allows us to probe the 2DES, and we need to understand the various experimental knobs that we have at our disposal.

Luckily for the reader, we only have one tool in our measurement toolbox to discuss: the four-terminal resistance of the 2DES. There are actually two tools, the other being capacitance measurements, but we will not concern ourselves with that technique here. What makes this lone tool so powerful, however, is the fact that we can measure the four-terminal resistance under a variety of conditions by varying external parameters such as carrier density n, the magnetic field $\mathbf{B}$, and the temperature T. The way we measure the four-terminal resistance of the 2DES is to source a known current through the device using two leads and measure a voltage drop across the device using the other two leads. In practice, even though we are actually measuring a voltage, we say that we are measuring a resistance because it is a more useful quantity. Consider both four-terminal contact arrangements in Fig. 2.8. We will be referring to this figure in the following subsections.

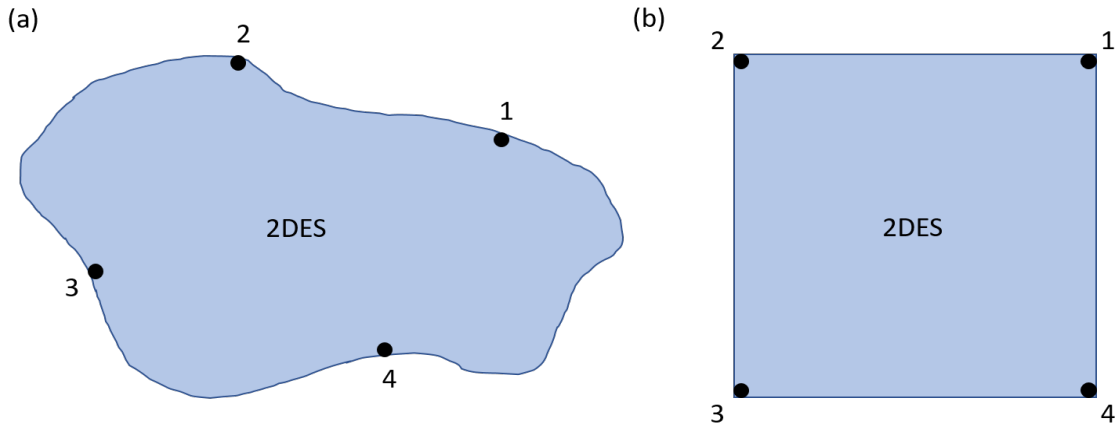

Figure 2.8: Illustrations of a four-terminal contact arrangement for a 2DES with (a) an arbitrary, asymmetric geometry and (b) a symmetric, square geometry.

2.2.1 Longitudinal resistance

The longitudinal resistance R_{xx} is the simplest four-terminal resistance to measure. It is called longitudinal because the voltage is measured along the same direction as the current I, hence the double-x subscript. Referring to Fig. 2.8, if a current is passed from contact 1 to contact 2, and a voltage is measured between contact 4 and contact 3, can define a longitudinal resistance, $R_{12,43}$, as:

$$R_{12,43} = \frac{V_4 - V_3}{I_{12}} \tag{2.59}$$

2.2.2 Hall resistance

The Hall resistance (or transverse resistance) R_{xy} is found by measuring a voltage that is transverse to the direction of the passing current, hence the x-y subscript. Referring to Fig. 2.8, if a current I is passed from contact 1 to contact 3, and a voltage is measured between contact 2 and contact 4, can define a Hall resistance, $R_{13,24}$, as:

$$R_{13,24} = \frac{V_2 - V_4}{I_{13}} \tag{2.60}$$

Under zero-field conditions ($\mathbf{B} = 0$) and barring voltage offsets, the Hall resistance for symmetric geometries is typically zero. Once we turn on a magnetic field perpendicular to the 2DES, however, charge begins to be deflected, with opposite-sign charge carriers building up on either side of the passing current, leading to a non-zero Hall resistance.

2.2.3 Van der Pauw method

The Van der Pauw (VdP) method is a four-point probe technique that allows one to measure the resistivity of a material or system of arbitrary geometry. For a two-dimensional system, this method yields the sheet resistance R_s, which is measured in $\Omega/\square$ (Ohms per square). For this method, we need to measure two longitudinal resistances that must satisfy the Van der Pauw equation [184]:

$$e^{-\pi R_{horizontal}/R_s} + e^{-\pi R_{vertical}/R_s} = 1 \tag{2.61}$$

where $R_{horizontal}$ could be any of four horizontal longitudinal resistances, such as $R_{43,12}$ or $R_{21,34}$, and $R_{vertical}$ could be any of four vertical longitudinal resistances, such as $R_{23,14}$ or $R_{41,32}$ (see Fig. 2.8). Eq. 2.61 does not have a nice analytic form when solving for R_s, however, it can also be expressed as:

$$R_s = \frac{\pi}{\ln(2)} \frac{R_{horizontal} + R_{vertical}}{2} F \tag{2.62}$$

where F is a correction factor that must be solved for numerically and is a function only of the ratio, $r = R_{horizontal}/R_{vertical}$ (for $R_{horizontal} > R_{vertical}$). F can be obtained by solving:

$$\frac{r-1}{r+1} = \frac{F}{\ln(2)} \operatorname{arccosh}\left(\frac{e^{\frac{\ln(2)}{F}}}{2}\right) \tag{2.63}$$

It can easily be shown that for a symmetric geometry, such as in Fig. 2.8(b), when $R_{horizontal} = R_{vertical} = R_{xx}$ that R_s simplifies to:

$$R_s = \frac{\pi}{\ln(2)} R_{xx} \tag{2.64}$$

There are many subtleties when using the VdP method, including error corrections for contact size and sample thickness. For a detailed discussion of the VdP method, I point the reader to Schroeder (2006) [184].

2.2.4 Parameter phase space

There are three primary parameters that can be varied while measuring our devices: the 2D electron density n, the magnetic field $\boldsymbol{B}$, and the temperature T. The electron density is controlled by a global gate and is directly proportional to the applied global gate voltage, V_G. Using a parallel plate-capacitor model, we can write the 2D electron density n as:

$$n = \frac{C}{e} V_G \tag{2.65}$$

where C is the geometric capacitance per unit area between the 2DES and the global gate. Typical operating densities for our devices range from $\sim 10^{11} - 10^{12}$ cm^{-2}, which correspond to global gate voltages between about 1 V and 30 V.

With the introduction of a magnetic field, we can make Hall measurements which yield such important information as the carrier density (which can be compared to Eq. 2.65). From Hall measurements we also get the Hall coefficient R_H, which relates the current in the x-direction, the Hall voltage in the y-direction and the magnetic field in the z-direction with the 2D electron density n and is given by:

$$R_H = \frac{V_H}{I_x B_z} = \frac{1}{en} \tag{2.66}$$

Other important quantities that can be extracted from measurements include the electron mobility μ, which is one metric we use for determining how pristine the H-Si(111)

surface is. If we find the electron density from a Hall measurement and the sheet resistance using the VdP method, we can extract an electron mobility:

$$\mu = \frac{R_H}{R_s} = \frac{1}{enR_s} \tag{2.67}$$

We can also deduce information about the thermally-averaged carrier lifetime, $\langle\tau\rangle$, which is related to the 2D conductivity σ_{2D} (or the reciprocal of the sheet resistance), and is given by [68]:

$$\sigma_{2D} = \frac{1}{R_s} = \frac{ne^2\langle\tau\rangle}{m^*} \tag{2.68}$$

The final experimental knob that we can twist is the temperature of the device. The temperature essentially sets one of the important the energy scales for the phenomenon that we are trying to observe. For example, the thermal energy available to an electron in the system is k_BT, and the Landau level splitting is $\hbar\omega_c$. Thus, if we wish to resolve individual quantized levels when performing four-terminal resistance measurements, we expect that we will need to be in the temperature regime such that $\hbar\omega_c >> k_BT$. Likewise, as I will discuss in Ch. 6, to resolve spin-orbit effects on I-Si(111), we must be in the temperature regime such that $\Delta E_{SO} >> k_BT$. A good rule of thumb when comparing energy scales $\mu_B B$, eV, and $\hbar\omega$, to the thermal energy k_BT is: 1 K $\sim$ 1 T $\sim$ 0.1 mV $\sim$ 130 GHz. There are other parameters that one could vary, such as the tilt of the magnetic field, or the strain of the sample, but I did not consider these parameters in my work.

2.3 Topology: an aside

Topology is the mathematical study of smooth, continuous (i.e. differentiable) deformations to geometric systems in which certain properties remain unchanged. The most

common example to illustrate topology is to imagine objects with a number g of physical holes, where g is known as the genus. A sphere, no matter how much it is smoothly deformed (no punctures, no gluing), will always have zero holes, or $g = 0$. Likewise, a torus under any smooth deformation will always have exactly one hole or $g = 1$. In 1982, Thouless et al. proposed a new type of ordering for material phases: topological order [185]. Topological order, in brief, describes a class of materials and systems, including topological insulators (TI), in which the band structures can be labeled with topological quantum numbers called Chern invariants.

2.3.1 The Chern invariant and the Berry phase

A 2D band structure is produced when crystal momentum $\mathbf{k}$ living on a 2-torus, is mapped to the Bloch Hamiltonian $H(\mathbf{k})$ [133]. Smooth changes in the material parameters, namely $\mathbf{k}$, that modify the band structure, but do not lead to gapless states or a crossing of occupied and unoccupied bands, form a set of topologically equivalent Bloch Hamiltonians. Each set of Hamiltonians that can be continuously deformed into one another without closing a gap can be assigned a Chern invarient, $m \in \mathbb{Z}$, given by:

$$m = \frac{1}{2\pi} \iint d^2\mathbf{k}\, \mathcal{F}(\mathbf{k}) \tag{2.69}$$

where $\mathcal{F}(\mathbf{k})$ is the total Berry flux through the Brillioun zone. The Berry flux, or Berry curvature as it is also commonly known, is the curl of the Berry connection, $\mathcal{F}(\mathbf{k}) = \nabla \times \mathcal{A}(\mathbf{k})$, analogous to the relationship between the magnetic field and the vector potential in classical electromagnetism. Here, the Berry connection $\mathcal{A}(\mathbf{k})$ determines the geometric phase that a wavefunction acquires when its Hamiltonian is adiabatically cycled through configuration space along a closed-loop path. For the Bloch Hamiltonian, if we adiabatically cycle our system along a closed-loop path through $\mathbf{k}$-space such that

$H(\mathbf{k}_i) \longrightarrow H(\mathbf{k}_f)$ where $\mathbf{k}_f = \mathbf{k}_i$, then our Bloch wavefunction picks up a geometric phase factor:

$$\Psi_f(\mathbf{k}) = e^{i\gamma}\,\Psi_i(\mathbf{k}) \tag{2.70}$$

where γ is called the geometric phase, or Berry phase, and is given by:

$$\gamma = \oint_C d\mathbf{k}\,\mathcal{A}(\mathbf{k}) = \iint_S d^2\mathbf{k}\,(\nabla \times \mathcal{A}(\mathbf{k})) \tag{2.71}$$

In Eq. 2.70, I omitted the dynamic phase factor acquired under time evolution for brevity. Comparing Eq. 2.69 to Eq. 2.71, we see a simple relationship between the geometric phase arising from $\mathbf{k}$-space trajectories and the rich topological structure revealed by the Chern invariant, which is equal to the Berry phase modulo 2π, or $2\pi m = \gamma$.

One way to illustrate this is to consider a trajectory along a $\mathbf{k}$-space path on a 2-torus that begins and ends at the same point. Any path that traverses through the 2-torus hole (without returning back through) and reconnects to the initial $\mathbf{k}$-point must fully wind around the axial body of the 2-torus at least once, representing a 2π rotation about that axis. The number of windings about the 2-torus axis that complete the trajectory in this manner *must* be an integer and is indeed equal to the Chern invariant m, with the Berry phase γ representing total rotation angles. From a solid-state perspective, we can think of the Chern invariant as the number of times a band gap between occupied and unoccupied bands must close and reopen before we arrive at a normal insulator state. For a normal insulator (SiO_2, vacuum, etc), the band gap is finite everywhere, and the Chern invariant is $m = 0$, thus extending our typical notion of a normal insulator to be a smaller subset of a much larger class of topological insulators.

2.3.2 The integer quantum Hall effect

The most important topology can be understood by considering an example from arguably one of the most important discoveries in solid state physics: the integer quantum Hall effect (IQHE). In 1980, von Klitzing showed that when a 2DES is subjected to strong magnetic fields at low temperature, the Hall conductance σ_{xy} becomes exactly quantized [186]:

$$\sigma_{xy} = \nu \frac{e^2}{h} \tag{2.72}$$

where ν is an integer. Even more surprising was the fact that this exact quantization of the Hall conductance is extremely robust against perturbations from defects and disorder [187]. The robust quantization of σ_{xy} was elucidated when Thouless et al. reformulated the IQHE using the Kubo formula and showed that ν in Eq. 2.72 is *exactly* the same as m in Eq. 2.69 [185]! The IQHE was thus the first example of a new phase of topological matter that has a non-zero Chern invariant. The robustness of the effect aries because smooth transformations (perturbations) of the Hamiltonian cannot change the Chern invariant. Furthermore, it was realized that when two topological insulators with different Chern invariants are brought together, there must be a phase change across the boundary, which inevitably requires band gap closure and leads to dissipationless and chiral edge modes at the interface [133]. This is exactly what happens in the IQHE when a 2DES in a magnetic field ($m = \nu \neq 0$) abutts a normal insulator ($m = 0$) at the sample edge. The connection between the IQHE and topology led to enormous efforts both theoretically and experimentally to understand these new classes of topological materials [133–137], and there remains a vast horizon for future exploration.

What does all of this mean for experimental device physics? Well, the Chern invariant is a good quantum number under local perturbations of the Bloch Hamiltonian, so long

as those perturbations do not close a gap. While we typically think about observables such as spin or momentum representing coherent quantum states that possess good quantum numbers, the Chern invariant is another good quantum number we can now attach to our system. From a device standpoint, this opens the door to new classes of devices in which coherent quantum systems can be engineered to be topologically protected from decoherence due to local perturbations. For example, we can think about creating devices that house topologically protected two-level systems that could be used for topological quantum computation [139, 140].

Chapter 3: Non-invasive SOI-based devices

The central aspect of my research was the development of an electrostatic gating method that was completely non-invasive to the pristine surface under study. This was accomplished by realizing an architecture in which all dopants, metals, and harsh device processing were moved from the pristine surface to an adjacent SOI gate chip [188]. Methods for the non-invasive gating of pristine materials have, of course, been demonstrated before in which the ohmic contacts reside on the pristine surface and the electrostatic gates reside on a separate chip [101, 189]. What is notable about the new architecture that I developed, however, is that the electrostatic gates *as well as* the ohmic contacts, are placed on the SOI piece. This distinction delineates the first truly non-invasive electrostatic gating method for probing 2D electron systems on pristine materials, and in particular pristine, chemically-terminated, intrinsic-Si surfaces. This offers a non-invasive approach to the electrostatic gating of pristine materials to create and control 2D, and potentially 1D and 0D, micro- and nano-structures that are traditionally fabricated directly on a semiconductor surface. The ideas for this approach did not arise in a vacuum, of course, but rather are an extension and continuation of the ideas developed in the Kane lab by Eng, McFarland, Kott, and Hu. A brief summary of this prior work is provided in the next section.

3.1 A brief history of Si(111) Van der Waals devices

About ten years prior to my arrival at the Laboratory for Physical Sciences, Eng was developing the first generation of Si flip-chip devices in an attempt to probe 2D transport on H-Si(111) surfaces using a vacuum FET approach. The goal was to obtain high-

mobility Si surfaces in order to observe the integer and fractional quantum Hall effects, and to do so by encapsulating carefully prepared H-Si(111) surfaces in vacuum [106].

In his design, seen in Fig. 3.1, Eng used an SOI gating structure which served solely as a global gate to induce electron accumulation. The top of the handle-Si layer was doped through a deep boron implant in order to create the conductive gate layer, while the top-Si layer was doped via a shallow boron implant to act as a shield layer to define the 2DES. The ohmic contacts resided on the H-Si(111) piece and were fabricated through direct phosphorous doping of the Si surface. They were quite large in size and accessed a large-area 2DES that was around 1 mm^2. Early experiments by Eng and McFarland reported mobilities of roughly 8,000 cm^2/Vs at liquid helium temperatures and 24,000 cm^2/Vs at 300 mK – record mobilities for H-Si(111) at the time [106, 108].

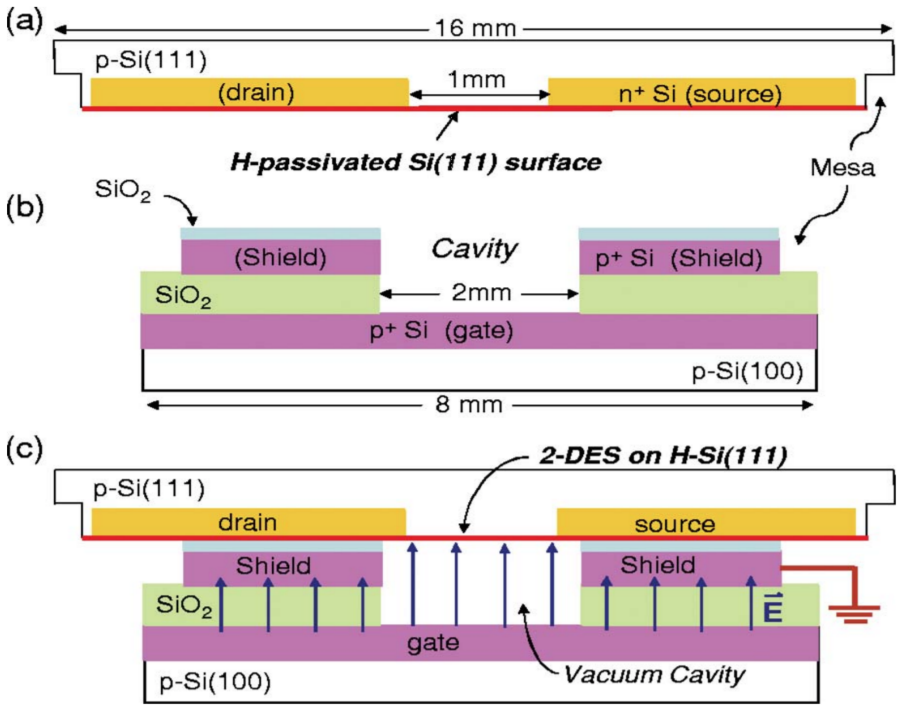

Figure 3.1: Illustration of the first generation SOI gating structure developed by Eng (from Ref. [106]): (a) H-Si(111) piece with phosphorus doped ohmic contacts, (b) the SOI gate piece with top-Si shields to define the 2DES on the H-Si(111) surface, (c) the Van der Waals bonded device. Ohmic contacts (n^+ Si) are shown in yellow, BOX in green, global gate and shield in purple, and Si in white. A forward bias applied to the global gate results in electron accumulation on the H-Si(111) surface.

Eventually, McFarland and Kott took up the reigns and improved upon the surface preparation. In doing so, they were able to achieve even higher electron mobilities of 325,000 cm^2/Vs – the current record for H-Si(111) surfaces [107]. They went on to explore the temperature dependence and valley degeneracy breaking mechanisms of 2DESs on these surfaces. In their investigations, they observed well-developed fractional quantum Hall hierarchies and electron-electron interactions in these highly-correlated systems [107, 109].

The next in line to take over the direction of the device design was Hu. Prior to his work, interest in studying two dimensional hole systems (2DHSs) had piqued, due to the success of studying 2DESs on these surfaces. To this end, Hu, McFarland, and Kott then employed the same device architecture in Fig. 3.1 to look at 2DHSs on H-Si(111) surfaces [110, 111].

Hu subsequently modified the device architecture in two ways [112], as seen in Fig. 3.2. First, the SOI gate/shield piece was replaced by a SiO_2-Si(100) gating chip with a vacuum cavity. It was found that global gate leakage, which had been a significant problem with early generation devices, was greatly improved due to the full coverage of the gating chip with SiO_2. Second, the four ohmic contacts in the old architecture were replaced with six P contacts (aligned along the six equivalent valley projections) which were interdigitated with six B contacts. Both sets of the six n-type and p-type ohmic contacts served dual purposes. The first was to supply the 2D region with either electrons (n-type) or holes (p-type) while the other set served as the electrostatic confinement and ohmic contact isolation for either the 2DES or 2DHS. For positive applied global gate voltages, electrons accumulated on the H-Si(111) surface, allowing the six n-type ohmic contacts to electrically access the 2DES while the p-type contacts confined the 2DES to a VdP configuration. For negative applied global gate voltages, holes accumulated on the H-Si(111) surface, and the ohmic contact roles were reversed. This new architecture paved the way for the first ambipolar device structure on H-Si(111) which could probe both electrons and holes in the same

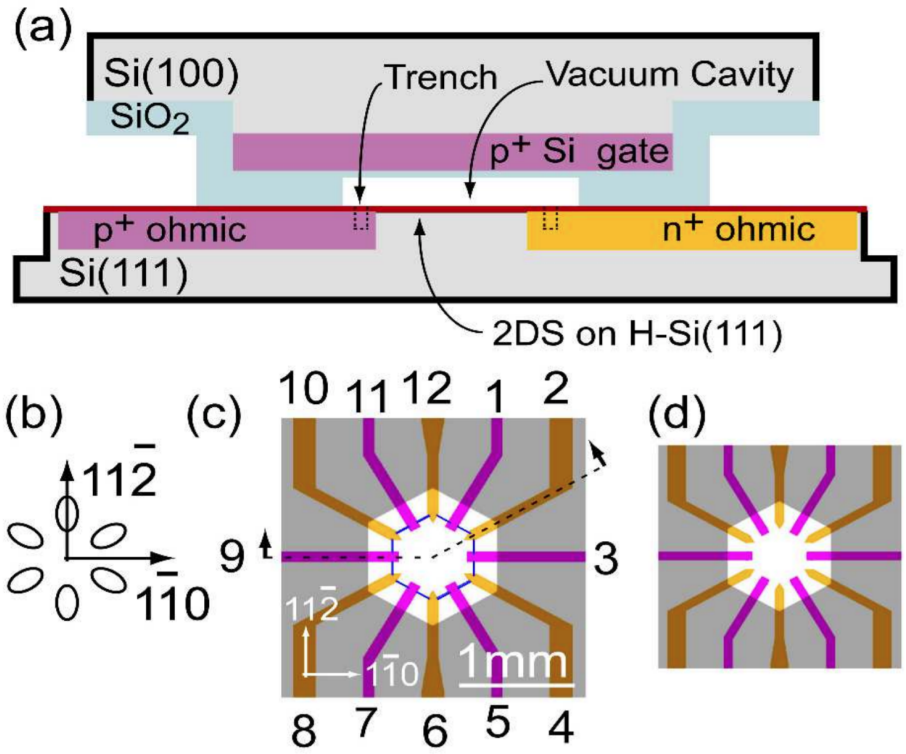

Figure 3.2: Illustration of the ambipolar device architecture developed by Hu (from Ref. [112]): (a) the Van der Waals bonded device with the cross-section cut-line defined in (c), (b) a schematic of the six valley projections onto the Si(111) surface, (c)-(d) the twelve ohmic contacts (six P contacts and six B contacts) labeled in clockwise order. The P ohmic contacts (n^+ Si) are shown in yellow and are aligned with the six valley projections, the B ohmic contacts (p^+ Si) shown in purple, SiO_2 in blue, global gate in purple, and Si in gray. A positive (negative) bias applied to the global gate results in electron (hole) accumulation on the H-Si(111) surface.

system. Furthermore, due to the alignment of the six n-type contacts along the valley projections, the six-fold valley degeneracy of the system could be investigated more directly.

It had been known since the first development of this novel device architecture that ohmic contacts fabricated directly onto the surface of the H-Si(111) piece could be a potential source of contamination and disorder for the 2DES. It was noted that this could limit the functionality of devices as dimensions were scaled down to the nano-scale. To this end, one of the primary goals in developing the non-invasive SOI-Si architecture described in this dissertation was to remove all dopants from the Si surface, allowing a path

forward for the miniaturization of the device dimensions.

3.2 Architecture overview

Two similar yet distinct architectures are detailed in the following subsections. The first iteration of my non-invasive SOI devices were the simplest possible proof-of-concept devices: two-terminal devices with large-area ohmic contacts for bonding, illustrated in Fig. 3.3. By "two-terminal" I mean there are two ohmic contacts. Of course there are gate contacts, and in the more complicated four-terminal devices (see Fig. 3.4), also extra ohmic contacts and extra gate contacts. For my purposes, devices were categorized by the number of ohmic contacts they had. The SOI-based devices presented in this work are comprised of two individual pieces: an SOI piece and a minimally processed, or pristine, intrinsic H-Si(111) piece, that are Van der Waals bonded to one another at room temperature. The SOI piece houses all electrical components, including the ohmic contacts, the global gate, and (for the four-terminal devices) the proximity depletion gates (PDGs). This eliminated the need to subject the H-Si(111) piece to any harsh processing. The pristine H-Si(111) piece is host to the 2DES which is created through surface accumulation by the global gate in both the two- and four-terminal architectures. In the four-terminal architecture, the 2DES is confined to a Van der Pauw (VdP) geometry by the PDGs. The ohmic contacts on the SOI piece make physical and electrical contact with the pristine H-Si(111) piece, while all gates on the SOI piece are separated from the H-Si(111) surface by vacuum. Due to the equal isotropic expansion and contraction of the Si cubic lattices at the SOI-Si bonding interface, and because all non-Si components are far from the bonding interface, we do not expect strain to play a significant role in our devices. This is consistent with the fact that our devices remained bonded through many thermal cycles.

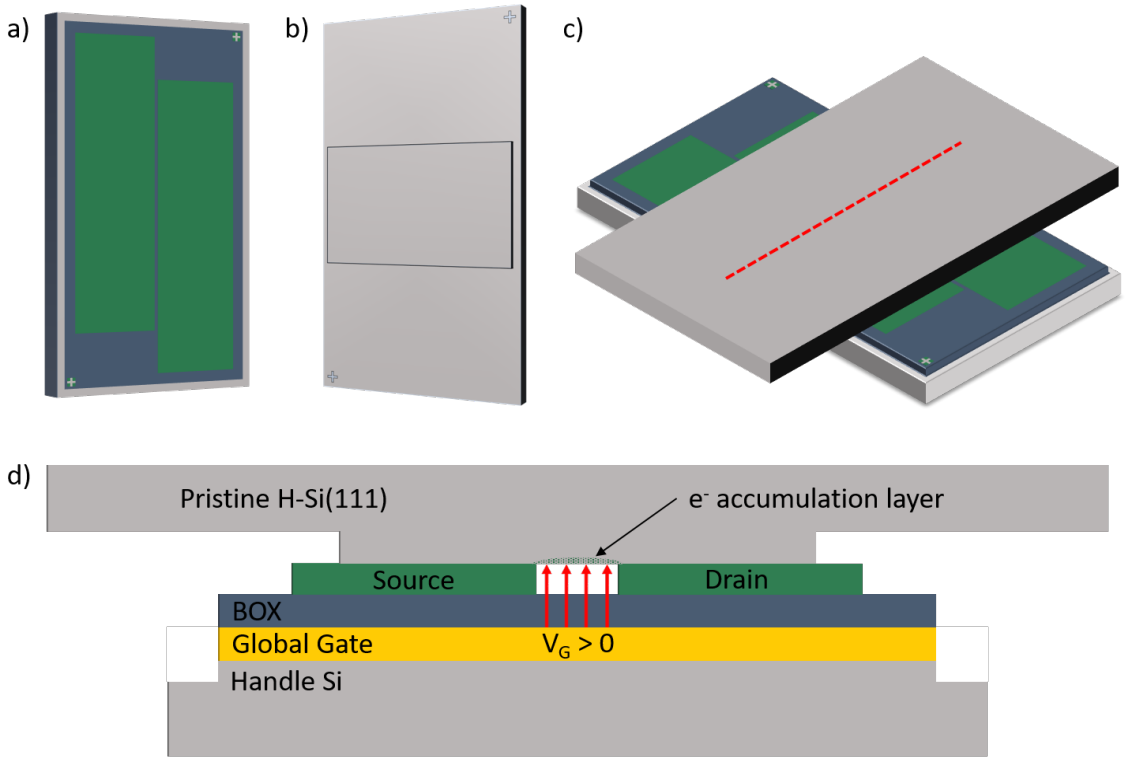

Figure 3.3: Illustration of the two-terminal device architecture. (a) The SOI piece housing all electrical components, (b) the pristine, intrinsic H-Si(111) piece, (c) the Van der Waals bonded device, and (d) a cross-sectional view of the bonded device along the red dashed line in (c). Ohmic contacts (n^+ Si) are shown in green, BOX in blue, global gate in yellow, and Si in gray. A positive voltage applied to the global gate results in electron accumulation on the H-Si(111) surface.

3.3 SOI two-terminal test devices

When the idea of a non-invasive SOI architecture was initially conceived, there were some concerns about whether or not the device would even be viable. Foremost among these concerns was whether electrical contact could be made between the samples, such that ohmic contact could be made to the 2DES. Traditional methods to make contact to a 2DES typically use some form of direct dopant or metal placement onto the 2D surface of interest. This makes electrical contact to the 2DES relatively straightforward and well understood. By contrast, an architecture in which the ohmic contacts must be brought into physical contact with the 2DES through Van der Waals bonding in order to make electrical contact is non-trivial. We were indeed able to make physical and electrical contact between the SOI and Si pieces, and the first hurdle in the experiment had been cleared. However, as we will see in Ch. 4, the electrical characteristics were not ideal at low temperatures.

Once a device is bonded and wired (see Fig. 3.5), it is ready to be mounted to a dip-stick apparatus for measurements. The sample is enclosed in a vacuum can that can be lowered directly into liquid nitrogen or liquid helium dewars (for measurement at 77 K or 4.2 K, respectively). At a given temperature, there are essentially three measurements that can be performed on these test devices:

1. Measure the global gate leakage I_G to the ohmic contacts.

2. Measure the source-drain current I_{sd} while holding a constant source-drain bias V_{sd} and sweeping the global gate V_G.

3. Measure the source-drain current I_{sd} while holding a constant global gate voltage V_G and sweeping the source-drain bias V_{sd}.

For each device, the first step was to check that we were actually connected to the gate layer. To do this, I wired two connections to the gate and simply used a multimeter to confirm that the circuit was not broken. Typical gate resistances for good connections

were about 30 Ω. Once I knew that the gate was connected, I always checked the gate leakage by tying the ohmic contacts to ground and sweeping V_G over a range of voltages. If the gate did not leak, I proceeded to measurements 2 and 3. The second measurement allowed me to measure the threshold voltage, while the third measurement determined if the conduction throughout the device was ohmic. At a given global gate voltage V_G above threshold, we ideally wanted a linear I-V relationship between the source and drain.

3.4 SOI four-terminal devices

My next task was to extend this architecture to four-terminals in order to make Van der Pauw and Hall measurements on our 2DES. To do this, I added two more ohmic contacts, as well as four additional metal gates, called proximity depletion gates (PDGs). These were placed on the SOI piece in between each ohmic contact, where they were recessed into the BOX and separated from the H-Si(111) surface by vacuum. The PDGs allow us to electrostatically define a Van der Pauw geometry in the accumulated electrons on the H-Si(111) surface through surface depletion.

After checking that the global gate is connected properly and that there is no leakage to the ohmic contacts, I proceeded with the following measurements:

1. Measure the leakage current I_{PDG} from the 2DES to the PDGs.

2. Measure the two-terminal source-drain current I_{sd} between any two ohmic contacts while holding a constant source-drain voltage V_{sd} or global gate voltage V_G and sweeping the other. This measurement yields R_{2T}.

3. Measure the four-terminal longitudinal resistance, R_{xx}.

4. Measure the four-terminal Hall resistance R_{xy} (with a magnetic field present).

5. Measure the four-terminal Van der Pauw sheet resistance R_s.

For these measurements, except for the initial leakage check in measurement 1, the PDGs were tied to ground to confine the electrons to a Van der Pauw geometry. As mentioned in § 2.2, the majority of the interesting physics seen in our devices is captured in measurements 3, 4, and 5, while varying parameters such as the carrier density n, the magnetic field $\boldsymbol{B}$, and the temperature T. These measurements will be discussed in Ch. 4.

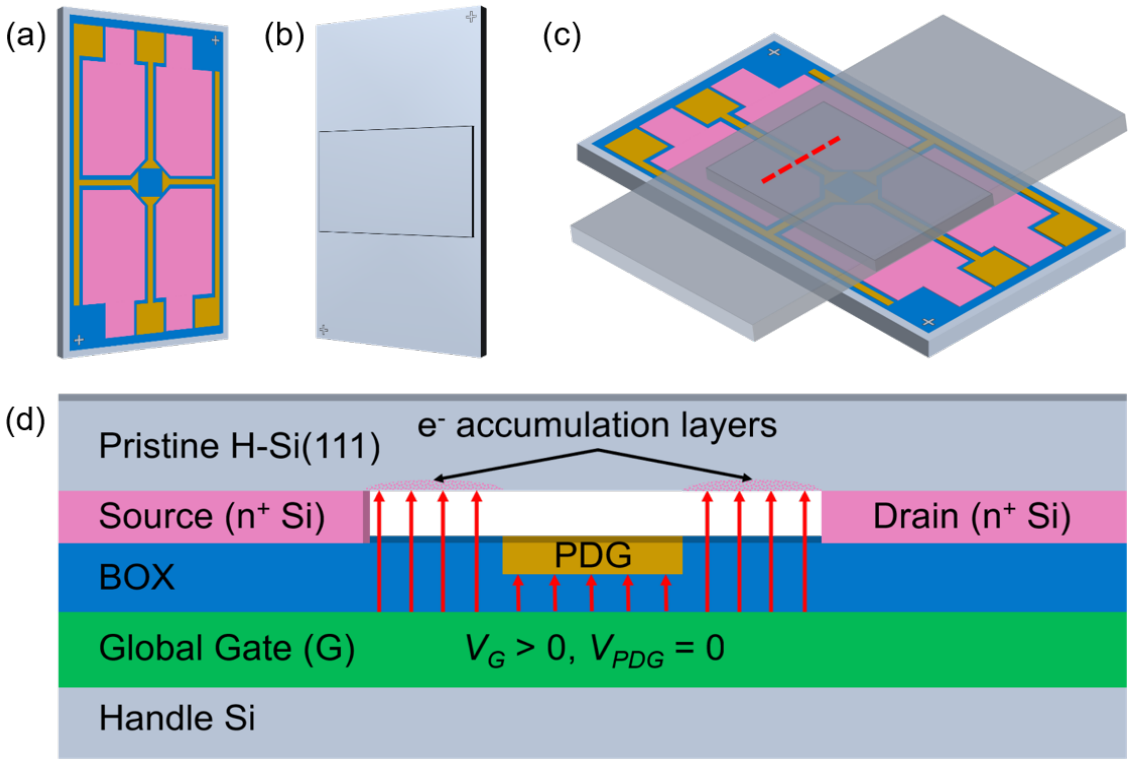

Figure 3.4: Illustration of the four-terminal device architecture. (a) The SOI piece housing all electrical components, (b) the pristine, intrinsic H-Si(111) piece, (c) the Van der Waals bonded device, and (d) a cross-sectional view of the bonded device along the red dashed line in (c). Ohmic contacts (n^+ Si) are shown in pink, BOX in blue, global gate in green, PDGs in gold, and Si in gray. A forward bias applied to the global gate results in electron accumulation on the H-Si(111) surface, except where the grounded, vacuum-separated PDGs block the E-field (solid red arrows), depleting the local region.

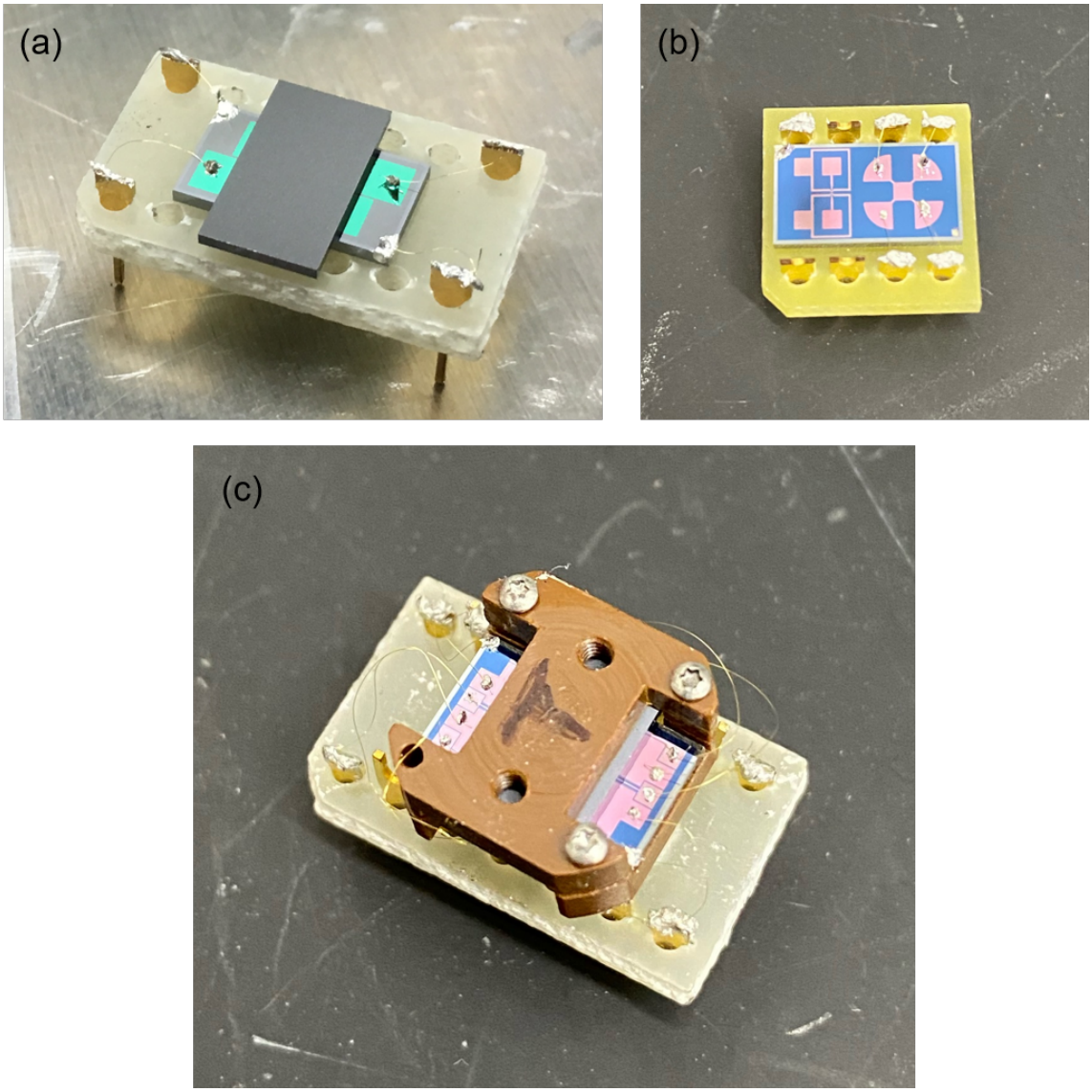

Figure 3.5: (a) Bonded and wired two-terminal device ready to be mounted to the dipstick. One wire is attached to each ohmic contact, and two wires are connected to the global gate (four total). (b) Wired cloverleaf device for measuring the ohmic contact sheet resistance. (c) Bonded and wired four-terminal device ready to be mounted to the dipstick. One wire is attached to each ohmic contact and each PDG, and two wires are connected to the global gate (ten total).

3.5 Device fabrication

The following sections detail the device fabrication, chemical preparation, and Van der Waals bonding of the two-terminal and four-terminal SOI-based devices. Full device recipes can be found in appendix A.

3.5.1 The SOI wafer

The SOI wafers that were used in the fabrication of the SOI gate chips were commercially available 300 mm (12 inch) wafers from Soitec, as seen in Fig. 3.6. These wafers were unique from other SOI wafers in that they came with a 3.5 μm n^+ heavily-doped epitaxial layer (2x10^{19} P/cm^3) already built in, which served as the global gate for our devices. The inclusion of this layer was not only beneficial from an ease of fabrication standpoint, but this also allowed me to forgo a deep implant step that was previously used to define the global gate in early generation devices – a step that could potentially damage the BOX layer and lead to global gate leakage.

The wafer layers nominally included an 88 nm thick top-Si layer (resistivity 15 Ω-cm), a 190 nm buried oxide (BOX) layer, and a 3.5 μm n^+ epitaxial layer (2x10^{19} P/cm^3), all on top of a standard handle-Si layer. 300 mm wafers are quite unwieldy, however, so we had these 12 inch wafers sent to Micro Precision Engineering to be laser-cut and resized to 100 mm (4 inch) wafers, yielding four 100 mm wafers for each 300 mm wafer. These wafers were also quite difficult to acquire. Soitec does not tend to manufacture specialty wafers for university level research, therefore these wafers were left over from a larger industrial order. Finding more wafers with similar specifications could require some luck; however, with persistence and sufficient funds, these wafers can be obtained.

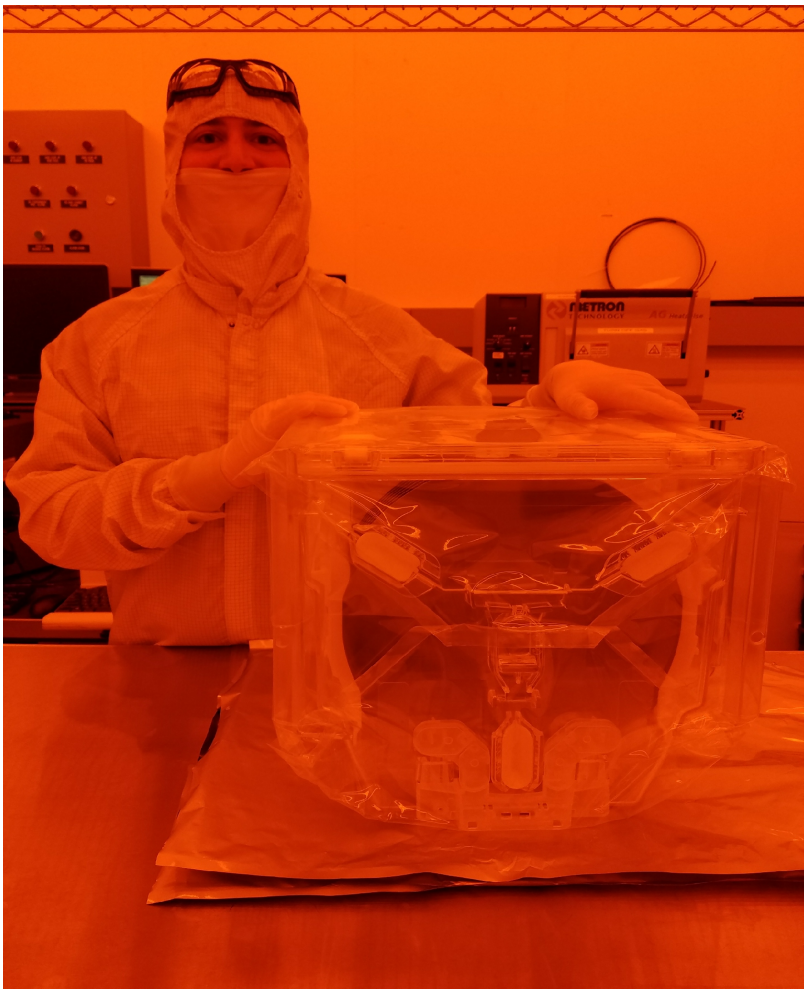

Figure 3.6: The 300 mm (12 inch) SOI wafers used for my device architecture, which were subsequently resized to 100 mm (4 inch) wafers. The wafer layers nominally included an 88 nm thick top-Si layer (resistivity 15 Ω-cm), a 190 nm buried oxide (BOX) layer, and a 3.5 μm n^+ epitaxial layer ($2x10^{19}$ P/cm^3) all on top of a standard handle-Si layer. Me grinning for scale.

3.5.2 The SOI piece

The SOI piece (see Figs. 3.3(a) and 3.4(a)) was fabricated on a 4-layer prime-grade 100 mm SOI wafer (Soitec, (100), SmartCut) as discussed in the previous section. The SOI wafer was controllably thinned through a series of thermal oxidations in a high-purity dry oxidation furnace and BOE (6:1) wet etches to remove the oxide. This oxidation/stripping cycle was repeated until a top-Si thickness of about 25 nm was achieved. A final dry thermal oxidation cycle consumed about 5 nm of Si, resulting in final Si film thickness of 20 nm with a 10 nm sacrificial capping oxide, which remained throughout subsequent processing. Prior to each oxidation, a standard RCA clean was applied. Film thicknesses (grown oxide and top-Si) were measured before and after each oxidation, and after each BOE strip, using ellipsometry to monitor the process. The purpose of this top-Si thinning step was to increase the sidewall verticallity of the ohmic contacts post-etch and minimize any edge effects that might lead to higher contact resistance at the SOI-Si bond edge (see Fig. 5.1).

After the top-Si was thinned and capped, the SOI wafer was implanted with arsenic, with energy 6 keV, dose $4\text{x}10^{14}$ cm^{-2}, tilt of 7°, and a soft-electron shower to mitigate charge accumulation that could damage the BOX layer. The As implants were then thermally activated in a tube furnace anneal at 1000 °C for 30 minutes in an N_2 ambient. Ohmic contacts were patterned and isolated in the n^+ top-Si layer using standard photolithography and reactive-ion etching (RIE). Old photoresist was removed by immersion in hot acetone (80 °C, 30 minutes), hot IPA (80 °C, 10 minutes), and a DIW dump-rinse bath. This was followed by immersion in a fresh piranha bath (3:1 H_2SO_4:H_2O_2, 30 minutes), a DIW dump-rinse, and a final spin-rinse-dry (SRD) cycle. For the four-terminal SOI devices, the next step is to fabricate the proximity depletion gates using a lift-off metallization process; the recipe is laid out in the next section (§ 3.5.3). Finally, a 2 μm high mesa was formed by photolithograhy and dry-etching around the perimeter of each die in

order to promote bonding in the final step. This final mesa step is optional and in later device fabrication runs I omitted this step. This is possible because the mesa structure of the Si(111) piece forms all of the bonding perimeter, and thus an SOI mesa is not required. Old photoresist was again removed using the same acetone/IPA/DIW/piranha/DIW/SRD procedure, after which a protective resist film was deposited, the wafer was mounted to dicing tape, and then diced into 5.6 x 10 mm^2 samples.

3.5.3 Proximity depletion gates

The PDGs were fabricated using standard photolithographic lift-off techniques (see Fig. 3.7). After patterning the photoresist to define the PDGs, the SOI wafer was immersed in BOE (6:1) for 15 s to form a local trench in the BOX approximately 20 nm deep. It was then immediately rinsed in a DIW dump-rinse bath. Subsequently, 4 nm of a tantalum adhesion layer followed by 16 nm of a gold capping layer were sputter-deposited. Lift-off was performed in a double-bath immersion of the SOI wafer in Remover PG (80 °C, 30 minutes), followed by a fresh solution of Remover PG (80 °C, 10 minutes), a DIW dump-rinse bath, and a SRD cycle. Ta has good adhesion to SiO_2, and both Ta and Au have excellent corrosion resistance to both piranha and dilute HF solutions [190]. Profilometer and AFM scans reveal that the top of the PDGs are co-planar with the rest of the BOX.

3.5.4 The Si(111) piece

The Si(111) piece (see Figs. 3.3(b) and 3.4(b)) was fabricated on a prime-grade 100 mm intrinsic Si(111) wafer (Topsil, FZ, (111) +/- 0.1°, resistivity >20,000 Ω-cm). The Si(111) wafer was cleaned using standard RCA chemistry, followed by a high-purity dry thermal oxidation at 950 °C to grow a 20 nm sacrificial oxide. Using a similar photolithography and RIE procedure that was used for the SOI piece, a 10 μm mesa was created to promote bonding. In addition to promoting bonding, this large mesa structure has greatly reduced parasitic edge leakage from the global gate to the 2DES, due to the separation

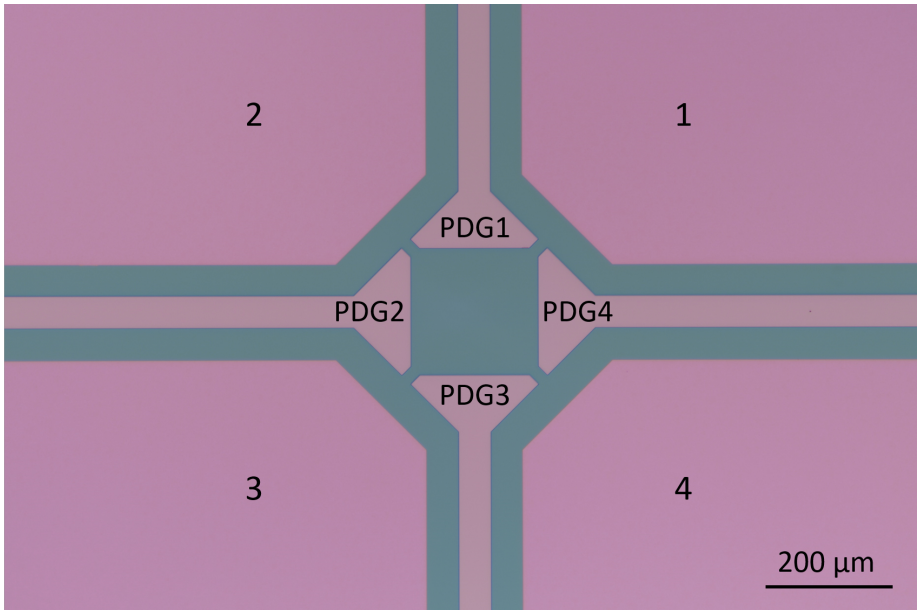

Figure 3.7: Optical micrograph showing the center of the SOI piece that will eventually be positioned directly over top of the H-Si(111) piece. Ohmic contacts are labeled quadrant-wise (1-4) while the PDGs are arranged along the cardinal directions (PDG1...PDG4). Everywhere on the SOI piece where the BOX is shown (blue-green) corresponds to where the 2DES resides on the H-Si(111) surface. The PDGs confine the 2DES to a 200 μm x 200 μm square in the center with four 20 μm access channels.

of the Si(111) surface from the long edge of the SOI piece. The Si(111) wafer was then cleaned using the same acetone/IPA/DIW/piranha/DIW/SRD procedure, after which a protective resist film was deposited, the wafer was mounted to dicing tape, and then diced into 5.6 x 10 mm^2 samples.

3.5.5 H-termination and Van der Waals bonding

Prior to bonding, individual SOI and Si(111) pieces were stripped of photoresist and cleaned using an acetone/IPA/DIW/piranha/DIW/SRD procedure. This last cleaning step was carried out in personal glassware that was regularly cleaned in piranha solution to minimize cross-contamination. After the final cleaning step, samples were transferred to an ultra-clean (less than 1 particle >0.1 μm per cubic foot) glove box with an inert N_2 environment (less than 1 ppm O_2). The Si(111) sample was immersed in a deoxygenated solution of dilute 10:1 HF for 2 minutes to strip off the sacrificial oxide. After a 1 minute rinse in deoxygenated DIW, the Si(111) piece was immersed in deoxygenated, ultra-high purity ammonium fluoride (40% NH_4F by w.t., less than 10 ppb trace ions) undisturbed by agitation or stirring for 15 minutes. This final wet treatment in aqueous NH_4F atomically flattens and hydrogen-passivates the Si(111) surface [41–44].

In a parallel fashion, the SOI piece was immersed in deoxygenated 10:1 HF for 90 s to strip the sacrificial oxide and hydrogen-passivate the ohmic contacts. All beakers and tweezers used in these etch steps were made of ultra-clean Teflon that were regularly cleaned in RCA baths and piranha solution. Both samples, now hydrophobic, were blown dry with N_2 (no DIW rinse) and placed on a hotplate at 120 °C for about 1 minute to remove any excess moisture.

The samples were placed in a bonding puck facing one another and skew-perpendicular. The puck was then transferred to a bonding chamber (see Fig. 3.8) where they were heated *in situ* to about 120 °C for 10 minutes while the chamber was evacuated to about 10^{-6} Torr. The two pieces were then pressed together against a sapphire boss using a sapphire

rod on a z-translation stage. Bonding was detected using an infrared camera with backside illumination.

After Van der Waals bonding (see Figs. 3.3(c) and 3.4(c)), the samples were transported in a sealed container to another N_2 ambient glovebox (see Fig. 3.9) where they were secured loosely into a sample holder that provided mechanical support without adding additional strain. Multiple thermal cycles in which the device remains bonded and intact is evidence that no significant strain is being introduced by the sample attachment. The device was then wired to a DIP chip socket using 1 mil Au wire and In solder.

In the next chapter (Ch. 4) I discuss the measurements of this device now that it is wired and ready for cool-down. Needless to say, the process I just described did not always yield working devices. There were many iterations of devices with a range of I-V and leakage characteristics, depending on how good the bond was or how clean the samples were (see the device graveyard in Fig. 3.10 for reference). However, the data presented in the next chapter are for the most part typical of good working devices.

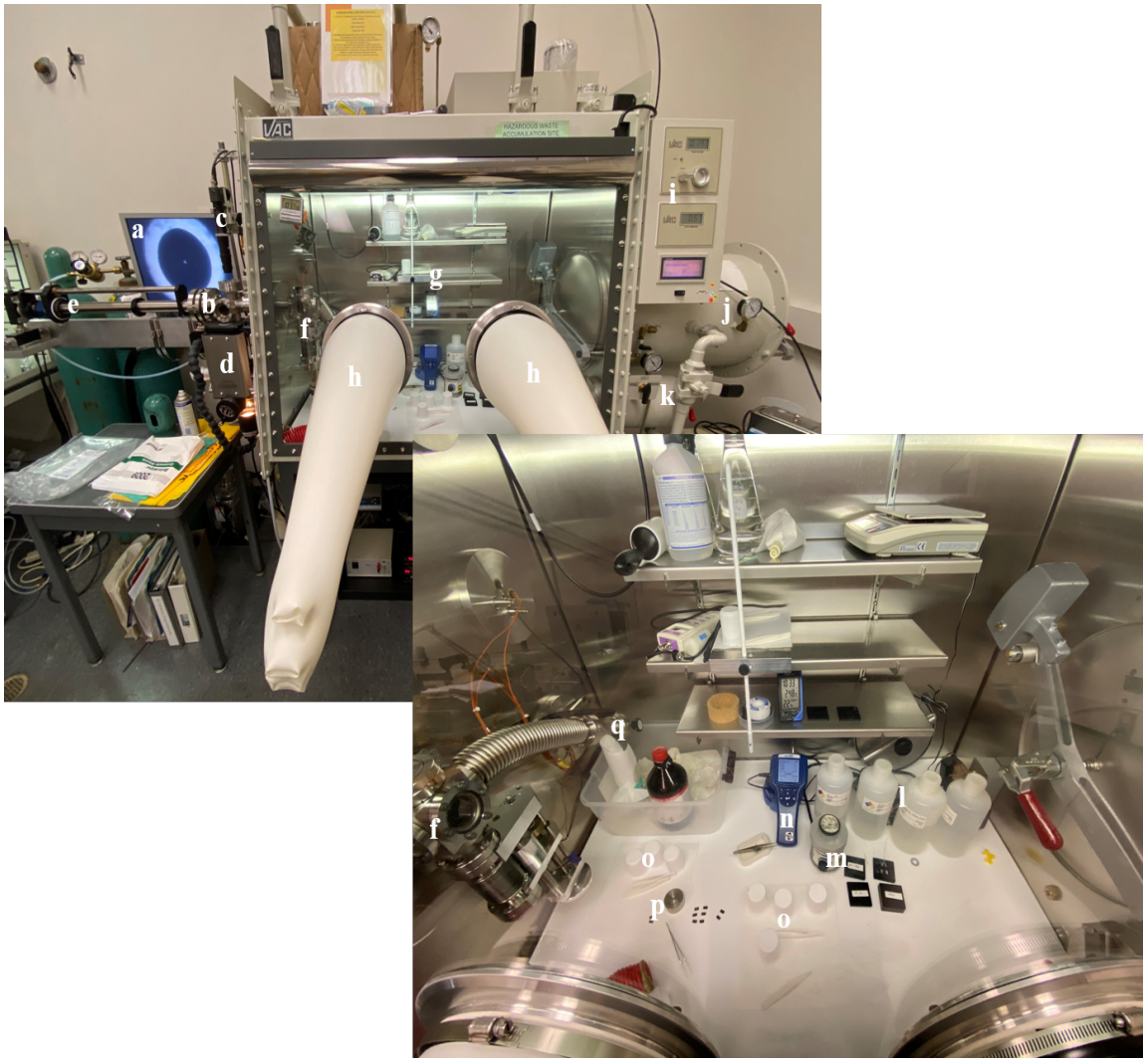

Figure 3.8: Glovebox for final chemical passivation and bonding. (a) bonding monitor, (b) bonding chamber, (c) IR bonding camera, (d) z-translation stage, (e) transfer rod, (f) loading chamber, (g) main glovebox cabin, (h) HF-resistant butadyl gloves, (i) oxygen and moister analyzers, (j) large load-lock, (k) small load-lock, (l) HF and NH_4F chemistry, (m) hotplate, (n) micron particle counter, (o) teflon beakers and tweezers, (p) bonding puck, (q) evacuation port to turbo pump.

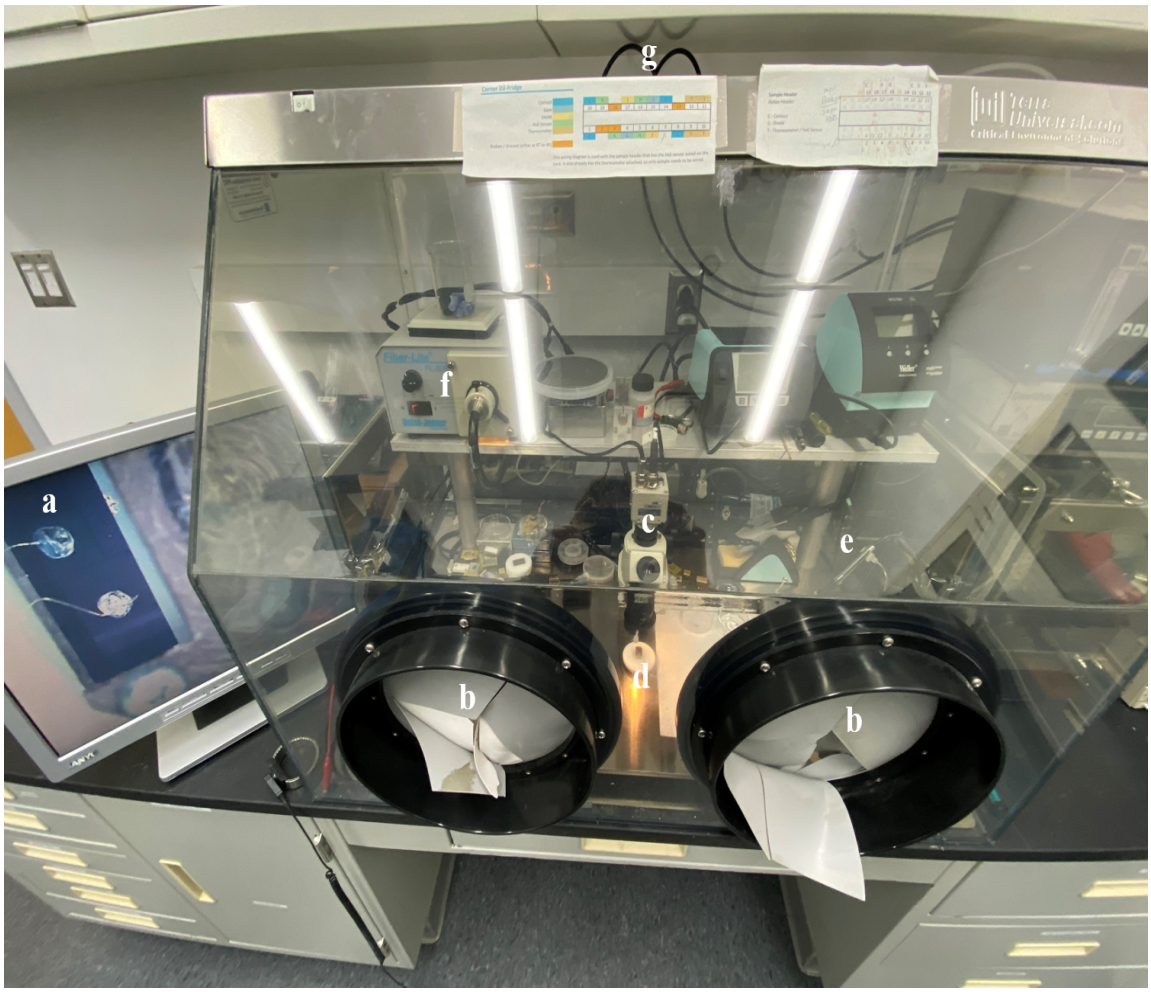

Figure 3.9: Glovebox for wiring of bonded device. (a) wiring monitor, (b) hand entry ports, (c) microscope and camera assembly, (d) sample being wired (seen on monitor in (a)), (e) indium solder iron, (f) sample illumination, (g) N_2 gas in-lines.

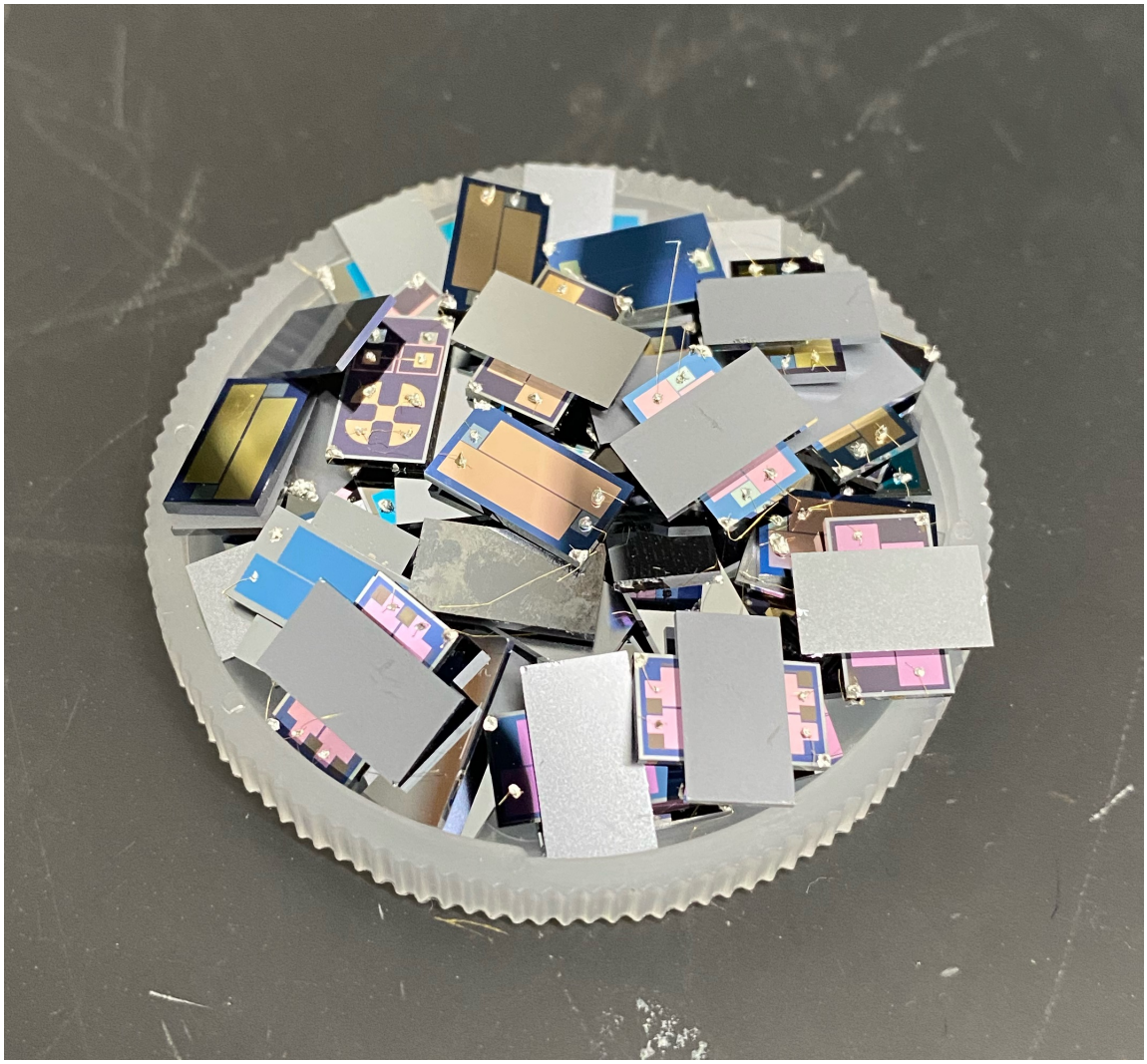

Figure 3.10: Device graveyard – where bad devices go when they die.

Chapter 4: 2DES transport on H-Si(111)

The measurements presented in this chapter were obtained from the same four-terminal device described by Robertson et al., unless otherwise noted [188]. Measurements were carried out under vacuum in a homemade vacuum dip-stick which fits directly into liquid nitrogen and liquid helium dewers, enabling quick cool-down for test measurements. After removal from the glovebox, the bonded samples saw ambient atmospheric conditions for no more than 2-3 minutes while the device was mounted to the dip-stick apparatus.

4.1 Baseline measurements

Baseline measurements of the device were made to ensure proper operation. Low sheet resistance of the ohmic contacts, minimal gate leakage, proper 2DES confinement to a Van der Pauw (VdP) configuration, and low series contact resistance were all necessary for establishing good device performance. For the measurements in § 4.1.3 and § 4.1.4, the device was configured according to the schematic illustrated in Fig. 4.1.

4.1.1 Ohmic contact sheet resistance

Several clover leaf test dies (see Fig. 3.3(b)) were prepared simultaneously alongside the actual device dies on the same SOI wafer. Measurements of the test dies at 4.2 K showed an ohmic contact sheet resistance of $\sim$3 k$\Omega/\square$. The sheet resistance of the ohmic contacts depends upon the arsenic doping density, which for this device was roughly 2x10^{20} cm^{-3}, and inversely on film thickness, at least until a thickness of about

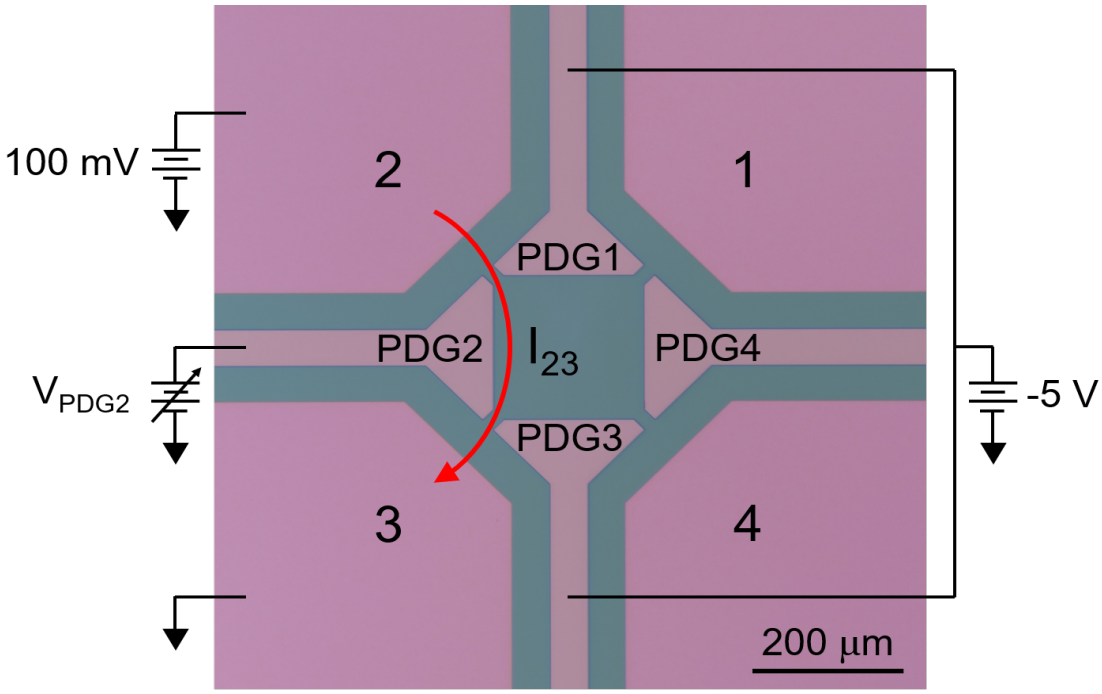

Figure 4.1: Schematic of a wired four-terminal device for measurements of the PDG leakage and the two-terminal resistance discussed in § 4.1.3 and § 4.1.4, respectively. The red arrow shows the current entering through ohmic contact 2, being injected onto the H-Si(111) surface (not shown), traveling through the VdP square, and then exiting through ohmic contact 3.

10 nm. For this particular device run, the top-Si thickness was about 20 nm. Previous measurements of some of my earlier devices with a top-Si layer of approximately 10 nm showed a non-linear increase in the sheet resistance, suggesting increased scattering of electrons at the film boundaries. As such, I do not recommend the use of sub-20 nm thick ohmic contacts for future device runs.

4.1.2 Global gate leakage

For a fully fabricated and wired four-terminal SOI device, the global gate leakage to both the ohmic contacts and the PDGs was sub-40 pA, demonstrating good global gate isolation. Figure 4.3 shows measurements of the background leakage and the source-drain currents under similar conditions. To examine the extent to which the global gate is isolated from the rest of the sample and can withstand high voltages, I fabricated several MOS-Cap devices out of scrap SOI samples. After wiring the top-Si island and grounding the gate layer, I swept a DC voltage across the BOX and did not see breakdown until about 120 V. This suggests that the BOX-vacuum dielectric in our devices can withstand fields as high as 6 x 10^6 V/cm.

4.1.3 Proximity depletion gate leakage

To ensure that there was no negative-bias leakage of the 2DES to the PDGs, a reverse bias of V_{PDG} = -5 V was applied to all PDGs with the ohmic contacts grounded and a forward bias of V_G = 15 V applied to the global gate. Sub-40 pA leakage was measured, demonstrating good PDG isolation. VdP confinement of the 2DES was demonstrated by tying PDG1 and PDG3 to a reverse bias of V_{PDG1} = V_{PDG3} = -5 V, applying a constant DC source-drain bias V_{23} = 100 mV, a forward global gate bias V_G = 15 V, and sweeping PDG2 from V_{PDG2} = -5 V to 1 V, as shown in Fig. 4.2. No modulation of the source-drain current (I_{23}) was seen from V_{PDG2} = -5 V to about 0.4 V, demonstrating that all of the current on the H-Si(111) surface was flowing through the VdP square. After $\sim$0.4 V,

I_{23} began to increase due to the inversion of the H-Si(111) surface directly beneath PDG2 which opened up new current paths, and then dropped again as forward-bias leakage began to dominate. This suggests that the H-Si(111) surface beneath the PDGs is fully depleted when $V_{PDG} < 0.4$ V.

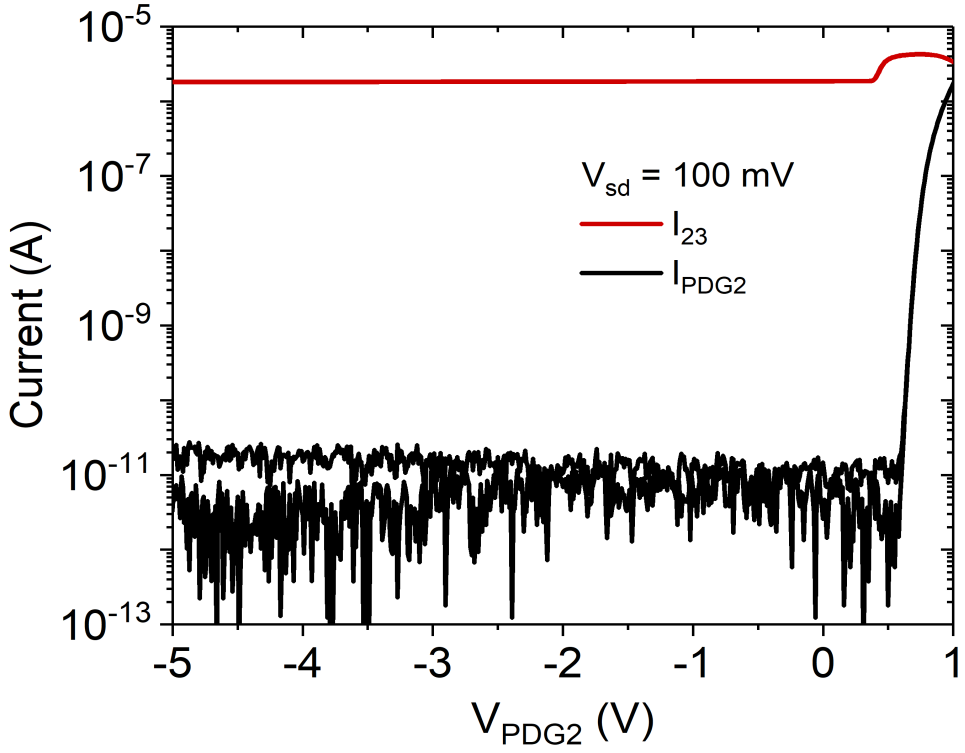

Figure 4.2: A plot of current I vs V_{PDG2} illustrating VdP confinement of the 2DES at 77 K according to the schematic shown in Fig. 4.1. V_{PDG2} was swept while holding $V_{PDG1} = V_{PDG3}$ = -5 V, V_G = 15 V, and applying a constant DC source-drain bias of V_{23} = 100 mV (I_{23} shown in red). For comparison, leakage from the 2DES to PDG2, I_{PDG2}, is shown in black. There is no current modulation below V_{PDG2} ~0.4 V, indicating that all of the current is flowing through the VdP square when $V_{PDG} < 0.4$ V.

4.1.4 Ohmic conduction at 77 K

Ohmic conduction in the device at 77 K was demonstrated through simple two-terminal measurements by sweeping the global gate voltage from V_G = 0 V to 20 V at three different DC source-drain biases, V_{23} = 1 mV, 10 mV, and 100 mV, with all PDGs grounded.

Figure 4.3 shows good linearity across a wide range of source-drain biases, with a total series resistance of approximately 57 kΩ at V_G = 15 V. This two-terminal series resistance (R_{2T}) can be described by:

$$R_{2T} = R_{2DES} + 2R_{ohmic} + 2R_{contact} \approx 57\ k\Omega \tag{4.1}$$

where R_{2DES} is approximately 620 Ω (from four-terminal measurements) and R_{ohmic} is 8-9 kΩ. This means $R_{contact}$ was on the order of 20 kΩ at 77 K.

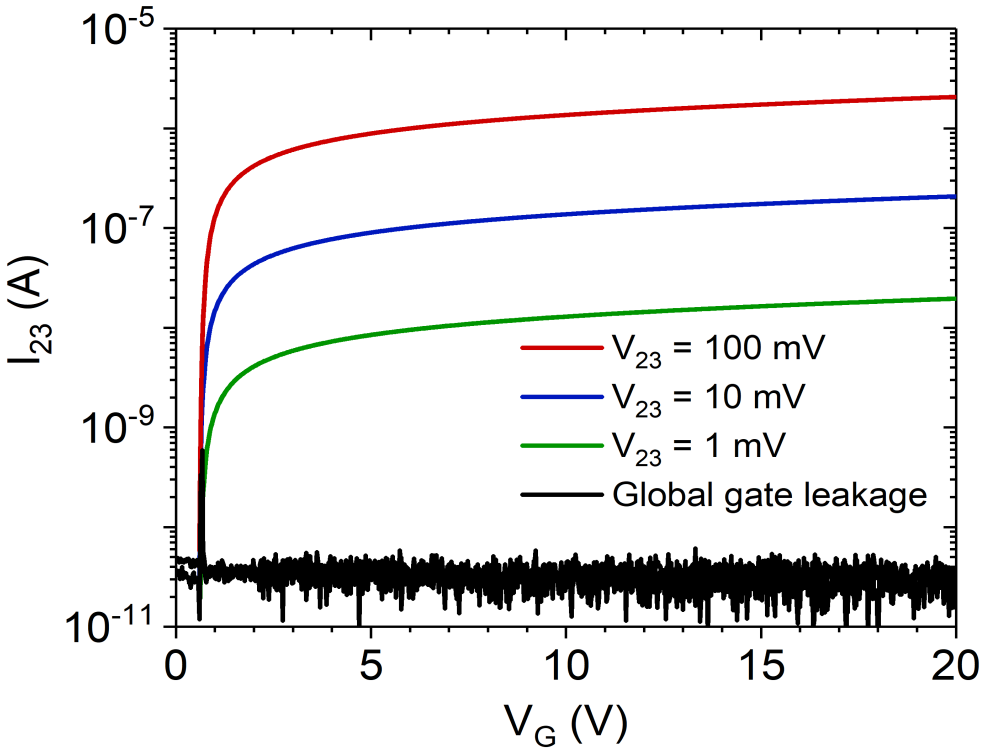

Figure 4.3: Plot of I_{23} vs gate voltage showing ohmic behavior of the device at 77 K over a range of two-terminal DC source-drain biases (red, blue, green). For comparison, leakage from the 2DES to the global gate is shown in black. The spike in the global gate leakage at the threshold voltage, $V_G \approx 0.6$ V, indicates the formation of the 2DES on the H-Si(111) surface.

4.2 Transport measurements at 77 K

Upon demonstration of good baseline operation, standard low frequency AC lock-in techniques were performed at 77 K (15.915 Hz, 100 nA) to measure the sheet resistance and the Hall density of the 2DES (see Fig. 4.4), with all PDGs tied to ground. A 200 gauss coil magnet, which fit snugly around the vacuum dip-stick, was used to measure the 2D Hall density at V_G = 5 V and V_G = 10 V, which I found to agree well with the expected geometric densities at those voltages. The fit line (red line in Fig. 4.4) shows a density of $n = 0$ cm^{-2} at $V_G \approx 0.6$ V, which is close to the threshold voltage seen in Fig. 4.3. From Fig. 4.4, I can extract a density dependent carrier mobility, using Eq. 2.67. At V_G = 15 V ($n \approx 5\text{x}10^{11}$ cm^{-2}), the 2DES mobility is approximately 4,400 cm^2/Vs at 77 K. This can be compared to the best Si(111) MOSFETs which have electron mobilities of about 2,500 cm^2/Vs, even at sub-4.2 K temperatures [191, 192]. This demonstrates that we do indeed have a high-quality 2DES on our H-Si(111) surface that has not been destroyed through the gating process.

4.3 Low temperature measurements: 4.2 K and beyond

As the device was further cooled to 4.2 K, however, the two-terminal resistance became large and non-linear (see Fig. 4.5). Measuring the two-terminal resistance R_{2T} at 4.2 K under similar conditions as discussed previously (V_G = 15 V, PDGs grounded, and a 100 mV source-drain bias), I found the total series resistance was approximately 1 MΩ (see Fig. 4.5). I attributed this large series resistance to the SOI-Si interface contact resistance $R_{contact}$. Referring to Eq. 4.1, this implies that $R_{contact} \approx 500$ kΩ at 4.2 K, assuming R_{ohmic} remains constant with temperature and R_{2DES} only decreases with temperature. Due to the dramatic increase in the contact resistance at low temperatures (4.2 K and below), I did not do four-terminal measurements at 4.2 K on our devices.

Ultimately, with changes to the processing techniques for making ohmic contact to the

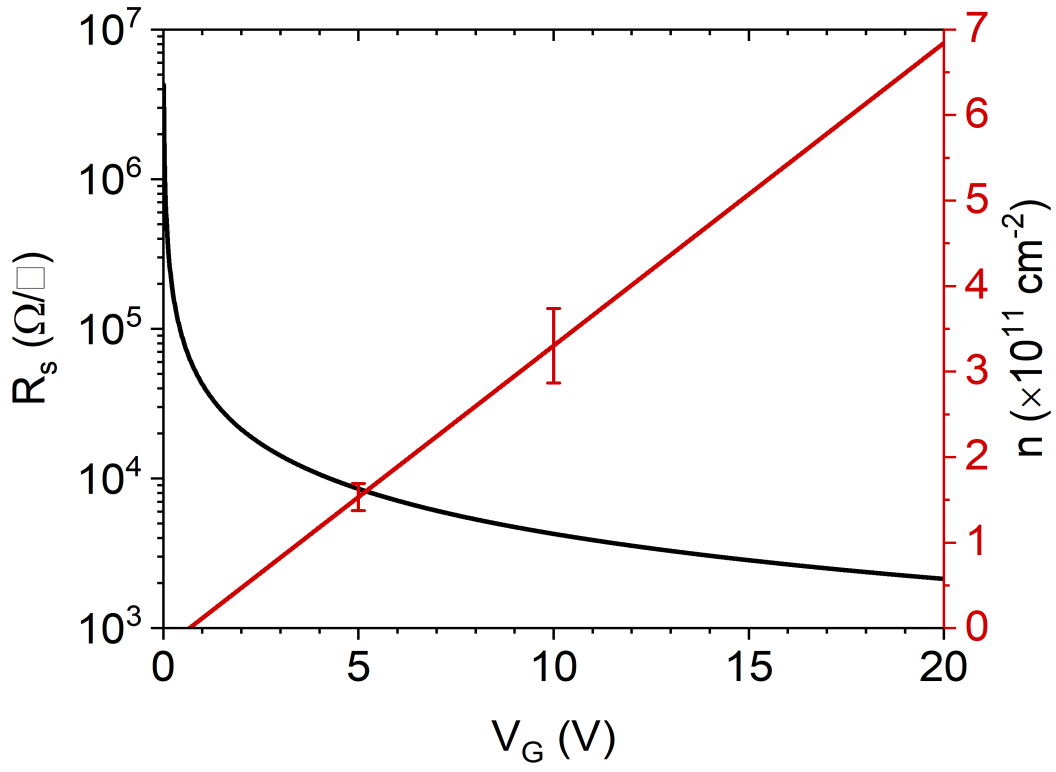

Figure 4.4: Sheet resistance (black) and electron density (red) of the device at 77 K from four-terminal VdP and Hall measurements, respectively. From these measurements we can extract a density dependent carrier mobility, according to Eq. 2.67, and see that at V_G = 15 V ($n \approx 5\text{x}10^{11}$ cm^{-2}), the 2DES mobility is approximately 4,400 cm^2/Vs at 77 K.

2DES, it should be possible to perform low temperature magnetotransport measurements in our devices. Unlike other non-invasive gating methods that have been mentioned, series contact resistance at the SOI-Si bonding interface is an inherent feature of our device architecture due to placement of the ohmic contacts on the SOI piece rather than on the Si surface itself. Nevertheless, the challenges of reducing $R_{contact}$ through improved processing were outweighed by the benefits of having a completely undoped, pristine, intrinsic Si surface to chemically terminate and electrostatically gate. In the following chapter (Ch. 5), I discuss in detail the large contact resistance that plagued our devices and present a viable solution to improve performance at low temperatures.

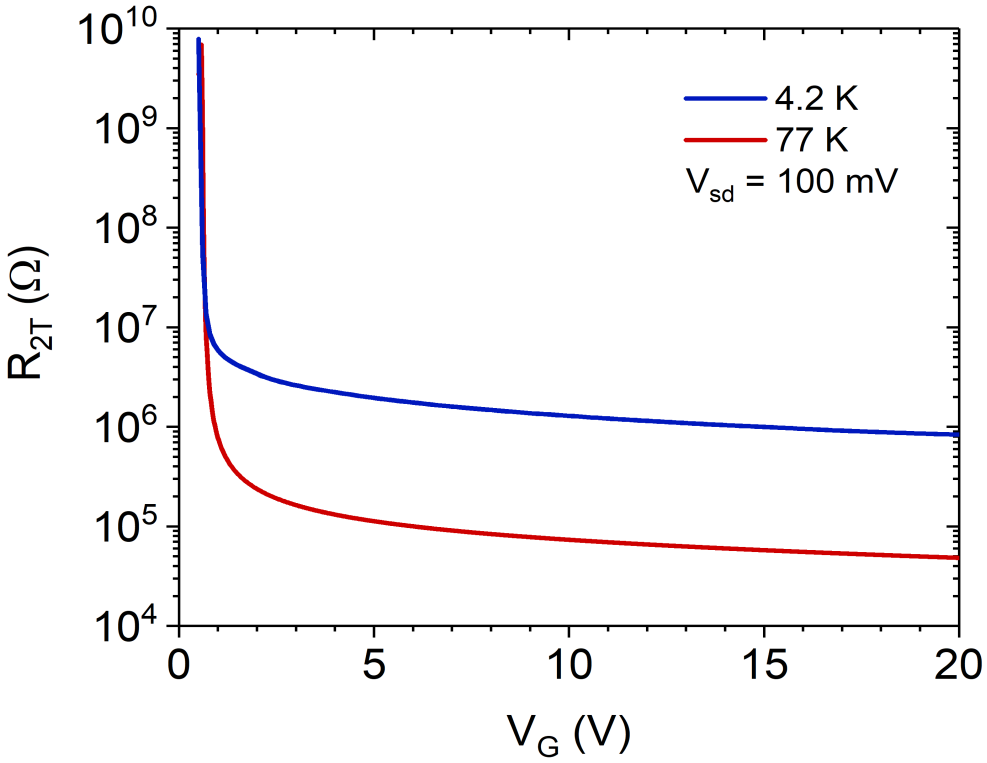

Figure 4.5: Plots of the two-terminal resistance R_{2T} vs gate voltage V_G of the device at 77 K (red) vs 4.2 K (blue). The contact resistance $R_{contact}$ is strongly temperature dependent and presents a serious challenge for measuring our devices at 4.2 K.

Chapter 5: The SOI-Si bonding interface

5.1 Contact resistance – Achilles

The primary challenge I faced during the development of the non-invasive architecture was the presence of a large series contact resistance at the SOI-Si bonding interface at low temperatures. The same feature that enables our devices to be completely non-invasive is also our Achilles' heel, being that the ohmic contacts and the 2DES are on two separate chips and current must therefore be injected across a Van der Waals bond. This requires that the bonding interface, especially at the bonding edge between the two samples, be nearly perfect.

Figure 5.1 shows SEM cross-sectional images of the ohmic contacts on two different SOI devices after final processing and pre-bonding. It can be seen that the sidewall and bonding edge are not ideal and therefore will not form a perfect union with the Si piece. Ideally, we would like the SOI sidewall and the Si(111) surface to form a right angle, with uniform contact along the bond edge. In reality, the sidewalls are not exactly vertical and thus imperfections and rounding of the ohmic contacts at the bonding edge results in a shielding of the Si(111) surface from the global gate at the bond edge. This leads to decreased electron accumulation at the corner and an increased contact resistance.

For both the two-terminal and four-terminal devices, the series contact resistance between any two ohmic contacts, R_{2T}, can be expressed by Eq. 4.1 which I again write here:

$$R_{2T} = R_{2DES} + 2R_{ohmic} + 2R_{contact} \tag{5.1}$$

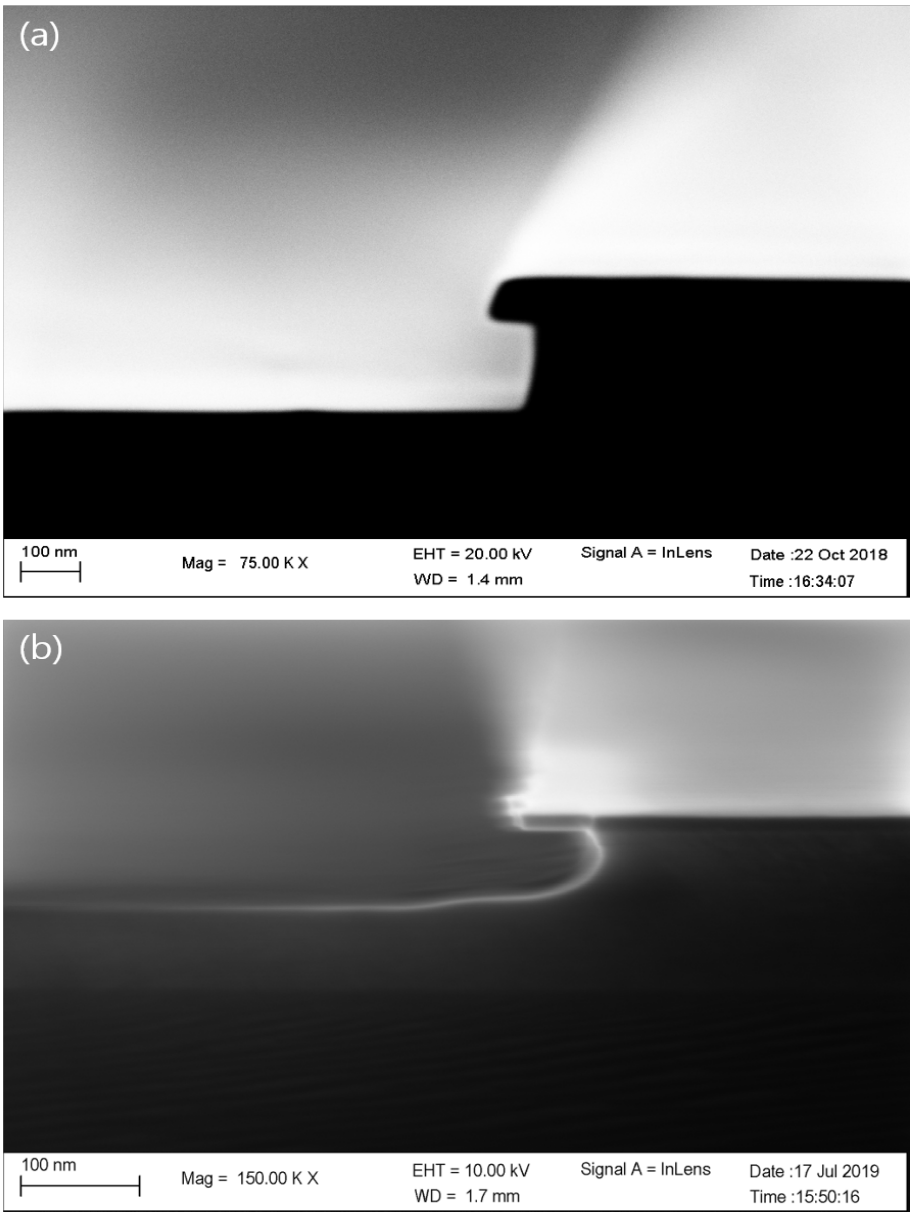

Figure 5.1: SEM micrograph cross-sections at the ohmic contact edge of two different cleaved SOI pieces after final processing (pre-bonding). (a) An older device with thicker top-Si ($\sim$ 88 nm) showing a rounded sidewall profile. (b) A newer device with thinned top-Si ($\sim$ 20 nm) showing a more vertical but still imperfect sidewall profile. This imperfection at the SOI-Si bonding edge leads to an increase in $R_{contact}$ and presents a fundamental challenge for our devices.

where R_{2DES} is the resistance of the 2DES on the Si surface. R_{2DES} is inversely proportional to the applied global gate voltage V_G and tends to decrease with temperature. R_{ohmic} is the resistance of the ohmic contacts which is determined by the doping level and remains essentially constant across all temperatures. The final term, $R_{contact}$, is the resistance across the SOI-Si bonding interface. Figure 4.5 shows the dramatic difference in the two-terminal resistance of a device at 77 K vs 4.2 K, illustrating the fundamental challenge with our devices. As we will see in the next section, this contact resistance has a complicated configuration and temperature dependence; lowering this resistance is critical for our device performance at low temperatures.

5.1.1 Current injection across a Van der Waals bond

To understand the temperature dependence of $R_{contact}$ and the other parameters that affect the contact resistance, I now establish a more theoretical framework to describe the current flowing across the SOI-Si bond edge. A detailed description of the formation of a metal-semiconductor junction and the current flow through such a junction can be found in Ch. 3 of Sze and Ng (2007) [66], for example, but here I provide a brief summary.

When a metal comes into contact with a doped semiconductor, the Fermi level in the band gap of the semiconductor must align with that of the mid-band Fermi level in the metal at thermal equilibrium. This causes the conduction and valence bands of doped semiconductors to bend upwards (n-type) or downwards (p-type) near the interface, forming what is known as a Schottky barrier (SB) (see Fig. 5.2). The bending of the bands creates an electric field and an associated built in potential ψ_{bi} that depends on the doping levels in the semiconductor. However, in the case of an ideal intrinsic semiconductor, there are no dopants, and thus no band bending and no built in potential. For our devices, a SB is formed when the degenerately doped (i.e. metallic) ohmic contacts are brought into contact with the 2DES on the intrinsic Si surface. In this scenario, the built in potential ψ_{bi} is

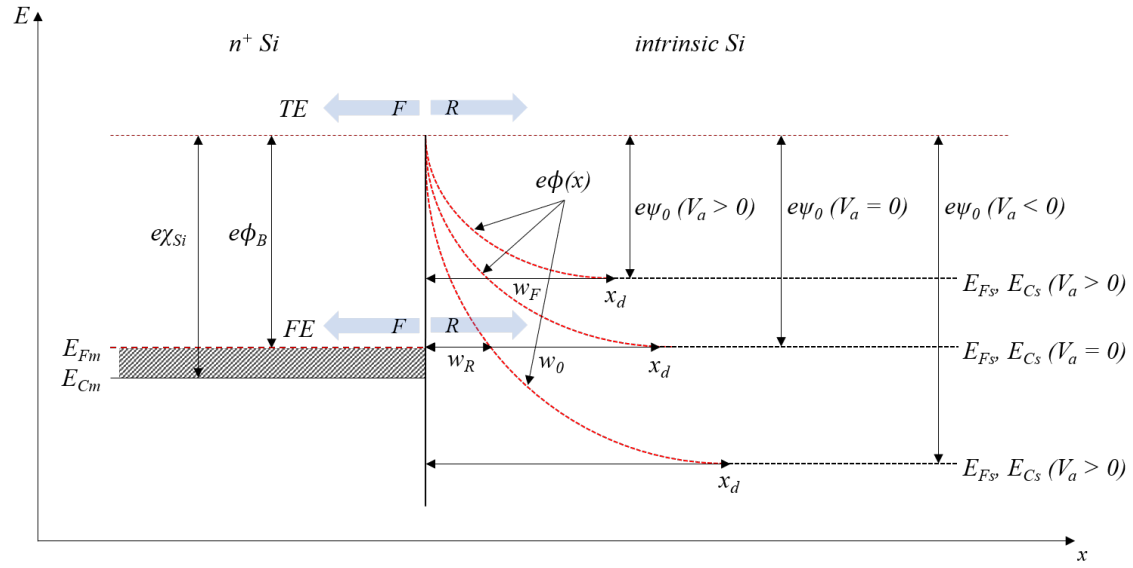

Figure 5.2: Schematic of a Schottky barrier (SB) junction between the metallic n^+-Si and the 2DES on the i-Si surface. The blue arrows indicate the direction of the carrier flow (for electrons) for thermionic emission (TE) and field emission (FE), thus the current is in the opposite direction. The SB height ϕ_B is fixed by the materials (namely the doping levels in the ohmic contacts) and may have some temperature dependence. The function $\phi(x)$ plotted in red describes the conduction band of the 2DES near the interface and is shown for the forward, zero, and reverse applied source-drain bias cases, which raise or lower the conduction band relative to the Fermi level E_{Fm} of the ohmic contacts by an amount $\phi_B - \psi_0 = V_a$. The global gate-dependent depletion width x_d defines the domain over which the conduction band-bending occurs due to a variable charge configuration (Eq. 5.32), and is equal to the tunneling width for the zero- and forward-bias cases. w_R is the tunneling width for the reverse-bias case.

replaced by the global gate-induced potential ψ_0 (see Fig. 5.2). In the absence of interface states, a non-zero bias applied to the global gate causes the conduction band in the 2DES bulk to shift down to the Fermi level and electrons which are able to flow across the barrier begin to populate the surface. If interface states are present, then a threshold voltage V_T must be reached before the interface states are filled and free electrons can begin to accumulate. For the device described in Ch. 4, $V_T \approx 0.6$ V. This band bending is pinned at the device interface by the SB height ϕ_B and is described by the function $\phi(x)$. This potential is what creates the barrier through which electrons must tunnel or over which electrons must be thermally excited over and emitted.

I can define two different Fermi levels, E_{Fm} for the ohmic contact and E_{Fs} for the 2DES. $E_{Fm} = E_{Fs}$ only under equillibrium conditions (i.e. when there is no applied source-drain voltage). As illustrated in Fig. 5.2, when a voltage V_a is applied to the ohmic contact, the Fermi level in the 2DES shifts up or down relative to E_{Fm} for positive or negative applied voltages, respectively. Furthermore, due to the design of our devices, there will always be a forward-bias and a reverse-bias SB to consider when current flows from one ohmic contact to another. When a small source-drain voltage, $V_{sd} << \phi_B$, is applied, the source-side (at ground) sees a reverse applied bias, $V_a \approx -V_{sd}/2$, and the drain-side (at V_{sd}) sees a forward applied bias, $V_a \approx V_{sd}/2$. This assumes that the source-2DES and the 2DES-drain resistances are roughly equal, so that half of the source-drain voltage drops across each SB in the current path. For $V_a > \phi_B$, the drain-side is dominated by thermionic emission, since the conduction band is above the SB height on that side, while the source-side is limited by reverse-bias tunneling. This means that almost all of the voltage drop is across the source-side, which sees an applied bias of $V_a \approx -V_{sd}$.

The intrinsic SB height ϕ_{B0} is fixed by the doping level in the n^+ Si and can be modified by other effects, such as 2D confinement in the semiconductor, image-charge lowering, or the presence interface states. For a normal metal-semiconductor junction, the SB height is

given by:

$$\phi_{B0} = \phi_m - \chi_s \tag{5.2}$$

where ϕ_m is the metal work function and χ_s is the semiconductor electron affinity. If the metal is replaced by a degenerately doped semiconductor (as is the case with my devices), the effective work function of the metallic semiconductor is given by:

$$\phi_s = \chi_s - \frac{(E_C - E_F)}{e} \tag{5.3}$$

where E_c is the energy of the conduction band edge. The SB height then becomes:

$$\phi_{B0} = \frac{E_F - E_C}{e} \cong \frac{k_B T}{e}\left[ln\left(\frac{N}{N_c}\right) + \frac{1}{2^{3/2}}\left(\frac{N}{N_c}\right)\right] \tag{5.4}$$

where N is the density per unit energy per unit volume of free electrons in the ohmic contacts and N_c is the 3D effective density of states for the n^+-Si conduction band. Eq. 5.4 is a valid approximation when the Fermi level in the n^+-Si is near or above the conduction band [66].

A significant amount of work has been done investigating the band structure of Si striated with heavily δ-doped layers, where the Fermi level resides tens to hundreds of meV above the conduction band [193]. There is some debate on exactly how these models extend to uniformly doped Si and whether or not the Fermi level in ultra-high degenerately n-doped Si is actually above the conduction band. Nevertheless, I will assume Eq. 5.4 is a good starting point for determining ϕ_{B0}.

Additionally, because of the 2D-confinement of the electrons on the intrinsic Si surface, the effective conduction band minimum of the 2DES has been shifted up in energy

by E_0^z (see Eq. 2.35), which *increases* the SB height to $\phi_B = \phi_{B0} + E_0^z/e$. Furthermore, for more realistic scenarios, I would need to consider interface states and image-charge lowering which modifies the barrier height to $\phi_B = \phi_{B0} + E_0^z/e + \phi_{D_{it}} - \phi_{ic}$. Here, I am not concerned with the exact expression for the SB height, but note that this parameter has a great deal of tunability. In practice, I assumed a total effective height ϕ_B, with implicit dependencies. I have also not yet assumed a specific shape for the SB potential $\phi(x)$, as this will be the focus of §§ 5.1.2 and 5.1.3.

I can now find an expression for the current density across the SB interface, and find the parameters which contribute to the SOI-Si contact resistance $R_{contact}$. There are two primary mechanisms for current flow across the SB: thermionic emission (TE) and field emission (FE, or tunneling). For both TE and FE, the total current density through a SB is the algebraic sum of the current density from the metal to the semiconductor J_{MS}, and the current density from the semiconductor to the metal J_{SM}. Thus I can write the total current density as $J = J_{MS} - J_{SM}$. For my purposes, I will not be concerned with TE since we are dealing with low temperatures, and I expect that tunneling will be the dominate transmission mechanism in my devices. Following Sze and Ng, and the reference therein by Chang et al. [194], the tunneling current density from the metal to the semiconductor in a SB with dimensionality factor α (see discussion below) is given by:

$$J_{MS} = \alpha\Theta(x)\int_0^{e\phi_B} F_m(1-F_s)dE \tag{5.5}$$

where $\Theta(x)$ is the tunneling transmission probability. In the Wentzel–Kramers–Brillouin (WKB) approximation $\Theta(x)$ is given by:

$$\Theta(x) = \exp\left(-\frac{2}{\hbar}\int_0^w \sqrt{2em^*\phi(x)}dx\right) \tag{5.6}$$

Here, $\phi(x)$ is the function describing the shape of the SB potential (or the conduction band of the 2DES near the SB interface) and w is the width of the SB (see Fig. 5.2). Similar to J_{MS}, the tunneling current density from the semiconductor to the metal of an SB is given by:

$$J_{SM} = \alpha\Theta(x)\int_0^{e\phi_B} F_s(1-F_m)dE \tag{5.7}$$

where F_m and F_s are the Fermi-Dirac distribution functions for the metal and semiconductor, respectively, and are given by:

$$F_s = \frac{1}{1+\exp\left(\frac{E-eV_a}{k_BT}\right)} \tag{5.8}$$

and:

$$F_m = \frac{1}{1+\exp\left(\frac{E}{k_BT}\right)}. \tag{5.9}$$

Thus the total FE current density can be written as:

$$J = J_{MS} - J_{SM} = \alpha\Theta(x)\left[\int_0^{e\phi_B} F_m(1-F_s)dE - \int_0^{e\phi_B} F_s(1-F_m)dE\right] \tag{5.10}$$

The integral in brackets evaluates to:

$$\Gamma(V_a) = \ln(2) - \ln\left(1+\frac{\cosh\frac{e(\phi_B+V_a)}{2k_BT}}{\cosh\frac{e(\phi_B-V_a)}{2k_BT}}\right) \tag{5.11}$$

and the current density becomes:

$$J = \alpha k_B T \Gamma(V_a) \Theta(x) \tag{5.12}$$

The prefactor, α, can be chosen for either a 3D, 2D, or 1D SB, by setting:

$$\alpha_{3D} = \frac{A^*_{3D} T}{k_B}, \tag{5.13}$$

$$\alpha_{2D} = \frac{A^*_{2D} T^{1/2}}{k_B}, \tag{5.14}$$

or:

$$\alpha_{1D} = \frac{A^*_{1D}}{k_B} \tag{5.15}$$

where A^*_{3D}, A^*_{2D}, and A^*_{1D} are the 3D, 2D, and 1D effective Richardson constants, respectively, and are given by [195]:

$$A^*_{3D} = g_v g_s \frac{4\pi m^* e k_B^2}{h^3}, \tag{5.16}$$

$$A^*_{2D} = g_v g_s \frac{\sqrt{2m^*} e \left(\pi k_B\right)^{3/2}}{h^2}, \tag{5.17}$$

and:

$$A^*_{1D} = g_v g_s \frac{e k_B}{h}. \tag{5.18}$$

While the ohmic contacts are effectively a 3D metal and the 2DES on the intrinsic Si

surface is inherently 2D, the current paths *across* the SB in our devices will either be 2D or 1D in nature. I have included the α prefactor for the 3D case just for reference, but I did not use it in the analysis here. A 2D path represents current flow across the SB in regions where there is perfect bonding along a significant length of the SOI-Si bond edge. A 1D path represents current flow across discrete bond points due to imperfect bonding along the SOI-Si bond edge. In a perfect bond scenario, we would expect 2D transmission to be the dominant effect. However, in reality it is likely to encounter a situation where most or all of the current is flowing through discrete 1D points where the SOI and Si are intimately bonded. Thus, I examine both the 2D and the 1D cases and see which one explains our data better. I note that A^*_{2D} (Eq. 5.17) and A^*_{1D} (Eq. 5.18) have units of A/m and A, respectively. To get the total *current* through the SB, we must multiply Eq. 5.12 by either the SOI-Si bond edge length L_{2D} or the number of SOI-Si bond points L_{1D}. Doing this gives us:

$$I_{2D} = L_{2D} A^*_{2D} T^{3/2} \Gamma(V_a) \Theta(x) \tag{5.19}$$

and:

$$I_{1D} = L_{1D} A^*_{1D} T \Gamma(V_a) \Theta(x) \tag{5.20}$$

I can then express $R_{contact}$ as the derivative of the applied source-drain voltage with respect to the current:

$$R_{contact} = \frac{dV_{sd}}{dI} \tag{5.21}$$

Now that I have expressions for the 2D and 1D FE current through the SB, I can examine which parameters impact the current flow and consider how we might adjust

those parameters reduce $R_{contact}$. The current is temperature independent in the $\Theta(x)$ term, however it is exponentially dependent on the barrier width and "weakly" exponentially dependent on the barrier height, as I will show. Other parameters include the global gate voltage V_G, the global gate capacitance C, and any spin or valley degeneracies that may be present. The last two parameters that I considered were the length of the SOI-Si bond edge L_{2D} and the number of SOI-Si bond points, L_{1D}, on which I_{2D} and I_{1D} have linear dependencies.

In the following sections, I will explore how these parameters influence the low-temperature 2D and 1D FE current through the SB. I will show that the SB width has a complicated inverse dependence on the global gate capacitance C, as well as the applied gate voltage V_G. This global gate voltage dependence provides an experimental means by which to decrease the width of the SB and thus increase the FE current.

5.1.2 Electrostatics at a corner: Laplace's equation

It is well known that the electric field at the corner of two intersecting conductive plates must vanish when the angle between the plates is less than π radians. Consider the illustration in Fig. 5.3, where two intersecting plates of fixed potential $\Phi = V$ meet at an angle β. Laplace's equation for the potential Φ with the boundary conditions shown in Fig. 5.3, is given by:

$$\nabla^2 \Phi(\rho, \phi) = 0 \tag{5.22}$$

The general solution to this boundary problem has been provided by Jackson [196], and is given in polar coordinates ρ and ϕ by:

$$\Phi(\rho, \phi) = V + \sum_{m=1}^{\infty} a_m \rho^{\frac{m\pi}{\beta}} sin\left(\frac{m\pi}{\beta}\phi\right) \tag{5.23}$$

where a_m are coefficients determined by boundary conditions imposed far from the corner (when $\rho \longrightarrow \infty$). For small ρ, the first term in the infinite sum dominates. Truncating the sum to first order gives an approximate solution:

$$\Phi(\rho,\ \phi) \cong V + a_1 \rho^{\frac{\pi}{\beta}} sin\left(\frac{\pi}{\beta}\phi\right) \tag{5.24}$$

Taking the negative of the gradient of Eq. 5.24, the electric field components become:

$$E_\rho(\rho,\ \phi) = -\frac{\partial \Phi}{\partial \rho} \cong -\frac{a_1 \pi}{\beta} \rho^{\frac{\pi}{\beta}-1} sin\left(\frac{\pi}{\beta}\phi\right) \tag{5.25}$$

$$E_\phi(\rho,\ \phi) = -\frac{1}{\rho}\frac{\partial \Phi}{\partial \phi} \cong -\frac{a_1 \pi}{\beta} \rho^{\frac{\pi}{\beta}-1} cos\left(\frac{\pi}{\beta}\phi\right) \tag{5.26}$$

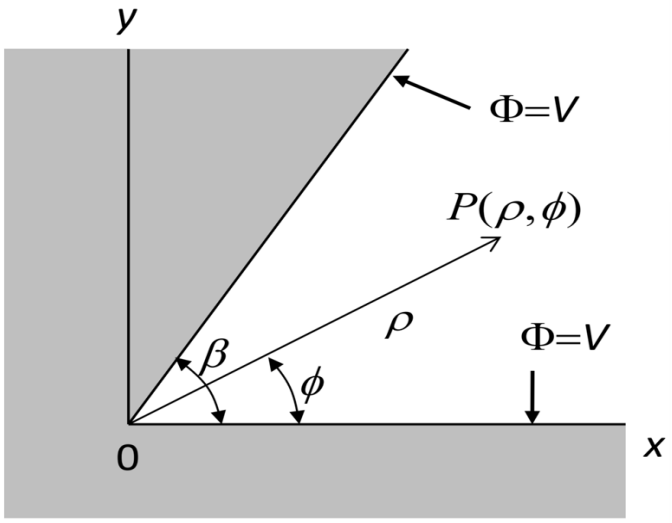

Figure 5.3: A schematic cross-section of two planar conductors intersecting at a corner. In this illustration, the 2DES on the i-Si surface is represented by the plane at $\phi = 0$ and the ohmic contact sidewall is represented by the plane at $\phi = \beta$, with the corner at $\rho = 0$ representing the SOI-Si bond edge. The electric field, and thus the surface charge density, must go to zero at the corner when $\beta < \pi$.

If we assume the conducting plate at $\phi = \beta$ is the ohmic contact side wall, and the conducting plate at $\phi = 0$ is the 2DES on the intrinsic Si(111) surface (see Figs. 5.3 and 5.4), we can deduce the nature of the surface charge density of the 2DES, $\sigma(\rho,\ 0)$, near the corner. The charge density along the plane $\phi = 0$ can be written:

$$\sigma(\rho,\ 0) = \varepsilon_0 E_\phi(\rho,\ 0) \cong -\frac{a_1 \pi \varepsilon_0}{\beta} \rho^{\frac{\pi}{\beta}-1} \tag{5.27}$$

For simplicity, I assume the SOI-Si bond edge intersects at a right angle, with $\beta = \frac{\pi}{2}$. The expression for the charge density of the 2DES along the Si(111) surface then becomes:

$$\sigma(\rho,\ 0) = -2a_1 \varepsilon_0 \rho \tag{5.28}$$

In this case we see that the charge density is linear in ρ. This is different from a normal SB where the charge density inside the depletion width is a constant given by the ionized donor density N_d. This will affect the shape of the SB potential $\phi(x)$, as we shall see. Now, if I fix the coordinate system to $\phi = 0$, I can return to Cartesian coordinates so that $\rho \longrightarrow x$. Equation 5.28 then becomes:

$$\sigma(x) = -2a_1 \varepsilon_0 x \tag{5.29}$$

To determine a_1, I impose the boundary condition that at the depletion width x_d the 2D charge density becomes the full density of the 2DES far away from the corner:

$$\sigma(x_d) = en = -2a_1 \varepsilon_0 x_d \tag{5.30}$$

thus:

$$a_1 = -\frac{en}{2\varepsilon_0 x_d}. \tag{5.31}$$

The charge density inside the depletion width then becomes:

$$\sigma(x) = \frac{en}{x_d} x \tag{5.32}$$

For this example, I chose an ideal angle $\beta = \frac{\pi}{2}$ to represent the corner of the SOI-Si bonding interface, although a more acute angle may model the interface more realistically. For example, if I choose an angle such as $\beta = \frac{\pi}{4}$ to represent the corner, to account for the rounded and sloped sidewall of the ohmic contacts (see Fig. 5.1), the surface charge

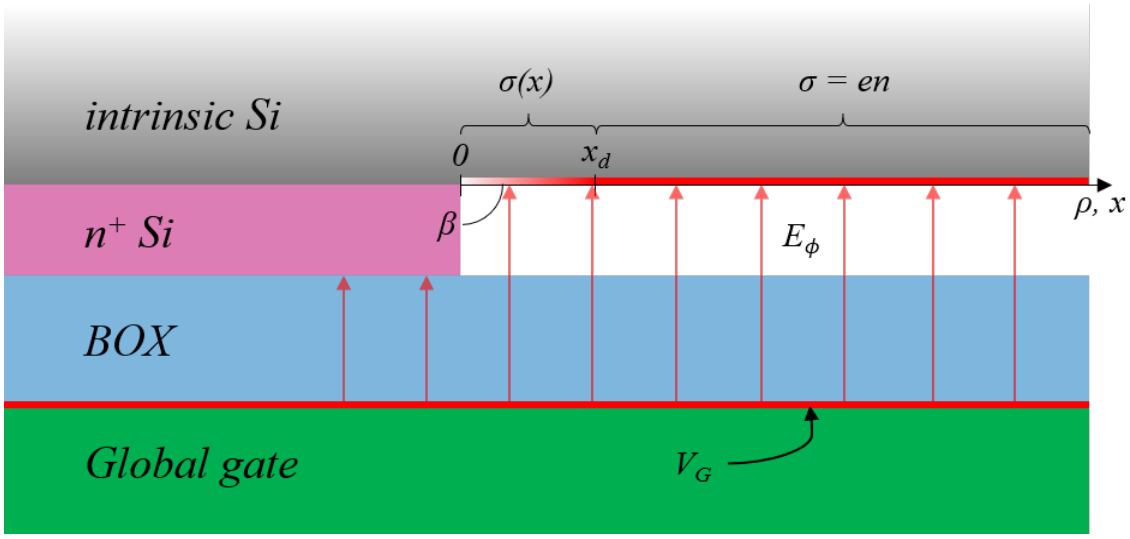

Figure 5.4: Schematic cross-section of the 2DES on the intrinsic Si surface and the ohmic contact on the SOI piece intersecting at a corner. In this illustration, $\beta = \frac{\pi}{2}$, but in reality β is probably less than $\frac{\pi}{2}$ due to sidewall rounding and other imperfections (see Fig. 5.1). The depletion width x_d defines the domain over which the electron surface charge density varies as described by Eq. 5.32. Both the 2DES density and the electric field E_ϕ from the global gate must vanish at the SOI-Si bond edge.

density in Eq. 5.32 would scale as $\sigma(\rho,0) \sim \rho^3$. Future modeling of this interface may require modifications such as this, or the inclusion of higher order terms in Eq. 5.23.

5.1.3 Schottky barrier potential: Poisson's equation

The task now is to solve the 1D Poisson equation to find $\phi(x)$ given the charge configuration $\sigma(x)$. Equation 5.32 has units of charge per unit area, however, so we must convert this 2D charge density into an effective 3D charge density. Assuming that the 2DES occupies a finite thickness Δz, the effective 3D charge density is:

$$P(x) = \frac{\sigma(x)}{\Delta z} \tag{5.33}$$

From § 2.1 that the 2DES thickness can be written in terms of the Fermi wave vector for a 2D system as:

$$\Delta z = \frac{2\pi}{k_F} = \frac{2\pi}{\sqrt{g_v g_s \pi n}} = \sqrt{\frac{4\pi}{g_v g_s n}} \tag{5.34}$$

The 1D Poisson equation for our system is thus:

$$\frac{d^2\phi(x)}{dx^2} = \frac{P(x)}{\varepsilon_s} = \sqrt{\frac{g_v g_s e^2 n^3}{4\pi\varepsilon_s^2}} \left(\frac{x}{x_d}\right). \tag{5.35}$$

The general solution to this equation can be found by integrating twice to obtain:

$$\phi(x) = \sqrt{\frac{g_v g_s e^2 n^3}{4\pi\varepsilon_s^2}} \left(\frac{x^3}{6x_d}\right) + Ax + B \tag{5.36}$$

where A and B are integration constants. Let's also recall that the 2DES density n is

controlled by the global gate voltage V_G which are related via Eq. 2.65 where $n = \frac{C}{e}V_G$. Plugging this into Eq. 5.36 yields:

$$\phi(x) = \sqrt{\frac{g_v g_s C^3 V_G^3}{16\pi e \varepsilon_s^2}} \left(\frac{x^3}{3x_d}\right) + Ax + B \tag{5.37}$$

I can now impose boundary conditions on $\phi(x)$ to find A and B. For convenience, I will set the zero-point of $\phi(x)$ to be located at the Fermi level E_{Fm} of the ohmic contact, which is equal to the Fermi level in the 2DES when $V_a = 0$. Examining Fig. 5.2, I apply the following boundary conditions:

$$\phi(x) = \begin{cases} \phi_B & x = 0 \\ V_a & x \geq x_d \end{cases} \tag{5.38}$$

and:

$$\phi'(x_d) = 0 \quad \text{(flat-band condition)} \tag{5.39}$$

Starting with the first boundary condition, if I plug in $x = 0$ into Eq. 5.37 I find:

$$\phi(0) = \phi_B = B \tag{5.40}$$

Next, I take the second boundary condition and plug in $x = x_d$ into Eq. 5.37 to get:

$$\phi(x_d) = V_a = \sqrt{\frac{g_v g_s C^3 V_G^3}{16\pi e \varepsilon_s^2}} \left(\frac{x_d^3}{3x_d}\right) + Ax_d + \phi_B \tag{5.41}$$

Solving for A and letting $\psi_0 = \phi_B - V_a$ gives:

$$A = -\left[\sqrt{\frac{g_v g_s C^3 V_G^3}{16\pi e \varepsilon_s^2}}\left(\frac{x_d}{3}\right) + \frac{\psi_0}{x_d}\right] \tag{5.42}$$

and the new expression for the SB potential is given by:

$$\phi(x) = \sqrt{\frac{g_v g_s C^3 V_G^3}{16\pi e \varepsilon_s^2}}\left(\frac{x^3}{3x_d}\right) - \left[\sqrt{\frac{g_v g_s C^3 V_G^3}{16\pi e \varepsilon_s^2}}\left(\frac{x_d}{3}\right) + \frac{\psi_0}{x_d}\right] x + \phi_B \tag{5.43}$$

To find the depletion width x_d I now impose the third boundary condition (Eq. 5.39) that $\phi(x)$ must return to the flat-band condition at $x = x_d$, or that the derivative of $\phi(x)$ with respect to x evaluated at x_d must vanish:

$$\phi'(x_d) = 0 = \sqrt{\frac{g_v g_s C^3 V_G^3}{16\pi e \varepsilon_s^2}}\left(\frac{x_d^2}{x_d}\right) - \left[\sqrt{\frac{g_v g_s C^3 V_G^3}{16\pi e \varepsilon_s^2}}\left(\frac{x_d}{3}\right) + \frac{\psi_0}{x_d}\right] \tag{5.44}$$

Solving for x_d yields the depletion width which depends on the SB barrier height, the capacitance of the global gate configuration, which for our devices is roughly 7 nF·cm^{-2}, the applied gate voltage, and any valley or spin degeneracies that are present:

$$x_d = \left(\frac{36\pi e \varepsilon_s^2 \psi_0^2}{g_v g_s C^3 V_G^3}\right)^{1/4} \tag{5.45}$$

Plugging this expression back into Eq. 5.43, we get a cleaner expression for the SB potential in terms of the SB height, the depletion width, and the applied source-drain voltage, which for the domain $0 \geq x \geq x_d$ is given by:

$$\phi(x) = \phi_B + \frac{\psi_0}{2}\left[\left(\frac{x}{x_d}\right)^3 - 3\left(\frac{x}{x_d}\right)\right] \tag{5.46}$$

A plot of Eq. 5.46 normalized by the SB height is shown in Fig. 5.5 for a range of global gate voltages V_G under zero applied bias ($\psi_0 = \phi_B$) and for a SB height of $\phi_B = E_0^z/e = 0.0195$ V.

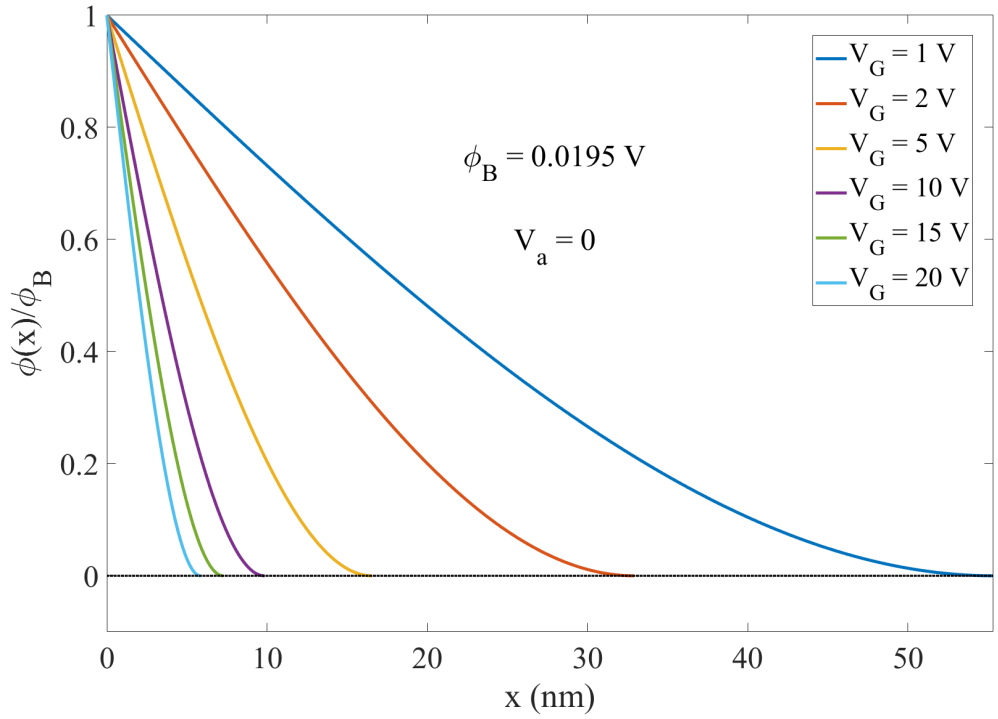

Figure 5.5: Plot of $\phi(x)/\phi_B$ vs x from Eq. 5.46 and plotted for a range of global gate voltages V_G, for a SB height of $\phi_B = E_0^z/e = 0.0195$ V, and for zero applied source-drain bias. This plot illustrates $\phi(x)$ is highly dependent on the applied gate voltage.

It is clear from Fig. 5.5 and Eq. 5.45 that the depletion width x_d depends on the applied gate voltage V_G, and more specifically that $x_d \sim V_G^{-3/4}$. To see this more clearly, a log-log plot of the depletion width vs. the global gate voltage is shown in Fig. 5.6.

This is extremely important, because it means I can control x_d with an applied gate voltage. But I did not want to rely solely on the global gate voltage to set x_d, because this introduces a large 2DES density far away from the SOI-Si contact edge. Instead, I introduced additional electrostatic gates that were independent of the global gate. This allowed me to tune the electrostatics at the SOI-Si bond edge, while allowing independent

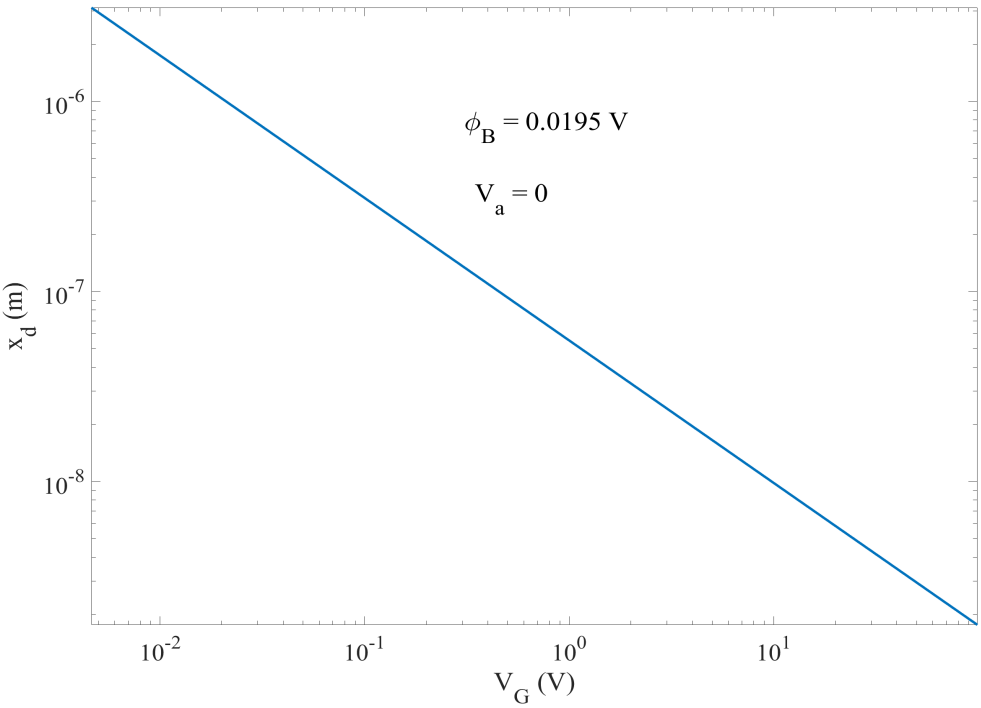

Figure 5.6: x_d from Eq. 5.45 plotted as a function of the global gate voltage V_G for a SB height of $\phi_B = E_0^z/e = 0.0195$ V and for zero applied source-drain bias. This plot illustrates that the depletion width x_d and thus the tunneling barrier width, can be controlled by an applied gate voltage.

control of the 2DES density. The addition of these extra gates to our device architecture is the focus of § 5.2.

Now that I have an expression for the SB potential, I can plug $\phi(x)$ from Eq. 5.46 into Eq. 5.6 to find the tunneling probability through the junction:

$$\Theta(x) = \exp\left(-\frac{2\sqrt{2m^*e}}{\hbar}\int_0^w \sqrt{\phi_B + \frac{\psi_0}{2}\left[\left(\frac{x}{x_d}\right)^3 - 3\left(\frac{x}{x_d}\right)\right]}\,dx\right) \tag{5.47}$$

For the forward-bias case, the SB barrier width w is replaced by the depletion width x_d. For the reverse bias case, w becomes w_R (see Fig. 5.2) and is not equal to the depletion width; to find w_R I must solve for $\phi(w_R) = 0$. I now examine both bias conditions in turn.

For the case $V_a > 0$, I take $\phi(x)$ and subtract out V_a, since V_a is the new zero-point or E_{Fs}. Subtracting V_a from $\phi(x)$ takes $\phi_B \longrightarrow \psi_0$ and gives:

$$\Theta_F(x) = \exp\left(-\frac{2\sqrt{2m^*e}}{\hbar}\int_0^{x_d} \sqrt{\psi_0 + \frac{\psi_0}{2}\left[\left(\frac{x}{x_d}\right)^3 - 3\left(\frac{x}{x_d}\right)\right]}\,dx\right). \tag{5.48}$$

Completing the integration gives:

$$\Theta_F(x) = \exp\left(-\frac{2\sqrt{2m^*e\psi_0}}{\hbar}\left[\frac{6}{5}\left(\sqrt{6}-2\right)x_d\right]\right) \tag{5.49}$$

and simplifies to:

$$\Theta_F(x) = \exp\left(-x_d\Lambda_F\sqrt{\frac{2m^*e}{\hbar^2}}\right) \tag{5.50}$$

where Λ_F is given by:

$$\Lambda_F = \left[\frac{12\psi_0^{1/2}(\sqrt{6}-2)}{5} \right] \tag{5.51}$$

For $V_a < 0$, the integral in Eq. 5.47 cannot be expressed in terms of elementary functions. Instead, I must either introduce elliptic integrals or find an approximation for $\phi(x)$ that can be readily integrated. For the latter scenario, the simplest approximation of $\phi(x)$ for $V_a < 0$ is a straight line passing through the points $(0, \phi_B)$ and $(w_R, 0)$. This is known as the triangular, or linear, potential approximation, and is given by:

$$\phi_{lin}(x) = \phi_B \left(1 - \frac{x}{w_R} \right). \tag{5.52}$$

Plugging this expression into Eq. 5.38, gives:

$$\Theta_R^{lin}(x) = \exp\left(-\frac{2\sqrt{2m^*e}}{\hbar} \int_0^{w_R} \sqrt{\phi_B \left(1 - \frac{x}{w}\right)} dx \right) \tag{5.53}$$

which upon integrating becomes:

$$\Theta_R^{lin}(x) = \exp\left(-\frac{2\sqrt{2m^*e\phi_B}}{\hbar} \left[\frac{2}{3} w_R \right] \right) \tag{5.54}$$

and simplifies to:

$$\Theta_R^{lin}(x) = \exp\left(-w_R \Lambda_R^{lin} \sqrt{\frac{2m^*e}{\hbar^2}} \right), \tag{5.55}$$

where Λ_R^{lin} is given simply by:

$$\Lambda_R^{lin} = \left[\frac{4\phi_B^{1/2}}{3}\right]. \tag{5.56}$$

The triangular approximation is valid when $|V_a|$ is on the order of ϕ_B. However, when $|V_a| << \phi_B$, this approximation significantly overestimates the potential. A better approximation of $\phi(x)$ is a parabola. Just like the triangular approximation, I can construct a parabola by demanding that it pass through the points $(0,\phi_B)$ and $(w_R,0)$; however, we must now choose a third point that will uniquely define the parabola that will best approximate $\phi(x)$. A convenient choice is to simply pick the mid-point $(\frac{w_R}{2},\phi_M)$, where $\phi_M = \phi(\frac{w_R}{2})$. After a bit of algebra, I find that the unique parabola passing through these three points is:

$$\phi_{par}(x) = \phi_B - [3\phi_B - 4\phi_M]\left(\frac{x}{w_R}\right) + [2\phi_B - 4\phi_M]\left(\frac{x}{w_R}\right)^2 \tag{5.57}$$

This parabolic approximation is plotted in Figs. 5.7-5.10 and provides a reasonable model for my purposes. In order to find w_R, we must set Eq. 5.46 equal to zero, and solve the cubic equation:

$$\phi(w_R) = 0 = \phi_B + \frac{\psi_0}{2}\left[\left(\frac{w_R}{x_d}\right)^3 - 3\left(\frac{w_R}{x_d}\right)\right] \tag{5.58}$$

After a bit more algebra, the tunneling width for the reverse bias condition is given by the second (middle) root of Eq. 5.58:

$$w_R = x_d\left[\frac{1}{2}\left(\Xi + \frac{1}{\Xi}\right) + \frac{i\sqrt{3}}{2}\left(\Xi - \frac{1}{\Xi}\right)\right] \tag{5.59}$$

where:

$$\Xi = \left[\frac{\phi_B}{\psi_0} - \sqrt{\left(\frac{\phi_B}{\psi_0}\right)^2 - 1} \right]^{1/3} \tag{5.60}$$

Plugging Eq. 5.57 into Eq. 5.6 and replacing w with w_R we get:

$$\Theta_R^{par}(x) = \exp\left(-\frac{2\sqrt{2m^*e}}{\hbar} \int_0^{w_R} \sqrt{\phi_B - [3\phi_B - 4\phi_M]\left(\frac{x}{w_R}\right) + [2\phi_B - 4\phi_M]\left(\frac{x}{w_R}\right)^2}\, dx \right) \tag{5.61}$$

After more algebra, I arrive at the expression for the reverse-bias tunneling probability in the parabolic approximation:

$$\Theta_R^{par}(x) = \exp\left(-w_R \Lambda_R^{par} \sqrt{\frac{2m^*e}{\hbar^2}} \right) \tag{5.62}$$

where Λ_R^{par} is given by:

$$\Lambda_R^{par} = \left[\frac{K_1 K_2 + \left(K_1^2 - K_2^2\right) \ln\left(\frac{K_2 - K_1}{K_2 - K_3}\right)}{8K_4} \right] \tag{5.63}$$

and the values K_1, K_2, K_3, and K_4 are given by:

$$K_1 = [3\phi_B - 4\phi_M] \tag{5.64}$$

$$K_2 = 2\sqrt{2\phi_B^2 - 4\phi_B\phi_M} \tag{5.65}$$

$$K_3 = 2\left[2\phi_B - 4\phi_M\right] \tag{5.66}$$

$$K_4 = \sqrt{8\phi_B^3 - 48\phi_B^2\phi_M + 96\phi_B\phi_M^2 - 64\phi_M^3} \tag{5.67}$$

While these expressions look complicated, they can easily be evaluated for a given ϕ_B and w_R. Having found the tunneling probability for the reverse-bias case in the parabolic potential approximation, the total 2D and 1D FE currents for a reverse applied bias is given by:

$$I_{2D} = L_{2D}A_{2D}^{*}T^{3/2}\left[\ln(2) - \ln\left(1 + \frac{\cosh\frac{e(\phi_B+V_a)}{2k_BT}}{\cosh\frac{e(\phi_B-V_a)}{2k_BT}}\right)\right]\exp\left(-w_R\Lambda_R^{par}\sqrt{\frac{2m^*e}{\hbar^2}}\right) \tag{5.68}$$

and:

$$I_{1D} = L_{1D}A_{1D}^{*}T\left[\ln(2) - \ln\left(1 + \frac{\cosh\frac{e(\phi_B+V_a)}{2k_BT}}{\cosh\frac{e(\phi_B-V_a)}{2k_BT}}\right)\right]\exp\left(-w_R\Lambda_R^{par}\sqrt{\frac{2m^*e}{\hbar^2}}\right). \tag{5.69}$$

Recall that due to the design of my devices, during any given measurement one side of the device will be under forward bias (the ohmic contact where the current is injected) while the other side will be under reverse bias (the ohmic contact where the current exits). This means that the total current will be limited by the contact with the larger resistance. For my devices, the reverse bias tunneling current is typically going to be the limiting factor (when $V_{sd} >> \phi_B$), thus I really only need to consider Eqs. 5.68 and 5.69 when modelling the data. This assumption breaks down when when $V_{sd} << \phi_B$, however, at which point the two contact resistances are roughly equal.

Figure 5.11 shows plots of I_{2D} and I_{1D} vs V_G, from Eqs. 5.68 and 5.69, respectively, which are plotted along with the 77 K and 4 K data from Fig. 4.5. The data are in better agreement with I_{1D} than with I_{2D}, at least in so far as the temperature dependence appears to be linear. This suggests that the primary transmission mechanism across the SB is due to electron tunneling at a few discrete SOI-Si bond points. This also indicates that the SOI-Si bond edge is not in intimate contact over the entire bond length ($\sim$ 3 mm for my devices), as we would like. The SOI-Si bond length L_{2D} used for the theoretical curve in this plot was 17 nm (see Table 5.1), which means that only about 0.0006% of the total bond length was accounted for. Only two points were used for generating the I_{1D} theory curve ($L_{1D} = 2$), i.e. only two $\sim$8.5 nm points were assumed to be in intimate contact along the SOI-Si bond edge. The SB height ϕ_B was chosen to be $\phi_B = E_0^z/e - \delta\phi = 0.0195 - 0.005$ V, where $\delta\phi$ is the effective barrier modification due to assumed image-charge lowering and interface states. This means I also assumed that $\phi_{B0} = (E_c - E_{Fs})/e = 0$. This model is fairly crude. In particular, it did not account for the current at low V_G, nor were image-charge or interface states thoroughly examined; thus there is room for improvement both in the analysis and the sample preparation.

Table 5.1: List of parameters used for the I_{1D} and I_{2D} current models plotted in Fig. 5.11.

Parameter	Symbol	Value
Schottky Barrier Height	ϕ_B	14.5 mV
Applied Voltage	V_a	100 mV
Global Gate Capacitance	C	7 nF cm^{-2}
Temperature	T	77 K and 4 K
1D Bond Points	L_{1D}	2
2D Bond Length	L_{2D}	17 nm
Valley Degeneracy	g_v	6
Spin Degeneracy	g_s	2

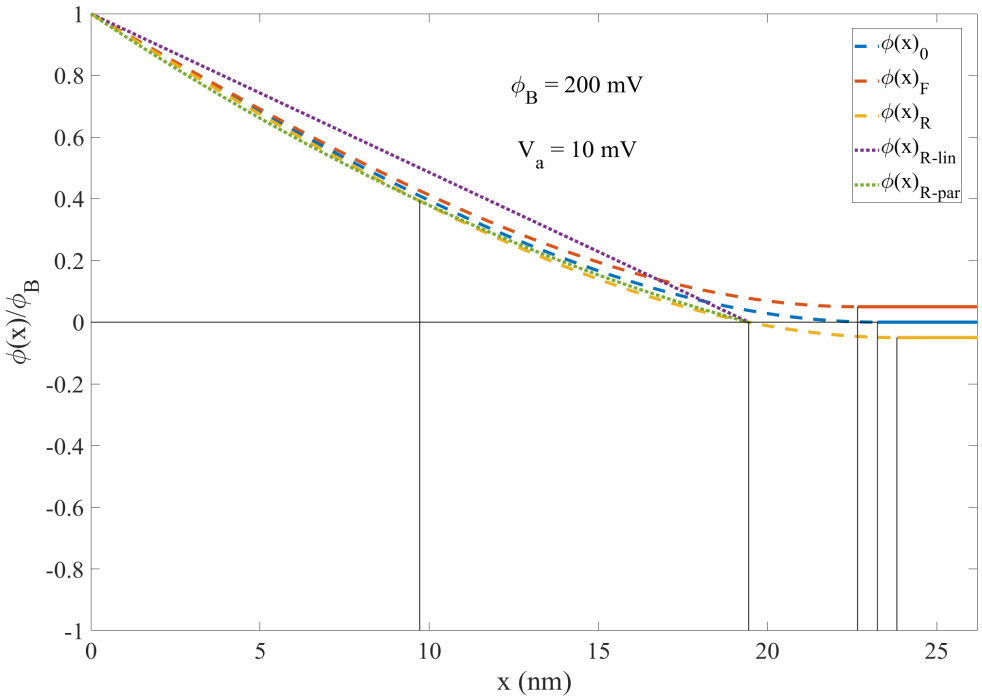

Figure 5.7: Plot of $\phi(x)/\phi_B$ vs x for the zero- (blue), forward- (orange), and reverse-bias (yellow) cases, as well as the triangular (purple) and parabolic (green) approximations to $\phi(x)$ for the reverse-bias case. Here $\phi_B >> V_a$, and in this limit $\phi(x)_{lin}$ overestimates $\phi(x)$ and $\phi(x)_{par}$ is a better approximation. From left to right, the vertical lines represent $\frac{w_R}{2}$, w_R, and x_d for the forward-, zero-, and reverse-bias cases, respectively.

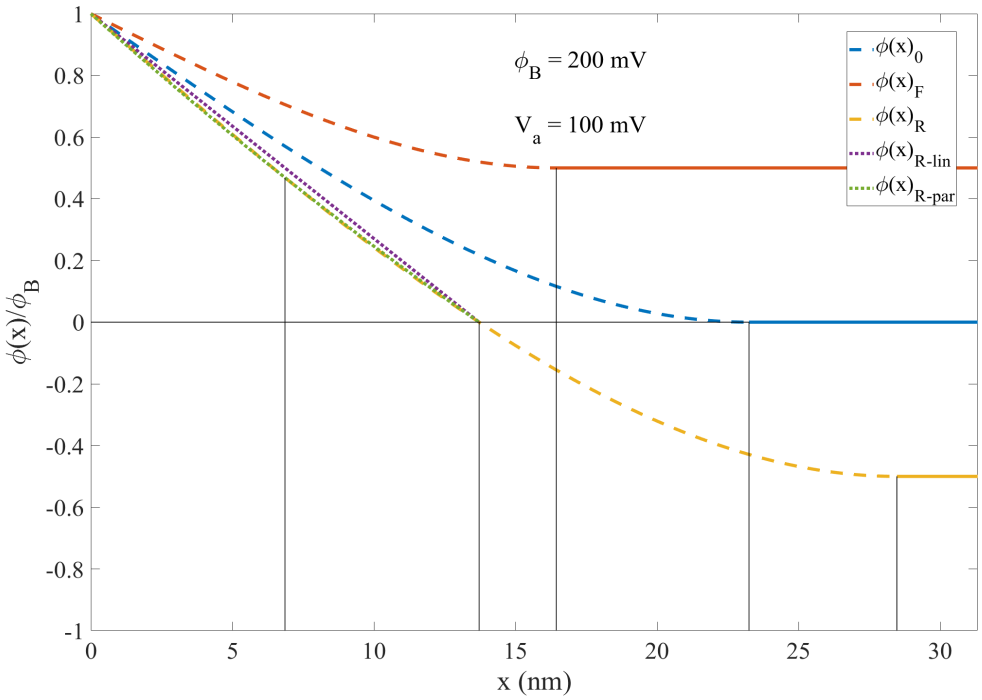

Figure 5.8: Plot of $\phi(x)/\phi_B$ vs x for the zero- (blue), forward- (orange), and reverse-bias (yellow) cases, as well as the triangular (purple) and parabolic (green) approximations to $\phi(x)$ for the reverse-bias case. Here $\phi_B > V_a$, and in this limit $\phi(x)_{lin}$ slightly overestimates $\phi(x)$ while $\phi(x)_{par}$ is still a slightly better approximation to $\phi(x)$. From left to right, the vertical lines represent $\frac{w_R}{2}$, w_R, and x_d for the forward-, zero-, and reverse-bias cases, respectively.

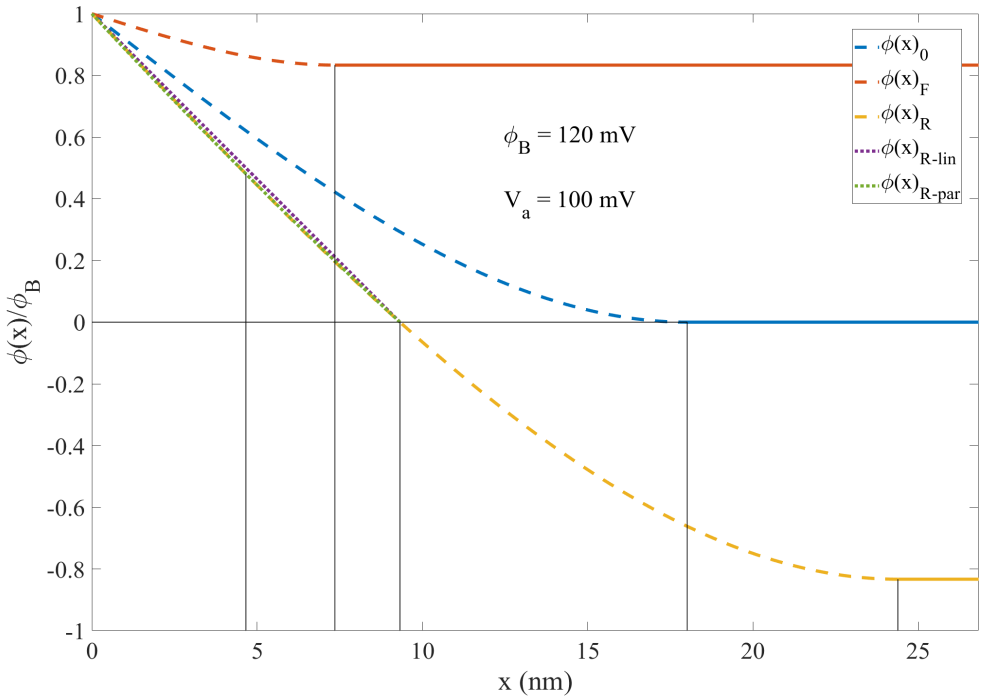

Figure 5.9: Plot of $\phi(x)/\phi_B$ vs x for the zero- (blue), forward- (orange), and reverse-bias (yellow) cases, as well as the triangular (purple) and parabolic (green) approximations to $\phi(x)$ for the reverse-bias case. Here $\phi_B \sim V_a$, and in this limit $\phi(x)_{lin}$ and $\phi(x)_{par}$ are both good approximations to $\phi(x)$, with $\phi(x)_{par}$ being marginally better. From left to right, the vertical lines represent $\frac{w_R}{2}$, x_d for the forward-bias case, w_R, and x_d for the zero- and reverse-bias cases, respectively.

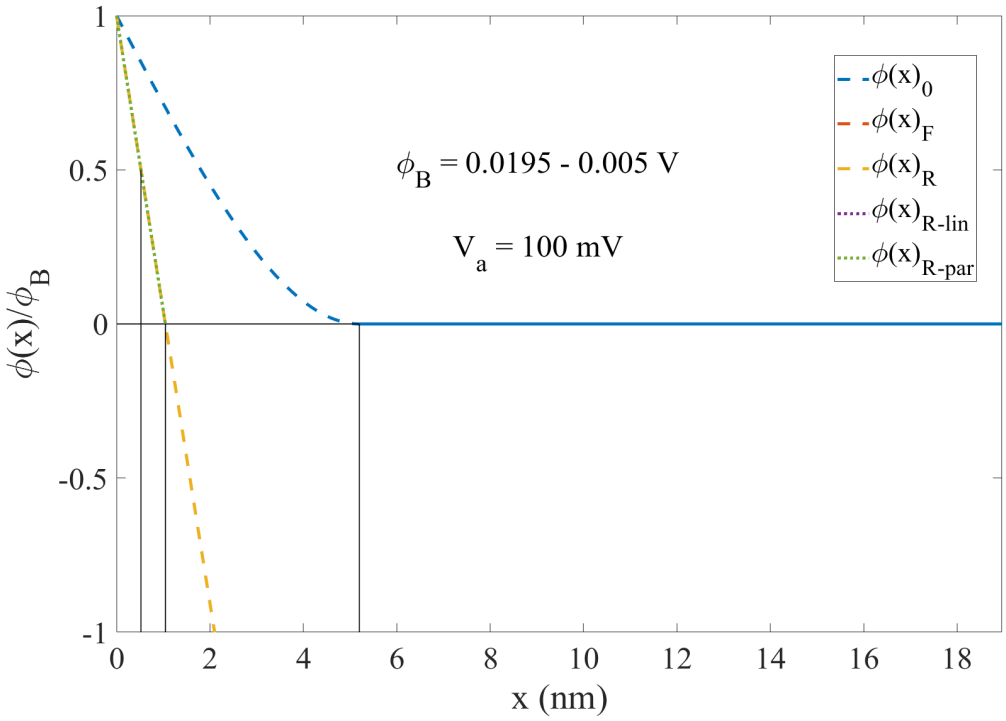

Figure 5.10: Plot of $\phi(x)/\phi_B$ vs x for the zero- (blue), forward- (orange), and reverse-bias (yellow) cases, as well as the triangular (purple) and parabolic (green) approximations to $\phi(x)$ for the reverse-bias case. Here $\phi_B < V_a$, and in this limit $\phi(x)_{lin}$ and $\phi(x)_{par}$ are good approximations of $\phi(x)$. Notice that the forward bias case is cut off in the plot because the conduction band here is greater than the SB height. From left to right, the vertical lines represent $\frac{w_R}{2}$, w_R, and x_d for zero-bias case.

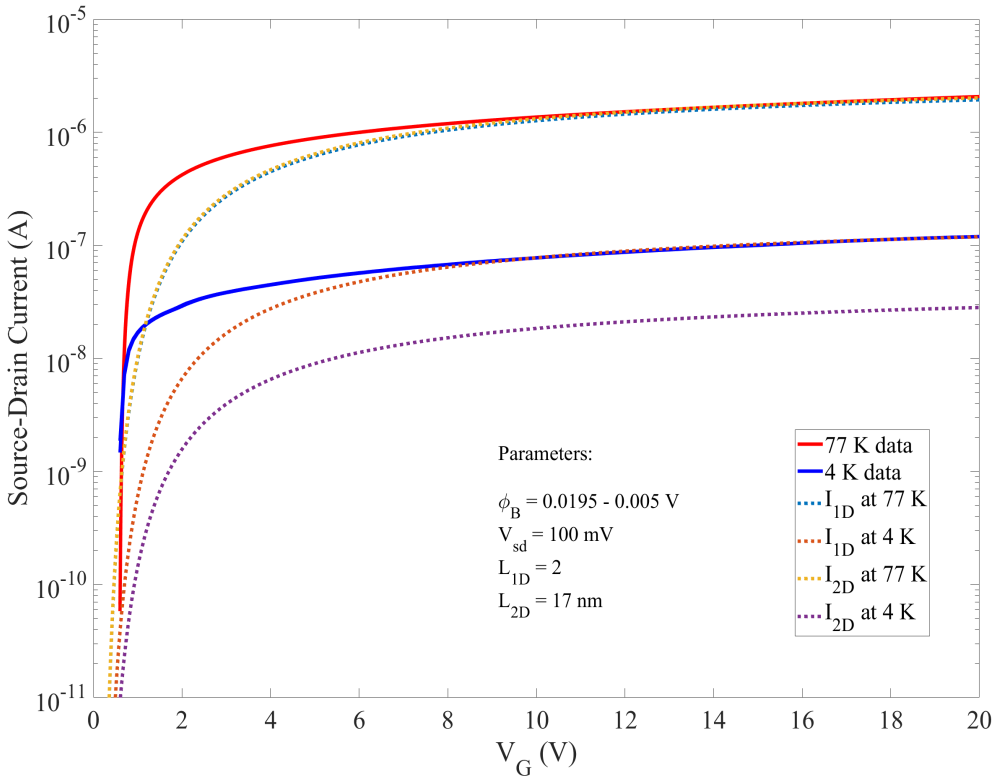

Figure 5.11: Plot of measured current vs V_G at 77 K (solid red) and 4 K (solid blue), and modeled current I_{1D} and I_{2D} vs V_G. This is the same data shown in Fig. 4.5. The data are in better agreement with I_{1D} (dashed blue and orange) than I_{2D} (dashed yellow and purple). This suggests that the primary transmission mechanism across the SB is due to electron tunneling at a few discrete SOI-Si bond points.

5.2 Proximity enhancement gates – Paris

Given the constraints on the current injection across the SOI-Si bond edge, I now discuss one approach I used to lower $R_{contact}$ through the implementation of independent gates. As I mentioned previously, I wanted to control the width of the SB using a gate voltage, but I did not want to rely solely on the global gate because I needed independent control of that gate for the 2DES density. To this end, I developed integrated proximity enhancement gates (PEGs) into my devices. In contrast to the proximity depletion gates (PDGs), the PEGs are positioned on the SOI piece in very close proximity (∼25 nm) to the ohmic contacts using a self-aligned metallization process. Figure 5.12 shows a rough illustration of the SOI-Si bond edge with the inclusion of a PEG.

For this experiment, I reverted back to the two-terminal SOI design in an attempt to simplify the problem and determine the viability of using PEGs as to fix the contact resistance issue.

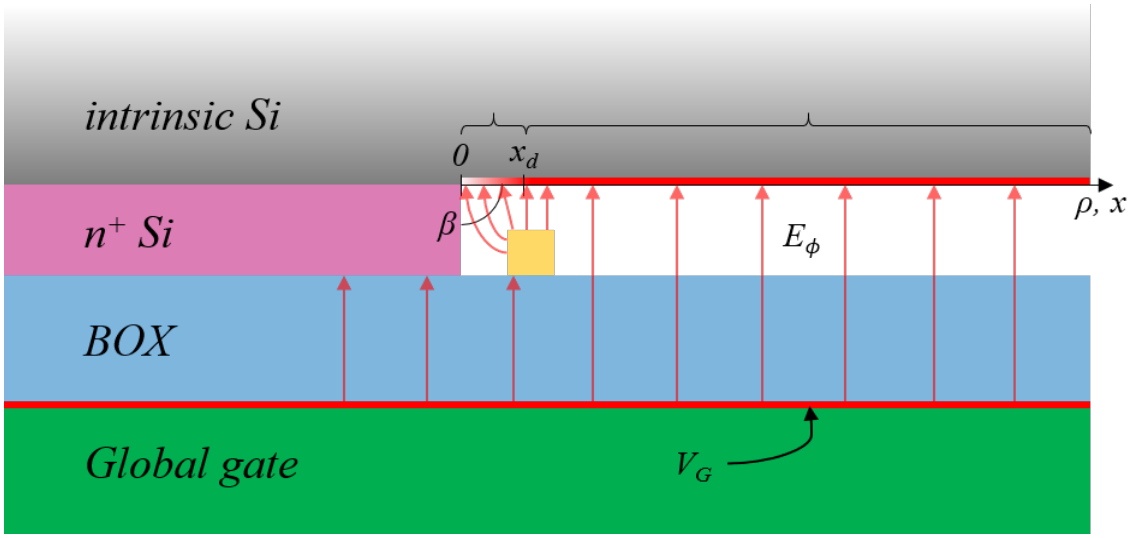

Figure 5.12: Schematic cross-section of the 2DES on the intrinsic Si surface and the ohmic contact on the SOI piece intersecting at a corner. This illustration is almost identical to Fig. 5.4, but here I have included the qualitative effects of a proximity enhancement gate (PEG). Notice that the depletion width x_d has been decreased compared with Fig. 5.4. The addition of the PEG allows control of x_d while still maintaining independent control of the 2DES density using the global gate, V_G.

The fabrication of the 2-terminal PEG devices begins the same way as a normal 2- or 4-terminal device, as described in § 3.5.2. I started by thinning the SOI wafer through a series of thermal oxidations and oxide removal in BOE (6:1). After top-Si thinning, the normal lithography step to define the ohmic contacts was replaced by a lift-off lithography step; an additional ∼35 nm lift-off resist (LOR) layer was applied before the normal photoresist layer. The top-Si was etched using RIE to define the ohmic contacts, and then immediately afterwards a ∼20 nm layer of chromium was deposited onto the exposed BOX using an e-beam evaporator. This etch-deposition step is the self-aligned metallization step referred to earlier, which enabled the boundaries of the deposited Cr to be self-aligned to the ohmic contacts that were previously etched. With continued improvement of the recipe for these etch and metallization steps, I achieved self-alignment of the metal-ohmic contacts to within ∼25 nm (see Fig. 5.13).

Lift-off was performed by a double-bath immersion of the SOI wafer in Remover PG (80 °C, 30 minutes), a fresh solution of Remover PG (80 °C, 10 minutes), followed by a DIW rinse and N_2 blow-dry. If additional cleaning was necessary, the SOI wafer was immersed in a fresh piranha bath (3:1 H_2SO_4:H_2O_2) for about 5 minutes, followed by a DIW rinse and N_2 blow-dry. Like Ta and Au, Cr has good adhesion to SiO_2 and has excellent corrosion resistance to both piranha and dilute HF solutions [190]. As a side note, I expect that the Ta/Au proximity depletion gates (PDGs) described in §3.5.3 could be replaced by a single Cr layer in future device runs.

Following lift-off of the Cr, the SOI wafer was patterned using standard photolithography in order to define the PEGs through a Cr wet-etch. After lithography, the SOI wafer was immersed in a diluted (2:1 Chrome-Etchant:DIW) solution for 10 s to remove all of the Cr except where the PEGs would remain (see Fig. 5.13). After the Cr wet-etch, the SOI wafer was immediately rinsed in DIW to stop the etch and was blown dry with N_2. Old photoresist was removed using the same acetone/IPA/DIW/piranha/DIW/SRD procedure described in § 3.5.2. A protective resist film was then deposited, the wafer was mounted

to dicing tape, and was diced into 5.6 x 10 mm^2 samples. From here, I followed the same wet-chemical preparation, bonding, and wiring procedure outlined in § 3.5.5.

After the device was wired, it was mounted to the dipstick apparatus and lowered into liquid nitrogen for measurement at 77 K. Upon passing the routine device operation tests, the source-drain current was measured as the PEG voltage was swept. Specifically, a global gate voltage of $V_G = 10$ V and a source-drain bias $V_{sd} = 100$ mV were applied to the device while both PEGs were swept from $V_{PEG} = -1$ V to 1 V. As can be seen in Fig. 5.14, the PEG leakage was minimal for reverse biases but significant at forward biases, much like the PDGs in Fig. 4.2. It can be seen, however, that for PEG voltages in the $\approx 0.3 - 0.6$ V range there was enhancement of the source-drain current. Above this range, the PEG leakage current began to dominate and the I-V characteristics broke down.

Leakage from the PEGs and PDGs (or any proximity gate that may be fabricated on the SOI piece) to the 2DES at forward biases was an ongoing issue that I was not able to fully resolve. However, I saw continued improvement in the leakage as I continued to refine the metalization process. Furthermore, I have measured the PEG leakage to the ohmic contacts for un-bonded devices (just the SOI piece) and saw little to no leakage in those devices. This indicates that there was good isolation between the ohmic contacts and the PEGs across the $\sim$25 nm gap, and suggests that the leakage was coming from PEG contact to the 2DES on the H-Si(111) piece possibly due to contamination or Cr nodules on the PEG surface that shorted to the 2DES.

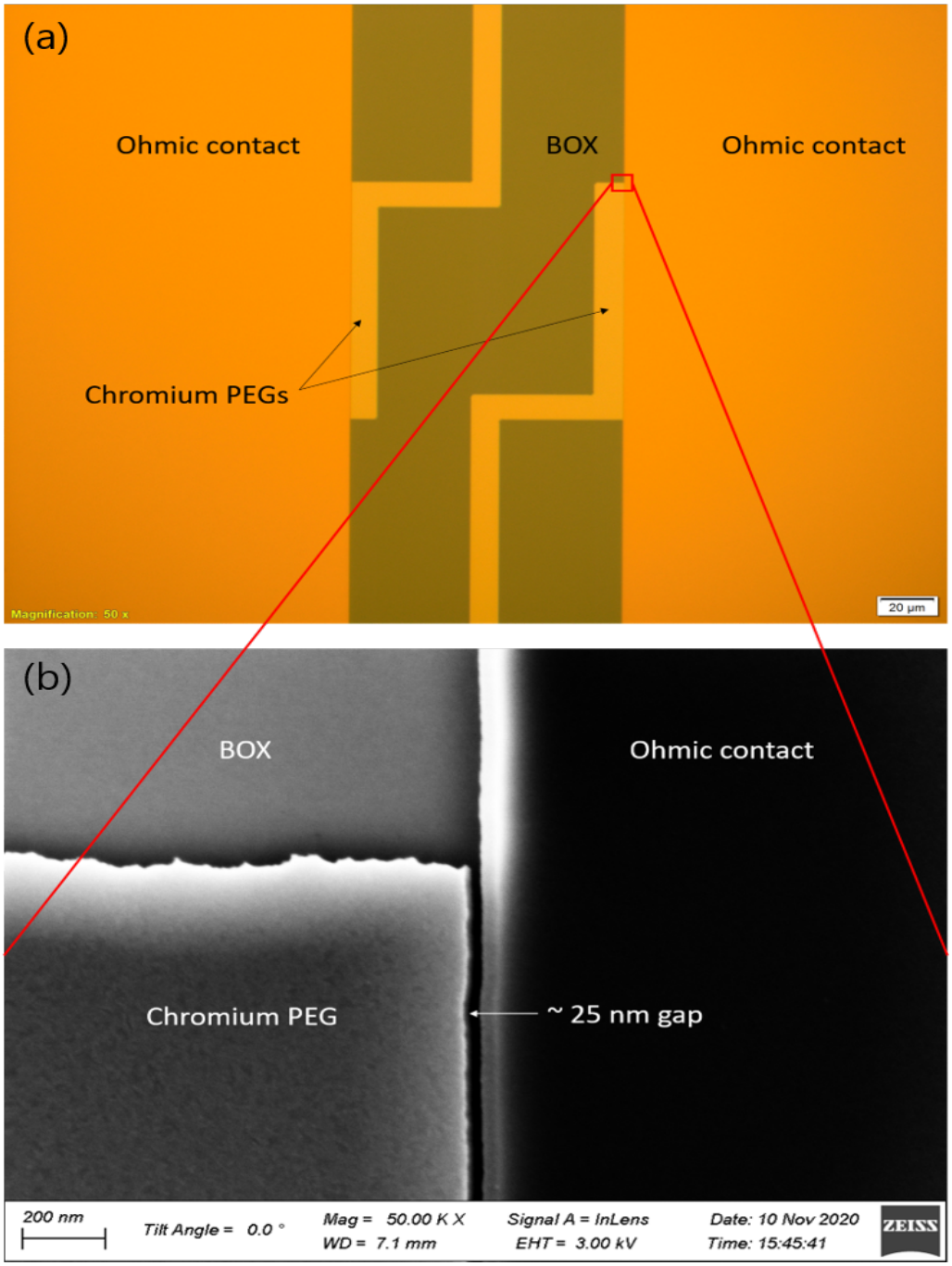

Figure 5.13: (a) An optical micrograph and (b) an SEM micrograph (bottom) of the PEGs in a two-terminal device. The ∼25 nm gap extends the entire length of the PEG-ohmic contact edge (100 μm) and we have shown that there is good electrical isolation across this gap from leakage measurements of unbonded devices. Leakage from the PEGs to the ohmic contacts for bonded devices is due to electrical shorts from the PEGs to the 2DES, caused either by contamination or by Cr nodules on the PEG surface that make physical contact with the 2DES.

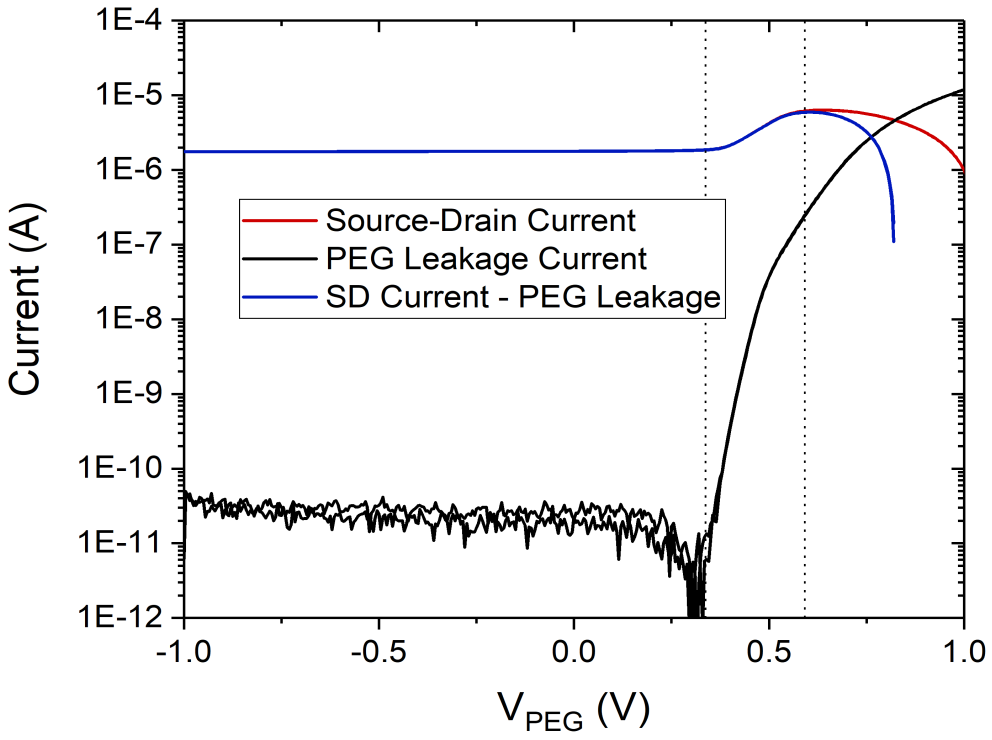

Figure 5.14: Plot of the source-drain current (red) and the PEG leakage current (black) vs V_{PEG} from a 2-terminal device with $V_G = 10$ V, $V_{sd} = 100$ mV, and T = 77 K. The blue curve is the source-drain current with the background PEG leakage current subtracted. There is some source-drain current enhancement between $V_{PEG} \approx 0.3 - 0.6$ V, beyond which the leakage current begins to dominate and the I-V characteristics break down. Forward bias PEG leakage was an ongoing issue that I was not able to fully resolve.

Chapter 6: Iodine-terminated Si(111) surfaces

This chapter details my results of the first magnetotransport measurements made on an iodine-terminated Si(111) (I-Si(111)) surface. The experiment was part of a collaboration between the Kane lab and the Butera lab at the Laboratory for Physical Sciences. Using our novel non-invasive SOI gating architecture, we were able to successfully Van der Waals bond to a I-Si(111) sample that was terminated with iodine in a UHV chamber by the Butera group. *In situ* X-ray photoelectron spectroscopy (XPS) and scanning tunneling microscopy (STM) measurements were provided by the Butera group, and 2D magnetotransport measurements were carried out by the Kane group. A special thank you to Dr. Kevin Dwyer for the many hours he spent exposing and collecting data on these samples.

6.1 Introduction

As I mentioned in Ch. 1, Si surfaces terminated in heavy halogens, and in particular iodine, are expected to exhibit enhanced spin-orbit interactions, and this could lead to topologically insulating behavior [97, 98]. Halogen terminated Si surfaces have been well-studied using topographical and spectroscopic analyses, in part because halogen-based plasmas are commonly used during the fabrication of Si-based electronics [197]. Most such investigations have focused on the impact of halogenation on the surface structure as the result of etching reactions. More recently, the halogen-Si system has received renewed attention as the basis of surface functionalization experiments to achieve desired surface terminations. For example, Butera et al. explored the stability of halogen-terminated Si surfaces in ambient environments to facilitate atomically precise surface functionalization

[59, 60].

In contrast, measurement of 2D electron transport on these surfaces, where we would expect to see effects from enhanced spin-orbit coupling, has not been previously reported. A related study examined the formation of a 2D hole system on a Cl-Si(111) surface, however, the surface oxidized rapidly and the measurements were poor [198]. The primary reasons for the lack of 2D transport data on X-Si surfaces are likely two-fold. First, it has been uncertain as to how stable X-Si surfaces are under ambient conditions. Only recently has Butera et al. demonstrated that the I-Si surface is actually quite stable against oxidation, hydration, and hydrocarbon physisorption under exposure to ambient lab conditions for over eight hours. The second possible reason for the lack of transport data on X-Si surfaces is due to the difficulties surrounding the electrostatic gating of these fragile surfaces. The surface must be carefully prepared in UHV (or using wet chemistry) and there cannot be an oxide or any other dielectric layer superimposed on the surface to act as an insulating layer for gate electrodes. Vacuum is probably the only suitable dielectric to achieve this, which is precisely the dielectric for my non-invasive SOI devices discussed in Ch. 3. Furthermore, because UHV preparation requires pristine materials, a means of electrical access to the 2DES on the pristine surface that does not require dopants is desirable. For these reasons, my non-invasive SOI devices are an ideal choice for the electrostatic gating and four-terminal probing of 2DESs on these surfaces.

To date, wet chemical processes have been used to achieve iodine termination of Si surfaces, however, these methods have primarily utilized methyl iodine [199–201]. In addition to depositing iodine these methods also deposit methyl groups, which can be deleterious to transport measurements and desired surface functionalization. Benzene iodine has been shown to be an improvement over methyl iodine [202]. However, this approach also results in trace amounts of undesired species termination, which is why gas-phase approaches to halogen termination are primarily used. Gas-phase halogenation has been demonstrated for both chlorination and bromination of H-Si(111) surfaces using pure Cl_2

and Br_2 gas at mTorr pressures [203, 204]. A different implementation must be used for gas-phase iodination of Si, however, which is why Butera et al. turned to a solid-state electrochemical source for their iodine experiments based in part on the work of Spencer et al. [205].

In the following sections, I present details of the I-Si(111) sample preparation, including the initial wet chemical treatment of the Si(111) surface and the dry UHV exposure. I then discuss preliminary surface data that was obtained on a I-Si(111) sample, including XPS and STM analysis. I also address the issues involved with surface reconstruction during heating and exposure. Finally, I present the first 2DES transport measurements of these surfaces and discuss my findings. Since this was the first experiment, my aim in this chapter is to establish an experimental procedure to measure transport on these surfaces. However, I cannot claim that I have found evidence of enhanced spin-orbit interactions. With refined preparation techniques, it may be possible to see these effects which I briefly discuss in the next section.

6.2 Spin-orbit coupling: the Rashba effect

The spin-orbit interaction is one of three relativistic corrections to the Hamiltonian of the Schrödinger equation, along with the relativistic correction to the kinetic energy and the zitterbewegung effect, that make up the fine structure observed in atomic spectral line splitting. The correction involves a coupling of the electron's spin with its orbital motion about a positively charged nucleus, which leads to inversion symmetry breaking. In the frame of the electron, the electron sees an effective magnetic field from the positively charged nucleus which appears to be orbiting around the electron. This effective magnetic field couples to the electron spin, giving rise to a momentum-dependent (inversion asymmetric) level splitting of the electron's energy spectra. In 3D and 2D crystalline systems, spin-orbit coupling manifests itself in what is known as the Rashba effect. The 3D case was first discovered by Rashba and Sheka in 1959 [206], and the 2D case was discovered

by Rashba and Bychov in 1984 [207]. The phenomenon has been well-studied both theoretically and experimentally for 2D systems in Si [208–219], including implications for qubit schemes [220]. The Rashba effect extends the notion of spin-orbit coupling in atomic systems to spin-band coupling in solid-state systems, and results from the combined effect of spin-orbit splitting and broken inversion symmetry of the crystalline potential due to applied electric fields. The simplest expression for this effect is given by the Rashba Hamiltonian:

$$H_R = -\alpha_R (\sigma \times \hat{\mathbf{p}}) \cdot \hat{z}, \tag{6.1}$$

where σ are the Pauli spin matrices, $\hat{\mathbf{p}}$ is the momentum operator, $\hat{z}$ is the direction of the applied electric field, and α_R is the Rashba parameter given by:

$$\alpha_R = -\frac{g\mu_B E_0}{2m^* c^2}. \tag{6.2}$$

Here, g is the electron g-factor, μ_B is the Bohr magneton, and E_0 is the magnitude of the applied electric field. For a 2DES where the applied electric field is perpendicular to the surface (as indicated by the dot-product with $\hat{z}$), the Rashba Hamiltonian becomes:

$$H_R = -\hbar\alpha_R (\sigma_x k_y - \sigma_y k_x) \tag{6.3}$$

The Rashba Hamiltonian can be included in the Hamiltonian for a 2DES, and gives rise to a crystal momentum-dependent band splitting. To lowest order in $\mathbf{k}_{||}$, where $\mathbf{k}_{||} = (k_x, k_y, 0)$, the Rashba spin-orbit level-splitting is given by:

$$\Delta E_{SO} = \pm\alpha_R k_{||} \tag{6.4}$$

where $k_{||}$ is the norm of $\mathbf{k}_{||}$. This level-splitting allows for the coherent manipulation of spin-momentum eigenstates. Pure spin states can be controlled through the application of an external magnetic field, however, the Rashba effect enables control of momentum-coupled spins by means of an applied electric field – a potentially easier task.

Furthermore, due to the σ_x and σ_y terms which appear in the Rashba Hamiltonian, the spin-split momentum states in the Rashba regime are in-plane polarized. This is different than Zeeman spin-band splitting, where spins are z-polarized, and will cause differences in the magnetotransport of electrons.

6.3 I-Si(111) sample preparation

All of the steps in the preparation of the I-Si(111) sample were carried out in either an N_2 ambient glovebox and transfer chamber or in UHV, and transported between environments in a hermetically sealed transfer chamber (see Fig. 6.1(a)). The I-Si(111) sample was from the same batch of samples used for the H-Si(111) experiments (Chs. 3 and 4), so I can pick up here where I left off in § 3.5.4. In § 3.5.5 I described how the Si(111) sample was immersed in a deoxygenated solution of dilute 10:1 HF for 2 minutes to strip off the sacrificial oxide. After a 1 minute rinse in deoxygenated DIW, the Si(111) piece was then immersed in deoxygenated, ultra-high purity ammonium fluoride (40% NH_4F by w.t., less than 10 ppb trace ions), undisturbed by agitation or stirring for 15 minutes. This final wet treatment in aqueous NH_4F atomically flattens and hydrogen-passivates the Si(111) surface [41–44]. Hydrogen termination is necessary prior to iodine exposure so that the dangling bonds are passivated and the surface remains in the (1x1) reconstructed regime.

After hydrogen passivation, the Si(111) sample was mounted to the sample holder (see Fig. 6.1(b)) and loaded into the transfer chamber through the front port. The transfer chamber was then removed from the glovebox, transported down the hall, and mounted to

the UHV system via the rear port. The rear gate valve was opened to establish an over-pressure of N_2 in the transfer chamber, which allowed the front port to be opened without introducing atmosphere so that the sample could be manually loaded. After the loading chamber was pumped to about 10^{-8} Torr, the sample was loaded into the UHV chamber where iodine exposure and *in situ* XPS and STM were performed. The base pressure in the exposure chamber was approximately $4x10^{-11}$ Torr, and the iodine source was a solid-source electrochemical source, as mentioned [205].

After the UHV chamber was pumped to base pressure, a backside sample heater was turned on and the sample was allowed to equilibrate to roughly 450 °C. The iodine source was then turned on and the sample was exposed for about 3 hours where thermally-assisted hydrogen-iodine exchange occurred in the one-to-one swapping regime. After initial exposure, the sample was rotated into the XPS position where spectra could be collected. This process was repeated until sufficient iodine signal from XPS was achieved, indicating sufficient coverage. The sample was then moved to the STM chamber where surface topography characterizations were made.

Once the sample was sufficiently iodine terminated, it was removed from the UHV chamber in the reverse process of loading, and transported back to the glovebox for final bonding to a four-terminal SOI chip. From here, I followed the bonding procedure and device wiring described in § 3.5.5.

Of the five Si samples that I exchanged with the Butera group, two of those samples were successfully bonded to my SOI architecture and I performed transport measurements on one of them (discussed in § 6.5). The first Si sample, after being wet-chemically prepared, was mounted to a standard molybdenum sample holder that the Butera group uses for their Si(100) samples. However, this holder requires the fastening of four small screws that secure the Si sample. This is a difficult task due to the loss of dexterity while working in the glovebox, but I also found that this process can introduce particulate contamination onto the Si surface (as revealed through SEM), which prevents bonding. The longer the Si

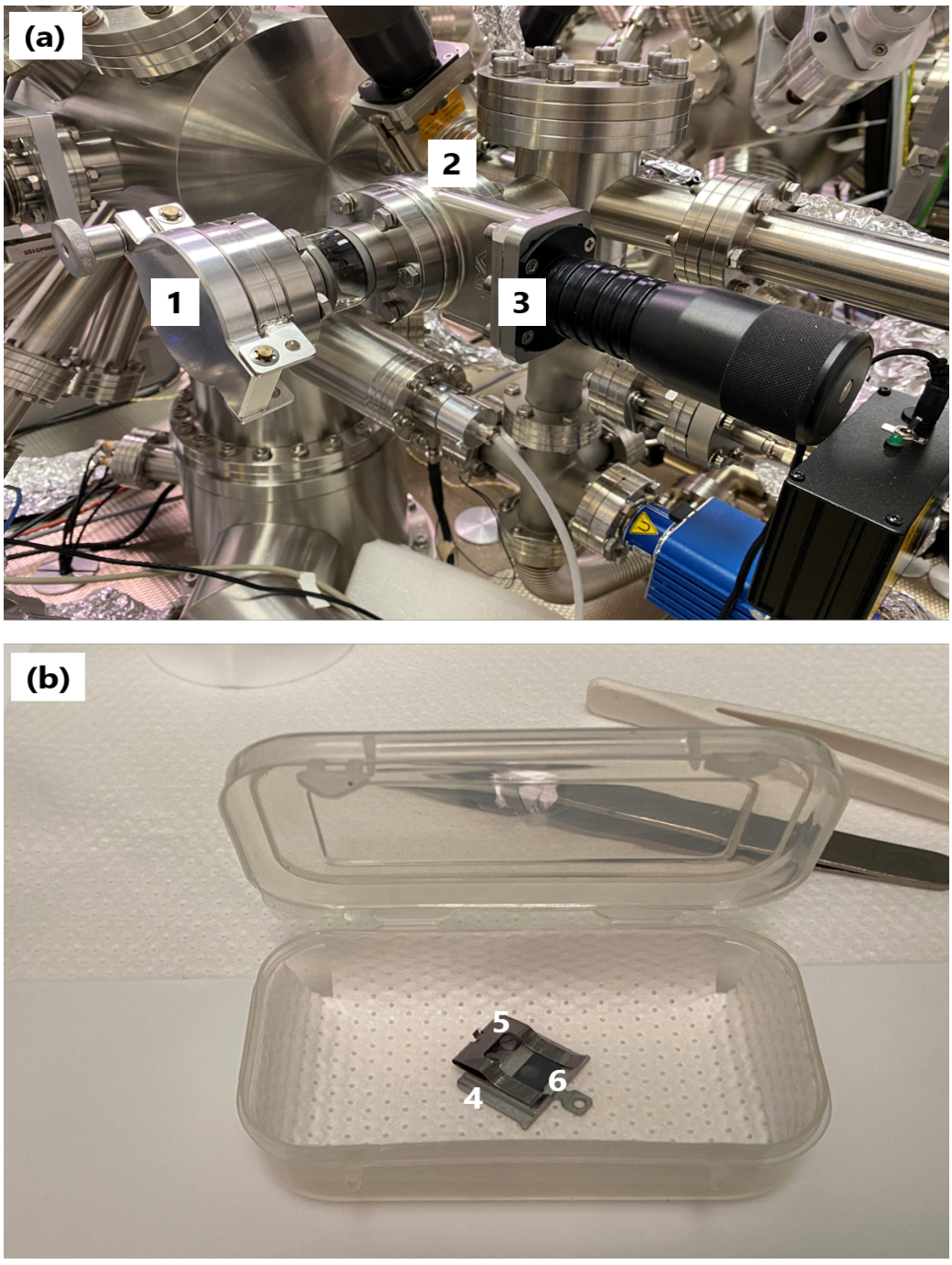

Figure 6.1: Images of (a) the transfer chamber attached to the UHV system and (b) the Si sample holder. (1) front port, (2) rear port, (3) rear gate valve, (4) molybdenum sample holder, (5) tantalum spring-clip, (6) secure Si sample.

surface is exposed to tools or screws directly above the surface, the more likely the surface will become contaminated in this way. To circumvent this, I designed a new Si sample holder made of molybdenum with a two-prong tantalum spring-clip to secure the Si sample (see Fig. 6.1(b)). With this design, Si samples can be quickly and securely mounted to the sample holder without the need for moving multiple parts directly above the surface nor long mounting times. Upon SEM inspection of a test sample mounted to this new sample holder, I found no obvious macroscopic particles on the surface. The next four Si samples exchanged with the Butera group used the new holder.

6.4 Surface analysis

In the following two sections, I discuss surface characterization measurements that were obtained from XPS and STM analysis. This demonstrated partial to full iodine coverage of the Si(111) surface. These measurements were performed at room temperature, under UHV conditions.

6.4.1 X-ray photoelectron spectroscopy (XPS)

As the name suggests, X-ray photoelectron spectroscopy (XPS) is an analysis technique where incident X-rays of known energy excite and eject electrons from atomic or molecular orbitals. The ejected electrons have energy that is characteristic of the material and can give a qualitative estimate of the surface coverage of iodine on the sample. Plotted in black in Fig. 6.2 is the XPS analysis of a pre-exposure H-Si(111) surface which was initially loaded into the UHV chamber after wet chemical preparation. Juxtaposed in red in the same plot is the XPS data collected after several iodine exposures, as described in § 6.3. It is clear that, after sufficient exposure, there are sharp iodine peaks from several of the characteristic iodine orbitals, including the 3s, 3p, 3d, and 4p orbitals (see Fig. 6.2).

From XPS measurements on several samples, we built up a data base of curves that

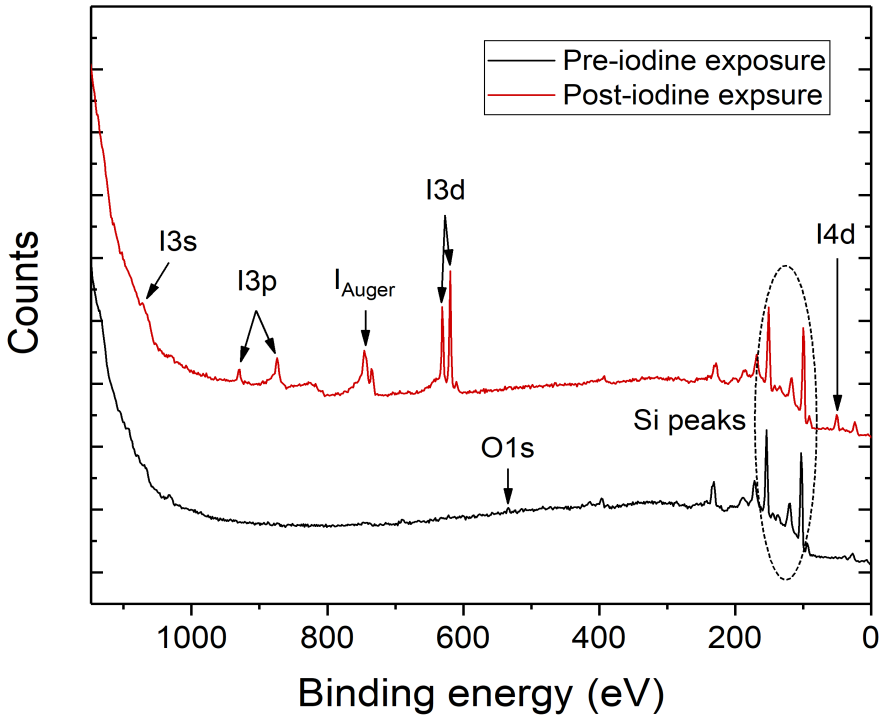

Figure 6.2: XPS analysis of the H-Si(111) surface (black) and the I-Si(111) surface (red), before and after iodine exposure in UHV. Sharp iodine peaks from several characteristic iodine orbitals can clearly be seen in the red curve, thus demonstrating qualitatively that there was iodination of the surface. Furthermore, there were no significant O or C peaks, indicating no obvious physisorbed contamination. The red curve is offset by 10,000 counts relative to the black curve for clarity.

can be compared with one another to give a good idea as to the degree of iodine coverage. The relative peak heights indicate more or less coverage. In the case of the sample whose XPS data is plotted in Fig. 6.2, the iodine peaks correspond to a greater than 50% coverage of the I-Si(111) surface. Also labeled are the iodine Auger peaks I_{MNN} which are two-electron events in which an incident X-ray ejects a primary electron, and in turn that electron is recaptured and ejects a secondary electron. Furthermore, it is clear from the data that contamination, albeit present, is quite low. In particular, the oxygen 1s peak in the unexposed curve disappears upon heating and exposure. Also, there appears to be a lack of other typical contaminants, such as carbon.

6.4.2 Scanning-tunneling microscopy (STM)

For a more quantitative analysis of the surface coverage, we used scanning-tunneling microscopy (STM). STM allows us to see with atomic resolution what the topography and morphology of the surface is like. Not only can we see where the iodine is (see orange dots in Fig. 6.3), but we get an idea of the iodine distribution and the surface reconstruction (if any). Figure 6.3 reveals that we did indeed have greater than 50% coverage of the I-Si(111) surface, but the distribution seemed to be fairly random, and not characteristic of a (1x1) or ($\sqrt{7}$x$\sqrt{7}$) reconstructed surface. This means that we were most likely in the partially iodine-terminated and partially reconstructed regime. The XPS analysis did not reveal the presence of any significant levels of O or C, suggesting that the bright conglomerates were most likely iodine clusters or Si adatoms terminated with iodine. At the temperature the sample was heated to, it is possible that most or all of the hydrogen may have been removed allowing the surface to reconstruct before exposure to iodine. In Fig. 6.3(b), the atomic steps characteristic of the Si(111) surface can be seen, indicating an atomically flat sample despite possible regions of Si adatom clusters due to partial reconstruction.

Because this experiment is in its early stages, we are still in the process of understanding the optimal time-temperature product for the iodine exposure. When the sample is

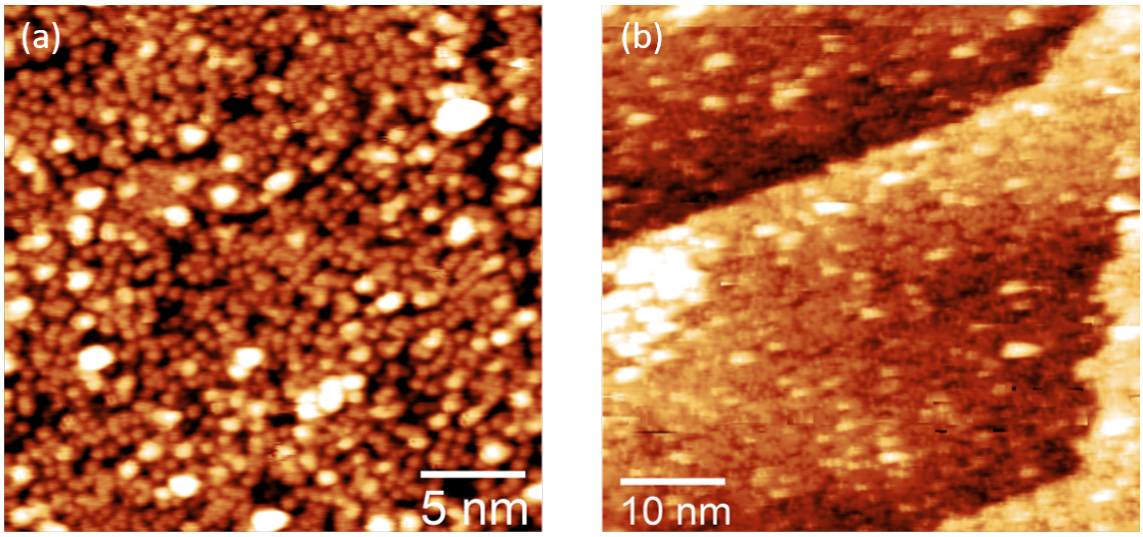

Figure 6.3: STM images of the I-Si(111) surface after final iodine exposure. The labels indicate the voltage and current values of the STM tip for filled-state mode. The orange dots are the iodine atoms, while the bright conglomerates are likely water or some other physisorbed contamination, or possibly large clusters of iodine attached to structural defects in on the Si surface. Much greater than 50% iodine cover is seen in (a) and (b), as well as the atomic steps in (b) typically seen on Si(111). This indicates atomic flatness depsite possible physisorbed contamination.

heated, the hydrogen will begin to be desorbed, allowing for direct iodine replacement or thermally-assisted exchange. However, at temperatures much beyond 450 °C the surface will begin to reconstruct in clusters as it loses larger amounts of hydrogen that prevented reconstruction. In the extreme limit that all of the hydrogen is removed at higher temperatures, the surface will fully reconstruct to the ($\sqrt{7}$x$\sqrt{7}$) configuration and the iodine will passivate the resultant adatoms. Idealy, we would like full iodine coverage of the I-Si(111) surface in the (1x1) regime, however, this requires lower temperatures and much longer exposure times to achieve.

6.5 2DES transport on I-Si(111)

Transport measurements were carried out on the first of the two successfully bonded SOI-I-Si(111) samples. The second bonded sample did not pass the routine operation tests;

the PDGs showed significant leakage to the 2DES. The sample discussed in this section was thermally cycled four different times, with baseline measurements being performed each cycle. The first three cycles were carried out using the home-made dipstick (discussed in Ch. 4) at 77 K, and the fourth and final cycle was carried out at about 80 K in a He^3 Heliox system equipped with a superconducting magnet with field capabilities up to 13 T. Hall measurements were made during this final cycle, and at modest fields up to about 2 T. While the sample remained bonded throughout the duration of the process, the I-V characteristics varied with each cooldown, including significant variations in the threshold voltage and PDG leakage (see Fig 6.4). This threshold voltage swing, as well as the varying PDG leakage, could be indicative of the SOI-Si bond being microscopically altered during thermal cycling, resulting in a variation of the SOI to Si surface separation. Additionally, significant hysteresis was observed in the source-drain current as the global gate was swept, which is unlike what I saw with the H-Si(111) samples.

This hysteresis could be the result of a number of factors. First, this could be the result of a change in the separation between the SOI and Si surface. As charge builds up on the I-Si surface the attractive electrostatic force between the two charged plates increases, which could lead to a decreased separation and then an increased separation again upon relaxation. This would suggest that the quality of the bond, while sufficient to remain bonded during thermal cycling, was not optimal. Another possibility is that charge traps on the I-Si surface were filled at high carrier densities due to the complex chemistry or roughness of the I-Si surface which subsequently remained as the global gate voltage was decreased. Finally, it has been shown that 2D hole systems form on the surface of Cl-Si due to the high electronegativity of Cl [198]. It is possible that 2D hole systems form on the I-Si surface as well. Although it would be less pronounced than the Cl-Si surface, a native 2D hole system on the I-Si would require a larger threshold voltage than the H-Si surface to first deplete the 2D holes and then invert the surface to accumulate electrons. The interactions and recombination of electrons with the 2D hole gas could not

only account for the hysteresis, but also for the large threshold voltages seen in Fig. 6.4.

I should include a disclaimer about the fourth and final measurements in the Heliox system. Due to human error, after I had mounted the bonded sample to the Heliox insert and pumped out the inner vacuum can (IVC), I realized that I had not given the sample enough vertical clearance, which resulted in the sample contacting the bottom of the IVC. Surprisingly, this did not result in the sample becoming unbonded. However, the force of the collision seemed to have pressed the sample together in such a way as to introduce significant global gate leakage for $V_G > 15$ V, as well as increased reverse-bias PDG leakage. Nevertheless, the sample was still intact and once the sample assembly was adjusted, I was able to carry out the final measurements.

Figure 6.4 shows the source-drain current as a function of the global gate voltage for each of the four thermal cycles. For each of these measurements, the PDGs were grounded and a source-drain bias of 100 mV was applied. The threshold voltage can be seen to vary between $\sim$1 V after the first cooldown to $\sim$3.5 V after the final cooldown. The hysteresis was also minimal for the final cooldown. In Fig. 6.5, we see that while the PDGs had a significant amount of leakage at large reverse-biases (especially for the fourth cooldown), there was minimal leakage in the vicinity of zero volts (ground). I also saw very little source-drain current modulation as the PDGs were swept, indicating good VdP confinement of the electrons on the surface.

For the fourth cooldown in the Heliox fridge, I wanted to measure 2D transport on the I-Si surface at elevated temperatures ($\sim$ 77 K), but in order to operate the superconducting magnet, the magnet needed to be cooled with liquid He (L-He). To do this, I did not introduce any He exchange gas into the IVC after it was evacuated, which allowed the sample to reach a base temperature of 77 K upon filling the system with liquid N_2 (L-N_2). Once the sample was cooled to 77 K, the L-N_2 was removed and the Heliox system was filled with L-He so that the magnet and IVC reached a base temperature of 4.2 K. The sample (surrounded by vacuum) remained close to 77 K once the residual exchange gas in

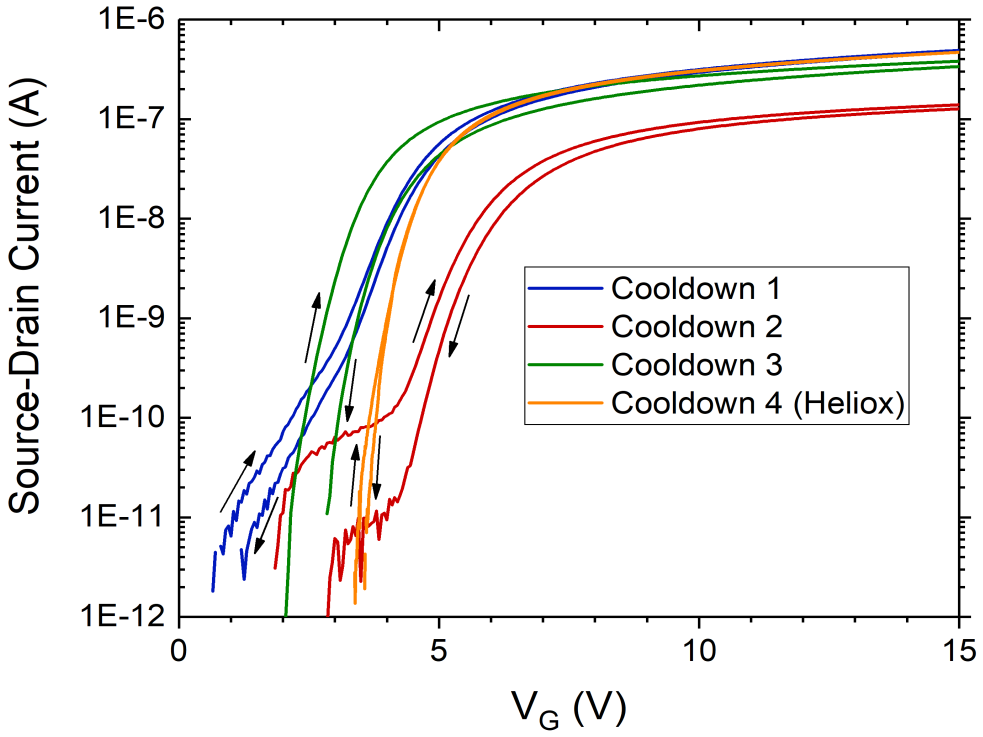

Figure 6.4: Plots of the source-drain current I_{sd} vs the global gate voltage V_G for each of the four thermal cycles. The threshold voltage shifted after each cooldown, suggesting that the bond quality was not optimal and that the bond distance may have altered. The hysteresis in the data also may indicate that there is a carrier-dependent filling of charge traps on the surface or that there is some global gate induced variation of the sample separation. Arrows indicate sweep direction.

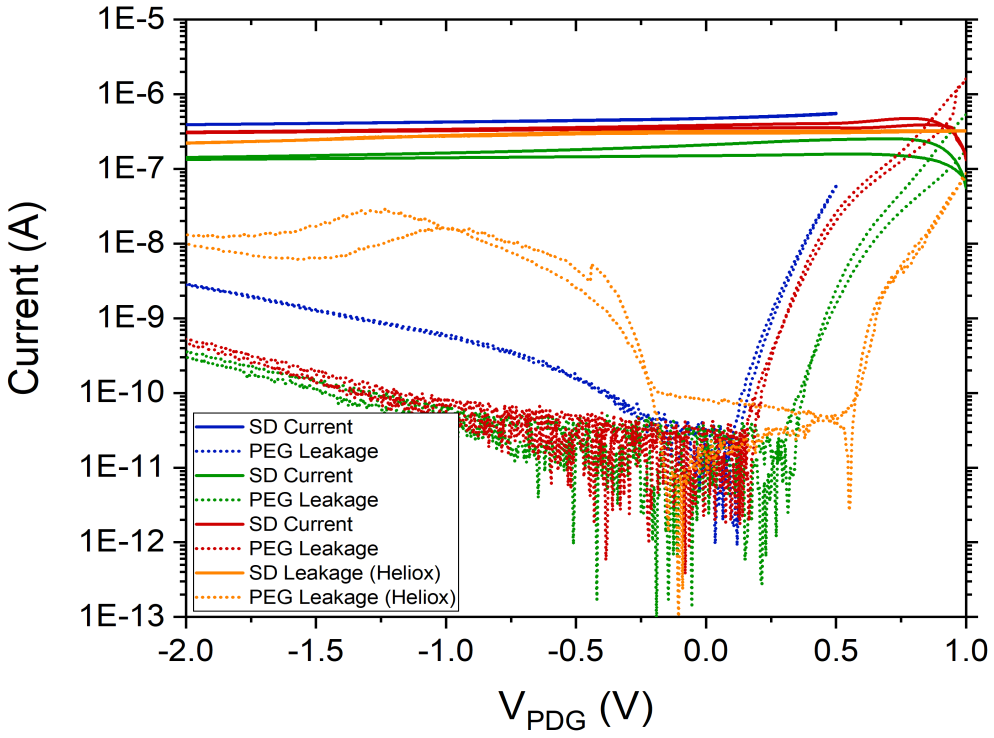

Figure 6.5: Plots of the source-drain current I_{sd} and PDG leakage I_{PDG} as a function of PDG voltage V_{PDG} for each of the four thermal cycles (see legend from Fig. 6.4). The PDG leakage is significantly higher for large reverse biases than for the H-Si(111) samples discussed in Ch. 4. However, there is minimal leakage around $V_{PDG} = 0$ V (ground). Additionally, there is minimal source-drain current modulation as the PDGs are swept, suggesting that there was good VdP confinement of the electrons on the surface.

the IVC froze out. During this process, the sample temperature rose to about 80 K where it remained during the measurement.

Upon demonstration of acceptable baseline operation, standard low frequency AC lock-in techniques were performed at 80 K (3.979 Hz, 50 nA) to measure the sheet resistance and the Hall density of the 2DES, with all PDGs tied to ground. Fig. 6.6 shows my Hall measurements for two different densities ($V_G = 10$ V and $V_G = 12$ V) at several different forward and reverse field values. The slopes of the fit lines are equal to the Hall coefficient (Eq. 2.66), where $R_H = \frac{1}{en}$, allowing me to extract the true carrier density n.

For both gate voltages, $R_{24,31}$ and $R_{13,24}$ was measured as a function of magnetic field. It is important to measure both Hall configurations, and do so for both field polarities, in order to account for any offset voltages. In this way I extracted carrier densities by taking the average of each pair of slopes in Fig. 6.6, yielding $n = 3.6\text{x}10^{10}$ cm^{-2} and $n = 5.4\text{x}10^{10}$ cm^{-2} at $V_G = 10$ V and $V_G = 12$ V, respectively. These densities are not in good agreement with the expected geometric densities, which for the H-Si(111) surface should be roughly $n = 4.3\text{x}10^{11}$ cm^{-2} and $n = 5.2\text{x}10^{11}$ cm^{-2} for these gate voltages – about an order of magnitude higher. As previously discussed, this may be due to the poor bond quality of the device, resulting in a greater than expected separation of the 2DES from the gate. This disparity may also be due to the presence of a native 2D hole system on the I-Si surface that shifts the threshold voltage higher than the H-Si surface, resulting in less than expected electron accumulation. The sheet resistance data were collected at the same global gate voltages and are listed in Table 6.1.

Table 6.1: Sheet resistance data for the I-Si(111) sample measured at two different global gate voltages. Also listed are the extracted Hall densities and the calculated carrier mobilities.

Gate Voltage	$R_{horizontal}$	$R_{vertical}$	r	R_s	n	μ
$V_G = 10$ V	10.8 kΩ	8.9 kΩ	1.21	44.4 kΩ/□	$3.6\text{x}10^{10}$ cm^{-2}	3900 cm^2/Vs
$V_G = 12$ V	8.7 kΩ	7.4 kΩ	1.18	36.4 kΩ/□	$5.4\text{x}10^{10}$ cm^{-2}	3200 cm^2/Vs

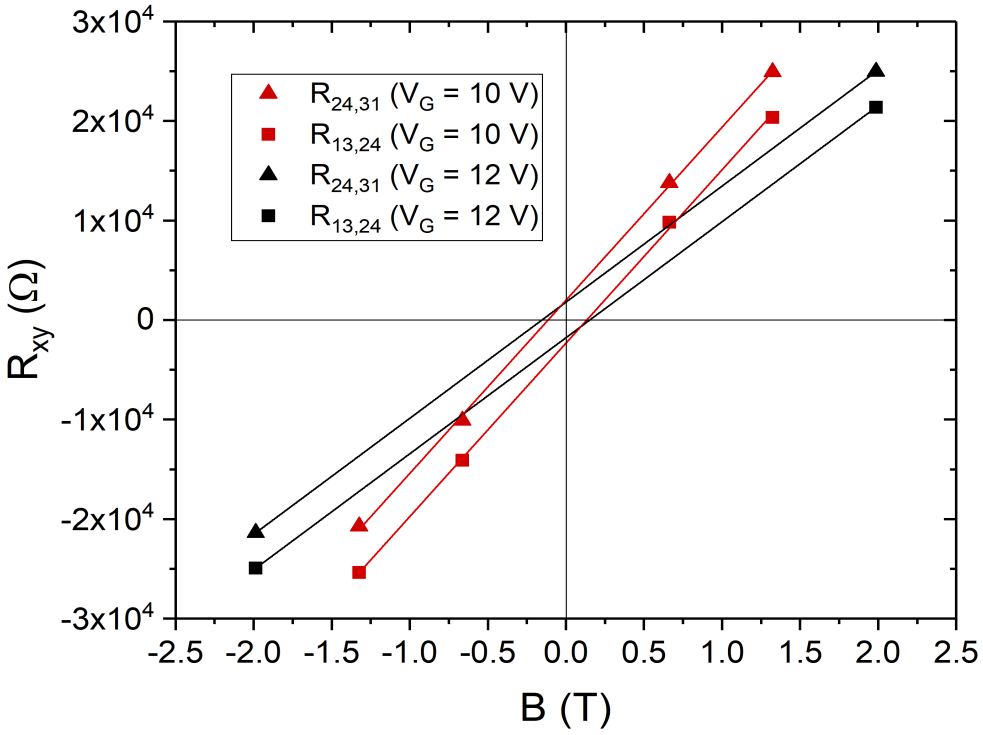

Figure 6.6: Plots of the Hall resistance R_{xy} at various magnetic field values B for two different carrier densities. Both Hall configurations, $R_{24,31}$ and $R_{13,24}$, were measured for each global gate voltage, and the carrier density was extracted by taking the average of each pair of slopes. The extracted carrier densities were $n = 3.6\text{x}10^{10}$ cm^{-2} and $n = 5.4\text{x}10^{10}$ cm^{-2} for $V_G = 10$ V and $V_G = 12$ V, respectively – about an order of magnitude lower than the expected geometric densities.

The sheet resistance values were obtained using Eq. 2.62, and were about an order of magnitude higher than the H-Si(111) samples. Again, this may be due to the poor quality bond or the presence of a native 2D hole system on the surface. Nevertheless, from the Hall and sheet resistance measurements, I was able to extract a carrier-dependent mobility (Eq. 2.67). The mobility turned out to be fairly close to the carrier mobility I found in the H-Si(111) samples (see § 4.2). This suggests that the quality of the surface had not been significantly degraded during iodination.

Every step of the process, especially the sample mounting and demounting steps (where the Si sample is at greatest risk for collecting dirt) must be carefully considered, with the primary focus being the minimization of events that might introduce contamination. A 50% bonding success rate (with the new holder), is actually a good start for a first experiment. Further refinement of the process, and perhaps an improved sample holder design, would help to increase the bond success rate which would increase throughput for additional transport measurements. Additionally, the Butera group is currently developing a toluene-based iodine wet chemistry, as well as a possible benzene- or mesitylene-based solution. A wet chemical approach may allow us to bypass the exchange process entirely and iodine terminate the Si surface *in situ* in the glovebox immediately after hydrogen termination in NH_4F.

On a final note, it would be interesting to explore the possible existence of this native 2D hole system on the I-Si surface that I suggested earlier. Probing of this system could be achieved in my devices by replacing the arsenic-doped ohmic contacts with column III acceptor-doped contacts. Through the application of a reverse bias on the global gate and a forward bias on the PDGs, 2D holes can be accumulated and confined to the I-Si surface in a VdP configuration and 2D hole transport can be measured. Understanding the electrostatic and electrochemical properties of the I-Si surface will be critical going forward with this experiment.

Chapter 7: Conclusions and future directions

7.1 Summary

In conclusion, I have described a demonstration of a new and effective method for the non-invasive electrostatic gating of pristine, chemically-terminated, intrinsic Si surfaces using a SOI-based device design. This novel architecture ensures that the pristine Si surface under study can be kept free of dopants and metals that would degrade the surface quality and be deleterious to transport measurements. Using this non-invasive gating method, I measured 2D transport on pristine, intrinsic H-Si(111) surfaces, and for the first time measured 2D electron transport on a pristine, intrinsic I-Si(111) surface. To date, no other 2D magnetotransport measurements have been realized on I-Si(111) surfaces, due in large part to the difficulties of implementing the electrostatic gating of these fragile surfaces. Having demonstrated that we can indeed non-invasively gate a pristine I-Si(111) surface, there is no reason, in principle, that my device architecture could not be used to gate a variety of other chemically prepared Si surfaces, and indeed chemically prepared Si surfaces of other crystal orientations. My novel device architecture offers a new path forward for the investigation of pristine Si surfaces that have previously been inaccessible to experiment.

Our device architecture stands out in two important ways. First, all of the electrostatic gates *as well as* the ohmic contacts reside on a single SOI chip, which suffers all of the harsh device processing. Second, because all electrical components are housed in the SOI chip, the pristine, intrinsic Si chip can remain free of dopants or metals. This allows for

a broad compatibility with existing wet chemical treatments and dry UHV preparation. This process compatibility of the pristine Si piece allows for the inclusion of other surface preparations that would not have been possible with doped Si. For example, the Si(111) surface is readily hydrogen-passivated and becomes atomically flat when prepared in ammonium fluoride solution, as I discussed in Ch. 3. However, the Si(100) surface is not well-suited for wet chemical preparation in NH_4F and becomes atomically and macroscopically rough after immersion [221, 222]. Thus, in order to study H-Si(100) samples or Si(100) samples with other surface terminations, it helps if they are compatible with dry UHV processing. My device architecture allows for this and it is this versatility of the Si piece that truly opens the door for a wide range of surface preparations to be studied.

This novel architecture is not without challenges, of course, and much work still remains to overcome these issues. In particular, the series contact resistance that arises at the SOI-Si bond edge is the primary challenge for our devices that still needs to be addressed. I spent a sizeable portion of this dissertation (Ch. 5) describing the physics of the current injection across the Van der Waals bond in my devices, and how one might go about decreasing the contact resistance. The current injection across a Van der Waals bond is an unavoidable and inherent feature in our architecture due to the placement of the ohmic contacts on the SOI piece. Further refinement of the device fabrication process should lead to an improved SOI-Si bond quality. Implementation of additional electrostatic gates (PEGs) will allow for independent tuning of the electrostatics at each SOI-Si bond edge. These and other efforts, while formidable, can in principle be achieved and will enable significantly better device performance at low temperatures.

7.2 Experimental proposals

Ultimately, reduced contact resistance at low temperatures are needed to allow low temperature quantum transport measurements in my devices. However, $R_{contact}$ notwithstanding, there are several interesting experiments that could be performed with our present

devices. In the following sections I propose several experiments in which our devices could be used in interesting ways, even at elevated temperatures.

7.2.1 Beyond Si(111): Si(100), Si(114), and more

In this dissertation, I focused on the Si(111) surface, in part due to the high-quality hydrogen-passivation that is achievable through wet chemical processing. However, there are many other surface orientations that could be engineered for transport measurements using our SOI gating architecture. In contrast to the six-fold valley degenerate Si(111) surface, the Si(100) and Si(110) surfaces have a two-fold and four-fold valley degeneracy in the ground sub-band, respectively. This means that 2D, 1D, and 0D micro- and nano-structures fabricated on the Si(100) surface, for example, have a two-fold valley degeneracy which could be exploited for quantum information processing.

Consider a quantum dot induced on a pristine Si(100) surface terminated with a heavy halogen like iodine. Electrons in this quantum dot would have a 2-fold valley degeneracy that could be lifted through spin-orbit coupling via an applied electric field (see the discussion of the Rashba effect in § 6.2). In effect, this system acts like a two-level system with an electric field-tunable splitting that could serve as a type of spin-valley qubit, similar to the proposal by Bourdet et al. [223].

As I noted, the Si(100) surface is not well-suited for wet chemical preparation in NH_4F because it becomes atomically and macroscopically rough after immersion [221, 222]. The same is true for the Si(110) surface, and potentially other interesting orientations that one may wish to investigate. Therefore these surfaces must be prepared and chemically-passivated using other techniques.

Vicinal Si(100) and Si(111) surfaces have a range of properties and morphologies that can be manipulated through various chemical adsorptions [224]. The Si(114) orientation is particularly interesting, and has been studied both theoretically and experimentally [225–227]. The ideal Si(100) surface is characterized by parallel dimer rows that rotate 90° from

terrace to terrace. The Si(114) surface, by contrast, consists of alternating, single-domain monomer, dimer, and tetramer rows from terrace to terrace, each with different selectivities to chemical termination. For example, the monomer and dimer rows are susceptable to chlorination, leaving the tetramer rows free for selective functionalization [225]. 2D electron or hole transport measurements on precisely functionalized Si(114) surfaces would be interesting.

7.2.2 Induced quantum dot probe

A recent experimental proposal by Shim et al. has called for the use of a specially configured STM tip to probe pristine materials by inducing a quantum dot on the surface or in the 2D quantum well [228]. Through the induction of a quantum dot, one can scan multiple regions of the surface and deduce basic properties of the material to determine if it would then be suitable for constructing a full device. This is an attractive proposal because many of the pristine materials that are experimentally interesting are fabricated in small batches under UHV conditions, using for example MBE. These materials are therefore in short supply. It is never desirable to waste hard to produce material, and this would allow relatively quick tests for quality before fabricating devices.

To this end, our device architecture could be modified in such a way as to create a non-invasive probe chip with a STM-like tip fabricated on the surface of the SOI piece in much the same way as the PDGs were fabricated in our devices. Figure 7.1 shows the basic idea. The probe chip would be Van der Waals bonded to the pristine material under test, enabling the induction of a quantum dot over the region of interest. Once the QD characterization measurements were made, the probe chip could be de-bonded from the pristine material leaving it ready for incorporation into a device.

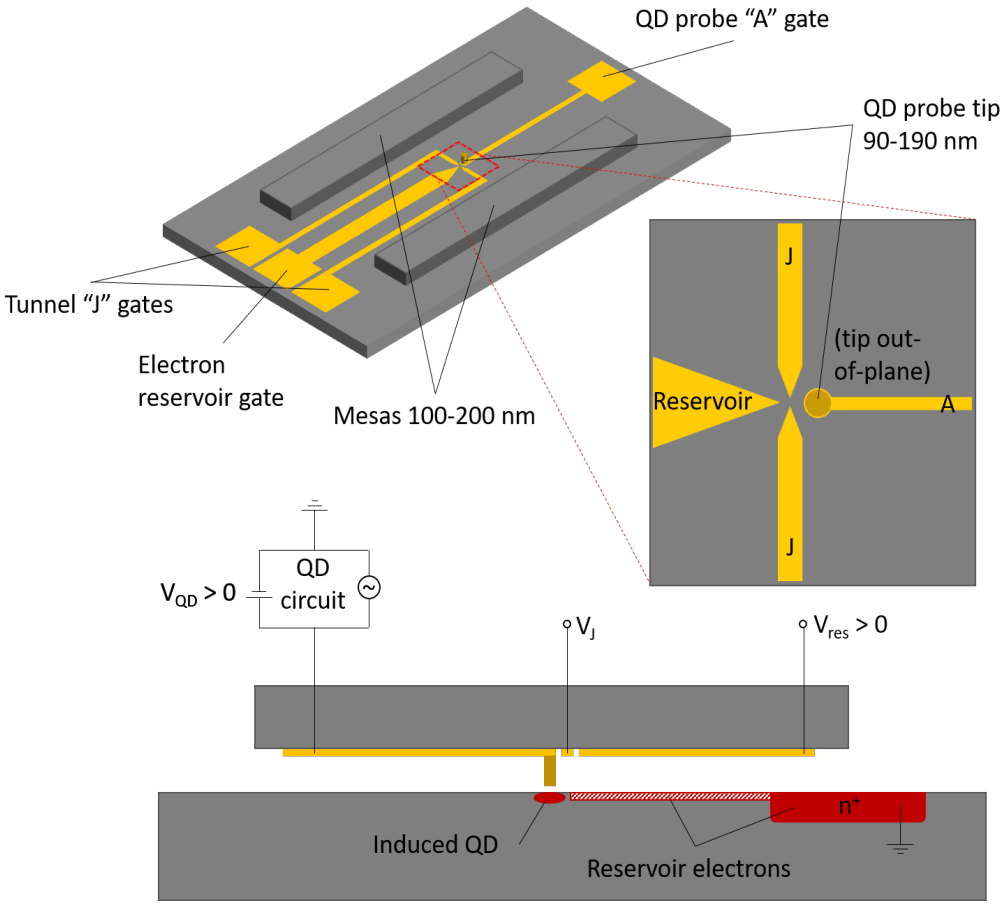

Figure 7.1: Schematic of QD probe chip as a modification of an SOI device. The mesas on the probe chip would Van der Waals bond to the pristine material under study. Metalization to create the gates and the probe tip would be similar to the PDGs in our devices. The n^+ electron reservoir supplies electrons to the QD via the electron accumulation channel (textured red), which is induced by the reservior gate. The A gate induces the QD, and the J gates load/unload electrons onto/off the QD.

7.2.3 Silicene air-bridge FET

Silicene is the 2D allotrope of Si and is analogous to graphene for carbon [165, 229]. Rather than having a planar structure like graphene, however, silicene has a buckled geometry, which leads to its instability in air from oxidation and hydration [230]. Planar silicene, formed by inclusion of Be bridges has also been theoretically investigated [231]. Silicene terminated with iodine, however, has excellent immunity to oxidation and it has been predicted that enhanced spin-orbit interactions and topological behavior can arise in such a system [232]. More recently, sheets of silicene have been isolated using a lamination transfer technique to produce a 2D room temperature operating silicene-based transistor [172].

Using established lamination transfer techniques, I propose a silicene FET structure using our non-invasive SOI gating architecture in which silicene could be de-laminated onto the SOI chip (much like the Si chip is bonded to the SOI chip in our devices). Consider Fig. 7.2. Upon delamination, the silicene film would be suspended in an air-bridge configuration that could be electrically accessed via the ohmic contacts and electrostatically gated using the PDGs and global gate. Furthermore, this silicene sheet could be iodinized through subsequent processing to protect against oxidation and enhance the spin-orbit interactions of electrons confined to this 2D system.

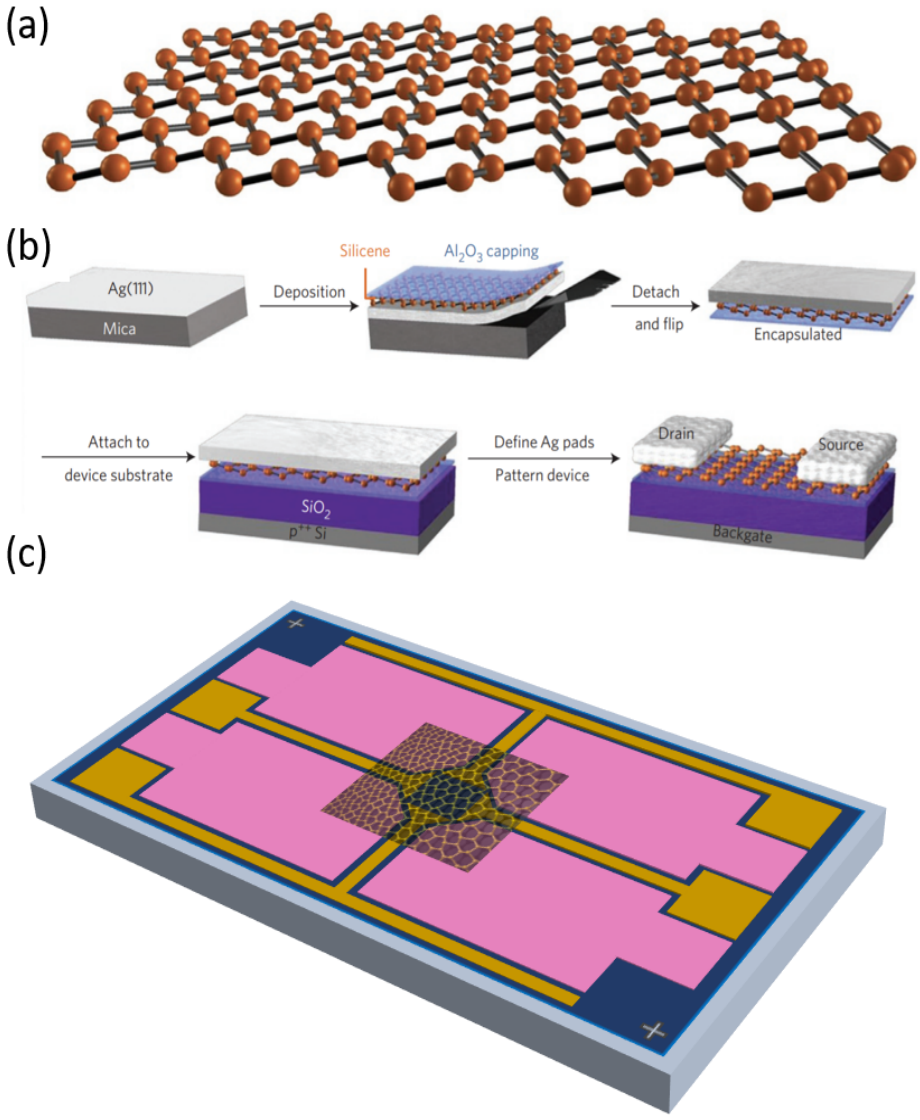

Figure 7.2: Illustration of a silicene air-bridge FET. (a) A single sheet of silicene, (b) lamination transfer sequence of silicene from mica-silver substrate to final Si-SiO_2 substrate, and (c) silicene sheet delaminated onto our SOI chip to form an air-bridge FET. (a) and (b) taken from [172].

Appendix A: Device fabrication recipes

This appendix describes in detail each step of the fabrication process for the devices I discussed in this work. A full reproduction of the devices should be achievable through implementation of these recipes. As with most fabrication processes, this was an evolving one. Furthermore, it should be noted that some of the device processing was carried out at the National Institute for Standards and Technology's Center for Nanoscale Science and Technology (NIST CNST), while others were carried out at the Laboratory for Physical Sciences (LPS) cleanroom facility.

Procedure for SOI 4T Device Wafer (at NIST)

Updated: 05/04/21 by Luke

Summary: Full process for the SOI 4T device wafer to be bonded with Si(111) or Si(100). Process consists of 8 primary steps:

1. SOI thinning using dry oxidation and 6:1 BOE etching (final top-Si thickness: 200Å; sacrificial oxide thickness: 100Å).
2. Ion implantation (Arsenic, $4x10^{14}$ cm^{-2} [$2x10^{20}$ cm^{-3}], 6 keV, 7° tilt).
3. N_2 furnace anneal to activate implants (1000°C, 30min).
4. Photolithography step 1: define ohmic contacts.
5. Furnace anneal/oxidation to repair top-Si from RIE damage (optional).
6. Photolithography step 2: define mesas (optional)
7. Photolithography step 3: depletion gate metallization (lift-off).
8. Dice SOI wafer into 10 x 5.6 mm^2 samples.

Nominal SOI wafer specifications:

Top Si orientation: (100)
Top Si thickness: 880 Å
BOX thickness: 1900 Å
Epi-layer (N=$2x10^{19}$ cm^{-3}) thickness: 3.5 µm
SOI wafer total thickness: 775 µm
Final die dimensions: 10 x 5.6 mm^2

Note: Oxidation times and thicknesses calculated using the Massoud model, not Deal-Grove.

1. SOI thinning using dry oxidation and 6:1 BOE etching

I. Measure initial SOI thicknesses using J. A. Woollam ellipsometer
- ☐ Collect data using recipe: 4in_13pt
- ☐ Analyze data using recipe: SOI-model

II. Full RCA clean using B102 Furnace RCA Clean bench
- ☐ Pre-soak in DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ SC1: 5:1:1 DIW:NH_4OH:H_2O_2, 80°C, 10 min
- ☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ HF dip: 50:1 DIW:HF, 21°C, 15 sec
- ☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ SC2: 5:1:1 DIW:HCl:H_2O_2, 80°C, 10 min
- ☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ Spin dry in SRD

III. Grow initial oxide in Sandvic high-purity dry-oxidation tube furnace

□ Recipe: 1000°C, 3 hrs, 15 min
□ Oxide thickness: 1150 Å
□ Top-Si thickness: 285 Å (585 Å Si consumed)

IV. Measure post-oxidation SOI thicknesses using J. A. Woollam ellipsometer
□ Collect data using recipe: 4in_13pt
□ Analyze data using recipe: SOI-model

V. Remove initial oxide in 6:1 BOE
□ Submerge SOI wafer in 6:1 BOE for 90 sec (etch rate @ 21°C: 860-930 Å/min)
□ DIW dump-rinse, 3 cycles

VI. Measure post-etch SOI thicknesses using J. A. Woollam ellipsometer
□ Collect data using recipe: 4in_13pt
□ Analyze data using recipe: SOI-model

VII. Full RCA clean using B102 Furnace RCA Clean bench
□ Pre-soak in DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
□ SC1: 5:1:1 DIW:NH_4OH:H_2O_2, 80°C, 10 min
□ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
□ HF dip: 50:1 DIW:HF, 21°C, 15 sec
□ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
□ SC2: 5:1:1 DIW:HCl:H_2O_2, 80°C, 10 min
□ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
□ Spin dry in SRD

VIII. Grow final sacrificial oxide in Sandvic high-purity dry-oxidation tube furnace
□ Recipe: 850°C, 40 min
□ Oxide thickness: 95 Å
□ Top-Si thickness: 200 Å (85 Å Si consumed)

IX. Measure post-oxidation SOI thicknesses using J. A. Woollam ellipsometer
□ Collect data using recipe: 4in_13pt
□ Analyze data using recipe: SOI-model

2. Ion implantation of SOI wafer

I. Clean substrate
□ Piranha clean SOI wafer using high-purity SSEC single wafer cleaning system
□ Repeat Piranha clean if necessary

II. Send out cleaned, bare SOI wafer for ion implantation (INNOViON):
□ Species: Arsenic, Dose: $4x10^{14}$ cm^{-2}, Energy: 6 keV, Tilt: 7°

3. N_2 furnace anneal to activate implants

I. Clean Substrate
☐ Piranha clean SOI wafer using high-purity SSEC single wafer cleaning system
☐ Repeat Piranha clean if necessary
II. Activate implants in Sandvik high-purity anneal tube furnace (N_2 ambient)
☐ Recipe: 1000°C, 30 min

4. Photolithography step 1: define ohmic contacts

I. Clean substrate
☐ Piranha clean SOI wafer using high-purity SSEC single wafer cleaning system
☐ Repeat Piranha clean if necessary

II. Photolithography
☐ Prime SOI wafer with HMDS in HMDS vapor primer
☐ Spin on positive-tone S1813 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec (optional)
- Spin: 5000 rpm, 1000 rpm/s, 60 sec (~1.2 μm thick)

☐ Softbake, 115 °C, 60 sec
☐ Expose in Suss MA6/MA8 aligner
- 150 mJ/cm^2, g-line filter, vacuum contact, 'SOI 4T Ohmic Contacts' mask

☐ Develop with Microposit MF-319, 60 sec, use gentle agitation
☐ DIW rinse thoroughly, 60 sec
☐ N_2 blow dry
☐ Hard bake, 90 °C, 10 min (optional)

III. Define ohmic contacts using RIE
☐ Pre-clean RIE1 chamber, recipe: _CNST_ChamberCLEAN_Light
☐ Etch recipe: LR-SOI-OC-O2/SF6
- O_2 Descum: 20 sccm O_2, 150 W, 200 mTorr, 30 sec
- Si etch: 10 sccm SF_6, 5 sccm O_2, 75 W, 10 mTorr, 3 min
- O_2 Ash: 30 sccm O_2, 150 W, 40 mTorr, 60 sec

☐ Clean RIE chamber, recipe: _CNST_ChamberCLEAN_Light

5. Furnace anneal/oxidation to repair top-Si from RIE damage (optional)

I. Remove old photoresist with Acetone/IPA/DIW clean:
☐ Set hot plate to 120°C
☐ Submerge SOI wafer in hot Acetone for 15-30 min
☐ Sonicate SOI wafer in Acetone for 5 min (optional)
☐ Submerge SOI wafer in hot IPA for 5-10 min

☐ DIW dump-rinse, 3 cycles

II. Remove residual photoresist with Piranha clean:
☐ Solution ratio: 4:1 H_2SO_4:H_20_2
☐ Set hot plate to 120°C
☐ Prepare H_2SO_4 in primary beaker
☐ Prepare H_20_2 in secondary beaker
☐ *Slowly* pour H_20_2 into primary beaker of H_2SO_4
☐ Submerge SOI wafer in Piranha solution for 15-30 min
☐ DIW dump-rinse, 3 cycles
☐ Spin dry in SRD

III. Modified RCA clean using B102 Furnace RCA Clean bench (no HF dip)
☐ Pre-soak in DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
☐ SC1: 5:1:1 DIW:NH_4OH:H_2O_2, 80°C, 10 min
☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
☐ SC2: 5:1:1 DIW:HCl:H_2O_2, 80°C, 10 min
☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
☐ Spin dry in SRD

IV. Anneal/oxidize SOI wafer in Sandvik high-purity dry-oxidation tube furnace
☐ Recipe 1: 800°C, 10 min, dry O_2 ambient
☐ Recipe 2: 1000°C, 30 min, N_2 ambient
800°C, 10 min, dry O_2 ambient

6. Photolithography step 2: define mesas (optional)

I. Clean substrate
☐ Piranha clean SOI wafer using high-purity SSEC single wafer cleaning system
☐ Repeat Piranha clean if necessary

II. Photolithography
☐ Prime SOI wafer with HMDS in HMDS vapor primer
☐ Spin on positive-tone SPR220-3.0 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec (optional)
- Spin: 3000 rpm, 1000 rpm/s, 60 sec (~2.5 µm thick)

☐ Softbake, 115 °C, 90 sec
☐ Expose in Suss MA6/MA8 aligner
- 280 mJ/cm^2, i-line filter, hard contact, “SOI Mesa” mask

☐ Post exposure bake, 115 °C, 90 sec
☐ Develop with Microposit MF CD-26, 60 sec, use gentle agitation
☐ DIW rinse thoroughly, 60 sec
☐ N_2 blow dry
☐ Hard bake, 90 °C, 10 min

III. Remove remainder of BOX using 6:1 BOE

□ Submerge SOI wafer in 6:1 BOE for 2 min (etch rate @ 21°C: 860-930 Å/min)

□ DIW dump-rinse, 3 cycles

IV. Define mesas using RIE

□ Pre-clean RIE1 chamber, recipe: _CNST_ChamberCLEAN_Light

□ Etch recipe: LR-SOI-Mesa-O2/SF6

- O_2 Descum: 20 sccm O_2, 150 W, 200 mTorr, 30 sec
- Si etch: 20 sccm SF_6, 75 W, 10 mTorr, 10 min
- O_2 Ash: 20 sccm O_2, 150 W, 40 mTorr, 30 sec

□ Clean RIE chamber, recipe: _CNST_ChamberCLEAN_Heavy

7. Photolithography step 3: proximity depletion gate metallization (lift-off)

I. Remove old photoresist with Acetone/IPA/DIW clean:

□ Set hot plate to 120°C

□ Submerge SOI wafer in hot Acetone for 15-30 min

□ Sonicate SOI wafer in Acetone for 5 min (optional)

□ Submerge SOI wafer in hot IPA for 5-10 min

□ DIW dump-rinse, 3 cycles

II. Remove residual photoresist with Piranha clean:

□ Solution ratio: 4:1 H_2SO_4:H_20_2

□ Set hot plate to 120°C

□ Prepare H_2SO_4 in primary beaker

□ Prepare H_20_2 in secondary beaker

□ *Slowly* pour H_20_2 into primary beaker of H_2SO_4

□ Submerge SOI wafer in Piranha solution for 15-30 min

□ DIW dump-rinse, 3 cycles

□ Spin dry in SRD

III. Clean substrate (if necessary)

□ Piranha clean SOI wafer using high-purity SSEC single wafer cleaning system

IV. Photolithography (lift-off)

□ Dehydrate SOI wafer on contact hotplate, 200°C, 5 min

□ Allow wafer to cool to RT

□ Prime SOI wafer with HMDS in HMDS vapor primer (optional)

□ Spin on PMGI SF6 2S lift-off resist

- Spin: 2500 rpm, 5000 rpm/s, 45 sec (~35 nm thick)

□ PMGI under-cut prebake, 150 °C, 3 min

□ Allow wafer to cool to RT

☐ Spin on positive-tone S1813 G2 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec (optional)
- Spin: 5000 rpm, 1000 rpm/s, 60 sec (~1.2 µm thick)

☐ Softbake, 115 °C, 60 sec
☐ Expose in Suss MA6/MA8
- 150 mJ/cm^2, g-line filter, vacuum contact, 'SOI 4T Depletion Gates' mask

☐ Develop with MF-319, 60 sec, use gentle agitation
☐ DIW rinse, 60 sec
☐ N_2 blow dry
☐ Hard bake, 90 °C, 10 min

V. Recess BOX by 200 Å using 6:1 BOE
☐ Submerge SOI wafer in 6:1 BOE for 15 sec (etch rate @ 21°C: 860-930 Å/min)
☐ Immediately move SOI wafer to DIW dump-rinse, 3 cycles

VI. Descum SOI wafer in RIE prior to metallization
☐ Pre-clean RIE chamber, recipe: _CNST_ChamberCLEAN_Light
☐ Recipe: LR-Descum-O2-1nm
- O_2 Descum: 30 sccm O_2, 150 W, 200 mTorr, 60 sec

☐ Clean RIE chamber, recipe: _CNST_ChamberCLEAN_Light

VII. Deposit metal gates using the 4Wave IBD/BTD Cluster Sputter tool

A. Tantalum + Gold
☐ Deposit 40 Å tantalum, subroutine: LR_Ta_4nm
☐ Deposit 160 Å gold, subroutine: LR_Au_16nm
☐ Master recipe: LR_TaAu_20nm

B. Chromium
☐ Deposit 200 Å chromium, subroutine: LR_Cr_20nm
☐ Master recipe: LR_Cr_20nm

VIII. Perform lift-off using Remover PG
☐ Submerge SOI wafer in primary bath of Remover PG, 60°C, 30 min
☐ Submerge SOI wafer in secondary bath of Remover PG, 60°C, 10 min
☐ DIW rinse, 1 min
☐ Spin dry in SRD

8. Dice SOI wafer into 10 x 5.6 mm^2 samples

I. Remove old photoresist with Acetone/IPA/DIW clean:
☐ Set hot plate to 120°C
☐ Submerge SOI wafer in hot Acetone for 15-30 min
☐ Sonicate SOI wafer in Acetone for 5 min (optional)

☐ Submerge SOI wafer to hot IPA for 5-10 min
☐ DIW dump-rinse, 3 cycles

II. Remove residual photoresist with Piranha clean:
☐ Solution ratio: 4:1 H_2SO_4:H_20_2
☐ Set hot plate to 120°C
☐ Prepare H_2SO_4 in primary beaker
☐ Prepare H_20_2 in secondary beaker
☐ *Slowly* pour H_20_2 into primary beaker of H_2SO_4
☐ Submerge SOI wafer in Piranha solution for 15-30 min
☐ DIW dump-rinse, 3 cycles
☐ Spin dry in SRD

III. Prepare SOI wafer for dicing
☐ Prime SOI wafer with HMDS in HMDS vapor primer
☐ Spin on positive-tone SPR220-3.0 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec (optional)
- Spin: 3000 rpm, 1000 rpm/s, 60 sec (~2.5 um thick)

☐ Softbake, 115 °C, 90 sec
☐ Apply wafer dicing tape, let cure for at least 1 hour (preferably overnight)

V. Using the Disco DAD3220 at LPS, dice wafers into 10 x 5.6 mm^2 samples
☐ Recommended blade: 35 µm kerf, ZH05-SD2000-N1-50-EE (Disco blade)
☐ Install blade, perform blade-chuck measurement, perform hairline adjustment
☐ Dicing recipe: "SOI 4in", located in folder "LR"
☐ Align wafer and check that indices are correct
☐ Dice wafer, occasionally pause cutting to ensure proper dicing

Disco blades:
35 µm kerf: ZH05-SD2000-N1-50-EE
45 µm kerf: ZH05-SD2000-N1-50-FF
Dicing Blade Technology blades:
230 µm kerf: CA-009-1800-060-H

VI. Take diced wafer into the cleanroom:
☐ Remove diced samples from wafer tape within ~1 hr for best ease of removal
☐ Place diced samples in organizing sample tray

Procedure for Si Wafer (at NIST)

Updated: 05/04/21 by Luke

Summary: Full process for the Si wafer to be bonded with SOI 4T Devices. Process consists of 3 primary steps:

1. Grow 200 Å sacrificial oxide in dry-ox furnace.
2. Photolithography step 1: define mesas.
3. Dice Si wafer into 10 x 5.6 mm^2 samples.

Nominal Si(111) wafer specifications:

Sacrificial oxide thickness: 200 Å
Orientation: (111) +/- 0.1°
Resistivity: >20,000 Ohm-cm
Doping: p-type (B)
Final die dimensions: 10 x 5.6 mm^2

Nominal Si(100) wafer specifications:

Sacrificial oxide thickness: 200 Å
Orientation: (100) +/- 0.5°
Resistivity: >20,000 Ohm-cm
Doping: p-type (B)
Final die dimensions: 10 x 5.6 mm^2

Note: Oxidation times and thicknesses calculated using the Massoud model, not Deal-Grove.

1. Growth of 200 Å sacrificial oxide in high-purity dry-ox furnace

I. Full RCA clean using B102 Furnace RCA bench

- ☐ Pre-soak in DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ SC1: 5:1:1 DIW:NH_4OH:H_2O_2, 80°C, 10 min
- ☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ HF dip: 50:1 DIW:HF, 21°C, 15 sec
- ☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ SC2: 5:1:1 DIW:HCl:H_2O_2, 80°C, 10 min
- ☐ DIW dump-rinse, 3 cycles, wait for resistivity to reach 14 MΩ-cm.
- ☐ Spin dry in SRD

II. Grow oxide in Sandvic high-purity dry-oxidation tube furnace

- ☐ Si(111) Recipe: 950°C, 17 min, 33 sec
- ☐ Si(100) Recipe: 950°C, 30 min, 50 sec
- ☐ Si(110) Recipe: 950°C, 16 min, 44 sec

III. Measure post-oxidation SiO_2 thickness using J. A. Woollam ellipsometer

☐ Collect data using recipe: 4in_13pt
☐ Analyze data using recipe: SiO2-Si_model

2. Photolithography step 1: define mesas

I. Clean Substrate
☐ Piranha clean Si wafer using high-purity SSEC single wafer cleaning system
☐ Repeat Piranha clean if necessary

II. Photolithography
☐ Prime Si wafer with HMDS in HMDS vapor primer
☐ Spin on positive-tone SPR220-3.0 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec
- Spin: 3000 rpm, 1000 rpm/s, 60 sec (~2.5 µm thick)

☐ Softbake, 115 °C, 90 sec
☐ Expose in Suss MA6/MA8 aligner
- 280 mJ/cm^2, i-line filter, hard contact, "Si(111) Mesa" mask

☐ Post exposure bake, 115 °C, 90 sec
☐ Develop with Microposit MF CD-26, 60 sec, use gentle agitation
☐ DIW rinse thoroughly, 60 sec
☐ N_2 blow dry
☐ Hard bake, 115 °C, 60 sec

III. Remove sacrificial oxide using 6:1 BOE
☐ Submerge Si wafer in 6:1 BOE for 20 sec (etch rate @ 21°C: 860-930 Å/min)
☐ DIW dump-rinse, 3 cycles

IV. Define mesas using RIE
☐ Pre-clean RIE chamber, recipe: CNST_ChamberCLEAN_Light
☐ Mesa etch recipe: LR-Si-Mesa-O2/SF6
- O_2 Descum: 20 sccm O_2, 150 W, 200 mTorr, 30 sec
- Si etch: 10 sccm SF_6, 100 W, 10 mTorr, 15-20 min
- O_2 Ash: 20 sccm O_2, 150 W, 40 mTorr, 30 sec

☐ Clean RIE chamber, recipe: CNST_ChamberCLEAN_Heavy

3. Dice Si wafer into 10 x 5.6 mm^2 samples

I. Remove old photoresist with Acetone/IPA/DIW clean:
☐ Set hot plate to 120°C
☐ Submerge Si wafer in hot Acetone for 15-30 min
☐ Sonicate Si wafer in Acetone for 5 min (optional)
☐ Submerge Si wafer in hot IPA for 5-10 min
☐ DIW dump-rinse, 3 cycles

II. Remove residual photoresist with Piranha clean:

☐ Solution ratio: 4:1 H_2SO_4:H_20_2
☐ Set hot plate to 120°C
☐ Prepare H_2SO_4 in primary beaker
☐ Prepare H_20_2 in secondary beaker
☐ *Slowly* pour H_20_2 into primary beaker of H_2SO_4
☐ Submerge Si wafer in Piranha solution for 15-30 min
☐ DIW dump-rinse, 3 cycles
☐ Spin dry in SRD

III. Prepare Si wafer for dicing
☐ Prime Si wafer with HMDS in HMDS vapor primer
☐ Spin on positive-tone SPR220-3.0 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec
- Spin: 3000 rpm, 1000 rpm/s, 60 sec (~2.5 um thick)

☐ Softbake, 115 °C, 90 sec
☐ Apply wafer dicing tape, let cure for at least 1 hour (preferably overnight)

V. Using the Disco DAD3220 at LPS, dice wafers into 10 x 5.6 mm^2 samples
☐ Recommended blade: 35 µm kerf, ZH05-SD2000-N1-50-EE (Disco blade)
☐ Install blade, perform blade-chuck measurement, perform hairline adjustment
☐ Dicing recipe: “Si 4in”, located in folder “LR”
☐ Align wafer and check that indices are correct
☐ Dice wafer, occasionally pause cutting to ensure proper dicing

Disco blades:
35 µm kerf: ZH05-SD2000-N1-50-EE
45 µm kerf: ZH05-SD2000-N1-50-FF
Dicing Blade Technology blades:
230 µm kerf: CA-009-1800-060-H

VI. Take diced wafer into the cleanroom:
☐ Remove diced samples from wafer tape within ~1 hr for best ease of removal
☐ Place diced samples in organizing sample tray

Procedure for SOI Proximity Enhancement Gates (at LPS)

Updated: 05/04/2021 by Luke

Summary: Full process for the proximity enhancement gates for the SOI 2T test device. Process consists of 3 primary steps:

1. Photolithography step 1: ohmic contacts and self-aligned metallization (lift-off)
2. Photolithography step 2: define the proximity enhancement gates
3. Metallization subtraction: Cr wet etch, or Au wet etch and Ta dry etch

1. Photolithography step 1: ohmic contacts & self-aligned metallization (lift-off)

I. Clean substrate (if necessary)

☐ Piranha clean SOI wafer (3:1 H_2SO_4:H_2O_2)

II. Photolithography (lift-off)

☐ Dehydrate SOI wafer in oven, 140 °C, 30 min

☐ Spin on HMDS adhesion layer
- Spin: 3000 rpm, 1000 rpm/s, 60 sec
- Recipe: LR3000RPM

☐ Spin on PMGI SF6 2S lift-off resist
- Spin: 2500 rpm, 5000 rpm/s, 45 sec (~35 nm thick)
- Recipe: LR2500RPM SFG2S

☐ PMGI under-cut prebake, 150 °C, 3 min

☐ Allow wafer to cool to RT

☐ Spin on positive-tone S1813 G2 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec (optional)
- Spin: 5000 rpm, 1000 rpm/s, 60 sec (~1.2 µm thick)
- Recipe: LR5000RPM

☐ Softbake, 115 °C, 60 sec

☐ Expose in Suss MJB4 aligner:
- 150 mJ/cm^2, UV400 filter, vacuum contact, ‘SOI Ohmic Contacts’ mask

☐ Develop with Microposit MF CD-26, 60 sec, use gentle agitation

☐ DIW rinse, 60 sec

☐ N_2 blow dry

☐ Hard bake, 90 °C, 10 min

III. Define ohmic contacts using Plasma Therm 790 RIE

☐ Pre-clean RIE chamber, recipe: O2CHAMBR, 10 min

☐ O_2 Descum, recipe: LRDESCUM, 30 sec

□ SiO_2 Etch, recipe: LR_SIO2, 30 sec (~30 nm/min)
□ Si Etch, recipe: LR_SOC, 45 sec (~55 nm/min)
□ O_2 Descum, recipe: LRDESCUM, 10 sec (optional)
□ Clean RIE chamber, recipe: O2CHAMBR, 5 min
□ Total etch depth: ~45 nm (Top-ox: 10 nm, n^+-Si: 20 nm, BOX etch: ~15 nm)

IV. Deposit metal using the CHA e-beam evaporator

A. Chromium
□ Allow chamber to stabilize to ~5 x 10^{-7} Torr
□ Deposit 10-20 nm chromium, 1 Å/s,
□ Material: Cr, #20
□ Recipe: Cr, #42
□ Current tooling factor: 160%

-or-

B. Tantalum
□ Allow chamber to stabilize to ~5 x 10^{-7} Torr
□ Deposit 5 nm tantalum, 1 Å/s,
□ Material: Ta, #
□ Recipe: Ta, #
□ Current tooling factor:

C. Gold
□ Allow chamber to stabilize to ~5 x 10^{-7} Torr
□ Deposit 5-15 nm gold, 1 Å/s,
□ Material: Au, #
□ Recipe: Au, #
□ Current tooling factor:

V. Perform lift-off using Remover PG
□ Submerge SOI wafer in primary bath of Remover PG, 80°C, 30 min (or until clean)
□ Submerge SOI wafer in secondary bath of Remover PG, 80°C, 10 min
□ DIW rinse, 1 min
□ N_2 blow dry

2. Photolithography step 2: define proximity enhancement gates

I. Clean substrate
□ Piranha clean SOI wafer (3:1 H_2SO_4:H_2O_2)

II. Photolithography
□ Dehydrate SOI wafer in oven, 140 °C, 30 min
□ Allow wafer to cool to RT

☐ O_2 descum in RIE, recipe: LRDESCUM, 30 sec
☐ Spin on HMDS adhesion layer
- Spin: 3000 rpm, 1000 rpm/s, 60 sec
- Recipe: LR3000RPM

☐ Spin on positive-tone S1813 G2 photoresist
- Pre-spin: 500 rpm, 5000 rpm/s, 1 sec (optional)
- Spin: 5000 rpm, 1000 rpm/s, 60 sec (~1.2 μm thick)
- Recipe: LR5000RPM

☐ Softbake, 115 °C, 60 sec
☐ Expose in Suss MJB4 aligher:
- 150 mJ/cm^2, UV400 filter, vacuum contact, 'SOI Proximity Gates' mask

☐ Develop with Microposit MF CD-26, 60 sec, use gentle agitation
☐ DIW rinse, 60 sec
☐ N_2 blow dry
☐ Hard bake, 90 °C, 10 min

III. Descum SOI wafer in RIE
☐ O_2 Descum, recipe: LRDESCUM, 30 sec
☐ Clean RIE chamber, recipe: O2CHAMBR, 5 min

3. Metallization subtraction: Cr, or Au and Ta

I. Chromium wet etch:
☐ Submerge SOI wafer in Transene Chromium Etchant 1020AC for 8-13 sec (~28 Å/sec)
☐ *Optional: dilute Transene Chromium Etchant 1020AC 2:1 with DIW to halve etch rate*
☐ Submerge SOI wafer in primary beaker of DIW for 15 sec
☐ Submerge SOI wafer in secondary beaker of DIW for 1 min
☐ N_2 blow dry

II. Gold wet etch:
☐ Submerge SOI wafer in Transene Gold Etchant TFA for 5-10 sec (~28 Å/sec)
☐ *Optional: dilute Transene Gold Etchant TFA 2:1 with DIW to halve etch rate*
☐ Submerge SOI wafer in primary beaker of DIW for 15 sec
☐ Submerge SOI wafer in secondary beaker of DIW for 1 min
☐ N_2 blow dry

III. Tantalum dry etch:
☐ Pre-clean RIE chamber, recipe: O2CHAMBR, 10 min
☐ Ta Etch, recipe: LR_Ta (~0.2 nm/s)
☐ Clean RIE chamber, recipe: O2CHAMBR, 10 min

Procedure for SOI-Si Bonding

Updated: 05/04/21 by Luke

Summary: Full process for SOI-Si bonding procedure. Process consists of 5 primary steps:

1. Final cleaning of SOI and Si samples (Acetone/IPA/DIW and Piranha).
2. Transfer cleaned samples to N_2-ambient glovebox in room 1204.
3. Etch and H-terminate SOI and Si samples in deoxygenated chemistry.
4. Load and bond samples in bonding chamber.
5. Transfer samples to N_2-ambient glovebox in room 1241 for wiring.

1. Final cleaning of SOI and Si samples

This step should be done using clean personal glassware

I. Locate personal glassware, prepare chemistry, clean samples:

- ☐ Personal glassware located in the LPS cleanroom 10K area
- ☐ Only use clean Teflon tweezers
- ☐ Prepare Acetone and IPA beakers (~80 mL each)
- ☐ Place Acetone and IPA beakers on hotplate (120°C)
- ☐ Select 2 SOI samples and 2 Si samples, place them securely in Teflon boat
- ☐ Submerge samples in hot Acetone
- ☐ Prepare H_2SO_4 beaker (60 mL) and H_2O_2 (20 mL), set aside, do not mix
- ☐ Transfer samples to hot IPA
- ☐ During IPA clean, slowly pour H_2O_2 into H_2SO_4 beaker
- ☐ Stir fresh Piranha mix with Teflon stir rod until thoroughly mixed
- ☐ Place Piranha solution with stir rod on hotplate (120°C)
- ☐ Transfer samples to DIW beaker
- ☐ Transfer samples to Piranha solution, secure Teflon boat with Teflon stir rod
- ☐ Rinse thoroughly (3x) in DIW
- ☐ Spin dry using SRD mobile station

II. Remove protective dicing photoresist with Acetone/IPA/DIW clean:

- ☐ Hot plate is set to 120°C
- ☐ Submerge SOI and Si samples in hot Acetone for 15-30 min
- ☐ Sonicate SOI and Si samples in Acetone for 5 min (optional)
- ☐ Submerge SOI and Si samples in hot IPA for 5-10 min
- ☐ DIW rinse, 1 min

III. Remove residual photoresist with Piranha clean:

- ☐ Solution ratio: 3:1 H_2SO_4:H_20_2
- ☐ Hot plate is set to 120°C
- ☐ Prepare H_2SO_4 in primary beaker
- ☐ Prepare H_20_2 in secondary beaker
- ☐ *Slowly* pour H_20_2 into primary beaker of H_2SO_4

- ☐ Submerge SOI samples in Piranha solution for 15-30 min
- ☐ DIW rinse, 1 min (3x)
- ☐ Spin dry using SRD mobile station
- ☐ Place cleaned samples in a clean sample tray

2. Transfer cleaned samples to N_2-ambient glovebox in room 1204

3. Etch and H-terminate SOI and Si samples in deoxygenated chemistry

I. Prepare deoxygenated chemistry in Teflon beakers:
- ☐ Beaker 1: ~20 mL of 10:1 DIW:HF
- ☐ Beaker 2: ~20 mL of DIW
- ☐ Beaker 3: ~20 mL of high-purity NH_4F
- ☐ Set hotplate to 120°C

II. Etch and H-terminate the Si sample:
- ☐ Etch sacrificial oxide in 10:1 DIW:HF for 2 min
- ☐ Rise Si sample in DIW for 1 min
- ☐ Etch and H-terminate Si sample in high-purity NH_4F for 15 min, do not agitate
- ☐ N_2 blow dry, do not rinse in DIW
- ☐ Place Si sample on hotplate for 1 min

III. Etch and H-terminate the SOI sample:
- ☐ Begin SOI etch when Si sample has 1 min remaining in high-purity NH_4F
- ☐ Etch sacrificial oxide and H-terminate in 10:1 DIW:HF for 90 sec
- ☐ N_2 blow dry, do not rinse in DIW
- ☐ Place SOI sample on hotplate for 1 min

IV. Place SOI and Si samples in bonding puck:
- ☐ While SOI sample in on hotplate, place Si sample face-up in bonding puck
- ☐ Place SOI sample face-down in bonding puck

4. Load and bond samples in bonding chamber

I. Load samples into transfer chamber:
- ☐ Using metal tweezers, place bonding puck onto the transfer chuck
- ☐ Close transfer chamber door, close green inlet valve
- ☐ Turn on turbo pump
- ☐ Set transfer chuck heater to 150°C (actual sample temperature ~115°C), 5 min
- ☐ Allow transfer chamber to reach 0.5 mTorr
- ☐ Turn on thermal lamp and bonding monitor

II. Load samples into bonding chamber:

- ☐ Slowly open gate valve between transfer chamber and bonding chamber
- ☐ Move bonding puck into the bonding chamber using the transfer rod
- ☐ Allow bonding chamber to reach ~10^{-6} mbar

III. Bond samples using micron actuator
- ☐ Slowly raise the sapphire rod until samples are picked up, lying flat upon one another only under the force of gravity
- ☐ Continue raising sapphire rod and initiate bonding by slowly and gently pressing samples between the sapphire rod and the sapphire boss
- ☐ Bond will be detected by infrared camera
- ☐ Release pressure and return samples to bonding puck
- ☐ Ensure that samples are bonded by observing that they do not come apart

IV. Unload bonded samples from bonding chamber
- ☐ Return bonding puck to transfer chamber using transfer rod
- ☐ Close gate valve between transfer chamber and bonding chamber
- ☐ Turn off turbo pump, allow to spin down for ~10 min
- ☐ Slowly open green leak valve until transfer chamber reaches 750 Torr
- ☐ Remove bonding puck from transfer chamber using metal tweezers

V. Clean up chemistry
- ☐ Dispose of used chemistry in the HF waste container
- ☐ Turn off hotplate
- ☐ Turn off N_2 gun supply

5. Transfer bonded sample to N_2-ambient glovebox in room 1241

I. Transfer bonded sample to N_2-ambient glovebox in room 1241 for wiring
- ☐ Place bonded sample in a hermetically sealed container inside 1204 glovebox
- ☐ Transfer bonded sample to glovebox in room 1241
- ☐ Open container inside 1241 glovebox and allow sample to equilibrate in N_2

Appendix B: Gallium nanowires fabricated via focused-ion beam lithography

This appendix contains some of the research I did towards the beginning of my tenure at LPS. At that point, I was attempting to fabricate in-plane nanowires and quantum point contacts on Si surfaces using gallium focused-ion beam direct-write lithography. The following pages are an abridged version of my candidacy paper that I wrote in the summer of 2017. Its purpose was to lay down a foundation for my future research, almost like a proposal and miniature literature review. Shortly afterwards in the fall of 2017, however, we switched focus and began to develop the non-invasive SOI devices, and this project was mostly scrapped. I've included this appendix to have a repository of the work I had begun, and the references for this section can be found here: [42, 66, 233–263].

I. Introduction

In this report I will detail the design and fabrication of our devices and introduce further developments that improve our device performance and allow us to investigate new 1D physics. In particular, I will focus on recent efforts to extend our probe of 2D electron transport in H-Si(111) to the nanoscale using a novel, focused-ion beam (FIB) direct-write implant lithography technique. Using this method, we can directly pattern quantum point-contacts (QPCs) onto the H-Si(111) surface and use these in-plane, degenerately-doped, lateral depletion gates to confine the 2DES to a 1DES. 1D confinement at low temperatures will lead to quantized conductance of the electrons and, due to the electron effective mass anisotropy in Si, it is predicted that valley filter phenomena may emerge [232].

II. Device Architecture and Fabrication

Device Architecture

Our devices are comprised of two pieces in a flip-chip assembly which are bonded together under high-vacuum and adhere to one another through Van der Waals

forces. The first piece, the H-Si(111) device piece, is a hydrogen-terminated Si(111) chip whose surface is host to a 2DES with unique symmetries and properties. Moreover, the Si(111) surface in our devices is hydrogen-terminated using an ultra-pure ammonium fluoride solution (40% NH_4F in H_2O). Wet treatment of the Si(111) surface using an NH_4F solution anisotropically etches any structural non-uniformities resulting in an ultra-flat, atomically smooth, hydrogen-passivated surface [42]. The second piece, the SiO_2-Si(100) remote gate piece, has a vacuum cavity that induces and encapsulates the 2DES on the H-Si(111) surface. A vacuum-dielectric remote-gate eliminates issues associated with lattice strain and interface oxide traps, inherent in traditional MOSFET devices [66]. A schematic of the device architecture can be seen in Fig. B.1.

Low temperature (300 mK) 2D transport is probed using 6 in-plane, degenerately-doped n^+ (P) ohmic contacts aligned along the major axes of the constant-energy ellipses. This allows us to probe the underlying symmetries of the 2DES through a series of magnetoresistance measurements. Six additional in-plane, degenerately-doped p^+ (B) ohmic contacts confine the 2DES and provide electrostatic isolation between adjacent n^+ ohmic contacts. These p^+ ohmic contacts can also serve as lateral depletion gates, modulating the large-channel (~10 μm) conductance of the 2DES. If extended to the nano-scale, or small-channel (~100 nm), these p-type lateral depletion gates will further confine the 2DES leading to 1D confinement and quantized conductance of the 2DES. We aim to achieve this 1D confinement by extending the p^+ ohmic contacts using a FIB for direct-write implant lithography. Using this technique, we can directly pattern QPCs of various size and separation distance onto the H-Si(111) surface.

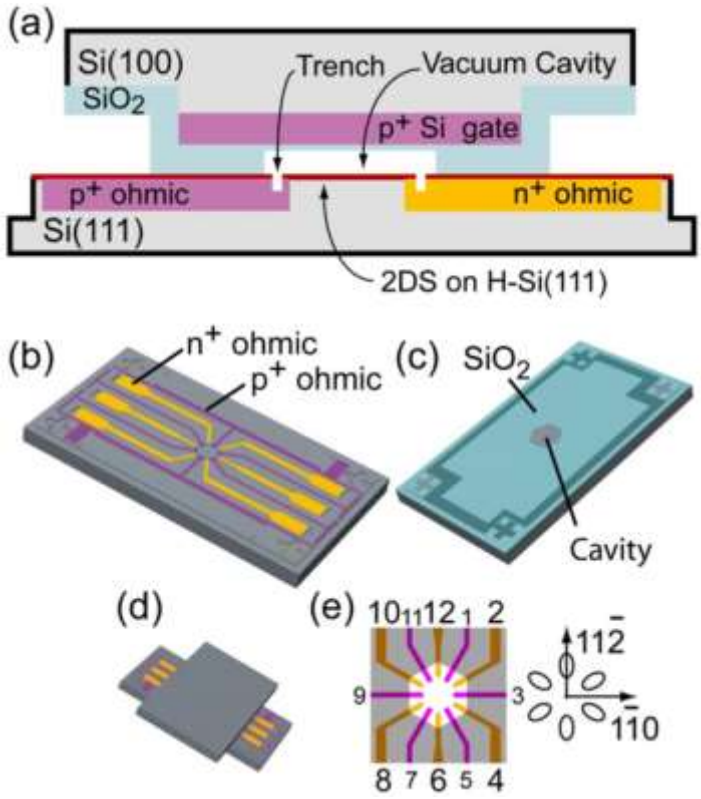

Figure B.1. (a) Cross-section of bonded device highlighting the vacuum cavity encapsulating the 2DES, (b) H-Si(111) piece with 12 ohmic contacts, (c) Fully-insulated SiO_2-Si(100) remote gate piece with center cavity, (d) bonded device, (e) ohmic contacts arranged in clock-scheme configuration next to coordinate map, illustrating the n^+ ohmic contacts overlay with the valley projections.

H-Si(111) Device Piece

The H-Si(111) piece is fabricated on a p^- high-purity Si(111) wafer (float zone, resistivity >10,000 Ω·cm). After a standard RCA clean (with HF dip), the wafer is immediately transferred to a CMOS tube furnace for growth of a ~20 nm sacrificial dry thermal oxide. This thin sacrificial oxide protects the Si(111) surface during the remainder of processing and is removed just prior to hydrogen termination and bonding. Next, a 2 μm deep Si mesa layer is formed by etching around the perimeter of each die

using reactive ion etching (RIE). This layer serves primarily to protect the final bonding process against rough edges created during dicing, but also to create permanent alignment marks for the remaining lithography steps. The wafer is then prepared and outsourced for boron implantation (9 x 10^{14} cm^{-2}, 15 keV, 7° tilt), after which the returned wafer is cleaned, prepared, and outsourced again for phosphorous implantation (4.5 x 10^{14} cm^{-2}, 50 keV, 7° tilt). These two ion implantation steps define the 6 p^+ and 6 n^+ ohmic contacts used to confine and probe the 2DES, respectively. After implantation, the dopants are activated by a CMOS-compliant rapid thermal anneal (RTA) treatment of 950°C for 1 minute. An optional final lithography step can be performed to remove the sacrificial oxide directly above the 2DES active region if it is desirable to pattern QPCs with a FIB without implanting through the oxide. The wafer is then diced into samples measuring 5.6 x 10 mm^2. Individual samples are then loaded into a dual-beam FIB/SEM tool for the patterning of Ga nanowires or QPCs using direct-write implant lithography (1 x 10^{15} cm^{-2}, 30 keV, 0° tilt). This step requires focusing the FIB off-site from the location of final writing, which in our device is done by focusing on 1 or more of 4 alignment marks placed symmetrically around and within ~50 microns of the 2DES active region. Imaging with a FIB is inherently destructive, so all imaging of the 2DES active region must be done using the SEM to avoid stray ion contamination. To activate the newly implanted Ga, the samples once again undergo a CMOS-compliant RTA treatment, however, a recipe of 650°C for 30 seconds is used to mitigate the lateral diffusion of the Ga atoms. Finally, the H-Si(111) samples are cleaned and moved to an oxygen-free environment (<4 ppm O_2). The sacrificial oxide is removed using a 20:1 HF solution and the Si(111) surface is hydrogen-passivated by submersion in a high-purity ammonium fluoride

solution (40% NH_4F in H_2O) for 15 minutes. The ammonium fluoride solution anisotropically etches any non-uniform Si features that may cause surface roughness, producing an ultra-flat, atomically smooth, hydrogen-terminated surface.

SiO_2-Si(100) Remote Gate Piece

The second component of our devices is the fully-insulated SiO_2-Si(100) remote gate piece with vacuum dielectric. A Si(100) wafer (float zone, Si:B, resistivity >10,000 Ω·cm) is outsourced for boron implantation (2.4 x 10^{15} cm^{-2}, 15 keV, 7° tilt) which forms the gate's conducting layer. Next, a 2 μm deep Si mesa layer is formed by etching around the perimeter of each die using reactive ion etching (RIE). This step serves an identical purpose to the mesa etch of the H-Si(111) piece. The wafer is then sent through a standard RCA clean (SC1, SC2, no HF dip) and immediately transferred to a tube furnace for the dopant activation and gate oxide growth steps. A ~340nm layer of SiO_2 is thermally grown using a anneal/dry/wet/dry recipe at 1050°C for 20/15/30/15 minutes, respectively. Following oxidation, the SiO_2 around the perimeter of the mesas is wet-etched (BOE 6:1) forming a 100nm deep recess in the oxide to preserve the original flatness of the mesa layer. In the final step, a cavity is formed in the SiO_2 using a dry-etch (RIE) followed by a controlled wet-etch (BOE 6:1) until ~30nm oxide remains. With approximately a 10:1 vacuum:SiO_2 cavity ratio, the total dielectric is very close to vacuum while also being fully insulated against gate leakage to the 2DES. The wafer is then diced into samples also measuring 5.6 x 10 mm^2, and prepared for final bonding with the H-Si(111) piece.

III. Writing Gallium Wires and QPCs with a FIB

Gallium and Boron Acceptors

Boron is typically the ion of choice for p-type doping of Si due to nearly 100% of dopants achieving electrical activation after annealing, although other column III species (Al, Ga, In, Tl) can be used as well [233-235]. Diffusion rates through Si and SiO_2 during high temperature processing vary greatly between implant species, therefore selecting the appropriate annealing schedule is important [236-242]. In the case of our experiment reported here, we use a combination of B and Ga as our implant species, with Ga implants in particular adhering to tight annealing procedures. Conventional B implantation through lithographically patterned masks is used to define the main p-type ohmic contacts, while Ga is used to directly pattern QPCs as nano-scale extensions of the B contacts. The central motivation for selecting Ga in addition to B is that Ga is used in most FIB microscopes as the primary ion source due to its near room-temperature melting point. Using a FIB, we pattern QPC's through direct-write implant lithography as a substitute for traditional direct-write e-beam lithography.

Background on Ga FIB Wires

Nanowires have many practical applications in response to the ever-decreasing geometry demands of electronic device technology, from component interconnects to transistors themselves [243-245]. Nanowires also provide a natural approach for probing 1D transport in 3D materials due to their intrinsically 1D geometry. Diameters typically range in size from tens of nanometers to a few and even single atoms [246, 247]. The

lateral confinement of carriers gives rise to discrete sub-band energies leading to quantized conductance of the electrons at low temperatures. Nanowires come in a variety of flavors as well including superconducting, metallic, semiconductor, and insulating, and there exists many design and fabrication techniques for such nanostructures [247-251].

Experiments in recent decades, however, have explored a new approach to fabricating nanowires in Si by directly doping via FIB implant lithography, in contrast to conventional ion implantation through an e-beam defined mask [252-255]. This mask-less lithography technique provides greater flexibility in patterning while still maintaining the precision required for nanowire fabrication. One group has even demonstrated progress towards precision single-ion placement of Ga in Si using a FIB [256]. This could provide a possible supplementary technique to the currently dominant STM hydrogen lithography for single-atom placement of P-donors in Si [257, 258]. Others have demonstrated the fabrication of nanostructures using a combination of FIB implantation and anisotropic wet-etching, with the Ga-implanted Si acting as a resist-less mask with very high selectivity [259, 260]. Of particular interest to our work, another group has demonstrated the effectiveness of FIB implanted Ga nanowires as lateral depletion gates in an in-plane FET device [261]. We want to use this FIB technology to incorporate these Ga in-plane lateral depletion gates (QPCs) into our devices to locally confine the 2DES to a 1DES and investigate the 1D transport of our system.

Patterning Ga Nanowires in Si

In order to ensure that FIB implanted Ga would work as good in-plane lateral depletion gates, 2 Ga nanowires of widths 150 nm and 40 nm as well as a 30 nm wire with a 250 nm gap, seen in Fig. B.2, were fabricated and sheet resistance was measured at 4.2 K. Several experiments have determined that a FIB dose of 1 x 10^{15} cm^{-2} would be sufficient to exceed the metal-insulator transition for Ga in Si and lead to ohmic conduction [233-235]. In a previous experiment of our own, several conventionally implanted Ga-Si samples with the aforementioned dose underwent a range of RTA treatments from 550°C-700°C for 30 seconds to determine the optimal annealing schedule. We determined that a RTA treatment of 650°C for 30 seconds was sufficient to achieve solid-phase epitaxial regrowth of the amorphous implanted Si while also minimizing the lateral diffusion of Ga, in good agreement with the literature [66, 232, 233, 239-241, 262]. After patterning the wires, the FIB samples underwent the same RTA treatment to activate the dopants. The samples were then submerged in liquid He and measured with a lock-in at low frequency ($100/2\pi \approx 15.915$ Hz) using a 4-terminal Van der Pauw configuration. All wires showed good conductance at low temperature, with the gapped wire showing noticeably higher resistance than the non-gapped wire of similar size.

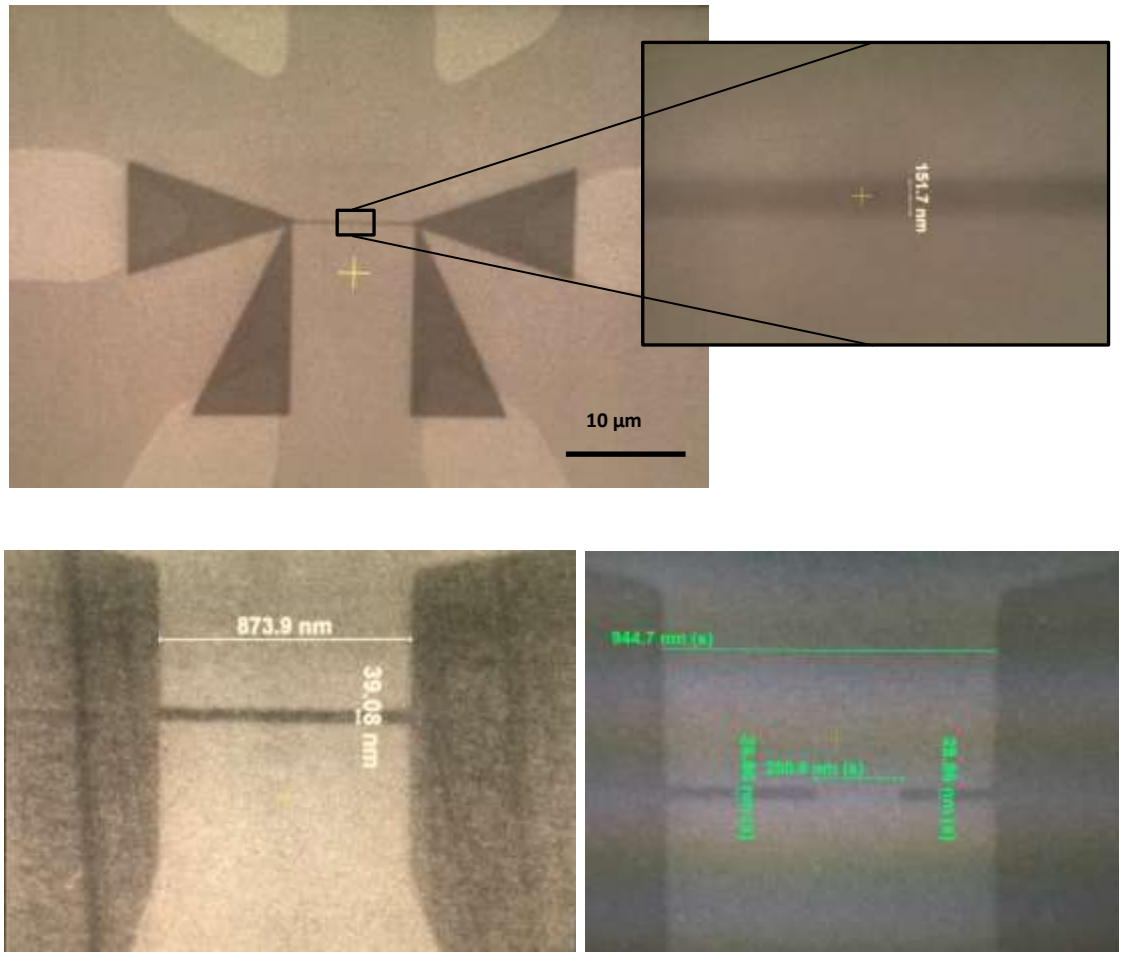

Figure B.2. SEM images of a 150 nm wire (top) with a sheet resistance of 1.3 kΩ/□, a 40 nm wire (left) with a sheet resistance of ~5.5 kΩ/□, and a 30 nm wire (right) with 250 nm gap with a sheet resistance of ~26.5 kΩ/□, all measured at 4.2 K.

This suggests that conduction is primarily through the wires themselves and substrate conduction has been frozen out. We concluded from these results that using a FIB to pattern nanowires and eventually QPCs will be viable using the dose and RTA treatment mentioned.

Patterning Ga QPCs in Si

FIB implanted QPCs were fabricated using the same recipe as the Ga nanowires in the previous section. In one sample, shown in Fig. B.3, QPCs of separation distance 250 nm and 500 nm were fabricated and transport was measured at 4.2 K. From the SEM images, it is clear that the FIB implanted regions are very sharp, and no visible ion contamination can be seen in the channels. If necessary, a more thorough analysis of dopant concentration and contamination in and around the channel could be performed using secondary-ion mass spectroscopy (SIMS) profiling.

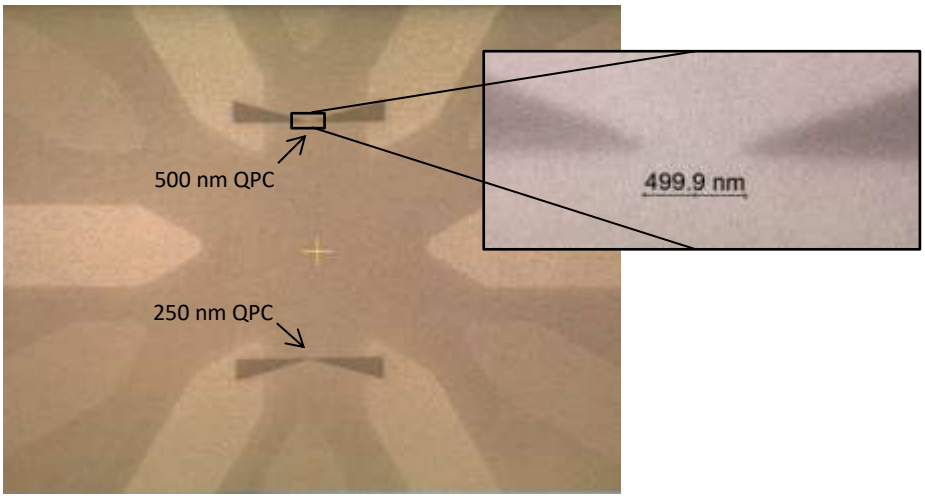

Figure B.3. SEM images of device with 500 nm and 250 nm QPCs before RTA treatment.

After fabrication of the QPCs, the sample was cooled to 4.2 K in a Heliox He-3 system. Initial baseline measurements of QPC leakage into the 2DES were performed, demonstrating insignificant leakage (< 100 pA) for reverses biases up to ~7 V. Resistivity and Hall measurements were performed yielding a peak carrier density of 6.2 x 10^{12} cm^{-2} and a mobility of ~150 $cm^2/V{\cdot}s$. In contrast to previous record mobilities in similar devices exceeding 300,000 $cm^2/V{\cdot}s$, the mobility measured here is quite low and is

possibly due to ion contamination or surface degradation. Further investigation into this issue is underway and will be a part of a series of ongoing measurements to determine the cause. Four-terminal measurements of conductance modulation of the large-channel gave expected results, as seen in Fig. B.4. Two-terminal I-V curves were also measured for the 500 nm QPC (small-channel), also shown in Fig. B.4. Resistance through the small channel was very large, exceeding 160 MΩ, possibly due to complete channel pinch-off from the QPCs. At this point, however, it is not clear what exactly the cause of this large resistance may be.

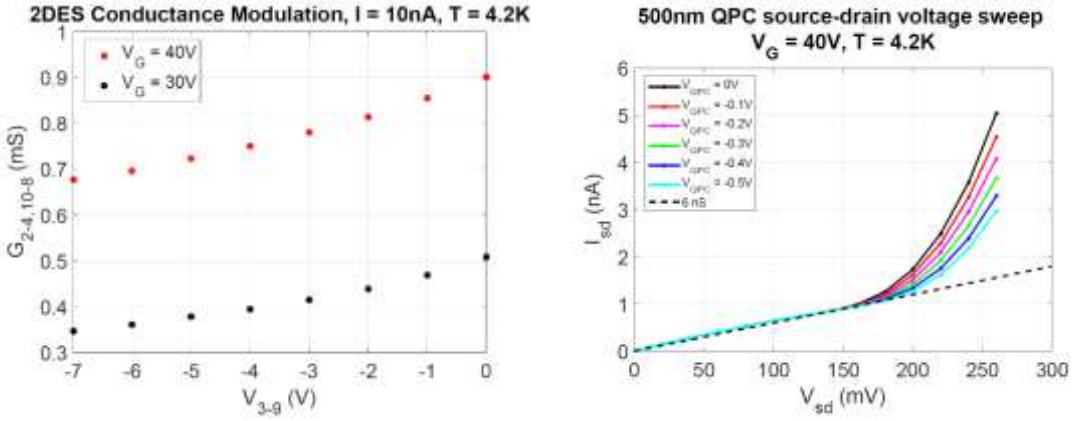

Figure B.4. (left) Large-channel conductance modulation for two different gate voltages, and (right) small-channel current modulation at different QPC reverse biases.

IV. Discussion and Conclusions

From the data in the previous sections, it is clear that the device's intended functionally has not yet been realized. The sample mobility is much lower than previous devices of similar architecture, which is the first issue that needs to be resolved. Two possible explanations for the unusually low mobility immediately stand out. The first and

most obvious is that the 2D active region has been contaminated by stray ion implantation during FIB writing. The second issue is surface degradation. During the device processing of the H-Si(111) piece, the last optional lithography step was included in order to locally remove the sacrificial oxide just above the 2D active region. The reason for including this step was two-fold: to mitigate the amount of oxygen contamination in the QPCs after Ga implantation, and to prevent Ga diffusion through the oxide to unknown off-site locations during the RTA treatment. In removing the protective oxide, however, the surface may have been exposed to other ambient contaminants creating additional scattering centers as well as surface roughness.

Once the issue of mobility has been resolved, the next step will be to optimize the QPC separation distance to ensure robust control of the small channel. If the separation distance is too close, complete channel pinch-off can occur at zero bias, and if the channel is too wide, breakdown of the QPC-2DES p-n junction will occur before the channel can be pinched off. Another adjustment that must be made in future devices is to pattern the QPCs in such a way that 4-terminal measurements can be made for the small channel.

At the time of writing this report (summer 2017), we are in the process of bonding and wiring up a new sample which has not undergone FIB implant lithography, but is otherwise identical to the sample with the 250 nm and 500 nm QPCs. If the mobility of this new sample dramatically improves, it will strongly suggest that the issue is Ga contamination from the FIB. If the new sample turns out to also have a similar low mobility, then we will move towards using samples which have not had the sacrificial oxide removed over the 2D active region. Although there remains a great deal of work to

be done in improving the device performance, we are confident that we will eventually be able to achieve our intended goal of local 1D confinement of the 2D system. The nanowire data presented in this paper demonstrates that we can in fact pattern lateral depletion gates using a FIB. Achieving 1D confinement, however, may require some additional fine tuning of the FIB writing specifications and procedures as well as tighter device processing.

V. Towards the Future: Valley Filters

The ultimate realization of our devices is to use the local 1D confinement of the 2DES to filter through electrons that occupy specific valleys. This phenomenon, known as valley filtering, arises due to the anisotropic electron effective mass in Si and other multi-valley systems [66, 232]. The relationship between conduction band curvature and electron effective mass, m^*, is given by the effective mass tensor [66]:

$$\frac{1}{m_{ij}^*} = \frac{1}{\hbar^2}\frac{\partial^2 E(k)}{\partial k_i \partial k_j}$$

Electrons in valleys that are perpendicular (or are not parallel) to the direction of transport will have a larger transverse mass compared to electrons occupying valleys that are parallel to the direction of transport. When the 2DES is locally confined by the QPCs, the potential energy landscape becomes quasi-harmonic in the transverse direction, illustrated below in Fig. B.5. It is well known that the level spacing in a harmonic potential is inversely proportional to the square root of the particle mass, therefore electrons with a heavier transverse mass will have lower ground state energies and tighter

energy bands. When the QPCs are relaxed from a completely pinched-off channel, the first transmission states to emerge in the channel will be those of the electrons with heavier effective mass.

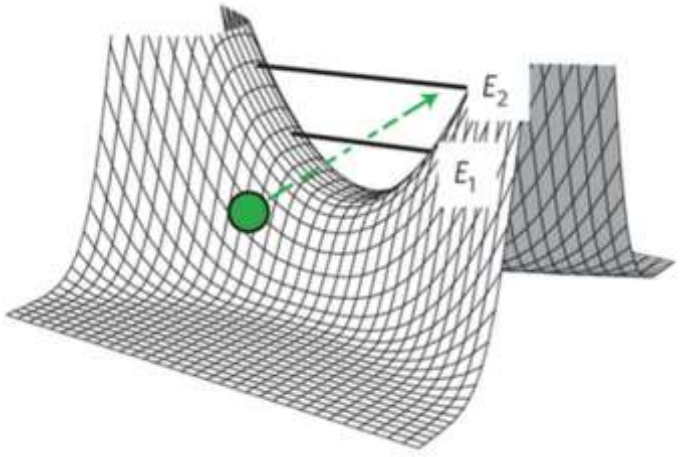

Figure B.5. QPC saddle potential illustrating the quasi-harmonic potential landscape in the transverse direction. Electrons with large transverse effective mass will have lower ground state energies and tighter level spacing in the near-pinched-off regime, allowing for selective transmission of these carriers. *Image from Adam Micolich, Nature Physics* ***9****, 530, (2013).*

In this way, electrons in valleys with heavy transverse mass can be filtered through the QPCs with the appropriate tuning. For devices with extremely high mobility, such as ours, *k* is a good quantum number and electrons should only undergo inter-valley scattering due to the presence of an impurity (intentional or unintentional), such as a single-electron occupying a precisely placed P-donor. This has many implications for donor-based measurements schemes for quantum information processing, due to the extreme sensitivity to inter-valley scattering.

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