Parallel Algorithms for Image Histogramming and Connected Components with an Experimental Study

David A. Bader*
dbader@eng.umd.edu

Joseph JáJá†
joseph@umiacs.umd.edu

Institute for Advanced Computer Studies, and
Department of Electrical Engineering,
University of Maryland, College Park, MD 20742

December 9, 1994

Abstract

This paper presents efficient and portable implementations of two useful primitives in image processing algorithms, histogramming and connected components. Our general framework is a single-address space, distributed memory programming model. We use efficient techniques for distributing and coalescing data as well as efficient combinations of task and data parallelism. Our connected components algorithm uses a novel approach for parallel merging which performs drastically limited updating during iterative steps, and concludes with a total consistency update at the final step. The algorithms have been coded in Split-C and run on a variety of platforms. Our experimental results are consistent with the theoretical analysis and provide the best known execution times for these two primitives, even when compared with machine specific implementations. More efficient implementations of Split-C will likely result in even faster execution times.

1 Problem Overview

Given an $n \times n$ image with k grey levels on a p processor machine ($p \leq n^2$), we wish to develop efficient and portable parallel algorithms to perform various useful primitive image processing computations. Efficiency is a performance measure used to evaluate parallel algorithms. This measure provides an indication of the effective utilization of the p processors relative to the given parallel algorithm. For example, an algorithm with an efficiency near one runs approximately p times faster on p processors than the same algorithm on a single processor. Portability refers to code that is written independently of low-level primitives reflecting machine architecture or size. Our goal is to develop portable algorithms that are scalable in terms of both image size and number of processors, when ran on distributed memory multiprocessors.

Our first algorithm computes the histogramming of an image; i.e., the output consists of an array $H[0..k-1]$ held in a single processor such that $H[i]$ is equal to the number of pixels in the image with grey level i. Without loss of generality, k is assumed to be a power of two. The second algorithm performs the connected components of images ([1], [6], [8], [9], [12], [16], [17], [20], [38]). The task of connected component labeling is cited as an important object recognition problem in the DARPA Image Understanding benchmarks ([37], [47]), and also can be applied

*The support by NASA Graduate Student Researcher Fellowship No. NGT-50951 is gratefully acknowledged.
†Supported in part by NSF grant No. CCR-9103135 and NSF HPCC/GCAG grant No. BIR-9318183.

to several computational physics problems such as percolation ([41], [5]) and various cluster Monte Carlo algorithms for computing the spin models of magnets such as the two-dimensional Ising spin model ([2], [3], [4], [39], [40]). All pixels with grey level (or 'color') 0 are assumed to be background, while pixels with color > 0 are foreground objects. A connected component in the image is a maximal collection of pixels such that a path exists between any pair of pixels in the component. Note that we are using the notion of 8-connectivity, meaning that two pixels are adjacent if and only if one pixel lies in any of the eight positions surrounding the other pixel, or 4-connectivity, in which only the north, east, south, and west pixels are adjacent. Each pixel in the image will receive a positive integer label; pixels will have the same label if and only if they belong to the same connected component. Also, all 0-pixels will receive a label of 0.

The majority of previous parallel histogramming algorithms are architecture- or machine-specific and do not port well to other platforms. Table 1 shows some previous running times for histogramming algorithms on parallel machines. Note that several of these machines are special purpose image processing machines. The last column corresponds to a normalized measure of the amount of work per pixel, where the total work is defined to be the product of the execution time and the number of processors. In order to normalize the results between fine- and coarse-grained machines, we divide the number of processors in the fine-grained machines by 32 to compute the work per pixel site.

Year	Researcher(s)	Machine	Processors	Image Size	Time	work per pixel
1980	Marks [32]	AMT DAP	1024	32×32	17.25 ms	539 μs
1983	Potter [36]	Goodyear MPP	16384	128×128	16.4 ms	513 μs
1984	Grinberg, Nudd, and Etchells [15]	3-D machine	16384	256×256	1.7 ms	13.3 μs
1987	Ibrahim, Kender, and Shaw [19]	NON-VON 3	16384	128×128	2.16 ms	67.5 μs
1990	Nudd, et al. [34]	Warwick Pyramid	16K base	256×256	237 μs	2.47 μs
1991	Jesshope [23]	AMT DAP 510	1024	512×512	86 ms	10.5 μs
1994	Bader and JáJá (This paper)	TMC CM-5	16	512×512	12.0 ms	732 ns
		IBM SP-1	16	512×512	9.20 ms	562 ns
		IBM SP-2	16	512×512	20.0 ms	1.22 μs
		Intel Paragon	8	512×512	20.8 ms	635 ns
		Meiko CS-2	4	512×512	15.2 ms	231 ns

Table 1: Implementation Results of Parallel Histogramming Algorithms

As with the histogramming algorithms, most of the previous connected components parallel algorithms as well are architecture- or machine-specific, and do not port easily to other platforms. Table 2 shows some previous running times for implementations of connected components for images using parallel machines. Again, several of these machines are special purpose image processing machines. The second last column corresponds to a normalized measure of the amount of work per pixel, where the total work is defined to be the product of the execution time and the number of processors. Note that only the entries labeled "DARPA II Image" use the benchmark image given in Figure 2. All other test images used are unknown to the authors.

Section 2 describes the algorithmic model used to analyze the algorithms whereas Section 3 describes the input images used, as well as the data layout on the Thinking Machines CM-5, IBM SP-1 and SP-2, Meiko CS-2, and Intel Paragon. The histogramming algorithm is presented in Section 4, and the binary connected components algorithm is described in Section 5. Section 6 generalizes the connected components algorithm to multi-grey level images.

The experimental data obtained reflect the execution times from implementations on the TMC CM-5, IBM SP-1 and SP-2, Meiko CS-2, and the Intel Paragon, with the number of parallel processing nodes ranging from 16 to 128 for each machine when possible. The shared memory model algorithms are written in Split-C [10], a shared memory programming model language which follows the SPMD (single program multiple data) model on these parallel machines, and the source code is available for distribution to interested parties.

Year	Researcher(s)	Machine	PE's	$\sqrt{n^2}$	Time	work/pix	Notes
1986	Little [29]	TMC Connection Machine	65536	512	450 ms	3.53 ms	Scanning alg. DARPA I
1986	Hummel [18]	NYU Ultracomputer	4096	512			Shiloach/Vishkin alg.
1987	Wallace and Howard [44], [45]	HBA	12	512	725 ms	33.2 μs	2-pass swath
1987	Ibrahim, Kender, and Shaw [19]	NON-VON 3	16384	128	12.5 ms	391 μs	4-conn.
1987	Sunwoo, Baroody, and Aggarwal [43]	Intel iPSC	32	256	5.074 s	2.48 ms	8-connectivity
1987	Rosenfeld [37]	BBN Butterfly	128	512	7.2 s	3.52 ms	DARPA I
		TMC CM-1	65536	512	400 ms	3.13 ms	DARPA I
		Columbia NON-VON	$1M$	512	1 s	125 ms	DARPA I (est.?)
		Caltech CUBE	256	512	14 ms	13.7 μs	DARPA I
		Mosaic	16384	512	6 ms	11.7 μs	DARPA I (est.?)
		Encore Multimax	20	512	22.7 s	1.73 ms	DARPA I
		HBA	16	512	170 ms	10.4 μs	DARPA I (est.?)
		HBA	100+	512	370 ms	181 μs	DARPA I (est.?)
1988	Krikelis and Lea [26]	WW Warp	10	512	5.6 s	214 μs	DARPA I
		PC Warp	10	512	980 ms	37.4 μs	DARPA I
		iWarp	72	512	470 ms	129 μs	DARPA I
		Columbia NON-VON	$1M$	512	1 s	125 ms	DARPA I (est.?)
		TMC CM-1	65536	512	400 ms	3.13 ms	DARPA I
1989	Manohar and Ramapriyan [31]	Goodyear MPP	16384	128	97.3 ms	3.04 ms	shrink/expand
1989	Kanade and Webb [24]	Warp	10	512	4.34 s	166 μs	shrnk/expnd, DARPA II Im.
1989	Weems, Riseman, Hanson, and Rosenfeld [48]	Alliant FX-80	8	512	7.225 s	220 μs	DARPA II Image
		Sequent Symmetry 81	8	512	15.12 s	461 μs	DARPA II Image
		Warp	10	512	3.98 s	152 μs	DARPA II Image
		TMC CM-2	32768	512	140 ms	547 μs	DARPA II Image
1990	Falsafi and Miller [14]	Intel iPSC/2	32	512	1.197 s	146 μs	
1991	Parkinson [35]	AMT DAP 510	1024	512	1.27 s	155 μs	
1991	Baillie and Coddington [4], [2]	Ncube-1	32	512	53.4 s	6.52 ms	
		Caltech Symult 2010	32	512	16.7 s	2.04 ms	
		Meiko CS-1	32	512	14.8 s	1.81 ms	
1991	Kistler and Webb [25]	Warp	10	512	1.31 s	50.0 μs	
1992	Choudhary and Thakur [7]	Intel iPSC/2	32	512	1.914 s	234 μs	multi-dim. D+C (partitioned input)
		Intel iPSC/2	32	512	1.649 s	201 μs	multi-dim. D+C (complete im./PE)
		Intel iPSC/2	32	512	2.290 s	280 μs	multi-dim. D+C (cmplt. + collect. comm.)
	(DARPA II Image)	Intel iPSC/860	32	512	1.351 s	165 μs	multi-dim. D+C (partitioned input)
		Intel iPSC/860	32	512	1.031 s	126 μs	multi-dim. D+C (complete im./PE)
		Intel iPSC/860	32	512	947 ms	116 μs	multi-dim. D+C (cmplt. + collect. comm.)
		Encore Multimax	16	512	521 ms	31.8 μs	multi-dim. D+C (partitioned input)
1993	Embrechts, Roose, and Wambacq [13]	Intel iPSC/2	16	256	360 ms	87.9 μs	divide & conquer
1994	Choudhary and Thakur [8]	TMC CM-5	32	512	456 ms	55.7 μs	multi-dim. D+C (partitioned input)
	(DARPA II Image)	TMC CM-5	32	512	398 ms	48.6 μs	multi-dim. D+C (complete im./PE)
		TMC CM-5	32	512	452 ms	55.2 μs	multi-dim. D+C (cmplt. + collect. comm.)
1994	Ziavras and Meer [49]	TMC CM-2	16384	128	35.4 s	1.11 s	
1994	Bader and JáJá	TMC CM-5	32	512	368 ms	44.9 μs	DARPA II Image
		TMC CM-5	32	512	292 ms	35.6 μs	mean of test images
	(This paper)	TMC CM-5	32	1024	852 ms	26.0 μs	mean of test images
		IBM SP-1	4	512	370 ms	5.65 μs	DARPA II Image
		IBM SP-1	32	512	412 ms	50.3 μs	mean of test images
		IBM SP-1	32	1024	863 ms	26.3 μs	mean of test images
		IBM SP-2	4	512	243 ms	3.71 μs	DARPA II Image
		IBM SP-2	32	512	284 ms	34.7 μs	mean of test images
		IBM SP-2	32	1024	585 ms	17.9 μs	mean of test images
		Meiko CS-2	2	512	809 ms	6.17 μs	DARPA II Image
		Meiko CS-2	32	512	301 ms	36.7 μs	DARPA II Image

Table 2: Implementation Results of Parallel Connected Components of Images Algorithms

2 Block Distributed Memory Model

We use the Block Distributed Memory (BDM) Model ([21], [22]) as a computation model for developing and analyzing our parallel algorithms on distributed memory machines. This model allows the design of algorithms using a single address space and does not assume any particular interconnection topology. The model captures performance by incorporating a cost measure for interprocessor communication induced by remote memory accesses. The cost measure includes parameters reflecting memory latency, communication bandwidth, and spatial locality. This model allows the initial placement of data and prefetching.

The complexity of parallel algorithms will be evaluated in terms of two measures: the computation time $T_{comp}(n,p)$, and the communication time $T_{comm}(n,p)$. The measure $T_{comp}(n,p)$ refers to the maximum of the local computations performed on any processor as measured on the standard sequential RAM model. The communication time $T_{comm}(n,p)$ refers to the total amount of communications time spent by the overall algorithm in accessing remote data. Using the BDM model, an access operation to a remote location takes $\tau + 1$ time, and l prefetch read operations can be executed in $\tau + l$ time, where τ is the normalized maximum latency of any message sent in the communications network. No processor can send or receive more than one word at a time.

Two useful data movement patterns, matrix transposition and broadcasting, are discussed next, and their analyses will be included as primitives in the algorithms that follow.

Given a $q \times p$ matrix on a p processor machine, where p divides q, the matrix transposition consists of rearranging the data such that the first $\frac{q}{p}$ rows of elements are destined to the first processor, the second $\frac{q}{p}$ rows to the second processor, and so on, with the last $\frac{q}{p}$ rows of the matrix destined to the last processor. An efficient matrix transposition algorithm consists of p iterations such that, during iteration i, each processor P_t prefetches the appropriate block of $\frac{q}{p}$ elements from processor $P_{(t+i) \bmod p}$.

Next, an efficient BDM algorithm is given which takes q elements on a single processor and broadcasts them to the other $p-1$ processors using just two matrix transpositions.

Performance analysis given will reflect the execution times from implementations on the CM-5, SP-2, and CS-2, each with $p = 32$ parallel processing nodes. The algorithms are written in SPLIT-C, a parallel extension of the C programming language, primarily intended for distributed memory multiprocessors. SPLIT-C can express the capabilities of the BMD model and provides a shared global address space, constructs to express data layout, and **split-phase** assignments. The **split-phase** assignment operator, :=, prefetches data from the specified remote location into local memory. Computation can be overlapped with the remote request, and the **sync()** function allows each processor to stall until all data prefetching is complete. The SPLIT-C language also supplies a **barrier()** function for the global synchronization of the processors.

2.1 Analysis For Matrix Transpose Algorithm

The analysis for the matrix transpose algorithm is similar to that of the LogP model analysis [11]. The algorithm to perform a $q \times p$ matrix transpose on a p processor machine operates as follows. The data layout of matrix A is straightforward; each column i of q elements is stored on processor i, for $i \in \{0, \ldots, p-1\}$. Note that the first index of A contains the processor number, while the second index provides the element offset in that processor.

Processor i runs the following program:

Algorithm 1 *Matrix Transposition*

Block Distributed Memory Model Algorithm.

Input:

{ i } is my processor number;

{ p } is the total number of processors, labeled from 0 to $p-1$;

{ A } is the $q \times p$ input matrix.

begin

1. **For** loop = 0 **to** $p-1$ **do**:
   1.1 **Set** r = (i + loop) **mod** p;
   1.2 **Prefetch** $A^T[i]\left[(r*\frac{q}{p})\ldots\left((r+1)*\frac{q}{p}\right)-1\right] :=$
   $A[r]\left[(i*\frac{q}{p})\ldots\left((i+1)*\frac{q}{p}\right)-1\right]$;
2. **Sync()**

end

Each prefetch in Step 1.2 requests a block of $\frac{q}{p}$ elements. Since each processor prefetches $p-1$ blocks of $\frac{q}{p}$ each, this matrix transpose algorithm will take $\tau + (p-1)\frac{q}{p}$ communication complexity, or

$$\begin{cases} T_{comm}(n,p) & = \tau + \left(q - \frac{q}{p}\right); \\ T_{comp}(n,p) & = \mathrm{O}(q). \end{cases} \tag{1}$$

2.2 Experimental Results for Matrix Transpose

Performance graphs for matrix transposition execution times using Split-C on a 32 processor CM-5, SP-2, CS-2, and 8 processor Paragon are given in Figures 6, 7, 8, and 9, respectively, in Appendix A.1. These figures also show the attained data bandwidth[1] per processor for the transpose algorithm. For large enough data sets on the CM-5, we achieve an average bandwidth of 7.62 MB/s per processor, which is more than three-fourths of the maximum user-payload bandwidth per processor of 12 MB/s per processor [28]. This is consistent with the results achieved by other research teams that have achieved 6.4 MB/s per processor (Culler at UC Berkley, [11]), and 7.72 MB/s per processor (Ranka at Syracuse University, [46]) for similar data movements on the CM-5. Note that some of these cited results are for low-level implementations using message passing algorithms. For large enough data sets, the SP-2 achieves greater than 24.8 MB/s per processor for the matrix transpose algorithm, using a high performance switch hardware rated by the vendor as having a peak node to node bandwidth of 40 MB/s [27]. The Meiko CS-2 achieves greater than 10.7 MB/s per processor. Note that the CS-2 result is much less than the maximum attainable bandwidth of 50 MB/s per processor [33] because our Split-C version has not been fully optimized to make use of the architecture's communications coprocessor. The 8 processor Paragon achieves greater than 88.6 MB/s per processor, with the maximum hardware bandwidth given by Intel as 175 MB/s per processor and application peak bandwidth as 135 MB/s per processor [30].

2.3 Analysis for the Broadcasting Algorithm

An efficient algorithm to broadcast q elements from a single processor to p processors is based on matrix transposition, where q is assumed to be larger than p. Processor 0 holds the q elements to be broadcast in the first column of matrix A. We compute the matrix transpose of A, thus, giving every processor $\frac{q}{p}$ elements. Each processor then locally rearranges the data so that an additional matrix transpose will result in each processor holding a copy of all the q elements in its column of A [21].

The following algorithm runs on processor i:

Algorithm 2 *Broadcast Algorithm*

Block Distributed Memory Model Algorithm to broadcast q elements from a single processor to all other processors.

Input:
{ i } is my processor number;
{ p } is the total number of processors, labeled from 0 to $p-1$;
{ A } is the $q \times p$ input matrix, with only the 0^{th} column as valid data.

begin

[1] Note that throughout this paper, the rate of "MB/s" will always represent 10^6 bytes per second.

1. **For** loop $= 0$ **to** $p-1$ **do**:
   1.1 **Set** r = $(i$ + loop) **mod** p;
   1.2 **Prefetch** $A^T[i]\left[(r*\frac{q}{p})\ldots\left((r+1)*\frac{q}{p}\right)-1\right] :=$
   $A[r]\left[(i*\frac{q}{p})\ldots\left((i+1)*\frac{q}{p}\right)-1\right]$;
2. **Sync()**
3. **For** loop $= 0$ **to** $p-1$ **do**:
   3.1 **Set** r = $(i$ + loop) **mod** p;
   3.2 **Prefetch** $A[i]\left[(r*\frac{q}{p})\ldots\left((r+1)*\frac{q}{p}\right)-1\right] :=$
   $A^T[r]\left[0\ldots\frac{q}{p}-1\right]$;
4. **Sync()**

end

Notice that at the end of Step 2, only the first $\frac{q}{p}$ elements in each column are valid. Because of this, we specialize the matrix transpose in Step 3 to prefetch only this first slot from every other processor.

The analysis of this broadcasting algorithm is simple. Since this algorithm just performs two matrix transpositions, the complexities of the broadcasting algorithm are

$$\begin{cases} T_{comm}(n,p) & = & 2\left(\tau + \left(q - \frac{q}{p}\right)\right); \\ T_{comp}(n,p) & = & O(q). \end{cases} \tag{2}$$

2.4 Experimental Results for Broadcasting

The performance graphs for broadcasting using the prefetching matrix transposition on a 32 processor CM-5, SP-2, and CS-2, and 8 processor Paragon are given in Figures 6, 7, 8 and 9, respectively, in Appendix A.1. As expected, these graphs show that the Split-C broadcasting algorithm takes roughly twice the time of the Split-C matrix transpose algorithm. In addition, these figures show the attained data bandwidth per processor for this broadcast algorithm. As expected, we achieve approximately the same results as that of the transpose algorithm on both machines.

3 Image (Data) Layout and Test Images

A straightforward data layout is used in these algorithms for all platforms. The input image is an $n \times n$ matrix of integers. We assign tiles of the image as equally as possible among the processors. If p is an even power of two, i.e. $p = 2^d$, for even d, the processors will be arranged in a $\sqrt{p} \times \sqrt{p}$ logical grid. For future reference, we will denote the number of rows in this logical grid as v and the number of columns as w. For odd d, we assign the number of rows of the logical processor grid to be $v = 2^{\lfloor \frac{d}{2} \rfloor}$, and the number of columns to be $w = 2^{\lceil \frac{d}{2} \rceil}$. Each processor initially owns a tile of size $\frac{n}{v} \times \frac{n}{w}$. For future reference, we assign $q = \frac{n}{v}$ and $r = \frac{n}{w}$. We assume that the p processors are labeled consecutively from 0 to $p-1$ and are assigned in row-major order to the logical processor grid just described.

Several test images have been used to test the correctness and the performance of the algorithms presented here. These test images, shown in Figure 1, are generated at runtime, with images 1-4, 7, and 9, augmented to the needed image size, while images 5, 6, and 8, scaled appropriately. Figure 2 is a 512×512, 256 grey-level, image from the Second DARPA Image Understanding Benchmark [47]. The histogramming algorithm is assumed to be correct because $\sum_{i=0}^{k-1} H[i] = n^2$, and for regular patterns, it is easy to verify that each $H[i]/n^2$ equals the percentage of area that grey level i covers in the image. Verifying the connected components algorithm is more difficult. In addition to the DARPA Benchmark Image, we include the most widely used patterns for binary images. A catalog of nine automatically generated scalable images is used, as shown in Figure 1, and include horizontal, vertical, and forward- and back-slanting diagonal bars, a cross, a filled disc, concentric circles with thickness, four squares inset from the four corners, and a dual-spiral pattern, a "difficult" image [42].

3.1 Connected Components Test Images

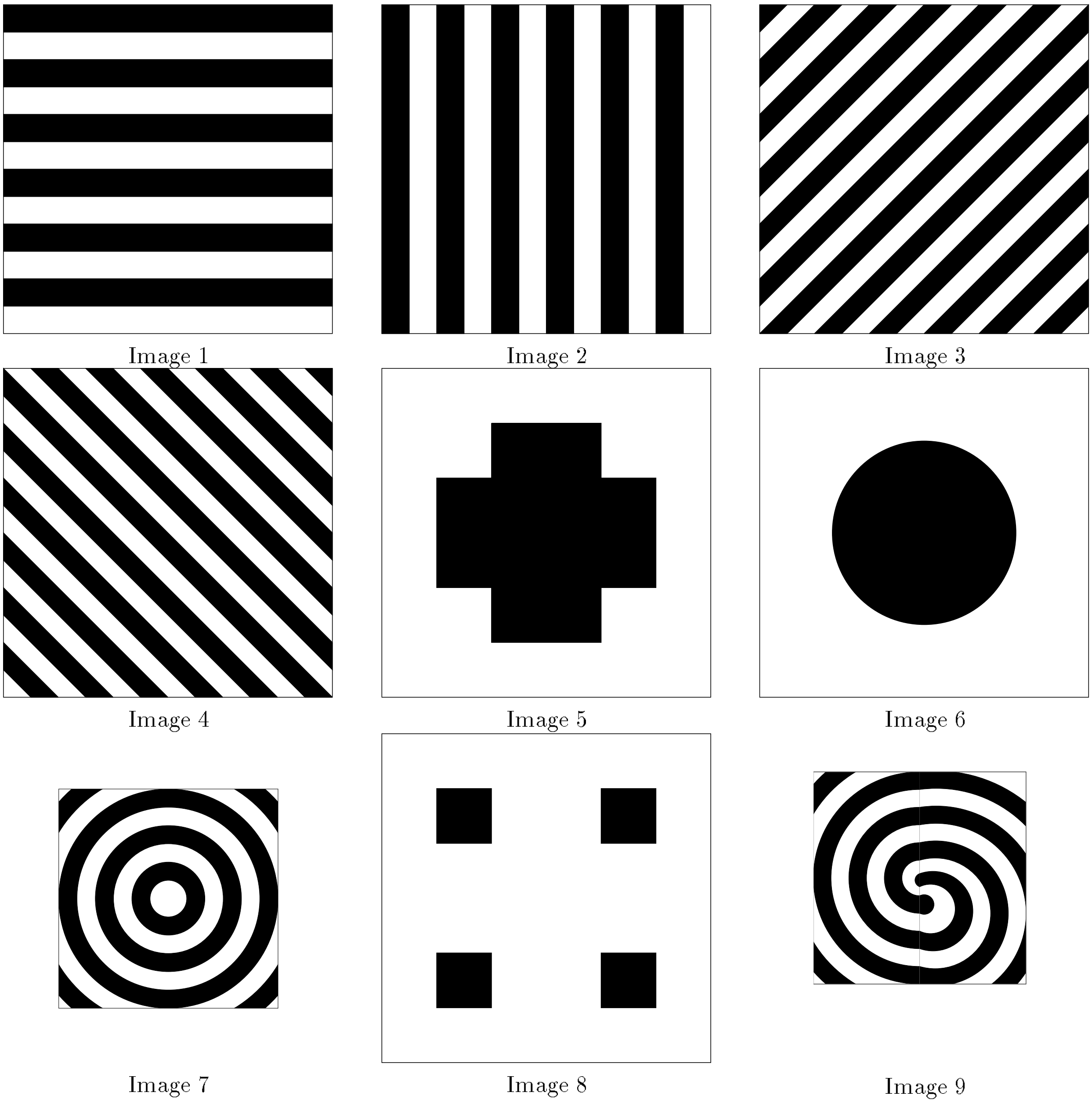


Figure 1: Binary Test Images

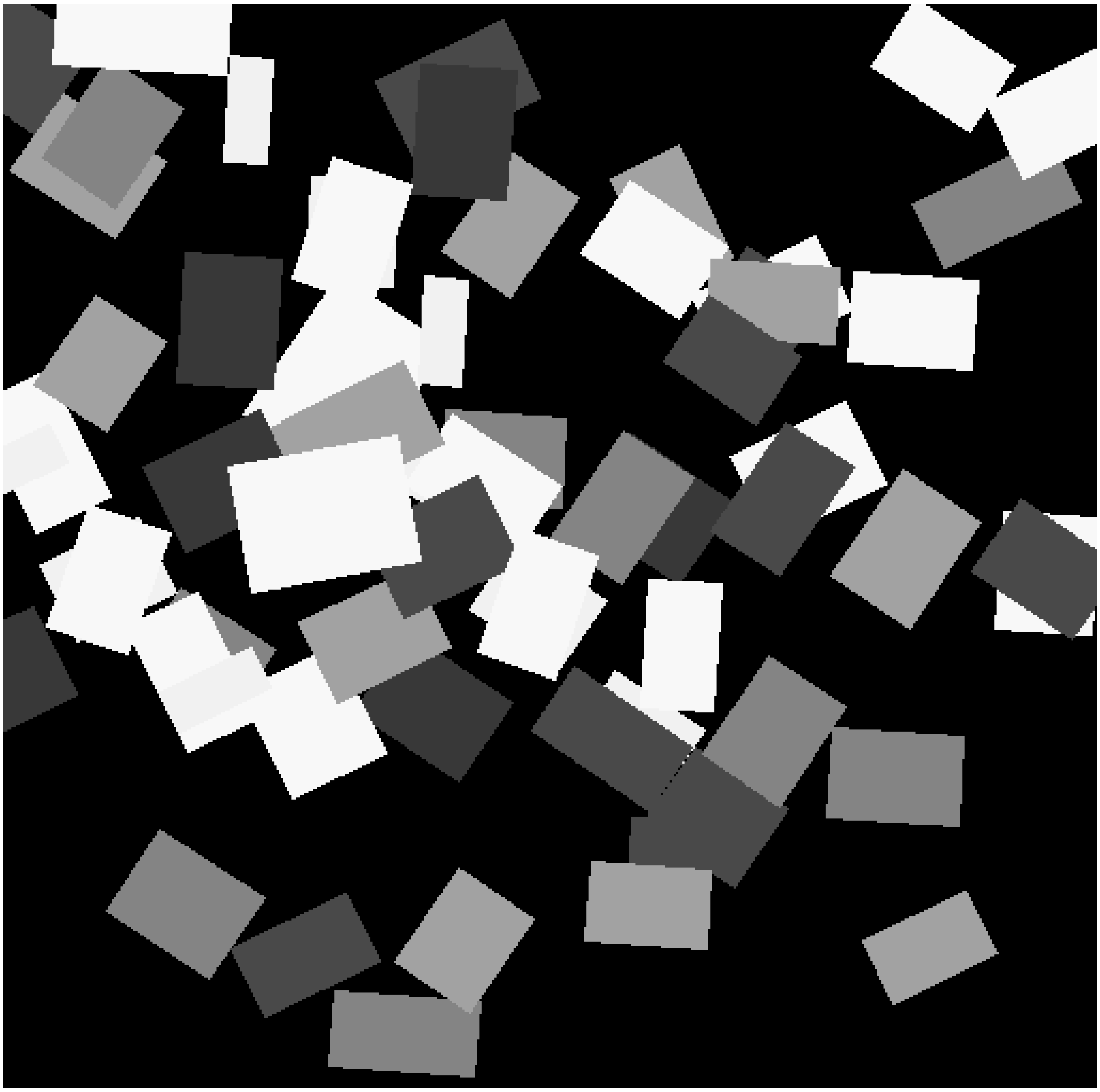


Figure 2: DARPA Image Understanding Benchmark Test Image

4 Histogramming

Histogramming is a useful image processing primitive. One application is histogram normalization (or equalization), a technique that flattens the histogram and, thus, improves the contrast of an image by "spreading out" colors which might be too clumped together for human visual distinction.

Let k be the number of grey levels in the $n \times n$ input image X, and without loss of generality, k is assumed to be a power of two. Note that this implies that for $k \geq p$, the value of $\frac{k}{p}$ is an integer ≥ 1. Our histogramming algorithm is quite simple. The first step consists of creating an array $H_i[0..k-1]$ on every processor i, such that each processor tallies the number of grey levels in its own $\frac{n}{v} \times \frac{n}{w} = \frac{n^2}{p}$ subimage into its array $H_i[\star]$. The purpose of the next step is to rearrange the data so that the tallies of each grey level reside on the same processor. If $k < p$ we use a truncated transpose to put each row into a processor, P_i, $0 \leq i \leq k-1$. If $k \geq p$ we transpose $\frac{k}{p}$ rows of the local histograms into each processor, such that each processor, P_i, has all the intermediate sums needed to compute $H\left[i\frac{k}{p}\right]$ through $H\left[(i+1)\frac{k}{p}-1\right]$. The routing step is followed by local computations of the histogram which can be done in $\mathrm{O}(k)$ operations. Next, one processor, P_0, prefetches the results by doing a circular data movement, as described in Section 2, and outputs the k-bar histogram of the image.

The communication complexity can be estimated as follows. Two main communication steps are used in our algorithm. The first is a matrix transpose of the $k \times p$ histogram array and takes $T_{comm}(n,p) = \tau + \left(k - \max\left(\frac{k}{p}, 1\right)\right)$. The second communication collects the histogram bars on a single processor and takes $T_{comm}(n,p) \leq \tau + \left(k - \max\left(\frac{k}{p}, 1\right)\right)$. Thus, the histogramming algorithm has the following complexities:

$$\left\{ \begin{array}{lcl} T_{comm}(n,p) & \leq & 2\,(\tau + k)\,; \\ T_{comp}(n,p) & = & \mathrm{O}\left(\frac{n^2}{p} + k\right). \end{array} \right. \tag{3}$$

4.1 Experimental Results for Histogramming

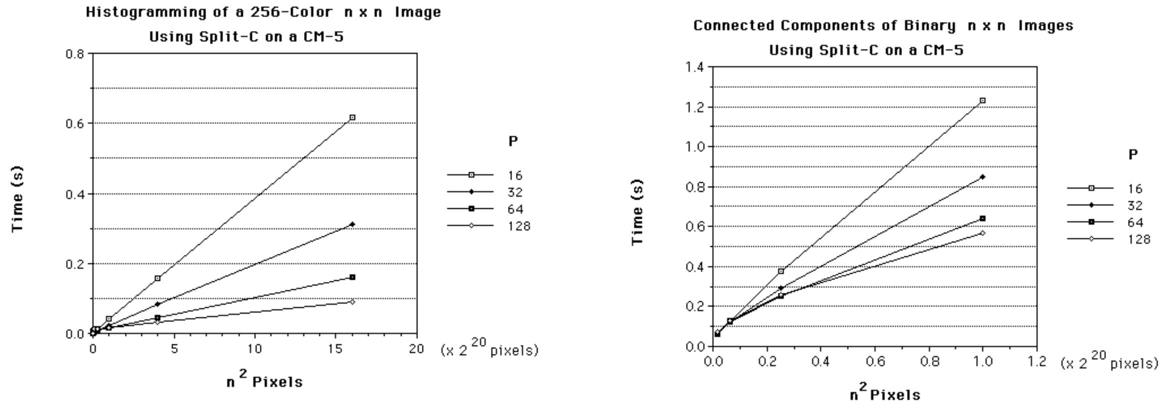
The above analysis indicates that, for fixed p and k, the communication complexity is independent of the problem size. Hence, as n increases, we expect the local computation to dominate.

The histogramming algorithm has been implemented on a CM-5 with p = 16, 32, 64, and 128 processors, and the algorithm's performance is plotted in Figure 3 for 256 grey levels for images ranging from 32×32 to 4096×4096 pixels in size, and expanded in Figures 12 - 14 for 128×128 to 1024×1024 images on 16, 32, and 64 processors. Corresponding performance graphs are given for the IBM SP-1 in Figure 18 and for the IBM SP-2 in Figure 20. Plots indicate quadratic performance as a function of n for fixed p, and scalability in terms of p. Hence, our theoretical analysis is supported.

Please refer to the plot in Figure 3 for an illustration of the scalability of the histogramming algorithm's performance. Since computation dominates for large n, the algorithm runs as $\mathrm{O}\left(\frac{n^2}{p}\right)$. We have plotted n^2 vs. time for four configurations of the CM-5. The resulting plot shows the linear relationship between time and image size for each fixed p. Also, when the number of processors double, the running time approximately halves.

5 Connected Components of Binary Images

The high-level strategy of our connected components algorithm uses the well-known divide and conquer technique. Divide and conquer algorithms typically use a recursive strategy to split problems into smaller subproblems, and, given the solutions to these subproblems, merge the results into the final solution. It is common to have either an easy splitting algorithm and a more complicated merging, or vice versa, a hard splitting, following by easy merging. In our



Histogramming Algorithm Performance Graph for $k <= 256$

Connected Components for Binary $n \times n$ Images

Figure 3: Histogramming and Connected Components Scalability on the CM-5

parallel connected components algorithm, the splitting phase is trivial and implicit, while the merging process requires more work.

Each processor holds a unique tile of the image, and hence can find the initial connected components of its tile by using a standard sequential algorithm based upon breadth-first search. Next, the algorithm iterates $\log p$ times[2], alternating between combining the tiles in **horizontal merges** of vertical borders and **vertical merges** of horizontal borders, with the number of horizontal merges equal to $\log w$ and the number of vertical merges equal to $\log v$, since $\log p = \log(v * w) = \log v + \log w$. Our algorithm uses novel techniques to perform the merges and to update the labels. We start by describing the initial sequential connected components algorithm.

5.1 Initialization and Sequential Connected Components

The initialization consists of entirely local operations on each processor. Pixels on each tile are examined in row-major order fashion. If a pixel is an unmarked, colored pixel, a breadth-first search procedure starting at that pixel labels all connected like-colored pixels within that tile with a globally unique label. When a pixel is visited in the labeling procedure, it becomes marked. During the initial row-major order search, for 8-connectivity, only the four pixels to the right, below-left, below, and below-right, need to be examined for connectivity. For 4-connectivity, only the pixels to the right and below need to be examined. This sequential connected components algorithm runs in $\mathrm{O}(|V| + |E|)$ where $|V|$ is the number of vertices, and $|E|$ is the number of edges searched. Since $|E| \le 8|V|$, this algorithm runs in $\mathrm{O}(|V|) = \mathrm{O}\left(\frac{n^2}{p}\right)$ time. The result is an array of positive integers corresponding to the unique label values of the connected components in the subimage.

The initial labeling of each pixel with local offset (i, j) in the processor with logical grid position (I, J) will be $(Iq + i)n + (Jr + j) + 1$. This labeling ensures that each processor will obtain unique labelings across the subimages after running the sequential connected components step, without having to do any communication among the processors. Thus, the initialization step runs in

$$T_{comp}(n, p) \ = \mathrm{O}\left(\frac{n^2}{p}\right). \tag{4}$$

5.2 Merging Algorithm - Overview

Now we are ready to begin the merging phase. As mentioned above, we merge the p subimages into larger and larger image sections with consistent labelings. There will be $\log p$ iterations

[2] Note that throughout this paper "log x" will always be the logarithm of x to the base $b = 2$, i.e. $\log_2 x$.

since we cut the number of uncombined subimages in half during each iteration. Unlike previous connected components algorithms, we use a technique which identifies processors as **group managers** or **clients** during each phase. The group managers have the task of organizing the retrieval of boundary data, performing the merge, and creating the list of label changes. Once the group managers broadcast these changes to their respective clients, all processors must use the information to update their **tile hooks**, data structures which point to connected components on local tile borders. See Figure 5 for an illustration of the **tile hook** data structure in which three tile hooks contain the information needed to update the border pixels. The clients assist the group managers by participating in the coalescing of data during each merge phase. Finally, the complete relabeling is performed at the very end using information from the tile hooks.

Without loss of generality, we first perform a horizontal merge along every other vertical border, then a vertical merge along every other horizontal border, alternating orientation until we have merged all the tiles into one consistent labeling. We merge vertical borders exactly $\log w$ times, where w is the number of columns in the logical processor grid. Similarly, we merge horizontal borders exactly $\log v$ times, where v is the number of rows in the logical processor grid.

The merging algorithm for a horizontal merge is similar to that of a vertical merge. Most of the code is identical, except for substituting "up" for "left" and "down" for "right." However, one nontrivial change relates to identifying during each iteration which processors will be **group managers** and which will be **clients**, concepts defined precisely in the following section.

5.3 Merging Algorithm - Group Managers' Task

We perform $\log p$ merge iterations, alternating between horizontal and vertical merge phases. For each odd merge iteration t, $1 \le t \le \log p$, we will perform the $\left(\frac{t+1}{2}\right)^{\text{th}}$ horizontal merge phase, and similarly, for each even merge iteration t, $1 < t \le \log p$, we will perform the $\left(\frac{t}{2}\right)^{\text{th}}$ vertical merge phase.

Let t represent the current merge phase iteration, with $1 \le t \le \log p$. Thus, there will be $\log w$ and $\log v$ horizontal and vertical merge phases, respectively.

During each merge, a subset of the processors will act as **group managers**. These designated processors will prefetch the necessary border information along the column (or row) that they are located upon in the logical processor grid, setting up an equivalent graph problem, running a sequential connected components algorithm on the graph, noting any changes in the labels, and storing these changes ((α_i, β_i) pairs) in a shared structure. The **clients** decide who their current group manager is and wait until the list of label changes is ready. They retrieve the list, and all processors make the necessary updates to a proper subset of their labels.

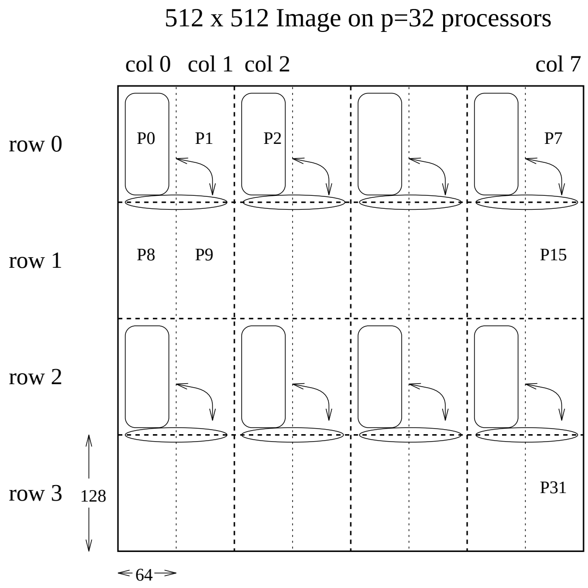
During odd merge iterations t, the horizontal merge phases, processors are **group managers** if they reside in the logical grid with both

- row numbers whose binary representation end with a 0 followed by $(\frac{t+1}{2} - 1)$ 1's (or just ending in a 0 when $t = 1$), and
- column numbers whose binary representation end in $\frac{t+1}{2}$ 0's.

Similarly, during the even merge iterations t, the vertical merge phases, processors are **group managers** if they reside in the logical grid with both

- row numbers whose binary representation end in $\frac{t}{2}$ 0's, and
- column numbers whose binary representation end with a 0 followed by $(\frac{t}{2} - 1)$ 1's (or just ending in a 0 when $t = 2$).

An example data layout and merge is given in Figure 4. This image is 512×512, distributed onto a 4×8 logical processor grid, with each tile being 128×64 pixels in size. This example shows the second merge step, a vertical merge, for $t = 2$. Group managers are, thus, any processor sitting in the logical processor grid with both last bits of the row and column numbers' binary representation equal to '0'. These group managers, along with their respective borders to be



Merge Phase 2: circled processors are group managers. (Vertical Merge)

Dotted borders were merged in Phase 1.

Circled borders will be merged in Phase 2.

Figure 4: Data Layout of a 512 x 512 Image on 32 Processors - Vertical Merge (t=2)

merged, are circled in this figure. Suppose now that $p \geq 128$, and we are at the $t = 7^{\text{th}}$ merge phase, which will be a horizontal merge. A processor in this case is a group manager if it is in a logical grid position whose row number's binary representation ends with 0111, and whose column number's binary representation ends with 0000.

For a horizontal merge, the group manager will prefetch the pixel colors and labels from the vertical borders to be merged, which spans across $2^{\frac{t+1}{2}}$ rows of processors. There are $2q$ $(= \frac{2n}{\sqrt{p}})$ pixels per processor row in the border to be merged, meaning that $2q2^{\frac{t+1}{2}} - q$ pixels and an equal number of labels need to be prefetched from the clients, while q pixels and q labels are locally available. Thus, each prefetch in the horizontal merge can be done in $T_{comm}(n,p) \;\leq \tau + 4q2^{\frac{t+1}{2}}$ and $T_{comp}(n,p) \;= \mathrm{O}\left(\frac{n}{\sqrt{p}} 2^{\frac{t+1}{2}}\right)$.

Similarly for a vertical merge, the group manager will prefetch the pixel colors and labels from the horizontal borders to be merged, which spans across $2^{\frac{t}{2}}$ columns of processors. There are $2r$ pixels per processor column in the border to be merged, meaning that $2r2^{\frac{t}{2}} - r$ pixels and an equal number of labels need to be prefetched from the clients for each iteration, while r pixels and r labels are locally available. Thus, each prefetch in the vertical merge can be done in $T_{comm}(n,p) \;\leq \tau + 4r2^{\frac{t}{2}}$ and $T_{comp}(n,p) \;= \mathrm{O}\left(\frac{n}{\sqrt{p}} 2^{\frac{t}{2}}\right)$.

Note that the running time of this prefetching is improved by using a second processor, called a **shadow** manager, which is designated as the processor adjacent to the group manager, directly across the border being merged. Using this implementation, both the group and shadow manager prefetch only their side of the border, respectively, and sort each border by label. The reasons for this sorting will be described below. The group manager then prefetches the sorted results from the shadow manager and continues on with the algorithm. From this point on, the shadow manager reverts back to being a client of this group manager.

The total complexities for prefetching summed up over the $\log w$ horizontal merges and the

$\log v$ vertical merges are

$$\begin{cases} T_{comm}(n,p) & \leq & \sum_{\rho=1}^{\log v}(\tau + 4q2^{\rho}) + \sum_{\kappa=1}^{\log w}(\tau + 4r2^{\kappa}) \\ & \leq & \tau \log p + 4q(v-1) + 4r(w-1) \\ & \leq & \tau \log p + 8n; \\ T_{comp}(n,p) & = & \mathrm{O}\left(\sum_{\rho=1}^{\log v}(4q2^{\rho}) + \sum_{\kappa=1}^{\log w}(4r2^{\kappa})\right) \\ & = & \mathrm{O}(qv + rw) \\ & = & \mathrm{O}(n). \end{cases} \tag{5}$$

The merging problem is converted into finding the connected components of a graph represented by the border pixels. We use an adjacency list representation for the graph, and add vertices to the graph representing colored pixels. Two types of edges are added to the graph. First, pixels are scanned down the left (or upper) border, and edges are strung linearly down the list between pixels containing the same connected component label. The same is done for pixels on the right (or lower) border. The second step adds edges between pixels of the left (upper) and right (lower) border which are both like-colored pixels and adjacent to each other. We scan down the left column (upper row) elements, and if we are at a colored pixel, we check the pixels in the right column (lower row) adjacent to it. In order to add the first type of edges, the pixels are sorted according to their label for both the left (upper) and right (lower) border by using radix sort[3]. Note the discussion above regarding the use of a shadow manager. A secondary processor is used to prefetch and sort the border elements on the opposite side of the border from the group manager, and the results are then sent to the group manager. This sort takes $T_{comp}(n,p) = \mathrm{O}(|V|)$ steps for a border of $|V|$ nodes[4]. The maximum number of edges attached to each vertex in this graph is at most five; two edges in its own column to pixels above and below of the same label plus the three adjacent pixels in the right column. Thus, inserting an edge into the adjacency list takes at most five steps, and we add at most $5|V|$ edges. For each horizontal merge step, the number of vertices $|V| \leq 2q2^{\frac{t+1}{2}}$, and for each vertical merge step, $|V| \leq 2r2^{\frac{t}{2}}$. Thus, the construction of this graph summed over all the iterations of the connected components algorithm takes

$$\begin{cases} T_{comp}(n,p) & = & \mathrm{O}\left(\sum_{\rho=1}^{\log v}(2q2^{\rho}) + \sum_{\kappa=1}^{\log w}(2r2^{\kappa})\right) \\ & = & \mathrm{O}(qv + rw) \\ & = & \mathrm{O}(n). \end{cases} \tag{6}$$

A sequential breadth-first search based connected components algorithm computes the connected components of this graph. It runs in $\mathrm{O}(|V| + |E|)$ steps, with $|V|, |E| = \mathrm{O}\left(q2^{\frac{t+1}{2}}\right)$ for horizontal merges and $\mathrm{O}\left(r2^{\frac{t}{2}}\right)$ for vertical merges. The pixels in this graph are then scanned again, and any changes in the labeling (α changing to label β) are eventually stored in a sorted array of all unique changes (α_i, β_i). The following algorithm describes the procedure for creating the sorted array of label changes from the original arrays.

Procedure 1 *Create_Change_Array*

Generate a sorted array of label change pairs.

begin

1. Copy all label pairs, (α, β), where label α has changed to label β, into a contiguous array.
2. Radix sort this array, using α as the sorting index.
3. Scan down the sorted array, copying all unique (α, β) pairs into a new array.

end

---

[3] Note that whenever radix sort is mentioned in this paper, the actual coding uses the standard **UNIX** quicker-sort function for smaller sorts, and radix sort for larger sorts, using whichever sorting method is fastest for the given input size.

[4] Our radix sort uses four passes; each pass will sort on one byte of the 32-bit key by using 256 buckets.

There are at most $2|V|$ changes, so Steps 1, 2, and 3 take $O(|V|)$ time. Thus, the creation of the sorted array of label changes takes $O(|V|)$ time. Summing over the $\log p$ steps, this is equivalent to $T_{comp}(n,p) = O\left(\sum_{\rho=1}^{\log v}(2q2^{\rho}) + \sum_{\kappa=1}^{\log w}(2r2^{\kappa})\right) = O(n)$.

The array structure is actually two contiguous arrays, one holding the obsolete labels (α's) and the other holding the corresponding new labels (β's). The size of these arrays of α's and β's is also placed into a shared memory location.

Now all the processors hit a barrier and wait until everyone has completed their tasks. After the barrier, the group manager will update its pixels' labels in $O\left(\frac{n^2}{p}\right)$ by the following procedure.

After the initial tile labelings, but before the merging iterations, each processor creates a sorted array of **hooks** to each local component containing a border pixel of the tile. There will be exactly one hook for each of these components, including the initial label of that component and the offset address in the tile of any pixel in that component. This is done as follows:

Procedure 2 *Create_Tile_Hooks*

Generate a sorted array of hooks to each component on a tile touching a boundary pixel.

begin

1. For each colored pixel on the tile border with offset position (i,j)
   1.1 Place $(label[(i,j)], (i,j))$ at the next position of an array.
2. Radix sort this array, using *label* as the sorting index.
3. Scan down the sorted array, copying all unique $(label[(i,j)], (i,j))$ pairs into a new array.

end

This initialization takes computational complexity of $O\left(\frac{n}{\sqrt{p}}\right)$ for each of Steps 1, 2, and 3, yielding a total of $T_{comp}(n,p) = O\left(\frac{n}{\sqrt{p}}\right)$.

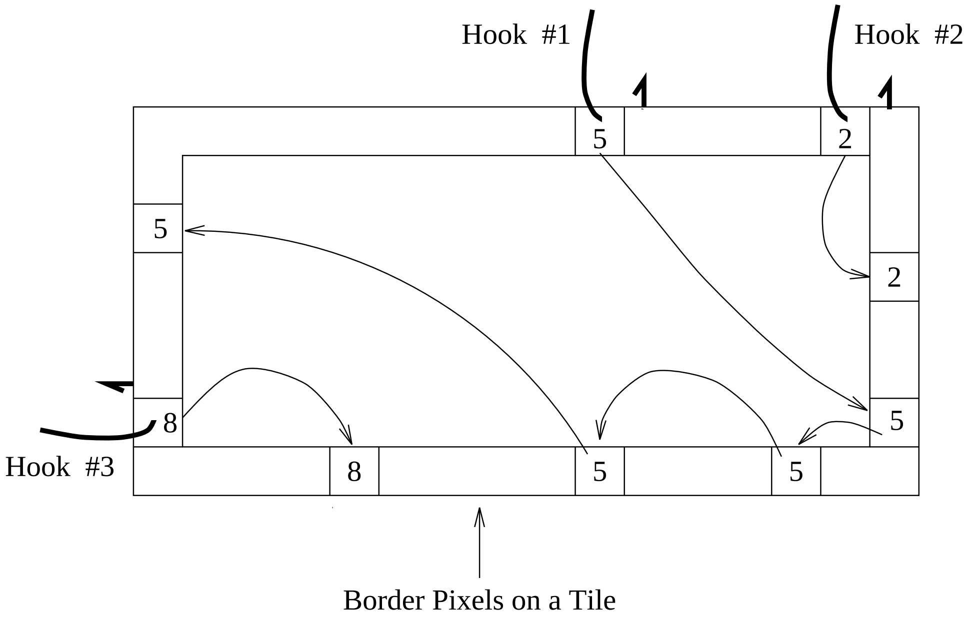


Figure 5: An example of Tile Hooks

At the conclusion of each of the $\log p$ merging steps, only the labels of pixels on the border of each tile are updated. There is no need to relabel interior pixels since they are not used in the merging stage. Only boundary pixels need their labels updated. The procedure is simple; for each colored pixel on the boundary, we will binary search the list of label changes in $T_{comp}(n,p) = O\left(\frac{n}{\sqrt{p}}\log|V|\right)$ per step. The total computational complexity over the $\log p$ merging iterations is then $O\left(\sum_{\rho=1}^{\log v}\left[\frac{n}{\sqrt{p}}\log(2q2^{\rho})\right] + \sum_{\kappa=1}^{\log w}\left[\frac{n}{\sqrt{p}}\log(2r2^{\kappa})\right]\right) = O\left(\frac{n}{\sqrt{p}}\log n \log p\right)$.

At the end of the last merging step, each processor must update its interior pixel labels. Each hook described above is compared to the current label at the hook's offset position index. If the hook's label *label*[i] is different from the current label at position i, the processor will run a breadth-first search relabeling technique beginning at pixel i, relabeling all the connected pixels' labels to the new label. Since there is only one hook per tile component on the border, the breadth-first search relabeling procedure takes $O\left(\frac{n^2}{p}\right)$ time.

The total complexity associated with updating the labels of each tile is $T_{comp}(n,p) = O\left(\frac{n}{\sqrt{p}} \log \frac{n}{\sqrt{p}} + \frac{n}{\sqrt{p}} \log n \log p + \frac{n^2}{p}\right) = O\left(\frac{n^2}{p}\right)$ assuming $p \le n$ for large enough n. For $n \ge 128$, $p \le \frac{n}{8}$ is sufficient.

After each merging step label update, the manager hits another barrier, waiting for the end of this iteration.

In summary, the group managers' routine has the following complexities:

$$\begin{cases} T_{comm}(n,p) & \le & \tau \log p + 8n; \\ T_{comp}(n,p) & = & O\left(\frac{n^2}{p} + n\right). \end{cases} \tag{7}$$

5.4 Merging algorithm - clients' task

The client processors are any processor not selected in the current iteration to run the group manager tasks. These processors calculate the logical processor grid address of the manager in charge of their border to be merged and wait for the first barrier. After this barrier, the clients prefetch the size (*chSize*) of the list of change pairs from the manager in $T_{comm}(n,p) \le \tau + 2^t$, where $\frac{t+1}{2}$ and $\frac{t}{2}$ are the number of vertical and horizontal merges, respectively, performed inclusively during the t^{th} merge phase.

Next, the clients prefetch a block of *chSize* (α, β) change pairs from the manager. This is done in $T_{comm}(n,p) \le \tau + 2\,(2^t)\,2q2^{\frac{t+1}{2}}$ for horizontal merges, and $T_{comm}(n,p) \le \tau + 2\,(2^t)\,2r2^{\frac{t}{2}}$ for vertical merges, since there are at most $2q2^{\frac{t+1}{2}}$ (or $2r2^{\frac{t}{2}}$) changes, and exactly $(2^t - 1)$ processors requesting these change pairs from each group manager. The client processors use the same procedure described in the previous section for relabeling their border pixels at the end of each merge iteration, and the interior pixels after the final merge. After each pixel label update, the clients hit another barrier, and wait for the end of this iteration.

Over the $\log p$ iterations, the clients' routine has the following complexities:

$$\begin{cases} T_{comm}(n,p) & \le & & \sum_{l=1}^{\log p}\left[\tau + 2^l\right] + \sum_{\rho=1}^{\log v}\left[\tau + 2\left(2^{2\rho}\right)2q2^{\rho}\right] + \\ & & & \sum_{\kappa=1}^{\log w}\left[\tau + 2\left(2^{2\kappa-1}\right)2r2^{\kappa}\right] \\ & \le & & (2\log p)\tau + 14np + 2p; \\ T_{comp}(n,p) & = & O(& \sum_{l=1}^{\log p} 2^l + \sum_{\rho=1}^{\log v}\left[2\left(2^{2\rho}\right)2q2^{\rho}\right] + \\ & & & \sum_{\kappa=1}^{\log w}\left[2\left(2^{2\kappa-1}\right)2r2^{\kappa}\right]\ ) + \\ & & & O\left(\frac{n^2}{p}\right) \\ & = & O(& np\ ) + O\left(\frac{n^2}{p}\right) \\ & = & O(& \frac{n^2}{p} + np\ ). \end{cases} \tag{8}$$

Clearly, for large p, this is not an optimal procedure for distributing the list of change pairs from a group manager to the respective clients. If a manager has $f(i) - 1$ clients at the end of iteration i, $0 \le i < \log p$, instead of sending the entire list of $c(i)$ change pairs to $f(i) - 1$ processors, a distribution algorithm based on the matrix transpose can be used. Using this algorithm, the manager will send blocks of size $\frac{c(i)}{f(i)}$ to each of $f(i)$ processors during the first phase. All of the $f(i)$ processors repeat this operation by concurrently sending their block to the other processors, in a circular fashion. The complexities for this are

$$\begin{cases} T_{comm}(n,p) & \le & 2\left(\tau + c(i) - \frac{c(i)}{f(i)}\right) \\ T_{comp}(n,p) & = & O\left(\frac{c(i)}{f(i)}\right). \end{cases} \tag{9}$$

The clients' complexities are thus improved to:

$$\begin{cases} T_{comm}(n,p) & \leq & \sum_{l=1}^{\log p}\left[\tau + 2^l\right] + \sum_{\rho=1}^{\log v}\left[2\left(\tau + 2q2^\rho\right)\right] + \\ & & \sum_{\kappa=1}^{\log w}\left[2\left(\tau + 2r2^\kappa\right)\right] \\ & \leq & (3\log p)\tau + 16n + 2p; \\ T_{comp}(n,p) & = & \mathrm{O}\left(\sum_{l=1}^{\log p} 2^l + \sum_{\rho=1}^{\log v}\left[\frac{2q2^\rho}{2^{2\rho}}\right] + \right. \\ & & \left. \sum_{\kappa=1}^{\log w}\left[\frac{2r2^\kappa}{2^{2\kappa-1}}\right] \right) + \\ & & \mathrm{O}\left(\frac{n^2}{p}\right) \\ & = & \mathrm{O}\left(\frac{n}{\sqrt{p}}\right) + \mathrm{O}\left(\frac{n^2}{p}\right) \\ & = & \mathrm{O}\left(\frac{n^2}{p}\right). \end{cases} \tag{10}$$

5.5 Parallel Complexity for Connected Components

Thus, for $p \leq n$, the total complexities for the parallel connected components algorithm are

$$\begin{cases} T_{comm}(n,p) & \leq & (4\log p)\tau + (24n + 2p) = (4\log p)\tau + \mathrm{O}\left(\frac{n^2}{p}\right); \\ T_{comp}(n,p) & = & \mathrm{O}\left(\frac{n^2}{p}\right). \end{cases} \tag{11}$$

Clearly, the computational complexity is the best possible asymptotically. As for the communication complexity, it seems that intuitively a latency factor τ has to be incurred during each merge operation, and hence the factor $(\log p)\tau$.

5.6 Experimental Results for Connected Components

Our theoretical analysis indicates that our connected components algorithm is scalable whenever $p \leq \frac{n}{c}$, where c is approximately 26 from the first expression in (11). We have implemented our algorithm in SPLIT-C on the CM-5; the resulting performance is plotted for images ranging from 128×128 to 1024×1024 pixels in size in Figures 15 - 17 for $p = 16$, 32, and 64 processors. Figure 3 presents the summary on the performance of our connected components algorithm on the CM-5 and clearly shows the scalability of our algorithm. Comparable results for execution on the IBM SP-1 are given in Figure 19, and for the IBM SP-2 in Figure 21.

6 Connected Components of Grey Scale Images

An $n \times n$ image with k grey levels, $(0 \ldots k-1)$, similarly can have its connected components labeled. A 0-pixel is assumed to be background, while each component is the set of like-colored connected pixels. Our algorithm for grey scale connected components of images is based upon the binary image algorithm in the previous section. Again, there will be three phases, an initial labeling, a merge of subimages, and a final updating of interior labels.

6.1 Initial labeling

Pixels on each tile are examined in row-major order. If a pixel is an unmarked nonzero-pixel, a breadth-first search procedure starting at that pixel labels all like-colored connected pixels situated on that tile with a globally unique label. A pixel is marked when visited only if it is a 0-pixel, or part of the current connected component.

6.2 Merging phase

The merging phase is almost identical to the previously described method for binary images. The only difference in the algorithms occurs when the group manager solves the problem of finding the connected components of the graph representing the border pixels during the merge of two subimages.

We use an adjacency list representation for the graph, and add vertices to the graph representing nonzero-pixels. As before, two types of edges are added to the graph. First, pixels are scanned down the left (or upper) border, and edges are strung linearly down the list between pixels containing the same connected component label. The same is done for pixels on the right (or lower) border. The second step adds edges between pixels of the left (upper) and right (lower) border which are both the same nonzero color and adjacent to each other.

A sequential breadth-first search based connected components algorithm computes the connected components of this graph. The pixels in this graph are then scanned again, and any changes in the labeling are stored in a sorted array of all unique changes (α_i, β_i), and propagated back to the clients processors.

Using the "hook" data structures, each processor then updates its border pixels from the current list of label changes. After the last merge step, each processor relabels its interior pixel labels.

The complexity for this algorithm remains the same as for binary images and is both efficient and optimal, i.e., for $p \leq n$,

$$\left\{ \begin{array}{lcl} T_{comm}(n,p) & \leq & (4 \log p)\tau + \mathrm{O}\left(\frac{n^2}{p}\right); \\ T_{comp}(n,p) & = & \mathrm{O}\left(\frac{n^2}{p}\right). \end{array} \right. \tag{12}$$

Results for the 256-grey level DARPA Image Understanding Benchmark image of size 512×512 pixels, shown in Figure 2, is given in Figure 10 for $p = 16$ to 128 processors on the CM-5, and for a wide range of configurations on the SP-1 and Meiko CS-2 parallel machines.

7 Implementation Notes

Note that the performance graphs for the CM-5, Figures 3, 6, 10 - 17, are for Split-C (version 1.2) programs linked with the CM-5 CMMD Message Passing Libraries (version 3.2), Figures 10, 18 - 19 are for the IBM SP-1 with the message passing libraries MPL, and Figures 7, 20 - 21 are for the IBM SP-2 with wide nodes and also MPL. Figures 8 and 10 are run on a Meiko CS-2 with Split-C linked with the Elan Widgets message passing library. Note that our port of Split-C to the CS-2 results in less than optimal performance because this Split-C installation has not been fully optimized to make use of Elan, the low level communications library. We expect results using an optimized platform shortly. Figure 9 is implemented on an 8-processor Intel Paragon, using the PAM message passing libraries, the Paragon Active Messages platform from UC Berkeley.

The source code for the parallel algorithms presented in this paper, image histogramming and connected components, is available for distribution to interested parties.

8 Acknowledgements

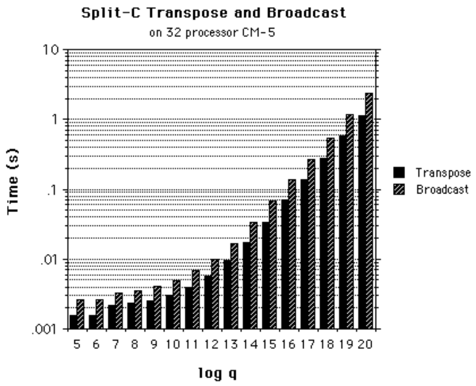
We would like to thank the UMIACS parallel systems staff, including Jerry Sobieski, Mitch Murphy, and Phil Iorio, for their help and machine maintenance while developing this research on the 32-processor UMIACS CM-5, the CASTLE group at Berkeley, especially the help and encouragement from Arvind Krishnamurthy, Lok Tin Liu, David Culler, Steve Luna, and Rich Martin, and the use of UC Berkeley's 64-processor CM-5 and 8-processor Paragon for testing purposes, and Charles Weems at the University of Massachusetts for providing the DARPA test image suite. Computational support on Berkeley's TMC CM-5 and Intel Paragon was provided by NSF Infrastructure Grant number CDA-8722788. We also thank Toby Harness and the Numerical Aerodynamic Simulation Systems Division of NASA's Ames Research Center for use of their 128-processor CM-5 and 128-node (all wide) IBM SP-2.

We thank Argonne National Labs for use of their 128-node IBM SP-1, and the Maui High Performance Computing Center for use of their 400-node IBM SP-2 machine. William Gropp, from the Mathematics and Computer Science Division of Argonne National Labs, provided significant help with the IBM SP-1 message passing interface, EUIH, written by Peter Hochschild of IBM-Yorktown, used in our original port of Split-C to the SP-1.

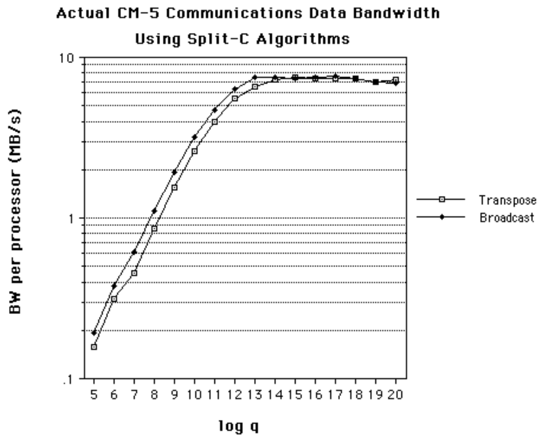
Also, Klaus Schauser and David Probert of University of California, Santa Barbara, provided access to the 64-node UCSB Meiko CS-2. The Meiko CS-2 Computing Facility was acquired through NSF CISE Infrastructure Grant number CDA-9218202, with support from the College of Engineering and the UCSB Office of Research, for research in parallel computing.

A Execution Time

A.1 Transpose and Broadcast Algorithms

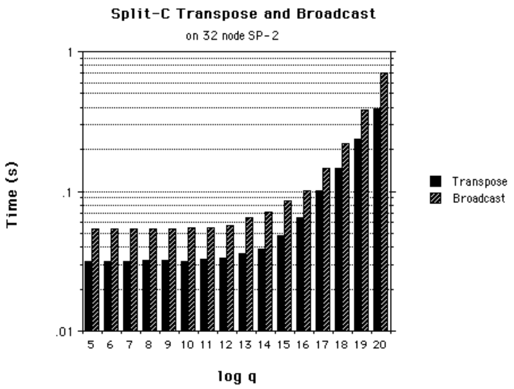


Execution Time

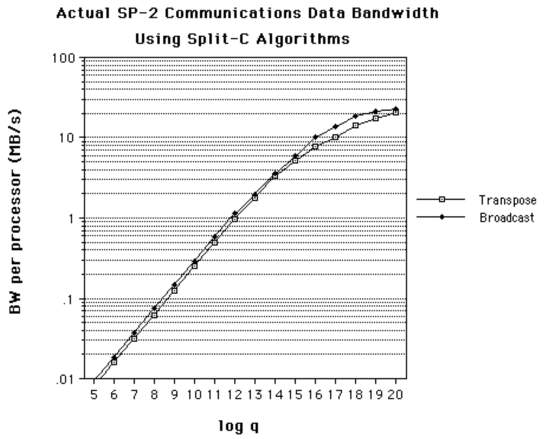


Bandwidth

Figure 6: Transpose and Broadcasting Performance Graphs on the TMC CM-5 (p=32)

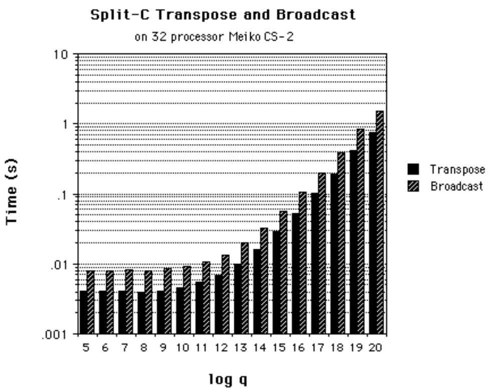


Execution Time

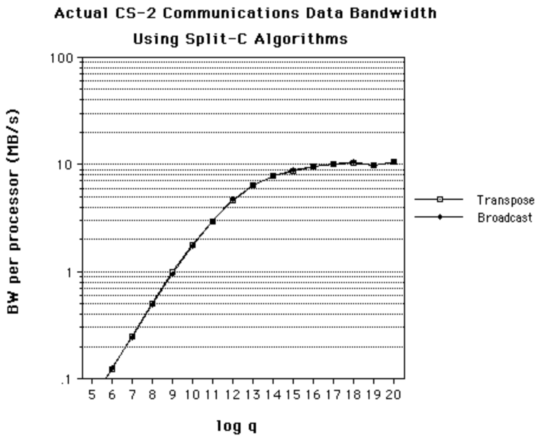


Bandwidth

Figure 7: Transpose and Broadcasting Performance Graphs on the IBM SP-2 (p=32)

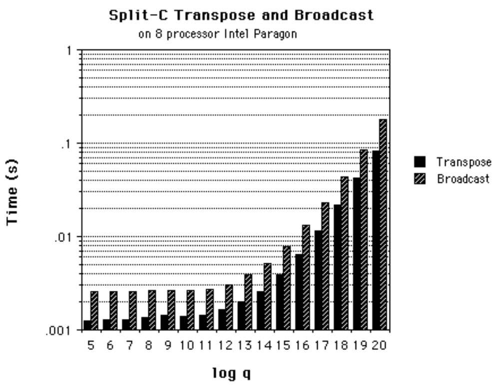


Execution Time

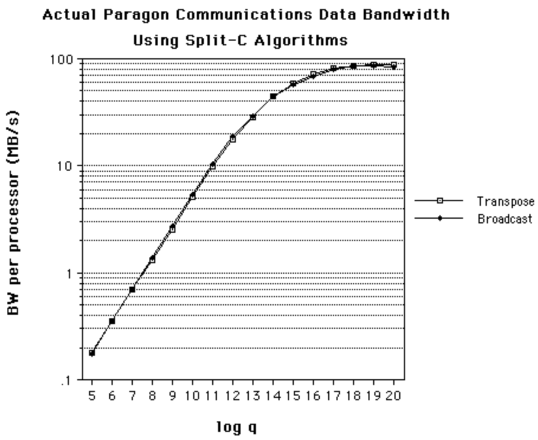


Bandwidth

Figure 8: Transpose and Broadcasting Performance Graphs on the Meiko CS-2 (p=32)



Execution Time



Bandwidth

Figure 9: Transpose and Broadcasting Performance Graphs on the Intel Paragon (p=8)

A.2 DARPA Image Understanding Benchmark

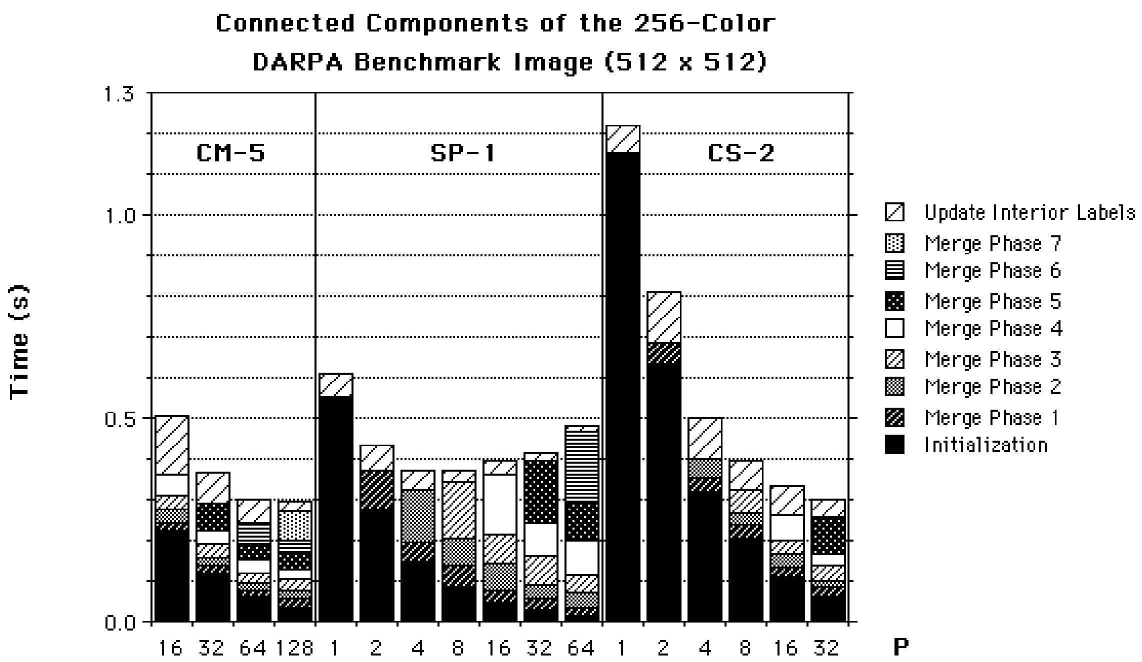
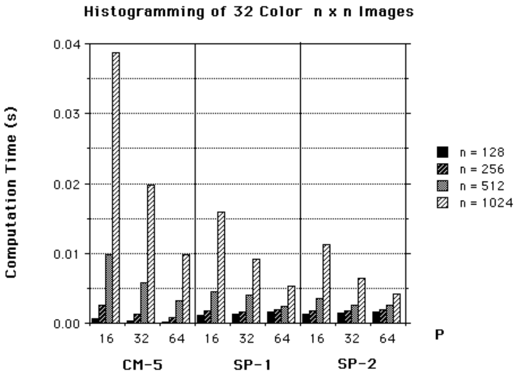
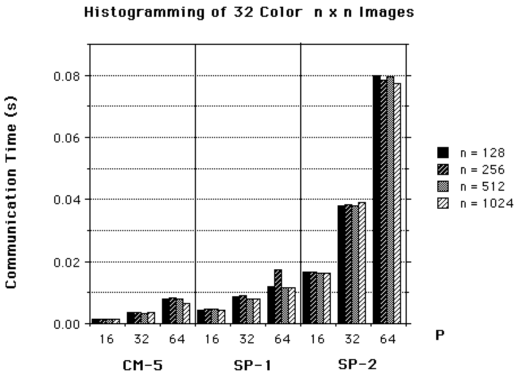


Figure 10: Connected Components of 512 x 512 DARPA Benchmark Image on Various Machines

A.3 Scalability of Histogramming Algorithm

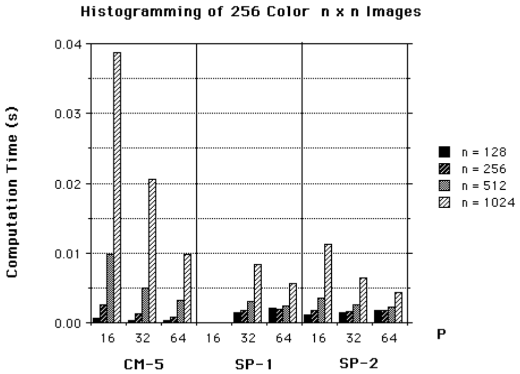


Computation Time

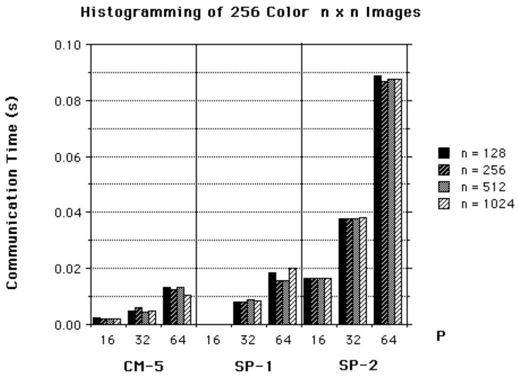


Communication Time

Histogramming of 32 color image



Computation Time

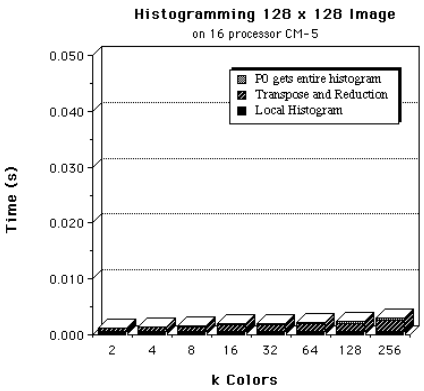


Communication Time

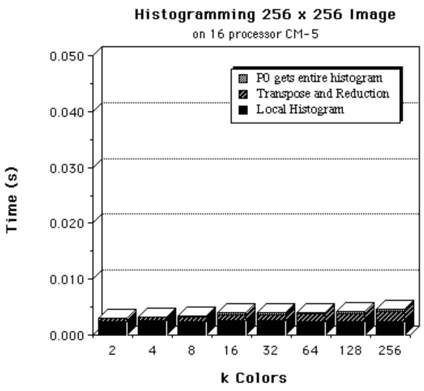
Histogramming of 256 color image

Figure 11: Histogramming Performance

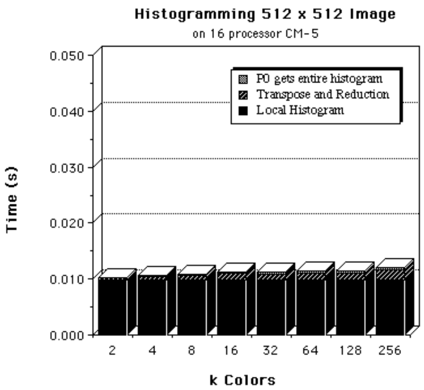
A.4 CM-5 Histogramming Performance Graphs



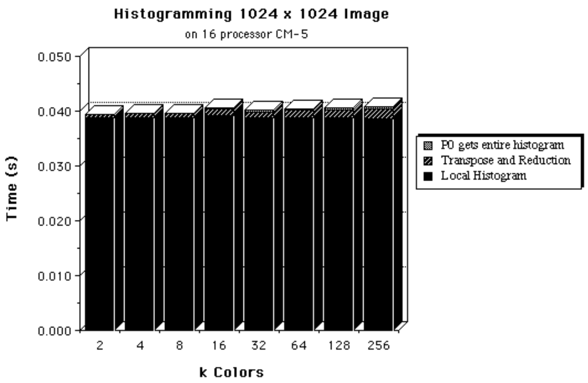
128x128 Images



256x256 Images

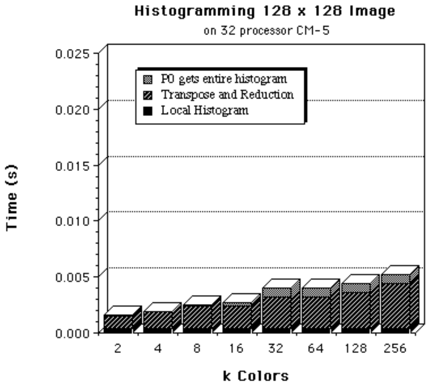


512x512 Images

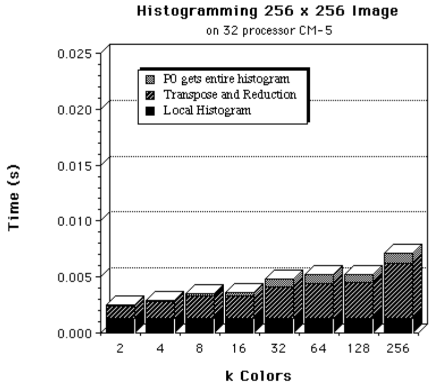


1024x1024 Images

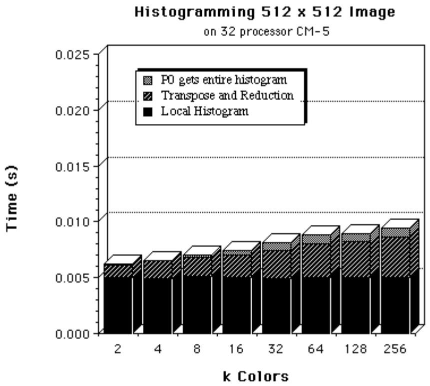
Figure 12: Histogramming Algorithm Performance Graph on the CM-5 (p=16)



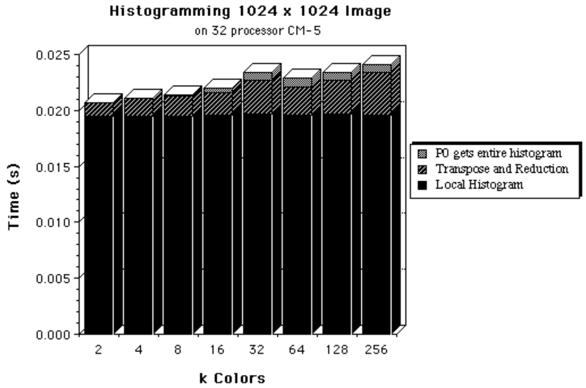
128x128 Images



256x256 Images

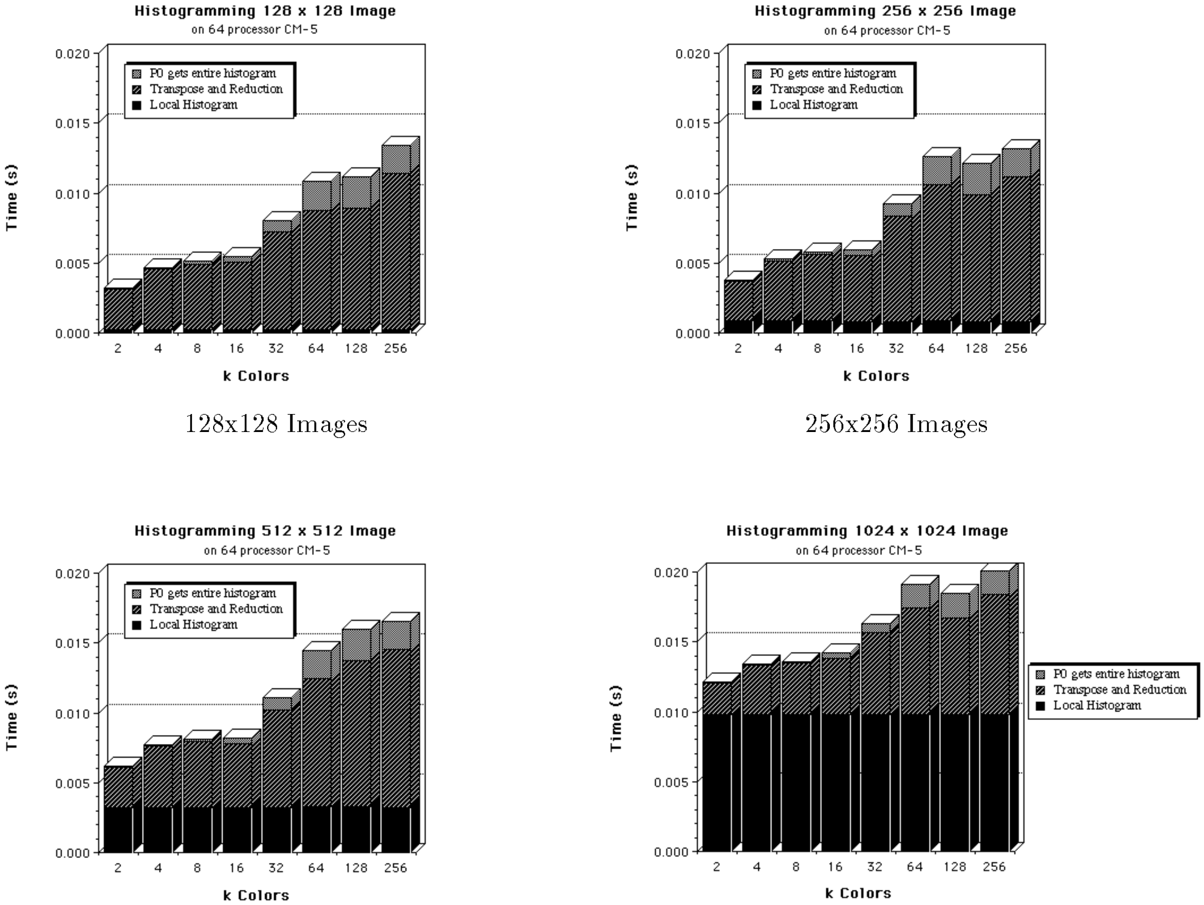


512x512 Images



1024x1024 Images

Figure 13: Histogramming Algorithm Performance Graph on the CM-5 (p=32)



128x128 Images

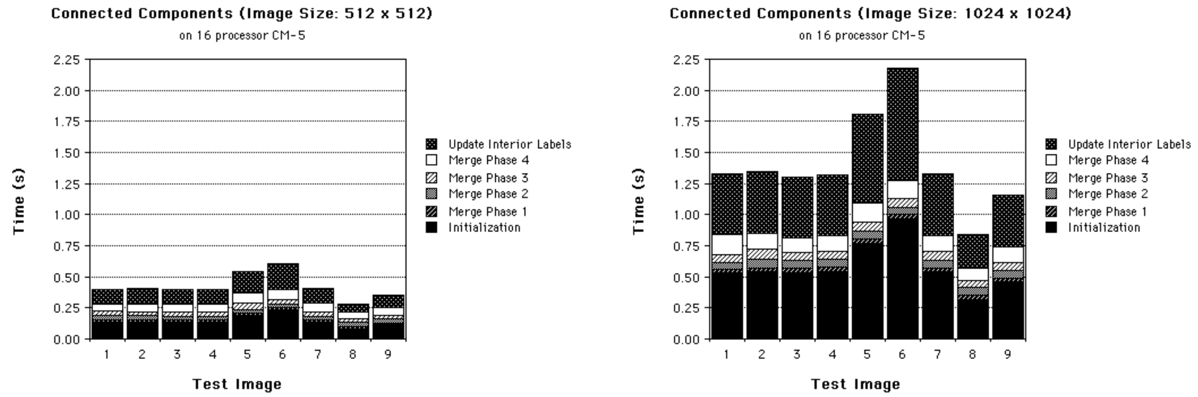
256x256 Images

512x512 Images

1024x1024 Images

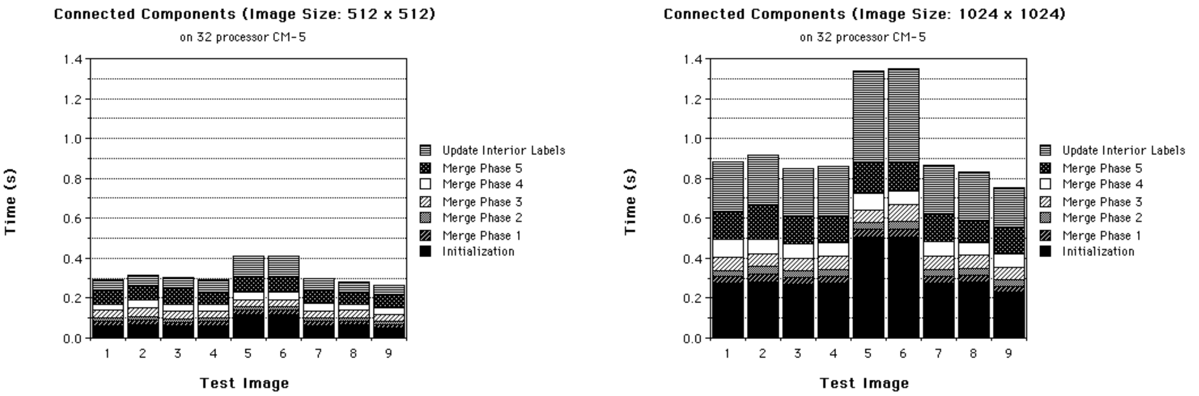
Figure 14: Histogramming Algorithm Performance Graph on the CM-5 (p=64)

A.5 CM-5 Connected Components Performance Graphs



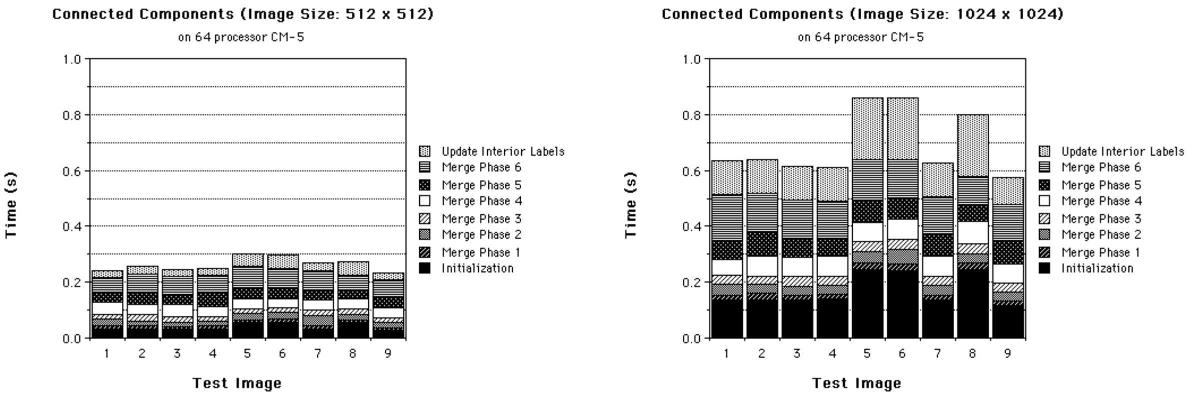
512x512 Test Images 1024x1024 Test Images

Figure 15: Connected Components Algorithm Performance Graph on the CM-5 (p=16)



512x512 Test Images 1024x1024 Test Images

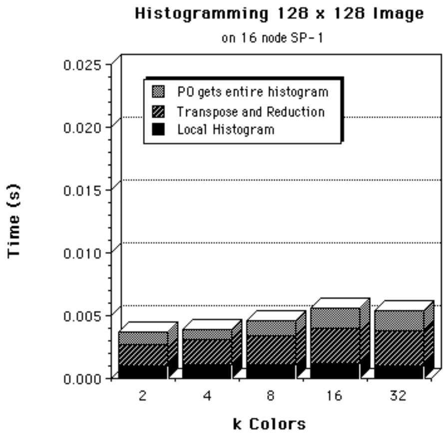
Figure 16: Connected Components Algorithm Performance Graph on the CM-5 (p=32)



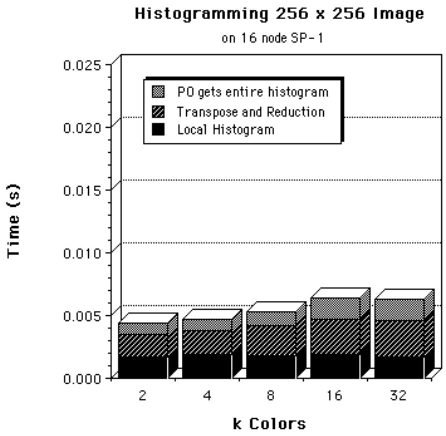
512x512 Test Images 1024x1024 Test Images

Figure 17: Connected Components Algorithm Performance Graph on the CM-5 (p=64)

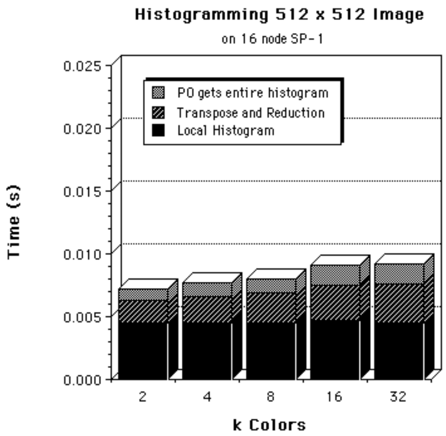
A.6 SP-1 Histogramming Performance Graphs



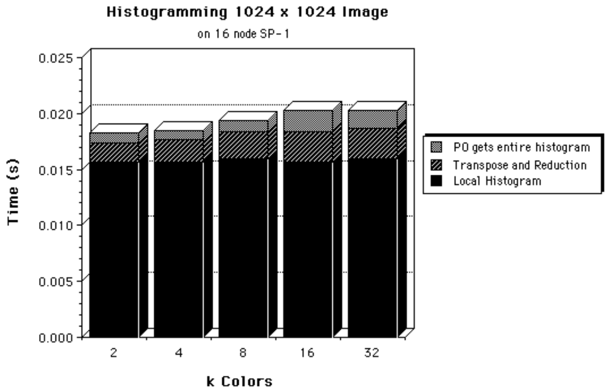
128x128 Images



256x256 Images



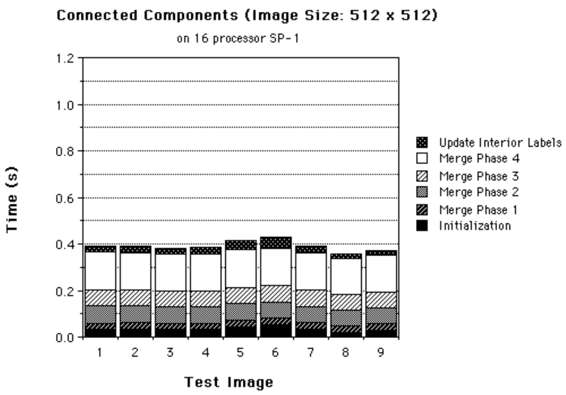
512x512 Images



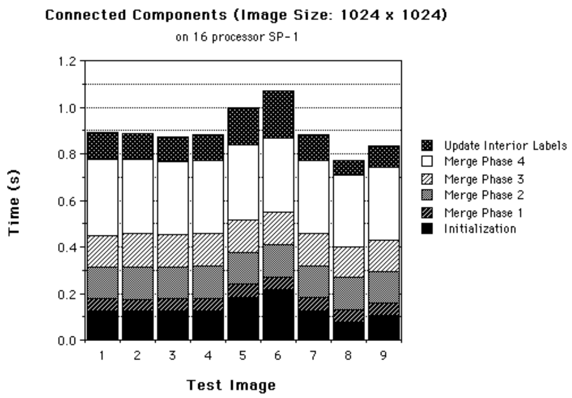
1024x1024 Images

Figure 18: Histogramming Algorithm Performance Graph on the SP-1 (p=16)

A.7 SP-1 Connected Components Performance Graphs



512x512 Test Images

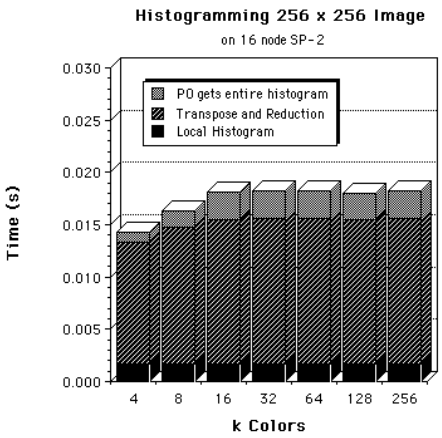


1024x1024 Test Images

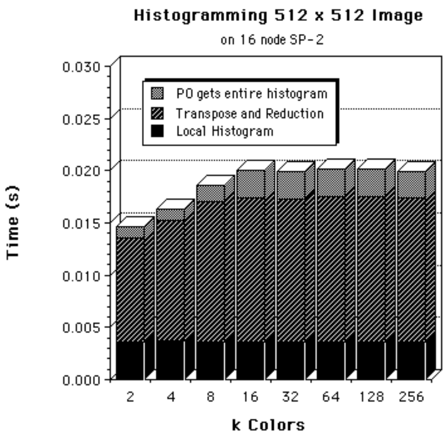
Figure 19: Connected Components Algorithm Performance Graph on the SP-1 (p=16)

A.8 SP-2 Histogramming Performance Graphs

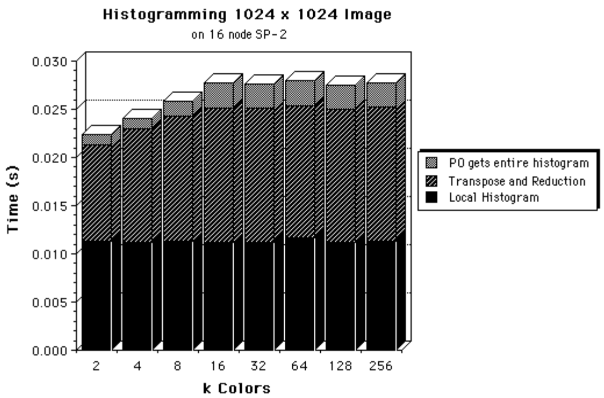
128x128 Images



256x256 Images



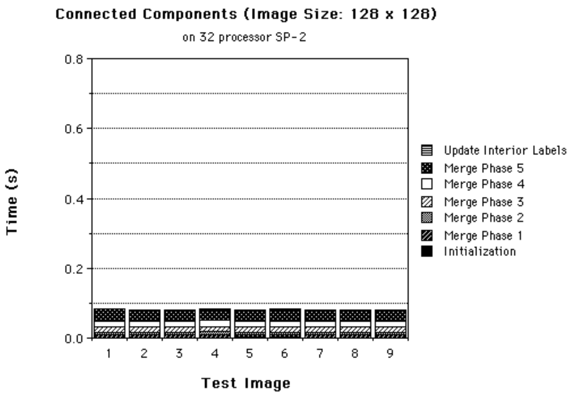
512x512 Images



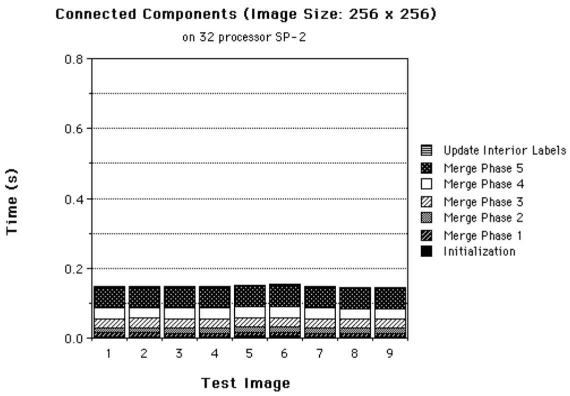
1024x1024 Images

Figure 20: Histogramming Algorithm Performance Graph on the SP-2 (p=16)

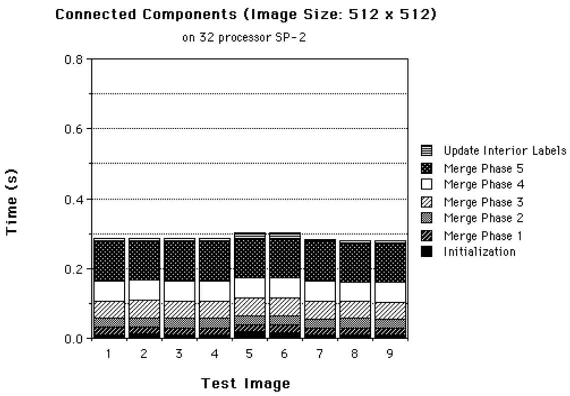
A.9 SP-2 Connected Components Performance Graphs



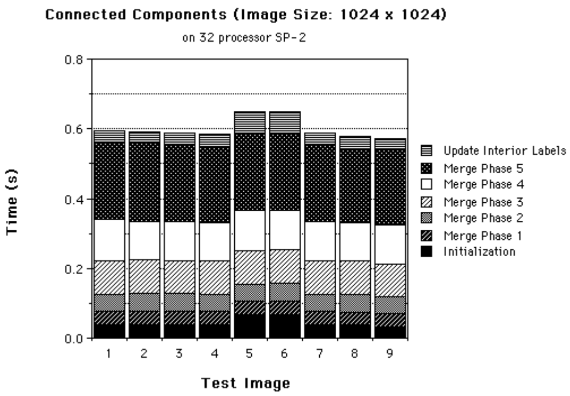
128x128 Test Images



256x256 Test Images



512x512 Test Images



1024x1024 Test Images

Figure 21: Connected Components Algorithm Performance Graph on the SP-2 (p=32)

References

[1] H. Alnuweiri and V. Prasanna. Parallel Architectures and Algorithms for Image Component Labeling. *IEEE Transactions on Pattern Analysis and Machine Intelligence*, 14:1014–1034, 1992.

[2] J. Apostolakis, P. Coddington, and E. Marinari. New SIMD Algorithms for Cluster Labeling on Parallel Computers. Technical Report SCCS-279, Physics Department, Syracuse University, Syracuse, NY, September 1992. Int. J. Mod. Phys. C 4, 749 (1993).

[3] J. Apostolakis, P. Coddington, and E. Marinari. New SIMD Algorithms for Cluster Labeling on Parallel Computers. *Int. J. Mod. Phys. C*, 4:749, 1993.

[4] C.F. Baillie and P.D. Coddington. Cluster Identification Algorithms for Spin Models - Sequential and Parallel. *Concurrency: Practice and Experience*, 3(2):129–144, 1991.

[5] R.C. Brower, P. Tamayo, and B. York. A Parallel Multigrid Algorithm for Percolation Clusters. *Journal of Statistical Physics*, 63:73, 1991.

[6] F.Y. Chin, J. Lam, and I-N. Chen. Efficient Parallel Algorithms for Some Graph Problems. *Communications of the ACM*, 25(9):659–665, 1982.

[7] A. Choudhary and R. Thakur. Evaluation of Connected Component Labeling Algorithms on Shared and Distributed Memory Multiprocessors. In *Proceedings of the 6th International Parallel Processing Symposium*, pages 362–365, March 1992.

[8] A. Choudhary and R. Thakur. Connected Component Labeling on Coarse Grain Parallel Computers: An Experimental Study. *Journal of Parallel and Distributed Computing*, 20(1):78–83, January 1994.

[9] N. Copty, S. Ranka, G. Fox, and R.V. Shankar. A Data Parallel Algorithm for Solving the Region Growing Problem on the Connection Machine. *Journal of Parallel and Distributed Computing*, 21(1):160–168, April 1994.

[10] D.E. Culler, A. Dusseau, S.C. Goldstein, A. Krishnamurthy, S. Lumetta, S. Luna, T. von Eicken, and K. Yelick. *Introduction to Split-C*. Computer Science Division - EECS, University of California, Berkeley, version 1.0 edition, March 6 1994.

[11] D.E. Culler, R.M. Karp, D.A. Patterson, A. Sahay, K.E. Schauser, E. Santos, R. Subramonian, and T. von Eicken. LogP: Towards a Realistic Model of Parallel Computation. In *Fourth ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, May 1993.

[12] M.B. Dillencourt, H. Samet, and M. Tamminen. Connected Component Labeling of Binary Images. Technical Report CS-TR-2303, Computer Science Department, University of Maryland, August 1989.

[13] H. Embrechts, D. Roose, and P. Wambacq. Component Labelling on a MIMD Multiprocessor. *CVGIP: Image Understanding*, 57(2):155–165, March 1993.

[14] B. Falsafi and R. Miller. Component Labeling Algorithms on an Intel iPSC/2 Hypercube. In *Proceedings of the Fifth Distributed Memory Computing Conference*, pages 159–164, Charleston, SC, April 1990.

[15] J. Grinberg, G.R. Nudd, and R.D. Etchells. A Cellular VLSI Architecture. *IEEE Computer*, 17(1):69–81, 1984.

[16] Y. Han and R.A. Wagner. An Efficient and Fast Parallel-Connected Component Algorithm. *JACM*, 37(3):626–642, 1990.

[17] D.S. Hirschberg, A.K. Chandra, and D.V. Sarwate. Computing Connected Components on Parallel Computers. *Communications of the ACM*, 22(8):461–464, 1979.

[18] R. Hummel. Connected Component Labelling in Image Processing with MIMD Architectures. In M.J.B. Duff, editor, *Intermediate-Level Image Processing*, chapter 7, pages 101–127. Academic Press, New York, 1986.

[19] H.A. Ibrahim, J.R. Kender, and D.E. Shaw. Low-Level Image Analysis Tasks on Fine-Grained Tree-Structured SIMD Machines. *Journal of Parallel and Distributed Computing*, 4:546–574, 1987.

[20] J. JáJá. *An Introduction to Parallel Algorithms*. Addison-Wesley Publishing Company, New York, 1992.

[21] J. JáJá and K.W. Ryu. The Block Distributed Memory Model. Technical Report CS-TR-3207, Computer Science Department, University of Maryland, College Park, January 1994.

[22] J.F. JáJá and K.W. Ryu. The Block Distributed Memory Model for Shared Memory Multiprocessors. In *Proceedings of the 8th International Parallel Processing Symposium*, pages 752–756, Cancún, Mexico, April 1994. (Extended Abstract).

[23] C.R. Jesshope. Parallel Computers - Architecutures and Programming. In R.A. Vaughan, editor, *Pattern Recognition and Image Processing in Physics*, pages 205–234. Scottish Universities Summer School in Physics, New York, 1990.

[24] T. Kanade and J.A. Webb. Parallel Vision Algorithm Design and Implementation 1988 End of Year Report. Technical Report CMU-RI-TR-89-23, The Robotics Institute, Carnegie-Mellon University, August 1989.

[25] J.J. Kistler and J.A. Webb. Connected Components With Split and Merge. In *Proceedings of the 5th International Parallel Processing Symposium*, pages 194–201, Anaheim, CA, April 1991.

[26] A. Krikelis and R.M. Lea. Performance of the ASP on the DARPA Architecture Benchmark. In *Proceedings of the 2nd Symposium on the Frontiers of Massively Parallel Computation*, pages 483–486, Fairfax, VA, October 1988.

[27] J.M. Kuzela. *IBM POWERparallel System - SP2 Performance Measurements*. Power Parallel Systems, IBM, October 1994.

[28] C.E. Leiserson, Z.S. Abuhamdeh, D.C. Douglas, C.R. Feynman, M.N. Ganmukhi, J.V. Hill, W.D. Hillis, B.C. Kuszmaul, M.A. St. Pierre, D.S. Wells, M.C. Wong, S.-W. Yang, and R. Zak. The Network Architecture of the Connection Machine CM-5. (Extended Abstract), July 28, 1992.

[29] J.J. Little. Parallel Algorithms for Computer Vision on the Connection Machine. Technical Report AIM-928, MIT AI Laboratory, November 1986.

[30] L.T. Liu. Personal communications. November 1994.

[31] M. Manohar and H.K. Ramapriyan. Connected Component Labeling of Binary Images on a Mesh Connected Massively Parallel Processor. *Computer Vision, Graphics, and Image Processing*, 45(2):133–149, 1989.

[32] P. Marks. Low-Level Vision Using an Array Processor. *Computer Graphics and Image Processing*, 14:281–292, 1980.

[33] Meiko. *Computing Surface - Communications Network Overview*. Meiko World Inc., Concord, MA, manual 84-cb041 edition, 1993.

[34] G.R. Nudd, T.J. Atherton, N.D. Francis, R.M. Howarth, D.J. Kerbyson, R.A. Packwood, and G.J. Vaudin. A Hierarchical Multiple-SIMD Architecture for Image Analysis. In *Proceedings of the 10th International Conference on Pattern Recognition*, pages 642–647, Atlantic City, NJ, June 1990.

[35] D. Parkinson. Experiments in Component Labeling in a Parallel Computer. In V.K. Prasanna Kumar, editor, *Parallel Architectures and Algorithms for Image Understanding*, pages 209–225. Academic Press, Inc., New York, 1991.

[36] J.L. Potter. Image Processing on the Massively Parallel Processor. *IEEE Computer*, 16(1):62–67, 1983.

[37] A. Rosenfeld. A Report on the DARPA Image Understanding Architectures Workshop. In *Proceedings of the 1987 Image Understanding Workshop*, pages 298–302, 1987.

[38] H. Samet and M. Tamminen. A General Approach To Connected Component Labeling of Images. Technical Report CS-TR-1649, Computer Science Department, University of Maryland, August 1986.

[39] A.D. Sokal. New Numerical Algorithms for Critical Phenomena (Multi-grid Methods and All That). In D.P. Landau, K.K. Mon, and H.-B. Schuttler, editors, *Computer Simulation Studies in Condensed Matter Physics: Recent Developments*. Springer-Verlag, Berlin, 1988.

[40] A.D. Sokal. New Numerical Algorithms for Critical Phenomena (Multi-grid Methods and All That). In *Proceedings of the International Conference on Lattice Field Theory*, Tallahassee, Fl, October 1990. (*Nucl. Phys. B (Proc. Suppl.)* **20**:55, 1991.).

[41] D. Stauffer. *Introduction to Percolation Theory*. Taylor and Francis, Philadelphia, PA, 1985.

[42] Q.F. Stout. Supporting Divide-and-Conquer Algorithms for Image Processing. *Journal of Parallel and Distributed Computing*, 4:95–115, 1987.

[43] M.H. Sunwoo, B.S. Baroody, and J.K. Aggarwal. A Parallel Algorithm for Region Labeling. In *Proceedings of the 1987 Workshop on Computer Architecture for Pattern Analysis and Machine Intelligence*, pages 27–34, Seattle, WA, October 1987.

[44] R.S. Wallace and M.D. Howard. HBA Vision Architecture: Built and Benchmarked. In *Proceedings of the 1987 Workshop on Computer Architecture for Pattern Analysis and Machine Intelligence*, pages 209–216, Seattle, WA, October 1987.

[45] R.S. Wallace and M.D. Howard. HBA Vision Architecture: Built and Benchmarked. *IEEE Transactions on Pattern Analysis and Machine Intelligence*, 11(3):227–232, 1989.

[46] J.-C. Wang, T.-H. Lin, and S. Ranka. Distributed Scheduling of Unstructured Collective Communication on the CM-5. Personal Communication., 1994.

[47] C. Weems, E. Riseman, A. Hanson, and A. Rosenfeld. An Integrated Image Understanding Benchmark: Recognition of a $2\frac{1}{2}$ D "Mobile". In *Image Understanding Workshop*, pages 111–126, Cambridge, MA, April 1988.

[48] C. Weems, E. Riseman, A. Hanson, and A. Rosenfeld. A Report on the Results of the DARPA Integrated Image Understanding Benchmark Exercise. In *Image Understanding Workshop*, pages 165–192, May 1989.

[49] S.G. Ziavras and P. Meer. Adaptive Multiresolution Structures for Image Processing on Parallel Computers. *Journal of Parallel and Distributed Computing*, 23:475–483, 1994.