ABSTRACT

Title of Dissertation:	LOW-COST AND HIGH-RELIABILITY, SINGLE-STAGE MICROINVERTER FOR RESIDENTIAL SOLAR APPLICATIONS
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Recent attention has focused on reduced cost, improved reliability, and enhanced functionality of power electronics in residential solar applications, specifically in the microinverter architecture. In particular, the Department of Energy SunShot Initiative 2030 goals target a Levelized Cost of Electricity (LCOE) of less than 5 ¢/kWh. Traditional microinverter costs represent nearly 22 % of fixed system-level costs and approximately 45 % of variable operation and maintenance costs related to reliability, inhibiting achievable LCOE. This dissertation proposes a next generation microinverter as a key enabler for advancements required to realize the 2030 goals, from cost and reliability perspectives. The proposed microinverter circuit utilizes a single-stage topology based on the Dual Active Bridge (DAB) circuit, leveraging a combination of wide-bandgap Gallium Nitride (GaN) devices and Si devices at high switching frequency. Additionally, the proposed converter realizes low-frequency energy storage through an active power decoupling (APD) circuit, which enables the

use of high-reliability film capacitors in contrast to the traditional use of lower-reliability electrolytic capacitors. Aside from topological advantages such as inherent galvanic isolation and low component count, design decisions and component selections are supported by multi-objective optimization, pushing the boundaries in the converter design.

The proposed microinverter circuit is analyzed in steady-state operation, where an improved analytical modelling technique is required to properly predict converter performance, and enable control-level optimization. Main-circuit parametric design optimization is performed to select transformer turns ratio and leakage inductances which minimize the converter's efficiency drop due to conduction loss, while enabling near-uniform zero-voltage-switching transitions minimizing switching-related losses. The analysis is extended to multi-objective analysis targeting minimization of cost, area, and efficiency drop, informing design tradeoffs and component selection both at the topology and device levels. To improve the performance of the main-circuit transformer, and reduce the cost with a planar PCB-based design, a novel integrated-leakage transformer is developed which adopts performance advantages over similar state-of-the-art designs. Finally, holistic multi-objective optimization procedure is developed for the APD based on cost, efficiency, and power density, to enable holistic component selection. To validate the design and associated analyses, a proof-of-concept for the main-circuit and APD are designed and tested.

LOW-COST AND HIGH-RELIABILITY, SINGLE-STAGE MICROINVERTER FOR RESIDENTIAL SOLAR APPLICATIONS

by

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Chapter 1. Power Converters in Microinverter Applications

Over the last decade, residential solar installments have experienced significant growth, fueled by reduced cost of power electronics as well as solar panels [1]. Residential solar installments are specifically popular for consumers interested to offset their residential energy consumption, reducing the greenhouse gas footprint of individual households, which consume an average of 10,972 kWh per year in the United States [2]. While environmental conditions differ across the United States in regards to sunlight and temperature, projects such as Google Project Sunroof have made the potential of solar installments clear to homeowners, where for example installations in Washington, DC can expect 1,037 kWh per kW of installed rooftop solar capacity [3]. To facilitate further penetration of residential solar applications, low cost and high performance power electronics are required. In particular, next generation power electronics for residential solar applications will enable lower Levelized Costs of Electricity (LCOE), as they deliver more reliable, efficient, and cost-effective power to the home and utility grid.

1.1. Levelized cost of electricity

Of principal importance in any solar-based energy generation system is the LCOE [4]. This metric identifies the total lifetime cost of the system divided by the lifetime energy generation, hence defining the effective cost of energy production of the renewable system. A simplified LCOE calculation can be performed with,

$$sLCOE = \frac{\sum_{n=0}^{n_s} \frac{c_n}{(1+d)^n}}{\sum_{n=0}^{n_s} \frac{e_n}{(1+d)^n}} \tag{1.1}$$

where c_n is the cost of the system in year n, d is the discount rate (i.e. the annual rate at which future costs and future energy production are discounted), e_n is the energy produced in year n, and n_s is the number of years in the system's service life [4]. The cost of the system can be defined by,

$$c_n = \begin{cases} c_{capital} & n = 0 \\ c_{O\&M} & n > 0 \end{cases} \tag{1.2}$$

where $c_{capital}$ is the initial capital cost of the system, and $c_{o\&m}$ is the yearly operation and maintenance related cost, which includes both fixed and variable costs [4]. Furthermore, the energy production of the system can be defined by,

$$e_n = \begin{cases} 0 & n = 0 \\ \max[Y(1-R_d)^{n-1}, 0] & n > 0 \end{cases} \tag{1.3}$$

where Y is the energy generation of the system in the first year, and R_d is the annual degradation rate of the system [4]. By considering the total lifetime of the system n_s, the sLCOE metric factors in both up-front fixed costs, and variable costs, relating to system-level operation and maintenance. Therefore, it is critical for solar-based energy generation systems to be both low in up-front costs, reliable to limit lifetime variable costs and system-level degradation, and highly efficient to maximize the energy output.

The Department of Energy (DOE) released 2030 LCOE goals for various types of solar-based systems on behalf of the SunShot program, as shown in Fig. 1.1 [5]. It is clear that the 2020 goals sought improvement over the state of solar-based LCOE in

2017, whereas the 2030 goals targeted a further 50% of the 2020 goal in each sector. In particular, the residential LCOE costs were targeted for the largest improvement, achieving an LCOE cost of 16 ¢/kWh in 2017, to the projected goal of 5 ¢/kWh in 2030. By enabling LCOE cost targets proposed by the 2030 SunShot goals, a large inrush of solar energy generation is anticipated, contributing to upwards of 17% of total electricity generation capacity in the United States in 2030, and upwards of 33% by 2050 [5].

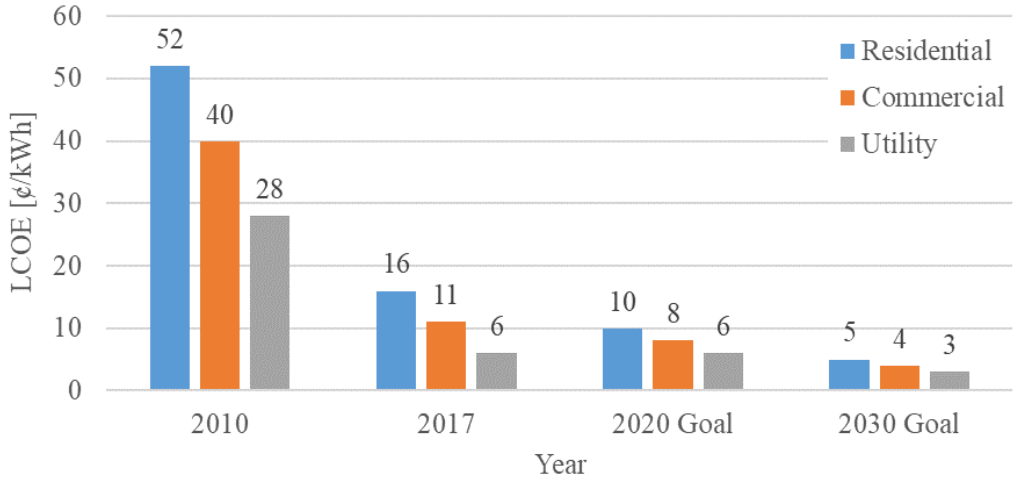


Fig. 1.1. SunShot LCOE goals for solar energy generation systems by sector [5].

1.2. Residential solar architectures

There are three principal architectures for residential solar installments, which all describe unique ways in which power electronics converters are interfaced between the rooftop photovoltaic (PV) panels and the utility grid. The three architectures, namely string inverter, DC optimizer, and microinverter, are shown in Fig. 1.2. The significant features in choosing solar architectures include: 1) panel-level maximum power-point tracking (MPPT), 2) power electronics cost per installed Watt [$/W], 3)

reliability, 4) safety, and 5) modularity. The following sections will break down the pros and cons of each of the three architectural implementations, followed by a comparison.

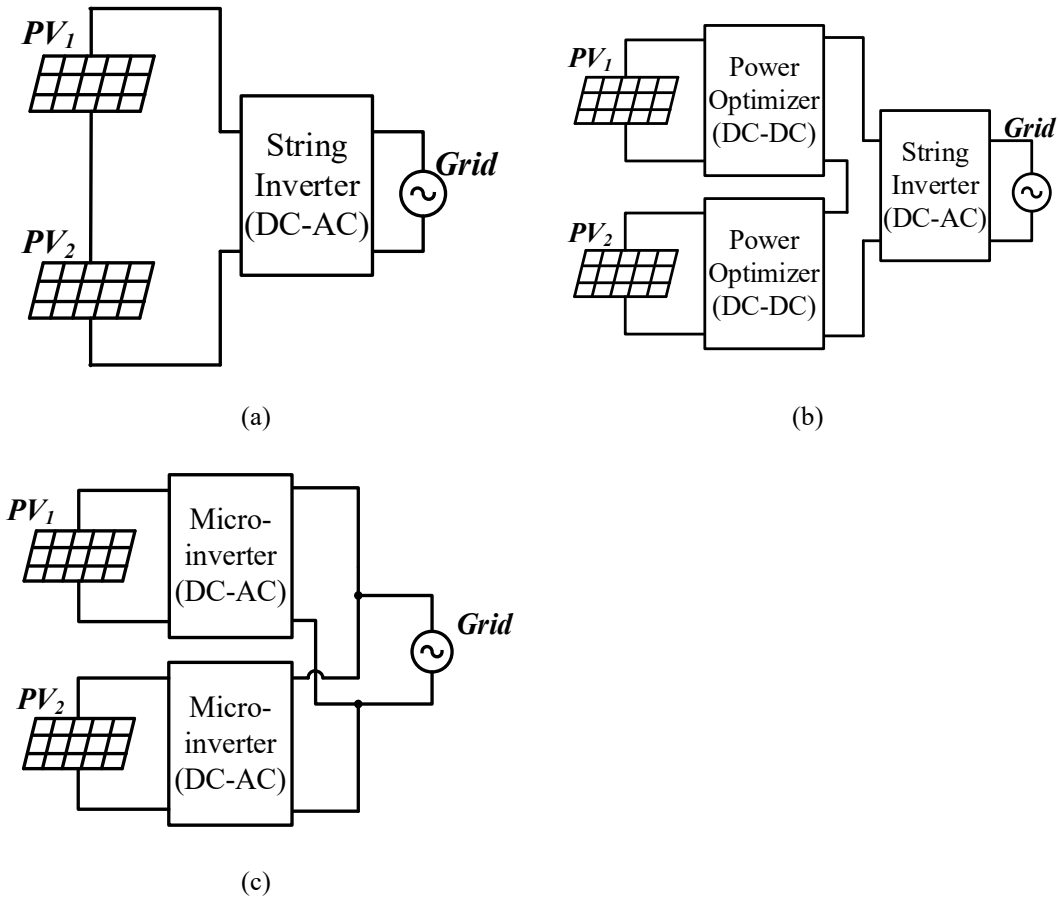


Fig. 1.2. Block diagrams of the three principal architectures used in residential PV applications, dictating unique ways in which power electronics interface between the PV panels and the utility grid, (a) string inverter, (b) DC optimizer, and (c) microinverter.

1.2.1. String inverter

The string inverter in Fig. 1.2(a) is a popular approach due to structural simplicity and ease of installment. The architecture requires only a single power electronics component, the string inverter, which extracts energy from the full PV string and injects it into the grid. With that being said, control over individual PV panel

operating points is largely lost, as only control over the string voltage is possible. As such, string-level partial shading conditions will cause the system to often operate away from the true maximum power point of the PV string. Furthermore this architecture is limited by safety issues, including the requirement of high-voltage DC wiring in the home between the PV panel bus and the string inverter. From a reliability perspective, the string inverter architecture is limited as any failures in the string inverter will result in full-system shut-down. Additionally, the string-inverter is not a modular solution, as most string inverters specify the maximum number of PV panels which can be connected in series and parallel.

1.2.2. DC optimizer

The DC optimizer approach shown in Fig. 1.2(b) is an approach combining a string inverter with individual PV panel-level DC-DC power electronics. The DC optimizers, i.e. the DC-DC converters interfaced with each solar panel, can enable panel-level maximum power point tracking, which is the major inhibitor of the string inverter architecture. However, the design still requires high voltage DC wiring in the home, which can be a safety concern. Furthermore, the reliability of the system includes both the reliability of the module-level DC-DC converters, and the string inverter, generating additional points of failure that can be undesirable. Finally, from a modular perspective, the system sizing is again limited by the specifications of the string inverter, though the addition of the DC optimizers enables some improvement.

1.2.3. Microinverter

The microinverter approach shown in Fig. 1.2(c) combines the advantages of the DC optimizer approach, without the requirement of a string inverter. In this case, each panel is interfaced by a DC-AC converter performing MPPT and grid integration. Microinverter systems are able to exhibit improved reliability due to the distributed power electronics configuration, where a failure in any microinverter will not bring down the full system. Furthermore, microinverter systems are wired with grid compliant AC cables which can be safer in residential applications than their DC counterpart. Finally, the microinverter architecture is truly modular, as any number of PV panels and dedicated microinverters can be placed upon the rooftop without restrictions due to system-level power rating. However, with the added advantages, current microinverter systems are not as cost effective as the other presented architectures.

1.2.4. Comparison

The aforementioned architectures for residential solar installments are compared over various metrics in Table 1.1. Based on system-level costs as of 2018, it is clear that the microinverter is the highest of the three architectures from the perspective of system-level cost per installed Watt [1]. With that being said, microinverter approaches provide safer residential installment options than DC optimizer and string inverter systems in the absence of a high voltage DC bus. Furthermore, microinverter structures adopt similar MPPT advantages as DC optimizers due to the module-level connection of the power electronics, but realize improved modularity.

Table 1.1. Comparison of residential solar architectures.

Architecture	MPPT	$/W [1]	Reliability	Safety	Modularity
String inverter	Poor	$2.54	Poor	High voltage DC bus	Low
DC optimizer	Good	$2.59	Poor	High voltage DC bus	Medium
Microinverter	Good	$3.06	Good	Grid-compliant AC bus	High

Further cost breakdown of the residential architectures is presented in Fig. 1.3, where the specific cost categories attributing to increased microinverter system-level costs as compared to the string inverter and DC optimizer systems are revealed. Specifically, increased cost of microinverter systems are mainly attributed to increased inverter-related costs, balance of system costs (i.e. the system-level costs associated with interconnection of the system with the PV panels and electric grid), and supply chain costs. Therefore, it is clear that microinverters should be targeted for advanced research to drive down inverter- and BOS-related costs.

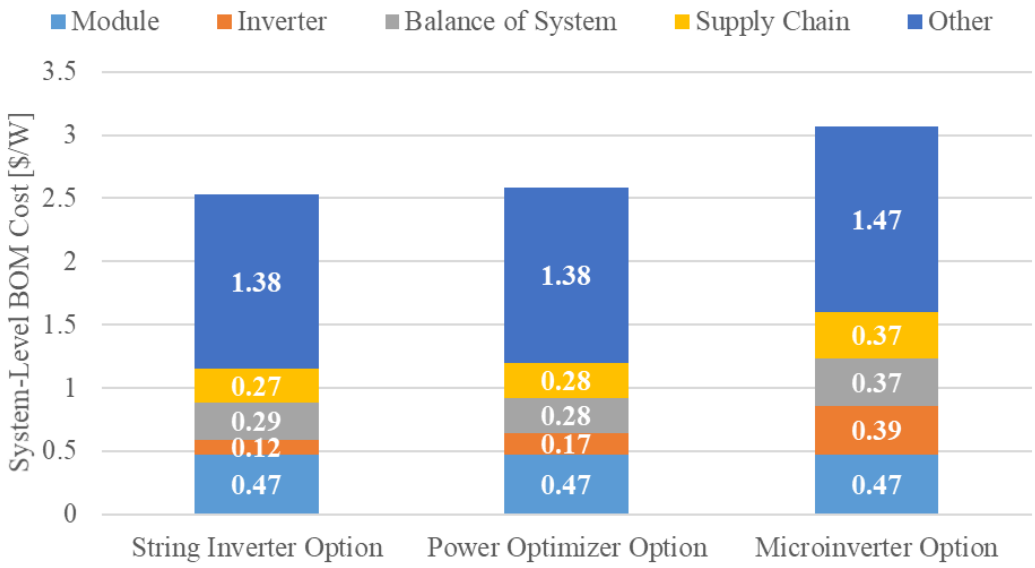


Fig. 1.3. Comparison of BOM cost breakdown for string inverter, power optimizer, and microinverter systems as of 2018 [1].

1.3. Trends in residential solar systems

There are several notable trends in residential PV systems within the microinverter architecture that are driving the future of the associated power electronics developments and the further reduction in residential LCOE costs. Ultimately, these trends will enable increased power rating of residential PV systems, at reduced system-level costs, with enhanced system-level functionality and reliability. Specific trends regarding PV panel power ratings, power electronics power density, power electronics reliability, and wide-bandgap device costs will be analyzed next, motivating the specifications of the proposed next-generation microinverter. Several trends are specifically motivated based on the production history of Enphase microinverters, the leading microinverter supplier in the United States.

1.3.1. Increased power rating of PV panel

The power ratings of PV panels in residential applications increased from 2010 to 2017 with improvements in cell technology. The average power rating of PV panels for residential solar applications has been tracked since 2010, with an increase from around 220 W in 2010 to roughly 280 W in 2017 [1]. The increase in PV panel power rating can also be corroborated by the increase in Enphase microinverter power ratings in the similar timeframe, with their third generation product rated for 190-270 W panels in 2011 [6], and their latest product rated for 235-350 W panels in 2018 [7]. In line with historical trends, a roadmap of prospective increases in PV panel power rating has been presented in [8], where increases in both cell- and module-level efficiency project increases in power level to upwards of 370 W for 60-cell panels, by 2025 [8]. Therefore, it is clear that as the PV panel power ratings continue to increase, demand for associated higher power level power electronics will grow.

1.3.2. Improved power electronics power density

Improved power density of microinverters is an important target for residential PV systems. Improved power density is desired both volumetrically with a small converter package, and gravimetrically with a small converter mass. Volumetric power density improvements can reduce wasted space within the microinverter enclosure minimizing potting material costs, as well as reducing the overall package volume and associated mechanical enclosure-related costs. On the other hand, gravimetric power density improvements help to reduce transportation related costs, as well as simplify system-level interconnections, reducing BOS related costs. Trends for Enphase microinverter gravimetric and volumetric power densities versus microinverter

generation number are presented in Fig. 1.4. It is clear that gravimetric power density is a significant metric, as each generation microinverter has achieved increases in this metric, while the volumetric power density remained within a tight range. This is due to the fact that microinverters do not necessarily require to be fit within a small space, as the microinverter can be placed anywhere underneath of the roof mounted solar panels, while the gravimetric specification affects system-level costs more directly.

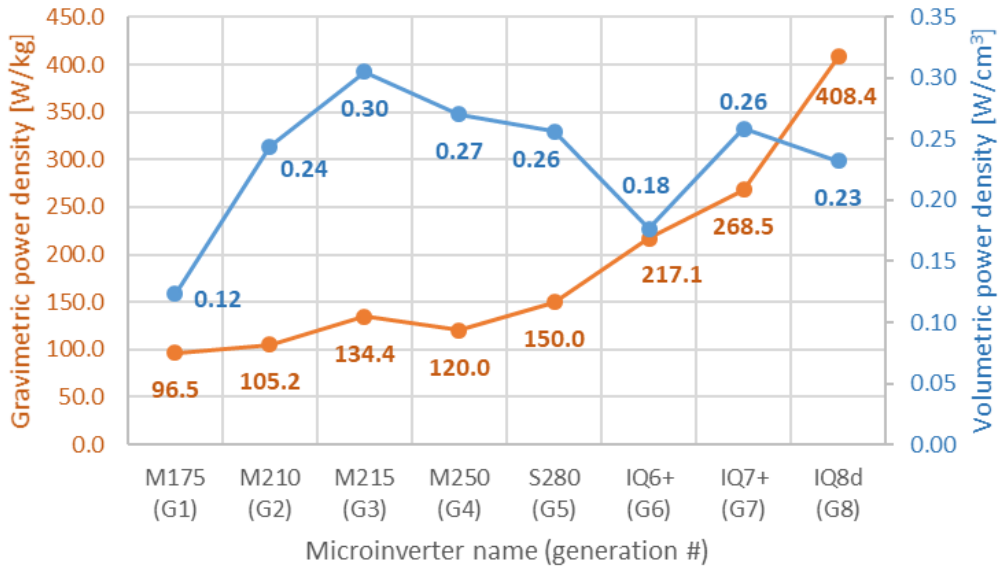


Fig. 1.4. Trend of Enphase microinverter gravimetric and volumetric power density over time.

1.3.3. Enhanced power electronics reliability

The reliability of a microinverter can be inferred from the variable operation and maintenance (O&M) costs of the residential system. This metric has been tracked since 2010 for residential PV systems in [1], where the variable cost over time is compiled in Fig. 1.5(a). It is shown that the O&M expenses have reduced from 54 $/kW/year in 2010 to 22 $/kW/year in 2018. Of the 22 $/kW/year in 2018, a further breakdown by O&M cost mechanism has been analyzed, where a significant portion of

the remaining O&M costs are due to inverter replacement, accounting for upwards of 10 $/kW/year [1]. Therefore, though the reliability of residential systems has improved since 2010, the inverter reliability still remains a bottleneck, negatively affecting residential LCOE costs.

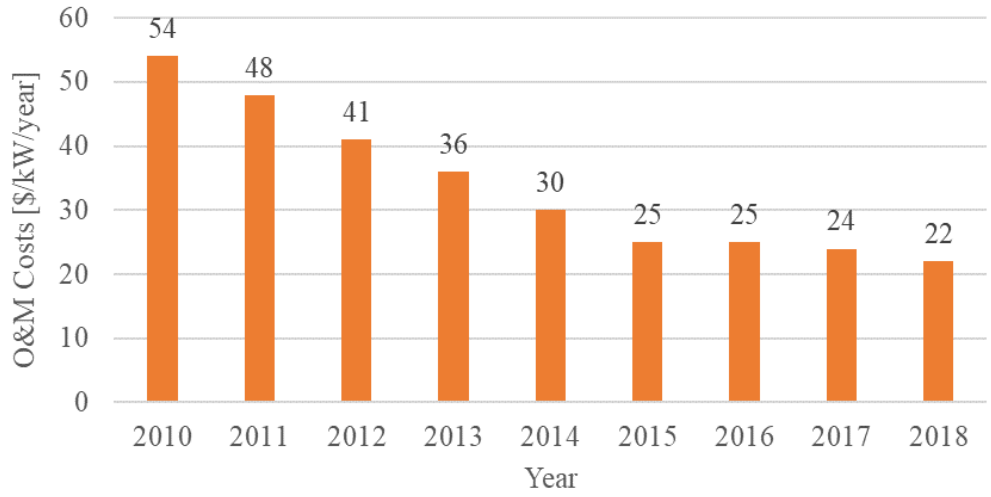


Fig. 1.5. Historical trend of O&M costs in residential PV systems from 2010 to 2018 [1].

1.3.4. Feasibility of wide band-gap semiconductors

Over the past few years, the usage of wide band-gap semiconductors has gained viability due to reducing costs and demonstrated device-level reliability. In particular, Gallium-Nitride (GaN) devices are potentially advantageous in microinverter applications, due to the high electron velocity, breakdown fields, and energy gaps, as compared to Si devices [9]. GaN devices have already reduced in cost over the last five years due to improvements in manufacturing, particularly for GaN-on-Si devices which can operate on the same fabrication lines as traditional Si devices, with higher yields due to reduced package geometries [10]. In 2015, GaN devices were projected to reduce in cost to 0.12 $/A by 2020, which has nearly been realized for many GaN devices from

leading suppliers [10]. While it is expected that GaN devices will continue to reduce, GaN device costs eventually may still be higher than that of similarly rated Si devices. With that being said, the usage of GaN devices enables improved system-level performance characteristics that enable cost reductions in other categories. For example, GaN devices can be operated at higher switching frequencies with reduced total losses, due to low parasitic capacitance and elimination of reverse-recovery charge, and hence system size can be reduced (due to high switching frequency) as well as volume related to thermal management (due to lower device losses). The final benefit of GaN which continues to grow as more research is conducted, is their superior reliability compared to similarly rated Si devices [11].

1.4. Microinverter approaches

Microinverter topologies can be generally broken down into two categories, namely non-isolated and isolated, where further breakdown describes the number of stages (typically either single-stage or two-stage) to process energy conversion from DC at the PV panel, to AC at the grid side. One of the main challenges in the power electronic converter design for PV applications is the high gain requirement from the low voltage PV panel (~30 V to ~60 V) to the high voltage, sinusoidal AC grid (~240 V_{rms}). With this in mind, typical two-stage applications adopt a front-end DC-DC converter with high-gain (either isolated or non-isolated) followed by a DC-AC converter. A comprehensive topological analysis was presented for microinverter systems from the literature in [12], where it was concluded that isolated systems are preferable due to secondary considerations including the elimination of leakage current that flows from the PV panel to the ground through unavoidable parasitic capacitances.

Furthermore, single-stage systems were identified to be preferable due to inherent benefits of low system complexity and part count, which can translate to higher power density and lower cost [12]. With that being said, leading microinverter manufacturers in the industry still adopt different approaches, such as Enphase with a single-stage topology [13], and Hoymiles with a traditional two-stage topology [14].

Aside from the large voltage gain requirement, a key challenge in microinverter structures is how to handle the inherent power mismatch between DC input and AC output. Key waveforms associated with the mismatch between fixed DC input power on the PV-side, and time-varying AC output power on the grid-side, with both a DC and sinusoidal component, is shown in Fig. 1.6. In light of the power mismatch, low frequency energy storage is required to store energy during the periods of excess generation, and supply energy during periods of excess demand, across the AC line-cycle. The most conventional approach for low frequency energy storage is to utilize a large capacitor bank at the DC input of the microinverter, which can be designed according to,

$$C_{in} = \frac{P_{in}}{V_{in}\Delta V_{in}\omega_g} \tag{1.4}$$

where P_{in} is the maximum input power of the system, V_{in} is the input voltage at the maximum input power, ΔV_{in} is the tolerated voltage ripple, and ω_g is the AC grid frequency. In an example application of a 400 W PV panel at 40 V and a tolerated voltage ripple of 1%, the required input capacitance can be calculated to be 6.6 mF, which will serve as a point of reference for latter analysis. This large capacitance bank can only be realized by the parallel connection of low voltage electrolytic capacitors,

which have associated reliability concerns [15]. While lower capacitance could be tolerated at the cost of increased input voltage ripple, the operation of the PV panel will experience fluctuation during the AC line cycle, and hence the PV panel maximum power may not always be able to be extracted.

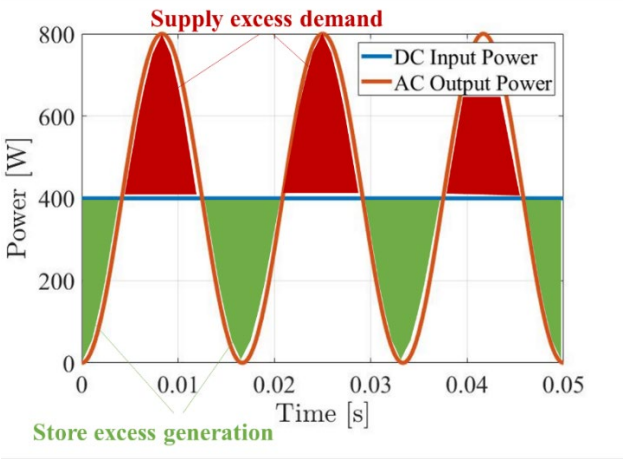


Fig. 1.6. Illustration of the inherent power mismatch between PV-side DC power and grid-side AC power, necessitating the use of low frequency energy storage.

1.5. Main goals and objectives

In light of the discussion surrounding the current state-of-the-art in power electronics for residential solar applications, and the associated trends, this dissertation targets a holistic design approach for next-generation microinverters (NGM) in residential PV applications, using emerging GaN power semiconductor devices. The proposed topological approach and subsequent design optimization analyses aim at reducing the microinverter bill-of-material (BOM) cost from several angles, while also enhancing the reliability, compared to state-of-the-art microinverter solutions. Additional more specific targets include high CEC efficiency, power density greater than 0.6 W/cm^3, and specific power greater than 400 W/kg. In line with the trends in PV deployment, the NGM prototype will be designed for an AC power rating of 400

VA and be compatible with PV panels that have a maximum power point (MPP) voltage between 30 V and 60 V (40 V nominal), with an MPP tracking efficiency greater than or equal to 99%. The output of the microinverter will be a 240 V grid, and the control-related design will comply with current and next-generation US grid-side standards such as IEEE 1547, and CA rule 21.

The microinverter will be realized by the isolated, single-stage, DC-AC indirect matrix converter (IMC) topology with a parallel-connected boost-type active power decoupling (APD) filter at the input, shown in Fig. 1.7. Compared to traditional microinverter approaches that utilize a large, low-lifetime, electrolytic capacitor bank to mitigate the double line frequency (DLF) ripple at the DC input, the size, required input capacitance, and reliability of the system can be significantly improved by employing the illustrated active filter circuitry. While the finalized topology is presented in Fig. 1.7, this dissertation will outline certain design- and system-level analyses that motivate the topological selection, as well as the component-level selections. In particular, a new approach for accurate main-circuit steady-state modeling will be proposed that accurately replicates experimental hardware performance even as the circuit is operated at high frequency. Next, a design optimization routine will be developed to select parametric values for the main-circuit transformer. Due to limitations in the original transformer design, a novel leakage-integrated transformer will be presented, which is advantageous over other state-of-the-art approaches considering geometrically optimized designs. Finally, a holistic system-level optimization procedure will be developed for the APD, to select all components and minimize cost, power density, and efficiency drop. Following the technical

sections, general conclusions will be drawn about the current state of the research, and required future areas of research will be discussed.

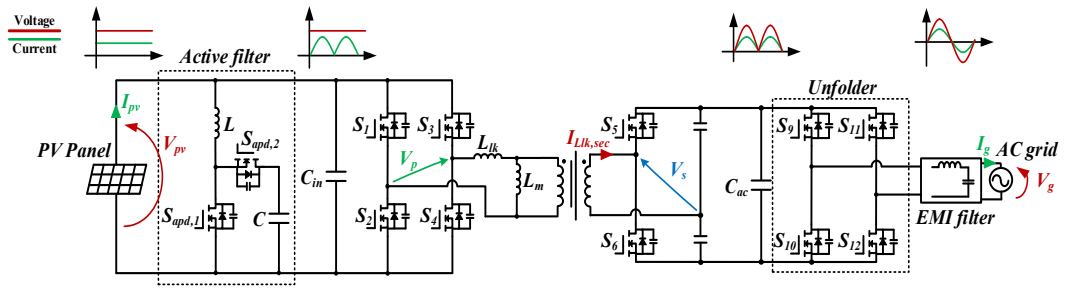


Fig. 1.7. Proposed NGM circuit topology with a parallel boost-derived active filter at the input side, followed by a single-stage DAB circuit with a line-frequency unfolder.

Chapter 2. Steady-State Modeling of DAB-Based Converters

The dual-active bridge (DAB) DC-DC converter remains one of the most popular choices for bidirectional DC-DC applications due to its advantages such as the absence of turn-off voltage spikes across switches and possibility of full zero-voltage-switching (ZVS) operation [16]. One such realization of the DAB converter is shown in Fig. 2.1, with a primary-side full-bridge and a secondary-side half-bridge. In this chapter, accurate modeling of the DC-DC steady-state performance of DAB-based converters will be developed. First, the principle of operation of the DAB will be analyzed, followed by analysis of ideal modeling techniques, particularly in the frequency-domain. While the presented ideal modeling technique will be shown to agree with ideal simulations, the inclusion of non-idealities in the system will invalidate the accuracy of the ideal model when running more accurate simulations, representative of experimental operating conditions. As such, an improved analytical modeling tool in the frequency-domain will be developed to facilitate improved prediction accuracy, confirmed by comparison to both simulation and hardware experiments. A portion of the analysis and results presented in this chapter are published in [17].

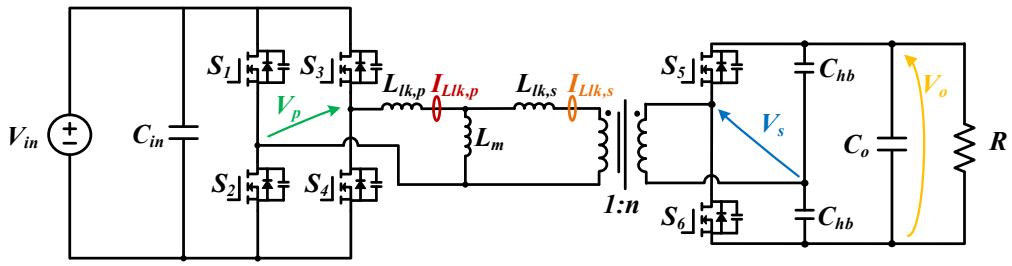


Fig. 2.1. DC-DC DAB circuit topology with a primary-side full-bridge and secondary-side half-bridge, connected through a high-frequency transformer represented by the T-model.

2.1. Traditional DAB steady-state modeling techniques

Steady-state analysis of the DC-DC DAB converter can be carried out using either time-domain-modeling (TDM) or frequency-domain-modeling (FDM) approaches. TDM proceeds by analyzing circuit operation in one of several modes, which arise due to the changing voltages of the two sides of the transformer and the relative value of the modulation parameters [18]-[22]. As such, FDM was developed in [23] to significantly simplify modeling efforts into a single set of equations that are always valid. While sufficient literature has been published regarding idealized DAB circuit operation with TDM and FDM, the principle limitation of the approaches in [18]-[23] is that they neglect to consider the effect of finite rise- and fall-times (t_r, t_f) of the devices during ZVS transitions, which will be shown to be critical to accurate analysis.

A TDM approach incorporating ZVS transitions based on the state-plane analysis has been developed in [24] on a 1 MHz DAB converter. While the analysis inherently includes the impact of switching transitions, state-plane analysis of the DAB is mode-dependent, which leads to non-generic analytical descriptions of the converter. A TDM approach for predicting ZVS boundaries is presented in [25]. However, this approach is based upon achieving ZVS "by-direction" and hence in certain instances can prove to be inaccurate, and further does not investigate the impacts that the switching transitions have on the operational characteristics of the system. Another TDM approach is presented in [26] with accurate ZVS analyses provided that the current at the start of the resonant transition is in the correct direction. While the impact

of ZVS on the effective phase-shift perturbation is identified, the mechanisms by which this occurs and implications to power transfer and RMS currents are not present.

Accurate charge-based considerations for ZVS were incorporated into the FDM approach in [23], however the implications of ZVS transitions were not incorporated into power flow and RMS current estimation. An admittance-matrix-based FDM approach for analyzing ZVS boundaries of DAB converters was presented in [27], where the ZVS boundaries are initially determined by analyzing "by-direction" considerations of the switching-leg's current, and ensuring that the current remains in the correct direction throughout the dead-time period is concluded to achieve ZVS fully. However, this will likely yield error for instance if inadequate dead-time duration is provided to fully undergo the ZVS transition, or if the initial energy at the start of certain ZVS processes is insufficient. In fact, the DAB inductor current for secondary-side device transitions can begin in the wrong direction and still achieve ZVS due to the inherent behavior of the current slope [24]; this is not accounted for in the ZVS boundary analyses in [25]-[27].

An iterative-based time-domain approach for waveform reconstruction was necessitated in [28] for accurate system modeling and loss analysis, however explicit details of the reconstruction method were not specified, and the implications of finite rise and fall times to effective operating parameters was not explored.

Therefore, considering the drawbacks of previous approaches in both time and frequency domains, and the need for such a detailed modeling tool, an improved analytical modeling (IAM) approach in the frequency domain is proposed in this chapter for the high-frequency DC-DC DAB converter, that could be generally

extended to any other DAB-based converter approach. The contributions of this chapter are to, 1) create a generic model of the DAB DC-DC converter in which the finite device commutation times are accurately considered, and is applicable even in high frequency applications, 2) analyze the impact of finite device transition times from perspectives of power transfer and RMS current, 3) accurately predict the ZVS performance of all device commutations including how much dead-time to provide to all transitions and how much residual voltage remains in quasi-ZVS (qZVS) scenarios, and 4) reconstruct time-domain waveforms from the frequency-domain with high accuracy to detailed simulation and experimental results.

2.2. DAB steady-state principle of operation

In any DC-DC operating point, the DAB topology in Fig. 2.1 can be reduced to the equivalent circuit representation in Fig. 2.2. In particular, the switching networks have been reduced to quasi-square-wave voltage sources, which will be clearer in the subsequent section. In steady-state, the input and output voltages of the converter are assumed to be constant, as the input and output capacitors are designed to maintain tight voltage ripples.

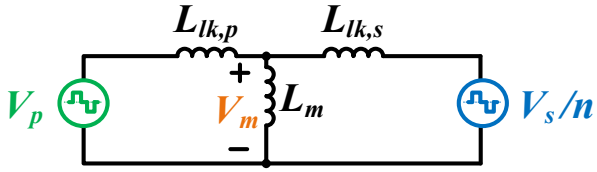


Fig. 2.2. DC-DC DAB equivalent circuit with primary- and secondary-side quasi-square-wave voltage sources separated by the transformer T-model inductance network.

In the equivalent circuit, two quasi-square-wave voltages are applied are either side of an inductive network. The inductive network shown is based on the transformer T-

model, consisting of primary- and secondary-side leakage inductances separated by a parallel branch magnetizing inductance. In the proposed converter, all required inductances in the power transfer process will be realized by the transformer, which will be analyzed in further detail in Chapter 4. In general, to transfer power from the primary-side to the secondary-side, the switching signals must be generated such that the fundamental harmonic component of the primary-side voltage *leads* the fundamental harmonic component of the secondary-side voltage.

The transformer applied voltages and currents are shown for three example operating points in Fig. 2.3. Each of the operating points are taken with V_{in} = 40 V, V_{out} = 240 V, n = 4, $L_{lk,p} = L_{lk,s}$ = 0.625 μH, and L_m = 40 μH. In the first case shown in Fig. 2.3(a), two square-wave voltages are applied on the primary- and secondary-sides to highlight the leading nature of the relative voltages through the use of the first modulation control variable, δ. In the second case shown in Fig. 2.3(b), a quasi-square-wave voltage is generated on the primary-side, through the use of control variable, θ. In a third case presented in Fig. 2.3(c), the switching frequency, f_{sw}, was varied with respect to the first and second cases, highlighting the usage of a third control variable.

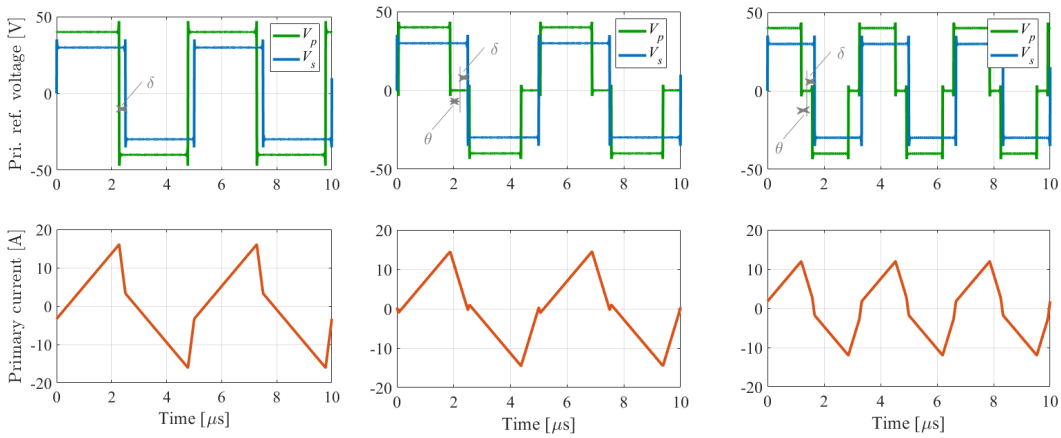


Fig. 2.3. Example operating points demonstrating possible variation of the DAB circuit modulation parameters, while ensuring primary-to-secondary power flow, (a) phase-shift variation, (b) phase-shift and zero-state variations, and (c) phase-shift, zero-state, and switching frequency variation.

To select and optimize the values of the control parameters at all operating points, the desired operating characteristics should be formulated, as infinitely many combinations of the control variables could result in the same amount of power transfer. As shown in Table 2.1, all three operating points in Fig. 2.3 have equivalent amounts of active power transfer, but differing values of transformer RMS current. Specifically, control variable combinations that achieve the lowest amount of total loss would be the most desirable, to maximize the circuit efficiency. More details regarding the optimization of control variables will be detailed in Chapter 3, built upon the analytical formulation of the circuit operating principle introduced in the next section.

Table 2.1. Numerical comparison of example operating points shown in Fig. 2.3.

Example case	θ	δ	f_{sw} [kHz]	$I_{rms,p}$ [A]	P [W]
1	0	0.046	200	8.67	198
2	0.068	0.057	200	8.06	198
3	0.059	0.083	300	7.38	198

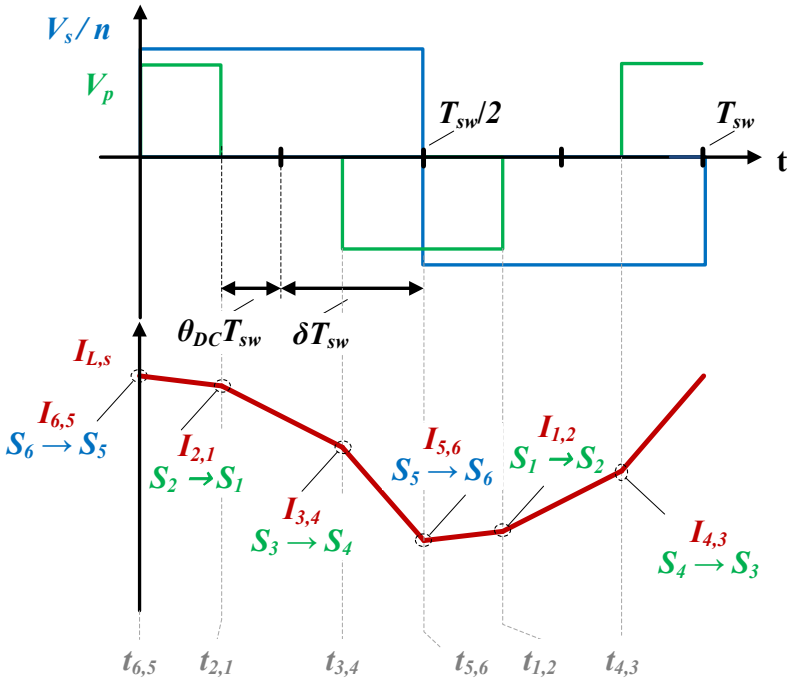
2.3. Ideal steady-state modeling in DAB converters

The ideal modeling of DAB converters takes several principal assumptions. First, the quasi-square-wave voltage waveforms achieve level transitions with zero rise-time and fall-time. As such, the Fourier decomposition of these voltages, and subsequent calculation of other circuit quantities, is straightforward to perform. The second assumption is that the input and output capacitors are designed such that the terminal voltage ripples are negligible, and hence the input and output capacitances can be modeled as ideal voltage sources. The third assumption is loss-less operation, where power is transferred with unity efficiency. Finally, the devices and transformer are considered to be ideal, and as such inherit no resistance or parasitic capacitance and inductance. Under these assumptions, a frequency-based Superposed Harmonic Analysis (SHA) model was utilized to analyze any mode of operation of the DAB-based circuit in Fig. 2.2. The SHA model, henceforth deemed the Original Analytical Modeling (OAM), is used to determine the total amount of power transfer, and transformer RMS current, given values of input and output voltage and a modulation parameter set $\{\theta, \delta, f_{sw}\}$.

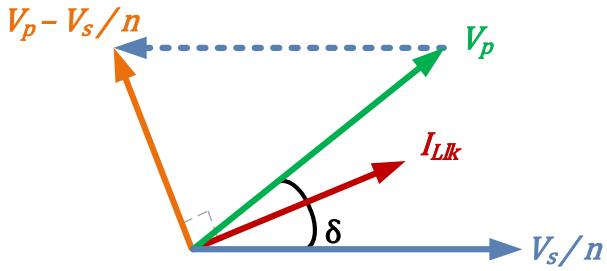
2.3.1. Frequency-domain modeling

To develop the SHA model, the values of the transformer voltages and currents must be derived for any arbitrary frequency, *'k'*. To aid the visualization of the frequency-domain modeling, an ideal time-domain waveform of the circuit waveforms and an associated vector diagram is presented in Fig. 2.4. For the following analysis it is assumed that the equivalent circuit is reflected to the primary-side of the transformer, as clear from Fig. 2.2. For notational simplicity, timing instants are defined via $t_{a,b}$,

where a is the outgoing switch index, and b is the incoming switch index (e.g. the timing of the turn-off of S_6 and turn-on of S_5 is deemed $t_{6,5}$).



(a)



(b)

Fig. 2.4. DAB equivalent circuit (a) example ideal waveforms, and (b) associated vector diagram of the circuit operation at an example harmonic.

Performing Fourier decomposition of the quasi-square-wave primary and secondary-side voltages yields their associated `k^{th}' harmonic vectors,

$$\overrightarrow{V_{p,k}} = \frac{4V_{in}}{k\pi}\cos(2\pi k\theta_{dc}) \angle 2\pi k\delta \tag{2.1}$$

$$\overrightarrow{V_{s,k}} = \frac{4V_o}{2nk\pi}\angle 0 \tag{2.2}$$

It is clear from Fig. 2.4(b) and (2.1)-(2.2) that the primary-side voltage vector is controlled to lead the secondary-side voltage vector by the angle $2\pi k\delta$. With the primary- and secondary-side voltages derived, the magnetizing voltage vector at the 'k^{th}' harmonic can be derived via,

$$\overrightarrow{V_{m,k}} = \overrightarrow{V_{p,k}}\,\Lambda_p + \overrightarrow{V_{s,k}}\Lambda_s, \tag{2.3}$$

$$\Lambda_x = \frac{\lambda_x}{1 + \lambda_p + \lambda_s} \tag{2.4}$$

$$\lambda_x = \frac{L_m}{L_{lk,x}} \tag{2.5}$$

where $x = \{p, s\}$ corresponding to the primary- and secondary-side, respectively. In many cases, the transformer design may be such that the magnetizing inductance is much greater than the leakage inductances (i.e. $L_m >> L_{lk,p(s)}$), and the leakage inductances on either side of the transformer are equal (i.e. $L_{lk,p} = L_{lk,s}$). Under these assumptions, the magnetizing inductance is simplified to be the mean of the applied primary- and secondary-side voltages, i.e. $\overrightarrow{V_{m,k}} = \left(\overrightarrow{V_{p,k}} + \overrightarrow{V_{s,k}}\right)/2$. However, this may not always be true, and as such the more generic formulation is utilized moving forward.

With all voltages in the circuit derived in the frequency-domain, the inductor current vectors at any 'k^{th}' harmonic can be determined by,

$$\overrightarrow{I_{p,k}} = \left[\frac{\overrightarrow{V_{p,k}}}{k\omega_{sw}L_{lk,p}}(1-\Lambda_p) - \frac{\overrightarrow{V_{s,k}}}{k\omega_{sw}L_{lk,p}}\Lambda_s\right]\angle -\frac{\pi}{2} \tag{2.6}$$

$$\overrightarrow{I_{s,k}} = \left[\frac{\overrightarrow{V_{p,k}}}{k\omega_{sw}L_{lk,s}}\Lambda_p - \frac{\overrightarrow{V_{s,k}}}{k\omega_{sw}L_{lk,s}}(1-\Lambda_s)\right]\angle -\frac{\pi}{2} \tag{2.7}$$

With the primary- and secondary-side current vectors derived, the total RMS currents on both sides of the transformer can be easily derived based on their current magnitudes via Parseval's theorem,

$$I_{x,RMS}^2 = \frac{1}{2}\sum_{k=1,odd}^{k_{max}} \left|\overrightarrow{I_{x,k}}\right|^2. \tag{2.8}$$

In particular, the summation here is shown to only include odd harmonics, as the waveforms exhibit odd-symmetry over a given half-switching-period. Finally, with the frequency-domain voltages and currents, the active power transfer at any 'k^{th}' harmonic can be derived and summed to determine the total power transfer with,

$$P_{x,k} = \frac{1}{2}\left|\overrightarrow{V_{x,k}}\right|\left|\overrightarrow{I_{x,k}}\right|\cos\left(\angle\overrightarrow{V_{x,k}} - \angle\overrightarrow{I_{x,k}}\right) \tag{2.9}$$

$$P_x = \sum_{k=1,odd}^{k_{max}} P_{x,k} \tag{2.10}$$

As initially detailed, the frequency-domain approach is powerful for its generality, as the circuit quantities of current and power transfer can be determined with a single-set of equations. Furthermore, the time-domain waveforms of voltage and current can be reconstructed with a harmonic sum of the relevant quantities. In particular, time-

domain reconstruction of the current waveforms is desirable to perform additional analysis regarding the performance of the switching transitions. The time-domain profile of the inductor current can be attained through,

$$I_x(r) = \sum_{k=1,odd}^{k_{max}} \left|\overrightarrow{I_{x,k}}\right| \sin\left(kr + \angle\overrightarrow{I_{x,k}}\right). \tag{2.11}$$

where r is a radian value between 0 and 2π. In particular, the radian notation is utilized as it is more generic and compact than the time-domain form (i.e. $r = k\omega_{sw}t$).

2.3.2. Comparison of OAM to ideal simulation

To validate the SHA model, a comparison was made with a DC-DC DAB converter simulation in MATLAB Simulink with the same fixed control parameters. An example of the results from the SHA model and converter simulation is shown in Fig. 2.5, where V_{in} = 40 V, V_{out} = 240 V, n = 4, $L_{lk,p}$ = 1.25 μH, f_{sw} = 200 kHz, θ_{dc} = 0.05, and δ = 0.2. The results clearly demonstrate the accuracy of the SHA model, as the two current waveforms are closely aligned. Based on its accuracy, the SHA model can be used analytically to modulate the control parameters to achieve an optimal commutation strategy.

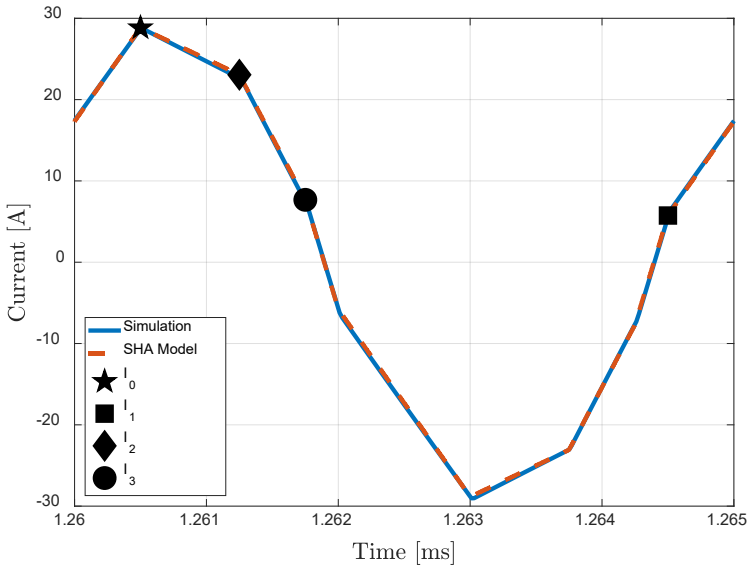


Fig. 2.5. Comparison between SHA model and converter simulation.

2.3.3. Commutation analysis in DAB converters

One of the main differences between ideal simulation and realistic hardware operating conditions is the consideration of the device dead-times, and associated voltage commutations of the devices during the dead-time. As such, it is necessary to examine the circuit operation during the dead-time. The equivalent circuit during an example switching transition of the secondary-side half-bridge leg is shown in Fig. 2.6.

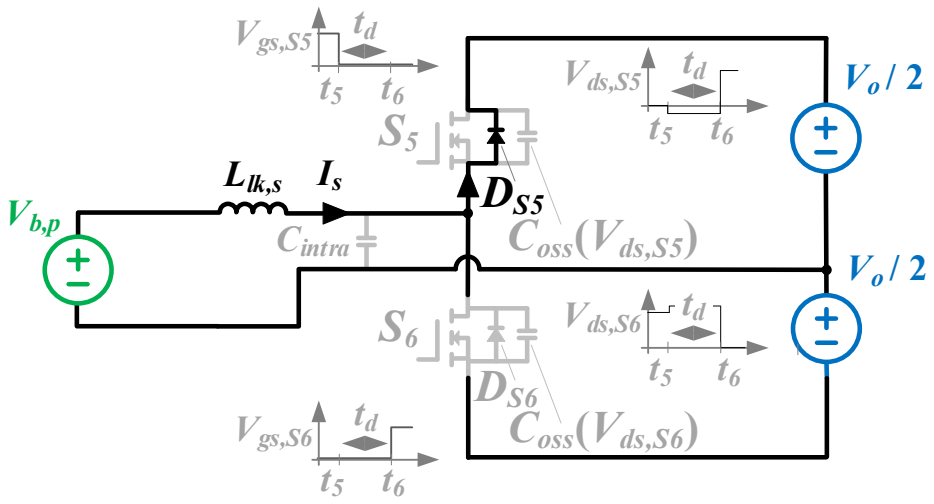


Fig. 2.6. Example equivalent circuit after the turn-off of switch S_5, when the current is in the improper direction to enable soft-switching.

The equivalent circuit consists of the two devices in one half-bridge leg, the other leg half-bridge capacitors realized by two voltage sources, the transformer's series inductance, the transformer's parasitic intra-winding capacitance, and an effective voltage source realized by the voltage applied from the opposite side of the transformer. Notably, the device output capacitance is non-linear and a function of the voltage across the device at any time, hence denoted $C_{oss}(V_{ds})$. If the current in the switching node is a particular direction, e.g. positive in Fig. 2.6, the device anti-parallel diode (or other reverse conduction mechanism) will conduct and the leg's applied voltage will remain mostly unchanged until the other device turns on. This operating case is deemed "hard-switching" because the incoming device, S_6, must realize a full voltage transition from V to 0, and a current transition from 0 to I_L, in a finite time, which incurs loss.

Conversely, if the transformer current is in the opposite direction, the device parasitic capacitors will realize the conduction path as shown in Fig. 2.7.

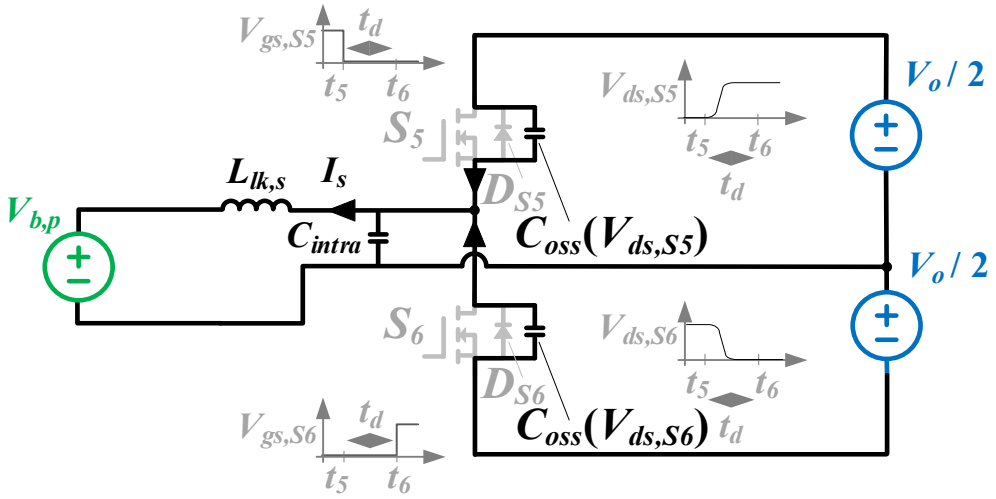


Fig. 2.7. Example equivalent circuit after the turn-off of switch S_5, when the current is in the proper direction to enable soft-switching.

In this case, a resonance will take place between the parasitic capacitors and inductor, facilitating the discharge of the incoming switch capacitance and a charging of the outgoing switch capacitance. If enough energy is present in the inductor prior to the initiation of the switching transition, and enough dead-time is provided between the switching signals, the incoming device can fully conduct the current with near-zero voltage prior to being turned on. This process is determined "soft-switching", often referred to as ZVS turn-on, and is a near loss-less process. Based on the equivalent circuit, equations for the currents in the three capacitors can be simplified to reveal their effective parallel connection,

$$i_{C_{oss}S5}(t) = C_{oss}(V_{ds,S5})\frac{dV_{ds,S5}(t)}{dt} \tag{2.12}$$

$$i_{C_{oss}S6}(t) = -C_{oss}(V_{ds,S6})\frac{dV_{ds,S6}(t)}{dt} = C_{oss}(V_o - V_{ds,S5}(t))\frac{d(V_{ds,S5}(t) - V_o)}{dt} \quad (2.13)$$

$$i_{C_{intra,s}}(t) = -C_{intra,s}\frac{d(V_o/2 - V_{ds,S5}(t))}{dt} \quad (2.14)$$

$$\begin{aligned} i_L(t) &= i_{C_{oss}S5}(t) + i_{C_{oss}S6}(t) + i_{C_{intra,s}}(t) \\ &= \left[C_{oss}(V_{ds,S5}) + C_{oss}(V_o - V_{ds,S5}) + C_{intra,s}\right]\frac{dV_{ds,S5}(t)}{dt} \\ &= C_x(V_{ds,S5})\frac{dV_{ds,S5}(t)}{dt} \end{aligned} \quad (2.15)$$

2.3.4. Comparison to detailed simulation

In circuit hardware implementation, many circuit non-idealities are present that are typically ignored in the ideal modeling stage. In particular, the non-idealities result in several of the operating assumptions to be broken, namely the finite rise- and fall-times of the transformer applied voltages, and the required inclusion of the non-idealities associated with the device and transformer parasitic capacitances, as introduced in the previous section. Table 2.2 highlights the considered transformer turns ratio, leakage inductance, transformer parasitic capacitance, and operating frequency of the following simulation cases.

Table 2.2. Parameters utilized in comparative analyses.

n	$L_{lk,p}$ & $L_{lk,s}$ [μH]	L_m [μH]	$C_{intra,p}$ [pF]	$C_{intra,s}$ [pF]	f_{sw} [kHz]
4.28	0.6275	80	384	22	200

Furthermore, realistic devices were selected with detailed device models imported from the respective manufacturers. The GaN-based EPC2001C [29] was selected for the primary-side whereas the Si-based IPD60R180P7 [30] was selected for the secondary-

side. The dead-times provided to the primary- and secondary-side switches were 100 ns and 600 ns, respectively.

Four cases were considered where in each case the input voltage was set to 40 V, and the output voltage and modulation parameters were varied. The controller parameters δ and θ (f_{sw} was fixed for all cases as detailed in Table 2.2) were fed to a modulator, providing the appropriate gating signals to the devices. The results are summarized in Table 2.3, where it is clear that the ideally predicted values of power transfer and RMS current deviate quite significantly in most cases from the detailed simulation in LTspice.

Table 2.3. OAM vs. LTspice for several DC-DC operating points.

Case	V_{out} [V]	Analysis	δ_{eff}	θ_{eff}	$I_{rms,s}$ [A]	P [W]
Sim. 1	340	OAM	0.03	0	1.61	245
		LTspice	0.045	0	2.11	328
Sim. 2	194	OAM	0.077	0.12	1.71	130
		LTspice	0.12	0.122	3.34	280
Sim. 3	107	OAM	0.093	0.19	1.67	59
		LTspice	0.12	0.191	1.33	48
Sim. 4	54	OAM	0.1	0.22	0.64	11
		LTspice	0.135	0.225	0.73	11.5

In particular, deviation between OAM and LTspice derived from the fact that the δ_{eff} has been perturbed significantly from the expected δ provided to the system. Notably, the θ parameter has not differed much between expected value and the simulation. In this case, perturbation of δ is more prominent than θ due to the low required dead-time of the GaN-based EPC2001C devices, and hence low ratio of

t_{dead}/T_{sw} in instances of soft-switching, whereas the secondary-side Si devices require a longer dead-time for device commutation. While the perturbation of δ could potentially be managed through the use of a closed-loop controller, it is important in the design and analysis stage of the converter to be able to accurately replicate expected behavior, particularly in regards to ZVS range (impacting switching loss) and RMS currents (impacting conduction loss).

The described modulation parameter perturbation can be explained with Fig. 2.8, a modification of that from Fig. 2.4(a), where the idealized operating behavior of the converter is shown alongside a first-order approximation of the accurate operating characteristics. For both the primary- and secondary-side voltage waveforms, the gating signals and device dead-time is explicitly shown. Three unique cases occur in this diagram to highlight the different ways in which the device dead-time may influence the converter operation. First, the $S_2 \leftrightarrow S_1$ transition on the primary-side and the $S_6 \leftrightarrow S_5$ transition on the secondary-side achieve ZVS. However, the $S_2 \leftrightarrow S_1$ transition is shown to complete in a much shorter duration than the $S_6 \leftrightarrow S_5$ transition. As such, the effective zero-crossing of the secondary-side transformer voltage (and hence the fundamental harmonic component of the secondary-side voltage) has inherent phase delay with respect to the ideal square-wave. Furthermore, the direction of the inductor current for the $S_3 \leftrightarrow S_4$ is incorrect for ZVS, and hence the transition is hard-switched after the allotted dead-time. In this case, the effective zero-state of the primary-side transformer applied voltage is slightly longer than otherwise predicted by the OAM. As such, the fundamental of the primary-side voltage is shifted, and the effective zero-state control parameter is perturbed. Due to these effects, it is clear that

the ideal modulation parameters, δ and θ, are perturbed to be δ_{eff} and θ_{eff}. Therefore, it is critical to incorporate the rise- and fall-times into the frequency-domain modeling for prediction accuracy, carefully incorporating the parasitic capacitances of the devices and transformer.

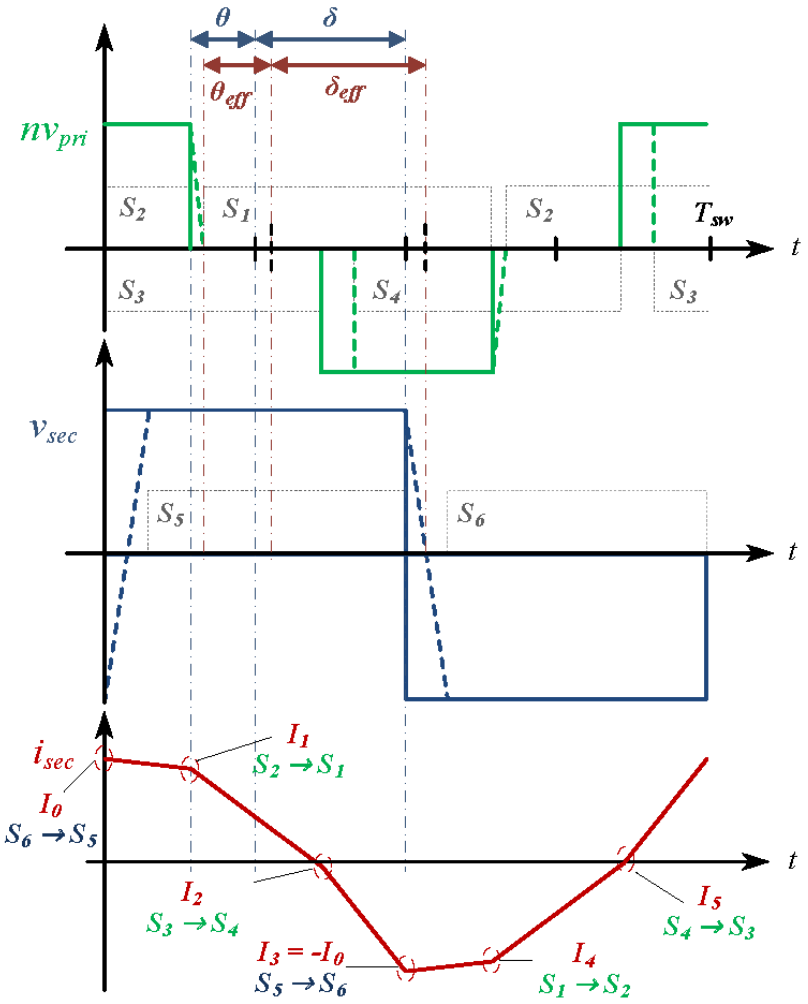


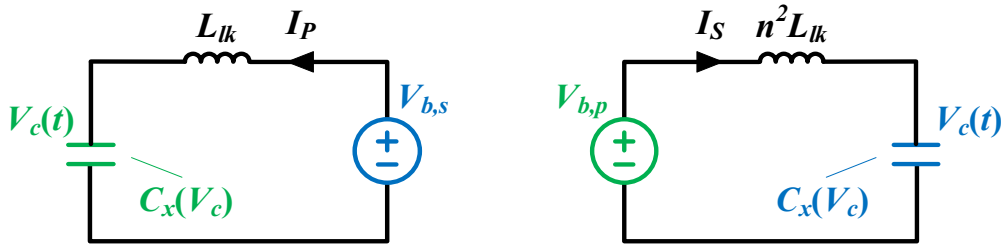
Fig. 2.8. DC-DC DAB more-accurate operational waveforms. The dotted lines indicate gating waveforms of the respective devices, the solid lines demonstrate ideal waveform behavior, and the dashed lines incorporate a linearized example of finite rise- and fall-time transitions. As a result, a difference between the modulator provided δ and θ, and δ_{eff} and θ_{eff}, are realized and shown explicitly. In this case, the $S_3 \leftrightarrow S_4$ transitions are hard-switched, while $S_1 \leftrightarrow S_2$ and $S_5 \leftrightarrow S_6$ transitions are soft-switched with finite transition times, both uniquely attributing to deviation between ideal and effective modulation parameters.

2.4. Improved analytical steady-state modeling of DAB converters

In facilitating an improved analytical model of the DAB converter, it is important to accurately model the charging and discharging dynamic of all parasitic capacitances during device dead-times. As such, this section will detail ZVS analysis in DAB converters, followed by a procedure for integrating these analyses into the frequency-domain modeling.

2.4.1. Switching transition circuit modeling

In the DAB converter, switching transitions occur on both the primary- and secondary-sides. As such, equivalent circuits during the switching transition can be derived as shown in Fig. 2.9, originally proposed in [31]. It is shown that the equivalent circuit during the device dead-time in a ZVS scenario consists of a non-linear capacitor $C_x(V_c)$ derived previously in (2.15), the total transformer series inductance reflected to one side, $L_{lk,x}$, and an effective voltage source $V_{b,x}$.



(a) (b)

Fig. 2.9. Equivalent circuit of ZVS transitions on the (a) primary-side, and (b) secondary-side.

As introduced in Section 2.2, the modulation parameters δ and θ vary the way in which the ideal voltages are applied across the transformer. As such, the effective blocking voltage appearing on the opposite site of the transformer as the commutation under interest, is dependent on the relative modulation parameters. For the three unique

commutations of the main-circuit, the value of blocking voltage was determined as a function of the relative modulation parameters, shown in Table 2.4. While only two different modes of operation are present considering control of δ and θ, many modes exist in realizations of the DAB converter with a secondary-side full-bridge, as an additional zero-state control is enabled, and in control implementations that additionally consider leg-level duty-cycle [20]. It will be shown moving forward that the proposed algorithm does not need to perform any modal analysis.

Table 2.4. Blocking voltage for the equivalent circuit in Fig. 2.9.

Transition	V_b	Condition
$S_1 \rightarrow S_2$	$V_{out}/2n$	$\delta > \theta$
	$V_{out}/2n$	$\delta < \theta$
$S_1 \rightarrow S_2$	$V_{out}/2n$	$\delta > \theta$
	$-V_{out}/2n$	$\delta < \theta$
$S_1 \rightarrow S_2$	nV_{in}	$\delta > \theta$
	0	$\delta < \theta$

2.4.2. Switching transition scenarios

Within any switching transition, three distinct possibilities may occur: 1. Full ZVS in Fig. 2.10(a) and (e), 2. quasi-ZVS (qZVS) in Fig. 2.10(b),(c),(f) and (g), and hard-switching in Fig. 2.10(d). As introduced in Section 2.3.3, for ZVS or qZVS to occur, the current must be in the correct direction to begin the charge and discharge process of the parasitic capacitances (e.g. $I_{Llk,s} > 0$ for the $S_6 \rightarrow S_5$ transition in Fig. 2.7). With that being said, it is possible for the current to begin in the wrong direction before a current zero-crossing into the correct direction during the device dead-time, deemed t_x', initiating the resonant transition. In these cases, a period of third-quadrant

device conduction (cf. Fig. 2.6) would occur before the resonant period (cf. Fig. 2.7). As such, these transitions are denoted delayed-ZVS (d-ZVS) and delayed-qZVS (d-qZVS).

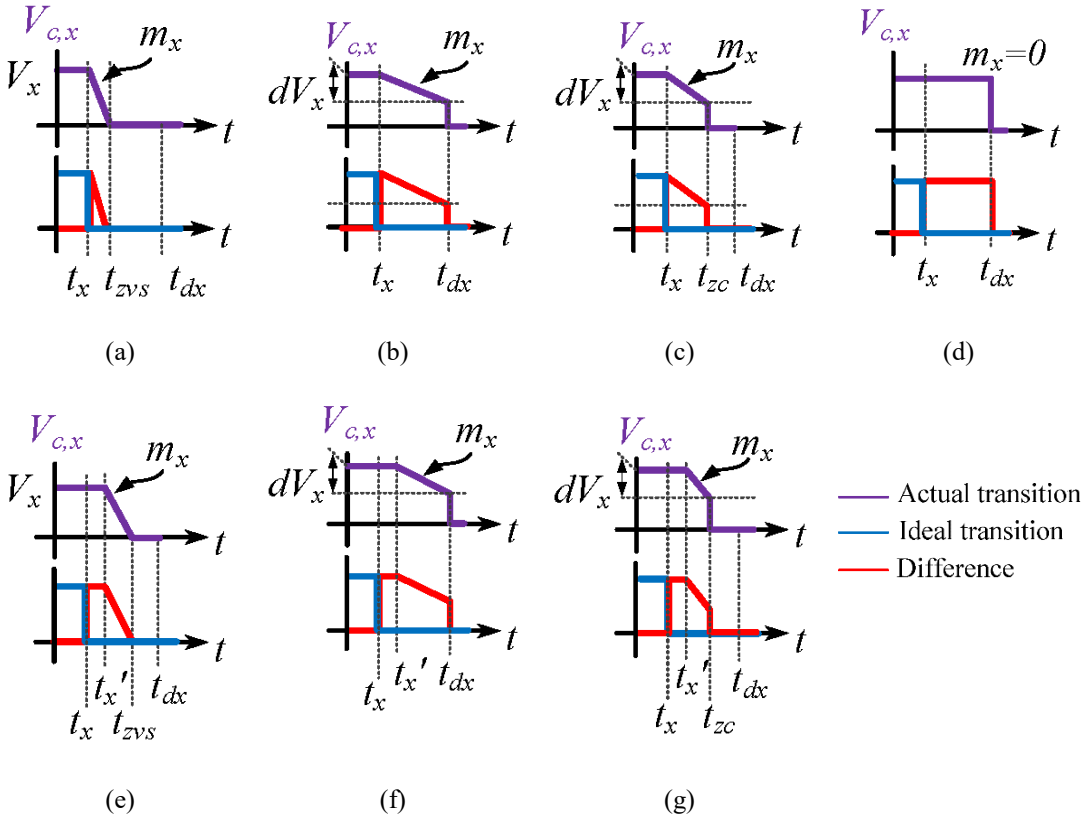


Fig. 2.10. All possible transition scenarios following the turn-off of a switch: (a) ZVS, (b) qZVS-TR, (c) qZVS-ER, (d) hard-switching, (e) d-ZVS, (f) d-qZVS-TR, (g) d-qZVS-ER..

Combining the equivalent circuit in Fig. 2.9 with the appropriately determined blocking parameters $V_{b,\bar{x}}$, L_{lk}, and C_x from Table 2.4, the total time required for a ZVS transition, with an initial transformer current $I_{L,0} = I_{Llk,x}(t_x)$, can be calculated via,

$$t_{zvs} = \int_0^{V_x} \frac{C_x(v_c)dv_c}{\sqrt{I_{L,0}^2 + \frac{2}{L_{lk,x}}\int_0^{v_c} C_x(v)\left(V_{b,\bar{x}} - v\right)dv}} \tag{2.16}$$

derived in [31]. Using this, the effective time-equivalent capacitance, $C_{eq,t,}$ can be calculated by numerically solving,

$$t_{zvs} = C_{eq,t}\int_0^{V_x} \frac{dv_c}{\sqrt{I_{L,0}^2 + \frac{C_{eq,t}}{L_{lk,x}}\left(2V_{b,\bar{x}}v_c - v_c^2\right)}}. \tag{2.17}$$

The previous equations facilitate a linear approximation to the highly non-linear voltage commutation using a fixed value time-equivalent capacitor. The time-equivalent capacitance is significant to consider as it is a linear capacitance which results in voltage variation in the same amount of time as the non-linear capacitor. In particular for ZVS transitions, the equivalent capacitor voltage will rise from 0 to V_x in the time duration t_{zvs}.

The borderline between ZVS and qZVS is determined by both time- and energy-related constraints. In the hardware it is often appropriate to select a maximum allowable amount of dead-time, t_{dx}, which will determine the borderline between ZVS and qZVS from a time-related perspective (qZVS-TR). That is to say, if $t_{zvs} > t_{dx}$, qZVS-TR will be present. These cases are shown in Fig. 2.10(b) and (f). On the other hand, the inductor current may exhibit a zero-crossing from the correct direction to the incorrect direction during the device dead-time due to insufficient initial energy (qZVS-ER). In this case, if additional dead-time is provided to the switch, the parasitic capacitor charging and discharging process would reverse back to the initial state. It is

desired to limit the additional dead-time in these cases, as the incurred loss would increase as the difference between the zero crossing instant and provided dead-time increases. These cases are shown in Fig. 2.10(c) and (g), where t_{zc} is defined as the time in which the current crosses from the correct to incorrect direction. In general, the qZVS transition type in Fig. 2.10(c) is the most generic transition as it contains all other transition types in the top row with appropriate adjustment of t_{zc} and dV_x. For example, the ZVS case can be realized by setting $t_{zc} = t_{zvs}$, and $dV_x = V_x$. To realize any of the bottom row cases, Fig. 2.10(d) can be used for $t \in [t_0, t_x']$ in cascade with Fig. 2.10(c) for $t \in [t_x', t_{dx}]$. However, in the cases of time- and energy-related qZVS and d-qZVS, post-processed corrections to (2.16) are required, as the voltage transition does not fully complete when the incoming device is turned on.

2.4.3. Time-related qZVS

In the case that the t_{zvs} result from (2.16) is greater than the designated maximum allowable dead-time, a qZVS-TR situation is present. The value of dV_x can be calculated by solving the differential equations corresponding to Fig. 2.9, using the linear time-equivalent capacitor in (2.17), with the solution given by the following equations,

$$dV_x = V_{b,\bar{x}} - A_t \omega_{eq,t} \cos\left(\omega_{eq,t} t_f + \phi_t\right) \tag{2.18}$$

$$\omega_{eq,t} = \left(L_{lk,x} C_{eq,t}\right)^{-1/2} \tag{2.19}$$

$$A_t = \sqrt{I_{L,0}^2 + \left(\frac{V_{b,\bar{x}}}{L_{lk,x}\omega_{eq,t}}\right)^2} \tag{2.20}$$

$$\phi_t = \tan^{-1}\left(\frac{\omega_{eq,t} L_{lk,x} I_{L,0}}{V_{b,\bar{x}}}\right) \tag{2.21}$$

Using (2.18)-(2.21), with final time $t_f = t_{dx}$, all parameters are known for the linear approximation to this transition, shown in Fig. 2.10(b) and (f).

2.4.4. Energy-related qZVS

If the energy at the start of the device commutation is insufficient to facilitate full ZVS, (2.16) will return a real plus imaginary time result. The physical meaning of the real-part to the solution is that the equivalent parasitic capacitor voltage will properly discharge in the time-shifted bound $t' \in [0,\ \Re(t_{zvs})]$, where $t' = t - t_x{}'$. However, if additional dead-time is provided to the devices, the inductor current will cross zero in the wrong-direction, causing the capacitor voltage to increase back towards V_x, incurring sub-optimal qZVS losses. While the real-part of the solution can be used to determine $t_{zc} = \Re(t_{zvs})$, the amount of voltage that has commuted during this time, dV_x, needs to be determined. This can be easily calculated by solving (2.18)-(2.21), with $t_f = \Re(t_{zvs})$.

2.4.5. General transition analysis

In order to circumvent the non-generality between time- and energy-related qZVS transition in the utilization of (2.16), a general transition analysis can be utilized based on the discrete solving method introduced in [32]. The block diagram for solving the transition is shown in Fig. 2.11. The analysis begins with input of the side of the transition of interest, x, the initial time of the transition, t_x, the maximum allowable time for the transition, t_{dx}, and the total voltage of the commutation, V_x. First, it is verified that the current direction is proper to enable to a resonant transition, where it is henceforth assumed that a positive current is the correct polarity. If the current is not positive, the algorithm proceeds by determining if the current crosses into the correct direction during the allowable duration of the switching transition. In instances of proper initial current direction, or in delayed transitions, the algorithm continues to the discrete solving block; otherwise, the transition is deemed to be hard-switched. In the subsequent discrete solving block for the switching commutation, the capacitor voltage, v_c, is stepped through in sufficiently small ΔV steps, where the total time duration of the transition, t_{tr}, and instantaneous value of inductor current, i_L, are linearly solved in each step according to,

$$v_c = v_c + \Delta V \tag{2.22}$$

$$t_{tr} = t_{tr} + C_x(v_c)\Delta V / i_L \tag{2.23}$$

$$i_L = i_L + \left(V_{b,\bar{x}} - v_c\right) C_x(v_c)\Delta V / i_L L_{lk,x} \tag{2.24}$$

derived as the discrete equivalent forms of the differential equations associated with Fig. 2.9. Therefore in each step, violation of time-related ($t_{tr} > t_{dx}$) and energy-related ($i_L < 0$) constraints can be evaluated, and all parameters required to model the realized

transition can be determined. The algorithm proceeds until one of the exit conditions is found, where the effective voltage transition can be modelled according to the diagnosed transition and mathematical modeling developed in the subsequent section.

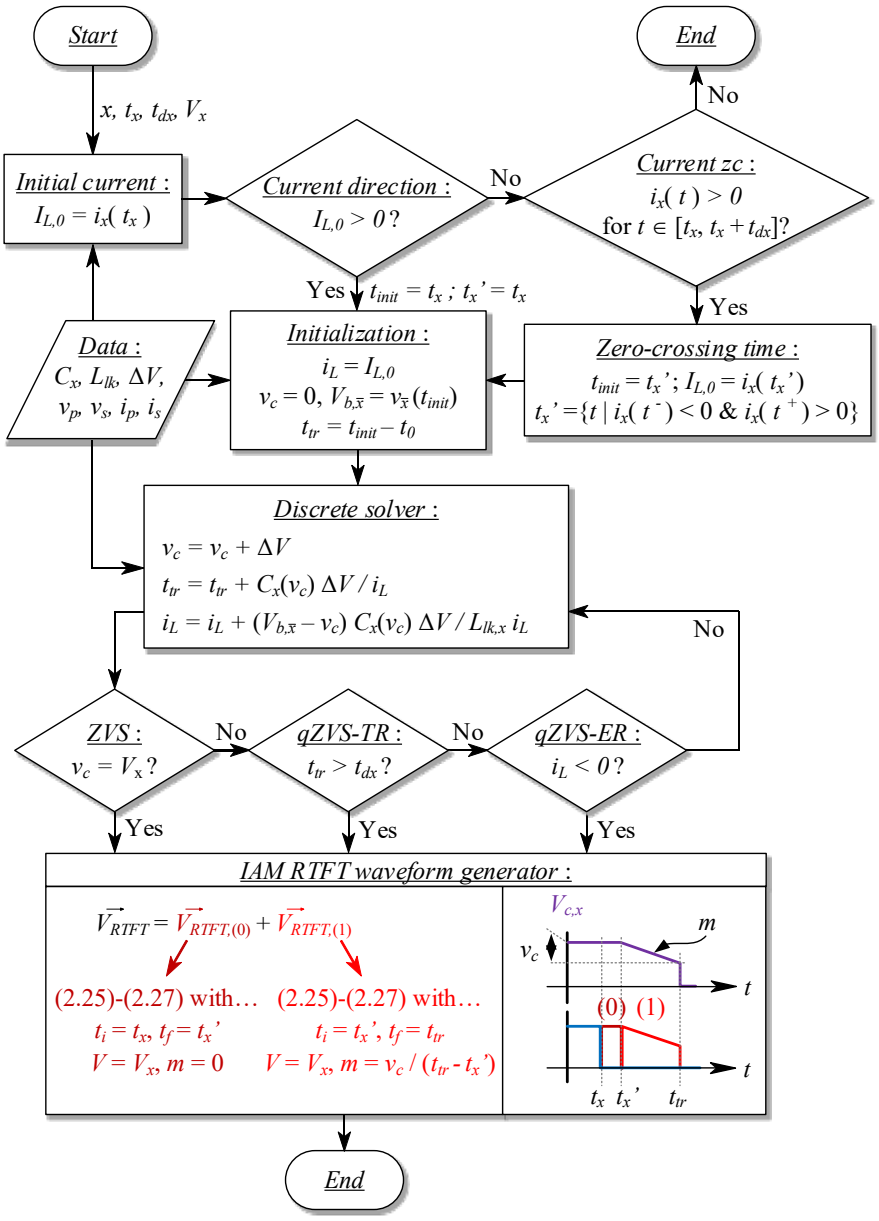


Fig. 2.11. Discrete solver for diagnosing switching transition types and finding the required parameters for waveform synthesis via the mathematical modeling.

2.4.6. Mathematical framework for IAM

In order to incorporate the various transition types as described in Fig. 2.10, a frequency-domain modeling of the voltage commutation intervals is required. The mathematical approach is pictorially shown in the bottom-halves of each sub-figure in Fig. 2.10, and in the waveform generator block in Fig. 2.11, where the ideal OAM vectors (in blue) are summed with the finite rise-time and fall-time (RTFT) vectors derived from the detailed transition analyses (in red), to create the equivalent voltage waveform (in purple). The RTFT vectors can be derived using Fourier decomposition, of which the result is included in below for the generic trapezoid in Fig. 2.10(c) with $t_x = t_i$, and $t_{zc} = t_f$,

$$\alpha_k = \frac{2}{k^2\pi} m\left[\cos(kt_i) - \cos\left(kt_f\right)\right] + \frac{2}{k\pi} V\left[\sin\left(kt_f\right) - \sin(kt_i)\right] - \frac{2}{k\pi} m\left(t_f - t_i\right)\sin\left(kt_f\right) \tag{2.25}$$

$$\beta_k = \frac{2}{k^2\pi} m\left[\sin(kt_i) - \sin\left(kt_f\right)\right] + \frac{2}{k\pi} V\left[\cos\left(kt_f\right) - \cos(kt_i)\right] - \frac{2}{k\pi} m\left(t_f - t_i\right)\cos\left(kt_f\right) \tag{2.26}$$

$$\overrightarrow{V_{RTFT,k}} = \sqrt{\alpha_k^2 + \beta_k^2}\sin\left(k\omega_{sw}t - tan^{-1}\left(\frac{\beta_k}{\alpha_k}\right)\right). \tag{2.27}$$

With the derived mathematical formulation, it is straightforward to sum the OAM and RTFT components via vector addition. Importantly, non-negligible magnitude and phase angle of the RTFT vectors can be present in low-order harmonics, which is the root cause in the perturbation of the effective modulation parameters. This is illustrated by a vector diagram in Fig. 2.12, where the RTFT vectors cause phase lag of both the primary- and secondary-side voltage vectors to a differing degree. As such, the effective δ is shown to be larger than the ideal parameter.

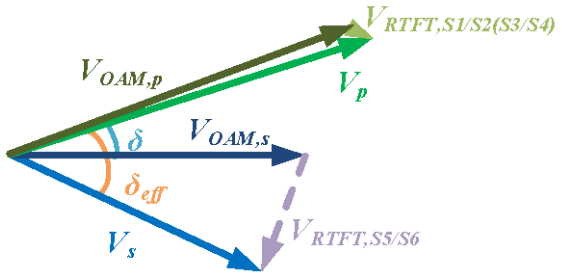
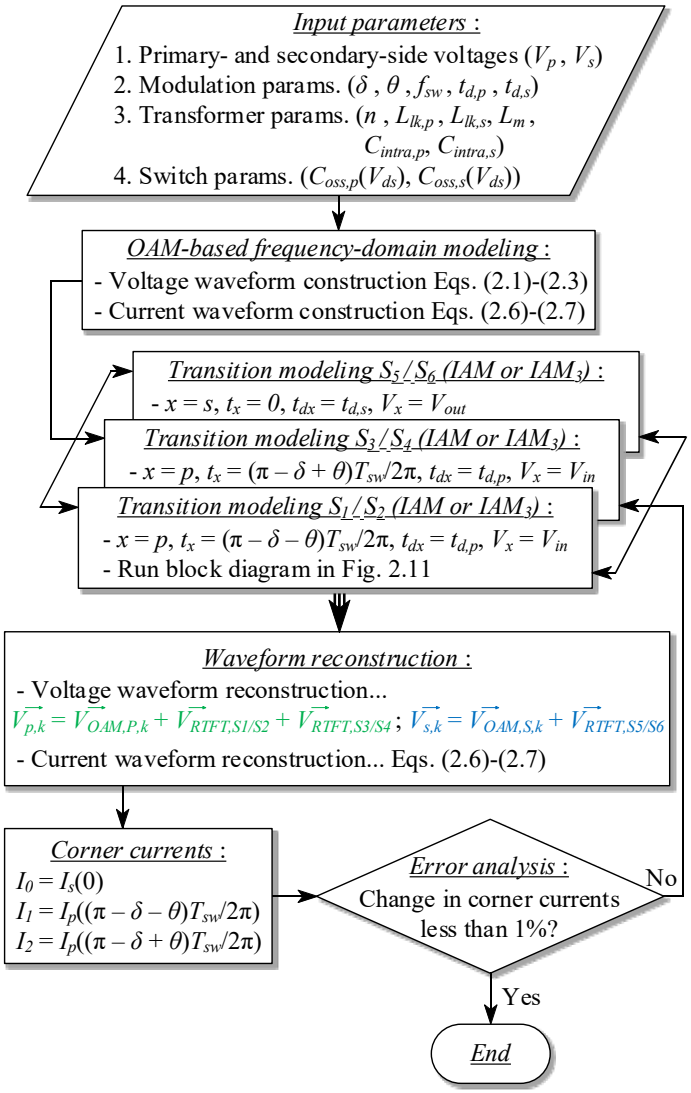


Fig. 2.12. Vector diagram including impacts of the RTFT vectors.

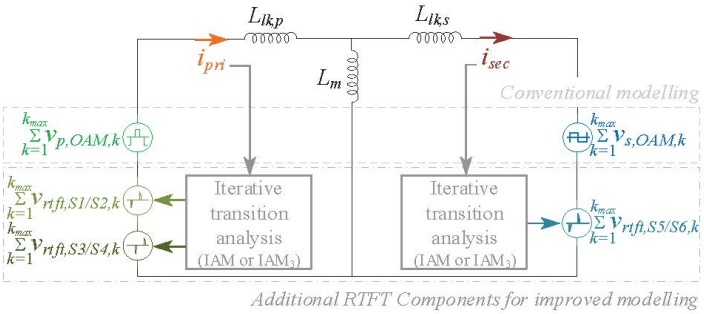
2.4.7. Implementation

The IAM is implemented via an iterative approach, which is described by the flow chart in Fig. 2.13(a). In the first step, the input operating parameters are fed into the OAM equation set (2.1)-(2.7), which is used to obtain the ideal frequency-domain voltage vectors and corresponding transformer current vectors. The time-domain transformer current can be reconstructed from the frequency-domain vectors via (2.11), and the corner currents (i.e. the value of the transformer current at the start of the switching transition) can be utilized to perform switching transition analyses. Importantly, the switching instant times of interest, t_x, are only dependent on the modulation parameters and have no modal implications; for the proposed topology and control scheme, the primary-side transitions of interest occur at $t_{p,(1,2)} = (2\pi - \delta \pm \theta)T_{sw}/2\pi$, and $t_s = 0$ corresponds to the secondary-side transition of interest. For consistency of analysis, the “transitions of interest" correspond to those where the current direction shall be positive to enable a ZVS transition. Eliminating modal independence of $V_{b,\bar{x}}$ is similarly straightforward, as the time-domain-reconstructed transformer voltage waveform of the side opposite to the commutation under interest can be inspected at time t_x. For example, during the $S_3 \rightarrow S_4$ primary-side transition,

the secondary-side value of $V_{b,s}$ can be determined by evaluating the time-domain-reconstructed secondary-side waveform $v_s(t_x)$. With x, t_x, t_{dx}, V_x, $V_{b,\bar{x}}$, and $I_{L,0}$ known, the frequency-domain RTFT voltage vectors for each switching transition can be extracted from the detailed discrete transition analyses and waveform generator described in Fig. 2.11. After conducting the transition modeling for all of the switching transitions of interest, the RTFT vectors are used as correction terms via vector addition to the frequency-domain OAM voltage vectors as explained in the previous section. The resultant modified primary- and secondary-side voltage vectors are used to reconstruct the current waveforms which is illustrated via the modified equivalent circuit in Fig. 2.13(b). The iterative procedure continues until the relative change between the inductor corner currents at the current and previous iteration are uniformly less than an arbitrary error margin of 1%.



(a)



(b)

Fig. 2.13. Implementation of the improved analytical modeling incorporating finite-duration transition time effects with the conventional frequency-domain modeling (a) iterative flow chart, and (b) equivalent circuit.

2.4.8. Limitations of IAM

A comparison between LTspice simulation and IAM prediction is shown for an example operating point in Fig. 2.14, with numerical comparison in Table 2.5.

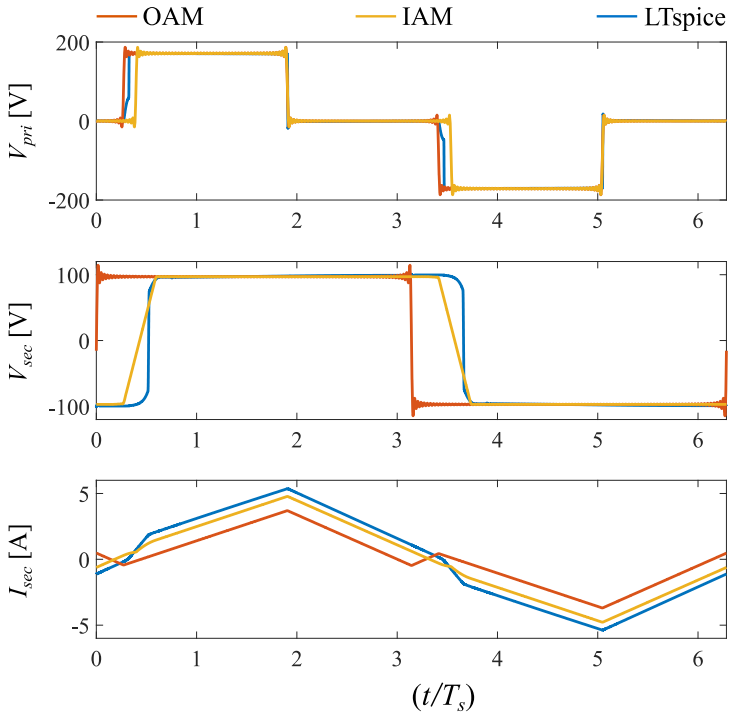


Fig. 2.14. Comparison between OAM, IAM, and LTspice at test case 2.

Table 2.5. Comparison of the test case sim. 2 DC-DC operating point.

I_{rms} [A]			P [W]		
OAM	IAM	LTspice	OAM	IAM	LTspice
1.71 (49%)	2.91 (13%)	3.34	130 (53%)	240 (14%)	279.6

In general, the IAM approach previously detailed is shown to still result in limitations, although it is improved in accuracy compared to OAM. This particular operating point was selected for comparison to highlight limitations in the OAM approach, and other literature that considers ideal analysis. In particular, OAM predicts the initial secondary-side current to be in the correct direction for ZVS (i.e. $I_{L,0} > 0$ at $t = 0$).

However, when considering the effects of device commutations, the current actually begins in the incorrect direction in LTspice. Therefore, analyzing ZVS boundaries without considering the effect that finite-duration transitions have on the operational behavior of the converter could lead to inaccuracies. Nevertheless, the operation point demonstrates a case of d-ZVS, where the secondary-side indeed achieves full ZVS although the initial current is in the incorrect direction.

Aside from the fact that error exists between OAM and IAM, there are still valuable quantitative and qualitative trends to analyze. First, the time-based ZVS analysis is verified as the total time of the secondary-side ZVS transition is very closely in agreement with that from LTspice. This is expected by (2.16), because the initial resonant transition current is the same in both cases; $I_{L,0} = 0$ as the ZVS transition is initiated by a current zero-crossing. With that being said, while the voltage commutation time is matched closely between IAM and LTspice, there is no guarantee that the final current will also match [24],[31],[32]. Due to this, small errors in the inductor current persist through the switching period and in fact leads to a mischaracterization of the primary-side lagging leg transitions; IAM predicts this transition to be hard-switched, while it is qZVS-ER in simulation.

In general, the errors in power transfer and RMS current are still not acceptable from a modeling standpoint at this operating point, even though the accuracy is enhanced compared to OAM. In this case, the power flow predicted by IAM is less than that of the LTspice simulation. This is in fact expected, as the zero-crossing of the secondary-side voltage occurs earlier in IAM than LTspice, hence the effective δ in

IAM is less than LTspice. Therefore, it is hypothesized that the reason for the incurred error in IAM is a result of the linear approximation to the non-linear device transition.

2.4.9. Corrections

To refine the zero-crossing, and overall shape, of the secondary-side voltage commutation, the ZVS transition is proposed to be broken down into a three-step, piece-wise linear transition. To understand the motivation for the three-step profile, an example C_{oss} vs V curve for the utilized high-voltage Si CoolMOS device, and the associated effective non-linear capacitance as developed in (2.15), is provided in Fig. 2.15. It is evident that after around 20 V (hereby deemed the critical voltage $V_{crit,x}$), the parasitic capacitance experiences an order of magnitude step reduction due to the completion of the channel depletion process [33]. Due to this, typically more time is required to charge and discharge the parasitic capacitance in the high-capacitance region (cf. the shape of the secondary-side voltage in Fig. 2.14). Notably, two high capacitance regions exist in the equivalent capacitance C_x, due to the charging and discharging behavior of the two devices in the switching leg (i.e. $C_x = C_{oss}(v_{ds}) + C_{oss}(V\text{-}v_{ds}) + C_{intra}$). Provided that the output voltage is larger than twice the critical voltage, three unique commutation sections can be modeled, namely: 1) 0 to V_{crit}, 2) V_{crit} to ($V_{out} - V_{crit}$), and 3) ($V_{out} - V_{crit}$) to V_{out}. Importantly, the three-step model is device-specific, and the critical voltage may differ depending on both device technology and internal device structure. In contrast to the considered Si CoolMOS device, the EPC2001C GaN-based device utilized on the primary-side has significantly reduced non-linearity, and hence the single-slope approximation in IAM is sufficient.

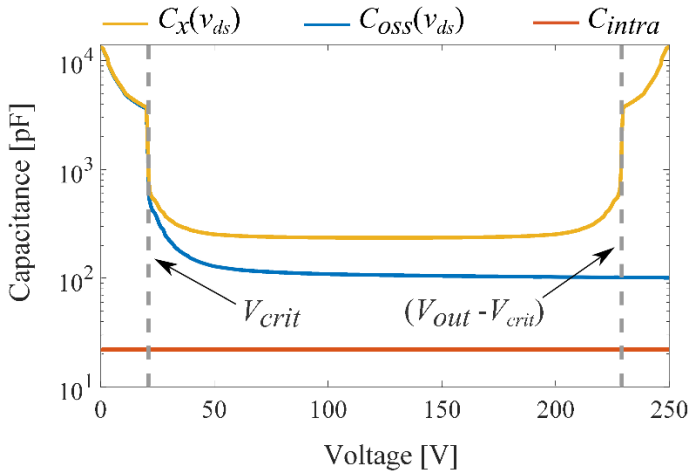


Fig. 2.15. Using an example Si CoolMOS device C_{oss} vs V curve [30] used to form the equivalent C_x capacitance. While the device has an order of magnitude reduction at V_{crit}, the equivalent capacitance C_x experiences this behavior at both V_{crit} and V_{out} - V_{crit}, due to the charging and discharging behavior of the two devices in the switching leg.

To model the three-section, piece-wise linear, voltage transition, hereby denoted IAM$_3$, the discrete approach introduced in Fig. 2.11 can be adapted to analyze and model the voltage commutation in each of the three voltage regions independently. Specifically, the exit logic and waveform generator blocks presented in Fig. 2.11 can be modified as shown in Fig. 2.16, where information regarding the time elapsed and capacitor voltage is stored in up to three unique sections, *S*. Regardless of the current section, conditions regarding qZVS-TR and qZVS-ER are evaluated and serve as exit conditions alongside the completion of full ZVS. The IAM$_3$ waveform generator is similar to that from IAM, where the single-slope RTFT vector in IAM, $V_{RTFT,(1)}$, is replaced by a summation of up to three unique RTFT vectors, one for each section that was reached. An example equivalent voltage commutation in the time-domain of the three-step voltage modeling approach under the d-ZVS case is shown in the bottom of the IAM$_3$ waveform generator block in Fig. 2.16, where four trapezoidal regions are positioned appropriately to construct the dynamic voltage profile.

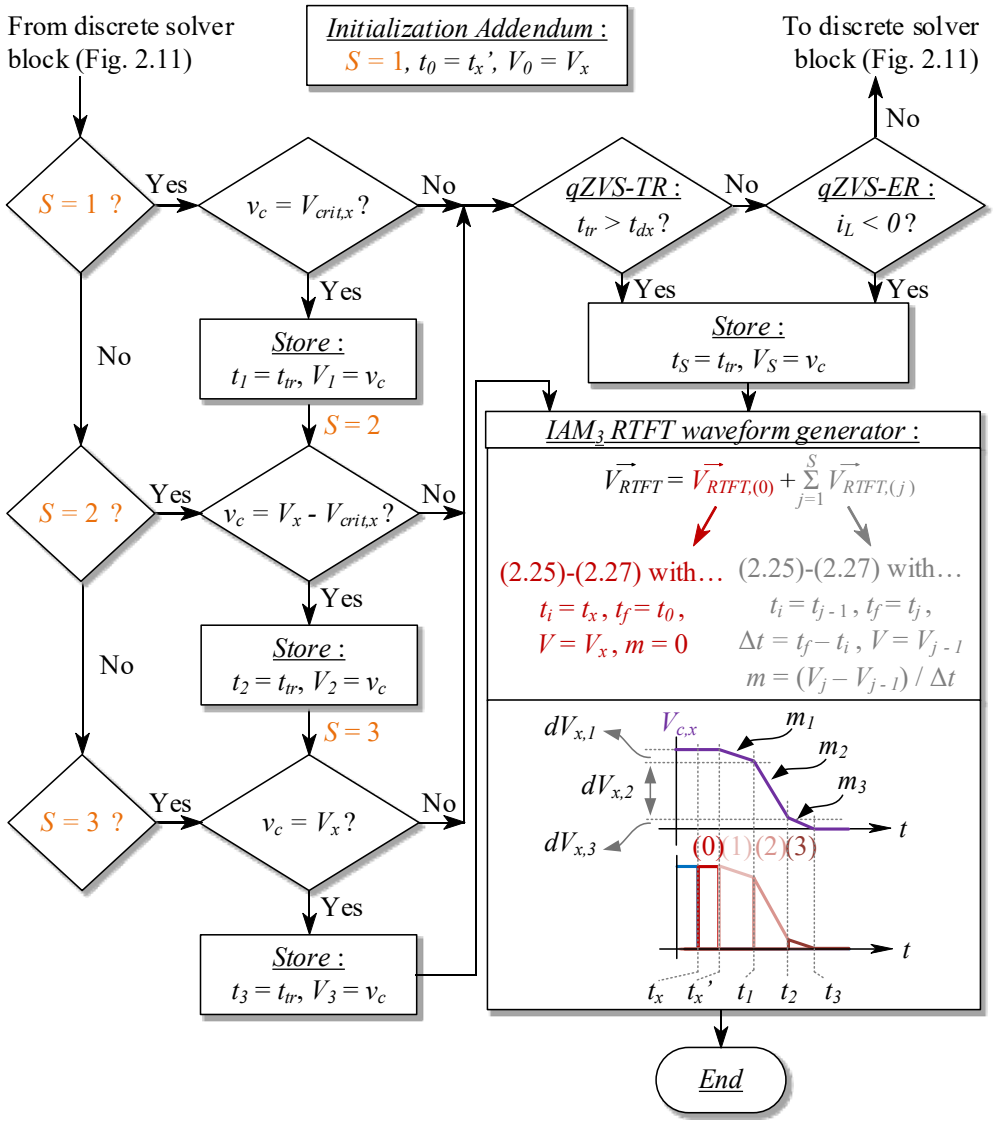


Fig. 2.16. Adaptation of the discrete solving method for the realization of the three-slope voltage commutation.

2.4.10. Comparison of corrections

The previous simulation scenario is re-compared against the IAM with the corrections outlined in the previous section in Fig. 2.17 and Table 2.6. It is evident that the IAM$_3$ corrections bring tight accuracy between the model and LTspice simulation, both in terms of RMS current and power transfer, as well as the time-domain waveform

recreation. Due to the highest level of accuracy with the three-step transition, it is henceforth used in the following comparison sections.

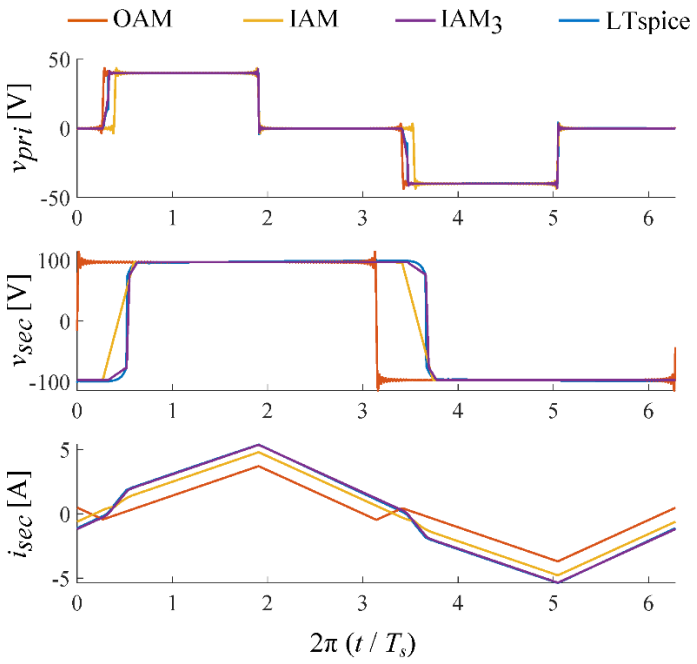


Fig. 2.17. Comparison of the Sim. 2 operating condition between OAM, IAM, IAM_3, and LTSpice.

Table 2.6. Refined comparison of the Sim. 2 operating point.

$I_{rms,IAM3}$ [A]	$I_{rms,sim}$ [A]	P_{IAM3} [W]	P_{sim} [W]
3.32 (0.61%)	3.34	278.14 (0.52%)	279.58

2.4.11. Harmonic and iteration analysis

As with any frequency domain modeling approach, the number of harmonics required to create an accurate representation of the waveforms under study needs to be analyzed. Furthermore, as the proposed approach is iterative, it is important to analyze how many iterations typically are required before convergence. To analyze these two factors, the previous test condition (test case Sim. 2 in Table 2.3) is analyzed as a function of the number of harmonics. In each case the procedure is iterated to convergence.

The impact of the number of harmonics on the prediction accuracy of power and RMS current, time duration of the algorithm, and the number of algorithmic iterations to convergence (measured in MATLAB R2019 on an Intel(R) Core(TM) i7-8700 CPU @ 3.20 GHz with 16.0 GB RAM, where the algorithm was run 20 consecutive times to measure average, maximum, and minimum time durations), are presented in Fig. 2.18. It is clear that the predictions of power and RMS current are accurate compared to the simulated values even when considering as low as five odd harmonics. Within a 5% error bound, the algorithm converges between 10 and 13 iterations. While increases in the number of harmonics will marginally increase the prediction accuracy, increased harmonic considerations naturally come at the cost of increased execution time of the algorithm.

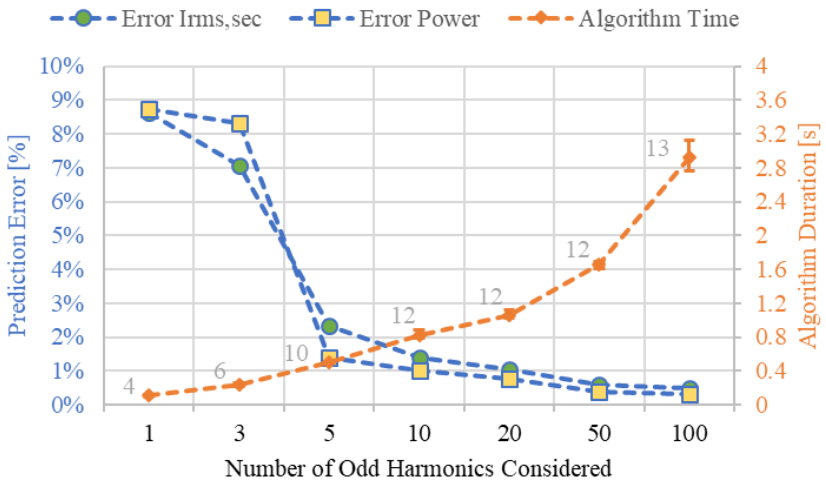


Fig. 2.18. Analysis of the impact of the number of harmonics for IAM_3 in example test case Sim. 2, on prediction accuracy and algorithm time duration. The total number of iterations required for convergence is shown as a data label for the algorithm duration trace.

2.5. Comparative results

2.5.1. Simulation comparison

The remaining test conditions from Table 2.3 were compared between OAM, IAM_3, and LTspice, with the results shown in Table 2.7. It is clear that regardless of the modulation parameters and relative primary- and secondary-side voltage levels, the IAM_3 modeling approach can predict detailed LTspice performance within 5% accuracy. This is further verified in the time-domain waveform regeneration of Sim. 1, Sim. 3, and Sim. 4, shown in Fig. 2.19, where the LTspice results and IAM_3 predictions nearly completely overlap.

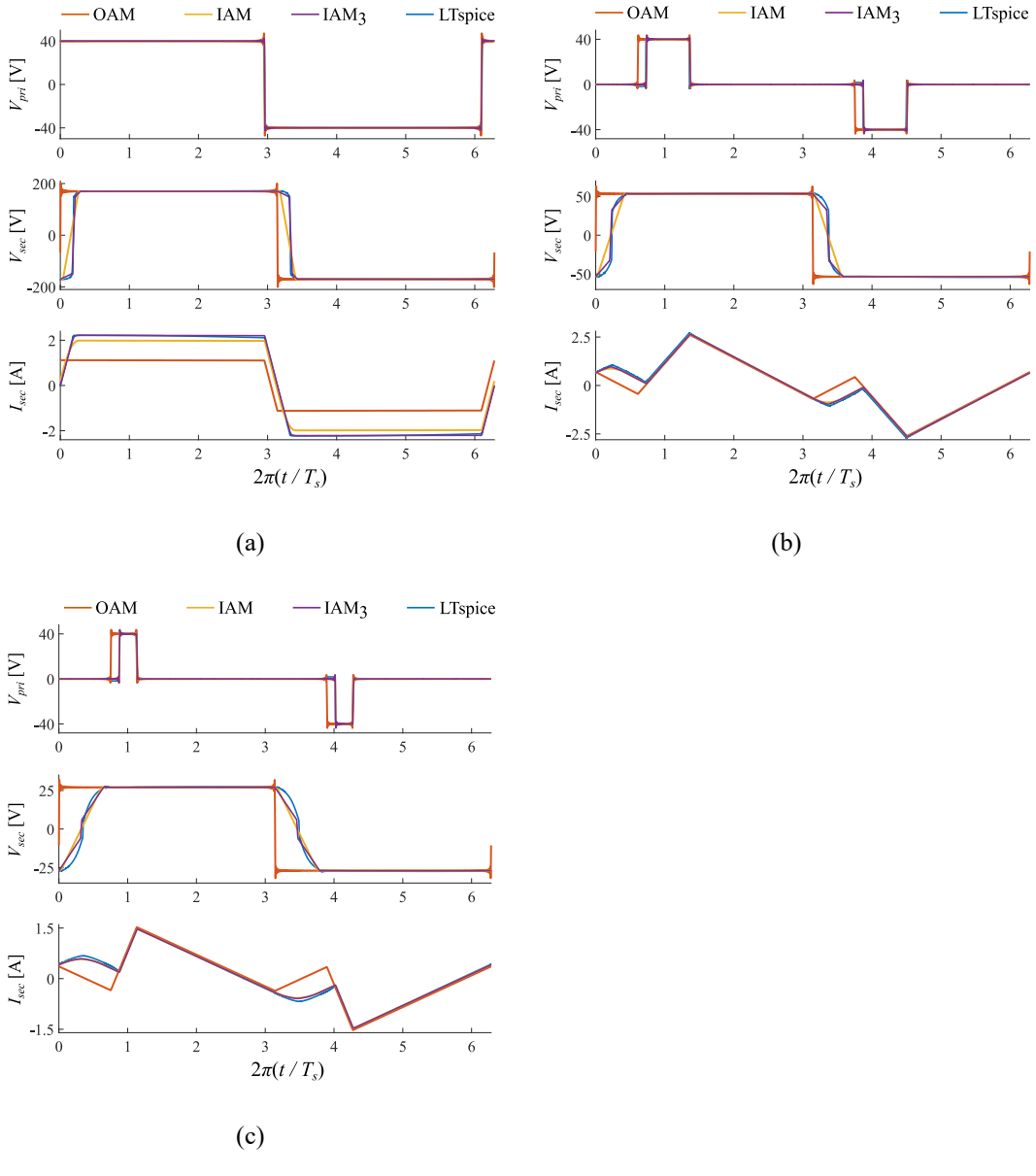


Fig. 2.19. Comparison of the OAM, IAM, and IAM_3 modeling approaches with LTspice results for three operating conditions provided in Table 2.3 (a) Sim. 1, (b) Sim. 3, and (c) Sim. 4.

Table 2.7. Comparison of modeling approaches for Sim. 1, Sim. 3, and Sim. 4, from Table 2.3.

Case	$I_{rms,s}$ [A]			P [W]		
	OAM	IAM_3	LTspice	OAM	IAM_3	LTspice
Sim. 1	1.61	2.12	2.106	245	330.55	328.3
Sim. 3	1.67	1.29	1.33	59	46.9	48.1
Sim. 4	0.64	0.71	0.73	11	11.61	11.53

Additional simulation comparisons have been performed over a wide switching frequency range, namely f_{sw} = {20 kHz, 200 kHz, 500 kHz, 1 MHz}. For comparative purposes, the Sim. 2 test case was evaluated at each switching frequency, where the inductances are each scaled according to, $L_z(f_{sw}) = L_{z,nom}(200\text{ kHz} / f_{sw})$, where z = {*lk,p*; *lk,s*; *m*}. By scaling the inductance proportional to the frequency, OAM predicts that the RMS current and power transfer should remain equal in each case. Comparison of the error between OAM and IAM_3, and LTspice shown in Fig. 2.20 highlights the contrary. First it should be noted that the error in OAM is within a reasonable range, <10% for power transfer and RMS, as the switching frequency reduces to 20 kHz (i.e. the ratio of dead-time to switching period reduces such that the transitions do not affect the performance significantly). However, as the switching frequency increases, OAM is invalidated with >50% errors in both RMS current and power transfer at high switching frequency. On the other hand, the error with the proposed IAM_3 modeling approach is uniformly less than 2% in each of the cases. As the trend of future power electronic converters is to increase switching frequency for volume and weight advantages, use of the proposed IAM modeling is indispensable for steady-state prediction accuracy.

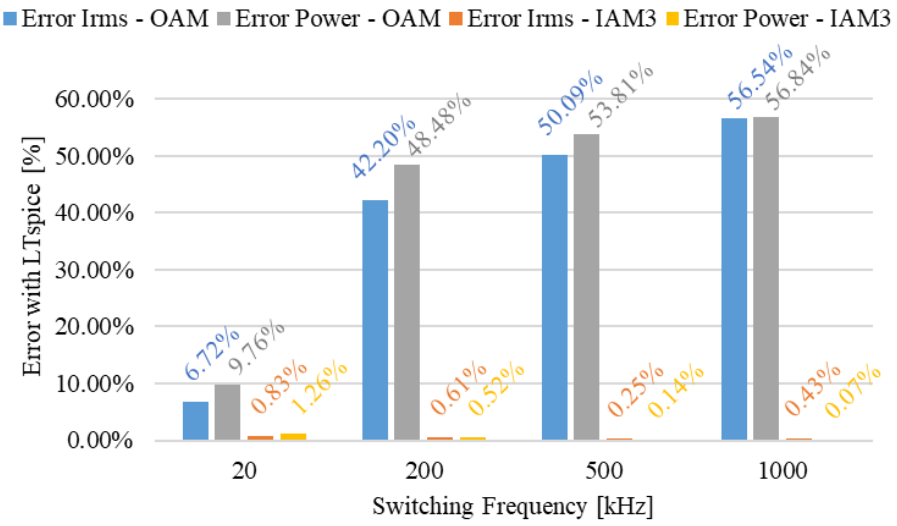


Fig. 2.20. Comparison of the error in RMS current and power transfer between OAM and IAM_3 versus LTspice, for the Sim. 2 operating condition with wide variation in switching frequency.

2.5.2. Experimental comparison

Several DC-DC operating points have been tested in hardware with the devices considered thus far, and other specifications provided in Table 2.2. The experimental results were facilitated by the prototype shown in Fig. 2.21. The specifications of the three tests are provided in Table 2.8.

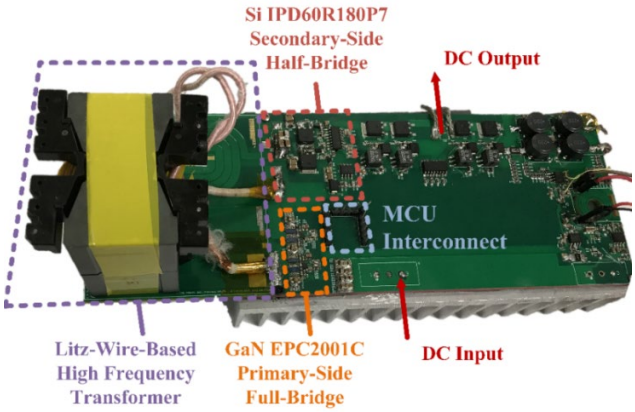


Fig. 2.21. Annotated photograph of the prototype used for experiments.

Table 2.8. Voltage levels and modulation parameter values for the experimental test conditions.

Test Case	V_{in} [V]	V_{out} [V]	δ	θ	f_{sw} [kHz]
Exp. 1	39.4	345.84	0.051	0.016	149
Exp. 2	40.1	276.74	0.0797	0.0747	249
Exp. 3	39.9	131.49	0.104	0.179	249

Of importance in comparing simulation and model results to a hardware experiment is including timing delays (propagation, rise-time, fall-time, etc.) between the controller and device gate-source voltage. With proper characterization, delay estimates can be incorporated into LTspice and model accordingly. In the model, the turn-off delay can be added to the start of the ZVS interval for each switch, and the difference between turn-on and turn-off delay can be added to the effective device dead-time, as shown in Fig. 2.22.

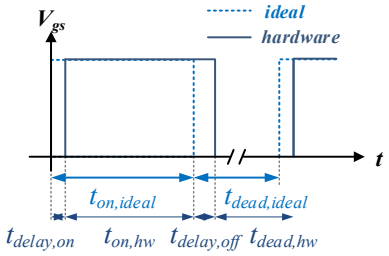


Fig. 2.22. Demonstrating the effect of timing delays on the model operation.

The numerical results of the experiment tests were extracted using a Keysight 1-GHz bandwidth oscilloscope (DSOX4104A) for RMS current measurements and a power analyzer (PA3000) for power transfer measurements. The experimental results were compared against LTspice and IAM_3, with implemented timing delays, numerically in Table 2.9 and pictorially in Fig. 2.23. From the numerical results it is clear that both the IAM_3 and LTspice are predictive of the hardware results, while the

OAM exhibits undesirable error. The accuracy of IAM_3 and LTspice to the experiment both validates the simulation verification from the previous section, and further necessitates the use of the proposed modeling approach. As such, the motivation for and contributions of IAM_3 are clear from the agreement between RMS current and power transfer, and the accuracy of time-domain waveform generation (and hence device transition modeling) that replicates the experimental performance of the converter.

Table 2.9. Comparison of the operating points in Table 2.8.

Test Case	Model	P [W] (error %)	$I_{rms,p}$ [A] (error %)
Exp. 1	OAM	358.96 (14.2%)	9.79 (13.8%)
	IAM_3	408.62 (2.3%)	11.12 (1.2%)
	LTspice	411.63 (1.6%)	11.28 (0.22%)
	Exp.	418.39	11.25
Exp. 2	OAM	215.8 (19.4%)	7.27 (22.5%)
	IAM_3	271.34 (1.3%)	9.39 (0.1%)
	LTspice	272.56 (1.8%)	9.47 (0.9%)
	Exp.	267.77	9.38
Exp. 3	OAM	54.19 (10.2%)	4.77 (14.5%)
	IAM_3	64.26 (6.5%)	5.61 (0.6%)
	LTspice	63.79 (5.7%)	5.63 (1%)
	Exp.	60.35	5.58

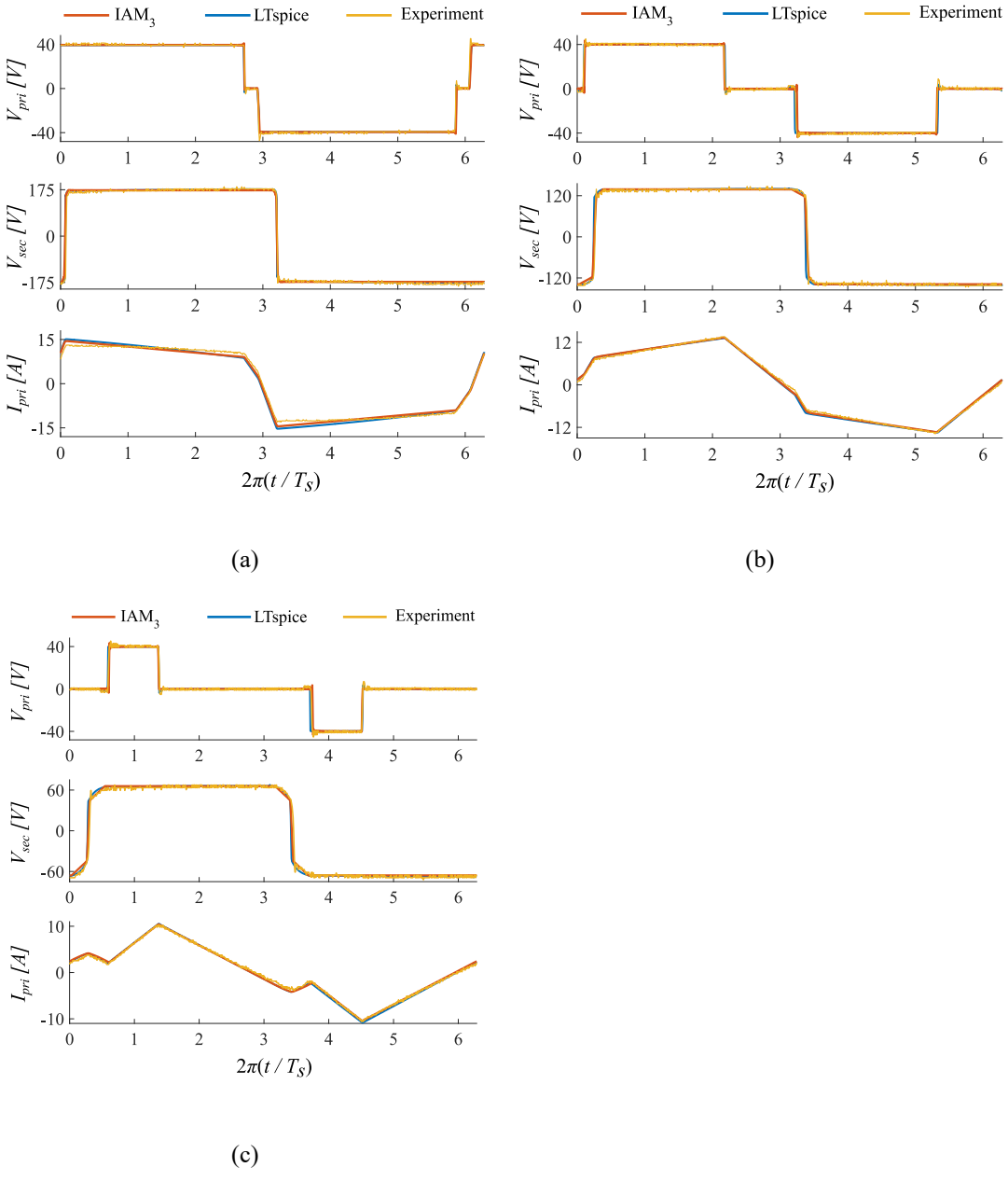


Fig. 2.23. Comparison of IAM_3 model predictions, LTspice simulation results, and experimental results for three operating conditions provided in Table 2.8, (a) Exp. 1, (b) Exp. 2, and (c) Exp. 3.

2.6. Summary

This chapter has proposed an improved FDM technique for modeling the steady-state performance of the DAB DC-DC converter. It is demonstrated that as DAB converters are operated at higher frequency, the finite rise- and fall-time of the effective

commutation capacitances during a switching transition can significantly perturb the effective modulation parameters, invalidating idealized modeling approaches. As such, a detailed switching transition model was incorporated with the traditional ideal frequency-domain-modeling in an iterative fashion. The proposed IAM_3 approach is shown to match closely with both LTspice simulation and hardware experiments. The proposed modeling approach can be used as an open-loop testing assist tool, as it exhibits high accuracy to experimental hardware results. Furthermore, the proposed modeling approach can be used as the inner-loop of an outer-loop modulation optimization function, to analyze modulation parameter trajectories that specifically minimize circuit losses.

The proposed improved FDM approach considering both ideal analysis and the effects of rise- and fall-time during switching transitions can also be applied for other topologies, namely any topology that can be equivalently modeled by the dual-port voltage circuit presented in Fig. 2.2 with an arbitrary impedance network between the two sources. This includes, but is not limited to, the three-phase DAB, resonant DAB, and non-isolated realizations of these structures. In the application of improved FDM modeling for other topologies, the principal difference is in characterization of the OAM equation set, particularly for the primary- and secondary-side voltages (which may have *m*-number of voltage levels) and the primary- and secondary-side currents (which will depend on the impedance network considered). Furthermore, the equivalent circuit for switching transitions may differ with a unique set of associated differential equations. Nevertheless, the differential equations according to the switching transition equivalent circuit can be discretized and solved with a similar technique utilized in the

“discrete solver" section of Fig. 2.11. With these two variations compared to the proposed topology, the RTFT waveform generation via IAM or IAM_3 can be utilized and summed with OAM as an error vector, similar to the approach demonstrated in Fig. 2.13. Therefore, while some variation may exist in the extension of the approach to other topologies, the fundamental mathematical modeling and utilization of the RTFT vectors remains the same.

Chapter 3. Main-Circuit Parametric Design, Component Selection, and Control Considerations

3.1. Traditional parametric design selection

The penetration of PV microinverters in residential solar applications has increased globally over the last ten years. This growth can be attributed to cost reductions of solar modules and power electronics, alongside improvements in system-level perspectives such as reliability [1]. In the pursuit of further reduced microinverter costs, single-stage approaches have become more prevalent in both industry and the literature [34]. In particular, the dual-active-bridge (DAB) DC-DC converter is a promising building block due to control flexibility and possibility of enabling wide-range ZVS operation [15]. For DC-AC applications, one of the possible ways to utilize a DC-DC DAB-based architecture is shown in Fig. 3.1, which interfaces a fixed DC voltage to a variable DC (rectified line-frequency AC) voltage, followed by a line-frequency unfolder stage [20]. While the secondary-side full-bridge implementation is shown in Fig. 3.1, secondary-side half-bridge realizations are also feasible as analyzed in Chapter 2, which can realize inherent AC-side voltage step-down and cost improvements due to the reduction in two high-frequency devices. To further improve the cost and power density of the microinverter system, the DAB power transfer inductance can be realized by the transformer's leakage inductance. As such, the DAB inductance is henceforth deemed L_{lk}.

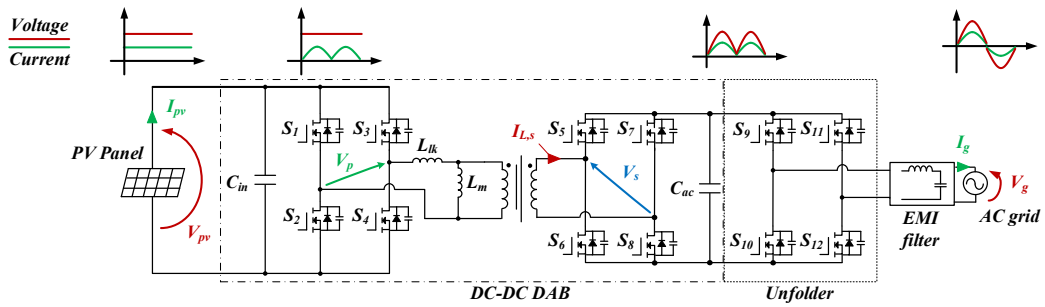


Fig. 3.1. Topology of the DAB-based, single-stage PV microinverter with representative low-frequency waveforms of voltage and current.

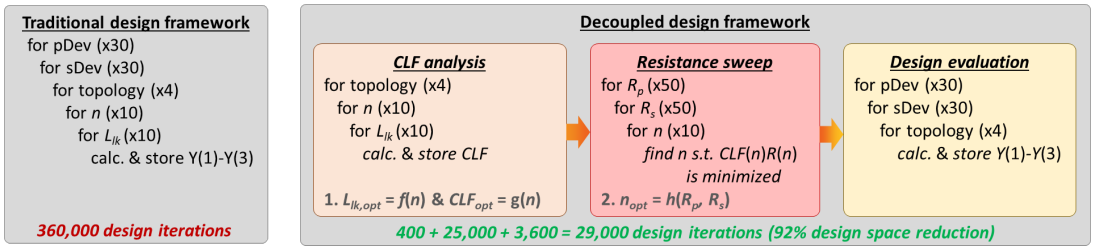
Optimal modulation of the various control variables in DC-AC DAB converters across the AC line cycle is critical to ensure power-factor-correction (PFC) of the AC-side current, while realizing low transformer RMS current (low conduction losses), and ZVS turn-on for all of the switches (low switching losses). Modulation optimization in DAB-based DC-AC converters is a well-researched topic in both the time-domain [20]-[22],[35]-[36], and frequency-domain [23]. With that being said, only [20] leverages the modulation to inform parametric design decisions of transformer turns ratio, and power transfer inductance. However, it is unclear how the work in [20], conducted for an AC-DC DAB converter in electric vehicle charging applications, may extend to microinverters where the California Energy Commission (CEC) weighted efficiency [38] is a more important metric than the average efficiency.

From a design perspective, [20],[21],[23],[36] have all restricted the usage of turns ratios such that $nV_{DC} > V_{ac,pk}/r$, where $r = \{1, 2\}$ for AC-side full- and half-bridges, respectively. In contrast, [22] showed that the optimal turns ratio to minimize turn-off currents lies instead in the bound $V_{ac,rms}/r < nV_{DC} < V_{ac,pk}/r$. However, a more systematic design approach is required in microinverter applications to evaluate the effect of the turns ratio selection as it relates to performance across the full operating range, as

opposed to a single power level, as well as how the component selection and turns ratio selections are inter-related. From the perspective of inductance design, [20] claims that the optimal power transfer inductance is within 75% to 85% of the maximum allowable value, but does not explicitly identify how the optimal inductance selection may impact the converter's performance. In other cases, typically a value of leakage inductance is selected near the maximum allowable limit without further analysis [21]-[22],[35]-[36]. In conclusion, without a comprehensive design optimization, sub-optimal design decisions may be made that limit the converter's maximum achievable efficiency, regardless of subsequent control-based optimization.

The main contribution of this chapter is to develop a holistic approach towards the DC-AC DAB design process featuring a decoupled analytical framework for computational simplification. A conventional design framework in shown in Fig. 3.2(a), where a '*for-loop*' is run for each of the decision space vectors to analyze converter performance. The proposed decoupled design framework is shown in Fig. 3.2(b), where three key steps are invoked: conduction loss factor minimization (determining the optimal leakage inductance as a function of the turns ratio), generalization of turns ratio selection as a function of primary- and secondary-side resistances (determining the optimal turns ratio as a function of the circuit resistances), and finally calculation of the objective functions within the component selection vectors in the decision space. In light of the principal contribution of this chapter, additional contributions focus on the results of each of the three decoupled analyses: a) extending modulation-based optimization to further identify optimal design values of transformer turns ratio, n, and power transfer inductance, L_{lk}, that minimize the

microinverter's CEC-related efficiency drop due to conduction loss; b) developing a map for optimal turns ratio selection for a given topology as a function of the primary- and secondary-side total resistances; and c) evaluation of efficiency drop, footprint area, and cost, serving as three objective functions in a multi-objective minimization procedure to develop concrete tradeoffs between four secondary-side switching networks, and three sets of unique device configurations. The final contribution of this chapter revolves around the adaption of the IAM_3 analysis from Chapter 2 to facilitate fully open-loop control from the main-circuit in DC-AC operation. A portion of the analysis and results presented in this chapter are published in [37].



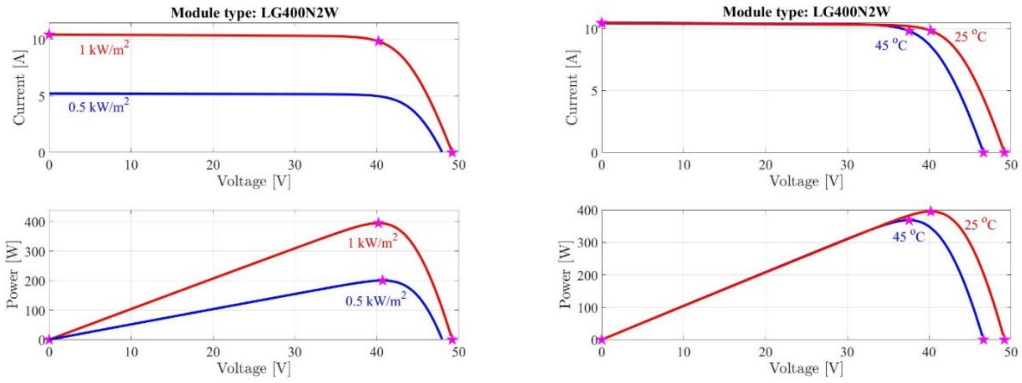
(a) (b)

Fig. 3.2. Flow chart for the (a) traditional main-circuit design framework, and (b) proposed decoupled design framework.

3.2. System-level microinverter analysis

From a system-level perspective, the DAB-based main-circuit topology is operated to extract power from the input-side PV panel, and deliver it to the utility grid. A PV panel can be generally modeled as a voltage controlled current source, and hence the operating point of the PV panel is determined through control of the input voltage [39]. The LG400N2W PV panel's current versus voltage curve, with variation as a function of temperature and irradiation, was evaluated in MATLAB Simulink and shown in Fig. 3.3 [40]. It is evident that variation in irradiation results in near-linear

variation in output power, at a near-constant MPP voltage. Furthermore, the variation in ambient temperature shows a reduction in both PV panel power, as well as MPP voltage, due to the negative temperature coefficient of the considered panel with respect to temperature.



(a) (b)

Fig. 3.3. Example LG400N2W PV panel operating point variation as a function of (a) irradiation, and (b) ambient temperature.

Dynamically, the microinverter should seek to operate the PV panel at its maximum power point (MPP) highlighted by the star-markers around 40 V in Fig. 3.3.

In steady-state, it can be assumed that the microinverter is operating such that the PV panel is at the MPP. As such, the input voltage, current, and power of the PV panel can be modeled as fixed DC quantities. On the grid-side, the AC voltage is sinusoidal at an assumed nominal amplitude and frequency, which is 240 V and 60 Hz for residential microinverter applications in the United States. The most typical operating condition requested by the utility grid regarding the phase angle between the grid voltage and grid current is that of unity power factor (UPF), where the grid voltage and current are completely in phase. As such, the grid-side power variation can be determined by,

$$P_o(t) = V_g(t)I_g(t) = 2V_{ac,rms}I_{ac,rms}\sin^2(\omega_g t) = V_g I_g\big(1 - \cos(2\omega_g t)\big), \quad (3.1)$$

where $V_{ac,rms}$ and $I_{ac,rms}$ are the RMS values of the grid voltage and current, respectively, and ω_g is the grid angular frequency. It is clear that the grid-side power has both an average and double-line-frequency (DLF) component.

Assuming loss-less power transfer of the dual-active-bridge (DAB) converter, the output power can be reflected to the input-side of the converter,

$$P_{in}(t) = V_{in}I_{in}\big(1 - \cos(2\omega_g t)\big), \quad (3.2)$$

where V_{in} and I_{in} correspond to the input voltage and current of the PV panel at a given maximum power point (MPP). The power flow comparison is shown pictorially in the equivalent system-level diagram in Fig. 3.1. It is clear that there exists an inherent power mismatch between the PV panel and the grid-side power, as discussed in Section 1.4. While conventional microinverter applications utilize large film capacitors to mitigate this power mismatch, an active power decoupler (APD) topology is proposed for use, of which the merits and demerits of using the APD will be addressed specifically in Chapter 5. Due to the fact that the APD and main-circuit input are both connected in parallel, the input voltage must remain fixed. Therefore, the main-circuit shall be controlled to modulate the drawn input current to achieve the average plus DLF profile.

3.3. Optimal L_{lk} and turns-ratio

The loss performance of the main-circuit is not only decided by the optimal selection of modulation variables, but is also dependent on offline design parameters,

namely the transformer turns ratio, leakage inductance, and magnetizing inductance. This is to say that control-level optimization can only improve converter performance so much, whereas appropriate parametric selection can be equally as important. With the developed frequency-domain framework from Section 2.3.1, parametric optimization can be performed to identify optimal design value and trade-offs.

3.3.1. Topological selection

The main-circuit could be realized with up to eight variations regarding the bridge structure on the primary- and secondary-sides. Due to the low-voltage nature of the PV-side and high-voltage nature of the grid-side, the number of variations can be reduced to just four. In particular, half-bridge structures on the low-voltage side are undesirable, as the transformer applied voltage is effectively halved and the current is doubled. Instead, worth considering are architectures with a primary-side full-bridge, and either a secondary-side full- (SSFB) or half-bridge (SSHB), shown in Fig. 3.4(a) and (b), respectively. The two structures inherit unique advantages, as the SSFB has an additional control-level degree of freedom with a secondary-side zero-state [θ_{AC}, where the primary-side zero-state is similarly deemed θ_{DC} – cf. Fig. 3.4(e)], whereas the SSHB may be more advantageous from a cost and reliability perspective, as there are two less high-frequency devices and associated gate driving components. Additional topological options are available where the unfolder is integrated with the secondary-side devices, deemed direct structures (-d), shown for the SSFB-d and SSHB-d in Fig. 3.4(c) and (d), respectively. Generally, the operation of the direct and indirect structures are equivalent in high-frequency, however component selection and design considerations such as cost, occupied footprint area, and loss, may lead the designer to

prefer one of these four structures over the others. These tradeoffs will be specifically evaluated in more detail in Section 3.4.5, and design guidelines will be developed.

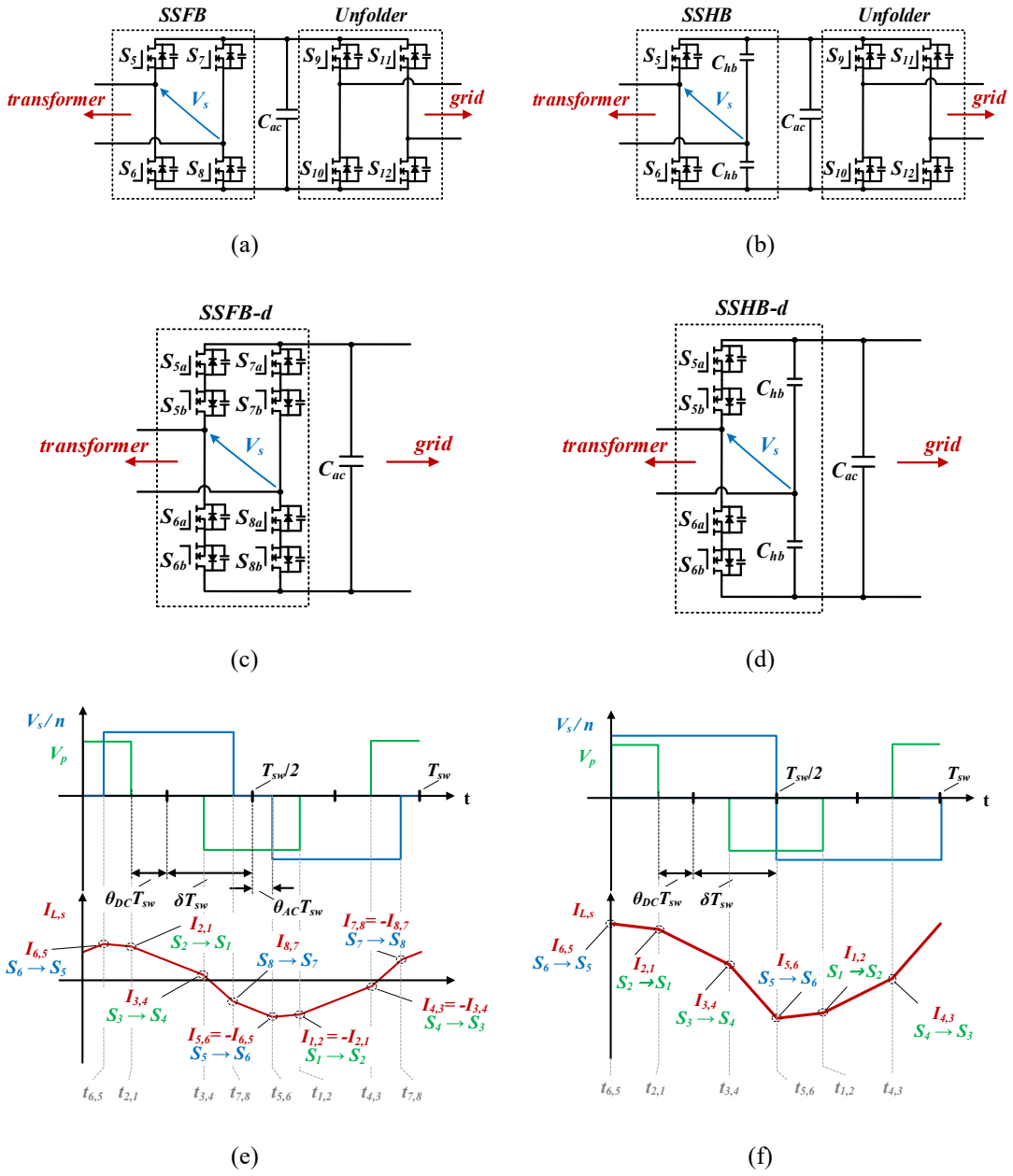


Fig. 3.4. Considered secondary-side switch configurations (a) SSFB + unfolder, (b) SSHB + unfolder, (c) SSFB-d, (d) SSHB-d, (e) example high frequency waveforms in full-bridge structures, and (f) example high frequency waveforms in half-bridge structures.

3.3.2. Objective function

As described in Appendix Section A, the main-circuit CEC efficiency drop can be decomposed by specific loss mechanism,

$$\eta_{MC,drop} = \sum_{i=1}^{6} C_i \left[\frac{L_{cond,s,i} + L_{sw,s,i} + L_{cond,t,i} + L_{core,t,i}}{P_i} \right] \tag{3.3}$$

where $L_{cond,s,i}$ and $L_{sw,s,i}$ denote the line-cycle-averaged conduction and switching losses in the devices, respectively, and $L_{t,i}$ defines the transformer related losses, at each average power level P_i. By leveraging the modulation optimization, the switching losses can be brought close to zero by ensuring near-uniform ZVS for all switching transitions, as will be described in the next section. Furthermore, core loss will be minimized through the optimization of the transformer core geometry, described in depth in Chapter 4. Therefore, parametric design decisions can be made by minimizing the impact of conduction-loss on CEC efficiency, through minimization of the following factor, termed the conduction loss factor (CLF),

$$CLF = \sum_{i=1}^{6} \frac{C_i}{P_i} I_{ac,rms,i}^2 \, , \tag{3.4}$$

where $I_{ac,rms,i}$ is the RMS of the transformer current across the AC line-cycle at average power level P_i. Multiplying the CLF by the circuit's resistances yields the total percentage penalty to the CEC efficiency incurred from conduction losses.

3.3.3. Operational constraints

Assuming loss-less unity power factor (UPF) grid-current injection, the time-varying output power characteristic can be derived based on (3.1) and (3.2),

$$P_o(t) = P_{av}\left(1 - \cos\left(2\omega_g t\right)\right) \tag{3.5}$$

where P_{av} is the operating MPP of the PV panel. In order to achieve variation of power as given by (3.5), the desired instantaneous power is equated to the power flow predicted by the frequency-based modeling in (2.10), creating an equality constraint,

$$C_1 = P_o(t) - P_{pri} \tag{3.6}$$

To enable ZVS of all high-frequency switches, the direction of the inductor current during a switching transition at a given switching node must be in the proper direction to facilitate the charge and discharge of device and transformer parasitic capacitances, as described in Section 2.3.3. The ZVS-by-direction inequality constraints for the switching transitions of interest are presented in Table 3.1 (cf. Fig. 2.4(a) and Fig. 3.1). In particular, the switching transitions of interest correspond to those in which the transformer current must be positive to enable ZVS. Due to operational symmetry of the DAB, ensuring ZVS-by-direction of one device transition in a switching leg will enable ZVS of the complementary switch in that leg as well. While up to four constraints exist when considering the SSFB architecture, constraints C_4 and C_5 will be equal (non-unique constraints) when considering the SSHB.

Table 3.1. Necessary (current-direction) constraints for ZVS of all device transitions.

Device Transition	Constraint #	Inequality constraint
$S_2 \rightarrow S_1$	C_2	$I_{L,p}(t_{2,1}) > 0$
$S_3 \rightarrow S_4$	C_3	$I_{L,p}(t_{3,4}) > 0$
$S_6 \rightarrow S_5$	C_4	$I_{L,s}(t_{6,5}) > 0$
$S_7 \rightarrow S_8$	C_5	$I_{L,s}(t_{7,8}) > 0$

Notably, for a given set of $\{n, L_{lk}, L_m\}$, it is not always possible to ensure that a ZVS by-direction condition is met for every device at all operating points along the AC line-cycle, particularly in the lower line-cycle region. In these cases, the inequality constraint of one of the device transitions can be shifted to allow a negative threshold (i.e. $I_{L,x}(t_x) > -I_{th}$, where $I_{th} > 0$). In this case, the optimization algorithm will be able to find feasible solutions to the optimization problem, though some instances of hard-switching will be realized. With that being said, the total hard-switching loss will typically not be very significant when averaged across the full AC line-cycle, as most of the time ZVS will be achieved, especially near the higher power processing points along the AC line-cycle. In the pursuit of wider ZVS capabilities, previous research has identified the use of reduced transformer L_m to L_{lk} ratios [42], which inevitably comes at the cost of increased winding RMS currents. Other previous approaches consider the use of commutation inductances in each switching network (discrete inductance connected between the two switching legs of a particular side, before the transformer), however this may require additional magnetic components potentially compromising cost and other performance metrics [20],[23].

3.3.4. Design constraints

In any isolated DAB design, there is no explicit design constraint on the turns ratio. However, in accordance with previous literature, a wide range of n has been considered such that $V_{ac,rms}/r < nV_{dc} < 1.5V_{ac,pk}/r$. For each value of turns ratio, n, there is an upper-bound of primary-side referred leakage inductance according to the DAB maximum power transfer condition, which can be derived according to,

$$L_{lk,max} = \frac{V_{in}V_{ac,pk}}{16nrf_{sw,min}P_{av,max}} \tag{3.7}$$

where $f_{sw,min}$ denotes the minimum limit on the switching frequency decided by the designer. In particular for variable switching frequency control implementations, the minimum switching frequency is selected in (3.7) to enable a larger upper bound of leakage inductance than in fixed frequency control implementations. Henceforth, the normalized leakage inductance is defined as $L_{lk,norm} = L_{lk}/L_{lk,max}$.

3.3.5. CLF optimization

A block diagram of the optimization procedure is shown in Fig. 3.5. The inner-loop modulation optimization objective function (i.e. the blue box, named constrained numerical optimization) is set to minimize the primary-side transformer RMS current, defined in (2.8), subject to (3.6) and the ZVS constraints in Table 3.1, at '*N*' number of DC-DC operating points across the AC line-cycle. Though analytical formulation of the problem is relatively simple, finding a closed-form solution is intractable and hence a numerical solution is obtained using the '*fmincon*' function in MATLAB's optimization toolbox. The nominal converter specifications, alongside ranges for modulation variables and converter parameters for both secondary-side realizations considered in this work are listed in Table 3.2. For all of the subsequent analyses, the magnetizing inductance is fixed as $L_m = 20L_{lk}$.

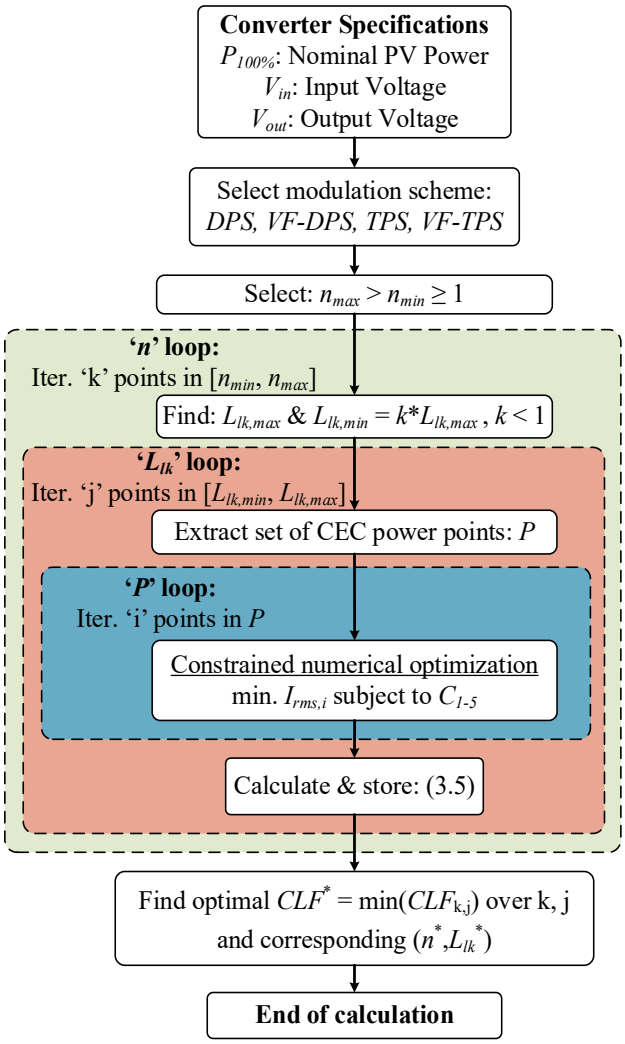


Fig. 3.5. Block diagram of the system-level design optimization of turns ratio and leakage inductance, with modulation optimization as the inner-loop.

Table 3.2. Decision space of the system-level optimization.

V_{in}	$V_{ac,rms}$	$P_{av,max}$	L_{lk}
40 V	240 V	400 W	[0.5, 0.95]$L_{lk,max}$
SSFB	n	f_{sw}	θ_{DC}, θ_{AC}, δ
	[6, 12]	[100, 300] kHz	[0, 0.25]
SSHB	n	f_{sw}	θ_{DC}, δ
	[3, 6]	[100, 300] kHz	[0, 0.25]

To validate the proposed frequency-domain modulation parameter optimization procedure, several DC-AC operating points were validated in simulation and compared to model estimates. The DPS and VF-DPS modulation types were considered with a secondary-side half-bridge, using $n = 4$ and $n = 5$, respectively. Similarly, both TPS and VF-TPS were considered with a secondary-side full-bridge, using $n = 7$ and $n = 8$, respectively. In each case, the total leakage inductance was selected as $L_{lk} = 0.95L_{lk,max}$. The simulation data was extracted in MATLAB Simulink using look-up-tables (LUTs) for the various modulation parameter trajectories, and the transformer primary-side RMS current was measured using the inherent signal statistics feature across two AC line-cycles. The model predictions and simulation results at the CEC operating points are presented in Fig. 3.6. It is clear that model and simulation results are very closely matched, within a maximum of 5% error in most cases, verifying the subsequent optimal design analyses.

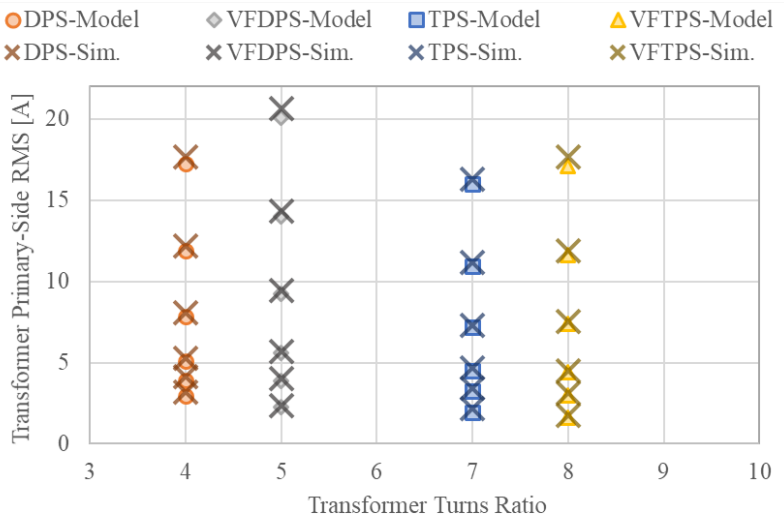


Fig. 3.6. Comparison of the ideal frequency-domain optimization model with corresponding simulations in MATLAB Simulink (data points with 'X' marker) for the considered modulation schemes and topologies.

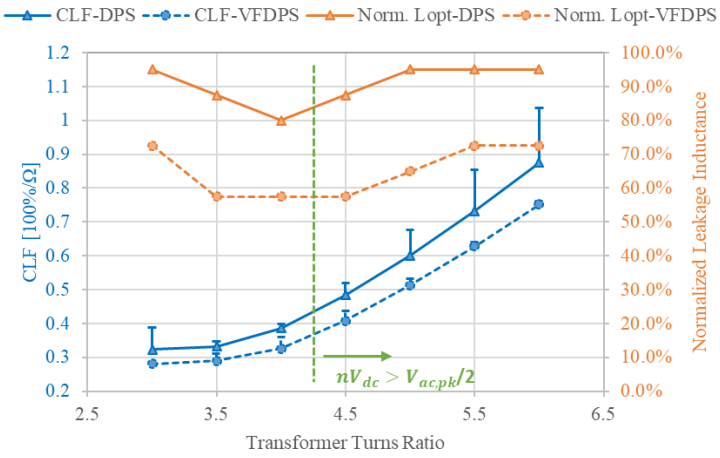
3.3.6. Results

The CLF for the two main topologies and two modulation strategies was extracted using the optimization routine in Fig. 3.5. In particular, the results for fixed-frequency modulation schemes (i.e. DPS and TPS) were extracted considering a switching frequency of 200 kHz. The results are shown for the half-bridge secondary-side and DPS modulations types in Fig. 3.7(a). It is clear that depending on the modulation type considered, the optimal value of leakage inductance where the CLF is minimized is unique. Furthermore, the implication of a non-optimal selection in leakage inductance is clear from the error bars in the CLF plots, where in certain cases the CLF may increase by more than 10%/Ω. With that being said, certain turns ratios near $nV_{dc} = V_{ac,pk}$/r show reduced variability in CLF as a function of leakage inductance. Similar results are presented in Fig. 3.7(b) for the full-bridge secondary-side and TPS modulation types. In each case, the introduction of variable frequency enables further minimization of the CLF, as expected through the introduction of an additional modulation variable and increased range of L_{lk}. An additional trend includes the monotonic increase of the CLF as a function of turns ratio. However, it must be made explicitly clear that this does not mean that lower turns ratios minimize the expected conduction loss in the circuit, as the impact of resistances has not yet been considered. In particular, lower values of turns ratio correspond to higher values of secondary-side resistances reflected to the primary. As such, the final selection of transformer turns ratio can be made on the basis of minimizing,

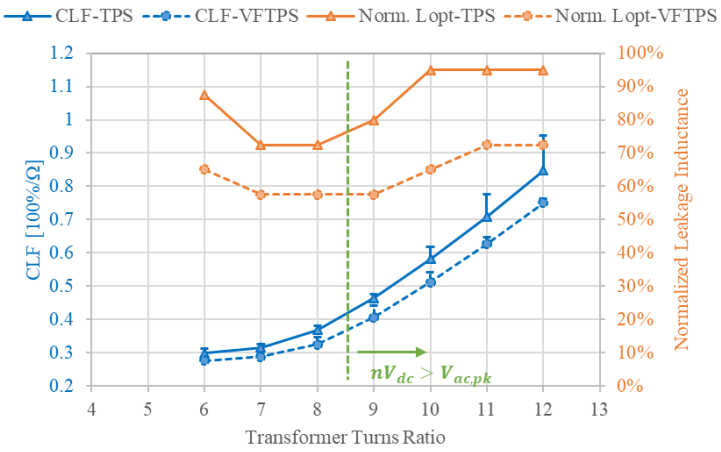
$$P_{cond,drop} = CLF \cdot R_{pri,tot} \tag{3.8}$$

$$R_{pri,tot} = n_{d,p}R_{ds,p} + R_{ac,p} + \left(R_{ac,s} + n_{d,s}R_{ds,s}\right)/n^2 \tag{3.9}$$

where $R_{pri,tot}$ is the total circuit resistance including devices, where $n_{d,x}$ is the number of primary- and secondary-side devices respectively, and transformer windings, reflected to the transformer's primary-side. As such, analysis of the optimal *n* to select is in fact design dependent, whereas the selection of optimal inductance is only a function of the turns ratio. Importantly, if considering lower values of magnetizing inductance relative to the leakage inductance, the primary- and secondary-side currents will become asymmetric (namely $I_{rms,p} \neq I_{rms,s}$) as non-negligible reactive current will be processed in the magnetizing branch. In this case, it could be required to separately consider the CLF on the primary and secondary, multiplied by the resistance on the appropriate side.



(a)



(b)

Fig. 3.7. Optimal CLF and associated normalized leakage inductance ($L_{lk}/L_{lk,max}$) at each turns ratio considering (a) DPS and VF-DPS in the SSHB architecture, and (b) TPS and VF-TPS in the SSFB architecture. In each case, the error bar on the CLF plot corresponds to the range of realizable CLFs for non-optimal leakage inductance selections within the normalized bounds specified in Table 3.2.

3.4. Extension to component selection

As concluded in the previous section, although a specific turns ratio and leakage inductance combination may correspond to the lowest CLF, the designer must consider the impact of the circuit's resistances in light of (3.8)-(3.9). As shown, the CLF cost function is scaled by the circuit's resistances (that are also functions of n and in some

cases also L_{lk} for the transformer) in the calculation of total conduction loss and efficiency drop. This analysis ultimately decides the most optimal set of $\{n, L_{lk}\}$ from the perspective of conduction loss implications to the CEC efficiency.

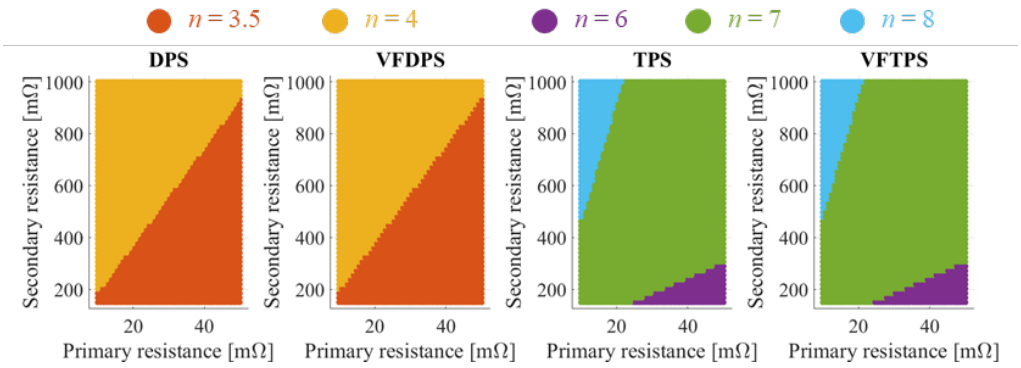
3.4.1. General analyses

Before considering any detailed component selection, a general design space analysis can be performed. Specifically, a vector of resistances are considered on the primary-side, between 10 mΩ and 50 mΩ, and the secondary-side, between 100 mΩ and 500 mΩ, representing typical ranges of total resistance that could be expected on either side. The CEC-related conduction loss drop is then calculated for each set of turns ratios and resistance values according to,

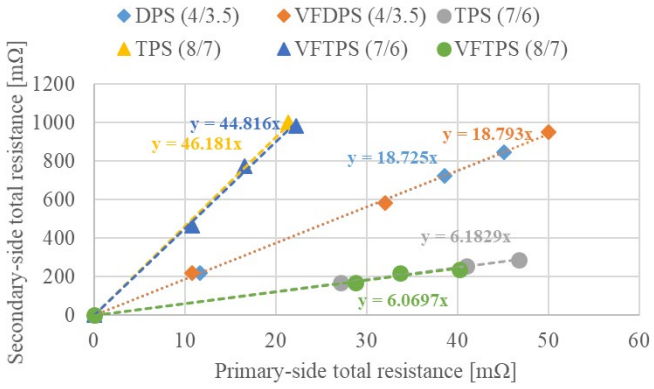
$$P_{cond,drop} = CLF \cdot (R_{p,tot} + R_{s,tot}/n^2) \tag{3.10}$$

where (3.8) is simplified to two lumped resistances on the primary- and secondary-side. For each set of resistances, the turns ratio corresponding to the minimal loss configuration is stored, where generally a minimum exists as the resistance expression decreases as a function of n [cf. (3.10)] while the CLF increases as a function of n (cf. Fig. 3.7). The results of this analysis are shown in Fig. 3.8(a), where it is clear that unique turns ratios are preferred in DPS versus TPS configurations, as a function of the relative secondary-to-primary-side resistance ratio. The results of this figure is summarized in Fig. 3.8(b), where the limit lines were extracted from Fig. 3.8(a), and plotted on a single axis set. To use this figure, the known total primary- and secondary-side resistances can be mapped into the 2D space and compared against the nearest decision line. For example, a design with $R_{p,tot}$ = 30 mΩ and $R_{s,tot}$ = 400 mΩ would have

an optimal turns ratio of 3.5 in a half-bridge, and an optimal turns ratio of 7 in a full-bridge. This analysis is extremely beneficial to the subsequent component selection in Section 3.4.5, as the understanding of which turns ratio to select is strictly shown to be a function of the relative primary- and secondary-side resistances. As a result, only one turns ratio needs to be evaluated as a function of the considered devices and transformer.



(a)



(b)

Fig. 3.8. Extension of the analysis in Fig. 3.7 to the optimal turns ratio selection for minimal CEC conduction loss drop as a function of the total primary- and secondary-side resistances, (a) selection maps for each modulation type, and (b) design space selection map summary with interpolated decision lines for each modulation type. In (b), for a known quantity of primary- and secondary-side resistances, as well as a selected topology and modulation scheme, the optimal n can be determined by mapping the design into the 2D space and evaluating the local position relative to the decision boundaries.

3.4.2. Design example

As a basic design example, the secondary-side indirect full-bridge and indirect half-bridge topologies in Fig. 3.4(a) and (c) were considered with the appropriate modulation schemes. Regarding component selection, the EPC2001C (5.6 mΩ) device was selected on the primary-side and the IPD60R180P7 (145 mΩ) was selected on the secondary-side. As a result, the total considered primary-side resistance is 11.2 mΩ, the secondary-side resistance is 145 mΩ in the SSHB and 290 mΩ in the SSFB, suggesting that the turns ratio of n = 3.5 is optimal for the SSHB [as 145 mΩ < 18.7*11.2 mΩ, cf. Fig. 3.8(b)], while n = 7 is optimal in the SSFB [as 6.1*11.2 mΩ < 290 mΩ < 45*11.2 mΩ, cf. Fig. 3.8(b)], regardless of considering switching frequency as an additional control variable. The results of the general system-level optimization analysis considering all turns ratios for the example component selection plotted in Fig. 3.9 confirm this result. In the case of the SSHB, the optimal value of turns ratio is n = 3.5 considering both VF-DPS modulation ($P_{cond,drop}$ = 1.22%) and DPS modulation ($P_{cond,drop}$ = 1.41%). It is evident that the optimal value of turns ratio is revealed as n = 7 for both the VF-TPS modulation ($P_{cond,drop}$ = 1.01%) and TPS modulation ($P_{cond,drop}$ = 1.12%) considering a SSFB. On another note, it is clear that for both secondary-side realizations of the example design, the optimal turns ratios lies in the bound $V_{ac,rms}/r < nV_{dc} < V_{ac,pk}/r$, with unique values of optimal leakage inductance for each modulation type considered (namely the difference in selection between VF and fixed-frequency-based modulation, cf. Fig. 3.7). Furthermore, SSFB realizations can achieve reduced total CEC conduction loss compared to half-bridge designs, at the cost of additional devices and associated gate driver circuitry. Compared to the traditional design criteria

in which $nV_{dc} > V_{ac,pk}/r$ (i.e. $n > 4.25$ for the SSHB, and $n > 8.5$ for the SSFB), a more optimal selection of turns ratio and corresponding leakage inductance can achieve reduced CEC conduction loss drops up to 0.4%.

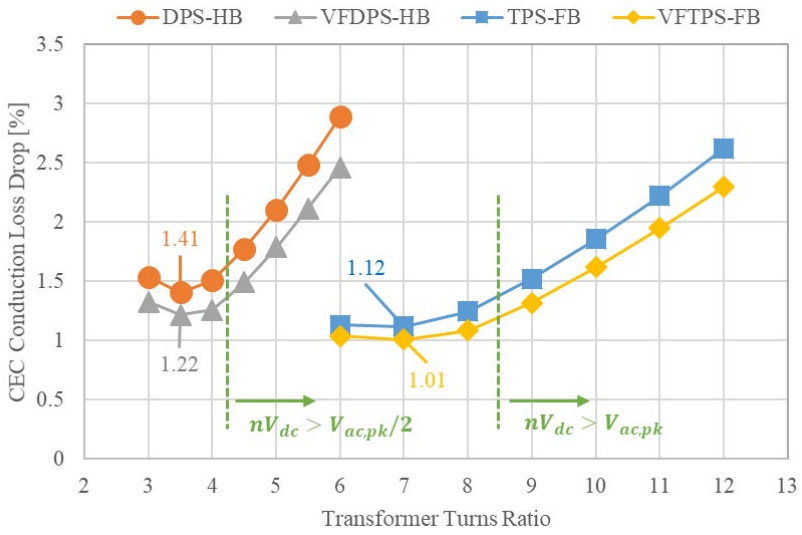
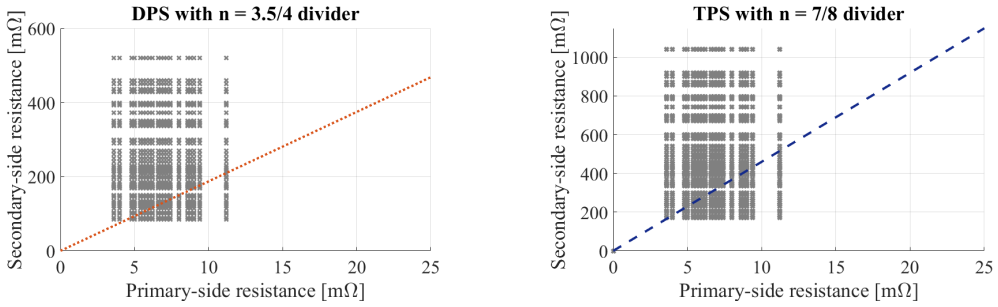


Fig. 3.9. Results of system-level optimization for the example design scenario considering both the SSHB (with DPS and VF-DPS control) and SSFB (with TPS and VF-TPS control). Conventional design selections for n, highlighted in green, lead to higher CEC efficiency drops than corresponding optimum values. In designs considered, this is about 0.25% and 0.4% higher for the SSHB and SSFB, respectively.

3.4.3. Device database and gate driver selection

The CLF analysis was extended to include a wide variety of devices on the primary- and secondary-sides, considering both Si and GaN device technologies. The full design database is shown in Appendix Section A. All possible device configurations in the direct and indirect secondary-side structures are plotted against the nearest decision lines from Fig. 3.8(b) in Fig. 3.10. It is evident that most of the device configurations lie in the bound where the turns ratio should be $n = 4$ for the SSHB and $n = 8$ for the SSFB. As such, only these two designs are henceforth considered. As a result, the optimal leakage inductances can be determined from the analysis presented in Fig. 3.7.



(a) (b)

Fig. 3.10. Total primary- and secondary-side resistances for all considered configurations plotted against the nearest decision line from Fig. 3.8(b) for the, (a) SSHB, and (b) SSFB.

On the other hand, the gate driver dimensions were based on previously developed hardware prototypes, where unique driver configurations were considered when using Si or GaN devices. For GaN devices on the primary-side the gate drive circuitry was based on the LMG1205 (T_{gd} = \$2.19, L = 7.5 mm, W = 8.25 mm), whereas for Si devices on the primary- or secondary-side the gate drive circuitry was based on the SI827x (T_{gd} = \$2.01, L = 16.7 mm, W = 14.7 mm). The final unique gate driver type is used for GaN devices with integrated gate drivers on the secondary-side, where only the area of an additional signal isolator was considered, NCP51530 (T_{gd} = \$0.72, L = 4.8 mm, W = 5.8 mm). Importantly, each of the gate drivers in the high frequency circuit are based on the bootstrap principle, though unfortunately this structure is not applicable on the secondary-side in direct configurations. In this case, a dual-driver is required, which is considered to occupy the same footprint area as the bootstrap approach, though the driver IC is modified from the SI8273 to the SI8274. On another note, only a single unfolder gate driver is considered with a custom design for cost minimization, with details of this structure presented in Appendix Section D.

3.4.4. Objective functions

There are three objective functions to evaluate in facilitating the topological and component selection for the proposed microinverter circuit. First, the cost of the components and associated gate drivers is calculated according to,

$$T = n_{d,p}T_{d,p} + \frac{n_{d,p}}{2}T_{gd,p} + n_{d,s}T_{d,s} + \frac{n_{d,s}}{2}T_{d,s} + n_{d,u}T_{d,u} + \gamma T_{gd,u} \qquad (3.11)$$

where $n_{d,x}$ are the number of devices, $T_{d,x}$ are the price of devices, and $T_{gd,x}$ are the price of gate drivers, where $x = \{p, s, u\}$ corresponds to the primary-side, secondary-side, or unfolder. As shown, the number of gate drivers required is always equal to half of the number of devices, which is to say that only half-bridge or dual-driver configurations have been considered, and a factor of γ was introduced to discern between indirect structures (with unfolder; $\gamma = 1$) versus direct structures (no unfolder; $\gamma = 0$).

The second objective function is the efficiency drop due to conduction loss of the design. This is straightforward to calculate, via (3.8)-(3.9), reshown below as,

$$\eta_{drop} = CLF\left(n_{d,p}R_{ds,p} + n_{d,s}R_{ds,s}/n^2\right) + 2\gamma CLF_u R_{ds,u} \qquad (3.12)$$

$$CLF_u = \sum_{i=1}^{6}\left(\frac{C_i}{P_i}\right)\cdot\left(\frac{P_i}{V_{grid}}\right)^2 = 0.42\%/\Omega \qquad (3.13)$$

where *CLFu* is the conduction loss factor of the unfolder, which is unique from the CLF of the main-circuit as most of the high frequency current in the transformer in indirect configurations is diverted to the differential-mode capacitance between the secondary-side bridge and the unfolder (cf. Fig. 3.1).

The final objective function is the footprint area occupied by the devices and associated gate drivers. This objective can be calculated according to,

$$A = n_{d,p}A_{d,p} + \frac{n_{d,p}}{2}A_{gd,p} + n_{d,s}A_{d,s} + \frac{n_{d,s}}{2}A_{d,s} + n_{d,u}A_{d,u} + \gamma A_{gd,u} \qquad (3.14)$$

where $A_{d,x}$ is the occupied footprint area of the device package, and $A_{gd,x}$ is the occupied footprint area of the gate driver circuit. A summary of the constants utilized in the calculation of the objective functions (3.11)-(3.14) is shown in Table 3.3. Importantly, the type of gate driver to use is also dependent on the device technology and topology considered as indicated in the previous section.

Table 3.3. Number of devices, gate drivers, type of gate driver, and presence of unfolder, determined by location within the topology and device technology.

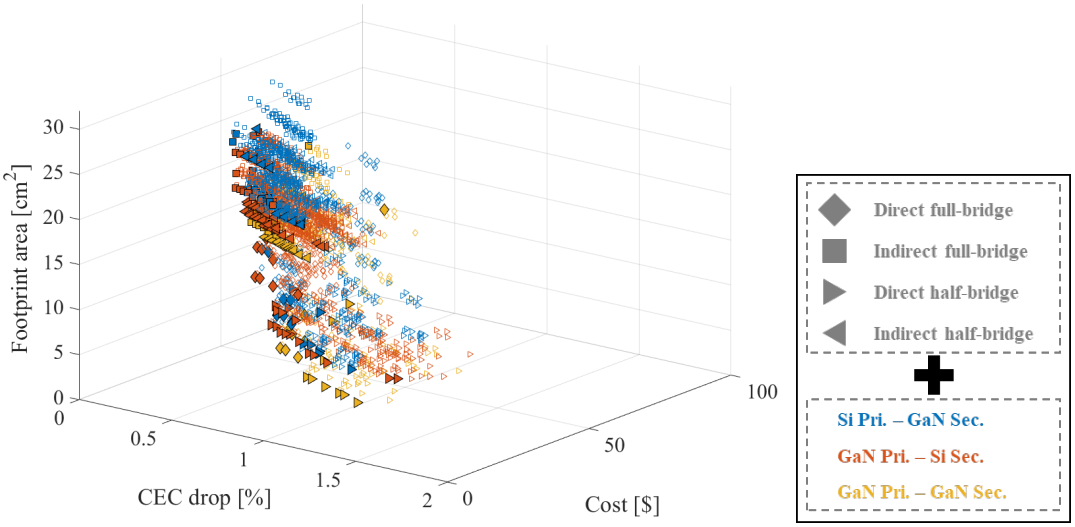
Location	$n_{d,x}$	$n_{gd,x}$	Device technology	Gate driver	γ
Primary ($x = p$) FB	4	2	Si	LMG1205	-
			GaN	SI8273	
Secondary ($x = s$) HB-d / FB-d	4 / 8	2 / 4	Si or GaN	SI8274	0
			GaN (w/ int. GD)	NCP51530	
Secondary ($x = s$) HB-i / FB-i	2 / 4	1 / 2	Si / GaN	SI8273	1
			GaN (w/ int. GD)	NCP51530	

3.4.5. Optimal design results

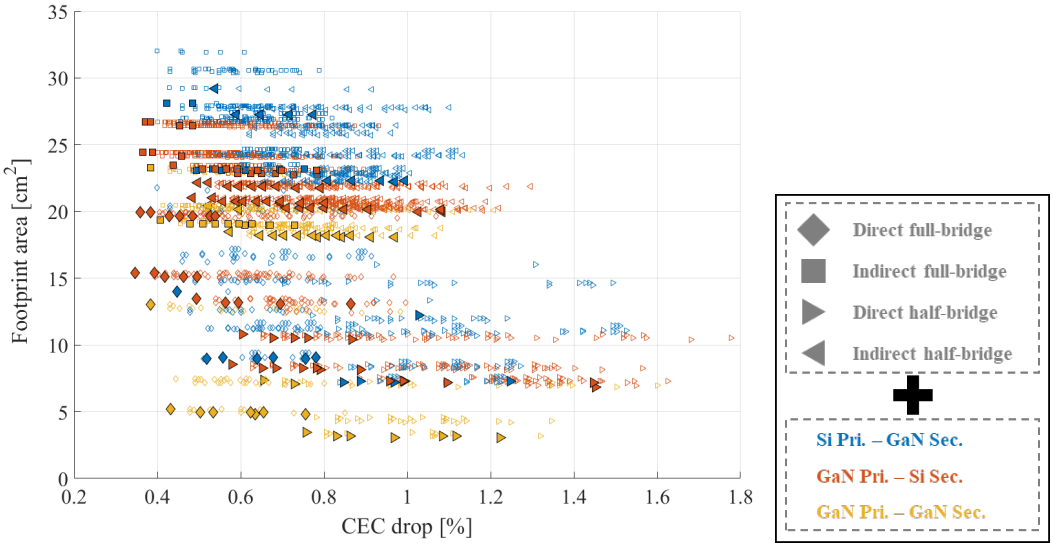
The results of the optimization analysis are shown in Fig. 3.11(a), where all possible configurations of devices and topology were evaluated. While all of the considered design configurations are shown as unfilled colored scatter points, the Pareto-optimal design configurations are shown as larger, filled points, with a black outline. To better understand the tradeoffs between the twelve unique approaches (i.e. four topologies with three device combinations), the 2D representations are shown in Fig. 3.11(b)-(d). The following principal conclusions can be drawn from this analysis:

1) In regards to the trade-off between footprint area and efficiency drop, in Fig. 3.11(b), the Pareto-front is primarily realized by the direct full-bridge topology (diamond marker) with either the GaN-Si (red) or GaN-GaN (yellow) configurations. This is due to the fact that the full-bridge generally has lower losses than the half-bridge, as the current is halved in the full-bridge with respect to the half-bridge and an additional control variable is present, though the number of devices in the conduction path is doubled. Furthermore, the indirect structure with the unfolder and associated gate driver occupies a larger area than the direct structure.
2) The trade-off between cost and efficiency drop is shown in Fig. 3.11(c), where the Pareto-front is realized by SSHB (square marker) and SSFB (left triangle marker) topologies with Si-GaN (blue) and GaN-Si (red) configurations. It is clear that the GaN-Si and Si-GaN configurations perform nearly equally as well across these two objective functions, while the SSHB outperforms in the cost objective and the SSFB outperforms in the efficiency drop objective. Therefore, in more cost sensitive designs, the SSHB configuration is preferable, versus loss sensitive designs where the SSFB would be preferable. In this case, the final decision of whether to go with a GaN-Si or Si-GaN design would be determined by the desired performance over the footprint area objective.
3) The trade-off between footprint area and cost is shown in Fig. 3.11(d), where two unique Pareto-fronts area realized. The bottom left corner highlights that the direct half-bridge designs (right triangle) are most optimal, however if footprint area is not necessarily at a premium the indirect half-bridge designs

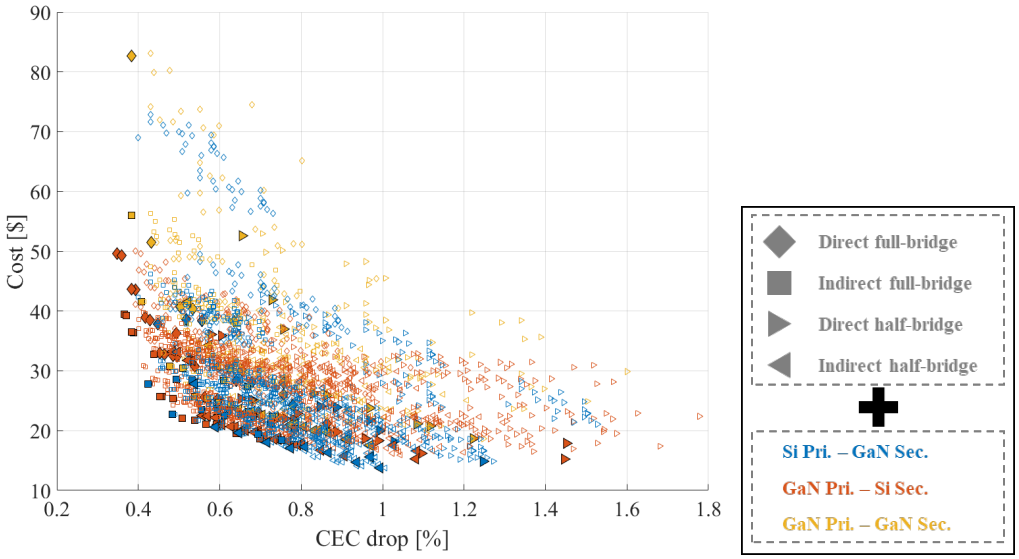
(left triangle) are also preferable. In light of the discussion from the previous cost and efficiency drop trade-off, it is clear that GaN-Si designs in the SSHB structure are more optimal from the footprint area objective than the Si-GaN designs.


Footprint area [cm^2]
30
25
20
15
10
5
0
0
0.5
1
1.5
2
CEC drop [%]
0
50
100
Cost [$]
Direct full-bridge
Indirect full-bridge
Direct half-bridge
Indirect half-bridge
Si Pri. – GaN Sec.
GaN Pri. – Si Sec.
GaN Pri. – GaN Sec.

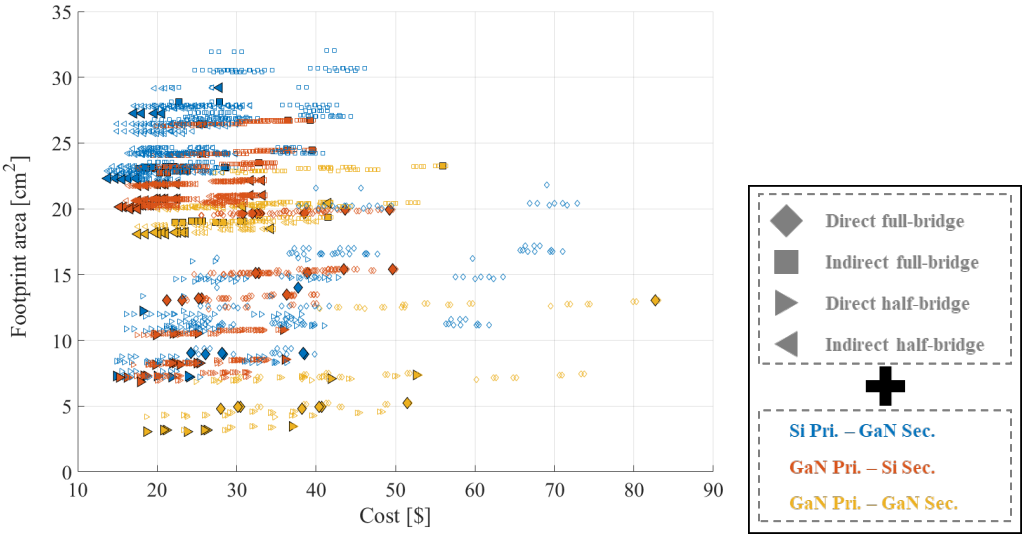
(a)


Footprint area [cm^2]
35
30
25
20
15
10
5
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
CEC drop [%]
Direct full-bridge
Indirect full-bridge
Direct half-bridge
Indirect half-bridge
Si Pri. – GaN Sec.
GaN Pri. – Si Sec.
GaN Pri. – GaN Sec.

(b)



(c)



(d)

Fig. 3.11. Results of multi-objective topology and component selection for the main-circuit, (a) 3D objective space, (b) 2D tradeoff between footprint area and efficiency drop, (c) 2D tradeoff between cost and efficiency drop, and (d) 2D tradeoff between footprint area and cost. In each plot, design candidates are shown as unfilled scatter points, whereas Pareto-optimal designs across the three objective functions are filled with a black outline.

In light of the identified tradeoffs between the three objective functions, a final design can be selected based on the required objectives in the microinverter design. In

particular, the proposed microinverter design should prioritize low cost while enabling high performance. Therefore, the indirect half-bridge designs with the GaN-Si configuration are deemed the final candidate, of which two example designs are highlighted in Table 3.4. The first is the originally selected design, considered for much of the analysis in this dissertation, as the selection was made early on in the research work. The second design is a more optimal configuration, selected based on up-to-date available components, as well as knowledge about more sophisticated loss mechanisms in some Si devices (e.g. C_{oss} hysteresis [109]-[110], generating loss in the device output capacitance even in ZVS conditions), which limits the secondary-side device decision space. It is clear that the updated design analysis can bring some benefits to both cost and CEC efficiency drop with slightly increased footprint area.

Table 3.4. Results of multi-objective design selection for the proposed microinverter.

Design	Topology	Pri. device	Sec. device	Unf. device	T [$]	η_d [%]	A [cm^2]
Original	SSHB	EPC2001C	IPD60R180P7	TK290P60Y	21.7	0.95	20.2
Updated	SSHB	EPC2204	STL33N60M2	IPD60R180P7	18.8	0.77	20.6

3.5. Circuit control

This section presents an extension of the analysis from Chapter 2 as it pertains to DC-AC modulation, as opposed to the previously presented DC-DC operating conditions. While the considered devices are the same, namely the EPC2001C and the IPD60R180P7, the transformer design is the optimally selected planar configuration from Chapter 4, as opposed to the wire-wound transformer from Chapter 2.

3.5.1. Control implementation

The main-circuit should be controlled such that the output current is a smooth sinusoidal waveform, with either unity or variable power factor with respect to the grid voltage. To achieve this goal, the control parameters should be modulated across the AC line-cycle to achieve the desired output current reference. In light of this, the control block diagram of the main-circuit shown in Fig. 3.12 is considered. The main control loops include:

(a) The maximum power point tracking logic, which sets the input voltage reference for the main-circuit. The MPPT logic is based on a simple perturb and observe (P&O) algorithm. The input voltage tracking is then ensured through the use of a PI controller, which sets the direct axis current reference (i.e. the average power reference) for the main-circuit.

(b) The current reference is generated by summing the direct axis current (from the V_{in} control block) with the quadrature axis current reference (from smart grid control and differential mode capacitor feed-forward). The DM current feed-forward term is especially important, as this current must be compensated by the main-circuit, else the output current on the grid-side of the EMI filer would have undesirable phase angle with respect to the voltage.

(c) The main-circuit control can be realized in one of two ways. Here, it is shown to be realized with the combination of look-up-tables (LUTs) for the θ and f_{sw} parameters, alongside a PI controller used to determine δ by ensuring that the converter current into the EMI filter is tracking the desired reference.

(d) An alternative control approach is the fully open-loop implementation where all of the control parameters are fed from a LUT as a function of the input voltage, grid voltage, and current reference.

(e) Smart grid control implementation including primarily a phase lock loop which determines the grid frequency, instantaneous grid angle, and amplitude of the grid voltage, through manipulation of the measured grid voltage. The simple DQ-axis SOGI PLL is shown in the Appendix Section C. Additionally, the converter requires smart-grid control functionality, which are explained in the CA rule 21 supplemental addition of UL 1741. For representative purposes, only the voltage ride through (VRT) and Volt-VAr control blocks are shown, though many more functionalities are required.

While the use of the closed-loop implementation in (*c*) has merits from a control perspective, it necessitates the use of an additional current sensor and associated dedicated circuitry, which increases the cost of the final prototype, and requires careful implementation of the controller for stability across the wide range of possible operating conditions. In contrast, the fully open-loop approach in (*d*) is the lowest cost solution requiring no additional current sensors or analog circuitry, however it is imperative that the delivered modulation parameters generate the desired output current. Therefore, the use of the fully open-loop approach can only be enabled with a corresponding high accuracy representation of the main-circuit, which was characterized in Chapter 2. Henceforth, the fully open-loop control implementation will be considered, where only characterization of the various LUTs is required.

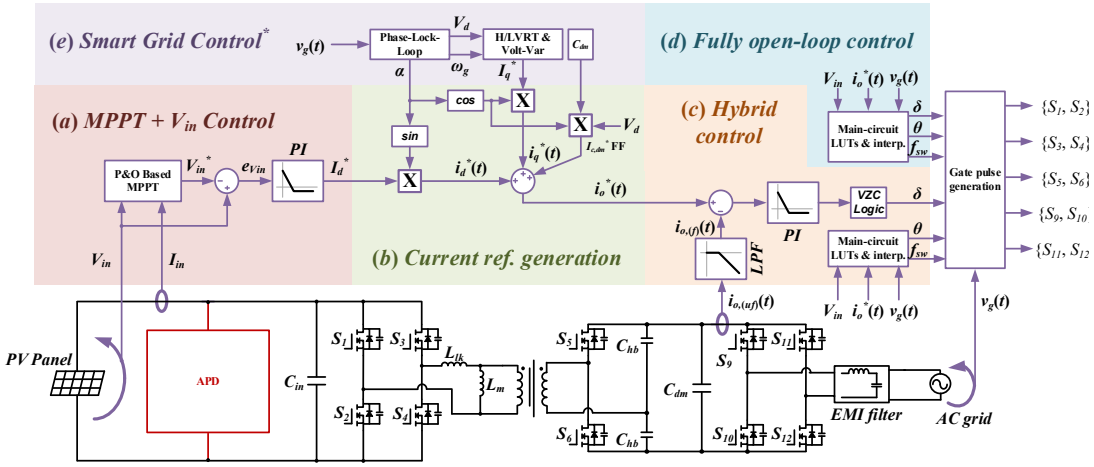


Fig. 3.12. Control implementation for the main-circuit based on either the hybrid utilization of LUTs in and a closed-loop controller in (*c*), or the full utilization of LUTs in (*d*). Other sections of the control implementation include MPPT and V_{in} control in (*a*), current reference generation in (*b*), and smart grid control considerations in (*e*). Importantly, the shown smart grid controls in (*e*) are very limited, and are purely for representative purposes (*).

3.5.2. IAM implementation for DC-AC

As shown in Fig. 3.12, the LUTs should take the input voltage, output voltage, and current reference as inputs, and output the corresponding modulation parameters. To derive these LUTs, the analysis from Chapter 2 can be leveraged to DC-AC analysis through the following procedure. First, the operating space is discretized across the three input dimensions, with v number of input voltage points, o number of output voltage points, and c number of grid current points. The set of allowable input parameters and the corresponding discretization numbers are indicated in Table 3.5.

Table 3.5. Range and discretization of the three LUT inputs.

Input voltage [V] / v	Grid voltage [V] / o	Grid current [A] / c
[30, 60] / 16	[0, 170] / 12	[-1, 2.5] / 35

For a given value of grid voltage and grid current, the power reference for the circuit is decided according to V_g*I_g. With a given value of input voltage, the scenario can be translated to the following constrained numerical optimization problem shown

in Fig. 3.13. In particular, for a given value of input and output voltages, the modulation parameter set should be determined such that the power transfer reference is met, the devices achieve ZVS (hence minimizing switching losses), and the transformer RMS current is minimized (hence minimizing the conduction losses). To facilitate the numerical optimization problem, MATLAB's inherent '*fmincon*' function is considered to navigate the decision space with the '*interior-point*' algorithm, while the developed IAM_3 algorithm returns the RMS current, power transfer, and ZVS transition types of the devices, for a specific input voltage, output voltage, and set of modulation parameters. In some operating conditions, it may not be possible to ensure ZVS for all of the devices, at which point ensuring ZVS of the Si devices is prioritized over the GaN devices. Nevertheless, at most only one primary-side leg will experience hard-switching, and the corresponding loss penalty will be low.

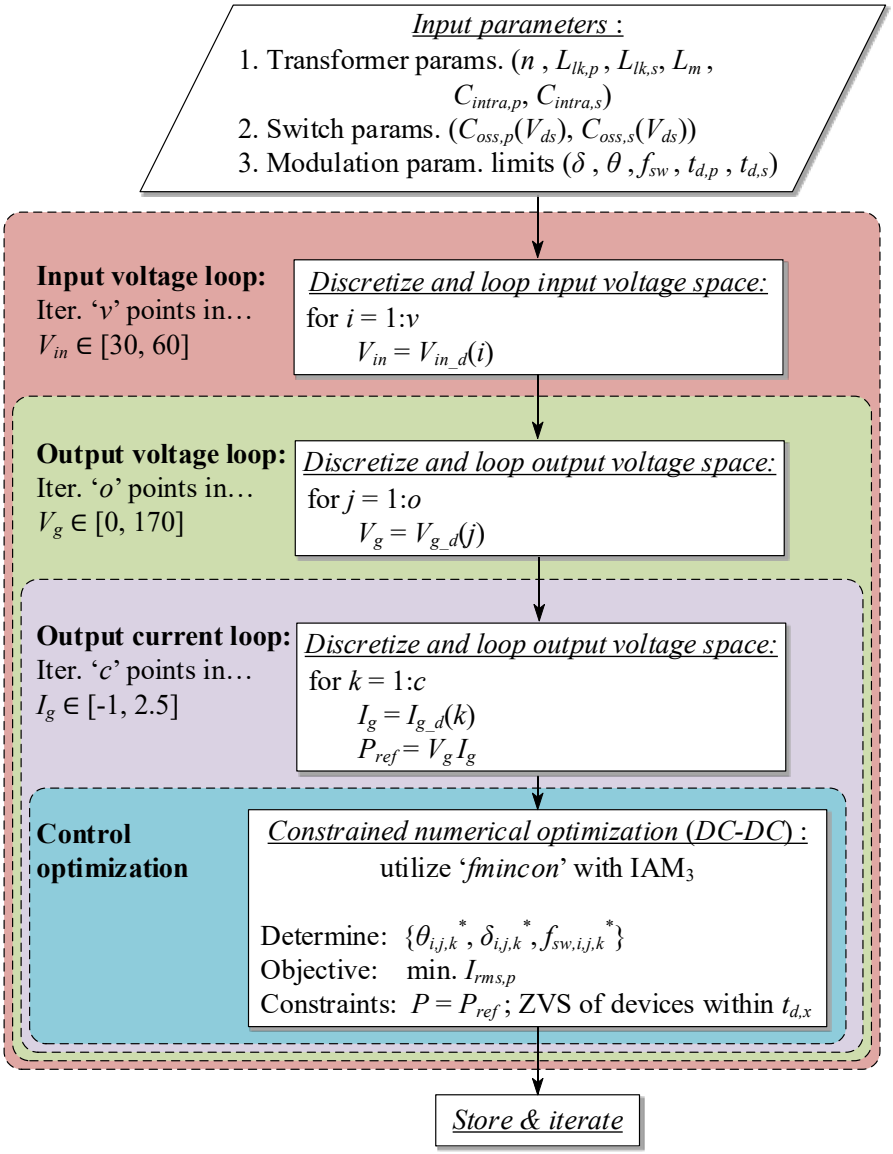
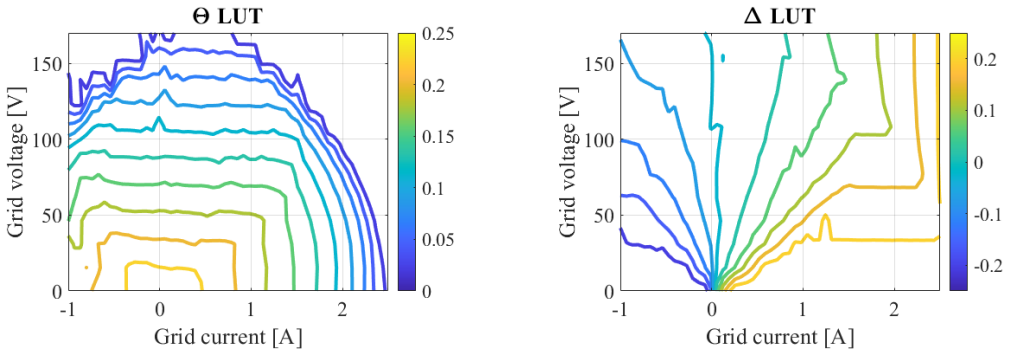


Fig. 3.13. Block diagram of the constrained numerical optimization procedure used to develop the main-circuit LUTs.

The results of the LUT derivations are provided in Fig. 3.14 for the θ and δ modulation parameters as a function of the grid voltage and current, at a given input voltage level of 40 V. The final modulation parameter f_{sw} is utilized to ensure wider variation of power for conditions in light of (3.7), else the switching frequency is maintained at 200 kHz. A more careful manipulation of the switching frequency to

further minimize conduction-related losses as presented in Fig. 3.7, or enable the minimization of EMI noise, is feasible but not considered at this time for simplicity.



(a) (b)

Fig. 3.14. 2D LUT contour plots for the (a) θ LUT, and (b) δ LUT. In this example, the input voltage is set to be fixed at 40 V.

3.5.3. LUT interpolation

In the previous section, analysis began by discretizing the operating region for each of the three input signals. However, in the hardware it will rarely be the case that the exact modeled operating scenarios are present without sufficiently small discretization of the operating space; instead, the input signals will be arbitrarily within the discretized space. As a result, an interpolation strategy is preferred to ensure that the converter tracks the proper power level for a given input and output voltage. The interpolation strategy is shown pictorially in Fig. 3.15, where a trilinear interpolation method is considered [43].

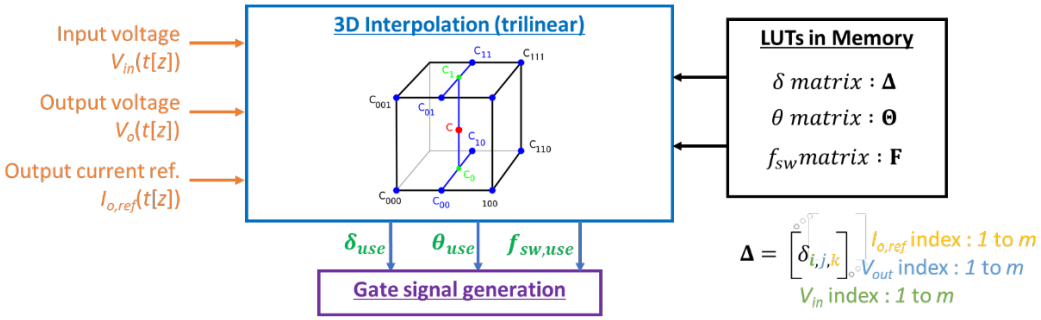
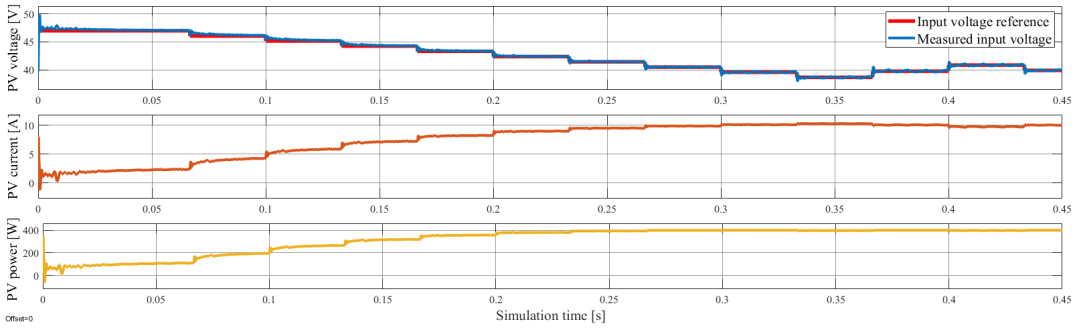


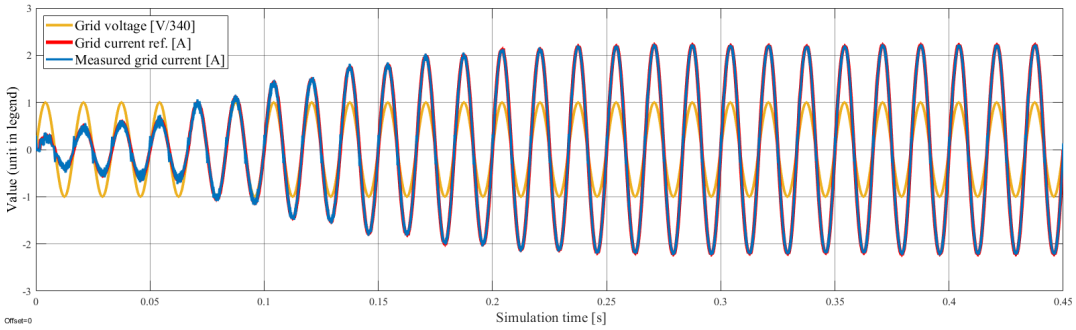
Fig. 3.15. Block diagram of trilinear interpolation algorithm.

3.5.4. Simulation results

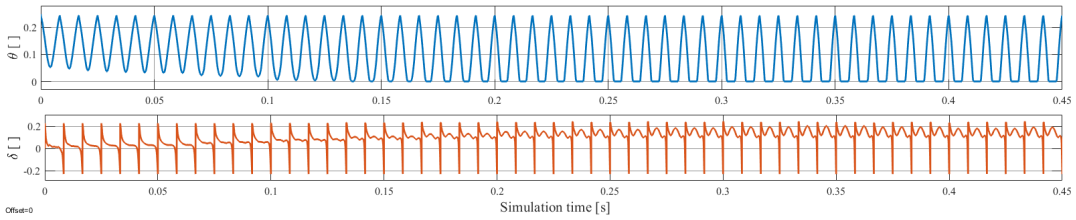
Simulation results were performed considering the OAM modulation strategy (as the simulation model is ideal, not considering device commutations during dead-time) to validate the proposed modulation analyses and interpolation algorithm. At the input, a PV panel was considered from Fig. 3.3 with a maximum power point of 400 W at 40 V. The APD was also active in the simulation to ensure double-line-frequency power buffering, though the details are withheld until Chapter 5. The results of the simulation considering start-up from the open-circuit voltage to the maximum power point are shown in Fig. 3.16. In particular, the input PV waveforms are shown in Fig. 3.16(a), where it is clear that the P&O type MPPT algorithm reaches, and then oscillates around, the maximum power point. On the other hand, in Fig. 3.16(b) the grid current is shown to be a smooth sinusoid with near-unity power factor with respect to the grid voltage. Finally, Fig. 3.16(c) shows that to achieve the power transfer and grid current shaping, the converter modulation parameters are dynamically varying across the line-cycle as a function of the measured input voltage, output voltage, and grid current reference, validating the proposed control scheme.



(a)



(b)



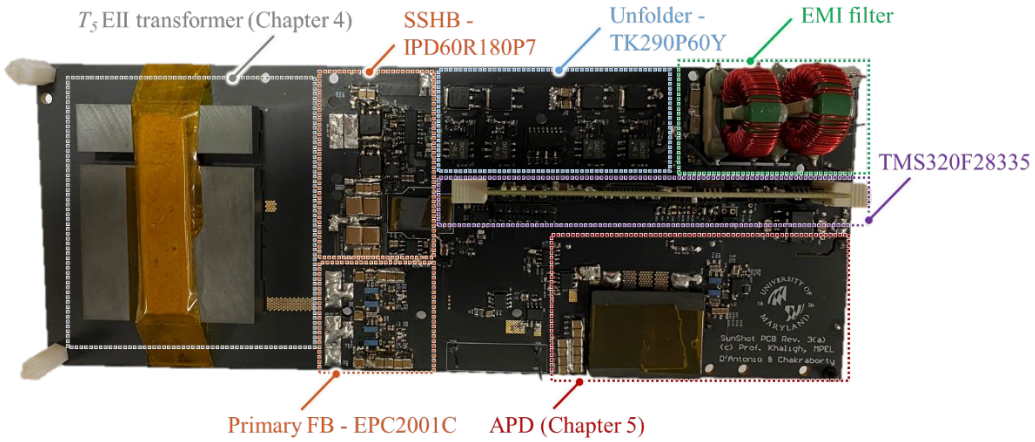
(c)

Fig. 3.16. Ideal simulation results of the microinverter circuit with a PV panel input and grid load, considering the proposed open-loop control approach with 3D trilinear interpolation, (a) input PV waveforms, (b) grid waveforms, and (c) modulation parameter variation.

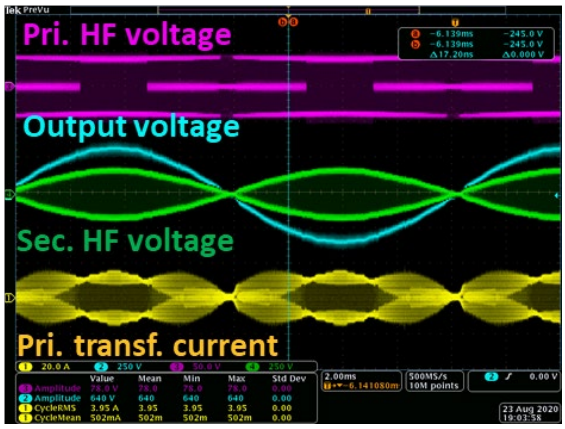
3.5.5. Experimental results

The converter hardware in Fig. 3.17(a) was assembled with the devices from Table 3.4 and the optimal transformer from Chapter 4. Experimental validation of the proposed IAM_3 modulation parameters in Fig. 3.14 were evaluated, where the converter was connected to a resistive load. The LUTs were delivered from the TMS320F28335 digital signal processor (DSP) according to the sensed input voltage,

output voltage, and desired grid current. The results of the experimental analysis are shown in Fig. 3.17(a), where the output current (and hence voltage due to the presence of the resistive load type) is shaped with a very low THD less than 3% as measured in Fig. 3.17(b). Furthermore, the efficiency at this power level is high at 96.7%



(a)



(b)

(c)

Fig. 3.17. Experimental results of the proposed modulation strategy at the 200 W power level, (a) experimental hardware prototype, (b) experimental electrical waveforms, and (c) experimental efficiency and THD measurements.

3.6. Summary

This chapter has discussed a holistic multi-objective analytical approach towards parametric selection of transformer parameters, as well as topology and component selection, of a DAB-based single-stage microinverter topology. Specifically, turns ratio (n) and leakage inductance of the transformer (L_{lk}) were considered as parametric design variables, in conjunction with four topological variations and associated control schemes, and component databases consisting of Si- and GaN-based primary- and secondary-side devices. To reduce the amount of design iterations to consider, a decoupled design framework was proposed. First, a CEC-weighted conduction loss term, deemed the CLF, was developed to characterize the optimal leakage inductance as a function of the turns ratio. Second, the optimal CLF as a function of turns ratio was multiplied by resistance vectors for the primary- and secondary-side to calculate the total circuit conduction loss as a function of resistance and turns ratio. The analysis revealed that in general, lowest CLF is achieved for a choice of n different from the conventional design choice of $nV_{dc} > V_{ac,pk}/r$, but instead $V_{ac,rms}/r < nV_{dc} < V_{ac,pk}/r$, where in fact the optimal turns ratio is shown to be a function of the relative primary- and secondary-side total resistances. The previous conclusions were finally leveraged to facilitate multi-objective trade-offs analysis of component cost, footprint area, and CEC efficiency between the four considered topologies and comprehensive component selection considering Si and GaN device technologies. For the proposed application aiming at cost minimization with good performance across the footprint area and efficiency drop metrics, the secondary-side half-bridge structure

with GaN-based primary-side devices and Si-based secondary-side devices was deemed to be the optimal configuration.

Furthermore, the implications of component selection on the control implementation in DC-AC operation were discussed. The accurate DC-DC steady-state analyses in Chapter 2 were leveraged for DC-AC control implementation, facilitating a fully open-loop control based on sensed values of input voltage, grid voltage, and grid current reference. The control principle was shown to rely on 3D LUTs for the modulation parameters, which were derived via constrained numerical optimization, and delivered to the system via trilinear interpolation. Simulation results confirmed the performance of the control implementation in a MPPT condition, where the converter operation varies greatly as the PV operating point navigates towards the maximum power point. Finally, a 400 W experimental prototype was developed based on the results of the design optimization analysis, which achieved an efficiency of 96.7% at the 200 W operating point, with a low THD of less than 3%. Future work can involve the minimization of the LUT memory space (i.e. minimizing the discretization indices for the three input signals) such that the converter operates properly, within the THD and power quality requirements.

Chapter 4. Transformer Analytical Comparison, Design, and Optimization

One of the most critical components in the proposed microinverter circuit is the transformer. The transformer contributes to loss in the system through both conduction in the windings, and core loss in the transformer core. As shown in the experimental results from the previous section, a poorly designed transformer can significant degrade the system efficiency. Furthermore, the transformer can potentially realize a large volume, occupying both footprint area and system height. With these two design details in mind, the transformer will be thoroughly analyzed and optimized in this chapter. A portion of the analysis and results presented in this chapter are published in [44].

4.1. Review of design principle in magnetics

In general, magnetics modeling comprises of three main components. First, it is desirable to theoretically estimate how much inductance a certain design may generate, which can be analyzed with reluctance modeling. Second, under a given excitation, understanding the expected within the core is important, which can be determined through theoretical core loss calculation. Finally, analysis of expected resistance can be performed as well, such that the winding losses can be predicted.

4.1.1. Reluctance modeling

Reluctance modeling is an important tool in magnetics design to translate the magnetic component into an equivalent electrical model, facilitating analytical predictions of parameters such as flux density and inductance. In the reluctance model,

applied magneto-motive-forces (MMF) are realized by voltage sources, and the core reluctance is realized by a resistance. Furthermore, the flux in the core is analogous to the current in the equivalent circuit, from which flux density can be calculated through dividing the flux by cross-section area. Example analysis is presented for a simple inductor in Fig. 4.1, with its equivalent reluctance model. As shown, the inductor is realized by a simple EE type core pair, with windings wound around the center leg, where the windings can be represented by a voltage source, of magnitude $MMF = N_p I_p$.

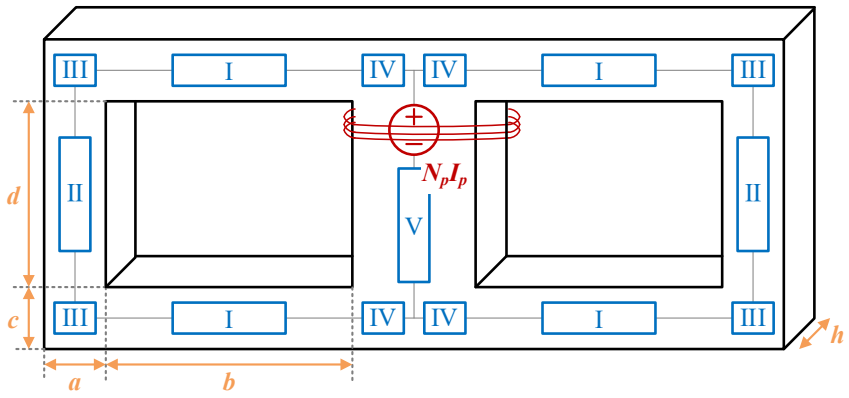


Fig. 4.1. Equivalent reluctance model of an example inductor.

As shown, there are five unique reluctances, of which each can be calculated through the conventional reluctance equation,

$$\mathcal{R}_i = \frac{l_{e,i}}{\mu_{r,i}\mu_0 A_{e,i}} \tag{4.1}$$

where $\mu_{r,i}$ corresponds to the relative permeability of the core section, $l_{e,i}$ is the effective magnetic path length (MPL) of the given section, and $A_{e,i}$ is the cross-section area of the section. To represent the reluctances of the corner sections, slight variation to the MPL and cross-section area are required, detailed in Table 4.1, due to the fact that the flux crowds towards the inside of the corner [45].

Table 4.1. Approximation for core dimensions in the various core sections [45].

Section	$l_{e,i}$	$A_{e,i}$
I	b	ch
II	d	ah
III	$\frac{\pi(a+c)}{8}$	$\frac{h(a+c)}{2}$

The equivalent reluctance model in Fig. 4.1 can be reduced to a simplified reluctance model where the resistances in each leg can be combined to a single equivalent resistance in series with the voltage source. The inductance can hence be calculated via the following two equations,

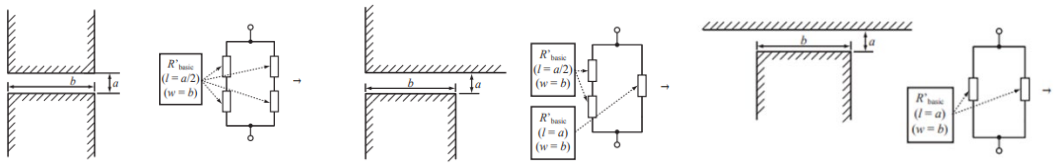
$$R_{tot} = \frac{(R_{eq,L} + R_{eq,R})}{2} + R_{mid} \tag{4.2}$$

$$L = \frac{N_p^2}{R_{tot}} = N_p^2 A_L \tag{4.3}$$

where A_L is the inverse of the total reluctance, termed the inductance factor, typically measured in [nH/turns^2]. The inductance factor for an example EE 32/16/9-3F36 core was theoretically calculated to be 6500 (L = 104 μH for 4 turns), where the inductance factor in simulation was determined to be 6625 (L = 106 μH for 4 turns), validating the analysis.

Aside from reluctance generated by the core, oftentimes air-gaps are intentionally placed in the core structure for additional controlled reluctance, typically used to reduce flux density. Furthermore, placement of the air-gap enables inductance control that is generally independent of the core material properties, enhancing manufacturability and repeatability of the design. Due to the unity relative permeability of air, the air-gap reluctance is typically much larger than that of any other core

reluctance [cf. (4.1)]. Therefore, it is critical to accurately model the air-gap reluctance, else predictions of inductance and other magnetic properties may be incorrect. In particular, it is important to consider the effect of fringing flux in the air-gap, which was evaluated and modeled in detail in [63]. The principal results regarding air-gap modeling is highlighted in Fig. 4.2, where up to three different air-gap setups can be realized.



(a) (b) (c)

Fig. 4.2. Equivalent reluctance for three unique air-gap types, (a) type-1, where two core pieces of same width are separated by an air-gap, (b) type-2, where two core pieces of differing widths are positioned flush to one side and separated by an air-gap, and (c) type-3, where a core pieces is separated from a horizontal core piece with an air-gap [63].

In each case, the effective air-gap reluctance is constructed by specific manipulations of a basic air-gap reluctance [63],

$$R'_{basic} = \frac{1}{\mu_0 \left[\frac{w}{2l} + \frac{2}{\pi}\left(1 + \ln\left(\frac{\pi h}{4l}\right)\right)\right]} \tag{4.4}$$

Using the basic reluctance, R' can be calculated for each air-gap type based on the analysis in Fig. 4.2, where then the effective gap cross-section area is increase (i.e. the reluctance is decreased) by two factors [63],

$$\sigma_y = \frac{R'}{\left(\frac{a}{\mu_0 b}\right)} \tag{4.5}$$

$$\sigma_x = \frac{R'}{\left(\frac{a}{\mu_0 t}\right)} \tag{4.6}$$

The 3D fringing factor can hence be calculated by the product of the two 1-D fringing factors, and the effective air-gap reluctance can be calculated via [63],

$$\mathcal{R}_{gap} = \frac{l_{gap}}{\mu_0 A_{gap}} \sigma_x \sigma_y \tag{4.7}$$

Using the previously presented air-gap correction approach, the inductance factor for the example case in Fig. 4.3 was calculated with an EI 32/16/9-3F36 core pair, and an air-gap of 0.1 mm. According to Fig. 4.2, the example case has a type-1 air-gap in the *yz*-plane and a type-3 air-gap in the *xz*-plane. The inductance factor was analytically calculated to be 1406 (L = 22.5 μH for 4 turns), which is very close to the simulated vale of 1400 (L = 22.4 μH for 4 turns).

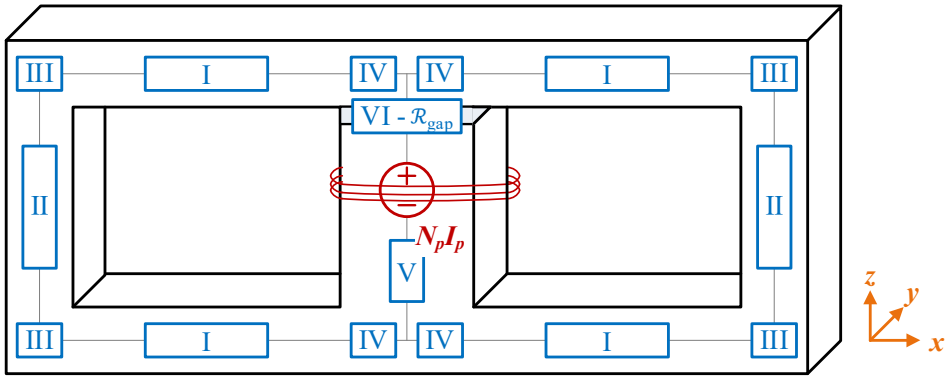


Fig. 4.3. Example inductor considered with center-leg air-gap to evaluate the accuracy of reluctance modeling with air-gaps.

4.1.2. Core loss modeling

Accurate calculation of core loss is critical to predict the amount of losses in the core, affecting both the electrical efficiency, and requirement of thermal management. The most generic core loss calculation tool is the improved Generalized

Steinmetz Equation (iGSE), which can determine accurately the losses in the given core, regardless of the shape of the excitation [66]. The iGSE is given by the following formula,

$$P_{igse} = \frac{k_i \left(\Delta B_{pp}\right)^{\beta-\alpha}}{T} \sum_m |B_{m+1} - B_m|^{\alpha} \cdot (t_{m+1} - t_m)^{1-\alpha} \tag{4.8}$$

where $\{k_i, \beta, \alpha\}$ are the Steinmentz coefficients for a particular core material, T is the period of the excitation, and B_m is the flux density at time t_m, and ΔB_{pp} is the peak-to-peak flux density of the overall periodic loop. To calculate the total power loss, the summation is performed at 'm' points across the periodic flux excitation where variation in B is nearly linear. While increased number of points will inevitably lead to improved calculation accuracy, known excitation waveform shapes can enable significantly reduced computational complexity, which will be exploited later.

4.1.3. Resistance modeling

Prediction of resistance in magnetics is a particularly difficult topic. DC resistance is straightforward to calculate via traditional resistance formulations,

$$R_{dc} = \frac{\rho l_w}{h_w d_w} \tag{4.9}$$

where ρ is the resistivity of the material (typically copper for PCB traces), l_w is the total winding length, h_w is the trace width, and d_w is the trace thickness. However, in isolated power electronics applications, the transformer current is typically composed of a near-zero DC component and multiple switching frequency components. As such, determination of conduction losses is due to the RMS current squared, multiplied the transformer AC resistance, at each frequency harmonic.

Determination of AC resistance depends on the transformer core structure as well as the winding design, and is a function of two mechanisms namely the skin effect and proximity effect. The skin effect describes the effective cross-section area through which high frequency current actually flows through the conductor, whereas the proximity effect considers the effect of placing multiple current carrying conductors in proximity with one another [70]-[71]. Basic DC-to-AC resistance ratio formulations can be predictive for sorting between a good winding design and a potentially poor winding design. The most commonly used approximations is Dowell's equation,

$$F_{r,l} = \left(\frac{R_{ac}}{R_{dc}}\right)_l = \Delta' \left[\zeta_1' + \frac{2}{3}(m_l^2 - 1)\zeta_2'\right] \tag{4.10}$$

$$\Delta = \left(\frac{d_w}{\delta(f)}\right) \tag{4.11}$$

$$\zeta_1' = \frac{\sinh(2\Delta) + \sin(2\Delta)}{\cosh(2\Delta) - \cos(2\Delta)} \tag{4.12}$$

$$\zeta_2' = \frac{\sinh(\Delta) - \sin(\Delta)}{\cosh(\Delta) + \cos(\Delta)} \tag{4.13}$$

where $F_{r,l}$ is the effective AC-to-DC resistance ratio at winding layer l, m_l is the MMF at a particular winding layer, $\delta(f)$ is the frequency-dependent conductor skin depth, Δ is the penetration ratio, ζ_1' is the skin effect factor, and ζ_2' is the proximity effect factor, and for simplicity a unity porosity factor was considered [71]. Dowell's equation assumes that the transformer winding structure only includes MMF variation in the z-dimension, however other manuscripts have noted that indeed MMF variation is multi-dimensional, and the placement of air-gaps in the core complicates the analysis further [62].

From a purely qualitative measure, Dowell's equation can be pictorially applied to the two transformer cases in Fig. 4.4. In Fig. 4.4(a) the primary- and secondary-side windings fully separated, where the MMF distribution increases to *NI* and then back to zero. On the other hand, Fig. 4.4(b) shows the primary and secondary windings fully interleaved, and hence the MMF distribution in the windings is shown to be alternatively *I* or zero. Based on Dowell's equation in (4.10) and the two transformer windings structures in Fig. 4.4, it is clear that the design in Fig. 4.4(a) would have an increased AC resistance than the case in Fig. 4.4(b), due to the higher value of m_l in each winding layer. While several approaches have been introduced in the literature to predict AC resistance as a function of DC resistance via the H-fields in the proximity of the windings, the most trustworthy tool to analyze AC resistance is through the help of 3D FEA simulation in ANSYS Maxwell. The approach used in the following sections is to analyze several designs in 3D FEA simulation to heuristically determine estimated values of DC-to-AC resistance ratios for a particular design type.

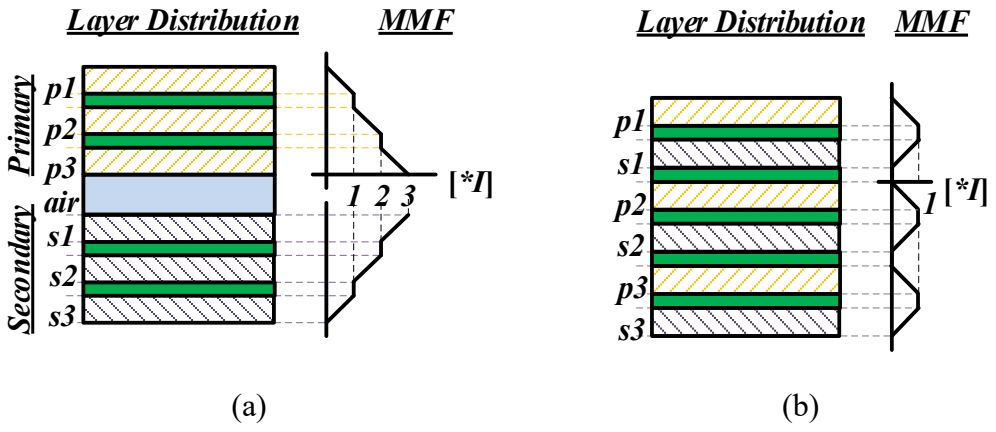


Fig. 4.4. Example winding structures for AC resistance qualitative analysis, (a) separated primary- and secondary-side windings, and (b) interleaved primary- and secondary-side windings.

4.2. Leakage-integrated transformers

High-frequency transformers are at the heart of many widely used isolated power converter topologies like flyback, phase-shifted-full-bridge (PSFB), resonant (LLC, CLLC), and dual-active-bridge (DAB), among others [46]. In flyback and PSFB-based topologies, the leakage inductance of the transformer is an undesirable parasitic element, which leads to voltage spikes across switches and is thus intended to be kept as low as possible in a good design. On the contrary, resonant and DAB-based topologies include an impedance network between the primary and secondary side of the transformer, consisting of series and parallel inductances. The series inductor acts as an energy storage and delivery element and is hence not intended to be minimal. Rather, its value should be high enough to satisfy power-flow, voltage-gain, and zero-voltage-switching (ZVS) requirements of the circuit.

Traditionally the inductance network would be realized by a discrete series inductor and a near-ideal transformer with low leakage inductance, represented in Fig. 4.5 when $\alpha_L \approx 1$ and $\alpha_p \approx \alpha_s \approx 0$. More recently, following the trend to design converters with low cost, low loss, and high power density, integration of the series inductor and transformer has been proposed, where the series inductance is realized by the transformer's leakage inductance [47]. To further improve the performance of the integrated structure, an increase in circuit switching frequency has been coupled with the utilization of planar cores with low profile height [47]. The integrated transformer case is also shown in Fig. 4.5 where $\alpha_L \approx 0$ and $\{\alpha_p, \alpha_s\} \neq 0$, and hence the inductance distribution in the transformer could be arbitrarily designed.

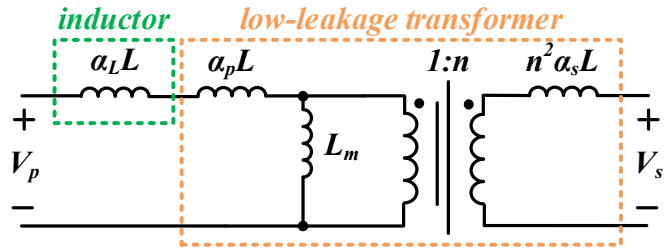


Fig. 4.5. General magnetics implementation consisting of an inductor and transformer. In non-integrated magnetics applications, the series inductor (with $\alpha_L \approx 1$) and ideally low leakage transformer (where $\alpha_p \approx \alpha_s \approx 0$) are implemented with independent core and winding sets. In integrated magnetics applications, the series inductor can be eliminated (with $\alpha_L \approx 0$) as the desired inductance is integrated into the transformer's leakage inductance. For the integrated case, the inductor's distribution could be arbitrarily set, where $\alpha_p + \alpha_s \approx 1$ when L_m is sufficiently larger than L.

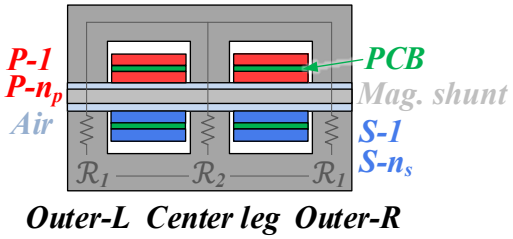
Previous literature has investigated different ways to controllably achieve desired values of leakage inductance and magnetizing inductance into a single transformer structure [47]-[61]. In general, the techniques for leakage integration involve manipulation of the transformer core structure [49]-[51], insertion of additional magnetic materials into the core structure [52]-[58], or manipulation of the winding structure [59]-[61]. The approach in [49] considers the use of vertically stacked transformer and inductor cores, exhibiting limitations in complex transformer core implementation and multiple winding PCBs. An improved planar-based matrix transformer implementation is considered in [50]-[51], where the magnetics core structure includes designated legs and flux paths for a series inductance and ideal transformer.

In [52]-[54], the primary- and secondary-side windings are both wound around the transformer core center leg, and controllable leakage inductance is realized by placing an intentional air-gap between the primary- and secondary-side windings, as shown in Fig. 4.6(a). Importantly, this winding structure requires separate PCBs for the two windings, which may compromise cost and manufacturability of the transformer.

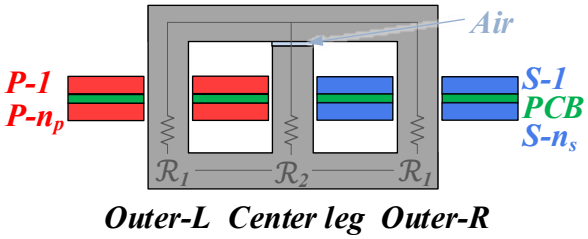
Furthermore, the maximum achievable leakage inductance is limited by the height of the air-gap between the windings. An alternative approach for this winding configuration with axial air gap separation between the primary- and secondary-side windings is presented in [55], where limitations exist in the usage of non-planar windings and maximum limits on the leakage inductance. To circumvent the limitation in maximum leakage inductance in air-gap implementations, [56]-[58] propose the use of a magnetic shunt (i.e. an additional core material with larger than unity permeability) located in the gap between the windings, also shown in Fig. 4.6(a). However, the magnetic shunt increases the transformer core complexity and assembly cost, incurs additional core loss in the transformer, and has temperature-dependent permeability leading to non-stable leakage inductance [54]. Furthermore, [52]-[57] do not achieve good winding interleaving, which will increase conduction-related losses due to the large DC-to-AC resistance ratio. A further extension in [58] proposes to include winding sets both on the transformer center leg as well as the magnetic shunt, which will have difficulties in manufacturability and conduction loss.

With regards to winding manipulation, [59] proposed to wind the primary- and secondary-side windings around the outer-left and outer-right legs of the transformer, shown in Fig. 4.6(b). In this design, hereby termed the "Shell" transformer, controllable leakage inductance is generated through proper design of the core center leg. However, while the windings could be implemented on a simple two- or four-layer PCB with minimal complexity, the transformer has a large footprint area, as the windings fully extend outside the transformer core. Furthermore, the AC resistance in this design is high, as the windings are not interleaved.

To address the issue of high AC resistance in the shell transformer, [60] proposes to wind the primary- and secondary-side windings asymmetrically (i.e. placing a different number of primary- and secondary-side turns) around the outer legs of the transformer core as shown in Fig. 4.6(c). In light of the winding structure, this transformer is henceforth deemed the asymmetrically-wound controllable leakage transformer (ACL). By asymmetrically distributing the windings, controllable leakage inductance can be generated by tuning the core reluctances, and winding interleaving is achieved. However, the winding structure is complex, as windings need to be routed around both the left and right core legs. Furthermore, for the advantages in AC resistance from winding interleaving, the structure has high overlap area between the primary- and secondary-side windings, which could generate undesirable amounts of inter-winding capacitance. A similar approach is also proposed in [61], however the windings are not interleaved as effectively as in [60], and hence will likely result in increased AC resistance.



(a)



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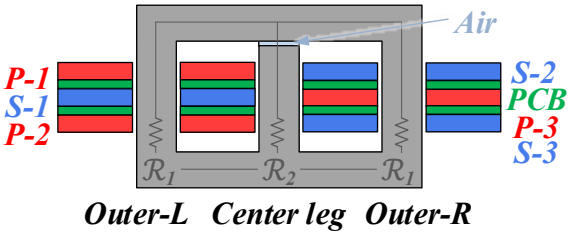


(c)

Fig. 4.6. Integrated transformer implementations from the literature with controllable leakage generated through, (a) air-gap or magnetic shunt material between the primary- and secondary-side windings, (b) relative reluctance of the outer and center legs with primary- and secondary-side windings wound around separate core outer legs (shell transformer), and (c) relative reluctance of the outer and center legs with asymmetrically distributed primary- and secondary-side windings (ACL transformer). Terms n_p and n_s denote an arbitrary number of winding layers used for the primary- and secondary-side windings, where each winding layer is comprised of m_p and m_s number of turns.

In all of the current state-of-the-art, there are limitations associated with subsidiary effects of the leakage inductance integration. Generally these limitations include: complexity in the core structure [49]-[50], [56]-[58], complexity in winding structure [52]-[58], [60]-[61], and high AC resistances due to winding structure [52]-[59]. As such the principal contribution of this chapter is to develop a transformer core plus winding structure that, 1) is capable of realizing controllable leakage inductance,

2) utilizes a simple core structure and winding layout that can be realized on a low-cost four-layer PCB, 3) achieves at least partial winding interleaving for low DC-to-AC resistance ratio, and 4) has low winding overlap area such that the parasitic capacitances do not degrade circuit performance. Furthermore, the second key contribution of the chapter is to develop a transformer geometry optimization procedure, which will be used to design the proposed transformer in proposed microinverter application, and enable design comparison to other transformer structures from the literature.

4.3. Electrical modeling of proposed transformer

A cross-section view of the proposed transformer design is shown in Fig. 4.7, including the core, the core's equivalent reluctance model, and the transformer windings [46]. The core can be realized through the use of an E-core, plus two I-core segments separated by an air gap. In light of the construction, the proposed implementation is henceforth referred to as the “EII” transformer. As can be observed, the terminal windings are wound around the left leg and the center leg, achieving partial interleaving in the left core window. The mutual flux path is completed between the outer left leg and the center leg, while the leakage flux path is completely between the winding legs and the outer right leg. Due to the fact that the leakage flux path is completed through the outer right leg, there is freedom to place an air gap anywhere along the core leg. As such, the air gap is shown to be placed along the top-section of the core (deemed a horizontal air-gap) to reduce the magnitude of the perpendicular component of the H-field at the winding, and improve the H-field symmetry along the cross-section of the windings [62]. As a result, the winding DC-to-AC resistance ratio

is reduced as compared to placement of the air gap along the vertical section of the core.

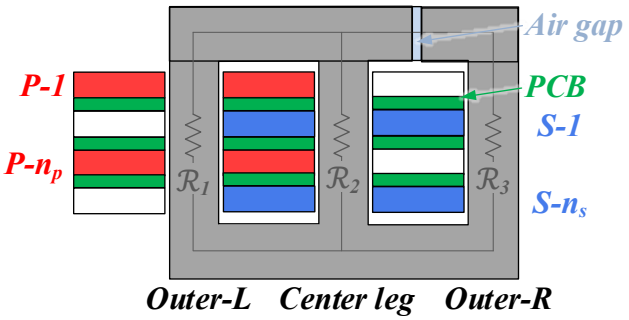


Fig. 4.7. Core and winding diagram of the proposed EII transformer. Within the core is the equivalent reluctance network, realized by a single equivalent reluctance for each core leg. Each winding layer may be comprised of an arbitrary number of turns. White portions in the winding structure indicate the absence of turns on the PCB layer.

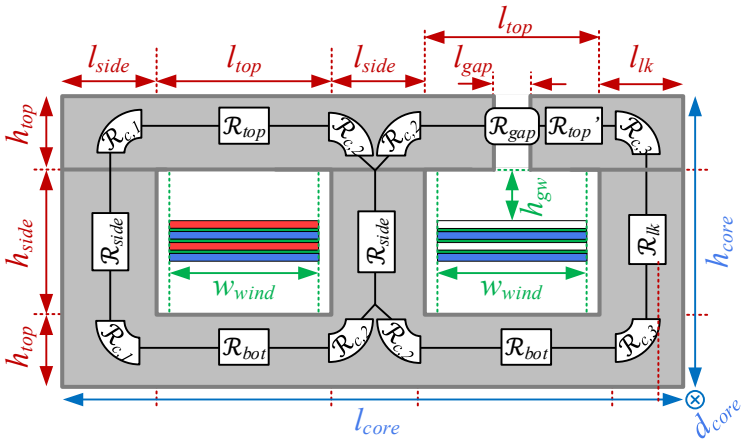
4.3.1. EII reluctance modeling

The detailed reluctance model of the core is presented in Fig. 4.8(a). Due to the fact that the mutual flux path is un-gapped in the proposed implementation (where otherwise the air-gap is a dominant reluctance component compared to the core reluctances), consideration of separate reluctances for the corners and straight core segments is critical, originally motivated and modeled in [63]. The considered lengths and areas of each reluctance segment is shown in Table 4.2, and the reluctances can be calculated via,

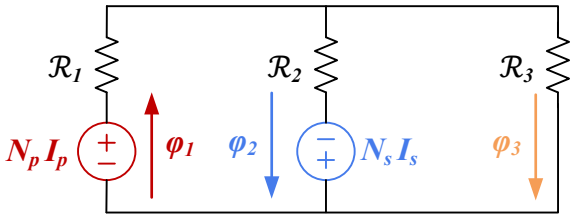
$$\mathcal{R}_x = l_x/\mu_{r,x}\mu_0 A_x \tag{4.14}$$

where l_x is the length of the reluctance segment, A_x is the effective cross-section area of the reluctance segment, and $\mu_{r,x}$ is the relative permeability of the core segment. The air-gap reluctance is important to model as accurately as possible, as it is the largest reluctance component in the network. Consideration of 3-D fringing effects can easily

be calculated via the formulation derived in [63], where in this case a type-I air-gap is utilized.



(a)



(b)

Fig. 4.8. Proposed transformer (a) detailed core reluctance modeling, and (b) equivalent reluctance network modeling. In (a), inner core dimensions are labeled in red, while the external core dimensions are labeled in blue. Additional dimensions related to the winding structure are identified in green. The primary-side windings extending outside of the core footprint on the left have not been shown.

Table 4.2. Lengths and areas for each reluctance in Fig. 4.8(a).

Reluctance (x)	Length	Area
Side (side)	h_{side}	$l_{side}d_{core}$
Corner 1 (c1)	$\pi(h_{top}+l_{side})/8$	$d_{core}(h_{top}+l_{side})/2$
Top | Bot (top | bot)	l_{top}	$h_{top}d_{core}$
Corner 1 (c2)	$\pi(h_{top}+l_{side}/2)/8$	$d_{core}(h_{top}+l_{side}/2)/2$
Top' (top')	$l_{top}-l_{gap}$	$h_{top}d_{core}$
Gap (gap)	l_{gap}	$h_{top}d_{core}$
Leak (lk)	h_{side}	$l_{lk}d_{core}$
Corner 3 (c3)	$\pi(h_{top}+l_{lk})/8$	$d_{core}(h_{top}+l_{lk})/2$

Conversion of the detailed reluctance network in Fig. 4.8(a) to the equivalent network in Fig. 4.8(b) can be facilitated by,

$$\mathcal{R}_1 = \mathcal{R}_{side} + 2\mathcal{R}_{c1} + 2\mathcal{R}_{c2} + \mathcal{R}_{top} + \mathcal{R}_{bot} \tag{4.15}$$

$$\mathcal{R}_2 = \mathcal{R}_{side} \tag{4.16}$$

$$\mathcal{R}_3 = \mathcal{R}_{gap} + \mathcal{R}_{top'} + 2\mathcal{R}_{c2} + 2\mathcal{R}_{c3} + \mathcal{R}_{lk} + \mathcal{R}_{bot} \tag{4.17}$$

From the equivalent circuit, equations for the flux in each of the three core legs can be derived as,

$$\phi_1 = \frac{N_p I_p(\mathcal{R}_2+\mathcal{R}_3) + N_s I_s \mathcal{R}_3}{\mathcal{R}_T} \tag{4.18}$$

$$\phi_2 = \frac{N_p I_p \mathcal{R}_3 + N_s I_s(\mathcal{R}_1+\mathcal{R}_3)}{\mathcal{R}_T} \tag{4.19}$$

$$\phi_3 = \frac{N_p I_p \mathcal{R}_2 - N_s I_s \mathcal{R}_1}{\mathcal{R}_T} \tag{4.20}$$

where $\mathcal{R}_T = \mathcal{R}_1\mathcal{R}_2 + \mathcal{R}_1\mathcal{R}_3 + \mathcal{R}_2\mathcal{R}_3$, $N_p = n_p m_p$ and $N_s = n_s m_s$ are the total number of primary- and secondary-side turns (n_p and n_s are the number of winding

layers on the primary- and secondary-sides, m_p and m_s are the number of primary- and secondary-side turns on each winding layer), and I_p and I_s are the terminal currents of the primary- and secondary-side. Using the flux expressions in each of the three core legs, the self- and mutual-inductances of each coil can be derived as,

$$L_{s,p} = \frac{N_p \phi_1|_{I_s=0}}{I_p} = \frac{N_p^2(\mathcal{R}_2 + \mathcal{R}_3)}{\mathcal{R}_T} \tag{4.21}$$

$$L_{s,s} = \frac{N_s \phi_2|_{I_p=0}}{I_s} = \frac{N_s^2(\mathcal{R}_1 + \mathcal{R}_3)}{\mathcal{R}_T} \tag{4.22}$$

$$M = \frac{N_s \phi_2|_{I_s=0}}{I_s} = \frac{N_p N_s \mathcal{R}_3}{\mathcal{R}_T} \tag{4.23}$$

Based on these equations, the magnetizing and leakage inductance in the transformer T-model of Fig. 4.5 can be determined through subtraction of the self and mutual terms and reflection by the transformer turns ratio [48],

$$L_{lk,p} = L_{s,p} - M/n = \frac{N_p^2 \mathcal{R}_2}{\mathcal{R}_T} \tag{4.24}$$

$$L_{lk,s} = L_{s,s} - M/n = \frac{N_s^2 \mathcal{R}_1}{\mathcal{R}_T} \tag{4.25}$$

$$L_m^{\gamma} = M \cdot T(\gamma) = \frac{N_p N_s \mathcal{R}_3}{\mathcal{R}_T} T(\gamma) \tag{4.26}$$

where $\gamma = \{p, s\}$ defines the side of the T-model that the magnetizing inductance is referred to, $T(\gamma) = \{1/n, n\}$ is the corresponding turns ratio reflection function, and $n = N_s / N_p$ is the transformer turns ratio. It is clear from (4.24)-(4.26) that control of the magnetizing inductance, and both leakage inductances, can be achieved through manipulation of the number of turns and the three equivalent reluctances $\{\mathcal{R}_1, \mathcal{R}_2, \mathcal{R}_3\}$.

In light of (4.24)-(4.26), it should be noted that the designer has near-independent control of both leakage inductance in the T-model. One desirable configuration is the case shown in Fig. 4.8, where an air-gap is only placed on the leakage leg of the core. In this case, $\mathcal{R}_3 > \mathcal{R}_1 > \mathcal{R}_2$, where each inequality is assumed to present at least an order of magnitude between terms (i.e. $\mathcal{R}_3 > 10\mathcal{R}_1$). In many cases where a large magnetizing to leakage ratio is preferred, the factor by which $\mathcal{R}_3$ is greater than $\mathcal{R}_1$ could be even larger. Therefore, (4.24)-(4.26) mathematically infer that the leakage inductance would be almost completely realized by the secondary-side (hereby deemed the EII Sec. configuration), as the leakage inductance on the primary-side would be small. Intuitively this is also clear, as the flux generated by the center-leg windings is more inclined to travel through the leakage leg, as compared to flux generated by the outer left leg windings, due to the relative magnitudes of $\mathcal{R}_1$ and $\mathcal{R}_2$. Naturally, other realizations are also possible where the leakage inductance could be nearly completely realized by the primary-side (e.g. exchanging the location of the primary and secondary-side windings in Fig. 4.7, henceforth referred to as the EII Pri.), or where the leakage distribution is closer to equal (e.g. by manipulating the core geometry through introducing air-gaps on the left- and center-leg such that $\mathcal{R}_2/\mathcal{R}_T \approx \mathcal{R}_1/\mathcal{R}_T$), though the latter configuration may result in reduced achievable L_m.

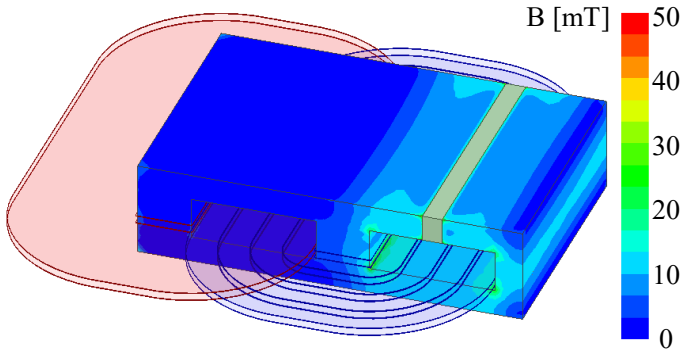
4.3.2. Comparison to simulation

To validate the proposed reluctance modeling, a comparison between the predicted and simulated (via 3D FEA simulations in Ansys Maxwell) magnetizing and leakage inductances for an example EII transformer is evaluated. For simplicity, the

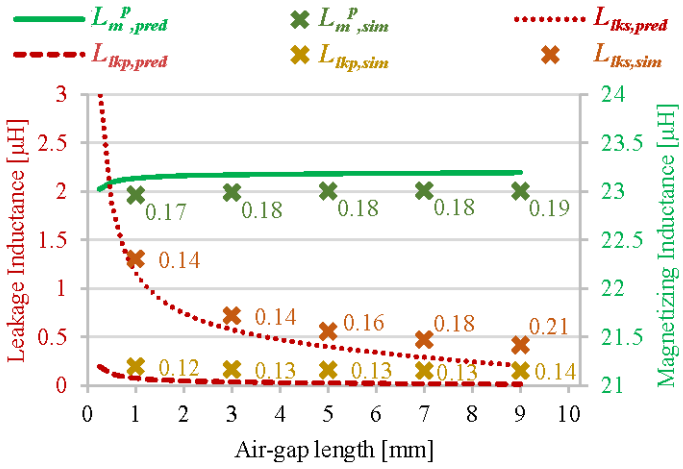
conventional E58 core geometry [73] was considered, where the core's center leg width and outer right leg width were exchanged (i.e. l_{side} = 8.1 mm, and l_{lk} = 4.2 mm). This particular manipulation is preferred as the center and outer left legs generally carry more flux than the outer right leg, and hence larger cross-section areas along this path are beneficial for core loss reduction. An example core and winding structure is shown in Fig. 4.9(a), with the flux density overlaid within the core. In the presented simulation, the sinusoidal current relationship is $I_p(t) = nI_s(t)$, where the resulting flux in the core will isolate the leakage mechanism, as the magnetizing current is zero (cf. Fig. 4.5). It is clear that there is larger flux density in the outer right and center legs as a result of the dual role that the center leg realizes (i.e. the mutual flux path between primary and secondary, and the leakage flux path between the outer right leg and center leg). While the proposed simulation is beneficial for visualization of leakage generation within the transformer, practically magnetizing current will always exist, which is critical to consider in loss analyses.

The magnetizing and leakage inductances are compared as a function of the air-gap width in Fig. 4.9(b), with the absolute value of difference between the simulation and predictions plotted as a data label. From a qualitative perspective, the relationships between the magnetizing inductance and the air gap length are directly proportional, while the relationship between the dominant leakage inductance and the air gap length are inversely proportional, expected from (4.24)-(4.26). Furthermore, the secondary-side leakage inductance is dominant compared to the primary-side leakage inductance, expected due to the fact that $\mathcal{R}_1 > \mathcal{R}_2$. From a quantitative perspective, it is clear that the predicted and simulated values of magnetizing inductance agree very closely. On

the other hand, there is some small error in both the primary- and secondary-side leakage inductance, with a near-uniform deviation of around 0.17 μH.



(a)



(b)

Fig. 4.9. 3D FEA simulations in Ansys Maxwell, (a) example core and winding configuration with overlaid core flux density in [mT], and (b) comparison of magnetizing and leakage inductance with predictions based on reluctance modeling. In (a), sinusoidal current excitations are applied with I_p = 4 A_{rms}, and I_s = 1 A_{rms}. In (b), the absolute value of inductance difference between the predictions and simulations are listed as labels for the simulation scatter-plots.

4.4. Transformer loss modeling

The proposed application of the EII transformer is a single-stage, single-phase, PV microinverter, based on the DAB topology shown in Fig. 4.10 [64]. The nominal specifications of the considered system are shown in Table 4.3. In the considered

topology, the leakage inductances act as the power transfer element between the primary- and secondary-side, while the magnetizing inductance can help to support zero-voltage-switching (ZVS) of the devices [68]. The considered control principle is phase-shift-based modulation, described in detail in Chapter 2, where in each switching period a quasi-square-wave voltage source can be applied on the primary-side and a square-wave voltage source can be applied on the secondary-side with a controllable phase shift; the transformer currents are hence decided according to the solution of the circuit in Fig. 4.5. Detailed analytical modeling in the frequency-domain regarding this control principle is well established, of which recent modeling efforts have been developed in [64] and [77].

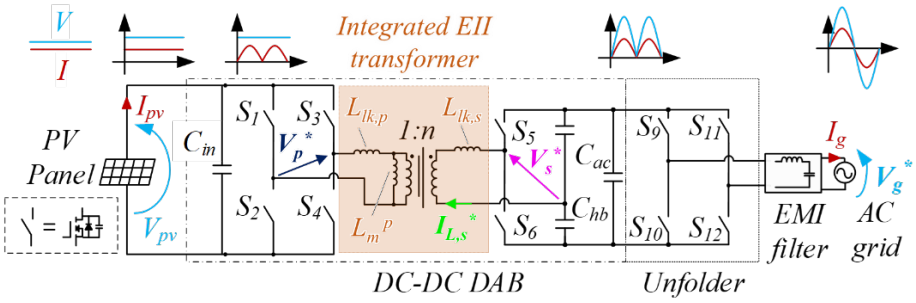


Fig. 4.10. Circuit schematic of the single-stage DC-AC microinverter based on the DAB circuit topology. The highlighted integrated EII transformer's leakage inductances are utilized for power transfer between the primary- and secondary-side. Waveforms probed in the experimental measurement section of this chapter are bolded and marked with an asterisk.

Table 4.3. Nominal operating conditions of the microinverter.

$V_{in,mpp}$ [V]	$P_{in,mpp}$ [W]	$V_{ac,rms}$ [V]	f_{grid} [Hz]	f_{sw} [kHz]
40	400	240	60	200

4.4.1. General conduction loss modeling

The conduction loss in the transformer can be calculated using the detailed formula,

$$P_{cond} = \frac{1}{2}\sum_{k=1,odd}^{k_{max}} \begin{bmatrix} \overrightarrow{I_{p,k}} & \overrightarrow{I_{s,k}} \end{bmatrix} \begin{bmatrix} R_p & R_m \\ R_m & R_s \end{bmatrix}_k \begin{bmatrix} \overrightarrow{I^*_{p,k}} \\ \overrightarrow{I^*_{s,k}} \end{bmatrix} \tag{4.27}$$

where $\overrightarrow{I_{p/s,k}}$ is the vector component of the primary- and secondary-side currents at the k^{th} harmonic, R_p is the primary-side self-resistance, R_m is the winding mutual resistance, and R_s is the secondary-side self-resistance [69]. However, while (4.27) is the most accurate conduction loss expression, especially in dual-active-bridge converters where the transformer primary- and secondary-side currents are composed of multiple harmonic components, the analysis requires characterization of the resistance matrix of a transformer design across multiple harmonics of the switching frequency. The winding AC resistances as a function of frequency are difficult to derive analytically, which are generally due to both skin and proximity effects, conventionally calculated via Dowell's formula [70]-[71]. However, the proposed winding structure consists of both interleaved winding sections (where the AC resistance could be calculated more accurately), and non-interleaved winding sections (which do not obey Dowell's assumptions due to MMF variation in both the horizontal and vertical directions) [65]. As such, determination of the resistance matrix of a given design can only be reliably determined through the use of 3D FEA simulations [72]. Nevertheless, coordination between the optimization routine and 3D FEA simulations for each considered design would significantly increase the computational complexity of the analysis, and hence simplifications to (4.27) were pursued.

4.4.2. Conduction loss simplifications

In light of the complexity issues regarding the use of (4.27), two approximations are proposed for computational simplification. First, the conduction loss at the k^{th} harmonic is expanded into,

$$P_{c,k} = I_{p,k}^2 R_{p,k} + I_{s,k}^2 R_{s,k} + 2 I_{p,k} I_{s,k} R_{m,k} \cos(\Delta\beta_k) \tag{4.28}$$

$$P_{cond} = \frac{1}{2} \sum_{k=1,odd}^{k_{max}} P_{c,k} \tag{4.29}$$

where $I_{p/s,k}$ is the magnitude of the primary- and secondary-side current at the k^{th} harmonic, and $\Delta\beta_k$ is the phase angle difference between the currents. While the phase angle difference is easily known through circuit modeling, the derivation of the mutual resistance analytically is difficult. As such, the proposed approximation sets $2\cos(\Delta\beta_k) \approx 2$, effectively establishing that the phase angle difference between the primary- and secondary-side currents is small enough to be ignored. The angular approximation is validated in Fig. 4.11(a) across the quarter-line-cycle at each CEC power level. It is clear that as the magnetizing inductance increases, the effect of the magnetizing current in perturbing the phase angle between the primary- and secondary-side is minimal. It is further evident that even for low magnetizing inductance of 10 μH, the approximation will only generate sufficient error in the low operating power levels. In these cases, specifically for negative R_m values, the predicted conduction losses will be slightly under-estimated.

The second approximation is proposed to promote a further simplification of the conduction loss calculation in (4.27). The calculation process is first given by,

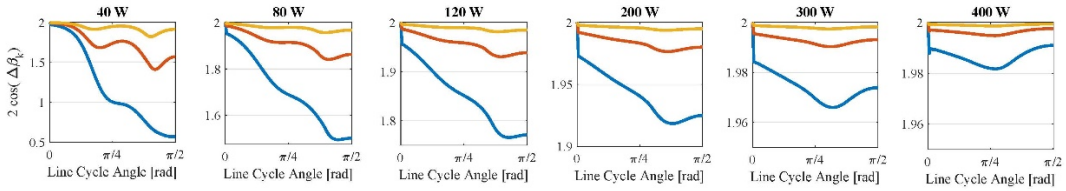
$$P_{c,k} \approx I_{p,r,k}^2 R_{p,k} + I_{s,r,k}^2 R_{s,k} + 2I_{p,r,k} I_{s,r,k} R_{m,k} \tag{4.30}$$

$$P_{cond} = \sum_{k=1,odd}^{k_{max}} P_{c,k} \tag{4.31}$$

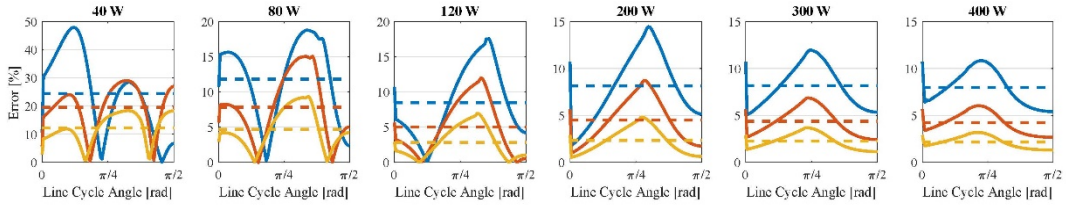
where the current magnitudes are replaced by the respective RMS value, through distribution of the factor of ½ in (4.29). Under the approximation that $I_{p,r,k} \approx nI_{s,r,k}$, this expression can be rewritten as,

$$P_{c,k} = I_{p,r,k}^2 (R_{p,k} + R_{m,k}/n) + I_{s,r,k}^2 (R_{s,k} + nR_{m,k}) \tag{4.32}$$

where the $2I_{p,r,k} I_{s,r,k} R_{m,k}$ expression is split and summed separately into the first two terms. Whereas the first approximation discussed the phase angle between the two currents, the second approximation targets equal relative magnitudes of the two currents. An analytical analysis of the magnitude approximation is formulated in Fig. 4.11(b), where the error incurred by the approximation is analyzed across a quarter-line-cycle for each CEC power level. For each power level, the error of the assumption is calculated at each DC-DC operating point as well as across the line cycle. It is clear that for even $L_m{}^p$ = 10 μH, errors in line-cycle RMS current are mostly below 10% despite certain DC-DC operating points having larger errors.



(a)



(b)

Fig. 4.11. Validation of approximation (a) $2\cos(\Delta\beta_k) \approx 2$, and (b) $\$I_{p,r,1} \approx nI_{s,r,1}$, for conduction loss calculation simplifications. In each case, the series of plots show the approximations across each CEC power level for an example 400 W microinverter, with $L_{lk,p} = 1.2\ \mu$H and varying values of $L_m{}^p$. The blue, red, and yellow traces correspond to an $L_m{}^p$ value of 10 μH, 20 μH, and 40 μH, respectively. In (b), the solid lines show local DC-DC operating point approximation error across the DC-AC line-cycle, whereas the dotted lines indicate the error in total line-cycle RMS.

In general, both of the proposed approximations benefit in accuracy for larger ratios of magnetizing to leakage inductance, which is desirable in the proposed transformer design as the magnetizing flux path is ungapped. Specifically, large magnetizing inductances yield low magnetizing currents and hence generally lower core losses (of which the modeling is formulated in the following section). Furthermore, the approximation errors are largest in the lower power levels, which are not as critical as the higher power levels (this will be clearer in Section 4.5.3, during the discussion of the CEC efficiency calculation). The two proposed approximations enable final restructuring of the conduction loss calculation into,

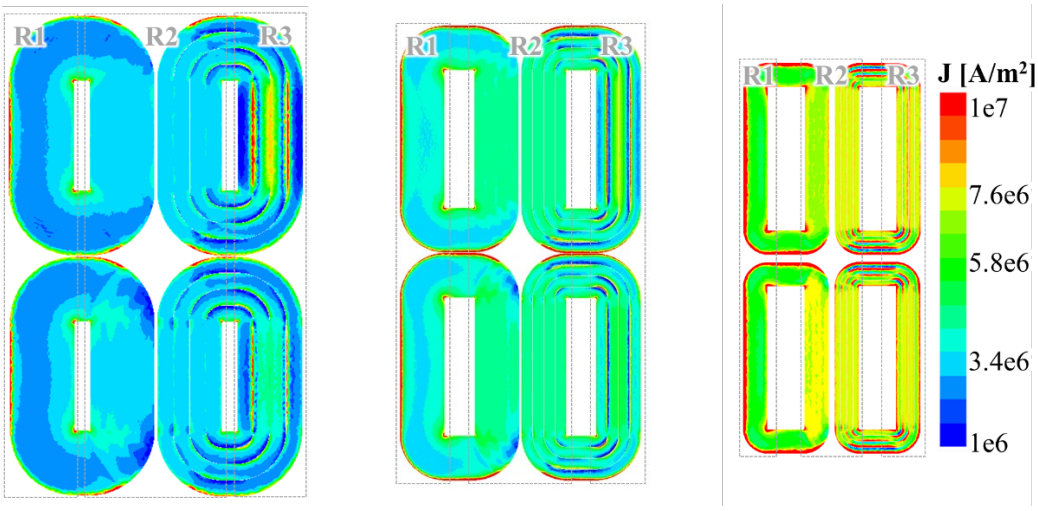
$$P_{cond} = \sum_{k=1,odd}^{5} I_{p,r,k}^2 \left(F_{r,p,k} R_{dc,p} + \frac{F_{r,s,k} R_{dc,s}}{n^2} \right) \tag{4.33}$$

where the first three odd harmonics are used for conduction loss calculation, $F_{r,p/s,k}$ is an equivalent primary- and secondary-side DC-to-AC resistance ratio at the k^{th} harmonic including contributions of both the self and mutual resistances, and $R_{dc,p/s}$ are the primary- and secondary-side DC resistances. This form, facilitated by the balanced current approximations, is also shown under similar conditions in [69]. The formulation is beneficial for analytical procedures, as trends can be derived through detailed FEA simulation for the DC-to-AC resistance ratios, which are multiplied by simply formulated DC resistances. While the proposed balanced current approximations have been shown to be sufficiently accurate in the conditions surrounding the proposed application, they certainly are not uniformly applicable, especially in designs with reduced ratios of magnetizing to leakage inductance.

4.4.3. Conduction loss design considerations

It is important to identify specific design trends associated with the formulation of the DC-to-AC resistance ratios, $F_{r,p}$ and $F_{r,s}$. Three unique transformer designs are analyzed in this sub-section with design parameters listed in Appendix Section G. In each case, the excitation frequency was fixed at 200 kHz, and the excitation amplitudes were 4 A_{rms} for the primary and 1 A_{rms} for the secondary. For each design, Fig. 4.12 demonstrates to-scale 3D FEA winding current distributions of the three designs, each with 5 mm for the distance between the leakage-leg air-gap and the windings beneath, deemed h_{gw} [cf. Fig. 4.8(a)]. The current distribution pattern in each case is consistent for each of the three indicated regions in Fig. 4.12, namely region 1 (R1) for the

windings outside of the core footprint, region 2 (R2) for the interleaved winding portion, and region 3 (R3) for the winding portion beneath the leakage leg air-gap. First, region 1 indicates current concentration towards the edges of the windings. Next, region 2 exhibits very balanced current distribution, as this region has strong winding interleaving. Finally, region 3 exhibits current concentration in the winding portion beneath the air-gap, due to the H-field pattern that emanates from the air-gap, as indicated in [74] and [75].



(a) (b) (c)

Fig. 4.12. Current density distributions to-scale for three designs under analysis, (a) transformer A, (b) transformer B, and (c) transformer C. Each of three unique regions (R1, R2, and R3) are highlighted for the three designs, where the current density has unique distribution patterns. The images in relationship to the winding stack-up Fig. 4.7 are P-1 on the top-left, P-2 on the bottom-left, S-1 on the top-right, and S-2 on the bottom-right.

Two key design insights regarding region 3 are important to investigate further, which also lead to determination of resistance trends in the other winding regions. First, while region 1 and region 2 realize similar current distribution patterns on each winding layer, the current distribution in region 3 is more uniformly distributed for the winding further from the gap than the winding closer to gap. This insight was also made in [62]

for an inductor winding design. As such, it is inferred that the distance between the gap and windings, h_{gw} is an important parameter to be designed properly. In light of this, trends of h_{gw} versus $F_{r,p/s}$ are developed and plotted in Fig. 4.13. It is clear that for each transformer design, the secondary-side $F_{r,s}$ is a strong function of this gap distance up to a certain point, whereas the $F_{r,p}$ is relatively flat. A general rule of thumb that can be applied, which was originally proposed for inductor windings beneath an air-gap in [75], is that the ratio of w_{wind} to h_{gw} (hereby deemed the Sullivan ratio, r_S) should be less than or equal to four. In the case of the proposed transformer, of which only a single set of windings is below the gap, this rule of thumb is also quite accurate, which would lead to h_{gw} selections of ~6 mm, ~4 mm, and ~2 mm for designs A, B, and C, respectively. Nevertheless, to ensure a closer-to-minimum $F_{r,s}$, the maximum bound of the Sullivan ratio is chosen to be three.

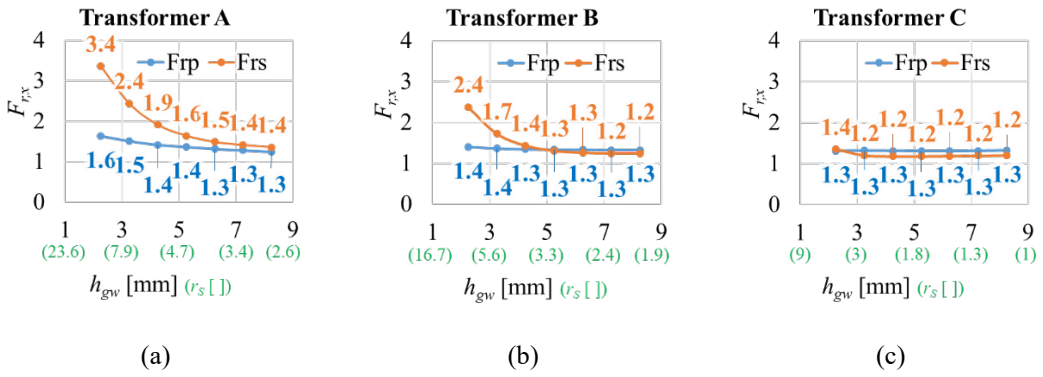


Fig. 4.13. Parametric analysis of the primary- and secondary-side DC-to-AC resistance ratios as a function of the air gap-to-winding distance (and Sullivan ratio in parenthesis) for, (a) transformer A, (b) transformer B, and (c) transformer C.

The second key insight is that the width of the crowding region is related to the width of the air-gap, implying that the ratio of the gap length to the winding width, $r_{gw} = l_{gap}/w_{wind}$ is an important design parameter. It should be noted that for a given transformer design, neither l_{gap} nor w_{wind} are free variables, and hence r_{gw} only serves

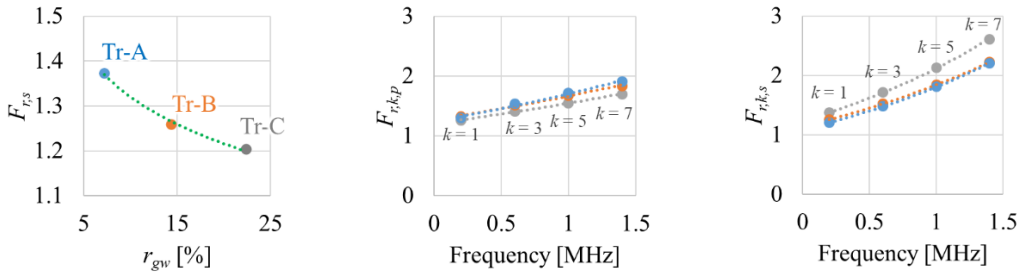
to preferentiate one design over another. The values of the secondary-side DC-to-AC resistance ratios are shown as a function of r_{gw} in Fig. 4.14(a). It is clear that the value of $F_{r,s}$ varies quite significantly as a function of r_{gw}, and fits to a logarithmic trend (with an $R^2 = 0.9952$) of which the relationship is henceforth used. Specifically a logarithmic fit was considered due to the logarithmic spread of the perpendicular H-field component fringing from the gap to the windings [74].

Maintaining a Sullivan ratio of three, analysis of the DC-to-AC resistance ratios were further evaluated as a function of switching frequency harmonic. The results are presented for the primary-side DC-to-AC resistance ratio in Fig. 4.14(b), where the value varies exponentially in each case, increasing by roughly a factor of 10% for successive harmonic levels. Furthermore, the results for the secondary-side DC-to-AC resistance ratio are highlighted in Fig. 4.14(c), where again exponential trends are identified with increases of roughly a factor of 20% for successive harmonic levels. Therefore, the following resistance trends are utilized in the following multi-objective optimization,

$$F_{r,p,k} = 1.3 \cdot e^{0.055(k-1)} \tag{4.34}$$

$$F_{r,s,k} = \left(1.67 - 0.15 \ln\left(r_{gw}\right)\right) \cdot e^{0.1(k-1)} \tag{4.35}$$

where the primary-side DC-to-AC resistance ratio of all designs is equal, whereas the secondary-side DC-to-AC resistance ratio is a function of the r_{gw} parameter.



(a) (b) (c)

Fig. 4.14. Parametric analysis of the primary- and secondary-side DC-to-AC resistance ratios as a function of (a) the gap to winding width ratio for the secondary-side, (b) the frequency for the primary-side, and (c) the frequency for the secondary-side. Logarithmic trends are identified for the air-gap width to winding width ratio on the secondary-side, while exponential trends are identified for the resistance ratios as a function of frequency. Design details for Transformer A are shown in blue, Transformer B in orange, and Transformer C in gray.

4.4.4. Core loss modeling

The proposed transformer structure exhibits non-uniform flux density due to the consideration of unique cross-section areas throughout the core, and the fact that the flux in the three legs is non-equal. As such, a unique core-loss calculation procedure is developed, similar to that proposed in [60], broken down into three key steps. First, the equivalent circuit for a given switching period is analyzed based on the superposed harmonic analysis developed in [64], from which the time-domain currents on the primary- and secondary-side can be reconstructed. After reconstructing the time-domain equivalent currents, the flux in each of the transformer legs can be found as a function of excitation current from the transformer's reluctance model, with (4.18)-(4.20). Finally, the core loss can be calculated in each of the core's reluctance sections independently and summed using an adaptation of the iGSE [66],

$$P_{core} = \frac{k_i}{T_{sw}} \left[\sum_{j=1}^{s} \left(\Delta B_{pp,j}^{\beta-\alpha} \sum_{i=1}^{d} \Delta t_i^{1-\alpha} \Delta B_{j,i}^{\alpha} V_j \right) \right] \tag{4.36}$$

$$\Delta B_{j,i} = \frac{\Delta \phi_{j.i}}{A_j} \tag{4.37}$$

where j corresponds to the core reluctance section (arbitrarily numbered from 1 to s); s corresponds to the maximum number of core sections considered; $\{k_i, \alpha, \beta\}$ are the Steinmetz parameters [66]; d is the number of unique time-steps that the switching period is discretized; $\Delta B_{j,i}$ is the change in flux density in the discrete time step Δt_i; $\Delta B_{pp,j}$ is the peak-to-peak flux density of core section j across the switching period; and $\{A_j, V_j\}$ are the cross-section area and volume of the core section (cf. Table 4.2). In the considered primary-side full-bridge / secondary-side half-bridge topology there are at most six unique piece-wise linear portions of the transformer current, and hence the maximum value of $d = 6$ [64].

The core loss modeling approach is validated using the Ansys Maxwell Magnetic Transient simulation, which allows arbitrary current excitation waveforms (determined from time-domain simulations of specific operating points) to be applied to the transformer windings. The simulation is then solved over several switching periods, where the average core loss can be extracted. An illustration of the core loss calculation process is highlighted in the top inset of Fig. 4.15. The transformer utilized for the analysis is that from Section 4.3.2, with an air-gap length of 3 mm. The predicted core loss across the AC line cycle is compared to simulation at four example operating points for the 200 W average power level. The comparative results are shown in the bottom half of Fig. 4.15, where the simulation and model agree within 100 mW of error in each case.

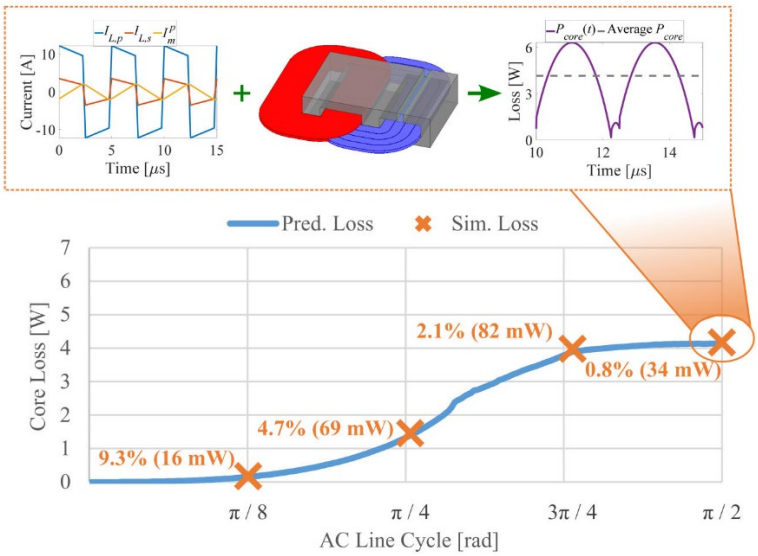


Fig. 4.15. Core loss simulation versus prediction at the 200 W average power level, with prediction error at the simulated points shown as a data label. The top inset highlights an example Ansys Maxwell Magnetic Transient simulation with user-defined current excitations applied to the core and winding geometry, which is solved over time to extract time-varying and switching period averaged core loss.

4.5. Multi-objective optimization of core geometry

The proposed transformer is evaluated in a constrained multi-objective optimization procedure of the core geometry, to select a design with the lowest transformer efficiency drop while satisfying power-throughput and size constraints, as explained in the following sections.

4.5.1. Parametric constraints

As detailed in Chapter 3, a target amount of leakage inductance is desired based on the maximum power transfer capability in the DC-AC DAB as well as limiting the conduction loss factor (CLF), which is a figure of merit denoting CEC-related conduction losses in the microinverter circuit. Generally, this constraint can be evaluated by checking,

$$C(1) = \{L_{lk,s}(l_{gap}) = L_{lk,des}\ for\ l_{gap} \in [0, l_{top}]\} \quad (4.38)$$

In other words, (4.38) evaluates whether or not the target leakage inductance can be generated by varying the air-gap length between zero and l_{top} [cf. Fig. 4.8(a)].

4.5.2. Geometric constraints

Additional design constraints are posed regarding the footprint of the transformer, with the goal of optimizing power density assuming the rest of the PCB is pre-designed. The geometric constraints are pictorially shown in Fig. 4.16, where the PCB length should not be violated, and the transformer depth ensures that the power density requirement is met. Mathematically, the geometric constraints are posed as,

$$C(2) = d_{core} + 2w_{wind} - D_{tr,max} \quad (4.39)$$

$$C(3) = l_{core} + w_{wind} - L_{tr,max} \quad (4.40)$$

where d_{core}, l_{core}, and w_{wind} are defined in Fig. 4.8(a), $D_{tr,max}$ and $L_{tr,max}$ are defined in Fig. 4.16, and the constraints are satisfied if the expression is less than or equal to zero. Dimensions of the PCB in Fig. 4.16 are highlighted in Table 4.4, alongside other relevant specifications used to determine the maximum allowable transformer dimensions. A 5 mm increase in PCB length and depth was considered, as well as a 1 mm increase in PCB height on the top and bottom, due to realistic implications of the microinverter packaging solution in the power density calculations. In the first iteration of the design optimization in Section 4.5.5, the outer core geometry is considered to be fixed to that of the E58 core from Ferroxcube [73]. Section 4.5.6 then highlights extension of the design analysis to a fully custom core geometry.

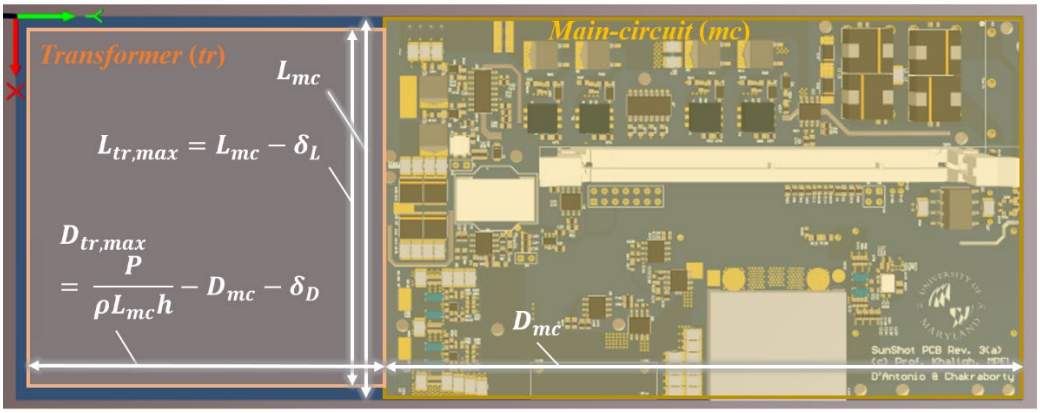


Fig. 4.16. Illustration of the transformer dimensional constraints in light of the main-circuit layout. Assuming the rest of the power circuit PCB has been pre-designed, the transformer length should not exceed the PCB length, while the maximum depth is decided according to the power density target and PCB height. Terms δ_D and δ_L denote additional margins on the allowable dimension.

Table 4.4. Specifications used for transformer footprint constraints.

L_{mc} (δ_L) [mm]	D_{mc} (δ_D) [mm]	h (top / bot) [mm]	ρ [W/cm^3]	$L_{tr,max}$ [mm]	$D_{tr,max}$ [mm]
90 (4)	150 (4)	25 (6 / 19)	0.6	87	83

In addition to constraints regarding the length and depth of the transformer footprint, additional constraints should be posed regarding the distance between the leakage leg air-gap and the windings below, in line with the discussion from Section 4.4.3. In particular, the ratio of winding width to the gap-to-winding distance should be less than or equal to three. This constraint can be posed mathematically as,

$$C(4) = \frac{w_{wind}}{h_{gw}} - 3 \tag{4.41}$$

where w_{wind}, and h_{gw} are defined in Fig. 4.8(a), and the constraint is again satisfied if the expression is less than or equal to zero.

4.5.3. Objective functions

As described in Appendix Section A, the converter CEC efficiency can be decomposed to identify CEC percentage drops due specifically to the transformer,

$$\eta_{CEC} = \sum_{i=1}^{6} C_i \left[1 - \frac{\left(L_{core,t,i} + L_{cond,t,i} + L_{o,i}\right)}{P_i}\right] \tag{4.42}$$

where $L_{core,t,i}$ and $L_{cond,t,i}$ denotes the transformer's line-cycle-averaged core and conduction losses respectively, and $L_{o,i}$ represents the other losses in the system (i.e. device conduction, switching, etc.), at each average power level P_i. The ideal modulation-level optimization (MLO) developed in Chapter 3 is used to determine circuit behavior at "N" number of DC-DC operating points across the symmetric DC-AC quarter-line cycle. In the utilization of the MLO, the time-domain transformer currents are hence known at every operating point for each CEC power level. As such, the core and conduction losses can be calculated at each DC-DC operating point according to the procedure described in Section 4.4, and averaged across each CEC power level via,

$$L_{core,i} = \frac{1}{N}\sum_{1}^{N} P_{core}\left(I_p(t), I_s(t), \phi_1, \phi_2, \phi_3, A, V\right) \tag{4.43}$$

$$L_{cond,i} = \frac{1}{N}\sum_{1}^{N} P_{cond}\left(I_p(t), I_s(t), \vec{x}\right) \tag{4.44}$$

where $I_p(t)$ and $I_s(t)$ are the time-domain expressions for the transformer terminal currents at each DC-DC operating point; φ_1- φ_3 are expressions of the flux in each core leg [i.e. (4.18)-(4.20)]; and $\{A, V\}$ are the areas of volumes of each core component from the detailed reluctance modeling [cf. Fig. 4.8(a)]. With the loss expressions derived at each CEC power level, the optimization objective functions are defined as,

$$PCF = Y(1) = \sum_{i=1}^{6} \frac{C_i}{P_i} L_{core,t,i} \tag{4.45}$$

$$WLF = Y(2) = \sum_{i=1}^{6} \frac{C_i}{P_i} L_{cond,t,i} \tag{4.46}$$

In particular, (4.45) describes the CEC efficiency drop due to core loss and is hence deemed the core loss factor (PCF), while (4.46) defines the CEC efficiency drop due to winding loss and henceforth is referred to as the winding loss factor (WLF). Together, the PCF and WLF add up to define the total CEC loss factor (TLF) of the transformer.

4.5.4. Optimization implementation

A flow-chart of the optimization procedure is shown in Fig. 4.17. In the first step, selection of core material, inductance targets, turns ratio, and dimensional constraints are input to the MATLAB-based program. A genetic algorithm (GA)-based multi-objective optimization procedure, which will be motivated in the following section, is used to navigate the three-dimensional search space consisting of the inner geometry parameters indicated in Fig. 4.17. For each set of design parameters $\overrightarrow{x_{1x3}}$, the constraints from Sections 4.5.1 and 4.5.2, namely (4.38)-(4.41), are evaluated. If the constraints are not met, the genetic algorithm re-iterates the design variables; else, the algorithm proceeds to calculate the objective functions according to the analysis in 4.5.3. The multi-objective optimization procedure thereafter seeks to identify the trade-off between core and conduction losses of the transformer, as they impact the CEC efficiency drop. The algorithm proceeds until the stop conditions associated with MATLAB's in-built multi-objective GA routine "*gamultiobj*" are met, typically limited

either by the number of generations or the relative change in Pareto candidates between generations. In addition to the EII, the shell transformer (with design details in Appendix Section A) and ACL transformers transformer (with design details in Appendix Section F) with $m_p = 1$ and $m_s = 4$ from Fig. 4.6(b) and (c), respectively, were analyzed for optimal geometric configurations.

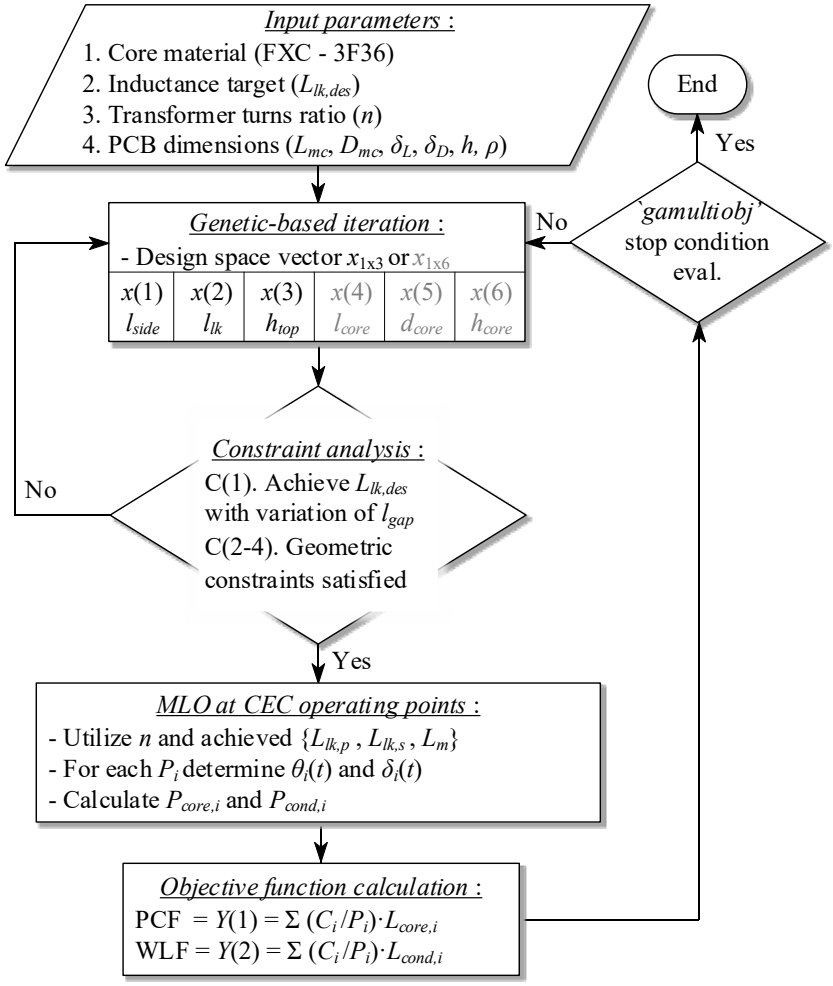


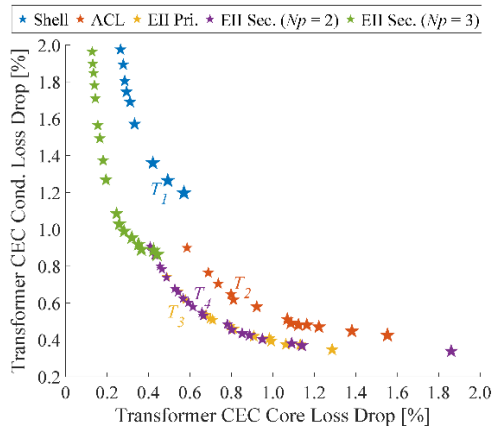
Fig. 4.17. Flow chart for facilitating the multi-objective optimization routine for the proposed EII transformer. Definition of the input vector is indicated in the iteration block in coordination with Fig. 4.8(a).

4.5.5. Results

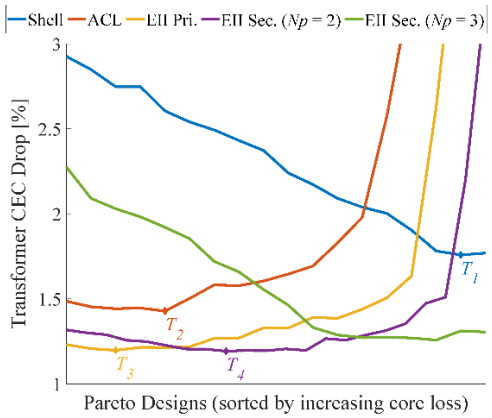
The results of the optimization procedure for the ACL transformer, shell transformer, and three variants of the EII transformer are depicted in the Pareto chart in Fig. 4.18(a). The shell and ACL transformer with less number of primary turns were not considered due to difficulty in achieving the leakage inductance target, or too high core flux density. In general, the trade-off between core and conduction loss is clear from the convexity of the Pareto curves towards the bottom-left corner. The size of each Pareto indicator is proportional to the footprint area of the transformer, where it is clear that the designs with larger footprint tend to have lesser conduction loss at the cost of increased core loss due to the usage of larger winding widths, which overhang from the core in multiple dimensions (cf. Fig. 4.6 and Fig. 4.7) One key takeaway from Fig. 4.18(a) is that the EII transformer designs with $N_p = 2$ perform better than the ACL transformer, specifically as a result of lesser CEC drop due to core loss (near uniform left shift in the Pareto front). On the other hand, the shell transformer suffers from much higher conduction losses than the EII designs with $N_p = 2$ due to the non-interleaving pattern of the windings. The performance of the shell transformer is similar to that of the EII with $N_p = 3$, though the EII still achieves lower core losses and slightly lower conduction losses in certain configurations, as the DC-to-AC resistance ratio in the EII is reduced in comparison to the shell. Finally, in comparison to a low-leakage transformer with a separate inductor in series on the primary-side, the EII transformers outperform from a loss perspective but are realized in a slightly larger total footprint area. The reduced loss in the EII is primarily due to reduced conduction losses, with a

balance of core losses, as the non-integrated transformer with a series inductor requires independent winding sets for each magnetic component.

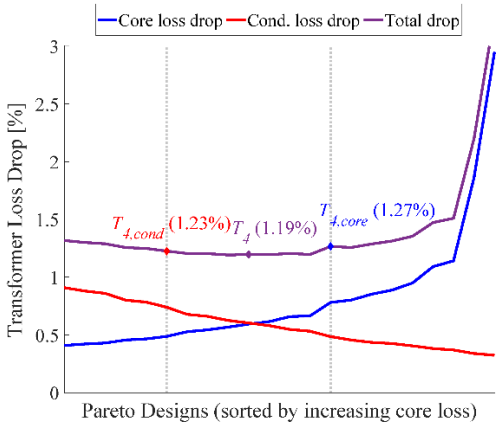
To determine the ideal candidate to pursue experimentally, the total transformer CEC drops for each of the Pareto candidates are shown in Fig. 4.18(b). It is clear in this case that the lowest loss designs for the EII configurations are lower than that in each of the other configurations. Indicated transformer designs T_1-T_4, representing the lowest loss designs for each transformer type, are summarized in Table 4.5. It is concluded that the EII transformer with $N_p = 2$ has the best performance, regardless of whether the leakage is lumped on the primary and secondary sides. As such, the decision of where to lump the leakage inductance can come from secondary considerations, such as zero-voltage-switching (ZVS), and a more comprehensive analysis can certainly explore those effects. However, since the focus of this chapter was to highlight the key advantages of the EII approach, optimal leakage distribution has not been investigated but is an area of future research. Finally, it may be noted that in addition to achieving the lowest loss, the EII transformer also has a lower footprint area than the optimal shell and ACL designs due to the reduced winding overhang outside of the core footprint.



(a)



(b)



(c)

Fig. 4.18. Results of the multi-objective optimization procedure of the considered integrated transformers, (a) Pareto chart, (b) total loss breakdown of Pareto candidates sorted by increasing core losses, and (c) breakdown of the EII Sec. (N_p = 2) Pareto candidates by loss mechanism. The size of the stars in the Pareto chart in (a) are proportional to the footprint area of the design. The indicated design points T_1-T_4 are highlighted in Table 4.5.

Table 4.5. Comparisons of optimal E58 transformer designs.

Tr. Type	$L_m{}^p$ [μH]	$L_{lk,p}$ [μH]	$L_{lk,s}$ [μH]	PCF [%]	WLF [%]	TLF [%]	A_{tr} [cm^2]
Ind. + Tr. T_0	20	1.18	n/a	0.12	1.04	1.16	40.6
Shell [59] T_1	27.7	0.58	0.58	9,48	1.26	1.75	66.1
ACL [60] T_2	39.2	0.6	0.6	0.81	0.62	1.43	48.4
EII Pri. [46] T_3	40.4	1.17	0.05	0.58	0.62	1.2	41.3
EII Sec. [46] T_4	38.6	0.07	1.2	0.59	0.6	1.19	42.2

One additional point of analysis for the EII Sec. transformers with N_p = 2 is highlighted in Fig. 4.18(c), where the total transformer drop of each Pareto candidate is broken down by loss mechanism. It is interesting to note that the total transformer drop is relatively constant within a range of Pareto candidates, around 1.2%. However, this total drop is achieved with differing proportions of core and winding losses. The T_4 selection achieves a more balanced distribution of core and winding losses, though there is freedom to select a design in which the loss is more skewed to the core, denoted $T_{4,core}$ or windings, termed $T_{4,cond}$. This implies that the decision of which design to select can come from other practical design perspectives, predominantly thermal management. In many cases, due to the large area of the core and the fact that the windings are embedded into the PCB, a larger core loss may be preferable for cooling.

4.5.6. Extension to custom core geometry

To facilitate a fully custom core analysis, three additional design parameters (outer core width, length, and height) can be introduced, where the design vector from

Fig. 4.17 is hence 6-dimensional, $\overrightarrow{x_{1x6}}$. Due to the dimensionality of the fully custom problem, and the inner-loop being computationally expensive, use of GA is invaluable; the computation time would be very high considering brute-force (BF) approaches (i.e. an exhaustive decision space search) that scale according to $t_{ex}v^p$, where t_{ex} is the execution time of one iteration, v is the dimension of the decision space vector, and p is the number of discrete possibilities of each design variable.

The results and comparison of the fully custom EII Sec. analysis (Custom-EII Sec.), versus the E58-EII Sec., is highlighted in Fig. 4.19. In this figure, an overlay of the BF analysis for the E58-EII Sec. transformer was performed to compare against the GA-based implementation. It is shown that the GA (total time = 36.27 hrs.) is capable of delivering near-optimal results based on the BF search (total time = 31.8 hrs.), at a similar total execution time. Importantly, the BF decision space contained 25 points for x_1 and x_2, and 5 points for x_3 (cf. Fig. 4.17 for variable identification), while the GA was executed to 100 generations. On the other hand, the fully custom design (total GA run time = 100.8 hrs.) Pareto front is nearly intractable with a BF-based search, where 25 points for the additional three input parameters $\{x_4, x_5, x_6\}$ would create a decision space with over 48 million unique designs. While the genetic algorithm enabled the initial optimization, the results later informed general design principles developed in Appendix Section H, which established simple transformer design considerations with near-optimal results.

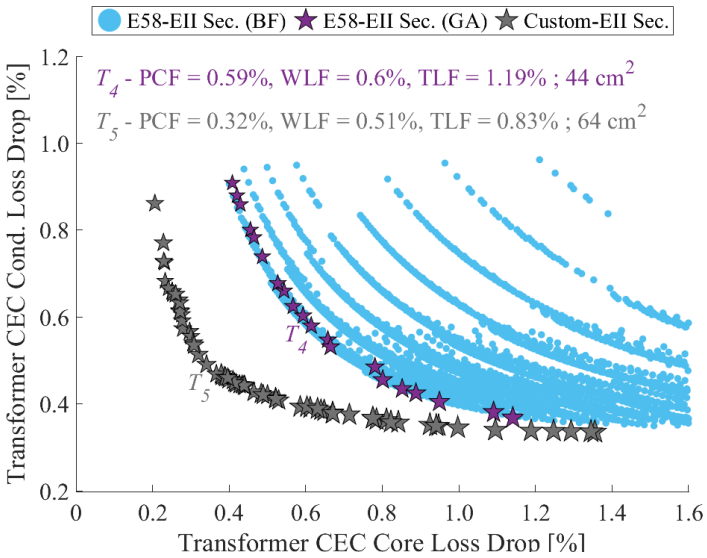


Fig. 4.19. Pareto-front comparison between the E58-EII Sec. and the Custom-EII Sec. Furthermore, utilization of GA is justified, as the BF- and GA-derived Pareto fronts are nearly identical for the E58 core analysis.

Comparing transformers T_4 and T_5 in Fig. 4.19, allowing all of the core dimensions to be variable enables a reduction in efficiency drop by almost 0.4%. However, for the reduction in loss attributed primarily to reduced core loss, the footprint area of the transformer increases by roughly 50%. Nevertheless, the proposed optimization procedure ensures that the circuit power density target is still maintained. The finally selected EII Sec. designs T_4 and T_5 are presented in Table 4.6, alongside predictions from 3D FEA simulation. It is clear that in both cases the predictions of magnetizing and leakage inductance agree well, further validating the transformer characterization from Section 4.3.1. Additionally, the AC resistance predictions in the model are within 5% of the 3D FEA results. Comparing the CLF with the analytically simplified approach in (4.33) versus use of (4.27), where the resistance matrix was extracted from 3D FEA simulations, yielded an absolute difference of 0.01% for T_4 and

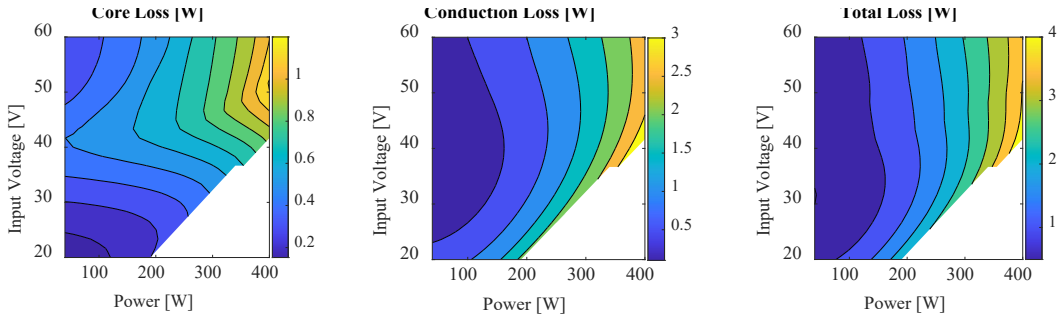
0.008% for T_5, validating the proposed AC resistance modeling and associated simplifications.

Table 4.6. Geometric and electrical specs. of the optimal E58-EII Sec. transformer with $N_p = 2$ (T_4), and the custom-EII Sec. (T_5). Electrical parameters are compared to simulation values in parenthesis.

Tr. #	l_{side} [mm]	l_{lk} [mm]	h_{top} [mm]	l_{gap} [mm]	l_{core} [mm]	d_{core} [mm]	h_{core} [mm]	R_{dc} [mΩ]	$R_{ac,1}$ [mΩ]	$L_m{}^p$ [μH]	$L_{lk,sec}$ [μH]
T_4	11.3	13.4	4.9	1.4	58.4	38.1	15.4	10.9 (10.5)	13.64 (13.6)	38 (39)	1.28 (1.2)
T_5	10.5	6.2	6.0	2.35	60.6	49.9	18.6	9.26 (9.35)	12.05 (12.1)	43.6 (43.9)	1.23 (1.25)

4.5.7. Extension of operation space

In microinverter applications, it is typical that the operating point of the solar panels vary uniquely from the nominal operating conditions across each day of the year due to changing temperatures, irradiation, and presence of partial shading conditions. While these details were not explicitly considered in the optimization process, the optimally selected T_5 transformer performance was validated across a wide range of operating points. The transformer core and conduction losses were analytically verified for an array of input voltages, namely 20 V to 60 V, with power levels between 40 W and 400 W, with results shown in the contour plots in Fig. 4.20. It is clear that the losses are quite uniform between the 20 V and 60 V operation cases across all power levels.



(a) (b) (c)

Fig. 4.20. Extended loss analyses of the T_5 transformer across a range of input voltage and power transfer conditions, where analytical calculations were performed for (a) core losses, (b) conduction losses, and (c) total losses. The white regions of the loss contours are infeasible operating points due to the maximum power transfer condition of the DAB converter with a fixed switching frequency [64].

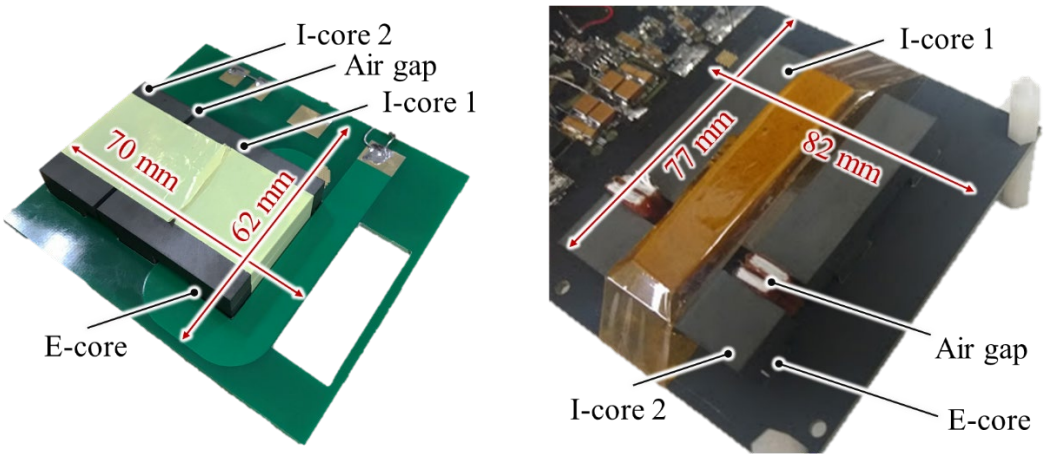
4.6. Experimental results

The EII transformer prototypes were connected to a microinverter circuit with the specifications in Table 4.3 to verify the effectiveness of the proposed design under nominal power transfer conditions. The circuit uses a combination of GaN-based devices (EPC2001C) on the primary-side, and Si-based devices on the secondary-side (IPD60R180P7) and unfolder bridge (TK290P60Y), one of the preliminary design selections from the design analyses in Chapter 3.

4.6.1. Transformer characterization

The selected EII Sec. transformer designs for the E58 (T_4) and custom design (T_5) from the previous section, each shown in Fig. 4.21, were fabricated by a Ferrite core manufacturer and evaluated for their electrical characteristics. Due to the fact that the magnetizing flux path is realized with an un-gapped core, it is first important to characterize the permeability of the core, as the material permeability is only guaranteed within $\pm$20% [76], and additional effects at the core interfaces may attribute to additional permeability reduction. A unique experimental value of permeability was

extracted for each core via the process described in Appendix Section I, as they were produced in separate batches. The effective permeability of the E58 core was concluded to be $\mu_r = 950$, while the effective permeability for the custom core was $\mu_r = 1250$.



(a) (b)

Fig. 4.21. Annotated photograph of the assembled EII Sec. transformers (a) E58-based design (T_4), and (b) custom core design (T_5). In each design, the core gap is controlled with a unity permeability shunt, and compressed with tape. In (b), an additional rigid sheet is placed on the top of the core for assembly support.

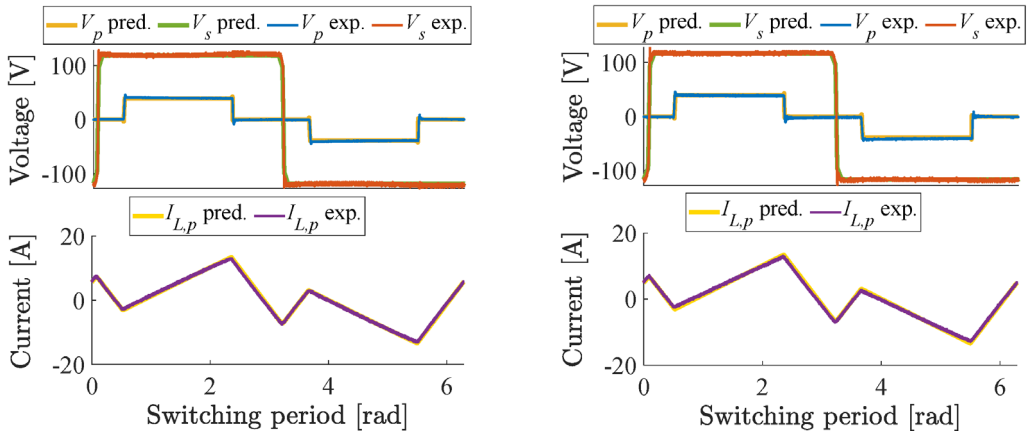
Using the calibrated permeability, the transformer's electrical characteristics were compared to predictions and 3D FEA simulations. The results of the comparison are highlighted in Table 4.7. Due to the permeability reduction, the achieved magnetizing inductance is less than the value expected considering the nominal permeability value (cf. Table 4.6). This may increase conduction losses due to increased RMS current, however there is no significant penalty to core loss, as the flux density in the ungapped magnetizing flux path is proportional to μ_r [cf. (4.18)-(4.20)]. Nevertheless, comparison of the transformer experimental parameters to prediction and 3D FEA simulation is accurate with the proper value of permeability, validating the transformer modeling.

Table 4.7. Experimental electrical parameters of T4 and T5.

Transformer	$L_m{}^p$ [μH]		$L_{lk,pri}$ [μH]		$L_{lk,sec}$ [μH]	
	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.
T_4	22.3	22.8	0.27	0.38	0.92	0.91
T_5	38.7	37.6	0.34	0.36	0.97	0.95

4.6.2. DC-DC hardware testing

The transformers were first connected to the main-circuit in which a steady-state DC-DC converter operation was analyzed. The resulting waveforms are shown in Fig. 4.22, including an overlay of predicted and experimental waveforms plotted in MATLAB. The electrical characterization of both the T_4 and T_5 designs is verified, as the experimental and predicted waveforms (evaluated via the IAM_3 approach in Section 2.4) nearly completely overlap. Furthermore, the transformer current waveforms do not exhibit significant ringing at the primary or secondary switching transitions, implying that the parasitic capacitances of the prototype are adequately mitigated.



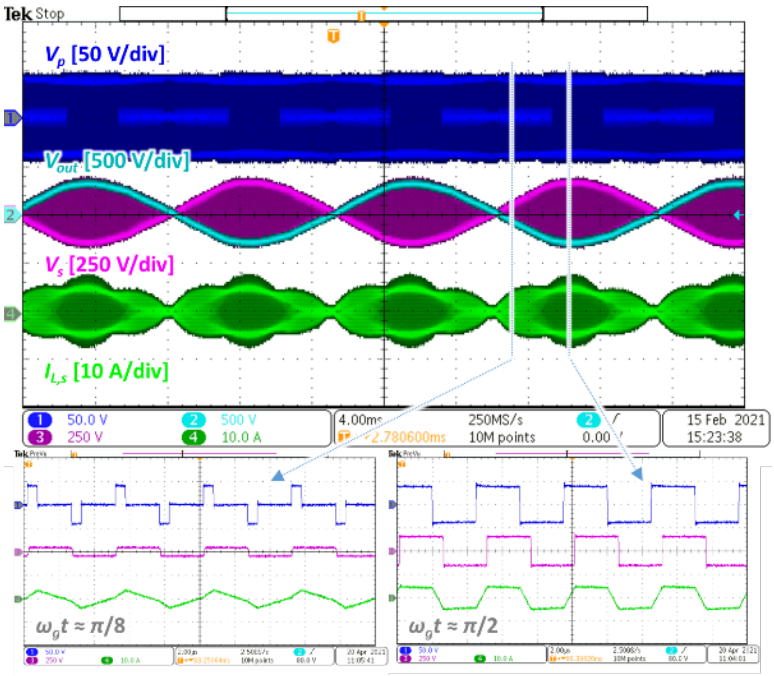
(a) (b)

Fig. 4.22. Comparison between predicted and experimental behavior of the main-circuit at an example DC-DC operating point with, (a) E58-EII Sec. T_4, and (b) Custom-EII Sec. T_5. The demonstrated waveforms are identified in Fig. 4.10.

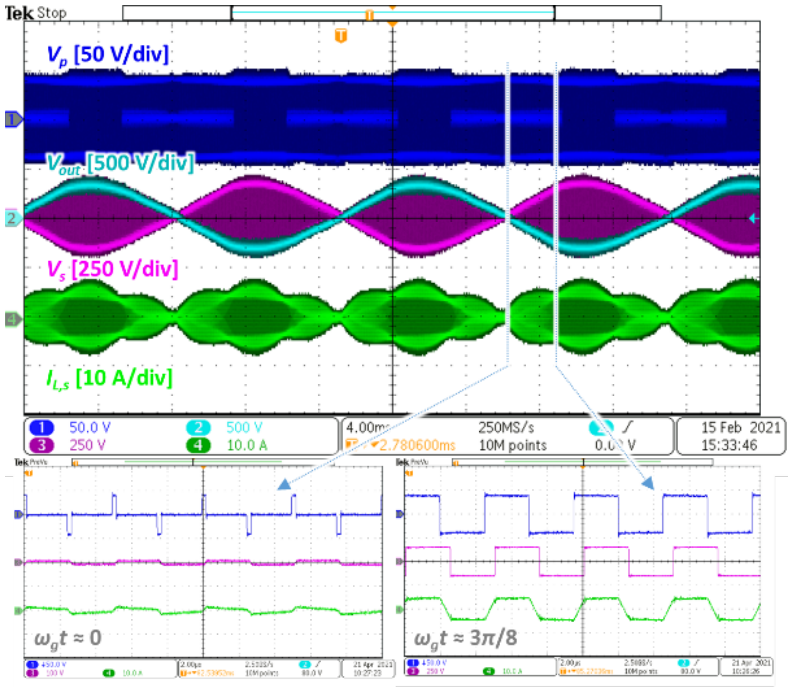
4.6.3. DC-AC hardware testing

The transformer was next evaluated in DC-AC operation for both electrical and thermal performance. In all experimental scenarios the DC input voltage was set to 40 V, and the modulation parameters were determined offline and delivered to the devices through the use of look-up tables (LUTs). The low-frequency electrical waveforms with a resistive load at the 300 W operating condition are shown using T_4 and T_5 Fig. 4.23(a)-(b), respectively. The two low-frequency waveforms are nearly identical and demonstrate good sinusoidal output voltage shaping, as the leakage inductance is controlled to be roughly equal between the two designs and the modulation parameters delivered to the devices were the same. In addition to the low-frequency circuit behavior, several high-frequency zoom-in waveforms are shown at various grid angles ($\omega_g t$), namely $\omega_g t = \{\pi/8, \pi/2\}$ for T_4 and $\omega_g t = \{0, 3\pi/8\}$ for T_5, are also provided in Fig. 4.23(a)-(b) to further demonstrate the phase-shift control principle as well as the transformer performance across a range of operating points. The DC-DC waveforms

were selected differently for each transformer to provide insight into the transformer performance across a wide range of secondary-side voltage levels and modulation conditions, as it was already established in Fig. 4.22 that the performance of both transformers is largely equivalent for similar DC-DC operating points.



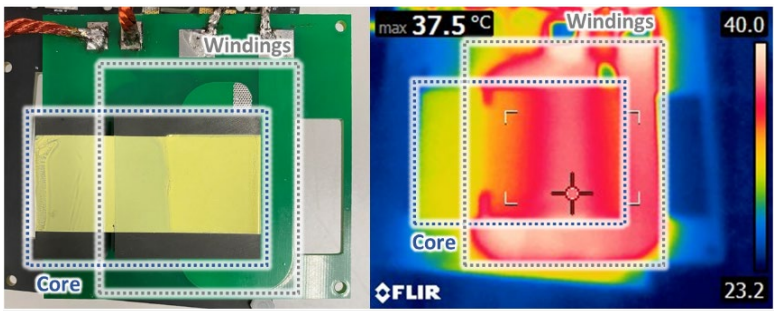
(a)



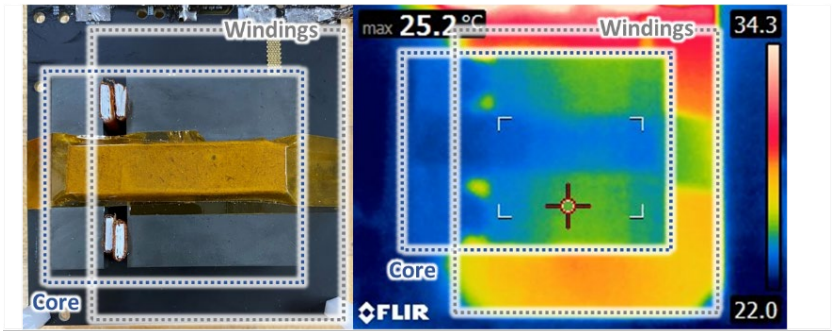
(b)

Fig. 4.23. Circuit electrical performance at the 300 W average power level, (a) low-frequency waveforms with T_4 and high-frequency zoom-in near $\omega_g t = \pi/8$ and $\omega_g t = \pi/2$, (b) low-frequency waveforms with T_5 and high-frequency zoom-in near $\omega_g t = 0$ and $\omega_g t = 3\pi/8$.

Thermal images, captured using a FLIR E6 infrared camera for both prototypes, are shown in Fig. 4.24. It can be observed that for the T_4 design in Fig. 4.24(a), the core hot spot temperature was 37.5 °C along the core region where the primary- and secondary-side windings overlap. This is due in part to indirect heating from the windings, as well as highest core loss density in this segment of the core as the cross-section area is the lowest in the magnetizing flux path. In comparison, the T_5 transformer in Fig. 4.24(b) exhibits significantly reduced core temperatures at 25.2 °C, while the surrounding windings reached ~29 °C. The reduced temperatures in both the core and windings exemplify improved loss performance of T_5.



(c)



(d)

Fig. 4.24. Circuit thermal performance at the 300 W average power level, (a) visible and infrared images of T_4 transformer, and (d) visible and infrared images of T_5 transformer.

4.6.4. Efficiency analysis

The efficiency of the circuit was analyzed at the 120 W, 200 W, and 300 W average power levels, as they contribute most significantly to the microinverter's CEC efficiency. The results of the efficiency characterization are shown in Fig. 4.25, where a peak efficiency of 96.5% is achieved at the 200 W power level with the T_5 transformer. Generally, up to 1% efficiency improvement is realized with the T_5 transformer compared to T_4. In addition to the general efficiency number, the predicted loss contributions from the transformer core, windings, and devices are shown as clustered columns on Fig. 4.25. It is evident that reduction of core loss is a principal contributor to improved efficiency with T_5.

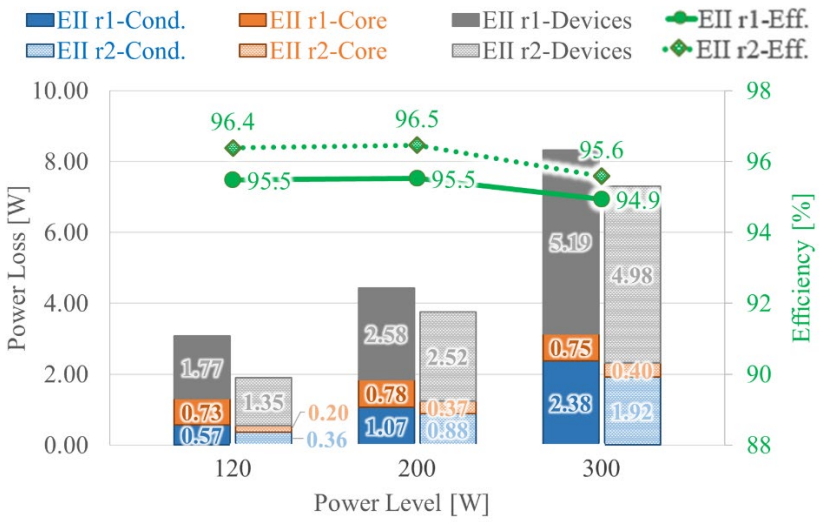


Fig. 4.25. Experimental efficiency of the microinverter with the expected loss breakdown between the transformer and devices at each power level.

4.7. Summary

This chapter has presented a novel planar-based integrated transformer concept and optimal design comparison to other similar leakage-integrated transformers from literature. The proposed transformer achieves asymmetrically distributed controllable

leakage inductance through an independent core leg, where a horizontal air gap is used for reluctance control and AC resistance minimization. Closed-form expressions of the core and winding losses of the proposed design in a DC-AC single-stage microinverter topology are developed and combined with the reluctance modeling in a multi-objective design optimization of the transformer geometry. Extending the design optimization to other integrated transformers from literature revealed benefits in the proposed structure from the perspectives of transformer efficiency (specifically regarding controlled AC resistance and low core losses), footprint area, and parasitic capacitance, alongside a simple winding layout and ease of manufacturability. The proposed transformer design was then analyzed considering a fixed outer geometry versus a fully custom geometry, where a theoretical 0.4% CEC efficiency improvement (from 1.19% to 0.83%) could be achieved at the cost of increased footprint area. Future work can be focused on the design and development of the gapped magnetizing path realization of the proposed transformer, to enable smaller total volume of the transformer with similar, or even lower, total CEC efficiency drops.

Chapter 5. APD Analysis, Design, and Optimization

5.1. Background

Single-phase inverters or rectifiers invariably require a low-frequency energy storage mechanism to buffer the instantaneous mismatch between constant DC power and double-line-frequency (DLF) AC power (cf. Section 1.4) [78]-[79]. The simplest and most practiced approach in the industry mitigate power mismatch is through the use of a capacitor bank at the DC terminals of a single-stage converter [80]-[81], or the intermediate DC-link of a two-stage converter [82], deemed passive power decoupling (PPD) shown in Fig. 5.1. However, stringent requirements on maintaining low voltage ripple at the DC port in many applications, including PV microinverters to achieve high-efficiency MPP tracking, necessitates the use of high-capacitance electrolytic capacitors, which can compromise reliability.

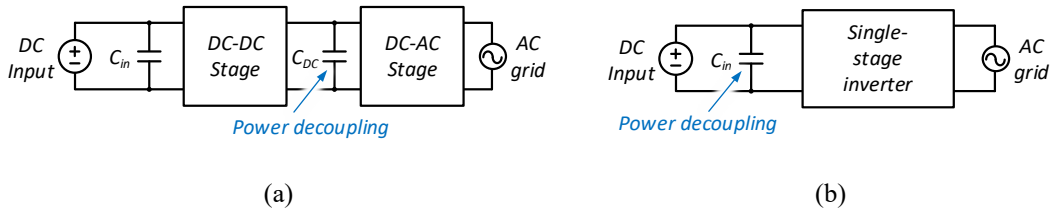


Fig. 5.1. Passive power decoupling approaches, where a bulk power decoupling capacitor is placed, (a) between the DC-DC and DC-AC stage of a two-stage inverter [80]-[81], and (b) at the DC-port of a single-stage inverter [82].

An alternate approach is the utilization of auxiliary active power decoupler (APD) circuits, which employ low-frequency energy buffer capacitors, placed at a different location than the terminal DC port of the converter. This enables wider voltage ripple to exist across the buffer capacitors, leading to a reduced capacitance requirement and use of longer-lifetime film or ceramic capacitors. This APD could be

realized by a voltage source in series with the DC port shown in Fig. 5.2(a) [83], a current source in series with the input capacitance in Fig. 5.2(b) [84], or a current source in parallel with the input port in Fig. 5.2(c) [85],[87]. Of course, the APD circuits in Fig. 5.2(a)-(c) could also be present between the DC-DC and DC-AC stages of a two-stage inverter in Fig. 5.1, or elsewhere within the circuit as in [88] where an APD is placed in series with the secondary-side of the transformer in a single-stage inverter. Finally, the APD could be realized by one port of a multi-port inverter structure, shown in Fig. 5.2(d) [86]-[87]. This chapter deals with one such form of the APD circuit placed in parallel to the DC port of the main converter, shown in Fig. 5.2(c), which is henceforth simply referred to as the APD.

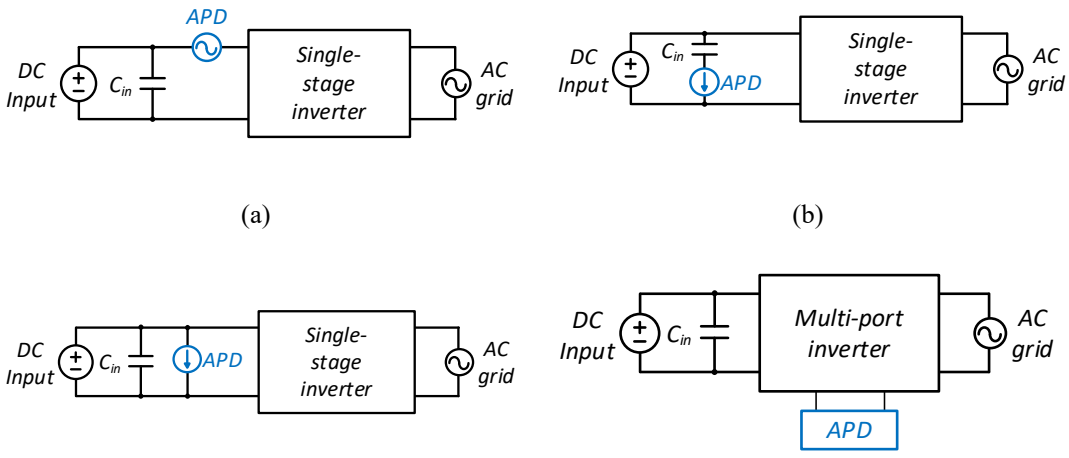


Fig. 5.2. Active power decoupling approaches, where additional circuitry is placed to facilitate equivalent voltage or current sources: (a) a voltage source in series with the DC input, (b) a current source in series with the input capacitor, (c) a current source in parallel to the DC input, or (d) a multi-port inverter of which the APD is realized by one port.

The majority of existing literature on APD topologies [89]-[93] is focused on the design and optimization of high DC voltage (~400 V) and high-power (~2 kW) applications, where buck-derived topologies are preferable. In contrast, the

microinverter application specifically focuses on the use of an APD in applications with relatively low DC port voltage (~40 V), where a boost-type topology is preferable since the decoupling capacitor has a higher available margin of voltage ripple above the DC port voltage. Such a boost-type APD was proposed in [89] and has been investigated with applications in single-phase inverter [85], LED driver [94], and single-phase rectifier [95]. Although the topology has been studied previously, these approaches lack holistic design-level optimization analyses.

The focus of this chapter is the multi-objective design optimization of the boost-type parallel APD circuit, used in PV microinverter applications. By exploring the design space constituted by design variables including device selection, capacitance value, capacitor geometry, inductance value, and inductor core geometry, the analysis aims to optimally select components in regards to a multi-objective optimization of efficiency, power-density, and cost. Analytical efficiency and other performance predictions are compared with experiments on a near-optimal continuous conduction mode (CCM)-based hardware prototype. The experimental prototype is finally confirmed with dual-loop closed-loop control, including both steady-state and transient testing results, as well as integrated testing with the main-circuit from Chapter 3. A portion of the analysis and results presented in this chapter are published in [96].

5.2. Boost-derived APD principle of operation

The boost-derived parallel APD topology is shown in Fig. 5.3. Importantly, the design and optimization of the APD is independent of the single-phase inverter topological selection and design, and as such the single-phase inverter is modeled as a generic block.

5.2.1. Low-frequency principle of operation

The APD switching devices S_1 and S_2 are operated to control the switching-period average of the inductor current, $i_{L,avg}(t) = \langle i_L(t) \rangle_{Tsw}$, to be equal to the 180 degree phase-shifted DLF component of the inverter input current, i_{inv},

$$i_{L,avg}(t) = \left[< i_{inv}(t) >_{2\omega_g} \right] \angle \pi = I_{in} \cos(2\omega_g t) \tag{5.1}$$

where I_{in} is the steady-state DC input current, and ω_g is the grid angular frequency. As such, the input current (and hence voltage) of the PV panel will be DC, and the PV panel maximum power-point can be tracked. The APD capacitor, C, acts as the DLF energy storage component. Due to the large allowable voltage ripple of the APD capacitor, the required capacitance can be much less than the traditional passive decoupling solutions (derived to be 6.6 mF in Section 1.4).

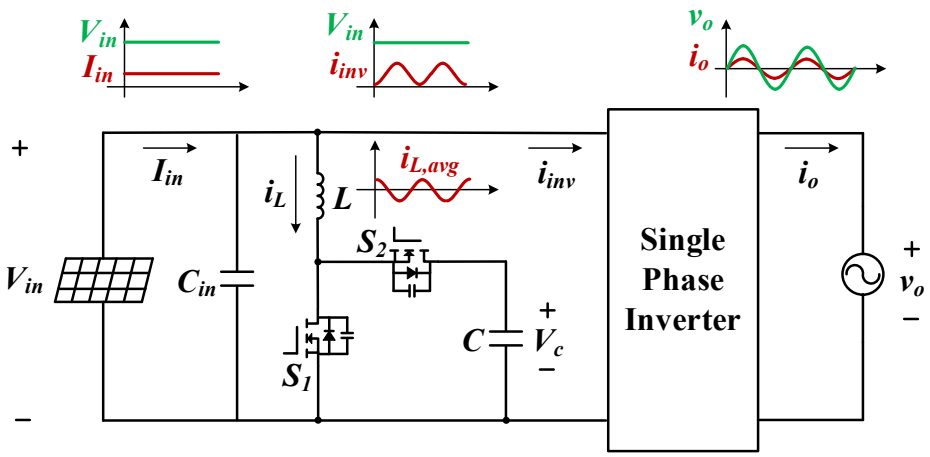


Fig. 5.3. Circuit schematic of the boost-derived parallel APD circuit topology.

The required APD decoupling capacitance can be determined via the closed-form time-varying expression for the capacitor voltage, $V_C(t)$. Modeling the PV input voltage as a fixed DC voltage, V_{in}, in steady-state $V_C(t)$ can be derived through,

$$V_{in}I_{L,avg}(t) = V_C(t)i_{C,avg}(t) = V_C(t)C\frac{dV_C(t)}{dt} \tag{5.2}$$

describing the switching-period-averaged power balance between the input (PV bus) and output (APD capacitor) of the APD. Substituting the inductor current profile from (5.1) leads to an implicitly defined differential equation for $V_C(t)$,

$$V_C(t)\frac{dV_C(t)}{dt} = \frac{V_{in}I_{in}\cos(2\omega_g t)}{C}. \tag{5.3}$$

One such solution to (5.3) can be derived as,

$$V_C(t) = \sqrt{\frac{V_{in}I_{in}}{\omega_g C}\left(\sin(2\omega_g t)+1\right) + V_{C,min}^2} \tag{5.4}$$

where the minimum value of the capacitor voltage, $V_{C,min}$, is selected as the boundary condition. Importantly, $V_{C,min}$ must be selected to guarantee the boost operation at all

times (i.e. $V_{C,min} > V_{in}$). With (5.4), $V_C(t)$ is known for all operating points and is dependent only on the values of C and $V_{C,min}$. Furthermore, the duty cycle across the line-cycle $d(t)$ is also known from the conventional boost converter voltage gain expression $d(t) = 1 - V_{in}/V_c(t)$.

5.2.2. High-frequency principle of operation

Due to the AC nature of the inductor current, the APD effectively works in "boost-mode" for half of the DLF period when $i_{L,avg} > 0$, and in "buck-mode" when $i_{L,avg} < 0$. In conventional CCM operation, the switching frequency is fixed and the inductance is designed to tolerate a specific current ripple, which generally causes the polarity of the inductor current to remain fixed during the switching period, except near the current zero-crossing when low average current values are required to be tracked. In general, usage of CCM modulation results in one device achieving inherent ZVS, while the other is hard-switched. Henceforth, the device achieving natural soft-switching (natural soft-switching refers to switching transition of the device which undergoes ZVS turn-on for CCM operation, that is S_2 in "boost-mode" and S_1 in "buck-mode") is deemed the synchronous device, while the other is termed the asynchronous device (i.e. S_1 in "boost-mode" and S_2 in "buck-mode"). The inductor current ripple, RMS current, peak current (i.e. the current value at the inherent ZVS transition), and valley current (i.e. the current value at inherent hard-switching if the same polarity as the peak current), in the inductor can be determined by,

$$\Delta I_{L,pp}(t) = \frac{V_{in} d(t)}{L f_{sw}} \tag{5.5}$$

$$I_{L,rms}(t) = I_{L,avg}^2 + \frac{1}{12} \Delta I_{L,pp}^2 \tag{5.6}$$

$$I_{peak}(t) = \left| I_{L,avg}(t) \right| + \frac{\Delta I_{L,pp}}{2} \tag{5.7}$$

$$I_{valley}(t) = \left| I_{L,avg}(t) \right| - \frac{\Delta I_{L,pp}}{2}. \tag{5.8}$$

5.3. Decision space identification

To facilitate a multi-objective design optimization, the decision space must first be identified. In particular, the decision space includes all of the components available for selection in the design, namely the devices, capacitors, and inductors, to identify the best combination of components per the objection functions. The following sections detail the various component databases considered for the three component categories.

5.3.1. Transistor database

From a device perspective, the APD shall consider only the use of GaN-based devices in the 150 V-200 V range. Due to the inherent hard-switching of the APD in CCM operation, GaN-based devices are considered due to the much improved switching characteristics (generally lower parasitic capacitances) over similarly-rated Si-based devices. Aside from the reductions in parasitic capacitance, the improved switching performance of GaN is realized by the absence of reverse recovery charge, Q_{rr}. From the voltage rating perspective, 150 V to 200 V enables a large voltage ripple to minimize the capacitance requirement.

In the 150 V to 200 V range, six unique devices from EPC are available, with specifications outlines in Table 5.1. The devices demonstrate trade-offs between voltage rating, conduction and switching-related performance (inferred from the tradeoff between $R_{ds,on}$ and C_{oss}), and cost. The cost column (indicated *per device* though there are two devices in the APD topology) was determined according to available quotations from trustedparts.com at a quantity of 1,000.

Table 5.1. Feasible devices for the APD circuit.

Switch	$V_{ds,max}$ [V]	$I_{d,max}$ [A]	$R_{ds,on}$ [mΩ]	C_{oss} [pF]	Cost [$]
EPC2033	150	48	5	480 @ 120 V	4.68
EPC2059	170	24	6.8	267 @ 85 V	1.78
EPC2010C	200	22	18	240 @ 100 V	3.39
EPC2207	200	14	15	130 @ 100 V	1.66
EPC2215	200	32	6	390 @ 100 V	3.16
EPC2034C	200	48	6	641 @ 100 V	3.48

In particular for CCM operation, hard-switching will result in a voltage overshoot across the devices at a switching transition due to parasitic inductances in the layout. As such, ~1.3x margin of the voltage rating is typically considered in the selection of the capacitor to ensure device safety at high stress conditions. That is to say that for the 200 V rated devices, the maximum voltage on the capacitor should be less than ~154 V, respectively. Due to this, the capacitance requirement will inevitably be larger considering 150 V devices, because of the restricted voltage range.

5.3.2. Capacitor database

The capacitor database can be formed with knowledge of the devices selected and known voltage profile of the APD as a function of the capacitance. The capacitance space is only limited by a lower bound, which corresponds to the minimum capacitance such that,

$$C_{min} = C\ s.t.\ \max\{(5.4) < V_{C,lim} \text{ for } P = P_{av,max} \text{ and } V_{C,min} = V_{in} + 5\text{ V}\} \tag{5.9}$$

where $V_{C,lim}$ is the upper limit on the capacitor voltage according to the tolerated switch stress identified in the previous section. Of course, any capacitance larger than the minimum will be a feasible design, however too large of a capacitor bank will be expensive and occupy significant volume in the system. To realize the total APD capacitance, a parallel connection of smaller capacitor "building blocks" enables high total capacitance as well as reduced equivalent series resistance (ESR), reducing the total capacitor loss. The considered capacitors with unique geometries are shown in Table 5.2, alongside the estimated capacitor cost according to available quotations from trustedparts.com at the largest available quantities. Interestingly, manufacturers provide similar capacitances in different packages (cf. the 22 μF, 33 μF, and 47 μF capacitors), which should be considered independently for unique volumetric advantages. The capacitors in Table 5.2 are in the R60 product line from KEMET, where the maximum dissipation factor is specified to be 1% [97], from which the equivalent series resistance can be calculated according to,

$$ESR(f) = \frac{DF}{2\pi f C}. \tag{5.10}$$

Table 5.2. Decision space of considered KEMET R60 capacitors [97].

Cap. index	C [μF]	Length [mm]	Width [mm]	Height [mm]	Cost [$]
1	6.8	32	13	12	0.94
2	10	32	9	17	1.45
3	15	32	11	20	2.20
4	22	32	13	22	2.77
5	22	41.5	11	22	2.77
6	22	32	24	15	2.77
7	33	41.5	24	15	2.99
8	33	41.5	13	24	2.99
9	33	32	14	28	2.99
10	47	41.5	24	19	5.45
11	47	32	18	33	5.45
12	47	41.5	16	28.5	5.45
13	68	41.5	19	32	6.33

5.3.3. Inductor database

Several inductors have been considered with variation in inductor geometry and number of turns. In regards to inductor geometry, only the ER core shape was selected due to the reduced footprint area as compared to EE core shapes, where the windings extend outside of the core footprint. The considered inductors are shown in Table 5.3, alongside estimated costs per core with available quotations from trustedparts.com at the maximum available quantity. Each of the inductor designs was simulated in Ansys Maxwell 3D to extract the inductance, DC resistance, and AC resistance as a function

of frequency, of which the parameters shown in Table 5.3. In each case, the core material was 3F36 from Ferroxcube, due to its advantages of low core loss at the considered operating frequency, and wide operating temperature range [98].

Table 5.3. Decision space of APD inductors considered for the multi-objective analysis.

Ind. index	Core	# turns, N	L [μH]	R_{dc} [mΩ]	$R_{ac,200k}$ [mΩ]
1	**ER 32/6/25**	8	31.7	32.2	94.5
2	Cost = \$1.21	10	40.5	53.1	159.1
3	L = 32.1 mm	11	52.9	63.5	189.1
4	W = 25.4 mm	14	68.3	104	330.1
5	**ER 41/7.6/32**	4	22.3	8.1	15.3
6	Cost = \$1.56	6	36.9	20.3	38.7
7	L = 40.6 mm	7	48.4	26.5	52.3
8	W = 32 mm	9	63.4	43.1	99.6
9	**ER 51/10/38**	4	31.1	8.6	13.3
10	Cost = \$3.35	5	48.9	15.2	22.7
11	L = 51 mm	6	62.3	21.8	32.8
12	W = 38.1 mm	7	75.2	28.3	44.9

5.4. Multi-objective optimization

With the decision space identified in the previous section, the constraints and objective functions over which to compare all feasible designs is formulated. The multi-objective analysis incorporates perspectives of loss, power density, and cost.

5.4.1. Efficiency drop analysis

The loss model of the APD considers device switching and conduction loss, inductor core and conduction loss, and APD capacitor ESR loss. Device switching loss is based on the approach introduced in [99] and can be calculated via,

$$P_{sw,on} = \left[\frac{1}{2} t_{ri} V_C I_{on} + \frac{1}{2} t_{fv} V_C (I_{on} + 2I_{oss})\right] f_{sw} \tag{5.11}$$

where I_{on} is the inductor current value at the turn-on transition instant, $2I_{oss}$ corresponds to additional channel current due to the charge and discharge of the parasitic output capacitance, t_{ri} is the rise-time of the device current, and t_{fv} is the fall-time of the device voltage. The calculations of t_{ri}, t_{fv}, and I_{oss} are based on detailed switching transition modeling considering parasitic drain inductance, common-source-inductance (CSI), non-linear output capacitance, and gate resistance. Details of these calculations have been omitted for brevity but can be found in [99]. In the following analyses, considered values of drain inductance L_d = 0.5 nH, L_s = 0.1 nH, and turn-on gate resistance R_g = 7 Ω. The parasitic inductances are based on typical values for EPC devices considering the device package (low L_s) and optimal power loop structure (low L_d) [100]-[101]. Aside from turn-on loss, turn-off loss can be treated as negligible for the GaN devices, informed by LTspice simulations.

To verify the switching loss model for the devices under study, example LTspice simulations were performed. The simulations were repeated to calculate switching loss of each considered device type under different DC-DC operation. Validation of the considered switching loss model is performed across six DC-DC operation points with V_{in} = 40 V, and unique average inductor current and capacitor

voltages. The turn-on loss was extracted from the multiplication of the device's simulated channel current and voltage waveform. The comparison is shown in Fig. 5.4, which shows a strong agreement between the predicted and simulated turn-on loss with less than 4% error at all evaluated conditions for two of the considered devices. Similar analysis was performed for all of the remaining devices, with tolerable error margins between simulation and analytical prediction.

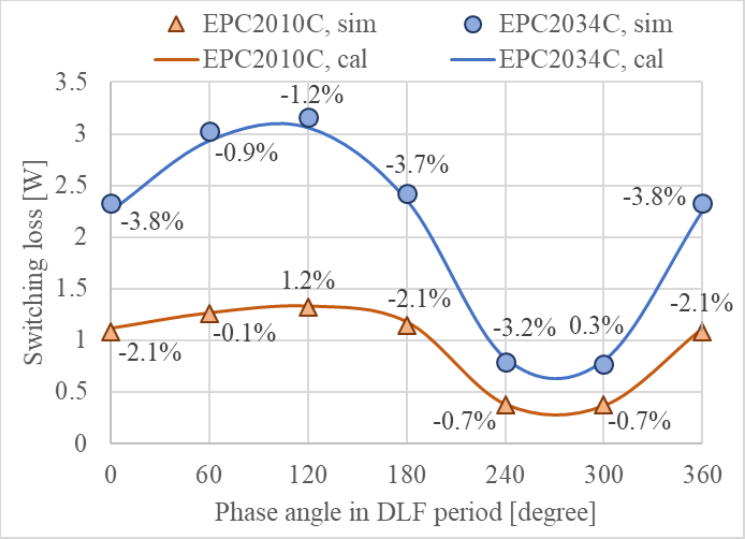


Fig. 5.4. Comparison of switching loss between the analytical prediction method derived in [99], and detailed LTspice simulations. Error between simulation and calculation is shown as a data label at each evaluated operating point.

Device conduction and inductor DC winding losses are calculated based on the inductor RMS current,

$$P_{cond,sw} = I_{L,RMS}^2 R_{ds,on} \tag{5.12}$$

$$P_{L,DC} = I_{L,RMS}^2 R_{L,DC} \tag{5.13}$$

where $I_{L,rms}$ is the RMS of the inductor current calculated from (5.6). On the other hand, the inductor's frequency-dependent AC winding loss is calculated according to the current ripple in the inductor,

$$P_{L,AC} = \left(\frac{\Delta I_{L,pp}}{2}\right)^2 R_{L,AC}(f_{sw}) \tag{5.14}$$

where ΔI_{Lpp} is the peak-to-peak current ripple from (5.5) and $R_{L,AC}$ is the AC resistance of the inductor windings at the switching frequency, f_{sw}. While the triangular inductor current is generally composed of multiple frequency harmonics, the considered assumption in (5.14) is that half the peak-to-peak ripple is the amplitude of the switching frequency component. While this is an over-approximation for the switching frequency component, it is tolerable to account for additional conduction loss components at higher frequency harmonics with lower amplitude currents but larger AC resistance. On the other hand, the capacitor ESR loss is calculated by considering four low-frequency harmonics of the switching period averaged capacitor current,

$$P_{C,ESR} = \sum_{k=1}^{4} |i_C|^2_{f=k\cdot 2f_g} ESR\left(k \cdot 2f_g\right) \tag{5.15}$$

where the 'k^{th}' frequency harmonic of the grid frequency of i_C is squared and multiplied by the capacitor ESR at the 'k^{th}' frequency harmonic of the grid frequency. Finally, inductor core loss is calculated using the general Steinmetz's equation (GSE) [102],

$$P_{core} = C_m \left(\frac{\Delta B_{pp}}{2}\right)^x f_{sw}^y V_e \tag{5.16}$$

where $\{C_m, x, y\}$ are the manufacturer specified Steinmetz parameters, ΔB_{pp} is the peak-to-peak flux density in the core, and V_e is the effective core volume. In the utilization of (5.16), the DC bias impact on the core loss has been neglected, which may lead to an underestimation of the core loss specifically at higher power levels [103].

With the loss model discussed above, power loss can be calculated at '*N*' number of operating points across the DLF period, and then averaged. Since the APD is connected in parallel to the main inverter circuit, the total microinverter circuit loss is the sum of the losses in the APD and the main inverter stage. To quantify the efficiency-related performance of the APD circuit, a factor deemed the APD efficiency drop ($\eta_{APD,drop}$) is introduced, which denotes the net decrease in microinverter efficiency due to the addition of the APD. This factor is given by,

$$\eta_{APD,drop-i} = \frac{P_{APD,loss-i}}{P_{in-i}} \tag{5.17}$$

where $P_{APD,loss\text{-}i}$ is the average of the losses in the APD across the DLF period at a given average input power level $P_{in\text{-}i}$. Finally, as defined in Appendix Section A, weighted efficiency metrics such as the California Energy Commission (CEC) efficiency are of particular significance. The APD efficiency drop at a given power level can be extended to define the APD CEC efficiency drop, calculated by,

$$Y(1) = \eta_{APD,drop} = \sum_{i=1}^{6} C_i \eta_{APD,drop-i} \,. \tag{5.18}$$

5.4.2. Power density analysis

As initially mentioned, design and optimization of the APD can be largely performed independently of the main-circuit design. With that being said, the APD and main-circuit should ultimately be designed on the same PCB for minimal cost, and hence some degree of cooperative design is required. Specifically this is important from a power density perspective, as the APD capacitor will decide a significant portion of PCB area. Furthermore, the APD capacitor will determine the bottom-side maximum height, as the APD capacitor will be one of the only components mounted on the bottom-side of the PCB (as it is a through-hole component). It is assumed moving forward that the main-circuit is already designed based on the T_5 transformer concluded to achieve optimal performance in Chapter 4, and the APD is to be designed to fit into the remaining space. An example of the main-circuit PCB layout with the optimal transformer from the previous section, is shown in Fig. 5.5. While the main-circuit occupies the green 'L' shaped area, the APD should be designed to fit into the remaining rectangular area without necessitating additional PCB length and width. However, additional area may be inevitable, and is represented by the dimensions ΔL and ΔW, such that,

$$A_{APD} = (L_A + \Delta L)(W_A + \Delta W) \tag{5.19}$$

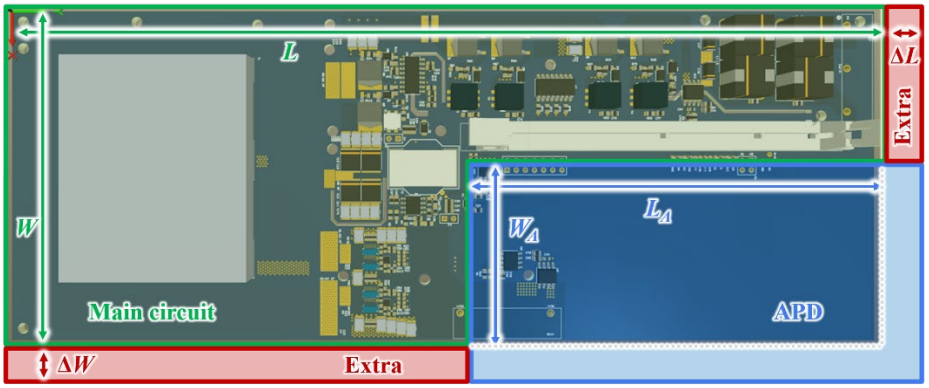


Fig. 5.5. Example main-circuit PCB area and associated dimensions, alongside variable identification associated with the placement of the APD with the main-circuit PCB.

Considering the use of GaN devices, which have an ultra-small package size, the main PCB area in the APD will be occupied by the inductor and capacitors. Because the capacitors are mounted on the under-side of the PCB, the remaining top-side area above the capacitors can be used for sensors, devices, gate driving, and other components, such that the area is not unused. Considering a specific capacitor and inductor, the required APD area can be calculated by,

$$A_{APD} = A_{ind} + A_{cap} n_{cap} \tag{5.20}$$

where A_{ind} is the inductor footprint area, A_{cap} is the capacitor footprint area, and n_{cap} is the number of capacitors in parallel to realize the total capacitor bank.

With knowledge of the cutout in the main-circuit PCB to occupy the APD (i.e. L_A and W_A), the "extra area", i.e. the area required to fit the APD external to the main-circuit footprint (the red portion in Fig. 5.5), can be calculated by,

$$A_{extra} = \Delta L(W - W_A) + \frac{A_{APD}}{L_A + \Delta L}(L - L_A)\,. \tag{5.21}$$

To minimize this area, a derivative can be taken with respect to the extra length, determining the minimum ΔL and ΔW combination to realize the required APD area. The closed-form expression for the optimal ΔL can be derived as,

$$\Delta L_{opt} = -L_A + \sqrt{A_{APD}\frac{L - L_A}{W - W_A}} \tag{5.22}$$

where ΔW can then be calculated according to (5.19). Importantly, values of ΔL and ΔW are limited to be strictly greater than or equal to zero. While the analysis assumes that the components can always fit within the provided area, and hence there is no associated "packing problem", it is a decent estimate of the impact of the APD on the full system power density. With the revised external dimensions decided, and considering the maximum top-side height is determined by the main-circuit and is known beforehand, the system-level power density can be calculated according to,

$$Y(2) = \rho = \frac{P_{av,max}}{(L + \Delta L)(W + \Delta W)\left(h_{top} + h_{cap}\right)}. \tag{5.23}$$

Based on analysis of the optimal transformer design from Chapter 4, and a revised main-circuit PCB, the considered dimensions of the main-circuit and available APD area are shown in Table 5.4, which is used for the subsequent optimal analysis.

Table 5.4. Considered main-circuit dimensions for power density analysis.

L [mm]	W [mm]	L_A [mm]	W_A [mm]	h_{top} [mm]
238	90	87	52	7

5.4.3. Cost analysis

The cost objective is straightforward to calculate via,

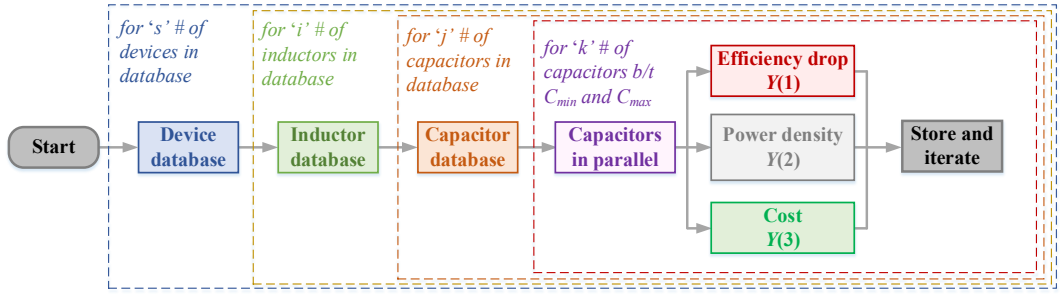
$$Y(3) = T_{tot} = 2T_{dev} + 2T_{ind} + n_{cap}T_{cap}. \tag{5.24}$$

where the costs of the devices ($2T_{dev}$), inductor core ($2T_{ind}$), and capacitors ($n_{cap}T_{cap}$), are summed. In particular, there are two devices in the circuit, two ER core pieces that create the full inductor core structure, and n_{cap} number of capacitors realizing the APD capacitor bank. The costs of the current sensor (ACS730LLCTR-20AB) and gate driver (LMG1210) have been omitted from the cost calculation, as these components are considered to be equal for all of circuit configurations.

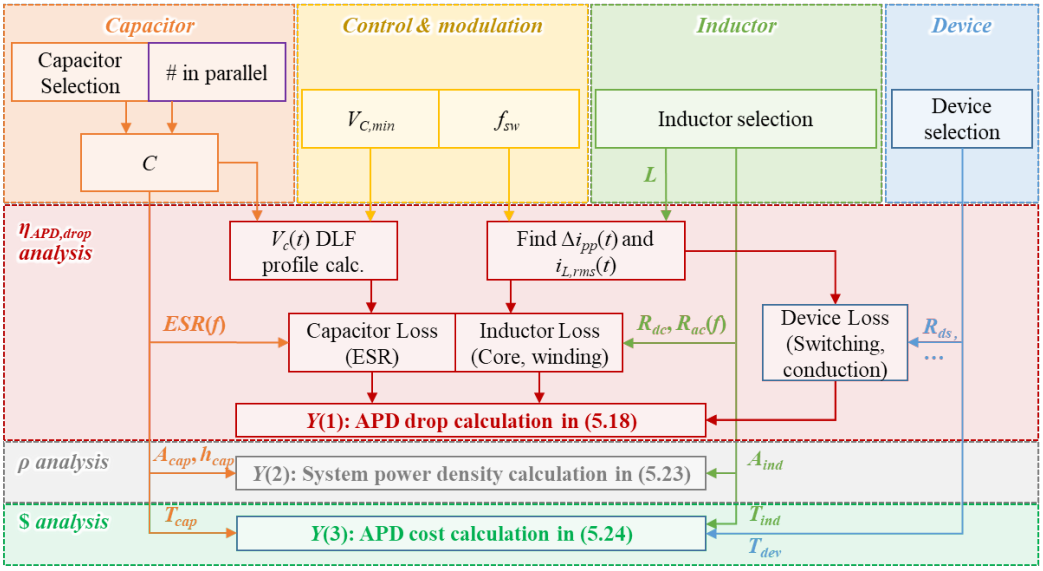
5.4.4. Optimization implementation

To perform the multi-objective optimization analysis, all possible combinations of designs in the decision space were analyzed for their performance across the objective functions of CEC efficiency drop, power density, and cost. A block diagram of the procedure is shown in Fig. 5.6(a), where there are independent for-loops for devices, inductors, and capacitors. In addition to these outer design loops, there is an inner design loop that varies the number of capacitors from a minimum number in parallel [cf. (5.9)] to a pre-determined maximum number in parallel. For the analysis in the subsequent section, the maximum capacitance of the APD to be considered was 300 μF. Finally, for a given set of device, inductor, and capacitor selections, the three objective functions are calculated [cf. (5.18), (5.23), and (5.24)], with a more detailed flow chart indicated in Fig. 5.6(b). Considering six devices, twelve inductors, thirteen

base capacitors, up to ten variations of capacitors in parallel, and five switching frequencies, around 34,000 unique design combinations were analyzed.



(a)



(b)

Fig. 5.6. Block diagram of the multi-objective optimization analysis for APD component selection (a) outer-loop component-level iteration, and (b) enhanced detail for objective function calculations.

5.4.5. Results

The results of the multi-objective analysis are presented in Fig. 5.7, including all feasible design configurations as unfilled circles and the Pareto front designs as filled stars. Based on optimization theory, the Pareto front is comprised of feasible

designs that are not dominated by any other feasible design. For any two feasible solutions, design 1 is said to dominate design 2 if,

$$Y_1(i) \leq Y_2(i)\ \forall i \in \{1,2,\dots,o\} \text{ and } \exists i \in \{1,2,\dots,o\}\ s.t.\ Y_1(i) < Y_2(i) \tag{5.25}$$

where o is the number of objective functions, in this case equal to three, and the objective is to minimize Y_i (the inequality signs are reversed in the case of maximization) [104]. Based on evaluation of the Pareto front candidates, a preference was first given to cost minimization, then loss minimization, and finally power density maximization. Based on these design tradeoffs, the indicated design was selected. The design details of the selected CCM configuration are highlighted in Table 5.5.

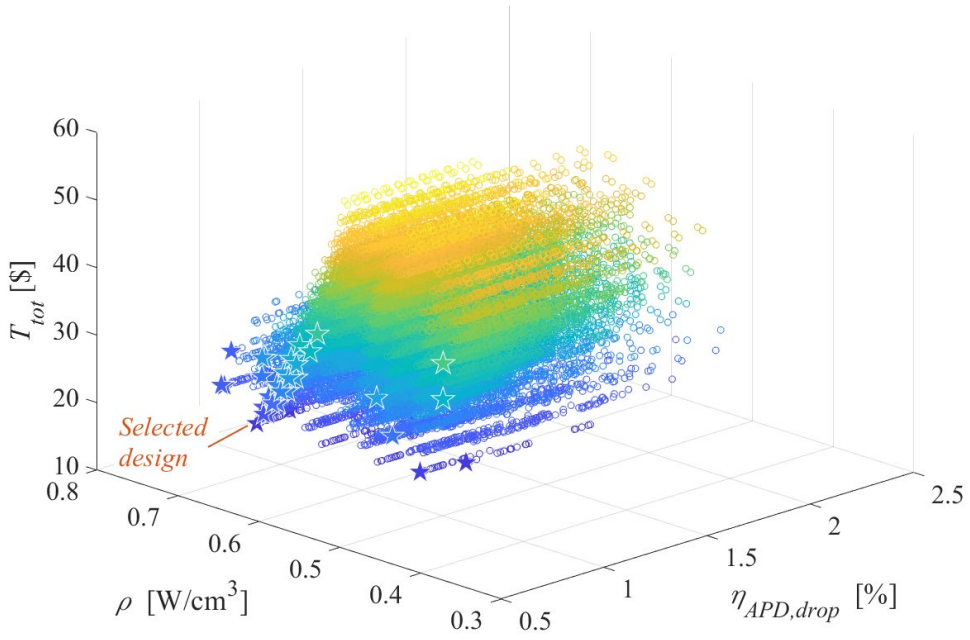


Fig. 5.7. Results of the multi-objective optimization analysis for the APD component selection, (a) full design space visualization, and (b) Pareto front candidates achieving the pre-determined efficiency drop and power density targets.

Table 5.5. Component selection for selected APD design.

Device	Inductor	Capacitor	n_{cap}	f_{sw}	$Y(1)$	$Y(2)$	$Y(3)$
EPC2207	ER41, $N = 4$, $L = 22\ \mu$H	33 μF (24 x 41.5 x 15 mm)	4	200 kHz	0.82%	0.6 W/cm^3	\$18.41

5.5. Controller design

The closed-loop system of the APD is shown in Fig. 5.8, featuring closed-loop controllers for the inductor current and average capacitor voltage. As shown, the dual-loop control enables the sinusoidal current tracking while simultaneously controlling the average voltage in the capacitor. The two loops are designed such that the inner current control loop has a much higher bandwidth than the outer voltage control loop. The DC component of the capacitor voltage, extracted with a low corner frequency low-pass filter, was compared to a reference, where the resulting error was controlled to zero via a PI controller. The output of this controller is effectively a DC current that is required to be injected into the APD to ensure capacitor voltage balance through each DLF period. A representative main-circuit current reference is generated by a signal generator and fed to the controller. In order to replicate the true performance as closely as possible, a DC offset was also introduced in the reference current signal from the signal generator, where the 120 Hz component was extracted with a band-pass filter. The 120 Hz current component plus the DC component from the voltage controller together constitutes the total current reference for the APD circuit. This current reference is compared to the sensed inductor current during each switching period, and the error is passed to a PI controller. The PI controller output sets the duty cycle of the low-side switch, from which the switching signals for the two devices can then be derived from a modulator.

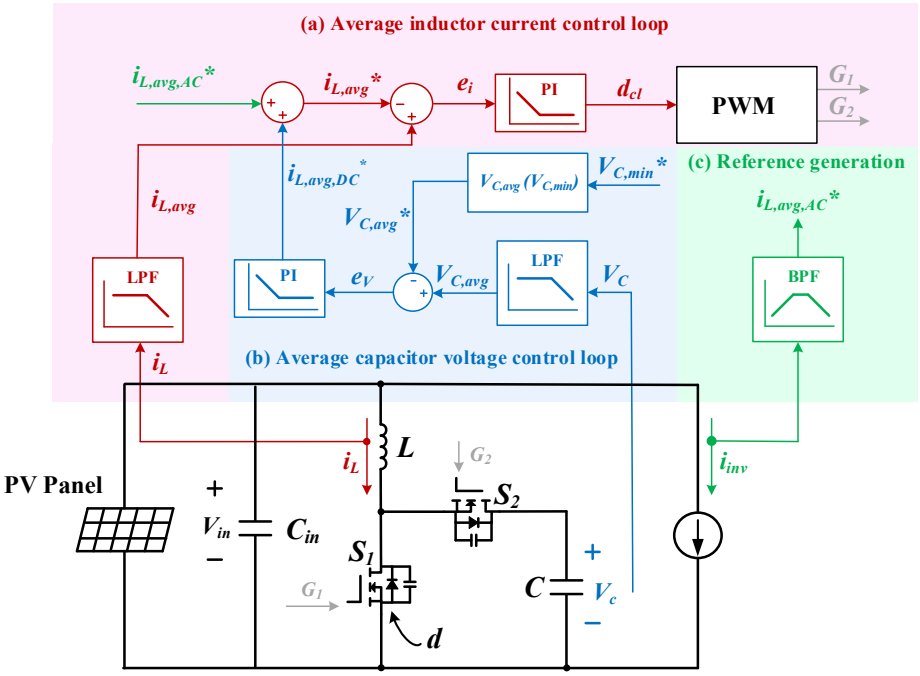


Fig. 5.8. Closed-loop control circuit for the experimental APD prototype.

As the APD is a non-linear time-varying dynamical system, the plant transfer function varies with both power level and terminal voltage levels. The approach of quasi-static approximation introduced in [106] is hence invoked, where it is assumed that the DLF variations are much slower than the current controller dynamics such that the circuit always operates at a quiescent operating point. In this case, an equilibrium analysis can be performed to design the average current controller with the time-varying transfer functions, where the system stability must be ensured across all operating points. The plant transfer function describing the perturbation of the duty cycle d to that of i_L, is derived using the approach in [106] as,

$$P(s) = \begin{cases} \dfrac{V_C^2 Cs + 2V_C V_{in} i_{L,avg}}{V_C^2 LCs^2 + V_{in} i_{L,avg} Ls + V_{in}^2}, & i_{L,avg} > 0 \\ \dfrac{V_C V_{in} C_{in} s + V_C |i_{L,avg}|}{V_{in} LC_{in} s^2 + |i_{L,avg}| Ls + V_{in}}, & i_{L,avg} < 0 \end{cases} \quad (5.26)$$

where V_{in}, V_C, and $i_{L,avg}$ describe DC-DC operating points that are time-varying across the DLF period.

A PI controller is used as the error-driven compensator in the inductor current loop for simplicity and satisfactory performance. The compensator transfer function, described by the proportional (k_p) and integral gain (k_i) can be written as,

$$C(s) = k_p + k_i/s \cdot \quad (5.27)$$

Furthermore, a low-pass-filter (LPF) is used to eliminate switching frequency ripple from the sensed inductor current, described by the following transfer function,

$$L(s) = \frac{1}{1 + s/2\pi f_{c,LPF}} \cdot \quad (5.28)$$

where $f_{c,LPF}$ is the corner frequency. The open-loop system transfer function can hence be written as,

$$H_{OL}(s) = P(s)C(s)L(s) \cdot \quad (5.29)$$

By analyzing H_{OL}, the LPF and PI controller parameters can be designed considering desired attenuation of switching ripple, low-frequency gain, crossover frequency, and phase margin. Both low frequency and high frequency properties need to be considered in the system-level controller design, where the low frequency (120 Hz) gain of the system determines the average current tracking performance, and the high frequency properties affect the system stability.

First, the LPF can be designed to attenuate switching ripple current components between the current sensor and the controller analog-to-digital converter (ADC). With a selected inductance of 22 μH and switching frequency of 200 kHz (cf. Table 5.5), an attenuation of roughly -12 dB is required at the largest ripple condition, such that a simple first order analog LPF can be implemented with a corner frequency of 50 kHz. Next, the PI controller should be designed such that two key details are met: 1) the system crossover frequency is around a decade below the switching frequency, and 2) the minimum phase margin is positive, greater than an arbitrary threshold of 60°. As previously mentioned, the constant variation of the DC-DC design point must also be explicitly considered for the APD controller design. Nevertheless, there will always exist one operating point for a particular system design in which the phase margin is the minimum, and the cross-over frequency (f_{cr}) is the maximum; this is to say that a system design that achieves stability at this operating point ensures stability at all other operating points. The loop transfer function bode plots for the family of DC-DC operating points at the 400 W average power level for the CCM system is shown in Fig. 5.9, according to the system parameters in Table 5.6. It is clear that the system achieves a maximum crossover frequency of 18.9 kHz and a phase margin of 61°. While detailed analysis was conducted for the closed-loop design of the current-loop PI compensator, design of the voltage-loop PI controller and LPF in Fig. 5.8 was determined empirically through extensive simulations, with the finally selected parameters listed in Table 5.6.

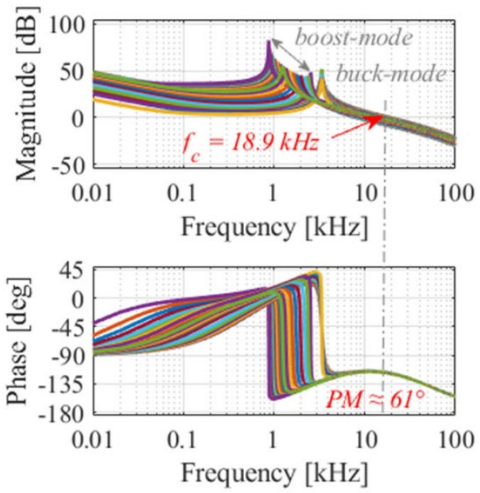


Fig. 5.9. Family of bode plots with identified minimum phase margin for the CCM design. The 400 W line cycle is considered with the design specifications from Table 5.6. An input capacitance of C_{in} = 100 μF is considered.

Table 5.6. System-level parameters for the current and voltage control loops.

Current loop			Voltage loop		
k_p	k_i	$f_{c,LPF}$	k_p	k_i	$f_{c,LPF}$
0.02	300	40 kHz	0.0185	0.055	12 Hz

5.6. Experimental results

The optimal APD design configuration highlighted in Fig. 5.7 with detailed specifications provided in Table 5.5, was built for experimental verification. The prototype APD was developed on an independent PCB for individual testing without the main-circuit inverter. A photograph of the prototype is shown in Fig. 5.10.

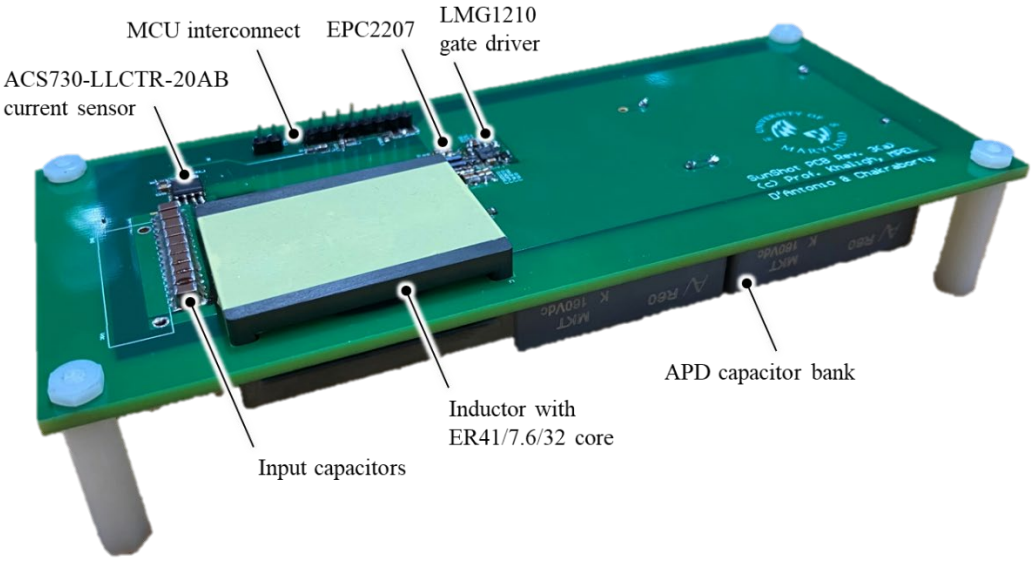
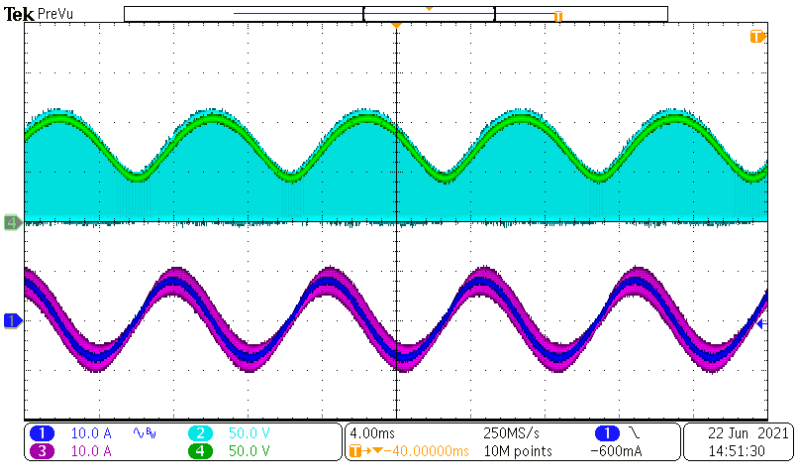


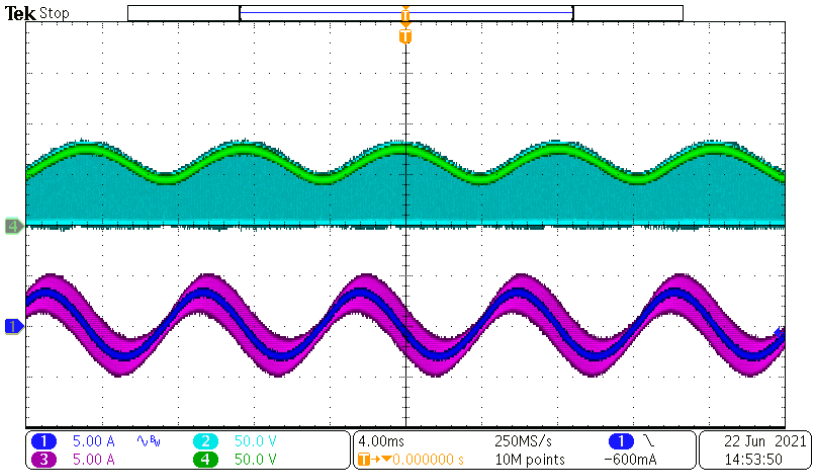
Fig. 5.10. Annotated photograph of the optimal APD hardware prototype.

5.6.1. Steady-state and dynamic performance

The hardware prototype was tested in closed-loop according to the control diagram in Fig. 5.8. Experiments were run on the hardware prototype up to the 300 W power level, of which results are shown at the 120 W power level in Fig. 5.11(a) and the 300 W power level in Fig. 5.11(b). In each case, the input voltage was 40 V, and the capacitor average voltage reference was set such that the minimum capacitor voltage was near 45 V. It is clear in both cases that the sinusoidal current tracking is enabled, and the capacitor voltage is regulated with the desired average (and hence also minimum) value.



(a)

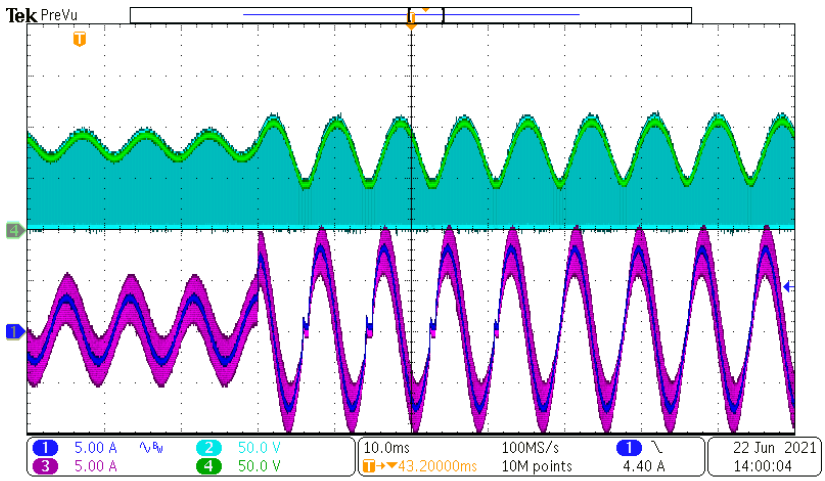


(b)

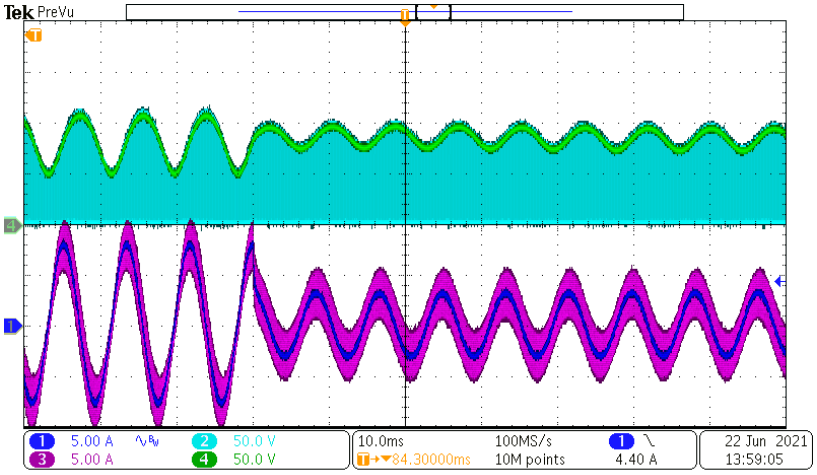
Fig. 5.11. Steady-state closed-loop results for the APD at (a) 120 W condition, and (b) 300 W condition.

Next, a dynamic experiment was run where the current reference was changed between ~3 A (i.e. the 120 W condition) to ~7.5 A (i.e. the 300 W condition), while the average capacitor voltage reference was not changed. The experimental results for the step-up transient are shown in Fig. 5.12(a), where it is clear that the current loop instantly tracks the new reference, while the capacitor voltage settles back to the desired average value after a couple of DLF cycles. On the other hand, the step-down transient

is shown in Fig. 5.12(b), where again both the current and voltage loops are able to nearly instantly react to the perturbed current reference.



(a)



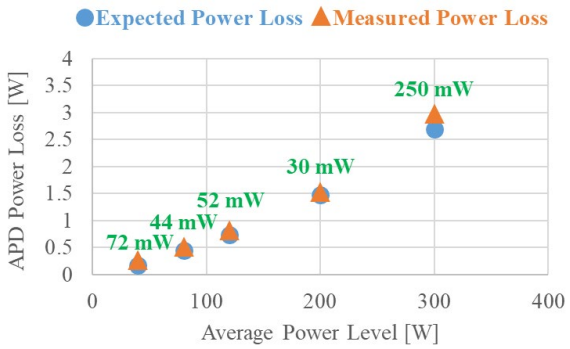
(b)

Fig. 5.12. Dynamic test results, (a) step-up transient from 120 W to 300 W, and (b) step-down transient from 120 W to 300 W.

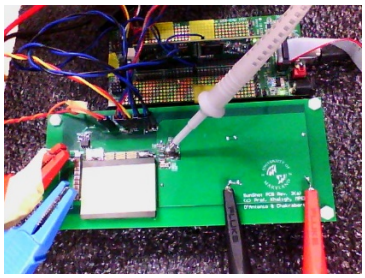
5.6.2. Efficiency

The efficiency of the APD was extracted at each of the CEC power levels corresponding to a maximum input power of 400 W. To experimentally extract the

efficiency of the APD, the circuit in Fig. 5.8 was employed, where the power loss in the APD was calculated by measuring the difference between the input power at the DC supply and the output power at the load resistor using a PA3000 power analyzer. The results of the efficiency analysis are shown in Fig. 5.13(a). It is clear that the efficiency model is able to accurately predict the loss performance of the converter (where the data labels indicate the loss difference between expected loss and measured loss in [mW]), validating the loss model used in the multi-objective optimization analysis. Thermal measurements are also provided for the 300 W operating point in Fig. 5.13(b-c) extracted with the FLIR E6 thermal camera, where it is shown that the switch node is the hottest point at a temperature of ~38 °C ($\Delta T \approx 14$ °C).



(a)



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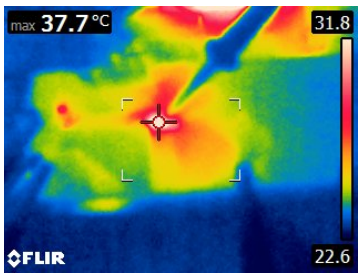


(c)

Fig. 5.13. Experimental results of the APD (a) efficiency at the CEC operating points, and (b-c) visible and infrared spectrum images at the 300 W operating point.

5.6.3. Integrated testing

The full-circuit closed-loop control system combining the main-circuit control in Fig. 3.12 with the APD control in Fig. 5.8 is evaluated in the hardware for a resistive load. The only difference between the APD control implementation in Fig. 5.8 versus the considered approach is that the APD current reference was derived from a single 120 Hz PR filter on the sensed input current as opposed to a BPF on the inverter-side current. The experimental hardware setup is shown in Fig. 5.14, where the CCM-based APD is utilized alongside the main-circuit with the T_4 transformer, and the supply input current was measured using an independent PCB. All of the sensed signals and control implementations were performed on a single TMS320F28335 control card. In this test, the main-circuit was implemented in the fully open-loop control configuration, while the closed-loop APD current and voltage loops were both active.

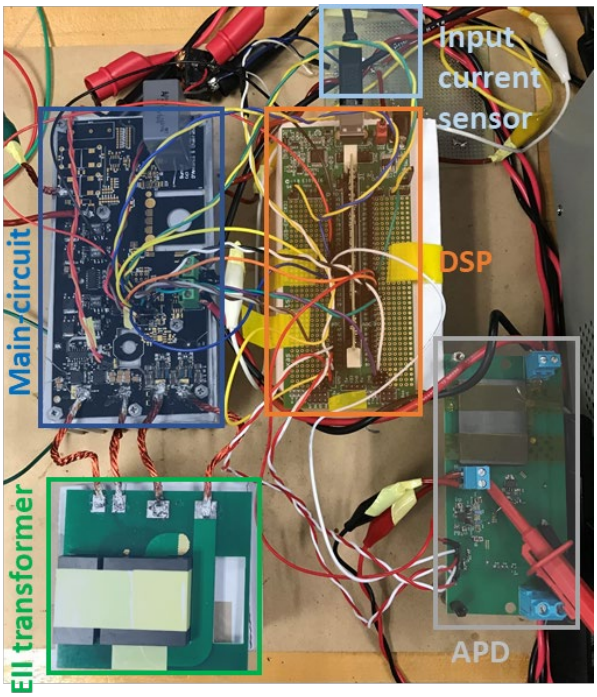
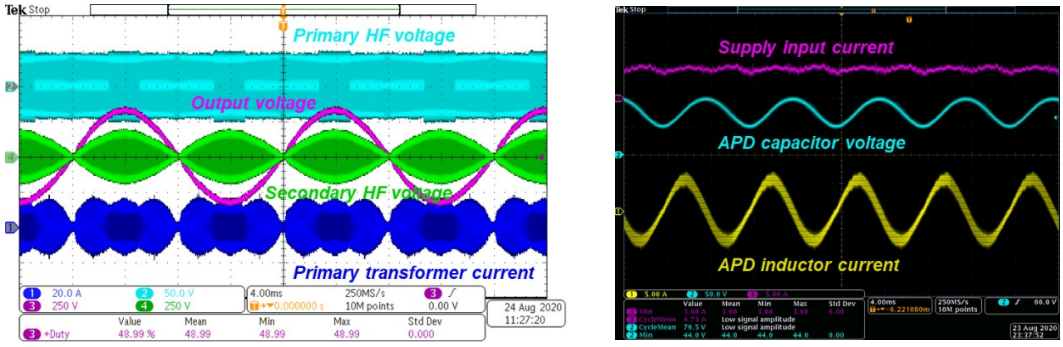


Fig. 5.14. Hardware setup utilized for integrated closed-loop testing with the rev. 2 main-circuit, T_4 transformer, and the CCM APD.

The results of the integrated testing experiment at the 200 W power level are shown in Fig. 5.15, where the main-circuit results in Fig. 5.15(a) are consistent with the previously shown open-loop results in Fig. 3.17, though the considered transformer is different (again validating the DC-AC modulation optimization procedure). Furthermore, Fig. 5.15(b) demonstrates the APD voltage and current signals, of which the current is very sinusoidal and the minimum capacitor voltage is near 45 V. The supply input current is also shown in Fig. 5.15(b), where the 120 Hz ripple is almost completely removed, yet some additional 240 Hz ripple remains. This remaining ripple can be negated through the use of an additional parallel 240 Hz PR controller in additional to the 120 Hz filter. Nevertheless, the proposed collaborative control method is validated.



(a) (b)

Fig. 5.15. Integrated testing experimental waveforms for (a) main-circuit (primary-side voltage, secondary-side voltage, transformer current, and output voltage), and (b) APD (capacitor voltage, inductor current, and system input current).

5.7. Summary

This chapter has developed a multi-objective optimization procedure for the APD circuit component selection, and development of the closed-loop control implementation of the optimal hardware. First, the CCM-based APD principle of operation was developed in both the low-frequency and high-frequency regimes. This analysis was then leveraged in the development of an analytical efficiency model for the converter. A multi-objective optimization procedure was developed to trade-off the APD efficiency, power density, and cost, across a wide range of configurations consisting of different devices, inductors, capacitors, and control variables. A hardware prototype was then built and tested, considering the optimal design configuration from the multi-objective analyses, to validate the efficiency model and demonstrate circuit performance in both steady-state and dynamic closed-loop control operation. The chapter concluded by demonstrating the integrated control performance considering both the main-circuit and APD, where the ripple in the input current of the DC source was mitigated by the APD control. Future work will focus on the analysis of other APD

control approaches, topologies, and generally microinverter circuits with integrated APD actions.

Chapter 6. Conclusion and future work

This dissertation has presented the motivation, development, and testing of a next generation microinverter, which is realized with an isolated, single-stage, DAB-based topology, achieving superior gravimetric power density, volumetric power density, cost, efficiency, and reliability, compared to the state-of-the-art. A summary of the contributions and major conclusions include the following:

- A more accurate steady-state modeling procedure was developed for the DAB circuit, predicting circuit-level performance even at high switching frequencies. The proposed analysis incorporates the device finite rise- and fall-times into the traditional frequency-domain circuit modeling, in an iterative algorithm. The predicted circuit performance was demonstrated to match both detailed circuit simulations in 3D FEA simulations, as well as experimental results, whereas ideal modeling schemes significantly mispredicted circuit behavior. This contribution furthered both the fundamental understanding of the DAB converter operated at high switching frequency.
- A design optimization routine was developed for parametric analysis of the main-circuit transformer turns ratio and leakage inductance, to facilitate low conduction loss contribution to the CEC efficiency. In this analysis, the conduction loss factor (CLF) was derived, in which it was shown that the optimal leakage inductance selection is purely a function of the turns ratio and the considered control principle. The CLF results were then extended to enable comprehensive component and topological selection for the main-circuit

secondary-side. Specifically, four secondary-side topology variations were compared considering a wide device database consisting of both Si and GaN devices in a multi-objective analysis of footprint area, efficiency drop, and cost. Clear trade-offs between four unique secondary-side converter architectures and three unique device technology combinations were presented, of which the optimal selection in a cost-sensitive application was shown to be the indirect half-bridge with GaN devices on the primary and Si devices on the secondary. The analytical approach established a systematic design process for the main-circuit, which could generally be applied to any similar application of the proposed topology, and identified key tradeoffs between various topological selections and current state-of-the-art devices.

- The control scheme for the main-circuit in DC-AC operation was developed based on the accurate circuit modeling in the first contribution. In particular, the accurate circuit modeling facilitated the removal of the output current sensor in the microinverter control architecture, enabling cost reduction in the circuit. As opposed to a closed-loop approach, the implemented control algorithm delivers the modulation parameters to the system according to 3D look-up-tables (LUTs) for each control variable, functions of the input voltage output voltage, and reference current. Importantly, the dynamic value of the control variable is equal to the trilinear interpolated value based on the aforementioned sensed and reference input values. The control algorithm was validated in a maximum power point tracking scheme in simulation, as well as

in a steady-state experimental test setup with a measured efficiency of 96.7% and an output current THD less than 3%.

- A novel EII transformer design was proposed that exhibits improved design characteristics over similar state-of-the-art leakage integrated transformer designs. Namely, these design advantages include a planar-based structure with three core pieces, and windings embedded into the circuit printed circuit board, for significant cost reductions as compared to wire-wound transformers. An analytical model was developed for the proposed transformer featuring asymmetrically distributed leakage inductances at the two ports, agreeing closely with simulation results for inductance predictions as well as both winding and core losses. A comprehensive multi-objective optimization routine was then developed to enable comparison of the proposed transformer against other planar-based transformers from the literature, in which the proposed design was most optimal from the loss perspective. Two of the optimally designed transformers were finally fabricated and tested experimentally, featuring high circuit efficiency and good thermal performance. The proposed transformer structure can be extended for advantages in any converter featuring integrated series leakage inductances, specifically in applications where asymmetric leakage is desired.
- A design optimization routine was developed for the active power decoupling (APD) circuit. The APD principle of operation was first established in both the high and low frequency regimes, and an accurate loss model was developed. This loss model was then leveraged alongside comprehensive cost and power

density functions in a multi-objective analysis enable component selection that achieves high power density, low efficiency drop, and low cost. The optimal APD circuit was experimentally validated in steady-state and dynamic testing scenarios, where the efficiency agreed closely with the theoretical predictions and the thermal performance of the devices was controlled. Finally, the APD was validated experimentally in an integrated testing scenario, where the main-circuit and APD controls work together to achieve high performance DC-to-AC power conversion.

Future work in this largely is focused on extensions of the technologies that have been proposed in this dissertation, and extended experimental results of the microinverter in field conditions. First, the microinverter prototype will be verified with a PV source and grid load to validate the proposed control principle in a maximum power point tracking environment, as was demonstrated in simulation. Furthermore, the microinverter will be validated in a wide variety of grid conditions, where additional smart grid control functionality must be incorporated. Nevertheless, the proposed open-loop control approach will remain unchanged; only the implementation of reactive current control as a function of the grid voltage, or limitation of active power transfer as a function of the grid frequency, will need to be implemented. Second, an extension of the proposed EII transformer has been introduced and should be optimized in a similar fashion to what was shown in Chapter 4. The proposed extension inherits an air-gap along the magnetizing flux path to minimize flux density within the core, supporting the transformer to be implemented in a smaller volume. However, at the cost of

minimizing volume, the magnetizing inductance will reduce while additional AC resistance effects could be generated, which may increase conductions losses and the total losses in the transformer. Finally, the future of power electronics aiming to increase power density as much as possible may necessitate the use of converter topologies featuring integrated power decoupling. The analysis of a family of these converters has been introduced and simulated, though the simulation should be validated in hardware, and systematic design and control principles need to be developed.

Appendices:

A. Microinverter and CEC efficiency

In PV microinverter applications, the California Energy Commission (CEC) efficiency is used to benchmark the circuit's efficiency performance. It is determined as a weighted sum of the circuit efficiency at various operating points,

$$\eta_{CEC} = \sum_{i=1}^{6} C_i \eta_{P_i} \tag{A.1}$$

where the weighting coefficients are C = [0.04, 0.05, 0.12, 0.21, 0.53, 0.05], the power levels of interest are P = [10%, 20%, 30%, 50%, 75%, 100%]$P_{av,max}$ [38], and $P_{av,max}$ corresponds to the maximum operating power level of the microinverter. It is clear that the microinverter CEC efficiency is weighted more towards the operating efficiency at the 50% and 75% power levels (since a typical PV module operates most frequently in this power level range), and hence the parametric design should be tailored accordingly.

For the proposed microinverter structure, consisting of an active power decoupler (APD) in parallel to the main-circuit inverter, the circuit losses at a given power level can be defined by the sum of the APD and main-circuit losses. Therefore, the converter CEC efficiency can be broken down by loss location,

$$\eta_{CEC} = \sum_{i=1}^{6} C_i \left[1 - \frac{L_{APD,i} + L_{MC,i}}{P_i}\right] = \sum_{i=1}^{6} C_i \left[1 - \eta_{APD,drop,i} - \eta_{MC,drop,i}\right] \tag{A.2}$$

where $L_{APD,i}$ and $L_{MC,i}$ denote the line-cycle-averaged losses in the APD and main-circuit, respectively, at a given average power level P_i. In light of the proposed form,

analysis specifically of the CEC efficiency '*drop*', deemed $\eta_{z,drop,i}$ (where z = {APD, MC}), of various loss mechanisms can be isolated and exploited for minimization.

For the main-circuit, the CEC efficiency drop can be decomposed by each of the various loss mechanisms,

$$\eta_{MC,drop} = \sum_{i=1}^{6} C_i \left[\frac{L_{cond,s,i} + L_{sw,s,i} + L_{cond,t,i} + L_{core,t,i}}{P_i} \right] \tag{A.3}$$

shown to consist of losses in the switches (conduction and switching) and losses in the transformer (conduction and core). Other main-circuit losses, including capacitor ESR losses and device driving loss are typically quite small relative to the other losses and hence were not considered. In this dissertation, the efficiency optimization strategy targets decoupled loss analysis, whereby the switch-related losses are minimized in Chapter 3, and the transformer-related losses are minimized in Chapter 4.

For the APD, the CEC efficiency drop can again be expanded to isolate individual loss mechanisms,

$$\eta_{APD,drop} = \sum_{i=1}^{6} C_i \left[\frac{L_{sw,i} + L_{ind,i} + L_{cap,i}}{P_i} \right] \tag{A.4}$$

Including losses in the switches (conduction and switching), inductor (conduction and core), and capacitor (ESR). In Chapter 5, minimization of the APD drop is utilized as one of the three principal objective functions to facilitate component selection.

B. Devices database in main-circuit component selection

In Section 3.4, a device database is considered to evaluate optimal device configurations for the various topological candidates. The device database is realized by a wide set of devices consisting of both Si and GaN technologies. The primary-side devices, with a maximum drain-source voltage between 80 V and 100 V, are shown in Fig. B.1(a). On the other hand, the secondary-side devices, with a maximum drain-source voltage between 600 V and 650 V, are shown in Fig. B.1(b). In each case, a value of 1 in the Si column indicated the device is based on Si technologies, whereas a value of 0 indicates the device is based on GaN. Additionally, the device maximum drain-source voltage, drain current, drain-source resistance, cost, and package dimensions were all stored. In particular, costs were based on distributor cost estimates extracted from trustedparts.com at a quantity of 1,000. While the project targets bulk manufacturing, the device costs were largely all available at a maximum quantity of 1,000, enabling a closer to one-to-one comparison.

For the secondary-side devices, two additional columns are present, namely "int. GD" and "Coss hysteresis". First, "int. GD" indicates certain GaN devices that have the gate driver integrated into the same package as the device [107]. Second, "Coss hysteresis" indicates Si devices in which losses still occur even in ZVS conditions due to an inherent charge versus voltage hysteresis behavior [109]-[110]. While these devices were considered initially in the project, and the final prototype secondary-side device exhibits this non-ideality (the effect was unknown until later in the research), the final results presented in Section 3.4.5 enable an improved device selection for future improvements in the design.

Name	Si	Vds,max	Id,max	Rds,on	Cost	L	W
EPC2065	0.00	80.00	60.00	2.70	1.85	3.47	1.92
EPC2029	0.00	80.00	48.00	2.50	3.84	4.57	2.57
EPC2021	0.00	80.00	90.00	1.80	4.53	6.02	2.27
EPC2001C	0.00	100.00	36.00	5.60	2.48	4.08	1.60
EPC2204	0.00	100.00	29.00	4.40	1.23	2.47	1.47
EPC2053	0.00	100.00	48.00	3.10	1.76	3.47	1.92
EPC2032	0.00	100.00	48.00	3.00	3.92	4.57	2.57
EPC2022	0.00	100.00	90.00	2.40	4.62	6.02	2.27
EPC2218	0.00	100.00	90.00	2.40	2.39	3.47	1.92
BSC040N08NS5ATMA1	1.00	80.00	100.00	3.40	0.90	4.80	5.70
IRF100S201	1.00	100.00	192.00	3.50	1.20	9.75	12.20
IRFS4010TRL7PP	1.00	100.00	190.00	3.30	1.74	9.75	12.20
BSC040N10NS5SCATMA1	1.00	100.00	140.00	3.40	1.64	4.95	5.95
IPD053N08N3GATMA1	1.00	80.00	90.00	4.40	1.09	5.97	6.40
BSC052N08NS5ATMA1	1.00	80.00	95.00	4.40	1.12	4.80	5.70
STH240N10F7-6	1.00	100.00	180.00	2.00	1.49	10.00	15.30
IPD90N08S405ATMA1	1.00	80.00	90.00	4.50	0.82	5.97	6.40
IPB049N08N5ATMA1	1.00	80.00	90.00	4.30	0.96	9.75	12.20
IPD050N10N5ATMA1	1.00	100.00	80.00	4.30	1.27	5.97	6.40
IAUT150N10S5N035ATMA1	1.00	100.00	150.00	3.70	1.57	9.80	11.68
BSC035N10NS5ATMA1	1.00	100.00	100.00	2.90	1.68	4.80	5.70
BSC057N08NS3GATMA1	1.00	80.00	100.00	4.70	0.66	4.95	5.95
STL120N8F7	1.00	80.00	120.00	4.00	0.74	5.00	5.95
BSC034N10LS5ATMA1	1.00	100.00	100.00	2.80	2.00	4.80	5.70
IPB042N10N3GATMA1	1.00	100.00	100.00	3.60	2.00	9.75	12.20
BSC050N10NS5ATMA1	1.00	100.00	100.00	4.30	1.60	4.80	5.70
IAUS165N08S5N029ATMA1	1.00	80.00	165.00	2.40	2.14	9.80	11.68
IPB027N10N5ATMA1	1.00	100.00	120.00	2.40	2.45	9.75	12.20

(a)

Name	Si	Int. GD	Vds,max	Id,max	Rds,on	Cost	L	W	Coss hysteresis
GS-065-008-1-L	0	0	650	8	225	2.89	5	6	0
GS-065-011-1-L	0	0	650	11	150	3.6	5	6	0
GS66504B	0	0	650	15	100	6.52	5	6.56	0
NV6115	0	1	650	8	170	1.98	5	6	0
NV6117	0	1	650	12	120	3.26	5	6	0
NV6125	0	1	650	8	175	1.98	8.7	6.7	0
NV6127	0	1	650	12	125	3.26	8.7	6.7	0
LMG3410R150	0	1	600	17	150	6	7.6	7.6	0
IPL60R105P7AUMA1	1	0	600	33.00	85.00	2.39	7.9	7.9	1
STB34N65M5	1	0	600	28.00	90.00	2.34	9.75	12.2	1
IPB60R120P7ATMA1	1	0	600	26.00	100.00	1.64	9.75	12.2	1
IPL60R125P7AUMA1	1	0	600	27.00	104.00	1.62	7.9	7.9	1
STB33N60DM6	1	0	600	25.00	115.00	2.16	9.75	12.2	0
STL33N60M2	1	0	600	22.00	115.00	1.78	7.9	7.9	0
STB28N60M2	1	0	600	22.00	135.00	1.37	9.75	12.2	0
STB28N60DM2	1	0	600	21.00	130.00	1.52	9.75	12.2	0
IPD60R180P7SAUMA1	1	0	600	18.00	145.00	0.72	5.97	6.4	1
IPL60R185P7AUMA1	1	0	600	19.00	149.00	1.38	7.9	7.9	1
STB24N60M2	1	0	600	18.00	168.00	1.03	9.75	12.2	0
IPL65R195C7AUMA1	1	0	600	12.00	173.00	1.48	7.9	7.9	1
STL24N60M2	1	0	600	18.00	186.00	1.37	7.9	7.9	0
STL26N60DM6	1	0	600	15.00	175.00	1.5	7.9	7.9	0
STD18N65M5	1	0	600	15.00	198.00	1.1	5.97	6.4	1
IPD65R225C7ATMA1	1	0	600	11.00	199.00	0.8	5.97	6.4	1
STB22N60M6	1	0	600	15.00	196.00	1.22	9.75	12.2	0
STL18N65M5	1	0	600	15.00	215.00	1.14	5	5.95	1
IPD60R280P7SAUMA1	1	0	600	12.00	214.00	0.48	5.97	6.4	1
IPL60R285P7AUMA1	1	0	600	13.00	218.00	0.91	7.9	7.9	1
STB18N60DM2	1	0	600	12.00	260.00	1.02	9.75	12.2	0
STD16N65M5	1	0	600	12.00	230.00	1.15	5.97	6.4	1

(b)

Fig. B.1. Main-circuit device database, (a) primary-side devices, and (b) secondary-side devices.

C. SOGI-based DQ-PLL

One of the fundamental building blocks to inverter operation is the phase lock loop (PLL). In the proposed operating case, the PLL is implemented in the direct-quadrature (DQ) domain, and can be described by the block diagram in Fig. C.1. The implementation of a DQ-PLL is slightly different for a single-phase system, compared to traditional three-phase systems, as the imaginary q-axis does not exist and hence needs to be created. Nevertheless, orthogonal signal generation (OSG) is made feasible for single-phase systems with various approaches, of which the second-order generalized integrator (SOGI) is considered [105]. The SOGI enables creation of the orthogonal V_α and V_β components, which are passed through an $\alpha\beta$-DQ transformation block via the Park transformation,

$$V_d = V_\alpha \cos(\theta_g) + V_\beta \sin(\theta_g) \tag{C.1}$$

$$V_q = -V_\alpha \sin(\theta_g) + V_\beta \cos(\theta_g) \cdot \tag{C.2}$$

PLL operation is hence achieved through the use of a PI controller, used to control the q-axis voltage component to zero over time. The output of the PI controller is then summed with a feed-forward nominal angular frequency (in this case $2\pi \cdot 60$ Hz), where the output of the summation defines the grid angular frequency at any time. Finally, wrapped integration (from 0 to 2π) of the frequency yields the instantaneous grid angle.

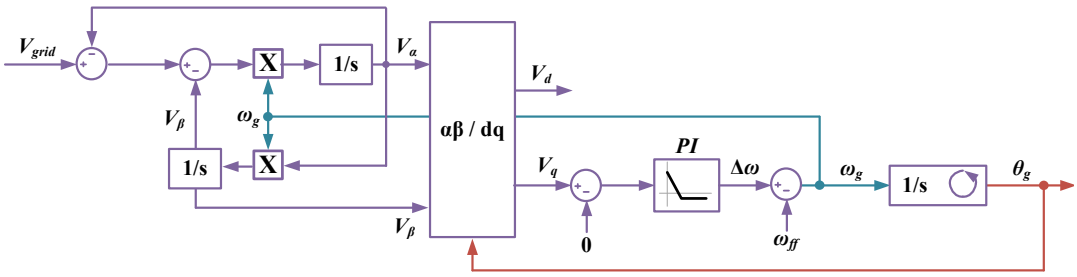


Fig. C.1. Block diagram of the single-phase DQ-PLL.

D. Low cost unfolder gate driver

The schematic of a single-output unfolder gate drive circuit is shown in Fig. D.1. On the primary-side there is a series capacitor that is used to block the DC component of the high frequency (> 100 kHz) drive signal, to obtain a zero-average AC voltage across the transformer. The transformer-applied AC voltage is stepped up by the transformer and half-wave-rectified by the diode on the secondary-side. Importantly, this rectification allows only the positive voltage to pass through and be applied across the output capacitor. The final RC elements on the secondary-side are used for low-pass filtering as the device is switched at 60 Hz, and not high-frequency. The state of the switch is then controlled by the optocoupler with an inverse relationship. When the optocoupler is *ON*, the gate-source is shorted by the optocoupler series resistor turning the switch *OFF*. Conversely, when the optocoupler is turned *OFF,* the switch is *ON*.

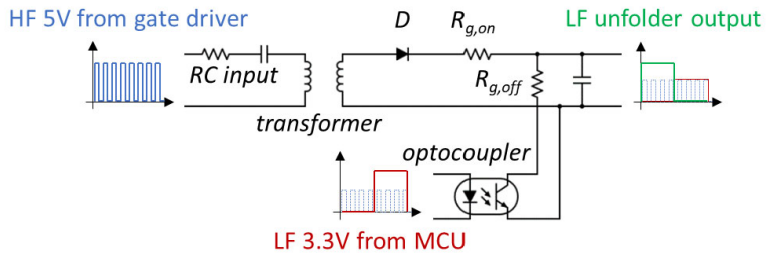


Fig. D.1. Single unfolder device gate driver circuit schematic.

In some designs, of which one is highlighted in Fig. D.2, the unfolder gate driver can be realized by using four individual gate drive transformers to step-up and provide isolation to the primary-referred drive signal. However, this four transformer design is not cost-effective due to the high price of the gate drive transformers, and the required footprint area is about 17 cm^2.

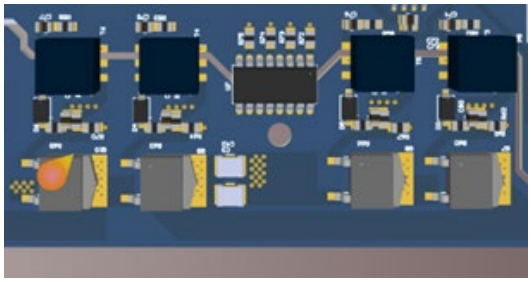
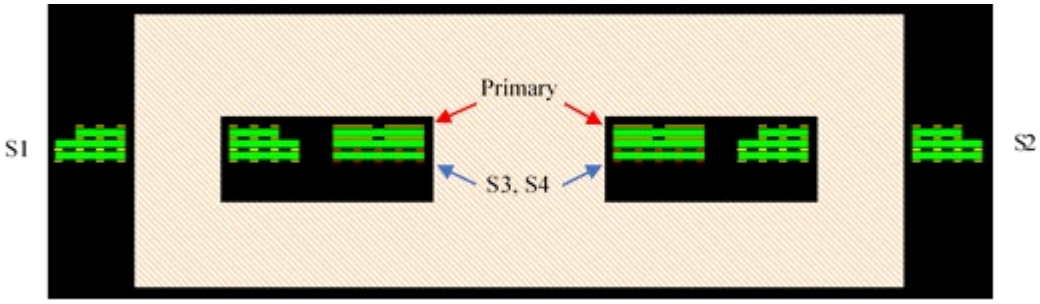


Fig. D.2. Unfolder PCB layout considering four individual gate drive transformers.

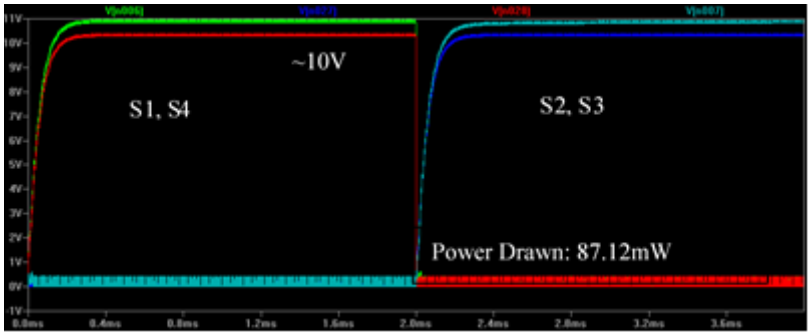
To reduce the cost and area of the unfolder gate driver, the four transformers could be integrated and realized by a single planar transformer. The inputs of each of the four transformers is the same, hence making it possible to combine all primaries together with a single input. Furthermore, the bottom switches of the unfolder bridge can be driven by the same transformer terminal because they share the same source terminal. One of the principal challenges in this design though is to fit the four windings into a single four-layer PCB with realistic limitations of minimum trace width and trace

spacing. In order to reduce the required turns ratio (and hence the total number of secondary-side turns), inherent gain can be generated by using a drive signal with a duty ratio below 50%. The peak of the transformer-applied voltage can be calculated as $(1 - D)V_{in,}$ where D is the duty ratio and V_{in} is the peak voltage of the input drive signal. As opposed to using a duty ratio of 50% that requires a turns ratio of four to step-up a 5 V input to 10 V output, using a 15% duty ratio and a turns ratio of ~2.35 is preferable as the number of secondary-side turns is reduced nearly by a factor of two. The latter design was pursued with the E18/4/10-3C97 core from Ferroxcube.

To fit all four windings on the 4-layer PCB, the winding design in Fig. D.3(a) is used. In the design, the primary and S_3/S_4 transformer terminals are placed on the central leg. The S_1 and S_2 terminals are then wound along the outer legs of the core, with an increased number of turns than S_3/S_4 due to the reduced flux density in the outer legs compared to the center leg. While this approach helps to fit the four windings, it also reduces the parasitic inter-winding capacitance that would exist if all four windings were placed on the center leg with complete overlap area. The transformer design was simulated in Ansys Maxwell 3D, and the inductance and AC resistance values obtained were input into a detailed LTspice model of the gate driver. The results of the simulation are shown in Fig. D.3(b). It is clear from the simulation that the gate driver functions properly, and has a low power consumption of less than 100 mW.



(a)



(b)

Fig. D.3. Improved unfolder gate drive transformer, (a) cross-section winding view, and (b) detailed LT-Spice simulation results.

Comparative results of the proposed planar design versus the previous design from perspectives of cost and area are shown in Table D.1. It is evident that the proposed planar design brings advantages in both transformer footprint area and cost. The cost reductions are particularly significant, and should reduce even further considering alternate component sourcing and proper high volume quotations.

Table D.1. Comparison between the previous and proposed unfolder gate drive transformer.

	Current Design (DA2320)	Planar Design (ER18/3.2/10)
Gate Transformer Area	350.25mm^2	213.02mm^2
Transformer Cost	$3.48	$1.13

E. Shell transformer modeling

The shell transformer and its associated reluctance diagram is shown in Fig. 4.6(b). Expressions of flux in each leg, and the magnetizing and leakage inductance have been derived previously in [59]. The key flux equations are summarized by,

$$\phi_L = \frac{N_p I_p(\mathcal{R}_1 + \mathcal{R}_2) - N_s I_s \mathcal{R}_2}{\mathcal{R}_1(\mathcal{R}_1 + 2\mathcal{R}_2)} \tag{E.1}$$

$$\phi_M = \frac{N_p I_p - N_s I_s}{\mathcal{R}_1 + 2\mathcal{R}_2} \tag{E.2}$$

$$\phi_R = \frac{N_p I_p \mathcal{R}_2 - N_s I_s(\mathcal{R}_1 + \mathcal{R}_2)}{\mathcal{R}_1(\mathcal{R}_1 + 2\mathcal{R}_2)} \tag{E.3}$$

where N_p and N_s are the number of primary- and secondary-side turns. Furthermore, the key inductance equations are summarized by,

$$L_m^{\gamma} = \frac{N_p N_s \mathcal{R}_2}{\mathcal{R}_1(\mathcal{R}_1 + 2\mathcal{R}_2)} T(\gamma) \tag{E.4}$$

$$L_{lk,p} = L_{lk,s} = \frac{N_p^2 \mathcal{R}_1}{\mathcal{R}_1(\mathcal{R}_1 + 2\mathcal{R}_2)}. \tag{E.5}$$

F. ACL transformer modeling

The ACL transformer and its associated reluctance diagram is shown in Fig. 4.6(c). Expressions of the flux in each leg, and the magnetizing and leakage inductance have been derived previously in [60] for the unity turns ratio case, but the more generic equations are presented here. The key flux equations are summarized by,

$$\phi_L = \frac{N_{p1}I_p(\mathcal{R}_1+\mathcal{R}_2)+N_{p2}I_p\mathcal{R}_2}{\mathcal{R}_1(\mathcal{R}_1+2\mathcal{R}_2)} - \frac{N_{s1}I_s(\mathcal{R}_1+\mathcal{R}_2)+N_{s2}I_s\mathcal{R}_2}{\mathcal{R}_1(\mathcal{R}_1+2\mathcal{R}_2)} \tag{F.1}$$

$$\phi_M = \frac{(N_{p1}-N_{p2})I_p-(N_{s1}-N_{s2})I_s}{\mathcal{R}_1(\mathcal{R}_1+2\mathcal{R}_2)} \tag{F.2}$$

$$\phi_R = \frac{N_{p1}I_p\mathcal{R}_2+N_{p2}I_p(\mathcal{R}_1+\mathcal{R}_2)}{\mathcal{R}_1(\mathcal{R}_1+2\mathcal{R}_2)} - \frac{N_{s1}I_s\mathcal{R}_2+N_{s2}I_s(\mathcal{R}_1+\mathcal{R}_2)}{\mathcal{R}_1(\mathcal{R}_1+2\mathcal{R}_2)} \tag{F.3}$$

where N_{p1} and N_{s1} are the number of primary- and secondary-side turns on the left-leg, and N_{p2} and N_{s2} are the number of primary- and secondary-side turns on the right leg. Furthermore, the key inductance equations are summarized by,

$$L_m^{\gamma} = \frac{(N_{p1}N_{s1}+N_{p2}N_{s2})(\mathcal{R}_1+\mathcal{R}_2)+(N_{p1}N_{s2}+N_{p2}N_{s1})\mathcal{R}_2}{\mathcal{R}_1(\mathcal{R}_1+2\mathcal{R}_2)}T(\gamma) \tag{F.4}$$

$$L_{lk,p} = \frac{(N_{p1}N_{s2}-N_{p2}N_{s1})(N_{p1}-N_{p2})}{(\mathcal{R}_1+2\mathcal{R}_2)(N_{s1}+N_{s2})} \tag{F.5}$$

$$L_{lk,s} = \frac{(N_{p1}N_{s2}-N_{p2}N_{s1})(N_{s1}-N_{s2})}{(\mathcal{R}_1+2\mathcal{R}_2)(N_{p1}+N_{p2})}. \tag{F.6}$$

In the optimization analysis, the configuration considered was $\{N_{p1}, N_{p2}, N_{s1}, N_{s2}\} = \{2, 1, 4, 8\}$, which generates balanced inductances on the primary- and secondary-sides.

G. Transformer designs in conduction loss analysis

In developing the analytical framework regarding the DC-to-AC side resistance ratios in Chapter 4, three unique transformer designs were considered that realized a wide variation across the design space. These three designs were informed from the custom transformer multi-objective design analysis in Section 4.5.6. With reference to the custom Pareto front in Fig. 4.19, Transformer A is one of the bottom-right corner designs with a PCF of 1%, Transformer B is the finally selected design T_5, and Transformer C is the design in the upper-left corner. Key design specifications related

to conduction losses are highlighted in Table G.1, where clearly the designs have unique values geometric variables as well as r_{gw}.

Table G.1. Transformer design parameters considered for conduction loss analyses.

Tr.	l_{side} [mm]	d_{core} [mm]	w_{wind} [mm]	l_{gap} [mm]	r_{gw} [%]
A	5	38.6	23.1	1.7	7.2
B	10.5	49.9	16.2	2.4	14.4
C	12.5	49.9	8.45	2	22.3

H. General EII transformer design guidelines

While the analysis in Section 4.5 leverages a genetic algorithm to perform multi-objective design optimization of the EII transformer geometry, standard design principles for the proposed transformer may also be beneficial for reduced design time. Optimal design of the proposed transformer comes down to the minimization of the total loss, of which there are core and conduction loss contributions. In the most general case, all six dimensions of the transformer are allowed to vary, and each of the six variables have an important impact to the two loss categories. First, design variables x_1, x_2, and x_4 are coupled: for a given value of x_4, reducing x_1 and x_2 will reduce the cross-section area of the core flux paths while widening the cross-section area of the windings (hence lower x_1 and x_2 may facilitate lower conduction losses while increasing the core losses). Second, increase in design variable x_5 will increase the cross section area of all core segments, while lengthening the windings (again demonstrating a tradeoff between core and conduction losses). Finally, design variables x_3 and x_6 are also coupled to a degree: for a given value of x_6, increases in x_3 will increase the cross-section area of the flux path on the top and bottom of the core geometry, however, the

air gap will then approach the secondary-side windings. This would increase the DC-to-AC resistance ratio of the windings below the gap as described at length in Section 4.4.3. In conclusion, from a qualitative perspective, it is clear that each of the design variables represent tradeoffs between core and conduction losses.

To begin, it almost always desirable to make x_3 close (if not equal) to the upper bound of what is tolerated, in order to minimize the flux density in the upper and lower portions of the core. Depending on the design of the winding width, the parameter x_6 can then be selected such that the Sullivan ratio is equal to three. With the design of x_3 and x_6 clear, it is left to determine x_1, x_2, x_4 and x_5. A reasonable design consideration for x_1, x_2, and x_4 is to ensure that 50% of the core's width can be used for windings, while the other 50% is for the core legs, mathematically expressed as,

$$2x_1 + x_2 = \frac{1}{2}x_4 \tag{H.1}$$

To constrain the decision space associated with the previous equation, the two geometric constraints related to the power density are invoked,

$$x_4 + \frac{x_4 - 2x_1 - x_2}{2} = L_{tr,max} \tag{H.2}$$

$$x_5 + x_4 - 2x_1 - x_2 = D_{tr,max} \tag{H.3}$$

where for simplicity it is assumed that the transformer occupies the maximum allowable footprint area. As such, there is a system of three equations with four unknowns. To reduce one of the free variables, it can be assumed that $x_2 = \frac{1}{2}x_1$, as the width of the leakage leg is not too critical due to the air gap. Therefore, the following matrix (of which A is full rank and hence invertible) can be solved,

$$\begin{bmatrix} 2 & -1/2 & 0 \\ -1 & 3/2 & 0 \\ -2 & 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_4 \\ x_5 \end{bmatrix} + \begin{bmatrix} 1 \\ -1/2 \\ -1 \end{bmatrix} x_2 = \begin{bmatrix} 0 \\ L_{tr,max} \\ D_{tr,max} \end{bmatrix} \quad \text{(H.4)}$$

In light of the discussion in Section 4.4.3, the secondary-side winding losses are highly sensitive to the core's distance from the winding gap. Therefore, the following argument can be made regarding design parameters x_3 and x_6. Namely,

$$r_S = \frac{\left(x_4 - 2x_1 - x(2)\right)/2}{x_6 - 2x_3 - 2.5} = 3 \quad \text{(H.5)}$$

With the proposed design constraints for $L_{tr,max}$ and $D_{tr,max}$ indicated in Table 4.4, the design in Table H.1 is realized. Interestingly, the PCF of the example considered design is 0.33% and the WLF is 0.5%, and hence achieves a total loss factor of 0.83% which is equal to the optimally selected design T_5 (though the design dimensions are unique). The proposed analysis may be beneficial in reducing the design time of the EII transformer, however it may not be always guaranteed that the proposed design rules generate as close to an optimal design.

Table H.1. Example EII design based on general design principles.

x_1	x_2	x_3	x_4	x_5	x_6
14 mm	7 mm	6 mm	70 mm	48 mm	20 mm

I. Permeability characterization

The effective permeability of an ungapped core combination is likely to differ from the expected relative permeability of a single core piece. Permeability variation is a result of two principle phenomenon: (1) material permeability tolerance, and (2) interface permeability reduction. In the first case, the permeability of a core material is typically only guaranteed within a certain range, in this case $\pm$20% for the 3F36 core

material [76]. In the second case, at the interface of two ideally ungapped core blocks, a small interface air-gap is practically unavoidable.

To characterize the effective permeability of the core, the following test can be performed. First, the core is assembled in the desired configuration. Next, basic inductance calibration is performed with a single set of windings of varying number of turns, *N*, placed along each of the core's legs. The resulting inductance data can then be curve-fit to the form,

$$L(N) = N^2 A_L = \frac{N^2}{\mathcal{R}_{tot}} \cdot \tag{I.1}$$

Analytical determination of the effective $\mathcal{R}_{tot}$ based on the winding configuration can hence be performed with reluctance modeling, and the effective value of μ_r can be found when $A_{L,pred}(\mu_r) = A_{L,exp}$.

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