ABSTRACT

Title of Dissertation: FAILURE MECHANISM INVESTIGATION FOR SILICON CARBIDE POWER DEVICES

Xiaohu Zhang, Doctor of Philosophy, 2006

Directed By: Associate Professor, Dr. Joseph B. Bernstein, Department of Mechanical Engineering

Silicon carbide (SiC), as one of the wide bandgap semiconductors, is a promising material for next-generation power devices due to its high critical electric field, high thermal conductivity, and high saturated electron drift velocity properties. Extensive studies have been focused their electrical characterizations. Failure mechanisms of SiC devices, however, have not been fully explored. In this work the failure mechanisms of SiC power devices, including Schottky diodes, power MOSFETs and IGBTs, are investigated.

The characteristics of SiC Schottky diodes have been investigated and simulated based on the drift-diffusion model. Interface state degradation has been identified as the mechanism responsible for the non-catastrophic failure happened in Schottky diode. Experimental and simulation results are provided to support this conclusion. Single-event burnout (SEB) and single-event gate rupture (SEGR) failure

mechanisms have been investigated for SiC power MOSFETS in details in this work since power MOSFETs have been used in very critical applications. The features of SiC power MOSFET SEB and SEGR failures have been simulated successfully and compared to those of Si power MOSFETs. The much better robustness of SiC power MOSFES against SEB failures has been demonstrated by the simulation results. At last the latch-up failure mechanism has been investigated for SiC IGBTs. Compared to Si IGBTs, the results show that SiC IGBTs have a stronger capability against the latch-up failure.

The design and application guideline for SiC power devices can be made base on the results obtained in this work.

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FAILURE MECHANISMS IN WIDEBAND SEMICONDUCTOR POWER DEVICES

By

Xiaohu Zhang

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Advisory Committee:
Professor Joseph B. Bernstein Chair/Advisor
Professor Martin Peckerar
Professor Mohammad Modarres
Professor Ali Mosleh
Professor Carol Smidts

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Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 Why SiC

Silicon carbide (SiC), as one of the wide bandgap semiconductors, is the promising material for next-generation power devices due to its wide bandgap, high critical electric field, high thermal conductivity, and high saturated electron drift velocity. SiC has many polytypes. Out of all kind of polytypes, 4H-SiC and 6H-SiC are the most used ones for electronic devices. Both polytypes have a hexagonal frame with a carbon atom situated at the center of a tetragon of Si atoms as shown in the Fig.1.1. (a). The difference between the polytypes is the stacking order between succeeding layers of carbon and silicon atoms. A unit cell of 4H-SiC with the CABA stack sequence is shown in Fig.1.1. (b) meanwhile a unit cell of 6H-SiC has a stack sequence CBABCA. This study is only focused on in 4H-SiC.

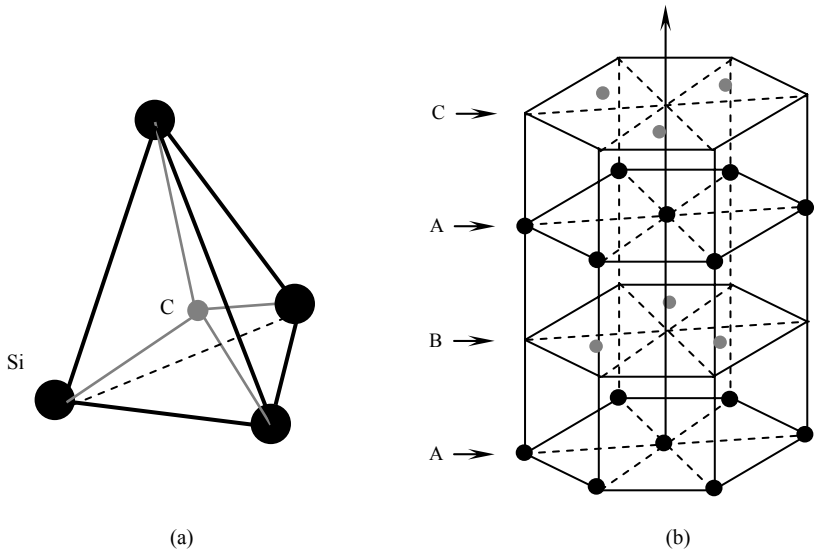


Fig.1. 1(a) A carbon atom situated above the center of a tetragon of Si atoms (b) A unit cell of 4H-SiC

The typical properties of 4H-SiC, 6H-SiC and Si are compared in Table 1.1 below.

Table 1. 1 The properties of 4H-SiC, 6H-SiC and Si

	4H-SiC	6H-SiC	Si
Bandgap (eV)	3.26	3.03	1.12
Critical Electric Field (V/cm)	2.2×10^6	2.4×10^6	2.5×10^5
Thermal Conductivity (W/cm·K@RT)	3.0-3.8	3.0-3.8	1.5
Saturated Electron Drift Velocity (cm/sec)	2.0×10^7	2.0×10^7	1.0×10^7

The high bandgap of SiC results in a very low intrinsic carrier concentration and negligible junction leakage currents. This allows high-temperature operation of SiC devices without excessive leakage current and avoiding thermal runaway.

The high critical electric field E_c of SiC enables drift layers that are 10 times smaller than those of Si for a given blocking voltage, thus reduces both the storage of minority carriers (Q_{rr}) and associated switching losses at a given switching frequency. One of applications of this feature is to use SiC Schottky diodes instead of traditional Si PiN diodes in the continuous conduction mode power factor correction circuits. A simple CCM-PFC circuit is shown in Fig.1.2.

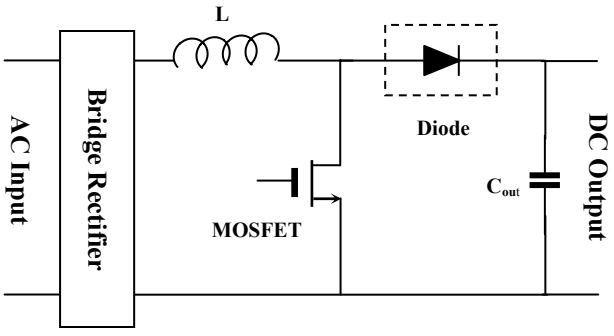


Fig.1. 2 A simple CCM PFC circuit

This circuit achieves near-unity power factor by chopping the full wave rectified input with a fast switch (MOSFET), and then stabilizing the resulting DC waveform using a capacitor. Traditionally a Si PiN diode is used in this circuit to prevent the current flow back from the capacitor. During the switching transient, a large current resulting from the large reverse recovery current of the Si PiN diode and the rectified input current rushes into the MOSFET. This large current is a big burden of the MOSFET switch, limiting the frequency and efficiency of the circuit.

However, due to the majority carrier transport property of SiC Schottky diode, it can offer very low reverse recovery switching loss in this PFC circuit while still keeping comparable on-state performance as conventional silicon rectifiers. In this case, only a small capacitive current flows through the MOSFET during its turn-off transient.

The high thermal conductivity makes SiC a better thermal conductor. Heat will flow more readily through SiC than Si materials. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amount of excess heat.

With the availability of high quality commercial 4H-SiC and 6H-SiC SiC wafers, it has become more and more practical to make SiC power devices such as Schottky diodes, power MOSFETs and IGBTs. However, research studies on SiC power devices have been mainly focused on the electrical characterizations of them.

Little attention has been paid to studying the failure mechanisms of SiC power devices. This dissertation attempts to conduct some typical failure mechanism investigation for SiC power devices and contribute in this research area. The most frequently used power devices, Schottky diodes, power MOSFETs and IGBTs have been chosen and studied in this work. The failure mechanisms of these SiC power devices have been investigated and compared with traditional Si power devices.

The outline of this dissertation is as follows. In this introduction chapter the general failure mechanisms of these power devices have been categorized and introduced. In chapter 2 the drift-diffusion model has been introduced in details since it is the basis of the simulations conduced in this work. In chapter 3 the DC characteristics of a SiC Schottky diode have been measured and simulated to verify the correctness of the physical models used for 4H SiC. A non-catastrophic failure mechanism has been investigated for the SiC Schottky diode. In chapter 4 the Single-event-burnout (SEB) and the Single-event-gate rupture failure mechanisms have been studied for SiC power MOSFETs. Investigating these two failure mechanisms is crucial since the failures triggered by them happen in very critical applications. In chapter 5 the latch-up failure mechanism has been investigated for SiC IGBTs. Finally the study conduced in this work has been summarized. We will begin by introducing the general failure mechanisms happened in power Devices.

1.2 Failure Mechanism of power devices

In this section the failure mechanisms of Schottky diodes, power MOSFETs and IGBT are introduced respectively.

1.2.1 Failure mechanism of Schottky diodes

A Schottky diode is typically made by a piece of metal layer and a piece of semiconductor material layer (n-type or p-type). The schematic cross-section of a Schottky diode is shown in Fig.1.3. As a majority carrier device, Schottky diodes have the primary advantages of very low forward voltage drop and near to zero switching time. These characteristics make them the ideal switching devices used extensively in the power supply industry. However, few complete reports about the failure mechanisms happened in Schottky diodes have been documented. Thus a summary of failure mechanisms of Schottky diodes is provided in this section which can be used for device design guideline.

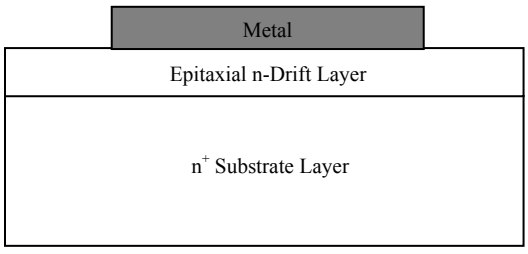


Fig.1. 3 The schematic cross-section of a Schottky diode

As the simplest semiconductor device, the failure mechanisms of Schottky diodes can be categorized into two groups: non-catastrophic and catastrophic. non-catastrophic failures happen when the characteristics of Schottky diodes degrade over time due to the non-catastrophic failure mechanism. The diode cannot perform as required after a certain amount of device lifetime. In contrast, catastrophic failure mechanisms result in failures happened suddenly in the Schottky diode during their normal operation. The two types of failure mechanisms are introduced respectively in the following sections.

1.2.1.1 Catastrophic failure mechanisms of Schottky diodes

Catastrophic failures of Schottky diode are one of major failures happened in field for Schottky diodes. Research efforts have been made to identify the failure mechanisms behind the failures. Lin *et al.* reported catastrophic failures of GaAs Schottky diodes in [1]. The failure analysis showed that the inside cracks were formed due to the release of high structure overstress caused by the high junction temperature within the device during its long time operation. When the cracks propagated into the Schottky contact region, it will cause the abrupt electrical change of the device and lead to a catastrophic failure. Catastrophic failures of GaAs Schottky diode was also investigated by Brandt *et al.* in [2]. In the designed tests, GaAs Schottky diodes were driven in a forward operation mode with a high current density. Hot spots or hot filaments were generated inside the bulk material because of the high local current density. Then catastrophic failure was observed in the

device with a destroyed GaAs layer. The failure mechanism was attributed to this thermal degradation inside the device.

Another type of catastrophic failure mechanism of Schottky diodes is known as diode avalanche breakdown. When the applied reverse voltage applied on the Schottky diodes, the electric field within the diode is so strong that thermally generated electrons and holes can get enough kinetic energy to knock on atoms and generate extra electron-hole pairs within the diode. With these newly generated electron-hole pairs, this process will continue and be amplified under the high electrical field. As a result, a dramatically increased reverse current will generate within device and destroy the device thermally over a certain time period.

1.2.1.2 Non-catastrophic failure mechanisms of Schottky diodes

Non-catastrophic failure happens in Schottky diodes. The characteristics of the Schottky diodes such as I-V characteristics can be seriously degraded during their normal operation. Lin *et al.* defined the non-catastrophic failure criteria for the tested GaAs Schottky diodes when any of three conditions is met: (1) the ideality factor η changes by 10%, (2) the series resistance R_s change by 20%, (3) the turn-on voltage V_0 (voltage where current is 1μA) change by more than 20% [1]. In the following accelerating tests they performed, non-catastrophic failures were recorded when the diode characteristics slowly degraded to the failure criteria. The SEM image of the non-catastrophically failed device showed no crack within the diode. Schubler *et al*,

conducted another reliability test on Schottky diodes under electrical pulse stress in [3]. I-V characteristic degradation of Schottky diodes was also observed. However the failure mechanisms responsible for these non-catastrophic failures in Schottky diode were not clear to the authors.

In this work, the interface state degradation between the metal and semiconductor layer is believed to be responsible for these non-catastrophic failures. Interface states were experimentally proved to be thermally active. The formation of interface traps in Au/InGaP Schottky diodes was reported in [4]. The interface states were generated during heat treatment. The origin of these interface states was attributed to the transformation of a simple phosphorus vacancy to antisite-related defect such as Ga_p, and In_p. Interface states generated during the annealing process in Ti/n-GaAs Schottky diode were also investigated in [5]. The interface states were attributed to the annealing processing which removed the passivation effect of the native oxide layer and reactivated these surface defects. Similar results were obtained for n-type 6H-SiC Schottky diodes in [6]. During annealing process significant reactivation of the passivated defects was shown to start at some temperature between 350 and 400 ^{0}C. Thus in this study the interface states is proposed to be responsible for these non-catastrophic failures of Schottky diodes. Detailed numerical simulations for proving this will be introduced in Chapter 3.

1.2.2 Failure mechanism of power MOSFETs

Power MOSFETs are the key components in power electronic circuits. They have been used extensively in all kinds of industry applications. A complete understanding of the failure mechanisms of power MOSFETs will help to provide guidelines for field applications and prevent failures.

Traditional lateral MOSFETs have the drain-to-source current confined to a thin planar volume of silicon lying parallel to the gate. The device conduction area and power handling capability, however, are limited by this geometry. Power MOSFETs solved this problem with a vertical conduction channel. The rating of power MOSFETs can reach to hundreds of voltages and hundreds of amperes with the greatly increased conduction area.

There are two main vertical gate structure designs for power MOSFETs: DMOS and VMOS. Fig.1.4 shows the vertical cross-section of a DMOS structure. The current path in the device is created by inverting the p-base region under the gate which is the same approach used for the lateral MOSFETs. N^+ source current flows underneath the gate area and vertically through the drain region. As majority carrier devices with gate control, Power MOSFETs have many advantages over traditional power bipolar transistors, such as very fast switching speed and simple gate-driven circuits.

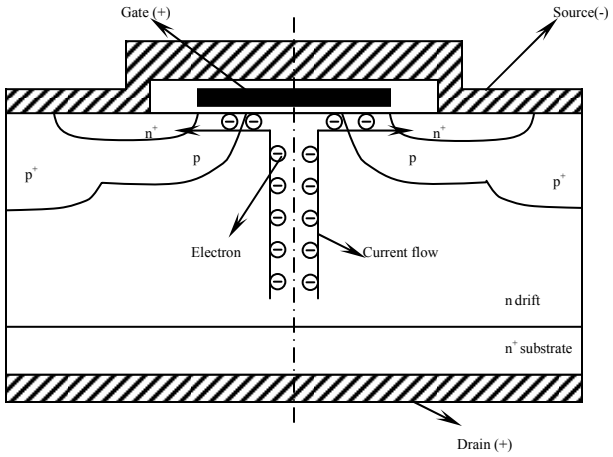


Fig.1. 4 Vertical DMOS Cross Section

The failure mechanisms of power MOSFETs are different from those of traditional lateral MOSFETs due to their special structures. For example, hot carrier degradation (HCD) is one of failure mechanisms of lateral MOSFETs, but is not an issue for power MOSFETs since the gate region and drain region of it are separated at the two ends of the device. Compared to the extensive study of failure mechanisms of lateral MOSFETs, a review of failure mechanisms of power MOSFETs is needed. The main failures of power MOSFETs can be categorized into two groups: gate oxide breakdown and the activation of parasitic structures inherent in power MOSFETs. The activation of parasitic structures of power MOSFET can be further divided into two categories: the activation of parasitic bipolar transistor (BJT) in power MOSFETs and the activation of parasitic diode in power MOSFETs. These failures can be triggered by different mechanisms when powers MOSFETs are used in different harsh environment, such as extreme transient stress or high radiation environment. The inherent parasitic bipolar and diode structure in power MOSFETs are introduced

in the next section followed by the discussion of the failure mechanisms of power MOSFETs.

1.2.2.1 Inherent parasitic structures in power MOSFET

Since the gate structure of power MOSFETs are similar to that of lateral MOSFETs, only the inherent parasitic structures of power MOSFET are addressed here. The inherent parasitic structures in power MOSFET include a parasitic bipolar transistor and a parasitic diode.

A parasitic *NPN* bipolar transistor inherent in a DMOS is shown on the left side of Fig.1.5. The source, p-region, and n drift region of this power MOSFET comprise the emitter, base and collector region of the parasitic bipolar transistor respectively. In normal operation of the power MOSFET, this parasitic bipolar transistor is always off since the source and p-region is connected by the same metallization layer that shorts the base-emitter junction of the bipolar transistor.

The parasitic body diode formed between the source and the drain is shown on the right side of Fig.1.5. The source acts as anode of the diode and the drain acts as cathode of the diode. This diode is usually reverse biased since the drain voltage is normally larger than the source voltage.

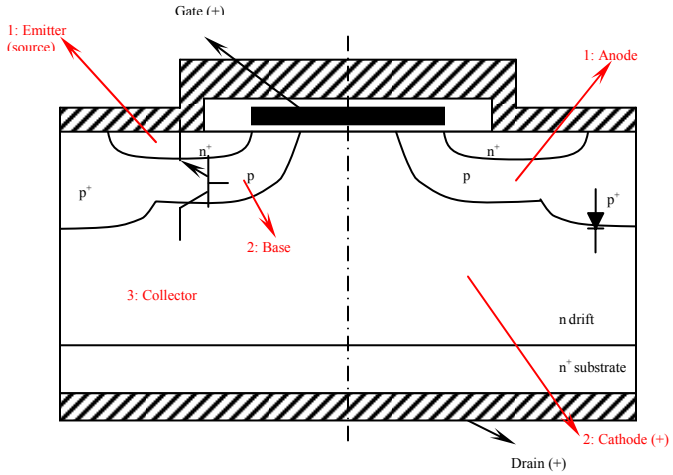


Fig.1. 5 Parasitic NPN transistor and diode inherent to DMOS

The parasitic BJT and diode introduced above are the weaknesses of power MOSFETs. Although those parasitic devices keep inactive under normal condition, failure can still occur when the turn-on of those devices is triggered under certain circumstances. The failure mechanisms of them will be introduced and summarized in the following.

1.2.2.2 Failure mechanisms in power MOSFETs

Gate Dielectric breakdown in power MOSFETs

Gate dielectric breakdown is inherent in MOS devices since the unique MOS gate structure is used to control the turn-on and turn-off of the devices. Two failure mechanisms have been identified for gate dielectric breakdown in power MOSFETs:

Time-dependent dielectric breakdown (TDDB) and Single-event-gate-rupture (SEGR).

Time Dependent Dielectric Breakdown (TDDB)

As the most common failure mechanism in MOSFETs, time dependent dielectric breakdown (TDDB) has been studied extensively. Generally speaking, Time-dependent dielectric breakdown (TDDB) means the destruction of gate dielectric layers over time. This breakdown is related to the defect accumulation within the dielectric material. The basic idea is that with the electric field stress over time, defects are built up in the SiO_2 gate. When the defect density reaches a critical level, a conduction path is formed. Abrupt increased gate current is observed and eventually the MOSFET lost its gate voltage controllability. Different mechanisms have been proposed to explain how the defected inside SiO_2 is created and accumulated. Among them the thermochemical model, the hydrogen model and the anode-hole-injection (AHI) model are widely accepted ones. The thermochemical model, also known as E model, assumes a direct correlation in existence between the electric field and the oxide degradation. The weak chemical bonds (Si-Si bonds) in SiO2 associated with oxygen vacancies experience heavy strains due to the high electric field applied across the oxide and some bonds may obtain enough thermal energy to break off and create defects. The hydrogen model states that a hydrogen atom will be kicked out from the SiO_2/Si interface when electron reaches the anode. This atomic hydrogen then will diffuse into the oxide bulk. When it encounters an oxide defect, presumably an oxygen vacancy, it can turn the defect into a trap that

contributes to breakdown. The anode-hole-injection (AHI) model proposes that the origin of the positive trapped charges in the oxide after stress is due to anode injection of holes. It should be pointed out that these models can only fit experimental data in a certain range of electric field. Great care should be taken in using them in field.

Single-event-gate-rupture (SEGR) in Power MOSFETs:

SEGR is another failure mechanism of oxide breakdown happened in power MOSFETs. Power MOSFETs are often used in space system because of their outstanding electrical characteristics. However they are vulnerable to SEGR failures when exposed to the radiation environment of space. The natural space contains high-energy protons and heavy ions as the existing of extensive radiation. When a heavy ion penetrates the gate region of a power MOFET while the drain is under positive bias (n-channel), the electron-hole pairs generated along the path of the ion start to separate as shown in Fig.1.6. The holes are driven toward the gate and the electrons flow toward the drain. A net positive charge accumulates in the silicon at the Si-SiO_2 interface as a result of this charge separation. The charge buildup results in a transient electric field increase upon the gate oxide. If the increased electric field exceeds the critical oxide breakdown field E_{cr}, oxide breakdown occurs and results in a permanent short circuit through the oxide. This failure mechanism has been studied extensively in the 90's. Different aspects about this failure mechanism has been reported in literature, including oxide thickness dependence, temperature dependence and ion threshold energy, etc [7]~[13].

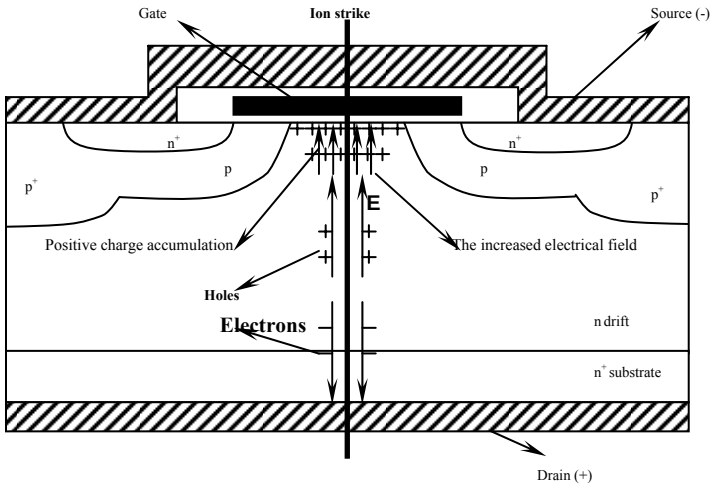


Fig.1. 6 SEGR of power MOSFET

Activation of parasitic bipolar transistor (BJT) in power MOSFETs

The parasitic BJT structure in a power MOSFET is shown in Fig.1.5. As we mentioned before the parasitic BJT is normally inactive since the base-emitter junction is shorted together. However the BJT can still be turned on under some circumstances, even though the base-emitter junction is shorted externally. This will cause the device to lose the gate control and result failures of power MOSFETs. Two types of mechanisms that can active the parasitic BJT in power MOSFETs were identified. One mechanism is activated during the turn-off of power MOSFETs. When a power MOSFET is turned off, the very high *dV/dt* or *dI/dt* can activate the parasitic BJT. The other mechanism is triggered when power MOSFET is used in a high radiation environment. The parasitic BJT can be turned on when a heavy ion strike on the power MOSFETs device.

Activation of parasitic BJT during the turn-off of power MOSFETs

In order to explain how the activation of parasitic BJT in power MOSFETs occurs, the equivalent circuit for an n-channel power MOSFET is shown in Fig.1.7 where a NPN parasitic bipolar transistor is included. C_{gd} and C_{gs} represent the parasitic capacitances between gate to drain and gate to source. C_{db} is another parasitic capacitance existing between drain and source. Z_{gs} is the gate-to-source impedance and R_{be} is the resistance along the source channel.

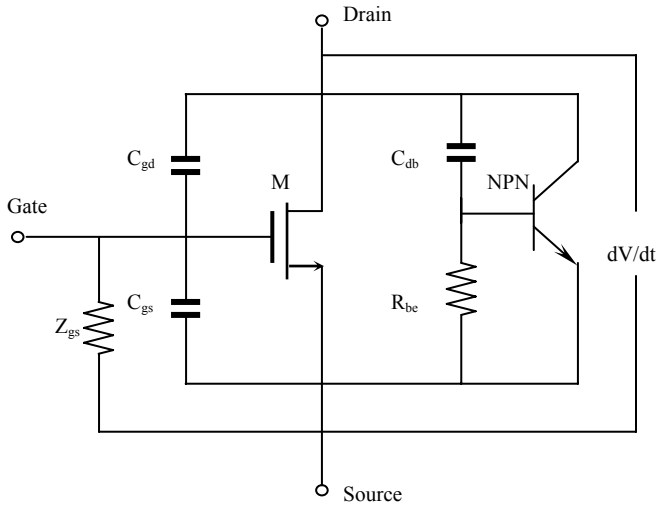


Fig.1. 7 Equivalent circuit of a power MOSFET

Failure can happen during the turn-off of a power MOSFET. A sudden increase in drain voltage (dV/dt) changes the voltage across capacitor C_{db}, a displacement current flows through resistor R_{be} when a power MOSFET is turning off. The current generates a voltage drop in the base-emitter junction. When $V_{be,}$ the voltage across the R_{be}, is increased to approximately 0.7V, the parasitic bipolar

transistor, shown in Fig.1.5 and Fig.1.7, is turned on. When the parasitic bipolar transistor is on, the device lose its gate control and the breakdown voltage of the device is reduced from BV_{CBO} to BV_{CEO} which is 50~ 60% of BV_{CBO}. If a drain voltage is larger than BV_{CEO} is supplied, the device falls into an avalanche breakdown. If the avalanche current is not limited externally, the device can be destroyed thermally.

Single-event-burnout (SEB) in Power MOSFETs

Similar to SEGR, SEB is also initiated when a heavy ion strike through a power MOSFET biased in the OFF state. As the heavy ion traverses the device, electron-hole pairs are generated along its track length and create transient currents in which holes flow up towards source via the lateral base region and electrons toward drain. This current leaking through the p-base region will generate a voltage drop in the base-emitter junction as shown in Fig.1.8. When the voltage drop is larger than a threshold value it will turn on the parasitic bipolar junction transistor inherent in power MOSFETs. Due to a regenerative feedback mechanism, high current and voltage will occur in the device channel and trigger the second breakdown of power MOSFET and destroy the device.

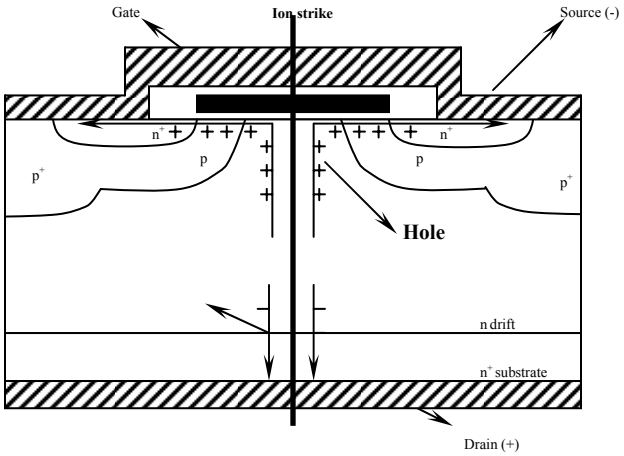


Fig.1. 8 SEB of power MOSFET

Parasitic diode avalanche breakdown in power MOSFETs

Avalanche breakdown can happens in the parasitic diode in power MOSFETs. As shown in Fig.1.5 the parasitic diode formed between the source and drain of the power MOSFETs. The source acts as the anode and the drain acts as the cathode. Since this diode is always under reverse biased, a sudden increased drain-source voltage can result in an avalanche breakdown in this diode.

As an example, a synchronous-rectified converter is constructed in Fig.1.9 to illustrate this failure mechanism. The power MOSFETs are used as synchronous rectifiers in this half-bridge switching circuit with an inductive load. In this circuit, the high-side power MOSFET (M_1) is first turned on to load the inductor L to the desired current level first. Then M_1 is turned off to force the inductor current to freewheel through the body-diode of the low side MOSFET (M_2). Finally M_1 is

turned on again to turn the diode off. However after the M_1 is turned off, a very high voltage can be created in the inductance which is much larger than V_{in}. This voltage is completely applied on M_2. The abnormal high voltage can cause avalanche breakdown in the Mdiode within M_2.

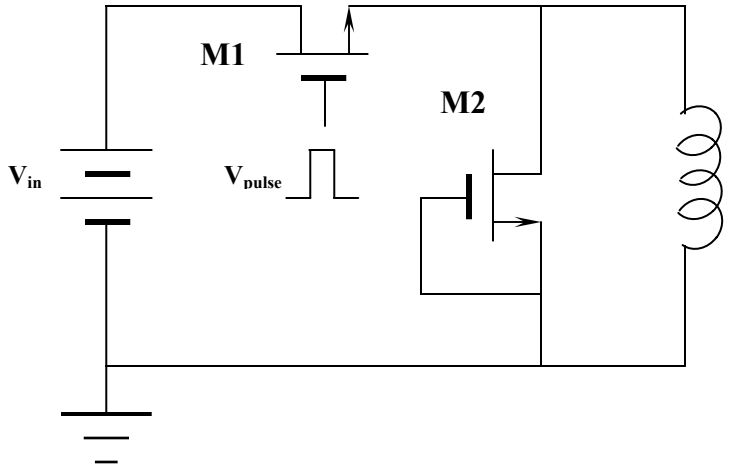


Fig.1. 9 A synchronous rectifiers with power MOSFETs

1.2.3 Failure Mechanisms in IGBTs

IGBTs (Insulated gate bipolar transistors) are another type of important power devices widely employed in hard-switching applications, such as include power conversion and motor drives. By combining the best features of BJT and MOSFET, IGBTs have many desirable properties including a MOS input gate, high switching speed, low conduction voltage drop, high current carrying capability and wide SOA. IGBTs have either a punch-through structure (PT) or non-punch-through structure

(NPT) which features different characteristics [14]. Fig.1.10 shows the vertical cross section of a PT and a NPT IGBT structure. IGBT structure is similar to the power MOSFET structure except an additional p+ layer has been added to the drain side of the MOSFET. It consists of a four-layer sandwich of $n^+/p/n/p^+$. The gate consists of a polysilicon layer which is separated by an oxide layer grown on the top surface of the silicon wafer. The polysilicon layer overlaps the n^+-source, p-base and n-drift regions. The emitter is made of metal contact which overlaps the n^+-source and p-base regions on the top. The collector is made by metal contact on the p^+-region in the bottom.

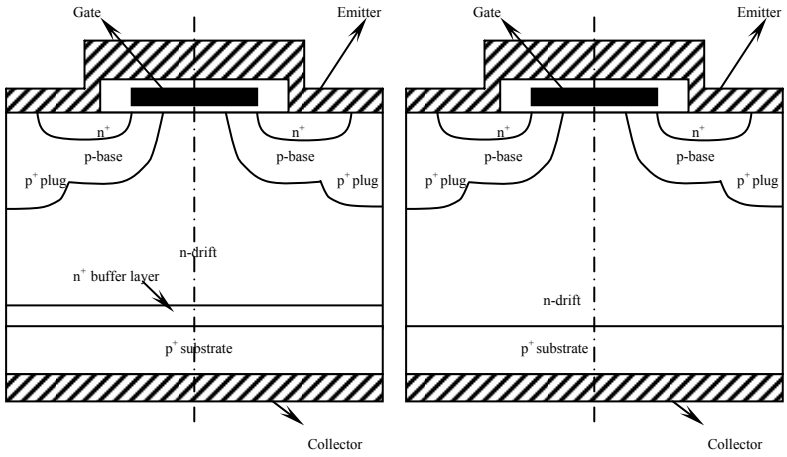


Fig.1. 10 The vertical cross section of the PT and NPT IGBT structures

In the normal operation mode, the collector is positive with respect to emitter. If the gate is at zero potential with respect to emitter, no main current flows from collector to the emitter. As shown in Fig.1.11 when gate potential becomes positive with respect to emitter, electrons are attracted in the p region below the gate oxide and eventually inverting the polarity of p type to n type. This inversion layer hence provides an n-channel from the n^+ layer to the n layer. Electrons are injected from the

n+ emitter contact into the n- region thus lowering the potential of this region and forward biasing the $p^+ n^-$ junction from the collector side. Hence holes are injected from the collector into the n-drift layer.

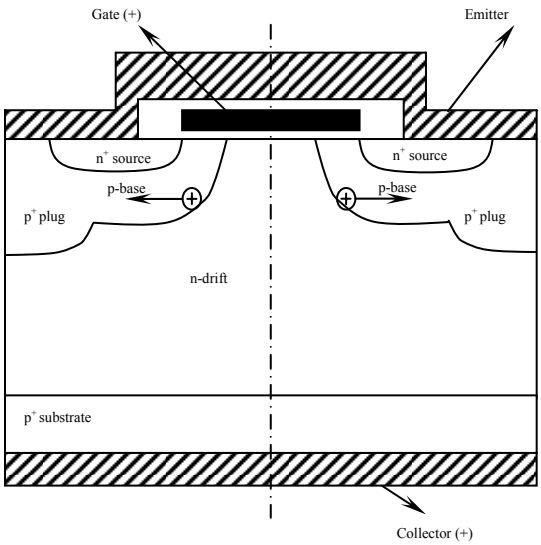


Fig.1. 11 The operation of the turn-on process of IGBTs

The excess holes and electrons in the n- region reduce the resistivity of this region. This is known as conductivity modulation, which reduces the on-state resistance of the device. This is why for a similar voltage design, an IGBT has a lower on-state resistance than a power MOSFET which does not exhibit conductivity modulation. In the PT structure, the injected holes from the p+ collector have to cross over the n+ buffer layer to reach n- base. Some of these holes are lost in the buffer layer due to recombination process. Consequently, the injection efficiency of the p+ is reduced. This has a significant influence on the dynamic characteristics of the IGBT.

Thermally assisted carrier multiplication

Thermally assisted carrier multiplication was proposed as the failure mechanism of IGBTs in [15]. Current flow through a region with high-electric field within IGBTs will lead to significant power dissipation. This dissipated power results in self-heating within the device and raises the working temperature of the device. The raised temperature will greatly increase the intrinsic carrier concentration and the net carrier multiplication rate of IGBTs. Again since IGBTs are used in high current conditions, the large current leads to a redistribution of charges and the electric field within the device. The increased charge density leads to higher peak electric field at the reverse-biased junction. This results in higher impact generation rate at the junction with a lower breakdown voltage than static conditions. With the combination effects of these two factors, IGBTs can fail under certain conditions. The most common high stress switching conditions for IGBTs are short circuit and clamped inductance switching conditions. How IGBTs failure because of thermally assisted carrier multiplication under these two conditions are introduced below.

Short circuits failure

Short-circuit switching is one of the most severe stress conditions for power devices, since a large current flows through the device while it is supporting the entire bus voltage. A test circuit for IGBT short circuits failures was used in [15] as shown in Fig.1.12**.** The IGBT was turned on with full bus voltage across and turned off after

a desired duration of stress. The results showed that the device subjected to this short-circuit stress failed after 15μs of stress [15].

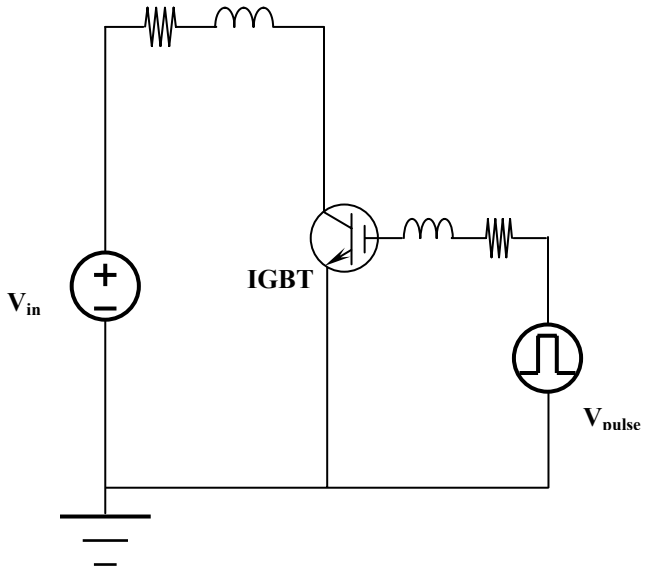


Fig.1. 12 Test circuit for IGBTs for short circuits failures

During the test the device can turned off successfully when gate voltage is removed and the temperature is within safe limits. The inversion channel under the gate is removed when the gate voltage is below the threshold value and electron current is abruptly cut off in the channel. Because the current out of the emitter is only the hole current, the current density is much lower and temperature within the device gradually falls off. The trapped excess charge in the drift region decays due to recombination.

However if the device is allowed to operate over a long duration under short condition, the temperature will rise steadily. Current crowding around the reverse-biased junction curvature will result in a much higher impact generation rate. The

carrier density is dramatically increased. Thus, there will have a local maximum of impact generation around the p-base/n-drift junction. The high impact generation and temperature in this region will initiate a regenerative process and the device will eventually break down due to this thermally assisted carrier multiplication. Under this condition, the current of IGBTs will rise uncontrollably while voltage falls down. The device fails to turn off even after gate voltage is removed and result in a catastrophic device failure.

Clamped inductive switching failure

Most common loads in power electronic circuits are inductive in nature. Thermally assisted carrier multiplication as the failure mechanism can also happen in IGBTs under clamped inductive switching condition [15]. A clamped inductive switching circuit for IGBTs is shown in Fig.1.13.

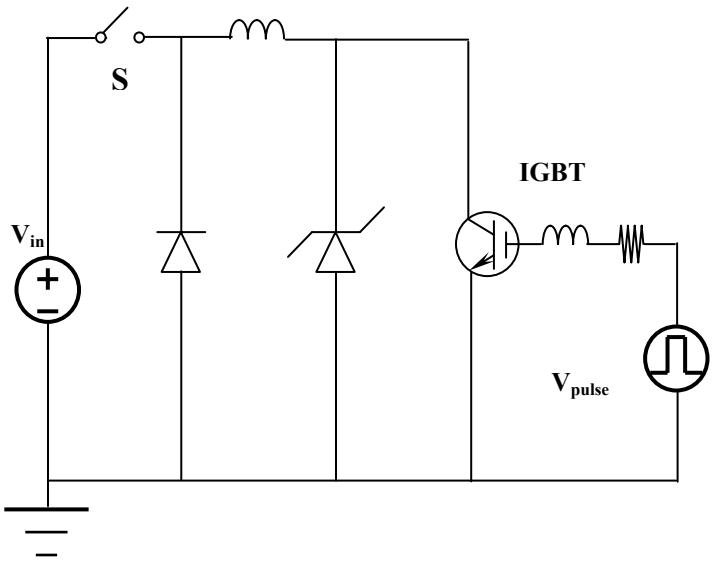


Fig.1. 13 A clamped inductive switching circuit used for IGBTs

In this circuit the switch S and the IGBT are turned on at the same time. After the inductor charges up through the device to a desired current level, the switch and IGBT are turned off simultaneously. The current will flow through IGBT and the freewheel diode D. Because the gate voltage is removed, the voltage on IGBT starts increasing rapidly to support the external current. The Zener diode will clamp the device voltage to the Zener diode breakdown voltage and prevent IGBT failure due to excessive rise in voltage. Once the voltage on IGBT beyond the Zener diode breakdown voltage, current will divert to the Zener diode and IGBT current decays with a recombination-dominated current tail.

In the on-state of IGBT, the electrons flow through the MOS channel and holes flow laterally in the p base. When the gate voltage is removed, electron current will be cut off. The inductive load, however, will still force the current through the device. This current can only be supported by the hole current and the displacement current of expanding depletion region in the device bulk. The hole current will rise up to meet the external current requirements within the IGBT. With the voltage on the IGBT rising up to support the inductor current, the electric field and impact generation rate at the p-base n-drift region junction keep increasing. The power dissipation will be significant with the high current density and high electric field in this region. Beyond a threshold value of power dissipation, the temperature rise is high enough to lead to device destruction. IGBT failure in this condition is due to thermally assisted carrier multiplication along the parallel plane reverse-biased junction of p base with the n-drift region.

Latch up failure in IGBTs

The IGBT structure shown in Fig.1.10 has a parasitic thyristor structure (NPNP) between the collector and the emitter. When the parasitic thyristor is turned on, the IGBT current will not be controlled by the MOS gate. The IGBT could be destroyed because of the excessive power dissipation produced by the high current flowing through the devices. The parasitic thyristor latch up can occur in IGBTs in two modes: static lat-up mode and dynamic latch-up mode. In the static mode, when the steady-state current density exceeds a critical value the latch-up will occur. The dynamic latch-up happens during switching conditions [16].

Static latch-up:

Since the conductivity of the drift region under the gate electrode is increased by the introduction of electron current through the channel, most of the holes injected into the drift region are injected at p-base region under the channel and flow to the source metal along the bottom of n^+-source. Due to this, the lateral voltage drops across the p-base region. If the voltage drop becomes greater than a threshold value, electrons are injected from the n^+-emitter to the p-base, and the parasitic NPN transistor (n^+-emitter, p-base and n-drift) is turned on. If the sum of the two NPN, PNP parasitic transistors base transport gain becomes larger than 1 ($\alpha_{TNPN}+\alpha_{TPNP}\geq 1$), the parasitic thyristor will be turned on and latch-up occurs [17]. As shown in Fig.1.10 the introduction of a deep, high concentration of p^+ region in IGBT device is used to reduce the resistance of p-base region and the potential drop caused by the hole current along the n^+-emitter and p-base junction. Once the voltage drop in that

junction can be control under the threshold voltage, the parasitic NPN transistor will be disabled.

Dynamic latch-up

Dynamic latch-up occurs in IGBTs under switching conditions. It is very interesting to know that the dynamic latching current is identical to the static latching current when latch-up happens during the turn-on of IGBTs and lower during gate-controlled turn-off of IGBTs [17]. When the IGBT is turned off, the depletion layer of the N^- drift and P base junction is abruptly extended to support the rising voltage, this increased depletion layer will increase the resistance of p base region. In addition to the displacement current, IGBT can latch up at a current lower than 1/2 of the static latch-up current.

1.3 Numerical simulation of failure mechanisms of SiC power devices

Two-dimensional numerical simulation approach has been used in this work to study the failure mechanisms of SiC power devices. The simulation algorithm is based on the basic semiconductor drift-diffusion model including Poisson equation, current continuity equation and carrier drift-diffusion equation. The detailed drift-diffusion model introduction is given in Chapter 2. The failure mechanisms of SiC Schottky diode, power MOSFETs and IGBTs are studied and studied in Chapter 3, Chapter 4, and Chapter 5 respectively.

Chapter 2: Drift-Diffusion Modeling for SiC Power Devices

The drift-diffusion model is frequently used to describe the characteristics of semiconductor devices which is the basis for all the numerical simulations conducted in this work. The basic equations included in the drift-diffusion model are introduced in details in this chapter. Different SiC physical models associated with the drift-diffusion model are discussed.

2.1 Poisson's Equation

Poisson equation relates the potential in a semiconductor material to its charge density by a divergence relationship:

$$\vec{\nabla}^2\phi - \frac{q}{\varepsilon}\left(n - p + N_a^- - N_d^+\right) = 0 \quad (2.1)$$

Where ϕ is the potential, e is the electron charge, ε is the dielectric permittivity of the semiconductor, n and p are the electron and hole concentrations, and N_d^+ and N_d^- are the ionized donor and acceptor concentration.

The values of N_d^+ and N_d^- in equation (2.1) are usually taken the initial carrier doping values. However the results obtained in this way will be only approximated ones without taking the incomplete ionization effect into consideration. The incomplete ionization in SiC can be modeled as [18]:

$$N_d^+ = \frac{N_d}{1 + g_d \frac{n}{N_c} \exp\left(\frac{E_c - E_d}{K_B T}\right)} \quad (2.2)$$

for donors and

$$N_a^- = \frac{N_a}{1 + g_a \frac{p}{N_v} \exp\left(\frac{E_a - E_v}{K_B T}\right)} \quad (2.3)$$

for acceptors.

Where N_d^+ and N_a^- are the ionized (activated) donor and acceptor concentration while N_d and N_a are the initial donor and acceptor doping values respectively, n and p are the electron and hole concentration, g_d is the ground-state degeneracy of donor impurity levels in SiC and g_a is the ground-state degeneracy of acceptor impurity levels, N_c is the conduction band effective density of states and N_v is the valence band effective density of states, E_c is the conduction band minimum energy and E_d is the valence band maximum energy, E_d is the inner-gap energy level for donor impurity

states and E_a is for acceptors, k_B and T are the Boltzmann constant and ambient temperature, respectively.

In equations (2.2) and (2.3) the energy difference $\Delta_d = E_c - E_d$ and $\Delta_a = E_a - E_v$ are the thermal ionization energy needed for the donor and accepter impurity atoms respectively.

The relationship between the electron concentration n, hole concentration p, and the conduction band minimum energy level E_c and valence band maximum energy level E_v are given by:

$$n = N_c \exp\left(\frac{E_f - E_c}{k_B T}\right) \quad (2.4)$$

and

$$p = N_v \exp\left(\frac{E_v - E_f}{k_B T}\right) \quad (2.5)$$

Where E_f is the Fermi level.

The Fermi level E_f is only quoted under thermal equilibrium condition. However two quasi-Fermi levels for electron and hole are needed to be introduced to handle nonequilibrium cases. The quasi-Fermi levels for electrons and hole are related to the intrinsic carrier concentration and the electron and hole concentrations respectively. They are defined as follows:

$$E_{fn} = E_i + k_B T \ln\left(\frac{n}{n_i}\right) \quad (2.6)$$

for electrons and

$$E_{fn} = E_i + k_B T \ln\left(\frac{n}{n_i}\right) \quad (2.7)$$

Where E_i is the intrinsic Fermi level.

Because of the lattice structure of silicon carbide, impurity atoms can occupy different types of sites in the crystal. For examples there are two inequivalent (C or Si) sites in 4H-SiC, one with cubic (k) surrounding and the other with hexagonal (h) surrounding as described in [19]. Since each site has different ionization energy for the dopants, this indicates different values of Δ_d or Δ_a. The model for incomplete ionization in (2.2) can be expanded as:

$$N_d^+ = \sum_i \frac{\delta_i N_d}{1 + g_d \frac{n}{N_c} \exp\left(\frac{E_c - E_{di}}{k_B T}\right)} \quad (2.8)$$

for electrons and

$$N_a^- = \sum_i \frac{\delta_i N_a}{1 + g_d \frac{p}{N_v} \exp\left(\frac{E_{ai} - E_v}{k_B T}\right)} \quad (2.9)$$

for holes.

Where δ_i is the probability of a site being ionized at the ith site and E_{di} and E_{ai} are the ionization energy associated with that site. Based the assumption that average contribution is from the different ionization levels, the value of δ_i in (2.8) is 1/2 for 4H-SiC since it has two sites for donor impurity to occupy. And the value of δ_i for 6H-SiC is 1/3 since it mainly has three main ionization energy levels. The values of g_a and g_d in the equations are equal to the reciprocal of δ_i.

The most common dopant for n-type SiC is *N*. Doping with *N* leads to a donor (substituting on C-site) which has two different energy levels below the conduction band. The reason for the two ionization energies is that in 4H-SiC there are two inequivalent C (or Si) sites, one with cubic (k) surrounding and the other with hexagonal (h) surrounding [20]. Nitrogen atoms substituting on these sites experience somewhat different surroundings, giving rise to different ionization energies. In fact, it was found in [3] that *k*-type *N* causes deeper levels than *h*-type *N*. It is also expected that the number of *k*-type and *h*-type donors are more or less the same. In 4H-SiC the two ionization energies are E_c-E_h = 52 meV, E_c - E_k = 92 meV where E_c denotes the conduction band minimum and E_h (E_k) the energy level of the cubic (hexagonal) *N* donor. Then from equation (2.8) we have that

$$\frac{N_d^+}{N_d} = \frac{1}{2} \times \left(\frac{1}{1 + 2 \times \frac{n}{N_c} \exp\left(\frac{0.052}{k_B T / q} \right)} + \frac{1}{1 + 2 \times \frac{n}{N_c} \exp\left(\frac{0.092}{k_B T / q} \right)} \right) \quad (2.10)$$

$$N_c = 2*\left(\frac{2\pi k_B T m_n^*}{h^2}\right)^{3/2} \qquad (2.11)$$

Where N_c is the averaged density of states, m_n^* is the effective mass for the conduction bands, h is Planck's constant, and k_B is Boltzman's constant. For 4H-SiC, m_n^* equals $0.76m_o$. The incomplete ionization of n-type 4H SiC doped with Nitrogen is plotted in Fig.2.1. The results show that the incomplete ionization will not be a problem until the doping concentration is up to $1\times10^{17}cm^{-3}$.

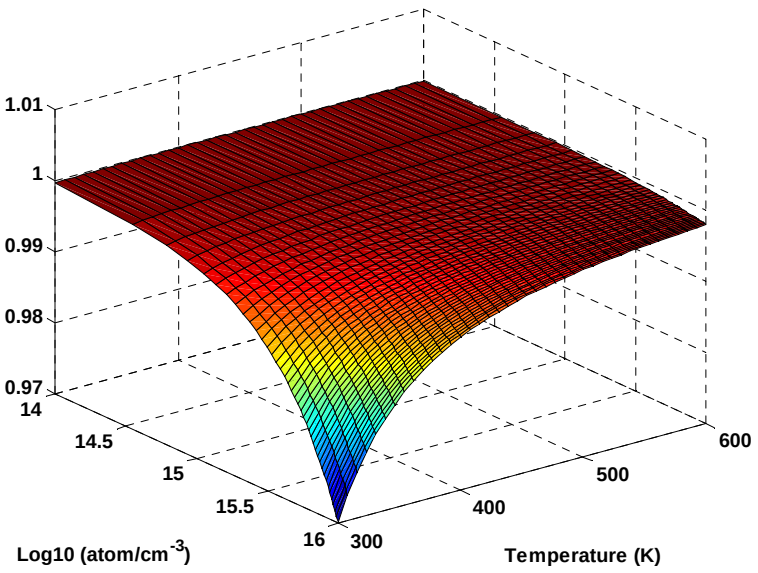


Fig.2. 1 The incomplete Ionization of n-type 4H SiC doped with Nitrogen

2.2 Current Continuity equations

The change rate of electrons within a one-dimensional distance *dx* can be modeled as [21]

$$\frac{\partial n}{\partial t} Adx = \left(\frac{\vec{J}_n}{-q} - \frac{\vec{J}_n(x+dx)}{-q} \right) A + (G_n - R_n) Adx \quad (2.11)$$

Where A is the cross section area, G_n and R_n represent the generation and recombination rates of electrons within dx, J_n is the electron current density. Equation $\left(\frac{\vec{J}_n}{-q} - \frac{\vec{J}_n(x+dx)}{-q} \right)$ stands for the net increase of electron within dx. The second term in equation $J_n(x+dx)$ can be expanded by a Taylor series:

$$\vec{J}_n(x+dx) = \vec{J}_n(x) + \frac{\partial \vec{J}_n}{\partial x} dx + \cdots \quad (2.12)$$

Then equation (2.11) can be simplified as:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \frac{\partial \vec{J}_n}{\partial x} + (G_n - R_n) \quad (2.13)$$

The analogous equation for holes is given by

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \frac{\partial \vec{J}_p}{\partial x} + (G_p - R_p) \quad (2.14)$$

Equations (2.13) and (2.14) are called current continuity equations. The current continuity equations state that the time varying charge density is equal to the

net increase rate of carrier densities flow into the space plus the net carrier generation within the space.

2.3 Drift-diffusion current equations

Drift Current

In the drift-diffusion model, the current composes of two components: drift current and diffusion current. The current due to carrier drift under the applied field is called drift current. This drift electron current density can be found by summing the product of the charge of each electron times its drift velocity over all the carriers *n* within per unit volume:

$$\vec{J}_{n-drift} = -qn\vec{v}_n \quad (2.15)$$

Where $\vec{v}_n$ is the average electron drift velocity due to an applied electrical field. The drift velocity is related to electron mobility and the applied electric field $\vec{E}$ as:

$$\vec{v}_n = -\mu_n \vec{E} \quad (2.16)$$

Then we have

$$\vec{J}_{n-drift} = qn\mu_n \vec{E} \quad (2.17)$$

Diffusion Current

The carriers tend to mover from a region of high concentration to a region of low concentration. The current associated with this diffusion process in semiconductor is called diffusion current. Again the electron diffusion current in a one-dimensional distance *dx* can be expressed as:

$$\vec{J}_{n-diff} = -qD_n\left(n(x) - n(x+dx)\right) \quad (2.18)$$

With a similar Taylor series expansion and first order approximation to (2.12), we have:

$$\vec{J}_{n-diff} = qD_n \frac{dn}{dx} \quad (2.19)$$

Where D_n is the electron diffusion coefficient and can be can be related to the electron mobility using the Einstein relation:

$$\frac{D_n}{\mu_n} = \frac{k_B T}{q} \quad (2.20)$$

2.4 The Drift-Diffusion Model

The total electron transport current can be simply obtained by adding up the drift current and the diffusion current:

$$\vec{J}_n = \vec{J}_{n-drift} + \vec{J}_{n-diff} = qn\mu_n \vec{E} + qD_n \frac{dn}{dx} \quad (2.21)$$

A similar total hole transport current can be derived as:

$$\vec{J}_p = \vec{J}_{p-drift} + \vec{J}_{p-diff} = qn\mu_p \vec{E} + qD_p \frac{dp}{dx} \quad (2.22)$$

Where D_p is the hole diffusion coefficient and has a similar Einstein relation as equation (2.20).

Replacing the electric field E in equations (2.21) and (2.22) based on the relationship $E = -d\phi / dx$, the drift-diffusion model is expressed as:

$$\vec{\nabla}^2 \phi - \frac{q}{\varepsilon}\left(n - p + N_a^- - N_d^+\right) = 0 \quad (2.1)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial \vec{J}_n}{\partial x} + \left(G_n - R_n\right) \quad (2.13)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial \vec{J}_p}{\partial x} + \left(G_p - R_p\right) \quad (2.14)$$

Where current densities $\vec{J}_n$ and $\vec{J}_p$ are defined as

$$\vec{J}_n = -qn\mu_n \frac{\partial \phi}{\partial x} + qD_n \frac{dn}{dx} \quad (2.21)$$

$$\vec{J}_p = -qn\mu_p \frac{\partial \phi}{\partial x} - qD_p \frac{dp}{dx} \quad (2.22)$$

It is apparent that recombination, generation, and mobility play important roles in the model of drift-diffusion. The models used to describe these physical phenomena will be introduced in the following.

Generation and Recombination

Shockley-Read-Hall Recombination:

There are many recombination centers in semiconductor bulk that determine the lifetime of carriers. They have localized electrons states with energies within the forbidden gap, typically close to the intrinsic Fermi level. The theory for recombination through these localized centers is called *Shockley-Read-Hall* theory [4]:

$$R^{SRH} = \frac{np - n_i^2}{\tau_n\left[p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right] + \tau_p\left[n + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right]} \quad (2.23)$$

$$\tau_n = \frac{1}{N_t \nu_{th} \sigma_n} \quad (2.24)$$

$$\tau_p = \frac{1}{N_t \nu_{th} \sigma_p} \quad (2.25)$$

Where N_t is the density of state, v_{th} is the electron thermal velocity, σ_n is called the capture cross section describing the effectiveness of the localized state in capturing an

electron, σ_p is the capture cross section for holes. τ_n and τ_p are the lifetime of electrons and holes, respectively.

Since most elective recombination centers are close to the intrinsic Fermi level, equation (2.23) can be simplified as:

$$R^{SRH} = \frac{np - n_i^2}{\tau_n(n + n_i) + \tau_n(p + n_i)} \quad (2.26)$$

The lifetimes τ_n and τ_p as a function of doping and temperature are given by the following equations [22]:

$$\tau_{n,p} = \frac{\tau_{no,po}(\frac{T}{300})^{\gamma_{n,p}}}{1 + (\frac{C}{C_{n,p}^{ref}})^{\alpha_{n,p}}} \quad (2.27)$$

Where τ_{no} and τ_{po} are the intrinsic minority carrier lifetimes, $\gamma_{n,p}$, $\alpha_{n,p}$ and C_n^{ref} are empirical modeling parameters

Auger Recombination

Auger recombination describes the direct recombination process of electrons and holes [21]. When excess carriers recombine in a region that has a high doping concentration the probability of direct recombination between holes and electrons

may not be negligible compared to the probability of recombination through traps (SHR recombination). This direct recombination process is called Auger recombination. In Auger recombination, three free carriers interact, either two electrons and a hole, or two holes and an electron. Two of the carriers recombine and the third carries away the momentum of the oncoming carriers and the energy released by the recombination event. Because of the need for the simultaneous interaction of three carries we can expect that Auger recombination is highly unlikely expect in heavily doped material. An expression for the Auger recombination rate R^A is

$$R^A = \Gamma_n n\left(pn - n_i^2\right) + \Gamma_n p\left(pn - n_i^2\right) \quad (2.28)$$

Where Γ_n is the coefficient representing interactions in which the remaining carrier is an electron, and Γ_p is the coefficient representing interactions in which the remaining carrier is a hole. Extracted and derived values for the recombination models in SiC are found in [6].

Impact Ionization Generation

Some carriers in the devices may reach very high transport speeds. These high-speed particles are also high in energy, and this energy may contribute to the generation of excess electron-hole pairs. The generation occurs when the high energy particle collides with a bonded particle resulting in one additional free electron and

one additional free hole. This type of generation is referred to as avalanche or impact ionization generation. The impact ionization model can be expressed by [22]

$$G^{II} = \alpha_{n,ii}\frac{\vec{J}_n}{q} + \alpha_{p,ii}\frac{\vec{J}_p}{q} \quad (2.29)$$

Where $\alpha_{n,ii}$ and $\alpha_{p,ii}$ are the electron and hole impact ionization coefficients. As described in [22][24,25], the ionization coefficients for 4H-SiC can be expressed in terms of the local electric field according to

$$\alpha_{n,ii} = 1.66\times10^{6}\exp\left[-\left(\frac{2.2\times10^{7}}{E_{n,\|}}\right)\right] \quad (2.30)$$

$$\alpha_{p,ii} = 5.86\times10^{6}\exp\left[-\left(\frac{1.4\times10^{7}}{E_{p,\|}}\right)\right] \quad ((2.31)$$

Where $E_{n,\|}$ and $E_{p,\|}$ are the electric field components in the direction of current flow.

Mobility Model

The Caughey-Thomas model is used for 4H-SiC low-field mobility modeling [22]:

$$\mu_{n,p}^{LF}(T,C) = \mu_{n,p}^{\min} + \frac{\mu_{n,p}^{\delta}(\frac{T}{300})^{\alpha_{n,p}} - \mu_{n,p}^{\min}}{1+(\frac{C}{C_{n,p}^{ref}})^{\gamma_{n,p}}} \quad (2.32)$$

Where α, γ and C^{ref} are model parameters and C is the net ionization doping. The high field mobility model used is [22]:

$$\mu_{n,p}^{HF}(T,C) = \frac{\mu_{n,p}^{LF}}{(1+(\frac{\mu_{n,p}^{LF}\left|\vec{E}\right|}{\upsilon_{n,p}^{sat}})^{\beta_{n,p}})^{1/\beta_{n,p}}} \quad (2.33)$$

2.5 Boundary Conditions

The boundary conditions associated with the drift-diffusion model on silicon carbide power device modeling are needed to be addressed here.

Ohmic Contacts

Ohmic contact is defined as the contact itself offers negligible resistance to current flow when compared to the bulk [21]. That means that when voltage is applied across a device with ohmic contacts, the voltage dropped across the ohmic contact is negligible compared to voltage drops elsewhere in the device. Thus no power is dissipated in the contact. An importance and useful consequence of this property is that all free-carrier densities at an ohmic contact are unchanged by current flow. It is well-known that the material potentials of a doped semiconductor in thermal equilibrium can be modeled by the following equations:

$$\phi_n = V_T \ln\frac{N_d^+}{n_i} \quad (2.34)$$

for n-type semiconductor and

$$\phi_p = V_T \ln \frac{N_a^-}{n_i} \quad (2.35)$$

for p-type semiconductor.

Where n_i is the intrinsic carrier concentration, V_T is the thermal voltage, and N_d^+ and N_a^- are the ionized (activated) donor and acceptor concentrations respectively. There is no voltage drop across the ohmic contact, so the boundary condition for electrostatic potential at the contact-semiconductor boundary is equal to

$$\phi_n' = V_a + \phi_n \quad (2.36)$$

for ohmic contacts at n-type material side and

$$\phi_p' = V_a + \phi_p \quad (2.37)$$

for ohmic contacts at p-type material side.

Because of the no-power-loss property of the ideal ohmic contact, thermal equilibrium, and therefore charge neutrality, can be assumed at the contact-semiconductor boundary. The total charge density ρ is given by

$$\rho = q(p - n + C) = 0 \quad (2.38)$$

Where $C = N_d^+$ and N_a^- which is the net ionization doping concentration. Since it is under thermal equilibrium conditions, the mass action law $np = n_i^2$ holds. Then we have that:

$$n = \frac{C}{2} + \frac{\sqrt{D^2 + 4n_i^2}}{2}, p = \frac{n_i^2}{n} \quad (2.39)$$

for n-type material and

$$p = -\frac{C}{2} + \frac{\sqrt{D^2 + 4n_i^2}}{2}, n = \frac{n_i^2}{p} \quad (2.40)$$

for p-type material.

Chapter 3: Characterizations and failure mechanism investigation for SiC Schottky Diodes

As discussed in Chapter 1, Schottky diodes can provide the benefits of very low forward voltage drop and much quick switching time as a majority carrier device. These features make Schottky diodes very good switching devices used in power supplies. With the properties of high breakdown voltage and high thermal conductivity, SiC Schottky diodes can offer extra advantages over traditional Si and GaAs Schottky diodes. For Schottky diode the maximum blocking voltage can be simply described by equation:

$$V_{\max} = \frac{E_c W}{2} \quad (3.1)$$

Where E is the critical breakdown electric field of the material and W is the depletion width of the Schottky diode which is determined by

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_a)}{qN_d}} \quad (3.2)$$

Where ε_s is the dielectric constant of the material, V_{bi} is the build-in potential of the diode, V_a is the applied reverse bias, and N_d is the doping density of the material. The critical electric field E_c for 4H SiC, Si and GaAs are 2.2×10^6 (V/cm), 2.5×10^6 (V/cm),

and 3×10^5 (V/cm) respectively. The calculated results for ideal results for ideal breakdown voltage of SiC and GaAs and Si Schottky diode are plotted in Fig.3.1 which shows the advantages of SiC when used in power devices.

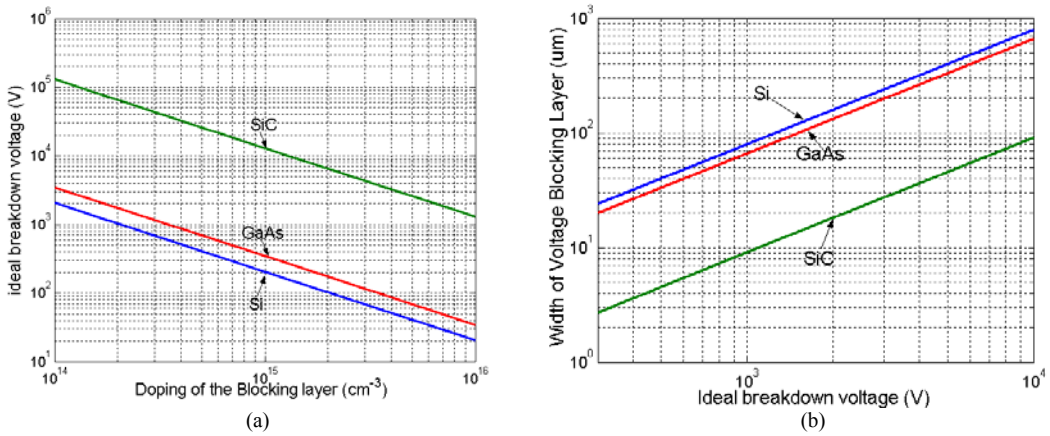


Fig.3. 1 Comparison of the ideal breakdown voltages of SiC, GaAs and Si devices (a) for different doping levels (b) for different the blocking layer thickness

The results in Fig.3.1 (b) showed that SiC Schottky diodes can be made with a much smaller physical size compared to Si and GaAs diodes for a same block voltage requirement. This advantage is also applicable to all other SiC power devices. In this chapter the experimental and simulation of 4H SiC Schottky diode are introduced first in section 3.2. The correctness of the drift-diffusion model with the associated SiC physical models and parameters is verified by agreement between the experimental and simulation results. The failure mechanism investigation for non-catastrophic failures happened in Schottky diodes is conducted in the following section.

3.1 Numerical Simulation of SiC Schottky Diodes

3.1.1 Introduction

With material progress and the development of high quality single crystal 4H-SiC wafers, high voltage 4H-SiC Schottky diodes have been fabricated in [26]~[29]. To get more reliable and quantitative information about the 4H-SiC Schottky diodes, detailed device characterizations are needed.

Experimental and simulation results on n-type Ti/4H-SiC Schottky diodes conducted in this work. I-V measurements for 4H-SiC Schottky diodes at different temperatures were first performed using an ITS8000 testing system. This system allows the I-V characteristic to be recorded from 273K-550K. The electrical characteristics were then simulated based on the drift-diffusion model. The simulated device structure is presented in Fig.3.3. It includes a 4μm epitaxial n-drift layer and a 1μm epitaxial n^+ layer. The two layers are uniformly doped by 1×10^{15} cm^3 and 1×10^{18} cm^3 respectively.

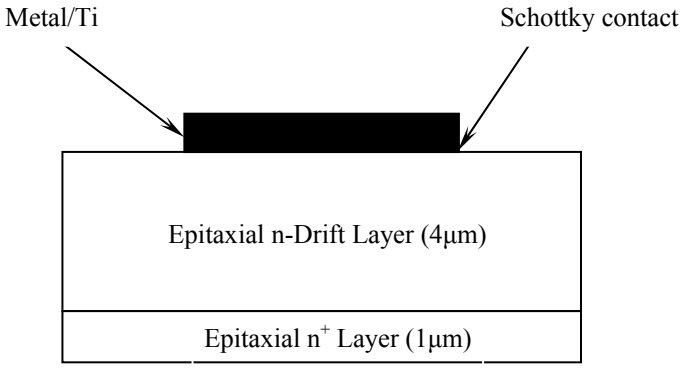


Fig.3. 2 The schematic cross-section of the active layers of SiC Schottky diode

3.1.2 Physical Models of SiC Schottky Diodes

To simulate the characteristics of 4H-SiC Schottky diodes under different temperatures, the carrier mobility, and intrinsic concentration, generation and recombination models, including their temperature dependence were used in the drift-diffusion model with proper boundary conditions.

Drift-Diffusion Model

Since only the I-V characteristics of SiC Schottky diode were simulated, the steady state drift diffusion model is used, which means $\partial n/\partial t = 0, \partial p/\partial t = 0$ in equations (2.12) and (2.13), the current continuity equation is simplified as:

$$-\frac{1}{q}\frac{\partial \vec{J}_n}{\partial x} = \left(G_n - R_n\right) \quad (3.3)$$

$$\frac{1}{q}\frac{\partial \vec{J}_p}{\partial x} = \left(G_p - R_p\right) \quad (3.4)$$

The Poisson equation and current transport equations keep same for the steady state drift diffusion model

Boundary Conditions

When a voltage V_a is applied to the metal gate, the potential boundary condition ψ_{MS} at the Schottky contact side is given by

$$\psi_{MS}(T) = \psi_o(T) + V = \frac{1}{2}\left\{E_g(T) - V_{TH}\ln\left(\frac{N_V(T)}{N_C(T)}\right)\right\} - \phi_B + V_a \quad (3.5)$$

Where T is the lattice temperature, E_g is the bandgap of SiC, ϕ_B is the barrier height, V_{TH} is thermal voltage, ψ_o is the potential at zero bias voltage and N_c and N_v are the effective density of states in the conduction band and valence band [30].

The potential boundary condition ψ_{SO} at the ohmic contact side is

$$\psi_{SO}(T) = V_{TH}\ln\left(\frac{N_D(T)}{n_i}\right) \quad (3.6)$$

Intrinsic Carrier Concentration and Band Gap Narrowing

The intrinsic carrier concentration n_i is determined by the standard textbook equation. The first order temperature dependence model for bandgap narrowing is modeled by [22]:

$$E_g(T) = E_{go} + \frac{dE_g}{dT}(T - 300) \quad (3.7)$$

Where E_{go} is the bandgap of 4H-SiC at room temperature.

The carrier mobility model and generation and recombination models used in the simulation are the same as the models introduced in Chapter 2. The parameters used in simulation are listed in Table 3.1.

Table 3. 1 Parameters for 4H-SiC device simulation

Parameter	4H-SiC	REF	Parameter	4H-SiC	REF
Dielectric constant ε	9.66	[31]	***Mobility μ***		
Intrinsic concentration n_i (cm^{-3} at 300K)	5.27×10^{-8}	[18]	μ_n^{δ} (cm^2/Vsec)	947	[18]
M_C (Effective Mass in Conduction Band)	$0.76m_0$	[18]	$\mu_n^{\min}$ (cm^2/Vsec)	0	[18]
M_V (Effective Mass in Valence Band)	$1.20m_0$	[18]	C_n^{ref} (cm^{-3})	1.94×10^{17}	[18]
Bandgap narrowing (eV)			α_n	-2.4	[18]
E_{go} (eV)	3.26	[18]	γ_n	0.61	[18]
dE_g/dT (eV/K)	-3.3×10^{-4}	[18]	β_n	2	[32]
Shockley-Read-Hall SRH			***Shockley-Read-Hall SRH***		
τ_{no}(sec)	1×10^{-9}	[33]	C_n^{ref} (cm^{-3})	3.1×10^{15}	[33]
τ_{po}(sec)	6×10^{-7}	[33]	$\alpha_{n,p}$	0.37	[33]
$\gamma_{n,p}$	2.5	[34]	β_n	2	[32]

3.1.3 Simulation Results and Discussion

The SiC parameters and the various semiconductor physics models are incorporated into the simulator. The experimental and simulation results of the forward current-voltage (I-V) characteristics of the Ti/4H-SiC Schottky diode at four different temperatures are plotted in Fig.3.4. Simulation and measurement are in very good agreement and indicate that the model is relatively accurate.

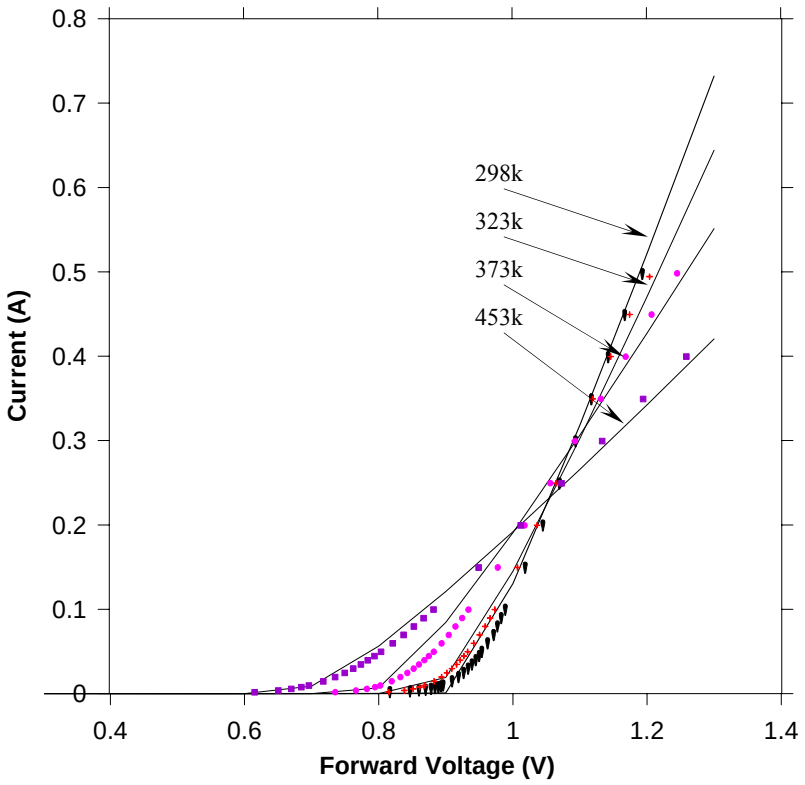


Fig.3. 3 Simulation of forward I-V characteristics of Ti/4H-SiC Schottky diode for different Temperatures (solid curve). Experimental results of Ti/4H-SiC Schottky diodes are compared (dot curve)

With zero applied bias the difference between the potentials in boundary conditions (3.5) and (3.6) largely determines the turn-on voltage for SiC Schottky diodes. At higher temperature the values of increased thermal voltage V_{TH} and the narrowing of bandgap E_g are very small compared to the decreased value of barrier height in equation (3.5), thus the potential ψ_{MS} on the Schottky contact side is increased mainly because of the decreased value of barrier height ϕ_B. Meanwhile the potential value ψ_{SO} on the ohmic contact side is decreased because the intrinsic carrier density in equation (3.7) is increased 10 orders of magnitude (from 6.4×10^{-9}cm^{-3} to 60 cm^{-3}) as temperature increases from 298K to 453K. So the effects of decreased potential ψ_{SO} and the increased potential ψ_{MS} give rise to a decreased turn-

on voltage for the Schottky diodes with increasing temperature. From Fig.3.4 we can see the turn-on voltage is decreased approximately from 0.9V to 0.6 V when the temperature is increased from 298K to 453K.

Barrier height is one of the important parameters for Schottky diodes. Barrier height and its temperature dependence for SiC Schottky diodes have been discussed previously [35]~[38]. However, barrier height is difficult to determine in Schottky diodes because it involves many complex physical mechanisms. Because of different fabrication processes in making Ti/4H-SiC Schottky diodes, a range of 0.99~1.15eV of barrier height at room temperature has been reported [26][28]. In [38] a negative temperature dependence of barrier height on n-type 6H-SiC Schottky diodes was also found. By combining our simulation and IV measurement, the barrier heights of 4H-SiC Schottky diodes can be extracted and are 1.14eV, 1.06eV, 0.97eV and 0.91eV under the temperature 298.15K, 323.15k, 373.15k, and 423.15K respectively.

Our results are similar to the negative temperature dependence reported in [38] for 6H-SiC Schottky Diodes. As barrier height is found to be approximately linearly dependent on temperature, then a relationship between barrier height and temperature can be given by

$$\phi_B(\mathrm{T}) = \phi_{B0} + \gamma T \quad (3.8)$$

Where ϕ_{B0} is the barrier height at room temperature. Based on the data in table 2, a γ value of 4.25×10^{-4} eV/K is determined by least square fitting.

On-resistance (R_{on})

One of the advantages of SiC Schottky diodes is that they have lower on-resistance than traditional Si Schottky diodes. The on-resistance (R_{on}) of 4H-SiC Schottky diodes can be two orders lower than the value of Si Schottky diodes, and less than one-fifth of the value of 6H-SiC [28]. A Schottky diode can be modeled as a series combination of a diode and a resistor described as on-resistance R_{on}. The voltage V_D across the Schottky diode can then be expressed in terms of the total voltage drop V_F across the series combination of the diode and the resistor $V_D=V_F - IR_{on}$. Then for a Schottky diode, we have that [39]:

$$I_F = I_s[\exp[q(V_F - I_F R)/nkT] \quad (3.9)$$

$$I_s = A_{eff} A^* T^2 \exp(-q\phi_B / kT) \quad (3.10)$$

Where A_{eff} is the effective area of the diode, A^* is the Richardson constant, q is the electron charge, ϕ_B is the Schottky barrier height of the diode, K is the Boltzmann's constant, n is the ideality factor and T is the temperature.

On-resistance R_{on} can be extracted from I-V characteristics by taking derivative with respect to current I_F and rearranging items in equation (3.9):

$$R_{on} = \frac{\partial V_F}{\partial I_F} - \frac{nkT}{q} \times \frac{1}{I_F} \quad (3.10)$$

When the diodes work in the far forward region, the value of the second term in (14) can be ignored and on-resistance R_{on} is simplified by

$$R_{on} \approx \frac{\partial V_F}{\partial I_F} \quad (3.11)$$

Apparently R_{on} is the slope of I-V curves. In Fig.3.5 on-resistance R_{on} extracted from Fig.3.4 is plotted in log scale. It shows clearly that R_{on} increases monotonically with temperature which is similar to the results in [26] and [29]. A $T^{2.23}$ on-resistance variation with temperature is obtained for these 4H SiC Schottky diodes. The result is consistence with that in [29] and [40].

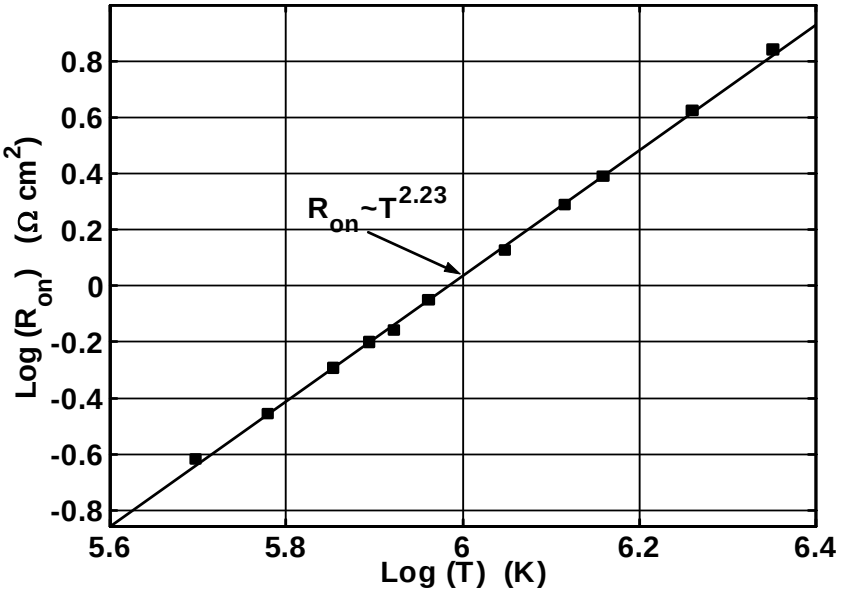


Fig.3. 4 Temperature dependence of on-resistance

Mobility Temperature dependence

For power devices the on-resistance R_{on} for a specified breakdown voltage is given by [17]

$$R_{on} = \frac{4V_B^2}{\varepsilon_s E_c^3 \mu_n} \quad (3.12)$$

Where ε_s is the permittivity of SiC, E_c is the critical electric field, V_B is the breakdown voltage and μ_n is electron mobility. Once the doping and structure in the device are specified the breakdown voltage and the critical electric field of the device are determined. With ε_s, E_c, V_B are all constants in equation (3.12), a relationship between on-resistance and mobility is obtained in equation (3.13)

$$\mu_n \propto (1/R_{on}) \quad (3.13)$$

Just as predicted in [26] the increase in on-resistance R_{on} is a measure of the decrease in the mobility with temperature. It is obvious from our previous result (Fig.3.5) that a temperature dependence relationship $\mu_n \sim T^{-2.23}$ can be obtained in (3.13).

Another temperature dependence relationship between mobility and temperature can also be derived from the mobility models used in equations (2.33) and (2.34). The mobility variation under different temperatures along the device from n^+ epilayer to n drift epilayer is showed in Fig 3.6. The average mobility in these two

epilayers under different temperatures is showed in Fig.3.7. Clearly mobility is a function of temperature and doping density.

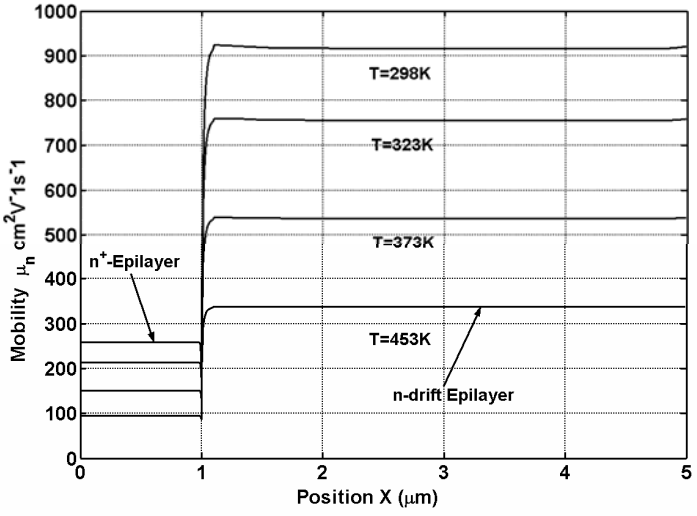


Fig.3. 5 Mobility variation from n^+ epilayer to n-drift epilayer under different temperature

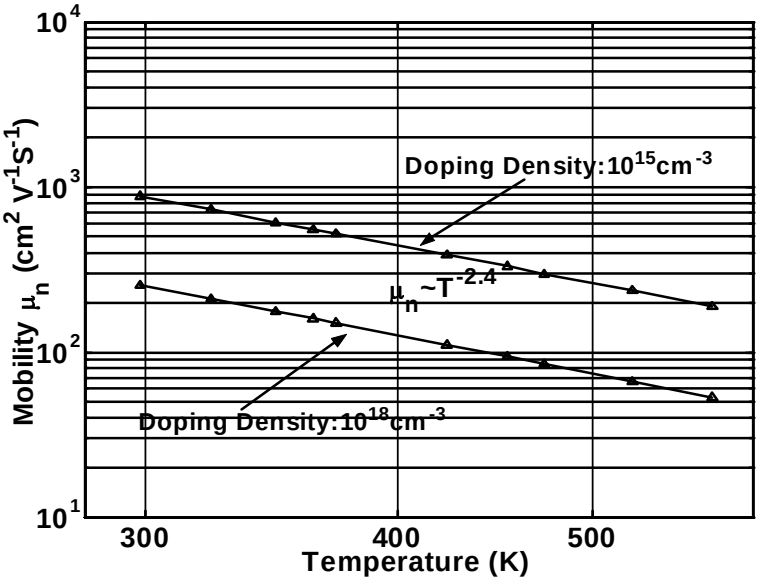


Fig.3. 6 Average mobility for different doping density under different temperature from the drift-diffusion model

A $T^{-2.4}$ variation with temperature is obtained by fitting curves in Fig.3.6. From the two mobility temperature dependencies from the on-resistance model and

mobility model, we conclude that a temperature variation of $T^{-2.4\sim-2.2}$ for mobility in 4H-SiC Schottky diodes is appropriate.

3.2 Non-catastrophic failure mechanisms of SiC Schottky diodes

3.2.1 Introduction

Non-catastrophic failures were observed in Schottky diodes. The characteristics of diodes were slowly degraded during device normal operation. Failure criteria for non-catastrophic failures were introduced for GaAs Schottky diodes in [1]. These criteria were related to the degradation of device characteristics such as diode ideality factor, series resistance, and turn-on voltage. However a detailed data analysis for device characteristic degradation was not provided and the failure mechanism responsible for this non- catastrophic failure was not clear to the authors. Thus the investigation of this non-catastrophic failure mechanism of Schottky diode was conducted in work

A Schottky diode is made of a metal layer and a semiconductor layer. When the metal is contacted with the semiconductor surface, the metal and semiconductor do not make intimate contact since interface states exist between metal and semiconductor surface as shown in Fig.3.7

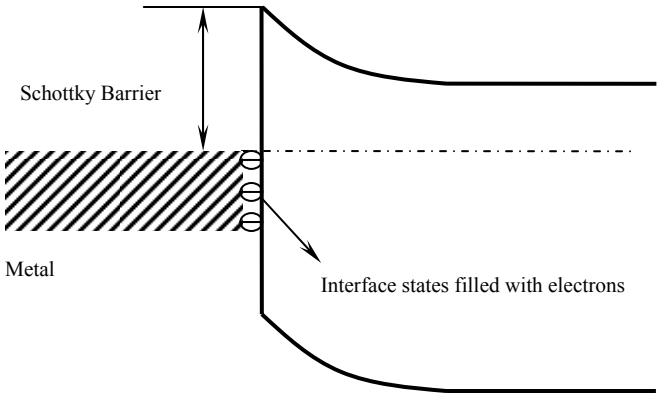


Fig.3. 7 The Band diagram of an n-type Schottky diode with interface states

Interface states as the main defects existing in Schottky diodes were studied extensively in literature. They can be easily induced at the metal-semiconductor interface during device fabrication. For example, some chemical bonds in the surface of semiconductor can become unbonded and form some interface states in diodes during fabrication process such as annealing. The formation of interface traps in Au/InGaP Schottky diodes was reported in [4]. The interface states were generated by heat treatment in Au/$In_{0.5}Ga_{0.5}P$ contacts. The origin of these interface states is attributed to the transformation of a simple phosphorus vacancy to antisite-related defect such as Ga_p, and In_p. Interface states generated during the annealing process in Ti/n-GaAs Schottky diode were also investigated in [5]. The interface states were attributed to the annealing processing which removed the passivation effect of the native oxide layer and reactivated these surface defects. Similar results were obtained for n-type 6H-SiC Schottky diodes in [6]. During the annealing process significant

reactivation of the passivated defects is shown to start in the interface at temperature between 350 and 400 ^{0}C in the SiC Schottky diodes.

Because interface states in n-type Schottky diodes can act as the traps of electrons, the characteristics of the Schottky diodes will be affected. The interface states filled with electrons will serve as Coulomb scattering centers and suppress the I-V characteristics of the diodes. In this study, device simulations were conducted to show how interface states cause the degradation of I-V characteristics of Schottky diodes and lead to the non-catastrophic failure of the diodes.

3.2.2 Simulation of I-V characteristic degradation of SiC Schottky diodes

Simulation Algorithm

MEDICI, as a two-dimension semiconductor device simulator, has been used extensively by researchers and engineers to gain physical insights and to aid design and analysis of semiconductor devices [41]. Given device structure, material type, proper physical model, doping profiles, and boundary conditions, MEDICI can numerically solve the five semiconductor fundamental equations which govern the behaviors of the semiconductor Trapped Charge Advanced Application Modules (AAM) is one of advanced modules of MEDICI providing the ability to simulate the characteristics of semiconductor devices containing traps. It can simulate all types of traps in semiconductor devices including interface states. The Poisson equation is then modified to include the number of electrons that are trapped by the interface states:

$$\varepsilon\nabla^2\phi = -q(p - n + N_D^+ - N_A^-) - \rho_{it} \quad (3.14)$$

Where ρ_{it} are the charged interface states.

Along the outer (non-contact) edges of devices, homogeneous (reflecting) Neumann boundary conditions are imposed so that current only flows out of the device through the contacts. In the absence of surface charge along such edges, the normal electric field component becomes zero. At the interface between two different materials, the difference between the normal components of the respective electric displacements must be equal to interface states according to:

$$n \cdot \varepsilon_1 \nabla\phi_1 - n \cdot \varepsilon_2 \nabla\phi_2 = \rho_{it} \quad (3.15)$$

The simulated device structure is shown in Fig.3.8:

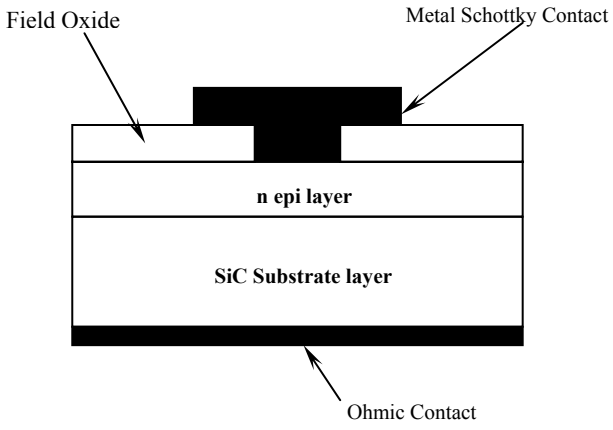


Fig.3. 8 The Schematics of SiC Schottky diode with field plate

The dimension and doping profiles of the simulated device are listed in table 3.2.

Table 3. 2 Device dimension and doping profiles for the simulation

	Epi Layer	Buffer Layer	Substrate Layer
Doping density (cm^{-3})	1×10^{15} cm^{-3}	1×10^{18} cm^{-3}	1×10^{18} cm^{-3}
Thickness (μm)	4μm	1μm	30μm

3.2.3 Results and Discussion

The distribution of interface states is assumed to be uniform in the horizontal direction of the device. The simulated results are shown in Fig.3.9 for four different interface states densities: zero, 1×10^{10} cm^{-2}, 1×10^{11} cm^{-2}, 1×10^{12} cm^{-2} respectively.

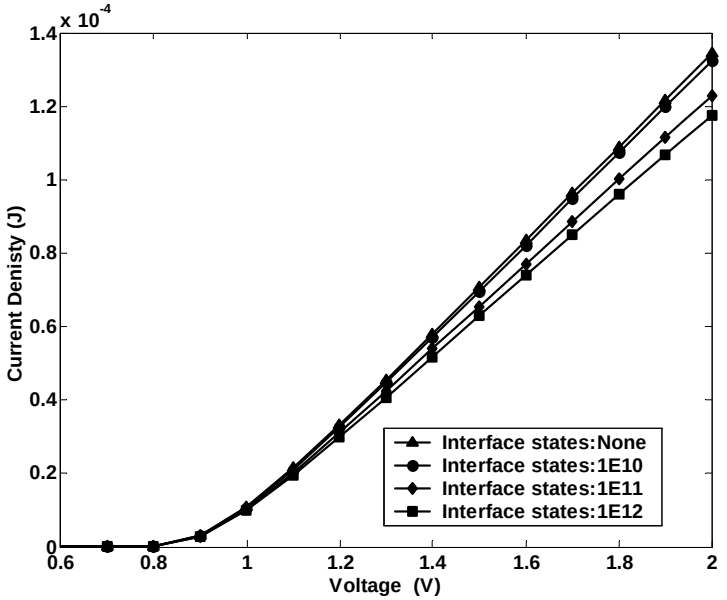


Fig.3. 9 Simulation results of SiC Schottky diode with different interface states

The degradation effect of interface states on the forward I-V characteristics of Schottky diodes was shown clearly in Fig.3.9. With increasing density of interface

states, the forward I-V characteristics of the simulated SiC Schottky diode were degraded. When the density of interface states is 1×10^{10} cm^{-2}, the current density of the SiC Schottky diodes is degraded by 1.27% at the 2V. Practically this effect can be ignored. The current value of the diode at 2V, however, will be decreased by 8.31% and 12.85% respectively when interface states were increased from 1×10^{11} cm^{-2} to 1×10^{12} cm^{-2}. If a 10% current density degradation at 2V is defined as the failure criteria of the Schottky diodes, the threshold interface states 5.2×10^{11} cm^{-2} can be obtained from the simulation.

In conclusion, we believe that interface states are one of main failure mechanisms responsible for the non-catastrophic failures of Schottky diode. Interface states are thermally activated and can be easily induced during long time device normal operation, and the characteristic can be degradation slowly. The effect of interface states can be modeled as an additional resistance in the diode circuit model as follows:

3.2.4 The modified diode equation

For a Schottky diode, the forward current–voltage characteristics with series resistance due to thermionic emission can be expressed as [39]:

$$I = I_s \exp\left[\frac{q(V_A - IR_s)}{nK_B T}\right] \quad (3.16)$$

Where V_A is the applied voltage, n is the ideality factor, R_s is the series resistance of the diode, K_B *is* the Boltzmann's constant, T *is* temperature, and I_s is the diode saturation current given by

$$I_s = A_{eff} A^* T^2 \exp(-q\phi_B / kT) \quad (3.17)$$

Where A_{eff} is the effective area of the diode, A^* is the Richardson constant, q is the electron charge, ϕ_B is the Schottky barrier height of the diode.

To determine diode parameters such n and R_s, an equation can be derived from (3.15)

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \quad (3.18)$$

Clearly a plot of $dV/dLn(I)$ versus I of diodes will give R_s as the slope and nkT/q as the y-axis intercept. From the intercept the ideality factor value will be extracted. The plot for the simulated SiC Schottky diode is shown in Fig.3.11in the following.

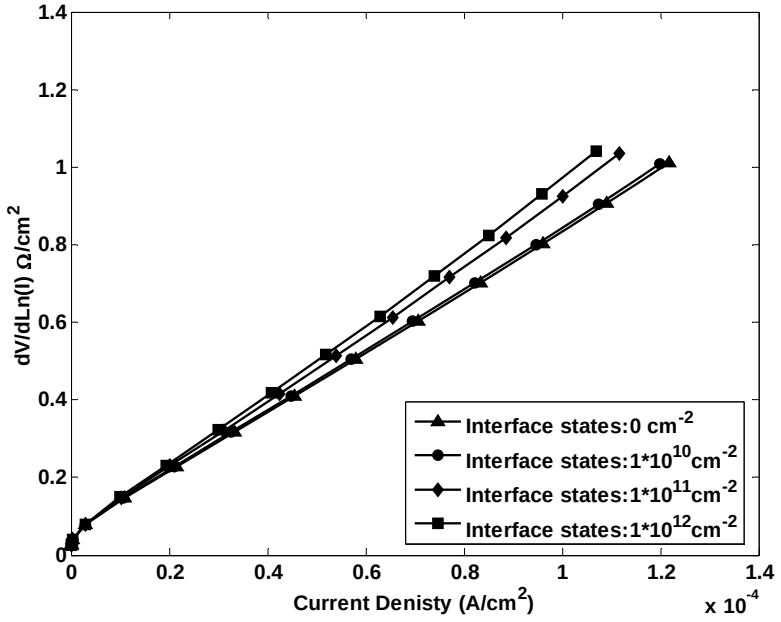


Fig.3. 10 The *dV/dLn(I)* versus *I* plot for the simulated Schottky diode

The series resistance values for different interface states are obtained from the slope of the plot. The values are 7.89×10^{3} Ω/cm^{-2}, 7.98×10^{3} Ω/cm^{-2}, 8.80×10^{3} Ω/cm^{-2} and 9.36×10^{3} Ω/cm^{-2}. An increase of 1.13%, 11.5% and 17.4% is observed when the density of the interface states is increased from zero to 1×10^{10} cm^{-2}, 1×10^{11} cm^{-2}, 1×10^{12} cm^{-2} respectively. We clearly see the result that the series resistance of the Schottky diode will increase with increased interface states.

Since the effect of interface state is purely resistive, a modified equation for Schottky diode is proposed:

$$I = I_s \exp\left[\frac{q(V_A - I(R_s + R_{it})}{nK_B T}\right] \quad (3.18)$$

Where R_{it} accounts for the resistance effect of interface states on the I-V characteristics of Schottky diode. The resistivity is given by:

$$\rho = \frac{1}{q\mu_n n} \quad (3.19)$$

Where q is electron charge, μ_n is electron mobility, and n is carrier concentration. A resistivity original from the interface is proposed

$$\rho_{it} = q\lambda_n N_{it} \quad (3.20)$$

Where λ_{it} describes the effectiveness of the interface state in capturing an electron. An equivalent circuit model is plot in Fig.3.12

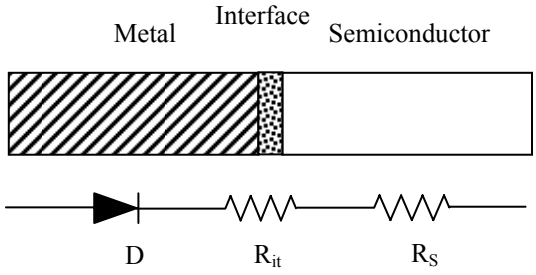


Fig.3. 11 A modified equivalent circuit model for Schottky diode

Chapter 4: Failure Mechanisms Investigation for SiC Power MOSFETs

In this chapter, two important failure mechanisms: single-event burnout (SEB) and single-event-gate rupture (SEGR) have been investigated for SiC power MOSFETs by two dimensional simulations. The drift-diffusion model is still the basis of simulation. Unlike the static-state simulations conduced for the DC characteristic simulation for SiC Schottky diodes in the previous chapter, transient simulations are required to simulate the SEB and SEGR failures. We will begin with the SEB failure mechanism investigation for SiC power MOSFETs

4. 1. Two-dimensional simulation study of the single-event burnout for SiC Power MOSFETs

4.1.1 Introduction

Single-event burnout (SEB) is one of the failure mechanisms triggered by heavy ions when power MOSFETs are used in radiation environments. As shown in Fig.4.1, a SEB failure is initiated when heavy ions strike through a power MOSFET biased in its OFF-state. The electron-hole pairs are generated along the ion impact track. A transient current is then generated inside the power MOSFET due to the influence of the electric field formed by the drain and source voltage, where holes

flow up towards source via the lateral p-base region and electrons toward drain. This current generates a voltage drop along the p-base region of the inherent NPN (The n^+-source/p-base/n-drift) parasitic bipolar junction transistor (BJT) within the power MOSFET. Once this voltage drop is larger than a threshold value, the parasitic BJT in the power MOSFET will be turned on. Due to a regenerative feedback mechanism in the BJT, high current and voltage will occur in the device, trigger the second breakdown of the power MOSFET and destroy the device [42]. The SEB failure has been studied extensively for Si power MOSFET in 1990s [42]~[46].

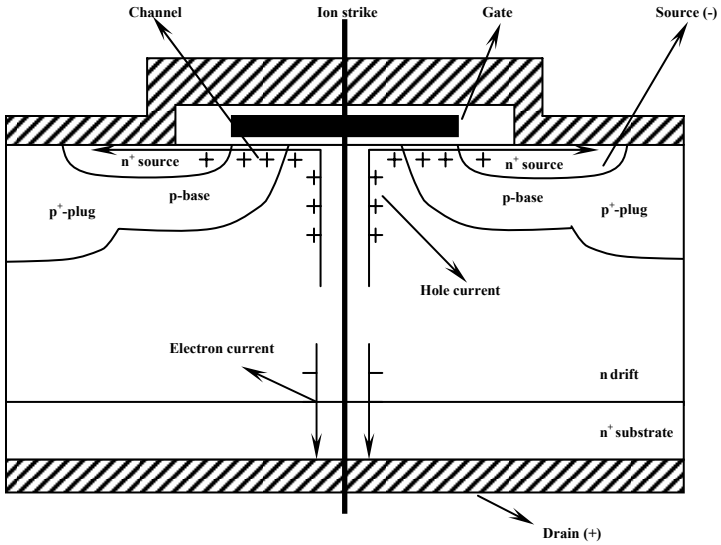


Fig.4. 1 The SEB failure in an n-type power MOSFET

In recent years, SiC has received great attention because of its potential applications in high temperature, high power, high frequency, and radiation environments. It is important to investigate the SEB failure mechanism of SiC power MOSFETs under radiation conditions and compare it with traditional Si power

MOSFETs. However, few investigation of the SEB in SiC power MOSFETs has been reported. In this study, detailed two-dimension simulations of the single-event burnout (SEB) were conduced to study the SEB failures occurred in SiC power MOSFETs [41]. A comparison was made between the SEB failures happened in SiC power MOSFETs and Si power MOSFETs to show the different robustness of the devices against SEB failures.

4.1.2 SEB threshold current density for SiC and Si power MOSFET

A detailed review of the SEB Models for power MOSFETs was reported in [46]. The current-induced avalanche model (CIA) is one of the models explaining the SEB failure mechanism based on the current-induced avalanche in the collector of the parasitic BJT (the drain of the power MOSFET): After the ion injection, a transient current is generated and instantly increased within the power MOSFET. With the partially turn-on of the inherent parasitic BJT, the location of the maximum electric field inside the device is redistributed and shifted from the n^+-source/p-base junction to the n-drift and n^+-substrate interface close to the drain region. This process is also known as the base pushout phenomena of bipolar transistors under high current injection. This maximum electric field continues to increase at the n-drift and n^+-substrate interface with the increased current. Since the impact ionization rate α inside the device is exponentially related to the local electric field, the α decreases significantly at the n^+-source/p-base junction and increases at the n-drift and n^+-substrate interface as the peak electric field inside the device is redistributed [47].

When this high impact ionization rate occurs at in the n-drift and n^+-substrate interface, a large amount of holes are injected into the base region. The n^+-source/p-base junction will then be forwarded, meanwhile the n^+-source also injects electrons across the p-base region into the high field drain region where more avalanching and subsequent injection occurs. Once this regenerative feedback mechanism is initiated, the parasitic BJT will be fully turned on and trigger the SEB failure.

The threshold current density J_c at which the peak electric field changes from the n^+-source/p-base junction to the n-drift and n^+-substrate interface is given by [46]:

$$J_c = qv_s[N_n + 2\varepsilon V_{ds}/(qW_n^2)] \quad (4.1)$$

Where q is the electronic charge, v_s is the electron saturation velocity, N_n is the ionized doping concentration in the epi-region, V_{ds} is the applied drain and source voltage, ε is the permittivity of device material, and W_n is the epi-region thickness.

The electron saturation velocity v_s is 2.2×10^7 cm/s at room temperature for 4H-SiC and 1×10^7 cm/s for Si. The relative dielectric constants ε_s for 4H-SiC and Si are 9.66 and 11.7 respectively. Applying these data with the doping density N_n and thickness of epi-region W_n extracted from the simulation results (assume complete ionization and a thickness of 12μm epilayer) to equation (4.1), the calculated threshold current density J_c is 1.4×10^4 A/cm^{-2} for SiC power MOSFET and 6.5×10^3 A/cm^{-2} for Si power MOSFET respectively. This higher threshold current density J_c of SiC power MOSFET is mainly originated from the doubled electron saturation

velocity. The higher threshold current density J_c indicates that SiC power MOSFET has a better capability against the SEB failures than Si power MOSFET. This can be verified by simulations in following sections.

4.1.3 Device simulation structure and physical models

A half-cell structure of the n-type power MOSFET shown in Fig. 4.1 is used in the simulation because of its geometry symmetry. The device mesh grid is shown in Fig.4.2. The width and height of the structure are 20μm and 18μm respectively. The oxide thickness is 300Å. The device doping file is plotted in Fig.4.3. The doping densities of n-drift, n^+ substrate and n^+ source regions are 3×10^{15} cm^{-3}, 1×10^{18} cm^{-3}, and 1×10^{20} cm^{-3} respectively. The doping densities of p base-region and p^+ region are 1.5×10^{17} cm^{-3} and 5×10^{19} cm^{-3}.

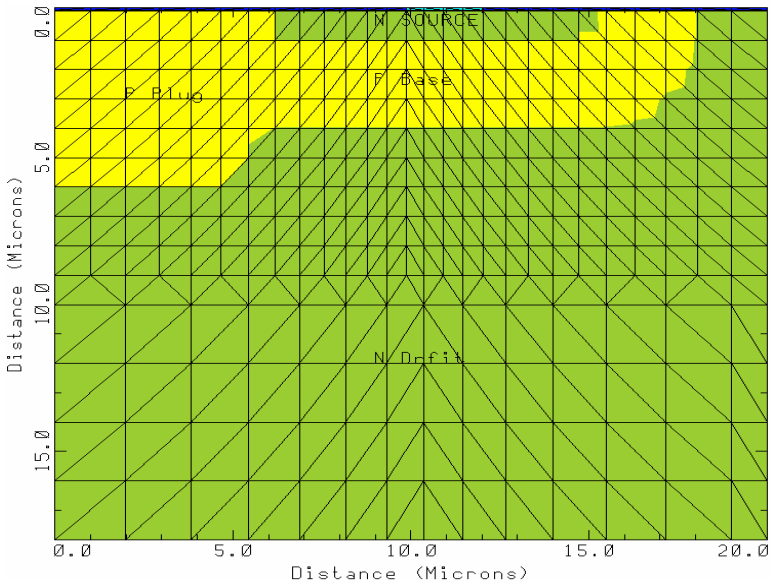


Fig.4. 2 The mesh grid of the simulated power MOSFET

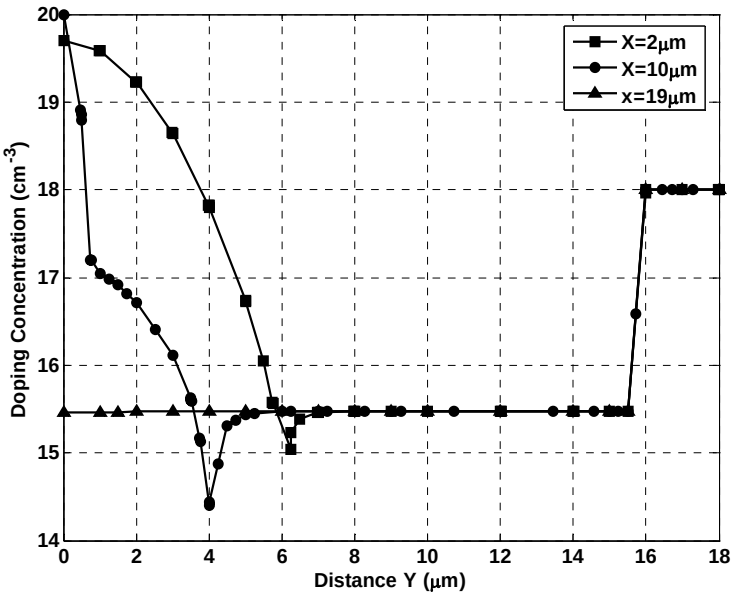


Fig.4. 3 The doping profile of the simulated power MOSFET

Various physics models for SiC power MOSFET are incorporated in the simulator as listed below in Table.4.1.

Table 4. 1 Physical Models for the 4H-SiC power MOSFET

Models	4H-SiC
Relative Dielectric Constant ε_s	9.66 [31]
Intrinsic Concentration n_i (cm^{-3} at 300K)	5.27×10^{-8} [18]
Bandgap Narrowing Model (eV)	$E_g(T) = 3.26 - 3.3\times10^{-4}(T-300)$ [18]
Low-field Mobility Model (cm^2/Vsec)	$\mu_n^{LF} = 947\times(T/300)^{-2}/[1+(N/1.94\times10^{17})^{0.61}]$ [22]
High-field Mobility Model (cm^2/Vsec)	$\mu_n^{HF} = \mu_n^{LF}/[(1+(\mu_n^{LF}\lvert E_{n,\parallel}\rvert/2\times10^7)^2)^{1/2}]$ [22]
Impact Ionization Model	$\alpha_{n,ii} = 1.66\times10^6\exp[-2.2\times10^7/E_{n,\parallel}]$ [22][24,25]
	$\alpha_{p,ii} = 5.86\times10^6\exp[-1.4\times10^7/E_{p,\parallel}]$ [22][24,25]
Carrier Life Time Model	$\tau_n = 1\times10^{-9}(T/300)^{2.5}/[1+(N/3.1\times10^{15})^{0.37}$ [22]
	$\tau_p = 6\times10^{-7}(T/300)^{2.5}/[1+(N/3.1\times10^{15})^{0.37}]$ [22]

Where E_g is the bandgap of the material, T is temperature, μ_n^{LF} and μ_n^{HF} are the low field and high filed electron mobility, N is the carrier doping density, $\alpha_{n,ii}$ and $\alpha_{p,ii}$ are the electron and hole impact ionization coefficients, $E_{n,||}$ and $E_{p,||}$ are the electric field components in the direction of current flow, and τ_n and τ_p are the lifetime of electrons and holes

4.1.4. Simulation Algorithm

To simulate the SEB failure in SiC power MOSFETs, a linear energy transfer (LET) file is needed to describe the energy loss of the ions when they pass through the device. A LET has the unit of MeVcm^2/mg where the ion energy loss per unit path length (MeV/cm) is normalized by the density of the device material (mg/cm^3). Thus a LET file is roughly independent of the impacted device material. A LET file can be generated by the computer TRIM and SRIM codes developed by Ziegler, *et al*. [48]. The LET file is related to the electron-hole pair generation rate in the continuity equation by

$$G_n(l,r,t), G_p(l,r,t) = L(l)\cdot R(r)\cdot T(t) \quad (4.2)$$

Where *L(l)* is a table of LET values as the function of length *l* read from the LET file, *R(r) and T(t)* describe the radial *r* dependence and time *t* dependence of the impacted carrier generation. In this study the radial dependence and time dependence are in Gaussian forms as shown in equation (4.3) and (4,4):

$$R(r) = \exp\left[-\left(\frac{r}{R.Char}\right)^2\right] \quad (4.3)$$

$$T(t) = \frac{2\exp\left[-\left(\frac{t-T_0}{T_c}\right)^2\right]}{T_c\sqrt{\pi}erfc\left(-\frac{T_0}{T_c}\right)} \quad (4.4)$$

Where *R.Char* is the characteristic radial distance of the charge generation, T_0 is the peak time of the Gaussian, T_C is the characteristic time of the charge generation pulse. The LET file used in the simulation is shown in Fig.4.4.

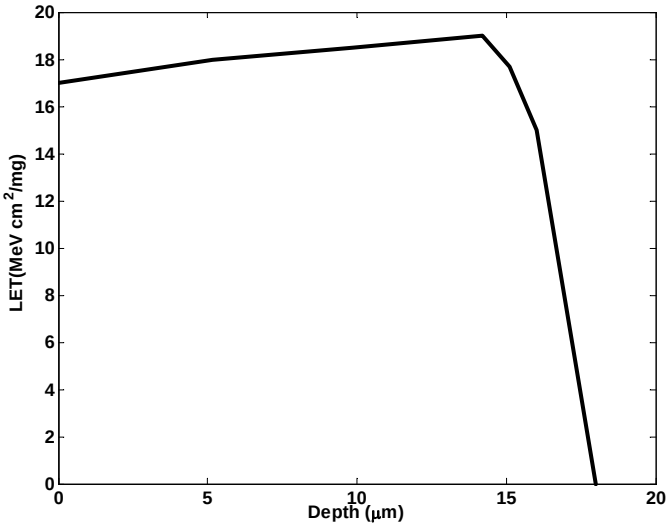


Fig.4. 4 The LET file used in simulation

A simple first-order (implicit) backward difference formula (BDF1) has been used in the program for the transient simulation where the continuity equations (2.13) and (2.14) are discretized as follows:

$$\frac{n_k - n_{k-1}}{\Delta t_k} = F_n\left(\psi_k, n_k, p_k, \mu_{n,k}, \mu_{p,k}, T_k\right) = F_n(k) \quad (4.5)$$

$$\frac{p_k - p_{k-1}}{\Delta t_k} = F_p\left(\psi_k, n_k, p_k, \mu_{n,k}, \mu_{p,k}, T_k\right) = F_p(k) \quad (4.6)$$

$$\frac{n_k \mu_{n,k} - n_{k-1}\mu_{n,k-1}}{\Delta t_k} = F_{u_n}\left(\psi_k, n_k, p_k, \mu_{n,k}, \mu_{p,k}, T_k\right) = F_{u_n}(k) \quad (4.7)$$

$$\frac{p_k \mu_{n,k} - p_{k-1}\mu_{p,k-1}}{\Delta t_k} = F_{u_p}\left(\psi_k, n_k, p_k, \mu_{n,k}, \mu_{p,k}, T_k\right) = F_{u_p}(k) \quad (4.8)$$

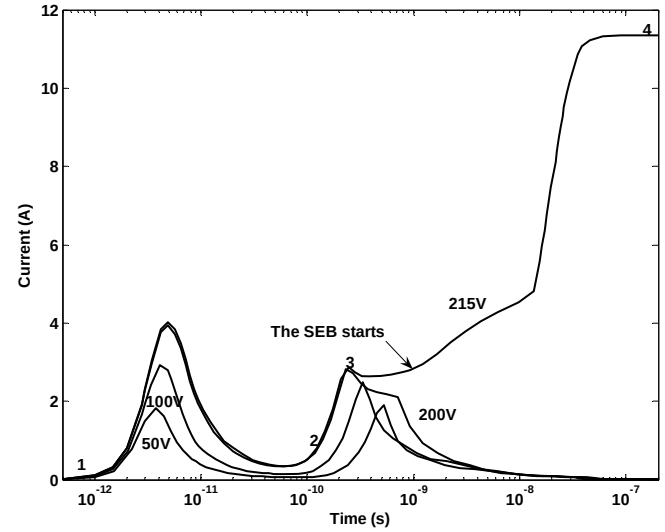
$$\frac{T_k - T_{k-1}}{\Delta t_k} = F_T\left(\psi_k, n_k, p_k, \mu_{n,k}, \mu_{p,k}, T_k\right) = F_T(k) \quad (4.9)$$

Where $\Delta t_k = t_k - t_{k-1}$ and ψ_k denotes the potential at time t_k, and so on. This scheme (also known as the backward Euler method) is a one-step method and is known to be both A- and L-stable. The disadvantage is that it suffers from a large local truncation error (LTE) which is proportional to the size of the time steps taken. As an alternative to BDF1, a second-order backward difference formula (BDF2) could also be used in the simulation program [49].

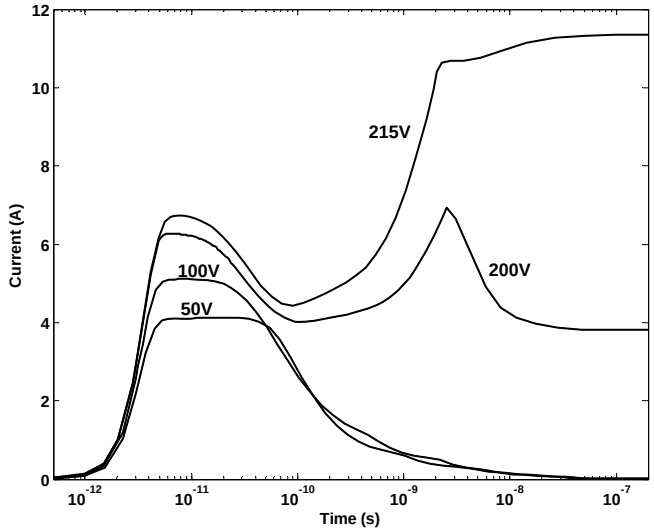
4.1.5 Results and discussion

Different simulations were conducted for the SiC power MOSFET while the SiC power MOSFET was held in its OFF-state (V_{GATE} was set at zero). The simulations were first implemented to obtain the SEB threshold drain-source voltage

of the device. With the same LET file, the simulations were performed at different locations of the device under different drain-source voltages (V_{DS}). The results are shown in Fig.4.5.



(a)



(b)

Fig.4. 5 Transient drain currents of the simulated SiC power MOSFET under different drain-source voltages at (a) The channel region: The Gate-Channel-N-drift region, (b) The source region: The N^+ source-P-base-N-drift region.

The transient drain currents of the simulated SiC power MOSFET are shown in Fig.4.5 under four different drain-source voltages (V_{DS}): 50V, 100V, 200V and 215V respectively. The ions were set to strike vertically through (a) the device channel region and (b) the device source region. The results show that the SEB threshold voltage is 215V at the channel region and 200V at the source region.

Different transient current behaviors are observed at the channel region and source region. When the ions passed through the device channel region, two current peaks were clearly observed in the current curves when V_{DS} was up to 200V. The first current peak was generated by carrier separations after the ions striking through the device. The second current peak happened between 0.23ns and 0.52ns depending on the applied voltage. The more higher the voltage was applied, the more earlier the second current peak happened. This current peak represents the partially turn-on of the parasitic BJT. However the current were not large enough to be self-sustained and fell off to zero when the V_{DS} was lower than 215V. The SEB failure happened in the SiC power MOSFET when V_{DS} reached 215V where the current continuously increased after the second current peak showing the fully turn-on of the parasitic BJT. When the ions passed through the device source region, however only one current peak was observed in Fig.4.5 (b) before the SEB failure happened where the V_{DS} was up to 150V. This is because the ions directly strike through the region where the parasitic bipolar transistor is located (the N^+ source-P-base-N-drift region), the transient current was the sum of the ion current and the current generated by the parasitic bipolar transistor. The SEB failure was observed once the V_{DS} reached

200V when the parasitic bipolar transistor was fully turned on and the SEB failure started.

The simulations were also conducted at the device p^+-plug region. No SEB failure was observed. The transient currents at different locations under the 215V V_{DS} are shown in Fig.4.6.

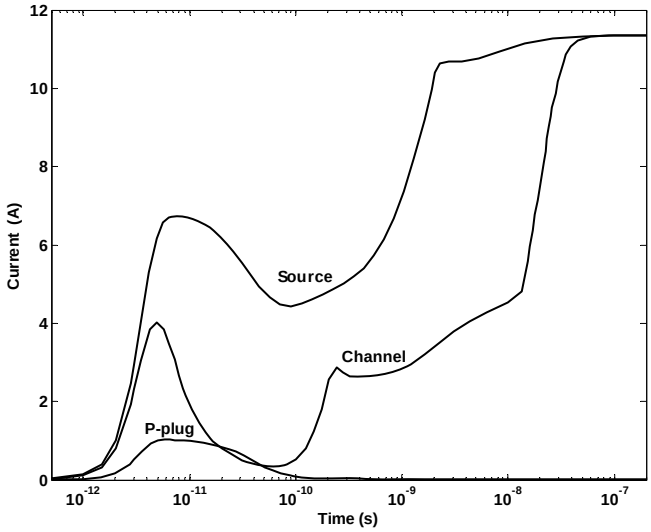


Fig.4. 6 Transient drain currents at different impact positions for SiC power MOSFET

Apparently the results shown in Fig.4.6 indicate that the device source region is the most sensitive region for the SEB failure since it is the region where the parasitic bipolar transistor is located, and the p^+-plug region is the most insensitive region. Although there is a difference between the SEB threshold voltages at the channel region and source region, the value is very small and can be ignored. This is because the ion current generated at the channel region has to leak though the source region later on and turn on the parasitic bipolar transistor in the same way as the ions

strike directly on the source region. Thus it is reasonable to assume the SEB sensitivity is the same at device source region and channel region.

The similar simulations were performed again for a Si power MOSFET having the same device structure, doping profiles as shown in Fig.4.2 and Fig.4.3. Si physical parameters and models are default built in the software. A SEB threshold voltage 75V was obtained for this Si power MOSFET to trigger the SEB failure by using the same LET file. A comparison between the simulated SiC and Si power MOSFET was made in Fig.4.7 under V_{DS}=75V. The transient current of the SiC power MOSFET only showed a partially turn-on of the parasitic BJT and vanished after the second current peak at V_{DS}=75V. The SEB failure, however, easily happened in Si power MOSFET as shown in Fig.4.1.7. The drain current of the Si power MOSFET started to increase after the first current peak, without showing the second current peak.

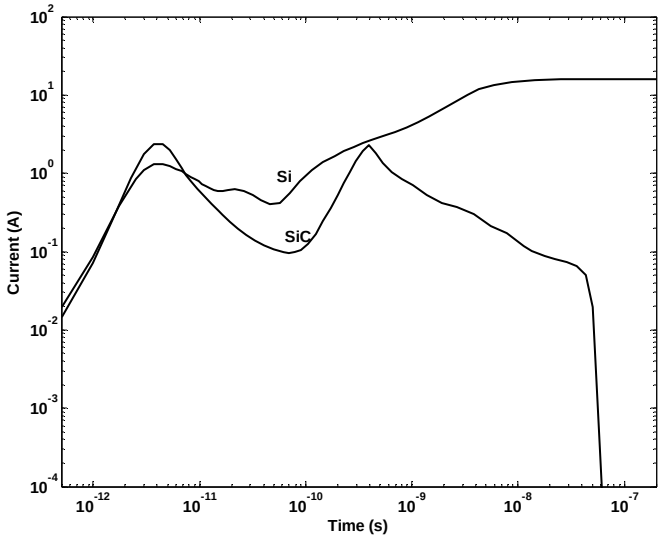


Fig.4. 7 The comparison of Si and SiC power MOSFSET SEB sensitivity at V_{DS}=75V

Fig.4.8, Fig.4.9 and Fig.4.10 clearly show how SEB happened in the SiC power MOSFET under 215V V_{DS}. Just as described in the introduction, the internal device physic changes inside the device are plotted corresponding to the points 1,2,3,4 shown in Fig.4.5 (a) before and after the SEB failure. The maximum electric field shifted from the n^+-source/p-base junction to the n-drift and n^+-substrate interface as shown in Fig.4.8. The electric field between n^+ source, p-base region, and n-drift region is completely disappeared after the SEB happened.

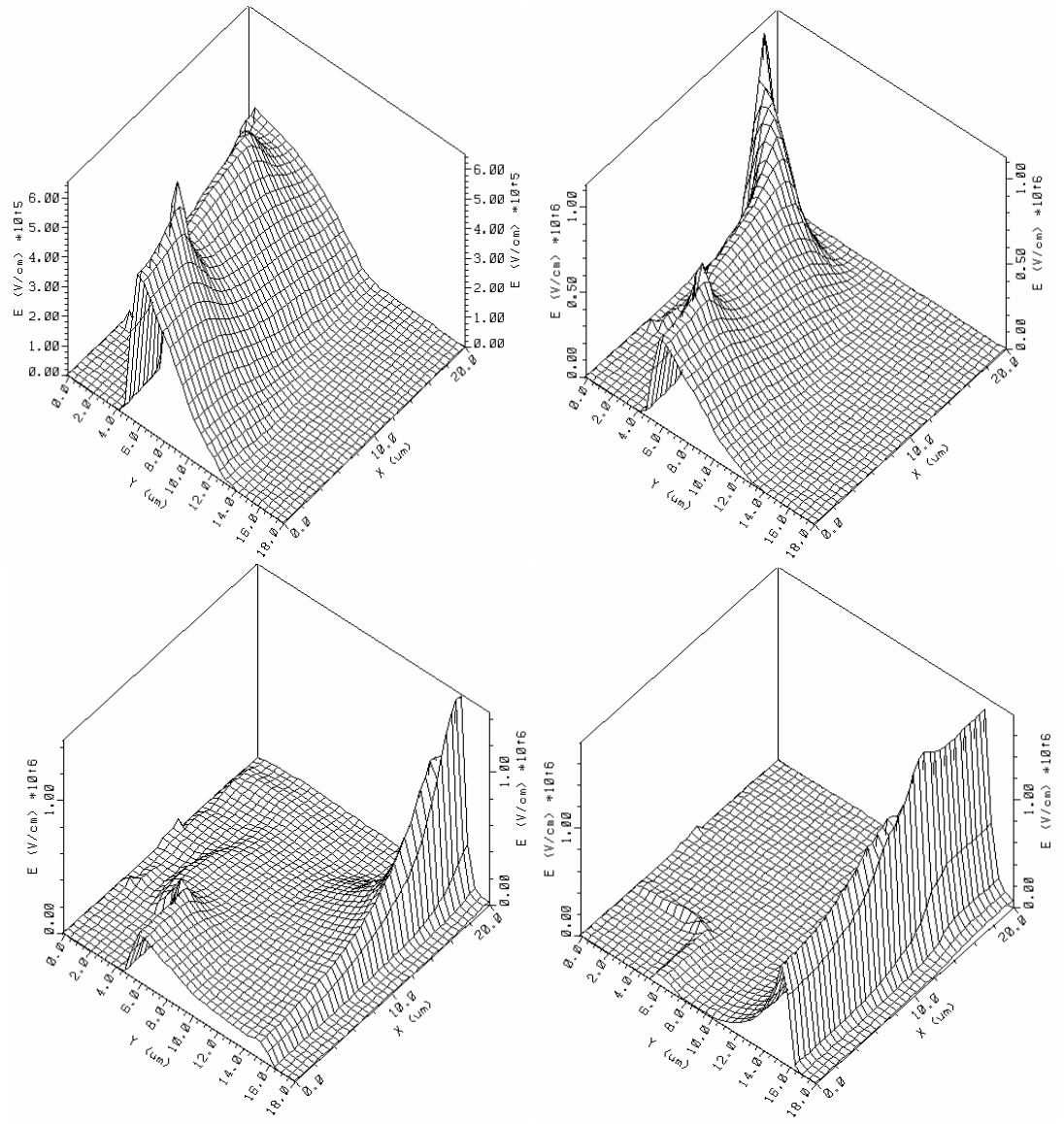


Fig.4. 8 Electric field evolution inside SiC power MOSFET before and after the SEB

The current flowlines in Fig.4.9 shows the activation of the parasitic BJT. The current first flowed though the channel region normally. However after the SEB failure, the current path was totally shifted to the path along the n^+-source/p-base/n-drift region which indicated the fully turn-on of the parasitic bipolar transistor and the device lost its MOS gate control. The potential contours within the device are shown as the horizontal dash lines. The interval of two lines indicates a 20V-difference of the potentials. The potential contours were shrunk to the n-drift/n^+-substrate interface indicating the maximum electric field redistribution within the device.

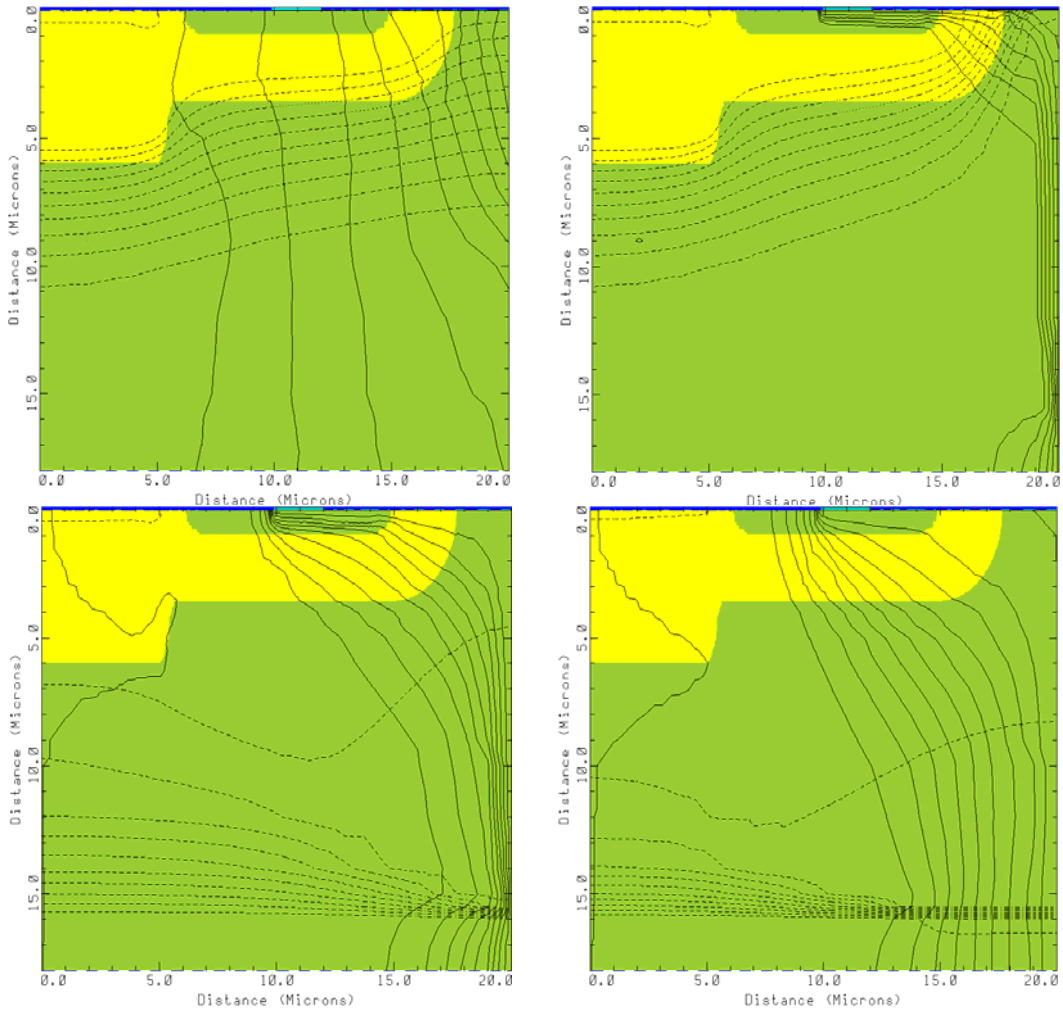


Fig.4. 9 Equipotential lines (horizontal dash line) and current flow lines (Vertical dark line) inside the device before and after the SEB

The large magnitude change of the maximum impact ionization rate α is observed in Fig.4.10. The impact ionization rate α was increased from around 700/(cm^3·s) to 1.2×10^{28}/(cm^3·s) resulting in the high carrier injection happened within the device. As introduced above, it is the result of the inside maximum electric field shifting.

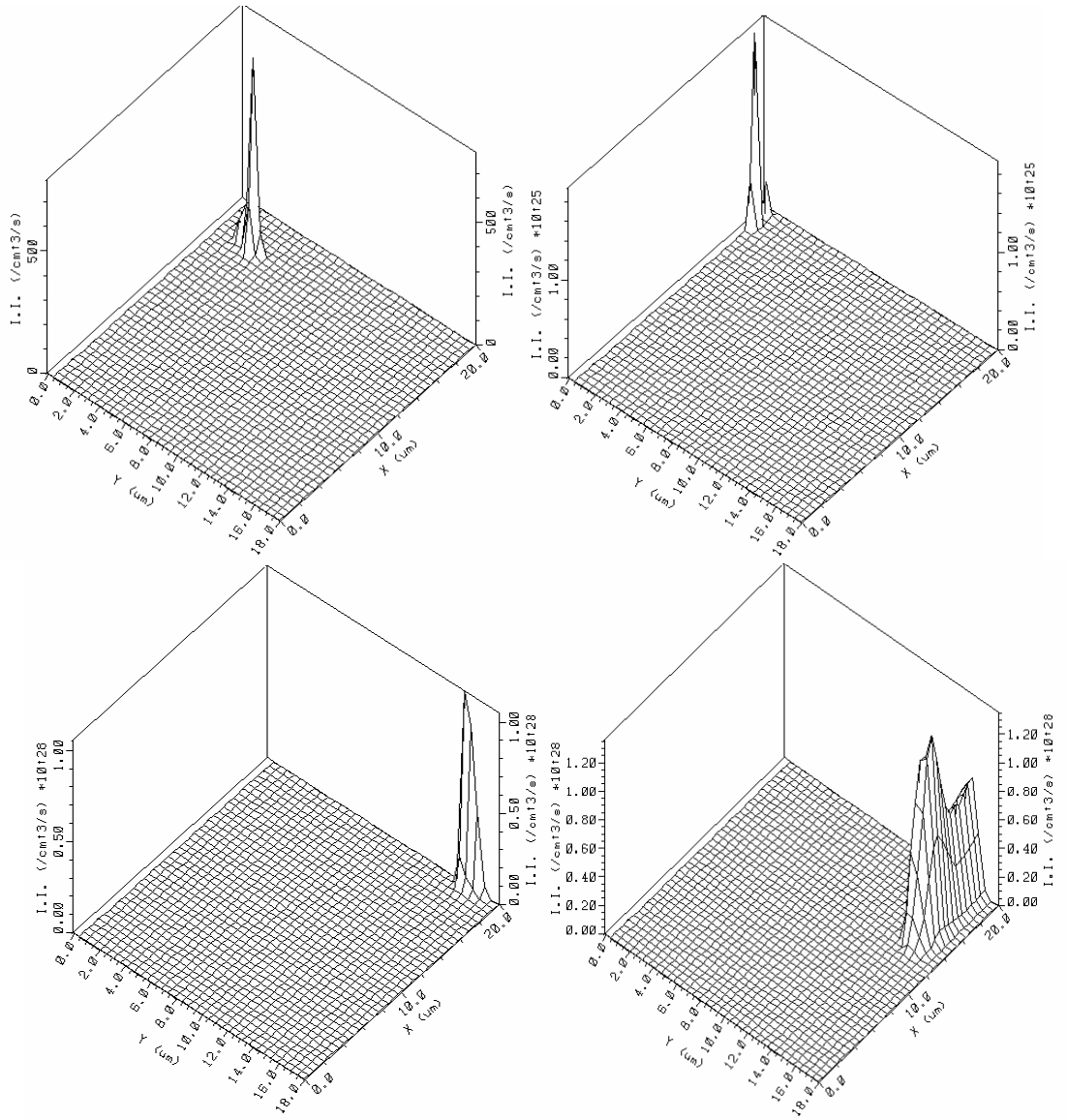


Fig.4. 10 Impact ionization generation rate of the device before and after the SEB

The turn-on of the parasitic bipolar transistor was further verified by the hole concentration change within the device before and after the SEB as shown in Fig.4.11. The minimum hole concentration (red color region) plotted in the figures is 1×10^{14} cm^{-3}. Every color change implies a10 times increase in the hole concentration.

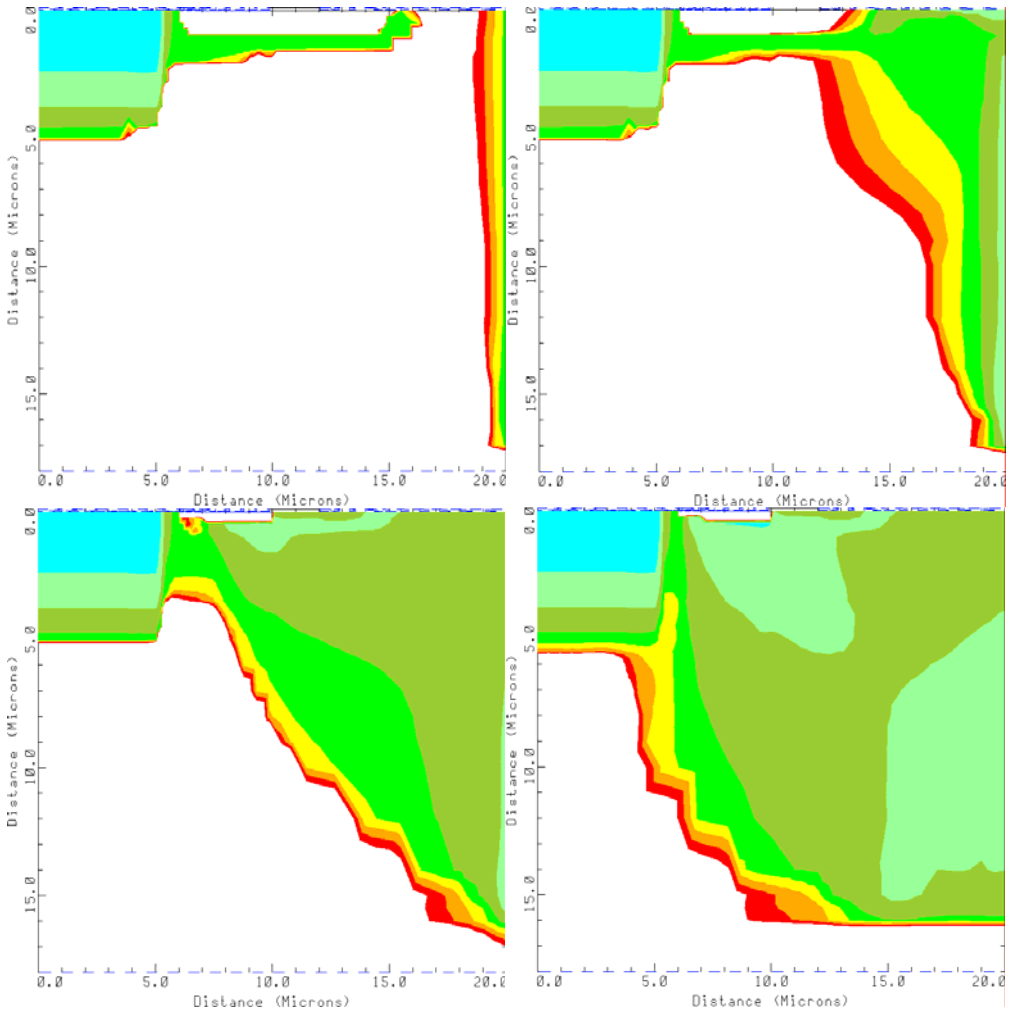


Fig.4. 11 The hole concentration change within the device before and after the SEB

In Fig.4.11, the holes are mainly limited in the p-plug, p-base region, and along the ion track. With the current leaking through p-base region, the high hole

concentration region along the ion track spreads out. The high hole concentration along the ion track is gradually shifted from the original ion track to the path along the n^+ source, p-base and n-drift region which indicates that the SEB failure inside the device.

The comparison above was made between the SiC power MOSFET and the Si power MOSFET where they have an identical geometry and doping profiles. However they have a 10 times block voltage difference because of the different critical electrical filed E_c of the material (SiC: 2.2×10^6 V/cm, Si: 2.5×10^5 V/cm) according equation (3.1). Since one of the advantages of SiC is much smaller device dimension need for the same voltage rating requirement, it is very important to compare the performance of SiC power MOSFET and Si power MOSFET with a same blocking voltage. To do this comparison, the new SiC power MOSFET scaling down from the same voltage rating Si MOSFET needs to be made first. The device scaling factors from Si to SiC are derived as follows. First, the width ratio of SiC and Si drift region is given by

$$\frac{W_{SIC}}{W_{SI}} = \frac{\sqrt{\frac{2\varepsilon_{sic}(V_{sic-bi}-V_R)}{qN_{sic-d}}}}{\sqrt{\left(\frac{2\varepsilon_{si}(V_{si-bi}-V_R)}{qN_{si-d}}\right)}} \quad (4.9)$$

Where $N_{si\text{-}d}$ and $N_{sic\text{-}d}$ are the doping densities of the *N*-drift regions, V_R is the reverse bias applied to the *PN* junction. Since usually V_R is much larger than the build-in voltage V_{bi}, it is reasonable to assume that

$$V_{sic-bi} - V_R \approx V_{si-bi} - V_R$$

Then we have

$$\frac{W_{SiC}}{W_{Si}} = \sqrt{\frac{\varepsilon_{sic-s} N_{si-d}}{\varepsilon_{si-s} N_{sic-d}}} \quad (4.10)$$

$$N_{sic-d} = \left(\frac{W_{Si}}{W_{SiC}} \right)^2 \frac{\varepsilon_{sic-s}}{\varepsilon_{si-s}} N_{si-d} \quad (4.11)$$

Then for the same blocking voltage, the width and doping scale factors K_{width} and K_{doping} are obtained from equations (3.1) and (4.11) respectively:

$$K_{width} = \frac{W_{Si}}{W_{SiC}} = \frac{E_{c-SiC}}{E_{c-Si}} \quad (4.12)$$

$$K_{doping} = \frac{N_{sic-d}}{N_{si-d}} = \left(\frac{W_{Si}}{W_{SiC}} \right)^2 \frac{\varepsilon_{sic-s}}{\varepsilon_{si-s}} \quad (4.13)$$

With the ratios of $E_{c\text{-}sic}/E_{c\text{-}si}= 2.2\times10^6/2.5\times10^5=9$ and $\varepsilon_{sic}/\varepsilon_{si}=9.66/11.9=0.8$ the scaling factors k_{width} and k_{doping} are calculated as 9 and 63 respectively.

Using the scaling factors k_{width} and k_{doping} derived above, an equivalent voltage rating SiC power MOSFET has been scaled down from the Si power MOSFET structure and doping described in section 4.1.3. The n-drift doping density is calculated as 1.9×10^{17} cm^{-3} according equation (4.13). The scaled mesh grid of the new SiC power MOSFET is shown in Fig.4.12.

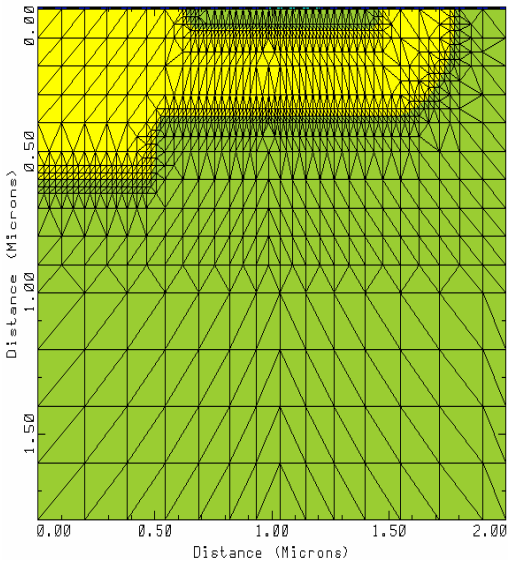
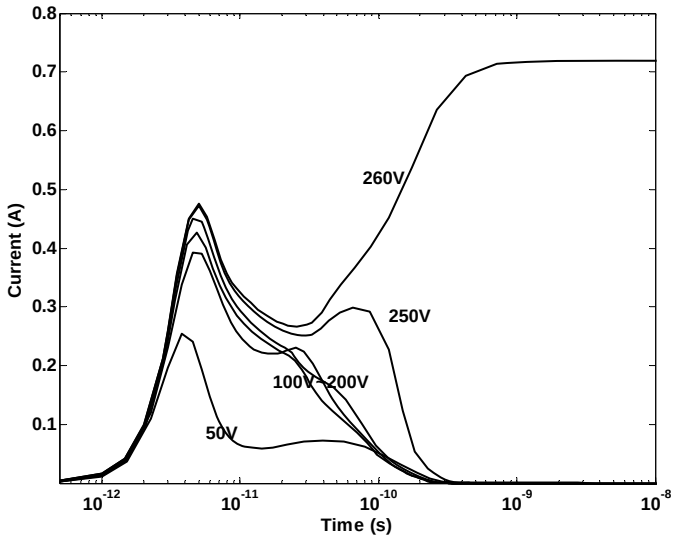
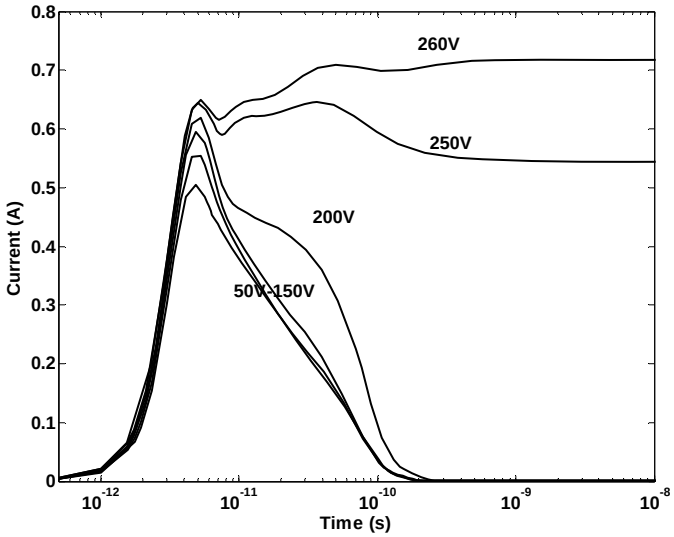


Fig.4. 12 The scaled mesh grid of the new SiC power MOSFET

Simulations were conducted for this new SiC power MOSFET to obtain the SEB threshold drain-source voltages as shown in Fig.4.13 and Fig.4.14. In Fig.4.13 the SEB threshold drain-source voltages 260V, 250V were obtained respectively where the ions strikes vertically through (a) the channel region (b) the source region.



(a)



(b)

Fig.4. 13 Transient drain currents of the new designed SiC power MOSFET under different drain-source voltages at (a) The channel region (b) The source region.

The SEB simulation results were replotted for the new SiC power MOSFET device under the drain source 250V as shown in Fig.4.14. The results verified again that that the most sensitive region is around the source region. No SEB failure was triggered at the p-plug region.

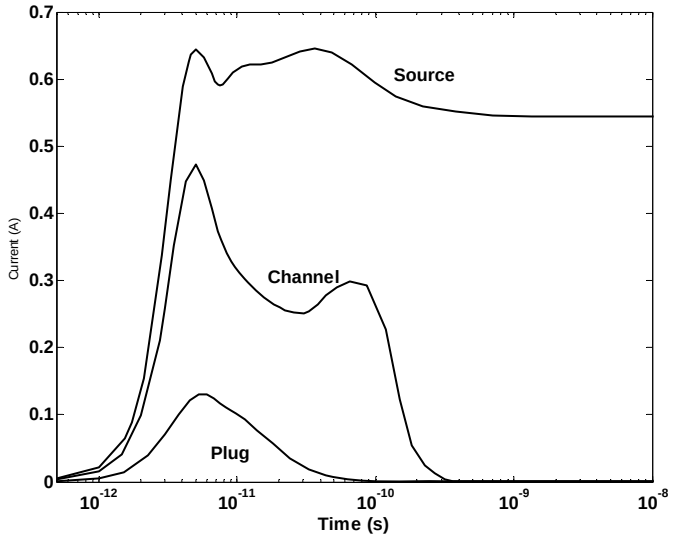
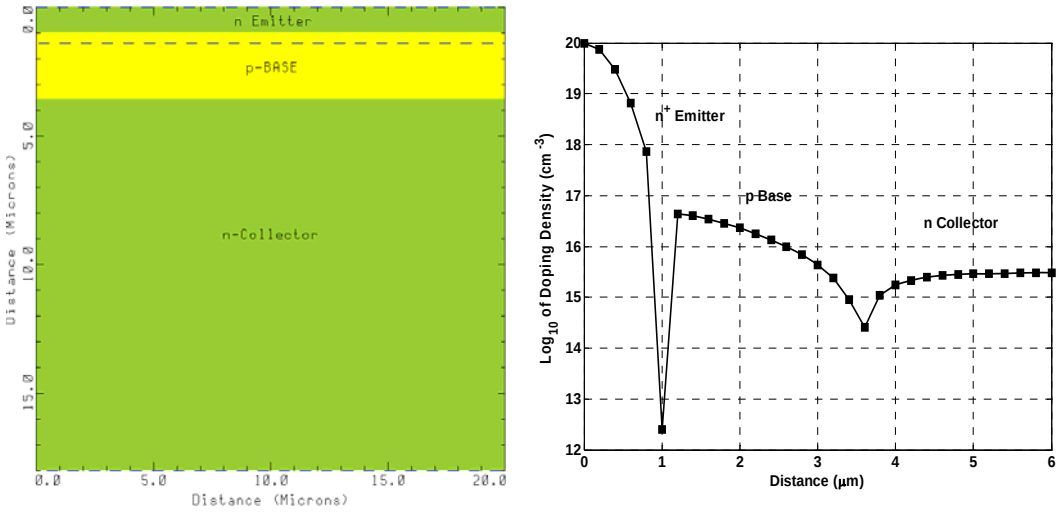


Fig.4. 14 Transient drain currents at different impact positions for the new SiC power MOSFET

Clearly the different radiation robustness of SiC power MOSFETs and Si power MOSFETs results from the different characteristics of the parasitic bipolar transistors within the device. It is very helpful to explain the difference between the SiC and Si power MOSFET failures if the behavior of the parasitic bipolar transistor can be further investigated. For this purpose, the parasitic n^+ source/p-base/n-drift transistor was extracted from the power MOSFET as shown in Fig.5.15. The device dimension and doping profiles are the same with the ones in the original MOSFET except the n^+-source and p-base here are extended as rectangular regions.

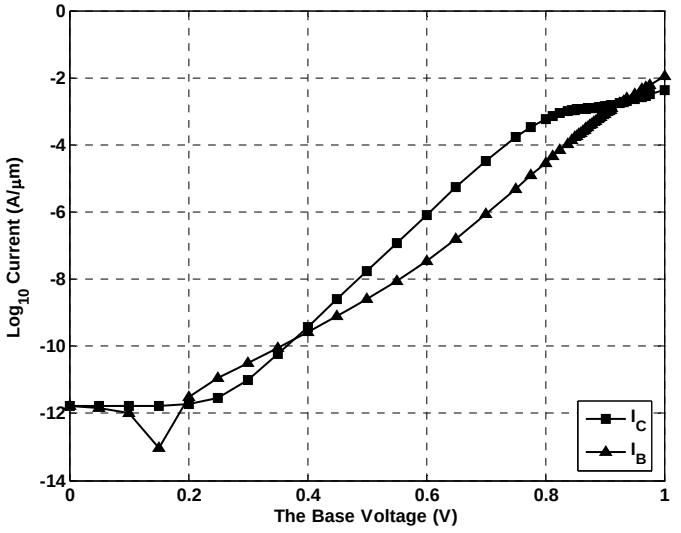


(a) (b)

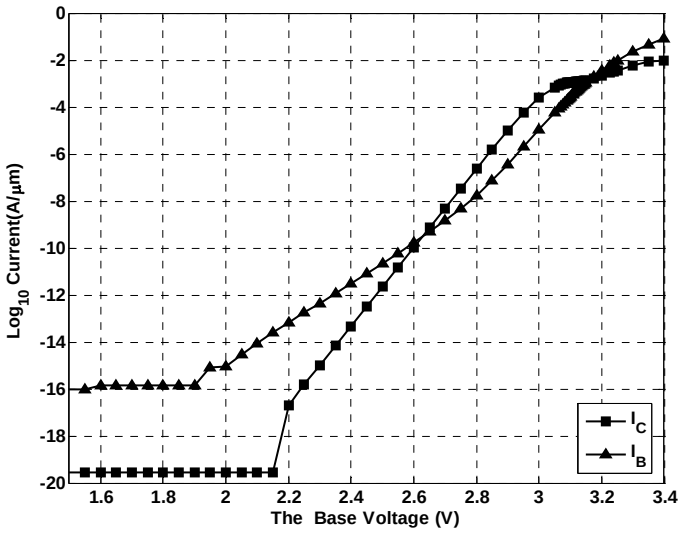
Fig.4. 15 The parasitic n^+ source/ p-base/n-drift transistor (a) structure and (b) doping profile

The I-V characteristics of the Si and SiC *NPN* transistors were obtained as shown in Fig.4.16, showing very different device behaviors. The Si *NPN* became active once the base voltage (V_{Base}) is larger than 0.4V, however, a 2.6V high base voltage is required to turn the parasitic SiC *NPN* transistor on. As shown in Fig.4.16

(a), and (b) this threshold base voltage is located at the point where the collector current (I_C) becomes larger than the base current (I_B).



(a)



(b)

Fig.4. 16 The IV Characteristics of the parasitic BJT in the power MOSFET (a) Si (b) SiC

The built-in potential of a *PN* junction is given by:

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right) \quad (4.14)$$

Where V_{bi} is the build-in potential of the *PN* junction, V_T is the thermal voltage, N_d and N_a are the donors and acceptors concentration of the *PN* junction respectively, and n_i is the intrinsic carrier concentration of the material which is 1.45×10^{10} cm^{-3} for Si and 5×10^{-8} cm^{-3} for SiC.

Assuming the doping profile is uniform in p-base and n^+ source region with a density of 7×10^{16} cm^{-3} and 1×10^{20} cm^{-3} respectively, the built-in potential ration is calculated as is calculated as 1.03V for this Si *PN* junction and 3.09V for SiC *PN* junction. The actual built-in potentials are lower that the calculated ones because of the Gaussian doping profiles. The build-in potential ratio between SiC and Si *PN* junction is calculated as 3 based on the results above. It is very interesting to notice that this ratio is almost same with the SEB threshold drain-source voltage ratio between SiC power MOSFET and Si power MOSFET which is also around 3 (215/75). This built-in potential different of the parasitic SiC and Si *PN* junction will well explain the robustness difference between SiC power MOSFET and Si power MOSFET.

The current gain β of the parasitic transistor can be obtained by taking the ratio of the collector current I_C and the base current I_B. The maximum current gain $\beta_{Si\text{-}max}$ and the average current β_{Si} of the Si parasitic *NPN* transistor were calculated as 39.7 and 20.5 respectively within the base voltage range of 0.4V~0.9V. In contrast, the maximum current gain $\beta_{SiC\text{-}max}$ and the average current β_{SiC} of the SiC parasitic *NPN* transistor were calculated as 28.2 and 11.5 respectively within the base voltage

range of 2.6V~3.1V. As a conclusion, the lower built-in potential, turn-on voltage and the higher current gain of the Si *NPN* parasitic transistor contributes the lower robustness of Si power MOSFET against the SEB failure compared to the SiC power MOSFET parasitic transistor when the ions strike through the device and active the parasitic bipolar transistor.

4.2 Two-dimensional simulation study of single-event gate rupture for SiC Power MOSFETs

Single-event gate rupture (SEGR) is another catastrophic failure mechanism of power MOSFETs. It happens when heavy ions penetrate the gate region of a power MOSFET. The electron-hole pairs generated along the path of the ions are separated under a positive drain bias as shown in Fig.4.17. Holes are driven toward the gate and the electrons flow toward the drain. Holes will accumulate at the Si-SiO_2 interface and induce an equal image charge at the other side of gate, resulting in a transient electric field increase across the oxide at the track position. If this increased field exceeds the critical oxide breakdown field E_{cr}, oxide breakdown occurs and results in a permanent short circuit through the oxide. This failure mechanism has been also studied extensively for Si power MOSFET in 1990s [7, 9~11, 13, 46, 50~52]. Different aspects about this failure mechanism have been reported in literatures including oxide thickness dependence, temperature dependence and ion threshold energy, etc. However, the SEGR failure investigation for SiC power

MOSFETs has not been seen in literatures. In this section SEGR failure mechanism is investigated for a SiC power MOSFET by two-dimensional simulations [41]. The device geometry, doping profile, LET file and physical models used in this simulation are the same as the ones used for the SEB study.

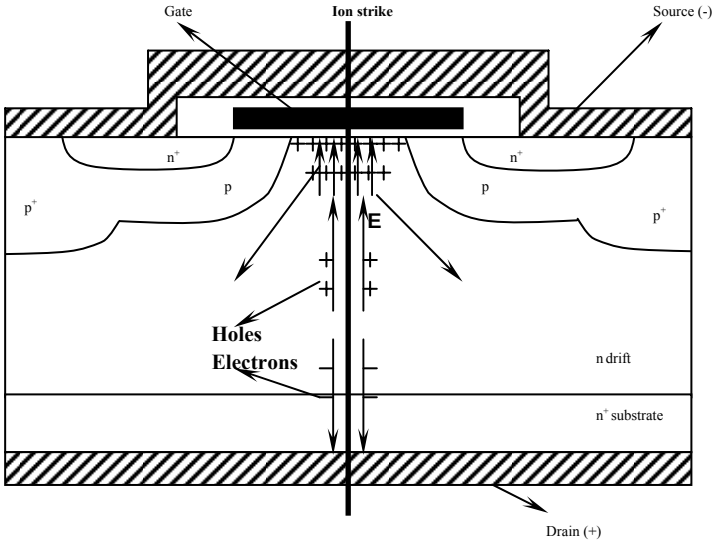


Fig.4. 17 SEGR of a power MOSFET

Results and discussion

Simulation results for the SiC power MOSFET were obtained under different the gate bias and drain bias combinations [50]. These bias values were obtained experimentally when SEGR occurred. Fig.4.18 shows the transient maximum vertical electric field in oxide versus time for the LET file. The first thing we notice that the electric field maintains a straight line when the drain-source voltage (V_{ds}) is zero. That is because an interfacial layer of holes is induced by the gate bias under the gate and results in that the field in oxide is independent from the field in

semiconductor under zero drain-source voltage. Without the vertical field generated by the drain-source voltage the electron-hole pair separation and hole accumulation under the gate area do not occur. The electric field is a constant value determined by V_{gs}/d_{ox} where d_{ox} is the thickness of the oxide. For all the cases of $V_{ds} \neq 0$, the transient electric field reached a value larger than the oxide critical electric field E_{cr} at around 3ps. The transient high electric field will reach its maximum value around 80~90ps. The transient lifetime of this high electric field is dependent on V_{ds} and lasted 0.7ns for $V_{ds}=30V$ and 1.7ns for $V_{ds}=10V$. Then it will decay to the pre-strike value as shown in Fig.4.18.

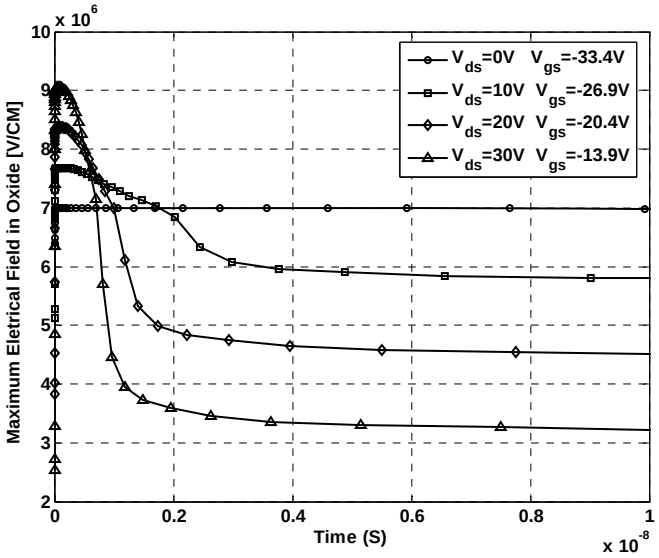


Fig.4. 18 The transient maximum vertical electric field in oxide versus time

The transient response comparison between the SiC power MOSFET and Si power MOSFET is shown in Fig.4.19 for V_{ds}=30V. The maximum electric field within the Si power MOSFET was only 3% lower than that of the SiC power MOSFET. This is because this electric field mainly depends on the oxide thickness

and the applied bias and is independent of the materials. For Si power MOSFET the transient high electric field reached its maximum point by 26ps in contrast to 84ps for the SiC power MOSFET. The lifetime of this transient high electric field was shorter for Si power MOSFET and lasted for 0.24ns. However the lifetime of that for SiC power MOSFET was 0.7ns instead as shown in Fig.4.19.

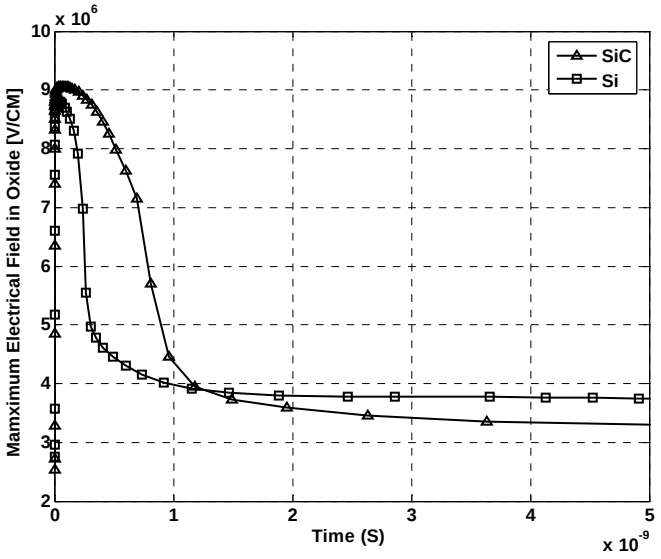


Fig.4. 19 The transient response comparison between SiC power MOSFET and Si power MOSFET

The transient source current response comparison between the SiC power MOSFET and Si power MOSFEST is plotted in Fig.4.20 on a log scale showing the difference between these two devices. For SiC the current surge peaked around 0.69ns and then decays to a very small value. However the current for Si power MOSFET quickly rose to a large current value and stabilized. This shows the turn-on of the parasitic BJT inside Si power MOSFET which causes the different behavior of SiC and Si power MOSFET during the SEGR failure.

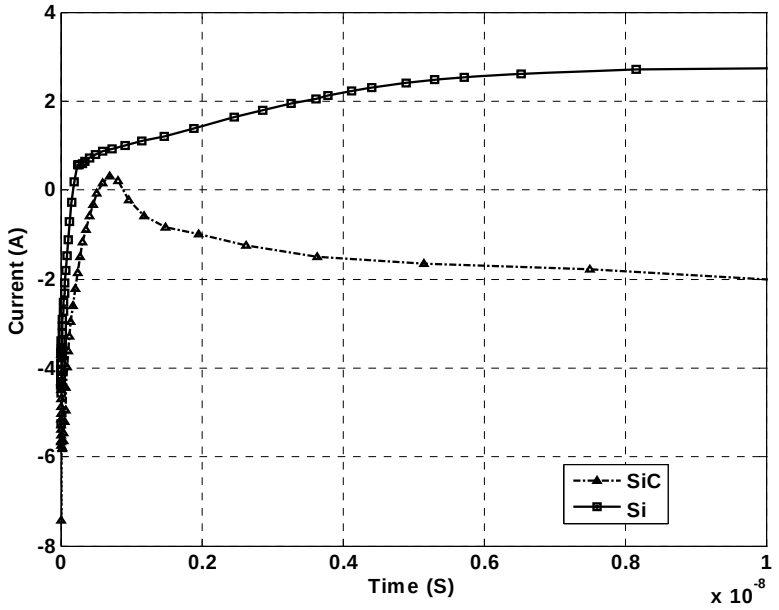


Fig.4. 20 The transient current response comparison between SiC power MOSFET and Si power MOSFET

We know that during the electron-pair separation process holes diffuse toward the p-body at a slower rate than holes drifting toward the interface and result in the hole accumulation phenomena. However in Si power MOSFET, under the bias condition of $V_{ds}=30V$, $V_{gs}=-13.4V$, the parasitic BJT was turned on and SEB failure occurred. So it will drag more holes and divert them to the source region than the SiC power MOSFET. This explains why the maximum value of the transient electric field in Si power MOSFET is lower than that of SiC power MOSFET since less holes accumulate at the interface of Si device. This also makes the lifetime for the transient high electric field inside Si power MOSFET shorter than SiC power MOSFET as shown in Fig.4.19.

As a conclusion, the SEGR failure behavior of SiC power MOSFETs is comparable to Si power MOSFET if the devices have the same oxide thickness and

applied bias. However SiC power MOSFET will be a better choice to used in radiation environment since it also has a strong resistance to SEB failures as shown in Fig.4.20.

Chapter 5 Failure Mechanism Investigation for SiC Insulated Gate Bipolar Transistors (IGBTs)

5.1 Introduction

As introduced in Chapter 1, IGBTs are one of important power devices widely used in power converter and motor drive applications. The basic cross-sections of a IGBTs were already shown in Fig.1.8. By combining the features of BJT and MOSFET, IGBTs have many desirable properties, such as MOS input gate, high switching speed, low conduction voltage drop, high current carrying capability and wide SOA. However latch-up failures are inherent in IGBTs because of the parasitic thyristor structure (*NPNP*) within the device. When the parasitic thyristor is turned on, the IGBT current will not be controlled by the MOS gate. The IGBT could be destroyed because of excessive power dissipation produced by the high current flowing through the device. The parasitic thyristor latch up can happen in IGBTs in two modes: static lat-up and dynamic latch-up. In the static mode, when the steady-state current density exceeds a critical value, the lateral voltage drop across the p-base region becomes greater than a threshold value. The parasitic *NPN* transistor (n^+-emitter, *p*-base and n-drift) and *PNP* transistor (*p*-base, n-drift, and n^+-substrate) shown in Fig.1.11 will be turned-on. Once the sum of the base transport factors of the *NPN*, *PNP* parasitic transistors becomes larger than 1 ($\alpha_{TNPN} + \alpha_{TPNP} \geq 1$), the parasitic thyristor (*NPNP*) will be turned on and the latch-up failure occurs. The

other latch up failure mode of the IGBT is called the dynamic latch up which means the latch up failure happens during switching conditions. In this work, the study is only focused on the static latch-up failure mechanism investigation.

As one of promising wide bandgap materials, SiC can contribute benefits in making IGBTs. High voltage rating IGBTs can be easily made from SiC with relatively small physical size. Compared to Si IGBTs, SiC IGBTs can operate at higher power levels and dissipate larger amounts of heat generated within the device with much higher thermal conductivity. (SiC: 3.0~3.8 W/cm· K vs. Si 1.5 W/cm· K). With all these good features, SiC IGBTs are expected to have a better capability than SiC IGBTs against latch-up failures. Thus a detailed simulation investigation of latch-up in SiC IGBTs is needed. In this chapter, the latch-up failure mechanism of IGBTs is illustrated first based on their equivalent circuit models. Then the simulation algorithm is introduced. Heat equations are added to modify the basic drift-diffusion models. Simulation results are presented and discussed at the end.

5.2 Latch-up failure mechanisms of IGBTs.

The basic failure principles of static and dynamic latch up were simply introduced in Chapter 1. An equivalent IGBT circuit model is plotted in Fig 5.1. This equivalent circuit consists of a coupled *PNP* and *NPN* transistor pair representing the four layer parasitic thyristor structure and a MOSFET shunting the

upper NPN transistor [17]. Also R_s denotes the resistance between the base and the emitter of the device.

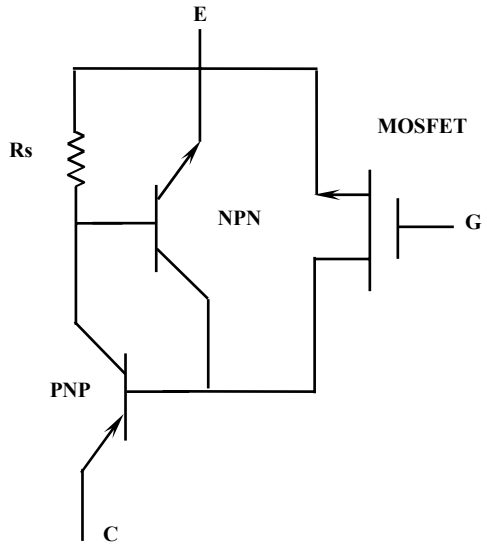


Fig.5. 1 Equivalent circuit of the IGBT

If the resistance R_s is small, the n^+ source/p-base junction will not become forward-biased during forward conduction. The upper *NPN* transistor can be assumed to be inactive and removed from the equivalent circuit. Then a bipolar transistor-*MOSFET* model is developed for IGBT forward conduction analysis as shown in Fig.5.2.

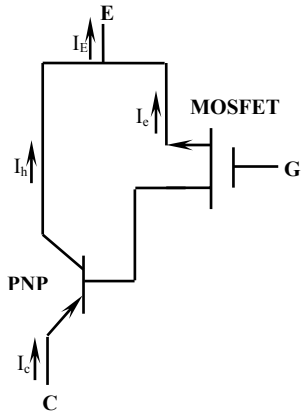


Fig.5. 2 The PNP/MOSFET equivalent circuit model of a IGBT

For a bipolar transistor, the transport factor α is defined as the ratio of the collector current $I_{Collector}$ and emitter current $I_{Emitter}$ which is a value smaller than 1; the current gain β is defined as the ratio of the collector current $I_{Collector}$ and base current I_{Base};

$$\alpha = \frac{I_{Collector}}{I_{Eitter}} \quad (5.1)$$

$$\beta = \frac{I_{Collector}}{I_{Base}} = \frac{\alpha}{1-\alpha} \quad (5.2)$$

The emitter efficiency γ_E of a bipolar transistor is defined as the effectiveness of an emitter junction in injecting electrons into the base which is given by:

$$\gamma_E = \frac{I_{nE}}{I_{nE} + I_{pE}} \quad (5.3)$$

Where I_{nE} and I_{pE} are the electron and hole current crossing the emitter-base junction which can be obtained through simulation results.

The base transport factor, α_T, which equals the ratio of the electron current injected in the collector to the electron current injected in the base, is related to the transport factor α above in the following equation:

$$\alpha_T = \frac{\alpha}{\gamma_E} \quad (5.4)$$

Considering the *PNP/MOSFET* equivalent circuit model shown in Fig.5.2, the electron current I_e flowing through the *MOSFET* channel (The base current) and the

hole current I_h (The collector current) flowing across the *PNP* bipolar transistor are related thought the transport factor of the wide-base *PNP* transistor:

$$I_h = I_e\left(\frac{\alpha_{PNP}}{1-\alpha_{PNP}}\right) \quad (5.5)$$

The current I_C in Fig.5.2 is related to the current I_h by:

$$I_h = \alpha_{PNP} I_C \quad (5.6)$$

During Latch-up, the voltage drop of the resistance R_s shown in Fig.5.1 can not be ignored because of the large conduction current density. The lateral hole current I_h will produces a forward bias through R_s across the n^+ source/*p*-base junction. Assuming the hole current I_h traverses under the entire p^+-base region, this forward voltage drop can be given by:

$$V_F = R_s I_h \quad (5.7)$$

With equation (5.2), we have

$$V_F = \alpha_{PNP} R_s I_c \quad (5.8)$$

Assume a forward voltage V_F is needed to active the Si N^+-*P* junction, the steady-state latch-up threshold current can be given by

$$I_C = I_{Latch-up} = \frac{V_F}{\alpha_{PNP} R_s} \quad (5.9)$$

For a bipolar transistor, since the γ_E value is very close to 1 in equation (5.4), the transport factor α_{PNP} is determined primarily by the base transport factor α_T which is given by [17]:

$$\alpha_T = \frac{1}{\cosh(W_L / L_a)} \quad (5.10)$$

Where W_L is the undepleted base width of the *PNP* transistor and L_a is the ambipolar diffusion length.

For the resistance R_s we have,

$$R_s \propto \rho_s L_E \quad (5.11)$$

Where ρ_s is the sheet resistance of the p-base, L_E is the length of the p-base region.

With equations (5.9), (5.10) and (5.11), a relationship between the latch-up threshold current $I_{latch\text{-}up}$, base transport factor α_T and N^+-emitter length L_E is given by

$$I_{Latch-up} \propto \frac{1}{\alpha_T \rho_s L_E} \quad (5.12)$$

From equation (5.12) we can see that a lower base transport factor α_T , sheet resistance ρ_s and shorter Length L_E will lead to a larger latch-up current $I_{latch\text{-}up}$. A latch up threshold current comparison between SiC IGBT and Si IGBT can be made based on this equation.

If a SiC IGBT and a Si IGBT have a same device geometry and doping profile, the undepleted base width W_L in equation (5.10) of the SiC IGBT will be always larger than that of the Si IGBT because of the much smaller depletion width W_D of the SiC IGBTs. This result stems from the big difference of the critical electric field E_c of SiC and Si as introduced before. Since the function *cosh(x)* is monotonously increase in the domain of $x>0$, then the base transport factor α_T of the SiC IGBT will be always smaller than the Si IGBT. This will lead to a larger latch-up threshold current for the SiC IGBT according equation (5.12).

For same voltage rating device, the physical size of the SiC IGBT will be much smaller than that the Si IGBTs including the parameter L_E. Thus a larger latch-up threshold current $I_{latch\text{-}up}$ for the SiC IGBT can be also derived from equation (5.12). So we can have a conclusion that the SiC IGBT will be more robust again the static latch-up failures than the Si IGBT. This fact is further verified by the simulations introduced in the following sections where the simulation algorithms will be introduced in 5.3 and results and discussion in 5.4.

5.3 Simulation Algorithms

As one kind of power devices, heat generation and power dissipation are always the concerns for IGBTs. During its normal operation, the temperature inside the IGBT is very high and the temperature distribution is not uniform. Thus the

simulation must have the capability to simultaneously solve the electrical and thermal equations and perform nonisothermal electrical analysis. To compute the spatially dependent lattice temperature, the heat flow equation is used

$$\rho c \frac{\partial T}{\partial t} = H + \vec{\nabla}\left(\lambda(T)\vec{\nabla}T\right) \quad (5.13)$$

Where ρ is the mass density of the material (g/cm^3), c is the specific heat of the material (J/g-K), H is the heat generation term (W/cm^3), λ is the thermal conductivity of the material (W/cm-K), and T is the lattice temperature. The heat generation term is modeled by:

$$H = H_n + H_p + H_R \quad (5.14)$$

Where H_n is the lattice heating due to electron transport, H_p is the lattice heating due to hole transport, and H_R is the lattice heating due to carrier recombination and generation. They are given by:

$$H_n = \vec{J}_n \cdot \vec{E} \quad (5.15)$$

$$H_p = \vec{J}_p \cdot \vec{E} \quad (5.16)$$

$$H_R = U_{SRH}\left(E_g + 3kT\right) \quad (5.17)$$

Equation (5.17) specifies that each recombining carrier pair transfers $3kT_{Lattice}$ Joules to the lattice in addition to the gap energy E_g.

The basis semiconductor equations introduced in chapter 2 need to be modified to take into account of the effect of lattice temperature as follows.

Poisson's Equation

$$\vec{\nabla}^2(\phi-\theta)-\frac{q}{\varepsilon}\left(n-p+N_a^- - N_d^+\right)=0 \quad (5.18)$$

Where θ is the band structure parameter for the material and is given by

$$\theta=\chi+\frac{E_g}{2q}+\frac{kT}{2q}\ln\left(\frac{N_c}{N_v}\right) \quad (5.19)$$

Current drift-diffusion Equations

$$\vec{J}_n=qn\mu_n\vec{E}+k\mu_n\left(T\vec{\nabla}n+n\vec{\nabla}T\right) \quad (5.20)$$

$$\vec{J}_p=qn\mu_p\vec{E}-k\mu_p\left(T\vec{\nabla}p+p\vec{\nabla}T\right) \quad (5.21)$$

In this work, the simulation was conducted by using *the lattice temperature advanced application module* provided by MEDICI where these equations are discretized and solved numerically [41].

5.4 Simulation Result

5.4.1 Comparison with the same geometry and doping profile

Based on the modified drift-diffusion equations, the nonisothermal electrical and thermal characteristics of the Si IGBT or SiC IGBT can be obtained once the device structure, doping profiles and the applied bias are given. The comparison can be made between the performance of the SiC and Si IGBT during normal device operation. In this section the simulation was first conducted under the condition that the SiC IGBT and Si IGBT have the same geometry and doping profiles. The mesh grid and doping contour of the Si and SiC IGBT are shown in Fig 5.3 where the contour line was made by every $\log_{10}$ difference of the doping density.

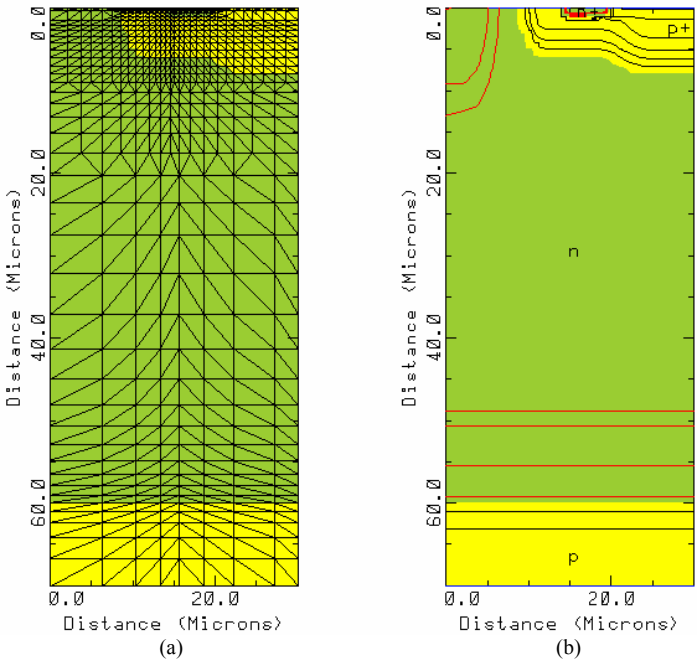


Fig.5. 3 (a) The device mesh grid and (b) The doping profile contours

The height and width of the simulated IGBT are 70μm and 30μm respectively. The doping density for n-drift region (uniform), n^+ source (Gaussian) and n+ buffer region (Gaussian) are $1\times10^{14}cm^{-3}$, $1\times10^{20}cm^{-3}$ and $1\times10^{16}cm^{-3}$ respectively. The doping density for p-base region (Gaussian), p^+ plug region (Gaussian) and p collector region (Gaussian) are $1\times10^{17}cm^{-3}$, $1\times10^{19}cm^{-3}$ and

$1\times10^{18}cm^{-3}$ respectively. The physical models and their parameters for SiC are the same as introduced in chapter 3.

The isothermal and nonisothermal I-V characteristics of a Si IGBT were simulated and plotted in Fig.5.4 where a 25V gate bias was applied. Different behavior was observed for these two results. At lower voltages (<4V), the two I-V curves are essentially the same indicating that the temperature effect can be ignored in this voltage range. However, the nonisothermal I-V curve deviated from the isothermal one at higher voltage (>4V) because of the device physical parameter degradation (carrier mobility) caused by the elevated lattice temperature within the device as shown in Fig.5.5. The self-heating effect within the device should be taken into consideration. Showing in Fig.5.4, the latch-up failure started to happen in the Si IGBT at the point 2 where the current density I_{ds} was 2.25×10^{-4} A/μm, the applied collector voltage was 8.64V and the temperature was increased to 554K.

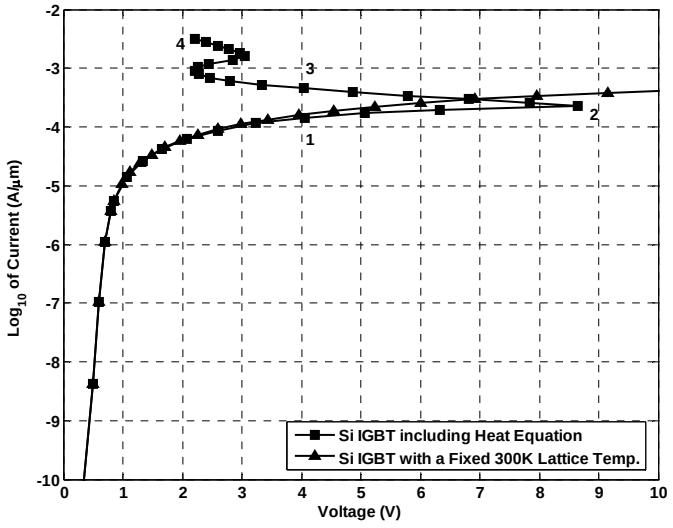
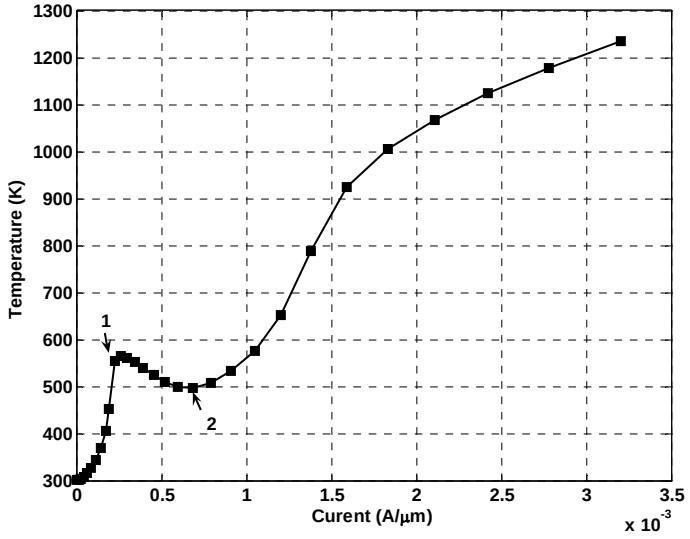
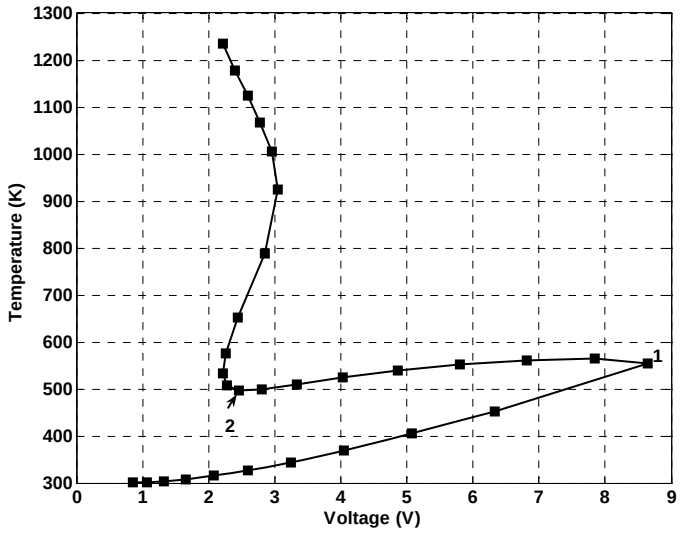


Fig.5. 4 The nonisothermal and isothermal I-V characteristics of the simulated Si IGBT

The maximum temperature within the device resulting from the self-heating effect is shown in Fig.5.5 regarding to the collector current and voltage respectively.



(a)



(b)

Fig.5. 5 The maximum temperature increase within Si IGBT vs. (a) current, (b) voltage

As shown in Fig.5.5, the temperature within the device was increased up to 554K at point1 before the latch-up failure happened in the Si IGBT where the parasitic *NPN* transistor was partially turned on. After this point, a period of

temperature decrease was observed from point 1 to point 2 where the current density was increased from 2.25×10^{-4} A/μm to 6.88×10^{-4} A/μm. This is the transition region where the main current path was shifted from the channel to the path going through the parasitic *NPNP* structure. After this period, the temperature within the device was increased to a very high value and the parasitic *NPNP* thyristor was fully turned on and the IGBT lost its MOS gate control. This latch-up failure can be verified by the current flowlines plotted in Fig.5.6. The current flowline figures are corresponding to the current at points 1,2,3,4 in Fig.5.4 respectively.

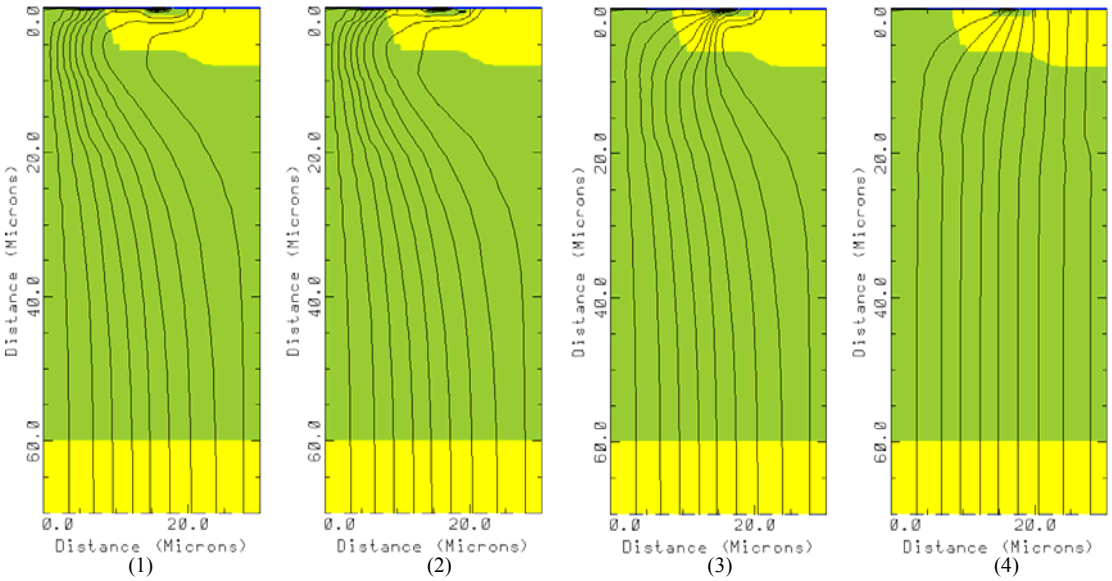


Fig.5. 6 The current flowlines within the Si IGBT before and after the latch-up failure

As shown in Fig 5.6, during the normal operation of the Si IGBT, the current flowed from p-collector region (Collector) to the n^+ emitter region (Emitter) by going through the path made by the n^+ buffer, n-drift region and the inversion channel during (1) and (2). A very small leakage current was observed through the parasitic *NPN* bipolar transistor at this stage. However at (3), the main current path was

shifted from the channel region to the path which is vertically through the parasitic *NPNP* structure. The current going through the inversion chancel decreased dramatically. At (4), the parasitic *NPNP* structure was fully turned on. There was no current flowing through the channel region and the Si IGBT was latched up and lost its gate control.

The same simulation was conducted for the SiC IGBT sequentially. The nonisothermal and isothermal simulation results are plotted in Fig.5.7.

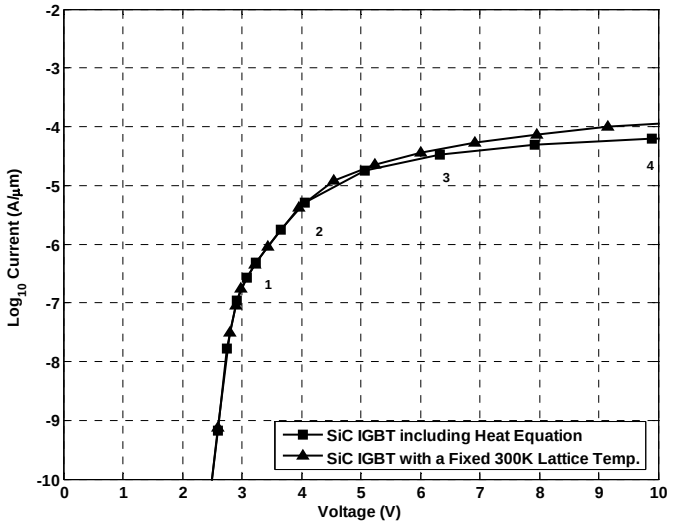


Fig.5. 7 The nonisothermal and isothermal I-V characteristics of the SiC IGBT

A small difference between the SiC nonisothermal and isothermal results is shown in Fig.5.7. The two curves are approximately the same up to 5V. Then the nonisothermal I-V curve started to increase slowly than the isothermal one because of the high temperature parameter degradation which is similar to the result of Si IGBT. However there is no latch-up failure was observed in SiC IGBT in both cases. The actual simulation results showed that no latch-up failure was observed even the

applied voltage was up to hundred voltages. This result indicates a very good capability of SiC IGBT against the latch-up failure compared to Si IGBT. The maximum lattice temperature growth within the SiC IGBT is also shown in Fig.5.8.

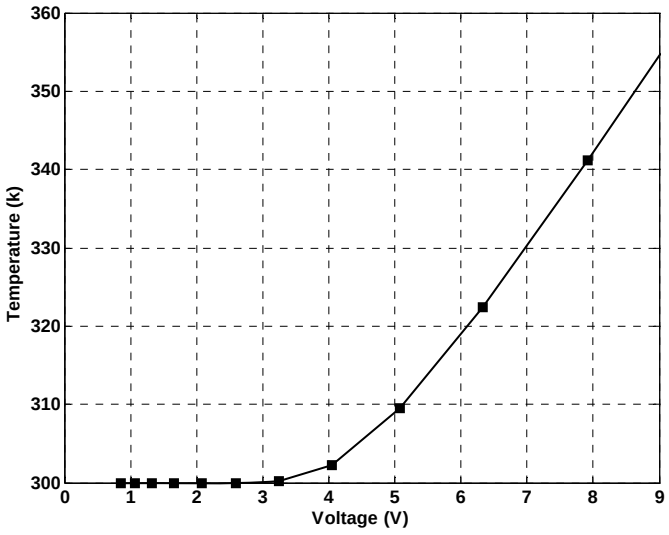


Fig.5. 8 The maximum temperature growth within the SiC IGBT vs. current

The lattice temperature increased monotonically with the increased anode voltage (current). No temperature snapback was observed for the SiC IGBT indicating the current conduction mechanism was consistent under all the applied bias. This conclusion was verified by the current flowlines plotted in Fig.5.9 where the four plots are corresponding to the points 1,2,3,4 shown in Fig.5.7 respectively. Under all the applied biases, the current was well confined within the path which is made by p^+ substrate, n drift, and inversion channel. No leakage current was observed going through the parasitic *NPNP* thyristor. This showed the normal operation of the SiC IGBT all the time. And no latch-up failure was observed.

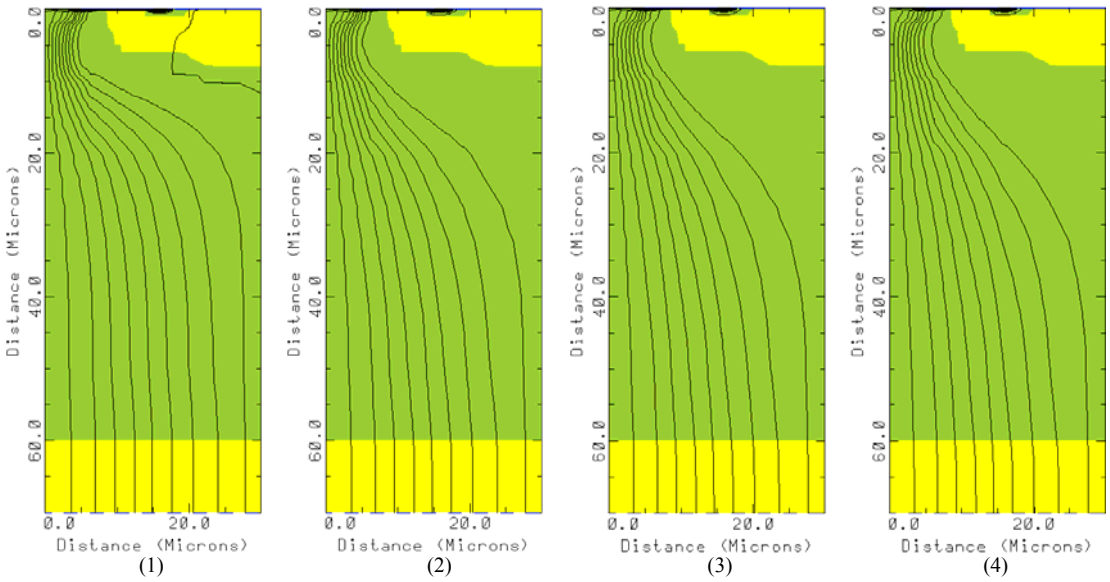


Fig.5. 9 The current flowlines within the SiC IGBT

Another comparison was made between the nonisothermal results of Si IGBT and SiC IGBT in Fig.5.10. When $V_{Collector}$ is driven up to 10V, SiC IGBT works normally with the lattice temperature only up to 341K. However the Si IGBT failed due to the latch-up at 8.6V. The simulation result even shows the SiC IGBT can work normally at a much higher voltage with a very high lattice temperature (for example, at $V_{collector}$=550V, T=1365K). This is because: (1) the theoretical breakdown voltage for such a 40μm thickness of SiC n-drift region is 4KV (2). Heat can flow more readily through SiC than Si due to its the higher thermal conductivity (SiC:3.0-3.8 W/cm·K, Si:1.5 W/cm·K). These features enable SiC IGBTs to operate at high power levels and still dissipate the large amounts of excess heat. This point can be further strenghted by the thermal flux comparison between SiC IGBT and Si IGBT as shown in Fig.5.11 where almost two order higher thermal flux was observed in SiC IGBT at current density 4×10^{-5} A/μm.

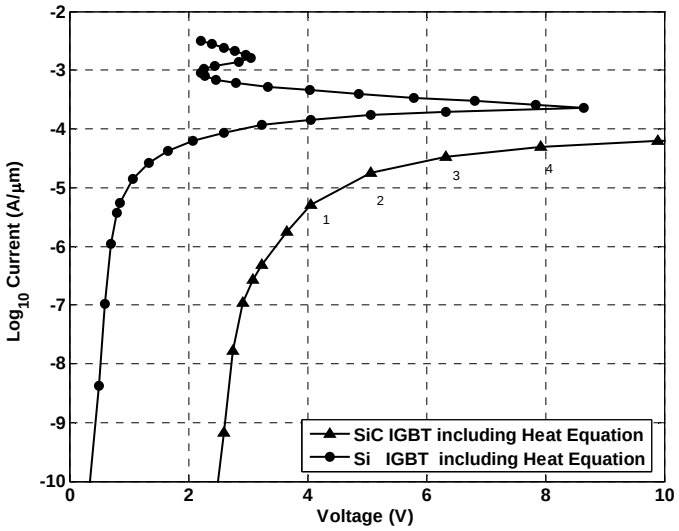


Fig.5. 10 The nonisothermal I-V characteristics comparison between Si IGBT and SiC IGBT

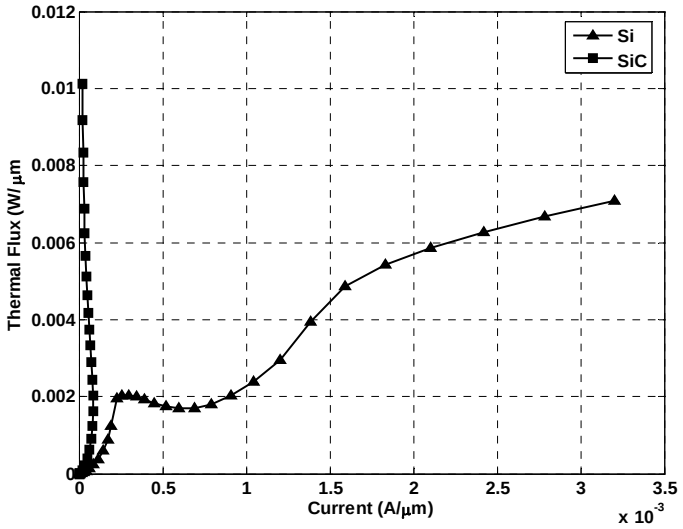


Fig.5. 11 The thermal flux compassion between Si IGBT and SiC IGBT

5.4.1.1 Device Internal Physics Investigation

The internal physical parameters inside the SiC and Si IGBT are needed to be further investigated to explain the different results when the self-heating effect was

included in device modeling as shown in Fig.5.10. Beside the internal physical parameters (potential, carrier density, and mobility), the voltage-drop along device p-base region and the characteristics of the parasitic bipolar transistor were all combined together to account for this difference. 3D potential plots for the Si IGBT and SiC IGBT are first shown in Fig.5.12 and Fig.5.13 respectively. These potential figures are corresponding to the potentials at points shown in Fig.5.4 respectively.

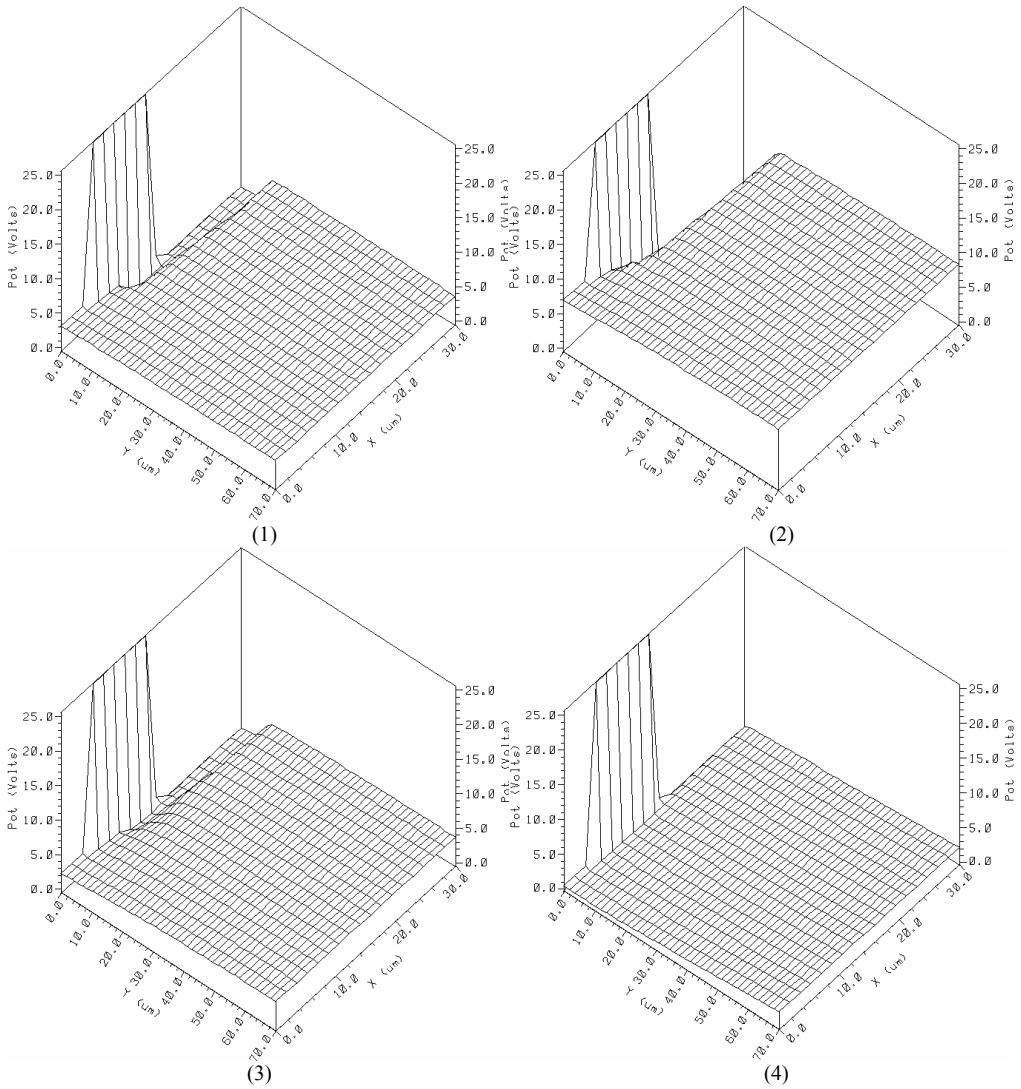


Fig.5. 12 3D Potential plot corresponding to four stages of the Latch-up happened in Si IGBT.

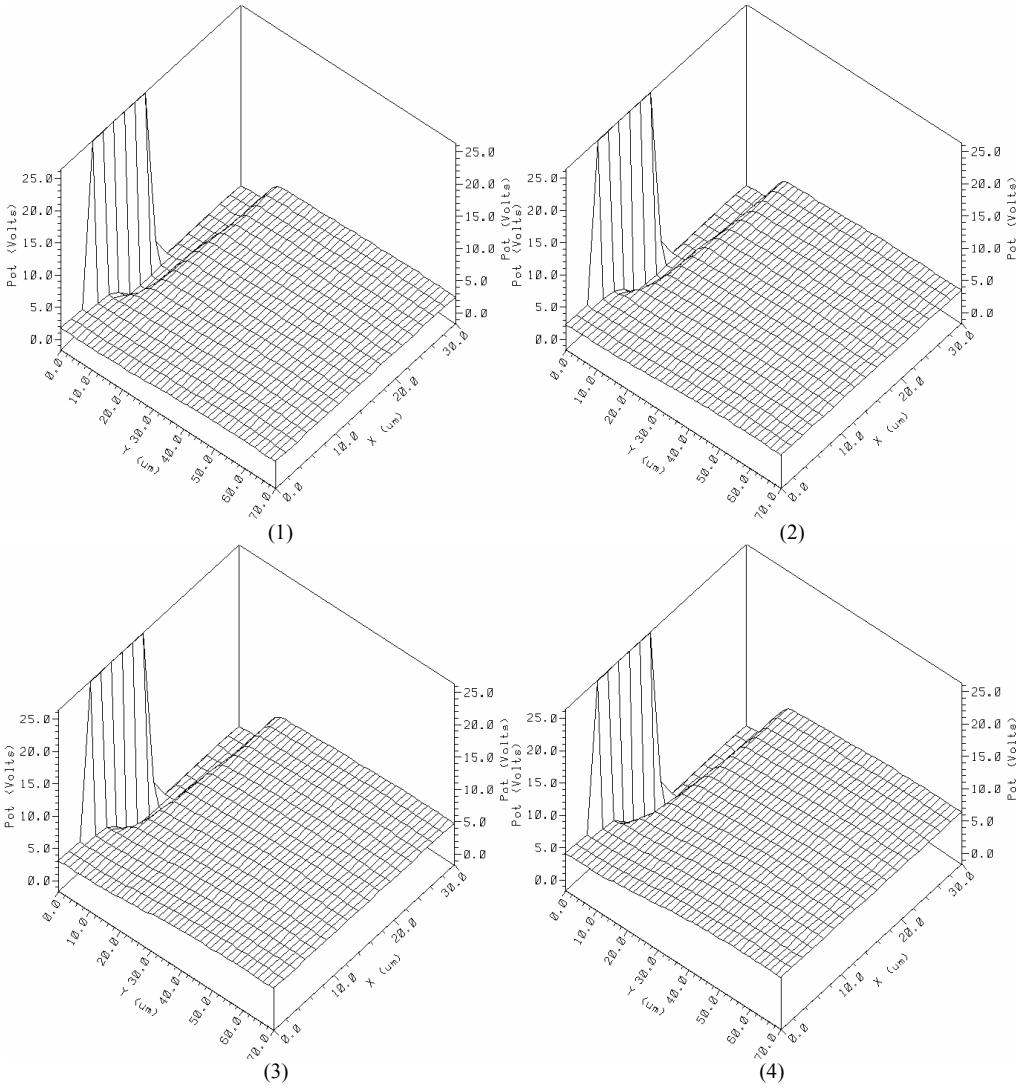
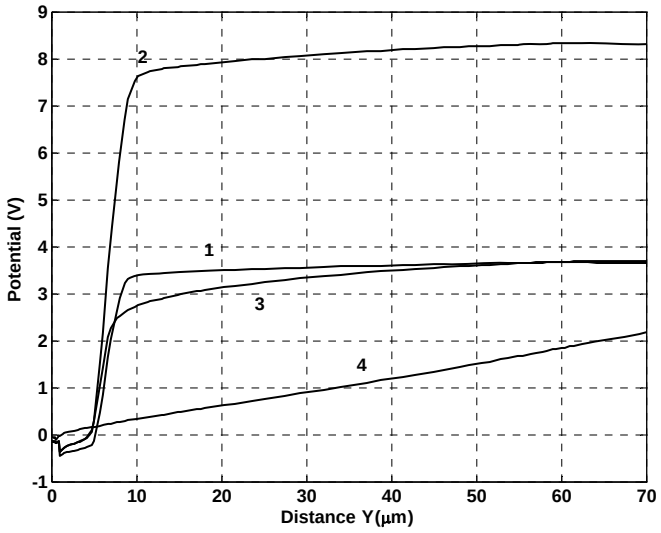


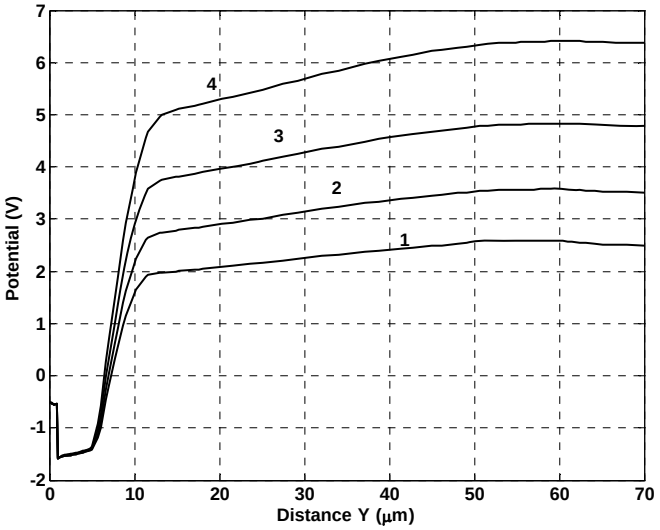
Fig.5. 13 3D potential plots for SiC IGBT.

In Fig.5.12, the potential barrier between the n^+ source and p-base region of the Si IGBT decreased gradually. This parasitic *PN* junction became more and more forward biased. At last this potential barrier was totally disappeared showing the happening of the latch-up failure. However, as shown in Fig.5.13, the change of this potential barrier within the SiC IGBT was very little expect that the potential was

increased with the applied bias at the collector side. This indicated the normal operation of the device. The potential barrier change within the Si and SiC IGBT can be further demonstrated in Fig.5.14 where the 1-D potentials are plotted along the vertical cross-line of the device at x=20m.



(a)



(b)

Fig.5. 14 (a) 1D potentials for Si IGBT at x=20um (b) 1-D potentials for SiC IGBT at x=20um

In Fig.5.14, it clearly shows the potential barrier variation between n^+ source and p-base region of the Si IGBT and SiC IGBT. This dramatic potential barrier change within Si IGBT explains how the latch-up failure happened in Si IGBT. In Fig.5.14 (a) the potential barrier of Si IGBT deceases gradually because of a voltage drop generated by the lateral leakage current through device p-base region. And this voltage drop will forward the *PN* junction between n^+ source and p-base region, turn on the upper *NPN* parasitic bipolar transistor, lead to the latch-up failure of the SiC IGBT, and redistribute the potential inside the device. Once the latch-up happened, the potential plot almost became a straight line. The device worked as a resistor under this condition. Meanwhile the potential barrier of the SiC IGBT changed very little and can be ignored as shown in Fig.5.14 (b), showing the normal operation of the device.

5.4.1.2 The voltage drop along p-base region

Since the lateral current leaking through the p-base region forwarded the parasitic N^+ source/p-base junction, played an important role during the latch-up failure of Si IGBT, it is necessary to check the magnitude of the voltage drop created by this current along the p-base region. The results will explain the difference performance of the Si and SiC IGBT with the self-heating effect taking into consideration. In this work, the p-base region of the IGBT was modeled by a rectangle box as shown in Fig.5.15. Then the voltage drops were calculated based on the information of doping concentration, mobility, and current density extracted from the simulation results.

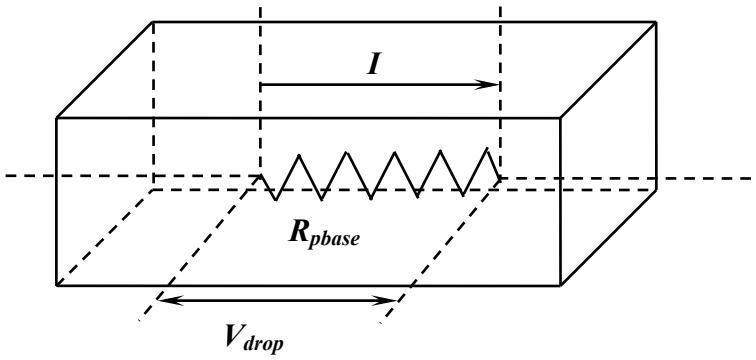
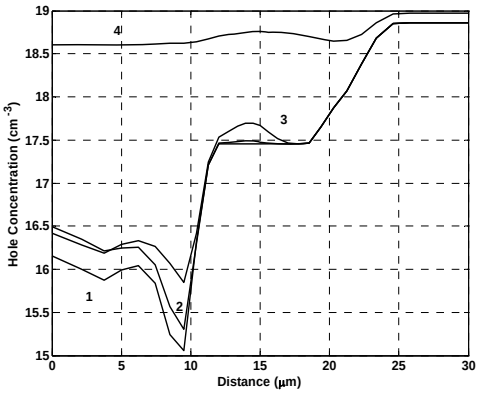
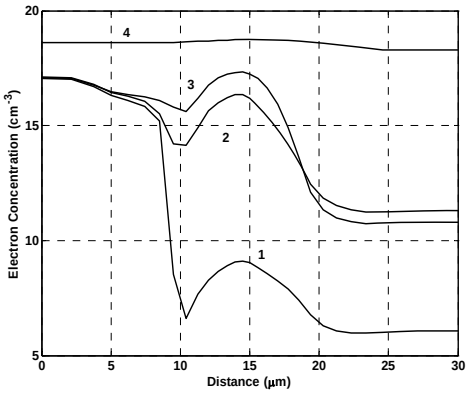


Fig.5. 15 The rectangular box approximation of p-base region within the IGBT

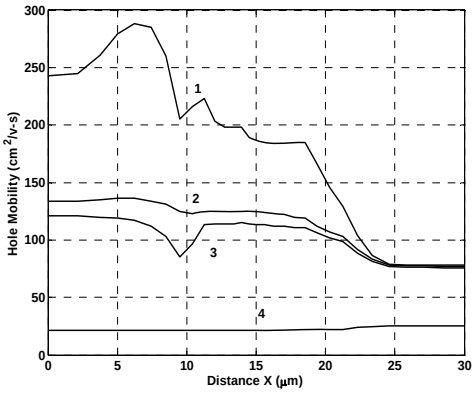
The current density, carrier concentration and mobility variations within the simulated Si IGBT before and after the latch-up are shown in Fig.5.15 respectively. The denoted number shown in the figure are corresponding to the points shown in Fig.5.4 where the values were taken along the horizontal crossline of the device at y=1.5μm.



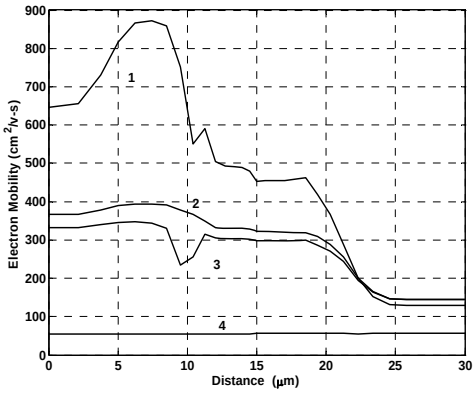
(a) Hole Concentration



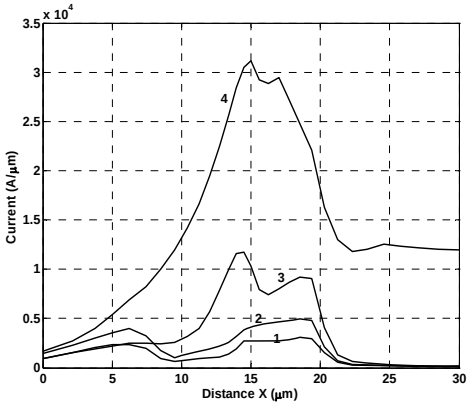
(b) Electron concentration



(c) Electron Mobility



(d) Hole Mobility



(e) Current density

Fig.5. 16 The current density, carrier concentration and mobility change within the simulated Si IGBT before and after the latch-up

The highly increased carrier density and much worse mobility degradation with the elevated lattice temperature within the device were observed in Fig.5.16 (c)-(d). The main current path shifting from the channel region to the parasitic *PNPN* structure can be verified in Fig.5.16 (e). The voltage drop along p-base region is given by:

$$V_{drop} = J \times \rho \times L_E \quad (5.22)$$

Where J is the current density, ρ is the resistivity of the p-base, and L_E is the effective length of the p-base.

We know that the resistivity ρ is given by:

$$\rho = \frac{1}{q(\mu_n n + \mu_p p)} \quad (5.22)$$

Where μ_n, μ_p are electron and hole mobility, and n, p are electron and hole concentration. Since this calculation is only for comparison purpose, the average values of these parameters along p-region are used. The effective length of the p-base L_E was 10μm extracted from the simulation results.

The calculated voltage drop values along p-base region of Si IGBT are shown in table 5.1. It shows that carrier concentration is increased greatly with the temperature increase inside the device. This leads to almost one order increase of hole concentration and dramatic change of electron concentration in p-base region. The increased hole concentration and decreased mobility will be offset and keep its contribution to resistivity in p-region almost same magnitude. The total voltage drop along the p-base region was gradually increased from 0.14V to 0.5V before the latch-up happened. The parasitic NPN transistor within Si IGBT will be activated and turned on once the voltage drop increased to this voltage range.

Table 5. 1 The voltage drops along p-base region in Si IGBT

	Hole Concentration (cm^{-3})	Hole Mobility (cm^2/V-S)	Electron Concentration (cm^{-3})	Electron Mobility (cm^2/V-S)	Current Density ($A/\mu m^2$)	Resistivity ($\Omega \cdot \mu m$)	Voltage Drop (V)
1	5.28×10^{17}	176	4.22×10^{8}	431	2.01×10^{-5}	6.72×10^{2}	0.14
2	5.35×10^{17}	109	6.68×10^{15}	287	3.26×10^{-5}	1.04×10^{3}	0.34
3	6.02×10^{17}	118	7.37×10^{16}	308	7.56×10^{-5}	6.66×10^{2}	0.50
4	5.26×10^{18}	22	4.73×10^{18}	56	2.40×10^{-4}	1.64×10^{2}	0.39

The same approach is used to calculate the voltage drop along the p-base of the simulated SiC IGBT. The calculated voltage drop values along p-base region in SiC IGBT are shown in table 5.2.

Table 5. 2 The voltage drops along p-base region in SiC IGBT

	Hole Concentration (cm^{-3})	Hole Mobility (cm^2/V-S)	Electron Concentration (cm^{-3})	Electron Mobility (cm^2/V-S)	Current Density ($A/\mu m^2$)	Resistivity ($\Omega \cdot \mu m$)	Voltage Drop (V)
1	5.27×10^{17}	93	1.01×10^{-34}	349	1.36×10^{-7}	1.27×10^{3}	0.003
2	5.27×10^{17}	87	2.53×10^{-33}	334	6.03×10^{-7}	1.36×10^{3}	0.02
3	5.27×10^{17}	79	5.16×10^{-31}	308	1.22×10^{-6}	1.50×10^{3}	0.04
4	5.27×10^{17}	69	5.98×10^{-28}	276	1.84×10^{-6}	1.72×10^{4}	0.06

The data in table 5.2 shows that the average hole concentration is the same for these four data points and the average electron concentration is so small that its contribution to resistance can be ignored. And the leakage currents in the p-base region are two orders smaller than that of Si IGBT. The voltage drops in p-base region of SiC IGBT shown in table 5.2 is too small to forward the p-base/n^+ source *PN* junction. The 1D current density plots of the SiC IGBT is shown in Fig.5.17.

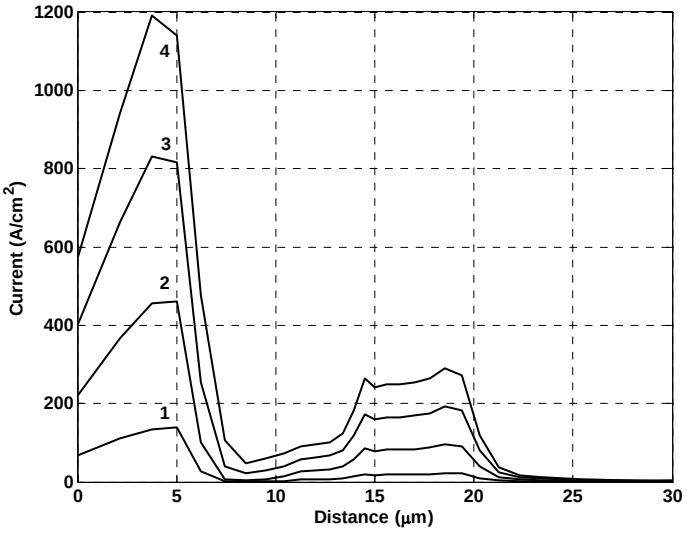
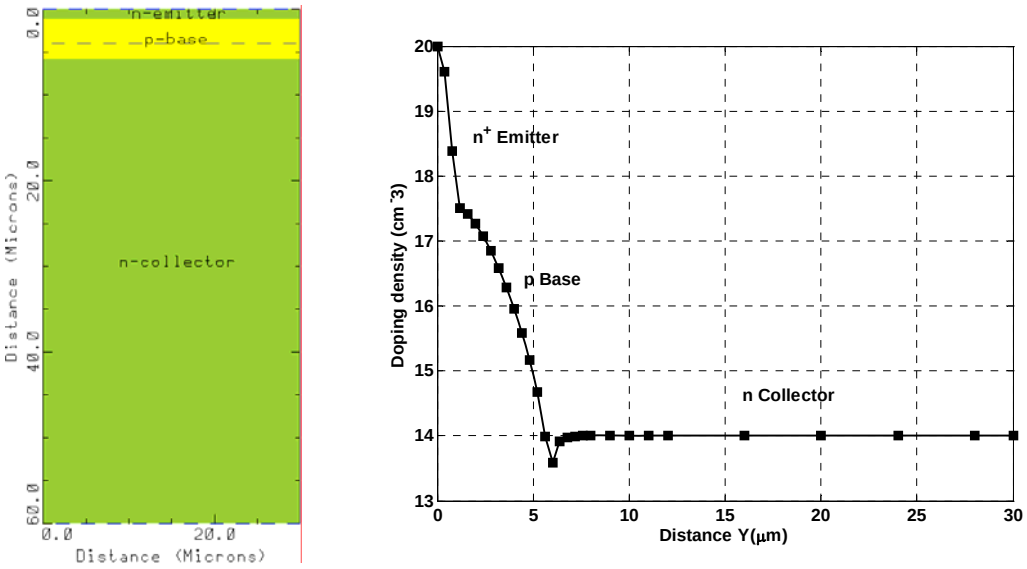


Fig.5. 17 The 1D current density plots at y=1.5 μm

In Fig.5.15 (e), that maximum current peaks is located at the p-base region from x=12 μm to x=22 μm, showing the turn-on of the parasitic bipolar transistors within the Si IGBT. However the current as shown Fig.5.17 mainly flows from the n-drift region to the channel region and the leakage current through p-base region is very small. The will support the conclusion that no main current shift happened in the SiC IGBT and the parasitic bipolar transistor within it keeps inactive all the time, And the SiC IGBT works normally during the simulation.

5.4.1.3 The parasitic bipolar transistor investigation

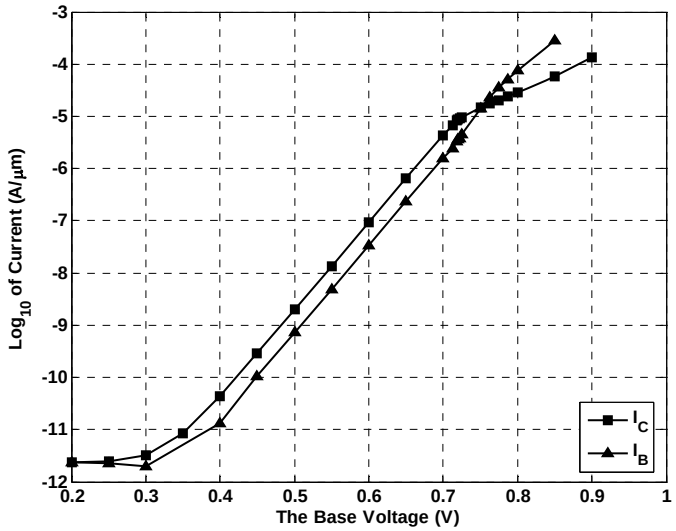
To further prove the robustness of SiC IGBT against the latch-up failure, the parasitic bipolar transistor was investigated in this work. It will be very helpful if we can compare the gains of the parasitic bipolar transistors within Si IGBT and SiC IGBT. And the gain variation of the parasitic bipolar transistors with the increased lattice temperature inside the SiC and Si IGBT will explain the different behavior of these two devices. As shown in Fig.5.18 (a), a *NPN* bipolar transistor is extracted from the parasitic n^+ source/ p-base/n-drift structure within the IGBT. The physical structure of n^+ source and p-base are extended as rectangular regions. The doping profiles of those regions are the same with those in the Si and SiC IGBT shown in Fig.5.18 (b).



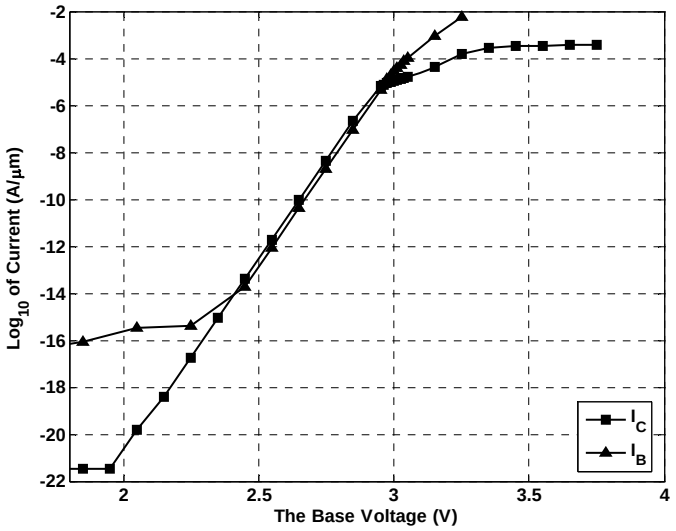
(a) (b)

Fig.5. 18 The extracted parasitic n^+ source/ p-base/n-drift transistor: (a) structure, (b) the doping profile

The I-V characteristics of the Si and SiC *NPN* transistors were obtained by simulation as show in Fig.5.19 (a) and (b).



(a)



(b)

Fig.5. 19 The I-V characteristics of the parasitic NPN transistors: (a) Si (b) SiC

As shown in Fig.5.19, the most distinct difference between the I-V characteristics of the SiC and Si NPN transistors is the difference of the turn-on voltage of the transistor. The Si *NPN* transistor became active at V_{Base}=0.4V while the SiC *NPN* transistor started to work at V_{Base}=2.45V. A six times difference on the turn-on voltage was observed.

In Fig 5.19 (a), an average current gain 2.75 (β) was obtained from the ratio of the collector current over the base current I_C/I_B where the V_{Base} of the Si *NPN* varied from 0.4V to 0.7V. However a ¼ lower average current gain 2.08 (β) was obtained for the SiC *NPN* transistor as V_{Base} varying from 2.45V to 2.95V as shown in Fig.5.19 (b). Using equations (5.2), (5,3) and (5,4), the values of transport factor α, the emitter efficiency γ_E, and the base transport factor α_T of the SiC and Si transistor are calculated as 0.73 and 0.68, 0.992 and 0.992, 0.74 and .068 respectively. For the Si

and SiC IGBTs, it also showed that $\alpha_{T\text{-}Si\text{-}PNP} > \alpha_{T\text{-}SiC\text{-}PNP}$ through the parasitic *PNP* transistor simulation. As introduced in the beginning, the latch-up failure happens If the sum of the transport factors of the *NPN, PNP* parasitic transistors becomes larger than 1 ($\alpha_{TNPN} + \alpha_{TPNP} \geq 1$). A conclusion that the Si IGBT is more vulnerable than SiC IGBT again the latch up failure can be made here since the sum of Si ($\alpha_{TNPN} + \alpha_{TPNP}$) is lager than the sum of SiC ($\alpha_{TNPN} + \alpha_{TPNP}$).

The I-V characteristics of the parasitic Si, SiC *NPN* transistors under different lattice temperatures were further simulated. The Si result is shown in Fig.5.20.

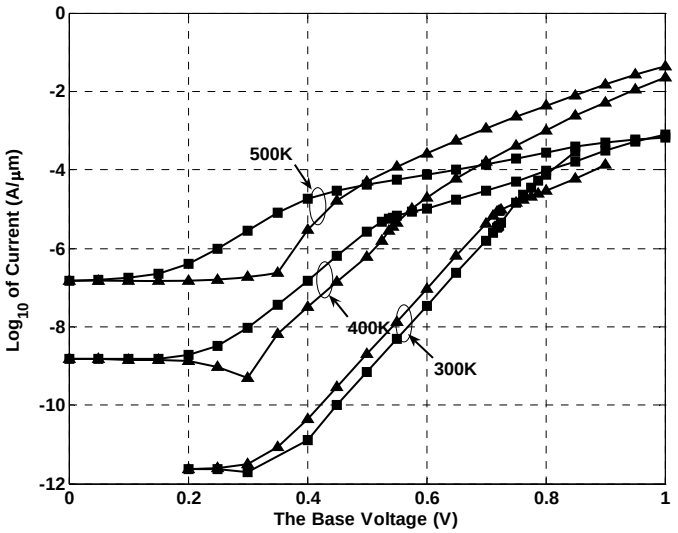


Fig.5. 20 The I-V characteristics of the Si NPN transistors under 300K, 400K and 500K

The maximum current gains (β) of the Si *NPN* transistor were 4.4, and 12.8 under 400k and 500k respectively. And the corresponding base voltage (V_B) was in the range of the voltage drops shown in table.5.1. The base transport factors (α_T) were calculated as 0.81 and 0.93 respectively. This will make the Si IGBT easily

meet the condition for the latch-up failure that the sum of the transport factors of the *NPN, PNP* parasitic transistors $(\alpha_{TNPN} + \alpha_{TPNP})$ is larger than 1.

The I-V results for SiC *NPN* transistors are shown in Fig.5.21.

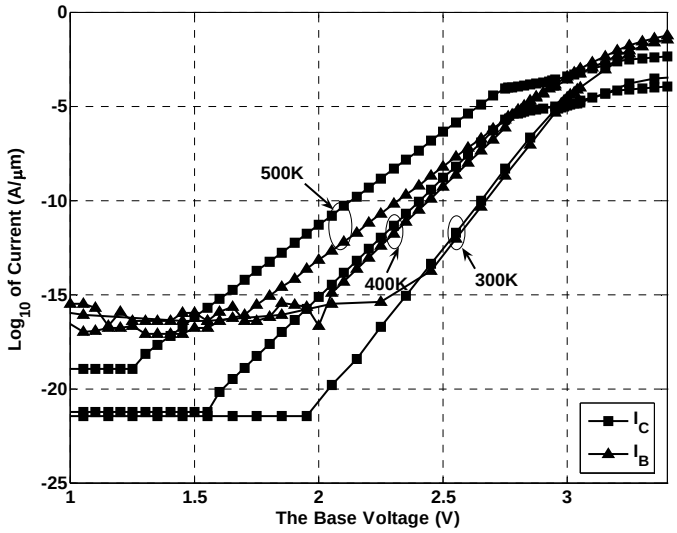


Fig.5. 21 The I-V characteristics of the SiC NPN transistor under 300K, 400K and 500K

The maximum current gains (β) of the SiC *NPN* transistor were 2.8 and 7.5 under 400k and 500k respectively. The corresponding base voltage (V_B) was in the range of 1.7~2.8V. However the calculated voltage drops shown in table.5.2 are far from this range. Then the parasitic *NPN* transistor within the SiC IGBT will not be activated at all. This explains why there is no latch-up failure in the SiC IGBT during simulation. Also it was observed that the current gain β of the SiC *NPN* transistor increased slower with temperature compared to Si *NPN* transistors. This result is consistent with the result that a lower positive temperature coefficient of current gain was obtained for SiC *NPN* bipolar transistor in [53].

5.4.2 Comparison with same voltage rating

One of the advantages of SiC is the much smaller device dimension for the same device rating requirement. Then in this study the comparison between SiC IGBT and Si IGBT was also conducted under the same voltage rating condition. To do this comparison, the new SiC IGBT scaling from Si IGBT was made first with the scaling factors K_{width} and K_{doping} derived from Chapter 4. The meshes of the simulated SiC IGBT and Si IGBT are compared in Fig 5.22. The doping density of the n drift region of SiC IGBT was increased to 6.3×10^{15} cm^{-3}. The height and weight of the device were scaled down to 3μm and 7μm respectively.

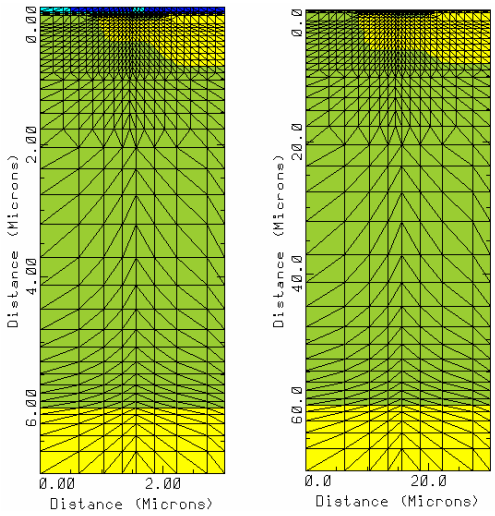


Fig.5. 22 The mesh grid of the simulated SiC and Si IGBT with a same voltage rating

The I-V characteristics of the SiC IGBT with and without heat equations are shown in Fig.5.23. The non-isothermal I-V characteristic comparison between the

same voltage rating Si IGBT and SiC IGBT is shown in Fig 5.24. Clearly there is no latch-up failures happened in the simulated SiC IGBT.

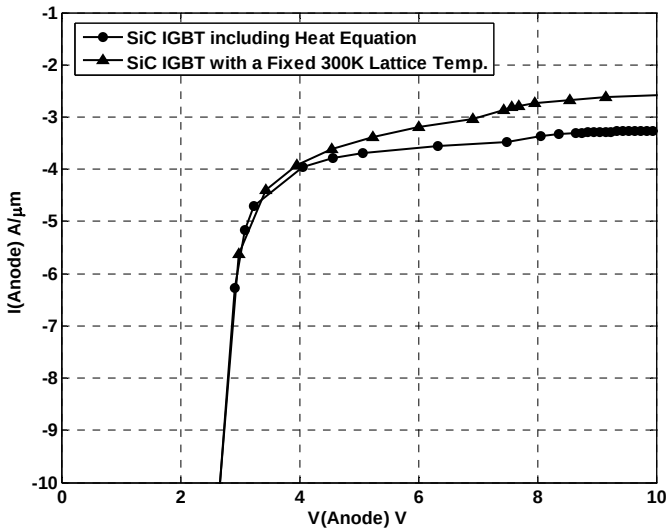


Fig.5. 23 The simulation results for SiC IGBT with same voltage rating

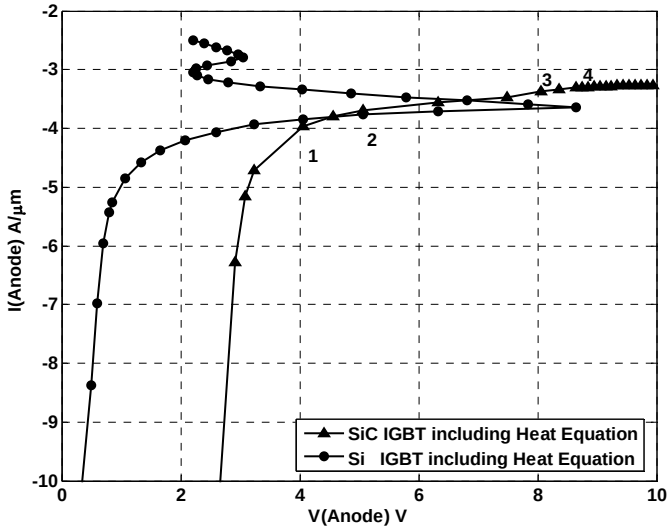
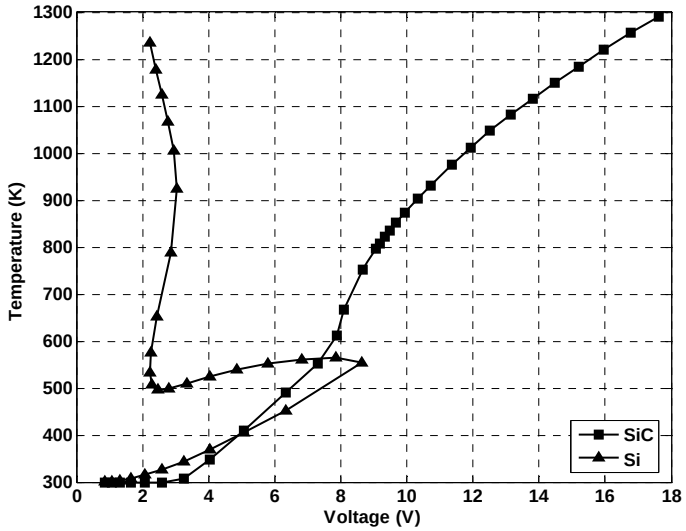


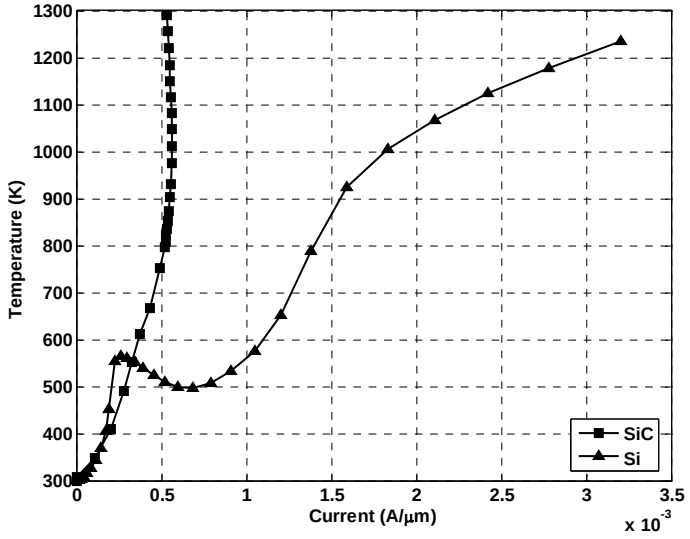
Fig.5. 24 The I-V characteristic comparison between Si IGBT and SiC IGBT

The maximum lattice temperature within the new SiC IGBT is shown in Fig.5.25 compared to that of Si IGBT. The result showed that the SiC IGBT works

normally under a very higher temperature up to 1300K with a stable current density in the range of 10^{-4} A/μm and very high applied voltage, indicating the better electro-thermal behavior of SiC IGBT.



(a)



(b)

Fig.5. 25 The maximum lattice temperature comparison between SiC IGBT and Si IGBT (a)vs.Voltage (b)vs. Current

The better high temperature performance of SiC IGBT can be explained by the higher thermal conductivity, thereafter the higher thermal flux as shown in Fig. 5.26.

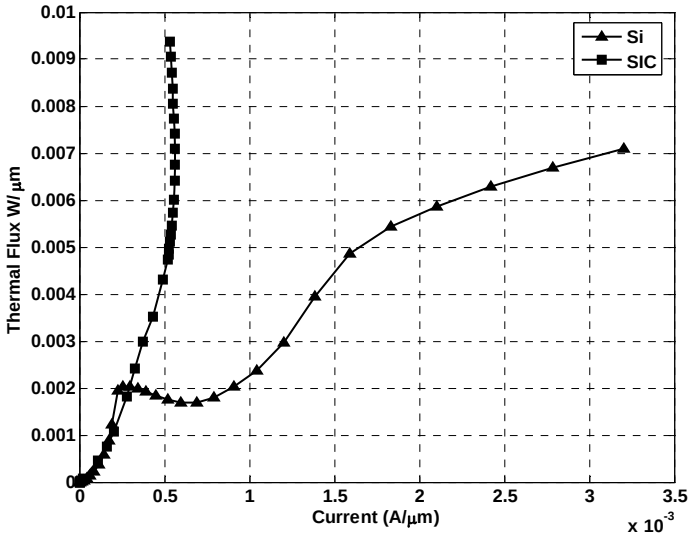


Fig.5. 26 The thermal flux comparison between SiC IGBT and Si IGBT

The current flowlines in Fig.5.24 shows that the SiC IGBT works properly with a limited parasitic bipolar transistor leakage current, indicating that no latch up failure happened in this new SiC IGBT too.

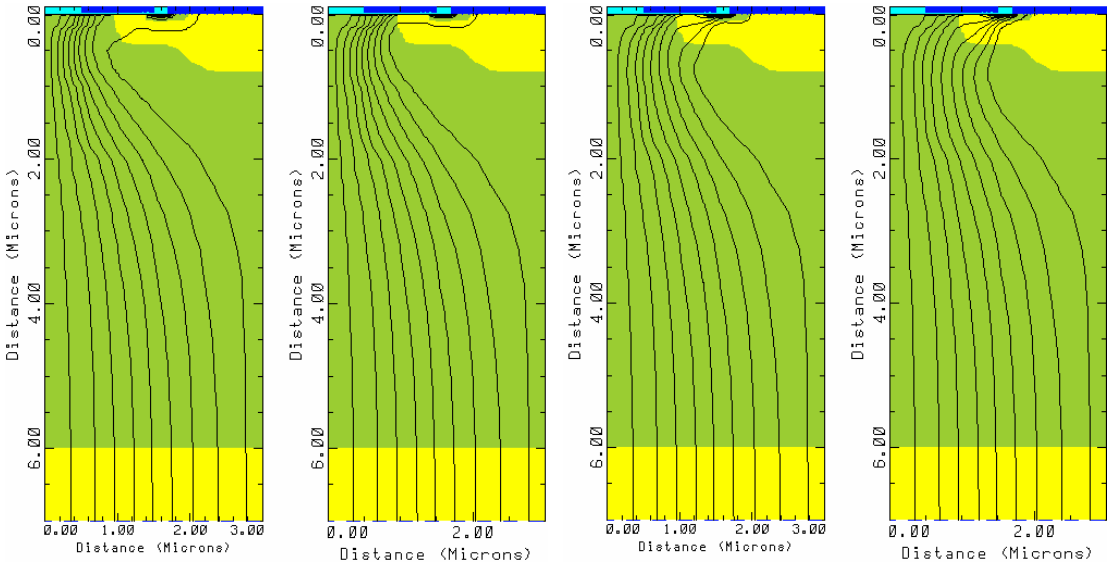


Fig.5. 27 The current flowlines of the SiC IGBT

5.4.2.1 Device Internal Physics Investigation

The internal physical parameters of this SiC IGBT were also checked in this section. The potential barrier change within the SiC IGBT is shown in Fig.5.27 where the 1-D potentials are plotted along the vertical cross-line of the device at x=0.8μm μm. The results show that the potential barrier between n^+ source and p-base *PN* junction was decreased gradually with the increasing applied voltage. The parasitic *NPN* transistor was partially turned on by the decreased potential barrier. This result is consistent with the current flowlines shown in Fig.5.26. However, this barrier was not disappeared as happened in Si IGBT above. And no latch-up failure was observed in this SiC IGBT. Then the internal device physic parameters were investigated to explain this robustness of SiC IGBT

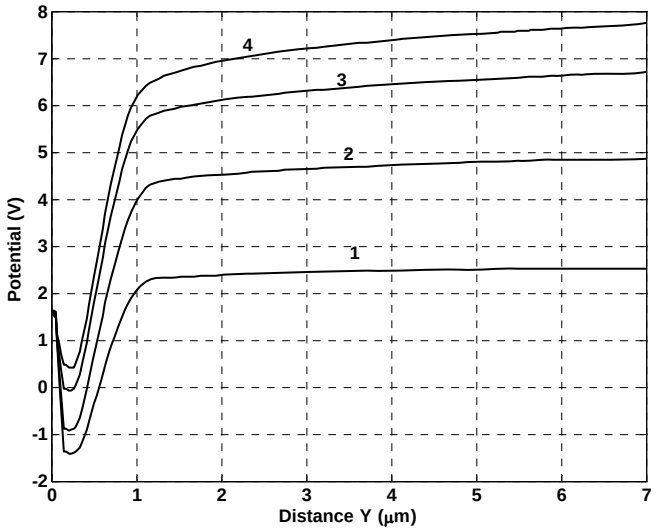
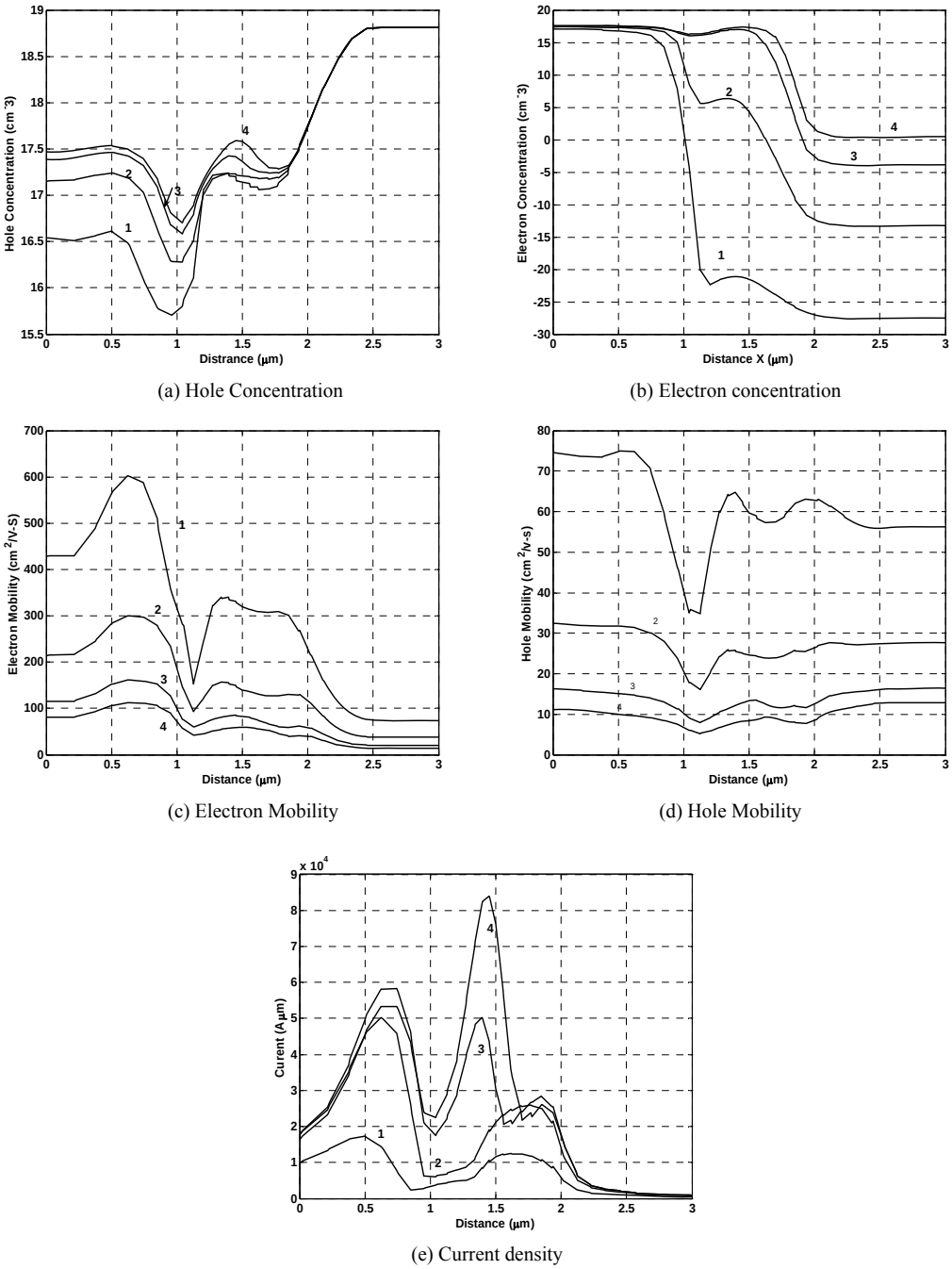


Fig.5. 28 The potential changes at x=0.8μm with the applied bias up to 8V.

The p-base voltage-drop was investigated. The current density, hole concentration and mobility are shown in Fig.5.28. The calculated voltage drops along p-base region in the SiC IGBT are shown in table 5.3.



(a) Hole Concentration

(b) Electron concentration

(c) Electron Mobility

(d) Hole Mobility

(e) Current density

Fig.5. 29 The current density, carrier concentration and mobility change within the simulated SiC IGBT

Table 5. 3 The voltage drops along p-base region in SiC IGBT with the same voltage rating

	Hole Concentration (cm^{-3})	Hole Mobility (cm^2/V-S)	Electron Concentration (cm^{-3})	Electron Mobility (cm^2/V-S)	Current Density ($A/\mu m^2$)	Resistivity ($\Omega \cdot \mu m$)	Voltage Drop (V)
1	4.69×10^{17}	60.1	1.70×10^{-22}	271	8.10×10^{-5}	2.21×10^{3}	0.004
2	4.78×10^{17}	25.1	4.17×10^{5}	125	1.64×10^{-4}	5.20×10^{3}	0.17
3	5.11×10^{17}	12.3	2.72×10^{16}	67	2.75×10^{-4}	9.93×10^{3}	0.55
4	5.55×10^{17}	8.4	7.11×10^{16}	47	4.02×10^{-4}	1.34×10^{4}	1.07

A maximum 1.07V voltage-drop was along the p-base region as shown in table 5.3. However the built-in potential for SiC IGBT was calculated as 3.13V if we assume that the doping densities are uniform in the n^+ source region and the p-base region with a density of 5×10^{17} cm^{-3} and 1×10^{20} cm^{-3} respectively. Thus this limited voltage-drop can only lower the potential barrier as shown in Fig.5.28. Then the partially the parasitic upper *NPN* transistor was turned on as the current flowlines shown in Fig.5.27 and 1D current plots shown in Fig.5.29. However the parasitic NPN transistor did not work in its active region with this limited voltage drop as shown in the following simulation.

5.4.2.2 The parasitic bipolar transistor investigation

The parasitic *NPN* bipolar transistor within the new SiC IGBT was also simulated with the same approach used in last section. The I-V characteristics of the transistor under 300K, 400k, and 500K are shown in Fig.5.30. Average current gains 22, 47, and 72 were obtained under these temperatures where the corresponding V_{Base} varied in the range of 1.8V to 3V. This high current gain of the transistor is the result

of the different doping profile. A three times lower positive temperature coefficient of current gain is obtained for the SiC transistor compared to that of Si transistor. With a 1.07V voltage-drop in p-base region, the parasitic SiC NPN did not work in its active region as shown in Fig.5.30. Only a limited leakage current went through the device parasitic structure. A conclusion that the latch-up failure can not be triggered in the SiC IGBT can be drawn here.

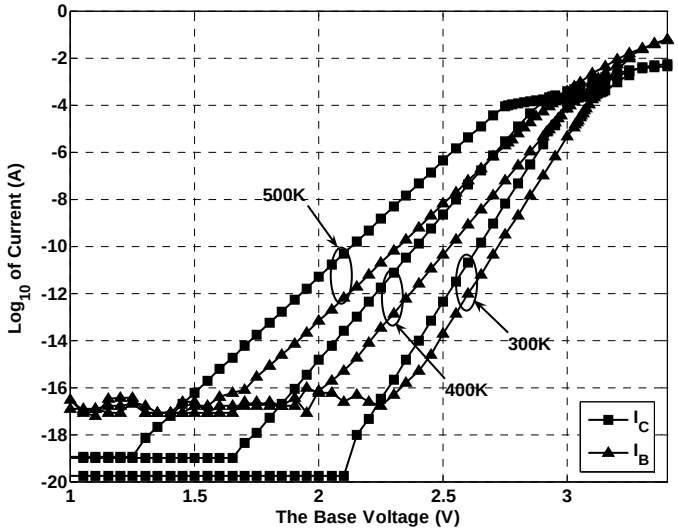


Fig.5. 30 The I-V characteristics of the new SiC NPN transistor under 300K, 400K and 500K

Chapter 6: Summary and Future Work

6.1 Summary

In this work, extensive studies have been conducted to investigate the failure mechanism for SiC power devices.

A complete set of SiC physical models and parameters for SiC has been set up. Some scaling factors for SiC power devices scaling down from Si power devices have been proposed. The drift-diffusion model has been introduced in details in chapter 2 which forms the basis for the simulations implemented in this work.

In Chapter 3, the I-V characteristics of 4H-SiC Schottky diodes have been measured and simulated. Some important parameters of Schottky diodes including barrier height ϕ_B, on-resistance R_{on} and mobility μ have been extracted from the simulation results. Later on the simulation results showed that the interface states existing between metal and semiconductor are the failure mechanism responsible for the non-catastrophic failures happened in the 4H-SiC Schottky diodes. The basic Schottky equation has been modified to account for the degradation effect caused by the interface states.

Single-event burnout (SEB) and Single-event gate rupture (SEGR) are the two very important failure mechanisms for electronic devices. They were investigated in Chapter 4 for SiC power MOSFET. The advantages of SiC power MOSFETs over Si

power MOSFETs against those failure mechanisms have been demonstrated by the simulation results.

Again in Chapter 5 the robustness of SiC IGBTs again the latch-up failure has been investigated compared to Si IGBTs. The high build-in potential in the parasitic *PN* junction, high turn-on voltage of the parasitic bipolar transistor and the lower positive temperature coefficient of the parasitic bipolar transistor current gain made the SiC IGBT a latch-up free device.

Contributions of this work are summarized as follows:

1. Categorized the general failure mechanisms for SiC Schottky diodes, power MOSFETs, and IGBTs.
2. Proposed and verified a complete set of SiC physical models and parameters for SiC device simulation.
3. Extracted the barrier height ϕ_B, mobility μ, on-resistance R_{on}, and interface state degradation resistance R_{it} parameters for SiC Schottky diodes used for DC characteristic SPICE simulation.
4. Identified interface states as the failure mechanism responsible for the non-catastrophic failure happened in Schottky diodes. The conclusion is supported and simulation and experimental results.
5. Derived the scaling factors k_{width} and k_{doping} to scaling the SiC devices down from the Si devices.
6. Developed a simulation approach to simulate the SEB failure threshold current, voltage for SiC power MOSFETs.

7. Identified that the better robustness of SiC power MOSFETs against SEB failures comes from: (1) Three times larger built-in potential between the n^+-source/p-base region (2) Two times larger SEB threshold current density (3) Three times larger SEB threshold voltage (4) Six times higher turn-on voltage of the parasitic bipolar transistor (5) Lower current gain of the parasitic bipolar transistor.
8. Found out that the SEGR failure behavior of SiC power MOSFETs and Si power MOSFET is comparable.
9. Investigated the basic I-V characteristics and internal physics of SiC IGBTs with self-heating effect. Compared to Si IGBTs, no latch-up failures were observed because: (1) The higher built-in potential of SiC PN junction, (2) The higher turn-on voltage of the parasitic NPN transistor, (3) lower temperature coefficient of the parasitic bipolar transistor current gain.

6.2 Future Work

6.2.1 Experimental verifications

In this study a detailed simulation investigation of several failure mechanisms of SiC power devices has been conducted. The results showed the better performance of SiC power devices against the SEB, SEGR and latch-up failures. However these

results need to be experimentally verified. Special device characterizations in this aspect need to be conduced to support our conclusions.

6.2.2 Circuit Simulation

The advantages of SiC power devices can be further demonstrated by some circuit simulation, for example, an unclamped inductance circuit. Without parameter approximations, the designed SiC devices can be inserted into a SPICE-based circuit to simulate the performance of it. An unclamped inductive test circuit is shown in Fig.6.1. The transient characteristics of SiC power MOSFET designed above can be simulated.

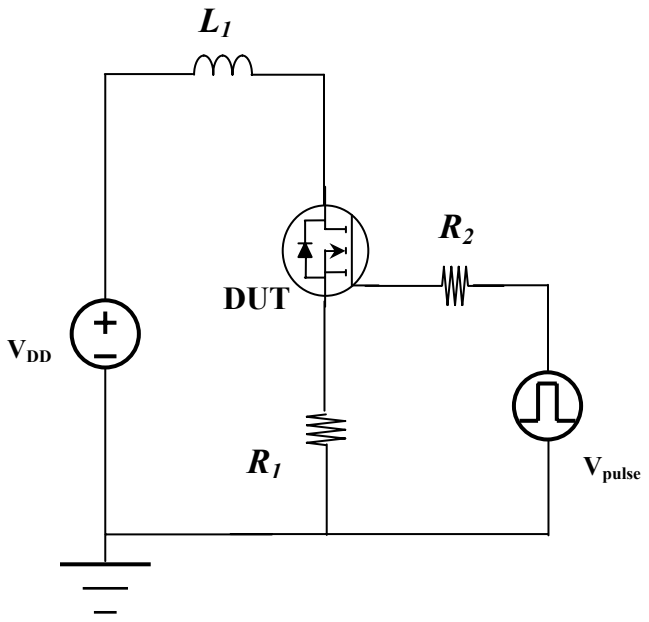


Fig.6. 1 An unclamped inductive test circuit

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