#### ABSTRACT

Title of Dissertation:	ATOMICALLY PRECISE FABRICATION AND CHARACTERIZATION OF DONOR- BASED QUANTUM DEVICES IN SILICON
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Atomically precise donor-based quantum devices in silicon are a promising candidate for scalable solid-state quantum computing and analog quantum simulation. This thesis demonstrates success in fabricating state-of-the-art silicon-phosphorus (Si:P) quantum devices with atomic precision. We present critical advances towards fabricating highfidelity qubit circuitry for scalable quantum information processing that demands unprecedented precision and reproducibility to control and characterize precisely placed donors, electrodes, and the quantum interactions between them.

We present an optimized atomically precise fabrication scheme with improved process control strategies to encapsulate scanning tunneling microscope (STM)patterned devices and technological advancements in device registration and electrical contact formation that drastically increase the yield of atomic-precision fabrication.

We present an atomic-scale characterization of monolayer step edges on Si (100) surfaces using spatially resolved scanning tunneling spectroscopy and quantitatively determine the impact of step edge density of states on the local electrostatic environment. Utilizing local band bending corrections, we report a significant band gap narrowing behavior along rebonded SB step edges on a degenerately boron-doped Si substrate.

We quantify and control atomic-scale dopant movement and electrical activation in silicon phosphorus (Si:P) monolayers using room-temperature grown locking layers (LL), sputter profiling simulation, and magnetotransport measurements. We explore the impact of LL growth conditions on dopant confinement and show that the dopant segregation length can be suppressed below one Si lattice constant while maintaining good epitaxy. We demonstrate weak-localization measurement as a high-resolution, high-throughput, and non-destructive method in determining the conducting layer thickness in the sub-nanometer thickness regime.

Finally, we present atomic-scale control of tunnel coupling using STMpatterned Si:P single electron transistors (SET). We demonstrate the exponential scaling of tunnel coupling down to the atomic limit by utilizing the Si (100) 2×1 surface reconstruction lattice as a natural ruler with atomic-accuracy and varying the number of lattices counts in the tunnel gaps. We analyze resonant tunneling spectroscopy through atomically precise tunnel gaps as we scale the SET islands down to the fewdonor quantum dot regime. Finally, by combining single/few-donor quantum dots with atomically defined single electron transistors as charge sensors, we demonstrate single electron charge sensing in few-donor quantum dots and characterize the tunnel coupling between few-donor quantum dots and precision-aligned single electron charge sensors.

#### ATOMICALLY PRECISE FABRICATION AND CHARACTERIZATION OF DONOR-BASED QUANTUM DEVICES IN SILICON

by

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Dissertation submitted to the Faculty of the Graduate School of the University of Maryland, College Park, in partial fulfillment of the requirements for the degree of Doctor of Philosophy 2019

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## Table of Abbreviations

2DEG	Two-dimensional electron gas
AC	Aberration-corrected / Alternative current
AES	Auger electron spectroscopy
APT	Atom probe tomography
ARPES	Angle-resolved photoemission spectroscopy
A.U.	Arbitrary unit
CI	Constant interaction
CVD	Chemical vapor deposition
DB	Dangling bond
DC	Direct current
DFT	Density functional theory
DI	Deionized
DOS	Density of states
EDS	Energy-dispersive X-ray spectroscopy
EELS	Electron energy loss spectroscopy
EMT	Effective mass theory
EUV	Extreme-ultraviolet
ESD	Electron stimulated desorption
FET	Field effect transistor
FIB	Focused ion beam
FCC	Face centered cubic
FWHM	Full width half maximum

HAADF	High angle annular dark field
HLN	Hikami-Larkin-Nagaoka
LDOS	Local density of states
LEED	Low-energy electron diffraction
LL	Locking layer
MBE	Molecular beam epitaxy
ML	Monolayer
NIST	National Institute of Standards and Technology
PES	Photo emission spectroscopy
PFKFM	Peak-force Kelvin force microscopy
Si:P	Silicon-phosphorus
PLAPT	Pulsed laser atom probe tomography
PPE	Two-photon photoemission spectroscopy
QD	Quantum dot
QEC	Quantum error correction
QI	Quantum information
QPC	Quantum point contact
RF	Radio frequency
RIE	Reactive ion etching
RMS	Root mean square
RTA	Rapid thermal anneal
SA	Single layer type A
SB	Single layer type B

- SEM Scanning electron microscopy
- SET Single electron transistor
- SIMS Secondary ion mass spectrometry
- SMU Source measure unit
- STM Scanning tunneling microscope
- STS Scanning tunneling spectroscopy
- SUSI Si sublimation source
- TDS Thermal desorption spectroscopy
- TEM Transmission electron microscopy
- UHV Ultrahigh vacuum
- UNSW University of New South Wales
- VBM Valence band maximum
- VDP van der Pauw
- WKB Wenzel-Kramers-Brillouin
- WL Weak localization
- XPS X-ray photoelectron spectroscopy

## **Chapter 1: Introduction**

The emergence of the semiconductor industry in the second half of the twentieth century has transformed people's lives and remains a driving force for the world's technological revolution. The modern semiconductor industry, having products that range from smartphones to supercomputers, is built on silicon because of the superb electrical, thermal, mechanical, and chemical properties of this material. The electrical transport properties of silicon can be easily controlled using doping processes, leading to the invention of transistor devices where electrical current can be controlled using electrical voltage signals. A transistor is the fundamental building block and carrier of information in a classical computer where binary digital bits are represented by voltage and current signals with the bits sequentially being acted upon by logic gates to perform classical computation. Downscaling of transistors has been driven by a constant demand for faster calculation, lower power consumption, increased system complexity, smaller size, and lower fabrication cost.<sup>1, 2</sup> Moore's Law predicts that the number of transistors on a single wafer doubles roughly every two years.<sup>3</sup> As microelectronics fabrication continues scaling down to the 5 nm node by 2020, the channel length of a transistor will be comparable to the size of single dopant atoms (an isolated phosphorus donor in silicon has a Bohr radius of  $\sim 2.5$  nm). At these scales, the discrete nature of single dopants becomes significant, and variability of dopant position at the atomic scale results in irreproducible characteristics in classical transistors. In the meanwhile, state-of-the-art semiconductor fabrication techniques that combine thermal diffusion or ion implantation with extreme-ultraviolet (EUV) lithography or electron-beam lithography are incapable of controlling single dopants with atomic precision. The failing of classical transport laws due to quantum effects and the intrinsic limitations of conventional semiconductor fabrication techniques are major hurdles to further scaling of modern integrated circuits. The success of Moore's law ended in 2016.<sup>4</sup>



Figure 1.1 Bloch sphere representation of a single qubit state. The eigenstates of the qubit, the  $|0\rangle$ , and  $|1\rangle$  are located at opposite poles on the sphere along the z-axis. The other points on the sphere represent superposition states  $|\psi\rangle$  that are parameterized by angles  $\theta$  and  $\varphi$ .

The ever-growing demand for computational power in modern society can be uniquely satisfied by computational methods beyond classical computation. The combination of quantum mechanics and computer science has provided a new paradigm for computing: quantum computing. In quantum computing, the unit of information is a qubit whose states represent a complex-valued superposition of 0 and 1 states, which gives rise to the potential computational power of a quantum computer. The state of a single qubit can be described by  $|\psi\rangle = a_0|0\rangle + a_1|1\rangle$ , where  $a_0$  and  $a_1$  are complex coefficients

that describe both the magnitude and phase of the  $|0\rangle$  or  $|1\rangle$  states. The normalization condition requires that the probability of finding the qubit in these two states,  $a_0^2$  and  $a_1^2$ , satisfies  $a_0^2 + a_1^2 = 1$ . An arbitrary state of a single qubit can be conveniently mapped to a point on a unit sphere, called the Bloch sphere, where the south and north poles represent the  $|0\rangle$  or  $|1\rangle$  eigenstates respectively. Single qubit gate operations move the qubit state around the Bloch sphere surface. Quantum mechanical coupling, called entanglement, can exist between multiple qubits, at a variety of spatial separations, such that manipulation or the state of one qubit influences the state of the others. Entanglement has no classical analog and is one of the key powers of quantum computing: the number of coefficients required to describe the state of a quantum system increases exponentially with the number of entangled qubits.

Quantum computers can solve some problems that classical computers are unable to address and perform certain tasks exponentially faster than classical computers. The history of the quantum computer dates to 1982 when Richard Feynman first suggested the use of quantum mechanical phenomena to simulate quantum systems.<sup>5</sup> The discovery of Shor's quantum algorithm to break RSA encryption codes in 1994<sup>6</sup> and the world's first demonstration of a quantum logic gate using trapped ions at NIST in 1995<sup>7</sup> became the primary drivers of early enthusiasm in quantum computing research. Quantum computing is generally classified into two approaches. The first approach is known as analog quantum computing and includes quantum simulators,<sup>8</sup> adiabatic quantum computing,<sup>9</sup> and quantum annealing,<sup>10</sup> where computations are performed by directly applying analog control of a Hamiltonian to evolve the quantum states. The second approach is gate-based digital quantum computing,<sup>11</sup> where the computation is broken down into a sequence of quantum gate operations, and compatible with error correction. The last two decades have witnessed tremendous progress in the implementation of quantum computers and quantum algorithms, as well as the thriving growth of quantum sensing<sup>12</sup> and metrology,<sup>13</sup> quantum communication<sup>14</sup> and conceptualization of a quantum internet.<sup>15</sup> Today, it is believed that quantum computers will transcend the boundaries of classical computers and significantly advance people's capability to overcome challenges in optimization problems,<sup>16</sup> quantum chemistry,<sup>17</sup> artificial intelligence,<sup>18</sup> quantum cryptography<sup>19</sup> and other unknowns in the future. Technology companies, such as IBM, Intel, Microsoft, and Google, are investing heavily in the race to build quantum computers,<sup>20</sup> with IBM launching cloud-based quantum computers in 2016 and Google announcing a 72-qubit general-purpose quantum computer chip in 2018.

The quantum algorithms that govern universal quantum computing operations are universal and independent of the physical implementation of the quantum computer. A gate-based universal quantum computer requires the realization of five criteria first proposed by DiVincenzo: <sup>11</sup>

- 1. Well defined two-level systems that can be employed as qubits in a scalable manner.
- 2. The ability to initialize the states of the qubits.
- 3. Long enough coherence time for the gate and error-correction operations.
- 4. The ability to read out the states of the qubits.
- 5. The ability to conduct a set of universal gate operations.

Implementing a functional quantum computer is challenging because it requires entirely new quantum hardware architectures, quantum algorithms, software stacks, and control protocols.<sup>21</sup> The most significant challenges reside in the critical needs for high fidelity gate operations and scalability of the qubit system. Qubits are intrinsically subject to state degradation due to noise, an effect termed decoherence. The coherence time must be much longer than the gate operation time of a qubit, which requires the qubit systems to be sufficiently isolated from the environment to prevent interactions that cause decoherence. Also, device fabrication imperfections and gating signal distortions are sources of errors for quantum gate operations. Running full-scale quantum algorithms and exploiting quantum computations' potential to outperform classical computation requires many qubits and gate operations.<sup>22</sup> In addition, emulating an error-free quantum computation demands quantum error correction (QEC)<sup>23</sup> that further increases the required number of qubits and gate operations. There will be many physical qubits required for each logical qubit.

A wide variety of qubit platforms are currently being pursued worldwide,<sup>24</sup> including the superconducting quantum computer,<sup>25</sup> trapped-ion quantum computer,<sup>26</sup> semiconductor quantum computer,<sup>27</sup> photonic quantum computer,<sup>28</sup> and topological quantum computer.<sup>29</sup> Among the different quantum computing systems, the semiconductor qubit platform based on silicon holds great promise of scalability thanks to the massive silicon-based semiconductor industry and vast existing knowledge of silicon properties that has been established over the last half-century.

Single spins in an external magnetic field form an inherently two-level system that is one of the natural choices for qubits in silicon (other choices for qubits include charge qubits and singlet-triplet qubits in silicon<sup>30</sup>). Silicon is an excellent host material for spin qubits because of its weak spin-orbit coupling and the abundance of isotopic <sup>28</sup>Si (~95% in natural Si) with zero nuclear spins (therefore, no hyperfine interactions) that allows long coherence time for high-fidelity quantum gate operations.<sup>31</sup> Further improvement of coherence time can be made through isotopic purification of <sup>28</sup>Si where a single donor's electron spin and nuclear spin coherence times have been demonstrated to exceed 1 second and ~30 minutes, respectively, in bulk<sup>32, 33</sup> and 0.5 second and 30 seconds in gated nanostructures.<sup>34</sup>



Figure 1.2 Schematic of an elementary building block of Kane's quantum computer. The quantum information is encoded in the nuclear spins of individual phosphorus donors that are separated by 20 nm and embedded in a Si host. The A-gates control the resonance frequency of individual nuclear spin qubits to be selectively addressed by an external AC magnetic field. The J-gates control the electron-mediated interactions between adjacent qubits. This figure is taken from Kane.<sup>35</sup>

In 1998, Bruce Kane<sup>35</sup> proposed the use of nuclear spins of individual isotope <sup>31</sup>P atoms in silicon to construct a scalable quantum computer. A schematic of Kane's quantum computer architecture is illustrated in Figure 1.2. The Kane architecture consists of an array of equally spaced (~20 nm) single phosphorus donors that are aligned with a series of control (labeled A and J) gates. The qubit operation is realized by combining the gates with an alternating magnetic field. The A gates above the donors control the hyperfine interaction at the donors that can bring the nuclear spin into and out of resonance with the alternating magnetic field, which allows individual addressing of the quantum states of each qubit. The J gates between neighboring donors carry out two-qubit gate operations by turning on and off the coupling between adjacent nuclear spins through the electron-mediated Heisenberg exchange coupling. Spin state readout is proposed by using an ultrasensitive electrometer, such as a single electron transistor (SET),<sup>36</sup> to detect the spin-dependent tunneling from the target qubit to a charge neutral donor.<sup>35</sup> Since Kane's seminal work, several other donor-based quantum computer architectures have been proposed utilizing different types of dopants<sup>37, 38, 39, 40, 41</sup> as well as electron spin qubits and charge-based qubits in silicon.<sup>42, 43</sup>

Over the last decade, significant progress has been made towards implementing a donor-based Si quantum computer. This includes the demonstration of successful initialization, readout,<sup>36, 44, 45</sup> and manipulation<sup>31</sup> of both the nuclear and electron spins of single donor qubits. However, due to the intrinsic valley degeneracy in the silicon conduction band, the strength of exchange coupling depends strongly on donor separation, even on the scale of single Si lattice constants.<sup>46</sup> Accurate gate operation relies on accurate dopant placement with atomic-scale precision. Scaling up Kane's quantum computer requires deterministic placement of a vast array of single donors into Si lattice sites with atomic-scale precision within a defect-free single crystalline silicon host environment.

STM-based atom-by-atom fabrication represents the state-of-the-art in fabrication precision in silicon.<sup>47</sup> In 1994, Lyding, Shen, Tucker and coworkers first demonstrated the hydrogen-lithography technique on Si (100) surfaces using STM to generate device patterns with atomic precision.<sup>48, 49</sup> Selective adsorption of gaseous precursors that are compatible with hydrogen lithography on Si (100) surfaces were subsequently investigated.<sup>50, 51, 52, 53, 54</sup> About ten years ago, a group effort led by Michelle Simmons at the University of New South Wales first experimentally demonstrated a complete STM-based fabrication scheme for atomically precise fabrication in silicon, which combines atomic-precise hydrogen lithography and selective phosphine dosing with low-temperature epitaxial silicon overgrowth.<sup>55 56, 57</sup> Though conceptually straightforward, to fabricate a quantum device with atomic perfection one must overcome many technological challenges, such as extremely high vacuum levels, atomic-precision STM lithography, defect-free low-temperature epitaxial overgrowth, precise contact alignment, and high-yield electrical contacts to atomic devices. Currently, only a few research groups in the world are capable of fabricating STM-patterned Si:P devices.

The successful demonstration of deterministic placement of single donors in silicon <sup>58, 59</sup> and atomically abrupt low-resistance dopant wires that can function as inplane gate electrodes for qubit operations <sup>60</sup> has opened the door to building donorbased qubit circuitry in silicon with atomic precision. Since then, tremendous progress has been made by Simmons and her coworkers in demonstrating the essential building blocks of donor-based silicon quantum computation in an atomically precise manner, such as observation of exchange coupling between precision placed donors in silicon, <sup>61, 62</sup> high-fidelity electron spin read-out of precision placed single donors,<sup>44, 63, 64</sup> and single-shot single-gate radio-frequency (RF) spin readout in silicon.<sup>65</sup> Hill and coworkers have proposed a surface code architecture in silicon that enables a three-dimensional all-epitaxial fabrication pathway towards large-scale donor-based quantum computation.<sup>66, 67</sup> Usman and coworkers demonstrated the first spatial metrology of single dopants in silicon with exact lattice site precision.<sup>68</sup> In spite of these recent advances, however, scaling up these basic building blocks into a vast array of functional single donor qubits remains an unsolved challenge. Fabricating high-fidelity qubit circuitry for scaled quantum information processing demands unprecedented precision and reproducibility to control and characterize the precision-placed donors, electrodes, and the quantum interactions among them.

In this thesis, we first present a complete atomically-precise fabrication scheme with improved strategies for fabrication quality. We then demonstrate atomic-scale characterization of mono-atomic layer step edges on Si (100) surfaces, which is critical to *in-situ* metrology at the atomic scale for silicon-based quantum computing. By adopting a locking layer technique during the device encapsulation overgrowth and combining dopant concentration profiling with weak localization measurements, we develop a fabrication and metrology strategy to control and characterize, at the atomic-scale, dopant movement and electrical activation in Si:P monolayers. Using these improved fabrication strategies to define and maintain atomically abrupt dopant

confinement in silicon, we demonstrate atomic-scale control of tunnel coupling and illustrate the exponential scaling of tunnel resistance at the atomic limit. Finally, we characterize resonant tunneling spectroscopy through precision placed few-donor and single-donor quantum dots with the goal of fully realizing atomic-scale design and engineering of the tunnel coupling in up-scaled donor qubit systems and analog quantum simulators.

Following the brief introduction in this chapter, we structure this thesis as follows:

**Chapter 2** summarizes the background and theoretical concepts necessary to understand the thesis research presented in the following chapters. We first introduce the working principles of a scanning tunneling microscope (STM), which is the central experimental tool for atomic-scale characterization and fabrication in this thesis. We review the tunneling theory in STM that is essential for interpreting and understanding the experimental results under different STM operation modes, such as imaging, spectroscopy, and atomic-scale manipulation. We briefly discuss the material and electronic properties of single crystalline silicon as well as the Si (100) surface that will act as the host material and provide the central surface platform for the atomically precise donor-based fabrication in this thesis. In particular, we review the chemical interactions of hydrogen and phosphine (PH<sub>3</sub>) on the silicon surface as well as the molecular dynamics governing the silicon homoepitaxy overgrowth, which lays the foundation for the advancement in process development that enables control of individual dopants in silicon with atomic-precision. Furthermore, we introduce the concept of single electron tunneling and the constant interaction model of Coulomb blockade in single electron transistors (SET), which will be used as a central tool to demonstrate for the first time atomic-scale control of tunnel coupling using atomicallyprecise fabrication techniques. The subsequent four chapters present the main experiments and results in this thesis.

**Chapter 3** describes the primary experimental fabrication methods in this thesis. We present a complete atomically precise fabrication scheme with an emphasis on advances in atomic-precise fabrication techniques that have been developed in the Silver group during this thesis work. Following an overview of the device fabrication processes, we present technical discussions regarding our experimental implementation and materials characterization for high-quality atomically-precise fabrication in silicon, which includes chemical and thermal sample cleaning, hydrogen-termination in UHV, hydrogen-lithography using STM, phosphorus dosing and incorporation, and lowtemperature epitaxial overgrowth. We present a detailed investigation of the impact of hydrogen lithography conditions on the epitaxial and electrical quality of STMpatterned devices, highlighting the importance of a near-perfect UHV environment as well as the contamination-free Si surfaces and STM tips to achieve success in atomically precise fabrication. We illustrate two novel methods to form high-yield, low-resistance ohmic electrical contact to the STM-patterned devices by utilizing palladium silicide formation and ion-implantation. Then we explain how the electrical and magneto-transport properties of the fabricated  $\delta$ -doped devices and STM-patterned devices are measured at low temperatures.

**Chapter 4** presents a detailed spatially resolved Scanning Tunneling Spectroscopy (STS) study across monolayer step edges on Si (100) surfaces and quantitative determination of the local density of state distributions and band gap information at the step edges. The influence on the local electrostatic environment of the interactions between the step edge states and the STM tip is quantified under real scanning tunneling measurement conditions. We uniquely utilize the dangling bond states as a fingerprint to quantify the local band bending landscape, which therefore allows us to make critical corrections to the experimentally observed surface state energy levels. The elucidation of the local electronic environment near the monolayer step edges in this chapter contributes to future investigations on the electronic behavior of single donors near atomic step edges at surfaces or interfaces using STM, and also provides strong support in understanding defect dimensionality and its influence on the local conductivity properties of semiconducting surfaces.

In **Chapter 5**, we develop an atomically precise fabrication and metrology strategy to control and characterize single dopant atom movement and electrical activation in Si:P monolayers. Using a room-temperature grown locking layer (LL) technique, we successfully suppress the dopant segregation length to below a single Si lattice constant while maintaining epitaxy. Fine tuning the LL growth parameters provides a key tool for direct control of dopant movement at the atomic scale. Dopant segregation, diffusion, and growth front roughening effects have been taken into account at the atomic scale to quantify the impact of parametric control of the Si:P monolayer

synthesis on dopant confinement, the local crystalline environment, and dopant electrical activation, which will provide unique insight into the dopant and atomic lattice arrangements at Si:P 2-D interfaces and their effect on few-atom electronics. We demonstrate that a high LL growth rate in combination with a low-temperature LL rapid thermal anneal can create exceptionally sharp dopant confinement while maintaining good electrical quality within Si:P monolayers. We perform weak localization-based thickness measurements on the Si:P monolayers in the sub-nanometer regime. We show good agreement between the measured electrical thickness and the quantified dopant distribution profiles that not only demonstrates the weak localization analysis as an effective quantum metrology technique for quantifying the electrical thickness with atomic precision but also validated the capability of the LL technique in providing superb 2-D electrical confinement quality in the fabricated Si:P monolayers. The parameter space that we have explored in this study is fully compatible with state-ofthe-art hydrogen lithography techniques using scanning tunneling microscopy and can be applied directly to the fabrication of atomically precise Si:P quantum computing devices and atomically engineered superlattice materials.

In **Chapter 6**, we demonstrate the first systematic atomic-scale control of tunnel coupling in Si:P devices after overcoming critical challenges in achieving ultra-clean and atomically-abrupt hydrogen lithography, the prevention of unintentional dopant movement during encapsulation overgrowth, and high-yield, low-resistance ohmic contact formation. Using the Si (100)  $2 \times 1$  surface reconstruction lattice as a natural atomically-precise ruler, we systematically vary the tunnel junction gap distances with

sub-nm precision in a series of STM-patterned single electron transistors (SETs). Using low-temperature transport measurements, we extract the single electron tunneling resistance from the zero-bias Coulomb oscillation peaks and demonstrate, in a reproducible manner, the expected exponential scaling of tunneling resistance at the atomic limit. We demonstrate that, by varying the number of surface lattice constants within the fabricated tunnel junction gaps, the SET operation can be transitioned from the linear conductance regime to the strong tunnel coupling regime to the weak tunnel coupling regime. We show a difference of four in the resistance values of a pair of nominally identical tunnel gaps, corresponding to a difference in the effective tunnel gap distances of half a dimer row pitch: the intrinsic limit of hydrogen lithography precision on Si (100) 2×1 surfaces. We present a detailed resonance tunneling spectroscopy analysis through STM-patterned few donor quantum dots and illustrate the impact of the source and drain reservoir's density of states modulation on the single electron tunnel coupling as we scale the electrode width down to the atomic scale. Finally, by combining single/few-donor quantum dots with atomically defined single electron transistors as charge sensors, we demonstrate single electron charge sensing in few-donor quantum dots and characterize the tunnel coupling between few-donor quantum dots and precision-aligned single electron charge sensors. Our results demonstrate a key step towards atomic-scale design and engineering of tunnel coupling for high-fidelity quantum manipulations in large scale donor-based quantum computers as well as towards the atomically precise construction of Hubbard model hopping and exchange Hamiltonians in donor-based analog quantum simulators.

**Chapter 7** concludes this thesis and illustrates the experiments that are currently underway in our group to demonstrate high-fidelity spin readout and manipulation in atomically precise donor qubits.

## **Chapter 2: Theory and Background**

### **2.1 Introduction**

In this chapter, we present fundamental theories and background literature that are necessary to understand the results presented in thesis. We first introduce the basic principles of scanning tunneling microscopy (STM), which is the enabling method for precise atomic fabrication. We then review the detailed formulation of perturbation theory of tunneling that is essential for understanding the tunneling events in STM (Chapter 4) as well as in atomic-scale quantum devices (Chapter 6). Next, we introduce the fundamentals of Si (100) surfaces, dosing, and epitaxial overgrowth that are necessary to understand the overall atomically precise fabrication strategies discussed in Chapter 3 and Chapter 5. We then illustrate the fundamental operating principles behind single electron transistors (SET) to help understand the experimental results in Chapter 6. Based on the orthodox theory of single electron tunneling, we present a detailed theoretical derivation to quantify the single electron tunneling resistance in a metallic SET from transport measurements at low-temperatures. To facilitate analyzing the measured single electron tunneling spectroscopy in a single atom transistor in Chapter 6, we review the theoretical background and simulation methods for analyzing the resonant tunneling features of quantum dots.

#### 2.2 Scanning Tunneling Microscopy

Since the invention of the Scanning Tunneling Microscope (STM) by Binnig and Rohrer in 1982,<sup>69</sup> STM has become an invaluable tool for surface science and nanotechnology because of its unrivaled capability to image a solid-state surface in a non-invasive way with true atomic resolution. The ultimate atomic-scale resolution of STM is a direct result of the lateral extent of the atomic-scale wavefunction at the tip apex and the exponentially sensitive tunneling current in the vertical direction. Additionally, the rich physics of the tip-surface interaction has enabled the STM to manipulate solid state matter atom by atom. This capability was demonstrated most impressively by Eigler's groundbreaking work to arrange individual Xe atoms on a Ni surface to form the famous "IBM" logo.<sup>70</sup> Crommie and coworkers then constructed a quantum corral on a Cu surface using individual Fe atoms, demonstrating the ability to control the electronic quantum behavior in an atomically precise manner.<sup>71</sup> (Figure 2.1)

It is appropriate to mention here the historical role played by two NIST (formally known as the National Bureau of Standards, NBS) scientists, Russell D. Young and E. Clayton Teague in the invention of STM. Young invented the topografiner that used a piezoelectric driver to scan a surface with a probe in a field emission mode.<sup>72</sup> Teague conducted vacuum electron tunneling experiments at the bias and tunnel gap distances similar to those standard for STM operation.<sup>73</sup> Later, Binnig and Rohrer combined these two technological achievements and created the STM.



Figure 2.1 Atomic scale manipulation. (a) A NIST logo that is fabricated by using a low temperature STM at 4 K to move individual cobalt atoms on a copper surface. The ripples in the background are the images of the electron density on the surface. The image is taken from Celotta *et al.*<sup>74</sup> (b) An STM-fabricated quantum corral nanostructure that is composed of 48 Fe atoms on a Cu (111) surface. The corral acts as a circular quantum well where the quantum confinement results in standing wave states of surface electrons within the corral. The image is taken from Crommie *et al.*<sup>71</sup>

Figure 2.2 shows a schematic of the basic construction of an STM. Three sets of piezoceramic actuators in the x, y, and z directions allow atomic-precision positioning of the tip in 3-dimensions. In a typical constant-current imaging mode, the tunneling current through the tip is amplified and compared with the set-point current. As the probe is scanned across the surface, the difference between the measured tunneling current and the set-point value is used as a feedback signal through a real-time feedback control circuit to regulate the tip height and maintain a constant tunneling current. A high signal-to-noise ratio is achieved by having the first stage of signal amplification *in-situ* close to the STM stage. Mechanical vibrations from the environment are isolated from the STM through a variety of isolation and damping mechanisms often including eddy current damping. The tip positioning as recorded during the scan generates a surface contour map which is a convolution of the wavefunction at the tip apex and the atomic scale features on the scanned surface area. In the next section, we illustrate how to interpret STM images and extract the physical phenomena of interest.



Figure 2.2 Schematic diagram of a scanning tunneling microscope (STM) for surface atomic-scale imaging and manipulation. This simplified schematic illustrates the principles of STM operation where a biased metallic tip is brought into close proximity of a conducting surface resulting in tunneling current. While a piezoelectric tube scanner raster-scans the tip in the x-y directions, a tunneling current is kept constant by a feedback control loop which regulates the z-height of the tip. The recorded topographical z-map reflects the surface morphology and the surface local density of

states (LDOS). A surface defect with high LDOS will appear as a bright spot in the STM image. Changes in the bias and tunneling current settings can change the STM operation from an imaging mode to an atomic manipulation mode.

During STM operation, a conducting STM tip's apex is brought within a few Ångstroms of an electrically conducting sample surface, forming a tunnel junction between the tip and the sample. The vacuum region between the tip apex and the sample surface serves as the tunnel barrier with the barrier height on the order of the surface work function. The wavefunction overlap within the tunnel barrier enables a finite transmission probability of electrons between the tip and sample states. At a zero tipsample bias condition, a contact potential is formed across the junction through tunneling due to the surface work function difference between the tip and the sample. Depending on the bias polarity applied across the tunnel junction, tunneling events are dominated by electrons tunneling from the tip into the empty states above the sample's Fermi level, or those tunneling from the occupied states below the sample's Fermi level into the tip. At a given bias *V*, the tunneling current  $I_t$  generally depends exponentially on the gap separation  $z_t$ ,

$$\frac{l_t(z_t)}{l_t(z_t - \Delta z_t)} \approx e^{-2\kappa\Delta z_t}$$

#### Equation 2.1

Here  $\kappa = \sqrt{2m_e(\phi - eV)}/\hbar$  is the decay constant that can be derived using the WKB approximation and assuming a rectangular barrier,  $m_e$  is the effective electron mass from the sample surface,  $\phi$  is the average work function of sample and tip, and  $\hbar$  is

the reduced Planck's constant. Atomic resolution imaging can be achieved when there is a single atom protrusion or atomically localized density of states at the tip apex at the Fermi level.

### 2.3 Tunneling Theory - STM and Beyond

The basic theoretical description of the tunneling process in an STM is typically derived from Bardeen's early work on *macroscopic* tunnel junctions.<sup>75, 76, 77</sup> Following the discussion of Gottlieb *et al.*,<sup>75</sup> in this section, we review the theoretical foundation of Bardeen's approach and the Tersoff-Hamann interpretation of tunneling in STM applications. In a later section in this chapter, we will review the single electron tunneling in SETs where charging effects on a small island dominate the transport through an *ultra-small* tunnel junction.<sup>78</sup>

The discussion in this section follows the traditional approach to Bardeen's theory.<sup>75, 76</sup> Duke observed that Bardeen's theory is analogous to Oppenheimer's theory of field ionization of hydrogen. There are two assumptions that are inherent in the Oppenheimer perturbation theory,

- 1. The tunnel coupling is weak enough that the first order Fermi's Golden rule approximation is valid.
- 2. The tip and sample states can be treated as orthogonal to each other.

Additionally, there are important assumptions that are made in Bardeen's theory that are reasonable if the STM tip and sample are considered to be large systems whereby each has an electron reservoir of virtually unlimited capacity.
- The electron-electron interactions (Coulomb repulsion) are ignored. Therefore, a single electron Hamiltonian is applicable. Note that in cases where samples exhibit single-electron charging effects,<sup>79</sup> such as in an SET, the tunneling rates cannot be described simply by Bardeen's theory because of this assumption. (This will become important for single electron transistors and quantum devices.)
- 2. Despite the tunnel coupling, it is assumed that the occupation probability for the tip and sample are independent and remain unchanged.
- 3. The charge relaxation on the tip and sample electrodes in response to tunneling events can be ignored, and the tip and sample are each in electrochemical equilibrium. In other words, the inelastic interactions between the tunneling electrons and the electromagnetic environment of the external circuit (also commonly known as the environmental impedance) are ignored. This is also an assumption that we have adopted in analyzing single electron tunneling in the atomically precise SETs in this thesis.

# 2.3.1 The Perturbation Approach for Tunneling Rates

The above assumptions simplify describing the tunneling process in an STM to solving the Schrodinger equation for a single electron Hamiltonian,

$$H\psi(\vec{r}) = -\frac{\hbar^2}{2m}\Delta\psi(\vec{r}) + V(\vec{r})\psi(\vec{r})$$

Equation 2.2



Figure 2.3 Schematics of the total tunnel junction potential  $V(\vec{r})$  and the isolated sample and tip region potentials  $V_{sam}(\vec{r})$  and  $V_{tip}(\vec{r})$ .

Furthermore, the tunnel junction can be treated as an isolated sample region and tip region that is divided by an arbitrary boundary surface within the barrier,

$$H_{sam}\varphi(\vec{r}) = -\frac{\hbar^2}{2m}\Delta\varphi(\vec{r}) + V_{sam}(\vec{r})\varphi(\vec{r})$$
$$H_{tip}\phi(\vec{r}) = -\frac{\hbar^2}{2m}\Delta\phi(\vec{r}) + V_{tip}(\vec{r})\phi(\vec{r})$$

Equation 2.3

With  $V(\vec{r})$  being the single electron potential of the overall tunnel junction system,  $V_{sam}(\vec{r})$  and  $V_{tip}(\vec{r})$  are illustrated in the schematics of Figure 2.3.  $\varphi(\vec{r})$  and  $\phi(\vec{r})$  are the eigenstates of the isolated sample and tip systems, respectively.

Applying the Oppenheimer approximation, we now seek approximate expressions for single electron scattering rates. We consider the case where an electron is in a sample eigenstate  $\varphi(0)$  at time t = 0 with  $H_{sam}\varphi(\vec{r}) = \varepsilon\varphi(\vec{r})$ . In the weak tunnel coupling regime, the time evolution of the electronic state can be expressed as  $\psi(t) = e^{-\frac{it\varepsilon}{\hbar}}\varphi(0) + \sum_k a_k(t)\phi_k$ , where the summation is over all the bound states of the tip,  $H_{tip}\phi_k = E_k\phi_k$ . Then substituting this expression into the full Hamiltonian and

projecting both sides onto one of the tip states  $\phi_j$  will yield a coupled differential equation for the coefficients  $a_i(t)$ ,

$$i\hbar \frac{d}{dt}a_{j}(t) = e^{-\frac{it\varepsilon}{\hbar}} \langle \phi_{j} | H - H_{sam} | \varphi \rangle + E_{j}a_{j}(t) + \sum_{k} a_{k}(t)\phi_{k} \langle \phi_{j} | H - H_{tip} | \phi_{k} \rangle$$
$$\approx e^{-\frac{it\varepsilon}{\hbar}} \langle \phi_{j} | H - H_{sam} | \varphi \rangle + E_{j}a_{j}(t)$$

Equation 2.4

The assumption of weak tunnel coupling implies that the  $a_k(t)$  terms in the summation that start with  $a_k = 0$  remain small for a short period of time. This is commonly known as the *first order approximation* in tunneling rate calculations. Then the differential equation (Equation 2.4) can be reduced to a solvable form with the following solution,

$$a_j(t) = \frac{e^{-it\varepsilon/\hbar} - e^{-itE_j/\hbar}}{\varepsilon - E_j} \langle \phi_j | H - H_{sam} | \varphi \rangle$$

Equation 2.5

The orthogonality assumption between tip states and sample states gives,

$$\langle \phi_j | \psi(t) \rangle = a_j(t) + \langle \phi_j | \varphi \rangle e^{-\frac{it\varepsilon}{\hbar}} \approx a_j(t)$$

Equation 2.6

Therefore,  $a_j(t)$  can be interpreted as the transmission probability from a sample eigenstate  $\varphi$  to a tip eigenstate  $\phi_j$ . The total transmission rate for an electron initially in the sample eigenstate to transition to tip states, assuming all tip states are available, is then expressed as,

$$\frac{d}{dt}\sum_{j} |a_{j}(t)|^{2} = \frac{d}{dt} 4 \sum_{j} \frac{\sin^{2}(t(E_{j}-\varepsilon)/(2\hbar))}{(E_{j}-\varepsilon)^{2}} |\langle \phi_{j}|H - H_{sam}|\varphi\rangle|^{2}$$
$$= \frac{d}{dt} 4 \sum_{j} P_{t}(E_{j}-\varepsilon)\mathcal{M}^{2}(\phi_{j},\varphi)$$

## Equation 2.7

Fermi's Golden rule states that, under a constant perturbation, the main contribution of  $P_t(x)$  (see Equation 2.7) comes from the interval  $-2h\Gamma < x < 2h\Gamma$ , where  $h\Gamma$  is the quantum broadening of the tunneling event, and  $\Gamma$  is the tunneling rate. Assuming the density of tip states per unit energy can be treated as constant over h/t, Fermi's Golden rule can be applied to approximate the sum by an integral with respect to energy. Typical STM tunneling current is ~50 pA and corresponds to an energy interval of ~1  $\mu$ eV. We now introduce the Pauli exclusion principle and the Fermi-Dirac distribution function,  $F_{\mu_t}(\varepsilon)$ , with the chemical potential of the tip at  $\mu_t$ . Denoting  $\rho_{tip}(\varepsilon)$  as the tip density of states at the energy level  $\varepsilon$  and  $N_{\varepsilon}$  as the number of tip states within the energy interval [ $\varepsilon - 2h/t, \varepsilon + 2h/t$ ], the tunneling rate expression in Equation 2.7 reduces to,

$$\frac{d}{dt}\sum_{j}\left|a_{j}(t)\right|^{2}\approx\left(1-f_{\mu_{t}}(\varepsilon)\right)\frac{2\pi}{\hbar}\mathcal{M}^{2}(\varphi)\rho_{tip}(\varepsilon)$$

Equation 2.8

Here 
$$\mathcal{M}^2(\varphi) = \frac{1}{N_{\varepsilon}} \sum_{j:|E_j - \varepsilon| < 2h/t} \mathcal{M}^2(\phi_j, \varphi)$$
, and  $f_{\mu}(\varepsilon) = \frac{1}{e^{(\varepsilon - \mu)/k_B T} + 1}$ .

Summing up the transmission rate for all the sample states  $\varphi_n$  in both tunneling directions, we obtain the total tunneling current,

 $I = I_{tip \to sam} - I_{sam \to tip}$ 

$$= \frac{2\pi e}{\hbar} \sum_{n} \left[ f_{\mu_t}(\varepsilon_n) \left( 1 - f_{\mu_s}(\varepsilon_n) \right) \right]$$
$$- \left( 1 - f_{\mu_t}(\varepsilon_n) \right) f_{\mu_s}(\varepsilon_n) \left[ \mathcal{M}^2(\varphi_n) \rho_{tip}(\varepsilon_n) \right]$$
$$= \frac{2\pi e}{\hbar} \int_{-\infty}^{+\infty} d\varepsilon \left[ f_{\mu_t}(\varepsilon) \left( 1 - f_{\mu_s}(\varepsilon) \right) \right]$$
$$- \left( 1 - f_{\mu_t}(\varepsilon) \right) f_{\mu_s}(\varepsilon) \left[ \mathcal{M}^2(\varepsilon) \rho_{tip}(\varepsilon) \rho_{sam}(\varepsilon) \right]$$

Equation 2.9

Note that in the above formulation, the bias across the junction is embedded as the chemical potential difference between the sample and the tip,  $eV_{bias} = \mu_t - \mu_s$ . For a continuous state spectrum at the sample with the sample density of states  $\rho_{sam}(\varepsilon)$ , the summation in Equation 2.9 can be replaced by an integral over all energies. See the last part of Equation 2.9, where  $\mathcal{M}^2(\varepsilon)$  is the average of  $\mathcal{M}^2(\varphi_n)$  over all sample states  $\varphi_n$  whose energy lie within a small energy interval at  $\varepsilon$ .

In the small bias limit  $V_{bias} \rightarrow 0$ , the density of states  $\rho_{tip}$  and  $\rho_{sam}$  as well as the transmission probability  $\mathcal{M}^2$  can be treated as constants at the Fermi levels of the tip and sample over a small bias window, and can then be taken out of the integral. Using the properties of the integration of Fermi-Dirac functions,<sup>80</sup>

$$\int_{-\infty}^{+\infty} d\varepsilon f_{\mu_t}(\varepsilon) \left(1 - f_{\mu_s}(\varepsilon)\right) = \frac{eV_{bias}}{1 - \exp(-eV_{bias}/k_BT)}$$
$$\int_{-\infty}^{+\infty} d\varepsilon f_{\mu_s}(\varepsilon) \left(1 - f_{\mu_t}(\varepsilon)\right) = \frac{-eV_{bias}}{1 - \exp(eV_{bias}/k_BT)}$$

Equation 2.10

Substituting the Fermi-integrals into the total tunneling current equation, we obtain the expression in the small bias limit,

$$I = I_{tip \to sam} - I_{sam \to tip} = \frac{2\pi e}{\hbar} \mathcal{M}^2 \rho_{tip} \rho_{sam} e V_{bias}$$

## Equation 2.11

More specifically, in the linear response regime at small bias, if we define the tunnel resistance  $R_T$  as

$$R_T = \frac{\hbar}{2\pi e^2 \mathcal{M}^2 \rho_{tip} \rho_{sam}}$$

## Equation 2.12

Here the density of states  $\rho_{tip}$  and  $\rho_{sam}$  and the transmission probability  $\mathcal{M}^2$  are the corresponding values at the Fermi levels. Then the tunneling rate from the tip to the sample and vice versa can be written as

$$I_{tip\to sam} = e\Gamma_{tip\to sam} = \frac{V_{bias}}{R_T \left[ 1 - \exp\left(-\frac{eV_{bias}}{k_B T}\right) \right]}$$
$$I_{sam\to tip} = e\Gamma_{sam\to tip} = \frac{-V_{bias}}{R_T \left[ 1 - \exp\left(\frac{eV_{bias}}{k_B T}\right) \right]}$$

#### Equation 2.13

At this point, we have obtained the expression for tunneling rates using Fermi's Golden rule to first order. The same derivation will be useful in the study of single electron tunneling in Chapter 6 of this thesis, where single electron charging effects are taken into account and the  $eV_{bias}$  term in the tunneling rate expression in Equation 2.13 is replaced with the change in Helmholtz free energy  $\Delta F$  before and after a single electron tunneling event.

To calculate the matrix element  $\langle \phi_j | H - H_{sam} | \varphi_n \rangle$ , Bardeen has shown that the volume integral can be approximated by a flux integral through an arbitrary surface within the barrier that separates the sample and tip systems.<sup>75, 77</sup> Let the separation surface be denoted as  $\partial T$ , the matrix element simplifies into a flux integral over the separation surface,

$$\langle \phi_j | H - H_{sam} | \varphi_n \rangle \approx -\frac{\hbar^2}{2m} \int_{\partial T} \left[ \overline{\varphi_n(\vec{r})} \nabla \phi_j(\vec{r}) - \phi_j(\vec{r}) \nabla \overline{\varphi_n(\vec{r})} \right] \cdot d\vec{n}$$
  
Equation 2.14

Up until this point, the derived tunneling rate and matrix element formulations are generally applicable for a broad range of tunneling problems. Tersoff and Hamann<sup>81, 82</sup> developed Bardeen's formula for STM applications by modeling the tip states as *s*-orbital type wavefunctions. This formulation leads to straightforward interpretations of the measured STM tunneling current (at the small bias limit) as proportional to sample's *local* density of states per unit volume at the Fermi level  $\mu$  and at the center of the tip,  $\rho_{sam}(\vec{0})$ .

$$I = I_{t \to s} - I_{s \to t} = \frac{2\pi e}{\hbar} \mathcal{M}^2 \rho_{tip} \rho_{sam} eV_{bias} = \frac{h^3 e}{m^2} |A|^2 \rho_{tip} \rho_{sam}(\vec{0}) eV_{bias}$$
Equation 2.15

Here  $|A|^2$  is an averaged normalization constant of the spherically symmetric tip states within the small bias interval.



Figure 2.4 Energy diagram of two electrodes separated by a rectangular tunnel barrier. In the small bias regime where  $eV_{bias} \ll E_{Barr}$ , direct tunneling dominates the electrical transport through the barrier. In ultra-small tunnel junctions where the charging energy becomes non-negligible,  $eV_{bias}$  is replaced by the change of Helmholtz free energy  $\Delta F$  in determining the tunneling rate.

## **2.3.2 WKB Approximation of Rectangular Barriers**

Solving for the tunneling rates using the Oppenheimer approximation, as illustrated in the previous section, requires the overall potential to be a perturbation of a solvable problem. Alternatively, the tunneling rates in STM and other generalized tunnel junctions are commonly estimated using the semi classical Wenzel-Kramers-Brillouin (WKB) approximation (see Figure 2.4), which is valid provided that the de Broglie wavelength of the incident particles is small compared with the spatial extent of the tunnel barrier thickness. The WKB approach is the most straightforward way to calculate the exponential dependence of the transmission probability on the barrier gap distance. In Chapter 6 of this thesis, we will use the WKB approximation to estimate the tunnel barrier height in our atomically precise Si:P SETs. A generalized formula has been derived by Simmons <sup>83, 84</sup> for the tunneling current between metallic electrodes separated by a thin insulating film. Starting with the tunneling probability expression,  $D(E_x)$ , from the WKB approximation,

$$D(E_x) = \exp\left\{-\frac{4\pi}{h}\int_0^s [2m(V(x) - E_x)]^{\frac{1}{2}}dx\right\}$$

Equation 2.16

Here *s* is the barrier width and  $E_x = \hbar^2 k_x^2/2m$  is the kinetic energy component of the incident electron in the *x* (tunneling) direction. Assuming the two electrodes to be three-dimensional with an isotropic conduction band valley centered at k = 0, the net electron flow density through the barrier can be expressed as,

$$J = \int_{0}^{E_{m}} D(E_{x}) dE_{x} \left\{ \frac{4\pi m^{2} e}{h^{3}} \int_{0}^{\infty} [f(E) - f(E + eV)] dE_{r} \right\}$$

Equation 2.17

Here  $E_m$  is the maximum energy of the electrons in the electrodes (zero temperature approximation),  $E_r$  is the energy associated with the motion perpendicular to the tunneling direction, and f is the Fermi-Dirac function. For a rectangular barrier in the low-voltage regime  $V_{bias} \cong 0$  (as shown in Figure 2.4), the above expression can be simplified to the following form, <sup>83, 84</sup>

$$J = \left[\frac{(2mE_{Barr})^{\frac{1}{2}}}{s}\right] \left(\frac{e}{h}\right)^2 V_{bias} \exp\left[-\frac{4\pi s}{h}(2mE_{Barr})^{\frac{1}{2}}\right]$$

Equation 2.18

Assuming the cross-sectional area of the tunnel junction to be A, the effective tunnel resistance R in this linear response assumption can be expressed as

$$R = \frac{V_{bias}}{A \cdot J}$$

Equation 2.19

In the case of a single ultra-small tunnel junction for which the charging effects on the electrode plates cannot be ignored, the  $V_{bias}$  in the above *R* and *J* expressions will be replaced with the change in Helmholtz free energy  $\Delta F$  before and after a single electron tunneling event.

In an STM-patterned Si:P tunnel junction, the barrier height can be roughly estimated as the difference between the Fermi energy of the electrodes and the conduction band minimum. We expect exponential dependence of the tunnel conductance on both the barrier height and barrier gap distance, whereas a linear dependence on the tunneling cross-sectional area is expected. The experimental demonstration of this behavior in STM patterned Si:P devices is an important result of this thesis.

# **2.4 STM Operation Modes**

# 2.4.1 Imaging Modes of STM

Constant current and constant height modes are the two commonly used STM imaging modes. In the constant current imaging mode, the tunneling current is maintained at a set-point current during scanning while the tip height is adjusted through a feedback control loop. The tip height (z) values are recorded as a function of the lateral piezo displacement of the tip. Following Tersoff-Hamann's interpretation, <sup>81</sup> the recorded z-

map represents a surface contour of a constant local sample density of states  $\rho_{sam}(\vec{0})$ . The actual  $\rho_{sam}(\vec{0})$  value depends on the bias and set-point current conditions. In the constant-height imaging mode, the tip height remains constant above the sample surface without engaging a feedback control loop. The tunneling current is recorded as a function of the lateral piezo displacement of the tip. This recorded tunneling current map represents the local sample density of states  $\rho_{sam}(\vec{0})$  variations at the position of the tip.

# 2.4.2 Scanning Tunneling Spectroscopy

Scanning tunneling spectroscopy (STS) encompasses an ever-growing collection of techniques for characterizing the electronic properties of surfaces at the atomic scale.<sup>85</sup> Earlier work on STS focused on characterizing the local density of states by holding the tip over a giving point on the surface and acquiring the I-V or differential conductance curves.<sup>86, 87</sup> Recent developments in STS greatly expanded the scope of STS applications ranging from characterizing spin-polarized excitations for quantum materials<sup>88</sup> to characterizing single subsurface dopants for qubit applications.<sup>68, 89</sup>

Here we briefly review the application of current-voltage STS to the study of local density of states (LDOS) in a sample. Following Feenstra's original formulation,<sup>86, 87</sup> at finite bias V, the total tunneling current can be approximately expressed as,

$$I \propto \int_{0}^{eV} \rho(E)T(E, eV)dE$$

where  $\rho(E)$  is the sample LDOS at the tip center ( $\rho_{sam}(\vec{0})$  in the Tersoff-Hamann formula), and T(E, eV) is the transmission probability ( $\mathcal{M}^2$  in the Tersoff-Hamann formula). Computing the first order derivative over the bias will highlight the sample LDOS features, as expressed in Equation 2.21.

$$\frac{dI}{dV} \propto e\rho(eV)T(eV,eV) + e\int_{0}^{eV} \rho(E)\frac{d}{d(eV)}[T(E,eV)]dE$$

Equation 2.21

However, because of the exponential decay of the tunneling current over tip-sample separation s, the amplitudes of the measured sample DOS at different s also follow this exponential relation. Because one does not have absolute control over the tip-sample separation at different surface locations due to variations in surface topography at the atomic scale, it becomes inconvenient to compare the measured sample DOS features across different surface sites. Feenstra *et al.*<sup>87</sup> have shown that, by normalizing the differential conductance with the measured conductance, one can remove the experimental dependences of the tip-sample separation. This will be discussed in more details in Chapter 4.

# 2.4.3 Atomic Manipulation using STM

Atomic manipulation using the scanning tunneling microscope (STM) has been motivated by a desire to fabricate atomically precise nanostructures.<sup>70, 90</sup> Detailed understanding and precise control of STM tip-surface interactions is a key to successful

atom-scale device fabrication and in-situ characterization. Historically, different mechanisms have been proposed to explain the observed modifications on different surfaces due to tip-surface interactions, such as field evaporation, <sup>90, 91, 92, 93, 94, 95, 96, 97,</sup> <sup>98</sup> mechanical contact, <sup>91, 92, 96, 97, 99</sup> Joule heating, <sup>99, 100, 101</sup> electron induced desorption or sublimation,<sup>102</sup> and chemical reactions,<sup>103, 104</sup> etc.<sup>105</sup> Mass exchange between the tip and the surface has been an obvious way to modify local surface properties at large scales. For instance, controlled deposition of tip materials has been used to fabricate atomically registered nanodots as well as electrical contacts and interconnects among atomically precise quantum devices in silicon.<sup>106</sup> At the atomic scale, the attractive and repulsive forces between the tip and an adsorbate have been utilized to drag atoms and molecules across the surface and form artificial lattice structures.<sup>70, 107</sup> Electronic and vibrational excitations can be induced through inelastic tunneling processes that achieve selective chemical dissociation/synthesis,<sup>108, 109, 110</sup> desorption of individual adsorbates,<sup>48, 111</sup> as well as the reversible transfer of single atoms/molecules between the surface and the tip.<sup>112</sup>

On Si surfaces, in particular, the rich physics in STM tip-induced atomic scale modification has been explored by numerous groups including tip-sample chemical interactions, field evaporation in tunnel junctions, tunneling to point contact transitions, and tunnel junction and Schottky-barrier contact properties.<sup>93, 113, 114, 115, 116, 117, 118, 119, 120</sup>

Besides the direct manipulation of single Si atoms on clean Si surfaces,<sup>121</sup> atomic-scale functionalization of hydrogen-terminated Si (100) surfaces [H:Si (100)] has held the greatest promise for precise atomic manufacturing in Si.<sup>47, 51, 57, 122</sup> The electron stimulated desorption (ESD) of H from Si surfaces was first reported by Becker et al. on hydrogen-terminated Si (111) surfaces by elevating the STM bias and tunneling current beyond the standard imaging conditions.<sup>102</sup> In 1994, Lyding, Shen, Tucker, *et al.*<sup>49</sup> demonstrated the first selective desorption of hydrogen atoms from the hydrogen-terminated Si (100) surface as well as area-selective chemistry on a patterned Si(100) surface in a UHV environment. Two hydrogen desorption mechanisms have been proposed which correspond to two distinct STM operation regimes for hydrogen lithography applications.<sup>48</sup> (See Figure 2.5) When an external potential beyond the work functions of both the tip and the H-terminated Si (100) surface is applied across the tunnel junction (typically between 6 and 8 volts), the STM operates in a field emission mode and the emitted electrons can be accelerated with high kinetic energies. Under such conditions, the breaking of silicon-hydrogen  $\sigma$  bonds is dominated by a direct electronic excitation mechanism where the silicon-hydrogen valence bonds are excited from a  $\sigma$  bonding state to a  $\sigma^*$  anti-bonding state. When the applied bias is lower and the STM operates in the tunneling regime (typically between 3 and 5 volts), the desorption of hydrogen atoms occurs predominately through a multi-electron vibrational heating mechanism in which thermal excitation breaks the silicon-hydrogen bonds. Alternatively, a coherent-resonant electron scattering mechanism has also been proposed to describe hydrogen desorption at low bias voltages as a two-electron process.<sup>123</sup>



Figure 2.5 The mechanisms of selective hydrogen desorption using STM: (a) direct electronic excitation mechanism where the Si-H bond electrons can be directly excited from a  $\sigma$  bonding state to a  $\sigma^*$  anti-bonding state. The desorption efficiency is determined by competition between the time evolution of the Si-H bonding distance and the relaxation rate of the excited electrons. (b) multi-electron vibrational heating mechanism. The desorption efficiency is determined by the competition between vibrational heating and cooling of the bond electrons. Plot (a) is taken from Abeln.<sup>124</sup>

# 2.5 Silicon

Silicon has laid the foundation of the modern semiconductor industry, which has led to the on-going information revolution. It has also become increasingly evident that Si may be an excellent host material for forthcoming solid-state quantum computing technology. Because of its technological and scientific importance, Si has become one of the most-studied elements on the periodic table. In this section, we briefly introduce Si as a substrate material with a specific emphasis on the Si (100) surface, which is the starting point of Si:P atomic device fabrication.

Silicon is a group IV element with an atomic number of 14. In bulk, single crystal silicon, each silicon atom forms sp3 hybridized covalent bounds with four neighboring silicon atoms in a tetrahedral way that takes the form of the diamond-type face centered cubic (FCC) lattice, as shown in Figure 2.6. The cube side (lattice constant) for silicon is a = 5.43 Å.



Figure 2.6 A schematic image of the bulk Si single crystalline structure. This figure is taken from Ashcroft and Mermin.<sup>125</sup>

Figure 2.7 depicts the first Brillouin zone and the band structure of silicon in *k*-space. Bulk intrinsic silicon has an indirect band gap of ~1.12 eV at room temperature. The conduction band minima are located at  $k = 0.85 \frac{2\pi}{a}$  along the <100> directions that form six equivalent and energetically degenerate valleys of the conduction band. <sup>28</sup>Si has nuclear spin zero and is the most abundant silicon isotope, comprising ~92% of natural silicon.



Figure 2.7 The band structure of bulk single crystal silicon. (a) diagram of the first Brillouin zone of a face-centered cubic lattice. (b) Simplified band structure of bulk silicon with the high symmetry points marked in (a). The red arrow indicates the position of the conduction band minimum. The grey band indicates an indirect bandgap of approximately 1.12 eV at 300 K. The plots are taken from Chelikowsky.<sup>126</sup>

# 2.5.1 Si (100) Surfaces

A Si (100) surface is obtained by cleaving single-crystal Si along a (100) lattice plane, which exposes two unsaturated Si dangling bonds at each Si (100) surface atom. To lower the surface energy, the surface atoms relax into a 2×1 surface reconstruction configuration. Two silicon atoms dimerize and form a covalent  $\sigma$  bond and a weaker  $\pi$ bond, resulting in filled  $\sigma$  and  $\pi$  bonding orbitals and empty  $\sigma^*$  and  $\pi^*$  antibonding orbitals. On a clean Si (100) surface, an STM images the spatial LDOS distribution of the  $\pi^*$  and  $\pi$  orbitals at positive and negative sample biases, respectively. (The energy levels of the  $\sigma$  and  $\sigma^*$  orbitals are typically outside of the STM bias window in imaging mode) Si dimers form dimer rows in parallel along the [110] direction, with a pitch of 7.68 Å. The separation between adjacent dimers within a dimer row is 3.84 Å. The surface atom density is  $6.78 \times 10^{14}$ /cm<sup>2</sup> on the Si (100) surface. Miscut angles from the (100) plane result in steps and terraces, where dimer rows on one terrace orient orthogonally to those on adjacent terraces due to the stacking sequence of the diamond lattice. The step height is  $a/4 \approx 1.36$  Å, which equals the separation between neighboring Si atoms in single-crystal Si.



Figure 2.8 Schematics for a reconstructed Si (100) surface in the ground state. (a) Sideview schematic of a dimer row on a reconstructed Si (100) c (4×1) surface, where the silicon atoms within a dimer buckle alternately along a dimer row. (b) Top-view schematic indicating a unit cell of the c (4×2) symmetry. (c) The Brillouin zone for the c (4×2) cell (solid lines) and 2×1 cell (dashed lines). (d) Simplified surface band structure of reconstructed Si (100) c (4×2) surfaces along the line  $\Gamma - J'_2$  in the first surface Brillouin zone in (c). The dots are calculated dangling-bond surface-state quasiparticle energies. The crosses are experimental results from angle-resolved photoemission experiments from Johansson *et al.*<sup>127</sup> The shaded regions are the projected bulk Si band structures. These figures are reproduced from Northrup.<sup>128</sup>

Theoretical calculations reveal that the ground state of the Si (100) surface energetically favors a c (4×2) surface reconstruction rather than the 2×1 reconstruction. <sup>129, 130, 131</sup> In the c (4×2) reconstruction, as illustrated in Figure 2.8, dimers are tilted alternately along a dimer row. The two  $\pi$  orbitals and two  $\pi^*$  orbitals, conventionally labeled as  $\pi_1$ ,  $\pi_2$ ,  $\pi_1^*$ , and  $\pi_2^*$  molecular orbitals, arise from the four "dangling bond" electrons in a c (4×2) surface unit cell. Spatial overlap of molecular orbitals among neighboring c (4×2) unit cells broadens the filled  $\pi$  and empty  $\pi^*$  orbitals into surface bands, as depicted in the surface Brillouin zone of Figure 2.8 (c), where the existence of a surface band gap makes the Si (100) c(4x2) surface semiconducting. In Chapter 4, we will present a detailed investigation of the Si (100) surface band structure along monolayer step edges using spatially resolved scanning tunneling spectroscopy. At room temperature, thermal excitation switches a dimer rapidly between two energetically degenerate, asymmetric configurations that leads to dynamic buckling.<sup>132</sup> However, because of the time-averaging effect of dynamic buckling during STM image data acquisition, dimers appear to be symmetric in a typical STM image and the Si (100) surface appears to have a  $2\times1$  reconstruction. Surface defects or step edges can break the energy degeneracy of the two asymmetric buckling configurations at adjacent dimers and locally suppress dynamic buckling. Alternatively, dynamic buckling can also be suppressed at low temperature where thermal excitation no longer overcomes the energy barrier between the two asymmetric buckling configurations.<sup>133, 134</sup>

# 2.5.2 Interaction of Hydrogen with Si (100) Surfaces

Si-dangling bonds on clean Si (100) surfaces are chemically reactive. In a UHV environment, molecular hydrogen has a negligible sticking coefficient on clean Si (100) surfaces whereas atomic hydrogen has a sticking coefficient that approaches one. Exposing a clean Si (100) surface to atomic hydrogen forms an atomic layer of hydrogen resist on the surface while also making it chemically inert. Hydrogen depassivation lithography using an STM can selectively remove the hydrogen resist and re-expose chemically reactive Si-dangling bonds on the H-terminated Si (100) surface, allowing for selective adsorption of gaseous precursors onto the patterned regions.

Both substrate temperature and partial pressure of atomic hydrogen affect the adsorption phase of H on Si (100) surfaces (See Figure 2.9).<sup>135, 136</sup> Exposing a clean Si (100) surface to atomic H at a substrate temperature between  $\sim$ 350 °C and  $\sim$ 420 °C

results in a monohydride resist, where incoming H atoms break  $\pi$  bonds and one H atom is attached to each surface Si atom, forming a reconstructed H:Si (100) 2×1 surface. There exists a finite probability that incoming H atoms will break both the  $\sigma$  and the  $\pi$  bond in a dimer and form dihydride, where two H atoms are attached to one surface Si atom. Partial desorption of H can convert the dihydride phase into the monohydride phase through an intermediate H (3×1) phase. Also, a hemihydride phase can exist for incomplete hydrogen termination or during H-desorption. Significant thermal desorption of H from Si (100) surfaces starts to occur when the substrate temperature is raised above ~420 °C and H atoms desorb in pairs forming H<sub>2</sub> molecules.<sup>137</sup>



Figure 2.9 Different phases of H-termination on Si (100) surfaces. Figure taken from Schofield.<sup>138</sup>

## 2.5.3 Interaction of Phosphine with Si (100) Surfaces

Selective adsorption of gaseous precursors that are compatible with hydrogen lithography techniques on Si (100) surfaces has been extensively studied with a variety of gaseous species, such as  $O_2$ , NH<sub>3</sub>, and PH<sub>3</sub>.<sup>49, 50, 122, 139</sup> In this section, we briefly

review the chemical reactions of  $PH_3$  adsorption and P incorporation on Si (100) surfaces.

At room temperature, PH<sub>3</sub> has a sticking coefficient approaching 1 at exposed Si-dangling bonds on Si (100) surfaces. As illustrated in Figure 2.10, extensive STM and ab-initio investigations have revealed the dissociation pathway of PH<sub>3</sub> upon adsorption.<sup>53, 140, 141, 142</sup> Sequentially, a PH<sub>3</sub> molecule dissociates into PH<sub>2</sub> + H, PH + 2H, and P + 3H configurations where the dissociated H atoms terminate adjacent Si-dangling bond sites, making the adsorption a self-limiting process. At high doses, the adsorbed PH<sub>3</sub> competes for the available dangling bond sites, and the dissociation reaction becomes a stoichiometric process. For saturation-dosed Si (100) surfaces at room temperature, a phosphorus coverage of ~0.37 ML is the most commonly reported value in the literature.<sup>143, 144, 145, 146, 147, 148, 149</sup>

Upon thermal annealing of the saturation dosed surface at a temperature between 250 °C to 600 °C, most of the adsorbed PH<sub>x</sub> (x=0,1,2) dissociate entirely (leaving isolated P atoms bound to the underlying Si) while the remaining PH<sub>x</sub> recombine with H and desorb into the PH<sub>3</sub> gas phase. It is energetically favorable for the isolated P atoms to substitutionally switch positions with the top layer of Si atoms and form Si-P heterodimer structures.<sup>52, 53, 54</sup> The substituted Si atoms are ejected onto the surface and nucleate into small islands.<sup>54</sup> It has been found that the P coverage reduces from ~0.37 ML to ~0.25 ML after the incorporation anneal. Thermal desorption of P from Si surfaces has been reported at temperatures above 600 °C.<sup>150, 151</sup>



Figure 2.10 Schematics showing progressive dissociation of an adsorbed phosphine molecule on clean Si (100) surfaces at room temperature. A thermal anneal at ~350 °C incorporates the P atom into the top layer of Si.<sup>141, 152</sup> Figure taken from Goh.<sup>153</sup>

# 2.5.4 Epitaxial Overgrowth on Si (100) Surfaces

Embedding STM patterned Si:P devices in an all-epitaxial Si environment is essential to electrically activate the donors and isolate the donors from surface and interface defects.. In this section, we briefly review Si homoepitaxial overgrowth at low temperatures.

Epitaxial overgrowth, as opposed to amorphous overgrowth, is an overgrowth process where the adatoms rearrange themselves to match the substrate lattice and grow in a crystalline manner. The primary methods for Si homoepitaxial overgrowth include chemical vapor deposition (CVD) and molecular beam epitaxy (MBE). In CVD overgrowth, clean Si surfaces are dosed with silane (SiH<sub>4</sub>) at elevated temperatures where SiH<sub>4</sub> decomposes into Si atoms on the surfaces and the H atoms desorb. In MBE overgrowth, source Si is vaporized into a flux of Si atoms using e-beam or direct current heating and then deposited onto a Si substrate. Figure 2.11 illustrates a variety of atomic-scale dynamic processes that occur at the growth-front during MBE overgrowth.<sup>154</sup> An impinging adatom may land on top of a flat terrace or a preexisting 2-D island. The adatom can diffuse across the terrace or island if its thermal energy

overcomes the surface diffusion barriers, which can be anisotropic on flat terraces and is also different at step edges. If two diffusing adatoms meet, they may form a nucleus that grows into a stable 2-D island as adatoms continue attaching to the island. The diffusing adatoms can also attach to preexisting step edges and result in the well-known step "flow" process. At the same time, some adatoms detach from islands and step edges or desorb from overgrowth surfaces. As the surface atoms become bulk and the adatoms become new surface atoms during overgrowth, surface reconstruction also affects the adatoms' behavior.

The growth front morphology is profoundly influenced by dynamic equilibrium among the fundamental behaviors of adatoms, which is determined primarily by the adatom flux rate and the growth-front temperature. At a given adatom flux rate, increasing the surface temperature promotes the adatom mobility on growth-front surfaces so that the adatoms are more likely to reach and attach onto terrace steps. Decreasing the surface temperature, on the other hand, reduces adatom mobility and enhances the formation of stable islands on flat terraces. At a given surface temperature, increasing the adatom flux rate increases the chance of nucleation on terraces or preexisting islands. Decreasing the adatom flux rate, on the other hand, reduces the chance of adatoms meeting each other during diffusion, and the adatoms are more likely to attach onto terrace edges. Therefore, moving within the parameter space from high growth temperature and low growth rate to low growth temperature and high growth rate, the epitaxial growth modes gradually transition from a step flow growth mode to a layer-by-layer growth mode, to a 2-D island growth mode, and finally to a 3-D island growth mode.<sup>155</sup>

Growth front roughness can be used as an indicator of epitaxy quality. At a given growth temperature and growth rate, there exists an epitaxial thickness beyond which the epitaxy breaks down due to the buildup of growth front roughness.<sup>156</sup> Though cross-sectional TEM has conventionally been used as a standard method to characterize the epitaxial quality, the averaging effect over the finite lamella thickness [on the order of ~(50 to 80) nm] complicates the interpretation of high-resolution TEM images. For this reason, STM observation of growth front roughness not only provides an alternative way to characterize the epitaxial quality but also provides a lateral resolution that is particularly suitable for comparing the epitaxial quality difference between the inside and outside of STM-patterned Si:P devices. Characterization of epitaxial quality in STM-patterned devices and blanket  $\delta$ -layers will be presented in Chapters 3 and 5.



Figure 2.11 Schematics that summarize the fundamental behaviors of ad-atoms on a clean surface during an epitaxial overgrowth process using the molecular beam epitaxy (MBE) growth method. Image is taken from Voigtländer.<sup>154</sup>

## **2.5.5 Si:P δ-doped Systems**

The 2D confinement in Si:P monolayers [in the Si (100) plane] lifts the single-crystal bulk Si valley degeneracy in the [010] direction. This leads to the formation of two  $\Gamma$  sub-bands and a four-fold degenerate  $\Delta$  sub-band in the [010] and [100] projection directions, respectively (see Figure 2.7). The effective mass of free electrons traveling in a phosphorus-doped delta layer plane is isotropic in the two  $\Gamma$  sub-bands and anisotropic in the four  $\Delta$  sub-bands. The band structure and occupation of the conduction band in Si:P monolayers in the Si (100) plane have been intensively studied using effective mass theory (EMT) and density functional theory (DFT).<sup>157, 158, 159, 160, 161</sup>



Figure 2.12 Band structure and electron density distribution in 2-D  $\delta$ -doped Si:P monolayers. (a) Schematic of the 6-fold degenerate conduction band valleys within the first Brillouin zone of bulk silicon. For 2-D confinement in the z [001] orientation, the

valleys are projected onto the Si:P  $\delta$ -doped (001) plane, i.e., the x-y plane. (b) The calculated band structure of a saturation doped (1/4 ML P coverage) Si:P monolayer. (c) The calculated electron density distributions in the z-direction for a  $\delta$ -doped Si:P monolayer with different levels of P coverage. Plots in (b) and (c) are taken from Carter.<sup>157</sup>

Carter *et al.* have performed DFT calculations on the 2-D sub-band structures and donor electron density distributions in P-doped monolayers at different P coverages,<sup>157</sup> [as shown in Figure 2.12 (b) and (c)] where a large supercell was used to include the effect of dopant disorder in the simulation. The simulations predict that the Fermi level of saturation-doped Si:P monolayers ranges from ~80 meV to ~130 meV below the conduction band minimum of bulk silicon, and the energy splitting between the minima of  $\Gamma_1$  and  $\Gamma_2$  sub-bands is about 60 meV. For 1/4 ML P coverage, the electron density drops to 1/10 of its peak value at approximately 1 nm from the doping plane.

# **2.6 Single Electron Transistor (SET)**

Single electron transistors (SETs) have been used as ultra-sensitive charge sensors for spin-readout and initialization in atomically precise Si:P qubit devices. Single electron tunneling spectroscopy measurements on quantum dots and single donors are essential for understanding the confinement potentials and single donor properties for quantum information processing.<sup>162</sup> Following the discussions of Grabert *et al.*<sup>78</sup> and Kouwenhoven *et al.*,<sup>162</sup> in this section, we review the fundamentals of single electron transport in SETs, for both the classical and quantum-dot regimes. A study of atomic-

scale control of the tunnel coupling in Si:P single electron transistors will be presented in Chapter 6.



Figure 2.13 Schematics of a single electron transistor (SET) and the Coulomb blockade phenomena. (a) In an SET, a conducting island (or "dot") is tunnel-coupled to drain and source electrodes (reservoirs) and capacitively coupled to a gate electrode. With a sufficiently small dot at low temperatures, the Coulomb blockade effect dominates the electrical transport through the island. (b) An equivalent circuit diagram of an SET, where the tunnel junction is treated as a tunnel resistance and capacitance connected in parallel. We adopt an asymmetric bias configuration in all the SET measurements in this study, where the source electrode is grounded, and both the drain-source bias  $V_{DS}$ and the gate voltage  $V_{GS}$  are applied with respect to the source ground. (c) The energy diagram of an SET, where  $\mu_S$  and  $\mu_D$  are the chemical potentials of the source and drain leads (reservoirs) respectively;  $\mu_{IS}(N)$  is the chemical potential to add the

 $(N + 1)^{st}$  electron onto the island when the island is occupied with N excess electrons.  $E_{Barr}$  is the barrier height defined by the energy difference between the electrodes' Fermi level and the conduction band edge of the substrate. We assume a rectangular barrier shape in this study. (d) Energy diagrams representing a single electron transistor at small source-drain bias. The number of excess electrons on the dot is quantized with successive chemical potential levels separated by the addition energy  $E_{add}$ . In the upper panel, current is blocked and the number of excess electrons on the dot is fixed. In the lower panel, the Coulomb blockade can be removed when the electrochemical potential of the dot is brought into tunnel resonance with the source-drain electrodes. (e) Continuously sweeping the gate voltage shifts the electrochemical potential of the dot, which leads to conductance oscillations across the source and drain electrodes (Coulomb oscillations). The number of electrons on the dot is constant within the blockaded regions. (f) Charge stability diagram obtained by measuring the source-drain conductance while sweeping the gate voltage and source-drain bias. Conductance is blocked within the shaded diamonds (Coulomb diamonds). The addition energy  $E_{add}$ , gate lever arm  $\alpha_G$ , and mutual capacitances can be extracted from the dimensions of the Coulomb diamonds.

A single-electron transistor consists of a conducting island (or quantum dot) that is capacitively coupled to gate electrodes and tunnel- and capacitively coupled to source and drain electrodes. (See Figure 2.13) The gate and source/drain electrodes are assumed to be metallic with continuous DOS distributions. For an ultra-small island at low temperatures and with small source-drain bias, the conductance through the island is suppressed because of a classical charging energy  $E_C = e^2/C_{\Sigma}$ , where  $C_{\Sigma} = C_S + C_D + C_G$  represents the total capacitance of the island. This suppression of single electron tunneling events due to the charging energy is known as Coulomb blockade. Coulomb blockade can be removed by applying a gate voltage that capacitively brings the discrete charging energy levels of the island into tunnel resonance with the source-drain electrodes. Continuously sweeping the gate voltage will result in conductance oscillations as a function of the gate voltage, known as Coulomb blockade oscillations.

Two basic conditions are required for observing single electron phenomena in an SET. First,  $E_c$  must be larger than the thermal energy  $k_BT$  to prevent thermal fluctuations at the Fermi levels of the source and drain leads from overcoming the Coulomb blockade barrier. This condition can be fulfilled by fabricating very small SET islands with small  $C_{\Sigma}$  (therefore large  $E_c$ ), and having the SET operated at cryogenic temperatures,

$$E_C = \frac{e^2}{C_{\Sigma}} \gg k_B T$$

Equation 2.22

where  $k_B$  is Boltzmann's constant and T is the absolute temperature.

Second, the tunnel coupling between the island and source/drain leads must be weak enough to suppress fluctuations of the number of electrons on the island. In other words, the lifetime broadening of the electron charging energy levels on the dot due to the tunnel coupling to the source/drain leads must be smaller than  $E_c$ . Based on the energy-time uncertainty principle, where the relevant energy and time uncertainty scales are the charging energy and the time to charge or discharge the island, we have

$$\Delta E \Delta t = \frac{e^2}{C_{\Sigma}} (R_{S,D} C_{\Sigma}) \gg h$$
$$R_{S,D} \gg \frac{h}{e^2} \approx 25.8 \text{ k}\Omega$$

#### Equations 2.23

Here  $R_{S,D}$  is the tunneling resistance between the source (drain) and the island, *h* is Plank's constant. This second condition can be fulfilled by fine-tuning the sourceisland and drain-island tunnel barriers to achieve good electron localization on the island while still maintaining finite tunneling (typically  $R_{S,D} \ll 1 \text{ T}\Omega$ ) for the blockade effect to be measurable.

## **2.6.1 Constant Interaction Model**

Electrical transport through an SET can be well described using the constant interaction (CI) model.<sup>163</sup> [See Figure. 2.13 (b)] Even with its simplicity, the CI model has been successfully applied to quantum dot systems with dots ranging from large metallic islands and semiconductor quantum dots<sup>162</sup> to single donors.<sup>164, 165</sup> The two essential assumptions of the CI model are:

- 1. The quantum levels on the dot can be calculated independently of the number of electrons on the dot.
- 2. The Coulomb interactions among electrons on the dot as well as between the electrons on the dot and those in the environment can be parameterized by constant capacitances, which are independent of the number of electrons on the

dot and the applied bias and voltage. This assumption is valid when the dot size is much larger than the screening length (i.e., no electric field inside the dot).<sup>162</sup>

The two characteristic energies in SET operation are electron-electron interaction energy (i.e., electrostatic capacitive charging energy  $E_C$ ) and quantum confinement energies due to small island sizes. The electronic state energy spacing (single particle level spacing),  $\Delta E$ , due to quantum confinement increases as the island size decreases.

The total energy of the dot, U(N), with N excess electrons in their ground state, can be expressed as

$$U(N) = \frac{1}{2}C_{\Sigma}V_{IS}^2 + \sum_{i=1}^{N}\varepsilon_i$$

Equation 2.24

where  $V_{IS}$  is the dot (island) potential relative to the ground, and  $\varepsilon_i$  is the single-particle energy of the  $i^{th}$  electron on the dot. The chemical potential  $\mu_{IS}(N)$  of the island is defined as the energy required to add the  $(N + 1)^{st}$  electron onto the island when the island is occupied with N excess electrons,

$$\mu_{IS}(N) = \int_{N}^{N+1} -eV_{IS}(n)dn = U(N+1) - U(N)$$

#### Equation 2.25

The energy spacing between the chemical potentials for adding the  $(N + 1)^{st}$  and the  $N^{th}$  electron onto the dot is commonly referred to as the addition energy,  $E_{add} = \mu_{IS}(N) - \mu_{IS}(N - 1)$ , which is the summation of charging energy and the single particle level spacing. The ratio of the gate capacitance and total capacitance is

commonly known as the lever arm,  $\alpha_G = C_G/C_{\Sigma}$ , that denotes how effective the gate is in changing the dot potential.

# 2.6.2 Electrical Transport in Metallic SETs

If  $\Delta E \ll k_B T \ll E_C$ , the electrical transport in an SET is in the classical Coulomb blockade regime where  $E_{add} \approx E_C$  and the dot can be treated as a metallic island with a continuum of energy levels. A description of the electrical transport in metallic SETs has been established by the well-known orthodox theory.<sup>78, 80, 162</sup> In this section, we review the fundamentals of the orthodox theory and present a compact analytical model for simulating the single-electron tunneling in metallic SETs.

In the orthodox theory, the energy that determines the transport of single electrons through an SET is the Helmholtz free energy F = U - W, where U is the total electrostatic energy stored in the system and W is the work done by voltage sources. The change in F due to a single-electron tunneling event is a measure of the tunneling probability; at the zero-temperature limit, a single electron tunneling event can only happen if it results in a negative change in F. When there are N excess electrons on the island, based on charge conservation, the electrostatic potential of the island,  $V_{IS}(N)$ , can be expressed as,

$$V_{IS}(N) = \frac{1}{C_{\Sigma}} \left[ (-Ne + Q_0) + (C_D V_{DS} + C_G V_{GS}) \right]$$

#### Equation 2.26

Here  $Q_0 (|Q_0| \le \frac{e}{2})$  represents the fractional electron charge that is present on the island when the voltage electrodes are floating, typically due to background charges from the environment. Therefore, the electrochemical potential of the island can be expressed as,

$$\mu_{IS}(N) = \int_{N}^{N+1} -eV_{IS}(n)dn = \frac{e^2}{2C_{\Sigma}} - e\frac{C_D V_{DS} + C_G V_{GS} - (Ne - Q_0)}{C_{\Sigma}}$$

Equation 2.27

The change in Helmholtz free energy  $\Delta F$  of the SET system due to a single-electron tunneling event can be expressed as the chemical potential difference between the finial state and the initial state of the tunneling electron. We adopt the convention that  $\Delta F_S^{N+1,N}$  represents the  $\Delta F$  when an electron tunnels from the source to the island and changes the number of excess electrons on the island from N to N + 1. We list all four variations for  $\Delta F$  below.

$$\Delta F_{S}^{N+1,N} = -\mu_{S} + \mu_{IS}(N)$$
  
=  $\frac{e}{C_{\Sigma}} \left( \frac{e}{2} + (Ne - Q_{0}) - C_{D}V_{DS} - C_{G}V_{GS} \right)$ 

$$\Delta F_S^{N,N+1} = \mu_S - \mu_{IS}(N) = -\Delta F_S^{N+1,N}$$

$$\Delta F_D^{N+1,N} = -\mu_D + \mu_{IS}(N)$$
  
=  $\frac{e}{C_{\Sigma}} \left( \frac{e}{2} + (Ne - Q_0) + (C_S + C_G)V_{DS} - C_G V_{GS} \right)$ 

$$\Delta F_D^{N,N+1} = \mu_D - \mu_{IS}(N) = -\Delta F_D^{N+1,N}$$

Equations 2.28

The corresponding expressions for the tunneling rate and tunnel resistance for the single electron tunnel event are given in Equations 2.29 and 2.30.<sup>78, 80</sup> Here the single electron tunneling rate  $\Gamma_T$ , where the subscript T = S, D denotes the tunnel junction on the source or drain side respectively, is calculated using Fermi's golden rule approximation. For simplicity, we assume the single electron tunneling events to be elastic without electromagnetic interactions between the tunneling electron and the environmental impedance.<sup>166</sup>

$$\Gamma_T = \frac{2\pi}{\hbar} |A|^2 D_i D_f \int dEf(E) [1 - f(E - \Delta F)] = \frac{1}{R_T e^2} \frac{-\Delta F}{1 - \exp(\frac{\Delta F}{k_B T})}$$

Equation 2.29

$$R_T = \frac{\hbar}{2\pi e^2 |A|^2 D_i D_f}$$

### Equation 2.30

The drain-source bias window (typically < 10 meV when measuring metallic SETs) within the Coulomb blockade regime is small compared to the barrier height (on the order of 100 meV). Hence, we work in the linear response regime where an individual tunnel junction barrier gives a linear I - V characteristic when neglecting charging effect. In this regime, the tunneling matrix element A and the initial (final) density of states  $D_i$  ( $D_f$ ) can be treated as constants over the bias window and can be taken out of the integral. The physical tunnel barrier parameters are embedded in the tunnel resistance  $R_T$ .<sup>80</sup> We emphasize that the tunnel resistance should not be confused with Ohmic resistance because of the different charge transport nature through a tunnel junction and an ohmic resistor.<sup>167</sup>

The equilibrium current through an SET can then be expressed using a steady state master equation.<sup>78</sup>

$$\frac{\partial P(N)}{\partial t} = \Gamma^{N,N+1}P(N+1) + \Gamma^{N,N-1}P(N-1) - (\Gamma^{N+1,N} + \Gamma^{N-1,N})P(N)$$
  
Equation 2.31

Here P(N) represents the occupancy probability when there are N excess electrons on the island,  $\Gamma^{N,N+1} = \Gamma_S^{N,N+1} + \Gamma_D^{N,N+1}$  represents the total tunneling rate for one electron to tunnel from the island to the drain and source leads when there are N + 1excess electrons on the island before the tunneling events. We adopt the convention such that  $\Gamma_S^{N,N+1}$  represents the tunneling rate for an electron tunneling from the island to the source and changes the number of excess electrons on the island from N + 1 to N. The stationary probability in equilibrium can be obtained by solving  $\partial P(N)/\partial t =$  $0,^{78}$ 

$$P(N)(\Gamma_{S}^{N+1,N} + \Gamma_{D}^{N+1,N}) = P(N+1)(\Gamma_{S}^{N,N+1} + \Gamma_{D}^{N,N+1})$$

Equation 2.32


Figure 2.14 Comparison of an experimentally measured charge stability diagram (a) and a simulated charge stability diagram (b).  $I_{DS}$  is plotted using absolute values for clarity. The measurement is taken on an STM-patterned, metallic SET (to be presented in Chapter 6) using a dilution refrigerator with a base temperature of ~10 mK. The electron temperature is approximately between ~200 mK to 1 K. The simulation treats the capacitance and junction resistance values as input parameters. The capacitance inputs are extracted from analyzing the average geometry of the measured Coulomb diamonds in (a):  $C_{\Sigma} = 13.5$  aF,  $C_{G} = 2.8$  aF,  $C_{D} = 5.6$  aF, and  $C_{S} = 5$  aF. The source and drain tunnel junction resistances are taken as  $R_{S} = 0.1$  M $\Omega$  and  $R_{D} = 0.1$  M $\Omega$ . Other input parameters are T = 1 K,  $Q_{0} = -0.1e$ , where *e* represents the elementary charge.

Since at a given bias, the two most-probable charge states dominate the SET island occupancy, following the discussions of Inokawa *et al.*,<sup>168</sup> we adopt a two-state approximation that P(N) + P(N + 1) = 1. This is a good approximation in the conductance regions when the thermal broadening  $k_BT$  is much smaller than the charging energy  $E_c$ .<sup>168</sup> (Note, the two-state model has also been shown to be applicable in the strong tunneling regime.<sup>169</sup>) Combining the equilibrium condition in Equation 2.31 and the two-state approximation, we obtain an analytical expression for the total tunneling current through a metallic SET,

$$I_{DS}(N) = -eP(N) \Gamma_D^{N+1,N} + eP(N+1)\Gamma_D^{N,N+1}$$
$$= e \frac{\Gamma_D^{N,N+1}\Gamma_S^{N+1,N} - \Gamma_D^{N+1,N}\Gamma_S^{N,N+1}}{\Gamma_D^{N+1,N} + \Gamma_S^{N+1,N} + \Gamma_D^{N,N+1} + \Gamma_S^{N,N+1}}$$

#### Equation 2.33

Here the first and second terms account for an electron tunneling from the source to the drain and vice versa. In simulating the charge stability diagram that includes a wide range of gate voltage, we assume  $I_{DS} = \sum_{N} I_{DS}(N)$ . A full charge stability diagram can be simulated taking  $C_S$ ,  $C_D$ ,  $C_G$ ,  $R_S$ ,  $R_D$ , T and  $Q_0$  as input parameters. In Figure 2.14, we present an experimentally measured charge stability diagram (a) and a simulated diagram (b). The simulation reproduces the main features of the measured charge stability diagram very well.

## 2.6.3 Co-tunneling

The simplest form of the orthodox model only includes the first-order perturbation term of the tunneling current that predicts the Coulomb blockade behavior. Higher-order perturbative terms lead to corrections to the Coulomb blockade conductance, especially when the tunnel resistance is no longer large compared with the resistance quantum.<sup>170</sup> In this regime, co-tunneling events dominate the conductance within Coulomb blockaded regions when the sequential tunneling of single electrons is suppressed.

In an SET, quantum mechanics allows the tunneling of electrons through both junctions in parallel. In the Coulomb-blockade regions, a tunneling event through either of the two junctions can be suppressed for two reasons: first, it increases the system's free energy; second, it is forbidden by energy conservation. However, the energy-time uncertainty relation allows a virtual electron in the forbidden state on the island within a corresponding time scale  $\hbar/E_c$ . In the meanwhile, another electron from the island can tunnel off to the other lead through the Heisenberg uncertainty relationship as well.

We call this an inelastic co-tunneling event because of the creation of an electron-hole excitation on the island after the co-tunneling event. If the same electron tunnels off the island from this virtual state, we call it an elastic co-tunneling event. In an elastic co-tunneling event, the coherence of the wavefunction becomes important when calculating the elastic co-tunneling rate. In an inelastic co-tunneling event, since it involves tunneling of two different electrons in two different junctions, coherence between the wavefunctions of the two electrons can be neglected when calculating the inelastic co-tunneling rate.

It has been shown that for metallic SETs whose electron density of states,  $1/\Delta E$ , at junction electrodes is high,  $\Delta E \ll E_C$  (single particle energy spacing smuch smaller than the charging energy  $E_C$ ), the elastic co-tunneling rate is smaller than the inelastic cotunneling rate by a factor of  $\Delta E/E_C$ .<sup>171</sup> Therefore, inelastic tunneling events dominate the co-tunneling process in a metallic SET. On the other hand, since external energy is required to allow an inelastic co-tunneling event to excite the dot into an excited state, a vanishing drain-source bias is energetically unfavorable for an inelastic co-tunneling process to occur.

#### **2.6.4 Electrical Transport through Quantum Dots**

If  $k_BT \leq \Delta E$ , the electrical transport in an SET is in a quantum dot regime where the discrete nature of single particle energy levels on the dot cannot be ignored. This allows the individual single particle levels on the dot to be resolved and identified in single electron tunneling spectroscopy. Detailed measurement of the tunneling spectroscopy features of few-donor and single-atom SETs is essential to understanding the impact of

device architectures on quantum dot confinement potentials and to predicting the behavior of donor-based qubits in quantum information applications.<sup>172, 173</sup> From the previous review on the tunneling rate formulation using Fermi's golden rule in the weak tunnel-coupling regime, the tunneling rate  $\Gamma_T$  (subscript T = S, D) between the metallic source/drain reservoirs and a single particle level  $\mu_N$  on the dot depends on both the wavefunction of the dot state and the DOS,  $\rho_T$ , of the source/drain reservoirs,

$$\Gamma_T = \frac{2\pi}{\hbar} \sum_g \mathcal{M}_T^2(\mu_N) \rho_T(\mu_N)$$

#### Equation 2.34

where  $\mu_N$  is the dot chemical potential when there are *N* excess electrons on the dot, *g* is the degeneracy number of the  $\mu_N$  level,  $\rho_T(\mu_N)$  is the source/drain DOS at the  $\mu_N$  level, and  $\mathcal{M}_T^2(\mu_N)$  is the averaged tunneling coefficient at the  $\mu_N$  level. Considering the Fermi Dirac distribution on the source/drain reservoir at  $\mu_N$ ,

$$f_T(\mu_N) = \frac{1}{e^{(\mu_N - \mu_T)/k_B T} + 1} = \frac{1}{e^{\Delta F_T^{N+1,N}/k_B T} + 1}$$

#### Equation 2.35

Here  $\mu_N = \mu_{IS}(N)$  and  $\Delta F_T^{N+1,N}$  are defined in the previous section using the constant interaction model and  $\mu_T$  (subscript T = S, D) represents the Fermi level in the source/drain reservoir. Following the derivations of Park,<sup>174</sup> the single electron tunneling rates can be expressed as,

$$\Gamma_{S}^{N+1,N} = f_{S}(\mu_{N})\Gamma_{S}$$
$$\Gamma_{S}^{N,N+1} = [1 - f_{S}(\mu_{N})]\Gamma_{S}$$
$$\Gamma_{D}^{N+1,N} = f_{D}(\mu_{N})\Gamma_{D}$$

$$\Gamma_D^{N,N+1} = [1 - f_D(\mu_N)]\Gamma_D$$

Equation 2.36

Treating  $\Gamma_S$  and  $\Gamma_D$  as constants in the linear response regime, the total single electron tunneling current through an SET is determined by solving the master equation from the previous section with the result,

$$I_{DS}(N) = e \frac{\Gamma_D^{N,N+1} \Gamma_S^{N+1,N} - \Gamma_D^{N+1,N} \Gamma_S^{N,N+1}}{\Gamma_D^{N+1,N} + \Gamma_S^{N+1,N} + \Gamma_D^{N,N+1} + \Gamma_S^{N,N+1}}$$
$$= e \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D} [f_S(\mu_N) - f_D(\mu_N)]$$

Equation 2.37

Taking a partial derivative of  $I_{DS}$  and converting the current signal into a differential conductance signal to improve the visibility of tunneling spectroscopy features, (and hence forth omitting  $\mu_N$  in  $f_T(\mu_N)$  for brevity)

$$\frac{\partial I_{DS}(N)}{\partial V_{DS}} = \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D} \frac{e^2}{k_B T} \left[ (1 - f_S) f_S \frac{C_D}{C_{\Sigma}} + (1 - f_D) f_D \frac{C_S + C_G}{C_{\Sigma}} \right]$$
  
Equation 2.38

at zero drain-source bias,  $f_S = f_D$ . Therefore, the Coulomb oscillation peaks in the differential conductance at zero drain-source bias can be simplified as,

$$\frac{\partial I_{DS}(N)}{\partial V_{DS}}\Big|_{V_{DS}=0} = \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D} \frac{e^2}{k_B T} \left[ (1 - f_S) f_S \right] = \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D} \frac{e^2}{4k_B T} \left[ \cosh(\frac{\mu_N}{2k_B T}) \right]^{-2}$$
$$= G_{max} \left[ \cosh(\frac{e\alpha_G (V_{GS}^* - V_{GS})}{2k_B T}) \right]^{-2}$$
$$V_{GS}^* = \frac{\left[ \left( N + \frac{1}{2} \right) e - Q_0 \right]}{C_G}$$

$$G_{max} = \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D} \frac{e^2}{4k_B T}$$

Equation 2.39

Here  $\alpha_G = C_G/C_{\Sigma}$  is the gate lever-arm,  $V_{GS}^*$  is the peak position on the gate voltage  $V_{GS}$  axis, and  $G_{max}$  is the peak amplitude. At low-temperatures (when  $k_BT \leq \Delta E$ ) and in the weak tunnel coupling regime, fitting the Coulomb oscillation peak shapes is a common practice to estimate the electron temperature. However, as the lifetime broadening due to strong tunnel coupling becomes comparable to the thermal broadening, the tunneling rate also starts to contribute to the peak shapes. In such cases, higher-order tunneling components must be included.<sup>171</sup>

# 2.7 Chapter Summary

In this chapter, we have reviewed the fundamentals of STM imaging and atom manipulation operations, single-crystal Si and Si (100) surfaces, chemical reactions of hydrogen and phosphine on Si (100) surfaces, and epitaxial overgrowth, all of which are necessary to understand the complete atomically precise fabrication scheme to be presented in Chapter 3. We have reviewed the basic theory of the perturbation approach to the tunneling rate in STM, and electrical transport in SETs in both the classical and quantum dot regimes.

# **Chapter 3: A Complete Atomically Precise Fabrication Scheme**

# **3.1 Introduction**

Following the first demonstration by Lyding, Shen, Tucker, et al.<sup>49</sup> at the University of Illinois of H lithography using an STM, Shen *et al.*<sup>48</sup> outlined the concept of making devices using dopants whose positions were determined by a STM-lithography based fabrication scheme. In the following 10 years, Michelle Simmons and her team at the University of New South Wales (UNSW) realized the fabrication of atomically precise Si:P devices and were the first to demonstrate a complete fabrication scheme.<sup>55 56, 57</sup> Since then, the UNSW team has made great progress, including a demonstration of the world's first atomically-precise single-atom transistor<sup>59</sup> and high-fidelity electron spin read-out of precision placed single donors in silicon.44, 63, 64 As a result of their groundbreaking work, atomically precise Si:P systems have been recognized as one of the most promising candidates for making a scalable solid-state quantum computer. In this chapter, based on the initial fabrication scheme laid out by UNSW, we describe the implementation of a complete atomically precise fabrication scheme developed in our lab during this thesis work, with an emphasis on the technological advances that have led to the successful fabrication of state of the art atomically-precise Si:P quantum devices in our lab. We describe in detail the process development and optimization in our group to improve the quality and fidelity of atomically precise fabrication.



Figure 3.1 Schematic overview of a complete fabrication scheme for STM-patterned devices and blanket doped delta-layer devices. See text for details.

# **3.2 Fabrication Process Overview**

The schematics in Figure 3.1 summarizes the fabrication flow and specific steps of the two types of Si:P devices that are presented in this thesis:  $\delta$ -doped Si:P monolayer devices and STM-patterned Si:P devices. Fabricating an STM-patterned device starts

with creating registration markers on a 2.5 mm  $\times 10$  mm  $\times 0.3$  mm Si (100) substrate to enable device re-location and for contact alignment purposes. Fabricating  $\delta$ -doped Si:P monolayer device starts with a blank Si substrate. We first chemically clean a substrate and load it into an ultrahigh vacuum (UHV) system. Subsequently, we thermally degas and flash anneal the substrates at high temperatures in the UHV system to generate a clean Si (100) surface with a  $2 \times 1$  surface reconstruction. For STM-patterned devices, we introduce a monolayer of hydrogen atoms onto the surface and create a chemically inert resist layer. Next, an STM tip is used to define a device structure with atomic precision in the hydrogen resist by selectively removing hydrogen atoms from the surface to expose chemically-reactive Si dangling bonds. The substrate is then dosed with PH<sub>3</sub> gas at room temperature, where the PH<sub>3</sub> molecules adsorb only onto patterned regions. In contrast, when fabricating a  $\delta$ -layer device, the clean Si (100) surface is uniformly dosed with PH<sub>3</sub> gas after the high-temperature flash anneal. After PH<sub>3</sub> dosing, a short thermal-anneal allows the adsorbed P to substitutionally replace Si atoms from the first layer of the substrate, so that P atoms are incorporated into the Si lattice. Subsequent low-temperature epitaxial overgrowth encapsulates the P atoms in a crystalline Si environment, after which the sample can be taken out of the UHV system. For STM-patterned devices, we obtain device coordinates relative to etched registration markers with a combination of optical microscopy and surface potential mapping. We then deposit e-beam-defined contact metal over the top of STM-patterned contact pads and anneal to form silicide contacts to the buried device. In contrast, for blanket delta-layer devices, the active area of the device is created in a lithographicallydefined etching step which removes P from outside the device area, followed by metal deposition and electrical contact formation.

From the perspective of process development and characterization, in the following sections we will discuss each of the key fabrication steps in detail.

# **3.3 Ultrahigh Vacuum Environment**

A good ultrahigh vacuum (UHV) environment, having a base pressure on the order of  $10^{-11}$  Torr or below, is essential for successful atomically precise fabrication. It not only allows generation of ultra-clean samples that remain uncontaminated during a long device fabrication process [~ (12 to 24) hours for hydrogen lithography and ~5 hours for encapsulation overgrowth] but is also a vital prerequisite to obtaining a stable STM tip for atomically resolved hydrogen depassivation lithography. A single contaminant defect in proximity to a donor or within a tunnel gap can be detrimental to device performance or even cause total failure of the device. According to the Hertz-Knudsen formula,<sup>175</sup> the impinging flux F (in units of  $m^2s^{-1}$ ) onto a flat sample surface can be expressed as  $F = 0.01P/\sqrt{2\pi m k_B T}$ , where P is the partial pressure in the unit of mbar and m is the particle mass in the unit of kg. Assuming the residual gas to be  $N_2$  and a clean Si (100) surface, one can estimate that for a partial pressure of  $10^{-6}$  Torr. 1 monolayer (ML) of residual gas particles impinge onto the Si (100) surface over a period of 1 second. The typical base pressure in our UHV systems (both the STM chamber and the overgrowth chamber) is  $\sim 3 \times 10^{-11}$  Torr. This corresponds roughly to a 10-hour period for 1 ML of residual gas particles to impinge the surface. For a typical epitaxial growth rate of 0.01 ML/second, a base pressure of  $\sim 3 \times 10^{-11}$  Torr corresponds to one impinging residual gas particle per 300 adatoms of Si. The probability that an impinging particle adsorbs onto the surface is determined by the sticking coefficient of the impinging particle. The dominant residue gas species in a stainless steel UHV system is H<sub>2</sub>, which has an extremely low dissociative adsorption sticking coefficient on clean Si (100) surfaces, on the order of  $10^{-9}$  at room temperature ( $\sim 300$  K). <sup>176</sup> This means a  $\sim 3 \times 10^{-11}$  Torr base pressure shall be able to maintain sufficiently clean device lithography patterns as well as overgrowth layers with respect to H<sub>2</sub>. H<sub>2</sub>O is another common residual gas species in UHV systems that has a sticking coefficient on Si (100) surfaces on the order of  $10^{-5}$  at room temperature.<sup>177</sup> We routinely bake our UHV systems to above 150 °C to eliminate residual H<sub>2</sub>O in the systems.



Figure 3.2 Schematics of the registration marker design. (a) The shallow-etched and deep-etched markers are in blue and red colors respectively. SEM images of the overlay target design and the inner shallow-etched marks are also shown. (b) Optical images of STM-tip navigation on a sample surface using the registration markers. The tip apex location on the sample surface is along the axis of the tip and its mirror reflection on the surface. The intersection of two axes that are viewed from two different angles determines the actual tip location on the sample surface.

# **3.4 Registration Markers Design and Fabrication**

Throughout device fabrication, relocating STM-patterned devices is required for both *in-situ* device characterization using STM and *ex-situ* alignment of ohmic electrical contacts to the buried device. The limited scan range and scan speed of an STM present a significant challenge to relocating STM-patterned features using an STM after the sample has been removed from the STM stage for other fabrication processes. The lack of an optical or topographical signature from the buried devices. In a project led by Dr. Pradeep Namboodiri in our group, we have developed a two-layer etched registration marker strategy that has enabled efficient in-situ device re-location using an STM as well as sub-50 nm contact alignment accuracy using an e-beam aligner.<sup>178, 179</sup> Because neither metal deposition nor ion-implantation are involved in the registration process, the pre-etched registration markers are fully compatible with subsequent sample chemical cleaning and thermal flash anneal processes.

Figure 3.2 (a) shows the overall registration marker design. The first layer of etched registration markers is shallow-etched for *in-situ* STM positioning and device re-location. The shallow etch depth is typically 50 nm, a value that follows from a previous study from our group which attempted to engineer Si (100) morphology that is suitable for STM-based fabrication.<sup>180</sup> The STM registration markers consist of multiple sets of 50  $\mu$ m  $\times$  50  $\mu$ m grids. We use a long working distance optical microscope to guide the STM tip to specific squares for device fabrication and relocation, as shown in Figure 3.2 (b). By utilizing the mirror reflection of an STM tip on the substrate surface and by comparing different viewing angles, we improve the typical *in situ* re-location accuracy to within approximately  $\pm 5 \,\mu\text{m}$ . The second layer of etched registration marks is deep-etched for e-beam alignment of ohmic contacts. This deep-etch depth is typically 2  $\mu$ m, which minimizes the effects from thermal deformation during the high-temperature flash anneal process. The deep-etched marks consist of one set of global alignment marks at the two ends of a chip and sets of local alignment marks close to the device fabrication regions.

These two-level registration markers are patterned at the wafer-scale using an ASML optical stepper. The measured overlay accuracy between the two registration marker layers across a 4-inch wafer is within ~10 nm. The shallow-etched registration marks are etched using reactive ion etching (RIE) with a  $CF_4$ - $SF_6$  etchant. The deepetched registration marks are etched using a Bosch etch process.<sup>181</sup> After two-level etching, the wafer is diced into Si chips that fit onto the STM sample holders.

## **3.5 Preparation of Clean Si (100) Surfaces**

The STM patterned Si:P device fabrication starts with a Si (100) substrate of dimensions 10 mm  $\times$  2.5 mm  $\times$  0.3 mm that can be mounted into a standard Omicron VT-STM direct current heating sample holder. Before loading into the UHV system, the sample goes through a thorough wet-chemical cleaning procedure to remove organic and inorganic residues on the substrate surfaces. The sample is first sonicated in PG remover and subsequently isopropanol to remove residual photoresist. After a sonicating rinse in deionized water (DI water,  $18.2 \text{ M}\Omega \cdot \text{cm}$  resistivity), the sample is submerged in a Piranha solution (3  $H_2SO_4$ : 1  $H_2O_2$ ) for 10 minutes targeting organic residue as well as trace metals, metal oxides, and carbonates. After another sonicating rinse in DI water, the sample is submerged in a 2% HF solution for 1 min to remove the silicon oxide that forms during Piranha cleaning. This is followed by another sonicating rinse in DI water. The sample is then cleaned in a standard cleaning 1 (SC-1) solution (1:1:5 solution of NH<sub>4</sub>OH (ammonium hydroxide) +  $H_2O_2$  (hydrogen peroxide) +  $H_2O$  (DI water)) at (75 to 80) °C for 10 minutes. The sample goes through another DI water sonicating rinse, 2% HF dip, and DI water sonicating rinse. Subsequently, the sample is cleaned in a SC-2 solution [1:1:5 solution of HCl (hydrochloric acid) +  $H_2O_2$  (hydrogen peroxide) +  $H_2O$  (DI water)] at (75 to 80) °C for 10 minutes. SC-1 and SC-2 cleaning recipes are widely used Si cleaning procedures which remove metallic and ionic contaminants from Si. Finally, the sample goes through a final DI water sonicating rinse before being blown dry with high-purity nitrogen gas. After the chemical cleaning procedures, we examine and record the sample surface images using a Nikon Eclipse optical microscope in both bright field and dark field imaging modes to ensure no dust particles are present on the sample surface before loading the sample into the UHV system.

After loading the sample into the UHV system, we degas the sample holder and sample overnight on a standard Omicron sample manipulator by passing 1.2 A through a pyrolytic boron nitride (PBN) back-heater and heating the substrate to  $\sim$ 580 °C using direct current resistive heating. This degassing procedure serves to desorb residual water vapor and atmosphere gas residue on the sample holder and substrate.

After degassing, we flash-anneal the sample to 1200 °C using direct current heating. This radical thermal process sublimates surface layers of silicon atoms as well as any residual contaminants at the atomic scale, which is critical for obtaining ultraclean and defect-free Si (100) 2×1 reconstructed surfaces. A cooling shroud filled with liquid nitrogen is used to maintain the vacuum pressure (typically below  $2 \times 10^{-10}$  Torr) during the flash anneal. Because the flash anneal process induces morphology evolution of the pre-etched fiducial marks,<sup>178</sup> we restrict the 1200 °C flash anneal process to less than 1 min to minimize its impact on contact alignment accuracy. After flash annealing, we quench the substrate temperature quickly through the temperature zone<sup>182</sup> of surface roughening down to ~800 °C, and then slowly cool down the substrate at a rate of ~2 °C/sec to ~300 °C for subsequent hydrogen passivation or to room temperature for obtaining a bare Si (100) surface. The quick temperature quench step avoids surface roughing while the slow cool-down process eliminates vacancy defects on the final Si (100) 2×1 reconstructed surface.<sup>182</sup>



Figure 3.3 STM In-situ characterization of hydrogen-terminated (H:Si) surfaces on a degenerately boron-doped p-type Si (100) substrate. (a) filled state image at -2.0 V, 0.18 nA. (b) empty state image at +2.0 V, 0.18 nA. The bright dots are single Si dangling bonds which indicate missing hydrogen atoms. The atomic-scale features on the H:Si surface, such as dihydrides, vacancies, and single dangling bonds appear differently under different imaging conditions. (c) Hydrogen depassivation lithography is used to remove the hydrogen-resist in the left part of the image. The depassivated regions appear to be bright in the STM images due to the relatively high local density of states in the exposed dangling bond regions. Inset: Low-energy electron diffraction (LEED) pattern on a Si (100) surface after flash anneal at 1200 °C, showing a square lattice surface reconstruction with a  $2 \times 1$  periodicity. <sup>183</sup> (d) The normalized differential conductance spectra (dn spectra) measured on a clean Si (100) surface and hydrogen-

terminated Si (100) surface. Hydrogen termination removed dangling bond states from the substrate band gap, resulting in a wider surface band gap.

# **3.6 Hydrogen Resist Formation on Si (100) Surfaces**

After creating a clean Si (100) 2×1 reconstructed surface, whether for STM investigation of bare Si (100) surfaces or blanket  $\delta$ -layer fabrication, the sample is transferred directly to the STM chamber for STM characterization or phosphine dosing. In cases of fabricating STM-patterned devices, we carry out hydrogen termination by exposing the clean Si (100) surface to an atomic hydrogen flux at elevated substrate temperature. First, the substrate temperature is stabilized at ~300 °C by direct current heating on a thermal manipulation stage. We use a hot tungsten filament as a hydrogen "cracker," which is direct-current heated to approximately  $\sim 1800$  °C to  $\sim 2000$  °C, to "crack" hydrogen molecules into atomic hydrogen. The tungsten filament is degassed before the sample is flash annealed to suppress any rise in chamber pressure when turning on the cracker after the clean surface is prepared. Before introducing ultrahigh purity hydrogen gas (>99.9999%) into the preparation chamber, we throttle the ion pump to prevent overloading it during the hydrogen dosing. We then introduce molecular hydrogen gas into the preparation chamber through a sapphire UHV leak valve until the chamber pressure stabilizes at  $\sim 2 \times 10^{-6}$  Torr. We then turn the substrate to face the hydrogen cracker that is approximately 3 cm away from the sample. Because of radiative heating from the tungsten filament, we estimate the actual substrate temperature during this hydrogen termination process to be  $\sim$ 350 °C. To obtain high-quality monohydride [Si (100)  $2 \times 1$ :H] surfaces, it is important to maintain the substrate temperature above ~350 °C where the monohydride (Si (100)  $2\times1:H$ ) phase becomes energetically favorable over dihydride [Si (100)  $1\times1:H$ ] and intermediate H ( $3\times1$ ) phases. The surface temperature must also stay below ~450 °C where hydrogen dissociation from a monohydride phase starts to occur.<sup>184</sup> After exposing the heated surface to atomic hydrogen for about 8 minutes, we finish the hydrogen-termination process by sequentially turning off the W-filament current, closing the hydrogen gas leak valve, opening the ion pump valve, and finally cooling the sample to room temperature. It is important to turn off the hydrogen cracker and pump out hydrogen before cooling down the sample to room temperature. Otherwise, atomic hydrogen etching of the Si (100) surface can occur when the sample cools to room temperature, generating a rough Si surface on the atomic scale that is not suitable for atomic device patterning.<sup>185</sup> Figure 3.3 shows examples of *in-situ* characterization of the high-quality hydrogen-terminated Si (100)  $2\times1$  surfaces that are prepared in this study.



Figure 3.4 Characterization of an STM-tip that is prepared using poly-crystal tungsten. Scanning electron microscopy (SEM) images (a), (b) and a transmission electron microscopy (TEM) image (c) of the tip. The facets of the tungsten crystal after etching

are clearly visible in (a) and (b). The high resolution TEM image in (c) shows the tip apex is free from tungsten oxide or major contaminants.

# **3.7 STM Tip Preparation**

A clean, mechanically stable, and atomically sharp tip is highly desirable for atomicscale imaging and manipulation using STM (see Figure 3.4). Despite an STM tip's capability to probe the atomic world and decades of effort expended in studying STM tips, STM tip fabrication remains both an art and a science, and still requires faith as much as skill in preparing STM tips for atomically precise fabrication. Controlling the tip profile using electrochemical etching has been extensively studied.<sup>186, 187</sup> Primarily, we prepare STM tips by electrochemically etching a polycrystalline tungsten wire. The end of the tungsten wire is partially submerged (~2 mm) in a 1 Mol/L solution of KOH while a DC voltage (typically 3 V to 5 V) is applied using a Unisoku tip preparation station. The voltage is rapidly turned off when a current drop (due to the removal of the end of the tip) is detected, with the typical cut-off current being 0.1 mA. The tip and tip-holder are then loaded into the UHV system and thoroughly degassed in-situ by annealing to approximately 500 °C for one or two days using a PBN radiative heater. Sufficiently outgassing the tip before use helps to minimize the contaminants that can desorb or migrate from the tip to sample surfaces during STM imaging and lithography.

We emphasize that obtaining an atomically sharp and contaminant free tip only accounts for half of the hydrogen lithography equation. An ultra-clean vacuum environment accounts for the other half of the equation. Both surface and vacuum cleanliness contribute to stability during imaging and hydrogen lithography operations.



Figure 3.5 Atomically resolved STM images (-2 V sample bias, 0.1 nA setpoint current) of STM-patterned device geometries with atomic-precision. The images are taken after STM lithography but before PH<sub>3</sub> dosing. We use the Si (100) 2x1 dimer reconstruction lattice as a natural atomic ruler and attempt to align critical device dimensions with the underlying dimer rows. (a) An atomically abrupt island with source and drain leads. (b) An atomically precise quantum dot with source and drain leads. (c) Atomically precise double quantum dots. (d) An atomically precise  $3 \times 3$  quantum dot array.

## **3.8 Hydrogen Lithography Using an STM**

The monohydride passivation on the Si (100) 2×1 surface serves as a chemically inert and atomically thin resist layer for subsequent atomic-scale device lithography procedures. Using an STM tip, we desorb hydrogen resist atoms, which exposes chemically reactive Si dangling bonds, within pre-designed regions of device components. This process is called hydrogen lithography. Exclusively in this thesis work, a negative bias is applied to the STM tip during lithography. We choose between the tunneling and field emission lithography modes depending on the sizes of device components and the tolerance of patterning precision. Despite varying requirements for lithography precision, we emphasize that all lithography patterns must be *completely depassivated* and *contamination-free* for successful atomic device fabrication.

We use tunneling mode lithography to pattern device components on the sub-10 nm scale that require atomic-scale precision. Typical parameter ranges for tunneling mode lithography are [-5 V, -3 V] for the tip bias and [15 nA, 55 nA] for the tunneling current set-point. Because of the small tip-sample separation during tunneling mode lithography, the tunneling electron beam is spatially focused under the atomic-scale tip apex. This allows the creation of lithographic patterns with atomic-scale precision and atomically abrupt edges, and even deterministic desorption of single H atoms. However, because the H desorption yield per electron in tunneling mode is quite low,<sup>48</sup> lithography speed (hydrogen desorption area per unit time) is also low. For complete H-desorption in tunneling mode, the scan velocity is typically 100 nm/sec and the scanline spacing is typically 0.5 nm/line. We use field-emission mode lithography to pattern micrometer-scale device components, such as van der Pauw (VDP) squares and contact pads. The typical parameter ranges for field-emission mode lithography are [-8 V, -6 V] for the tip bias and [0.2 nA, 3 nA] for the field-emission current set-point. Because of the relatively large tip-sample separation in field-emission mode, the field-emission electron beam is less confined, and the lithography loses its atomic precision due to spurious hydrogen desorption at pattern edges.<sup>188</sup> However, in field emission mode, highly efficient hydrogen desorption can be achieved. For complete H-desorption in field-emission mode, the scan velocity is typically 500 nm/sec and the scan-line spacing is typically 2 nm/line.

We point out that the actual hydrogen-desorption capability using pre-defined lithography parameters is highly tip-dependent. The set of optimal lithography parameters must be calibrated for each tip and must be recalibrated as tip condition evolves over time. Figure 3.5 shows atomically resolved STM images of a typical set of hydrogen lithography patterns with atomic precision. We also use the Si (100)  $2\times1$ surface reconstruction lattice as a natural atomic ruler to measure the pattern geometries with atomic precision.



Figure 3.6 *In-situ* characterization of phosphine (PH<sub>3</sub>) dosing and phosphorus (P) incorporation in Si (100) surfaces using STM and Auger electron spectroscopy (AES). STM images of the Si surface after saturation dosing with PH<sub>3</sub> at room temperature (a) and after thermal incorporation anneals at ~380 °C for 2 minutes (b). (c) (d) Auger measurement in studying thermally induced P incorporation and desorption on Si (100) surfaces. (c) Comparison of the Auger spectra on a clean Si (100) surface before and after PH<sub>3</sub> saturation dose and incorporation anneal at 380 °C for 2 minutes. (d) Comparison of the Auger spectra on a P-incorporated Si (100) surface with sequential direct-current anneals at 400 °C, 600 °C, 700 °C, and 800 °C for 1 minute at each temperature.

# **3.9 Dosing and Incorporation**

After STM lithography, the sample is dosed with phosphine gas (PH<sub>3</sub>)  $3 \times 10^{-8}$  Torr for 3 minutes at room temperature. PH<sub>3</sub> selectively adsorbs into depassivated regions where chemically reactive Si dangling bonds are exposed. The remaining hydrogen resist layer prevents the rest of the surface area from being doped.

The PH<sub>3</sub> dosing is followed by thermal annealing at  $\sim$ 380 °C for 2 minutes to allow phosphorus atoms to incorporate into the top layer of Si atoms. Figure 3.6 (a) (b) show STM images on a clean Si (100) surface after PH<sub>3</sub> dosing and after P incorporation anneal. Each incorporated phosphorus atom substitutes an underlying Si atom and forms three covalent bonds with the Si substrate, resulting in a P-Si heterodimer on the 2×1 reconstructed surface.<sup>54</sup> The covalent bonds bind the P atom strongly within the Si lattice and help to reduce P diffusion and segregation during the subsequent encapsulation overgrowth. Also, the thermal incorporation anneal has been found to improve P electrical activation ratio after encapsulation overgrowth.<sup>189</sup> After the incorporation anneal, device regions are partially H-terminated due to the residual H atoms from PH<sub>3</sub> dissociation; and the substituted Si atoms are ejected onto the surface and form single Si atom islands or short Si chains. It has been shown by the UNSW team that the ejected Si atoms can be reliably utilized to verify successful P incorporation.<sup>59</sup>

### 3.9.1 Auger Characterization of P Incorporated Si (100) Surfaces

In addition to STM, we use Auger electron spectroscopy (AES) for *in-situ* characterization of PH<sub>3</sub> dosing and P incorporation. AES is a standard surface analysis method used to determine the elemental composition of the top few atomic layers of a surface in a UHV environment.<sup>190</sup> This technique is based on the detection and analysis of the energy distribution N(E) of Auger electrons which are emitted in the relaxation of an excited ion with an inner shell vacancy (Auger process). The surface layer atoms are excited by a focused low-energy (typically 1.5 keV to 3 keV) incident electron beam. Because of the relatively low intensity of the Auger peaks over the background of secondary or inelastically backscattered electrons, first-order differentiation of N(E) is commonly used to present the measured spectrum. The primary characteristic peak positions for Si and P elements in an Auger spectrum are ~92 eV and ~121 eV respectively. [See Figure 3.6 (c) & (d)] Quantification of the measured element's surface concentration is achieved by comparing the relative intensity of Auger peaks.

Previous thermal desorption spectroscopy (TDS) studies using XPS <sup>52, 191</sup> and Auger techniques<sup>192</sup> have shown that thermal desorption of the incorporated P atoms does not occur below 600 °C. Figure 3.6 (c) shows the measured Auger spectrum on a clean Si (100) surface before and after P-incorporation, where the characteristic P Auger peak shows up after a P incorporation anneal while the amplitude of the Si peak decreases. As shown in Figure 3.6 (d), the P Auger peak remains essentially unchanged during short thermal anneals up to 700 °C for 1 min and disappears upon raising the anneal temperature to 800 °C. This is in good agreement with previous reports in the literature that show a substantial drop in surface P concentration is observed at 750 °C.<sup>191</sup>



Figure 3.7 *Ex-situ* characterization of Si:P  $\delta$ -layers using secondary ion mass spectrometry (SIMS), transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS). (a) SIMS measurement of P depth concentration profiles on  $\delta$ -layer samples with different doping density. The measured concentration peaks are positioned at zero on the x-axis. The doping density is varied by adjusting the PH<sub>3</sub>

exposure of the dosing process. (b) Aberration-corrected (AC) high-resolution highangle-annular-dark-field (HAADF) scanning transmission electron microscopy (STEM) image of a saturation doped Si:P  $\delta$ -layer sample, showing high epitaxial quality at the  $\delta$ -interface and in the encapsulation layer. (c) Cross-sectional EDS concentration maps of C, P, Si, and O of a saturation doped Si:P  $\delta$ -layer sample, showing no detectable C and O concentrations at the  $\delta$ -doped P interface. The TEM sample is prepared using a standard focused ion beam (FIB) lift out technique. The sample is capped with Pt over the targeted area prior to FIB milling.

## **3.9.2 SIMS Characterization of Dopant Concentration Profiles**

We use secondary ion mass spectrometry (SIMS) as a primary tool to characterize the dopant concentration profile in the overgrowth direction. SIMS analyzes the composition of thin films by sputtering the surface with a focused primary ion beam. A percentage of the sputtered surface species (monoatomic and polyatomic particles) are ionized and then accelerated, collected, and analyzed using a mass spectrometer. The elemental, isotopic, or molecular composition is determined by measuring the mass/charge ratio of the collected secondary ions. The primary advantage of SIMS is its high sensitivity down to part per billion levels. This allows depth profiling of low concentration species as well as high depth resolution using low primary beam energies and slow sputtering rates. The major disadvantage of SIMS is that it is destructive and requires the target structures to be larger than a few micrometers. Because of this limited lateral resolution, we typically use blanket  $\delta$ -doped Si:P layers to characterize the dopant distribution in the overgrowth direction. Cs<sup>+</sup> and O<sup>+</sup><sub>2</sub> are the most common

primary ion beam species used in SIMS measurements. For targeting different elemental species, the ion yield, which is the percentage of the sputtered atoms that become ionized, is primarily determined by the ionization potential for positive ions and the electron affinity for negative ions. Oxygen bombardment enhances positive ion yields and cesium bombardment enhances negative ion yields. Therefore, we use a  $Cs^+$  primary beam to analyze phosphorus and use  $O_2^+$  to analyze elemental boron in our samples.

In quantitative analysis of a SIMS measurement, the element composing the substrate (the matrix element) is typically used as the reference element. The target element is commonly known as the analyte element. There is the following expression:

$$\frac{I_R}{C_R} = RSF_E \frac{I_E}{C_E}$$

#### Equation 3.1

where  $I_R$  ( $I_E$ ) is the measured secondary ion counting rate for the reference (analyte) element.  $C_R$  ( $C_E$ ) is the concentration of the reference (analyte) element.  $RSF_E$  is the relative sensitivity factor for the analyte element. In trace element analysis, the reference element concentration can be assumed as a constant. Taking  $RSF = C_R \cdot RSF_E$ , we have

$$C_E = RSF \frac{I_E}{I_R}$$

#### Equation 3.2

The *RSF* values are calibrated using standard materials that are prepared by ion implantation.<sup>193</sup> For depth concentration profiling, the  $I_E/I_R$  is monitored as a function of time and the time-axis is converted to the depth-axis using the sputtering rate, which

is obtained by measuring the depth of sputter craters. For accurate depth profiling measurement, the focused primary ion beam sputters the sample in a raster manner over a square area. Sputtering edge effects are avoided by only analyzing secondary ion and crater depth data from the flat region in the center of the sputtered area. In this thesis, the measurement and analysis of the depth concentration profiles of P donors were carried out in collaboration with Dr. Steve Smith from EAG laboratory. Combining the superb sensitivity of SIMS with the monoatomic layer control of epitaxial overgrowth thickness, we will present how to quantify dopant movement at the atomic scale in Si:P monolayers in Chapter 5.

# **3.10 Silicon Encapsulation Overgrowth**

After dopant incorporation, epitaxial encapsulation overgrowth is required to embed the dopant atoms into a 3-D crystalline Si lattice environment. This encapsulation overgrowth serves two purposes: 1) It electrically activates the dopant atoms. 2) It isolates the device from defects at the sample surface. Previous studies have shown that the epitaxial encapsulation must exceed ~8 nm to protect the device from the influence of surface states.<sup>194</sup> <sup>195</sup> Great care must be taken to suppress dopant movement during the epitaxial overgrowth while maintaining good epitaxy quality.<sup>196, 197, 198</sup>



Figure 3.8 Si sublimation source (SUSI) and epitaxial growth rate calibration. (a) The Si arch filament inside a SUSI where the water-cooling shroud, Ta shutter, and Si shields have been removed. (b) Calibrated growth rates as a function of the direct current that passes through a Si arch filament. The reference growth rate is measured as a function of current through a new filament at a substrate distance of 10 cm. (c) and (d) show two examples of STM images on the Si (100) surfaces after submonolayer Si overgrowth at ~250 °C. The surfaces are H-terminated at the same temperature following overgrowth to improve imaging quality. Overgrowth island coverages are (c) ~33% and (d) ~93% of a monolayer.

### **3.10.1 Silicon Sublimation Source and Growth Rate Calibration**

Silicon overgrowth is performed using a Silicon sublimation source (SUSI), which is particularly suitable for ultrahigh purity and low growth rate applications. A SUSI assembly consists of an intrinsic Si sublimation filament, a degenerately doped Si preheating plate, an intrinsic Si shield, an integrated tantalum shutter, and a watercooled cooling shroud. [see Figure 3.8 (a)] The intrinsic Si shield blocks any line-ofsight paths from the SUSI. Sublimation happens within a range of temperatures and pressures over which solid and gaseous phases coexist. The sublimation rate, and therefore the growth rate, follows an approximately exponential dependence on the current that passes through the Si arch filament. This exponential dependence originates from the *Clausius-Clapeyron* equation<sup>199</sup> that describes the approximate relation between the vapor pressure and filament temperature. We calibrate the growth rate at different filament currents primarily by measuring a film thickness at the step edge of a shadow mask using a WYCO NT2000 vertical scanning and phase-shifting interference microscope.<sup>200</sup> SIMS, TEM, and STM imaging of sub-monolayer overgrowth have also been used for cross-calibrating the growth rate. See Figure 3.8 (b). Over the lifetime of a SUSI filament, filament consumption can induce slow drift in the deposition rate. We monitor the deposition rate after each overgrowth and adjust the input current to maintain the desired deposition rate.

Before turning on the SUSI source, we resistively heat the sample and use an infrared pyrometer to stabilize the sample temperature at 250 °C. Then the SUSI current is slowly turned on (at  $\sim$ 10 A/min) to reach the desired deposition rate. Because the hot SUSI filament will interfere with the pyrometer, the sample temperature can no longer be measured directly. At this stage, we closely monitor the sample resistance which

reflects the sample temperature due to the monotonic resistance-temperature relationship within the temperature range of our overgrowth process.<sup>201</sup> Because the hot filament will heat the sample slightly once the sample is facing it, we maintain a constant sample temperature during the Si overgrowth by monitoring the sample resistance.

### **3.10.2 Impact of Hydrogen Resist on Epitaxial Overgrowth**

Because the hydrogen atoms reduce Si adatom's diffusivity on the surface during the low-temperature epitaxial overgrowth, residual hydrogen is less desirable from the perspective of optimizing epitaxy quality. We found that, on a bare Si (100) surface, the growth front approaches a constant roughness during overgrowth.<sup>202</sup> In contrast, on an H-terminated surface, H atoms segregate with the growth front and lead to increased growth front roughness during overgrowth.<sup>202</sup> On the other hand, it is advantageous to preserve the hydrogen resist during the dopant incorporation anneal before overgrowth; the chemical bonding of hydrogen resist helps prevent lateral diffusion of the incorporated P atoms and maintains device integrity at the atomic scale. In this thesis, we limit the incorporation anneal temperature to below the thermal desorption temperature of the hydrogen resist (~450 °C).



Figure 3.9 Flow chart summarizing the temperature profiles and time scales of *in-situ* Si:P device fabrication steps. In fabricating a blanket-doped delta-layer device, the sample surface is doped with  $PH_3$  directly after the 1200 °C flash anneal. Fabricating a STM-patterned device involves STM-lithography and STM-imaging steps that are the most time-consuming steps throughout the entire fabrication scheme.

# 3.11 Transition from $\delta$ -doped to STM-patterned Si:P Devices

Blanket-doped Si:P monolayers are often used as a template to develop and optimize the doping and overgrowth processes for STM-patterned Si:P devices. This is because a blanket-doped layer provides easy access to material characterization techniques, such as SIMS and TEM. Several new atomically-precise fabrication techniques, such as phosphorus incorporation anneals<sup>151, 189</sup> and locking layer overgrowth,<sup>198</sup> were developed using large-area Si:P delta-layers and have now become common practice in atomic-precision device fabrication. In addition, fine-tuning of system-specific process parameters for doping density,<sup>192</sup> overgrowth temperature,<sup>146, 197</sup> overgrowth rate,<sup>203</sup> and growth front roughness<sup>145, 146</sup> is commonly performed using delta-doped layers. The low thermal budget parameter space explored in these studies is required to

be compatible with the atomically-precise fabrication. However, one key difference between the fabrication of blanket  $\delta$ -layers and STM-patterned devices is the inclusion of STM patterning steps over the critical Si:P device regions and the presence of a hydrogen resist layer outside of the device regions. The immediate transferability of fabrication parameters that are optimized from  $\delta$ -layers to STM-patterned devices has not been well understood historically. As illustrated in Figure 3.9, STM lithography is the most time-consuming step throughout the entire fabrication scheme, typically ranging from  $\sim 12$  hours to  $\sim 24$  hours per device, depending on the pattern complexity. Tip-surface interactions and exposure time during STM lithography and imaging can affect Si:P device quality, for example, by influencing epitaxial overgrowth quality. In this section, we use STM-patterned van der Pauw (VDP) structures as a test device to investigate the impact of STM-patterning conditions on the quality of STM-patterned Si:P devices (see Figure 3.10). After device encapsulation overgrowth, we use STM to re-locate the device and characterize the overgrowth quality directly on top of the buried device. To preserve the surface cleanliness for detailed atomic scale characterization as well as to eliminate the effects from surface states on STS measurements, we hydrogen-terminate the surface after overgrowth. The topographical roughness contrast is typically weak between the overgrowth inside and outside of the device regions.



Figure 3.10 Fabrication of STM-patterned van der Pauw (VDP) devices. (a) STM image of a 5  $\mu$ m × 5  $\mu$ m VDP device pattern after hydrogen lithography. (b) STM topographic image (+2 V sample bias, 0.1 nA set-point current) of the VDP device after encapsulation overgrowth and a subsequent hydrogen termination of the overgrown surface. Topographic features are barely detectable. (c) differential conductance (dI/dV) image acquired simultaneously with (b). The spectroscopic signature of the buried VDP device is visible. (d) Optical image of the VDP device after electrical contacts have been made. A successful STM-patterned device is optically invisible. (e) Schematic that overlays the contact design and the buried VDP device.



Figure 3.11 Impact of STM-lithography conditions on the quality of STM-patterned van der Pauw (VDP) devices. (a)-(d) Optical and peak-force Kelvin force microscopy (PFKFM) characterization of two distinct VDP devices, VDP-1 and VDP-2, after

encapsulation overgrowth. VDP-1 is optically invisible, and VDP-2 is optically visible in both bright-field (a) and dark-field (b) optical microscopy images. (c) both VDP-1 and VDP-2 show strong electrical signatures in PFKFM measurement, which are utilized for contact alignment relative to etched registration marks. (d) Bright-field optical image after electrically contacting the two VDP devices. The sheet resistance values are measured at T = 4 K. (e)-(h) STM images and cross-sectional TEM images of VDP-1 and VDP-2 after encapsulation overgrowth. The STM images are taken at the VDP device boarders. The low growth temperature results in 3-D island growth mode, where epitaxial nature of the overgrowth can be determined by whether the 3-D island orientations are in alignment with orientation of the crystalline Si substrate. In the cross-sectional TEM images, the red dashed lines mark the location of VDP devices. The overgrowth on the VDP-2 is amorphous, in support of the observed morphological irregularity in the STM image (f). (i) Correlation between sheet resistance and the difference in growth front roughness between the inside and the outside of STM-patterned VDP device regions. The analyzed roughness is based on calculating averaged root mean square (RMS) roughness from topographic STM images, where the uncertainties represent one standard deviation. Data points within the blue and red regions represent devices with acceptably low and unacceptable high sheet resistance values, respectively. We note that both the tip condition and the scale of the imaging affect the absolute value of STM measured surface roughness. To eliminate such imaging artifacts, we compare only roughness values taken from the same STM image across device boundaries.
The impact of different STM-lithography conditions on the Si:P device properties is illustrated in Figure 3.11. Two VDP devices, VDP-1 and VDP-2, are patterned next to each other on the same sample. This guarantees that both devices experience identical P incorporation and overgrowth conditions. The two VDP devices show distinct optical visibility in both bright field and dark field imaging modes. However, strong electronic signal contrast can be observed on both devices using peak force Kelvin force microscopy (PFKFM), which allows us to align electrical contacts to both devices. The sheet resistance at 4 K is ~1.5 k $\Omega$ /sq and >1 G $\Omega$ /sq for VDP-1 and VDP2, respectively. During process development, we find that the optically visible devices generally exhibit poor electrical properties. STM and TEM investigations on these two devices provide additional insight. The overgrowth is epitaxial on the hydrogen-resist and optically invisible (and electrically functional) for the VDP-1 device, while it is amorphous for the optically visible (and electrically defective) VDP-2 device. The drastic difference in epitaxy quality explains the variations observed in electrical properties between these two devices. In Figure 3.11 (i), we characterize a few representative VDP devices by their growth front roughness and electrical sheet resistance values. For the devices with low sheet resistance, the growth front roughness inside the device is similar to the growth front roughness outside the device (on the hydrogen resist). However, for the devices with high sheet resistance, due to the poor epitaxy quality, the growth front roughness inside the device is subject to large roughness variations with respect to the surrounding surface.



Figure 3.12 Impact of vacuum exposure before (a) and after (b)  $PH_3$  dosing on the sheet resistance of STM-patterned VDP devices. The exposure time before  $PH_3$  dosing includes both the STM lithography time and STM imaging time. The sheet resistance values are measured at T = 4 K. The impact of vacuum exposure is compared under two different sets of vacuum conditions. Before UHV system bakeout, the UHV vacuum has deteriorated due to repeated  $PH_3$  dosing experiments from  $\delta$ -layer fabrication. A UHV system bakeout restores a good quality vacuum environment. The approximate range of acceptable and unacceptable sheet resistance are shaded in blue and red respectively.

One potential cause of the significant variation in STM-patterned VDP devices is vacuum exposure variation during the STM-lithography step. For a delta-layer device, the clean Si surface is typically dosed within 1 hour of the sample flash anneal, so the impact from vacuum exposure is minimal. For STM-patterned devices, the STM lithography and imaging steps during device patterning are time-consuming, ranging from a few hours to more than 24 hours depending on the device design and tip performance. Once the hydrogen resist is lithographically patterned, the exposed device regions become chemically reactive and subject to contamination during the prolonged STM patterning process. The team at UNSW has implemented multiple-doping procedures where PH<sub>3</sub> dosing of the central device region is performed before STMpatterning the large area (and therefore time-consuming) contact pads.<sup>59</sup> As shown in Figure 3.12, we investigated the impact of vacuum exposure before and after PH<sub>3</sub> dosing on the sheet resistance of STM-patterned VDP devices. Since the STM chamber in our system also functions as a PH<sub>3</sub> dosing chamber, repeated PH<sub>3</sub> dosing experiments deteriorate the STM chamber vacuum. Regularly scheduled system bakeout is required to maintain good UHV vacuum in the STM chamber. For a set of VDP devices fabricated before a scheduled system bakeout, there exists a positive correlation between pre-dosing exposure time and sheet resistance. Low sheet resistance is only obtained for samples with a pre-dosing exposure time of less than ~5 hours. In an improved vacuum environment after a system bakeout, the VDP device sheet resistance remains low within a pre-dosing exposure up to at least ~30 hours. On the other hand, we found no obvious correlation between sheet resistance and vacuum exposure after a saturation dose of  $PH_3$ , both before and after system bakeout. The results in Figure 3.12 are direct evidence that, under our improved vacuum conditions, vacuum exposure has a negligible impact on the 2-D conductivity of STM-patterned devices.

T=4 K	$ ho~({ m k}\Omega/{ m sq})$	$n(10^{14}{ m cm^{-2}})$	$\mu (\mathrm{cm}^2/\mathrm{Vs})$	$l_{\phi}\left(\mathrm{nm} ight)$
Blanket $\delta$ -layer Devices	$0.8 \pm 0.2$	~2	30~60	25~101
STM-patterned VDP Devices	$1.1 \pm 0.4$	~1.8	19~44	26~48

Table 3.1 Typical electrical characteristics (at T=4 K) of  $\delta$ -doped and STM patterned VDP devices that are patterned under improved vacuum conditions. The fabrication of STM-patterned VDP devices follows the optimized P incorporation and encapsulation overgrowth processes for  $\delta$ -layer devices.



Figure 3.13 High-quality epitaxial encapsulation overgrowth on a STM-patterned 4terminal device. (a) Stitched STM images of a STM-patterned device after hydrogen depassivation lithography but before  $PH_3$  dosing. The patterning begins with the central region where atomic precision is required. An atomic resolution STM image is taken after patterning the central region to verify the atomic precision. Subsequently, the interconnect leads and contact pads are patterned. (b) STM topographical image (+2 V

sample bias, 0.1 nA set-point current) after encapsulation overgrowth. (c) dI/dV map acquired during STM topographical imaging. The strong differential conductance contrast originating from the buried device is utilized for *in-situ* re-location of buried devices. (d) (e) Zoomed in STM images at the central device region after overgrowth.

In Table 3.1, we summarize typical electrical parameters from the STM-patterned VDP devices that are fabricated under improved vacuum conditions, which compare well with the characteristic properties from  $\delta$ -layer devices. Following the optimized practice of encapsulation overgrowth, which will be described in detail in Chapter 5, we achieve high-fidelity and high-quality epitaxial encapsulation of STM-patterned devices, as illustrated in Figure 3.13.

### **3.12 Electrical Contacts to Atomic-scale Devices**

Forming robust ohmic contacts to buried, STM-patterned devices represents a key challenge in the fabrication of atomic-precise Si:P devices. In this section, we briefly review the two electrical contact strategies that have been developed in our group during this thesis. In a project led by Dr. Scott W. Schmucker, Dr. Pradeep Namboodiri, and Dr. M.D. Stewart, Jr., we developed a low-resistivity, high yield palladium silicide (Pd<sub>2</sub>Si) contact strategy.<sup>204</sup> In a project led by Dr. Aruna N. Ramanayaka and Dr. Joshua Pomeroy, we developed a photolithography-defined ion-implant contact strategy.<sup>205</sup> While the ion-implant contact approach uniquely contributes to our process development and will have immediate use for future *in situ* low temperature STM

device characterization, we exclusively use the Pd<sub>2</sub>Si contact approach for all STMpatterned devices in this thesis.

### **3.12.1 Previous Efforts**

The choice of strategies to electrically contact atomically precise Si:P devices is limited by the extremely restrictive thermal budget (ideally  $\leq 250$  °C) that is required to retain the precision nature of the fabricated devices. The team in UNSW have demonstrated two contact strategies using aluminum spiking<sup>206</sup> and aluminum vias<sup>207</sup> that meet the thermal budget requirement. For Al spiking contacts, e-beam defined Al metal is first deposited over the top of STM-patterned contact pads. A thermal anneal at 350 °C for 15 minutes under an  $N_2$  atmosphere allows silicon to diffuse into the Al metal pads and Al to refill the rectangular cavities that are left behind in the substrate, forming Al spikes. An electrical contact is formed when an Al spike penetrates through a buried contact pad. However, the randomness of the Al spiking process and low spike density are major drawbacks of Al spiking contacts resulting in low contact yields and irreproducibility in contact resistance. For Al via contacts, an array of dry-etched holes (the vias) are e-beam defined on STM-patterned contact pads, exposing the P-doped regions on the inner wall of the vias. Then e-beam defined Al is deposited and fills in the vias, forming electrical contact to the exposed contact pads. Al via contacts have been demonstrated by the UNSW team to form high fidelity contacts with low contact resistances.<sup>208</sup> However, the via etching process likely increases the risk of contaminating the exposed contact interface and leads to narrow process windows and significant variability and difficulty in reproducing the UNSW approach.



Figure 3.14 Pd<sub>2</sub>Si Contacts for STM-patterned and blanket  $\delta$ -layer devices. (a) crosssectional TEM micrograph of an annealed Pd<sub>2</sub>Si contact to a buried Si:P layer device. The red arrow indicates the P-doped layer. (b) Bright-field optical image of an STMpatterned device after e-beam defined Pd<sub>2</sub>Si contact formation. (c) Overlay between the Pd<sub>2</sub>Si contacts design and stitched STM images of the buried device after hydrogen lithography. (d) (e) Bright-field optical images of a typical  $\delta$ -layer device (a Hall bar) after a lithographically-defined etch step which removes P from outside the device area (d), and after Pd<sub>2</sub>Si contacts fabrication.

### 3.12.2 Silicide (Pd<sub>2</sub>Si) Contacts

For the Pd<sub>2</sub>Si contact strategy developed in our group,<sup>204</sup> e-beam defined Pd is deposited on top of STM-patterned contact pad regions and annealed at ~250 °C for 20 minutes. During the annealing process, Si and Pd interdiffuse and form a silicide in contact with the buried P-doped contact pads (see Figure 3.14). For Pd<sub>2</sub>Si silicide formation, 0.7 nm Si is consumed per nm of deposited Pd metal. To ensure silicide contacts reach the buried device (at ~30 nm below the surface), we deposit ~100 nm Pd to form silicide ~70 nm into the substrate. We have demonstrated low contact resistivity [on the order of (200 to 300)  $\Omega \cdot \mu$ m] and exceptionally high yield (>96% with 95% confidence) for Pd<sub>2</sub>Si contacts to buried Si:P planar structures.<sup>204</sup> One of the advantages of Pd<sub>2</sub>Si contacts over Al via contacts is that silicide formation does not expose the buried contact pads, ensuring an atomically clean contact interface. Also, the Pd<sub>2</sub>Si contact strategy is advantageous over the Al spiking contact strategy because the silicide formation process is deterministic, with sub-surface metal diffusion occurring uniformly across each lithographically-defined contact.



Figure 3.15 Ion-implant contacts to STM-patterned Si:P devices. (a) AFM topography image and (b) peak force Kelvin force microscopy (PFKFM) image of an STMpatterned wire device using ion-implant contacts. The images are taken after encapsulation overgrowth. Low-energy ion implantation of phosphorus atoms is used to create degenerately doped contact wires. Registration marks are etched for STM tip re-location and optical alignment. PFKFM measures the local surface work function variation. Both the buried ion-implant wires and the buried STM-patterned device are heavily doped with phosphorus, giving the same surface work function contrast in (b).

(c) Schematic (cross-sectional view) of the ion-implant contacts to STM-patterned devices. Electrical contacts are formed at the overlapping interface between the STM-patterns and the implant wires.

# **3.12.3 Ion-implant Contacts**

For ion-implant contacts,<sup>205, 209</sup> low-energy ion implantation of phosphorus atoms is used to create degenerately-doped contact wires before UHV sample preparation. The separation of the implanted wires has been optimized to be large enough to maintain electrical isolation after the sample flash anneal yet sufficiently small to fit in the maximally allowed STM scanning frame. Electrical contact is realized by defining STM-patterned contact pads on top of implant wires that allows a 2-D overlap between the electron systems of the device and the implant wires (see Figure 3.15). After encapsulation overgrowth, aluminum metal contacts are deposited using photolithography and form Al spiking contacts to the pre-defined implant wires. Detailed electrical characterization of the ion-implant contacts has been published elsewhere.<sup>205</sup>

# 3.13 Low-temperature Electrical Characterization

After successful fabrication of Si:P devices, we characterize electrical transport properties of the fabricated devices at low temperature. The manifestation of weak localization effects and single electron tunneling effects are enhanced at low temperature due to the suppression of random thermal fluctuations. Lightly boron doped Si substrates [ $\sim 3 \times 10^{15}$ /cm<sup>3</sup> doping density, (1 to 10)  $\Omega \cdot$  cm resistivity] are used for all the samples in this thesis. Free electron charge carriers originating from the substrate are frozen out at temperatures below ~50 K and cease to contribute to electrical transport.

We primarily use an Advanced Research Systems (ARS) closed-cycle helium cryostat with a base temperature of 3 K and a BlueFors LD400 dilution refrigerator with a base temperature of  $\sim 10$  mK for electrical characterization in this thesis. The cryostat features 12 bare copper wires for general measurements and four co-axial cables for low-noise measurements. The cryostat system is equipped with a GMW electromagnet that can generate a magnetic field up to 2 Tesla at the sample. The magnetic field at the sample location is calibrated using a SENIS AG magnetic field transducer. The cryostat design allows us to rotate the sample in the magnetic field for angle-dependent magneto-transport measurements. The dilution refrigerator features 36 low-Ohmic Cu+NbTi/CuNi twisted-wire pairs and a magnetic field up to 13 Tesla. Samples of particular interests have also been measured, in collaboration with Dr. Joseph Hagmann and Dr. Curt Richter using a He<sup>3</sup> cryostat system with a base temperature of 300 mK and a magnetic field up to 15 Tesla, or in collaboration with Dr. Andrew Murphy and Dr. Neil Zimmerman using another BlueFors dilution refrigerator with a base temperature of  $\sim$ 7 mK and a magnetic field up to 10 Tesla.



Figure 3.16 Hall and weak localization (WL) measurements on Si:P  $\delta$ -layer devices. (a) Schematic showing the AC measurement setup for Hall and weak localization measurements at low temperatures. (b) Example of Hall resistance  $\rho_{xy}$  typical for Hall measurements in a perpendicular and parallel magnetic field. (c) Example of the weak-localization correction to conductivity typical for sheet resistance  $\rho_{xx}$  measurements in a perpendicular and parallel for sheet resistance  $\rho_{xx}$  measurements in a perpendicular and parallel magnetic field.



Figure 3.17 Example of temperature dependent measurement results of a  $\delta$ -layer device. (a) Sheet resistance  $\rho_{xx}$  as a function of temperature. The logarithmic increase in sheet resistance with decreased temperature is dominated by weak localization (WL) effects. (b) Measurement of the WL quantum correction to  $\rho_{xx}$  at different temperatures. The WL effect is more prominent at lower temperatures. (c) Phase-

coherence length  $l_{\phi}$  as a function of temperature.  $l_{\phi}$  is obtained by fitting the WL results in (b) using the Hikami model (see Chapter 5 for details).

### **3.13.1 Si:P δ-layer Devices**

To characterize the 2-D electrical and magneto-transport properties of Si:P delta-doped layers, we fabricate blanket Si:P  $\delta$ -layers into Hall bar devices [see Figure 3.14 (d) & (e)]. Two-terminal and four-terminal direct-current (DC) I-V measurements are carried out using Keithley 2636B or 2401 System Source Measure Unit (SMU) to measure the contact resistance and 2-D sheet resistance of a Hall bar device. Magneto-transport measurements are performed using an alternating-current (AC) lock-in technique at low frequencies (11 Hz ~ 17 Hz) [see Figure 3.16 (a) for the AC measurement setup]. A constant AC excitation current is created by including a current limiting resistor  $(100 \text{ M}\Omega)$  between the sinusoidal voltage output of a lock-in amplifier and the source contact of a Hall bar device. A magnetic field is applied perpendicular or parallel to the sample substrate. Two synchronized lock-in amplifiers [Stanford Research System (SRS) SR830 or Ametek 7230 lock-in amplifiers] are used to monitor the voltage drop along the Hall bar (for weak localization characterization) and across the Hall bar (for Hall characterization). An optimum parallel magnetic field is obtained by fine-tuning the sample orientation while monitoring the slope of Hall resistance versus magnetic field (Hall slope) until it reaches zero. [See Figure 3.16 (b) & (c)] Figure 3.17 shows examples of temperature dependent measurement results of a  $\delta$ -layer device. Detailed magneto-transport characterization on Si:P  $\delta$ -layer devices will be presented in Chapter



Figure 3.18 Measurement setup for electrical transport characterization of STMpatterned four-terminal devices.





Figure 3.19 An example of a charge stability diagram of an STM-patterned single electron transistor (SET) that is measured at a base temperature of T=20 mK. The charge stability diagram is obtained by measuring differential conductance across drain-source leads while sweeping the source-drain bias at each gate voltage. A small AC excitation of 100  $\mu$ V at 11 Hz is superimposed on a DC bias across the source-drain leads using the adder circuit as shown in Figure 3.18. Typical measurement time for these data is approximately 24 hours.

### **3.13.2 STM-patterned Si:P Devices**

To characterize the electrical transport properties of STM-patterned Si:P devices, we first check for good ohmic contact by measuring the two-terminal resistance of the source and drain contact pads, which is typically a few k $\Omega$ . For gated devices, such as gated tunnel junctions and single electron transistors (SETs), we determine the effective gate voltage range for each gate, where the gate leakage current is required to remain below a certain threshold (typically ~50 pA) within the effective gate range. Excessive gate leakage current can alter the equivalent circuit diagram of a device and even cause damage at the atomic scale.<sup>207</sup> Finally, transport properties are measured as a function of control parameters, such as gate voltage, temperature, and magnetic field. In the case of SETs, we map the drain-source conductance while sweeping drain-source bias and gate voltage, generating charge stability diagrams. We also carry out charge offset drift measurements by repeatedly measuring the zero-bias Coulomb blockade oscillations as a function of time over a long period of time (typically a few days).

Figure 3.18 illustrates the measurement setup for STM-patterned four-terminal devices, where the output of the adder circuit can be approximated as,

$$V_{out} = \frac{V_{DC}R_2||R_3}{R_1 + R_2||R_3} + \frac{V_{AC}R_1||R_3}{R_2 + R_1||R_3} \approx \frac{V_{DC}R_3}{R_1} + \frac{V_{AC}R_3}{R_2} \qquad \text{for } R_3 \ll R_1, R_2$$
  
Equation 3.3

A Keithley 2636B SMU channel is used to apply a DC gate voltage and monitor gate leakage current. In DC measurements, a second SMU channel is used to apply DC bias across the source-drain leads and monitor the source-drain current. In AC measurements, an adder circuit is used to combine a small AC excitation signal and a DC bias (from the Sine output and the Aux output of an SRS SR830 lock-in amplifier. 109

The mixed bias is then applied across the drain and source leads. The source-drain current is amplified using an SRS SR570 low noise current amplifier, whose output voltage signal is taken as the lock-in amplifier input. In this thesis, all the SETs are biased using an asymmetric configuration where the source electrodes are grounded through the current amplifier. Bayonet Neill–Concelman (BNC) cables and connectors are used to connect all the instruments to a break-out box. Co-axial cables in the cryostat are used for both low noise DC and AC measurements. The automation of measurement and data acquisition are realized using LabView package via the general-purpose interface bus (GPIB).

An example of a charge stability diagram and charge offset drift measurement results from an STM-patterned SET is shown in Figure 3.19. Detailed electrical transportation characterization of STM-patterned SETs will be presented in Chapter 6.

### **3.14 Chapter Summary**

In this chapter, we have presented a complete atomically precise fabrication scheme that has been established in our lab during this thesis. We presented advancements in device fabrication and process control strategies that improve device quality and drastically increase fabrication yield. We summarized our optimal process parameters as well as lessons that we have learned during process development. This chapter is intended to provide the reader with useful insights into critical challenges in atomic precision fabrication and how to address them.

# **Chapter 4: Spatially Resolved Scanning Tunneling Spectroscopy of Single Layer Steps on Si (100) Surfaces**

Defects on surfaces can significantly affect surface electronic properties. Understanding the electronic and geometric effects that result from surface defects is critical to meaningful STM characterization of donor-based atomic-scale quantum devices, particularly those fabricated using hydrogen lithography.<sup>165, 210</sup> Although defects on flat terraces can be largely eliminated by careful sample cleaning and optimization of vacuum thermal processes, step-edge defects are inherent to Si (100) surfaces. The driving force behind the step formation on Si (100) surfaces is to minimize the anisotropic surface strain energy induced by the [110] direction miscut angle.<sup>211, 212</sup> The step density can further increase after Si homoepitaxial deposition,<sup>213</sup> which is an integral part of the donor-based atomic-scale device fabrication process. These effects that result from a large number of step edges can, however, be reduced by creating large atomically flat terraces by controlling the formation of the atomic step/terrace morphology.<sup>214</sup> STM studies<sup>215</sup> have indicated that some step edge formations are active sites to trap and bond Si monomers during Si homoepitaxy growth. It has been shown that atomic steps at a quantum-well interface in a Si-SiGe heterostructure can suppress the valley-splitting.<sup>216</sup> Step edges on surfaces have also been proposed as templates for conducting channels and spin chains for future silicon quantum computing.<sup>217, 218</sup> Therefore, detailed studies of the electronic properties of single-layer steps on the Si (100) surface not only contribute to successful fabrication and characterization of donor-based atomic-scale quantum devices and provide a better understanding of atomic dynamics on Si (100) surfaces, but also provide a means to engineer the electronic properties of nearby atomic structures.

# **4.1 Introduction**

Scanning tunneling microscopy (STM) is a powerful tool to investigate the geometric and electronic properties of Si (100) surfaces with atomic resolution. Single layer step morphology and growth mechanisms on Si (100) surfaces have been intensively studied using STM.<sup>212, 215, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230</sup> In addition, extensive scanning tunneling spectroscopy observations<sup>231, 232, 233</sup> and ab initio calculations<sup>234, 235, <sup>236, 237, 238</sup> have been carried out to study isolated dangling bonds and dangling bond wire systems on H-terminated Si (100) surfaces due to their technological importance as atomic-scale nanowires<sup>239</sup> and potential use in achieving atomic-scale quantum devices.<sup>240</sup> However, in spite of the significant effect on local electronic behavior, there has been very limited experimental<sup>230, 241</sup> and theoretical work<sup>211, 242</sup> providing insight into the electronic properties of single layer step edges on the Si (100) surface. In contrast to single point scanning tunneling spectroscopy,<sup>230, 241</sup> spatially resolved scanning tunneling spectroscopy can provide direct information on the spatial variation of energy states along a line scan.</sup>

Single-layer steps on Si (100) surfaces have been intensively studied using STM imaging because of their technical role in the homoepitaxy of Si on Si (100) substrates as well as the heteroepitaxy of III-V semiconductors on Si (100) substrates.<sup>243, 244, 245</sup> Single-layer steps on Si (100) surfaces can be classified as Single Layer Type A (SA) steps and Single Layer Type B (SB) steps <sup>246</sup> where the dimer is

perpendicular to the step edge on the upper terrace of an SA step and parallel to the step edge on the upper terrace of an SB step as shown in Figure 4.1.

In this Chapter, we present a spatially resolved Scanning Tunneling Spectroscopy (STS) study across single layer SA and SB step edges on Si (100) surfaces at room temperature. On a heavily boron-doped p-type substrate, the local density of states (LDOS) across SA steps was found to be very similar to those observed on flat terraces. STS observations show a narrow surface band gap at the SB step edge with a prominent density of states (DOS) peak located at the lower edge of the unoccupied dangling bond surface states on a clean Si (100) 2x1 surface. To quantitatively characterize the surface DOS at the step edges as well as their influence on the local electrostatic environment, we employ 3-D electrostatic simulations and firstly assume a hyperbolic tip shape and fit the tip geometry and work function parameters by comparing the simulated band bending with the experimental values on flat terraces. Then, by estimating the SB edge DOS peak area and width, and their spatial distribution from the STS and STM observations, we fit the edge state energy levels at and near the SB step edge. The simulated local band bending landscape in the proximity of the tip and the SB step edge at various sample bias conditions is compared with the features in a measured spectroscopic map. Finally, the observed surface band gap at the SB step edge is corrected using the simulated local band bending results.



Figure 4.1 Atomic structure of the monolayer SA step edge and rebonded SB step edge configurations on Si (100) surfaces as proposed by Chadi.<sup>246</sup> The large spheres represent Si atoms at the upper terrace. The medium spheres represent Si atoms one monolayer below the upper terrace. The light gray dots represent the Si atoms of the substrate. Dimers on the upper terrace are perpendicular to the SA step edge and parallel to the SB step edge. The orange spheres represent buckled dimer atoms along the SA step edge. The red spheres represent Si atoms at the rebonded SB step edge. The green spheres represent Si atoms adjacent to the SB step edge on the upper terrace.

# **4.2 Experimental Methods**

A degenerately boron-doped p-type Si (100) substrate [(0.01 to 0.02)  $\Omega$ ·cm, miscut angle <±0.25°] was sonicated in deionized water and isopropanol at room temperature followed by chemical cleaning using RCA and Base Piranha followed by a dip into 2% HF solution before loading into the ultrahigh vacuum (UHV) system. The substrate was

degassed at 550 °C overnight, followed by several rapid flash anneals to 1200 °C using direct current heating while maintaining the chamber pressure below  $9 \times 10^{-10}$  Torr  $(1.2 \times 10^{-7} \text{ Pa})$ . After the final flash, the substrate was quenched to about 900 °C and slowly cooled down at -2 °C/sec. to room temperature.<sup>247</sup> Quadrupole high depth resolution second ion mass spectroscopy (SIMS) measurements were used to provide subsurface and bulk dopant density information for experimental and theoretical analyses, which showed that the thermal process results in a subsurface dopant depletion region (due to dopant out-diffusion) extending approximately 30 nm into the substrate. However, because the dopant depletion region is still degenerately doped after sample flashing, we treat this dopant depletion effect as negligible. Therefore, in this work, we assume a uniform dopant density as measured from deep inside the bulk sample substrate (3.5e18 /cm<sup>3</sup>). A chemically etched polycrystalline tungsten tip was cleaned in-situ by annealing to approximately 1000 °C for several hours before use. Tip condition was monitored by STM imaging stability as well as robust atomic resolution imaging of Si (100) dimers.

STM images at both negative and positive sample biases were taken on step edges, as shown in Figure 4.2. The dimer rows appear as bright rows in the filled state STM image in Figure 4.2 (a), and appear as dark rows in the empty state STM image in Figure 4.2 (b). To map the LDOS of the surface, we took I-V curves at points every 0.2 nm along the STS lines as depicted in the STM images in Figure 4.3 (b) and (c). The spectroscopy line in Figure 4.3 (b) was taken across dimers on a flat terrace. The spectroscopy line in Figure 4.3 (c) intersects an SA step edge and an eight-dimer-row wide (~6.16 nm wide) rebonded SB step edge at the same time. The section was taken

about 30 degrees with respect to the upper terrace dimer row direction. The I-V curves at each spatial point were measured at a constant tip-sample separation, which was set by the constant current imaging condition V = -1.8 V, and I = 0.18 nA, with the feedback loop on. The normalized differential conductance (dn) spectra, (dI/dV)/ $\overline{(I/V)}$ , were numerically derived from the measured I-V spectra following Feenstra.<sup>248</sup> <sup>87</sup> The tunneling current contains an energy integral of the product of the LDOS  $\rho(E)$ and transmission probability, T(E, eV), as shown in Equation 4.1, where E is the DOS energy level relative to the sample Fermi level and V is the sample bias. The normalized differential conductance (dI/dV)/(I/V) can be expressed in the form of Equation 4.2. Since T(E, eV) and T(eV, eV) appear as ratios in both the denominator and numerator, the transmission coefficient's exponential dependence on the tipsample separation and on sample bias voltage tends to cancel. As a result, the normalization procedure essentially eliminates the dependence of the measured DOS features at different tip-sample separations. The second term in the numerator in Equation 4.2 is a slowly varying "background" term due to the dependence on the sample bias voltage of the tails of the local wavefunctions in the tunneling barrier.<sup>87</sup> The total conductance (I/V) in the denominator in Equation 4.2 is a normalization factor. In order to avoid divergence of the dn spectrum at the band edges of large-bandgap surfaces and to obtain an experimental approximation of the surface DOS, the conductance (I/V) is smoothed over the range of voltages, denoted as  $\overline{(I/V)}$ , following Feenstra.<sup>248</sup>  $\Delta V$  is the band gap of bulk Silicon,  $\exp(-a'|V|)$  is a weighting factor, and a' is a typical exponential slope value, 2 V<sup>-1</sup>, of the tunneling current I(V).<sup>248</sup> In summary, the dn spectra as a function of sample bias approximately represent the surface LDOS distribution at different energy levels  $(cm^{-2}eV^{-1})$ . To first order, the integrated area under each peak is proportional to the total LDOS  $(cm^{-2})$  of the corresponding surface state.

$$I \propto \int_0^{eV} \rho(E) T(E, eV) dE$$

Equation 4.1

$$\frac{dI/dV}{I/V} = \frac{\rho(eV) + \int_0^{eV} \frac{\rho(E)}{T(eV,eV)} \frac{d}{d(eV)} [T(E,eV)] dE}{\frac{1}{eV} \int_0^{eV} \rho(eV) \frac{T(E,eV)}{T(eV,eV)} dE}$$

Equation 4.2

$$\overline{(I/V)} = \exp(a'|V|) \int_{-\infty}^{+\infty} [I(V')/V'] \exp\left\{\frac{-|V'-V|}{\Delta V}\right\} \exp(-a'|V'|) dV'$$

Equation 4.3



Figure 4.2 STM images of single layer SA and rebonded SB steps on a degenerately boron-doped p-type Si (100) substrate surface. (a) Filled state image: -1.5 V, 0.15 nA, (b) Empty state image: +0.7 V, 0.15 nA. The dimer rows appear as bright rows in the filled state image (a), and appear as dark rows in the empty state image (b). The dimers along SA step edges are buckled. The spatial distribution of unoccupied edge states at the rebonded SB step edge is emphasized by the bright protrusions along the rebonded SB step edge in (b). (c) A zoom-in on the squared area in (b) with a close-up view of the corresponding atomic structure, where the large blue circle marks a dimer at the upper edge of the rebonded SB step edge, and the two small circles mark the unpaired dangling bonds at the lower edge of the rebonded SB step edge.



Figure 4.3 (a) A filled state STM image of an SA and a rebonded SB step edge taken at -1.8 V, 0.18 nA. (b) plots the  $(dI/dV)/(\overline{I/V})$  spectra across dimer rows on a flat terrace. (b) plots the  $(dI/dV)/(\overline{I/V})$  spectra across a monolayer SA step edge and a rebonded SB step edge. The spectroscopy paths are indicated by the dashed lines in the STM images and the atomic structure diagrams above the spectroscopy maps. The  $(dI/dV)/(\overline{I/V})$  spectra are plotted in color scales [in arbitrary units (A.U.)] with the bias voltage on the vertical axes and the spatial coordinate X on the horizontal axes. The red dots in the spectroscopy maps illustrate the measured topography profiles along the spectroscopy paths in arbitrary units. The spectroscopic features from the  $\pi$ ,  $\pi_1^*$ , and  $\pi_2^*$  surface dangling bond states are marked in yellow, as will be discussed in the

experimental section. The yellow arrows in (c) emphasize the prominent unoccupied LDOS peak at the rebonded SB step edge as well as a measured peak position shift along the spectroscopy path. The dashed lines in red-violet represent the simulated local band bending curves under the tip apex, as will be discussed in the theoretical section.

# **4.3 Experimental Results and Discussion**

# **4.3.1 Identifying Surface Dangling Bond States in Scanning Tunneling Spectroscopy**

The electronic structure of Si (100) surfaces has been extensively studied using angleresolved photoemission spectroscopy (ARPES),<sup>127, 249, 250, 251, 252, 253</sup> inverse photoemission,<sup>251, 254</sup> electron-energy-loss spectroscopy (EELS), two-photon photoemission spectroscopy (PPE),<sup>255, 256</sup> as well as scanning tunneling spectroscopy<sup>257, 258</sup> and numerous theoretical calculations.<sup>259, 260</sup> The asymmetric (buckled) c (4x2) dimer model of the Si (100) surfaces, first introduced by Chadi,<sup>261</sup> results in minimum surface free energy and a semiconducting surface band gap that agrees with photoemission experiments. This c (4×2) buckled dimer reconstruction structure is well known as the ground state of the Si (100) surface at low temperature. The asymmetric dimer atoms are connected by a dimer bond and are attached to the bulk substrate via back bonds. The occupied dangling bond state is primarily located at the upper Si atom of the buckled dimer, and the unoccupied dangling bond state is primarily located at the lower dimer atom. They are conventionally denoted as the  $D_{up}$ and  $D_{down}$  dangling bond states. Since the charge transfer from the lower dimer atom to the upper atom is incomplete,<sup>257</sup> and also because STM/STS observations at room temperature are the result of time-averaged rapid flipping of buckled dimers, we adopted the nomenclature of  $\pi$  and  $\pi^*$  (anti- $\pi$ ) states from a symmetric dimer picture to represent the occupied and unoccupied dangling bond states for the remainder of this paper. The agreement between room temperature photoemission spectroscopy results with low-temperature electronic structure calculations suggests that the energetics of buckled dimer surface reconstruction persists up to room temperature.<sup>128</sup>

We follow the conventional description and denote the two occupied  $\pi$  surface bands as  $\pi_1$  and  $\pi_2$ , and the two unoccupied  $\pi^*$  surface bands as  $\pi_1^*$  and  $\pi_2^*$ , which are derived from the four dangling bonds in each of the c (4×2) unit cells.<sup>127, 128, 250, 251, 262, <sup>263</sup> Based on previous photoemission experiments<sup>47, 48, 62, 64, 65, 69</sup> and theoretical results<sup>52, 66, 67, 69</sup> on the  $\pi$  and  $\pi^*$  band structures on Si (100) surfaces, we adopted the following set of surface dangling bond parameters in Gaussian distribution in this study [Table 1 and Figure 4.6 (b)]. The  $\pi$  band is composed of two sub-bands centered at -0.25 eV and -0.50 eV below the valence band maximum (VBM) with a full width at half maximum (FWHM) of 0.30 eV and 0.20 eV, respectively. The two  $\pi^*$  sub-bands are centered at 0.69 eV (averaged between experimental values of 0.66 eV <sup>48</sup> and 0.72 eV <sup>47</sup>) and 1.20 eV above the VBM with FWHM of 0.30 eV and 0.20 eV respectively. From the atomic density on the Si (100) plane, we have  $3.37 \times 10^{14}$  /cm<sup>2</sup> as the surface state density for each of the four dangling bond states ( $\pi_1$ ,  $\pi_2$ ,  $\pi_1^*$ , and  $\pi_2^*$ ), including spin degeneracy.</sup>

Dangling Bond States		Donor-like $\pi$ Bands			Acceptor-like $\pi^*$ Bands		
		Energy level	Surface	FWHM	Energy	Surface	FWHM
		above VBM	Density	(eV)	level above	Density	(eV)
		(eV)	(/cm²)		VBM (eV)	(/cm²)	
On Flat	1 <sup>st</sup> sub-band	-0.50	3.37e14	0.30	0.69	3.37e14	0.30
Terraces	2 <sup>nd</sup> sub-band	-0.25	3.37e14	0.20	1.20	3.37e14	0.20
At SB Step	SB Edge State						
Edge	Peaks (intrinsic	E1	4.20e14	0.32	E <sub>2</sub>	8.11e14	0.30
	model)						

Table 4.1 Surface dangling bond state parameters on flat terraces of Si (100) surfaces adopted from previous PES and DFT results.<sup>127, 249, 250, 251, 252, 253, 254, 255, 256, 259, 260</sup> In the intrinsic edge state model, which is discussed in the theatrical section, the surface state density and FWHM at the step edge are scaled by the same factors used when scaling the peaks from the flat terraces.  $E_1$  and  $E_2$  are the two fitting parameters in the intrinsic SB edge state model.

Photoemission Spectroscopy (PES) studies<sup>264, 265, 266, 267</sup> have shown that the Si (100) surface is semiconducting at room temperature. The surface bandgap of the clean Si (100) surface is approximately half the bandgap of an H-terminated Si (100) surface.<sup>263</sup> Due to the inelastic scattering of vertically injected tunneling electrons from a 3-D tip at the surface, the measured DOS spectrum is an integral over the entire 2-D *k*-space band diagram. At room temperature, we obtained dn curves on both clean and H-terminated Si (100) surfaces, as shown by the brown and blue curves in Figure 4.4 (b), that agree very well with previous studies.<sup>232, 257, 258, 263, 268, 269</sup> The absence of the three peaks on the hydrogen-terminated surface confirms that the occupied state peak and the two unoccupied state peaks on clean Si (100) surfaces, the peak in the negative bias region

arises from the occupied  $\pi_2$  band centered at 0.25 eV below the VBM. The occupied  $\pi_1$  band cannot be resolved due to its broad dispersion in k-space and the limited energy resolution at room temperature. The first unoccupied state peak arises from the states at the bottom of the unoccupied surface  $\pi^*$  band centered at 0.69 eV above the VBM. The assignment of the second unoccupied state peak has been discussed extensively<sup>257,</sup> <sup>258, 263, 269, 270</sup> regarding whether this peak originates from unoccupied back-bond states or the upper edge of the  $\pi^*$  band. The second unoccupied state peaks in the blue and cyan curves in Figure 4.4 (b) show a spatial variation with a high intensity between dimer rows and a low intensity over the dimer rows, which agrees with recent experimental<sup>269</sup> and theoretical<sup>271</sup> studies. Previous interpretation<sup>233, 259, 272, 273</sup> assigned this peak to either the unoccupied back-bond\* states or the unoccupied dimer-bond states, while the dangling bond  $\pi^*$  state might also mix into this peak.<sup>271</sup> However, due to the high strength of the second unoccupied state peak in the dn spectrum and the relatively high energy level of the unoccupied dimer-bond state from photoemission results,<sup>251, 255, 256</sup> most recent STS observations and ab initio calculations<sup>257, 258</sup> have assigned this second unoccupied state peak to the upper edge of the  $\pi^*$  dangling bond state band ( $\pi_2^*$  state band). The unoccupied dimer-bond state may account for the third unoccupied state peak as observed near +2.0 V sample bias voltage.<sup>257</sup> In summary, we assign the observed first occupied state peak in our STS spectra to the second occupied  $\pi$  band ( $\pi_2$  band) at -0.25 eV below the VBM, and the observed first and second unoccupied state peaks to the  $\pi_1^*$  and  $\pi_2^*$  bands at +0.69 eV and +1.20 eV above the VBM respectively.

The measured I-V curves are averaged over different regions (as indicated in Figure 4.1) on the surface and converted to dn spectra as shown in Figures 4.4 (a) and (b). The SB edge region is defined by the bright protrusion area, about 0.8 nm wide, along the SB step edge, as shown in Figure 4.2 (b) and (c). The SA step edge region is about 1 dimer row wide along the SA step edge. The "near SB edge region" covers the upper terrace areas within two to three dimers of the SB edge (the green region in Figure 4.1). The flat terrace region is defined as areas at least 4 nm away from any step edge. While the surface dangling bond states that correspond to  $\pi$ ,  $\pi_1^*$ , and  $\pi_2^*$  bands are recognizable near the SB step edge, the measured dangling bond peak positions near the SB step edge feel strong Coulomb interactions from the charge states at the edge, and therefore shift from the corresponding peak positions as observed on flat terraces. As the data acquisition points move further away from the SB step edge into the upper flat terrace, the measured spectroscopic features approach the blue curve in Figure 4.4 (b) that was obtained on a flat terrace. Due to the finite size of the tip, the LDOS measurements on a lower terrace near a step edge is expected to strongly convolute with the step edge geometry. The potential irregularity of the tip shape could further complicate this geometric convolution effect. In the interest of simplicity, we only used the LDOS spectra measured on the upper terrace side of the step edge where the geometrical convolution with the step edge is relatively small.

The room temperature measured dn peaks from dangling bond states are fitted using a Gaussian function, as shown in Figure 4.5. The area under each of the dangling bond peaks is averaged over dimer tops and dimer troughs on flat terraces and then normalized to the known dangling bond DOS values on flat terraces,  $3.37 \times 10^{14}$  /cm<sup>2</sup>.

The surface LDOS at the step edges are scaled by the same factors used when scaling the peaks from the flat terraces. The derived LDOS values are summarized in Table 4.2. Comparing the DOS values on flat terraces with those at an SA step edge, the densities of the  $\pi_2$  and  $\pi_1^*$  dangling bond states are lower and the densities of the  $\pi_1$ and  $\pi_2^*$  dangling bond states are higher. But the total number of dangling bond states at the SA step edge is roughly conserved. The upper terrace near the SB step edge has fewer dangling bond states in total, and the SB step edge has larger dangling bond DOS in total as compared with the total dangling bond DOS on the flat terrace. However, the total number of dangling bond states is roughly conserved in combining "near SB step edge" and the SB step edge regions.



Figure 4.4 (a) The averaged I-V curve spectra, and (b) the normalized differential conductance  $(dI/dV)/(\overline{I/V})$  spectra (dn spectra) measured at dimer tops and dimer troughs on flat terraces as well as at monolayer step edge regions on a clean Si (100) 2×1 surface of a  $3.5 \times 10^{18}$  /cm<sup>3</sup> boron-doped p-type substrate. The spectrum curves measured on the flat terraces of a hydrogen-terminated Si (100) 2×1 surface of the same

substrate are also plotted for comparison. The zero sample bias aligns with the substrate's Fermi level. Band gap features appear in all the spectroscopy curves, indicating that the monolayer step edges under observation do not change the semiconducting nature of the surface, but do change the local semiconducting properties of the surface.



Figure 4.5 The measured surface states peaks in the (dI/dV)/(I/V) spectra curves are fitted using Gaussian distributions. (a), (b), (c), and (d) plot the original spectra data points as well as the fitted curves on flat terraces, at the SA step edge, near the SB step edge, and at the SB step edge respectively. The four peaks on the flat terrace correspond to the  $\pi_1$ ,  $\pi_2$ ,  $\pi_1^*$ , and  $\pi_2^*$  dangling bond states. The observed onset energy levels of the band extrema are determined by assuming linear onsets on the normalized differential

conductance spectra following Feenstra.<sup>248</sup> The spectra are fitted with straight lines on either side of the onset, and the onset position is obtained by the intersection of the lines.

Surface	DOS Peaks Normalized to the average of Dimer Top and Trough						
Regions	(x10 <sup>14</sup> /cm <sup>2</sup> )						
	1st	2nd	1st	2 <sup>nd</sup> unoccupied	Total		
	Occupied	Occupied	unoccupied	State Peak			
	State Peak	State Peak	State Peak				
Terrace Ave	3.37	3.37	3.37	3.37	13.48		
Dimer Top	3.29	3.59	3.13	3.72	13.73		
Dimer Trough	3.45	3.15	3.61	3.02	13.23		
SA Edge	4.20	2.56	1.79	4.10	12.65		
Near SB Edge	2.47	2.86	3.12	2.11	10.56		
SB Edge	2.01	4.20	8.11	2.38	16.70		

Table 4.2 Normalized DOS of each surface state peak at different areas on the Si (100) surface. The area under each of the dangling bond peaks is averaged over dimer tops and dimer troughs on flat terraces and then normalized to the known dangling bond DOS values. The surface LDOS at the step edges are scaled by the same factors used when scaling the peaks from the flat terraces.

### 4.3.2 Tunneling Spectra at the Single Layer SA Step Edge

Yokoyama et al.<sup>274</sup> has studied the influence of step induced local stress on dimer buckling and the  $(2\times1)$  reconstruction phase transitions on Si (100) surfaces. At room temperature, the buckling along the upper edge of an SA step is stabilized due to an increased flip-flop barrier height caused by a small displacement (lattice strain) of second layer atoms in the presence of an SA step edge.<sup>211, 227</sup> The dimer rows are buckled along the upper edge of SA steps in our STM images [as shown in Figure 4.2 (a), (b) and Figure 4.3(a)], which agrees with the previous observations<sup>12,13,262</sup> at room temperature.

SA step edges have lower formation energy than SB step edges because SA step edges do not lead to large lattice strains or extra dangling bonds. The surface dimerization is nearly unchanged near an SA step edge.<sup>246, 275</sup> Along the upper edge of an SA step, only one buckling type was observed experimentally, where the upper atoms in the buckled dimers are aligned with the lower terrace dimer centers, and the lower atoms in the buckled dimer are aligned with the troughs between dimer rows on the lower terrace.<sup>221, 227</sup> The appearance of alternative buckling along the first dimer row on the upper terrace of an SA step has been shown to be induced by step edge geometries rather than electronic structure.<sup>211</sup> Our dn spectra at an SA step edge [yellow curve in Figure 4.4 (b)] reveal that its electronic structure behaves very similarly to that on flat terraces, which supports previous observations. A band gap of about 0.5 eV observed at an SA step edge is roughly the same as that observed on flat terraces. Besides, the continuity of the dn spectra across the SA step edge [Figure 4.3 (c)] shows that the presence of an SA step edge introduces little perturbation to the local electronic environment.

### 4.3.3 Tunneling Spectra at the Single Layer SB Step Edge

The observed monolayer SB step edges in this work appear bright in low positive sample bias imaging conditions as shown in Figure 4.2 (b) (c). As can be seen from the red curve in Figure 4.4 (b), at the SB step edge, a prominent unoccupied state peak

stands out near the lower edge of the  $\pi_1^*$  surface band. In addition, as the data acquisition point approaches the SB step edge from the upper flat terrace, the observed  $\pi$  state peak shifts towards the higher sample bias voltage as can be seen in Figure 4.3 (c). The explanation of this peak position shift over space will be given in the theoretical section.

Two types of SB step edge configurations have been proposed by Chadi.<sup>246</sup> One is the nonrebonded SB step edge that does not form dimer bonds with the lower terrace atoms and has a dangling bond on each of the upper terrace edge atoms. The other one is a rebonded SB step edge (as shown in Figure 4.1) that forms dimer-like bonds with the lower terrace atoms and has an unpaired dangling bond at each of the Si atoms on the lower terrace edge. The nonrebonded SB step configuration is considered to be energetically unfavorable when compared with the rebonded type SB step edge configuration,<sup>221, 222, 246, 276</sup> though the step edge energetics are affected by detailed reconstruction on the upper and lower terraces.<sup>211</sup> In practice, three types of SB step edges have been observed by STM, namely, rebonded SB edges, nonrebonded SB edges, and nonrebonded SB edges with a split-off dimer. <sup>221, 222, 229, 230</sup> As shown by STM imaging in Figure 4.2, both the SB step edge dimers on the upper terrace and the edge atoms on the lower terrace appear as bright protrusions in an empty state image [Figure 4.2 (b) (c)], indicating that the observed SB step edges in this work are rebonded SB step edges.<sup>230 277</sup> The spatial extension of the bright protrusion areas along the rebounded SB step edge in Figure 4.2 (b) and (c) agree very well with the spatial distribution of the prominent unoccupied LDOS peak at the SB step edge, as marked by a yellow arrow in Figure 4.3 (c). Upon hydrogen chemisorption, the nonrebonded SB step edge becomes energetically favorable and dominates the monolayer SB step structures on hydrogen-terminated Si (100) surfaces.<sup>278, 279, 280</sup> As will be shown in the last section of this chapter, we did not observe band gap edge states nor local charging effects across either SA or SB step edges on hydrogen terminated Si (100) surfaces. The STS spectra across both the SA and SB step edges are essentially the same as the brown curve shown in Figure 4.4. This provides additional evidence that the observed edge states on the clean Si (100) surfaces are related to the surface dangling bonds at the step edges.

According to Jaloviar et al.,<sup>275</sup> the rebonded dimer on the lower terrace has one of its dangling bonds bonded as a backbond with the upper edge atom, and this rebonding causes strain on the backbond of the nearest dimer on the upper terrace. As a result, our observation of the strong enhancement of local density of unoccupied states along the rebonded SB step edge is likely to originate from a combined effect of both the  $3P_z$  orbital of the unpaired dangling bond along the lower edge and the rehybridization of rebonded step edge atomic orbitals. Surface atom core level shifts have been used as a tool to probe the local chemical bonding environment of individual surface atoms due to their sensitivity to the local valence charge distributions.<sup>281, 282, 283, <sup>284</sup> On clean Si (100) c (4×2) reconstruction surfaces, shifted core components in the surface Si 2*p* spectrum have been identified by previous photoemission spectroscopy and theoretical studies.<sup>281, 282, 283</sup> Our characterization of the local valence states and charge redistributions at the rebonded SB step edge may provide additional information on unidentified core shift components.</sup>
It is interesting to mention here that, from Figure 4.2, the flat terrace areas appear to include local defects which have a structure similar to the step edges B. Indeed, some of the vacancy defects and C-type defects on flat terrace areas could behave very similar to SB step edges in bias dependent STM images. Although we have not explored this phenomenon, it will be very interesting to study the local band structure of these terrace defects in future work.

# **4.4 Quantifying Step Edge Effects on the Local Electrostatic Environment**

We used band bending calculations to simulate the SB step edge's influence on the local electrostatic environment under various scanning tunneling conditions. The principle underlying the surface band bending calculations can be explained in the following way. The truncation of 3-D bulk Si introduces 2-D surface states on the surface. The surface charge states give rise to subsurface band-bending near the surface. Similarly, the truncation of a 2-D flat surface terrace at a step edge introduces 1-D edge states along the step edge. The step edge charge states can give rise to 2-D surface band-bending. However, since the tunnel junction in an STS measurement has 3-D characteristics and the 2-D terraces on the Si (100) surface are also sitting on a 3-D bulk Si substrate, both the surface charge states and the step edge charge states influence the band bending near a surface step edge.

An example of a band diagram at a specific sample bias is illustrated in Figure 4.6 (c). The surface band bending is the potential difference between the surface and deep inside the bulk substrate. The STS measured dangling bond energy levels can be

expressed as  $E_{STS} = eV_{bias} + E_{Fermi}$  above the bulk VBM, where  $V_{bias}$  is the corresponding sample bias value at the measured DOS peak. The photoemission spectroscopy results are given by  $E_{PES}$  above the VBM. Therefore, the surface band bending  $BB_{Exp}$  can be derived from the following expression,

$$BB_{Exp.i} = E_{STS_i} + E_{Fermi} - E_{PES_i}$$

Equation 4.4

where *i* stands for  $\pi$ ,  $\pi_1^*$ , and  $\pi_2^*$  surface states as observed in the STS spectra.  $E_{Fermi}$  is the Fermi level relative to the bulk VBM (0.025 eV from our semi-classical calculations for this work) and  $BB_{Exp.}$  is the band bending value at the sample bias,  $V_{bias}$ . Following Equation 4.4, the experimentally observed local band bending values on the flat terrace and near the SB step edge were plotted as blue and green colored data points in Figures 4.7 (a) (b). The band-bending data points in red color were obtained by substituting  $E_{PES}$  with the best-fit energy levels  $E_1$  and  $E_2$  at the SB step edge using the intrinsic edge state model, which will be discussed in the next section. The error bars for each data point represent one standard deviation of the measured peak positions.



Figure 4.6 Three-dimensional (3-D) calculation of the local electrostatic environment at rebonded SB step edges. (a) A 3-D diagram showing a hyperbolic tungsten tip at monolayer step edges on a Si (100) surface. *s* is the tip-sample separation, and *R* is the tip radius of curvature. (b) The DOS distributions used in band bending simulations. The blue curve represents the occupied and unoccupied dangling bond DOS distributions on flat terraces as adopted from previous PES and DFT results.<sup>127, 249, 250,  $2^{51, 252, 253, 254, 255, 256, 259, 260}$  The red curve represents the best-fit rebonded SB edge DOS distribution using an intrinsic edge DOS model.<sup>76</sup> The flat green line represents the best-fit rebonded SB edge DOS distribution using an extrinsic edge DOS model<sup>76</sup> where a uniform defect state distribution in units of  $(cm^2 \cdot eV)^{-1}$  and an edge state charge neutrality level above the VBM (vertical dashed purple line) are the two fitting parameters. (c) An example of the band diagram near a clean Si (100) surface at a negative sample bias. The surface DOS distributions are also plotted at the substratevacuum interface with the DOS amplitudes in arbitrary units. The different surface</sup>

DOS distributions on flat terraces and at the step edge regions will give very different electrostatic characteristics at the surface.

The electrostatic calculations in this study were conducted using a three-dimensional tip-semiconductor tunneling model following Feenstra.<sup>285, 286, 287</sup> We assumed a hyperbolic shaped tip [Figure 4.6 (a)] described by three key parameters, namely, the tip-sample separation (s), tip radius of curvature (R), and the tip potential boundary condition at zero bias (*CPot*). It is worth pointing out that in our theoretical calculations, *CPot* is defined as the tip potential relative to the ground potential (VBM deep inside the bulk substrate). Since the substrate doping level is experimentally known from SIMS measurements and the commonly used electron affinity energy of Si (0.41 eV) was adopted in this work, the *CPot* value depends only on the tip work function and is independent of the surface state distributions on the Si surface. The surface dangling bond state distributions on flat terraces were adopted from the photoemission spectroscopy results as described before.

The SB edge effects on the local electrostatic environment are modeled in two different ways. The first model is to treat the edge states as additional extrinsic defect surface states that distribute uniformly over all the surface and the energy space. The measured local band bending near the SB step edge were used to fit the two edge state parameters, namely, the uniform edge DOS distribution in units of  $(\text{cm}^2 \cdot \text{eV})^{-1}$  and an edge states charge neutrality level in units of eV above the VBM at the surface. The edge states below (above) the edge state charge neutrality level are donor (acceptor) like. The surface charge density was calculated by comparing the Fermi level at the

surface with the overall surface charge neutrality level. Surface state resonances with bulk states below the VBM or above the conduction band minimum (CBM) are not treated in these simulations.<sup>287</sup> A more realistic way is to treat the SB edge states as an intrinsic surface state distribution, therefore, the states are localized in specific areas on the surface and in the energy domain. From the STM and STS observations, we limit the observed SB edge states within a 0.8 nm wide by 6.16 nm long region that corresponds to an eight-dimer-row wide SB step edge. The edge state distribution is composed of a pair of occupied and unoccupied state peaks on either side of the Fermi level. The DOS and FWHM at the SB step edge are scaled by the same factors used when scaling the peaks from the flat terraces. SB edge state energy levels  $E_1$  and  $E_2$  are the two fitting parameters in this intrinsic SB edge state model, as listed in the last row in Table 1.

In general, we first used the band bending values obtained on flat terraces [blue data points in Figure 4.7 (a) (b)] as constraints to obtain a set of best-fit tip parameters. We then used these best-fit tip parameters and the observed band bending values at and near the SB step edge [red and green data points in Figure 4.7 (a), (b)] as constraints to obtain a set of best-fit step edge parameters. Finally, both the best-fit tip and SB edge state parameters were used to quantify the edge induced charge states and their effects on the local electrostatic environment in the STS measurements.

### 4.4.1 Quantifying the Tip parameters on Flat Terraces

The parametric fitting procedures yielded a tip-sample separation of 0.408 nm, a tip radius of curvature of 52 nm, and a *CPot* value of -0.61 eV. This predicted large tip

radius of curvature is with respect to its local electrostatic potential effects. However, since it is the topmost atom at the tip apex that dominates the tunneling conductance, such a large tip radius does not affect the ability to obtain atomically resolved images and spectroscopy results.

## **4.4.2 Quantifying the Edge States Using an Extrinsic Edge State Distribution Model**

Using an extrinsic edge state model, the best-fit effective rebonded SB step edge DOS is 5.3e13 / (cm<sup>2</sup> eV) with an edge state charge neutrality level approximately 0.01 eV above the VBM. The fitted DOS result is plotted in Figure 4.6 (b). To properly interpret the best-fit edge parameters in this crude model, one should recall that from the experimental results [Figure 4.4 (b)] rather than an idealized uniform distribution, the rebonded SB step edge induced states are in fact mainly distributed near the upper edge of the surface band gap. As a result, the fitted charge neutrality level, under the approximation of a uniform edge state distribution, represents a lower limit of the real charge neutrality level of the edge state distribution.



Figure 4.7 Local surface band bending at Si (100) rebonded SB step edges. (a) Simulated band bending curves using the best-fit tip parameters on flat H-terminated Si (100) terraces (solid brown curve), on flat clean Si (100) terraces (solid blue curve), and at the rebonded SB step edge using intrinsic (solid red curve) and extrinsic (dashed purple curve) edge state distribution models. (b) The simulated surface band bending under the tip apex with the tip at different distances from the SB step edge using the intrinsic SB edge state distribution model. According to Equation 4.4, the experimental band bending data points on flat terraces (blue points), near the SB step edge (green points), and at the SB step edge (red points) are plotted in (a) and (b). Error bars for each point represent one standard deviation of the measured peak positions. (c) The simulated band bending landscapes at -0.6 V sample bias with the tip at different

distances from the SB step edge, using the intrinsic edge state model. The band bending landscapes at +0.6 V and +1.2 V sample biases at the same distances are given in (d). The dashed lines in red-violet connect the local band bending values under the tip apex at different tip positions. These dashed lines are used to map the experimentally observed peak position shift in Figure 4.3 (c).

## **4.4.3 Quantifying the Edge States Using an Intrinsic Edge State Distribution Model**

Using the intrinsic edge state model, the best-fit edge peak positions for the occupied and unoccupied states at the SB step edge are  $E_1 = -0.4$  eV and  $E_2 = +0.5$  eV above the VBM. The best fit SB edge state distribution is plotted in red curves in Figure 4.6 (b). Figure 4.7 (a) summarizes the simulated surface band bending under the tip apex under different surface conditions.

In Figure 4.7 (a), the brown curve shows the simulated surface band bending on a flat Hydrogen terminated Si (100) surface, i.e., in the absence of any dangling bond surface state. By adding dangling bond states on the flat terrace, the surface band bending is strongly pinned over the entire sample bias range, as shown by the blue curve. The dashed purple curve shows the calculated band bending under the tip apex in the presence of SB step edges using the best-fit uniform extrinsic edge DOS distribution model. The red curve is the simulated band bending under the tip apex using the best-fit intrinsic edge state distribution model when the tip is at the SB step edge. Comparing the purple and red curves, the extrinsic edge state model gives a stronger pinning effect at small sample biases due to the non-zero SB edge DOS distribution across the Fermi level. But the intrinsic edge state model provides stronger pinning effects at larger sample biases. Figure 4.7 (b) shows the simulated surface band bending under the tip apex with the tip at different distances from the SB step edge using the intrinsic SB edge state distribution model. It can be seen that the SB step edge's influence on the measured band bending under the tip apex becomes negligible when the tip is more than 3 nm away from the SB step edge. This prediction provides a crucial threshold distance within which the LDOS, and charge distributions at the rebonded SB step edge are likely to have a significant electrostatic influence on atomically precise quantum structures.

Figures 4.7 (c) and (d) show the simulated band bending landscapes with the tip at different distances from the SB step edge under three different sample bias conditions. The dash curves connect the local band bending values under the tip apex as a function of the tip distance from the SB step edge. At negative sample biases, the local charge arising from the intrinsic SB edge states significantly pin the bands at the SB step edge due to the low-lying unoccupied edge states. At positive sample biases, the local band bending at the SB step edge is slightly enhanced since the occupied edge state lies slightly below the  $\pi_2$  dangling bond state of the flat terraces. The dash curves from the simulation agree very well with the observed peak position shifts from Figure 4.3 (c) as the probe tip moves away from the SB step edge.

Surface Regions	Measured Band Gap	Band Gap as corrected
	(eV)	from BB simulation (eV)
Dimer Top	$0.5 \pm 0.1$	0.3 ± 0.2
Dimer Trough	$0.5 \pm 0.1$	0.3 ± 0.1
SA Edge	0.5 ± 0.1	0.3 ± 0.1
Near SB Edge	0.18 ± 0.05	0.14 ± 0.05

SB Edge 0.18 ± 0	05 0.17 ± 0.05
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Table 4.3 The measured band gaps from the experimental observations and their band bending corrected values from the intrinsic SB edge states model.

### **4.4.4 Characterizing the Band Gaps at Monolayer Step Edges**

We note that, as shown in figure 4.4 (b), the surface DOS within the surface band gap and at the Fermi level is nonzero on both the clean and hydrogen-terminated Si (100) surfaces. This nonzero value is the measurement noise level that originates from limited signal-to-noise ratio under the room temperature measurement conditions and from the conductance normalization procedure which exacerbates the tunneling noise at low bias near the Fermi level at the constant tip-sample separation data acquisition conditions. This noise level is observed in both the clean and hydrogen-terminated Si (100) surfaces spectra where the surfaces are known to be semiconducting. Therefore, the band gaps in this work are determined by assuming a linear onset of the normalized conductance above the noise level. Following Feenstra,<sup>248</sup> the onset bias of band extrema on either side of the band gap is determined by assuming a linear onset of the normalized conductance above the noise level. The measured gap on the flat terrace is about 0.5 eV. However, the gap significantly narrows down to about 0.18 eV near and at the rebonded SB step edge. The simulated band bending curves from the intrinsic SB edge states model in Figure 4.7 (a) and (b) were used to correct each of the conductance onset points. Specifically, the band gap values at Dimer Tops and Dimer Troughs on flat terraces and at the SA step edge were corrected by the blue curve in

Figure 4.7 (a). The band gap values at and near the SB step edge were corrected by the red and the red-violet curves in Figure 4.7 (b). The band gap values before and after band bending corrections are summarized in Table 4.3. The surface band gap values at the SA step edge decrease slightly as compared with the band gap value on flat terraces. The band gap at the SB step edge is only about half of the surface band gap value on flat terraces. Due to the observed band gap narrowing along the rebonded SB step edge, one must use caution when characterizing shallow atomic quantum devices near surfaces or interfaces in the presence of SB step edges. The 1-D edge states may introduce additional conducting channels or interband recombination paths having significant impacts on device functionality.

However, one needs to be cautious when interpreting this significant band narrowing behavior at the observed SB step edge. In addition to the atomic orbital hybridization as mentioned previously, the specific finite length of the 1-D edge and the substrate doping level are also likely contributions to the LDOS distributions along the step edges.

It is useful to compare the unpaired dangling bond states along the SB step edge as presented in this work with previous studies on 1-D dangling bond wire systems on Hydrogen terminated Si (100) surfaces. Interactions among dimers in a dangling bond wire system introduce dispersion from the hybridization of single dangling bond orbitals along the wire, also known as proximity broadening. Theoretical studies by Raza et al.<sup>236</sup> on unpaired dangling bond wires of infinite length along the dimer row show a wide surface state band centered near mid-gap of about 1.15 eV that eliminates the surface band gap. In contrast, the surface state dispersion of paired dangling bond wires of infinite length shows a semiconducting behavior, very similar to the  $\pi$  and  $\pi^*$  surface state bands on clean Si (100) terraces. Recent DFT calculations<sup>234, 238</sup> studied the energetics and stability of infinite and finite unpaired dangling bond wires. These DFT calculations found that finite unpaired dangling bond wires develop localized electronic states. Hitosugi et al.<sup>231</sup> observed these localized states created by the finite 1D length using STS on H-terminated Si (100) 2×1 surfaces.

The effects of substrate doping on the step edge states can be viewed in analogy to charge-induced state shifting<sup>258</sup> observed in isolated individual surface states. Isolated dangling bond states on Si (100) surfaces have been observed by Boland<sup>233</sup> and Hitosugi et al.<sup>231</sup> on moderately doped p-type substrates and heavily doped n-type substrates, where two peaks with similar magnitude are introduced on each side of the surface Fermi level. From the observations of Reusch et al.,<sup>258</sup> heavily doped p-type substrates give rise to a prominent unpaired dangling bond state peak above the Fermi level at the lower edge of the  $\pi^*$  band, but no additional occupied states above the  $\pi$  band. Observation of the dangling bond features across the SB step edge on the heavily boron-doped p-type substrate, shown in Figure 4.4 (b), shows a prominent unoccupied edge state peak above the Fermi level and a small DOS enhancement below the Fermi level, similar to the isolated unpaired dangling bonds on heavily doped p-type substrates.

As a final remark following the analysis of the edge states on clean Si (100) surfaces, we note a subtle but interesting attribute in our STS measurement results. As can be seen in Figure 4.3 (c) in the previous section, at small negative biases, the measured band bending on the right upper terrace is about 0.05 eV higher than that on

the lower and left upper terraces. While we cannot be definitive in the understanding of the cause, there are three known effects which may be present. The likely dominant effect is band-pinning due to charge transfer as a result of the rebonded SB step edge states. Our simulations (Figure 4.7 (c) show that at -0.6 eV sample bias, the local band bending is pinned to about 0.03 eV when 1.5 nm from the SB step edge on the right upper terrace (which corresponds to a distance of 3 nm to the right of the rebonded SB step edge in Figure 4.3 (c) after correcting for drift and dimer row/scan axis misalignment). The data [pink dashed line in Figure 4.7 (c)] show that the band-pinning under the tip due to the SB edge states requires more than a 5 nm distance from the rebonded SB step edge to asymptotically die out. The second known effect is that the actual potential landscape is not symmetric about the SB step edge due to the anisotropy of dimer rows, edge state asymmetry, and proximal distance of a terrace to the edge states. Finally, in a physical measurement situation, there are surface potential fluctuations due to random surface defects and subsurface dopants.

# **4.5 Impact of Hydrogen Termination on the Step-edge Electronic Structures**



Figure 4.8 Scanning tunneling spectroscopy of step edges on hydrogen-terminated Si (100) surfaces. (a) (b) The filled state STM images were taken at -1.8 V, 0.18 nA on a hydrogen-terminated Si (100) surface with high densities of SA and SB step edges. (b), (d) Plots of the  $(dI/dV)/(\overline{I/V})$  spectra across monolayer SA and SB step edges on the hydrogen terminated surface. Following the plot conventions in Figure 4.3, no edge states in the surface band gap are observed.

To investigate the impact of hydrogen termination on the electronic structure at the SA and SB step edges, as shown in Figure 4.8, we take STS across both SA and SB step edges on a hydrogen-terminated Si (100) surface. The high island density on the surface results from a sub-monolayer Si deposition process before the hydrogen termination. No edge states within the band gap nor local charging effects are observed at monolayer 144

step edges on the hydrogen-terminated surface. As expected, hydrogen termination saturates the dangling bonds both on flat terraces and at step edges, thereby removing the edge states from the surface band gap. As such, it is a clear demonstration of the lack of influence of a hydrogen-terminated step edge on the local electronic structure and STS spectra. This observation highlights the advantage of hydrogen termination in sub-surface imaging applications using STM/STS, such as *in-situ* characterization of buried single donor devices after the encapsulation overgrowth.

### **4.6 Chapter Summary**

We have conducted a detailed spatially resolved Scanning Tunneling Spectroscopy study across monolayer step edges on Si (100) surfaces, and quantitatively determined the local density of state distributions and band gap information at the step edges. The influence on the local electrostatic environment due to step edge states has been quantified while accounting for the effects of scanning tunneling measurement conditions. The dangling bond states on Si (100) surfaces have been utilized as a fingerprint to quantify the local band bending landscape and to make corrections to the experimentally observed surface state energy levels and band gap values at the step edge regions. We observe a significant band gap narrowing behavior along a rebonded SB step edge on a degenerately boron-doped p-type Si substrate. This study provides a clear experimental demonstration of the local electronic environment near the monolayer step edges on Si (100) surfaces, which paves the way towards successful *insitu* re-location and characterization of dopant quantum structures with potential applications in future silicon quantum computing.<sup>217</sup>

## **Chapter 5: Quantifying Atom-scale Dopant Movement and Electrical Confinement in Si:P Monolayers**

### **5.1 Introduction**

Highly phosphorus-doped silicon (Si:P) monolayers are a novel 2-D system that can be patterned with atomic-scale precision using advanced hydrogen lithography techniques.<sup>165, 288, 289</sup> When coupled to low-temperature epitaxial overgrowth, individual dopant placement into Si lattice sites with atomic precision in all three dimensions becomes possible.<sup>208</sup> In this way, atomically precise Si:P planar architectures, such as atomically abrupt wires,<sup>290, 291</sup> tunnel junctions,<sup>292</sup> quantum dots,<sup>210, 293</sup> single atom transistors,<sup>165</sup> and ordered single dopant arrays<sup>30, 294</sup> have been successfully defined on H-terminated Si(100) surfaces. These patterned devices are all encapsulated in epitaxial overgrown crystalline Si. Central to the fabrication and performance of these planar Si:P devices is the preservation of exact lattice locations of deterministically placed dopant atoms during overgrowth. In atomically precise fewdopant quantum devices and superlattice dopant arrays, spatial fluctuation in dopant positions by even a single lattice constant can disrupt the quantum device performance and dramatically alter the quantum coupling.<sup>295</sup> In highly doped Si:P planar contact and gate regions, deviation of the 2-D dopant confinement from an ideal Si:P monolayer has profound effects on 2-D electrical properties.<sup>296</sup> Atomically sharp dopant confinement, high dopant activation ratios, and a defect-free epitaxial environment are essential attributes of proposed donor-based Si:P quantum computer architectures,<sup>208, 293, 297</sup> necessitating the development of precision metrological and fabrication methodologies to control dopant confinement and epitaxial quality at the atomic scale.<sup>298</sup> In this chapter, we develop a robust quantification method to monitor and control, at the ultimate monoatomic layer scale, unintentional dopant movement and formation of lattice defects to enable characterization and optimization of Si:P monolayer fabrication, fundamental to donor-based Si quantum computing and atomically precise 2-D superlattice design.

Encapsulation of a Si:P monolayer device within a crystalline Si matrix fully activates P dopants, isolates the conducting channels from the complex surface and interface interactions, and protects the Si:P system against ambient degradation.<sup>195</sup> However, dopant segregation, diffusion, and surface roughening during the epitaxial encapsulation process redistributes dopant atoms and introduces large positional uncertainties in the resulting dopant locations.<sup>20, 21, 23, 30, 31</sup> Defect formation in epitaxial Si overgrowth can create deactivation centers,<sup>299</sup> decrease free carrier mobility,<sup>289</sup> and increase noise floors in Si:P 2-D systems.<sup>300</sup> A key development to address the wellknown trade-off between low-temperature encapsulation for sharp dopant confinement and high-temperature encapsulation for optimum epitaxial quality<sup>145, 146, 151</sup> has been the recent application of thin room-temperature grown layers, commonly referred to as locking layers (LL), followed by encapsulation overgrowth at elevated temperatures.<sup>198, 301, 302</sup> While theoretical calculations have been carried out on the effects of various levels of dopant confinement on Si:P 2-D properties,<sup>288, 296</sup> experimental quantification of dopant confinement and redistribution within roomtemperature grown LLs remains challenging with little success at the monoatomic layer scale. The importance of this challenge is paramount to the development and performance of atomically precise 2-D superlattice designs and donor-based quantum computing.<sup>30, 165</sup>

In this study, we develop for the first time a robust method to quantify dopant movement at the atomic scale during Si:P monolayer fabrication by combining segregation/diffusion models with sputtering profiling simulations. Dopant segregation, diffusion, surface accumulation, and growth front roughening have been taken into account in this quantitative investigation on the impact of LL growth parameters on dopant confinement, local crystalline quality, and dopant activation in Si:P 2-D systems. The extraordinarily high dopant density within the 2-D layers and the kinetically controlled 3-D island growth front during the room temperature LL overgrowth create a complex yet unique 2-D system environment that has been studied little to date. We experimentally determine, for the first time, the LL growth rate dependence of the dopant segregation length and the dopant diffusivity within LLs below the hydrogen desorption temperature. We combine scanning tunneling microscopy (STM), transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), atom probe tomography (APT), and low-temperature magnetotransport measurements to obtain detailed insight into optimizing Si:P 2-D system fabrication at the individual atom layer scale. To achieve this, we use weak localization analysis as a non-destructive quantum metrology method to explore the impact of the LL technique on the electrical thickness of the fabricated Si:P monolayers and verify the electrical confinement quality that is achievable using the LL technique. The locking layer overgrowth parameter space explored in this study is fully compatible with current state-of-the-art hydrogen lithography techniques and can be applied directly to fabricate atomically precise superlattices and quantum devices.



#### 5.2 Methods

Figure 5.1. STM topography images (+2 V bias on the substrate, 0.2 nA set-point current, 25 nm  $\times$  25 nm, acquired from different samples at different stages of preparation) with complementary atomic lattice top and side view schematics of the phosphine dosing, incorporation, and encapsulation processes on a blanket Si (100) 2×1 surface. In the schematic figures, the blue and cyan atoms represent Si on the surface and in bulk, respectively. Red atoms represent P, and orange atoms represent H. (a) A

typical starting Si (100) surface with a 2×1-dimer row reconstruction and the characteristic alternating dimer rows across a step edge. (b) The Si (100) surface covered with ~0.37 ML of adsorbed PH<sub>x</sub> (x=0,1,2) groups after saturation dosing (approximately 1.5 Langmuir exposure) at room temperature. (c) The surface after an incorporation flash anneal with the brighter regions being islands formed by ejected (substituted) Si atoms. Since the ejected Si should be in one to one correspondence with incorporated P atoms, the ejected Si island coverage represents the incorporated P concentration.<sup>58, 165, 303</sup> (d) The growth front morphology of a nominal 270 °C overgrowth on top of the P-incorporated surface. The overgrowth is in the kinetically rough growth mode due to limited Si adatom migration on the growth front. Though it is difficult to distinguish P atoms on a rough growth front,<sup>304</sup> as shown in the side view schematics (bottom panel), the incorporated P atoms segregate above the original doping plane during the 270 °C overgrowth, which broadens the delta layer.

As described in detail in Chapter 3, Si:P monolayers are fabricated using atomic layer doping.<sup>305, 306, 307</sup> Figure 5.1 illustrates the Si:P 2-D system fabrication process. The samples discussed in this study were fabricated on 1-10 Ohm-cm boron-doped p-type Si chips. First, an atomically flat, clean Si (100)  $2\times1$  reconstructed surface is prepared in an ultrahigh vacuum (UHV) system with a  $6.6\times10^{-9}$  Pascal ( $5\times10^{-11}$  Torr) base pressure, Figure 5.1(a). Detailed preparation procedures have been published elsewhere.<sup>308</sup> Then the surface is dosed (~1.5 Langmuir exposure) with phosphine (PH<sub>3</sub>) gas at room temperature to achieve a saturation surface coverage of ~0.37 ML of phosphorus species [Figure 5.1(b)].<sup>52, 146</sup> PH<sub>3</sub> molecules dissociate into H atoms and

 $PH_x$  (x=0, 1, 2) groups and terminate the Si dangling bonds on the Si (100) surface.<sup>140,</sup> <sup>152</sup> A Rapid Thermal Anneal (RTA) at nominally 384 °C for 2 minutes incorporates the P atoms substitutionally into the silicon lattice within the first atomic layer.<sup>141, 189,</sup> <sup>309</sup> This P incorporation enhances the electrical activation of the dopants and helps minimize segregation during the subsequent Si overgrowth process.<sup>189</sup> The substituted Si atoms in the top layer eject onto the surface and form short 1D Si chains perpendicular to the underlying dimer rows [see Figure 5.1(c)].<sup>58, 303</sup> Some of the Si surface bonds are terminated by H atoms that dissociate from phosphine molecules. The total phosphorus coverage is reduced during the incorporation anneal due to partial PH<sub>x</sub> and H recombination and thermal desorption of molecular PH<sub>3</sub>.<sup>52, 145, 310</sup> This phosphorus incorporation process results in a partially hydrogen-terminated Si (100) surface with approximately one quarter to one third monolayer coverage <sup>52, 146, 152, 189</sup> of incorporated P atoms. The presence of hydrogen atoms on the growth front hinders the Si adatom diffusion and enhances the growth front roughness.<sup>311</sup> Hydrogen removal has been realized as a useful step before Si deposition to improve the epitaxial quality.<sup>137, 303</sup> While it has been shown that the presence of hydrogen released by phosphine dosing does not have a significant impact on the electrical activation of the dopant atoms, the free carrier mobility is likely to be limited by the lower epitaxial quality at the delta layer interface.<sup>189</sup>

The SIMS measured P concentration is  $(2.0 \pm 0.2) \times 10^{14}$ /cm<sup>2</sup> in our delta layer samples after encapsulation overgrowth is consistent with the ejected Si atom coverage. The Si atom density on Si (100) surfaces is  $6.78 \times 10^{14}$ /cm<sup>2</sup>. The SIMS measured P concentration,  $(2.0 \pm 0.2) \times 10^{14}$ /cm<sup>2</sup>, corresponds to  $(0.30 \pm 0.03)$  ML P atom coverage following incorporation anneal on the Si (100) atomic plane. The ~0.37 ML coverage discussed in conjunction with the STM images describes the surface coverage of the adsorbed PH<sub>x</sub> (x = 0,1,2) groups after saturation PH<sub>x</sub> dosing on clean Si (100) surfaces at room temperature.<sup>152, 312</sup> The phosphorus coverage reduces upon the incorporation anneal due to partial PH<sub>x</sub> and H recombination and thermal desorption of molecular PH<sub>3</sub>.<sup>52, 145, 310</sup> A comparison between the 0.37 ML coverage after room-temperature saturation dosing and the total P concentration from SIMS measurement indicates a loss of ~19% of the adsorbed PH<sub>x</sub> species during our incorporation annealing procedures, which is in complete agreement with the literature.<sup>52, 145, 310</sup>

The side-view schematics in Figure 5.1 (d) illustrate P segregation during lowtemperature encapsulation, which results in P moving away from the original doping plane, broadening the confinement of P atoms asymmetrically in the overgrowth direction. It is well known that temperature measurement of silicon in the lowtemperature range (below ~400 °C) and a UHV environment is challenging and is likely to be the largest source of chamber-to-chamber variation in low-temperature epitaxial growth.<sup>155, 197, 304, 313</sup> In this study, sample temperatures are measured using infrared pyrometers with the emissivity value calibrated using Au-Si (363 °C, 97.15/2.85 wt-%) eutectic alloys on Si substrates in a high vacuum environment. The encapsulation overgrowth temperature and locking layer rapid thermal anneal temperature are  $(2.7 \pm 0.2) \times 10^2$  °C and  $(3.8 \pm 0.2) \times 10^2$  °C respectively, where the uncertainties are given as one-sigma standard deviations. We overgrow Si using a Silicon Sublimation Source (SUSI-40) by passing DC current through a high-purity intrinsic Si filament,<sup>213</sup> which is shielded by Si from any hot metal and ceramic components to prevent contamination. The SUSI growth rate is calibrated by using phase shift interferometry, SIMS, cross-section TEM results as well as imaging sub-monolayer deposition using STM. The calibrated SUSI growth rate has been published elsewhere.<sup>213</sup> The SIMS measurement of the P concentration profile uses a Cs<sup>+</sup> primary ion-beam with an acceleration energy of 1 keV or 0.3 keV and an incident angle of 60°. Negative ions of <sup>30</sup>Si+<sup>31</sup>P are measured to obtain phosphorus concentration profiles. The estimated calibration uncertainty for P quantification is nominally  $\pm$  10%.



Figure 5.2. The process flow diagram of the delta layer fabrication procedures illustrating the timing and temperature at each step of the process. The blue box highlights the steps that were systematically varied in this study: the locking layer (LL) overgrowth varies from 0 ML to 16 ML with or without a subsequent LL Rapid Thermal Anneal (RTA) at 380 °C for 14 seconds. The red line represents the thermal profile as a function of time.

An optimized locking layer (LL) deposited at room temperature followed by encapsulation overgrowth at elevated temperatures is critical to simultaneously suppress dopant segregation and maximize crystalline quality at the Si:P 2-D system.<sup>198, 301, 314</sup> The maximum epitaxial thickness, beyond which overgrowth becomes amorphous, decreases rapidly at reduced temperatures due to surface roughening.<sup>155, 156</sup> On Si (100) surfaces, the limiting epitaxial thickness falls below 3nm for room temperature overgrowth, which is insufficient to isolate the 2-D Si:P system from interface states and traps.<sup>195</sup> The essential idea behind LL overgrowth is that dopant segregation can be greatly suppressed during room-temperature LL overgrowth. Before reaching the limiting epitaxial thickness for room-temperature growth, the overgrowth temperature is increased to sustain the epitaxial growth mode.<sup>198, 302, 314</sup> Figure 5.2 illustrates the entire growth process for a Si:P monolayer, locking layer (LL), and encapsulation overgrowth. Before starting the low-temperature encapsulation at 270°C, the sample temperature is maintained for 17 minutes to stabilize the temperature and Si deposition rate.<sup>315</sup> As a result, the surface undergoes a low temperature thermal anneal before each deposition step at elevated temperatures. We will discuss the effect of this pre-deposition anneal on the LL in a later section.

## 5.3 Epitaxial Quality at Locking Layer Interface

(b) (a) 3ML LL @ 0.6ML/min 11 ML LL @ 0.6ML/min 10nm 10nm 3ML LL @ 0.6ML/min Overgrowth @ (2.7  $\pm$  0.2)  $\times$   $10^2~^{\circ}\mathrm{C}$ 11 ML LL @ 0.6ML/min Overgrowth @ (2.7  $\pm$  0.2)  $\times$   $10^2~^{\circ}\mathrm{C}$ 10:11:12:12 8 nm 8 nm 



Figure 5.3 Top panels: STM topography images (+2 V bias on sample, 0.2 nA set-point current) of various LL surfaces before low-temperature encapsulation. Bottom panels: High-resolution cross-section TEM/STEM micrographs near the LL interface regions after LL deposition and low-temperature encapsulation overgrowth. The locking layer growth conditions [thickness, growth rate, and rapid thermal anneal (RTA)] and the subsequent encapsulation overgrowth are marked in the graphs. The red arrows in TEM/STEM images indicate the LL interfaces.

STM micrographs of LL surface morphology before low-temperature encapsulation overgrowth are shown in the top panels in Figure 5.3. Compared with the surfaces after P incorporation [Figure 5.1 (c)], the LL deposition introduces high island/step densities on the starting surface for low-temperature encapsulation overgrowth. The bottom panels in Figure 5.3 show high-resolution cross-section TEM/STEM micrographs near the locking layer interface regions after LL deposition and low-temperature encapsulation overgrowth. The lattice planes align very well across the doping plane, and no distinction in crystalline quality can be observed between the encapsulation overgrowth layers and the substrates, indicating good epitaxial overgrowth quality in the encapsulation layer grown at 270 °C. Thin (3 ML) LL deposition on top of a Si:P monolayer at room temperature is within the kinetically controlled 3-D island growth mode as a result of negligible Si adatom surface migration [Figure 5.3 (a)].<sup>316, 317</sup> We observe no interface contrast at the 3 ML LL plane, which indicates that excellent epitaxial quality can be maintained at a few-ML RT-grown LL interface. Thicker RTgrown LLs lead to smaller 3-D island sizes and higher LL surface roughness [Figure 5.3 (b)], which may affect the epitaxial quality within the LL and alter the initial surface conditions for subsequent low-temperature encapsulation overgrowth.<sup>318</sup> In contrast to Figure 5.3 (a), a greater variation in TEM contrast in the locking layer region above the delta-doped region is observed in Figure 5.3 (b), which is likely caused by a higher concentration of defects and increased strain at the thicker LL interface region. However, the detailed physical mechanism at the thicker LL interface remains to be explained. Annealing at elevated temperatures is known to repair Si lattice defects and interstitial dopant defects and decreases local lattice strain.<sup>319</sup> In Figure 5.3 (c), an RTA at 384 °C for 14 seconds flattens the LL surface and improves the LL crystallinity because of an increase in island size and diffusion of Si atoms to step edges, regardless of the higher growth rate.<sup>308</sup> The surface roughness effect from higher locking layer growth rates are not obvious after LL RTA [Figure 5.3(d)]. However, TEM contrast at the LL interface [Figure 5.3 (c), (d)] remains observable after such a short RTA process.



Figure 5.4 Growth front morphology evolution during epitaxial encapsulation overgrowth, where the overgrowth in the upper panels (a - e) uses a locking layer and the overgrowth in the lower panels (f - j) does not use a locking layer. All the STM images are taken at +2 V sample bias and 0.2 nA set-point current. As the corresponding overgrowth progresses, STM images are acquired as described in each of the panels.



Figure 5.5 Impact of overgrowth conditions on the growth front root mean square (RMS) roughness. (a) summarizes the growth front roughness evolution throughout a complete encapsulation overgrowth process with and without using a locking layer. The STM images shown in Figure 5.4 are a subset of STM images that are used to calculated data points in (a). (b) The locking layer surface roughness evolution (red curve) as a function of the duration of rapid thermal anneal (RTA) at 384 °C. For comparison, we also plot the surface roughness evolution of a saturate-doped surface after incorporation anneal (blue curve) and a locking layer grown on a clean Si (100) surface (green curve) under the same RTA process.

# 5.4 Growth Front Roughness Evolution During Locking Layer Overgrowth

Inserting a LL can alter the initial surface morphology before low-temperature encapsulation overgrowth and affect the resulting overgrowth epitaxial quality.<sup>318</sup> We use STM to monitor the surface morphology evolution during the overgrowth with and

without a LL. Figures 5.4 (a) through (e) show STM images on a flash-annealed RTgrown LL surface deposited at  $(1.8 \pm 0.1)$  ML/min, followed by 270 °C encapsulation growth at the same growth rate. Figures 5.4 (f) through (j) show STM images of 270  $^{\circ}$ C encapsulation growth fronts deposited at  $2.6 \pm 0.12$  ML/min without using a LL. In Figure 5.5 (a), we analyze STM images including those in Figure 5.4 and plot the growth front root mean square (RMS) roughness as a function of overgrowth thickness. Although the LL RTA significantly smooths the LL surface and the 270 °C growth rate is lower on the LL sample than on the no-LL sample, the growth front roughness during the encapsulation overgrowth remains higher on top of the LL than directly on top of the P-incorporated surface. We explore the impact of the LL RTA time on the LL growth front roughness by sequentially heating and imaging the surface morphology on a VT-STM stage. As shown by the red curve in Figure 5.5 (b), the LL surface roughness drops sharply within the first 14 seconds of LL RTA, and then remains stable following additional RTA. Since the surface roughness is a direct indicator of the underlying crystalline quality, this indicates that a 14 seconds RTA is sufficient to fully crystallize the LL. To evaluate the impact of the P incorporated initial surface on the LL roughness, we conducted a similar RTA study on a clean Si surface, shown by the green curve in Figure 5.5 (b). We found that, although the LL growth front roughness before RTA is significantly higher on a P incorporated initial surface than on a clean Si (100) surface, a 14 seconds RTA smooths out the LL roughness of the two cases to a similar level.

### 5.5 Modeling the P-profile with Locking Layers

The depth resolution of the SIMS technique is on the order of several nanometers due to atomic mixing and sputter roughening effects during the profiling process. It has been recognized that some correction to the measured SIMS data, which takes into account distortion effects from the sputtering process, is necessary to obtain the true composition depth profile from the measurement.<sup>320, 321, 322, 323</sup> The measured SIMS profile is a convolution of the real P concentration profile with a sputtering depth resolution function. Quantifying the concentration profile with sub-nanometer depth resolution can only be accomplished by applying an appropriate deconvolution or through profile reconstruction methods.<sup>324</sup> A direct deconvolution is complicated and yields large errors due to measurement signal noise.<sup>320, 321, 325</sup>In this study, we fit a simulated convolution to the measured SIMS results and reconstruct the actual dopant concentration profile using the best-fit parameters. We use a first-order segregation model to simulate the dopant concentration profile. A second order segregation component is unnecessary because the P coverage on the growth front surface of this study is not high enough to form P-P donor pair defects,<sup>147, 150, 326</sup> which is considered the primary cause of the breakdown of the first order model.<sup>327</sup> The depth resolution function is simulated using the Mixing-Roughness-Information-depth (MRI) sputter profiling model<sup>320, 321, 322, 324, 325, 328</sup> to account for sputtering-induced broadening effects during the SIMS measurement.

Dopant segregation during epitaxial Si overgrowth is such that as a new monolayer overgrows on top of the surface, a portion of the P atoms on the initial surface floats onto the new surface due to the lower configuration energy on the surface (segregation energy).<sup>327, 329, 330</sup> This segregation proportion depends critically on overgrowth temperature, overgrowth rate, and the initial surface conditions such as surface step density and surface passivation conditions.<sup>326</sup> In our first order segregation model, the total overgrowth is divided into a LL region and an encapsulation region. A constant incorporation probability  $a_{LL}$  in the LL region ( $a_{CAP}$  in the encapsulation region) is defined as the percentage of the surface phosphorus atoms that are incorporated into the existing layer as another monolayer of Si atoms is overgrown on top of that layer. The segregation model is expressed in the following form,

$$\frac{dN_{surf}}{dx} = a_i N_{surf}$$

Equation 5.1

where  $N_{surf}$  is the phosphorus atom density on the growth front surface; x is overgrowth thickness in units of ML. The segregation length in each region,  $l_i$  is defined as the length over which the coverage reduces to 1/e of the original coverage, where e is the base of the natural logarithm. It follows that  $l_i = 1/a_i$ .



Figure 5.6 Reconstruction of the physical dopant concentration profiles from SIMS measurements. 1 keV and 0.3 keV primary ion beam energies are used for SIMS measurements on the individual LL sample (see Sample LL-T3 in Table 1.). (a) The atomic mixing length (w) depends critically on the primary ion beam energy and is obtained by fitting the trailing edge of the measured SIMS profile M(x). (The fitted w lines are shifted to avoid masking the data points) (b) The SIMS data and the fitted

SIMS results M(x) are plotted as data points and solid curves. We intentionally shift the zero position of the measured SIMS profile peaks for comparison purposes. (c) the reconstructed concentration depth profiles N(x) are plotted in bars. Each bar represents 1ML. (d) Comparison between the reconstructed P concentration profile N(x) and the atom probe tomography (APT) result.

The MRI sputter profiling convolution is governed by three well-defined physical parameters: the atomic mixing length w, the roughness  $\sigma$ , and the information depth  $\lambda$ . The atomic mixing length w depends critically on the sputtering primary ion beam energy and is obtained by fitting the exponential section of the trailing edge of the profile [Figure 5.6 (b)].<sup>331</sup> The roughness,  $\sigma$ , consists of contributions from the surface roughness of the original dosing plane due to steps and kinks, the surface roughness after overgrowth, sputtering induced surface topography, and mixing length straggling.<sup>320, 332</sup> The information depth  $\lambda$  for SIMS is given by the escape depth of the secondary ions. Since the sputtered secondary ions are from the top layer in SIMS measurements with low primary ion beam energies, we take  $\lambda$  to be 1 ML in this work.<sup>320</sup>

First, the physical bulk concentration profile N(x) is obtained by calculating the surface concentration as the overgrowth proceeds layer by layer using the recurrence relation implied by Equation 5.1. We emphasize that N(x) represents the physical bulk concentration assuming an atomically flat single terrace initial dosing plane. Atomic layer steps and kinks could introduce surface roughness on the initial dosing plane. In this study, the initial dosing plane roughness is included in the total roughness parameter,  $\sigma$ , which is to be convoluted with N(x) in the next step. Recently, our group has shown that a large atomically flat single terrace dosing plane can be formed on micropatterned Si (100) in a controlled way,<sup>178</sup> where the reconstructed profile N(x) represents the real physical bulk concentration at local single terrace regions. In the next step, the three convolution functions,  $g_w$ ,  $g_\sigma$ , and  $g_\lambda$ , are sequentially applied to N(x) to obtain the sputter convoluted profile M(x), as shown in Equation 2.  $w_0$  and  $\lambda_0$  are the respective normalization factors of  $g_w$  and  $g_\lambda$  for the conservation of the total number of phosphorus atoms. The total concentrations of P atoms are obtained by integrating the SIMS depth profiles and used as an input normalization factor. Since the segregation length in the low-temperature encapsulation overgrowth layer is much longer than the characteristic sputtering length scales (w, w) $\sigma$ ,  $\lambda$  ), we obtain  $a_{CAP}$  by directly fitting the exponential section of the leading edge of the encapsulation layer profile above the LL. By using the pre-fitted w and  $a_{CAP}$  as inputs, the LL incorporation probability  $(a_{LL})$  and surface roughness  $(\sigma)$  are treated as independent fitting parameters to fit M(x) to the measured SIMS profiles.

$$M(x) = \int_{-\infty}^{+\infty} N(x')g(x - x')dx'$$
$$g(x) = g_w(x) * g_\sigma(x) * g_\lambda(x)$$
$$g_w(x) = \begin{cases} \frac{1}{w_0} \exp\left[\frac{-(x+w)}{w}\right] & x > -w\\ 0 & x \leq -w \end{cases}$$
$$g_\sigma(x) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[\frac{-x^2}{2\sigma^2}\right]$$
$$g_\lambda(x) = \begin{cases} \frac{1}{\lambda_0} \exp\left(\frac{x}{\lambda}\right) & x \leq 0\\ 0 & x > 0 \end{cases}$$
$$166$$
In Figure 5.6, we numerically fit two SIMS profiles measured on the same delta layer sample but with different primary ion beam energies of 1 keV and 0.3 keV. The depth is in units of monolayer (ML) thickness, and the SIMS-measured concentration peak positions are shifted to the zero-depth position for comparison.



Figure 5.7 Correlation between the fitting parameters  $a_{LL}$  and  $\sigma$ . The plot shows the weighted  $\chi^2$  surface in fitting the measured profile on Sample LL-T3 using 1keV primary beam energy, where  $a_{LL}$  and  $\sigma$  are the two fitting parameters. The color scale is in arbitrary units. The dashed circles (from small to large) represent the likelihood contours at 99%, 95%, and 90% confidence intervals. The Pearson correlation coefficient calculated from the covariance matrix between  $a_{LL}$  and  $\sigma$  generally ranges from 0.05 to 0.5 (0.38 in this case), indicating that the incorporation probability in the LL is only weakly correlated with the surface roughness.

When fitting the depth profile, data points are weighted by their Poisson error deviation. As shown in Figure 5.7, the individual fitting parameters  $a_{LL}$  and  $\sigma$  are only weakly correlated with each other (Pearson correlation coefficient < 0.5 between  $a_{LL}$  and  $\sigma$ ). As can be seen from the best-fit parameters in Table 1, a 0.3 keV beam energy results in a smaller atomic mixing length (~5.4 ML) than the 1 keV beam energy does (~7.3 ML). The simulation separates the sputter broadening effects from the actual P-profile and the reconstructed profiles at 1 keV and 0.3 keV show excellent agreement with each other, independent of sputter beam energies. As can be seen from Table 5.1, the segregation incorporation probabilities during 270 °C overgrowth  $(a_{CAP})$  are approximately one order of magnitude lower than that during RT LL overgrowth  $(a_{LL})$ , which accounts for the concentration discontinuity between the LL and subsequent encapsulation overgrowth layer. The best-fit sputtering front roughness ranges approximately from (3 to 4) ML for samples with a LL, which is in good agreement with the observed surface roughness in AFM and cross sectional TEM images. As shown in Figure 5.6 (c), due to the atomic mixing effect, the measured SIMS concentration peaks lie shallower than the reconstructed profile peaks. The dependence of the measured SIMS profile peak positions on the sputter ion beam energy highlights the importance of using profile reconstruction techniques to extract the real depth information of incorporated dopant atoms following atomic device encapsulation.

As shown in Figure 5.6 (d), our reconstructed profile agrees well with the Pulsed Laser Atom Probe Tomography (PLAPT) measurement result. We note that several factors can limit the resolution of the APT technique, such as low counting number noise, the evolution and local variation of tip shape, field-induced surface

migration, crystallographic dependence of evaporation fields between Si and P species, and aberration effects, *etc*.<sup>333, 334, 335, 336</sup>.

Table 5.1 summarizes the detailed LL fabrication parameters (LL thickness, LL growth rate, and LL RTA) of the LL samples investigated in this study as well as the best-fit parameters. Uncertainties are given as one-sigma standard deviations, which include only statistical uncertainties.

<u>Sample</u> <u>Name</u>	LL Thickness (ML) SD $\leq 15\%$	LL Growth Rate (ML/min) SD $\leq 15\%$	LL RTA (384°C 14sec.)	Primary beam energy (keV)	$a_{LL}$ (/ML) SD $\leq 20\%$	$a_{CAP}$ (/ML) SD $\leq 20\%$	$D (cm2 / s)$ $SD \leq 50\%$	$\begin{array}{l} {\sf Mixing} \\ {\sf Length} \\ w({\sf ML}) \\ {\sf SD} \\ \leq 10\% \end{array}$	Roughness $\sigma$ (ML) SD $\leq 20\%$
LL-TO	0		No	1.0		0.018		7.3	4.2
LL-T1	3	0.6	No	1.0	0.18	0.043		7.4	4.1
LL-T2	6	0.6	No	1.0	0.18	0.041		9.5	2.8
LL-T3	11	0.6	No	1.0	0.18	0.032		7.3	3.2
LL-T3	11	0.6	No	0.3	0.19	0.033		5.4	3.2
LL-T4	16	0.6	No	1.0	0.20	0.046		7.7	3.3
LL-R1	11	1.1	No	1.0	0.24	0.016		8.1	2.1
LL-R1- RTA	11	1.1	Yes	1.0	0.23	0.025	$3.2 \times 10^{-17}$	7.7	2.8
LL-R2- RTA	11	1.8	Yes	1.0	0.29	0.046	$1.3 \times 10^{-17}$	7.1	3.0

Table 5.1 Summary of the LL fabrication parameters (LL thickness, LL growth rate, and LL RTA) of the LL samples investigated in this study and the best-fit parameters from the P-profile modeling. Uncertainties are given as one standard deviation (SD), which only include statistical uncertainties.  $a_{LL}$  and  $a_{CAP}$  are dopant segregation incorporation probabilities during the LL overgrowth and encapsulation overgrowth, which represent the probabilities that a dopant on the surface monolayer remains within the same layer and does not segregate onto the upper layer during the subsequent one monolayer overgrowth. *w* is the atomic mixing length in the sputtering process.

Roughness is the sputter milling front roughness that consists of contributions from both the original surface/interface roughness and the sputtering induced surface topography.



## **5.6 Locking Layer Thickness**

Figure 5.8 The effect of locking layer (LL) thickness on delta layer confinement and electrical properties. All locking layers are grown at 0.6 ML/min at room temperature with no LL RTA. (a) The measured and fitted SIMS concentration profiles of LL samples with different LL thicknesses (see Samples LL-T0, LL-T1, LL-T2, LL-T3, and LL-T4 in Table 5.1). (b) The reconstructed P concentration profiles. (c) The delta layer free carrier mobility  $\mu$  (cm<sup>2</sup>/(V s)) and 2D sheet carrier density  $n_s$  (cm<sup>-2</sup>) are

characterized at T=2 K using the van der Pauw technique. (d) The total and activated P locking probability 1 nm and 2 nm from the initial dosing plane as a function of LL thickness.

Figure 5.8 shows the effect of LL thickness on the delta layer confinement and electrical properties. All the LLs in Figure 5.8 are deposited at 0.6 ML/min at room temperature without an LL RTA. Figure 5.8 (b) illustrates the reconstructed P concentration profiles [N(x)] with different LL thicknesses. Without a LL, all the dosed P atoms in the initial dosing plane experience a high segregation probability with the encapsulation overgrowth at 270 °C. Due to the reduced segregation rate in the LL overgrowth, the reduction in the number of P atoms with each additional monolayer of growth is greater in the LL than in the encapsulation layer regardless of the numbers of LL MLs. This reduced segregation rate in the LL is only the result of the incorporation probability  $a_{LL}$  and is independent of the LL overgrowth thickness. At the same LL segregation probability, increasing the LL thickness drives down the remaining number of P atoms on the LL surface that experience a higher segregation probability in the subsequent 270 °C encapsulation overgrowth as expected from Equation 5.1. The reconstructed concentration profiles give approximately the same peak height at the dosing plane independent of LL thicknesses. It is the atomic mixing effect that accounts for the measured concentration peak height variations at different LL thicknesses in Figure 5.8 (a).

Both the free carrier mobility and dopant activation ratio in the delta layers decrease as the LL thickness increases [Figure 5.8 (c)]. This drop in carrier density for samples with thicker LLs may be attributed to the formation of nonincorporated interstitial dopants, inactive dopant-vacancy complexes,<sup>337</sup> and deep level point defects in the lattice<sup>155</sup> as evidenced by the degradation in crystal quality [see Figure 5.3 (a), (b)].<sup>203</sup> In Figure 5.8 (d), we define the total locking probability as the probability for a single phosphorus atom to remain within a certain distance from the initial dosing plane after the entire encapsulation overgrowth process. The activated locking probability is calculated by multiplying the total locking probability with the dopant activation ratio. As expected, the total locking probability reaches its maximum at 11 ML and decreases at 16 ML LL thickness due to the inverse relationship between dopant confinement and activation ratio.



Figure 5.9 The locking layer (LL) rapid thermal anneal (RTA) effect on dopant redistribution in Samples LL-R1 and LL-R1-RTA. (a, b) The measured and fitted SIMS profiles. Sample LL-R1 has an 11ML LL grown at 1.1ML/min at room temperature without RTA. Sample LL-R1-RTA has the same RT-grown LL followed by a 380 °C RTA for 14 seconds before low-temperature encapsulation overgrowth. (c)The reconstructed P concentration profiles before and after low-temperature encapsulation overgrowth in Sample LL-R1 (left two panels) and Sample LL-R1-RTA (right two panels).



Figure 5.10 In Sample LL-R1-RTA, the measured SIMS profile is fitted using three parameters,  $a_{LL}$ , D and  $\sigma$ . (a), (b), and (c) plot the weighted  $\chi^2$  surface between each parameter pairs at the  $\chi^2$  minimum. The color scales are in arbitrary units. The dashed circles (from small to large) represent the likelihood contours at 99%, 95%, and 90% confidence intervals. The Pearson correlation coefficients at the  $\chi^2$  minimum are 0.89 between D and  $a_{LL}$ , 0.06 between  $\sigma$  and  $a_{LL}$ , and -0.22 between D and  $\sigma$ . There exists a relatively strong correlation between the LL incorporation probability  $a_{LL}$  and LL RTA diffusivity D. (Note, an absolute value below 0.8 can be considered as a weak correlation).

## **5.7 Locking Layer Rapid Thermal Anneal**

Keizer and coworkers have found that a finely tuned LL rapid thermal anneal (RTA) can effectively restore the active carrier density while maintaining ultra-sharp dopant profiles.<sup>20, 56</sup> They observed that application of an LL RTA slightly reduces the P peak height and raises the segregation tail of the encapsulation layer. We observe similar behavior in SIMS measured results when applying a short RTA (380 °C for 14 seconds.) after RT LL overgrowth [Figure 5.9 (a), (b)]. This RTA induced dopant

redistribution can be quantified by adding a diffusion component into our simulation algorithm to account for the P diffusion towards the surface during LL RTA (Equation 5.3), where the segregation profile after the RT LL deposition is used as the initial condition for the diffusion simulation. The diffusion equation is expressed as,

$$\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2}$$

#### Equation 5.3

where *N* is the phosphorus atom density in each monolayer, *t* is the flash anneal time in seconds, *x* is depth in units of ML, D is the diffusivity in units of ML<sup>2</sup> · s<sup>-1</sup> and is treated as an independent fitting parameter. Since the RTA temperature (380 °C) is well below the thermal desorption temperature of incorporated phosphorus atoms on Si (100) surfaces ( $\approx 600$  °C),<sup>52, 145</sup> we treat the phosphorus accumulation on a LL surface during a LL RTA as a diffusion sink where the diffusing P atoms remain trapped on the LL surface during an RTA. Dopant diffusion from the surface into the overgrowth silicon is negligible within the low temperature range of this study because this process must overcome not only the diffusion barrier but also the segregation energy at the surface. Only the phosphorus atoms in the LL surface monolayer participate in the segregation process of the subsequent encapsulation overgrowth at 270 °C.

Extrapolations from previous diffusivity studies show a more than five orders of magnitude difference between the diffusivity of P in Si at our LL RTA temperature (380 °C) and encapsulation temperature (270 °C).<sup>338, 339, 340, 341, 342</sup> Therefore, we assume the P diffusion during the 270 °C thermal soak and encapsulation overgrowth is negligibly small and is not included in our model.<sup>301 150, 195</sup> Dopant diffusion into the

substrate Si is also neglected at low temperatures in this study due to the low number of defects present in the Si substrate after flash annealing at 1200 °C.<sup>340, 343, 344, 345</sup>

We apply LL RTA to two of the samples in this study, Sample LL-R1-RTA and Sample LL-R2-RTA, where the LLs of the same thickness (11 ML) are grown at 1.1 ML/min and 1.8 ML/min respectively. We obtain the best-fit LL diffusivity to be about  $3.2 \times 10^{-17} \text{ cm}^2/\text{s}$  for Sample LL-R1-RTA and about  $1.3 \times 10^{-17} \text{ cm}^2/\text{s}$  for Sample LL-R2-RTA (see Table 5.1). As shown in Figure 5.10, among the three free fitting parameter  $(a_{LL}, \sigma, \text{ and } D)$ , a relatively strong correlation exists between  $a_{LL}$  and D (Pearson correlation coefficients  $\approx -0.2$  between D and  $\sigma$ , and  $\approx 0.9$  between D and  $a_{LL}$ ). However, the best-fit  $a_{LL}$  value in Sample LL-R1-RTA shows good agreement with the best-fit  $a_{LL}$  value in Sample LL-R1 where the RT-grown LL is deposited at the same deposition rate and thickness but without an LL RTA. This indicates that the simulation can distinguish the diffusion effect from the segregation effect in the SIMS profiles. As illustrated in the first and third panels of Figure 5.9 (c), before low temperature encapsulation overgrowth, the LL RTA induces dopant atom diffusion within the LL, which reduces dopant density at the initial dosing plane and drives some subsurface dopant atoms out of the LL to the surface. This dopant accumulation on the LL surface results in slightly higher dopant concentration in the subsequent encapsulation overgrowth layer because the subsequent segregation starts with a higher initial surface coverage [second and fourth panels in Figure 5.9 (c)].

### **5.8 Locking Layer Growth Rate**



Figure 5.11 The fitted P segregation length  $(l_{LL})$  of room-temperature grown locking layer at different growth rates.



Figure 5.12 The effect of locking layer (LL) growth rate on delta layer confinement and electrical properties. (a, b) Measured and fitted SIMS concentration profiles of samples with different LL growth rate. Samples LL-T3 and LL-R1 in (a) do not have an LL RTA. Samples LL-R1-RTA and LL-R2 RTA in (b) have an LL RTA. (c) The reconstructed P concentration profiles. (d) The total and activated P locking probability

within 1 nm and 2 nm from the initial dosing plane as a function of LL thickness. (e) The delta layer free carrier mobility  $\mu$  [cm<sup>2</sup>/(V s)] and 2D sheet carrier density  $n_s$  (cm<sup>-2</sup>) are characterized at T=2 K using the van der Pauw technique.

Our fitting results show that the LL segregation length decreases with increasing LL growth rate at room temperature. (Figure 5.11) The segregation length values agree very well with the values reported from previous STM and Auger studies at similar growth rates and temperatures.<sup>196</sup> Physically, this segregation length dependence on growth rate arises from the time allowed for a dopant on the growth front to exchange its lattice position with newly deposited Si atoms before incorporation.<sup>326,346</sup> Increasing the LL growth rate reduces the time allowed for segregation exchange during LL overgrowth, and therefore increases the incorporation probability within the LL (Table 5.1) and dopant confinement.

As can be seen in Figure 5.12 (a, b, c), increasing LL growth rate improves dopant confinement in situations with and without an LL RTA. Increasing the LL growth rate from 0.6 ML/min (Sample LL-T3) to 1.1 ML/min (Sample LL-R1) increased the P density at the dosing plane from  $2.5 \times 10^{21}$ /cm<sup>3</sup> to  $3.5 \times 10^{21}$ /cm<sup>3</sup>. At 1.8 ML/min LL growth rate in Sample LL-R2-RTA, 95% of the P atoms can be confined within a 1 nm thick layer [Figure 5.12 (d)]. However, as can be seen from Figure 5.12 (e), which presents both carrier concentration for the four samples as well as Hall mobility, increasing the LL growth rate results in decreased dopant activation ratio in samples with and without a 14 sec. LL RTA at 380 °C. While the activated P locking probability decreases, the total P locking probability increases with increased LL growth rate.

Even though P is better confined through either increasing the LL thickness or increasing the LL growth rate, we emphasize the advantages of increasing LL growth rate to improve P confinement. As can be seen in Figure 5.8 (b), increasing the LL thickness merely extends the P concentration profile within the LL further into the exponential tail while the exponent remains unchanged. While a thicker locking layer can effectively reduce the remaining P coverage on the LL surface that further segregates during the subsequent encapsulation overgrowth at elevated temperature, it has no effect on the P concentration peak height within the LL. On the other hand, increasing the LL growth rate effectively increases the exponent of P profiles within the LL [Figure 5.12 (c)], which improves both the sharpness and concentration peak height of the P profile.

## **5.9 Discussion**

Dopant confinement and electrical activation are highly sensitive to LL fabrication processes at the ML scale. Due to the low segregation probability during LL overgrowth at room temperature, increasing the LL thickness improves delta layer confinement by suppressing the number of dopant atoms that further segregate during the subsequent encapsulation overgrowth at elevated temperature. However, crystalline quality at the LL interface degrades with increased LL thickness which results in lower P activation ratios and free carrier mobilities. Therefore, we identify optimal LL thicknesses that balance dopant confinement and activation at a fixed LL growth rate. In this study, we found such an optimal LL thickness to be approximately 11 ML when depositing the LL at 0.6 ML/min, where 90% of P atoms are confined within 2 nm of the original dosing plane with an activation ratio of 88%. P density at the original dosing plane is independent of LL thickness, and we estimate a P peak concentration of about  $2.5 \times 10^{21}$ /cm<sup>3</sup> can be achieved at a 0.6 ML/min LL growth rate.

RTA after LL overgrowth improves both the dopant activation ratio and free carrier mobility. This increase in carrier mobility after an LL RTA occurs because increased Coulomb scattering from additional ionized impurities is offset by decreased point defect scattering due to improved crystal quality, which results in a net increase in the carrier mobility. However, the LL RTA broadens the P distribution within the LL and accumulates P on the LL surface which increases the number of P atoms that segregate during encapsulation layer overgrowth. We note that our calculated P diffusivity within RT-grown LLs at 380 °C is about  $3.2 \times 10^{-17} \text{ cm}^2/\text{s}$ , which is approximately three orders of magnitude higher than the corresponding P diffusivity extracted from previous studies within bulk Si at high P concentration (~ $1.3 \times$  $10^{-20}$  cm<sup>2</sup>/s).<sup>341, 347</sup> This is likely due to the higher concentration of structural or charge defect complexes within the RT-grown LL and the non-equilibrium local point defect concentration near the highly doped delta layer region and the relatively rough LL surface. <sup>299, 339, 347, 348, 349</sup> Elemental SIMS analysis shows a high concentration of atomic point defects due to oxygen, hydrogen and other contaminants that are incorporated into the overgrown locking layers which do not have a significant effect on epitaxy but likely enhance dopant diffusion.<sup>345, 350</sup> We are not aware of any literature values of P diffusivity in the low temperature range of this study and with similar Si

LL configurations. Further studies are needed to characterize the detailed physical mechanism(s) of the observed high P diffusivity within RT-grown LLs on Si surfaces with high P coverage.<sup>349</sup>

Increasing the LL growth rate decreases the LL segregation length and improves dopant confinement more efficiently than merely increasing LL thickness in the sense that both the sharpness and the peak height of the P concentration profile can be improved within the LL. However, higher LL growth rates affect the local crystal quality at the LL interface and compromise dopant activation.<sup>203</sup> The drop in activated P locking probability [Figure 5.12 (e)] with higher LL growth rates highlights the side effect of improving P confinement by increasing the LL growth rate, which can be mitigated by a short LL RTA. Increasing the LL growth rate from 0.6 ML/min to 1.1 ML/min results in a drop in P activation ratio from 88% to 61% while the mobility increases from 75  $\text{cm}^2/\text{Vs}$  to 83  $\text{cm}^2/\text{Vs}$ . The competing response of activation ratio and free carrier mobility to increased LL growth rate may suggest that the mobility is primarily limited by Coulomb scattering from ionized impurities for room-temperature grown LL without a LL RTA. On the other hand, for LL samples with a LL RTA, an increased LL growth rate results in a reduction of both the P activation ratio and free carrier mobility. Further study is necessary to fully explore the electronic transport dependence on the LL overgrowth parameters. In addition, in order to fully explain the detailed physical mechanisms of P segregation and diffusion in this study, it might be necessary to extend our simple model with additional complexities, such as the growth front roughness,<sup>156</sup> step density<sup>326</sup> evolution, vacuum contamination and autodosing,<sup>302, 350, 351</sup> etc., which are beyond the scope of this study.

## 5.10 Weak localization thickness measurement of Si:P monolayers

Weak localization analysis using a parallel magnetic field has been proposed as an extremely sensitive probe of 2-D system thickness with sub-monolayer thickness resolution.<sup>352, 353, 354, 355, 356</sup> Unlike the SIMS and APT approaches that measure the depth concentration profile of the dopant atoms, the weak localization approach measures the thickness of the region where free charge carriers actually propagate in a low dimensional structure. In this sense, the weak localization measured thickness can be understood as the "electrical thickness" of the overall conducting channels. In Si:P monolayers, because the ionized cores of P dopants provide the 2-D confinement potential for conducting electrons, the electrical thickness and dopant distribution thickness are intrinsically related. More importantly, the measurement of electrical thickness serves to bridge the gap between the dopant confinement and the transport properties of the confined electrical system.

Following the weak localization analysis developed by Dr. Joseph A. Hagmann and Dr. Curt Richter within our team,<sup>357</sup> we examine the impact of atomic-scale delta layer confinement on the weak localization signals in both a perpendicular and a parallel magnetic field and extract the delta-layer thickness information from weak localization analysis. We demonstrate the first weak localization thickness measurement in Si:P monolayers in the sub-nanometer thickness regime and compare the measured weak localization thickness with the quantified dopant distribution thickness from SIMS profile reconstruction. The good agreement between the measured thickness from the SIMS reconstruction and weak localization methods verifies the weak localization method as an alternative way to quantify atomic-scale dopant movements in Si:P monolayers. Also, the non-destructive and high throughput nature of weak localization-based measurements compensate some of the major drawbacks of SIMS measurement.

### **5.10.1 Weak Localization Quantum Corrections**

At low enough temperatures, the electrons in an electron gas system can maintain phase coherence over many scattering events. In the absence of a magnetic field, the constructive interference of an electron traveling along the same path in opposite directions (time-reversal symmetry in a self-intersecting trajectory) enhances the probability of the electron to be backscattered coherently to its original location. This phenomenon is called weak localization (WL), which suppresses the conductivity in a low dimensional system. The WL correction to the classical diffusive magneto-transport for disordered 2-D systems is given by,<sup>358, 359</sup>

$$\delta\sigma_{WL}(B=0) = \frac{e^2}{\pi h} ln \frac{\tau}{\tau_{\varphi}} = p \frac{e^2}{\pi h} ln \frac{T}{T_o}$$

#### Equation 5.4

where  $\tau_{\varphi} \sim T^{-p}$  is the phase relaxation time (also called dephasing time, which is the mean time over which the wave function loses phase coherence), and  $\tau$  is the mean free time.  $\tau_{\varphi}$  characterizes the inelastic scattering process and  $\tau$  characterizes the elastic scattering process. Within the diffuse transport scenario,  $\tau_{\varphi} \gg \tau$  and  $\delta \sigma_{WL} < 0$ . The

temperature dependence of  $\tau_{\varphi}$  is characterized by an exponent factor p that is related to both the system's dimensionality and scattering mechanisms.<sup>360</sup>



Figure 5.14 Graphical representation of the weak localization (WL) quantum corrections to the classical Drude conductivity in 2-D systems. Two trajectories in a self-intersecting loop interfere constructively and decrease the conductance. Magnetic flux through a loop, from either a perpendicular magnetic field (a) or a parallel magnetic field (b), breaks the time-reversal symmetry and causes the phase coherence to decay. (c) An example of the measured WL correction to classical conductivity as a function of perpendicular and parallel magnetic field. For the perpendicular magnetic field, the average area (S) of phase coherent loops is on the order of the phase coherence length scale  $(S \sim l_{\varphi}^2)$ . For the parallel magnetic field, however, because the 2-D layer thickness is much smaller than  $l_{\varphi}$ , the magnetic flux through a phase coherent loop is limited by the 2-D layer thickness (t) with an average loop size  $l_{\varphi}t$ . (The plots in this figure are taken from samples fabricated by Xiqiao Wang and measured by Joseph Hagmann.<sup>361</sup>)

A magnetic field applied perpendicular to the conduction plane introduces an *Aharanov-Bohm* phase difference,  $\Delta \phi$ , between the forward and reversed trajectories that breaks the phase coherence.

$$\Delta \phi = 2\pi \frac{BS}{h/2e} = \frac{2S}{l_m^2}$$
$$l_m = \sqrt{\frac{\hbar}{eB}} = \frac{25.7}{\sqrt{B}} nm T^{-\frac{1}{2}}$$

#### **Equations 5.5**

where  $l_m$  is the magnetic length that defines the radius of a circle that encloses a magnetic flux quantum in the magnetic field *B*, and *S* is the loop area projected in the magnetic field direction. In practice, the WL correction,  $\Delta \sigma_{WL}$ , to the classical 2-D conductivity can be extracted from,

$$\Delta \sigma_{WL}(B) = \delta \sigma_{WL}(B) - \delta \sigma_{WL}(0) = \sigma_{xx}(B) - \sigma_{xx}(0) \approx \frac{1}{\rho_{xx}(B)} - \frac{1}{\rho_{xx}(0)}$$
Equation 5.6

where the last equality is an approximation in the weak field regime where  $\mu B \ll 1$ , which is suitable for the WL analysis on saturation doped Si:P  $\delta$ -layer in this thesis. For a 2-D system with weak spin and spin-orbit scattering,  $\Delta \sigma_{WL}$  (as a function of the perpendicular magnetic field) can be described by Hikami-Larkin-Nagaoka (HLN) model.<sup>362</sup> Phase coherent properties, such as the phase relaxation time  $\tau_{\varphi}$  and the phase coherence length  $l_{\varphi} = \sqrt{D\tau_{\varphi}}$ , of a 2-D system can be extracted by analyzing WL measurement results using the HLN model. The application of the HLN model requires the conduction to be in a diffusive regime where the electron's mean free path l is much shorter than the magnetic length  $l_m$ . The HLN model is particularly suitable for studying the Si:P  $\delta$ -doped layers where l is only a few nanometers and the trajectory bending due to cyclotron effects is negligible so that the electron motion can be seen as diffusive with respect to the magnetic field. The HLN equation can be expressed as,

$$\Delta \sigma_{WL}(B_{\perp}) = \alpha \frac{e^2}{\pi \hbar} \left[ \Psi \left( \frac{1}{2} + \frac{B_{\varphi}}{B_{\perp}} \right) - \Psi \left( \frac{1}{2} + \frac{B_o}{B_{\perp}} \right) + \ln \frac{B_o}{B_{\varphi}} \right]$$
$$B_o = \frac{\hbar}{4De\tau}$$
$$B_{\varphi} = \frac{\hbar}{4De\tau_{\varphi}}$$

#### Equation 5.7

where  $\Psi$  is the digamma function,  $B_o$  and  $B_{\varphi}$  are characteristic magnetic fields associated with the mean free time ( $\tau$ ) and phase relaxation time ( $\tau_{\varphi}$ ) respectively, Dis a diffusion constant defined as  $D = \frac{1}{2}v_F^2\tau$  with  $v_F$  being the Fermi velocity. The prefactor  $\alpha$  in the HLN equation characterizes the sub-band occupancies:  $\alpha = 1$  if the conduction electrons only occupy a single sub-band and  $\alpha \neq 1$  if the conduction electrons occupy multiple sub-bands from a single valley or multiple valleys. <sup>192, 363</sup> The Fermi velocity in a single sub-band 2DEG system can be expressed as,

$$v_F = \frac{\hbar k_F}{m^*} = \frac{\hbar}{m^*} \sqrt{\frac{4\pi n_s}{g_s g_v}}$$

#### Equation 5.8

we assume the conductivity in our Si:P  $\delta$ -layers is dominated by electrons from the lowest energy sub-bands, and choose the effective mass to be,  $m^* = 0.19m_e$ . This choice of effective mass is supported by angle-resolved photoemission spectroscopy measurements and density functional theory calculations of similar Si:P  $\delta$ -doped systems.<sup>364</sup> We assume the spin and valley degeneracy in the Fermi velocity calculation to be  $g_s = 2$ , and  $g_v = 2$  in this study.

### 5.10.2 Weak Localization Thickness Measurements

In practice, all 2-D electron gas systems have finite confinement potential, which allows electron scattering trajectories to deviate from an ideal 2-D plane. The transport is typically considered to fall into the 2-D regime if the relevant transport length scales (mean free path l in a ballistic system or the phase coherence length  $l_{\varphi}$  in a disordered system) are significantly greater than the finite thickness t. Because of the finite cross section of the out-of-plane scattering loops in the parallel field direction, applying a parallel magnetic field will break the time-reversal symmetry of self-intersecting loops that are out-of-plane, which reduces localization in a similar manner as applying a perpendicular magnetic field. WL analysis using a parallel magnetic field has been shown to be an extremely sensitive probe of thickness, t, of a 2-D system with a submonolayer thickness resolution.<sup>352, 353, 354</sup> The thickness measured by WL analysis can be interpreted as the "electrical thickness" of transport channels of free charge carriers. The weak localization thickness analysis in this section follows the discussions of Sullivan *et al.*<sup>354</sup> and Hagmann *et al.*<sup>357</sup>

In a perpendicular magnetic field, in-plane self-intersecting loops dominate magneto conductance effects. In a parallel magnetic field, however, only the out-of-plane self-intersecting loops are subject to weak localization magneto transport corrections. For the out-of-plane intersecting loops, additional scattering at the upper and lower boundaries of 2-D confinement enhances the dephasing rate. Therefore, for the contribution to the WL correction from the out-of-plane intersecting loops, the expression is modified as  $\frac{\tau}{\tau_{\varphi}} \rightarrow \frac{\tau}{\tau_{\varphi}} + \frac{\tau}{\tau_{\parallel}}$ , such that,

$$\delta \sigma_{WL}(B_{\parallel}) = \frac{e^2}{\pi h} ln \left( \frac{\tau}{\tau_{\varphi}} + \frac{\tau}{\tau_{\parallel}} \right)$$

#### Equation 5.9

where the expression for the dephasing rate enhancement,  $\frac{\tau}{\tau_{\parallel}}$ , is a function of  $B_{\parallel}$ , and is determined by the relative length scales among the coherent length  $l_{\varphi}$ , mean free path l, and the correlation length  $l_c$  of the thickness fluctuations in a  $\delta$ -layer.

In an actual Si:P  $\delta$ -doped layer, due to the statistical nature of phosphorus segregation during the overgrowth, which is the dominant mechanism of Si:P  $\delta$ -layer broadening, the P distribution in the z-direction fluctuates across the doping plane. The correlation length scale is a characterization of the thickness fluctuations in this dimensionally confined system. Both the electron density distribution and the P distribution contribute to the weak localization thickness, t, of the  $\delta$ -layers. The relative length scales between the thickness fluctuation correlation length  $l_c$  and the phase coherence length  $l_{\varphi}$  capture the geometric impact of the delta layer thickness fluctuations on the weak localization correction to conductivity.<sup>353</sup> In Si:P  $\delta$ -doped layers, it is reasonable to estimate  $l_c$  as the mean donor in-plane spacing  $1/\sqrt{n}$  (~1 nm for our saturate-doped delta layer).<sup>354</sup> At temperature T = 4 K in a saturation-doped Si:P  $\delta$ -layer,  $l \approx (4 \text{ to } 8) nm$  and  $l_{\varphi} \approx (50 \text{ to } 100) nm$ . This corresponds to the situation  $l_c \ll l \ll l_{\varphi}$ . The dephasing rate enhancement can be expressed as,<sup>353</sup>

$$\frac{\tau}{\tau_{\parallel}} \cong \sqrt{4\pi} \frac{e^2}{\hbar^2} \frac{l_c}{l} l_{\varphi}^2 t^2 B_{\parallel}^2$$

Equation 5.10

Therefore, in a parallel magnetic field  $B_{\parallel}$ , the change in conductance becomes,<sup>365</sup>

$$\Delta\sigma(B_{\parallel}) = \delta\sigma(B_{\parallel}) - \delta\sigma(0) = \left(\frac{e^2}{2\pi^2\hbar}\right)\ln(1 + \sqrt{4\pi}\frac{e^2}{\hbar^2}\frac{l_c}{l}l_{\varphi}^2t^2B_{\parallel}^2)$$

#### Equation 5.11

where the WL thickness t can be treated as a fitting parameter, following Hagmann et al.<sup>357</sup>



Figure 5.15 The SIMS measured and reconstructed dopant distribution profiles of the two Si:P delta-layer samples for the weak localization thickness study. Sample WLB is fabricated with a 15 ML locking layer grown at 1.8 ML/min. Sample WLC is fabricated without a locking layer. (a) The measured (data points) and fitted (lines) SIMS profiles. (b) (c) The reconstructed P distribution profile in a linear scale plot (b) and a logarithmic scale plot (c).



Figure 5.16 Suppression of weak localization effects with magnetic fields perpendicular and parallel to the sample plane.

	n <sub>2D</sub> (cm <sup>-2</sup> )	μ (cm²V <sup>-1</sup> s <sup>-1</sup> )	Mean free path, I (nm)	Phase coherence length, l <sub>\$</sub> (nm)	WL-measured thickness, Δ (nm)	Dopant distribution thickness (nm)
No locking layer	1.9 × 10 <sup>14</sup>	97	16	150 ± 0.5	24.2 ± 0.5	~30
locking layer	7.2 × 10 <sup>13</sup>	43	4.3	53 ± 0.3	0.85 ± 0.04	~2

Table 5.2 Low-temperature (2K) electrical measurement results of the two delta-layer samples for the weak localization thickness study. The free carrier density  $n_{2D}$ , mobility  $\mu$ , and mean free path l are extracted from Hall measurement analysis. The phase coherence length  $l_{\varphi}$  and weak localization thickness  $\Delta$  are extracted from weak localization analysis from perpendicular and parallel magnetic field, respectively. The uncertainties in  $l_{\varphi}$  and  $\Delta$  are dominated by fitting errors and are given by one standard deviation. The dopant distribution thicknesses are estimated from SIMS reconstructed dopant depth concentration profiles at free carrier degenerate concentration levels of  $\sim 3 \times 10^{18}/\text{cm}^3$ .

We examined the weak localization-measured thickness on two Si:P samples of drastically different levels of dopant confinement: one with a locking layer (Sample WLB) and the other without a locking layer (Sample WLC). The SIMS-measured and reconstructed P depth concentration profiles are shown in Figure 5.15. With the intention of probing the limit of dopant confinement of our process, we fabricated the LL sample at a LL growth rate of 1.8 ML/min and an LL thickness of 15 ML. The

sample with no LL exhibits a significantly broadened dopant distribution profile due to dopant segregation.

We summarize the low-temperature weak localization measurement on the LL sample and no LL sample in Figure 5.16, where both the perpendicular and parallel magnetic field is examined. Table 5.2 summarizes the detailed electrical characterizations of the two samples. As expected from previous studies, the LL sample exhibits significantly lower free carrier density, mobility, mean-free-path and phase coherence length, as compared with the no LL sample. We estimate the dopant distribution thickness using SIMS reconstructed profiles at the free carrier degenerate level of about  $3 \times 10^{18}$ /cm<sup>3</sup>, see Figure 5.15 (c). However, considering the complications regarding dopant activation, Bohr radius of dopant atoms, etc., more elaborate estimates of the dopant distribution thickness are required for better comparison with the measured electrical thickness and will be presented in the following section. Nevertheless, the weak localization measured electrical thicknesses of the two samples agree well with the dopant confinement thicknesses estimated from the SIMS measurement, demonstrating the applicability of the weak localization approach in characterizing the thickness of Si:P monolayers.

#### **5.10.3 Dephasing Mechanisms**

In addition to an external magnetic field, the major dephasing mechanisms in solids are electron-phonon, electron-electron, and spin-flip interactions.<sup>360</sup> The dominant

dephasing mechanisms in a system can usually be extracted from the temperature dependence of the phase coherence length  $l_{\varphi}$  using the power law,

$$l_{\omega} \propto T^{-p}$$

#### Equation 5.12

At high temperatures (T > 100 K), electron-phonon interactions dominate the dephasing. At low temperatures, the dephasing in a system with high carrier densities is dominated by electron-electron interactions, which is the case of our saturate-doped Si:P  $\delta$ -layers that are measured at 4 K.



Figure 5.17 The temperature dependence of the phase coherence length in the LL sample and no LL sample. (a) The LL and no LL samples exhibit an electron-electron dephasing mechanism for a 2-D and 3-D system respectively. The temperature

dependent weak localization measurement results are shown in (b) for the no LL sample and in (c) for the LL sample.

Electron-electron interactions are the dominant dephasing mechanism in the two Si:P samples in this study due to the high free carrier concentration and low measurement temperature. To probe the impact of a LL on the electrical dimensionality of Si:P systems, we examine the temperature dependence of the phase coherence length. Figure 5.17 shows the weak localization measurement results at different temperatures and the plot of  $l_{\varphi}$  as a function of temperature for both samples. The  $l_{\varphi}$  in the locking layer sample shows a power law temperature dependence of approximately  $T^{-0.51\pm0.01}$ , which is close to the expected temperature dependence  $T^{-0.5}$  in a 2-D disordered conducting system due to electron-electron interactions.<sup>359</sup> This is in good agreement with the measured electrical thickness of the LL sample (~1 nm) that is much shorter than the phase coherence length  $l_{\varphi} \approx 53$  nm. The  $l_{\varphi}$  in the no locking layer sample shows a power law temperature dependence of approximately  $T^{-0.71\pm0.02}$ , which is close to the expected temperature dependence  $T^{-0.75}$  in a 3-D disordered conducting system due to large energy transfer electron-electron interactions. <sup>359</sup> This indicates that the confinement in the no LL sample is not purely 2-D. However, since the measured electrical thickness (~24 nm) is still small compared with  $l_{\varphi}$  (~150 nm), the use of 2-D weak localization and 2-D density of states in our analysis remains justified.

## **5.11 Chapter Summary**

To summarize, we have developed a robust quantification method using roomtemperature grown locking layers (LL) and segregation/diffusion and sputter profiling simulations to monitor and control, at the atomic scale, unintentional dopant movement and lattice defect formation during the Si:P monolayer fabrication. By combining SIMS, TEM, STM, APT, and low-temperature magneto-transport measurements, we have shown that increasing LL thickness decreases both the dopant activation ratio and carrier mobility. Specific LL growth rates correspond to optimal LL thicknesses that balance the tradeoff between dopant confinement and activation. LL RTA restores LL crystalline quality but induces dopant diffusion and surface accumulation at the LLs. The dopant segregation length can be suppressed below one Si lattice constant by increasing LL growth rate above 1.8 ML/min. We compare the effects of increasing LL growth rate and increasing LL thickness on delta layer quality, emphasizing the advantage of the former in improving P confinement in both the profile sharpness and peak concentration heights. We demonstrate that high LL growth rates in combination with a low-temperature LL RTA can create exceptionally sharp dopant confinement while maintaining good electrical quality within Si:P monolayers. The new model developed in this study provides valuable insight into the interplay among dopant movement, activation, and surface roughening at the mono-atomic layer scale. By comparing the SIMS reconstructed dopant profile distribution with the electrically measured weak localization thickness, we have demonstrated the applicability of weak localization analysis as a non-destructive quantum metrology method in determining the conducting layer thickness in the Si:P monolayers fabricated using the locking layer technique. By analyzing the temperature-dependent dephasing behavior in the fabricated Si:P monolayers, we have validated the improved 2-D electronic confinement quality in an LL sample as compared to a no LL sample. The locking layer fabrication and quantification methods demonstrated in this study provide unique tools to study atomic dopant movement and the local crystalline environment in Si:P monolayers and their effect on atomic scale electronics for future semiconductor and solid-state quantum devices.

# **Chapter 6: Atomic-scale Control of Tunnel Coupling**

# **6.1 Introduction**

Atomically precise silicon-phosphorus (Si:P) quantum systems are actively being pursued to realize universal quantum computation<sup>66</sup> and analog quantum simulation.<sup>366</sup> Persistent efforts in atomically precise fabrication using scanning tunneling microscopes (STM) have enabled quantum state initialization and readout using deterministically placed phosphorus donor qubits.<sup>59, 367, 368</sup> Atomically precise control of the tunneling coupling strength is not only critical to successful spin-exchange operations in quantum computing<sup>46, 369</sup> but also essential in tuning the correlation phases in Fermi-Hubbard simulators.<sup>366</sup> STM-patterned tunnel junctions with atomically abrupt Si:P nanogaps were first demonstrated by the Simmons' group.<sup>370</sup> Although STM-patterned tunnel junctions lack the degree of tunability of top-gate defined tunnel barriers in conventional semiconductor heterostructures,<sup>371</sup> it was shown by Pok<sup>372</sup> and Fuhrer et al.<sup>373</sup> that engineering the nanogap geometry, such as lead width and separation, is a method to directly control the tunnel barriers and the tunnel rates in STM-patterned devices: even a  $\sim 1$  nm difference in the tunnel gap distance can drastically affect the tunnel coupling and transport properties in atomically precise Si:P devices. <sup>374</sup> Although tunnel coupling of individual atomic scale STM-patterned Si:P devices has been demonstrated,<sup>61, 62, 208, 292, 373</sup> due to critical challenges in preventing unintentional dopant movement at the atomic scale during encapsulation overgrowth of STM-patterned Si:P devices, and achieving ultra-clean and atomically abrupt hydrogen lithography, systematic and reliable control of tunnel coupling at the atomicscale has not been demonstrated to date.

In this section, we overcome these challenges by uniquely combining atomically abrupt hydrogen lithography<sup>48, 375</sup> with recent progress in low-temperature epitaxial overgrowth using a locking-layer technique,<sup>198, 357, 376</sup> allowing the first demonstration of the exponential scaling of the tunneling resistance on the tunnel gap distance at the atomic limit in a systematic and reproducible manner. We define the tunnel gaps with atomically abrupt edges using ultra-clean hydrogen lithography while utilizing the Si (100) surface reconstruction lattice to quantify the tunnel gap distances with atomic accuracy. We suppress unintentional dopant movement at the atomic scale using an optimized, room-temperature grown locking layer, which not only locks the dopant position within lithographically defined regions during encapsulation overgrowth but also improves device reproducibility by minimizing the impact of overgrowth temperature variations on dopant confinement profiles.<sup>376</sup> Furthermore, our recent development of a high-yield, low-temperature method for forming ohmic contact to buried atomic devices enables robust electrical characterization of STMpatterned devices with minimum thermal impact on dopant confinement.<sup>377</sup> With improved capabilities to define and maintain atomically abrupt dopant confinement in silicon, we fabricated a series of STM-patterned Si:P single electron transistors (SETs), where we systematically vary the tunnel junction gap distance with atomic precision, and have used them to demonstrate and explore atomic-scale control of the tunnel coupling. Instead of geometrically simpler single tunnel junctions, we chose SETs in this study because the observation of the Coulomb blockade signature is a direct indication that conductance is through the STM-patterned tunnel junctions. SETs are also essential building blocks for silicon-based quantum information (QI) processing, such as qubit state initialization and readout.<sup>36</sup>

In this chapter, we first briefly review the importance of tunnel coupling in universal quantum computing and analog quantum simulators to motivate the development of the atomic-scale control of tunneling coupling. Then, we present an experimental demonstration of atomic-scale control of tunnel resistances in a series of carefully fabricated Si:P single electron transistors in the metallic regime, where we have demonstrated, for the first time, the exponential scaling of tunneling coupling down to the atomic limit in doped nanostructures in silicon. As we scale the SET island size and electrode width down to the atomic scale and present resonant tunneling spectroscopy analysis through few-donor quantum dots and illustrate the impact of the quantum dots' excited states and source/drain reservoir's density of states modulation on the tunnel coupling in atomically precise tunnel gaps. Finally, we combine single/few-donor quantum dots with atomically defined single electron transistors as charge sensors and demonstrate single electron charge sensing in few-donor quantum dots. We present characterization of the tunnel coupling between few-donor quantum dots and precision-aligned single electron charge sensors.

#### 6.1.1 Tunnel Coupling in Quantum Computation and Simulation

The conditions for realizing universal quantum computing are extremely demanding, requiring precise control of gate operations on two-level (qubit) quantum systems, a high degree of quantum coherence, and the scalability of millions of qubits.<sup>378</sup> Solid

state implementations of quantum computers, such as coupled quantum dots,<sup>378</sup> donor nuclear spins<sup>31, 35</sup> or electron spins,<sup>379</sup> hold real promise for practically realizing large scale quantum computation. Single qubit manipulation and logic gate (CNOT or NAND) operations are the two basic building blocks for universal quantum computation.<sup>380, 381</sup> Single spin qubit operations require control over a local magnetic field (a Zeeman magnetic interaction),  $H_z = g\vec{S}_i\vec{B}$ , where g is the Lande g-gactor. For logic gate operations, two-qubit gating is enabled by controlled gating of tunnel barriers that mediate the tunable exchange coupling between spins (a Heisenberg interaction)<sup>27.</sup> <sup>61</sup> If the barrier potential is high and the tunneling forbidden, quantum spin states remain isolated and do not interact, i.e. exchange is turned off. When the barrier is pulsed low, a transient Heisenberg coupling is turned on between neighboring spin qubits,<sup>378</sup>  $H_s(t) = J(t) \vec{S}_1 \cdot \vec{S}_2$ , where  $J(t) = 4t_0^2(t)/E_c$  is the time dependent exchange constant due to the turning on and off of the tunnel matrix element  $t_0(t), E_c$ is the charging energy of a dot and  $\vec{S}_i$  is the spin operator for dot *i*.

Along with the important role of tunnel coupling in quantum computation, control over the tunnel coupling is a key ingredient for performing analog quantum simulations in order to explore novel electronic and spin physics of strongly correlated electron systems in solids. Of particular interests is the quantum simulation of the Fermi-Hubbard model using coupled quantum dot systems<sup>382, 383, 384</sup> where the tunnel coupling strength can be tuned to cover a wide range of correlated phases in many-body systems. Quantum dot systems offer a versatile platform for analog quantum simulations.<sup>385</sup> The properties of a quantum dot system are dominated by Coulomb repulsion and the quantum fluctuations associated with electron hopping and spin
exchange, which can be described by the generalized Hubbard model,<sup>383</sup>  $H = -\sum_{i,j} t_{i,j} c_i^{\dagger} c_j + \sum_i U_i n_{i,\uparrow} n_{i,\downarrow} + \sum_i \mu_i n_i$ , where the first term describes the tunnel couplings which include hopping, spin-exchange, and higher order coupling terms; the second term is the Coulomb repulsion term, and the third terms describes the chemical potential.

In addition to the important role of tunnel coupling in the Hamiltonian for both quantum computation and quantum simulations, from an implementation perspective, tunnel coupling is also an enabling element for quantum state initialization and readout in quantum computers and quantum simulators. Single electron transistors (SET) have been used as ultrasensitive charge sensors for spin readout and initialization through spin-to-charge conversion. Control over the dot-reservoir tunnel coupling in an SET allows for high fidelity spin initialization and readout in both the conventional DC charge sensing mode and an advanced radio frequency reflectometry charge sensing mode. <sup>386</sup> For DC-SET operations, the tunnel coupling must be weak enough for a well-defined number of excess electrons on the island and narrow lifetime broadening. The tunnel coupling must also be strong enough to allow measurable current and sufficient charge detection sensitivity.

# 6.2 Exponential Scaling of Tunnel Resistance at the Atomic Limit



Figure 6.1 (a) Electrical contacts (sketched in white) overlaid on top of an STMpatterned SET device. (b) STM image of the central device region of a typical SET device acquired immediately following hydrogen lithography. The bright areas are STM-patterns where the hydrogen-resist has been removed, exposing the chemically reactive dangling bonds. The central device region shows a central island that is tunnel coupled with source and drain leads and capacitively coupled to two in-plane gates. Gate 2 is patterned with a deliberate shift towards the source electrode to allow tuning the tunnel coupling symmetry. A high-resolution STM image at the center region is overlaid on a large-scale lower-resolution STM image. (c) Atomic resolution STM image of an SET pattern (SET-C in Figure 6.2) where the tunnel gaps are defined with atomic precision. The imaged rows running from upper left to lower right are  $2 \times 1$ surface reconstruction dimer rows on the Si (100) surface. The junction gap distance,

*d*, and junction width, *w*, are marked in the image. The circle marks the image of a single dangling bond (DB). The STM image is taken at -2 V sample bias and 0.1 nA setpoint current. (d) An equivalent circuit diagram for the SET, where tunnel junctions are treated as a tunneling resistance and capacitance connected in parallel and the combined coupling of the two gates to the SET island is treated as a capacitor. (e) The energy diagram of an SET, where  $\mu_S$  and  $\mu_D$  are the chemical potentials of the source and drain leads respectively;  $\mu_{IS}(N)$  is the chemical potential of the island that is occupied with *N* excess electrons.  $E_{Barr}$  is the barrier height defined by the energy difference between the electrodes' Fermi levels and the conduction band edge of the substrate. We assume a rectangular barrier shape in this study.

Figure 6.1 (b) shows an STM image of the atomically precise central region of a typical SET device after hydrogen-lithography, but before phosphine dosing. P dopants only incorporate into the bright regions where the STM tip has removed H surface termination atoms and exposed chemically reactive Si-dangling bonds. We observe optimal atomically precise SET lithography by orienting the device in the [110] lattice direction and aligning the geometries at the critical device region (island and tunnel junctions) with the underlying surface reconstructed lattice. The Si (100) 2x1 surface reconstruction features dimer rows of pitch 0.77 nm that can serve as a natural "atomic ruler" allowing us to define the critical dimensions with atomic precision. [Figure 6.1 (c)] The planar source and drain, island (quantum dot), and gates are saturation-dosed resulting in degenerate dopant densities over three orders of magnitude beyond the Mott metal-insulator transition.<sup>60</sup> The island is capacitively coupled to the two in-plane

gates through an effective capacitance  $C_G$  and to the source (drain) electrodes through tunnel barriers represented by a tunneling resistance  $R_S(R_D)$  and a capacitance  $C_S(C_D)$ , where each resistance is coupled in parallel with its respective capacitance [Figure 6.1 (d)]. The gate voltages applied to both gates tune the local electrochemical potential of the island and modulate the source-drain current flowing through the central island. Single electrons tunnel sequentially through both barriers due to the electron addition energy (charging effect) on the island.<sup>78</sup> [Figure 6.1 (e)]



Figure 6.2. High-resolution STM topography images of the hydrogen-lithography patterns of the wire and SET devices in this study. The devices are named as Wire-A, 206

and SET-B to SET-I according to the figure labels. Different STM tips/tip conditions are used for the STM images under imaging conditions: -2 V sample bias and 0.1 nA or 0.05 nA setpoint current.

Device	Gap distance <i>d</i> (dimer rows)	Lead/island width <i>w</i> (dimer rows)	Island length (dimer rows)	# of squares in leads	$R_{\rm S} + R_{\rm D} \left( M \Omega \right)$
Wire-A	0	15.5±1.4	N/A	57±4	N/A
SET-B	7.4±0.6	15.3±0.6	15.2±0.8	74±6	0.011±0.009
SET-C	9.5±0.7	15.7±0.7	13.1±0.6	56±4	0.113±0.061
SET-D	11.1±0.7	15.0±0.8	14.3±0.6	52±4	0.340±0.101
SET-E	11.7±0.4	17.5±1.0	14.9±0.5	56±4	2.06±0.69
SET-F	11.8±0.6	15.2±0.4	15.3±0.4	62±5	2.49±0.63
SET-G	12.2±1.4	18.8±1.2	17.0±1.5	49±4	5.55±2.91
SET-H	13.5±0.6	15.1±0.3	15.4±0.7	52±4	127±59
SET-I	16.2±0.6	17.6±0.7	16.3±0.7	48±4	764±250

Table 6.1. Critical dimensions of the hydrogen lithography patterns from the highresolution STM images (shown in Figure 6.2), where tip convolution artifact has been corrected. The total pattern areas (in units of squares, or the length-width aspect ratio of the STM-patterned leads) from the source and drain leads between the two inner contact probes (see Figure 1 (a)) are also given. The uncertainties in the number of squares is dominated by the uncertainty in the e-beam alignment between the electrical contacts and the STM-patterned contact pads. The right-most column of the table lists the measured total junction resistances ( $R_S + R_D$ ), where corrections have been taken to eliminate contributions from the source and drain lead sheet resistance. The  $R_S + R_D$ for SET-B represents an ohmic resistance where the uncertainty is dominated by uncertainty in estimating the number of squares in the source/drain leads. The  $R_S + R_D$ for SET-C to SET-I represents tunneling resistances where the error bars include contributions from both the variation (one standard deviation) in the Coulomb oscillation peak height over the corresponding gating range (-200 mV to 200 mV, see Figure 6.3 (b)) from multiple gate sweeps and the uncertainty in the subtracted source and drain leads resistance.

Figure 6.2 shows a series of STM images acquired following hydrogen-lithography with surface reconstruction dimer rows clearly visible. While attempting to keep lead width and island size identical, we systematically increase the number of dimer row counts within the tunnel junction gap starting from a continuous wire with zero gaps up to SET tunnel gap distances of ~16.2 dimer rows, covering a large range of SET device operation characteristics with respect to tunnel junctions used in QI applications. Because isolated single dangling bonds do not allow dopants to incorporate, we disregard them in quantifying the device geometry. We estimate the critical dimensions of the STM-patterned tunnel junctions in a SET from the STM topography images in Figure 6.2, where the gap-distance, d, is the average across the full junction width,  $w_{i}$ using both junctions. The junction width is the average over the island and the first 15 nm of the source and drain leads near the island. The hydrogen lithography and STMimaging are carried out using different tips and/or under different tip conditions. To eliminate the effects of tip convolution in an STM image, we estimate the convolutioninduced image-broadening,  $\Delta b$ , from the difference between the imaged single dangling bond size, b, (full-width at half maximum (FWHM)) and the size of a single dangling bond,  $b_0$ , where we have assumed  $b_0$  equals half a dimer row pitch. (see Figure 6.1 (c)). The image-broadening,  $\Delta b = b - b_0$ , is then used to correct the critical

dimensions that are read out from the half-maximum height positions in the STM topography images. The critical dimensions after tip-convolution correction are summarized in Table 6.1 for all devices in this study. The uncertainty in the reported dimensions is given as one standard deviation in the distribution of measurement samples.

# 6.2.1 Methods

The Si:P single electron transistors (SETs) are fabricated on a hydrogen-terminated Si (100) 2x1 substrate  $(3 \times 10^{15} / \text{cm}^3 \text{ boron doped})$  in an ultrahigh vacuum (UHV) environment with a base pressure below  $4 \times 10^{-9}$  Pascal ( $3 \times 10^{-11}$  Torr). Detailed sample preparation, UHV sample cleaning, hydrogen-resist formation, and STM tip fabrication procedures have been published elsewhere.<sup>202, 308</sup> The device geometry is defined using an STM tip in the low-bias  $(3 V \sim 5 V)$  and high-current  $(15 \text{ nA} \sim 50 \text{ nA})$ regime by selectively removing hydrogen atoms from the hydrogen passivated Si (100) surfaces. We then saturation-dose the patterned device regions with PH<sub>3</sub> followed by a rapid thermal anneal at 350 °C for 1 minute to incorporate the P dopant atoms into the Si surface lattice sites while preserving the hydrogen resist to confine dopants within the patterned regions. The device is then epitaxially encapsulated with intrinsic Si by using an optimized locking layer process to suppress dopant movement at the atomicscale during epitaxial overgrowth.<sup>198, 376</sup> The sample is then removed from the UHV system and Ohmic-contacted with e-beam defined palladium silicide contacts.<sup>377</sup> Lowtemperature transport measurements are performed using either a closed-cycle cryostat at a base temperature of 4 K or a dilution refrigerator at a base temperature of  $\sim 10$  mK.

For SET-B to SET-G, the zero-DC bias differential conductance ( $G_0$ ) are measured using 0.1 mV AC excitation at 11 Hz. For SET-H and SET-I,  $G_0$  is numerically estimated from the measured DC charge stability diagrams. The gate leakage currents are on the order of ~10 pA or less within the gating range used in this study.

The theoretical analysis of the transport through SETs is based on an equivalent circuit model (see Figure 6.1 (d)) under a constant interaction approximation. The analytical expressions regarding the equilibrium drain-source conductance in the main text are derived using the standard Orthodox theory under a two-state approximation.<sup>168, 387</sup>

# 6.2.2 Results



Figure 6.3 Electrical characterization of the set of devices using a cryostat with a basetemperature of 4 K. (a) Four-point  $I_{DS} - V_{DS}$  measurement of Wire-A and SET-B while keeping the gates grounded. Inset: Representative 2-point I-V characteristics of a device contact pad. (b) Differential conductance at zero drain-source bias ( $G_0$ ) of the set of SET devices that are measured at T = 4 K. For SET-B to SET-G,  $G_0$  is measured using 0.1 mV AC excitation at 11 Hz. For SET-H and SET-I,  $G_0$  is numerically estimated from the measured DC charge stability diagrams. From top to bottom: SET-B (red) to SET-I (dark blue). The difference in the oscillation period in gate voltage is due to the variations in gate designs that alter the gate capacitance. (c) The measured total tunneling resistance values  $R_S + R_D$  as a function of the lithographically-defined

tunnel gap distances. The WKB-fitting is based on the tunneling resistance values from SET-C to SET-I, where the lateral electrical seam width of the electrodes and the rectangular barrier height are taken as free fitting parameters. (d) The measured differential conductance  $dI_{DS}/dV_{DS}$  (on a color linear scale) charge stability diagram of SET-C (upper panel) and SET-F (lower panel) at T = 4 K.

In Figure 6.3 (a), the I-V characteristics of Wire-A exhibit Ohmic behavior with a 4point resistance of 96.8 k $\Omega$ . The inset shows a representative 2-point I-V characteristics  $(3.5 \text{ k}\Omega)$  across an individual contact pad of a device. Detailed characterization of our high-yield, low-resistance electrical contacts to STM-patterned devices has been published elsewhere.<sup>377</sup> Considering the actual STM-patterned wire geometry [approximately  $57 \pm 4$  squares between the e-beam patterned voltage contact probes, see Figure 6.2(a)], this corresponds to a sheet resistance of  $(1.7 \pm 0.2)$  k $\Omega$  in the STMpatterned electrodes, in excellent agreement with previous results on metallically doped Si:P delta layers.<sup>192</sup> It should be noted that we are focused on optimized tunnel junction geometry and minimizing dopant movement during fabrication, which results in higher sheet resistance than is otherwise possible.<sup>198, 376</sup> Given the ultrahigh carrier density and small Thomas Fermi screening length<sup>60</sup> in this saturation-doped Si:P system and the relatively large island size<sup>387</sup> of the SETs, we treat the energy spectra in the islands and source and drain leads as continuous ( $\Delta E \ll k_B T$ , where  $\Delta E$  is the energy level separation in the island and source and drain reservoirs) and adopt a metallic description of SET transport.<sup>78</sup> The tunneling rates,  $\Gamma_{S,D}$ , and the tunneling resistances,  $R_{S,D} = \hbar/(2\pi e^2 |A|^2 D_i D_f)$ , across the source and drain tunnel barriers can be

described using Fermi's golden rule, <sup>80</sup> where *A* is the tunneling matrix element,  $D_{i,f}$  represents the initial and final density of states,  $\hbar$  is the reduced Plank's constant, and *e* is the charge of an electron.

In the following, we show that the total tunneling resistance  $R_S + R_D$  of an SET can be extracted by measuring, at zero drain-source DC-bias, the peak amplitudes of the differential conductance Coulomb oscillations, as shown in Figure 6.3 (b). At  $V_{DS} =$ 0 V, the differential conductance Coulomb blockade oscillations reach peaks at  $V_{GS} =$  $V_{GS}^{peak} = \left(N + \frac{1}{2}\right)\frac{e}{C_G}$ , where N is an integer and  $\left(N + \frac{1}{2}\right)e$  represents the effective gating charge when the island Fermi level  $\mu_{IS}(N)$  aligns with  $\mu_S$  and  $\mu_D$ . At low temperatures and in the metallic regime,  $\Delta E \ll k_B T \ll E_C$ , where  $E_C = e^2/C_{\Sigma}$  is the charging energy, and  $C_{\Sigma} = C_S + C_D + C_G$  is the total capacitance, and assuming energy independent tunnel rates and density of states in a linear response regime, Beenakker and co-workers<sup>163, 388</sup> have shown that the peak amplitude of the zero-bias differential conductance oscillations in an SET reduces to the following temperature independent expression for arbitrary  $R_S$  and  $R_D$  values,

$$\frac{dI_{DS}}{dV_{DS}}\Big|_{V_{GS}^{peak}} = \frac{e^2\rho}{2}\frac{\Gamma_S\Gamma_D}{\Gamma_S + \Gamma_D} = \frac{1}{2}\frac{G_SG_D}{G_S + G_D} = \frac{1}{2(R_S + R_D)}$$

#### Equation 6.1

where  $G_S$  and  $G_D$  are conductances through the source and the drain tunnel barriers,  $\rho$  is the density of state in the metallic island, and the density of states in the leads is embedded in the tunneling rates.

In Figure 6.3 (b) we observe Coulomb blockade oscillations in all SETs except SET-B. The absence of the Coulomb blockade effect in SET-B is straightforward to

understand considering the decay of the electron wave function (on the order of the Bohr-radius) beyond the doped regions. The small gap distance (~7.4 dimer rows  $\approx$  5.7 nm) in SET-B is comparable to twice the Bohr radius,  $r \sim 2.5$  nm, of an isolated P atom in bulk Si,<sup>389</sup> indicating significant wavefunction overlap within the gap regions between the island and the source/drain reservoir. One of the fundamental requirements to observe the Coulomb blockade effect in an SET is to have the island sufficiently isolated from the source/drain reservoir ( $R_{S,D} \gg \frac{h^2}{e} \approx 26 \text{ k}\Omega$ ) so a well-defined integer number of electrons can reside on the island.<sup>80</sup>

Given that SET-B does not exhibit single electron tunneling behavior (Coulomb oscillations), we estimate the resistance at the junction gaps in this device using 4-point I-V measurement. As shown in Figure 6.3 (a), SET-B has a linear I-V behavior with the 4-point resistance of 136.7 k $\Omega$ . Subtracting the resistance contribution from the source/drain leads (~74 squares) using the estimated sheet resistance (~1.7 k $\Omega$ ) from Wire-A, we obtain a junction resistance value of ~5.5 ± 4.5 k $\Omega$  per junction in SET-B, which does indeed fall below the resistance quantum (~26 k $\Omega$ ), and explains the absence of Coulomb blockade behavior. We emphasize that, due to the absence of the Coulomb blockade effect, the estimated resistance at the junctions in SET-B is an ohmic resistance, which should not be confused with the tunneling resistance.

For the rest of the SETs, the measured peak amplitudes of the differential conductance Coulomb blockade oscillations decrease by more than three orders of magnitude as the averaged gap distances increase from ~9.5 to ~16.2 dimer rows [Figure 6.3 (b)] Following equation 6.1, we extract the total tunneling resistance,  $R_S$  +  $R_D$ , from the Coulomb oscillation peak heights. For accuracy, we also subtracted from

 $R_S + R_D$  the contribution from the source/drain sheet resistance according to the number of squares in the source/drain leads (see Table 6.1). Figure 6.3 (c) summarizes the measured junction resistance values (after sheet resistance correction from the source and drain leads) as a function of the averaged gap distances. The tunneling resistance follows a clear exponential relationship with the gap distances.

# 6.2.3 Modeling the Tunnel Barriers Using the WKB Method

It has been found essential for capacitance modeling (See Table 6.2 in the next section) to add a lateral electrical seam<sup>390</sup> and a vertical electrical thickness<sup>157</sup> to the STM-patterned hydrogen-lithography geometry (Figure 6.2) to account for the Bohr radius and yield the actual "electrical geometry" of the device. We fit the tunneling resistance (multiplied by two to account for  $R_S + R_D$ ) from SET-B to SET-H as a function of the tunnel gap distance using the WKB method assuming a rectangular barrier shape.<sup>83</sup> We expect exponential dependence of the tunnel conductance on both the barrier height and barrier width, whereas a linear dependence on the tunneling cross-section area is expected. Therefore, small variations in the STM-patterned junction width, *w*, is assumed to have minor effects on the tunnel conductance. We adopt an averaged value of w = 12 nm (see column 3 in Table 6.1) in the WKB simulation. We account for the "electrical geometry" of the devices by assuming an electrical thickness of z = 2 nm,<sup>157</sup> while treating the lateral electrical seam width, *s*, and the rectangular barrier height, *E*<sub>barr</sub>, as fitting parameters.

We fit the measured tunneling resistance  $R_S + R_D$  as a function of the STMpatterned tunnel gap distance, *d*, using the well-known Simmons' WKB formulation in the low-bias (linear response) regime.<sup>83, 391</sup> We adopt an ideal rectangular barrier shape ignoring the image force correction to the barrier potential when an electron approaches the dielectric barrier interface. The barrier height,  $E_{barr}$ , is defined as the energy difference between the electrode reservoirs' Fermi level and the conduction band minimum. The electrical junction width and the electrical junction gap distance are expressed as (w + 2s) and (d - 2s) respectively. (w + 2s)z represents the electrical tunnel junction cross-sectional area. The WKB tunneling resistance,  $R_T$ , in the low-bias regime is expressed in Equation 6.2.<sup>83, 391</sup>

$$\frac{1}{R_T} = \frac{[(w+2s)z]\sqrt{2m^*E_{barr}}}{(d-2s)} \left(\frac{e}{h}\right)^2 \exp\left[-\frac{4\pi(d-2s)}{h}\sqrt{2m^*E_{barr}}\right]$$

Equation 6.2

Where *h* is Plank's constant, *e* is the charge of a single electron, and  $m^*$  is the effective mass of the conducting electrons. Conductivity in the degenerately  $\delta$ -doped Si:P electrodes is assumed to be dominated by the lowest energy sub-bands, with effective mass  $m^* = 0.21m_e$  as measured by Miwa *et al.* using direct spectroscopic measurement in blanket  $\delta$ -doped Si:P layers,<sup>364</sup> where  $m_e$  is the free electron mass. We point out that, at a given barrier height  $E_{barr}$ , the dependence of WKB tunneling resistance,  $R_T$ , on the gap distance, *d*, deviates from an ideal exponential behavior, especially at small gap distances, due to the pre-factor in front of the exponential term in Equation 6.2.

We obtain  $(100 \pm 50)$  meV as the best-fit barrier height (uncertainty represents two  $\sigma$ ), which is in good agreement with the theoretically predicted range of Fermi levels below the Si conduction band edge in highly  $\delta$ -doped Si:P systems, ~80 meV to ~130 meV, from tight-binding<sup>157</sup> and density functional theory<sup>389</sup> calculations. A similar barrier height value (~80 meV) has also been experimentally determined in a Fowler-Nordheim tunneling regime by Fuhrer's group using a similar STM-patterned Si:P device.<sup>373</sup> We obtain  $(3.1 \pm 0.4)$  nm as the best-fit seam width (uncertainty represents two  $\sigma$ ), which is in good agreement with the Bohr radius of isolated single phosphorus donors in bulk silicon ( $r \sim 2.5$  nm).<sup>389</sup> Using the best-fit seam width from the WKB simulation, we also find good agreement between the experimental and simulated capacitance values from the SETs.

# **6.2.4** Comparison between the Measured and Simulated Capacitances in STM-Patterned SET Devices

The mutual capacitance values in a SET can be extracted from the Coulomb diamond shapes in an experimentally measured charge stability diagram. We calculate the total island capacitance  $C_{\Sigma}$  and the island-gate capacitances  $C_{G}$  from the average height  $(E_{C}/e)$  and width  $(\Delta V_{G})$  of the Coulomb diamonds using  $E_{C} = \frac{e^{2}}{C_{\Sigma}}$  and  $\frac{e\Delta V_{G}}{E_{C}} = \frac{C_{\Sigma}}{C_{G}}$  where  $E_{C}$  is the charging energy and  $C_{\Sigma} = C_{S} + C_{D} + C_{G}$  is the total island capacitance. Along the negative (positive) slopes of the Coulomb diamonds,  $\mu_{IS}$  aligns with the chemical potential of the drain  $\mu_{IS}$  (source  $\mu_{IS}$ ). At the alignment condition, the change in free energy due to a single electron tunneling event is zero. Therefore, the island-drain and island-source mutual capacitances  $C_{D}$  and  $C_{S}$  can be derived by setting the  $\Delta F$ expression to zero,

$$\Delta F_{\mathcal{S}}^{N+1,N} = \frac{e}{C_{\mathcal{S}}} \left( \frac{e}{2} + (Ne - Q_0) - C_D V_D - C_G V_G \right) = 0$$

$$V_{D} = -\frac{C_{G}}{C_{D}}V_{G} + \frac{\frac{e}{2} + (Ne - Q_{0})}{C_{D}}$$

$$\frac{\partial V_D}{\partial V_G} = -\frac{c_G}{c_D}$$
 (along the negative slopes of diamonds)

Equations 6.3

Similarly, we have

$$\frac{\partial V_D}{\partial V_G} = \frac{c_G}{c_S + c_G}$$
 (along the positive slopes of diamonds)

Equation 6.4



Figure 6.4. FastCap input profiles. The mutual capacitance between SET components is modeled using the FastCap software package.<sup>392</sup> The device components are treated as metallic conductors and are meshed into 3-D wire grid. The device geometry is extracted from the STM-lithography image with a uniform thickness of 2 nm to account for the finite 2-D confinement in the z-direction. A lateral seam of ~2 nm is added to account for the spatial extension of electron density in the lateral directions. We find

better agreement with the experimental data when using the "electrical geometry" as the FastCap input.

Capacitance modeling of STM-patterned Si:P devices has demonstrated success in accurately predicting the device electrostatics down to the atomic scale.<sup>390</sup> Table 6.2 compares the experimentally observed SET capacitances and the simulated capacitances, where the device components are treated as metallic sheets in the shape of the "electrical geometry" of the device. <sup>390, 393</sup> A uniform electrical thickness of z=2 nm in the z-direction is assumed for both the Simulation 1 and Simulation 2. No lateral electrical seam is added to the hydrogen lithography pattern in Simulation 1. The simulated capacitances from Simulation 1 agree poorly with the measured capacitances. In Simulation 2, a lateral electrical seam width of 3.1 nm from the WKB tunneling resistance fit is added to the STM-patterned device geometry, which significantly improves the agreement between the simulated and measured capacitances.

	$E_{\rm C}$ (meV)	$\mathcal{C}_{\Sigma}$ (aF)	$\mathcal{C}_{\mathbf{G}}$ (aF)	$\mathcal{C}_{\mathrm{S}}$ (aF)	$\mathcal{C}_{\mathrm{D}}$ (aF)
Experiment	11.9 <u>+</u> 0.3	13.5 <u>+</u> 0.3	$2.8 \pm 0.2$	$5.0 \pm 0.3$	5.7 ± 0.3
Simulation 1 (no seam)	19.5	8.2	2.6	2.8	2.8
Simulation 2 (with 3.1 nm seam)	10.5	15.3	3.2	6.0	6.1

Table 6.2 The experimental and simulated charging energy and capacitances of SET-G. The experimental capacitances are extracted using the height and width of the

measured Coulomb diamonds [Figure 6.5 (a) in a later section] as well as the slopes of the positive and negative diamond edges.<sup>78</sup> The uncertainties result from the experimental determination of the Coulomb diamond dimensions from the measured charge stability diagrams while extracting the experimental capacitances. The capacitance simulation is carried out using a finite-element 3D Poisson solver, FastCap.<sup>392,394</sup>

## 6.2.5 Discussion

Figure 6.3 (c) is a key result of this study, clearly demonstrating an exponential scaling of tunneling resistance to the atomic limit. In addition, we find that to obtain tunneling resistance values comparable to those reported in the literature from similar STM-patterned tunnel junctions,<sup>292, 370, 372</sup> we need to pattern our tunnel gaps with smaller gap distances in general. This further emphasizes the improved dopant confinement in the our STM-patterned devices. We highlight that the series of devices shown in Figure 6.2 were fabricated in series from two different UHV-STM systems. This is important as it further demonstrates atom scale control across similar but non-identical hardware platforms using the same nominal methods and processes.

In Figure 6.3 (c), it is notable that a change of only nine dimer rows gives rise to over four orders of magnitude change in the junction resistance. Increasing the gap distance over a small range (from ~7 dimer rows to ~12 dimer rows in the gap) dramatically changes the SET operation from a linear conductance regime to a strong tunnel coupling regime (at ~9 dimer rows separation) to a weak tunnel coupling regime. The first clear transition in operation regimes is seen between SET-B and SET-C. As noted in Figure 6.3 (b), the device with the narrower gap (~7.4 dimers) shows no sign of Coulomb oscillations while SET-C with a gap of ~9.5 dimers shows differential conductance oscillations as the gate voltage is swept, resulting in a clear signature of Coulomb diamonds in its charge stability diagram, as shown in the upper panel of Figure 6.3 (d). The relatively strong tunnel coupling at the ~9.5 dimer rows gap blurs the charge quantization on the island and introduces finite conductance within the Coulomb diamonds through higher order tunneling processes (co-tunneling) that involve two (or more) electrons.<sup>395</sup> By increasing the gap distance by another ~2 dimer rows, we increase the average tunneling resistance per junction by roughly one order of magnitude from ~57 k $\Omega$  in SET-C to ~1.25 M $\Omega$  in SET-F. This transitions the SET operation into a weak tunnel coupling regime where the Coulomb blockade diamonds are very well established [Figure 6.3 (d) lower panel]. Tuning the tunnel coupling between strong and weak coupling regimes in atomic devices is an essential capability: e.g. for simulating non-local coupling effects in frustrated systems.<sup>385</sup>

# 6.2.6 Quantifying Individual Junction Resistance in an SET



Figure 6.5 DC measurement of SET-G using a dilution refrigerator with a basetemperature of ~10 mK. (a) The DC-measured charge stability diagram, where the drain-source current  $I_{DS}$  is plotted as the absolute values for clarity. (b) The measured Coulomb blockade oscillations at selected drain-source biases. (c) Simulated Coulomb blockade oscillations at positive drain-source bias, assuming asymmetric junction resistances  $R_S = 9R_D$ . At  $V_{DS} = 0.8E_C/e$ , the dotted and dashed lines plot the simulated tunneling current through the rate-limiting source and drain tunnel junctions at the leading and trailing edges of the Coulomb oscillation peaks respectively, while ignoring the other junction in series. (d) The extracted junction resistances from Coulomb oscillation peaks along the gate voltage axis. The horizontal and vertical

uncertainties at the data points are calculated by averaging the oscillation peak positions and the tunneling resistances at different drain-source biases.

Probe-based atom scale fabrication is acutely demanding on tip sharpness and stability for both atomic precision lithography and atomic resolution imaging. Having demonstrated atom scale control of the tunnel coupling, we now take an additional step to characterize the junction resistance difference in a pair of nominally identical tunnel junctions in SET-G, where both the tunnel gaps have irregular edges and the tunnel gap distances are less well-defined when compared with the tunnel gaps in the other SETs, representing a lower bound of controllability among the SET devices in this study. Characterizing individual junction resistances in an SET requires transport measurements at lower temperatures and finite source-drain bias.<sup>78</sup> We present the measured charge stability diagram and finite bias Coulomb oscillations in Figure 6.5 (a) and (b). In Figure 6.5 (b), the Coulomb oscillation peaks are asymmetric across the gate voltage. For positive drain-source bias, at the leading edge of the Coulomb oscillation peak of  $N \leftrightarrow N + 1$  transition, the island spends most of the time unoccupied (N). So, the total tunneling rate is limited by tunneling from the source to the island, and thus the total tunneling resistance is dominated by  $R_{\rm S}$ . The other three cases are analogous. Figure 6.5 (c) takes  $V_{DS} > 0$  for instance and shows a numerical simulation (at T = 0 K) of  $I_{DS} vs. V_{GS}$  at different drain-source bias. The dashed and dotted lines in Figure 6.5 (c) illustrate the asymptotic slopes at the leading and trailing edges of the Coulomb oscillation peaks at  $V_{DS} = 0.8E_C/e$ , which also represent the tunneling current through the rate-limiting source and drain tunnel junctions,

respectively, while ignoring the other junction in series. At T = 0 K, the source and drain junction resistances can be derived from the right derivative at the leading edge, where  $V_{GS} = V_{GS}^L = \left(N + \frac{1}{2}\right)\frac{e}{c_G} - \frac{c_D}{c_G}V_{DS}$ , and from the left derivative at the trailing edge, where  $V_{GS} = V_{GS}^T = \left(N + \frac{1}{2}\right)\frac{e}{c_G} + \frac{(C_S + C_G)}{c_G}V_{DS}$ , of a Coulomb oscillation peak in  $I_{DS}$ .

Following the well-established Orthodox theory for a metallic SET,<sup>80</sup> the tunneling resistance across the individual tunnel barriers can be extracted from the peak shapes of Coulomb oscillations in  $I_{DS}$ . In this section, we derive the explicit expressions to estimate individual tunnel junction resistance in a metallic SET using an analytical model that was first proposed by Inokawa and Takahashi.<sup>168</sup>

The tunneling probability through an SET is determined by the change in the SET's Helmholtz's free energy F = U - W, where U is the total electrostatic energy stored in the system and W is the work done by voltage sources, due to a single electron tunneling event. Following the constant interaction model in a metallic regime [See Figure 6.1 (d)], the change in F when an electron tunnels from the source/drain electrodes to the island and transitions the number of excess electrons on the island from N to N + 1 can be expressed as  $\Delta F_{S,D}^{N+1,N} = -\mu_{S,D} + \mu_{IS}(N)$ , where  $\mu_{S,D}$  and  $\mu_{IS}(N)$  are the chemical potential of the source/drain leads and an SET island with N excess electrons.<sup>371</sup>

In the zero-temperature limit, T = 0 K, the tunneling rates can be expressed using Fermi's golden rule.

$$\Gamma_{S,D}^{N+1,N} = \frac{1}{R_{S,D}e^2} (-\Delta F_{S,D}^{N+1,N}) \Theta(\Delta F_{S,D}^{N+1,N})$$

$$\Gamma_{S,D}^{N,N+1} = \frac{1}{R_{S,D}e^2} (-\Delta F_{S,D}^{N,N+1}) \Theta(\Delta F_{S,D}^{N,N+1})$$

Equation 6.5

Where  $\Theta(x)$  is a unit step function. For simplicity, we have assumed the single electron tunneling events to be elastic without electromagnetic interactions between the tunneling electron and the environmental impedance.<sup>166</sup>

In an equilibrium condition, the stationary occupancy probability, P(N), of the SET island (with N excess electrons) can be derived by requiring dP(N)/dt = 0 in a steady state master equation <sup>78</sup> and obtaining  $P(N)(\Gamma_S^{N+1,N} + \Gamma_D^{N+1,N}) = P(N + 1)(\Gamma_S^{N,N+1} + \Gamma_D^{N,N+1})$ . At low-temperatures where  $k_BT \ll E_C$ , only the two most-probable charge states dominate the SET island occupancy at a given bias. Adopting a two-state approximation, <sup>168</sup> P(N) + P(N + 1) = 1, an analytical expression of the total drain-source current through the SET can be obtained,

$$I_{DS}(N) = -eP(N) \Gamma_D^{N+1,N} + eP(N+1)\Gamma_D^{N,N+1}$$
$$= e \frac{\Gamma_D^{N,N+1}\Gamma_S^{N+1,N} - \Gamma_D^{N+1,N}\Gamma_S^{N,N+1}}{\Gamma_D^{N+1,N} + \Gamma_S^{N+1,N} + \Gamma_D^{N,N+1} + \Gamma_S^{N,N+1}}$$

Equation 6.6

Using the expression of  $\mu_{IS}(N)$  from the constant interaction model,<sup>371</sup> we have,

 $I_{DS}|_{T=0}$ 

$$=\frac{1}{C_{\Sigma}}\frac{\left[\frac{e}{2}+(Ne-Q_{0})+(C_{S}+C_{G})V_{DS}-C_{G}V_{GS}\right]\left[\frac{e}{2}+(Ne-Q_{0})-C_{D}V_{DS}-C_{G}V_{GS}\right]}{R_{D}\left[\frac{e}{2}+(Ne-Q_{0})-C_{D}V_{DS}-C_{G}V_{GS}\right]-R_{S}\left[\frac{e}{2}+(Ne-Q_{0})+(C_{S}+C_{G})V_{DS}-C_{G}V_{GS}\right]}$$

Equation 6.7

where  $Q_0 (|Q_0| \leq \frac{e}{2})$  represents a fractional electron charge that is present on the island when the voltage electrodes are floating, typically due to background charges from the environment. Taking  $V_{DS} > 0$  at T = 0 K for instance, the source and drain junction tunneling resistances can be derived from the right derivative at the leading edge, where  $V_{GS} = V_{GS}^L = \left(N + \frac{1}{2}\right)\frac{e}{c_G} - \frac{c_D}{c_G}V_{DS}$ , and from the left derivative at the trailing edge, where  $V_{GS} = V_{GS}^T = \left(N + \frac{1}{2}\right)\frac{e}{c_G} + \frac{(C_S + C_G)}{c_G}V_{DS}$ , of a Coulomb oscillation peak in  $I_{DS}(V_{GS})$ . According to Equation 6.7 (assuming  $Q_0 = 0$ ), the right derivative at the leading edge, where  $V_{GS} = V_{GS}^L = V_{GS}^L$ , has the following expression,

$$\frac{\partial_{+}I_{DS}}{\partial V_{GS}}\Big|_{V_{GS}^{L}} = \lim_{\Delta V_{GS} \to 0} \frac{I_{DS}(V_{GS}^{L} + \Delta V_{GS}) - I_{DS}(V_{GS}^{L})}{\Delta V_{GS}}$$
$$= \lim_{\Delta V_{GS} \to 0} \frac{1}{C_{\Sigma}\Delta V_{GS}} \frac{(C_{\Sigma}V_{DS} - C_{G}\Delta V_{GS})(-C_{G}\Delta V_{GS})}{R_{D}(-C_{G}\Delta V_{GS}) - R_{S}(C_{\Sigma}V_{DS} - C_{G}\Delta V_{GS})} = \frac{C_{G}}{R_{S}C_{\Sigma}}$$
Equation 6.8

Similarly, the left derivative at the trailing edge, where  $V_{GS} = V_{GS}^T$ , has the following expression,

$$\frac{\partial_{-}I_{DS}}{\partial V_{GS}}\Big|_{V_{GS}^{T}} = \lim_{\Delta V_{GS} \to 0} \frac{I_{DS}(V_{GS}^{T}) - I_{DS}(V_{GS}^{T} - \Delta V_{GS})}{\Delta V_{GS}}$$
$$= \lim_{\Delta V_{GS} \to 0} \frac{-1}{C_{\Sigma} \Delta V_{GS}} \frac{(C_{G} \Delta V_{GS})(C_{G} \Delta V_{GS} - C_{\Sigma} V_{DS})}{R_{D}(C_{G} \Delta V_{GS} - C_{\Sigma} V_{DS}) - R_{S}(C_{G} \Delta V_{GS})} = \frac{-C_{G}}{R_{D} C_{\Sigma}}$$

Equation 6.9

In Equations 6.8 and 6.9, the gate and total capacitances,  $C_G$  and  $C_{\Sigma}$  are extracted from the measured Coulomb diamond dimensions in Figure 6.5 (a) (see Table 6.2). To estimate the drain and source tunneling resistances from the Coulomb oscillation peaks that are measured at finite temperatures [Figure 6.5 (b)], we approximate the asymptotic slopes at the leading and trailing edges by fitting the leading and trailing slopes of the measured Coulomb oscillation peaks and average over a range of  $V_{DS}$  bias. [see Figure 6.5 (d)] We find a factor of approximately four difference in the source and drain tunneling resistances. Possible contributions to this resistance difference include atomic-scale imperfections in the hydrogen lithography of tunnel gaps, the randomness in the dopant incorporation sites within the patterned regions, and unintentional, albeit greatly suppressed, dopant movement at the atomic-scale during encapsulation overgrowth. From the exponential dependence in Figure 6.3 (c), a factor of four corresponds to an uncertainty in the gap distance of only about half of a dimer row pitch distance, which represents the ultimate spatial resolution [a single atomic site on the Si (100) 2x1 reconstruction surface] and the intrinsic precision limit for the atomically precise hydrogen-lithography. In Figure 6.5 (d), we also plot the source and drain resistance values as a function of gate voltage. There is more significant gate modulation on the source junction resistance, but little or none on the drain junction resistance.

# 6.3 Tunnel Coupling of Atomic-scale Few-donor Quantum Dots

So far, our discussion on the atomic control of tunnel coupling in a single electron transistor has been based on an SET island in the metallic regime, where the energy level distributions on the island and the reservoir leads can be treated as continuous. In the metallic regime, the continuum spectrum of the ground and excited states within the drain-source bias window contribute to the tunneling rate of sequential single electron tunneling events. The measured tunneling rates in the previous section are averaged values over a small bias window centered at the Fermi level of the metallic island. As the SET island is scaled down to a few-donors<sup>396</sup> or even a single donor<sup>59</sup> in the quantum dot region, the single-particle energy level spacing  $\Delta E$  becomes large compared with thermal broadening. Then, controlling the tunnel coupling in this quantum dot regime requires characterization of tunneling rates at the individual quantum level.

Historically, transport studies through few/single donors have been realized by using planar nano-scale field effect transistors (FET),<sup>397</sup> gated nanowires (silicon FinFET)<sup>398</sup> or gated nanobridges<sup>399</sup> where the few or single dopant atoms in the transport channel are placed by either low-energy ion implantation<sup>397, 400, 401</sup> or diffusion from highly doped source/drain contact extensions.<sup>164, 402, 403, 404</sup> The spatial precision of the dopant placement in these approaches is limited to ~10 nm,<sup>397</sup> which is insufficient for practical implementations of solid-state quantum computation. Fuchsle et al.<sup>59, 396</sup> demonstrated the first STM-patterned Si:P few/single-donor SETs using atomically abrupt hydrogen lithography and low-temperature epitaxial overgrowth techniques.<sup>57</sup> Beside the promise of fabricating donor-based quantum devices with atomic precision, another key advantage that distinguishes this STM Si:P fabrication method from other conventional fabrication methods is that the few/single donor quantum dot is encapsulated in an all-epitaxial environment that isolates the

single donor from defects near the surface or nearby interface. While tight binding calculations have shown that disorder in the highly doped source/drain leads has little impact on the quantum dot, donor placement with atomic precision is required to control the electronic structure of few/single-donor quantum dots.<sup>405</sup>

In the following sections, we first briefly review resonant tunneling features in quantum dots that originate from both the intrinsic properties of the SET dot, such as excited states of the dot, and extrinsic effects, such as quantum confinement DOS features in the source and drain leads. Using single charge tunneling simulations, we illustrate the manifestation of tunnel coupling asymmetry in resonant tunneling features, following Escott, *et al.*<sup>406</sup> and the approach laid out in their review article on the resonant tunneling features of quantum dots. We then demonstrate the fabrication and characterization of few-donor quantum dots at the atomic scale using STM. Combining low-temperature electrical transport measurement with single electron tunneling simulations, we characterize the atomic-scale tunnel coupling features by analyzing charge stability diagrams of our few-donor quantum dots.



Figure 6.6 Single electron tunneling spectroscopy through discrete energy levels and excited states. (a)  $U_1^G (U_2^G)$  and  $U_1^E (U_2^E)$  are the ground and excited state energy levels for the quantum dot charge state N = 1 (N = 2), where the excited state energy level lays  $\Delta E_1 (\Delta E_2)$  above the ground state energy level. The solid arrows indicate the possible single electron transitions between different states. Transitions between excited states are ignored. (b) The corresponding chemical potentials for the transitions depicted in (a). (c) Schematic of the charge stability diagram at the transition between N = 1 and N = 2. The diamond edges (black lines) represent the differential conductance lines that only involve ground states. The diamond edges with negative (positive) slopes represent the situation when the ground state chemical potential level is in alignment with the source (drain) Fermi level. The excited state chemical potential level is conductance lines (solid red and green lines) that run parallel to the diamond edges outside of the blockaded regions. (d) Energy diagrams showing the level alignment at the indicated positions in (c).

# 6.3.1 Tunneling Spectroscopy through Excited States

At the limit of zero drain-source bias, only a single chemical potential level  $\mu_N$  on the dot is involved in single electron tunneling. As the drain-source bias window increases, excited states become available for single electrons to tunnel through. The additional single electron conduction channels from excited states give rise to additional differential conductance features that run parallel to the diamond edges outside of blockaded regions. (See Figure 6.6) When only the ground states of the quantum dot are involved, the chemical potential can be expressed as  $\mu_N^0 = U_{N+1}^G - U_N^G$ , where  $U_N^G$ represents the total energy of a dot when the N excess electrons are all in their ground states. We denote the total energy of a dot with excited states occupancy as  $U_N^E$ , where the excited states can refer to either orbital excited states, or spin excited states in external magnetic fields, or lifted valley excited states due to strong confinement. To illustrate the basic principles of single electron tunneling through excited states, we take the transition between N = 1 and N = 2 charge states for example and assume one excited state for each charge state. (See Figure 6.6) We ignore the transition between the two excited states because its transition probability is small compared with the transition probability that involves at least one ground state. The three chemical potential levels can be expressed as,

$$\mu_1^{-1} = U_2^G - U_1^E$$
$$\mu_1^0 = U_2^G - U_1^G$$
$$\mu_1^1 = U_2^E - U_1^G$$

Equations 6.10

And the spacings of the chemical potential levels represent the energy of the excited states,

$$\Delta E_1 = U_1^E - U_1^G = \mu_1^0 - \mu_1^{-1}$$
$$\Delta E_2 = U_2^E - U_2^G = \mu_1^1 - \mu_1^0$$

#### Equations 6.11

As shown in Figure 6.6 (c), the differential conductance features due to excited states run parallel to the diamond edges outside of the blockaded regions. The line features with negative (positive) slopes correspond to when the chemical potential levels aligned with the source (drain) Fermi level. The sizes of the bias window at the intersections along the diamond edges represent the energy spacing between the ground and excited states. Identifying these intersection points at the diamond edges is the primary way to reconstruct the excited states spectrum of a quantum dot.<sup>164, 406</sup> Because the conductance through an excited chemical potential level is only sustainable when both the ground and the excited chemical potential levels are within the bias window, the differential conductance line features from excited states only appear outside of Coulomb diamonds. For instance, if only the excited level  $\mu_1^{-1}$  is within the bias window [see case 2 in Figure 6.6 (d)], the single electron conductance will be blockaded once the excited State  $U_1^E$  relaxes into its ground state  $U_1^G$ . On the other hand, if both the  $\mu_1^{-1}$  and  $\mu_1^0$  levels are within the bias window, both the  $U_1^E$  and  $U_1^G$  states contribute to the conductance.

Following the approach laid out by Park,<sup>174</sup> we derive an analytical expression of the total tunneling current using an equilibrium master equation. We denote the tunneling rates between source/drain and each of the chemical potential levels as  $\Gamma_{T1}^{a}$ , where T = S, D represents the source and drain leads, and a = -1, 0, 1 represents the three chemical potential levels. We denote the Fermi-Dirac distribution in the source/drain reservoirs at a chemical potential of the dot as  $f_{T1}^a = f_T(\mu_1^a)$ . We denote the occupation probability at the ground and excited states as  $P_1^G, P_1^E, P_2^G$ , and  $P_2^E$ . Using the two-(charge)state approximation, we have the normalization condition,  $P_1^G + P_1^E + P_2^G + P_2^E = 1$ . The time derivatives of each of the occupation probability can be expressed as, (for simplicity, we have ignored the relaxation rate from an excited state state to the corresponding ground state.)

$$\begin{split} \frac{\partial P_1^G}{\partial t} &= -P_1^G [\Gamma_{S1}^0 f_{S1}^0 + \Gamma_{D1}^0 f_{D1}^0 + \Gamma_{S1}^1 f_{S1}^1 + \Gamma_{D1}^1 f_{D1}^1] - P_1^E \cdot 0 \\ &+ P_2^G [\Gamma_{S1}^0 (1 - f_{S1}^0) + \Gamma_{D1}^0 (1 - f_{D1}^0)] \\ &+ P_2^E [\Gamma_{S1}^1 (1 - f_{S1}^1) + \Gamma_{D1}^1 (1 - f_{D1}^1)] \\ \\ \frac{\partial P_1^E}{\partial t} &= -P_1^G \cdot 0 - P_1^E [\Gamma_{S1}^{-1} f_{S1}^{-1} + \Gamma_{D1}^{-1} f_{D1}^{-1}] + P_2^G [\Gamma_{S1}^{-1} (1 - f_{S1}^{-1}) + \Gamma_{D1}^{-1} (1 - f_{D1}^{-1})] \\ &+ P_2^E \cdot 0 \\ \\ \frac{\partial P_2^G}{\partial t} &= P_1^G [\Gamma_{S1}^0 f_{S1}^0 + \Gamma_{D1}^0 f_{D1}^0] + P_1^E [\Gamma_{S1}^{-1} f_{S1}^{-1} + \Gamma_{D1}^{-1} f_{D1}^{-1}] \\ &- P_2^G [\Gamma_{S1}^0 (1 - f_{S1}^0) + \Gamma_{D1}^0 (1 - f_{D1}^0) + \Gamma_{S1}^{-1} (1 - f_{S1}^{-1}) + \Gamma_{D1}^{-1} (1 - f_{D1}^{-1})] \end{split}$$

$$+ P_2^E \cdot 0$$

$$\frac{\partial P_2^E}{\partial t} = P_1^G [\Gamma_{S1}^1 f_{S1}^1 + \Gamma_{D1}^1 f_{D1}^1] + P_1^E \cdot 0 - P_2^G \cdot 0 + P_2^E [\Gamma_{S1}^1 (1 - f_{S1}^1) + \Gamma_{D1}^1 (1 - f_{D1}^1)]$$
  
Equations 6.12

The equilibrium condition gives,

$$\frac{\partial P_1^G}{\partial t} = \frac{\partial P_1^E}{\partial t} = \frac{\partial P_2^G}{\partial t} = \frac{\partial P_2^E}{\partial t} = 0$$

#### Equation 6.13

Combining the equilibrium condition with the normalization condition, we can solve for  $P_1^G$ ,  $P_1^E$ ,  $P_2^G$ , and  $P_2^E$ . Finally, the total single electron tunneling current,  $I_{DS}$ , thought the quantum dot can be expressed as,

$$\frac{I_{DS}}{e} = -P_1^G [\Gamma_{D1}^0 f_{D1}^0 + \Gamma_{D1}^1 f_{D1}^1] - P_1^E [\Gamma_{D1}^{-1} f_{D1}^{-1}] + P_2^G [\Gamma_{D1}^{-1} (1 - f_{D1}^{-1}) + \Gamma_{D1}^0 (1 - f_{D1}^0)] + P_2^E [\Gamma_{D1}^1 (1 - f_{D1}^1)]$$

# Equation 6.14

Similarly, we can derive the tunneling current at the  $N = 0 \leftrightarrow N = 1$   $(D^0 \leftrightarrow D^-)$  transition in a single donor SET. Since there is no excess electron at the N = 0 charge state, excited states of an empty quantum dot do not exist. Therefore, all the excited state tunneling lines can only originate from the excited states at the N = 1 charge states, which only terminate at the N = 1 Coulomb diamond.





Figure 6.7 Calculated charge stability diagram of a single atom transistor. (a) (b) assume symmetric tunnel barriers with  $\Gamma_{DN}^a = \Gamma_{SN}^a = 1pA/e$ , where *e* is the charge of an electron. a = 0, 1 for N = 0 and a = -1, 0, 1 for N = 1. (c) assumes asymmetric tunnel barriers ( $R_S > R_D$ ) where  $\Gamma_{DN}^a = 5\Gamma_{SN}^a = 5pA/e$ . (d) assumes asymmetric tunnel barriers ( $R_D > R_S$ ) where  $\Gamma_{SN}^a = 5\Gamma_{DN}^a = 5pA/e$ . (e) assumes symmetric tunnel junctions and the tunneling involving the excited state at N = 1 has a higher tunneling rate, i.e.  $\Gamma_{T0}^1 = \Gamma_{T1}^{-1} = 5\Gamma_{T0}^0 = 5\Gamma_{T1}^0 = 5\Gamma_{T1}^1 = 5pA/e$ , where T = S, D. (f) assumes symmetric tunnel junctions and the tunneling event involving the excited state at N = 1 has a higher tunneling symmetric tunnel junctions and the tunneling  $S_{T1}^0 = S\Gamma_{T1}^0 = 5\Gamma_{T1}^0 = 5\Gamma_$ 

2 has a higher tunneling rate, i.e.  $\Gamma_{T1}^1 = 5\Gamma_{T1}^{-1} = 5\Gamma_{T0}^0 = 5\Gamma_{T1}^0 = 5\Gamma_{T0}^1 = 5pA/e$ , where T = S, D. In all the calculations, only one excited state is assumed for each of the  $D^0$  (N = 1) and  $D^-$  (N = 2) charge states, as shown in Figure 6.6 (a). The excited state energy levels are assumed to be  $\Delta E_1 = 10$  meV, and  $\Delta E_2 = 20$  meV. The input capacitance values are  $C_S = C_D = 1.28$  aF, and  $C_G = 0.47$  aF. An artificial offset charge  $Q_0 = -0.65e$  is used to match the observed gate voltage offset in the experimental result that is to be shown in a single atom transistor in the next Chapter. The simulation temperature is taken to be T = 5 K.

In the previous analysis, we treated the tunneling rates at individual quantum dot levels as a set of input parameters. Quantifying the conductance line intensity of the excited state levels requires detailed modeling of the tunneling rates. In this section, we qualitatively illustrate the impact of the tunneling rates on the visibility of the excited state spectroscopy features.

First, the magnitude of the differential conductance lines at the excited state levels can be either positive or negative depending on the relative tunneling rate through the ground state level  $\Gamma^G$  and the excited level  $\Gamma^E$ . Because of the sequential tunneling nature of conductance, when both the ground state level  $\mu_N^G$  and the excited level  $\mu_N^E$  are within the bias window, single electrons only tunnel through one level at a time. When a single electron tunnels onto the  $\mu_N^E$  level at a tunneling rate  $\Gamma^E$ , the  $\mu_N^G$ level becomes unavailable until the single electron tunnels off the  $\mu_N^E$  level. Therefore, when the total tunneling rate with both of the ground and excited levels within the bias window is lower than the tunneling rate through the ground level alone, the differential conductance lines at the excited state becomes negative, and vice versa.

Second, the tunnel barrier symmetry between the source and drain sides affects the visibility of the excited lines. When the tunnel barriers are symmetric, the excited state conduction lines appear in both directions of the drain-source bias. Figure 6.7 (a) and (b) plot the simulated tunneling current and differential conductance charge stability diagram of a single donor SET where we assumed only one excited state for each of the  $D^0$  and  $D^-$  charge states and equal tunneling rates through the ground and excited states at the source and drain tunnel junctions. Because all tunneling rates are set to be equal, there are no negative differential conductance lines. When the tunnel barriers are asymmetric, the tunneling rate through the rate-limiting tunnel barrier dominates the total tunneling rate. Therefore, the excited state spectroscopy features are only visible when the excited state level comes in alignment with the Fermi level of the reservoir on the side of the rate-limiting barrier. In this case, the excited state differential conductance lines will have a stronger contrast in one biasing direction than the other (for the  $D^+ \leftrightarrow D^0$  transition) or running in one parallel orientation than the other (for the  $D^0 \leftrightarrow D^-$  transition). The impact of asymmetric tunnel barriers on the excited state spectroscopy features is shown in Figure 6.7 (c) and (d), where the source and drain tunnel junctions, respectively, are the rate-limiting junctions. Figure 6.7 (e) and (f) simulate the cases where the tunneling events involving the excited states at N = 1 and N = 2, respectively, have higher tunneling rates than the other tunneling events. The "V" shape features result from an increased tunneling rate when the excited level enters the bias window.

One of the most outstanding challenges of using tunneling spectroscopy to probe the intrinsic excited state spectrum of a quantum dot is that many of the extrinsic properties of the system can also introduce similar resonance features in the measured tunneling spectroscopy results. In the following section, we briefly review the signatures of DOS modulations in the source and the drain reservoir in the measured tunneling spectroscopy.



Figure 6.8 Single electron tunneling spectroscopy features due to the density of state (DOS) modulation in the source and drain reservoirs. (a) Schematic of the single electron tunneling through a discrete quantum dot level where the quasi-1D confinement in the source and drain leads gives rise to van Hove singularities. The arrows mark the energy spacings between the 1-D sub-band energy levels and the corresponding Fermi level. (b) Schematic of the resonant tunneling features outside of the blockaded regions that originate from the DOS singularities in the source and drain leads that are shown in (a).
#### **6.3.2 Resonant Features from DOS of Reservoirs**

DOS features in source and drain reservoirs can introduce resonant tunneling spectroscopy features in quantum dots. Addressing a small quantum dot requires the cross-sectional area of the source and drain leads to be similar to that of the quantum dot. The source and drain reservoirs are commonly made of a 2DEG. When the width of the leads becomes comparable or even smaller than the characteristic length scales, such as Fermi wavelength  $\lambda_F$  and mean free path l, the source/drain reservoirs are quasi-1D, where the DOS features van Hove singularities at 1-D sub-band levels. (See Figure 6.8 (a)) The tunneling rate through a discrete level on the dot is directly proportional to the reservoir DOS at the dot level.

Recall from the previous discussion that the alignment between a discrete dot level and the source (drain) Fermi level corresponds to the diamond edge with positive (negative) slopes. Similarly, the alignment between a discrete dot level and a source (drain) DOS singularity within the bias window gives rise to resonant tunneling features that run parallel with the diamond edges that correspond to the source (drain) Fermi level. [See Figure 6.8 (b)] The bias window where a DOS line joints a diamond edge represents the energy spacing,  $\Delta E_{DOS}$ , in a reservoir between the DOS singularity and the Fermi level. Within a bias window, both the filled DOS singularities in one reservoir and the empty DOS singularities in the other reservoir contribute to the DOS lines. However, for SETs with asymmetric tunnel barriers, only the DOS features through the rate-limiting barrier are visible.



Figure 6.9 Schematics of the co-tunneling process. (a) Energy diagrams of the elastic (1) and inelastic (2) co-tunneling processes at N = 1 charge state. The chemical potential levels that involve the first excited state at N = 1 are shown. A co-tunneling process involves two simultaneous tunneling events: an electron on the dot tunneling into a reservoir, and a reservoir electron tunneling into the dot. (b) Although Coulomb blockade forbids sequential single electron tunneling inside a Coulomb diamond, co-tunneling events introduce finite conductance within the Coulomb diamond. The elastic co-tunneling process becomes possible when the bias window exceeds the energy separation of the excited state,  $\Delta E_1$ . The horizontal red lines within the diamond mark the onset of the inelastic co-tunneling process. The red lines outside the diamond represent the sequential tunneling features involving the excited state  $U_1^E$ .

### 6.3.3 Co-tunneling through Excited States

Signatures of co-tunneling events can be used to identify the resonant tunneling features that originate from excited states on the dot. A co-tunneling process involves two simultaneous tunneling events: an electron on the dot tunneling into a reservoir, and a reservoir electron tunneling into the dot. When the single particle energy spacing on the dot is non-negligible comparing with the charging energy, such as the case of few-donor SETs, both the inelastic and elastic co-tunneling events are essential attributes of the co-tunneling process.<sup>171, 407</sup> Elastic co-tunneling can occur at any drain-source bias, leading to a small background conductance within the blockaded regions. At finite bias, inelastic co-tunneling becomes possible when the bias window becomes equal or greater than the excited level spacing on the dot. As shown in Figure 6.9 (a), an inelastic co-tunneling event leaves the dot in an excited state. Inelastic cotunneling conductance leads to a conductance step within the Coulomb diamond at the bias that corresponds to the excited level spacing on the dot. [See Figure 6.9 (b)] This conductance step manifests itself as a horizontal line within the Coulomb diamond in a differential conductance charge stability diagram. At Coulomb diamond edges, the inelastic co-tunneling line within the blockaded region joins the excited state lines within the transition regions. In an SET with measurable co-tunneling conductance, the co-tunneling lines can be used to distinguish excited state features from other extrinsic features.406,408



Figure 6.10 Hydrogen lithography image and charge stability diagram of a few-donor quantum dot SET-1. (a) STM images of the central region of the few-donor quantum dot SET-1 after hydrogen lithography, but before PH3 dosing. The tunnel gaps distances can be estimated by counting the number of dimer rows in the gaps. (b) Close-up STM image of the H-desorbed quantum dot region. The number of exposed Si dangling bonds (DB) and dimers can be counted by overlaying the Si (100) 2x1 surface reconstruction lattice grids with the STM images after hydrogen lithography. Based on the accepted P incorporation mechanisms,<sup>58, 140, 152, 310, 312, 409</sup> the allowed and forbidden P incorporation sites are highlighted in green and red respectively. (c) and (d) plot the low-temperature (T=4 K) differential conductance charge stability diagram in linear (c) and logarithmic (d) color scales. Resonant tunneling features [marked by arrows in (c)]

are visible running parallel to the Coulomb diamond edges. The occupation number of the dot is expressed using an integer N. In (d), co-tunneling features are visible within the Coulomb diamonds at positive gate voltages.

### **6.3.4 STM-patterned Few-donor Quantum Dots**

Following the same methods as described in previous sections, here we fabricate and characterize two STM-patterned SETs (SET-1 and SET-2) in the few-donor quantum dot regime where the source/drain lead width and island sizes are on the order of a few nanometers. Figure 6.10 illustrates the STM lithography pattern and low-temperature charge stability diagram of SET-1. From the high-resolution STM image in Figure 6.10 (a), we can determine the tunnel gap distances to be ~8 dimer rows on the drain side and ~7 dimer rows on the source side, which is comparable to the gap distances in SET-B that we previously studied in the metallic regime (see Figure 6.2). While Coulomb blockade was not observed in SET-B at low-temperature electrical measurement of SET-1 demonstrate clear Coulomb blockade behavior [see Figure 6.10 (c), (d)] with tunneling resistances on the order of mega-ohms, highlighting the impact of island size and source/drain lead width on the tunnel coupling at the atomic scale.

We estimate the number of donors in the quantum dot by counting the number of hydrogen-desorbed dimer sites that are available for P incorporation [see Figure 6.10 (b)]. While it is possible to directly count the number of incorporated donors by taking high-resolution STM images after P incorporation anneal, we avoid this timeconsuming step to minimize the risk of surface contamination. As has been reviewed in Chapter 2, at least 3 adjacent H-desorbed dimers within a dimer row are necessary to incorporate one P donor. In Figure 6.10 (b), we identify the potential dimer sites for P incorporation sites using green ellipses. For saturation dosed blanket Si:P  $\delta$ -layers, we reliably obtain a P incorporation density of ~0.25 ML, representing an upper bound of the incorporation density in the quantum dot. Fuchsle *et al.*<sup>396</sup> have found that the P incorporation density in nm scale desorbed areas decreases significantly due to competition for dangling bond sites to lose H atoms from absorbed PH<sub>x</sub> (x=1, 2) during incorporation. We estimate the lower bound for incorporated P donors in a quantum dot by exclusively taking 3 contiguous dimers to incorporate a single P donor. For SET-1, there are 25 desorbed dimers available for P incorporation, with 9 dimers in the first two dimer rows and 7 dimers in the third dimer row. We estimate that there are 8 to 12 donors incorporated in this quantum dot. However, because of the statistical nature of the phosphine adsorption, dissociation, and incorporation processes, electrical characterization is needed to determine the actual number of incorporated donors.

Figure 6.10 (c) and (d) illustrate the charge stability diagram of SET-1 that is measured at 4 K. The height of each Coulomb diamond represents the addition energy,  $E_{add} = E_c + \Delta E$ , where  $E_c$  is the charging energy and  $\Delta E$  is the single particle level spacing. Comparing with the previously studied SETs with larger islands in the metallic regime, the addition energy of the quantum dot increases significantly due to its reduced dot size. As can be seen in Figure 6.10 (d), co-tunneling signatures become apparent within the blockaded regions at positive gate voltages. Also, several resonant tunneling features are visible outside of the blockaded regions at negative gate voltages, as marked by white arrows in Figure 6.10 (c). Regardless of whether these resonant tunneling features originate from excited states on the dot or quantized DOS levels in source/drain reservoirs, the observation that they all run in the same parallel orientation with positive slopes may indicate that the total tunnel conductance is limited by the tunnel junction on the drain side, in good agreement with the estimated tunnel gap distances in Figure 6.10 (a).



Figure 6.11 Hydrogen lithography image and charge stability diagram of a few-donor quantum dot SET-2. (a) (b) (c) and (d) follow the conventions in Figure 6.10.

We demonstrate a second recent STM-patterned few-donor Si:P quantum dot (SET-2) in Figure 6.11. While maintaining approximately the same tunnel gap distances as those

in SET-1 [see Figure 6.11 (a),  $\sim 8$  dimer rows on the drain side and  $\sim 9$  dimer rows on the source side], we further reduce the H-desorbed area of the quantum dot [see Figure 6.11 (b)]. Following the previous convention, we estimate the number of incorporated P donors in the dot to range from 2 to 4. From the charge stability diagram of SET-2 that is measured at 4 K (Figure 6.11 (c) (d)), we extrapolate the addition energy to be ~104 meV and ~126 meV for the N and N+1 electron occupancy, which are comparable to each other and dramatically higher than the addition energy ( $\sim 65$  meV) for the N+2 electron occupancy. In addition, we observe the tunnel coupling drops significantly from the N+2 to the N+1 and N electron occupation. We speculate that the N and N+1charge states occupy the same spin-degenerate orbital, while the N+2 charge state occupies the next orbital with a larger spatial wavefunction extension. In Figure 6.11 (d), as indicated by arrows at the  $N \leftrightarrow N + 1$  transition, we observe symmetric resonant tunneling features in terms of positive and negative biases, which indicates approximately equal tunnel coupling through the drain and source tunnel junctions [see simulated results in Figure 6.7 (b)]. The enhanced differential conductance in "V" shapes, as indicated by red arrows in Figure 6.11 (d), indicates higher tunneling rates through an excited state than the tunneling rates through the ground state [see simulated results in Figure 6.7 (f)]. The resonant tunneling feature as marked by the black arrow in Figure 6.11 (c) remains to be explained. We are currently working in collaboration with Dr. Bryant Garnett and Dr. Ehsan Khatami to understand the atomic and electronic structures of our fabricated few-donor quantum dots from the perspectives of tightbinding and Hubbard model simulations.

## 6.4 Charge Sensing in Atomically-defined Few-donor Quantum Dots

Single shot spin readout in the solid state was first demonstrated by Elzerman et al.<sup>410</sup> in GaAs/AlGaAs systems using a quantum point contact (QPC) as a charge sensor. Morello *et al.*<sup>36</sup> have adapted Elzerman's protocol and reported the first single shot spin readout of single P donors in Si using an electrostatically defined SET,<sup>36, 411</sup> where single phosphorus atoms were ion-implanted near the SET region and anneal-activated thereby establishing both capacitive and tunnel coupling with the SET island. The SET island serves both as a charge sensor and an electron reservoir that allows high fidelity and fast single-shot spin-readout. Following this seminal work by Morello et al., Mahapatra, Buch *et al.*<sup>44, 45</sup> later demonstrated the first charge sensing and spin readout using STM-patterned phosphorus-donor clusters [See Figure 6.12 (a)]. Single shot spin readout is a two-step process. First, the spin state is converted into a charge state. Subsequently, the charge state is read out using a charge sensor. As a first step towards demonstrating spin-readout and spin manipulation in atomically defined single/fewdonor quantum dots, in this section, we demonstrate charge sensing in STM-defined few-donor quantum dots and characterize the tunnel coupling between the few-donor quantum dots and precision aligned single electron charge sensors.

### 6.4.1 Charge Sensing using Single Electron Transistors



Figure 6.12 Charge sensing of a donor-cluster qubit using a single electron transistor (SET). (a) Schematic device architecture to readout the spin of a donor cluster qubit. The donor cluster qubit is tunnel- and capacitively coupled to the SET charge sensor island. (b) Equivalent circuit under the constant interaction model. (c) Simplified energy level diagram. (d) Simulated charging energy variations as a function of donor-dot separation. See Equation 6.16 for the charging energy definitions of  $E_{C1}$ ,  $E_{C2}$ , and  $E_m$ . (e) (f) simulated differential conductance lines in gate space at zero drain-source bias by setting the donor-dot separations to be 10 nm in (e) and 15 nm in (f). The chemical potential level of the SET island (donor cluster) aligns with the source/drain Fermi level on the red (blue) lines. The chemical potential levels of the SET island and the donor clusters are aligned on the green lines. Examples of the occupation numbers of the SET island and the donor cluster are denoted in the format (N, n) in (e). The arrow represents an example of  $V_{G1}$  and  $V_{G2}$  gate voltage sweeping trajectory for

performing single shot spin readout at a charge transition on the donor cluster where the transmitted electron is unpaired in an orbital shell.

To use the SET as a charge sensor, the first step is to map out the SET conduction lines in the gate-gate parameter space. Figure 6.12 (b) and (c) illustrate schematics of the equivalent circuit under the constant interaction model and a simplified energy level diagram, respectively. While both the SET island and the donor cluster are capacitively coupled to both gates, Gate 1 dominates the capacitive coupling to the SET island and Gate 2 dominates the capacitive coupling to the donor cluster. The electrochemical potential of the SET island and the donor cluster can be expressed as,

$$\mu_{1} = \left(N_{1} - \frac{1}{2}\right)E_{C1} + N_{2}E_{m} - \frac{1}{e}\left[\left(C_{11}E_{C1} + C_{12}E_{m}\right)V_{G1} + \left(C_{22}E_{m} + C_{21}E_{C1}\right)V_{G2}\right]$$
  
$$\mu_{2} = \left(N_{2} - \frac{1}{2}\right)E_{C2} + N_{1}E_{m} - \frac{1}{e}\left[\left(C_{12}E_{C2} + C_{11}E_{m}\right)V_{G1} + \left(C_{21}E_{m} + C_{22}E_{C2}\right)V_{G2}\right]$$
  
Equations 6.15

where  $E_{C1}$  and  $E_{C2}$  are the charging energy of the SET dot and the donor dot, respectively.  $E_m$  is the mutual charging energy between the donor cluster and the SET island, which represents the change in the energy of the donor cluster (SET island) when an electron is added to the SET island (donor cluster).

$$E_{C1} = e^2 \frac{C_{\Sigma 2}}{C_{\Sigma 1}C_{\Sigma 2} - C_m^2}$$
$$E_{C2} = e^2 \frac{C_{\Sigma 1}}{C_{\Sigma 1}C_{\Sigma 2} - C_m^2}$$
$$E_m = e^2 \frac{C_m}{C_{\Sigma 1}C_{\Sigma 2} - C_m^2}$$

Equations 6.16

And  $C_{\Sigma 1}$  and  $C_{\Sigma 2}$  are the total capacitance of the SET dot and the donor cluster,

$$C_{\Sigma 1} = C_{11} + C_{21} + C_{S1} + C_{1D} + C_m$$
$$C_{\Sigma 2} = C_{12} + C_{22} + C_{S2} + C_{2D} + C_m$$

#### Equations 6.17

Figure 6.12 (e) and (f) plot the simulated charge stability diagram in the gate-gate voltage space, taking calculated capacitance values as inputs. The charge-sensing device design in Figure 6.12 (a) is essentially a double dot system in a parallel configuration, where the tunnel coupling from the source and drain leads to the donor cluster is negligibly small. Therefore, only the SET conduction lines [red lines in Figure 6.12 (e) & (f)] are experimentally visible in the gate-gate sweep map, representing charge transitions on the SET island. The terminals at the discontinuities of the SET conduction lines are triple points where the electrochemical potential of the donor cluster  $(\mu_2)$ , the SET island  $(\mu_1)$ , and the source-drain leads  $(\mu_0)$  are aligned, and electrons are allowed to transit among these three components. The green lines connecting the two triple points within the same discontinuity are charge transition lines where electrons tunnel between the SET island and the donor cluster. The donorleads charge transition lines (blue lines) connecting triple points between subsequent discontinuities in the direction of the Gate 2 axis are typically invisible experimentally due to the weak tunnel coupling between the donor cluster and the leads. The charge state of the system can be denoted as (N, n), see Figure 6.12 (e), where N is the integer number of charges on the SET island and n is the integer number of charges on the donor cluster. As the donor cluster's chemical potential is brought across the chemical potential of the SET island, a single charge transition event occurs over a time scale

that is set by the tunneling rate between the donor cluster and the SET island. This charge state transition on the donor cluster alters the electrochemical potential on the SET island through the mutual capacitance coupling between them, resulting in a discrete shift of the SET conduction lines on the Gate 1 axis. The essential idea of SET charge sensing is to detect the change in conductance through the SET island in response to the change in the donor cluster's charge state.



Figure 6.13 STM images of the central parts of charge-sensing/spin-readout devices that have been fabricated and are currently in the process of being electrically measured. (b) (c) (d) To optimize the spin readout fidelity and speed, we have

fabricated a series of donor-cluster spin-readout devices with different separations between the donor cluster and the SET island.

#### 6.4.2 Few-donor Quantum Dots with Precision Aligned Charge Sensors

One of the critical challenges in designing a high-fidelity, high-speed charge sensor is to optimize the separation between the donor cluster and the SET island. From the perspective of capacitance coupling, the shift in SET conduction lines in response to a single charge transfer at the donor cluster is proportional to  $\Delta q/e$ , where  $\Delta q$  is the induced charge on the SET island due to a charge transfer at the donor cluster. Therefore, to increase the charge sensitivity, it is preferable to place the donor cluster close to the SET island for increased mutual capacitance [see simulated results in Figure 6.12 (d) (e) (f)]. From the perspective of tunnel coupling, a smaller separation allows higher charge transfer (tunneling) rates between the donor cluster and the SET island reservoir, which is preferable for high-speed spin readout operations. However, as will be seen in the following section, the tunneling rate should not be too high or it will compromise fidelity in the spin-readout. As shown in Figure 6.13, we have fabricated a series of charge sensing and spin-readout devices with different separations between the donor cluster and the SET island to explore the impact of atomically defined tunnel coupling on single electron charge sensing and spin selective-readout.



Figure 6.14 Charge offset lines in the Coulomb blockade diagram (a) and gate-gate map (b) of a SET charge sensor. The hydrogen-lithography pattern of the measured charge sensor is shown in Figure 6.13 (d). The gate-gate map in (b) is acquired by

monitoring the drain-source current at a constant drain-source bias of 5 mV and sweeping the Gate-2 voltage at each Gate-1 voltage. Charge transitions at the few-donor quantum dot give rise to four charge offset lines as indicated by red triangles in both graphs.  $N_{donor}$  represents the number of excess electrons on the few-donor quantum dot. The electrical measurements are carried out at a base temperature of T = 20 mK. The typical data acquisition time for generating the plots in (a) and (b) is ~15 hours.

Taking the charge sensing device shown in Figure 6.13 (d) for example, we first measure the Coulomb blockade diagram of the SET charge sensor [see Figure 6.14 (a)]. We observe four charge offset lines (as indicated by red triangles) that correspond to charge transitions on the few-donor quantum dot. The four charge offset lines in the Coulomb blockade diagram have similar slopes, indicating the charge transitions occur at the same charge center (i.e. the few-donor quantum dot). Figure 6.14 (b) shows the gate-gate map (in the 2-D gate voltage space spanned by  $V_{GS1}$  and  $V_{GS2}$ ) of the drain-source current at a constant drain-source bias (5 mV), where each SET conduction line represents a charge state transition on the SET island and the offset discontinuities at SET conduction lines represent charge transitions on the quantum dot. Due to the negligible tunnel coupling between the source/drain leads and the few-donor quantum dot, drain-source conduction lines through the quantum dot are not visible in the gate-gate map.



Figure 6.15 Optimizing the charge sensing path in gate voltage space. (a) After taking a gate-gate map near a charge transition ( $V_{DS} = 3 \text{ mV}$ ), single-line scans are taken in the gate voltage space scanning from a fixed starting point ( $V_{01}, V_{02}$ ) to ending points ( $V_{01} - \Delta V_{GS1}, V_{02} + \Delta V_{GS2}$ ). In this case, the starting point is chosen to be on a SET conduction line,  $\Delta V_{GS1}$  is kept constant, and  $\Delta V_{GS2}$  is treated as a variable. (b) The measured current ( $V_{DS} = 5 \text{ mV}$ ) along scan paths is plotted against  $V_{GS1}$  at different  $\Delta V_{GS2}$ . The optimal range of  $\Delta V_{GS2}$ , at which the paths are along the direction of SET conduction lines, is identified by the shaded region.

Scanning in the gate voltage space across a discontinuity along a SET conduction line will bring the chemical potential of the quantum dot to the same level as the chemical potential of the SET island reservoir, resulting in loading or unloading of a single electron onto or from the quantum dot. The occurrence of a charge transition event is revealed by a sudden change in the SET conductance. Scanning in gate voltage space along the direction of SET conduction lines ensures that the chemical potential of the SET charge island (and therefore the charge sensor signal) is unaffected by the gate

voltage and responds only to charge transitions on the quantum dot. As can be seen in Figure 6.14 (b), the slopes of the SET conduction lines vary due to differences in the capacitance coupling of the SET island to Gate-1 and Gate-2 in the gate voltage space. To ensure the charge sensing path is along the SET conduction line, we plot the SET current over a range of scan directions in the gate-voltage space, starting at a fixed point on a SET conduction line (see Figure 6.15). The optimized range of the charge sensing path is shaded in Figure 6.15 (b).



Figure 6.16 Probing the characteristic tunneling time between few-donor quantum dots and SET charge sensors. The separation between the few-donor quantum dot and the

SET island is about 15 nm [see Figure 6.13 (b)]. (a) Gate-gate map of the SET current at a discontinuity in an SET conduction line. The charge sensing path is indicated by the dashed double-arrow line. (b) Monitoring the SET current while ramping slowly across the discontinuity in gate voltage space. (c) Upper panel: the applied gate voltage pulse sequence for measuring the characteristic tunneling time; Middle and lower panels: examples of representative SET current response during a single gate voltage pulse. (d) SET current response averaged over 1000 cycles of gate voltage pulses and exponential fits to the averaged current response to the loading and unloading events. The uncertainties in the best-fit time constants represent 95% confidence intervals. The electrical measurements are carried out at a base temperature of T = 20 mK.

To characterize the time scale of the tunneling events between the few-donor quantum dot and the SET island, we pulse the gate voltage across a charge transition level on the quantum dot and monitor the charge sensing current in the time domain (see Figure 6.16). As can be seen in Figure 6.16 (c), the on and off states of the SET current, which represents the loading and unloading of an electron from the quantum dot, can be detected in real-time. The time delay between the voltage pulse edges and the current response represents the waiting time before a tunneling event occurs. The characteristic tunneling time can be extracted by averaging the current responses from a large number of voltage pulse cycles and followed by an exponential-fit of the averaged current response [see Figure 6.16 (d)]. In this example, we obtain the time constants for loading and unloading tunnel events as  $\tau_{load} = 288 \pm 3 \text{ ms}$  and  $\tau_{unload} = 388 \pm 5 \text{ ms}$ . Adjustment of these tunneling time constants can be achieved by fine-tuning the

amplitude of the gate voltage pulse along the charge sensing path thereby altering the position of the chemical potential level of the quantum dot with respect to the SET island's Fermi level.

## **6.5 Chapter Summary**

In summary, we have reported atomic scale control over the tunnel coupling in STMpatterned Si:P single electron transistors. By using the natural surface reconstruction lattice as an atomic ruler, we systematically varied the tunneling gap distances with atomic precision and demonstrated exponential scaling of tunneling resistance to the atomic limit. We characterized the tunneling resistance difference in a pair of nominally identical tunnel junctions that correspond to half a dimer row pitch difference in tunnel gap distances. We demonstrated successful fabrication of STM-patterned Si:P fewdonor quantum dots with atomic-precision defined tunnel gaps and analyzed the resonant tunneling spectroscopy through atomic-scale tunnel coupling. Finally, we presented single electron charge sensing in few-donor quantum dots using precisionaligned single electron charge sensors and characterized the single electron loading and unloading time constants on and off the few-donor quantum dots. These results are an important step towards atomic precision design and engineering of tunnel coupled nano-scale components needed for donor-based solid-state quantum computing and analog quantum simulation in silicon.

## **Chapter 7: Conclusions and Future Work**

This thesis covers several critical scientific and technological advances in atomically precise fabrication and characterization that not only demonstrated success in fabricating and characterizing state of the art atomically-precise silicon-phosphorus (Si:P) quantum devices in the Silver Group but also presented essential steps towards fully realizing scalable donor-based silicon quantum computing and quantum simulation. Through detailed process development and optimization, in Chapter 3, we demonstrated successful implementation of an optimized atomically precise fabrication scheme with emphasis on technological advances and process control strategies in lowtemperature device encapsulation overgrowth, device registration/contact alignment, and silicide electrical ohmic contact formation, etc. that improve device quality at the atomic scale and drastically increase atomic-precision fabrication yield. We summarized our optimal process parameters in each fabrication step as well as lessons that we have learned during process development and in the transition from  $\delta$ -doped to STM-patterned Si:P device fabrication, highlighting the importance of a near-perfect UHV environment as well as the need for contamination-free Si surfaces and STM tips to achieve success in atomically precise fabrication. We demonstrated examples of high-quality electrical characteristics of our blanket-doped and STM-patterned Si:P devices to validate the optimized fabrication processes that have been developed in our lab during this thesis work.

In atomically precise fabrication in silicon, the universal presence of single layer step edges, at Si (100) surfaces/interfaces and at the low-temperature epitaxial growth front, modifies the local electrostatic environment at the atomic scale and presents significant challenges to quantitative characterization of buried dopant devices as well as accurate imaging and re-location of fabricated quantum structures. In Chapter 4, we demonstrated the first detailed spatially resolved scanning tunneling spectroscopy study across monolayer step edges on Si (100) surfaces and quantitative determination of the local density of states distributions and behavior of the band gap at step edges. We characterized the influence on the local electrostatic environment due to step edge states while fully taking into account the effects of scanning tunneling measurement conditions. We utilized the dangling bond states on Si (100) surfaces as a fingerprint to quantify the local band bending landscape and to make corrections to the experimentally observed surface state energy levels and band gap values at the step edge regions. We observed a significant band gap narrowing behavior along a rebonded SB step edge on a degenerately boron-doped Si substrate. Through detailed elucidation of the local electronic environment near monolayer step edges, this study provides insights into the electronic behavior of atomic structures near atomic step edges at surfaces or interfaces as well as the underlying mechanisms of the step edge effects in epitaxial encapsulation overgrowth in donor-based atomic-precision fabrication.

A significant remaining challenge in donor-based atomically precise fabrication in silicon is to suppress unintentional dopant movement at the atomic scale during device encapsulation overgrowth at low-temperatures. Uncontrolled dopant segregation, diffusion, surface roughening, and defect formation during the encapsulation overgrowth introduce large uncertainties to the exact dopant placement as well as the dopant's electrical activation. In Chapter 5, we have developed a unique method by combining dopant segregation/diffusion models with sputter profiling simulation to monitor and control, at the atomic scale, dopant movement using roomtemperature grown locking layers (LL). Using Si:P monolayer systems, an overgrowth testbed where the dopant behavior is directly tied to the deterministic placement of single dopants, we explored the impact of LL growth rate, thickness, rapid thermal anneal, surface accumulation, and growth front roughness on dopant confinement, local crystalline quality, and dopant electrical activation within Si:P monolayers. We demonstrated that dopant movement can be more efficiently suppressed by increasing the LL growth rate than by increasing the LL thickness. We found that the dopant segregation length can be suppressed below a single Si lattice constant by increasing LL growth rates at room temperature while maintaining good epitaxy. Although dopant diffusivity within the LL is found to remain high (on the order of  $10^{-17}$  cm<sup>2</sup>/s) even below the hydrogen desorption temperature, we demonstrated that exceptionally sharp dopant confinement with high electrical quality within Si:P monolayers can be achieved by combining a high LL growth rate with a low-temperature LL rapid thermal anneal. We examined the effect of Si:P monolayer confinement on the weaklocalization signal in parallel and perpendicular magnetic fields. We found good agreement between the weak localization measured electrical thickness with the sputter-profiling quantified dopant distribution at the atomic-scale, demonstrating weak-localization measurement as a high-resolution, high-throughput, and nondestructive method in determining the conducting layer thickness in the sub-nanometer thickness regime. By taking temperature-dependent phase coherence length measurements, we have verified the advantage of using the LL technique in creating high-quality 2-D electrical confinement. The fabrication and characterization methods developed in this chapter provide key tools for suppressing and quantifying dopant movement at the atomic scale for the purpose of fabricating donor-based quantum devices in silicon with atomic precision.

A fundamental requirement for the scalability and performance of donor-based silicon quantum systems is the atomically precise control of tunnel coupling for highfidelity spin readout/initialization and tunable exchange coupling in multi-qubit gate operations and quantum simulations. In Chapter 6, we have achieved unprecedented control of atomic-scale tunnel coupling, in a systematic and reproducible manner, by defining the tunnel gap geometry with atomic precision using ultra-clean STM hydrogen lithography and suppressing atomic-scale dopant movement during device encapsulation using the advances in locking layer epitaxial overgrowth techniques that we developed in Chapter 5. We reported the first demonstration of the exponential scaling of tunnel coupling down to the atomic limit in doped nanostructures in silicon by using the Si (100) 2x1 surface reconstruction lattice as a natural nanometrology ruler with atomic-scale accuracy and by intentionally varying the number of lattice counts in the tunnel gaps of atomically precise single electron transistors. We characterized the tunnel coupling asymmetry in a pair of nominally identical tunnel junctions due to atomic scale variations, substantiating the impact on tunnel resistances from even half a dimer row variation in STM-defined tunnel gap distances. We scaled the single electron transistor island size and electrode width down to the atomic scale and demonstrated successful fabrication and characterization of STM-patterned few-donor quantum dots with atomically precise tunnel junctions. Combining low-temperature electrical transport measurement with single charge tunneling simulations, we presented detailed resonant tunneling spectroscopy analysis through few-donor quantum dots and illustrated the effects due to the excited states of the quantum dots and the density of states modulation of the source/drain reservoir on the coupling through tunnel gaps at the atomic scale. Finally, by combining single/few-donor quantum dots with atomically defined single electron transistors as charge sensors, we demonstrated single electron charge sensing in few-donor quantum dots and characterized the tunnel coupling between few-donor quantum dots and precisionaligned single electron charge sensors. Our results presented in this chapter demonstrate a key capability to design and engineer tunnel coupling with atomicprecision, a necessary requirement for successful implementation of scalable donorbased quantum computing and analog quantum simulation in silicon.

## 7.1 Future work

The results reported in this thesis represent important steps toward the realization of donor-based silicon quantum computing and analog quantum simulation in our group. In this section we detail experiments that are currently underway to control atomically precise donor qubits in silicon.

### 7.1.1 A Single Atom Transistor

Recently, Dr. Jonathan Wyrick in our group has successfully fabricated an STMpatterned single atom transistor (see Figure 7.1), demonstrating our capability of fabricating single donor qubits for spin readout and manipulation.



Figure 7.1 A single atom transistor that was fabricated by Jonathan Wyrick and measured by Ranjit Kashid at 4 K and by Xiqiao Wang at 20 mK base temperature. (a) High resolution STM image of a donor quantum dot after hydrogen lithography. (b) (c) Experimental charge stability diagram measured at T=4 K, which is plotted in linear (b) and logarithmic (c) color scales. The three charge configurations  $(D^+, D^0, \text{ and } D^-)$  of a single donor are labeled in (b).

## 7.1.2 Donor Qubit Electron Spin Readout

Having demonstrated single electron charge sensing, we are currently working on robust demonstration of high-fidelity spin readout in single/few-donor quantum dots. In a spin-to-charge conversion, an electron in an up or down spin state can either tunnel out of the donor into a reservoir, leaving behind a positively charged donor, or remain on the donor, leaving an uncharged dot (see Figure 7.2).



Figure 7.2 Schematic illustration of energy selective spin-to-charge conversion. Under a constant external magnetic field  $B_0$ , the energy level of the spin qubit and the metallic energy spectrum in the SET island split by Zeeman energy  $\Delta E_Z$ . The spin-up and spindown levels are shown in pink and blue respectively. See the main text for operation details.

A static magnetic field  $B_0$  is applied to create a Zeeman splitting between the energy levels of a spin-up and spin-down electron.

$$\Delta E_Z = E_Z^{\uparrow} - E_Z^{\downarrow} = g_e \mu_B B_0 S_Z^{\uparrow} - g_e \mu_B B_0 S_Z^{\downarrow} = g_e \mu_B B_0$$
Equation 7.1

Where  $g_e$  is the electron spin gyromagnetic ratio,  $\mu_B$  is the Bohr magneton, and  $S_Z^{\uparrow} = \frac{1}{2}$  and  $S_Z^{\downarrow} = -\frac{1}{2}$  are the electron spin antiparallel and parallel to  $B_0$ . Taking the free electron  $g_e$  factor to be 2,  $g_e \mu_B = \gamma_e = 116 \,\mu\text{eV/T}$ , which corresponds to 28 GHz/T for spin control using an oscillating magnetic field.

In an energy-selective spin-to-charge conversion, the electrochemical potential of the spin-up  $(\mu_2^{\uparrow})$  and spin-down  $(\mu_2^{\downarrow})$  qubit states are positioned on either side of the

electrochemical potential of the SET island  $(\mu_1)$ , such that  $\mu_2^{\downarrow} < \mu_1 < \mu_2^{\uparrow}$ . Only an electron with the spin state on the upper energy level is allowed to tunnel off of the donor and into the reservoir. In this method, a high degree of spin selectivity requires the Zeeman splitting to be large compared with the thermal broadening at the reservoir's Fermi level,  $\Delta E_Z \gg k_B T$ , where *T* is the electron temperature. In addition, the single particle energy spacing  $\Delta E$  on the SET island is required to be much smaller compared to the Zeeman splitting in order to ensure that, in the readout phase, the SET island has an empty spin-up state available to receive a spin-up electron from the donor while having a filled spin-down state available to subsequently tunnel into the donor,  $\Delta E_Z \gg \Delta E$ .<sup>411</sup> Therefore, it is advantageous to have a relatively large SET island charge sensor in single shot spin readout applications (see our SET design in Figure 6.13).

To read out the spin states of a single electron that is bound to a single phosphorus donor, the  $V_{G1}$  and  $V_{G2}$  gate voltages are repeatedly swept across the donor cluster charge transition line in the direction parallel to the SET conduction lines while monitoring the response in SET conductance according to the load/readout/empty cycle described below. Sweeping parallel to the direction of the SET conduction lines ensures that the electrochemical potential of the SET is kept fixed. For charge sensing of a donor cluster, assuming the electron states on a donor cluster are filled up obeying the Pauli principle, spin readout can only occur at a charge transition where the transmitted electron is unpaired in a new orbital shell. For the charge stability diagram, the single electron is paired up after being loaded on a half-filled orbital (both the spin-up and spin-down levels are occupied), preventing the spin states from being read out.

Following the three-step single shot spin readout protocol by Elzerman *et al.*,<sup>410</sup> we illustrate the energy selective spin-to-charge conversion in Figure 7.2, taking the electron spin on a single donor as an example.

• Load

When the donor is empty, set the gate voltages within the domain of  $(N_1, 1)$  so that both the Zeeman-split chemical potential levels,  $\mu_2^{\uparrow}$  and  $\mu_2^{\downarrow}$  are pulled far below the chemical potential level of the electron reservoir  $\mu_1$ . After a characteristic tunnel time,  $1/\Gamma$ , an electron from the SET island will tunnel into either the  $\mu_2^{\uparrow}$  or  $\mu_2^{\downarrow}$  state on the donor. Once the donor is loaded with an electron (donor charge state transition  $0 \Rightarrow 1$ ), it electrostatically raises the chemical potential level of the SET dot above the sourcedrain level and switches the SET conduction current. The change in SET conductance at this stage signals that an electron has been successfully loaded onto the donor.

• Readout

The gate voltages are now positioned on the donor-reservoir transition line that connects the two triple points, where, in the case of B = 0, the chemical potential of the donor, SET dot, and the leads are aligned with each other. At  $B \neq 0$ , the Zeeman energy splits the donor's electrochemical potential into the  $\mu_2^{\uparrow}$  level above the electron reservoir  $\mu_1$  and the  $\mu_2^{\uparrow}$  level below  $\mu_1$ . If the donor electron is spin-up after load, it is energetically favorable for it to tunnel into the electron reservoir after a characteristic tunnel time. This charge state transition  $1 \Rightarrow 0$  on the donor alters the electrochemical potential on the dot  $\mu_1$ , and therefore giving a step change in the SET conductance: the SET senses a spin-up state. After the  $1 \Rightarrow 0$  charge transition on the donor, if the electron reservoir level  $\mu_1$  remains between the  $\mu_2^{\uparrow}$  and  $\mu_2^{\downarrow}$  levels, then an electron can subsequently tunnel back into the  $\mu_2^{\downarrow}$  state, restoring the donor charge state as well as the SET conductance after the characteristic tunnel time. This characteristic tunnel time must be long enough to ensure high fidelity detection of the  $1 \Rightarrow 0$  charge transition for the spin-up state. On the other hand, if the donor electron is spin-down after load, then the electron is energetically favorable to remain on the donor, and no charge transition events will be detected during the period of the read.

• Empty

Here the gate voltage is positioned into the  $(N_1 + 1,0)$  domain so that both the  $\mu_2^{\uparrow}$ and  $\mu_2^{\downarrow}$  levels are brought above the electron reservoir's Fermi level  $\mu_1$ . After a characteristic tunnel time, the donor is emptied regardless of the spin state of the donor electron. A switching event is detected in the SET conductance as a signal of the charge state transition  $1 \Rightarrow 0$  on the donor. This load-readout-empty gate voltage pulse sequence is repeated to measure the relative probabilities of the two spin states.



Figure 7.3 Examples of measurement results of an STM-patterned device [similar to the one shown in Figure 6.13 (b)] demonstrating two types of charge sensing current response during read. Base temperature: ~20 mK. Magnetic field: 4 T. Note, in this example, the SET current switches on when an electron is loaded onto the few-donor quantum dot.



## 7.1.2 Donor Qubit Electron Spin Control

Figure 7.4 Spin control using microwave pulses. (a) Schematic of a microwave antenna near the qubit to generate oscillating magnetic field  $B_1$  at the qubit site that is perpendicular to the static magnetic field  $B_0$ . (b) (c) (d) Schematic illustration of the control, readout, and initialization of an electron spin qubit.

After a demonstration of high-fidelity spin readout, the immediate next step is to demonstrate spin manipulation for quantum computing applications. The rotation of spin on the Bloch sphere is driven by applying an AC magnetic field  $B_1$  at the Larmor frequency of the Zeeman split. (See Figure 7.4) The Rabi oscillation frequency of the spin rotation on the Bloch sphere is determined by the oscillation amplitude of the perpendicular magnetic field,  $f_{Rabi} = \gamma_e B_1/h$ . Experiments are currently underway in our group to implement the spin manipulation scheme in Si:P systems that was first demonstrated by Morello *et al.* using implanted dopant atoms.<sup>379</sup>

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