

ABSTRACT

Title of Dissertation: DEVICE DEVELOPMENT AND
 CHARACTERIZATION FOR
 SOLID-STATE QUANTUM COMPUTATION

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Solid-state quantum computing devices are among the most promising candidates for realizing quantum computers, due to the characteristics that they are more versatile and more easily scalable compared to other implementations, and the anticipated integration with existing silicon device fabrication and nanoscale technology. In the solid-state quantum computing field, superconducting and semi-conducting qubits have achieved tremendous progress. However, there still exist issues such as material instabilities, device vulnerabilities, fabrication complexities, measurement noise, etc., that hinder the performance improvement in the device level. In addition, the future of large scale quantum computing relies on efficiently transducing quantum information between different bases, which requires mutually compatible devices and materials.

In this thesis, I report on the device development and characterization for solving issues and improving performance in two solid-state quantum computing fields –

superconducting and semiconducting, and finally propose and evaluate a device architecture of compatibly integrating these two types of quantum computing devices for qubit implementation. For superconducting quantum computing, the material instability of aluminum oxide (AlO_x), which is thought to be a decoherence source in superconducting quantum computing circuits, is remarkably mitigated on single-electron devices with $\text{Al}/\text{AlO}_x/\text{Al}$ tunnel junctions. By employing plasma oxidation and ultra-high vacuum (UHV) chambers, one manifestation of AlO_x instability – the long-term charge offset drift of $\text{Al}/\text{AlO}_x/\text{Al}$ single-electron transistors (SETs) is significantly reduced (best $\Delta Q_0 = 0.13 \text{ e} \pm 0.01 \text{ e}$ over ≈ 7.6 days and no observation of ΔQ_0 exceeding 1 e), compared to the results of devices with conventionally fabricated $\text{Al}/\text{AlO}_x/\text{Al}$ tunnel junctions in previous studies (best $\Delta Q_0 = 0.43 \text{ e} \pm 0.007 \text{ e}$ over ≈ 9 days and most $\Delta Q_0 \geq 1 \text{ e}$ within one day). For semiconducting quantum computing, robust single metal gate layer metal-oxide-semiconductor (MOS) quantum dot devices are developed for improving fabrication efficiency and reducing failure modes, with sufficient device performance for diagnostic qubits. No failures with gate voltage excursions $> 10 \text{ V}$ are observed. Quantum dot formation, capacitive charge sensing with signal-to-noise ratio ($\text{SNR} > 5$) sufficient for spin readout, and reasonable effective electron temperatures ($T_e \approx 200 \text{ mK}$) that enable spin qubit studies, are demonstrated. Along the device development, measurement noise that determines the performance of device characterization is also studied and improved. The noise level in a dilution refrigerator with $\approx 10 \text{ mK}$ base temperature is substantially lowered from $\approx 4 \text{ K}$ to $< 0.5 \text{ K}$. Finally, the device design, modeling, and theoretical calculations of integrating the charge stability improved $\text{Al}/\text{AlO}_x/\text{Al}$

SETs with the streamlined, robust silicon MOS quantum dots are presented for advancing an integrated solid-state qubit platform. An analytical method is proposed to evaluate the device feasibility and find the optimal operating point for performing charge sensing and spin readout, which can be used to optimize device design and guide experimental measurement for better qubit performance in versatile spin qubit scenarios. Via increasing the charging energy of the charge sensor by a factor of 2, the SNR at the optimal operating point can be improved by a factor of ≈ 6 . These achievements together are building blocks to implement an integrated solid-state qubit platform integrating semiconducting and superconducting devices, with the capability of transducing quantum information between different bases.

DEVICE DEVELOPMENT AND CHARACTERIZATION
FOR SOLID-STATE QUANTUM COMPUTATION

by

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Foreword

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Dedication

This dissertation is dedicated to my maternal grandfather, who brought me so much happiness in my childhood. I, always, miss you.

Acknowledgments

Coming to the final stage of Ph.D study and looking back these years of doing scientific research, I think now I have a little more understanding to the cartoon series created by Prof. Matthew Might – “The illustrated guide to a Ph.D” [1]. What is a Ph.D doing? – Standing at some edge of human knowledge by reading research papers, selecting a direction on the boundary, and trying to push a dent in the vast, unknown universe. During these years, every time when I felt lost of direction and asked myself what the meaning of my work is, I thought of this cartoon and began to gradually understand that, this is what research is and the work of a scientific researcher is digging in the unknown dark. So finally, I produced this dissertation to explain the “dent” that I pushed in the past years.

Here I would like to sincerely thank my research advisor at National Institute of Standards and Technology (NIST), Dr. Josh Pomeroy, who guided me through these years of conducting Ph.D research, creating fruitful scientific results and reaching this significant milestone. We had a lot of enlightening discussions when I got confusions, difficulties and distractions, and he continuously taught me how to be a qualified scientific researcher. I am quite proud of the work we have done together. This experience is destined to leave an important mark in my life. I would also like to express my deep gratitude to my academic advisor at the University of Maryland,

Prof. Edo Waks. The strong support and helpful advice from Prof. Waks extend from the class of quantum mechanics to the long period of my Ph.D study, assisting me to get through multiple stages to obtain a doctoral degree.

It is nearly impossible to thank everyone that gave me a hand in my successful completion of this dissertation. For these years of working at the Quantum Processes and Metrology group at NIST, I want to thank our present and previous group members, Zac Barcikowski, Dr. Aruna Ramanayaka, Dr. Ryan Stein, Dr. Ke Tang, Dr. Kevin Dwyer, Dr. Hyun Soo Kim, Dr. Binhui Hu, Dr. Roy Murray, Dr. Xiqiao Wang, Dr. Ranjit Kashid, and physicists, Dr. Michael Stewart, Jr. and Dr. Richard Silver. I want to specially thank Dr. Neil Zimmerman for training me and giving me the access to the dilution refrigerator. They all gave me a lot of helpful suggestions and brilliant insights. We collaborated and achieved lots of interesting research results. Very importantly, this work would have been impossible without funding from our group leader, Dr. Garnett Bryant. I also need to appreciate Dr. Pradeep Namboodiri for spending much time last year on taking AFM (atomic force microscope) images for my devices.

Most gratefully, I want to acknowledge my family for the endless support they gave me through my life. This dissertation should really be dedicated to them. Thank you to my mom and dad for cultivating me with infinite patience and love, and encouraging me to pursue a Ph.D study. My mom and dad's endeavor and enthusiasm in their major always impact and motivate me. Specifically, I owe thanks to my beloved husband, Dr. Bingbing Ji, for his continued and unfailing love, emotional support and encouragement in my down time, and help from his area

of expertise. Without their support, I could not get through this long and very challenging journey.

Finally, I want to thank my committee members: Prof. Christopher Davis, Prof. Thomas M. Antonsen, Jr., and Prof. John Cumings, for their careful review of this dissertation.

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Chapter 1: Introduction

With the increasing demand of computational power and shrinking size of microelectronic transistors, quantum computing has been attracting more and more attention in both research and industrial fields. On the one hand, quantum computing provides fundamentally different algorithms and remarkably enhanced calculation speed than classical computing for those difficult problems that have exponentially increasing complexity [3]. On the other hand, an end-point of “Moore’s law” [4] that successfully predicts continuous reduction in transistor dimensions, is approaching due to the domination of quantum effects [5]. Instead of making great efforts to suppress quantum effects, it is more wise to harness the quantum effects for the benefit of solving complex problems. So far, the achievements in implementing quantum logic gates, quantum algorithms, surface code, machine learning, etc. are exciting, and quantum computers for wide applications are expected to be commercially available within a few years [6, 7, 8, 9, 10, 11, 12, 13].

Shor’s algorithm for prime factorization [14] is the most famous example that demonstrates the supremacy of quantum computers over classical computers for specific problems. For modern classical computers, this computational problem of factorizing a large composite integer N into prime numbers requires billions of

years to solve, which is computationally unreachable, and therefore has being widely used for a basic encryption tool in information security, known as Rivest-Shamir-Adleman (RSA) cryptosystem [15]. However, due to Shor’s algorithm, a quantum computer can solve it within a few hours and is capable to invalidate the current RSA cryptography schemes.

For representing information, the counterpart of a bit in quantum computing is the quantum bit, known as qubit. There are two significant properties of qubits that make a quantum computer fundamentally different from a classical computer – quantum superposition and quantum entanglement [3]. Unlike in classical computing where a bit can only be in the 0 state or 1 state, the qubit in quantum computing can be in both ground and excited states at the same time with a probability for each, called superposition [16]. Superposition indicates the wave-like property and complies with the Schrodinger equation. If one qubit is in the superposition of two classical states, then n qubits are in a superposition of 2^n classical states. Therefore, by connecting many qubits via superposition, vast computational spaces are created. The quantum entanglement was discovered by Albert Einstein [17]. If two qubits are generated and “entangled”, there is a correlation between them – if one qubit is in one specific state, the other qubit has to be in another specific state. A representative example is the electron spin such that when two electrons are entangled, then one of the electrons is always measured to be spin-up if the other electron is measured to be spin-down. With quantum algorithms using quantum entanglement, particular complex problems can be solved more efficiently on quantum computers than classical computers. These two properties together give

quantum computers massive computational power. These special properties leads to the critical requirement of quantum computers – the internal operation must be isolated from the rest of the universe [18]. Loss of information from the system into the environment can disturb the fragile quantum mechanical waves and cause quantum decoherence. There are three important time scales that determine the qubit fidelity – T_1 , T_2 and T_2^* . T_1 is the relaxation time that an excited state takes to decay towards the ground state. T_2 is the coherence time or dephasing time, which characterizes the time that a qubit can keep its quantum coherence properties. T_2^* is the measured decay time which is close but smaller to T_2 due to experimental or environmental imperfections.

There are many physical realizations of qubits such as nuclear magnetic resonance (NMR) [19, 20, 21], ion traps [22, 23, 24], superconducting circuits [25, 26, 27], nitrogen vacancies (NV centers) in diamond [28], semiconductor quantum dots [29, 30, 31, 32], etc. Among these paths, solid-state implementations appear to be promising because of the potential scalability and possible integration with existing silicon device fabrication and nanoscale technology [3, 33, 34]. Here in this thesis, I will focus on the two solid-state quantum computing approaches – superconducting and semiconducting quantum computing. More specifically, nanoscale device development and characterization for both superconducting and semiconducting quantum computing fields will be presented and discussed. One type of device is metallic single-electron transistor (SET) with Al/AlO_x/Al tunnel junctions, which is also know as Josephson junction and a key component in superconducting quantum computation. The other type of device is silicon metal-oxide-semiconductor (MOS)

quantum dot for semiconducting quantum computation which utilizes spin qubit. In this chapter I will introduce the basic principles for understanding the operating mechanisms of these devices for quantum computing.

1.1 Electron Transport through Quantum Dots

This section closely follows the discussion in Ref. [35].

The basic operating mechanisms of the devices discussed in this thesis rely on the electron transport mechanism through quantum dots. Quantum dot can be considered as a small island confining electrons which is coupled to three terminals – source, drain and gate electrodes [35, 36], as shown in Fig. 1.1. They together constitute a single-electron transistor (SET). The small conductor acts as an island for confining individual electrons residing in it, and is also called as “island” in SET devices. The source and drain electron reservoirs are coupled to the dot through tunnel barriers. Electron tunneling can only occur between the dot and source/drain reservoirs, as indicated by the arrows. The source and drain electrodes connect the dot to macroscopic voltage sources and current meters. The gate electrode controls the electrostatic potential of the dot. The number of electrons on the dot can only be an integer, which leads to the quantized charge on the dot. Electrons on the dot occupy quantized energy levels. The thermal energy $k_B T$ (k_B is the Boltzmann constant and T is the thermal temperature) must be smaller than the energy level spacing on the dot, ΔE , to resolve the energy level quantization. The level spacing at the Fermi energy E_F for a box of size L is [35]: $(N/4)\hbar^2\pi^2/mL^2$ for

1D, $(1/\pi)\hbar^2\pi^2/mL^2$ for 2D and $(1/3\pi^2N)^{1/3}\hbar^2\pi^2/mL^2$ for 3D (N and m are integer numbers, $\hbar$ is the reduced Planck constant). $\hbar^2\pi^2/mL^2$ is the characteristic energy scale. When electron tunneling occurs, the system adjusts the number of electrons on the dot to minimize the total energy. To observe the phenomena originating from the charge discretization, two conditions are required: 1) charging energy of the quantum dot must exceed the thermal energy, $E_C \gg k_B T$ where E_C is the charging energy of the dot that will be discussed below; 2) the tunnel resistances between the dot and source/drain are sufficiently high to confine the electrons, $R_t \gg h/e^2$ where R_t is the tunnel resistance of a single tunnel barrier and h/e^2 is the resistance quantum (h is the Planck constant).

Fig. 1.2(a) shows the potential diagram of a quantum dot along the transport direction. The states in the source/drain reservoirs of electrons are filled up to the electrochemical potentials $\mu_{\text{source}}/\mu_{\text{drain}}$, respectively. The externally applied source-drain bias V_{sd} produces an energy window between the source and drain reservoirs: $eV_{sd} = \mu_{\text{source}} - \mu_{\text{drain}}$. Neglecting thermal energy and co-tunneling, transport only occurs when available charging levels on the dot fall within the energy window [35]. The number of available states is determined by the electrochemical potential of the dot, $\mu_{\text{dot}}(N)$, where N is the number of electrons on the dot. At a fixed gate voltage V_g , N is the largest integer that satisfies $\mu_{\text{dot}}(N) < \mu_{\text{source}} \cong \mu_{\text{drain}}$. The states in the dot are filled up to $\mu_{\text{dot}}(N)$ and separated by the single-particle energy spacing ΔE . For the electrochemical potential of the dot, the general form is: $\mu_{\text{dot}}(N) = \mu_{\text{ch}}(N) + e\varphi(N)$, where $\mu_{\text{ch}}(N)$ is the chemical potential and $e\varphi(N)$ is the electrostatic potential.

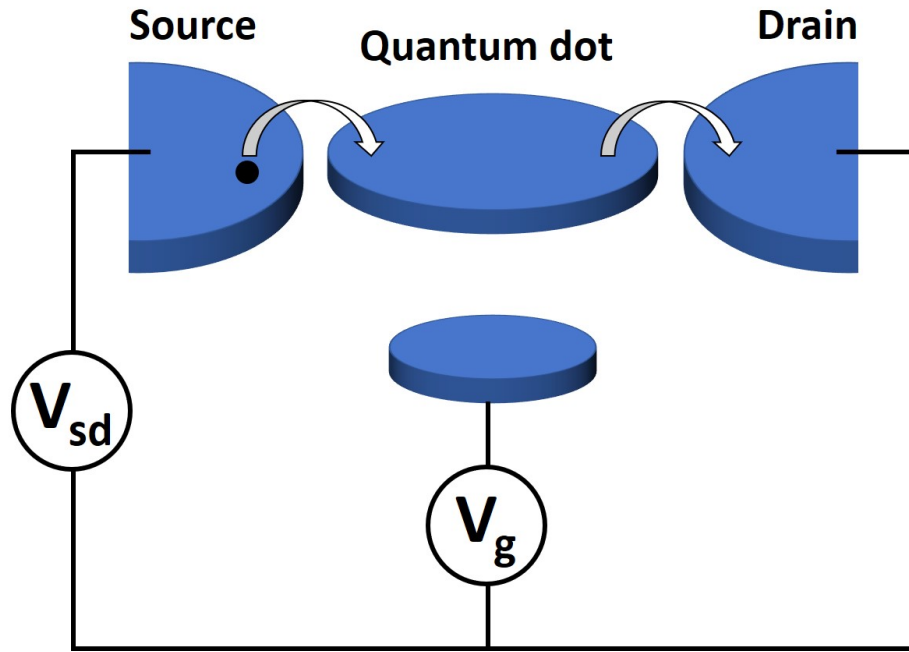


Figure 1.1: (Adapted with permission from Ref.[35], Copyright 1997, Springer Science Business Media Dordrecht) Schematic diagram of a quantum dot. The dot is coupled to source, drain and gate electrode. Electron tunneling can only occur between the dot and the source/drain reservoirs, as indicated by the arrows.

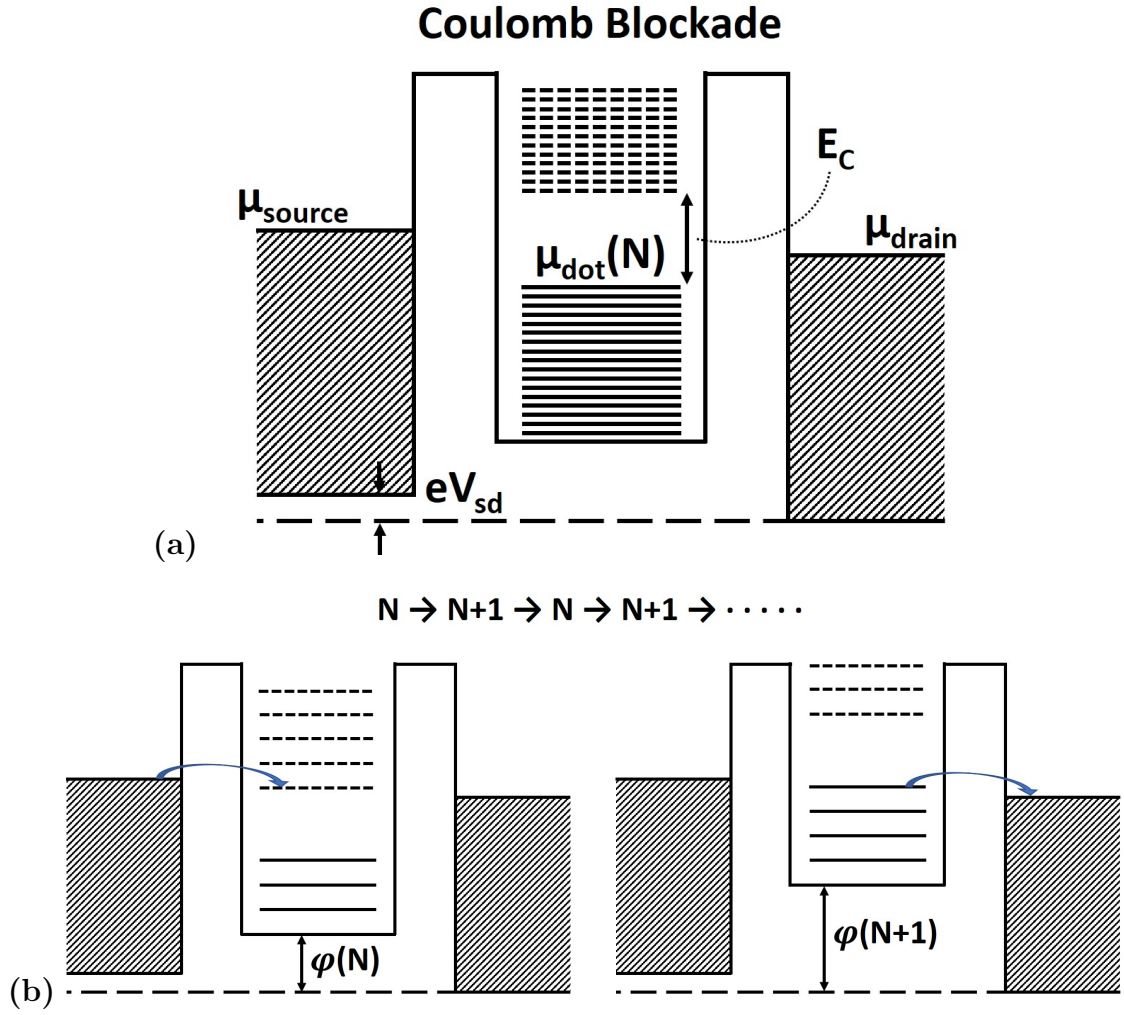


Figure 1.2: (Adapted with permission from Ref.[35], Copyright 1997, Springer Science Business Media Dordrecht) Potential diagram of a quantum dot along the transport direction. (a) Coulomb blockade regime. (b) Single electron tunneling regime.

To add one electron to the dot, the required addition energy is the electrochemical potential difference between the two charge states, N and $N + 1$, which is referred to as the charging energy: $E_C = \mu_{dot}(N + 1) - \mu_{dot}(N) = \frac{e^2}{C_\Sigma}$. Here C_Σ is the dot's total capacitance. This non-zero addition energy leads to a blockade for electrons tunneling on the dot, as illustrated in the low bias regime in Fig. 1.2(a), where there is no current between the two peaks. The addition of one electron on the dot would raise $\mu_{dot}(N)$ (the highest solid line) to $\mu_{dot}(N + 1)$ (the lowest dashed line), which is higher than the reservoir's electrochemical potential. Therefore, the electrons in the source reservoir cannot tunnel on the dot. This is the case of "Coulomb blockade" – the electron transport is blockaded when $\mu_{dot}(N) < \mu_{source}, \mu_{drain} < \mu_{dot}(N + 1)$. In the case of Coulomb blockade, electron exchange is prohibited and the number of electrons on the dot is fixed, so there is no current through the dot.

The gate electrode is coupled to the dot and controls the dot's electrostatic potential. By changing the gate voltage, $\mu_{dot}(N + 1)$ can be moved down to fall within the source-drain bias window, between μ_{source} and μ_{drain} , as illustrated in Fig. 1.2(b) left panel. Since $\mu_{source} > \mu_{dot}(N + 1)$, an electron from the source reservoir can tunnel onto the dot and raise the dot's electrostatic potential from $e\varphi(N)$ to $e\varphi(N + 1)$, $e\varphi(N + 1) - e\varphi(N) = E_C$, illustrated as an increase in the conduction band bottom in Fig. 1.2(b). Now the states in the dot are filled up to the dot's electrochemical potential $\mu_{dot}(N + 1)$, as illustrated in Fig. 1.2(b) right panel. Since $\mu_{dot}(N + 1) > \mu_{drain}$, one electron can tunnel off the dot to the drain reservoir, decreasing the dot's electrochemical potential back to $\mu_{dot}(N)$. A new cycle begins

by a new electron tunneling from the source reservoir on the dot and this single electron tunneling process repeats with the number of electrons on the dot jumping between N and $N + 1$: $N \rightarrow N + 1 \rightarrow N \rightarrow N + 1 \rightarrow \dots$. Therefore, current through the dot can be measured due to the successive discrete charging and discharging of the dot.

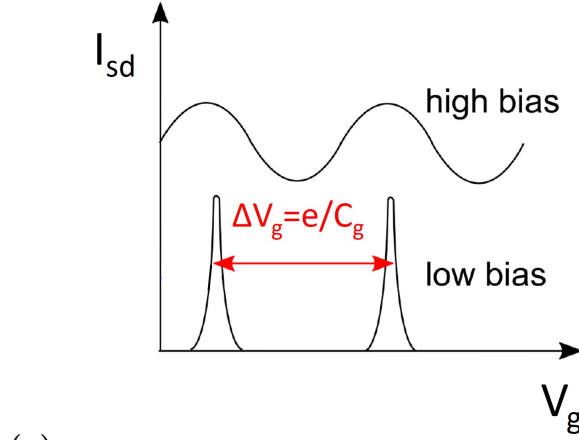
At a fixed source-drain bias, the current through the dot oscillates between zero (Coulomb blockade) and non-zero (no Coulomb blockade) by sweeping the gate voltage V_g , which is known as Coulomb blockade oscillations, as illustrated in Fig. 1.3(a). The oscillation period for single electron tunneling in the gate voltage direction is: $\Delta V_g = \frac{e}{C_g}$, where C_g is the coupling capacitance between the gate and the dot. In the blockade region between peaks, the number of electrons on the dot is fixed to an integer N . In the crossover between two stable charge states or the peak region on the right, the number of electrons on the dot jumps between N and $N + 1$ and results in a “charge degeneracy” [37], which induces the observed current peaks. And in the next blockade region, the number of electrons on the dot is increased to $N + 1$. When the source-drain bias increases and opens the bias window, more than one energy level falls within the bias window and transport is no longer blockaded. In this case, the current oscillates nearly sinusoidally without reaching zero, increasing as a level enters and decreasing as a level leaves the bias window, as shown in Fig. 1.3(a) [36]. If we fix the gate voltage V_g and sweep the source-drain bias V_{sd} , a non-linear current-voltage characteristic known as Coulomb staircase can be measured, as shown in Fig. 1.3(b). A new current step occurs at the threshold voltage (e/C_Σ) at which one more conduction channel is allowed on

the island. The threshold voltage is periodic in gate voltage, in accordance with the Coulomb oscillations. By sweeping both V_g and V_{sd} and measure the conductance, the so-called Coulomb diamonds can be measured as shown in Fig. 1.3(c). Transport is blocked inside the diamonds. The height of the diamonds indicate the charging energy.

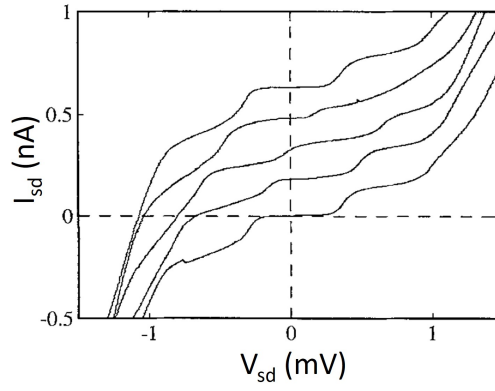
1.2 Metal-Oxide-Semiconductor (MOS) Structure

This section closely follows the discussion in Ref. [39].

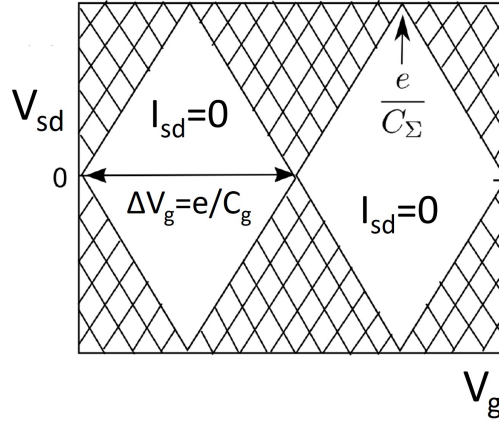
One direct way to realize an SET island (dot) is to confine electrons in a small piece of metal with insulating materials as tunnel barriers for controlling electron exchange between the dot and source/drain. Another way to realize smaller quantum dots is to form confined electron regions in semiconductors, which can be achieved by metal-oxide-semiconductor (MOS) structures. Shown in Fig. 1.4 is a cross-sectional view of the basic MOS device structure. The MOS device is fabricated from a silicon substrate which is moderately doped for p -type or n -type. Shown here is a p -type substrate. The substrate together with its ground is called the base. On the top of the base is an insulating layer of silicon dioxide grown on the surface of the silicon substrate, acting as the gate dielectric. The top gate layer is usually formed by deposition of some metal or highly conductive poly-Si. The gate electrode is used to apply an electric field through the oxide to the silicon. For the MOS device shown in Fig. 1.4, the source and drain regions are n -type to provide electron carriers. The source and drain electrodes are ohmic contacts which are connected to macroscopic



(a)



(b)



(c)

Figure 1.3: (a) Coulomb blockade oscillations as a function of the gate voltage V_g at low and high source-drain bias, V_{sd} . (b) Coulomb staircase measurement as a function of V_{sd} . (c) (Adapted from Ref.[36]) Schematic Coulomb diamonds as a function of V_g and V_{sd} . ((a) and (c) are adapted from Ref.[36], an Open Access article under Creative Commons Attribution License; (b) is adapted with permission from Ref.[38], Copyright 1991, Springer-Verlag.)

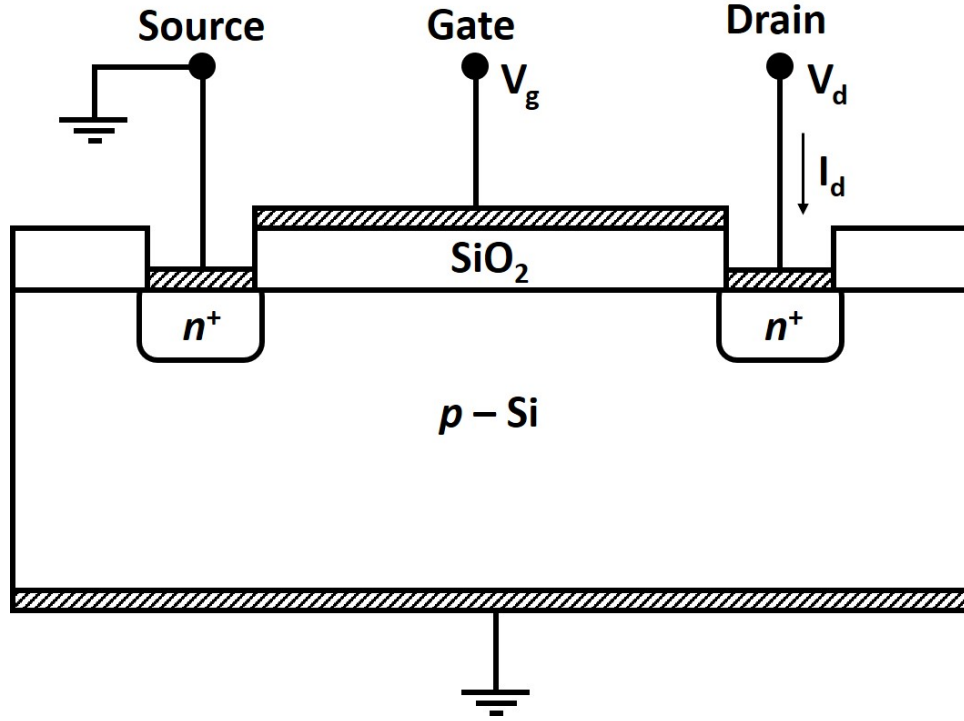


Figure 1.4: (Adapted with permission from Ref.[39], Copyright 2018, Springer-Verlag GmbH Germany) Schematic diagram of the cross-sectional view of the basic MOS device structure. Shown here is a p -type substrate and n -type source and drain regions.

voltage sources and current meters. The electric field applied by the gate electrode can induce changes of the carrier properties in the silicon layer underneath the gate, i.e., changes of conductance in the source-drain channel.

For the operating of the MOS device, there are four regimes related to four different gate voltage ranges, V_g [39, 40]. Shown in Fig. 1.5 top half are the schematic energy band diagrams of the MOS structure in these four regimes. For each V_g range, the diagram shows three regions and they represent metal, oxide and semiconductor from the left to the right. In the metal regions, the Fermi levels for the metal $E_{F,m}$ are denoted by the solid lines and the dashed lines denote the positions of the

Si Fermi levels E_F . In the oxide regions, we show the valence band edge. In the semiconductor regions, we show the Si conduction band edge E_c , the intrinsic Fermi level for the undoped Si E_{Fi} (illustrated as dashed lines), the Fermi level E_F for the p -type Si, and the valence band edge E_v in each diagram. Fig. 1.5 bottom half show the charge layers of the interfaces in each regime and the names of these regimes.

When $V_g = 0$, the Fermi levels in the metal and semiconductor regions line up and there are no net charges at the interfaces. This is the flat-band regime where the energy bands in the semiconductor are flat.

When $V_g < 0$, an electric field is built up in the oxide and the negative gate voltage bends the Si energy bands up at the semiconductor-oxide interface. The Fermi level E_F is constant through the semiconductor region because the system is in thermal equilibrium and there is no current. The valence band edge E_v is now closer to the Fermi level E_F at the semiconductor-oxide interface than in the bulk semiconductor. Therefore, holes accumulate at the semiconductor-oxide interface and electrons accumulate at the metal-oxide interface. This is the accumulation regime where the surface of the semiconductor is more p -type than the bulk material.

When the gate voltage is positive but less than some threshold value V_{th} which is determined by the electrical and geometry properties of the MOS structure, $0 < V_g < V_{th}$, the electric field applied by the gate voltage bend the Si energy bands down at the semiconductor-oxide interface, resulting in a space charge region and a depletion of holes. This is the depletion regime where a negatively charged layer of localized states is formed at the semiconductor-oxide interface and corresponding positively charged region is formed at the metal-oxide interface. The induced

depletion region width increases as V_g increases. V_{th} is the gate voltage that causes the intrinsic Fermi level E_{Fi} and the actual Fermi level E_F to be identical at the semiconductor-oxide interface.

When $V_g > V_{th}$, the Si energy bands at the semiconductor-oxide interface are further bent down and the intrinsic Fermi level at the interface E_{Fi} drops below the actual Fermi level E_F . The conduction band edge E_c at the surface is now closer to the Fermi level E_F than the valence band edge E_v , while E_v is closer to E_F than E_c in the bulk Si. This is the inversion regime, where the surface of the semiconductor at the semiconductor-oxide interface is now inverted from p -type to n -type, inducing the inversion layer, where mobile electrons reside. The inversion layer creates a conducting channel between the source and drain regions. The electrons in this inversion layer are of wide interest, since their motion in one dimension is confined and quantized, forming two-dimensional electron gas (2DEG) [39]. Most importantly, they can be controlled by the gate electrode.

1.3 Electron Spin Readout in Solid-State Quantum Computing

This section closely follows the discussion in Ref. [30].

Over the past several decades, tremendous advances have been achieved in the field of quantum information. Among these building blocks towards sophisticated quantum computing processors, solid-state quantum computing has many attractive features such as being considered more versatile and more easily scalable, and the anticipated integration with existing silicon device fabrication and nanoscale

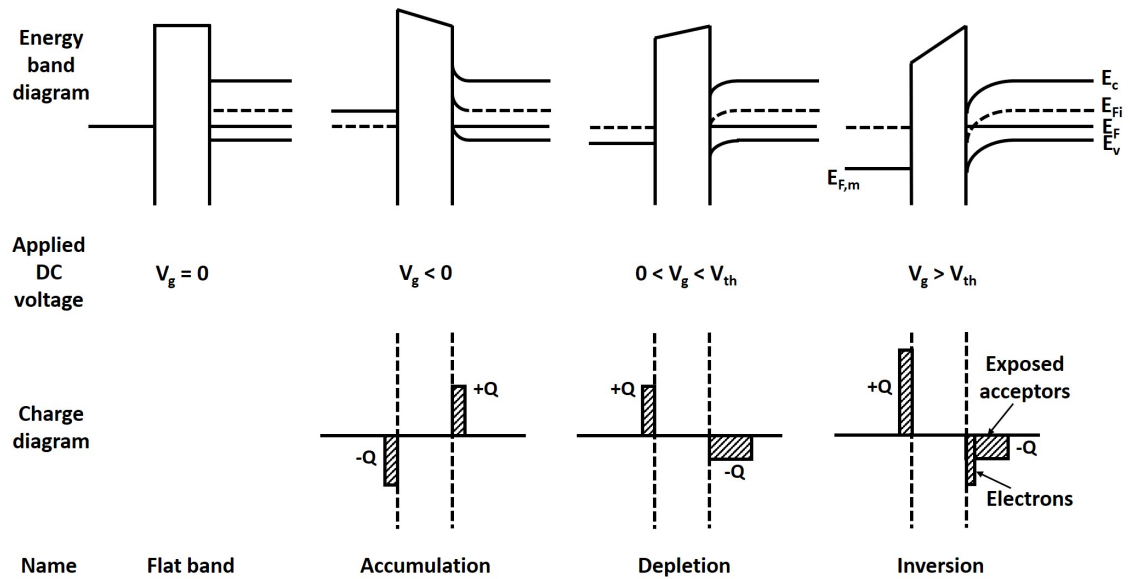


Figure 1.5: (Adapted with permission from Ref.[39], Copyright 2018, Springer-Verlag GmbH Germany) Schematic energy band diagrams and the charge configurations of MOS device in four regimes – flat band regime, accumulation regime, depletion regime and inversion regime.

technology [33, 41]. Electron spins confined in solids are considered as carriers for quantum information and can represent well-isolated qubits due to long coherence times [32, 42], fast gate operations [43, 44], and the potential for scalability [45, 46].

To perform computation, the electron spin qubits must be initialized and measured [47, 48, 49]. In both circuit-based and measurement-based quantum computing, the readout of an individual electron spins is a critical step, which have been achieved with spin-to-charge conversion followed by charge detection. More specifically in this technique, whether an electron can tunnel depends on its spin state, and a charge detector electrostatically coupled to the electron site can sense whether the charge is displaced, thereby indicate the spin state [32, 42, 50, 51]. SET devices are extraordinarily sensitive to charge change in the vicinity of the SET island and can consequently be used as charge detectors [52].

Fig. 1.6(a) and (b) illustrate an example operation of electron spin readout [30]. The spin-dependent tunneling of electrons is achieved by applying a magnetic field B so that the spin-up state has a higher energy than the spin-down state, differentiated by the Zeeman splitting $E = g\mu_B B$, where $g \approx 2$ is the spin gyromagnetic ratio and μ_B is the Bohr magneton. To perform the readout, the electrochemical potentials on the SET island (μ_{SET}) and a nearby electron site ($\mu_{\uparrow}$ for spin-up state and $\mu_{\downarrow}$ for spin-down state) are set by the gate voltages such that the SET current I_{SET} is zero when the electron is on the electron site, and I_{SET} is nonzero when the electron is on the SET island. There are three phases in the readout process. (1) Load phase, when the gate voltage is tuned such that $\mu_{\text{SET}} > \mu_{\uparrow}, \mu_{\downarrow}$, an electron in an unknown spin state tunnels from the SET island to the electron site, and I_{SET} drops

to zero. (2) Read phase, when the gate voltage is tuned such that $\mu_{\downarrow} < \mu_{\text{SET}} < \mu_{\uparrow}$, a spin-down electron remains trapped on the electron site, resulting in $I_{\text{SET}} = 0$, while a spin-up electron can tunnel onto the SET island and lead to $I_{\text{SET}} > 0$. A different spin-down electron from the SET island can later tunnel back onto the electron site, causing $I_{\text{SET}} = 0$ again. Therefore, the signal of a spin-up electron is a current pulse at the beginning of the read phase, while no SET current change is observed during the whole read phase if the original electron is in spin-down state. (3) Empty phase, when the gate voltage is tuned such that $\mu_{\text{SET}} < \mu_{\uparrow}, \mu_{\downarrow}$, to empty the electron site to prepare for a new cycle. The remaining spin-down electron on the electron site tunnels back onto the SET island, leading to $I_{\text{SET}} > 0$.

1.4 Motivation and Project Goals

SET devices, which can be realized either in metals or in semiconductors, play an important role in single spin readout for solid-state quantum computing. For metallic SET devices, the tunnel barriers are realized by sandwiching a very thin insulator between the SET island metal and source/drain metal [53, 54]. This structure is known as tunnel junctions. The widely used tunnel junctions in metallic SETs are Al/AlO_x/Al tunnel junctions, because aluminum as metal leads has good conductance, and its native oxide has good dielectric properties and is relatively easy to fabricate. Al/AlO_x/Al tunnel junctions are also popular in superconducting quantum computing communities as Josephson junctions [55, 56, 57]. For semiconductor SET devices, the dot is formed by inducing an electron layer (2DEG) using

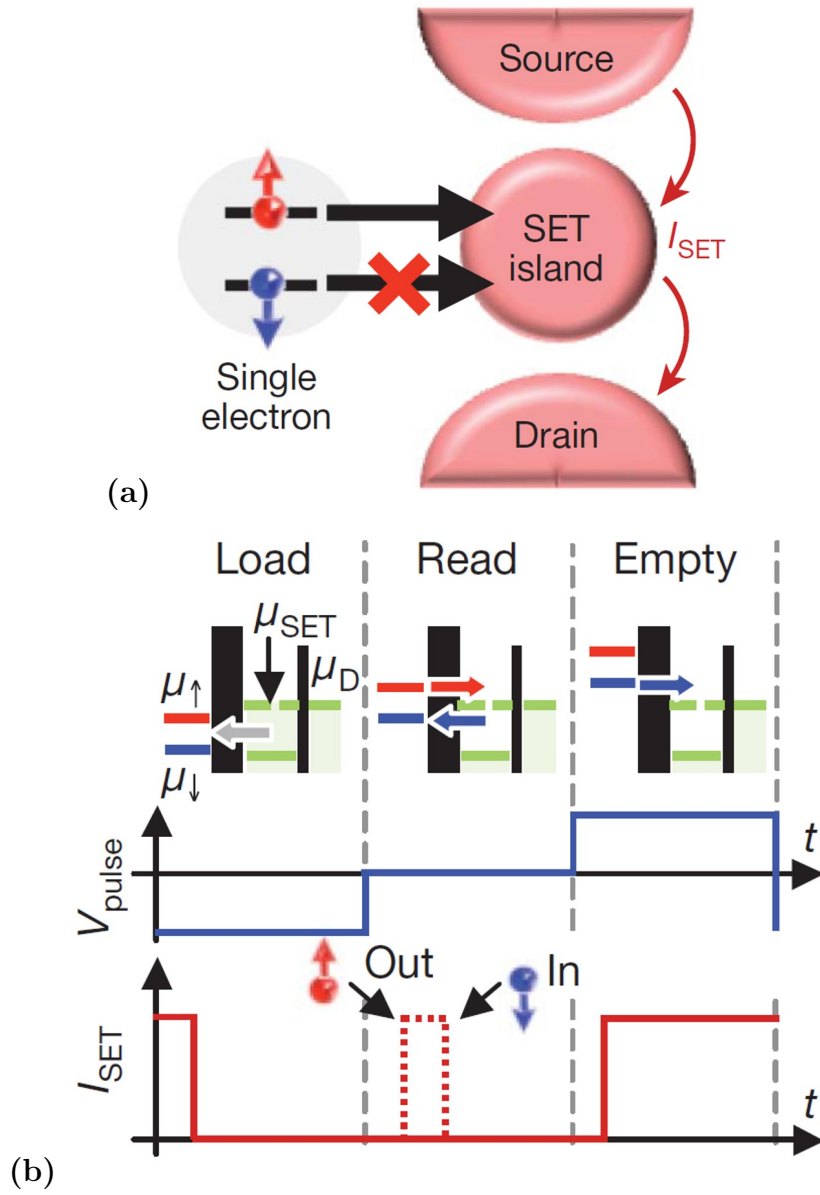


Figure 1.6: (Adapted with permission from Ref.[30], Copyright 2010, Nature Publishing Group) An example operation of electron spin readout. (a) A schematic diagram showing spin-dependent tunneling. (b) Illustration of the electrochemical potentials, gate pulse sequence and SET current showing the readout process.

the electric field applied by the inversion gate and inducing tunnel barriers using the electric field applied by the barrier gates in the MOS structure. Al together with AlO_x are also widely used as the gate material and gate isolation.

Metallic SET devices are relatively easy to fabricate and low-cost, since the device fabrication mainly involves two metal layer deposition and oxide growth in between them, and minimum requirements for the substrate (substrate with surface dielectric). By using double-layer stencil masks and double-angle deposition, the deposition of two metal layers only require one e-beam lithography process [54]. Since the dot is already defined by the island metal and tunnel junctions when the device is fabricated, metallic devices don't require much efforts to tune the single electron tunneling conditions. However, the tunnel barriers are fixed and cannot be tuned in metallic devices. Shrinking the dot size is also limited.

Fabricating semiconductor SET devices is more complicated because of the MOS mechanisms. It requires high-quality silicon substrate, the substrate needs to be implanted for the source/drain regions, silicon dioxide needs to be grown as the primary gate isolation, the ohmic contacts cannot be fabricated together with the gate structures, and devices with multiple gate layers can have more failure modes, etc. Compared to metallic devices, semiconductor devices require much more efforts to tune the quantum dots and tunnel barriers. On the other hand, the quantum dots formed in semiconductors are tunable and can be made very small, thereby are more likely to achieve few electron regime to have better qubit performance [30, 31, 58].

It is noted that aluminum and its oxide are ubiquitously employed in solid-state quantum computing field. However, amorphous AlO_x with initial nonequilibrium

structure is frequently reported to have a broad distribution of electrically active defects, exhibiting instabilities and therefore inducing decoherence sources in qubit devices [55, 59]. One manifestation of AlO_x instabilities is charge offset drift in SET devices, which is observed as random fluctuations of the phase of the device’s control curve [36] and can be utilized as a metric to evaluate the material instabilities in SET devices.

Therefore, the goal of this work is to first mitigate AlO_x instabilities in quantum computing devices by using charge offset drift as the metric, seek for a robust approach to improve fabrication efficiency and reduce failure modes of MOS quantum dot devices with reduced but still sufficient capabilities to fulfill our qubit development, and finally design a feasible way to integrate metallic and semiconductor devices together to develop a preliminary qubit platform for diagnostics. During this process, studying the noise sources are necessary to evaluate and improve our measurement capabilities for advancing qubit implementation.

1.5 Dissertation Outline

- **Chapter 2:** The experimental apparatus and methods used to fabricate and characterize solid-state quantum computing devices in this work are demonstrated. This is mainly focused on our customized instruments, process and measurement methods in addition to the standard cleanroom fabrication techniques.
- **Chapter 3:** Reduction of charge offset drift in metallic SETs using plasma

oxidized aluminum is presented and discussed. The charge offset drift (ΔQ_0) measured from the plasma oxidized AlO_x SETs in this work is remarkably reduced (best $\Delta Q_0 = 0.13 \text{ e} \pm 0.01 \text{ e}$ over ≈ 7.6 days and no observation of ΔQ_0 exceeding 1 e), compared to the results of conventionally fabricated AlO_x tunnel barriers in previous studies (best $\Delta Q_0 = 0.43 \text{ e} \pm 0.007 \text{ e}$ over ≈ 9 days and most $\Delta Q_0 \geq 1 \text{ e}$ within one day). This improvement is primarily attributed to using plasma oxidation, which forms the tunnel barrier with fewer two-level system (TLS) defects, and secondarily to fabricating the devices entirely within a UHV system.

- **Chapter 4:** Development of robust, single metal gate layer MOS quantum dot devices with reduced failure modes and compromised electrostatic gate control is presented and discussed. Quantum dot formation, capacitive charge sensing between channels, and reasonable effective electron temperatures that enable spin qubit studies are presented. The costs and benefits of the trade-off between device performance and fabrication efficiency are discussed.
- **Chapter 5:** Noise study based on Coulomb blockade peak width broadening and improvement of device measurement capabilities are presented and discussed. Temperature-dependent conductance measurements and comparison of effective electron temperature (T_e) using two different quantum dot systems, P donor-based and MOS-based Si quantum dots, are presented. The noise origins and factors inducing high T_e are discussed and analyzed. The noise level in a dilution refrigerator with $\approx 10 \text{ mK}$ base temperature is sub-

stantially lowered from ≈ 4 K to ≈ 0.5 K by rearranging ground configuration and noise filtering.

- **Chapter 6:** The design and development of integrating stability improved metallic AlO_x SETs and streamlined single metal gate layer MOS quantum dot devices for a hybrid qubit architecture are presented and discussed. The design of device structure and streamlined process flow will be presented, as well as the device modeling and simulation. An analytical method is proposed to evaluate the device design for charge sensing and spin readout feasibility.
- **Chapter 7:** A summary of the main scientific results and impacts of these results are presented. Future scientific research proposals enabled by this work are discussed.

Chapter 2: Experimental Apparatus and Methods

The device fabrication in this work are partly done with standard cleanroom fabrication facilities, and partly done with our customized experimental system and methods. The device characterization is mostly done in a 10 mK dilution refrigerator (DR) system, and partly done in a 4 K cryogenic system. In this chapter, I will introduce our experimental apparatus and methods used for fabricating plasma oxidized aluminum oxide (AlO_x) tunnel barriers in ultra-high vacuum (UHV) environment, and low-temperature systems for device characterization.

2.1 UHV Chamber Configuration

The plasma oxidized AlO_x tunnel barriers and UHV environment which contribute to the remarkable charge stability improvement of metallic SETs are achieved within a custom multi-chamber UHV system with base pressure $< 10^{-7}$ Pa (10^{-9} Torr). This custom multi-chamber UHV system is an integrated single system equipped with capabilities of deposition, plasma oxidation and X-ray photoelectron spectroscopy (XPS), as well as introducing and transferring samples between different chambers. Therefore, during the the whole course of fine structure fabrication of SET devices, we are able to keep the devices in UHV environment except for

the short time when the sample is exposed in oxygen plasma. Fig. 2.1 shows an overview of our custom multi-chamber UHV system, which consists of a load lock chamber for introducing samples and storing waiting samples, a deposition chamber for electron-beam (e-beam) evaporation, a plasma chamber for plasma oxidation, and an *in situ* XPS system for characterizing materials (not used in this work). The deposition chamber, plasma chamber and XPS chamber are all connected via the load lock chamber. Each chamber has its own vacuum pumping line and different chambers are isolated by highly reliable vacuum gate valves to keep their own vacuum pressure without being affected by other chambers. There are three magnetically coupled transfer rods installed in the deposition chamber, plasma chamber and XPS chamber, respectively. They are used to transfer samples between the load lock chamber and the other three process chambers, while opening the gate valve between the two sample transfer chambers.

To maximize the device volume fabricated in a single run, this system is designed for wafer scale (3 in wafer) processing. Samples are first introduced in the load lock chamber without interrupting the vacuum of other chambers. There is an elevator with 25 slots in the load lock chamber which can store 25 wafers at a time and move up and down for the transfer rods to select which wafer to be transferred to other chambers. Once the samples are loaded in, the load lock chamber can be pumped down to a typical pressure of 10^{-9} Torr, via a turbo pump backed by a scroll pump. The door of the load lock is sealed via a copper o-ring to ensure good vacuum. The load lock chamber is also served as the transfer station when transferring samples among the other three chambers. The sample is mounted in a

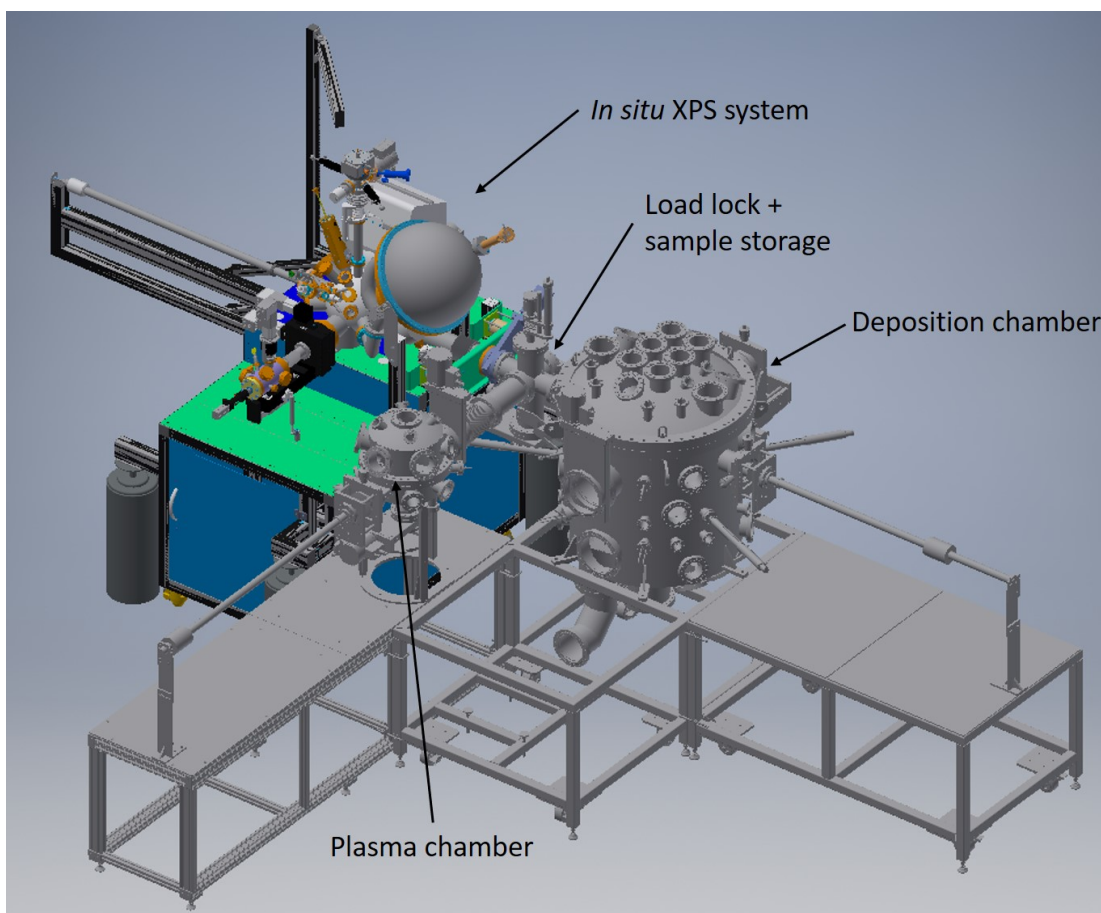


Figure 2.1: An overview of our custom multi-chamber UHV system, which consists of a load lock chamber for introducing samples and storing waiting samples, a deposition chamber for e-beam evaporation, a plasma chamber for plasma oxidation, and an *in situ* XPS system for characterizing materials.

a stainless-steel cassette and securely grounded by system ground throughout the whole processing in this UHV system.

Once the load lock chamber is pumped down to approximately 10^{-9} Torr, the gate valve between the load lock chamber and the plasma chamber can be opened and the SET device sample that has e-beam lithography patterned resist is transferred to the plasma chamber first for resist descum. The plasma chamber is kept under UHV (10^{-9} Torr) all the time except for the oxygen plasma processing period. During the oxygen plasma process, the plasma chamber is filled with research grade oxygen. Then the electrodes in the plasma chamber are energized to strike oxygen plasma. Details of the oxygen plasma process will be discussed in Section [2.2](#). Once the oxygen plasma process is done, the plasma chamber is immediately pumped down via its vacuum line all the way to its base pressure. When the plasma chamber is under UHV, the sample can be transferred to the deposition chamber via the load lock chamber for subsequent processing steps.

The deposition chamber is typically kept at a base pressure of $\approx 10^{-10}$ Torr and equipped with an e-beam evaporator. There are 5 pockets on the e-beam evaporator storing evaporant materials, providing selections of source materials among gold (Au), copper (Cu), aluminum (Al), cobalt (Co) and niobium (Nb) metals. There are crucible liners containing these metals to decrease heat transfer between the evaporant and the hearth, and provide better uniformity and deposition rate control. The source materials are placed linearly on a motor-controlled rail and the selected source material can be moved to the e-beam spot position for thin film deposition. During the e-beam evaporation, the e-gun hearth is cooled by continuous

chilled water flow. The deposition chamber is also equipped with a liquid nitrogen (LN_2) cooling shroud above the evaporating sources, and thermocouples for monitoring the metal shroud temperature. There are feedthroughs connecting the cooling shroud with LN_2 dewar to fill the shroud with LN_2 during e-beam evaporation. The LN_2 cooling shroud plays two role during the metal deposition: 1) regulate the temperature of the deposition chamber that is continuously heated by the source materials, 2) adsorb and freeze residual gases in the deposition chamber to provide better vacuum pressure and reduce impurities of deposited films. Typically with the metal shroud filled with LN_2 and at temperature $\approx -160^\circ\text{C}$, the deposition chamber pressure can be maintained below 5×10^{-11} Torr during the whole course of e-beam evaporation.

A motor controlled manipulator with capabilities of axial and radial rotation can hold and move the sample above the evaporation source for metal deposition. The distance between the source and the sample is ≈ 46 cm. For normal deposition, the sample is held face down with its normal aligned with the incidence of the evaporation vapor. For angle deposition, the sample is rotated axially to form a deposition angle between the sample normal and the incidence of the evaporation vapor. A commercial quartz crystal microbalance (QCM) deposition monitor is mounted in the deposition chamber to monitor deposition rate and measure deposited film thickness. There are three parameters set on the QCM controller for using different source materials: density, z-ratio, and tooling factor. Density and z-ratio are set according to the materials properties. Tooling factor is a geometric correction and is calibrated regularly by comparing the profilometry measured film

thickness representing the actual film thickness, with the QCM measured film thickness. The calibrated tooling factor (TF_m) can be calculated as: $TF_m = TF_i \cdot (t_m/t_i)$, where TF_i is the initial tooling factor, t_i is the film thickness measured by QCM, and t_m is the actual film thickness measured by profilometry. The QCM controller also controls the pneumatic shutter which can open and close the path between the evaporating source and the sample. Typically the source material is first evaporated at the desired evaporation rate with shutter closed for sacrificing a few nanometer thick film to clean the source material. After the source is cleaned to a satisfactory extent, the deposition can be started manually by opening the shutter through the QCM controller and making film thickness monitor start from zero. The desired film thickness is set on the QCM controller. When the film thickness monitored by the QCM reaches the set point, the QCM controller automatically closes the shutter and ends the metal deposition.

2.2 Plasma Oxidation

The advantage of plasma oxidized AlO_x tunnel barriers over conventional thermally oxidized AlO_x tunnel barriers was originally studied in the field of magnetic tunnel junctions (MTJ) for magnetic random access memory (MRAM) and other magnetic sensor applications, where the much higher magnetoresistance (MR) values were obtained through plasma oxidized barriers rather than thermally oxidized barriers [60, 61]. Plasma oxidation is found to incorporate much higher oxygen content (the oxygen incorporation rate scales logarithmically with time) in much shorter

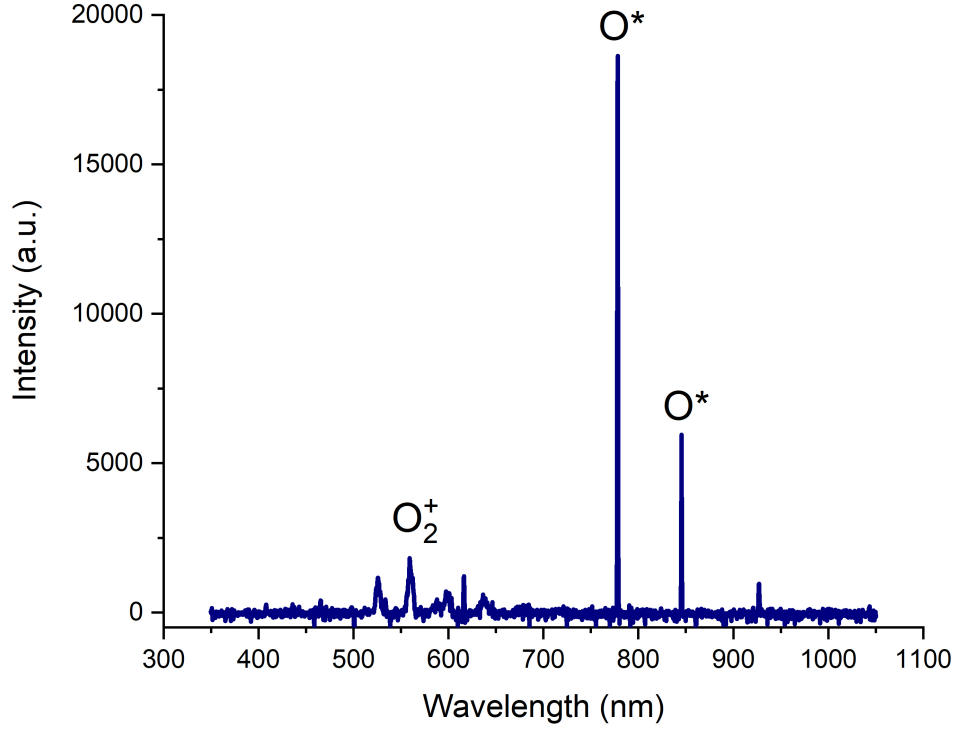


Figure 2.2: A typical optical emission spectrum of oxygen plasma taken in our plasma chamber (160 mTorr, 59 W, DC) [65]. The important species are charged O_2^+ molecules at 550 - 560 nm and neutral O^* free radicals at 777 nm.

time and form aluminum oxide that is much closer to stoichiometric Al_2O_3 than thermal oxidation [62, 63]. In the process of aluminum oxidation for both plasma and thermal processing, it is experimentally found that aluminum are the moving species by using oxygen isotopes, i.e., aluminum diffuses through the forming oxide and reacts with oxygen at the surface [62, 64]. During this phase, the growing oxide thickness increases with increasing processing time.

Kuiper et al. studied the mechanism of plasma oxidation [62, 63]. The oxygen plasma itself is charge neutral but consists of positive, negative and neutral species.

The negative species are mostly electrons but also include negatively charged oxygen ions and molecules. The positive species are mostly the singularly charged O_2^+ molecules. There also exists a large amount of electrically neutral, highly reactive O^* free radicals in the oxygen plasma. Shown in Fig. 2.2 is a typical optical emission spectrum of oxygen plasma taken in our plasma chamber (160 mTorr, 59 W, DC) [65]. In the spectrum, the important species are charged O_2^+ molecules at 550 - 560 nm and neutral O^* free radicals at 777 nm. Due to the experimental results that no effect measured when applying a voltage to the sample during plasma oxidation, Kuiper et al. deduced that neutral and low-energetic O^* radicals are the most significant species in the plasma oxidation [62, 63]. This also agrees with the observation that highest oxidation is obtained at the lowest pressure. At higher pressure, O^* free radicals have a shorter mean free path, and will collide with background gas particles and get thermalized before reaching the sample surface. At lower pressure, the mean free path of O^* free radicals are longer, and it is more likely that the O^* free radicals collide with the sample before colliding with other gas particles.

In our fabrication process, after the deposition of bottom layer aluminum, the sample is transferred *in situ* to the plasma chamber and plasma oxidized under condition of 21 Pa (160 mTorr) of research grade oxygen using 57 W to 60 W (100 mA at -570 V to -600 V) DC for 7 s. Fig. 2.3 shows the interior of our plasma chamber with ignited oxygen plasma. Inside the plasma chamber are two concentrically mounted circular electrodes in a parallel plate configuration, spaced by ≈ 3.8 cm distance, which is at the same order of the mean free path of O^*



Figure 2.3: The interior of our plasma chamber with ignited oxygen plasma. The bottom plate is the anode with the 3 in Si/SiO₂ wafer sample positioned in the center. The top plate is the cathode, connected to a high voltage power supply outside the vacuum chamber, through the Kapton coated wire.

free radicals at the experimental pressure. The bottom electrode is the anode. The sample (3 in Si/SiO₂ wafer) is facing up, held by a motor-controlled elevator, positioned in the center and in electrical contact with the anode plate. The top electrode is the cathode. Both anode and cathode plates are made with stainless steel. There is a Kapton coated wire that connects the top electrode (cathode) to a high voltage power supply sitting outside the vacuum chamber, through the top flange of the plasma chamber.

The pumping system of the plasma chamber is designed for efficiently filling the chamber with O₂ gas for plasma oxidation and fast pumping down the chamber back to its base pressure after the oxidation process. In a typical operation of plasma oxidation, the gate valve isolating the turbo pump and the chamber is closed so that the chamber is not pumped out by any vacuum pumps and the turbo pump is still kept at its full spin speed for fast evacuating the chamber after the plasma process. There is a stainless steel tube of gas line controlled by a manual leak valve connecting the plasma chamber and an 99.99 % pure O₂ source bottle. The research grade O₂ gas can now be leaked into the plasma chamber by opening the leak valve. There is also a backing valve connecting the plasma chamber and the backing scroll pump. The O₂ pressure in the plasma chamber is monitored and can be tuned to the desired pressure through combined control of the leak valve and the backing valve.

Once the plasma chamber is filled with pure O₂ gas, the high voltage power supply outputs a timed, negative DC bias in constant current mode to the top electrode (cathode) in the plasma chamber, to strike a plasma discharge in the background of O₂ gas [66]. The power supply is operated in fast mode and the rise

time to reach the current set points is < 1 ms. There is an optical spectrometer installed in the plasma chamber to monitor plasma composition during the oxidation process (see Fig. 2.2), making sure that the ignited plasma spectrum mainly consists of O_2^+ and O^* peaks without the presence of other impurities, as described in the literature [62, 63]. The processing parameters (O_2 pressure, power and time) of plasma oxidation were varied to optimize O^* intensity by previous group members in a smaller system using similar processing [67, 68]. For this system, these parameters were tuned by matching the resistance-area (RA) product of fabricated Co/ AlO_x /Co tunnel junctions with previous optimized results [65]. The typical RA product of Co/ AlO_x /Co tunnel junctions is $\approx 10^5 \Omega\mu m^2$ for 1.1 nm Al (expected to be fully oxidized and turn into ≈ 1.3 nm AlO_x after plasma oxidation) sandwiched between two Co layers. It is noted that in this bias direction, positive radicals (O_2^+) are accelerated toward the top cathode plate, away from the sample, which is in agreement with the literature [62, 63] that the neutrally charged O^* free radicals are the dominant species contributing to the the oxidation process.

After the plasma oxidation, the backing valve connecting the plasma chamber and the backing scroll pump is opened first to roughly reduce the chamber pressure to approximately 50 mTorr. Then we close the backing valve, and open the gate valve between the plasma chamber and the turbo pump which is kept at its full spin speed, to bring the chamber back to its base pressure (10^{-9} Torr). After oxidation, the sample is held under UHV for overnight to allow the formed oxide to relax, as detailed in Section 3.2.

2.3 Low-Temperature Systems for Device Characterization

2.3.1 10 mK Dilution Refrigerator

Dilution refrigerator (DR) systems are refrigerator systems that provide continuous cooling at temperatures below 300 mK. With the cooling power generated by mixing the two isotopes of helium, 3-He and 4-He, a DR can provide temperatures < 10 mK with no moving parts at the low temperature stages. The DR's continuous cooling cycle can only be started with $T \leq 4.2$ K. Previously, this precondition temperature was achieved by liquid helium bath in the wet DR. The DR system we are using in this work (Bluefors BF-LD400) is a modern DR (also known as dry DR), which can precool to reach the precondition with a Cryomech Pulse Tube (PT) cryocooler.

The DR cooling power is provided by 3-He/4-He mixtures at low temperatures. As shown in Fig. 2.4, at saturated vapor pressure pure 4-He undergoes a phase transition from a normal fluid into a superfluid at 2.17 K, resulting in completely different properties of the two isotopes below this transition temperature [69]. Diluting the 4-He with 3-He results in a decreasing superfluid transition temperature, as shown in Fig. 2.4. At temperatures below 0.8 K the 3-He/4-He mixture will separate into two phases: a 3-He rich phase (the concentrated phase) and a 3-He poor phase (the dilute phase). At very low temperatures the concentrated phase becomes pure 3-He while the dilute phase contains approximately 6.4 % 3-He and 93.6 % 4-He. The enthalpy of 3-He in the dilute phase is larger than that in the

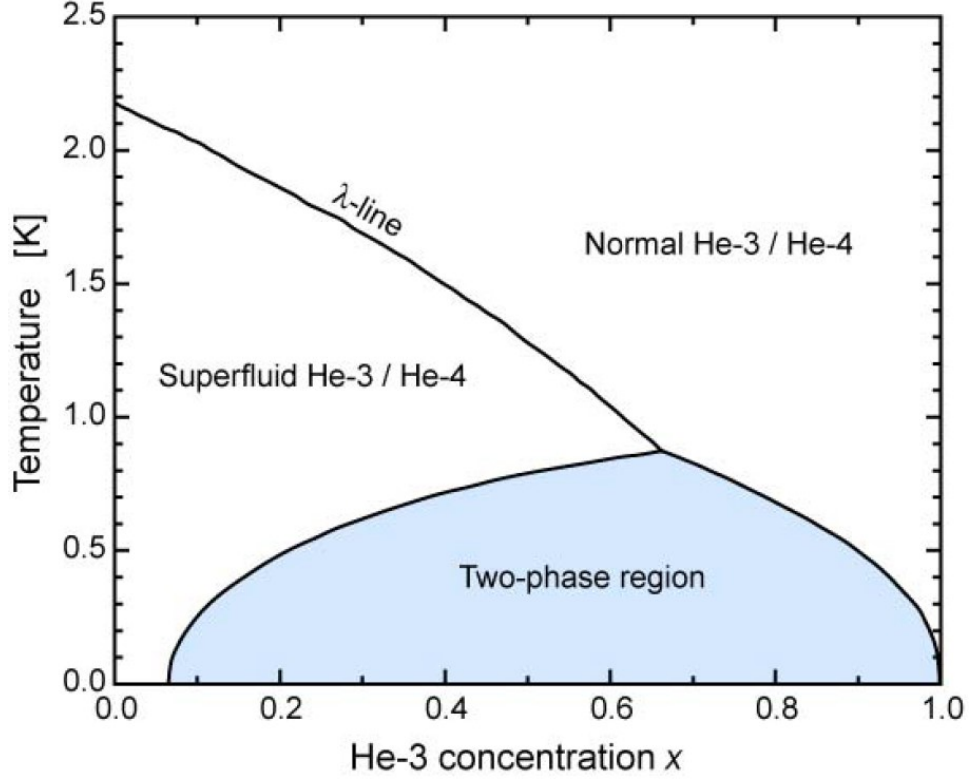


Figure 2.4: (Taken from Ref.[69]) Phase diagram of He-3/He-4.

concentrated phase, leading to energy consumption in moving 3-He atoms from the concentrated phase to the dilute phase. Therefore, heat can be removed from the well isolated mixing chamber environment in the DR and cooling is accomplished.

Shown in Fig. 2.5 left panel is the interior of our DR cryostat. There are different temperature stages for reaching the base temperature in the mixing chamber, where our samples discussed in this work are installed. The radiation shields of different temperature stages and the outer vacuum cans are not shown. As mentioned before, in our dry DR system we use a PT cryocooler to obtain the starting temperature $T \leq 4.2$ K to enter the DR cycle. The flanges of the 50 K and

quasi-4 K radiation shield are connected to the two stages of the PT. Flexible copper braids are used to protect the cryostat from vibrations caused by the PT. The whole radiation shield assembly is kept in one common vacuum space to be isolated from the surrounding environment. The 3-He gas is precooled to $T < 4.2$ K by different heat exchangers. There is a cold trap at approximately 50 K, which traps contamination in the circulation and also acts as a heat exchanger. The 3-He gas is then thermalized at the regenerator tube and the second stage of the PT.

After being pre-cooled to $T < 4.2$ K, the 3-He/4-He mixture is pressurized to approximately 2 bar by a compressor and then precooled by the heat exchangers in the condensing line to lower temperature to be partly condensed after the main flow impedance. The condensing line enters the still pumping line at approximately the quasi 4 K flange. The flow impedance is located inside the top part of the still. The mixture is condensed to liquid phase to fill the mixing chamber, heat exchangers and part of the still. The DR cycle is started by pumping the still. In the cycle, the helium pumped away can return into the system through the condensing line. The pumping causes helium evaporation, which is a heat absorbing process and decreases the mixture temperature to $T < 0.8$ K. At this temperature the phase separation of the mixture appears. The heavier 4-He rich phase (dilute phase) tends to accumulate at the bottom of the mixing chamber and the two phases (dilute and concentrated) will finally settle as shown in Fig. 2.5 right panel.

In the mixing chamber the 3-He is forced through the phase boundary to enter the dilute phase and absorbs heat as we discussed above. Due to the lack of 3-He in the still by pumping, the osmotic pressure drives the 3-He from the mixing chamber

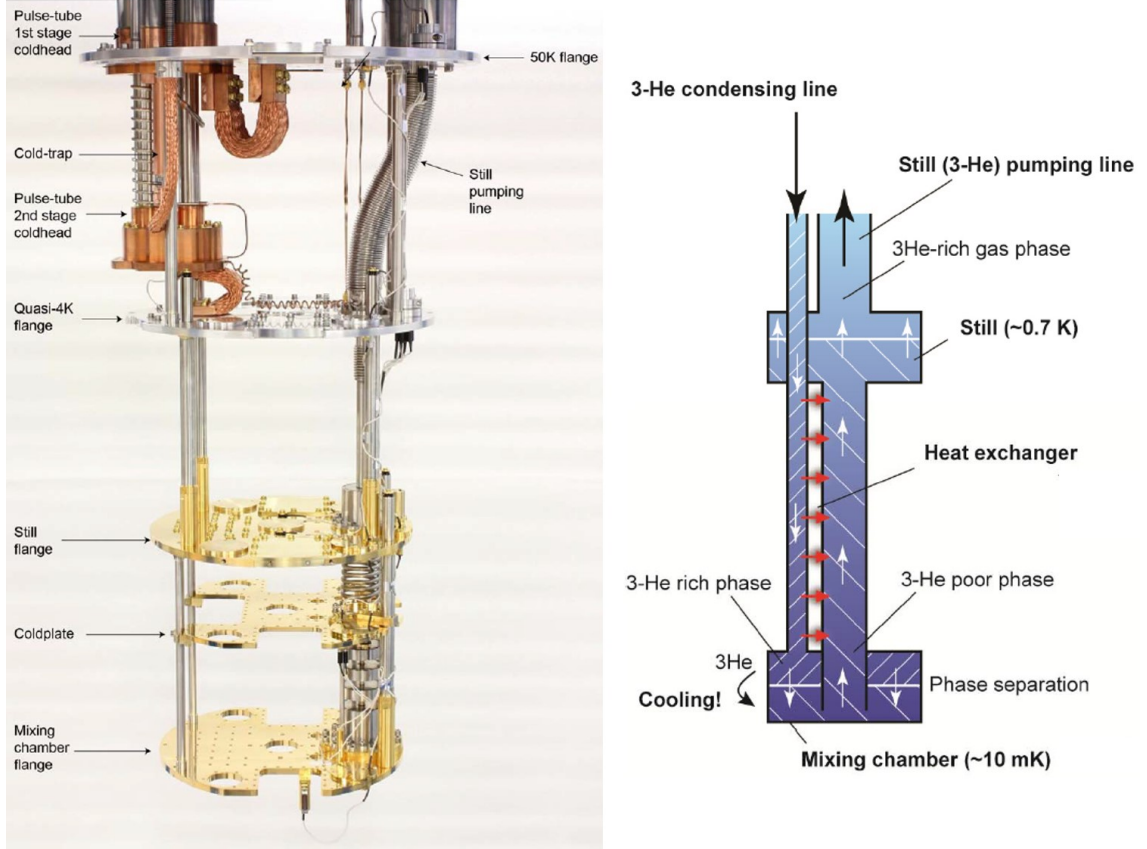


Figure 2.5: (Taken from Ref.[69]) Left panel: the interior of DR cryostat. Right panel: Schematic diagram of the DR circulation.

to the still in the dilute stream. Due to the large difference in vapor pressure between 3-He and 4-He, the helium pumped away from the dilute phase is almost pure 3-He. The 3-He then return into the condensing line of the DR, precooled and rejoin the concentrated phase. The cooling power of the DR depends on the amount of 3-He atoms crossing the phase boundary, which is the flow rate. Usually heat is applied to the still to increase the vapor pressure, obtaining a high enough circulation and flow rate.

2.3.2 4 K Cryogenic System

Shown in Fig. 2.6(a) is a schematic diagram of our 4 K closed cycle cryogenic system (ARS DE-204S). It mainly consists of the expander, radiation shield, vacuum shroud, compressor and vacuum pump [70]. The expander is also known as coldhead, which is where the refrigeration cycle happens. It is connected to the compressor via two gas lines and a power cable. One gas line is the high pressure line, which provides high pressure helium gas to the expander. The other gas line is the low pressure line, which returns low pressure helium gas from the expander. The sample is installed in the coldhead and kept in vacuum isolated from surrounding environment. The radiation shield blocks thermal radiation from the vacuum shroud. The compressor supplies the necessary helium gas flow for the expander to obtain the refrigeration capacity. The electrical power cable drives a motor which turns a valve disc inside the expander. There is also a temperature controller which can read the temperature from the temperature sensors and also provide heat power to heat the system through a PID control.

The cooling mechanism is based on the principle of the Gifford-McMahon refrigeration cycle [71]. The motor rotates the valve disk, which opens the high pressure path. Therefore, the high pressure helium gas is allowed to pass through the regenerating material and go into the lower portion of the expander. There is a displacer assembly inside the lower portion of the expander. After this, the pressure differential drives the displacer up so that the gas at the bottom will expand and cool. Then, the motor continuously to rotate the valve disk, which opens the low pressure

path. Therefore, cold gas is allowed to flow through the regenerating material which removes heat from the system. Finally, the pressure differential drives the displacer back to its original position and the refrigeration cycle repeats.

This 4 K cryogenic system is designed to be compatibly operated in a magnetic field, by inserting the coldhead part where the sample resides into the center of an electromagnet, as shown in Fig. 2.6(b). With this configuration, magnetic field can be applied perpendicularly to the sample surface for performing magnetic field measurements at cryogenic temperatures, as detailed in Section 4.4.

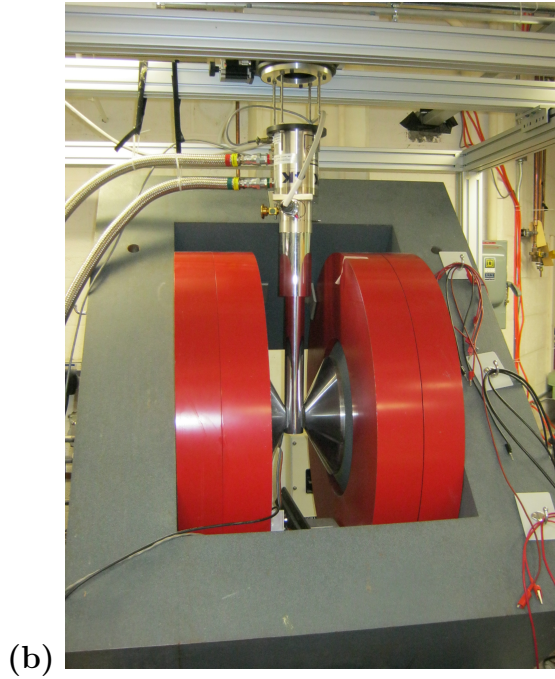
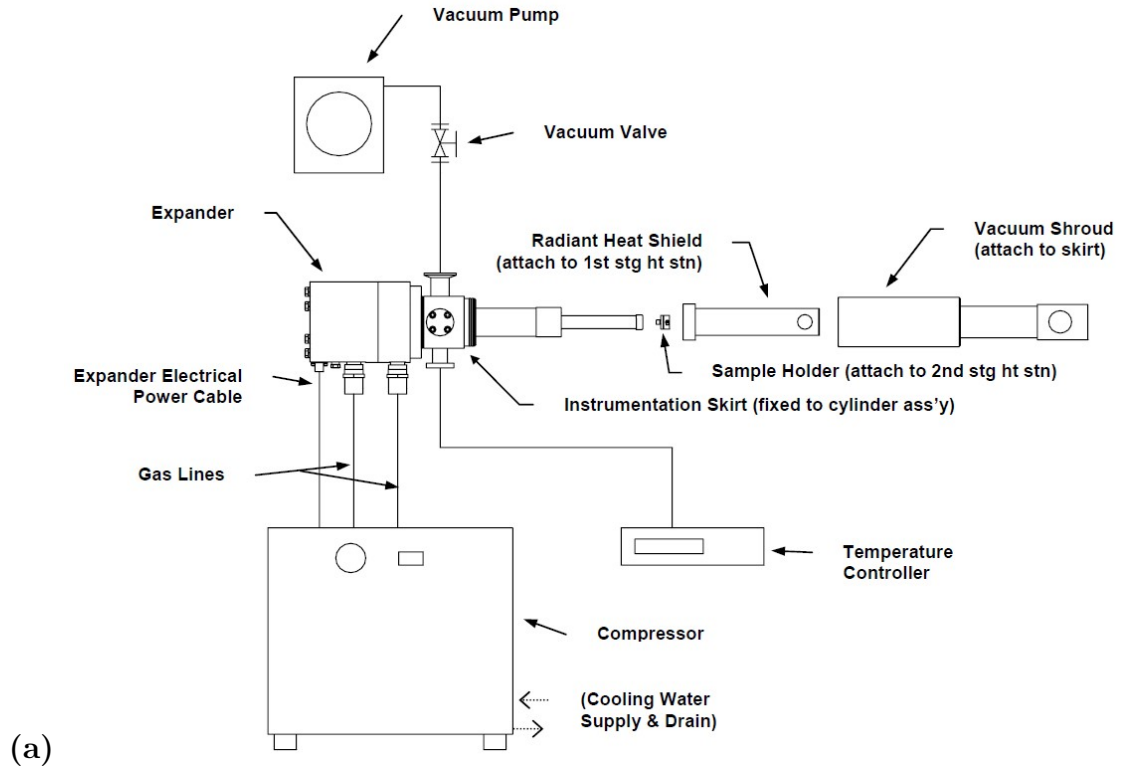


Figure 2.6: (a) (Taken from Ref.[70]) Schematic diagram of our 4 K closed cycle cryogenic system. (b) Photo of coldhead part where the sample resides being inserted into the center of an electromagnet.

Chapter 3: Reducing Charge Offset Drift in Metallic SETs with Plasma Oxidized Aluminum

In this chapter, I will discuss the work on studying and solving the charge instability issue called charge offset drift associated with aluminum oxide (AlO_x), which is an important material in solid-state quantum computing devices. AlO_x is often employed as the gate insulator in silicon-based semiconductor quantum computing devices, and almost ubiquitously as a tunnel barrier in superconducting quantum information architectures. However, AlO_x is frequently reported to have a broad distribution of electrically active defects, including two-level systems (TLSs) [59]. TLSs, believed to arise from the initial nonequilibrium structure of AlO_x [72], have been shown to be the dominant decoherence source in superconducting qubits [73]. Here I report on the excellent charge stabilities over more than a week measured on our AlO_x -based single-electron transistors (SETs) fabricated in ultra-high vacuum (UHV) chambers using *in situ* plasma oxidation. This improvement of charge stability enables applications of AlO_x as tunnel barriers, capacitor dielectrics or gate insulators in close proximity to qubit devices, and also enables the possible device integration of metallic SETs in a quantum computing architecture. Historically, AlO_x -based SETs and gate materials exhibit time instabilities due to charge

defect rearrangements that are observed as abrupt and unpredictable changes in the devices' control parameters. Similarly, in superconducting quantum computing applications, defects in AlO_x often dominate the loss mechanisms such as decoherence, limiting relaxation times and constraining possible qubit choices [59, 72]. To characterize the charge offset stability of our AlO_x -based devices, we fabricate SETs with sub-1 e (e is the elementary charge) charge sensitivity and utilize charge offset drift measurements (measuring voltage shifts in the SET control curve over long periods of time). The charge offset drift (ΔQ_0) measured from the plasma oxidized AlO_x SETs in this work is remarkably reduced (best $\Delta Q_0 = 0.13 \text{ e} \pm 0.01 \text{ e}$ over ≈ 7.6 days and no observation of ΔQ_0 exceeding 1 e), compared to the results of conventionally fabricated AlO_x tunnel barriers in previous studies (best $\Delta Q_0 = 0.43 \text{ e} \pm 0.007 \text{ e}$ over ≈ 9 days and most $\Delta Q_0 \geq 1 \text{ e}$ within one day). We attribute this improvement primarily to using plasma oxidation, which forms the tunnel barrier with fewer two-level system (TLS) defects, and secondarily to fabricating the devices entirely within a UHV system.

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3.1 Introduction

The future of large scale quantum computing depends on successfully merging diverse materials and qubit architectures that each realize different functionalities,

i.e., computation, cache, memory or long range transmission. To accomplish this, quantum information must be efficiently transduced between bases, e.g. superconducting and semiconducting qubits, requiring mutually compatible materials and designs. Specifically within those two realms, aluminum and its native oxides (AlO_x) have enabled great advances, providing simple and reliable tunnel couplings in superconducting circuits [74, 75, 76] and isolation oxides between nanoscale gates for semiconducting qubit control [31, 77]. However, superconducting qubits still suffer from unacceptably high relaxation rates, motivating device designs that minimize AlO_x utilization and the electric field density within the oxides (reduced participation factor). Similarly, aluminum implementation in semiconducting devices is most successful the farther the aluminum is from the sensitive region of the device [30, 31, 78, 79]. In both cases, the amorphous AlO_x formed during thermal oxidation is thought to have a high density of electrically active defects originating from its nonequilibrium structure [72, 73], which interact with the quantum system and create a substantial loss mechanism.

Nonetheless, aluminum and AlO_x remain highly desirable choices due to the nearly ideal WKB-like (Wentzel–Kramers –Brillouin) attenuation of states in the tunnel barriers, i.e., minimal tunneling dependence on angular momentum, spin, etc., and their compatibility with nanofabrication techniques. Therefore, efforts to identify and suppress the instabilities of AlO_x are of great significance for enhancing qubit performance. Further, establishing stable aluminum oxides enables expanded use of metallic single-electron transistors (SETs), to be used as surface mounted charge sensors, reducing the density of in-plane circuit elements. These charge

sensors could, for example, provide projective spin readout through spin-to-charge conversion techniques already demonstrated [30, 80, 81].

SETs are considered to be the world’s most sensitive electrometers, with the capability of detecting the motion of individual electrons or charge instabilities [36, 52, 82, 83, 84]. The same sensitivity that enables exquisite readout of a target qubit is also susceptible to any other charge motion within the local environment, e.g., unintentional charge defects. Therefore, these characteristics of SET sensitivity can be employed to probe whether sufficiently stable charge environments can be realized, e.g., to what extent the instabilities of AlO_x are suppressed.

Here we utilize one characteristic of SETs, known as charge offset drift, to evaluate the material stability of our plasma oxidized aluminum. Typically, the dependence of the SET’s source-drain current I_s on the gate voltage V_g , which is the SET’s control curve, has a periodic behavior with each period corresponding to a 1 e change in the island’s net charge. The period is determined by the coupling capacitance between the gate and the SET island. When the source-drain bias $V_d \approx 0$, the control curve looks like a series of sharp peaks, but at modest bias (temperature), i.e., $0 < eV_d(k_B T_e) < E_C$, the control curve smooths out similar to a sinusoid, where E_C is the charging energy of the SET island, k_B is the Boltzmann constant, e is the elementary charge and T_e is the effective electron temperature. The phase of the control curve corresponds to the voltage offset between consecutively measured curves. The difference in phase of different curves is referred to as charge offset, denoted by $Q_0 = \frac{\text{phase}}{\Delta V_p} e$, which originates from the device’s local electrostatic environment that is affected by different fabrication procedures. If there exists

random fluctuation in the SET’s local electrostatic environment, the phase of the SET’s control curve (Q_0) will then exhibit time instability referred to as charge offset drift, ΔQ_0 [36]. Therefore, the time trace of the phase is a sensitive indicator of SET’s charge stability and charge offset drift (ΔQ_0) can be used to quantitatively evaluate this stability.

Extensive prior work examining the charge offset stability of various devices showed that metallic SETs incorporating AlO_x tunnel barriers demonstrate the largest charge offset drift ($\Delta Q_0 \gg 1e$), while silicon SETs show very small charge offset drift ($\Delta Q_0 \ll 0.1e$). In addition, silicon SETs with aluminum gates exhibit intermediate charge offset drift ($\Delta Q_0 \approx 0.1e$). [36, 52, 53, 82, 83, 84, 85] The large, abrupt phase changes leading to large ΔQ_0 in metallic SETs are attributed to two-level system (TLS) defects associated with amorphous AlO_x , consistent with similar findings from TLS spectroscopy studies in the context of superconducting qubits [86, 87, 88]. In our group’s prior work, we mitigated long-term, macroscopic resistance drift using plasma oxidized AlO_x tunnel barrier devices [89], a behavior thought to originate from the same bath of defects that causes significant charge offset drift [90, 91]. Plasma oxidation, compared to conventional thermal oxidation, incorporates higher oxygen content in the barrier layer at a considerably faster rate, resulting in a much better initial quality [62, 63, 92]. To explore whether the macroscopic improvements seen in plasma oxidized AlO_x improve the feasibility for AlO_x use in quantum computing applications, we fabricated metallic SETs with plasma oxidized AlO_x tunnel barriers and measured their long-term charge offset drift. We find these devices exhibit significantly reduced charge offset drift – the

best $\Delta Q_0 = 0.13 \text{ e} \pm 0.01 \text{ e}$ over ≈ 7.6 days and no observation of ΔQ_0 exceeding 1 e, compared with any other previously reported metallic SETs [36, 53, 84, 93] where the best $\Delta Q_0 = 0.43 \text{ e} \pm 0.007 \text{ e}$ over ≈ 9 days and most $\Delta Q_0 \geq 1 \text{ e}$ within one day. We attribute this improvement to i) using plasma oxidation to form the tunnel barriers and ii) fabricating the devices entirely within a system of ultra-high vacuum (UHV) chambers.

3.2 Device Fabrication

In order to reduce the fabrication time and increase the device volume, the macroscopic contact electrodes and interconnects are fabricated first by wafer-scale photolithography, sputter deposition of 10 nm titanium and 50 nm gold, and a subsequent lift-off process. Next, the device fine structures are fabricated by double angle, shadow evaporation techniques [94], as illustrated in Fig. 3.1. The processes are as follows: first, double layer electron-beam (e-beam) resist (methyl methacrylate – MMA, and polymethyl methacrylate – PMMA) is spin coated on the SiO_2/Si substrate wafer and patterned by high-resolution e-beam lithography. The thickness of each resist layer is approximately 150 nm as the undercut room is feasible for conducting double-angle deposition using our material stacks without any metal lift-off issues. With thicker material stacks, the deposited material may clog the patterned openings on the resist in the first deposition and affect the deposition angle in the second deposition. In that case, the deposition angle in the first deposition should be considered to be closer to the normal deposition in order to not clog

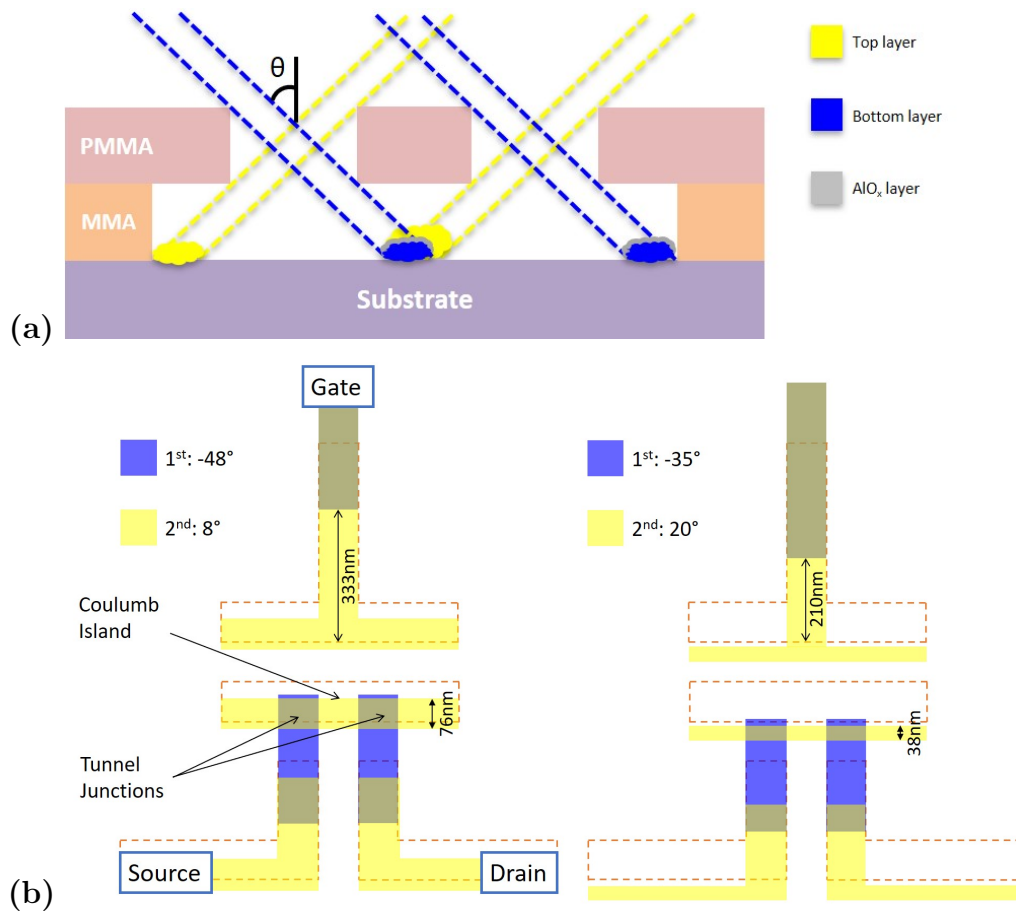


Figure 3.1: (a) Cross-sectional cartoon illustrating double angle, shadow evaporation and the formation of tunnel junctions. (b) Plan-view cartoon demonstrates that size of tunnel junctions can be varied by manipulating deposition angles.

the openings too much. Also, thicker material stacks (≈ 100 nm total thickness) could cause lift-off issues, even if it does not exceed the bottom layer resist thickness, as shown in our early tests. By controlling the e-beam dose, we can form an undercut in the bottom MMA resist layer as shown in Fig. 3.1(a). Fig. 3.2 shows the dose test we did to find the optimal e-beam dose for desired device patterns. Fig. 3.2(a) is the SEM image of the device pattern after e-beam lithography and resist development. The dimensions of six different positions denoted in Fig. 3.2(a) were measured for different doses and plotted in Fig. 3.2(b) and (c). Considering the metal deposition effects and sufficient undercut for forming tunnel junctions, e-beam dose of $1500 \mu\text{C}/\text{cm}^2$ was chosen for the coarse region and $1800 \mu\text{C}/\text{cm}^2$ was chosen for the fine region to ensure no resist residue in the region of tunnel junctions. All of the steps leading up to deposition of the fine structure are performed *ex situ* in a nanofabrication facility.

Once the large-scale fanout and nano-scale lithographic stencils are complete, the wafers are loaded into our customized system of UHV chambers with a base pressure of $< 10^{-7}$ Pa (10^{-9} Torr) equipped with deposition and plasma oxidation capability (see Ref. [89] for equipment details) for the metalization of fine structures. It is noted that the e-beam resist residue descum before this metalization step is done in our oxygen plasma chamber so that we can keep the sample in the UHV environment (except for the short time when the chamber is filled with oxygen/plasma) until the completion of metalization without being exposed to the atmosphere. To find out the appropriate oxygen plasma etch time for e-beam resist descum and also study the impact of our plasma oxidation on the e-beam resist, we

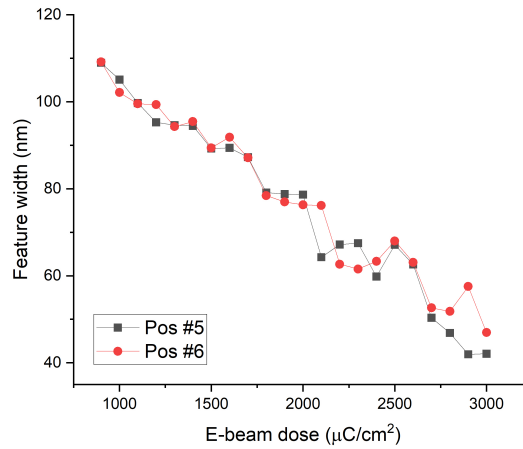
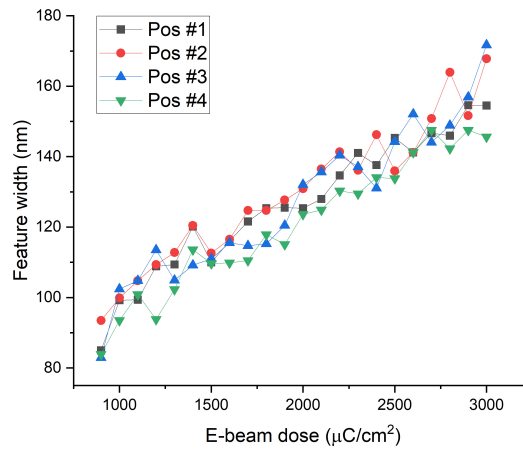
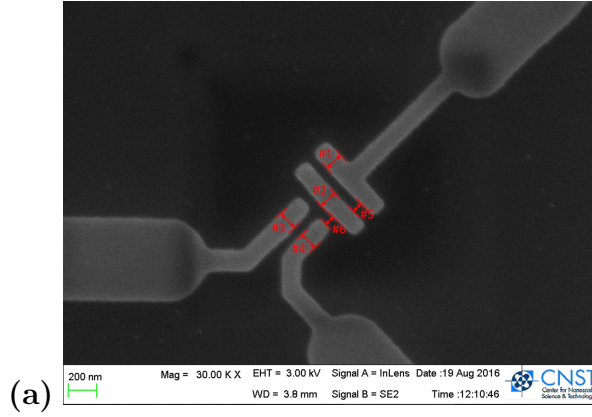


Figure 3.2: E-beam lithography dose test. (a) SEM image of the device pattern after e-beam lithography and resist development. (b) and (c): The measured dimensions of six different positions denoted in (a) with varying e-beam doses.

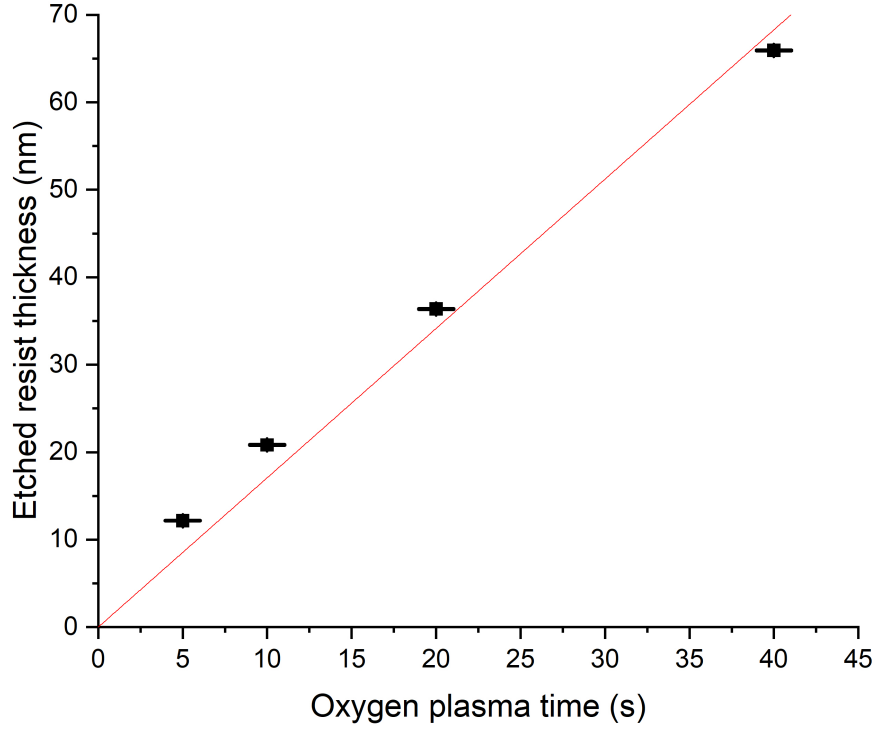


Figure 3.3: Ellipsometry measured thickness difference before and after plasma process (etched thickness) of e-beam resist vs the oxygen plasma time. Black dots denote the data and red line is the linear fit. The measurement uncertainties are within ± 0.05 nm. The etch rate obtained from the linear fit is approximately 1.7 nm/s.

conducted a series of tests to study the resist etch rate of our oxygen plasma – DC plasma at 21 Pa / 160 mTorr of research grade oxygen with 57 W to 60 W for some amount of time. These parameters of oxygen plasma are what we use for forming AlO_x and were optimized for optimal performance of plasma oxidation, as detailed in Section 2.2. Four test wafers were coated with double layer e-beam resist using the same recipe and undergone oxygen plasma for 5 s, 10 s, 20 s, and 40 s. The e-beam resist thickness were measured by ellipsometry before and after oxygen plasma etch, respectively. Fig. 3.3 shows the ellipsometry measured thickness difference before and after plasma process (etched thickness) of e-beam resist vs the oxygen plasma time. The etch rate obtained from the linear fit is approximately 1.7 nm/s. The plasma time selected for resist descum is 5 s, which corresponds to etching ≈ 10 nm resist and is sufficient to remove resist residual without damaging the device pattern. After resist descum, the wafer is transferred to the deposition chamber for metal deposition of the device fine structure without leaving UHV environment. The sample transferring and structure of UHV chambers are described in details in Section 2.1. As shown in Fig. 3.1(a), we first deposit the bottom layer (2 nm cobalt as a sticking layer and then 20 nm aluminum, 0.01 - 0.02 nm/s with pressure $< 10^{-9}$ Torr) at the first angle (35°). Then the wafer is transferred to the plasma chamber again where the surface of the bottom aluminum layer is oxidized using oxygen plasma with the aforementioned parameters for 7 s, as illustrated in Fig. 3.1(a). The oxide is then allowed to relax in vacuum for at least 12 h before the top layer is deposited, consistent with prior work [89] mitigating resistance drift. Empirical results have shown that depositing the top layer directly after the oxida-

tion can lead to higher resistance drift of the tunnel junctions, which is not desired. The AlO_x layer produced under this condition is 2.03 ± 0.10 nm thick, extracted using the WKB transport model [89]. Note that although plasma can attack the e-beam resist used for shadow evaporation, the influence of oxygen plasma on the e-beam pattern at this step is not critical since most part of the resist has been coated by the metal in the first deposition and the uncoated part is not that sensitive to < 15 nm loss according to our calibration in Fig. 3.3. The wafer is then transferred back to the deposition chamber where 30 nm aluminum is deposited at the second angle (20°) for the top layer (0.01 - 0.02 nm/s with pressure $< 10^{-9}$ Torr), as shown in Fig. 3.1(a). Overlapping of the two deposited layers at the SET island (Coulomb island) form the SET tunnel junctions – one AlO_x layer sandwiched by two aluminum layers. By manipulating the two deposition angles, we can control the size of the tunnel junctions, as demonstrated in Fig. 3.1(b) and detailed below.

Fig. 3.4(a) shows a false-color scanning electron microscope (SEM) image of the device fine structure with a schematic cross-section through the tunnel junction in Fig. 3.4(b). The blue part is the bottom layer and the top layer is shown in green. It can be observed that, in addition to the tunnel junctions, other parts of the device (source, drain and gate) also consist of overlapping of two layers, with a thin layer of AlO_x sandwiched in between. According to the resistance property of layered materials – resistance area product is constant for the same layer, resistance of AlO_x in these parts is several orders of magnitude smaller than the tunnel junctions due to the large area. Therefore, the lead resistance is negligible compared to the tunnel junction resistance in the SET circuit. In our case of plasma oxidized AlO_x

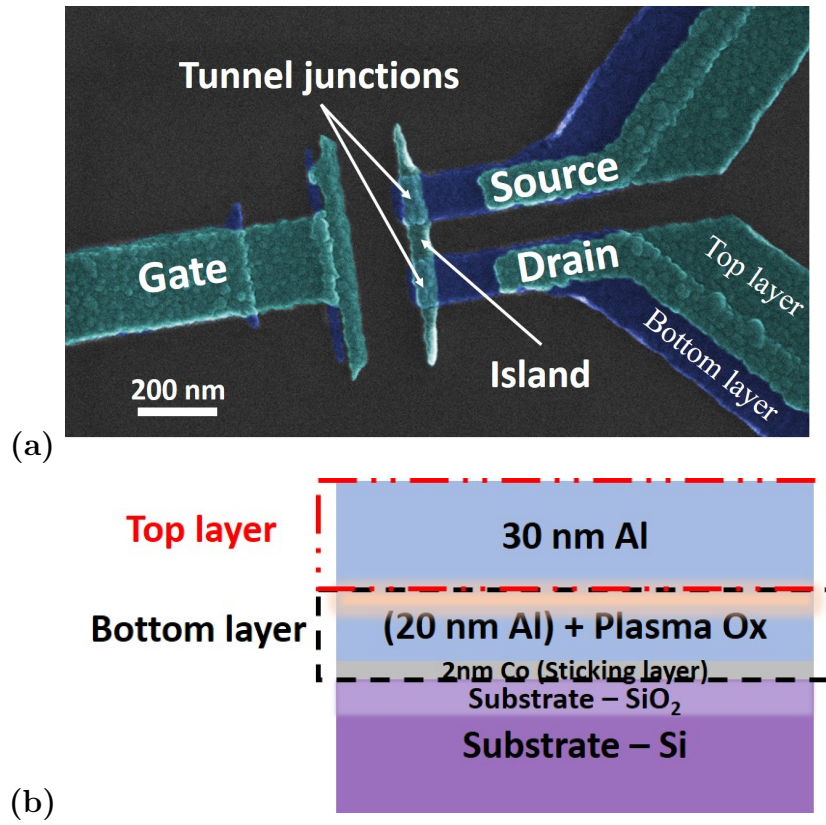


Figure 3.4: (a) False-colored SEM image of an Al/AIO_x/Al SET identical to the one discussed in this chapter. The blue part is the bottom layer with plasma oxide on the surface and the green is the top layer. (b) A cross-sectional cartoon through the tunnel junction of the Al/AIO_x/Al SETs.

SETs, the resistance of a single tunnel junction is usually in the order of magnitude of tens of $M\Omega$, as is closer to stoichiometric Al_2O_3 [62]. By controlling the deposition angle, the size of the island and tunnel junctions can be controlled to a precision of < 5 nm along the direction of rotation. Additionally, the pattern is designed so that, depending on angle, some features do not appear in both layers. For example, we only want the island and the bar of the gate to appear in the top layer, as shown in 3.4(a). During the deposition steps, a liquid nitrogen cryoshroud is kept cold to insure high vacuum ($< 10^{-9}$ Torr). The substrate temperature begins at ambient temperature and is expected to warm somewhat. By combining e-beam lithography with photolithography, the total lithographic exposure time is < 1 h for a 75 mm wafer with 100 devices. Fig. 3.5 show a complete device wafer consisting of 25 dies, with each die containing four SET devices and two test devices. The die size of 10×10 mm is chosen for fitting the sample box of our dilution refrigerator (detailed in Section 5.2.2) and the distribution of the device bonding pads are designed to fit the bonding pads of the sample box. The two types of test devices are for measuring the lead resistances of optical layer and e-beam layer, respectively.

3.3 Electrical Measurements and Results

3.3.1 Device Design and Characterization

When a metallic island is separated from source and drain reservoirs by tunnel junctions, the resulting SET can confine an integer number of electrons on the island. As a result of this charge quantization, the charging energy required to add

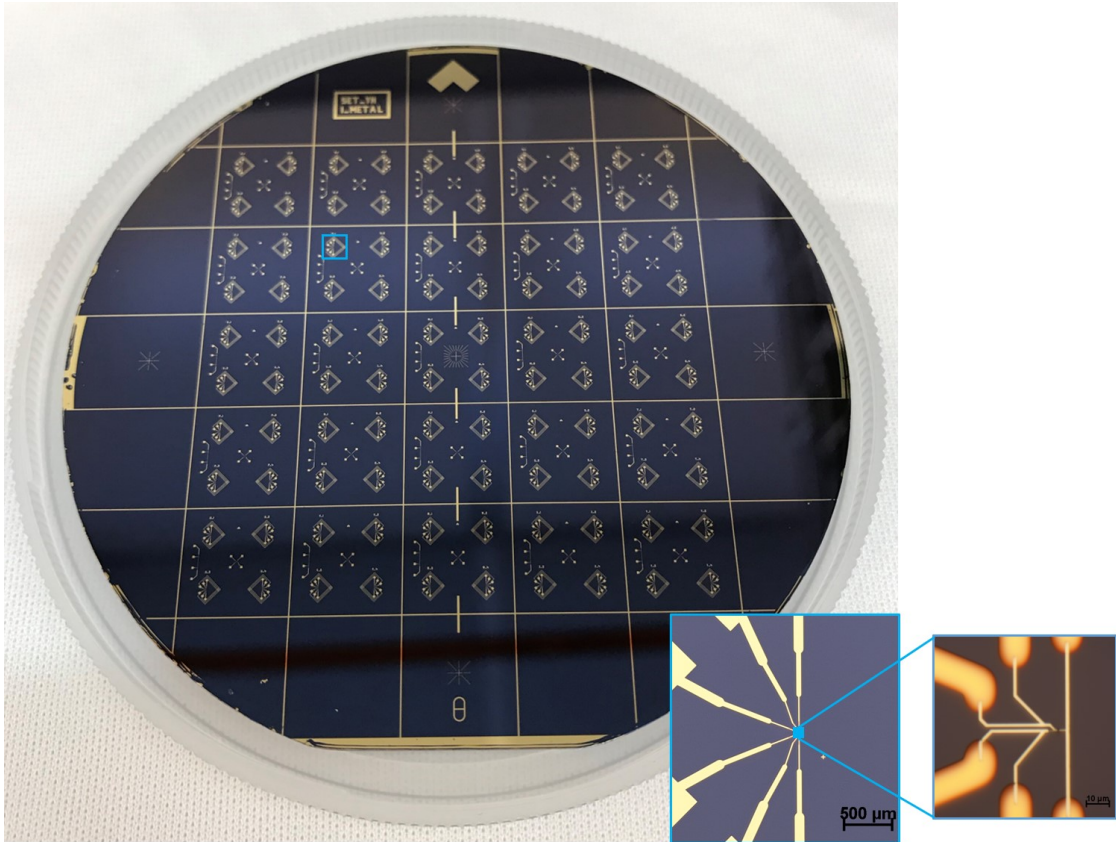


Figure 3.5: A complete SET device wafer consisting of 25 dies, with each die containing four SET devices and two test devices. Inset: optical microscope image of an SET device.

or remove a single electron from the island is $E_C = e^2/C_\Sigma$, where e is the charge of a single electron and C_Σ is the island's total capacitance. Coulomb blockade due to discrete electron charges is strongly visible when: i) the tunnel junction conductances $\ll 2e^2/h$ (h is the Planck constant), and ii) $k_B T_e \ll E_C$ [35]. The first criterion requires that the tunnel barriers are sufficiently opaque such that the electrons can be confined on the island. The second criterion requires that the charging energy exceeds the thermal energy for the charge quantization on the island to be observed. If the bias $V_d \ll E_C/e$, then the spacing between single electron energy levels is larger than the bias window V_d and for some values of V_g no energy levels on the island will fall within the bias window. In that case, the source-drain current I_s can be ≈ 0 , known as Coulomb blockade, as detailed in Section 1.1. When a single electron energy level on the island does fall within the source-drain bias window, then electrons can tunnel on and off of the island, producing a source-drain current I_s . The maximum of I_s is reached when an energy level is fully within the bias window, producing a conductance peak that may be broadened by bias or temperature. As V_g is swept, different energy levels move through the bias window, producing a periodic current oscillation vs V_g , referred to as Coulomb blockade oscillation (CBO). The oscillation period ΔV_g is determined by the capacitance between the gate and the island, $\Delta V_g = e/C_g$. Since the total charge on the metallic island is $\gg 1$ e, C_g is approximately constant and the charging energy is assumed constant [95]. When the temperature or bias becomes comparable to the charging energy, these peaks merge into oscillations that are nearly sinusoidal.

To conduct the charge offset drift measurements, the samples are cooled in a

cryogen-free dilution refrigerator (DR) with a base temperature of approximately 10 mK. As shown in Fig. 3.4(a), the SET consists of a small conducting island coupled to the source and drain electrodes through two Al/AlO_x/Al tunnel junctions. The gate electrode is capacitively coupled to the island and manipulates the electrostatic potential via the gate voltage V_g , modifying the charge configuration of the island. A small, constant DC bias, $V_d \approx 0.5$ mV, is applied on the drain electrode while measuring the current via a transimpedance amplifier on the source electrode, I_s . On the time scale of seconds, the standard deviation/typical noise of the current and voltage are ≈ 0.06 pA (see Fig. 3.14) and ≈ 5 μ V [96], respectively. The device's control curve is observed by measuring I_s vs V_g applied on the gate electrode. A typical charge offset drift measurement involves repeatedly measuring this control curve every few minutes for about one week, as discussed further below.

The devices used in this study and shown in Fig. 3.4 are designed to exhibit Coulomb blockade behavior at temperatures < 1 K, with designed single tunnel junction size of 40 nm by 100 nm. Based on the lithographic design and SEM images of similar devices, we estimate the single tunnel junction dimensions are (47 ± 10) nm by (109 ± 10) nm. Using a parallel plate capacitor model with an AlO_x permittivity of $(10.4 \pm 1.1) \cdot \epsilon_0$ and a thickness of (2 ± 0.2) nm, we estimate each junction capacitance to be (236 ± 65) aF (ϵ_0 is the vacuum permittivity). A gate capacitance of (6.9 ± 3.1) aF was calculated by modelling a gate of (560 ± 50) nm $\times$ (80 ± 10) nm $\times$ (40 ± 10) nm (length $\times$ width $\times$ height) and an island of (560 ± 50) nm $\times$ (47 ± 10) nm $\times$ (40 ± 10) nm with a separation of (145 ± 10) nm on a SiO₂/Si substrate using the capacitance solver FastCap and a

SiO₂ permittivity [97] of $3.9 \cdot \epsilon_0$ and thickness of 100 nm. Therefore, a CBO period of (23.2 ± 10.4) mV is expected on these devices. Adding up these capacitance gives an expected charging energy, $E_C/k_B = (3.9 \pm 1.1)$ K, which agrees well with the experimental results shown in the next section.

3.3.2 Charge Offset Drift Measurement

In prior studies of Al/AlO_x/Al SETs, the local electrostatic environment of the island would often change with time randomly, which appears as the phase of the CBO fluctuating with time. This time instability, referred to as charge offset drift, has been an issue in metallic SET devices for a long time. Many factors contribute to the vulnerable electrostatic environment of the island, including unintentional charge defects from multiple fabrication processes, temporal or thermal material relaxation, circuit noise, etc.

Fig. 3.6(a) illustrates an example CBO from one of our plasma oxidized Al/AlO_x/Al SETs (W119-C1) at the base temperature of ≈ 10 mK, with oscillations from each single electron conductance peak moving through the bias window as V_g is swept. In this case, the bias voltage $V_d \approx 0.5$ mV is applied on the drain electrode, with the current measured on the source held at ground, and the current oscillates sinusoidally. The nonideal broadening is believed to be due to a noise-induced high T_e , which prevents complete Coulomb blockade, discussed further below. The nonzero current offset observed in the CBO is attributed partially to the merged peaks and an imperfect zero on the current preamplifier. For

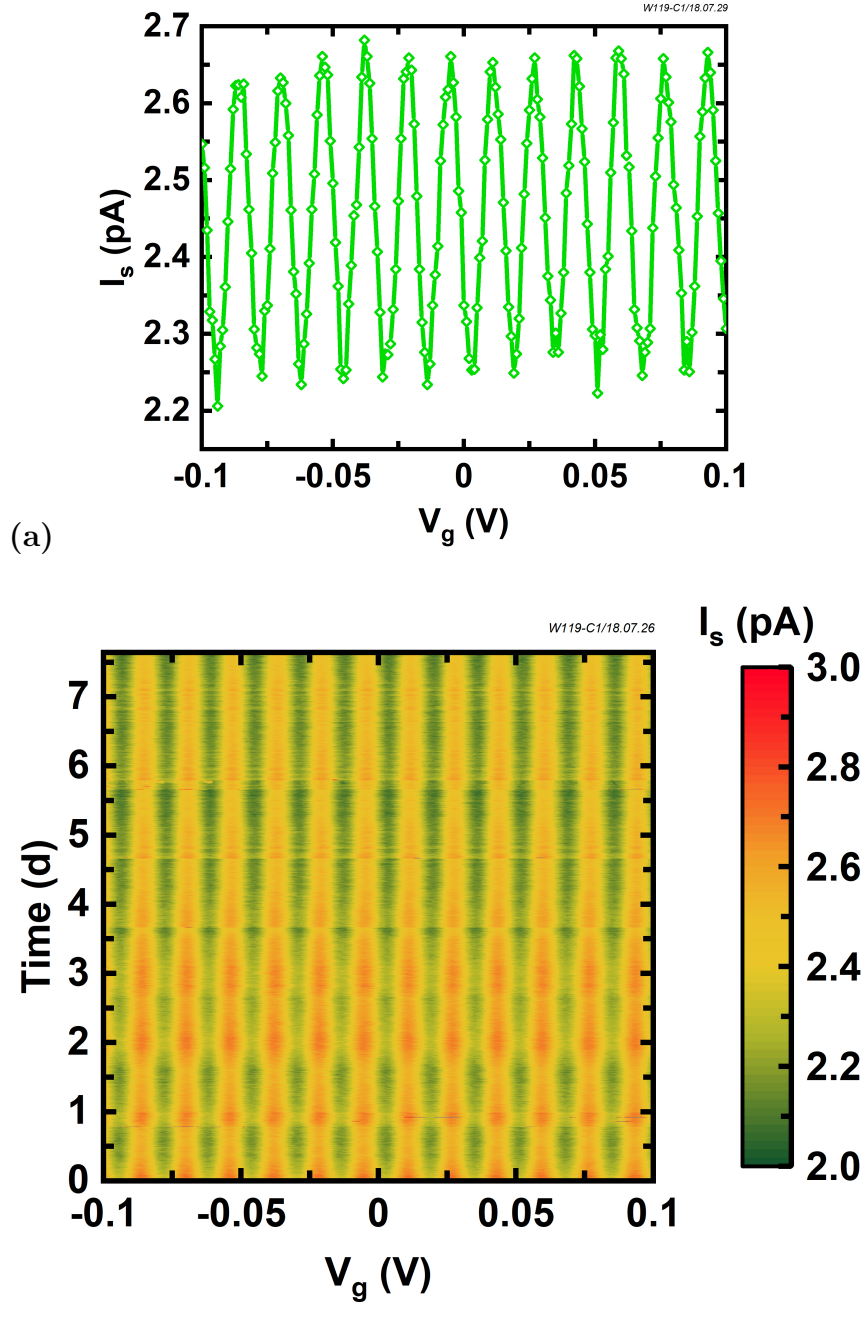


Figure 3.6: (a) A representative I_s vs V_g CBO from device W119-C1 at ≈ 10 mK with an applied bias $V_d \approx 0.5$ mV taken from $t \approx 2.3$ d in panel (b), a color map of I_s vs V_g spanning > 1 week. The vertical stripes indicate that the CBO phase remains stable with time.

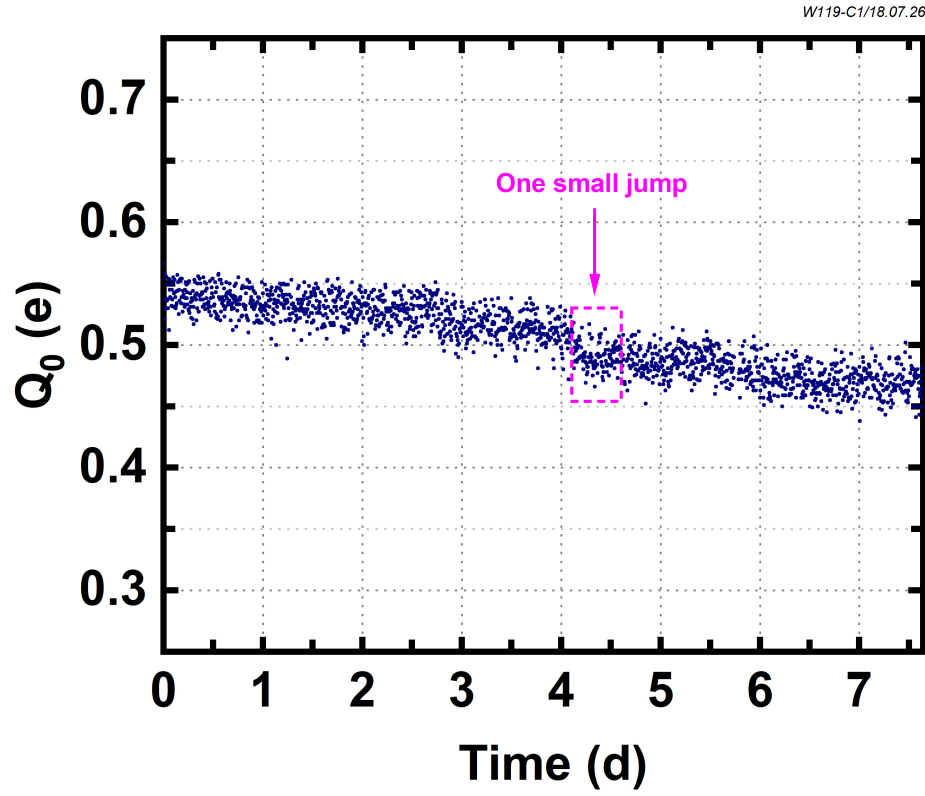


Figure 3.7: The charge offset, Q_0 , extracted from the phase in Fig. 3.6(b), as a function of the time.

this device, the oscillation period $\Delta V_g = (16.26 \pm 0.04)$ mV, from which the gate capacitance $C_g = e/\Delta V_g \approx 9.8$ aF, is in agreement with the design estimate of (6.9 ± 3.1) aF.

To evaluate the charge offset stability in our plasma oxidized SETs, the CBO is repeatedly measured every five minutes over many days for device W119-C1. The result of this long-term repetitive measurement is shown in Fig. 3.6(b). For each V_g sweep, the value on the y-axis is the time when that sweep ends. The color scale on the z -axis represents the I_s value measured from the source electrode. The high and low current values form vertical stripes in time, which clearly show that the CBO phase in our Al/AlO_x/Al SET remains quite stable without sudden shifts over the course of more than 7 days. Compared to the results from Al SET devices with thermally oxidized AlO_x tunnel barriers where frequent, abrupt shifts were observed in the CBO phase [36, 53, 84, 93], this device exhibits much improved charge offset stability.

To numerically evaluate the stability, we extract the charge offset, Q_0 , from the repeated sweeps. Here we use two methods for extracting Q_0 data compared in this work and the two methods are consistent within 10 %, verified by Hu et al. [98] If the source-drain current oscillates nearly sinusoidally as a function of the gate voltage, the measured I_s vs V_g is fit to:

$$I_s^t(V_g) = A_s \cdot \sin[2\pi(V_g/\Delta V_g + Q_0^t/e)] + I_0 \quad (3.1)$$

where A_s is the oscillation amplitude, Q_0^t is the phase for a given t and I_0 is a

nonideal offset. For each line in Fig. 3.6(b), the measured current data is fit to Eq. 3.1. Then the charge offset as a function of each sweep, $Q_0(t)$ as a set of Q_0^t , is plotted as a function of time in Fig. 3.7. These data do not exhibit the dramatic, abrupt jumps characteristic seen in devices of prior work (one small jump exists from $t \approx 4.1$ d to $t \approx 4.7$ d), but do show a slow, linear drift of $(-8.1 \pm 0.6) \times 10^{-3}$ e/d. The total charge offset drift over ≈ 7.6 days is $\Delta Q_0 = (0.13 \pm 0.011)$ e, where ΔQ_0 is defined as the full range of Q_0 values measured and the uncertainty is calculated as the standard deviation of 100 data points in a stable range (from ≈ 4.8 d to ≈ 5.2 d). For previously reported metallic SETs with thermally oxidized Al/ AlO_x /Al tunnel junctions, most ΔQ_0 are much greater than 1 e and show many abrupt jumps [36, 53, 84, 93].

When the SET control curve displays sharper peaks and cannot be well fit sinusoidally (see Fig. 3.8(a)), individual peaks of the CBO are fit to a Gaussian to locate the peak's center position:

$$I_s(V_g) = I_0 + A_g \cdot \exp[-((V_g - V_c)/V_w)^2] \quad (3.2)$$

Here, A_g , V_c and V_w denote the area/height parameter, center position and full width at half maximum (FWHM) of each Gaussian peak, respectively. In this case, $Q_0(t) = e \cdot \text{mod}[V_c(t)/\Delta V_g]$, where ΔV_g is the gate voltage difference between two adjacent peaks. $Q_0(t)$ data from device W119-C3 (shown in Fig. 3.9) is calculated in this way. The long-term charge offset drift on devices W119-C1 and W119-C3 are measured at the same time. From the CBO shown in Fig. 3.8(a), we can

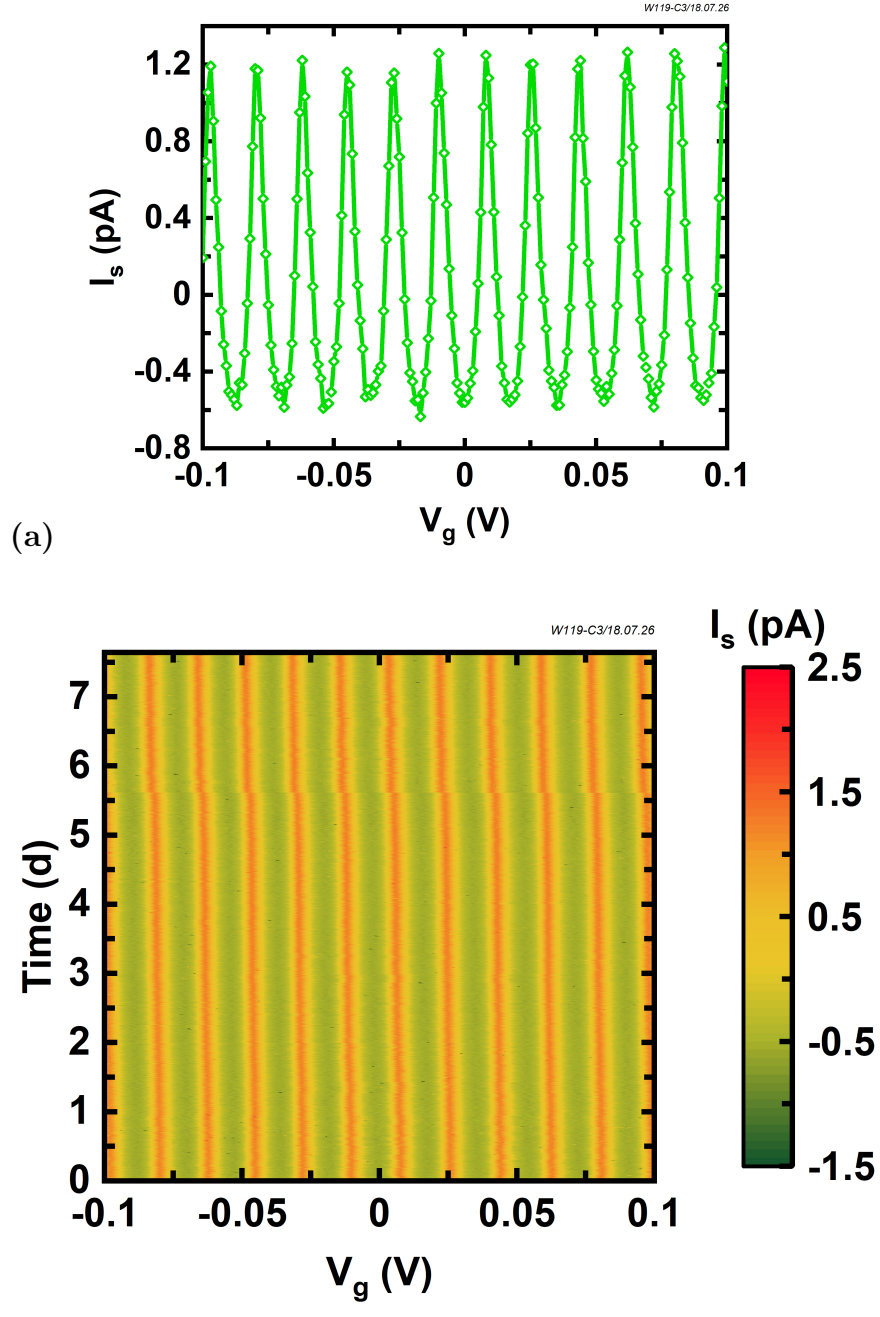


Figure 3.8: Charge offset drift measurement results on W119-C3. (a) An example CBO at ≈ 10 mK with an applied bias $V_d \approx 0.5$ mV taken from $t \approx 5$ h from panel (b), a color map of I_s vs V_g spanning > 1 week.

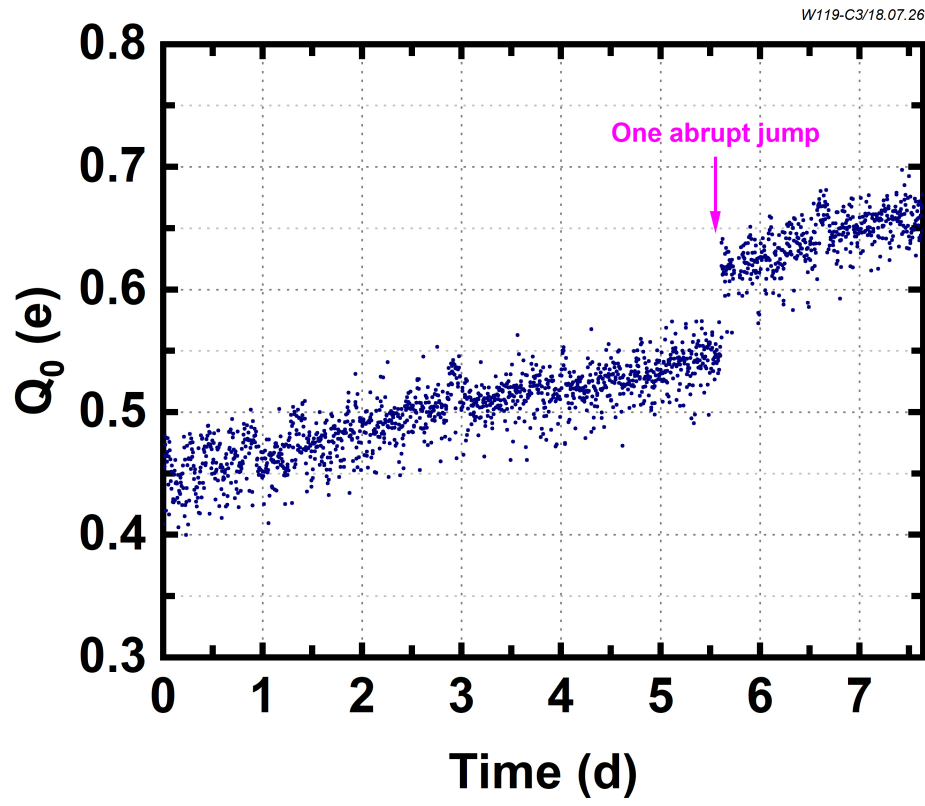


Figure 3.9: The charge offset, Q_0 , extracted from the phase in Fig. 3.8(b), as a function of the time.

see that device W119-C3 exhibits larger oscillation period $\Delta V_g = (17.9 \pm 0.5)$ mV but narrower peak width (FWHM = $6.3 \text{ mV} \pm 0.3 \text{ mV}$ for a typical peak at base temperature) compared to device W119-C1 ($\Delta V_g = 16.26 \text{ mV} \pm 0.04 \text{ mV}$ and FWHM = $10.7 \text{ mV} \pm 0.7 \text{ mV}$ for a typical peak at base temperature). This results in a smaller linewidth/period ratio, which suggests lower noise/temperature than W119-C1. Again, the nonzero current offset (negative in the case of W119-C3) observed in the CBO is attributed to an imperfect zero on the current preamplifier. Two different preamplifiers were used on each device and had different current offsets. It can be observed from the long-term repetitive CBO in Fig. 3.8(b) and the charge offset ($Q_0(t)$) data in Fig. 3.9 that, device W119-C3 shows one abrupt jump of $\delta Q_0 \approx 0.07 \text{ e}$ after $t \approx 5.6 \text{ d}$ of measurement, but is otherwise stable with a linear drift of $(21 \pm 1) \times 10^{-3} \text{ e/d}$. In this device, we find the ΔQ_0 over ≈ 7.6 days is $(0.30 \pm 0.014) \text{ e}$.

We also fabricated devices with different geometries. Fig. 3.10(a) shows the SEM image of two SET islands parallel to each other. The blue part represents the bottom layer with plasma oxide on the surface and the green is the top layer. The top/bottom SET is reflection of each other with an “in-line” arrangement. Shown in Fig. 3.10(b) and Fig. 3.11 are the measured charge offset drift and extracted $Q_0(t)$ data on an in-line Al/AlO_x/Al SET (W119-T1-2, bottom device of the mirror configuration), which was interrupted by other experiments several different times, represented by the breaks on the time scale. Jumps in the current offset value are due to other circuit nonidealities in the low bias regime. Due to the stronger gate capacitance resulted from this geometry, this device exhibits a smaller oscillation

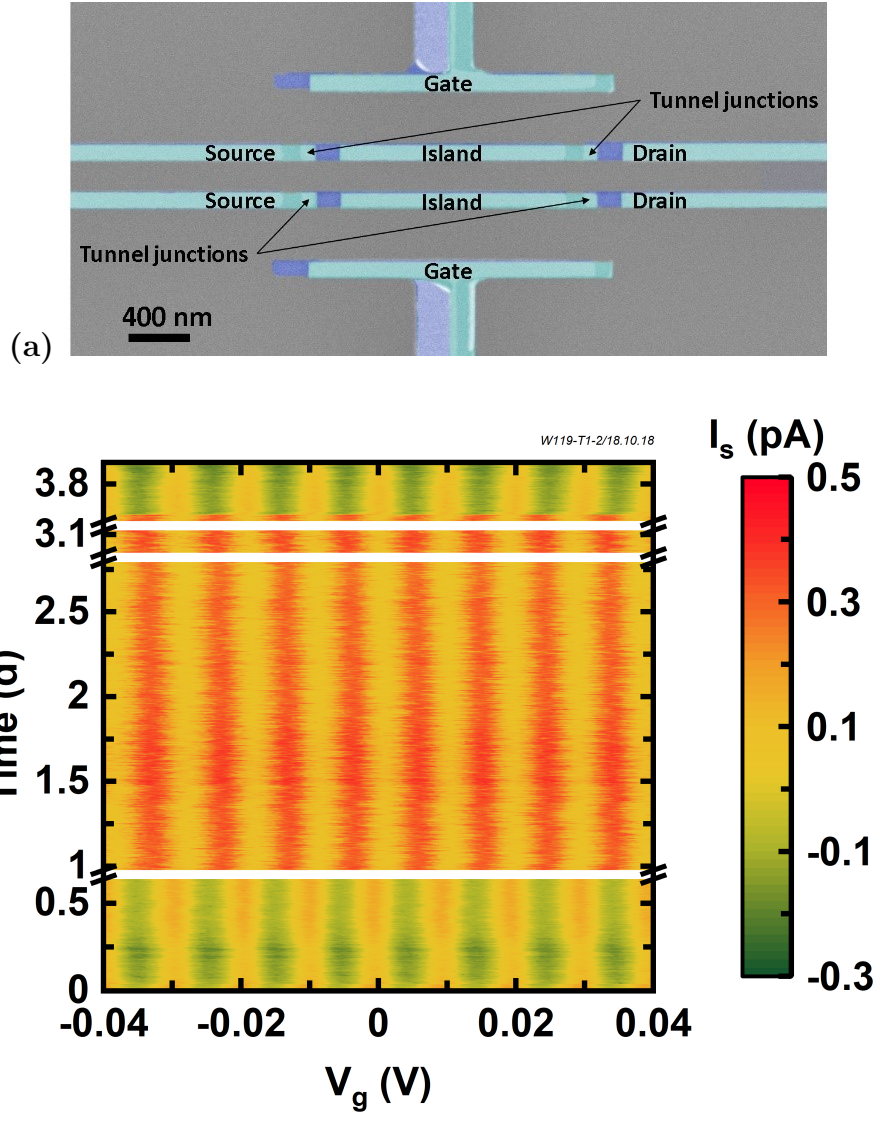


Figure 3.10: In-line SET devices and corresponding charge offset drift measurement result. (a) False-colored SEM image of in-line SET devices. (b) Long-term repetitive CBO taken over ≈ 3.9 days as a function of time. The charge offset drift measurement was interrupted by other experiments several different times, represented by the breaks on the time scale.

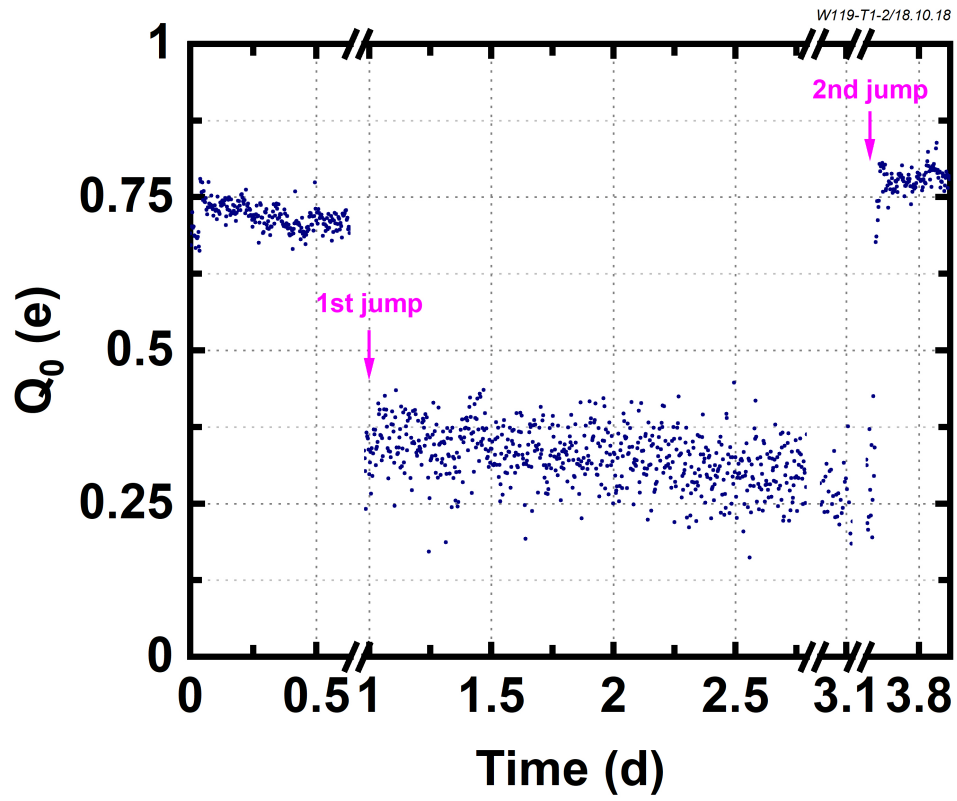


Figure 3.11: The charge offset, Q_0 , extracted from the phase in Fig. 3.10(b), as a function of the time.

period ($\Delta V_g = 9.8 \text{ mV} \pm 0.5 \text{ mV}$) as expected, from which a gate capacitance of $C_g \approx 16 \text{ aF}$ is extracted. The total charge offset drift extracted using Sine method is, $\Delta Q_0 = (0.68 \pm 0.038) \text{ e}$ over ≈ 3.9 days with multi-hour breaks. We can see that the oscillation phase and current level fluctuate between measurement intervals, but are stable within an interval. In the middle period of the measurements, there is a 180° phase shift from the beginning, but the phase stays stable for more than two days regardless of the interruptions.

3.3.3 Attempt for Charge Sensing

Capacitance (aF)	Top gate	Bottom gate
Top island	16.2	13.3
Bottom island	12.7	16.7

Table 3.1: Extracted gate-island capacitances of mirror configured in-line SETs.

The more compact “in-line” structure is designed for being integrated with other quantum devices as charge sensors in the future. In this case, we care about the gate control on the SET island that will be used as charge sensor and the effect of the gate manipulation on the other channel that will be used as target dot to be sensed, which will be discussed in Chapter 6. Therefore, with the mirror configuration shown in Fig. 3.10(a), we measure the gate manipulation of both gates on both SET islands, as shown in Fig. 3.12 and extract the gate-island couplings as shown in Table 3.1. In Fig. 3.12, “Ts” is the top device’s source, “Tg” is the top device’s gate, “Bs” is the bottom device’s source and “Bg” is the bottom device’s gate. Fig. 3.12(a) shows the SET current measured from the source electrode of

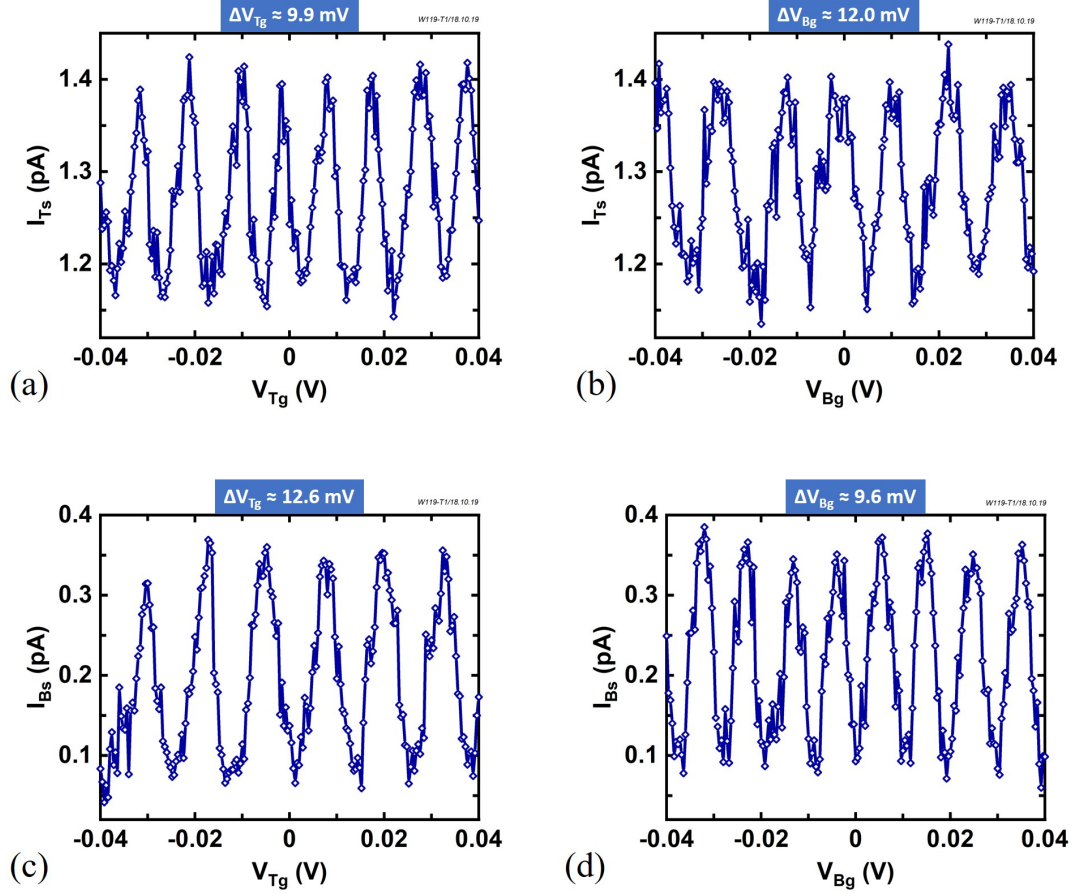


Figure 3.12: Crosstalk of mirror configured in-line SETs as shown in Fig. 3.10(a). (a) CBO of the top island controlled by the top gate. (b) CBO of the top island controlled by the bottom gate. (c) CBO of the bottom island controlled by the top gate. (d) CBO of the bottom island controlled by the bottom gate.

the top device (I_{Ts}) by sweeping the top gate voltage (V_{Tg}), which is the CBO of the top island controlled by the top gate. Similarly, Fig. 3.12(b) is the CBO of the top island controlled by the bottom gate, Fig. 3.12(c) is the CBO of the bottom island controlled by the bottom gate, and Fig. 3.12(d) is the CBO of the bottom island controlled by the top gate. From the extracted gate-island capacitance values shown in Table 3.1, the coupling between the gate of one channel and the island of the other channel is only $\approx 25\%$ smaller than the coupling between the gate and the island of one channel. These capacitance values need to be taken into consideration for designing charge sensing devices, which will be discussed in Chapter 6 where we use these Al/AlO_x/Al SETs as charge sensors.

Device	t_{meas} (d)	jumps	ΔQ_0 (e)
W119-C1	7.6	1	0.13 ± 0.011
W119-C3	7.6	1	0.30 ± 0.014
W119-T1-2	3.9	2 ^a	0.68 ± 0.038
NIST-G (Ref. [53] - FIG. 3)	18.8	$> 100^b$	≥ 1
PTB (Ref. [53] - FIG. 4)	9.0	7 ^c	0.43 ± 0.007
NIST-B (Ref. [53] - FIG. 5)	7.5	$> 50^b$	≥ 1
SOI Si (Ref. [85] - FIG. 7)	7.9	0	0.03 ± 0.003

Table 3.2: Comparison of charge offset stabilities for several Al/AlO_x/Al devices used in this study and available in the literature, with a silicon SOI device as a high quality benchmark in the last row. Footnotes: a – Non-contiguous measurements with multi-hour breaks; b – Main method doesn’t apply and number of jumps is roughly estimated by times of Q_0 change > 0.2 e. c – 5 out of 7 jumps are correlated with liquid helium transfers.

A summary of results from three plasma oxidized Al/AlO_x/Al devices fabricated in this work, three thermally oxidized Al/AlO_x/Al devices presented in Ref. [53], and the best known ΔQ_0 result from an all-silicon device with no metals published in Ref. [85], which is thought to have less TLS defects than devices con-

taining AlO_x , are shown in Table 3.2. The measurement duration ‘ t_{meas} ’, ‘jumps’ and ΔQ_0 from the longest single cooldown of each device are calculated and compared. t_{meas} is the total span of charge offset drift data, which includes break in some cases, a ‘jump’ occurs when the 100 pt running standard deviation increases by a factor of three, ‘ ΔQ_0 ’ is defined as the full range of the Q_0 values measured. The uncertainty of ΔQ_0 in each device (not relevant on the two devices drifting more than 1 e) is defined as the standard deviation of 100 data points in one stable range, which indicates the measurement stability. For devices fabricated in this work, W119-C3 has the same device geometry as W119-C1, while W119-T1-2 has an alternative “in-line” geometry, as shown in Figs. 3.4(a) and 3.10(a) respectively, but all of them exhibit extended periods (> 1.5 days) without jumps. Note that the charge offset drift measurements of W119-T1-2 were often interrupted and stressed by other measurements as discussed above. This device correspondingly exhibits jumps after measurement breaks and larger ΔQ_0 uncertainty, but the charge offset stability in each continuous interval remains stable. As summarized in Table 3.2, all our plasma oxidized Al/ AlO_x /Al devices are much more stable than the historic thermally oxidized ‘NIST-G’ and ‘NIST-B’ devices in Ref. [53], while they are comparable to the ‘PTB’ device, which is thought to be the best metallic Al/ AlO_x /Al device in Ref. [53]. The nonmetallic, silicon SOI (silicon-on-insulator) device from Ref. [85] is included for reference as one of the best results from an extended charge offset stability measurement. We systematically find our metallic devices are much more stable, with no evidence in any measurements of the gross, erratic charge offset seen in the historic metallic devices. Considering the relatively large systematic

measurement noise seen here, the charge offset stabilities in these devices might be even better than shown in Table 3.2. For some applications, the best devices studied here approach the stabilities seen in silicon devices, improving the prospects for implementing metallic SETs with simpler fabrication requirements than silicon SETs.

3.3.4 Temperature Dependence Measurement

Finally, we use the temperature dependence of the current lineshape to determine the total capacitance C_Σ and charging energy E_C for two devices in comparison with the design values. The absence of strong Coulomb blockade in these devices, as shown in Figs. 3.6(a) and 3.8(a), prevents estimation of C_Σ and E_C using a Coulomb diamond measurement, as illustrated in Fig. 1.3(c). As mentioned earlier, strong Coulomb blockade behavior can only be observed when $k_B T_e \ll E_C$. As the bath temperature increases, the source/drain reservoirs broaden and the single electron conductance peaks will be thermally broadened [99]. An individual current peak in the classical regime where metallic quantum dot fits [95] is described as [35, 99, 100]:

$$I \approx \frac{1}{2} I_\infty \cdot \cosh^{-2} \left[\frac{\alpha e (V_g - V_c)}{2.5 k_B T_e} \right] \quad (3.3)$$

where $I_\infty = V_d / R_\infty$ is the reference current characterized by the bias voltage, R_∞ is the device resistance outside of blockade ($V_d \gg E_C / e$), and $\alpha = C_g / C_\Sigma$ is the lever arm. Therefore, as the bath temperature (T) increases from the base temperature (≈ 10 mK), the current peaks spaced by ΔV_g thermally broaden and eventually

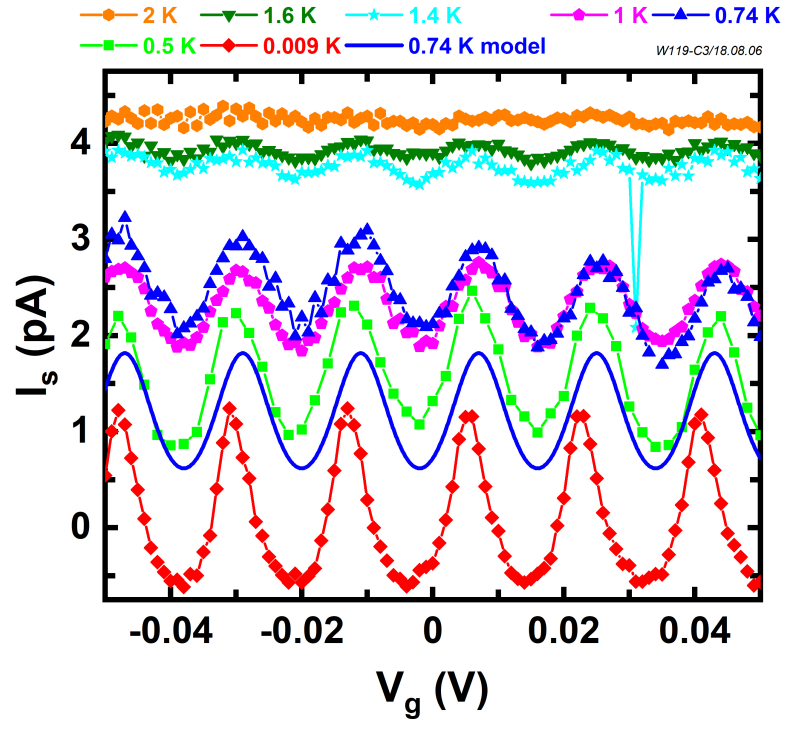
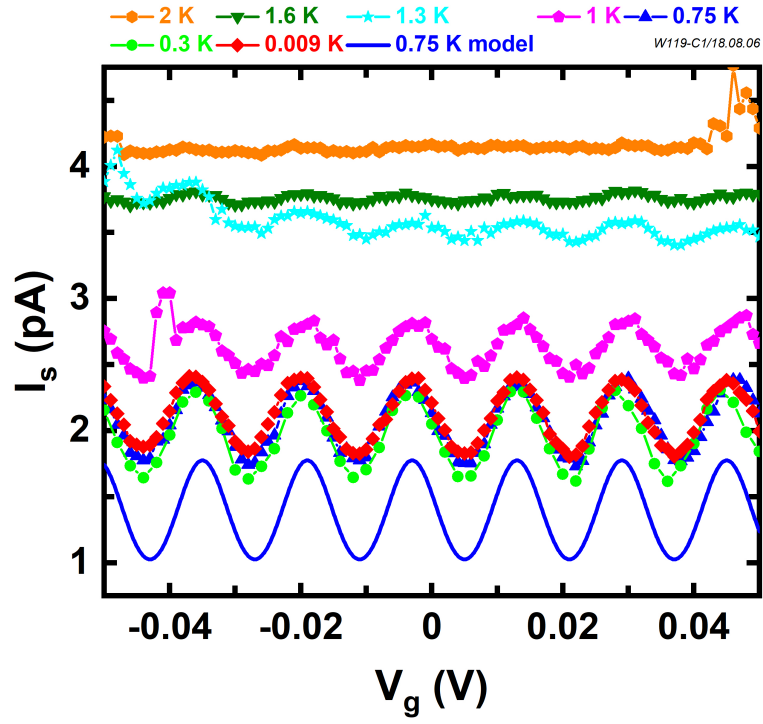


Figure 3.13: (a) CBO on the Al/AlO_x/Al SET (W119-C1) at varying temperatures. (b) CBO on the Al/AlO_x/Al SET (W119-C3) at varying temperatures.

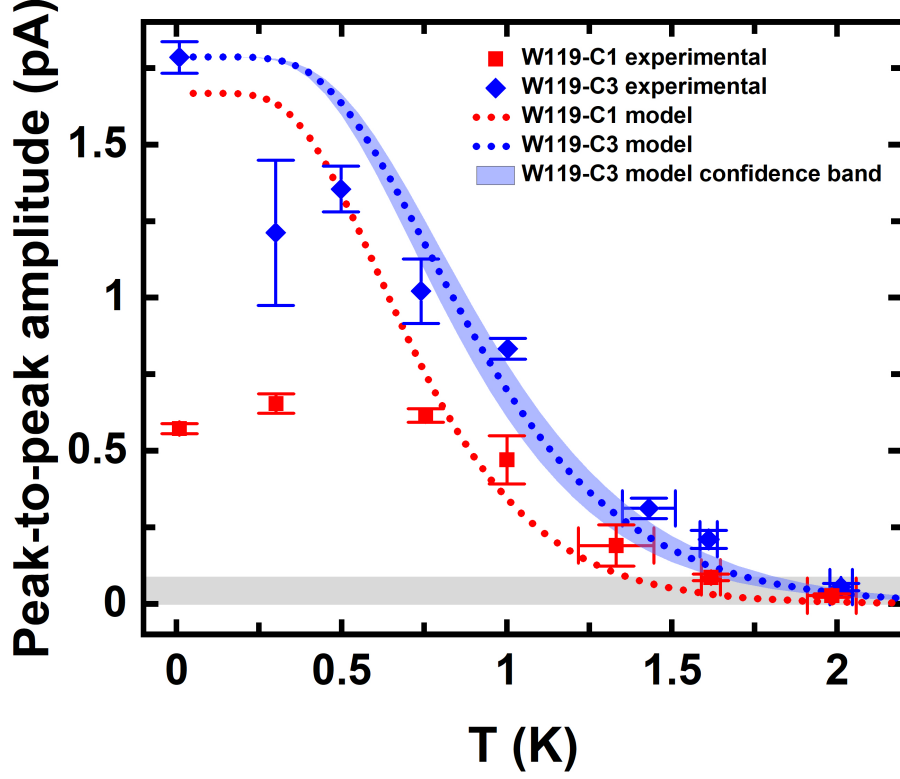


Figure 3.14: The symbols show CBO peak-to-peak amplitudes extracted from the oscillations in Fig. 3.13(a) and (b) vs temperature. Red squares (blue diamonds) are extracted from W119-C1 in Fig. 3.13(a) (W119-C3 in Fig. 3.13(b)). The horizontal error bars represent temperature fluctuations within ± 3 min of the log time. Temperature errors < 20 mK are not shown. The red (blue) dotted line represents the peak-to-peak trend from the model when $E_C/k_B = 4.5$ K (5.6 K) for $R_\infty = 150$ M Ω (140 M Ω). The blue shaded region shows the model variation when C_Σ varies such that E_C/k_B varies over a range of ± 0.3 K, centered around the best-fit value. The gray shaded region at the bottom indicates the measurement noise.

blend together. Experimentally, the CBO is typically only visible when $k_B T_e < 0.3 E_C$ [35]. Fig. 3.13(a) and (b) show CBO sweeps as a function of the temperature from W119-C1 and W119-C3, respectively. As expected, the oscillations die down with increasing temperature and vanish at temperatures above > 1.3 K for W119-C1 and > 1.6 K for W119-C3, when the oscillation is lost in the noise – gray shaded region in Fig. 3.14. The blue solid lines in Fig. 3.13(a) and (b) show the model CBO curves calculated from an array of 25 current peaks (Eq. 3.3) that span $V_g = 0$ spaced by ΔV_g based on the extracted C_g and ΔV_g values as listed above, $T_e = 0.75$ K for W119-C1 and $T_e = 0.74$ K for W119-C3, $R_\infty = (133 \pm 20)$ M Ω for W119-C1 and $R_\infty = (145 \pm 20)$ M Ω for W119-C3 (taken from separate I_s vs V_d measurements) and C_Σ adjusted to match the temperature dependence below. Note that it is important to include sufficient number of peaks outside the window to capture tails of peaks. The peak-to-peak amplitude of the CBO vs temperature is shown in Fig. 3.14 where the red squares (blue diamonds) are from W119-C1 (W119-C3) in Fig. 3.13(a) (Fig. 3.13(b)). The two data points near 2 K are found by fitting a sine function to the CBO to suppress noise and the fitting errors are represented by the vertical error bars. All other data points are peak-to-peak amplitudes found by the average of adjacent peak-to-valley values from the CBO and the vertical error bars represent the standard deviation of all peak-to-valley values at that temperature. The horizontal error bars represent temperature fluctuations within ± 3 min of the log time. Temperature errors < 20 mK are not shown. The red (blue) dotted line shows the peak-to-peak amplitudes taken from model curves like that shown in Fig. 3.13(a) and (b), where $C_\Sigma = 410$ aF (329 aF), i.e., $E_C/k_B = 4.5$ K (5.6 K),

for $R_\infty = 150 \text{ M}\Omega$ (140 M Ω), is adjusted to best capture the experimental trend while using all other experimentally determined quantities. The blue shaded region around the blue dotted line shows the peak-to-peak amplitude range for W119-C3 corresponding to E_C/k_B varying over a range of $\pm 0.3 \text{ K}$, centered around the best-fit value. The experimental values and the model values agree well at temperatures $\geq 0.75 \text{ K}$. The discrepancy at temperatures below 0.75 K implies that the electron temperature for W119-C1 is (0.5 – 0.75) K. The gray shaded region at the bottom indicates the limit given by the current noise. The oscillations are not visible when the temperature is $> 1.3 \text{ K}$ (1.6 K), which also agrees with Ref. [35] that oscillations are not visible when $k_B T \geq 0.3 E_C$. The good agreements between the lines and the data allow us to constrain the uncertainty of E_C/k_B to within about $\pm 0.3 \text{ K}$ and the best-fit E_C/k_B values agree well with the design values for these devices given above – $E_C/k_B = (3.9 \pm 1.1) \text{ K}$. Taken as a whole, these measurements allow us to obtain the devices’ charging energy and indicate the devices were realized as designed and are functioning in the single electron regime consistent with the accepted theory.

3.4 Discussion and Summary

We now discuss the microscopics that can explain the improved charge offset stability. The charge offset drift is thought to be caused by a broad distribution of electrically active defects associated with amorphous AlO_x tunnel barriers or gate dielectrics fabricated by conventional thermal oxidation [36, 84, 101]. Among these defects, TLSs originating from the initial nonequilibrium structure of amorphous

AlO_x [102] are quite common, which is also the predominant decoherence source in superconducting qubits [59]. The exact location of the TLSs in the device that adversely affects the charge offset noise remains uncertain, specifically on whether they reside in the tunnel barriers, in the substrate material, or both [103, 104, 105]. Additionally, in a recent paper [98] and unpublished data (private communication with M. D. Stewart, Jr. research group), ΔQ_0 reductions were observed by adding a poly-Si top gate on bulk silicon SETs and replacing bulk Si with SOI substrate in SETs using AlO_x/Al metal gates. These results imply that the AlO_x instability is not the only factor affecting the magnitude of the charge noise, but that deliberate device design, e.g., using SOI substrate instead of bulk Si, can also mitigate defect interactions with quantum dots.

Devices fabricated in the present work did not utilize any geometries such as adding top gate layer that expected to mitigate charge offset drift. Therefore, we attribute the significant reduction of charge offset drift to i) the better initial oxide quality achieved in the tunnel barrier using plasma oxidation, and ii) the complete processing within a UHV environment. Firstly, previous studies [62, 63, 92] have shown that in plasma oxidation, the Al layer can incorporate much more oxygen in a much shorter time and the measured O/Al ratio is much closer to stoichiometric Al₂O₃ than in conventional thermal oxidation. In plasma oxidation, the neutrally charged, low energy O^{*} free radicals are the dominant reactive species that accelerate the oxidation process [62], and our plasma is tuned to optimize O^{*} production (discussed in Section 2.2). Therefore, a smaller number of unoxidized Al defects are expected in AlO_x tunnel barriers produced by plasma oxidation relative

to those formed by thermal oxidation. We have previously shown reduced long-term resistance drift on AlO_x tunnel barrier devices [89], consistent with this picture. Secondly, UHV conditions for contamination control are well established to reduce impurity concentrations [106] and improve surface smoothness [107] in the thin Al film deposition, as well as limiting uncontrolled oxide formation in the as-deposited Al layer before deliberate oxygen plasma treatment and reducing structural defects in the tunnel barriers. In a recent paper [108], improved charge offset stability is also observed in metallic Fe SETs, which are also fabricated in UHV environment. We propose that plasma oxidation is more likely to be the dominant underlying cause for the significant ΔQ_0 reduction, but either mechanism could be significant.

We also implemented plasma oxidized AlO_x tunnel barriers in SETs fabricated from other materials and measure their long-term charge offset drift. Fig. 3.15 shows the charge offset drift measurement from a $\text{Co}/\text{AlO}_x/\text{Co}$ SET (W118-I4) having the same device geometry but different layer structures as the $\text{Al}/\text{AlO}_x/\text{Al}$ SET shown in Fig. 3.4(a). For the $\text{Co}/\text{AlO}_x/\text{Co}$ SETs, the bottom layer consists of 20 nm Co and 1.1 nm Al that is fully plasma oxidized as the tunnel barrier (expected AlO_x thickness of ≈ 1.3 nm [89]), and the top layer consists of 10 nm Co, 20 nm Cu and 10 nm Au. Qualitatively, we see improvements in the charge offset drift compared to the historical thermal oxide data shown in Table 3.2, but it is not as dramatic as in these aluminum only devices. The process optimization and data are far less complete for these devices. Compared to the $\text{Al}/\text{AlO}_x/\text{Al}$ devices with the same geometry, this device exhibits a larger oscillation period ($\Delta V_g = 22.81 \text{ mV} \pm 0.08 \text{ mV}$) which indicates weaker gate coupling ($C_g \approx 7 \text{ aF}$).

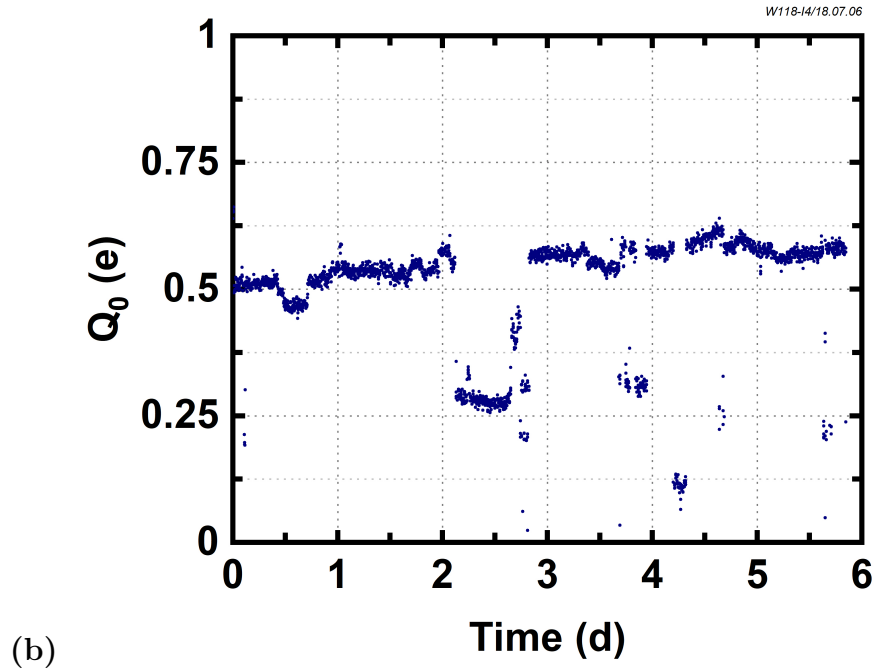
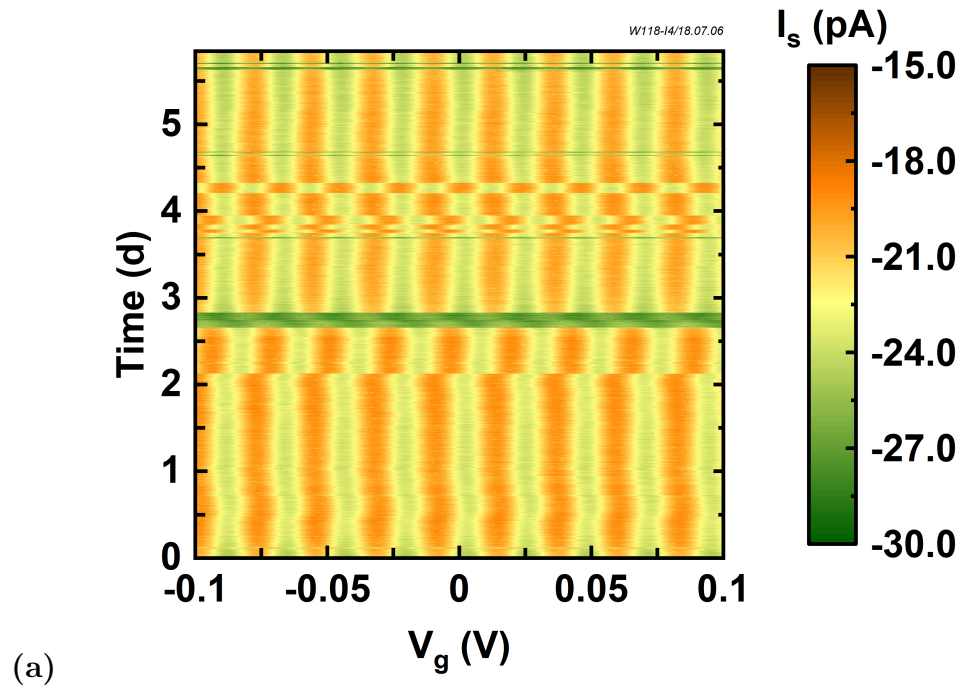


Figure 3.15: Plasma oxidized AlO_x tunnel barriers implemented in $\text{Co}/\text{AlO}_x/\text{Co}$ SETs. (a) Long-term repeating CBO taken over ≈ 5.5 days as a function of time. (b) Extracted charge offset, Q_0 , as a function of time.

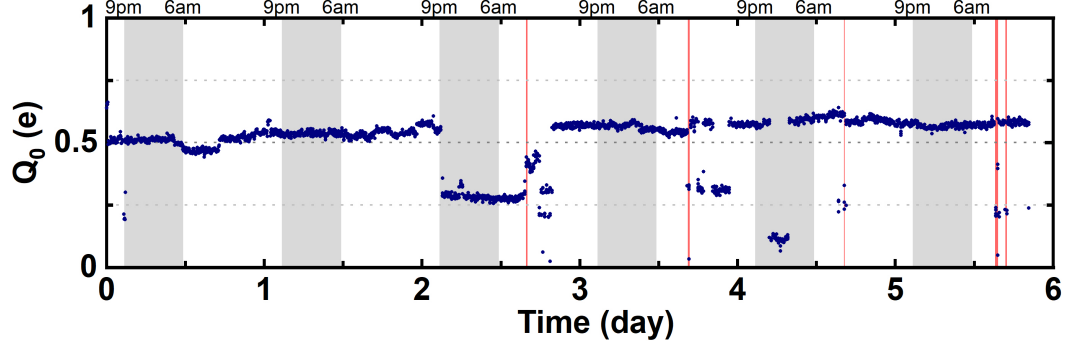


Figure 3.16: Possible correlation between $Q_0(t)$ data of Co/AlO_x/Co SET and the external disruptions. The grey shaded regions denote the night time during the measurement. The red shaded regions denote the time duration when people enter the lab for liquid nitrogen transfer, instrument checks, etc.

There are more jumps over the measurement course than above, but are also long periods where the phase is stable and shows very small linear drift ($0.013 \text{ e/d} \pm 0.0002 \text{ e/d}$). The total charge offset drift extracted using Sine method is, $\Delta Q_0 = (0.64 \pm 0.007) \text{ e}$. In Fig. 3.16, we show the possible correlation between the $Q_0(t)$ data and the external disruptions. The grey shaded regions in the background denote the night time during the measurement when the external environment outside the lab should be the quietest. The red shaded regions denote the time duration when people entered the lab for liquid nitrogen transfer, instrument checks, etc. It can be seen that the $Q_0(t)$ data is much more stable in the night time and that these abrupt jumps mostly happen in the daytime and have some correlation with the external disruptions. Also, the $Q_0(t)$ tends to go back to its previous track after these disruptions. Therefore, we may deduce that Co/AlO_x/Co devices are more susceptible to the external events than Al/AlO_x/Al devices. Very little charge offset drift data on Co/AlO_x/Co SETs is present in the literature, but the $Q_0(t)$

shown here is still much better than the previous thermal oxidized Al/AlO_x/Al SETs [36, 53, 84, 93].

Finally, the stability of these devices suggests an opportunity to evaluate Al/AlO_x/Al SETs as charge sensors for MOS (metal-oxide-semiconductor) quantum dot based charge qubits or spin-to-charge conversion in spin qubits. In this application, an abrupt change in I_s , corresponding to a 1 e change on a capacitively-coupled qubit, is used to detect a change in qubit charge configuration. The qubit is typically configured such that a charge transition corresponds to a projective readout of the qubit. However, operationally, the charge sensor is often operated in a constant feedback mode, where instead of change in current, an abrupt change in the gate voltage (charge offset) needed to maintain a constant charge sensor current indicates a charge transition. In order to hypothetically consider device W119-C1 as a charge sensor, we set the criterion that the change in the control voltage (charge offset) due to a charge transition must exceed 5 SD (99.97 % readout confidence) of the noise for a period long compared to a measurement. For device W119-C1, a SD of Q_0 over a 10-hour period is 0.011 e (also the uncertainty in Table 3.2), corresponding to a SD in gate voltage ≈ 0.18 mV ($\Delta V_g \approx 16$ mV). Therefore, as long as $C_c/C_{\Sigma_MOS} > 5SD$ or $C_c/C_{\Sigma_MOS} > 0.055$, where C_c is the coupling capacitance between the MOS quantum dot and the SET charge sensor and C_{Σ_MOS} is the total capacitance of the quantum dot, the induced charge change on the charge sensor can be distinguished from background instability with 99.97 % confidence. For a typical silicon MOS quantum dot, the total capacitance is ≈ 50 aF and requires $C_c > 2.8$ aF, which is quite small compared to typical coupling capacitances (for example

≈ 20 aF in Ref. [109]). Given the long term stability seen in these devices, this hypothetical operation could be expected to persist for periods > 1 week without any retuning events.

In summary, we fabricated novel metallic AlO_x SET devices incorporating plasma oxidized AlO_x tunnel barriers in a UHV system. Much improved charge offset stabilities are observed in these devices in multi-day measurements, in contrary to the large charge offset drift measured from historical metallic devices using typical, thermally oxidized AlO_x tunnel barriers. Numerical results of Q_0 data demonstrate this improvement quantitatively. Two factors combine to suppress the TLS defects in the AlO_x tunnel barriers: i) Plasma oxidation, which is a more efficient oxide process and can provide better initial oxide quality, and ii) the UHV environment, which can drastically reduce contamination in the entire fabrication process and preserve the quality of the formed AlO_x tunnel barriers. Future experiments using thermal oxidation in the UHV environment could separate the impacts of these two possibilities. We speculate that there is some overlap between i) the class of slow defects (time scale: hours or days) that generate slow charge offset drift and ii) the class of faster defects (time scale: microseconds) that lead to decoherence from relaxation or dephasing. For this reason, success in suppressing time instabilities in AlO_x may pave the way to reducing some decoherence sources associated with AlO_x [72, 73] and enabling expanded implementation within quantum computation systems.

Chapter 4: Developing Single Layer MOS Quantum Dots for Diagnostic Qubits

In this chapter, I will be discussing the research work on silicon-based semiconducting metal-oxide-semiconductor (MOS) quantum devices. Semiconductor quantum dots are promising qubit candidates since they can leverage the highly developed semiconductor industry in the past decades. With demonstrations of high-fidelity single and two-qubit gates [110, 111], silicon MOS spin qubits have attracted more and more research interests for being used to encode the quantum information. Here we report on the design, fabrication and characterization of single metal gate layer, metal-oxide-semiconductor (MOS) quantum dot devices robust against dielectric breakdown, which are considered as prototypes for future diagnostic qubits. These devices were developed as a preliminary solution to a longer term goal of a qubit platform for intercomparison between materials or for in-line diagnostics, and to provide a testbed for establishing classical measurements predictive of coherence performance. For this stage, we seek a robust MOS design that is compatible with wafer and chip architectures, that has a reduced process overhead and is sufficiently capable of challenging and advancing our measurement capabilities. In this work, we present our initial batch of silicon MOS devices using a single gate layer, which

have not exhibited any failures with gate voltage excursions > 10 V, but do exhibit the reduced electrostatic control expected of a single gate layer design. We observe quantum dot formation, capacitive charge sensing between channels, and reasonable effective electron temperatures that enable spin qubit studies. The costs and benefits of the trade-off between device performance and fabrication efficiency will be discussed, as well as opportunities for future improvements.

The main results of this chapter is published in Ref. [112]. This chapter is partially reproduced from [112], with the permission of AIP Publishing, Copyright 2021.

4.1 Introduction

Among the candidate qubits for building large-scale quantum computers, silicon-based architectures are attractive because they leverage existing industrial infrastructure with a plausible path to massive scale-up. The spin states of individual electrons trapped in semiconductor quantum dots can encode quantum information with long coherence times [113] due to the weak spin-orbit coupling and possibility to eliminate nuclear spins [114]. To read the spin state, single-shot readout of individual electron spins in semiconductors has been realized with high fidelity by using spin-to-charge conversion followed by charge detection [30, 80, 81, 115]. These capabilities have been demonstrated using silicon-based MOS quantum dots with lithographically defined metal gate electrodes on the surface.

For quantum dots to be used to host qubits, the electrostatic well trapping

individual electrons must be small enough for the size quantization energy to be larger than the thermal energy. Practically, in surface-gated silicon MOS devices, this means defining a system of gates that controls the chemical potentials at length scales much less than 100 nm, preferably closer to 10 nm. Typically, this results in complex, multilayer gate stacks utilizing multiple materials that have large overlap areas separated by very thin dielectrics [31, 58], which provide ample opportunities for failure [116]. Moreover, the process flows for those devices are time consuming and may not be entirely necessary for diagnostic purposes, such as probing the quality of gate materials or material interfaces, optimizing a specific material recipe or process step, etc. However, to be sufficiently useful in this context, we do need to measure coherence time for comparison with potential classical indicator measurements, test different ^{28}Si isotopic enrichment levels, and compare different dielectric materials, etc. Additionally, a process flow that is compatible with chip-scale fabrication is needed to work with our enriched ^{28}Si substrates [117, 118]. Therefore, developing a chip compatible and robust “working” qubit with a relatively simple fabrication process that reduces failure modes and obtains higher device yields is our longer term objective. In these efforts, we take guidance from similarly streamlined MOS quantum dot designs, e.g., single polysilicon gate layer [115, 119, 120] and two-layer metal gate stack with fewer electrodes [121].

In order to achieve robust working qubits, we seek controllable quantum dots that are able to do projective readout. We start from the design of Sherbrooke/Sandia group’s single polysilicon gate layer devices [122], but modify the design to account for local processing strengths and concerns, replace the polysili-

con with elemental metals, and start with a relaxed design rule. In this work, we present a device composed of two mirror configured silicon MOS quantum dot channels defined and gated with a single titanium/palladium (Ti/Pd) metal gate layer. Electron transport measurements are presented in single and double quantum dot configurations, capacitive charge sensing between two channels is shown, and electron temperature assessments are included. The devices are robust against dielectric breakdown – we never experience an electrostatic discharge (ESD) failure on these devices despite a minimum level of protections. Preliminary measurements indicate that these single metal gate layer devices have advanced our initial goals for forming controllable quantum dots and demonstrating charge sensing, which are critical for approaching the longer term goal of qubit development. As an evaluation of the tunnel coupling tuning needed for future qubit control/readout, we present simultaneous temperature dependent measurements on transport and charge sensing to determine the upper bound of effective electron temperature and tunnel couplings.

4.2 Design Rules, Experimental and Modelling

As stated earlier, our main goal is to develop a MOS quantum dot design that has higher device yields, robustness against dielectric breakdown, and the potential to be developed into a “working” qubit for characterizing and optimizing the effects of materials and interfaces on qubit coherence. To begin, we discuss a few design rules/choices made based on literature and prior experience. Generally, MOS qubits achieve the best gate field definition when utilizing the possible thinnest SiO₂ gate

oxide and the narrowest gates to control the size and shape of inversion regions that form the quantum dots. The smallest dots are made utilizing multiple, overlapping metal gates that enable electrostatic control near the 10 nm limit, but often fail due to poor isolation dielectrics between the overlapping gate layers, or broken gate lines where one layer climbs over the edge of another [116]. At the time we initially designed the devices shown here, those failure modes did not have robust solutions, so we first chose to use only one gate layer, thereby using intervening vacuum as the inter-gate isolation. This choice comes at the cost of less direct field control between inversion regions and various gates, as well as larger features in general, but otherwise eliminates all topography in the fine regions and leaves the primary SiO₂ as the only isolation susceptible to failure.

Secondly, we chose an ≈ 30 nm SiO₂ barrier as a compromise between maximizing the direct capacitance of the gate to the region below it while still keeping a thick enough oxide to have mechanical strength during wirebonding. As additional protection, we thickened the gate contact pads to a total thickness > 900 nm. In prior devices we experienced wire bonds breaking through the SiO₂ when using ≈ 100 nm thick bond pads (especially in the case of thin SiO₂) and creating a direct leakage path from the gate metal to the two-dimensional electron gas (2DEG). Systematic experiments carried out using 300 nm, 600 nm and 900 nm metal pad thickness, indicated that > 95 % success rate can be achieved using a total metal stack thickness > 900 nm with ≈ 30 nm thermally grown oxide. Using a thicker field oxide thinned down in the fine region was also considered, but this could reduce the fidelity of the electron-beam (e-beam) lithography and limit scaling the design rule

to much smaller dimensions. Additionally, trench isolation was considered for isolating possible wirebonding breakthroughs from the inversion areas, but a developed trench isolation process was not in place when these devices were being fabricated.

Thirdly, we chose to use Ti/Pd gates and minimize the gate metal thickness of the fine features to make scaling down to smaller design rules more feasible and enable compatibility with multiple gate layers in the future. Therefore, the e-beam lithography must be done first to insure good overlap to the thicker fanout of photolithography. However, some portions of the e-beam metallization must be exposed during photolithography in order to make good electrical contact at the e-beam/photo junction of the wires. If aluminum (Al) is used for the fine structure, these exposed portions are vulnerable to attack from our typically used photore-sist developer (tetramethylammonium hydroxide, TMAH based). Additionally, Al gates are known to form an oxide layer around them, deforming the shape of the electrodes and affecting the SiO_2 underneath them [123]. Therefore, we chose to use Pd which is resistant to TMAH etching and also forms electrodes with smaller grains compared to Al [58, 124]. However, our initial attempts to use Pd alone [125] revealed instances of the metal peeling, and we used Ti/Pd for all the gate leads to insure good adhesion.

For the initial development of this device line, we chose a relaxed design rule that uses relatively large features and spaces between gates. Fig. 4.1 shows a representative device layout of two single gate layer MOS devices designed in mirror configuration, with one inversion gate and three finger gates for each device channel, and one screening gate in between them. Fig. 4.1(a) is a schematic cross section

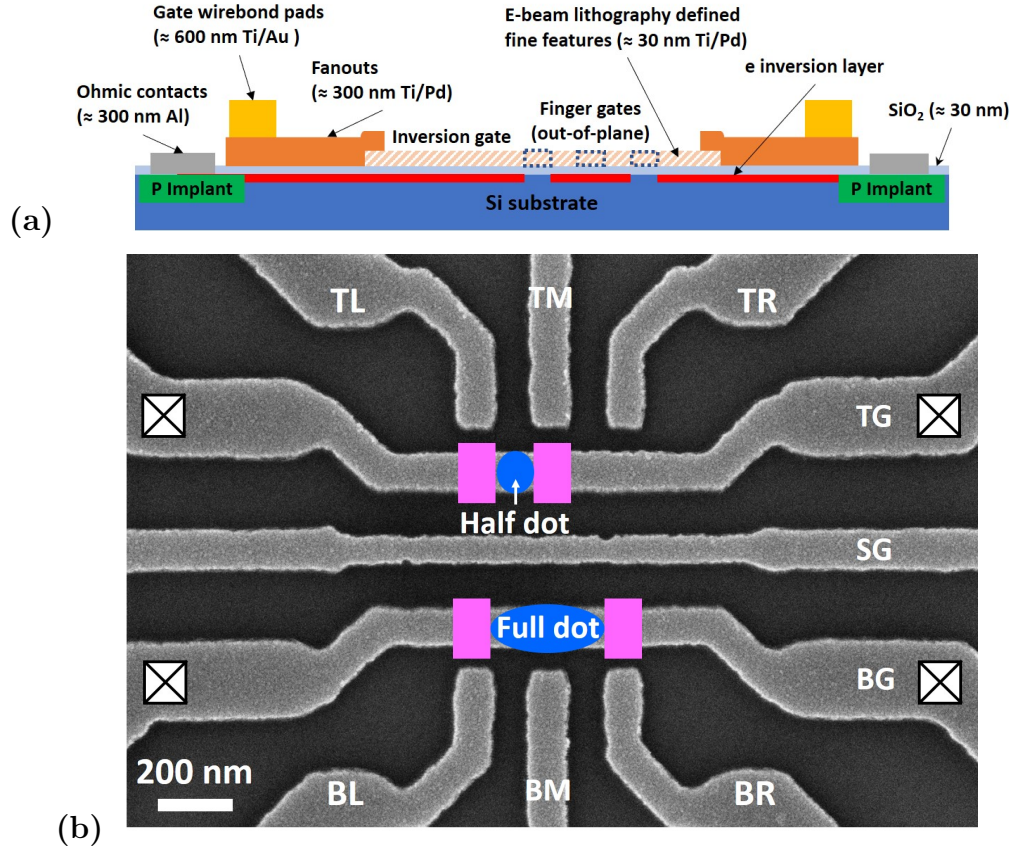


Figure 4.1: (a) A schematic cross section of a device along an inversion gate configured for a “full dot” as shown in the lower channel of (b), which shows the plan view of the device layout used here. An inversion layer is induced at the Si/SiO₂ interface under the TG/BG gates and then electrostatic barriers are set by the two outer finger gates. Crossed boxes represent the ohmic source and drain contacts out of view. The intended configuration for a “half” and “full” dot are schematically marked in blue, and tunnel barriers are denoted by magenta rectangles. The modelled capacitances for these dot configurations are shown in Table 4.1.

of the complete material stack for the whole device. The fabrication process is as follows. We start with a 100 mm intrinsic silicon wafer ($\rho > 1 \times 10^4 \Omega\cdot\text{cm}$) and first use photolithography and deep Si etch to register alignment marks for the alignment of subsequent fabrication steps. After alignment marks are registered on the wafer, the regions of ion implantation are patterned by photolithography and the wafer is then ion implanted (^{31}P , 30 keV, $5 \times 10^{15}/\text{cm}^2$) to define ohmic contacts. Then the wafer is oxidized with a layer of ≈ 30 nm thermal SiO_2 , which is grown at 1000 °C for 21 min as the only dielectric. Next for the device layout, as mentioned previously, the e-beam layer must be done before the optical layer to ensure good contact/overlap between these two layers, since the optical layer is 10 times thicker than the e-beam layer (as shown in Fig. 4.1(a)). The Ti/Pd fine structure is defined first using e-beam lithography (resist: PMMA) and e-beam evaporation (5 nm Ti / 25 nm Pd) with a lift-off process. The macroscopic contact electrodes and fanout are formed using photolithography, e-beam evaporation (5 nm Ti / 300 nm Pd) and a lift-off process. Then the ohmic contacts of source/drain electrodes are made by opening a window in SiO_2 with photolithography and etching over the implanted region, then metallization of 300 nm Al using e-beam evaporation. After these steps, before thickening the gate electrode contact pads, a forming gas (FG, N_2 with 10 % H_2) anneal for 30 min is performed next, which helps to passivate dangling bonds at the Si/ SiO_2 interface, spike Al ohmic contacts, and repair damage in the silicon oxide due to e-beam lithography [124, 126]. Finally, we use photolithography to define windows on the gate contact pads that need to be thickened and deposit another thick metal layer of 50 nm Ti / 550 nm Gold (Au) on these gate contact pads to

avoid breaking through the thin SiO₂ gate isolation layer during wire bonding. In total, four lithographic patterning and subsequent metallization steps are employed to form the whole wafer consisting of > 100 chips with various gate layout designs.

A scanning electron microscope (SEM) image of the device layout used for the data presented here is shown in Fig. 4.1(b). The device has a pair of MOS channels in a mirror image configuration with one inversion gate to induce 2DEG at the Si/SiO₂ interface and turn on the channel, and three finger gates to create barriers and define the quantum dots or for use as plunger gates. As shown in the figure, by using different combinations of finger gates to set tunnel barriers in the device channel, we can tune quantum dots of different sizes. T(B) refer to top (bottom), L/M/R to left/middle/right fingers and G to global inversion gate. Additionally, a screening gate, SG, between the two channels can help confine the quantum dots formed in the two channels. Ohmic contacts of source/drain electrodes are indicated by the crossed boxes, S(D) is source (drain).

To develop an expectation of the relevant capacitances for tuning and comparison with data, COMSOL multiphysics was used to model capacitances of various gates to quantum dots assuming electron accumulation as shown in Fig. 4.1(b) for an intended “half dot” (top channel) and an intended “full dot” (bottom channel). Capacitances for selected gates are shown in Table 4.1. A gate oxide thickness of 33 nm was used based on ellipsometry measurements, a 2DEG thickness of 4 nm was assumed and SiO₂ permittivity [97] of $3.9 \cdot \epsilon_0$ and Si permittivity of $11.7 \cdot \epsilon_0$ were employed. These expected capacitances are compared to the data later for triangulating the experimentally formed quantum dots.

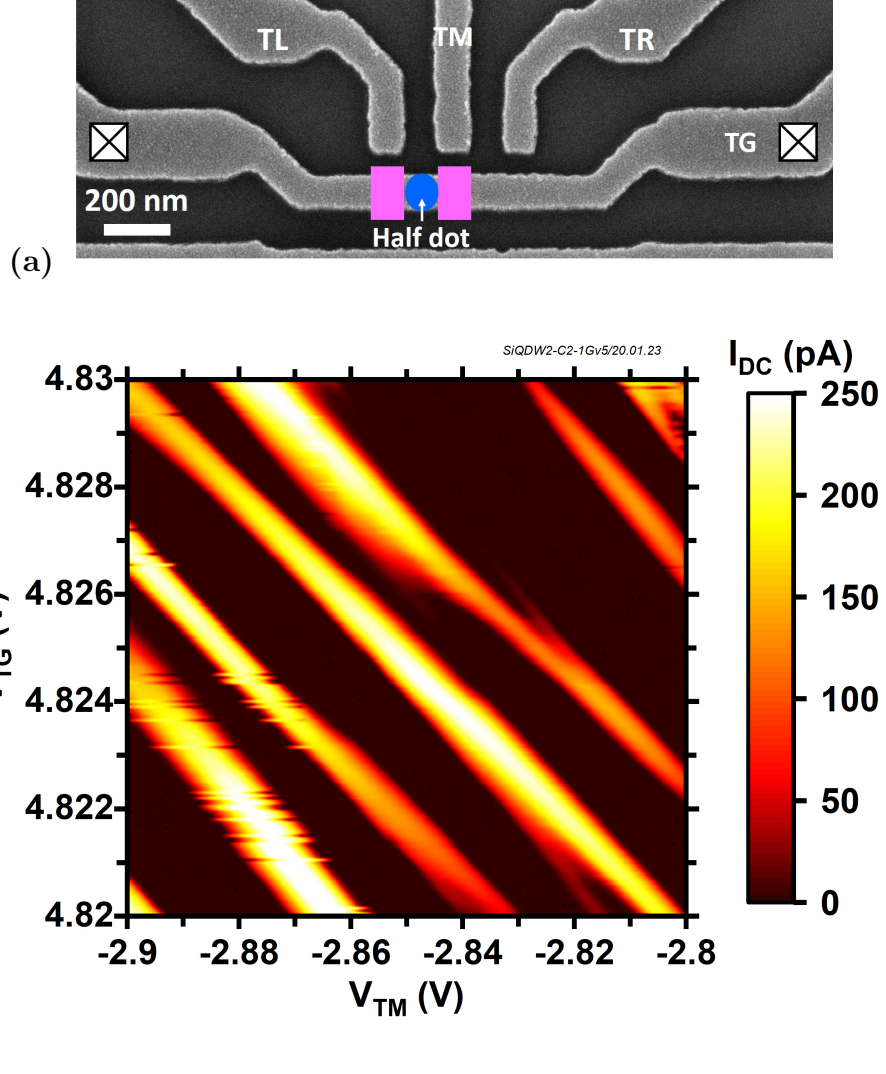
Capacitance (aF)	(T/B)L	(T/B)M	(T/B)R	(T/B)G	SG	Size (nm×nm)
Half dot	4.3	3.5	1.9	26.7	5.4	100 × 100
Full dot	6.4	7.6	6.4	55.7	11.5	300 × 100

Table 4.1: COMSOL modelled capacitance values (aF) between gates and dots, assuming the configurations shown in Fig. 4.1(b). A gate oxide thickness of 33 nm and an inversion layer thickness of 4 nm are used.

4.3 Electrical Measurements of Silicon MOS Quantum Dots

The electrical measurements of the MOS quantum dots shown in this section were conducted in a cryogen-free dilution refrigerator with a base temperature of ≈ 10 mK. Measurements were conducted by transport in a single channel or using one channel to form a dot(s) and the other channel as an SET charge sensor (CS). Bias is applied on the source electrode and the drain electrode is connected to a current preamplifier. For the charge sensing measurements, a feedback loop is applied to the CS plunger gate to maintain a constant current while recording the current and the applied plunger gate voltage.

Our first step to evaluate these single gate layer devices is to form quantum dots by applying negative voltages on the finger gates to induce tunnel barriers in the device channel. Once evidence of Coulomb blockade is observed, the gate voltage periodicity ΔV_g of single electron peaks is used to determine the gate capacitance $C_g = e/\Delta V_g$, and the source-drain bias height V_{SD} of Coulomb diamonds is used to find the total capacitance. Fig. 4.2(b) shows the DC measured charge transitions in the top channel, with the intended half dot configuration shown in Fig. 4.2(a). By sweeping one finger gate (“TM”) and the inversion gate (“TG”), the electrostatic



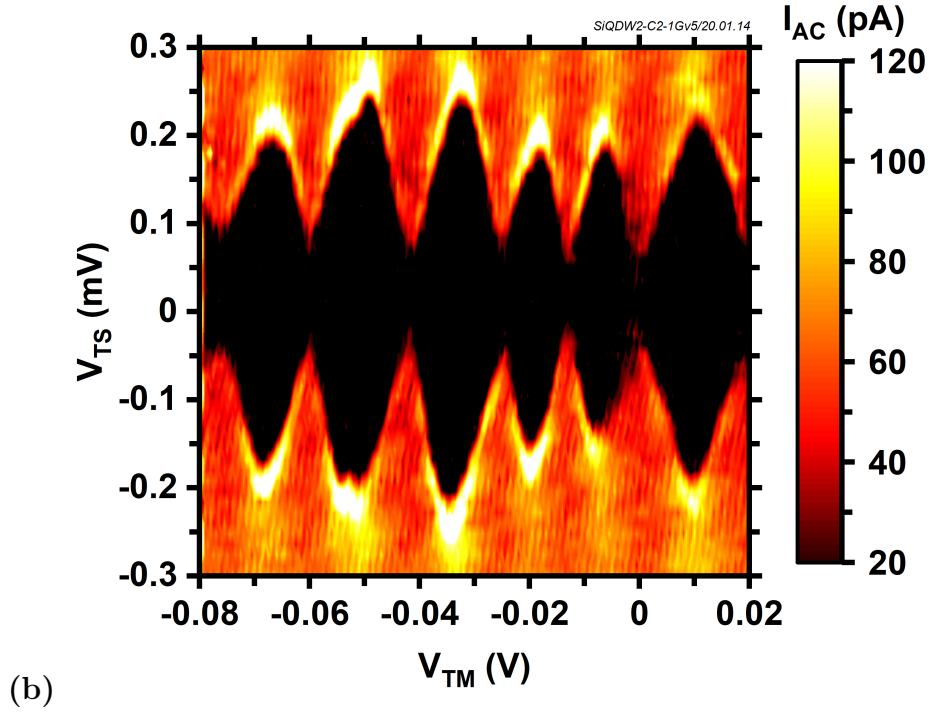
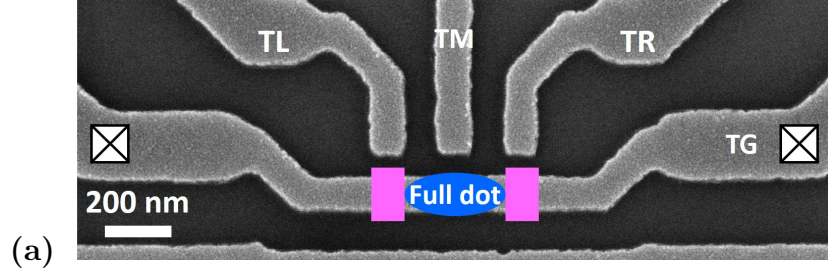


Figure 4.3: (a) Intended device configuration of a full dot in the top channel. (b) Coulomb diamonds measured with the device configured as shown in (a) indicate the formation of a quantum dot. Irregularities in the diamonds indicate that unintended barriers are also present in the channel.

potential of the formed dot is changed and charge transitions are induced along the swept directions. Here “TL” is used as the barrier gate and “TM” is used as both barrier and plunger gates. The observed charge transitions indicate that there is dot formed in the channel. The slopes of these charge transition lines are due to the ratio between the coupling capacitances of the target dot to each sweeping gate. Using the charge transition period along each sweeping gate voltage direction, we calculate the gate capacitance between TM and the dot as $C_{\text{TM}} = e/\Delta V_{\text{TM}} \approx 4.8$ aF, and the gate capacitance between TG and the dot as $C_{\text{TG}} = e/\Delta V_{\text{TG}} \approx 48$ aF, which are reasonable values for a formed dot in the device channel according to the modelling. Compared to the modelled values, C_{TG} is larger than the coupling capacitance between the inversion gate and a half dot but smaller than the coupling capacitance between the inversion gate and a full dot. This indicates that the formed dot size is between the illustrated half dot and full dot. In addition, irregularities in the charge transition periods can be seen. These are probably due to some nonidealities in the device channel. Shown in Fig. 4.3(b) are Coulomb diamonds measured by lock-in from the top channel with barriers applied from the “TL” and “TR” finger gates and the TM finger gate used as a plunger (as shown in Fig. 4.3(a)), and an AC excitation of $20 \mu\text{V}$. The irregularities observed in the diamond pattern indicate that more than one dot feature is contributing in the channel. From the period of the conductance peaks near $V_{\text{SD}} = 0$ V, we calculate the TM plunger gate capacitance to the dot $C_{\text{TM}} = e/\Delta V_{\text{TM}} \approx 8.9$ aF, which is within 20 % compared to the modelled value. From the largest diamond, the charging energy, $E_C = eV_{\text{SD}} = e^2/C_\Sigma$ is ≈ 0.25 meV, indicating a total capacitance $C_\Sigma \approx 640$ aF. This total capacitance is

much larger than the modelled value for a “full dot” configuration, and implies a larger dot than expected. Nonetheless, based on these single gate layer devices, we are able to configure quantum dots and measure electron transport using various gate combinations as barriers and plunger. The gate capacitance is capable to efficiently manipulate the chemical potentials of the formed dots, and the induced charge change can be seen above the noise level with a signal-to-noise ratio (SNR) > 5 , sufficient for charge sensing [81].

In order to use a quantum dot as a qubit, one must have readout sensitive to the projection of a single quantum state. Within MOS, projective quantum readout can be accomplished by configuring the dots so that the charge transition (or absence) in response to a gate excitation constitutes a readout. This requires detection of single electron charge transition on a quantum dot. This can be extended to electron spin readout by breaking the spin-state energy degeneracy (e.g., in a magnetic field) of the basis states so that a charge transition indicates the spin state, i.e., spin-to-charge conversion, and detecting the single transition by charge sensors [30, 80, 81, 115].

The development of single electron charge sensing for readout was a primary goal for the devices presented here and motivated the mirror configuration of two devices, as shown in Fig. 4.1(b). To attempt charge sensing, we tuned a half dot in the top channel (CS) for capacitively sensing changes in the charge configuration of a full dot (target) in the bottom channel, as marked in Fig. 4.1(b). We found the direct capacitance of the bottom gates on the CS required correction to maintain a position of high sensitivity. Therefore, we implemented a constant PI (proportional-integral) feedback loop, where a setpoint current through the top

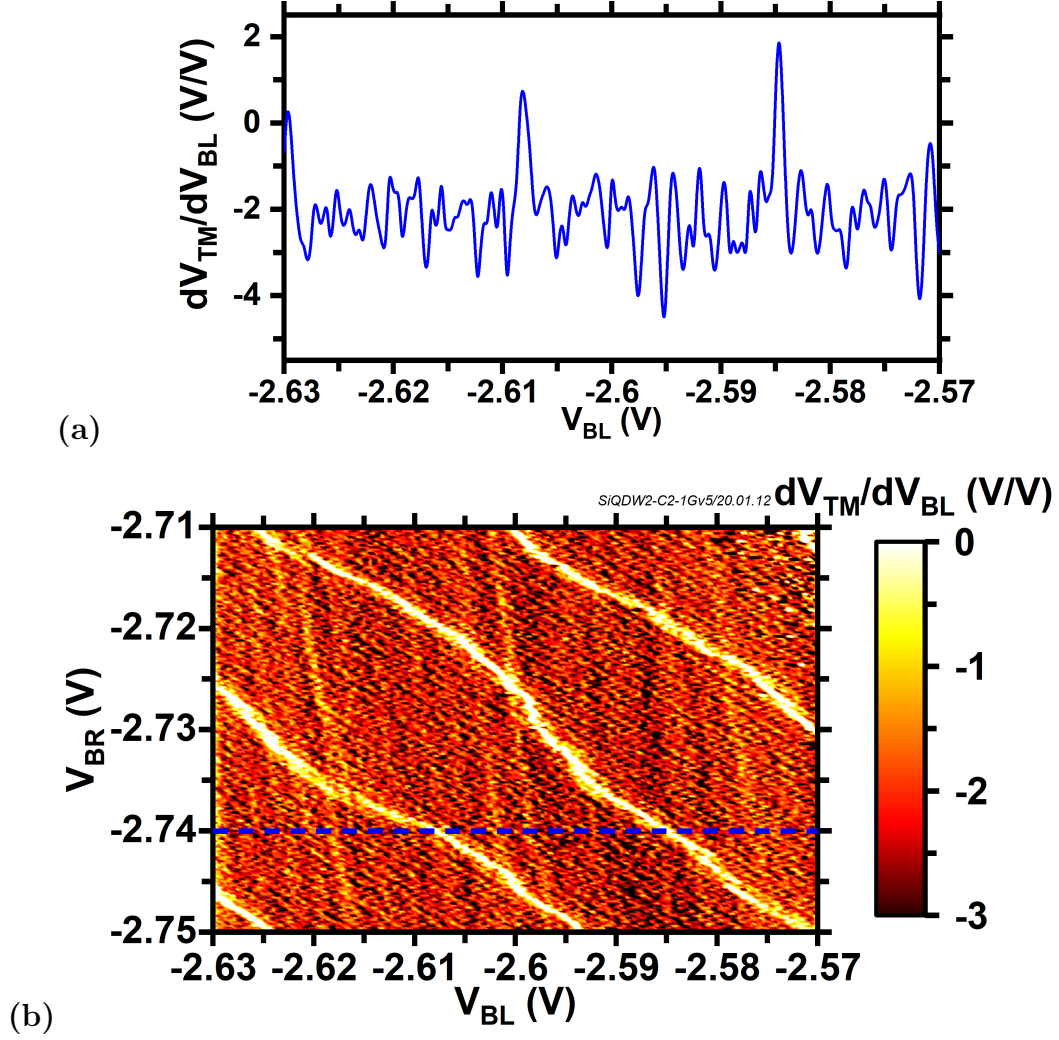


Figure 4.4: Charge sensing data using a top channel half dot and the bottom channel configured as a full dot. (a) Charge sensing signal measured in the SET sensor of a sweep at $V_{BR} = -2.74$ V, taken from the slice marked by the blue dashed line in (b). (b) Charge sensing by configuring the top channel as the SET sensor and the bottom channel as the target dot, as marked in Fig. 4.1(b). According to the slope, the target dot is more coupled to “BR” gate.

SET channel (CS) was maintained by adjusting the CS plunger voltage (V_p) and we recorded both the CS current and the plunger voltage. A charge transition on the target dot causes an abrupt change in the CS current (an error in the feedback), and a subsequent correction by the feedback loop results in an abrupt change in the plunger voltage. The errors in the current and the derivative of the plunger voltage map out the boundaries of the target’s charge stability regions, as seen in Fig. 4.4(b). As the bottom two finger gates are swept, the electrostatic potential of the target dot is changed and charge transitions are induced along both directions $-V_{BL}$ and V_{BR} . The parallel line features shown in Fig. 4.4(b) indicate charge transitions on the target dot induced by changing V_{BL} and V_{BR} . The linecut in Fig. 4.4(a) shows the SNR in that instance of > 5 , which is comparable to signal strengths used for single shot readout [81]. The slopes of these lines are determined by the ratio between the coupling capacitances of the target dot to each barrier gate. From the charge transition period along each gate voltage direction, the gate capacitances in the bottom channel are, $C_{BL} = e/\Delta V_{BL} \approx 6.4$ aF and $C_{BR} = e/\Delta V_{BR} \approx 8$ aF, respectively. The target dot is $\approx 25\%$ more strongly coupled to “BR” gate than to “BL” gate, probably due to some nonideality. Based on the symmetry and similarity to the model values, the target dot is likely between the barriers induced by “BL” and “BR” gates as intended. Additionally, another set of parallel lines are seen in Fig. 4.4(b) with a weaker SNR, indicating an additional unintended dot in the channel. From the period and slope, we estimate the coupling capacitances between this unintended dot and the barrier gates as $C_{BL} \approx 8$ aF and $C_{BR} \approx 1.4$ aF. Therefore, this unintended dot is likely located near the “BL” gate.

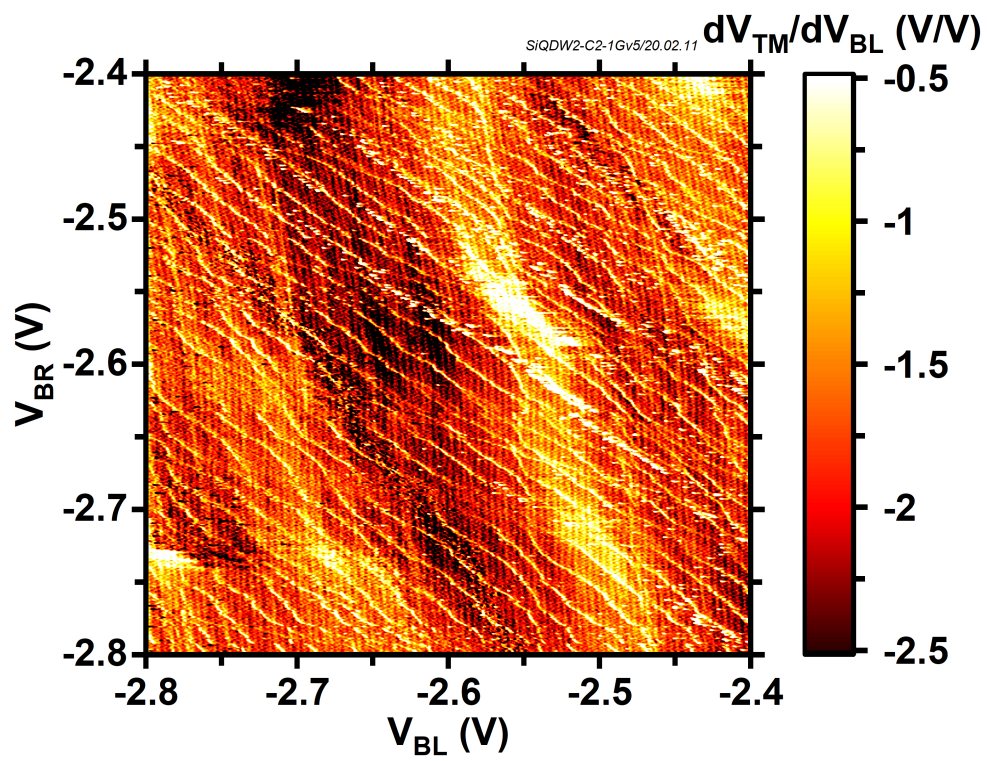
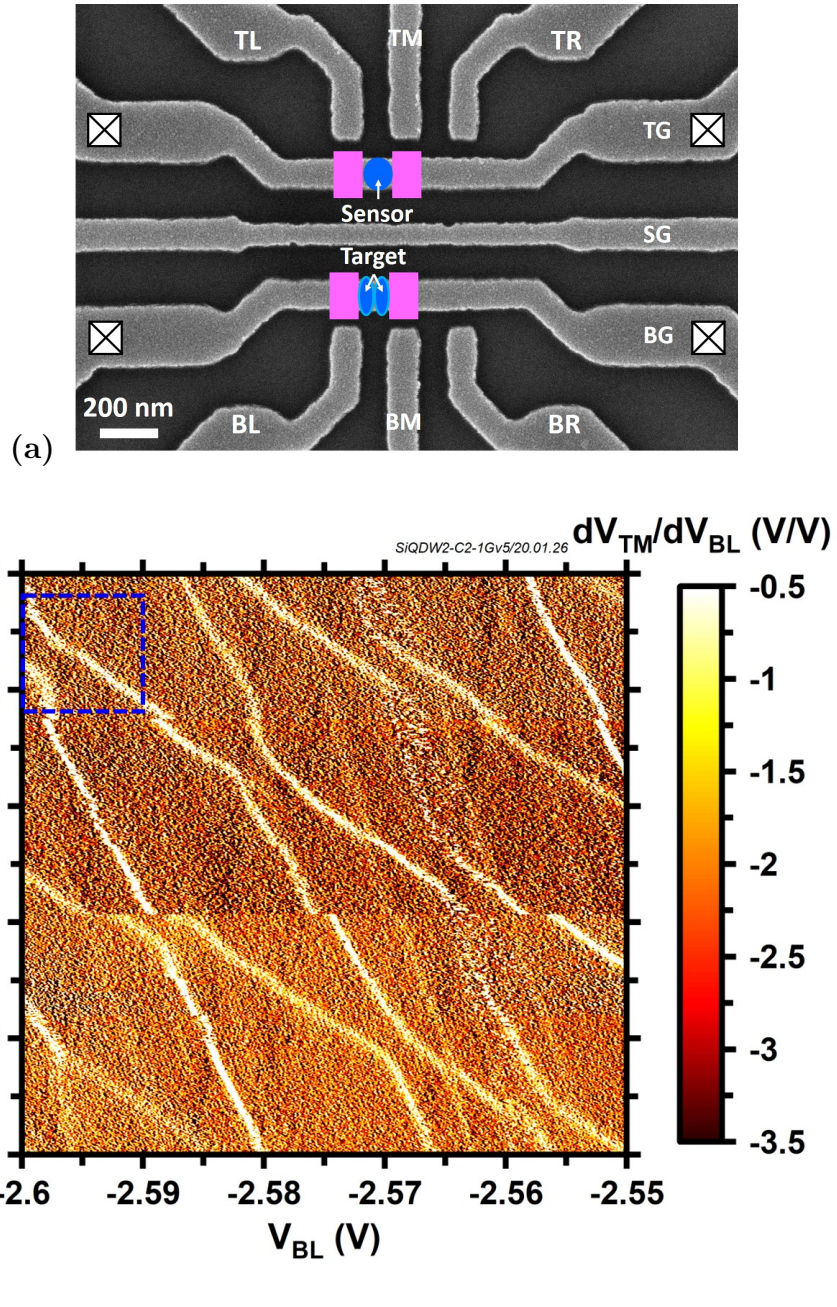


Figure 4.5: Large range charge sensing with the same dot configuration used in Fig. 4.4(b).

Charge sensing allows charge reconfigurations to be detected that might be invisible in transport and enables mapping the charge stability regions over very large gate voltage ranges. Shown in Fig. 4.5 is a charge sensing measurement consisting of ≈ 50 charge transitions sensed by the CS. The dominant feature consists of parallel lines with the same negative slope as the lines in Fig. 4.4(b), likely due to the intended dot confined by “BL” and “BR” gates. Other than the main feature, a fainter array of big bright spots is also seen, that are similarly spaced along V_{BL} and V_{BR} , probably due to some other charge instabilities weakly coupled the CS. Overall, the charge sensing reveals a remarkable amount of details over a wide range.

While an individual quantum dot provides exquisite charge sensitivity, and single-electron charge sensing capability provides a readout mechanism, these alone make realization and control of a qubit very challenging. Forming a tunnel coupled double quantum dot enables the possibility of exchange control and other choices of qubit encoding, e.g., singlet-triplet qubits [127]. Double quantum dots also enable the charge degree of freedom to be employed to form charge qubit [128]. Therefore, our intention with these devices was also to form double dots toward the formation of qubits. Using the robust charge sensing, we found that, as we were sweeping the half dot configuration as shown in Fig. 4.6(a), we would see regions that appeared to correspond to a double dot charge stability pattern. Fig. 4.6(b) shows a “honeycomb” double-dot stability diagram sensed by the SET sensor in the top channel. Two sets of charge transition lines are visible and they correspond to each of the two dots, respectively. According to the slope and period of each set of parallel lines, one dot is more coupled to “BL” gate and the other dot is more coupled to



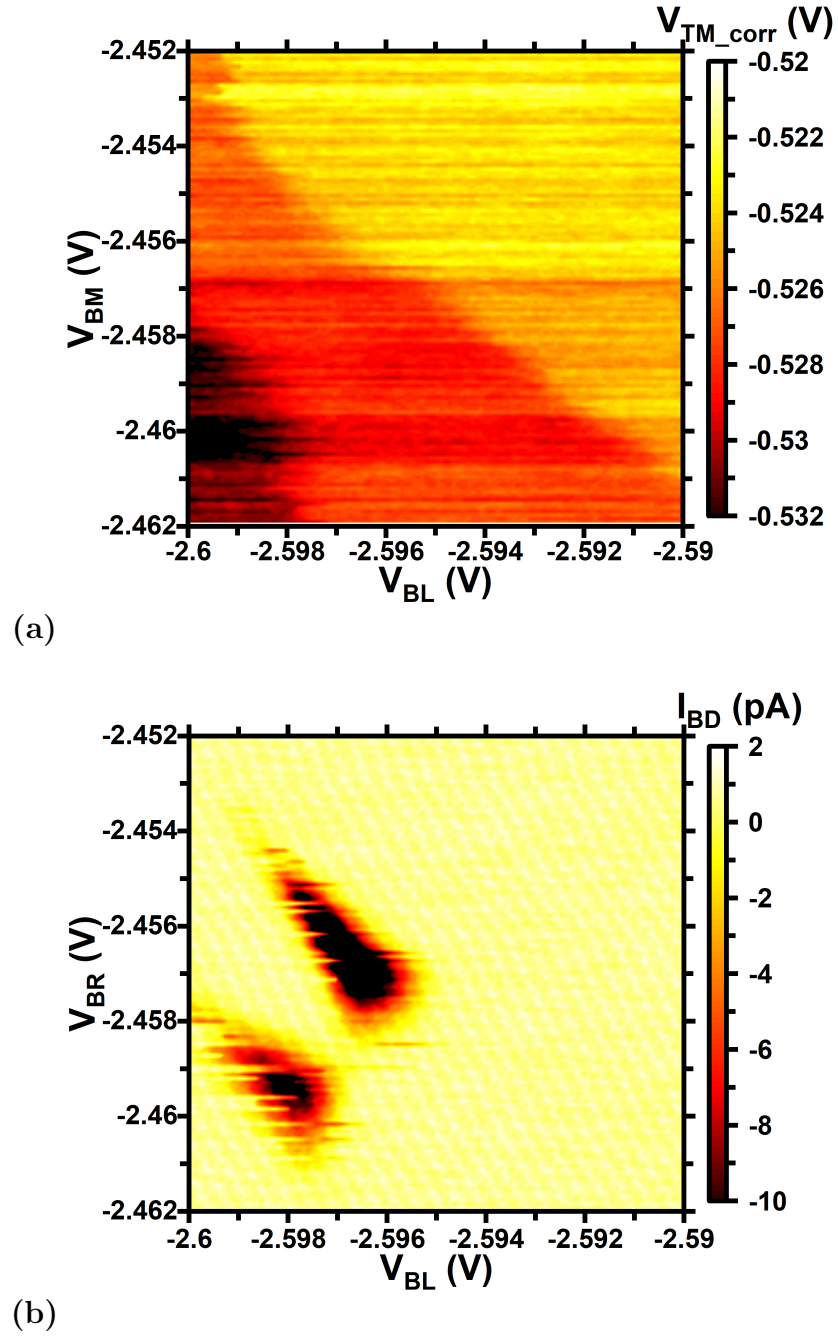


Figure 4.7: (a) Charge sensor feedback control voltage (after correction for direct capacitance) from the blue dashed line boxed region in Fig. 4.6. (b) Bias triangles in the same blue dashed line boxed region.

“BM” gate. We estimate that the capacitances between each dot and the two barrier gates are: $C_{D1-BL} \approx 10.7$ aF, $C_{D1-BM} \approx 5.8$ aF, $C_{D2-BL} \approx 6.4$ aF, $C_{D2-BM} \approx 9.1$ aF, where “D1” and “D2” refer to the two dots, respectively. However, charge transitions from D1 to D2 are not visible, e.g., Fig. 4.7(a) shows the plunger gate voltage after correcting for direct capacitance, and no contrast is visible between $(j+1, k) \Leftrightarrow (j, k+1)$ charge stability regions, where the left and right element inside the parentheses refer to the number of electrons on each dot, respectively. Capacitance triangulation suggests that both dots are probably interior to the barrier gates, likely due to an unintended barrier in that region, so that the capacitive coupling from each dot to the CS is almost equal and the CS is not sensitive to the charge change. To confirm that two coupled dots in series are present, we applied a small V_{SD} on the bottom channel and observed bias triangles at the triple points, shown in Fig. 4.7(b). Therefore, double quantum dots were found in these devices, and hopefully the device versions with smaller gate widths and more finger gates will provide more deliberate electrostatic control.

As stated earlier, another motivation for these devices was to advance our measurement capability toward demonstrating tunable tunnel couplings and qubit control/readout. As a starting point, we examine the effective electron temperature and tunnel couplings implied by the Coulomb blockade linewidth measured by direct transport and also the width of the charge transition sensed capacitively. Firstly, for Coulomb blockade oscillations of an SET, the lineshape of an individual Coulomb

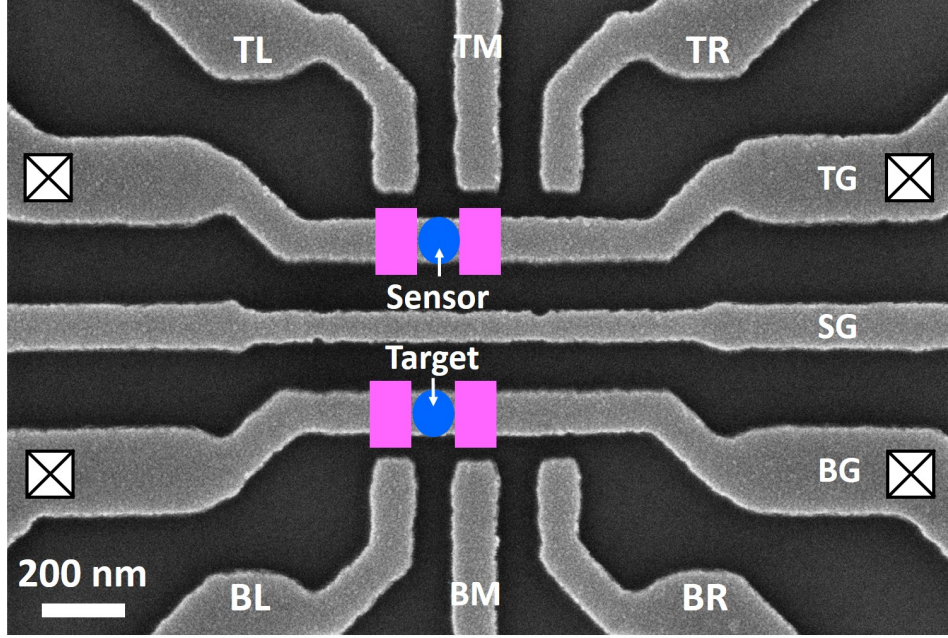


Figure 4.8: Intended device configuration of the temperature dependence measurement.

blockade current peak is given by [35, 99, 129]:

$$I_{\text{SET}} \approx I_A \cosh^{-2} \left[\frac{2 \ln(1 + \sqrt{2})(V_p - V_{c,\text{CB}})}{w_{\text{CB}}} \right] \quad (4.1)$$

where I_{SET} is the SET current, I_A is the peak height, V_p is the swept plunger gate voltage, $V_{c,\text{CB}}$ is the Coulomb peak center position, and w_{CB} is the Coulomb peak width. For this analysis, we consider the temperature dependent broadening plus a small additional width due to tunnel coupling [130], such that $e \cdot \alpha \cdot w_{\text{CB}} = \sqrt{(4.35k_B T_e)^2 + (2h\Gamma_c)^2}$, where α is the lever arm of the plunger gate, k_B is the Boltzmann constant, T_e is the electron temperature, h is the Planck constant, and Γ_c is the tunnel coupling. For each temperature, we measure Coulomb resonances

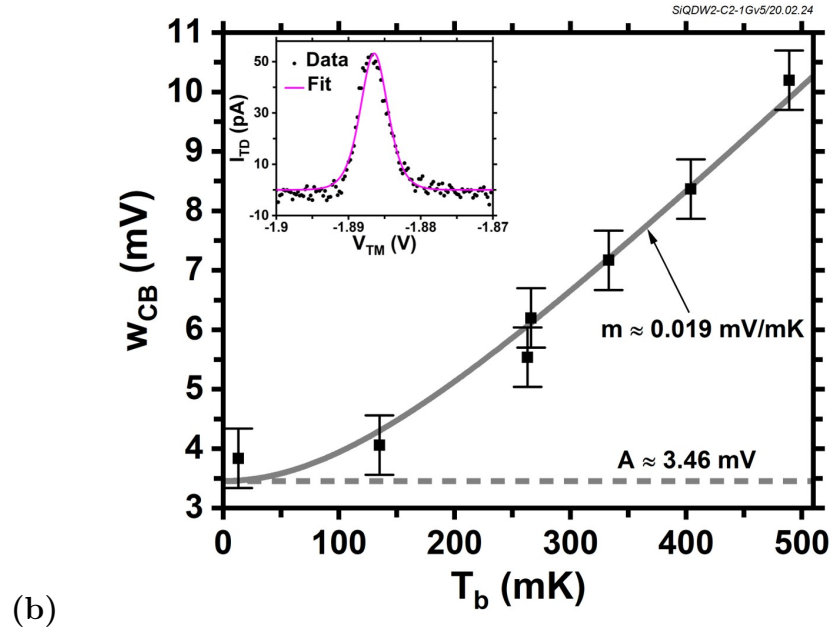
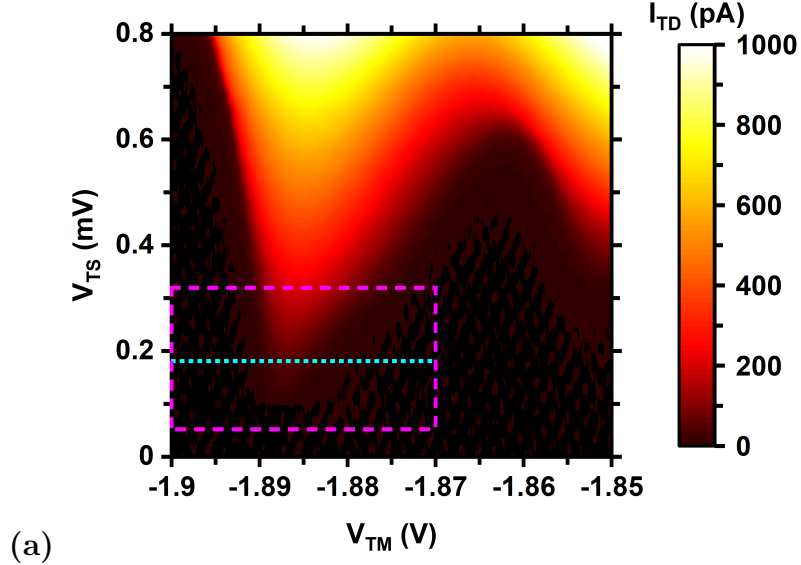


Figure 4.9: (a) Measured Coulomb blockade at base temperature. The data region being fitted to extrapolate the zero-bias linewidth is marked by magenta dotted box. Blue dotted line is the data of the example fit in (b) inset. (b) Temperature dependence of the Coulomb blockade linewidth as shown in the inset. The vertical error bars represent fitting errors. The horizontal error bars represent temperature fluctuations within ± 3 min of the log time. Temperature errors < 10 mK are not shown.

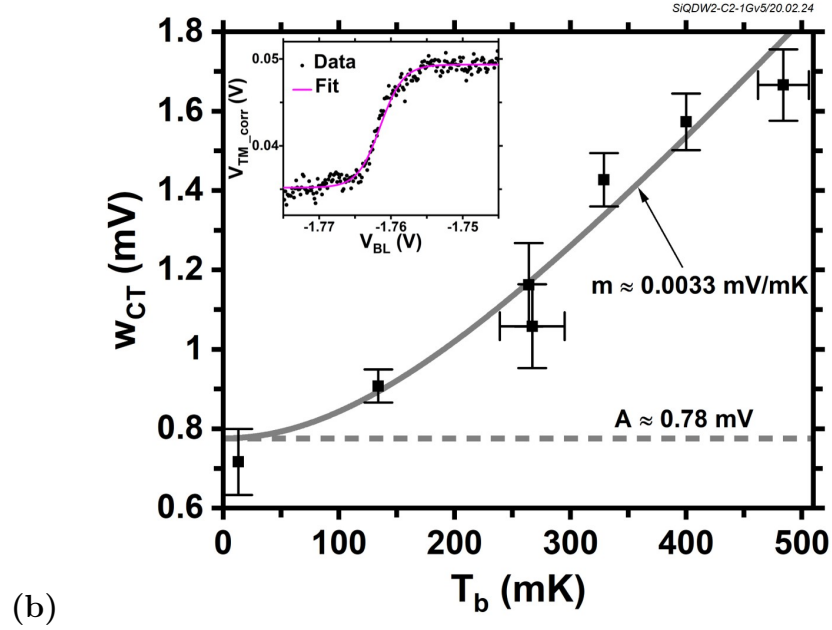
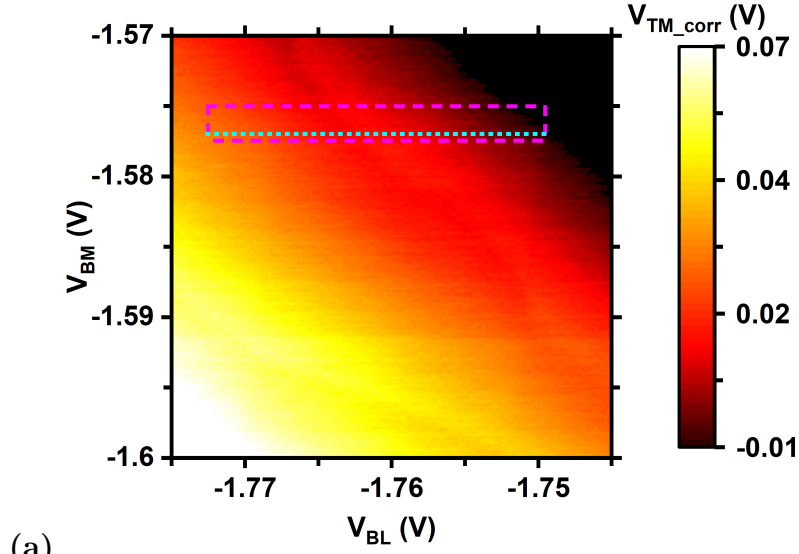


Figure 4.10: (a) Measured charge transitions at base temperature. The data region being fitted to average the charge transition width is marked by magenta dotted box. Blue dotted line is the original data before linear slope correction of the example fit in (b) inset. (b) Temperature dependence of charge transition width measured by charge sensing as shown in the inset. The vertical error bars represent fitting errors. The horizontal error bars represent temperature fluctuations within ± 3 min of the log time. Temperature errors < 10 mK are not shown.

in the zero source-drain bias limit (see Fig. 4.9(a) for an example) and extract w_{CB} using Eq. 4.1 (see Fig. 4.9(b) inset for an example). In Fig. 4.9(b) we show w_{CB} vs. the bath temperature T_b . The peak width increases with temperature when $T_b \gtrsim 180$ mK but saturates at low temperature. The data is fit to $w_{\text{CB}}(T_b) = \sqrt{(mT_b)^2 + A^2}$, giving a linear scaling factor $m \approx 0.019$ mV/mK and $A \approx 3.46$ mV as the effective electron temperature, tunnel coupling, etc. in low temperature regime where $T_e(h\Gamma_c/k_B) > T_b$. Using the fit m value, we can determine the lever arm $\alpha \approx 0.02$, which agrees well with Coulomb diamonds measured with this configuration. We can also determine an upper bound for the effective electron temperature $T_e \approx 182$ mK, or, similarly, an upper bound for the tunnel coupling $\Gamma_c \approx 8.3$ GHz.

Secondly, for the charge transition width measured capacitively, the lineshape of a single charge transition is approximated by the Fermi-Dirac (FD) distribution [130, 131]:

$$V_{\text{corr}} \approx \frac{V_A}{e^{(V_g - V_{c\text{-CT}})/w_{\text{CT}}} + 1} \quad (4.2)$$

where V_{corr} is the voltage (corrected for direct capacitance) applied on the SET plunger gate, V_A is the total voltage change between the two charge states, V_g is the swept gate voltage, $V_{c\text{-CT}}$ is the center of the charge transition and w_{CT} is the charge transition width. At each temperature, we measure the charge transitions using the CS dot (see Fig. 4.10(a) for an example) and the same charge transition is extracted, corrected for the linear slope, and fit using Eq. 4.2 (an example fit after linear slope correction is shown in Fig. 4.10(b) inset). Fig. 4.10(b) shows the extracted w_{CT} values vs. T_b , which have the similar hockey stick shape as

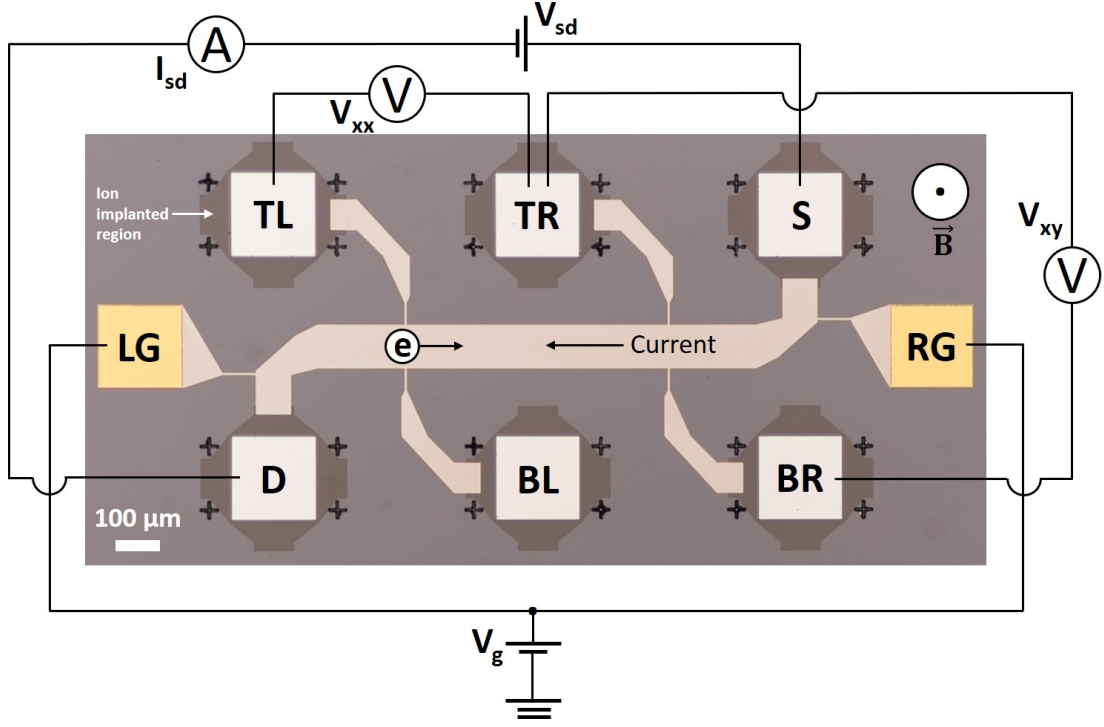


Figure 4.11: Optical image of a typical Hall bar test device and the circuit diagram of the transport measurements.

Fig. 4.9(b). As above, this is fit to extract the linear scaling factor and the temperature independent part. Again, we can determine an upper bound for the effective electron temperature $T_e \approx 234$ mK, or, similarly, an upper bound for the tunnel coupling $\Gamma_c \approx 10.6$ GHz. In both of these cases, the results indicate that our charge sensing noise is sufficiently low to pursue single-shot readout for advancing the future goal of a working qubit.

4.4 Electrical Measurements of Silicon MOS Hall Bar Devices

It is commonly known that the e-beam lithography in the fabrication process of MOS quantum devices creates defects at the Si/SiO₂ interface, which can induce charge traps in the device channel. It has been found that a FG anneal can restore the device's peak mobility after being significantly degraded by e-beam exposure to within a factor of two of the peak mobility before the e-beam exposure. Furthermore, the FG anneal can efficiently remove the shallow defects generated by e-beam exposure, which are within 4 meV below the conduction band edge. [126] Therefore, we employed FG anneal after forming the device fine structure in the fabrication process to repair the damage caused by e-beam lithography. To further assess the oxide interface of these MOS devices, Hall bar test devices were also designed and fabricated on each device die, as shown in Fig. 4.11. Using these MOS Hall bar test devices, we can conduct cryogenic-temperature transport measurements of the electron mobility, which is a commonly used method to evaluate the oxide interface in MOS devices. However, these measurements are indirect measurements of the confined shallow traps. [132] Peak mobility is measured at relatively high electron densities where the 2DEG can effectively screen out the scattering centers [133]. Therefore, for quantum devices operating in the less electron regime, the peak mobility is not a sufficient indicator for quality of the oxide interface [126]. An effective way is to use a percolation transition model [134] to fit the transport measurement data and extract the percolation threshold density. The percolation threshold density is a good indicator of the Si/SiO₂ interface quality.

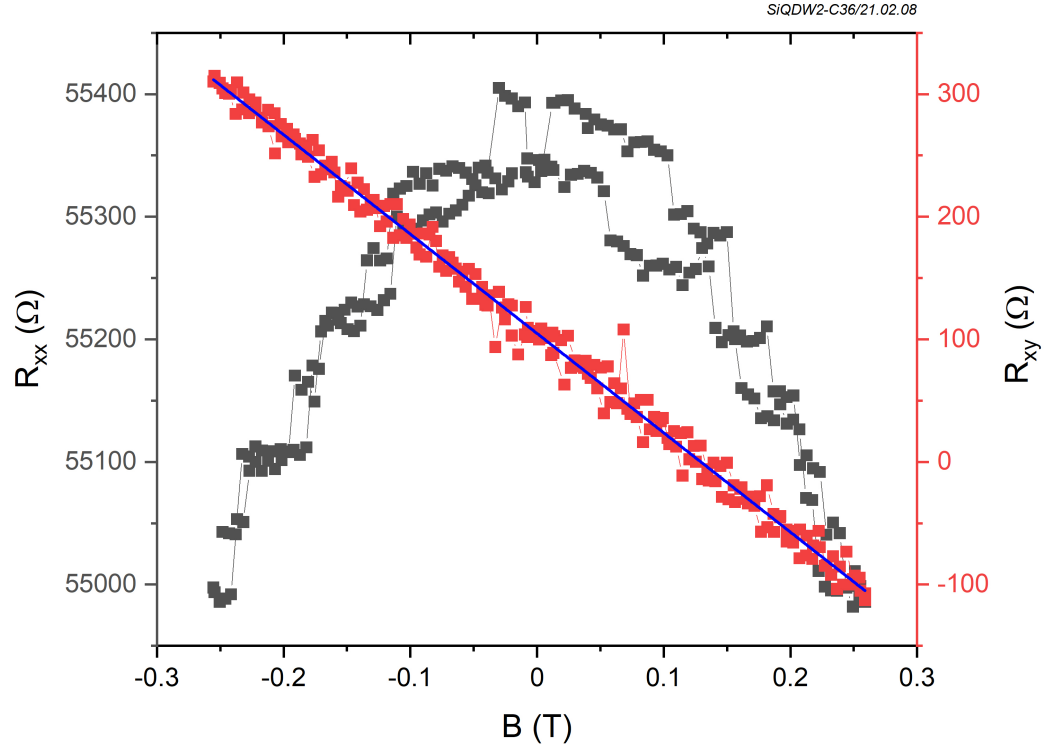
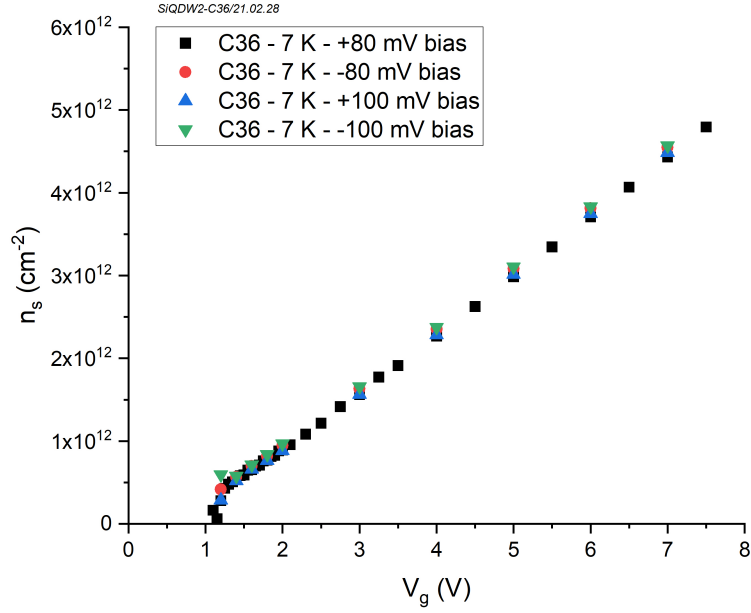


Figure 4.12: An example R_{xx} and R_{xy} vs B Hall measurement data at 7 K, with 1.8 V applied on the gate and the I_{sd} measured with -80 mV voltage source bias. For each measurement, the magnetic field was first swept forwards from negative to positive and then swept backwards from positive to negative to ensure good data reliability. Blue solid line is the linear fit of R_{xy} vs B data.

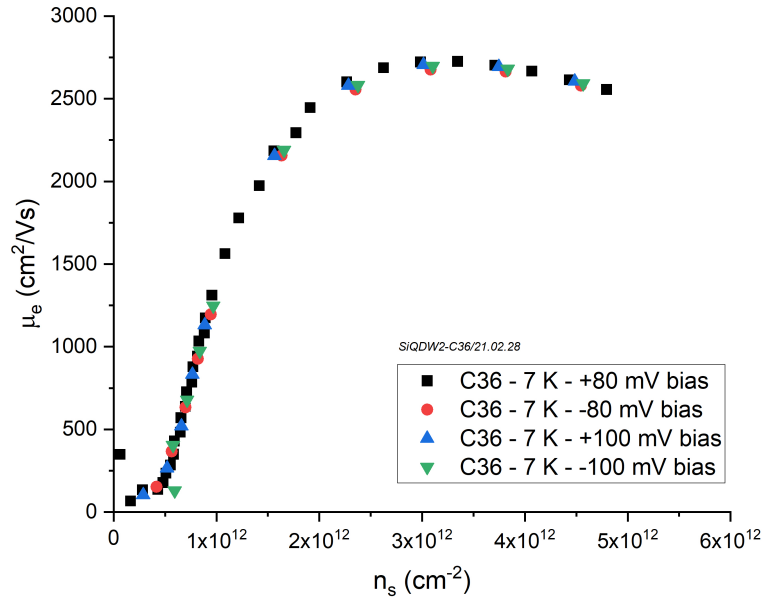
In Fig. 4.11, we show the optical image of a typical Hall bar test device on each device die fabricated in this work and the circuit diagram of the transport measurements. The test devices were fabricated along with the fabrication of the MOS quantum dot devices. The star-like shadow regions under these aluminum ohmic contact pads (in silver color) are the ion implanted regions. The center region of the Hall bar in light gold color was fabricated along with the gate fanout of the MOS quantum dot devices. Similarly, the two gate contact pads in gold color were thickened by 50 nm Ti/550 nm Au in the last process step to protect the thin oxide layer underneath during wire bonding. The electrical transport measurements were conducted in our 4 K cryogenic system with magnetic field applied between -0.25 T and 0.25 T, and at temperatures between 7 K and 20 K using DC measurement circuits. DC gate voltage V_g was applied on the two gate contact pads (“LG” and “RG”) above threshold to induce 2DEG and turn on the device channel. At each temperature, we varied the gate voltage V_g between 1 V and 7.5 V to change the electron density in the channel. At each gate voltage, by sweeping the magnetic field between -0.25 T and 0.25 T, I_{sd} , V_{xx} and V_{xy} were measured. Then, $R_{xx} = V_{xx}/I_{sd}$ and $R_{xy} = V_{xy}/I_{sd}$ can be plotted as functions of the applied field B . Fig. 4.12 shows an example R_{xx} and R_{xy} vs B data at 7 K, with 1.8 V applied on the gate and the I_{sd} measured with -80 mV voltage source bias. For each measurement, the magnetic field was first swept forwards from negative to positive and then swept backwards from positive to negative to ensure good data reliability. The electron density at each gate voltage can be calculated by $n_s = \frac{B}{eR_{xy}}$, where e is the elementary charge,

and $\frac{B}{R_{xy}}$ is the reciprocal of the fitted slope of R_{xy} vs B data (see the blue solid line in Fig. 4.12). The electron mobility can be calculated by $\mu_e = \frac{1}{en_s R_{sq}}$, where $R_{sq} = \frac{R_{xx}}{\text{number of squares}}$ is the sheet resistance along the xx direction at zero field (here, number of squares = 6). Shown in Fig. 4.13(a) and (b) are the extracted n_s vs V_g data and μ_e vs n_s data at 7 K, respectively. Here we use constant voltage source to measure the source-drain current I_{sd} between “S” and “D”. To check the uncertainties introduced by the voltage source, the data were measured with different biases and polarities as shown in Fig. 4.13. It can be seen that the data measured in different bias series align well with each other, so we choose to use 80 mV single bias for the measurements at higher temperatures. Fig. 4.13(a) shows good linearity between the gate voltage and the electron density above ≈ 1 V, indicating that the MOS gate can turn on the channel and well manipulate the induced 2DEG underneath it. From the average of the extracted linear slopes at different temperatures (Fig. 4.15(a)), the gate capacitance density can be calculated as $(1.11 \pm 0.01) \times 10^{-7}$ F/cm², which indicates the SiO₂ thickness of (31.1 ± 0.3) nm that agrees well with the ellipsometry measurement. Fig. 4.13(b) shows that the peak mobility ≈ 2720 cm²/Vs was achieved at $V_g \approx 5.5$ V and $n_s \approx 3.3 \times 10^{12}$ cm⁻². These data imply that these test devices are able to perform transport measurements and reveal the oxide interface properties for these quantum dot devices on the same chip sample.

To extract the percolation threshold density, we plot the measured conductivity ($\sigma = 1/R_{sq}$) vs the electron density (n_s) data at each temperature and fit the



(a)



(b)

Figure 4.13: Extracted electron density and mobility data from Hall measurements at 7 K. The data were measured with different biases and polarities to check the uncertainties introduced by the voltage source. (a) Extracted n_s vs V_g data from a series of Hall measurements at 7 K. (b) Extracted μ_e vs n_s data from the same series of Hall measurements at 7 K.

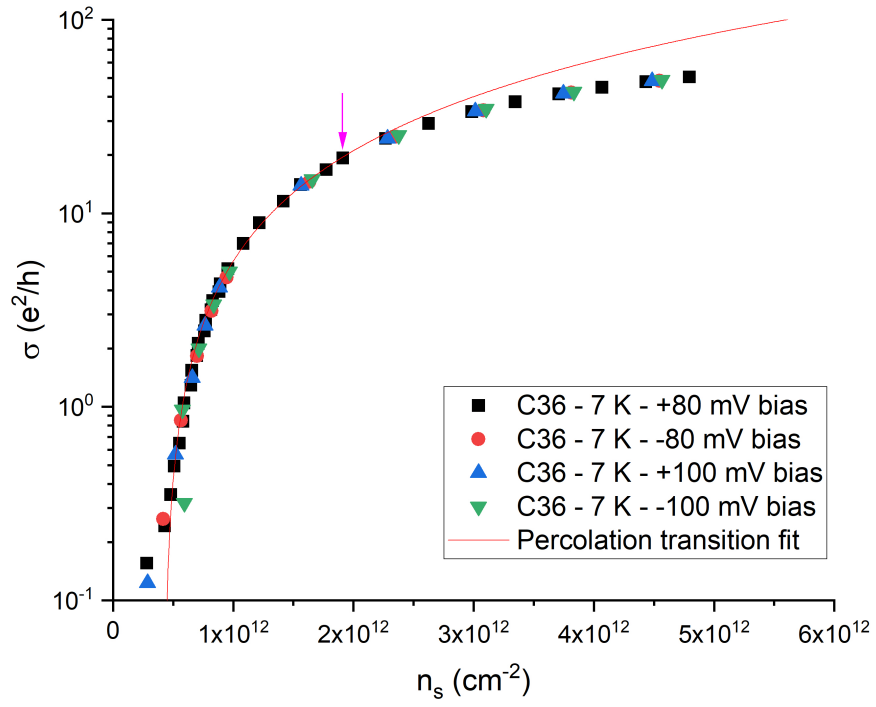
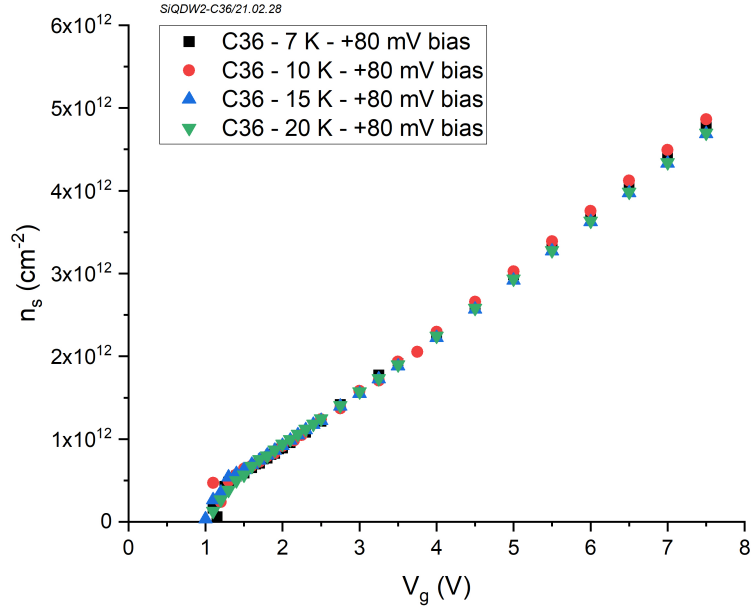


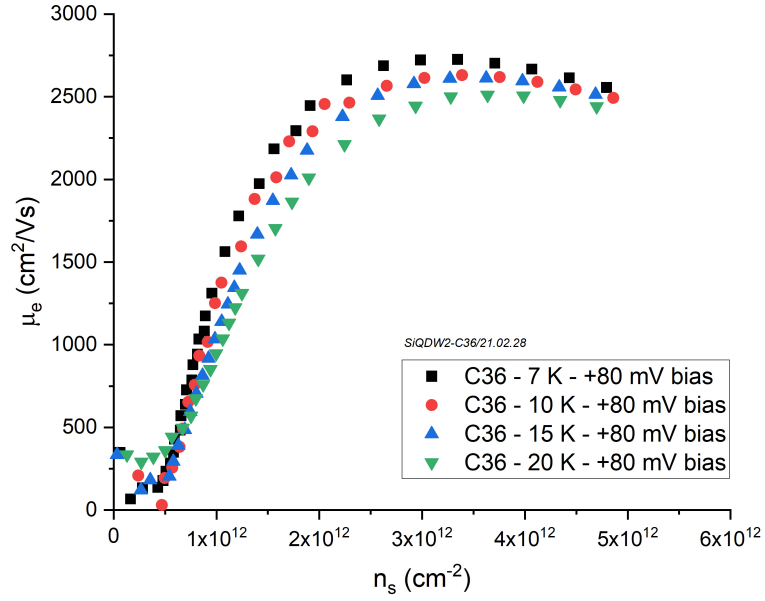
Figure 4.14: An example percolation transition fit for the σ vs n_s data at 7 K. The data is fit at low electron density range ($\leq 2 \times 10^{12} \text{ cm}^{-2}$), marked by the arrow. $n_p \approx 4.2 \times 10^{11} \text{ cm}^{-2}$ from the fit.

data with a percolation transition model [134] of the form $\sigma(n_s) = A(n_s - n_p)^p$ and extract the percolation threshold density, n_p . n_p provides a measure of the minimum number of electrons required to fill the disorder landscape before a conducting channel can be turned on [126]. p is the critical percolation exponent and is held at 1.31 here, which is the expected value for a 2D system. A is the pre-factor, which we leave as a free parameter here. Shown in Fig. 4.14 is an example percolation transition fit for the σ vs n_s data at 7 K. We fit the data at low electron density range ($\leq 2 \times 10^{12} \text{ cm}^{-2}$, marked by arrow in the Fig. 4.14) with holding p at 1.31 since this is the data range that determines n_p . The data are fit well in this range, as shown in Fig. 4.14. And we extract $n_p \approx 4.2 \times 10^{11} \text{ cm}^{-2}$ at 7 K. This value is in the same order of magnitude compared to other published results [126, 134] at this temperature, therefore is a reasonable percolation threshold density for MOS devices.

A more desired indicator to evaluate the oxide interface quality is the zero temperature percolation threshold density, n_0 . By measuring transport data and extracting n_p at various temperatures, n_0 can be extrapolated by using the functional form $n_p = n_0 + Ce^{-b/T}$ to extrapolate the percolation threshold to zero temperature. The exponential term b is an energy gap related to the impurity distribution of the system. We conducted preliminary temperature series of Hall transport measurements from 7 K to 20 K, as shown in Fig. 4.15. The linearity between the electron density n_s and gate voltage V_g doesn't change obviously with the temperature but the electron mobility μ_e decreases with increasing temperature. We follow the same procedure of extracting n_p at 7 K to extract n_p at other temperatures and plot n_p vs



(a)



(b)

Figure 4.15: Extracted electron density and mobility data from temperature dependent Hall measurements. (a) Extracted n_s vs V_g data from temperature dependent Hall measurements. (b) Extracted μ_e vs n_s data from temperature dependent Hall measurements.

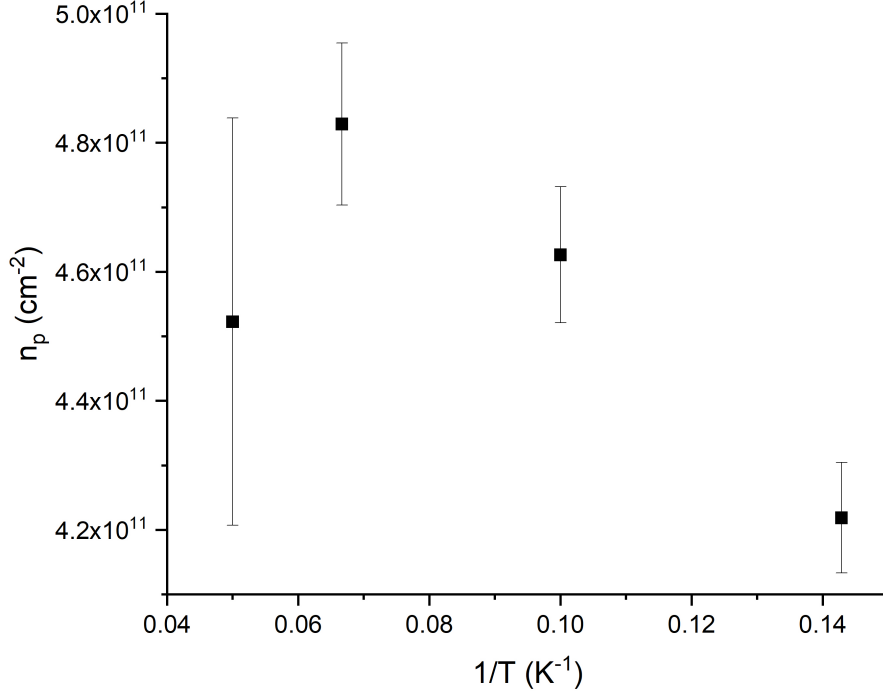


Figure 4.16: Extracted percolation threshold density n_p at various temperatures. Error bars represent the fitting errors.

$1/T$ in Fig. 4.16. For temperatures between 7 K and 15 K, n_p increases with increasing temperature as expected, according to the extrapolation function. However, it's impossible to extract a precise n_0 value from this preliminary data set due to the lack of data at low temperatures and deviation of the data at 20 K. More complete data sets for n_p vs $1/T$ and the extracted n_0 value will be evaluated in future work. In general, this preliminary data set shows comparable n_p values compared to other published data [126, 134] and indicate reasonable oxide interface quality for these MOS quantum dot devices.

4.5 Discussion and Summary

Finally, we discuss the performance vs. fabrication efficiency for this design approach. Our intent is to develop a straightforward fabrication process to make electrically robust and chip-compatible quantum dots as a step towards the longer term goal of a diagnostic qubit. Compared to multilayer devices in general, single-layer devices have fewer fabrication steps and failure mechanisms, which can lead to a higher device yield. As a trade-off, the single-layer devices presented in this paper have less direct control of the dot's electrostatic potential compared to multilayer devices and will likely make reaching the single-electron regime more challenging. As we have seen, the location of the dots and the barriers do not always seem to be as intended and additional resonances in the channel are common.

Given the simplicity of the devices, the possible sources for the non-idealities in the transport are limited. Some nonideal features may arise from film microstructure and grains within the gate metals, which we observed in SEM and atomic force microscope (AFM) images (see Fig. 4.17) taken after the electrical measurements. Additionally, during these measurements, the end-to-end electrical resistance of the inversion gate line was very high, implying structural defect(s) somewhere along the gate. Another defect mechanism observed in other devices is the partial delamination of Pd layer while the Ti layer appears to stick well to the SiO₂. Further, some of the irregular features in the transport and charge sensing measurements may arise from Si/SiO₂ interface traps or an irregular potential at the Si/SiO₂ interface. These nonidealities can induce unintended barriers and give rise to unintended dots,

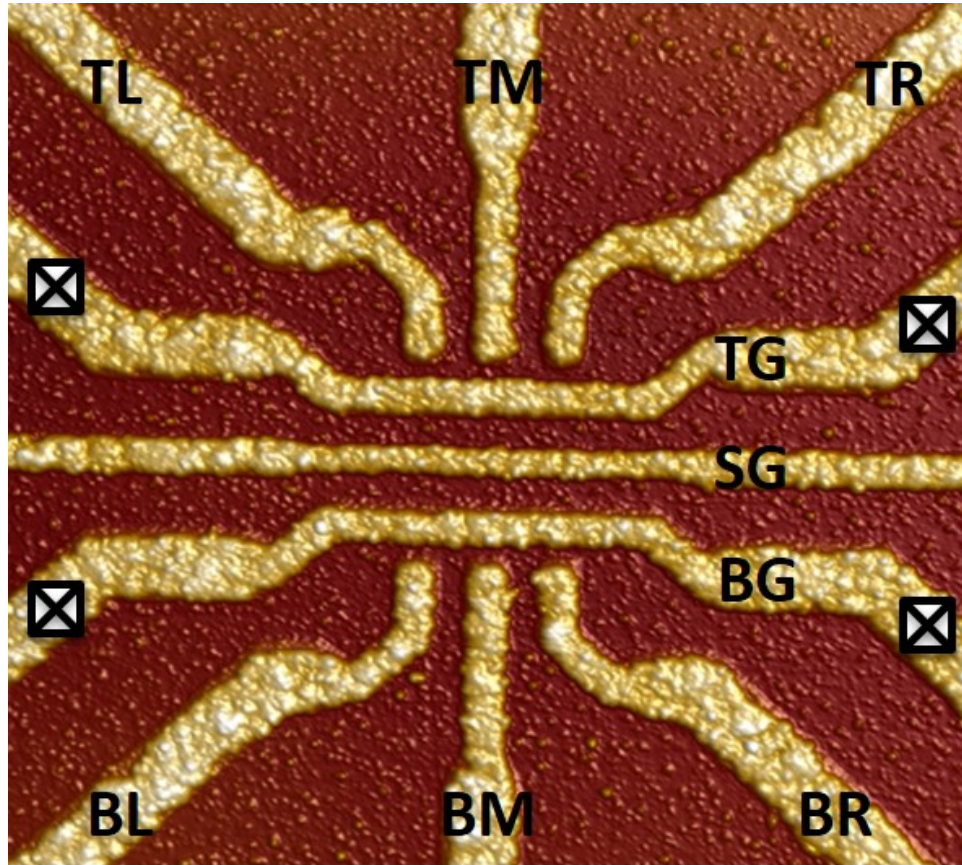


Figure 4.17: (Taken by Dr. Pradeep Namboodiri) Atomic force microscope (AFM) image of an identical device revealing the gate metal film quality in the device fine structure.

device instability, and noise at a variety of frequencies, etc.

Future improvement of these devices to yield cleaner dots and enable reaching the few-electron regime could include additional diagnostic measurements on the gate materials and gate oxides, and a focus on the gate line pattern and e-beam dose. Due to the fabrication simplicity, the gate material stack and the gate oxide can be tested relatively quickly in this single-layer diagnostic platform to optimize the material deposition in terms of grain size, thickness, and the anneal parameters for lithographic fidelity, wire conductivity and resultant dot performance. Additionally, the design rule can be substantially reduced, and thus the dot size, which increases the charging energies and makes reaching the few-electron regime more likely. Smaller dots can also decrease the cross section with defects in the oxide which might otherwise dominate the device. Finally, improved modelling for matching the observed capacitances with electrostatic models and extending these to accurately predict inversion areas can allow for gate designs with smoother potentials in the channel and fewer unintended barriers. Progress in these directions could help these single-layer devices approach the single-electron regime.

The generation of devices presented here provides a simple testbed for examining these materials and design issues for rapid feedback. Based on these devices, future work and refined devices are expected to extend to spin readout, single-shot statistics, and the eventual implementation of a spin qubit, etc.

Chapter 5: Study and Improvement of Measurement Noise

In quantum science research, both cryogenic temperatures and low measurement noise are required for high fidelity. In this chapter, I will present the work on studying and improving the measurement noise. Temperature-dependent conductance measurements and comparison of effective electron temperature (T_e) using two different quantum dot systems, P donor-based and MOS-based Si quantum dots, will be discussed. Measurements are made in various cryogenic systems over temperatures varying from 10 mK to 25 K. The effective electron temperature is extracted by fitting the experimental data using theoretical models. The Coulomb resonance is not only thermally broadened by the thermal temperature but also broadened by other temperature-independent sources such as gate noise, triboelectric noise, etc. The noise origins and factors inducing high T_e are discussed and analyzed. The noise level in a dilution refrigerator (DR) with ≈ 10 mK base temperature was substantially lowered from ≈ 4 K to ≈ 0.5 K by rearranging ground configuration and noise filtering.

The P donor-based Si quantum dots used in this chapter is provided by R. M. Silver research group at National Institute of Standards and Technology.

5.1 Introduction

In the quantum measurements of solid-state quantum computing devices, both cryogenic “bath” temperature and low measurement noise are required for high-fidelity quantum state readout, through spin-to-charge conversion and charge detection. For the former, the cryostat’s base temperature (the devices’ bath temperature, T_b) has been lowered to ≤ 10 mK in sophisticated $^3\text{He}/^4\text{He}$ dilution refrigerators [135]. For the latter, one indicator of the device noise – effective electron temperature (T_e), can usually be one to two orders of magnitude higher than T_b [136]. In the electron transport measurements, the high measurement noise or poor thermalization can increase the thermal energy of the electrons and smear out the quantization of electron motion and charge, presenting limitations for coherent measurements and device integration.

To evaluate T_e , a common way is to measure the peak width broadening of the Coulomb resonance peak. The full width at half maximum (FWHM) of a Coulomb resonance peak (Coulomb peak width) in a quantum dot is determined by the tunnel coupling between the quantum dot and the electron reservoirs ($\hbar\Gamma_c$), and the thermal broadening (T_e) [137]. When the conductances of the tunnel barriers are small ($\ll \frac{e^2}{h}$), the peak broadening due to the tunnel coupling ($\hbar\Gamma_c$) is small, which indicates that the tunneling process of higher order is suppressed [138], and the peak broadening is dominated by the thermal broadening, T_e , at small source-drain bias. High T_e in the measurement may come from noise sources extrinsic to the device or from intrinsic noise in the device, which can be measured by the broadening of

Coulomb blockade peaks in the measurements of quantum dot devices.

For the temperature broadening of the Coulomb peaks' lineshape, typically the temperature can be divided into three regimes [35]:

- 1) High temperature regime, $e^2/C_\Sigma \ll k_B T_e$, where the thermal energy, $k_B T_e$, exceeds the quantum dot's charging energy, e^2/C_Σ (C_Σ is the dot's total capacitance), leading to the fact that the discreteness of charge on the dot cannot be discerned. In this regime, the device conductance (G_∞) does not depend on the electron occupation of the dot and is completely determined by the ohmic sum of the left and right tunnel barriers, $1/G_\infty = 1/G_{\text{left}} + 1/G_{\text{right}}$.
- 2) Classical or multi-level regime, $\Delta E \ll k_B T_e \ll e^2/C_\Sigma$ (ΔE is the energy level spacing of the dot for electron occupation), where many levels are excited by thermal fluctuations. In this regime, the lineshape of an individual conductance peak is given by [99, 100]:

$$\frac{G}{G_\infty} = \frac{e\alpha\Delta V_g/k_B T_e}{2\sinh(e\alpha\Delta V_g/k_B T_e)} \approx \frac{1}{2} \cosh^{-2} \left(\frac{e\alpha\Delta V_g}{2.5k_B T_e} \right) \quad (5.1)$$

where $\alpha = C_g/C_\Sigma$ is the lever arm of the plunger gate, and $\Delta V_g = |V_g - V_{g,c}|$ is the distance to the peak center along the gate voltage direction. In this regime, the FWHM of a single peak has a linear temperature dependence: $e\alpha \cdot \text{FWHM} = 4.35k_B T_e$ [95]. Also, the single conductance peak maximum G_{max} in this regime is constant with varying temperatures, $G_{\text{max}} = G_\infty/2$. The factor of 2 in this conductance expression is due to that the probability of an electron tunneling through the dot in this regime decreases to half compared to the high temperature regime, be-

cause an electron can only tunnel on after the previous one tunnels off [35]. Fig. 5.1 shows an example of the calculated Coulomb blockade oscillations varying with temperature in the classical regime based on our Al/AlO_x/Al SETs (detailed in Section 3.3.4). Each oscillation curve is an integration of 25 individual Coulomb peaks, using experimentally measured high temperature device conductances G_∞ , and Coulomb peak center $V_{g,c}$. The Coulomb oscillations are visible when $k_B T_e < 0.3e^2/C_\Sigma$ ($T_e < 1.7$ K for capacitance values used in the above example), also confirmed by our experimental observations [54].

3) Quantum or single-level regime, $k_B T_e \ll \Delta E, e^2/C_\Sigma$, where the tunneling happens only through a single energy level on the dot. In this regime, the lineshape of an individual conductance peak is given by [99, 139]:

$$\frac{G}{G_\infty} = \frac{\Delta E}{4k_B T_e} \cosh^{-2} \left(\frac{e\alpha \Delta V_g}{2k_B T_e} \right) \quad (5.2)$$

In this regime, the temperature dependence of the peak width is also linear but with a different rate: $e\alpha \cdot \text{FWHM} = 3.5k_B T_e$ [95]. In addition, the conductance peak maximum $G_{\max} = G_\infty \cdot (\Delta E/4k_B T_e)$ decreases linearly with increasing temperature in this regime, while remains constant in the classical regime. It is noted that metal quantum dots cannot access the quantum regime because ΔE of metals is very small [95].

If the quantum dot is in the strong coupling regime, $e^2/C_\Sigma \ll h\Gamma_c, \Delta E$, the zero-temperature lineshape of the Coulomb peak is given by the Breit-Wigner for-

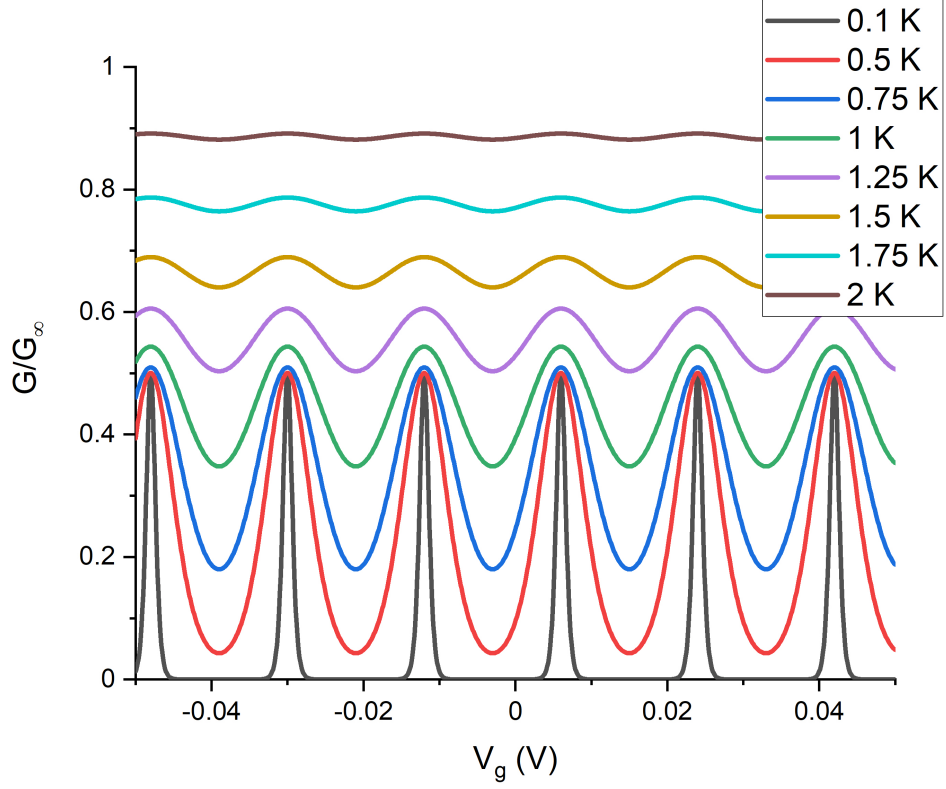


Figure 5.1: Calculated Coulomb blockade oscillations varying with temperatures in the classical regime based on our Al/AlO_x/Al SETs (detailed in Section 3.3.4). Each oscillation curve is an integration of 25 individual Coulomb peaks, using experimentally measured high temperature device conductances G_{∞} , and Coulomb peak center $V_{g,c}$. The Coulomb oscillations are visible when $k_B T_e < 0.3e^2/C_{\Sigma}$ ($T_e < 1.7$ K for capacitance values used here), also confirmed by our experimental observations [54].

mula [140]:

$$G = \frac{2e^2}{h} \frac{(h\Gamma_c)^2}{(h\Gamma_c)^2 + (e\alpha\Delta V_g)^2} \quad (5.3)$$

The conductance peak maximum equals to the conductance quantum, $2e^2/h$. Coulomb peaks in the regime $k_B T_e \sim h\Gamma_c$ have the Lorentzian lineshape of Eq. 5.3.

Here in this work, we conducted and compared noise measurements in different cryogenic systems. The electron temperature in a dilution refrigerator with base temperature $T_b \approx 10$ mK is substantially mitigated from ≈ 4 K to ≈ 0.5 K, by rearranging ground configuration and noise filtering. To study the extrinsic systematic noise origins and the intrinsic lattice couplings that affects the electron mobility, we compare noise evaluation on two different quantum dot systems, P donor-based and MOS-based Si quantum dots, cooled down together and measured using the same measurement setup on the same platform. Temperature-dependent and bias-dependent Coulomb blockade peak width are measured in different cryogenic setups over temperatures ranging from 10 mK to 25 K. The upper bound of the effective electron temperature T_e is extracted by fitting the experimental data using the theoretical models in the classical regime. We finally found that it's currently impossible to observe the T_e difference caused by intrinsic noises and distinguish between extrinsic noises and intrinsic noises, as we are still limited by the lead noise at low thermal temperature.

5.2 Devices and Experimental Methods

The Coulomb blockade peak width of two different quantum dot systems are compared in this chapter, P donor-based and MOS-based Si quantum dots, to study the measurement noise. The MOS-based Si quantum dot devices used in this work have the same fabrication process as detailedly described in Chapter 4. Here we briefly introduce the P donor-based Si quantum dots.

5.2.1 P Donor-Based Si Quantum Dots

One type of devices compared in this work is the scanning tunneling microscope (STM)-patterned atom-scale P donor-based silicon quantum dot device [2, 141]. The critical part of the atomically precise fabrication is STM-based H-depassivation lithography, which is patterning the H terminated silicon surface, Si(100) 2×1 : H in a UHV environment and has been developed by several research groups in the past years [142, 143, 144, 145, 146]. Using STM hydrogen (H)-depassivation lithography, SETs with smaller dots on the scale of the atomic lattice can be fabricated with near atomic precision, relative to atomically aligned source, drain and gates.

Here we briefly describe the fabrication process. A silicon chip is first cleaned and then loaded into the UHV chamber. The silicon chip is first flashed to 1200 °C for approximately 45 s to form the Si(100) 2×1 reconstruction. Then the sample surface is passivated by atomic hydrogen to form a stable and chemically inert H-terminated surface. After the passivated surface is formed, the device geometry is defined using H-depassivation lithography in the STM to selectively remove H atoms

from the surface and produce unpassivated, chemically active areas. When the device patterning is done by H-depassivation lithography, the sample surface is exposed to phosphine (PH_3) gas, to saturate the unpassivated surface areas. Phosphorus (P) adatoms are incorporated and substitute with Si atoms within the first atomic layer through a thermally activated process. The sample with patterned Si : P devices is then encapsulated with a silicon encapsulation layer by low temperature (275 °C) epitaxial Si overgrowth. The process is optimized by first depositing ≈ 11 atomic layers of Si locking layer at room temperature, and then continuing deposition at 275 °C to mitigate dopant movement in case the distortion of patterned devices, and preserve Si epitaxial growth simultaneously. After the encapsulation, the Si : P devices are enclosed underneath the Si epitaxial layer so that the sample can be securely taken from UHV without contaminating or degrading the device area. Finally, contact pads are formed by a low temperature palladium silicide process [147], where palladium is deposited and annealed to form palladium silicide, contacting with the device. Shown in Fig. 5.2 is the STM image of a typical device consisting of a dot in the center, and source, drain, and two in-plane gate electrodes. Table 5.1 shows the modelled capacitance values calculated by FastCap software packages for a typical STM-patterned P donor-based Si quantum dot device as shown in Fig. 5.2 [2].

Capacitance (aF)	Source	Drain	Gate1	Gate2	Total
Dot	5.1	5.1	1.2	1.1	12.5

Table 5.1: FastCap modeled capacitance values (aF) between source, drain, gate electrodes and dots, and the total capacitance for a typical STM-patterned P donor-based Si quantum dot device as shown in Fig. 5.2 [2].

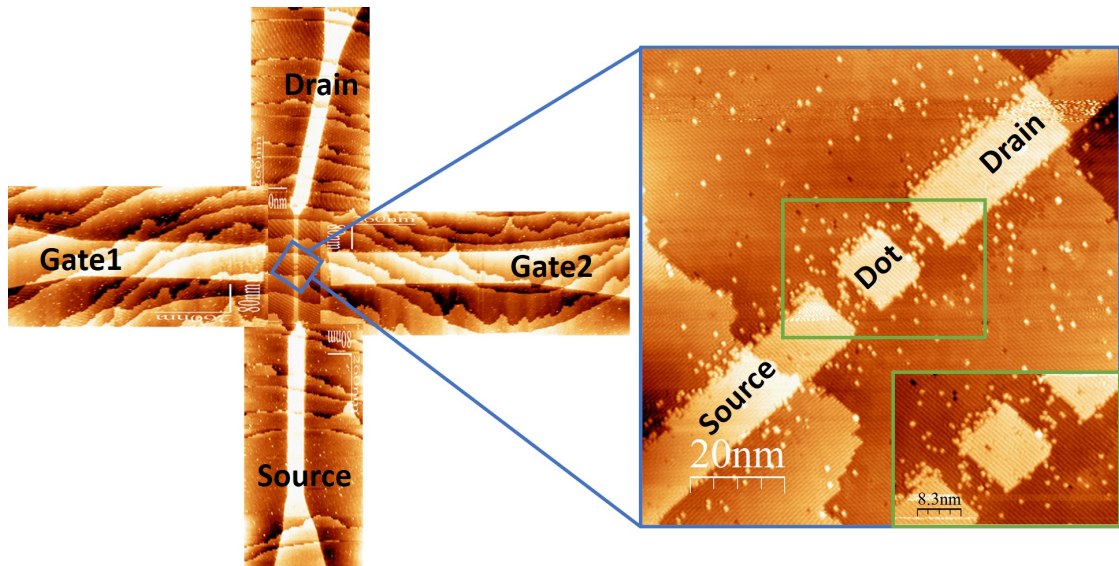


Figure 5.2: (Taken by Dr. Xiqiao Wang) STM image showing a typical atom-scale P donor-based silicon quantum dot device consisting of a dot in the center, source, drain, and two in-plane gates. The left panel is a larger-scale view and the right panel is a smaller-scale view of the device fine structure with an inset showing a close view of the atom-scale quantum dot.

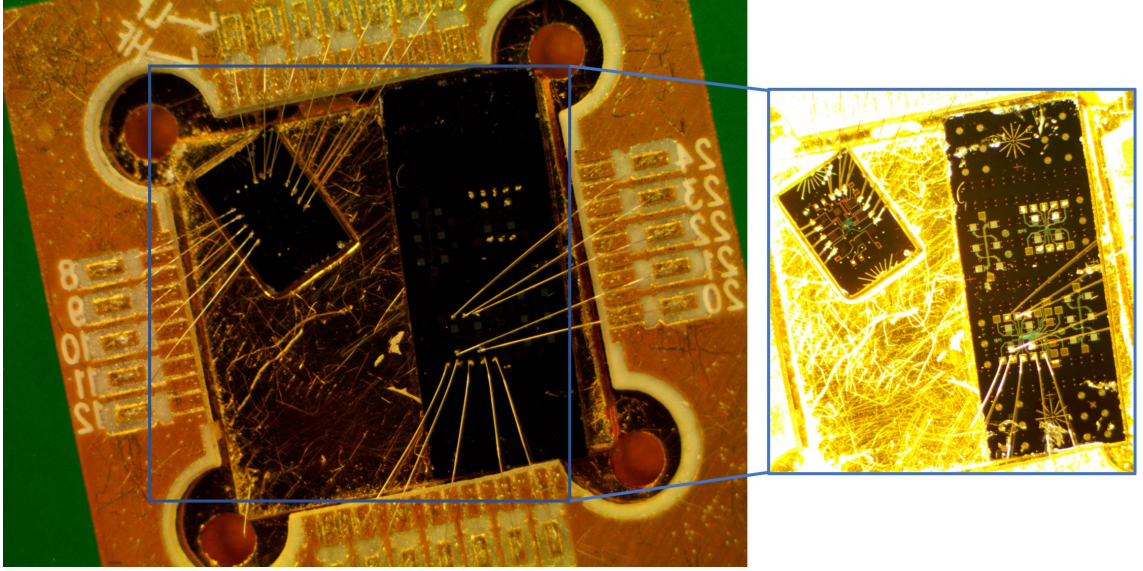


Figure 5.3: Sample box with both device chips wire bonded for simultaneous measurement in DR. The left panel is an overall view of the sample box with LF and HF wire bonding pads. The right panel is a close view of the devices with contact pads wire bonded.

5.2.2 Sample Configuration for Simultaneous Measurement

Shown in Fig. 5.3 is the sample box with both device chips (P donor-based and MOS-based Si quantum dots) wire bonded for simultaneous measurement in our DR. There are 24 contact pads for 24 low-frequency (LF) signal lines and 24 contact pads for 24 high-frequency (HF) signal lines on the sample box that can be used to connect to the contact pads on the devices through wire bonding. These LF signal lines of the sample box can be connected to the DR circuits using μ D connectors and cables, and these HF signal lines are connected to the DR circuits using high speed multicoax TR connectors and cables.

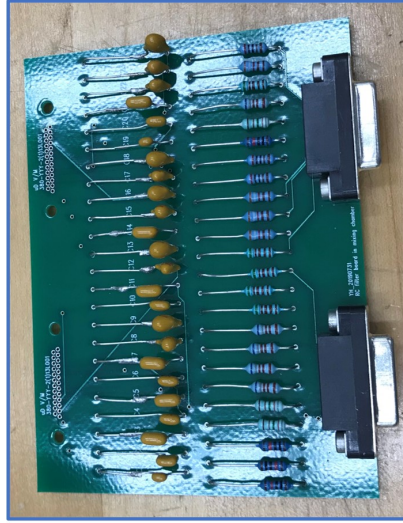
5.2.3 RC filter PCB

To implement noise filtering directly after the signal transmitting from the devices and before the signal transmitting to the devices in the mixing chamber (base temperature stage) of the DR, resistor-capacitor (RC) low-pass filters on printed circuit boards (PCBs) for 24 LF signal lines were designed and made with different low-pass filter configurations. Shown in Fig. 5.4(a) is a test board for testing the change of the roll-off characteristics of various resistor and capacitor groups at cryogenic temperatures, relative to room temperature characteristics, since the filter PCBs are designed for directly connecting to the sample box and using at cryogenic temperature stages. There are μ D connectors soldered on the PCB to insert the PCB in the DR measurement circuit, and each μ D connector connects 12 signal lines to the DR circuits. According to the the roll-off characteristics obtained and presented in Section 5.3.2, we can select and apply suitable low-pass filters for different signal lines, as shown in Fig. 5.4(b). The filter PCBs are placed between the sample box and the DR circuits, and can be cooled down together with the sample box.

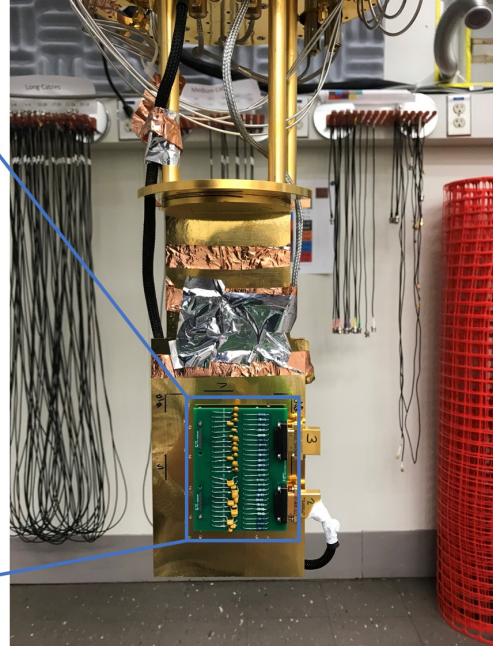
5.3 Results and Discussion

5.3.1 Discussion of Noise Origins

In quantum science research, both cryogenic temperatures and low measurement noise are required for high fidelity. For silicon quantum dot devices, an increase



(a)



(b)

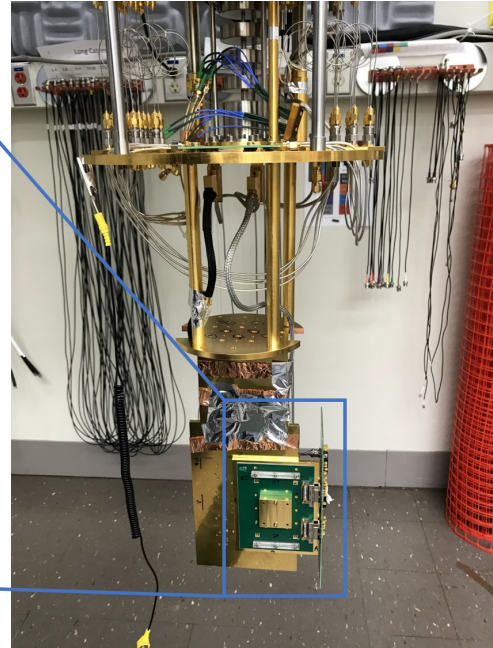


Figure 5.4: RC low-pass filter PCBs for 24 LF signal lines. (a) A test board for testing the change of the roll-off characteristics of various resistor and capacitor groups at cryogenic temperatures, relative to room temperature characteristics. (b) Filter PCBs with selected low-pass filters used in the measurements.

in either one causes broadening of Coulomb blockade peaks, which is usually referred to as a high T_e . The Coulomb resonance peak is not only thermally broadened by the actual thermal temperature or bath temperature T_b , but also broadened by other T-independent sources, such as gate noise V_g^{noise} , source-drain bias V_{sd} , source-drain noise V_{sd}^{noise} , triboelectric noise, etc. At low source-drain bias, $V_{sd} \ll E_C/e$ where E_C is the charging energy, the Coulomb peak width increases linearly with T_b when $T_b > T_e$, i.e., the thermal noise exceeds the T-independent noises. The rate is determined by $\text{FWHM} = \frac{nk_B}{e\alpha} \cdot T_b$, where $n = 4.35$ for classical regime and $n = 3.5$ for quantum regime. When $T_b < T_e$, the Coulomb peak width saturates at a constant value determined by the T-independent noises. Therefore, at low V_{sd} , the Coulomb peak width vs T_b shows a hockey stick shape as shown in Fig. 4.9(b). When V_{sd} becomes comparable to the charging energy, the contribution to the Coulomb peak width broadening from V_{sd} and V_{sd}^{noise} is not negligible. As indicated by the Coulomb diamonds in Fig. 1.3 and Eq. 6.17, the Coulomb peak width scales linearly with V_{sd} and saturates at some constant value determined by V_{sd}^{noise} .

5.3.2 Cryogenic Temperature Testing of RC Low-Pass Filters

As mentioned before, we made a test board as shown in Fig. 5.4(a) with different resistor-capacitor combinations to test the change of roll-off characteristics of various low-pass filters at cryogenic temperatures, to compare with their room temperature characteristics. Fig. 5.5(a) is the measurement circuit we implemented to efficiently test 24 low-pass filters within a single cooldown. A typical cooldown

without magnet takes approximately 32 hours from room temperature to base temperature. Here in the measurement circuit, V_{app} represents the AC voltage applied as the input, R_x is a large resistor of known resistance placed in the room temperature circuit, V_{meas} is the measurement point from room temperature circuit to measure the circuit response to an input. In the circuit inside DR that will be at cryogenic temperatures, R_f and C_f are the carbon film resistor and ceramic capacitor soldered on the PCB to make a low-pass filter, and V_{out} is the signal output point that will be connected to the device but not used in this filter test measurement. With this measurement circuit, we can apply AC voltages V_{app} on all 24 μ D lines and measure the response at V_{meas} outside the DR. If we measure the response at V_{out} inside the DR, we need to occupy half of the μ D lines for the measurement side and can only test 12 low-pass filters in a single cooldown.

Eq. 5.4 is the calculated expression of V_{meas} with a given V_{app} according to Kirchhoff's circuit laws, based on this circuit, where j is the unit imaginary number and $\omega = 2\pi f$ is the angular frequency. This is the formula to be used to fit the measurement data and extract R_f and C_f at cryogenic temperatures. To verify the validity of this measurement circuit and the theoretical formula, we measured the circuit response at room temperature with known R_x , R_f and C_f , simulated the circuit shown in Fig. 5.5(a) in SPICE (simulation program with integrated circuit emphasis), and compared with the calculated results of V_{meas} from Eq. 5.4. Fig. 5.5(b) shows an example comparison with $R_x = 100 \text{ k}\Omega$, $R_f = 10 \text{ k}\Omega$ and $C_f = 0.1 \text{ }\mu\text{F}$, where the measurement, simulation and calculation from Eq. 5.4 agree very well. Therefore, we confirmed the validity of this measurement circuit

and the theoretical formula in Eq. 5.4.

$$V_{meas} = \text{mod} \left[V_{app} - \frac{V_{app}}{R_x + R_f + \frac{1}{j\omega C_f}} \cdot R_x \right] \quad (5.4)$$

We then cooled down the filter test PCB to ≈ 4 K and ≈ 10 mK, respectively. The circuit responses were measured with different room temperature resistors (R_x) for all 24 groups of low-pass filters, at room temperature (RT), ≈ 4 K and ≈ 10 mK, and fit using Eq. 5.4 to extract the values of R_f and C_f . We found that for most groups of filters, the cutoff frequency increases by ≈ 20 times and measured voltage at high frequency limit doesn't change much, from RT to cryogenic temperatures. Since the cutoff frequency is determined by both resistance component and capacitance component via $f_c = \frac{1}{2\pi \cdot (R_x + R_f) \cdot C_f}$, and the measured voltage at high frequency limit is only determined by the resistance component via $V_{meas} = V_{app} - \frac{V_{app}}{R_x + R_f} \cdot R_x$, we can initially guess that from RT to cryogenic temperatures, R_f doesn't change much but C_f decreases by ≈ 20 times. However, for some groups of filters with larger capacitors ($1 \mu\text{F}$ and $10 \mu\text{F}$), the measured voltage at high frequency limit increases > 5 times from RT to cryogenic temperatures, which can only be explained by a large increase of the resistance component of the circuit. From the other lines with smaller capacitors, we can confirm that the same type R_f doesn't change much at cryogenic temperatures. Therefore, the possible explanation is that, for those filter groups with larger capacitors ($1 \mu\text{F}$ and $10 \mu\text{F}$), the capacitor introduces a large serial resistance component in the circuit at cryogenic temperatures. Those larger capacitors ($1 \mu\text{F}$ and $10 \mu\text{F}$) behave abnormally

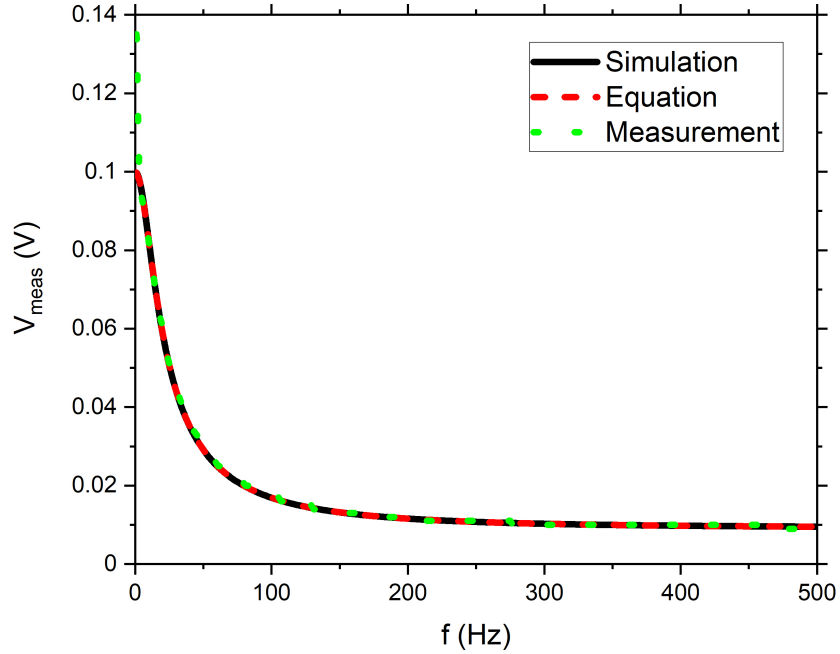
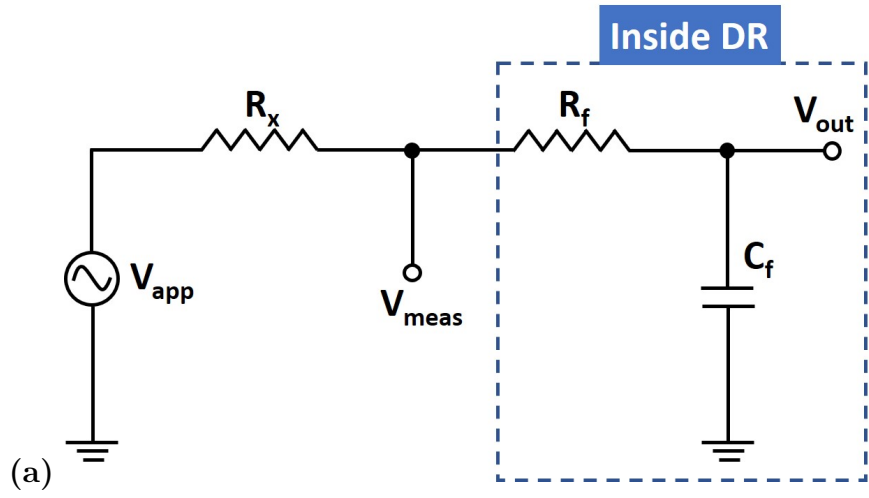


Figure 5.5: (a) The measurement circuit we implemented to efficiently test 24 low-pass filters within a single cooldown. R_f and C_f are the carbon film resistor and ceramic capacitor soldered on the PCB to make a low-pass filter. (b) An example comparison to verify the validity of the measurement circuit in (a) and the theoretical formula Eq. 5.4, with $R_x = 100 \text{ k}\Omega$, $R_f = 10 \text{ k}\Omega$ and $C_f = 0.1 \text{ }\mu\text{F}$, indicating that the measurement, simulation and calculation agree very well.

at cryogenic temperatures, so here we exclude those groups of filters for the data analyses. Fig. 5.6(a) and (b) show the ratios between the extracted 4 K values and RT values for these resistors and capacitors, respectively, using 4 different R_x in the measurements. Fig. 5.6(c) and (d) show the ratios between the extracted 10 mK values and RT values for these resistors and capacitors, respectively, using 5 different R_x in the measurements. In most cases, the resistors change within $\approx 20\%$, and the capacitors decrease by ≈ 20 times at cryogenic temperatures. To further analyze the resistor and capacitor change from RT to cryogenic temperatures, the corresponding histograms of the ratio data shown in Fig. 5.6 are plot in Fig. 5.7. It can be observed that for most resistors, the resistance change within $\approx 10\%$ at 4 K, and change within $\approx 20\%$ at 10 mK. And for most capacitors, the capacitance decreases by ≈ 15 to ≈ 18 times at 4 K, and decreases by ≈ 18 to ≈ 20 times at 10 mK. Among these, we chose two groups of low-pass filters for the device measurements ($R_f = 10\text{ k}\Omega$ and $C_f = 0.47\text{ }\mu\text{F}$ for source-drain lines, $R_f = 5.11\text{ k}\Omega$ and $C_f = 0.22\text{ }\mu\text{F}$ for gate lines) that consist of capacitors with relatively more stable performance at cryogenic temperature, as shown in Fig. 5.4(b).

5.3.3 Noise Measurements on Quantum Dot Devices

The P donor-based quantum dot devices were first checked in our 4 K cryogenic system, which takes < 2 hours to cool down to the base temperature and therefore enables fast sample turnaround. Fig. 5.8 shows the AC lock-in measured Coulomb diamonds by sweeping the voltage on the two plunger gates together (see Fig. 5.2).

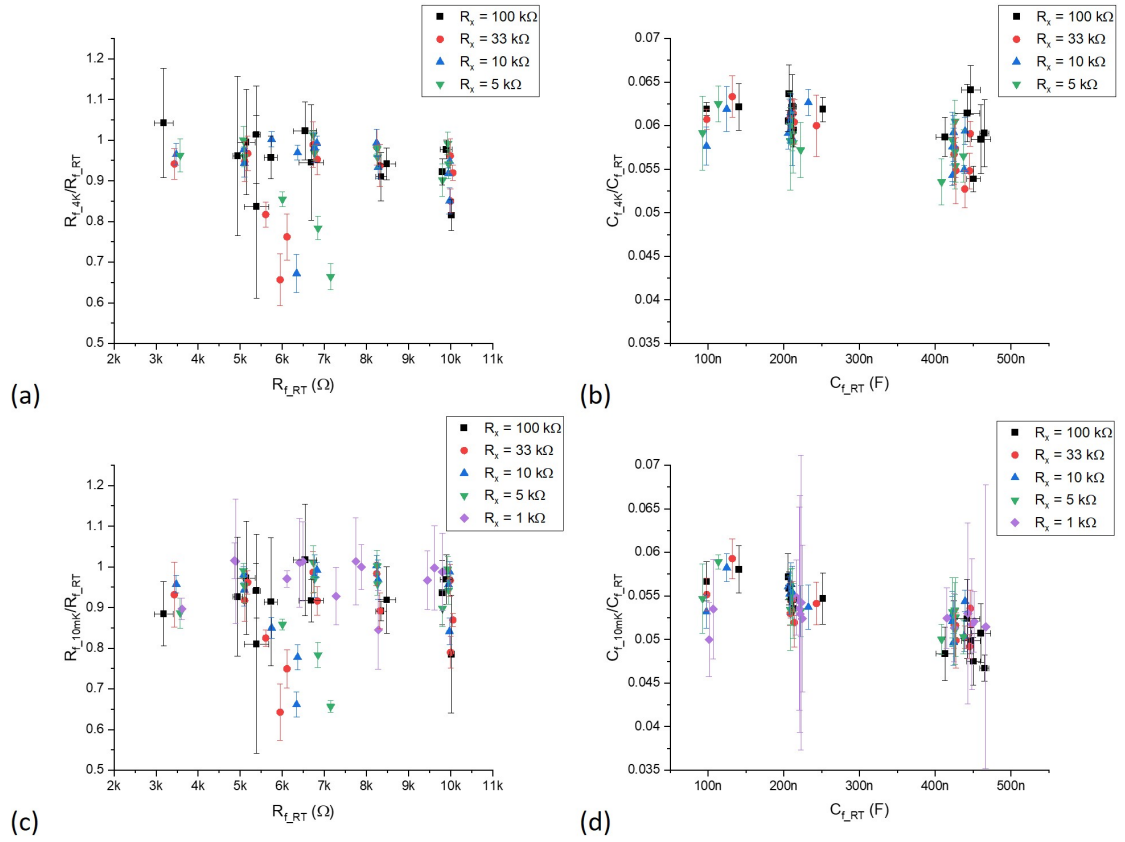


Figure 5.6: (a) and (b) show the ratios between the extracted 4 K values and RT values for these resistors and capacitors, respectively, using 4 different R_x in the measurements. (c) and (d) show the ratios between the extracted 10 mK values and RT values for these resistors and capacitors, respectively, using 5 different R_x in the measurements.

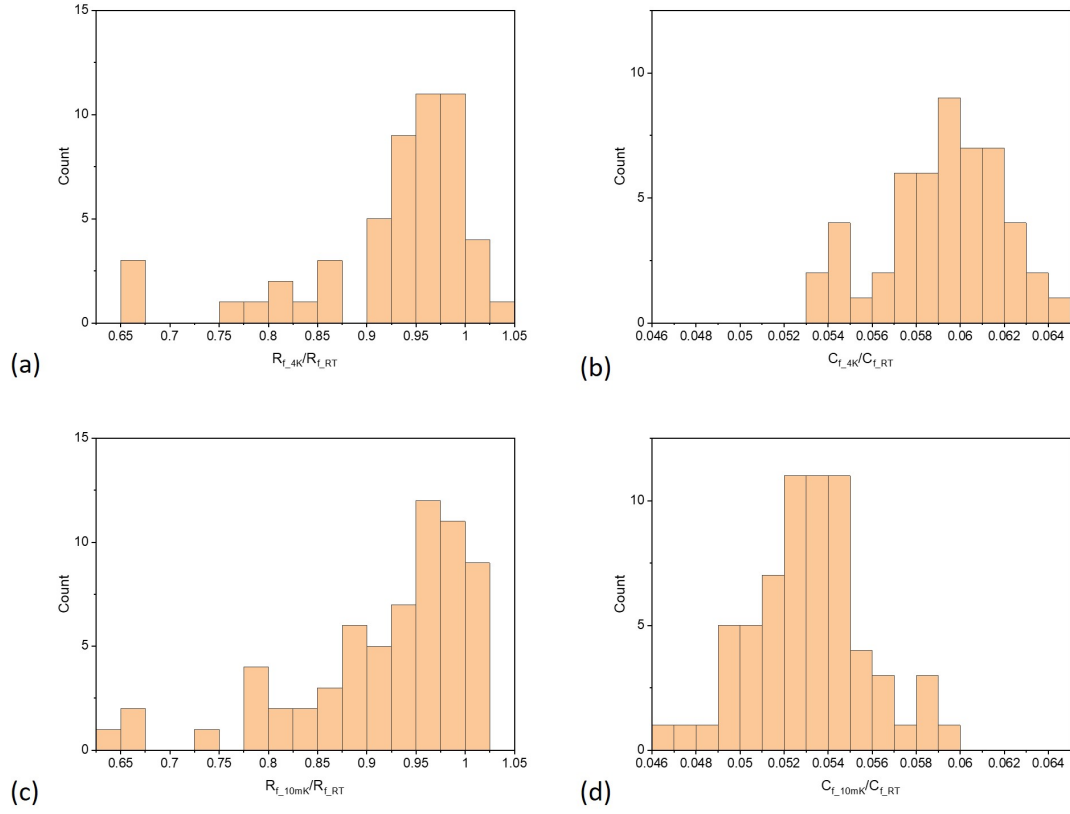


Figure 5.7: Corresponding histograms of the ratio data shown in Fig. 5.6 with (a) for resistor change at 4 K, (b) for capacitor change at 4 K, (c) for resistor change at 10 mK, and (b) for capacitor change at 10 mK.

The well defined diamonds with sharp edges imply well defined quantum dot and tunnel barrier, as well as sufficient gate control and charging energy over the thermal noise. Having the diamonds, the plunger gate lever arm can be determined through $\alpha = C_g/C_\Sigma$, where the gate capacitance can be calculated by $C_g = e/\Delta V_g$ (ΔV_g is the diamond period) and the dot's total capacitance can be calculated by $C_\Sigma = e/\Delta V_s$ (ΔV_s is the diamond height). With the lever arm obtained from diamonds, we then conducted temperature dependent measurement of zero-bias Coulomb oscillation peaks as shown in Fig. 5.9(a), to set the real energy scale of the dot by linking to the absolute temperature variation and extract the effective electron temperature T_e . As predicted by the theory, the linewidth of the Coulomb peaks is broadened by the thermal energy as the bath temperature T_b increases. Each of these peaks are fit with Eq. 4.1 and the FWHM vs T_b of the four peaks centered at four different positions in Fig. 5.9(a) are plotted in Fig. 5.9(b). The linear broadening trend can be seen but the hockey stick shape and the saturation point is absent due to that the base temperature is not low enough.

Table 5.2 summarizes the lever arm α extracted from the diamonds, base temperature FWHM of Coulomb peaks, and the calculated effective electron temperature T_e by using the classical regime formula $e\alpha \cdot \text{FWHM} = 4.35k_B T_e$. At this temperature, it's impossible to reach the quantum regime which requires $k_B T_e \ll \Delta E, e^2/C_\Sigma$. There is > 500 mK mismatch between T_e and T_b , indicating the contribution of T-independent noise sources. Due to other measurement noise and fit uncertainties, the slope of the temperature dependence is not very clear, so that we are not able to extract the lever arm from the temperature dependence to set

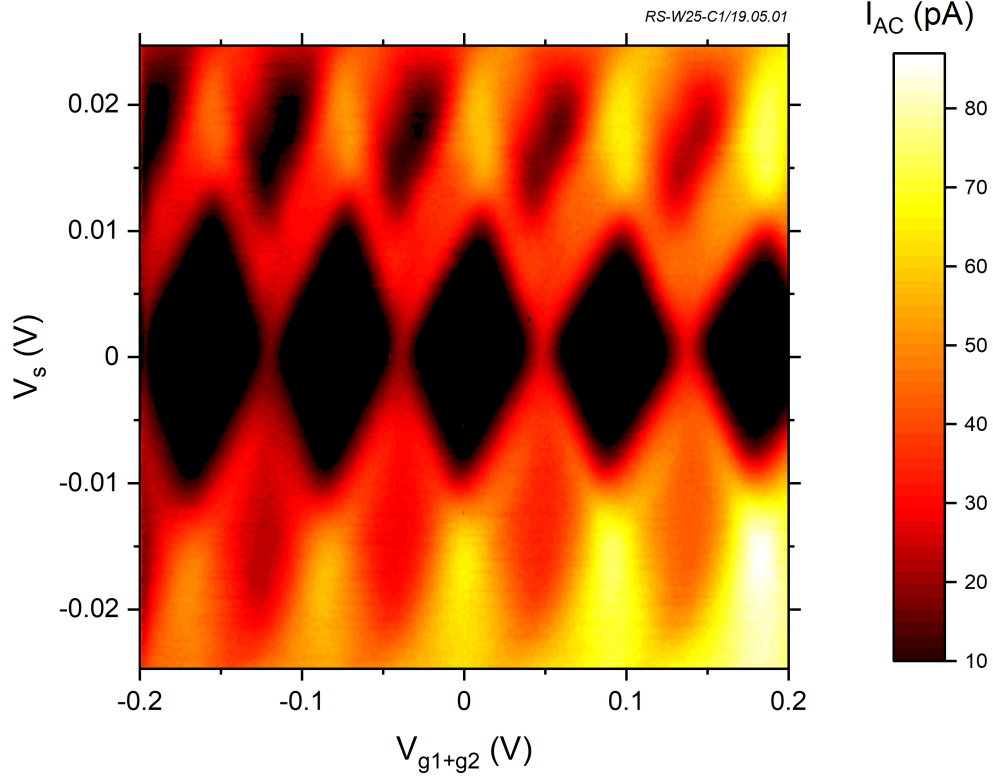
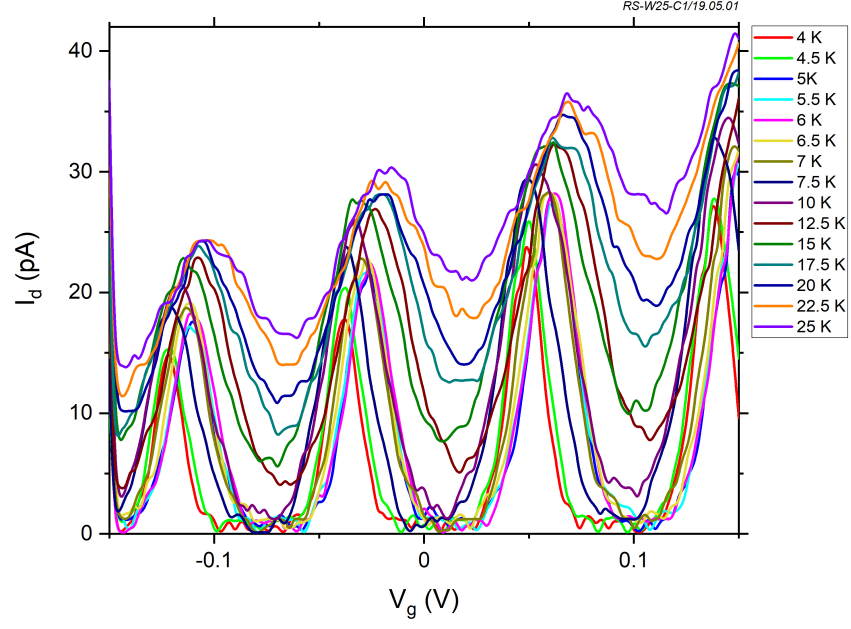
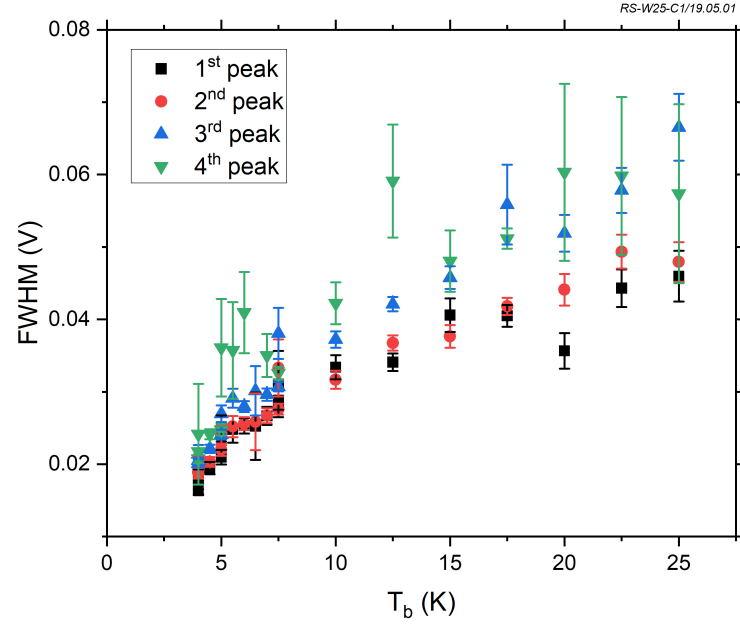


Figure 5.8: AC lock-in measured Coulomb diamonds of P donor-based quantum dot device in 4 K cryogenic system, by sweeping the voltage on the two plunger gates together. The well defined diamonds with sharp edges imply well defined quantum dot and tunnel barrier, as well as sufficient gate control.



(a)



(b)

Figure 5.9: (a) Temperature dependent measurement of zero-bias Coulomb oscillation peaks on P donor-based quantum dot device in 4 K cryogenic system. (b) Extracted FWHM vs T_b of the four peaks centered at four different positions in (a).

the real energy scale. But the calculated temperature dependence slope based on the lever arm obtained from the diamonds ($3 \text{ mV/K} \pm 0.8 \text{ mV/K}$) agrees with the general broadening rate observed from Fig. 5.9(b). Therefore, we confirmed the Coulomb blockade characteristics of the P donor-based quantum dot devices and need to lower T_b for measuring the saturation point and a hockey stick shape to get the noise limit.

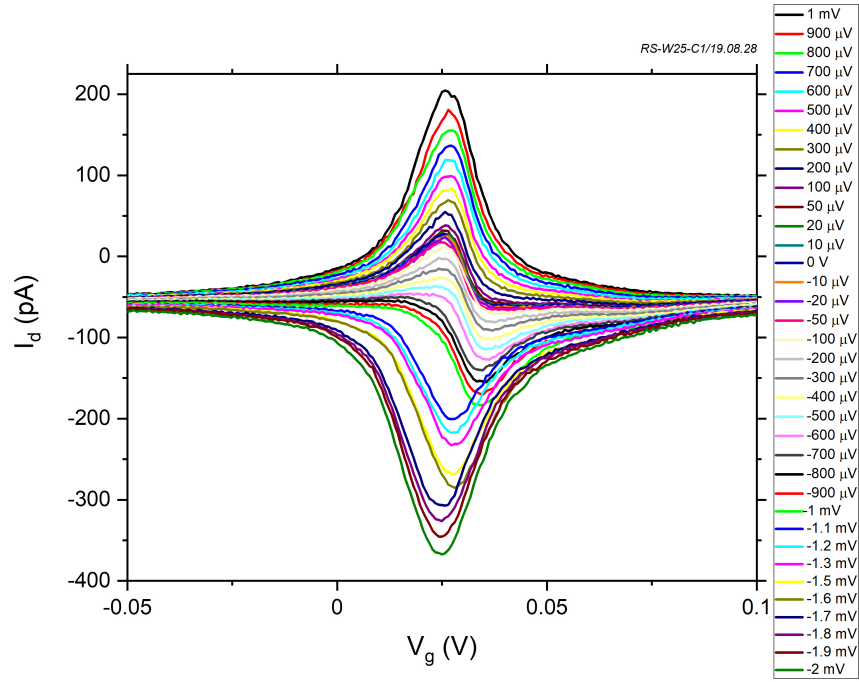
$T_b = 4 \text{ K}$	1 st peak	2 nd peak	3 rd peak	4 th peak
α	0.15	0.13	0.11	0.11
FWHM (V)	0.014	0.013	0.015	0.017
T_e (K)	5.6	4.6	4.7	4.9

Table 5.2: Summary of the lever arm α extracted from the diamonds, base temperature FWHM of Coulomb peaks, and the calculated effective electron temperature T_e by using the classical regime formula $e\alpha \cdot \text{FWHM} = 4.35k_B T_e$.

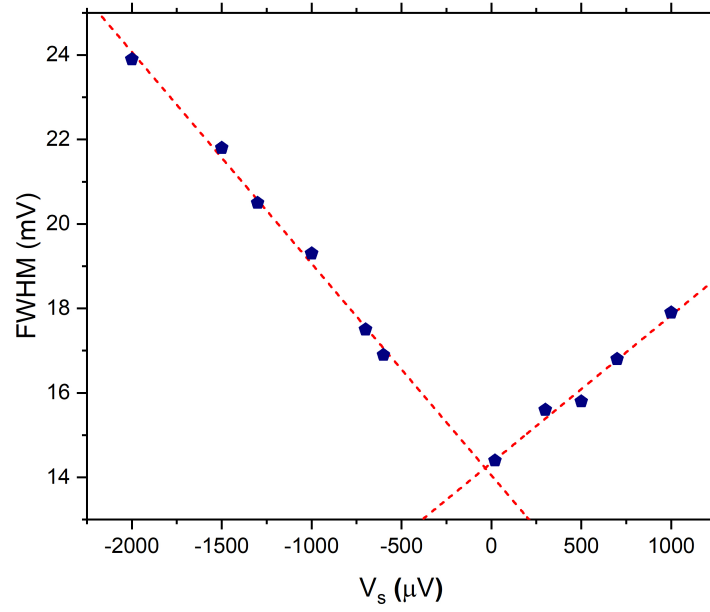
The P donor-based quantum dot devices were then cooled down to $\approx 10 \text{ mK}$ in our dilution refrigerator (DR) system, where we measured and improved the measurement noise. In a initial temperature dependent measurement of Coulomb peak linewidth with DR measurement circuit, we found that the measured peak width had a linear dependence on T_b and saturated below 2 K (not shown). A considerable mismatch ($> 2 \text{ K}$) between the lattice temperature (T_b) and the carrier temperature (T_e) was observed. Therefore, we first conducted a series of measurements as discussed below to find out different noise sources. According to discussions in Section 5.3.1, the Coulomb peak width should scales down linearly with source-drain noise. To check if the source-drain bias polarity affects the noise and confirm the linearity of FWHM vs source-drain noise, we conducted bias dependent measurement of an individual Coulomb peak with the source-drain bias varying from -2 mV

to 1 mV, as shown in Fig. 5.10(a) and the fitted peak width using Eq. 4.1 vs V_s of some peaks is plotted in Fig. 5.10(b). In Fig. 5.10(b), the two dash-dotted lines represent linear fits in positive and negative bias sides, respectively. First, both the positive and negative sides show good linearity. Second, the two linear fits intersect at near zero-bias point with ≈ 14 mV FWHM, confirming the existence of other noise sources which are independent of both bias values and polarities. Third, the absolute value of the scaling factor is 30 % smaller at the positive side than that at the negative side, may indicating some source-drain noises at the negative bias side only.

We then conducted DC Coulomb diamond measurements to confirm the existence of various noise sources. Shown in Fig. 5.11(a) is a partially measured Coulomb diamond near zero source-drain bias. Obviously, the diamond doesn't close with decreasing absolute bias values, and there is a region with constant diamond width (Coulomb peak width) extending ≈ 1 mV near zero bias along the source-drain bias direction, as guided by the dashed lines. We think the constant peak width region that precludes the closure of Coulomb diamond is the evidence of source-drain noise, $V_{sd}^{noise} \approx 1$ mV. The existence of V_{sd}^{noise} precludes the Coulomb peak width to scale down with decreasing absolute bias values and causes the Coulomb peak width to saturate, as discussed in Section 5.3.1. Fig. 5.11(b) shows a wider diamond scan of one and half diamonds in the view. It can be observed that there are some shaded regions of small diamond shape outside the main diamonds, looking like shadows of the diamonds on both left and right sides along the V_g direction. We think these shaded regions duplicating the diamond shape are more associated with the gate



(a)



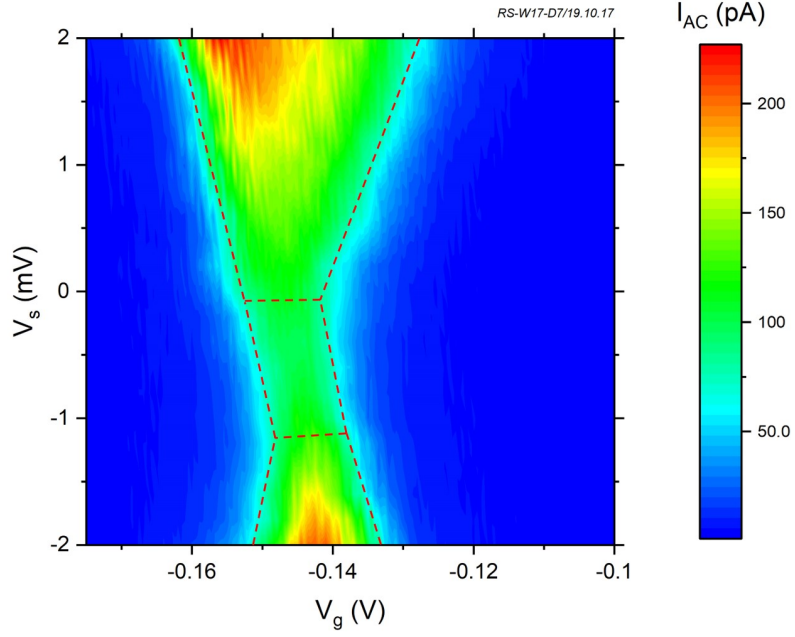
(b)

Figure 5.10: (a) Bias dependent measurement of an individual Coulomb peak on P donor-based quantum dot device at ≈ 10 mK in DR. (b) Extracted FWHM vs V_s of some peaks in (a).

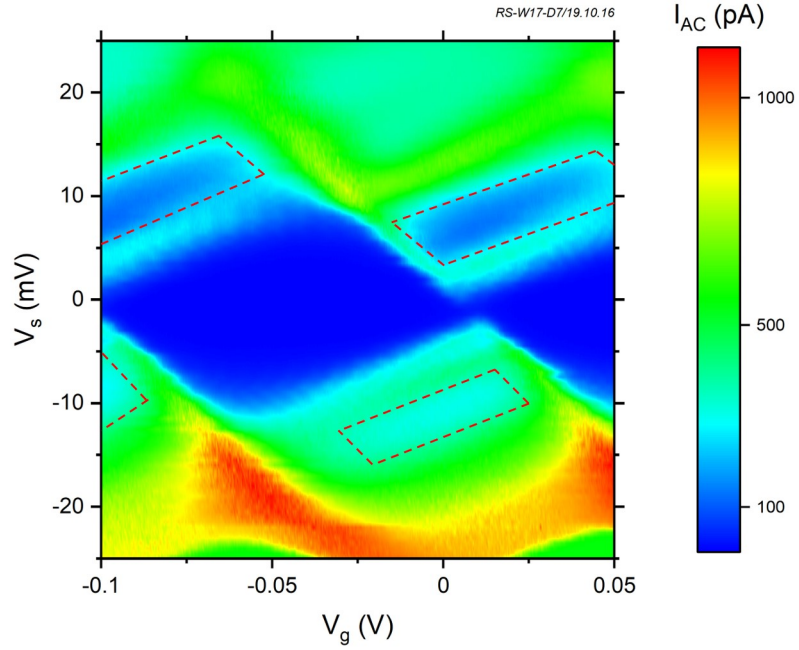
noise, V_g^{noise} .

After checking the existence of these noise sources, the measurement circuits were adjusted to mitigate noise. Inside the DR, we made and installed low-pass filter PCB as discussed in Section 5.3.2. Outside the DR, we improved the ground configuration between the DR and other measurement instruments, and applied room temperature low-pass filters on source, drain and gate lines. These adjustments were guided by suppressing the noise amplitude, which is monitored using a spectrum analyzer over the range of < 1 kHz. With these noise mitigation, we substantially narrowed down the zero-bias Coulomb peak width on similarly fabricated P donor-based Si quantum dots from ≈ 14 mV to ≈ 1.9 mV, as shown in Fig. 5.12(a). The dotted line shows the fit for extracting the peak width. Fig. 5.12(b) shows the measured partial Coulomb diamond near zero source-drain bias after noise mitigation. The diamond now closes nicely at the intersection of the positive part and the negative part, and the offset of zero source-drain bias is also corrected, i.e., the intersection aligns with zero bias. Note that this is a different P donor-based quantum dot device but with similar fine structures and lever arm ($\alpha \approx 0.1$) used for the noise mitigation here since the previously shown device was damaged.

Another motivation of this work is to distinguish intrinsic noise sources and extrinsic noise sources by comparing two different Si quantum dot systems using the same measurement setup. The two different quantum dot systems – P donor-based and MOS-based, have different electron transport mechanisms. The electron mobility (μ_e) is very different in the two quantum dot systems: $\mu_e \approx 40$ $cm^2/(V \cdot s)$ for



(a)



(b)

Figure 5.11: (a) A partially measured Coulomb diamond near zero source-drain bias, indicating the existence of source-drain noise. (b) A wider diamond scan of one and half diamonds, indicating the existence of gate noise.

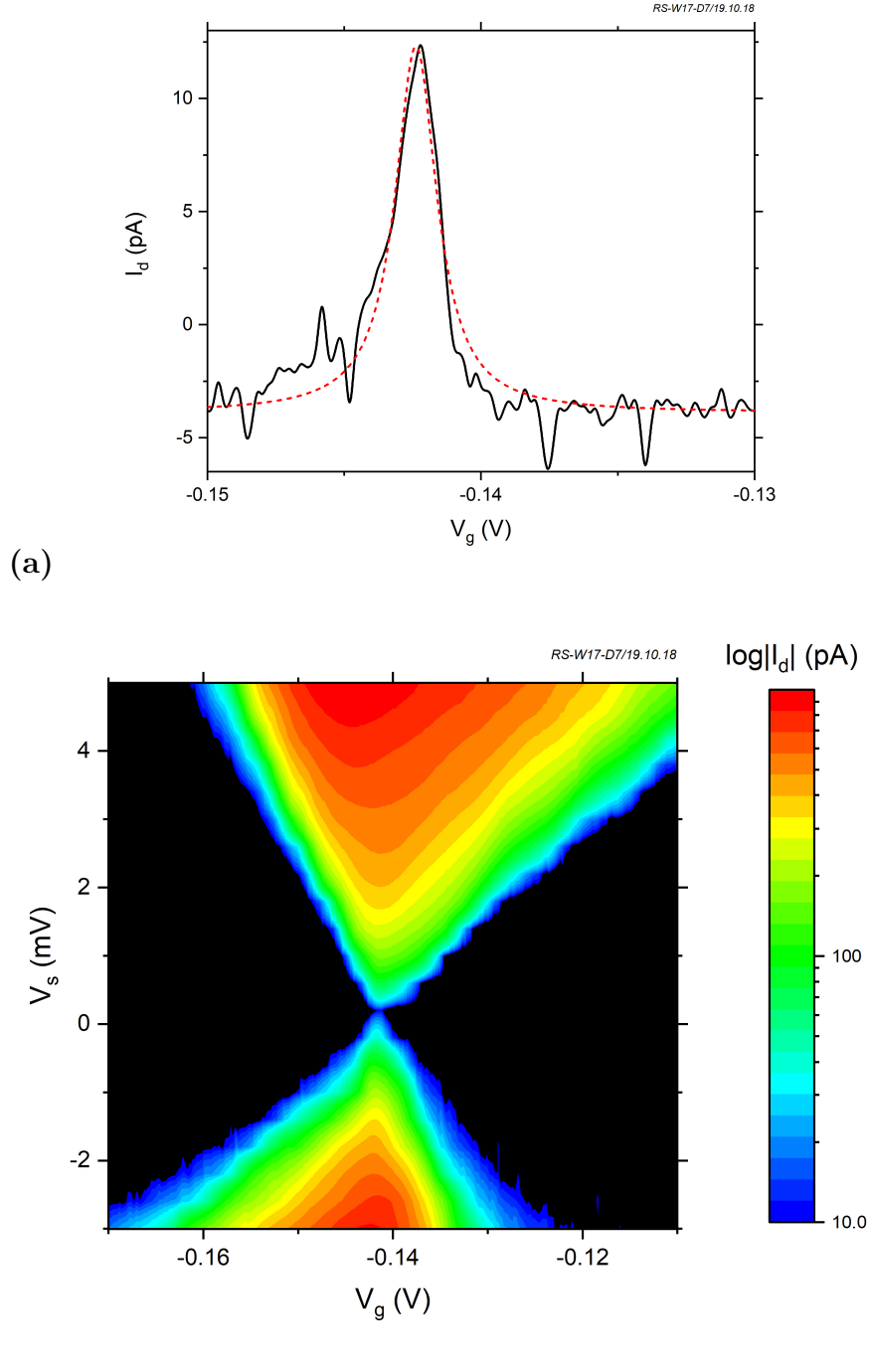


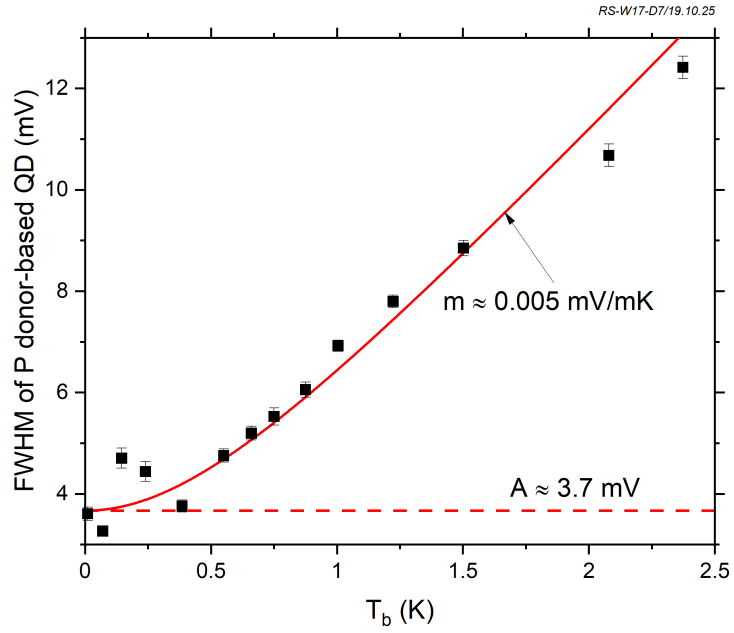
Figure 5.12: (a) Zero-bias Coulomb peak linewidth narrowed down to ≈ 1.9 mV, after noise mitigation. $V_s \approx 180 \mu V$. Dotted line shows the fit. (b) The measured partial Coulomb diamond near zero source-drain bias after noise mitigation.

P donor-based dots and $\mu_e \approx 4000 \text{ cm}^2/(V \cdot s)$ for MOS-based dots. P donor-based dots with much lower electron mobilities are expected to have the effective electron temperature much closer to the lattice temperature (bath temperature) than MOS-based dots. Whether this characteristic relates to a measurable T_e difference depends on the extrinsic noises. If the extrinsic noise occupies a large portion in the total noise, then it would be difficult to distinguish a relatively small difference in the intrinsic noise. Therefore, we wire bonded one P donor-based device and one MOS-based device in the sample box as mentioned in 5.2.2 and cooled them down simultaneously. To set up the absolute energy scale and compare the effective electron temperature on the two quantum dot systems, temperature dependent measurements of Coulomb blockade linewidth were conducted on the two devices with the same measurement setup in DR, as shown in Fig. 5.13(a) and (b), respectively. Classical regime is confirmed by the observation that the change of the Coulomb peak height with temperature follow the pattern given by the classical regime (not shown). To extract the effective electron temperature to compare noise of the two different quantum dot systems, the FWHM vs T data are fit with $\text{FWHM}(T_b) = \sqrt{(mT_b)^2 + A^2}$, same as used in Section 4.3, and the fitted curve, fitted m and A values for both devices are shown in the figures. Therefore, we obtain the upper bound of $T_e - T_e \approx 694 \text{ mK}$ for P-donor based device and $T_e \approx 347 \text{ mK}$ for MOS-based device. The reason that the P donor-based device has higher T_e may be due to its high lead noise. Therefore, it's impossible to tell the T_e difference caused by intrinsic noises, and distinguish between extrinsic noises and intrinsic noises, especially that P donor-based dots are expected to exhibit lower effective electron

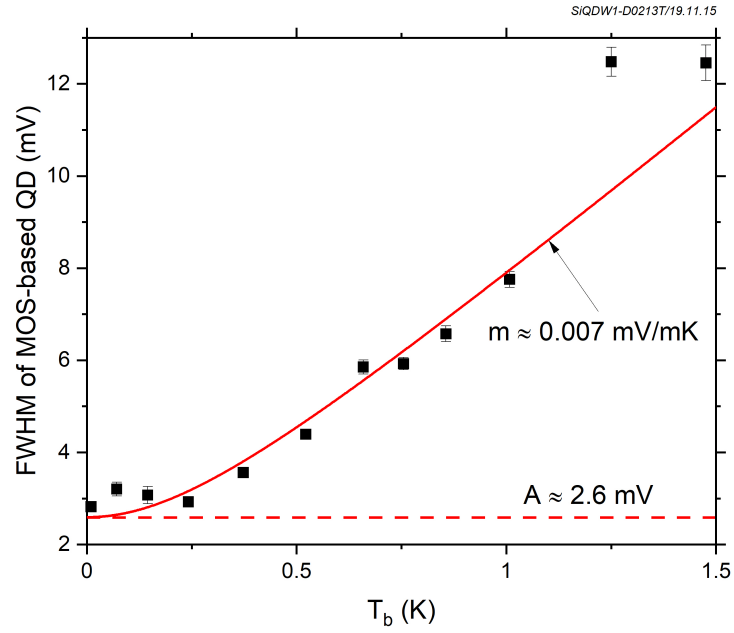
temperature than MOS-based dots, as we are still limited by the lead noise at low thermal temperature, and the intrinsic noise difference between the two quantum dot systems could be relatively small compared to our current extrinsic noises. The noise level was further mitigated later on MOS quantum dot separately, as shown in Chapter 4. Also, we found no obvious difference in the noise level after removing the low-pass filter PCB in the base temperature stage, probably due to its unstable noise filtering performance due to the resistance and capacitance change at cryogenic temperature.

5.4 Summary

To summarize, in this work we studied and analyzed noise sources in silicon quantum dot measurements. The noise level in a dilution refrigerator with ≈ 10 mK base temperature was substantially lowered from ≈ 4 K to ≈ 0.5 K by rearranging ground configuration and noise filtering. We made and tested low-pass filter PCB, comparing its performance change between room temperature and cryogenic temperature. No obvious suppression of noise was observed with the filter PCB, probably due to the unstable resistance and capacitance change at cryogenic temperature. By comparison of the noise level on two different quantum dot systems, P donor-based and MOS-based Si quantum dots, with the same measurement setup on the same platform, we were not able to measure the T_e difference caused by intrinsic noises, and distinguish between extrinsic noises and intrinsic noises, as we are still limited by the lead noise, and the intrinsic noise difference



(a)



(b)

Figure 5.13: (a) Temperature dependence of Coulomb blockade linewidth of P donor-based Si quantum dot device. (b) Temperature dependence of Coulomb blockade linewidth of MOS-based Si quantum dot device, with the same measurement setup.

between the two quantum dot systems could be relatively small compared to our current extrinsic noises.

Chapter 6: Can Plasma Oxidized Al/AlO_x/Al SETs Detect Charge Motion on Silicon MOS Quantum Dots?

In the work presented in Chapter 3, we achieved long-term charge offset stability (best $\Delta Q_0 = 0.13 \text{ e} \pm 0.01 \text{ e}$ over ≈ 7.6 days) by using plasma oxidized AlO_x as tunnel barriers in Al/AlO_x/Al SETs [54], which makes using the Al/AlO_x/Al SETs as charge sensors possible. And in Chapter 4, we achieved tuning controllable quantum dots and performing persistent charge sensing (SNR > 5) on single metal gate layer silicon MOS quantum dot devices [112], which is compatible to be integrated with Al/AlO_x/Al SETs. In Al/AlO_x/Al SET, the quantum dot is formed in the metal island. In MOS quantum dot devices, the quantum dot is formed in the Si substrate. A natural question is, can these two types of devices be integrated to form an integrated qubit platform for diagnostic purposes for both semiconducting and superconducting quantum computing, and have quantum dots in different planes for reflectometry? In this chapter, I will present the design and development of charge stable, plasma oxidized Al/AlO_x/Al SETs for use as charge sensors in single metal layer gated silicon MOS quantum dots, extending an integrated architecture that enables fabricating both devices simultaneously. The design of device and streamlined process flow will be presented, as well as the device modeling and simulation.

An analytical method is proposed to evaluate the device design for charge sensing and spin readout feasibility.

6.1 Introduction

Solid-state quantum computing devices are among the most promising candidates for the realization of quantum computation, because they can be well controlled, manipulated, and integrated. In Chapter 3 and Chapter 4, we have fabricated and characterized devices relating to two areas of solid-state quantum computing – Al/AlO_x/Al SET devices for superconducting quantum computing and Si MOS quantum dot devices for semiconducting quantum computing. For metallic Al/AlO_x/Al SET devices, the charge offset drift that precludes device integration for building high-fidelity quantum computer can be largely suppressed by applying plasma oxidation and UHV environment [54]. For Si MOS quantum dot devices, the fabrication complexity and failure modes can be reduced by employing single gate layer device structure, which also enables integration with other quantum architectures [112]. With these progress, and considering that superconducting SET charge sensors provide higher sensitivity [148, 149] and semiconducting MOS devices provide tunable smaller dots [77, 124], developing a hybrid architecture integrating these two types of devices and performing electron spin readout can be a promising approach for solid-state quantum computing.

There are a few prior studies on similar integrated structure. Sun et al. incorporated an Al/AlO_x/Al SET as the gate of a narrow MOS field-effect transistor

(FET), observed formation of Si MOS quantum dot and measured charge sensing signal on Al/ AlO_x /Al SET induced by the MOS dot and defect in the MOS channel [109, 150]. Jenei et al. studied the coupling between the Al/ AlO_x /Al SET and the 2DEG induced in MOS structure, and measured charge noise of the metallic SET detector [148, 151]. However, in these studies, the coupling and charge sensing between the two types of quantum dots were not deliberately controlled and electron spin readout for qubit implementation was not explored. Due to the AlO_x tunnel barriers, the total capacitance of the Al/ AlO_x /Al SET is usually four to five times larger than the total capacitance of the Si MOS quantum dot device, leading to an asymmetric capacitance structure. The charge change on one device induced by the charge change on the other device, is determined by the ratio of the coupling capacitance and the total capacitance of the other device [109]. Therefore, the charge sensing signal on the Si dot will be four to five times smaller than that on the Al dot and the Al/ AlO_x /Al SET is chosen to be the charge sensor in this integrated structure. Because of this asymmetric capacitance structure, the integrated device will need more careful design and analyses for optimizing qubit performance.

In this chapter, the design and development of charge stable, plasma oxidized Al/ AlO_x /Al SETs for use as charge sensors in single metal layer gated silicon MOS quantum dots will be presented and discussed. The reduced charge noise on Al/ AlO_x /Al SETs makes it possible to use these metallic SETs as charge sensors in qubit devices. The single gate layer structure of MOS quantum dots makes it possible to fabricate both devices simultaneously, since single gate layer doesn't require producing gate isolation layer and more deposition steps for multiple gate layers.

Modeling and calculation of charge sensing stability diagram for vertically and laterally aligned configurations will be presented. An analytical method for evaluating charge sensing and spin readout feasibility will be demonstrated. This integrated architecture is expected to be useful as a diagnostic qubit platform for simplifying the process flow, testing gate materials and tunnel barrier materials, and detecting oxide interface defects, etc.

6.2 Design of Device Fabrication

Here we integrate the fabrication process of double-angle deposited Al/ AlO_x /Al SETs and single gate layer MOS quantum dots to fabricate the two types of devices simultaneously. The designed process flows are described as follows. We start with 3" research grade intrinsic silicon wafers and there are 7 major steps.

- 1. Register alignment marks for alignment of multiple layers. Photolithography and deep Si etch are used to form etch marks on the Si wafer.
- 2. Implant ions to provide carriers for ohmic contacts of the MOS quantum dots. Photolithography and commercial ion implantation of ^{31}P are used for this step. Here we designed different styles of implantation regions to connect with photolithography defined layer (photo layer), or e-beam lithography defined layer (e-beam layer), or both, which will be discussed later.
- 3. Grow oxide (SiO_2) on the surface of Si wafer to provide gate isolation for Si MOS quantum dots, which can be done with furnace oxide growth and the oxide thickness can be controlled.

- 4. Define metal layer of large electrode fanout for both Al/ AlO_x /Al SETs and MOS quantum dots, which is the photo layer. This step consists of photolithography, e-beam metal deposition of 5nm Ti + 50 nm Au, and subsequent lift-off process. Here we want to keep the photo layer thin to insure good connection with the e-beam layer deposited in the next step.

- 5. Define metal layer of device fine structure for both Al/ AlO_x /Al SETs and MOS quantum dots, which is the e-beam layer. This step consists of e-beam lithography, double-angle deposition of 2 nm Co + 20 nm Al + plasma oxidation + 30 nm Al, and subsequent lift-off process. Note that using Al layer for fine structure is safe here, because the photo layer is previously formed, and we expose some portions of the photo layer in this step to make good electrical contact at the photo/e-beam junctions. Therefore, no part of the e-beam layer will be exposed to the photoresist developer. In addition, double-angle deposition ensures good photo/e-beam contact when the wire junctions are aligned with the deposition direction. These are why the e-beam layer comes after the photo layer.

- 6. Make ohmic contact pads for source and drain electrodes. This requires opening windows in SiO_2 by photolithography and etching over the implanted region, followed by e-beam metal deposition of 300 nm Al and subsequent lift-off process. Note that this step involves oxide etch, so that the metal deposition of ohmic contact pads cannot be incorporated into other metal deposition steps.

- 7. Thicken gate contact bond pads to protect the gate oxide underneath during wire bonding. This step consists of photolithography, e-beam metal deposition of 50 nm Ti + 800 nm Au, and subsequent lift-off process. The targeted total thickness of these gate contact pads is > 900 nm, which has been tested as sufficient to avoid oxide breakthrough [112].

In our single gate layer MOS quantum dot devices [112], the ion implanted regions are capacitively coupled with the photo layer of the inversion gate to connect to the source and drain electrodes, as shown in Fig. 6.1(a). The star-shaped, pink regions located underneath the source and drain contact pads (“TS”, “TD”, “BS”, “BD”) are the implanted regions. Other patterns represent the metal gate layout and contact pads. After the ion implantation, the whole Si wafer is oxidized to form the gate oxide layer before any metallization. The source and drain contact pads are metalized after etching the oxide in the pad region to form ohmic contacts. In this configuration, the induced inversion layer (2DEG) forms a long path across the device fine area and the photo/e-beam junctions. Any defects in the inversion gate in this area could induce defects in the inversion layer and may affect the device channel in the fine region. Here we propose a possible device design to mitigate this possible problem, which is to extend the implanted region to the device fine area and use the e-beam layer of the inversion gate to couple with the implanted region, as shown in the bottom half of Fig. 6.1(b). The implanted regions are extended to the device fine area through implant wires, and the e-beam layer of the inversion gate couples with the implant wire after the photo/e-beam junction, as shown in

the figure inset. This approach provides direct coupling to the inversion gate in the e-beam defined area and could improve the inversion layer induced in the device fine area. The validity of using implantation wires to extend the implanted regions to the device fine area by photolithography only has been verified by our group’s previous work [152], where photolithographically defined implant wires enable successful measurement of STM-patterned nanoscale devices. The minimum required separation between implant wires after the high temperature processing specified in Ref. [152] is $\leq 2 \mu\text{m}$ to keep electrical isolation. For the application in our Al/AlO_x/Al SET and MOS QD integrated devices, the device fine region (e-beam layer) is $\approx 40 \times 40 \mu\text{m}^2$ and the implant wires only reach the edges of the fine region so we are far beyond reaching the electrical isolation limit. Here for complete comparison for the analyses of measurement results, we add one design with the implanted regions coupled with both photo and e-beam layers, as shown in the top half of Fig. 6.1(b).

6.3 Device Modeling Results

6.3.1 Device Design and Capacitance Modeling

For the device design, here we present two basic configurations – lateral configuration and vertical configuration for the Al/AlO_x/Al SET and MOS QD integrated devices. Fig. 6.2(a) shows the lateral configuration, where we design an individual inversion gate (“Top gate”) for the MOS quantum dot, and three finger gates on one side to be used as plunger gate or barrier gate or both for the MOS quantum dot. The Al/AlO_x/Al SET is placed on the other side of the MOS quantum dot

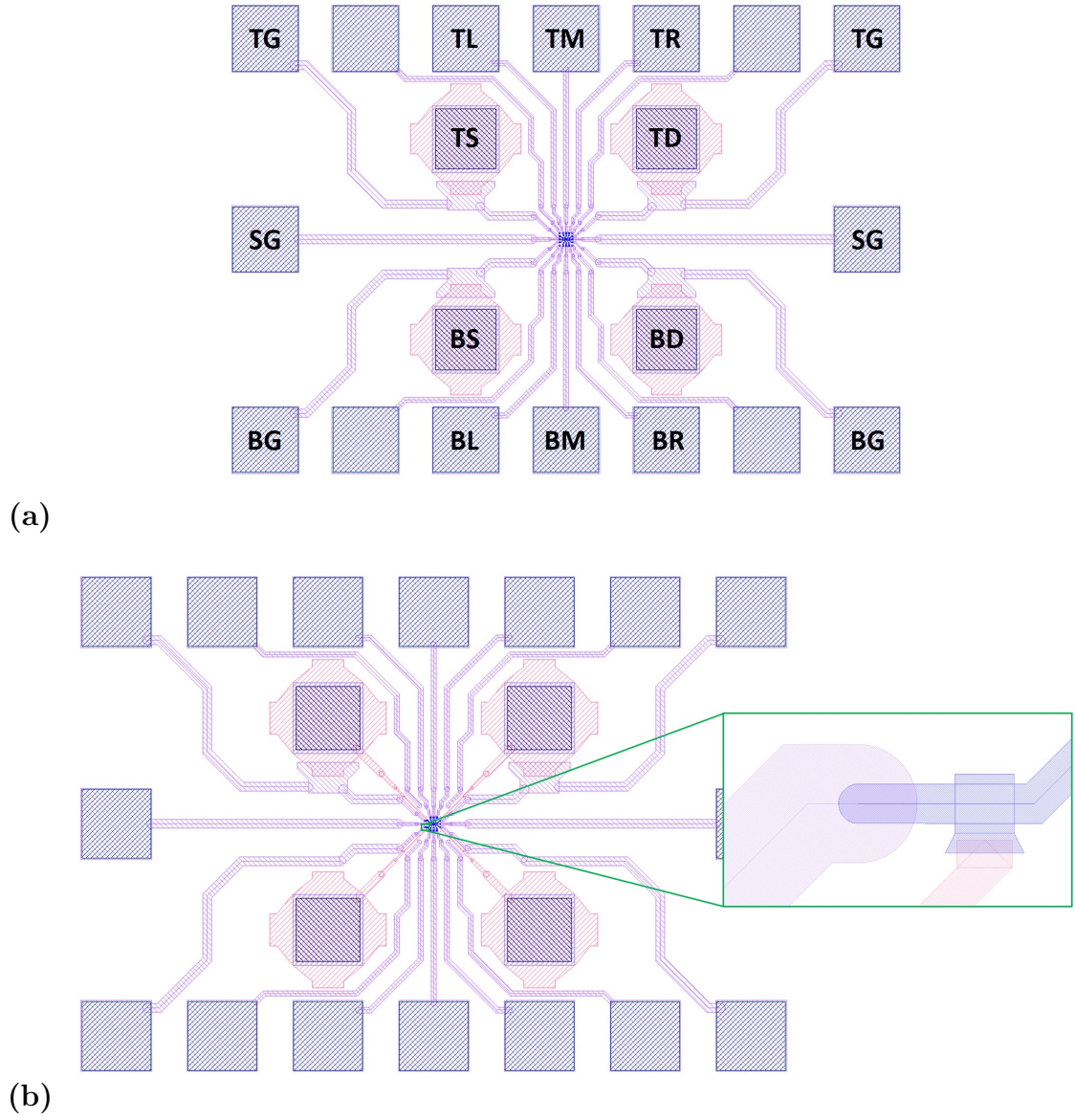


Figure 6.1: (a) Device layout of single gate layer MOS quantum dot devices, where the star-shaped, pink regions located underneath the source and drain contact pads ("TS", "TD", "BS", "BD") are the implanted regions. Other patterns represent the metal gate layout and contact pads. (b) Design of implantation wires in the Al/AlO_x/Al SET and MOS QD integrated devices.

device, with a side gate to control the electrostatic potential of the Al/AlO_x/Al SET island. The Al/AlO_x/Al SET island is coupled with the source and drain electrodes through AlO_x tunnel junctions. Here we use the “in-line” design for the Al/AlO_x/Al SET [54], as it makes room for placing the MOS device. Fig. 6.2(b) shows the vertical configuration, where we use the Al/AlO_x/Al SET to serve as the inversion gate for the MOS quantum dot, and there is no individual inversion gate. For the lateral configuration, the advantage is that the MOS quantum dot can be tuned separately, not depending on the Al/AlO_x/Al SET, therefore reducing the chance to blow up the AlO_x tunnel junctions during quantum dot tuning. Also the AlO_x tunnel junctions could induce some defects in the MOS channel. The disadvantage is the smaller coupling between the two devices, as the two devices are pulled away from each other. For the vertical configuration, the advantage is a larger coupling between the two devices, as they are only separated by a thin layer of SiO₂. The disadvantage is the difficulty to induce 2DEG using the Al/AlO_x/Al SET and the risk to blow up the AlO_x tunnel junctions.

To evaluate the charge sensing feasibility, we use FastCap software package to model the capacitances for the two configurations. Here we start with relatively relaxed designs, where the width of these wire electrodes is 100 nm, and the separation between gates is also 100 nm. The thickness of the metal electrodes is 50 nm, and the SiO₂ thickness is 25 nm. The thickness of the inversion layer used to model is 4 nm. The AlO_x tunnel junction size is 100 nm × 40 nm × 2 nm (length × width × thickness). Shown in Tables 6.1 and 6.2 are the FastCap modeled capacitance values for the lateral and vertical configurations, respectively. S(D) refers to

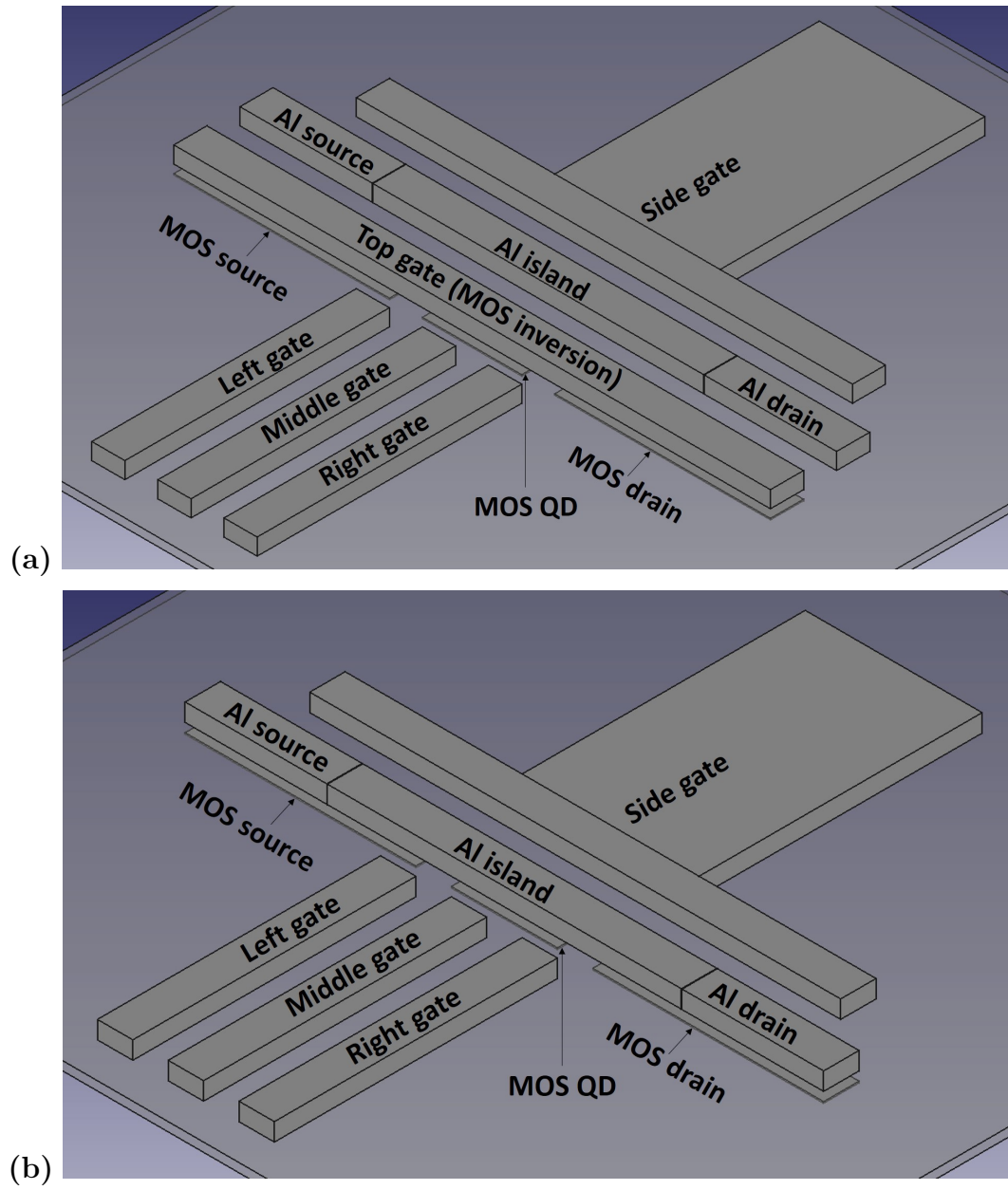


Figure 6.2: (a) Lateral configuration, where the Al/AIO_x/Al SET and the MOS quantum dot device are placed side by side. (b) Vertical configuration, where the Al/AIO_x/Al SET is used as the inversion gate of the MOS quantum dot device.

source (drain), and S(T/L/M/R)G refers to side (top/left/middle/right) gate. The Al/AlO_x/Al SET device is denoted by “Al”, and the Si MOS device is denoted by “Si”. Not shown in the tables is the coupling capacitance between the Al/AlO_x/Al SET island (dot) and the Si MOS quantum dot, which is 16.8 aF for the lateral configuration and 54.3 aF for the vertical configuration. These capacitance values will be used later in the charge sensing calculation to predict the charge stability diagram.

Cap (aF)	S (Al)	D (Al)	SG	S (Si)	D (Si)	TG	LG	MG	RG	C_{Σ}
Al dot	310	311	28.3	18.7	18.5	25	6.2	6.8	6.4	748
Si dot	3.8	4.1	16.9	16.5	16.3	57.4	8.6	10	8.4	159

Table 6.1: FastCap modeled capacitance values of the laterally configured Al/AlO_x/Al SET and MOS QD integrated device. Coupling capacitance between the Al/AlO_x/Al SET island (dot) and the Si MOS quantum dot is 16.8 aF.

Cap (aF)	S (Al)	D (Al)	SG	S (Si)	D (Si)	LG	MG	RG	C_{Σ}
Al dot	310	311	28.3	48.8	46.4	9.3	9.4	9.6	827
Si dot	4.1	4	24.7	16.5	16.3	8.6	10	8.4	147

Table 6.2: FastCap modeled capacitance values of the vertically configured Al/AlO_x/Al SET and MOS QD integrated device. Coupling capacitance between the Al/AlO_x/Al SET island (dot) and the Si MOS quantum dot is 54.3 aF.

6.3.2 Charge Stability Diagram Calculation

To calculate the shape of the charge stability diagram when the two types of devices are configured for charge sensing, here we model the integrated devices using the circuits presented in Fig. 6.3 [109]. Fig. 6.3(a) is the circuit diagram for the lateral configuration. N_{Al} and N_{Si} represent the number of electrons on

the Al/AlO_x/Al SET island and Si MOS quantum dot, respectively. The coupling capacitance between the dot of each device is denoted by C_c . The two dots are coupled to their own source and drain leads through two tunnel barriers. Due to the very small source-drain bias of each device, the two tunnel barrier capacitances for each device are simplified to a single capacitance – C_1 and C_2 as shown in the circuit diagram. The source and drain leads of each device are also capacitively coupled to the dot of the other device, represented by C_3 and C_4 . The side gate (“SG”), top gate (“TG”) and all finger gates are all capacitively coupled to each dot, as shown in the FastCap modeling result. In the modeled experimental setup, we sweep the voltages on the side gate (V_{SG}) and top gate (V_{TG}), and measure the movement of the conductance peaks of each device. V_{TG} will only vary above the threshold voltage to maintain the “on” state of the inversion layer. The finger gates will be biased at constant voltage to set up tunnel barriers. For the vertical configuration, the inversion layer of the Si MOS device will be induced by the Al/AlO_x/Al SET, where the voltages of the source and drain leads of the Al/AlO_x/Al SET will be set above the threshold voltage of the Si MOS device but their difference will be maintained at a small value, which is the bias of the Al/AlO_x/Al SET. For the vertical configuration, we sweep the voltages on the side gate (V_{SG}) and middle finger gate (V_{MG}), and measure the movement of the conductance peaks of each device. The left and right finger gates are set as barrier gates.

With the circuit model set up and under the assumption that the system can minimize its electrostatic energy automatically by independently adjusting the number of electrons on the two dots, the total electrostatic energy for the system in

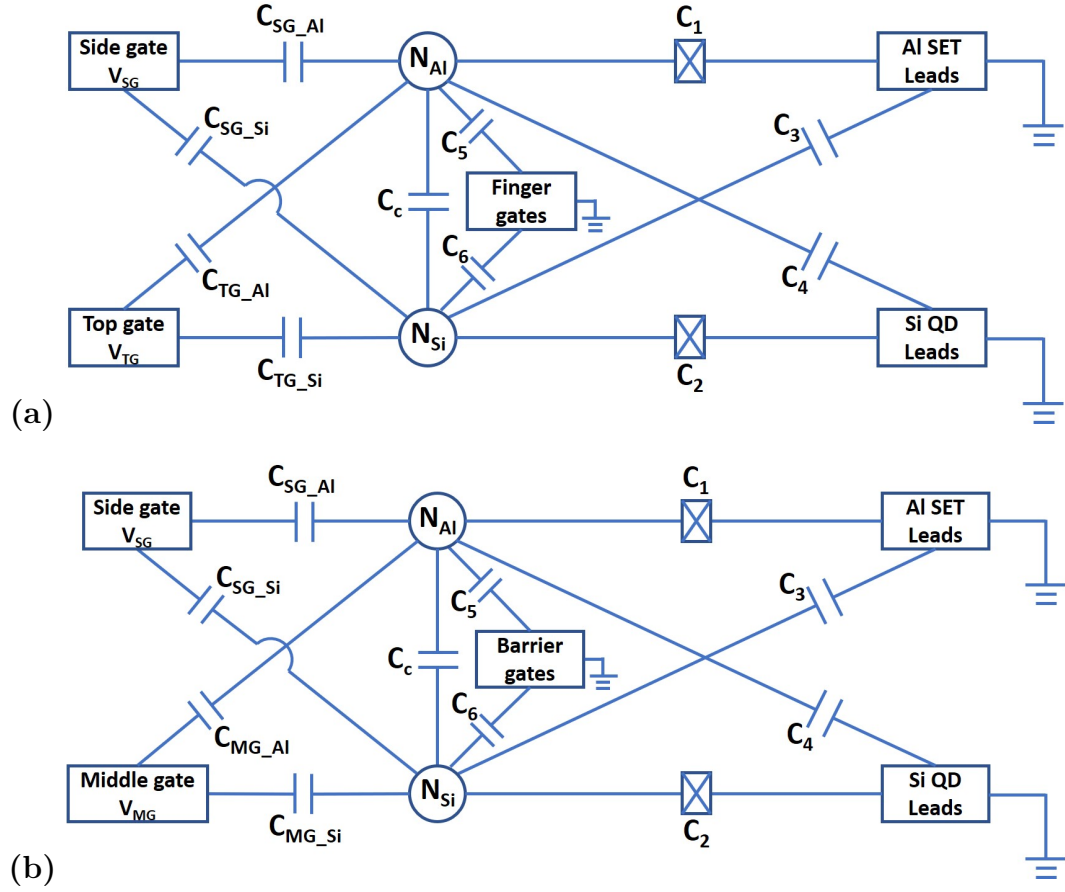


Figure 6.3: Circuit model for the Al/AIO_x/Al SET and Si MOS QD integrated device system. (a) Lateral configuration, where we sweep V_{SG} and V_{TG} , as shown on the left. (b) Vertical configuration, where we sweep V_{SG} and V_{MG} , as shown on the left.

the lateral configuration is given in matrix form by [109, 153]

$$E(N_{\text{Al}}, N_{\text{Si}}, V_{\text{SG}}, V_{\text{TG}}) = \frac{1}{2} Q^T \begin{pmatrix} C_{\Sigma\text{-Al}} & -C_c \\ -C_c & C_{\Sigma\text{-Si}} \end{pmatrix}^{-1} Q \quad (6.1)$$

where

$$C_{\Sigma\text{-Al}} = C_1 + C_3 + C_c + C_{\text{LG-Al}} + C_{\text{MG-Al}} + C_{\text{RG-Al}} + C_{\text{SG-Al}} + C_{\text{TG-Al}} \quad (6.2)$$

and

$$C_{\Sigma\text{-Si}} = C_2 + C_4 + C_c + C_{\text{LG-Si}} + C_{\text{MG-Si}} + C_{\text{RG-Si}} + C_{\text{SG-Si}} + C_{\text{TG-Si}} \quad (6.3)$$

are the total capacitance of the Al device and Si device, respectively.

$$Q = \begin{pmatrix} Q_{\Sigma\text{-Al}} \\ Q_{\Sigma\text{-Si}} \end{pmatrix} = \begin{pmatrix} -eN_{\text{Al}} + C_{\text{SG-Al}}V_{\text{SG}} + C_{\text{TG-Al}}V_{\text{TG}} \\ -eN_{\text{Si}} + C_{\text{SG-Si}}V_{\text{SG}} + C_{\text{TG-Si}}V_{\text{TG}} \end{pmatrix} \quad (6.4)$$

represents the total charges on the two dots. N_{Al} and N_{Si} represent the number of electrons on the Al dot and Si dot, respectively. They are constant values, not variables. By matrix operation, we get

$$E(N_{\text{Al}}, N_{\text{Si}}, V_{\text{SG}}, V_{\text{TG}}) = \frac{1}{2(C_{\Sigma\text{-Al}}C_{\Sigma\text{-Si}})} (Q_{\Sigma\text{-Al}}^2 C_{\Sigma\text{-Si}} + 2Q_{\Sigma\text{-Al}}Q_{\Sigma\text{-Si}}C_c + Q_{\Sigma\text{-Si}}^2 C_{\Sigma\text{-Al}}) \quad (6.5)$$

When $C_c = 0$, Eq. 6.5 reduces to

$$E(N_{\text{Al}}, N_{\text{Si}}, V_{\text{SG}}, V_{\text{TG}}) = \frac{Q_{\Sigma_{\text{Al}}}^2}{2C_{\Sigma_{\text{Al}}}} + \frac{Q_{\Sigma_{\text{Si}}}^2}{2C_{\Sigma_{\text{Si}}}} \quad (6.6)$$

This is the sum of the energies of two independent dots. For both devices, under energy degenerate conditions, Coulomb blockade is lifted, resulting in the maximal SET conductances. If we plot the maximal SET conductances of the two devices together to form a charge stability diagram, there are in total six such degeneracy conditions associated with adding or subtracting one electron from one dot, determined by $E(N_{\text{Al}}, N_{\text{Si}}, V_{\text{SG}}, V_{\text{TG}}) = E(N_{\text{Al}} + \delta N_{\text{Al}}, N_{\text{Si}} + \delta N_{\text{Si}}, V_{\text{SG}}, V_{\text{TG}})$ with $\delta N_{\text{Al}} = 0, \pm 1$, $\delta N_{\text{Si}} = 0, \pm 1$ and $|\delta N_{\text{Al}} + \delta N_{\text{Si}}| < 2$. The six equations determine six boundaries of the cell with $(N_{\text{Al}}, N_{\text{Si}})$ charge state: $(N_{\text{Al}} + 1, N_{\text{Si}})/(N_{\text{Al}}, N_{\text{Si}})$; $(N_{\text{Al}} - 1, N_{\text{Si}})/(N_{\text{Al}}, N_{\text{Si}})$; $(N_{\text{Al}}, N_{\text{Si}} + 1)/(N_{\text{Al}}, N_{\text{Si}})$; $(N_{\text{Al}}, N_{\text{Si}} - 1)/(N_{\text{Al}}, N_{\text{Si}})$; $(N_{\text{Al}} - 1, N_{\text{Si}} + 1)/(N_{\text{Al}}, N_{\text{Si}})$; and $(N_{\text{Al}} + 1, N_{\text{Si}} - 1)/(N_{\text{Al}}, N_{\text{Si}})$. Here we list the derived functions of the six boundaries of the $(N_{\text{Al}} = 0, N_{\text{Si}} = 0)$ cell as follows.

Boundary of $(N_{\text{Al}} = 1, N_{\text{Si}} = 0)/(N_{\text{Al}} = 0, N_{\text{Si}} = 0)$:

$$(C_{\Sigma_{\text{Si}}}C_{\text{SG}_{\text{Al}}} + C_cC_{\text{SG}_{\text{Si}}})V_{\text{SG}} + (C_{\Sigma_{\text{Si}}}C_{\text{TG}_{\text{Al}}} + C_cC_{\text{TG}_{\text{Si}}})V_{\text{TG}} - \frac{1}{2}eC_{\Sigma_{\text{Si}}} = 0 \quad (6.7)$$

Boundary of $(N_{\text{Al}} = -1, N_{\text{Si}} = 0)/(N_{\text{Al}} = 0, N_{\text{Si}} = 0)$:

$$(C_{\Sigma_{\text{Si}}}C_{\text{SG}_{\text{Al}}} + C_cC_{\text{SG}_{\text{Si}}})V_{\text{SG}} + (C_{\Sigma_{\text{Si}}}C_{\text{TG}_{\text{Al}}} + C_cC_{\text{TG}_{\text{Si}}})V_{\text{TG}} + \frac{1}{2}eC_{\Sigma_{\text{Si}}} = 0 \quad (6.8)$$

Boundary of $(N_{\text{Al}} = 0, N_{\text{Si}} = 1)/(N_{\text{Al}} = 0, N_{\text{Si}} = 0)$:

$$(C_{\Sigma\text{Al}}C_{\text{SG}\text{Si}} + C_cC_{\text{SG}\text{Al}})V_{\text{SG}} + (C_{\Sigma\text{Al}}C_{\text{TG}\text{Si}} + C_cC_{\text{TG}\text{Al}})V_{\text{TG}} - \frac{1}{2}eC_{\Sigma\text{Al}} = 0 \quad (6.9)$$

Boundary of $(N_{\text{Al}} = 0, N_{\text{Si}} = -1)/(N_{\text{Al}} = 0, N_{\text{Si}} = 0)$:

$$(C_{\Sigma\text{Al}}C_{\text{SG}\text{Si}} + C_cC_{\text{SG}\text{Al}})V_{\text{SG}} + (C_{\Sigma\text{Al}}C_{\text{TG}\text{Si}} + C_cC_{\text{TG}\text{Al}})V_{\text{TG}} + \frac{1}{2}eC_{\Sigma\text{Al}} = 0 \quad (6.10)$$

Boundary of $(N_{\text{Al}} = -1, N_{\text{Si}} = 1)/(N_{\text{Al}} = 0, N_{\text{Si}} = 0)$:

$$\begin{aligned} & [(C_{\Sigma\text{Al}}C_{\text{SG}\text{Si}} + C_cC_{\text{SG}\text{Al}}) - (C_{\Sigma\text{Si}}C_{\text{SG}\text{Al}} + C_cC_{\text{SG}\text{Si}})]V_{\text{SG}} \\ & + [(C_{\Sigma\text{Al}}C_{\text{TG}\text{Si}} + C_cC_{\text{TG}\text{Al}}) - (C_{\Sigma\text{Si}}C_{\text{TG}\text{Al}} + C_cC_{\text{TG}\text{Si}})]V_{\text{TG}} \\ & - \frac{1}{2}e(C_{\Sigma\text{Al}} + C_{\Sigma\text{Si}} - 2C_c) = 0 \end{aligned} \quad (6.11)$$

Boundary of $(N_{\text{Al}} = 1, N_{\text{Si}} = -1)/(N_{\text{Al}} = 0, N_{\text{Si}} = 0)$:

$$\begin{aligned} & [(C_{\Sigma\text{Al}}C_{\text{SG}\text{Si}} + C_cC_{\text{SG}\text{Al}}) - (C_{\Sigma\text{Si}}C_{\text{SG}\text{Al}} + C_cC_{\text{SG}\text{Si}})]V_{\text{SG}} \\ & + [(C_{\Sigma\text{Al}}C_{\text{TG}\text{Si}} + C_cC_{\text{TG}\text{Al}}) - (C_{\Sigma\text{Si}}C_{\text{TG}\text{Al}} + C_cC_{\text{TG}\text{Si}})]V_{\text{TG}} \\ & + \frac{1}{2}e(C_{\Sigma\text{Al}} + C_{\Sigma\text{Si}} - 2C_c) = 0 \end{aligned} \quad (6.12)$$

Using these six boundary functions to determine the center cell with the charge state of $(N_{\text{Al}}, N_{\text{Si}}) = (0, 0)$, we can construct the charge stability diagram with the FastCap modeled capacitance values. Shown in Fig. 6.4(a) left panel is the plotted charge stability diagram of the lateral configuration shown in Fig. 6.2(a). The right panel shows the zoom in view of the boxed region in the left panel, which reveals

the details of the triple points. The coupling between the two devices causes breaks in the charge transition lines of both devices, and produces boundary between (0,0) and (1,-1) charge states. The shifts on charge transition lines of Al dot and Si dot are determined by $C_c/C_{\Sigma_Si} \approx 0.11$ and $C_c/C_{\Sigma_Al} \approx 0.02$, respectively. Due to the total capacitance difference of the two dots, the charge transition line shifts are more obvious on the Al dot than on the Si dot. The assumption of this modeling is that the system always stays at the lowest energy of a particular charge state. Therefore, to further validate the charge stability diagram constructed by the boundary functions, we plot the nine energy surfaces $E(N_{Al}, N_{Si}, V_{SG}, V_{TG})$ shown in Fig. 6.4(a) vs V_{TG} and V_{SG} , as shown in Fig. 6.4(b) left panel, and view from the bottom of the plot box to find out the lowest energy surfaces in each region, as shown in Fig. 6.4(b) right panel. Not shown in the figures are the energy surfaces of outer cells with $|\delta N_{Al} + \delta N_{Si}| \geq 2$, which define the outer boundaries of the nine plotted cells. The consistency with the energy surface constructed stability diagram validates the boundary constructed stability diagram in Fig. 6.4(a) left panel.

Similarly, in the vertical configuration shown in Fig. 6.2(b), the total electrostatic energy is given by

$$E(N_{Al}, N_{Si}, V_{SG}, V_{MG}) = \frac{1}{2(C_{\Sigma_Al}C_{\Sigma_Si})}(Q_{\Sigma_Al}^2C_{\Sigma_Si} + 2Q_{\Sigma_Al}Q_{\Sigma_Si}C_c + Q_{\Sigma_Si}^2C_{\Sigma_Al}) \quad (6.13)$$

Here we sweep V_{SG} and V_{MG} in the modeled experimental setup.

$$C_{\Sigma_Al} = C_1 + C_3 + C_c + C_{LG_Al} + C_{MG_Al} + C_{RG_Al} + C_{SG_Al} \quad (6.14)$$

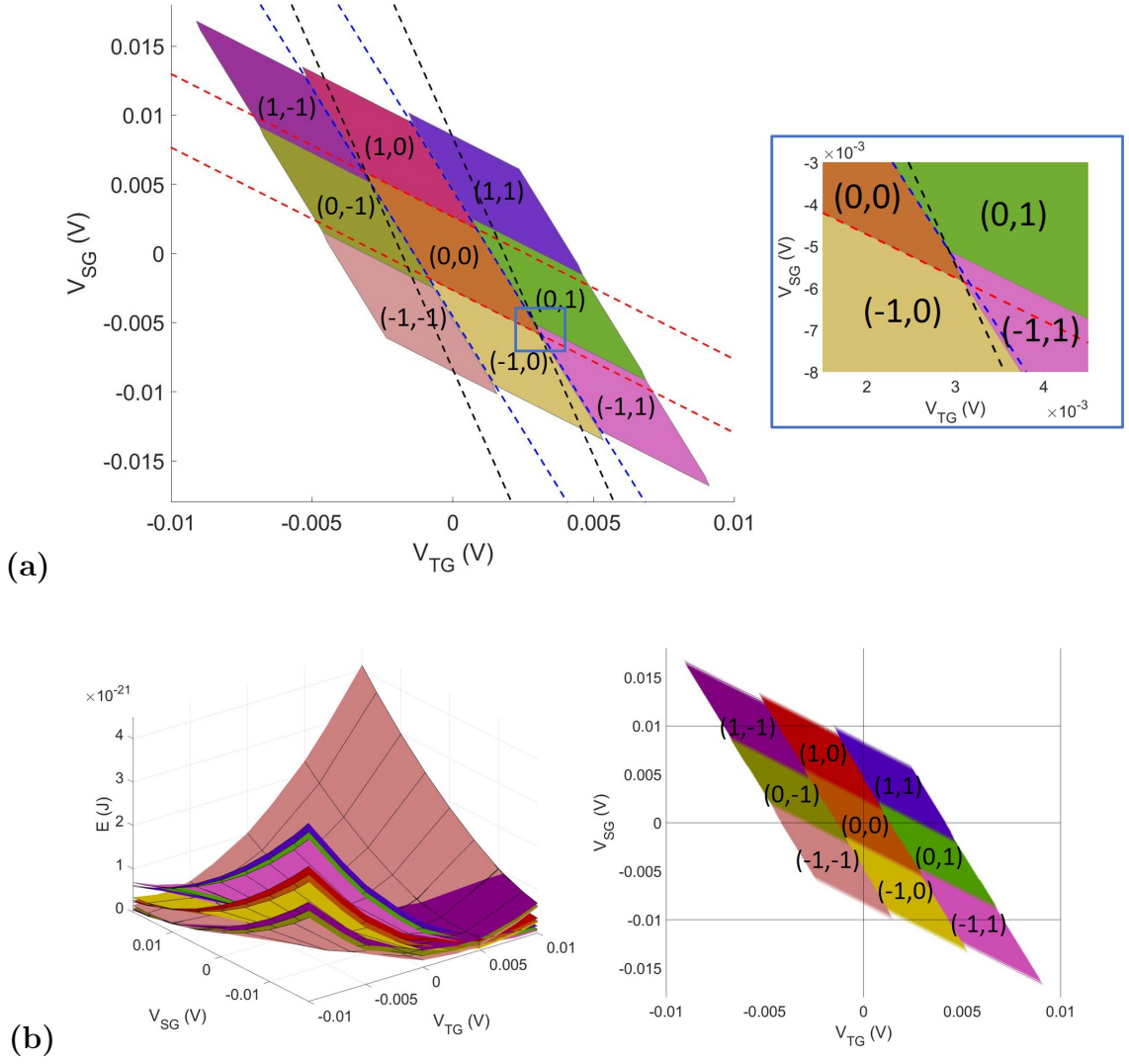


Figure 6.4: Modeled charge stability diagram for lateral configuration shown in Fig. 6.2(a). (a) Left panel: charge stability diagram constructed by six boundary functions, given in Eqs. 6.7, 6.8, 6.9, 6.10, 6.11, 6.12. Right panel: zoom in view of the boxed region in the left panel, which reveals the details of the triple points. (b) Left panel: nine energy surfaces $E(N_{Al}, N_{Si}, V_{SG}, V_{TG})$ shown in (a) vs V_{TG} and V_{SG} . Right panel: view from the bottom of the plot box in left panel showing the lowest energy surfaces in each region.

$$C_{\Sigma, \text{Si}} = C_2 + C_4 + C_c + C_{\text{LG}, \text{Si}} + C_{\text{MG}, \text{Si}} + C_{\text{RG}, \text{Si}} + C_{\text{SG}, \text{Si}} \quad (6.15)$$

and

$$Q = \begin{pmatrix} Q_{\Sigma, \text{Al}} \\ Q_{\Sigma, \text{Si}} \end{pmatrix} = \begin{pmatrix} -eN_{\text{Al}} + C_{\text{SG}, \text{Al}}V_{\text{SG}} + C_{\text{MG}, \text{Al}}V_{\text{MG}} \\ -eN_{\text{Si}} + C_{\text{SG}, \text{Si}}V_{\text{SG}} + C_{\text{MG}, \text{Si}}V_{\text{MG}} \end{pmatrix} \quad (6.16)$$

Again, we can get six boundary functions of the center cell and construct the stability diagram as shown in Fig. 6.5. We note that these charge stable regions are very narrow and hard to be distinguished. This is because the gate capacitance ratios of the two dots to the two swept gates in this configuration are too close to each other, resulting in the very similar charging line slopes of the Al dot and Si dot. With this kind of stability diagram, it could be difficult to find a suitable region to perform charge sensing experiment. The method for evaluating charge sensing feasibility will be discussed in Section 6.4.

6.4 Discussion and Summary

Now we discuss how to evaluate the feasibility of charge sensing and electron spin readout of these integrated devices using the modeled stability diagram. To perform charge sensing, we will monitor the conductance or current change on the Al/AlO_x/Al SET charge sensor induced by a charge transition on the MOS quantum dot. One approach to measure is to follow the trace of the conductance or current peak denoted by the red dotted line in Fig. 6.4(a) right panel. Ideally, the current measured on the boundary between (0,0) and (-1,0) charge regions is maximum and stable since the Al/AlO_x/Al SET island is configured in the electron tunneling

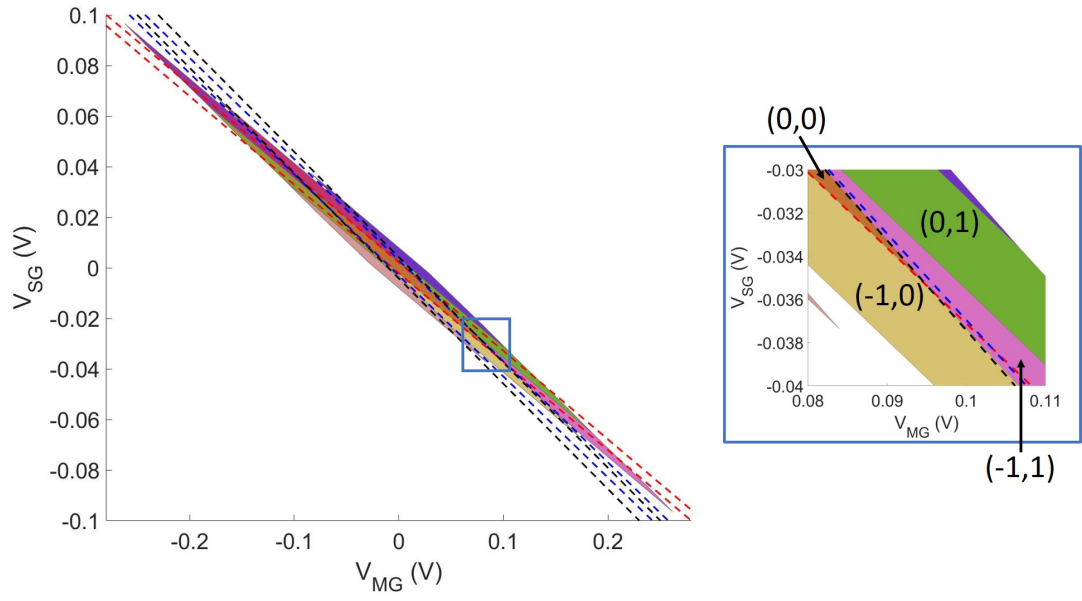


Figure 6.5: Modeled charge stability diagram for vertical configuration shown in Fig. 6.2(b). Left panel: charge stability diagram constructed by six boundary functions. Right panel: zoom in view of the boxed region in the left panel, which reveals the details of the triple points.

regime and the electron number on the MOS quantum dot is constant. If we keep the V_{SG} vs V_{TG} ratio and increase V_{TG} along the direction denoted by the red dotted line, when V_{TG} increases to ≈ 3.1 mV, we will encounter a charging event on the MOS quantum dot when the electron number on the MOS dot increases from 0 to 1, which will shift the Coulomb peak of the Al/AlO_x/Al SET sensor and cause the charge state on the Al/AlO_x/Al SET island to change from the electron tunneling regime to the Coulomb blockade regime. For the measurement, we should measure a current drop on the Al/AlO_x/Al SET sensor, which is only induced by the charging event on the MOS quantum dot. In the ideal case, by monitoring the Al/AlO_x/Al SET current change from maximum to zero, we can sense a charge transition on the MOS quantum dot.

In the real experiment, whether this current change on the Al/AlO_x/Al SET can be measured and resolved, and in which range to operate the measurement is more complicated and depends on the electron temperature, measurement noise, etc. Here we take the stability diagram of 100 nm lateral configuration in Fig. 6.4(a) right panel as an example to provide an analytical method to evaluate the feasibility of charge sensing and further spin readout. For the charge sensing experiment, we need to measure the current on the Al/AlO_x/Al SET sensor so here we simulate the current map of the SET sensor in the region of this stability diagram. In the real measurement, the electron temperature can cause noise broadening on the Coulomb oscillation current peak of the SET sensor and the charge transition width of the target MOS quantum dot. The source-drain bias can also broaden the Coulomb peak of the SET sensor. It is natural to assume that the lowest bias and the

corresponding minimum peak broadening would be optimal to obtain a sensing signal as this condition gives the minimum overlap between the current peak before and after the charge transition on the target dot.

The SET current model we used in previous chapters (Chapters 3, 4, 5) [35, 99, 100] only applies to small source-drain bias, V_{sd} . However, for this simulation the Coulomb peak broadening due to the source-drain bias of the SET sensor should be incorporated to find out the optimal operation range for optimal sensing signal. Here for the current simulation of the SET sensor, we use an analytical model based on the “orthodox” theory and the steady-state master equation [154, 155] that is valid over a wide source-drain bias for $|V_{sd}| \leq e/C_{\Sigma\text{-Al}}$. The SET current-voltage characteristics when the electron number on its island jumps between n and $n + 1$ is given by:

$$I_{\text{SET}} = \frac{e}{2R_{\Sigma\text{-Al}}C_{\Sigma\text{-Al}}} \frac{(\tilde{V}_{\text{SG}}^2 - \tilde{V}_{sd}^2) \sinh(\tilde{V}_{sd}/\tilde{T}_e)}{\tilde{V}_{\text{SG}} \sinh(\tilde{V}_{\text{SG}}/\tilde{T}_e) - \tilde{V}_{sd} \sinh(\tilde{V}_{sd}/\tilde{T}_e)} \quad (6.17)$$

where

$$\tilde{V}_{\text{SG}} = \frac{2C_{\text{SG-Al}}(V_{\text{SG}} - V_{\text{SG-c}})}{e} - \frac{C_{\text{SG-Al}}V_{sd}}{e} - 2n \quad (6.18)$$

$$\tilde{V}_{sd} = \frac{C_{\Sigma\text{-Al}}V_{sd}}{e} \quad (6.19)$$

$$\tilde{T}_e = \frac{2k_B T_e C_{\Sigma\text{-Al}}}{e^2} \quad (6.20)$$

Here, $R_{\Sigma\text{-Al}}$ is the total resistance of the Al/ AlO_x /Al SET, $V_{\text{SG-c}}$ is the Coulomb peak center along the V_{SG} direction. For the parameters, we estimate $T_e = 100$ mK from previous evaluation [112] of our measurement system shown in

Section 2.3.1, $R_{\Sigma_Al} = 120 \text{ M}\Omega$ from our previously measured plasma oxidized Al/AlO_x/Al SET devices [54]. FastCap modeled results for this integrated device are used for the capacitance values. Here we start with $V_{sd} = 100 \text{ }\mu\text{V}$, which is about half of the Coulomb diamond top ($e/C_{\Sigma_Al} \approx 214 \text{ }\mu\text{V}$). Using this analytical SET model, current maps of the SET sensor without and with the shift caused by a charge transition event occurs on the MOS quantum dot are plotted in Fig. 6.6(a) and (d), respectively. The arrows denote the difference in the peak center positions for the two regimes. The current is the summation of the center Coulomb peak and two adjacent Coulomb peaks.

The noise broadening on the charge transition width of the MOS quantum dot is adapted from a conductance model [130, 156]:

$$P_e = \frac{1}{2} \pm \frac{1}{2} \tanh \left(\frac{\alpha e V_{TG}}{2 k_B T_e} \right) \quad (6.21)$$

where P_e is the probability of finding an excess electron on the MOS quantum dot, and $\alpha = \frac{C_{TG_Si}}{C_{\Sigma_Si}}$ is the lever arm of the sweeping gate. With the electron temperature assumed above and capacitance values from FastCap modeling, the probabilities of the SET current maps in Fig. 6.6(a) and (d) are plotted in Fig. 6.6(b) and (e), respectively, incorporating the charge transition width broadening due to the electron temperature. By multiplying the SET current and probability in the two regimes – $N_{Si} = 0$ and $N_{Si} = 1$, we obtain the SET current map with charge transition broadening as shown in Fig. 6.6(c) and (f). Summing up the SET current in the two regimes before and after the charge transition on the MOS quantum dot, the

simulated measurement of SET sensor's current is shown in Fig. 6.7, incorporating noise broadening on both sensor dot's Coulomb peak and target dot's charge transition.

With the simulated charge sensing signal shown in Fig. 6.7, the next step is to evaluate the device's feasibility of performing spin readout. To read out an electron spin, a magnetic field B is required to split the energies of the spin-up state and spin-down state by Zeeman splitting $E_Z = g\mu_B B$, as detailed in Section 1.3. Therefore, we need to simulate the charge sensing signals for spin-up and spin-down electrons respectively with an applied magnetic field, to see if a signal difference on the sensor dot can be measured to distinguish the spin state of a loaded electron on the target dot. For spin up (down) electrons, the charge state boundaries of the Si dot are shifted by adding $E = \frac{1}{2}\mu_B B$ ($E = -\frac{1}{2}\mu_B B$) to the energy surfaces where the MOS quantum dot is getting or losing an electron. By calculation, the charge stability diagrams with an applied field $B = 2$ T can be plotted for spin-up and spin-down electrons respectively, as shown in Fig. 6.8(a) and (b). The arrows denote the different charge transition positions for the two regimes. The corresponding SET sensor current maps are shown in Fig. 6.8(c) and (d). To perform the spin readout measurement, we find the optimal operating voltage trace by looking at the signal difference between spin-up and spin-down states as shown in Fig. 6.8(e) and finding the trace of the maximum contrast as denoted by the blue dashed line. This optimal operating voltage trace has a shift ΔV_{SG} along V_{SG} direction from the current peak trace that gives the maximum current drop due to charge sensing in the absence of the magnetic field, i.e., the charge state boundary extension of the

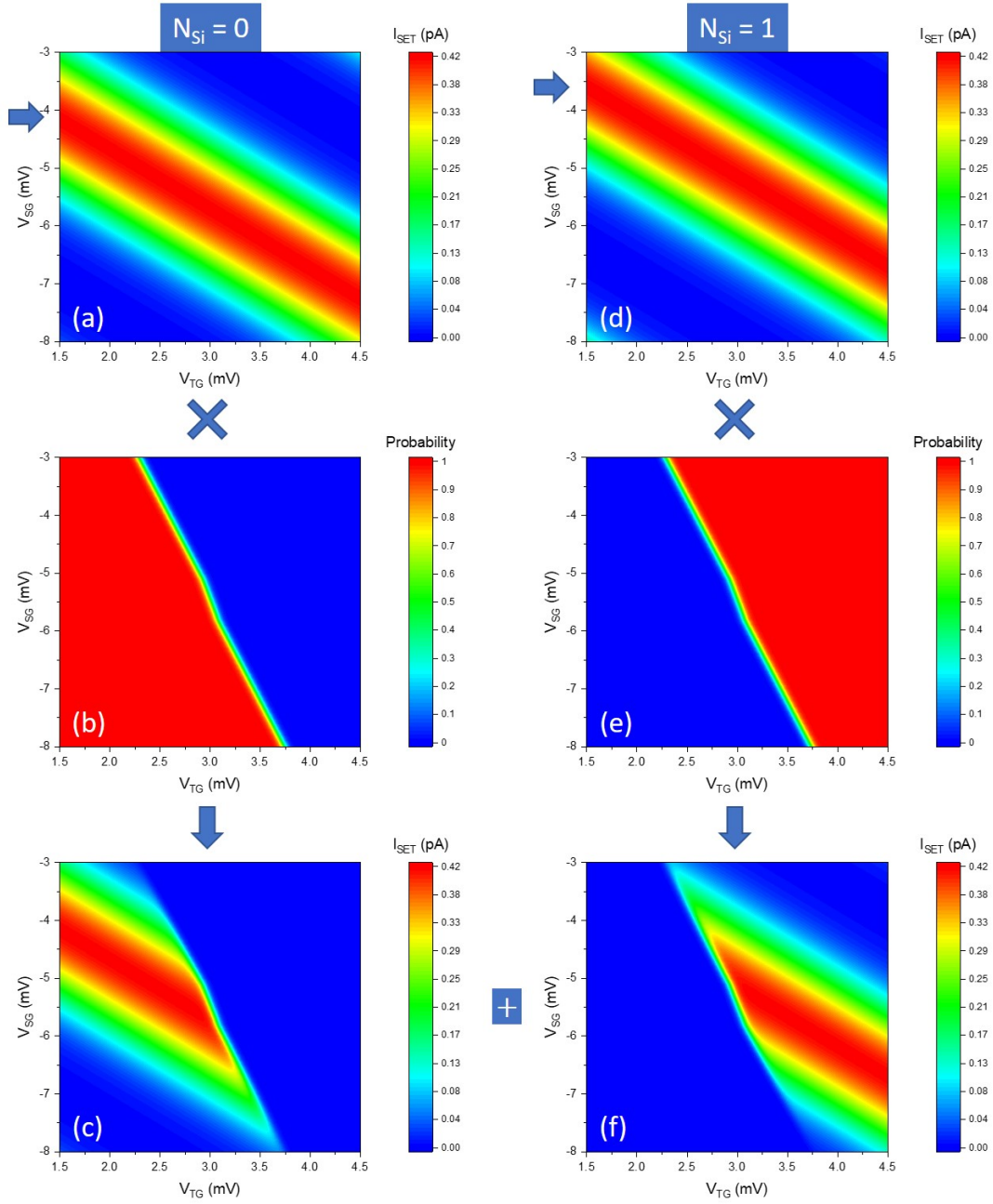


Figure 6.6: (a) and (d): current maps of the SET sensor without and with the shift caused by a charge transition event occurs on the MOS quantum dot. (b) and (e): probabilities of the SET current maps (a) and (b), respectively, incorporating the charge transition width broadening. (c) and (f): SET current map with charge transition broadening for $N_{\text{Si}} = 0$ and $N_{\text{Si}} = 1$.

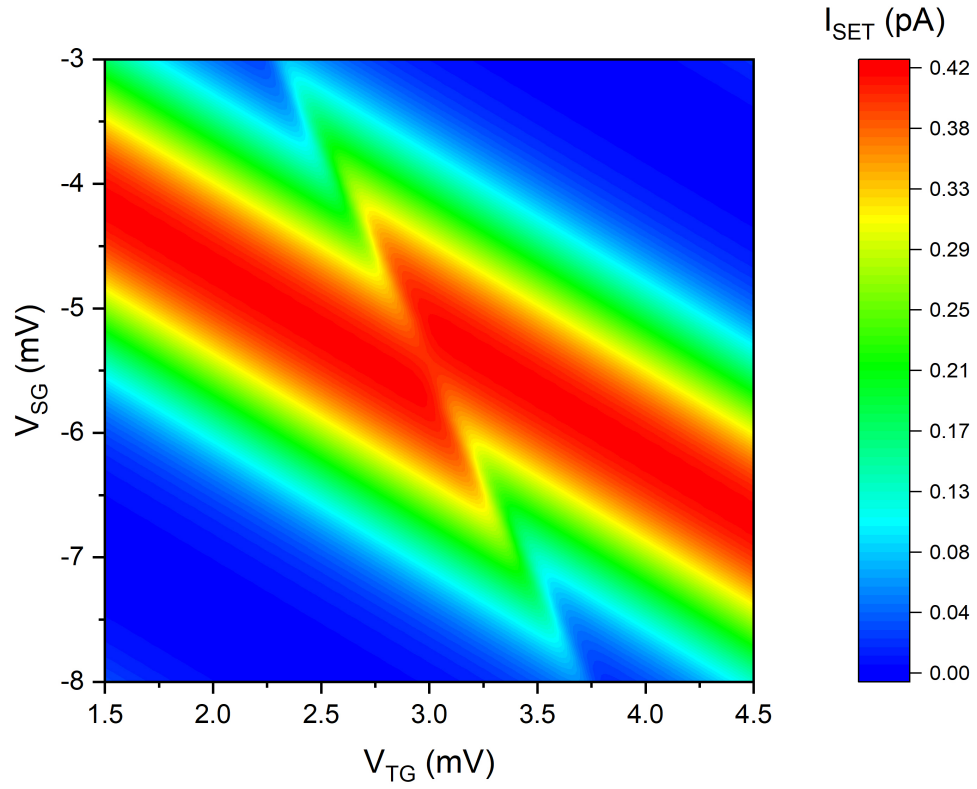


Figure 6.7: Simulated SET charge sensor current using the simulation process shown in Fig. 6.6, incorporating noise broadening on both sensor dot's Coulomb peak and target dot's charge transition. $T_e = 100$ mK and $V_{sd} = 100$ μ V.

Al dot, as denoted by the red dotted line. The SET sensor signal along the optimal operating trace for spin-up and spin-down states are plotted in Fig. 6.8(f). For the measurement, V_{TG} is first pulsed from the zero electron configuration ($V_{TG} = 2.5$ mV can be a good choice) to one electron configuration ($V_{TG} = 4.25$ mV can be a good choice) for loading an electron in an unknown spin state onto the MOS quantum dot. Then, within the spin lifetime ($T_1 \sim 1$ s [30, 119]) before the spin decays, V_{TG} is pulsed back to a position that demonstrates different signals for different spin states. $V_{TG} = 3.4$ mV can be a good choice, where spin-up results in high current level and spin-down results in low-level current.

So far, we haven't included the measurement noise yet. However, whether the sensing signal can be recognized also depends on the measurement noise level. Here we define the SET sensor current difference between a spin-up electron and a spin-down electron (as shown in Fig. 6.8(e) and (f)) as our signal. Assuming a measurement noise of ± 0.05 pA (standard deviation), the signal in Fig. 6.8(e) and (f) mixed with measurement noise are plotted in Fig. 6.9(a) and (b), which indicates the signal-to-noise ratio (SNR) of approximately 3 (pA/pA)² at $V_{sd} = 100$ μ V. Again, in Fig. 6.9(b), the red dotted line denotes the charge state boundary extension of the Al dot, and ΔV_{SG} denotes the shift of the optimal operating voltage trace along the V_{SG} direction. Here we define $SNR = (A_{\text{signal}}/A_{\text{noise}})^2$, where A_{signal} (A_{noise}) is the signal (noise) amplitude. Using this approach, we can then calculate SNR for a wide source-drain bias range and find out the optimal operation range of the SET charge sensor. From the SNR vs V_{sd} data shown in Fig. 6.9(c), 70 μ V $\leq V_{sd} \leq 240$ μ V is a feasible bias range with $SNR \geq 2$ [81] for resolving the signal

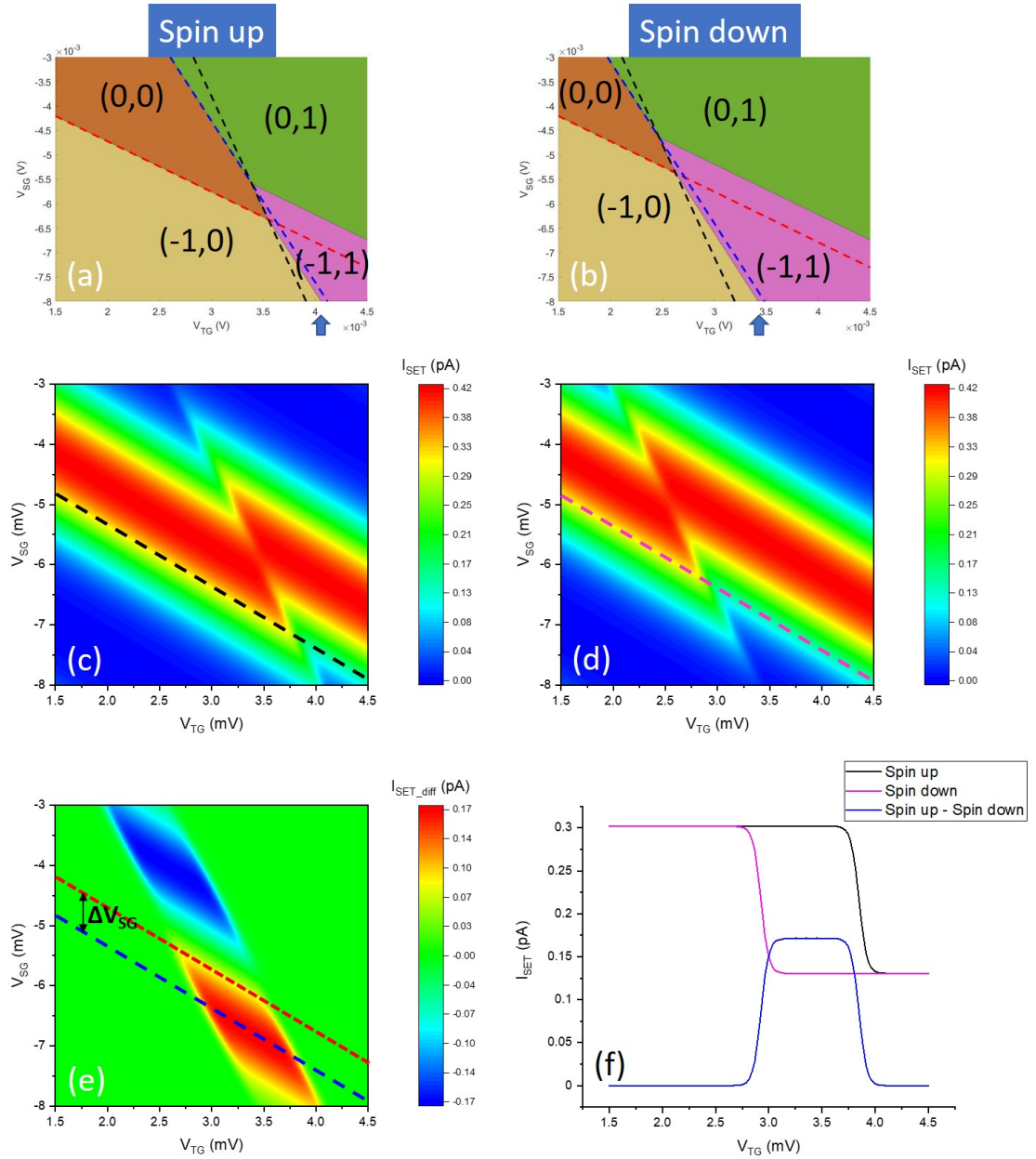


Figure 6.8: Charge sensing simulation with an applied magnetic field $B = 2$ T. (a) and (b): charge stability diagrams for spin-up and spin-down electrons, respectively. (c) and (d): SET sensor current maps for spin-up and spin-down electrons, respectively. (e) SET sensor signal difference between spin-up and spin-down states. (f) SET sensor signal along measurement traces denoted by dashed lines in (c), (d) and (e).

from the background noise. For optimal measurement signal, the SET sensor should be operated at $V_{sd} \approx 175 \mu\text{V}$, which is not the lowest bias that gives the narrowest peak width and minimum overlap between the current peaks before and after the charge transition on the target dot. ΔV_{SG} vs V_{sd} is also plotted in Fig. 6.9(c), indicating the change of the optimal operating position with V_{sd} .

The reason that the signal first increases and then decreases with increasing V_{sd} can be explained in Fig. 6.10. Shown in Fig. 6.10(a) are the simulated Coulomb diamonds using Eq. 6.17 for the SET charge sensor with our electron temperature assumption $T_e = 100 \text{ mK}$. For a single Coulomb peak, higher V_{sd} leads to higher SET current. But as V_{sd} increases, the individual Coulomb peak is also broadened and adjacent peaks merge together, as detailed in Section 1.1 and shown in Fig. 6.10(b). The Coulomb blockade is lifted as V_{sd} increases, raising the SET current minimum. Therefore, the SET current amplitude not monotonically increases with increasing V_{sd} but depends on the competition between the current maximum and minimum. The peak and valley values of the SET current at different V_{sd} values are plotted in Fig. 6.10(c). The peak value increases linearly with V_{sd} , showing an ohmic characteristic. The Coulomb blockade is lifted when V_{sd} exceeds approximately $150 \mu\text{V}$ and the valley value begins to increase faster than the peak value. The SET signal strength is therefore the current difference between the peak and the valley, i.e., the peak-valley amplitude. As shown in Fig. 6.10(c), the SET signal first increases and then decreases with increasing V_{sd} and reaches its maximum at approximately $V_{sd} \approx 175 \mu\text{V}$, consistent with the result obtained from sensing signal. Therefore, it looks like the operating range of the SET sensor is limited by

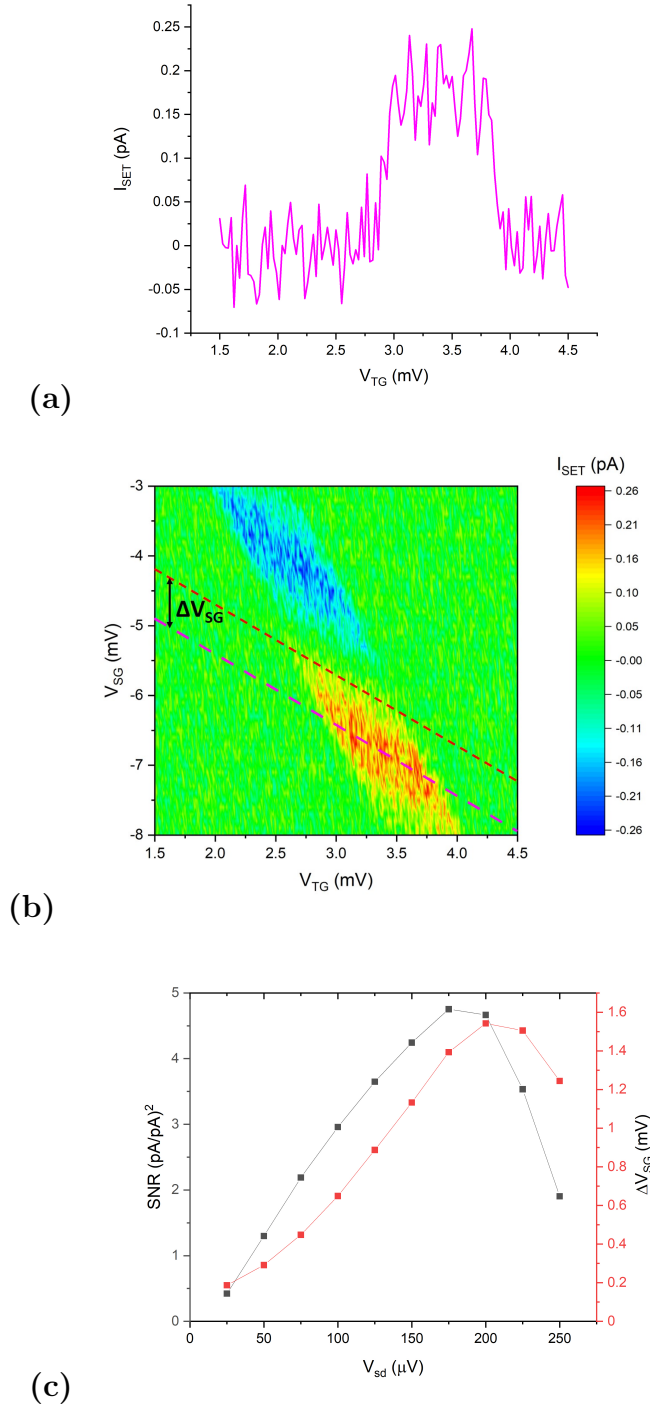


Figure 6.9: Electron spin readout signal mixed with measurement noise of ± 0.05 pA (standard deviation). (a) SET sensor signal along the measurement trace denoted by the dashed line in (b) SET sensor signal map including measurement noise of ± 0.05 pA at $V_{\text{sd}} = 100$ μV . (c) Calculated SNR and ΔV_{SG} for a wide range of V_{sd} .

the diamond size, i.e., the charging energy. To verify this guess, we reduce the total capacitance of the SET sensor, $C_{\Sigma Al}$, by a factor of 2, which results in 2 times larger charging energy and Coulomb diamonds, and obtain the SNR vs V_{sd} using the same method. In Fig. 6.11, we compare the SNR vs V_{sd} of the modified device with SET sensor having 2 times larger charging energy (diamonds) with the original one. It is observed that the SNR is largely increased in a wider V_{sd} range and the optimal operating point of the SET sensor is $V_{sd} \approx 400 \mu\text{V}$. This indicates one direction to feedback the device design for better measurement signal – reduce $C_{\Sigma Al}$, i.e., increase the SET sensor’s charging energy.

Overall, the whole process illustrates an analytical method to evaluate the feasibility of performing charge sensing on these integrated devices and can be used to find out the optimal operating range for the SET charge sensor which is not the condition that gives the narrowest Coulomb peak. Using the simulation results, the device design can therefore be improved to optimize the measurement signal with a more realistically calibrated measurement noise. This analytical method is not limited to the specific device structure presented here, but can be used in versatile charge sensing and spin qubit scenarios.

To summarize, we propose a new device design for integrating our charge offset drift mitigated metallic SET devices [54] with streamlined, robust single metal gate layer MOS quantum dot devices [112] to form a hybrid quantum computing device, using the metallic SET as the charge sensor. This device architecture can be used to provide more choices of qubit diagnostics for both semiconducting and superconducting quantum computing devices. By using capacitance modeling and

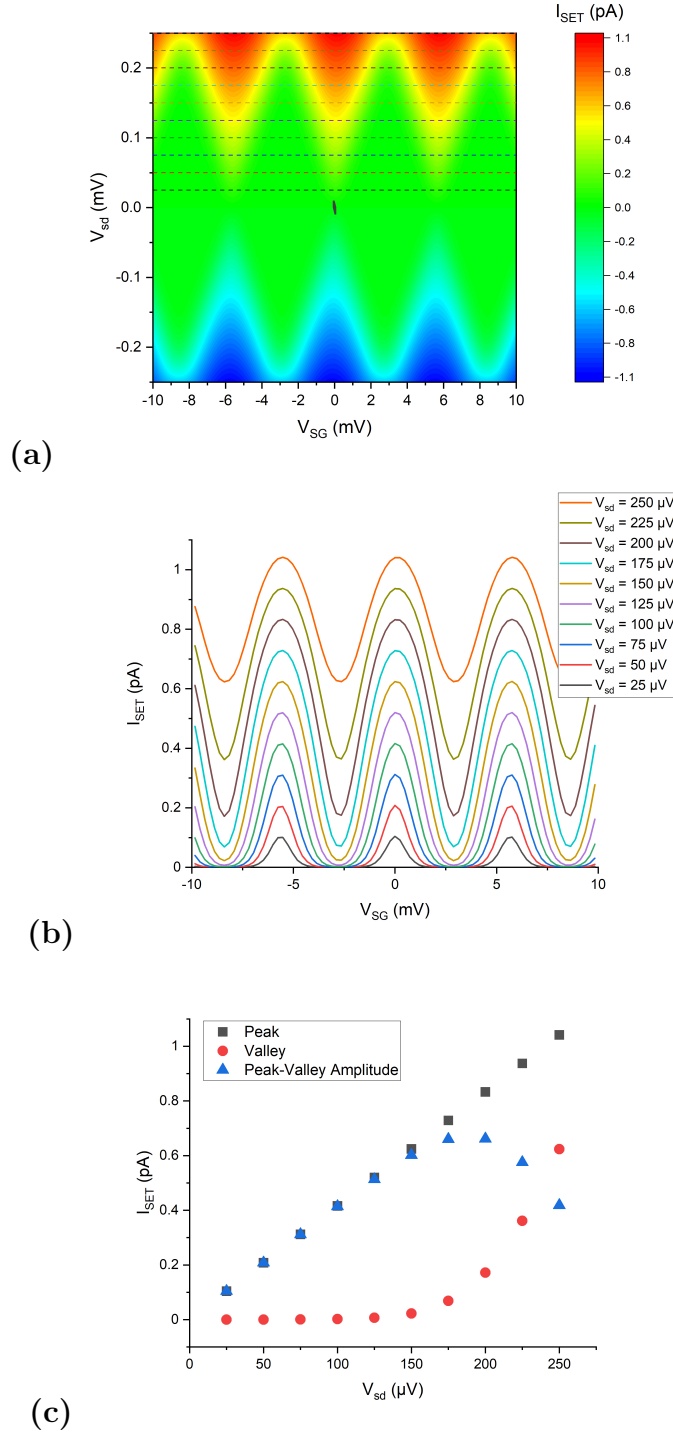


Figure 6.10: SET sensor simulation using Eq. 6.17. (a) Simulated Coulomb diamonds with $T_e = 100$ mK. (b) SET Coulomb blockade oscillation (I_{SET} vs V_{SG}) in a wide V_{sd} range, extracted from these dashed lines in (a). (c) SET current peak value, valley value and peak-valley amplitude in the same V_{sd} range as (b).

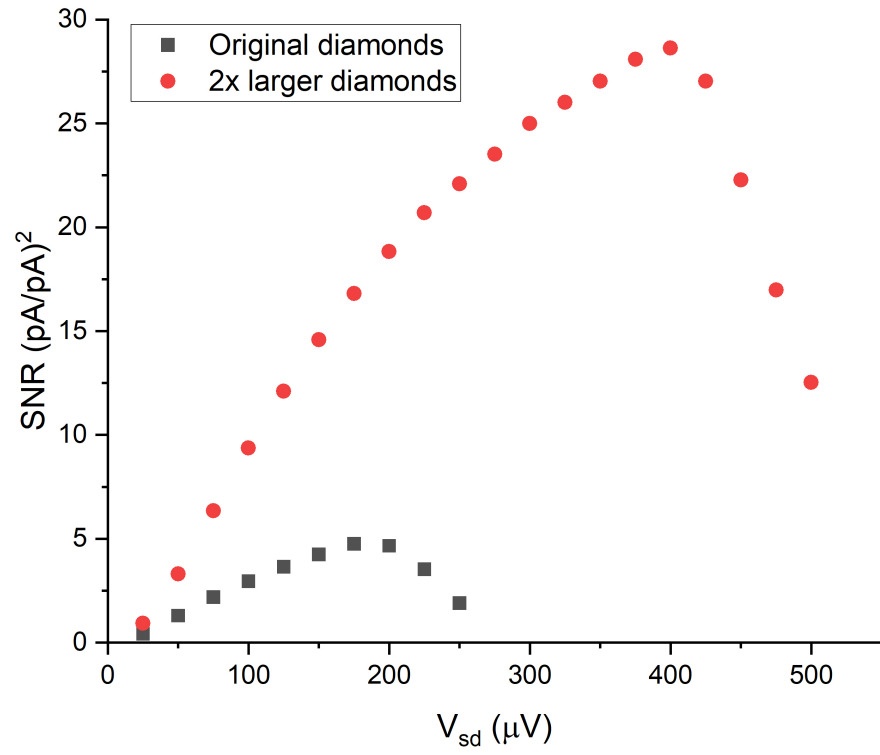


Figure 6.11: SNR vs V_{sd} comparison between the original device and the modified device with the SET sensor having 2 times larger diamonds.

system energy calculation based on a circuit model, the charge stability diagram is simulated. Finally, we present an analytical method to simulate measurement signal and find out the device's optimal operating conditions. The simulation process proposed in this chapter can be used to evaluate a device design for charge sensing and spin readout feasibility, and to improve the device design for better performance.

Chapter 7: Summary of Results and Future Work

7.1 Summary of Results

In this thesis, two types of solid-state quantum computing devices – metallic single-electron transistors with Al/AlO_x/Al tunnel junctions and semiconducting Si MOS quantum dots were developed, fabricated and studied, as well as the discussion of integration scheme of the two types devices for developing preliminary qubit platform.

The performance of widely used AlO_x in solid-state quantum computing has been limited by its material instabilities. In chapter 3, we have successfully reduced the long-term time instability – charge offset drift in AlO_x-based metallic SETs by employing plasma oxidation and UHV fabrication environment. The charge offset drift (ΔQ_0) measured from the plasma oxidized AlO_x SETs in this work is remarkably reduced (best $\Delta Q_0 = 0.13 \text{ e} \pm 0.01 \text{ e}$ over ≈ 7.6 days and no observation of ΔQ_0 exceeding 1 e), compared to the results of conventionally fabricated AlO_x tunnel barriers in previous studies (best $\Delta Q_0 = 0.43 \text{ e} \pm 0.007 \text{ e}$ over ≈ 9 days and most $\Delta Q_0 \geq 1 \text{ e}$ within one day). In plasma oxidation, the Al layer can incorporate much more oxygen in a much shorter time and the oxide is much closer to stoichiometric Al₂O₃ than in conventional thermal oxidation. Therefore, a smaller

number of unoxidized Al defects are expected in AlO_x tunnel barriers produced by plasma oxidation relative to those formed by thermal oxidation. UHV conditions for contamination control are well established to reduce impurity concentrations and improve surface smoothness in the thin Al film deposition, as well as limiting uncontrolled oxide formation in the as-deposited Al layer before deliberate oxygen plasma treatment and reducing structural defects in the tunnel barriers. Success in suppressing time instabilities in AlO_x may pave the way to reducing some decoherence sources associated with AlO_x and enabling expanded implementation within quantum computation systems.

In typical surface-gated silicon MOS devices, the device fabrication is time consuming and involves many lithography steps, which may not be entirely necessary for diagnostic purposes. In chapter 4, we have developed streamlined single metal gate layer, metal-oxide-semiconductor (MOS) quantum dot devices robust against dielectric breakdown, which are considered as prototypes for future diagnostic qubits. These devices are able to form quantum dots, demonstrate capacitive charge sensing between channels, and present reasonable effective electron temperatures (≈ 200 mK) that enable spin qubit studies. These devices were developed as a preliminary solution to a longer term goal of a qubit platform for intercomparison between materials or for in-line diagnostics, and to provide a testbed for establishing classical measurements predictive of coherence performance. We discussed the costs and benefits of the trade-off between device performance and fabrication efficiency, as well as opportunities for future improvements.

To achieve high fidelity in quantum science research, both thermal energy and

measurement noise need to be suppressed. In chapter 5, we studied and reduced the noise broadening of Coulomb blockade peak width using two different quantum dot systems, P donor-based and MOS-based Si quantum dots. Measurements are made in various cryogenic systems over temperatures varying from 10 mK to 25 K. The noise broadening origins and factors inducing high T_e were discussed and analyzed. The noise level derived from the Coulomb peak width broadening in a dilution refrigerator with ≈ 10 mK base temperature was substantially lowered from ≈ 4 K to ≈ 0.5 K.

In chapter 6, we discussed the design and development of charge stability improved, plasma oxidized Al/AlO_x/Al SETs for use as charge sensors in single metal layer gated silicon MOS quantum dots, extending an integrated architecture that enables fabricating both devices simultaneously. By using capacitance modeling and calculation of predicted charge stability diagram, we propose an analytical method to evaluate the charge sensing and electron spin readout feasibility, which will be useful for tweaking the device design to obtain better experimental performance. This device architecture can be used to provide more choices of qubit diagnostics for both semiconducting and superconducting quantum computing devices, and further implement solid-state quantum computing.

Each chapter of this thesis is a building block to implement an integrated solid-state quantum computing qubit platform integrating semiconducting and superconducting devices, and to develop the capability of transducing quantum information between different bases. The achievement of mitigating AlO_x instability that accounts for quantum decoherence, the success of making single metal gate layer MOS

quantum dots that shows robustness against device breakdown, and the capability of simulating and evaluating integrated device design demonstrate the potential to develop the integrated qubit device for advancing solid-state quantum computing.

7.2 Future Work

With the design, modeling and evaluation of hybrid devices integrating stability improved Al/AIO_x/Al SETs and streamlined single gate layer MOS quantum dots, the natural next step is to fabricate the device, conduct capacitive charge sensing, using the Al/AIO_x/Al SET as the charge sensor and MOS quantum dot as the target dot, and perform single-shot readout of electron spin with applied magnetic field. By measuring the probability of observing a spin-up electron $P_{\uparrow}$ with different load/wait times τ_w , the electron spin lifetime or relaxation time T_1 can be extracted by $P_{\uparrow}(\tau_w) = P_{\uparrow}(0)\exp(-\tau_w/T_1)$ [30]. Also, the readout fidelity needs to be assessed, i.e., the probability that an electron spin state is correctly identified. For quantum computation, the electron spin coherence times T_2 is more important than T_1 because for most systems $T_1 \gg T_2$ [18]. To achieve long coherence times, the spin qubit devices will be ultimately fabricated on our isotopically enriched ²⁸Si substrate to eliminate decoherence mechanisms due to ²⁹Si nuclear spin diffusion [117, 118]. With this implementation, we can measure and compare coherence times with different ²⁸Si isotopic enrichment levels. Finally, to advance quantum computing, these qubit devices can be coupled in a scalable manner to implement quantum logic gates with multiple qubits. This requires deliberate control of the exchange coupling among

the qubits [31, 157]. The realization of quantum logic gates will enable the necessary operations for universal quantum computation [47].

For the two components of the hybrid qubit devices, there are interesting directions to be pursued and room to be further improved. For the Al/ AlO_x /Al SETs, we are still interested in separating the contributions from the plasma oxidation and UHV environment and a control group of thermally oxidized SET devices fabricated in the same UHV environment is expected. Also, since we believe plasma oxidation and UHV environment combined lead to ultra stable AlO_x with reduced charge defects [54], the reason why the charge offset stability of Co/ AlO_x /Co SETs are not as good as Al/ AlO_x /Al and seem to be more susceptible to the environmental disturbance can be explored. The material stacks and the fabrication process of two types of SETs can be compared. The superconductivity of the Al/ AlO_x /Al SET can be explored. It is also of interest to test plasma oxidized SETs with other metals, such as superconducting Niobium (Nb), as this will give us more choices of materials in the integrated devices to improve the qubit performance.

For the Si MOS quantum dots, future scaled-down devices with multiple, overlapping gate layers are anticipated to form smaller, deliberately controlled and cleaner dots reaching few-electron and hopefully single-electron regime for optimal qubit performance [31, 58]. Our plasma oxidation technique can be considered to produce the gate isolation oxide for promisingly reduce the failure mode of gate-gate isolation [116]. The currently used 33 nm thickness of the gate dielectric SiO_2 can be reduced to obtain larger direct gate capacitance for better control of the charge inversion layer. Reliable trench isolation is expected to be developed to eliminate

concerns of wire bonding breakthroughs so that maintaining mechanical strength with thicker SiO_2 is no longer necessary.

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