ABSTRACT

Title of Document: CARBON NANOTUBE THIN FILM AS AN ELECTRONIC MATERIAL

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Directed By: Professor Ellen D. Williams and Associate Professor Michael S. Fuhrer, Department of Physics

Carbon nanotubes (CNT) are potential candidates for next-generation nanoelectronics devices. An individual CNT possesses excellent electrical properties, but it has been extremely challenging to integrate them on a large-scale. Alternatively, CNT thin films have shown great potential as electronic materials in low cost, large area transparent and flexible electronics.

The primary focus of this dissertation is patterning, assembling, characterization and assessment of CNT thin films as electronic material. Since a CNT thin film contains both metallic and semiconducting CNTs, it can be used as an active layer as well as an electrode material by controlling the growth density and device geometry. The growth density is controlled by chemical vapor deposition and airbrushing methods. The device geometry is controlled by employing a transfer printing method to assemble CNT thin film transistors (TFT) on plastic substrates. Electrical transport properties of CNT TFTs are characterized by their conductance,

transconductance and on/off ratio. Optimized device performance of CNT TFTs is realized by controlling percolation effects in a random network.

Transport properties of CNTs are affected by the local environment. To study the intrinsic properties of CNTs, the environmental effects, such as those due to contact with the dielectric layer and processing chemicals, need to be eliminated. A facile fabrication method is used to mass produce as-grown suspended CNTs to study the transport properties of CNTs with minimal effects from the local environment. Transport and low-frequency noise measurements are conducted to probe the intrinsic properties of CNTs.

Lastly, the unique contrast mechanism of the photoelectron emission microscopy (PEEM) is used to characterize the electric field effects in a CNT field effect transistor (FET). The voltage contrast mechanism in PEEM is first characterized by comparing measurements with simulations of a model system. Then the voltage contrast is used to probe the local field effects on a single CNT and a CNT thin film. This real-time imaging method is assessed for potential applications in testing of micron sized devices integrated in large scale.

CARBON NANOTUBE THIN FILM AS AN ELECTRONIC MATERIAL

By

Vinod Kumar Sangwan

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Advisory Committee:
Professor Ellen D. Williams, Chair
Professor Romel D. Gomez
Associate Professor Michael S. Fuhrer
Associate Professor Ian Appelbaum
Dr. Vincent W. Ballarotto

Dedication

To my parents, Ved Kaur and Dharam Singh

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Chapter 1 : Introduction

1.1 Historical Background of Carbon Nanotubes

Carbon is found in a wide variety of compounds due to its unique capacity for diverse orbital hybridizations (sp, sp^2 and sp^3). However, till last century, pure elemental compounds of carbon were thought to be limited to diamond, graphite and amorphous carbon. In the beginning of the 20^{th} century, the first carbon fiber was discovered and used in early prototypes of light bulbs by Thomas A. Edison [1]. After WW II, research in carbon fibers was further stimulated by the needs of the space and aircraft industries for strong and lightweight composite materials. However, the smallest diameter achievable for a carbon fiber was reported to be ~ 100 A [2]. The existence of smaller diameter carbon fibers was seriously reconsidered after the discovery of a new allotrope of carbon, buckminsterfullerene (buckyballs) by Kroto and Smalley in 1985 [3]. Buckyballs are hollow spherical molecules consisting of sp^2 hybridized carbons and they triggered speculation about the existence of hollow cylindrical forms of carbon [4-6]. Soon after, the first carbon nanotube was observed by Iijima [7] using transmission electron microscopy in 1991. Since then carbon nanotubes have been extensively studied by scientists around the world.

1.2 Structure and Properties of Carbon Nanotubes

Carbon nanotubes are hollow cylindrical sheets of graphite seamlessly rolled in diameters ranging from 0.7 to 10 nm [8, 9]. A single- (multi-) walled nanotube

results from rolling a single (multiple) graphene sheet(s). Most single-walled nanotubes (SWNT) have diameters less than 2 nm. The two hemispherical ends of CNTs can be neglected for all the properties and applications discussed in this work. Thus the large aspect ratio (> 10^4) makes CNTs essentially one-dimensional nanostructures. To understand the structure and properties of SWNTs, I first consider a honeycomb graphene sheet.

Graphene is a two dimensional hexagonal lattice of sp^2 hybridized carbon atoms (Fig. 1.1) with a basis containing two carbon atoms [9]. Interestingly, a CNT can be obtained by rolling a graphene sheet without distortion in countless many ways. The structure and properties of a CNT depends on the direction in which graphene is folded. For the purpose of completeness, let me introduce the classification system for CNTs. The structure of a nanotube is specified by a vector $\vec{OA}$, connecting the lattice point A (n, m) with the origin O (0, 0), see Fig. 1.1(a). The vector $\vec{OA}$, also called the chiral vector ($\boldsymbol{C_h}$), can be written as $\boldsymbol{C_h} = n\boldsymbol{a_1} + m\boldsymbol{a_2}$, where $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ are two unit vectors (Fig. 1.1), and n and m integers such that $0 \le |m| \le n$. The vector $\boldsymbol{C_h}$ lies along the circumference of the nanotube designated as (n, m), and a translational vector ($\boldsymbol{T}$, perpendicular to $\boldsymbol{C_h}$) defines the axis of the nanotube.

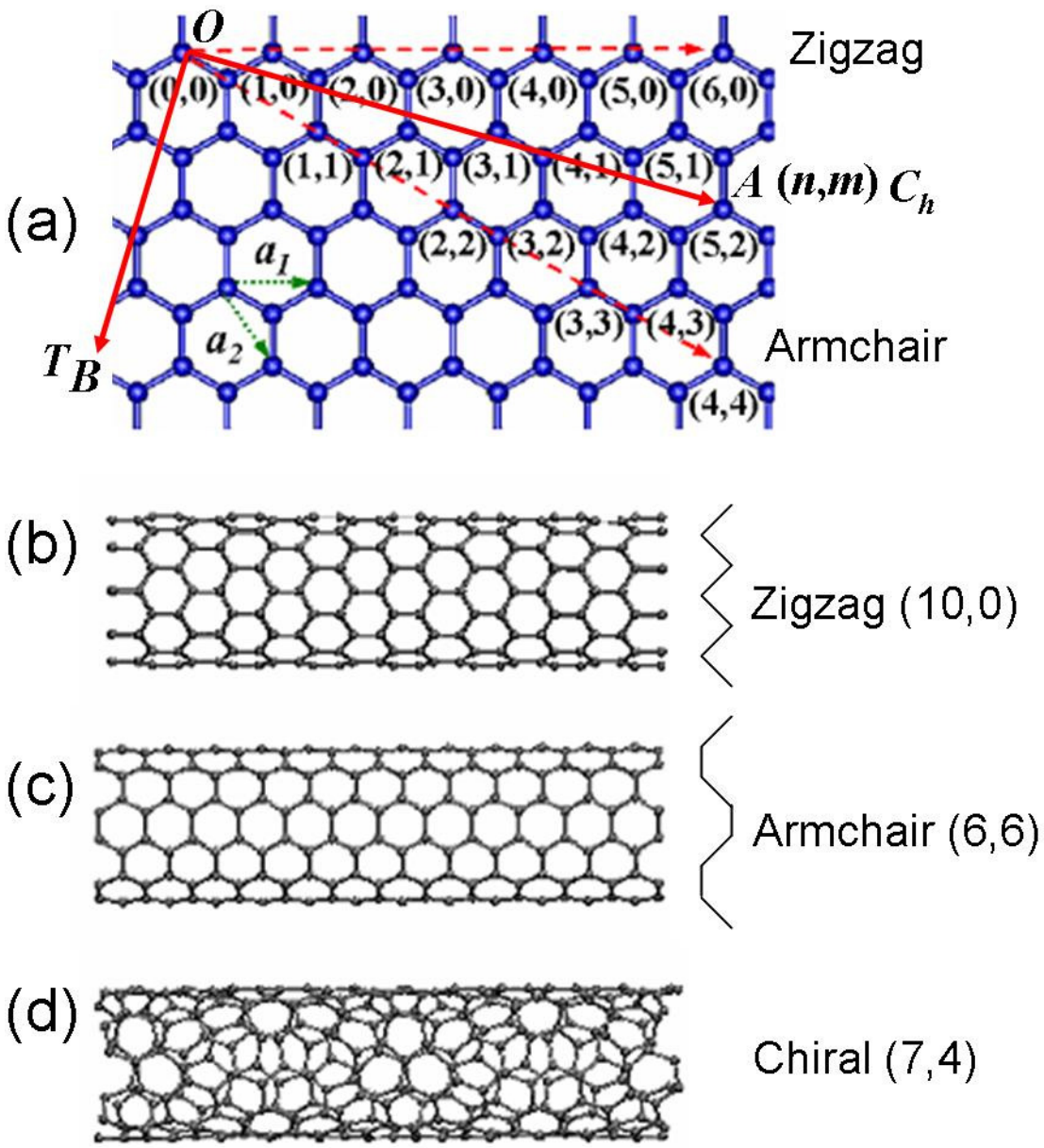


Figure 1.1 a) The honeycomb lattice structure of unrolled CNT (graphene). The unit vectors are denoted by $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$. A CNT designated by (n,m) is obtained by connecting the lattice point (n,m) with the origin. The chiral vector ($\boldsymbol{C_h}$), connecting (n,m) and (0,0), defines the circumference of the CNT. The translation vector ($\boldsymbol{T}$) is perpendicular to $\boldsymbol{C_h}$, and is parallel to the axis to the CNT. b), c) and d) The structure of a zigzag, an armchair and a chiral CNT is shown, respectively. (Courtesy of Prof. Susan Sinnott, UFL).

All possible nanotubes can be classified as achiral or chiral. An achiral nanotube is identical to its mirror image where a chiral nanotube is not. There are only two possible achiral nanotubes; zigzag and armchair nanotubes. A zigzag nanotube (Fig. 1.1(b)) is obtained by connecting a lattice point (n,0) with the origin (horizontal dashed line in Fig. 1.1(a)). An armchair nanotube (Fig. 1.1(c)) is obtained by connecting a lattice point (n, n) with the origin (slanted dashed line in Fig. 1.1(a)). The names zigzag and armchair come from the shape of the cross-sectional rings of the CNTs, as shown on the right side of Fig. 1.1(b) and (c). Connecting any other point (n, m) with the origin will result in a chiral CNT (Fig. 1.1(d)). Note that all the possible chiralities of CNTs in the graphene sheet in Fig. 1.1 correspond to the lattice points in between the two dashed lines. Connecting the origin with lattice points from outside the two dashed lines does not produce a different chirality. The diameter of a CNT resulting from a chiral vector (n, m) is given by [9]

$$d = a\sqrt{n^2 + m^2 + nm}, \qquad 1.1$$

where d is the diameter and a = 2.49 A is the lattice constant of the honeycomb lattice. Though the diameter of three CNTs in Fig. 1.1(a), (b) and (c) (10a, 10.4a and 9.64a, respectively) are almost the same, they show very different electrical properties. Now we will discuss the effect of chirality the CNT on electrical properties of the CNT.

The band structure of CNTs can be simply derived from that of graphene. The tight binding solution of graphene was by derived by P. R. Wallace in 1947 [10]. The band structure near the band edges is shown in Fig. 1.2, where the third dimension (vertical axis) represents energy. One can imagine six pairs of cones and

inverted cones meeting at six corners of a hexagon (i.e. K points). Thus, graphene can be called a zero-gap semiconductor. The energy dispersion relation at low energies near the band edge is given by [9]

$$E(k_x, k_y) = \pm\gamma_0\sqrt{1+4\cos(\frac{\sqrt{3}k_x a}{2})\cos(\frac{k_y a}{2})+4\cos^2(\frac{k_y a}{2})}\,, \qquad 1.2$$

where $\boldsymbol{k_x}$ and $\boldsymbol{k_y}$ are wavevectors, γ_0 is a transfer integral, and a is the lattice constant.

When graphene is rolled into a (n, m) CNT the lattice points (n, m) and the origin correspond to the same carbon atom. Since the wavefunction is single-valued at the origin, a periodic boundary condition is imposed on the wavevector along the circumference of the CNT. Therefore, the wavevector associated with the $\boldsymbol{C_h}$ becomes quantized, while the wavevector associated with $\boldsymbol{T}$ remains unchanged for a long CNT. The boundary condition is expressed as $\boldsymbol{k}.\boldsymbol{C_h} = 2\pi q$, where q is an integer. This condition defines a set of allowed wavevectors $\boldsymbol{k}$ parallel to $\boldsymbol{C_h}$. Thus, the energy bands consist of a set of one-dimensional energy dispersion relations. These wavevectors can be thought of as regularly spaced vertical planes in the band diagram of graphene in Fig. 1.2. The energy bands of CNTs can be obtained from cross-sections of these vertical planes with the cone-shaped band structure. Intersection of a plane with a cone produces either a pair of straight lines (if sliced through origin) or a hyperbola (if slices miss the origin). If the vertical planes are aligned such that they do not intersect with the K points, all the sub-bands are hyperbolic with a finite band-gap (Fig. 1.3(a)). These CNTs are semiconducting with a direct band-gap. However, if some of the vertical planes intersect with the K points of the hexagon, the resulting first sub-band is linear with zero band-gap and all other sub-bands are hyperbolic (Fig. 1.3(b)). These CNTs are zero-gap semiconductors but they exhibit metallic

conduction at finite temperature because an infinitesimal energy is needed to excite carriers into the conduction band.

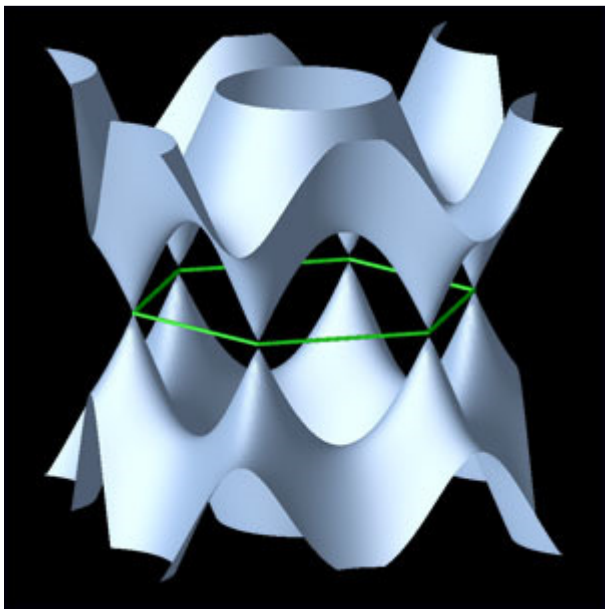


Figure 1.2 Schematic of band structure of 2-dminesional graphene.

CNTs can be divided in three different categories; metallic, semi-metallic, and semiconducting. The chirality $\boldsymbol{C_h} = (n, m)$ of a CNT can uniquely determine the category of the CNT. For the sake of completeness I will state classification conditions without deriving them (the full derivation can be seen in Ref. [9]). A CNT is semiconducting if the quantity $(n - m)$ is not a multiple of 3. If $(n - m)$ is a multiple of 3, two cases arise depending on whether or not $(n - m)$ is also a multiple of $3p$, where p is the highest common divisor of n and m. In case $(n - m)$ is a multiple of 3 but not of $3p$, the resulting CNT is metallic. When $(n - m)$ is a multiple of both 3 and $3p$, the resulting CNTs are semi-metallic or small-gap semiconducting. Semi-metallic CNTs are expected to be metallic from this simple analysis of band structure

but a small band gap (~ 10 meV) exists because of the curvature of the CNT. It has been observed that from an ensemble of CNTs, approximately 1/3 of CNTs are metallic or small-gap semiconducting and the remaining 2/3 of CNTs are semiconducting.

Within this simple analysis, the band gap of semiconducting CNTs (E_g) varies inversely with the diameter of CNTs [11, 12], $E_g = \frac{2\gamma_0 a_1}{d}$, where γ_0 is a transfer integral, a_1 is the nearest neighbor C-C distance in the graphene sheet, and d is the diameter of the CNT. Interestingly, to the first order, the band gap of a semiconducting CNT depends only on its diameter, not on its chirality. However, as we just discussed, CNTs of the same diameter can be either metallic or semiconducting depending on the chirality. Now I will briefly discuss the application of electric properties of CNTs in electronic devices.

Carbon nanotubes possess many remarkable properties. Instead of writing an exhaustive review, I will briefly mention some of the most outstanding and relevant properties. CNTs have been claimed to be one of the strongest and stiffest materials discovered so far. The Young's modulus of SWNTs along the axial direction has been reported to be as high as ~ 2 TPa [11-18] (compare with that of steel ~ 200 GPa). The absence of any dangling bonds makes CNTs stable at high temperatures and compatible with different chemical environments [19]. However, since all the atoms in a CNT are on the surface, they are free to interact with the environment. This property can be useful by functionalizing CNTs for sensing applications [20].

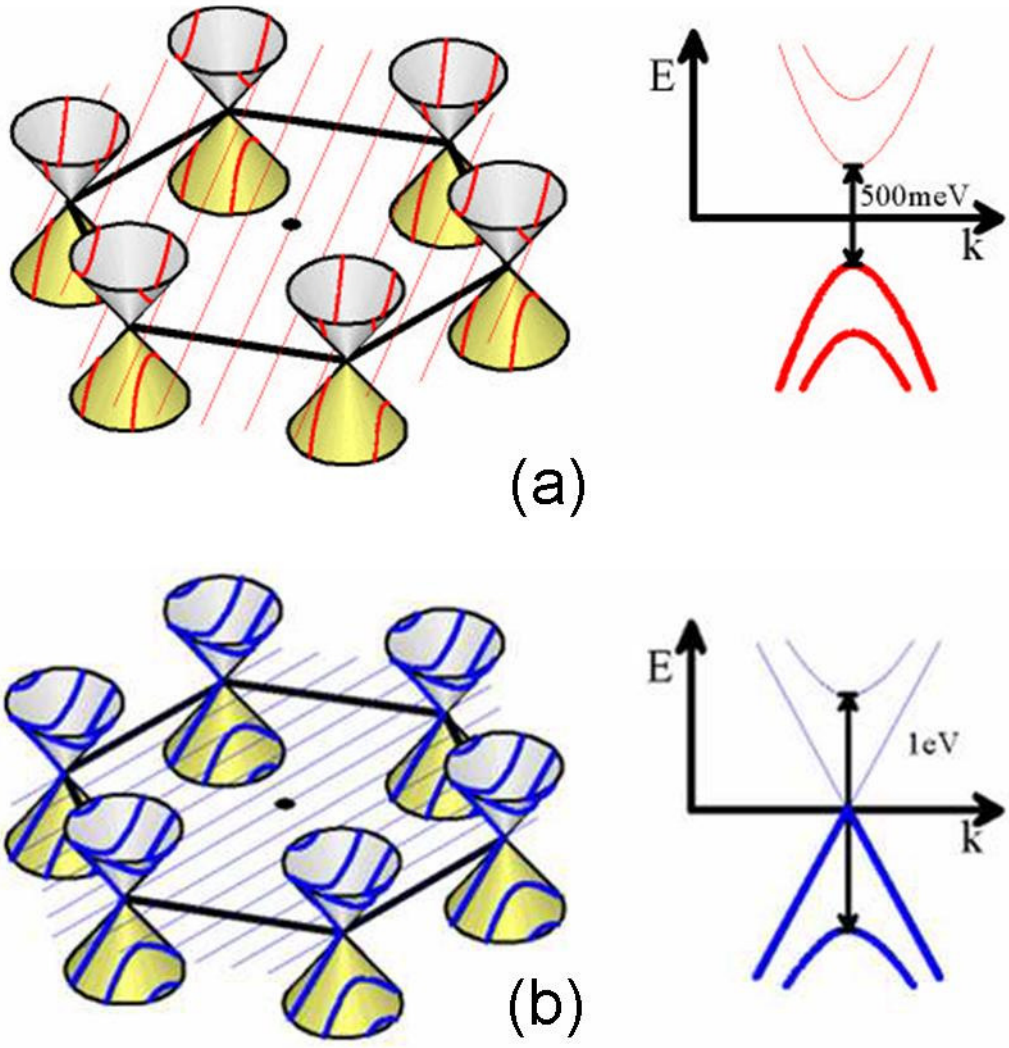


Figure 1.3 The band structure of the CNT can be obtained by applying the boundary conditions on the band structure of graphene. Slices represent the chiral vector of resulting CNTs. a) When slices (red lines) do not pass through any K point, the resulting sub-bands are hyperbolic with a finite bandgap, and a. semiconducting CNT is obtained. b) When slices (blue lines) pass through a K point, the resulting first subband is linear with zero bandgap, and a metallic CNT is obtained. (Courtesy of Prof Michael Fuhrer, UMD)

Defect-free CNTs have long mean free paths of for phonons (~ 1.5 μm [21, 22]) and electron transport (~ 1 μm [23-25]). Due to the first fact, CNTs, like graphite, are very good heat conductors. The thermal conductivity of CNTs at the room temperature is predicted to be as large as 6000 W/m-K (compare with that of

copper, 385 W/m-K). Long mean free paths of electrons makes CNTs excellent 1-dimensional materials to study various quantum phenomena. Ballistic transport has been observed in up to micron long metallic [23, 25] as well as semiconducting CNTs [24]. Even in the diffusive regime, the current densities as high as 10^9A/cm^2 have been observed in both metallic [26] and semiconducting SWNTs [27].

Semiconducting CNTs have been studied extensively in a field effect transistor (FET) geometry [28-32]. In a CNT FET, the CNT is contacted by two metal electrodes (the source and the drain) forming a 1-dimensional device channel in between them. The third electrode (the gate) is separated from the device channel by a dielectric layer. One of the most common materials to make CNT FET with is a Si substrate with a thermally oxidized layer (SiO_2, ~ few 100 nm thick). In a bottom gate FET geometry, the underlying conducting substrate (Si) is used as a gate electrode. In a top gate geometry, an additional metal electrode can also be deposited (separated by a dielectric) on the top of the CNT. Depending on the requirements of specific experiments, several other variations can be introduced in this basic FET geometry. To characterize a material in a FET, the response of gate bias on the device current is monitored. From this, the velocity and mobility of the charge carriers can be calculated. In a semiconducting CNT, the density of carrier in the conduction band can be modulated by the gate bias. These FETs show gate dependent device current. In contrast, the device current in a metallic CNT is independent of the gate bias. SWNTs have exceptionally large room temperature field-effect mobility (~ 10^5 cm^2/Vs [29]) and saturation carrier velocity (~ 2 x 10^7 cm/s [27]). Semiconducting CNT, can also be turned off (~ nA) by controlling the

gate bias, thus producing a high on/off ratio of the devices. These properties make CNT very interesting nanoelectronics materials.

1.3 Why Carbon Nanotube Thin Films Devices?

As discussed in the previous section, an individual semiconducting, single-walled CNT is an excellent semiconducting material with field-effect mobility as large as 10^5 cm^2/Vs [29]. High quality FETs [28, 29, 31, 33] and circuits consisting of individual CNTs have been demonstrated [34]. However, it is difficult to fabricate devices and integrated circuits based on individual CNTs. Techniques such as "find and wire" [29, 35], AFM manipulation [36], mechanical transferring [37], self-assembly [38, 39] or electrophoresis [40] have been employed in the manipulation of individual CNTs and the fabrication of CNT devices. These techniques, however, are labor intensive and difficult to integrate into large-scale fabrication processes.

Additionally, the electronic characteristics of single CNTs are dependent on CNT chirality [8]. No known growth mechanism produces CNTs of precisely controlled chirality, even though success has been recently reported in controlled separation or growth of CNTs with desired characteristics. For example, CNTs of uniform diameter have been purified with potential scalability [41]; metallic CNTs in a FET geometry have been burned at high bias [42, 43]; metallic CNTs in a thin film have been etched by reactive ion etching [44]; and semiconducting CNTs have been selectively grown by a CVD method [45]. However, it remains difficult to incorporate individual CNTs with uniform characteristics in large-scale electronics. Therefore, a thin film of CNTs [46] presents an interesting alternative to single CNTs

as it avoids the difficulties of manipulating individual nanotubes. A CNT thin film also averages out the non-uniformities resulting from nanotube geometry variations.

In applications such as large area, flexible panel displays [47], disposable electronics (e.g. radio frequency identification (RFID)) [48, 49], biocompatible electronics and chemical sensors, the field-effect mobility of the device can be sacrificed for cost and ease of fabrication. Many organic semiconducting materials such as Pn and P3HT have been suggested as potential candidates in these applications. However, CNT thin films not only have better field-effect mobility [50], but they also exhibit the added advantages of environmental stability and large flexibility [51]. Thus, it is worthwhile to incorporate CNT thin films in large area flexible electronics on transparent substrates. Random networks of CNTs [46, 52] as well as aligned CNTs [39, 53-55] have been demonstrated as the potential component in such devices. While aligned CNTs can have the advantage of large channel current they are expected to have a poor on/off ratio due to the presence of metallic CNTs. In contrast, in random networks, the role of metallic CNTs could be more effectively subdued (using percolative effects) to obtain better on/off ratios [52].

1.4 Overview of the Thesis

This thesis explores the scope of using CNT thin films as electronic materials. This research involved a wide variety of fabrication and characterization techniques, which will be introduced in detail where they are first encountered in this thesis. Most of the fabrication steps can be carried out in a moderately equipped clean-room. However, some procedures required very specific tools such as a nano-imprint

machine for transfer printing. Most of the characterization methods will also be familiar to someone with a basic knowledge of MOSFET engineering. However, some characterization tools, such as the photoelectron emission microscope, may be new to some readers. Ample discussion is dedicated to such tools and methods. This research also involved several kinds of simulations carried out by commercially available software packages. Major themes of the thesis can be divided into the following four sections:

a. Controlled growth and patterning of CNTs

We primarily employed chemical vapor deposition (CVD) and airbrushing commercially obtained CNT solutions to obtain CNT thin films. Controlled growth of CNTs by CVD is discussed in Chapter 3. I will also describe and compare different techniques to pattern CNTs in Chapter 3. Chapter 6 discusses the methods of airbrushing CNT thin films and patterning airbrushed CNTs. A novel technique to pattern suspended CNTs is discussed in Chapter 4. These devices were used to study intrinsic properties of individual CNTs.

b. Assembling devices

In this research, I use transfer printing methods extensively to assemble various device geometries on plastic substrates. Transfer printing is used to pattern CNT thin films in Chapter 3, to assemble CNT thin film transistors (TFTs) in Chapter 4 and Chapter 6, and to fabricate suspended CNTs in Chapter 4. Thus, I will introduce the concept of transfer printing in Chapter 2 before anything else in this

thesis. Since photolithography is used in almost all the chapters, it is also introduced in Chapter 2.

c. Assessment of CNTs in electronics applications

The scope of CNT thin films as semiconducting materials is discussed in Chapter 5. The percolation effects in a CVD grown random network of CNTs are studies to optimize the device performance. This experiment is carried out keeping in mind the low-cost large electronic applications in mind and CNT thin films stand out as a potential candidate. The potential of using CNT thin films as electrode materials is discussed in Chapter 6. Airbrushed CNTs are used for this purpose. I also demonstrate all-carbon devices in Chapter 6, where the active layers as well as the electrodes are made from CNTs. The effect of the environment and dielectric layer in CNT devices is assessed in Chapter 4. This experiment involves electronic transport and low frequency noise measurements in pristine suspended CNTs.

d. Unique characterization of CNTs using PEEM

Finally, I will introduce a novel method to characterize the local field effects in CNT devices using PEEM in Chapter 8. This method also has the potential of being used to probe percolative effects in CNT thin film devices. Before that, I will introduce PEEM and its contrast mechanisms in Chapter 7. The voltage contrast of PEEM will also be characterized by studying a model system in Chapter 7.

In the next chapter, I will introduce the concept and procedure of transfer printing.

Chapter 2 : Transfer Printing

Since its inception in the 1950's, semiconductor integrated circuit technology, largely based on processing using photolithography, has dominated solid-state electronics. Photolithography is an expensive method that involves high temperature processes, is limited by optical resolution, and it is restricted by photoresist chemistry and inorganic semiconducting materials. Recently, alternative fabrication methods have been developed to meet requirements of new materials, device geometries and applications. Such techniques include ink-jet printing [56], soft-lithography (e.g. micro-contact printing [57, 58], replica molding [59]), nanoimprint lithography (NIL) [60] and transfer printing (TP) [61, 62]. These methods are compatible with organic as well as conventional inorganic electronic materials. Moreover, these methods have potential to incorporate a wide variety of device configurations.

Here, transfer printing is of particular interest. Transfer printing does not involve chemical processing and is scalable to high volume manufacturing processes (such as roll-to-roll printing [63]) on large areas of flexible substrates. It is important to understand that transfer printing is not a form of lithography but rather is used in conjunction with patterning techniques. Transfer printing offers sequential assembly of lithographically prepared device components incorporating a wide variety of materials. As a result, different components of the device can be independently fabricated on different substrates using different, even otherwise mutually incompatible, processing techniques. Most of the device components such as metal electrodes, CNT thin-films and organic semiconductor layers can be prepared

independently on inorganic substrates. Transfer printing allows sequential incorporation of the device components onto polymer and plastic substrates without affecting the quality of the original device components.

For logic circuits, it may be desirable to encapsulate the active layer in order to isolate any sensitive component from the environment. However, for sensors the active layer needs to be in communication with the environment. Therefore, both top and bottom gate CNT devices have been fabricated here by sequential assembly of components (electrodes, dielectric layer and patterned CNT thin films) by a transfer printing method. In this chapter I will first discuss general concepts and the scope of transfer printing methods. Then, I will describe some commonly used photolithography recipes to fabricate metal electrodes. These recipes will be frequently referred to in subsequent chapters.

2.1 Introduction to Transfer Printing

Transfer printing works on the simple principle of differential adhesion [61, 62]. The work of adhesion, W_A (cohesion, W_C) is defined as the reversible energy gained in bringing together unit areas of two different (similar) materials from infinity to interfacial contact, in vacuum. For a successful transfer printing the following requirements need to be fulfilled:

1. When a uniform un-patterned printable layer is to be printed onto a device substrate from a transfer substrate the work of adhesion (W_A) at the interfaces between the printable layer (PL) and the device substrate (DS) needs to be larger than that between the printable layer and the transfer

substrate (TS). This condition can be written as:

$$W_A(PL/DS) > W_A(PL/TS)$$

2. The work of cohesion of a material is required to be higher than the work of adhesion for at least one of its two interfaces with other materials. If this fails, the material will be torn and fractions of material will be transferred to both substrates during a printing attempt. This condition applies to all the materials involved in the transfer printing and can be expressed as:

$$W_C(TS) > W_A(TS/PL)$$
$$W_C(PL) > W_A(TS/PL) \text{ or } W_C(PL) > W_A(DS/PL)$$
$$W_C(DS) > W_A(DS/PL)$$

3. Transfer printing can also be used to print stacked assemblies of multiple printable layers. In this case, in addition to the previous conditions mentioned above, the work of adhesion between the transfer substrate and the topmost printable layer must also be smaller than the work of cohesion of all the printable layers and the work of adhesion of all the interfaces between them:

$$W_A(TS/i) < W_C(i), W_C(j), W_C(k), W_A(i/j), W_A(j/k), W_A(k/DS)$$

4. To make a device in a useful geometry, the printable layer usually needs to be patterned. In that case, the transfer substrate and the device substrate also come in to contact during transfer printing. The work of adhesion between the two substrates must be less than the work of cohesion of both substrates to avoid mechanical damage when they are separated after transfer printing:

$$W_A(TS/DS) < W_C(DS), W_C(TS)$$

5. Finally, the transfer printing should not deteriorate the electronic, mechanical and other relevant characteristics of the device components.

Fig. 4.1 shows a schematic of a transfer printing process when a stack of multiple printable layers is transferred to a device substrate. When the desired necessary works of adhesion and cohesion are optimized, the printable layers are transferred to the device substrate upon separation of the transfer and the device substrates. Multiple layered devices can also be fabricated by sequential transfer printing of one or a few printable layers at a time, thereby reducing some (but not all) constraints on sequential printing.

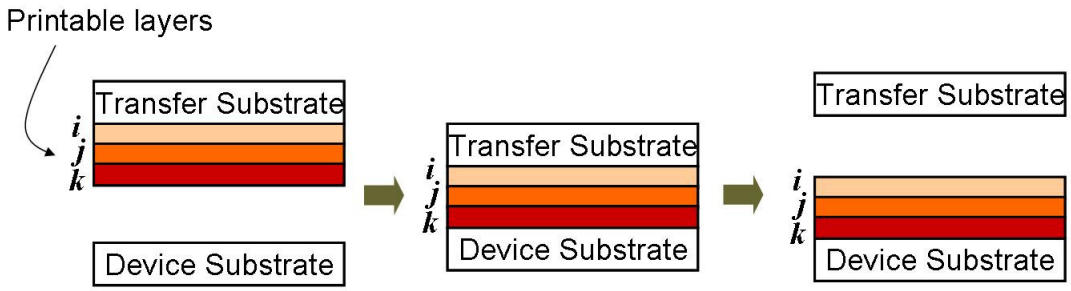


Figure 2.1 Schematic of transfer printing method used to transfer multiple printable layers from the transfer substrate to the device substrate.

Irrespective of the technology used, the transfer printing process should depend only on the above conditions. Since the substrate materials used in flexible electronics are polymeric, temperature (above the glass transition temperature, T_g) combined with pressure is an efficient way to establish the differential adhesion. We

use a Nanonex 2500 imprint machine to achieve this. This machine uses a gas medium to control the pressure (up to 600 psi) and three 500 W tungsten halogen lamps as the heat source to control the temperature (up to 300 ^{o}C). The transfer substrate containing the printable layer is placed on the top of the device substrate with the printable player sandwiched between them. If required, the Nanonex 2500 manual contact aligner can be used to align the printable layer onto the device substrate prior to this step. Two silicone rubber sheets are used to hold the substrates together during transfer printing. The chamber is first evacuated to –14 psig for 3 minutes to create a vacuum between the rubber sheets, which are then mechanically sealed from the chamber throughout the subsequent steps. Then, the chamber is pressurized by N_2 gas and lamps are turned on to heat up the chamber. The temperature of the chamber is monitored by a thermocouple placed under the bottom rubber sheet, and is controlled by using a PID algorithm. The control unit also supports programming the sequence in which pressure and temperature are varied. For most of the applications discussed, the chamber is fully pressurized before turning on the lamps. But for some applications, it is desired to reach an intermediate pre-pressure before turning on the lamps and then attaining the final desired pressure. After transfer printing, the device substrate and the transfer substrate are gently separated.

2.2 Preparation of the Metal Electrodes

The gate and the source and drain electrodes are patterned on Si transfer substrates using photolithography. The Au electrode material is incorporated with either addition of material by e-beam evaporation or subtraction of material using Au

etchant. The material additive technique is described first below, followed by a description of the additive layer.

The Si wafer piece is first cleaned with 1,1,2 trichloroethylene (TCE), acetone, methanol and isopropanol (IPA), followed by baking in a dry oven at 120 ^{o}C for 10 min. A negative photoresist (NR7 1500 PY) is spin coated at 4000 rpm for 1 min to produce 1.5 μm thick layer and then prebaked at 120 ^{o}C for 1 min. The photoresist is then exposed to UV light (12 mW/cm^2) through an optical mask for 16 sec. The photoresist is post-baked at 120 ^{o}C for 1 min to accelerate the chain reactions that polymerize the exposed resist. The photoresist is developed in resist developer (RD6) for 15 sec. A Au film of the desired thickness (usually 100 nm) is then deposited by e-beam evaporation at 2 x 10^{-6} Torr. The Au layer is exposed to reactive ion etching (RIE) using O_2 plasma for 5 min. This increases the surface roughness of the Au electrodes to improve their adhesion to polymeric substrates in transfer printing. Finally, the photoresist lift-off is carried out by a gently stirred resist remover (RR2) heated at 85 ^{o}C. Negative photoresist produces an under-cut in the side walls which is essential to the lift-off. Au is found to have very weak adhesion to the Si surface, possibly due to a thin water layer absorbed on the native oxide surface. In standard practice, a thin film of wetting layer (Cr or Ti) is deposited before Au deposition to improve adhesion. However, for this application, the wetting layer increases the work of adhesion such that the electrodes could not be printed to any of device substrates. Without the wetting layer, extra care is needed for the fragile Au electrodes to survive the lift-off. The minimum feature size achievable by the additive method is 1 μm.

A subtractive approach has also been used to fabricate Au electrodes and successfully incorporate them into transfer printing. First, a Au film is deposited on a clean Si wafer piece by e-beam evaporation followed by exposure to O_2 plasma to produce a rougher top surface. Then, a positive photoresist (OiR 908 35) is spin coated at 4000 rpm for 1 min to produce a 3.5 μm thick layer. The photoresist is pre-baked at 90 ^{o}C and exposed to UV through a photomask. The photoresist is developed in OPR 6242 for 1 min. Then, the Au film, exposed through the windows in the photoresist layer, is etched away by Au etchant GE-1848 (Transene Company, Inc). Finally, the photoresist is removed by soaking in acetone for 5 min. Here, the photoresist does not and need not have an undercut in side walls since it does not involve a lift-off step. Moreover, the surface of the Si substrate can be treated with release layer before depositing the Au film, to further decrease the adhesion of Au to the Si substrate to promote the transfer printing. This is a robust technique to produce a high through-put of Au electrodes. However, since chemical etching is an isotropic process, the minimum feature size of electrodes must be larger than the thickness of the film. The minimum feature size achievable for 100 nm thick electrodes is 1 μm. If precise and smooth features of electrodes are not required, Au electrodes can also be directly deposited on a Si substrate (clean or RL treated) using a shadow mask. The minimum feature size achievable in this case is 100 μm.

We primarily use poly (methyl methacrylate) (PMMA) as the dielectric layer in transfer printed devices, but several other polymeric materials have been incorporated as proof-of-concept dielectric layers (Chapter 5). The solution of PMMA (MicroChem, molecular weight 950,000) in anisole with different

concentrations (4% and 7%) is spin-coated at different speeds (from 1500 to 4000 rpm) on a substrate to obtain dielectric layers of desired thickness (varying from 0.2 to 1.0 μm). The PMMA film is then baked on a hot plate (from 90 - 150 ^{o}C) to evaporate the solvent. Several polymeric device substrates have been successfully incorporated in transfer printing, but we primarily focused on a polyethylene terephthalate (PET) (Dupont Mulinex 453/700) substrate for flexible and transparent CNT devices. We purchased the PET film with a special surface treatment to enhance adhesion. The active area for CNT devices consisting of random network CNTs was patterned by various methods discussed in Chapter 2. Since the CNT films are not optically visible, 30 nm thick Ti alignment markers were fabricated on the SiO_2/Si substrate using photolithography before CNT growth. These markers are used to align the CNT thin film to the device substrate in subsequent printing steps using a manual contact aligner.

2.3 Surface Treatments to enhance Differential Adhesion

As-made device components may not have the necessary differential adhesion required for transfer printing. Therefore, we developed some techniques to control the work of adhesion of the printable layers and the substrates. The surface energy of a material can be enhanced by increasing the surface roughness and/or by modifying the surface chemically. We found that a Au electrode with the top surface exposed to O_2 plasma for 5 min resulted in more robust transfer printing to PET. Similarly, an untreated Au electrode did not print to an untreated PET surface very well, but transferred to an as-obtained pretreated PET film. We also employed a corona discharge technique to further improve the adhesion of PET films. Corona discharge,

however, makes the PET surface so adhesive that it also becomes irreversibly bonded to a Si transfer substrate during printing. Additional surface treatments can be done to the Si surface to avoid this problem. Such bonding problems were avoided by using fluorinated silane self-assembled monolayers (SAMs). We used a (tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane SAM for this purpose. The silane end of the SAM attaches to the Si or SiO_2 surface and the fluorinated part of the SAM acts as a release layer for other materials. The SAM can be deposited on a surface either by vapor phase deposition or liquid phase deposition using microcontact printing. In the first case, the SAM was deposited by exposing the Si substrate to the vapors of the fluorinated silane. To mask the Au electrodes on the Si substrate from the vapors of the fluorinated silane, the Au surface was first treated with a thiol- terminated SAM (benzyl mercaptan). The thiol group attaches to the Au surface but not to the Si surface.

The procedure for adhesion modification is as follows: The Si substrate containing Au electrodes is placed in a home-made chamber, and evacuated to 50 mTorr. Then, benzyl mercaptan vapors are introduced to the chamber for 2 hours. The substrate is rinsed with IPA, and then the release layer is deposited in the same manner using another similar chamber. It was found that excessive exposure (more than 5 min) of the Si surface to fluorinated silane decreased the surface adhesion so much that even dielectric polymers such as PMMA could not be spin-coated. However, exposure for 2 min results in successful spin-coating of polymer as well as useful differential adhesion for transfer printing. Treated substrates are stored in a dry N_2 box because the silane SAM is known to deteriorate in air.

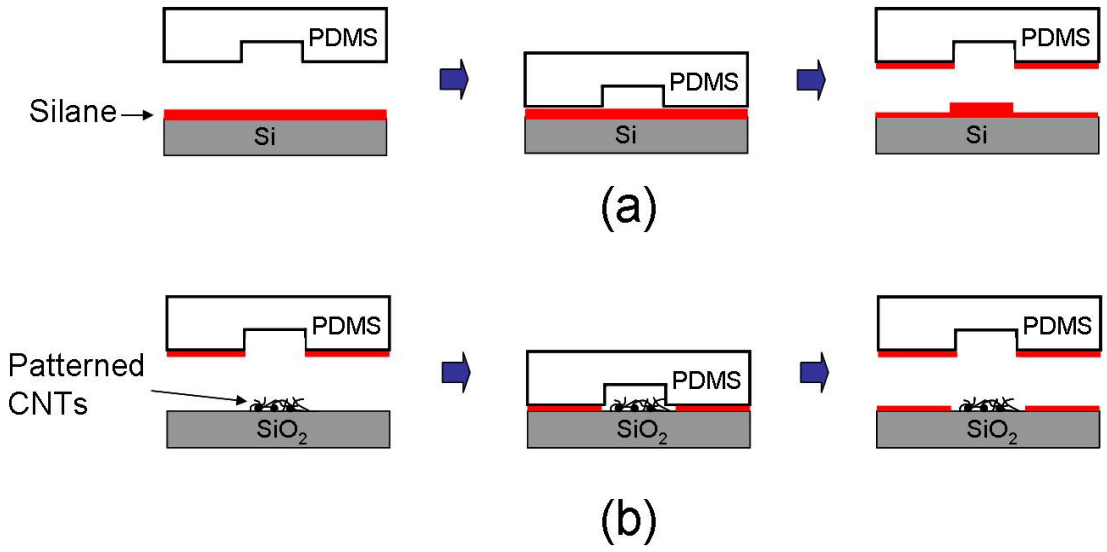


Figure 2.2 a) PDMS stamps are treated with release layer on Si substrate for 15 minutes. b) The PDMS stamps are aligned over patterned CNT thin films and release layer treatment is done on the area outside the CNT patterns by micro-contact printing.

A release layer treatment was also used on SiO_2 substrates containing CNT thin films. When CNT thin films are patterned by photolithography, the surface treatment is done by vapor phase deposition before removing the photoresist covering the patterned CNTs (see details in Chapter 3). In other patterning techniques, where CNTs are not covered by a photoresist, the release layer is patterned onto the Si substrate by micro-contact printing using polydimethylsiloxane (PDMS) stamps. PDMS stamps have been extensively used in similar applications in soft-lithography [57, 58].

The procedure for patterning the release layer by PDMS stamps is as follows: First, a 10 mM solution of (tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane is prepared in anhydrous ethanol. PDMS stamps are made from the same master Si

stamp as used in Section 3.2.3 to make PET templates. A Slygard 184 silicone elastomer base is mixed with its curing agent by stirring vigorously for 5 min, creating air bubbles in the elastomer paste. To remove the bubbles, the paste was kept in a chamber that is slowly evacuated to approximately 100 mTorr. The elastomer is then poured onto the master Si stamp, placed in an oven and heated at 120 ^{o}C. The oven is slowly evacuated to remove the bubbles introduced during the pouring step. After curing the stamps in the oven for 1 hour, the master Si stamp and its PDMS negative are carefully separated. In parallel, the fluorinated silane solution is spread over a blank Si substrate in a dry N_2 chamber. After the solvent evaporates, the PDMS stamp is kept on the Si substrate for 15 minutes to treat the protruding parts of the stamp with silane, as illustrated in Fig. 2.2(a). The PDMS stamp is then aligned and brought into contact with the SiO_2/Si substrate containing the patterned CNT thin films, such that the CNT patterns lie under the trenches in the stamp, as shown in Fig. 2.2(b). Since the same master stamp is used to make both the PET stamp to pattern the CNTs and the PDMS stamp to pattern the release layer, only the area outside the patterned CNTs is treated with the release layer. Therefore, the CNTs remain pristine. This step exposes the silane-treated stamp to air so the time involved in this step should be minimized. After 15 minutes of contact, the stamp and the substrate are separated and stored in dry N_2 box till further use.

Chapter 3 : Growth and Patterning of Carbon Nanotubes

In this chapter we describe the CNT growth process and fabrication techniques to pattern CNT thin films. Some of the commonly used techniques to synthesize CNTs are arc discharge [7], laser ablation [64], high pressure decomposition of carbon monoxide (HiPCO process) [65] and chemical vapor deposition (CVD) [66-71]. The CVD process has been shown to produce large quantities [72] of long single walled nanotubes [30, 73] with fewer defects [74]. CVD can also be used to control the average length of CNTs, the areal density of CNT thin films, and the distribution of CNT diameters by varying the growth duration, the density and the size of the catalytic particles. We used CVD grown CNT thin films as the active layer in CNT thin film transistors (TFTs). For the fabrication of CNT TFTs, it is desirable to pattern the CNT thin films to isolate the devices that are in close proximity to each other. Various fabrication techniques to pattern CVD-grown as well as airbrushed CNT thin films will be described in this chapter.

3.1 Carbon Nanotube Growth by Chemical Vapor Deposition

CNT thin films can be grown by CVD using many catalytic materials such as Fe, Ni, Co, Mo etc. [75]. We use iron nanoparticles on thermally oxidized Si (300 nm or 500 nm thick SiO_2) substrates to grow CNTs. Iron catalytic particles can be dispersed on the growth substrate in various ways such as using supported catalyst [70], using ferric nitrate nanoparticles in isopropyl alcohol (IPA) [36], and using

ferritin encapsulated iron nanoparticles in de-ionized water (DI) [76, 77]. We used the last two methods to obtain iron nanoparticles.

The process for dispersing catalyst particles on a growth substrate is as follows: Anhydrous ferric nitrate is dissolved in IPA (70 μg/ml) and mixed well by stirring the solution overnight. Pieces of thermally oxidized Si (500nm SiO_2) wafer pieces were cleaned with solvents (acetone, methanol and IPA) and dipped in the catalyst solution for 10 seconds. Then they were dipped in a hexane solution (mixture of 5% cyclo-hexane and 95% n-hexane) for 10 seconds. The hexane solution helps ferric nitrate nanoparticles to precipitate and stick to the SiO_2 surface. The resulting samples are ready for CVD growth. Ferritin catalyst solution was purchased from Atomate Corporation and stored at 2^o to 8^o C. Ferritin protein molecules have a spherical structure with a cavity inside, in which the iron nanoparticles are stored [77]. The concentration of the ferritin was diluted from 51 mg per ml aqueous solution (0.003 molar, as purchased) to 0.1 - 0.5 mg per ml by adding de-ionized water (DI). Wafer pieces of the growth substrates (thermally oxidized Si or quartz) were soaked in ferritin solution for 8 minutes. After drying the SiO_2 surface with nitrogen gas, the wafer pieces are ready for CVD growth as described below.

Ferrin nitrate soaked chips (roughly 0.5 cm x 0.5 cm) were put in a quartz boat and set in a single zone Lindberg/BlueM tube furnace with a 1 inch quartz glass tube, Fig. 3.1. O_2 was flushed out of the quartz tube before introducing the explosive gases. This is done by flowing argon gas for 10 minutes with the flow rate of 730 ml/min (Table 3.1). Then O_2 was purged out of the flammable gas lines by flowing

CH_4, H_2 and C_2H_4 for 3 minutes with a flow rate of 1000 ml/min. The furnace was then heated up to 850^oC gradually through several ramping and soaking steps using an Omega CN4431 PID-temperature controller. The oven was soaked for 5 minutes at each of 3 intermediate temperatures (600 ^oC, 750 ^oC, 825 ^oC) to stabilize the temperature. Ar gas was kept flowing (730 ml/min) during heating. At 850 ^oC, CNTs were grown by flowing CH_4, H_2 and C_2H_4 in the furnace at the flow rates of 1900 ml/min, 1300 ml/min and 10 ml/min, respectively. The growth parameters are shown in Table 3.1. These flow rates have been reported to produce optimized long single walled nanotubes [30]. H_2 is believed to reduce iron nanoparticles whereas CH_4 and C_2H_4 act as carbon feed-stock for CNT growth. The growth was done for 8 to 10 min and then the furnace was purged with Ar and simultaneously cooled down to room temperature. The resulting film is expected to have mostly single-walled CNTs with a ratio of one-third metallic CNTs to two-thirds semiconducting CNTs [30]. When using ferritin catalyst, an additional calcinations step is required to burn the ferritin covering off the iron nanoparticles. For that purpose the samples were initially heated up in air keeping both ends of the tube open at 850^oC for 10 minutes before the growth. The furnace was cooled down to room temperature. Then, the procedure for the growth of CNTs is exactly same as described above, and shown in Table 3.1.

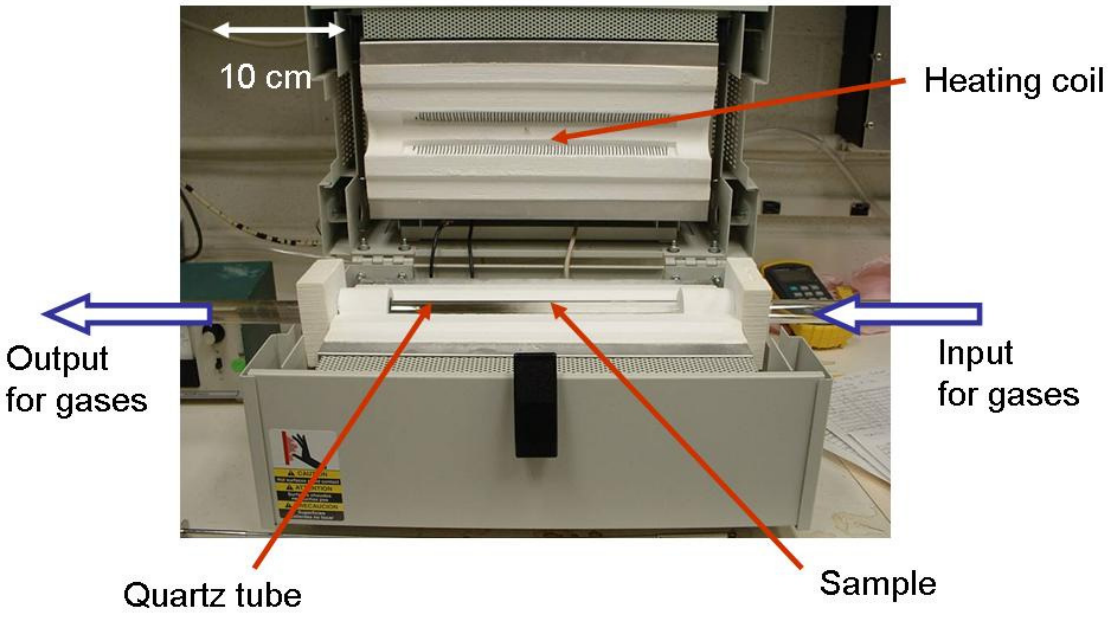


Figure 3.1 Chemical Vapor Deposition (CVD) set up for CNT growth.

Action	Gas	Flow	Temperature	Duration
Purge	Ar	729 ml/min	RT	10 min
Heat	Ar	729 ml/min	RT – 600° C	10 min
	Ar	729 ml/min	600° C – 750° C	5 min
	Ar	729 ml/min	750° C – 825° C	5 min
	Ar	729 ml/min	825° C – 850° C	10 min
Grow	H2	1900 ml/min	850° C	8-10 min
	CH4	1300 ml/min		
	C2H4	10 ml/min		
Cool	Ar	729 ml/min	850° C - RT	~ 2 hours

Table 3.1 Growth procedure of CNTs using CVD.

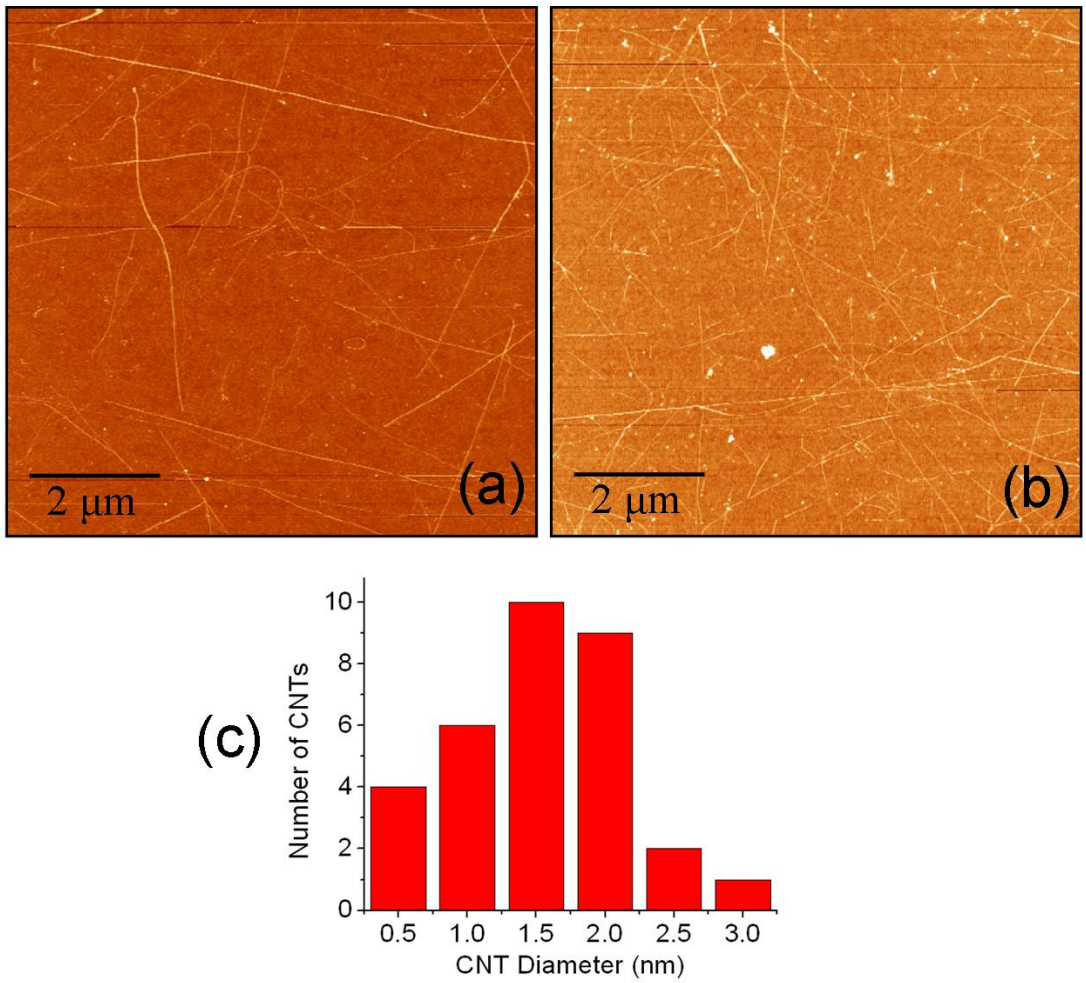


Figure 3.2 AFM images of CNT thin film grown by CVD using a) ferric nitrate, and b) ferritin catalyst. c) Diameter histogram of CNT grown using ferric nitrate.

Fig. 3.2(a) and (b) show AFM pictures of CNT thin films grown from ferric nitrate and ferritin catalyst, respectively. CNT thin films grown from ferritin catalyst tend be slightly denser than those from ferric nitrate for the above mentioned concentrations. The band gap of a semiconducting CNT is known to depend on its diameter [11, 12] and smaller diameter CNTs are reported to higher energy band-gap leading to larger on/off ratio of the devices. So, it is desirable for our purpose to have CNTs within a narrow range of small diameter. The diameter of a CNT is known to

correlate with the diameter of the catalyst particle [77-81]. Since ferritin protein cavities restrict the size of iron nanoparticles, the resulting catalyst particles are expected to have smaller and more consistent size [82]. Ferric nitrate catalyst has also been shown to produce mostly single walled CNTs. The diameter of the CNTs was obtained from the height profile in AFM images. A histogram of the diameter of 35 CNTs (grown from ferric nitrate) shows a peak around 1.5 nm, see Fig. 3.2(c). This diameter distribution suggests that most of the CNTs are single walled. The average diameter of the CNTs grown by ferritin was found to be 1.4 nm from analysis of AFM images (Fig. 3.2(c)).

3.2 Controlling the Density Carbon Nanotubes

The density of the CNTs is expected to depend on the growth time, flow rate of feed gases and the concentration of the catalyst solution. A direct linear correlation was not observed between the density of CNTs and the growth time. It has been suggested that CNTs stop growing after some time and gas flow for longer duration has less and less effect on CNT density. Most of the CNT thin films reported in this thesis were prepared by 8 to 10 min growth. The density of CNTs in a thin film was controlled by two methods: by varying the ratio of feed gases and by varying the concentration of the catalyst. Controlling the density of CNTs by varying the concentration of ferritin catalyst was difficult, due to solution to solution variability and handling issues. Therefore, ferric nitrate catalyst was used in both methods.

It is usually difficult and unreliable to characterize the density of CNTs by counting the number of CNTs per unit area. Thus, we employ here a grid method to determine the density of nanotubes. A two dimensional grid of lines was overlaid on SEM images of CNTs as shown in Fig. 3.3(a). The density of the CNT network is characterized by an average density of intersecting points, p (the number of intersections per unit gridline length) between CNTs and the grid. We simulated random networks in Interactive Data Language (IDL 6.0) to confirm that the parameter p correctly characterizes the density (number of lines per unit area). The average density of intersections between the grid and a network of random lines (generated by IDL) varied linearly with the density of the network. The grid spanned over an area (100 μm x 100 μm) larger than average length of CNTs (7 μm). The total length of grid lines was also chosen sufficiently large, ~ 1.2 mm. The average density parameter p was obtained from grid analysis at two opposite corners of each sample.

In the first method, the density of CNTs thin films was controlled by relative composition of the gases H_2 and CH_4 (no C_2H_4) [76] while keeping the total gas flow constant at 2000 ml/min. The concentration of ferric nitrate was kept 70 μg/ml. The parameter p is plotted against ratio of CH_4 to the total gas (in absence of C_2H_4) flow rate in Fig. 3.3(b). The highest density of CNTs (p = 0.13, i.e. roughly 50 CNT/100 μm^2) was achieved at 65% CH_4 after which the yield of CNTs exhibited a sudden drop, probably due to poisoning of the catalyst by excessive carbonation [76]. A small amount of C_2H_4 (3 ml/min) could be introduced in the furnace to obtain denser CNT films.

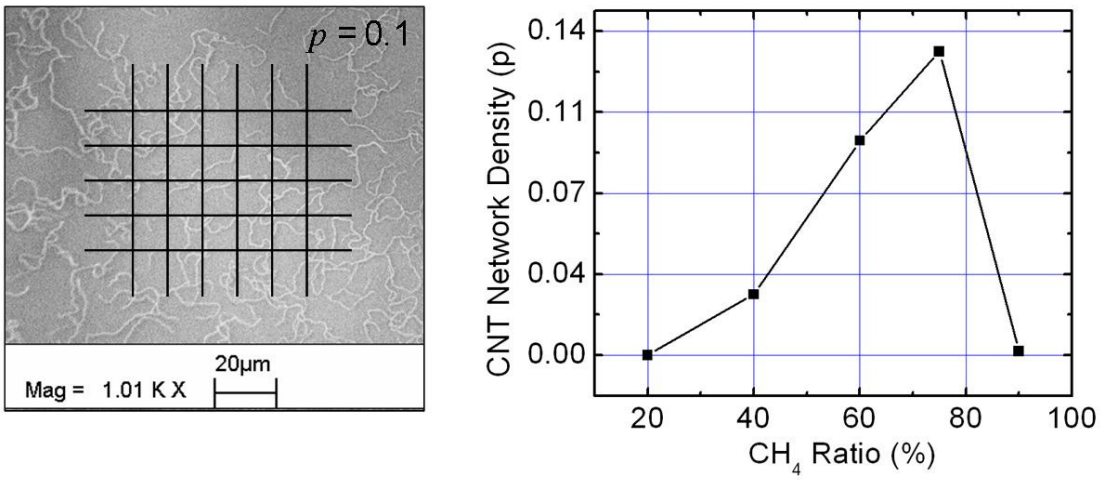


Figure 3.3 a) An SEM image of CNT thin film grown by 40% H_2 and 60% CH_4 with total gas flow of 2000 ml/min. Overlaying grids is used to characterize the density of CNT mat. The image has p = 0.1 intersections/μm, which corresponds to roughly 40 CNTs/100 μm^2. b) CNT network density as a function of ratio of CH_4 to total gas feed.

In the second method, the density of CNT was controlled by varying the concentration of the ferric nitrate solutions. The gas flow rate of CH_4, H_2 and C_2H_4 was kept at 1900 ml/min, 1300 ml/min and 8 ml/min, respectively. Ferric nitrate solutions of ten different concentrations (varying from 2 μg/ml to 133 μg/ml) were prepared and dispersed on different growth substrates. CNTs were grown for 10 min on all the substrates. Fig. 3.4(a) shows the variation in the average density of CNTs (p) as a function of concentration of the catalyst. Fig. 3.4(b), (c) and (d) show SEM images of CNT thin films obtained from catalyst concentration of 2 μg/ml, 20 μg/ml and 66 μg/ml, respectively. It is interesting to note that CNT density initially increases rapidly with the concentration and then becomes almost constant for concentrations higher than 66 μg/ml. The maximum density of CNTs achievable from the first method was 0.14 intersections/μm. (We found that CNTs with density higher density is needed for high quality CNT thin film devices (see Chapter 4)) This

method was used to produce CNT thin films with densities in a broad range varying from p = 0.35 intersections/μm (Fig. 3.4(b)) to p = 3.43 intersections/μm (Fig. 3.4(d)). These CNT thin films were used in an experiment to study the effect of the CNT density on device performance (see Chapter 4).

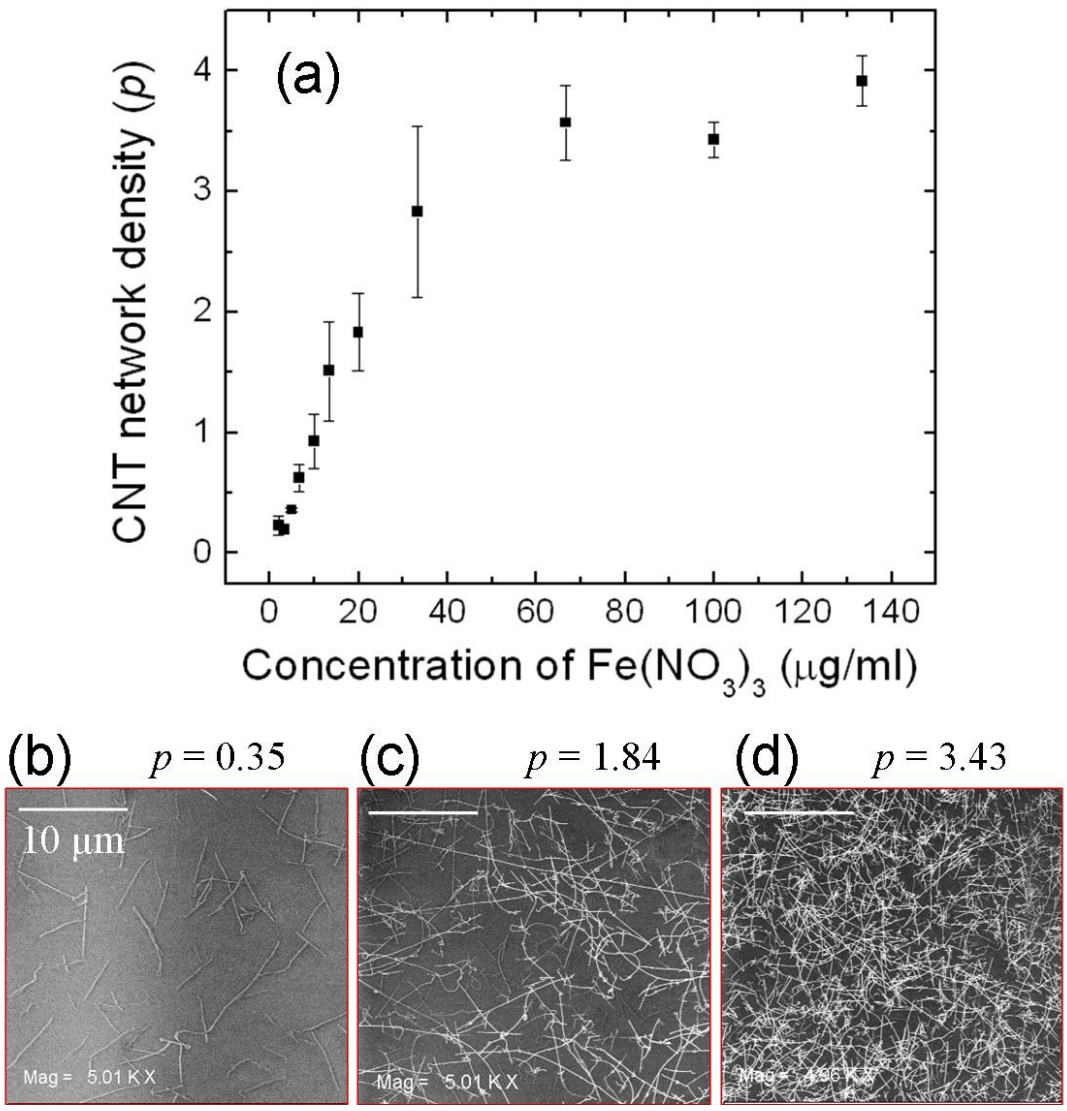


Figure 3.4 a) Average density of CNT network (p) is plotted against the concentration of ferric nitrate solution. The error bars correspond to the difference in the density of CNTs at two opposite corners of a growth substrate. b), c) and d) SEM image of CNT thin film with p = 0.35, 1.84 and 3.43 intersection/μm, respectively. The scale bar in all the images is 10 μm.

3.3 Techniques for Patterning Carbon Nanotube Thin Films

It is essential to pattern CNT thin films to make useful arrays of devices. Even when study of a single device is intended, patterning the CNT film is important. For example, when wafer pieces are immersed in catalyst solution, the CNTs are expected to grow everywhere on the SiO_2 surface, including the edges. It was observed that the percolating network of CNTs makes a conducting path to the Si back gate. Thus, it is undesirable to make CNT thin film transistors directly on the growth substrate without patterning the CNT thin film. Patterning the CNT thin films is also needed to define geometrical parameters of the device, such as the channel length and the channel width. Various techniques to pattern CNT thin films will be discussed in this section.

3.3.1 Photolithographic Patterning of CVD grown CNTs

Photolithography offers a straightforward way to pattern CNT films. Since the CNT thin films are not sufficiently optically visible for using a contact aligner, prior to CNT growth 30 nm thick Ti alignment markers were fabricated on the SiO_2/Si substrate by photolithography. To pattern the CNT thin film, a photoresist (positive toned OiR 908 35, Fujifilm or negative toned NR7 1500 PY, Futurrex Inc.) was spin coated over the SiO_2/Si substrate surface containing the CNT thin film. The photoresist was exposed to UV light (12 mW/cm^2) through a photomask to define desired shape and size (e.g. 200 μm square areas) using a Karl Suss Mask Aligner. After developing the photoresist, the film area to be retained was protected by the remaining photoresist. The CNTs outside the covered area were burned by reactive

ion etching (RIE) using an O_2 plasma (power = 100 W, pressure = 200 mTorr, PlasmaTherm 790 Series) for 1 min. Now the photoresist can be removed by acetone and we get a patterned CNT film. Schematic of this procedure are shown in the first two steps in Fig. 3.5.

The as-patterned CNT film can be used to make devices on the SiO_2 substrate. However, to make patterned CNT films compatible with the transfer printing process (see Chapter 2) we need to do a surface treatment to the SiO_2 substrate. Before removing the remaining photoresist that covered the patterned film, the exposed SiO_2/Si surface was treated with a (tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane self-assembled monolayer (SAM). This SAM treatment creates a release layer to decrease the work of adhesion of the SiO_2 surface to establish a desirable differential adhesion against device substrates [61] (see Section 2.3 for details). Finally, the remaining photoresist was washed away with acetone and the resulting CNT film is ready to be transfer printed. A schematic of this process is shown in the last two steps in Fig. 3.5.

A possible disadvantage of this patterning technique is that the CNTs have been exposed to various chemical treatments. The effect of chemical processing on transport properties of CNT TFTs is discussed in Appendix B. Moreover, the SAM layer on the SiO_2/Si surface is not compatible with the annealing process to remove possible surface contaminants [83]. Therefore, patterning processes that do not expose the CNT film to resist processing chemicals have been developed. Two such patterning methods are (1) CVD-grown CNT films from pre-patterned catalyst and

(2) transfer printing of CVD grown CNTs to polymer stamps. These techniques have the advantage that no chemicals come in contact with the CNTs during the patterning.

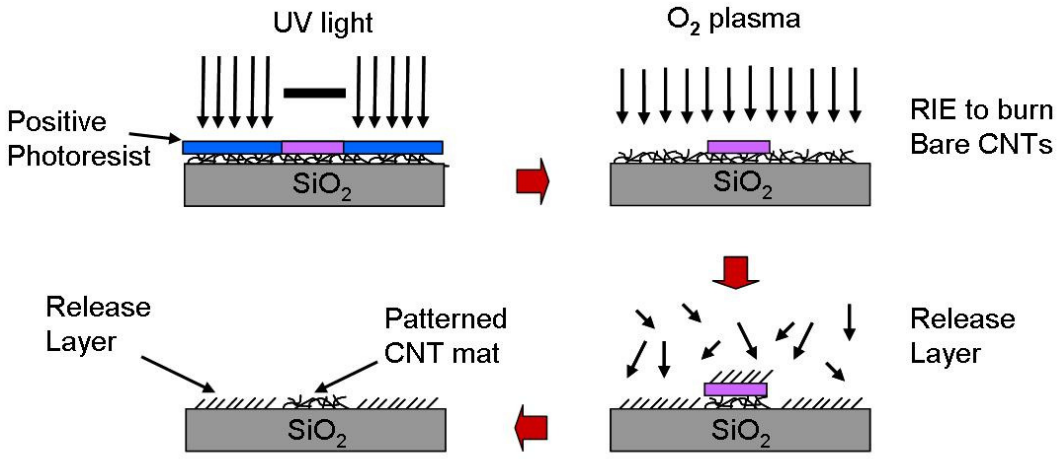


Figure 3.5 Photolithography and reactive ion etching are used to pattern a CNT thin film after grown of CNTs where a release layer is applied prior to lift-off to aid transfer printing.

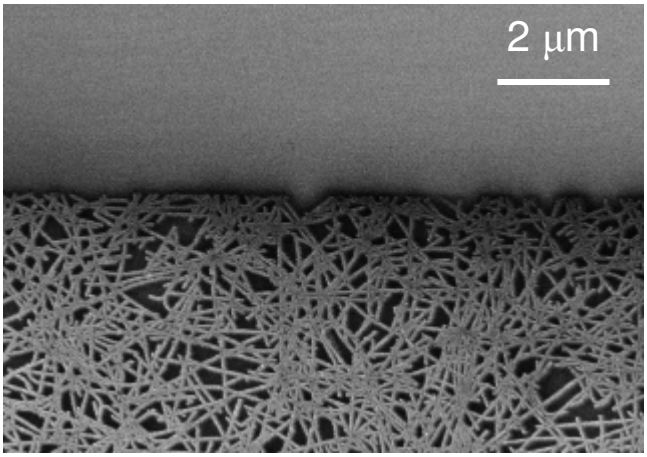


Figure 3.6 SEM micrograph of the edge of a CNT thin film patterned by photolithography.

3.3.2 Pre-patterning of the Catalyst

As stated above, it is desirable to develop a patterning technique by which CNTs are not left with residues of resist-processing chemicals. This can be achieved by patterning catalyst nanoparticles prior to CNT growth. Isolated CNTs have been grown by using patterned catalysts [71, 84]. Here we wish to grow a patterned CNT thin film using a similar process. We used different processing chemicals here.

3.3.2.1 Pre-patterning the Catalyst using a Photoresist

In this case, CNT films were grown using pre-patterned ferritin catalyst. A positive photoresist (OiR-908 35) was spin coated onto a SiO_2/Si substrate. The photoresist was exposed through a photomask containing 500 μm square features. After developing the photoresist, the ferritin was deposited onto the patterned SiO_2/Si substrate by soaking in an aqueous solution of ferritin (0.5mg/ml) for 8 minutes. CNTs were then grown by CVD as described earlier in this chapter. This patterning process is shown schematically in Fig. 3.7.

Fig. 3.8 shows AFM and SEM images of the patterned CNT thin films. A continuous and uniform CNT thin film can be seen in the patterned area. There is, however, a dense strip of CNTs on the edge of the patterned area, possibly due to excessive deposition of the catalyst near the edge of patterned photoresist. There are also some CNTs grown outside the patterned area because during the lift-off step some ferritin molecules can stick back to the substrate. The density of the CNTs outside the pattern is reduced by facing the substrate down and slowly moving it up during lift-off. CNTs outside the patterned area are too sparse to make any

percolative network. Thus, multiple devices fabricated on a substrate are still electrically isolated from each other.

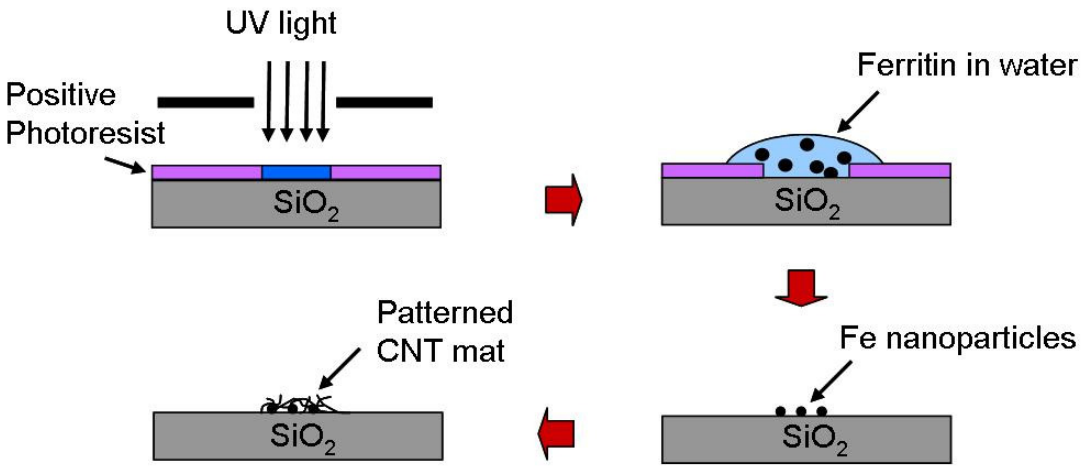


Figure 3.7 Photolithography is used to pattern the ferritin catalyst before CNTs are grown.

Here, we cannot treat the SiO_2 surface with the release layer in gaseous phase because the CNTs would also get exposed. CNT thin films on untreated SiO_2 substrate are not compatible with a reliable and complete transfer printing process (CNTs do transfer print to PET partially). However, the surface treatment on these patterned CNT thin films can be carried out by micro-contact printing of the release layer using elastomeric templates. This process is explained in detail in Section 2.3.

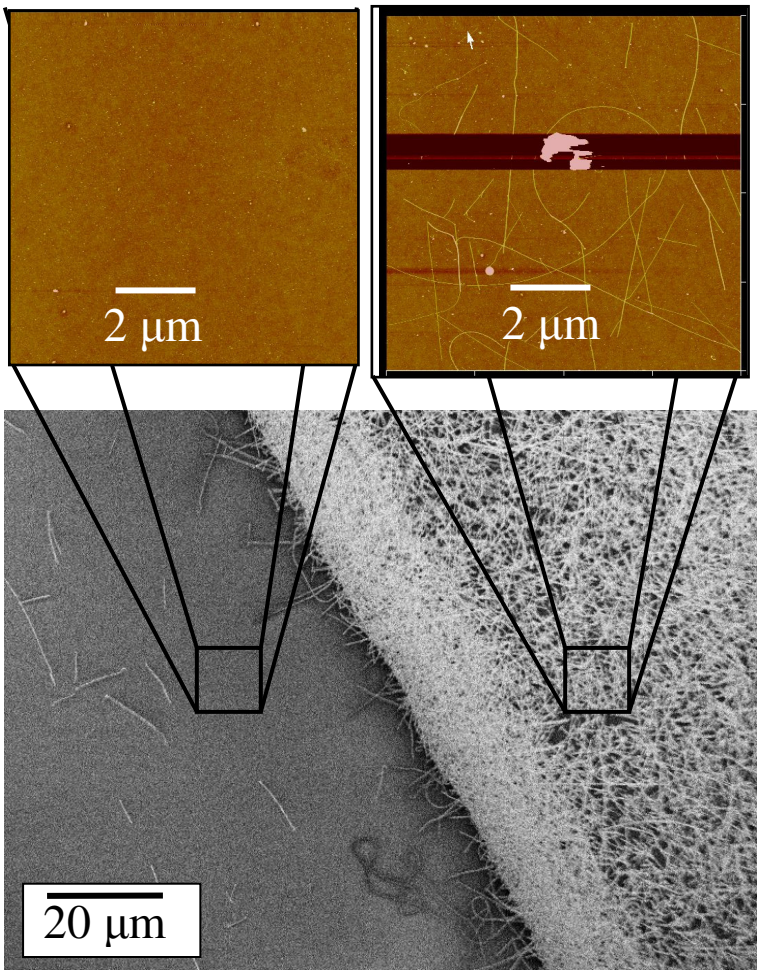


Figure 3.8 An SEM image of the edge of a CNT thin film patterned by pre-patterning the ferritin catalyst by photoresist. Two AFM images are also taken from the regions b) inside and c) outside the patterned CNTs films.

Ferric nitrate catalyst cannot be used to grow patterned CNTs by this method because hexane was observed to react with the positive photoresist. We also could not use negative photoresist because the stripping chemical for the negative resist (RR2) affects the patterning process such that no CNTs were seen after the growth. We can use PMMA to pattern ferric nitrate because it can be easily removed by acetone, which does not affect the catalyst. However, PMMA is not a photoresist for the UV power range available in our photolithography machine. Using e-beam

lithography to pattern the desired large area (up to 500 μm) of PMMA is a very time consuming and inefficient process. Thus, we used a bilayer of PMMA and negative photoresist to pattern PMMA by photolithography, as illustrated in Fig. 3.9.

3.3.2.2 Pre-patterning the Catalyst using a Bilayer of Photoresist and PMMA

A 200 nm thick layer of PMMA (A4, MicroChem Corp.) was spin coated on a thermally oxidized Si substrate containing Ti alignment markers. The substrate was hard baked at 180^{o} C for 5 min to evaporate the solvents. Then, a negative photoresist (NR7-1500 PY) was spin coated at 4000 rpm for 1 min and baked at 120^{o} C for 1 min. The photoresist was exposed to UV through the photomask to define the desired pattern (e.g. 200 μm square features). The sample was then post-baked at 120 ^{o}C for 1 min and developed in resist developer (RD6) for 15 sec.

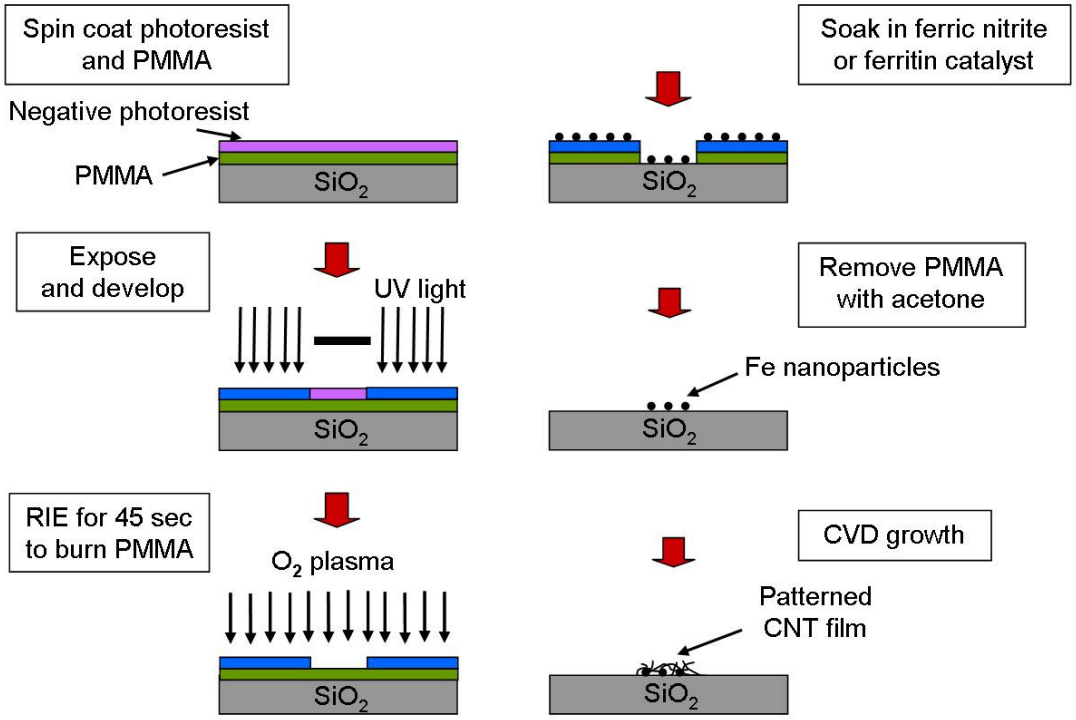


Figure 3.9 Schematic of the photolithography steps to synthesize patterned CNT thin films using prepatterning of the catalyst by a bilayer of photoresist and PMMA.

At this stage the PMMA layer is exposed through the opening in the photoresist layer. Patterned photoresist is used as a mask to burn the exposed PMMA by reactive ion etching (RIE) using O_2 plasma. The negative photoresist is also etched by RIE, but since the thickness of the photoresist (1.5 μm) is much larger than the thickness of PMMA (200 nm), the etching time can be optimized such that PMMA layer is etched completely before any appreciable etching occurs in the photoresist layer. The optimum etching time to burn a 200 nm thick PMMA layer was found to be 45 sec (power = 100 W, pressure = 200 mTorr). Now, the SiO_2 surface is exposed through the window in the bilayer of the photoresist and PMMA. The sample is soaked in either of the catalyst solutions, ferric nitrate or ferritin, to

deposit iron nanoparticles on the substrate. PMMA is lifted off using acetone, and CNTs are grown using CVD as described earlier. The patterned CNT film can be used to fabricate a device on the SiO_2 substrate. However, these patterned CNT thin films are not compatible (even after the surface treatment with release layer SAM) with the transfer printing process because oxygen plasma makes the SiO_2 surface too adhesive for CNTs. Therefore, a slight variation is introduced in the fabrication process to avoiding exposing the SiO_2 surface to oxygen plasma.

This can be done by keeping another sacrificial layer of photoresist underneath PMMA, as illustrated in Fig. 3.10. A positive photoresist (OiR-908 35) layer was exposed and developed to obtain a 200 μm square mesa of the photoresist on the SiO_2/Si substrate. A 200 nm thick layer of PMMA is spin coated on the sample and is soft baked at 90^o C for 3 min (hard baking is not compatible with the photoresist mesa underneath PMMA). Then another layer of a negative photoresist (NR7-1500 PY) is spin coated on PMMA and exposed through the same photomask aligned in the same position as in the previous exposure. After developing the photoresist we get a window in the negative photoresist overlaying the mesa of positive photoresist underneath PMMA layer. The exposed PMMA layer can be etched by using oxygen plasma. Now the SiO_2 surface is kept safe from oxygen plasma by the positive photoresist mesa. After PMMA is etched in the window, the positive photoresist is exposed to UV light without using any photomask. This makes the positive photoresist soluble in the developer (OPD 4262). Once the positive photoresist mesa is removed by the developer the wafer piece is ready for catalyst deposition. Either ferric nitrate or ferritin solution can be used to pattern the catalyst

particles. Finally, PMMA (and thus, negative photoresist) was stripped away by acetone and the patterned thin film of CNTs was grown by CVD.

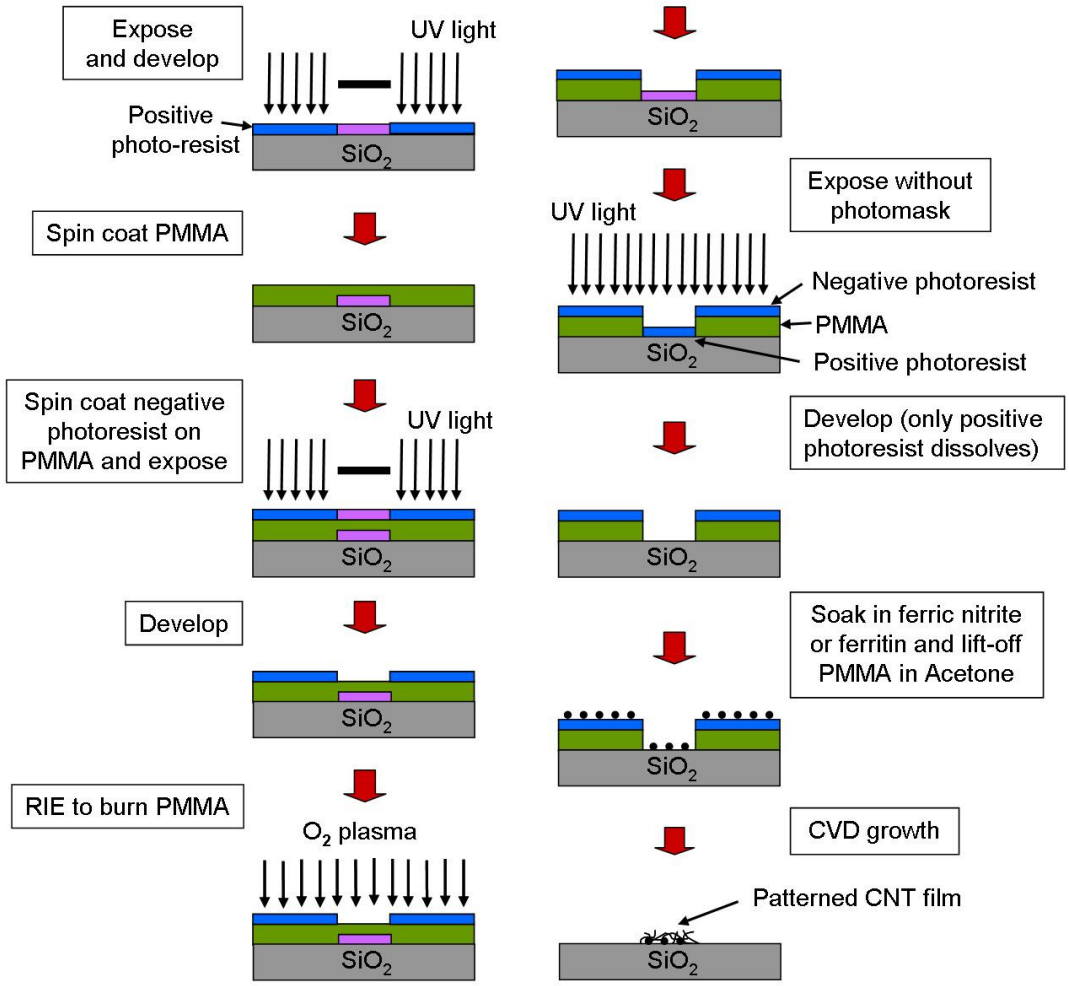


Figure 3.10 Schematic of the photolithography steps to grow patterned CNT thin films by prepatterning of the catalyst. An extra positive photoresist mesa underneath the PMMA keeps SiO_2 safe from RIE hence CNT thin films are compatible with transfer printing.

This method is rendered cumbersome by the complexity of photolithographic steps and by the necessity to align the mask precisely in two photolithographic steps. The edge roughness of CNT thin films is limited by the alignment capabilities in the

photolithography. Fig. 3.11 shows an optical image of the patterned windows in the bilayer of the photoresist and PMMA.

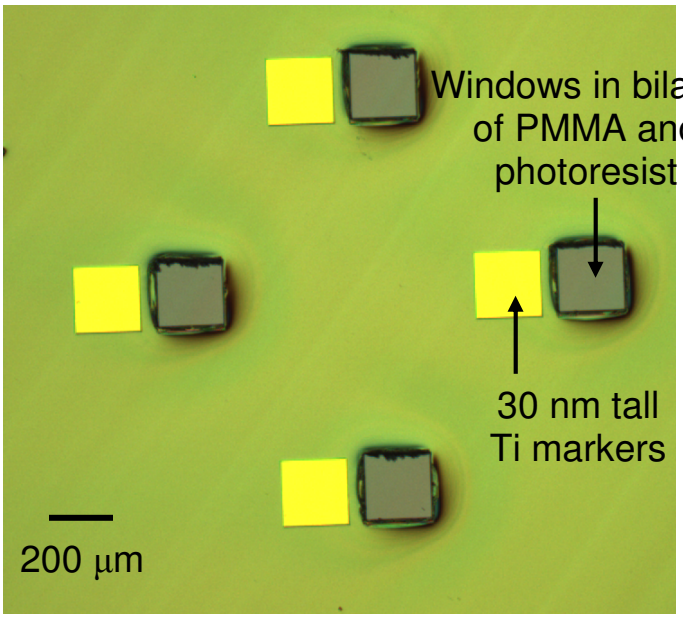


Figure 3.11 An optical image of a patterned bilayer of the photoresist and PMMA shows that the edges of the patterned bilayer are not very sharp due to the alignment limitations in the photolithography machine. Ti markers help in locating the position of CNT thin films for the device fabrication.

3.3.2.3 Growth of CNTs on Prepatterned Catalyst and Electrodes

Using the two patterning techniques discussed above, the patterned CNT thin films can be transferred to another substrate containing electrodes without any further chemical exposure of the CNTs. However, in order to make control devices on a SiO_2/Si substrate, the fabrication of electrodes on the patterned CNT thin film necessarily exposes CNTs to the processing chemicals. This can be avoided by first fabricating the electrodes on a SiO_2/Si substrate, followed by CNT growth from prepatterned catalyst. However, Au and Ti are not compatible with the high temperatures used in the CVD process. Pd is not a suitable alternative because it acts

as a catalyst for CNT growth and a forest of CNTs is seen growing on the electrodes. Thus, we used Pt electrodes for such devices. Pt electrodes were first fabricated by photolithography, followed by prepatterning of the catalyst over the device channel following one of the techniques described in Section 2.2. Fig. 3.12 shows a SEM image of one such device.

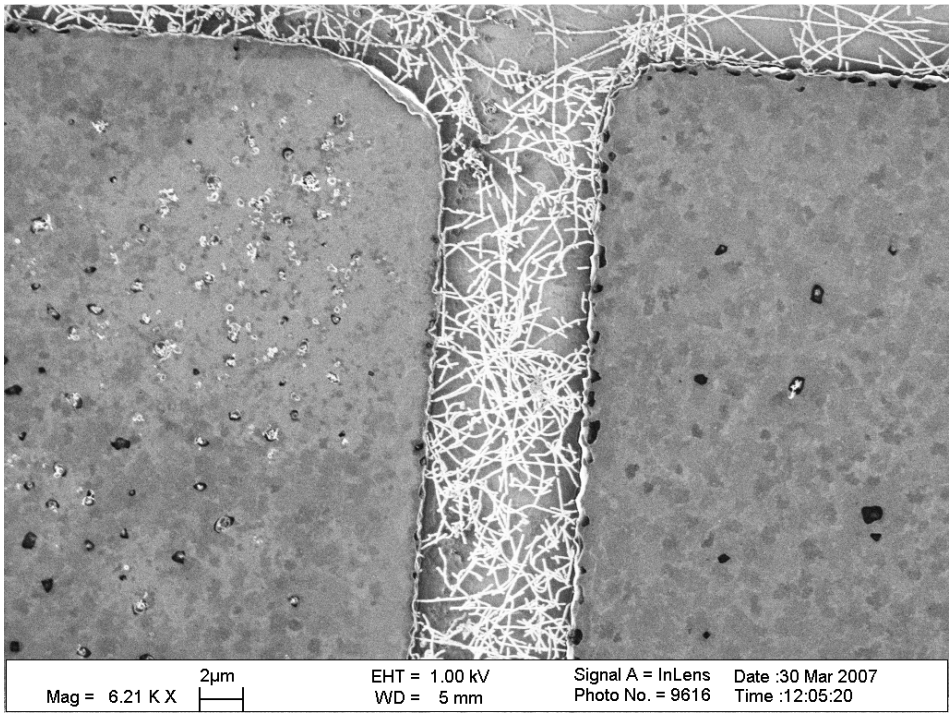


Figure 3.12 SEM image of a CNT thin film device fabricated by growing CNTs from pre-patterned catalyst on a SiO_2/Si substrate with pre-fabricated Pt electrodes.

3.2.3 Patterning CNT Thin Films using Transfer Printing

Since CNTs can be transfer printed onto a PET substrate [62, 85], it should be possible to pattern CNT thin films by transfer printing to a PET stamp. This process is illustrated in Fig. 3.11. The PET stamp is made by pressing a PET substrate against a rigid template at a raised temperature similar to nanoimprint lithography

[86] or a hot embossing process [87-89]. The first step is to fabricate a master Si template that can be used to pattern a PET template. For this, standard photolithography was performed on a Si substrate to create the desired patterns (200 μm square) of a photoresist (3.5 μm OiR 908-35) (Fig. 3.11(a)). The photoresist is used as a mask to etch the exposed Si surface by RIE, using a mixture of CHF_3 and O_2 plasma (power = 175 W, pressure = 40 mTorr). CHF_3 and O_2 plasma also etches the photoresist mask but at a slower rate (Fig. 3.11(b)). The photoresist was completely etched away in 70 minutes which produced a 22 μm tall Si stamp. Further etching affects all areas of the Si substrate equally, so the maximum height of the Si stamp produced by the above mentioned photoresist and RIE recipe is 22 μm. We made master templates consisting of 200 μm square, 22 μm (by etching for 70 minutes) and 16 μm tall (by etching for 50 minutes) mesas. Fig. 3.12(a) shows the height profile of a 16 μm tall Si stamp as measured with a Tencor profilometer.

The second step was to use the master template to fabricate a PET template. The surface of the master Si template was treated with (tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane for 2 hours. This SAM acts as a release layer and the adhesion of the Si surface to the PET is reduced. A PET stamp was made by pressing a PET substrate between the Si template and a plane Si substrate at 600 psi (300 psi pre-pressure), 170 ^{o}C for 20 min in a Nanonex imprinter machine (Fig. 3.11(c)). The pressure was first raised to 300 psi and the chamber was heated to 170^{o}C. Then, the pressure was increased to 600 psi and kept constant for 15 minutes. Heating the substrates without the pre-pressure resulted in occasional slipping of substrates due to thermal expansion. Fig. 3.12(b) shows a comparison between the height profiles of

PET stamps made with and without a planar Si substrate in the back during transfer printing. The planar Si substrate on the back of PET and pre-pressure are essential parts of the process to produce rectangular stamps with steeper side walls.

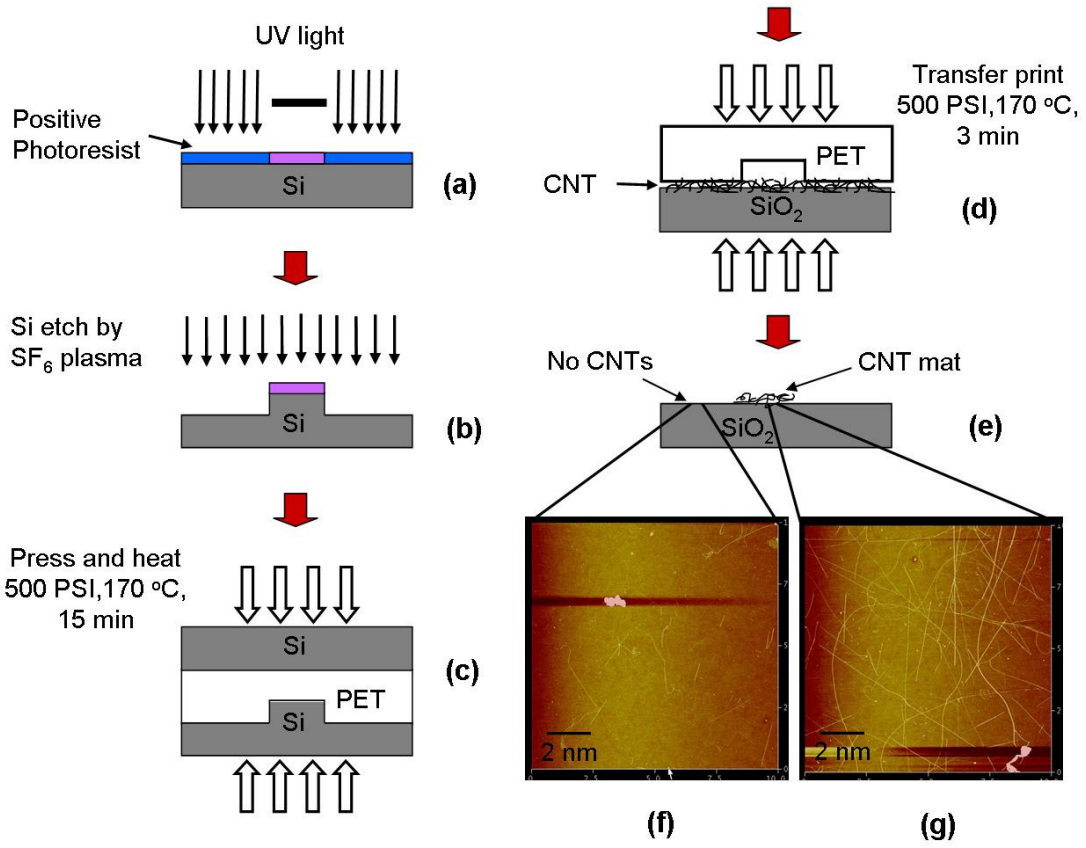


Figure 3.13 Illustration of steps for patterning CNT films using transfer printing. (a-b) Fabrication of Si template using photolithography and reactive ion etching. (c) Hot embossing against Si master template is used to make a PET template. (d-e) The PET template is used to pattern the CNT film resulting in CNTs remaining only in the patterned area as seen in the AFM images in (f) and (g).

It is worth noticing that the area of the bottom of the PET trench (160 μm to 180 μm square) is less than the area of the master stamp (200 μm square). This is due to relaxation of the strained PET while cooling down. PET stamps made from 16 μm-tall master stamps have steeper side walls than the PET stamps made from 22 μm-tall

master stamps, Fig. 3.13(a). Smaller stamps require less material to be displaced, which results in better embossing and hence truer negative copies of the master stamps. The area of the mouth of the trench (the actual area of CNT thin film to be patterned) in a 16 μm deep PET stamp surface was very close to 200 μm square. Thus, we used 16 μm deep PET stamps to pattern all CNT thin films used in making devices. A master template was used multiple times to make PET stamps. After every 4 or 5 printing steps, the surface of the Si stamp was treated with release layer.

The final step was to pattern the CNT thin film by transfer printing CNTs to the PET template (Fig. 3.11(d) and (e)). The CNTs transfer to the template wherever the raised area of the PET template contacts the SiO_2/Si surface and remain on the SiO_2/Si surface wherever the recessed area of the PET template does not contact the SiO_2/Si surface, as illustrated in Fig. 3.11(f) and (g). For this, transfer printing conditions that preserved the trench pattern in the PET template were determined. Printing parameters of 400 psi and 140 ^{o}C for 3 min were sufficient to preserve the template pattern and also to transfer print the CNTs to the PET. A planar Si substrate was placed on the back of PET template to distribute the pressure in the raised areas of PET. Without the planar Si substrate, the PET trenches collapsed under pressure as low as 100 psi. Fig. 3.13(b) shows the height profile of a PET stamp before and after the patterning of a CNT thin film. The depth of the PET trench has decreased from 16 μm to 3 μm. So, a PET stamp can only be used once. It was observed that increasing the depth of the original PET trench did not improve the depth of PET trench (3 μm to 8 μm) after one patterning step. That is another reason to consistently use 16 μm-tall master stamps throughout the experiments.

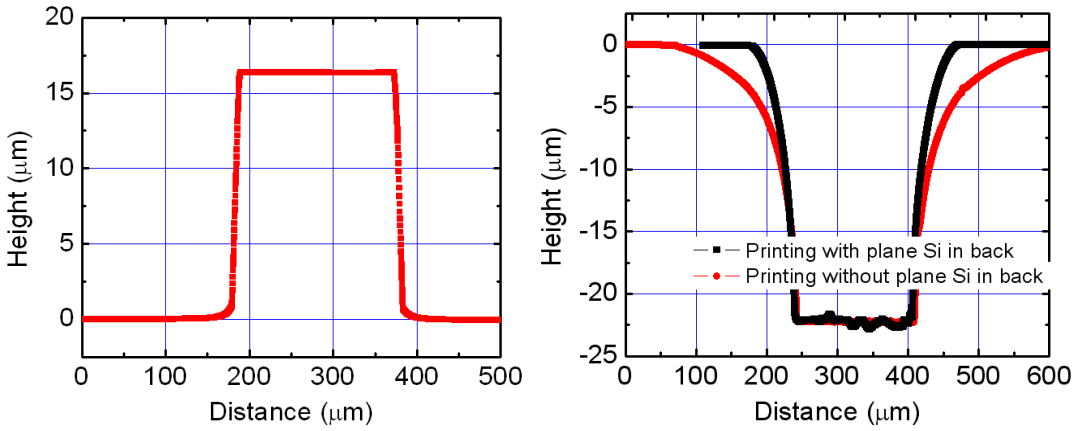


Figure 3.14 a) Height profile of a master 16 μm tall Si stamp. b) Comparison of height profiles of PET stamps with and without a plane Si substrate in the back of PET. Having blank Si in the back significantly improves the profile of the PET stamp.

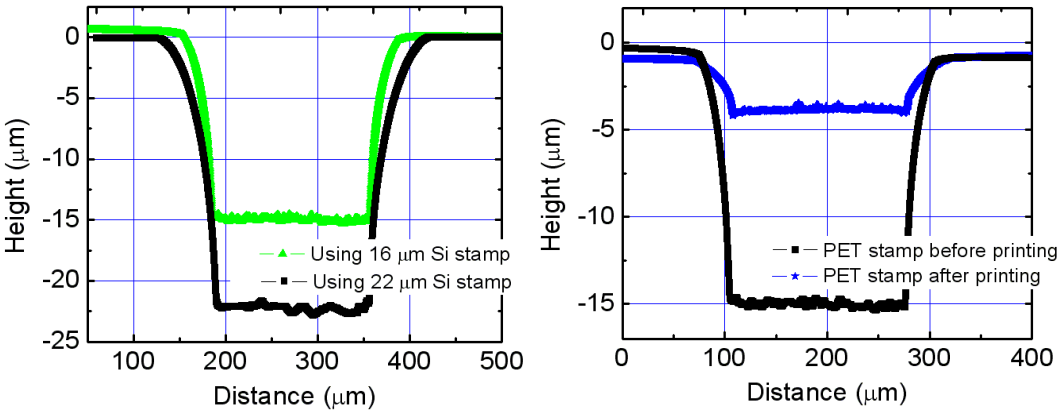


Figure 3.15 a) Profile of the PET stamps made from two master Si stamps of two different heights. A 16 μm tall Si stamp produced better PET stamps than 22 μm tall Si stamp. b) Height profile of a PET stamp before and after transfer printing. The depth of the trench reduced from 16 μm to 3 μm after one printing step.

This process does not expose the CNT films to any chemical processing or photolithography. The resolution of the patterned CNT film area is limited by the ability to create vertical walls in the trenches of the PET template and by the thermostability and sag of the template during transfer printing.

3.4 Comparison of Patterning Methods

The ideal method to pattern CNT thin films would be the one which meets all of the following requirements: (1) It should not expose the CNTs to any processing chemicals, (2) not limit the choice of materials in the device components, (3) have low edge roughness, (4) be compatible with transfer printing and finally should be as straightforward and simple as possible. Various patterning techniques were developed to meet these requirements. However, there is not one method which is better than all others in all aspects. Table 3.2 lists the various pros and cons of the CNT patterning methods discussed in this chapter. The patterning methods were discussed in this chapter in the chronological order in which they were developed. Each patterning method was developed to remove the limitations of the preceding method. Most of the devices reported in this thesis were fabricated using one of two patterning methods (#1 and #6 in Table 1). Method #1 is the most straightforward and useful to make a large number of devices. Moreover, this is the only method which could be used to pattern airbrushed CNT thin film electrodes (as discussed in Chapter 6). Patterning technique #6 consumes more time but produces pristine CNT thin film devices. Patterning technique #5 was used to study CNT thin film devices in PEEM (as will be discussed in Chapter 5).

Patterning methods	Advantage	Disadvantage	Transfer printing compatibility	Edge roughness
1. Photolithography (Fig. 3.5)	•Straightforward	•Exposure to chemicals	Yes, with RL treatment	Limited by photolithography < 1 μm
2. Prepatterning catalyst by photoresist (PR) (Fig. 3.7)	•No chemical exposure for printed devices	•Incompatible with $Fe(NO_3)_3$	Yes, with RL treatment	Limited by CNT length ~ 10 μm
3. Prepatterning catalyst by PMMA+PR bilayer (Fig. 3.10)	•No chemical exposure for printed devices •Compatible with ferritin & $Fe(NO_3)_3$	•Cumbersome •Poor resolution	Yes, with RL treatment	Limited by misalignment of two masks, > 10 μm
5. Prepatterning catalyst on Pt electrodes (Fig. 3.12)	•No chemical exposure for control devices •Compatible with ferritin & $Fe(NO_3)_3$	•Incompatible with transfer printing •Limited electrode material	No	Limited by CNT length ~ 10 μm
6. Transfer printing (Fig. 3.13)	•No chemical exposure for printed devices •Compatible with any catalyst	•Large edge roughness	Yes, with RL treatment	Limited by stamp profiles ~ 15 μm

Table 3.2 A comparison of various CNT thin film patterning methods discussed in this chapter.

Chapter 4 : Transport and 1/f Noise in Suspended Carbon Nanotubes

The direct contact between carbon nanotube (CNT) and the dielectric layer in CNT field effect transistors (CNT-FETs) affects both the transport[74, 90] and noise characteristics[91]. Thus, suspended CNT-FETs, in which direct contact with the dielectric is absent, have the potential for improved control and performance. However, fabrication methods for suspending CNTs demonstrated to date are arduous, and either involve harsh chemical treatment, or severely limit the materials which may be used.

One approach is to selectively etch the dielectric layer underneath the CNTs to produce a suspended device[91]. This technique requires critical-point drying, and exposes the CNTs to harsh chemical processing. Another approach uses chemical vapor deposition (CVD) to grow CNTs on pre-patterned electrodes with trenches between the electrodes[74, 90, 92]. This method limits the substrate and electrodes to materials compatible with high temperature growth conditions. In this chapter we present a simple, fast, and scalable method of creating high-quality suspended CNT-FETs using a printing/lamination process. The technique does not expose the CNTs to any chemical treatment, and could be generalized to a wide variety of substrates and electrodes. The resulting FETs have improved transport and low frequency noise characteristics, and allow greater control of contacts to the source and drain.

4.1 Fabrication of the Devices

The fabrication scheme involves transfer printing nanotubes[85, 93] from a substrate covered with CVD-grown nanotubes to a second substrate with pre-patterned metal electrodes, as shown in Fig. 4.1(a). The source-drain electrodes (50 or 90 nm Au on 10 nm Ti, rms roughness 0.87 nm) are fabricated by a first step of photolithography on 300 nm thermal oxide with a heavily doped Si substrate as a global back gate. Then, a second photolithography step is carried out to fabricate pillars (500 nm Au on 10 nm Ti, see schematic in Fig. 4.1(b)) on the inner edges of the electrodes. On a separate SiO_2 substrate, a CNT thin film (~ 150 CNTs/100 μm^2) is grown by a CVD process using an aqueous ferritin solution (0.5 mg/ml) as the catalyst [43]. The resulting nanotubes are mostly single-walled with average diameter around 1.4 nm. The nanotube-covered substrate is pressed against the substrate with the electrodes at 300 psi and 90 ^oC for 3 minutes (Fig. 4.1(a)) using a nano-imprint machine (Nanonex NX2000). A SEM micrograph (Fig. 4.1(c)) of the electrodes after printing shows bright contrast for a suspended CNT. A CNT lying on SiO_2 across the channel and two short CNTs that did not bridge across the channel show darker contrast due to charge transfer[94]. A SEM image of the original CNT-covered SiO_2 substrate following printing (Fig 4.1(d)) shows 100% removal of CNTs in the region that was pressed into contact with the Au electrodes and approximately 4% transfer of CNTs in the region of the channel between the electrodes. The pillars on the electrodes are essential to transfer printing. Their protrusion ensures conformal contact between the rough Au surface and the CNTs, and their size increases the local force between the substrates by reducing the area of contact.

Increasing the height of the pillars causes decreased capacitance of the overall gate dielectric. Decreasing the height below 500 nm results in more CNTs touching the SiO_2; for example, with shorter 250 nm thick Au/Ti pillars, most of the CNTs fall on the SiO_2 surface. This configuration was used to make control FETs with a single CNT lying on SiO_2 in the channel. Decreasing the thickness of pillars further results in reduced transfer of CNTs to the pillars.

As mentioned earlier, imaging contrast in SEM offers a straightforward method to distinguish between suspended CNTs and CNTs touching the SiO_2 surface. We took SEM images of tilted samples to confirm this. The SEM image in Fig. 4.2(a) shows bright contrast for a suspended CNT with the device chip normal to the electron beam. Fig. 4.2(b) shows a SEM image of the same device by tilting the normal axis of the sample at 70^o angle with respect to the electron beam. A red dotted line is drawn parallel to the CNT as an aid to the eye. It can be seen that the CNT is indeed suspended. The SEM image in Fig. 4.2(c) shows dark contrast for a CNT lying on the SiO_2 surface. The SEM image of the tilted sample in Fig. 4.2(d) shows that the CNT is indeed lying on the dielectric surface. We performed quick SEM imaging at high scanning speed to identify the suspended CNTs to avoid excessive charging of the dielectric layer.

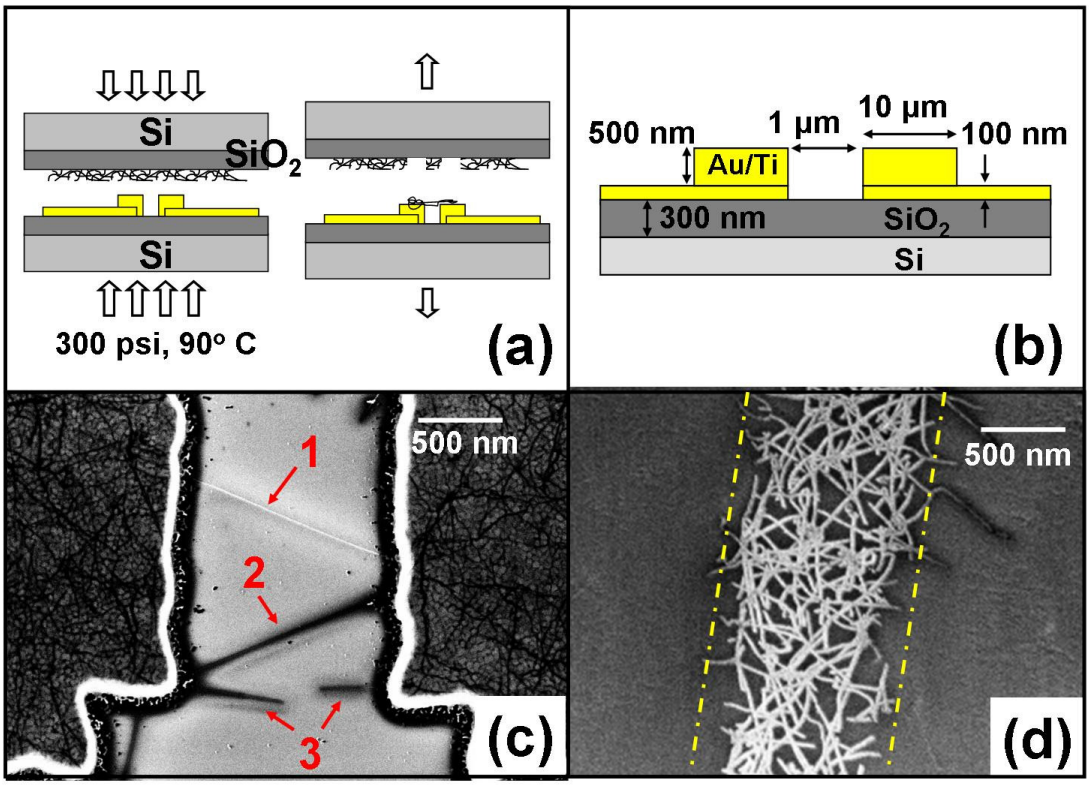


Figure 4.1 a) CNT covered substrate is pressed against electrodes at 300 psi, 90 ºC for 3 minutes to transfer CNT in suspended configuration. b) Optimized dimensions of electrodes; the width of pillars (not shown) is 5 µm. c) SEM image of a device containing one suspended nanotube (indicated by arrow 1), one nanotube lying on SiO_2 (arrow 2) and two short CNT falling into the channel (arrow 3). d) SEM image of CNT covered substrate showing residual nanotubes after printing. Dashed line indicates the contact positions of the Au electrodes during printing.

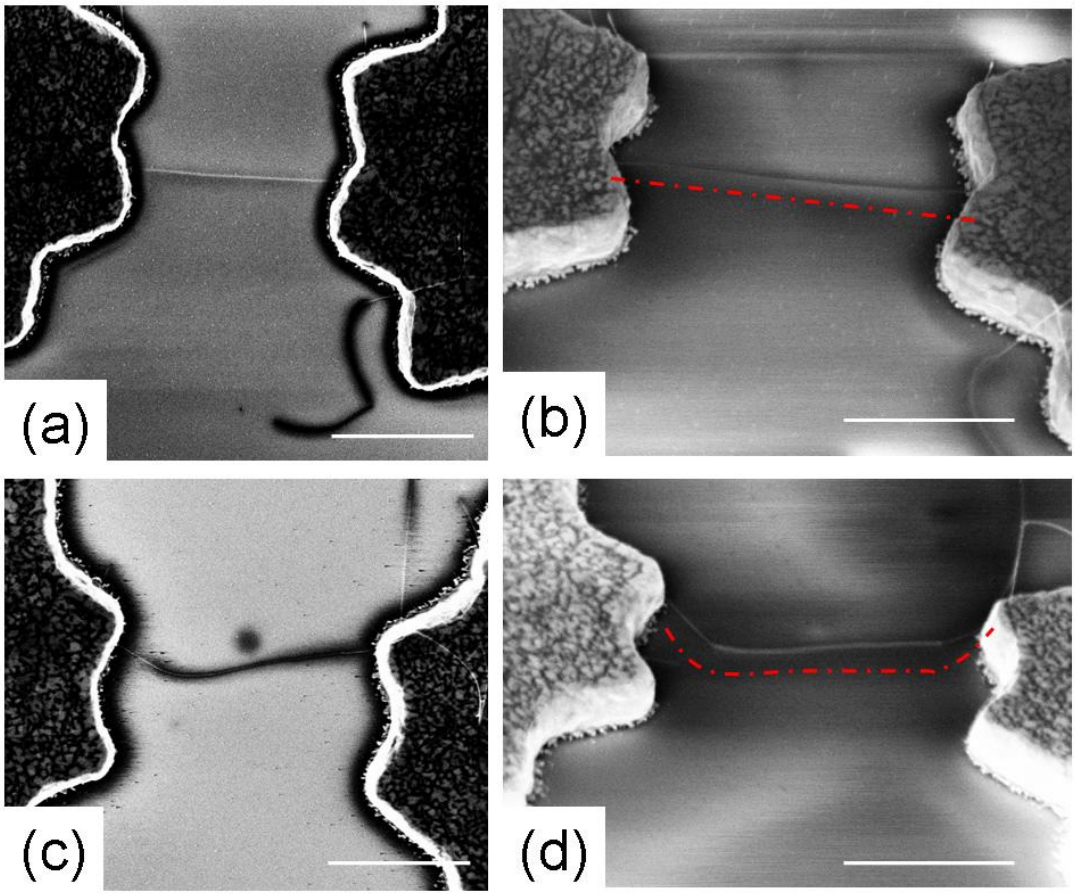


Figure 4.2 a) SEM image of a suspended CNT device. Suspended CNT shows bright contrast compared to the background from SiO_2 surface. b) SEM image of the sample tilted at an angle (70^o) with respect to electron beam shows that the CNT is indeed suspended. Red dotted line is an aid to the eye. c) SEM image of a control device. d) SEM image of the tilted sample shows that CNT is touching the SiO_2 surface. 1 μm long white scale bars are shown in bottom right corner of all the images.

The number of suspended nanotubes in each device depends on the channel length (L) and the original density of nanotubes on the growth substrate. The yield of devices with a single suspended CNT across the channel was optimized to 20% by making the channel width and channel length 5 μm and 1 μm, respectively. The schematic in Fig. 4.1(b) shows the optimized geometry of pillars and electrodes. Three different growth densities (~ 35 CNT/100 μm^2, ~ 150 CNT/100 μm^2 and ~ 300

CNT/100 μm^2) of as-grown CNT thin films were tested, with 150 CNT/100 μm^2 resulting in the best yield of single-CNT devices. For these parameters, 60% of devices had multiple CNTs across the channel, whereas 20% of the devices had no CNTs. Both metallic and semiconducting nanotubes are observed following printing, and those with good semiconducting properties are used in the device characterization.

4.2 Versatility of the Fabrication Method

The transfer method offers facile control over the density of the suspended CNTs in a device. This can be achieved by two methods. The density of suspended CNTs can be controlled by varying the growth density of CNTs in the transfer substrate. Fig. 4.3(a) shows a SEM image of a single suspended CNT printed from a CNT thin film with density ~ 150 CNT/100 μm^2. Fig. 4.3(b) shows 6 suspended CNTs printed from a CNT thin film with density ~ 300 CNT/100 μm^2. Of course, not all the devices fabricated using 150 and 300 CNT/100 μm^2 show 1 and 6 suspended CNTs, respectively. Fig. 4.3(a) and (b) show 'typical' devices for illustrative purposes. The number of suspended CNTs per device can also be increased by repeating the transfer printing step multiple times. Figs. 4.3(c) and (d) show a device where the number of suspended CNTs was increased from 3 to 16 after 5 printing steps from a CNT thin film with density ~ 150 CNT/100 μm^2.

The nanotube-covered SiO_2 substrate can be used several times for printing because the actual transfer of the CNTs occurs in the small area of the pillars, compared to the total area of the chip. If a device is destroyed during measurements,

another device can be fabricated on the same electrodes by repeating the printing step. Using this procedure, device characteristics can be tested for multiple configurations on the same electrode set. Furthermore, the printing process is also scalable to produce a large number of devices, as illustrated in Fig. 4.4. Fig. 4.4(a) shows an optical image of a chip containing 51 electrode sets, onto which CNTs were simultaneously printed. Fig. 4.4(b) shows a zoomed-in optical image of the devices and Fig. 4.4(c) shows a SEM image of one such device. Of the 51 sets, 10 devices were observed to have a single suspended CNT, consistent with the expected 20% yield. In this case, a printing step takes 8 minutes to produce on average 10 suspended single-CNT devices, and the process could be further scaled up by printing on multiple chips simultaneously. Since our method is based on pressure-induced attachment of nanotubes to metal electrodes, suspended CNT-FETs can potentially be made on any robust substrate with a sufficiently malleable metal as the pillar-electrodes. We have fabricated suspended CNT-FETs on SiO_2 and sapphire substrates using Au and Pd as electrodes.

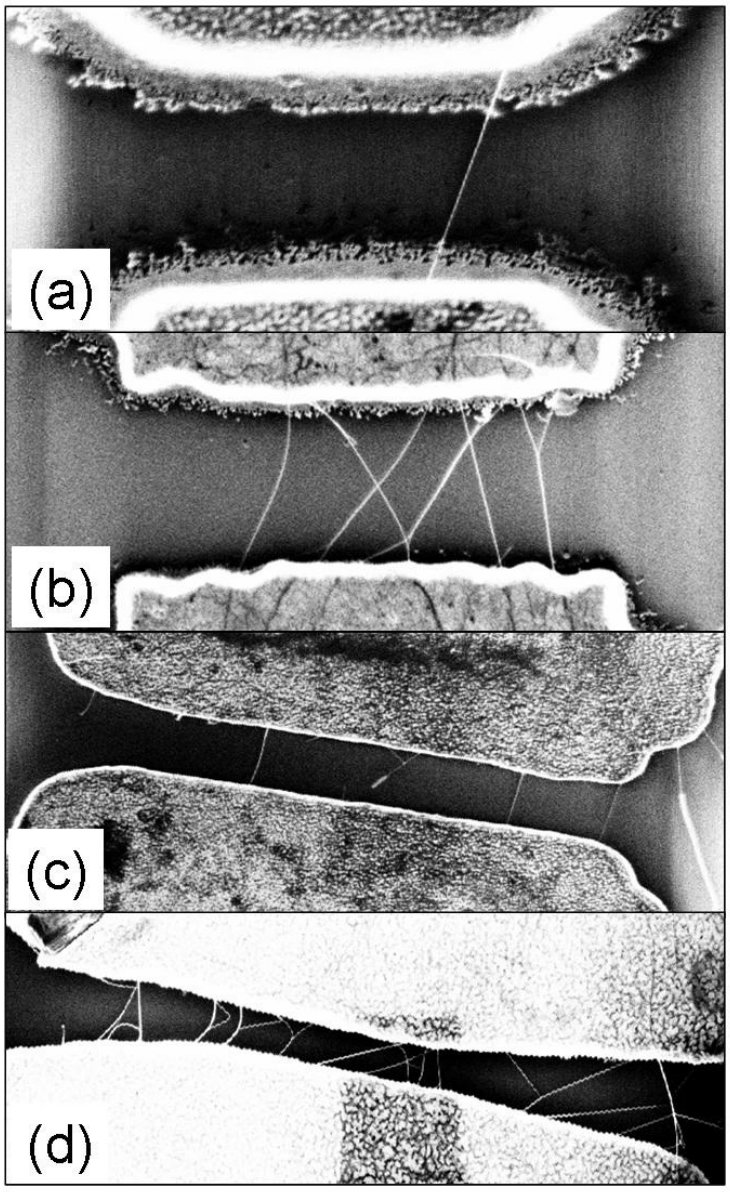


Figure 4.3 a) An SEM image of a single suspended CNT printed from a CNT thin film with density ~ 150 CNT/100 μm^2. Channel width, W of electrodes is 5 μm. b) Six suspended CNTs were printed from a denser CNT thin film (~ 300 CNT/100 μm^2). c) Three suspended CNTs were printed on a device with W = 10 μm from a CNT thin film with density ~ 150 CNT/100 μm^2. d) 16 suspended CNTs were obtained on same electrodes by 5 transfer printing steps from the same CNT thin film as a transfer substrate. Channel length, L = 1 μm is same in all the images.

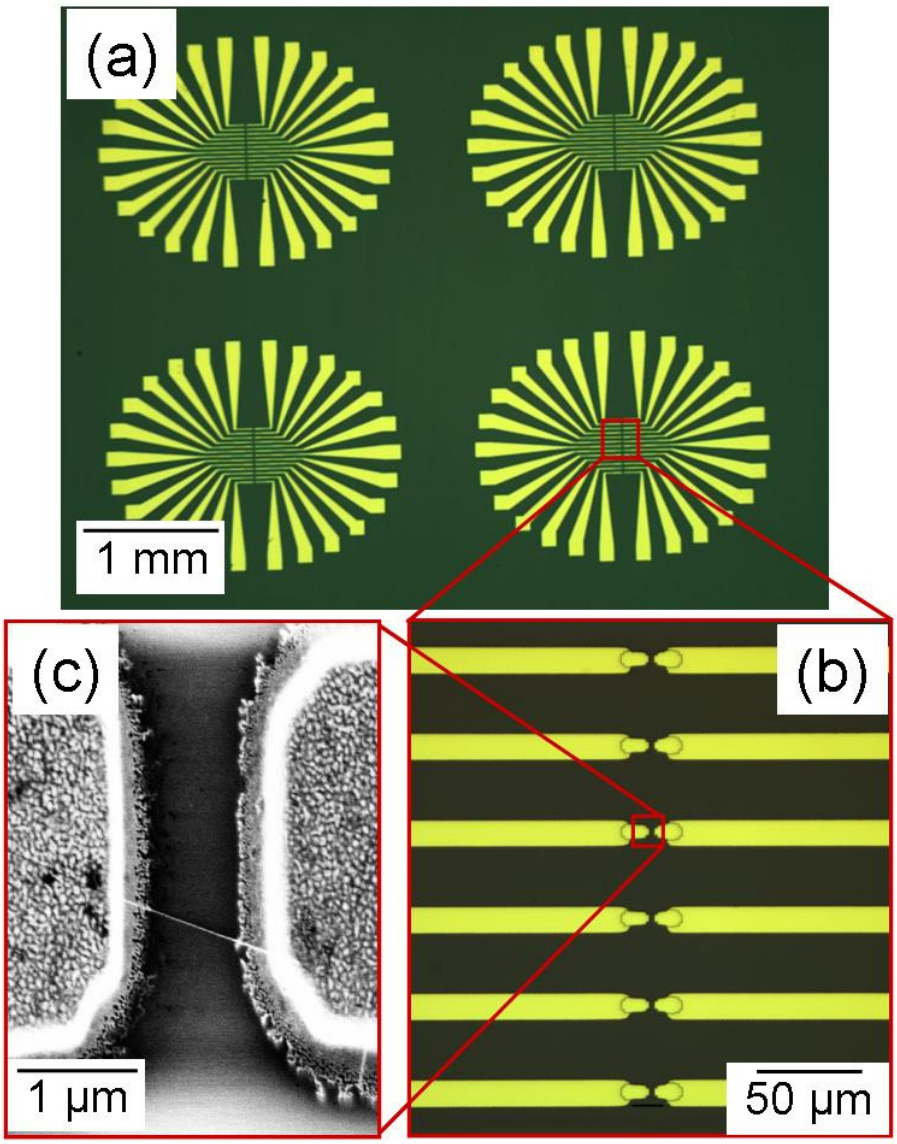


Figure 4.4 a) An optical image of a chip containing 51 electrode pairs. b) A zoomed-in optical image of few devices. c) An SEM image of device with a single suspended CNT.

4.3 Transport Measurements

The quality of the printed suspended CNT-FET and control FET (with a single nanotube in contact with the SiO_2) was tested using transport measurements at room temperature (Desert Cryogenics TT-Prober System) in air as well as in vacuum (5 x

10^{-6} Torr). In Fig. 4.5, transfer characteristics of a suspended CNT-FET are compared with that of a control FET. The vertical axis is normalized to the on-state conduction (at $V_g = -30$V) for both the devices. Suspended CNT devices have lower sub-threshold swing (region where current grows exponentially with drain bias) (> 1.3 V/decade), lower on-state conduction (< 1 μS), greater ambipolarity, smaller threshold voltage (gate voltage of minimum conductance), and less hysteresis than control CNT-FETs on SiO_2 (which are similar to those reported in literature[29]), as shown in Fig. 3(a). The differences likely result from a lack of doping from the substrate and/or reduced gate capacitance in suspended devices compared to control devices, as discussed below. This behavior of suspended CNTs was consistently observed in 8 out of 11 devices.

It has been noted previously that as-fabricated CNT-FETs on SiO_2 are p-doped, while suspended CNTs are nearly intrinsic[95]. Doping via the dielectric layer may also be removed by high-current annealing[96]. In this latter case, undoped CNT-FETs showed greater ambipolarity, smaller threshold voltage, and reduced on-state conductance, similar to the results presented here and consistent with our suspended CNT-FETs being undoped. Hysteresis is also reduced in the suspended CNT-FET as compared to the control device, consistent with hysteresis being due to charge traps on or in the dielectric[30, 33, 97]. Hysteresis in CNT devices is discussed in more details in Appendix B.

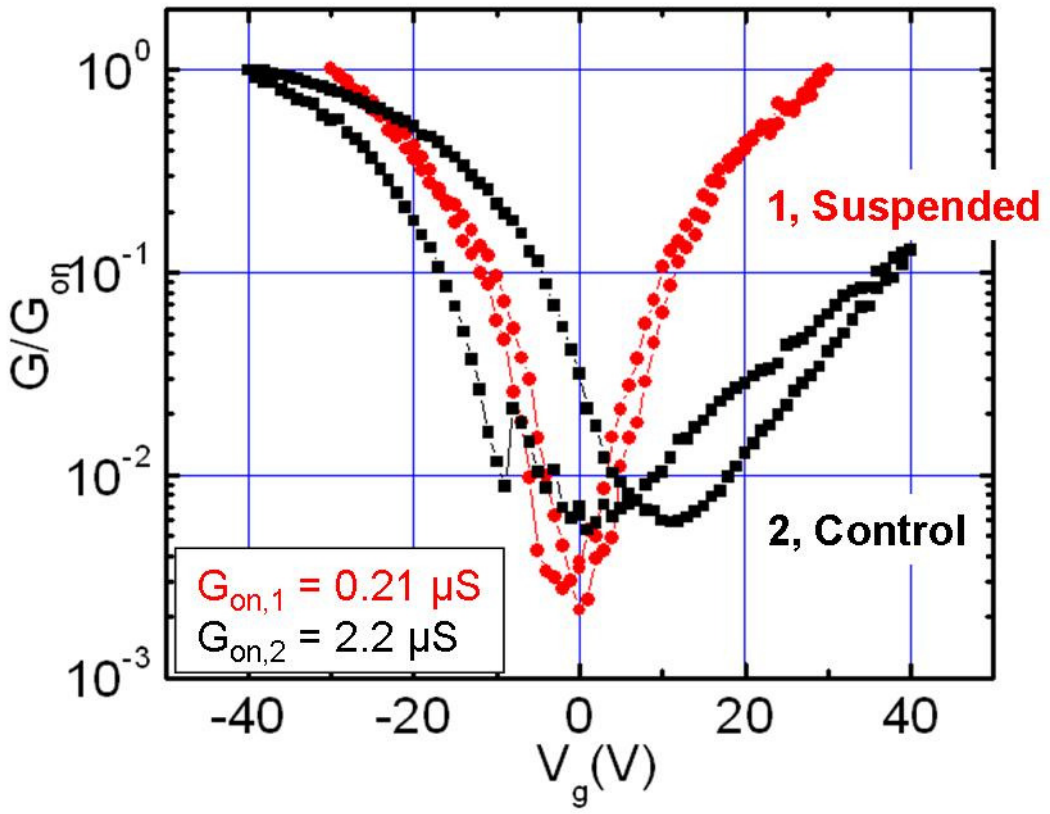


Figure 4.5 Transfer characteristics of a suspended CNT-FET (1) is compared with transfer characteristics of a control CNT-FET (2). Conductance in y-axis is normalized to the 'on' state conductance G_{on} at $V_g = -30$ V (shown in the box) for both the devices.

The electrostatics of any suspended CNT device present some intrinsic issues with gate-coupling. Simulations of electric potential were done using Poisson Superfish[98], see Fig. 4.6(a). Supporting information and code of POISSON-SUPERFISH program is provided in Appendix C. Pink lines represent equi-potential surfaces when the gate is biased at 50 V. Fig. 4.6(b) shows the electric potential along the length of a CNT in three different geometries; suspended CNT (1), control CNT (2) and standard top-electrode CNT-FET (3). Line 2 overlaps line 1 near the contacts and overlaps line 3 in the middle of the channel. Thus, the contacts of both control (black line, 2) and suspended CNT-FETs (red line, 1) are only weakly

coupled to the gate modulation, whereas the contacts in a standard top-electrode CNT-FET (blue line, 3) are strongly coupled. The simulations also confirm that suspended CNTs are more weakly coupled to the gate than control CNTs and standard top-electrode CNT-FETs, where the CNTs are physically closer to the gate. In this particular case (V_g = 50), the suspended CNT experiences 2 V (near contacts) to 7 V (middle), whereas the control CNT experiences 2 V (near contacts) to 23 V (middle). The decreased capacitance of the suspended CNT devices results in lower conduction (<1 μS) and higher sub-threshold swing (> 1.3V/decade) compared to that reported in literature for CNT-FETs on SiO_2[29, 96]. The fact that Schottky barriers at the contacts are relatively less influenced by gate modulation (due to electrode screening) in the case of both control and suspended CNT-FETs[99] may also play a role in the reduced on-conductance.

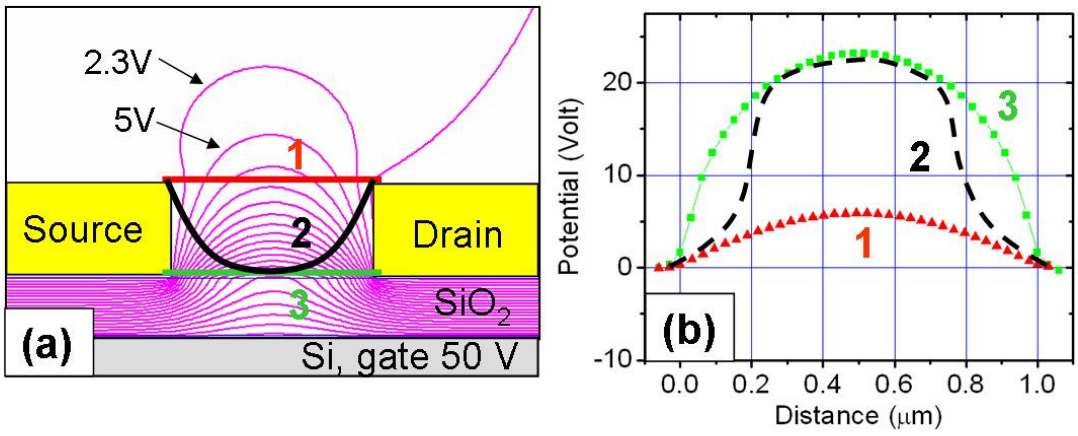


Figure 4.6 a) Simulations of equi-potential lines using Poisson-Superfish [98]. Three possible positions of CNTs are suspended (1), control (2) and top-electrode (3). b) Potential along CNTs in three different geometries is plotted with respect to distance in device channel (L = 1 μm). The influence of the CNT is not included in these simulations.

4.4 Introduction to 1/f Noise

There are four major sources of noise in electronic devices. In a device with resistance *R*, spontaneous current fluctuations can arise from thermal fluctuations. The current fluctuation is called thermal or Johnson noise. Thermal noise is given by $S_I(f) = 4kT/R$ at zero bias, where S_I is the current noise power per unit of frequency (A^2/Hz), *k* is Boltzmann constant, *f* is frequency and *T* is temperature [100]. Thermal noise is independent of frequency and is also called "white" noise. It is always found in a device showing diffusive conduction process. When a device is biased, current fluctuation can also occur due to randomly generated electrons across the potential barriers in the channel. This noise is called shot noise and is also frequency-independent. Shot noise is given by $S_I(f) = 2eI$, where *e* is charge of an electron and *I* is the current [100]. Another source of noise in semiconductors is random generation-recombination processes between the bands and traps. The fluctuation in the number of free electrons in the conduction band causes conduction fluctuation (S_G). It is given by $S_G(\omega) = 4\tau/(1+\omega^2\tau^2)$, where τ is the relaxation time of the trap and ω is angular frequency [100].

There is, however, another kind of noise in electronic devices called 1/*f* noise or "pink" noise. The striking feature of 1/*f* noise is that the power spectral density of conduction fluctuation is inversely proportional to frequency over a large range of frequency. 1/*f* noise has been observed in a wide variety of physical systems, such as vacuum tubes, semiconductors, metals, and SQUIDs. Unlike other noise processes, no universal physical phenomenon has been attributed to the source of 1/*f* noise. The

search for 'universality' in 1/*f* noise processes has kept this field active for the last 4 decades. The most commonly-accepted theory on the origin of 1/*f* noise, proposed by Dutta and Horn [101], relates 1/*f* noise to a broad energy spectrum of fluctuators. For example, a broad spectrum of trap energies can give rise to 1/*f* spectra in generation-recombination noise. A historical overview of 1/*f* noise can be found in a review article by Weissman [102]. A strictly phenomenological equation, proposed by Hooge [100, 103], is used to describe 1/*f* noise as

$$S_I = \frac{AI^{\beta}}{f^{\alpha}}, \qquad 4.1$$

where S_I is noise spectral density of current fluctuations, $\beta = 2$, $\alpha \approx 1$, and $A = \alpha_H/N$. The dimensionless quantity α_H is called Hooge's constant and N is the number of carriers in the device. The value of α_H has been reported to be in range 10^{-3} to 10^{-6} for commonly used semiconductors Si, Ge and GaAs [100]. At some low frequency, noise must stop following the 1/*f* behavior, because otherwise the total noise power integrated over all frequencies will diverge. The noise must also have a slope steeper than – 1 at high frequency in order for the Fourier transform to have a finite value. However, to date, experimentalists have not been able to observe the expected deviations at these two extremes of frequency spectrum.

4.5 1/f Noise in CNTs

CNTs are unique electronic systems to study 1/*f* noise in 1-dimensional materials. Initially, CNTs were expected to have large 1/*f* noise as compared to their higher dimensional counterparts because all the carbon atoms residing at the surface of a CNT are free to interact with the environment. The presence of a defect on a 1-

dimensional channel can strongly affect conduction. The earliest 1/*f* noise experiment was done in CNTs thin films by Collins et al [104]. The value of A (α_H) was reported to be 10^{-7} (0.2) around 10 orders (3 orders) of magnitude larger than that of a typical resistor. It seemed to agree with current opinion, but further analysis pointed out the erroneous assumption of taking the number of carriers equal to the number of atoms in a CNT. Later investigations [104-110] of devices with the standard CNT-FET configuration (e.g. CNTs in contact with the oxide dielectric layer) have shown noise levels with an effective Hooge's constant of respectively $\alpha_H = 2 \times 10^{-3}$ and 9.3×10^{-3} for diffusive transport and $\alpha_H = 7.4 \times 10^{-4}$ for ballistic transport ([107], [106], [105]).

Here, we aim to study the influence of the dielectric layer on 1/*f* noise in CNTs. For that purpose, the current noise spectral density (S_I) was measured for suspended CNT-FETs and control devices under ambient conditions, as well in vacuum (5×10^{-6} Torr). Measurements were done in the linear region ($V_d << |V_g - V_{th}|$), at fixed source-drain bias, as a function of gate voltage. Gate voltage was supplied by dc batteries to minimize external fluctuations. Current signal from devices was amplified using an Ithaco 1211 Low Noise Current Preamplifier (DL Instruments) (rise time = 0.01 sec, suppression = 10^{-3}). Drain voltage (drain current) was controlled (measured) by a BNC 2090 DAQ. Drain current fluctuations were measured by a SR760 FFT Spectrum Analyzer (Standford Research Systems). Measurements were taken in frequency range 5 Hz to 1.5 kHz in the steps of 3.7 Hz. Sensitivity of Ithaco preamplifier was varied to bring the output voltage within reliably measureable range for DAQ board (i.e. between 0.5 to 5 V). A schematic for experimental set-up is shown in Fig. 4.7(a).

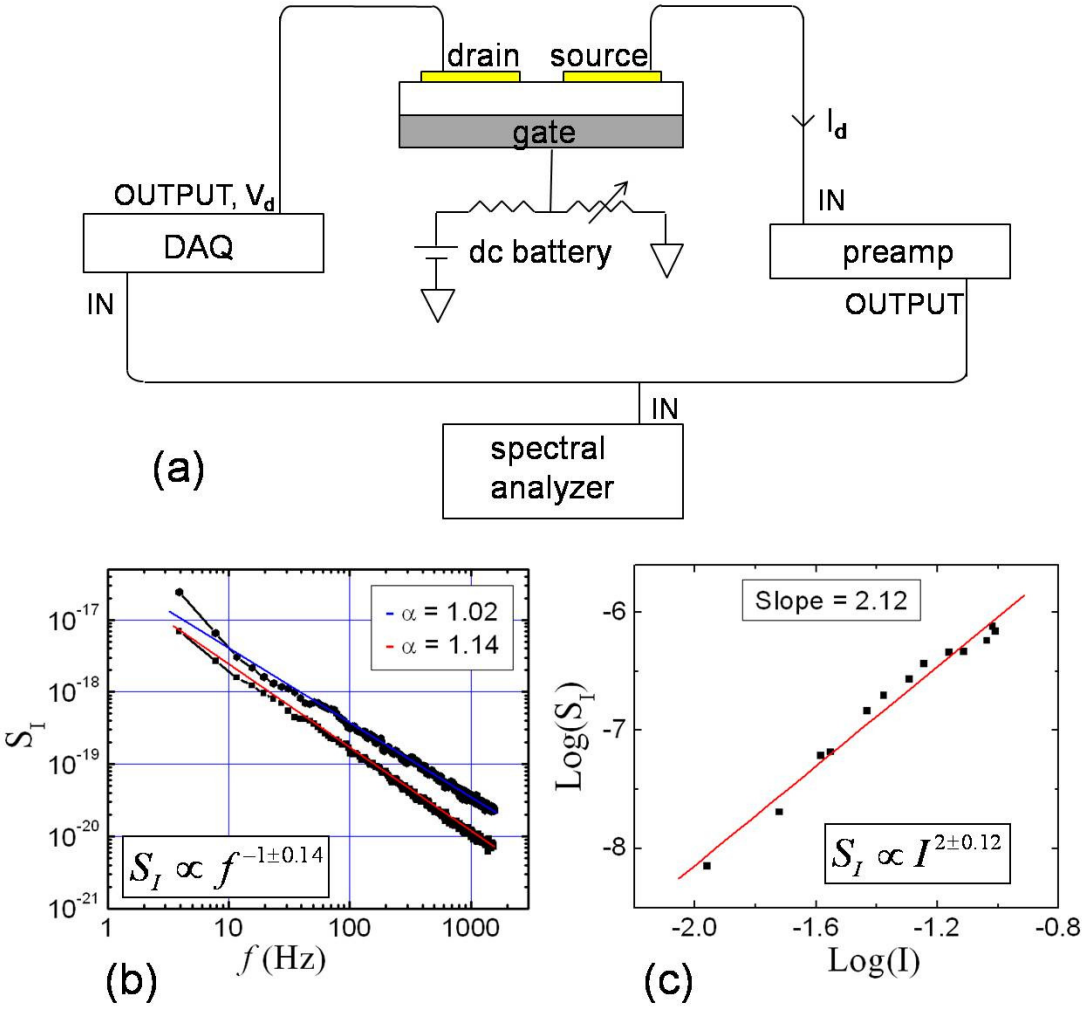


Figure 4.7 a) Schematic of noise measurement set-up. b) Noise spectral density (S_I) is plotted against frequency for two suspended CNT devices with exponent, α, nearest (1.02) and furthest (1.14) from expected value of 1. c) The plot of log(S_I) against log(I) with slope 2.12.

In Fig. 4.7(b) noise spectral density (S_I) is plotted as a function of frequency. The plot shows two cases of suspended CNTs with the value of α closest and furthest from the expected value of 1. Control CNT devices also showed 1/f behavior as expected. Fig. 4.7(c) shows the most deviant case of a suspended CNT device where S_I is proportional to $I^{2.12}$. Thus the dependence of S_I on frequency and current follows the expected Hooge's law behavior with $\alpha = 1 \pm 0.14$ and $\beta = 2 \pm 0.12$ for both the

suspended and control CNT-FETs, where the error corresponds to the most deviant case. Fig. 4.8 shows the frequency dependence of S_I/I^2 for two cases of suspended CNT devices and one control device at V_d = 50 mV and V_g = – 30 V. The noise power S_I/I^2 for the suspended CNT-FETs is 3 to 10 times smaller than that of the control device; this is especially surprising since the reduced gate capacitance means *smaller N* for the suspended device, which would give *larger* noise by Hooge's law. Moreover, the noise power (3 x 10^{-8} to 8 x 10^{-9} at 100 Hz) is also smaller than that previously reported for suspended CNTs prepared by post-etching (~10^{-7} at 100 Hz)[91].

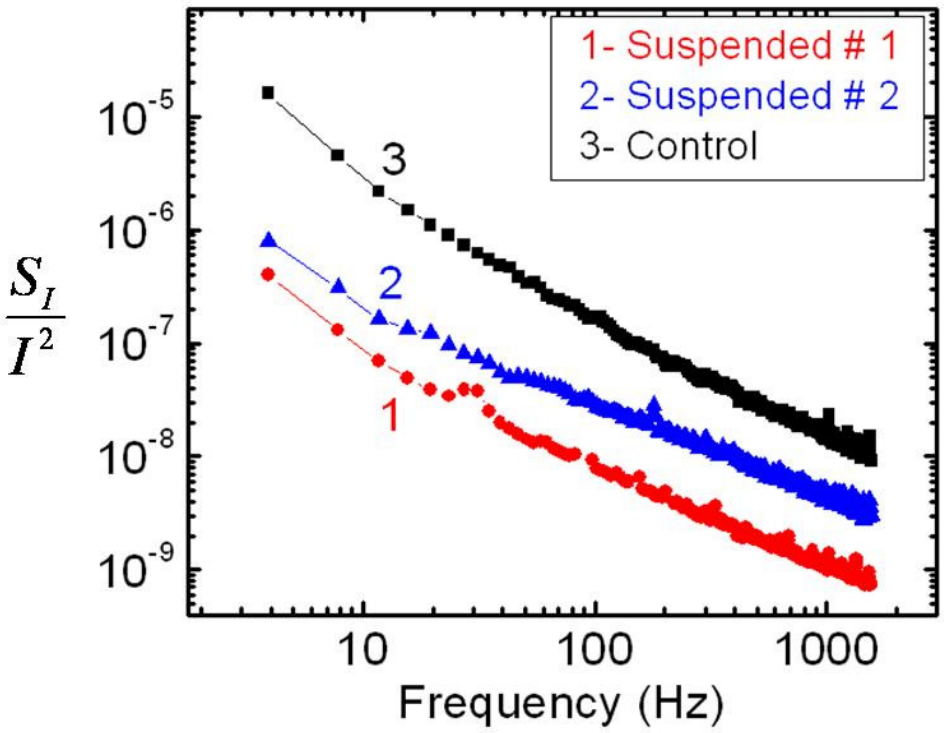


Figure 4.8 Noise power as a function of frequency for a control device and two extreme cases of suspended CNT-FETs at V_d = 50 mV at V_g = – 30 V, i.e. when devices are fully turned on. The two suspended CNT devices show 3 and 10 times less noise power as compared to the control device.

In this discussion, we compared the quantity I^2/S_I for suspended and control CNT devices and concluded that suspended CNTs have up to an order of smaller noise magnitude. However, it is essential to establish the validity of this comparison between two kinds of devices with different resistance. Suspended and control CNT devices have similar kinds of electrode contacts, but the contact resistance is expected to have some variation from device to device. Preliminary work on the impact of contact resistance in 1/*f* noise in ballistic CNT FETs have been reported in Appenzeller et al [105]. For fuller understanding, the role of contacts on transport properties of CNT FETs should also be considered [111]. A detailed treatment of the effect contact resistance on noise is out of scope of this research, but here we point out some of the consequences of variation in the total resistance of the device.

Let's model variation in the device resistance as an addition of an external resistance in series with the device. We consider both the cases: when the external resistance does and does not have its own resistance fluctuations. Even when a "quiet" resistance is assumed not to have its own resistance fluctuations, it could affect the measured noise power (S_I/I^2). First, consider a device with resistance R and fluctuation amplitude $\delta R \ll R$ (Fig. 4.9(a)). The device current can be expressed as

$$I_1 = \frac{V}{R+\delta R} \sim \frac{V}{R}\left(1-\frac{\delta R}{R}\right) = I_0\left(1-\frac{\delta R}{R}\right) = I_{1,0} + \delta I_1 \qquad 4.2$$

where $I_{1,0} = I_0$.

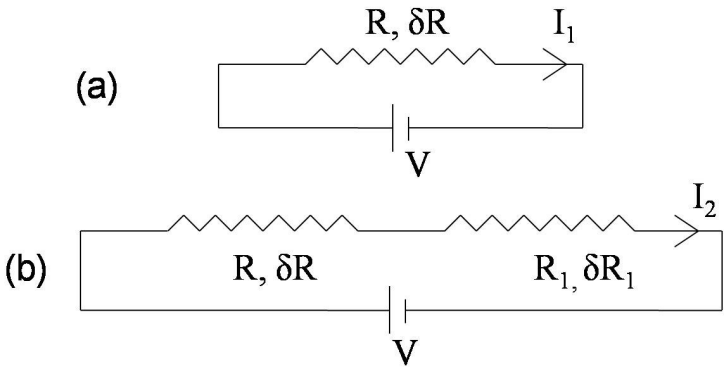


Figure 4.9 a) Circuit diagram of a device with resistance R with resistance fluctuations δR. b) An external resistance R_1 with resistance fluctuations δR_1 is connected in series with the device.

When a resistance $R_{1,}$ with fluctuations $\delta R_1 << R_1$, is connected to the device in series (Fig. 4.9(b)), the device current (I_2) can be expressed as

$$I_2 = \frac{V}{R + R_1 + \delta R + \delta R_1} \sim \frac{V}{(R + R_1)}\left(1 - \frac{\delta R + \delta R_1}{(R + R_1)}\right)$$
$$= I_0\left(\frac{R}{R + R_1}\right)\left(1 - \frac{\delta R + \delta R_1}{(R + R_1)}\right) = I_{2,0} + \delta I_2 \qquad 4.3$$

where,

$$I_{2,0} = I_0\left(\frac{R}{R + R_1}\right)$$

Therefore,

$$I_{2,0} = I_{1,0}\left(\frac{R}{R + R_1}\right)$$

$$\delta I_2 = -I_{,01}\left(\frac{R}{R + R_1}\right)\left(\frac{\delta R + \delta R_1}{R + R_1}\right)$$

Spectral noise density is proportional to δI^2, i.e. $S_I \sim (\delta I)^2$.

So, we can write normalized noise power as

$$\frac{S_{I_1}}{I_{1,0}^2} \sim \frac{(\delta I_1)^2}{I_{1,0}^2}$$

$$\frac{S_{I_2}}{I_{2,0}^2} \sim \frac{(\delta I_2)^2}{I_{2,0}^2}$$

Thus, we have

$$\frac{S_{I_2}}{I_{2,0}^2} = \left(\frac{R}{R+R_1}.\frac{\delta R + \delta R_1}{\delta R}\right)^2 \frac{S_{I_1}}{I_{1,0}^2} \qquad 4.4$$

where it is assumed that $\delta R \neq 0$. If the additional resistance R_1 is "quiet", i.e. $\delta R_1 = 0$, we obtain

$$\frac{S_{I_2}}{I_{2,0}^2} = \left(\frac{R}{R+R_1}\right)^2 \frac{S_{I_1}}{I_{1,0}^2} \qquad 4.5$$

If $\delta R/R = \delta R_1/R_1$, then we obtain

$$\frac{S_{I_2}}{I_{2,0}^2} = \frac{S_{I_1}}{I_{1,0}^2} \qquad 4.6$$

It is not surprising that a "quiet" resistance would reduce the overall noise power and a resistance with proportionally equal "noisy" in series would keep the overall noise power same. In the second case, both, the current and current fluctuations are changed by same factor and thus, and they cancel out in normalized noise power.

In Ref. [105] the effect of the contact on the noise is studied. Here, ballistic CNT FET (L = 200 nm) with Pd, Ti and Al contacts are considered. In spite of three order of magnitude difference in device resistance, the normalized noise power for Pd-contacted and Al-contacted devices is within same range. It may sound surprising, but it is in agreement with our argument if the following two assumptions are true. First, the contacts are major source of noise and second, fluctuations in the contact resistance increase proportionally with the contact resistance. The first assumption is likely to be true for ballistic CNT FETs, and is also hinted by authors in

Ref. [105]. Validity of the second assumption is hard to verify, but if it is true then this situation is similar to our case of $\delta R = \delta R_1$, for which noise power is expected to remain same. Though, further work is needed to fully understand the role of contact resistance in noise of CNT FETs it is not surprising that CNT devices with different contact resistance show similar noise. In same Ref. [105], it is also shown that the noise of a device can be reduced by connecting multiple segments (say, X number) of a single CNT in parallel. The resistance (current) of the final device is decreased (increased) by X-times. The noise power in the final device is reduced by a factor of X because the number of carriers is increased by a factor of X.

What are implications of this discussion for our experiment? Here, it is argued that the different in noise in suspended and control CNTs is not due to presence of an additional "quiet" resistance in series, rather it is due to different level of interaction with underlying oxide substrate. Both, the suspended and control devices have top electrode contacts. As shown by simulations earlier in this chapter, the source-drain contacts in both kinds of devices are well screened by tall electrodes. Therefore, the contact resistance remains relatively unaffected by the gate voltage. Transfer curves in Fig. 4.5 show an order of magnitude different smaller current for a suspended than a control CNT device. The difference in resistance of suspended and control device is not due to different contacts, but due to different gate capacitance (c_g) (Fig. 4.6(b)). From electric field simulations (discussed later in the chapter) of c_g the gate capacitance for the suspended CNT was calculated to be 2.6 aF/μm and c_g for the control CNT 35.2 aF/μm. Thus, suspended CNTs have 13 times smaller c_g than control CNTs. Fig. 4.10 shows transfer curve modified from Fig. 4.5, where the

current in the transfer curve for the suspended CNT is scaled up by a factor of 13. Thus, the data is normalized with respect to gate capacitance and current is plotted against 'effective' V_g. Both the devices show similar 'effective' conductance for holes, but, as expected, suspended CNTs show larger conductance for electrons. Here, the transfer curve in hole-conduction regime was considered for noise analysis. Thus, since we ruled out the possibility of a significant difference in resistance of suspended and control CNT devices, it is reasonable to compare the noise power of suspended and control CNT.

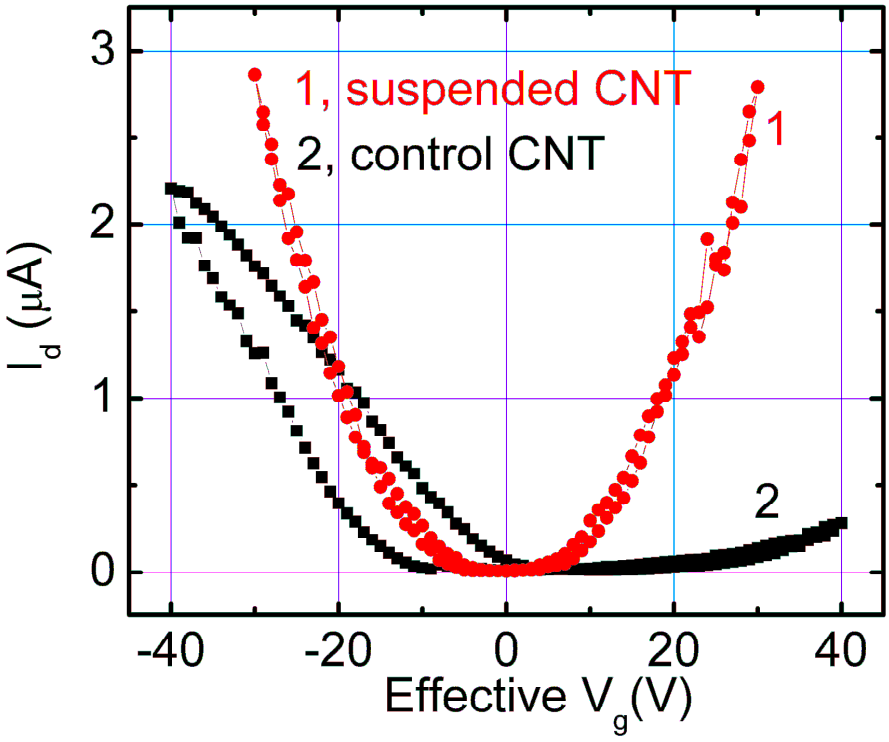


Figure 4.10 Transfer curves of suspended and control CNTs where drain current is plotted against 'effective' gate voltage as seen by the CNT.

Further comparisons between suspended CNT and control devices were conducted by calculating Hooge's constant. The dependence of the noise on carrier density was evaluated from the slope of the inverse noise power, I^2/S_I, as a function of frequency ($I^2/S_I = (1/A)*f$) in the linear region of transport behavior of the device.

The carrier density of a CNT in FET geometry can be controlled by gate bias (V_g). Therefore,

$$\frac{I^2}{S_I} = \left(\frac{1}{A}\right) f \tag{4.7}$$

and

$$\frac{1}{A} = \frac{N}{\alpha_H} = \frac{c_g L |V_g - V_{th}|}{\alpha_H e}, \tag{4.8}$$

where c_g is the gate capacitance per unit length, L is length of the CNT, V_{th} is gate threshold voltage and e is charge of an electron.

In Fig. 4.11(a), inverse noise power is plotted against frequency for different gate biases and the quantity $1/A$ was calculated from the slope. The linear dependence of $1/A$ on V_g, as shown in Fig. 4.11(b), indicates that field-effect mobility fluctuations, rather than charge carrier number fluctuations, are the origin for the noise in our suspended CNTs[106, 112]. Thus, Hooge's constant is independent of V_g. In the case of carrier density fluctuations, Hooge's constant is expected to vary with V_g, which we do not observe here. Gate capacitance $c_{g,susCNT}$ for a long suspended CNT (geometry 1 in Fig. 4.6(a)) is calculated by

$$c_{g,susCNT} \approx \frac{2\pi k \varepsilon_o}{\ln\left(\frac{h+2t}{h}\right) + k \ln\left(\frac{2h^2 + 2ht - rh}{rh + 2rt}\right)} = 8.2\ \text{aF/}\mu\text{m} \tag{4.9}$$

for the SiO_2 dielectric constant k = 3.9 and thickness t = 300 nm, the height of the CNT above the SiO_2 h = 500 nm and the CNT radius r = 1 nm. We estimate from numerical simulations that this capacitance is reduced to 2.6 aF/μm for L = 1 μm due to screening by the source-drain electrodes. Using this capacitance, Hooge's constant for four suspended CNT devices ranged from 6.1 x 10^{-3} to 9.3 x 10^{-4} with an average of 2.6 x 10^{-3}. The gate capacitance of a CNT lying on SiO_2, $c_{g,control}$ (geometry 1 in Fig. 4.6(a)) was calculated by

$$c_{g,control} = \frac{2\pi k\varepsilon_o}{\ln(2h/r)} = 35.2 \text{ aF/μm.} \qquad 4.10$$

The resulting Hooge's constant for 2 control devices was more than an order of magnitude larger than suspended CNTs, with an average of 5.6 x 10^{-2}. These observations point to the fact that the bulk of the noise in CNTs comes from the charge trapped on the surface of the dielectric layer.

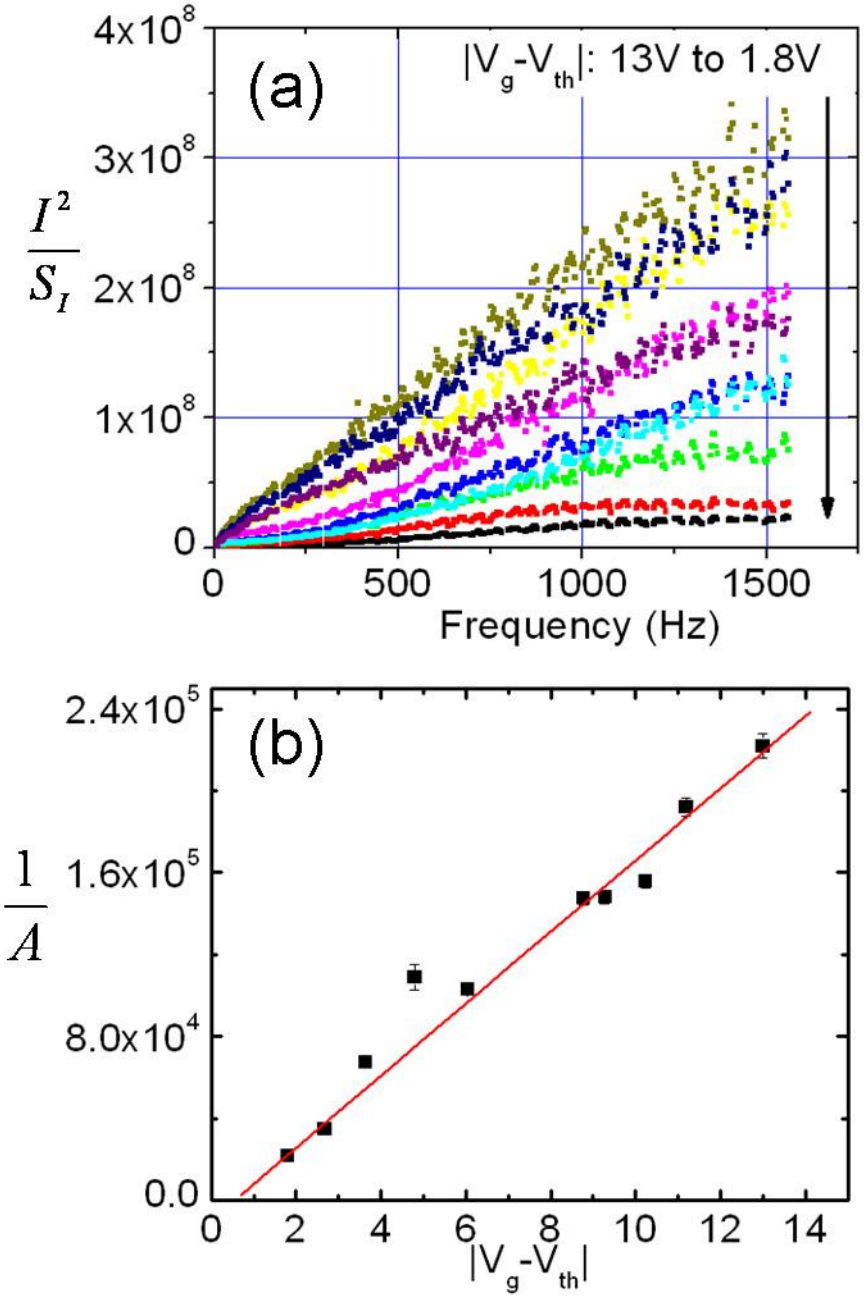


Figure 4.11 a) Inverse noise power of a suspended CNT is plotted against frequency for different V_g. b) The plot of $1/A$ versus $|V_g - V_{th}|$ is linear with Hooge's constant, $\alpha_H = 2.84 \times 10^{-3}$.

4.6 Conclusions

In conclusion, we have fabricated suspended nanotube devices with a straightforward technique that allows fabrication of as-grown nanotubes in a scalable fashion. The number of suspended CNTs can be controlled by tuning the parameters such as channel length and number of printing steps. Suspended CNTs showed reduction in substrate-induced effects, demonstrating intrinsic ambipolar behavior with negligible hysteresis in vacuum. We find that suspending the nanotubes also decreases the spectral noise power by 3 to 10 times, and the average Hooge's constant for a suspended CNT-FET was found to be 2.6×10^{-3}, over an order of magnitude smaller than identical devices with the CNTs in contact with SiO_2. Such pristine suspended CNTs, with decreased influence of the SiO_2 surface both in transport characteristics, as well as in $1/f$ noise, may enable studies of the intrinsic properties of carbon nanotubes. Effect of chemical processing on transport and $1/f$ noise is discussed in more details in Appendix B.

Chapter 5 : Carbon Nanotube Thin Film as a Semiconducting Material

In this chapter, I will report various experiments done to realize CNT thin films as semiconductor materials. First, the percolation theory for 2-dimensional random networks of conducting sticks will be introduced. I will then discuss the effects of CNT density and channel length on performance of the control devices fabricated on the SiO_2/Si substrate. Finally, I will describe several transfer printing methods to fabricate CNT TFTs on flexible substrates, and the effects of device geometry in transport properties.

5.1 Percolation Theory of 2D Random Conducting Sticks

To fully understand the mechanism of conduction in a random network of carbon nanotubes (CNTs) we need to consider percolation theory in two dimensional systems [113, 114]. Percolation theory is a statistical concept to study the behavior of connected clusters of randomly distributed elements in an infinitely large lattice. Percolation theory has been very useful for describing a variety of physical phenomena such as polymerization, H_2 storage in disordered medium, spreading of forest fires, and percolation of oil in fractured rocks underground. Percolation theory has also been successfully used to describe the conductivity of a random network of resistors. Here I will first illustrate the fundamental principle of percolation theory by considering a square lattice, and then discuss percolation effects in CNT thin film devices.

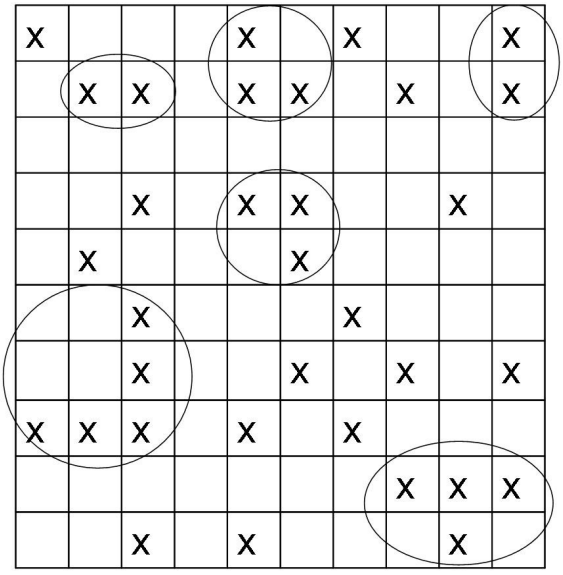


Figure 5.1 A square lattice consisting randomly distributed occupied sites.
A group of nearest neighbor occupied sites is defined as a cluster. Clusters with more than one member are encircled.

Fig. 5.1 shows a 10 by 10 square lattice with some squares filled with X's while others are empty. (Scaling behavior in percolative systems is true only in an infinitely large lattice, though a finite lattice is used here for illustration.) The squares with one common side are called 'nearest neighbor sites'. Here we define a cluster as a group of occupied sites connected to each other by one unbroken chain of nearest neighbor links from one occupied square to the other. This definition is arbitrary and is used for illustrative purposes. Clusters containing more than one member are encircled in Fig. 5.1.

Let's assume that a site is occupied with a probability p. At $p = 0$, all the sites are unoccupied and at $p = 1$ all the sites are occupied. If the total number of sites is N (N approaching a very large number) then $p*N$ sites are occupied. Thus p can also be called density of the sites. As p is increased from $p = 0$ to $p = 1$, larger and larger clusters begin to form. The percolation threshold (p_{th}) is the minimum density of sites

at which infinitely long clusters are formed. At $p > p_{th}$, one can always find at least one continuous chain of connected sites spanning the whole lattice from top to bottom and from left to right in Fig. 5.1. The "critical" density for the simple system described here is 0.5928. This value depends on the dimension of the system (e.g. p_{th} = 0.5 for a cubic system in 3D) and the structure of the lattice (e.g. p_{th} = 0.5 for triangular lattice in 2D). Percolation behavior depends on how individual elements are defined. So far we have considered 'site percolation'. 'Bond percolation' is another way of analyzing this system where two nearest neighbors are considered to be connected by a bond. Percolation behavior also depends on how the clusters are defined. For example, when a cluster in a square lattice in 2D is defined to include nearest as well as next nearest neighbors then p_{th} decreases to 0.4072 (Strangely, it is 1 – 0.5928!).

5.2 Percolation Theory for CNT Thin Films

Now let's consider CNT thin films. CVD grown CNT thin films have ~ 30% metallic and ~ 70% semiconducting and semi-metallic CNTs [115]. The simplest approximation to study transport through a CNT thin film is a random network of straight conducting sticks. A cluster consists of CNTs connected to each other such that there is at least one conducting path from any nanotube to any other nanotube in the cluster. The first Monte Carlo simulation of an isotropic randomly-oriented, equal-length stick system was reported by Pike and Seager [116]. This method was exploited to further study an anisotropic and distributed-length stick system by Balberg and Binenbuam [117]. The conductivity of a random network of conducting

sticks exhibits critical behavior at the percolation threshold as described by the following scaling law.

$$\sigma \propto (p - p_{th})^t , \qquad 5.1$$

where σ is conductivity, p is the density of sticks and the exponent t is estimated to be ~ 1.303 [118]. The value of p_{th} depends on factors such as length of the CNTs and the definition of density in the network. Density of the sticks can be defined in a number of ways such as the number of sticks per unit area, a volume or weight fraction of the conducting materials. Since it is cumbersome to count nanotubes in a random network, we adapt an alternative method to quantify the density of nanotubes. As previously described in Section 3.2, we quantify CNT density by the number of interactions per unit length of a regular grid. To confirm the validity of this method, we simulated random sticks in IDL 6.0 with controlled density and counted intersections with an overlapped regular grid. We observed that the number of intersections per unit length of the regular grid varies linearly with the number of random sticks per unit area.

Percolation behavior in finite sized systems is of more practical importance. Analytical scaling laws from infinite lattice are not precisely valid in finite systems but they offer approximate solutions. The relevant size parameters in a thin-film transistor are channel width W, channel length L, density of CNTs p and average length of CNTs l_{CNT}. For $W >> L$ and $L >> l_{CNT}$, the conductivity of a CNT network follows a power law relation with dimensions of the system (channel length L in this case). The exact form of the power law depends on the density of the network. The scaling law at two extreme conditions, at and much above percolation threshold, is;

$$\sigma \propto L^{-1.8}, \text{ for near percolation threshold } p \sim p_{th}$$
$$\sigma \propto L^{-1}, \text{ for much above percolation threshold } p >> p_{th} \qquad 5.2$$

Assuming CNTs as straight conducting sticks, the percolation threshold is approximately the density of CNTs at which the average distance between two CNTs is equal to the average length of CNTs, i.e. $p_{th} \sim 1 / \langle l_{CNT} \rangle^2$. The earliest attempts to incorporate a CNT network in thin-film devices exhibit *L*-dependent scaling behavior [46]. Numerical simulations [119] confirm this behavior when conditions $W >> L$ and $L >> l_{CNT}$ are satisfied. These simulations also demonstrate the expected deviation from scaling laws in the case of $L < l_{CNT}$ and $L \sim l_{CNT}$ (discussed later in this chapter). CNT devices with $W >> L$ show the expected scaling behavior and have reasonably good field-effect mobility (70 cm^2/Vs), but these devices are plagued with low on/off ratio (~ 10) due to the metallic CNTs. It was demonstrated by Cao et al [52] that restricting the lateral dimension can effectively reduce metallic paths in a CNT thin-film and thus improve the on/off ratio of the device to up to 10^4. The channel width of the devices studied in this work is within the same order of magnitude of the channel length ($W \sim L$).

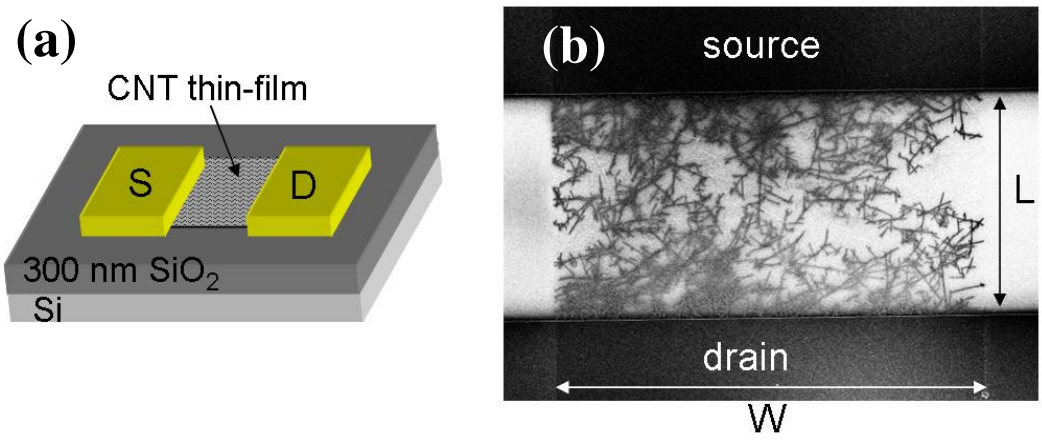


Figure 5.2 a) Schematic of a CNT thin-film device on a 300 nm thick thermally oxidized Si substrate. b) SEM micrograph of a device with L = 20 μm and W = 50 μm.

5.3 CNT Thin Film Devices

CNT thin film devices were fabricated on a 300 nm thick thermally oxidized Si substrate containing a CVD grown CNT thin film. 100 nm thick Au S/D electrodes (with a 10 nm thick Ti film as a wetting layer) were fabricated in contact with the CNT thin films using standard photolithography (using negative photoresist for good lift-off) and e-beam deposition. Since chemical exposure of CNTs is unavoidable in this process, the CNTs were also patterned by photolithography (Section 3.3.1). Here, CNTs were patterned after S/D electrode fabrication to avoid the extra step of putting the alignment markers on SiO_2 needed to align S/D electrodes on the patterned CNTs. The resulting devices consist of a highly doped Si global back gate, a 300 nm thick SiO_2 dielectric layer and top contact Ti/Au S/D electrodes (Fig. 5.2(a)). CNT thin films with controlled variable densities were used to make the CNT thin-film devices. The devices have channel width W = 50 μm and channel lengths L varying from 1 μm to 100 μm in steps of 5 μm. Fig. 5.2 (b) shows

a SEM image of a CNT network patterned into a device channel. The average length of CNTs is observed to be approximately 7 μm.

The charge transport behavior of a TFT is characterized by current-voltage (*I-V*) measurements. Measurements were taken in air at room temperature using a Cascade probe station and two Keithley 2400 source meters. One source meter is used to control the gate bias and measure the gate leakage current, while the other was used to bias and measure the current between the S/D electrodes. LabVIEW programs were used to control the measurement setup and acquire the data through a computer. The current between the S/D electrodes (I_d) is measured as a function of the bias between the S/D electrodes (V_d) and the bias between the source and the gate electrode (V_g). These *I-V* measurements were used to determine the charge carrier field-effect mobility (μ), the threshold voltage (V_{th}) and the ratio of the drain currents in on and off states of the device (I_{on}/I_{off}). Output and transfer characteristics of a device (with L = 100 μm, W = 50 μm) are shown in Fig. 5.3 (a) and (b), respectively. Field-effect mobility (μ) is calculated using

$$\mu = \frac{L}{V_d C_g}\left|\frac{\partial I_d}{\partial V_g}\right|, \qquad 5.3$$

and

$$C_g = \frac{\varepsilon A}{d} = \frac{\varepsilon L W}{d}, \qquad 5.4$$

where C_g is gate capacitance, ε and d are the dielectric constant (3.9 for SiO_2) and thickness of the dielectric layer, respectively. The field-effect mobility of the device is measured in the linear regime, $-2\ \text{V} < V_d < 2\ \text{V}$, and was found to be 12 cm^2/Vs. It is obvious that this number underestimates the intrinsic field-effect mobility of the

device since the gate capacitance was calculated assuming a parallel plate capacitor geometry. The area coverage of CNT networks of CNT densities used here is very small (usually 0.1% of the total area of the channel). Keeping that in mind we will take this number as a calibration of device performance throughout this thesis. The I_{on}/I_{off} ratio of the device is the ratio of device currents in on- and off- conditions and from now on will be referred as 'on/off'. In the downward gate sweep (from 30 V to – 30 V) in Fig. 5.3 (b), the device is 'off' at V_g = 30 V and turns 'on' at V_g = 18 V. The on/off ratio of this device at V_d = – 1 V is ~ 10^3. CNTs show p-type behavior on SiO_2 in ambient conditions. This has been associated with doping of CNTs by charge impurities in SiO_2 [30] and/or lowering of the work function of the metal at the contact by absorbates such as O_2 [120]. For a long CNT device, trapped charge impurities on SiO_2 are expected to play a bigger role than the contacts.

5.4 Optimization of the Device Performance

We will now discuss the effect of the device geometry (L) and the density of CNT network (p) on the device performance of CNT thin-film devices. Ten different sets of CNT thin-film devices were made with density varying from 0.2 - 3.92 intersections/μm. Each set consists of 20 devices with L varying from 1 μm to 100 μm in steps of 5 μm (W = 50 μm). The resistance of the devices was calculated by taking the inverse slope of the I_d vs V_d curve from the output characteristics in the linear regime. In the left column of Fig. 5.4, the device resistance (R) in the on- (at V_g = – 30 V) and off- states (at V_g = 30 V) is plotted against L for different CNT densities. The density of CNTs is shown in the rectangular boxes in between the two

columns and corresponds to both graphs in each row. In the right column of Fig. 5.4, the on/off ratio as a function of field-effect mobility is shown in a log-log plot for the same devices. Ideally, the on/off ratio of the device in the linear regime should be equal to the ratio of device resistance in 'on' and 'off' states. In the devices reported here, the ratio of 'on' and 'off' resistances differs significantly from the on/off ratio measured from transfer curves for the following reason: Here, the device resistance is obtained from the slope of the *I-V* curves in the range $1\ \text{V} < V_d < 1\ \text{V}$; and the *I-V* curves in the 'off' state are usually noisy (e.g. see fluctuation in 'off' current in Fig. 5.3(b). This could be due to either the current noise in the device or sensitivity of the measurement system (Keithley 2400). The on/off ratio in the right hand column of Fig. 5.4 is computed by considering peaks in "noisy" current in the 'off' state, e.g. 'off' current in Fig. 5.3(b) is taken as 2 nA, which underestimates true on/off ratio.

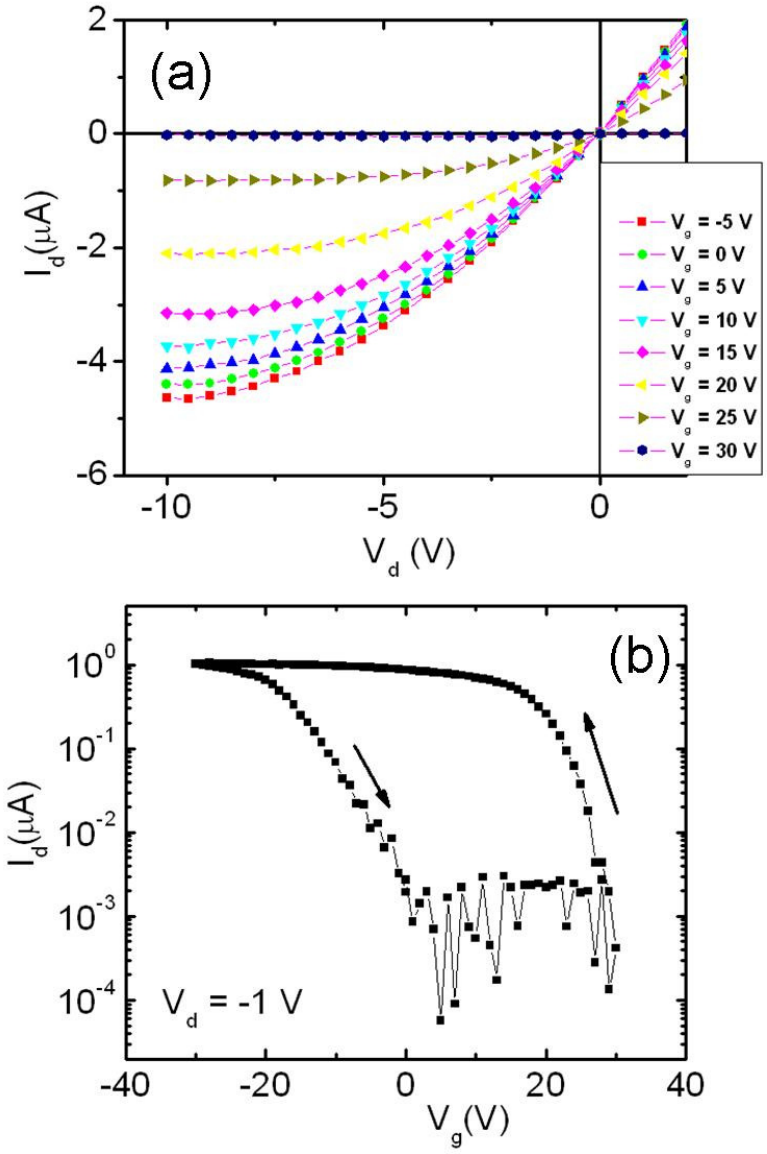
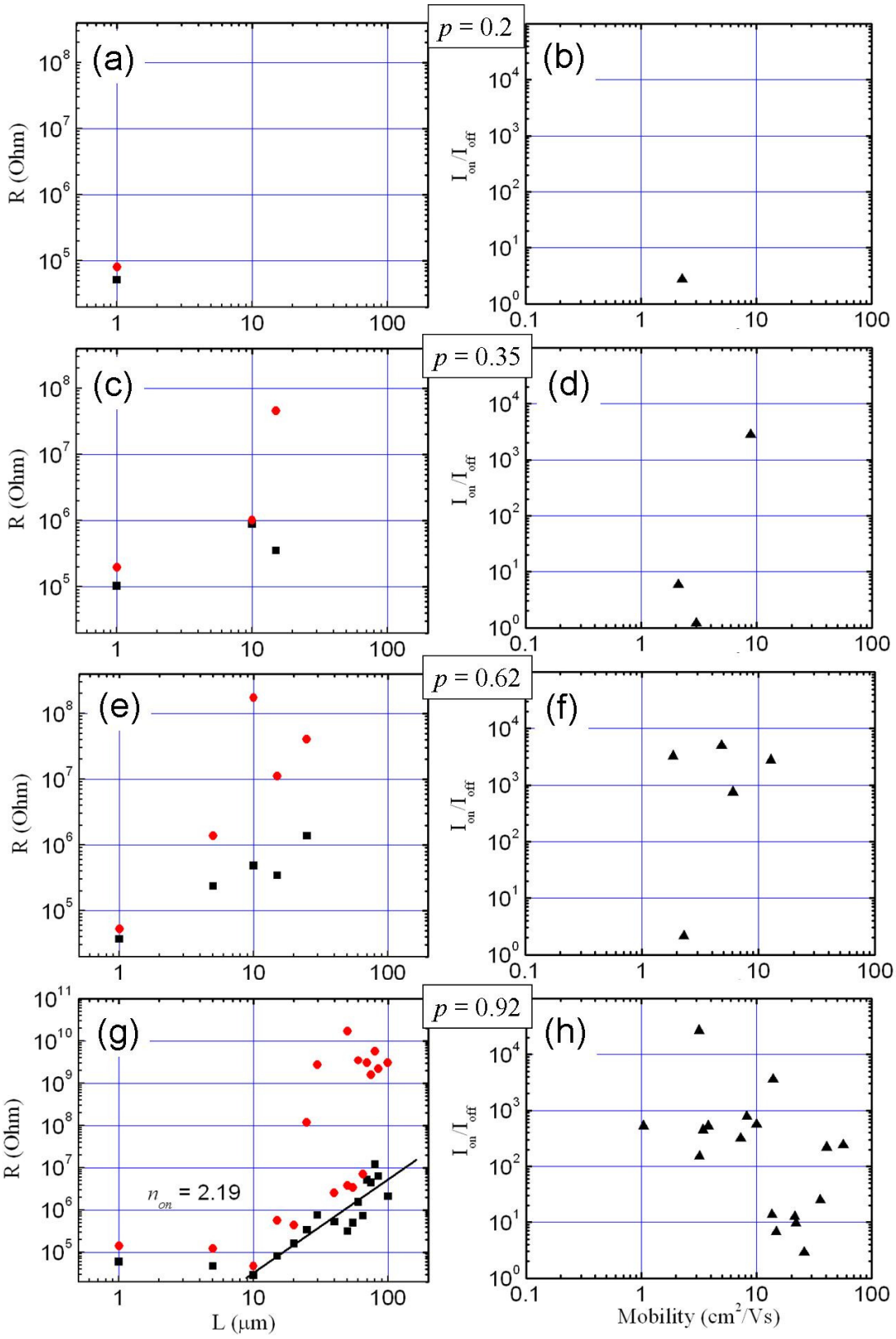


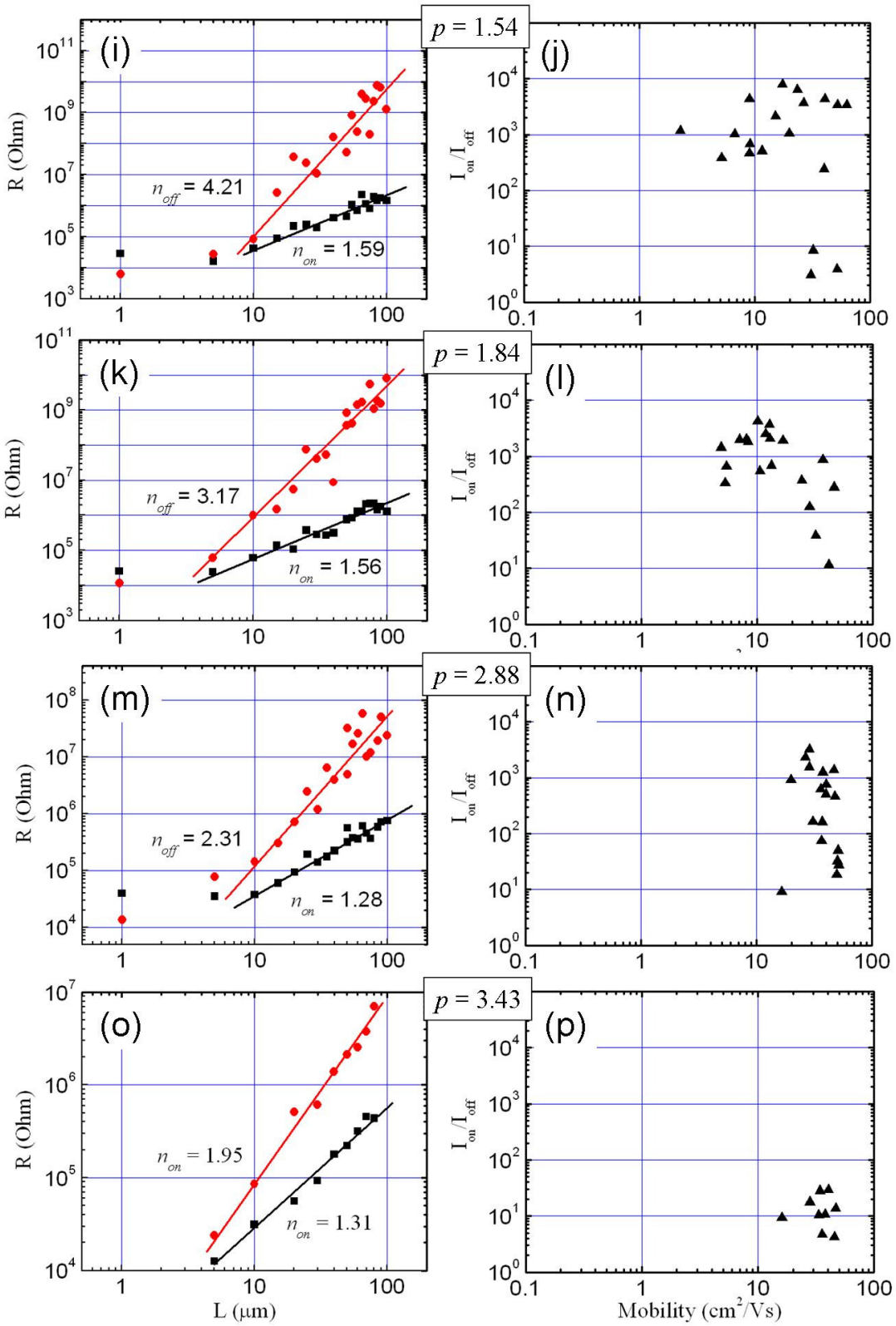
Figure 5.3 a) Output characteristic of a CNT thin-film transistor with $W = 50$ μm and $L = 100$ μm for gate bias (V_g) varying from 30 V to – 5 V. b) Transfer characteristic of the same device at $V_d = -1$ V. Drain bias was swept as indicated by the arrow.

We analyze the data in Fig. 5.4 starting from the lowest density (top of Fig. 5.4) to the highest density (bottom of Fig. 5.4). At the lowest density ($p = 0.2$ intersections/μm), there is only one working device with $L = 1$ μm (Fig. 5.4(a)). The CNT network is too sparse to form clusters and the conducting channel is formed by

individual CNTs crossing the 1 μm long channel. The low on/off ratio (< 2) of this device (Fig. 5.4(b)) can be explained by metallic CNTs shorting the source and drain electrodes. We observe that electrical response of the devices with $L < l_{CNT}$ (where $l_{CNT} \sim 7$ μm) is dominated by metallic CNTs for all different densities of CNTs. Almost all the devices with $L = 1$ and 5 μm show on/off ratio less than 10. At slightly increased density ($p = 0.35$ intersections/μm) (Fig. 5.4(c)) we observe three working devices with $L \leq 15$ μm. The first two of these devices show low on/off ratio (< 10) but the on/off ratio of the third device ($L = 15$ μm) jumps to 3×10^3. The high on/off ratio in this device is likely due to absence of a conducting path consisting of all metallic CNTs. As CNT density is increased further, bigger clusters of CNTs become more probable and the maximum channel length at which the device conducts increases. At $p = 0.92$ intersections/μm all the devices from $L = 5$ to 100 μm show a conducting channel.

The resistance of a random network is expected to increase with L by a power law ($R \sim L^n$). The exponent n is extracted from the least squares fit in log-log plot of R vs L ($\log(R) = n*\log(L) + \text{constant}$) for $L > 5$ μm. The 'on' resistance in Fig. 5.4(g) shows power law behavior with $n_{on} = 2.19$. However, the 'off' resistance is too noisy for a linear fit. Since n_{on} is slightly higher than the value expected at the percolation threshold (1.8), the CNT density at $p = 0.92$ intersections/μm can be expected to be below the percolation threshold. The measured field-effect mobility of the devices varies from 1 to 50 cm^2/Vs with lower on/off ratio at the higher range of mobilities.


p = 0.2
(a)
(b)
p = 0.35
(c)
(d)
p = 0.62
(e)
(f)
p = 0.92
(g)
(h)
R (Ohm)
I_on/I_off
n_on = 2.19
L (μm)
Mobility (cm²/Vs)


p = 1.54
(i)
(j)
n_{off} = 4.21
n_{on} = 1.59
p = 1.84
(k)
(l)
n_{off} = 3.17
n_{on} = 1.56
p = 2.88
(m)
(n)
n_{off} = 2.31
n_{on} = 1.28
p = 3.43
(o)
(p)
n_{on} = 1.95
n_{on} = 1.31
R (Ohm)
I_{on}/I_{off}
L (μm)
Mobility (cm²/Vs)

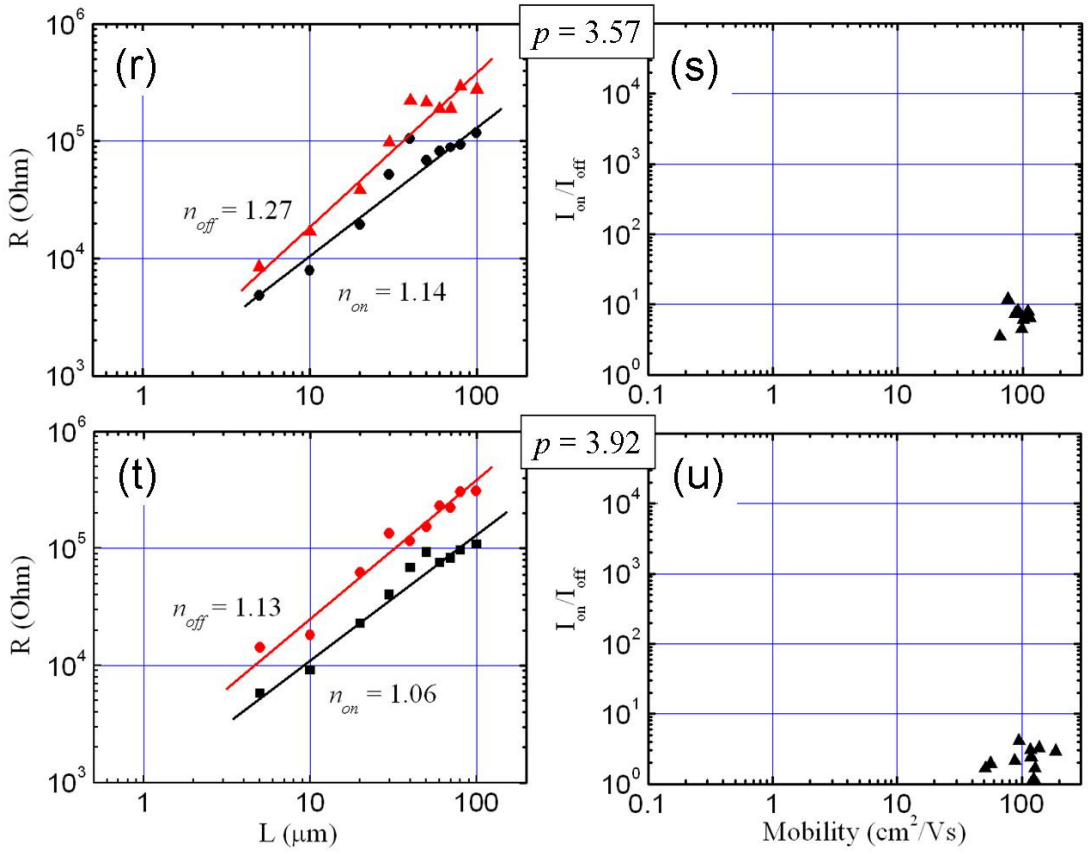


Figure 5.4 Left column from (a) to (t): Device resistance in on-(black squares and off states (red circles) is plotted against channel length (L) as CNT density (shown in the box in the center) is increased from top to bottom. The values of n shown are the slopes of the straight lines fit to the data. Right column (b) to (u): on/off ratio as a function of field-effect mobility of devices is plotted for the corresponding devices in the left column in same row.

At a higher density (p = 1.54 intersections/μm, Fig. 5.4(i)) we observe power law behavior of the device resistance in the 'off' as well as 'on' states. In the 'off' state, only metallic CNTs are expected to carry current. Since the density of metallic CNTs is always less than the net density of CNTs, n_{off} is always larger than n_{on}. Thus, on/off ratio of the devices increases roughly as a power law with L. On/off ratio is limited by 'off' current. The lowest 'off' current measured in the devices reported here is ~ 1 nA. Both 'on' and 'off' state power law exponents decrease with

increasing CNT density (Fig. 5.4(i) to (t)). Device resistance data also becomes less scattered at high density. It is important to mention that $R \sim L^n$ power law is expected to hold at or above percolation threshold. Therefore, ideally 'off' state resistance should not follow this power law when density of metallic CNTs is less than percolation threshold. However, we do observe power law behavior for 'off' state resistance as well, possibly due to presence of long CNTs in the channel.

A high quality FET is expected to have high field-effect mobility, high 'on' current and high on/off ratio. To achieve this, a large number of gate-tunable paths are desired. Devices with low CNT density are limited by low 'on' current and low field-effect mobility. However, increasing the CNT density would result in low on/off ratio due to increased number of metallic CNTs. An optimized field-effect mobility and on/off ratio should be realizable somewhere between these two extreme cases. In the right column, the scatter in field-effect mobility of the devices tends to decrease with increasing CNT density, whereas the average field-effect mobility of the devices tends to increase. The on/off ratio of the device, however, stays between 2 to 10^4 for all the devices in a set for CNT density varying from p = 0.92 to 2.88 intersections/μm. The average on/off ratio of devices with L > 50 μm is approximately 10^3. At p = 2.88 intersections/μm we achieve optimized device performance. The field-effect mobility of the devices is between 15 to 50 cm^2/Vs and on/off ratio goes up to 4000. As CNT density is increased further, on/off ratio of the devices at p = 3.43 intersections/μm drops between 4 and 40. At this density, the exponent of 'off' state resistance of the device is 1.95, close to the percolation threshold value of 1.8. We conclude that at p = 3.43 intersections/μm the density of

metallic CNTs is either above or close to the percolation threshold. At higher CNT density, the average on/off ratio of the devices decreases and average field-effect mobility increases. At the highest density of CNTs considered here, p = 3.92 intersections/μm, the field-effect mobility of the device is between 50 - 190 cm^2/Vs and on/off ratio is between 1.2 to 6.

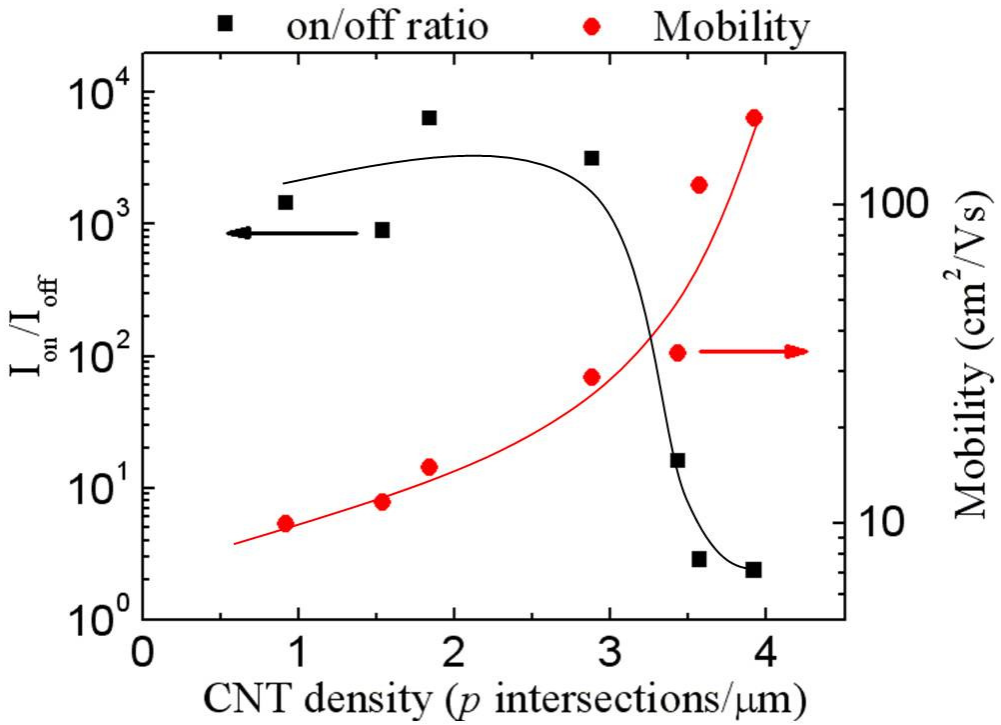


Figure 5.5 On/off ratio and field-effect mobility versus density of CNTs in a device with L = 100 μm. Curved lines are to aid the eye.

The effect of percolation on device properties can be seen more clearly by considering a device with L = 100 μm. In Fig. 5.5, on/off ratio and field-effect mobility of a device is plotted as a function of density of CNTs. This device did not show any conduction for $p < 0.92$ intersections/μm. For $p < 2.88$ intersections/μm the on/off ratio remains in between 10^3-10^4, whereas field-effect mobility of the device

increases with CNT density. At p ~ 3 intersections/μm, there is a sudden drop in on/off ratio of the device, whereas field-effect mobility keeps on increasing. Note that on/off does not reach 1 (where field-effect mobility is expected to be zero) even for very high density CNT thin films. Thus, there is trade-off between on/off ratio and field-effect mobility of the device. Device performance is optimized for a density of CNTs less than but as close as possible to the percolation threshold of metallic CNTs.

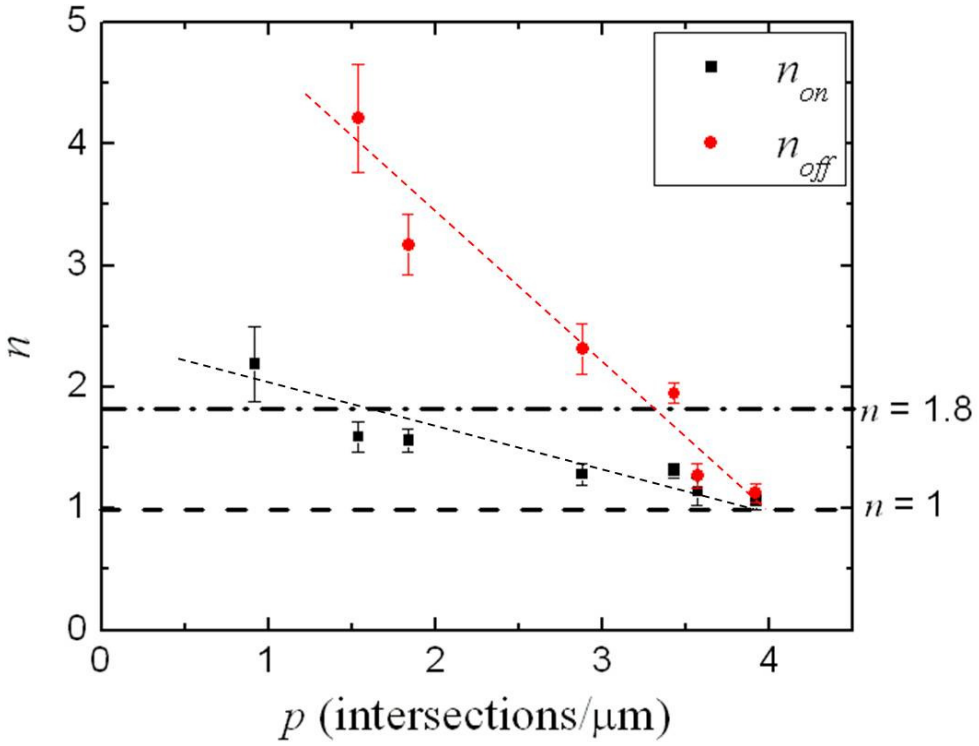


Figure 5.6 Power law exponents from length dependence of 'on' and 'off'-resistances of CNT devices are plotted as a function of CNT density. For a percolation network of CNTs, n is expected to be in between 1 and 1.8, shown by horizontal dashed lines. CNTs density required from good devices is between 0.92 and 2.88 intersections/μm. Slanted dashed lines are to aid the eye.

In Fig. 5.6, the power law behavior of device resistance is summarized. The exponents are plotted against the CNT density. The exponents approach 1 at high

density, i.e. for a homogeneous system. CNT devices with reasonably good field-effect mobility and on/off ratio are obtained for CNT density between 0.92 and 2.88 intersections/μm. In this range of CNT density, the 'on' resistance exponent is less than 1.8 and the 'off' resistance exponent is more than 1.8. This confirms that the net density of CNTs is above percolation threshold, whereas the density of metallic CNTs is below the percolation threshold. Optimum device performance is achieved at CNT p = 2.88 intersections/μm. Field-effect mobility (up to 50 cm^2/Vs) and on/off ratio (up to 4000) of these devices is comparable to the high device performance reported in Cao et al [52] (field-effect mobility up to 70 cm^2/Vs and on/off up to 10^4). In Ref. [52], long and narrow strips of CNT thin-films were used to enhance device performance. Lateral confinement (lower W) in a random network severely limits metallic paths, and therefore improves the on/off ratio. Here, we achieved reasonably good device performance without doing any additional processing on CNT thin-films.

In a CNT thin-film, not only individual CNTs but CNT - CNT junctions also affect overall electrical response of the network. Metallic CNTs (mCNT) are conducting at all the gate voltages and the conductivity of semiconducting CNTs (sCNT) can be modulated by the gate electrode. mCNT - mCNT junctions and sCNT - sCNT junctions are shown to be less resistive than the Schottky barrier in mCNT - sCNT junctions [121]. Gate modulation can not only change the conductivity of a sCNT but it can also modulate Schottky barriers at mCNT - sCNT junctions. Thus, conductivity in a random network of nanotubes is more complex than percolative networks of conducting sticks considered here. In Ref. [122], numerical simulations have demonstrated that percolation theory of conducting sticks alone is insufficient to

correctly explain conductivity in a random network of CNTs. Even a small number of metallic CNTs can "block" gate-tunable paths in a CNT network by Schottky barriers. To fully optimize the device performance, the effect from CNT - CNT junctions also needs to be reduced. This can be achieved by either selectively growing only semiconducting CNTs or by controlling the overall CNT density and device geometry such that the effect of Schottky barriers is minimized in a CNT thin-film. The experiment described here provides useful insight in this direction. To summarize, the parameters for optimum devices are as follows: CNT density p = 2.88 intersections/μm, W = 50 μm and L = 50 to 100 μm.

5.5 CNT Thin Film Devices on Flexible Substrates

Here, I will describe the transfer printing steps involved in fabricating bottom gate and top gate CNT TFTs on PET substrates [85]. Au is used for gate, source and drain electrodes, and PMMA is used as a dielectric material. I will compare transport properties of the devices fabricated in different device geometries. Then, channel length dependence of device performance will be studied and compared with the control CNT thin film devices discussed in the previous section. The density of CNT thin film used in CNT TFTs discussed in this section is 1.75 – 2 intersections/μm.

5.5.1 Bottom Gate Devices

First, 100 nm thick Au electrodes were transfer printed from a release layer (RL)-treated Si transfer substrate to a PET device substrate, see 1st step in Fig. 5.7. As discussed in Section 2.3, RL decreases the adhesion between PET and SiO_2 substrate. The printing conditions were 500 psi, 170 ^{o}C for 3 minutes for all the

printing steps. The dielectric layer can be applied to the device substrate in three different ways: directly spin coating on the PET device substrate, transfer printing from a blank Si substrate, and spin coating on the Si substrate containing source and drain (S/D) electrodes and printing the dielectric along with the electrodes. We used each of the three options to apply the dielectric layer (up to 1 μm-thick), but a short to the gate electrode through the PMMA was observed in all three cases. One probable explanation is that CNTs are hydrophobic and they tend to blend well in PMMA above its glass transition temperature ($T_{g,PMMA}$ = 105 ^{o}C). We used the first and the third options in combination to produce thicker (~ 2 μm) dielectric layers to eliminate the gate leakage. A 1 μm-thick PMMA dielectric layer was spin-coated and baked at 90 ^{o}C for 3 minutes on the release layer treated Si substrate containing 30 nm thick S/D electrodes. Another 1 μm-thick PMMA layer was spin coated and baked on the gate electrodes on the PET device substrate. The S/D electrodes were aligned to overlap the device channel over the gate electrode through the transparent PET device substrate. Then, the S/D electrodes and the PMMA layer were simultaneously transfer printed onto the second PMMA layer on the gate electrodes with the same printing conditions as in the 1st step, see the 2nd step in Fig. 5.7.

The patterned CNT thin films were finally printed onto the S/D electrodes using alignment markers, see the 3rd step in Fig. 5.7. CNT thin-films were patterned by photolithography and reactive ion-etching as described in Sections 3.3.1. The bare SiO_2 surface outside the patterned CNT area was exposed to release layer. Without the release layer treatment of the SiO_2 transfer substrate, the dielectric layer peeled from PET and transferred back to the SiO_2 substrate. Proof-of-concept bottom gate

CNT thin film devices were first reported in Ref. [62] and an optimized method was reported in Ref. [85]. Working devices were obtained by this method, but AFM and SEM studies showed some residual CNTs on the SiO_2 transfer substrate after the transfer printing. The partial transfer printing results in a lower density of CNTs in the device than the original density of the CNTs. The density of CNTs can be increased in the device by having even higher initial density of the CNTs, but this process cannot be fully controlled. Partial transfer of CNTs in this case could be due to an atomically thin layer of photoresist left on CNTs by photolithography. A complete transfer of CNTs was achieved by patterning the CNT thin films by PET stamps, as discussed in Section 3.2.3. An optical image of a bottom gate device is shown in Fig. 5.8. The devices consisted of 100 nm wide S/D electrodes with the channel length varying from 1 μm to 105 μm in steps of 3 μm.

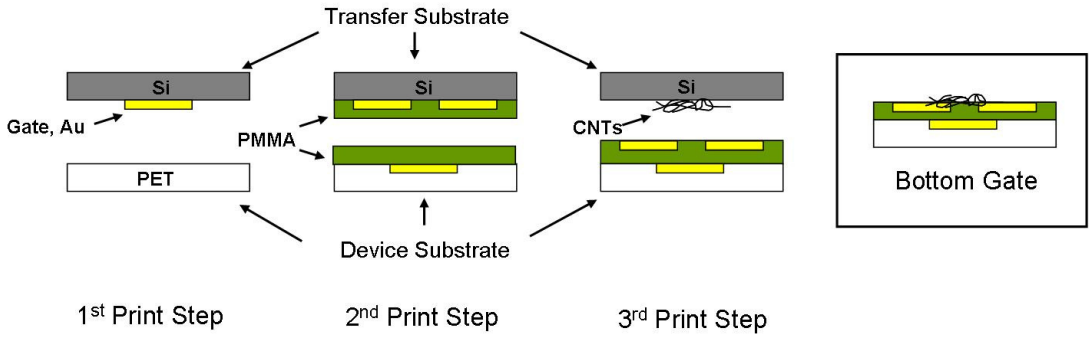


Figure 5.7 Schematic of printing steps involved in fabrication of bottom gate CNT thin film device. a) First Au gate electrodes were printed on PET substrate. b) Then 1 μm-thick PMMA dielectric layer was spin coated on both PET device substrate and Si transfer substrate containing the source-drain electrode. The source-drain electrodes were transfer printed onto the device substrate. c) Patterned CNT thin film was printed onto the source-drain electrodes. d) Schematic of the final bottom gate CNT device.

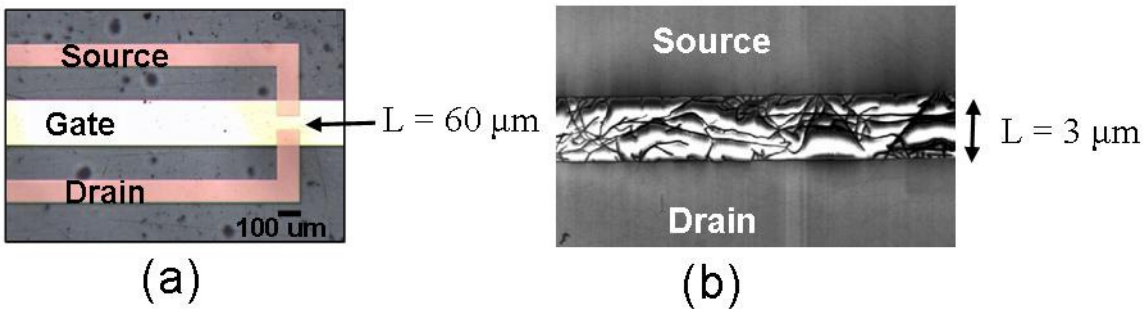


Figure 5.8 a) An optical image of a bottom gate device with L = 60 µm.
b) An SEM image of the channel of a bottom gate device with L = 3 µm. The CNTs show up as dark lines in the SEM image due to charging of the dielectric layer. The dark spots in the optical image are from the underlying sample holder.

5.5.2 Top Gate Devices

For top gate TFT devices, the first step was to transfer print the patterned CNT film from the release layer treated SiO_2/Si transfer substrate onto a PET device substrate, see 1st step in Fig. 5.9. The same printing conditions as in the bottom gate devices (500 psi and 170 ˚C for 3 min) were used for all the printing steps in top gate devices. The SiO_2/Si substrate contains 30 nm tall Ti alignment markers on the edges of the patterned CNT thin-films. Alignment markers on SiO_2 do not transfer print to the PET substrate, but do leave a visible imprint that was used to align subsequent layers. From both SEM and AFM measurements it was determined that the CNT film was fully transfer printed onto the PET substrate surface.

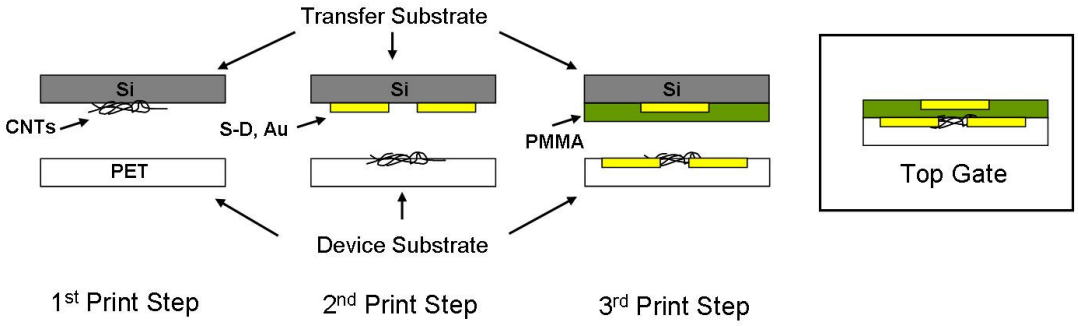


Figure 5.9 Schematic of printing steps involved in assembling a top gate CNT device. a) First, patterned CNT thin films are printed to a PET device substrate. b) Then untreated S/D electrodes are printed onto the CNT mat on PET. c) Finally the gate electrodes and the dielectric layer were printed simultaneously on the S/D electrodes. d) Schematic of of the final top gate device.

The second step was to transfer print 30 nm thick S/D electrodes (same geometry as in bottom gate devices) onto the PET device substrate such that the gap between the electrodes is aligned with the CNT thin film, see 2nd step in Fig. 5.9. Here, however, the release layer treatments used previously to improve transfer printing were omitted so that an untreated Au surface was in direct electrical contact with the CNT film. Omission of these release layer treatments (developed for printing involving a Si and SiO_2 surface against a PMMA surface) was found not to be detrimental to the transfer printing of the S/D electrodes onto a PET surface. The last step was to simultaneously transfer print the 100 nm thick gate electrode and dielectric layer onto the device substrate. This involved transfer printing the gate electrode from a Si transfer substrate onto a PMMA dielectric layer. For this step, it was necessary to perform the release layer treatment that was omitted for printing the S/D electrodes onto PET. Prior to transfer printing the gate electrode, a 600 nm thick film of PMMA was spin coated and baked at 90^{o}C for 3 min onto the Si transfer substrate containing gate electrodes. This PMMA-coated transfer substrate was then

aligned with and printed onto the PET device substrate such that the gate electrode was above the gap between the S/D electrodes. None of the top gate devices showed gate leakage for a 600 nm-thick dielectric layer. It could be that CNTs already printed on the flexible PET surface are not as prone to blend into PMMA as CNTs on the rigid SiO_2 substrate.

5.5.3 Control Devices

Transfer printed CNT thin film devices were compared with CNT thin film control devices fabricated on thermally oxidized Si substrates. Control devices were fabricated using the same method as used for CNT thin film devices in the previous section on the study of percolation effects. However, these control devices used a 500 nm thick SiO_2 dielectric layer. The S/D electrodes for the control device were of the same geometry as those used in the transfer printed devices.

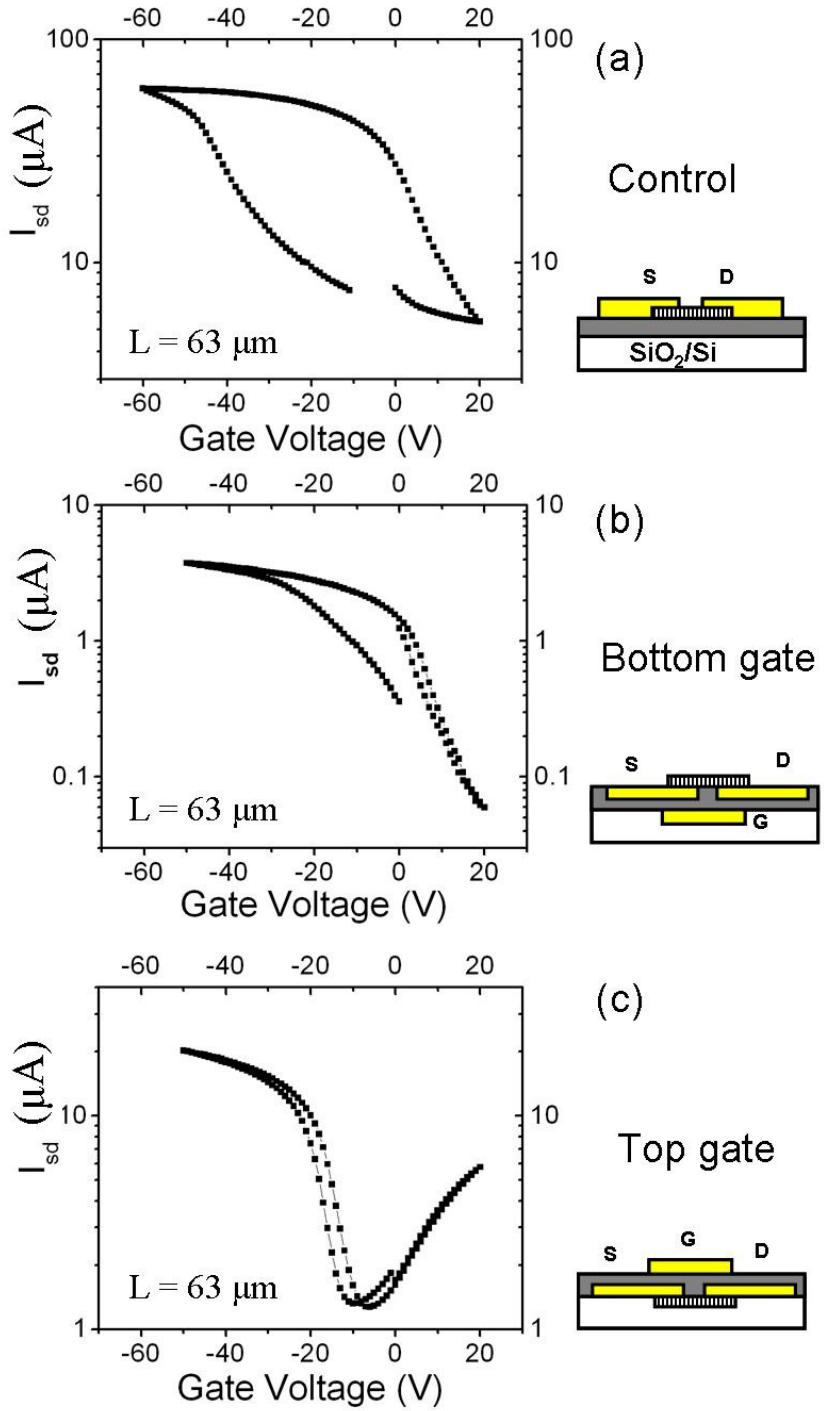


Figure 5.10 Transfer characteristics of a (a) control, (b) bottom gate and (c) top gate device. These devices have a channel length, L = 63 μm and S/D electrode width, W = 100 μm. A cross-sectional schematic showing the device geometry is shown on the right side for each device.

5.5.4 Transport Properties of Transfer Printed Devices

Transport properties of control devices have already been reported extensively in the previous section. Here we will discuss transport properties of bottom gate and top gate devices. Fig. 5.10 shows the transfer characteristics for (a) control, (b) bottom gate and (c) top gate devices with a S/D electrode width of 100 μm and a channel width of 63 μm. The top gate and bottom gate devices, in which the CNT film is in contact with polymeric interfaces, show less hysteresis than the control devices, where the CNTs are in contact with a SiO_2 dielectric layer. Large hysteresis for CNT devices using a SiO_2 dielectric layer has been reported by others and attributed to charging effects in the dielectric layer [30, 33]. Typical *p*-type transistor response is observed for the control and bottom-gate devices, whereas the top gate device shows ambipolar behavior. A possible origin of the different behavior is that the CNT film may be doped *p*-type by contact with the SiO_2 dielectric layer [30, 96] and not doped by the polymeric dielectric layer. In top gate devices CNTs are encapsulated from the environment (e.g. O_2 and H_2O) where CNTs are exposed to the environment in bottom gate devices. Therefore, the ambipolar behavior in top gate devices could also require protection from interaction with the environment. This in agreement with experiments done on suspended CNTs (Chapter 4) and on chemically processed CNTs (Appendix B). Annealing suspended CNTs in vacuum (~ 10^{-6} Torr) resulted in greater ambipolarity (Section 4.3). Annealing in vacuum is known to release surface absorbates, such as O_2, that are believed to play a role in determining the type of the charge carriers in CNTs [120].

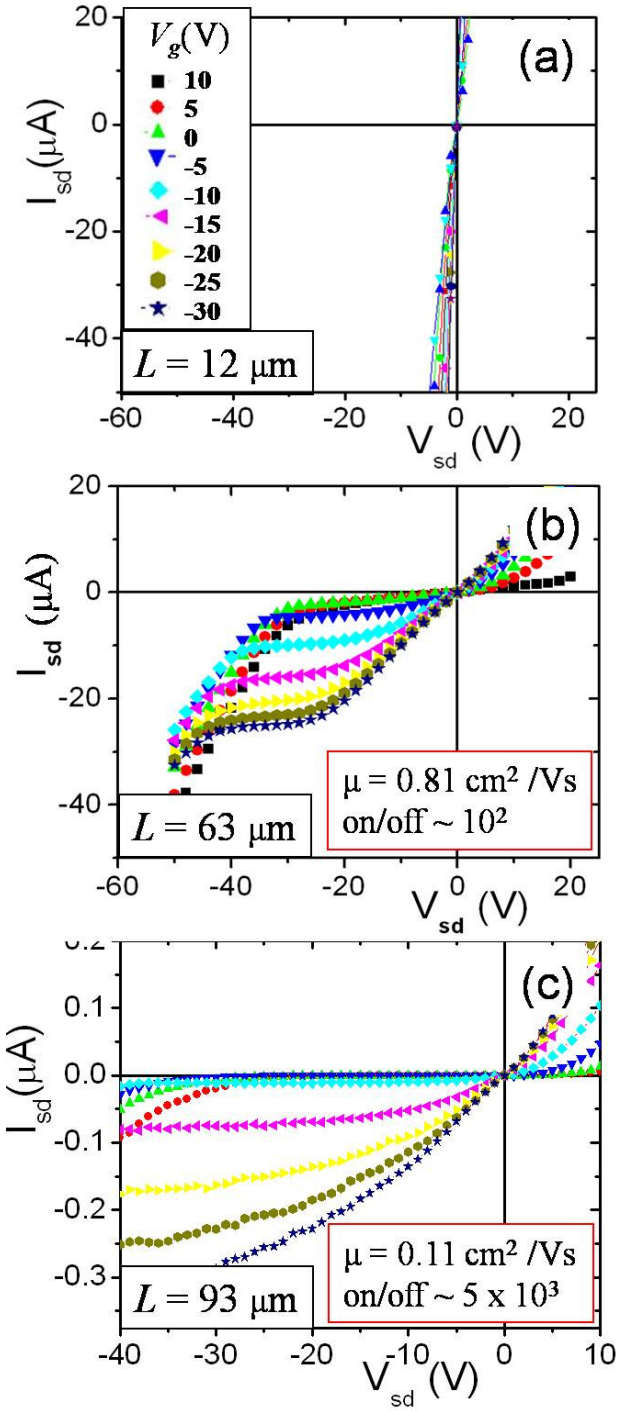


Figure 5.11 a), b), c) Output characteristics of top gate devices with W = 100 μm and L = 12 μm, 63 μm and 93 μm, respectively. (a) Linear I-V characteristics with weak gate dependence is observed with low on/off ratio (~10) at small channel length. (b) Semiconducting behavior is observed with field-effect mobility ~ 1 cm^2/Vs and on/off ratio ~ 10^2 for intermediate channel lengths. (c) The device shows transistors behavior with low conductance but high on/off ratio. The color legend in (a) applied to all the graphs.

Output characteristics of the devices were studied as a function of channel length. The density of CNT thin films was kept constant in both top- and bottom gate devices by using the same catalyst concentration and growth conditions. Output characteristics of top gate devices at channel lengths 12 μm, 63 μm and 93 μm are shown in Fig. 5.11(a), (b) and (c), respectively. Top gate devices exhibit a qualitative channel length dependent behavior similar to control devices. At shorter channel lengths (< 60 μm, see Fig. 5.11(a)) the linear response of the top gate device resembles a resistor with an on/off ratio on the order of 10. At longer channel length (> 60 μm), some devices exhibit output characteristics of a transistor with an on/off ratio on the order of 10^2 (at $V_d = -1$V) and effective field-effect mobility (calculated assuming a uniform film covering the entire device area) on the order of 1 cm^2/Vs (see Fig. 5.11(b)). Interestingly, top gate devices are turned 'on' even at positive V_g for $V_d >> V_g$. The current in Fig. 5.11(b) increases sharply at $V_d = -30$ V. At this point, electrons also carry current in the channel, as expected from ambipolar devices, Fig. 5.10(c) (Fig. 5.10(c) and Fig. 5.11(b) correspond to the same device). For $L > 93$ μm, top gate devices show a highly resistive channel (> 50 MΩ in the 'on' state). Output characteristics of a device with $L = 93$ μm is shown in Fig. 5.11(c). The device still shows transport behavior of a transistor with very small 'on' state conductance (~ 0.01 μS) at $V_g = -30$ V. The field-effect mobility of this device is 0.11 cm^2/Vs and on/off ratio is approximately 5 x 10^3. Top-gate devices can be turned-off much more effectively ('off' current ~ 10^{-11} A) at large channel lengths (L > 90 μm). As for control devices, the sheet resistance (ρ) of top gate devices was observed to increase with channel length from $\rho(L = 12$ μm) = 1 MΩ to $\rho(L = 93$ μm)

= 250 MΩ. However, there are large variations in transfer printed devices as compared to control devices. Variability in device performance from the expected L dependence for control devices could be due to variability in the final CNT density in top gate devices. In spite of complete transfer of CNTs on the PET substrate, device-to-device variation can be introduced due to diffusion of some CNTs during printing at elevated temperatures.

Output characteristics of bottom gate devices were also studied as a function of channel length. Surprisingly good transistor behavior was observed in bottom gate devices independent of the channel length. The average on/off ratio was found to be ~ 10^3. This is notably higher than the average on/off ratios measured for control and top gate devices. Field-effect mobility was measured in the range from μ = 0.08 cm^2/Vs (for L = 12 μm) to μ = 13.7 cm^2/Vs (for L = 60 μm). The different transport behavior of these bottom gate devices as compared to control devices may be related to the lower CNT density caused by the partial transfer print of the CNT film for the bottom gate geometry. Partial transfer printing can introduce large device-to-device variability in bottom gate devices. Thus variability in CNT density overwhelmed the expected L-dependent variation in the device performance. In some bottom gate devices, discontinuities in drain current were observed during the very first sweep of the drain voltage in output measurements at V_g ~ 15 V. This is believed to be due to burning of certain conducting paths in the CNT network. This was observed only in bottom gate devices, not in control or top gate devices. Inadvertent burning of CNTs could have introduced additional variation in bottom-gate devices.

5.6 Conclusions

In this chapter, we studied effects of percolation in a random network of CNTs. Device performance of control CNT thin film devices was optimized by controlling the CNT density. Optimized CNT thin film devices showed field-effect mobility up to 35 cm^2/Vs at on/off ratio up to 10^4, which is comparable to other high quality devices in literature. Transfer printing offers a versatile way of fabricating CNT thin film device on transparent and flexible substrates with device field-effect mobility (up to 10 cm^2/Vs) better than organic semiconductors. CNT thin film devices were demonstrated in top gate and bottom gate device geometries. Top gate devices showed small hysteresis and slightly ambipolar behavior probably due to encapsulation of CNTs. The performance of transfer printed CNT thin film devices could be further improved by optimizing CNT density.

Chapter 6 : Carbon Nanotube Thin film as an Electrode Material

Next-generation displays and solar cells require high-performance transparent and flexible device components. Carbon nanotube (CNT) thin films have been successfully incorporated as both semiconductor elements [46, 52, 85, 123] and electrodes [124-126] for flexible, transparent electronics. CNT thin films have been demonstrated to have higher field-effect mobility and stability in air than organic semiconductors (e.g. Pentacene and P3HT) [50, 52]. However, the use of nontransparent metals (e.g. Au, Ti and Pd) as electrodes makes CNT and organic thin-film transistors (TFTs) only partially transparent. Conventional transparent conducting films (e.g. indium tin oxide (ITO) and $(In,W)_2O_3$) are potential electrode materials in organic TFTs [127] and CNT TFTs [128, 129], but expensive growth techniques and inherent brittleness makes these materials incompatible with flexible electronics. CNT thin films are an alternative transparent, flexible electrode in organic TFTs [51, 124, 125] on plastic substrates. For the fabrication of such devices, patterned CNT thin films have been assembled onto plastic substrates using air-brushing [130] and transfer printing [85, 93, 131]. Printing patterned CNT thin films from a transfer (growth) substrate to a device substrate eliminates the need for solution processing techniques to be used on the device substrate [132]. In this way, CNT thin films can be assembled as both the electrodes and the active layer in the same device (all-CNT TFT). All-CNT devices reported previously [51] show gate leakage and poor on/off ratio (up to 100). Here, we report all-CNT devices with

field-effect mobility up to 33 cm^2/Vs and on/off ratio up to 10^4 with gate-leakage similar to control devices fabricated on a SiO_2 substrate (~ 1 nA).

CVD-grown CNT networks with long carbon nanotubes and low areal density are a promising semiconductor material. However, they are too resistive to be used as electrodes. Alternatively, air-brushed CNT thin films can be prepared with sheet resistance as low as $1k\Omega$ per square (at 80% transparency) making them attractive materials for electrodes. Additionally, CNT thin films can be airbrushed at room temperature over large areas of diverse substrate materials. Here, all-CNT TFTs are fabricated using air-brushed CNT thin films as conducting layers (source, drain and gate electrodes) and chemical vapor deposition (CVD) grown networks as semiconducting layers.

Organic semiconductors are also promising materials for low-cost, large-area flexible electronics. Organic semiconductors have been incorporated in display drivers [133], rf identification tags [134] and sensor arrays. Different approaches to construct organic digital circuits include p-type FET circuits [135], complementary circuits [136, 137] and hybrid organic/inorganic complementary circuits [138]. Complementary circuits have the advantage of lower power dissipation and better noise margin over circuits made from only p-type FETs. Low contact resistance is desired for high performance devices. Contact resistance is of special concern in complementary circuits where two different kinds of contacts are formed between electrodes and n-type and p-type semiconductors. For low contact resistance, the work function of the electrode is required to match the HOMO (highest occupied molecular orbital) and the LUMO (lowest unoccupied molecular orbital) of p-type

and n-type semiconductors, respectively. Commonly used metal electrodes (e.g Au and Al) form more favorable contact with one or the other kind of organic semiconductor. High-quality inverters with low operating voltage and high dc gain have been fabricated using pentacene and C_{60} active channels [139]. However, these circuits employ two different metal electrodes: Au for p-type channel and Ca for n-type channel, to minimize the contact resistance. Using different electrode materials adds undesirable complexity in the fabrication process. Elsewhere, CNT thin film electrodes have been demonstrated to form low resistance contacts with organic semiconductors such as pentacene [125], P3HT [126] and poly (3,3'''–didodecylquarterthiophene) [140]. Here, we also demonstrate successful incorporation of airbrushed CNT thin film electrodes in organic complementary circuits.

In this chapter, I will report techniques for patterning and printing CNT thin films as both electrodes and semiconducting layers over a large area of the plastic substrate (PET). Airbrushed CNT thin films will be characterized using optical (transparency), mechanical (flexibility) and electrical measurements (sheet resistance). The transport properties of the all-CNT TFTs and organic complementary circuits will be discussed and compared to high-quality control devices.

6.1 Airbrushing CNT Thin Films

CNT powder (P3-SWNT from Carbon Solutions, Inc.) was dissolved in a solution of 1% by wt. surfactant sodium dodecyl sulfate (SDS) in de-ionized (DI)

water [126]. P3-SWNTs are functionalized with 4-6 atomic% carboxylic acid group (-COOH) with carbonaceous purity greater than 90%. The CNT solution was well dispersed through ultra-sonication for 90 min. Carbonaceous impurities [124] were removed by centrifugation at 12,000 rpm for 40 min. The top two-thirds of the solution was extracted from vials (capacity 1.5 ml) using a micro-pipette. The well-dispersed and purified CNT solution was airbrushed from an airbrush (Aztek A470 airbrush kit) vertically fixed 15 cm above the substrate (see Fig. 6.1 for set-up). This airbrush allows independent control over the volume of pressurized air (25 psi) and CNT solution in the aerosol. The spot size of the spray is determined by the airbrush nozzle and the distance between the nozzle and the substrate. A large spot size (~ 3 cm) was chosen to ensure a uniform CNT thin film in an array of devices spread over an area of 1 cm^2. Since CNT thin films are not clearly visible, a fixed laser beam was used to align the spray to the desired location on the substrate. The substrate was kept on a hot plate (at 165 ^oC) to accelerate water evaporation. After deposition, the airbrushed CNT thin film was cooled down and soaked in a large quantity of DI water for 30 min to remove the surfactant.

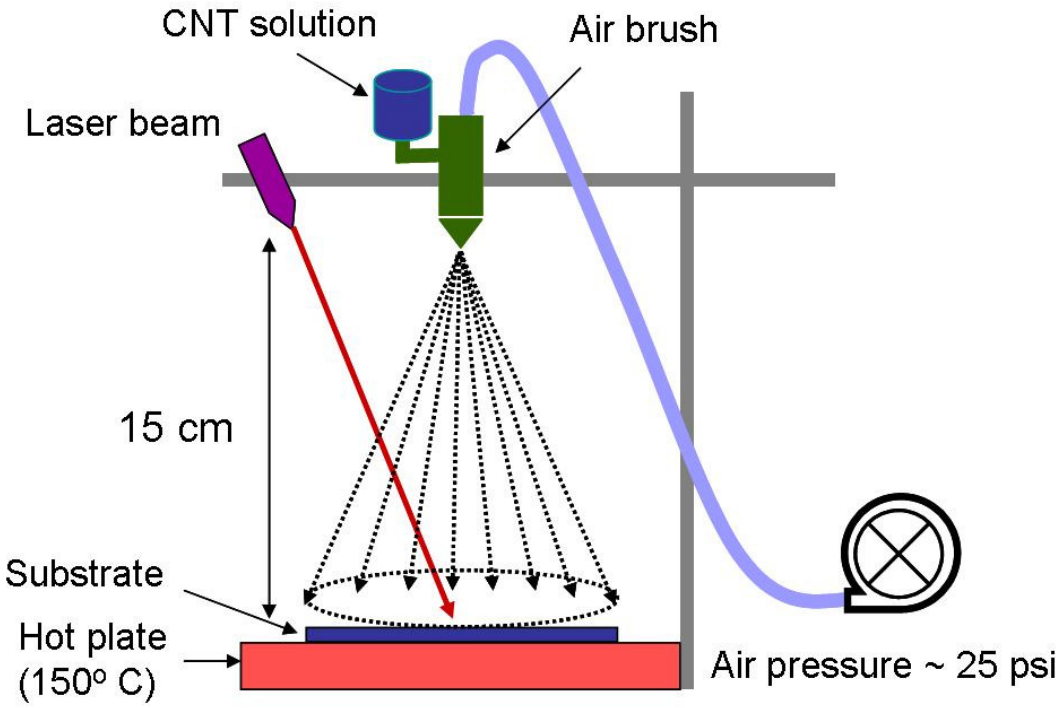


Figure 6.1 Schematic of the experimental set-up for airbrushing CNT solution.

The thickness of a CNT thin film can be controlled by various parameters such as flux of the aerosol, density of the solution and duration of airbrushing. The density of CNT solution was varied (while keeping flux and airbrushing duration constant) to study the individual aerosol droplets on a 500 nm thick thermally oxidized Si substrate. Fig. 6.2(a) (b) and (c) show SEM images of a few or a single dried droplet from CNT solutions with density 3 mg/ml, 1 mg/ml and 0.03 mg/ml, respectively. The ratio of CNTs to SDS (i.e. CNT:SDS = 1:10) was kept constant in all different concentrations. The diameter of dried aerosol droplets was observed to range from 5 μm to 20 μm. The total number of CNTs in a droplet depends on the density of the solution. For 3 mg/ml solution, the droplet area is completely filled with CNTs, Fig. 6.2(a). For 1 mg/ml solution, the CNTs tend to stack in a garland-

shaped structure, possibly due to the "coffee-stain effect", Fig. 6.2(b). "Coffee-stain effect" is produced by the capillary flow of liquid induced by the differential evaporation rates over the drop. For 0.03 mg/ml solution, there are very few CNTs per droplet and they are stacked in a circle. A continuous CNT thin film can be obtained by airbrushing for longer times so that aerosol droplets overlap each other. Airbrushing dilute CNT solutions for a longer time is expected to produce more uniform CNT thin films than airbrushing dense CNT solution for a short duration. However, airbrushing of very dilute solution is a time consuming process. Therefore, we airbrushed CNT solution with a medium density 1 mg/ml in all the devices reported here. Continuous airbrushing at a rate faster than the evaporation rate of water resulted in a non-uniform CNT thin film due to the coffee-stain effect. Airbrushing a CNT solution in multiple short pulses (0.5 sec each) produced a more uniform thin film compared to films produced by a continuous spray. Thus we kept the aerosol flux and density of the CNT solution constant and varied the airbrushing duration (number of pulses) to control the thickness of a CNT thin film. Fig. 6.2(d) shows an AFM image of a 30 nm thick CNT thin film obtained by airbrushing the CNT solution (1 mg/ml) in 20 pulses.

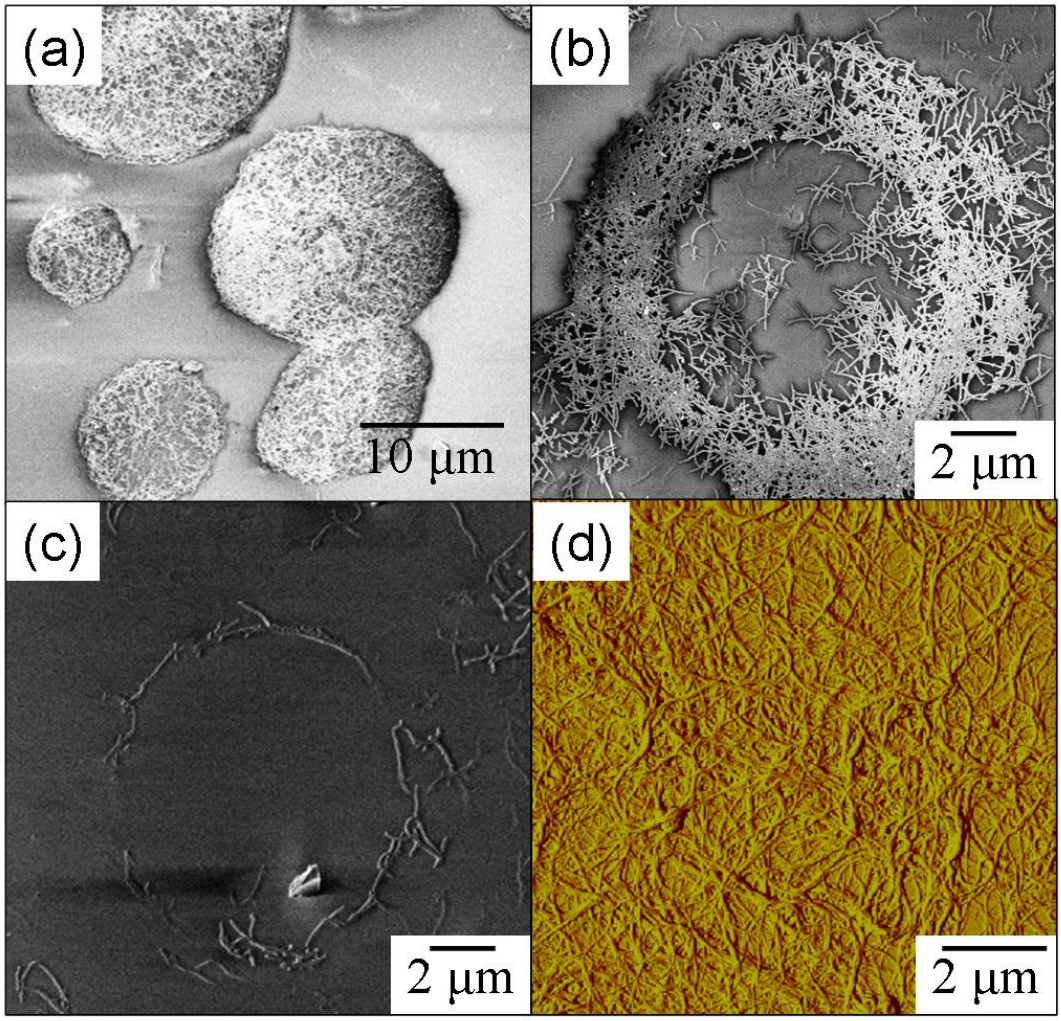


Figure 6.2 a) A SEM image of CNTs in dried droplets of 3 mg/ml solution. b) A SEM image of a single dried droplet of 1 mg/ml solution. The CNTs form a garland shaped structure due to the coffee-stain effect. c) A SEM image of a single dried droplet of 0.03 mg/ml solution. Individual CNTs line up along the perimeter of the droplet due to coffee-stain effect. d) An AFM image of a uniform CNT thin film obtained by airbrushing 1 mg/ml solution.

CNTs were successfully airbrushed on glass, thermally oxidized Si and PET substrates. CNT thin films on PET substrates were used for optical and electrical characterization. The transparency of the films was measured using a UV-Vis-IR Spectrophotometer (Cary 5000) normalized to the transparency of a blank PET substrate. Fig. 6.3(a) shows the transparency (T) of a CNT thin film as a function of

wavelength of the incident light. CNT thin films show a remarkably constant transparency over a broad range of wavelength. In comparison, the transparency of a conventional transparent electrode material, In_2O_3, decreases significantly at wavelengths higher and lower than 550 nm. Sheet resistance (R) was measured using a two-probe geometry on rectangular CNT thin films. CNT thin films of different thickness were deposited through a shadow mask. Au electrodes were evaporated through another shadow mask to obtain 1 cm^2 CNT thin films in between the electrodes. In Fig. 6.3(b), sheet resistance is plotted against transparency of airbrushed CNT thin films measured at wavelength 550 nm (the middle of the visible range). As expected, there is a trade-off between conductivity and transparency of thin films. The devices reported here use CNT thin films with transparency of 80% and sheet resistance of 1 $k\Omega$ per square (an AFM image is shown in Fig. 6.2(d)).

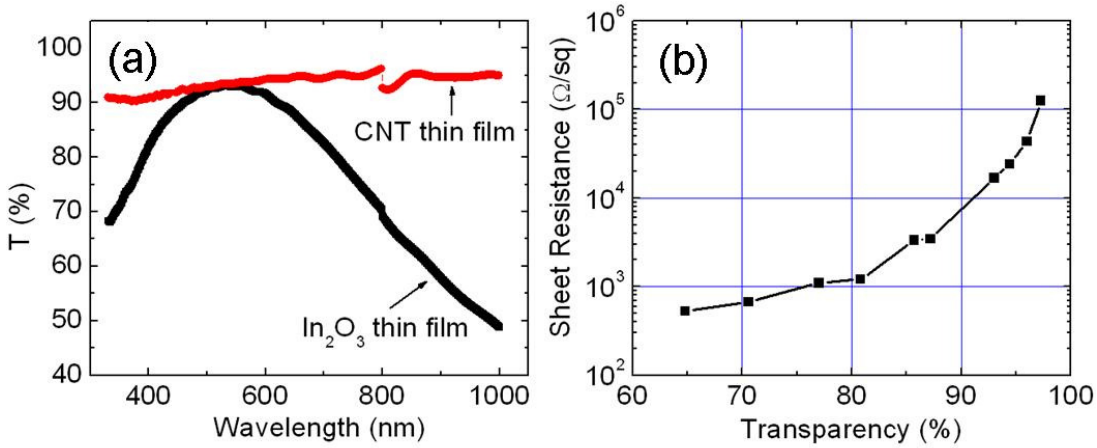


Figure 6.3 a) Transparency of a CNT thin film (sheet resistance ~ 10 kΩ) and an In_2O_3 thin film (i.e. PET films coated with In_2O_3/Au/Ag, commercially available from Delta Technologies Limited) is plotted as a function of wavelength. The discontinuity in transparency at 800 nm is due to switching of the light source. b) Sheet resistance of airbrushed CNT thin films (thickness varying from ~ 1 nm to ~ 40 nm) is plotted as a function of transparency (%).

Large area CNT thin films can be patterned by airbrushing through a shadow mask. However, the low resolution (~ 100 μm) and large edge roughness (~ 20 μm) of the shadow mask severely limits the potential of CNT thin films. Thus, we used photolithography (negative photoresist, NR7 1500 PY) and reactive ion etching (O_2 plasma) to pattern airbrushed CNT thin films electrodes (Section 3.3.1). In contrast to CVD grown CNTs, it can be challenging to pattern multi-layered airbrushed CNT thin films (thickness ~ 30 nm) by photolithography. The fragile airbrushed CNT thin films can be easily washed away by even a slightly vigorous spray of solvents. Airbrushed CNT thin films could not be patterned by a positive photoresist, OIR 908-35. The photoresist developers seeped into CNT thin film underneath the photoresist and dissolved the whole pattern in the solution. Negative photoresist should also be used with care. For example, lift-off of the negative photoresist at a temperature lower (~ 70 ^{o}C) than designated temperature (85 ^{o}C) produced aesthetically appealing but otherwise useless patterns of CNT thin films, as in Fig 6.4.

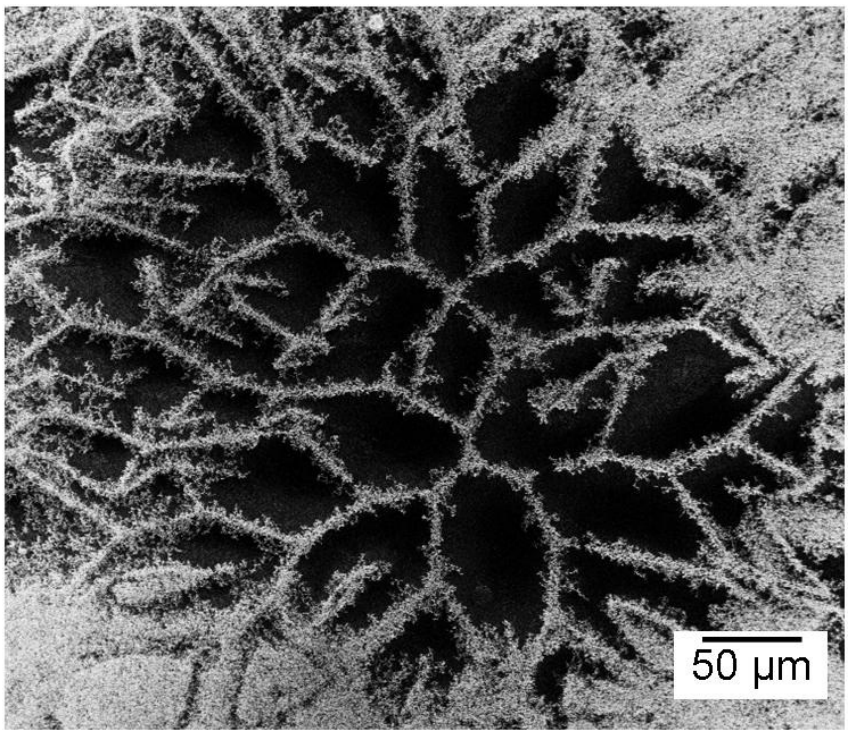


Figure 6.4 CNT thin film flowers obtained after lift-off of a negative photoresist at sub-optimal lift-off temperature.

6.2 Transfer Printing CNT Electrode Sub-assemblies

As discussed in Chapter 5, patterned Au electrodes can be directly printed from a release layer-treated transfer substrate to a device substrate. This recipe, however, was not successful in transfer printing airbrushed CNT thin films. CNT thin films transferred only partially onto PMMA and PET substrates at printing parameters ranging from 200 psi to 600 psi and from 100 ^{o}C to 180 ^{o}C, see Fig. 6.4(a). An optical image in Fig. 6.4(b) shows CNT thin film electrodes left on the Si substrate after transfer printing to a PET substrate at 500 psi, 170 ^{o}C for 3 min. The partial transfer (Fig. 6.4(c)) can be attributed to a stronger CNT/Si adhesion strength

as compared to the cohesion strength of the 30 nm thick CNT thin film. Here we developed a new recipe for complete transfer printing of airbrushed CNT thin films.

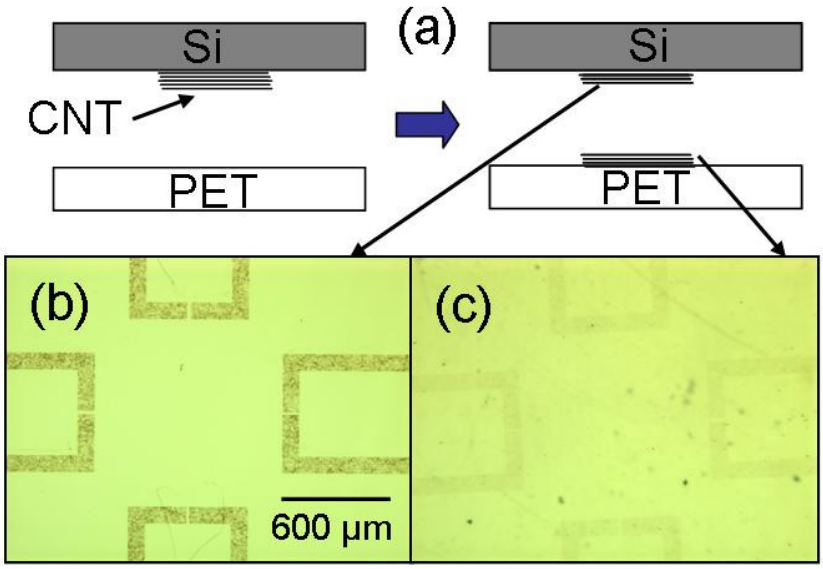


Figure 6.5 a) Schematic of transfer printing an airbrushed CNT thin film from a Si substrate to a PET substrate. b) An optical image of CNTs left on Si substrate. c) An optical image of printed CNT electrodes on PET.

CNTs were first airbrushed onto a Au-coated (50 nm thick) Si transfer substrate and then patterned into gate electrodes (Fig. 6.6(a)). The Au carrier film is used here as a low adhesion layer to assist the transfer printing procedure. The complete transfer of the CNT/Au bilayer exploits the fact that the Au/Si adhesion strength is less than the Au cohesion strength and Au/CNT/polymer adhesion strength [61]. The CNT gate electrodes/Au bilayer was transfer printed from the Si transfer substrate to a PET device substrate at 400 psi, 120 ^{o}C for 3 min (Fig. 6.6(b)). The Au film was then etched away by Au etchant (GE-1848, Transene Company, Inc).

The dielectric layer was prepared by depositing a 50 nm thick Al_2O_3 layer onto the gate electrodes by e-beam evaporation, followed by spin-coating a 800 nm

thick PMMA layer (Fig. 6.6(c)). The Al_2O_3 is used to eliminate the gate leakage that is otherwise observed, even with a 2 μm thick stand-alone PMMA layer. The Al_2O_3 is used as a diffusion barrier for CNTs that appear to diffuse through the bulk of the polymer dielectric layer at the elevated temperatures associated with the transfer printing process. To print the source and drain electrodes, another Au carrier film with patterned CNT source-drain electrodes was printed onto PMMA at 400 psi, 120 ^{o}C for 3 min (Fig. 6.6(d)) followed by etching of the Au film by Au etchant. In the final step, a patterned semiconducting thin film is transfer printed from a transfer substrate to the electrode sub-assembly (Fig. 6.6(e)). We have successfully printed pentacene (500 psi, 120 ^{o}C for 3 min) and CVD grown semiconducting CNT thin films (500 psi, 170 ^{o}C for 3 min) in the last step. Using the Au carrier film, we have also achieved proof-of-concept transfer printing of airbrushed CNTs to other polymer dielectric materials such as poly(4-methylstyrene), poly(alpha-methylstyrene), polystyrene, poly-4-hydroxystyrene, polyvinyl alcohol and polycarbonate. By treating the Si surface of the transfer substrate with a release layer before deposition of the Au carrier film, airbrushed CNTs were also printed onto polyimide and polyvinyl nitrile.

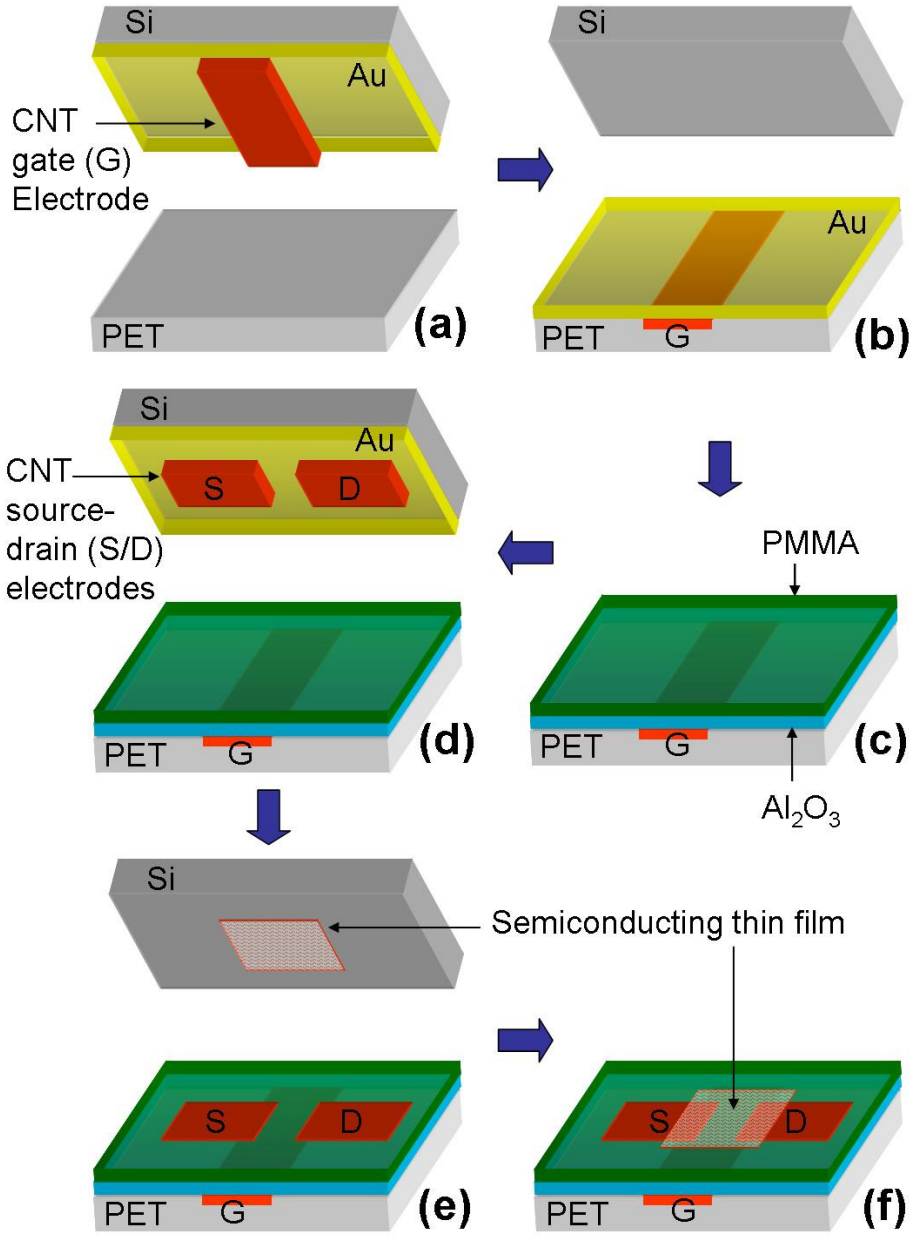


Figure 6.6 Schematic of different transfer printing steps used to fabricate all-CNT bottom gate devices. a) & b) A 50 nm thick Au carrier film is first transfer printed onto a PET device substrate along with a patterned CNT gate electrodes. The Au film was then etched away by an Au etchant. c) A 50 nm thick layer of Al_2O_3 was evaporated on gate electrodes followed by spin-coating a 800 nm thick PMMA layer. d) CNT source-drain electrodes were printed onto PMMA using another Au carrier film. The Au film was again etched away by the Au etchant. e) and f) The active component of the device, a patterned CNT thin film or an organic semiconductor film was transfer printed onto CNT electrode sub-assembly.

To complete the discussion on the fabrication process, it is important to characterize the effect of photolithography and transfer printing on the sheet resistance of airbrushed CNT thin films. Rectangular films of CNTs were airbrushed through a shadow mask on 10 pieces of SiO_2/Si substrate. Au electrodes were evaporated on each sample for a two-probe resistance measurement. Four-probe van der Pauw measurements of sheet resistance also produced similar results but the data reported here was carried out by two-probe measurements. Resistance was measured before and after exposing the samples to all of the photolithography steps (except etching CNT by RIE). The resistance of the samples was found to be within 5% of the original value. Some of the polymer resists (e.g. PMMA) could be removed by annealing the samples in H_2 at 450 ^oC [83]. However, we observed a two times increase in the sheet resistance of airbrushed CNT thin film after H_2 annealing. This effect of annealing on CNT thin film is not well understood.

To characterize the effect of transfer printing, CNTs were airbrushed on three sets of samples (6 samples in each set, each with sheet resistance ~ 600 Ω). Three sets of CNT thin films were transfer printed onto PET substrates at three different transfer printing conditions. After printing at 400 psi, 65 ^oC for 3 min, the average sheet resistance of the first set remained within 1.5% of the original value. After printing at 400 psi, 120 ^oC for 3 min, the average sheet resistance of the second set increased by 6% of the original value. After printing at 500 psi, 170 ^oC for 3 min, the average sheet resistance of the third set increased by 23% of the original value. Pressing a multi-layered CNT thin film should improve its conductivity by making more intimate CNT-to-CNT contacts. Instead, transfer printing at high temperature

decreases the conductivity of CNT thin films. Pressing a CNT thin film against a plastic substrate above the glass transition could diffuse these materials into each other and disrupt CNT-to-CNT contacts. CNT electrodes were printed at 400 psi, 120 ^{o}C for 3 min in the all the devices reported here. Thus, the sheet resistance of the electrodes is expected to remain within 10% of its original value.

6.3 Characterization of the Dielectric Layer

Gate leakage in printed CNT electrodes is a serious issue [51]. We characterized the PMMA/Al_2O_3 dielectric layer in a parallel plate (1mm x 1mm) capacitor geometry on PET substrates. A 50 nm-thick Au layer was used as one of the electrodes and a CNT thin film as the other electrode. An additional 50 nm-thick Au film was deposited on the CNT film to avoid a distributed capacitor and resistance network of CNTs. A control capacitor was fabricated with Au layers as both electrodes. The dielectric layer consisted of 800 nm-thick PMMA and 50 nm-thick Al_2O_3 layers in both kinds of capacitors. The capacitance ($C = \varepsilon A / d_{eff}$, where *C, A,* ε and d_{eff} are capacitance, area, dielectric constant and effective thickness of the dielectric layer, respectively) was measured using a Andeen-Hagerling AH2700A capacitance bridge. The capacitance of the CNT thin film capacitors (25.2 ± 3.5 pF) was found to be approximately 3 times higher than that of control capacitors (8.3 ± 0.65 pF), suggesting 2 to 3 times smaller effective thickness of the dielectric layer due to percolation of CNTs in the PMMA. The ac conductance (500 Hz to 20 kHz) of the CNT thin-film capacitors was observed to be 5 times higher than the control capacitors. The capacitors were broken into pieces (by making them brittle in

liquid N_2) for direct visual inspection of the cross-section of the dielectric layer. Fig. 6.7(a) and (b) show SEM images of cross-sections of a CNT thin film and control capacitor, respectively. CNTs percolating through the PMMA layer could be seen in the CNT thin film capacitor, Fig. 6.7(a). The absence of black lines in the control capacitors (see Fig. 6.7(b)) suggests that they are not just charging effects in SEM. It is possible that some of the CNTs could be drooping or bending on the cleaved side. Since we did not observe a gate leakage current larger than 1 nA in any of the devices with Al_2O_3/PMMA dielectric layer, we conclude that the Al_2O_3 film acts as an effective diffusion barrier for CNTs.

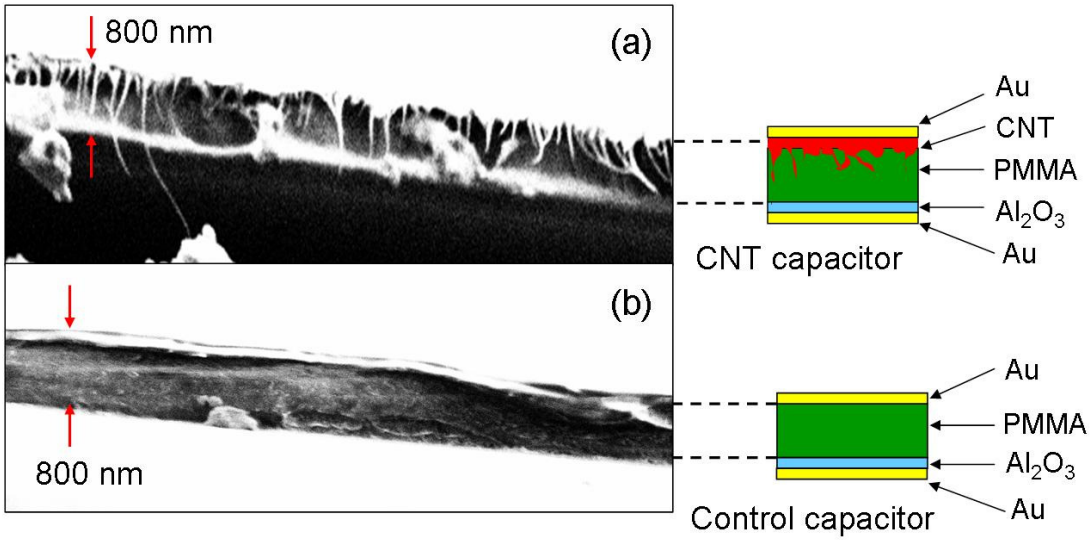


Figure 6.7 a) A SEM image of cross-section of a CNT thin-film capacitor reveals CNTs percolating through a 800 nm thick PMMA dielectric layer. The capacitor was sandwiched between two Au films for accurate measurements. b) A SEM image of cross-section of a control capacitor is shown to compare with the image in (a) to establish the identity of the CNTs. Schematics of the two capacitors on right hand side show the different layers.

6.4 All-Carbon Nanotube Thin film Transistors

All-CNT bottom gate devices were fabricated with a channel width (W) of 100 μm and channel length (L) varying from 10 μm to 100 μm in steps of 10 μm. To demonstrate the potential of our transfer printing technique for large area electronics on transparent and flexible substrates, we made 90 all-CNT electrode sub-assemblies on a one inch square PET substrate (Fig. 6.8(a)). These electrode sub-assemblies could not be converted into complete devices due to limited size of our CVD furnace to grow CNTs over such a large area. The optical image in Fig. 6.8(b) shows a magnified view of a set of ten completed devices with L varying from 10 μm to 100 μm.

Device performance of all-CNT bottom-gate devices is compared with control bottom-gate devices made by using Au as electrode material. Control devices were fabricated using the transfer printing method described in Chapter 5 [85]. Briefly, first 100 nm-thick Au gate electrodes were transfer printed onto a PET device substrate. A 50 nm-thick Al_2O_3 layer was deposited on the gate electrodes following by spin-coating a 800 nm-thick PMMA layer. Then, 30 nm-thick source-drain electrodes were printed on device substrates. Finally, a patterned CVD grown CNT thin film was printed onto the source-drain electrodes.

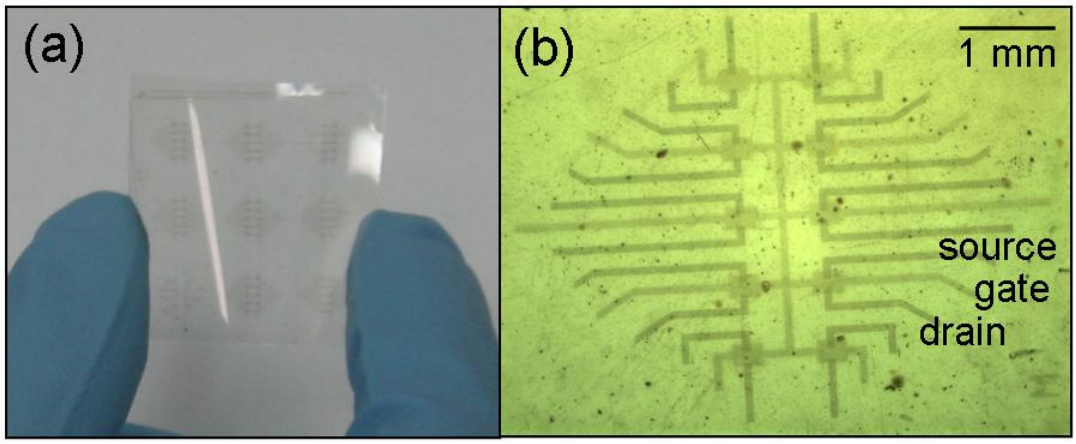


Figure 6.8 a) An optical image of a one inch square PET substrate with 90 CNT electrode sub-assemblies. b) Zoomed in optical image of a group of 10 all-CNT devices with channel length varying from 10 to 100 μm. Some of the dirt particles seen in the image are from the underlying plate.

Transport measurements were made in ambient conditions using a Cascade Microtech Summit 12K probe station. Au pads (100 nm thick) were deposited on the CNT electrodes 500 μm away from the device channel to make better contact with the probe tips. The resistance of the CNT source-drain electrodes was subtracted from the total measured resistance to obtain the real resistance of the device. CNT thin film devices show a poor on/off ratio due the presence of metallic CNTs in the random network [85, 130]. We employed an electrical breakdown technique [42] to eliminate metallic paths in the CNT networks. Drain bias was increased in a controlled fashion while keeping the gate bias at 30 V. Fig. 6.9(a) shows the intermediate transfer characteristic curves (from curve 1 to 4) of an all-CNT device with L = 60 μm and W = 100 μm after successive burnout of metallic CNTs. Fig. 6.9(b) shows the output characteristics of the device in the final condition. The on/off current ratio (V_d = – 1 V) of the device has increased from 10 to 6000 whereas the field-effect mobility (linear regime, – 1 V < V_d < 1 V) of the device decreased from

10.3 cm^2/Vs to 4.8 cm^2/Vs. It is interesting to note that the on-state hole conduction (at $V_g = -30$ V) decreased only by 3 times whereas the on-state electron conduction (at $V_g = 30$ V) decreased by an order of magnitude. This is probably because these devices exhibit ambipolar behavior and electric breakdown at $V_g = 30$ V affects not only metallic CNTs but also CNTs with electrons as charge carriers. At larger channel lengths, a high on/off ratio is observed without having to burn metallic paths. After burning metallic paths in the device channel, the on/off ratio of all the devices with different L was improved up to 10^2 - 10^4, and no L dependence in the final on/off ratio of the devices was observed. Electrical breakdown was also employed to improve the on/off ratio in control devices.

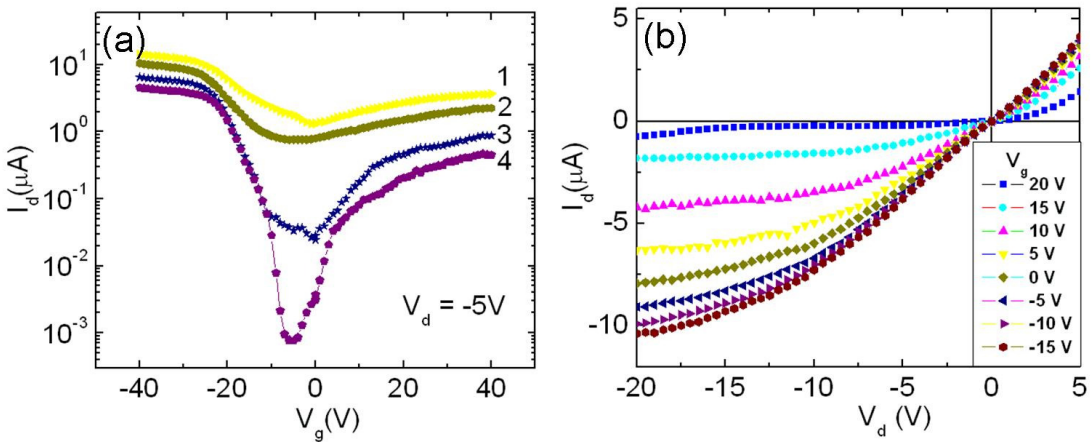


Figure 6.9 a) Transfer characteristics of an all-CNT device ($L = 60$ μm) at $V_d = -5$ V. The on/off ratio was increased by 3 orders of magnitude by successively (curves 1 through 4) burning metallic CNTs at $V_g = 30$ V. b) Output characteristics of the final device.

In Fig. 6.10, the on/off ratio is plotted as a function of field-effect mobility for all-CNT devices and control devices. The range of the on/off ratio is similar for both kinds of devices and is 2 orders of magnitude higher than that previously reported for

all-CNT devices [51]. The field-effect mobility of the devices varies from 1 to 33 cm^2/Vs. Overall, the device performance of all-CNT devices on plastic is comparable to the control CNT thin film devices reported here and elsewhere [85, 130, 131].

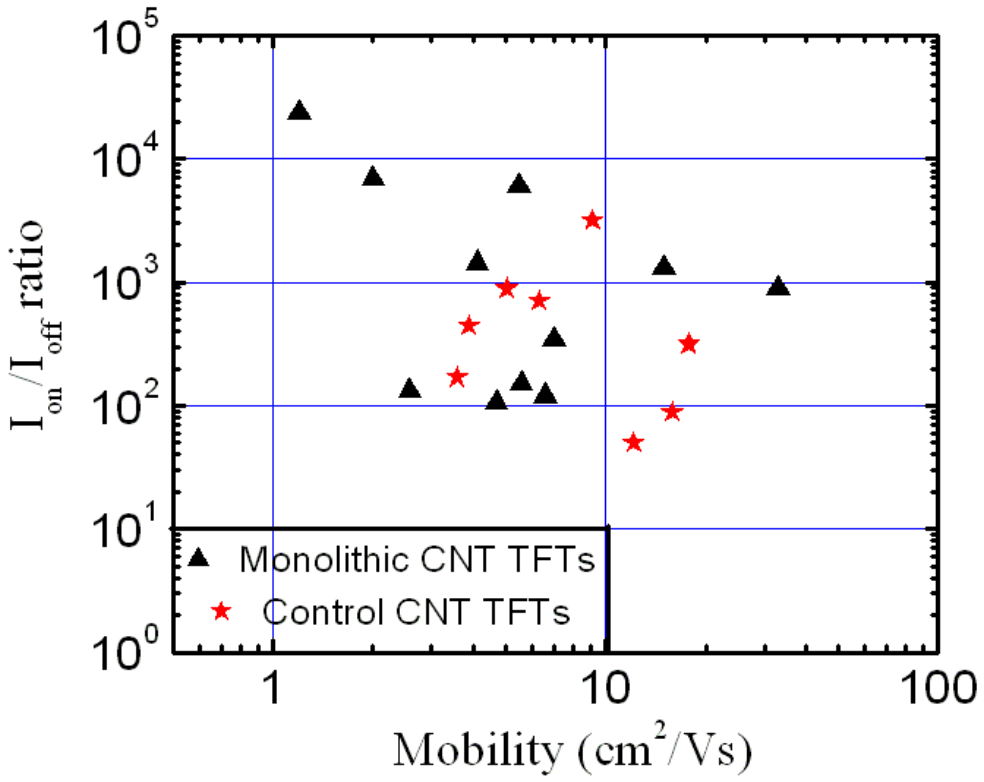


Figure 6.10 On/off ratio is plotted as a function of mobility for all-CNT as well as control CNT devices with L varying in range 10 - 100 μm. The on/off ratio of the devices was increased up to 10^2 - 10^4 after burning metallic paths in the channel.

The contact resistance (R_c) of the device can be estimated by studying the device resistance ($R(L,V_g)$) as a function of L and V_g (i.e. using $R(L,V_g) = \alpha(V_g)L + R_c$). This method is useful if device resistance scales linearly with channel length. In that case, R_c can be obtained by extrapolating R vs L curves to zero channel length. The resistance of a CNT thin film, however, shows a power

law relation with channel length ($R(L,V_g) \propto L^{\beta}$), due to percolation effects. As discussed in Chapter 5, the scaling exponent (β) ranges from 1 to 1.8 depending on CNT density. Previous experimental results [46] as well as theoretical simulations [119] also confirm this. Thus, the linear scaling analysis of the device resistance cannot be employed here to calculate the contact resistance in CNT thin-film devices. Comparable device performance of all-CNT and control devices suggests comparable quality of the contacts. In general, the electrodes and active layer from the same material are expected to have less resistive contact. However, this simplistic assumption may not be valid in a complex material like CNTs. The contact between two CNTs also depends on the chirality of the CNTs. The contact resistance between two semiconducting CNTs and two metallic CNTs is expected to be less than a Schottky contact between a semiconducting and a metallic CNT in reverse bias [121]. The contact between CNT electrodes and active layer could also be affected by remnant impurities in airbrushed CNTs. In fact, the contact between CNTs and Au is not perfectly well understood. Au electrodes have been shown to form Schottky barrier [141] as well as Ohmic contact with CNTs [142]. Experiments done on single CNTs may be better suited to understand the physics of the contact. Here, we conclude from these experiments that the all-CNT TFTs demonstrated here show device performance as good as Au contacted CNT TFTs, even though we were using a low-end quality CNT solution for electrodes (P3 CNTs from Carbon Solutions Inc.). The sheet resistance of CNT electrodes and the device field-effect mobility of all-CNT devices can be further improved by using high quality purified CNT solutions.

6.5 Flexibility of CNT Thin Films

We characterized the mechanical properties of airbrushed CNT thin films by conducting bending experiments. PET stripes coated with airbrushed CNT thin films were wrapped around cylinders of varying diameters to induce tensile strain. The variation in sheet resistance (R_f/R_i; where R_i and R_f are sheet resistance before and after bending) as a function of radius of curvature (r) is plotted in Fig. 6.11. Bending was done in two different ways; by keeping CNT electrodes on the outer side of bent PET (black) and inner side of bent PET (red). In both cases, sheet resistance starts changing at r = 10 mm, but changes only by 7% when the substrate is bent to r = 2 mm ($R_{i,CNT}$ = 500 Ω per square) (see inset of Fig. 6.11). Bending a CNT thin film multiple times also did not significantly change the sheet resistance. Bending a CNT thin film to r = 2 mm 35 times increases the sheet resistance by 12%, most of which occurs during the first few runs. We compared the flexibility of the airbrushed CNT thin film with that of a commercially available In_2O_3/Au/Ag film (Delta Technologies Limited). A PET film sputtered with In_2O_3/Au/Ag showed three orders of magnitude increase in the sheet resistance ($R_{i,In2O3}$ = 10 Ω per square) for r = 3 mm, Fig. 6.11. Unbent In_2O_3 films have smaller sheet resistance than CNT thin films, but CNT thin films are observed to have superior flexibility.

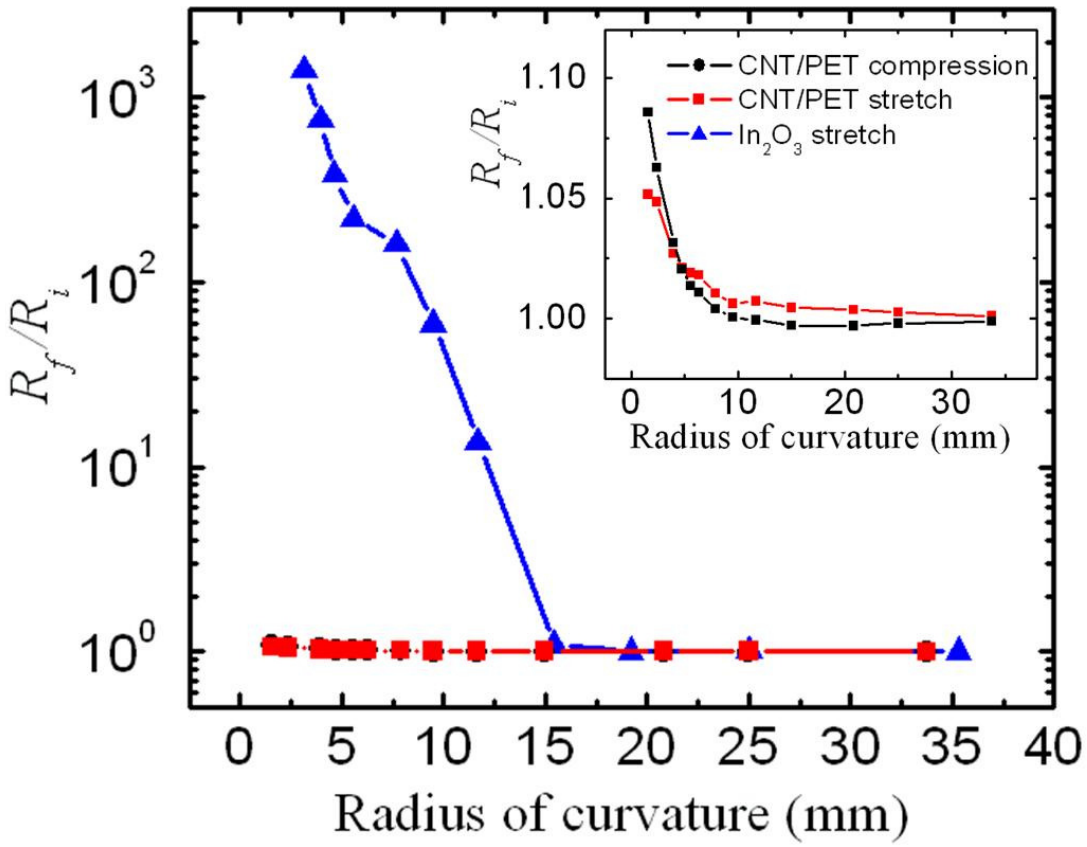


Figure 6.11 Ratio of the sheet resistances, R_f/R_i, before and after bending as a function of the radius of curvature (r) for airbrushed CNT thin film (red squares) as well as In_2O_3 (blue triangles) on a PET substrate. Two different ways were used to induce tensile strain in CNT thin films (black and red curves in the inset, see text). Stretching In_2O_3 thin film results in three orders of magnitude increase in sheet resistance at r = 3 mm. The sheet resistance of CNT thin films increases only by 7% at r = 2 mm (see inset).

6.6 CNT Thin Film Electrodes in Organic Complementary Circuits

Organic semiconductor TFTs were fabricated on air-brushed carbon nanotube thin film electrodes using pentacene, P3HT and C_{60} as active material. First, the CNT/organic semiconductor interface was studied by fabricating organic TFTs on a

Si/SiO_2 substrate. The contact resistance (R_c) of the device was calculated by characterizing the device resistance ($R(L,V_g)$) as a function of L and V_g ($R(L,V_g) = \alpha(V_g)L + R_c$). This experiment revealed $R_c < 30$ kΩ-cm for CNT/pentacene devices and $R_c < 50$ kΩ-cm for CNT/P3HT devices [126]. The contact resistance of both CNT/pentacene and CNT/P3HT devices was found to be lower than that from bottom contact Au/Cr electrodes and comparable to bottom contact Au electrodes (i.e. without using Ti or Cr as the wetting layer). We also demonstrated transparent and flexible pentacene TFTs that use CNT thin film electrodes transfer printed on PET substrate. The average field-effect mobility (on/off ratio) of transfer printed CNT/pentacene devices was observed to be 0.06 cm^2/Vs (5×10^3). Detailed discussion on the CNT/organic semiconductor interface can be found in the doctoral dissertation by Adrian Southard [143].

The transport mechanism in organic semiconductors is very sensitive to the morphology of the thin film. Performance of both pentacene and C_{60} TFTs can be improved by doing surface chemistry on the dielectric layer. Surface treatment by hexamethyldisilazane (HMDS) has been shown to increase the field-effect mobility and on/off ratio and decrease the threshold voltage in pentacene based TFTs [144]. A thin film of polystyrene has been shown to improve C_{60} devices by passivating the charge impurities on the dielectric layer [139]. We do not do any surface treatment in the device discussed here. Thus, though there is ample room for improvement in devices, we focus here on the demonstration of the CNT thin film as an effective electrode material in complementary circuits.

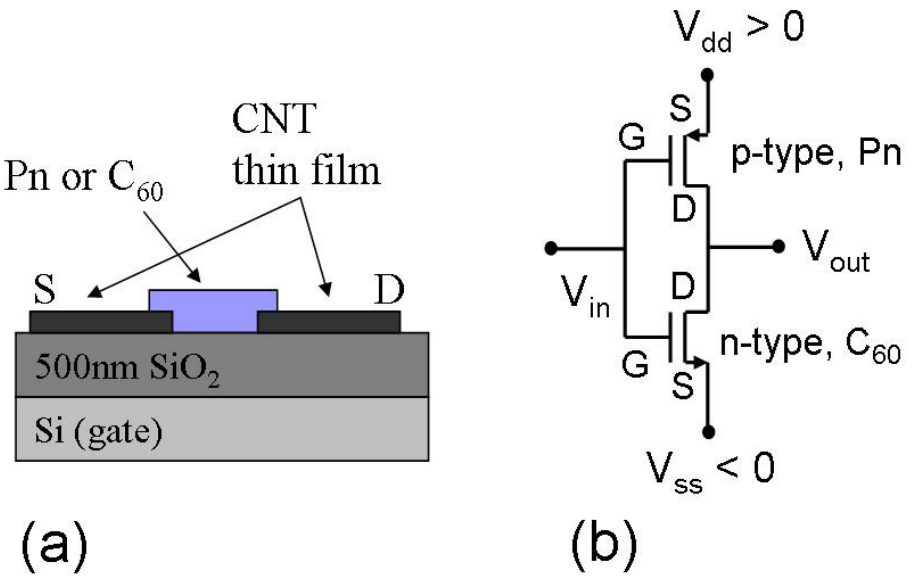


Figure 6.12 a) Schematic of pentacene and C60 TFTs used for complementary circuits. b) Circuit diagram of a complementary inverter using n-type and p-type field effect transistors.

Complementary circuits were fabricated using n-type (C_{60}) and p-type (pentacene) organic TFTs on CNT thin film electrodes. Individual devices were fabricated on a 500 nm SiO_2/Si substrate and connected through an external wire to make an inverter circuit. A schematic of the complementary organic TFTs is shown in Fig. 6.12(a). First, airbrushed CNT thin film source-drain electrodes were patterned by photolithography. Then, organic semiconductor layers, pentacene or C_{60}, were thermally evaporated on the electrodes through a shadow mask. A 40 nm-thick pentacene film was deposited by heating the pentacene cell at 175 ^{o}C (deposition rate = 1 A/sec, chamber pressure = 5 x 10^{-8} Torr) in a home-made MBE system. The substrate was kept at 40 ^{o}C during the deposition. The sample holder (AJA International) was rotated at 30 rpm to obtain a uniformly thick pentacene film. C_{60} film was deposited in a thermal evaporation chamber kept in a dry N_2 glove box. A 200 nm-thick C_{60} film was obtained at a deposition rate of 1.5 A/sec (pressure 2 x

10^{-6} Torr). Devices were fabricated with channel width $W = 2$ mm and channel length (L) varying from 5 μm to 100 μm. Transport measurements of pentacene and C_{60} TFTs were done in a dry N_2 glove box (MBRAUN Unilab (1200/780)). Since exposure to air deteriorates the quality of the C_{60} film, all the experimental steps (growth, wiring and measurements) were carried inside the glove box. Pentacene TFTs were, however, briefly exposed to air during transportation to the glove box. Pentacene devices regained good electrical performance after being kept in a dry N_2 environment for few days.

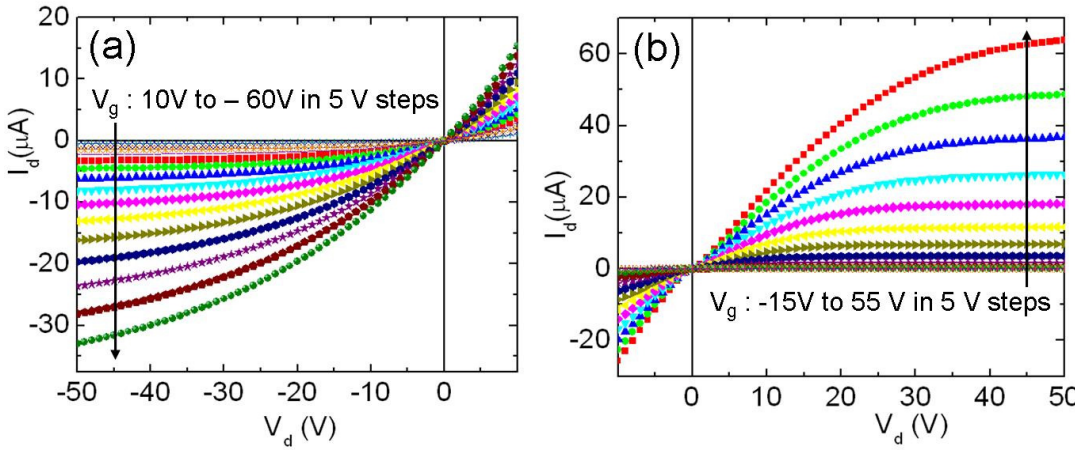


Figure 6.13 a) Output characteristics of a p-type pentacene device ($L = 30$ μm) and b) a n-type C_{60} device ($L = 70$ μm). Both of these devices were made using CNT thin film source-drain electrodes on 500 nm thick SiO_2/Si substrate.

An inverter circuit consists of a pair of complementary FETs (see Fig. 6.12(b)) with their gate electrodes tied together to the input port and drain electrodes tied together to the output port. The source electrode of the pull-up transistor (pentacene) and the pull-down transistor (C_{60}) devices are biased at a positive voltage (V_{dd}) and a negative voltage (V_{ss}), respectively. Output characteristics of a pentacene

and a C_{60} device are shown in Fig. 6.13(a) and (b), respectively. The field-effect mobility of pentacene and C_{60} was obtained as high as 0.09 cm^2/Vs and 0.5 cm^2/Vs with an average of 0.05 cm^2/Vs and 0.3 cm^2/Vs, respectively. In Fig. 6.14(a), transfer characteristics of a C_{60} and pentacene TFT are shown at $V_d = 5$ V and $V_d = -5$ V, respectively. Both types of devices show similar on-state current and field-effect mobility. Typical on/off ratios of pentacene and C_{60} devices were observed to be 10^4 and 10^3, respectively (see Fig. 6.14(b)). The off-state current of C_{60} (10 nA) devices was observed to be an order of magnitude more than pentacene devices (1 nA). A large leakage current in C_{60} devices could be due to the increased likelihood of small molecules shorting to the gate through pin-holes in the dielectric layer.

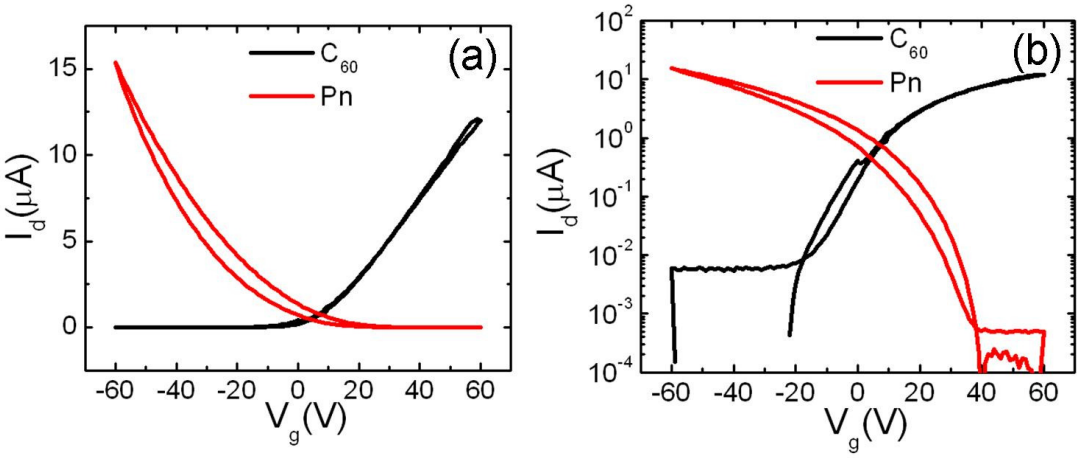


Figure 6.14 a) Transfer characteristics of C60 and pentacene TFTs are compared at $V_d = 5V$ and $V_d = -5V$, respectively. b) Transfer characteristics of the C_{60} and pentacene TFT is plotted on a logarithmic scale to show off-state currents of the devices.

The voltage transfer characteristic of a pentacene-C_{60} inverter is shown in Fig. 6.15(a). A symmetric voltage transfer curve means equal noise margin in both the complementary devices. Here, voltage transfer is nearly symmetric. The switching

happens quite close to $V_{in} = 0$ V (the ideal switching voltage = $(V_{dd} + V_{ss})/2$). For a symmetric transfer characteristic, the transconductance parameters of the devices must be equal, a condition called 'matching'. Thus the condition for matching is

$$\mu_p \left(\frac{W}{L}\right)_p = \mu_n \left(\frac{W}{L}\right)_n , \qquad 6.1$$

where the subscripts p and n are used to denote the devices parameters of p- and n-type transistors, respectively. In this particular case, we have $W_p = W_n = 2$ mm, $L_p =$ 30 μm, $L_n = 70$ μm, $\mu_p = 0.05$ cm^2/Vs and $\mu_n = 0.3$ cm^2/Vs. Thus, the ratio of device parameters is

$$\frac{\mu_p \left(\frac{W}{L}\right)_p}{\mu_n \left(\frac{W}{L}\right)_n} = 0.38 . \qquad 6.2$$

Since this ratio is quite close to the ideal value of 1, a nearly symmetric transfer curve obtained for this inverter. By controlling the device geometry (e.g. L) a perfect matching condition can be achieved. Comparable field-effect mobility in our devices allows us to obtain symmetric transfer curves for an inverter made from devices with comparable geometry.

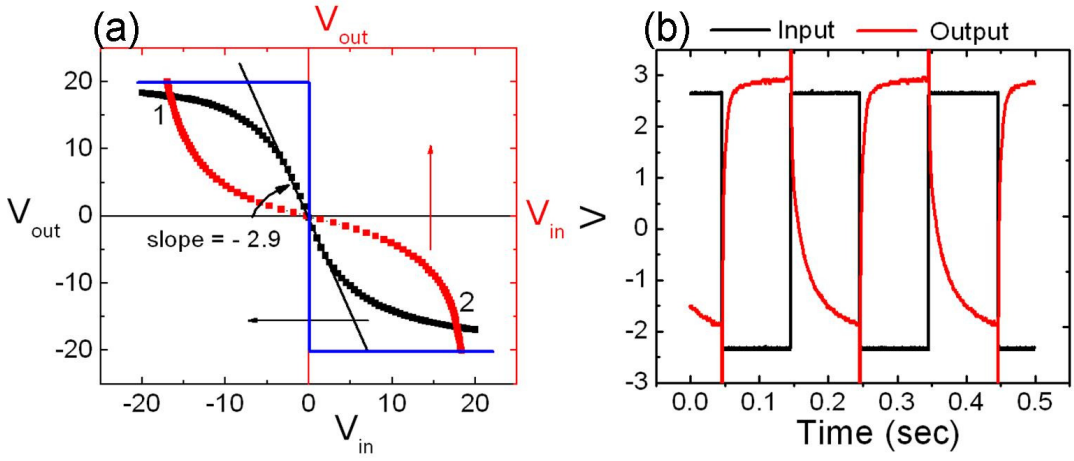


Figure 6.15 a) Input-output voltage transfer characteristic of a pentacene-C_{60} inverter. b) Input and output waveforms of the inverter at frequency 5 Hz.

The blue line in Fig. 6.15(a) represents the transfer curve of an ideal inverter. The output voltage swing (V_{out}: – 17 V to 18 V for V_{in}: – 20 V to 20 V) is somewhat lower than the ideal value (V_{out}: V_{ss} to V_{dd}). It also takes rather large input voltage (~ 20 V) for the output voltage to saturate. This deviation from an ideal inverter is because none of these complementary devices is completely turned 'off' for any value of V_g (V_{in}) between – 20 V and 20 V (see transfer characteristics in Fig. 6.14(b)). The operating voltage of an inverter can be reduced by reducing the threshold voltage of the complementary transistors, e.g. by increasing the capacitance of the dielectric layer. The input dc current of our inverter is also rather large, 10 nA (due to gate leakage in C_{60} device). Both of these limitations can be overcome by fabricating high quality devices on surface-treated dielectric layers.

Fig. 6.15(b) shows the output waveform of the inverter in response to a square waveform. The speed of the operation is characterized by 'propagation delay', the time taken for the output voltage to drop to switching voltage (0 V in our case). The propagation delay for the pentacene and C_{60} devices was approximately 3 ms and 8

ms, respectively. The output voltage decay can be fit to a capacitor discharge equation. Thus, propagation delay is determined by capacitance of the device channel. The ratio of propagation delay for this inverter, 0.375 (3/8) is quite close to the ratio of matching parameters, 0.38. Capacitance of the devices can be reduced by using smaller channels. Here, a large device geometry was chosen for ease of fabrication in this proof-of-concept demonstration.

One of the applications of inverters is ring oscillators. For a stable 5-ring oscillator, the slope of the voltage transfer curve must be less than – 1 at the switching voltage (0 V). The inverter transfer curve in Fig. 6.15(a) (slope = – 2.9) fulfills this condition. An inverse voltage transfer curve, V_{in} versus V_{out}, (red curve in Fig. 6.15(a)) is also plotted in the same graph. The two transfer curves intersect at three points; the origin and the points denoted by 1 and 2. A stable oscillator is expected to oscillate between the points 1 and 2. Thus, organic complementary circuits based on CNT thin film electrodes could also be utilized in 5-ring oscillators.

6.7 Conclusions

We have demonstrated fabrication techniques to incorporate transparent airbrushed CNTs as electrodes to achieve all-CNT and organic TFTs on large area of transparent, flexible substrate. Airbrushed CNTs are solution processed at room temperature to achieve sheet resistance of 1 kΩ per square at 80% transparency. Conductivity of CNT thin film can be further improved by purifying a well-dispersed solution of long metallic CNTs through differential ultracentrifugation [41]. We presented sequential printing methods to achieve 100% transfer of airbrushed CNT to

8 different polymer films. CNT thin film electrodes were also incorporated in complementary organic devices (Pn and C_{60}). These devices showed comparable transconductance and symmetric voltage transfer in an inverter circuit. Finally, the nontransparent element (Au electrodes) in CNT thin film devices are substituted with transparent CNT electrodes while achieving similar device performance. Superlative flexibility of CNT thin films offers additional incentive for their exploitation in flexible electronics.

Chapter 7 : Voltage Contrast in Photoelectron Emission Microscopy

Using voltage-induced image contrast for analysis of integrated circuits (IC) is a well known technique [145, 146]. Both the scanning electron microscope (SEM) and focused-ion beam tools use this type of contrast to test circuits on IC chips. This is done by applying an external bias to a specimen and analyzing variations in image contrast to determine if a circuit functions properly. However, image as well as specimen degradation can occur from prolonged exposure to a charged-particle beam, and thus can limit device testing [147]. Limitations are mainly due to deleterious beam effects such as inelastic scattering of electrons, inadvertent ion implantation, as well as surface sputtering, all of which can permanently damage the device under test.

Imaging surfaces with low energy electrons with techniques like low energy electron microscopy (LEEM) [148-152] and photoelectron emission microscopy (PEEM) [153-156] is also well established. These techniques generate real-time in-situ images of the surface that can be used to analyze the device. In PEEM, the imaging electrons are generated by near-threshold photoemission, and thus the image intensity is sensitive to surface fields. This means that non-destructive voltage contrast can be acquired with PEEM. However, the lateral fields responsible for the contrast can arise from either an externally applied bias or in combination with surface topography. By varying the external bias, voltage contrast and topography contrast can be readily distinguished.

In this chapter, we describe how PEEM voltage contrast arises when an external voltage is applied to a device. To achieve this, we have fabricated test structures that allow the two types of image contrast to be distinguished. The voltage contrast behavior is characterized by comparing measured voltage contrast with calculated voltage contrast from two different models. In the first model, electron trajectories are numerically simulated to quantify the intensity profiles. In the second model, an electron optics formulation developed by Nepijko [157-160] is used to quantify the intensity profile. Agreement between the measured and calculated voltage contrast as well as topography contrast suggests that simple electrostatic models are sufficient to describe voltage contrast in PEEM. Although fundamentally different, PEEM voltage contrast can be used in the same manner as voltage contrast is used in SEM and FIB tools.

7.1 Photoelectron Emission Microscope

Photoelectron emission microscopy (PEEM) has unique features which enable the user to obtain real-time images of biological materials, metals, semiconductor electronic devices and other sub-micron scale structures in a non-intrusive manner [161-164]. Historically, this imaging technique has been used to investigate nanometer-scale surface chemistry, organic substances, thin-film magnetism, polymers, morphology and visualization of electronic devices based on unconventional contrast mechanism [161, 165].

Two main features of photoelectrons emitted from a material are photo-electron yield and kinetic energy; these have been utilized by microscopy and

spectroscopy, respectively, to obtain information about the material. The yield can be used to obtain spatial information about the positions from which photoelectrons are emitted, which led to development of one of earliest electron microscopes, PEEM. In near-threshold PEEM, UV light is focused on the sample whose photo-threshold is almost equal to the energy of the incident photons, producing low energy electrons. These low energy electrons are accelerated through an applied electric field before being imaged by an electrostatic lens system. PEEM is an important probing tool because it possesses features which are not found in other microscopes. The image is formed by the continuous emission of electrons from the illuminated area of the sample (parallel imaging) rather than by scanning the sample (sequential imaging). Therefore, this real-time imaging technique enables one to observe in-situ sample changes.

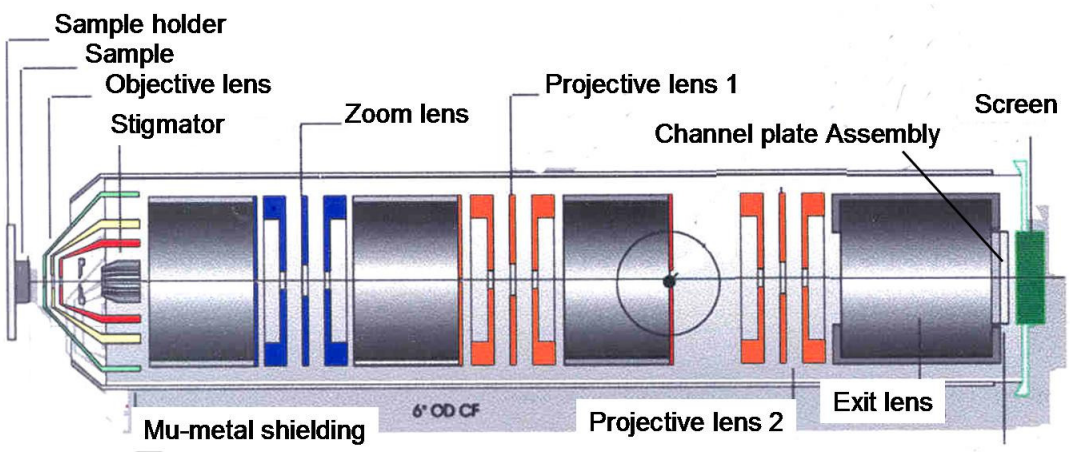


Figure 7.1 Schematic of the PEEM systems with all major components labeled. (Courtesy of Staib Instruments)

7.2 Optics of Image Formation in PEEM

A photoelectron emission microscope is schematically shown in Fig. 7.1. The specimen is located in the UHV chamber, the leftmost part in the diagram, and is illuminated with light from an off-axis UV lamp. Electrons emitted by virtue of the photoelectric effect are accelerated by the high electric field between the sample and the first lens element of the microscope. The effect of an accelerating electric field on the electrons is conceptualized as an immersion lens. The immersion lens is also referred to as a cathode lens, and the fringing fields at the aperture of the anode produce a virtual image that is focused by the objective lens. The objective lens is a modified Einzel lens, as shown in Fig. 7.1. The remaining part of the system involves an electrostatic lens system used to magnify and transfer the information carried by the electrons onto the phosphorus screen, producing a visible image. A channel plate is used to amplify the photo-current signal (~ nA), making real-time data acquisition possible. In PEEM, the specimen is part of the microscope and the physics of image formation happens in the cathode lens (i.e. contrast, resolution and aberrations). So, it is sufficient to analyze the electron optics in the cathode lens alone to understand the fundamentals of image formation.

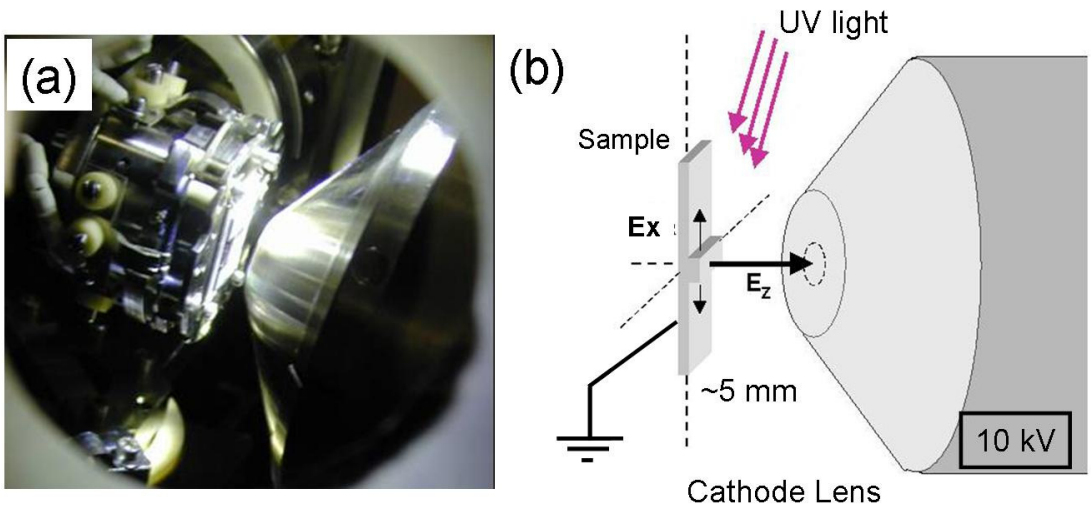


Figure 7.2 a) A picture of sample holder in the PEEM sample region which acts a cathode lens. b) Schematic of the cathode lens in PEEM.

Fig. 7.2(a) shows a picture of the PEEM chamber. Our PEEM system uses a Hg arc lamp with maximum photon energy around 5.1 eV whereas the photo-threshold of Si (a commonly used material) is 5.0 eV. An electric field of 2 x 10^5 V/m is produced by applying 10 kV (V_a) to the aperture lens which is kept at a distance ~ 5 mm (l) away from the grounded specimen (i.e. cathode). This field is substantially uniform except in the immediate vicinity of the anode aperture. The disturbance created by the aperture acts as a thin diverging lens. If the surface of the specimen is perfectly flat, all the electrons will follow simple parabolic trajectories in the uniform electric field. However, a spatial non-uniformity in the local fields on the specimen can be caused by any one or a combination of parameters like topography and bias. This non-uniformity results in electric field perturbation near the surface of the sample. The lateral component of the perturbed electric field is responsible for producing certain types of contrast observed in PEEM. To understand the basic

image formation mechanism further, we will consider geometrical optics where electron beams are taken as rays and the specimen is assumed to be planar.

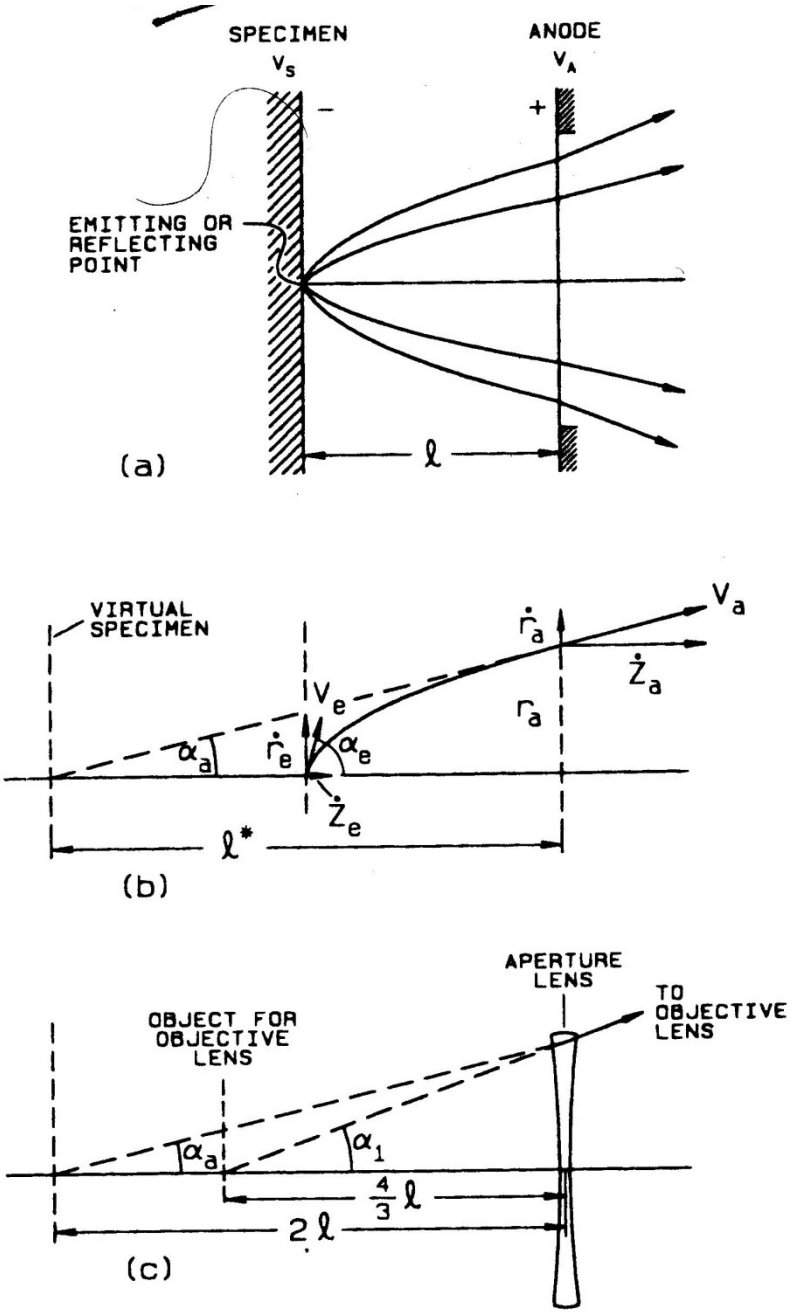


Figure 7.3 a) Trajectories of electrons emitted from a flat surface follow parabolic paths. b) Tangent of the trajectory defining the virtual specimen at *l**. c) Optics of uniform field combined with diverging aperture lens. (Illustrations are taken from Rempfer et al [154])

The image formation process can be thought of as occurring in two steps [154]. First, the electron is emitted from the specimen surface with a velocity V_e and an angle α_e (w.r.t. z axis, optical axis of PEEM. It will trace a parabolic trajectory (Fig. 7.3(a)) and pass through the aperture plane with velocity V_a at angle α_a (w.r.t. z axis). If the tangents to these parabolic curves are extrapolated backward, they would meet the optical axis at the virtual specimen plane located at distance l^* from the anode, Fig. 7.3(b). l^* is given by

$$l^* = 2l\left(1+\frac{z'_e}{z'_a}\right)^{-1}, \qquad 7.1$$

where z'_e and z'_a are the z components of the initial velocity and the velocity at the aperture plane, respectively. In the second step, the virtual specimen plane acts as the object for the aperture lens whose focal length is $f_A = -4l$. Thus, the aperture lens forms a virtual image of the virtual specimen at a distance of around $(4/3)l$ from the anode with a lateral magnification of $2/3$, Fig. 4(c). Though the aperture lens (and subsequent lenses) can change the magnification, the image formation happens in the cathode lens. Thus, we will neglect the effects of the aperture lens (and subsequent lenses) in the simulation and analytical model discussed in this chapter. The final image will be obtained by simulating the distribution of electrons at the aperture lens plane.

7.3 Fabrication of the Devices

To generate potential gradients at the sample surface in a controlled manner, layered device structures were fabricated where the top metal layer is electrically

isolated from the bottom metal layer. This process was used previously for fabrication of devices used to characterize topography-induced contrast in PEEM [166]. Thin films of Ti (500 nm), SiO_2 (200 nm) and Ti (100 nm) were successively deposited on a clean Si wafer by electron-beam evaporation. The tri-layered wafers were then patterned by photolithography using a positive photoresist (908 20 HC, Fujifilm). The photoresist was used as an etch mask and the exposed surface was etched to the bottom Ti layer in a reactive ion etcher with a SF_6 plasma (pressure = 525 mTorr, rf power = 550 W). The etching time was carefully controlled in order not to overexpose the underlying Ti thin film. Finally, the photoresist was removed in heated n-methyl pyrolidinone to obtain sets of isolated raised lines which could be independently biased. The thickness and profile of the resulting Ti and SiO_2 bi-layer was characterized by profilometry and SEM. A cross-sectional schematic of the sample is shown in Fig. 7.4(a). A scanning electron micrograph of the sample (see Fig. 7.4(b)) confirms the desired vertical profile of the bi-layer with a total thickness of 350 nm. Topography contrast samples consist of rectangular Ti bars on the underlying Ti surface without an insulating SiO_2 thin film. Topography samples of different heights were etched using SF_6 plasma with the same photolithography process as in voltage contrast samples.

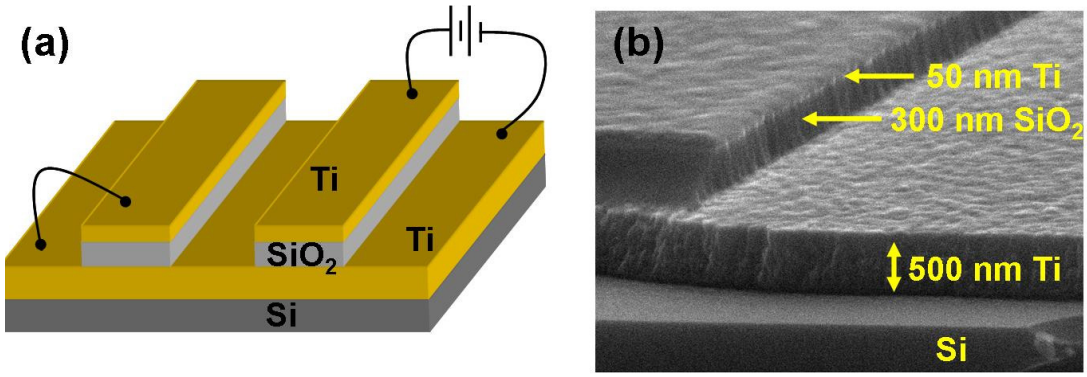


Figure 7.4 (a) Schematic of a tri-layered sample for voltage contrast.
The top layer can be independently biased with respect to the background Ti surface.
(b) An oblique SEM micrograph of the sample shows different layers.

7.4 Measurement and Image Analysis

After the sample is introduced into the UHV ($5x10^{-9}$ to 10^{-8} Torr) chamber, it is aligned by moving it with a 5-axis (3 translational and 2 rotational) manipulator (Thermionics) which has translational precision of 1 μm. The stage was carefully positioned to keep the sample approximately 5 mm from the aperture lens. The final image is formed on the phosphorus screen. The images were recorded using a 16-bit CCD camera which produces a 1280 x 1024 bitmap and stored in 12-bit tif format. The data acquisition software (PCO) allows for variation in camera exposure time, averaging of several consecutive images, background subtraction and noise correction. All the images for the voltage contrast were taken with an exposure time of 0.8 sec and averaged over 16 exposures. The image intensity was quantified by averaging line-scans along 200 parallel lines to obtain an averaged intensity profile. Line-scans were taken by IDL 6.1 codes provided in Appendix D. To correct for background intensity fluctuations, a 10^{th} order polynomial was first fitted to the average background intensity profile while substituting the edge intensity curves with

linear interpolation, and then subtracted from the original line scan data. Image contrast can be characterized by any of three parameters: the area under the curve A, full-width half-minimum Γ and depth of the intensity dip d. However, d and Γ tend to be more sensitive to fluctuations in the intensity peak than A. Moreover, A is also more amenable in comparing with numerical simulations. Therefore, we quantified the experimental contrast using the area A_{expt}, which is calculated as the area under the intensity profile between the two points where intensity increases by 90% of the minimum intensity at the dip. A_{expt} was calculated using MATLAB codes provided in Appendix E.

7.5 Contrast Mechanisms in PEEM

An important feature of PEEM is its novel contrast mechanisms. Contrast of an image depends on many parameters like the photo-yield of the material, topography, bias and doping, providing an excellent way of characterizing samples, which may be otherwise impossible with other microscopes. Here, we will limit the discussion to topography and, especially, voltage contrast.

7.5.1 Topography Contrast

Any geometrical relief in a planar specimen would result in local distortion in the uniform electric field in order for Dirichlet boundary conditions to hold. This can be best illustrated by an example of electrostatic simulation done by the finite element method (Poisson Superfish [94], Appendix C). Fig. 7.5(a) shows simulations of electric field (arrows) and equipotential surface (lines) in the vicinity of a 300 nm

wide and 100 nm thick topography sample. The perturbation of the electric field near the edges is clearly visible. Electrons passing through perturbed electric fields will trace different trajectories resulting in contrast in the image (red arrows in Fig. 7.5(b)). Thus, the Gaussian imaging condition for these electrons is destroyed. Electrons emitted from the edge of a step, where the field is drastically perturbed, may not even reach the objective lens so the edges will show up as dark lines in the image. It is primarily the lateral component of electric field (E_x) that is responsible for topography contrast.

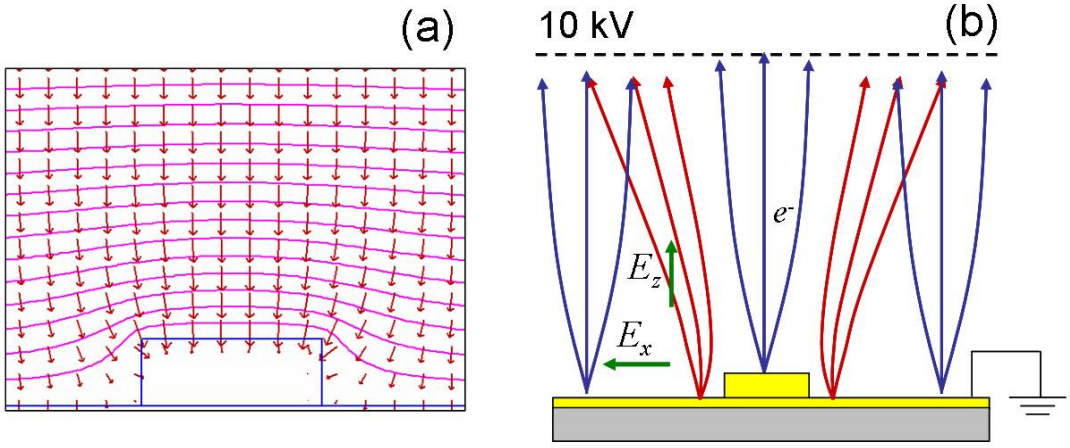


Figure 7.5 a) Electrostatic simulations show perturbation of the electric field (arrows) near the edges of a metal line of height 100 nm. Horizontal lines depict equipotential surfaces. The sample was grounded and the aperture lens was kept at 10 kV. b) Schematic of trajectories of electrons emitted from a grounded topography sample. Trajectories of electrons emitted near the sample edge (red lines) are perturbed by lateral component of the electric field (E_x). The dashed line shows aperture lens plane.

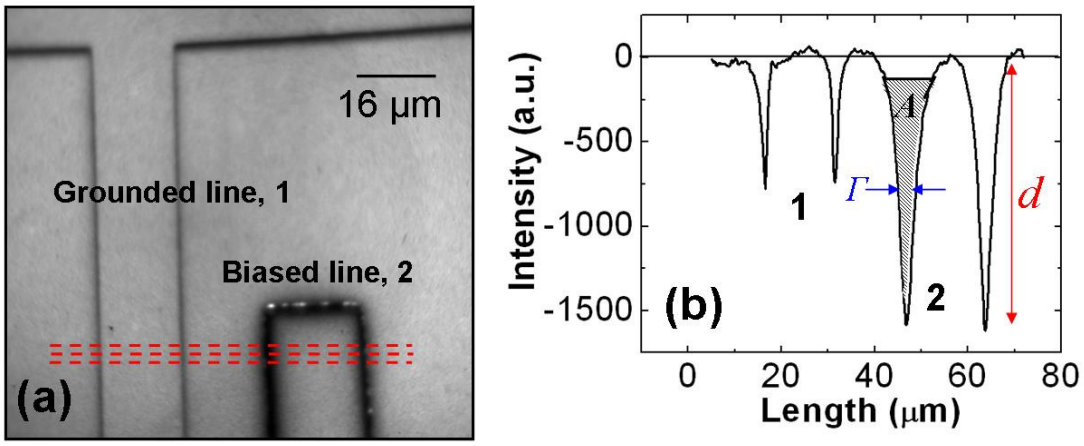


Figure 7.6 a) A PEEM image of a sample showing the effect of bias on imaging contrast. b) Intensity scans were averaged over 200 lines in the region depicted by dotted lines in (a). Intensity dips in the biased sample show increase in full width half minimum (Γ), depth (d), and hence the area (A) under the curves.

7.5.2 Voltage Contrast

The fundamental principle of voltage contrast is not different from topography-based contrast. In voltage contrast, we can control the local field modulation by systematically varying the applied voltage on the sample. To illustrate voltage contrast, we briefly describe a typical PEEM image of the device in Fig. 7.6(a). Shown in the image is a pair of 16 μm wide structures with a separation of 16 μm. The top Ti layer in the Ti/SiO_2/Ti structure at the left (1) is shorted to the underlying Ti surface and grounded in order to get direct comparison between the biased and unbiased structures. The Ti line on the right (2) is externally biased at 5 V with respect to the background Ti surface. The contrast observed along the edge of Ti line 1 is solely due to topography, whereas the contrast observed along the edge of Ti line 2 is due to both topography and the external bias. Fig. 7.6(b) shows an intensity profile averaged from 200 line scans taken along a group of dashed lines shown in Fig. 7.6(a). The 4 features arise from the contrast at the edges of the lines. In this

particular case, A, Γ and d for the biased (5 V) structure are approximately 6.5, 2.5 and 2 times, respectively, larger than the corresponding parameters for the unbiased structure. The external bias increases contrast at the edges of line 2 in magnitude and lateral extent. Therefore, calculating the electric field near the edge of the metal line is necessary to determine the effect of bias on image intensity profile.

7.6 Numerical Model

The numerical model used to describe the measured intensity profile calculates the electron trajectories in the PEEM immersion lens. The calculation was done by SIMION 7 [83] which uses a finite difference method to calculate the electric potential, and a Runge-Kutta method was used to calculate the electron trajectories. The top plate of the simulation box (100 μm x 100 μm; grid size: 5000 x 5000) was biased at 200 V ($10\text{kV}\times 100\mu\text{m}/5\text{mm}$) to obtain the desired E_0 (2 V/μm). Neumann boundary conditions were set on the side edges. The initial kinetic energy of the electrons was assumed to be 0.3 eV. The electrons were emitted at angles -10^{o}, -6^{o}, -2^{o}, 0^{o}, 2^{o}, 6^{o}, 10^{o} with respect to the surface normal at each of the 150 regularly spaced emission points on both sides of the edge of the sample. A sample of electron trajectories from 12 emission points near an edge of a voltage contrast sample is shown in Fig. 7.7(a). The top metal layer of the sample was biased at – 1 V. The position and velocity of the electrons at the top plate of simulation box were used as initial conditions to simulate the electron trajectories in the bigger simulation space (from y = 100 μm to y = 5 mm i.e. whole PEEM immersion lens). The field perturbation due to the sample is neglected in this region and the analytical

expression of electron trajectories in a uniform electric field E_0 is used to trace the parabolic rays of the electrons (using MATLAB codes provided in Appendix E). The array of x coordinates of electrons at the aperture lens plane (y = 5 mm) is taken to represent the distribution of the electrons exiting the acceleration region of the microscope. In Fig. 7.7(a), the electrons emitted near the edge of the metal line are strongly displaced due to the tangential field strength E_x on the electron trajectories. Extrapolating the trajectories backward, the point where the tangent lines intersect to form a virtual image depends on the magnitude of E_x. Near the edge of the metal line, the virtual image is displaced by 14% from the true virtual plane, and the central angle of the electron trajectories is offset from normal by approximately 15 degrees (larger than acceptance half-angle of our system ~ 6 degrees). This means that the affected region of the virtual object plane is no longer conjugate with the true virtual image plane and thus will not appear in focus in the final image. In the following, we will use distribution of electrons over the array of x coordinates at the anode plane (z = 5 mm) to represent the distribution of the electrons at the anode plane.

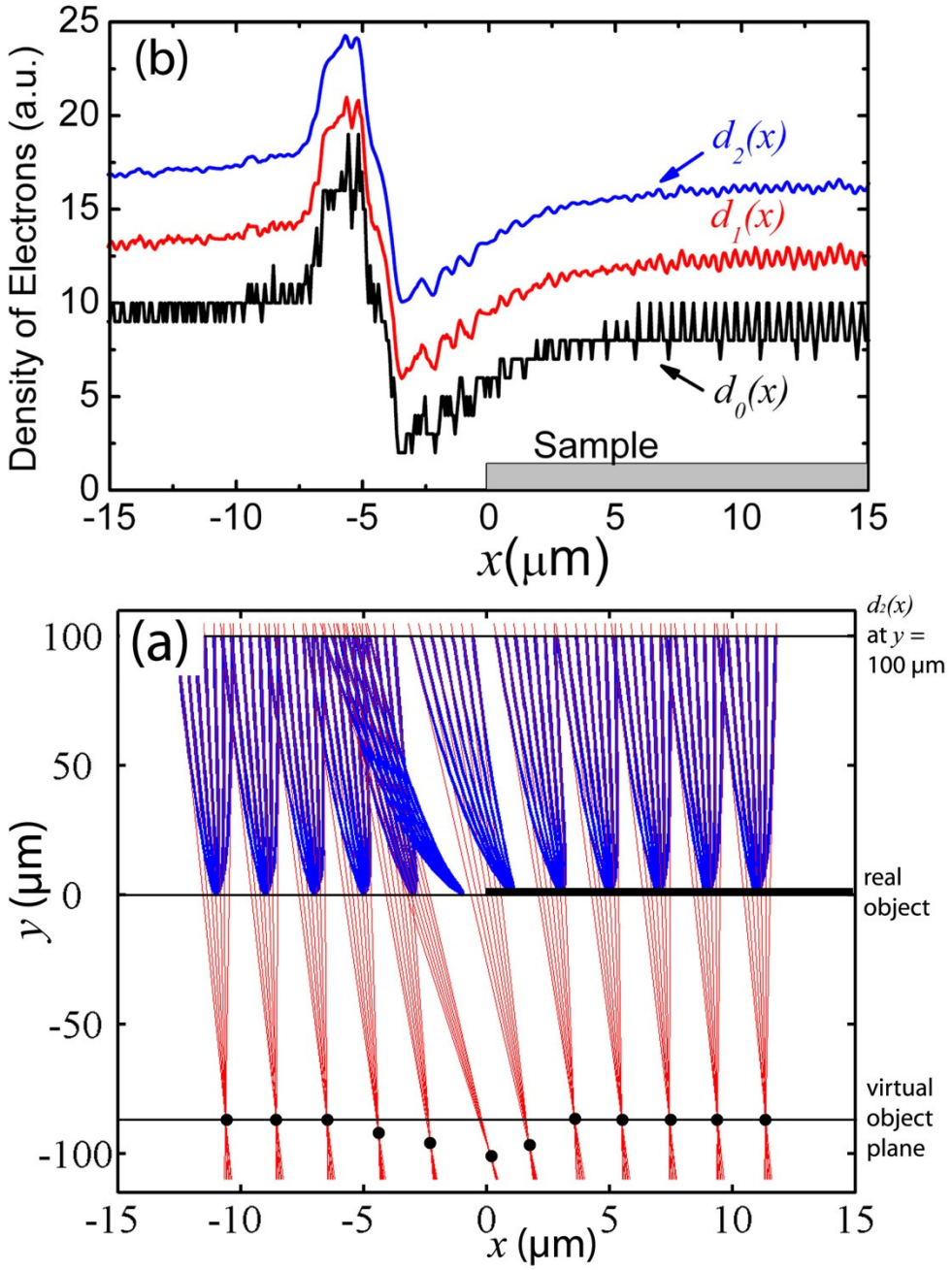


Figure 7.7 a) Electron trajectories simulated using SIMION 7 when the sample is biased at – 1 V. The electrons emitted at near the sample edge with initial angles – 10°, – 6°, – 2°, 0°, 2°, 6°, 10° with respect to the surface normal The tangents (red lines) of the trajectories at z = 100 μm are extrapolated back to form the virtual specimen plane for illustrative purpose. The points of least confusion for the perturbed electrons are deviated from the virtual specimen plane by up to 15 %. b) Digitized density of electrons $d_0(x)$ at the aperture lens plane (z = 5 mm) and averaged densities $d_1(x)$ and $d_2(x)$ plotted as a function of position, x. The y axis corresponds to $d_0(x)$ and subsequent plots are shifted by 3 units.

The density of exiting electrons d_0 is calculated as a function of x by counting the number of electrons in uniformly spaced segments along the x coordinate (using MATLAB codes provided in Appendix E). Due to the finite numbers of electron rays in the simulation, $d_0(x)$ showed fluctuation between discrete levels. A smoother distribution $d_1(x)$ was obtained by doing a running average over five nearest neighbors in $d_0(x)$. This process was repeated again in $d_1(x)$ to obtain an even smoother distribution $d_2(x)$. Fig. 7.7(b) illustrates how this averaging technique minimizes the numerical noise generated in the calculation. Since every electron that is emitted from the sample (i.e. cathode) is counted at the anode plane, the peaks and dips shown in Fig. 3(b) arise from charge conservation. Thus, the area of a dip is equal to the corresponding peak area in $d_2(x)$. The dip area quantifies the decrease in electron density per unit length while the peak area quantifies the increase in electron density per unit length. However, the peak area does not necessarily correspond to brighter intensity in the final image. This can be understood by examining the virtual image formation shown in Fig. 3(a). In segments of $d_2(x)$ where the electron distribution is high (producing a peak in $d_2(x)$), electrons strongly deflected by the lateral electric field are contributing to the electron density. As mentioned above, the virtual object plane for the perturbed electrons is not the same as the virtual object plane of the unperturbed electrons. Thus, the peak areas in $d_2(x)$ include electron density that will not be focused to a corresponding bright intensity in the final image.

The numerical electron density distribution can also be thought of as a result of the displacement of electrons from the intensity dip to the intensity peak due to the lateral component of the electric field. However, in practice we have a contrast

aperture (diameter 70 μm) in the back focal plane of the microscope. The absence of intensity peak in the final image can also be partially attributed to the contrast aperture where some of the electrons deviated by large angles are eliminated before reaching the imaging plane. The affect of these deflected electrons appears as the dip area, which thus is used to quantify the affected region of the virtual image plane. The area of the minimum peak A_{num} was determined in the same manner used for the measured contrast (i.e. the area between the two points where intensity increases by 90 % of the minimum intensity at the dip) (Appendix E).

7.7 Analytical Model

We also utilized an analytical treatment [157-160, 167] to quantitatively predict the electron density distribution in the PEEM image due to the local electric fields on the sample surface. This method has been used earlier to model image deterioration in PEEM [160] and surface potential mapping of microelectronic devices in PEEM [159]. We use it here for modeling PEEM contrast induced by externally biasing a specimen. Deflection of the electron trajectories due to the local fields is calculated with a first order approximation. A Cartesian coordinate system is chosen such that the *x*-*y* plane coincides with the sample surface, and the *z*-axis coincides with the optical axis of the cathode lens in PEEM. The long rectangular samples studied here allow us to assume that the local electric potential varies only along one of the coordinates (chosen as *x* in Fig. 7.2(b)). We also assume absence of the contrast aperture in the model used here. The photoelectrons are traced through the acceleration region without any restriction, and thus the total electron current is

conserved. The shift in electron trajectories S as a function of local electric potential ϕ is derived from Dyukov et al. [157] and is given as [167]

$$S(x) = \frac{1}{\pi E_0} \int_{-\infty}^{\infty} \phi'(x-\xi) \ln(1+\frac{l^2}{\xi^2}) d\xi, \qquad 7.2$$

where E_0 is accelerating field, and l is the distance between the sample surface and aperture lens. When the top layer of the device is grounded, the surface of the sample is an equipotential. Thus, in the vicinity of the surface, the electric potential can be assumed to follow the contour of the topography (i.e. $\phi_{topo}(x) = E_0 h(x)$).

Furthermore, the rectilinear step can be approximated as a smoothly varying step of height h_0 and half-width a,

$$h(x) = \frac{h_0}{\pi} \tan^{-1} \frac{x}{a}. \qquad 7.3$$

When the surface of the metal line is biased with respect to the grounded background surface, the surface of the metal line is not an equipotential. However, the effect of external bias on the topography can be taken into account by changing the height of the step such that it becomes an equipotential surface. An external bias of voltage V_{bias} would correspond to the change in height of the step by V_{bias}/E_0. Therefore, the local electric potential for a biased sample takes the form

$$\phi_{bias}(x) = \frac{(E_0 h_0 - V_{bias})}{\pi} \tan^{-1} \frac{x}{a}. \qquad 7.4$$

Differentiation and substitution of this expression for the electric potential in Eq. 1 yields a shift of the form

$$S(x) = -\frac{(E_0 h_0 - V_{bias})}{2\pi E_0} \ln \frac{x^2 + (1+a)^2}{x^2 + a^2}. \qquad 7.5$$

The role of the local electric field is to redistribute the electron current density in a plane as dictated by the expression for shift given above. For a planar sample, the electrons are nominally collected at a point x. However, in the presence of a local perturbation due to external biasing or topography, the electrons are collected at a point $x + S(x)$. The redistributed electron density is expressed in terms of the shift as [158]

$$j(x+S) = \frac{j_0(x)}{1 + dS/dx}, \qquad 7.6$$

where $j_0(x)$ is the distribution of electrons in the case of a planar sample and is a constant (designated j_0). After substituting the expression for $S(x)$ in Equation (4), we get

$$j(x+S) = j_0\left(1 - \frac{(E_0 h_0 - V_{bias})(a^2 + x^2)\left(\frac{2x}{a^2 + x^2} - \frac{2x\left((a+l)^2 + x^2\right)}{(a^2 + x^2)^2}\right)}{2E_0\pi\left((a+l)^2 + x^2\right)}\right)^{-1} \qquad 7.7$$

where we can assume that $j_0 = 1$ since the intensity is in arbitrary units. The expression for $j(x)$ in Eq. (5) gives the intensity profile for a sample with a specified height h_0, and applied voltage V_{bias}. Other parameters were kept the same throughout the calculations reported here (E_0 = 2 V/μm, l = 5 mm and the edge smoothness parameter a = 100 nm). The same expression is used to calculate topography contrast by taking V_{bias} = 0 V. Since this analytical formulation does not take into account the contrast aperture, a peak in the intensity profile is produced next to the dip. The analytical contrast is characterized as the area under the intensity dip A_{theo} in the same manner as the numerical contrast A_{num} and measured contrast A_{expt} (Appendix E).

7.8 Results and Discussion

First, we will consider voltage contrast in PEEM. A set of PEEM images of a 300 nm tall isolated Ti line were acquired as the external voltage was varied from – 6 V to 6 V in steps of 1 V. The inset in Fig. 7.8 shows a set of corrected line scans taken over the edge of the line for 0 V to – 5 V, and clearly illustrates the effect of biasing the line. As the bias increases (both polarities), the image intensity near the edge of the line decreases and the lateral extent of the affected area increases. Both of these features can be seen by examining A and the corresponding Γ as shown in Fig. 7.8, which also illustrates that either A and Γ can be used to quantify voltage contrast. In addition, the measurements show that both quantities have a minimum near $V_{bias} = 1$ V, not at $V_{bias} = 0$ V. As shown below, the magnitude of A at $V_{bias} = 0$ V is due to the height of the metal. Although not shown here, the measured intensity starts to saturate at higher biases ($|V_{bias}| > 8$ V) due to the limited dynamic range of the channel plate.

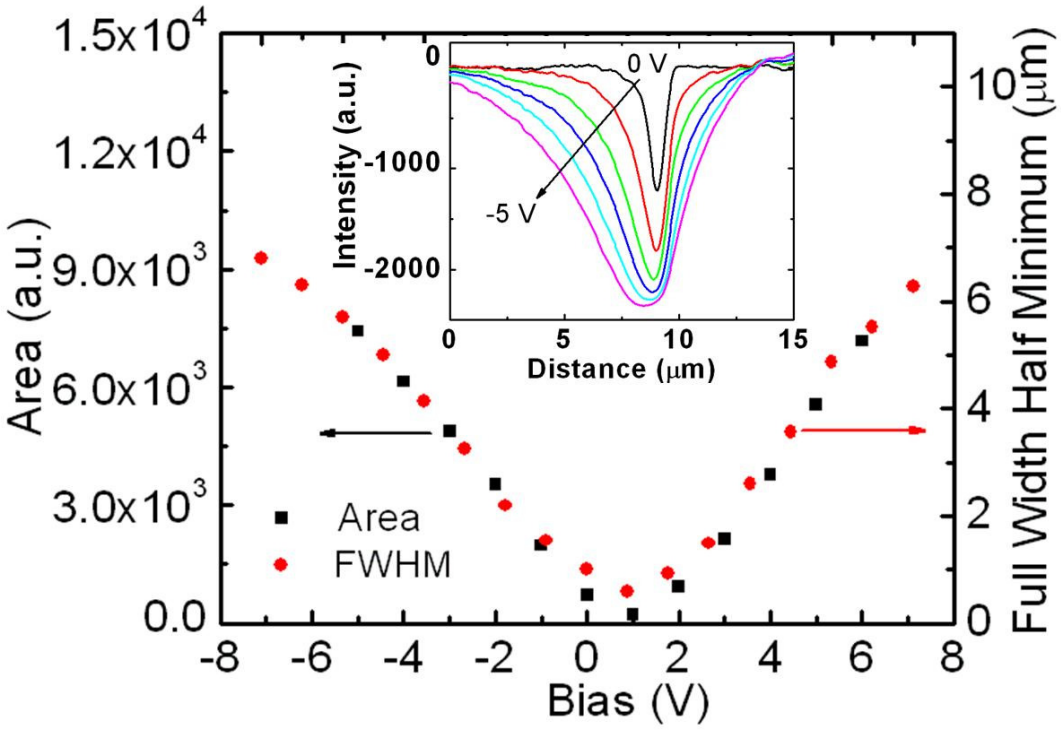


Figure 7.8 The area under the curve A and the full width half minimum Γ as a function of bias on the top Ti line of the sample with height of 300 nm. The inset shows intensity profile of the edge of the line for bias varying from 0 V to – 5 V (as indicated by the arrow).

To model the observed behavior, numerical and analytical calculations of intensity profiles were done for a sample defined as lying in the region $x > 0$ with the edge of interest at $x = 0$. For the numerical model, the electron density distribution $d_2(x)$ was calculated for biases ranging from – 7 V to 7 V in 0.5 V increments. For the analytical model, the redistributed electron density $j(x + S)$ was calculated for biases ranging from – 8 V to 8 V in steps of 0.2 V (using MATLAB codes provided in Appendix E). Results for $d_2(x)$ and $j(x + S)$ are shown in Fig. 7.9(a) and (b), respectively, for – 3 V to 1 V. Notice that for $x > 0$ both $d_2(x)$ and $j(x + S)$ decreased as the bias decreased to – 3 V. $d_2(x)$ is minimized around $V_{bias} = 0.5$ V and $j(x + S)$ is minimized at $V_{bias} = 0.6$ V (where $j(x + S)$ becomes constant and equal to 1). This

behavior is similar to the measured intensity profile. Also, we find that further increase in the bias inverts the calculated electron densities (e.g. black line in Fig.7.9(a) and 7.9(b) for V_{bias} = 1 V) because the local electric field changes direction.

For direct comparison with the measured intensity profiles, the calculated electron densities were scaled such that $A_{expt} = A_{num} = A_{theo}$ for $V_{bias} = -1$ V. In the numerical case, the scaling factor corresponds to the ratio of the actual density of photoelectrons emitted from the surface to the density of electrons assumed in the calculations. In the analytical case, the scaling is equivalent to setting the parameter j_0 to a value other than 1 in Eq. 5. These scaling factors are kept constant in all the voltage contrast results reported here. However we note that the relative contrasts do not change significantly by changing the value of V_{bias} used to scale the data. The measured intensity profile at $V_{bias} = -1$ V is compared with the scaled $d_2(x)$ (blue circles) and $j(x + S)$ (red squares) in Fig. 7.10. Neglecting the peaks outside the sample region, we find that there is good agreement between the scaled calculated electron densities and the measured intensity profile.

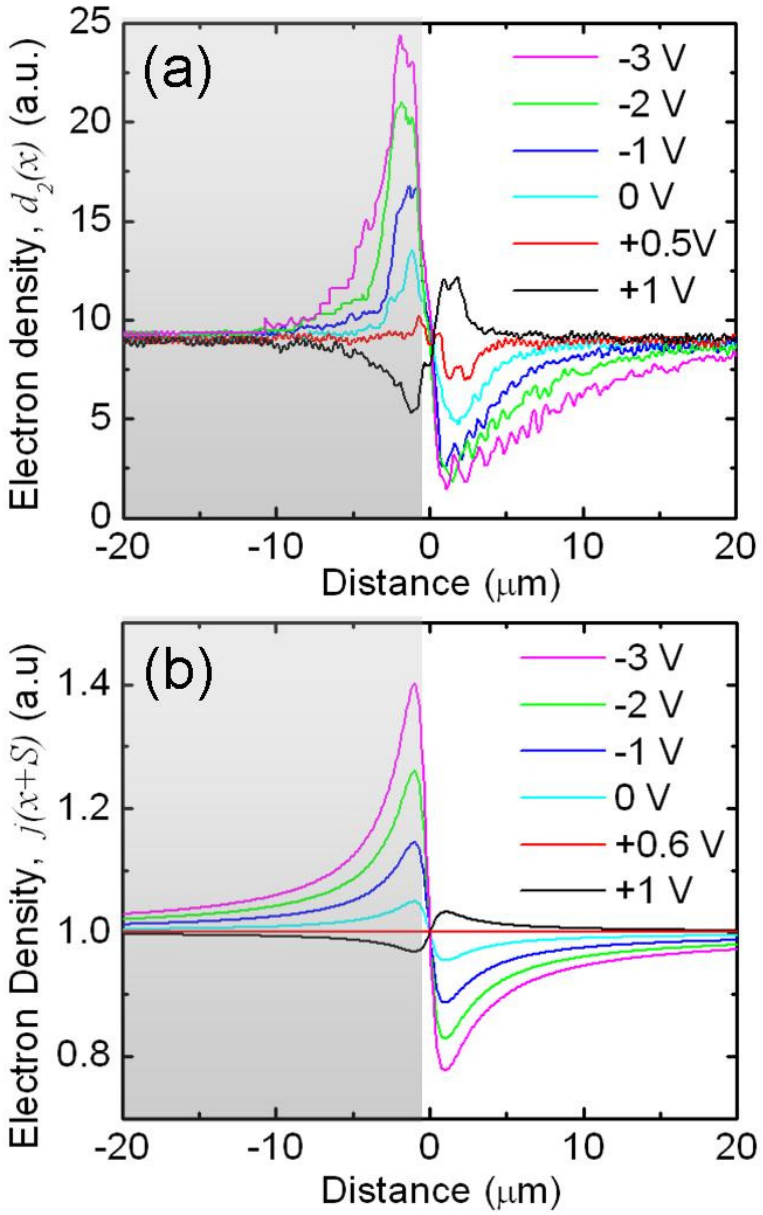


Figure 7.9 a) Electron distribution $d_2(x)$ obtained from the numerical method is plotted against the distance across the line edge for selected value of biases. b) Electron distribution $j(x + S)$ obtained from the analytical approach is plotted against the distance across the line edge for corresponding biases. The sequence of the intensity peak and the dip changes at $V_{bias} = 0.5$ V. Part of curves under the shaded area is not considered for characterization of image contrast.

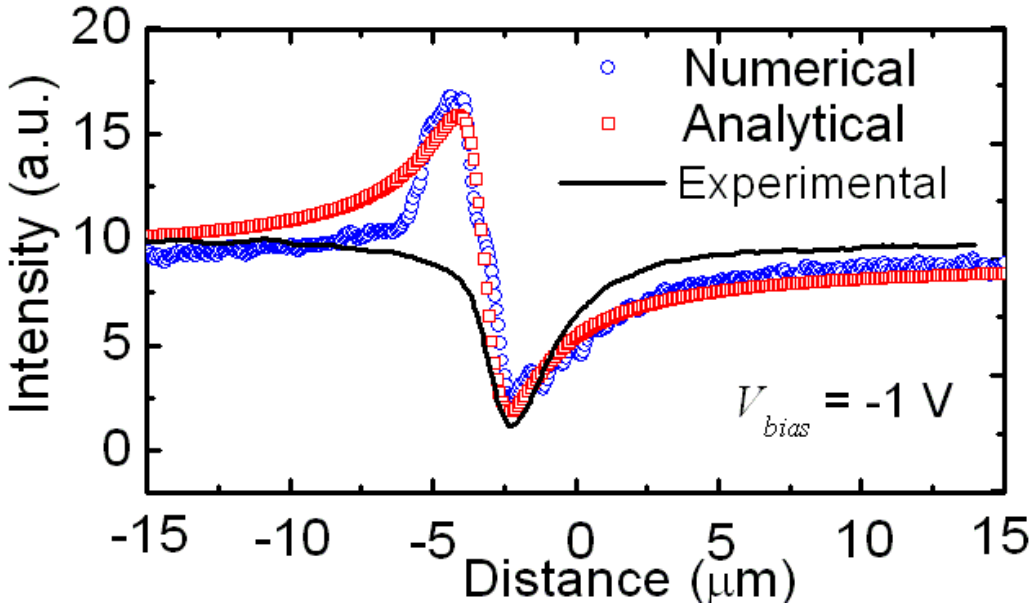


Figure 7.10 Intensity profiles obtained from two analyses (blue and red curves for numerical method and analytical method, respectively) are compared with intensity profile obtained from PEEM image. The peak in intensity (bright line) is absence in case of experimental curve due to the contrast aperture.

The voltage contrast and topography was quantified by extracting the area under the curves for the calculated electron distributions and comparing with the areas extracted from the measured intensity profiles. As shown in Fig. 7.11, there is excellent agreement between the measured and calculated voltage contrast as a function of applied bias [168]. We find that the minimum numerically calculated voltage contrast occurs at V_{bias} = 0.5 V, which is near the minimum voltage contrast measured at V_{bias} = 1 V. The minimum analytically calculated contrast occurs at V_{bias} = 0.6 V and is equal to zero. The minimum voltage contrast should occur when the lateral component of the externally applied field is roughly equal and opposite to the lateral component due to the height of the line. For a line h_0 = 300 nm tall in a uniform electric field, this corresponds to a V_{bias} = 0.6 V

($V_H = |\vec{E}_0| \times h_0 = 10\text{kV} \times 300\text{nm}/5\text{mm}$). Minimizing (or eliminating) the contrast at the edge of the metal line can, in principle, allow for determination of the height of the structure.

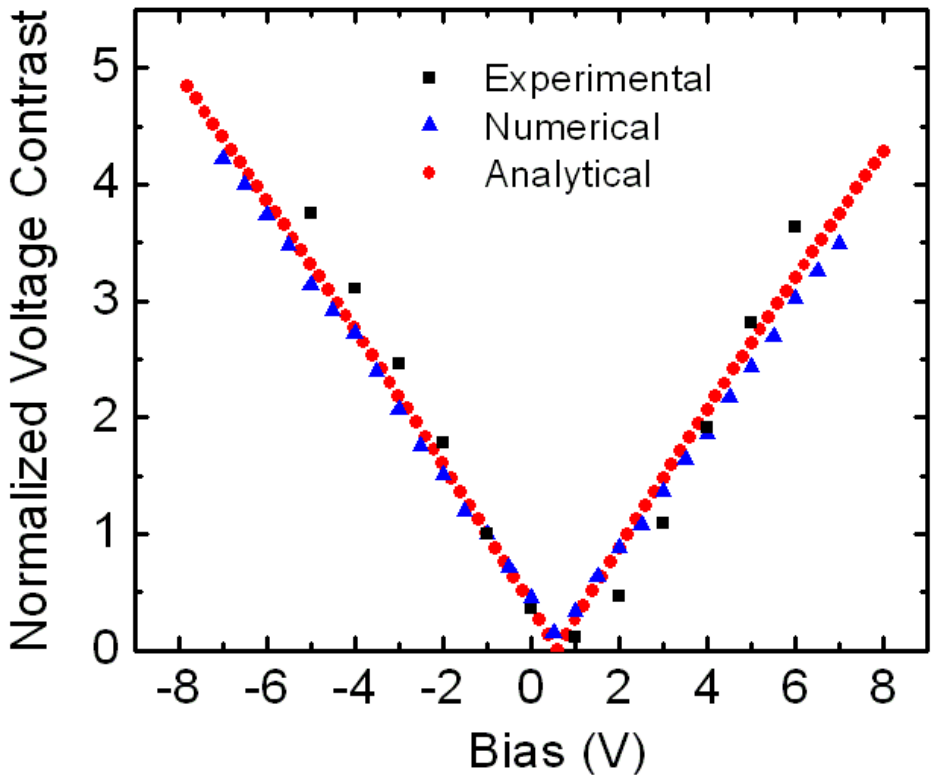


Figure 7.11 The area under the intensity dips from measured and calculated intensity profiles is plotted against the external bias of the sample. Since the three data sets are in arbitrary units they are scaled to be equal to 1 at $V_{\text{bias}} = -1$ V.

To first order, our calculations show that the observed voltage contrast can be explained semi-quantitatively by considering image formation in the PEEM immersion lens. Deviation of the electron distribution due to an applied sample bias is manifested as a change in the virtual image plane. The affected virtual image plane is no longer part of the conjugate plane of the unaffected virtual image plane, and this

results in the observed voltage contrast near the edge of the metal line. Careful analysis of the uncorrected line scans reveals that the average image intensity is also affected by the applied sample bias. When the applied bias increases a few volts (both polarities), the average image intensity increases in a region to the right of the metal line pair. Further increase in the sample bias results in the average intensity decreasing. This suggests that some of the slightly deviated electrons from the virtual object plane do reach the final image, adding to the average intensity. However, they do not arrive at the corresponding focused point because the deviated electrons are not part of the virtual object plane. We note that the aperture in the back focal plane may affect voltage contrast in the same manner in which it limits spherical aberrations. Increasing the diameter of the aperture to allow more electrons through will decrease the amount of contrast in the final image. However, if the virtual plane for the deviated electrons has been sufficiently displaced, Hamiltonian optics predicts that there is no optical path connecting the two planes. We do not have the experimental capability to investigate the effect of moving the back focal plane aperture; this should be explored in future work.

More careful modeling of the external electric field near the edge of the metal line shows that E_x can become significantly larger than the accelerating field. Poisson Superfish [94] software (Appendix C) was used to calculate the electric field near the line edge as the external bias was varied from – 8 V to 8 V in 0.5 V increments. A simulation box of size 12 μm x 12 μm (grid size: 400 x 400) was defined above the sample edge. The upper boundary of the simulation box was set to 24 V ($10\text{kV}\times 12\mu\text{m}/5\text{mm}$) to produce a uniform accelerating field E_0 of 2 V/μm far away

from the edge of the sample. Neumann boundary conditions ($E_x = 0$) were used on the two side walls. Fig. 7.12(a) shows contours of equal E_x in the vicinity of the edge of a sample biased at $V_{bias} = 0$ V. In Fig. 7.12(b), E_x at 30 nm above the metal line ($1.1 \times h_0$, h_0 is height of the sample) is plotted as a function of x for several sample biases. The calculation shows that E_x is much less than 1 V/μm except within 1 μm of the line edge, where it increases significantly. E_x is also observed to be zero everywhere for $V_{bias} = 0.6$ V where minimum contrast was also observed (red curve in Fig. 7.12). Near the step edge, E_x can become as large as 15 V/μm, approximately 7 times larger than E_0 used to image our devices. This means that the applied field can no longer be considered a perturbation to the accelerating field as it is significantly larger. Instead, the electrons traveling in this physical area will be significantly altered from their characteristic curves. Therefore voltage-induced contrast appears only in regions where the externally applied field is sufficient enough to affect PEEM image intensity (i.e. near the edges of the metal lines). This is different than voltage contrast in SEM (or FIB) where the image intensity of the whole structure is affected by the applied bias.

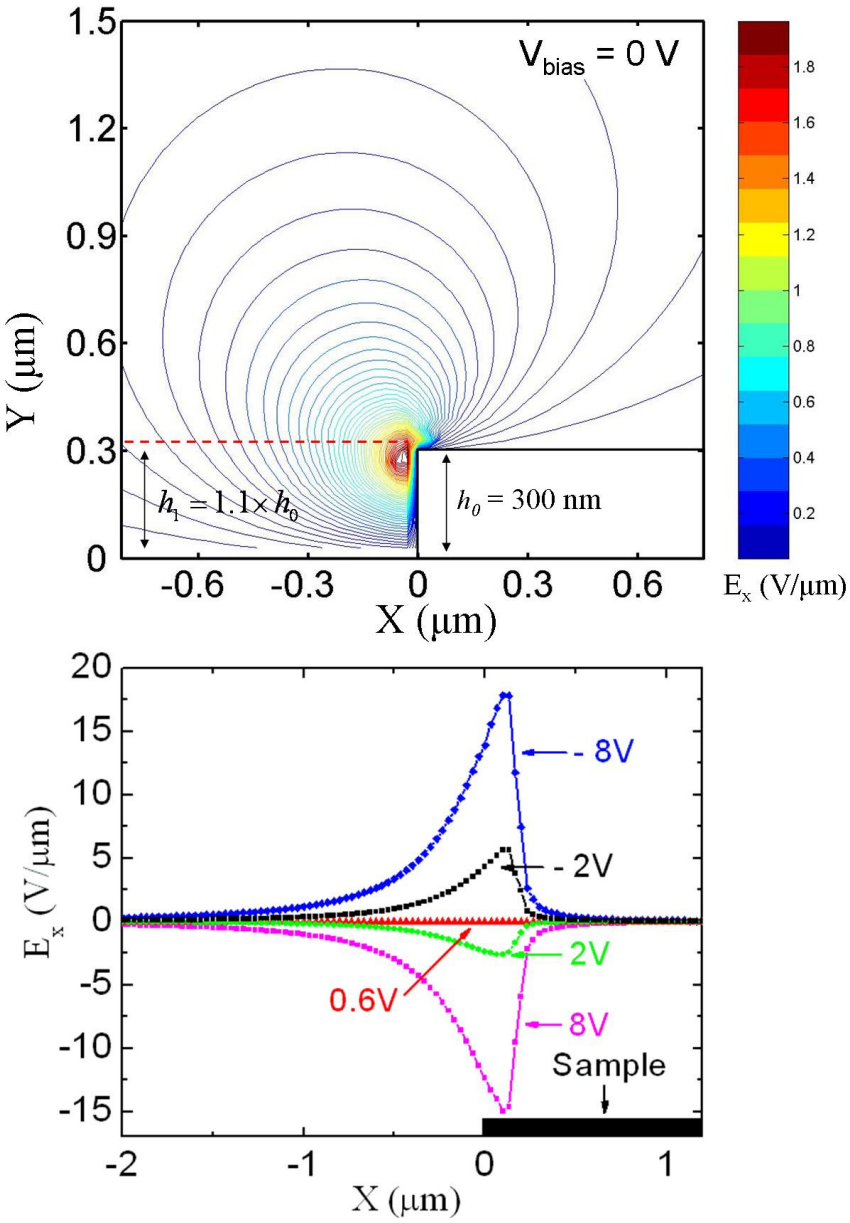


Figure 7.12 a) Lateral component of electric field (E_x) is simulated for a 300 nm-tall metal line (V_{bias} = 0 V) using Poisson Superfish [94]. Color coded lines (see color bar on the right) show contours of equal magnitude of E_x. b) E_x along the dotted line in (a) at a height h_1 = 1.1 x h_0 (330 nm) is plotted as a function of x. Magnitude of E_x is zero for all x when the sample is biased at 0.6 V.

Finally, we will briefly discuss measurements and simulations for the topography contrast in PEEM. Experiments and preliminary simulations on topography contrast were previously reported by Siegrist et al [166]. Metal lines of

three different heights 75 nm, 150 nm and 287 nm were imaged in PEEM. For the numerical model, the electron density distribution $d_2(x)$ was calculated for sample heights varying from 75 nm to 550 nm in 75 nm increments. For the analytical model, the redistributed electron density $j(x + S)$ was calculated for sample heights ranging from 30 nm to 600 nm in steps of 30 nm. Normalized contrast was obtained by the area under intensity curves (intensity dips for numerical and analytical models) such that that $A_{expt} = A_{num} = A_{theo}$ for $h_0 = 300$ nm. Fig. 7.13 shows that there is good agreement between calculated and measured topography contrast. Topography contrast is observed to increase linearly with the sample height such that $A_{expt} = 0.0508\ h_0 - 1.758$, $A_{num} = 0.0376\ h_0 + 2.488$ and $A_{theo} = 0.0417\ h_0 + 0.908$. As we discussed before, the voltage contrast in PEEM can be used to predict the height of a sample. If a sample cannot be biased, the linear dependence of topography contrast on the height of the sample can be alternatively used to obtain the approximate height of the sample.

As we have shown here, PEEM voltage contrast can be generated by applying either a positive or negative bias to a metal line. Observing the change in the edge contrast of metal lines in PEEM will thus allow identification of lines that are continuous with a voltage probe. Conversely, a metal line that is not continuous would not produce changes in image contrast. Therefore, this technique can be used to test IC functionality in the same manner as SEM and FIB tools. In applications where rapid inspection of large areas is desired, the large field of view and high information throughput of PEEM, which is not a scanning technique, may be preferable.

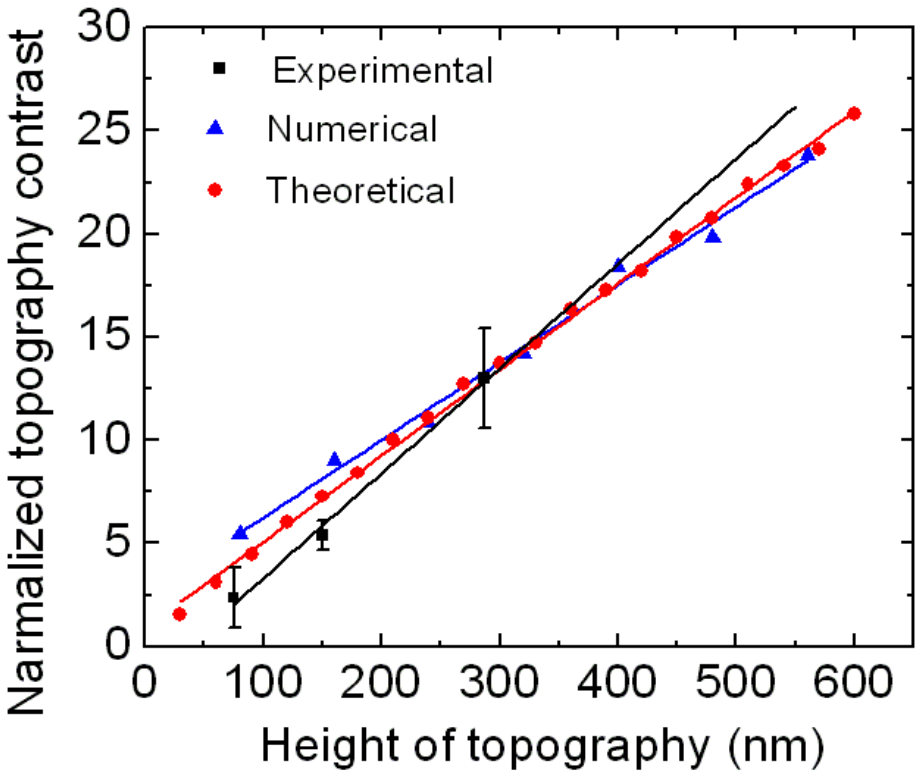


Figure 7.13 The area under the intensity dips for measured and calculated intensity profiles is plotted against the height of the grounded sample. The normalized topography contrast from experiments and numerical model was scaled to be equal to analytical model at sample height h_0 = 300 nm. The experimental data was averaged over results from two samples with the different between them shown by the error bars.

7.9 Conclusions

In conclusion, we have demonstrated that voltage contrast in PEEM can be readily achieved and distinguished from topography contrast. Using simple devices with isolated metal lines, the measured voltage contrast agrees well with the calculated voltage contrast that is based on electrostatic effects to the distribution of imaging electrons. These models show that the electron distribution leaving the accelerating region of the microscope is affected by local electric fields on the specimen. Since the electron distribution can be influenced near the edge of a biased

structure, the corresponding image intensity can be systematically varied. As a result, voltage contrast information can be obtained with PEEM. Thus, it is straightforward to distinguish between an open and a break in a metal line by simply tuning the external bias and observing the edge contrast response. An interesting corollary is that the height of a structure can be measured by determining the bias necessary to minimize the voltage contrast. Topography contrast in itself can also be used to obtain approximate height of a structure. PEEM voltage contrast offers a useful method to probe local potential variations in electronic devices.

Chapter 8 : Characterizing Carbon Nanotube Devices using Photoelectron Emission Microscopy

Electronic transport in a random network of CNTs is dominated by percolative paths. Percolative effects of CNT random networks on the device performance has been studied experimentally [46] as well as analytically [119]. An alternative approach to characterize the field effects in a CNT network is through direct visualization. Field effects in isolated CNTs [169] and CNT arrays [170] have been probed using electrostatic force microscopy (EFM). Field effects in CNT networks have also been studied through the voltage contrast in scanning electron microscopy (SEM) [171, 172]. While EFM is limited by scanning speed, charge implantation in SEM could affect the electronic response of the device. Here, we report a non-destructive real-time *in-situ* imaging tool to probe field effects in CNT thin film transistors. We use the unique voltage contrast mechanism of photoelectron emission microscopy (PEEM) to characterize local field effects in CNT networks.

8.1 Device Fabrication and Experimental Set-up

The PEEM set-up used for near-threshold photoelectron imaging has already been described in Chapter 7. Briefly, a computer controlled 5-axis manipulator was used to position the devices approximately 5 mm from the aperture lens. PEEM images were stored in 1280 x 1024 bitmap in 12-bit .tif format. To fabricate CNT thin film devices, CNTs were grown on 500 nm-thick thermally oxidized Si

substrates via chemical vapor deposition (CVD) using ferric nitrate nanoparticles as the catalyst [132] (Section 3.1). Source and drain electrodes (100 nm Au or Pt on 10 nm Ti) were evaporated using photolithography (Section 2.2).

Strong electric fields near thin electrodes (< 100 μm) can cause arcing in the PEEM chamber. Therefore, 2 mm wide electrodes were used with channel length L varying from 20 μm to 100 μm. The CNT thin film was patterned into the device channel (with channel width W 10 μm to 100 μm) using photolithography and reactive ion etching (O_2 plasma) [85]. Thus, the device channel was kept small (as compared to the width of the electrodes) in order to image the whole device in one exposure (commonly used field of view ~ 80 μm). The samples were mounted on a sample holder and transferred to the PEEM UHV (5×10^{-9} to 10^{-8} Torr) chamber through a load-lock system. The sample was positioned 5 mm away and parallel to the aperture lens plane. Three electrodes in a CNT field effect device can be independently biased by a specially configured sample holder during *in-situ* imaging. Fig. 8.1(a) shows a schematic of a CNT device kept in a PEEM cathode lens.

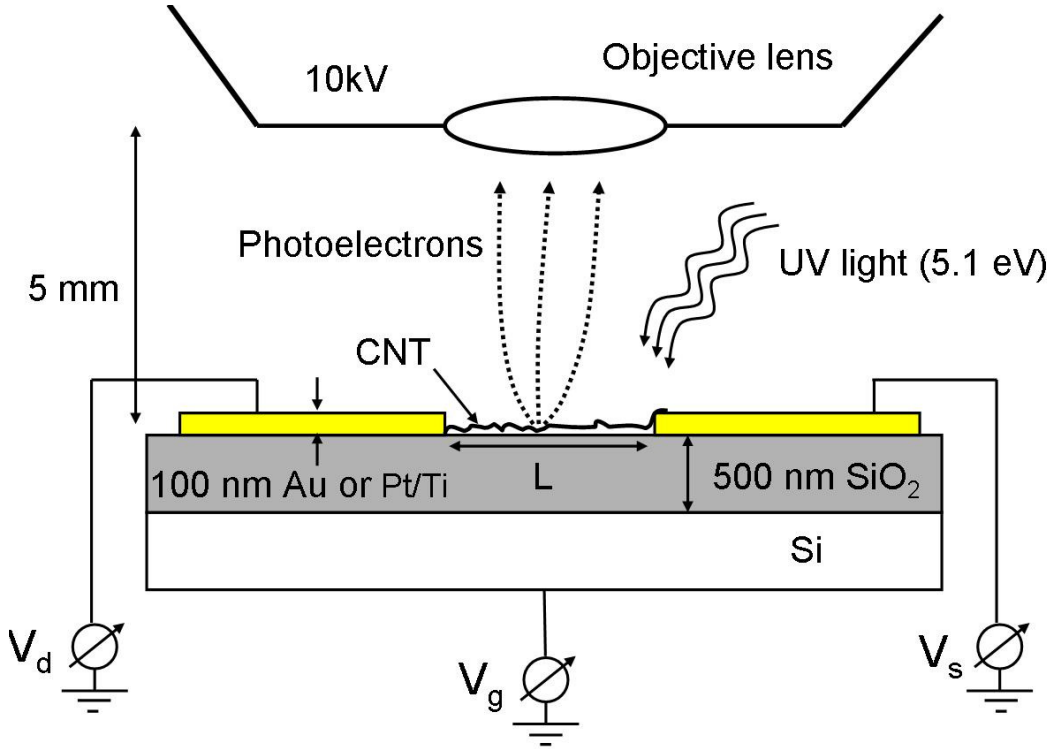


Figure 8.1 Schematic of a CNT device in the PEEM chamber.

8.2 Voltage Contrast in a Single CNT

A control device was imaged to quantify the effect of applied bias (V_{bias}) on the contrast of an individual CNT. The control device consisted of a single CNT connected to only one of the electrodes (drain) in the device. The source and the drain electrodes (100 nm Au on 10 nm Ti) were deposited by photolithography on a sparse network of CNTs. A low density CNT thin film and a large channel length (100 μm) were chosen so that no CNT bridged the source and drain electrodes. A long isolated CNT (~ 50 μm) was selected for imaging. The Si back gate and source electrodes were grounded. This CNT was biased through the drain electrode (V_{bias}) without any current flowing in the device.

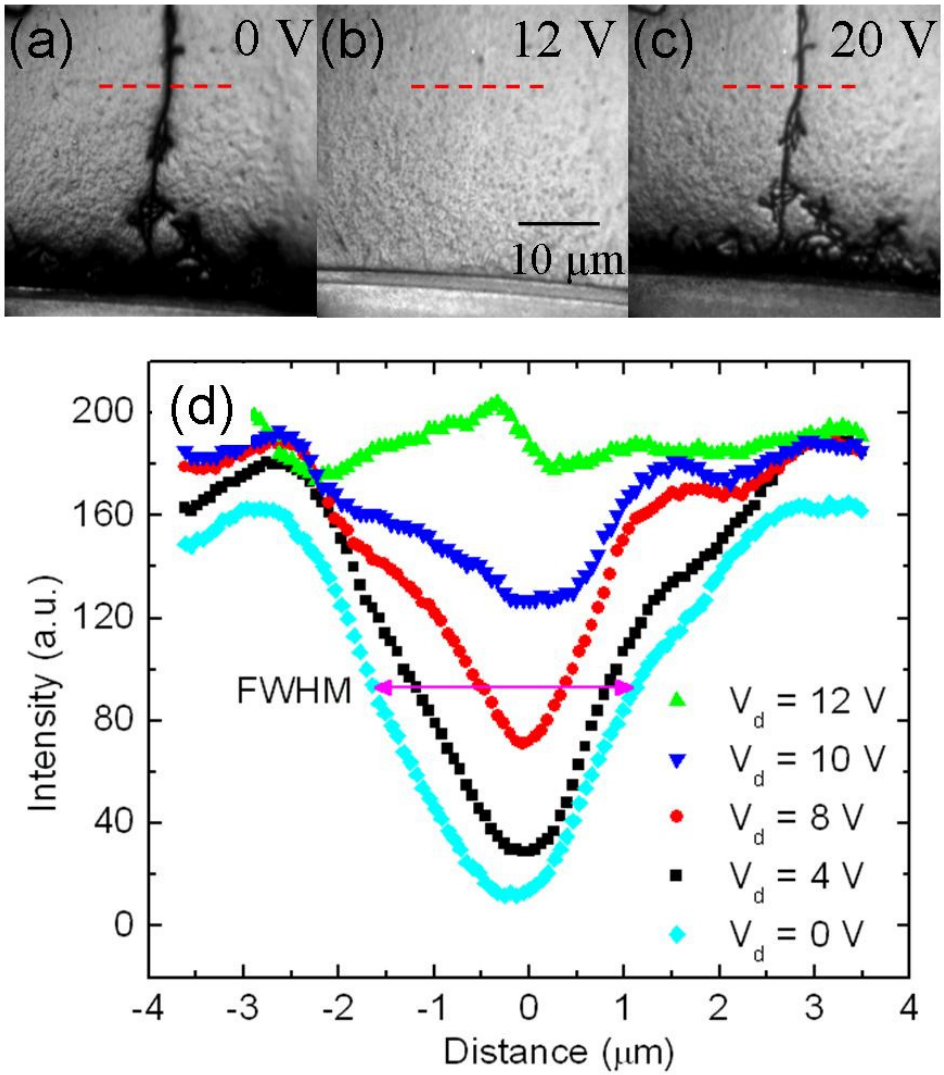


Figure 8.2 a), b), c) PEEM images of a CNT at V_{bias} = 0 V, 12 V and 20 V, respectively. The scale bar in (b) applied to all three images. d) Intensity scans (along red dashed lines shown in (a), (b) and (c)) are plotted for different values of V_{bias}. The full width half minimum (FWHM), as shown by the magenta arrow, is taken as the apparent diameter of the CNT.

The Hg lamp in our system illuminates the sample at a 70^{o} angle with respect to the optical axis of the PEEM in the vertical plane. To avoid any shadowing effects, the device was positioned to obtain a vertically aligned image of the CNT on the screen. The images (8 or 12 bitmap .tiff) were taken with an exposure time of 0.13 sec and averaged over 8 exposures. The CNT was imaged at V_{bias} varying from 20 V

to – 30 V with steps of 2 V. Fig. 8.2(a), (b), (c) show three PEEM images at V_{bias} = 0 V, – 12 V and – 20 V, respectively. At V_{bias} = – 12 V (see Fig. 8.2(b)) the apparent diameter of the CNT is reduced below the resolution limit of the microscope. The image intensity was quantified by averaging the line-scans (using IDL 6.1 codes provided in Appendix D) along 20 parallel lines (within 1 μm) across the CNT (red dashed lines in Fig. 8.2(a), (b) and (c)). The background intensity fluctuations were not subtracted from these line-scans (see Section 7.4 for details). Fig. 8.2(d) shows intensity profiles measured across the CNT image for selected values of V_{bias} in the range 0 V to 12 V. The intensity (pixel depth of the .tiff image files) is in arbitrary units. The apparent diameter of the CNT was characterized by the full with half minimum (FWHM) of intensity profiles. In Fig. 8.3, the apparent diameter (FWHM) of the CNT is plotted as a function of V_{bias}. The contrast varies strongly near the minimum point at V_{bias} = 12 V and tends to saturate at higher biases on both the positive and negative sides. There are two interesting observations in this measurement. First, the apparent diameter of the CNT is of the order of 1 μm, several hundreds of times larger than the true diameter of the CNT. Second, the apparent diameter of a CNT can be controlled by an external bias. The apparent diameter of a CNT in PEEM images can be used as a tool to probe the local potential on the CNT. In this respect, this technique can be used for applications similar to voltage contrast in SEM. In the next section, I will discuss a possible explanation of the contrast mechanism.

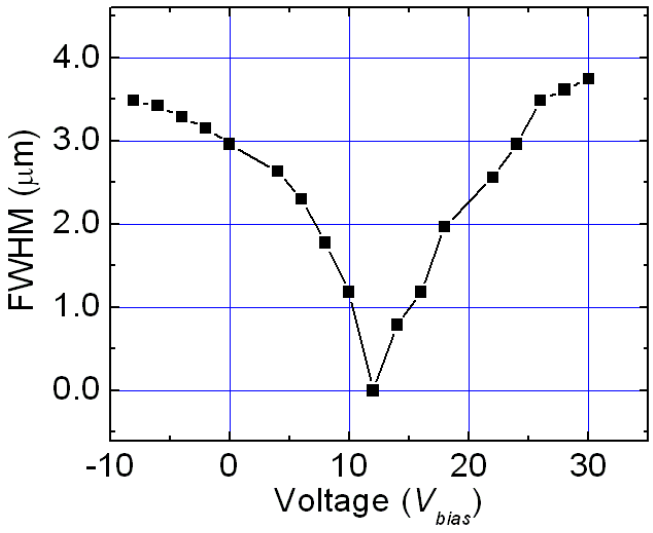


Figure 8.3 Apparent diameter of CNT (FWHM as shown in Fig. 8.2) as a function of V_{bias}.

8.3 Image Formation Mechanism of CNT on SiO_2

The work function of SiO_2 (9.3 eV [173]) is too large for photoemission using 5.1 eV photons. Thus, the large band gap makes SiO_2 effectively transparent to UV light. Internal photoelectron emission occurs at the Si/SiO_2 interface and a distribution of photoelectrons is excited to the conduction band of SiO_2 [173-176]. The band diagram of the Si/SiO_2 interface is shown in Fig. 8.4. The flatband photothreshold of an electron in the Si valence band is 5.27 eV, which is greater than the incident photon energy by 0.1 eV. However, in our devices, the Si substrate is highly doped. It has been shown that the Si band gap and, thus, photothreshold, can be decreased by up to 0.2 eV in heavily doped Si (10^{20} cm^{-3}) [177]. The electrons injected into the oxide conduction band can drift through several microns under the influence of high electric field (10^5-10^6 V/m) without significant trapping [174]. The electric field in the oxide layer of our sample is ~ 5 x 10^5 V/m (i.e. $10\text{kV}/5\text{mm}\times\kappa$,

where the dielectric constant for SiO_2, $\kappa = 3.9$). Crude calculations suggest that the energy gain by a photoelectron in the electric field inside the 500 nm thick oxide layer can be up to ~ 1 eV (assuming electron mobility in SiO_2 ~ 20 cm^2/Vs [178]). If the energy of electrons is greater than the surface barrier at the oxide-vacuum interface (0.9 eV), the electrons can be emitted into vacuum. Photoemission could also result from impurities, defects and surface absorbates (e.g. residual photoresist) in or on the SiO_2 dielectric layer.

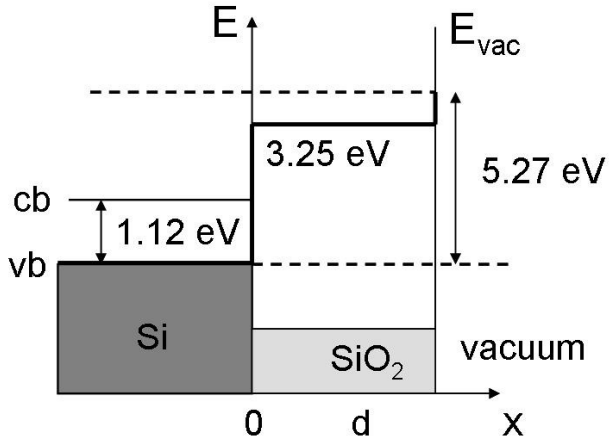


Figure 8.4 Band diagram of the Si/SiO2 interface. The energy required for an electron in the Si valence band to be excited into vacuum is equal to the sum of the Si band gap (~1.12 eV), the conduction-band offset for SiO_2/Si interface (~3.25 eV), and the electron affinity of SiO_2 (~0.9 eV).

The image contrast in PEEM is strongly influenced by the local electric fields near the surface of the device. Perturbation in the local fields, especially the lateral component E_x, can be generated either by the topography [166] or the externally applied bias [168] (Chapter 7). Electrostatic simulations were carried out using Poisson-Superfish [41] (Appendix C) to better understand the role of electric field perturbations in the imaging contrast of CNT devices. First, let's consider the case of

a CNT (diameter = 1 nm) lying on a metallic electrode. Both the electrode and the CNT were grounded and immersed in a uniform electric field (E) of 2 x 10^6 V/m (equal to the electric field in the PEEM cathode lens, $10\text{kV}/5\text{mm}$) by setting appropriate boundary conditions. Simulated equipotential lines in the vicinity of the CNT are shown in Fig. 8.5(a). The potential at the lowest equipotential line is 0.01 and the potential difference between two successive lines is 0.01 V. Note that the electric field far away from CNT can be estimated by comparing the scale bar (1 nm) with the distance between two neighboring lines (0.5 nm) (E ~ 0.01V/0.5nm = 10^6 V/m). Equipotential lines become nearly flat a few nm away from the CNT. Thus, the physical extent of the electric field perturbation is comparable to the dimensions of the CNT within an order of magnitude, in agreement with the discussion on topography contrast in Chapter 7. We attempted to image CNTs printed on Au electrodes in PEEM, but no CNTs were seen on the metal electrodes. This is not surprising because the size of regions with a perturbed electric field in this case is well below the resolution of our PEEM set-up (~ 80 nm).

Now let's consider electric field simulations for a CNT lying on a 500 nm oxide layer. The back gate Si and CNT were grounded. A uniform electric field of 2 x 10^5 V/m was created above the CNT through appropriate boundary conditions. Fig. 8.5(b) shows the simulated equipotential lines. A line with 0.16 V is shown and the potential difference between any two neighboring lines is 0.02 V. Nonuniformity in the electric field extends up to ~ 100 nm in this case.

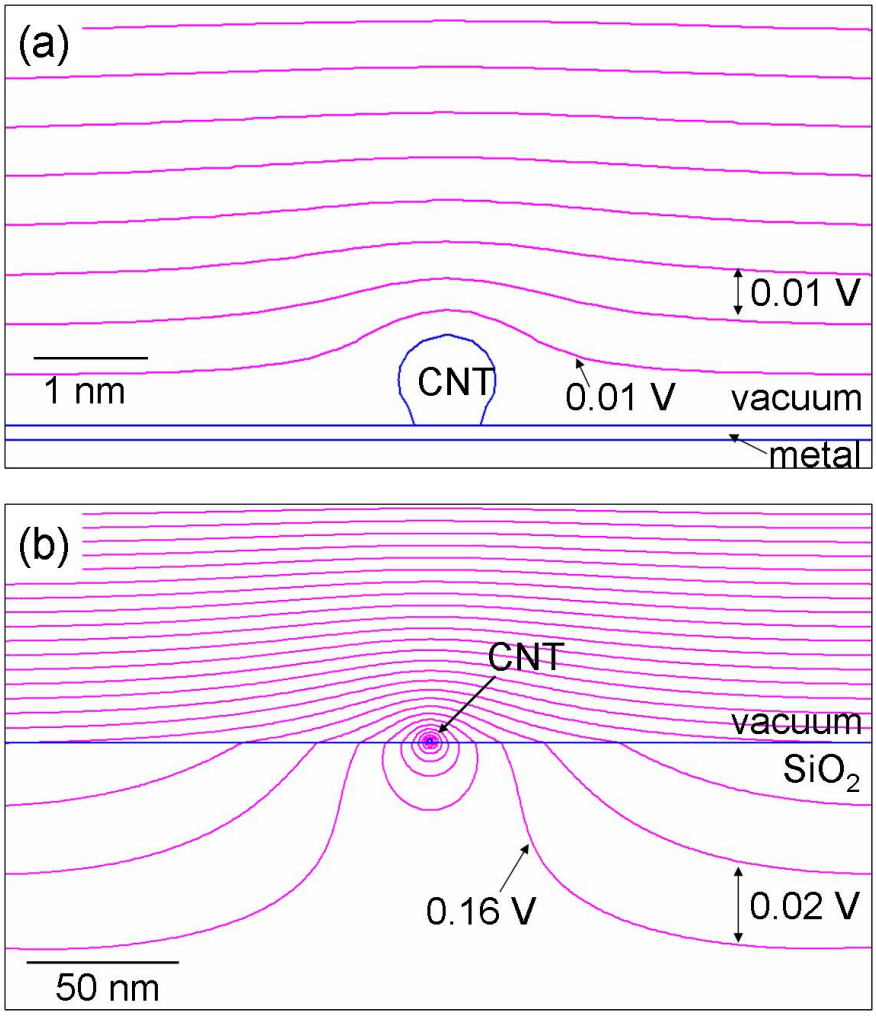


Figure 8.5 Electric field simulations were done using Poisson-Superfish. a) Equipotential lines simulated for a CNT (V_{bias} = 0 V) on a metal surface. The potential difference between neighboring lines is 0.01 V. b) Equipotential lines simulated for a CNT (V_{bias} = 0 V) on a 500 nm thick oxide layer. The potential difference between two neighboring lines is 0.2 V. Note the scale bar in (b) is 50 nm as opposed to 1 nm in (a).

To quantify the field perturbation, we calculated the lateral component of the electric field (E_x) near the CNT. Fig. 8.6(a) shows the variation in the relative strength of E_x (i.e. the ratio $E_x/|E_0|$, where $E_0 = 5 \times 10^5$ V/m is the uniform electric field in the cathode lens far from the device) along a line 1.5 nm (d_{CNT} = 1 nm) above the substrate (see inset in Fig. 8.6(a)). The height 1.5 nm is chosen arbitrarily;

choosing any other height will not change the qualitative aspect of this discussion (Section 7.8). The CNT is situated at $x = 0$, where the sign of E_x is changed. The relative E_x for the CNT on a 500 nm oxide layer can be compared with the CNT on a metal electrode. Fig. 8.6(b) shows a zoomed view of the graph for the CNT on metal. The maximum perturbation in electric field for the CNT on the oxide ($E_x/|E_0| = 3$) is an order of magnitude higher than that for the CNT on the metal ($E_x/|E_0| = 0.3$). The field perturbation also decays more slowly in the case of the CNT on the oxide. For a quantitative comparison, let us define the field perturbation by $|E_x|$ being more than 10% of $|E_0|$ (i.e. $|E_x|/|E_0| > 0.1$, denoted by the region in between the blue dots in Fig. 8.6(a) and (b)). The field perturbation for the CNT on the oxide spans a range (~ 150 μm) over an order of magnitude more than that for the CNT on the metal (~ 6 μm). The large difference in two cases can be explained intuitively, by thinking of a CNT on a 500 nm oxide as a 500 nm-tall topography feature. Thus, photoelectrons emitted from the oxide will experience a stronger perturbation in the electric field than the photoelectrons emitted from the metal electrode. Moreover, the electrons inside the oxide layer will also be influenced by the perturbed electric field. Therefore, the large apparent diameter of CNTs on the SiO_2 surface can be qualitatively explained by the electric field simulations.

The occurrence of minimum contrast at $V_{bias} = 12$ V suggests a minimum perturbation in the local electric field at this voltage. It corresponds to the voltage where effects due to applied bias cancel the effects due to the topography (Chapter 7). However, we cannot at present explain the significance of the specific value of 12 V in this case. Similar experiments done on two other individual CNT and several CNT

thin film (discussed in the next section) devices exhibited minimum contrast at V_{bias} = 3 V to 4 V. Both the analytical approach and simulation of this electrostatic problem gives the solution for the minimum contrast, $V_{bias,\,min}$ = 0.25 V (i.e. $|E_0|/\kappa * d$, where the uniform electric field in the cathode lens $E_0 = 2 \times 10^5$ V/m, the dielectric constant $\kappa = 3.9$ for SiO_2 and the thickness d = 500 nm). The measured value of V_{bias} for minimum contrast varies from sample to sample and is different from the expected value from this simple electrostatic model. Though our electrostatic model provides a reasonable explanation of the large apparent diameter of CNTs in PEEM, a more careful electrostatic model should be used to take into account the charge transfer between the CNT and the oxide layer, defects in the oxide layer, and the current flow between the grounded gate and biased CNT through electrons in the conduction band of SiO_2.

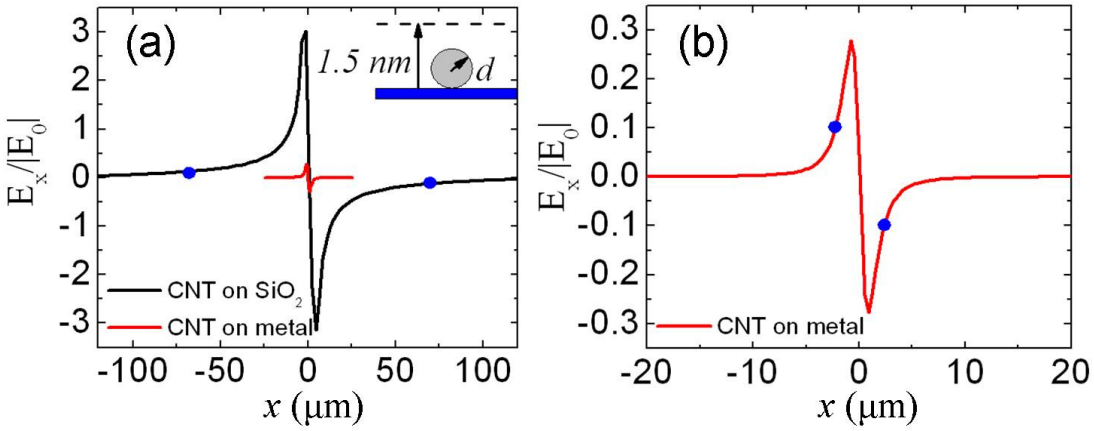


Figure 8.6 a) The ratio $E_x/|E_0|$ is plotted along a line 0.5 nm above a CNT (d = 1 nm, see inset) lying on a 500 nm thick oxide (black curve) and a metal electrode (red curve). E_0 (= 5 x 10^5 V/m) is the uniform electric field far from the CNT. b) The magnified graph for the CNT in the metal electrode shows weaker field perturbations as compared to CNT on the oxide. The blue dots on the curves in both the graphs represent the point at which $|E_x|/|E_0| = 0.1$.

8.4 Probing Local Potential in CNT Devices

We will now consider a working CNT device to illustrate the potential application of image contrast to the local potential in the devices. The device consists of two CNTs bridging the source and drain electrodes across a 50 μm-long channel. One of the CNTs is straight, while the other forms a loop and crosses itself, Fig. 8.7(a). The device was imaged at different drain bias keeping the gate and the source electrodes at ground. The images were averaged over 8 exposures (1.5 sec each) and stored in 1280 x 1024 bitmap of 8-bit tif format. Fig. 8.7(a) shows a PEEM image of the device at V_{bias} = 6 V. Fig. 8.7(b) and (c) show intensity line-scans at three different positions (a, b and c) on the straight CNT and the looped CNT (1, 2 and 3), respectively. The variation in the apparent diameter is larger along the length of the looped CNT as compared to the straight CNT. The apparent diameter of the looped CNT changed from ~ 1 μm to 2.5 μm from the source to the drain electrode, whereas the apparent diameter of the straight CNT remains almost constant. We attribute this to a larger potential drop along the looped CNT. To confirm this, we probed the local potential on the CNT using an electrostatic force microscope (EFM) (Dimension 5000 from Veeco instruments). We used EFM in dc-mode (Dynamic Contact), in which a metal coated AFM tip is kept at ground during scanning. The drain electrode bias was varied and the gate and the source electrodes were grounded. We captured topography and interleaved phase images over a 20 μm x 20 μm area. In Fig. 8.7(d), two interleaved phase images are combined to image most of the CNT. We did not image the CNT near the electrodes to avoid capacitive coupling between the tip and the electrodes. There is significant variation in the apparent diameter of the looped

CNT from one electrode to the other. EFM imaging of the straight CNT (image not shown here) revealed almost no variation in the apparent diameter. From this, we conclude that there is more potential drop across the looped CNT as compared to the straight CNT. The higher resistance of the looped CNT could be due to a combination of any of these three reasons: the different chirality of CNTs, the strain (possibly defects) caused by loop, and different metal-CNT contacts in two cases. However, this simple and qualitative analysis also suggests that the local potential can be probed using the voltage contrast mechanism in PEEM. For practical applications, it would be useful to find a quantitative correlation between the local potential and the apparent diameter in the PEEM images of the CNTs. For that purpose, ac-EFM could provide further insight in the problem.

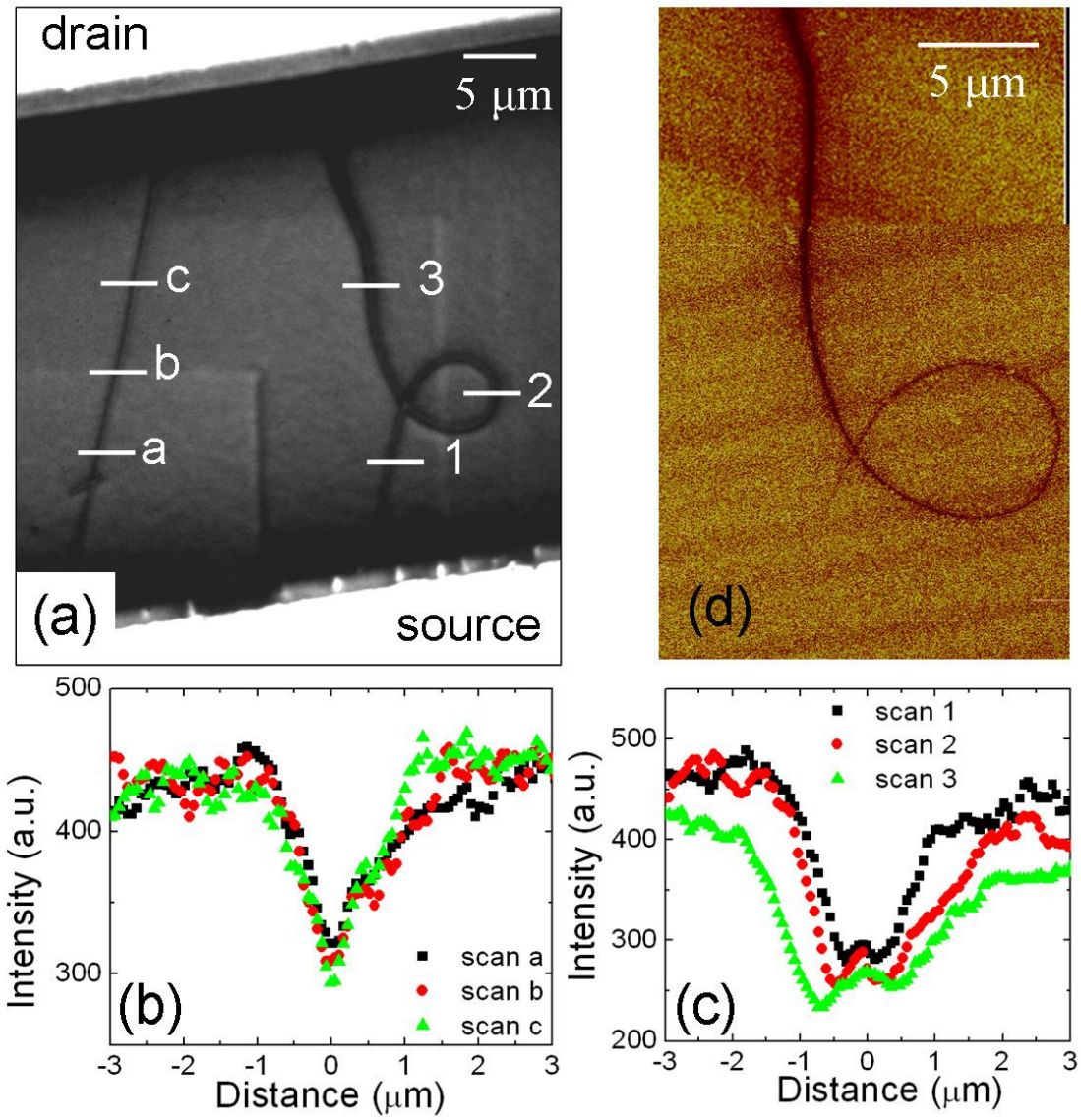


Figure 8.7 a) PEEM image of a CNT FET containing two CNTs. The drain electrode was biased at 6 V whereas source and gate electrodes were grounded. b) Intensity scans at lines a, b and c across the straight CNT. c) Intensity scans at lines 1, 2 and 3 across the looped CNT. d) DC-EFM image (phase) of the looped CNT at V_{bias} = 2 V.

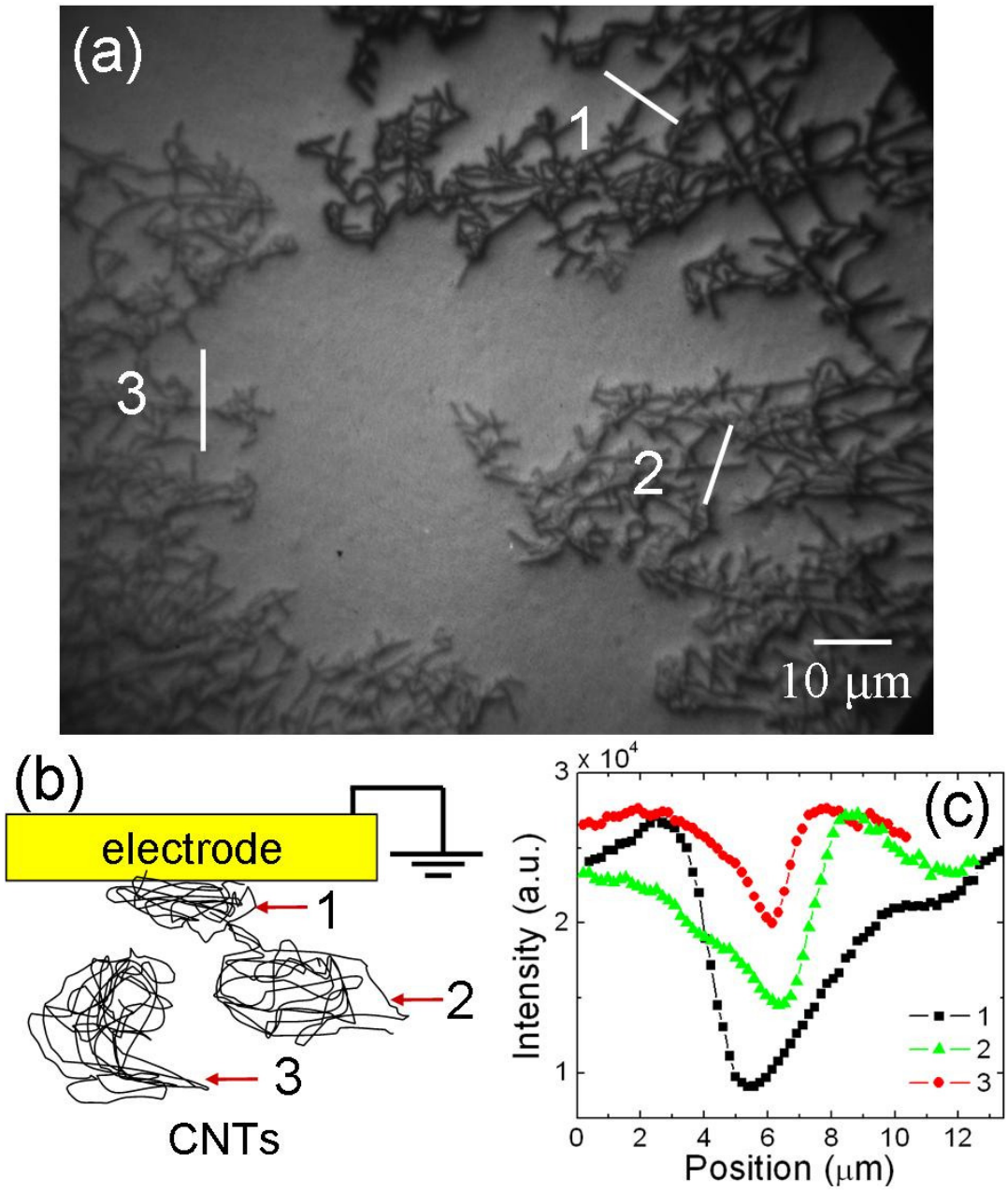


Figure 8.8 a) PEEM image of three different segments of a thin film of well connected CNTs. b) Schematic of the sample illustrating thin film segment 1 is well connected to a grounded electrode, thin film segment 2 is connected to thin film segment 1 through just 2 CNTs and thin film segment 3 is completely isolated. c) Intensity line-scans (along white lines in (a)) taken across three CNTs from each of the three different thin film segments show the apparent diameter of CNTs with different connectivity.

8.5 Imaging Contrast and CNT Network Connectivity

The PEEM voltage contrast approach to probe local potential on a single CNT can be extended to CNT thin films. In a CNT thin film, the conductivity (and thus the local potential) is determined by percolation effects. Before analyzing percolation effects in working CNT thin film devices, I consider CNT thin films in a simpler geometry. Fig. 8.8(a) shows a PEEM image of three different CNT thin film segments on a SiO_2 substrate. CNT thin film segment 1 is well connected to a grounded electrode (Fig. 8.8(b)) and thin film segment 2 is connected to segment 1 through just 2 CNTs. CNT thin film segment 3 is completely isolated. The CNTs in the three different segments show different contrast. Fig. 8.8(c) compares the intensity line-scans across three CNTs from different thin films. The apparent diameter is largest for the grounded network segment (1) and weakest for the isolated network segment (3). The apparent diameter of CNTs in the weakly grounded thin film segment (2) is in between the two extremes. The apparent diameter of the grounded CNTs is approximately equal to the apparent diameter of a grounded single CNT, as discussed in the previous section. The apparent diameter of CNTs in the isolated network is close to a single CNT biased at $V_{bias} \sim 2$ V. This suggests that an isolated CNT on an oxide layer could be at a slightly positive potential compared to a grounded CNT. This could possibly be due to different mechanisms of charge transfer between an isolated CNT and oxide layer than a grounded CNT. This suggestion is supported by the image contrast in weakly grounded CNTs. The different contrast of the thin film segments 1 and 2 can be attributed to a potential difference between the two segments. Moreover, the apparent diameter changes

suddenly at the two CNTs bridging segments film 1 and 2. That means there is some current flowing between segments 1 and 2 and a potential difference is established at the resistive link between the two thin films. The current between thin film segments 1 and 2 can occur if charge is supplied by the oxide layer. It has already been suggested that SiO_2 could conduct through the electrons in the conduction band [178].

8.6 Probing Percolation Effects in CNT Thin Film Devices

We performed *in-situ* imaging of CNT TFTs in PEEM. Let us consider an example to illustrate the mechanism of imaging percolation effects in a CNT network. Figs. 8.9(a) to (f) show PEEM images of a CNT thin film device at the drain bias varying from 0 V to 5 V. The images were averaged over 8 frames (each with 1 sec exposure time). The channel length and width of the device are 50 μm and 30 μm, respectively. The gate and the source electrode (the electrode on the right in images in Fig. 8.9) were grounded. One striking observation is that at V_{bias} = 3 V (Fig. 8.9(d)) the apparent diameter of all the CNTs in the channel is below the PEEM resolution. Moreover, the contrast of CNTs for a given drain bias is not uniform throughout the network. This behavior is not clearly visible to the eyes except for small drain biases. For example, at V_{bias} = 1 V (Fig. 8.9(b)) CNTs near the drain (on left side) are slightly darker than CNTs near the source (on right side). This behavior reverses for V_{bias} = 4 V (Fig. 8.9(e)) where CNTs near the source are darker. Note that contrast of the edges of the electrodes also follows this trend. The contrast variation in the device channel can be attributed to a potential drop in the percolating network of CNTs. In a CNT network, most of the potential drop occurs at resistive

CNT-to-CNT junctions. This technique could be useful in identifying resistive junctions and thus to map out current carrying paths in a CNT thin film device.

Another observation worth mentioning is that the area inside the channel is slightly darker than the SiO_2 surface outside the channel. The CNT thin film was patterned by RIE, so the SiO_2 surface outside the channel was exposed to the O_2 plasma, whereas the SiO_2 surface inside the channel was exposed to processing chemicals. A few atomic layers of the photoresist are likely to have been left on the surface inside the channel. This shows that the imaging contrast in PEEM can be very sensitive to chemical properties of the surface.

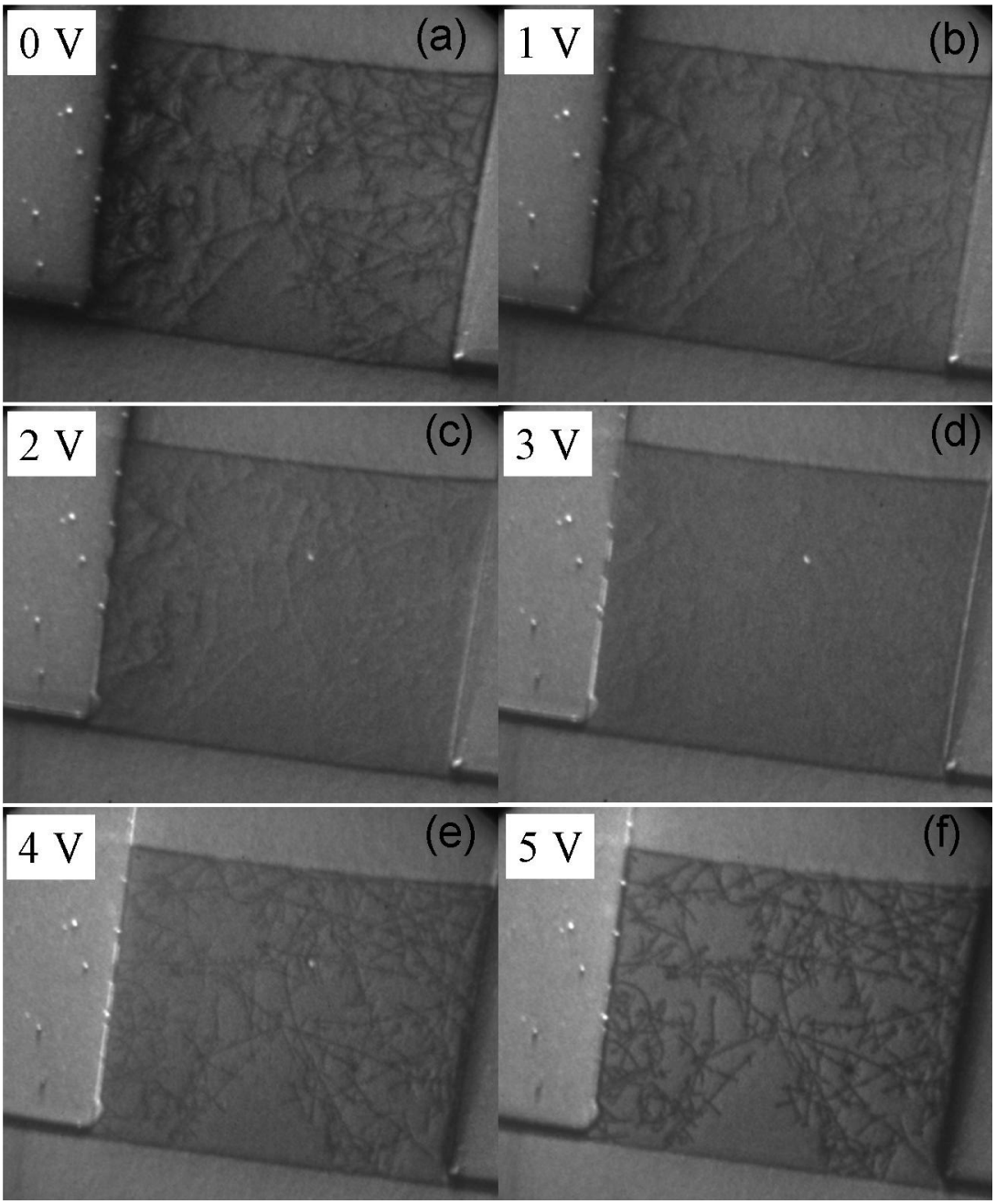


Figure 8.9 PEEM images of a CNT thin film devices under different drain voltages (V_{bias}) (left hand electrode in images). The gate and the source electrodes are grounded whereas the drain bias was varied from 0 V (a) to 5 V (f). The device channel length L = 50 μm.

Conclusions

In this chapter we utilized the voltage contrast mechanism of PEEM to characterize field effects in CNT thin film devices. The apparent diameter of a CNT in a PEEM image is much larger than its true diameter and the apparent diameter can be controlled by the applied bias, indicating the strong effect of local field perturbations in image contrast in PEEM. As we discussed in Chapter 5, the device performance of CNT thin film devices can be optimized through percolation analysis. Percolation effects in a random network were characterized by electrical response. Here we showed that the voltage contrast mechanism in PEEM allows direct visualization of the percolative paths in a conductive CNT thin film. The resolution of PEEM is not as good as some currently available tools such as EFM but PEEM offers some other unique advantages. Whereas the potential of EFM is limited by the scanning speed, PEEM produces real-time imaging at video rate. Thus PEEM is a powerful technique to probe local field effects in CNTs. The technique can be extended to probe field effects in other nano- or microstructures. The true potential of this technique can be realized through real time testing of large arrays of electronics devices in integrated circuits.

Chapter 9 : Summary

In this dissertation, we have reported the development and characterization of CNT thin films as useful electronic materials. For potential applications of a CNT thin film as an electronic material, it is necessary to control the geometry of the devices and integrate them on large area substrates. We showed that a CNT thin film can be utilized as semiconducting as well as electrode materials in a thin film transistor. The density of semiconducting CNT thin films (characterized by a parameter p (section 3.2)) was controlled by using a CVD growth method and the density of CNT thin film electrodes was controlled by airbrushing commercially obtained CNT solutions. It is essential to pattern the CNT thin films to integrate them in large scale. Thus, several different fabrication methods were developed to pattern pristine CNT thin films. A transfer printing method was used to pattern as-grown CNT thin films with a resolution of 5 μm and edge roughness of ~1 μm. The transfer printing technique was also configured by a novel surface treatment method to print Au electrodes, several polymer dielectric layers and CNT thin films onto various plastic substrates.

We studied the effects of percolation in the electrical response of a random network of CNTs. The performance of CNT thin film devices was optimized by controlling the density of the CNTs and the device geometry. For a semiconducting response, it is necessary to obtain a density of CNTs above the percolation threshold, but low enough for the metallic CNTs to be below the percolation threshold. We observed that the percolation threshold of CNTs occurs at a net density parameter p =

0.92 intersections/μm, whereas the percolation threshold of metallic CNTs occurs when the net density reaches p = 3.43 intersections/μm. High quality CNT thin film devices can be fabricated using the density of CNT thin films between these limits. Optimized devices were obtained at p = 2.88 intersections/μm with mobility up to 50 cm^2/Vs and on/off ratio > 10^3. It is worth mentioning that these devices can be compared with high quality devices made by using several parallel arrays of CNT thin film strips [52] (the lateral confinement is used to increase the on/off ratio by restricting metallic paths in the network). In contrast, we achieve comparable device performance by controlling the density of CNTs.

We have demonstrated that a dense thin film of CNTs can also be used as a potential electrode material. Airbrushed CNT thin film electrodes were patterned and printed over large area of polymer and plastic substrates. All-CNT devices were also demonstrated where all the active and conducting device components were made by using CNT thin films. CNT thin film electrodes showed a sheet resistance of 1 kΩ/square at 80 % transparency. The typical mobility (~10 cm^2/Vs) and on/off ratio (~10^3) of all-CNT devices are comparable to that of control CNT thin film devices (fabricated using Au electrodes) [85]. We also demonstrated that CNT thin film electrodes can be successfully incorporated in organic semiconductors. Complimentary circuits were demonstrated by using n-type (C_{60}) and p-type (Pn) thin film transistors. These CNT thin film electrodes are more resistive than commonly used transparent oxide electrodes (such as In_2O_3) but CNT thin film electrodes are much more flexible than In_2O_3. There is lots of room for improving the conductance of CNT thin films and we note that there has been some recent progress reported in

the literature [179]. The fabrication techniques demonstrated here can easily incorporate high quality CNT thin film as electrode in organic electronics.

The effects of the oxide dielectric layer in 1/*f* noise mechanism in CNT field effect transistors were also studied. We developed a versatile transfer printing method to fabricate as-grown single suspended CNT devices. Suspended CNTs were compared with the control devices consisting of a single CNT lying on the dielectric layer. As expected, suspended CNTs showed intrinsic transport properties CNTs through increased ambipolarity and reduced hysteresis. 1/*f* noise of suspended CNTs was found to be 3 to 10 times smaller for the suspended CNTs [132]. The Hooge's constant for suspended CNTs (2.84×10^{-3}) was observed to be approximately an order of magnitude less than that of unsuspended CNTs (5.4×10^{-2}). This suggests that majority of the noise in CNT devices comes from the interaction with the oxide layer. This is in agreement with earlier work reported in the literature [91]. Nevertheless, our pristine suspended CNTs showed up to an order of magnitude less noise than that reported for chemically treated CNTs.

Finally, we discuss a novel technique to visualize the field effects in a CNT thin film devices. We first characterized the voltage contrast in photoelectron emission microscope (PEEM) by doing measurements and numerical simulations of a model system. The numerical simulations of voltage contrast confirmed that the lateral component of the local electric field affects the image formation [168]. For example, CNTs show a much larger than expected apparent diameter (~ 1 μm) in PEEM, which can be explained by the large perturbation in the electric field in the vicinity of the CNT on the oxide layer. Thus, voltage contrast in PEEM can be used

to probe the local potential in a network of CNTs. The conducting paths in a CNT thin film were observed to have a different apparent diameter as compared to isolated CNTs. Electrostatic force microscopy (EFM) is typically used to probe the local potential in nanoelectronics, so the PEEM results were compared with EFM measurements of a isolated CNT. To first order, the EFM results are in good agreement with the PEEM results. Whereas EFM has high resolution, the limitation comes from slow scanning speed. PEEM offers an alternative real-time imaging of large arrays of nanoelectronics devices, and thus shows promise as a powerful tool for rapid characterization of large arrays of few micron-sized devices.

Appendix A : Abbreviations used in the Thesis

CNT – carbon nanotube

SWNT – single-walled nanotube

TFT – thin film transistor

FET – field-effect transistor

CVD – chemical vapor deposition

PEEM – photoelectron emission microscopy

TP – transfer printing

NIL – nanoimprint lithography

RIE – reactive ion etching

RL – release layer

SAM – self-assembled monolayer

DI – de-ionized water

RT – room temperature

IDL – Interactive Data Language

SEM – scanning electron microscope

AFM – atomic force microscope

EFM – electrostatic force microscope

UHV – ultra-high vacuum

FIB – focused ion beam

dc – direct current

ac – accelerating current

L – channel length

W – channel width

V_d – drain voltage

I_d – drain current

V_g – gate voltage

C_g – gate capacitance

μ – field-effect mobility

I_{on}/I_{off} – on-off ratio

T_g – glass transition temperature

S/D – source and drain electrodes

G – gate electrode

PMMA – poly (methyl methacrylate)

PET – polyethylene terephthalate

TCE – 1,1,2 trichloroethylene

IPA – isopropanol

PDMS – polydimethylsiloxane

P3HT – poly (3-Hexylthiophene)

Pn – pentacene

C_{60} – buckminsterfullerene

Appendix B : Effects of Chemical Processing on Electrical Properties of Carbon Nanotube Thin Film Devices

Photolithography is indispensible for most of the patterning techniques discussed in Chapter 3. Some processing resists (e.g. PMMA) cannot be completely etch away by chemical stripping and the remnant thin film can affect the properties of CNTs [83]. To incorporate processed CNT thin film in devices, it is important to understand the effects of chemical processing on electronic properties of CNT thin films. Here, we report some preliminary work to investigate the effects of standard chemical processing on CNTs. Specifically, we chose PMMA as processing chemical because it has been extensively used as the gate dielectric in devices reported in this thesis.

B. 1 Fabrication and Measurements

For the fabrication of pristine CNT thin film transistors (TFTs), CNT thin films were first grown by CVD on 500 nm thick thermally oxidized Si substrate (Chapter 3). Source-drain electrodes (10 nm Ti and 90 nm Pt) were then deposited through a shadow mask (Fig. B.1(a)). CNT thin films were patterned into a device channel (200 μm x 1000 μm) using reactive ion etching (O_2 plasma) through a shadow mask. Thus, CNT thin film devices (total seven devices) were prepared using as-grown CNTs without any chemical treatment. Then, different lithography processing steps were performed on the devices and measurements were conducted at each of the intermediate processing stages, shown in Fig. B.1(b). We conducted

transport as well as 1/*f* noise measurements on the devices. First, measurements of pristine CNT TFTs were performed in air and then samples were transferred to a Desert Cryogenics TT-Prober System to repeat the measurements in vacuum (2 x 10^{-6} Torr). Then, PMMA (A4 MicroChem, Corp.) was spun coat and baked at 150 ^{o}C for 3 min to obtain 400 nm thick films on the samples. The third set of measurements was conducted on CNT TFTs covered with PMMA. PMMA was then stripped in acetone and a fourth set of measurements was taken. Finally, PMMA was completely removed from the substrate by annealing the devices in H_2/Ar at 450 ^{o}C for 60 min [83]. The devices were again measured in vacuum.

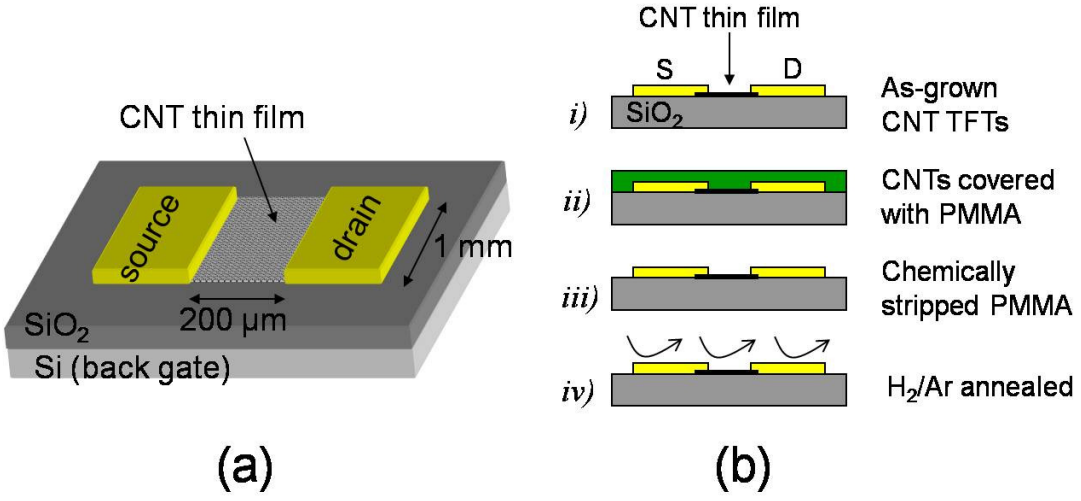


Figure B.1 a) Schematic of CNT TFT on thermally oxidized Si substrate.
b) Four stages in photolithography at which electrical measurements were conducted. All of these measurements were done in vacuum (2 x 10^{-6} Torr).

B.2 Results and Discussions

As-grown pristine CNT thin film devices show p-type behavior (Fig. B.2(a)), possibly due to doping from SiO_2 substrate. Field-effect mobility of pristine CNT

devices in air was observed to be in the range 0.5 – 2 cm^2/Vs and on/off ratio of the order of 10^3. The reason for the low mobility and low conductance of these devices is primarily due to the large channel length of the devices (200 μm). As discussed earlier in this thesis, calculation of field-effect mobility assumes a continuous semiconducting film in the device channel, whereas the actual total coverage of CNTs is about 0.1% of the device channel area. This overestimation of the gate capacitance (c_g) results in an underestimation of the field-effect mobility. Since these devices were fabricated using shadow masks, smaller channel length device could not be fabricated. However, one advantage of the long channel length is that all the devices showed reasonably good on/off ratio (> 10^3). Now, the hysteresis in CNT devices will be briefly discussed.

B.2.1 Hysteresis in CNT devices

Hysteresis in CNT devices has been mentioned at several places in this thesis (Section 4.3, Section 5.4 and Section 5.5.3). Here, we would like to make a few final comments on this in light of the experiments discussed here, as well as other experiments reported earlier in the this work. CNT thin film devices on SiO_2 substrate show significant hysteresis in air (Fig. 5.3, Fig. 5.9 and Fig. B.2) [30, 33, 180]. The hysteresis in CNT devices has been previously attributed to charge traps in SiO_2 as well as water molecules adsorbed on the SiO_2 surface [30, 33]. However, controlled experiment reported in Ref. [33] claimed that charge traps in water molecules adsorbed on CNTs and SiO_2 are the main cause of hysteresis. Both, suspended CNT and CNTs lying on SiO_2 (control devices) showed some hysteresis in

air. Hysteresis was completely removed by placing the suspended CNT FET in vacuum (without heating), whereas control devices still showed some hysteresis in vacuum. It is exactly what we also observed in suspended and control devices, as discussed in Section 4.3. Hysteresis in control devices can also be completely removed by heating the devices at 200 ^{o}C in vacuum (10^{-7} Torr) for ~ 4 hours [33]. This shows that water molecules adsorbed on CNTs are easier to remove than water molecules adsorbed on SiO_2 substrate, as expected from H-bonding between Si-OH bonds and water molecules. The charge trapped in surrounding water molecules could be injected from either CNTs or from trapping/detrapping mechanism in SiO_2. In Ref. [180], it is argued that the charge in surrounding dielectric is injected by CNT itself. Low temperature measurements show that this charging mechanism is not temperature driven [180], which rules out the possibility of trapping/detrapping mechanism in SiO_2 as the source of hysteresis. Hysteresis in CNTs also depends on various experimental parameters, such as time delay between successive measurements and range of gate sweeps [181]. This suggests that the observed hysteresis has a relaxation time comparable to experimental time scale. Fig. B.2(a) shows transfer curves for a CNT thin film device for different rate of gate sweep ($\Delta V_g/\Delta t$). The time delay between two successive gate voltages (ΔV_g = 1 V) was varied from 100 ms to 4 sec. The hysteresis of the device was quantified by the difference between threshold voltage (ΔV_{th}) for forward and reverse gate sweeps. As shown in Fig. B.2(b), the hysteresis is strongly dependent on time delay (Δt). Unless otherwise noted, all the transport measurements in this appendix were taken at gate

sweep rate of 1V/100 ms . The discussion on environmental effect on hysteresis in CNT devices is continued in the next section.

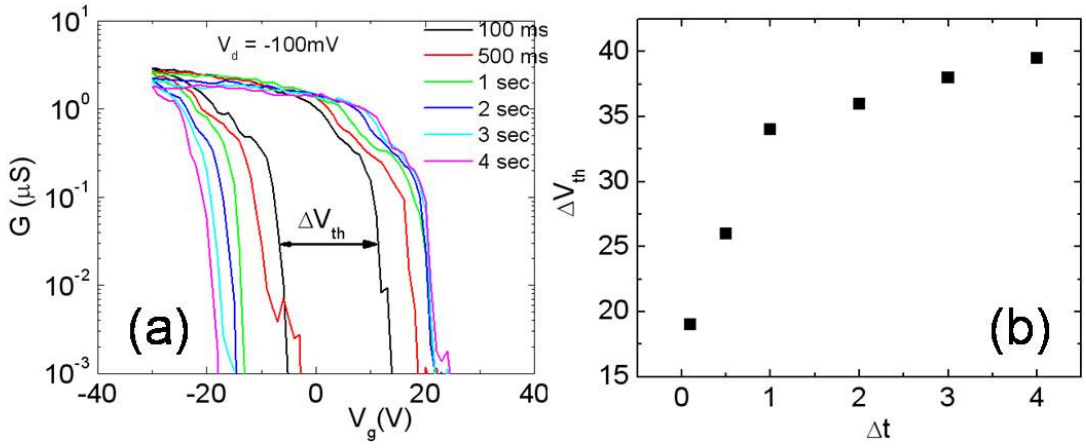


Figure B.2 a) Transfer curve of a CNT thin film device measured in air. Different curves correspond to different time delay between successive measurements. b) Variation of hysteresis (defined as ΔV_{th}, see (a)) as a function of time delay.

B.2.2 Effects of chemical processing on transport properties

Now, we turn to the effect of chemical processing on transport behavior of the CNT thin films. Fig. B.3 shows transfer characteristics of a CNT thin film device at 5 different processing stages mentioned in Section B.1. Pristine CNT thin film devices were first measured in air (blue curve, B.3), then in vacuum (red curve, B.3). There is a 2 to 4-times reduction in transconductance (thus field-effect mobility and on-state conductance) from air to vacuum. This is in agreement in previously reported experiments [106, 108]. Surface adsorbates are expected to enhance transconductance of CNTs by donating the charge to CNTs and by increasing effective c_g of the devices. Adsorbates can be partially removed at 2 x 10^{-6} Torr resulting in decreased transconductance and threshold voltage (in forward as well as

reverse gate sweep). There is also a slight increase in electron conduction in the device in vacuum. This could be attributed to a decreased work function of electrodes in absence of adsorbates [120], in agreement with discussion in Section 4.3. However, this effect is not significant possibly because the transport in a long-channel (L = 200 μm) CNT thin device is dominated by CNT-CNT junctions rather than Schottky barriers at the contacts.

In the third processing stage, the transconductance and field-effect mobility of PMMA-covered CNT thin film devices is increased to that observed for pristine devices in air (green curve in Fig. B.3). PMMA can contribute to current enhancement of CNTs by charge transfer in a manner similar to charge transfer due to surface adsorbates in air. However, there is one interesting distinction. Hysteresis of the devices has been completely removed in presence of PMMA. Quenching of hysteresis by PMMA by passivation of trap charge has also been previously reported in literature [33, 182]. In Ref. [33], passivation is attributed to two possible factors. First, the ester groups of PMMA can H-bond to silane groups and this, combined with baking at 150 ^{o}C could remove water molecule from the vicinity of CNTs. Second, the hydrophobic nature of PMMA can prevent water molecule from permeating through the PMMA layer. This is a possible reason for the observed removal of hysteresis in transfer printed top gate CNT thin film devices, as discussed in Section 5.5. Completely encapsulated CNTs in top gate device have similar geometry to PMMA-covered CNT devices studied here. Partially reduced hysteresis in transfer printed bottom gate could be explained by assuming reduced, but not negligible,

interaction between water molecule and partially exposed CNTs lying on PMMA surface.

After removing PMMA by acetone, the transconductance of the device has again decreased (black curve in Fig. B.3) to the value observed for the pristine device in vacuum (stage 2). However, hysteresis of the device remains quenched. It is interesting to note that both, the increased transconductance and quenched hysteresis are attributed to PMMA, but removal of PMMA affects transconductance but not hysteresis. Thus, an atomically thin layer of PMMA left on SiO_2 surface can successfully passivate CNTs. After complete removal of PMMA by H_2/Ar annealing, hysteresis reappears in the devices (cyan curve in Fig. B.3). The transconductance and the field-effect mobility of the device do not change in this step. However, there is another interesting observation in the annealed CNT device. Off-current (on/off ratio) of the device has decreased (increased) by an order of magnitude. We are currently unable to provide a plausible cause of this observation. However, annealing could be a useful technique to enhance the on/off ratio of the CNT thin film devices.

The results are summarized in Fig. B.4. Field-effect mobility (Fig. B.4(a)), threshold voltage (V_{th}) (Fig. B.4(b)), and on/off ratio (Fig. B.4(c)) of six different devices are shown at five different processing stages. Higher field-effect mobility (and higher conductance) of CNT devices in air and in presence of PMMA is due to a charge transfer. Field-effect mobility and threshold voltage follow same trend for all the devices. On/off ratio remains almost constant during first four processing stages, but increased on/off ratio (due to decreased off-current) after annealing is not well understood.

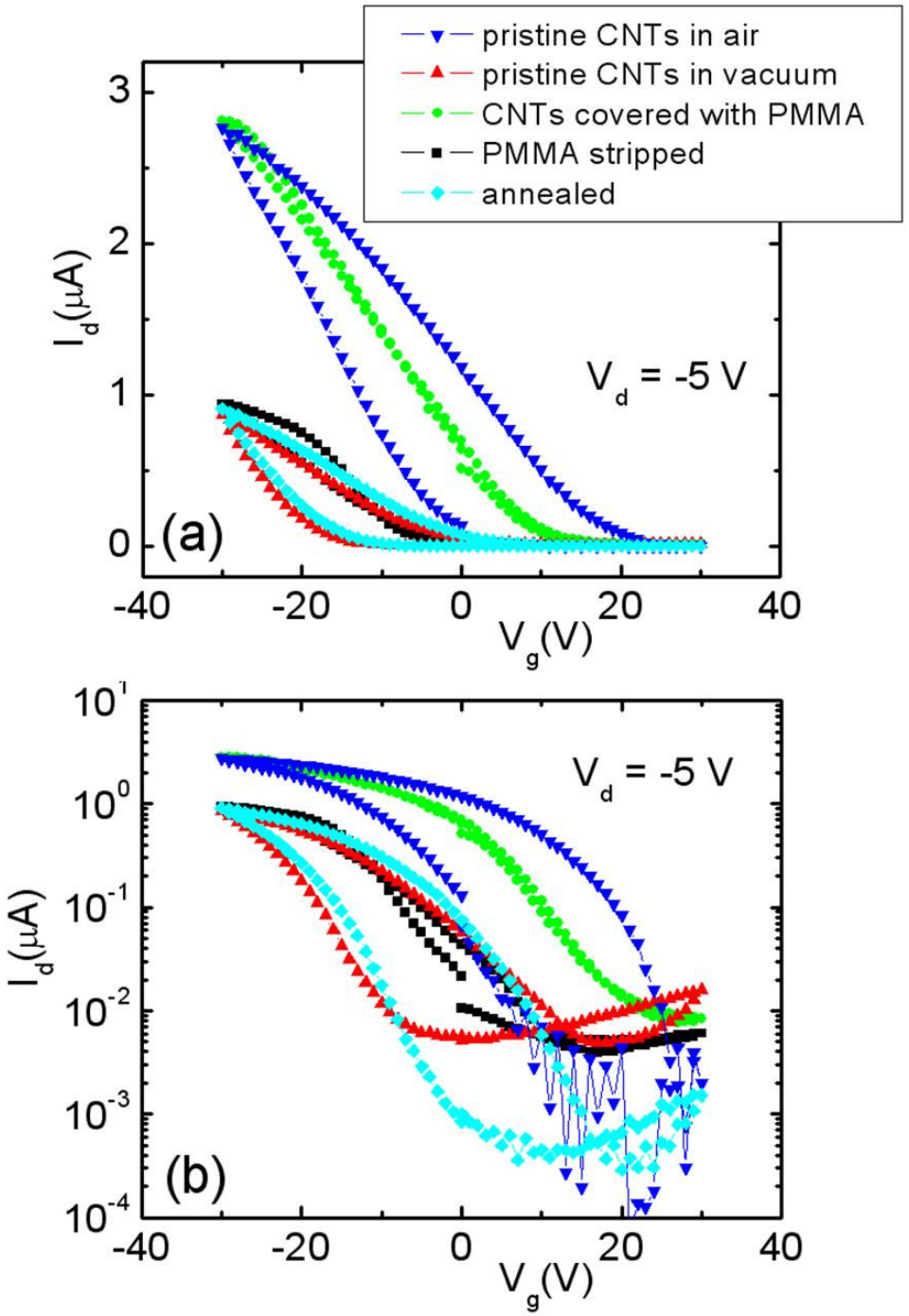


Figure B.3 a) Transfer characteristics of a CNT thin film devices at different stages of chemical processing. b) The same transfer curves are shown in log-linear plot. The legend for both the plots is shown in (a).

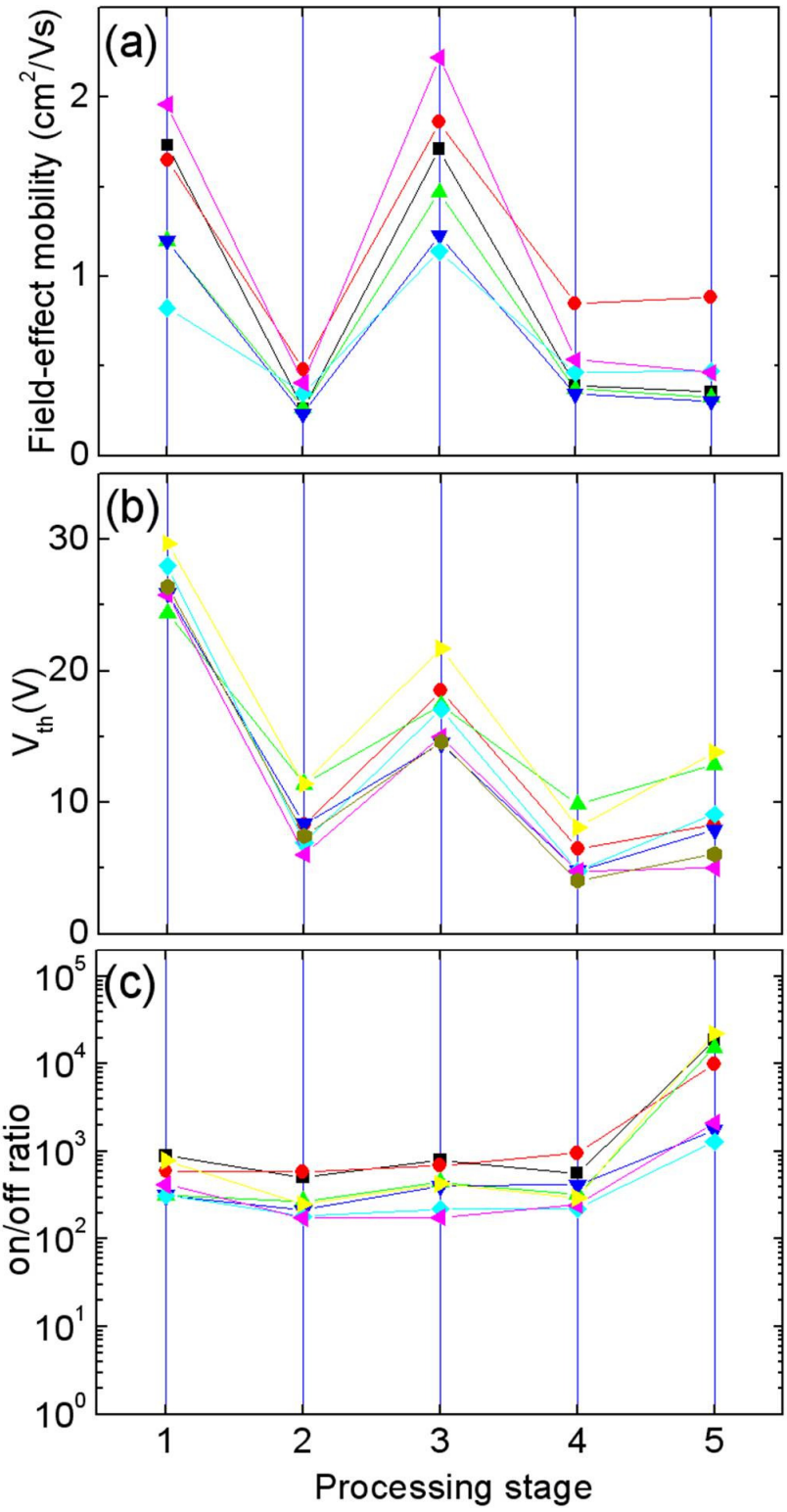


Figure B.4 a) Field-effect mobility b) threshold voltage (V_{th}) and c) on/off ratio of several CNT thin film devices at different processing stages.

B.2.3 Effects of chemical processing on 1/*f* noise

As discussed in Chapter 4, the majority of the 1/*f* noise in CNT devices is due to charge traps present in the dielectric layer. Since the density of charge traps near a CNT also depends on the local chemical environment, 1/*f* noise measurement can be used as a tool to characterize the effects of the chemical processing on CNTs. Here, 1/*f* noise measurements were conducted in vacuum (2 x 10^{-6} Torr) for two CNT thin film devices at all the processing stages except the first stage (pristine devices in air). Measurements were carried out in the same manner as described in Section 4.5. First, the noise spectral density (S_I) was measured as a function of drain voltage to confirm 1/*f* and I^2 behavior as expected, $S_I = \frac{AI^{\beta}}{f^{\alpha}}$. Then, S_I was measured as a function of gate voltage (V_g) at a constant drain bias of 0.5 V. Inverse noise amplitude ($1/A = I^2/fS_I$, at f = 100 Hz) is plotted as a function of V_g in Fig. B.5(a) (scattered data points). The transfer curves (continuous lines) are also plotted for the sake of comparison. CNT thin film devices show decay in the drain current (I_d) with time due to slow charging/discharging of the dielectric layer. It takes approximately 2 minutes to take one noise data point at each V_g. It would be misleading to compare the noise data with transport data taken at delay time of 100 ms (Fig. B.3). Therefore, transport measurements were also conducted simultaneously with the noise data for each value of V_g.

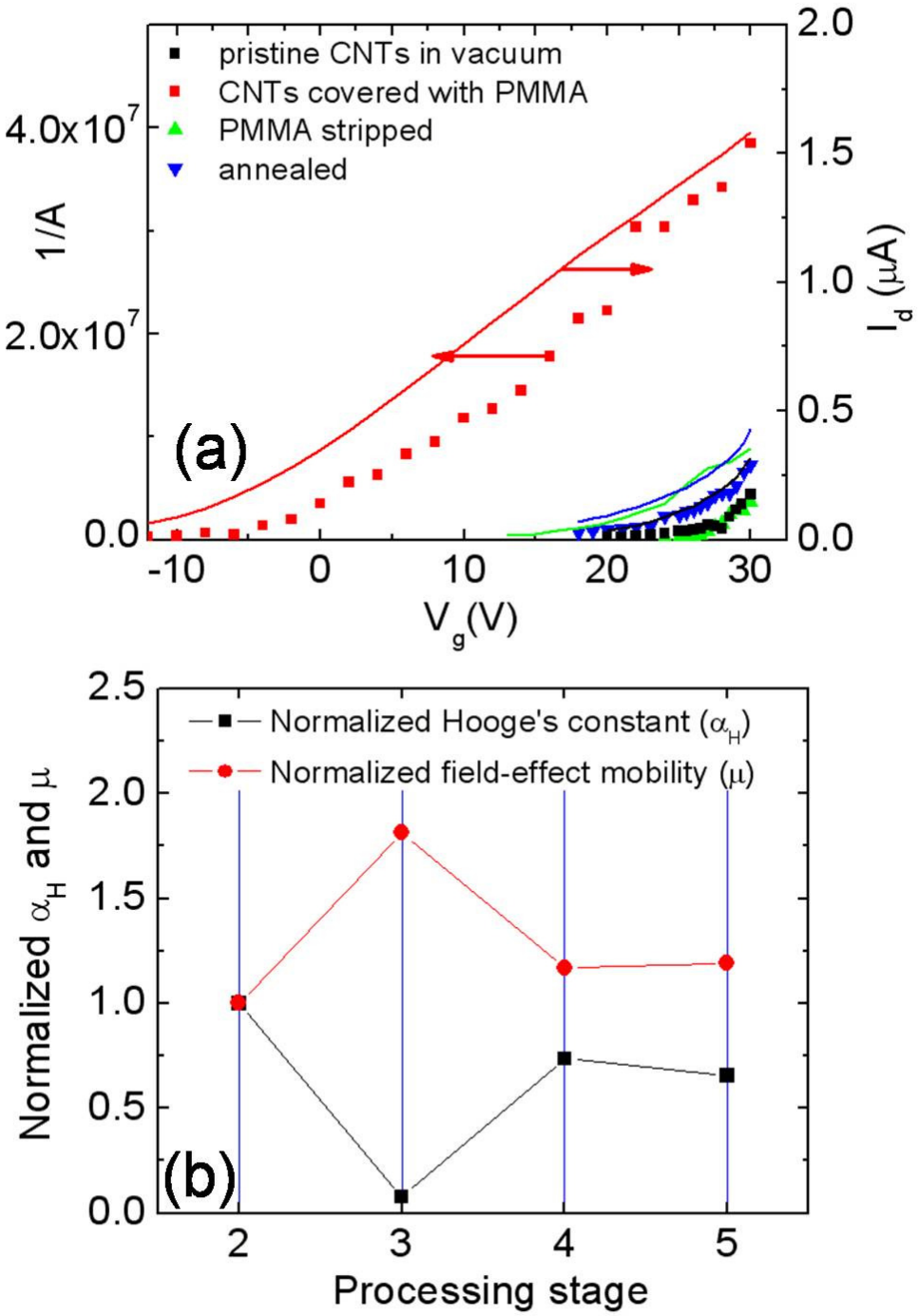


Figure B.5 a) 1/*A* (scattered data) and I_d (continuous lines) of a CNT thin film device is plotted against gate voltage at four different processing stages. 1/*A* and I_d correspond to the left and the right axes, respectively. b) Normalized Hooge's constant and field-effect mobility are plotted at different processing stages.

We used the dependence of $1/A$ on density of carriers (and thus V_g), i.e. $1/A = N/\alpha_H = C_g(V_g - V_{th})/\alpha_H e$ to calculate Hooge's constant (α_H). Hooge's constant is inversely related to the slope of $1/A$ vs V_g; whereas, field-effect mobility (μ) is directly deduced from the slope of transfer curves ($\mu = \frac{L}{V_d C_g}\left|\frac{\partial I_d}{\partial V_g}\right|$). In Fig. B.5(b), normalized α_H and μ of the device are shown at each processing stage, where α_H and μ were normalized to their respective values at the second stage (pristine device in vacuum). Increased μ in PMMA-covered devices has been explained in the previous section. Decreased α_H in the PMMA-covered device is correlated to corresponding increase in μ. However, α_H decreased by 12 times, whereas μ increased only by a factor of 1.8. The exact cause of this behavior is not currently understood. The effect of chemical processing on two quantities is inversely correlated, because gate dependence of $1/A$ and I_d follow the same trend (Fig. B.5(b)). The inverse correlation between α_H and μ has also been previously observed in case of Pn TFTs [183]. In Pn TFTs, the scaling of noise power on field-effect mobility follows the same power law behavior as conductivity on density of a 2-dimensional percolative system. Conduction through a CNT thin film is also dominated by percolation effects. CNT-density dependent noise measurements might be helpful to further understand this behavior.

In conclusion, we studied the effect of chemical processing on transport and $1/f$ noise in CNT thin film devices by using PMMA as processing chemical. We discussed the difference between electrical response of pristine and processed CNT devices. This study is particularly relevant for sensor based applications of CNTs

where processing effects have to be carefully characterized and controlled to obtain desirable response in the final device.

Appendix C : Simulation of Electric Fields using POISSON-SUPERFISH

The software package POISSON-SUPERFISH has been used to simulate electric field at several occasions in the thesis. This software uses finite-element method to simulate electric and magnetic fields. POISSON-SUPERFISH is available for free download at Los Alamos Accelerator Code Group (LAACG) website, http://laacg1.lanl.gov/laacg/services/download_sf.phtml

Here, an example program is provided to help beginners. This code is used to simulate electric field (and equi-potential lines) for suspended CNT geometry in Fig. 4.6. Commands are succinctly explained through comments (followed by "!"). This file has to be saved as *filename.am*. *filename.am* has to be executed by a software unit called AUTOMESH that accompanies P-S package. AUTOMESH defines the geometry and boundary conditions of the problem and automatically creates another file named *filename.T35* in the same folder. Finally, *filename.T35* has to be executed by another software unit called PANDIRA. PANDIRA plots equi-potential lines and arrows representing electric field in *filename.T35* which can be modified through GUI. Output data (electric field and electric potential at each grid point) is then automatically exported to a file named *OUTPAN.TXT*.

----------Program suspendedCNT.am----------

; Copyright 1998, by the University of California.

; Unauthorized commercial use is prohibited.

```
&reg kprob=0,   ! Poisson or Pandira problem
xjfact=0.0,         ! Electrostatic problem
mode=-1,            ! Some material has fixed permittivity
fixeps=3.9,         ! Relative permittivity
dx=0.03,            ! Mesh interval, dy = dx by default. Dy can also be explicitly
                    ! defined.  For a rectangular mesh, also include command “itri=2”
icylin=0,           ! Cartesian coordinates
nbsup=0,            ! Dirichlet boundary condition at upper edge
nbslo=0,            ! Dirichlet boundary condition at lower edge
nbsrt=1,            ! Neumann boundary condition at right edge
nbslf=1             ! Neumann boundary condition at left edge
ltop=45 &           ! Maximum row number of the grid for which output data is
                    ! exported to OUTPAN.TXT.

&po x=0.0,y=0.0 &   ! This defines four corners of the whole geometry.
&po x=0.0,y=3.0 &
&po x=5.0,y=3.0 &
&po x=5.0,y=0.0 &
&po x=0.0,y=0.0 &   ! The first and final points have to be same.
&reg mat=0,voltage=50.0, ibound=-1 &    ! This defines gate voltage as 50 V at
&po x=0.0,y=0.0 &                       ! lower plate defined by two points.
&po x=5.0,y=0.0 &                       ! “mat=0” defines it as a metal.
```

```
&reg mat=3,mtid=3 &    ! This defines geometry of the dielectric layer.
&po x=0.0,y=0.01 &      ! “mat = 3” defines a new material type whose properties,
&po x=0.0,y=0.31 &      ! such as dielectric constant are given at the end of program
&po x=5.0,y=0.31 &
&po x=5.0,y=0.01 &
&po x=0.0,y=0.01 &      ! Again, first and final points have to be same.

&reg mat=0,voltage=0.0,ibound=-1 &  ! This defines the pillars on the left.
&po x=0.0,y=0.31 &
&po x=0.0,y=0.81 &
&po x=2.0,y=0.81 &
&po x=2.0,y=0.31 &
&po x=0.0,y=0.31 &

&reg mat=0,voltage=-1.0,ibound=-1 &  ! This defines the pillars on the right.
&po x=3.0,y=0.31 &
&po x=3.0,y=0.81 &
&po x=5.0,y=0.81 &
&po x=5.0,y=0.31 &
&po x=3.0,y=0.31 &
&mt mtid=3              ! Dielectric constant for mtid = 3 (SiO2 in this case) is defined.
epsilon=4.0  &
```

Appendix D : IDL 6.1 Codes for PEEM Image Processing

As discussed in Section 7.4, PEEM images were stored in 12-bit .tiff format. The intensity profiles were taken using the following program in IDL 6.1. The program *linescan.pro* first prepares the image and other parameters for intensity scans and then, calls another program *myprofile.pro* to get final intensity profile. (*initialx*, *initialy*) and (*finalx*, *finaly* (= *initially*)) are two ends of the first horizontal straight line along which the first scan is taken (Fig. D.1). Final intensity profile is averaged over *num* number of scans taken along vertically stacked *num* number of lines separated by *stepy* pixels (*stepx* = 0). Output data is stored in text file *filename*.

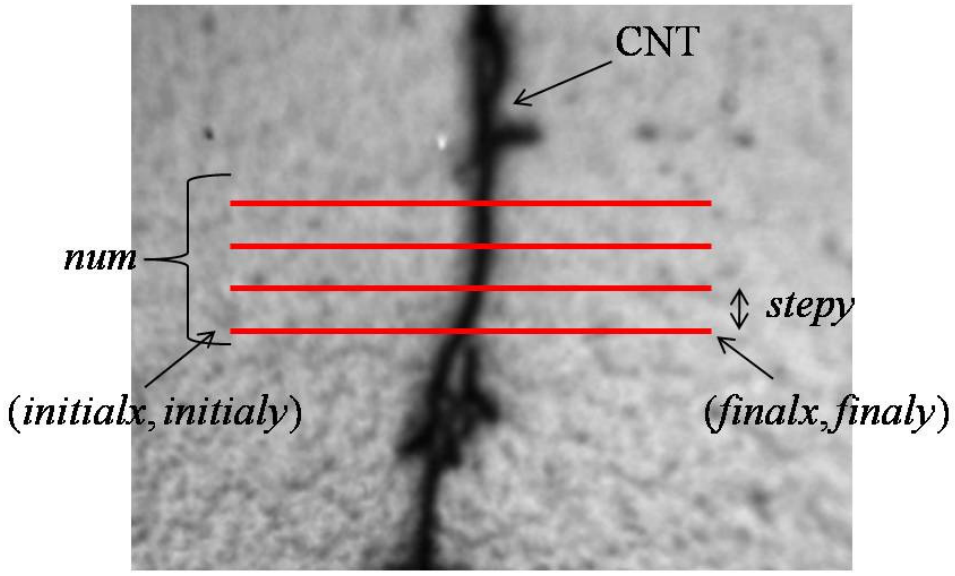


Figure D.1 Schematic of multiple intensity scans taken by program *linescan.pro.*

----------Program linescan.pro----------

```
PRO linescan, image_name, initialx, finalx, initialy, stepx, stepy, num, filename
device, retain=2
```

```
on_error,2          ; Return to caller if an error occurs
finaly = initialy
image1 = read_tiff(image_name)
image = reverse(rotate(image1,3)) ; The image is rotated to make the direction of
; intensity profile is horizontal.  The exact angle is specific to the image.

window, 0, xsize=1024, ysize=1024
tvscl, image
ploty = intarr(finalx-initialx)
averagey = intarr(finalx-initialx)

for i = 0L, num, 1L do begin
    initialx = initialx + stepx
    finalx = finalx + stepx
    initialy = initialy + stepy
    finaly = initialy
    r=myprofile(image, initialx, initialy, finalx, profilex, profiley)
   ploty = profiley + ploty
endfor

averagey = ploty/(num+1)
window, /free
plot, profilex, averagey
```

```
get_lun, u
openw, u, filename, /get_lun
printf, u, averagey, format='(1i6)'
free_lun, u


end
```

---------Program myprofile.pro----------

```
FUNCTION myprofile, image, xx, yy, xx1, profilex, profiley, xstart = x0, ystart = y0,
nomark = nomark
on_error,2
s=size(image)
sx = s[1] & sy=s[2]
if n_elements(x0) le 0 then x0 = 0
if n_elements(y0) le 0 then y0 = 0
Pnt1:
   y = yy - y0
   x = xx - x0
   if !order ne 0 then y = sy - 1 - y
   if (x lt 0) or (x ge sx) or (y lt 0) or (y ge sy) then begin
      message, 'Point outside image', /CONTINUE
      goto, pnt1
```

```
      endif
pnt2:
   wait,.5        ;for fast displays
   yy1 = yy
   y1 = yy1 - y0
   x1 = xx1 - x0
   if !order ne 0 then y1 = sy - 1 - y1 ;Invert?
   if (x1 lt 0) or (x1 ge sx) or (y1 lt 0) or (y1 ge sy) then begin
      message, 'Point outside image.', /CONTINUE
      goto, pnt2
      endif
   if not keyword_set(nomark) then $
      plots,[xx,xx1],[yy,yy1],/dev,/noclip ;Draw the line

dx = float(x1-x)       ;delta x
dy = float(y1-y)
n = abs(dx) > abs(dy)
if n eq 0 then message, 'Zero length line.'
r = fltarr(n+1)

if abs(dx) gt abs(dy) then begin
   if x1 ge x then s=1 else s=-1
   sy = (y1-y)/abs(dx)
```

```
  endif else begin
   if y1 ge y then sy=1 else sy=-1
   s = (x1-x)/abs(dy)
  endelse

outxx = long(findgen(n+1l)*s+x)
outyy = long(findgen(n+1l)*sy+y)
profiley = image[long(outyy)*sx + outxx]
profilex = outxx
return, profilex
return, profiley

end
```

Appendix E : MATLAB Codes for Analysis of Electron Trajectory Data

As discussed in Section 7.6, SIMION was used to simulate electron trajectories from the sample surface ($y = 0$) to $y = 100$ μm. Since, field perturbations are negligible far from the sample edge ($y > 100$ μm), electron trajectories are simulated in this region by assuming a uniform electric field. A single output file of SIMION contains coordinates (x, y) and velocity (V_x, V_y) of electrons at $y = 100$ μm emitted at a fixed angle. For example, the file *H300nmVP1p5Angle80_1.txt* contains the data (x, y, V_x, V_y) for all the electrons emitted at -10^o (represented by '*Angle80'* in the file name) angle w.r.t. surface normal of a 300 nm tall ('*H300nm'*) sample biased at +1.5 V ('*VP1p5*'). The files *H300nmVP1p5Angle80_1.txt* and *H300nmVP1p5Angle80_2.txt* contain the data for the electrons emitted on the left ($x < 0$) and right side ($x > 0$) of topography edge. Electrons in these two regions have to be simulated separately because their initial y coordinate is different due to topography of the sample. First, electrons trajectory data from different files is combined in a single file (*final.txt*) by a program *simionresult.m*. Then, the second program *extend.m* calculates parabolic curves for all the electrons in the region between $y = 100$ μm and $y = 5$ mm. The program *extend.m* takes the data from *final.txt* (x, y, V_x, V_y at $y = 100$ μm for all the electrons) as input and produces x coordinates of electrons at $y = 5$ mm as output in *output.txt*.

The third program, *count.m* calculated the density of number of electrons ($d_0(x)$, $d_1(x)$ and $d_2(x)$, see Section 7.6) by taking raw distribution of electrons in

output.txt as input. $d_0(x)$, $d_1(x)$ and $d_2(x)$ are plotted and final output $d_2(x)$ is written in an array $j(n)$.

The fourth program, *area.m* calculated the area under the dip (A_{num}) of the electron density curve, $d_2(x)$ (Section 7.5.2). The area is calculated between two points where electron density drops to 90% of the maximum density. Note the absence of '*clear*' command in the beginning of the program. That is because some of the variables stored in MATLAB workspace are used as input in this program. Therefore, the following first four programs must be run in the sequence they are reproduced here. The area under experimental intensity profiles (A_{expt}) can be obtained "*trapz*" command in MATLAB.

The fifth program *analytical.m* plots the analytical expression (Equation 7.7) for intensity profile and calculated the area under the curves (A_{theo}).

----------Program 1. simionresult.m----------

```
clear
load -ascii H300nmVP1p5Angle80_1.txt;
 a = H300nmVP1p5Angle80_1;
 load -ascii H300nmVP1p5Angle84_1.txt;
 b = H300nmVP1p5Angle84_1;
 load -ascii H300nmVP1p5Angle88_1.txt;
 c = H300nmVP1p5Angle88_1;
 load -ascii H300nmVP1p5Angle90_1.txt;
 d = H300nmVP1p5Angle90_1;
 load -ascii H300nmVP1p5Angle92_1.txt;
```

```
e = H300nmVP1p5Angle92_1;
load -ascii H300nmVP1p5Angle96_1.txt;
f = H300nmVP1p5Angle96_1;
load -ascii H300nmVP1p5Angle100_1.txt;
g = H300nmVP1p5Angle100_1;
load -ascii H300nmVP1p5Angle80_2.txt;
h = H300nmVP1p5Angle80_2;
load -ascii H300nmVP1p5Angle84_2.txt;
i = H300nmVP1p5Angle84_2;
load -ascii H300nmVP1p5Angle88_2.txt;
j = H300nmVP1p5Angle88_2;
load -ascii H300nmVP1p5Angle90_2.txt;
k = H300nmVP1p5Angle90_2;
load -ascii H300nmVP1p5Angle92_2.txt;
l = H300nmVP1p5Angle92_2;
load -ascii H300nmVP1p5Angle96_2.txt;
m = H300nmVP1p5Angle96_2;
load -ascii H300nmVP1p5Angle100_2.txt;
n = H300nmVP1p5Angle100_2;

global final;
final = [a;b;c;d;e;f;g;h;i;j;k;l;m;n];
```

----------Program 2. extend.m----------

```
EXTEND
clear
double precision
global final;  % final.txt is output file of SIMION
inp1 = final/20000000;  % unit conversion
[rows, columns] = size(inp1);
l = 0.005;
e = 1.6*10^(-19);
m = 9.1*10^(-31);
vol = 10000;
a = (e*vol/(m*l));
ym(1,1) = 0;
xm(1,1) = 0;
i=1;
N=20;

for i = 1:rows
    x0(i) = inp1(i,1);
    y0(i) = inp1(i,2);
    vx0(i) = inp1(i,3);
    vy0(i) = inp1(i,4);
    y(i) = l;
```

```
for j=1:N
    ym(i,j) = y(i)*j/N;
    xm(i,j) = (1/a)*(-vx0(i)*vy0(i) + a*x0(i) + sqrt((vx0(i)*vy0(i))^2 +
2*a*ym(i,j)*vx0(i)^2 + 2*a*y0(i)*vx0(i)^2));
end
    x(i) = (1/a)*(-vx0(i)*vy0(i) + a*x0(i) + sqrt((vx0(i)*vy0(i))^2 + 2*a*y(i)*vx0(i)^2
+ 2*a*y0(i)*vx0(i)^2));
    vx(i) = vx0(i);
    vy(i) = vy0(i) + (a/vx0(i))*(x(i)-x0(i));


end
xm = transpose(xm);
ym = transpose(ym);
 plot(xm,ym,'r-')
global output;
    output_t = [x]; % Use “output_t = [x; y; vx; vy];” if needed
    output = transpose(output_t);
```

----------Program 3. count.m----------

```
COUNT
clear
double precision
global output
    a = (sort(output))*10^6;
k = size(a);
total = a(k)-a(1);
d = a(5)-a(1);
dx = (a(2)-a(1))/3;
m = total/dx;


for n = 1:m
   j(n) = 0;
   x(n) = a(1) + (n-1)*dx;
   y(n) = x(n) + d;
   for i = 1:k
      if x(n) <= a(i) & a(i) < y(n)
         j(n) = j(n)+1;
      end
   end
end
subplot(2,2,1)
```

```
plot(x,j)


for n = 3:m-2
  j(n) = (j(n-2)+j(n-1)+j(n)+j(n+1)+j(n+2))/5; % j(n) is smoothed by averaging 5
end                                            % nearest neighbors
subplot(2,2,2)
plot(x,j)


for n = 3:m-2
  j(n) = (j(n-2)+j(n-1)+j(n)+j(n+1)+j(n+2))/5; % j(n) is again smoothed by averaging
end                                            % 5 nearest neighbors
subplot(2,2,3)
plot(x,j)
```

----------Program 4. area.m----------

```
elim = 50;
avg = 10;
sx = size(x);
sizex = sx(2);
xx = x(elim:sizex-elim);
jj = j(elim:sizex-elim);


jjx = size(jj);
sizejj = jjx(2);
```

```
y1 = mean(jj(1:avg));

y2 = mean(jj(sizejj-avg:sizejj));

x1 = xx(1);

x2 = xx(sizejj);

m = (y2-y1)/(x2-x1);

c = y2 - m*x2;

y = m*xx + c;


jf = jj - y;

[jfmax,xmax] = max(jf);

[jfmin,xmin] = min(jf);

xxmin = min(xmin,xmax);

xxmax = max(xmin,xmax);

[jf1,xx1]=min(abs(jf(xxmin:xxmax)));

xx1 = xx1 + xxmin-1; % Replace it with "xx1 = xx1 + xxmin;" for negative bias data

m1 = (jf(xx1)-jf(xx1+1))/(xx(xx1)-xx(xx1+1));

xx0 = xx(xx1+1) - jf(xx1+1)/m1;

newj = [jf(1:xx1),0]; % Replace it with "newj = [0, jf(xx1:sizejj)];" for negative bias

newx = [xx(1:xx1),xx0]; % Replace it with "newx = [xx0, xx(xx1:sizejj)];" for

                        % negative bias


[peak, xpeak]= max(abs(newj));

sizenewx = size(newx);
```

```
xend = sizenewx(2);
for i = 1:xpeak, % Replace with “for i = 1:xend-xpeak,” for negative bias
   if abs(newj(xpeak-i+1)) < abs(0.1*peak)
% Replace it with “if abs(newj(i + xpeak)) < abs(0.1*peak)” for negative bias
      finalx = newx(xpeak-i:xend); % Replace with “finalx = newx(1:i+xpeak);”
                                   % for negative bias
      finalj = newj(xpeak-i:xend); % Replace with “finalj = newj(1:i+xpeak);”
                                   % for negative bias
      area = trapz(finalx,finalj)
      figure
      plot(finalx,finalj,'o')
      return
   end
end
```

----------Program 5. analytical.m----------

```
clear
double precision
h0 = 300*10^-9;
e0 = 2*10^6;
L = 5*10^-3;
fraction = 0.2;
j0 = 1;
a = 1*10^-6; % a determines steepness of the step
```

```
for k = 1:3
   for i = 1:800
      j = i -400;
      x(i) = j*10^-7;
     % v(k) = 2*(k -1);
      v(k) = (k-0.5);
      J(i) = j0/(1 + (((-e0*h0+v(k))*(a^2+x(i)^2))*(2*x(i)/(a^2 +x(i)^2) -
2*x(i)*(x(i)^2+(a+L)^2)/(a^2 +x(i)^2)^2))/(2*e0*pi*(x(i)^2 + (a+L)^2)));
% This expression was obtained from Mathematica.
% Sign of "v(k)" is changed to change bias sign
   jj(i,k)=J(i);
   end
   plot(x,J)
   hold on

   JJ = abs(J(200:400) - 1);
   sx = size(JJ);
   sizeJJ = sx(2);
   [maxvalue,imax]=max(abs(JJ));
   fracmax = fraction*maxvalue;
   arr2 = abs(JJ(imax:sizeJJ)-fracmax);
   [minvalue, mini]=min(arr2);
   secondpt = mini + imax;
```

```
    finalx = x(1:secondpt);
    finalj = JJ(1:secondpt);
    area(k) = trapz(finalx,finalj);

    XX = x(200:400);
    totalarea(k) = trapz(XX,JJ);
end
```

Bibliography:

1. Edison, T.A. 1892: US Patent 470,925.
2. Oberlin, A., M. Endo, and T. Koyama, *High resolution electron microscope observations of graphitized carbon fibers.* Carbon, 1976. **14**(2): p. 133.
3. Kroto, H.W., et al., *C-60 - Buckminsterfullerene.* Nature, 1985. **318**(6042): p. 162-163.
4. Hamada, N., S.-i. Sawada, and A. Oshiyama, *New one-dimensional conductors: Graphitic microtubules.* Physical Review Letters, 1992. **68**(10): p. 1579.
5. Mintmire, J.W., B.I. Dunlap, and C.T. White, *Are fullerene tubules metallic?* Physical Review Letters, 1992. **68**(5): p. 631.
6. Saito, R., et al., *Electronic structure of graphene tubules based on C60.* Physical Review B, 1992. **46**(3): p. 1804.
7. Iijima, S., *Helical Microtubules Of Graphitic Carbon.* Nature, 1991. **354**(6348): p. 56-58.
8. Dresselhaus, M.S., G. Dresselhaus, and P.C. Eklund, *Science of Fullerenes and Carbon Nanotubes*. 1996, San Diego, CA: Academic Press.
9. Saito, R., G. Dresselhaus, and M.S. Dresselhaus, *Physical Properties of Carbon Nanotubes*. 2003, London, UK: Imperial College Press.
10. Wallace, P.R., *The Band Theory Of Graphite.* Physical Review, 1947. **71**(9): p. 622-634.
11. Olk, C.H. and J.P. Heremans, *Scanning Tunneling Spectroscopy Of Carbon Nanotubes.* Journal Of Materials Research, 1994. **9**(2): p. 259-262.
12. Wildoer, J.W.G., et al., *Electronic structure of atomically resolved carbon nanotubes.* Nature, 1998. **391**(6662): p. 59-62.
13. Demczyk, B.G., et al., *Direct mechanical measurement of the tensile strength and elastic modulus of multiwalled carbon nanotubes.* Materials Science And Engineering A-Structural Materials Properties Microstructure And Processing, 2002. **334**(1-2): p. 173-178.
14. Treacy, M.M.J., T.W. Ebbesen, and J.M. Gibson, *Exceptionally high Young's modulus observed for individual carbon nanotubes.* Nature, 1996. **381**(6584): p. 678-680.
15. Walters, D.A., et al., *Elastic strain of freely suspended single-wall carbon nanotube ropes.* Applied Physics Letters, 1999. **74**(25): p. 3803-3805.
16. Wong, E.W., P.E. Sheehan, and C.M. Lieber, *Nanobeam mechanics: Elasticity, strength, and toughness of nanorods and nanotubes.* Science, 1997. **277**(5334): p. 1971-1975.
17. Yu, M.F., et al., *Tensile loading of ropes of single wall carbon nanotubes and their mechanical properties.* Physical Review Letters, 2000. **84**(24): p. 5552-5555.
18. Yu, M.F., et al., *Strength and breaking mechanism of multiwalled carbon nanotubes under tensile load.* Science, 2000. **287**(5453): p. 637-640.
19. Jaffe, R.L. and B. Jarvis, *Models of carbon nanotube reactivity.* Abstracts Of Papers Of The American Chemical Society, 2001. **221**: p. 243-IEC.

20. Goldsmith, B.R., et al., *Conductance-controlled point functionalization of single-walled carbon nanotubes.* Science, 2007. **315**(5808): p. 77-81.
21. Berber, S., Y.K. Kwon, and D. Tomanek, *Unusually high thermal conductivity of carbon nanotubes.* Physical Review Letters, 2000. **84**(20): p. 4613-4616.
22. Che, J.W., T. Cagin, and W.A. Goddard, *Thermal conductivity of carbon nanotubes.* Nanotechnology, 2000. **11**(2): p. 65-69.
23. Bachtold, A., et al., *Scanned probe microscopy of electronic transport in carbon nanotubes.* Physical Review Letters, 2000. **84**(26): p. 6082-6085.
24. Javey, A., et al., *Ballistic carbon nanotube field-effect transistors.* Nature, 2003. **424**(6949): p. 654-657.
25. Mann, D., et al., *Ballistic transport in metallic nanotubes with reliable Pd ohmic contacts.* Nano Letters, 2003. **3**(11): p. 1541-1544.
26. Yao, Z., C.L. Kane, and C. Dekker, *High-field electrical transport in single-wall carbon nanotubes.* Physical Review Letters, 2000. **84**(13): p. 2941-2944.
27. Chen, Y.F. and M.S. Fuhrer, *Electric-field-dependent charge-carrier velocity in semiconducting carbon nanotubes.* Physical Review Letters, 2005. **95**(23).
28. Appenzeller, J., et al., *Field-modulated carrier transport in carbon nanotube transistors.* Physical Review Letters, 2002. **89**(12).
29. Durkop, T., et al., *Extraordinary mobility in semiconducting carbon nanotubes.* Nano Letters, 2004. **4**(1): p. 35-39.
30. Fuhrer, M.S., et al., *High-mobility nanotube transistor memory.* Nano Letters, 2002. **2**(7): p. 755-759.
31. Martel, R., et al., *Single- and multi-wall carbon nanotube field-effect transistors.* Applied Physics Letters, 1998. **73**(17): p. 2447-2449.
32. Tans, S.J., A.R.M. Verschueren, and C. Dekker, *Room-temperature transistor based on a single carbon nanotube.* Nature, 1998. **393**(6680): p. 49-52.
33. Kim, W., et al., *Hysteresis caused by water molecules in carbon nanotube field-effect transistors.* Nano Letters, 2003. **3**(2): p. 193-198.
34. Chen, Z., et al., Science, 2006. **311**: p. 1735.
35. Brintlinger, T., et al., *Electrodes for carbon nanotube devices by focused electron beam induced deposition of gold.* Journal Of Vacuum Science & Technology B, 2005. **23**(6): p. 3174-3177.
36. Hafner, J.H., et al., *High-yield assembly of individual single-walled carbon nanotube tips for scanning probe microscopies.* Journal Of Physical Chemistry B, 2001. **105**(4): p. 743-746.
37. Ming, X., et al., Nano Letters, 2005. **5**: p. 1515-18.
38. Rao, S.G., et al., *Large-scale assembly of carbon nanotubes.* Nature, 2003. **425**(6953): p. 36-37.
39. LeMieux, M.C., et al., *Self-sorted, aligned nanotube networks for thin-film transistors.* Science, 2008. **321**(5885): p. 101-104.
40. Lee, S.W., et al., *Production of individual suspended single-walled carbon nanotubes using the ac electrophoresis technique.* Applied Physics A, 2004. **78**: p. 283-6.
41. Arnold, M.S., et al., *Sorting carbon nanotubes by electronic structure using density differentiation.* Nature Nanotechnology, 2006. **1**(1): p. 60-65.

42. Collins, P.C., M.S. Arnold, and P. Avouris, *Engineering carbon nanotubes and nanotube circuits using electrical breakdown.* Science, 2001. **292**(5517): p. 706-709.
43. Collins, P.G., et al., *Current saturation and electrical breakdown in multiwalled carbon nanotubes.* Physical Review Letters, 2001. **86**(14): p. 3128-3131.
44. Zhang, G.Y., et al., *Selective etching of metallic carbon nanotubes by gas-phase reaction.* Science, 2006. **314**(5801): p. 974-977.
45. Ding, L., et al., *Selective Growth of Well-Aligned Semiconducting Single-Walled Carbon Nanotubes.* Nano Letters, 2009. **9**(2): p. 800-805.
46. Snow, E.S., et al., *Random networks of carbon nanotubes as an electronic material.* Applied Physics Letters, 2003. **82**(13): p. 2145-2147.
47. Gelinck, G.H., et al., *Flexible active-matrix displays and shift registers based on solution-processed organic transistors.* Nature Materials, 2004. **3**(2): p. 106-110.
48. Kelley, T.W., et al., *Recent Progress in Organic Electronics: Materials, Devices, and Processes.* Chemistry of Materials, 2004. **16**: p. 4413-4422.
49. Forrest, S.R., *The path to ubiquitous and low-cost organic electronic appliances on plastic.* Nature, 2004. **428**(6986): p. 911-918.
50. Bradley, K., J.C.P. Gabriel, and G. Gruner, *Flexible nanotube electronics.* Nano Letters, 2003. **3**(10): p. 1353-1355.
51. Cao, Q., et al., *Highly bendable, transparent thin-film transistors that use carbon-nanotube-based conductors and semiconductors with elastomeric dielectrics.* Advanced Materials, 2006. **18**(3): p. 304-+.
52. Cao, Q., et al., *Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates.* Nature, 2008. **454**(7203): p. 495-U4.
53. Kang, S.J., et al., *Printed multilayer superstructures of aligned single-walled carbon nanotubes for electronic, applications.* Nano Letters, 2007. **7**(11): p. 3343-3348.
54. Kang, S.J., et al., *High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes.* Nature Nanotechnology, 2007. **2**(4): p. 230-236.
55. Kocabas, C., et al., *Guided growth of large-scale, horizontally aligned arrays of single-walled carbon nanotubes and their use in thin-film transistors.* Small, 2005. **1**: p. 1110-1116.
56. Calvert, P., *Inkjet Printing for Materials and Devices.* Chemistry of Materials, 2001. **13**: p. 3299-305.
57. Biebuyck, H.A. and N.B. Larsen, *LITHOGRAPHY BEYOND LIGHT: MICROCONTACT PRINTING WITH MONOLAYER RESISTS.* IBM Journal of Research & Development, 1997. **41**: p. 159.
58. Kumar, A. and G.M. Whitesides, Appl. Phys. Lett., 1993. **63**: p. 2002-4.
59. Xia, Y., et al., Science, 1996. **273**: p. 347-9.
60. Chou, S.Y., P.R. Krauss, and P.J. Renstrom, *Imprint Lithography with 25-Nanometer Resolution.* Science, 1996. **272**: p. 85-87.
61. Hines, D.R., et al., *Transfer printing methods for the fabrication of flexible organic electronics.* Journal Of Applied Physics, 2007. **101**(2).

62. Hines, D.R., et al., *Nanotransfer printing of organic and carbon nanotube thin-film transistors*
on plastic substrates. Applied Physics Letters, 2005. **86**: p. 163101-163103.
63. Gamota, D.R., et al., eds. *Printed Organic and Molecular Electronics*. 2004, Kluwer Academic Publishers: Boston.
64. Thess, A., et al., *Crystalline ropes of metallic carbon nanotubes.* Science, 1996. **273**(5274): p. 483-487.
65. Bronikowski, M.J., et al., *Gas-phase production of carbon single-walled nanotubes from carbon monoxide via the HiPco process: A parametric study.* Journal Of Vacuum Science & Technology A-Vacuum Surfaces And Films, 2001. **19**(4): p. 1800-1805.
66. Cassell, A.M., et al., *Large scale CVD synthesis of single-walled carbon nanotubes.* Journal Of Physical Chemistry B, 1999. **103**(31): p. 6484-6492.
67. Dai, H., Nanotube growth and characterization. Topics in Applied Physics, 2001. **80**: p. 29–53.
68. Dai, H., et al., *Single-wall nanotubes produced by metal-catalyzed disproportionation of carbon monoxide.* Chemical Physics Letters, 1996. **260**(3-4): p. 471.
69. Dai, H.J., et al., *Controlled chemical routes to nanotube architectures, physics, and devices.* Journal Of Physical Chemistry B, 1999. **103**(51): p. 11246-11255.
70. Kong, J., A.M. Cassell, and H.J. Dai, *Chemical vapor deposition of methane for single-walled carbon nanotubes.* Chemical Physics Letters, 1998. **292**(4-6): p. 567-574.
71. Kong, J., et al., *Synthesis of individual single-walled carbon nanotubes on patterned silicon wafers.* Nature, 1998. **395**(6705): p. 878-881.
72. Resasco, D.E., et al., *A scalable process for production of single-walled carbon nanotubes (SWNTs) by catalytic disproportionation of CO on a solid catalyst.* Journal Of Nanoparticle Research, 2002. **4**(1-2): p. 131-136.
73. Zheng, L.X., et al., *Ultralong single-wall carbon nanotubes.* Nature Materials, 2004. **3**(10): p. 673-676.
74. Cao, J., Q. Wang, and H. Dai, *Electron transport in very clean, as-grown suspended carbon nanotubes.* Nature Materials, 2005. **4**(10): p. 745-749.
75. Yuan, D.N., et al., *Horizontally aligned single-walled carbon nanotube on quartz from a large variety of metal catalysts.* Nano Letters, 2008. **8**(8): p. 2576-2579.
76. Edgeworth, J.P., N.R. Wilson, and J.V. Macpherson, *Controlled growth and characterization of two-dimensional single-walled carbon-nanotube networks for electrical applications.* Small, 2007. **3**(5): p. 860-870.
77. Li, Y.M., et al., *Growth of single-walled carbon nanotubes from discrete catalytic nanoparticles of various sizes.* Journal Of Physical Chemistry B, 2001. **105**(46): p. 11424-11431.
78. An, L., et al., *Synthesis of nearly uniform single-walled carbon nanotubes using identical metal-containing molecular nanoclusters as catalysts.* Journal Of The American Chemical Society, 2002. **124**(46): p. 13688-13689.

79. Cheung, C.L., et al., *Diameter-controlled synthesis of carbon nanotubes.* Journal Of Physical Chemistry B, 2002. **106**(10): p. 2429-2433.
80. Choi, H.C., et al., *Delivery of catalytic metal species onto surfaces with dendrimer carriers for the synthesis of carbon nanotubes with narrow diameter distribution.* Journal Of Physical Chemistry B, 2002. **106**(48): p. 12361-12365.
81. Zhang, Y., et al., *Imaging as-grown single-walled carbon nanotubes originated from isolated catalytic nanoparticles.* Applied Physics A-Materials Science & Processing, 2002. **74**(3): p. 325-328.
82. Jeong, G.H., et al., *Effect of nanoparticle density on narrow diameter distribution of carbon nanotubes and particle evolution during chemical vapor deposition growth.* Journal Of Applied Physics, 2005. **98**(12).
83. Ishigami, M., et al., *Atomic structure of graphene on SiO2.* Nano Letters, 2007. **7**(6): p. 1643-1648.
84. Tselev, A., et al., *A photolithographic process for fabrication of devices with isolated single-walled carbon nanotubes.* Nanotechnology, 2004. **15**(11): p. DOI 10.1088/0957-4484/15/11/017|PII S0957-4484(04)79842-6.
85. Sangwan, V.K., et al., *Patterned Carbon Nanotube Thin-Film Transistors with Transfer-Print Assembly.* Mater. Res. Soc. Symp. Proc., 2007. **963**: p. 0963-Q0910-0957.
86. Hsu, J.W.P., *Soft lithography: contacts to organics.* Materials Today, 2005. **July/August**: p. 42-54.
87. Heyderman, L.J., et al., *Flow behaviour of thin polymer films used for hot embossing lithography.* Microelectronic Engineering, 2000. **54**(3-4): p. 229-245.
88. Scheer, H.C. and H. Schulz, *A contribution to the flow behaviour of thin polymer films during hot embossing lithography.* Microelectronic Engineering, 2001. **56**(3-4): p. 311-332.
89. Schift, H., et al., *Pattern formation in hot embossing of thin polymer films.* Nanotechnology, 2001. **12**(2): p. 173-177.
90. Cao, H., et al., *Suspended carbon nanotube quantum wires with two gates.* Small, 2005. **1**(1): p. 138-141.
91. Lin, Y.M., et al., *Impact of oxide substrate on electrical and optical properties of carbon nanotube devices.* Nanotechnology, 2007. **18**(29).
92. Leroy, B.J., et al., *Simultaneous electrical transport and scanning tunneling spectroscopy of carbon nanotubes.* Nano Letters, 2007. **7**(10): p. 2937-2941.
93. Hines, D.R., et al., *Nanotransfer printing of organic and carbon nanotube thin-film transistors on plastic substrates.* Applied Physics Letters, 2005. **86**(16).
94. Brintlinger, T., et al., *Rapid imaging of nanotubes on insulating substrates.* Applied Physics Letters, 2002. **81**(13): p. 2454-2456.
95. Minot, E.D., et al., *Determination of electron orbital magnetic moments in carbon nanotubes.* Nature, 2004. **428**(6982): p. 536-539.
96. Chen, Y.F. and M.S. Fuhrer, *Tuning from thermionic emission to ohmic tunnel contacts via doping in Schottky-barrier nanotube transistors.* Nano Letters, 2006. **6**(9): p. 2158-2162.

97. Radosavljevic, M., et al., *Nonvolatile molecular memory elements based on ambipolar nanotube field effect transistors.* Nano Letters, 2002. **2**(7): p. 761-764.
98. Vigil, R.D. and R.M. Ziff, *Random Sequential Adsorption Of Unoriented Rectangles Onto A Plane.* Journal Of Chemical Physics, 1989. **91**(4): p. 2599-2602.
99. Heinze, S., et al., *Carbon nanotubes as Schottky barrier transistors.* Physical Review Letters, 2002. **89**(10).
100. Hooge, F.N., *1/F Noise Sources.* Ieee Transactions On Electron Devices, 1994. **41**(11): p. 1926-1935.
101. Dutta, P. and P.M. Horn, *Low-Frequency Fluctuations In Solids - 1-F Noise.* Reviews Of Modern Physics, 1981. **53**(3): p. 497-516.
102. Weissman, M.B., *1/F Noise And Other Slow, Nonexponential Kinetics In Condensed Matter.* Reviews Of Modern Physics, 1988. **60**(2): p. 537-571.
103. Hooge, F.N., *1/F Noise Is No Surface Effect.* Physics Letters A, 1969. **A 29**(3): p. 139-&.
104. Collins, P.G., M.S. Fuhrer, and A. Zettl, *1/f noise in carbon nanotubes.* Applied Physics Letters, 2000. **76**(7): p. 894-896.
105. Appenzeller, J., et al., *1/f noise in carbon nanotube devices - On the impact of contacts and device geometry.* Ieee Transactions On Nanotechnology, 2007. **6**(3): p. 368-373.
106. Ishigami, M., et al., *Hooge's constant for carbon nanotube field effect transistors.* Applied Physics Letters, 2006. **88**(20).
107. Lin, Y.M., et al., *Low-frequency current fluctuations in individual semiconducting single-wall carbon nanotubes.* Nano Letters, 2006. **6**(5): p. 930-936.
108. Liu, F., et al., *Noise in carbon nanotube field effect transistor.* Applied Physics Letters, 2006. **89**(6).
109. Snow, E.S., et al., *1/f noise in single-walled carbon nanotube devices.* Applied Physics Letters, 2004. **85**(18): p. 4172-4174.
110. Tobias, D., et al., *Origins of 1/f noise in individual semiconducting carbon nanotube field-effect transistors.* Physical Review B, 2008. **77**(3).
111. Chen, Z.H., et al., *The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors.* Nano Letters, 2005. **5**(7): p. 1497-1502.
112. Vandamme, L.K.J., X.S. Li, and D. Rigaud, *1/F Noise In Mos Devices, Mobility Or Number Fluctuations.* Ieee Transactions On Electron Devices, 1994. **41**(11): p. 1936-1945.
113. Stauffer, D., *Introduction to Percolation Theory*. 1985, Philadelphia: Taylor & Francis Inc.
114. Essam, J.W., *Percolation Theory.* Reports On Progress In Physics, 1980. **43**(7): p. 833-912.
115. Kim, W., et al., *Synthesis of ultralong and high percentage of semiconducting single-walled carbon nanotubes.* Nano Letters, 2002. **2**(7): p. 703-708.
116. Pike, G.E. and C.H. Seager, *Percolation And Conductivity - Computer Study.1.* Physical Review B, 1974. **10**(4): p. 1421-1434.

117. Balberg, I. and N. Binenbaum, *Computer Study Of The Percolation-Threshold In A Two-Dimensional Anisotropic System Of Conducting Sticks.* Physical Review B, 1983. **28**(7): p. 3799-3812.
118. Frank, D.J. and C.J. Lobb, *Highly Efficient Algorithm For Percolative Transport Studies In 2 Dimensions.* Physical Review B, 1988. **37**(1): p. 302-307.
119. Kumar, S., J.Y. Murthy, and M.A. Alam, *Percolating conduction in finite nanotube networks.* Physical Review Letters, 2005. **95**.
120. Martel, R., et al., *Ambipolar electrical transport in semiconducting single-wall carbon nanotubes.* Physical Review Letters, 2001. **87**(25).
121. Fuhrer, M.S., et al., *Crossed nanotube junctions.* Science, 2000. **288**(5465): p. 494-497.
122. Topinka, M.A., et al., *Charge Transport in Interpenetrating Networks of Semiconducting and Metallic Carbon Nanotubes.* Nano Letters, 2009. **9**(5): p. 1866-1871.
123. Hu, L., D.S. Hecht, and G. Gruner, *Percolation in transparent and conducting carbon nanotube networks.* Nano Letters, 2004. **4**(12): p. 2513-2517.
124. Zhang, D.H., et al., *Transparent, conductive, and flexible carbon nanotube films and their application in organic light-emitting diodes.* Nano Letters, 2006. **6**(9): p. 1880-1886.
125. Cao, Q., et al., *Transparent flexible organic thin-film transistors that use printed single-walled carbon nanotube electrodes.* Applied Physics Letters, 2006. **88**(11).
126. Southard, A., et al., *Solution-processed Single-Walled Carbon Nanotube Electrodes for Organic Thin-Film Transistors.* Organic Electronics (submitted), 2009.
127. Kim, H., et al., *Improvement of the contact resistance between ITO and pentacene using various metal-oxide interlayers.* Organic Electronics, 2008. **9**(6): p. 1140-1145.
128. Kim, S., et al., *Fully Transparent Thin-Film Transistors Based on Aligned Carbon Nanotube Arrays and Indium Tin Oxide Electrodes.* Advanced Materials, 2009. **21**(5): p. 564-+.
129. Takenobu, T., et al., *High-performance transparent flexible transistors using carbon nanotube films.* Applied Physics Letters, 2006. **88**(3).
130. Artukovic, E., et al., *Transparent and flexible carbon nanotube transistors.* Nano Letters, 2005. **5**(4): p. 757-760.
131. Hur, S.H., et al., *Nanotransfer printing by use of noncovalent surface forces: Applications to thin-film transistors that use single-walled carbon nanotube networks and semiconducting polymers.* Applied Physics Letters, 2004. **85**(23): p. 5730-5732.
132. Sangwan, V.K., et al., *Facile fabrication of suspended as-grown carbon nanotube devices.* Applied Physics Letters, 2008. **93**(11).
133. Ha, Y.G., et al., *Fabrication and characterization of OLEDs using MEH-PPV and SWCNT nanocomposites.* Synthetic Metals, 2005. **153**(1-3): p. 205-208.

134. Subramanian, V., et al., *Printed organic transistors for ultra-low-cost RFID applications.* Ieee Transactions On Components And Packaging Technologies, 2005. **28**(4): p. 742-747.
135. Klauk, H., D.J. Gundlach, and T.N. Jackson, *Fast organic thin-film transistor circuits.* Ieee Electron Device Letters, 1999. **20**(6): p. 289-291.
136. Crone, B., et al., *Large-scale complementary integrated circuits based on organic transistors.* Nature, 2000. **403**(6769): p. 521-523.
137. Crone, B.K., et al., *Design and fabrication of organic complementary circuits.* Journal Of Applied Physics, 2001. **89**(9): p. 5125-5132.
138. Dodabalapur, A., et al., *Hybrid organic inorganic complementary circuits.* Applied Physics Letters, 1996. **68**(16): p. 2246-2248.
139. Zhang, X.H., et al., *Low-voltage flexible organic complementary inverters with high noise margin and high dc gain.* Applied Physics Letters, 2009. **94**(4).
140. Zhang, Y.Y., et al., *Poly(3,3 '"-didodecylquarterthiophene) field effect transistors with single-walled carbon nanotube based source and drain electrodes.* Applied Physics Letters, 2007. **91**(22).
141. Cui, X.D., et al., *Controlling energy-level alignments at carbon nanotube/Au contacts.* Nano Letters, 2003. **3**: p. 783-787.
142. Ghanem, T.K., M.S. Fuhrer, and E.D. Williams, *Electronic Transport in Low Dimensions: Carbon Nanotubes and Mesoscopic Silver Wires.* Ph.D. Dissertation, University of Maryland College Park, 2008.
143. Southard, A., *Solution processed carbon nanotube thin films*, in *Department of Physics*. 2009, University of Maryland College Park: College Park.
144. Lim, S.C., et al., *Surface-treatment effects on organic thin-film transistors.* Synthetic Metals, 2005. **148**(1): p. 75-79.
145. Newbury, D.E., et al., *Advanced Scanning Electron Microscopy and X-Ray Microanalysis*. 1987: Plenum, New York.
146. Seiler, H., *Secondary-Electron Emission In The Scanning Electron-Microscope.* Journal Of Applied Physics, 1983. **54**(11): p. R1-R18.
147. Campbell, A.N. and J.M. Soden, *Microelectonics Failure Analysis 4th Edition*. Vol. 1. 2001: ASM International, Materials Park, OH. 161.
148. Bauer, E., *The Possibilities For Analytical Methods In Photoemission And Low-Energy Microscopy.* Ultramicroscopy, 1991. **36**(1-3): p. 52-62.
149. Bauer, E., *Low-Energy-Electron Microscopy.* Reports On Progress In Physics, 1994. **57**(9): p. 895-938.
150. Heringdorf, F., M.C. Reuter, and R.M. Tromp, *Growth dynamics of pentacene thin films.* Nature, 2001. **412**(6846): p. 517-520.
151. Tromp, R.M. and M.C. Reuter, *Imaging With A Low-Energy-Electron Microscope.* Ultramicroscopy, 1993. **50**(2): p. 171-178.
152. Ondrejcek, M., et al., *LEEM Investigations of Surfaces Using a Beam of Energetic Self-Ions.* Microscopy Research And Technique, 2009. **72**(3): p. 197-207.
153. Rempfer, G.F. and O.H. Griffith, *Emission Microscopy And Related Techniques - Resolution In Photoelectron Microscopy, Low-Energy Electron-*

Microscopy And Mirror Electron-Microscopy. Ultramicroscopy, 1992. **47**(1-3): p. 35-54.
154. Rempfer, G.F., K.K. Nadakavukaren, and O.H. Griffith, *Topographical Effects In Emission Microscopy.* Ultramicroscopy, 1980. **5**(4): p. 437-448.
155. Ballarotto, V.W., et al., *Photon energy dependence of contrast in photoelectron emission microscopy of Si devices.* Applied Physics Letters, 2001. **78**(22): p. 3547-3549.
156. Kong, X.H., J.E. Rowe, and R.J. Nemanich, *Single molecule measurements with photoelectron emission microscopy.* Journal Of Vacuum Science & Technology B, 2008. **26**(4): p. 1461-1465.
157. Dyukov, V.G., S.A. Nepijko, and N.N. Sedov, *Electron Miscroscopy of Local Potentials (in Russian).* 1991: Naukova Dumka, Kiev.
158. Nepijko, S.A., et al., *Measurement of the electric field distribution and potentials on the object surface in an emission electron microscope without restriction of the electron beams.* Journal of Microscopy, 2003. **211**: p. 89-94.
159. Nepijko, S.A., et al., *Use of emission electron microscope for potential mapping in semiconductor microelectronics.* Journal of Microscopy, 2002. **206**: p. 132-138.
160. Nepijko, S.A., et al., *Resolution deterioration in emission electron microscopy due to object roughness.* Annalen Der Physik, 2000. **9**(6): p. 441-451.
161. Gunther, S., et al., *Photoelectron microscopy and applications in surface and materials science.* Progress In Surface Science, 2002. **70**(4-8): p. 187-260.
162. Bauer, E., *Photoelectron microscopy.* Journal Of Physics-Condensed Matter, 2001. **13**(49): p. 11391-11404.
163. Griffith, O.H. and W. Engel, *Historical-Perspective And Current Trends In Emission Microscopy, Mirror Electron-Microscopy And Low-Energy Electron-Microscopy - An Introduction To The Proceedings Of The 2nd International-Symposium And Workshop On Emission Microscopy And Related Techniques.* Ultramicroscopy, 1991. **36**(1-3): p. 1-28.
164. Griffith, O.H. and G.F. Rempfer, *Advances in Optical and Electron Microscopy*. Vol. 10. 1987, London: Academic Press.
165. Griffith, O.H., et al., *Photoelectron Microscopy - New Approach To Mapping Organic And Biological Surfaces.* Proceedings Of The National Academy Of Sciences Of The United States Of America, 1972. **69**(3): p. 561-&.
166. Siegrist, K., E.D. Williams, and V.W. Ballarotto, *Characterizing topography-induced contrast in photoelectron emission microscopy.* Journal Of Vacuum Science & Technology A, 2003. **21**(4): p. 1098-1102.
167. Nepijko, S.A., et al., *Peculiarities of imaging one- and two- dimensional structures in an emission electron microscope. 1. Theory.* Journal of Microscopy, 2000. **199**: p. 124-129.
168. Sangwan, V.K., et al., *Characterizing Voltage Contrast in Photoelectron Emission Microscopy.* Journal of Microscopy (under review), 2009.
169. Zdrojek, M., et al., *Charging and emission effects of multiwalled carbon nanotubes probed by electric force microscopy.* Applied Physics Letters, 2005. **86**(21).

170. Ba, L., et al., *Probing local electric field distribution of nanotube arrays using electrostatic force microscopy.* Journal Of Applied Physics, 2003. **93**(12): p. 9977-9982.
171. Jesse, S., et al., *In situ electric-field-induced contrast imaging of electronic transport pathways in nanotube-polymer composites.* Applied Physics Letters, 2006. **89**(1).
172. Homma, Y., et al., *Mechanism of bright selective imaging of single-walled carbon nanotubes on insulators by scanning electron microscopy.* Applied Physics Letters, 2004. **84**(10): p. 1750-1752.
173. Weinberg, Z.A., G.W. Rubloff, and E. Bassous, *Transmission, Photoconductivity, And The Experimental Band-Gap Of Thermally Grown Sio2-Films.* Physical Review B, 1979. **19**(6): p. 3107-3117.
174. Williams, R., *Photoemission Of Electrons From Silicon Into Silicon Dioxide.* Physical Review, 1965. **140**(2A): p. A569-&.
175. Goodman, A.M., *Photoemission Of Electrons From Silicon And Gold Into Silicon Dioxide.* Physical Review, 1966. **144**(2): p. 588-&.
176. Ballarotto, V.W., et al., *Photoelectron emission microscopy of ultrathin oxide covered devices.* Journal Of Vacuum Science & Technology B, 2002. **20**(6): p. 2514-2518.
177. Wagner, J., *Photoluminescence And Excitation Spectroscopy In Heavily Doped N-Type And P-Type Silicon.* Physical Review B, 1984. **29**(4): p. 2002-2009.
178. Goodman, A.M., *Electron Hall Effect In Silicon Dioxide.* Physical Review, 1967. **164**(3): p. 1145-&.
179. Gruner, G., *Carbon nanotube films for transparent and plastic electronics.* Journal Of Materials Chemistry, 2006. **16**: p. 3533-3539.
180. Vijayaraghavan, A., et al., *Charge-injection-induced dynamic screening and origin of hysteresis in field-modulated transport in single-wall carbon nanotubes.* Applied Physics Letters, 2006. **89**(16).
181. Kar, S., et al., *Quantitative analysis of hysteresis in carbon nanotube field-effect devices.* Applied Physics Letters, 2006. **89**(13).
182. Rispal, L., et al., *Polymethyl methacrylate passivation of carbon nanotube field-effect transistors: Novel self-aligned process and effect on device transfer characteristic hysteresis.* Japanese Journal Of Applied Physics, 2008. **47**(4): p. 3287-3291.
183. Conrad, B.R., et al., *Percolative effects on noise in pentacene transistors.* Applied Physics Letters, 2007. **91**(24).