ABSTRACT

Title of dissertation: MONOCRYSTALLINE SUPERSATURATED ALUMINUM LAYERS BURIED IN EPITAXIAL SILICON

Hyun Soo Kim, Doctor of Philosophy, 2019

Dissertation directed by: Professor Agis Iliadis
Department of Electrical and
Computer Engineering

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Quantum information device performance in semiconductors and superconductors is limited by the quality of materials and interfaces, particularly the interface to the oxide layer. By merging semiconductors and superconductors in a single crystal material, the oxide layer can be eliminated, and the advantage of both systems can be realized. To explore interface free circuits in quantum computing, I have synthesized and studied a new two-dimensional hole gas in silicon using aluminum layers sandwiched between single crystal Si layers. At high enough Al density, this system is expected to behave as a superconductor in single crystal Si.

The samples were fabricated by low temperature molecular beam epitaxy (MBE) with modulation doping of elemental Al. Scanning tunneling microscope (STM) and scanning transmission electron microscope (STEM) images show epitaxial Si layers with low surface defects and no crystalline defects in the Al enriched

region. Electrical measurements show that holes are the dominant carrier in this system with charge carrier densities of $\approx 1.39 \times 10^{14}$ cm^{-2}, and Hall mobilities of ≈ 20 cm$^2/V \cdot s$. The charge carrier density corresponds to $\approx (0.93 \pm 0.1)$ hole per Al dopant atom. Unfortunately, no superconductivity was observed down to 300 mK. The likely reason for this is found to be re-distribution of Al dopants over $\approx$ (17 to 25) nm due to thermal annealing up to 550 °C, which decreases the peak Al concentration in Si below the critical density for superconductivity.

Al has not been well studied as a dopant in Si due to its low solid solubility, low vapor pressure, and tendency to segregate. To better understand Al as a dopant, the structures and electrical properties of incorporated Al in Si(100) are studied using STM. The scanning tunneling spectroscopy (STS) spectra show shifts of the band edges on incorporated Al compared to (2×1) Si(100) dimers.

To test the compatibility of elemental Al for STM lithography with a hydrogen resist layer, a standard experimental protocol is tested. Elemental Al is evaluated using 3 different metrics: 1) sticking coefficient contrast, 2) effective enthalpy of sublimation contrast, and 3) surface diffusivity by deposition rates. Elemental Al is shown incompatible with STM lithography and hydrogen masking. Our study suggests that other dopants may overcome this difficulty.

Finally, a new method using ion implanted wires is a promising technique for making electrical contacts to devices in Si fabricated with STM lithography. Here, I report a new *in situ* method for detecting ion implanted wires using STM and STS with a novel lock-in technique. Using the ion implanted wires, a-first-of-its-kind STM-patterned nano-wire made of P dopants is demonstrated.

MONOCRYSTALLINE, SUPERSATURATED ALUMINUM LAYERS BURIED IN EPITAXIAL SILICON

by

Hyun Soo Kim

Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
2019

Advisory Committee:
Professor Agis Iliadis, Chair/Advisor
Dr. Joshua M. Pomeroy, Co-Advisor
Professor Robert Newcomb
Professor Martin Peckerar
Professor Kevin Daniels
Professor Lourdes Salamanca-Riba

Foreword

As approved by the Dissertation Committee and the certification letter to the Graduate School, Hyun soo Kim made substantial contributions to the relevant aspects of the jointly authored work included in the dissertation. The certification letter to the Graduate school is included in this section.

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To the Graduate School

Ref. Hyun soo Kim Contributions 09/29/2019

This letter is to certify that my student Hyunsoo Kim had substantial contributions in the two co-authored papers shown below and hence parts of the works can be used in his PhD dissertation:

- Aruna N Ramanayaka, **Hyun-Soo Kim**, Joseph A Hagmann, Roy E Murray, Ke Tang, F Meisenkothen, HR Zhang, LA Bendersky, AV Davydov, Neil M Zimmerman, et al. "Towards superconductivity in p-type delta-doped Si/Al/Si hetero-structures". ***AIP Advances, 8(7):075329, 2018.***

- Aruna N Ramanayaka, **Hyun-Soo Kim**, Ke Tang, Xiqiao Wang, Richard M Silver, Michael D Stewart, and Joshua M Pomeroy, "STM patterned nanowire measurements using photolithographically defined implants in Si (100)". ***Scientific Reports, 8(1):1790, 2018.***

The dissertation advisor, Prof. Agis Iliadis, the co-advisor Dr. Joshua Pomeroy (NIST) and the Dissertation Committee of the Department of Electrical and Computer Engineering, have determined that the student, Hyunsoo Kim (UID:110739012), had substantial contributions in those papers and hence, the material can be used as part of his dissertation.

The paper published in the journal of ***AIP Advances*** is about the study of material synthesis and characterization of a new semiconducting material. Hyun soo Kim has developed and fabricated the new material and was involved in part of its characterization. Since the journal is about developing new materials, the development of the new material is a substantial portion of the published work.

The paper published in journal of ***Scientific Reports*** is partially reproduced in chapter 5 of the dissertation. For that work a new imaging method was developed by my student Hyunsoo Kim, which is the theme of chapter 5 in the dissertation. The new imaging method is critical in the fabrication of the devices presented in the journal. Also, Hyunsoo Kim prepared most of the samples presented in the journal. Therefore, Hyunsoo Kim made substantial contributions to the co-authored work without which no publication would have been possible and hence that part of his work can be included in the dissertation.

Sincerely

Prof. Agis Iliadis

Electrical and Computer Engineering Department

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SPRINGER NATURE

Title: STM patterned nanowire measurements using photolithographically defined implants in Si(100)

Author: A. N. Ramanayaka et al

Publication: Scientific Reports

Publisher: Springer Nature

Date: Jan 29, 2018

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Acknowledgments

Firstly, I'd like to express my sincere gratitude to my advisor Dr. Pomeroy at the National Institute of Standards and Technology (NIST) for his support of the research and my Ph.D. study, motivation, and immense knowledge. Josh always guided me to be a scientist who is not just following orders but can think and work independently. I remember the first day in a lab him showing me how to run STM in a lab and sitting next to each other in front of a small computer desk. At that moment, I did not know that a small desk at the corner of a lab in a basement is where I would spend five years. Since the first day, he has been the best advisor among many other advisors that I have been working with. Josh has been always willing to understand and help me not only in research but also in other things. To summarize, I would give Josh most of the credit for me to get here.

I also would like to thank my on-campus advisor Prof. Agis Iliadis at UMD, for his insightful comments and encouragement, which guided me to widen my research perspectives.

Besides my adviosr, I would like to thank the rest of my dissertation committee members Professor Robert Newcomb, Professor Martin Peckerar, Professor Kevin Daniels, and Professor Lourdes Salamanca-Riba for their insightful comments and consideration, but also for the hard questions, which incensed me to widen my research from various perspectives.

I thank my fellow labmates for the stimulating discussions and years of work in the lab. I want to thank Dr. Kevin Dwyer, a former group member, who has

been breaking and fixing things in a lab together. I also thank Ke Tang and Dr. Aruna Ramanayaka for helpful discussion and countless hours of work in a lab. Their support allow me to have fruitful results. Thank you to all members of Atom Scale Device Group at NIST including Dr. Bryant Garnett, Dr. Neil Zimmerman, Dr. Michael Stewart, Dr. Justin Perron, Dr. Roy Murray, Dr. Hamza Shakeel, Zac Barcikowski, Ryan Stein, Yanxue Hong, Dr. Xiqiao Wang, Dr. Pradeep Namboodiri, and Dr. Jonathan Wyrick for their insights and discussions. Without all the members, my dissertation may not be completed. I truthfully appreciate each and everyone.

Last but not the least, I would like to express my deepest gratitude to my family for their endless love, encouragement, support, and great faith in me. Special thanks to my wife, Sul A Lee and twins, Inseo Paige Kim, and Sejin Aaron Kim. While working and taking care of twins, Sul A supported me to finish my degree. I truly thank Sul A for sticking by my side during . Inseo and Sejin are the best gift and the greatest achievement in my life. Just the presence of Inseo and Sejin is and will be the greatest motivation and joy.

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Chapter 1

Introduction

Over the last 50 years, the semiconductor industry has greatly advanced the number of transistors following the Moore's law, as shown in Fig. 1.1. Moore's law predicts that the number of transistors and computational power double every two years since 1965. Since the first 20 μm metal-oxide-semiconductor field-effect transistor (MOSFET) transistor in 1960, as shown in Fig. 1.1, integrated circuits now have tens of millions of transistors. [3] The processing power of a smartphone that we use everyday on our palm already surpass the processing power of the first supercomputers that sent us to the moon. Recently, mass production of a single transistor with a size of 5 nm node using extreme ultraviolet lithography (EUVL) was announced, which will be commercially available soon. [4] The semiconductor industry now even announced the plan for commercialization of the 3 nm node in near future. [5] The advancement in scaling of nanodevices was only possible with development of new materials. As the size of transistors shrinks, quantum effects affect the device's performance. For example, as a size of a node shrinks, gate tunneling becomes significant as a consequence of shrink in the oxide thickness, which

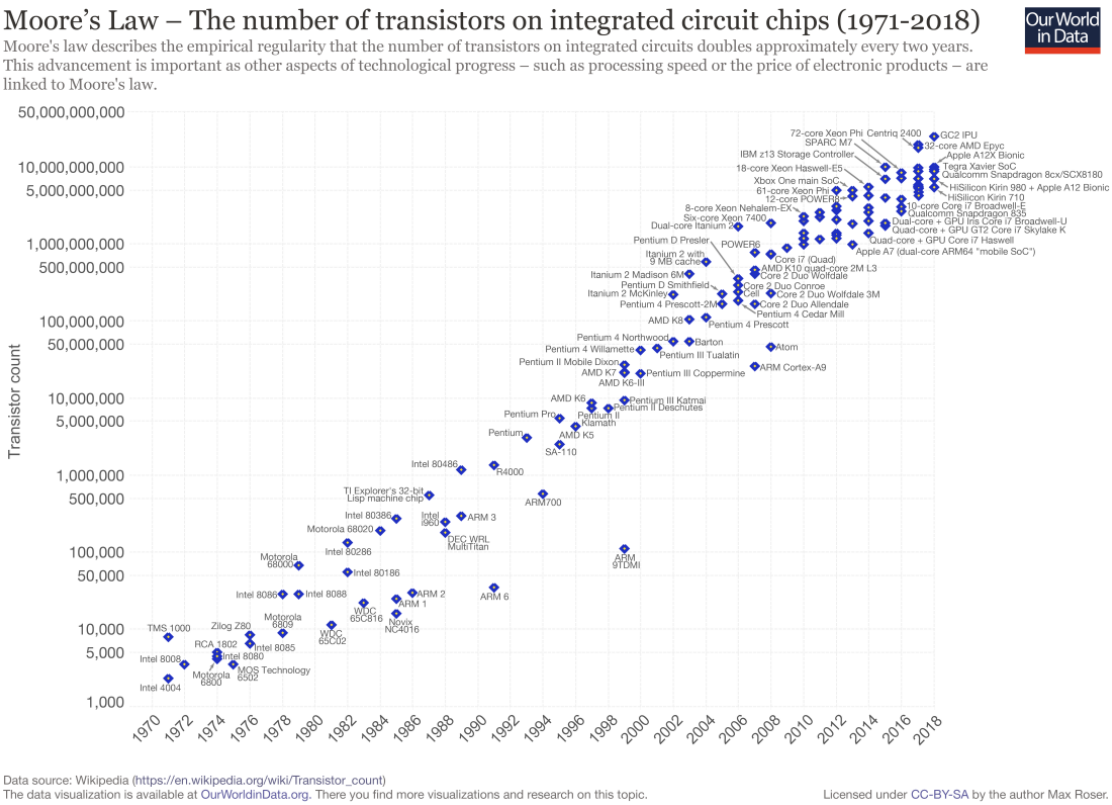

Fig. 1.1: This is a plot of the number of MOS transistors from 1971 to 2018. Moore's law is the observation that the number of transistors doubles every two years. [7]

demands the development of a new gate material with a high dielectric constant. [6] Then, the incorporation of new materials requires the development of new fabrication technology to be compatible with existing materials and fabrication technology.

Fig. 1.2 shows a schematic overview of new materials with respect to the year they entered mass production. [8] In order to solve the problems of scaling of nanodevices, the demands of developing new materials is increasing every year almost exponentially. [9] The size of the stack of the new materials each year in Fig. 1.2 keeps increasing. Beyond the 5 nm or the 3 nm nodes, not only the technical challenges, such as fabrication technology, quantum effects, and material issues, the Moore's law approaches to the fundamental limit, as the size of the node reaches

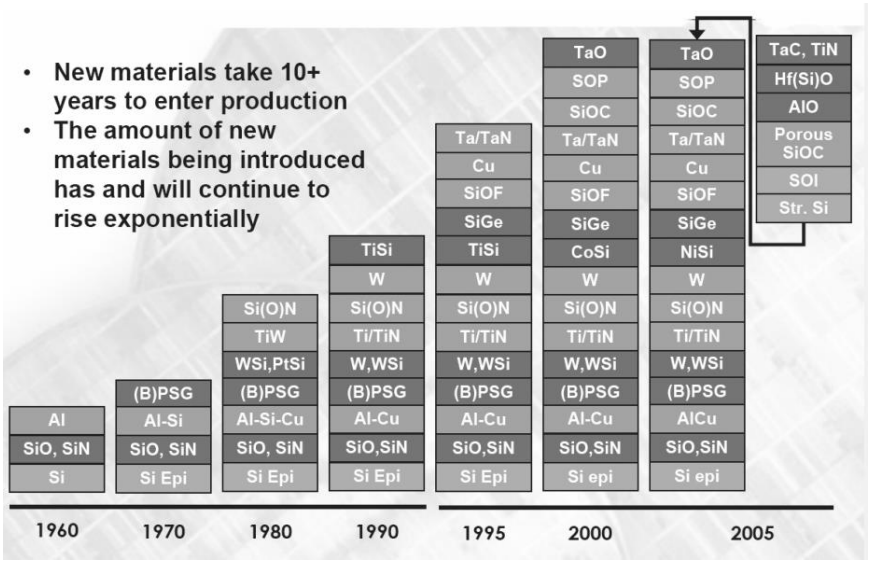

Fig. 1.2: This is a schematic overview of new materials with respect to the year they entered mass production. [8]

to the atomic scale. Even with great advancement, there are still limitations in the classical computer, which uses the bits of 0 and 1. The quantum computer with quantum bits (qubits) can solve problems that are not possible with the classical computer because of superposition and entanglements. [10, 11]

The two-level system qubit with basis vectors $|0\rangle$ and $|1\rangle$ is often described by the Bloch sphere as shown in Fig. 1.3. [12] A pure energy state, $|\phi\rangle$ of a qubit is represented by the mixed states or superposition of basis vectors $|0\rangle$ and $|1\rangle$, which for example corresponds to the spin-up and spin-down states of the electron spin. A quantum computer uses $|0\rangle$, $|1\rangle$, and superposition of two qubit states. Superposition enables a qubit to have any value between $|0\rangle$ and $|1\rangle$. Entanglement enables qubits to share states with each other. Therefore, n qubits can have superposition of up to 2^n states. As an example of the computational power, for 3 bits, there are eight configurations, such as (000), (010), (001), (100), (110), (011), (101), and (111). In

order to compute a solution for 3 bits, the classical computer has to compute each of eight configurations one at a time while the quantum computer can compute all eight configurations at once. As the complexity of the problem increases, the computational power of the quantum computer rapidly exceeds the classical computer. With the most sophisticated optimization processes, some computations in the classical computer that require enormous number of calculations cannot be solved, such as integer factorization (cryptography), optimization (supply chain, logistics, and air traffic), and simulations for chemistry and materials. This kind of computation with the classical computer can take longer than life time of the universe.

In quantum computing, various types of qubits have been extensively studied, such as the semiconductor, the superconductor, the trapped ions, and etc. For all quantum computing, the two-level qubit with $|0\rangle$ and $|1\rangle$ are represented with the Bloch sphere shown in Fig. 1.3. [13] The north and south poles of the Bloch sphere represent $|0\rangle$ and $|1\rangle$, respectively. The surface of the Bloch sphere presents the mixed states of superposition, $|\Phi\rangle$ of $|0\rangle$ and $|1\rangle$. The qubits are characterized by two important parameters, such as the spin relaxation time (T_1), and the coherence time (T_2). T_1 to relax from the higher energy state of $|0\rangle$ to the lower energy state of $|1\rangle$ is described with a red arrow (θ) in Fig. 1.3. [13] Another parameter, represented with a green arrow (φ) in Fig. 1.3, is the time to maintain the coherent phase of spins. The qubits need to maintain their quantum phase before the information of the qubit is lost due to the interaction to the environment. For quantum computing, T_2 is needed to be $\approx 10^6$ times longer than the gate operation time since the coherent phase of spins needs to be maintained during gate operation due to the dephasing

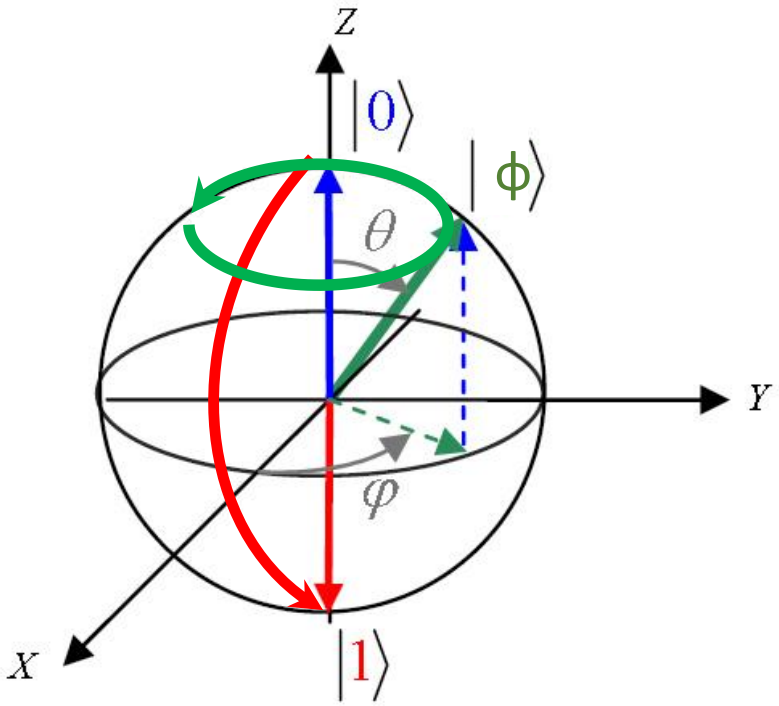

Fig. 1.3: This is the Bloch sphere which is geometrical representation of a two-level qubit. The north and south poles of the Bloch sphere reprent the basis of the qubit as $|0\rangle$ and $|1\rangle$. The surface of the Bloch sphere, $|\Phi\rangle$, is the mixed states or superposition of the basis vectors $|0\rangle$ and $|1\rangle$. The red arrown pointing from $|0\rangle$ to $|1\rangle$ represents the relaxation time which means average lifetime in the higher energy state. The green arrow represents lifetime to maintain coherent phase.

error. T_2 is measured by the electron spin resonance (ESR), which is related to the linewidth of the ESR signal in the bulk ESR experiments. [14, 15] For ESR experiment, the external magnetic field along the z-axis in Fig. 1.3 induces the energy separation between the spin-up and the spin-down states, known as Zeeman splitting, with the precession of the spin states about the z-axis, known as Larmor precession. By applying an microwave driving field, which is resonant with the Zeeman splitting, the spin states of $|\Phi\rangle$ in Fig. 1.3 can be rotated about the x-

axis, which means that $|\Phi\rangle$ is on the x-y plane of the Bloch sphere. [14] Then, the spin states are measured over varying spin evolution time, which determines the dephasing time or T_2. The interact of the spins to the environment, due to the inhomogeneous magnetic fields, reduce the coherence time denoted as T_2^*, which is considered as "effective" T_2. Certain manipulations of the spins using the pulse sequences, such as a Hahn echo or dynamical deoupling ,can enhance the coherence time by reducing the effect of the environmental noise.

The trapped ion quantum computing has the relatively long T_2. The trapped ion quantum computing uses the ions as qubits trapped in free space using the electromagnetic field at radio frequency (RF). Since the ions are trapped in free space, the interaction to the environment is minimized, which results in the long T_2 up to 600 seconds using the dynamic decoupling technique. [16–18] Typical two-qubit gate operation time for the trapped ion is 1 to 100 μs, which exceeds the 10^6 ratio between T_2 and the gate operation time. Also, the controllable entanglement of 20 trapped ions has been demonstrated. [19] However, the trapped ions quantum computing also has some disadvantages, such as slow gate speeds, difficulty to scale many number of trapped ions, error correction for lost ions, dephasing due to a nonuniform magnetic field, and the physical movements due to the unintended electric fields. [18]

In semiconductor quantum information, Si is a promising candidate for intrinsic material properties and compatibility with existing complementary metal-oxide-semiconductor (CMOS) technologies. Long coherence time has been demonstrated in Si due to small spin-orbit coupling, which is a important parameter for spin re-

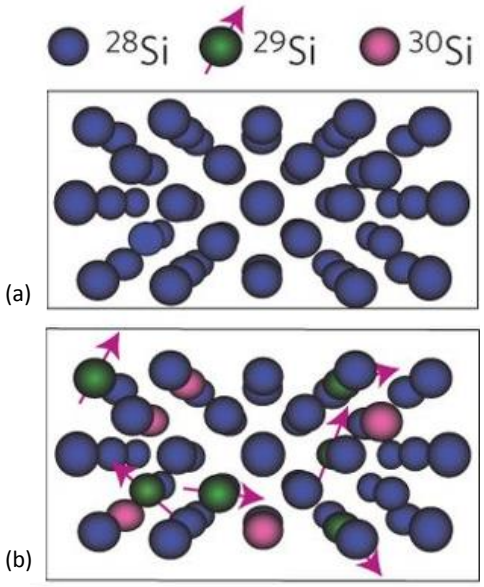

Fig. 1.4: A schematic drawing of the isotopically purified ^{28}Si and natural abundance Si. The blue spheres are the ^{28}Si. The green spheres are the ^{29}Si. The red arrow represents the nuclear spins. The red spheres are ^{30}Si. (a) This is the schematic drawing of isotopically purified ^{28}Si by eliminating ^{29}Si ^{30}Si isotopes. (b) This represents Si with natural abudance of ^{28}Si, ^{29}Si, and ^{30}Si with random distribution of nuclear spins of ^{29}Si. [23]

laxation. [11, 20, 21] Due to the small atomic number and the large band gap, the spin-orbit coupling in Si is small. The inversion symmetry in Si eliminates Dresselhaus effect, which leads to the long T_1. Si also has been demonstrated to have the long T_2 to exceed 1 seconds for a single donor's electron spin and $\approx$ 30 minutes for nuclear spin in bulk, which could be achieved with isotopic purification of ^{28}Si. [21, 22]

Natural abudance Si is comprised of three isotopes, 92.23 % of ^{28}Si, 4.67 % of ^{29}Si, and 3.1 % of ^{30}Si. The ^{29}Si has a nuclear spin $I = \frac{1}{2}$ while ^{28}Si and ^{30}Si have zero nuclear spin. The nuclear spin of the ^{29}Si isotope causes the inhomogeneous magnetic field. The inhomogeneous magnetic field is also known as the Overhauser field due to nuclear and impurity spins in the crystal. Without the Overhauser field

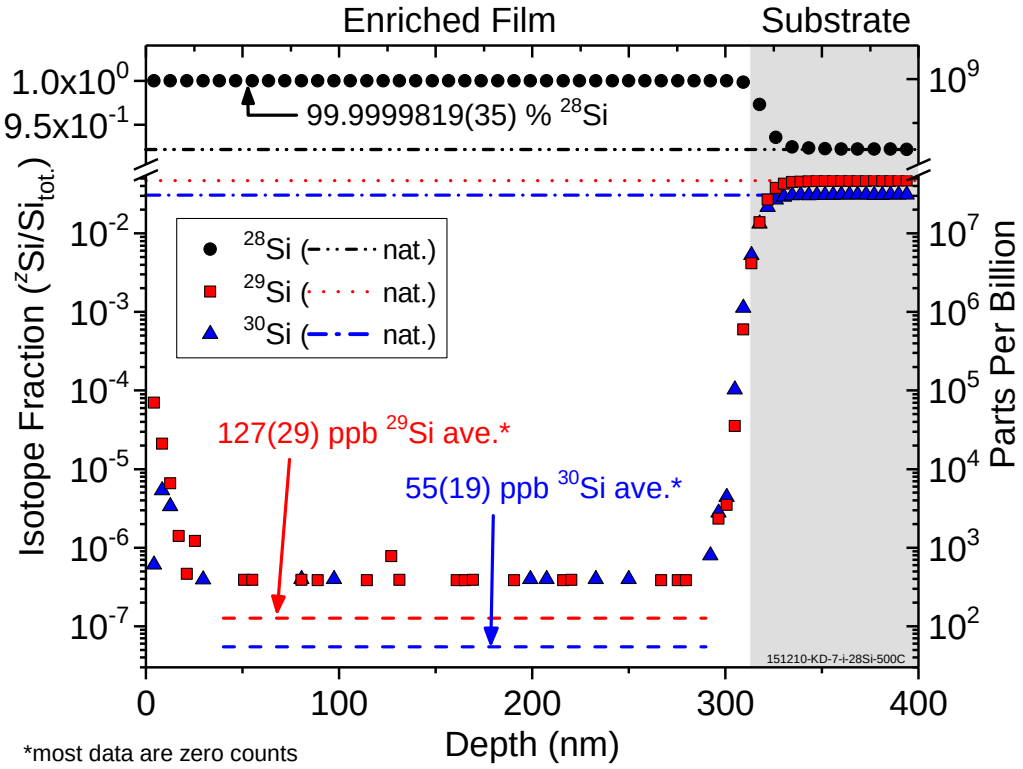

Fig. 1.5: The isotopically enriched ^{28}Si epilayer grown at 450 °C using the Penning ion source and the mass spectrometer. The fabrication method is explained in section 2.4.1. This plot is the depth profile of concentration of Si isotopes (^{28}Si, ^{29}Si, and ^{30}Si) measured by the secondary ion mass spectrometry (SIMS). The enrichment level of the ^{28}Si isotope of this sample is < 1 ppm.The red dots are ^{29}Si with the average concentration of 127(29) ppb (red dashed line). The blue dots are ^{30}Si with the average concentration of 55(19) ppb (blue dashed line). The gray area is the substrate where the concentration of the Si isotopes returns to the natural abundance level.

from ^{29}Si nuclear spin, the coherence time can be greatly enhanced. Theoretical study ^{28}Si and bulk ESR experiments predicted the increase in coherence time with decrease of the ^{29}Si concentration. [24, 25] This is often referred as "semiconductor vacuum", which means the nuclear spin free environment by eliminating the nuclear spin of ^{29}Si. The high isotopically enrichement level of ^{28}Si to 99.9999819(35) % is achieved with less than 1 ppm of ^{29}Si and ^{30}Si as measured by secondary ion mass

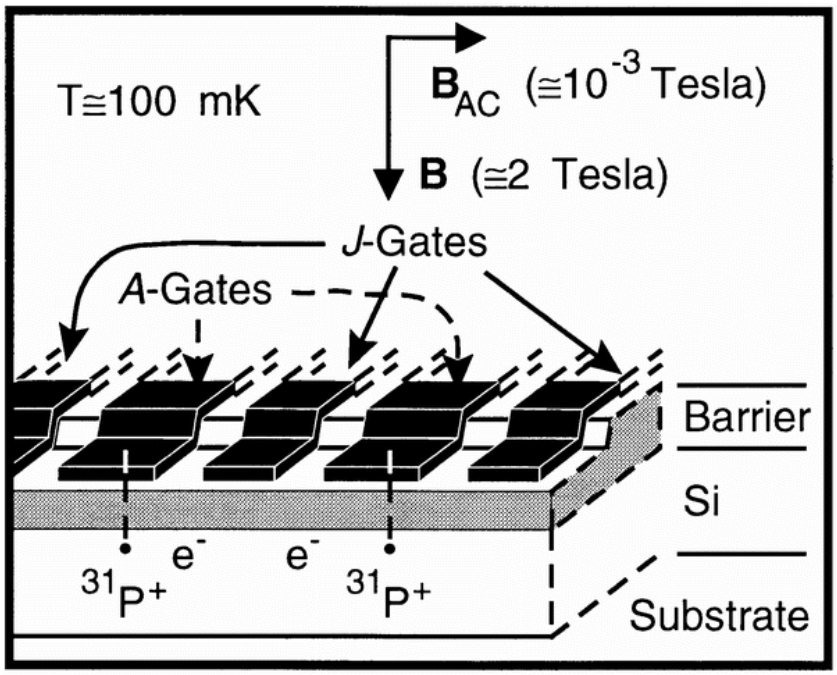

Fig. 1.6: This is a schematic drawing of the proposed Kane quantum computer, which is made of an array of ^{31}P donors in Si. The Kane quantum computer is proposed to operate using A-gates to control the ^{31}P donors, J-gates to control the coupling between the electron spins of the donors, and a global AC magnetic field to flip nuclear spins. This is taken from Ref. [11].

spectrometry (SIMS) in Fig. 1.5. The ^{28}Si enriched film is grown using a Penning ion source and a mass spectrometer. The limitation of this method to enrich the ^{28}Si isotope is the chemical contamination from the ion beam, which is discussed in section 3.3.2.

Quantum dots in solid state quantum information are electrostatically defined by gate electrodes. Various structures of the quantum dots have been demonstrated including the Si surfaces, Si nanowires, and Si/SiGe heterostructures. Also, another popular quantum computing device in Si is the Kane quantum computer proposed by Bruce Kane, which is made of an array of phosphorous donor (^{31}P) in Si. [11] As shown in Fig. 1.6, the proposed Kane quantum computer uses three parameters to

control the qubits; the A gates above the donor to control the ^{31}P donor (electron-nuclear coupling), J gates to control the coupling between the electron spins of the donors, and a global AC magnetic field to flip nuclear spins. The single electron transistors (SET) are proposed to detect the spin-dependent tunneling from the target qubit to a charge neutral donor. [11, 26] This proposed quantum computer requires precise placement of the ^{31}P donor in Si. Research groups have used ion implantation and scanning tunneling microscopy (STM) lithography with H passivation to fabricate devices towards the quantum dots and P donors in Si. [27–29] Especially, since the first demonstration of the STM lithography by J. Lyding *et al.*, the group at University of New South Wales first demonstrated nanowires, quantum dots, and a single atom transistor. [30–33] Another group at National Institute of Standards and Technology (NIST) also demonstrates the nanowires and quantum dots made of P donors in Si using the STM lithography. [34]

The electron-based qubits in Si, such as P donor qubits in Si and etc, makes the electrical coupling difficult due to the weak spin-orbit interaction. Stronger spin-orbit coupling in a hole-based spin qubit can enables the realization of all-electrical spin manipulation. [35, 36] Electrical manipulation of hole spin in Si has been demonstrated, which can allow to couple qubits over long distance. [37] Hole-based qubit designs have attracted significant interest in semiconductor quantum information device architectures as a result of the longer spin decoherence times due to the suppression of hyperfine interaction between holes and nuclear spins. [35,38] In addition, the absence of the valley degeneracies makes the hole spin qubits more attractive compared to six fold valley degeneracy of the electron. However,

the acceptor based devices in Si fabricated by STM lithography have not been demonstrated. Significant remaining challenges for the semiconductor qubit are the reproducible coupling between qubits, which is mainly due to the material and the interface between the semiconductor and the oxide layer.

On the other hand, in superconducting quantum information, the Josephson junction (JJ) has been used for magnetometers, voltage standards, logic and qubits. [39–43] Major companies, such as IBM, Intel, Microsoft, and Google, have been investing on superconducting quantum computing. [44] One of advantages of superconducting qubits is good coupling mechanism using cavity quantum electrodynamics (cQED) to enable coupling many qubits. [45] However, disadvantage of superconducting qubits is poor coherence times of < 100 μseconds. Also, the major source of the losses is in or, at the interfaces between dielectrics (oxides), JJ junctions, and the substrate.

Superconductor and semiconductor qubits have been studied and demonstrated as candidates for the quantum computer, which shows the strengths and weakness of each materials. [10,11,46] Both of superconductor and semiconductor are limited by material and interface qualities. [47] By combining two materials into a single crystal superconducting semiconductor, this new type of quantum information devices made of superconducting semiconductor with no interface can have the strengths of both superconductor and semiconductor. [48] The proposed quantum information devices consist of the superconducting wires, JJs and qubits in a single Si crystal to keep the devices from the interfaces. This proposed device can harness the strength of the long coherence time of the semiconductor qubits and cQED coupling of supercon-

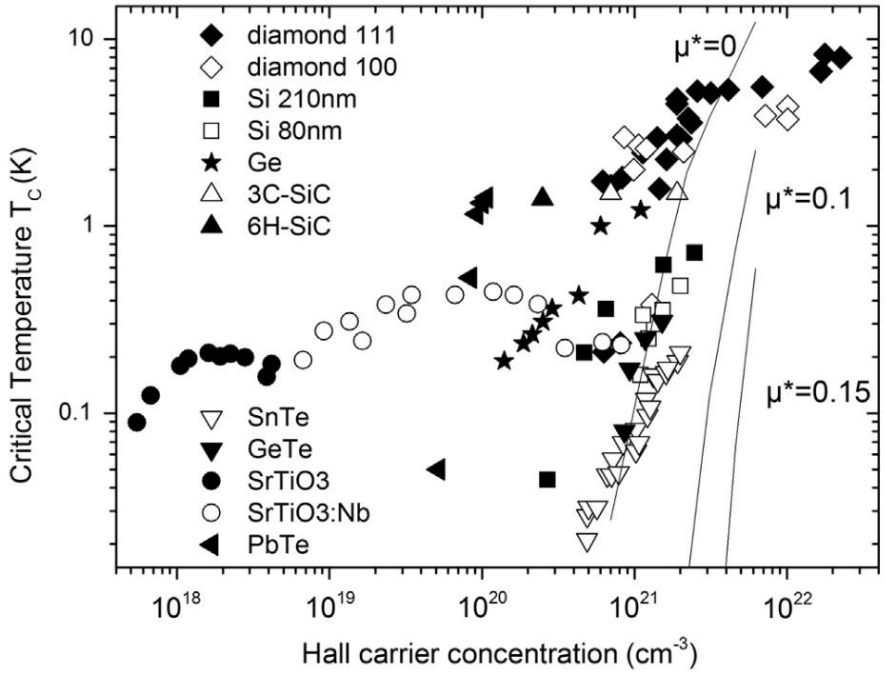

Fig. 1.7: This is a plot of the critical temperature T_c (K) as a function of the Hall carrier concentration for various superconducting semiconductor materials. This is from Ref. [49]

ductor and eliminate the interface loss for both semiconductor and superconductor. In order to fabricate quantum computing devices with interface free superconducting semiconductor as proposed by Shim and Tahan, the two-dimensionally confined superconducting semiconductor with single-crystallinity is required. [48]

The first superconducting semiconductor was demonstrated in heavily boron doped diamond grown by the microwave plasma-chemical vapor deposition (CVD) method with high pressure or high temperature. The highest critical temperature measured on the highly boron doped diamond is 11.4 K. [50] Since the heavily B doped diamond, the superconductivity in a semiconductor has been demonstrated in a wide range of materials, such as GeTe, PbTe, $SrTiO_3$, and In_2O_3 as shown

in Fig. 1.7. [51–54] For the proposed quantum device by Ref. [48], covalent superconductor is necessary to combine superconducting circuits and qubits using STM lithography. [48] Superconductivity in Ge and SiGe was theoretically predicted in the 1960s. [55] Also, the superconductivity in Si also has been predicted. [56] However, since the theoretical prediction, it took a few decades to observe superconductivity in Ge and Si. [57,58] Superconductivity in a semiconductor is only possible at doping densities above the metal-insulator-transition (MIT). The band gap of a semiconductor is typically much larger than the superconducting energy gap. Therefore, pure semiconductors are not superconducting. [59] For a semiconductor, doping, which is the impurity atoms substituting the semiconductor atoms creates impurity energy states within the band gap, such as donor states and acceptor states. As the doping concentration increases, the donor or acceptor energy states overlap and causes the band of the electronic energy states by broadening of the donor or acceptor states. [59] For a degenerately doped semiconductor, the electrons remain in the conduction band even at 0 K and contribute to the electrical conduction, which works as unpaired electrons in the normal state of the superconductor. [59] In order to achieve superconductivity in a covalent semiconductor, the doping density correspond to being above the equilibrium solid solubility limit. The equilibrium solid solubility limit means the limit of the amount of the solute in solvent in solid compounds. The nonequilibrium doping at such high density causes inhomogeneous materials such as segregation of dopants, formation of clusters and precipitates, and pollycrystalline materials. [60–62]

In order to achieve the doping density above the solid solubility, non-equilibrium

doping techniques are required, such as high-pressure/high-temperature synthesis, or chemical vapor deposition, gas immersion laser doping, and high influence ion implantation with rapid thermal annealing or flash lamp annealing for Si and Ge. [58, 63–65]

All the superconductivity in the covalent superconducting semiconductor has been observed in the highly hole doped materials; B doped diamond, B doped Si (B:Si), Ga or Al doped Ge (Ga:Ge or Al:Ge), B or Al doped SiC (B:SiC or Al:SiC). [57, 58, 63, 65] The recent study of the single-crystalline Ga:Ge and Al:Ge shows superconductivity at T_c of 0.45 K and 0.15 K, respectively with a doping density of 6 at. %, which is nearly 8 times higher than solid solubility limit. [65] Despite of the single-crystallinity, Ga:Ge and Al:Ge are not compatible with Si qubits using STM lithography. The proposed qubits require a superconducting Si with single crystallinity, which can fabricate Si qubits with long coherence time with superconducting circuits.

The next superconducting Si also has been demonstrated using non-equilibrium doping with Ga and B. [58, 61] The Ga:Si, which is fabricated by rapid thermal annealing (RTA) of gallium ion implanted Si, had the higher critical temperature (T_C) of 7 K. However, since the superconducting region lie at the Si-SiO_2 interface, this is not ideal to make interface-free quantum information devices. As mentioned above, the interface between the superconductor and the dielectric causes significant loss in quantum computing devices. Also, the interface in semiconductor quantum dots affects the reproducibility of coupling between devices. [61, 62] Therefore, by burying the active device regions from the dielectric interface, the devices in a single crystal

can be protected from the main source of the loss.

Another superconducting Si is the hyper-boron doped Si (B:Si), above the solid solubility limit (1.2 at. % or 6×10^{20} cm^{-3}) by using gas immersion laser doping. [58] The T_C of B:Si with the B density of 6.5 at. % or 3.2×10^{21} cm^{-3} is approximately 0.35 K. The highly Al doped Si is predicted to have the higher critical temperature for superconductivity than the highly B delta doped Si. [66] The lattice contraction due to the substitution by impurities with a smaller covalent radius, like the Al influence the electron-phonon coupling strength. [66] However, the superconducting Al-Si superlattice has not been demonstrated yet. However, the Al has not been studied well as dopants in Si due to the technical challenges of Al doping in Si, such as low solid solubility of Al in Si (0.04-0.06 at. % or 2-3$\times$ 10^{19} cm^{-3}), low vapor pressure of Al, and tendency of segregation at the high doping density. [67]

Alternative method to overcome these obstacles for non-equilibrium doping and fabricate a 2D plane of dopants in single crystalline Si is delta-doping using low temperature molecular beam epitaxy (MBE). The doping profile in the material growth direction resembles a delta-function with a sharp spike only a few nm in width. As semiconductor growth techniques with a monolayer control of doping and low temperature MBE advances, atomically abrupt junctions, which are 2D doped planes in the material growth direction become possible as demonstrated in Si delta-doped with Sb, B, and P by several groups. [68–71]. Ion implantation also gives the sharp doping profile at various doping densities. However, the radiation damage induced by the injected ions causes crystal damage of the implanted crystal and can introduce other chemical impurities, such as C and O. [72] The damage in

the crystal requires a careful annealing to recrystallize the amorphized region. [73] Another limitation of the ion implantation is the relatively broad dopant profile due to the straggle and the proximity effect of the ion implantation. Also, the control of the depth and the straggle is not independent.

The first delta-doped semiconductor is GaAs doped with Si and Ge using chemical vapor deposition (CVD) in 1979. [74] Then, epitaxial GaAs with periodically modulated Ge doped planes was demonstrated to fabricate various doping profiles with various doping profiles at different densities. [75]. Also, the Sb delta-doping in Si was demonstrated for doping densities exceeding the solid solubility limit. [76–79] The 2D system like the delta-doping is a precursor to make other low dimensional nanodevices, such as nanowires, the SET, a single atom transistor, and etc. Delta-doping requires low thermal budget to minimize dopant diffusion and create an epitaxial Si overgrown layer.

Along with the development of superconducting semiconductor, fabrication of nanodevices using STM lithography is challenging to align and connect the buried devices to external electrical contacts. After device fabrication with STM lithography, the nanodevices are buried with Si capping layers. Therefore, even with the most advanced, state-of-the-art fabrication tools, simply finding the buried nanodevices to contact is often unsuccessful, and every devices requires a customized pattern for electrical contacts. Typically, the buried nanodevices are imaged using scanning capacitance microscope (SCM), kelvin probe force microscope (KPFM), and scanning microwave microscopy (SMM) [80–82] However, those methods requires a customized pattern for electrical contacts for every devices with the elec-

tron beam lithography. Also, those methods are *ex situ* process. Until now, the STM patterned devices are fabricated in two-dimensional plane. In order to scale 2D devices by STM lithography, multiple layers of 2D STM patterned devices has to be fabricated in UHV during the entire fabrication process. Therefore, *in situ* imaging technique is required to scale STM patterned devices.

In this thesis, I first demonstrate the epitaxial growth of Si at low temperature (450 °C) using the ultra-high vacuum (UHV) MBE system, which is essential to make the delta-doped layers in Si. Then, I demonstrate the Al delta-doped Si, which is the Si/Al/Si heterostructure, using dosing of atomic layer of elemental Al and low temperature UHV Si MBE. I optimize the material synthesis to achieve the high charge carrier density and sharp spatial confinement, which is required to observe superconductivity in highly Al delta doped Si. I also developed an *in situ* imaging method to detect pre-implanted contacts for STM lithography using real time STM and scanning tunneling spectroscopy (STS). To simplify the fabrication process for STM patterned devices, the photolithographically defined ion implanted wires in a wafer scale are demonstrated with. I considered distinct physical mechanisms; sticking, sublimation, and surface density modulation, to test compatibility of candidate dopants with STM lithography using the H resist layer in UHV. Elemental Al has been tested for the 3 mechanisms with the H resist layer on the Si(100) surface.

1.1 Outline

- **Chapter 2:** The experimental apparatus and methods to fabricate the Al delta-doped Si(100) including the ^{28}Si ion-beam deposition system, Si electron gun deposition system, and the UHV furnace for the elemental Al deposition, the *in situ* hydrogen passivation for the STM lithography are presented. Also, *ex situ* and *in situ* sample preparation process to obtain a clean (2×1) reconstructed Si(100) are discussed. The basic principle of the STM, STS, and STM lithography is presented.

- **Chapter 3:** The fundamentals of the (2×1) reconstructed Si(100) surface, surface defects, chemical and metal impurities are discussed. UHV Si overgrowth using MBE at the low temperature is presented including epitaxy and impurities in Si. In order to improve the chemical impurities in the overgrown Si layers, post-annealing process after Si deposition is presented.

- **Chapter 4:** The fabrication process to optimize the doping process for the Al-delta doped Si is presented. The material synthesis of the Al delta-doped Si is characterized by Scanning Transmission Electron Microscope (STEM), X-ray Energy Dispersive Spectroscopy (EDS), and Atom Probe Tomography (APT). Using mesa-etched Hall bar devices, electrical properties of the Al delta-doped layer is characterized.

- **Chapter 5:** Real-time STM/STS using lock-in technique is presented to detect ion implanted wires made of various dopants for STM lithography. Using

a real-time STM/STS lock-in technique, nanowires made of the P dopants are fabricated using the photolithographically defined, pre-implanted wires, and electrically characterized.

- **Chapter 6:** I design and test the 3 distinct physical mechanism to verify if a candidate dopant is compatible with STM lithography and the H resist layer. Elemental Al is used for the set of tests.

- **Chapter 7:** A summary of the main scientific results is presented. Then, experimental proposals to study the incorporated Al in Si using the STS is discussed. Also, a proposed fabrication process to improve the spatial confinement of the Al delta-doped layer in Si is discussed.

Chapter 2

Experimental Apparatus and Characterization Methods

In this chapter, I will explain the experimental apparatus and characterization methods. Most of our fabrication process are performed in the ultra-high vacuum (UHV) condition of the base pressure of $\approx 4 \times 10^{-11}$ Torr. Starting with the UHV chamber configuration, I will go through the UHV chamber configuration consisting of scanning tunneling microscopy (STM) chamber, the UHV deposition systems, and ^{28}Si ion beam deposition system. Then, I will explain how the pyrometer to measure the sample temperature from the outside of the vacuum to avoid the metal contamination from the thermocouple. The sample preparation process and the fabrication process require accurate temperature reading; therefore, using the Au-Si and Al-Si eutectic samples, the emissivity of the pyrometer is calibrated. Then, the basic principle of STM, which is extensively used in this work. The STM also can be used as a spectroscopic tool and a lithographic tool, which will be explained in this chapter.

Then, the detail procedures of the *ex situ* and *in situ* sample preparation

process is discussed to obtain a clean (2×1)Si(100) reconstructed surface with low surface defects and no contaminants, which is inspected by the STM. The *in situ* sample preparation included the high temperature flash annealing to 1200 °C, which can cause outgassing from the other parts of the sample holder and manipulator. The two other methods are tested to reduce the temperature during the *in situ* sample preparation process.

In the last section of this chapter, the UHV deposition systems are introduced including ^{28}Si ion-beam deposition system, the Si(100) electron beam deposition system, the UHV thermal furnace for the elemental Al deposition, and the *in situ* hydrogen passivation system.

2.1 UHV Chamber Configuration

These experiments require an UHV chamber in order to reduce contamination sources during the process. The vacuum system consists of three parts such as a load lock vacuum chamber, an UHV deposition chamber, and the UHV scanning tunneling microscope. The load lock chamber is an auxiliary chamber to reduce the time cycle during loading and unloading the samples to UHV chambers. The load lock chamber is separated from the UHV deposition with a gate valve. The base pressure of the UHV deposition chamber is typically 5.0×10^{-11} Torr. Especially, in UHV surface science, the langmuir is often used to define the unit of exposure to a surface by the adsorption of gases. One langmuir(L) is defined by the exposure of 10^{-6} Torr during one second with assumption that the sticking coefficient is 1. [83]

1L corresponds a monolayer of absorbed gas molecules on the surface. Since most of the fabrication and surface characterization processes are performed in the UHV deposition chamber, the lowest possible vacuum pressure is one of the most important conditions to prepare the clean flat surface on the substrates before fabrication process.

This chamber is equipped with two turbo pumps, an ion pump, titanium sublimation pump, and liquid nitrogen cryoshroud. For deposition, an Si evaporator is installed at some distance from an Al evaporator (Radak 1 furnace from Luxel) to avoid Al auto-doping during Si deposition. For hydrogen passivation, a hydrogen gas manifold and cracking tungsten filament are installed. For surface analysis, reflection high-energy electron diffraction (RHEED) and the Auger electron spectrometer (AES) are installed to analyze the surface crystal structures and chemical contaminants. The chamber is constantly monitored by residual gas analyzer during every process. The sample preparation, the Si deposition, and RHEED are performed on the 5 axis-sample manipulator with heating capability. The Al deposition and AES are done on the magnetically coupled transfer rod. The UHV STM chamber is separated from the deposition chamber by a gate valve. The base pressure of the STM chamber is $\approx 4 \times 10^{-11}$ Torr using an ion pump, TSP, and LN_2 cryoshroud. The sample can be transferred between different locations in the UHV system using wobble sticks and a magnetically coupled linear translator arm.

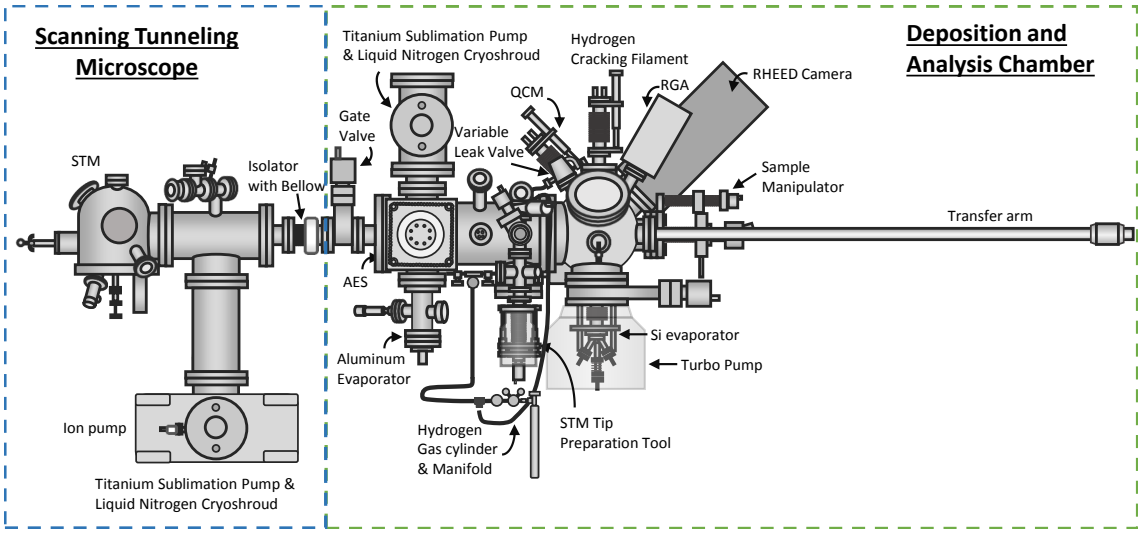

Fig. 2.1: This is the side-view of the UHV system. The deposition and analysis chamber is pictured at the right. The load lock chamber is located above STM tip preparation tool. The STM chamber is pictured on the left. A long transfer arm is used to move samples to various locations in the UHV system for fabrication and analysis.

2.1.1 UHV Chamber analysis

The deposition chamber is pumped by two turbo pumps (Pfeiffer Vacuum 685 L/s and Edward Vacuum 300 L/s), the titanium sublimation pump with liquid nitrogen cryoshroud, and the ion pump. The typical base pressure of the deposition chamber is 5.0×10^{-11} Torr. In order to achieve the UHV condition, when the chamber is exposed to the air, the entire chamber needs to be heated above 150°C for several days, commonly referred as bake-out. The water and other impurities inside the chamber are pumped slowly, therefore, the heating of the chamber can shorten the period to reach the UHV environment.

The residual gas analyzer on the deposition chamber monitors the partial pressure of vacuum components which can be contaminants in our samples. RGA shows that H_2, C, H_2O, CO and N_2, and CO_2. These components might contribute

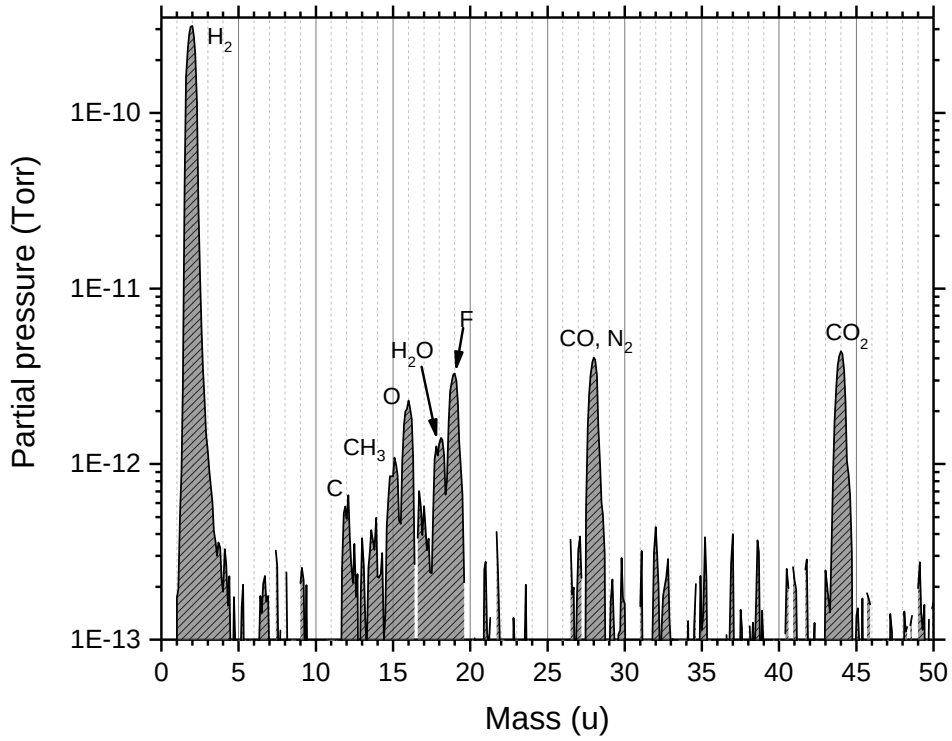

Fig. 2.2: This is a typical RGA scan of the deposition chamber at 5.2 $\times 10^{-11}$ Torr.

to the contaminants in our samples.

2.1.2 Temperature calibration with Si eutectic samples and a pyrometer

The sample preparation and other *in situ* fabrication process strongly depends on the accurate temperature measurement on the sample. Since thermocouples cause metal contamination on the sample discussed in section 3.3.1, a pyrometer is used to measure the surface temperature from outside of the UHV chamber. The pyrometer measures thermal radiation emitted from an object at certain wavelengths, which allows measurement of the temperature at some distance. However,

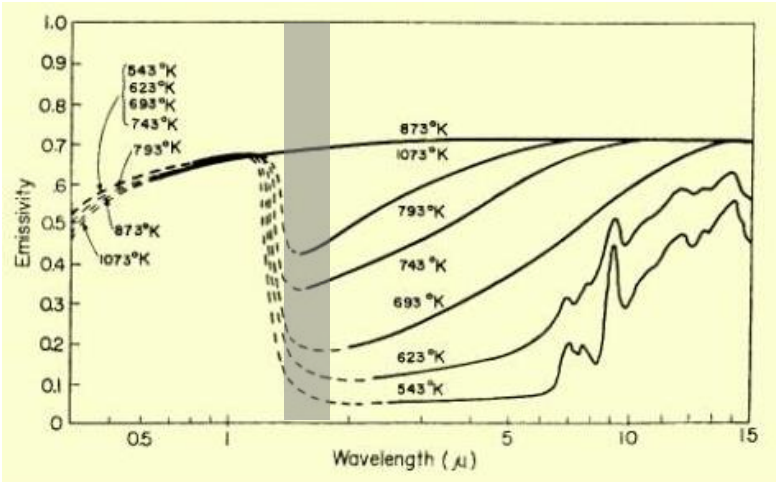

Fig. 2.3: This is a spectral emissivity of Si at the range of temperatures from 543 K to 1073 K. The shaded area is the range of the operating wavelength for the pyrometer. This is taken from Ref. [1].

the pyrometer requires a careful calibration of emissivity, which is the ratio of the amount of energy received at the pyrometer compared to a blackbody at the same temperature. The choice of the pyrometer is limited because of the wide range of temperature required for the fabrication process from 300 °C to 1200 °C, the distance from the sample in the UHV chamber to the pyrometer at the outside of the chamber, and the small size of our sample (4 mm × 10 mm). Our pyrometer is SI16 from Sirius with the temperature range of 300 °C to 1300 °C and a working distance of 2000 mm. The spectral range of the pyrometer is between 1.45 μm and 1.8 μm. Unfortunately, the emissivity of silicon at the spectral range of the pyrometer changes from $\approx$ 0.05 to 0.7 as the temperature increases from 543 K to 1073 K in Fig. 2.3. [1] During fabrication process, the emissivity needs to be carefully chosen according to each temperature range.

For the emissivity calibration, eutectic samples were used as references. An

eutectic is a mixture of two or more substances with a lower melting point than the constituents. Also, the eutectic point is a single temperature which phase changes from solid to liquid. Au-Si and Al-Si eutetics are used for calibration. The eutectic point of Au-Si is at 363 °C with 2.3 Si wt%. [84] The eutectic point of Al-Si is at 577 °C with 12.5 Si wt%. [85]

Fig. 2.4 is the Au-Si eutectic. The inset shows a Si chip wrapped with a Au wire on a sample holder. The sample is mounted on the manipulator in the UHV chamber. The laser pointer on the pyrometer assists us to focus the pyrometer to a sample surface with a correct working distance at a right angle, while monitoring a sample with a CCD camera as shown in Fig. 2.4. The temperature of a sample is controlled by a DH power supply in Fig. 2.9 to run a current through the Si chip. 0.05 A of the current is applied through a chip in Fig. 2.4(a). As the temperature slowly increases with an increasing current, the phase transition from a solid to the eutectic point is visible in Fig. 2.4. The DH current in Fig. 2.4(b) is, then at 0.16 A. In order to observe this transition, because of the native oxide and mixing between Au and Si, careful thermal cycles slightly below and above the eutectic point are required. After a few cycles near the eutectic point, the phase transition from Fig. 2.4(a) to (b) becomes a single point in the DH current. The temperature of the sample surface is measured using the pyrometer while adjusting the emissivity. The calibrated emissivity for Au-Si eutectic is 0.25, which is a similar to Ref. [1] assuming some loss from a glass window on the chamber. The Al-Si eutectic in Fig. 2.4 (c) and (d) is also used as a reference point at 577 °C. 500 nm of Al is deposited on a Si(100) chip in the inset of Fig. 2.4(c). Then, the sample is heated and cooled

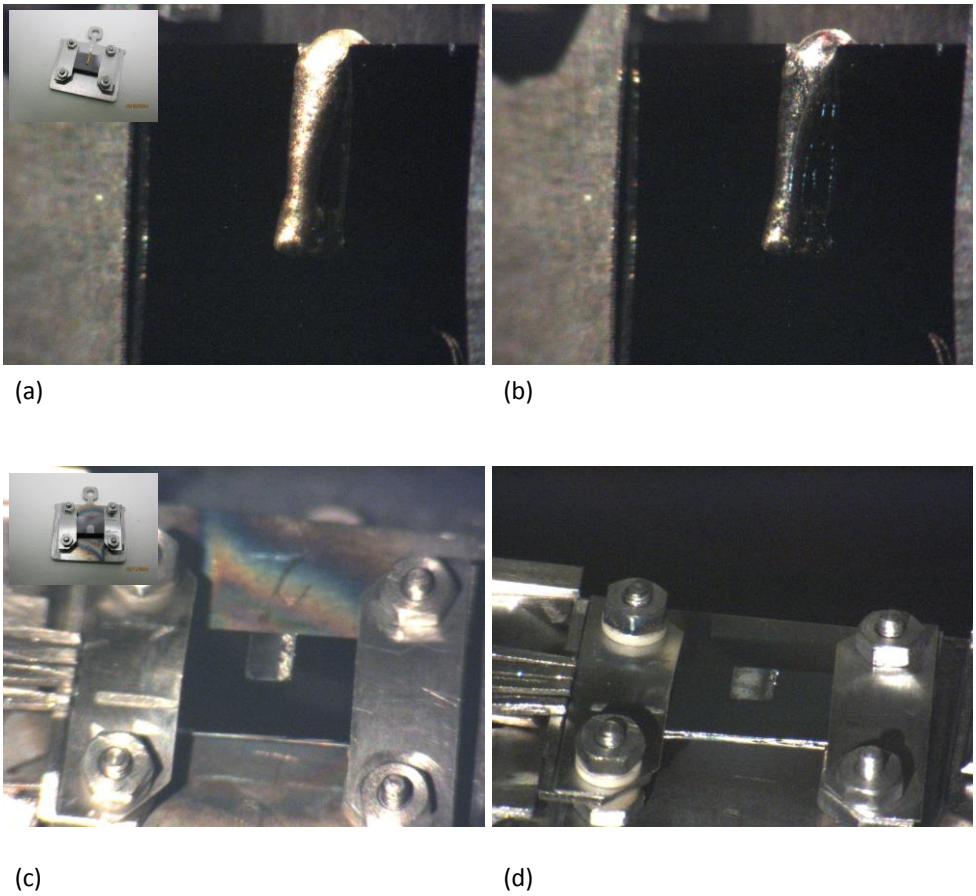

Fig. 2.4: The inset in (a) is a picture of Si(100) chip with a gold wire mounted on a sample holder. (a) and (b) are the Au-Si eutectic sample. (a) This is taken below the eutectic point. 0.05 A of current is running through a Si chip. (b) The phase transition at the eutectic point is visible on the Au wire surface. 0.16 A is running through the Si chip. The temperature is measured on a spot near the Au wire where Au is diffused into the Si chip using a pyrometer while calibrating the emissivity to read 363 °C. The calibrated emissivity at Au-Si eutectic point is 0.25. (c) and (d) shows the emissivity calibration procedure using the Al-Si eutectic sample. The inset in (c) shows a Si chip with 500 nm thick Al(gray square near the bottom edge of the Si chip) mounted on a sample holder. (c) This is after a first melt at 0.35 A. Then, it went through the melting and cooling cycles to make the Ai-Si eutectic near the edge of the deposited Al area. (d) This is taken after the test at room temperature. The calibrated emissivity with Al-Si eutectic point at 577 °C is 0.42.

by a DH power supply while monitoring with a CCD camera. The phase transition around the eutectic point is also observed with same procedure as the Au-Si eutectic. Fig. 2.4(c) is taken after Al is melted for the first time at 0.35 A. Fig. 2.4(d) is taken after a few cycles of melting. The calibrated emissivity with the Al-Si eutectic point is 0.42 at 577 °C. Above ≈ 800 °C, the emissivity is 0.68. [1].

2.2 Scanning Tunneling Microscope (STM)

In this work, I extensively used the scanning tunneling microscope a topographic tool to study the surface quality such as defects, impurities, roughness, and etc., and as a spectroscopic tool to measure $I(V)$ characteristics at the surface, and as a lithographic tool using a hydrogen masking. Scanning tunneling microscope has been widely used as a topographic instrument with atomic resolution. When a metal tip and a conducting or semiconducting sample are separated within a couple of nanometers and bias is applied between them, the tunneling current, I, is measured as a feedback signal. [86]

$$I_T \propto e^d \tag{2.1}$$

The exponential dependence of the tunneling current, I_T, to the tip-sample separation,d, gives the vertical and lateral sub-atomic resolution. To first order, the STM topography is a sample topography. However, as shown, [86]

$$I_T \propto \int_{-\infty}^{\infty} \rho_t(E - eV_T)\rho_s(E)(f_t(E - eV_T) - f_s(E))|M(E - eV_T, E)|^2 dE \tag{2.2}$$

The tunneling current, I_T, depend on the density of states of a sample, ρ_s,

and the tunneling matrix element, $|M|^2$. $f(E)$ is the Fermi-Dirac distribution for the electrons. The tunneling current depends on the local density of states of the sample assuming that the metal tip has a relatively constant local density of states within a bias window. In the one dimensional case, the tunneling matrix element can be simplified as:

$$|M(E - eV_T, E)|^2 = exp[-2d\sqrt{\frac{m_e}{\hbar}(\Phi_t + \Phi_s + eV_T - 2E)}] \tag{2.3}$$

m_e is the electron mass; Φ_t is the workfunction of the tip; Φ_s is the workfunction of the sample; V_T is the applied voltage; E is the energy with respect to the fermi energy. Also, in a more realistic case, the tunneling matrix can be very complicated depending on the actual geometry and wavefunctions of atoms at the tip apex and the sample, etc,. However, J. Tersoff and D. R. Hamann showed that for an atomically sharp tip the tunneling current matrix element depends on the position of the atom at the tip apex and the atom on the surface. [87–89] Also, at low bias conditions, the workfunction of a tip and a sample are much larger than V_T. Therefore, the tunneling matrix, M, can be assumed to be constant within the bias window.

Unlike AFM, the STM topography is affected by the local electronic properites. However, the advantage of STM is that STM can also measure the local electronic properties of a sample surface with atomic resolution.

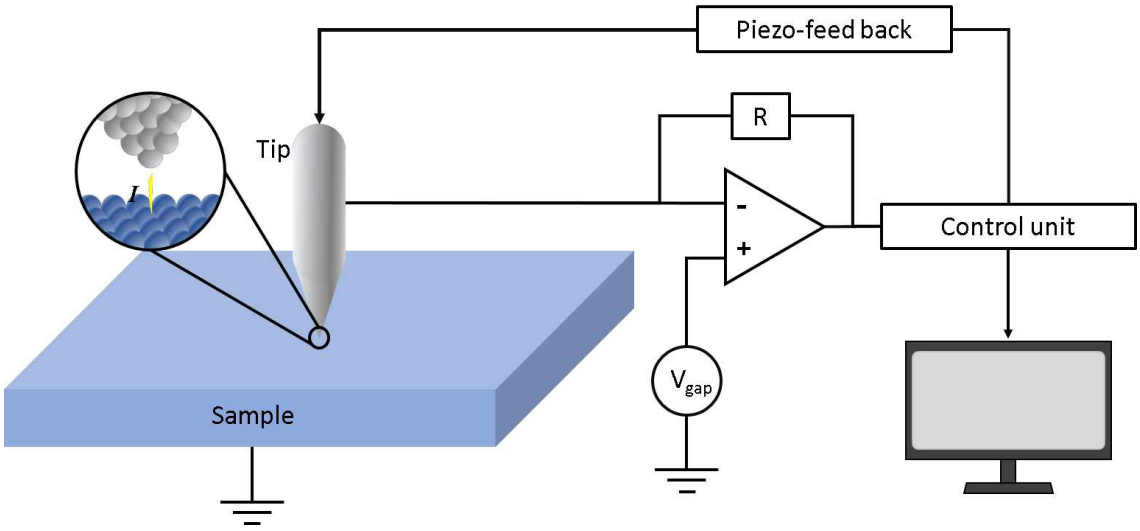

Fig. 2.5: This is the schematic drawing of STM. When a tip-sample separation is within 2-3 nm and a DC bias, V_{gap}, is applied to a tip in my STM, the tunneling, I, is measured and amplified. In this work, STM topography is taken at the constant tunneling current mode. Therefore, during STM topography scanning, in order to maintain a constant tunneling current, the tip-sample separation is controlled by the piezo-feedback, which gives topography of the sample.

2.2.1 STM Topography

As shown in the figure 2.5, STM measures the topography of conducting or semiconducting samples with atomic resolution using a tunneling current between a few atoms of the metal tip and atoms on the sample surface.

Typically, when the tip-sample separation is less than 2-3 nm and DC bias, V_T is applied to a tip or a sample, the tunneling current can flow between a few atoms at the tip apex and atoms on the sample surface. The tunneling current is amplified by a current amplifier and compared to the set-point value. For the constant tunneling current mode, a vertical and lateral motion of the tip by piezoelectric transducers keep a constant tunneling current during scanning and give topography of the sample. The piezoelectric transducers control three-dimensional motion of

the tip, which is recorded as topography of the sample. Since the tunneling current exponentially depends on the tunneling gap, which is a tip-sample separation for STM as shown in Eq. 2.1, STM can image the topography vertially and laterally with atomic resolution. However, since the tunneling current also corresponds to the local density of states of surface atoms and the tunneling matrix element, the STM topography is not exact physical topography. It is rather the constant tunneling probability. As shown in Eq. 2.2, the tunneling current integrates the local density of states of the sample over the energy between $E_F \leq E \leq E_F + eV_T$. Therefore, the STM topography depends on the V_{gap} since the surface states of the sample changes as V_T changes. The interpretation of STM topography needs to take account the electrical properties of surface atoms. This may sounds disadvantageous, however, this aspect of STM actually gives advantages to use STM for a spectroscopy and atom manipulation. Also, the change of the surface states of the sample as a function of V_T is slow at constant V_{gap} compared to d.

2.2.2 Scanning tunneling spectroscopy(STS)

As briefly mentioned on a previous section, the STM can be used as a various spectroscopic tool. The particular spectroscopic mode with the STM that we interested in scanning tunneling spectroscopy (STS). [90] STS measures $I(V)$ characteristics at given points on the surface. Based on Eq. 2.2, the tunneling current integrates the local density of states of the tip, the sample, and the tunneling matrix element within a bias window.

The first derivative of the Eq. 2.2 with respect to the bias, V

$$\left.\frac{\partial I_T}{\partial V}\right|_{V_T} \propto \int_{-\infty}^{\infty} dE[-\rho_s(E)\rho_t'(E-eV_T)f_t(E-eV_T) - \rho_s(E)\rho_t(E-eV_T)f_t'(E-eV_T) + \rho_s(E)\rho_t'(E-eV_T)f_t(E-eV_T)f_s(E)] \tag{2.4}$$

Assuming constant ρ_t and zero temperature for f', Eq. 2.4 can be simplified:

$$\left.\frac{\partial I_T}{\partial V}\right|_{V_T} \propto \int_{-\infty}^{\infty} dE[-\rho_s(E)\rho_t(E-eV_T)\delta(E-eV_T)] = \rho_t\rho_s(eV_T) \tag{2.5}$$

Therefore, the first derivative of I_T is proportional to the local density of states of the sample at V_T.

Using Eq. 2.5, $I(V)$ spectroscopy at a fixed position with STM can measure the local density of states with atomic resolution. However, since the tunneling current exponentially depends on the separation between a tip and a sample, when measuring $I(V)$, once the tip reaches at a desirable position with a given V_T and I_T, the feedback loop is turned off to fix the separation. Then, the voltage is swept while measuring I_T. Then, by numerically taking $\frac{dI}{dV}$, the local density of states of the sample can be obtained. In order to map the density of states for a large area, this method takes long time. For area of 10 nm $\times$ 10 nm, taking the topography and spectroscopy can take more than several hours. While the tip is scanning the area, in order to obtain $I(V)$ at each point, the feedback loop needs to be turned off and the voltage is swept for the entire area, which is time consuming. Longer the surface is exposed to the environment, more contaminants will be accumulated on the surface.

Therefore, another way to measure the density of states is to use the DC bias mixed with sinusoidal modulation voltage, which allows to measure the $\frac{dI}{dV}$ at a fixed voltage. [91] This allow us to measure the density of states of $\frac{\partial I_T}{\partial V}\big|_{V_T}$ simultaneously with the topography. The modulation technique can significantly reduce the measurement time, which is one of the most important factors to minimize for the subrface to exposed to the absorbates. In order to measure $\frac{\partial I_T}{\partial V}\big|_{V_T}$ with high signal to noise ratio, the lock-in technique is used as shown in Fig. 2.6. However, the density of states at the different energies needs to be scanned separately with different V_T.

As depicted in Fig. 2.6, $\tilde{V}_{AC} = V_{AC}sin(\omega t)$ is applied on top of the DC bias where V_{AC} is rms AC bias at frequency ω. Therefore, $V_T = V_{DC} + \tilde{V}_{AC}sin(\omega t)$.

$$I_T(V_{DC}+V_{AC}sin(\omega t)) = I_T(V_{DC})+V_{AC}\left.\frac{\partial I_T}{\partial V}\right|_{V_{DC}} sin(\omega t)+\frac{V_{AC}^2}{2}\left.\frac{\partial^2 I_T}{\partial V^2}\right|_{V_{DC}}+\cdots \quad (2.6)$$

The lock-in amplifier detects the signal at the reference frequency of ω. For the first harmonic, it measures the amplitude of the $sin(\omega t)$ term, which is proportional to $\frac{\partial I_T}{\partial V}\big|_{V_{DC}}$ in Eq. 2.6. While sweeping V_{DC} for $I(V)$, the lock-in signal, $\frac{\partial I_T}{\partial V}\big|_{V_{DC}}$, can be simultaneously measured.

Using this lock-in technique, I also measure the $\frac{\partial I_T}{\partial V}\big|_{V_{DC}}$ map simultaneously with measuring topography at given V_{DC} and I_{set} as shown red squares in Fig. 2.6.

The procedure to set-up the lock-in amplifier is as follow:

1. The STM tip approaches to the sample while monitoring the distance between the tip and the sample using a CCD and high magnification lens.

2. When the STM tip is close to the sample surface, using the "autoapproach"

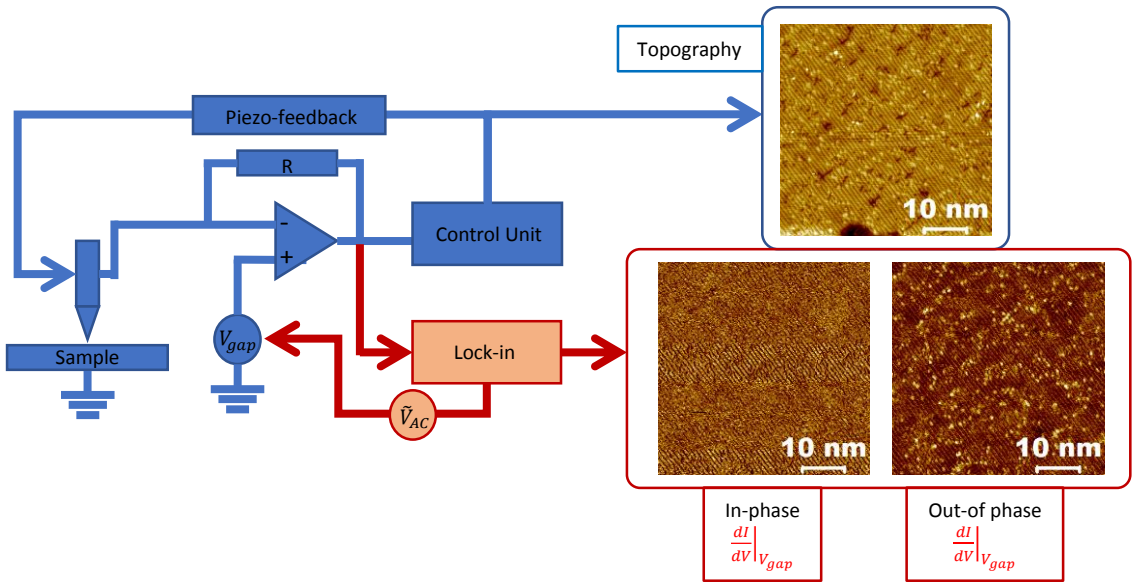

Fig. 2.6: The blue lines and rectangle represent the set-up for STM topography same as Fig. 2.5. In order to measure the $\frac{dI}{dV}$ at a V_{gap} with lock-in amplifier, the V_{AC} is mixed with V_{gap} which is a dc bias. This enables me to obtain $\frac{dI}{dV}$ map at a given V_{gap} simultaneously while measuring topgraphy as well as $\frac{dI}{dV}$ spectra with $I(V)$ spectra at a fixed point.The topography in a blue square is Si(100) surface with surface defects. The in-phase and out-of phase images in red squares in this figure are measured at frequency of 80 kHz and $V_{rms} = 50$ mV. Especially, out-of phase image shows the various local density of states of different surface defects.

function, the STM tip detects the surface at a given V_{gap} and I_{set}.

3. Then, retract the tip two coarse steps (≈ 2 μm) using a STM tip controller. Make sure that there is no tunneling current.

4. Mix the AC signal to the STM DC bias from the lock-in amplifier.

5. Set the phase using autophase function on the lock-in amplifier.

6. Give 90 ° phase shift to maximize the imaginary or Y part.

7. Start the "autoapproach" to the surface.

2.2.3 STM lithography

J. Lyding *et al.* first demonstrated STM lithography technique in UHV to be fabricated with H:Si(100). [30] STM lithography enables atomically precise devices such as a single atom transistor, nanowires, and single electron transistors. [31–34] Later, T. C. Shen showed two distinct desorption mechanism as a result of bias conditions and the electron dosage. [92] In the low bias condition lower than 6.5 V, the multiple-electron vibrational heating mechanism causes depassivation to break Si-H bonds. The low energy electrons from a tunneling current repeatedly excited the Si-H bonds which cause depassivation. Meanwhile, at high bias condition $>$ 6.5 V, the Si-H bonds can be excited from the σ bonding state to the σ^* antibonding state to break Si-H bonds.

The two desorption mechanisms result in two different patterning modes called fine mode (low bias) and field emission mode (high bias) in Fig. 2.7(a) and (b),

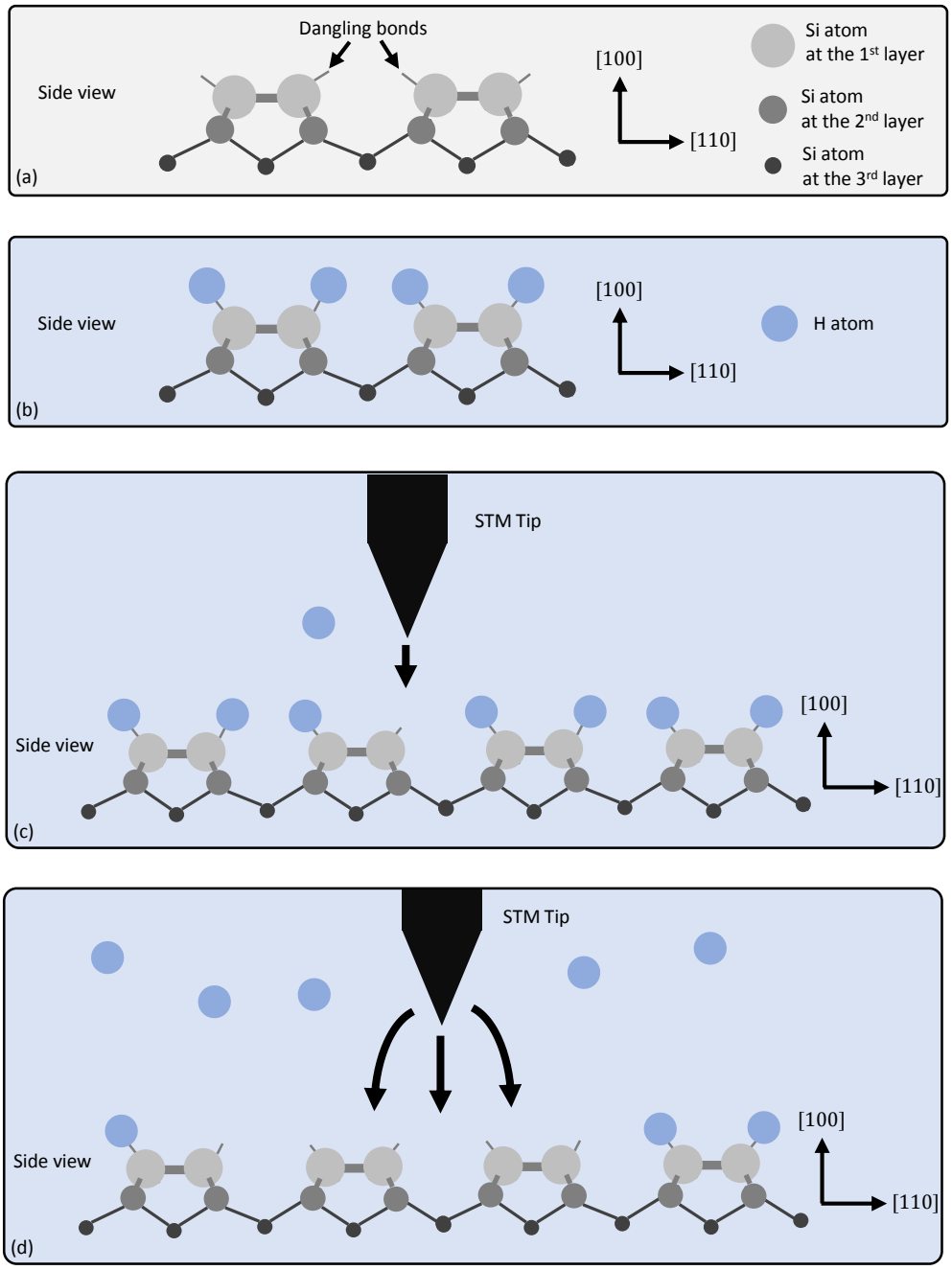

Fig. 2.7: This is a schematic drawing of STM lithography procedure. (a) and (b) are hydrogen passivation steps described in Fig. 2.26. (c) This is a schematic drawing for a fine mode at low bias condition. In this mode, a single H atom can be selectively removed. (d) This is a field emission mode at high bias condition. The tip is further away from the surface. The field emission from a tip to the surface can depassivate a larger area.

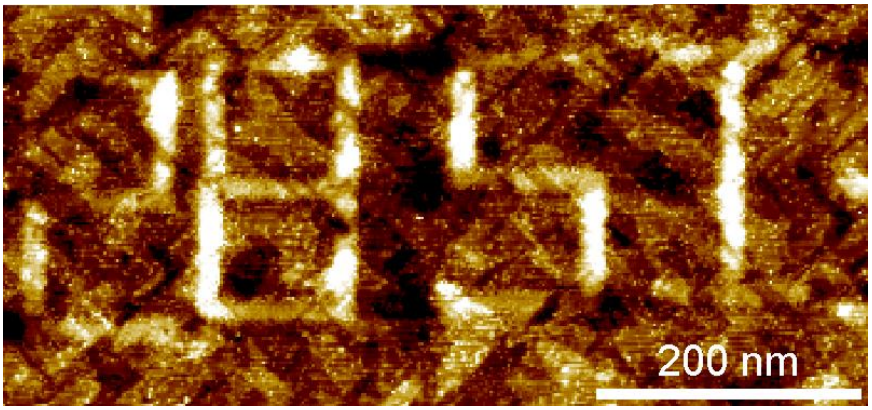

Fig. 2.8: This is a STM image of "28SI" patterned by STM lithography on the hydrogen passivated 28 enriched Si(100) epilayer.

respectively. The high bias can depassivate a large area with a faster speed because of the large separation between a tip and a sample and a field emission from a tip at high voltage. Typically, the linewidth of high bias patterning is between 10 to 15 nm. [93] However, the edge of the patterns are not very sharp. The field emission at large separation causes some depassivation outside of the intended patterning regions. However, some features of devices do not require sharp edges such as large contact pads and electrodes.

The low bias patterning has the advantage of atomic resolution, which allows the STM to desorb a single hydrogen atom at a time. Since the low bias patterning is due to multiple electron vibrational heating, the electron dosage is an important parameter, which can be controlled by the tunneling current and the scanning speed. [30, 94] Similar to the electron beam lithography, the STM lithography also has been characterized with the electron dose, especially for the low bias patterning in

Ref. [94], which uses the following equation.

$$\frac{Q}{L} = \frac{I \times t}{v \times t} = I/v \tag{2.7}$$

I is the tunneling current. v is the patterning speed of a STM tip. L is the length of the pattern. The typical electron dosage for low bias patterning is between 10^{-3} to $10^{-}2$ C/cm, which means high tunneling current of a few nA and slow scanning speed approximately tens of nm/second. [94] The patterning speed is very slow and time consuming. Despite of the UHV condition, any molecule in the vacuum chamber will stick to the surface. Since the cleanness is the key factor for device performance, the shorter lithography time is crucial. Therefore, the low bias patterning is used a fine feature requiring atomical precision.

2.3 Sample preparation

2.3.1 *ex situ* preparation

The cleanness of the chamber and samples during the whole fabrication process is the most important aspect of any experiment in this dissertation. The sample preparation before being introduced to the vacuum chamber is also as important as the vacuum condition. The various types of Si(100) substrates have been used in this work such as n-type(P doped), p-type(B doped), and intrinsic(10 kΩ·cm and 20 kΩ·cm).

The *ex situ* preparation is a cleaning process from dicing until introduction to the load lock chamber. First, a wafer is spin coated with a photoresist layer

before dicing into 4 mm by 10 mm chips to protect the surface from dust during dicing. Each 4 mm by 10 mm chip is cleaned by complementary-metal-oxide-semiconductor(CMOS) technology to remove organic and metal contamination and provide a thin chemical oxide layer to protect the surface from contamination until *in situ* cleaning. Ref. [95] showed that the chemically grown SiO_2 layer protects the surface from contamination compared to a hydrogen passivated surface. Our cleaning procedure is carefully desinged to remove the organic and metal contaminants and finish with the chemically grown SiO_2 layer to protect the surface while transporting a sample from a cleanroom after the last step of cleaning procedure to the vacuum chamber. The cleaning process consists of a piranha etch, HF etch, down stream asher, and Stanard Clean 2(SC2) in a cleanroom.

The detail cleaning steps are as follow:

1. Photoresist remover for 5 minutes.
2. Isopropanol rinse for 30 seconds.
3. Deionized water rinse.
4. Downstream asher.
5. Piranha etch: 6:1 H_2SO_4:H_2O_2 for 12 minutes
6. Deionize water rinse.
7. 50:1 H_2O:HF for 10 seconds.
8. Deionize water rinse.

9. SC-2: 5:1:1 H_2O:HCl:H_2O_2 at 80 °C for 12 minutes.

10. Deionized water rinse.

11. N_2 blow dry.

Typically, the sample is loaded to the load lock about 1 hour after the last step of cleaning procedure, the N_2 blow dry. The 1 hour is time for samples to be mounted on a sample holder, which is made of molybdenum. It is important to minimize the time between the last step of cleaning and being loaded to the vacuum chamber to reduce contamination on the surface.

2.3.2 *in situ* preparation

This *in situ* preparation is to remove the chemically grown oxide as a result of SC-2 cleaning and contamination on the surface, and prepare a clean (2×1) reconstructed Si(100). After *ex situ* cleaning procedure, ≈ 2 nm thick SiO_2 layer is chemically grown to protect the surface from the contamination until *in situ* cleaning. After the sample is loaded to the vacuum chamber, the SiO_2 layer needs to be thermally removed for further process such as Si overgrowth, Al deposition, and H passivation. In order to remove the SiO_2 layer in UHV chamber, high temperature annealing is required. [96] However, when the sample is annealed, the sample manipulator as shown in Fig. 2.9 also outgasses, which can contaminate the sample. Therefore, a lower temperature with shorter period is desirable.

After *in situ* cleaning, the sample is inspected by STM to ensure that the surface is a clean (2×1) reconstructed Si(100) with low surface defects and contam-

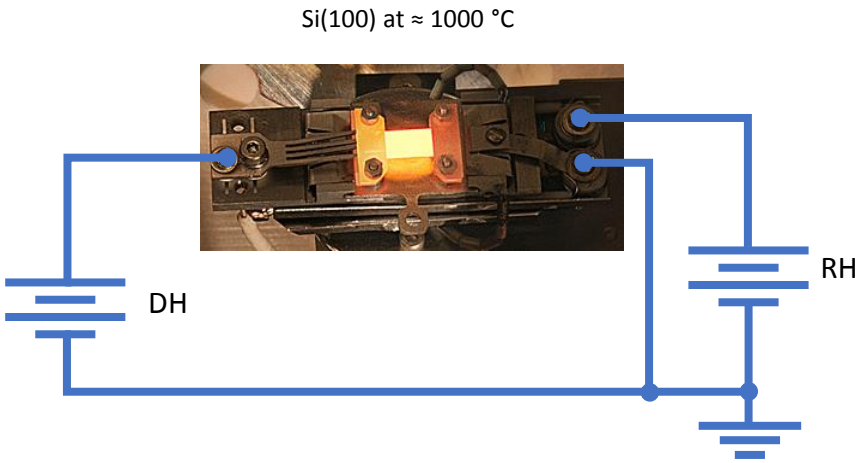

Fig. 2.9: The picture is a Si(100) substrate at 1000°C. The RH power supply is a power supply for a tungsten filament below the sample. The tungsten filament is used to degas the sample holder and a sample at ≈ 600 °C before high temperature flashing. The DH power supply is used to drive current through the sample for high temperature flashing.

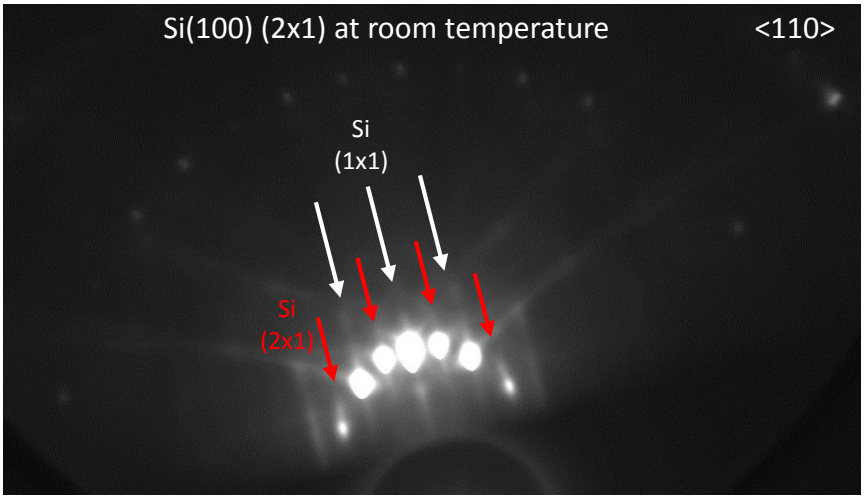

Fig. 2.10: This is a RHEED pattern of a clean (2×1)Si(100) substrate after 1200 °C flashing. The white arrows indicate the diffraction spots and (1×1) Si of bulk Si crystal. The red arrows indicate the (2×1) reconstructed Si(100) surface. This pattern was acquired with the substrate at room temperature and the electron beam in the <110> direction

ination. Occasionally, the sample is inspected by RHEED as shown in Fig. 2.10. Fig. 2.10 is acquired at room temperature with the electron beam in the $< 110 >$ direction. The long streaks with white arrows are diffraction from the bulk Si crystal. The shorter lines with red arrows between bulk streaks are due to the reconstructed (2×1) Si(100) surface. The semicircle of the spots is the zeroth Laue zone. The e-beam spot is about ≈ 0.25 mm^2. The long vertical streaks in patterns in Fig. 2.10 shows a flat surface.

We had histroy of C contamination during *in situ* preparation. The samples with SiC contamination were cleaned only by an HF etch before loading to the vacuum chamber in Fig. 3.7. The C contamination can be due to poor *ex situ* cleaning procedure with a HF etching as the last step, which results in better *ex situ* cleaning procedure in the previous section. [95] Also, some of studies show that SiC are formed around above 700 °C. [97]. Then, the other study shows that SiC are formed between 800 °C and 1000 °C. SiC starts to be decomposed above 1000 °C. [98] The previous studies suggest that the contaminants on the surface after *ex situ* cleaning procedure results the C contamination after *in situ* cleaning procedure. Therefore, our current *in situ* cleaning procedure uses the high temperature flash annealing around 1200 °C.

The high temperature SiO_2 removal procedure requires flash annealing procedures to heat the sample to the high temperature around 1200 °C for about 30 seconds in total. In order to keep the sample surface clean during *in situ* cleaning, the chamber pressure during annealing is kept under 1.0×10^{-9} Torr. Therefore, before high temperature flash annealing, the sample needs to be degassed at 600 °C

for typically longer than 16 hours using a hot tungsten filament below the sample on the manipulator and simultaneously running a current directly through the sample. After degassing, the tungsten filament is turned off. The temperature of the sample is set to 600 $^{\circ}C$ by the current running directly through the sample during flash annealing. The first step is to remove the native oxide layer from the *ex situ* cleaning of SC-2 by flash annealing at 1050 °C for 1 minute. When the chemically grown SiO_2 layer is thermally desorbed, the contamination on the surface is removed, which is similar to the lift-off process in commercial CMOS fabrication technology. The sample holder and other parts of the manipulator outgass at 1050 °C, therefore, the chamber pressure during further higher temperature flash annealing can be kept under 1.0×10^{-9} Torr. Between each high temperature flash annealing, the sample is kept at 600 °C. Then, the sample is flash annealed to 1150 °C for 15 seconds. Then, the sample is flash annealed 3 times to 1200 °C for 10 seconds. After the last 1200 °C anneal, the sample is rapidly cooled down to 800 °C. From 800 °C to room temperature, the sample is slowly cooled down at 1 °C/sec. The picture of a sample at 1000°C with wiring diagram is shown in Fig. 2.9.

A example of flash annealing procedure is as follow:

1. Degas at 600 °C for 16 hours with a hot tungsten filament and direct current heating.

2. Flash to 1050 °C for 1 minute then rapidly cool to 600 °C.

3. Flash to 1150 °C for 15 seconds then rapidly cool to 600 °C.

4. Flash to 1200 °C for 10 seconds then rapidly cool to 600 °C.

5. Flash to 1200 °C for 10 seconds then rapidly cool to 600 °C.

6. Flash to 1200 °C for 10 seconds then rapidly cool to 800 °C then slowly cool down by 1 °C/sec.

The *in situ* flash annealing at 1200 °C is widely used to achieve the clean (2×1)Si(100) surface. However, one of the limitations is to heat the other parts of the manipulator, which can introduce the chemical contamination from outgassing such as C, N, and O. Also, the flash annealing introduces the stress to the sample due to the high temperature process and rapid heating and cooling. The samples are often bowed after flash annealing, which makes the post fabrication process difficult. In order to lower the thermal budget for *in situ* SiO_2 removal, I explored two different SiO_2 removal processes which are similar to etching and lift-off. Both SiO_2 removal methods follow same deposition steps such as $SiO_2 + Si \rightarrow 2\ SiO$. [99–101] With the same decomposition process, I studied two different removal process which are similar to etching and lift-off. For the lift-off, I studied the temperature ranges such as ≈ 800 °C. For the etching, the SiO_2 layer is removed using Si deposition source at 700 °C. The goal of the low temperature SiO_2 removal tests is to remove the chemically grown SiO_2 and achieve a clean (2×1)Si(100) surface with no surface defects and chemical contaminants. In the next section, the detail procedures and the results of two low temperature SiO_2 removal methods are presented.

SiO_2 removal by Si flux

As briefly introduced in the previous section, two methods to remove the SiO_2 layer are tested. For both methods, the SiO_2 needs to be decomposed to SiO, which is a gaseous form, by $SiO_2 + Si \rightarrow 2SiO$. The first lift-off method is similar to the high temperature flash annealing. For the lift-off method, the sample is annealed to ≈ 800 °C for a longer period of time of 20 minutes. The SiO_2 decomposition happens at the interface between the SiO_2 and the Si since the decomposition needs an additional Si atom. In case of SiO_2 decomposition at the higher temperature compared to the etching method, SiO formed at the interface diffuses through SiO_2 layer into the vacuum. [100, 102–105] In order for SiO to overcome the potential barrier of SiO_2, the lift-off method requires high temperature. However, by providing the flux of Si atoms on the SiO_2 surface SiO can be decomposed at the SiO_2 surface at lower temperature of 700 °C.

I used the e-beam evaporator for the Si flux as described in section 2.4.2. Then, the sample is heated to 700 °C. During this process, the surface is monitored by RHEED as shown in Fig. 2.11. The sample is cleaned by *ex situ* cleaning process as described in section. 2.3.1. Then, the surface has $\approx$ 2 to 3 nm of chemically grown SiO_2 layer. The sample is degassed at 600 °C for 17 hours. Fig. 2.11(a) is taken at 700 °C after being degassed. 600 °C is not a high enough temperature to decompose SiO_2 layer. [100, 102–105] While the surface temperature is held at 700 °C, the Si atoms are deposited at the rate of 1 ML/min. Ref. [96] shows that if the deposition rate is too high at a given temperature, the Si atoms on the surface can

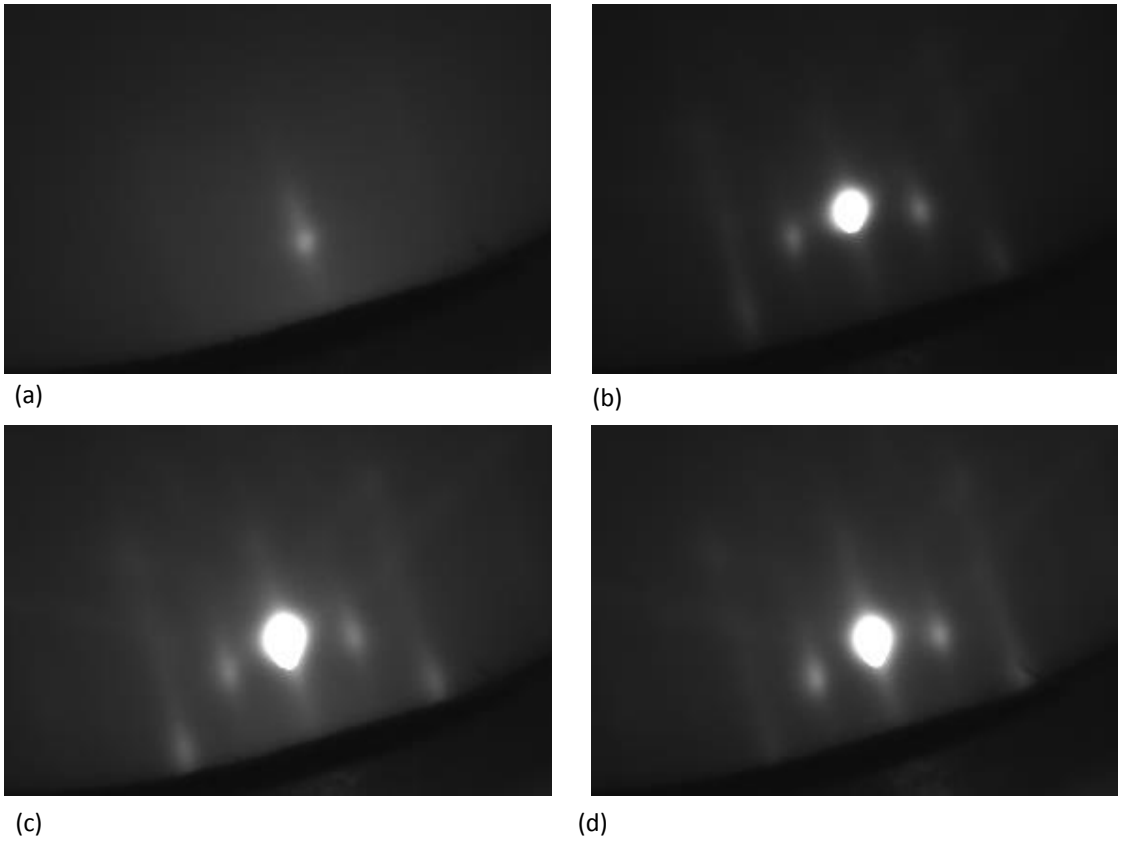

Fig. 2.11: (a) This is taken at 700 °C after degass for 17 hours at 600°C. The long streaks from (1×1) Si(100) are barely visible because of SiO_2 layer. (b) The sample is held at 700 °C. Then, ≈ 1.36 nm of Si is deposited at the rate of 1 ML/min. The faint short lines from (2×1) Si(100) dimers between long streaks starts to appear. (c) The toal of ≈ 2.7 nm of Si is deposited at 700 °C at the deposition rate of 1 ML/min. The short (2×1) lines becomes brighter. (d) Total of ≈ 4 nm of Si is deposited at 700 °C. (d) looks similar to (c). The chemically grown SiO_2 is typically 2∼3 nm thick. After the deposition of ≈ 4 nm Si, the SiO_2 layer must be removed.

accumulate as measured by AES. The deposition rate and the surface temperature are determined by Ref. [96]. Fig 2.11(b) is taken after deposition of ≈ 1.36 nm of Si. The long bright streaks from (1×1) Si are visible. Also, the short lines between long streaks from (2×1) Si(100) dimer rows starts to appear. Fig. 2.11(c) is taken after the deposition of ≈ 2.7 nm of Si. The long streaks are clearly visible. The (2×1) lines are well developed indicating that most of the SiO_2 is removed. Fig.

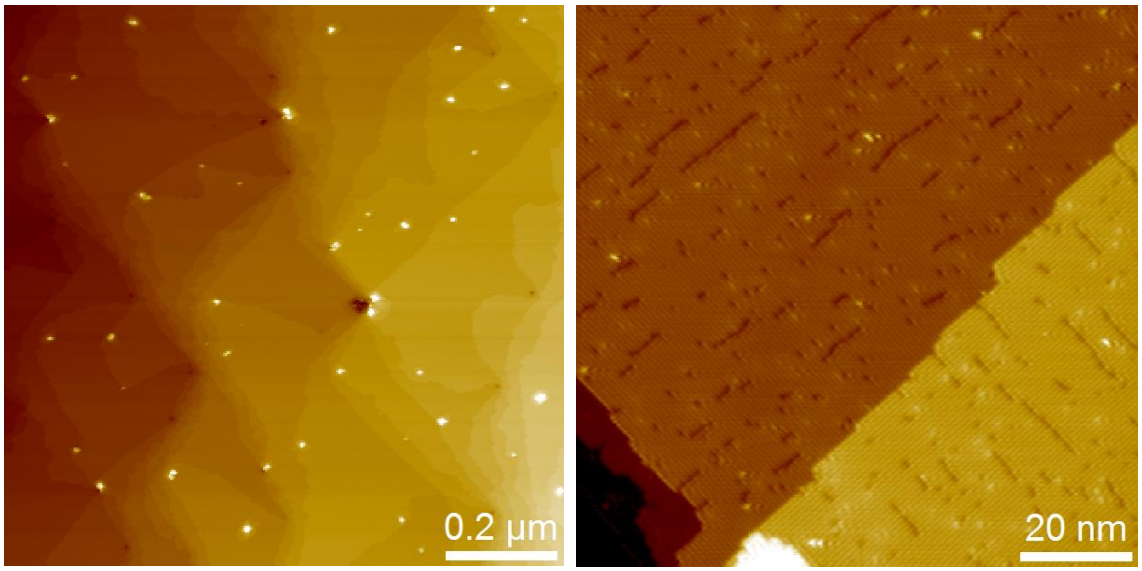

Fig. 2.12: This samples is cleaned with *ex situ* cleaning process as descripted in section 2.3.1. After being degassed at 600 °C for 17 hours, the sample is held at 700 °C while depositing ≈ 4 nm of Si at 700 °C at the rate of 1 ML/min. (a) and (b) are taken at $V_{tip} = 2.00V$ and $I_{set} = 150$ pA. (a) This is a large area (1 μm^2) scan. The bright pyramids are SiC. There are several pits which may be induced by chemical contaminants or strain. (b) This is a zoom-in image (100 nm × 100 nm). The dark lines on the surface are most likely metal contamination, which explained at section 3.3.1.

2.11(d) is taken after ≈ 4 nm of Si is deposited. This image is very similar to Fig. 2.11(c). After Fig. 2.11(d), the sample is moved to the STM chamber in Fig. 2.12.

Fig. 2.12 shows (2×1)Si(100) dimer rows. The entire SiO_2 layer seems to be removed. However, the pyramid shaped SiC are formed on the surface. Also, several pits on the surface are visible which are due to chemical contaminants or strain as discussed in section 3.3. Fig. 2.12(b) is a zoom-in image of (a). The high density of the dark lines due to metal contamination are visible. Also, the bright spot along the dimer rows indicates O, OH, H_2O, or other chemical contamination on the surface. With Si flux method, the surface temperature during SiO_2 removal can be reduced. However, STM images shows high density of chemical and metal

contamination on the surface. This method is similar to etching SiO_2 layer from the top. Therefore, while SiO_2 is removed with Si flux, the remaining contaminants while transporting a sample from a cleanroom to the vacuum chamber are left on the surface. These contaminants are not removed with SiO_2 layer. However, if C on the surface is removed before SiO_2 removal with Si flux, this method may be possible. In the next section, I also tested a hydrogen cleaning to remove C and O after 600 °C degassing. [106, 107]

SiO_2 removal by thermal decomposition

As shown in Fig. 2.12, Si flux method to remove SiO_2 is not feasible. Therefore, I pursued removing the SiO_2 at higher temperatures such as 800 °C. The contamination while transporting a sample from a cleanroom to the vacuum chamber is not avoidable. As shown in Fig. 2.12(a), large amount of SiC pyramids are visible on the surface. This indicates that the absorbed C on the SiO_2 surface are left even after SiO_2 removal with Si flux. Therefore, I tested another cleaning step in the UHV chamber to remove C and O using atomic hydrogen after 600 °C degassing. [106, 107] As shown in section 2.4.4, the hydrogen gas manifold and a cracking filament are installed in the deposition chamber to create H^+ ions in the chamber. After 600 °C degassing for 18 hours, the sample is held at 600 °C. Then, the hydrogen gas is introduced to the chamber with a hot tungsten filament at $\approx$ 1000 °C to raise the background pressure to 5×10^{-6} Torr. The sample is exposed to the atomic H for 20 minutes. After atomic H cleaning, the leak valve is closed and the tungsten filament is turned off. Then, the sample is heated to 800 °C for 20

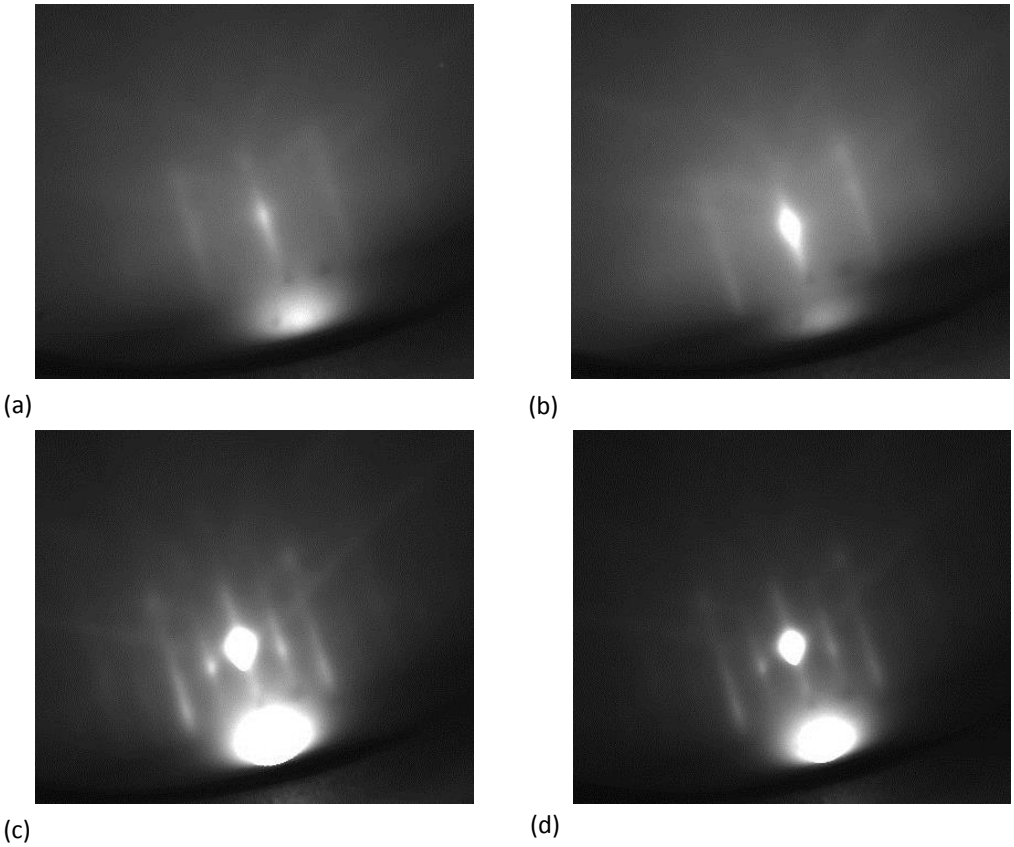

Fig. 2.13: (a) This is taken at 600 °C after 600 °C degassing for 18 hours. (b) After the atomic H cleaning for 20 minutes at the H pressure of 5×10^{-6} Torr. The sample temperature is 600 °C. After atomic H cleaning procedure, the sample is heated to 800 °C. (c) This is taken 7 minutes after being heated to 800 °C. The short lines for (2×1) Si(100) dimers between (1×1) streaks are visible. (d) After 17 minutes at 800 °C, the RHEED pattern is very similar to (c) with good (1×1) streaks and (2×1) lines.

minutes. During the whole process, the sample is monitored with RHEED in Fig. 2.13.

Fig. 2.13(a) is taken after 600 °C degassing. It shows (1×1) streaks from Si crystal structure. Fig. 2.13(b) is taken after atomic H cleaning. This is very similar to Fig. 2.13(a), which means that the SiO_2 layer is not removed. Fig. 2.13(c) is taken 7 minutes after the sample is heated to 800 °C. The short lines due to (2×1) Si(100) dimer rows between (1×1) streaks are visible. After 17 minutes, Fig. 2.13(d)

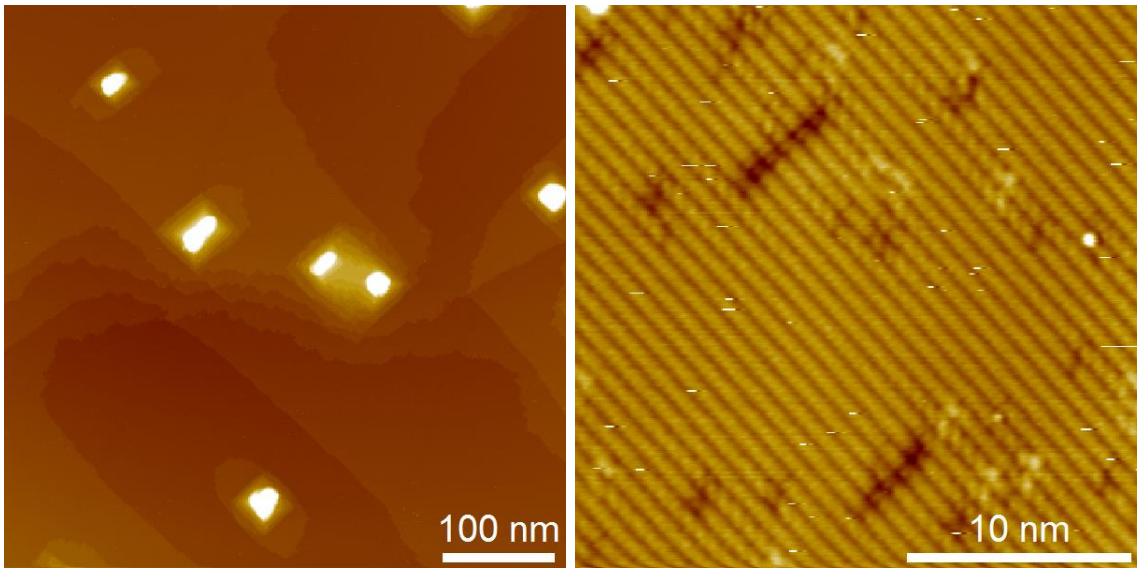

Fig. 2.14: Both images are taken at $V_{tip} = 2.00$ V and $I_{set} = 150$ pA. (a) This is a large area scan (500 nm $\times$ 500 nm). Similar to Fig. 2.12, there are SiC pyramids on the surface. (b) There are very short dark lines with lower density compared to Fig. 2.12(b). However, the dark lines indicating metal contamination still exist. The short one dimer long vacancy defects are also visible.

seems same as Fig. 2.13(c). After 20 minutes at 800 °C, the sample is moved to the STM chamber for inspection. This low temperature *in situ* process is similar to Ref. [95], which removed the SiO_2 layer at 900 °C.

Both of Fig. 2.14 are taken at $V_{tip} = 2.00$ V and $I_{set} = 150$ pA. Fig. 2.14(a) shows SiC pyramids on the surface. Fig. 2.14(b) shows dark lines indicating metal contamination. The density of metal contaminants in Fig. 2.14 is lower than in Fig. 2.12(b). There are also vacancy defects which are one or two dimers long. As shown in Fig. 2.14(b), the high density of buckled dimers with bright spots indicates H, OH or H_2O. The STM images indicate that 800 °C annealing does not clean the surface contaminants even though the SiO_2 layer is removed. However, we had history of having contamination in the H gas manifold since H_2 reacts with adsorbates on the

H gas manifold surface. With more careful cleaning of the H gas manifold, such as bake-out and pumping the manifold to high vacuum, the surface cleaning using H^+ ions can be improved to achieve a clean (2×1) Si(100) surface.

2.4 UHV Deposition

2.4.1 ^{28}Si Ion-beam Deposition

As well summerized in Ref. [20] by Zwanenburg, silicon is a very promising material for quantum information due to the weak spin-orbit coupling, zero nuclear spin of ^{28}Si, and the well established CMOS fabrication techniques. Si is also demonstrated to have long coherence times. [21, 22] However, natural abundance silicon consists of 4.7 % of ^{29}Si with spin-half nuclear spin, which is a noise source to spin qubits in Si. By removing the residual ^{29}Si, which is often referred as "semiconductor vacuum", coherence times has improved. [21, 22, 108] SIMS measurements for ^{28}Si, ^{29}Si, and ^{30}Si in Fig. 2.17 shows high enrichment levels up to 99.99987 %, which is the highest reported ^{28}Si enrichment. Our group has been fabricating highly enriched ^{28}Si using the hyperthermal energy ion beam deposition system as described in Fig. 2.15. [109, 110]

Natural abundance SiH_4 gas is introduced into the Penning ion source. Using a confinement magnet, cathodes, and anode, the SiH_4 gas is ionized. Ions in the Penning ion source are extracted by the extraction cusp. Then, the ions are transported through a series of electromagnetic lens, which is the red dashed line in Fig. 2.15. The mass/energy selecting magnet works as a mass spectrometer. The mass

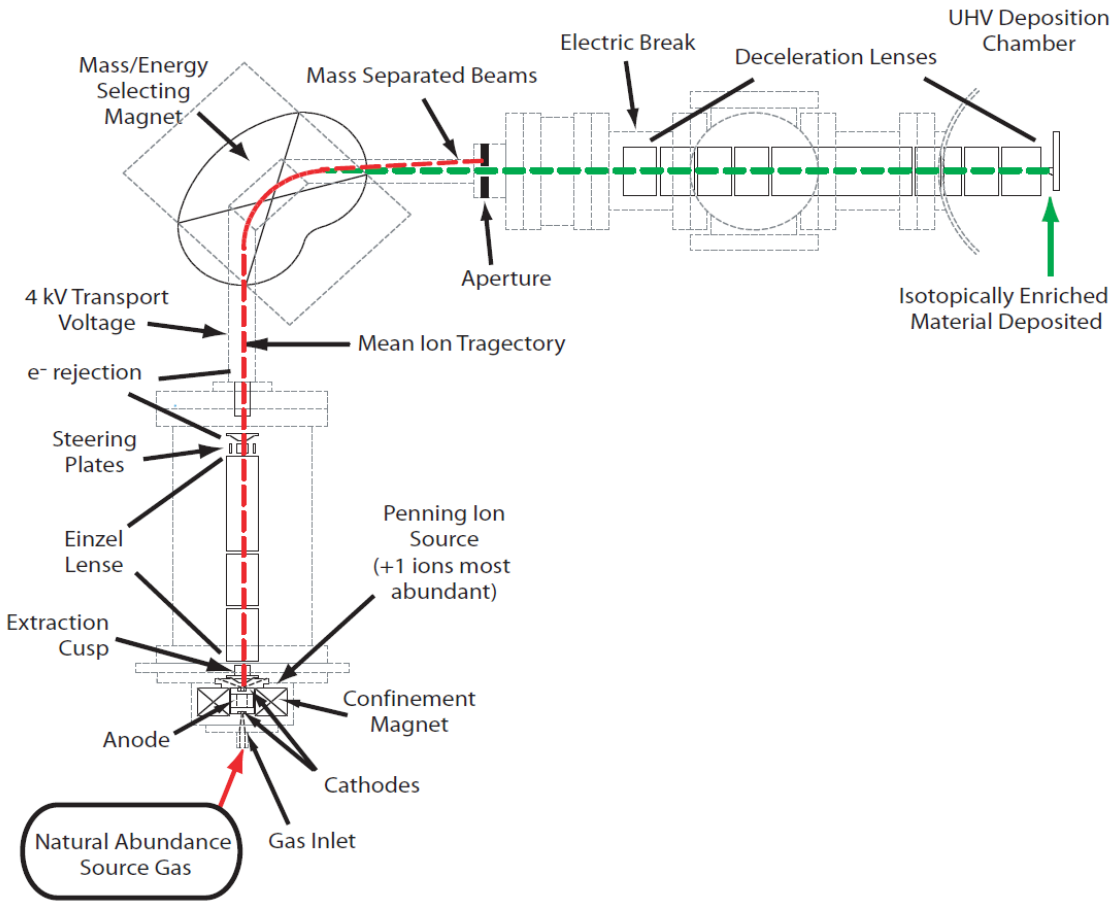

Fig. 2.15: This is a schematic drawing of the ion-beam deposition system. The natural abundance SiH_4 gas is introduced to the Penning ion source. The extracted ions are transported through the series of electromagnetic lens. These ions are bent by mass/energy electing magnet. This allows to selectively deposit ^{28}Si (dashed green line) through the aperture on the sample in the UHV deposition chamber. This is from Ref. [111]

spectrum of the ion beam system is in Fig. 2.16. The peaks at each mass from 28 up to 33 are well separated. Especially, the peaks at ^{28}Si and ^{29}Si are well separated by $\approx 11\ \sigma$. [109] The ^{28}Si beam (the green dashed line in Fig. 2.15) passes through the aperture. The ^{28}Si is deposited on the sample in the UHV deposition chamber.

Over the last several years of this project, the enrichment level has been improved as shown in Fig. 2.17. These ^{28}Si epilayers are grown by a previous group

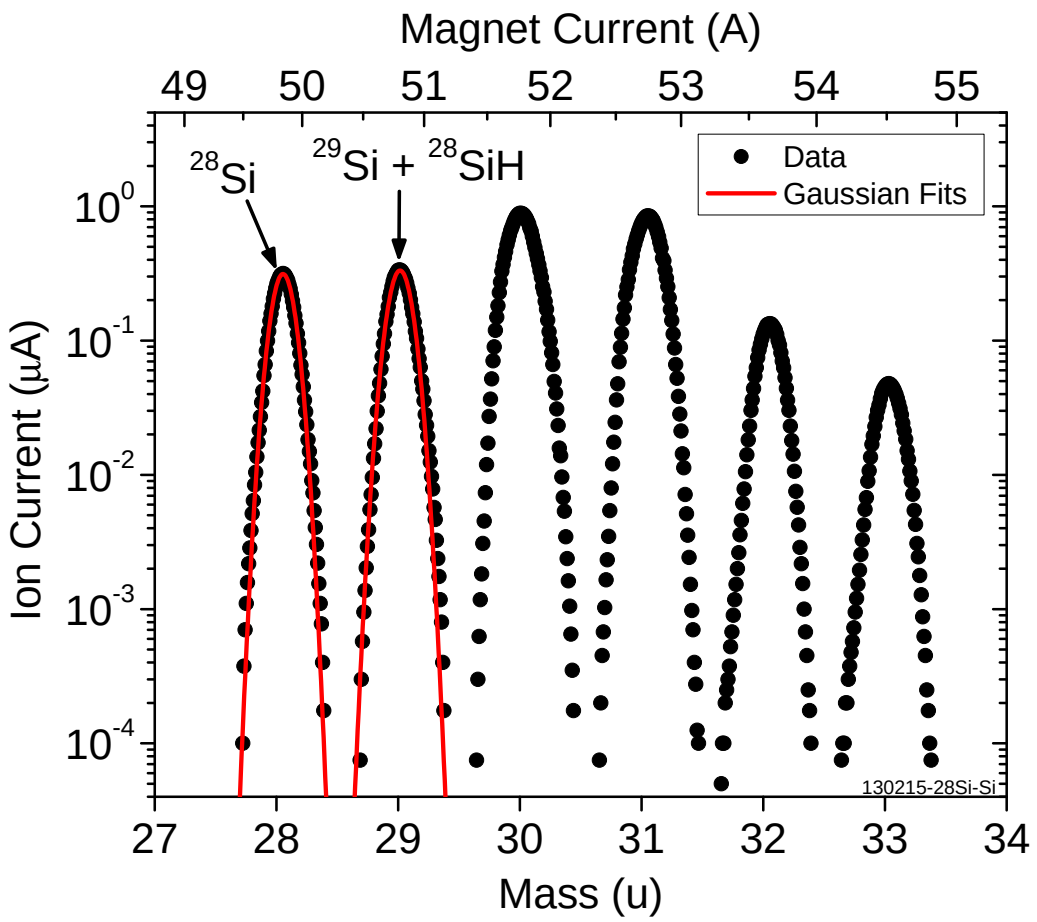

Fig. 2.16: Mass spectrum using the ion beam 28Si deposition system. The ion current is measured at the manipulator while sweeping the magnetic field of the mass selecting magnet in Fig. 2.15. The peak at mass 28 is ^{28}Si. Mass 29 is ^{29}Si and ^{28}SiH. The peaks at mass 28 and 29 are well separated by $\approx 11\ \sigma$. This figure is taken from a Ref. [109].

member, Dr. Kevin Dwyer and a current graduate student, Ke Tang from University of Maryland, College Park. The gray area in Fig. 2.17 is from the time before I joined the group. Since joining the group, I inspected every substrate and ^{28}Si epilayer with STM and some with RHEED. Also, I have improved the cleanness of the substrates, parts in the UHV deposition chamber, and implementing the UHV Penning ion source. The red dashed line in Fig. 2.17 represents when a new UHV compatible Penning ion deposition system. During the first experiments, the con-

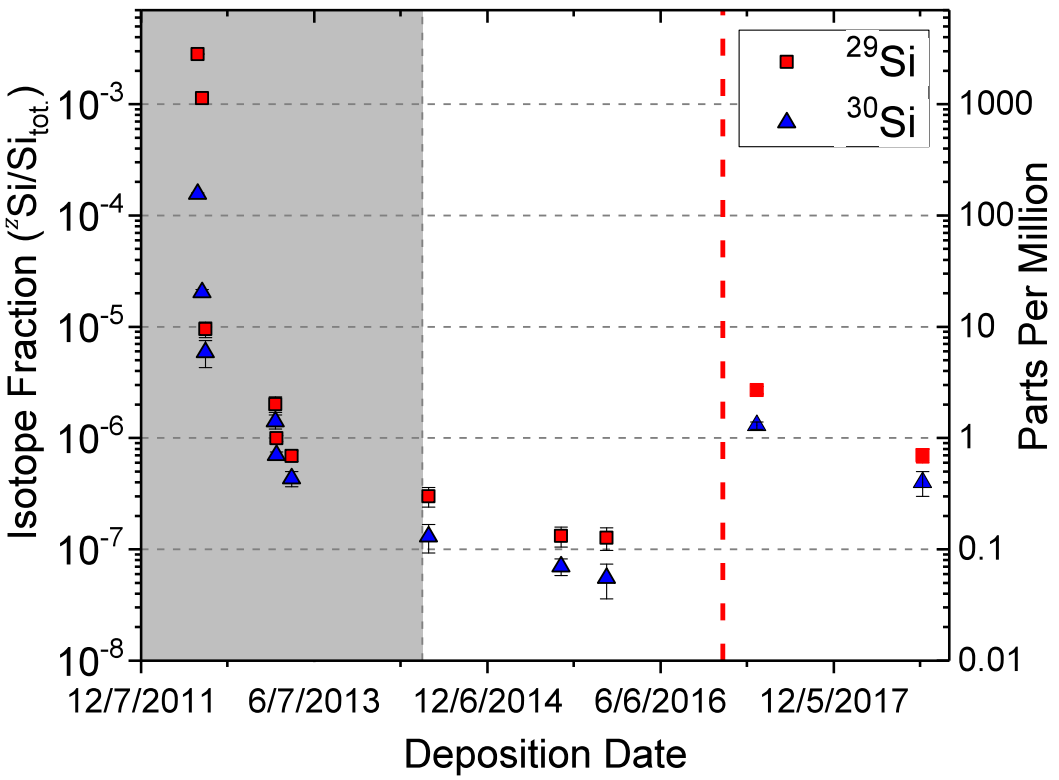

Fig. 2.17: This is a timeline of the ^{28}Si enrichment using the ion beam deposition system. The measurements within the gray shade are before joining the group. The red line represent the time when the new UHV ion beam deposition system is installed.

centration of ^{29}Si in the ^{28} enriched epilayer is increased compared to old Penning ion source. However, the enrichment level of ^{28}Si has been improving.

All ^{28}Si samples are inspected by STM before and after deposition. Fig. 2.18 are STM images taken after $\approx$ 204 nm thick ^{28}Si epilayer is grown at 450 °C. Fig. 2.18(a) is a large area (1 μm $\times$ 1μm). Compared to a Si epilayer in Fig. 3.12 grown by EFM, because of the higher deposition rate, the ^{28}Si epilayer forms smaller Si islands. Fig. 2.18(b) is a small area scan of 15 nm $\times$ 15 nm on one of Si islands. This shows a clean (2$\times$1) Si(100) dimer rows with very low density of defects.

Our UHV deposition system consist of an e-beam Si deposition source and

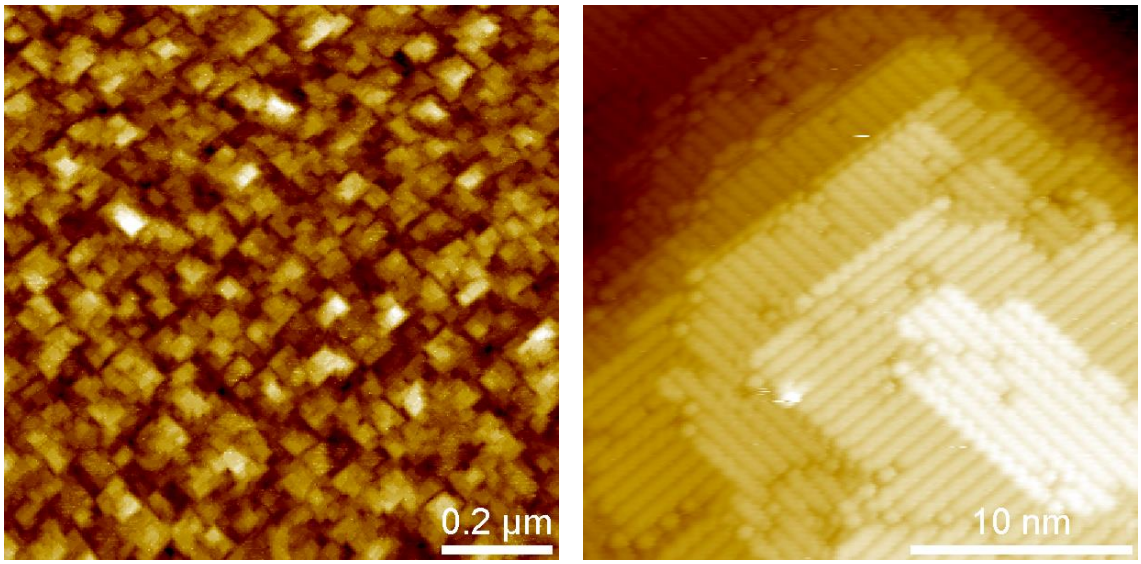

Fig. 2.18: ≈ 204 nm thick ^{28}Si epilayer grown at 450 °C Both images are taken at V_{tip} = 2.00 V and I_{set} = 150 pA. (a) This is a large scale STM image (1 μm × 1 μm). The height range from the highest peak to the lowest valley within this image is ≈ 3.6 nm. (b) This is a small scale image(15 nm × 15nm). This is one of the island with a very small amount of defects.

a ^{28}Si ion beam deposition source, which allow us to study the kinetics of two different types of Si deposition systems. Also, the ^{28}Si epilayer could be implanted with Si/Al/Si heterostructures, and *in situ* detection of pre-implanted patterns for STM lithography progress with e-beam Si deposition system as the work progresses to study silicon quantum devices.

2.4.2 Si(100) E-gun Deposition

The UHV deposition and analysis chamber is equipped with a Si thermal evaporator (EFM 3 from Omicron). This evaporator allows a Si evaporation source to be mounted without a crucible. A float-zone(FZ) i-Si(100) rod is mounted on a molybdenum adapter, which electrically and mechanically couple the Si(100) rod

to a stainless steel rod. As shown in 2.19, a high voltage is applied to the silicon source to attract an electron beam from a hot filament. Then, the evaporated Si ions are measured at the aperture of a evaporator to estimate a deposition rate. The actual deposition rate is calibrated by a quartz crystal microbalance(QCM), which can be moved to the same position as the Si(100) substrate by linear translator. Also, the deposition rate and the quality of the Si(100) epilayer are then checked using STM. On a clean Si(100), a sub-monolayer of Si(100) was deposited at room temperature. Then, the newly formed Si(100) islands on the surface wer measured by STM enabling us to estimate the deposition rate at given heating power of the EFM3. The maximum deposition rate for a i-Si(100) rod is 1/3 monolayer(ML)/min ($\approx$ 0.136 nm for 3 minutes). Since the FZ Si(100) rod is used for a evaporation source without a crucible, as the temperature of a Si(100) rod is near the melting point, the end of the rod is melted down.

A higher deposition rate is desirable to minimize the contamination from the background gas. Since the deposition rate is limited, the UHV chamber is one of the most important requirements to grow high quality Si(100) epilayer. Typical UHV chamber pressure is 2 $\times 10^{-11}$ Torr. During Si deposition, the FZ i-Si rod is the only part that is heated which minimize outgassing from the other parts of the evaporator. Also, the FZ i-Si rod is the highest quality silicon available in terms of chemical impurities and crystal quality.

A QCM is installed on a linear translator as shown in Fig. 2.20, which allows QCM to be moved to a position where a sample is located during deposition. The deposition rate is measured before and after Si deposition for good estimation of the

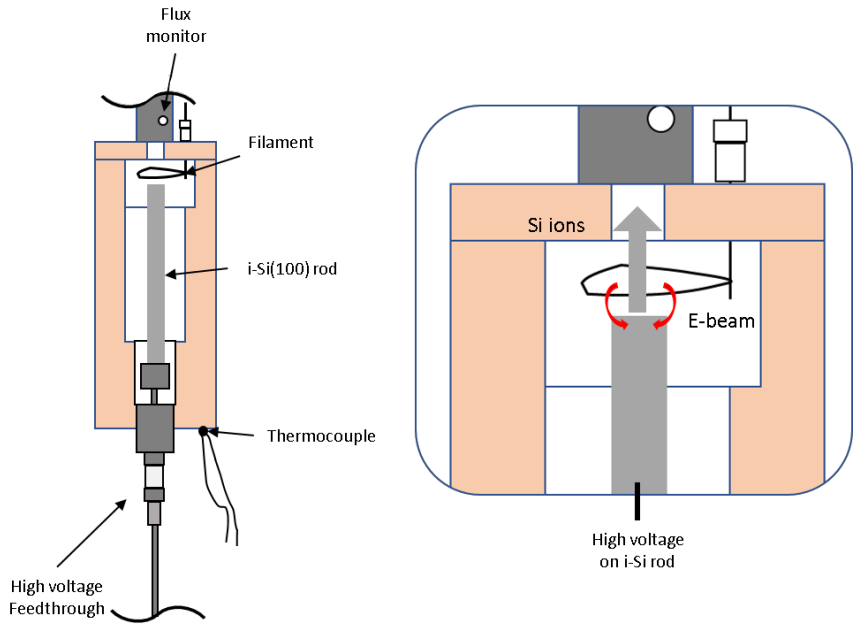

Fig. 2.19: This is a schematic drawing of a Si e-beam evaporator(EFM 3 from Omicron). Electrons from a hot tungsten filament are attracted to the end of a Si evaporation source(FZ i-Si rod) by a high voltage on thei rod. A flux of a Si ion beam current is measured at the aperture of the EFM 3 to estimate a deposition rate.

thickness of the deposited Si layer. Also, at the maximum deposition rate by the EFM, the sub monolayer of Si on the Si(100) substrate is deposited on the Si(100) substrate at the room temperature. Then, the sample after deposition is scanned by STM, which gives us another direct measure of the deposition rate. The deposition rate is checked regularly with STM as shown in Fig. 2.21. Fig. 2.21 shows small, clean Si(100) islands.

The maximum deposition rate of the EFM is 1 ML/min, which is checked by the QCM and the EFM. The STM images of $\approx$ 60 nm thick Si epilayer grown by the EFM at 450 °C at the deposition rate of 1 ML/min show a reasonably clean (2×1) reconstructed Si(100) with a small surface defects in Fig. 3.12.

In the next section, the aluminum deposition in the UHV deposition chamber

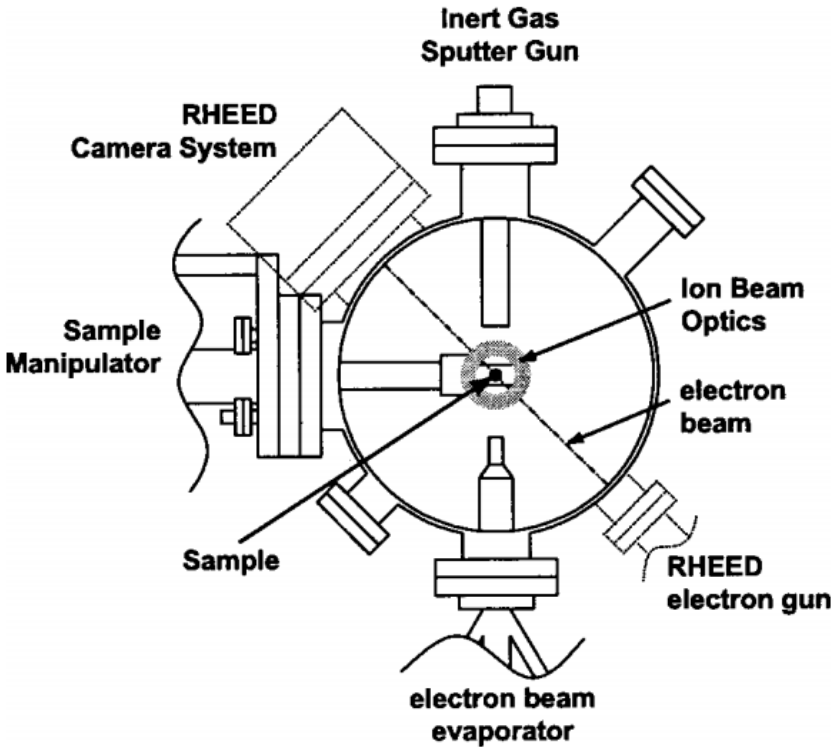

Fig. 2.20: This is a schematic of the EFM, a manipulator, and the QCM. The QCM is mounted on a linear translator, which allows the QCM to be moved to a position where the sample is located during deposition. This figure is taken from Ref. [111]

is discussed. The Al is deposited using a UHV commercial evaporation furnace. The deposition rate and the quality of the deposited Al are checked by the STM, which will be presented in the following section.

2.4.3 Aluminum Deposition

As shown in Fig. 2.1, the aluminum deposition is performed in the UHV deposition chamber. Initially, aluminum rods wrapped around a tungsten wire are mounted on a top of the manipulator. However, this caused Al auto-doping in Si epilayer measured by the secondary ion mass spectrometry(SIMS). In order to avoid auto-doping, the Al deposition source is moved a far from the manipulator where

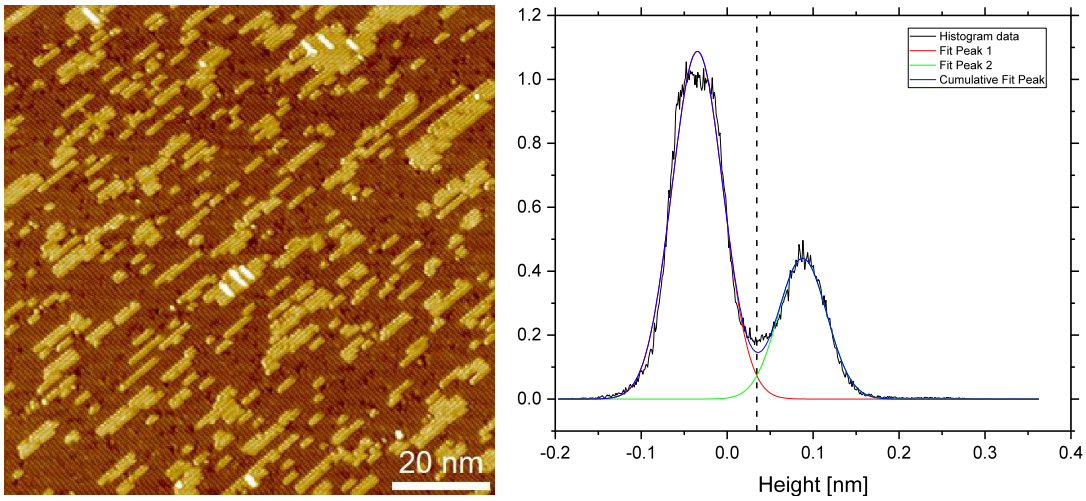

Fig. 2.21: This is a STM image taken after Si deposition with sub monolayer coverage which is estimated 0.25 ML (1 ML = 6.78×10^{14} cm^{-2}). STM is set to be V_{tip} = 1.90 V and I_{set} = 150 pA. The area coverage on a single terrace provides the deposition rate at a given EFM power for a deposition time. The figure on the right is the height histrogram of the STM image with two fitted gaussian curves. The first peak with a red fitted curveis for a lower terrace(the substrate). The second peak with a green fitted curve is for the second Si layer(the deposited Si). The intercepted point marked with a dashed line is used as a threshold of the height to estimate the area coverage of the new formed Si islands from deposition.

Si epilayers are deposited, as shown in Fig. 2.1. With this change of Al deposition source position in the chamber, Al atoms are no longer measured in Si epilayers by SIMS on multiple samples.

The Al deposition source is now a commercial evaporation furnace(Luxel Radak 1). Fig. 2.22 is a schematic of the set-up in a chamber. The furnace is mounted at the bottom of the small chamber. The shutter located at the top of the furnace is pneumatically controlled.

The Al source material such as small pellets is mounted inside a PBN liner. Then, PBN liner is mounted inside a alumina crucible. The stress on a liner and a crucible from a thermal expansion during cooling down Al source from above the

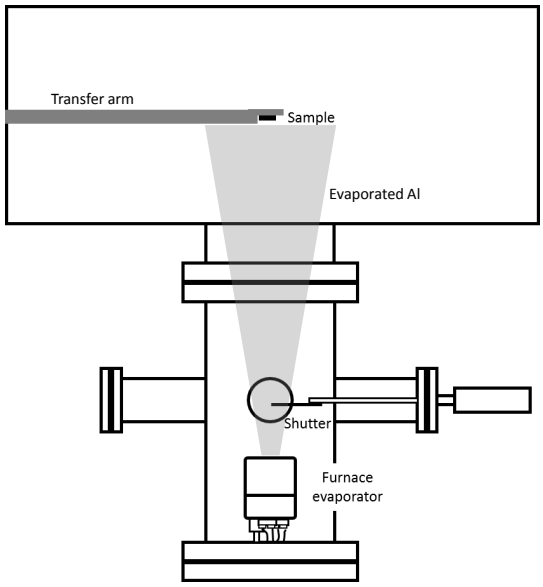

Fig. 2.22: This is a schematic drawing of the Al evaporation furnace(Luxel Radak 1) installed on the deposition chamber. During deposition, the sample is mounted on the transfer arm. The pneumatic shutter is mounted on top of the furnace.

melting point can break the crucible. To prevent the crucibles to be broken and the leakage of the melted Al through the crucible, the Al furnace is kept around at 860 °C which is above the melting point of Al, 660 °C.

The evaporation rate of Al is calculated by a Hertz-Knudsen equation. The Hertz-Knudsen equation describes the rate of sticking of molecules or atoms of the unit area.

$$\frac{1}{A}\frac{\mathrm{dN}}{\mathrm{dt}} = \frac{\alpha p N_A}{\sqrt{2\pi MRT}} \tag{2.8}$$

where A, surface area(m^2); N, number of gas molecules; α, sticking coefficient, which is between 0 and 1; p, the vapor pressure at a given temperature(Pa); N_A, the Avogadro constant (6.022×10^{23} mol^{-1}); M, molar mass (26.982 kg mol^{-1} for Al); R, gas constant ($8.314 J\cdot$ $\mathrm{mol}^{-1}\cdot$ K^{-1}); T, temperature(K). For our calculation, the sticking coefficient of 1 is used which assume that all Al adatoms stick on the surface. The

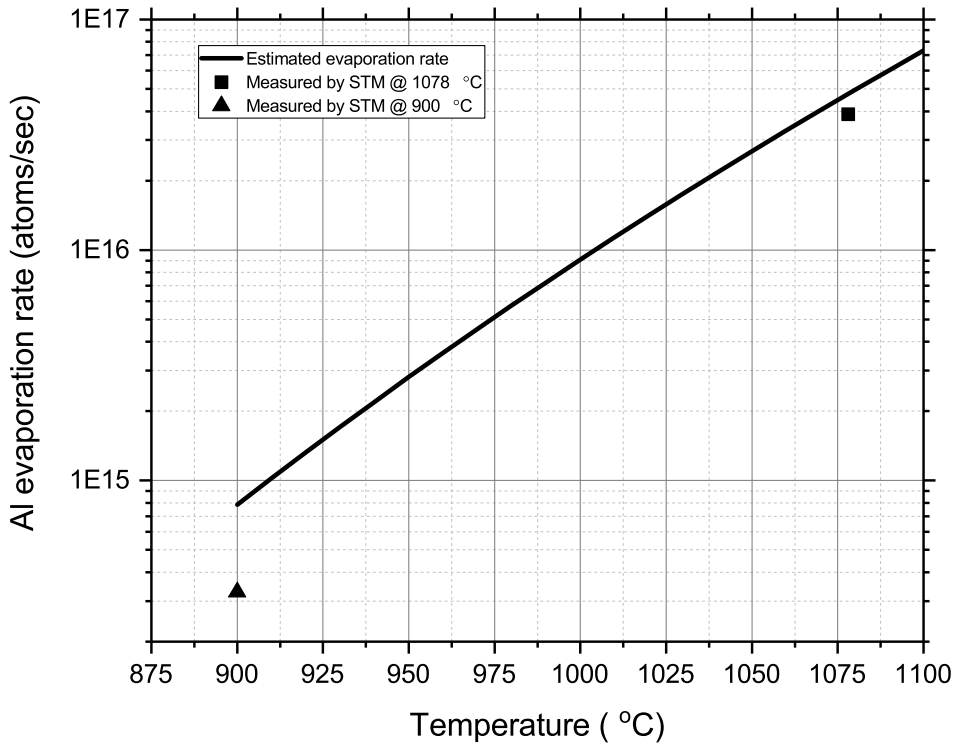

Fig. 2.23: This is the calculated evaporation rate of Al using Eq. 2.8. The triangle at 900 °C is the Al deposition rate measured by the STM, which is $\approx 3.28 \times 10^{14}$ atoms/second. The square at 1078 °C is the deposition rate measured by the STM, which is $\approx 3.89 \times 10^{14}$ atoms/second.

area of Radak crucible, 0.37 cm^2, is used. Then, the calculated value is compared to the STM image as shown in Fig. 2.24. The calculated value at 1078 °C is higher than the measured value by the STM. A thermocouple measures the temperature at the bottom of the outer crucible, which is not an accurate temperature of Al source. The value measured by the STM is the deposition rate, which need to consider the geometrical factors. With a rough estimation of the distance and the orientation of the Al evaporator and the sample, the direct measurement of the deposition rate by the STM is more reliable than the temperature of the crucible.

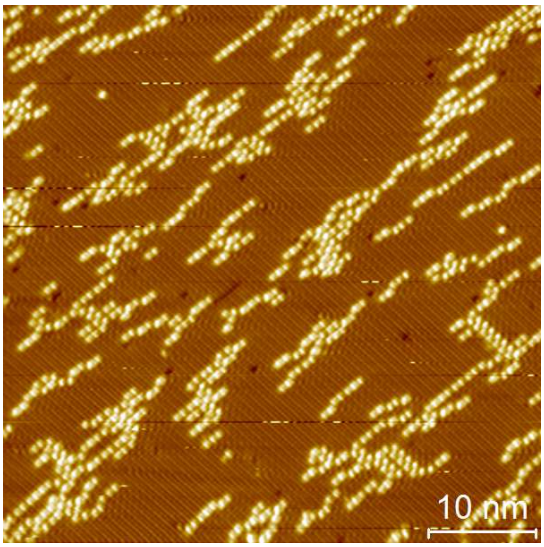

Fig. 2.24: This is a STM image taken at V_{tip} = -2.00 V and I_{set} = 150 pA. The estimated area coverage of Al is ≈ 17 % using same method as in Fig. 2.21(b). The Al adatoms form the chains on the surface running perpendicular to the underlying (2×1) reconstructed Si(100) dimers.

Fig. 2.24 is taken after Al deposition. The crucible temperature measured by a thermocouple is 1078 °C for 35 seconds. The Si(100) substrate is prepared by the *ex situ* cleaning in a cleanroom and the *in situ* high temperature flash annealing as described in section 2.3. Fig. 2.24 shows the Al chains growing perpendicular to the underlying Si(100) dimer rows. The areal coverage of deposited Al on the surface is ≈ 17 %. The areal coverage is estimated in a same way as Fig. 2.21 from the height histogram and Gaussian fitting to two peaks from the substrate and Al adatoms. The deposition rates at two temperatures of 900 °C and 1078 °C are measured by the STM. The deposition rate at 900 °C is ≈ 3.28 × 10^{14} atoms/second(triangle in Fig. 2.23). The deposition rate at 1078 °C(square in Fig. 2.23) is ≈ 3.89 × 10^{14} atoms/second. The deposition rates measured by the STM are in Fig. 2.23 are used for the experiments in the chapters 4 and 6.

In the next section, the *in situ* hydrogen passivation process on Si(100) is

discussed. The atomic layer of the hydrogen atoms passivating on the Si(100) has been used as a resist layer in the CMOS fabrication techniques for STM lithography. The procedure to passivate the Si(100) surface with the H passivation(H:Si(100)) and the STM images of a clean H:Si(100) surface will be presented.

2.4.4 H passivation

STM also has been used to manipulate individual atoms and molecules on the surface with atomic precision. Using hydrogen passivated Si(100) surface (H:Si(100)) as a resist layer in conventional CMOS lithography techniques, research groups have demonstrated STM lithography with atomic precision. [30, 32, 33, 92, 112–114] By selectively removing hydrogen atoms using a STM tip at various bias and tunneling current conditions, the STM can pattern device structures.

Hydrogen gas with ultra high purity(99.9999 %) is used. The hydrogen gas manifold is pumped with a turbo pump down to $\approx 2\times10^{-9}$ Torr. Then, it is baked out with a heat tape at $\approx$ 150°C for a several days to remove the residual adsorbates or contaminants inside the gas manifold while pumping out the manifold with a turbo pump. When the hydrogen gas manifold is clean, the ultra high purity hydrogen gas is loaded to a manifold at $\approx$ 15 psi.

Before hydrogen passivation, the sample is prepared as described in section 2.3 to ensure a clean (2×1) reconstructed Si(100) surface and inspected with STM. The hydrogen passivation procedure is as follows:

1. Degas a tungsten filament mounted at the top of the deposition chamber as

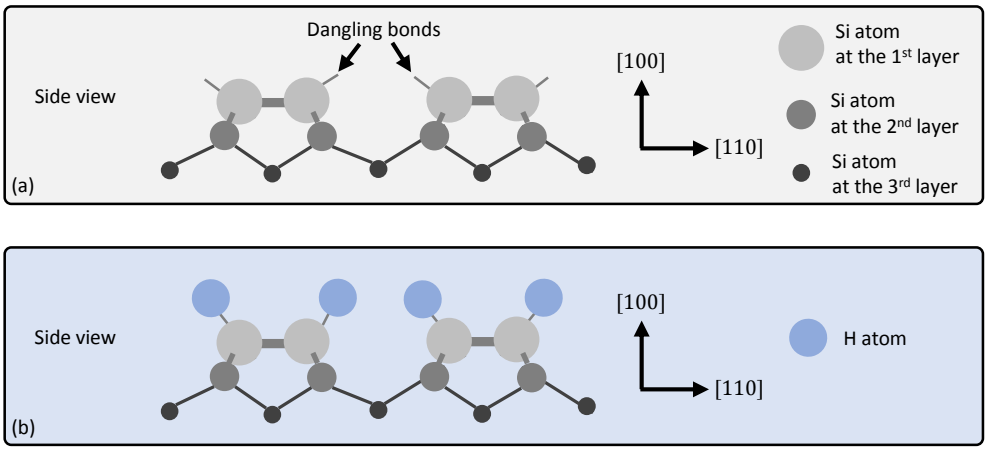

Fig. 2.25: This is a schematic drawing of H passivated Si(100) surface. The cartoon at (a) shows the side view of the top three layers of Si(100) substrate. There are dangling bonds at the top surface. When a bare Si(100) surface is exposed to H atoms, H atoms passivate to Si(100) dangling bonds as depicted (b).

depicted in Fig. 2.1 at ≈ 1800°C for 2 hours.

2. Turn off a tungsten filament. Fill the cryoshroud with LN_2

3. *in situ* substrate preparation as described in section 2.3.2.

4. Heat the sample at ≈ 300°C. Rotate the 5 axis manipulator so that sample is not facing the tungsten filament.

5. Turn on the tungsten filament to 1800 ° to decompose H_2 into H^+.

6. Refill a cryoshroud with LN_2.

7. Turn off the ion pump on the deposition chamber.

8. Close the two gate valves between the deposition chamber and the turbo pumps.

9. Open the leak valve on the hydrogen gas manifold until the ion gauge on the deposition chamber reaches to 2×10^{-6} Torr.

10. Rotate the manipulator until the surface of the sample is oriented perpendicular to the filament.

11. Keep the chamber pressure at 2×10^{-6} Torr for 10 minutes.

12. After 10 minutues, close the leak valve and rotate the manipulator.

13. Cool down the sample to room temperature and turn off the filament.

14. Open the gate valves to pump out the hydrogen gas.

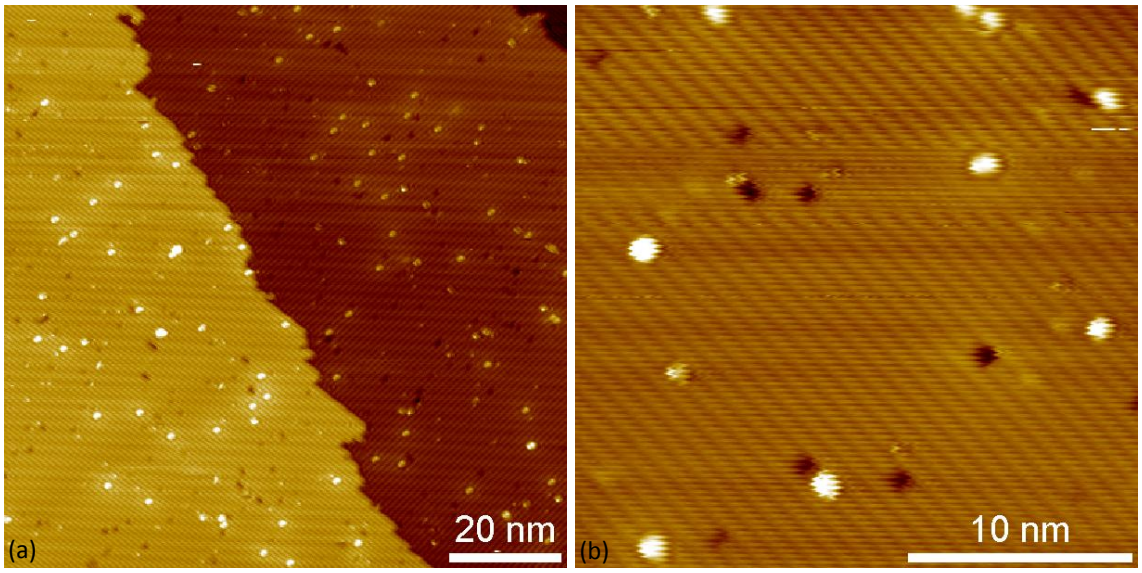

Fig. 2.26: STM images of H:Si(100) taken at $V_{tip} = 1.90$ V and $I_{set} = 100$ pA. (a) This is 100 nm × 100 nm. (2×1)Si(100) dimer rows are visible. The top terrace is the step A(S_A). The next terrace with a step B(S_B) at the right top corner of the image. The bright spots are dangling bonds of Si(100). Based on the number of dangling bonds, > 99% of the surface is passivated by hydrogen atoms. (b) This is 25 nm × 25 nm. The bright spot are dangling bonds. The dark features are vacancy defects.

15. Turn on the ion pump.

16. Transfer the sample to the STM chamber.

The hydrogen passivated Si(100) surface (H:Si(100)) is shown in Fig. 2.26. The bright spots in Fig. 2.26 are remaining dangling bonds. The Fig. 2.26 shows three atomic steps. The top terrace is the step A(S_A). The nex terrace is the step B(S_B). At the top right corner shows the another lower terrace. The Fig. 2.26(b) shows a clean H:Si(100) with very low density of surface defects. The H:Si(100)

surface is used to fabricate nanowires using STM lithography, which is discussed in section 2.2.3 and phosphine(PH_3) dosing in chapter 6, and test the elemental Al for the STM lithography.

2.5 Summary

In this chapter, the experimental set-up and background of the STM, the STS, and the STM lithography are discussed. Also, the *ex situ* and *in situ* sample preparation process are discussed. In order to obtain a clean (2×1)Si(100) surface, the components in the UHV chamber has been modified. The UHV chamber with the base pressure of 4-5 $\times$ 10^{-11} Torr is always monitored by RGA. Also, the careful calibration for the pyrometer using Au-Si and Al-Si eutectic samples has been performed since our *in situ* process for the sample preparation, Si overgrowth, and fabrication of Si/Al/Si(discussed in chapter 4) depends on the correct temperature reading.

As shown in section 2.3.2, the clean (2×1)Si(100) surface is prepared by our *ex situ* and *in situ* cleaning process, which is always inspected by the STM. Our tests to lower the temperature to remove SiO_2 layer by Si flux and thermal decomposition are not yet successful. However, with a careful *in situ* cleaning by improving the H^+ cleaning process, SiC and vacancy rows on the surface can be reduced. The UHV deposition chambers are also equipped with two Si deposition systems (^{28}Si ion source, e-gun deposition for Nat. Si), the thermal furnace for the elemental Al, and the *in situ* H passivation system, which are inspected by the STM.

In the following chapter, the UHV Si(100) growth at the low temperature is presented. The UHV Si growth at low temperature is challenging due to the roughness, impurities and limitation of epitaxy. The detail discussion of the Si(100) surface structure with metal and chemical impurities is presented.

Chapter 3

Low Temperature Epitaxial Si(100) Growth

3.1 Introduction

Silicon has been a driving workhorse in semiconductor industry since Si is a relatively cheap material and it is easy to obtain high quality epitaxy with very low impurities. The commercially available Si wafers or even most of high quality Si epi fabricated at research labs require high temperature processing. In addition, lots of Si CMOS fabrication processes require high temperature in order to achieve low chemical impurities and defects. [21] As Si CMOS technology advances, the size of a single transistor gets smaller. During last a few decades, the STM enabled the atomically precise devices in Si(100) using the hydrogen resist layer and phosphine gas dosing, such as a single atom transistor, nano-wires, and etc. [30, 33, 113, 115] High quality epitaxial Si grown at low temperature is a key requirement for new low dimensional devices in Si due to thermal diffusion of dopants during high temperature process. The low chemical impurities and good single crystallinity greatly

affect the device performance. I have studied *ex situ* and *in situ* surface preparation process for UHV MBE Si(100) growth in the chapter 2. I fabricated high quality epitaxial single crystal Si(100) at low temperature measured by the STM.

In this chapter, I introduce the fundamental of (2×1) reconstructed Si(100) surfaces, surface defects, impurities, and Si overgrowth at low temperature. In order to obtain the epitaxial Si overgrown layer, we need better understanding of Si(100) crystal, defects, and impurities. Since the Si epilayer is overgrown at the low temperature, the overgrown Si layers are rougher than the starting substrate. Therefore, our test to make the surface smoother is discussed. Also, the high epitaxial quality of the Si layers grown by the EFM is inspected using the STM.

3.2 (2×1) reconstructed Si(100)

Si(100) is essential to the semiconductor industry and has been extensively studied as a template to grow various types of materials. Therefore, the fabrication process for the Si(100) substrate is well established. The epitaxial growth of Si(100) has been studied by many research groups, which will be discussed in section 3.3. [116–124] Especially, for STM lithography, (2×1) dimer rows can be used as a natural alignment marks for patterning. I have improved the *ex situ* and *in situ* sample preparation process in section 2.3. In this section, I will discuss the epitaxial growth of Si(100) and impurities.

As discussed in 2.3.2, the RHEED pattern in Fig. 2.10 shows the (2×1) Si(100) surface after *in situ* cleaning. Every sample is also inspected using STM after *in*

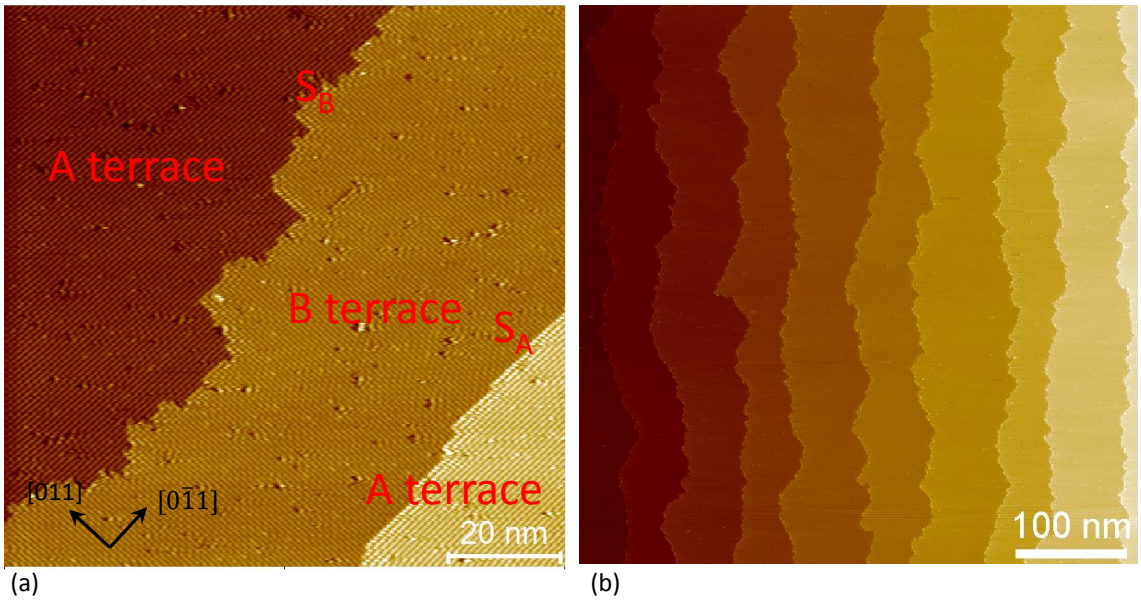

Fig. 3.1: Filled state STM images at V_{tip} = 2.00 V and I_{set} = 100 pA. (a) This is 50 nm × 50 nm filled state STM image of (2×1) Si(100) surface. The top terrace is the B terrace. The bottom terrace is the A terrace. The edge of the B terrace is the S_B step. The edge of the A terrace is the S_A step. This STM image shows very low density of surface defects which appear as the dark spots. The surface coverage of the surface defects is less than 1 %. (b) This is the large area scan of 500 nm × 500 nm. The size of the terrace is nominally decided by the wafer miscut angle. The typically length of a terrace of our substrate is ≈ 100 nm. The height of the terrace is 0.138 nm which is a quarter of the Si atomic spacing.

situ cleaning as shown in Fig. 3.1. Fig. 3.1 are the filled state images taken at V_{tip} = 2.00 V and I_{set} = 100 pA. Fig. 3.1(a) is 50 nm × 50 nm image of a clean (2×1) reconstructed Si(100) surface with very low surface defects. The top terrace of Fig. 3.1(a) is the B terrace where the dimer rows run along the [011] direction. A dimer is the bonding of top two Si atoms, which appear as ellipsoids in the filled state image due to π bonding states. The terrace below and above the B terrace is called A terraces, which the dimer rows run perpendicular to the B terrace. Fig. 3.1(b) is a large area scan of 500 nm × 500 nm. The height of each terrace is a quarter of Si crystal atomic spacing which is 0.138 nm. The typcial length of the terrace of our samples is ≈ 100 nm. This is nominally determined by the miscut angle of the

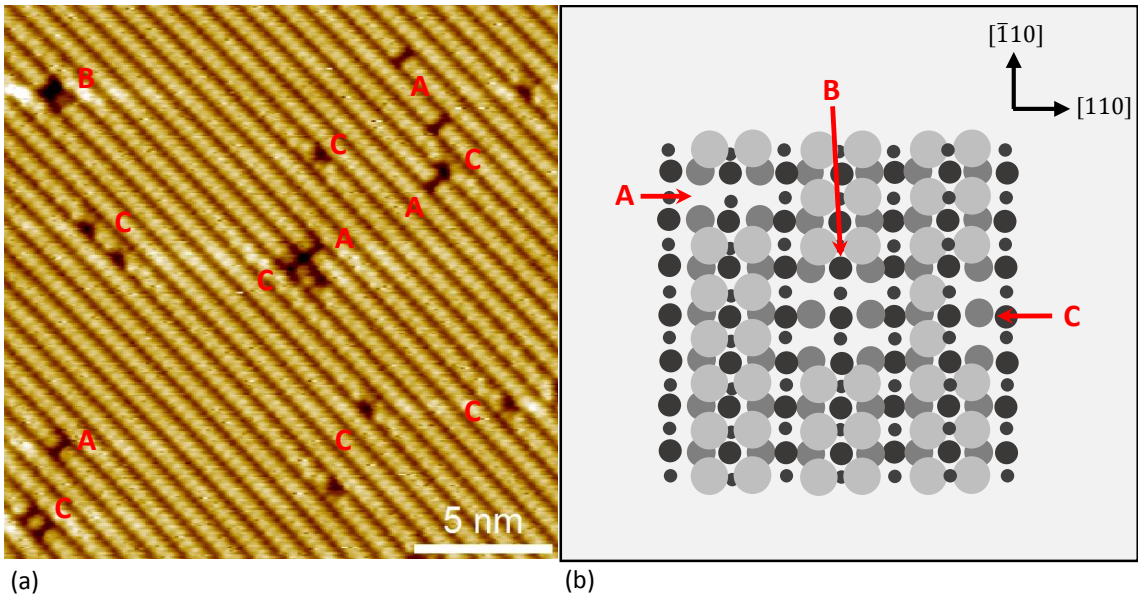

Fig. 3.2: (a) This is a filled state STM image of Si(100) surface taken at $V_{tip} = 2.00$V and $I_{set} = 100$ pA. The dark spots with different shapes are surface defects such as vacancy defects and absorbates. A and B defects are vacancy defects. The A defect is two missing Si atoms or one dimer at the top surface as described in schematic drawing of surface defects (b). The B defect is four adjacent missing atoms(two dimers). The one of C defects are two missing atoms along the dimer row as shown in (b). The C defect can be also due to H, O, OH, and H_2O absorbates on the surface. The C defects causes the buckled dimers. [125]

wafer. Our Si(100) wafers from VA semiconductor are specified at $\pm$ 0.05 °.

Fig. 3.1 shows a clean Si(100) surface, however, there are surface defects appearing as dark features. These defects can affect the morphology, the growth of the Si epilayer, the quality of the hydrogen passivation, and the single atomic layer of Al. It is important to minimize the surface defects and understand the causes and effects of the defects. Fig. 3.2 (a) shows a filled state image of the Si(100) surface with different types of defects labeled as A, B, and C. A, B, and C types are the most common defects on Si(100) surface. A and B defects are missing Si atoms at the surface as illustrated in Fig. 3.2(b). The A defect is two missing Si atoms that forms one missing dimer. The B defect is a pair of A defects (two missing dimers). [126]

Unlike A and B defects, there are various types of C defects. First, similar to A and B, the C defect can be caused by missing atoms shown in Fig. 3.2(c). The C defects can also be induced by absorbates, such as H, O, OH, and H_2O. [126–129] Ref. [130] using STM and FT-IR shows that number of C-type defects increases as the elapsed time increases since the *in situ* high temperature flash cleaning. Also, from that study, as the background pressure increases, the C defect density increases. Depending on the configuration of C defects, $I(V)$ characteristics show metallic behaviors at room temperature, which means that STS spectra taken on C defects does not show the band-gap.

At the lower temperature of 80 K, as the Si(100) surface reconstruction shift from (2×2) to (4×2), the $I(V)$ characteristics shows semiconductor like behavior with a band gap of $\approx$ 0.5 eV. [131] Ref. [129] shows different types of C defects using STM and STS. More interestingly, for our study, the III metal such as Al, In, and Ga are influced by the C defects. [132, 133] The metal adatoms on the Si(100) surface form self-assembled chains growing perpendicular to the underlying Si(100) dimer rows. However, the previous studies show that C defect terminates the metal chains, which results in the change in the electronic states measured by the STM and the STS. [134] The STS measured on the terminated Al and In chain shows the shift of the π-bonding state closer to Fermi level resulting the narrower band gap. [134–136]

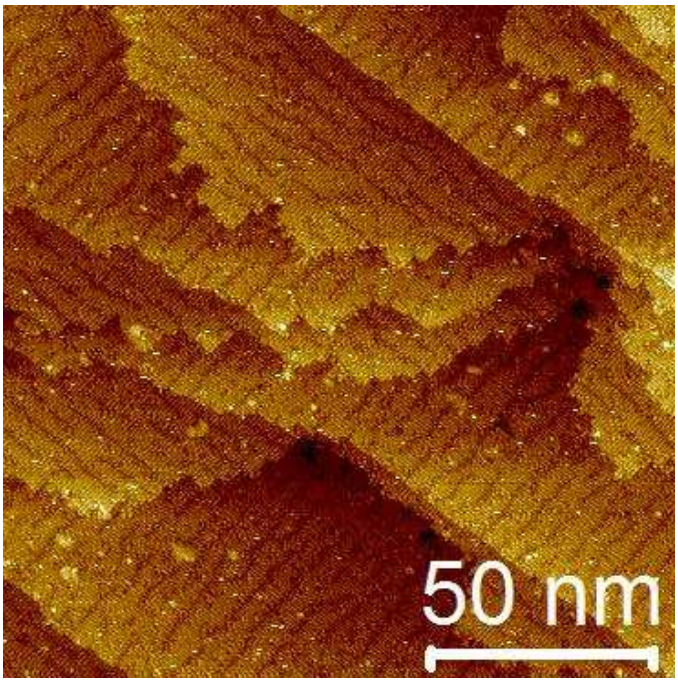

Fig. 3.3: The long dark vacancy lines growing perpendicular to the Si dimer rows indicates the metal contamination. This is taken at $V_{tip} = 2.00$ V and $I_{set} = 150$ pA. The area coverage of dark vacancy lines is ≈ 1 %.

3.3 Impurities in Si(100)

3.3.1 Metal Impurities

In order to fabricate high quality epitaxial Si(100) layers, all types of contaminants in the film or the substrate must be removed. Ni atoms or other metal contaminants in the Si(100) substrate cause strain, which increases the surface roughening and stacking faults. These contamination strongly depends on the *ex situ* and *in situ* sample preparation. [137, 138] Especially, metal contaminants, such as Ni and Fe, often come from a sample holder, tweezers made of stainless steel, and the thermocouple. [137] After the *in situ* cleaning, metal contaminants appear as dark vacancy lines growing perpendicular to the (2×1) Si(100) dimer rows as shown in Fig. 3.3.

The filled state image of Si(100) after flash annealing in Fig. 3.3 shows dark vacancy lines, which are most likely due to Ni contaminants. The many parts in the UHV chambers and tweezers are made of stainless steel, which contain Ni. Also, other metal atoms in the subsurface of Si(100) appear as dark vacancy lines, which will be discussed later in chapter 6. The Ni and Fe atoms within first few layers from the surface cause repulsive interactions between vacancies along a dimer row and attractive interactions between vacancies in adjacent dimer rows. [139–141] As low as the surface coverage of $\approx 1\%$ Fe causes dark vacancy lines. [142] In our study with Al in Si(100), incorporated Al in Si(100) shows a same dark lines (chapter 6).

In order to get rid of unintended metal contamination, the careful handling and cleaning procedures are most important. As discussed in section 2.3.1, the *ex situ* cleaning procedure is carefully designed to remove the organic and metallic contamination on the surface using SC2 cleaning procedure. After *ex situ* cleaning, the 2-3 nm thick chemically grown SiO_2 is protecting the surface until the sample is introduced into the vacuum chamber. We made an effort to minimize the time between the last step of *ex situ* cleaning and loading into the vacuum chamber. Also, the sample holders are made of molybdenum. We avoid any stainless steel that make direct contact to the sample. [143]

The *in situ* cleaning procedure also impacts the metal contamination. [137, 138] As described in section 2.3.2, in order to remove the chemically grown SiO_2 and achieve the clean (2×1) Si(100) surface, the sample is flashed at 1200 °C for tens of seconds in UHV. Then, the sample is quickly cooled down to 800 °C after last 1200 ° flashing. Then, the sample is cooled down slowly from 800 °C to room temperature.

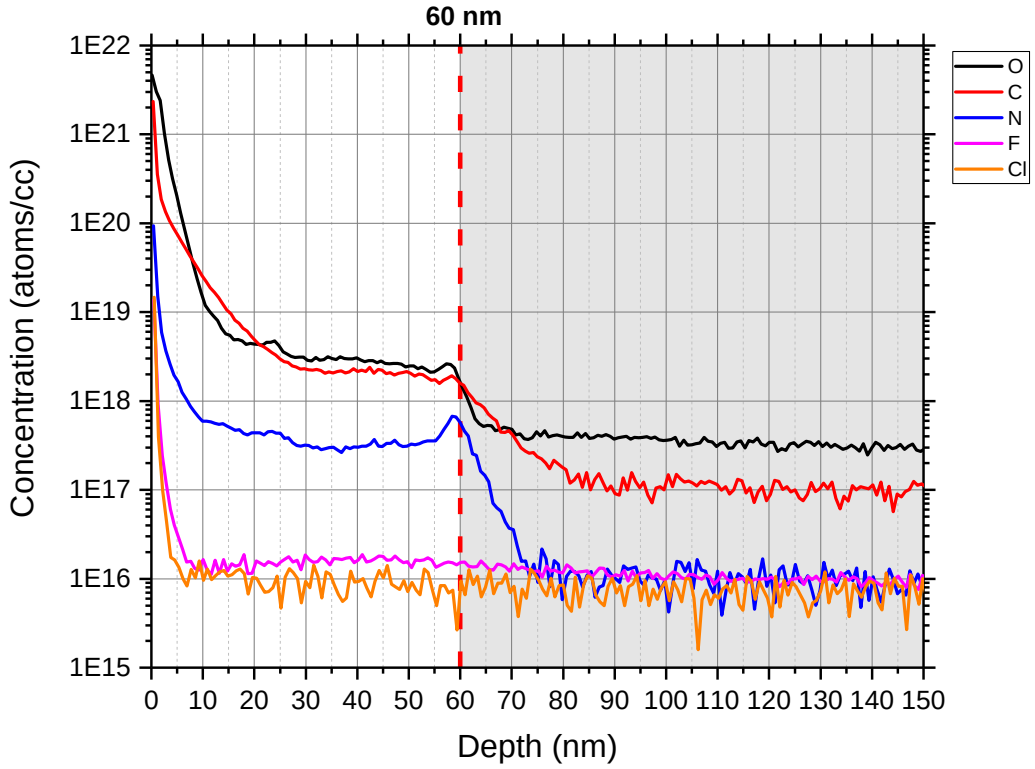

Fig. 3.4: This is SIMS result of chemical impurities such as O, C, N, F, and Cl. There are O, C, and N in the epilayer overgrown at 450 °C using the electron beam evaporator. F and Cl are lower than SIMS detection limits.

Also, during high temperature flashing, the chamber pressure is always $< 1\times10^{-9}$ Torr. These are the typical cleaning procedure to eliminate the dark vacancy lines.

3.3.2 Chemical Impurities

C, N, and O are the most common impurities in Si. Those chemical impurities causes strain and pinning sites during Si growth. The chemical impurities degrade the device performance and crystal quality. Also, the impurities act as scattering sites and charge traps which reduces electronic properties. [144, 145]

Using a≈ 60 nm of Si(100) epilayer, our overgrown Si(100) epilayer is char-

acterized by by secondary ion mass spectrometry (SIMS) in Fig. 3.4. ≈ 60 nm of Si(100) epilayer is grown at 450 °C with a deposition rate of 0.136 nm/min using the electron beam evaporator in UHV as described in section 2.4.2. During the Si deposition, the chamber pressure is below 2×10^{-10} Torr. Fig. 3.4 is the depth profile of C, N, O, F, and Cl concentrations. SIMS measures the depth profile of the material composition by sputtering the material with a focused ion beam (typcially O_2 or Cs) with a depth range of a few angstroms to micrometers. Then, the sputtered materials are collected by mass spectrometer to analyze the composition. The surface is at the left side of the Fig. 3.4 at depth of 0. The red line labeled as 60 nm is the interface between the Si epilayer and the substrate. SIMS results in Fig. 3.4 shows that F and Cl are below its detection limit ($< 10^{16}$ atoms/cc) even though Fig. 2.2 shows a peak at mass 19. C, O, and N are detected within the epilayer. The sharp decrease of the concentration near the surface to ≈ 20 nm represents absorbates on the surface due to the sputtering process after the UHV fabrication process. When the sample is exposed to the ambient, all the chemical impurities are build-up on the surface. The concentration of C is $\approx 2\times10^{18}$ atoms/cc. The concentration of O is $\approx 3\times10^{18}$ atoms/cc. The concentration of N is $\approx 3\times10^{17}$ atoms/cc. After high temperature flashing, the substrate was transferred to the STM chamber and measured by STM for a couple of hours where the baseline pressure is typically 4.3×10^{-11} Torr. During this period, C, N, and O in the STM chamber may be absorbed on the surface, which shows the increase of C, N, and O concentrations at the interface in Fig. 3.4.

The RGA scan shown in Fig. 2.2 shows H, C, N, and O in the deposition

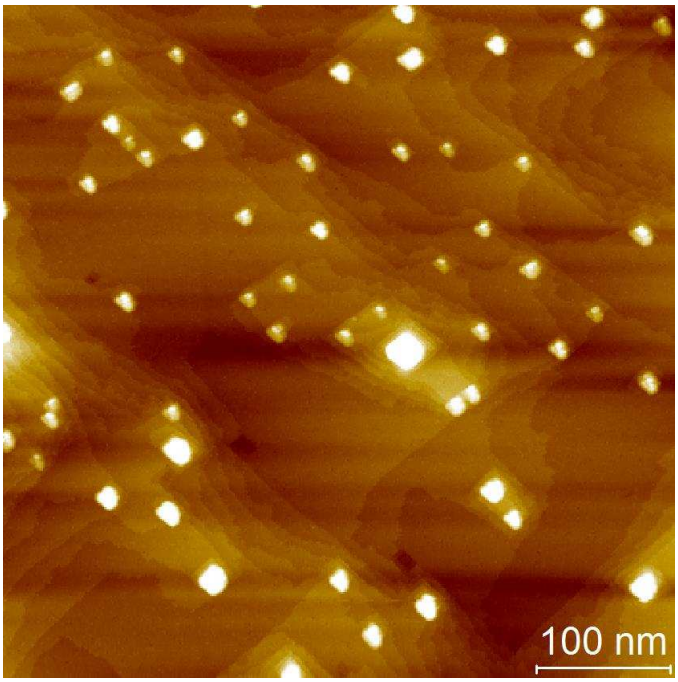

Fig. 3.5: The bright pyramids on the surface are SiC which exist in the overgrown Si epilayer.

chamber. These can contribute to contamination during Si overgrowth. Also, as shown in Fig. 2.19, our Si e-beam evaporator does not use crucible in order to minimize the outgassing of impurities from the other parts of the evaporator. However, the hot tungsten filament heats up some other parts of the evaporator, which can outgass and deposite with Si.

Our previous experiments indicates the C contamination in the epilayer. Fig. 3.5 shows SiC formed on the surface. The pyramid shape of bright areas in Fig. 3.5 indicates SiC. SiC on some substrates are observed via RHEED on the substrate after high temperature flahsing indicating large amount of carbon contamination on the surface.

The low C contamination results in forming SiC on the surface as shown in Fig. 3.6. Fig. 3.6 is 100 nm thick ^{28}Si epilayer grown at 450 °C. Then, this sample

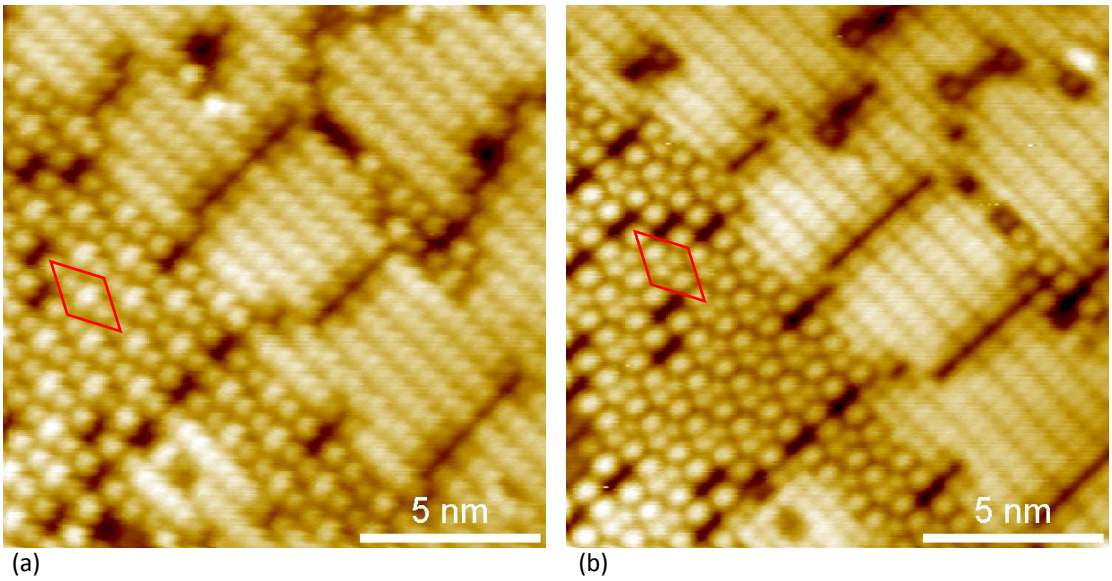

Fig. 3.6: This is 40 nm thick ^{28}Si epilayer grown at 450 °C. Then, the sample is annealed to 600 °C for 1 hour. (a) and (b) are taken on the same area. (a) This is a filled state image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. A dumbbell shape marked with red with one large ellipsode and two spheres along Si(100) dimer rows indicates C-induced (4×4) reconstructed Si(100). (b) This is an empty state image at V_{tip} = -2.00 V and I_{set} = 100 pA. The dumbbell feature in a filled state shows 4 spheres. This is also observed by other group. [146]

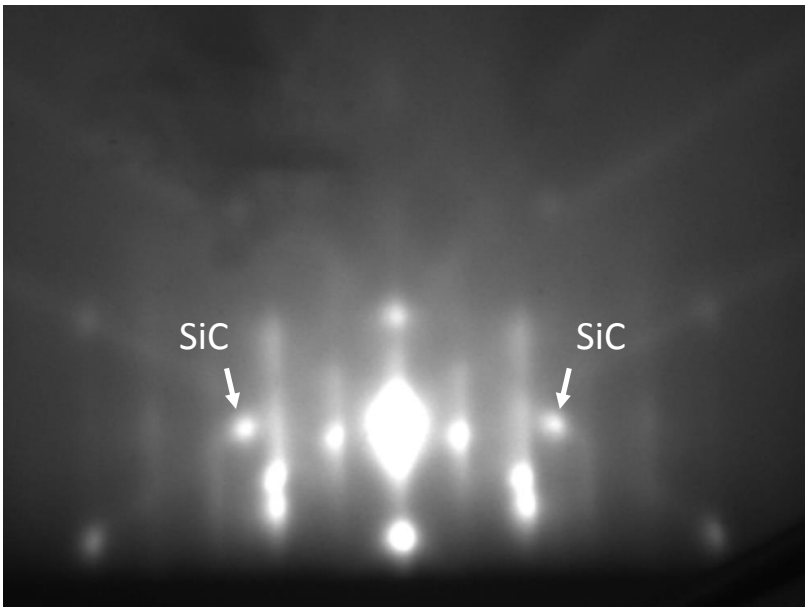

Fig. 3.7: This is RHEED patterns showing (1×1) streaks and (2×1) lines Si(100). However, there are additional pattern outside of (1×1) streaks which two arrows are indicating SiC.

is annealed to 600 °C for 1 hour. Fig. 3.6 shows C-induced (4×4) reconstructed Si(100) which is also observed by other group. [146] Fig. 3.6(a) is a filled state image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. Fig. 3.6(b) is an empty state image at V_{tip} = -2.00 V and I_{set} = 100 pA. The left side of Fig. 3.6 (a) and (b) show (4×4) reconstructed Si(100) which is same as Ref. [146]. This study shows after annealing to 750 °C, c(4×4) appeared along the dimer rows up to 0.07 ML of C. As the area coverage of C contaminants goes beyond 0.07 ML, various types of reconstructed SiC form on the surface. [146] This particular reconstruction is due to the increased tensile strain by C. The C contaminants could come from the background gas in the UHV chamber during annealing process. However, during annealing, the chamber pressure is $< 10^{-10}$ Torr. The absorption of C in the UHV chamber is very unlikely. The partial pressure of C in UHV is less than 10^{-11} Torr. Even if all the C in UHV stick to the sample, it is below the detection limit of SIMS of 10^{16} cm^3. The ^{28}Si epilayer typically contains 4.5 × 10^{19} atoms/cc from the previous SIMS measurements, which means that the C contaminants are coming from the deposition source. The C in the epilayer could cause the SiC at the surface.

3.4 Post-annealing process for overgrown Si(100): Improvements in chemical impurities

In order to improve the chemical impurities in ^{28}Si epilayer, we annealed the ^{28}Si samples to 950 °C for 1 hour in the UHV chamber. The thermal annealing out-

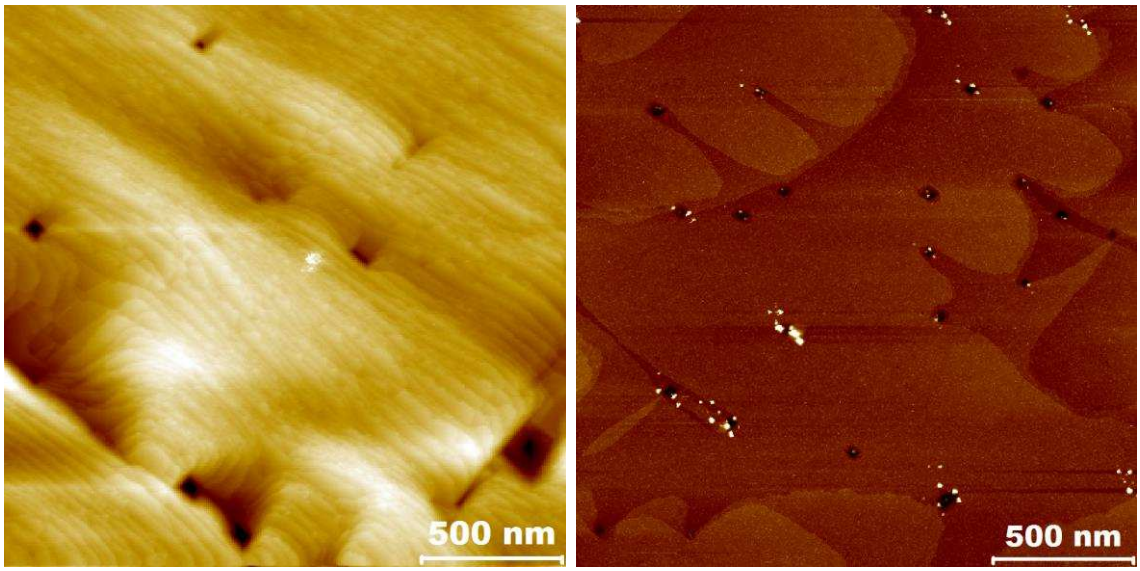

Fig. 3.8: (a) 30 nm Si epilayer grown at 600 °C shows the pits. (b) a few nm of Si epilayer grown at 700 °C has pits and contaminants around and inside the pits.

diffuses the C, N, and O from the ^{28}Si epilayer. Ref. [147] studies the solid solubility of O in Si and activation energy (67.1 kcal·mol^{-1} $\approx$ 2.91 eV) and prefactor (3.2) of O diffusion in Si under 1200 °C to 1000 °C. This study summarizes the activation energy and prefactor of O in Si from previous studies, which shows a range of values due to the different treatments of silicon substrates and process environments. Another interesting result in Ref. [147] is the O diffusion profile for different inital O concentration for 10^{18}, 6×10^{17}, and $5\times$ 10^{15} at. cm^{-3}. For three different O concentrations, the extrapolated O concentration at the surface is $\approx 10^{17}$ at. cm^{-3}. The solid solubility of O in Si is 2.8×10^{18} at. cm^{-3}. [148] Above the solid solubility, the O forms SiO clusters in Si. Fig. 3.9(a) shows that the O concentration in ^{28}Si film is slightly higher than the solid solubility. Another common impurity in Si is C. C in Si causes nucleation of O precipitates. [149] The solid solubility of C at 850 °C is $\approx 1.9 \times 10^{14}$ cm^{-3}, which is much lower than typical C concentration in

Si wafers and our samples. [150] Ref. [151] finds kick-out mechanisms of C diffusion in Si above 800 °C. The other impurity in our samples is N, known to cause the vacancies and pinning dislocations. [152] In the case of N, the activation energies of 2.38-2.8 eV are measured. [153–155]

Fig. 3.9(a) is a SIMS result showing depth profiles of C, N, O, F, and Cl concentration of ^{28}Si epilayer as grown. C is measured to have highest concentration of 9.5 $\times$ 10^{18} cm^{-3}. N is measured to be 5.5 $\times$ $10^{18}cm^{-3}$. O is 2.1 $\times$ $10^{18}cm^{-3}$. In this sample, Cl of 2.2 $\times$ 10^{17} cm^{-3} and F or 2.5 $\times$ 10^{17} cm^{-3} are also detected. In order to reduce the C, N, and O concentration in our samples, we annealed the other ^{28}Si epilayer grown at 450 °C to 950 °C for 1 hour in Fig. 3.9(b). The O concentration is reduced to $\approx$ 2.5 $\times$ 10^{17} cm^{-3}. The depth profiles of C and N decrease near the surface and the substrate, which show the thermal diffusion. Also, the C concentration at the plateau is $\approx$ 8.7 $\times$ 10^{18} cm^{-3}. N is measured to be $\approx$ 3.3 $\times$ 10^{18} cm^{-3}. The F and Cl are below the detection limit of 10^{16} cm^{-3}.

Fig. 3.10 are STM images of ^{28}Si epilayer grown at 450 °C before and after annealing at 950 °C. The first row of Fig. 3.10(a), (b), and (c) are the STM images of the as grown ^{28}Si epilayer. Fig. 3.10(a) shows the island growth mode. Fig 3.10(b) and (c) show (2×1) dimer rows and terraces. This sample is then moved to the main chamber and annealed to 950 °C for 1 hour in UHV condition. After annealing, the sample is moved to the STM chamber for inspection. The second row of Fig. 3.10(d), (e), and (f) are taken on a similar location as Fig. 3.10(a)-(c) after 950 °C annealing. After 950 °C annealing, ^{28}Si film shows high density of contaminants, which are most likely C or N. The pyramid and rectangular mountains

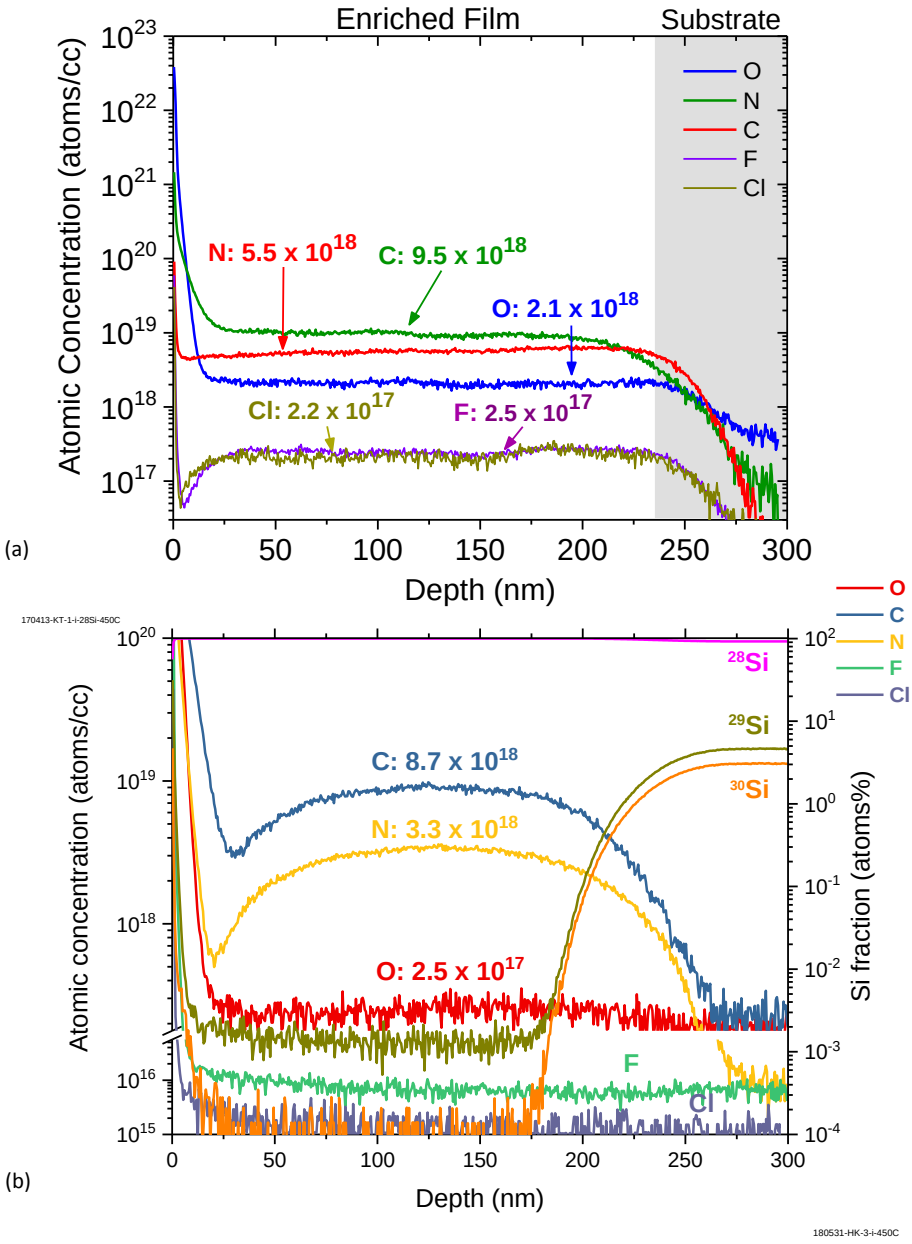

Fig. 3.9: (a) This is a SIMS for C, N, O, F, and Cl in ^{28}Si epilayer grown at 450 °C. This sample contains high density of chemical impurities such as O(2.1×10^{18} atoms/cc), N(5.5×10^{18} atoms/cc), C(9.5×10^{18} atoms/cc), Cl(2.2×10^{17} atoms/cc), and F(2.5×10^{17} atoms/cc). The shaded area is the substrate where the atomic densities of chemical impurities decreases below the detection limit. (b) This is the SIMS measurement of same chemical impurities from another 165 nm ^{28}Si sample after 950 °C for 1 hour. The atomic concentration of C, N, and O decreases. F and Cl are not detected. The maximum C, N, and O concentration decreases near the surface and the interface between the substrate and epilayer. This is due to the thermal out-diffusion of C, N, and O from the epilayer. The growth conditions for both samples, such as the deposition rate, and the chamber pressure are nominally identical.

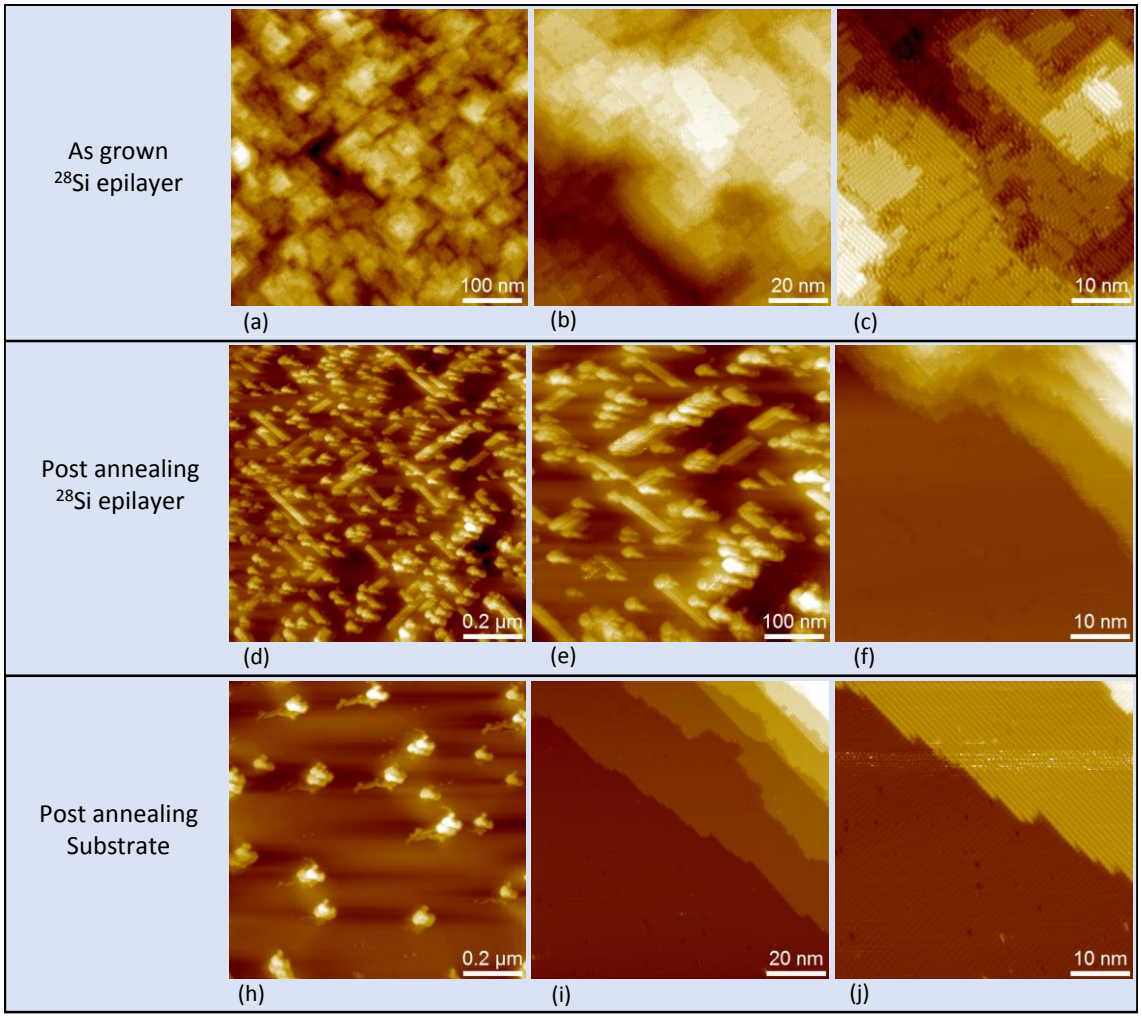

Fig. 3.10: STM images are taken at $V_{tip} = 2.00V, I_{set} = 100pA$. (a), (b), and (c) are STM images of ^{28}Si epilayer as grown at 450 °C. (a) is a large area image(500 nm by 500 nm). (b) This is 100 nm × 100 nm area showing Si islands with (2×1) dimer rows. (c) This is a small area (50 nm × 50 nm). This sample is annealed up to 950 °C for 1 hour. After annealing, (d), (e) and (f) are taken on ^{28}Si epilayer. After annealing, (h), (i), and (j) are taken on the substrate far from the ^{28}Si deposited area. (d) and (e) shows that most of the surface area is covered with SiC. This is due to the out-diffused C from the ^{28}Si epilayer. (f) shows (2×1) dimer rows and terraces on some area without SiC. (h) The substrate shows much less SiC formed on the surface compared to (d). (i) and(j) show that A and B terraces with (2×1) dimer rows. The surface defect density is very low.

are typically SiC. As shown in Fig. 3.9(b), C and N out-diffuse and accumulate on the surface and appeared on the STM images in Fig. 3.10(d)-(f). The size and the shape of some contaminants are due to the tip artifacts. Fig. 3.10(c) is taken around the contaminants. It shows clean (2×1) dimers and terraces of the Si(100) surface.

Since the deposited ^{28}Si epilayer is covering only a small portion of the (4 mm ×10 mm) chip, some areas on the substrate are not exposed to the ^{28}Si ion beam. Fig. 3.10(h)-(j) are taken on the substrate which is exposed to the same environment as Fig. 3.10(d)-(f). Fig. 3.10(h) has fewer contaminants compared to Fig. 3.10(d). This indicates that the most of contaminants shown on Fig. 3.10(d) and (e) are from out-diffused C and N from ^{28}Si epilayer. Fig. 3.10(i) and (j) show a clean (2×1) dimers and terraces with less than 1% vacancy defects on the surface. Therefore, the contaminants comes from the deposition source. The mass spectrum of the ion beam deposition system in Fig. 2.16 shows a good separation between mass 28 and 29. However, unfortunately, CO^+ and N^2 also has mass ≈ 28, which is same as ^{28}Si. This is the main source of the contamination in the ^{28}Si epilayer.

3.5 Low Temperature Si(100)

Low temperature Si epitaxy has been studied by numerous groups as low as room temperature. [116–124] Epitaxial silicon growth below 500 °C has been shown to have a critical thickness for epixaxy, h_{epi}, which is the maximum thickness to stay epitaxial. [116–118] As the thickness grows beyond h_{epi}, the film becomes

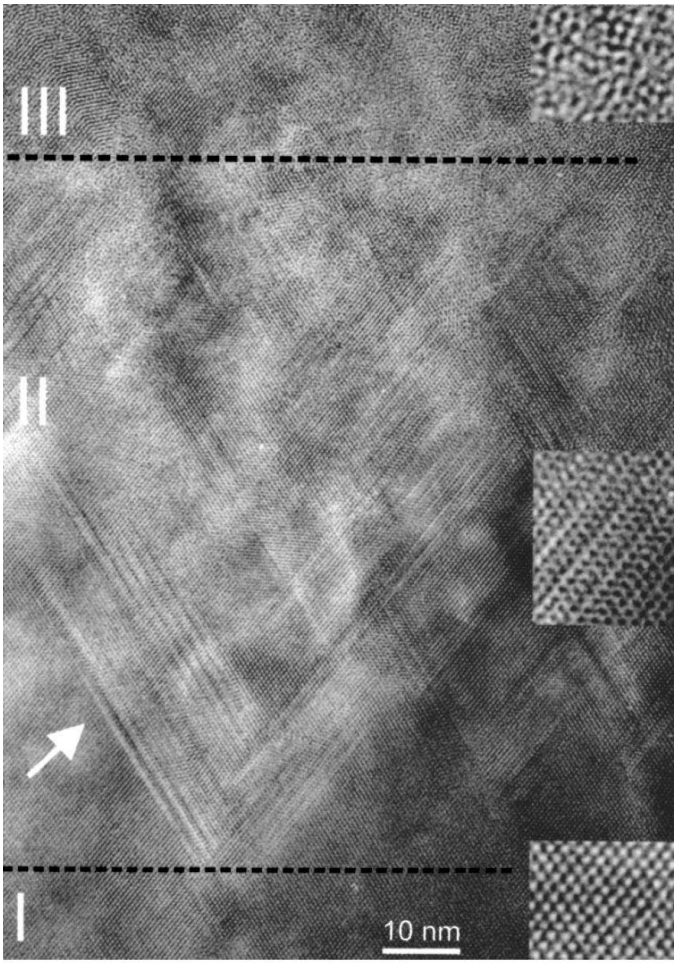

Fig. 3.11: TEM images shows the critical thickness for MBE grown Si epilayer at low temperature. This is taken from Ref. [2].

amorphous. A study shows that h_{epi} exponentially increases as the substrate temperature increases with an ativation energy of ≈ 0.4 eV at a given deposition rate. [116] Other study shows that as the deposition rate increases at a given substrate temperature during Si growth, stacking faults increases as shown in TEM images. As the Si epi layer gets thicker beyond h_{epi}, TEM shows that the epi layer becomes amorphous. [46] However, when the substrate temperature is above 500 °C, the recrystallization in overgrown Si layers is faster than the deposition rate, which h_{epi} becomes infinity.

Fig. 3.11 shows a TEM image of overgrown Si(100) layers at 270 °C by ion assisted deposition from Ref. [2]. As the film gets thicker from I to III in Fig. 3.11, the visible defects in the film becomes worse. The bottom region (I) shows good defect free epitaxy. In the middle region (II), the density of stacking faults increases as the film gets thicker. The top region (III) becomes amorphous as the Si thickness goes beyond h_{epi}. Many groups have been trying to explain the causes of h_{epi}. Many theoretical and experimental studies suggest several factors, such as the presence of H, chemical impurities, surface roughening, etc. Each of the factors plays a role for h_{epi}. Also, most of these factors affect each other.

h_{epi} also depends on the deposition rate. If the deposition rate is less than the recrystallization rate at a given temperature, h_{epi} can increase.

3.6 Epitaxial Quality: STM

In this section, the epitaxial quality of Si grown by EFM is verified by STM as shown in 3.12. Fig. 3.12 are STM images of 60 nm thick epilayer grown at 450 °C. As described in section. 2.4.2, EFM is thermal evaporator. The advantage of EFM is that the evaporation source of FZ i-Si(100) rod is held on the Mo adapter so that the other parts of the evaporator is not heated by the e-beam. However, this limits the deposition rate to ≈ 0.13 nm/min. Typically, the chamber pressure during deposition is $\approx 2 \times 10^{-10}$. As a result, the chemical impurities measured by SIMS in Fig. 3.4 are lower than in the ^{28}Si epilayer.

The epitaxial quality of 60 nm thick Si grown at 450 °C in Fig. 3.4 is inspected

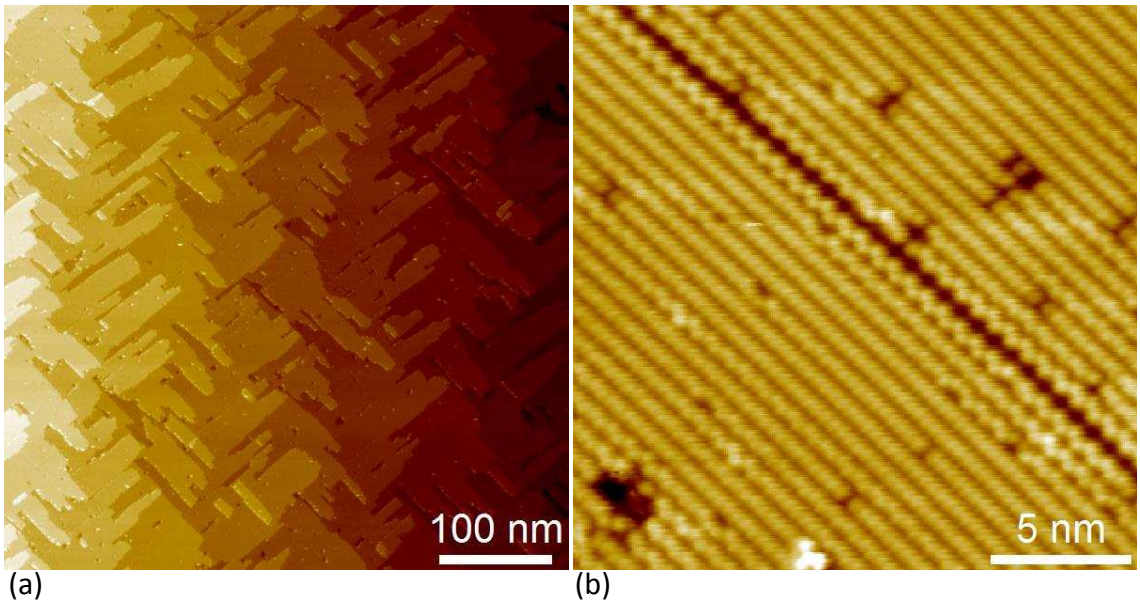

Fig. 3.12: Both images are taken on a same sample as in Fig. 3.4. (a) A large area (500 nm × 500 nm) scan shows a step flow growth mode. (b) This is a small area scan showing a reasonably clean (2×1) reconstructed Si(100) with a small surface defects.

right after deposition by STM. Fig. 3.12(a) taken at $V_{tip} = 2.00$ V, $I_{set} = 150$ pA is 500 nm × 500 nm. This shows a clean step flow growth mode in Fig. 3.12(a). This is due to the low deposition rate limited by the instrument.

Fig. 3.12(b) is a smaller scale STM image (20 nm × 20 nm). This shows clean (2×1) dimer rows with very low vacancy surface defects. There are some buckled dimers with bright spots in the middle of the buckled dimers, which is typically of O or OH as explained in section 3.2. The dark vacancy line growing diagonally in the Fig. 3.12(b) is one Si atom wide. This is a consequence of the reconstruction of Si atoms not due to contaminants.

This sample was not inspected by transmission electron microscopy(TEM). However, later in section 4.3.1, the Al delta-doped Si which is fabricated with EFM is measured by STEM in Fig. 4.5. Fig. 4.5 show a single crystal Si quality with no

stacking faults or other contamination. The Si epilayers grown at low temperature in our UHV system show a high quality epitaxial single crystal.

3.7 Summary

The epitaxial Si(100) overgrown layers are essential to fabricate the atomically abrupt junction with the Al dopants in chapter 4 and nanodevices using the pre-implanted wires and the STM lithography in chapter 5. The atomically precise devices requires the low thermal budget to minimize the thermal dopant diffusion. The UHV Si(100) MBE at low temperature below 500 °C is challenging because of the critical thickness for epitaxy, the metal and chemical impurities. By improving our *ex situ* and *in situ* cleaning procedure, the metal contamination is no longer present in our samples measured by the STM and the SIMS. However, the SIMS and the STM show C, O, and N in the overgrown ^{28}Si and Nat. Si layers. In order to improve the chemical impurities, the post-annealing process at 950 °C in the UHV chamber is tested on the ^{28}Si epilayers. The SIMS data shows the diffusion of C, N, and O the overgrown film. Also, the STM images of as-grown and post-annealed surfaces show the SiC formed on the surface indicating the diffusion of C from the overgrown Si film. The post-annealing process reduces the concentrations of C, N, and O in the overgrown Si film. The STM images of the ^{28}Si and Nat. Si films show the good epitaxial quality. Using the UHV Si(100) MBE, the chapter 4 and 5 will present the Al delta-doped Si(100) and the nano-devices made of P dopants using *in situ* real-time STS mapping for pre-implanted wires and the STM lithography.

Chapter 4

Al delta-doped Si(100) - Si/Al/Si heterostructures

4.1 Introduction

Silicon is the workhorse material in the semiconductor industry due to the high quality oxides that can be grown and the desirable dopant chemistry for a variety of both n- and p-type dopants. While Si is predominantly used as a semiconductor, superconductivity in Si has also been achieved in gallium enriched Si layers by rapid thermal annealing of gallium ion implanted Si [57] and also by doping boron in Si above the equilibrium solubility by using gas immersion laser doping. [58, 156] The recent study also demonstrated superconductivity in Al- and Ga-doped Ge(Ge:Al and Ge:Ga). [65] The critical superconducting temperatures for Ge:Al and Ge:Ga are 0.15 K and 0.45 K, respectively. The dopant concentrations for Ge:Al and Ge:Ga are reported to be $\approx$ 6 % and $\approx$ 10%. In a recent article, Shim et. al proposed the idea of fabricating superconducting circuits and Josephson junctions (JJ) in a group-IV semiconductor. [48] Realization of this proposal primarily depends on

successful realization of superconductivity in a semiconductor. Despite the higher critical temperature ($T_c \approx 7$ K) of the Ga doped Si, the material system may not be ideal for quantum information processing device fabrication as the superconducting regions lie at the Si-SiO_2 interface. [57] In quantum information, the superconducting materials and semiconductors have issues with material quality at the interfaces. The T_c of the B doped Si system is approximately 0.35 K [58,156], but an Al doped Si system is predicted to have an order of magnitude higher T_c compared to B doped Si. [66]

Semiconducting p-type delta-layers in the Al delta-doped Si can also shed light on other interesting scientific and technological areas. For instance, as a result of longer spin decoherence times due to the suppression of hyperfine interaction between holes and nuclear spins, hole-based qubit design has attracted significant interest within semiconductor quantum information processing device architectures. Stronger spin-orbit coupling in a hole-based spin qubit can enable the realization of all-electrical spin manipulation. Moreover, hole spin qubits in Si can also benefit from the absence of valley degeneracy that complicate the electrical properties in electron base qubits.

Also, p-type delta doping in combination with atomically abrupt interfaces to n-type delta doping in Si can open new avenues for realizing new transistor mechanisms that offer substantial energy reductions in switching applications along with short gate lengths and low leakage. [157] To reach atomically abrupt interfaces and the ultimate goal of single atom placement and measurement, new MBE techniques have been developed that allow the formation of delta layers, as discussed in

chapter 3. The delta layer refers to the formation of a two dimensional doped region embedded in Si, whose effective thickness is similar to the electronic Bohr radius of the dopant in Si, resulting in the electronic structure having a two-dimensional form. Despite the success of the phosphine dosing of Si(100) surfaces and subsequent epitaxial overgrowth to treat n-type dopant layers with atomically abrupt interfaces, a complementary p-type system has yet been to emerge. [32, 33, 70, 81, 158]

Therefore, our realization of a p-type delta-doped Si can benefit a variety of research disciplines. New opportunities emerge when both semiconducting and superconducting properties exist in the same crystalline Si without a different material interface.

In this chapter, the material synthesis of the Al delta-doped Si has been studied using STM, APT, STEM, and EDS. The STM images and STEM show epitaxially overgrown Si(100) with low surface defects and no stacking faults. The APT and EDS show the distribution of Al dopants in the overgrown Si layers with a width of 15 nm. The electrical properties are characterized by the mesa-etched Hall bar devices at cryogenic temperature. The majority carrier in the Al delta-doped Si(100) is measured to be the hole with a charge carrier density of 1.39×10^{14} cm^{-2}, which agrees to the estimated Al dosing density determined by the STM image. The maximum Hall mobility at 2 K is 20 cm$^2/(V \cdot s)$, which is comparable to mobilities for B:Si at similar densities.

4.2 Material synthesis

In this section, I will go through the *in situ* fabrication process of Si/Al/Si hetrostructure samples in the UHV chambers. There are two different fabrication processes, which will be called 1st generation and 2nd generation Al delta-doped samples in the following sections. The difference in fabrication process for two samples are how the Al dopants are activated. The Al dopants in the 1st gen. samples are activated in *ex situ* rapid thermal annealing (RTA) at various temperature and annealing periods. The 1st gen. samples are used to optimize the dopant activation process. Using the optimized temperature and period from 1st Gen. samples, the Al dopants in 2nd gen. samples are activated by *in situ* RTA in the UHV chamber before overgrowing Si epilayers. Therefore, the entire fabrication process for the 2nd gen. samples is done in UHV conditions, which is also crucial to minimize the chemical contamination from the chamber background gases, until the mesa-etched Hall bar devices are fabricated in a cleanroom.

4.2.1 1st generation Al delta-doped samples

In this section, the fabrication process of the 1st gen. Al delta-doped Si(100) is presented. During each step of fabrication process, the sample is inspected by STM, which are presented in this section. The 1st Gen. The Al dopants in the 1 st Gen. Al delta-doped Si(100) are activated by the *ex situ* RTA at various temperature and periods to optimize the dopant activation. The optimized temperature and time are used for the 2nd gen. Al delta-doped Si(100) to be fabricated all in the UHV

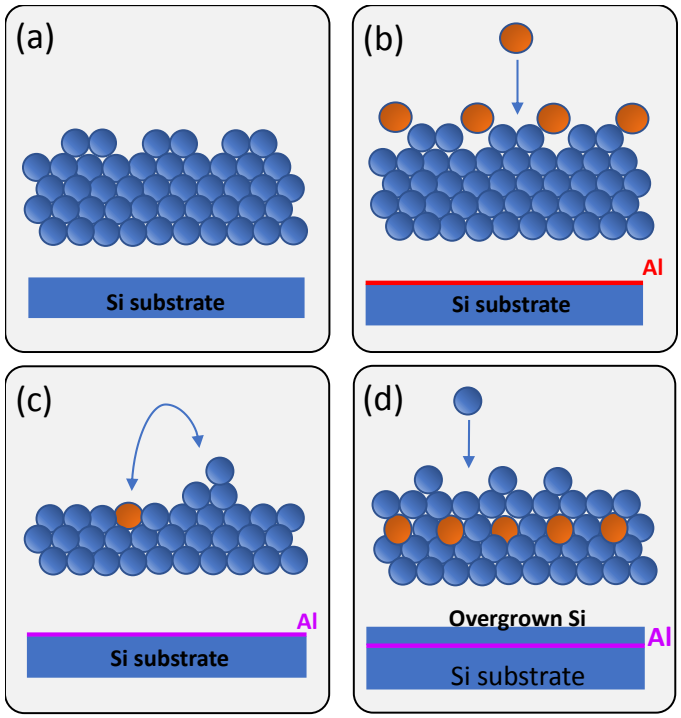

Fig. 4.1: This is a schematic drawing of fabrication process. (a) A clean (2×1) reconstructed Si(100) substrate. (b) a single atomic layer of Al atoms are deposited at the room temperature. (c) The sample is rapidly annealed to 550 °C for 1 minute. (d) 60 nm of Si epilayer is overgrown on top of Al delta layer at room temperature.

condition.

Fig. 4.1 is a schematic drawing of fabrication process. This process is same for both of the 1st and 2nd gen. Al delta-doped samples:

1. Fig. 4.1(a). A clean (2×1)Si(100) substrated is prepared by *ex situ* and *in situ* cleaning procedures as described in the section 2.3. The blue circles represent Si atoms.

2. Fig. 4.1(b). A single atomic layer of Al atoms (orange circles) are deposited on the surface at room temperature using the UHV thermal furnace as described in section 2.4.3. The deposition rate is $\approx 4.7 \times 10^{13}$ cm^{-2}·min^{-1}.

3. Fig. 4.1(c). The sample is annealed to 550 °C for 1 minute in UHV condition. The Al atoms are substituted into the Si lattice site. The substituted Si atoms form new Si islands on the surface.

4. Fig. 4.1(d). 60 nm of Si capping layers are overgrown at room temperature using the Si thermal evaporator as described in section 2.4.2. The deposition rate is ≈ 0.13 nm·min^{-1}.

Each step of fabrication process is inspected by STM as presented in Fig. 4.2. Each figure in Fig. 4.2 corresponds to a step in Fig. 4.1. Fig. 4.1(a) is taken after *in situ* cleaning at $V_{tip} = 2.00$ V, $I_{set} = 100$ pA. Clean (2×1)Si(100) surface with dimer rows are visible with very low density of surface defects. The right side of the image in Fig. 4.2(a) shows a single atomic height step edge. On the clean surface in Fig. 4.2(a), a single atomic layer of Al atoms is deposited on the surface, as shown in Fig. 4.2(b). Fig. 4.2(b) is taken at $V_{tip} = -2.00V$ and $I_{set} = 100$ pA. Single Al atoms reside on 2 (2×1)Si(100) dimers, which appear as a sphere in Fig. 4.2(b). The (2×2) ordering of Al atoms on Si(100) can be seen, indicating good crystal structure and coverage of Al atoms. The 2D density of Si atoms in Si(100) surface is 6.78×10^{14} cm^{-2} [159]; therefore, for the single atomic layer of the Al, the maximum number of Al atoms that can be put down on a Si(100) is $\approx 1.69 \times 10^{14}$ cm^{-2}. From Fig. 4.2(b), the dosing density of Al is estimated to be $\approx (1.5 \pm 0.2) \times 10^{14}$ cm^{-2}, close to the saturation density. The dark area in Fig. 4.2(b) are not surface defects. Depending on the position of Al atoms next to the neighboring Al atoms, the width of 1 (2×1)Si(100) dimer may be missing Al atoms.

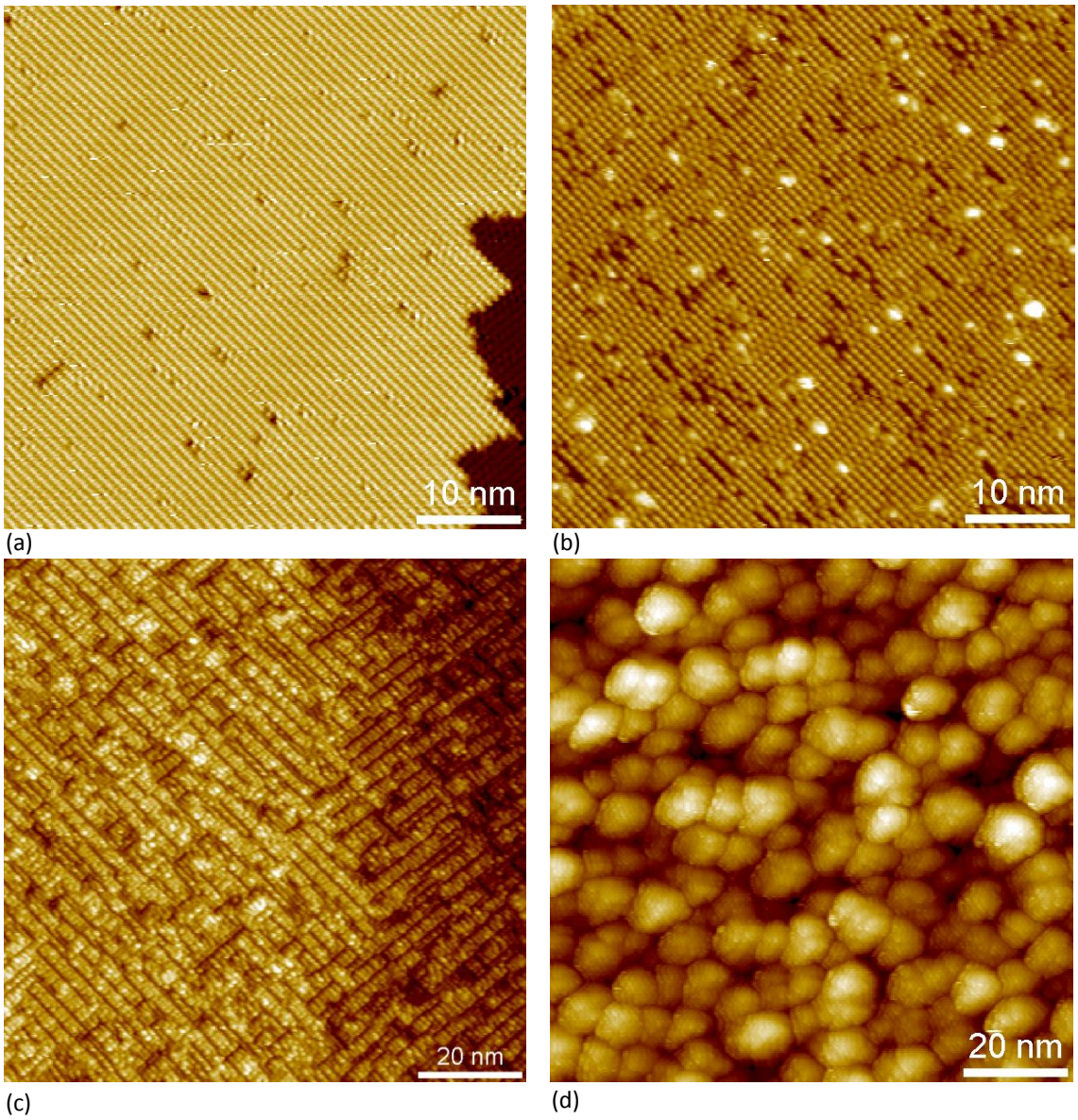

Fig. 4.2: (a) This is STM image of a clean (2×1) reconstructed Si(100) used as a starting substrate. (b) This is taken after $\approx 1.7 \times 10^{14}$ atoms/cm^2. (2×2) ordering of Al adatoms on Si(100) covered the surface as deposited on the surface (a). There are some bright spots which may be Al clusters. (c) The sample in (b) is annealed to 550 °C for 1 minute to incorporate the Al into Si(100) substrate. The incorporated Al appeared as the dark lines that are perpendicular to the underlying (2×1) dimer rows. (d) The 60 nm of Si capping layer is overgrown at room temperature. The Si capping layer is amorphous polycrystalline since the substrate temperature during the overgrowth is at room temperature.

The bright spheres on the top of single atomic layer of Al (the second layer) are the Al atoms. After Al dosing, the sample is annealed to 550 °C for 1 minute to

incorporate the Al atoms into Si lattice sites. Fig. 4.2(c) is taken after the annealing process at V_{tip} = -2.00 V and I_{set} = 100 pA. This image is a 100 nm × 100 nm area, which is larger image than Fig. 4.2(a) and (b). Fig. 4.2(c) shows three distinct atomic layers, or three terraces. The incorporated Al atoms buried into the surface appeared as dark lines. The metal atoms near the Si surface appeared as dark lines as described in section 3.3.1. Previous studies show the Al atoms on Si(100) are incorporated into the substrate at the temperature above ≈ 500 - 550 °C. After incorporation, ≈ 60 nm of Si capping layer is overgrown at room temperature at a rate of ≈ 0.13 nm·min^{-1}. This growth rate is limited by the instrument, which is explained in section 2.4.2. In order to minimize chemical contamination, such as C, O, and N, during the Si overgrowth, the chamber pressure is maintained at ≈ 2×10^{-10} Torr by two turbo pumps, an ion pump, a TSP, and a LN_2 cryoshroud, as described in section 2.1. Fig. 4.2(d) is taken at $V_{tip} = 2.00V$ and I_{set} = 100 pA. Since the overgrown Si layers are deposited at room temperature, as shown in Fig. 4.2(d), the overgrown Si layers are initially polycrystalline. In order to optimize the dopant activation process, the samples are taken out of the UHV chamber. Then, the samples are broken into smaller pieces and annealed by the RTA at various temperature and time, which is simpler and faster process than fabricating samples at various conditions in the UHV chamber due to the limitation of Si deposition rate.

From the RTA test to thermally activate Al dopants, the optimized activation temperature and time for the 1st Gen. Al delta-doped samples are 550 °C for 10 minutes in Fig. 4.3. This is determined by measuring the charge carrier density

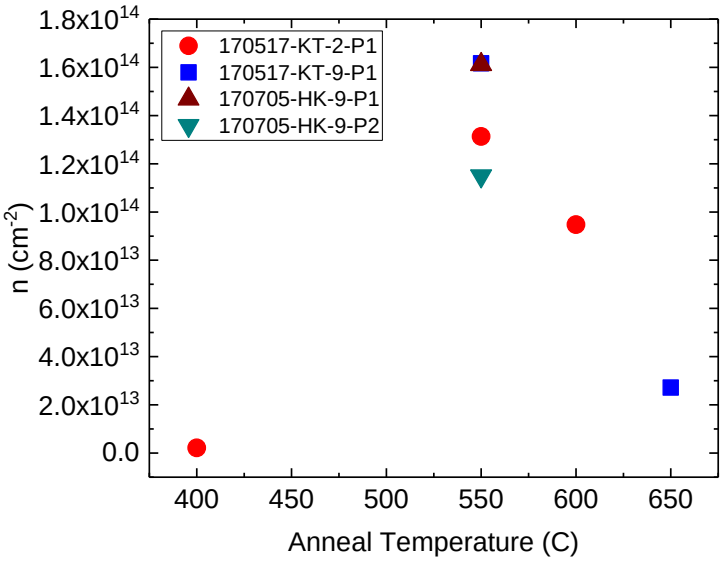

Fig. 4.3: This is a plot of the charge carrier density as a function of *ex situ* annealing temperature for 10 minutes by the RTA for the 1st generation Al delta-doped Si samples. This is measured on the mesa-etched Hall bar devices at 4 K. At an annealing temperature of 550 °C, the charge carrier density is at the maximum. At 400 °C, some Al atoms may not be activated as dopants; therefore, the charge carrier density is lower than 550 °C annealed samples. For higher temperature annealing to 600 °C and 650 °C, due to the high temperature, Al atoms may diffuse further. The profile of Al dopants may be spread out, and the tail of the dopant profile is too low to electrically conduct at 4 K. From this result, the 2nd gen. Al delta-doped Si are annealed to 550 °C for 10 minutes *in situ* in the UHV chamber.

using the Hall measurements at 4 K after fabricating the mesa-etched Hall bar devices, as described in section 4.4.2. The maximum charge carrier density of $\approx 1.6 \times 10^{14}$ cm^{-2} at 4 K is found in the samples annealed to 550 °C for 10 minutes. When annealed to 400 °C for 10 minutes, some Al dopants are not thermally activated, which results in a very low charge carrier density of $\approx 2 \times 10^{12}$ cm^{-2}. The samples annealed to 600 °C and 650 °C for 10 minutes, Al atoms may thermally diffuse, which results in the decrease of the peak Al dopant density. Also, the dopant density at the tail of the thermally diffused Al dopant profile may be too low to electrically

conduct at 4 K. Therefore, the thermal diffusion at 600 °C and 650 °C decreases the charge carrier densities compared to the samples annealed to 550 °C.

Minimizing the chemical contaminants is very important for any fabrication process. In order to reduce the chemical contamination, the fabrication process for the 2nd gen. Al delta-doped Si are all done in UHV condition until the mesa-etched Hall bar fabrication process. The next section discuss the fabrication process of the 2nd gen. Al delta-doped samples using a schematic drawing and STM images taken during fabrication process.

4.2.2 2nd generation Al delta-doped samples

Among the 1st gen. Al delta-doped samples annealed to the various temperatures and time, the sample that was annealed to 550 °C for 10 minutes are measured to have the highest charge carrier density of $\approx 1.6 \times 10^{14}$ cm^{-3} in Fig. 4.3. The whole fabrication process of the 2nd gen. Al delta-doped sample is done in UHV condition in order to minimize the chemical contamination including *in situ* 550 °C for 10 minutes. The 2nd gen. Al delta-doped sample are annealed to 550 °C for 10 minutes in UHV condition. In this section, STM images taken at each fabrication process step are presented in Fig. 4.4.

The substrates are prepared by *ex situ* and *in situ* cleaning procedure, as described in section 2.3. Fig. 4.4 is taken after high temperature *in situ* flashing at $V_{tip} = 2.00$ V, $I_{set} = 150$ pA. Fig. 4.4(a) shows a clean (2×1) reconstructed Si(100) surface with less than 1 % density of surface defects. On the right side of the image, a terrace edge and a lower terrace with (2×1) dimer rows perpendicular to the

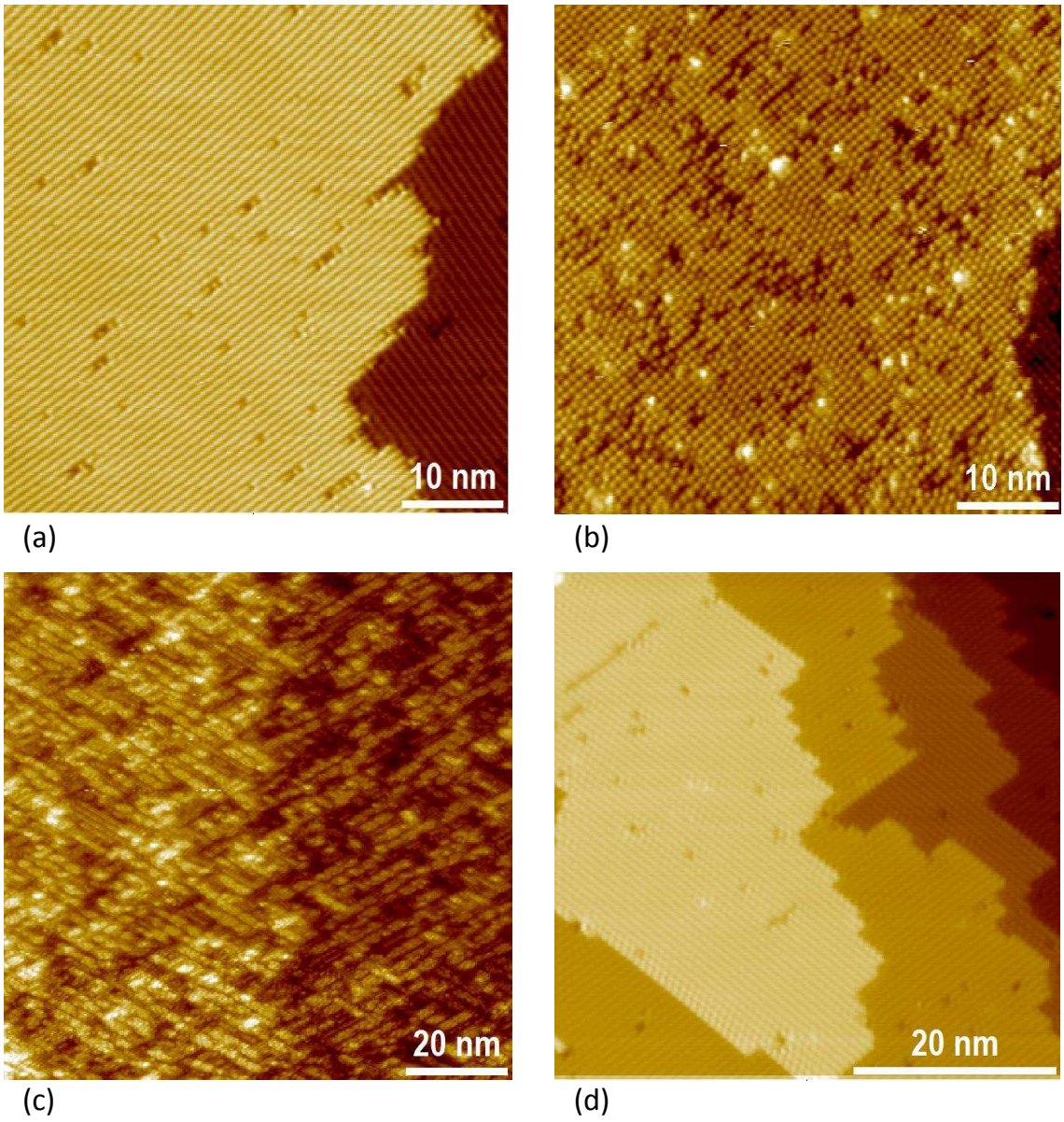

Fig. 4.4: (a)A clean (2×1) reconstructed Si(100) surface with low surface defects after high temperature *in situ* cleaning. (b)This is taken after single atomic layer of Al deposition at room temperature. (2×2) reconstructed Al atoms on the surface are visible. The estimated Al dosing density from this image is $\approx 1.5 \pm 0.2 \times 10^{14}$ cm^{-2}. (c)This is taken after 550 °C annealing to incorporate Al into the substrate. (d) After ≈ 60 nm of Si deposition at room temperature, the sample is annealed to 550 °C for 10 minutes for re-crystallization and Al dopant activation.

upper terrace can be seen. On this surface, $\approx 1.69 \times 10^{14}$ cm^{-2} of the Al atoms are deposited at room temperature at the deposition rate of $\approx 4.7 \times 10^{13}$ cm^{-2}·min^{-1}. The deposition condition is same for both of the 1st and 2nd gen. The Al delta-

doped samples. Fig. 4.4(b) shows (2×2) ordering of Al atoms on the Si(100) surface indicating good crystal structure and coverage of Al atoms. In Fig. 4.4(b), the Al dosing density of $\approx 1.5 \pm 0.2 \times 10^{14}$ cm^{-2} is same as Fig. 4.2(b). The uncertainty in Al coverage is largely due to the uncertainty in counting and determining the length scale of the STM image. In Fig. 4.4(c), the sample is subject to an anneal at 550 °C for 1 min to incorporate the Al into the Si lattice. Fig. 4.4(c) shows a step edge in the middle of the image. The dark lines on upper terrace are perpendicular to the dark lines on the lower terrace due to the Si diamond like crystal structure. The dark lines in Fig. 4.4 indicate reconstruction of surface due to the incorporated Al atoms. On this sample, ≈ 60 nm of Si is deposited at room temperature at a deposition rate of ≈ 0.16 nm·min^{-1}. Then, the sample is annealed to 550 °C for 10 minutes in UHV, which is the temperature for the maximum charge carrier density in Fig. 4.3. The *in situ* annealing process re-crystallizes and activates the Al dopants. Fig. 4.4(d) is taken after ≈ 550 °C annealing, which shows a clean (2×1) reconstructed Si(100) surface.

The STM images verify the crystallinity of the surface as shown in Fig. 4.4(d). In order to confirm the epitaxy of the sample and other defects such as stacking faults, clusters, and etc., and measure the distribution of the Al dopants, this sample is further inspected by scanning transmission electron microscope (STEM), energy dispersive X-ray spectroscopy (EDS), and atom probe tomography (APT) in the next section. STEM shows epitaxy of the overgrown Si layers with no defects. EDS and APT shows the distrubtion of Al atoms in Si layers.

4.3 Material characterization

In this section, the crystal quality and the distrubtion of Al atoms in 2nd gen. Al delta-doped samples are inspected by scanning transmission electron microscope (STEM), energy dispersive X-ray spectroscopy (EDS), and atom probe tomography (APT). First, STEM shows that the overgrown Si is crystalline near the Al enriched region. EDS and APT show a distribution of Al dopants in the Si over a similar range ($\approx$ 25 nm). The STEM presented in this section is acquired in collaboration with Dr. H. R. Zhang, Dr. L. A. Bendersky, and Dr. A. V. Davydov at NIST. The APT in this section is acquired in collaboration with Dr. F. Meisenkothen.

4.3.1 Crystal quality: STEM

The surface of the annealed overgrown Si layers is epitaxial with low surface defects as shown in Fig. 4.4. However, it is not clear if the overgrown layer has crystalline defects based on the STM images. Therefore, STEM is used to characterize the crystallinity and defects of the overgrown Si layers. This specimen for STEM is taken from a 2nd gen. Al delta-doped sample.

Fig. 4.5(a) is a large area image of a 2nd gen. Al delta-doped sample showing no visible crystalline defects. Fig. 4.5(b) is $\approx$ 60 nm from the surface where Al atoms are enriched. This image shows the Si is crystalline. The Si atoms with a diamond crystal structure is visible. Also, the interface between the substrate and the overgrown Si could not be identified indicating high quality epitaxy. The STM image in Fig. 4.4 and Fig. 4.5 verify the single crystalline overgrown Si within the

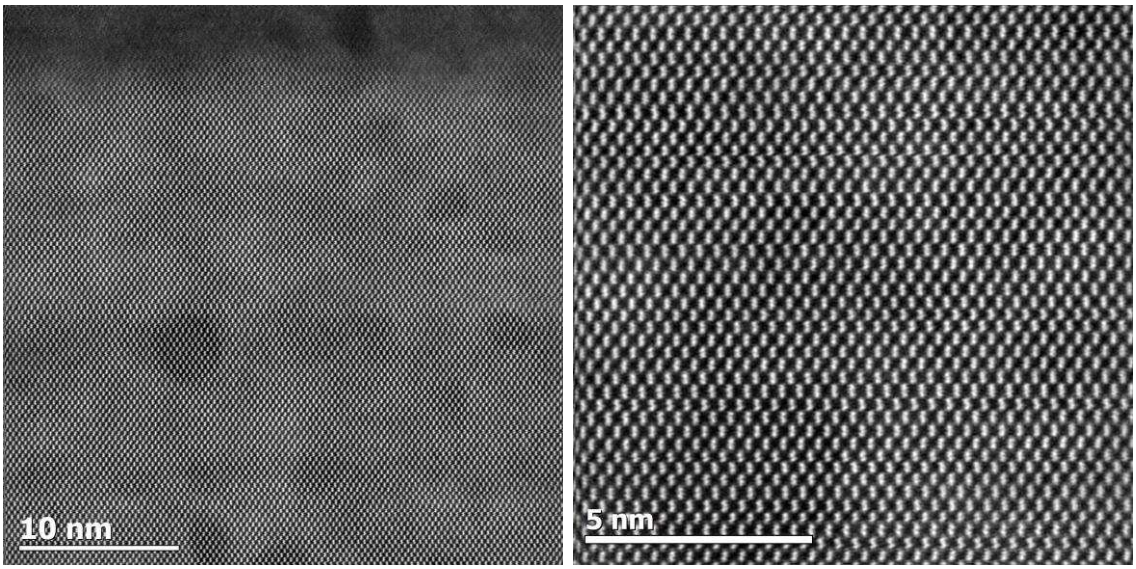

Fig. 4.5: This sample is measured on Si/Al/Si heterostructure with 60 nm overgrown Si epilayer. (a)STEM image of a large area of Si/Al/Si. The darker area at the top of Si epilayer indicates some amorphous Si which might be casued during ex-situ Hall bar device fabrication process in Fig. 4.9 or sample preparation for TEM. (b) This is taken near Al doped region, which shows good Si crystal structure.

Al delta-doped region.

Al dopant distrubtion is measured on this STEM specimen using the EDS in Fig. 4.5(b), which is presented in the following section.

4.3.2 Thermal Al dopant diffusion in Si measured by EDS and APT

The EDS is an analytical technique used to analyze the chemical contents of a specimen with atomic or nano scale. The EDS detects the X-rays emitted from a specimen irradiated by the electron beam that is also used in the STEM, in our case to characterize the chemical contents. EDS, combined with STEM can map the chemical contents in a specimen. The EDS data in Fig. 4.6 are from line cuts

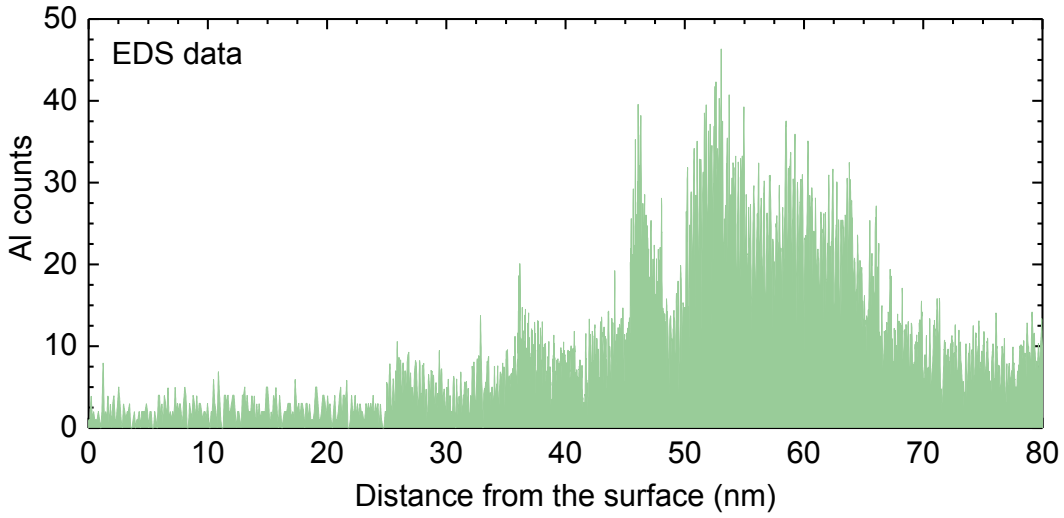

Fig. 4.6: This plot shows the density of Al atoms vs. position measured using energy dispersive x-ray spectroscopy (EDS) from a sample in Fig. 4.5. This is the sum of 5 EDS line cuts. As expected the peak value of Al signal is near the interface between Si epilayer and the substrate. However, the distribution of Al seems to be $\approx$ 15 nm.

in the vertical direction in Fig. 4.5 to characterize the Al distribution in the Al delta-doped sample.

Fig. 4.6 shows the EDS signal of Al in the Al delta-doped Si as a function of the distance from the surface in the STEM image. Fig. 4.6 is the sum of 5 line cuts in Fig. 4.5(b). The peak Al counts in Fig. 4.6 is $\approx$ 55 nm from the surface, which is estimated thickness of the overgrown Si in section 4.2. Fig. 4.6 shows a distrubtion of Al dopants with $\approx$ 25 nm. Also, the majority of Al dopants are diffused into the overgrown layer.

The Al dopant distribution in the same sample is also inspected by APT. APT is also the analytic tool to characterize the chemical content. The advantage of APT is the capability to map the chemical contents in 3D at the atomic scale. For APT, unlike the thin slice of a specimen for STEM, the specimen is prepared in the form

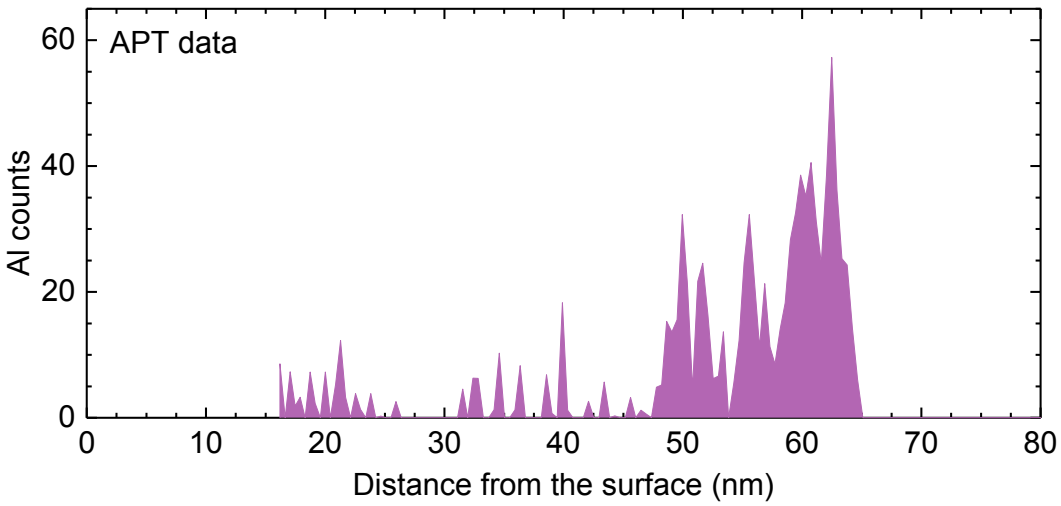

Fig. 4.7: This is the Al contents as a function of a distance from the surface in the same sample as Fig. 4.5 and 4.6. The peak Al concentration is at ≈ 60 nm from the surface as expected. This also shows a distribution of Al with a width of ≈ 17 nm.

of a sharp tip. By applying high voltage or high power laser on a sharp tip, an atomic layer on the surface is evaporated. The evaporated atoms are accelerated to the detector by apply high voltage. From the time of flight mass spectrometry, the chemical contents of the evaporated atoms can be analyzed. By analyzing the layer by layer of the specimen, a 3D map of the chemical contents can be measured by APT.

Fig. 4.7 shows the Al contents measured by APT as a function of depth from the surface in the same sample as Fig. 4.5 and Fig. 4.6. Fig. 4.7 shows the peak Al counts at ≈ 60 nm from the surface. On average the APT extracted Al atom density is approximately $(1.2 \pm 0.3) \times 10^{14}$ cm^{-2}, and shows that the Al dopants have distributed over a width of ≈ 17 nm. The apparent decrease of the average Al density in APT data compared to the STM estimation due to the difficulty in

properly modeling the background in the APT concentration profile. The APT data also shows diffusion of Al dopants toward the overgrown Si layer similar to the EDS data. The Al delta-doped samples are annealed to 500 °C for 10 minutes at the last step of fabrication to re-crystallize the polycrystalline Si grown at room temperature as described in section 4.2. Especially, for the overgrown polycrystalline Si, more crystalline defects are seen than in the FZ i-Si(100) substrate. During the 550 °C annealing process, the Al dopants may be diffused to the overgrown Si. The prefactors, D^0, and activation energies, E_a^0, of bulk diffusion of Al in Si are 1.385 $cm^2 \cdot s^{-1}$ and 3.41 eV, respectively. [68] However, the extrinsic effects, such as the enhancement of diffusion by defect interaction with electric field effects needs to be considered for diffusion in Si, which are the D_0^1 of 2480 $cm^2 s^{-1}$ and E_a^1 of 4.20 eV. [68, 160]. The diffusion coefficient with extrinsic effects and dopant concentration, N, can be written as $D(N) = h\left[D^0 + D^1 \frac{N}{n_i}\right]$. [161] h is the field enhancement factor, and h =2 at $N \approx 1\times\ 10^{20}$ cm^{-3}. If the thermal diffusion is modeled with a Gaussian profile with the E_a and D_0 of Al bulk diffusion in Si, assuming the initial peak Al density of $\approx 1.6\times10^{21}$ cm^{-3}, the estimated diffusion width of Al is $\approx$ 15 nm, which is similar to the EDS and APT data.

The EDS and APT data both indicate the diffusion of Al dopants toward the overgrown Si layers, probably due to 550 °C annealing. In order to minimize the thermal diffusion of Al dopants in Si, the overgrown Si layer can be deposited at slightly elevated temperature of $\approx$ 300 °C - 325 °C instead of room temperature. Based on the estimation using the Al bulk diffusion in Si mentioned above, the Al dopants in Si does not diffuse at 300 °C - 350 °C. Also, as explained in chapter 3, by

keeping the growth rate of Si small at ≈ 0.4 nm·min^{-1} or lower, the Si capping layers can be epitaxially overgrown at 300 °C - 350 °C. [68, 69] For the next generation Al delta-doped Si, after 550 °C to incorporate Al into the substrate, the substrate is held at 300 °C - 350 °C during Si overgrowth to reduce the Al dopant diffusion while maintaining the epitaxial quality of the Si capping layers.

4.4 Electrical properties - Hall measurements

In this section, I will explain the Hall measurement technique used to characterize the electrical properties of the Si/Al/Si heterostructures, such as the charge carrier type, density, and Hall mobility. Then I will show the charge carrier density, Hall mobilities of 1st and 2nd generation samples. The data in Fig. 4.3 is measured on the same mesa-etched Hall bar devices.

4.4.1 Hall effect measurements

The Hall effect measurement has a long history starting with Edwin H. Hall in 1879. The Hall effect enables direct measurement of the charge carrier type and density, Hall mobility, and the quality of materials. The Hall effect measurement uses the Lorentz force, which is the combination of the electric force and the magnetic force. In Fig. 4.8, as the charge carrier moves along the electric field, $\mathbf{E}$ is perpendicular to the magnetic field, $\mathbf{B}$, the charge carriers experience the Lorentz force $-q \cdot \mathbf{v} \times \mathbf{B}$ where q is the elementary charge, $\mathbf{v}$ is the particle velocity. Then, the total force is $-q(\mathbf{E} + \mathbf{v} \times \mathbf{B})$. For the bar-shaped sample shown in Fig. 4.8, due

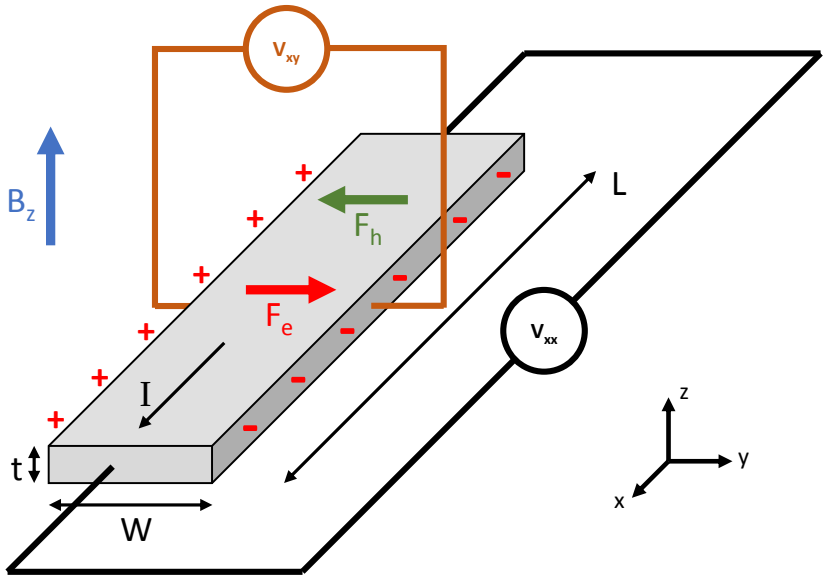

Fig. 4.8: This is a schematic drawing of Hall effect caused by the Lorentz force on moving charges. The charges built up on the side of the current path in a sample causes the potential difference

to the Lorentz force, the electrons would be drifted toward the side of the sample in y-direction. Holes are drifted toward the opposite direction in y-direction. This results in the potential drop, V_{xy} across the transverse direction of the sample, which is called the Hall voltage. The relationship between the Hall voltage and the charge carrier density is explained in the following equation:

$$V_H = IB/qnt = IB/qn_s \tag{4.1}$$

$$n_s = IB/qV_H \tag{4.2}$$

where I is the current, t is the sample thickness, n_s is the sheet density. From the equation 4.1 with known values of I, B, and q, the charge carriers density, n_s can be measured.

The sheet resistance, $R_\square$ of the semiconductor can be measured by 4 point measurements. Using the euqation, $\mu = 1/(qn_sR_\square)$, the Hall mobility can be deter-

mined.

The Hall effect for the Al delta-doped Si are measured at cryogenic temperature down to 10 mK. The mesa-etched Hall bar devices are used for the Hall effect measurements. The fabrication process of the mesa-etched Hall bar devices are presented in the next section. The electrical properties, such as charge carrier density, the Hall mobility, and the sheet resistance are presented later in the last section 4.4.3 of this chapter.

4.4.2 Device fabrication - Hall bar

In this chapter, the fabrication process of the mesa-etched Hall bar devices is presented. Fig. 4.9 shows a micrograph of the mesa-etched Hall bar devices and Van der Pauw devices. The yellow circled devices are characterized in this chapter. Two squares with bright rectangles at the top of the micrograph are the Van der Pauw devices, which has not been used in this work. These are the same sample used for STEM, EDS, and APT in section 4.3. The mesa-etched Hall bar devices(50 μm $\times$ 1000μm) with multiple terminals with Al contact pads, which are bright rectangles on each terminal, as shown in Fig. 4.9. Each terminal has mesa-etched holes that are filled with Al metal to make electrical contacts between Al contact pads and Al delta-doped layers buried in Si.

Shown in Fig. 4.10, are the schematic drawings of fabrication process:

1. Fig. 4.10(a): This a schematic drawing of Al delta-doped Si as grown in the UHV chamber. The Hall bar devices with holes on the terminals and Van der

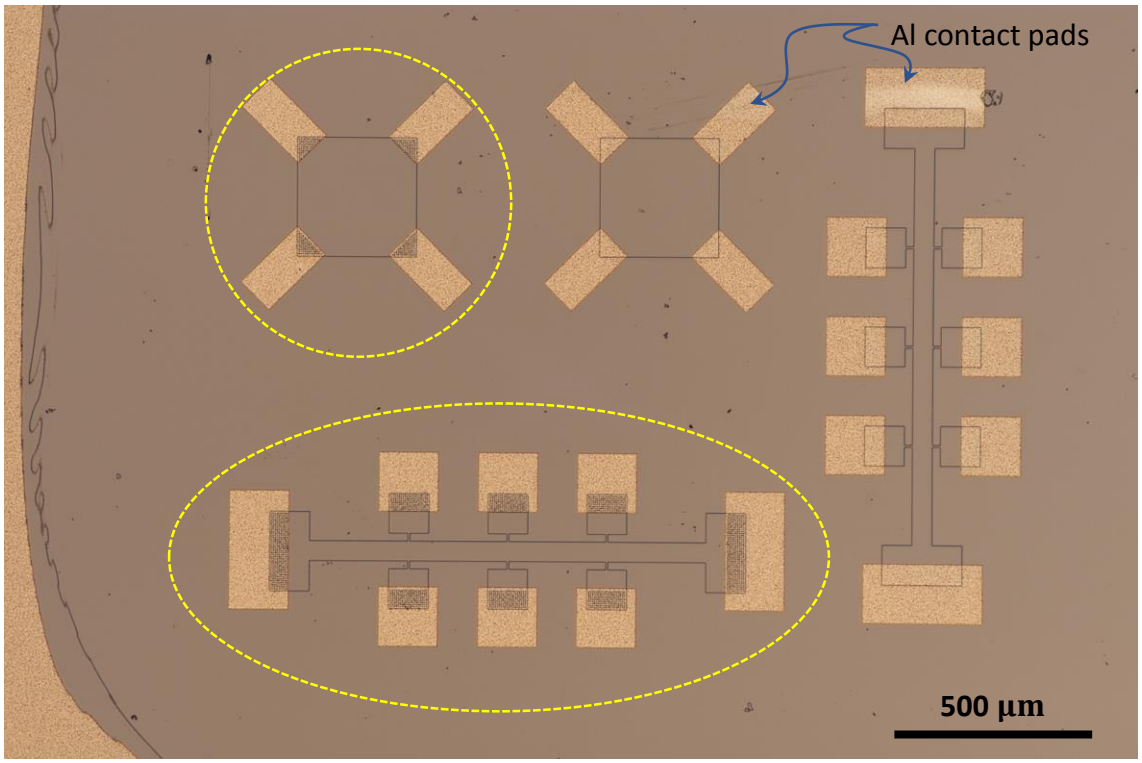

Fig. 4.9: This shows two Hall bar devices and two Van der Pauw devices. All devices are mesa-etched. The bright rectangles on the devices are Al contact pads. The yellow circled devices are used in this chapter. Both devices have etched via holes under the Al contact pads to facilitate electrical contacting.

Pauw devices are patterned with photolithography for mesa-etching.

2. Fig. 4.10(b): The sample in an oxygen plasma is mesa-etched in a reactive ion etching (RIE) chamber. The depth of the etching is $\approx$ 100 nm, which is well below the Al enriched region as confirmed by EDS and APT.

3. Fig. 4.10(c): $\approx$ 300 nm thick Al metal layer is sputter deposited on to the mesa-etched sample.

4. Fig. 4.10(d): The Al metal layer is etched away except in the metal contact areas defined with photolithography. Finally, the samples are subjected to an RTA at 350 °C for 30 minutes in N_2 to establish the electrical connection

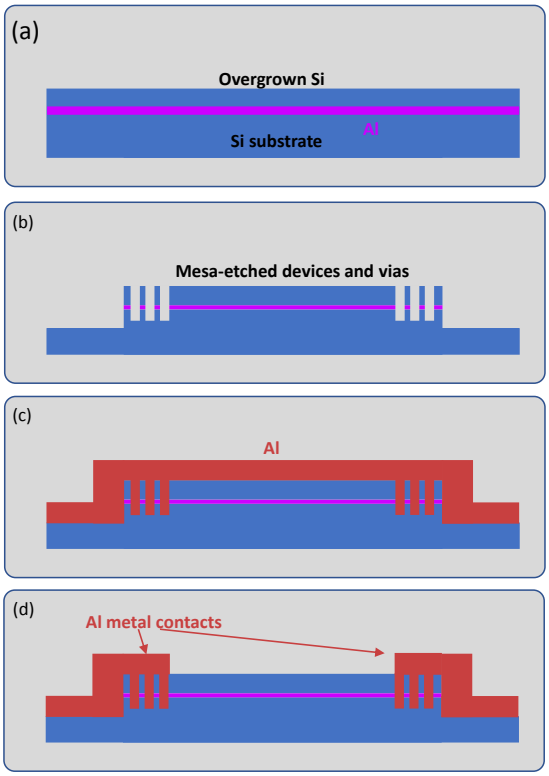

Fig. 4.10: (a) This is a schematic cross section drawing of Si/Al/Si heterostructure as grown in the UHV chamber. (b) After photolithography, the Hall bar devices and the Van der Pauw devices are mesa-etched below the Al delta-dopes layer. (c) The Al is then deposited on a chip. (d) The Al is etched except in the metal contact areas defined with photolithography.

between the buried Al delta layer and the Al metal contacts.

Fig. 4.9 shows the completed Hall bar devices and Van der Pauw devices. In the following section, the yellow circled mesa-etched Hall bar device in Fig. 4.9 is characterized by Hall effect measurements.

4.4.3 Charge carrier densities and Hall mobility

In this section, the electrical properities of the Al delta-doped Si, such as charge carrier density, Hall mobility, and the resistance per square ($R_{\square}$), are characterized using the mesa-etched Hall bar device in Fig. 4.9. In order to freeze out the electrical

conduction throught the substrate and the overgrown Si, the sample is cooled down to 50 mK as showin in Fig. 4.11. The same sample is characterized with STM, STEM, EDS, and APT in the previous sections.

Fig. 4.11(a) is the same Hall bar device circled in Fig. 4.9. Fig. 4.11(a) shows the experimental set-up of the Hall effect measurement. The DC current I_{SD} is applied from the top electrode to the bottom electrode. The Hall voltage, V_{xy} is measured between the bottom two side electrodes. For the sheet resistance measurement and the magnetoresistance, R_{xx}, the voltage drop, V_{xx} across the far electrodes on the left side in the Fig. 4.11(a) are measured. A perpendicular magnetic field, $\mathbf{B}$, is applied out of the plane. For the resistance of the 2D material, the resistance per square, $R_{\square}$ is the sheet resistance divided by the number of squares between two electrodes on the left marked with V_{xx}.

Fig. 4.11(b) shows the resistance per square, $R_{\square}$ as a function of temperature for Hall bar device. The higher temperature ($T \geq 3$ K) data were measured in a closed cycle refrigerator, while warming up the system and low temperature ($T \leq 3$ K) data were measured in a cryogenic free dilution refrigerator (DR). The sample did not exhibit superconductivity down to the base temperature ($T = 10$ mK) of the DR. As shown in Fig. 4.11(b), $R_{\square}$ rapidly increases until temperature reaches 30 K with decreasing temperature. Below 30 K, the substrate becomes insulating. Then, $R_{\square}$ below 30 K shows just the conduction through the Al delta-doped region.

Fig. 4.11(c) is the Hall resistance, R_{xy} at 2 K. The positive slope of R_{xy} indicates that the dominant charge carriers contributing to the transport are in fact holes. The charge carrier density, n extracted from the slope of Fig. 4.11(c) using

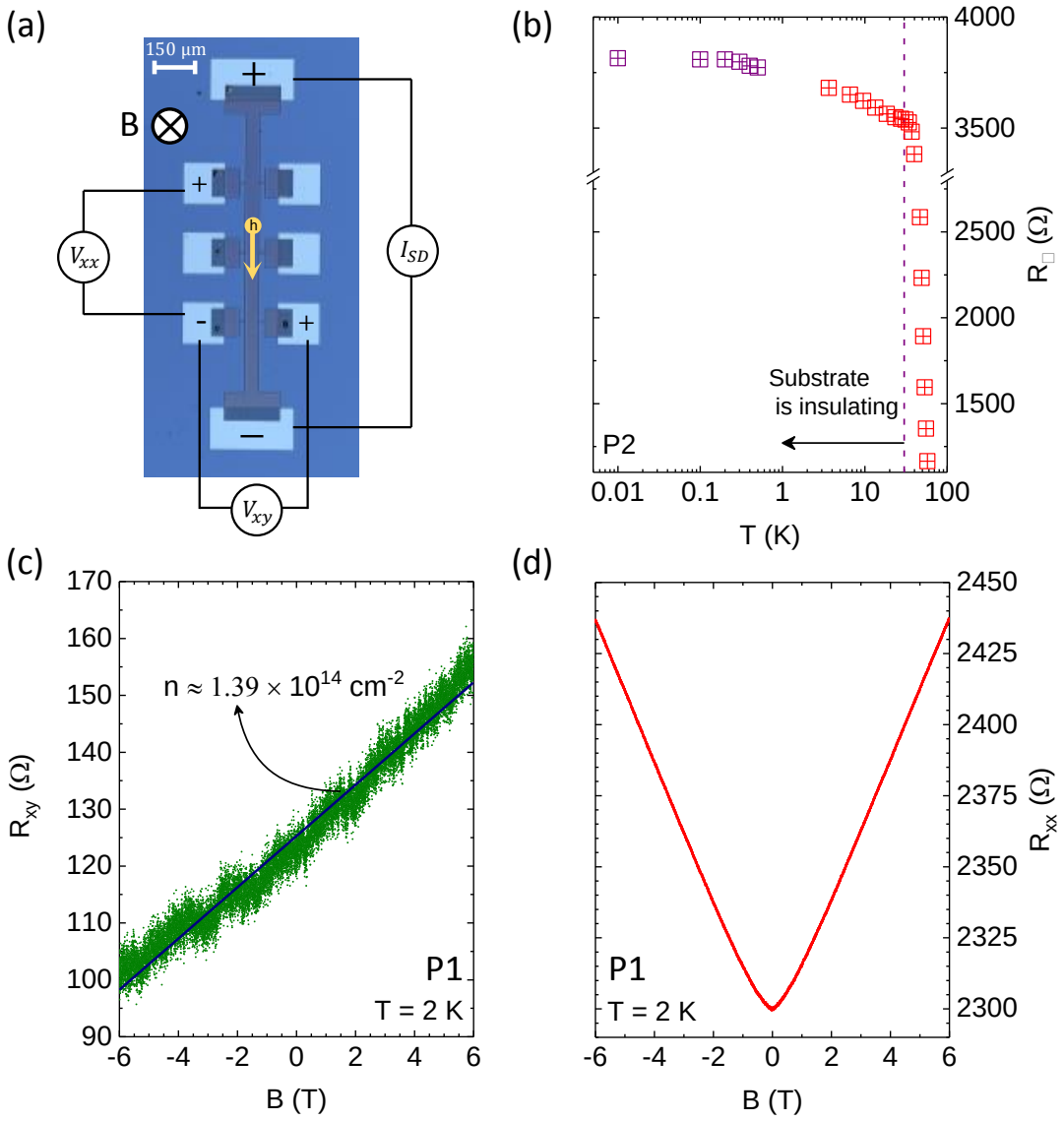

Fig. 4.11: (a) This is an optical image of a mesa-etched 50 μm wide Hall bar device. It shows a schematic of the measurement circuit. (b) The resistance per square ($R_{\square}$) as a function of the temperature (K) down to 10 mK is shown. Below the dashed line at 30 K, the substrate is insulating and the delta layer reaches a finite resistance. (c) The Hall resistance (R_{xy}) and (d) the magnetoresistance (R_{xx}) measured at 2 K. R_{xx}, near zero B field, deviates from a parabolic nature while at $B < 1$ T, R_{xx} demonstrates fairly parabolic behavior. [162] This is taken from Ref. [163].

Eq. 4.1 is $\approx 1.39 \times 10^{14}$ cm^{-2}. The Hall mobility is extracted from $R_{\square}$ and μ is ≈ 20 cm$^2/V \cdot s$. The mobility for this Al delta-doped Si is comparable to mobilities

reported for the B delta-doped Si at similar densities of ≈ 20 cm$^2/(V \cdot s)$ at p-type doping density of 5×10^{14} cm^{-2}. [156] The relative uncertainties for both n and μ are less than 1 %. The extracted charge carrier density corresponds to approximately (0.93 ± 0.1) hole per Al dopant atom. In Fig. 4.11(d), at low B field < 1 T, R_{xx} demonstrates fairly parabolic behavior of the 2D conducting channel. [162] However, near zero B field, R_{xx} deviates from a parabolic nature. Then, at high B fields ($B > 1$ T), R_{xx} deviates from parabolic to linear. The linear behavior can be due to polycrystallinity or topological effects. [164–167] Aside from these, a strong field, non saturating linear magnetoresistance is also proposed for crystals with inhomogeneities. Polycrystallinity and inhomogeneities in the material (inhomogeneities in distribution of Al dopants) are possible for observed linear magnetoresistance. [168]

We have successfully fabricated the Al delta-doped Si, which is comparable to the similar B delta-doped system. We found that the majority charge carrier in the Al delta-doped Si is hole. We also achieved close to the unity dopant activation. STM and STEM data show good epitaxial quality with the low density of surface defects and no defects in the crystallinity. This sample show a good electrical conductivity down to $T = 10$ mK. However, we have not observed superconductivity. According to the APT and assuming a 2D density of Al atoms to be $\approx 1.5 \times 10^{14}$ cm^{-2} (maximum density of Al atoms according to STM analysis), the estimated upper bound for 3D density of Al atoms in Si is approximately 0.2% (0.1%). But the estimated 3D density of Al in these samples, considering APT data, is only approximately a tenth of what is predicted to observe superconductivity in B:Si heterostructure assuming similar conditions apply for Al delta-doped Si. [169] As

mentioned in section 4.3.2, by considering the extrinsic effects in Al diffusion due to the polycrystalline Si, the high concentration of Al dopants, the enhancement of diffusion by defect interaction of electric field effects, can diffuse more into the overgrown Si as measured in EDS and APT. Therefore, even though the initial 2D density of Al atoms is $\approx 1.5 \times 10^{14}$ cm^{-2}, the final 3D Al density falling below the critical density predicted for superconductivity due to re-distribution as the dominant reason for not observing superconductivity in these samples.

In the future, increasing the growth temperature (e.g., 300 °C - 350 °C) of the Si capping layers will enable to achieve crystallinity in the overgrown Si layer, and constrain the Al dopants to a narrow region to achieve a higher 3D density of Al in Si.

4.5 Summary

I have successfully synthesized a quasi two-dimensional hole gas in Si by using a monolayer of Al sandwiched in Si. STM and STEM show a clean epitaxial Si(100) surface with low density of defects and crystallinity with no defects in the Al enriched region, respectively. Using mesa-etched Hall bar devices, the charge carrier density and the Hall mobility are measured to be $\approx 1.39 \times 10^{14}$ cm^{-2} and ≈ 20 cm$^2/(V \cdot s)$, respectively, which is comparable to the similar B delta-doped Si. The extracted charge carrier density corresponds to approximately (0.93 ± 0.1) hole per Al dopant atom. The $R_\square$ measured as a function of temperature does not show signs of superconductivity. The redistribution of Al dopnts over approx-

imately 17 nm according to APT data reduces the 3D Al density to only 10 % of the predicted density to observe superconductivity in B doped Si assuming similar conditions apply for Al delta-doped Si. This dopant diffusion is the main cause for not observing superconductivity in these devices. In the future experiments, parameters such as the Si overgrowth temperature and annealing temperature will be optimized to reduce the Al distribution width and increase the final 3D Al density, while maintaining the crystallinity of the overgrown Si.

Chapter 5

in situ detection of pre-implanted contacts for STM lithography using real time STM/STS

5.1 Introduction

The pre-implanted contacts with photolithography in a wafer scale has been demonstrated to fabricate the nanowires using STM lithography and phosphine dosing. [34] The pre-implanted contacts dramatically simplifies the contemporary strategies for aligning and contacting STM patterned nanodevices. Specifically, no sample specific patterning or alignment is required outside of the STM patterning step, in contrast to typical contacting schemes. Our strategy does not use any electron beam lithography, at any stage. Furthermore, the bulk of the *ex situ* processing is done on the wafer scale, i.e., the alignment marks, implant and shallow etch features are all performed at the wafer level. Since a typical 100 mm wafer can yield $\approx$ 100 of the 4 mm $\times$ 10 mm chips used in the vacuum processing, the productivity benefit of the wafer scale processing can be enormous after only a few

chips. Finally, since this approach provides overlap between two conducting planes, rather than drilling holes or slicing faces through the delta layer plane, the quality and reliability of the contacts may be better once it is optimized. But, in order to realize this approach, detailed knowledge of the dopant diffusion for the complex thermal histories used in the UHV sample preparation is needed.

For STM lithography with hydrogen passivation, the substrate needs to be flash annealed in UHV condition as described in section 2.3.2, which causes thermal dopant diffusion. In this chapter, the thermal budget of high temperature flashing for the pre-implanted wires are studied using P implanted wires. The typical high temperature flashing procedure in UHV does not cause electrical shorting between pre-implanted wires.

In order to make electrical connection between the pre-implanted wires and STM patterned devices, the pre-implanted wires needs to be degenerately doped near the surface where the pre-implanted wires and the STM patterned devices are electrically connected. Therefore, the shallow ion implantation are perforemed with a dose of 5×10^{15} atoms/cm^2 at an ion energy of 30 keV, which estimates the peak concentration of $\approx 1 \times 10^{21}$ atoms/cm^3 at a mean depth of $\approx$ 50 nm from the surface. Then, as a first step of STM lithography, the pre-implanted wires need to be identified using STM. One of the technical challenges is to find a same place again in STM system when the sample is moved between chambers at different fabrication process steps such as H passivation, dopant dosing, and Si overgrowth. Also, the maximum field of view of STM is typically 15 μm by 15 μm. I used the shallow etched lines ($\approx$ 100 nm deep) and high magnification optical telescope ($\approx$ 5.62X) to

align the STM tip to the same area for STM lithography after being moved between chambers.

For STM lithography, the pre-implanted wires need to be identified using STM. The real-time lock-in technique is used to detect the change in the local density of states between the substrate and the pre-implanted wires by mixing an AC modulation of the gap voltage as explained in section 2.2.2. The difference in doping concentrations between the pre-implanted wires and the substrate results the change in the Fermi energy position in bulk. [170] For n-type Si, the relative Fermi energy, E_F, to the mid gap of E_i can be deduced from the carrier density, n, based on the relationship: $E_F = E_i + kT \cdot ln(\frac{n}{n_i})$. For Si, n_i is 1.5 $\times$ 10^{10} cm^{-2} at 300 K. E_i is the mid gap of Si. [170] Therefore, the pre-implanted wires can be identified by measuring the change in the local density of states due to the change in the Fermi energy position. As described in section 2.2.2, the lock-in technique allows us to measure the $\frac{\partial I_T}{\partial V}\big|_{V_{DC}}$ simultaneously while measuring STM topography. In this chapter, the various dopants(P, As, and B) and substrates(i-Si, n-Si, and p-Si) are tested to detect the pre-implanted wires using the lock-in technique with STS. The pre-implanted wires with P and As show good contrast in the lock-in signal. However, B is apparently, thermally diffused or out-diffused to vacuum during high temperature flashing. Kelvin probe force microscope (KPFM) verifies the lock-in technique with STS. This imaging method substantially reduces the risk of misalignment between the STM and implanted patterns.

In the last section, a nano-wire is fabricated using the pre-implanted wires and STM lithography with P dosing. The electrical measurement at low temperature

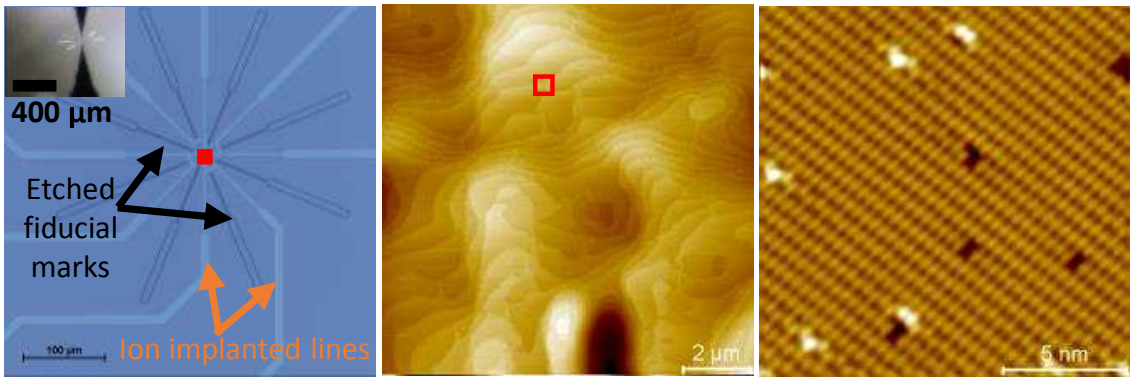

Fig. 5.1: (a) is the optical image of a complete device. The black arrows indicates the etched fiducial lines. The orange arrows indicate the ion implanted regimes. The inset shows that the STM tip is aligned to the center of the fiducial patterns using its reflection on a Si chip. (b) is the large area scan (12 μm $\times$ 12 μm). It is taken at the red square in (a). (c) This is taken at a red square in (b). It shows a clean (2×1) reconstructed Si(100) with only a few defects.

shows linear $I(V)$ characteristic of the STM fabricated nano-wire made of P dopants.

5.2 Pre-ion planted sample fabrication process

In this section, the fabrication process for ion implanted lines and fiducial patterns are explained. The entire fabrication process was done at the wafer scale until the *ex situ* cleaning to load the chips into the vacuum chamber. Devices described in this section are also used in chapter 6. [34] Fig. 5.1(a) shows the optical image of a complete device before being introduced to the vacuum chamber. The mean depth of the etched fiducial patterns is $\approx$ 50 - 100 nm from the surface. Then, the substrate is cleaned by RCA cleaning procedure to remove organic and metal contaminants. After cleaning, the regions for ion implantation are patterned by photolithography. Patterned substrates are then sent for external commercial ion implantation, specifically, a dose of 5×10^{15} atoms/cm^2 was implanted at an ion

energy of 30 keV. Since the STM patterned devices are nearly two dimensional, for a good electrical connection between STM patterned devices and the ion implanted electrodes, the dopant concentration of the electrodes at the surface should be degenerate. Therefore, the low energy ion implantation parameters are used. According to SRIM, the peak concentration of the implanted ions is $\approx 1 \times 10^{21}$ atoms/cm^3. Due to the damage during ion implantation, the ion implanted region is still visible in Fig 5.1(a). However, the *in situ* cleaning explained in section 2.3.2 such as high temperature flashing recrystallizes and heals the damage from ion implantation so that the ion implanted regimes are not visible after *in situ* cleaning.

The device in Fig. 5.1 shows 4 electrodes with 2 lines for each electrode. The etch fiducial patterns are visible through the coarse alignment telescope used to orient the STM tip with the sample, as shown in the inset of Fig. 5.1(a), where the tip can be seen entering from the bottom of the image and its reflection from surface goes out the top. Typically, the alignment accuracy is better than 5 μm as determined from the offsets from multiple, independent tip approaches. The same location can be found again using microscopic features in the STM within $\approx$ 20 minutes. Fig. 5.1(b) is a STM scan of 12 μm by 12 μm area taken at a red square in Fig. 5.1(a). During high temperature flashing, the damage from the ion implantation and etched fiducial patterns cause the wavy and complex step structures. A dark valley at the bottom of Fig. 5.1(b) is one of the implanted line. Fig. 5.1(c) is a small area scan taken at the red square in Fig. 5.1(b). It shows a clean (2×1) reconstructed Si(100) surface.

On a same chip, two different wire configurations are fabricated as shown in

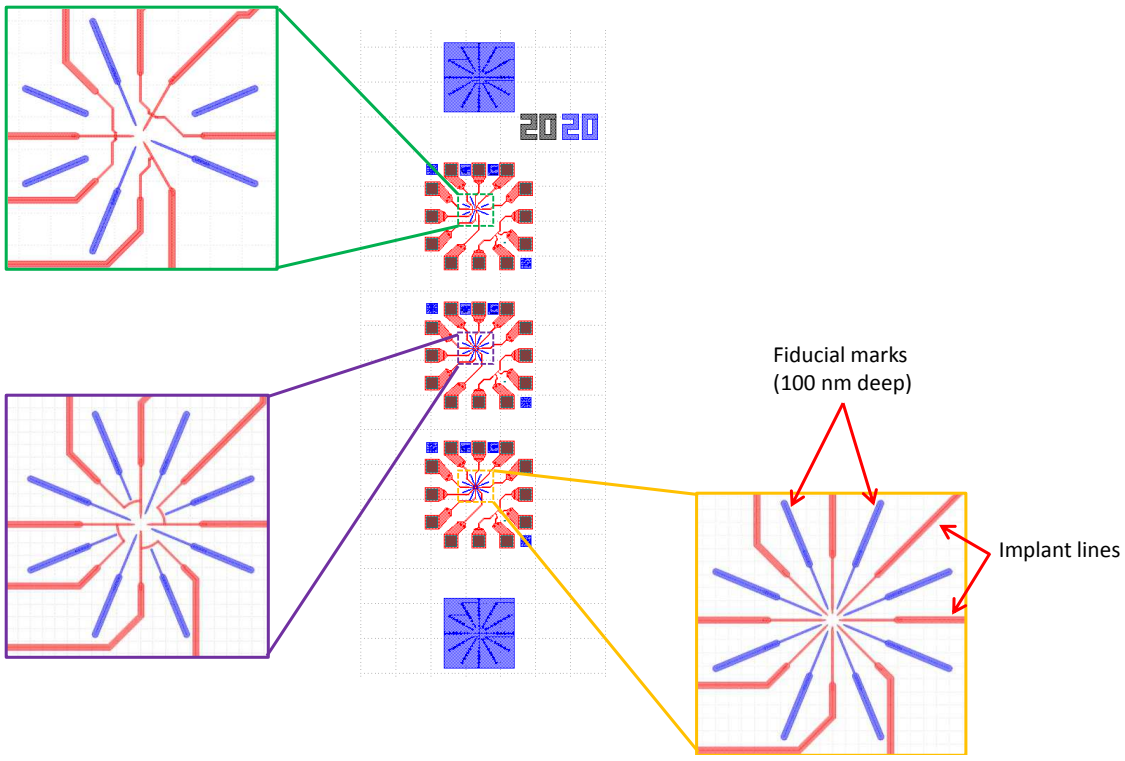

Fig. 5.2: This is a layout of the devices with different electrode configuration on a chip.

Fig. 5.2. The detail fabrication process is as follow:

1. RCA cleaning to remove the organic and metal contaminants.
2. Photolithography for ion implantation.
3. Ion implantation: dose: e.g.,5×10^{15} atoms/cm^2 at 30 keV for P, B, and As.
4. RCA cleaning
5. Photolithography for deep etching of Si.
6. $\approx$ 100 nm deep reactive ion etching (RIE) etching.
7. Remove photoresist.
8. Spin the photoresist.

9. Dice the wafer into 4 mm by 10 mm chips.

When the chips are introduced to the chamber, the chips are prepared as described in section 2.3.2.

To test the thermal dopant diffusion during high temperature flashing as explained in section. 2.3.2, the separation of the electrodes varies from 5 μm to tens of μm. From Ref. [34], the typical high temperature flash does not cause shorting or electrical leakage with 2 μm separation at 4 K. In the next section, using the effective thermal activation parameter D^*_Σ, the various flash annealing temperature and periods are tested with the P implanted samples. The As and B implanted wires is discussed.

5.3 Thermal dopant diffusion

As described in section 2.3.2, in order to fabricate atomically precise dopant devices in Si using STM lithography, the high temperature flashing in the UHV condition is required to remove the chemically grown SiO_2 layer and reconstruct the Si(100) surface. The high temperature flashing significantly diffuses the dopants in the pre-patterned region as shown in Fig. 5.1. In order to use the pre-implanted lines for electrodes, all the wires must remain electrically isolated from each other.

The complexity and variability of the in-vacuum thermal processing from run to run complicates quantitative comparison between samples, which is important for determining how sensitive the selected spacing is to the details of a particular thermal process. Table 5.1 summarizes the approximate aggregate activation of

Tab. 5.1: For each sample, the integrated thermal activation parameter D^*_Σ is shown in the second column, followed by the aggregate time spent at each 1000 °C, 1100 °C, and 1200 °C. Using the D^*_Σ parameter for each sample, we calculate equivalent activation times (t_{eq}) if the sample had sat at a single temperature of either 1100 °C or 1200 °C. The next two columns provide single dopant bulk and surface diffusion lengths using $E_a = 3.5$ eV [171] for 3D, $E_a = 0.94$ eV [172] for 2D and $D_0 = 3.85$ cm^2/s [173] for both bulk and surface diffusion. Finally, the equivalent time at 1100 °C is used to estimate the spreading of the implanted dopants "edge" using an online diffusion calculator, corresponding to a dopant density of 3.8×10^{18} cm^3.

Sample	D^*_Σ	Total time (s) [a]			t_{eq} (min) [b]		Diffusion length (μm) [b]		l_c (μm) [c]
		1000 °C	1100 °C	1200 °C	1100 °C	1200 °C	l_{3D}	l_{2D}	
D1	0.084 ± 0.003	60	0	0	0.10	0.01	0.02	2.09×10^3	-
D2	2.5 ± 0.3	55	48	23	2.81	0.38	0.10	3.99×10^3	0.23
D3	5.1 ± 0.4	69	54	45	5.86	0.79	0.14	5.73×10^3	0.34
D4	6.1 ± 0.4	0	97	51	6.97	0.94	0.15	5.78×10^3	0.37
D5	7.5 ± 0.6	0	7	60	8.56	1.15	0.17	4.53×10^3	0.43
D6	9.1 ± 0.5	0	151	93	10.34	1.39	0.19	7.04×10^3	0.46
D7	26.2 ± 0.5	52	1816	23	29.95	4.03	0.32	16.08×10^3	0.78

[a] The total times reported for each sample for each temperature is the time that the sample reached 95% of the corresponding temperature and we estimate the uncertainty to be ± 2 s.

[b] Relative uncertainty for equivalent anneal time (t_{eq}) and the diffusion lengths (l_{3D}, and l_{2D}) are estimated as $< 10\%$.

[c] l_c is the broadening of the critical concentration for metal-insulator transition relative to the as implanted dopant profile due to annealing at 1100 °C for $t = t_{eq}$ time using publicly accessible dopant profile calculator [174].

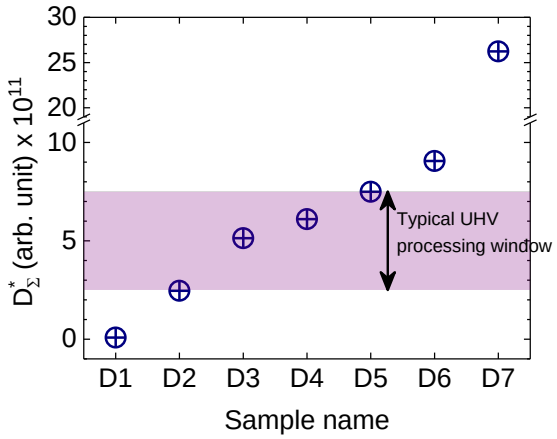

Fig. 5.3: Effective thermal activation for ther thermal processes of P dopants.

each sample at $T = 1000$ °C, $T = 1100$ °C and $T = 1200$ °C. This history can be used to estimate diffusivity $D = D_0 e^{-\frac{E_a}{k_B T}}$ [171], given a particular choice of E_a, the activation energy, and k_B, the Boltzmann constant. In all likelihood, the diffusion of P atoms can be influenced by both bulk and surface diffusion mechanisms. Furthermore, extended thermal treatments can cause sublimation of phosphorus that depletes the surface dopant density [175] and reduces the efficacy of contacts. The shallow nature of the implant opens up the possibility of many possible diffusion or depletion mechanisms. For reference, we have calculated bulk 3D diffusion lengths, surface diffusion lengths and expected dopant profile broadening (see Table 5.1) and none of these match with the experimental findings, discussed further below. Therefore, to parameterize the thermal history of each sample and allow comparison with equivalent single temperature processes, we define the integrated effective thermal activation of implanted ions as:

$$D^*_\Sigma = \frac{k}{2} \sum_i (e^{-\frac{E_a}{k_B T(t_{i+1})}} + e^{-\frac{E_a}{k_B T(t_i)}})(t_{i+1} - t_i) \tag{5.1}$$

where k is a scaling parameter that is equal to 10^{11} $1/s$ added for convenience and has no physical significance, and $T(t)$ represents the temperature profile of the UHV flash anneal process, specific to the sample being considered. For the parameterization, we use $E_a = 3.5$ eV [171] to provide an approximate thermal weighting. The D^*_Σ values calculated on several chips are shown in Fig 5.3 and Table 5.1, where the shaded range spanning $D^*_\Sigma \approx 5$ represents the range typically used for preparing chips in UHV. Thermal activation of the dopants for this set was accomplished in multiple ways: sample D1 was heated to 1000 °C in a rapid thermal annealer (RTA) for one minute; samples D2, D3 and D5 were UHV flash annealed using our standard flash anneal protocol (the variation in D^*_Σ is primarily due to different times spent at 1200 °C); samples D4 and D6 were repeatedly flash annealed two and three times, respectively; and, finally, sample D7 was flash annealed once followed by a 30 min anneal at 1100 °C.

The Table 5.1 and Fig. 5.3 are for P dopant diffusion. The As and B implanted samples are also measured in section 5.4.2 and 5.4.3. The activation energy of E_a for As in Si is 4.23 eV in the temperature range of 1100 °C - 1350 °C. [176] The thermal diffusivity exponentially depends on E_a. E_a of As dopant ($E_a = 4.23\ eV$) is higher than $E_a = 3.5\ eV$ for the P. Therefore, based on the studies of P dopant diffusion, for our typical UHV processing window in Fig. 5.3, the pre-implanted lines with As dopants will be diffused less compared to the P dopants, which means that the As pre-implanted wires can be electrically isolated even at higher D^*_Σ. The activation energy of B in Si is 3.46 eV, which is slightly lower compared to P and As. [173, 177] The diffusivity of B in Si is higher, which results in faster diffusion

in Si. Therefore, the B implanted lines may diffuse during the typical *in situ* flash annealing.

The samples presented in the following sections are prepared by *in situ* flash annealing process, which are similar to D2 or D3. In the next section, while measuring topography, and using the lock-in technique as explained in section 2.2.2, the ion implanted lines on the various kinds of substrates are detected.

5.4 STM and STS results on various implanted dopants in Si(100) substrate

In this section, the results of various substrates(i-Si, n-Si, and p-Si) and ion implanted patterns(P, As, and B) are presented with STM topography and the lock-in technique. Fig. 2.6 shows the schematic drawing of the experimental set-up with the lock-in amplifier to detect the change in the local density of states simultaneously with STM topography. By mixing AC modulation to V_{gap}, the $\frac{\partial I_T}{\partial V}\big|_{V_{gap}}$ is simultaneously measured with the STM topography. The lock-in measurement on the feedback current is performed to measure $\frac{\partial I_T}{\partial V}\big|_{V_{gap}}$ during STM topography. [86] Due to the bandwidth of the STM, the AC frequency is set at 80 kHz, which is above the STM feedback bandwidth and lower the circuit bandwidth of 100 kHz. The rms amplitude of V_{AC} is 200 mV.

Fig. 5.4 shows a schematic drawing of a real-time STM and STS set-up using a lock-in technique with a schematic drawing of a tunnel junction between a metallic STM tip and a sample. In Fig. 5.4, the tunnel junction is expressed as a capacitance

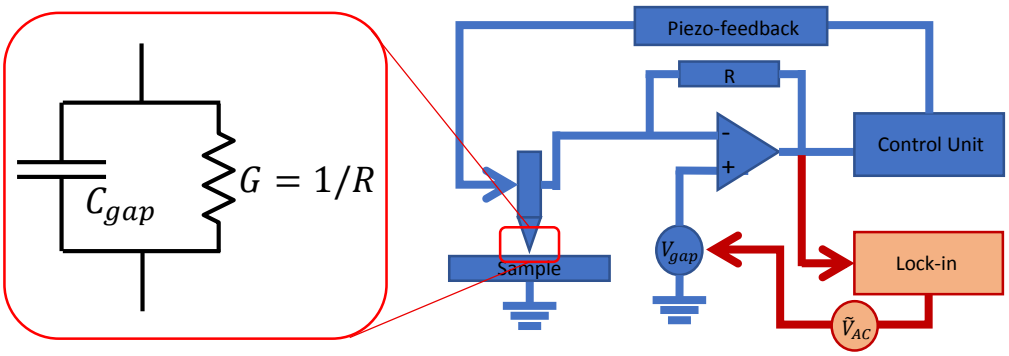

Fig. 5.4: This is a schematic drawing of a real-time STM and STS set-up. A metallic STM tip and a sample is a tunneling junction consisting of a metal, vacuum, and semiconductor. This can be expressed as a capacitance of C_{gap} and a conductance of $G = 1/R$ in parallel.

of C_{gap} and a conductance(resistance) of $G(1/R)$ in parallel. The total impedance of the tunnel junction, Z_T can be written as follow:

$$\frac{1}{Z_T} = \frac{1}{R} + i\omega C \tag{5.2}$$

$$Z_T = \frac{R(1 - i\omega RC)}{1 + (\omega RC)^2} = \frac{R}{1 + (\omega RC)^2} - \frac{i\omega R^2 C}{1 + (\omega RC)^2} \tag{5.3}$$

$$Re(Z_T) = \frac{R}{1 + (\omega RC)^2} \tag{5.4}$$

$$Im(Z_T) = -\frac{\omega R^2 C}{1 + (\omega RC)^2} \tag{5.5}$$

Due to the tip induced surface band-bending and surface states of Si(100) within a band gap, such as π, π^*, impurity states of dopants, $I(V)$ characteristics of the lightly doped n-Si and p-Si are almost identical. Also, after *in situ* flash annealing, the dopants near the surface may be depleted by thermal diffusion and sublimation into the vacuum, which can make the Fermi energy of E_F, near the

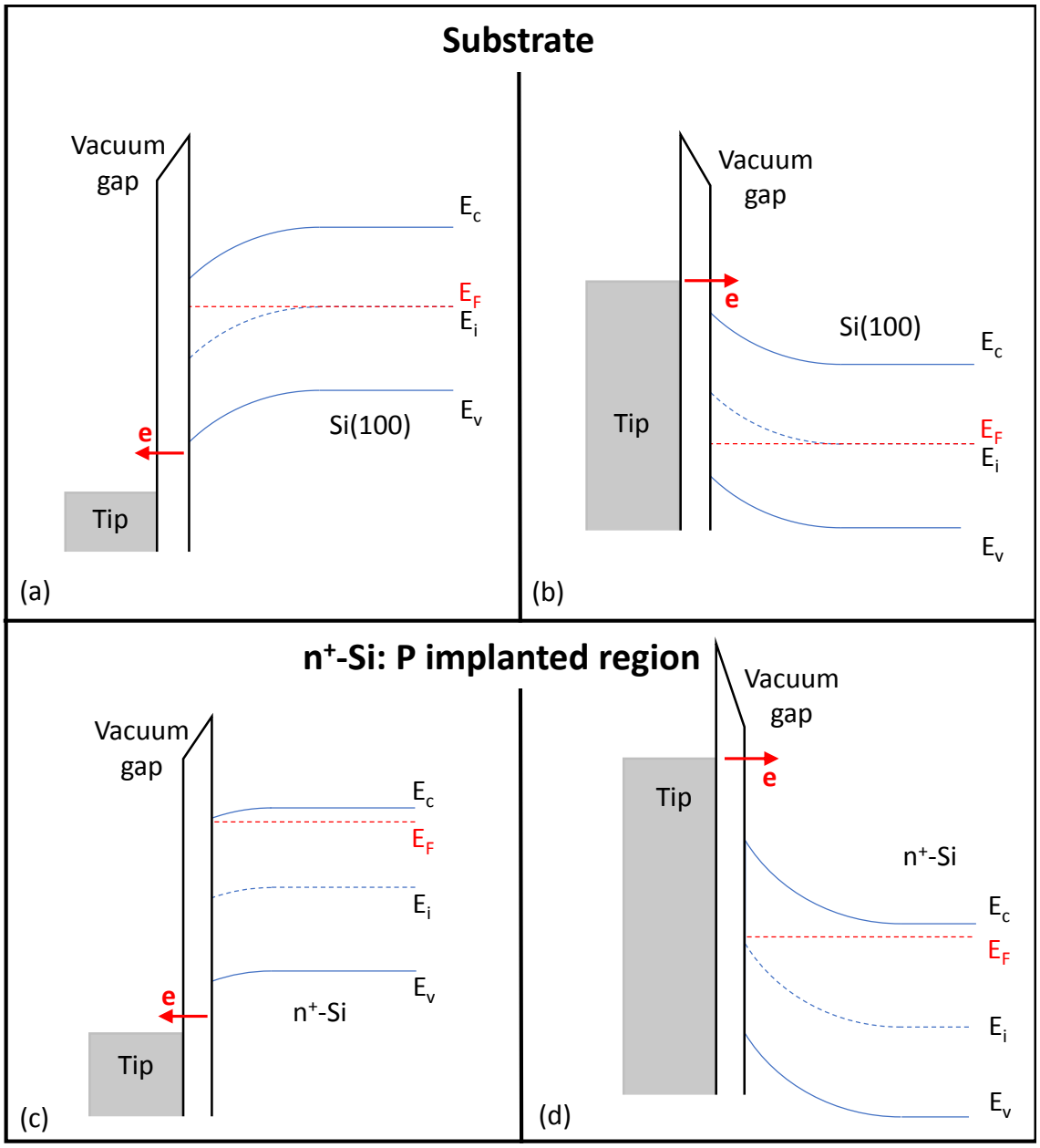

Fig. 5.5: This is a band diagram of a metal-vacuum-Si when electron is tunneling. E_C is the bottom of the conduction band. E_i is the mid-gap. E_F is the Fermi energy. E_v is the top of the valence band. For a same bias applied on a tip of V_{tip}, the amount of band bending at the surface is different for different E_F positions, which is caused by the doping density. For P implanted region of (d), E_F is very close to E_c; therefore, E_F can be pinned on E_c, which can drastically change the amount of band-bending. This causes the change in C_{gap}, which cause the change in $Im(Z_T)$ in Eq. 5.5. (a) and (b) are the band diagram of i-Si(100), which represent the substrate. (a) is for a positive V_{tip} and filled states. Electrons are tunneling from the valence band of Si to a tip. (b) is the band diagram for a negative V_{tip} and empty states. For empty states, electrons tunnel from a metal tip to the sample. (c) and (d) are the band diagram for the P implanted region where E_F is very close to E_c.

surface closer to the mid-gap of E_i. [178] Fig. 5.5(a) and (b) are the band diagram of a metal tip, vacuum, and i-Si, where E_F is positioned near at E_i. Fig. 5.5(a) is the filled states when V_{gap} is positive. For the filled states, electrons tunnel from a sample to a tip. Fig. 5.5(b) is the empty states when V_{gap} is negative. For the empty states, electrons tunnel from a tip to the sample.

Fig. 5.5(c) and (d) represent the filled states and empty states for the P implanted region, respectively. The implanted region is the degenerately P doped n^+-Si at the surface; therefore, E_F is positioned close to E_c. Fig. 5.5(c) represents the filled states. Fig. 5.5(d) represents the empty states. For a constant tunneling mode, in Fig. 5.4, the conductivity of the tunneling current is approximately constant for the substrate and the ion implanted region. For $Re(Z_T)$, this is proportional to $\frac{dI}{dV}$. As described in section 2.2.2, $\frac{dI}{dV}$ is also proportional to the local density of states of the sample. Due to the change in the E_F as a function of doping density, $E_F = E_i + kT \cdot ln(\frac{n}{n_i})$, the local density of states between the substrate and the implanted region is different, which causes the change in $\frac{\partial I_T}{\partial V}\big|_{V_{gap}}$. However, due to the surface states and impurity states within the band gap, the difference in the $I(V)$ characteristics between the substrate and the implanted region is not large. From the experiments, which are not presented here, we found that $V_{gap} = \pm$ 2.00 V gives the relatively good contrast between the substrate and the implanted wire. Due to the band-gap of Si, $V_{gap} > \pm$ 1.60 V is typically used for the Si in order to avoid the tip crash to the substrate. Also, as the $V_{gap} > \pm$ 2.20 V, because of the small tunneling gap (2nm or less), the high electric field between the tip and the sample often causes the modification of the tip apex or the sample surface.

As shown in Fig. 5.5(c), the filled states for n^+-Si, E_F is pinned to E_c; therefore, the amount of band-bending at the surface is relatively small compared to the substrate in Fig. 5.5(a). The surface band-bending, Φ_B, is defined as the difference in E_F and E_i at the surface in the metal-oxide-semiconductor (MOS) structure. [179] Also, in the STM study, the tip-induced band bending occurs, which is similar to the MOS structure. As shown in Fig. 5.5, the configuration of the metal-vacuum-Si is similar to the MOS structure. The tip-induced band bending also affects the STS spectra. [180–182] The spectral shifts due to the tip-induced band bending has been observed in Si(111), H:Si(111), Si(100), and GaAs. [183–190] However, if we consider the STM configuration as the simple MOS, the effect of Φ_B and Eq. 5.5 to the real-time STS mapping can be described.

The Φ_s depends on the position of E_F, which changes due to the doping concentration. The difference of the amount of the band bending at the surface determines the surface charge of Q induced by a bias. C_{gap} depends on the amount of surface bend bending, which is similar to the metal-oxide-semiconductor capacitance (MOSCAP). [179] For n-Si, $V_{vac} = \frac{Q}{\epsilon_0} \cdot d$, where ϵ_0 is the permittivity of the vacuum gap, d is the separation between a tip and Si. [191–193] The capacitance is defined as $C = \frac{dQ}{dV}$ [179]

For the STM as described in Fig. 5.5, the surface band-bending can be de-

scribed using the metal-oxide-semiconductor (MOS) structure as follow :

$$V_{gap} - V_{FB} = V_{vac} + \frac{\Phi_B}{q} \tag{5.6}$$

$$V_{FB} = \Phi_M - \Phi_s$$

$$= \Phi_M - (\chi + E_i - E_F) = \Phi_M - \left(\chi + E_i - kT \cdot ln\left(\frac{n}{n_i}\right)\right) \tag{5.7}$$

where V_{gap} is a bias applied on a STM tip. V_{FB} is the flat band bias, which is the workfunction difference between a STM tip and a semiconductor. V_{vac} is the potential drop in the vacuum gap. Φ_M is the workfunction of the STM tip. In a case of the STM, the workfunction of a tungsten (W) tip is 4.4 eV. Φ_s is the workfunction of a Si. χ is the electron affinity. For Si, χ is 4.2 eV. E_i is the mid-gap. E_i for the Si is 0.55 eV. The n is the doping density for n-type. For Si, n_i is 1.5 $\times$ 10^{10} cm^{-2} at 300 K. [170, 179] Therefore, the Φ_s changes as a function of the doping density. Then, V_{FB} depends on the doping density as shown in Eq. 5.7.

Therefore, according to Eq. 5.6 and 5.7, the change in the doping concentration can cause the change in Φ_s or V_{FB}. However, Φ_B depends on the doping density, E_F pinning to the surface states or impurity states, the detail structure of surface or the tip apex, and etc,. [194] It is challenging to obtain the exact values of Φ_B for the substrate and the implanted region. However, it is clear that the Φ_B between the substrate and the implanted region is different due to the doping density, which results in the change in V_{vac}. As mentioned above, C_{gap} depends on V_{vac}, which results in the difference in $Im(Z_T)$ in Eq. 5.5. In the next section, the lock-in signal of $Im(Z_T)$ of P, As, and B are presented.

The real-time STM and STS measurements are done by the constant current

mode at $V_{tip} = \pm$ 2.00 V and $I_{set} = 100$ pA. The estimated C_{gap} is ≈ 100 aF, which is mostly the local contribution of a tip apex. [82,195,196] The STM depends on the local electric charge, which can be altered by a local structure or defects. The detailed local electric charge at the surface can also affect the amount of the surface band bending, C_{gap}, and the tunneling matrix element. It is challenging to get the exact value of the C_{gap} and the tunneling impedance. Our results show great contrast between the substrate and the pre-implanted wires, which are due to the large difference in doping concentration or positions of E_F.

For all the experiments in the following sections, the center devices in Fig. 5.1 with four ion implanted wires are measured. As explained in the previous section, the samples are cleaned by *ex situ* and *in situ* cleaning process in section 2.3. As shown in Fig. 5.1(b) and (c), after cleaning, the samples are clean with low density of surface defects. The P and As implanted patterns can be detected using the lock-in technique as presented in the section 5.4.1 and 5.4.2. However, in the section 5.4.3, the B implanted patterns are not detected due to the dopant diffusion in the substrate and out-diffusion to vacuum during high temperature flash cleaning.

In the following sections, the figures consist of 3 images. The first panel is the topography taken at $V_{tip} = 2.00$ V and $I_{set} = 100$ pA. The second panel is the imaginary-part of the lock-in signal, taken at $V_{tip} = 2.00$ V and $I_{set} = 100$ pA, which is $Im(Z_T)$ in Eq. 5.5. The third panel is the imaginary part of the lock-in signal taken at $V_{tip} = -2.00$ V and $I_{set} = 100$ pA. The topography of the empty states at $V_{tip} = -2.00$ V and $I_{set} = 100$ pA is same as the filled states; therefore, the empty states topography is not included. The STM topography and STS map

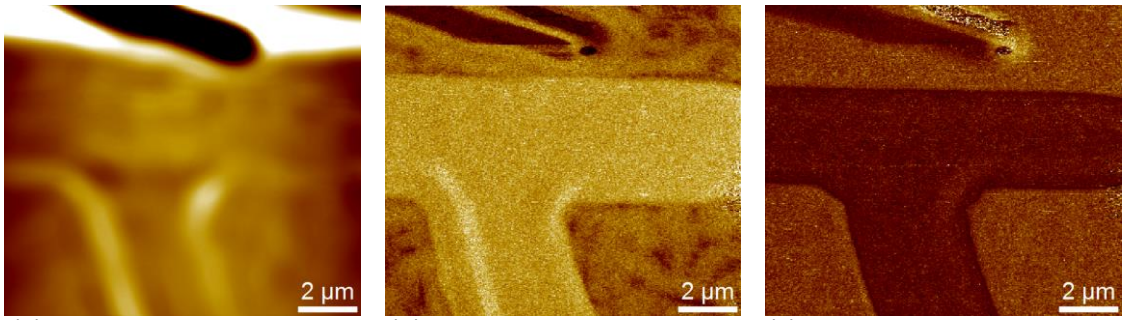

Fig. 5.6: The substrate of this sample is P doped n-Si(100). The wires are P ion implanted. (a) This is topography image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. The damage from the ion implantation and the different SiO_2 thickness between implanted region and bare substrate causes the topographic changes in the ion implanted region. (b) The imaginary part of the lock-in signal at V_{tip} = 2.00 V and I_{set} = 100 pA. (c) The imaginary part of the lock-in signal at V_{tip} = -2.00 V and I_{set} = 100 pA. The darker area is the P implanted region.

at $V_{tip} = \pm$ 2.00 V are taken simultaneously by dual bias mode. STM scans a single line twice by scanning $\pm$ +x-direction, then move up in y-direction. For a dual bias mode, when STM scans a line in the x-direction, V_{tip} is set to be 2.00 V. Then, when STM scans a same line in the -x-direction, V_{tip} is set to be -2.00 V. All the STM and STS maps that are presented in the following sections are measured simultaneously.

5.4.1 P implantation on substrates of n-Si(P) and p-Si(B)

In this section, P implanted wires on n-Si and p-Si substrates are measured. The n-Si substrate is (7-20) $\Omega \cdot cm$ lightly doped with P. The p-Si is (10-20) $\Omega \cdot cm$ lightly doped with B. Both samples are prepared by *ex situ* and *in situ* cleaning procedure described in section 2.3.

Fig. 5.6 is the sample with n-Si(100) substrate. The topography and real-time STS using lock-in technique are measured on the region shown in Fig. 5.1(a). Fig. 5.6(a) is topography taken at V_{tip} = 2.00 V and I_{set} = 100 pA. Fig. 5.6(b) is the

imaginary part of the lock-in signal taken at V_{tip} = 2.00 V and I_{set} = 100 pA, which is $Im(Z_T)$ in Eq. 5.5. Fig. 5.6(c) is the imaginary part of the lock-in signal taken at V_{tip} = -2.00 V and I_{set} = 100 pA.

The topographic image in Fig. 5.6(a) has an area of 12 μm by 12 μm. The dark feature at the top of the image is the etched fiducial mark, which is $\approx$ 100 nm deep. The pattern of the implanted region is similar to "T". As explained at section 5.2, due to the crystal damage from the ion implantation, the thickness of the chemically grown oxide from *ex situ* cleaning procedure between the substrate and implanted region is different. The step edges of Si(100) after the surface reconstruction by *in situ* flash annealing has complex landscape. Therefore, the edge of the implanted region in the topography is still visible. However, a clean (2×1)Si(100) surface is shown in Fig. 5.1(b) and (c).

Fig. 5.6(b) is the imaginary part of the lock-in signal at V_{tip} = 2.00 V and I_{set} = 100 pA. The bright area with a shape of "T" where P ions are implanted are clearly visible. As discussed in the previous section, the contrast between the substrate and the pre-implanted wire is due to the local density of states at V_{gap} and C_{gap}. Fig. 5.6(c) is the imaginary part of the lock-in signal at V_{tip} = - 2.00 V and I_{set} = 100 pA. The darker area with the shape of T is also visible. The contrast is due to the 90 degree phase shift during the initial set-up of the lock-in signal as explained at section 2.2.2. At $\approx$ 2 μm from the sample surface, the lock-in amplifier is set to maximize the imaginary part by the 90 phase shift after the auto-phase.

The next sample is the P implanted wires in the lightly B doped p-Si(100). Fig. 5.7(a) is the filled states topography at V_{tip} = 2.00 V and I_{set} = 100 pA. The

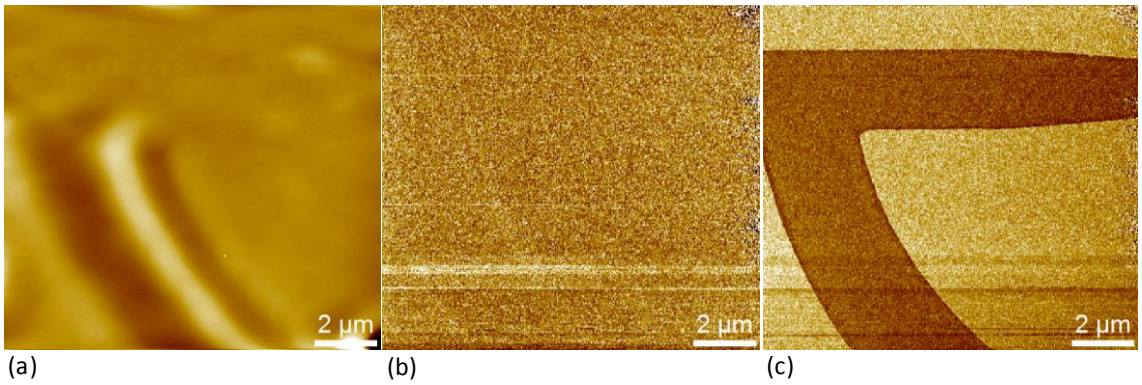

Fig. 5.7: The substrate of this sample is B doped p-Si(100). The P wires are ion implanted. (a) This is a topography image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. (b) The imaginary part of the lock-in signal at V_{tip} = 2.00 V and I_{set} = 100 pA. (c) The imaginary part of the lock-in signal at V_{tip} = -2.00 V and I_{set} = 100 pA.

topography of the p-Si(100) with P implantation is similar to Fig. 5.6(a) due to the complex surface reconstruction. As discussed in section 5.3, the activation energy of B for diffusion is lower and the vapor pressure of B is relatively higher than other dopants so that *in situ* flash annealing causes B dopants to diffuse into the substrate or out-diffuse into the vacuum. Like P, the position of E_F of the lightly B doped p-Si after flash annealing may be close to E_i as in Fig. 5.5(a) and (b).

Fig. 5.7(b) is the imaginary part of the lock-in signal taken at V_{tip} = 2.00 V and I_{set} = 100 pA, which are the filled states. The implanted region is not very clear in Fig. 5.7(b). As shown in Fig. 5.5, the relative difference of the band bending between the substrate and the implanted region for the filled states is smaller than the empty states. This can lead to less contrast of the imaginary part in the filled states images. Ref. [194] shows that in consideration of the tip-induced band bending the donors in subsurface is more distinguishable in the empty states. The tip-induced band bending changes drastically in the empty states as a function of doping concentration. [194] Fig. 5.7(c) is the imaginary part for the

empty states at V_{tip} = -2.00 V and I_{set} = 100 pA. It shows a very clear contrast between the substrate and the implanted region. In contrast to the filled states, the band bending for the empty states is much larger, which can induce the larger surface charge density. This may lead to better contrast between the substrate and the implanted region.

The bulk diffusion of dopants is affected by extrinsic factors, such as the background doping of the substrate. The flash annealing procedure for n-Si substrate and p-Si substrate was nominally the same; however, the dopant diffusion is exponentially depends on the temperature. Therefore, the small deviation of the temperature could change E_F at the surface. The real-time STS mapping strongly depends on the tunneling matrix element, which also depends on the density of states of the tip. Therefore, it is challenging to figure out the exact solution of the measurements of the real-time STS mapping. However, Fig. 5.6 and Fig. 5.7 show a clear contrast between the substrate and the implanted region, which can be used for STM lithography to fabricate nano-devices. The nano-wire fabricated by the P pre-implanted wires and STM lithography is discussed in later section 5.6.

In the next section, the detection of As implanted wires on i-Si and p-Si substrates is presented using the real-time STS mapping with STM topography.

5.4.2 As implantation on substrates of i-Si and p-Si(B)

In this section, As dopants are ion implanted with a same implantation parameters as P and the same patterns as in Fig. 5.2. The center device with four wires in Fig. 5.2 is measured. The substrates are i-Si(100) (FZ > 10 kΩ·cm) and

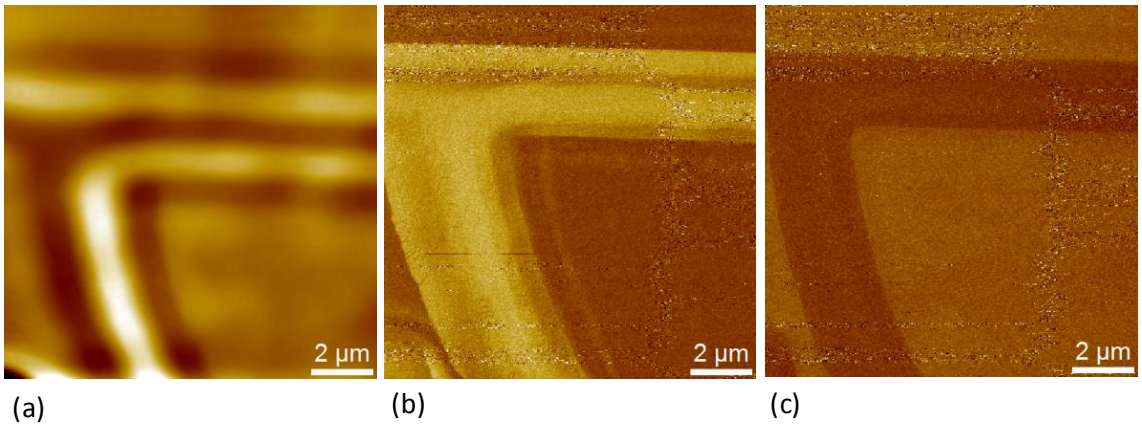

Fig. 5.8: The substrate of this sample is i-Si(100). The As are ion implanted. (a) This is topography image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. (b) The imaginary part of the lock-in signal at V_{set} = 2.00 V and I_{set} = 100 pA. The darker area is the As implanted region. (c) The imaginary part of the lock-in signal at V_{set} = -2.00 V and I_{set} = 100 pA.

p-Si(100) (B-doped). The lock-in amplifier is set up at the same frequency of 80 kHz and the rms amplitude of 200 mV same as the P implanted samples.

Fig. 5.8(a) is the filled states topography at V_{tip} = 2.00 V and I_{set} = 100 pA, which is similar to the P implanted samples. The left bottom corner shows the tip of the etched fiducial mark. Fig. 5.8(b) is the imaginary part of the lock-in signal for the filled states at V_{tip} = 2.00 V and I_{set} = 100 pA. It shows a clear contrast between the substrate and the implanted region. Fig. 5.8(c) is for the empty states at V_{tip} = -2.00 V and I_{set} = 100 pA. It also shows good contrast between the substrate and the implanted region. However, the width of the pattern is different. The amount of the band bending is not linear as a function of the bias or the doping concentration. [181, 194] For a same reason as P implanted sample, the tip-induced band bending in the empty states changes more drastically as a function of the doping concentration. [194] Therefore, Fig. 5.8(c) of the STS map in the empty

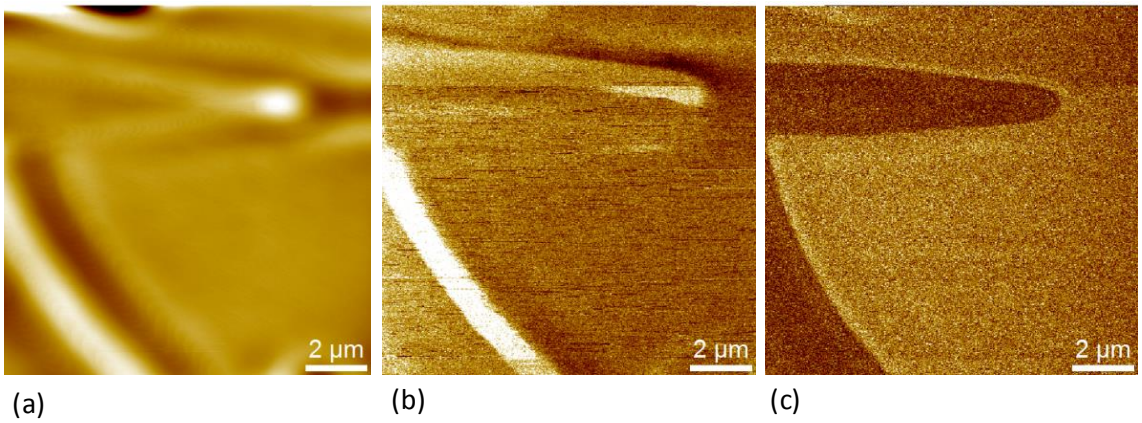

Fig. 5.9: The substrate of this sample is B doped p-Si(100). The As wires are ion implanted. (a) This is topography image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. (b) The imaginary part of the lock-in signal at V_{tip} = 2.00 V and I_{set} = 100 pA. The dark area at the top of the image is the etched fiducial mark. (c) The imaginary part of the lock-in signal at V_{tip} = -2.00 V and I_{set} = 100 pA.

states shows a better contrast.

The As dopants are also implanted in a p-Si(100) substrate(10-20 Ω·cm) with the same ion implantation parameters as other samples. Fig. 5.9 is the As implanted sample in p-Si(100). The position of E_F is expected to be near E_i as in Fig. 5.5(a) and (b). Fig. 5.9(a) is the filled states topography at V_{tip} = 2.00 V and I_{set} = 100 pA. Fig. 5.9(b) is the imaginary part of the lock-in signal in the filled states at V_{tip} = 2.00 V and I_{set} = 100 pA. Fig. 5.9(c) is the empty states images at V_{tip} = -2.00 V and I_{set} = 100 pA. The bright curve in Fig. 5.9(b) is the edge of the implanted wire. Ref. [194] shows a smooth and small change of ≈ 0.5 eV over the dopant concentration range of (10^{12} - 10^{22}) cm^{-3} in the tip-induced band bending for the filled states. However, since STS depends on the tunneling matrix element, which depends on the potential drop in vacuum gap, if the STM tip feedback is not fast enough, the deviation of the tunneling current could result in a change in the

lock-in signal. Also, the As dopants could be segregated to the interface between the implanted region and the substrate where the dopant diffusion can be affected by the damage from the ion implantation. Fig. 5.9(c) shows a clear contrast. As discussed in the previous section 5.4.1, the tip-induced band bending for donors changes drastically in the empty states.

The P implanted and As implanted samples are processed by the same *in situ* flash annealing process, e.g. 1050 °C (1min), 1150 °C (15 sec), and 1200 °C (3 times 10 secs). The larger activation energy of the diffusion coefficient makes As dopants diffuse less for the same thermal budget. The width of the horizontal implanted wire for As is slightly smaller than P. The larger activation energy also allows us to bring the As implanted wires closer at the active device patterning region and reduce the time for STM lithography process. This can then reduce the chemical contamination, such as C, O, and N, from the background vacuum.

Fig. 5.8 and Fig. 5.9 show a clear contrast between the substrate and the implanted wires. The advantage of the As implanted wires is the larger activation energy for diffusion in Si, which increases the thermal budget for fabrication process.

5.4.3 B implantation on substrates of n-Si(P) and p-Si(B)

In this section, the B ion implanted samples in n-Si(100) and p-Si(100) are measured. The B ions are implanted with a same parameters as P and As. As discussed in section 5.3, the activation energy of B is much smaller than P and As. The diffusion length of B during *in situ* flash annealing is expected to be longer. Also, the out-diffusion of B in Si at flash annealing can be induced due to the

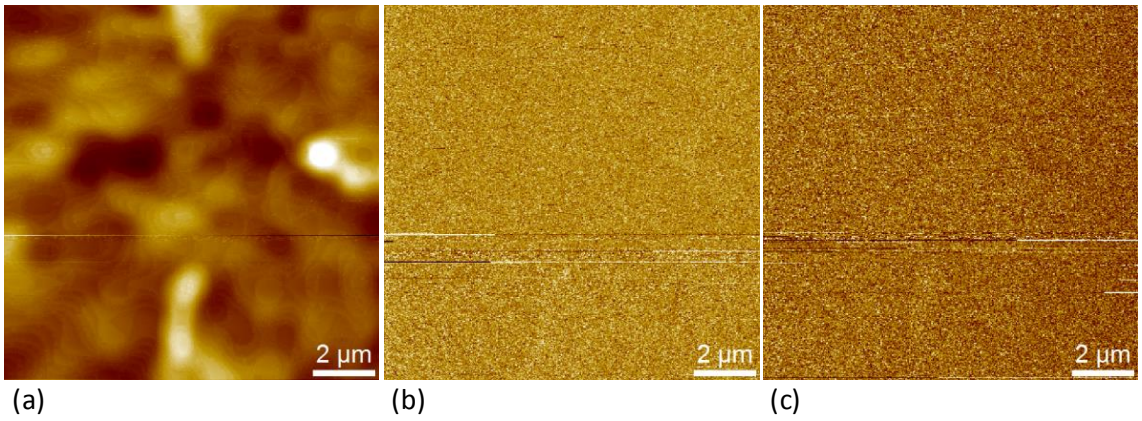

Fig. 5.10: The substrate of this sample is P doped n-Si(100). The B wires are ion implanted. (a) This is topographic image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. (b) The imaginary part of the lock-in signal at V_{set} = 2.00 V and I_{set} = 100 pA. (c) The imaginary part of the lock-in signal at V_{set} = -2.00 V and I_{set} = 100 pA.

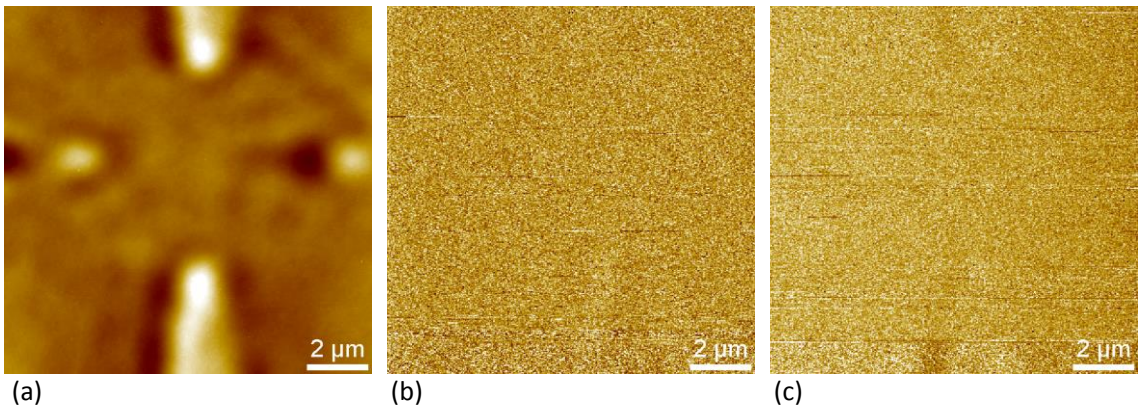

Fig. 5.11: The substrate of this sample is B doped p-Si(100). The B are ion implanted. (a) This is topography image taken at V_{tip} = 2.00 V and I_{set} = 100 pA. (b) The imaginary part of the lock-in signal at V_{tip} = 2.00 V and I_{set} = 100 pA. The darker area is the As implanted region. (c) The imaginary part of the lock-in signal at V_{tip} = -2.00 V and I_{set} = 100 pA.

high vapor pressure. So, the B implanted samples in Fig. 5.10 and Fig. 5.11 are flash annealed at 1200 °C for 20 seconds, which is 10 seconds shorter than typical flash annealing. This results in a higher density of vacancy defects on the surface measured by STM.

Fig. 5.10(a) and Fig. 5.11(a) are topography in the filled states at V_{tip} = 2.00 V

and I_{set} = 100 pA. The patterns of the four implanted wires can be identified by topography such as four tips coming from the top of the image, from the right side of the image, from the bottom of the image, and from the left side of the image. As discussed in section 5.1 and 5.4.1, due to the crystal damage from the ion implantation, the chemically grown SiO_2 layer from *ex situ* cleaning process is thicker than the substrate. During the *in situ* annealing, the reconstruction of the surface becomes complicated, which results in the complex waxy terraces. Therefore, the ion implanted region are visible. However, Fig. 5.10(b), (c), Fig. 5.11(b), and (c) do not show contrast between the substrate and the implanted region. As expected, the *in situ* flash annealing cause the diffusion of the B dopants due to the dopant diffusion to the substrate and out-diffusion into the vacuum. The doping concentration may be nearly the same within the scanned area of 12 μm $\times$ 12 μm. The B implanted wires are not feasible with *in situ* high temperature flash annealing. If the low temperature SiO_2 removal can obtain a clean (2×1) Si(100) surface, the B implanted wires may be used at a small thermal budget.

5.5 Kelvin probe force microscope

Kelvin probe force microscope (KPFM) measures the local surface potential or work function difference between a conducting AFM tip and a sample. [197–199] When a conducting tip approaches close to the sample, the Fermi levels of the sample and the tip are aligned at an equilibrium state. The workfunction difference between the sample and the tip induces an electric force, which causes the electric potential

between a tip and a sample to reach an equilibrium state. By applying a DC bias between a sample and a tip, the contact potential difference can be canceled. Then, the amount of applied bias to cancel the electric potential is the difference in the workfunction of the tip and the sample. Therefore, with a known workfunction of a tip, the workfunction of a sample can be measured. KPFM uses an AFM, which allows to map the local surface potential.

The workfunction of Si(100) is the electron affinity of 4.05 eV plus the relative Fermi energy position from the conduction band edge. [200, 201] Therefore, the change of the Fermi energy due to the change in doping concentration between the pre-implanted wires and the substrate results the change in workfunctions. Therefore, using KPFM, the pre-implanted lines can be detected by mapping the workfunctions of the sample. Eq. 5.7 for the real-time STS mapping using the lock-in technique also measures the change of the workfunction at the constant V_{gap} applied on the STM tip. KPFM and the real-time STS mapping in the previous sections measures the same thing, which is the change in the workfunction between the substrate and the implanted region. As mentioned in the introduction of this chapter, our real-time STS mapping using the lock-in technique can scan the topography and the STS map simultaneously at different bias conditions. Also, since our technique is *in situ*, it is compatible with STM lithography to fabricate the nanodevices in Si(100), which is presented in section 5.6. [34]

In order to measure the local surface potential using KPFM, the separation between the tip and the sample has to be constant during KPFM scanning. First, the AFM measures the topography. Then, using the topography, the KPFM scans

the surface at a fixed separation between the sample and the tip. By measuring the bias to cancel the local surface potential, which is induced by the difference in the workfunction of the sample and the tip, the KPFM map the workfunction variation of the sample. In our case, the 2D profile of the doping concentration at the surface changes as it scans across the substrate and the implanted region, which changes E_F position within the band gap.

In the following section, the topography and the workfunction of P and B implanted samples are measured using AFM and KPFM, which verifies the real-time lock-in technique with STS. All the samples, presented in the following sections, are cleaned by *ex situ* and *in situ* cleaning procedure and measured by the real-time STM and STS.

5.5.1 P implanted samples

Using KPFM, the P implanted in n-Si(100) sample is measured after high temperature flash annealing. This sample is flashed as described in section 2.3.2. The n-Si(100) substrate is (7 - 20) Ω·cm lightly doped with P. The 4 wire configuration device, which is the center device in Fig. 5.2, is measured.

Fig. 5.12 is the AFM and KPFM scans of the P implanted sample. The inset of Fig. 5.12(a) is the micrograph of the sample and the AFM tip. The red light is the reflected laser from a AFM tip. The eight dark lines are the etched fiducial patterns. As shown in the inset of Fig. 5.12(a), the AFM tip is aligned between two etched lines, where one of the 4 implanted wire is located. In Fig. 5.2, the photo-mask for ion implantation is designed to be 3 μm wide at the AFM tip position. Fig. 5.12(a)

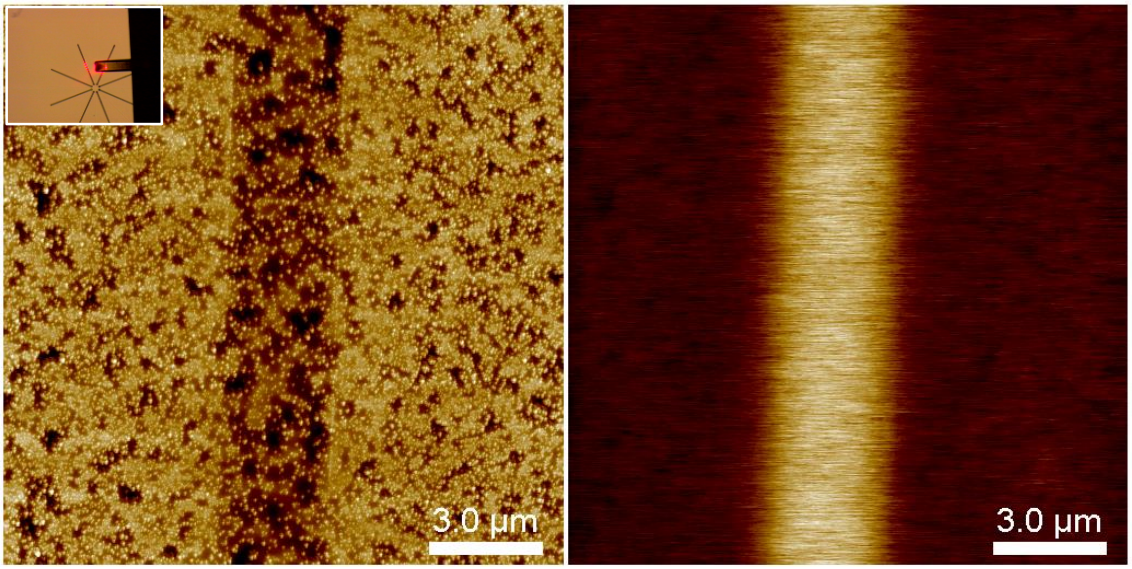

Fig. 5.12: The P implanted n-Si(100) sample is flashed in the UHV chamber before AFM and KPFM measurements. It is measured on one of ion implanted line between etched fiducial lines. The red lights with a large rectangle is the AFM tip position. (a) This is the topography measured by AFM. The Z range of this image is $\approx$ 40 nm. (b) KPFM measures the work function of the surface. The differences in the Fermi level position due to the different doping concentration change the work function of the surface between the substrate and P implanted region. The 3 μ wide bright vertical line in (b) is the preimplanted line.

is topography (15 μm by 15 μm) measured by AFM. The dark vertical feature with a width of 3 μm is the P implanted region. The height scale of Fig. 5.12(a) is $\approx$ 40 nm. As shown in the STM images in the previous sections, due to the crystal damage and different thickness of SiO_2 layer on the pre-implanted region after *ex situ* cleaning, the surface reconstruction is complicated, which is observed in the STM images in the section 5.4.

The AFM topographic image in Fig. 5.12(a) looks different from the STM topographic image in Fig. 5.6(a), which are diced from the same wafer. The AFM topography show lots of bright spots, which are most likely contaminants on the surface. Fig. 5.12(a) can not be directly compared to Fig. 5.6(a). The sample

preparation process for two samples are different. The sample measured in Fig. 5.6 is introduced to the vacuum chamber right after *ex situ* cleaning at the cleanroom. However, the sample in Fig. 5.12 is measured by the AFM before the sample is introduced to the vacuum chamber. This causes some contaminants from the AFM tip or abosrbates on the surface, which might not be removed by the *in situ* flash annealing. Compared to the AFM topography in Fig. 5.12(a), the B implanted samples in Fig. 5.13(a) and (c) do not show the bright spots or contamination on the surface. The B implanted samples are introduced to the chamber right after *ex situ* cleaning at the cleanroom before *in situ* flash annealing. Then, the B implanted samples are measured by the AFM and the KPFM. This is another evidence of the contaminants in Fig. 5.12(a) due to the longer exposure of the sample to the atmosphere before introducing to the chamber.

Fig. 5.12(b) is the image of the workfunction or the surface potential of the sample. The bright vertical line with a width of ≈ 3 μm is the ion implanted wire, which is also visible in Fig. 5.12(a). As explained in the previous section, the change in the workfunction of the ion implanted wire is due to the change in E_F for different doping concentration. The KPFM data shows that the ion implanted wires cause the change in the workfunction due to the change in the doping concentration between the substrate and the ion implanted wire as shown in the real-time STS detection in section 5.4.1.

In the next section, the AFM topography and KPFM of the B implanted samples, which are the same samples presented in Fig. 5.10 and 5.11 are presented.

5.5.2 B implanted samples

The B implanted samples in section 5.4.3 are also measured by the KPFM. The real-time STS data does not show the contrast between the substrate and the ion implanted wires after *in situ* high temperature flash annealing. During high temperature flash annealing, the B diffuses laterally in the substrate and out-diffuses to the vacuum. Therefore, the doping density on the scanned area (12 μm $\times$ 12 μm) in Fig. 5.10 and 5.11 is nearly the same. In order to verify our STS data, the two samples are measured by KPFM.

Fig. 5.13(a) and (b) are for the B implanted wires on the n-Si substrate. Fig. 5.13(c) and (d) are the B implanted wires on the p-Si substrate. Fig. 5.13(a) is the topography measured by the AFM. Three dark features are the etched fiducial patterns for the STM coarse alignment. The implanted wires are still faintly visible in Fig. 5.13(a). The AFM topography of the B implanted wires on the p-Si in Fig. 5.11(c) looks the same as Fig. 5.13(a). The KPFM does not show contrast between the substrate and the B implanted region in the center region where the nanodevices can be fabricated with the STM lithography for both samples. This sample shows no variation in the workfunction of the sample with the B implanted wires after *in situ* flash annealing.

Due to the low activation energy of the diffusion and the high vapor pressure of B, the B dopants diffuse in the substrate and/or out-diffuse into the vacuum during *in situ* high temperature flash annealing. If the low temperature SiO_2 removal methods in section 2.3.2 are available, then the B diffusion in Si can be minimized

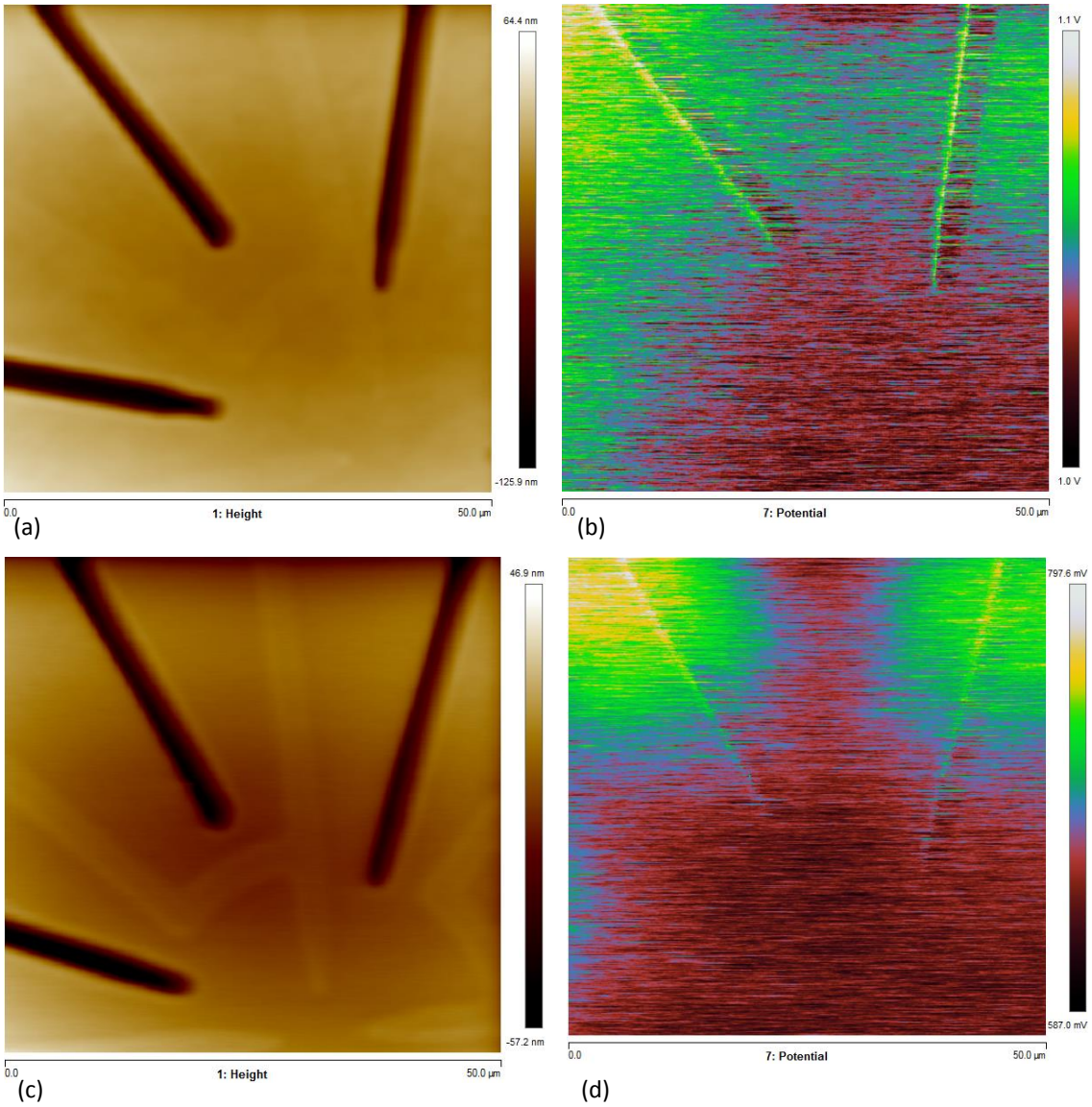

Fig. 5.13: (a)This is a topography of B implanted sample with n-Si(P) substrate measured by AFM. (b) This is Kelvin probe force microscope of (a). (c) This is a topography of B implanted sample with p-Si(B) substrate measured by AFM. (d) This is KPFM measurement of (c). As measured by STM and STS in Fig. 5.10 and 5.11, KPFM did not measure the change in the surface workfunction between the implanted region and the substrate. The high temperature *in situ* cleaning process diffuse the B dopants in the substrate and out-diffuse to the vacuum due to the low activation energy and high vapor pressure of B.

because of the exponential temperature dependence of the thermal diffusion. The B implanted wires can be used to fabricate p-type nanodevices and p-n junction in low dimension by the STM lithography.

5.6 STM patterned nanowires with P dopants

In this section, the electrical connection from a STM patterned nanoscale device to the pre-implanted wires is achieved by P ion implanted photolithograpically defined areas to create degenerately doped regions in Si substrate. The fabrication process of nano-wires using STM lithography and low temperature Si overgrowth is presented in the following section. A four wire implant patterns in Fig. 5.2 is used to demonstrate identification and electrical contacting to a STM patterned 2D nanodevice. The optical image of the completed device, the electrical characteristics of the P implanted wires and the P nanodevice with the P implanted wires are presented in this section.

5.6.1 Nano-wire by STM lithography fabrication process

Fig. 5.14 is a schematic drawing of fabrication process of an STM patterned device with ion implanted wires and PH_3 dosing. First, as explained in section 5.2, the P ion are implanted. Then, the fiducial patterns for coarse alignment with a STM tip is etched. After *ex situ* cleaning procedure, the chip is introduced to the vacuum chamber. Then, the sample is prepared by *in situ* cleaning procedure as described in section 2.3. Fig. 5.14(a) is after the sample preparation in a vacuum chamber.

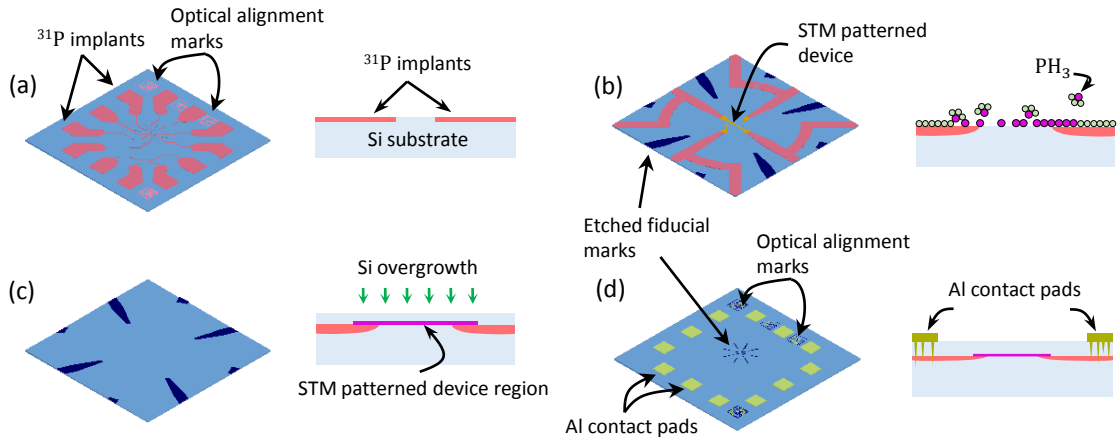

Fig. 5.14: This is a schematic drawing of fabrication process of STM patterned devices with ion implanted wires. Each panel has the top view(left) and the side view(right) of the fabrication step. (a) The pink area is heavily ^{31}P implanted regions with low energy ion implantation which are photolithographically defined. The fiducial marks for STM tip alignment is etched. The first ion implantation and etching fiducial marks are done in a wafer scale. Then, the wafer is diced into 4 μm by 10 μm chips. Each chip is cleaned by *ex situ* and *in situ* cleaning procedure fo H passivation. (b) After *in situ* cleaning and H passivation, using high magnification optical system and etched fiducial marks, the devices are patterned using STM lithography. The patterned region is dosed with phosphine(PH_3) and heated to incorporate the dopants. (c) A capping layer of Si is deosited to encapsulate the device. (d) Al metal contacts are deposited and patterned by photolithography. This is reformatted from Ref. [34]

The area colored with pink is heavily P doped region by photolithography and ion implantation. Then, the sample is passivated with an atomic layer of hydrogen, which is used similar to photoresist in commercial CMOS fabrication technology. Next, using an optical telescope, the STM tip is aligned to the center of the etched marks as shown in the inset of Fig. 5.1(a). Using the telescope in combination with the etched fiducial patterns, the first tip approach is within ≈ 5 μm of the implant/etch center point. At a pre-anneal depth of 100 nm, these features are deep enough to be seen by the optical telescope, yet shallow enough to scan across with the STM when using a large tunneling gap. Since each of the etch features points toward the center, the proximity of the initial approach combined with clever choices of scan size and rates allow one to center the frame on the pattern within about 30 minutes. The implanted lines themselves also have some residual topography that persists after the thermal processing that can be used to aid alignment as shown in Fig. 5.1(b). Consequently, considering all the features point to the center, identification of correction vectors is straightforward.

In Fig. 5.14(b), using STM, the hydrogen atoms can be deterministically removed to pattern nanodevices as explained in section 2.2.3. Fig. 5.14(b) shows a STM patterned device (light orange) where the hydrogen atoms are removed by STM lithography. Onto the ends of the implant lines, the large overlay regions of ≈ 1 μm^2 are patterned. Then, the narrow (≈ 300 nm) wires are patterned to connect the implant lines $b_2 \leftrightarrow d_2, c_2 \leftrightarrow d_2$, and $b_2 \leftrightarrow a_2$. Then, the sample is exposed to the phosphine gas(PH_3) and thermally activated to transfer the hydrogen pattern to heavily doped P regions in the silicon. The PH_3 can be bonded to Si(100) dangling

bonds of STM patterned region while the rest of the region is protected by the hydrogen passivated layer. The drawing on the right side of Fig. 5.14(b) is after PH_3 dosing. [32, 33, 113] Several depassivation and dosing cycles are used in the course of the full pattern.

The fine area is shown again in Fig. 5.14(c), where the patterned device and implant lines are overgrown with silicon while still in UHV, encapsulating the device and the implant lines. After overgrowing the Si capping layer, the sample is taken out of the vacuum chamber. Ohmic metal contacts are fabricated by sputter deposition of Al, followed by photolithography to define an etch mask where the photo-mask is optically aligned to the etched alignment marks on the substrate. Finally, the full die is shown again in Fig. 5.14(d), where photolithography is used to pattern macroscopic aluminum contact pads over the large implant regions ($\approx 200\ \mu m^2$) and the alignment of the metal photo mask to the sample is realized by using the etched optical alignment marks. Finally a low-temperature thermal spiking at 350 °C for 30 min in N_2 atmosphere establishes electrical contact through the silicon capping layer. [202, 203] The optical image of the completed device is in Fig. 5.15(a).

In the following section, the results of the electrical measurements are presented in Fig. 5.15(b).

5.6.2 Electrical measurements of STM patterned P nano-wire

In this section, using the device in Fig. 5.15(a), the STM patterned devices are characterized for electrical transport measurements at < 4 K. As shown in the annotated optical micrographs in Fig. 5.15(a), we have designed an implant pattern based on eight radial wires (navy) in which every other wire is cross-linked to its adjacent wire (e.g., b_1 connected to b_2), improving the measurements by eliminating parasitic resistances in the connecting circuits (leads, wire bonds, etc). Four of the implant lines continue toward the center for direct connection to the STM written pattern, terminating when the tips are on a 8 μm diameter circle to leave a clean space in which the device is patterned. Between each of the implant lines is a shallow radial etch feature (light blue) so that the implant lines and the etch features share a common center point and the radial etch features are terminated when the tips are on a 26 μm diameter circle to leave the clear space for the STM navigation.

The sample is mounted on a closed-cycle cryocooler measurement system that cooled the sample to < 4 K. Leakage resistance for the measurement system is < 10 GΩ. For the transport measurements of the STM written nanowire, a programmable constant-current source was stepped through an array of current values while a differential instrumentation amplifier was used to remove common mode voltage and amplify the signal measured by a voltmeter.

At 4 K, all of the aluminum to P doped contacts had low (< 30 kΩ) resistances as determined by pairwise measurements, e.g., $a_1 \leftrightarrow a_2$, etc. Example $I(V)$

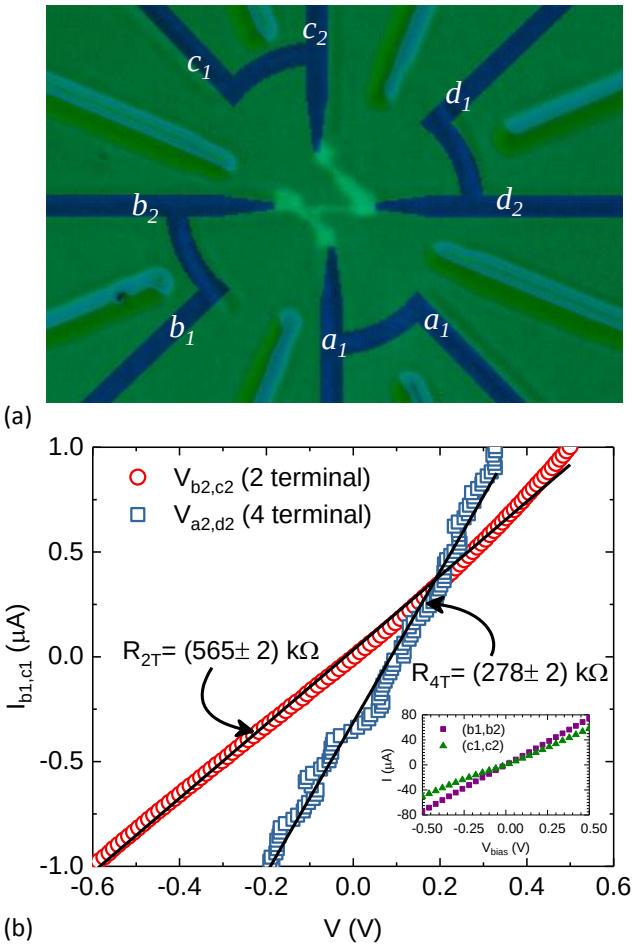

Fig. 5.15: (a) This is a differential interference contrast (Nomarski) microscopy image of the finished sample with STM patterned device with overlay (implanted regions marked with blue). (b) This is a plot of 2 terminals(R_{2T}, red circles) and 4 terminals (R_{4T}, blue squares) voltages measured across b_2, c_2 and a_2, d_2. The inset in (b) shows $I(V)$ characteristics of the P ion implanted wires of (b_1, b_2) and (c_1, c_2).

measurements of these implant line pair are shown in the inset of Fig. 5.15(b). For the electrical connections between the nanowire and the implants, the resistances for two (b_2 and c_2) of the four contacts were good and two (a_2 and d_2) of them were poor (insufficient for current, but sufficient for voltage probes). Using the good contacts to source and drain current through the STM written nanowire, first, "two terminal"(2 pt) measurement is performed by sending current from $b_1 \leftrightarrow c_1$ and

measuring the voltage drop from $b_2 \leftrightarrow c_2$, shown in Fig. 5.15(b) in red. Note that while this is a "two-terminal" measurement of the wire since it includes the nanowire to implant contact resistance, the independent voltage probes (b_2 and c_2) still eliminate the parasitic resistance from all the external connections and implant wire, etc. These measurements were performed in a current biased configuration from $\pm$ 1 μA, spanning a voltage range of more than a volt while remaining essentially linear.

Next, "four terminal"(4 pt) configuration is performed by using a_2 and d_2 as voltage probes to measure a subsection of the wire between b_2 and d_2, thus eliminating the voltage drop across the nanowire contacts. The four-terminal $I(V)$ measurement is shown in Fig. 5.15 in blue, and is also linear over the entire range of the measurement, with a resistance diminished roughly in proportion to the number of squares in the wire segment under measurement. The deviation from zero volts at zero current in the four terminal measurement is believed to be due to an offset in the differential amplifier used for the measurement. Looking more carefully at the results and using the STM image of the completed pattern, the wire under measurement in the 4 pt case is estimated to have (14.7 $\pm$ 2) squares, corresponding to $R_\square$ = (18.9 $\pm$ 2) kΩ for the wire. The uncertainties of the measurements and the calculated quantities are smaller than the symbols in Fig. 5.15(b); therefore, the uncertainties are not shown in the plot. While our $R_\square$ is somewhat high compared to other work in the field, it is similar to other STM patterned devices measured using standard e-beam lithography based contacting method in our group, consistent with our assessment of good implant to dopant contact. [33] Applying this $R_\square$ back to the 2 pt result, where (29.6 $\pm$ 3) squares are estimated, the expected full

wire resistance (without contacts) would be (560 ± 90) kΩ. The difference from the 2 pt measurement of ≈ 565 kΩ and the previous estimate can then be attributed to the nanowire to implant contact resistance, estimated to be (3 ± 45) kΩ each. While this value has a large uncertainty, it is a qualitatively small number that is certainly acceptable. The uncertainties reported for resistances are the standard deviations derived by propagating uncertainties and are dominated by the uncertainty in estimating number of squares contributing to each configuration. Comparing the 560 kΩ wire measurement, the $>$ 10G Ω implant isolation measurements and the geometrical considerations of source and drain, we concluded that a good electrical contact is made and an STM patterned device with a somewhat high $R_{\square}$ is measured.

The contact resistance between the STM written nanodevice and the preimplant wires was based on the measurements performed at 4 K; therefore, further assessments of the contact resistance (with lower uncertainty) and yield of these contacts at temperatures below 4 K will be the subject of future studies.

5.7 Summary

In this chapter, the detection of pre-implanted wires of P and As on the various substrates was demonstrated. The topography and the real-time STS mapping for the filled states and empty states are simultaneously measured using a lock-in technique. The real-time STS mapping of the P and As implanted wires are clearly visible. For both P and As implanted wires, the measurements in the empty states

show better contrast, which is due to the larger difference in the tip-induced band bending for donors as studied in Ref. [194]. This may cause a larger change in C_{gap} between the substrate and the implanted region. The As implanted wires show much less diffusion, which allows to bring the wire closer at the active device region. This can reduce time for the STM lithography process, which is important factor to keep the device clean by minimizing the contamination from the background gases. However, B dopants are diffused or out-diffused during *in situ* flash annealing so that the patterns of the implanted wires are no longer feasible for contacts. The low temperature SiO_2 removal may enable us to minimize the B dopant diffusion and achieve a clean (2×1) Si(100) surface for STM lithography with the hydrogen resist layer.

KPFM confirms the results of real-time STS mapping for the P implanted wires and B implanted wires. The change in the surface potential due to the doping concentration profile for the P implanted sample confirms the results of the real-time STS mapping. Also, due to the diffusion of B dopants, the B implanted wires are also not visible in KPFM.

Using the P implanted wires and STM lithography using PH_3 dosing, nanowires made of P dopants in Si are fabricated and characterized. Those pre-implanted wires for STM lithography can eliminate the use of highly specialized tools, e.g., electron beam lithography, which enables a big technological advantage for many research groups for realizing electrical connections to nanoscale devices. The benefits of photolithographically defined ion implantation at the wafer scale dramatically reduces the overhead for fabrication and measurement of STM defined nanode-

vices compared to chip-by-chip electron beam lithography. Additionally, this approach connects the STM patterned region with the external electrical connections in plane, increasing the number of available conduction channels between the two. This method also enables the ability to realize electrical connections to the STM patterned nanodevices *in situ*, and is a unique advantage of this method over contemporary contacting methods. The design rules and specifications demonstrated here provide room for a wide range of creative implementations, enabling a simpler path to challenging nanodevice, fabrication and measurements.

Chapter 6

Al doped device fabrication in Si(100) using STM lithography

The acceptor based quantum dots in Si are of interest due to large spin-orbit coupling and no valley degeneracy. However, the acceptor based quantum dots using STM lithography has not been demonstrated yet. The acceptor based quantum information devices fabricated using STM lithography can be combined with superconducting Al-Si superlattice in a single crystal material. The Al precursor for CVD and ALD has been shown to have high concentration of C, N, and O contamination. [114] I used the elemental Al to eliminate contamination during dosing process. I studied 4 possible methods to fabricate devices in Si(100) using STM lithography with the hydrogen mask such as sticking coefficients, the effective enthalpy of sublimation, surface diffusivity by deposition rates and surface temperatures. This set of methods can be used for any type of doping source to verify if the doping source can be used for STM lithography. The device design and fabrication process are explained in section 5.2.

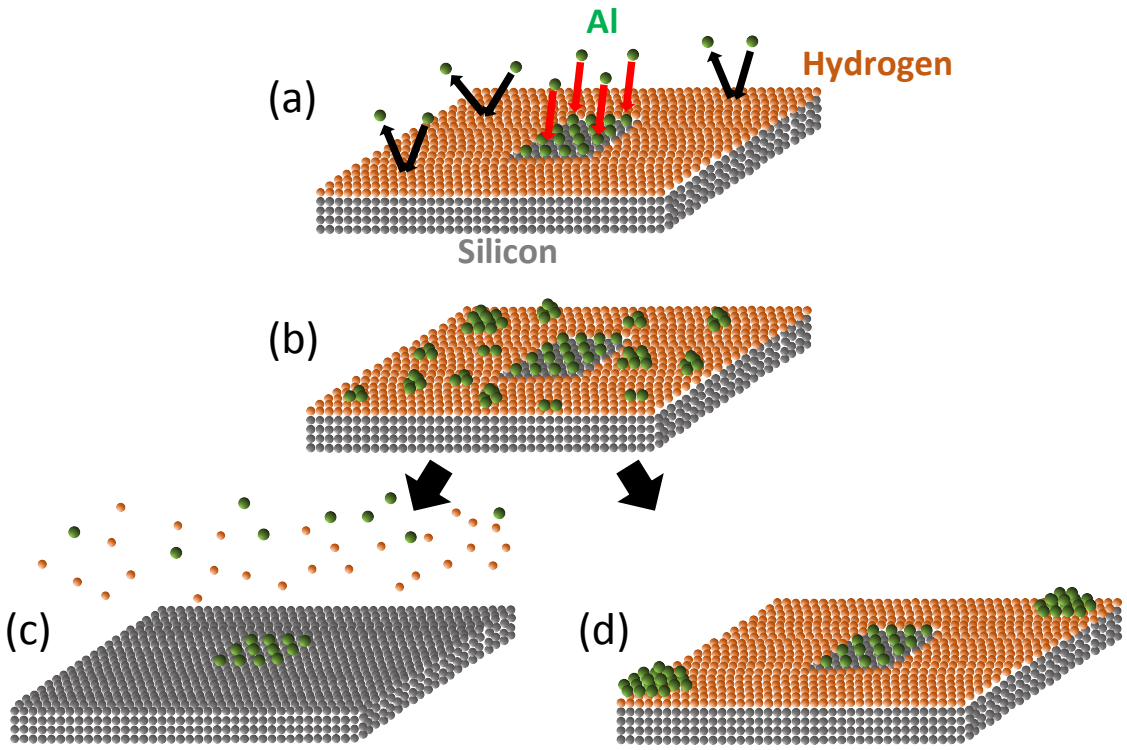

Fig. 6.1: The three possible physical mechanism for STM lithography with H:Si(100) is described in a cartoon.

6.1 Strategy: three possible mechanism for STM lithography with H:Si(100)

In this section, I will explain strategies of three physical mechanisms to evaluate the dopant source for STM lithography with H:Si(100): sticking coefficients, effective enthalpy of sublimation, and surface diffusivity. Fig. 6.1 describes each mechanism.

6.1.1 Sticking: the protection of the hydrogen resist layer from Al adatoms

Fig. 6.1(a) describes sticking coefficients which means that the dopant does not stick on the H:Si(100) but does stick on the bare Si(100). PH_3 and DMAH have been demonstrated in this way on H:Si(100). [33, 112, 204] In order to evaluate the relative sticking coefficients between H:Si(100) and bare Si(100), sqaure patterns are lithographically drawn on H:Si(100) using STM. Then, the elemental Al is deposited. Using fiducial systems and high magnification optical system described in section 5.2, the Al structures and relative density of H:Si(100) and bare Si(100) are compared using STM.

6.1.2 Lift-off: effective enthalpy of sublimation

Another possibility is a case where dopant stick both on H:Si(100) and on the bare Si(100) surface as depicted in Fig. 6.1(b). If the dopants on the passivated surface are weakly adsorbed while the dopants on the bare surface react before desorbing, and sufficiently high vapor pressure for the dopants on the hydrogen can be reached before the hydrogen releases, then a "lift-off" like process can occur where dopants outside the pattern desorb and leave dopants inside the patterns as depicted in Fig. 6.1(c). The hydrogen resist layer on Si(100) can be thermally desorbed by heating the surface above 450 °C while many dopants will react with the bare silicon below this temperature. For this test, we compare elemental Al deposited on H:Si(100) and bare S(100) after heating the substrate up to 470 °C for

30 seconds to remove the hydrogen resist layer.

6.1.3 Density modulation

The last possible mechanism is the least favorable since the average density of dopants inside and outside of the pattern is the same at completion—depicted in Fig. 6.1(d). This can result in the ability to pattern circuits if the dopants outside the pattern nucleate large, isolated clusters are too disconnected for electrical percolation, while those inside uniformly dope the silicon. This case requires a substantial difference in the distribution of the dopants inside vs. outside the pattern. This case is theoretically possible since the number density of island nuclei can be estimated based on this equation,

$$N \propto \left(\frac{R}{D}\right)^{p},\ p = \frac{1}{3}, \frac{2}{3} \tag{6.1}$$

where the power depends on the microscopic mechanism limiting diffusion (e.g., step vs terrace, isotopic vs anisotopic limited), N is number density of nuclei, R is deposition rate, D and is the surface diffusion coefficient. [205, 206] The power, p, depends on various diffusion mechanisms such as dimensionality of diffusion, isotropic or anisotropic diffusion, and flat surface or step edge limited diffusion. If dopants have a much higher diffusivity outside the pattern and nearly stationary sticking inside the pattern then continuous doping can be achived inside the pattern but disconnect clusters outside. To test this, we compare the island density inside and outside of a pattern for the same dose of aluminum and test for changes in the island density with dopant fluence.

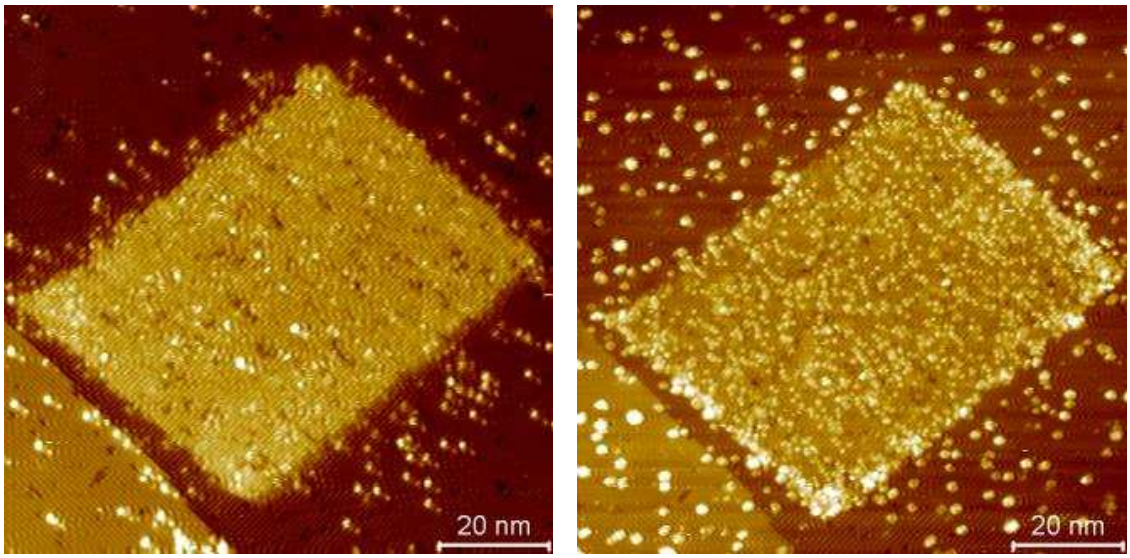

Fig. 6.2: (a) is taken at V_{tip} = 1.80 V, I_{set} = 130 pA after hydrogen depassivation using STM. The bright rectangle at the center is the depassivated area. The bright spot outside of the pattern is dangling bons. Then, the sample is moved to the deposition chamber for Al deposition. $\approx 1.7 \times 10^{13}$ atoms/cm^2 of the elemental Al is deposited at the room temperature. (b) is taken at V_{tip} = -1.90 V, I_{set} = 100 pA. Inside the rectangle pattern, Al chains are formed. Outside of the pattern where the hydrogen resist layer exist, Al adatoms are absorbed and form Al clusters.

6.2 Experimental results

In this section, I will discuss the experimental results of three physical mechanisms described in the previous section and Fig. 6.1.

6.2.1 The protection of the hyrogen resist layer from Al adatoms

The first mechanism is to study if the Al adatoms are sticked on the hydrogen resist layer or not. As explained in section. 6.1.1, after depassivating hydrogen layer in a red rectangle in Fig. 5.1 using STM, the elemental Al is deposited on

the substrate. Fig. 6.2(a) is a STM image at V_{tip} = 1.80 V, I_{set} = 130 pA after depassivating hydrogen in bright rectangle using STM. The physcial height of the bright area is lower than outside due to the absence of the hydrogen atoms on the surface. The outside of the rectangle is still hydrogen passivated. However, because of the higher density of states of the dangling bonds, the depassivated area appears to be higher.

After H depassivation, the sample is transfered to the magnetic transfer rod as depicted in Fig. 2.22. $\approx 1.7 \times 10^{13}$ atoms/cm^2 of the elemental Al is deposited at the room temperature at a deposition rate of $\approx 5.7 \times 10^{13}$ atoms/(cm^2·min). Then, the sample is moved back to STM and, by using fiducial patterns and high magnefication optics, the rectangle is found as explained in section 5.2. Fig. 6.2(b) is taken at V_{tip} = -1.90 V, I_{set} = 100 pA after Al deposition. Inside the rectangle, Al chains are formed oriented perpendicular to the underlying (2×1) reconstructed Si(100) dimer rows. Group III and IV metals, such as Al, Ga, In, Sb, and Pb, are known to form one-dimensional self-assembled chains on Si(100). [52, 207–209] The surface diffusion constant of Al adatoms on Si(100) is very high due to the low activation energy, which allows Al chains to be formed perpendicular to the underlying (2×1) Si(100) dimer rows even at the room temperature. [209] On the outside of the patterned regimes in Fig. 6.2(b) where the hydrogen resist layer still exists, Al clusters are formed, in an agreement with a previous experiment. [210] The elemental Al adatoms are absorbed on the hydrogen resist layer and diffuse to other Al adatoms, dangiling bond, or surface defects to form Al clusters. This is somewhat expected due to the physical vapor deposition process. Compared to

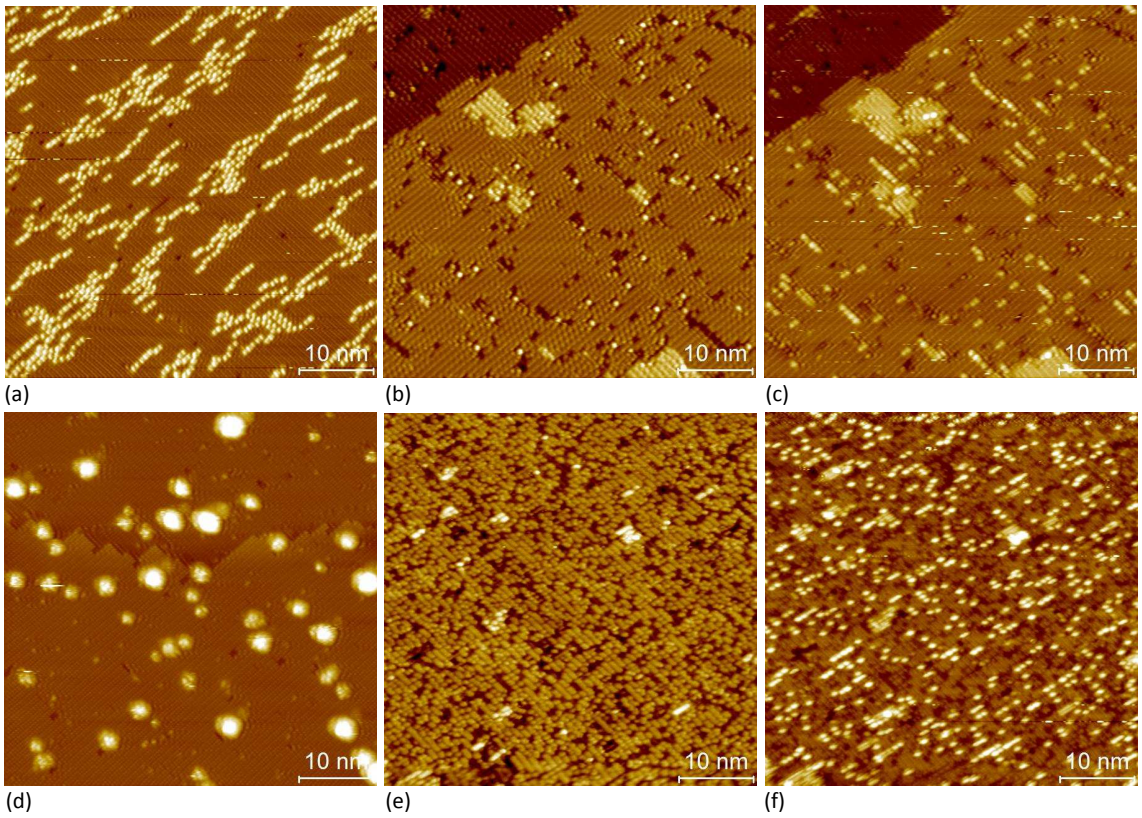

Fig. 6.3: (a) after $\approx 2.5 \times 10^{13}$ atoms/cm^2 of the elemental Al deposition on bare Si(100) and (d) hydrogen passivated Si(100). (a) and (d) are taken at V_{tip} = 2.00 V, I_{set} = 150 pA. (a) shows Al chains same as Fig. 2.24. (d) Al clusters are formed on the hydrogen resist layer same as Fig. 6.2. (a) and (d) are annealed to 470 °C for 30 seconds. Then, the samples are moved back to STM. (b) and (c) are taken simultaneously at V_{tip} = 2.00 V, I_{set} = 150 pA and V_{tip} = -2.00 V, I_{set} = 150 pA, respectively. The most of the dark lines in (b) are incorporate Al. The ejected Si atoms due to incorporated Al form new islands. The bright spots in (b) are Al-Si nano-clusters. The other bright lines that do not appear on (b) are remaining Al chains on the surface. (e) and (f) are simultaneously taken at V_{tip} = 2.00 V, I_{set} = 150 pA, and V_{tip} = -2.00 V, I_{set} = 150 pA, repectively. Compared to (c) ore Al adatoms are still on the surface an fewer new Si islands are formed, but the result is qualitatively the same for both of the bare and hydrogen passivated surfaces.

the anisotropic diffusion of Al adatoms on a bare Si(100), the Al adatoms on the hydrogen resist layer shows isotropic and higher mobility to form Al clusters.

6.2.2 Effective enthalpy of sublimation

Since the elemental Al stick on both outside and inside of the patterned regime, the next possibility we consider is to selectively remove the undesired Al clusters on the outside of the patterns. This is to utilize the H layer like a resist mask in CMOS applications to "lift-off" the undesired Al clusters while the dopants within the pattern remain. The hydrogen passivated layer on Si(100) can be thermally desorbed from the surface above 450 °C. [211]

To test "lift-off" concept, I prepared two samples of a bare Si(100) and H:Si(100). Then, the same amount of Al, $\approx 2.5 \times 10^{13}$ atoms/cm^2, is deposited at the room temperature in Fig. 6.4(a) and (d), respectively. Fig. 6.3(a) shows Al chains formed on the bare Si(100) as shown in Fig. 2.24. In order to "lift-off the hydrogen resist layer, both samples are annealed to 470 °C for 30 seconds, cooled and then returned to the STM. Fig. 6.4(b) and (c) are taken simultaneously at V_{tip} = 2.00 V, I_{set} = 150 pA, and V_{tip} = -2.00 V, I_{set} = 150 pA, respectively. In Fig. 6.3(b), the dark lines are substitutional replacements of silicon atoms in the substrate, consistent with observations in previous studies. [212] The dark lines due to incorporated Al atoms in Fig. 6.3(b) shows Al atoms inside the dark lines in Fig. 6.3(c). Fig 6.3(c) shows remaining Al chains on the surface which do not appear in Fig. 6.3(b). Group III atoms on Si(100) appear to have the similar height as unerlying Si(100) substrate on the fille state images(negative V_{tip}) while the Al chains in empty state images appear to have on atomic height. [52,207–209] In Fig 6.3(b) and (c), the bright spots are (3×4)Si-Al clusters. The bow-tie shape in Fig. 6.3(b) (filled state images) and

the two circles in Fig. 6.3(c) (empty state images) are identified on experiments an first-principle calculations published by others. [212, 213].

Fig. 6.3(e) and (f) are taken after 470 °C annealing at $V_{tip} = 2.00$ V, $I_{set} = 150$ pA and V_{tip} = -2.00 V, $I_{set} = 150$ pA, respectively. Qualitatively, Fig. 6.3(e) and (f) look the same as Fig. 6.3(b) and (c) showing that Al clusters are not removed during the heating and desorption of the hyrogen resist layer, i.e., they did not lift-off. During heating, the Al clusters might start to dissociate while the hydrogen resist layer is depassivated. In stead of lift-off, the dissociate Al atoms could diffuse on the surface to form Al chains or incorporate into the substrate. The shorter Al chains and less Si islands are formed on the surface compared to the bare Si(100) as in Fig. 6.3(b) and (c). Since the vapor pressure of Al at 470 °C is only $\approx 1.01 \times 10^{-11}$ Pa (7.60×10^{-14} Torr) an the chamber pressure is $\approx 6.7 \times 10^{-9}$ Pa (5.0×10^{-11} Torr), the Al clusters on H:Si(100) will require > 1000 seconds to decay while the hydrogen will be removed in only a few seconds. [214] Therefore, the Al clusters decaying by sublimation on the H:Si(100) is not feasible, and essentially the same low vapor pressure is why the first method was unsuccessful. Some other candidate dopants with vapor pressure higher than H:Si(100) equivalent vapor pressure might be remove by the thermal lift-off process, or even "reflected" during initial dosing.

In Fig. 6.4, I calculate the evaporation rate of various dopants as a function of temperature base on a Hertz-Knusen equation for various opants, such as Al, As, Bi, Ga, In, and Sb, and thermal desorption rate of hydrogen from H:Si(100). [214–220] The grey area indicates the lower and upper limits of hydrogen desorption rate due to the range of desorption activation energy from several studies. [217, 219–223] The

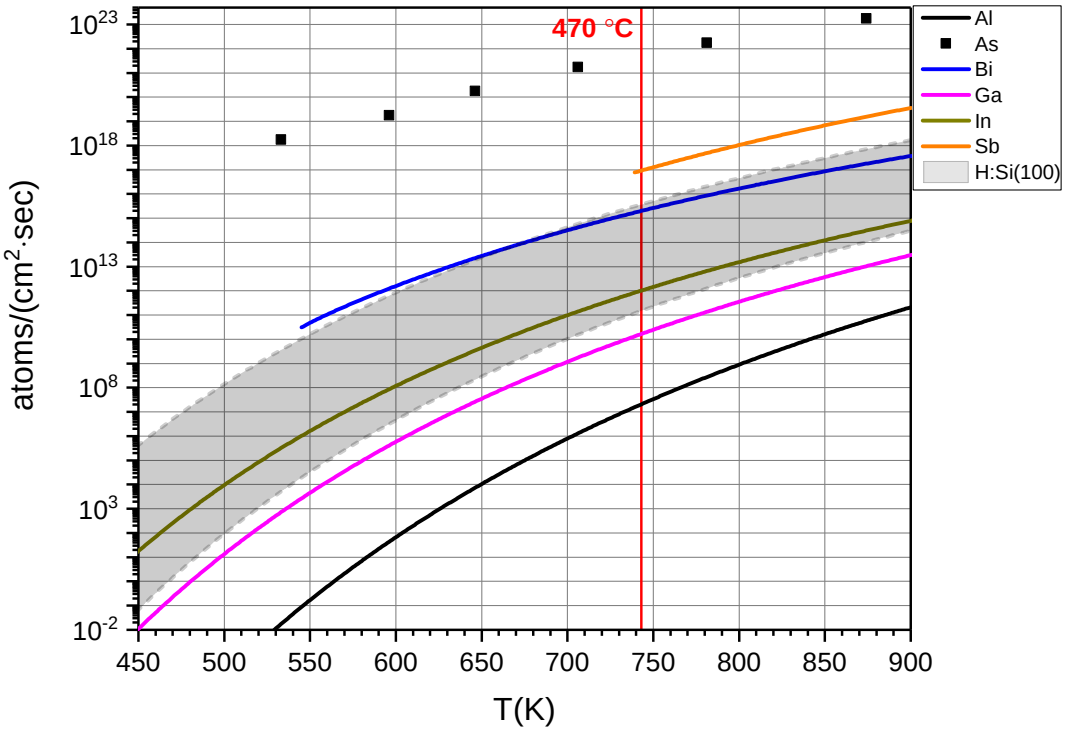

Fig. 6.4: This is a plot of calculated evaporation rate of various dopants and thermal desorption rate of the hydrogen resist layer as function of temperature. The gray area indicates the lower and upper limits of the hydrogen desorption rate of H:Si(100). The red vertical line at 470 °C is the temperature used in Fig. 6.3. Since In, Ga, Bi, and Al have lower vapor pressure than hydrogen resist layer. As and Sb can be good candidates for STM lithography with the hydrogen resist layer based on the higher evaporation rate than hydrogen.

red vertical line at 470 °C in Fig. 6.4 shows that the evaporation rate of Al is 4 to 7 orders of magnitude smaller than the hydrogen desorption rate. The calculated evaporation rate of As, In, and Bi may evaporate from or not even be absorbed on the hydrogen resist layer. However, unlike Al on the hydrogen resist layer, Bi adatoms on H:Si(100) chemically react with the underlying Si(100) substrate and from Bi nanolines. [224, 225] Therefore, As and Sb can be good candidates for STM lithography with hyrogen resist layer if those dopants o not react with the hydrogen

resist layer.

6.2.3 Surface diffusivity: deposition rates

The last method is to manipulate the density and the size of the particles inside and outside the pattern based on the relationship of surface diffusion and the deposition rate in section 6.1.3. Inside the patterned regions, Al acts as substitutial dopants, whereas outside the pattern, Al forms nanocrystals. If the Al nanocrystals remain intact with a long distance between each other after Si overgrowth, they would be electrically isolated from the STM patterned devices regions and other Al nanocrystals.

The number density of nulcei deceasses as the deposition rate decreases with a power law based on Eq. 6.1. The substrate temperature of all the experiments was set at the room temperature since the surface diffusion constant depends on the surface temperature. As discussed in section 6.2.1, Al adatoms on the hydrogen resist layer diffuse isotropically with high mobility.

I prepared two samples with hydrogen resist layer. The deposition rate is reduced from $\approx 5.7 \times 10^{13}$ atoms/(cm^2·min) to $\approx 1.1 \times 10^{12}$ atoms/(cm^2·min). Fig. 6.5(a) is taken after Al deposition at the deposition rate of $\approx 5.7 \times 10^{13}$ atoms/(cm^2·min) at $V_{tip} = 2.00$ V, $I_{set} = 60$ pA. The number density of Al clusters are averaged over the many different areas. The Al cluster density in Fig. 6.5(a) is $2.54 \pm 0.18 \times 10^{12}$ cm^{-2}. Then, in Fig. 6.5(b), the same amount of Al is deposited at the deposition rate of $\approx 1.1 \times 10^{12}$ atoms/(cm^2·min). Fig. 6.5(b) is taken at $V_{tip} = 2.10$ V and $I_{set} = 50$ pA. The average density of Al clusters in Fig. 6.5(b) is

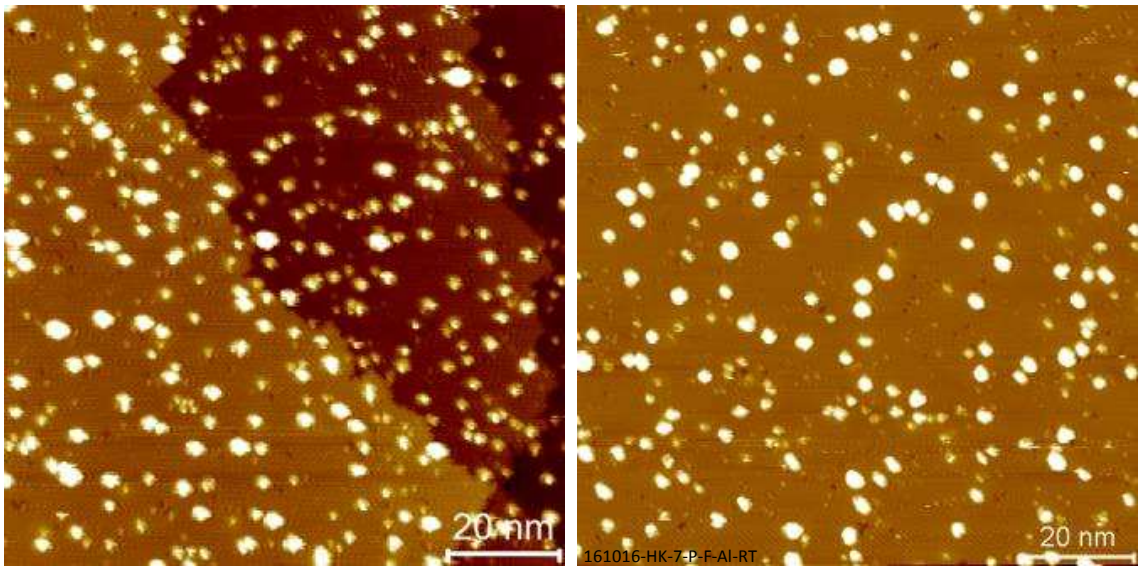

Fig. 6.5: (a) This is taken after $\approx 2.5 \times 10^{13}$ atoms/cm^2 of Al is deposited at the deposition rate of $\approx 5.7 \times 10^{13}$ atoms/cm^2·min

$2.27 \pm 0.10 \times 10^{12}$ cm^{-2}.

The substantial reduction of the deposition rate by 50 times does not decrease the density of Al clusters on the hydrogen resist layer. This indicates that the other factors are limiting the surface diffusion of Al adatoms on the hydrogen resist layer. The first factor is the remaining dangling bonds of Si(100) after hydrogen passivation. The daningling bonds can easily make Si-Al bonding with Al adatoms which other Al adatoms bonds to Al atoms to form Al clusters. However, the density of dangling bonds on H:Si(100) is one order of magnitude smaller than Al cluster density. Then, the surface defect density of H:Si(100) before Al deposition oo Fig. 6.5(a), such as dangling bonds, and vacancy defects, is $2.33 \times 10^{12} \pm 0.07$ cm^{-2}. The surface defect density of the hydrogen resist layer is similar to Al cluster density, which indicates that any type of surface defects act as bonding sites for Al adatoms

Surface defect density(10^{12} cm^{-2})	Al cluster density(10^{12} cm^{-2}) at $\approx 5.7\times10^{13}$ atoms/(cm^2·min)	Al cluster density(10^{12} cm^{-2}) at $\approx 1.1\times10^{12}$ atoms/(cm^2·min)
2.33 ± 0.07	2.54 ± 0.18	2.27 ± 0.10

Tab. 6.1: This is a summary of the number densities of surface defects of the hydrogen resist layer and Al cluster densities for two different deposition rates such as $\approx 5.7 \times 10^{13}$ atoms/(cm^2·min) and $\approx 1.1 \times 10^{12}$ atoms/(cm^2·min). The substrate temperatures are kept at the room temperatures in all experiments.

on the hydrogen resist layer. Unless the hydrogen resist layer is perfectly clean, this mechanism does not seem to be effective.

6.3 Summary and conclusions

In this chapter, I designed three methods, such as direct hydrogen resist layer protection, lift-off, and surface diffusion which can be used to evaluate any candidate dopant for STM lithography. The elemental Al does not seem be compatible with STM lithography with hydrogen resist layer based on this study. The elemental Al using PVD is absorbed to the hydrogen resist layer due to the low vapor pressure to form clusters which can cause unintentional electrical path through the outside of the devices. The lift-off process by thermally desorbing the hydrogen resist layer is not successful due to the low vapor pressure of Al. The substantial decrease of Al deposition rate by 50 times does not reduce the number density of Al clusters limited by the surface defects. With a perfectly clean H:Si(100) surface, the number density of Al clusters may be reduced further. The three strategic experiments to

evaluate a new doping source for STM lithography with hydrogen resist layer can be used for other doping sources. Based on the calculation of evaporation rate of various dopants for Si in Fig. 6.4, As and Sb can be good candidates for STM lithography with hydrogen resist layer.

Chapter 7

Electronic properties of the incorporated Al in Si(100) by scanning tunneling spectroscopy

7.1 Introduction

We have found in chapter 4 that the dominant charge carrier in the Al delta-dope Si(100) Si/Al/Si heterostructures is hole. Our Al delta-doped Si(100) shows the high charge carrier density of $\approx 1.39 \times 10^{14}$ cm^{-2} with a Hall mobility of ≈ 20 cm$^2/V \cdot s$, similar B delta-doped Si. As discussed in chapter 1, acceptor qubits in Si have strong spin-orbit interaction, which enables new ways to entangle spin qubits by coupling to electric fields and the deformation potential. [35, 226] Therefore, radio-frequency (RF) magnetic fields and the nano-magnets can be avoided, which are also known sources of decoherence. The Al in group III, is a p-type dopant in Si with impurity level at 67 meV above the valence band, which can be used to fabricate acceptor qubits in Si. [227] Also, Al dopants in Si are predicted to be superconducting at higher T_c compared to the highly B doped Si $T_c = 0.35$ K. [58, 66]

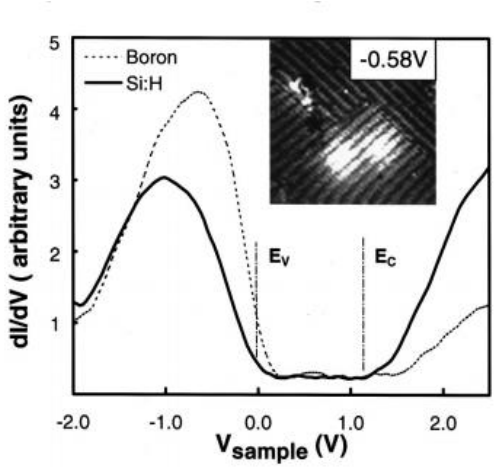

Fig. 7.1: This is H:Si(100) with degenerately B doped substrate. The bright features in the inset are two B dopants in Si. The solid line is taken on the H:Si(100) dimer. The dashed line is taken on one of bright features. The E_F changes between H:Si(100) and single B dopant. [231]

Therefore, Al is a good candidate for acceptor qubits, which can be fabricated as a new proposed interface free superconducting semiconductor qubit. [48]

Al is not a popular dopant in VLSI and ULSI due to technical difficulties, such as a low solid solubility, a high surface-segregation rate, and tendency to form clusters. [228–230] The electronic properties of Al dopant in Si has not been well studied. Therefore, we have studied the structures and electrical properties of incorporated Al atoms in Si(100) using STS and STM at room temperature in UHV. STS can provide the local density of states to understand the electrical properties of incorporated Al atoms in Si(100) similar to the Al delta-doped Si in chapter 4.

First, STS has been used to study the defects and the dopants (Si, Te, Mn and Zn) in GaAs. [232–237] Since the recent development of atomically precise dopant devices in Si using STM lithography, the need to understand dopants in Si has been growing. Other dopants in Si, such as P, As, and B, have been studied using

STS. [231, 238–241] These studies are motivated to detect individual dopants in Si, which appear as a protrusion or a depression in the STM images depending on the dopant types and the bias. Also, using low temperature STM and hydrogen passivated Si(100), the spatial profiles of the local density of states and the charge states of As donors has been studied. [240]. The donor states of As dopant in hydrogen passivated Si(100) also has been studied using the low temperature STS and differential conductance. [242] For B dopants in Si, the changes in E_v and E_c have been measured on single B dopant in H:Si(100) using STS as shown in Fig. 7.1. [231]

In this chapter, our preliminary results of STM and STS on incorporated Al dopants in Si(100) will be presented. Also, the future works to study the Al dopants in Si will be discussed.

7.2 Experimental methods

In this section, the sample preparation process is discussed. First, the sample is cleaned by the *ex situ* and *in situ* cleaning procedures as explained in section 2.3. Fig. 7.2(a) shows an optical image of Si(100) on a manipulator during *in situ* flash annealing at 1200 °C. The blue circles represent Si atoms at the top of Fig. 7.2(a). Using the UHV thermal furnace, elemental Al is then deposited at the rate of $\approx 3.89 \times 10^{14}$ atoms/(cm$^2 \cdot s$) at room temperature as shown in Fig. 7.2(b). The STM image in Fig. 7.2(b) is taken after the Al deposition at V_{tip} = -2.00 V and I_{set} = 100 pA. The areal coverage of the deposited Al on the Si(100) surface

is $\approx$ 25 %. The Al chains on the Si(100) surface are formed perpendicular to the underlying Si(100) dimer rows as shown in chapter 6. The sample in Fig. 7.2(b) is annealed to 550 °C for 1 minute to incorporate the Al atoms into Si(100) as shown in Fig. 7.2(c). After Al incorporation, both images in Fig. 7.2(c) are taken simultaneously at different bias conditions (left: V_{tip} = 2.00 V, I_{set} = 120 pA. right: V_{tip} = -2.00 V, I_{set} = 120 pA.). There are two Si(100) terraces with the S_B step edge. The (2×1) Si(100) dimer rows and buckled dimers are visible. The red circled feature in Fig. 7.2(c) are the incorporated Al in Si(100), in which we are interested. As discussed in section 6.2.2, the incorporated Al atoms appear as dark lines in the filled states images. Those dark features in the filled states image appear as the bright spheres in the empty states image, indicating that those are the incorporated Al atoms in the Si(100) surface. There are different types of Al-Si structures after incorporation in Fig. 7.2(c).

Those various Al-Si structures are discussed in Fig. 7.3. Fig. 7.3(a) and (b) are same as Fig. 7.2(c). The orange circles represent the Al atoms. The Al chains on the Si(100) are marked with green arrows in Fig. 7.3(a) and (b). Fig. 7.3(c) are the schematic drawing of the structure of the Al chain on the surface. In Fig. 7.3(c) and (d), the light gray circles represent the top most Si atoms. The darker and the smaller circles represent the Si atoms in the lower crystal planes. As shown in section 6.2.2, the Al chains on the Si(100) appear to have almost the same height the Si(100) surface in the filled states STM image. However, the Al chain appears to have one atomic height in the empty states. Another feature marked with an orange arrow is the pyramid-like Al-Si cluster. [243] Fig. 7.3(e) taken from Ref. [243] are

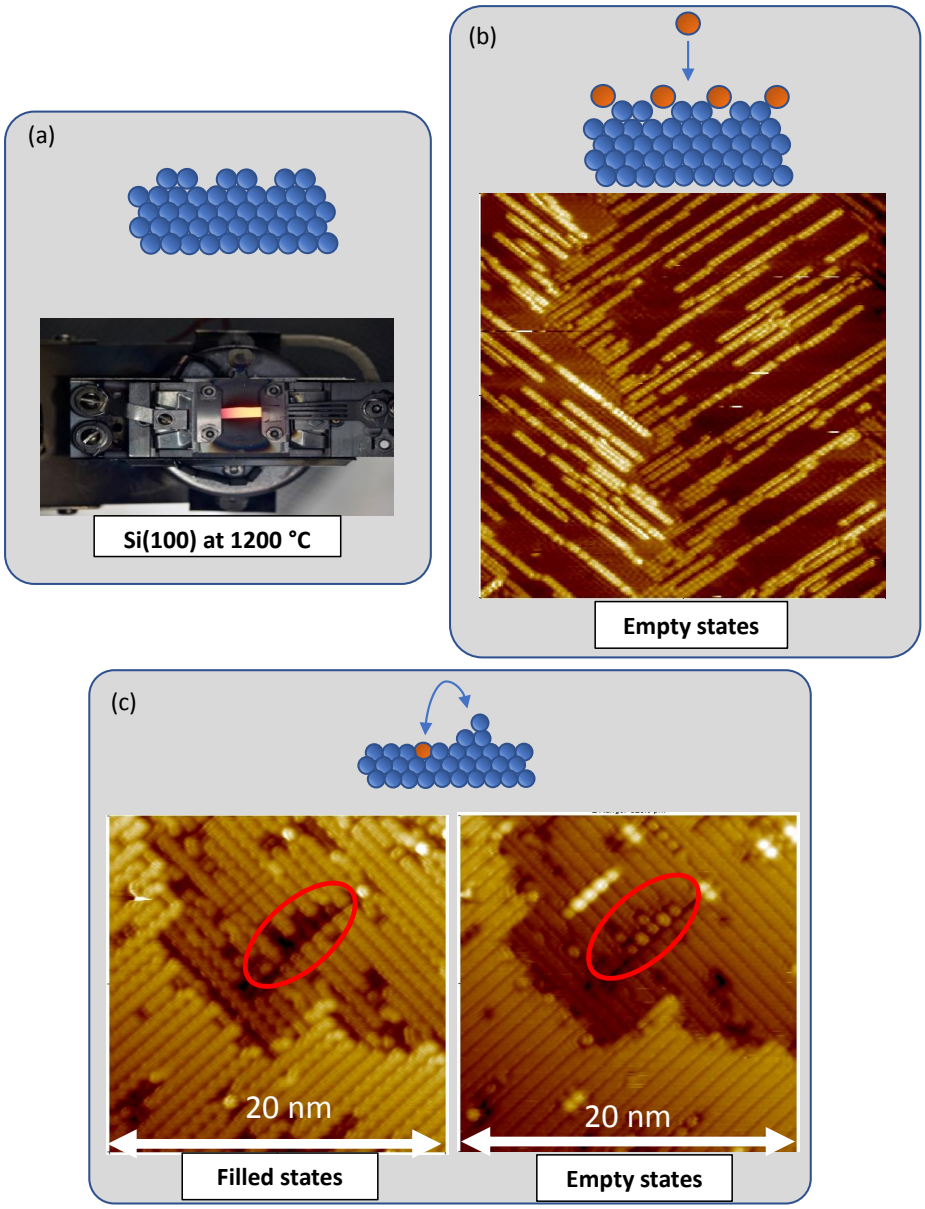

Fig. 7.2: Schematic drawings and STM images of the sample preparation process. (a) This shows the *in situ* flash annealing process to remove the chemically grown SiO_2 and achieve the clean (2×1) reconstructed Si(100) surface. The blue circles represent Si atoms. The optical image shows a Si(100) chip on the manipulator in UHV during 1200°C *in situ* flash annealing. (b) Using the UHV thermal furnace, elemental Al is deposited at room temperature. The estimated areal coverage of the deposited Al on the Si(100) surface is ≈ 25 %. The STM image shows the Al chains growing perpendicular to the underlying Si(100) dimers. The Al chains on two different terraces form perpendicularly to each other. (c) The sample in (b) is annealed to 550 °C for 1 minute to incorporate the Al atoms into Si(100). Using dual-bias mode, both STM images are taken simultaneously. The feature in the red circle is the incorporated Al in Si(100). Other Al-Si features are discussed in Fig. 7.3.

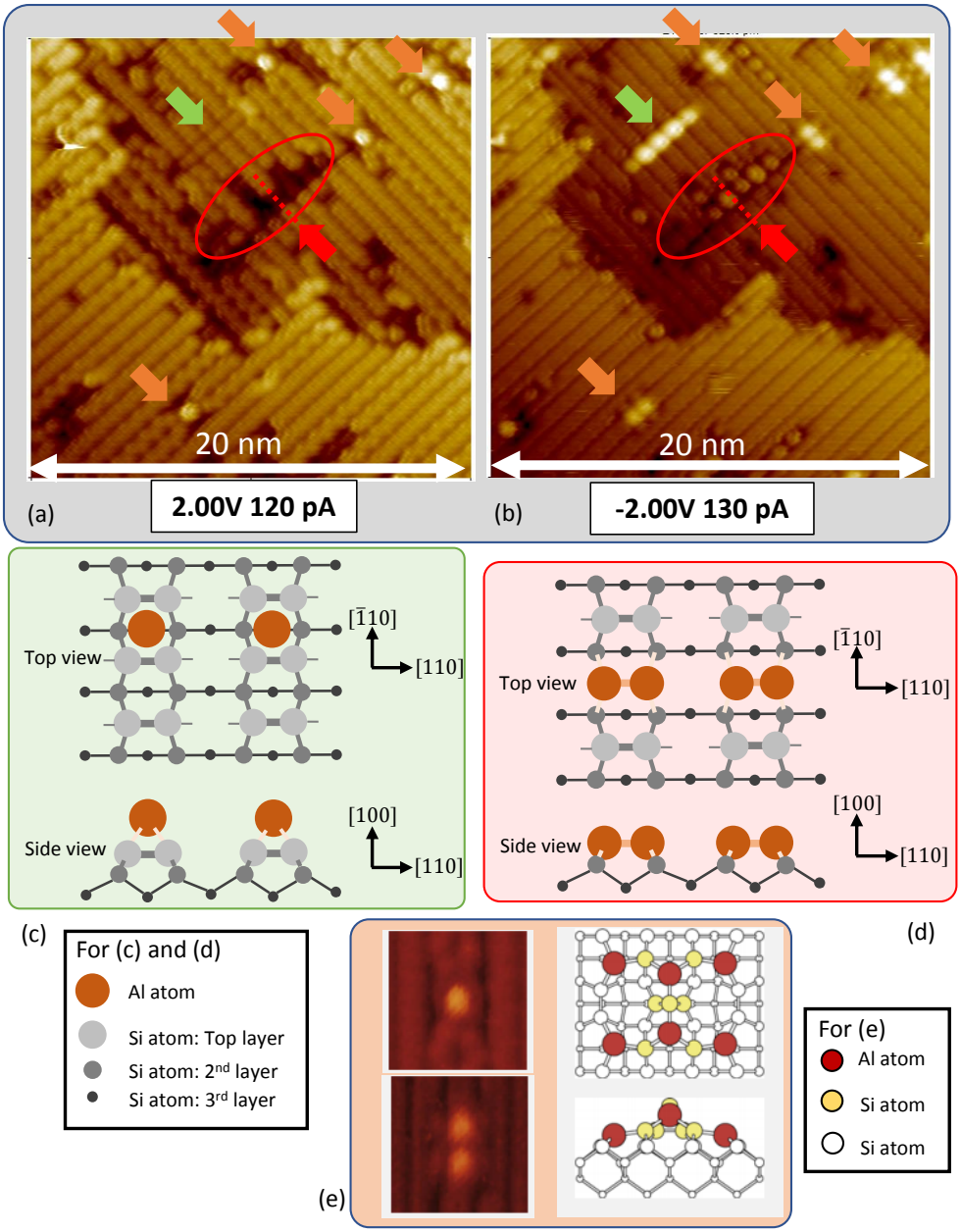

Fig. 7.3: (a) and (b) are the STM images taken simultaneously at V_{tip} = 2.00 V, I_{set} = 120 pA and V_{tip} = -2.00 V, I_{set} = 130 pA. They show two terraces with (2×1) Si(100) dimer rows. In (c) and (d), the light gray circles represent Si atoms at the top surface. The small darker gray circles are Si atoms in the 2nd layer. The small black circles are Si atoms in the 3rd layer. (c) The schematic drawing of the Al atoms (orange circles) forming a chain on the Si(100) surface, which is marked with a green arrow in (a). The Al chains are discussed in chapter 6. (d) This is a schematic drawing of the incorporated Al atoms in Si(100), which are marked with red circles and arrows in (a) and (b). Incorporated Al atoms replace Si atoms in the Si(100) surface. (e) This is taken from Ref. [243]. The features with orange arrows in (a) and (b) are the Al-Si clusters, which are not a Al doped Si diamond structure. Those are pyramid like (4×3) Al-Si clusters. The STS spectra in Fig. 7.4 are taken along the red dashed lines in (a) and (b).

the STM images of Al-Si clusters taken at V_{tip} = 2.00 V (top) and V_{tip} = -2.00 V (bottom). The schematic drawing shows the top view and the side view of the crystal structure of pyramid-like Al-Si clusters. This is not a Al doped Si diamond structure. Therefore, we studied the incorporated Al in Si(100) marked with red circles and arrows in Fig. 7.3(a) and (b). The STS spectra shown in Fig. 7.4 are taken along the red dashed line shown in Fig. 7.3(a) and (b).

The STS spectra shown in Fig. 7.4 are taken using the lock-in technique as explained in the section 2.2.2. The tip moves along the red dashed line in Fig. 7.3(a) and (b) in a constant tunneling mode. While measuring $I(V)$ spectra, the STM feedback is turned off to maintain a fixed separation between the tip and the sample. After obtaining the $I(V)$ characteristic at one position, the STM feedback is turned on. Then, the tip moves to the next position in a constant tunneling mode. Therefore, the $I(V)$ spectra along the red dashed line were measured at a constant tunneling impedance. The AC voltage with a frequency of 700 Hz and voltage of 30 mV is mixed with a DC bias. While sweeping a DC bias between ± 2.5 V, the $\frac{dI}{dV}$ is simultaneously measured using the lock-in technique. The real-part of the lock-in signal is same as the numerically taken $\frac{dI}{dV}$ from the $I(V)$ spectra. In the next section, the STS results on the incorporated Al in Si(100) are presented.

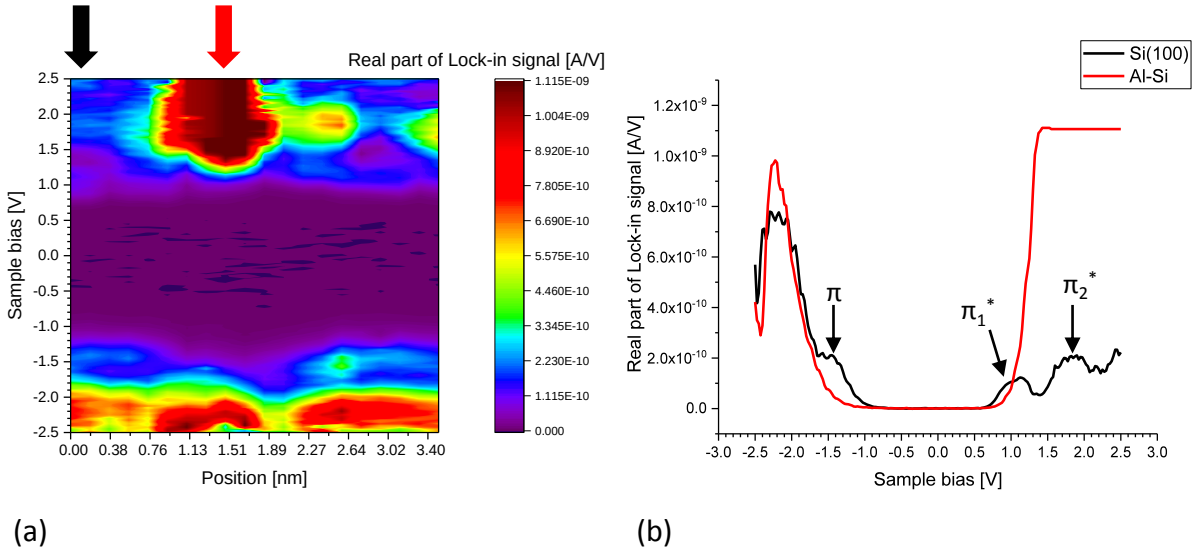

Fig. 7.4: (a) This color map is the $\frac{dI}{dV}$ taken by the lock-in technique. The color scale is the real part of the lock-in signal (A/V). The x-axis is the position, which is the red dashed line in Fig. 7.3(a) and (b). The y-axis is the sample bias (V). It shows the change in the band edges and peaks. (b) This plot shows the $\frac{dI}{dV}$ on the Si(100) dimer (black line) and the incorporated Al (red line). The STS spectra on the Si(100) dimer shows the surface states from the (2×1) reconstructed dimer, such as π, π_1^*, and π_2^*. The surface states disappear on the red line on the incorporated Al in Si. The incorporated Al in Si shows the changes in the band edges of E_v and E_c.

7.3 Scanning tunneling spectroscopy on the incorporated Al in Si(100)

In this section, using the lock-in technique, the STS on the incorporated Al in Si and neighboring Si dimers are measured as shown in Fig. 7.3(a) and (b). Fig. 7.4(a) is the $\frac{dI}{dV}$ measured by the lock-in technique along the red dashed line in Fig. 7.3(a) and (b). The color scale is the real part of the lock-in signal (A/V), which is $\frac{dI}{dV}$. As explained in section 2.2.2, $\frac{dI}{dV}$ is proportional to the local density of states of the sample. The x-axis of Fig. 7.4(a) is the position along the red dashed line in Fig. 7.3(a) and (b). The y-axis is the sample bias (V); therefore, the positive bias

is the conduction band. The negative bias is the valence band. E_F of the sample is at sample bias = 0 V.

The STS of the incorporated Al are between x ≈ 0.8 nm and x ≈ 2 nm in Fig. 7.4(a), while the outside of that range is the Si(100) dimers. Fig. 7.4(b) shows two $\frac{dI}{dV}$ spectra from a Si(100) dimer (black line) and the incorporated Al (red line), which are indicated in Fig. 7.4(a) with black and red arrows. The STS on the Si dimers shows the surface states from the (2×1) Si(100) dimer, such as π, π_1^*, and π_2^* as explained in section 5.4. On the incorporated Al, the peaks from π and π_1^* bonding states disappear. Then, at the high sample bias > 1.2 V, the lock-in signal is above the measurement limit, which is because the tunneling current above 1.2 V reaches the maximum limit of the STM (> 3 nA). The band edges of E_c and E_v change between Si(100) and the incorporated Al in Si. However, the $\frac{dI}{dV}$ on the incorporated Al does not show the change in the E_F as p-type dopant, which means that for p-Si(100), E_F is closer to the valence band as shown in Fig. 7.1. In our study on the Al delta-doped Si with the mesa-etched Hall bar devices, we found that the dominant charge carrier is the hole or the p-type dopant. The previous STS study of the B dopant in Si shows the shift of E_F toward E_v as shown in Fig. 7.1. [231] However, the previous STS experiments on dopants in Si are done with H:Si(100). [231,238–242] The surface states of Si(100) dimers are charged states that affect the electron tunneling. Also, the surface states pin the surface band-bending as explained in section 5.4. Therefore, the $\frac{dI}{dV}$ of the incorporated Al in Fig 7.4 may not be just density of states from the incorporated Al. In order to obtain the true local density of states of the incorporated Al in Si, the surface states need to be

eliminated. Hydrogen passivation is one of the well-known method to eliminate the surface states with previously demonstrated STS data by other groups. In section 6.2.2, we have demonstrated a clean H:Si(100) in the deposition chamber, which we can easily adopt to the STS experiments with the incorporated Al in Si.

First, using the P implanted samples in chapter 5, STS on the various types of Si(100) and H:Si(100) are measured as shown in Fig. 7.5. The curves in Fig. 7.5 are $(\frac{dI}{dV})/(\frac{I}{V})$ from DC $I(V)$ characteristics. Each curve is averaged over tens of curves on the (2×1) Si(100) or (2×1) n^+-Si(100) dimers. The two curves shown on Fig. 7.5(a) are taken on the Si(100) substrate (black curve) and the implanted region of n^+-Si(100) (red curve). Both curves show three surface states from the (2×1) Si(100) dimer of π, π_1^*, and π_2^*. The π peak for both Si(100) and n^+-Si(100) are same at ≈ 0.5 eV indicating the E_F pinning. [190]. However, the π_1^* and π_2^* are shifted closer to E_c for n^+-Si(100) (red curve). [190, 244]

The sample in Fig. 7.5 is passivated with the single atomic layer of hydrogen as described in section 2.4.4. The STS spectra on H:Si(100) is measured on n^+-Si(100) dimers. The π and π_1^* disappear after H passivation. Also, E_F is positioned close to E_c. Using STM lithography, the passivated hydrogen atoms are removed as described in section 2.2.3. Then, the STS spectra on H depassivated region are measured, which is the blue curve shown in Fig. 7.5(b). The π_1^* and π_2^* peaks appear again at the same positions as before H passivation (red curve).

Then, the STS spectra on the H passivated Si(100) substrate are also taken as shown in Fig. 7.5(c). The red curve is from Fig. 7.5(b). The black curve is measured on H:Si(100). E_F is different between the H:Si(100) substrate and H:n^+-Si(100).

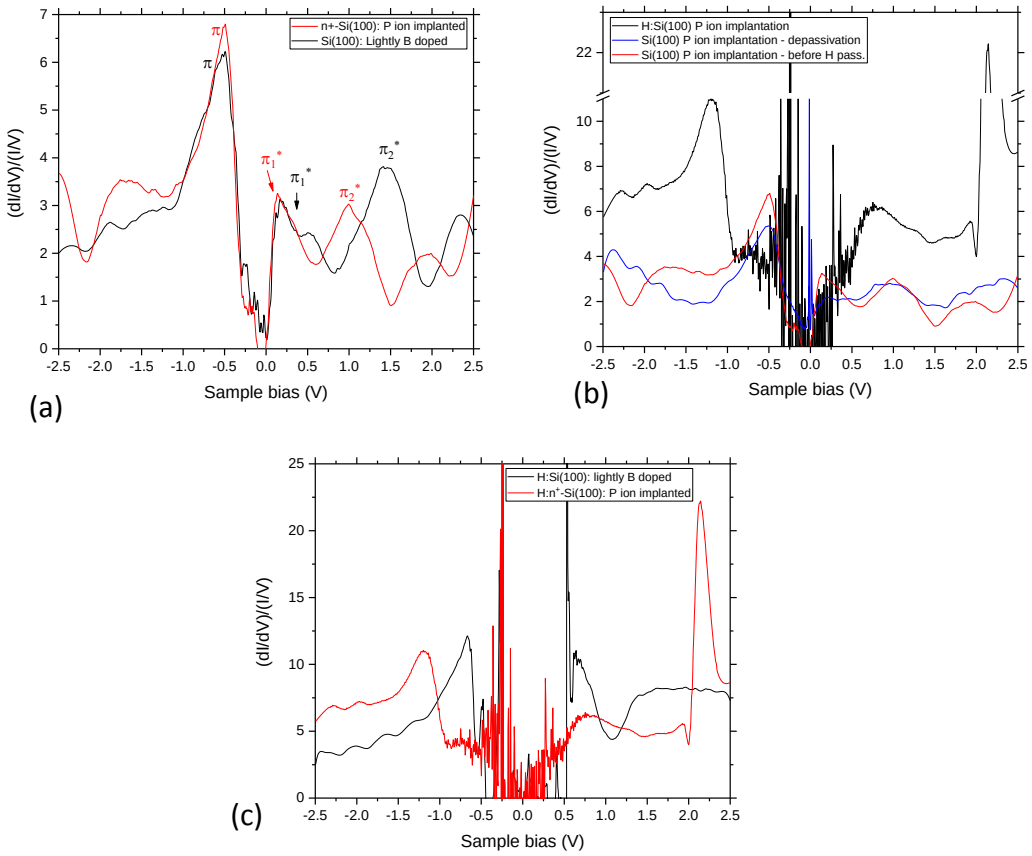

Fig. 7.5: All the STS are taken at the same STM set point at V_{tip} = 2.00 V and I_{set} = 100 pA. All the curves are numerically calculated $(\frac{dI}{dV})/(\frac{I}{V})$. Each curve is averaged over tens of $I(V)$ characteristics. (a) This sample is the P implanted (n^+-Si(100)) in the p-Si(100) substrate (B-doped). The black curve is measured on the substrate. The red curve is measured on n^+-Si(100). π peaks at $\approx$ -0.5 eV are same for both substrate and the n^+-Si(100) indicating the pinned band-bending. The anti-bonding peaks are shifted closer to the E_F. (b) This sample is passivated with atomic layer of hydrogen (H:Si(100)). The red curve is same as (a). The black curve is taken on the n^+-H:Si(100). The π, π_1^* peaks disappear. The surface band gap becomes larger compared to n^+-Si(100) by eliminating pinning at the surface states. Then, using the STM lithography, the hydrogen atoms are removed. The blue curve is taken on the depassivated area, which is n^+-Si(100). The π, π_1^*, and π_2^* peaks are positioned as same as before the passivation. (c) This plot shows the change of the band edges between the H:Si(100) substrate and the n^+-Si(100). The red curve is from the n^+-Si(100) as in (b). The black is taken on the H:Si(100) substrate. As expected, by eliminating the surface states, on the highly P doped region, E_F is positioned closer to the E_c. E_F on the substrate is positioned at the middle of the band gap.

While E_F on H:n$^+$-Si(100) is closer to E_c, E_F on the H:Si(100) substrate is positioned near the mid-gap of E_i as described in section 5.4. By eliminating the surface states of (2×)Si dimers, effect of dopants to E_F is observed similar to B dopants in Si as shown in Fig. 7.1. Therefore, H passivation would allow us to observe the local density of states of the incorporated Al in Si.

Our STS spectra on the various types of Si(100) and H:Si(100) show good agreement with the previous studies of STS on Si(100) and H:S(100). [190, 244] The next step to study the density of states of the incorporated Al in Si using STS is to eliminate the surface states by H passivation. As previous STS studies of other dopant in Si, elimination of the surface states will allow us to study the true local density of states of the incorporated Al in Si by removing the pinning of the band bending and charged surface states. [231, 238–242]

7.4 Summary

In this chapter, the incorporated Al in Si is identified using STM. The STS spectra of the incorporated Al in Si show the disappearance of the π and π_1^* peaks and the change of the band edges. However, due to the existence of the surface states of the (2×1) Si(100) surface, the STS spectra has not been shown the impurity states of Al dopants or the shift of E_F closer to E_v.

In order to study the true density of states of the incorporated Al in Si, the hydrogen passivation after Al incorporation needs to be done to eliminate the surface states. As the first step toward STS study of incorporated Al dopant with H:Si(100),

I have measured the various types of Si(100), n^+-Si(100), H:Si(100), and H:n^+-Si(100), which are in a good agreement with previous STS studies. In the future, the incorporated Al with H passivation will be studied using STS with expectation to observe the shift of the E_F similar to B dopants in Si or the impurity states of the Al dopant in Si. [231]

Chapter 8

Summary of Results and Future Experiments

8.1 Summary

This thesis covers developments of new semiconductor material, an imaging technique, and experimental protocols for new candidate dopants for STM lithography toward developing new proposed superconducting semiconductor qubits.

In chapter 4, we have successfully fabricated a quasi two-dimensional hole gas in Si using a monolayer of Al sandwiched in Si. We found the dominant charge carrier in the Al delta-doped Si is hole. We found that the charge carrier density and and the Hall mobility are $\approx 1.39 \times 10^{14}$ cm^2 and ≈ 20 cm$^2/V \cdot s$, which are comparable to the similar system of B delta-doped Si. [156] The extracted charge carrier density corresponds to $\approx (0.93 \pm 0.1)$ hole per Al dopant, compared to the measured dosing density using STM. STM and STEM show a clean epitaxial Si(100) with low density of defects, and crystallinity with no defects in the Al enriched region, respectively.

APT and EDS find Al dopant re-distribution over $\approx$ (17 - 25) nm, which results

in a reduction of the peak 3D Al density to only 10 % of the predicted density needed to observe superconductivity in B doped Si. The $R_{\square}$ measured below 50 mK does not show superconductivity, likely due to the reduction of the peak Al 3D density. The reduction of the Al density could be caused by 550 °C annealing to activate Al doapnts and recrystallize the polycrystalline Si overgrown at room temperature.

Chapter 5 demonstrated the *in situ* detection of ion implanted wires for P and As dopants in the various substrates using the real-time STS mapping with the lock-in technique. The STM topography and the real-time STS mapping for different bias are simultaneously measured. The change in E_F due to the doping density causes the change in the local density of states of the sample, and change in C_{gap} between the sample and the tip at a fixed bias resulting in contrast on the real-time STS mapping. However, during the *in situ* high temperature flash annealing, B dopants diffuse in the substrate or out-diffuse into vacuum; therefore, the patterns of the implanted wires are no longer visible or feasible for contacts. KPFM measuring the change in the surface workfunction as shown in Eq. 5.7 between the AFM tip and the sample, confirms the real-time STS mapping by detecting the change in the workfunction between the substrate and the implanted region due to the change in the doping density.

Using the P implanted wires and STM lithography, nanowires made of P dopants in Si are fabricated and characterized. The P implanted wires and the real-time STS mapping using the lock-in technique reduce the fabrication process time by using photolithographically defined ion implantation at the wafer scale compared to chip-by-chip electron beam lithography. This method also enables the ability to

realize the electrical connection to the STM patterned nanodevices *in situ*, and is a unique advantage of this method over contemporary contacting methods. Especially, the As implanted wires show less diffusion due to the larger activation energy and can bring the tip of the implanted wires closer, which reduces the STM patterning time and the contamination from the background gasses.

Chapter 6 shows experimental protocol to test candidate dopants for STM lithography with the hydrogen resist layer. Elemental Al has been tested for three methods; direct hydrogen resist layer protection, lift-off, and surface diffusion. Elemental Al using PVD is adsorbed to the hydrogen resist layer due to the low vapor pressure to form clusters, which can cause an unintentional electrical path through the outside of the devices. The lift-off process by thermally desorbing the hydrogen resist layer is not successful due to the low vapor pressure of Al. The substantial reduction of the deposition rate by 50 times does not reduce the number density of Al clusters limited by surface defects. Based on our tests, elemental Al is not compatible with the hydrogen resist layer for STM lithography. However, based on the calculation of the evaporation rate of various dopants for Si, As and Sb are good candidates for STM lithography with the hydrogen resist layer.

Chapter 7 shows the change in the band edges between the Si(100) substrate and the incorporated Al in Si using STS and STM. However, due to contribution to the electron tunneling from surface states, the STS spectra does not the shift of E_F closer to E_v or the impurity states of the p-type dopant. We have measured the STS spectra of various types of Si dimers, such as Si(100), H:Si(100), n^+-Si, and H:n^+-Si. Those STS spectra are in good agreement with previous STS studies from

other groups.

Each chapter of this thesis is a building block to fabricate new interface free quantum information devices, which can combine superconducting circuits and semiconductor qubits. Especially, our capability to fabricate ^{28}Si in the same vacuum system with the atomic layer deposition of the elemental Al and UHV STM gives us a potential to make an impact on the field of Si-based solid state quantum computing.

8.2 Proposals for Future Experiments

8.2.1 Superconducting semiconductor in the Al delta-doped Si

Chapter 4 shows the first reported Al delta-doped Si with the high charge carrier density of hole and Hall mobility similar to B delta-doped Si. However, the 550 °C annealing process for 10 minutes causes the Al diffusion resulting in the reduction of the peak Al 3D density; therefore, superconductivity in the Al delta-doped Si is not observed. This process is designed to optimize the dopant activation, which are based on the *ex situ* RTA results in Fig. 4.3. In order to increase the peak Al concentration in Al delta-doped Si, the next step is to optimize thermal process while maintaining crystallinity and reducing Al dopant diffusion.

The capping Si layers of the 1^{st} and 2^{nd} generation samples are grown at room temperature, which result in polycrystalline Si. The polycrystalline Si significantly affects the dopant activation in Si. [245] Therefore, the epitaxial Si capping layer is required to activate the Al dopants in Si, which also require the Si deposition at

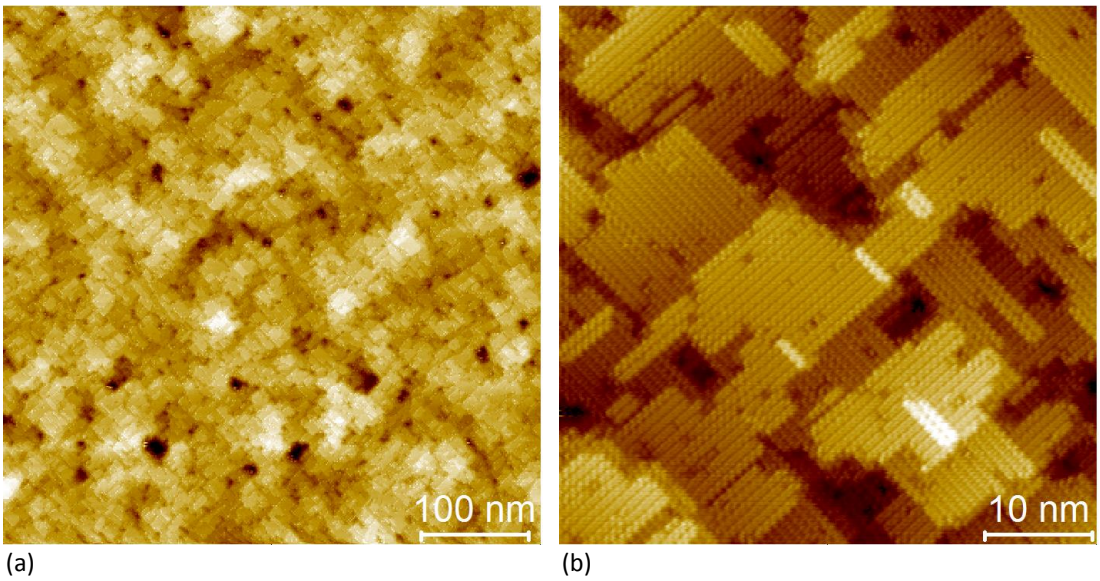

Fig. 8.1: STM images of ≈ 30 nm Si grown at 332 °C. (a) This is a large area scan (500 nm × 500 nm). Compared to Si grown at 450 °C as shown in Fig. 3.12, the surface is rougher with 3D growth mode-like surface. The valleys (dark features) and small islands are visible. (b) This is a small area scan (50 nm × 50 nm). It shows a clean (2×1) Si(100) with the low density of surface defects. Small Si(100) islands are visible.

the elevated temperature. In previous studies of the delta-doped Si, the epitaxial Si could be grown as low as 300 ° [69, 76–79] As the substrate temperature decrease, in order to achieve the epitaxy, the deposition rate also has to decrease. The Sb-delta layer with a width in the range of 1-10 nm in Si uses ≈ 0.4 - 0.6 nm /min. [69, 76–79] The maximum deposition rate of our current thermal Si evaporator is ≈ 0.14 - 0.16 nm/min, which is compatible with low temperature MBE. Therefore, the epitaxy of the overgrown Si layer at ≈ 300 - 330 °C is possible.

I have grown ≈ 30 nm of Si at 332 °C as shown in Fig. 8.1. Compared to the STM images of Si grown at 450 °C shown in Fig. 3.12, the STM image of the large area (500 nm × 500 nm) is rougher with islands and valleys (dark features). At the same deposition rate, as the substrate temperature decrease, the surface diffusion

of Si adatoms decreases, resulting in rougher surface or 3D like growth mode. The STM image of the small area (50 nm × 50 nm) as shown in Fig. 8.1(b) shows a clean (2×1) Si(100) surfaces with dimer rows and terraces. The STM images in Fig. 8.1 show good epitaxial Si(100) with very low density of surface defects.

Using the diffusion coefficient modeled with extrinsic effects and dopant concentration as discussed in section 4.3.2, the Al diffusion at 330 °C for 7 hours to deposit ≈ 60 nm of Si is estimated to be zero. As demonstrated in Fig. 8.1, the Si can be grown epitaxially at ≈ 330 °C, which is a low enough temperature to minimize the dopant diffusion during Si deposition.

Also, limitation of the current Si evaporator is the low deposition rate of ≈ 0.15 nm/min, which is 2 times lower than other delta-doped Si and low temperature Si MBE. By increasing the deposition rate, the Si capping layers will be exposed to the background gasses for a shorter period of time, which can reduce the contamination. We are also currently upgrading the Si evaporation source to a UHV e-beam evaporator with a liquid nitrogen cryoshroud. The new e-beam evaporator is designed to heat a small area of the Si evaporation source at the center in order to minimize outgassing from other parts of the evaporator. Also, the liquid nitrogen cryoshroud mounted on top of the e-beam evaporator can pump the contaminants, such as H_2O, C, O, etc.

Using the upgraded e-beam evaporator for Si deposition and the Si deposition at ≈ 330 - 330 °C, the epitaxial Al delta-doped Si with less Al diffusion and contamination can be achieved to pursue superconductivity in highly Al delta-doped Si.

8.2.2 Scanning Tunneling Spectroscopy on the incorporated Al with H passivation

In chapter 7, using STM, the incorporated Al and other Al-Si structures are shown in Fig. 7.3. Also, the changes in the band edges of the incorporated Al in Si are demonstrated. However, due to the surface states, the STS spectra of the incorporated Al in Si does not show a shift of E_F or the impurity states as p-type dopant in Si in Fig. 7.4. H passivation can eliminate the surface states and observe a shift of E_F as a doping density changes. Therefore, using H passivation, the STS spectra can show the local density of states of incorporated Al dopants in Si. As a first step, I demonstrated a clean H passivated Si(100) in Fig. 2.25 and STS in section 7.3.

We have passivated the Si(100) surface after Al incorporation as shown in Fig. 8.2. All STM images in Fig. 8.2(a) - (d) are the empty states images taken at V_{tip} = - 2.00 V and I_{set} = 100 pA. On a clean (2×1) Si(100) surface, the Al with the area coverage of ≈ 10 % is deposited at room temperature. Then, the sample is annealed to 550 °C for 1 minute for Al incorporation as shown in Fig. 8.2(a). The bright spheres of the incorporated Al in Si are visible. There are also two Al-Si clusters. This sample is then passivated with single atomic layer of H as described in section 2.4.4. Fig. 8.2(b) is taken after H passivation. The (2×1) Si(100) dimer rows are visible. Compared to Fig. 8.2(a), more bright features with various shapes appear. They can be dangling bonds, contaminants, other Al-Si formations, etc. Based on the STM topography in Fig. 8.2(b), it is difficult to figure out the Al

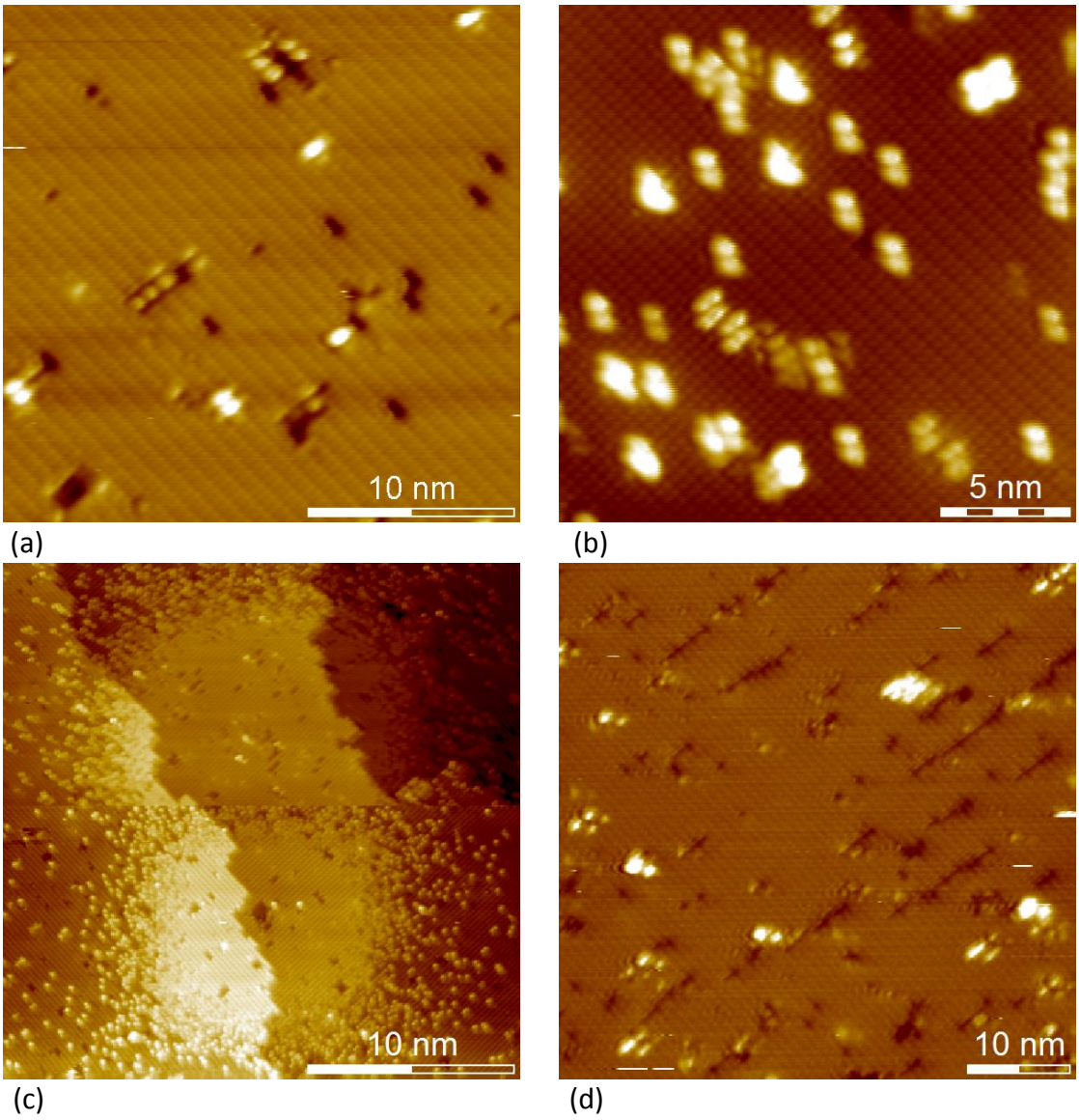

Fig. 8.2: The empty states STM images taken at V_{tip} = - 2.00 V and I_{set} = 100 pA. (a) After Al deposition with area coverage of ≈ 10 %, the sample is annealed to 550 °C for 1 minute to incorporated Al into Si. The (2×1) Si(100) dimer rows are visible. The bright features of 3 spheres are the incorporated Al. Two Al-Si clusters are also visible. (b) The sample in (a) is passivated with single atomic layer of H. Compared to (a), there are more bright features with various shapes, which can be dangling bonds, contaminants, or other reconstructed Al-Si. (c) Using the STM lithography, the H atoms are depassivated in two bright squares. Two step edges are visible. The dark lines or bright spheres of the incorporated Al are not visible within the depassivated area. (d) The sample in (c) is annealed to 550 °C for 1 minute to thermally desorb the H layer. The dark line growing perpendicular to the (2×1) dimer rows appear. However, the bright spheres of the incorporated Al in Si are not visible.

dopants in Si. Using STM lithography, the H atoms on Fig. 8.2(b) are removed. The large rectangle area in Fig. 8.2(c) is the depassivated area. Within the depassivated area, the dark features of the incorporated Al are not visible. During H passivation, the substrate is held at $\approx$ 300 °C, which can cause the Al atoms to diffuse to the subsurface. Another possibility is that the H atoms may react to the Al atoms to form reconstructed structures.

This sample is then annealed to 550 °C for 1 minute to thermally desorb the H layer as shown in Fig. 8.2(d). The dark lines appear again; however, the bright spheres of the incorporated Al are not found after annealing. The bright spheres of the incorporated Al are at the top surface as shown in Fig. 7.3. The dark lines could be Al atoms a few atomic planes below the surface. Those also can be contaminants from H passivation even though we have not observed the contamination from other H passivation test on the Si(100) substrate. There are more features that have not been observed before after H passivation on the incorporated Al sample as shown in Fig. 8.2(b). If those bright features were contaminants, such as F or Cl, the dark lines in Fig. 8.2(d) could be contamination not Al dopants. Or if they are Al dopants in Si, then a clean H:Si(100) is needed without unknown bright features on the H:Si(100) surface. Typically, single dopants in Si appear as a protrusion or a depression in the STM images as discussed in section 7.1. Therefore, the next step to study STS spectra of the incorporated Al in Si is to achieve a clean H:Si(100) after Al incorporation.

In order to have a well controlled sample, after Al incorporation, a several monolayers of Si can be overgrown. Then, the sample can be passivated with hydro-

gen. This could eliminate the possible reaction between H and Al on the surface.

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