ABSTRACT

Title of Dissertation: NANO-ENGINEERING OF DENSELY PACKED ELECTROCHEMICAL ENERGY STORAGE ARCHITECTURES BY ATOMIC LAYER DEPOSITION

Chanyuan Liu, Doctor of Philosophy, 2016

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Nanostructures are highly attractive for future electrical energy storage devices because they enable large surface area and short ion transport time through thin electrode layers for high power devices. Significant enhancement in power density of batteries has been achieved by nano-engineered structures, particularly anode and cathode nanostructures spatially separated far apart by a porous membrane and/or a defined electrolyte region. A self-aligned nanostructured battery fully confined within a single nanopore presents a powerful platform to determine the rate performance and cyclability limits of nanostructured storage devices. Atomic layer deposition (ALD) has enabled us to create and evaluate such structures, comprised of nanotubular electrodes and electrolyte confined within anodic aluminum oxide (AAO) nanopores. The V_2O_5- V_2O_5 symmetric

nanopore battery displays exceptional power-energy performance and cyclability when tested as a massively parallel device (~2billion/cm^2), each with ~1μm^3 volume (~1fL). Cycled between 0.2V and 1.8V, this full cell has capacity retention of 95% at 5C rate and 46% at 150C, with more than 1000 charge/discharge cycles. These results demonstrate the promise of ultrasmall, self-aligned/regular, densely packed nanobattery structures as a testbed to study ionics and electrodics at the nanoscale with various geometrical modifications and as a building block for high performance energy storage systems[1, 2].

Further increase of full cell output potential is also demonstrated in asymmetric full cell configurations with various low voltage anode materials. The asymmetric full cell nanopore batteries, comprised of V_2O_5 as cathode and prelithiated SnO_2 or anatase phase TiO_2 as anode, with integrated nanotubular metal current collectors underneath each nanotubular storage electrode, also enabled by ALD. By controlling the amount of lithium ion prelithiated into SnO_2 anode, we can tune full cell output voltage in the range of 0.3V and 3V. This asymmetric nanopore battery array displays exceptional rate performance and cyclability. When cycled between 1V and 3V, it has capacity retention of approximately 73% at 200C rate compared to 1C, with only 2% capacity loss after more than 500 charge/discharge cycles. With increased full cell output potential, the asymmetric V_2O_5-SnO_2 nanopore battery shows significantly improved energy and power density. This configuration presents a more realistic test - through its asymmetric (vs symmetric) configuration – of performance and cyclability in nanoconfined environment.

This dissertation covers (1) Ultra small electrochemical storage platform design and fabrication, (2) Electron and ion transport in nanostructured electrodes inside a half cell configuration, (3) Ion transport between anode and cathode in confined nanochannels in

symmetric full cells, (4) Scale up energy and power density with geometry optimization and low voltage anode materials in asymmetric full cell configurations. As a supplement, selective growth of ALD to improve graphene conductance will also be discussed[3].

NANO-ENGINEERING OF DENSELY PACKED ELECTROCHEMICAL ENERGY STORAGE ARCHITECTURES BY ATOMIC LAYER DEPOSITION

By

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Dissertation submitted to the Faculty of the Graduate School of the
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Dedication

To my family

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Contents

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Chapter 1. Background and Motivation

Li ion batteries play an important role in many aspect of our life, which are widely used as power supply for portable electronics, electric vehicles, and smart power grid and so on. A lithium ion battery is composed by two kinds of ion storage materials with different chemical potential when immersed in electrolyte. As shown in Figure 1, typical negative and positive electrode are graphite and $LiCoO_2$ as positive electrode, they are also called anode and cathode. During a discharging process, lithium ions move from anode to cathode through electrically insulating electrolyte, while electrons travel through outside circuit and generate electricity. This process is reversible during battery charging. Traditional batteries are composed of micron sized Li ion storage particles. They are randomly mixed with carbon black and binder, creating tortuous and uncontrolled electron and ion transport paths, which leads to long charging time. However, efficient and fast transport of both electrons and ions is required for high performance electrical energy storage, with ion transport through electrolyte between active storage electrode materials and current collectors for power exchanges with the external charging or load circuit.

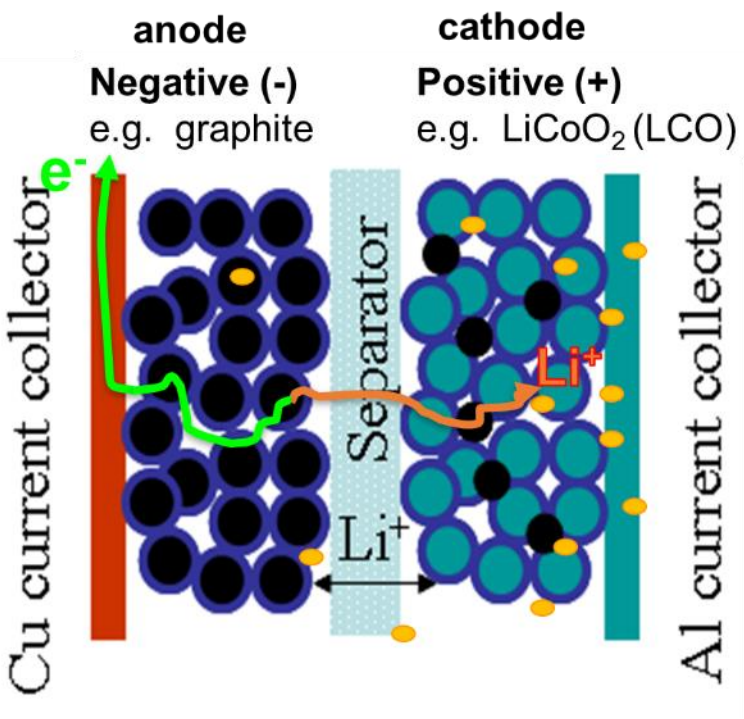


Figure 1 Schematic of a traditional lithium ion battery configuration with micronized storage materials and torturous electron and ion pathways. (Adapted and modified from UMD ENMA698N slides)

Nanostructured electrodes hold great promise for future electrical energy storage devices: the large surface area and short ion transport time through the electrode enables high energy storage at any given power density; and the enhanced mechanical properties under strain can facilitate the fabrication of flexible architectures. Moreover, power and energy metrics can be further improved if anode and cathode nanostructures could be brought into close proximity in a full cell configuration. Rolison et al[4] have reported a random network architecture based on nanoporous, interconnected scaffolds on which conformal layers of anodic, electrolyte, and cathodic materials are sequentially deposited to form a battery. In alternative, interdigitated three-dimensional (3D) architectures should allow denser packing of active storage electrodes at the micro or nano scale [5], However,

only a limited number of these regular 3D micro- or nanoscale batteries have been fabricated that can operate successfully [6-8].

A fully interdigitated 3D electrostatic nanocapacitor was reported by Banerjee et al [9] In it, an ultrathin (~6nm-thick) dielectric was used to separate two electrodes that were self-aligned within an anodic aluminum oxide (AAO) nanopore. This nanodevice achieved record areal capacity, with an estimated high power density and an energy density increased (cf. planar) to the low range of electrochemical capacitors. Despite further performance improvements through nanoengineering [10], the intrinsically high leakage current of such ultrathin dielectrics limits charge retention, requiring hybrid electrochemical-electrostatic circuits to retain the benefits of the 3D nanoarchitecture device.[11] Replacing the dielectric with a solid-state electrolyte in principle achieve a high performance electrochemical storage device, but low ionic conductivity, interface defects and fabrication challenges pose serious challenges to this pathway toward a full storage device based on 3D parallel nanostructures[5, 12-14]

An alternative solution would be to use liquid, organic electrolytes. An example of this configuration was reported by Ajayan et al. [8] In it, AAO nanopores were used to self-align nanowires made of Ni-Sn anode and polyaniline (PANI) cathode immersed in a liquid electrolyte. However, the full cell device showed relatively low areal capacity (8-10uAh/cm2) compared to other reported values of self-assembled nanoarchitectures for energy storage [15, 16]. The relatively low capacity of this full cell, especially when compared to the performances of the half-cell configuration, has raised questions about the practicability of head to head nanowire electrodes separated by an ultrathin electrolyte layer. A key concern has been directed to the low electronic and ionic conductivities within

these high aspect ratio structures. It is possible that a significant amount of lithium ions is depleted in the nanoconfined environment near the electrode, because Li ions that are quickly transported through the solid electrolyte interface (SEI), especially when the device operates at high power, may not be replenished by Li ions from the bulk electrolyte reservoir. In addition, Li ion deficiency may also alter SEI formation and stability: higher than normal localized ion currents can be expected in this regime, as probed by STM and modelled theoretically [17, 18]. A second concern comes from the electrode morphology. Complex 3D structures may produce inhomogeneous electric fields and ionic concentration gradients with consequent high local current densities that may cause undesired reactions at the SEI and generate leakage currents. In addition, thermal inhomogeneity may also lead to device failure[19]

Besides a high performance battery, we are also interested in the fundamental science related to densely packed electrodes, since highly confined electrolyte environments are unavoidable if electrodes are densely arranged to take advantage of nanostructuring for high power storage applications. This may give rise to new scientific questions about ionics and electrodics at mesoscale, including confined ion transport in electrolyte with limited ion concentration, electron transport in ultra-thin current collectors, and even electrical double layer at the surface of dense electrodes (Figure 2). With emerging number of nanostructure applications in electrode, there is a need to systematically investigate dense architectures design for understanding of ion behavior under confined environment with high charging/discharging rate.

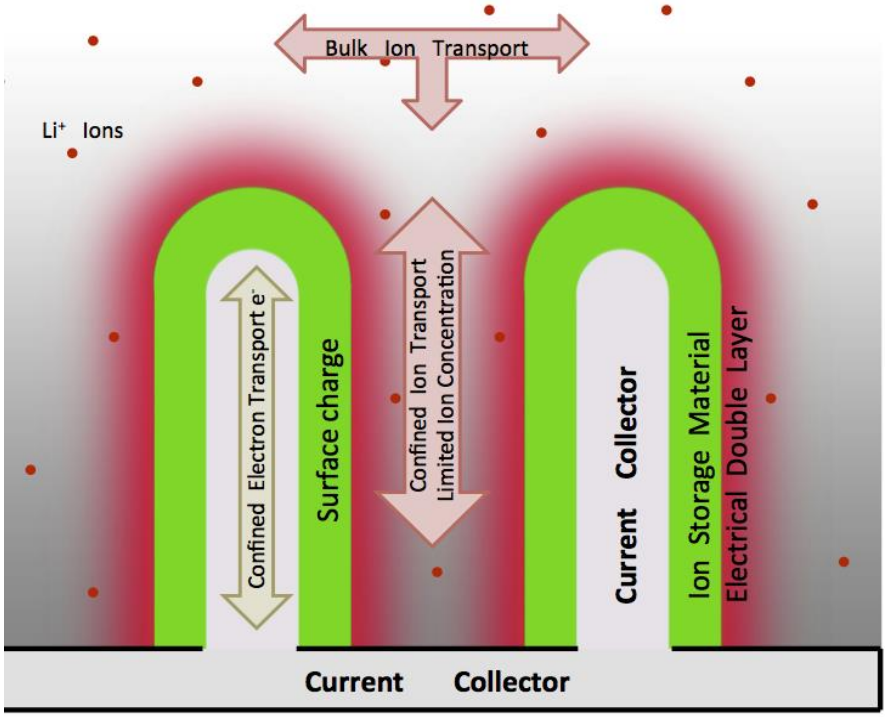


Figure 2 Scientific issues in ionics & electrodics with dense nanostructure architectures for electrical energy storage(Adapted from [20])

Chapter 2. Synergy Between atomic layer deposition (ALD) and anodic aluminum oxide (AAO)

The nanobattery structure is enabled by atomic layer deposition of various battery component materials, including anode, cathode and current collectors on electrochemically self-assembled porous AAO templates. These two techniques will be discussed in the following.

2.1. ALD and its applications in energy storage

2.1.1. Introduction to atomic layer deposition

A typical ALD reaction is composed by a binary sequence of self-limiting half-reactions, the principle of such self-limiting behavior was originally discovered as by Prof. Kol'tsov in the 1960 and named as "molecular layering". Then in the mid-1970s, Prof. Suntola and his team first introduced ALD thin film deposition technique. [21] At that time, this technique was initially called atomic layer epitaxy (ALE) and eventually adopted the name of atomic layer deposition. One of the main motivations for developing ALD technique is the semiconductor industry. ALD turn out to be commercially important when the semiconductor industry began to incorporate ALD into the manufacturing process flow to fabricate high performance complementary metal-oxide-semiconductor (CMOS) transistors in the early 2000s.

ALD is a self-limiting deposition method that enables sub-nanometer control of film thickness.[22] Unlike other thin film deposition techniques, such as sputtering and chemical vapor deposition, ALD is based on the sequential introduce of different chemical sources alternately, separated by inert gas purging, which leads to precursor saturation at

the surface during the exposure step and therefore self-limiting growth. Most of ALD processes have typical AB binary reaction sequences, where substrate is first exposed to precursor A, usually metal organics, which reacts with –OH groups at substrate surface, and form a conformal coating by self-limiting reaction, followed by purging away excess precursor and byproducts. Then the oxidant precursor B (typically H_2O) is introduced to react with the organic ligands and form a monolayer of metal oxide with –OH surface group again. After another purge step, one ALD cycle is finished with a monolayer growth. By repeating these steps, ultra-thin films can be deposited with sub-nanometer thickness control. [23, 24] This unique reaction mechanism also provides unprecedented uniformity and conformality, even on the most challenging high-aspect-ratio surfaces. [24-26]

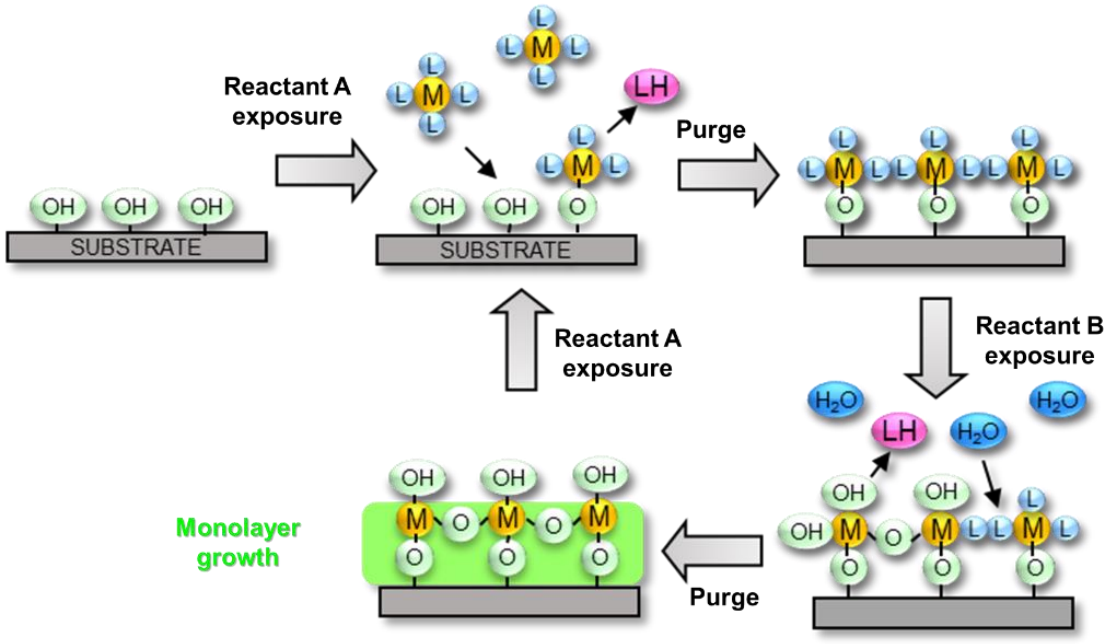


Figure 3 Schematic of self-limiting surface reaction in a metal oxide ALD process with an AB binary reaction sequence.

In semiconductor industry, ALD has been used for high-k dielectrics (eg. HfO_2) as gate oxides in the MOSFET devices, which need to be conformal and pinhole-free with well-controlled thickness in order to shrink device size and limit lower power consumption.[27, 28] Recently, ALD plays a more critical role in semiconductor processing with the introduction of tri-gate/FinFET design, where a high aspect ratio Si fin is surrounded by the gate oxide from three sides. ALD meets the harsh requirement for exceptional compositional and thickness uniformity in such 3D structures without pinholes [29]. Besides, ALD has enabled high performance DRAM fabrication by conformally depositing pinhole free dielectrics into high aspect ratio trenches. In addition, transition-metal nitrides deposited by ALD, like titanium nitride (TiN), tantalum nitride (TaN) and tungsten nitride(WN), have also been used as ultrathin diffusion barrier for copper contacts[30, 31]. Besides semiconductor industry, ALD films also act as interface buffer layer and surface passivation layer in photovoltaics [32, 33] and effective gas diffusion barriers on polymers [34, 35].

Due to the thermally activated and self-limiting reaction nature, ALD process maintains a constant growth rate within a temperature window, which is typically located from room temperature to 400C. (Figure 4) Within this window, the self-limited growth is independent from substrate temperature, while the growth rate can either increase or decrease when outside the temperature window. At low temperature, precursor usually exhibit reduced growth rate due to not energy to overcome the activation energy barrier for surface absorption and/or reaction. Higher growth rate may also happen at low temperature because of precursor condensation. On the other hand, if the temperature is too high, precursor may decompose directly on the surface which leads to a CVD process losing the

self-limiting property and has higher growth rate. Sometimes, the growth rate can also decline as a result of precursor desorption. [24, 26]

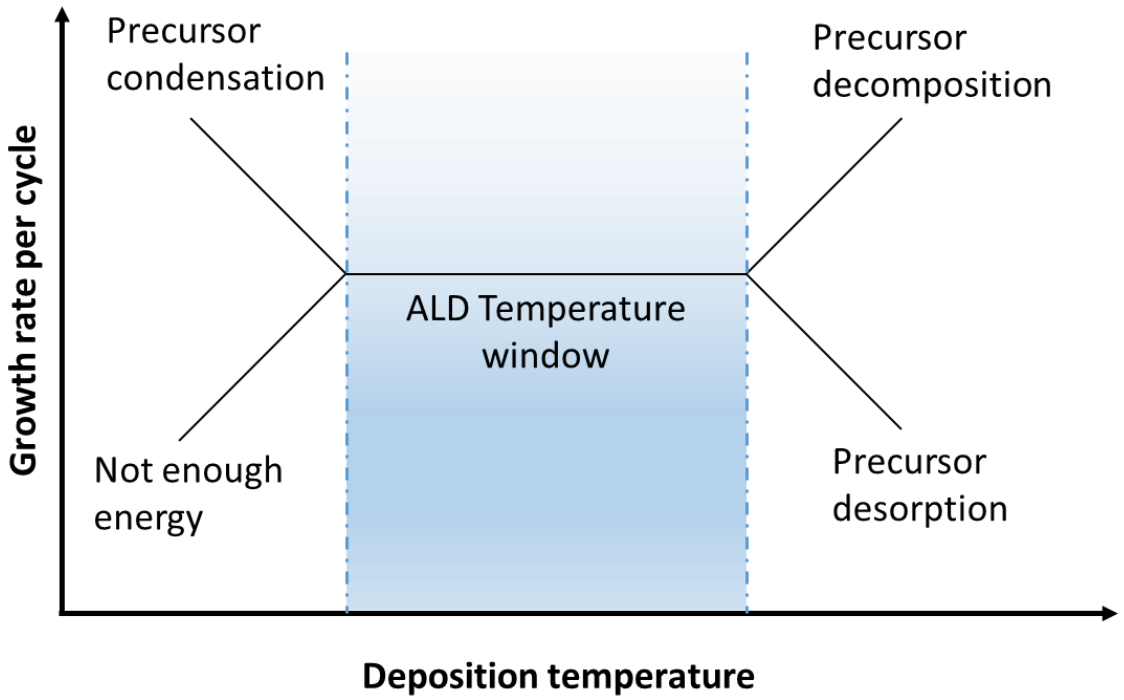


Figure 4 Schematics for ALD temperature window.

2.1.2. ALD applications in energy storage

During the recent five years, atomic layer deposition (ALD) is increasingly used as an effective technique to improve lithium ion battery performance because of its precise thickness control, unprecedented conformality in high aspect ratio 3D nanostructures and flexibility in material composition manipulation[36-38]. Emerging ALD applications in batteries are reflected by the growing number of scientific publications (Figure 5). One major research direction is to develop novel ALD process for anode [39-43] and cathode [44-49] materials, which can be further applied to high surface area 3D nano-scaffolds, reducing electron and ion transport length inside electrodes, as a result, providing high

power performance. Besides, thin lithium ion conducting films are applied onto both cathode and anode electrode materials to stabilize electrode/electrolyte interface, which creates an ion-conductive interlayer between electrode materials and electrolytes while electrically and chemically prevent the organic electrolytes from decomposition. Therefore, the chemical stability at electrode-electrolyte interface and the mechanical steadiness of electrode structure can be improved [50-53]. Moreover, solid-state electrolyte ALD processes [54-58] are also investigated aiming at 3D all-solid-state lithium ion batteries[59], which has large advantages in energy density and safety compared to traditional liquid electrolyte based batteries.

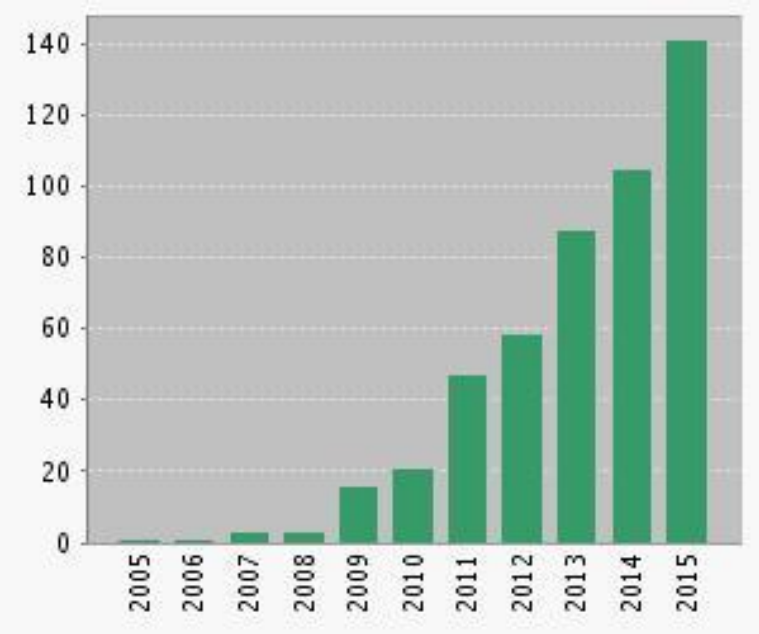


Figure 5 number of publications on ALD applications in battery, analyzed from the Web of Science

In this thesis, various ALD electrode materials with precise thickness control are employed to design fine-tuned battery nanostructures in a self-aligned full cell configuration and investigate the limiting factors for electron and ion transport in

nanoelectrodes with high packing density. ALD processes involved in this thesis for nanobattery fabrication are Ru and Pt as current collector, V_2O_5 as cathode material, TiO_2 and SnO_2 as anode materials.

2.2. AAO as templates for nanostructure synthesis

Porous anodic aluminum oxide (AAO) has high density of hexagonal self-aligned cylindrical pores (Figure 6). Pore diameter and pore distance are linearly proportional to the anodizing potential, described by

$$D_p = \lambda_p \cdot U \quad , \quad D_c = \lambda_c \cdot U$$

where D_p , D_c and U denote pore diameter, cell diameter (pore distance) and anodizing potential, respectively, with λ_p approximately 1.29 nmV^{-1} and λ_c around 2.5nmV^{-1}. The porosity (α) is defined by the project area of pores divided by the whole area, which can be expressed by following equations, with n denoting pore density ($1/cm^2$).

$$\alpha = \frac{\pi}{2\sqrt{3}} \cdot \left(\frac{D_p}{D_c}\right)^2 \quad \text{or} \quad \alpha = 10^{-14} n \cdot \pi \cdot \left(\frac{D_p}{2}\right)^2$$

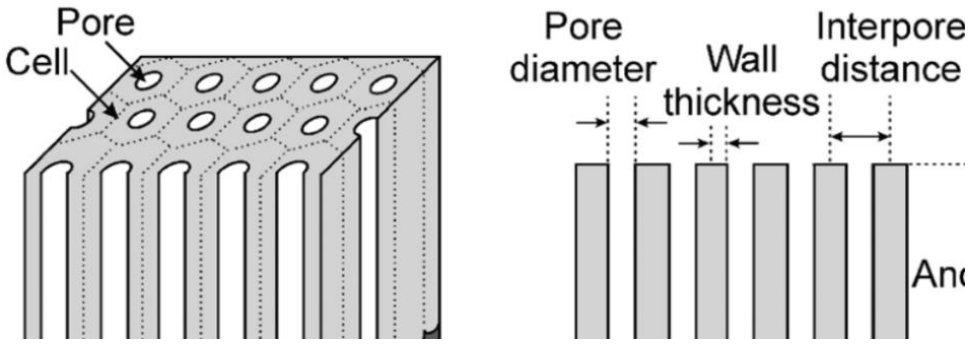


Figure 6 Schematic drawing of AAO self-aligned structure. Figure is adapted from Ref [60]

Such an extremely ordered, highly porous nanostructure offered by AAO has served as the template for the three dimensional (3D) nanobatteries, with wide applications in energy storage [61-63] and conversion [64-66] devices. Arranged in highly ordered hexagonal periodic structure, the nanopores of AAO have adjustable diameter and pore period via different anodization conditions, which offers a highly flexible and controllable platform as template for nanostructure Synthesis. The AAO templates used in this proposal are symmetric ones from Synkera with thickness of 50 μm, pore diameter of 150 nm and pore period of 250 nm, with porosity around 32%.

Chapter 3. Ultra small electrochemical storage platform

3.1. nanopore battery design

We designed a single nanotube structure that embeds all the components of an electrochemical storage device (illustrated schematically in Figure 7a) within the pores of a nanoscale template. Integrated current collectors (Ru metal) and active storage material (crystalline α-V_2O_5) were conformally coated at two ends of anodic aluminum oxide (AAO) nanotube arrays by atomic layer deposition (ALD). V_2O_5 at one end was prelithiated to serve as anode while pristine V_2O_5 at the other end served as cathode. After filling 1M $LiPF_6$ in EC: DEC (1:1) electrolyte into the AAO nanopores, we achieved parallel nanobattery arrays at areal density of 2×10^9 per square centimeter. Figure 7a illustrates the cross section of a single cell with 250 nm outer diameter and 50 μm length defined by AAO geometry. Integrated Ru coaxial current collector enables fast electron transport inside each electrode. Each V_2O_5 nanotube has 23nm wall thickness and 6 μm length, determined by ALD cycles (700 cycles x 0.33Å/cycle)[44] and scanning electron microscope (SEM) energy dispersive X-ray spectroscopy (EDX) (Figure 7b). This coaxial nanotube array architecture overcomes the challenge of fabricating full cells on a single substrate, using controlled-conformality ALD at the ends of AAO nanopores. The approach also takes advantage of the anode-cathode electrical isolation provided by the long AAO nanopores to achieve precise control over cell geometries and anode-cathode distances. AAO pores remain open after Ru and V_2O_5 ALD process for later electrolyte filtration. The resistance between two sides of AAO after Ru ALD is >20M Ohm, providing sufficient insulation, and the resistance across the 1cm wide device surface is about 150Ohm, offering good electrical contact for both electrodes. Figure 7c illustrates transmission electron

microscopy (TEM) images of a released Ru nanotube (300 ALD cycles) prepared from an AAO template (upper panel). It is approximately 15 μm long and 170nm in diameter. Insert is a magnified image of Ru nanotube. Lower panel shows selected area electron diffraction (SAED) indicating clear crystallinity of the Ru.

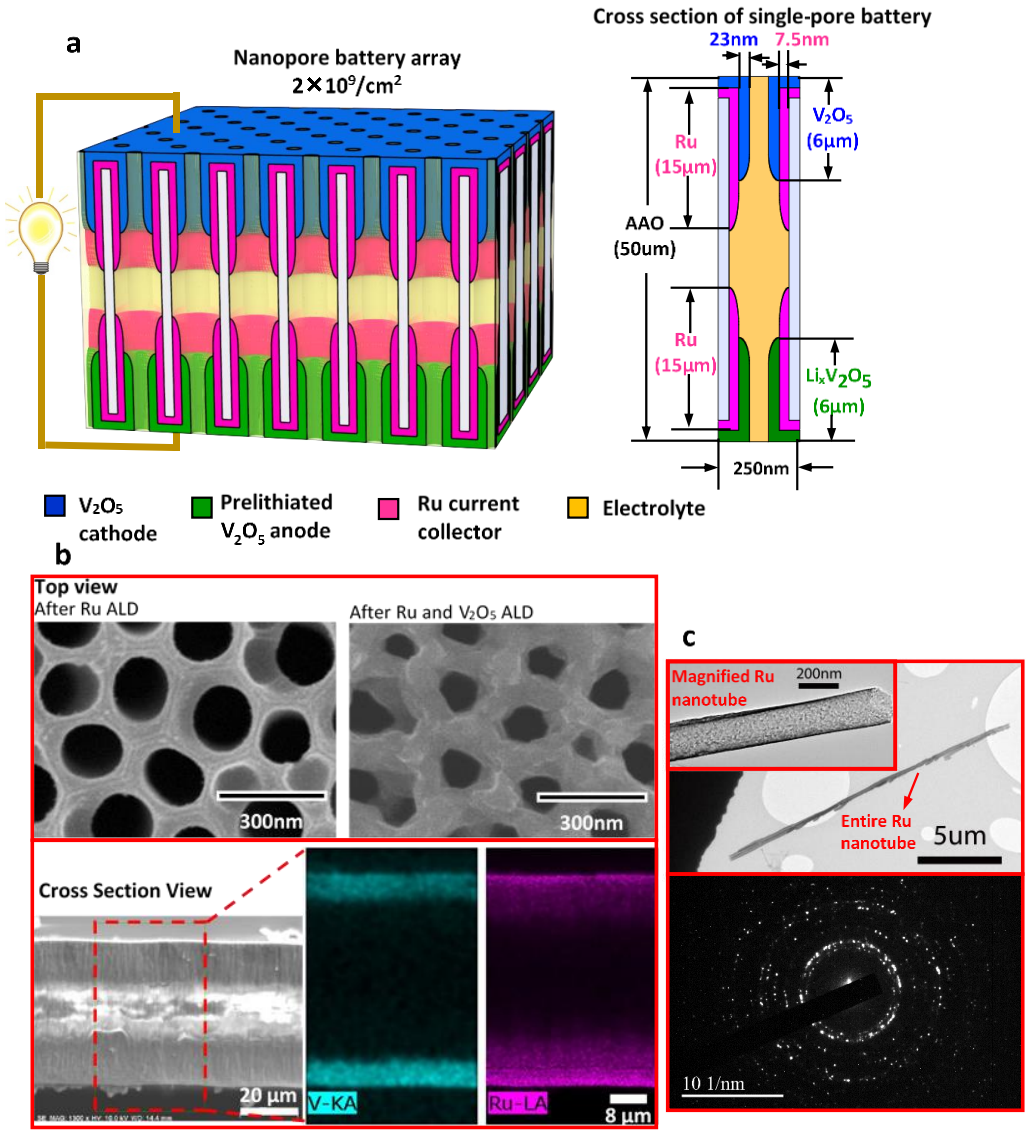


Figure 7 Nanopore battery design. (a) Schematic of parallel nanopore battery array and cross section of a single-pore battery. (b) SEM images of device top view indicate AAO pores remaining open after Ru and V_2O_5 ALD (upper panel).EDS mapping of device cross section demonstrates that Ru grows approximately 15 µm and V_2O_5 grows 6 µm into nanopores symmetrically (lower panel). (**c**) Transmission electron microscopy (TEM) image of a released Ru nanotube (300 ALD cycles) prepared from an AAO template (upper panel).

XRD spectrum further also confirms V_2O_5 to be orthorhombic phase (Figure 8a), with all the peaks matching with JSPDS No. 41-1426 expect for (001) peak. Such phenomenon can be explained by the preferential growth of V_2O_5 thin film along (001) direction. Considering AAO surface is perpendicular to XRD detection plane, (001) is suppressed. Figure 8a shows only two Ru peaks, which is due to the signal suppression from the V_2O_5 film, since the spectrum for AAO with only Ru displays full set of peaks (Figure 8b) and matches with previous reported results.

With anode and cathode precisely aligned in each single cell, this nanopore battery design avoids tortuosity and maximizes control over disparate length scales, providing optimum conditions for a high power device.

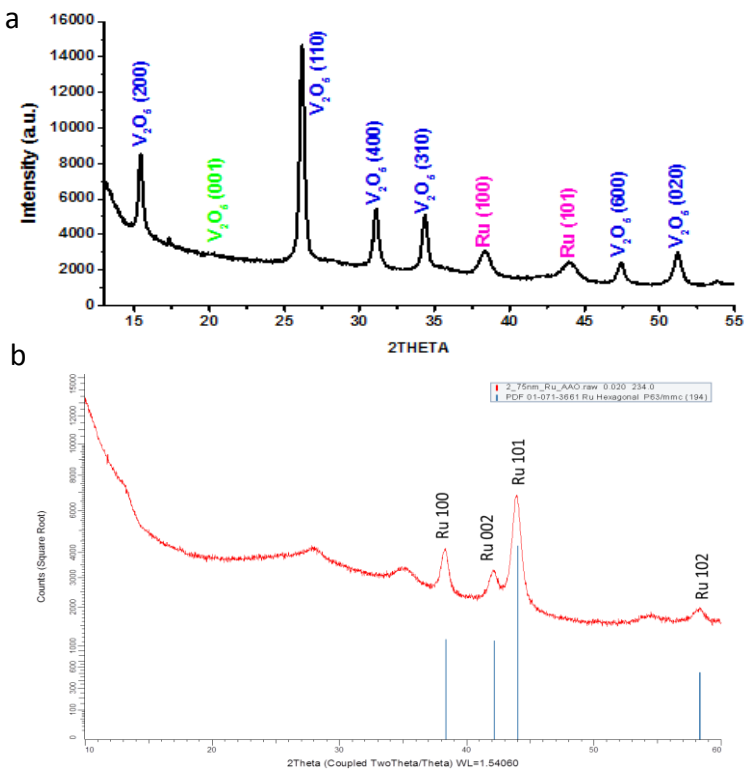


Figure 8 XRD spectrum of (a) a nanopore battery device, with 23nm V_2O_5 on top of 7.5nm Ru on an AAO substrate. And (b) 7.5nm Ru on AAO

3.2. Nanopore battery fabrication process flow and test setup.

The fabrication process of the nanopore battery array is illustrated in Figure 9. Symmetric AAO templates with thickness of 50 μm, pore diameter of 150 nm and pore period of 340 nm were purchased from Synkera. Here we choose Ru ALD process that is well established in our laboratory as current collectors, though a variety of other inexpensive conducting materials (including titanium nitride, tungsten[67, 68] and nickel[69]) are also available by ALD. Ru ALD using bis(2,6,6-trimethyl-cyclohexadienyl)ruthenium ($Ru(C_9H_{13})_2$, "Cyprus") and O_2 were carried out in a home-built viscous flow reactor furnace at 300 °C. The deposition rate was 0.5Å/cyc, yielding a 7.5nm film for a 150 cycle process with conductivity about 1.5×10^4 S cm^{-1}.The detailed

process parameters and Ru thin film conductivity were described in previous papers.[39, 70]

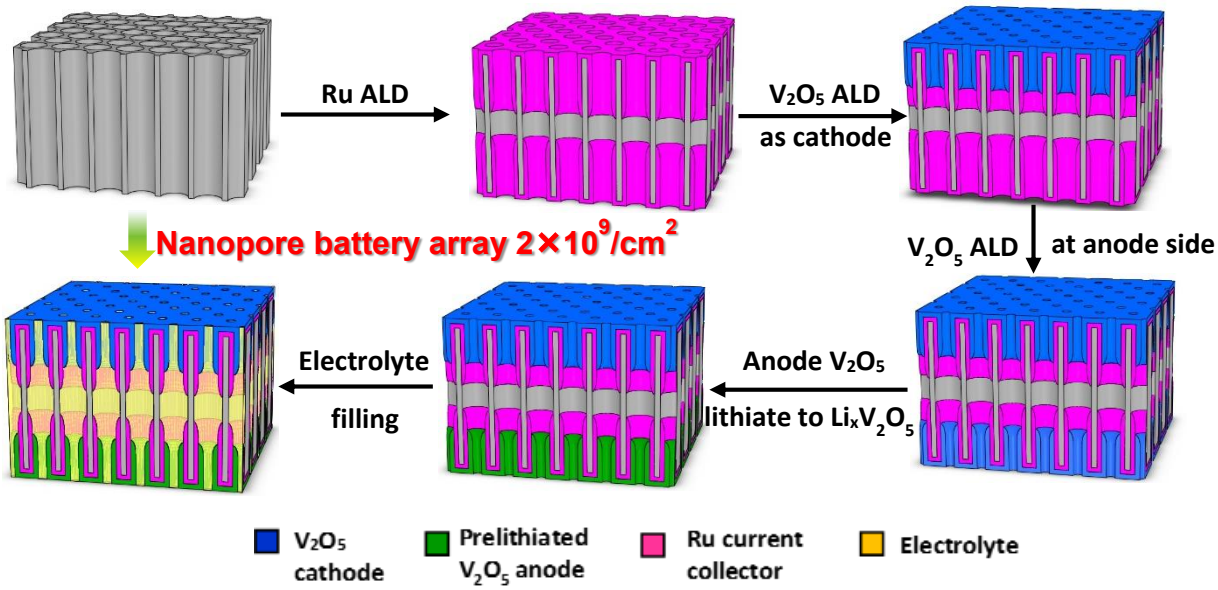


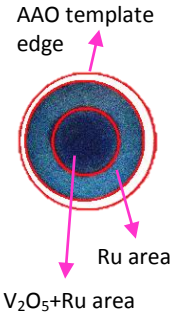
Figure 9 Fabrication process of nanopore battery.

During the Ru ALD process for a full cell, the AAO templates were pressed between two 1/2 inch nickel VCR face seal fitting gaskets with 0.44 inch inner diameter (0.95cm2 opening) from Swagelok, whose edges were then wrapped by aluminum foil and finally fixed by metal binder clips. The VCR gaskets served as contact masks to prevent Ru growth at the rim of AAO, which might cause shorting between anode side and cathode side. 5 sec pulse time of Cyprus was chosen to limit the Ru deposition depth to 15 μm into AAO pores, leaving 20 μm of bare AAO in the middle to act as a separator. Subsequently, crystalline V_2O_5 was deposited by ALD using vanadyl triisopropoxide (VO(OC3H7)3, VTOP) and ozone at 170°C in BENEQ TFS 500 reactor. Home-made contact masks with 6mm diameter opening controlled V_2O_5 growth into one side of Ru coated AAO pores with

deposition rate of 0.33Å per cycle to form nanotubes with 23nm wall thickness. V_2O_5 grew 6 µm deep into pores with 1s VTOP pulse time. Then the same procedure was repeated to grow V_2O_5 symmetrically at the other end of Ru coated AAO. The area of a full cell device is defined by the open area of contact mask (0.28 cm^2) and further measured by counting the pixel of V_2O_5 covered area (0.32cm^2) (Table 1). Commercially available templates can be purchased as large as 1200 cm^2 [71], suggesting that there is room for scaling up this design. For half-cell fabrication, a similar masking method is used with a VCR gasket sealing one side of the AAO against a solid plate during both Ru and V_2O_5 ALD process, resulting area of 0.95 cm^2.

Table 1Device Radius Measurement. The radii of AAO template, area coated with Ru and area coated with both Ru and V_2O_5 are measured by counting the pixels in inside each area. The radius of AAO template is known as 0.65cm

Features	Radius (pixel)	Actual Radius (cm)
AAO	286	0.65
Ru	251	0.57
V_2O_5+Ru	139.75	0.32



Afterwards, one side of V_2O_5 was electrochemically lithiated by discharging at 1C rate to different voltages (2.6V and 2.1V vs. Li metal). This prelithiated V_2O_5 was used as the anode of the full cell batteries. Both half cells and symmetric full cells are tested inside coin cells, the testing setup is illustrated in Figure 10. The prelithiation and full battery test are run inside glove box, without completely sealing the coin cells.

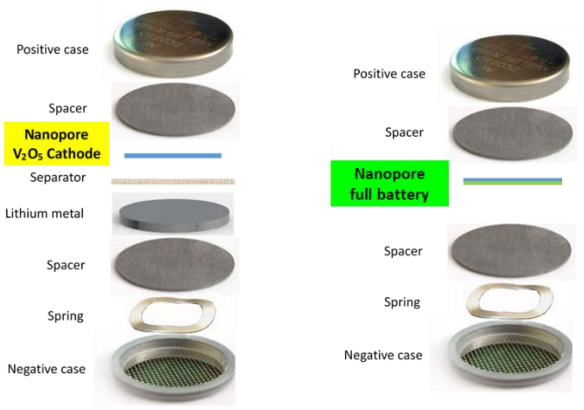


Figure 10 Coin cell setup for (a) half cell and (b) symmetric full cell testing.

In order to test the electron and ion transport, half cell, symmetric and asymmetric full cells are fabricated and tested. For clarity, the electrode materials for various cell configurations are summarized in Table 2. V_2O_5 is used as cathode material for all the configurations within one lithium ion insertion region. While for the anode side, lithium metal is used as both counter and reference electrode during half testing. In symmetric full cells, V_2O_5 also serves as anode, with one lithium ion insertion for a low voltage symmetric full cell and two lithium ion insertion for a high voltage symmetric full cell, which are also annotated as symmetric cycling and asymmetric cycling in the following text, respectively. TiO_2 and SnO_2 are used to compose asymmetric full cells to create larger full cell output voltage and to match with the high current density of V_2O_5 at high C-rate.

Table 2 Half cell and full cell test configurations.

Category	Half cell	Symmetric full cell		Asymmetric full cell	
Name/ annotation		Low voltage (Symmetric cycling)	High voltage (Asymmetric cycling)	V_2O_5-TiO_2 full cell	V_2O_5-SnO_2 full cell
Anode	Lithium metal	LiV_2O_5 (2.6~4V vs. Li)	$Li_2V_2O_5$ (2.6~2.1V vs. Li)	Anatase TiO_2 (1~2.5V vs. Li)	SnO_2 (0.5~2.6V vs. Li)
Cathode	V_2O_5 with 1 Li ion insertion (2.6~4V vs. Li)				

Chapter 4. Electron and ion transport in nanostructured electrodes (Half cell)

4.1. High power density enabled by nanostructured electrodes

Half cells were tested to investigate the electrochemical properties of the V_2O_5/Ru nanotube electrodes, demonstrating that their energy storage capacity arises mainly from the active V_2O_5, while the Ru nanotube current collectors provide high electrical conductivity. The cyclability and capacity retention at high rate of our 'all-in-one' array battery[2] compare favorably against other reported cathode configurations using nanostructured V_2O_5.[72, 73]

We observed high specific capacity of 157 mAh/g for one Li ion insertion (Figure 11a), which is indicated by phase changing plateaus at 3.4V and 3.2V (vs. Li/Li^+)[74]. Plateaus at 3.4V and 3.2V correspond to phase transformation from α-V_2O_5 to ε-V_2O_5 ($V_2O_5 + 0.5Li^+ + 0.5e^- \leftrightarrow Li_{0.5}V_2O_5$) and ε-V_2O_5 to δ-V_2O_5 ($Li_{0.5}V_2O_5 + 0.5Li^+ + 0.5e^- \leftrightarrow LiV_2O_5$), respectively. Cyclic voltammograms (CVs) of V_2O_5 in the potential range of 2.6−4 V (vs Li/Li^+) (Figure 11b) further demonstrate the Li ion insertion mechanism, which occurs in two sequential stages denoted by two sets of well-resolved peaks. A fraction of V^{5+} ions are reduced to V^{4+} ions at the first reduction peak (~3.4 V) while the remaining V^{5+} ions are reduced to V^{4+} at the second peak (~3.2 V). [74] The reverse reactions lead to the two corresponding oxidation peaks in the reverse scan. The pair of redox peaks look symmetric and all the peak potentials shift less than 30 mV in this scan range, which implies quite reversible Li insertion reaction.

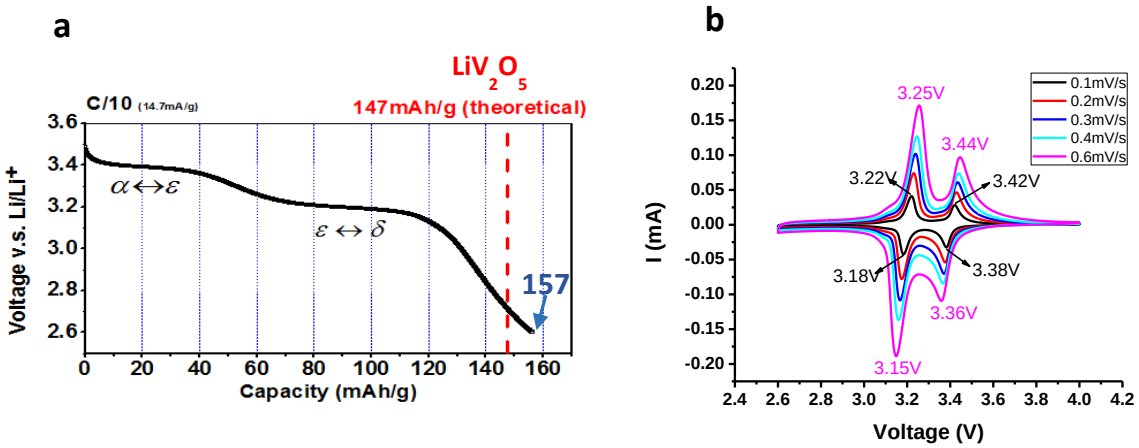


Figure 11 Electrochemical charge-discharge of a V_2O_5/Ru nanotube half cell device. (a) Galvanostatic Li ion insertion at C/10 rate with one Li ion insertion at 1st cycle. [74] (b) Cyclic voltammogram of V_2O_5/Ru nanotube cathode at different scan rates implies reversible Li^+ insertion reaction.

The V_2O_5 cathode with integrated Ru nanotube current collector displays high capacity at high charge-discharge rates. Its specific capacity has been measured to be 157mAh/g at 1C, over 147mAh/g at 5C and 83 mAh/g (53% of its original capacity at 1C rate) at 150C (24s charging time) (Figure 12a). Interestingly, excess capacity somewhat beyond theoretical (147 mAh/g for one Li insertion reaction per V_2O_5 formula unit) was observed at 1C rate and lower. The excess capacity could be associated with the electrical double layer capacity due to large surface area [75] and/or additional redox activity of possible RuO_2 formed on Ru surface caused by O_3 exposure during the V_2O_5 ALD process. Experiments using Ru/surface RuO_2 electrodes to simulate any such redox activity showed such contribute to be small (Figure 12a).

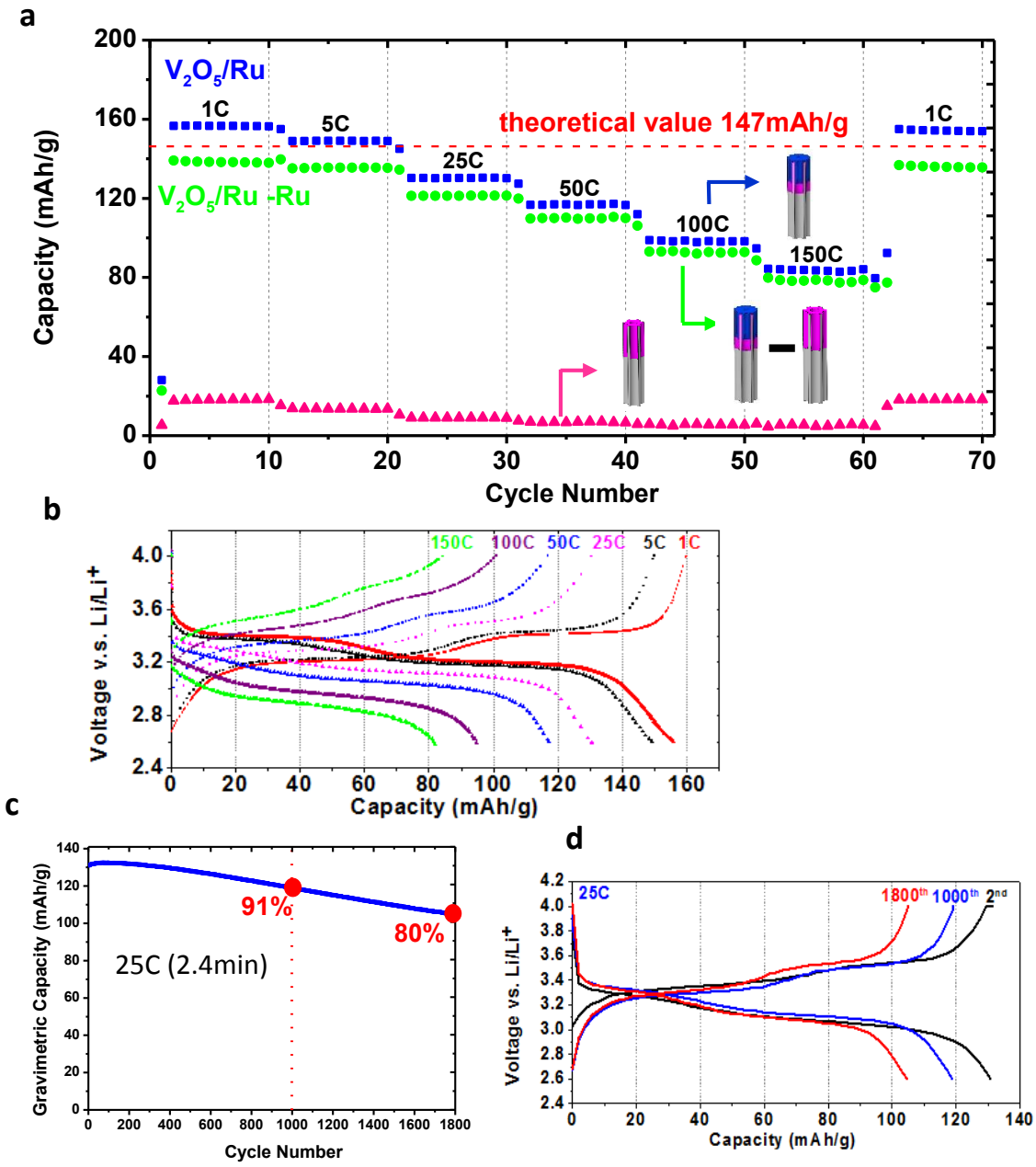


Figure 12, Electrochemical charge-discharge of a half cell device at high rate cycle life. (a) Rate performance of V_2O_5 /Ru nanotube battery (blue), O_3 treated Ru current collector (pink) and pure contribution of V_2O_5 (green). Inserted cartoon icons represent the configuration of each case. (b) Galvanostatic charge-discharge cycling curves of V_2O_5 /Ru nanotube cathode at various C-rates. (c) V_2O_5 /Ru nanotube cathode has 91% of the original capacity after 1000 cycles and 80% after 1800 cycles when cycled at 25C. (d) Charge/discharge curves at 2nd, 1000th, and 1800th cycle.

The plateaus in galvanostatic charge/discharge cycling curves (Figure 12b) clearly show the existence of a Faradaic Li ion insertion processes from 1C to 150C rate. This coaxial V_2O_5/Ru nanotube structure also demonstrates exceptional charge-discharge cycle life. When cycling at 25C, V_2O_5 /Ru coaxial nanotube cathode has 91% of the original capacity after 1000 cycles and 80% after 1800 cycles. (Figure 12c) The charge/discharge curves at 2nd, 1000th, and 1800th cycle plotted in Figure 12d elucidate steady phase transition plateau positions during the cycling, which indicates stable voltage output during long reversible battery cycling life.

To further investigate the contribution of the Ru nanotube current collectors from which electrons can transfer very easily from Ru to V_2O_5 layer in the coaxial nanotube structure, a planar structure of current collector was tested as a control. We designed the control device with 6μm deep V_2O_5 but only sputtered Au as planar current collector (Figure 13a) (instead of the nanotubular Ru). In this structure, the transport path length of electrons from Ru through V_2O_5 is nearly 6 μm in order to access the bottom end of V_2O_5 nanotube, which is up to 260X longer than the electron path length (23nm) in the V_2O_5/Ru coaxial nanotube structure (Figure 13b). In this case a potential gradient can develop along the V_2O_5 nanotube during charge-discharge cycle, leading to inhomogeneous current distribution along the length of the V_2O_5 nanotube which will be especially detrimental at high cycling rates. This hypothesis is confirmed by our COMSOL simulations (Figure 13c and d), which monitor the potential evolution at 3 different points along a V_2O_5 nanotube discharged at 25C. The simulations reveal that the further the point is from current collector, the faster the voltage of V_2O_5 drops in the planar current collector configuration. This inhomogeneous discharging profile results in lower capacity than a V_2O_5 nanotube

with the integrated Ru nanotube current collector, which has uniform potential profile along the V_2O_5 nanotube at 25C.

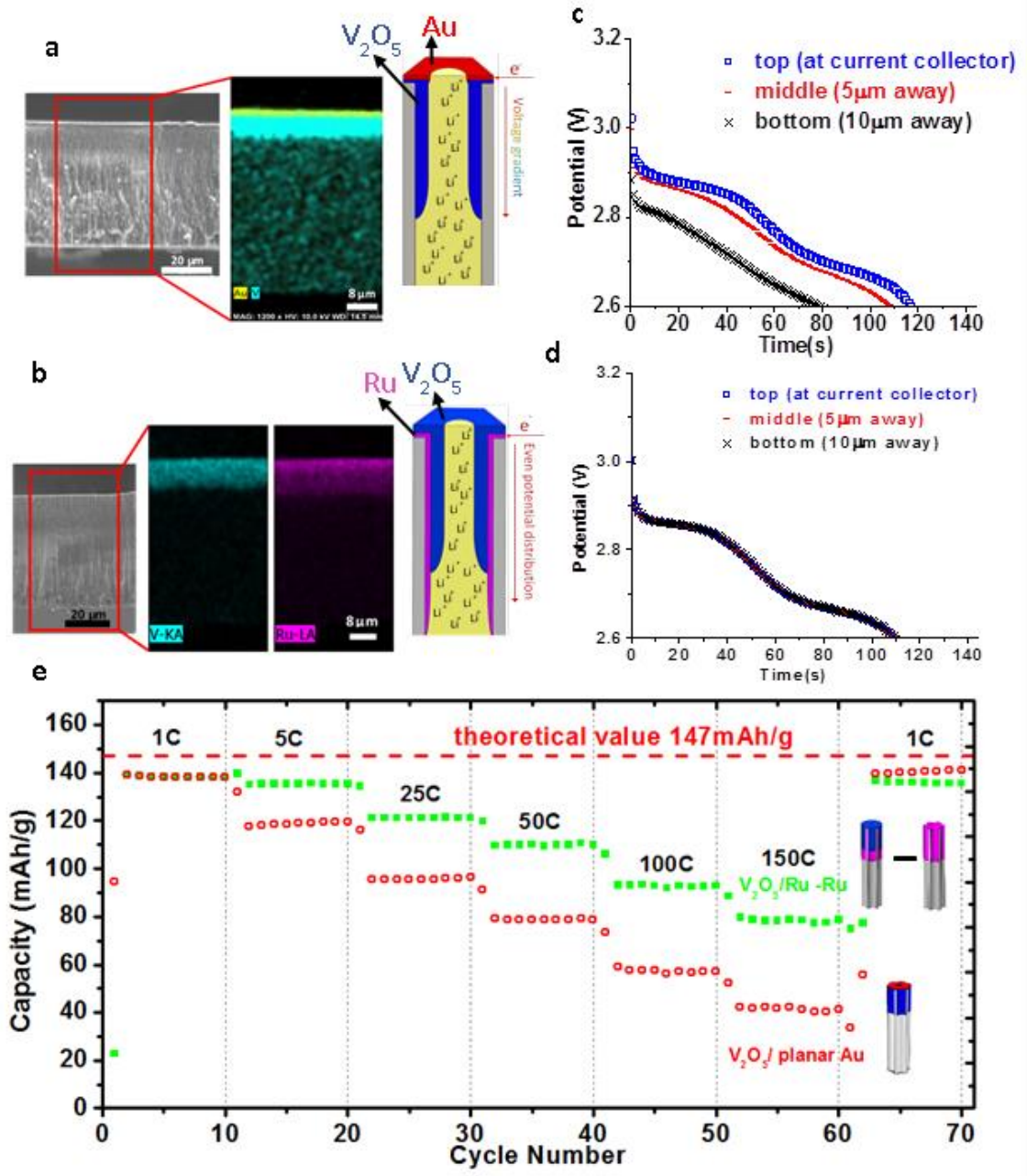


Figure 13 Rate performance of V_2O_5 nanotube half cell with planar Au vs. Ru nanotube current collectors. (a) and (b) SEM EDS mappings and schematic diagrams of cathode cross section with Au planar current collector and Ru nanotube current collector. (c) and (d) COMSOL simulation of potential evolution at 3 different points (at current collector, 5 μm away and 10 μm away)

along V_2O_5 nanotube discharged at 25C with planar and nanotube current collector, respectively (e) Rate performance up to 150C of V_2O_5/Ru nanotube cathode (with Ru capacity portion subtracted) (green cubes) and V_2O_5/planar Au (red circles). Cartoon icons represent the configuration of each case.

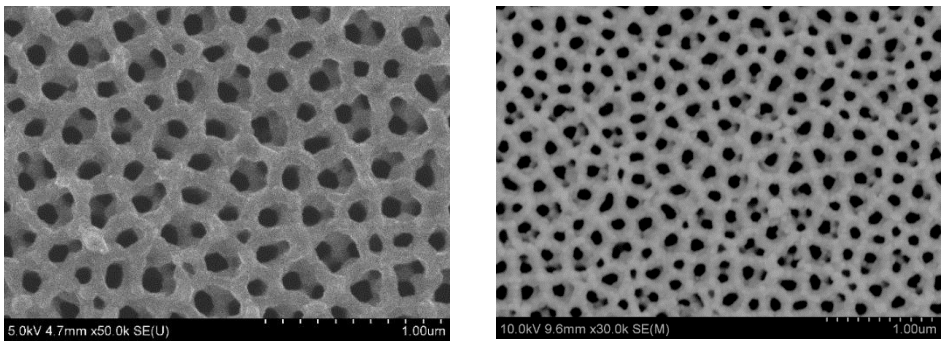


Figure 14 Top view for Nanotube Ru Current Collector vs Planar Au one. AAO pores remain open after current collector and vanadium oxide deposition for later electrolyte infiltration.

4.2. Deconvolution of surface reaction and ion insertion

The much higher capacity of the V_2O_5/Ru nanotube configuration than V_2O_5/planar Au at high rate (Figure 13e) underscores the importance of integrated current collector components in nanostructured electrodes for electron communication to/from the ion storage material. Furthermore, the high surface area and thin nature of the nanotube structure improves ion access and transport to/from the electrolyte to fully utilize the electrode material. While the distinct peaks in the CVs and plateaus in the galvanostatic discharge curves clearly show the characteristics of a lithium insertion reaction, the high capacity remained at high rate motivates further investigation into the kinetics of the devices.

The CVs can be used to probe the kinetics of the overall reaction, and quantify the contribution of fast, surface-dominant reactions as well as slower, diffusion insertion-dominant reactions to the total charge stored. Generally, the surface-dominant reaction

charge includes the electrical double layer and contribution from fast faradaic reactions on the exposed electrode surface. The insertion-dominant charge is generally the contribution from bulk Li insertion. These two contributions can be distinguished by their kinetics. Typically the slower insertion-dominant reaction current scales linearly to the square root of the scan rate ($\upsilon^{1/2}$), unlike surface-dominant reaction current, which scales linearly to the scan rate (υ). Because of this difference in scan rate dependence, the two contributions can be separated mathematically.

There are two methods commonly used in the literature to deconvolute surface and bulk charge in energy storage electrodes using cyclic voltammetry. Both methods rely on the fundamental concept that the surface and bulk of a material are governed by different kinetics, and will respond differently to increasing scan rates. However, each method takes a different mathematical approach to differentiate between the two. Trasatti's method[76] estimates the charge at a theoretical scan rate of 0, which corresponds to the maximum total charge possible at an infinitely slow scan rate, by plotting (1/Q) vs. the square root of the scan rate. The y-intercept of the linear region of the plot is $1/Q_{total}$.

$$\frac{1}{Q(\upsilon)} = k_2\sqrt{\upsilon} + const1$$

Then, to extract the surface charge, the charge is extrapolated to an infinitely fast scan rate by plotting charge vs. $v^{-1/2}$. The y-intercept is the surface charge, corresponding to a scan rate of infinity where it is assumed all bulk contributions are eliminated.

$$Q(\upsilon) = k\left(\frac{1}{\sqrt{\upsilon}}\right) + const2$$

The second method of deconvoluting surface and bulk charge has been described in detail in the literature by Dunn and coworkers [77]. This method deconvolutes the surface and bulk contributions to current at a given voltage, i(V), based on the following equation:

$$i(V) = k_1 v + k_2 v^{1/2}$$

When rearranged, this equation can be plotted with $i/v^{1/2}$ as a function of $v^{1/2}$, providing k1 and k2 as the slope and intercept respectively.

$$\frac{i(V)}{v^{1/2}} = k_1 v^{1/2} + k_2$$

Determining this ratio for a given number of points during each sweep of the CV can deconvolute the surface reaction and bulk insertion. Such method suits for reactions with little peak shifting, while the peak shift in CV curves for V_2O_5 is so high, especially at high scan rate, that Dunn's method does not provide a reliable quantification of the surface vs. insertion charge. Therefore, Trasatti's method[76] is used to distinguish the contribution from fast, surface-dominant (proportional to scan rate υ) and slower, diffusion insertion-dominant reactions (proportional to $\upsilon^{1/2}$) in the following.

<u>V_2O_5 with 3d Ru current collector</u>

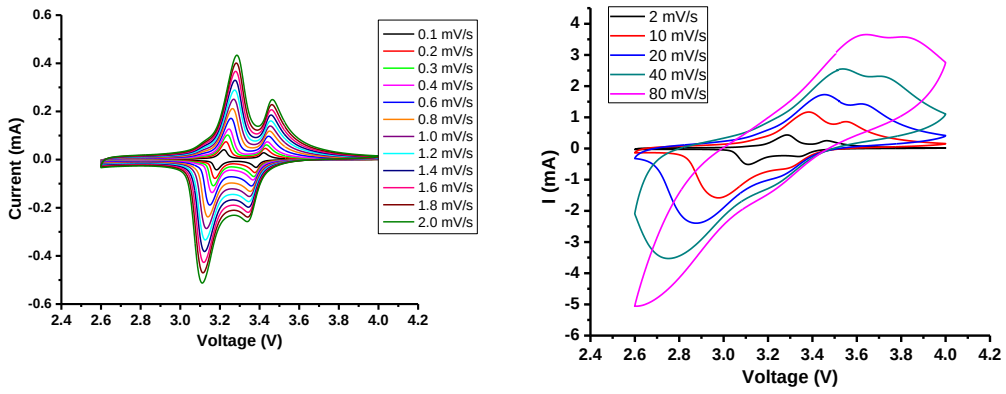


Figure 15. CV of V_2O_5 with Ru nanotube current collectors at different scan rate cycled inside a coin cell against Lithium metal. (Left panel: 0.1mV/s-2.0mV/s, right panel: 2mV/s-80mV/s). The CV curves show obvious ion insertion peaks up to 80mV/s.

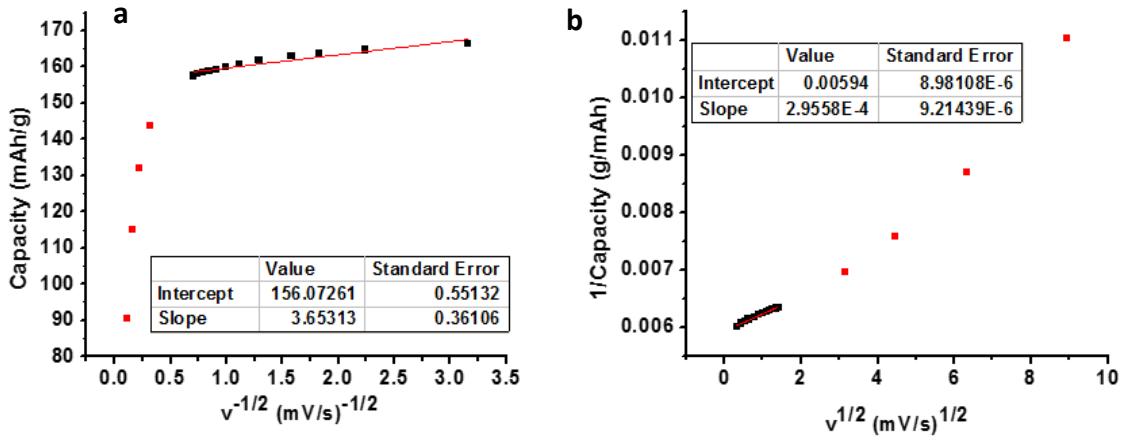


Figure 16. Trasatti's method for V_2O_5 with Ru nanotube current collectors. (a) Gravimetric capacity versus inverse square root of scan rate for V_2O_5/Ru nanotube arrays. The Intercept value represents the charge proportional to scan rate (v), which is 156.1 mAh/g. (b) Inverse gravimetric capacity versus square root of scan rate for V_2O_5/Ru nanotube arrays. The inverse of the intercept value is the total charge (168.4 mAh/g).

<u>V_2O_5 with planar Au current collector</u>

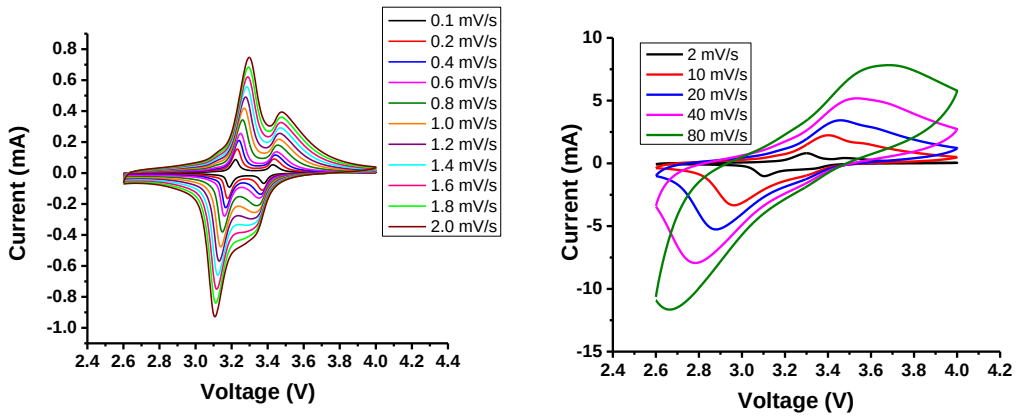


Figure 17. CV of V_2O_5 with planar Au current collectors at different scan rate cycled inside a coin cell against Lithium metal (Left panel: 0.1mV/s-2.0mV/s, right panel:2.0mV/s-80mV/s). The absolute current values are larger than the ones of V_2O_5/Ru nanotube, which results from the larger total mass of V_2O_5 in V_2O_5/planar Au cathode. However, its current normalized by V_2O_5 mass is smaller than that of V_2O_5/Ru nanotube. The two sets of peaks at ~3.2V and ~3.4V, corresponding to lithium ion insertion, merge together and can't be distinguished when scan rate is larger than 10 mV/s.

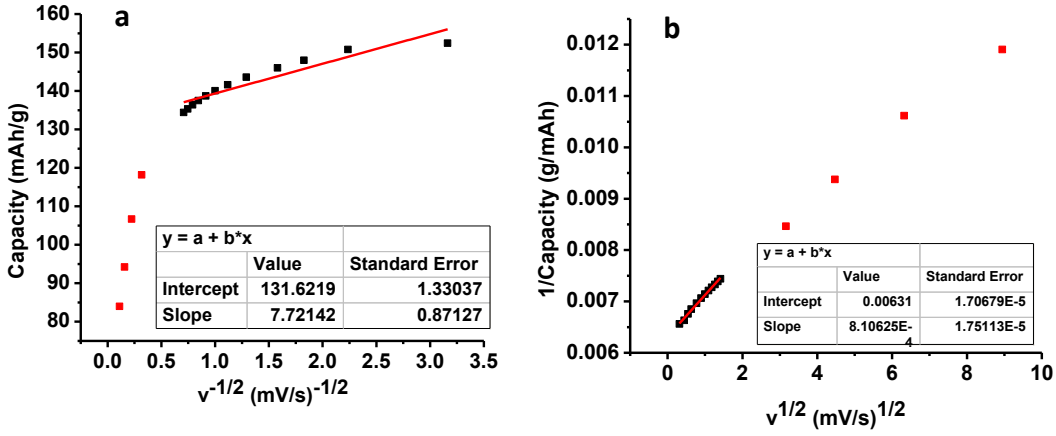


Figure 18. Trasatti's method for V_2O_5/Au cathodes. (a) Gravimetric capacity versus inverse square root of scan rate. The Intercept value represents the charge proportional to scan rate (v), which is 131.6 mAh/g. (b) Inverse gravimetric capacity versus square root of scan rate. The inverse of the intercept value is the total charge 158.5 mAh/g.

The υ-dependent surface-dominant reaction charge for the V_2O_5/Ru nanotube half cell is predicted to be 93.3% of the total charge, which is 10 percent more than that of V_2O_5/planar-Au counterpart (83%) (Figure 19a). Very importantly, the CVs of V_2O_5/Ru nanotube electrodes imply that most of these reaction charges are due to faradaic reaction process as they show characteristic oxidation and reduction reaction peaks at scan rates up to 80mV/s and much higher current values than that of the Ru nanotube control sample without V_2O_5, which shows only electrical double layer capacity. (Figure 19b) This suggests that most of Li-ion inserting-faradaic reactions of V_2O_5 nanotubes are taking place quickly enough to be indistinguishable from fast surface-dominant reactions. In conclusion, these structures have an active material thickness that is optimized to maximize power density by utilizing the available material so quickly that the kinetics of this insertion reaction are nearly indistinguishable from fast double layer charging behavior. In an important sense, this realizes the value nanostructuring offers for high power from high energy density storage materials.

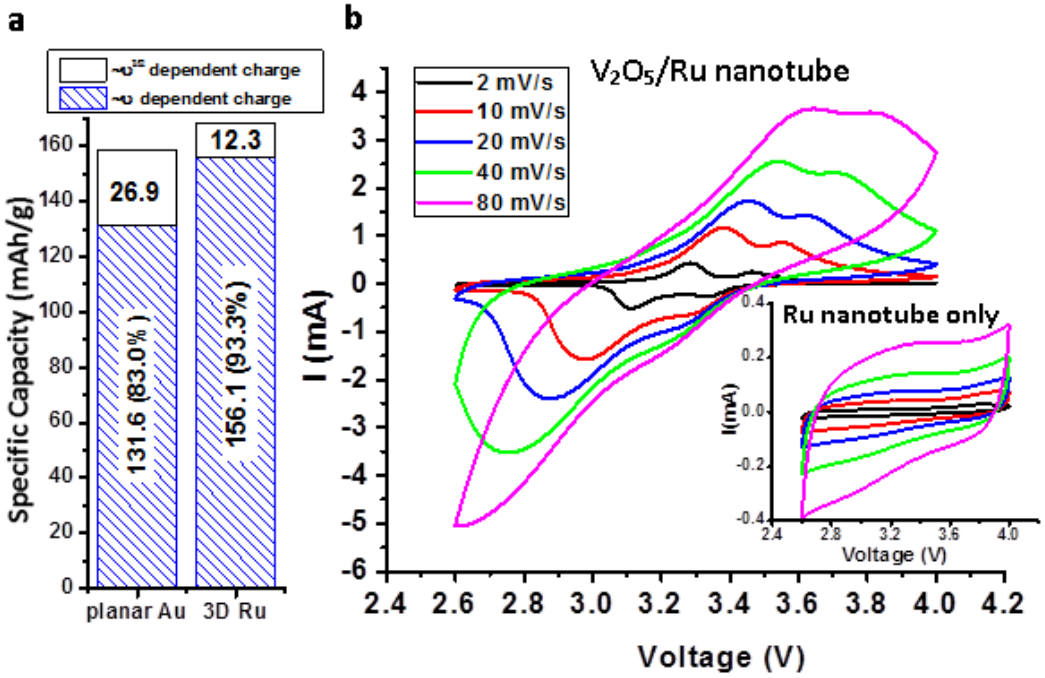


Figure 19 Deconvolution of charge contributions from cyclic voltammograms reveals fast lithium ion insertion. (a) Trasatti's method of deconvoluting charge storage contributions as a function of scan rates indicates that the Ru nanotube collectors facilitate fast electrochemical reaction, resulting in both higher overall capacity and a higher contribution from the υ-dependent charge, which includes the contribution of the electrical double layer and all fast Faradaic reactions which are not diffusion limited. (b) CV of V_2O_5/Ru nanotubes shows characteristic oxidation and reduction reaction peaks with scan rate up to 80mV/s. Insert shows CVs of Ru nanotubes cycled at the same scan rate, clearly showing only double layer charging, without any of the characteristic redox peaks.

Chapter 5. Ion transport through confined nanochannels (Symmetric full cell)

5.1. Demonstration of a symmetric full cell device

A full cell device can demonstrate the potential of this architecture to translate the half cell performance into usable, complete devices which do not sacrifice the high rate performance characteristics measured in the half cells. Figure 20 summarizes the electrochemical performance of a symmetrical full cell device, which has 106 μg V_2O_5 as cathode and 131 μg V_2O_5 as anode. The anode V_2O_5 was pre-lithiated at 1C current to 2.6V vs. Li/Li^+ with one Li ion insertion. Then the cell was cycled within a symmetric voltage window, between-1V and 1V. During the cycling process, cathode and anode switch between LiV_2O_5 and V_2O_5 in turn (Figure 20a).

Figure 20b displays CV of the full cell device at scan rate of 0.5mV/s, with two reduction peaks at -0.03 and -0.25V, and their corresponding oxidation peaks at 0.25V and 0.04 in the reverse scan, respectively. The difference between the reduction and oxidation peaks are 0.28V and 0.29V for the two characteristic reaction peaks. While naturally slightly larger than the half cell peak separation (0.2V), the full cell still shows good reversibility. The C rate and specific capacity were normalized by the weight of V_2O_5 cathode. The nanopore battery full cell has capacity of 150mAh/g at 1C and 70mAh/g at 150C (Figure 20c), which is consistent with the half-cell performance in terms of capacity retained at high rate. Interestingly, this seems to indicate that the confined electrolyte space is not a severely limiting factor in these devices. Additionally, 87.8% of original capacity remains after 1000 cycles at 25C rate with current density of $0.26mA/cm^2$ (Figure 20d).

Compared to a nanowire array full battery device inside AAO reported previously[8] , this nanopore battery triples capacity, with hundreds times longer cycle life even at much higher power density (8X current density). We attribute the superior lifetime to the conformal coaxial tubular structure enabled by ALD which reduces inhomogeneous charging at irregular sharp edges of electrodes[78-80] and provides reliable mechanical strength during the cycling[81]. Additionally, good crystallinity of V_2O_5 increases reversibility during lithiation and delithiation.[44]

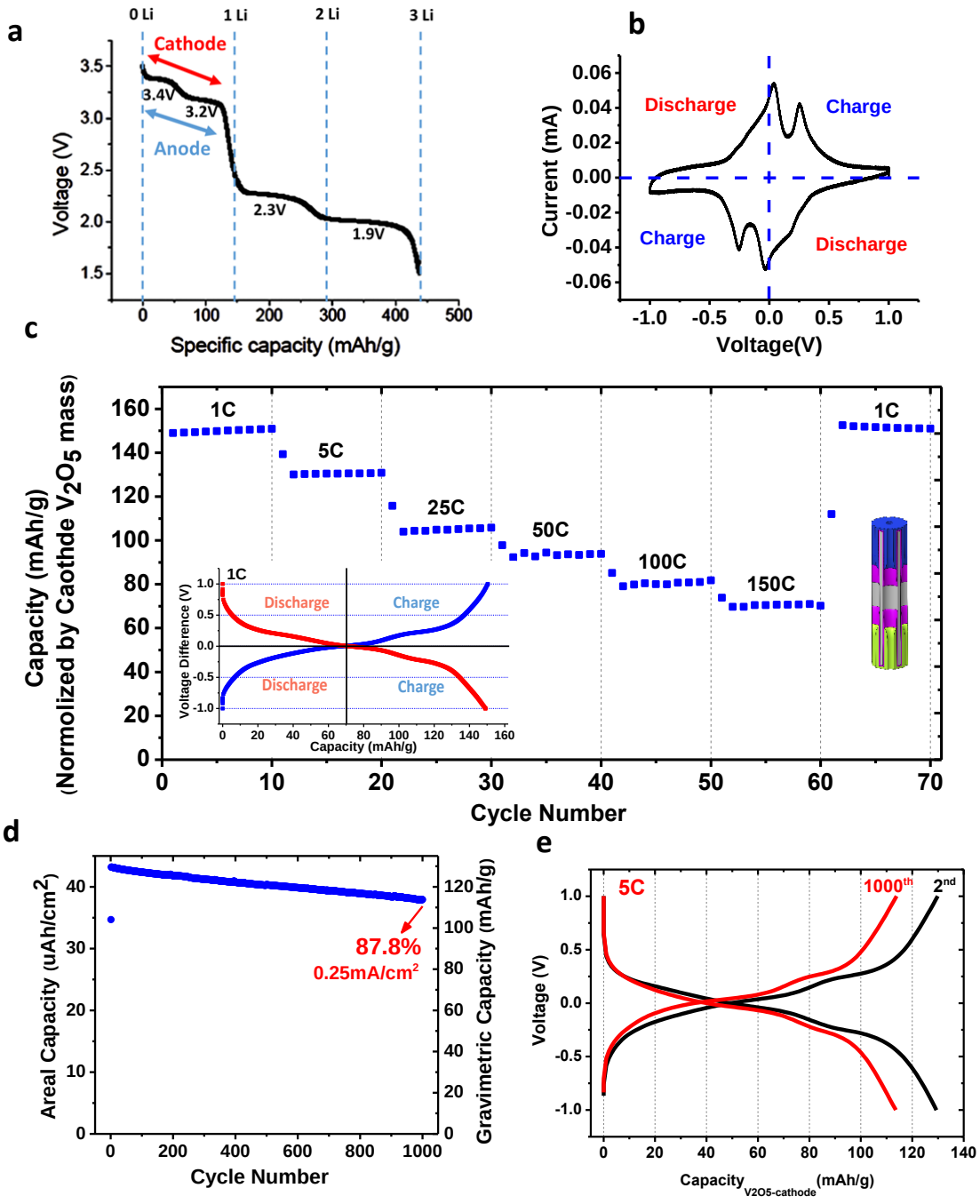


Figure 20. Symmetrically cycled full cell with voltage window form -1V to 1V. (a) Schematic diagram of cathode and anode voltage range. They are both in one Li ion insertion regime (4.0V to 2.6V). Phase transition plateau voltages are marked under the discharge curve. (b) Cyclic Voltammogram at 0.5mV/s scan rate. (c) Rate performance (Capacity normalized by cathode V_2O_5 mass). Insert shows charge and discharge curve at 1C. (d) Long cycle life with high current density. (e) Charge and discharge curves at 2nd and 1000th cycle.

5.2. Increase full cell voltage by asymmetric cycling

Increasing cell voltage is a possible method to improve energy and power density. A full cell device with voltage window from 0.2V to 1.8V was demonstrated by cycling the cathode between V_2O_5 and LiV_2O_5 and anode between $Li_2V_2O_5$ and LiV_2O_5 (Figure Figure 21a). In this situation, mass loading at cathode side was half that at anode side in order to compensate for possible faster capacity fade rate of the anode than of the cathode. Specific capacity normalized by the mass of anode is comparable to that of the half cell, with 178mAh/g at 1C rate and 82mAh/g at 150C (Figure Figure 21c). The CV curve at a scan rate of 1.2mV/s (Figure Figure 21b) displays two characteristic reduction peaks for phase transitions during one Li ion insertion at 0.88 and 0.51V, and their corresponding oxidation peaks at 1.13 and 0.76V. Redox peaks and oxidation peaks separations are both 0.37V, nevertheless this full cell with voltage window from 0.2V to 1.8V still displays excellent reversibility and cycling performance with 81.3% capacity remaining after 1000 cycles (Figure Figure 21d).

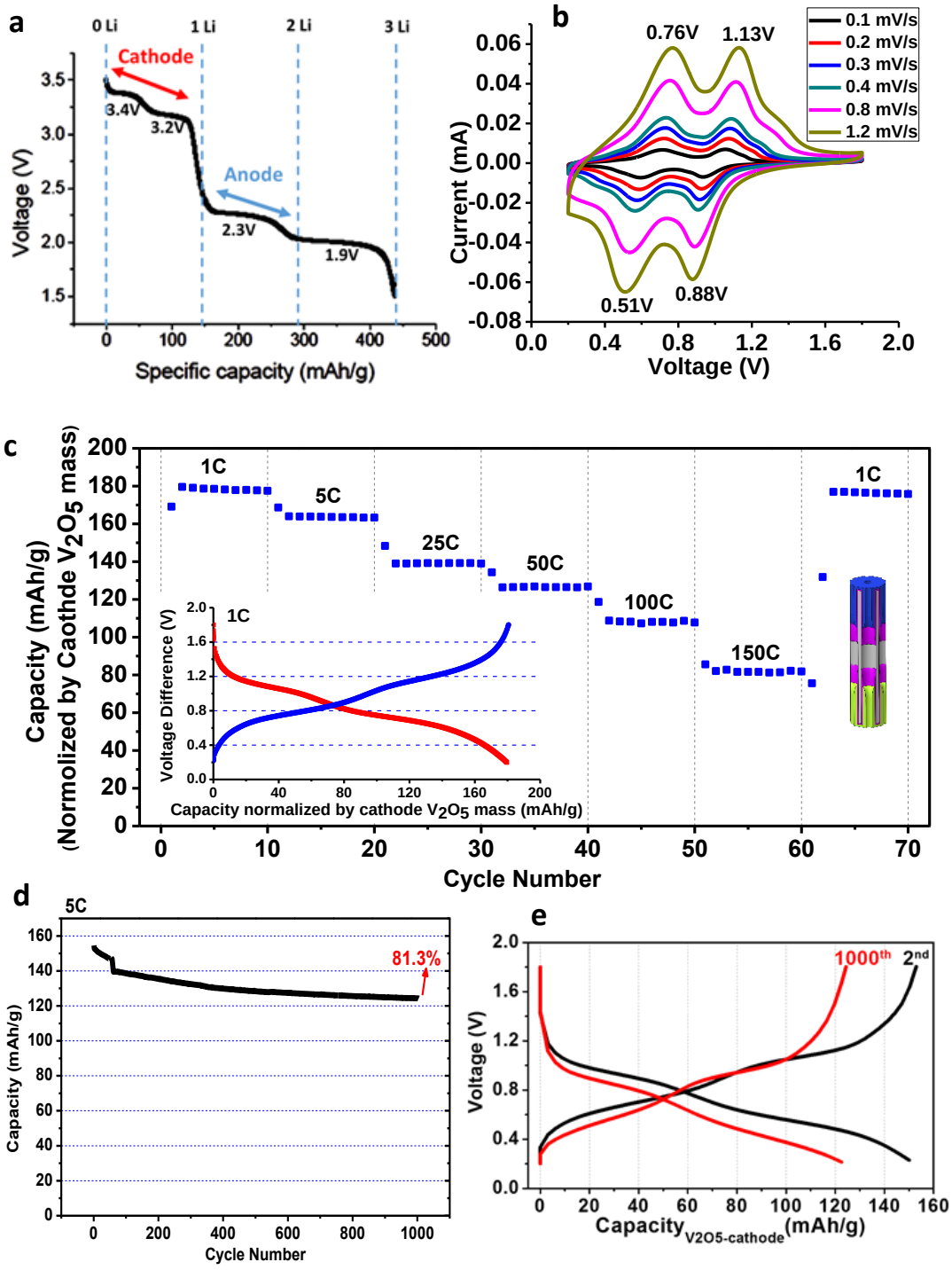


Figure 21. Asymmetrically cycling between 0.2V and 1.8V. (a) Schematic diagram of cathode and anode voltage range. Cathode is cycled in one Li ion insertion regime (4.0V-2.6V), while anode is cycled in two Li ion insertion regime (2.6V-2.1V) providing higher output potential than a symmetric cell in Figure 20. Phase transition plateau voltages are marked under the discharge

curve. (b) Cyclic Voltammogram at different scan rates. (c) Rate performance (Capacity normalized by cathode V_2O_5 mass). Insert shows charge and discharge curves at 1C. (d) Cycling performance at 5C. (e) charge and discharge curves at 2nd and 1000th cycle.

5.3. Ion diffusion through nanochannels

Highly confined electrolyte environments are inevitable if electrodes are densely packed to take advantage of nanostructuring for high power devices. In such situation, it is possible that a substantial depletion of lithium ions may occur in the nanoconfined electrolyte region near the electrode, especially when the device is operated at high power. The nanopore battery provides an extreme scenario for nanostructured Li ion batteries, where Li ions have to shuttle back and forth through narrow, high aspect ratio AAO channels between the coaxial anode and cathode during battery charging and discharging. The structure also has the advantage of tunable geometry and material variation to investigate ion transport inside extremely confined environment at high power. This "ionics" phenomena may become vital if nanostructures are assembled close enough so that their behavior are different from what they would have when isolated. Actually, the tradeoff between using nanostructured electrode and designing dense architectures may reveal new scientific issues involving ion transport at the nanoscale, reflecting design and performance challenges at the mesoscale [82, 83].

The nanopore full cells are tested under both symmetric and asymmetric cycling voltage window with Li ions shuttling back and forth between cathode side and anode side through AAO nanochannels. When both of the cathode and anode are cycled within one Li ion insertion regime (Figure 22a), a V_2O_5 cathode - LiV_2O_5 anode full cell is symmetrically cycled between -1V and 1V. While a V_2O_5 cathode - $Li_2V_2O_5$ anode full cell offers an asymmetric output potential range from 0.2V to 1.8V if cathode is cycled in one Li ion

insertion regime and anode is cycled in two Li ion insertion regime providing higher output potential than a symmetric full cell (Figure 22b). Figure 22d compares capacity retention of full cells (both symmetrically and asymmetrically cycled) to a half cell at various C-rates. They show similar trends in capacity retention, which implies that the present nanopore battery geometry does not impose serious constraints such as an ion depletion situation.

With regard to electrochemical performance, the asymmetrically cycled full cell with voltage window from 0.2V to 1.8V displays excellent reversibility and cycling performance with 81.3% capacity remaining after 1000 cycles (Figure 22e) , which has almost 3X capacity and more than 100X longer cycle life when cycled under 4X current density compared to the published nanobattery.[8]

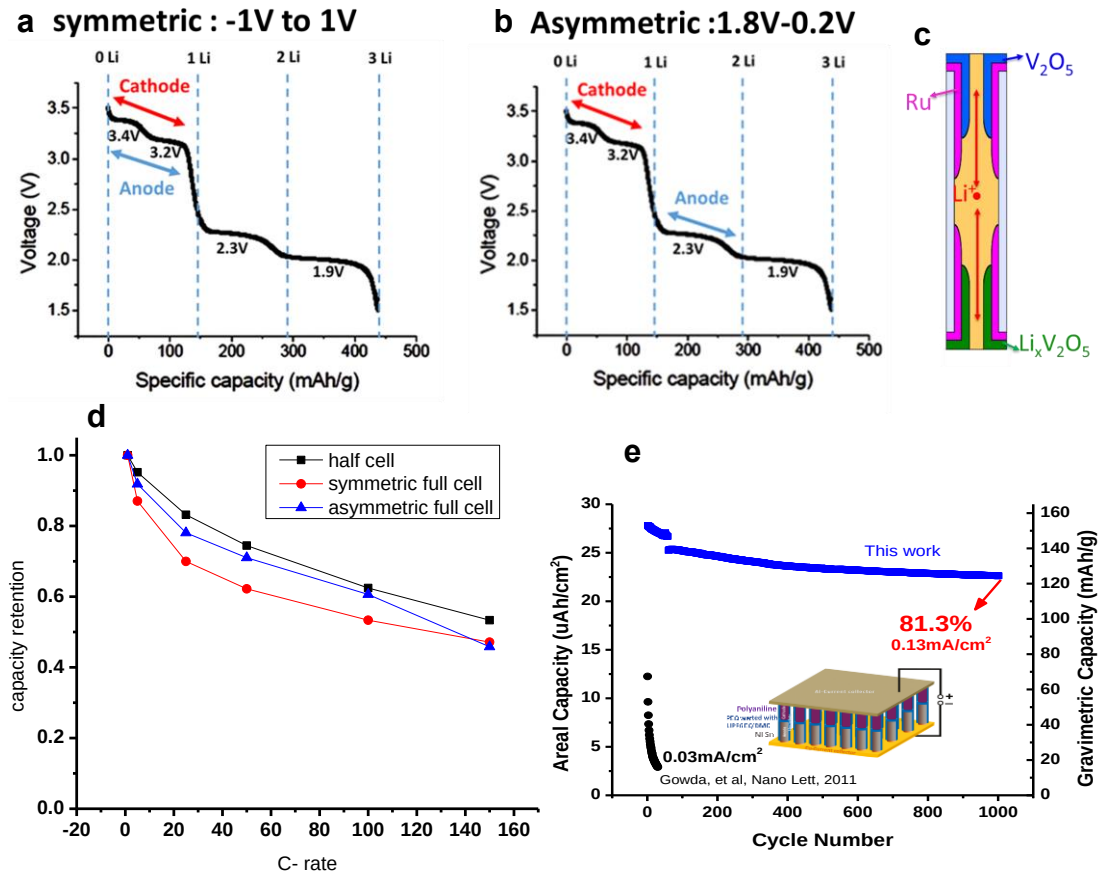


Figure 22 Full battery cycled inside confined nanotube environment. (a) Schematic diagram of cathode and anode voltage range in symmetric cycling configuration. (b) Schematic diagram of cathode and anode voltage range while the battery is under asymmetrically charging/discharging.. (c) Schematic of a single-pore battery cross section with Li ion shuttling back and forth between cathode side and anode side. (d) Normalized capacity retention from 1C to 150C of a V_2O_5 /Ru nanotube vs Li metal half cell (black square), a symmetrically cycled full cell (red cycle) and an asymmetrically cycled full cell (blue triangle). (e) Cycling performance of asymmetrically cycled full cell at 5C.

Chapter 6. Asymmetric nanopore full battery

6.1. Escalating full cell output potential

Increasing cell voltage is one possible method to improve energy and power density. A full cell device with voltage window from 0.2V to 1.8V was demonstrated by cycling the cathode between V_2O_5 and LiV_2O_5 and anode between $Li_2V_2O_5$ and LiV_2O_5. If anode side can be replaced by a lower potential material, the total output voltage can be further increased.

To begin with, Pt ALD process is established as current collector for nanopore battery, since surface RuO_2 on Ru metal has large capacity when discharged below 2V[84], which can interfere low voltage anode characterization. Pt process will be developed using Trimethyl(methylcyclopentadienyl)-platinum(IV) ($MeCpPtMe_3$) and O_2.

Sufficient dose of precursor is needed for uniform and conformal thin film deposition across both planar and 3D surfaces. Based on the kinetics of impingement flux onto a surface, one effective way to quantify the dose is by the product of a precursor's partial pressure (P) and the time (t) it takes to fully saturate a surface.

$$Pt = S\sqrt{2\pi mkT} \quad ,$$

where S is the number of molecules to saturate a unit surface area, m is the precursor molecular mass, k is the Boltzmann's constant, and T is the temperature[85]. On a planar sample, the growth rate of an ALD process will saturate with increasing dose of precursor due to the self-limiting behavior. While for a nanopore with high aspect ratio geometry, it

becomes significantly more difficult to saturate the exposure because of the limitation in precursor diffusion kinetics. A model of the relation between ALD conformality in high aspect ratio trenches and the exposure dose was proposed by Gordon et al[85], where a indicates the aspect ratio.

$$Pt = S\sqrt{2\pi mkT}\left(1+\frac{19}{4}a+\frac{3}{2}a^2\right)$$

Increasing precursor partial pressures and exposure times facilitate deeper penetration into high aspect ratio nanopores while the conformality will be hindered with increased molecular mass of precursor. As aspect ratio increases, the exposure dose scales up quadratically, which means a substantial longer exposure time in order to provide saturation for the entire surface.

Therefore, it is of great importance to optimize the exposure dose for nanopore batteries since the metal contacts at the two ends of AAO pores will penetrate too deep and short the device if the precursor is over-dosed, while under-dosing the precursor will lead to too small the length of electrodes, which may jeopardize the battery performance when cycled at high rate. In this nanopore battery, the depth of Pt into AAO pores is optimized using exposure mode in a Fiji F200 reactor with APC valve closed during precursor pulse to facilitate precursor diffusion into high aspect ratio channels. Pt grows deep into the AAO pores with 30s Pt precursor exposure time while keeping the two electrode insulated.

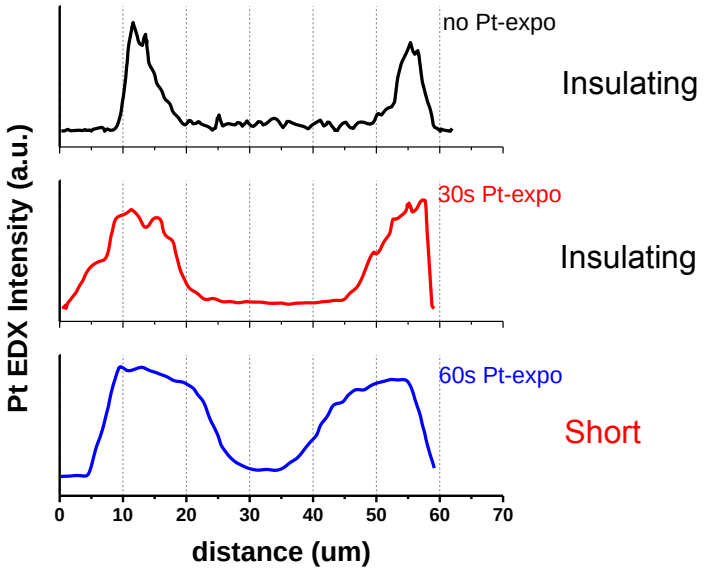


Figure 23 Pt EDS intensity line scan along AAO nanopore cross section with same Pt precursor pulse time and different precursor exposure time. The Pt electrodes at two sides of AAO are insulating with 0s and 30s exposure time, while they are shorted if the exposure time is increased to 60s.

After Pt current collector deposition, different anode material is explored to find the ones compatible with current nanopore system in order to fabricate an asymmetrical full cell nanopore battery. Promising candidates include amorphous and crystalline TiO_2 and amorphous SnO_2 by ALD, Si deposited by pulsed low pressure chemical vapor deposition (LPCVD), plasma enhanced PECVD and sputter (Table 3). Considering the rapid capacity fade of amorphous TiO_2 and the difficulty in controlling conformality by sputter or CVD, the anode materials investigated in this thesis will be ALD anatase TiO_2 and SnO_2.

Table 3 Candidates for nanopore battery anode materials.

Anode material & deposition techniques		Limitations
TiO_2	Amorphous (ALD thermal H_2O)	Rapid capacity fade
	Crystalline (ALD thermal O_3)	
Si	Plasma enhanced CVD/sputter	Low conformality low mass loading
	Pulsed LPCVD	Si deposition at two sides
SnO_2	ALD thermal H_2O	

6.1.1. V_2O_5-TiO_2 asymmetric full cell

Using the wide voltage range of V_2O_5, we have demonstrated an asymmetrical cycling window of a full cell device. In order to further enhance cell voltage, anatase ALD process is developed for anode deposition using TDMAT an O_3 as precursor, with growth rate around 0.5A/cyc. Though it is larger when temperate is higher than 230C, TDMAT doesn't decompose until 300C. XRD spectrum indicates that pure anatase phase begins to form at 225C, while Raman shows that crystallinity starts at 210C. It may due to locally micro crystalline domains, which are not predominant at large scale, thus not detectable by XRD. The CV curve shows reduction peak at1.6V oxidation peak at 2.2V.

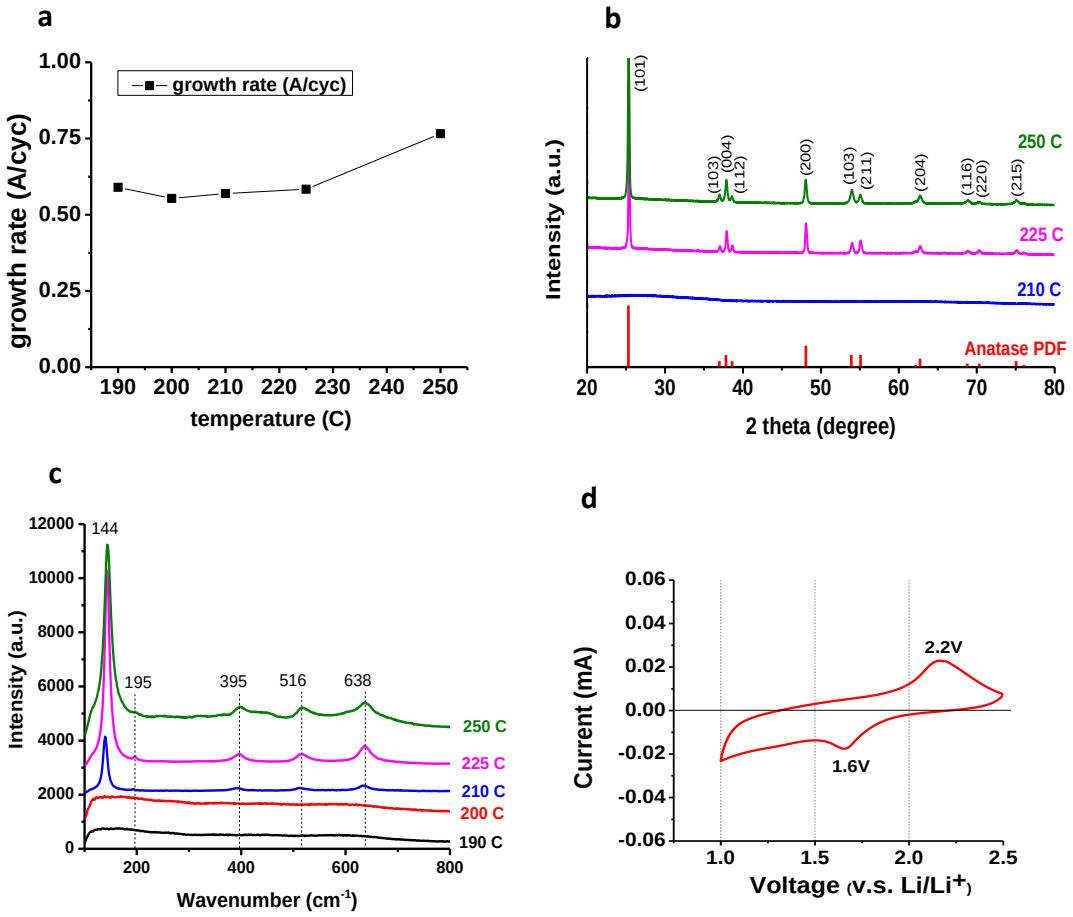


Figure 24 crystalline TiO_2 ALD process by TDMAT and O_3. (a) Ozone process temperature window. (b)XRD and (c) Raman spectra at various deposition temperature. (d) Cyclic voltammetry of TiO2 vs. lithium metal

In this V_2O_5-TiO_2 asymmetric full battery, Ru is also used as current collector, then crystalline TiO_2 and V_2O_5 are deposited on top of Ru sequentially. Figure 25a illustrates the EDS mapping for cross section of this asymmetric nanopore battery array. Ru penetrates around 10um into AAO pores at two ends, with V_2O_5 and TiO_2 at each side. Since the voltage window of TiO_2 is between 1V and 2.5V relative to lithium metal, we

achieve considerable increase of the full cell output voltage comparing to the symmetric configuration with V_2O_5 as the anode.

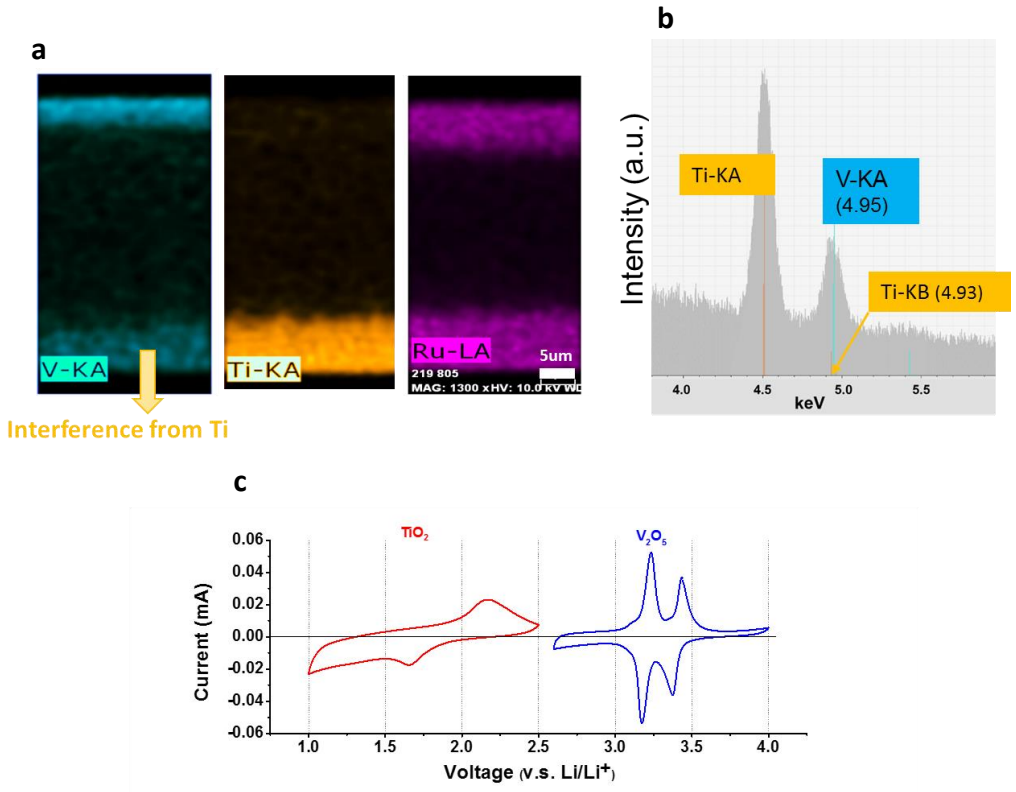


Figure 25 V_2O_5-TiO_2 asymmetric full cell. (a) EDS mapping for nanopore cross section (b) EDS spectrum showing Ti-KB (at 4.93keV) overlaps with V-KA (at 4.95keV), which explains the appearance of interference signal for V-KA from TiO_2 side in figure a. (c) CV measurement for V_2O_5 and TiO_2.

6.1.2. V_2O_5-SnO_2 asymmetric full cell

TiO_2 capacity can match with V_2O_5 at 1C cycling rate when current density is not very large, while its capacity fades rapidly under increased current density. SnO_2 shows great promise to match with V_2O_5 even at high cycling rate, since SnO_2 has large capacity and only a portion of which matches with V_2O_5 at low cycling rate, while at high cycling

rate, SnO_2 can extend to the full capacity range to provide high current density and compensate for capacity fading at high rate.

SnO_2 is deposited by a thermal process using Tetrakis(dimethylamino)tin(IV) (TDMA-Sn) and water at 150C with growth rate of 0.7A/cycle on silicon, which is confirmed by TEM cross section and in agreement with previous literature. In addition the SnO_2 ALD process has than 4% variation across a 4 inch wafer.

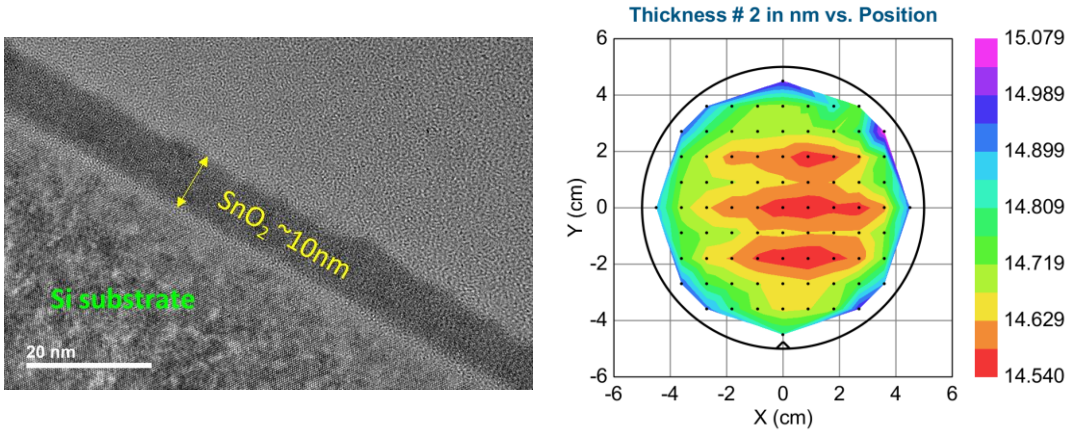


Figure 26 SnO_2 ALD process development. (a) TEM cross section confirms that 10nm SnO_2 is deposited by 150 ALD cycles (b) Thickness mapping of 200 cycle of SnO_2 by ellipsometer across a 4 inch silicon wafer.

We successfully fabricate a full battery consisting of an array of coaxial nanotubular electrodes and liquid electrolyte confined within AAO nanopores and connected in parallel. The nanoelectrodes are comprised of V_2O_5 cathode, SnO_2 and underlying Pt nanotube current collectors to form an asymmetric battery configuration, where the cathode and anode are separated by an electrolyte region.

The asymmetric nanopore battery array is tested in a Teflon Swagelok T-cell sealed under argon atmosphere (Figure 27a). V_2O_5 cathode side is in contact with a stainless steel rod as working electrode, SnO_2 is connected to the counter electrode by a piece of porous nickel foam (Figure 27a zoom in), which serves as a stress buffer layer to prevent AAO cracking while maintaining good electrical contact to SnO_2 anode. Its porous structure also ensure easy electrolyte filtration. The spring at counter electrode decouples rotational force during Swagelok connection sealing to avoid scratch on sample surface. Lithium metal is mounted by the side of AAO sample, serving as lithium source during SnO_2 pre-lithiation and reference electrode during full cell cycling.

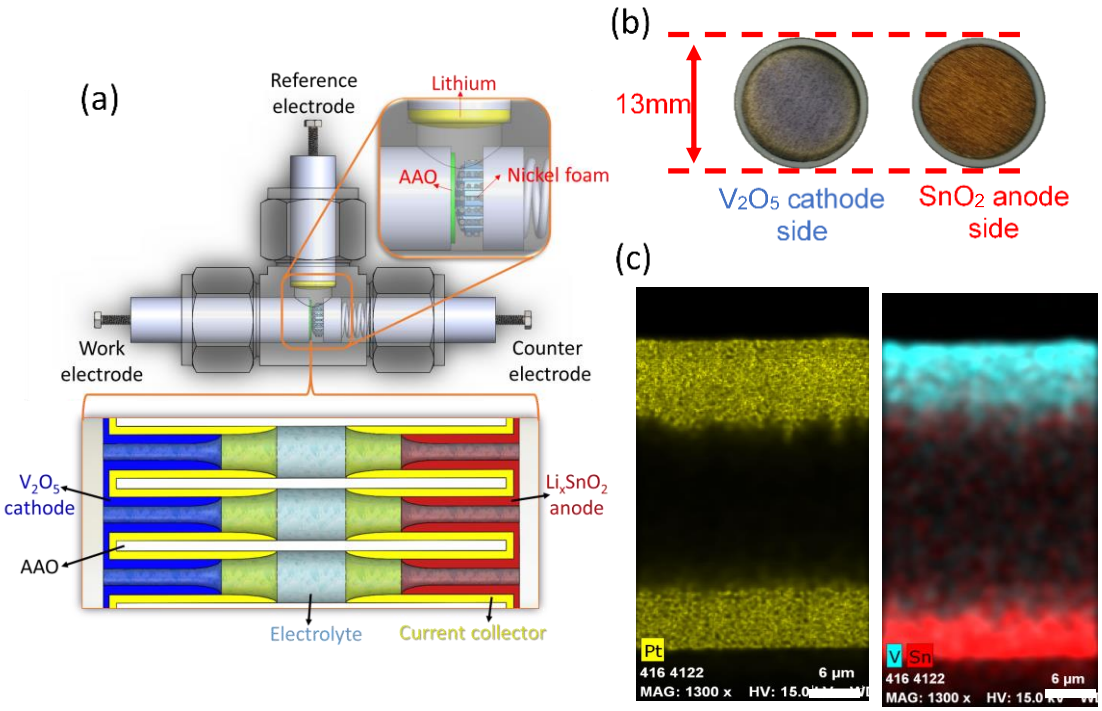


Figure 27 (a) schematic drawing of three electrode testing system for nanopore battery. Zoom-in image shows the cross section of the asymmetric nanopore battery inside AAO nanochannels. (b) photo images of a real device (c) EDS mapping for the cross section of the asymmetric nanopore battery.

In this asymmetric full cell, cathode V_2O_5 is cycled within one Li ion insertion region, from 3.8V to 2.8V vs Li metal. SnO_2 is electrochemically prelithiated as anode, the main reaction for SnO_2 is conversion ($SnO_2 + Li^+ + e^- \leftrightarrow Li_2O + Sn$). Various amount of lithium ion can be stored in SnO_2 during pre-lithiation process, which generates a wide voltage range for SnO_2. Charge/discharge profiles are plotted for full cells with moderate (Figure 28b) and deep (Figure 28c) SnO_2 prelithiation. When SnO_2 is cycled between 1.6-2.4V, full cell output voltage is from 0.3V to 2.0V, which can be raised up to a voltage window between 1.2V and 3.1V if SnO_2 is cycled within 0.7V to 1.7V range. For comparison, the absolute voltage range of both electrodes in a V_2O_5- V_2O_5 symmetric full cell is recovered from previous two electrode result by subtracting V_2O_5 cycling plot vs. lithium with the full cell profile (Figure 28a), where anode side V_2O_5 is confined in a relative high voltage to maintain high reversibility and the full cell output potential is limited.

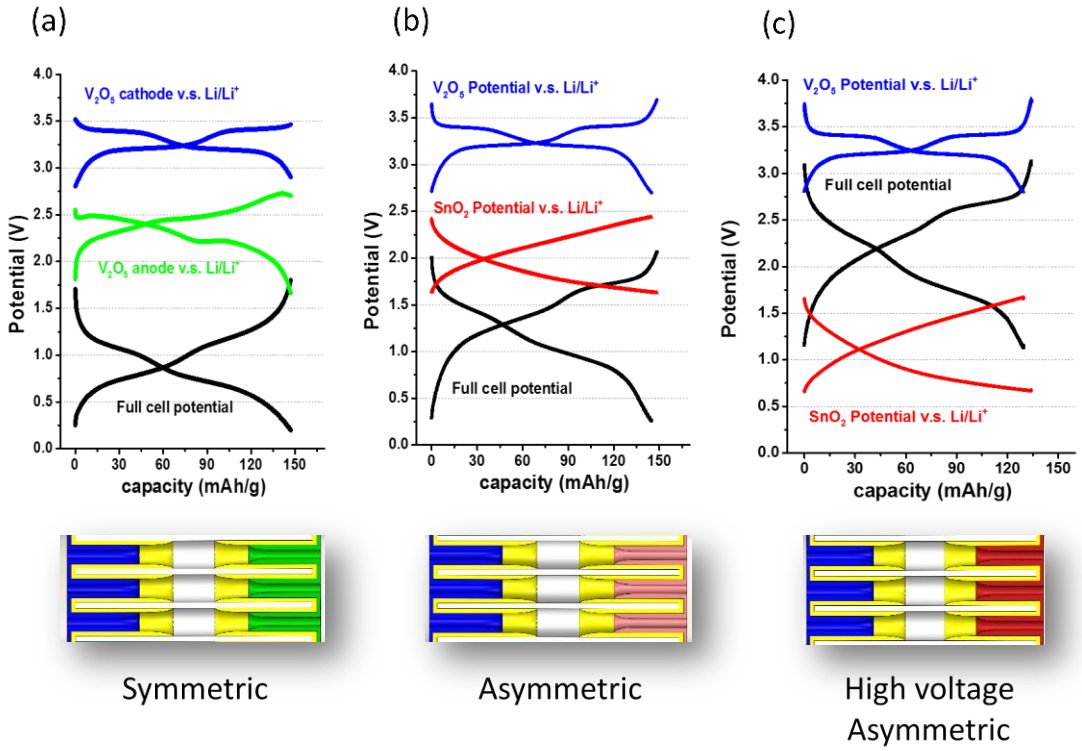


Figure 28 Charge/discharge profile at 1C for (a) V_2O_5- V_2O_5 symmetric full cell recovered from two electrode testing data, (b) V_2O_5- SnO_2 full cell with moderate SnO_2 pre-lithiation, and (c) V_2O_5- SnO_2 full cell with deep SnO_2 pre-lithiation.

When the capacity is normalized by V_2O_5 for convenient comparison with previous results, this asymmetric full cell has capacity of 130mAh/g at 1C, with 73% capacity retention at 200C (18s charge and discharge cycle) Impressively, the capacity fading after more than 500 cycles is only about 2% (Figure 29).

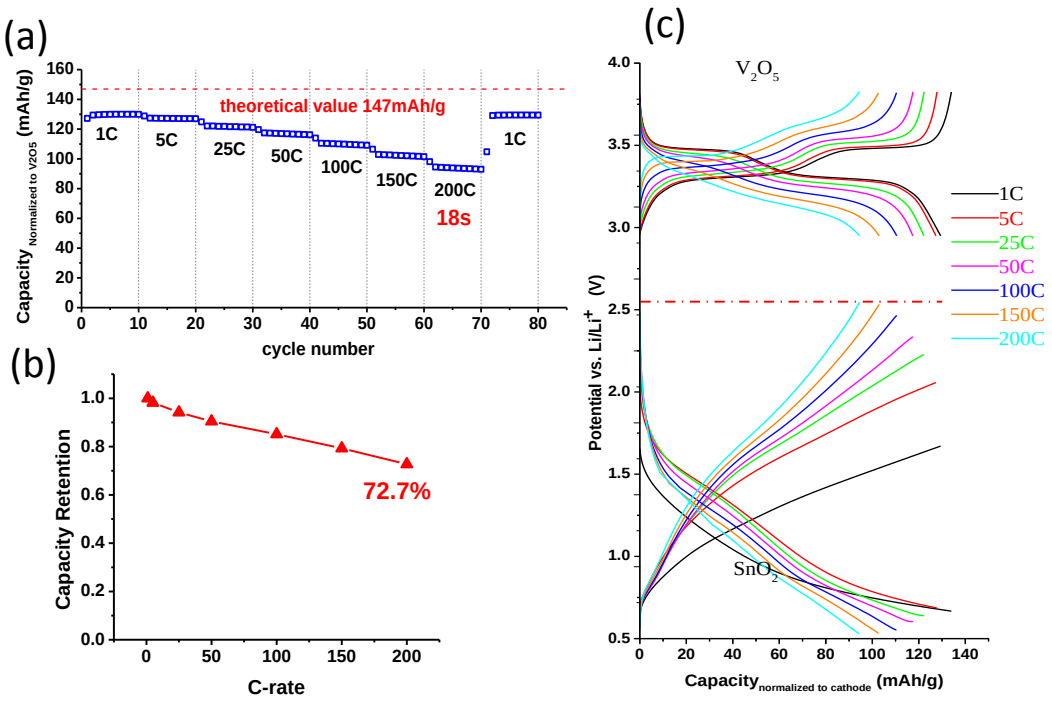


Figure 29 (a) Rate Performance of V_2O_5- SnO_2 full cell up to 200C. (b) Capacity retention with increasing C-rate. (c) Charge/discharge profile for both cathode and anode at various cycling rate.

When cycled at 5C, the normalized capacity of this full cell is highly stable within first 500 cycles with less than 2% capacity loss, nevertheless its capacity declines rapidly after 550^{th} cycle with 80% of the original capacity remaining at 946^{th} cycle. This stepwise life cycling behavior can be explained by the difference of capacity fading rate between V_2O_5 and SnO_2. Orthorhombic V_2O_5 thin film has been proved to have high reversibility within one lithium ion insertion region with long cycle life even at high current density. While SnO_2 shows limited cycle life, though thin film and protection layer can alleviate capacity fading. In this V_2O_5- SnO_2 full cell, V_2O_5 cathode is kept above 2.8V where fast one lithium insertion reaction happens and SnO_2 is confined below 2.8V to warrant a positive cell output potential. At 2^{nd} cycle, SnO_2 provides sufficient charge when cycled between

0.7V and 2.2V to match with V_2O_5. In order to maintain this capacity coherence with V_2O_5 side, the upper limit of voltage window of SnO_2 slowly increases and reaches the 2.8V limit at 550th cycle. After this critical point, the capacity of V_2O_5 cannot be fully utilized and the limiting factor for full cell capacity switches from V_2O_5 to SnO_2, which leads to the abrupt change in capacity fading rate.

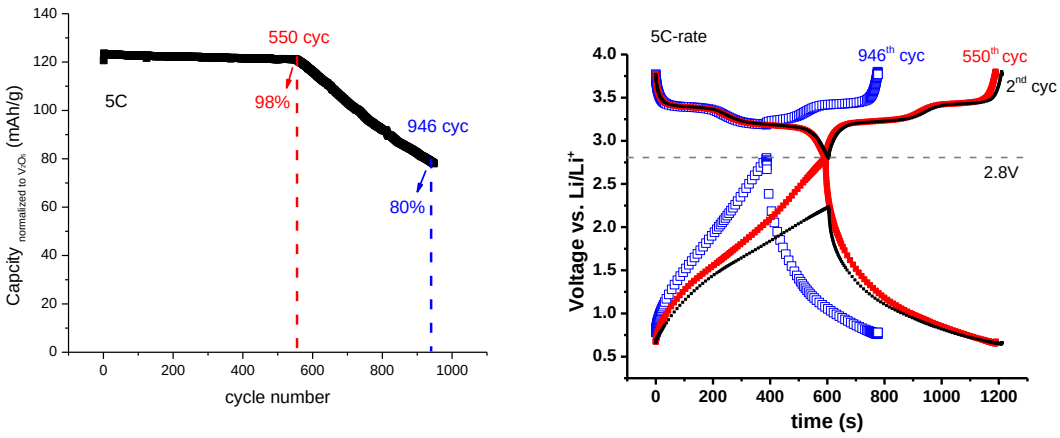


Figure 30 (a) Life cycling of V_2O_5- SnO_2 full cell. (b) Charge/discharge curves for V_2O_5 and SnO_2 at 2nd, 450th and 926th cycle.

When lithium ions are shuttled between the straight nano-channels between V_2O_5 cathode and SnO_2 anode inside the nanopore battery, using lithium metal as reference electrode, during cyclic voltammetry measurement we observe high capacity retention at high scanning rate, with distinct peaks up to 100mV/s indicating lithium ion insertion (Figure 31a). In contrast, if lithium metal is used as both counter and reference electrodes, capacity fades drastically with increasing scan rate with large separation between anodic and cathodic peaks (Figure 31b). Such different behavior in this two configuration demonstrates the importance of short ion transport path in high rate batteries, especially for nanostructured devices.

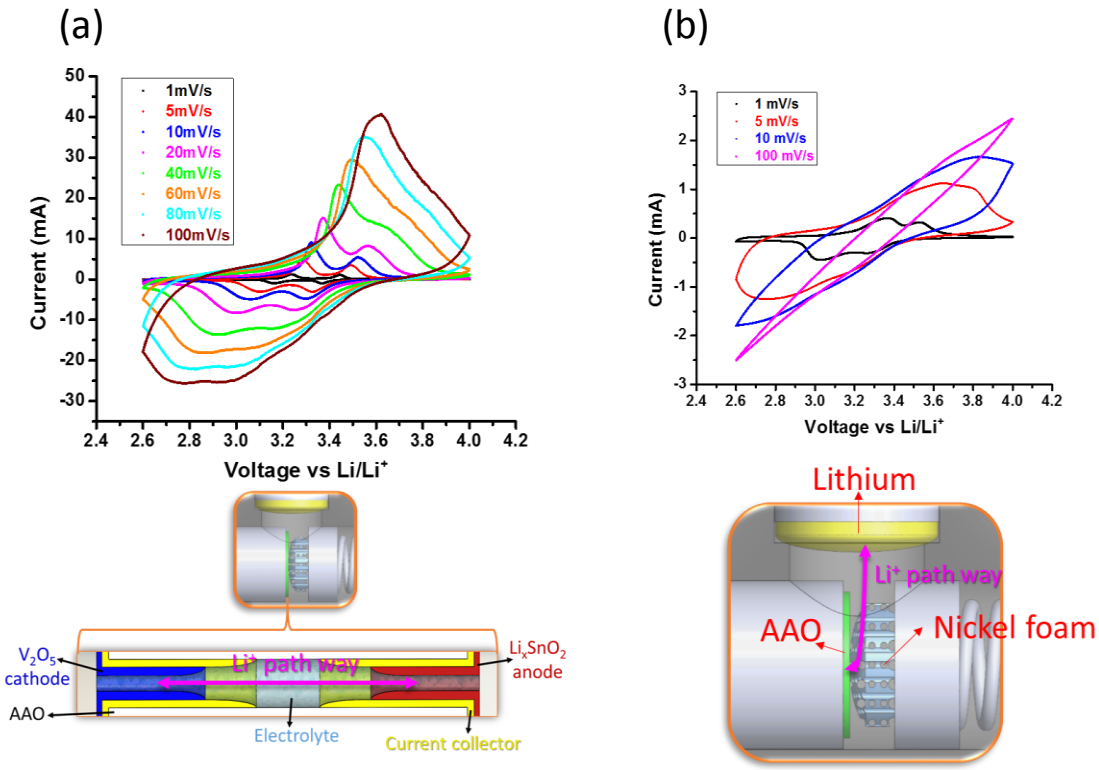


Figure 31 (a) Cyclic voltammetry with V_2O_5 as working electrode and SnO_2 as counter electrode, showing obvious ion insertion peaks with scan rate up to 100mV/s. Schematics illustrates lithium ions shuttle through straight nanotube. (b) Cyclic voltammetry with V_2O_5 as working electrode and lithium foil as counter electrode, displaying dramatic capacity fade with increasing scan rate, where lithium ions have long and tortuous pathway.

In summary, this nanopore structure overcomes the limitations of a conventional battery design, where micron sized ion storage particles are embedded in the random carbon black matrix. Each electrode microparticle cannot be guaranteed with either ion access from the electrolyte or electrical connectivity from the current collector due to the structural randomness, while a self-aligned electrode with integrated coaxial current collectors can ensure fast electron transport by underlying current collector and short Li ion diffusion path through thin V_2O_5 and SnO_2. Moreover, straight channels in the nanopore

battery facilitate Li ion transport between cathode side and anode side compared to tortuous ion pathways in polymeric separators.

6.2. Increase active storage material mass loading

By extending the design to various dimensions, we project that increased mass loading of storage materials will provide considerable improvement in power and energy density. Table 1 summarizes two strategies for geometry optimization. The volume of inactive non-storage material can be significantly reduced by maximizing AAO porosity (opt1). The AAO template used in this study has porosity of around 32%, but can be increased (e.g., by pore widening) up to 55%. Accordingly, cathode mass loading could be increased by 4.8X if unused volume from AAO is reduced and electrodes grow deeper into the pores. In addition, the mass loading of storage materials can be further amplified if we dissolve AAO and deposit electrode materials on both inner and outer side of the current collector nanotubes (opt2). V_2O_5 is assumed to be no more than 30nm thick for both of the optimizations to ensure a minimal sacrifice in power while escalating volumetric energy density. (Table 4)

Table 4 Cell geometry optimization for higher volumetric energy and power density

Geometry optimization	**current geometry**	**geometry opt1 (keep AAO)**	**geometry opt2 (dissolve AAO)**
AAO porosity	0.32	0.55	0.40
pore diameter (nm)	150	75.3	90
pore period (nm)	251	96.6	135
V_2O_5 depth (nm)	6000	20000	20000
Inner V_2O_5 thickness (nm)	21	20	30
Outer V_2O_5 thickness (nm)	N/A	N/A	20
Ru thickness (nm)	7.5	7.5	7.5
Actual V_2O_5mass (ug)	58	N/A	N/A
Actual V_2O_5 mass/volume (ug/cm2um)	3.9	N/A	N/A

Calculated V_2O_5 mass/volume (ug/cm2um)	5.5	42.09	94.92
1C power density (uW/(um·cm^2)	0.492	5.21	11.76
1C energy density (uWh/(um·cm^2)	0.598	6.34	14.29
150C power density (uW/(um·cm^2)	52.16	552.84	1246.75
150C energy density uWh/(um·cm^2)	0.192	2.03	4.59
*Assume power and energy density linearly increase with mass loading per volume			

Using asymmetric configuration to increase full cell output potential, the nano pore battery has massive improvement in the volumetric energy and power density. Moreover, we project that with geometry optimization to increase mass loading, the energy and power matrix can be further improved (Figure 32). The geometry optimization method include AAO pore widening, increase electrode depth and introduce interconnections between AAO pores in order to reduce the "dead" volume of AAO. We have successfully fabricated an interconnected AAO scaffold with 5.5X mass loading compared to the V_2O_5-SnO_2 asymmetric full cell even with the same electrode thickness, which means it can maintain the power performance while significantly increasing the energy density.

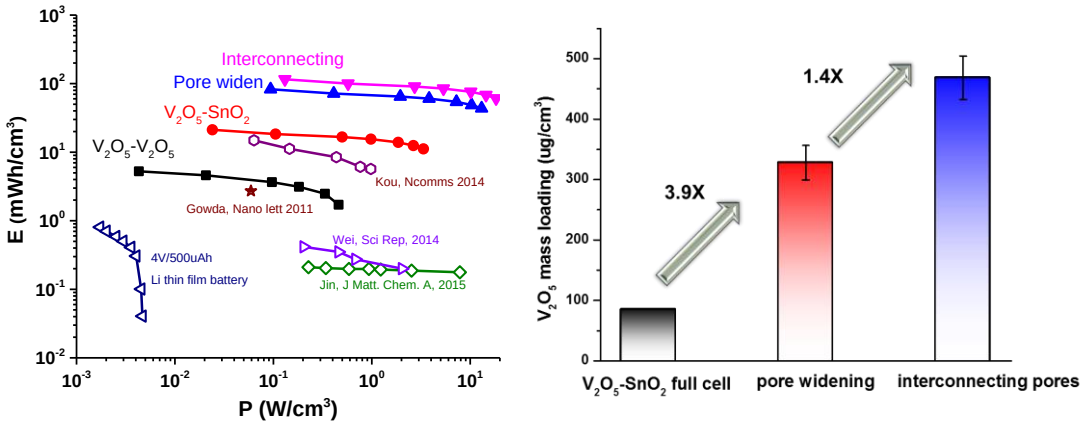


Figure 32 (a) Ragone plot for nanopore batteries. (b) Increase active material loading by AAO geometry optimization.

Chapter 7. Perspectives and future work

In this thesis, a full battery inside a single nanopore with $2X10^9$ /cm^2 density in parallel has been successfully fabricated. Such a platform uncovered the science that under current geometry ion transport in highly confined electrolyte is still very efficient and the limitations for high rate performance comes from electron conduction in electrodes. With integrated current collector, the nanopore battery has achieved rapid electron transport, which leads to theoretical capacity as fast battery (<1h charging) and high capacity retention at high rates (up to 72% with 18s charging). Moreover, the nanopore battery has realized ultra-fast ion diffusion in thin active storage material, which blurs the traditional boundary between surface reaction and bulk insertion. By using low voltage anode materials, the asymmetric nanopore battery has demonstrated significant improvement in energy and power density, which can be further improved by AAO geometry optimization.

7.1. Ionics near battery electrode surface under nano-confinement

Highly confined electrolyte environments become inevitable when electrodes are densely packed to take advantage of nanostructures in high power storage applications. Therefore, ion transport within nano-confined electrolyte between interfaces of electrolyte/active storage material is essential for understanding the underlying science at/near the battery electrode surface. [2] Exploring the nanoscale ion transport will provide guidance to overcome the current limitations and improve the performance of nanostructure systems for energy storage. Both the symmetric and asymmetric nanopore batteries discussed previously provide a good system to simulate the nanoconfinement of electrolyte controllably. Nonetheless, current research is still out of the electric double layer regime,

which can be in the range of several nanometers depending on solution concentration. Based on the interesting results we have achieved in the nanopore battery platform, we proposed to use solid-state nanofluidic devices as a model system to further investigate the physics of ionic transport in nanoscale-confined electrolyte. Our collaborator Prof. Mark Reed group has studied aqueous monovalent/divalent ions in nanochannels. [86, 87] Such nanochannel devices are fabricated via standard semiconductor approaches and benefit from well-defined geometries, with manifested potential of electrically modulating the ionic transport. [88] Utilizing atomic layer deposition (ALD) for well-controlled surface properties at the solid/fluid interface, nanofluidic devices can serve as an effective platform to explore a broad range of different electrode materials. ALD is known for the sub-nanometer control of film thickness due to its self-limiting deposition property. [89] Integrating ALD electrode storage material with nanofluidic devices opens up new opportunities for quantitatively understanding the physics of highly confined ionic systems, and provides important insights into the design of next generation batteries with improved performance.

Using the ion channel setup illustrated in Figure 33, we expect to detect surface charge variation and ion depletion during battery cycling by recording the conductance change with various gating voltage.

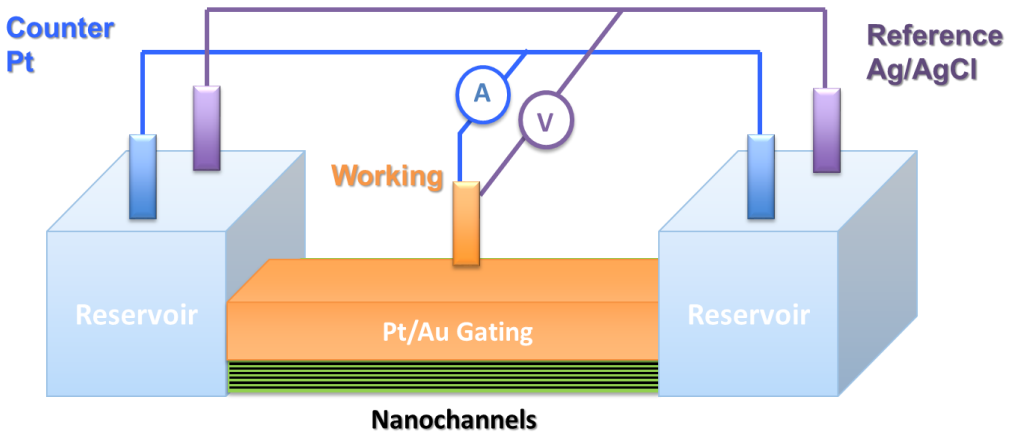


Figure 33 Schematic drawing for battery materials cycling inside nanochannels

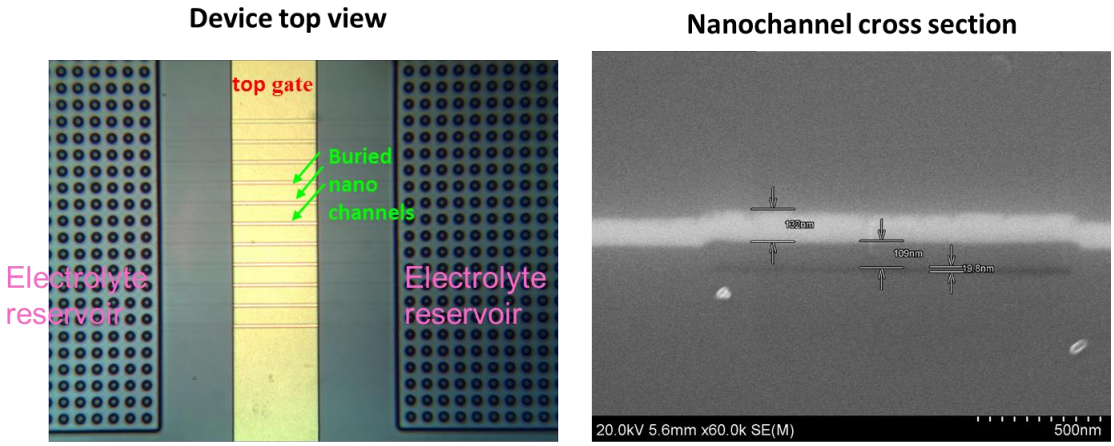


Figure 34 nanochannel top view and cross section view.

The advantages of ALD are tunable conformality of battery material (V_2O_5) inside nanochannels , as shown in Figure 35, and the capability to fabricate an extremely thin sacrificial layer to define ultrathin nanochannels (5nm or less).

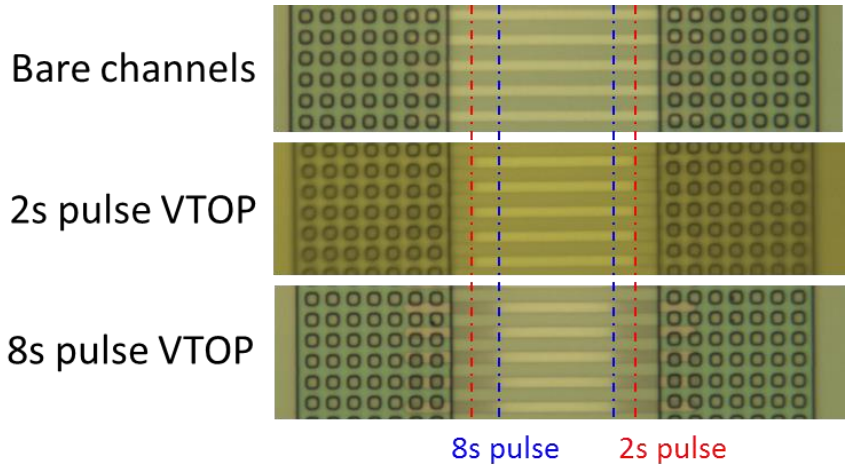


Figure 35 Revolve ALD V_2O_5 conformity in high aspect ratio nanochannels from optical microscope.

7.2. Solid-state nanopore batteries

The knowledge gained from the nanopore battery with liquid electrolyte brings us implications about design directions for all-solid-state nanobatteries. Two major challenges for all-solid-state batteries are low ionic conductivity of solid electrolyte and high inter-facial resistance. $LiAlS_2$ has been demonstrated with high ionic conductivity (10^{-4}S/cm) by our collaborators at Argonne National Lab.

In order to decrease interfacial resistance, $LiAlS_2$ was proposed to be both anode and cathode to avoid sharp heterogeneity at electrode/electrolyte interface in the conventional solid state battery design. Theoretically, $LiAlS_2$ can undergo the following decomposition reactions when it's held at certain potential.

High potential side: $LiAlS_2 \rightarrow 0.5Al_2S_3 + 0.5\underline{\mathbf{S}} + Li^+ + e^-$

Low potential side: $LiAlS_2 + 5.25Li^+ + 5.25e^- \rightarrow 0.25\underline{\mathbf{Li_9Al_4}} + 2Li_2S$

As a result, sulfur generated under high voltage can serve as cathode and Li_9Al_4 formed at the low potential side can function as anode, while still maintain similar structure and elemental components to $LiAlS_2$ electrolyte. The device include Pt at both side of AAO membrane as current collector and define the regime for both cathode and anode, and a continuous layer of $LiAlS_2$ all through the AAO pores. Various thickness of $LiAlS_2$ can be attempted, nevertheless, thickness around 60nm that almost closes the pores can maximize mass loading and the cross section area of ion conduction path.

Similar mechanism has been demonstrated in $Li_{10}GeP_2S_{12}$ (LGPS) micro particles mixed with carbon black[90], while the proposed Pt/$LiAlS_2$-$LiAlS_2$-Pt/$LiAlS_2$ nanopore battery is supposed to achieve higher rate performance enabled by faster electron conduction through integrated Pt current collector network and ion diffusion through nanometer thin lithium ion storage layer. In addition, vapor phase deposited $LiAlS_2$ will improve electrical contact between current collector and electrode material, compared to the hard pressing method in previous report [90].

Lithium *tert*-butoxide ($(CH_3)_3COLi$, LTB), Tris(dimethylamido)aluminum(III) ($Al(N(CH_3)_2)_3$, TDMA-Al) and Hydrogen Sulfide (H_2S) are used as precursors to deposit at 150C. The dosing of LTB, TDMA-Al, and H_2S is 5, 5, and 10 seconds, respectively.

In order to test the conformality of recipe for $LiAlS_2$, we use a Li_2S ALD process, which has the same pulse and purge time with the $LiAlS_2$ one, while omitting the step for aluminum precursor. EDS scan along the AAO cross section shows continuous sulfur signal, indicating conformal coating through the AAO pores. The top view of the AAO

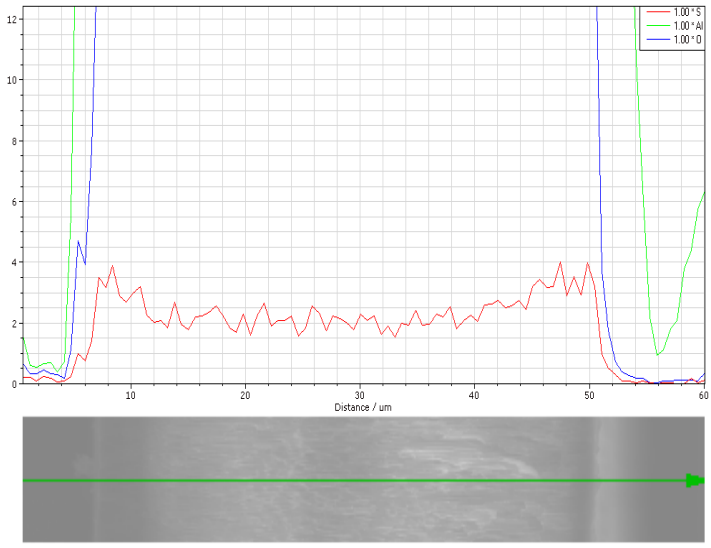


Figure 36 EDS line scane of AAO cross section after 500 cycles of Li_2S deposition

Chapter 8. Appendix/Side projects

8.1. Evaporator for air sensitive material

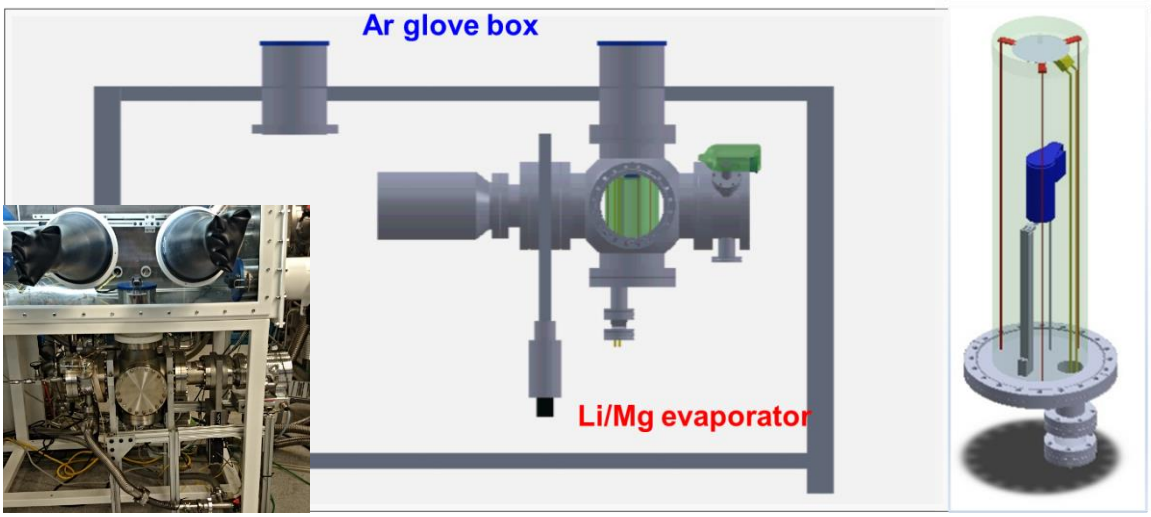


Figure 37 CAD design for air sensitive material evaporator, which is integrated with Ar glove box. Both evaporation source and samples can be loaded through Ar glove box and transfer to ALD and UHV integrated system without air exposure.

8.1.1. One application of lithium evaporator: deconvoluting interface engineering from physical wetting of a ALD layer between the lithium/garnet interface

The substantial ion conductivity improvement of Li/garnet/Li interfaces motivates us to further investigate the mechanism of this ultra-thin Al_2O_3 interlayer. Approximately 3μm Lithium metal is seamlessly coated on garnet surface by thermal evaporation providing intrinsically reliable physical contact (Figure 38a). The lithium electrode area is defined to be 0.25cm^2 by shadow mask (Figure 38b insert). EIS measurement was carried out from 1MHz to 50mHz at room temperature with the Li/garnet/Li samples directly pressed between two stainless steel disks (SSD). All the fabrication and testing are

conducted in argon or under vacuum with no air exposure. EIS of Li/bare garnet/Li indicates significant improvement from melted lithium electrodes (with larger than 3k Ωcm^2 interfacial resistance), which is contributed from improved physical wetting. The noise at high frequency may due to large contact resistance between lithium and SSD. Moreover, the interfacial resistance is further reduced with 10 cycle ALD Al_2O_3 interlayer. This result provides direct evidence that the Al_2O_3 layer not only improves physical wetting of lithium on garnet surface, but also acts as an important ion conductive interlayer when lithiated.

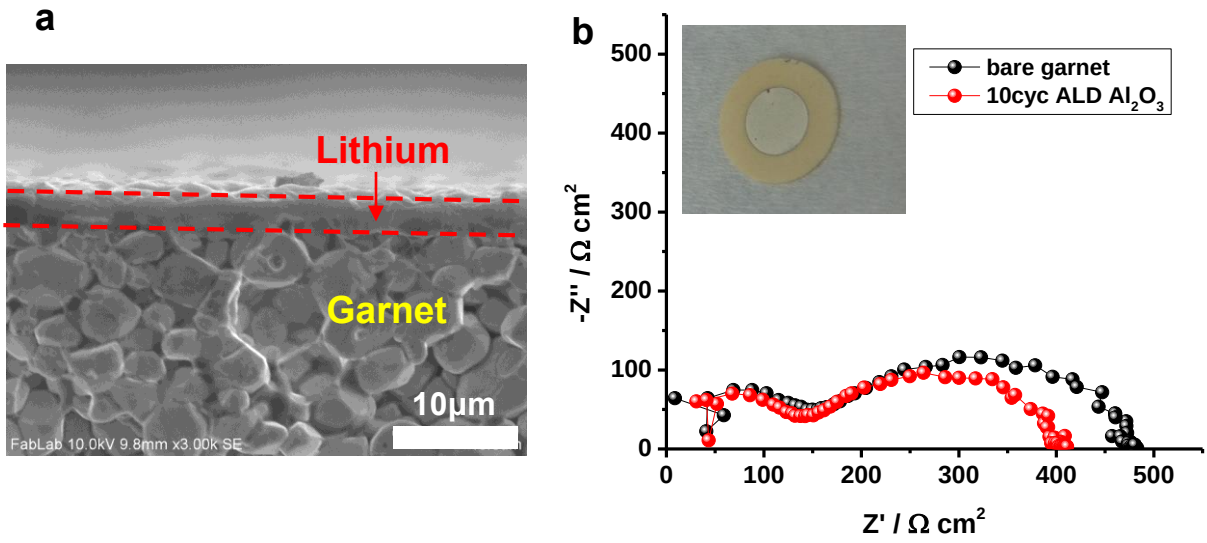


Figure 38 (a) cross section of evaporated lithium on garnet. (b) EIS of bare garnet and Al_2O_3 coated garnet with evaporated lithium contacts. Insert shows an image of real device with metallic lithium electrodes.

The fabrication and testing of evap-Li/ALD-Al_2O_3/garnet samples were carried out in clean argon or under vacuum, without air exposure. The integrated system used here contains a Cambridge Nanotech Fiji F200 ALD, which is connected with a home-built

thermal evaporator through an MBraun Argon glove box. Polished garnet samples were loaded from glove box to the ALD system. 10 cycles of Al_2O_3 were performed on the samples at 150C with 0.06s pulse time and 20s purge time for both TMA and H2O. Then the garnet samples were transferred through the glove box and loaded into the lithium evaporator together with fresh cut lithium source. The evaporator was pumped down to base pressure of $2X10^{-7}$ Torr. The crucible was heated to around 300 ℃ to obtain ~2A/s lithium deposition rate monitored by a quartz crystal microbalance (QCM). 3um lithium films were deposited at both sides of the garnet samples with and without ALD Al_2O respectively. The area of lithium was defined by shadow masks. After that, the samples were transferred back to glove box and tested under room temperature with two stainless steel disks pressing at both sides as electrical contact.

8.2. Nanopore battery Degradation.

A half cell was opened after rate testing and aging in electrolyte for more than 6 months. The electrode was found without any crack after reopening the coin cell and was washed by dimethoxyethane (DME) to clean the residue organic electrolyte before SEM testing. It still shows a strong vanadium signal in SEM EDS elemental mapping, revealing around 6μm depth vanadium oxide remaining in the pores (similar to the as-prepared measurement) after cycling (). No visible morphology changes were observed after cycling. Notably, the AAO membrane remained unbroken after reopening the coin cell, which demonstrates the mechanical robustness of AAO during processing.

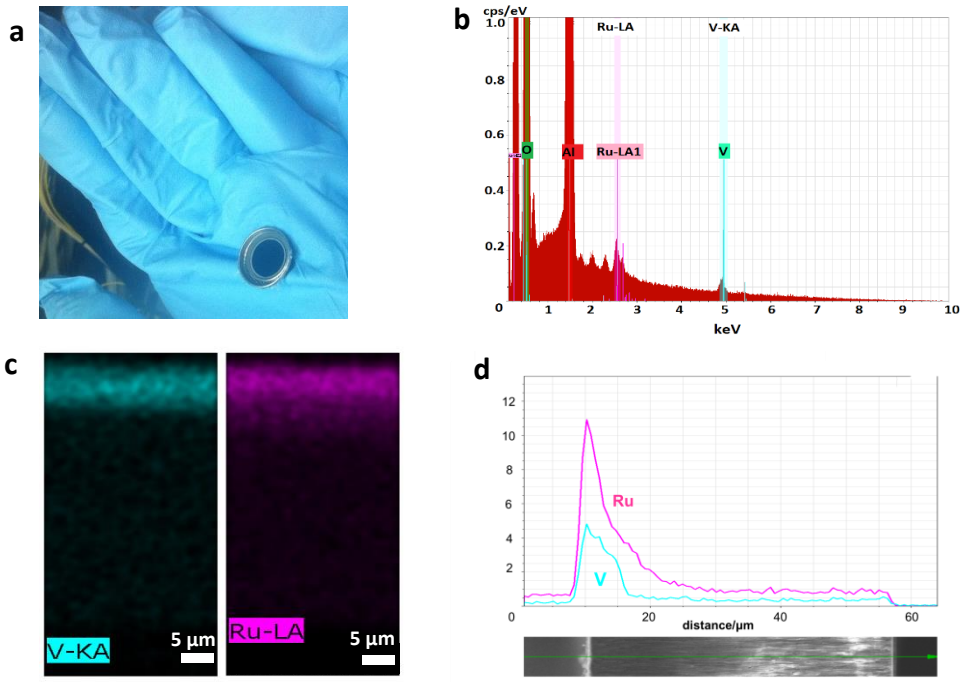


Figure 39. Half cell after cycling. (a) Intact half cell after cycling and reopening the coin cell, indicating the mechanical robustness of the device. (b) EDS spectrum indicates strong vanadium signal (blue). (c) and (d) elemental mapping and line scan both indicate around 6µm depth vanadium oxide remaining in AAO pores.

We are also interested in the local electrochemical stability of this massive nanobattery array, by cycling certain number of selectively connected nano batteries by EC-AFM in order to detect local electrochemical behavior and possible defect related local degradations. Hopefully to get a statistically understanding of this nanobatteries. We were ambitious at the beginning and wanted to measure single nanopore battery, but the current/noise ratio turns out to be a huge issue, so we decided to take a step back and try to measure a series of selectively parallel connected nanobatteries.

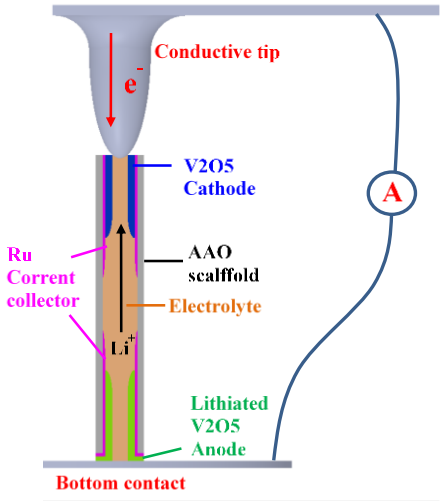


Figure 40 single nanopore battery cycled c-AFM

Top contact pads are patterned with shadow masks using evaporation, when the feature size is larger than 10um, we can get nice sharp well defined area. The edge definition is vague, when the critical dimension is smaller than 2um. So for smaller patterns, focused ion beam (FIB) is used to isolate the region of interest by sputtering the surrounding materials, which can then be approached by EC-AFM tip and selectively cycle parallel connected nanopore batteries. This technique provides an opportunity to detect local shorting and/or hot spot that could result in fast degradation.

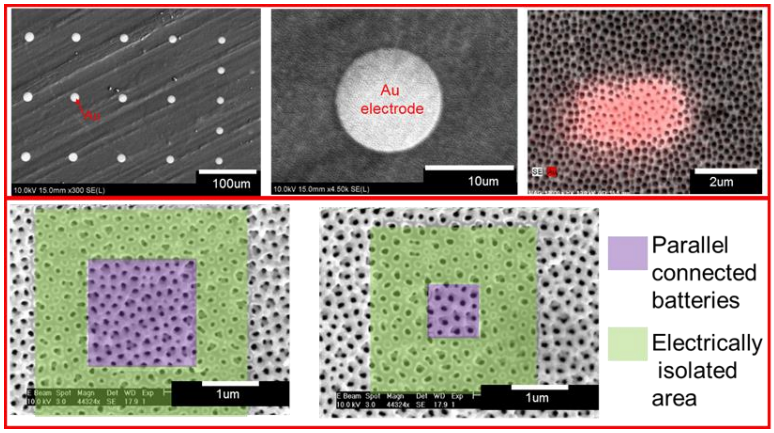


Figure 41 Patterned top electrodes by shadow mask evaporation and FIB

8.3. Active storage material loading compared to commercial batteries

With material and geometry optimization, the nanopore battery has achieved considerable energy and power density, nevertheless, the percentage of active storage materials is still insufficient compared to commercial 18650 batteries, due to the limited porosity of AAO.

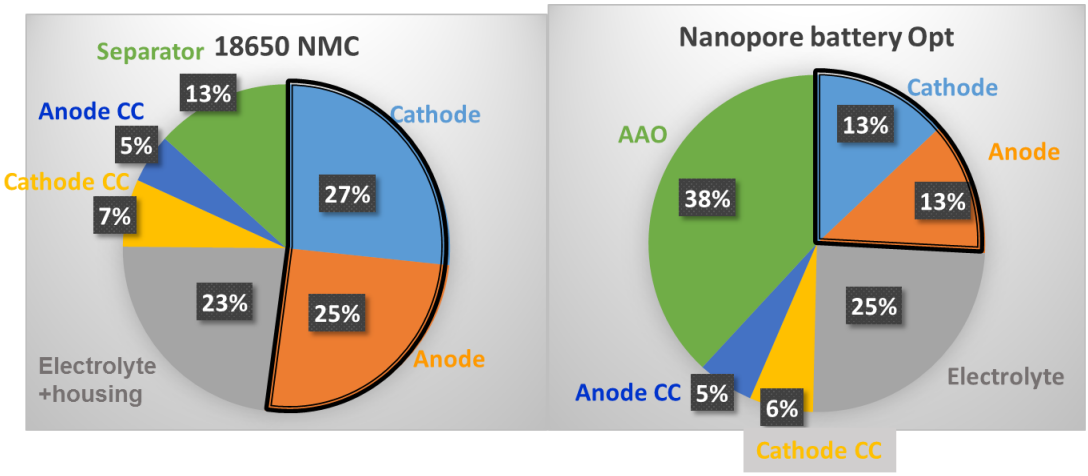


Figure 42 Volume percentage comparison between traditional a cylinder 18650 battery and the optimized nanopore battery

Layered structures of thin film solid state battery provides a solution to further increase active storage material mass loading. The mass loading of active storage material can be largely increased in a solid-state battery compared to a traditional cylinder battery, since thick aluminum and copper foil current collectors can be replaced by thin film current collector with much less electrolyte mass loading. Table 4 lists the mass loading for different battery components in 3D solid state batteries with single and double layer configurations.

Table 4 mass loading of battery components for single layer and bilayer solid state batteries.

	Single layer		Double layer	
component	thickness (nm)	Mass loading	thickness (nm)	Mass loading
cathode stor	500	49.7%	500 & 350	54.8%
anode stor	300	29.3%	300	28.7%
electrolyte	50	4.7%	50	5.2%
cathode curr coll	15	4.1%	15	4.7%
anode curr coll	15	4.2%	15	3.7%
Si pillar	NA	8.0%	NA	2.9%

Considering 20% housing weight, solid-state battery still gain more than 50% mass loading than traditional 18650 cylindrical battery (Figure 43). Considering planar LCO/LiPON/Li thin film batteries have been demonstrated with high capacity retention at high rate (up to 51.2C) [91], such high mass loading in solid state batteries can project record energy and power density.

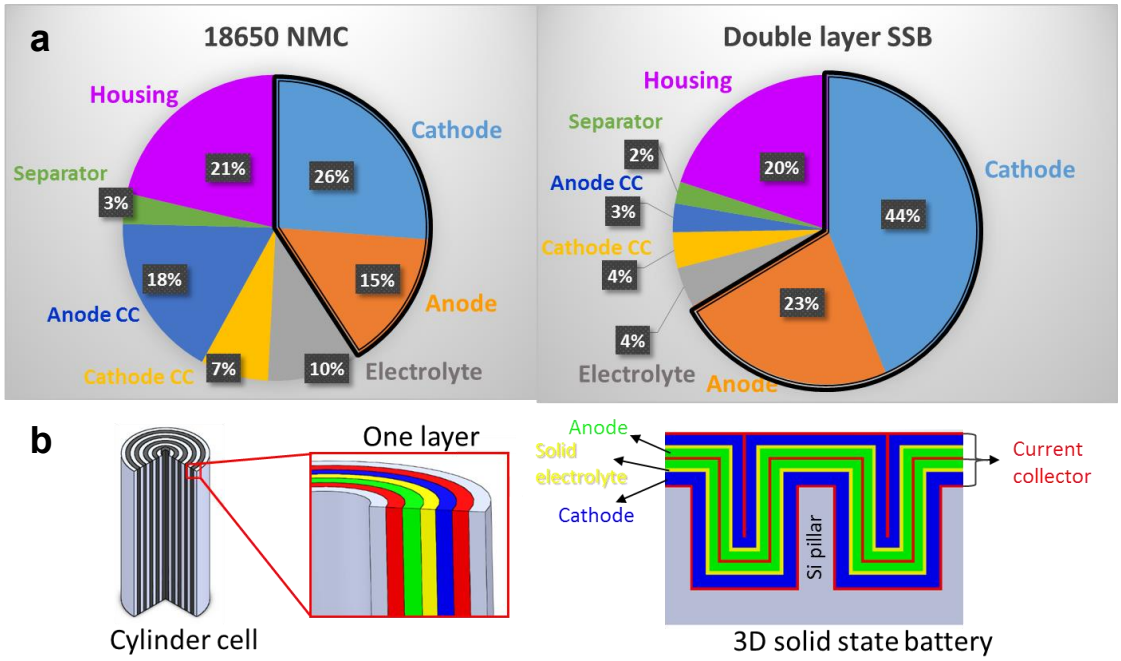


Figure 43 (a) mass loading comparison between traditional a cylinder battery and a 3D solid state battery. (b) schematic drawings corresponding to a cylinder battery and a 3D solid state battery,

with layers of current collector (red), cathode material (blue), electrolyte (yellow), anode material (green).

8.4. Improve graphene conductivity by ALD

With huge application potential in transparent and flexible electrodes for batteries and portable electronics, graphene has appealed enormous attention from researchers. Random networks of graphene flakes prepared by solution methods are especially attractive in nano-manufacturing due to its cost efficiency and low percolation threshold. One main challenge for solution based process is the difficulty to minimize the overlap between different flakes while still keep them electrically connected. When low concentration graphene ink is used to prepare high transmittance thin film, where the graphene flakes are easy to be separated with each other, which hinders the conductivity of the graphene film.

Defects in individual graphene flake also has vital influence on the electrical properties. Large scale graphene films grown by chemical vapor deposition (CVD) are inevitable to have structural defects like dislocations and grain boundaries. Another commonly used method to prepare graphene is physical exfoliation from highly ordered pyrolytic graphite (HOPG), which can also generate macroscopic defects like cracks, wrinkles and folds, arising from graphene transfer process. These defects all contribute to charge carrier scattering, which hinders electrical transport across the surface, limiting the performance and reliability of related devices.

ALD enables film deposition with subnanometer thickness control and unparalleled conformality even over the most demanding topography.[22, 24, 25] Furthermore, it can be material-selective, nucleating immediately on some surfaces but showing a substantial

nucleation delay on others [92, 93]. The ideal graphene basal plane is composed of sp^2 hybridized carbon atoms linked to one another in a 2D honeycomb lattice with high electron-density in its aromatic rings. Together with the high C–C bond energy (4.9 eV), the repelling field from delocalized π-orbitals lead to chemical inertness of graphene basal planes, which allows graphene to become the thinnest impermeable membrane[94]. Hydroxyl terminated substrate surface and defect sites on graphene (point, line and boundary) are considerably more reactive[95], providing an opportunity for selective ALD deposition of very thin conducting layers to improve conductivity across graphene defect sites. Ru and Pt both show significant nucleation barrier on CVD graphene [96]. Selective Al_2O_3 ALD on CVD graphene defects [97] demonstrates effective corrosion resistant coatings[98, 99]. Nevertheless, there remains insufficient research on selective ALD growth of conductive materials on graphene and to improve the conductivity of large scale solution based graphene thin films in a nano-manufacturing perspective.

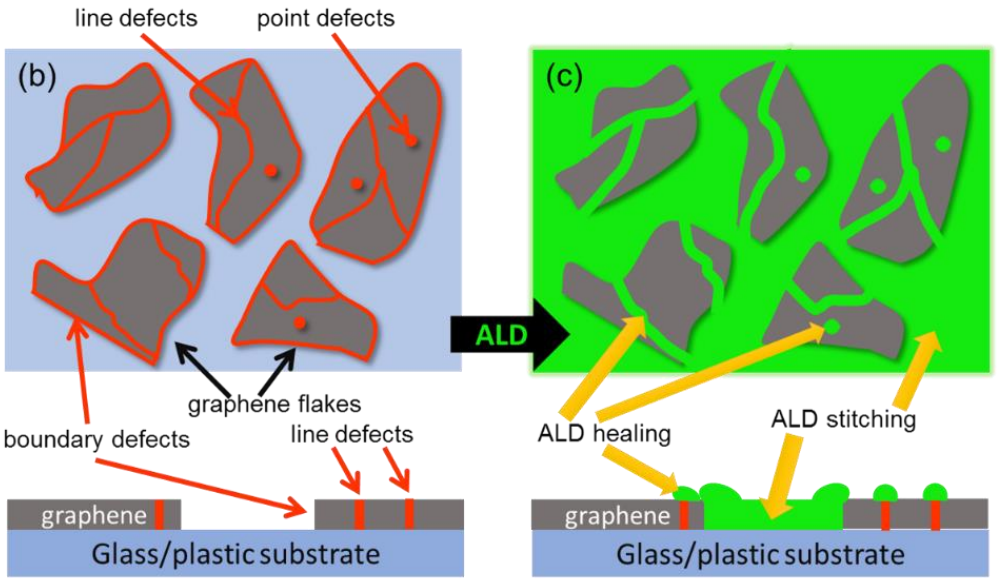


Figure 44(a) Selective ALD growth on substrate and graphene step edges. (b) Separated graphene flakes on substrate, with red indicating line and point defects within graphene flakes, and

boundary defects at graphene flake periphery. (c) Selective ALD provides conducting paths to heal point and line defects and to stitch flakes together while connecting at flake boundaries.

By exploring several conductive material ALD processes, including AZO, Ru and Pt, we investigate the chemistry of ALD on pristine graphene and defect sites, which defines selectivity and therefore spatial distribution of the growth. All these materials show significant selectivity on graphene edges and defects compared to clean graphene basal planes. Moreover, we also use the Pt ALD process to demonstrate a novel nano-manufacturing strategy to improve graphene thin film conductivity. To be specific, Pt is selectively deposited at flake peripheral boundaries, thus stitching nearby graphene flakes together electrically, and over possible point and line defects in graphene flakes, thus healing the defects (Figure 44). Therefore, by combining graphene flake assembly with ALD healing and stitching, we produce conductive paths around and across the electrical defects so that the benefits of the pristine graphene regions are realized.

8.4.1. Experimental methods

Graphene FET fabrication —To fabricate the graphene FET device, we spin-coated around 200nm Poly (methyl methacrylate) (PMMA) on a Si wafer with 300nm thermal oxide layer, then exfoliated graphene sheets from Kish graphite [100] on the PMMA coated wafer. With the assistance of alignment windows on shadow mask, the graphene flake was carefully aligned to the shadow mask using a micromanipulator stage. After that, 50nm Au electrode was deposited on top of the graphene flake in a Metra thermal evaporator.

Self-assembled graphene film preparation — The graphene flake films measured in this study were self-assembled using a previously published technique[101]. A solution

of exfoliated graphene flakes suspended in NMP was injected into a petri dish containing 40mL of DI water with a layer of 4mL of ethyl acetate floating on the surface of the water. The assembly of the loosely connected monolayer of graphene flakes was driven by desolvation from the NMP as well as convective plumes in the water created by the evaporation of the NMP. The glass substrates were coated by simple dip coating and dried in an oven at 120C for several hours.

Atomic layer deposition — Pt ALD process using trimethyl(methylcyclopentadienyl)platinum(IV) ($MeCpPtMe_3$) and O_2 at 270°C were carried out in a Cambridge Nanotech Fiji F200 with 1s $MeCpPtMe_3$ pulse time and 10s O_2 expose time at flow rate of 200sccm. The growth rate on Al_2O_3 and native Silicon oxide surface is ~ 0.4 Å/cycle. AZO thin films were deposited at 150 °C using a BENEQ TFS-500 ALD viscous-flow reactor. Diethyl zinc (DEZ, $Zn(C_2H_5)_2$) and distilled (DI) water were used as precursors to deposit ZnO films at a growth of 2 Å/cycle. Trimethyl aluminum (TMA, $Al(CH_3)_3$) and DI water were used as precursors at 150 °C for preparing ALD-Al_2O_3 films with growth rate of 1 Å /cycle. Pulse times for TMA and DI water cycles were 250 ms. One TMA-DI water cycle was inserted after a 20 DEZ-DI water cycles to achieve 3.0 at. % Al doping into ZnO film, which is reported to have the best electrical conductivity. [102]

Materials characterization — Surface morphology of exfoliated graphene flakes is imaged by tapping-mode AFM (NTEGRA Spectra, NT-MDT Co., Russia) with Au coated Si tips (NSG10, 3.1-37.6 N/m, 140-390 kHz). Scanning electron microscopy (SEM) characterization was conducted using a Hitachi SU-70 analytical SEM with EDX capability. High resolution transmission electron microscope (TEM) images of graphene

were captured by a JEOL JEM-2100 LaB6 TEM. The electrical properties of the thin films were measured using 4-point probe method by a Keithly 2400. Graphene FET was characterized using a probe station under vacuum.

8.4.2. Selective ALD growth on exfoliated graphene flakes

Pristine few layer graphene flakes are prepared on clean Si wafer (university wafer) by mechanical exfoliation of Kish graphite [100]. Before ALD process, we inspect the as-prepared graphene surface by AFM to confirm that the initial surface has clean basal plane and well defined step edges (Figure 45a). Height profile (Figure 45b) is measured along the green line marked in Figure 45a, presenting two steps with 10.3 nm and 2.9 nm in height, respectively. SEM image in Figure 45c also displays clear step edges, which is further confirmed by the stepwise EDS line scan profile of carbon signal.

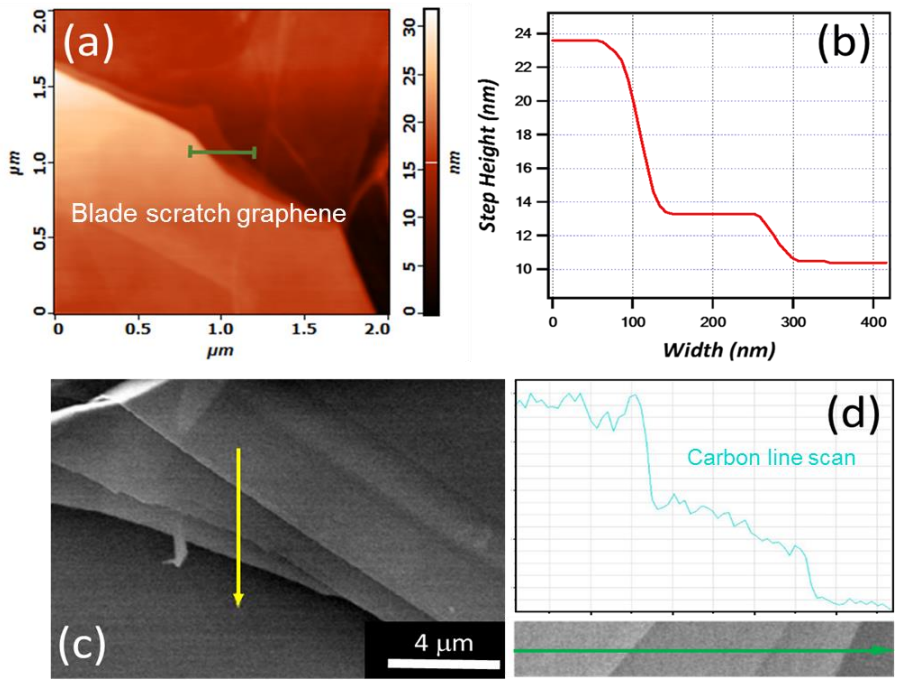


Figure 45 Morphology of as-prepared graphene surface. (a) AFM image and (b) height profile along the guide line shown in (a); (c) SEM image and (d) EDS-line scan for element C, Ru, O along the scan guide line (yellow arrow) in (c).

For the first time, we demonstrate selective growth of transparent conductor AZO on exfoliated graphene on Si wafer. As displayed in Figure 46 a and b, AZO grows at Si wafer, graphene step edges and possible defects and cracks, while pristine graphene basal planes are intact after AZO ALD process. EDS elemental mapping also confirms selective AZO growth (Figure 46 c and d). Zn signal matches with the shape of AZO grown on defects/cracks exactly though Al signal exhibit a more random distribution, which can be explained by low Al concentration and interference from high background signal.

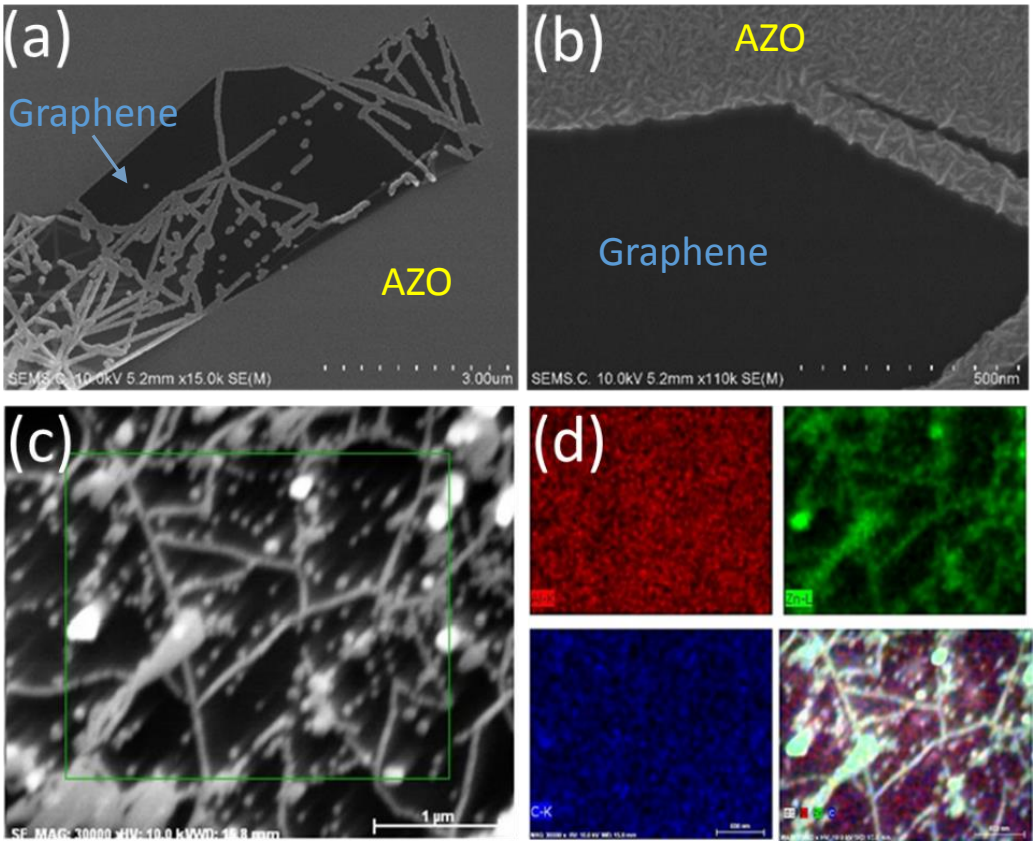


Figure 46 Selective ALD-AZO on pristine graphene flakes. (a-c) SEM images and (d) EDS elemental mapping of the sample area marked in (c).

Ru also shows distinctive selectivity on graphene edges and defects. As presented in Figure 47a, and b, after 150 ALD cycles Ru forms distinct nucleation islands on the graphene basal planes and line shape growth along the edges, which is further approved by Ru EDS line scan. Obvious Ru signal is detected at the graphene step edge (Figure 47d) compared to the background signal before ALD (Figure 45d).

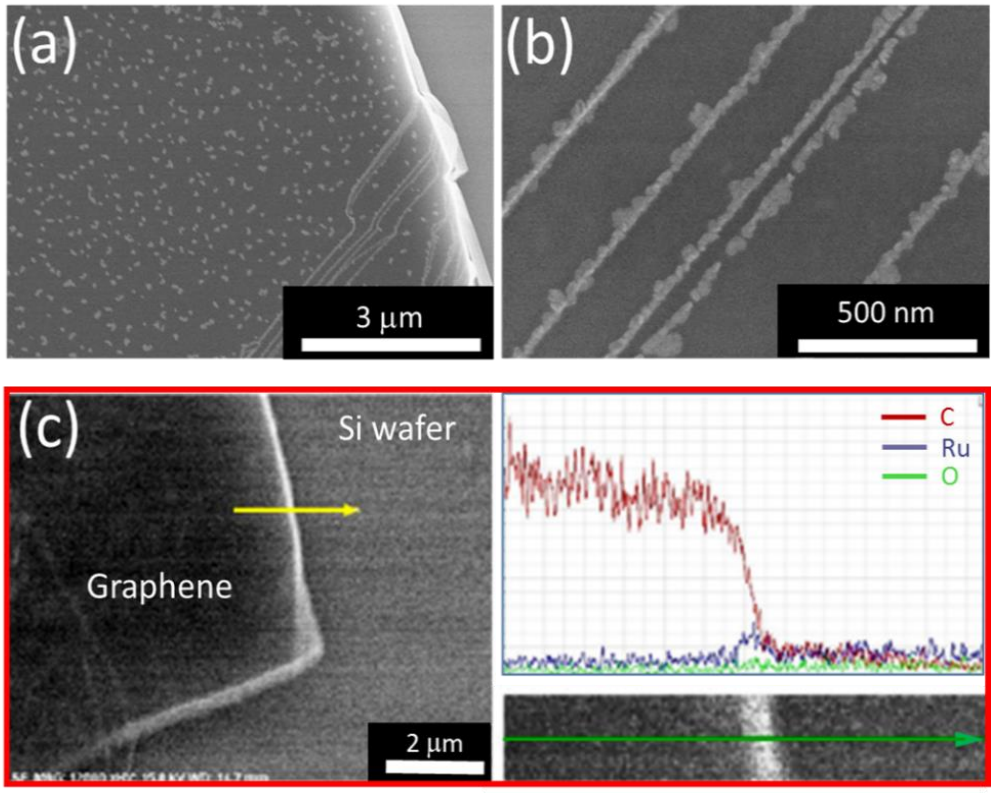


Figure 47 Selective ALD Ru growth on graphene. (a, b) SEM images of graphene after 150 cycles of ALD-Ru. (c) EDS line scan profile of ALD-Ru deposited graphene on Si substrate, for element C, Ru, and O along the scan guide line across the graphene step edge in figure c.

Similar selective growth for Pt is also demonstrated in Figure 48. Apparent Pt nucleation islands form on certain positions on the graphene basal plane, indicating possible defects underneath. Pt nucleation along graphene edges provides a conduction

path from the graphene flake to the continuous Pt film deposited in the same ALD process on Si substrate. Pt particle nucleation density is higher around the graphene step edge than on the basal plane. Noticeable growth is also observed on wrinkles, where extra stress accumulated at the folding may also facilitate the activation of carbon bonds at the graphene surface.

TEM also demonstrates preferential Pt growth at graphene step edges on a suspended CVD graphene fake. Pt particle nucleation density is higher around the graphene step edge than the basal plane. Noticeable growth is also observed on wrinkles, where extra stress accumulated at the folding may facilitate the activation of carbon bonds at graphene surface.

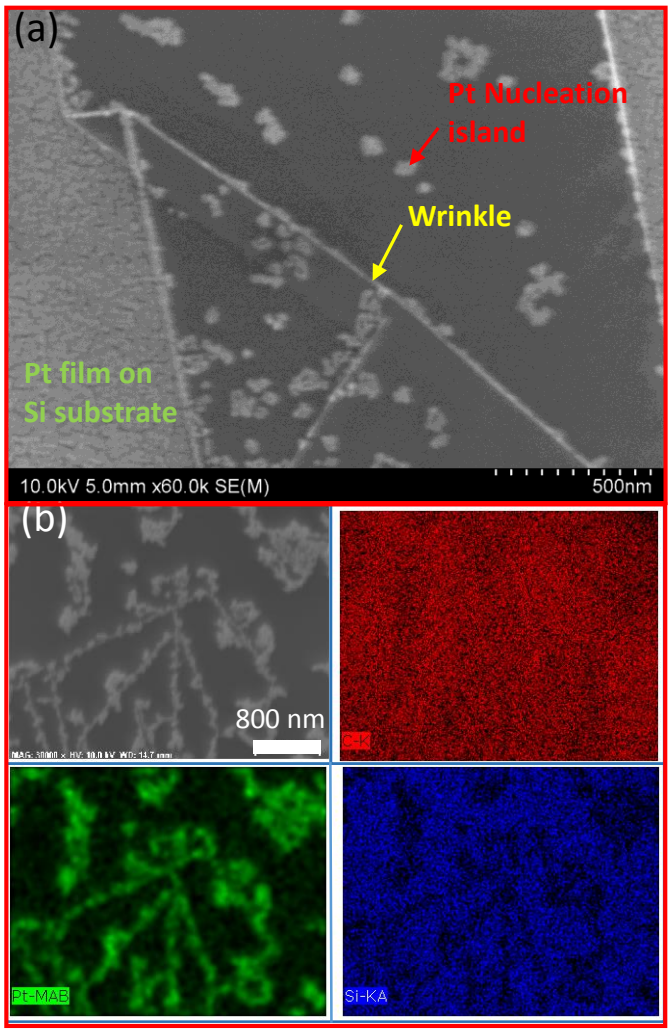


Figure 48 Selective ALD Pt growth on graphene. (a) SEM images of exfoliated graphene on Si wafer after 250 cycles of Pt. (b) EDS elemental mapping of Pt on graphene showing SEM (gray image in b), carbon (red), Pt (green) and Si (blue).

TEM also demonstrates preferential Pt growth at graphene step edges on a suspended CVD graphene flake. To further quantify the nucleation behavior of Pt, 90 cycles of ALD Pt with 60s exposure cycles were directly deposited on CVD graphene that had been transferred to a TEM grid. We observed that Pt nuclei are formed sporadically on the graphene flake, but with systematic statistical variation. For example higher Pt nuclei density develops near the step edge (as marked in Figure 49a) compared to that associated

with isolated defects on the graphene flake surface. Intensity line scan (Figure 49b) across the step edge indicates 5 layers of graphene at the step. In order to understand the substrate related ALD nucleation behavior, the TEM image is processed by Image J in step edge region (St), the upper-right basal plane region (B1) and the lower-left basal plane region (B2) as labeled in Figure 49 c. In both basal plane regions, Pt particles have similar density similar and area coverage, whereas the Pt particle density doubles within the step edge area, providing strong evidence for preferential ALD growth on graphene step edges (Figure 49d).

Considering the expense and feasibility in a manufacturing perspective, besides noble metals like Pt and Ru, various ALD processes for other earth abundant and cost effective metals and conductive compounds are worth further investigation, such as titanium nitride, nickel[69] and tungsten[67, 68].

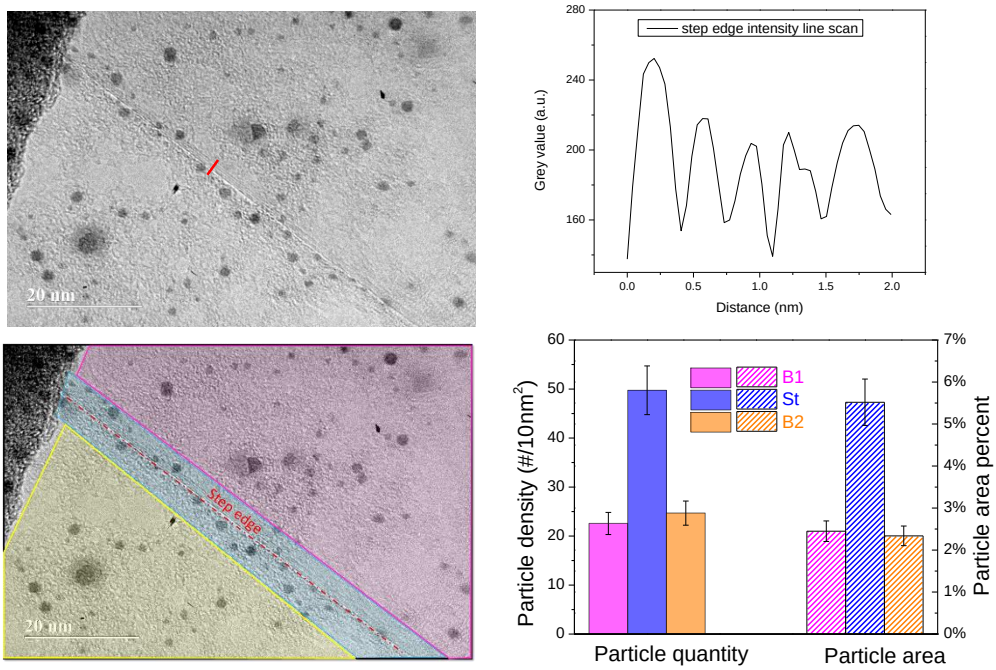


Figure 49 (a) TEM image of Pt particles nucleated on a CVD graphene flake (scale bars 20nm). (b) Intensity line scan across graphene step edge (shown as red line in (a)). (c) Basal plane regions B1 and B2 and step edge region between then on a graphene flake. (d) Particle number and particle area percentage in graphene basal plane and step edge area corresponding to Fig(c).

8.4.3. Improving conductivity of an individual graphene flake

Using previous described graphene flakes as a model system, we investigate how ALD Pt may benefit the conductivity of an individual graphene flake. In order to measure the electrical properties of a single graphene flake, we fabricate a graphene FET using a lithography-free technique[103] to pattern electrodes on exfoliated graphene flakes by shadow mask, which can avoid surface contamination from photo or e-beam resist, leaving a pristine graphene surface intact for selectivity investigation. Another major challenge is possible shorting of device electrodes after ALD process on common insulating oxide substrates (eg. SiO_2, Al_2O_3), which are –OH terminated and reactive to ALD precursors.

PMMA films has shown growth-inhibiting behavior for various noble metal processes and metal oxides.[104] Therefore, we spin coat a thin layer of PMMA onto SiO_2 substrate underneath the graphene flakes to prevent electrode shorting by ALD materials.

Using a two terminal measurement, source-drain current (I_{sd}) of the device is recorded between electrode 1 and 2 at room temperature with 10mV bias as a function of back gate voltage Vg, which controls the type and density of charge carriers. (Figure 50d) I_{sd} at V_g=0V increases after Pt ALD, showing conductivity improvement. The decrease of I_{sd}-V_g curve slope after the selective Pt ALD process indicates reduced electron mobility compared to pristine graphene, which is reasonable as Pt nano clusters may introduce more electron scattering. Besides, the Dirac point shifts from 12.6V to more than 25V, suggesting p-doping of the graphene from Pt, which can be explained by the high work function of Pt (6.35eV) compared to graphene (4.4eV) leading to electron transfer from graphene to Pt. As the gate voltage is swept from negative to positive and backwards, a pronounced hysteresis behavior is observed, as designated by the arrows denoting the sweeping direction. It may originate from charge transfer between graphene and Pt nano particles or charge injection into trap sites on the PMMA dielectric substrate.

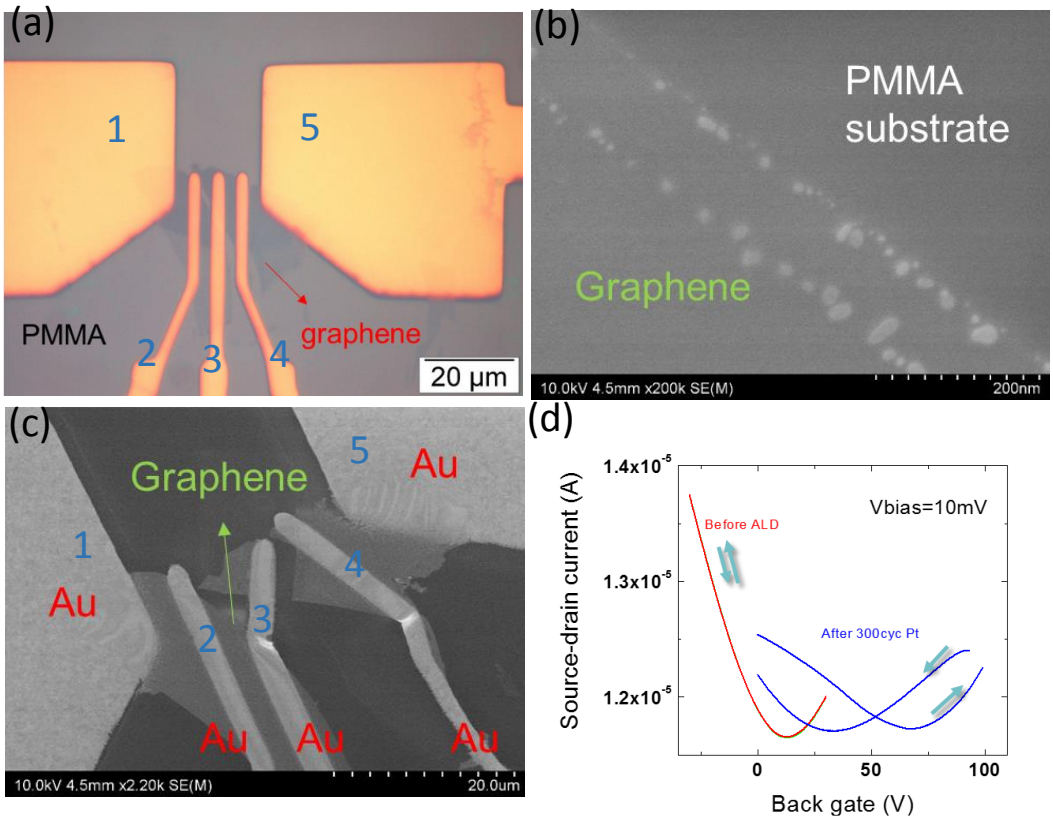


Figure 50(a) Optical image of transistor made from pristine exfoliated graphene on PMMA coated SiO2, with 5 Au electrodes. (b) SEM image of graphene after 300 Pt ALD cycles, showing selective growth at graphene step edges. (c) Electrode 3 and 4 curved after Pt ALD process. (d) Source-drain current vs. back gate voltage between electrode 1 and 2.

8.4.4. Introduction of p-doping to graphene by ALD vanadium pentoxide (V_2O_5)

ALD can also improve graphene conductivity by causing doping of the graphene. ALD V_2O_5 is a good candidate to introduce such p-doping considering its high work function (WF=7.0eV)[105] compared to graphene (around 4.6eV)[106]. In addition, V_2O_5 thin film has higher optical transmittance than a metal film like Pt, which will potentially benefit the optical properties of the graphene/V_2O_5 hybrid system. Using the lithography-free technique reported in 2nd year annual report, we fabricated a graphene FET with

patterned electrodes on exfoliated graphene flakes using a shadow mask to avoid any contamination from photo/ebeam resist during the fabrication process. The Raman spectrum corresponding to the graphene flaks I Fig. 4a shows a G band around 1593 cm^{-1} and a 2D band at 2652 cm^{-1} „ Almost no signal was observed in the region of the graphene D band, indicating that the graphene is monolayer thickness (Figure 51b). The ALD V_2O_5 deposits on Au electrodes and SiO_2 substrate, while it nucleates on graphene surface without forming a continuous film (Figure 51c and d).

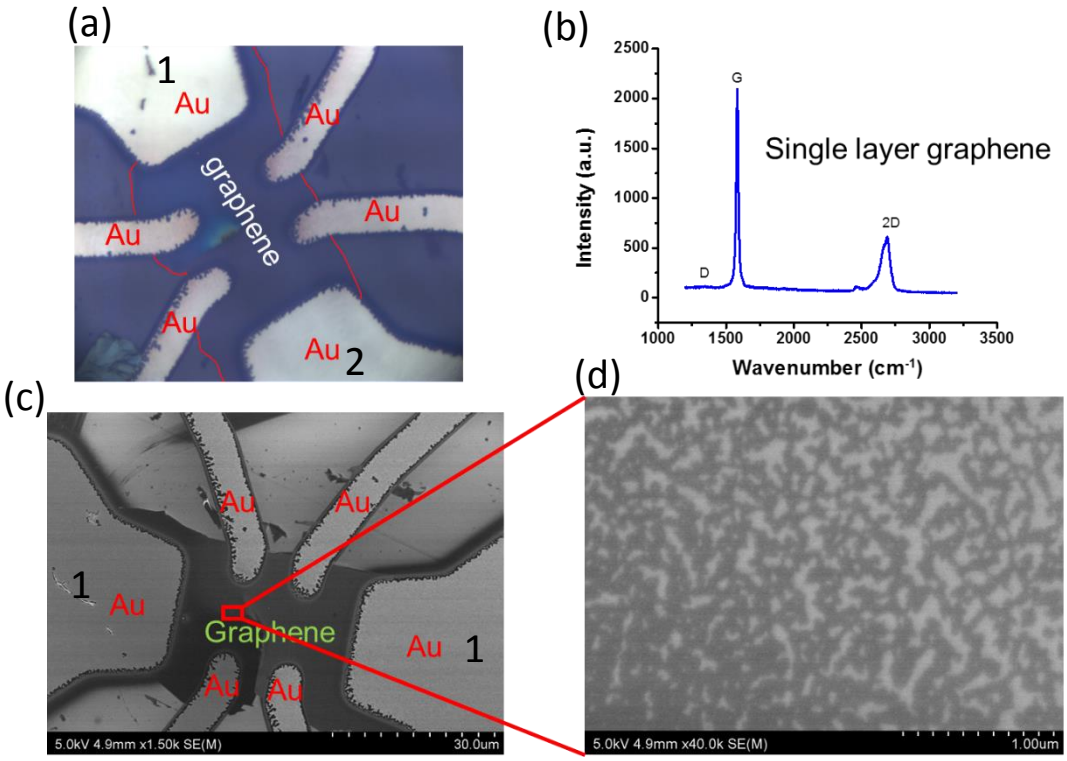


Figure 51. Graphene FET after 200 cycles of ALD V_2O_5 which dopes the graphene. (a) Optical image of transistor made from pristine exfoliated graphene Au electrodes. (b) Raman spectrum indicates single layer graphene. (c) SEM image of graphene after 200 V_2O_5 ALD cycles. (d) Zoom-in image of graphene surface showing V_2O_5 nucleation.

The source-drain current (I_{sd}) of the device was recorded between with 10mV applied between electrodes 1 and 2 (Fig. 4a) at room temperature as a function of back gate

voltage Vg (Figure 52). At zero gate voltage, subjecting the graphene flake to 200 cycles of ALD V_2O_5 doping almost doubles the graphene conductance (Figure 52b) - a considerable conductivity improvement. The slopes of the I-V curves for 100 and 200 cycles of V_2O_5 doping are nearly identical, which indicates that the electron mobility is not affected by the V_2O_5 doping level. The current device configuration uses 200nm SiO_2 as the dielectric layer. Due to the heavy doping from V_2O_5, the Dirac point has moved towards positive direction largely (>60V) after V_2O_5, as indicated in Figure 52b. Such high gating voltage is located in a region where the device is under the risk of dielectric layer break down and graphene damage. To further quantify the doping effect of V_2O_5, more systematic measurement need be done in the future using thinner dielectric layer with higher dielectric constant, eg. ALD grown 100nm Al_2O_3. In addition, it is important to compare the transmittance between pristine and V_2O_5-doped graphene.

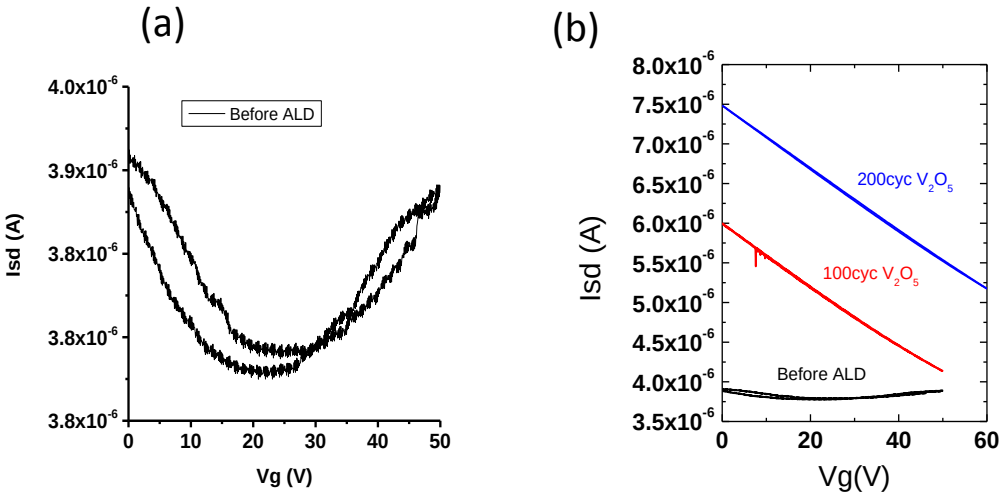


Figure 52 Source-drain current vs. back gate voltage for (a) pristine and (b) V_2O_5-doped graphene flake with 100 and 200 ALD cycles

8.4.5. Electrically connecting separated graphene flakes

Graphene flakes prepared by blading method have intrinsically pristine and clean surface and relatively large flake area, providing an excellent platform for fundamental study. While large area production of graphene films could be enabled by solution method for measuring sheet resistance variation with different ALD cycle numbers. Using Pt ALD on graphene as a model system, we demonstrate electrically stitching disconnected graphene flakes and healing defects on each flake. The ability to heal self-assembled films of solution-processed graphene flakes is important because of the ease and scalability of this technique in contrast to the synthesis and transfer of CVD graphene. Figure 53 a and b illustrate that Pt selectively nucleates on graphene edges and defects and provide electrical pathways around and across them, while Pt on glass substrate creates a conducting network connecting detached graphene flakes. The graphene basal plane is hydrophobic and inert, whereas dangling bonds at the periphery of the graphene flakes are more reactive, particularly to ligands on the ALD precursors (e.g., -CH3, -OH and -COOH), driving dissociative precursor chemisorption at the graphene edge sites to accomplish selective deposition at defects.

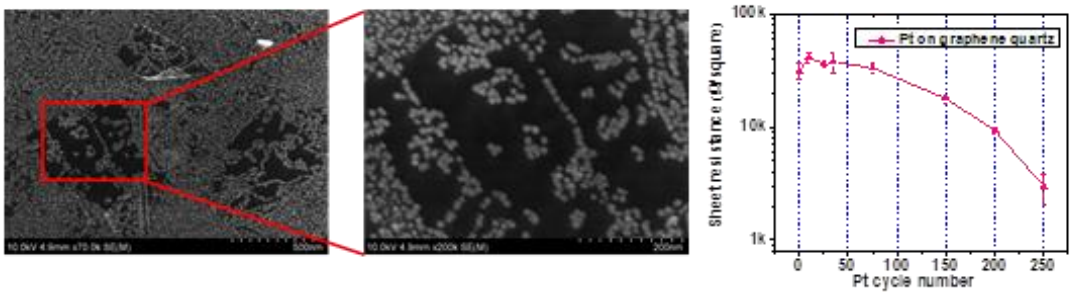


Figure 53 Pt ALD improves electrical properties of graphene flake thin film. (a) Separated graphene connected by Pt deposited on quartz substrate. (b) Zoomed-in image of one graphene flake in (b), showing Pt selective growth on defects and edges. (c) Sheet resistance of graphene decreases with respect to different ALD cycles.

Given the anticipated high cost of Pt as an ALD stitching/healing layer for graphene, we have investigated ALD Al-doped ZnO (AZO) for its substantially lower cost and the earth abundance of its constituents. Low conductivity CVD graphene on a quartz substrate was used as a demonstration, having been scratched and damaged to produce a high sheet resistance (i.e., low conductivity). 18 super cycles of AZO improve the graphene sheet resistance by 10X, while a similar ALD AZO film on bare quartz without graphene (as a control)shows poor conductivity (Figure 54).

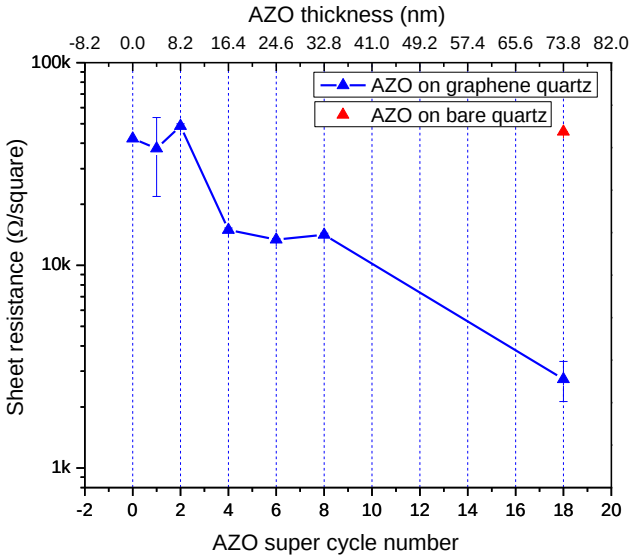


Figure 54 AZO improves conductivity of a low conductivity scratched CVD graphene

In summary, we have demonstrated selective ALD growth on graphene defects and boundaries with various ALD processes for conductive materials (AZO, Ru and Pt). Conductivity improvement and doping effect from Pt ALD on a single graphene flake is demonstrated by a back-gated graphene FET. Selective ALD growth on structural defects

present on graphene and over the blank area between graphene flakes leads to 10X conductivity of a graphene flake thin film. Selective ALD growth on graphene edges and defects shows clear evidence for nucleation dependence on available surface groups. Selectively deposition of ultrathin conducting coatings over point and line defects in graphene flakes heals the structural defects present on graphene. As a result, we can produce conductive pathways around and across the electrical defects sufficiently that the benefits of the pristine graphene regions are realized.

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