

ABSTRACT

Title of Document: A PHYSICS OF FAILURE BASED
QUALIFICATION PROCESS FOR FLEXIBLE
DISPLAY INTERCONNECT MATERIALS.

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The next paradigm shift in display technology involves making them flexible, bringing with it many challenges with respect to product reliability. To compound the problem, industry is continuously introducing novel materials and experimenting with device geometries to improve flexibility and optical performance. Hence, a method to rapidly qualify these new designs for high reliability applications is imperative.

This dissertation involves the development of a qualification process for gate line interconnects used in flexible displays. The process starts with the observed failure mode of permanent horizontal lines in the displays, followed by the identification of the underlying failure mechanism. Finite element analyses are developed to determine the relationship between the physical flexing and the mechanical stress imposed on the traces. The design of an accelerated life test is performed based on the known

agent of failure being cyclic bending that induces a tensile strain. A versatile dedicated test system is designed and integrated in order to rapidly capture changes in resistance of multiple traces during test. Dedicated test structures are also designed and fabricated to facilitate in-situ electrical measurements and direct observations.

Since the test structures were consumed during the integration of the test system, random failure times are used in the process of determining a life-stress model. Different models are compared with respect to their applicability to the underlying failure mechanism as well as parameter estimation techniques.

This methodology may be applied towards the rapid qualification of other novel materials, process conditions, and device geometries prior to their widespread use in future display systems.

A PHYSICS OF FAILURE BASED QUALIFICATION PROCESS FOR FLEXIBLE
DISPLAY INTERCONNECT MATERIALS

By

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Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
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Dedication

I would like to dedicate this to my family. First and foremost, my wife Mindy – without your understanding and support this would not have been possible. To my daughter Jennifer – I hope this inspires you to never give up. To my parents – for giving me a solid foundation to become a man and staying alive to see this day. To my brother, my two sisters, my nieces and nephews, and my close friends – I am thankful that you are all an integral part of my life. I know this was a long time coming, but I had to fight the good fight and here we are.

As thanks, I hope that none of you are ever required to read this document.

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Chapter 1: Introduction

1. Overview

The evolution of display technology has seen significant strides over the past 100 years. Starting from the initial black and white cathode ray tubes the technology was relatively stagnant until the Active Matrix Liquid Crystal Displays (AMLCD) that started in the 1980s. Then next major paradigm shift in displays is in making them flexible so as to open up entire new avenues for applications that have yet to be considered. Along with this new shift in display technology comes with it significant hurdles with respect to reliability.

The follow sections start with a general background to displays and continue through the process of identifying the failure mode to be investigated and concluding with the contribution of this work. Sections 1.1 and 1.2 provide a history of display technologies from its humble black and white beginnings to the most recent technologies that are enabling the transition to flexible displays. A detailed theory of operation of the specific flexible display that is under study for this investigation is provided in section 1.3. Sections 1.4 and 1.5 discuss the field use conditions unique to flexible displays and the resulting failures as observed by the end users. An analysis of the failure modes that underlie these conditions is performed in section 1.6 as well as the identification of the one failure mode relevant to this investigation is given in section 1.7. A circuit model is used to simulate the performance of the display in order to determine the failure threshold (section 1.8). This chapter concludes with a

formal statement of the problem followed by the motivation and contribution of this thesis, sections 1.9 and 1.10 respectively.

1.1. History of Display Technologies

There have been numerous display technologies over the years; however the following sub-sections shall highlight the most prominent technologies to include the cathode ray tube and the liquid crystal display.

1.1.1. Cathode Ray Tube

The cathode ray tube is the oldest display technology. It was first proposed in 1908 and by January 1926 a mechanical version called a “televisor” was demonstrated [Campbell-Swinton 1908]. By the mid 1930s, manufacturers developed screens with 343 lines of data presented at 30 frames per second. The image is generated by controlling the luminance of a matrix of pixels (the smallest element in a display image). These pixels are arranged in a series of rows and columns on the surface of a screen as shown in Figure 1.1.1-1 from University of Colorado Physics 2000 website.

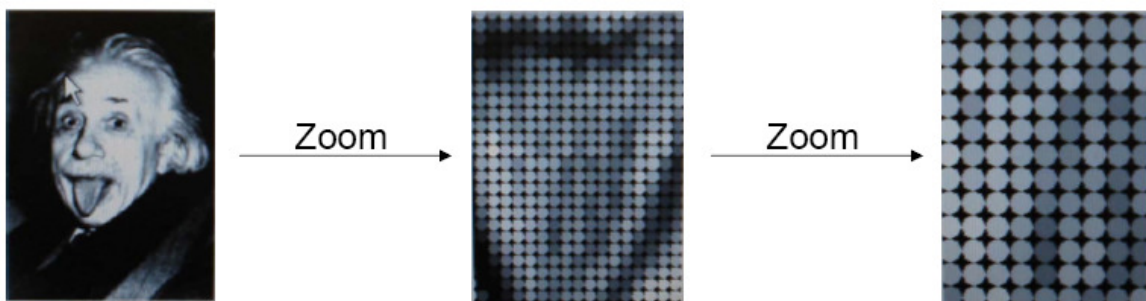


Figure 1.1.1-1 Breakdown of an image on a CRT display

With the advent of color, each pixel is made up of three sub-pixels (red, green, and blue) the combination of intensity for each sub-pixel determines the overall color spectrum for that pixel. A CRT is made up of a vacuum tube with three electron guns (one for each color) at the rear or cathode end of the tube. A high voltage (anode) is placed at the display face of the CRT for accelerating the electrons from the three guns. The beam passes through a series of magnetics (yokes) which deflect the beam both horizontally and vertically onto the display surface as show in Figure 1.1.1-2.

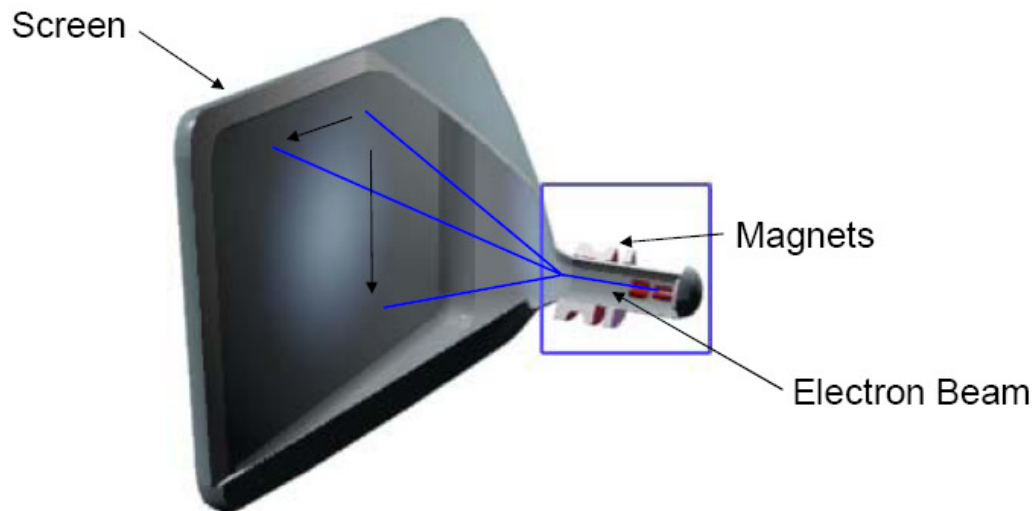


Figure 1.1.1-2 Cross section of cathode ray tube

A shadow mask is used to align the beam from the red gun to only hit red sub-pixels, likewise for green and blue pixels as evident in *Figure 1.1.1-3*. When the beam strikes the sub-pixel the phosphor is illuminated in that particular color – the higher the current, the brighter it glows. The beam continues scanning the screen and by the time the phosphor intensity starts to fall off, the beam has already scanned the rest of the display and strikes the sub-pixel again. The observer of the display sees the image due to a property of our eyes called persistence of vision.

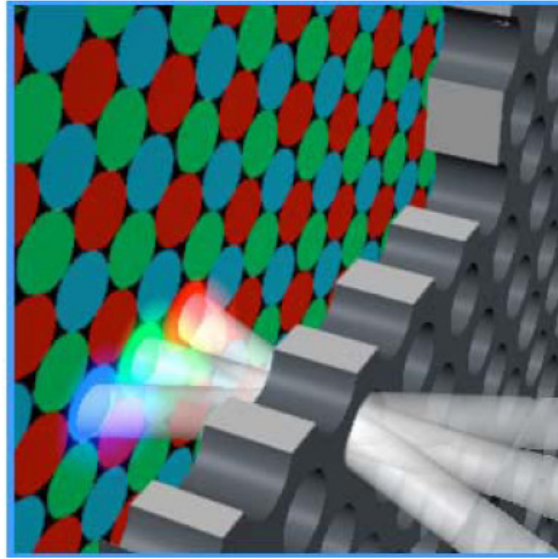


Figure 1.1.1-3 Shadow mask of cathode ray tube

The positive attributes of a CRT are high color saturation, wide viewing angle, low manufacturing cost, and reliability. The negative attributes include poor focus, amount of required mounting depth, and weight of the end item product. The liquid crystal display was the next major shift in display technology that targeted the mounting depth and weight problems of the CRT.

1.1.2. Liquid Crystal Displays

The term liquid crystal refers to a state of matter that has properties of both a liquid and a solid. In 1963, RCA discovered that light passing through a liquid crystal is affected by an electric field [Williams 1963]. By 1968, RCA made the first display device that leveraged this new technology [Heilmeyer 1968].

An LCD uses a similar premise for a color perception technology as the CRT in that the screen is made up of a matrix of sub-pixels (red, green, and blue). Instead of a cathode ray, each pixel is uniquely addressed by row and column drives that apply a voltage to the gate of a thin film transistor for that particular sub-pixel. These transistors are routed on one surface of glass, which contain the gate and drain. The source (or third terminal of the transistor) is on a separate layer of glass spaced in close proximity to the gate-drain layer. A front and rear polarizer are included in the optical stack to rotate the light 90 degrees along with a backlight to provide the luminance as shown in Figure 1.1.2-1.

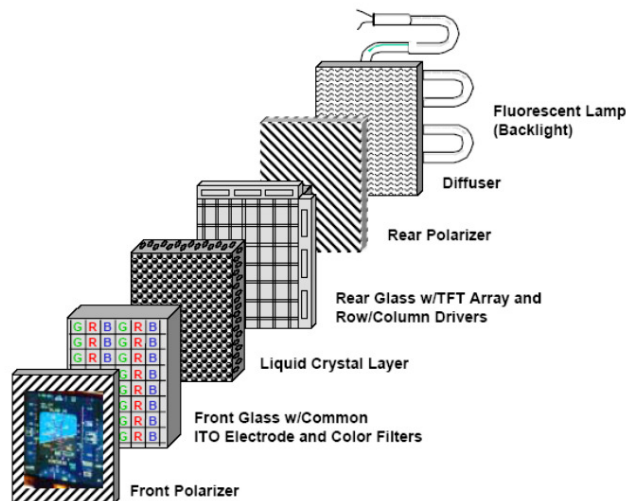


Figure 1.1.2-1 Optical stack up of an Active Matrix Liquid Crystal Display

Liquid crystal material is sandwiched between the two layers of glass. Liquid crystals are compounds with long, rod like molecules and in an unbiased state, the molecules arrange themselves in a loosely ordered fashion with their long axes parallel. When a

drive voltage is applied to the gate of a transistor, an electric field is produced between the source and drain and this field. This field causes the molecules to rearrange themselves vertically (in parallel with the field) and light is allowed to pass straight through.

Positive attributes of the AMLCD are sharpness, lightweight, and thin profile. The negative attributes are a narrow viewing area, moderate video response (due to the response time of the liquid itself), higher manufacturing costs, and lower brightness.

1.2. Advanced Display Technologies Enabling Flexibility

Flat panel displays have been in commercial use for decades. The technology involves the fabrication of thin film transistors on a glass substrate. In recent years, there has been a tremendous push to manufacture displays on flexible substrates. The benefits of this approach include the ability to lend themselves to roll-to-roll fabrication as well as impart flexibility into the end item product.

Recently there have been advances in display technology that are not only improving the performance but also enabling the possibility of making displays flexible. The following subsections highlight the most prominent advances over the past two decades with respect to three major types of Electro-Optic Materials

- **Emissive**
- **Reflective**
- **Transmissive**

1.2.1. Emissive Displays

Kodak first discovered organic materials that glowed in response to electrical currents in the late 1970's. Research continued through the 80's with the first efficient small-molecule OLED device being invented by Kodak in 1987 [Tang 1987 and Hack 2002]. The first color generated during this early research was green. By 1989, the Kodak research group demonstrated color improvements using fluorescent dyes, or dopants, to boost the efficiency and control of color output.

OLEDs are a fundamentally different technology from the CRT or AMLCD. An OLED is an electronic device similar in operation to a diode, but it is made by sandwiching a series of organic thin films between two conductors as reflected in Figure 1.2.1-1.

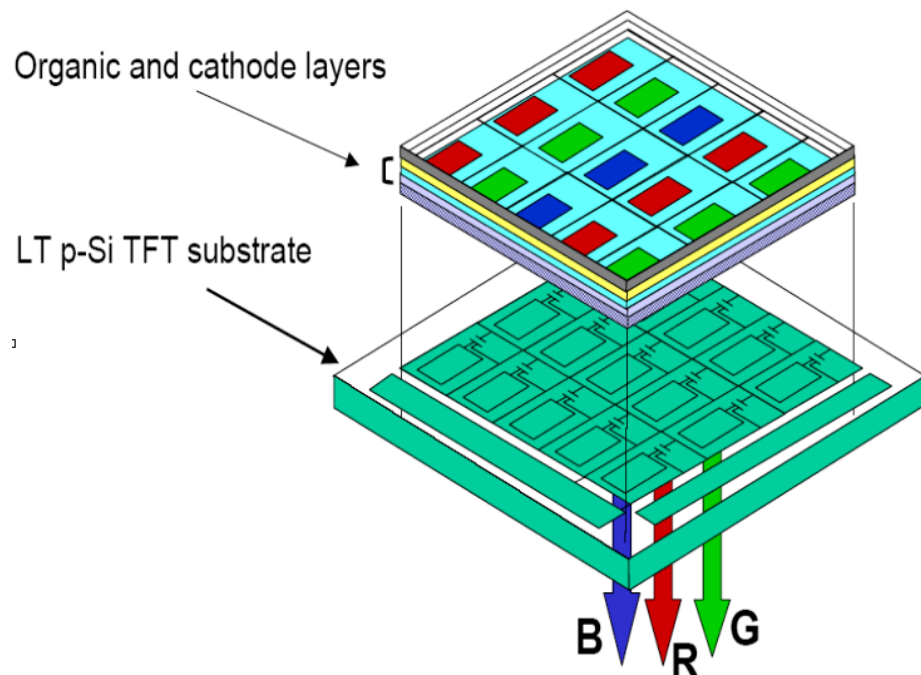


Figure 1.2.1-1 Cross section of Organic Light Emitting Device (OLED)

The operation of an OLED is much simpler than a cathode ray tube or an AMLCD. When a potential difference exists across the device, an electric current flows through the organic material and light is emitted. Figure 1.2.1-2 shows the operation of an OLED with current flowing from the cathode through the organic layers to the anode.

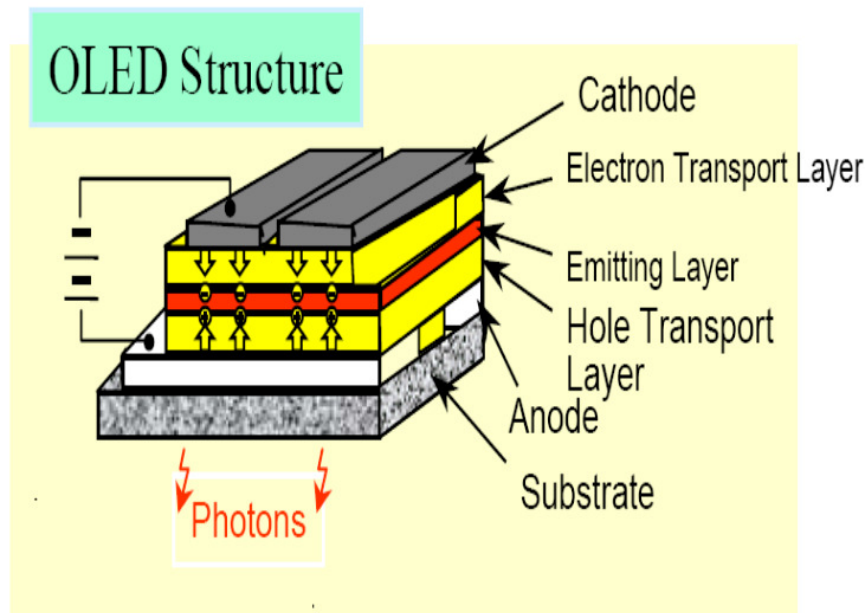


Figure 1.2.1-2 Operation of an Organic Light Emitting Device

OLED displays offer faster response time over LCDs (eliminates blurry images). This is due to an electric current driving the OLED versus a voltage driving the liquid crystal molecules (10 μ s versus 10ms). Wider viewing angle, higher contrast, higher brightness, better resolution, and lower power all make OLED displays very attractive to designers and consumers alike.

The reasons for the better performance lies in that OLEDs control the actual generation of light at the source level. An LCD's viewing angle is low due to the

optical characteristics of liquid crystal molecules varying depending upon the angle at which they are viewed. OLEDs emit at the source and spread the light uniformly in all directions to produce viewing angles similar to a CRT. LCD contrast limitations are based on the inability to control the passing of polarized light from 0% to 100%. OLED displays can achieve this based on precise control of the electric current passing through the pixel.

1.2.2. Reflective Displays

Under the heading of reflective display technologies, there are several types that lend themselves to the advent of flexibility to include polymer dispersed liquid crystals, cholesteric liquid crystals, bichromic ball composites, and encapsulated electrophoretics. Since the technology employed for this study involves encapsulated electrophoretics, most of the discussion shall cover this topic.

Electrophoresis is the translation of objects that are charged in a specific suspending dye fluid and their response to an electric field applied across that fluid. The objects are charged pigment particles contained in a thin film between electrodes. Optical contrast is obtained by moving the particles to either the top or bottom surface of the thin film as shown in Figure 1.2.2-1 [Dalisa 1977].

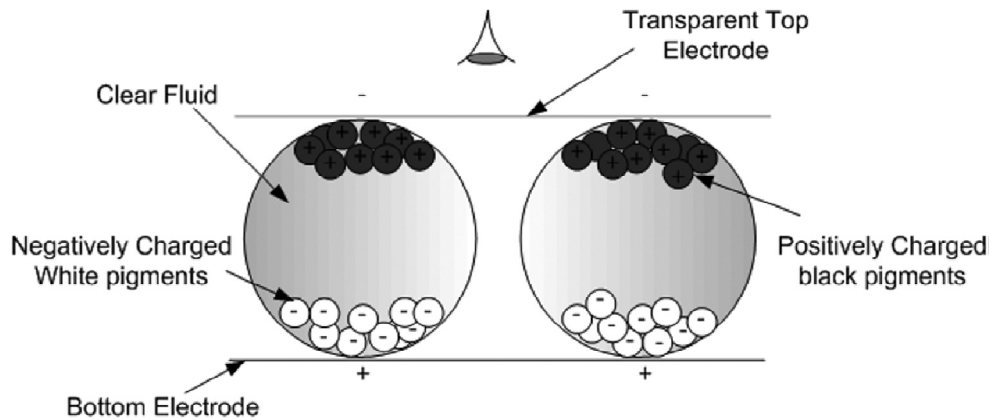


Figure 1.2.2-1 Cross section of Electrophoretic display

This technology lends itself to low power applications and sunlight readable since it uses ambient lighting to reflect back off the surface of the display. Figure 1.2.2-2 is an example of an electrophoretic display being used as electronic paper.

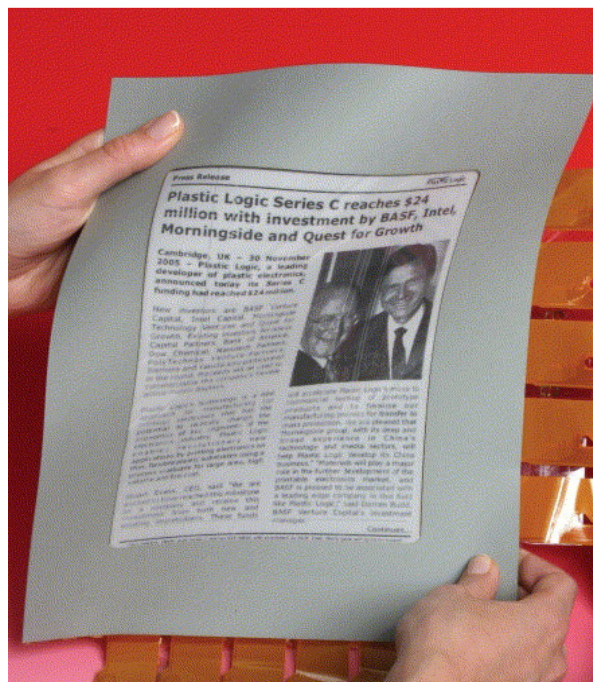


Figure 1.2.2-2 Electrophoretic display in an electronic paper application

1.2.3. Transmissive Displays

Liquid crystals are still the main choice for today's transmissive flat panel displays on glass substrates. Novel processes are being developed in order to paint liquid crystals onto flexible substrates. Detailed discussions on this topic are outside the scope of this research, but the main attributes of this approach involve photo enforced stratification [Quian 2000].

1.3. Theory of Operation

The following subsections provide a detailed discussion on the specific technologies employed for the flexible display used for this research. The topics include the basic fabrication steps, pixel design, the drive circuit, thin film transistor stack up, and the interconnects. Figure 1.3-1 is a picture taken of the end item product developed and manufactured at the Flexible Display Center (FDC) in Tempe, AZ a center sponsored by the Army Research Labs.



Figure 1.3-1 Picture of electrophoretic display manufactured by FDC

1.3.1. Basic Fabrication Steps

Figure 1.3.1-1 shows the cross section of the display. Since the fabrication of a flexible display requires unique processing steps, the following paragraphs provide a high level description of the fabrication sequences along with the terminology that shall be used throughout this document to ensure consistency since these terms are routinely interposed in industry.

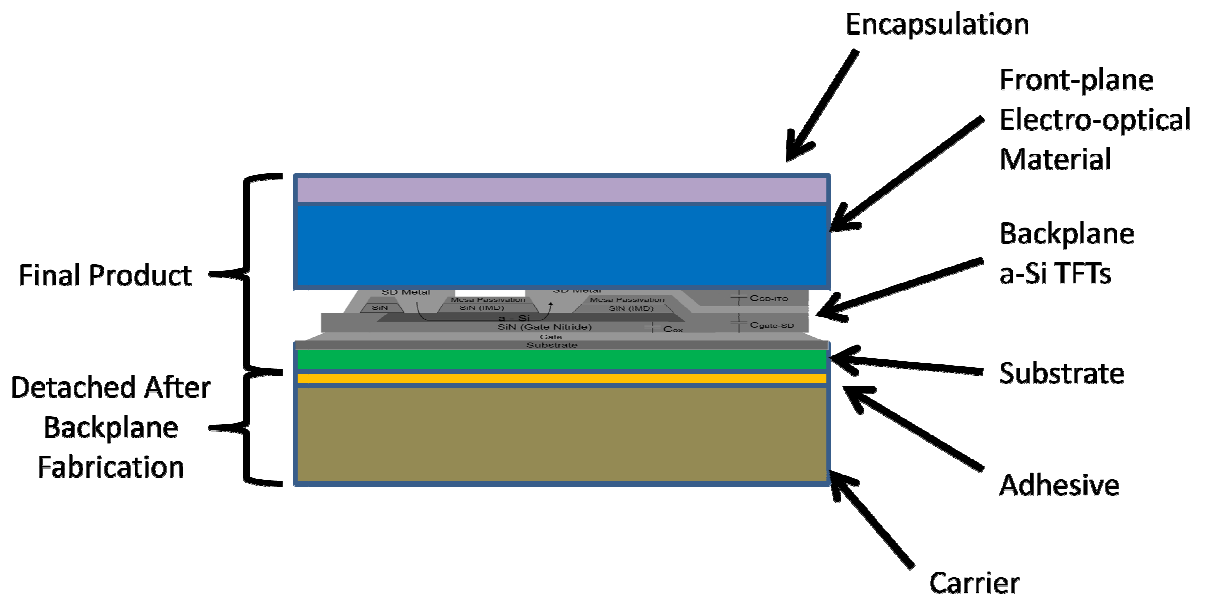


Figure 1.3.1-1 Cross section of Standard Flexible Display

Fabrication starts with a carrier to ensure stiffness and prevent bowing during the processing steps so that the geometries are maintained throughout manufacturing. The FDC has experimented with different carrier made out of different materials such as

Silicon and Aluminum, but for this research Aluminum was used as the carrier material.

The substrate is bonded to the carrier using a proprietary adhesive. The FDC has also experimented with different substrate materials. Initially, stainless steel was used and since then plastic substrates have been introduced such as Polyethylene Terephthalate (PET) and Polyethylene Naphthalate (PEN). The substrate material used for this research was PEN and more specifics of the material are provided in Chapter 2 of this thesis.

The backplane consists of the drive electronics that allow for the biasing of the electro-optical material (front-plane). On the backplane, an active matrix array of thin film transistors (TFT) are fabricated using amorphous Silicon (a-Si) as the main active material for the transistor. Specifics of the transistor composition are provided in section 1.3.4. The transistor controls the amount of voltage applied to an individual pixel element of the display and thereby controlling the response or how bright an individual pixel can be. Once the fabrication of the backplane electronics is complete, the need to maintain tight geometries is no longer pertinent and the substrate is debonded from the carrier.

The next step in the display fabrication is the application of the front-plane. Here the electro-optical (EO) material is deposited on the top surface of the backplane. Depending on the type of display (Emissive, Reflective, Transmissive) different electro-optical materials may be used. The most common materials used by the FDC are Electro-phoretic and organic semiconductor materials.

The cathode layer is applied to the top surface of the front plane in order to provide the ability to bias the EO material. In addition, the top surface of the display is encapsulated by a transparent material that prevents moisture ingress into the display since moisture has detrimental effects on the EO materials – especially if organic materials are used.

Figure 1.3.1-2 is a picture of the display fabricated on a stainless steel substrate instead of PEN that has been debonded from the carrier. The center of the wafer is the location of display with the electrophoretic material attached to the TFT backplane. Note that there are other test structures on the outlying areas of the wafer that will be cut out prior to final assembly of the display.

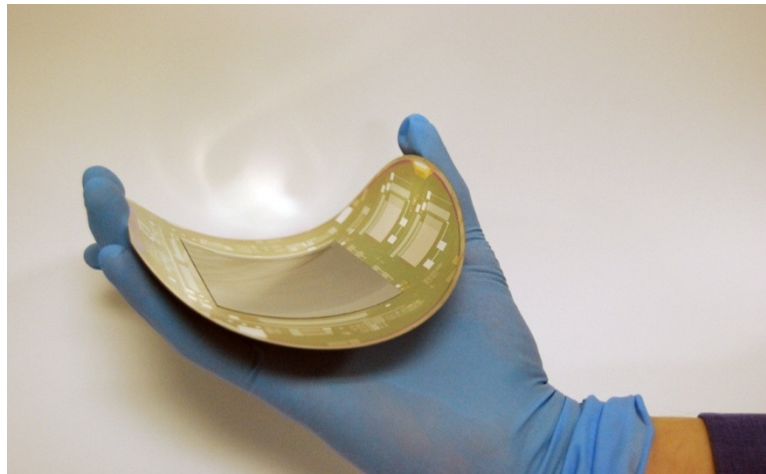


Figure 1.3.1-2 Photograph of display on stainless steel substrate

1.3.2. Electrical Operation of Display

The display is made up of an array of 320 x 240 pixels. Each pixel in the display is addressed in the matrix by row and column signals that represent gate and source connections of the drive transistor in the TFT backplane for each pixel as shown in

Figure 1.3.2-1. The drivers implement shift registers that increments the addressing of each row one at a time. Within a row time the source (column) drivers translate the image data and apply the appropriate voltage to each TFT.

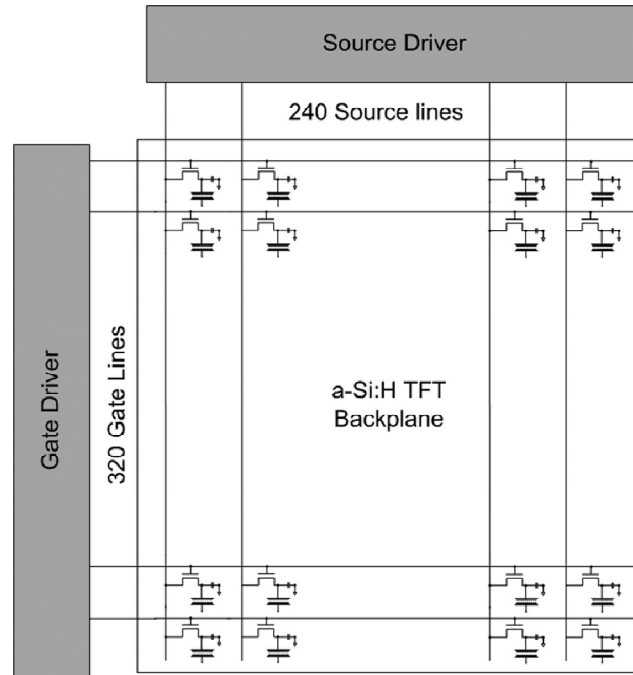


Figure 1.3.2-1 Schematic Diagram of gate/source (row/column) drive signals

1.3.3. Pixel Layout

A pixel is composed of two main elements. The first element is the individual pixel drive circuit, for this specific display type it is composed of one amorphous silicon thin film transistor (a-Si TFT). The second element of a pixel is the area dedicated to biasing the electro-optical material. Figure 1.3.3-1 represents the physical device geometry of the pixel using standard semiconductor deposition techniques. This figure identifies the gate line interconnects that are of specific interest in this investigation. Spacing between grid points is $10\mu\text{m}$, therefore the pixel dimensions are $240\mu\text{m} \times 240\mu\text{m}$.

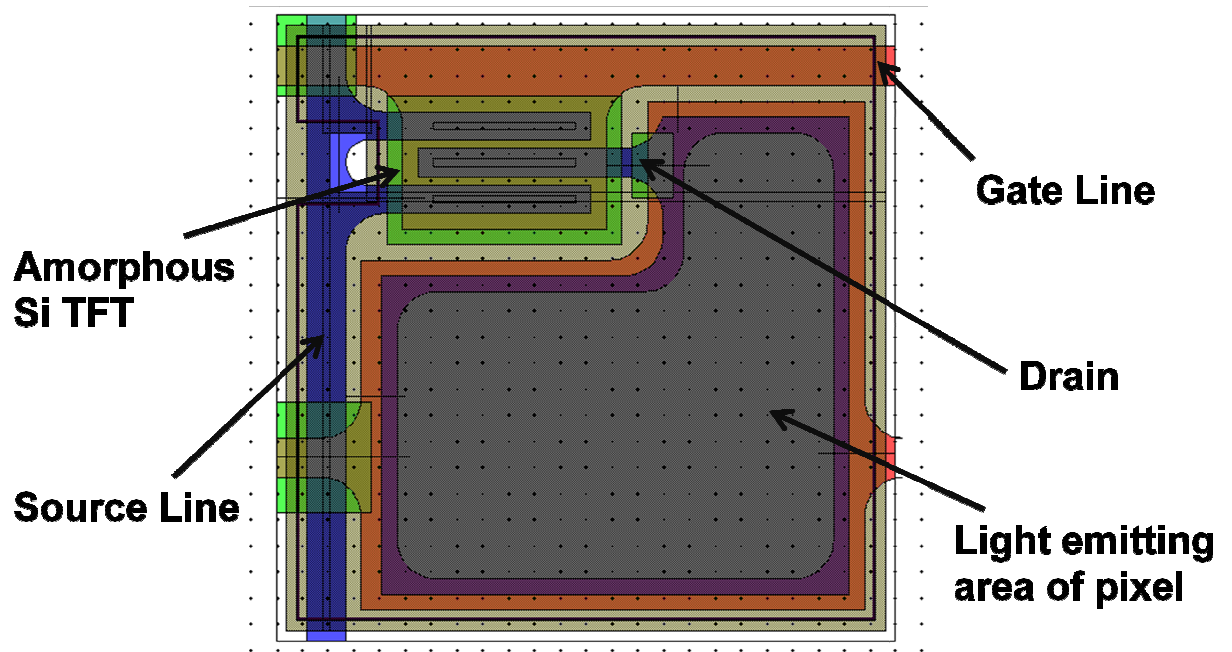


Figure 1.3.3-1 Diagram of one pixel

Operation of a pixel starts with a voltage applied to the gate of the thin film transistor which acts as a switch to transfer the image data (voltage) from the source line to the bottom electrode. The storage capacitor holds the voltage until the next frame of the image is loaded. This voltage is able to bias the electrophoretic material sandwiched between the bottom electrode and the top transparent electrode of the display as shown in Figure 1.3.3-2.

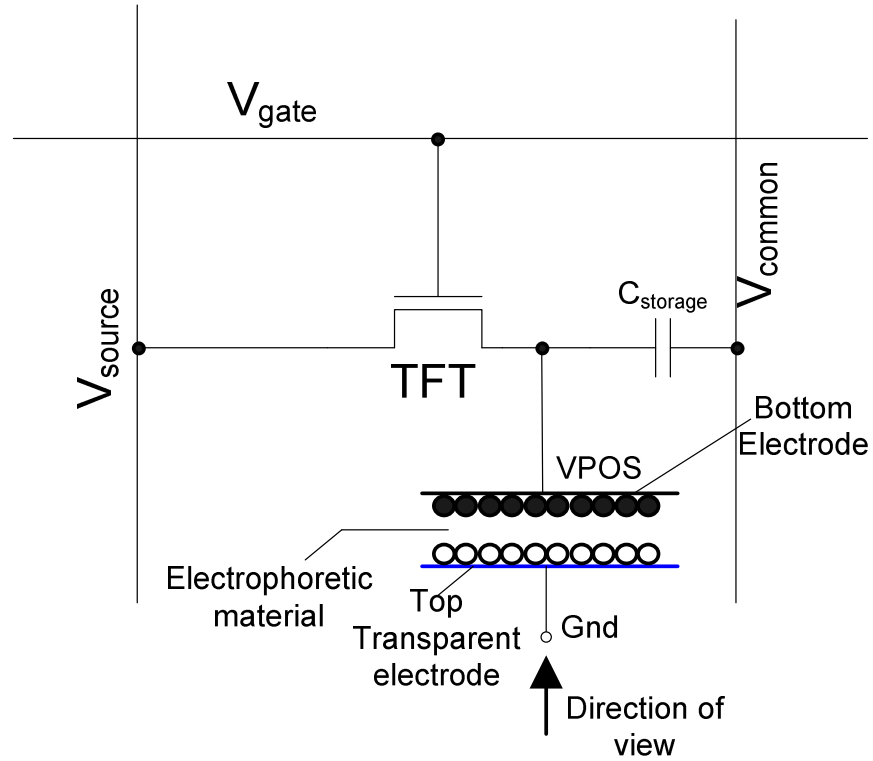


Figure 1.3.3-2 Schematic diagram of pixel

1.3.4. Thin Film Transistor

The amorphous Silicon thin film transistor is a bottom gate staggered structure. Figure 1.3.4-1 shows the cross section of the entire pixel with both the TFT on the left hand side and the light emitting area on the right hand side.

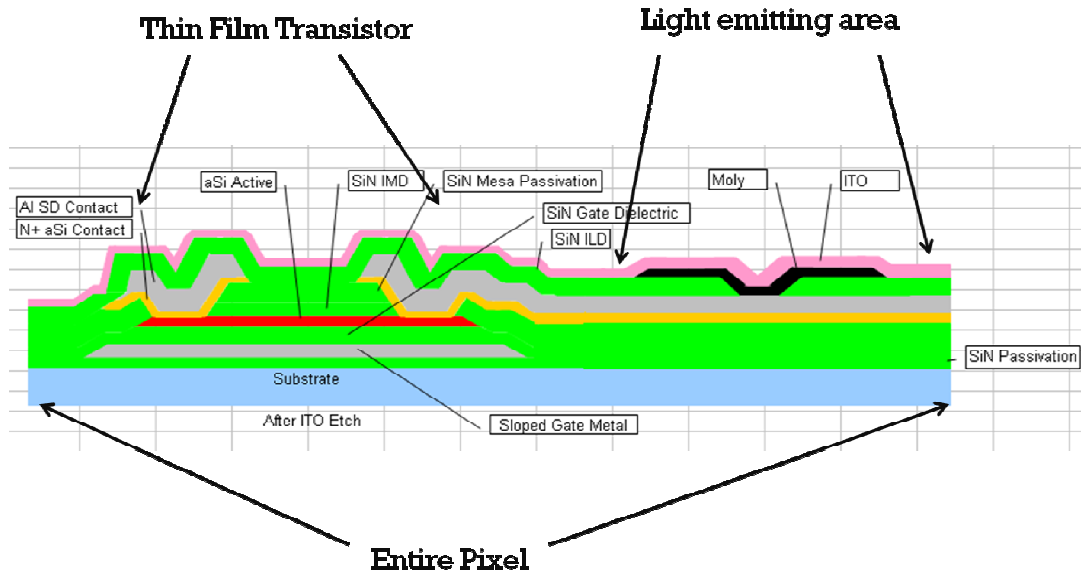


Figure 1.3.4-1 Cross section of entire pixel

A more detailed view of just the thin film transistor portion is provided in Figure 1.3.4-2. The fabrication process involves starting with a PEN substrate and patterning the gate metal. Three thin films are deposited (gate dielectric, a-Si:H, and back channel protection dielectric). The source and drain via openings are created by openings through the back channel protection dielectric to connect to the top metal. Next, the source/drain metal to include a low resistance n+ contact layer is deposited [Venugopal 2007].

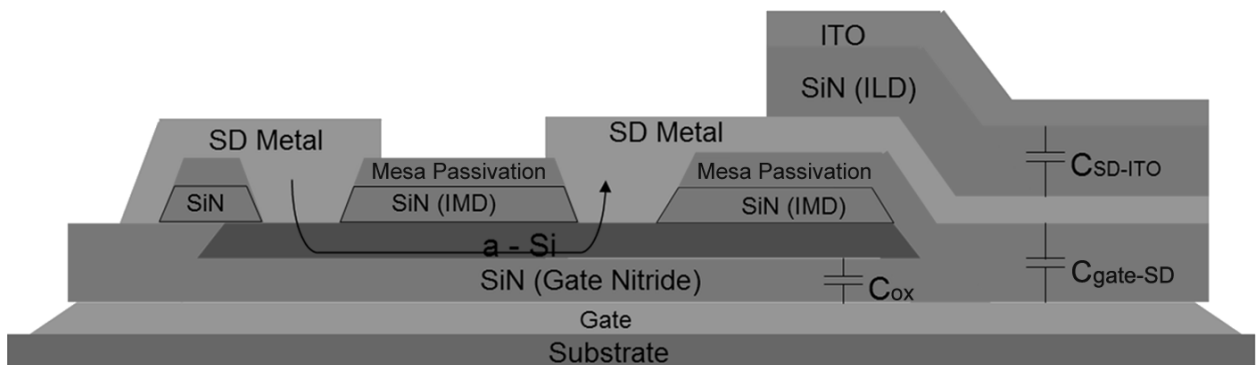


Figure 1.3.4-2 Detailed cross section of thin film transistor

1.3.5. Gate Line Interconnects

A DC magnetron sputtering system is used to deposit the gate material. Photo resist is spin coated on and then the gate layer mask is used for the exposure step. Figure 1.3.5-1 shows the resulting layer after etching. There are two circuit elements that comprise this layer. The first element is the gate (row) line interconnects that connect from the gate driver to each transistor. The second element becomes the bottom contact for the pixel storage capacitor. This also is the bottom electrode of the storage capacitor for each pixel.

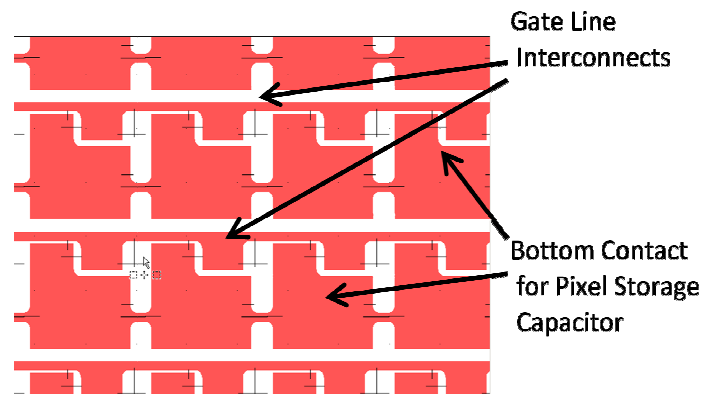


Figure 1.3.5-1 Gate layer after etching process

1.3.6. Transistor Operation

In order to better understand the failure modes of a display, it is essential to understand the operational characteristics of the thin film transistors. Operational characteristics of TFTs fabricated on glass are well understood and documented. On the other hand, electrical performance of TFTs fabricated on flexible substrates are less than ideal vary considerably due to the special processing considerations required due to the introduction of different substrate materials.

For rigid AMLCD displays the thin film transistors are deposited on glass and therefore can be fabricated at conventional process temperatures of (250-350C). This temperature range is the optimum for creating high quality hydrogenated amorphous silicon (a-Si:H). Unlike glass, plastics have a low heat resistance and therefore the deposition temperatures are usually at or below 150C. This lower deposition temperature results in inferior performance characteristics for the amorphous silicon [Sazonov 2000].

This lower temperature results in more dangling bonds of Silicon in the deposited film. Both Hydrogen and/or Helium dilutions are used in during the low temperature deposition process to attach to the dangling bonds and improve the electrical performance of the active region of the TFT [Parsons 2000]. For this investigation, the Flexible Display Center deposits the amorphous Silicon with a Hydrogen dilution at 150C.

Transistor operation is usually characterized by a plot of drain to source (I_{ds}) current as a function of the voltage applied at the gate of the transistor (V_{gs}). Several factors influence this function as defined in Equation 1.3.6-1. These factors include the mobility as denoted by μ , the capacitance as denoted by C_i , the dimensions of the active region – width and length (w and l), and the voltage threshold denoted by V_{th} .

$$I_{DS} = \mu C_i \frac{w}{2l} (V_{GS} - V_{th})^2 \quad (1.3.6-1)$$

The FDC conducted tests on the fabricated transistors and determined the mobility is in the range of $0.1 - 0.2 \text{ cm}^2/\text{V} \cdot \text{s}$ with an off state leakage current of approximately 10pA providing an on/off ratio of 10^6 . Figure 1.3.6-1 and Figure 1.3.6-2 show the I_{DS} characteristics of the fabricated transistors.

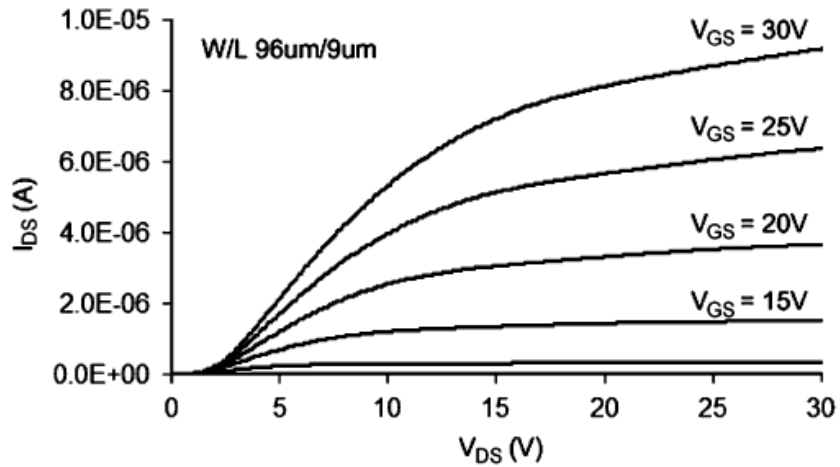


Figure 1.3.6-1 I_{DS} versus V_{DS} characteristics of TFT

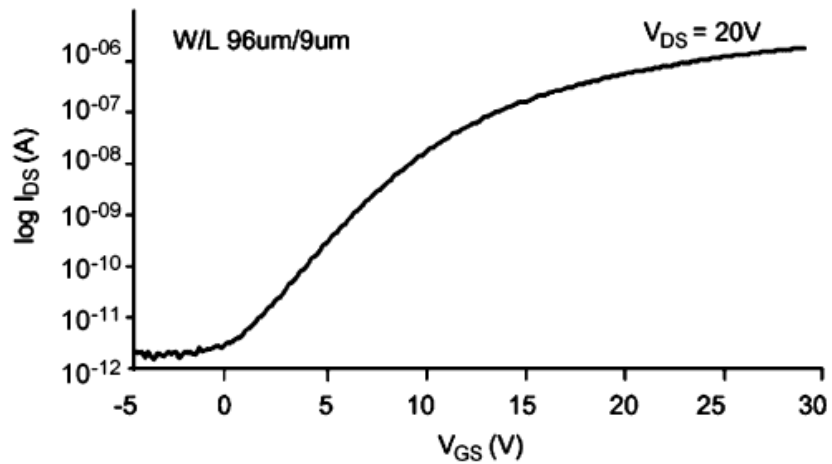


Figure 1.3.6-2 I_{DS} versus V_{GS} characteristics of TFT

Another unfavorable characteristic of amorphous thin film transistors fabricated at low temperatures on flexible substrates is the shift in threshold voltage through the life of the device. There are two main factors contributing to this shift in threshold voltage. The first is charge injection in the gate insulator which is the Silicon Nitride deposited on top of the substrate. The second is the creation of charged defect states (commonly called dangling bonds) in the amorphous silicon conducting channel. Over time this shift shall impact the performance of the overall display, but the above two factors are beyond the scope of this research.

1.4. Field Conditions for Flexible Displays

With the advent of making displays flexible, a whole new set of aspects are required when considering field use conditions. In addition, depending on the processes involved, handling to during initial fabrication may need to be considered as well. In some field use instances, the displays are shaped one time during system level assembly/integration to a conformed shape with a set radius of curvature that does not change. Figure 1.4-1 is an example of a wrist display assembly, whereby the display has been conformed one time to a set shape.



Figure 1.4-1 Pictures of wrist display conformed one time to a set radius

More stressful conditions involve displays that are routinely flexed, rolled, or even folded throughout their lifetime in the field as shown in Figure 1.4-2. The mechanical stresses endured throughout field use pose significant challenges with respect to reliability and device lifetime [Chwang 2003].



Figure 1.4-2 Example of field use conditions for flexible displays

1.5. Reliability Problem as Observed by the End User

Flexible displays provide a whole new set of reliability problems that were never present before with rigid displays. The basis of these problems stems from the fact that the display itself shall be subjected to bending both during initial fabrication as well as field use. Since there is limited reliability data from actual field use, not all of the reliability problems are known at this time. However, one known reliability problem at this time is that of “line outs”. This is a term that is used throughout industry to describe the condition of a display that contains either vertical or horizontal lines that can be observed visually by an operator. Depending on the display technology and the image being presented at the time of failure, these lines can be: white, black, red, blue, or green. The red, blue, and green would only be observed in color display since these are the basic primary colors used to make color images. Figure 1.5-1 is a picture of a flexible display with multiple line outs in both the horizontal and vertical directions.



Figure 1.5-1 Example of failure condition “line outs”

1.6. Failure Mode and Effects Analysis

In general, a complete Failure Mode and Effects Analysis (FMEA) for an entire display is a lengthy and involved task. Since the scope of this investigation revolves around line outs as observed by the end user, then only those failure modes that propagate and manifest themselves as such shall be considered in this analysis.

There are two main approaches to performing a FMEA. The first approach involves a top down perspective whereby the analyst starts with a block diagram of the system being investigated and correlates failure effects as observed at the system level with failure modes in the system block diagram. An iterative process takes place that involves linking the failure effects and associated high level failure modes to lower level failure modes of the design topology. This process continues until the analyst reaches the required level of identification of failure modes.

The second approach involves a bottom up approach whereby the analyst starts with identifying all the elements/components involved in the display. Once all the elements are identified, then failure modes for each element are characterized and their local impact/effects of the failure condition are determined. This process continues with postulating how the failure effects propagate to the next higher level of system integration. The analysis ends when the investigation determines how a particular low level failure mode manifests itself at the highest level of system integration and can be observed by the end user.

The FMEA performed for this investigation entailed both a top down as well as a bottom up approach for the specific end item observation of horizontal line outs in the display. The results of both were cross correlated and differences were resolved to result in one consolidated FMEA. Figure 1.6-1 is a diagram of the elements/components involved in the display system that contribute to the end item effect of horizontal line outs. Table 1.6-1 is an abridged version of the FMEA that identifies failure modes that contribute to horizontal line outs. The highlighted row in the FMEA table is the specific failure mode being that shall be discussed in greater detail in section 1.7 herein.

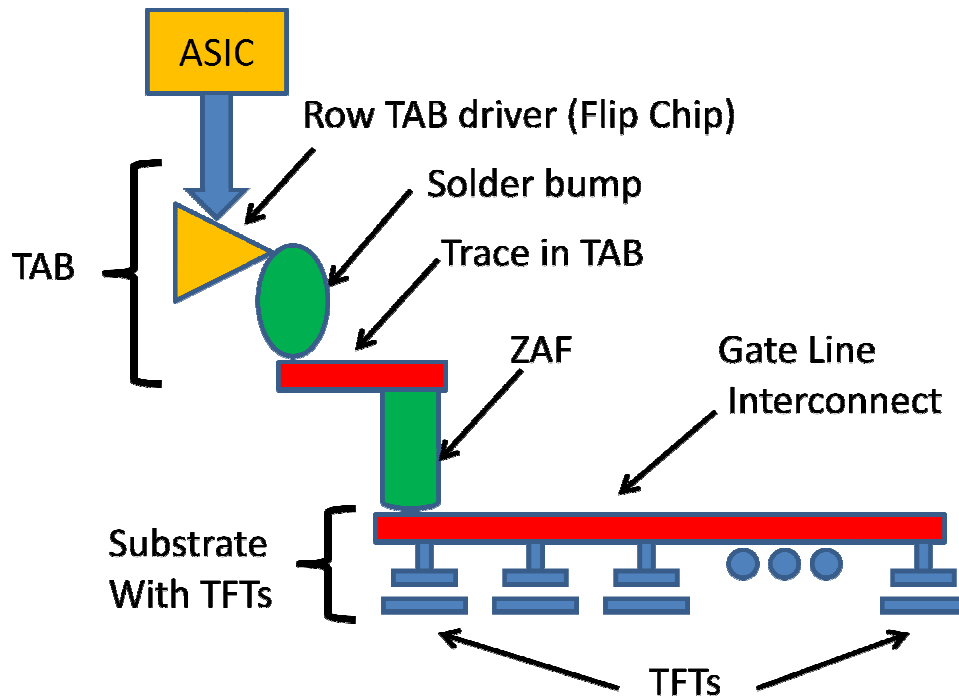


Figure 1.6-1 Diagram of FMEA Elements

Table 1.6-1 Failure modes that result in horizontal line-outs

Display Component/Element	Failure Mode	Local Effect	Next Higher Effect	End Item Effect
Display Driver ASIC	Internal Failure causing gross timing errors	Incorrect signals fed to shift registers for both Row and Column synchronizing	Row and Column data are incorrect and not-synchronized	Depending on severity of failure - could result in intermittent line outs to entire picture unreadable
Display Driver ASIC	Internal failure causing a specific Row command to not get fed into the Row shift register Driver circuit	Specific Row signal not being driven - no voltage applied to entire Row	No Gate voltage applied to TFTs on an entire row	Horizontal Line out
Display Driver ASIC	Internal failure causing a specific Column command to not get fed into the Column shift register Driver circuit	Specific Column signal not being driven - no voltage applied to entire Column	No Gate voltage applied to TFTs on an entire Column	Vertical Line out
Row TAB Driver Circuit	Open Circuit condition on a specific output signal of driver flip chip	No voltage applied to Row	No Gate voltage applied to TFTs on an entire row	Horizontal Line out
Row TAB Driver Circuit	Degraded Voltage on a specific output signal of driver flip chip	Low voltage applied to a specific row	No Gate voltage applied to TFTs on an entire row	Horizontal Line out
Row TAB Solder Bump to Flip Chip	Cracked solder bump - open circuit condition	No voltage applied to Row	No Gate voltage applied to TFTs on an entire row	Horizontal Line out
Row TAB Flex Traces	Open condition in TAB Flex traces	No voltage applied to Row	No Gate voltage applied to TFTs on an entire row	Horizontal Line out
Row TAB ZAF Connection	Open ZAF condition between TAB and Substrate	No voltage applied to Row	No Gate voltage applied to TFTs on an entire row	Horizontal Line out
Substrate -Row Line Interconnects	High impedance of Gate line Interconnects	Voltage drop across interconnect lines resulting in too low of voltage with respect to the Threshold Voltage of the TFT	Drive voltage on the Source of the TFT that represents the display image is not transferred to the Drain of the TFT.	Horizontal line through the display starting where the gate voltage is too low and continuing to the end of the substrate.
Internal TFT failure	Open Gate-condition	Drive voltage on the Source of the TFT that represents the display image is not transferred to the Drain of the TFT.	Inability of the transistor to adequately bias the electroluminescent material of the pixel	Individual pixels out on the display

1.7. Identification of Specific Failure Mode

As identified in Table 1.6-1, there are ten unique failure modes that could contribute to an end item effect of a horizontal line out as observed by the end user. Note that failure modes specific to the thin film transistors were not part of the 10 identified in Table 1.6-1. The reason for this is that both the bottom up approach and the top down approach did not yield any TFT failure modes that resulted in line outs. Catastrophic TFT failure modes resulted in individual pixel failures and gradual parameter drift failures that would affect all the TFTs in the display (such as voltage threshold drift) resulted in overall effects in the display performance and not an individual line out.

An investigation into all of these failure modes and specific failure mechanisms would be too broad of an investigation. Hence, it was decided that this investigation would focus on one particular failure mode that has been highlighted in the FMEA table.

This failure mode is high impedance of the gate line interconnects. The local effect of this condition is that the voltage as seen at the gate of a transistor is not high enough with respect to the TFT's threshold voltage. Another perspective of this condition as seen from the gate driver would be that the voltage threshold of the TFT would appear to be increasing. Hence, in keeping the gate voltage constant, the increased impedance of the gate line interconnect could be viewed as an increase in threshold voltage even though the internal threshold voltage of the TFT has not shifted.

The next higher effect of this failure mode is that the TFT does not adequately turn on and therefore the drive voltage coming from the column driver TAB (connected to the source of the TFT) does not get transferred to the drain side of the TFT. Hence, the end item effect is that the display image data initiating from the column TAB drivers does not bias the individual pixels in a particular row of the display. The end visual result as observed by the user is a “line out”.

1.8. Criteria for Failure

Now that a specific failure mode has been identified per section 1.7, the criteria for failure needs to be ascertained. An electrical circuit model was employed to simulate the behavioral characteristics of the TFT with increasing gate line impedance, the model program used is called Simulated Program with Integrated Circuit Emphasis (SPICE). Figure 1.8-1 is a schematic diagram of the TFT along with the pixel load as well as the gate voltage drive and the source voltage drive. Due to the proprietary nature of the design, circuit element values have been removed from the figure.

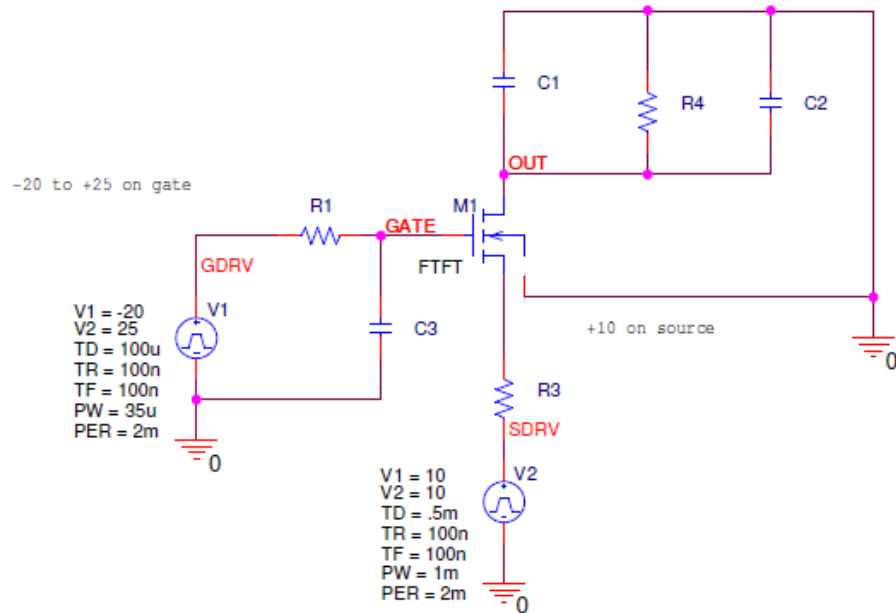


Figure 1.8-1 Schematic Diagram of SPICE Model

V1 is the gate driver voltage for an entire line and V2 is the source driver voltage for a column of pixels. R1 is the gate line resistance and C3 is the capacitance on the gate line. R3 is the source line resistance and M1 represents the TFT. On the Drain side of the TFT – C1 is the holdup capacitance and R4 in parallel with C2 represent the electrical equivalent circuit for the pixel. The circuit was simulated with the resistance value of R1 starting at its nominal value of 300k. The requirement is that the TFT turns on and transfers the 10V source drive to the drain in order to adequately drive the pixel within the 70uS line rate. Figure 1.8-2 shows proper operation of the circuit whereby at time equals 100uS the line pulse starts as defined by the red line. During this pulse, the blue drain/pixel voltage starts to ramp up from 0 volts to the 10V value as supplied from the yellow source line within the required line rate timeframe as shown by the red line at 170uS.

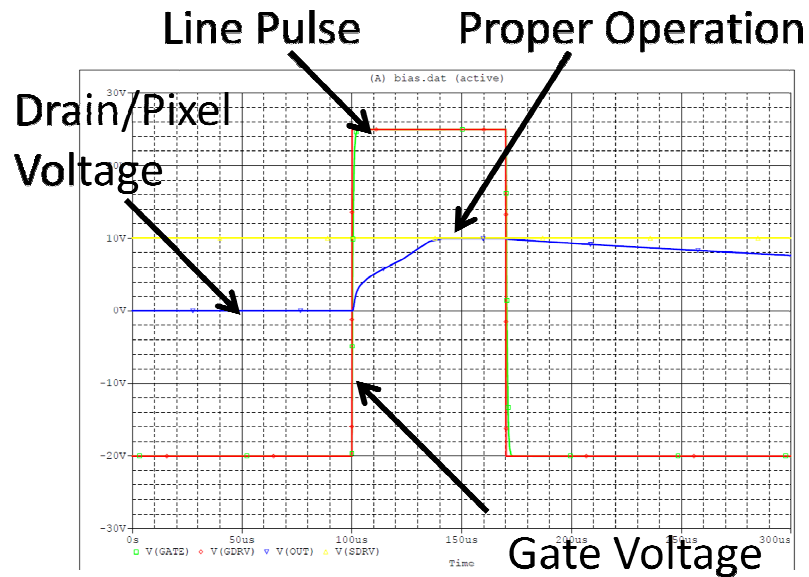


Figure 1.8-2 SPICE Model Output Showing Correct Operation

Figure 1.8-3 is the output of the SPICE when the gate line resistance is increased higher and higher beyond its nominal value. The failure condition is identified in the figure by the arrow pointing to the blue Drain/Pixel voltage line. In this figure the voltage does completely reach the source voltage of 10V within the line pulse window of 70uS. The value resistance value of the gate line where this threshold is reached is 450k Ohms.

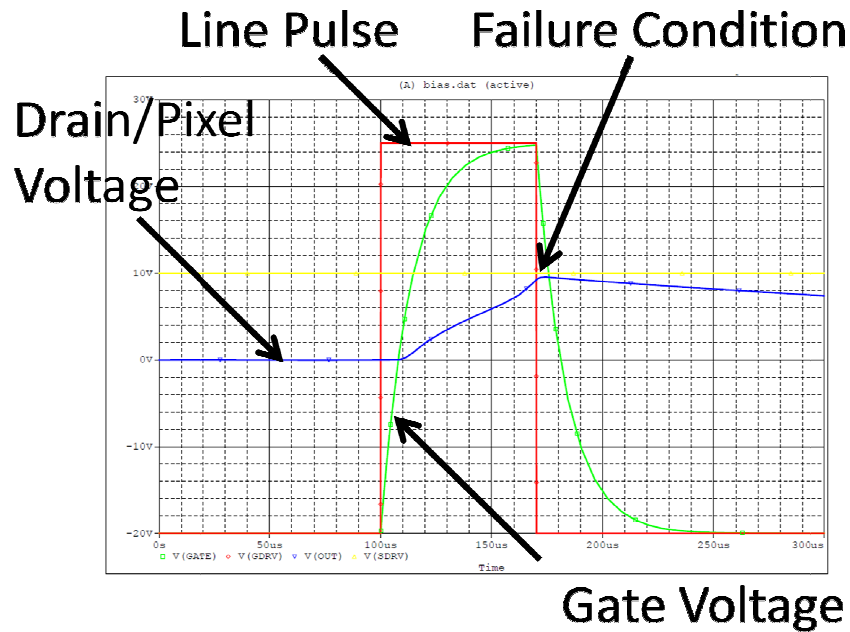


Figure 1.8-3 SPICE Model Output Showing Failure Condition

1.9. Statement of Problem

Given the myriad of reliability hurdles facing the adequate implementation of flexible displays in rugged field use environments, this investigation shall delve into understanding the particular failure condition observed by end users as “line outs”.

Based on the FMEA of section 1.6 several failure modes can manifest themselves as line outs, but only the failure mode of high impedance of the gate interconnect lines as identified in section 1.3.5 shall be of concern to this investigation. This impedance was modeled in SPICE as R1 in Figure 1.8-1 and simulation has determined that the threshold of failure is when this resistance exceeds 450k Ohms.

The problem being addressed by this thesis is: *What is an appropriate process for rapidly determining the life-stress relationship of gate line interconnects and using this relationship in the qualification of current and future flexible display designs?* In order to address this problem, there are several questions that this investigation will address:

- Given complex geometries, what is the best method to model the stresses?
- Should the model consider built in stresses from fabrication?
- How should a test be designed to obtain failure data in a timely manner?
- How does one select an appropriate model for flexible display failure modes?
- Once the model is determined, how does this aid in qualifying a new design?

1.10. Motivation and Contribution of this Thesis

Making displays flexible have created brand new failure modes as a result of unique failure mechanisms never before encountered with traditional style displays. Due to continuous advancements in flexible display technologies, from novel materials to unique fabrication techniques, it is apparent that a need exists for a method to rapidly test and assess their impact on reliability from a myriad of inter-related conditions. Therefore, the scope of this research has three main contributions.

The first element of this research is the design and fabrication of a dedicated test system to successfully capture dynamic changes in electrical performance of novel flexible test structures under accelerated fatigue stress conditions.

The second contribution of this research is the development and analysis of a finite element model of a specific test structure that is representative of an actual design in use for a current flexible display product.

The third and final contribution of this research is a framework for a methodology of testing and qualifying future multilayer interconnect designs on flexible substrates. This is achieved by a combination of the test system, finite element analysis of the test structure to characterize the failure mechanism, accelerated life testing, and Mean Time to Failure (MTTF) life-stress models.

Chapter 2: Analysis of Failure Mechanism

2. Overview

As defined in chapter 1, the failure mode of this investigation is increased resistance of gate line interconnects that result in the inability to drive thin film transistors required to bias pixels. The end item effect is manifested as “line-outs” visually observed in the display system. Now that the failure mode is succinctly defined, the next step is to understand the failure mechanism that is the root cause for inducing the failure mode observed at the system level. Examples of failure mechanisms vary from material interaction (Ohmic contact degradation), to electrical stress induced (electromigration, electro-static discharge), or to mechanically induced (die fracture from mismatch of thermal expansion coefficients).

This chapter shall identify and characterize the failure mechanism that causes the increased gate line resistance (failure mode). The following subsections provide a walkthrough of the process required to understand the failure mechanism. Section 2.1 is an in-depth analysis of the failure mode complete with micrographs from a Scanning Electron Microscope (SEM) as well as a proposed series resistance model used to characterize the failure mode. Section 2.2 covers fracture of thin films on compliant substrates. The difference between films in compression and tension as well as quantifying a fatigue induced failure shall be covered. Section 2.3 provides a background of the thermo-elastic properties of the materials used for the substrate, insulating layers, and gate line interconnect traces. Section 2.4 calculates the internal

stresses as a result of the fabrication process at elevated temperatures using materials with different coefficients of thermal expansion. Sub-section 2.4.2 is dedicated to a finite element analysis using a program called Coventor that specializes in modeling stresses from fabrication. Section 2.5 provides the background for understanding externally induced stress as a result of bending forces employed during field use conditions. Sub-section 2.5.2 contains the results of ANSYS finite element analyses used to predict stresses under specific field conditions.

2.1. Characterization of the Failure Mode

Since the resistance of the gate line interconnect is increasing throughout the life of device in the field, one needs to understand at a microscopic level what is actually happening to create the phenomena. There can be several factors that can influence the resistance of the interconnects such as cracks in the thin film as well as corrosion of the material itself. Corrosion is a concern due to the use of flexible displays in harsh environments. Contamination as a result of the introduction of impurities from raw materials used in the fabrication, the production environment itself, and material handling plays a major role in this process. Once contamination is introduced to the system, the combination of humidity, temperature, and a voltage potential become mechanisms to facilitate the corrosion phenomenon. Research on the influence of scratches of the ITO during fabrication found that the presence of Cl^- reacts with the moisture to form HCl that then reacts with the Indium Oxide (In_2O_3) causing the breaking of bonds of H-Cl and In-O and resulting in In-Cl and O-H bonds. This outcome of this chemical process is the eventual discoloration and structural damage of the ITO film [Leung 2008]. For this investigation, failure analysis techniques were

employed to capture images of the failure condition as well the proposition of a physical resistance model that relates the increasing resistance to mechanical cracks forming in the ITO film.

2.1.1. Cracks in Gate Line Interconnect Thin Film

During a root cause investigation, there are several failure analysis tools that can be employed to get a better understanding of the physics behind the failure at the microscopic level. Here a scanning electron microscope (SEM) was used to capture images of the gate line interconnect traces at high magnification. Figure 2.1.1-1 is an image capture from a Vega SEM manufactured by TESCAN at the Materials Analysis Group lab in Norcross, GA. The image was generated using a back scattered electron (BSE) detector with a SEM voltage of 20kV. Using the SEM, it was evident that micro-cracks are being formed in an ITO trace for a gate line interconnect.

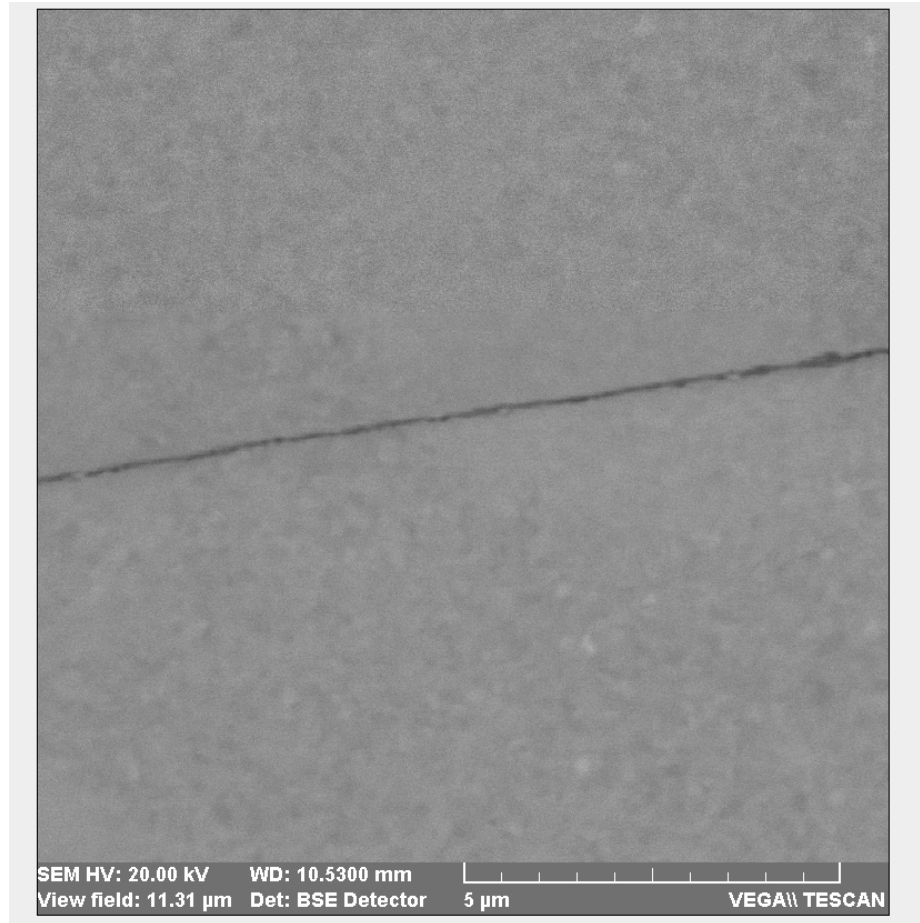


Figure 2.1.1-1 SEM Micrograph of Cracks in ITO Thin Film

In order to provide perspective of the SEM image in Figure 2.1.1-1 a diagram of the gate line interconnect from chapter 1 has been duplicated herein to show where in the system this crack exists. Figure 2.1.1-2 is taken from the gate mask used during fabrication of the flexible display. The top portion of the diagram is the actual gate line trace used to connect the drive voltage to the gates of two thin film transistors (TFT 1 and TFT 2). Example cracks have been drawn in on the left side of the trace. The bottom portion of the diagram is also part of the same mask, but this is the bottom electrode of a capacitor underneath the pixel area. The capacitor is electrically

isolated from the gate, but shown here since it is part of the same mask used in the photolithography process.

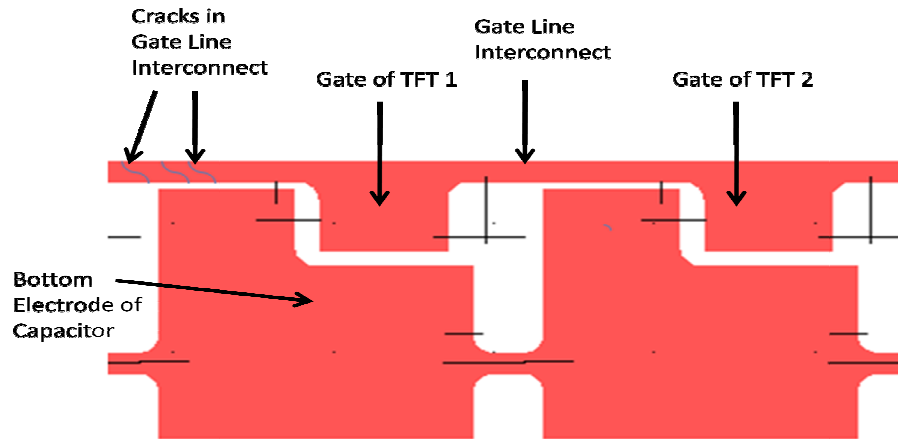


Figure 2.1.1-2 Cracks in Film of Gate Line Interconnects

It is common sense that a crack would increase the resistance of a trace, but a physical model is required in order to characterize the relationship between a crack and the trace resistance as well as the quantity of cracks to the trace resistance.

2.1.2. Series Resistance Model

Based on experimental observations of increasing resistance with increasing strain a physical model was developed to corroborate the evidence [Cairns 2000-A]. The main observations of ITO on PET were as follows:

- cracks traverse the entire width of the ITO structure
- ITO resistance increases rapidly when a threshold strain is reached
- resistance increase is synonymous with the initiation of cracks
- density of cracks per unit length of ITO increases rapidly and then saturates

The proposed model states that at some threshold strain the first crack in the ITO layer is formed. The crack is bridged by some minute amount of ITO material and its volume is assumed to be constant, the constant volume allows for a nonlinear increase in resistance of a crack as the width increases. Each crack is also independent of every other crack and therefore the resistance of the sample increases based on the series sum of resistances of each of the cracks, reference Figure 2.1.2-1.

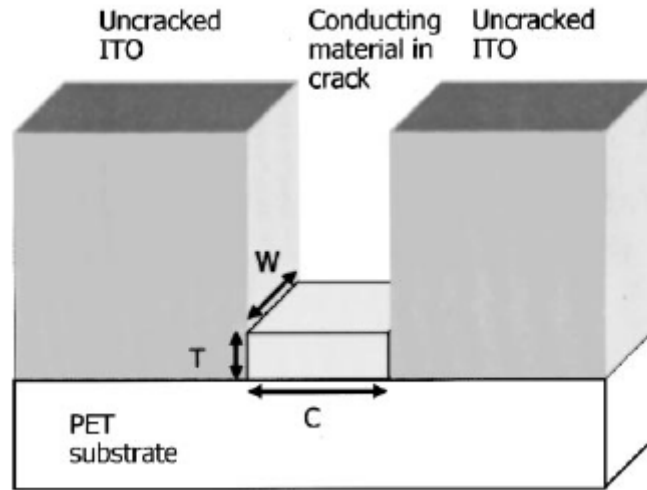


Figure 2.1.2-1 Diagram Showing Bridging Material Inside a Crack

If one treats the cracks as a set of resistors connected in series, then one can ignore the negligible change in resistance of the ITO versus that across the cracks as a function of strain. For each crack, the i^{th} resistance is calculated as:

$$R_i = \frac{\rho C_i}{A} = \frac{\rho C_i^2}{V} \quad (2.1.2-1)$$

Here ρ is the resistance property of the ITO material and C_i is the extent of the

opening of the crack as shown in Figure 2.1.2-1. V is the fixed volume of the ITO material on the substrate surface inside the crack which is calculated based on the thickness (T), width (W), and the crack opening (C). A is the cross sectional area of the volume based on thickness and width. The length of the bridging layer (C) is assumed to be zero at the instant the crack forms and then with increasing strain, C becomes larger. The length of the bridge as a function of strain is computed as:

$$C_i = D(\varepsilon - \varepsilon_{ci}) \quad (2.1.2-2)$$

Here, ε is the instantaneous strain, ε_{ci} is the strain at which the i th crack forms, and D is a length scale. Based on the assumption that the volume of ITO in the bridge zone is conserved then the resistance is defined as:

$$R_i = \frac{\rho D^2 (\varepsilon - \varepsilon_{ci})^2}{V} \quad (2.1.2-3)$$

Using n as the total number of cracks at strain ε , then the total resistance of all the cracks in the ITO layer is computed as:

$$R_{total} = \sum_{i=1}^n \frac{\rho D^2 (\varepsilon - \varepsilon_{ci})^2}{V} \quad (2.1.2-4)$$

Note that this is the calculated resistance of the cracks and this resistance needs to be added to the original resistance of the ITO material prior to any strain being imposed

to obtain the total resistance of the specimen under test. Given the SPICE model from section 1.8 determined the failure threshold was a trace resistance of 450k Ohms and the average initial trace resistance is approximately 200k Ohms, then the critical resistance to induce failure as a result of cracks is calculated to be approximately 250k Ohms.

This section provides a physical series resistance model that explains the correlation between crack size, number of cracks, and the increase in resistance of the gate line traces with increasing applied strain.

2.2. Fracture of Thin Films

Common failure modes of thin film layered devices involve the growth of micro cracks under stress. The specifics of the fracture mode depend on the substrate modulus, film adhesion, and film cohesion. The two most common types of failures for brittle films on flexible substrates are:

- Film cracking / channeling
- De-bonding

Film cracking is more common for films in tension with good adhesion between layers, while de-bonding is more common for films in compression when adhesion is poor [Hutchinson 1992]. Figure 2.2-1 shows the two types of fracture in thin films. The left hand portion of the figure reflects how cracks form from the structure in tension while the right hand portion of the figure reflects how cracks form from the structure in compression (de-bonding of the film followed by buckling).

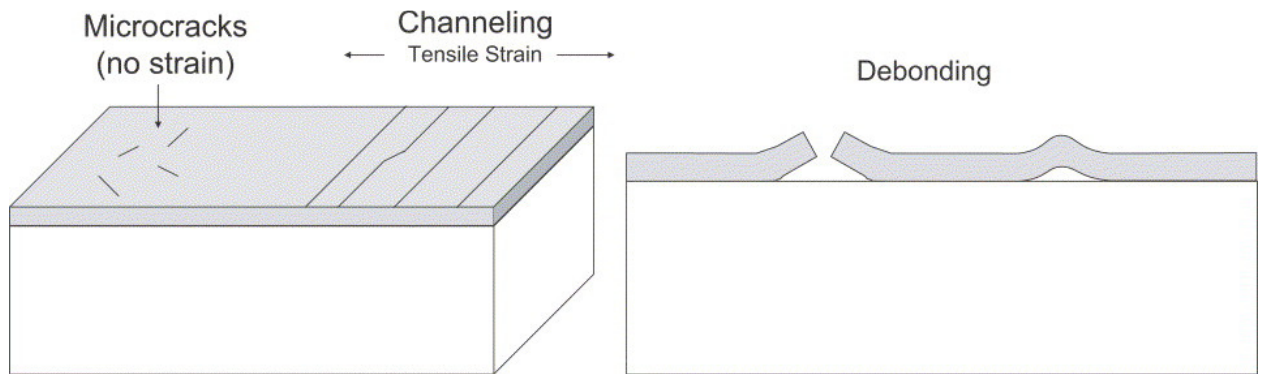


Figure 2.2-1 Common Types of Fracture in Thin Films

2.2.1. Thin Films in Compression

Although this study is focused on films in tension, this section provides a high level summary of failure of thin films while under compression in order to better understand the differences between the two types of failures. Under compression the film undergoes several stages until failure [Chen 2002]:

- De-lamination from substrate
- Buckling of the film
- Cracking of the thin film in a tunneling motion

Figure 2.2.1-1 shows a thin film in compression that has de-laminated and started to buckle.

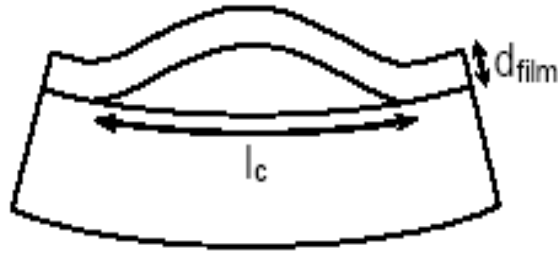


Figure 2.2.1-1 De-lamination of Thin Film Under Compression

As the de-bonded length grows, it will reach a critical value l_c that will cause it to buckle and then fracture. Equation 2.2.1-1 is used for determining the critical de-bonding length for buckling if the film is under compressive stress, where d_{film} is the thickness of the film and E_{film} is the elastic modulus of the film [Suo 2001].

$$l_c = \frac{\pi d_{film}}{\sqrt{3(1-\nu_{film}^2)}} \sqrt{\frac{E_{film}}{\sigma_{film}}} \quad (2.2.1-1)$$

2.2.2. Thin Films in Tension

The mechanics and brittle failure mechanisms of single and multilayered films on flexible substrates have been studied extensively [Andersons 2003]. As a background, the theory is that starting from a pre-existing defect (flaw in the deposited film) a crack will propagate with a depth equal to the film thickness. It will arrest at the film-substrate interface leaving it intact as shown in Figure 2.2.2-1. The crack elongates laterally in the film uninhibited until it merges with another crack or propagates all

the way to the edge of the film. This type of fracture is commonly referred to as a channel cracking and is the type of fracture that is the root cause for the increase in resistance of the series resistance model defined in section 2.1.

Since the film is under tension, it is critical to understand what is the amount of stress a film can be subjected to before a channel crack is initiated and starts to propagate. Section 2.2.3 is dedicated to the detailed understanding and physics behind channel cracking in thin films.

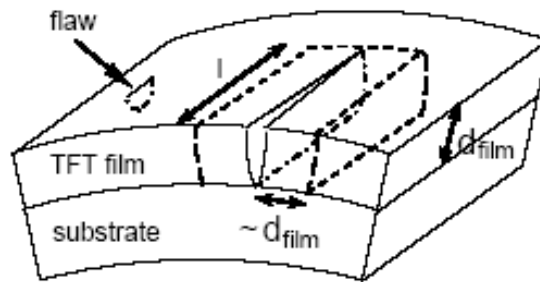


Figure 2.2.2-1 Initial Flaw and Growth of Crack in Thin Film Under Tension.

2.2.3. Channel Cracking as a Result of Induced Stress

Figure 2.2.3-1 is an exploded view of a test structure being subjected to a four-point bending test. Here the structure (consisting of a substrate with a thin film bonded to it) is exhibiting the propagation of a channel crack. It should be noted that the depth of the crack is limited to the thickness of the film and the crack propagates laterally

across the surface of the film normal to the stress being applied as a result of tension from the four point bending system [He 2004].

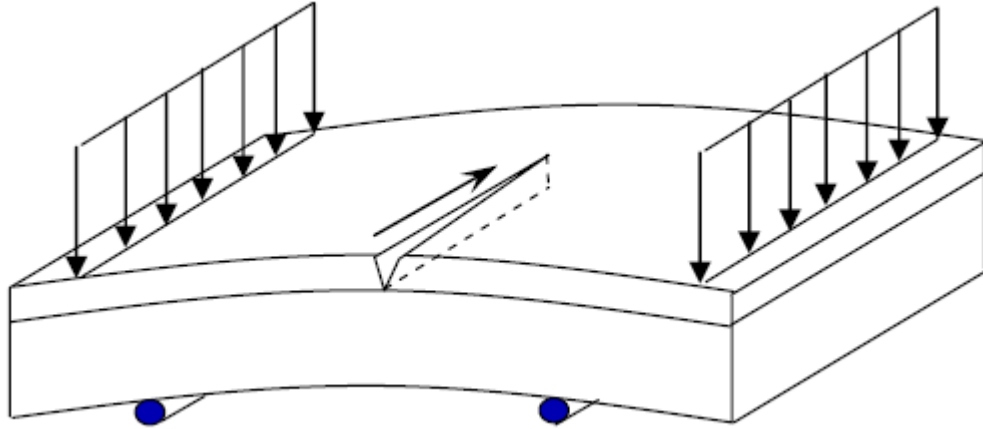


Figure 2.2.3-1 Channel Cracking in Thin Film Under Tension

During crack propagation a new crack surface is formed requiring new surface energy. G is the elastic energy reduction associated with the crack advancing per unit area. For a specific crack geometry, the crack driving force is determined by solving an elastic boundary value problem. The material in which a crack is propagating has an intrinsic property for crack resistance (Γ). Depending on where the crack is propagating, there are three different values of crack resistance: the film, the substrate, or the interface denoted as Γ_f , Γ_s , and Γ_i respectively. The Von Mises yield criterion states that material begins to yield when the second deviatoric stress invariant (J_2) reaches a critical value k which is $\sqrt{3}$ times lower than the tensile yield stress (σ_y). Substituting the principal stresses into the von Mises criterion equation

we have equation 2.2.3-1. For simple uniaxial stress both σ_2 and $\sigma_3 = 0$ and the Von Mises criterion reduces to $\sigma_1 = \sigma_y$.

$$(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_1 - \sigma_3)^2 = 2\sigma_y^2 \quad (2.2.3-1)$$

For brittle thin films, cracks propagate when the energy release rate is equal to or larger than the film's crack resistance [Hutchinson 1992]. Based upon exploded view of a channel crack in Figure 2.2.3-2, the growth of a channel crack is given by equation 2.2.3-2, where h_f is the thickness of the film, and σ_f is the stress in the film. \bar{E}_f is the effective plane strain elastic modulus of the film and ν is Poisson's ratio as defined in equation 2.2.3-3.

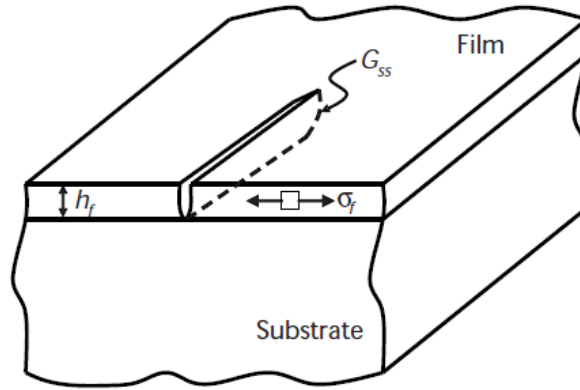


Figure 2.2.3-2 Steady State Growth of Channel Crack

$$G = Z(\alpha, \beta) \frac{\sigma_f^2 h_f}{\bar{E}_f} \geq \Gamma_f \quad (2.2.3-2)$$

$$\bar{E}_f = \frac{E_f}{(1-\nu^2)} \quad (2.2.3-3)$$

The term Z in equation 2.2.3-2 is a constant whereby its magnitude depends on the crack type and the elastic mismatch of the substrate and thin film. Z is a function of the Dundur's parameters α and β , whereby α is the more dominant factor. For plane strain conditions, α is given by equation 2.2.3-4 and β is given by equation 2.2.3-5 [Hutchinson 1992].

$$\alpha = \frac{\bar{E}_f - \bar{E}_s}{\bar{E}_f + \bar{E}_s} \quad (2.2.3-4)$$

$$\beta = \frac{\bar{E}_f(1-\nu_f)(1-2\nu_s) - \bar{E}_s(1-\nu_s)(1-2\nu_f)}{2(1-\nu_f)(1-\nu_s)(\bar{E}_f + \bar{E}_s)} \quad (2.2.3-5)$$

Using a two-dimensional finite element model [Huang 2003], one can calculate the crack opening displacement (z), from which the energy release rate for channel cracking can be determined per equation 2.2.3-6.

$$G_{ss} = \frac{\sigma_f}{2h_f} \int_0^{h_f} \delta(z) dz \quad (2.2.3-6)$$

The value of Z can be calculated by comparing 2.2.3-2 and 2.2.3-6 [Beuth 1992]. The value of Z as a function of α (with $\beta = \alpha/4$) where calculated and the numerical results are provided in Figure 2.2.3-3.

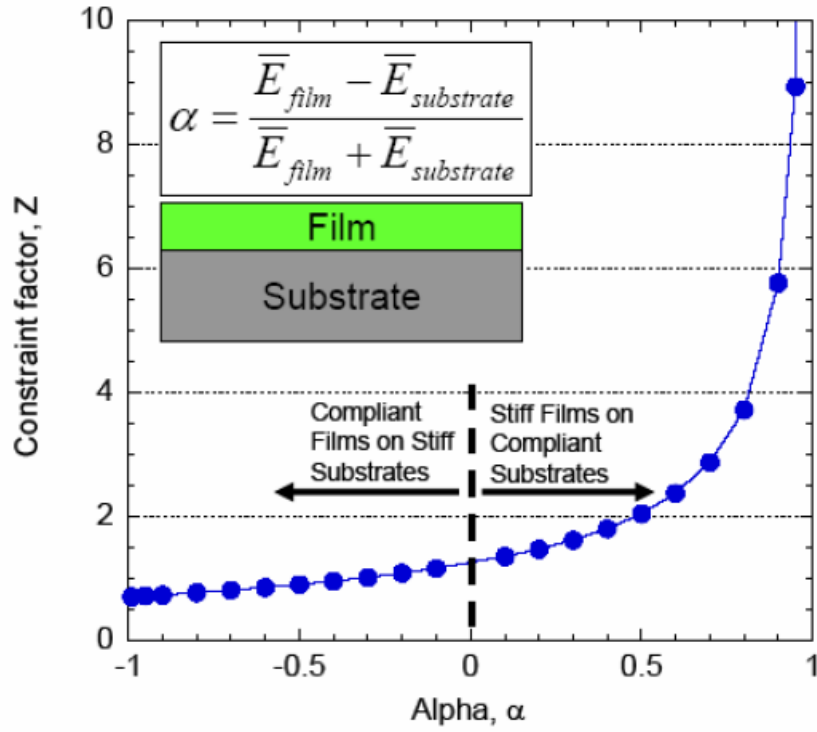


Figure 2.2.3-3 Z as a Function of α with $\beta = \alpha/4$ [Lu 2006].

Given the properties of the film and substrate, one can calculate the Dundur parameters and then the Z constant. Knowing the thickness and crack resistance (Γ) of a given film, one can determine the required stress of the film in order to propagate a channel crack. This is referred to as the intrinsic critical stress. As evident from equation 2.2.3-1, the intrinsic critical stress for crack propagation is proportional to the thickness of the film layer as shown in equation 2.2.3-7.

$$\sigma_{intrinsic} \propto \frac{1}{\sqrt{h}} \quad (2.2.3-7)$$

However, an initial review of test data does not fully corroborate this relationship, since the required stress for fracture seems to level off as the thickness increases [Leterrier 2003]. The data does corroborate when one factors in the amount of internal stress in the film as a result of fabrication (deposition at elevated temperatures), as shown in Figure 2.2.3-4. Note that the internal stress in the figure is negative reflecting compressive internal stress in the film from fabrication. The amount of internal stress is not only a function of film thickness, but also: substrate thickness, the Elastic Modules of the film and substrate, the difference in the coefficients of thermal expansion of both the film and substrate, and the deposition temperature. Section 2.4 is dedicated to determining the internal stress as a result of fabrication specific to this investigation.

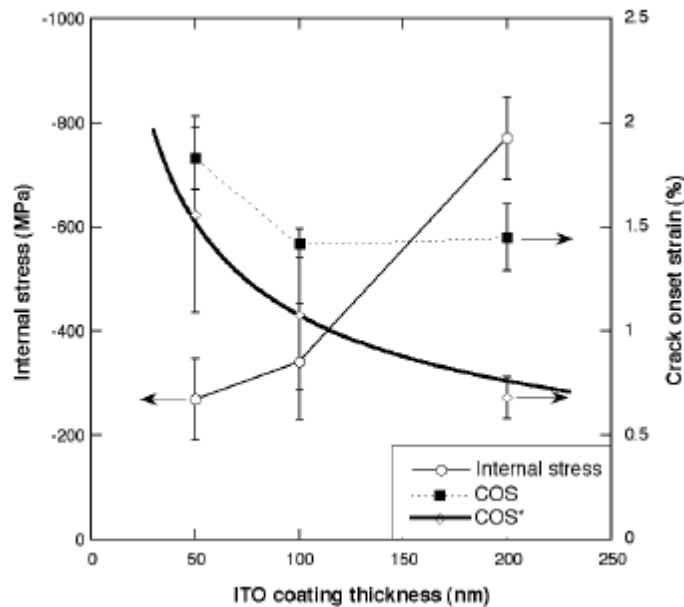


Figure 2.2.3-4 Impact of film thickness on intrinsic crack onset strain

The figure makes reference to crack onset strain, which is the strain at which the film resistance has increased by 10% as a result of film cracking. Chapter 3 is dedicated to previous work and the characterization of crack onset strain. Equation 2.2.3-8 summarizes the relationship between the external stress required for crack initiation to the intrinsic critical stress for crack propagation and the internal stress in the film.

$$\sigma_{external} = \sigma_{intrinsic} - \sigma_{internal} \quad (2.2.3-8)$$

Figure 2.2.3-5 provides an overall summary for the discussion provided in this section on channel cracking as a result of induced tensile stress. It shows how the material properties of the film and substrate impact the Dundur parameters that roll up into the Z constant of elastic energy G. Knowing the fracture resistance of the film (Γ), one can calculate the intrinsic stress ($\sigma_{intrinsic}$) required for crack propagation. Data has shown that a film's internal stress influences the amount of external stress required for crack propagation.

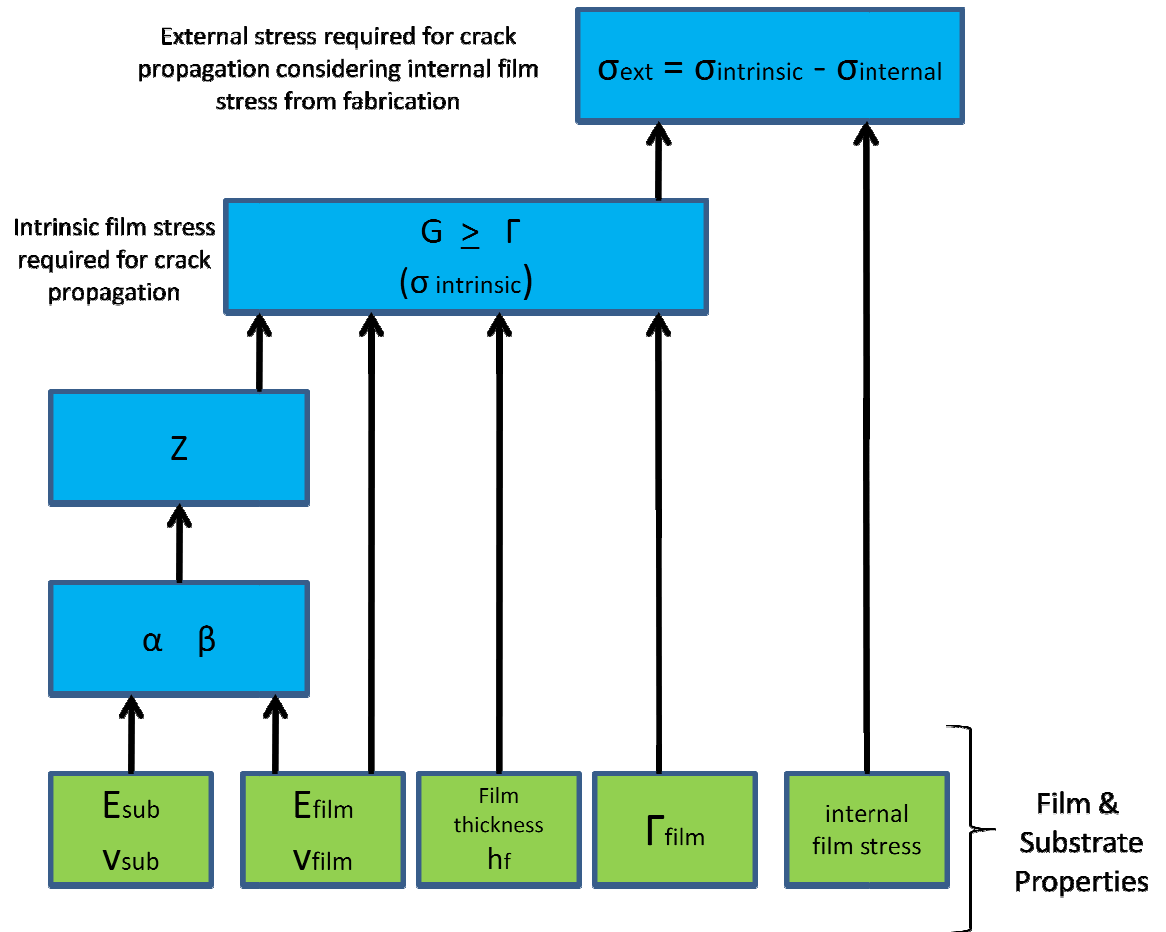


Figure 2.2.3-5 Relationship of Film and Substrate Properties to crack propagation

This section has outlined the general approach for determining the critical stress required for channel crack propagation in a given structure. Section 2.3 is dedicated to the material properties of the specific structure for this investigation and section 2.4 shall determine the amount of internal stress in the film as a result of fabrication. Knowing the material properties and internal stress, the external stress required for crack propagation shall be calculated based upon the method outlined in Figure 2.2.3-4. Section 2.5 shall relate the physical bending of the structure to the external stress applied to the thin film.

2.3. Properties of Materials Used in Investigation

Chapter 1 provided an overall perspective of a flexible display system that included a complex cross section of the device to include numerous materials required for fabrication. This investigation is only concerned with a subset of the device materials since the failure mode is specific to the gate line interconnect traces. Therefore, Figure 2.3-1 is a simplified cross section showing the layers and materials of concern to investigate the failure mechanism of channel cracking in the ITO thin film that makes up the gate line interconnect traces.

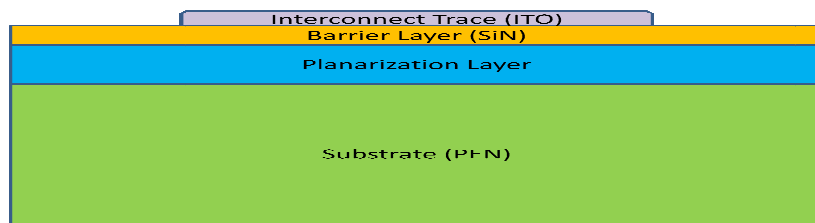


Figure 2.3-1 Cross section of device layers critical to failure mechanism

Each of the following sections is devoted to the material properties of the above identified layers in the cross section. Section 2.3.1 is dedicated to the substrate and its importance in a flexible display. Specific material properties are provided for Polyethylene Naphthalate (PEN) which is material chosen for this investigation. A discussion on the importance of the planarization layer is also provided. Section 2.3.2 is dedicated to the barrier layer and the material properties of Silicon Nitride. Section

2.3.3 is dedicated to the gate line interconnect layer and the material properties of Indium Tin Oxide (ITO).

2.3.1. PEN Substrate

When it comes to selecting an appropriate material for the substrate of a flexible display, several key characteristics exist. A few of these characteristics are: a low coefficient of thermal expansion, low shrinkage, and a relatively high processing temperature. The substrate material chosen for this particular study is Polyethylene Naphthalate (PEN). The supplier of this transparent flexible material is DuPont Teijin Films and their catalogue product: Teonix Q65FA is the specific one used for this investigation with a thickness of 125um. Table 2.3.1-1 provides a breakdown of the key property values for the Teonix Q65FA.

Table 2.3.1-1 Listing of material properties of PEN substrate

Property	Value
Upper processing temperature	180-220C
Young's modulus at 20C	5GPa
Young's modulus at 150C	3GPa
Glass transition	120C
Moisture pickup at 20C 40%RH	1,000ppm
Coefficient of thermal expansion	18-20ppm/C
Shrinkage at 150C after 30min	0.05%

Using a Scanning Electron Microscope (SEM) the surface quality of the PEN film has shown micro-roughness and sporadic surface peaks up to 10s of microns in the lateral

dimension and with heights of 100s of nanometers as reflected in Figure 2.3.1-1 [MacDonald 2007]. In order to improve surface quality by reducing surface peaks, a planarization layer is applied to the PEN substrate. This layer is deposited at 200°C using a spin coating technique resulting in a layer thickness of 2 microns. This is the first process step in the flexible display fabrication process as well as the fabrication of the test structures.

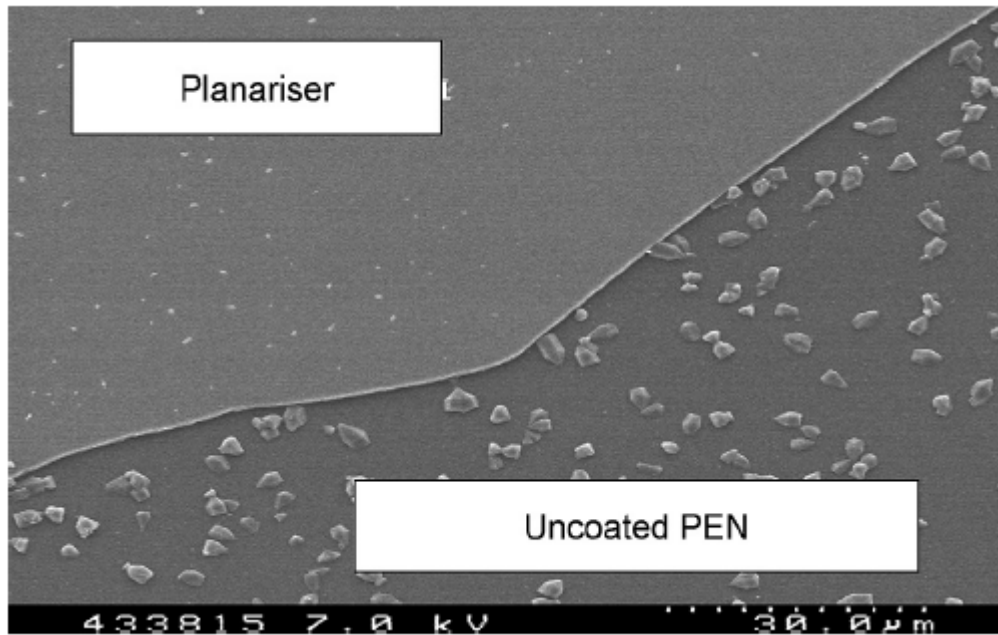


Figure 2.3.1-1 Surfaces of PEN film (Planarized versus Unplanarized)

2.3.2. SiN Buffer Layer

The next step in the fabrication process is the application of a buffer layer on top of the substrate. Using Plasma Enhanced Chemical Vapor Deposition (PECVD), a 0.3 micron thick layer of Silicon Nitride is deposited at 180°C. With respect to material properties of silicon nitride films deposited using PECVD, Isono et al used atomic

force microscope (AFM) tensile testing techniques to characterize the elastic properties of the thin films [Isono 2005]. For the elastic modulus, the results ranged from 102 GPa to 143 GPa and were independent of film thickness. The Poisson's ratio was determined to range between 0.2 to 0.26 using tensile and nano-indentation combined techniques. The value for the coefficient of thermal expansion (CTE) was determined by Toivola et al with a range from 2.19 ppm/ °C to 2.30ppm/°C [Toivola 2003].

2.3.3. ITO Gate Layer

Normally the gate layer material is molybdenum or aluminum, but in this investigation Indium Tin Oxide (ITO) has been chosen since it was the material requested by the Flexible Display Center (FDC) in Tempe, AZ. The FDC has been chartered by the Army Research Lab (ARL) to accelerate the development of flexible displays by investigating the use of novel materials. ITO has consistently been a material of choice for display products given its properties of being both optically transparent in the visible spectrum while also having conductivity approaching that of metals. To enable flexible- transparent displays that may be mounted on the windshield of a car to allow the user to see through the display, ITO is better suitable than standard metal conductors such as Molybdenum or Aluminum.

When it comes to employing different materials for use in display applications, a figure of merit (ϕ) is used to compare materials based on a ratio of their optical transmittance to their sheet resistance [Haacke 1976]. Equation 2.3.3-1 is used to

calculate this figure of merit whereby α is the visible absorption coefficient, ρ is the materials resistivity, and x is the thickness of the material.

$$\phi = \frac{x}{\rho} e^{(-10\alpha x)} \quad (2.3.3-1)$$

Even though thin metals, conducting polymers, and degenerately doped wide band gap semiconductors have reasonable figures of merit, ITO is commonly used in displays since it has a figure of merit orders of magnitude higher than these options with a value of $0.22\Omega^{-1}$ with a resistivity of $\rho = 1.6 \times 10^{-4} \Omega\text{cm}$ and a visual absorption coefficient α of 10^3cm^{-1} with a film thickness of 1,000 nm. Recent analysis was performed on ITO films deposited on polyethylene terephthalate (PET) substrates by using DC-Magnetron sputtering techniques. The film thicknesses ranged from 25.00 nm to 114.50 nm with varying deposition times with the results summarized in Table 2.3.3-1 and Figure 2.3.3-1 [Ali 2010].

Table 2.3.3-1 Electrical properties of ITO films deposited on PET

Film Thickness (nm)	Sheet Resistance (Ω/Sq)	Carrier Concentration N (cm^{-3})	Hall Mobility μ ($\text{cm}^2/\text{v-s}$)
25.00	18.85	1.09E+17	4.84
82.70	18.72	3.01E+19	5.32
114.50	17.75	7.94E+21	6.20

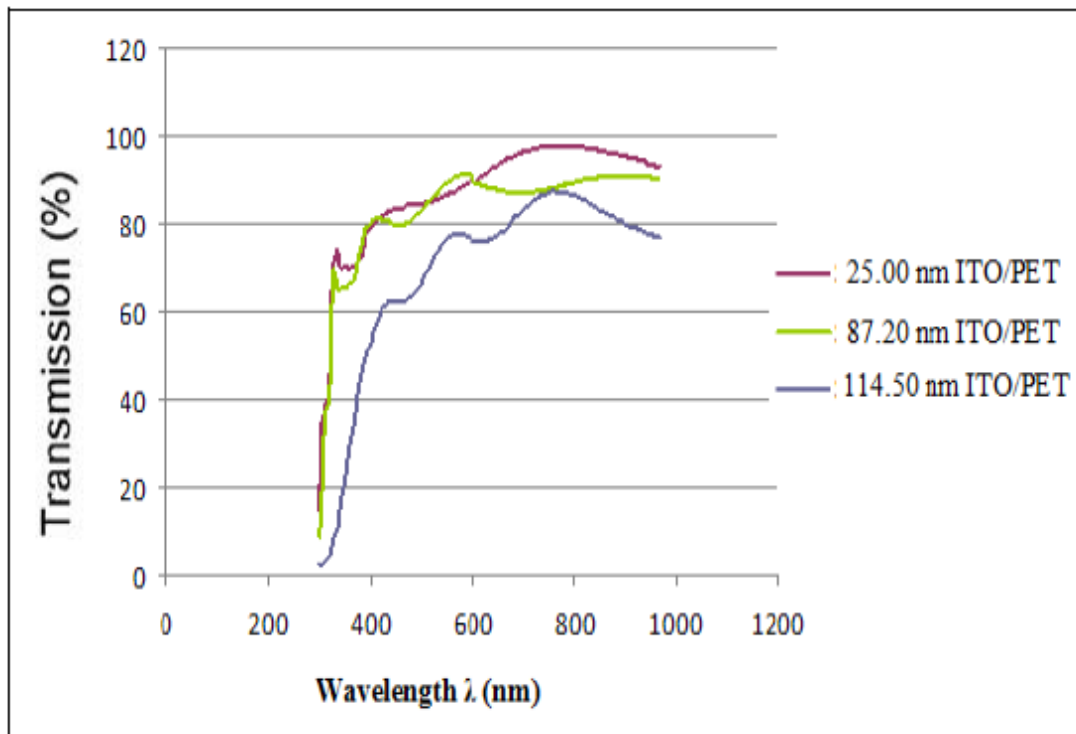


Figure 2.3.3-1 Optical transmittance (T) of ITO films deposited on PET

Indium oxide has a cubic bixbyte structure with a lattice constant of 1.0117nm [Hamburg 1986]. The bixbyte structure consists of an 80 atom unit cell with the Ia3 space group and 1nm lattice parameter with an arrangement based on stacking of InO_6 coordination groups [Paine 2005]. The structure is a face centered cubic array of cations having the tetrahedral interstitial positions being occupied by anions. The bixbyte may be visualized with respect to a simpler face-centered cubic fluorite (CaF_2) $2 \times 2 \times 2$ supercell with just one quarter of the anion sites vacant as shown in Figure 2.3.3-2 [Walsh 2010]. Leveraging the existing knowledge of the surface chemistry of the fluorite structure, one is able to gain some insight into the more complex bixbyte ITO structure.

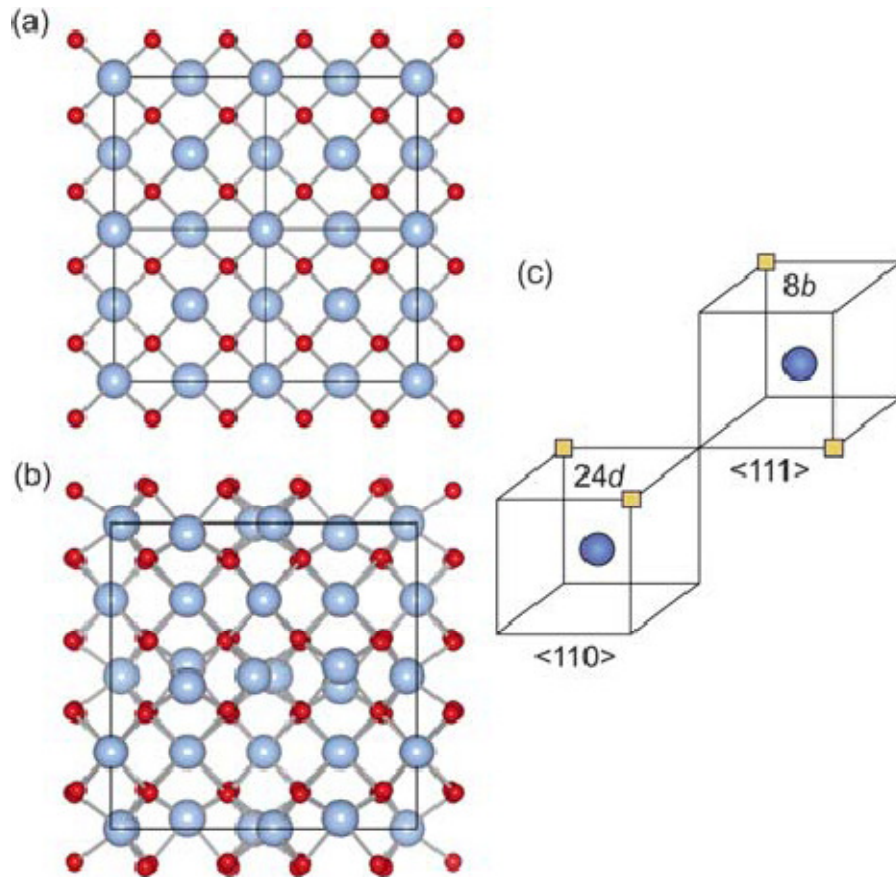


Figure 2.3.3-2 Structures of (a) fluorite, (b) bixbyite, and (c) anion vacancies

The most common method for depositing ITO is DC magnetron sputtering. ITO is commonly deposited onto glass substrates with a temperature between 250-350°C. Figure 2.3.3-3 shows the sputtering process. Even though this process offers the lowest resistivity the high deposition temperature makes it impractical for manufacturing flexible displays whereby the maximum process temperatures are limited based on the use of a polymer substrate.

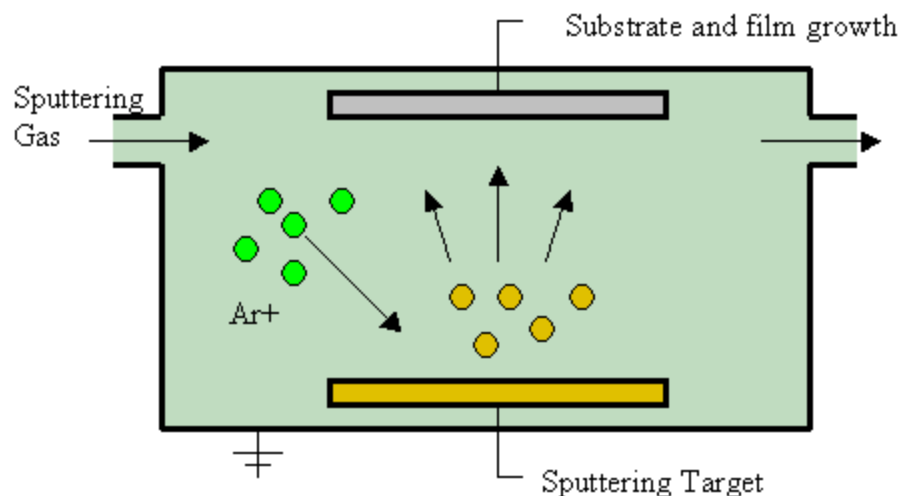


Figure 2.3.3-3 Diagram of sputtering process

Amorphous ITO is created during the physical vapor deposition process due to InO_x species arriving on the surface and are randomly oriented as they form a thin film covering the target surface. Crystallization of the amorphous ITO ensues by lateral growth of the islands until adjacent islands start to impinge upon each other and the result is the formation of grain boundaries.

The impact of ITO film thickness on the texture and surface morphology was extensively studied using samples deposited on glass substrates using DC Magnetron sputtering with a 3 in. circular target diameter and a ratio of 90 wt.% In_2O_3 – 10 wt.% SnO_2 [Liang 2010]. Figure 2.3.3-4 shows SEM micrographs of the ITO deposited as various thicknesses and the results indicate that surface roughness increases with increasing film thickness.

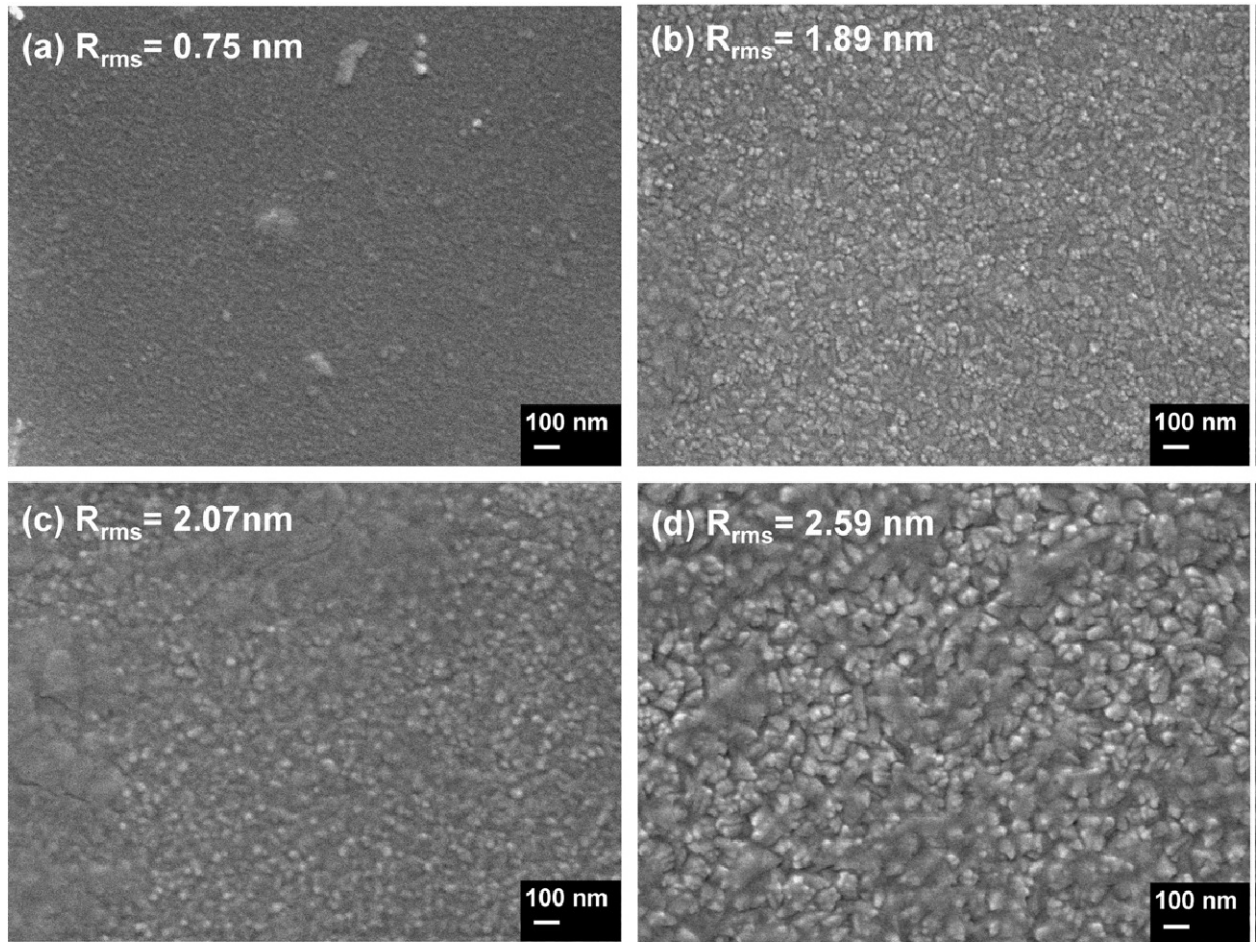


Figure 2.3.3-4 SEM micrographs of varying ITO film thicknesses

A comparative study was performed for ITO deposited at room temperature using both DC and RF magnetron sputtering techniques. The influence of sputtering power as well as the oxygen content in the Ar-O₂ gas mixture was analyzed and results are summarized in Figure 2.3.3-5 [Kurdesau 2006].

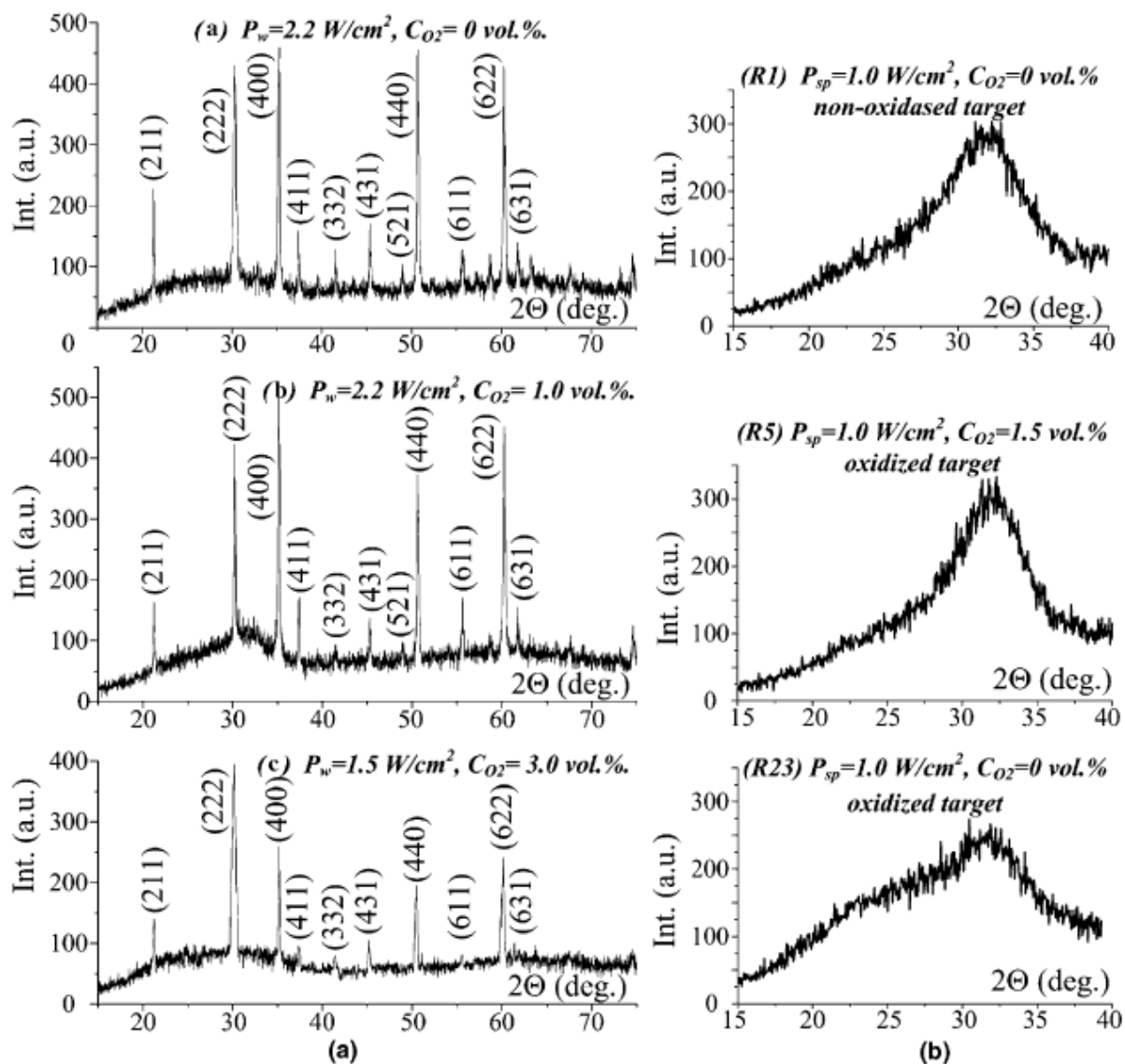


Figure 2.3.3-5 XRD of ITO deposited by RF (a) and DC (b) magnetron sputtering

For this investigation, the ITO is deposited at a temperature of $149^\circ\text{C} \pm 5^\circ\text{C}$, with a thickness of 500Å. The thermo-elastic properties of ITO have been determined by the works of Leterrier and Izumi to be the Elastic Modulus of 199GPa and the CTE of 7.6 ppm/ $^\circ\text{C}$ [Leterrier 2003a].

2.3.4. Summary of Material Properties

This section provides an overall summary of the material properties along with specific process conditions that are pertinent to this investigation. Table 2.3.4-1 below lists the Elastic Modulus, Poisson's ratio, the Coefficient of Thermal Expansion (CTE), thickness of the layer, and deposition temperature.

Table 2.3.4-1 Summary of Material Properties and Process Conditions

Layer	Material	Thickness (um)	Process	Process Temp (C)	Young's Modulus (Gpa)	Poisson's ratio	Density g/cm3	CTE (ppm/C)
Trace	Indium Tin Oxide	0.05	DC Magnetron Sputtering	98	116	0.35	6.8	9.25
Buffer	SiN	0.3	PECVD	180	122.5	0.23	2.5	2.2
Planarization	PTS-R9	2	Spin Coat	200	2.52	0.25	0.959	17.5
Substrate	"PEN"	125	N/A	N/A	3.7	0.33	1.36	21.5

2.4. Internal Fabrication Stress Specific to this Investigation

There are two main forces that contribute to the deformation of a flexible display:

- Internally produced forces
- External forces

Internally produced forces are a result of mechanical stresses introduced during fabrication of the display. External forces from bending, flexing, or folding are usually exerted after fabrication of the device is complete and the detailed analysis

specific to this investigation is discussed in section 2.5 using the ANSYS modeling tool. Section 2.4.1 shall cover the theory of internal stresses and the breakdown of constituent elements. Section 2.4.2 is dedicated to internal stresses when the substrate is stiff when compared to the deposited film versus section 2.4.3 that is dedicated to internal stresses when the substrate is more compliant. Section 2.4.4 shall cover the specific internal stresses unique to the test structures to be used for this investigation using the Coventor finite element analysis tool.

2.4.1. Theory of Internal Stresses

This section covers the theory of internal stresses as a result of fabrication a simple two layer structure. The internal stress acting on a film a result of fabrication is related to the total mismatch strain (ϵ_M) and is defined by equation 2.4.1-1 [Wagner 2005].

$$\epsilon_M = \epsilon_{th} + \epsilon_{rh} + \epsilon_0 \quad (2.4.1-1)$$

There are three main contributions to the total mismatch strain. The first contribution is a result of the strain caused by the substrate and film materials having different thermal expansion coefficients (α_f and α_s) Hence, during fabrication the temperature is elevated while a film is deposited and then when the structure is allowed to cool back down to room temperature, the substrate and film want to contract at different rates. This strain is calculated using equation 2.4.1-2 with T_{dep} being the deposition temperature and T_{room} being room ambient temperature after fabrication.

$$\varepsilon_{th} = (\alpha_f - \alpha_s)x (T_{dep} - T_{room}) \quad (2.4.1-1)$$

The second contribution is a result of strain caused by the substrate and film having different humidity expansion coefficients (β_f and β_s). When a sample is completely dried before vacuum processing and then exposed to ambient air with a specific amount of relative humidity (%RH), the calculation is defined in equation 2.4.1-3 and similar to how the thermal strain is calculated.

$$\varepsilon_{rh} = -(\beta_f - \beta_s)x \%RH \quad (2.4.1-2)$$

Built-in stress originates in films grown with out-of-equilibrium atoms that seek to move to low energy, equilibrium positions. Built-in strain is a function of the radio frequency power used during the plasma enhanced chemical vapor deposition process. Figure 2.4.1-1 shows the relationship of radio frequency power versus built in strain [Long 2006].

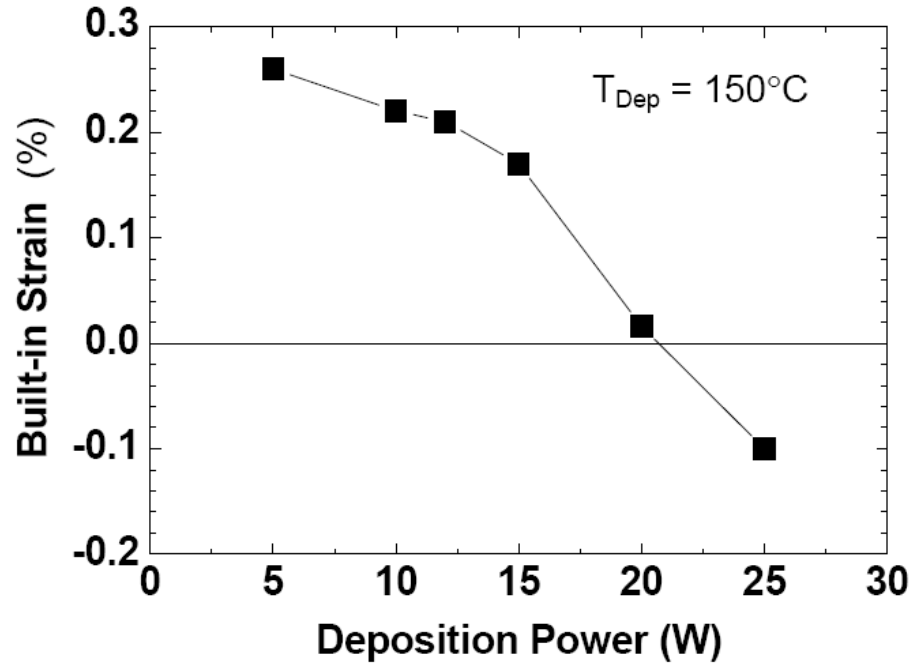


Figure 2.4.1-1 Relationship between Deposition Power and Built-in Strain

2.4.2. Internal Stresses Using a Stiff Substrate

Behavior of a film/substrate structure under stress depends on both the elastic modulus and thickness of the film and substrate (E_f, d_f, E_s, d_s). When the product of ($E_f \times d_f$) \ll ($E_s \times d_s$), then the substrate dominates and the film complies with it resulting in a biaxial stress in the plane of the film. The correlation of film stress to the mismatch strain is defined in Equation 2.4.2-1.

$$\sigma_{film} = \epsilon_M E_f^* \quad (2.4.2-1)$$

Note, E_f^* is the biaxial elastic modulus of the film. Hence, the stress in the substrate is much smaller than the stress in the film thus causing the substrate to bend with a

radius of curvature defined by the Stoney formula shown in Equation 2.4.2-2 [Timoshenko and Goodier 1970]. A standard practice of determining the stress in the film is by measuring the radius of curvature of a given structure and solving the equation below.

$$R = \frac{E_s^* d_s^2}{6\sigma_f d_f} \quad (2.4.2-2)$$

2.4.3. Internal Stresses Using a Compliant Substrate

Conversely to the discussion in 2.4.2, when a film is deposited on a compliant substrate, the substrate also deforms – thus the stress in the film is reduced. If the substrate is held in rigid during deposition, the stress in the film is defined by Equation 2.4.3-1.

$$\sigma_f = \frac{\varepsilon_M E_f^*}{1 + \frac{E_f^* d_f}{E_s^* d_s}} \quad (2.4.3-1)$$

When the substrate is no longer being held rigid (debonded from a rigid oxidized silicon wafer), the substrate may bend significantly. Unlike stiff substrates that use the Stoney formula, the radius of curvature is defined by equation 2.4.3-2.

$$R = \frac{(\bar{E}_s d_s^2 - \bar{E}_f d_f^2)^2 + 4\bar{E}_f \bar{E}_s d_f d_s (d_f + d_s)^2}{6\varepsilon_M (1+\nu) \bar{E}_f d_f d_s (d_f + d_s)} \quad (2.4.3-2)$$

The \bar{E} term in the above equation is the plane strain elastic modulus as defined in equation 2.4.3-3.

$$\bar{E} = \frac{E}{(1-\nu^2)} \quad (2.4.3-3)$$

A comparison was performed between the Stoney formula of Equation 2.4.2-2 and the results of Equation 2.4.3-2 [Gleskova 1998]. There are two subplots, one for a compliant substrate and one for a rigid substrate.

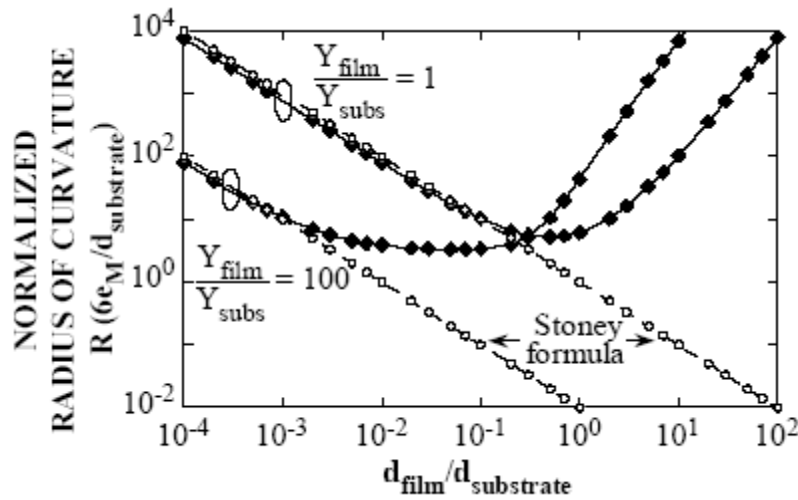


Figure 2.4.3-1 Stoney formula versus Equation 2.4.3-2

2.4.4. Finite Element Analysis of Internal Stresses

Section 2.3 discussed the theory of internal stresses for simple two layer structures consisting of a substrate and a thin film deposited uniformly across the entire substrate. Since the specific structure used for this investigation involves multiple

layers as well as a layer containing specific device geometry, a finite element analysis program has been employed. The SEMulator3D software program is a product from Coventor that is used extensively in the MEMs and 3-D IC manufacturing community. The program allows MEMs designers and process engineers to visualize the effects of design and process modifications in 3-D prior to the fabrication of the device.

The steps involved are first building the device by creating a 3-D model using their Process editor and Material Property database. Starting with the substrate, each layer is defined by the fabrication process used, the material being deposited (along with associated properties), the temperature of deposition, and any geometry defined by a mask for etching of the layer. The next step involves meshing of the 3-D model, followed by the analysis of different stresses using FEA simulation.

Macro-Electronics present unique problems for Finite Element Analysis (FEA) methods since there are drastic aspect ratios resulting from extremely thin films patterned across an entire wafer. Given this cumbersome situation, Coventor allowed the use of their high performance simulation machines in performing the finite element analysis for the specific structures used in this investigation. Figure 2.4.4-1 shows the finite element model of a single ITO on the substrate bent to a radius of curvature as a result of built in stresses from fabrication. Figure 2.4.4-2 is a plot of the principal tensile stress in both the top and bottom ITO layer being approximately 13MPa.

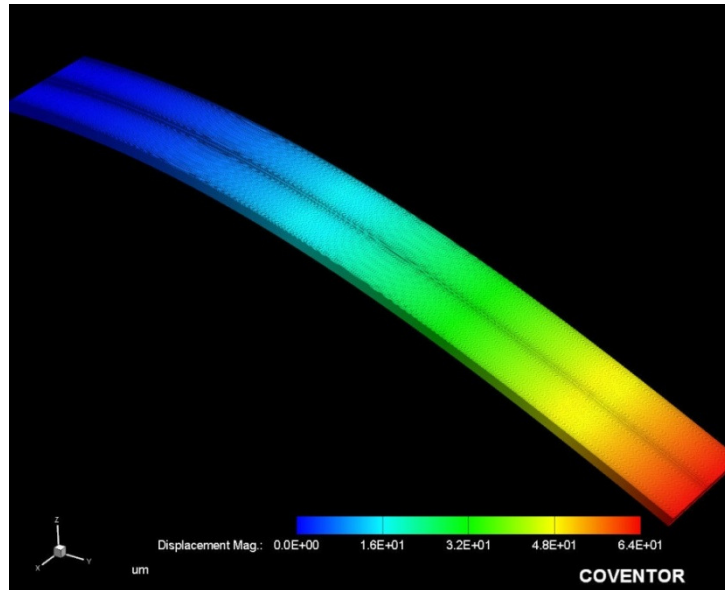


Figure 2.4.4-1 Coventor Finite Element Model of a single ITO strip

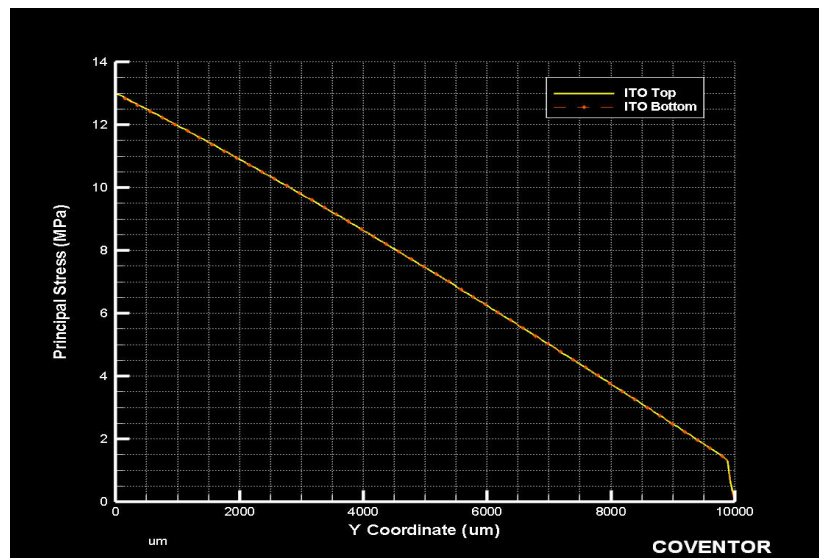


Figure 2.4.4-2 Principal built-in internal stress in ITO film from fabrication

2.5. External Stress and Strain from Bending

Section 2.4 covered the internal stresses as a result of fabrication. This section is devoted to the stresses caused by an externally applied bending moment. Section 2.5.1 introduces the theory behind determining the stress in the film of a simple two layer system. Given that the structure for this investigation is more complicated in terms of multiple layers as well as specific device geometry, a finite element analysis was performed using the ANSYS FEA software and the results are in section 2.5.2. The general approach taken for this section is summarized in Figure 2.5-1.

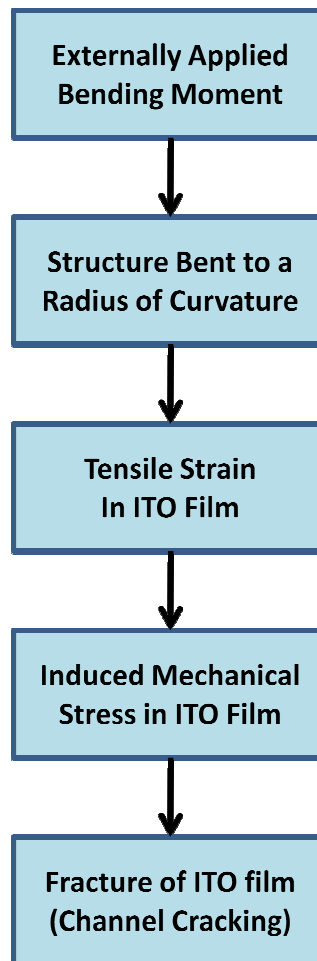


Figure 2.5-1 Relationship of Applied Bending Moments to Film Fracture

2.5.1. Theory based on Simple Two Layer System

When a simple two layer structure is bent to a specific radius of curvature (R) with the film on the outside, the top surface of the film is in tension and the bottom surface is in compression. Inside the structure, there exists a neutral layer that has no strain. Hence, the strain in the top surface can be computed by calculating the distance from the neutral layer divided by the radius of curvature. When the film and substrate have approximately the same Elastic Modulus, then the neutral surface is the midpoint of the structure and Equation 2.5.1-1 reflects this simple calculation.

$$\varepsilon_{top} = \frac{(d_f + d_s)}{2R} \quad (2.5.1-1)$$

When the substrate is more compliant ($E_f > E_s$), the neutral surface shifts from the midpoint towards the film. The strain on the top surface of the film must now be calculated using Equation 2.5.1-2 [Suo 1999].

$$\varepsilon_{top} = \left(\frac{d_f + d_s}{2R} \right) \frac{(1 + 2\eta + X\eta^2)}{(1 + \eta)(1 + X\eta)} \quad (2.5.1-2)$$

The first term is identical to equation 2.5.1-1, but the second term comes into play to compensate for the substrate being more compliant than the film. The term $\eta = d_f/d_s$ and $X = E_f/E_s$.

2.5.2. Results of ANSYS Model

Similar to the discussion on internal stress and strain from section 2.4, section 2.5.1 discussed the theory of strains resulting from an externally applied moment for simple two layer structures consisting of a substrate and a thin film deposited uniformly across the entire substrate. Since the specific structure used for this investigation involves multiple layers as well as a layer containing specific device geometry, a finite element analysis program (ANSYS) has been employed.

Since the structure of the model is based on large aspect ratios (very thin layers comprising a large 6" wafer structure), the Shell 281 Element was employed to allow reasonable simulation times to determine the appropriate stresses. Figure 2.5.2-1 shows the results of the finite element model having an ITO film thickness of 0.05um and bent to a radius of curvature of 0.25".

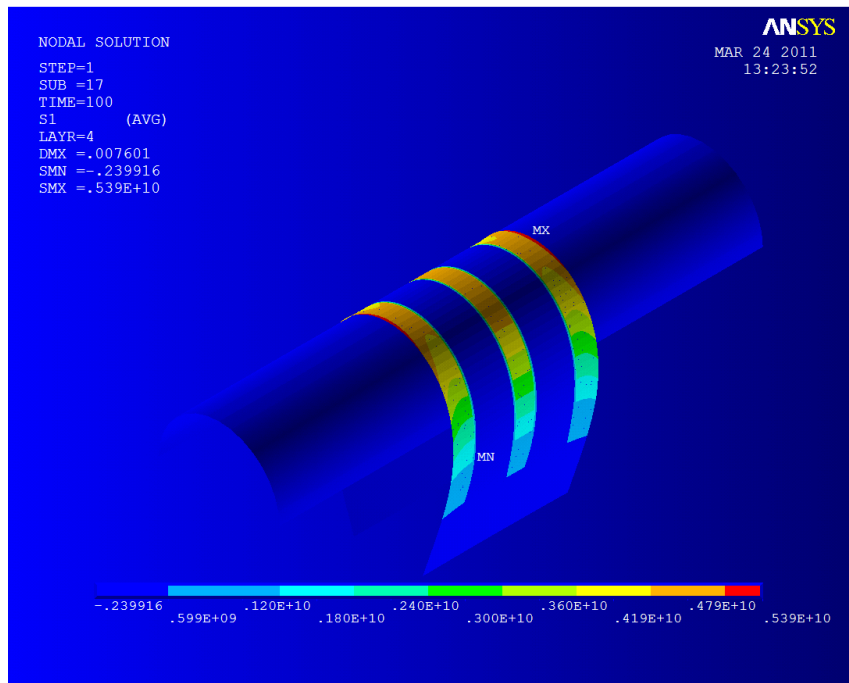


Figure 2.5.2-1 ANSYS FEA of Structure Bent to a Radius of 0.25 Inches.

The model was run varying the radius of curvature and the results of the principal stresses as a function of radius of curvature are plotted in Figure 2.5.2-2.

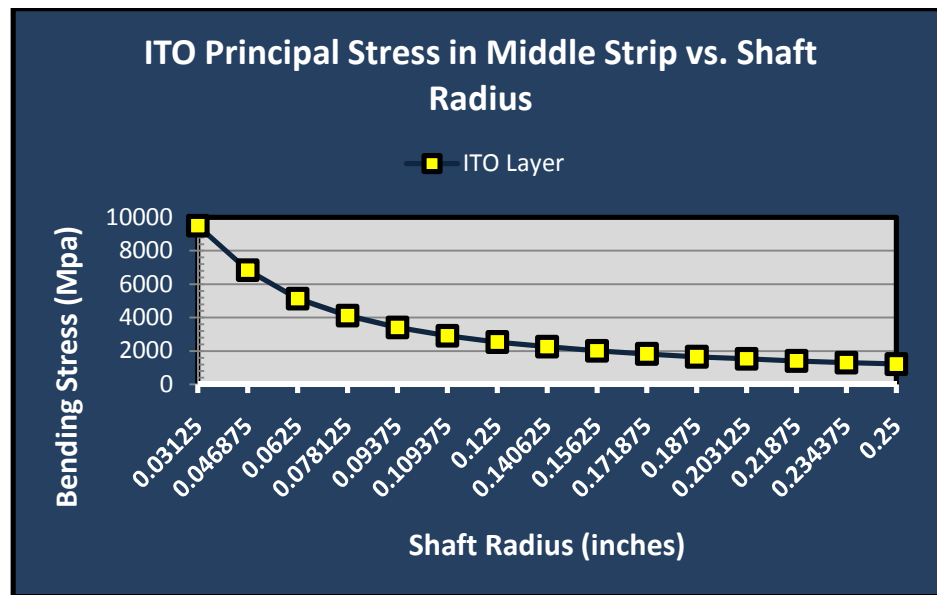


Figure 2.5.2-2 Principal Stress as a Function of Bending Radius

2.6. Summary of Failure Mechanism

The failure mode being researched is the inability to address display pixels due to high impedance on the gate lines of thin film transistors. The high impedance causes a voltage drop between the gate TAB driver and the gate itself thus not meeting the required threshold voltage. At a system level, this appears as parts of the display having individual pixels entire rows of the display becoming non-responsive to new video frame data being sent to the display. The high impedance is a result of cracks in the ITO gate lines that manifest themselves as narrow channels with a high resistance.

As more cracks are introduced, their resistance is summed together like series resistors in a circuit. The failure mechanism is channel cracking of the thin film resulting in an increase in resistance of the ITO based on the number of cracks.

2.6.1. Influence of Key Parameters on Three Different Stresses

There have been three main types of stresses discussed in this chapter: intrinsic critical stress for crack propagation, internal stress from fabrication, and external stress applied to the system. Section 2.2 discussed the concept of a thin film of a material having a particular value for crack resistance (Γ), and knowing this material property along with the other properties of the film and substrate as defined in section 2.3 one can determine the intrinsic critical stress required for crack propagation. Section 2.4 discussed the impact of fabrication parameters on the amount of internal stress in the film and employed the use a finite element model to determine that the ITO gate line interconnects are in tension. Section 2.5 used a different finite element model to determine how much external stress is applied to the ITO gate line interconnects as the structure is bent to a radius of curvature by an external bending moment is applied. Table 2.6.1-1 summarizes the dependencies of key material and fabrication parameters on the three types of stresses.

Table 2.6.1-1 Summary of Key Parameters on the Three Stress Types

	Intrinsic Critical Stress Required for Crack Propagation	Built-in Stress in the Film as a Result of Fabrication	External Stress Induced in the ITO Film as a Result of an External Bending Moment
Thickness (Film)	√	√	√
Thickness (Substrate)		√	√
Young's Modulus (Film)	√	√	√
Young's Modulus (Substrate)	√	√	√
Deposition Temperature		√	
Deposition RF Power		√	
CTE difference (film/substrate)		√	
CTE difference (film/substrate)		√	
Radius of Curvature (from external moment)			√

2.6.2. Summary Calculation of Stresses

Given the theory provided in section 2.2 and the material properties of Table 2.3.4-1, the critical intrinsic stress for crack propagation ($\sigma_{\text{intrinsic}}$) can be estimated by simplifying the structure to be a two layer system. Equation 2.6.2-1 was based on setting equation 2.2.3-1 equal to the crack resistance of the ITO film. Based on tensile testing performed on an ITO/PET structure [Chen 2002], the crack resistance (Γ) of an ITO film has a range of 52-62 (J/m²). Table 2.6.2-1 is a summary of the values to necessary to derive the value of $\sigma_{\text{intrinsic}}$.

$$Z(\alpha, \beta) \frac{\sigma_{\text{intrinsic}}^2 h_f}{E_f} = \Gamma \quad (2.6.2-1)$$

Table 2.6.2-1 Summary of Parameter Values to Calculate Intrinsic Critical Stress.

Parameter	Symbol	Reference	Value
Film Effective Elastic Modulus	\bar{E}_f	Equation 2.2.3-2	132GPa
Substrate Effective Elastic Modulus	\bar{E}_s	Equation 2.2.3-2	4.15GPa
Dundurs Parameter 1	α	Equation 2.2.3-3	0.939
Dundurs Parameter 2	β	Equation 2.2.3-4	0.239
Constraint Factor	Z	Figure 2.2.3-3	14.04
Crack Resistance	Γ	Chen 2002	52-62 (J/m ²)
Film Thickness	h_{film}	Table 2.3.4-1	0.05 (um)

Based on the values in Table 2.6.2-1, the intrinsic critical stress range for crack initiation has been calculated to be between 3,129MPa and 3,416MPa. The internal built-in stress from fabrication was calculated in section 2.4 to be only 13MPa and therefore is negligible in our determination for the amount of external stress needed to be applied to the structure. Based on ANSYS simulations from Figure 2.5.2-2, the radius of curvature for instant initiation of cracks is approximately 3/32". Therefore the execution of a meaningful life test would use mandrels having a radius larger than 3/32".

2.6.3. Conclusions

It is not the intention of this work to characterize the fracture mechanics of crack initiation and crack propagation of thin ITO films on compliant substrates. This has already been studied and the research has been referenced throughout this chapter. Instead of measuring crack characteristics throughout testing, this investigation shall measure the changes in resistance of traces throughout testing as a direct result of thin film cracking. It is these changes in resistance throughout testing under different stress levels that are of importance to characterizing the time to failure of the failure mode.

Chapter 3 highlights previous work on different methods used to investigate fracture in thin films, specifically ITO films on compliant substrates. Chapter 4 is dedicated to taking the investigation one step further by identifying the agent of failure that will be used to conduct a life test at different stress levels. This life test shall be used to obtain time to failure data and be used to create a life-stress model.

Chapter 3: Previous Reported Investigations

3. Overview

In general, previous works can be categorized by the test approach for stressing the test specimen. The first approach is employed to determine the maximum strain a device can be subjected to until failure. The second approach involves cyclic bending of a test specimen from a relaxed state to a stressed state that is defined as a set strain value and determines the number of cycles to failure.

In addition to the types of test methods employed, the type of test structure is another discriminating factor in terms of differentiating previous works. Most work has been performed on the test structure having the layer ITO being uniform across the entire the substrate, the works presented in sections 3.1 through 3.1.6 and 3.2 apply to this type of test structure. Section 3.1.7 covers the majority of works that have been performed on patterned ITO lines on flexible substrates. Some of the most recent tests related to flexible display materials that employ cyclic bending are targeted at overall device performance and not individual interconnects [Chen 2011, Dey 2010, Duan 2009].

3.1. Strain to failure methods

For strain to failure methods, the notion of crack onset strain (COS) has been historically defined as the specific value of strain that results in a 10% change in resistance of the conductive specimen. Figure 3.1-1 provides a graphical

representation of crack onset strain whereby the X axis represents strain and the Y axis is percent change in resistance. Under this approach there are three main methods: uniaxial tensile, two point bending, and biaxial. Section 3.1.1 through 3.1.3 covers these methods respectively. Each method has its advantages and drawbacks depending on what the main intent of the test is attempting to accomplish. Section 3.1.4 provides a discussion of observations from each of the three methods. Section 3.1.5 summarizes the analysis of the data while 3.1.6 provides a discussion on the analysis of fragmentation length.

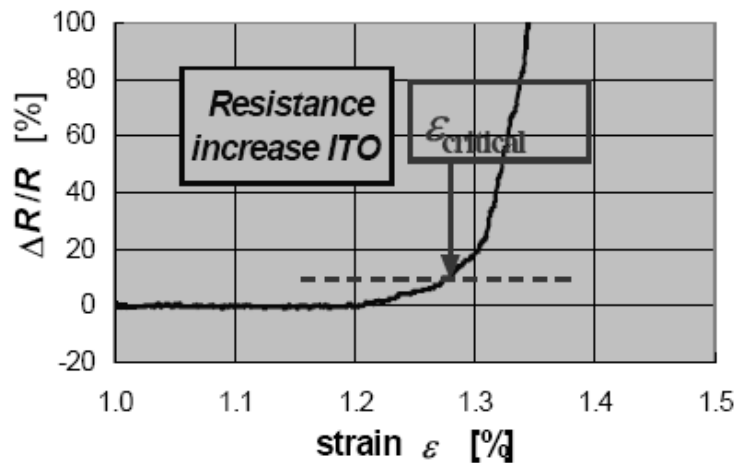


Figure 3.1-1 Graphical representation of historical COS

3.1.1. Uniaxial Tensile method

In the area of tensile testing, there have a multiple methods to inducing strain and monitoring the specimen under test. The first method, called uniaxial fragmentation test is highlighted in Figure 3.1.1-1 and Figure 3.1.1-2. In this method, a film specimen is attached at both ends to clamps and slowly pulled apart. It is loaded in

tension in situ under a microscope and therefore can be visually inspected for crack initiation and propagation while simultaneously monitoring changes in resistance. Although this method is tedious, it does allow for precise monitoring and observation of the failure process while under strain.

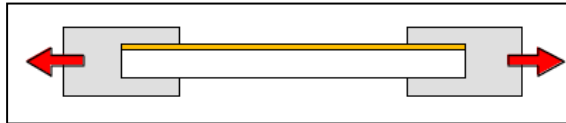


Figure 3.1.1-1 Overview sketch showing uniaxial testing method

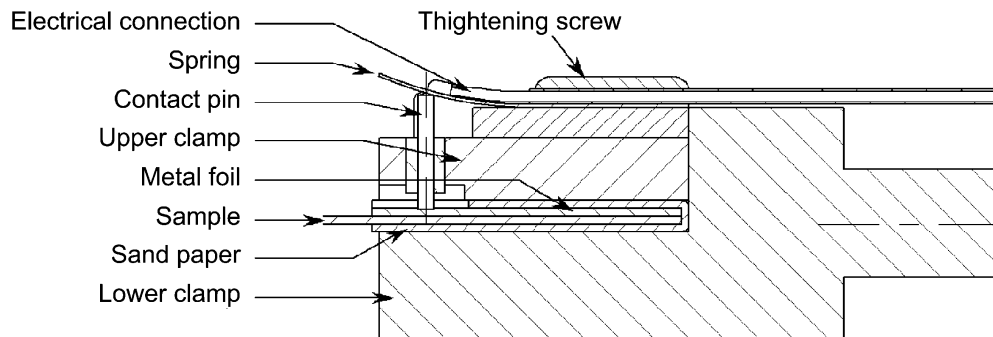


Figure 3.1.1-2 Detailed mounting sketch for uniaxial testing method

3.1.2. Two point bending method

The next method involves the installation of the test specimen between two parallel plates and is termed the two-point bending technique [Bouten 2002]. The test system

moves either one or both plates closer together and as such places the test specimen under a radius of curvature. With the film deposited on the outer surface, it is stressed in tension while the inner surface (substrate) is placed in compression as shown in Figure 3.1.2-1.

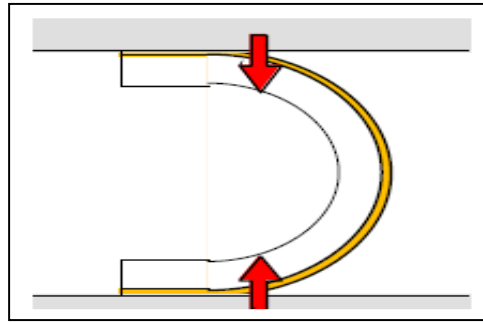


Figure 3.1.2-1 Sketch of two point bending method

The amount of strain varies across the specimen with the maximum amount of strain in the middle of the sample between the two plates. This method allows for the electrical monitoring of changes in resistance as a function of distance between the two parallel plates which correlates to a specific amount of strain. Similar to the tensile method, this method is also used to determine the critical strain to failure. However, it is not well suited for direct observation of the test structure while under strain and therefore does not require sophisticated image capturing techniques and is best implemented for testing conductive coatings such as ITO. The benefits are that it is faster than the tensile method and can be easily automated allowing for multiple cycles if necessary. The drawbacks include first that the strain is not uniform across the entire test structure. As the plates are drawn closer together, more of the test specimen shall become parallel to the plates and a smaller portion shall be bent to a set radius of curvature. The second drawback is that the system does not allow for the

specimen to be placed in a completely relaxed position since it has to be mounted to both of the parallel plates.

3.1.3. Biaxial method

The biaxial method is another approach that determines the failure process under two dimensional loading by employing the bulge cell methodology [Leterrier 2001 and Anderson 2003]. This method is shown in Figure 3.1.3-1 and Figure 3.1.3-2 and employs clamps that hold the substrate edges while pressurized gas is injected beneath the substrate causing it to bulge in the center [Hsu 2002].

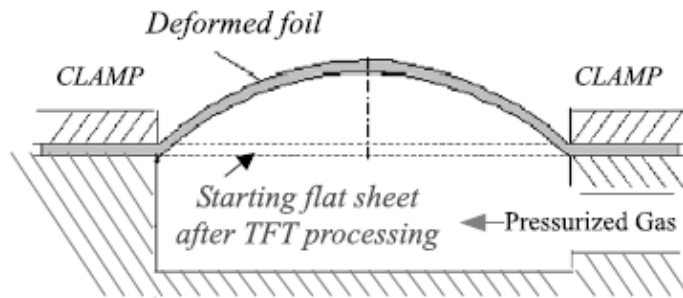


Figure 3.1.3-1 Sketch of bulge test method

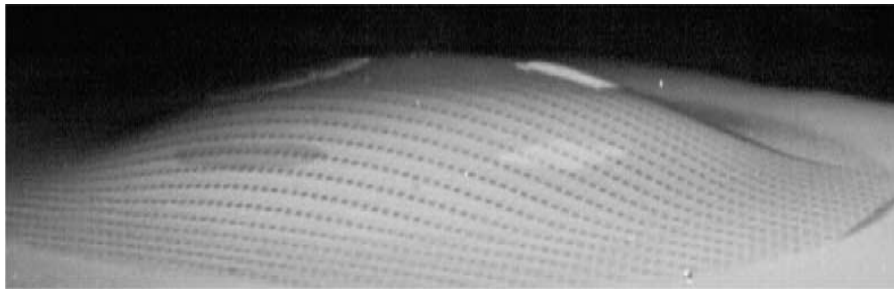


Figure 3.1.3-2 Polyimide foil with a-Si/SiN islands after deformation

3.1.4. Observations of failure patterns for the three methods:

Using 100nm thick ITO coating on a hard coated polymer substrate, the uniaxial test method captured images. As a result of localized stress concentrations, defect sites are originated and become the initial sites of the first cracks in the ITO when the specimen is subjected to strain. Both crack density and crack propagation are functions of the amount of strain in the specimen. These cracks are allowed to propagate perpendicular to the direction of tension [Leterrier 2004] from the defect sites. Eventually these cracks become unstable and eventually span the entire length of the sample width with a density greater than 100/nm as shown in Figure 3.1.4-1, note that the arrow in (b) indicates the failure initiation from a coating defect. The transition from crack growth to unstable propagation occurs roughly when the length of the crack becomes several hundred times greater than the thickness of the coating.

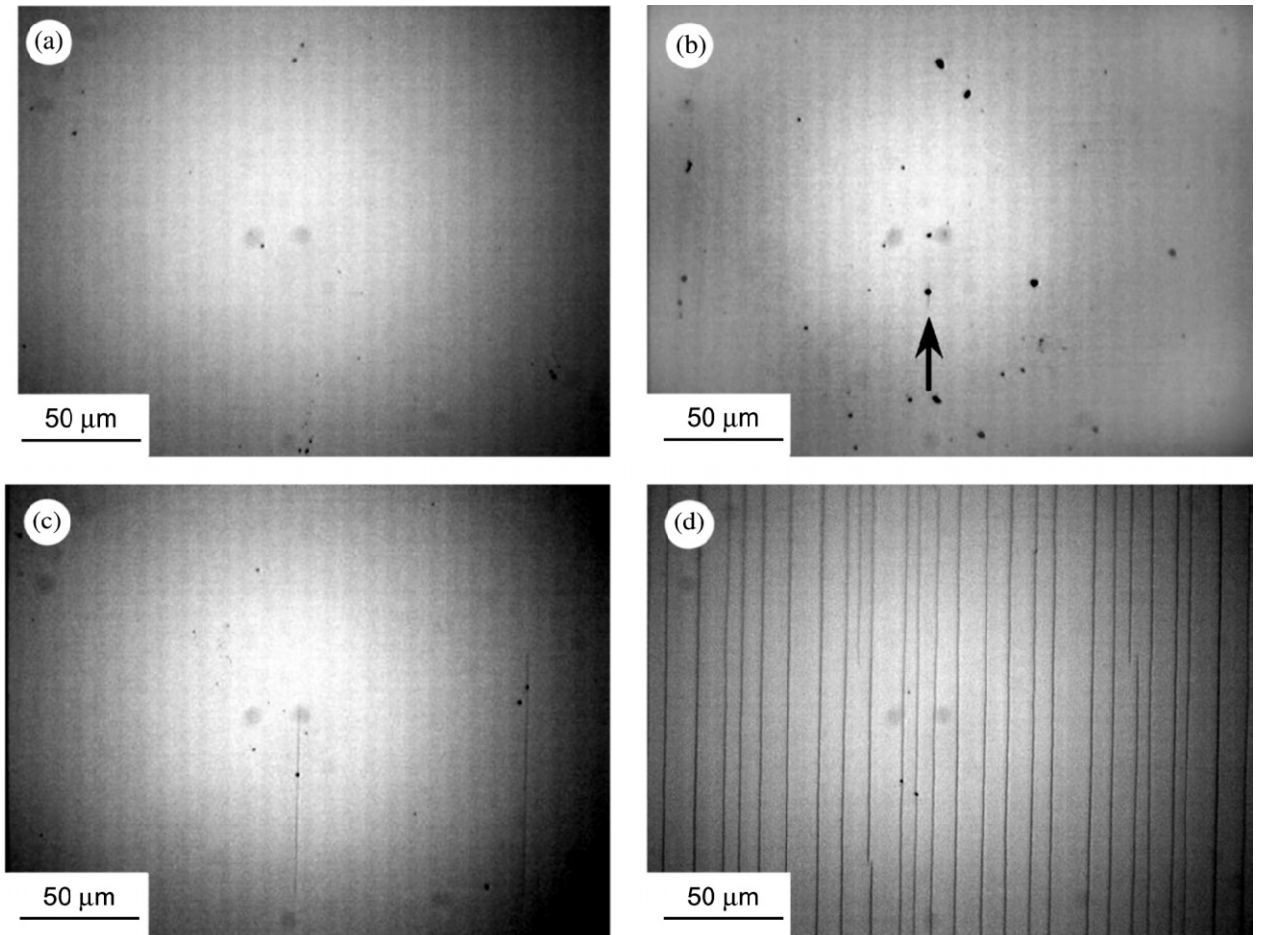


Figure 3.1.4-1 Cracking of ITO under % strain: 0 (a); 1.28 (b); 1.42 (c); 3.42 (d)

The biaxial loading reflects a different failure pattern as shown in Figure 3.1.4-2. Here cracks still originate from defect sites, but propagate with curved trajectories instead of being horizontal to each other in tensile or two-point bending systems. The cracks continue to propagate until reaching other cracks in which they intercept each other at roughly right angles [Anderson 2003].

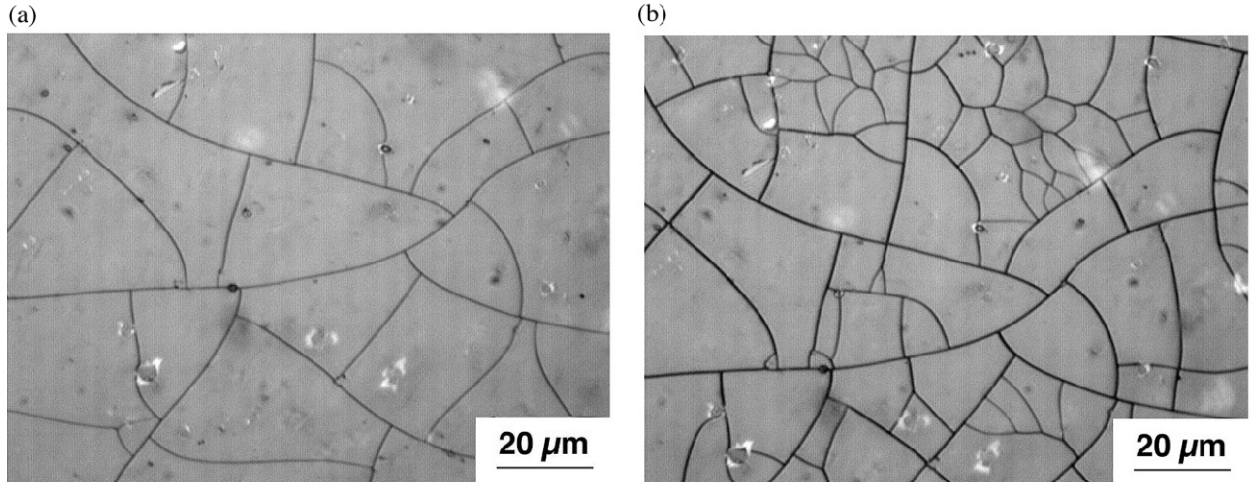


Figure 3.1.4-2 Fragmentation of SiOx coating under strain: 2.6% (a) and 3.6% (b)

3.1.5. Analysis of results between Uniaxial and Two Point Bending

Results for determining crack onset strain using both the Uniaxial and two point bending method were compared and shown to have similar results. Table 3.1.5-1 reflects not only similar results but also the influence of ITO thickness on the COS for both methods [Crawford 2005].

Table 3.1.5-1 Crack onset Strain (COS) of ITO layers

ITO thickness (nm)	Uniaxial COS	Two point bending COS
50	1.77	1.83
100	1.45	1.42
200	1.56	1.45

3.1.6. Analysis of Fragment Length

Using visual observation during tensile uniaxial load on specimens with 105nm thick ITO coated via DC magnetron sputtering on a 125um thick PET substrates, an analysis of fragment length (the distance between two horizontal cracks in the ITO) was performed. Figure 3.1.6-1 shows that fragment length decreases with increasing strain. In this figure, lines were drawn over the cracks in the figure to improve the presentation [Cairns 2000B].

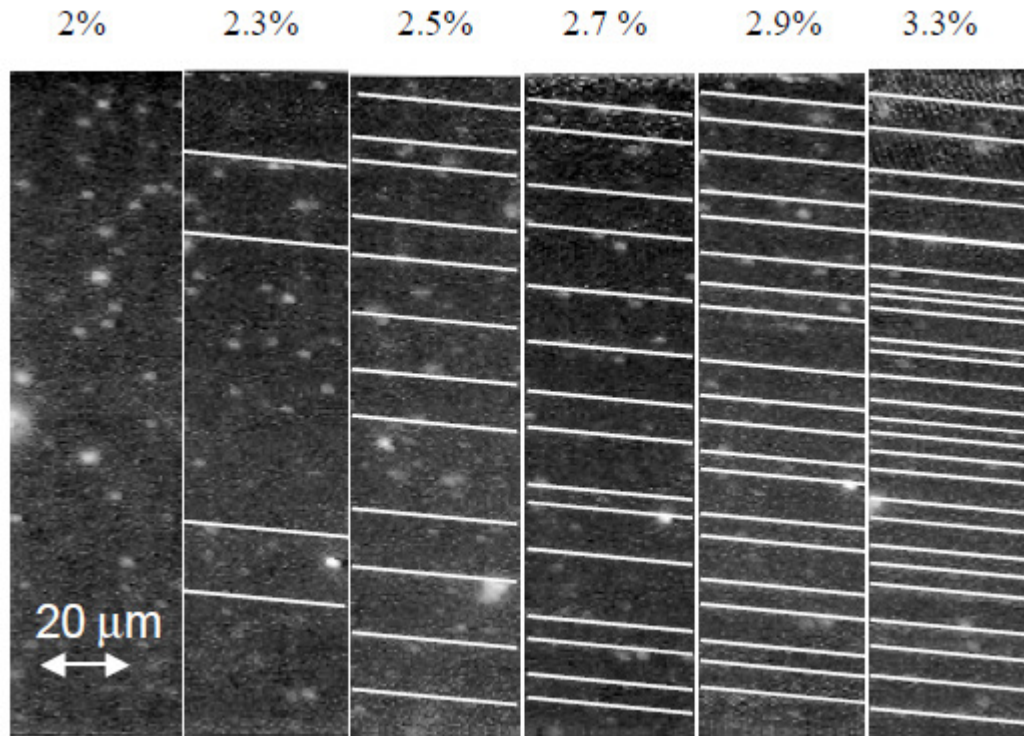


Figure 3.1.6-1 Fragmentation patterns of ITO with increasing strain

3.1.7. Patterned ITO lines on flexible substrates

As previously discussed, ITO is commonly used as a transparent anode layer that is common to all pixel elements. However, in some applications for transparent display applications interconnect lines are patterned out of ITO. The behavior of these patterned lines differs from those of uniform layers. The two point bending method was employed to obtain COS data on ITO line widths of 10, 30, 100, and 300 μm [Crawford 2005].

As evident in Table 3.1.7-1 the COS was shown to follow a systematic increase with decreasing line width. Based on 30 samples for each of the line widths, the data was

fit to Weibull plots and the data reflected a larger scatter for the narrower lines as evident by the lower modulus values.

Table 3.1.7-1 COS and modulus for different ITO trace widths

Width (um)	Crack Onset Strain
10	1.35
30	1.29
100	1.22
300	1.19

3.2. Cyclic Testing Method

The previous works discussed in section 3.1 were centered on determining the maximum strain a device can be subjected to until the resistance changes 10% or more which is commonly termed crack onset strain. The other important factor is how many cycles can a device be subjected to at a specific strain until failure. This becomes important when considering the reliability in service while the device is undergoing repeated deformation in the field.

Here a cyclic loading rig was designed as outlined in Figure 3.2-1. This figure reflects a system that allows for bending the sample around a mandrel and then allows the sample to return to its relaxed horizontal state by having a low tension spring attached to one end of the substrate while the other is fastened to the mandrel. Electrical connections are made to the ITO uniform layer by thin copper tape and measure the end to end resistance across the entire uniform ITO coating by use of a multimeter. The data from the multimeter is captured at specific intervals by the control computer.

This computer also controls the rotation of a stepper motor which in turn controls the smooth rotation of the mandrel via a timing belt [Gorkhali 2004].

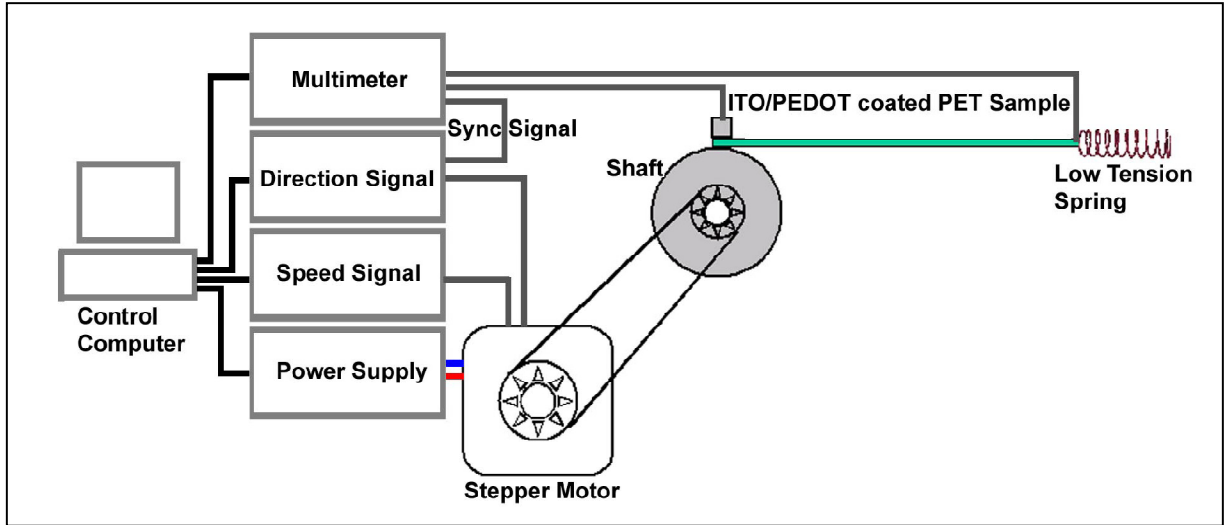


Figure 3.2-1 Sketch of cyclic mandrel test method

The test was executed on several mandrel sizes and the resistance of the ITO coated PET test specimen was monitored throughout the cyclic test and the percent change in resistance as a function of number of cycles is provided in Figure 3.2-2 and Figure 3.2-3. As is evident by the graph, there are three regimes of resistance change. First increased resistance due to changes in sample dimension until equilibrium width is obtained (50-100 cycles). Second, gradual linear increase in resistance from number of cracks developing in the specimen. Third, catastrophic failure of the sample due to severe cracking.

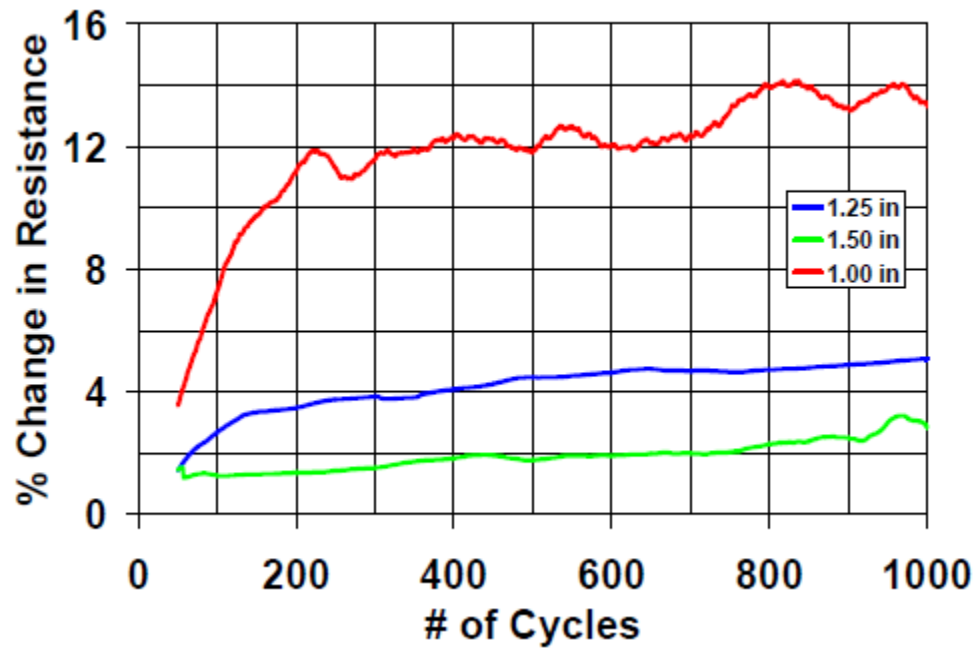


Figure 3.2-2 Resistance change per cycle for three mandrel sizes

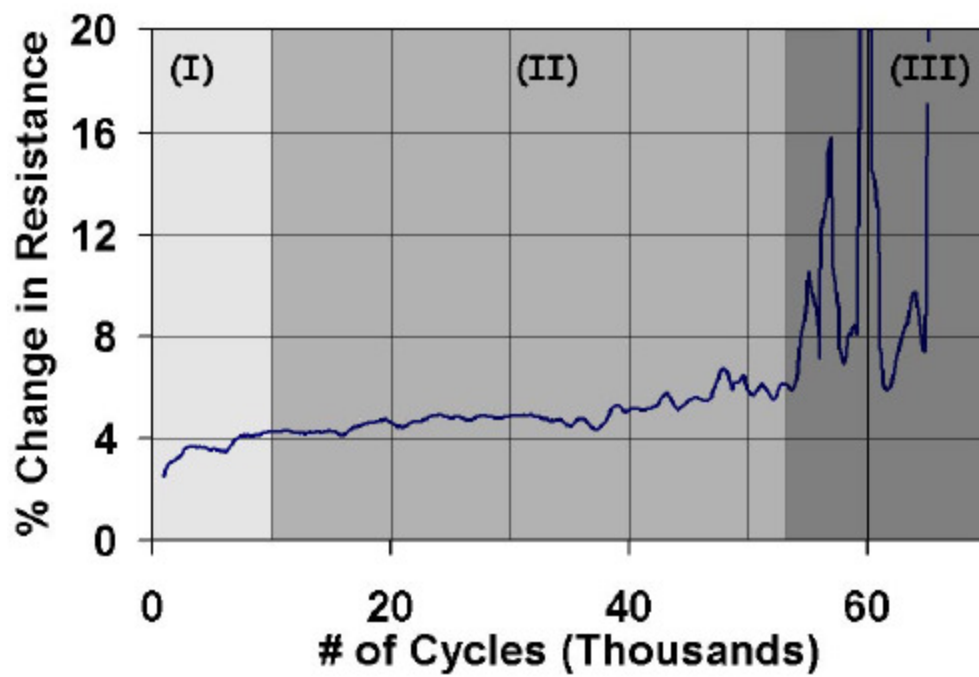


Figure 3.2-3 Resistance change per cycle showing three regimes of change

3.3. Critique of Previous Investigations

To date there have been significant strides in testing conductive coatings on flexible substrates. However, there are two main attributes of the testing, which if improved, would greatly enhance the meaningfulness of the testing. The first attribute is the notion of failure being historically defined as a 10% increase in resistance. It is apparent from the SPICE model in chapter that a 10% increase in resistance of the gate line interconnect is not enough to prevent effective biasing of the thin film transistors. Therefore, the failure criteria of the tests should be based on a meaningful resistance change that would actually prevent correct operation of the end item product.

The second attribute is the methodology of the test execution. The uniaxial, biaxial, and two point bending system are all relevant with respect to determining the crack onset strain for both uniform and patterned layers. However, these methods all lack the means for determining cycles to failure of the ITO-substrate structure when subjected to actual bending conditions in the field.

Hence, the cyclic mandrel method was employed to accurately capture resistance changes with respect to the number of cycles executed. However, the main drawback was that it focused on a uniform ITO layer only and lacked the ability to efficiently capture cycle to failure data for patterned ITO lines. The benefits and drawbacks of these methods are summarized in Table 3.3-1.

Table 3.3-1 Comparison of different test methods

Test method	Film structure	Result	Advantages	Drawbacks
Uniaxial Tensile	uniform film	COS and fragment length	direct observation of failure process	manual process
Two point bending	uniform film patterned lines	COS	fast and able to automate	limited to conductive coatings
Biaxial (Bulge)	uniform film	COS and failure patterns	conformal one time plastic deformation	Not applicable to standard applications
Cyclic Mandrel	uniform film	Resistance as a function of cycles	applicable to field use conditions	limited to uniform film

3.4. Rationale for Performing an Accelerated Life Test

It is apparent that a need is present for a new test to be performed that uses the cyclic mandrel method on patterned ITO traces. The results from this test can then be used to capture Time to Failure (TTF) data in order to better characterize the life-stress relationship for the failure mode of high impedance gate line interconnects.

In order for the test data to be meaningful and the data to be gathered in a reasonable amount of time, an Accelerated Life Test (ALT) needs to be designed. Chapter 4 is dedicated to the design of the ALT that was executed as part of this investigation. Chapter 5 is dedicated to the design and fabrication of the test system used to accurately capture in real time the changes in resistance of the ITO traces representing gate line interconnects while under cyclic loading.

Chapter 4: Design of Accelerated Life Test

4. Overview

This section addresses the design of an Accelerated Life Test (ALT) for the purpose of supporting this specific study. This section is broken into several sub-sections that walks through the design of the particular attributes of the accelerated life test used in this research. The first sub-section discusses the rationale of performing an accelerated life test followed by general guidelines for designing one. Section 4.3 is a discussion on failure mechanism as discussed in chapter 2 and how this mechanism can be accelerated. Here the term “agent of failure” is introduced to describe the type of stress application and the method of acceleration in context to this thesis. Section 4.4 is a detailed discussion of cyclic fatigue and why it was chosen as the agent of failure for the accelerated life test being performed for this study. The discussion continues with the requirements for the test structures to be designed and fabricated in support of this accelerated life test. The final section summarizes with a breakdown of the flow starting with the observed failure mode to the underlying failure mechanism and relating it to the agent of failure and acceleration method.

4.1. Rationale for Accelerated Life Testing

Prior to the advent of reliability engineering, industry would design, fabricate, and deliver products into the field and then wait for extended periods of time for those devices to fail to gather time to failure data and infer the products reliability. The

drawbacks to this approach are numerous in that sometimes not all failures are returned, the field stress conditions are not completely known, and product reliability is not quantified until after an extended period of time of the customer using it and then it could result in a company getting a bad reputation for delivering unreliable products.

One solution is a developer would run a controlled reliability life test prior to delivery of a product. Here one is able to control the stress conditions and analyze every failure that occurs. In general, the purpose of performing life testing is to understand failure modes and failure mechanisms of a product and assess the reliability prior to introducing it into the field. Depending on the failures found in life testing, failure analysis may be performed to determine root cause and design changes are made to eliminate specific failure modes from the design.

A drawback to this method is that the testing could take years to collect relevant data and pressure may be on the team to deliver the product prior to completion of the life test.

In order to obtain results faster and thus implement corrective actions in the product prior to full scale production, accelerated testing was developed. There are two main types of accelerated tests: (1) the elephant test and (2) the accelerated life test (ALT). Both tests use increased stress to shorten test time, but the elephant test is a single very high level of stress used to reveal a failure condition or give the design team confidence in the product. One could think of an elephant test as having a pass/fail

criteria. The second method, the accelerated life test is used to assess reliability or component life by performing the test at stress levels higher than those assumed to be experienced in the field, but are still within reasonable bounds of operation. This process is done by obtaining time to failure data and fitting it to a particular life distribution. When the test is conducted at different levels of stress, one can then extrapolate the multiple life distributions to a life-stress model. This life-stress model can be used to estimate the reliability at different stress levels to include the lower stress levels as expected to be observed in the field. A graphical example showing how this is done is provided in Figure 4.1-1 [Modarres 2006].

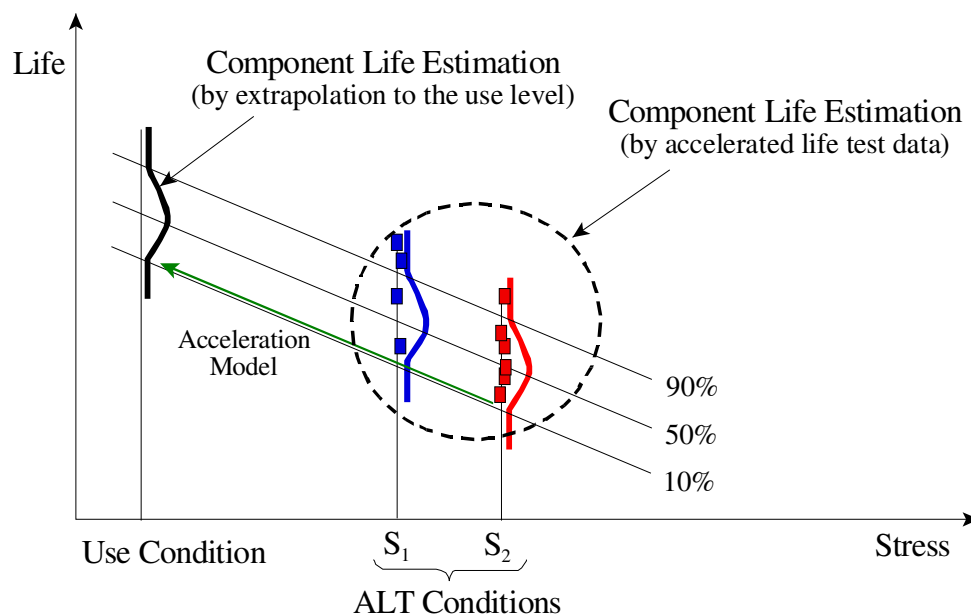


Figure 4.1-1 Graphical example of component life at different stress levels

In summary, the benefits of performing ALT is due to the fact that the testing results in gathering time to failure data in a controlled and rapid or accelerated manner. An accelerated life test can be used for the following purposes:

- Discover failures, perform root cause analysis and implement corrective actions during design stage
- Perform trade studies / compare different materials or manufacturing processes
- Assess component or system reliability prior to product release

4.2. Key Components of an Accelerated Life Test

The key to a successful ALT is to reduce the test time by increase stress levels. These stress levels are higher than those seen under normal operating conditions, but cannot be too high. If the stress levels are too high, then one runs the risk of introducing new failure mechanisms / failure modes that are not relevant to real operational conditions. Therefore, in order to design a good accelerated life test, one needs to understand the failure mechanism that is behind the failure mode, this task has already been performed in chapter 2 of this document. Once the failure mechanism is identified, a study needs to done to determine what triggers or accelerates this failure mechanism, this trigger is termed the “agent of failure”. Identifying and understanding the agent of failure is the key to designing and executing a good accelerated life test.

4.2.1. Types of Responses

With respect to how a test specimen responds while subjected to an accelerated life test, there are two main ways to view the process. The first is an accelerated

degradation test whereby one is measuring how the output or performance of a device changes over time. One has to define the failure threshold based upon a specific degraded level of operation. An example of this would be performing a life test on a fluorescent bulb. Initially the bulb is producing 200 foot lamberts of light. As the test continues the phosphor inside the bulb degrades over time resulting in less light output. A failure threshold would be defined based upon the end use application such as the bulb degrading to a point of only producing 100 foot lamberts.

The second type is based on a failure event. Here failure time or the interval containing the failure time is captured. Using the above example, one would not define failure based upon degraded light output, but based upon the bulb to no longer turn on. This could be a result of the bulb cracking or the filaments inside the bulb breaking and not being able to support an arc inside the fluorescent tube.

In this study the increasing impedance of the gate line interconnect is of key importance. SPICE modeling has determined a failure threshold of 400k Ohms as defined in section 1.8. Therefore the testing needs to monitor the increasing impedance of these interconnect lines starting from their initial value after fabrication up until the failure threshold is realized.

4.2.2. Acceleration Models

Since the purpose of performing an acceleration life test is to eventually predict the reliability of the product in the field under less stressful conditions, a mathematical model is created as a result of the data obtained from testing. The model needs to

provide a relationship between the acceleration variable and time to failure. Therefore, models fall into two main categories:

- Physical Acceleration Models
- Empirical Acceleration Models

An example of a physical acceleration model would be a fracture mechanics investigation defining crack initiation and propagation in a steel specimen under certain stress conditions.

If during a test, one does not exactly monitor the physical attribute of the root cause throughout the test, then the empirical model may be employed instead of a physical model [Ohring]. An example of this is the MIL-HDBK-217 method for prediction reliability of a resistor based upon the external operating temperature and the ratio of power dissipated to the rated power of the device. [MIL-HDBK-217]

In the instance of this study, the failure mechanism of channel cracking of the ITO gate line interconnects is the root cause for increasing impedance that results in observed line outs in the display. It is inferred that the increasing size and density of the channel cracks throughout the life test result in increasing the impedance of the interconnects. Therefore, the increasing impedance of the interconnects shall be monitored throughout the testing until it reaches the failure threshold. Since this study is not an investigation of the fracture mechanics behind the characterizing crack initiation and crack propagation of the channel cracks, direct visual observation of

cracks in the ITO traces is not relevant to this study and therefore an empirical acceleration model shall be used to characterize the life –stress relationship.

4.2.3. Acceleration Factor

The acceleration factor is a unit-less value that provides a correlation between a device under test at one stress level (usually normal use conditions) to another device under test exposed to a higher stress level (usually a reliability life test) as defined in equation 4.2.3-1.

$$AF = \frac{L_u}{L_a} \quad (4.2.3-1)$$

- AF is defined as the Acceleration Factor
- L_u is defined as the device life under normal use conditions
- L_a is defined as the device life under higher (accelerated) stress conditions

The acceleration factor for a device that follows an inverse power relationship between stress and life can be defined by equation 4.2.3-2 [Nelson 1990]. More detail of this relationship and the relevance to the actual time to failure data acquired from the acceleration life test performed shall be discussed in chapter 7 of this document.

$$AF = \left[\frac{V^u}{V^a} \right]^n \quad (4.2.3-2)$$

- V^u is defined as stress under normal use conditions

- V^a is defined as the stress under an accelerated life test condition
- n is defined as the power law exponent

As the acceleration factor is increased, the total test time is reduced. One needs to balance the need for a fast test with high acceleration factors with the requirement to obtain relevant failures by not introducing new failure mechanisms that are not germane to the investigation.

4.3. Accelerating the Failure Mechanism

The failure mechanism was discussed in Section 2, but only in the context of understanding how the specific failure mode is caused. With respect to designing an accelerated life test, an overview of failure mechanisms needs to be covered again since it is imperative to understand the different types of failure mechanisms and how they are accelerated by different agents of failure. The formal definition of a failure mechanism is physical process that is either caused by stress or eventually leads to stress. A failure mechanism involves an agent of failure and results in reducing the stress or endurance of a material or device.

4.3.1. Types of Failure Mechanisms

There are numerous types of failure mechanisms and to list them all is beyond the scope of this discussion. However, in designing an accelerated life test, one needs to understand the type of failure mechanisms being investigated in order to apply the correct stress to accelerate it. Table 4.3.1-1 is a sample listing of failure mechanisms

along with the impact of these failure mechanisms of the device under test. The third column lists the type of stress that exacerbates the failure mechanism such. Stress-Induced Mechanisms are caused by or are the result of localized stresses (permanent or temporary) in the device under test. Strength-Reduced Mechanisms are the result of the failure mechanism reducing the strength or damage endurance of the device under test.

Table 4.3.1-1 Categorization of Failure Mechanisms and Related Stresses

Failure Mechanism	Stress-Strength Relationship	Type of Applied Stress
Creep	Causes Reduction in Strength	Thermal
Fracture	Result of Localized Stress	Mechanical
Corrosion	Causes Reduction in Strength	Chemical
Buckling	Result of Localized Stress	Mechanical
Radiation Damage	Causes Reduction in Strength	Radiation
Wear	Causes Reduction in Strength	Mechanical

For this investigation, the failure mechanism is fatigue induced channel cracking (fracture) of the ITO gate interconnect lines that are a result of localized stresses in the ITO material from mechanical stress.

4.3.2. Types of Applied Stress (Agent of Failure)

When a device or material is exposed to a stress, the combination of the stress along with the exposure time to the applied stress work together to provide more opportunity for damage to be accumulated in the device or material under test. Stress comes in many forms and multiple stresses many work in tandem to synergistically accelerate a particular failure mechanism. A partial listing of stress types is as follows:

- Mechanical
- Thermal
- Electromagnetic
- Chemical
- Radiation
- Synergistic Combination of above stress groups

For this investigation, mechanical stress is the agent of failure and shall be the critical element in accelerating the failure mechanism for the acceleration life test since the test is attempting to duplicate field use conditions of physically flexing a display by the end user.

4.3.3. Methods for Applying Stress

In addition to the types of stresses, there are numerous methods to apply a specific stress. The following are the four main methods for applying a stress when executing an accelerated life test:

- Constant
- Step
- Cyclic
- Random

Constant stress is where the stress level is applied and does not change throughout the entire life test. Step stress is where successive higher levels of stress is applied as the test evolves. Cyclic stress is defined as a repetitive act of taking a test specimen in the unstressed state, then applying the specific stress for a set duration, and then removing the stress. This process is repeated throughout the entire life test. Finally, random stress testing involves applying randomly generated levels of stress throughout the test. Random vibration testing is common form of this type of stress

testing. For this investigation, application of the cyclic stress method shall be employed. A detailed analysis of the cyclic stresses to be applied shall be examined in section 4.4 herein.

4.3.4. Methods of Acceleration

The act of accelerating the testing is the key point in performing an accelerated life test. Once the failure mechanism, associated stress, and means of applying the stress have been determined the final step is deciding the optimum method to compress the test time. There are several methods that can be employed in isolation or in concert with one another to help compress test time while still collecting relevant failures. One type of acceleration would be to decrease the strength of the test structure from the original product that one is attempting to characterize by reducing the device size, altering device geometry critical to the failure mechanism, changing materials, or changing protective finishes. Of course it would be necessary to fully understand the impact of that these differences have in terms of expected life when one tries to extrapolate the life-stress model to the reliability of the actual product.

Another approach would be to keep the test structure identical to the original product in terms of size, geometry, materials, and finishes; but instead increase attributes of the test regime with respect to actual field use conditions. The three main attributes of the test regime that are usually performed are:

- Increasing the use rate
- Increasing the age rate
- Increasing the stress level

An example of increasing the use rate would be subjecting the test structure to a stress every hour instead of the normal stress exposure that occurs in the field (such as once a day). This would compress the test time by a factor of 24. An example of increasing the age rate would be to increase the exposure to higher temperatures or humidity levels than normally seen in the field to accelerate the chemical processes that trigger the known failure mechanism. Examples of Increasing the level of stress would be applying higher than expected voltage, pressure, or strain to the test structure than would be seen in actual field conditions.

For this investigation, the accelerated life test shall increase both the use rate as well as the stress level to compress test time. Under normal field use conditions, the display may be rolled and unrolled an average of 20 times per day. The test fixture (specifics defined in chapter 5) shall roll and unroll the test structure several hundred times per day. In addition to the increased use rate, the stress levels shall also be increased by imparting higher strain levels from bending the test structures around mandrels having a tighter radius of curvature. Equation 4.3.5-1 shows the function of increased gate interconnect resistance (R) as a function of the acceleration factors, higher stress (σ) and higher cyclic use rate (N).

$$\frac{\Delta R}{R} = f(\sigma, N) \quad (4.3.4-1)$$

4.4. Cyclic Fatigue as the Specific Method of Acceleration

Section 4.3 walked through the key attributes of designing a good accelerated life test by first identifying the agent of failure (stress that induces the failure mechanism), then determining the method for the applying the identified stress to the test structure, and finally the methods of accelerating the test as summarized below:

- Failure Mechanism – Fatigue induced Channel Cracking (Fracture)
- Agent of Failure – Mechanical Stress
- Application of Stress – Cyclic Loading
- Method of Acceleration – Increased Stress Level and Increased Use Rate

4.4.1. Constant Amplitude Cyclic Loading

Since the actual field use condition is the repetitive act of rolling and un-rolling the flexible display like a scroll, the accelerated life test shall apply the stress in a cyclic manner.

Figure 4.4.1-1 is a sketch of a generic profile for two cycles of constant amplitude cyclic loading. Equations 4.4.1-1 through 4.4.1-6 are standard definitions for this type of testing.

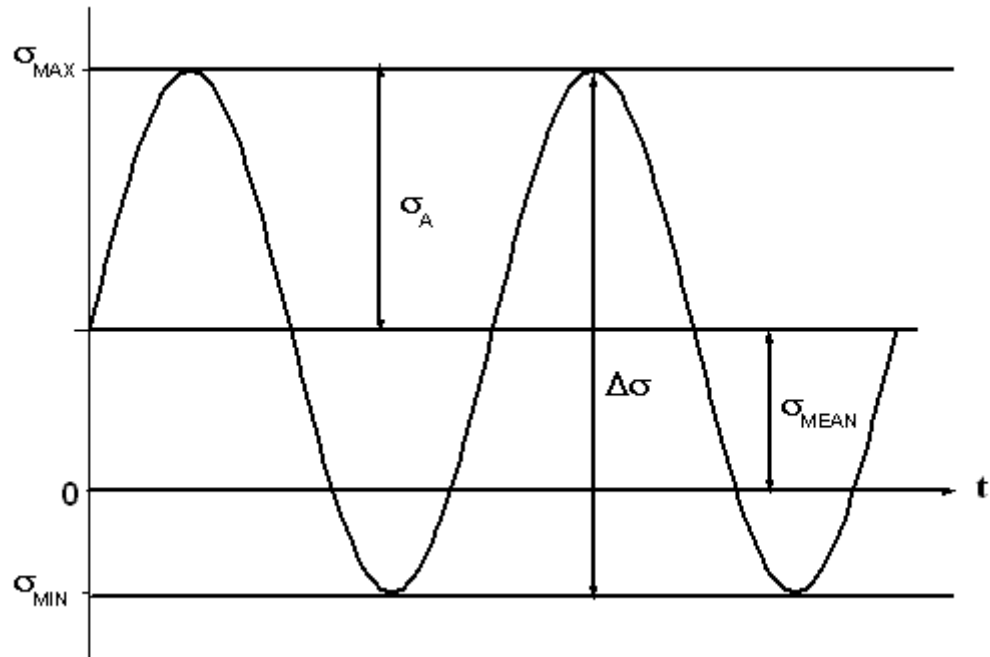


Figure 4.4.1-1 Generic Profile for Constant Amplitude Cyclic Loading

$$\text{Minimum Stress} = \sigma_{min} \quad (4.4.1-1)$$

$$\text{Maximum Stress} = \sigma_{max} \quad (4.4.1-2)$$

$$\text{Stress Range } \Delta_{\sigma} = \sigma_{max} - \sigma_{min} \quad (4.4.1-3)$$

$$\text{Stress Amplitude} = \frac{\Delta_{\sigma}}{2} \quad (4.4.1-4)$$

$$\text{Mean Stress } \sigma_{mean} = \frac{\sigma_{max} + \sigma_{min}}{2} \quad (4.4.1-5)$$

$$\text{Stress ratio } R = \frac{\sigma_{min}}{\sigma_{max}} \quad (4.4.1-6)$$

Using the above definitions, when the stress ratio $R = -1$ the testing has fully reversed loading. When the stress ratio $R = +1$, the load is static. And when the stress ratio $R = 0$ the testing is only in tension.

4.4.2. Specifics of Cyclic Loading for this Investigation

There are to be 3 tests executed, one test per mandrel size as defined in Table 4.4.2-1. For each test, the table lists the mandrel diameter size in inches, along with the radius of curvature in mm, followed by the calculated strain of the film, and finally the stress in the film (listed as max stress) based upon Young's modulus. The values for film strain and max stress in the table are based upon calculations from the finite element analysis performed in chapter 2 herein. For the cyclic loading performed for this investigation, the minimum stress shall be equal to zero since there is no reverse loading being performed. The test structure shall start at rest and be bent around a mandrel with the interconnect traces being on the outer surface so that they are subjected to tension stresses and no compressive stresses. Therefore, the stress ratio (R) is zero and the respective stress amplitudes and mean stresses are defined for each test in Table 4.4.2-1.

Table 4.4.2-1 Cyclic Loading Profile for each of the Three Life Tests

Life Test No.	Mandrel Size Diameter (inches)	Radius of Curvature (mm)	Film Strain (%)	Min Stress (GPa)	Max Stress (GPa)	Stress Amplitude (GPa)	Mean Stress (GPa)
1	1/4"	6.35	1.0	0	1.22	0.61	0.61
2	3/16"	4.76	1.4	0	1.66	0.83	0.83
3	1/8"	3.18	2.2	0	2.54	1.27	1.27

4.5. Test Structure Attributes Required to Support the Test

The stack up of the test structure has already been analyzed in chapter 2, however there are a few specific attributes of the test structures in this investigation that are required in order to adequately support a successful life test. There were two driving attributes that made it essential to have unique test structures fabricated for this investigation. The attributes were the need to directly measure the gate line interconnect impedance throughout the test as well as the need to visually inspect the interconnect traces after life testing. After the gate line interconnect is deposited and the geometry is etched out using photolithography, the remaining display stackup is built on top of this layer (thin film transistor, electro-optical material, and encapsulation layer). Hence, as shown in Figure 4.5-1, there does not exist a means to allow contact to the far side of the interconnect trace as well as a means to visually inspect them.

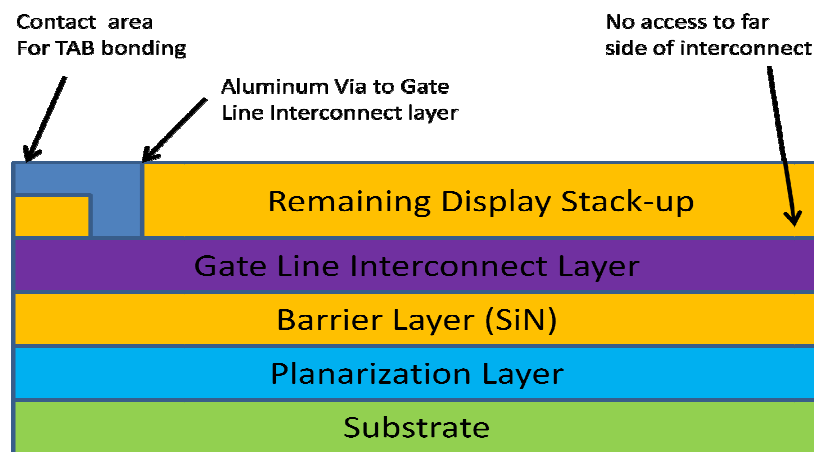


Figure 4.5-1 Cross Section Showing no Access to Far Side of Interconnect Layer

The idea of not depositing the remaining portion of the display stack-up only solves the problem for visual observation since the original mask for the gate line interconnect layer was designed to make use of Aluminum contact vias to eventually be TAB bonded to the driver electronics. Therefore, a unique mask was designed for the gate line interconnect layer in support of this investigation. Figure 4.5-2 is a .pdf image of the gate layer mask used to fabricate the test structures. The center portion is designed to be cut out leaving behind the other test structures that are not applicable to this investigation. The center portion is a rectangle comprised of the common bars, the ITO interconnect traces, and the pads to allow TAB bonding to the driver circuit card. More detailed discussion of this shall be provided in Chapter 5 herein.

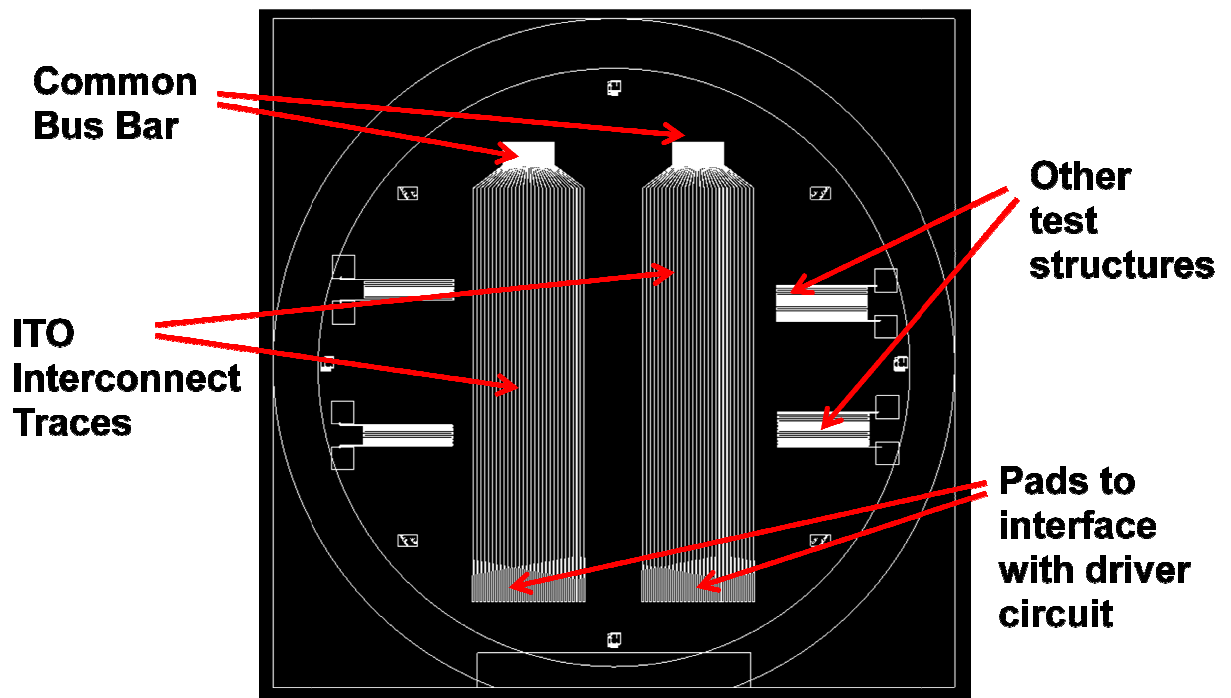


Figure 4.5-2 Custom Mask Layer to Fabricate Test Structures.

There are two main sets of traces designed in the mask. The first set of 30 traces contains 3 sub-groups of 10 traces each with widths of 1.5 μ m, 0.7 μ m, and 0.5 μ m. The second set of 30 traces contains 3 sub-groups of 10 traces each. The first subgroup contains 10 single traces of 1.5 μ m. The second sub-group contains 10 double redundant lines composed of two 0.75 μ m parallel lines. The third sub-group contains 10 triple redundant lines of three 0.5 μ m parallel lines. Table 4.5-1 shows the composition of the different traces on a substrate.

Table 4.5-1 Configuration of ITO traces

Group	Qty	width	configuration
I	10	1.5um	series
I	10	0.75um	series
I	10	0.5um	series
II	10	1.5um	series
II	10	0.75um	parallel
II	10	0.5um	parallel

4.6. Summary of Accelerated Life Test in Context with Investigation

Figure 4.6-1 reflects how the accelerated life test is integrated into the investigation of this thesis by allow one to rapidly capture relevant time to failure data in support of characterizing the life-stress model of the aforementioned failure mode resulting in line out in a flexible display.

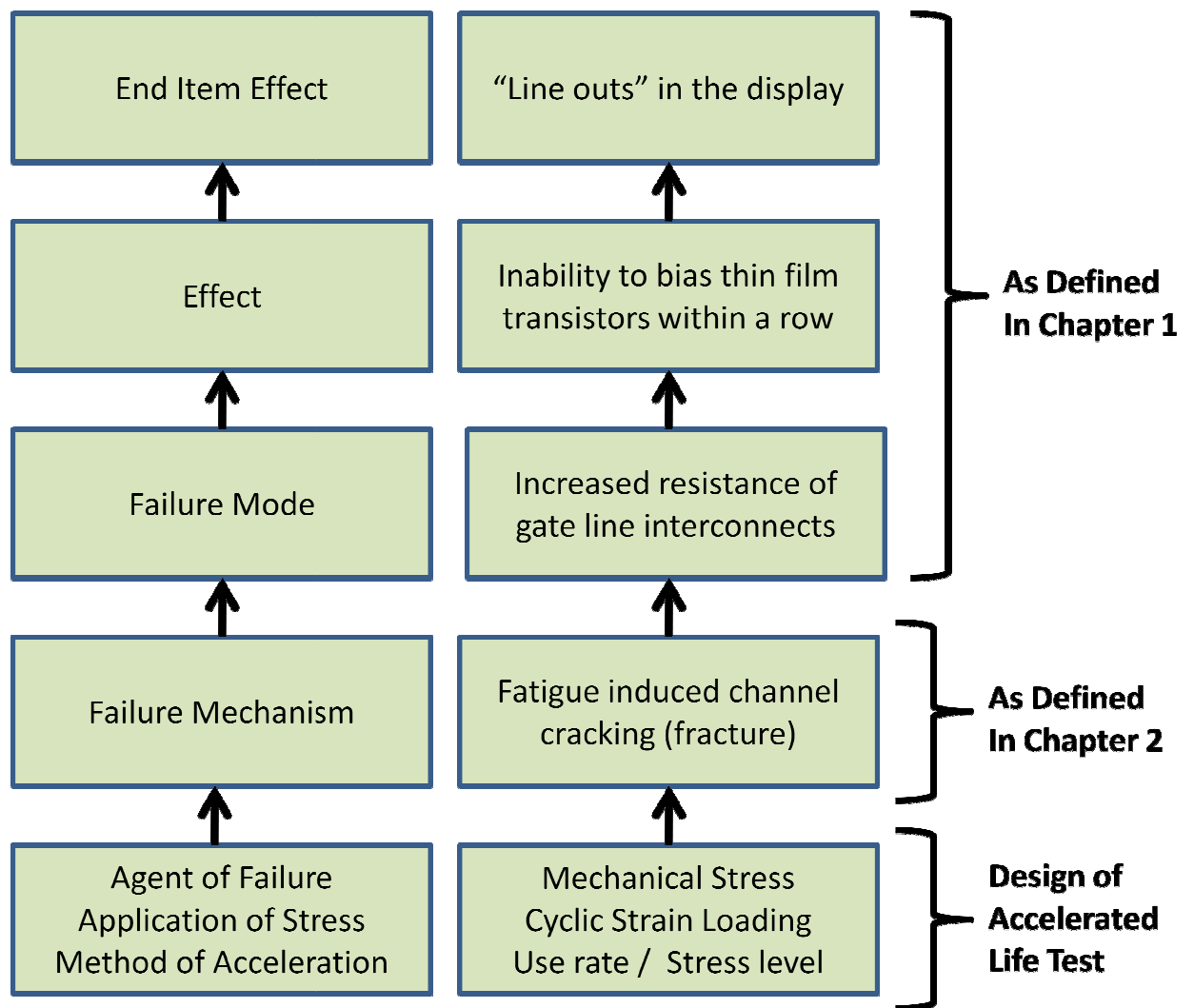


Figure 4.6-1 Relationship of Accelerated Life Test to Effect of the Failure Mode

Chapter 5: Dedicated Test System

5. Overview

In order to take advantage of the previous approaches and also fill the void of performing cyclic testing on patterned ITO traces on flexible substrates, a dedicated test system was designed, fabricated, and integrated for this research. A complete closed loop data capture system was designed with the intention of performing cyclic stressing of flexible substrates while simultaneously capturing resistance measurements of multiple gate line interconnects.

5.1. System overview

Figure 5.1-1 shows a top level block diagram of the dedicated test system with a personal computer running a Labview program at the heart of the design.

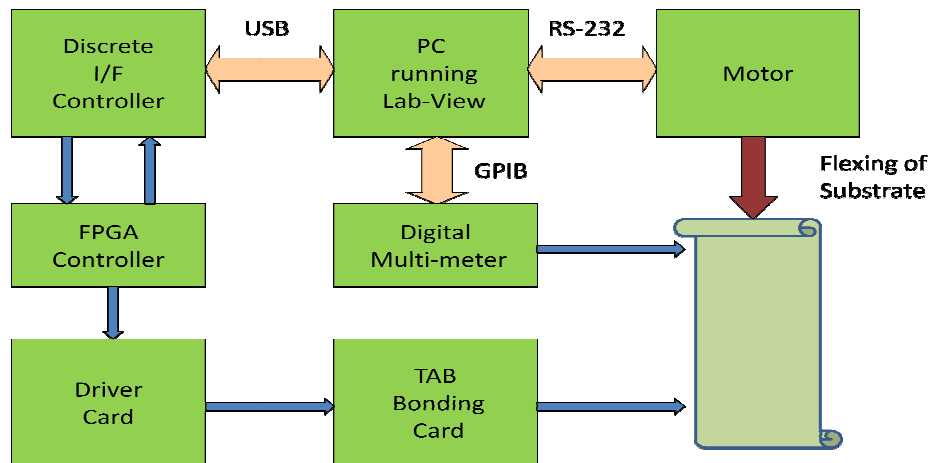


Figure 5.1-1 Block diagram of dedicated test system

This program runs in a loop set for the number of mechanical flexing cycles that is to be induced on the flexible substrate. During each cycle, the Labview program controls a stepper motor while simultaneously interfacing with all the other elements in the system either directly or indirectly. The main elements of this system will be discussed in greater detail in subsequent paragraphs. Table 5.1-1 provides a breakdown of all the major components in the system to include suppliers and supplier part numbers.

Table 5.1-1 Parts List of dedicated test system

Item	Description	Supplier	Part Number	Quantity
1	Personal Computer	Dell	DIM2400	1
2	Motor Controller Card	Pololu	SSC04A	1
3	Servo Motor	Grand Wing Servo	S125	1
4	Digital Multi-meter	HP	3478A	1
5	DIO Module	Measurement Computing	USB1208LS	1
6	FPGA Controller Card	Future Electronics	AXM-0330 revB	1
7	Driver Card	Custom	N/A	1
8	Flex Cables	Digikey	HFF-30U-06-ND	2
9	TAB Bond Card	Custom	N/A	1
10	Chassis Frame	Custom	N/A	1
11	Mandrels	McMaster-CARR	89945K131	3
12	Silver Epoxy	Resinlab	SEC1233	2

5.2. Labview Program

The heart of the dedicated test system is the Labview program running on a personal computer to control all of the elements that comprise the system. The program directly communicates via an RS-232 interface to the Pololu motor controller card.

The second piece of equipment that directly interfaces with the Labview program is a Hewlett Packard digital multi-meter by means of a General Purpose Interface Bus (GPIB) interface. Lastly, a USB interface is used by the PC to send and receive commands between the Labview program and a discrete input output (DIO) interface controller module supplied by Measurement Computing.

The overall operation of the Labview operates in a loop with three main steps: [1] Bend, [2] Sample, and [3] Relax. The program is also flexible in its ability to program the number of cycles between samples. Figure 5.2-1 shows the Labview program flow that represents one mechanical cycle to include a sample of all the gate interconnect lines.

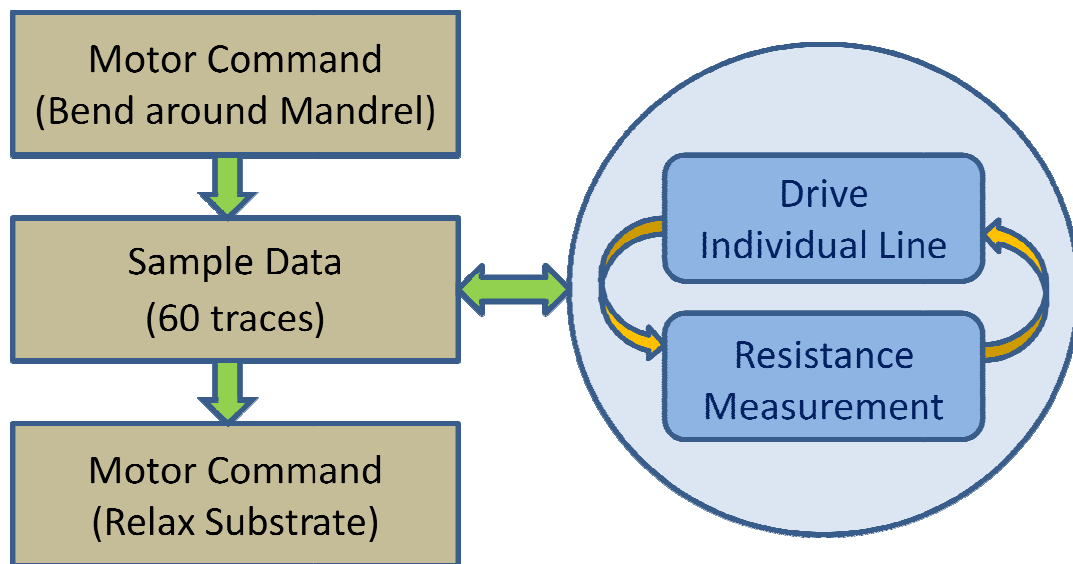


Figure 5.2-1 Flow diagram of Labview program.

5.2.1. Rotation Around Mandrel

The program loop starts with commanding the motor to rotate thereby bending the substrate around a mandrel with a set radius of curvature. At this moment a time stamp is generated for the data file for storing the upcoming resistance measurements.

Figure 5.2.1-1 is a screen shot of the Labview program showing these two parts.

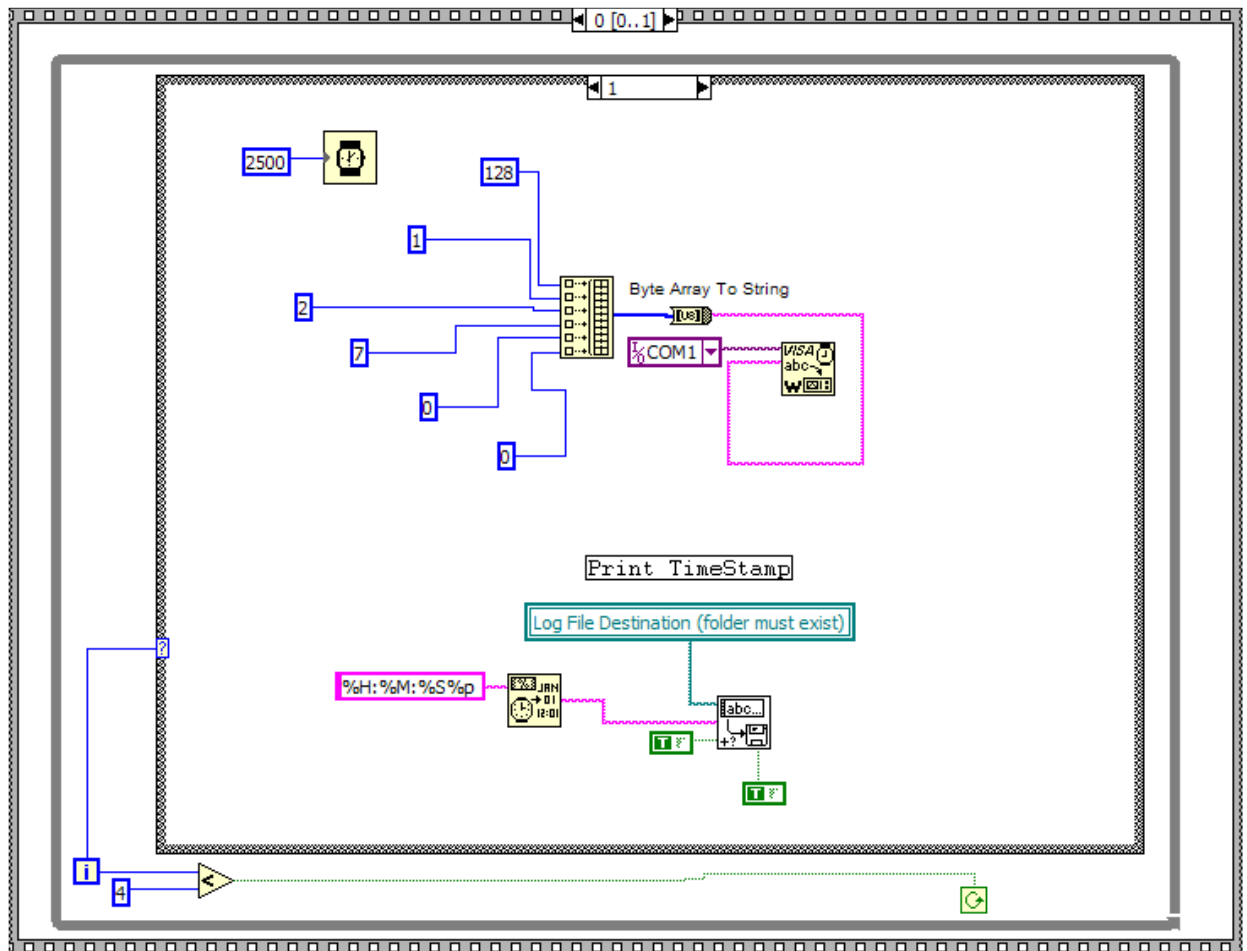


Figure 5.2.1-1 Labview Bend command and time stamp.

5.2.2. Discrete Interface Controller

Once the substrate is fully bent, the program enters the drive / sample cycle. This is accomplished by the PC communicating with discrete interface controller via a USB

interface. The discrete interface controller sets a discrete signal to the FPGA card to command it to start the drive / sample cycle. Figure 5.2.2-1 shows the Discrete Interface Controller along with Figure 5.2.2-2 reflecting the block diagram.



Figure 5.2.2-1 Discrete Interface Controller

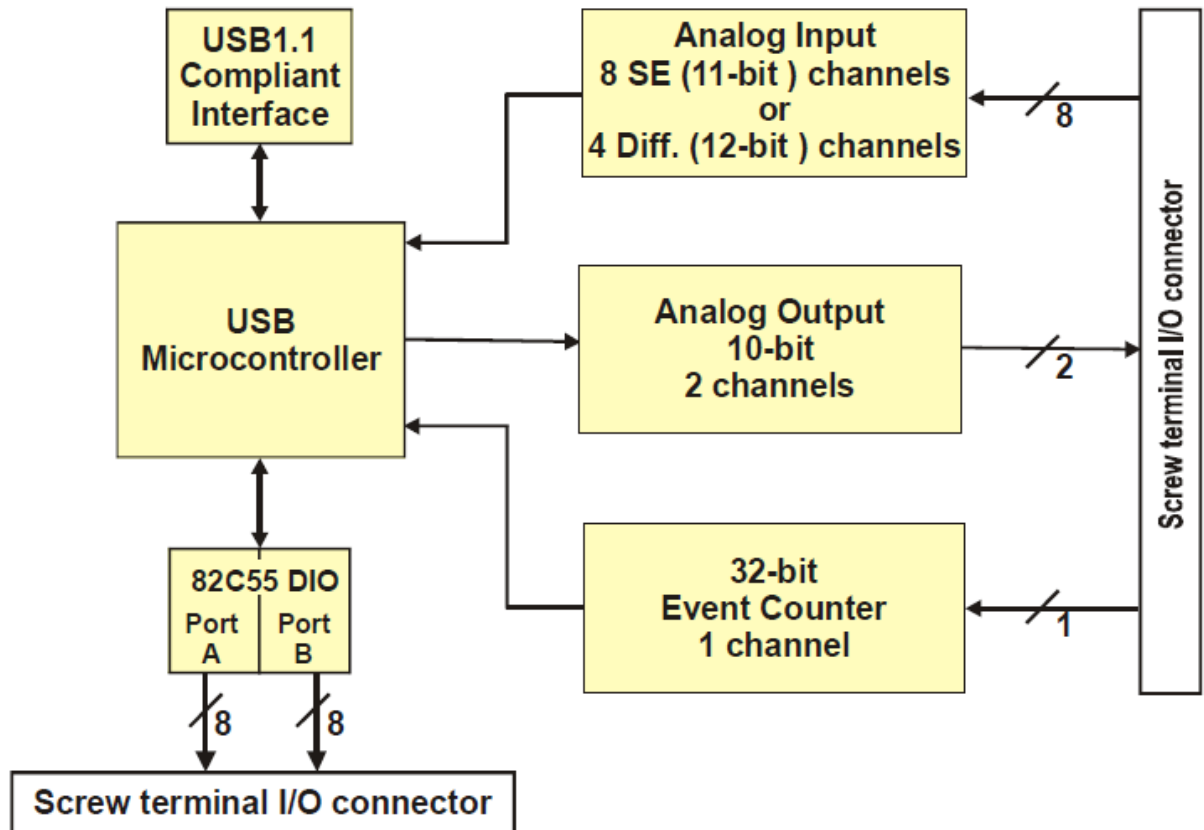


Figure 5.2.2-2 Functional block diagram of Discrete Interface Controller.

5.2.3. FPGA Card

The discrete signal generated by the Discrete Interface Controller commands the Field Programmable Gate Array (FPGA) circuit card to initiate the drive routine. An off-the shelf development kit was used to configure the FPGA with a unique program developed to rapidly drive and allow the resistance measurements of each of the individual traces on the flexible substrate. The program was written in VHDL (VHSIC (very high speed integrated circuits) hardware description language) and synthesized into an Actel Cyclone FPGA resident on the circuit card as shown in the block diagram provided in Figure 5.2.3-1.

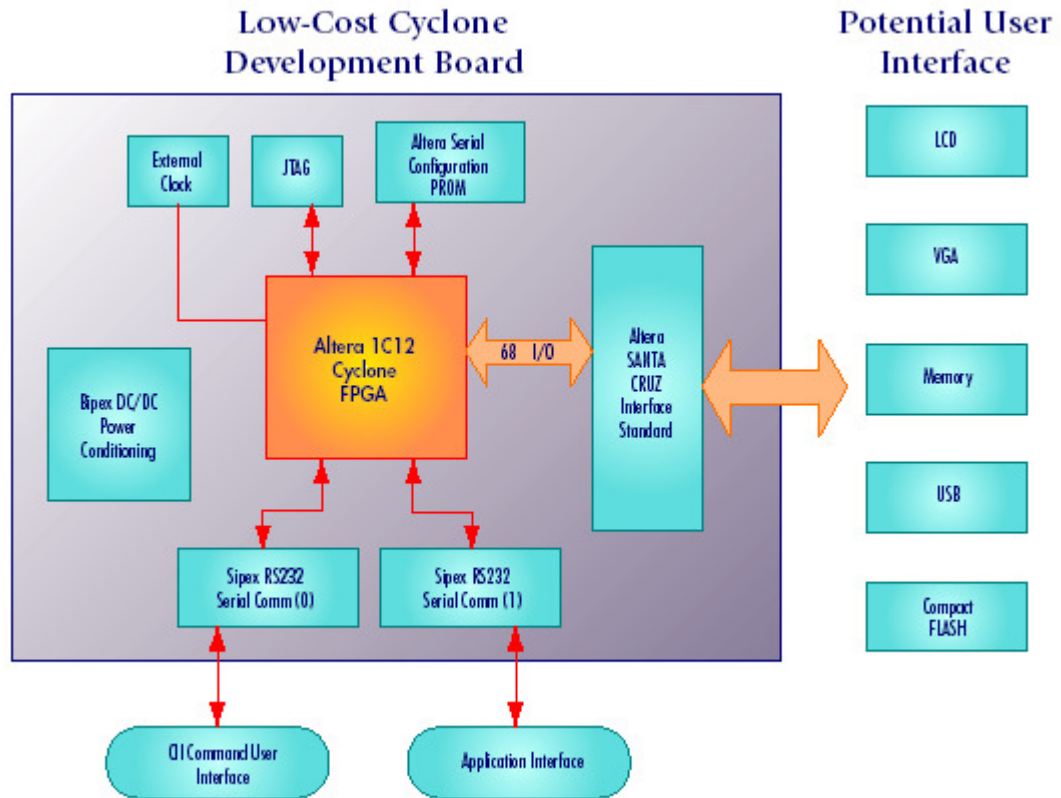


Figure 5.2.3-1 Block diagram of FPGA circuit card.

The operation of the FPGA entails several serial steps to individually control each of the traces on the flexible substrate. The FPGA is in a wait state until it receives the “start” command discrete. Once this start signal is enabled, the FPGA waits for 20ms and then drives the first line, this line is driven for a total of 640ms and during this time frame. After the first 20 ms of the 640 drive time, the sample signal is driven high by the FPGA and this is communicated back to the PC through the discrete interface controller. Figure 5.2.3-2 is a screen shot of the Labview program that waits for the sample command, note that the program times out if this condition is not met within 750ms.

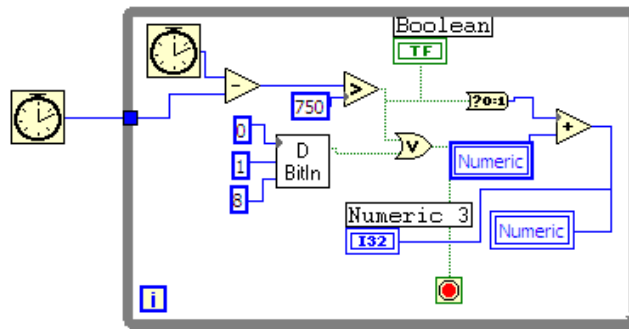


Figure 5.2.3-2 Screen shot of Labview program waiting for sample command

Once the Labview program receives the sample command, it triggers a resistance reading from the digital multi-meter (DMM) over a General Purpose Interface Bus (GPIB). Figure 5.2.3-3 is a screen shot of the program obtaining the DMM resistance reading and storing it in a data array.

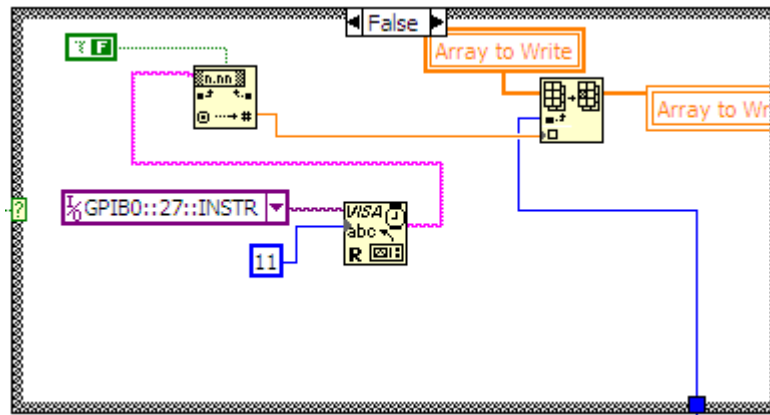


Figure 5.2.3-3 Screen shot of Labview program obtaining resistance reading

The FPGA allows 600ms for the PC and DMM to take a measurement and then it de-asserts the sample line. It then waits an additional 20ms to stop driving the line and then the process repeats itself until all the traces are measured. Figure 5.2.3-4

provides a timing diagram of the FPGA operation, note that in order to improve readability of the diagram, time was compressed for the duration of 250 to 600ms due to the fact that no signals are changing during this time period.

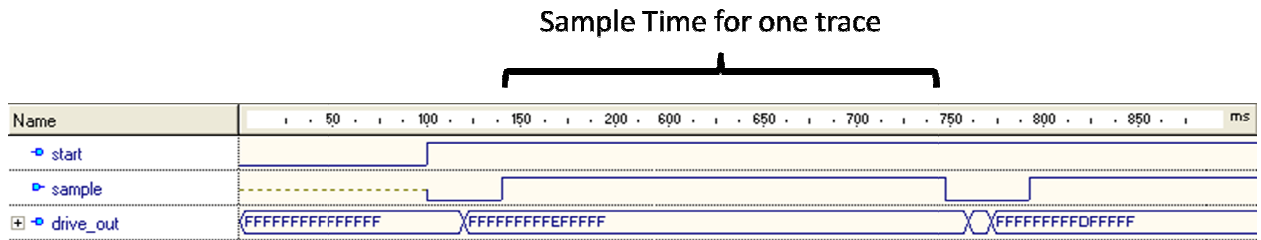


Figure 5.2.3-4 Timing diagram of the FPGA operation.

Once all the measurements are completed, the FPGA asserts a status signal to the Discrete Interface Controller that it is complete. This signal is communicated back to the Labview program via the USB interface.

5.2.4. Store Data and Return Substrate to Relaxed State

Once resistance measurements have been obtained for all the individual traces on the flexible substrate, the Labview program stores the contents of the data array into a log file as shown in Figure 5.2.4-1.

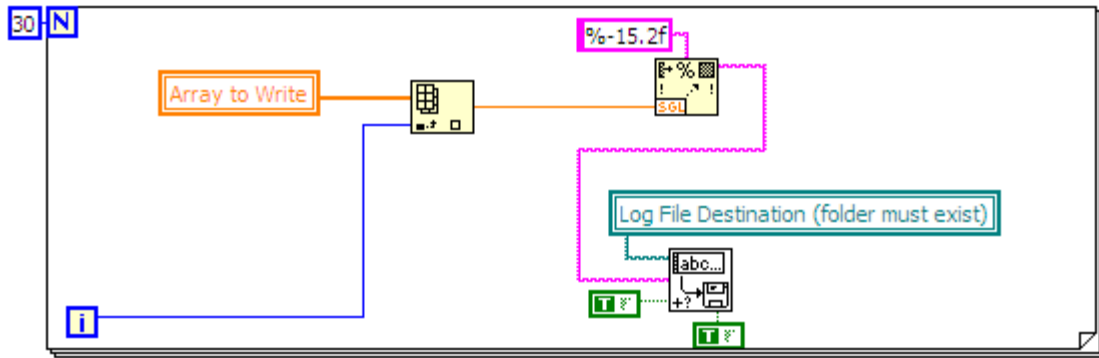


Figure 5.2.4-1 Screen shot of Labview storing data to log file

Finally, the Labview program commands the stepper motor to reverse direction and allows the flexible substrate to return to its relaxed (flat) condition as shown in Figure 5.2.4-2. This concludes one full mechanical cycle and this process is repeated based on a constant set in the Labview program.

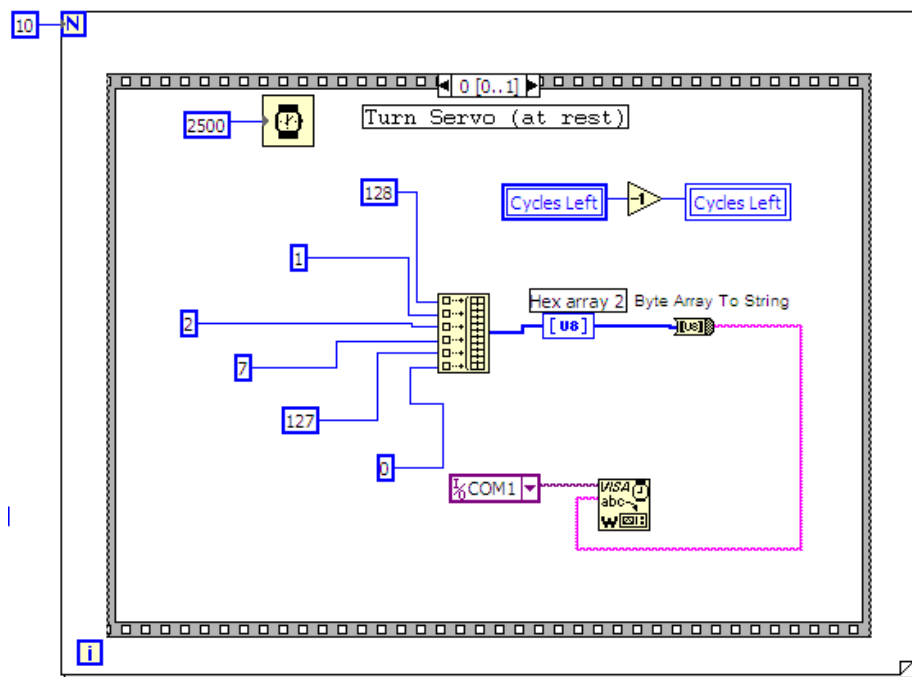


Figure 5.2.4-2 Labview commanding servo to return to relaxed position

5.3. Driver Card

The FPGA has the ability to control up to 60 individual discrete lines to the driver card. Each discrete line has a dedicated circuit that allows for the DMM to uniquely measure the resistance of that trace on the flexible substrate. Figure 5.3-1 shows the schematic representation of a dedicated circuit for driving two traces, specifically trace numbers 0 and 1 on the substrate. The “IN0” and “IN1” signals are commanded by the FPGA and controls the on state of the FET transistors Q1A and Q2B respectively. When the “IN1” signal is commanded high, the Q1B FET is on resulting in a low impedance path to ground that allows V_{cc} current to flow through the coil of the solid state relay allowing the “OUT1” signal (connected to trace 1 on the substrate) to be tied to the common signal.

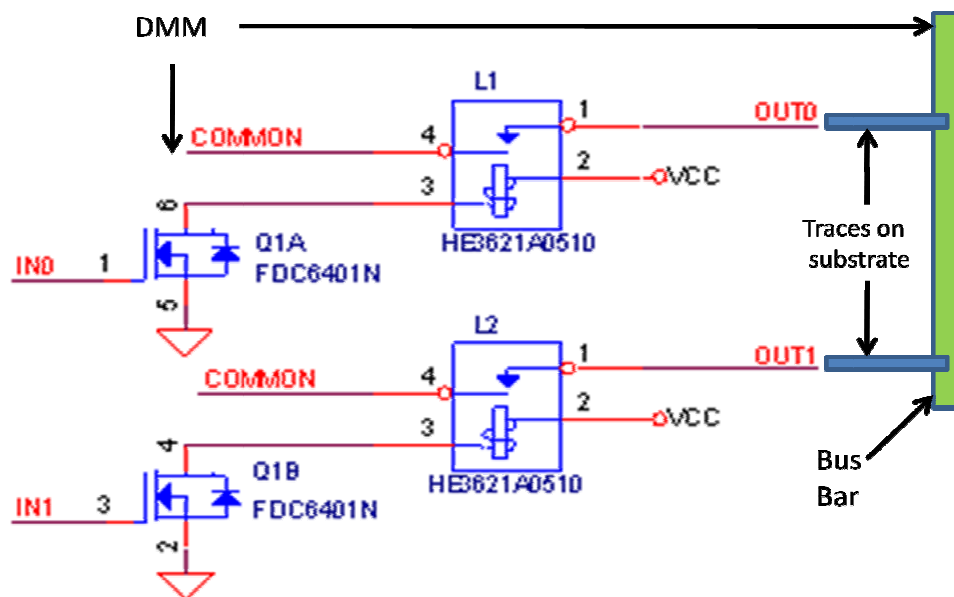


Figure 5.3-1 Schematic diagram of driver circuit for trace numbers 0 and 1

One side of the Digital Multi-meter (DMM) is connected to the common node on the driver card and the other side of the DMM is connected to the common bus bar on the flexible substrate where all the individual traces are eventually terminated. Thus one DMM is allowed to measure the resistance change of each individual trace on the substrate when that particular trace is connected through a relay by command of the FPGA. Figure 5.3-2 is a photograph of the actual driver card in the circuit.

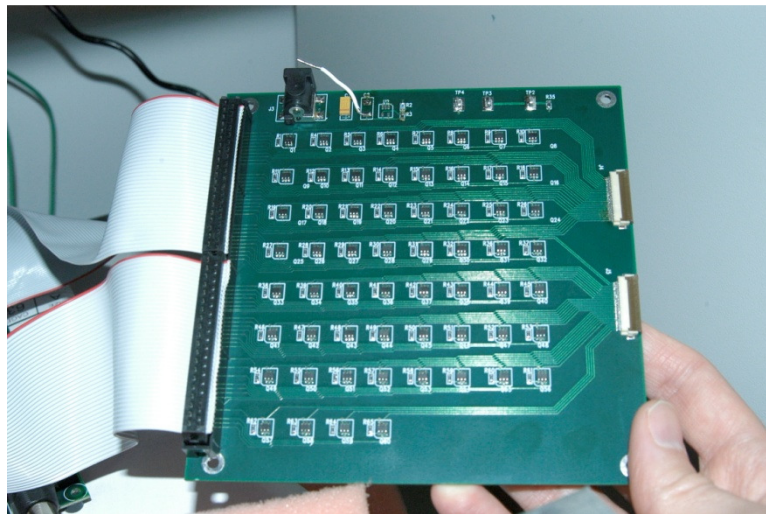


Figure 5.3-2 Photograph of driver card in circuit

5.4. TAB Bonding Card

The physical connection between the electrical circuitry of the driver card to the deposited traces on the flexible substrate is implemented by the TAB bonding card. Normally in displays, both flexible and those on glass substrates, a tape automated bonding process is employed to connect the printed circuit board lands to the traces on the display substrate material (glass, metal foil, or PEN). Bridging this physical gap is a polyamide film that normally contains a flip chip that is programmed to take

row/column signals and convert them to each unique row/column line to address each pixel in the array. Figure 5.4-1 is a diagram of an industry standard TAB.

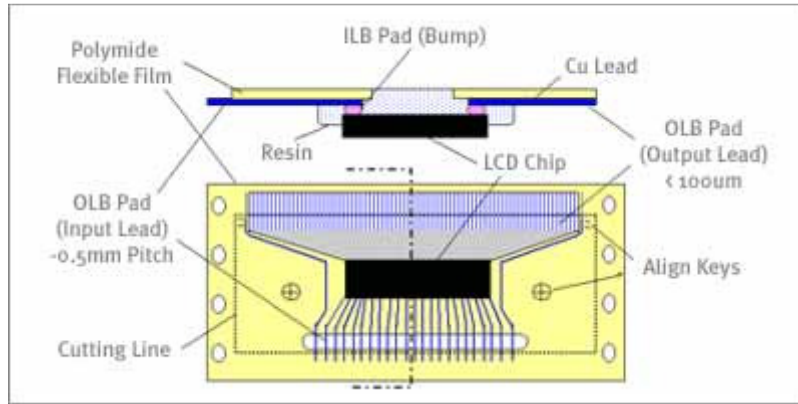


Figure 5.4-1 TAB outline diagram and cross section

An anisotropic conductive film (ACF) is used as the conducting element between the TAB bonding circuit card to TAB itself and the TAB to the display substrate (PEN for this study). ACF works by trapping conductive particles between the corresponding conductive pads on the IC and the substrate. As shown in Figure 5.4-2, ACF consists of a matrix of 3-5 μ polymer spheres, each nickel-gold plated and then coated with a final insulating layer in order to prevent shorting with a neighboring particle. The insulated particles are distributed in the film to prevent inadvertent connection in the X and Y axes.

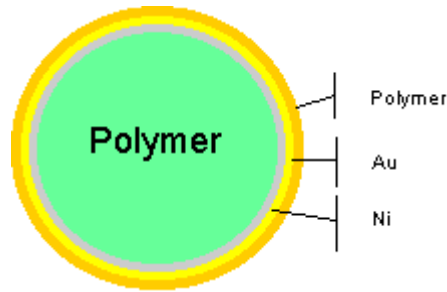


Figure 5.4-2 Cross section of ACF polymer sphere

During the bonding process, the insulation in the Z-axis where the balls are trapped is pushed away and therefore allows the Ni-Au layer on the particle to conduct in the Z axis. Figure 5.4-3 reflects the ACF both before and after the TAB bonding process. The advantages of this process is that after exposure to pressure and heat, both an electrical and physical connection is made in the Z axis but not the X or Y axes.

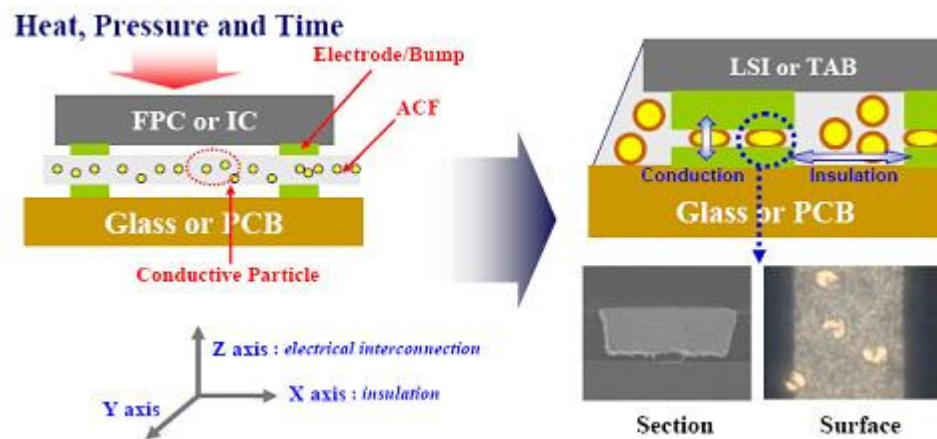


Figure 5.4-3 ACF before and after bonding process

Initially, a dedicated TAB was designed and fabricated for this particular research effort in order to connect the drive circuitry to the traces deposited on the flexible substrate. It was not until the actual bonding was to take place did an idea of eliminating the TAB altogether was devised. The solution involved making the pitch width of the traces on the flexible substrate identical to the pitch and width of the lands on the TAB driver printed circuit board so that the substrate could be directly bonded to the card. This turned out to be very beneficial since the TABs tend to be a source of high failure rates for displays.

The traces of the circuit board had to consist of electroless nickel plating covered with a thin layer of immersion gold in order to protect the nickel from oxidation. This electroless nickel / immersion gold combination is commonly referred to as ENIG and also allows for excellent surface planarity regardless of the work-piece geometry which is critical for the reliable operation of the anisotropic conductive film. Figure 5.4-4 shows the TAB bonding card with ENIG plating on the traces, note that the flexible substrate has not yet been attached to the card.

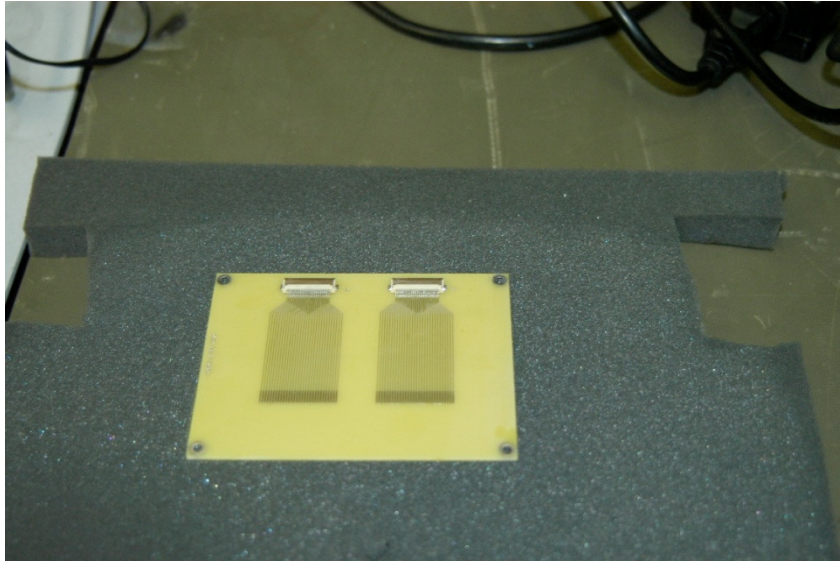


Figure 5.4-4 Picture of TAB bonding card without substrate attached

5.5. Mechanical Fixture

A mechanical fixture was designed and fabricated to allow the mounting of the motor, mandrel, and TAB card with a flexible substrate as shown in Figure 5.5-1.

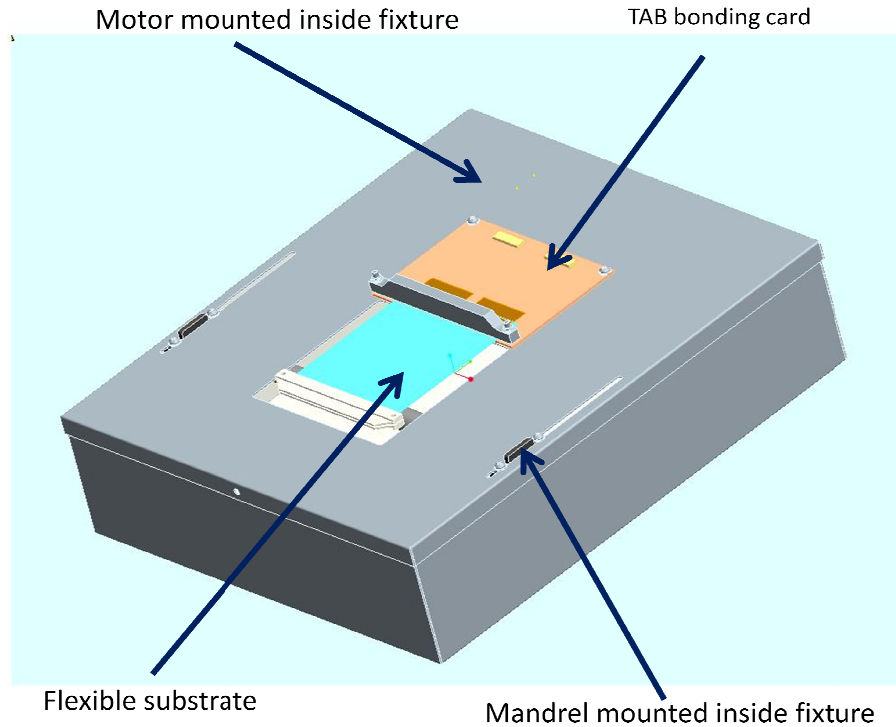


Figure 5.5-1 Pro-E three dimensional model of mechanical fixture

Once the substrate is bonded to it the TAB card, silver conductive epoxy is applied to the opposite end of the substrate to make a common bus bar with flying leads to allow for the digital multi-meter to connect to the ends of the ITO traces on the substrate. Figure 5.5-2 shows the leads connected to the flexible substrate after it has been bonded to the TAB bonding card, note that the substrate and ITO lines are transparent and there is manila colored paper underneath the transparent substrate.

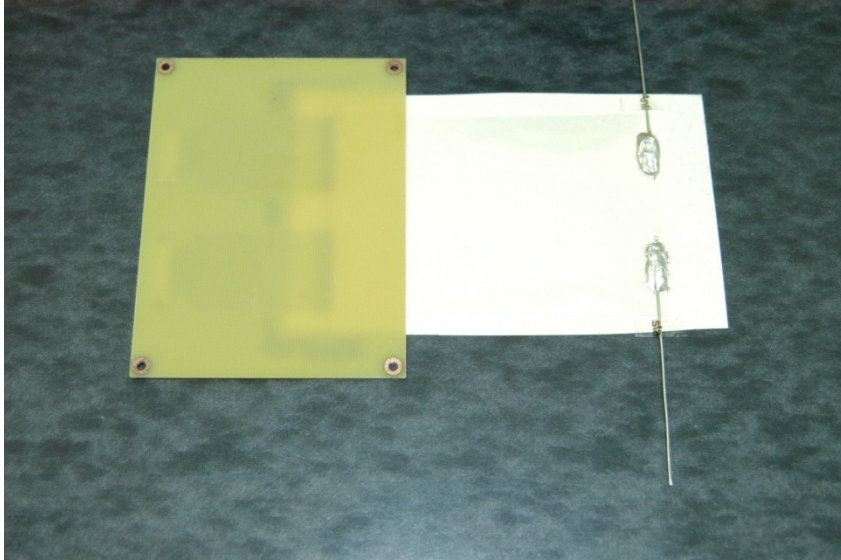


Figure 5.5-2 Leads attached to the common bus bar on the flexible substrate

The TAB card is then mounted into the lid of the fixture and a clamp is attached to the far end of the substrate just beyond the bus bar, whereby a small weight is attached to keep the substrate in a flat position. The motor drives a spindle that is also connected to the same clamp via a string. Figure 5.5-3 shows how these connections are made.

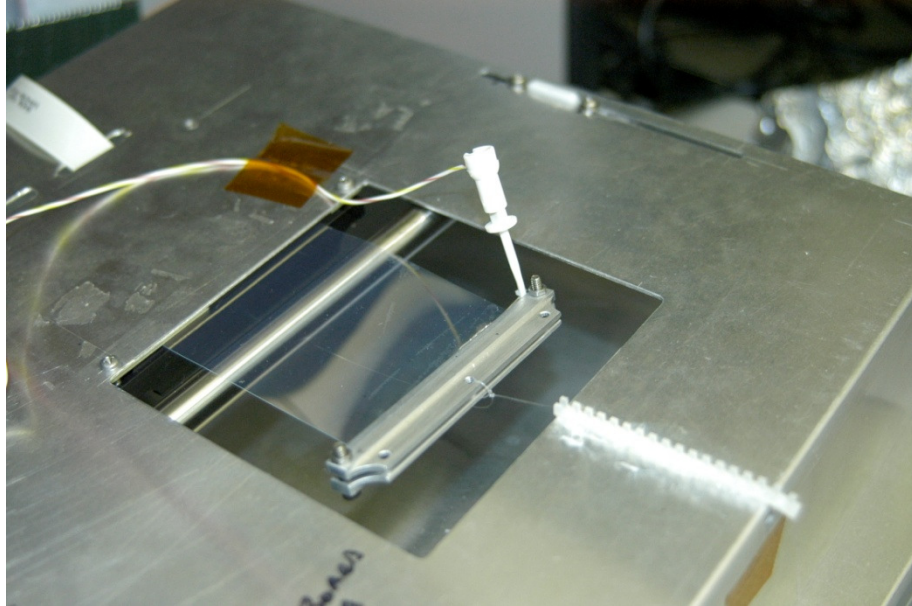


Figure 5.5-3 Fixture with substrate mounted and mandrel installed

When the motor rotates, it pulls the substrate around a mandrel of a set radius. Inserts were designed and fabricated to secure the mandrels in the fixture. Figure 5.5-4 and Figure 5.5-5 show the mandrels and drawing for the inserts prior to mounting in the fixture.

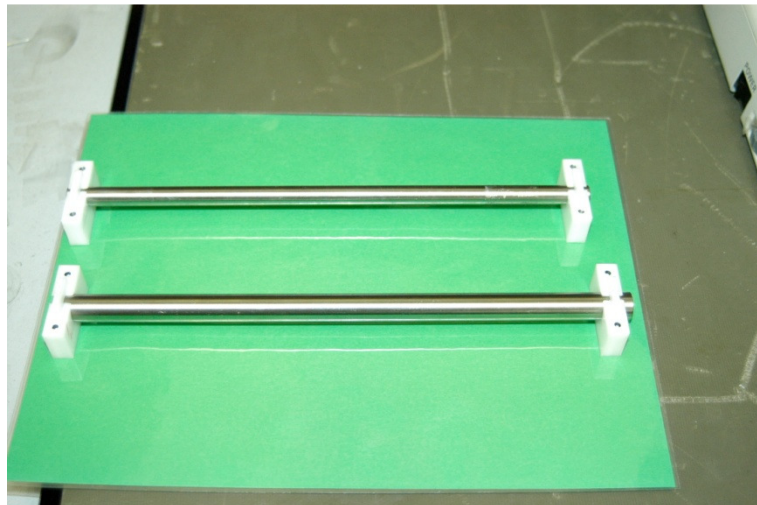


Figure 5.5-4 Picture of mandrels and insert drawing

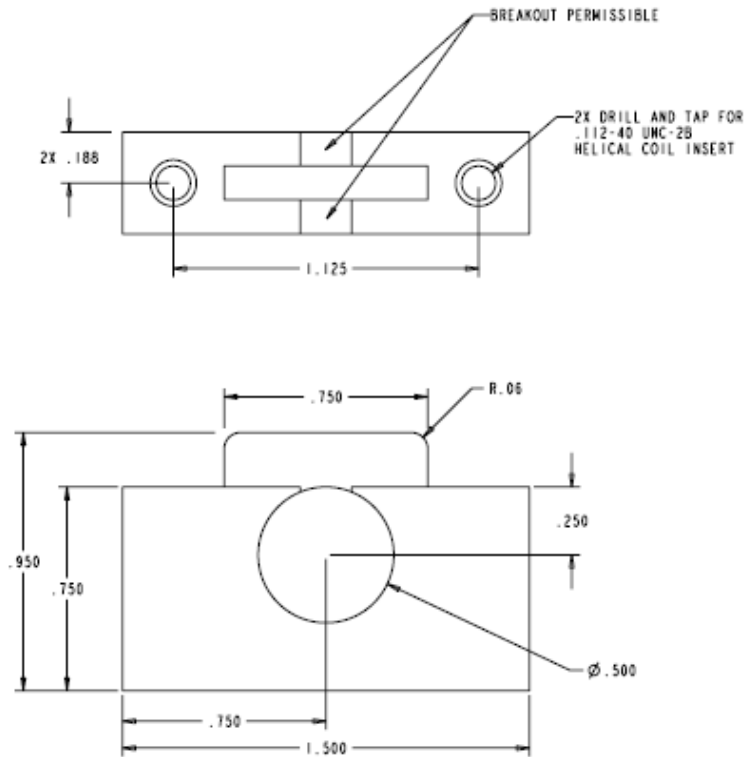


Figure 5.5-5 Drawing for the Mandrel Inserts

Mounted inside the fixture is the Pololu stepper motor that pulls the flexible substrate around the mandrel. In order to ensure that the substrate conforms to the shape of the mandrel under a flexed condition, the motor pulls the substrate tightly. It was found during testing that with the mandrel mounted rigidly, the bonding between the substrate and the card was inadvertently seeing a lot of stress. Since the test is designed to stress the ITO traces and not the TAB bonding sites, a thin compliant material was added around the mandrel to prevent stress to the TAB bonds while ensuring the substrate conforms to the mandrel's shape (radius of curvature). Figure 5.5-6 is a picture inside the fixture with the lid opened up, note the TAB bond card in the upper portion of the picture – this is mounted to the underside of the fixture cover plate.

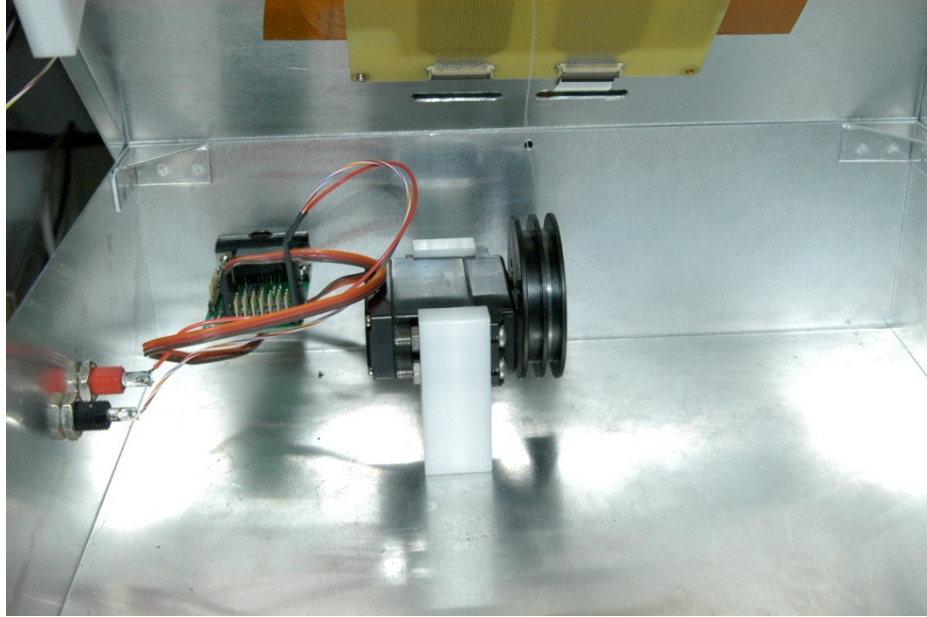


Figure 5.5-6 Stepper motor mounted inside the fixture

5.6. Verification of Dedicated Test System

This section entails the issues encountered with the test system during the initial set up/mounting of the test structures as well as issues as a result of the actual execution of the initial accelerated life tests attempted on the system. In all there were a total of nine problems identified. For each problem, an investigation was undertaken, the root cause was identified, and a corrective action implemented to eliminate the problem from future recurrence.

5.6.1. Initial Sporadic Resistance Readings

During initial testing, sporadic resistance readings of the traces were observed without any mechanical stress being applied. Analysis entailed the electrical aspects of the resistance monitoring systems. It was determined that the resistance monitoring

system was not providing enough isolation between the different drive circuits and since there were a total of 60 individual circuits, this poor isolation added up significantly. Therefore, the drive circuit of the resistance measuring system was modified to replace the driving FET transistors with relays in order to improve isolation.

5.6.2. Continued Sporadic Resistance Readings

After modifications to the drive circuit, sporadic resistance readings improved but still continued. Analysis moved to the interface of the TAB bonding itself and determined that the TAB bonding process being performed by technicians at the Flexible Display Center was not optimized. The TAB bonding issue was brought to the attention of the Flexible Display Center and subsequent test structures were properly TAB bonded.

5.6.3. Rapid Open Circuit Conditions

Once the resistance measurements were stable, rapid open circuit conditions were observed without the ITO traces having little exposure to mechanical cycling. Initial investigation thought traces were cracking due to limited bending around mandrel. When the radius of curvature was expanded and failures persisted, it was thought that uniaxial tension was the culprit. It was not until SEM analysis of the traces that the investigation determined that the traces themselves did not exhibit cracks. Follow up resistance measurements determined that open circuit conditions were evident at the

TAB bond interface. Neither biaxial nor uniaxial tension of the ITO traces themselves were determined to be the culprit. When even the smallest amount of tension was applied to the substrate that tension was translated back to the TAB bonding area. The circuit board clamp design to hold the substrate close to the circuit board was not sufficient in isolating the TAB bonds from tension being applied to the rest of the substrate. Double sided VHB (Very High-Strength Bond) tape was applied between the substrate and circuit board between the TAB bonding site and the remainder of the traces being exposed to the mechanical stress. This in turn was able to isolate the TAB bond sites from the external mechanical stress being imposed on the substrate.

5.6.4. Form Factor

During a flex cycle, it was observed that the substrate had a non-optimized form factor when attempting to physically conform around the mandrel. This was causing initial compression of the ITO traces instead of only applying tension stresses. Several items were investigated to improve the substrate form factor. These included position of mandrel, mounting position of the circuit board, position of the clamp, speed of the motor, and location of the motor with respect to the mandrel. It was determined that the angle between the motor position and the mandrel was too small and it resulted in the poor conforming shape of the substrate. The frame was modified to allow the motor to be mounted at a higher angle. This resulted in an improved form factor and eliminated the initial compression of the substrate.

5.6.5. Trace Failure During Calibration

When a new mandrel is mounted in the fixture, the system needs calibration to determine the optimum position of the motor and motor clamp. During this initial calibration, ITO traces were failing and getting open circuit conditions. Investigation determined that too much tension was being applied to the substrate during calibration of the motor position with respect to the mandrel. Since the mandrel is made of aluminum and is mounted to the fixture, there was not enough play in the system to allow for proper calibration. A thin layer of foam was applied to the aluminum mandrel to allow for a minor amount of cushion to be used during calibration.

5.6.6. Excessive Stress on Motor

During life testing, the motor would fail prematurely. IT was determined that the counter weights that pull against the motor were too high and therefore imparting too much stress on the motor during the cyclic bending. The motor was replaced and the counter weights were optimized to reduce the amount resistance that the motor had to work against as well as still be enough to pull the substrate back to its initial relaxed (unbent position).

5.6.7. Premature Meter Lead Fatigue

Along with the motor failure, the electrical leads for the digital multi-meter were breaking during life testing. Investigation determined that extensive cyclic testing of

the substrate was imparting mechanical fatigue in the electrical leads that connect to the bus bar since the leads were not properly mounted to allow for strain relief. As a corrective action, strain relief was provided for the electrical leads as well as a routine replacement was instituted after the leads were exposed to over 50,000 cycles.

5.6.8. Slippage of Clamp Assembly

Observation of the motor the clamp progressively got worse throughout the test. The investigation looked at how the motor was positioned, the co-planarity of the mandrel with respect to the motor and fixture, and mounting of the circuit board. It was concluded that the clamp was not properly centered with respect to the substrate and this was compounded by the fact that the clamp would slowly start to slip during the cyclic testing. The clamp was redesigned to allow for improved centering during the calibration process as well as improved grip to eliminate slippage during the cyclic testing.

5.6.9. Stresses Induced During Initial Mounting

When a new substrate is mounted to the test system, compressive and tensile stresses were inadvertently applied to the substrate / ITO traces. The line connecting the motor to the motor clamp was not long enough to allow enough slack during the attachment of the motor clamp to the substrate. Therefore, the substrate would have to be bent and stressed significantly to allow enough clearance to mount the clamp. During the mounting process, the motor was placed in the default reset position (0

degrees). This initial position did not allow for enough slack in the line. It was determined that the motor had a range of motion from 0-720 degrees of rotation. Once this was determined, the initial default reset position was changed to the 360 degree position and this allowed for slack in the line during the mounting of the motor clamp and therefore eliminated the unwanted stresses imposed on the ITO/substrate.

5.7. Summary

Since flexible displays are relatively new in terms of technology, there are limited test systems available to subject them to practical environmental conditions and accurately characterize them throughout reliability testing. Chapter 3 provided an overview of previous work and applicable testing systems, however given the specific requirements of this investigation a unique test system was required to be designed and fabricated.

Chapter 6: Life Test Data Analysis

6. Overview

As explained in chapter 5, this investigation entailed the design and verification of a new dedicated test system. Hence, there were multiple test structures that were prematurely damaged during the process of optimizing the test system. Since the test structures were fabricated by the Flexible Display Center using a unique mask set specific to this investigation, there were a limited number of test structures produced. Unfortunately, during this investigation the test structures were consumed by the test system verification process. This section was initially dedicated to the summary of the life test data performed at three different stress levels, but now it will show and analyze the limited data that was obtained during the process of verifying the new test system. The last portion of this section is dedicated to the process of how one would analyze the life test data and obtain meaningful interpretations.

6.1. Resistance Calculation

In order to prevent damage to exposed traces, a decision was made to not completely wrap the substrate around the mandrel. This is based on the fact that the substrate length is much longer than the circumference of the mandrel and would have required that the substrate be bent multiple times around the mandrel. If this were done, the exposed traces would have been in contact with the underside of the substrate and exposed them to a rubbing action. Since in the actual implementation of a flexible

display these traces are buried inside the display and are protected, this would have introduced a new and irrelevant failure mode to the investigation.

With this testing approach, only a portion of the entire trace length was exposed to the mechanical stress induced by the radius of curvature of the mandrel. Hence, the measured change in resistance is only relevant to a particular portion of the trace length. The raw change in resistance ($\Delta R_{\text{measured}}$) as captured by the digital multi-meter, has been proportioned across the entire length of the trace width ($\Delta R_{\text{inferred}}$). This proportion is based on the ration of the entire trace length (TL) to the arc length (AL) subjected to the mechanical stress as defined in equation 6.1-1.

$$\Delta R_{\text{inferred}} = \Delta R_{\text{measured}} \left(\frac{TL}{AL} \right) \quad (6.1-1)$$

6.2. Definition of Failure Based on Trace Width

In order to maintain consistency in analysis of determining cycles to failure based on raw resistance measurements, the failure threshold was set to be a percentage of the inferred change in resistance to the initial resistance of the trace as defined in equation 6.2-1.

$$\frac{\Delta R_{\text{inferred}}}{R_{\text{initial}}} \times 100\% \geq 110\% \quad (6.2-1)$$

The failure definition of 110% percent was determined based on the SPICE circuit simulation results of a failure threshold defined to be when the gate line resistance exceeds 450K ohms. The average initial resistance of the 15 μ m width gate lines was calculated to be 215, therefore a 110% change in resistance of the trace results in a failure condition.

In order to analyze the impact of trace width of cycles to failure, other traces were fabricated with widths of 7.5 μ m and 5 μ m. Even though their initial resistance is too high for adequate biasing of the thin film transistors used to drive the pixels, the analysis of their resistance data provides insight into the influence of trace width on cycles to failure. To maintain consistency in comparing the reliability of the narrower traces to the reliability of the baseline trace width structures, the same failure threshold of 110% has been employed.

6.3. Cycles to Failure Data

Raw data obtained during the integration of the dedicated test system for resistance values measured at every 10 bending cycles has been plotted in Figure 6.3-1. Due to the limited amount of test structures, additional data was simulated for analysis purposes.

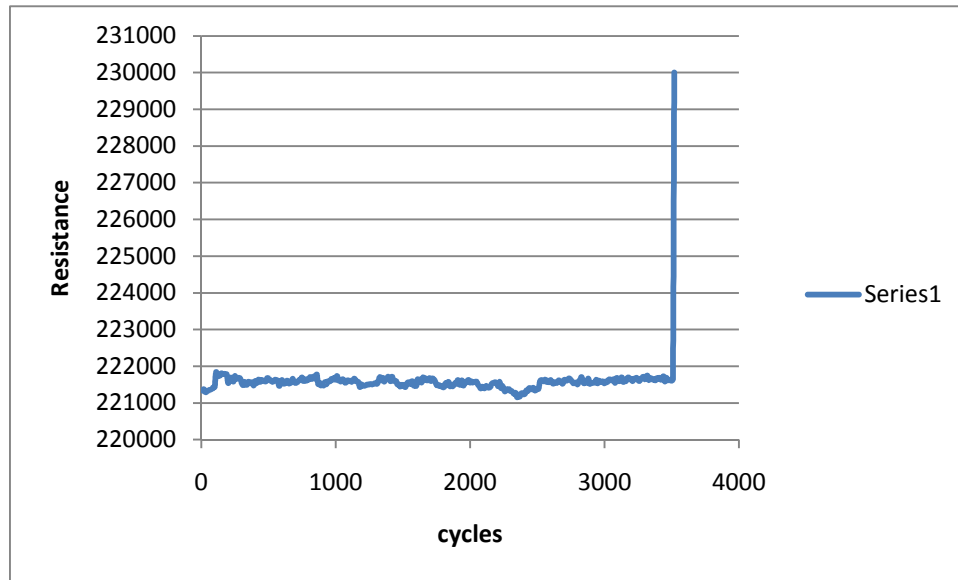


Figure 6.3-1 Resistance versus cycles for 15um trace

6.4. Process for Analyzing Life Test Data

Section 6.3 covered the analysis of the limited data obtained during the test system verification process. This section provides a generic process to be applied for the analysis of life data to allow for the determination of expected life under actual field use conditions. Since there are two main factors influencing the trace life in this investigation, section 6.4.1 analyzes how one would review data based on mechanical stress through mandrel size and section 6.4.2 analyzes the impact of device geometry by varying trace width. Random cycles to failure data was generated and is provided in Appendix A that was used as a basis for this section.

6.4.1. Analysis Based on Mechanical Stress

This section compares three traces of the same width but exposed to different mechanical stresses as imposed by the radius of the mandrel. Figure 6.4.1-1 reflects the ratio of $\Delta R / R_{\text{initial}}$ as a function of cycles for traces having a width of $15\mu\text{m}$.

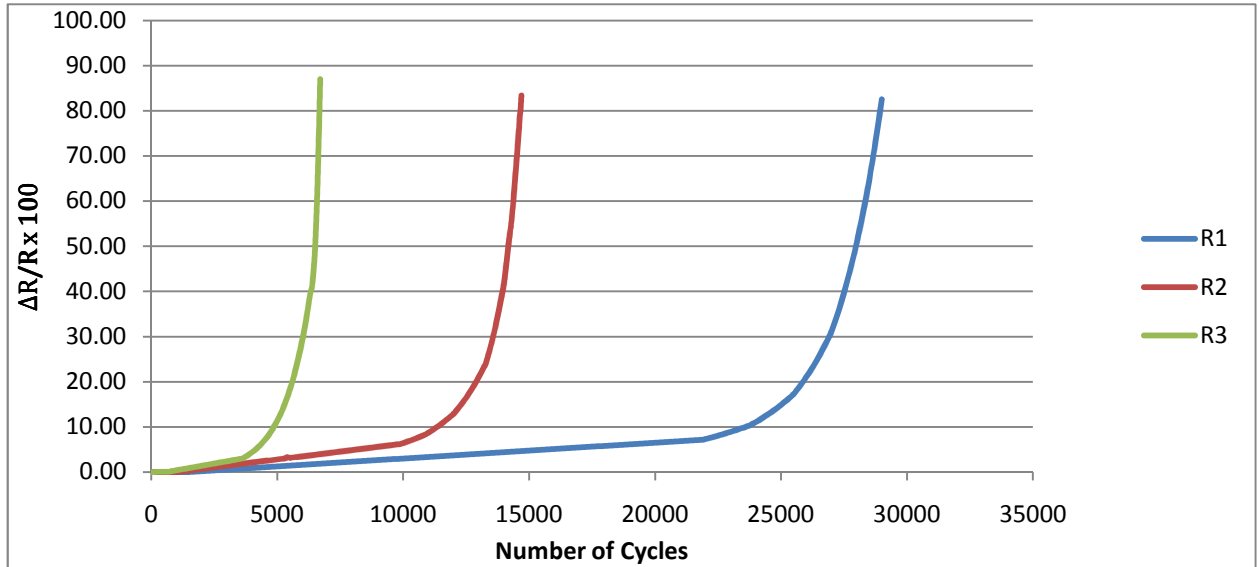


Figure 6.4.1-1 Simulated Influence of Mandrel Radius on Cycles to Failure

Given that each life test was composed of multiple traces each having their own times to failure, statistical analysis of the time to failure (more appropriately called cycles to failure) can be performed. Chapter 7 uses advanced analysis techniques to fit the data to specific distributions based on varying stress conditions.

6.4.2. Analysis Based on Device Geometry

As opposed to section 6.4.1, this section compares three traces of different widths while exposed to the same mechanical stress as imposed by the radius of the mandrel. Figure 6.4.2-1 reflects the ratio of $\Delta R / R_{\text{initial}}$ as a function of cycles for traces having a width of 15 μm , 7.5 μm , and 5.0 μm while subjected to a constant stress condition. Since there were a total of 10 data points for the 15 μm traces, 10 data points for the 7.5 μm traces, and 10 data points for the 5.0 μm traces, chapter 7 shall analyze the influence of trace size on life model parameters.

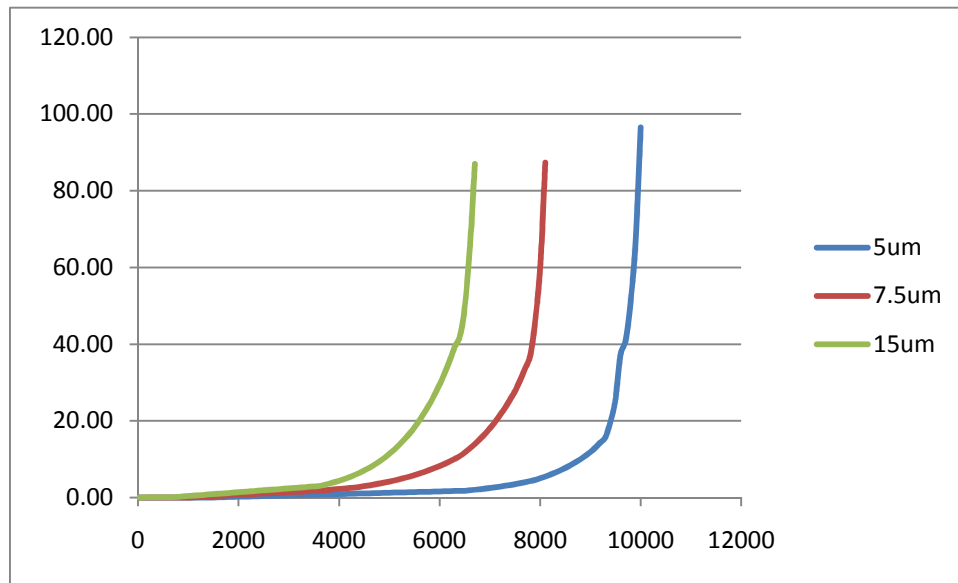


Figure 6.4.2-1 Simulated Influence of Trace Width on Resistance Change

6.5. Summary of Data Analysis

The raw resistance measurement of the traces during the life testing are required to be normalized based on the ratio of the change in resistance to the initial resistance. Given the fact that only a portion of the trace is subjected to the mechanical stress, the change in resistance has been proportioned based on the arc length of the trace that is actually wrapped around the mandrel.

The more important aspect of this section is the presentation of a process by which one can analyze life test data and isolate the impact of different test conditions such as mechanical stress and device geometry on the mean cycles to failure as well as the standard deviation. Chapter 7 is dedicated to the analysis of this data with respect to determining a life-stress relationship based on the underlying failure mechanism.

Chapter 7: Life-Stress Model Analysis

7. Overview

This chapter is dedicated to the analysis of life test data in order to determine a life-stress model. First the different life distributions that are commonly used in reliability engineering will be reviewed followed by the different stress models employed to model different types of failure mechanisms. Since this investigation revolves around mechanical stress as the agent of failure, an overview of the three main approaches to fatigue analysis will be provided. In terms of estimating life-stress model parameters, several methods will be covered followed by the benefits and drawbacks of each method. The last section is actual parameter estimation along with their goodness of fit based on simulated times to failure from chapter 6.

7.1. Life Distributions

This section briefly highlights three main types of distributions that are used in reliability analysis of life test data. The three distributions are the Exponential, the Weibull, and the Lognormal. There are numerous others, but for the context of this investigation these are the basic distributions commonly used for the majority of analysis.

7.1.1. Exponential Distribution

The exponential distribution is commonly used in reliability engineering. It is also the

simplest given that it has one variable lambda (λ) that is employed in Equation 7.1.1-1 which is the probability density function. Here lambda represents the failure rate, which is assumed to be constant [Kececioglu 1991].

$$f(T) = \lambda e^{-\lambda T} \quad (7.1.1-1)$$

Equation 7.1.1-2 is the Equation for reliability life. Therefore the reliability at time t_R is evaluated as the probability of a given product failing during a mission time between time equals zero and t_R .

$$R(t_R) = e^{-\lambda t_R} \quad (7.1.1-2)$$

For a repairable system, the term Mean Time Between Failure (MTBF) is commonly used. The MTBF is defined as $1/\lambda$ and results in a probability of 0.632 [O'Connor 2002]. The assumption is that the repair activity brings the product to an “as good as new” condition and therefore resets the clock back to zero since the failure rate is assumed to be constant. Another way that the Exponential distribution is used is to predict the number of failures of multiple similar systems. With 100 systems deployed, it is assumed that 63 will fail when all are operating within the time frame between time equal to zero and the MTBF.

Recent use of the exponential distribution was based on the collection of failure data of electronic systems accumulated several decades ago [MIL-HDBK-217 1995].

Early on, the data was tainted by equipment accidents, repair blunders, mixed operational environments, and defective records of operating times. The result of this early data produced what appeared to be a random constant failure rate [Ohring 1998].

7.1.2. Weibull Distribution

The Weibull distribution is a commonly used distribution in reliability investigations because of its enormous flexibility to provide different shapes to fit life test data. The Weibull can be a two parameter or a three parameter model [Nelson 1982]. Equation 7.1.2-1 is the probability density function for the two parameter model.

$$f(T) = \frac{\beta}{\eta} \left(\frac{T}{\eta}\right)^{\beta-1} e^{-\left(\frac{T}{\eta}\right)^{\beta}} \quad (7.1.2-1)$$

In the above Equation η is termed the time scale parameter and β is termed the shape or slope parameter. By adjusting either or both of these parameters one can fit an extensive variety of time to failure data to a Weibull distribution. When $\beta = 1$ the Weibull becomes an exponential distribution. When $\beta < 1$ the distribution reflects a system with a failure rate that decreases with time and likewise when $\beta > 1$ it reflects a failure rate that is increasing with time (wear-out condition). When $\beta = 2$ it becomes a special case of the Weibull called the Rayleigh distribution which appears in the applications for failure related to corrosion. The time scale parameter (η) has the units

of hours, miles, cycles, etc. When η is changed it has the same effect as a change of the abscissa scale. If η is increased while β is held constant the net result is that the distribution becomes stretched out to the right.

7.1.3. Lognormal

The lognormal is employed for general reliability analysis and is commonly used to analyze cycles to failure of a particular structure or in fatigue life testing. Since the logarithms of a lognormally distributed random variable are normally distributed, the probability density function is given by Equation 7.1.3-1 [Crow 1988].

$$f(t) = \frac{1}{\sigma t \sqrt{2\pi}} e^{\left(\frac{-[\ln(t) - \mu]^2}{2\sigma^2}\right)} \quad (7.1.3-1)$$

Here, σ is the standard deviation of the natural logarithms of the times to failure obtained during life testing and μ is the mean of the natural logarithms of the times to failure or stated another way $\mu = \ln(t_{50})$ [Aitchison 1957]. The PDF starts at zero and is skewed to the right by increasing to its mode and then decreasing thereafter. When a product has initially high failure rates but are decreasing with time, σ is greater than 2. When σ is close to 1 the failure rate is roughly constant and when $\sigma = 0.5$ it is indicative of an increasing failure rate. So the lognormal can be applied to the bathtub curve reflecting early infant mortality failures, steady state constant failure rates, and wearout time regimes.

Weibull distributions are usually a better fit for failures related to short failure times whereas the lognormal is usually better for predicting longer failure times since the lognormal tends to apply when the failure mechanism involves gradual degradation over time such as diffusion, corrosion, and chemical processes [Evans 1970, Meeker 1984]. Weibull distributions are implemented in cases of the weak link propagates to failure such as dielectric breakdown and fracture un ceramics [Ohring 1998]. As far as this investigation is concerned, both the Weibull and Lognormal shall be considered as potential distributions to describe the life of the particular failure mechanism being investigated.

7.2. Stress Models

As systems are being designed better and better, they have become more reliable to the point where failure rates are extremely under normal use or ambient conditions. Therefore acceleration factors (AF) are employed to assist in evaluating the execution of accelerated life tests. The design of an accelerated life test has already been discussed in chapter 4 herein. This section covers how different types of stresses influence how the acceleration factor is influenced. Equation 7.2-1 reflects the ratio of the Mean Time To Failure (MTTF) between normal use stress level and an accelerated stress level.

$$AF = \frac{MTTF_{use}}{MTTF_{accel}} = \frac{Rate (accel)}{Rate (use)} \quad (7.2-1)$$

There are numerous types of stress models, but this section covers the three main types: the Arrhenius, the Eyring, and the Inverse Power Law. Each of these stress models can be inserted into the different life models (exponential, Weibull, Lognormal) by setting the mean life parameter equal to the life-stress relationship of that particular stress model as defined in the following sections.

7.2.1. Arrhenius Relationship

The most common stress relationship used in accelerated testing is the Arrhenius since it is very applicable when temperature is the used to accelerate failures [Goba 1969]. The reaction rate is given in Equation 7.2.1-1 where R is the speed of the reaction.

$$R(T) = Ae^{-\frac{E_A}{KT}} \quad (7.2.1-1)$$

The other variables being:

- A is a non-thermal constant parameter
- E_A is the activation energy with units in electron volts (eV)
- K is Boltzman's constant (8.617385×10^{-5} eV/K)
- T is temperature (Kelvin)

The activation energy is defined as the energy that a molecule in the structure must acquire to participate in a chemical reaction and is therefore a measure of the impact that temperature has on the reaction. When temperature is used to accelerate a test the acceleration factor is determined by Equation 7.2.1-2.

$$AF = \frac{MTTF_{use}}{MTTF_{accel}} = \frac{Ae^{-\frac{E_A}{KT_{use}}}}{Ae^{-\frac{E_A}{KT_{accel}}}} = e^{\left(\frac{E_A}{T_{use}} - \frac{E_A}{T_{accel}}\right)} \quad (7.2.1-2)$$

The next step is to employ this stress based relationship of mean life to applied stress into the general life models (exponential, Weibull, Lognormal). Figure 7.2.1-1 shows how this compound function is developed. For an exponential life distribution, the MTTF is equal to $1/\lambda$ and therefore this can be inserted into the original exponential Equation as defined in Equation 7.1.1-1. Hence, the Arrhenius-exponential PDF is defined in Equation 7.2.1-3 and it is now a function that is dependent on both time and temperature. Note that this is given as one example and it is beyond the scope of this thesis to provide all the different permutations.

$$f(T) = \lambda e^{-\lambda T}$$

$$MTTF = \frac{1}{\lambda} = Ae^{-\frac{E_A}{KT}}$$

Figure 7.2.1-1 Development of compound life-stress model

$$f(time, Temp) = \frac{1}{Ae^{\left(\frac{E_A}{Temp}\right)}} e^{\left[\frac{-time}{Ae^{\left(\frac{E_A}{Temp}\right)}}\right]} \quad (7.2.1-3)$$

7.2.2. Temperature-Humidity Stress Model

While the Arrhenius model is used for a single stress being temperature, the Temperature-Humidity model (T-H) is applied when there are both stresses at work during an accelerated life test. Equation 7.2.2-1 is the relationship of MTTF based on these two stresses (temperature and humidity), note that it is a variation of the Eyring model [Meeker 1998].

$$Life(V, U) = Ae^{\left(\frac{\phi}{V} + \frac{b}{U}\right)} \quad (7.2.2-1)$$

- Φ and A are constant parameters
- b is another parameter but is known as the activation energy for humidity
- U is the relative humidity
- V is temperature in Kelvin

Hence the acceleration factor for a test involving both temperature and humidity can be determined from Equation 7.2.2.-2, note that the constant A has cancelled out.

$$AF = \frac{MTTF_{use}}{MTTF_{accel}} = e^{\phi\left(\frac{1}{V_{use}} - \frac{1}{V_{accel}}\right) + b\left(\frac{1}{U_{use}} - \frac{1}{U_{accel}}\right)} \quad (7.2.2-2)$$

7.2.3. Inverse Power Law

The inverse power law is frequently used for modeling failure mechanisms that are dependent on mechanical stress. The stress model is given by Equation 7.2.3-1 as follows.

$$L(V) = \frac{1}{KV^n} \quad (7.2.3-1)$$

The parameters are defined as:

- L represents the quantifiable life measure
- V represents the stress level
- K is a constant parameter specific to the structure
- n is another constant parameter specific to the structure

The parameter n is an indicator of how much the stress impacts the life of the system or structure under test [Lawless 1976]. Since this investigation is centered on mechanical stress as a result of an external bending moment applied, the IPL stress model is the most appropriate model. The next section covers a discussion on other popular models closely related to the IPL model, but it describes the rationale for not selecting them.

7.2.4. Coffin-Manson and the IPL Relationship

When thermal cycling is used during an accelerated life test that results in low cycle fatigue, Coffin and Manson suggested that the cycles to failure as a function of the temperature range be defined as Equation 7.2.4-1 [Coffin 1954, Manson 1953].

$$N = \frac{C}{(\Delta T)^\gamma} \quad (7.2.4-1)$$

- N is cycles to failure (thermal cycles)
- C is a constant parameter (dependant on the metal employed in the structure)
- γ is a second constant parameter (also dependant on the metal employed)
- ΔT is the entire range of the temperature swing employed in the life test

Other similar relationships exist that are specific to unique life tests being performed. An example would be the Palmgren's Equation used to determine the B_{10} life of ball bearings.

7.3. Modeling Fatigue

There has been significant research in the area of fatigue testing. Since this investigation involves cyclic testing of the test structure being bent to a set radius of curvature, the following sections describe the three main approaches to modeling this type of behavior.

7.3.1. Stress-Life

The stress-life model is based on the Wohler S-N diagram, which is a plot of increasing mechanical stress (S) along the y-axis versus cycles to failure (N) along the x-axis. Figure 7.3.1-1 is an example S-N diagram. It is common to employ four-point loading to a specimen that produces a fully reversed uniaxial state of stress.

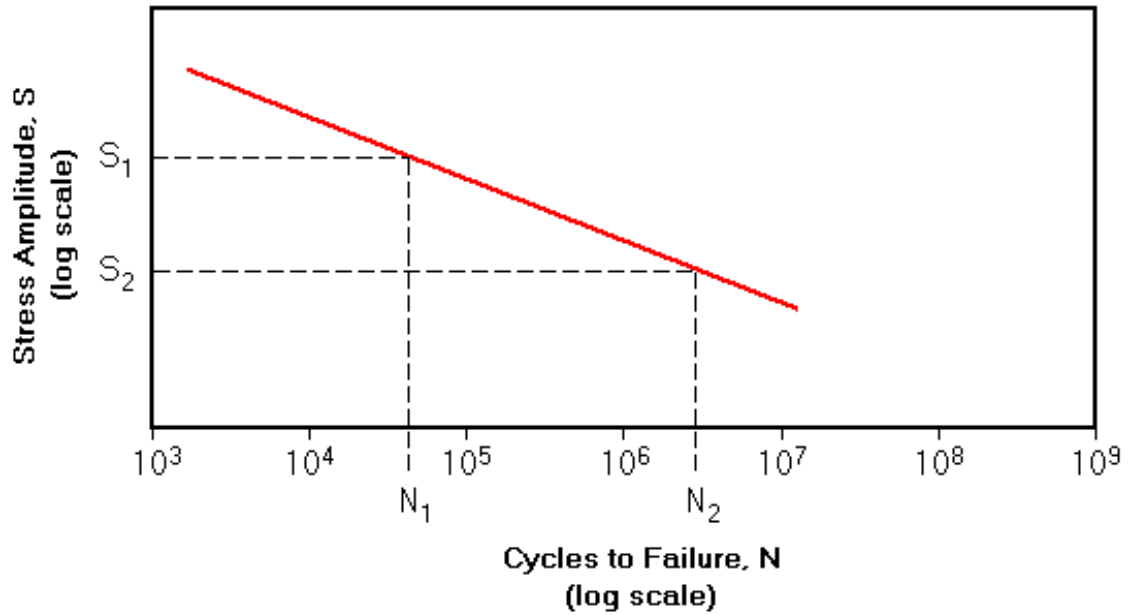


Figure 7.3.1-1 Example S-N Diagram

The main application of this approach is when the applied stress is primarily in the elastic region of the material under investigation and is commonly called high cycle fatigue [Juvinal 1967]. This model does not provide an accurate fit to the data when the applied strains have a significant amount of plastic deformation. Under these low cycle fatigue conditions, the strain-life model should be employed. The S-N method works well designs involving long life and constant amplitude. This method is empirical in nature and ignores the true stress-strain response of the material and does not distinguish between crack initiation and propagation. Equation 7.3.1-1 is the power relationship that defines the S-N curve, with C and b being determined from a slope and y intercept of the straight S-N line.

$$S = 10^C N^b \quad (7.3.1-1)$$

7.3.2. Strain-Life

Unlike the S-N approach, this method takes into account the actual stress-strain response of the material under investigation. Therefore, this method can be employed in situations where there are high strains, hence low cycle fatigue testing. Also, this method allows for the accurate modeling of the mechanism that leads to crack initiation. Another benefit of this method is that it can model the residual mean stresses resulting from the effects of sequence loading to allow for a more accurate estimates of cumulative damage as a result of the specimen being exposed to loads of different amplitudes. Other benefits include being able to consider device geometry, interaction of fatigue and creep, and the incorporation of transient material behavior [Bannantine 1990].

The drawbacks of the strain-life method are that it involves much more complicated levels of analysis, it only considers crack initiation (not propagation), still contains some empirical analysis (mean stress effects and notch size), and no defined way to take into account surface treatment or plating. Figure 7.3.2-1 is a diagram of a standard strain-life curve with cycles to failure on the x-axis and strain amplitude along the y-axis.

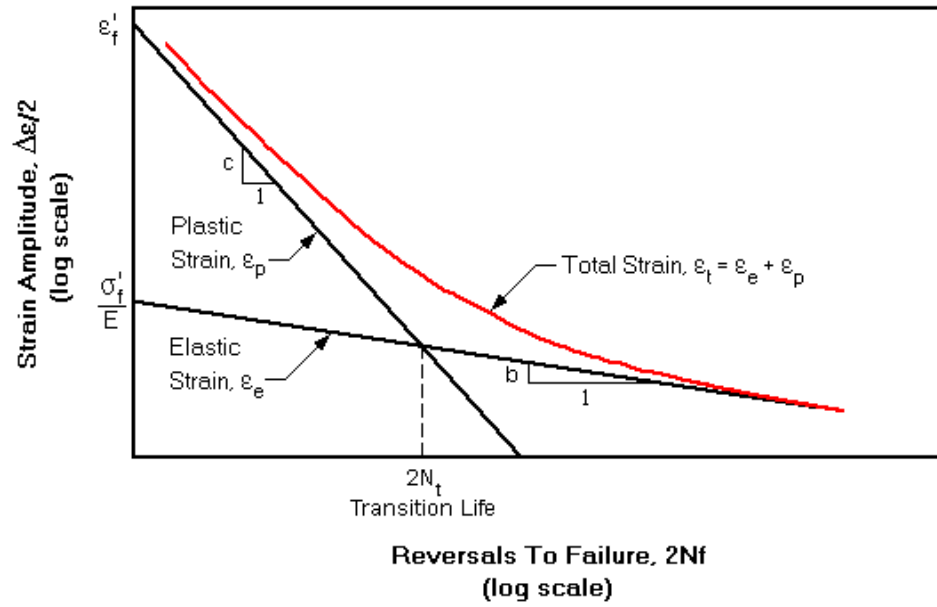


Figure 7.3.2-1 Example Strain-Life Curve

Equation 7.3.2-1 is used to determine the strain-life relation. The term on the left side of the Equation is the total strain amplitude that consists of an elastic component and a plastic component. The term $2N_f$ represents the number of reversals to failure. The exponents b and c represent the fatigue strength exponent and the fatigue ductility exponent respectively. The coefficients of fatigue strength and fatigue ductility are σ_f' and ϵ_f' respectively [Landgraf 1969].

$$\frac{\Delta\epsilon}{2} = \frac{\sigma_f'}{E} (2N_f)^b + \epsilon_f' (2N_f)^c \quad (7.3.2-1)$$

7.3.3. Fracture Mechanics

The fracture mechanics method, also termed linear elastic fracture mechanics (LEFM) is employed to determine the magnitude of mechanical stress near the crack tip based on remote stresses applied to the system, the shape and size of the crack itself, and the material properties of the crack. This is the only method of the three that deals with crack propagation and therefore gives insight into the actual mechanisms of fatigue. It is employed in situations whereby an initial existing flaw is assumed and is employed in large damage tolerant structures whereby crack growth can be tolerated (such as in aerospace applications). Figure 7.3.3-1 shows how the crack growth rate is plotted versus the range of the stress intensity factor as defined as the red curve. The black line is Paris' law being fitted to the quasi-linear portion of this curve on a log-log plot.

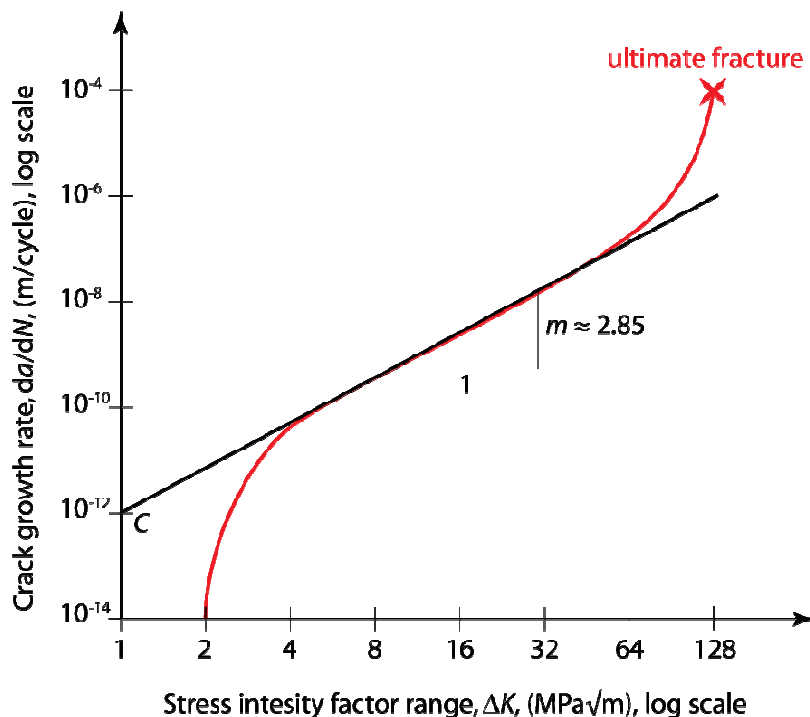


Figure 7.3.3-1 Crack growth rate as a function of stress intensity factor

Equation 7.3.3-1 is the Paris law model that defines the crack growth rate (da/dN) as the change in crack length (a) with the number of cycles (N) [Paris 1963]. Here the stress intensity factor, ΔK , depends on several key factors such as the magnitude of the loading, crack length, and device geometry. Both quantities (da/dN and ΔK) evolve during the fatigue testing until the specimen reaches failure. The parameters C and m of the Paris law model are determined graphically based on the y intercept and slope of the line on a log-log plot.

$$\frac{da}{dN} = C(\Delta K)^m \quad (7.3.3-1)$$

Hence the cycles to failure (N_f) can be calculated using Equation 7.3.3-2 as defined below.

$$N_f = \int_{a_i}^{a_f} \frac{da}{C(\Delta K)^m} \quad (7.3.3-2)$$

The drawbacks of this method involve the inability to deal with the initiation of a crack [Bannantine 1990]. The requirement to determine the stress intensity factor may prove very difficult for systems with complex geometries. In situations with significant plastic deformation, the linear elastic approach is not valid and elastic-plastic fracture mechanics must be employed and this tends to make the analysis extremely difficult.

7.3.4. Comparison of Fatigue Models

Each of the three main models has advantages and drawbacks as mentioned above. Since this investigation is interested in cycles to failure and not interested in attempting to physically measure crack propagation, the stress-life model is the most applicable to the accelerated life test defined in chapter 4. This fatigue model fits directly with the inverse power law stress model as defined in section 7.2.3.

7.4. Parameter Estimation Technique

When it comes to estimating model parameters based on raw data from a life test, there are three main methods. The first is regression analysis that is a common and easily understood approach that will be covered in section 7.4.1. A more robust method is the maximum likelihood method that shall be covered in section 7.4.2. Lastly, the least common method, Bayesian estimation process, shall be covered in section 7.4.3.

7.4.1. Rank Regression Analysis

Prior to dedicated software programs, reliability engineers would manually plot time to failure data and attempt to fit a line that best fit the data points. The rank regression or also called the least squares method is a more formalized process over the manual method by using a mathematical approach to fitting a line to the data points. The data is plotted on a graph with the x-axis representing times or cycles to failure and the y-axis represents the estimate of unreliability (1-R).

The next step is that a straight line is fitted to the data that optimizes its fit by minimizing the value of the sum of the squares of the difference between the actual data points and the potential straight line. Figure 7.4.1-1 shows both regression on the y-axis as well as regression on the x-axis.

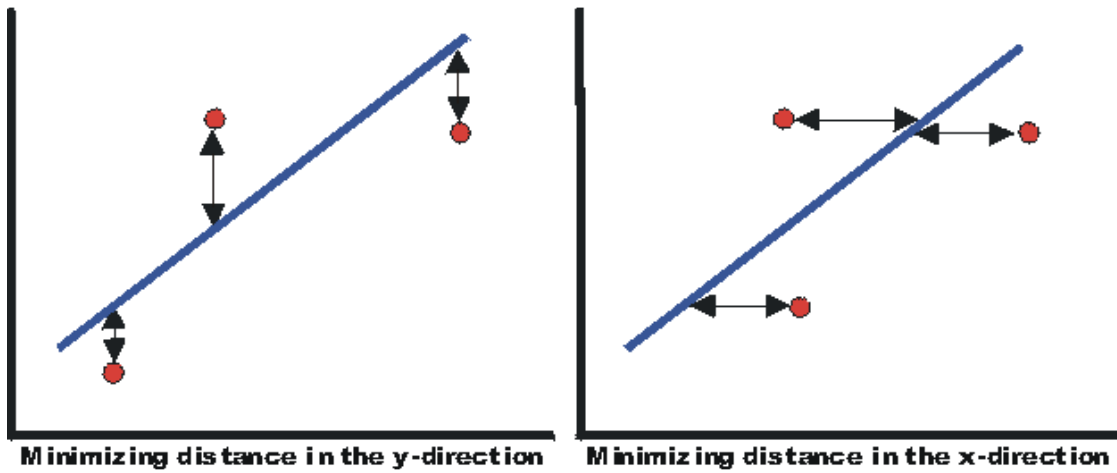


Figure 7.4.1-1 Regression Analysis in both y-axis and x-axis

The straight line takes the standard linear form $y = ax + b$, and Equation 7.4.1-1 is employed to determine rank regression in the y direction in order to determine least squares estimates of a and b in the linear Equation (note that \hat{a} in the Equation is the least squares estimate of a).

$$\sum_{i=1}^N (\hat{a} + \hat{b}x_i - y_i)^2 = \min(a, b) \sum_{i=1}^N (a + bx_i - y_i)^2 \quad (7.4.1-1)$$

Another benefit of the rank regression method is that it provides for a goodness of fit parameter, also known as the correlation coefficient (ρ) and it is defined in Equation 7.4.1-2. In the Equation, the parameter σ_{xy} is the covariance of x and y , and the parameter σ_x is the standard deviation in x , and the parameter σ_y is the standard deviation in y . The closer the correlation coefficient value is to 1 the better the fit of the line is to the data. Hence, a value of 1 means that the line is a perfect fit and therefore all the failure data points lie directly on the line [Reliasoft 2000].

$$\rho = \frac{\sigma_{xy}}{\sigma_x \sigma_y} \quad (7.4.1-2)$$

The rank regression technique is most useful when the underlying function that the data points represent is a linear function. The correlation coefficient also provides a sanity check for the distribution parameters to the life test data. The rank regression technique is best employed when analyzing life test data that contains individual single times to failure and does not have censored or interval data.

7.4.2. Maximum Likelihood Estimation

The Maximum Likelihood Estimation (MLE) technique attempts to determine the most likely values of the distribution parameters from a set of life test data points by maximizing the value of the “likelihood function”. The likelihood function is based on the probability density function for a given distribution. For a 2 parameter Weibull the variables of interest would be β and η . The likelihood function is computed by taking the product of the pdf functions with one element for each data point from the life test as shown in Equation 7.4.2-1

$$\Lambda = \ln(L) = \sum_{i=1}^n \ln f(x_i; \theta_1, \theta_2, \dots, \theta_k) \quad (7.4.2-1)$$

In the above equation $f(x; \theta_1, \theta_2, \dots, \theta_k)$ is a generic pdf with x representing the life data (times to failure), and n is the number of total failures from the life test. The only reason the logarithm of L is taken is due to the fact that it is easier to work with smaller numbers. This function can then be plotted as shown in Figure 7.4.2-1. The idea is to determine the values of θ_1 and θ_2 or for the two parameter Weibull (θ and β) that produces the highest value of the function. The most common way of obtaining this solution is to take the partial derivative of the log-linear Equation for each parameter and setting it equal to zero as defined in Equation 7.4.2-2.

$$\frac{\partial \Lambda}{\partial \theta_j} = 0, \quad j = 1, 2, \dots, k \quad (7.4.2-2)$$

This procedure results in a set of Equations with an equal number of unknowns and therefore the unknowns can be solved simultaneously. A distinct advantage for the MLE approach is that it can take into account suspension times, from life testing. Other methods such as probability plotting and rank regression can only consider relative locations of the suspensions. The MLE method becomes more powerful with more data points since it is asymptotically consistent. MLE estimate starts to converge on the true values of the underlying model parameters with more data points obtained from life testing. There are also unique situations when the MLE asymptotic principles become cumbersome. One example is with the three-parameter Weibull distribution and when the location parameter has a value close to 1 [Reliasoft 2007].

As a rule of thumb, it is best to employ the rank regression technique when the sample sizes from life testing are relatively small and do not contain much if any censoring. When the life test data has a reasonable number of data points and contains a lot of censoring, then it is best to employ the Maximum Likelihood Estimation method.

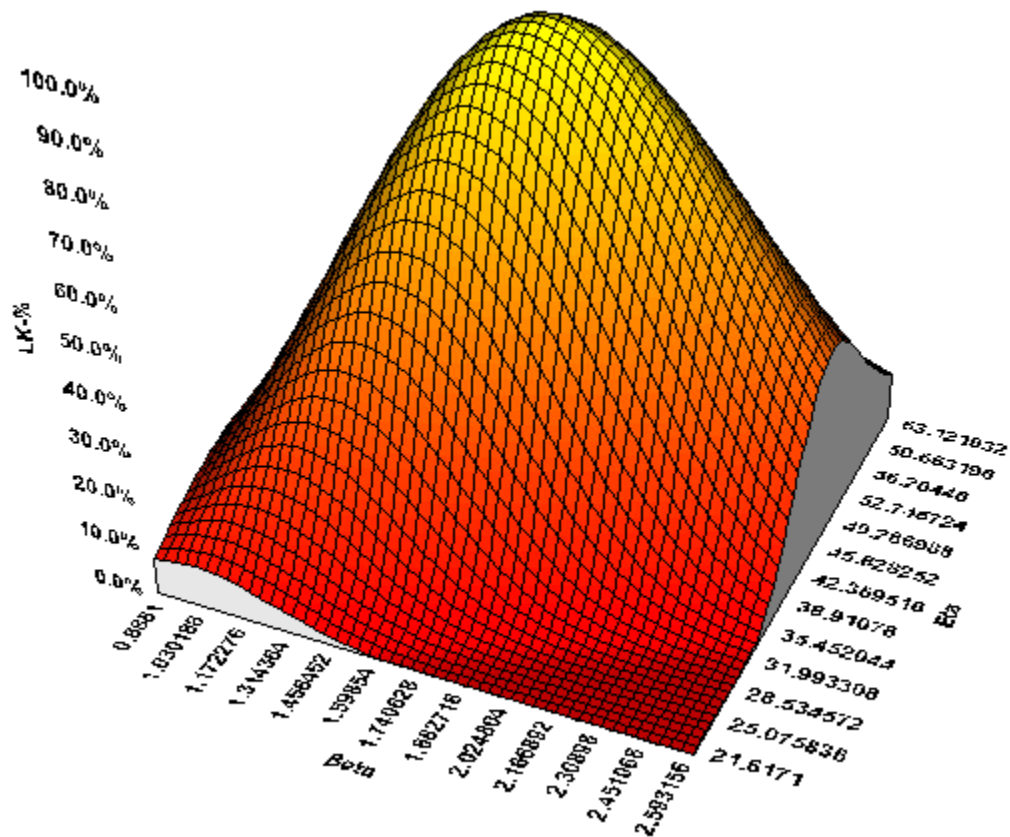


Figure 7.4.2-1 Maximum likelihood function surface for a two parameter Weibull

7.4.3. Bayesian Analysis

Baye's rule allows for a general framework of combining prior knowledge about a parameter of a distribution with new data obtained from a life test in order to make new and improved inferences about the distribution of the parameter. Equation 7.4.3-1 is the posterior probability density function using Baye's rule.

$$f(\theta|D) = \frac{L(D|\theta) \cdot \varphi(\theta)}{\int L(D|\theta) \cdot \varphi(\theta) d\theta} \quad (7.4.3-1)$$

In the above Equation, the random variable θ is the parameter that one is attempting to estimate using limited data from a recently executed life test (D). So $f(\theta|D)$ is the posterior distribution based on a combination of previous historical knowledge of θ , also termed the prior distribution $\varphi(\theta)$, and $L(D|\theta)$ is the likelihood function based on the chosen distribution and data from the life testing [Rausand 2004].

7.4.4. Comparison of Parameter Estimation Techniques

Since a prior distribution does not currently exist for cycles to failure of ITO interconnects on flexible substrates, the application of the Bayesian technique is not applicable at this time. Although once a baseline life model has been established, future investigations may take advantage of the Bayesian technique.

7.5. Analysis of Models Based on Life Data

The probability density functions of the IPL-Weibull life model and the IPL-Lognormal life model are given in Equations 7.5-1 and 7.5-2 respectively. Each pdf is

a function of t and V whereby t represents cycles to failure and V is the mechanical stress as a result of the radius of curvature.

$$f(t, V) = \beta K V^n (t K V^n)^{\beta-1} e^{-(t K V^n)^\beta} \quad (7.5-1)$$

$$f(T, V) = \frac{1}{T\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{T' + \ln(K) + n \ln(V)}{\sigma}\right)^2} \quad (7.5-2)$$

Reliasoft's Weibull++ software was used to calculate the correlation coefficients for both the Weibull and Lognormal distributions using rank regression on the x-axis for the data at each of the stress levels as shown in Table 7.5-1.

Table 7.5-1 Comparison of Weibull and Lognormal goodness of fit

	Weibull			Lognormal		
	β	η	ρ	μ	σ	ρ
R1	5.243	29.9655	0.9415	3.3001	0.2387	0.9668
R2	4.7488	15.2413	0.9817	2.6136	0.2541	0.09718
R3	3.0204	7.3591	0.994	1.8224	0.4004	0.9862

Both distributions have high correlation values, but the Weibull is slightly higher on average. Therefore, the IPL-Weibull distribution was selected as the preferred life-stress model. Next, the data was analyzed using Reliasoft's ALTA software to perform maximum likelihood estimation for K , n , and β as well as confidence limits as shown in Table 7.5-2.

Table 7.5-2 Weibull parameter estimation for 15um trace data

	Lower 95%	Lower 90%	Point Estimate	Upper 90%	Upper 95%
K	2.61E-5	3.68E-5	7.08E-5	10E-5	20E-5
n	0.8466	0.8966	0.9910	1.0855	1.1355
β	3.31	3.65	4.39	5.27	5.82

The life versus stress plot for 15um traces at each of the three different stress levels is provided in Figure 7.5-1. Therefore, there were 3 different life tests run for the 15um traces and each resulted in a distribution.

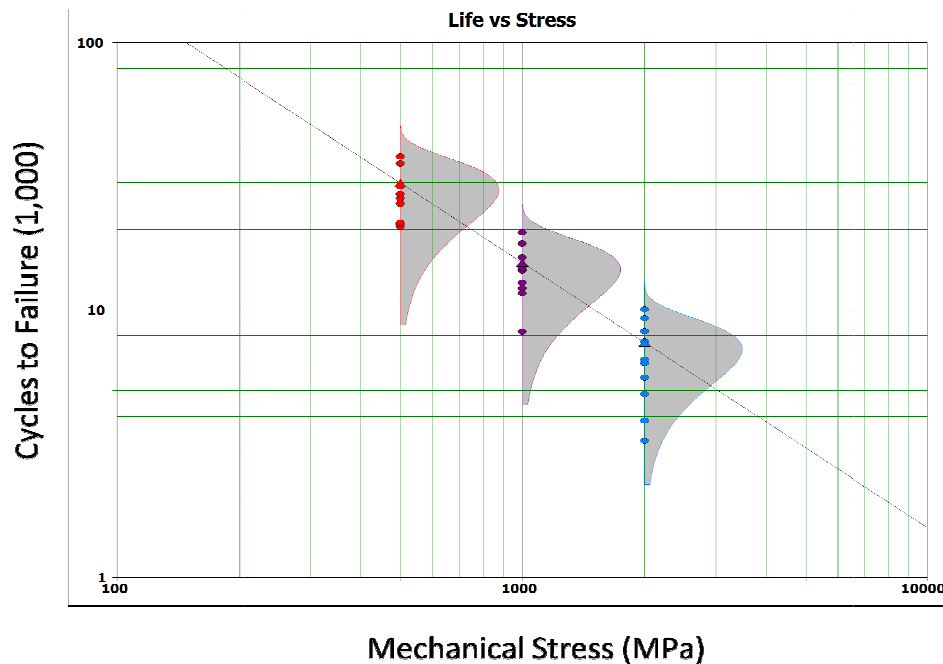


Figure 7.5-1 Life-stress plot of 15um traces

At each stress level, testing was conducted on three different trace widths (15, 7.5, and 5um). This resulted in a total of 9 distributions. It was apparent that the K model

parameter varied as a function of trace width as shown in Figure 7.5-2. A function was fitted to this curve resulting in a relationship of K as a function of trace width provided in Equation 7.5-3.

$$K = 2.5E^{-5}(\text{Trace Width})^{0.38} \quad (7.5-3)$$

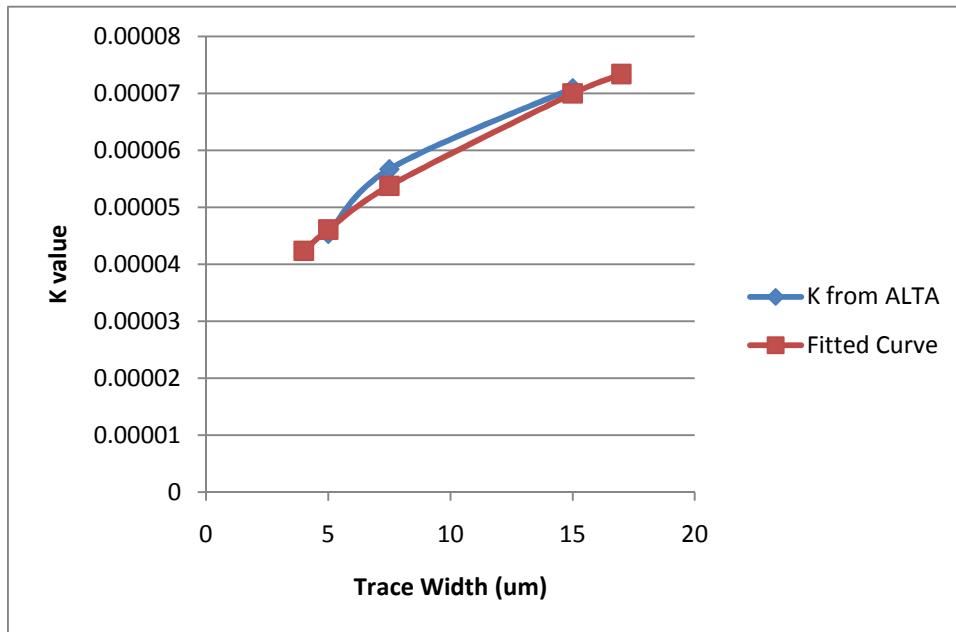


Figure 7.5-2 Plot of K model parameter as a function of trace width

7.6. Summary of Resulting Life-Stress Model

Given that the failure mechanism is channel cracking of a thin film, the appropriate stress model employed was the IPL (Inverse Power Law) model. Of the numerous life models available, the two most appropriate were the Weibull and lognormal

distributions. The process used special software to compute model parameters and using rank regression on the x-axis, the best fit life model was selected to be Weibull. Therefore, the IPL-Weibull model was selected as the life-stress model. The specific model parameters were determined using maximum likelihood estimation techniques under three separate stress conditions. The K value of the model varied as a function of trace width and this relationship was determined using curve fitting techniques.

Chapter 8: Conclusions and Future Research

8. Overview

This is the final section of the thesis. This chapter first provides a breakdown of the process that was employed throughout this research project starting from the identification of the problem of flexible displays through the eventual stress-life relationship that characterizes the reliability of displays when subjected to field use of cyclic mechanical stress. Next, this chapter highlights the contributions of this work in terms of the impact to the research community both in terms of specific life-stress relationships for the particular flexible display design identified in chapter one as well as an overall approach for qualifying future designs prior to mass production. The last section provides suggested areas of research that may continue enriching our understanding the stress-life relationships involved in flexible displays as well as improvements in the design to make it more robust to harsher field use conditions.

8.1. **Summary of Results**

A systematic process has been followed in this investigation. Figure 8.1-1 is a visual perspective of the overall high level view process followed. It starts with the failure as observed by the end user and ends with the life-stress relationship that provides a mathematical representation of the physical stresses and their impact on the display's reliability.

As the figure progresses downward, the main steps are highlighted. The first step was the determining the failure mode that was associated with the failure conditioned observed by the end user at the system level. Once the failure mode was determined the failure threshold was determined through circuit simulation. A physical model was used to associate the change in resistance to cracks in the traces. Next, the failure mechanism that is it the root cause of the failure mode was analyzed through finite element analyses. The agent of failure that accelerates the failure mechanism was determined and this formed the basis for designing an accelerated life test. As one progresses back up the V figure, the system and fixture used to execute the accelerated life test was designed and executed. The data was collected and using Maximum Likelihood Estimation (MLE) techniques parameters of the life-stress model were determined.

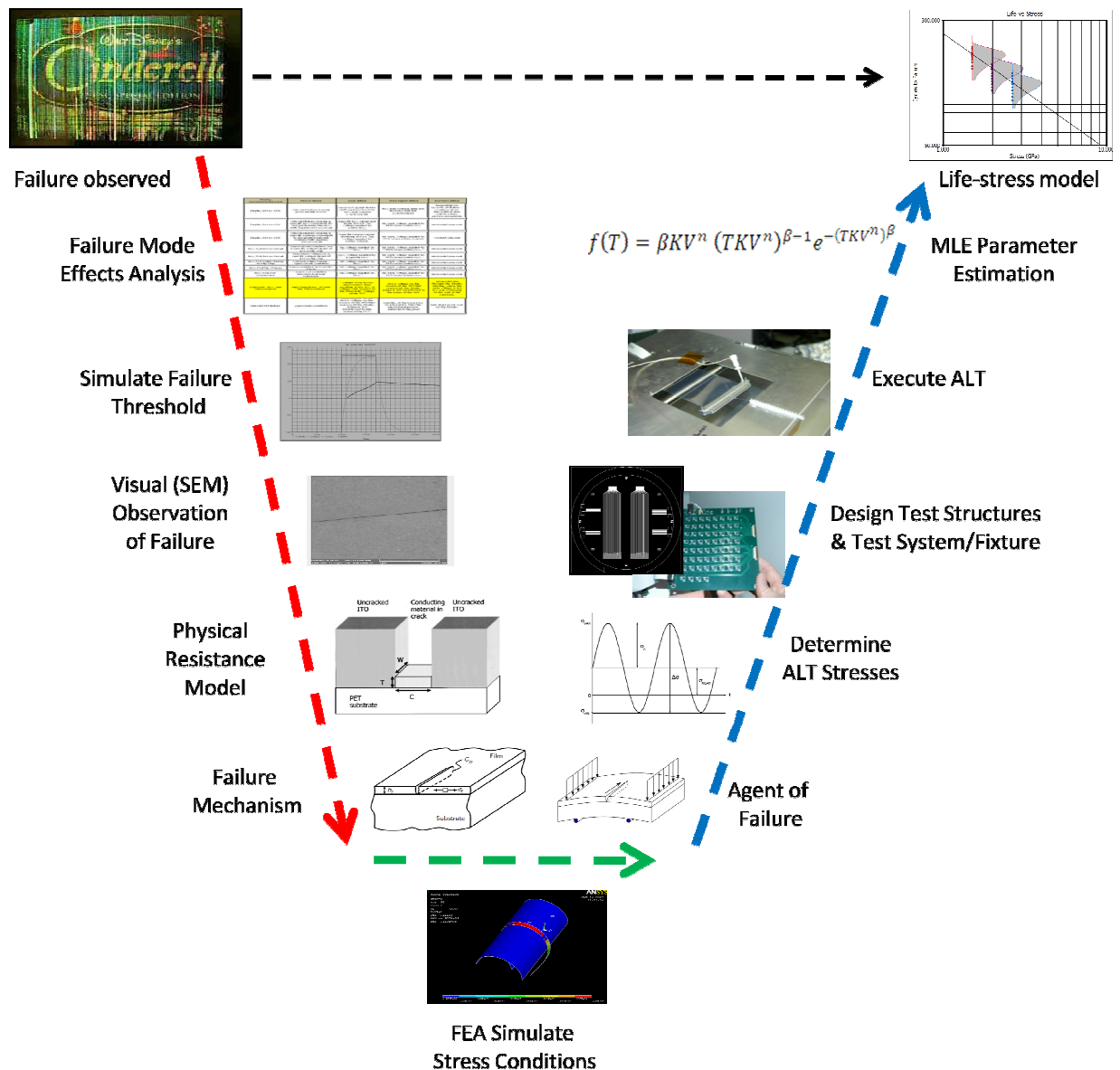


Figure 8.1-1 Top Level Overview of Process for Investigation

A more detailed breakdown summary of the process without visual cues is provided in Figure 8.1-2. In the figure there are three main columns: process steps, worked performed, and the specific results obtained from each of the steps.

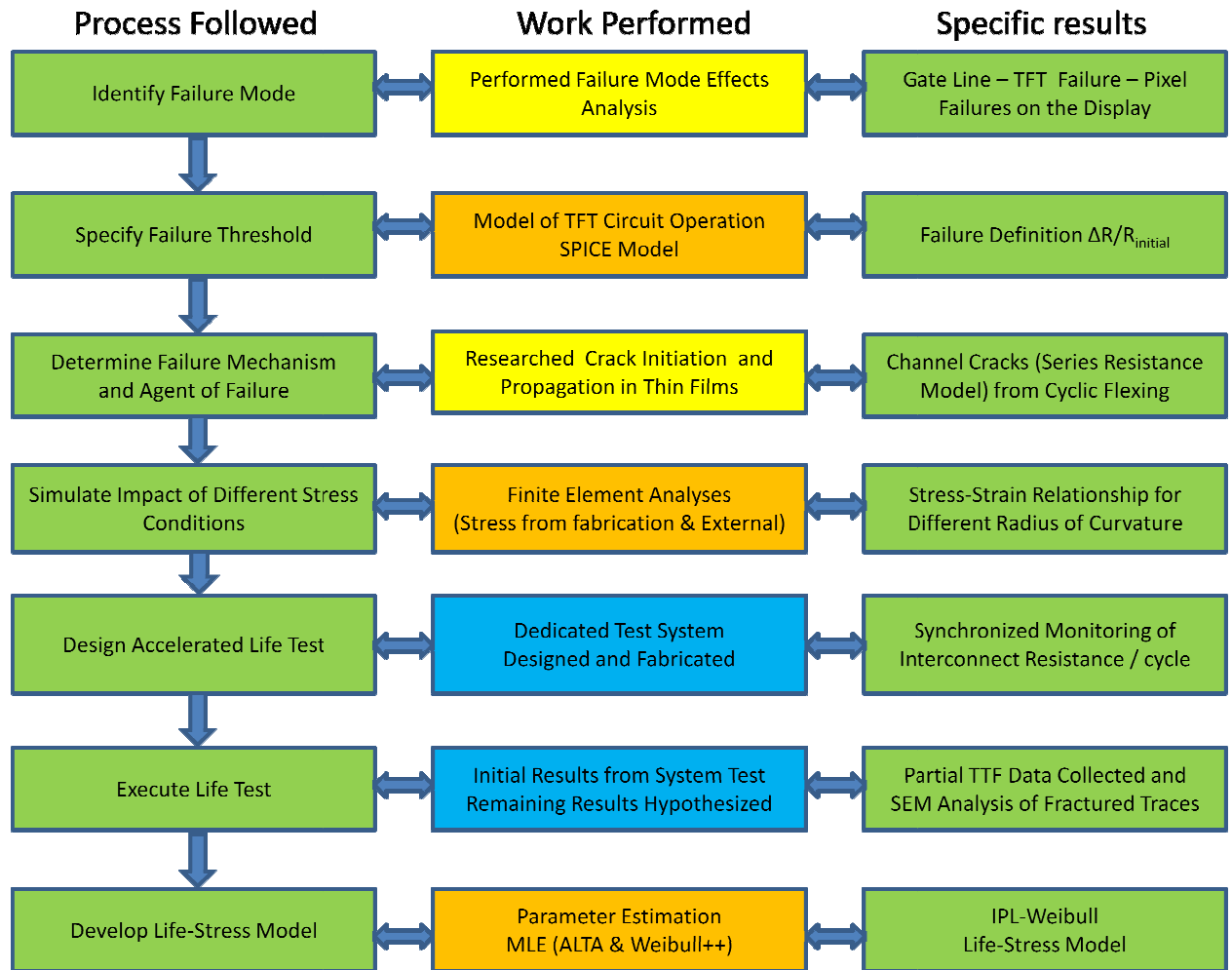


Figure 8.1-2 Block diagram of process, work, and results

The problem being addressed by this thesis is: *What is an appropriate process for rapidly determining the life-stress relationship of gate line interconnects and using this relationship in the qualification of current and future flexible display designs.*

This investigation concluded the following:

- Failure mode associated with the end item effect needs to be identified
- Failure threshold needs to be established
- Failure mechanism and associated agent of failure need to be understood
- Finite Element Analysis is needed to corroborate stress levels to failure mode
- Design of the Accelerated Life Test has to focus on the agent of failure
- Test structures and test system design are required to facilitate life testing
- Stress models need to be selected based on the underlying physics of failure
- Understanding the relationship of life model parameters to stress is paramount
- Addressing the Influence of physical device attributes on model parameters
- Qualification of design entails extrapolation of life distribution to use stress levels

8.2. Contributions

Due to continuous advancements in flexible display technologies, from novel materials to unique fabrication techniques, it is apparent that a need exists for a method to rapidly test and assess their impact on reliability from a myriad of inter-related conditions. With respect to contribution to the research community and general body of knowledge of flexible displays, this investigation has three main elements.

The first contribution has been the design and fabrication of a dedicated test system to successfully capture dynamic changes in electrical performance of novel flexible test structures under accelerated cyclic bending stress conditions.

The second contribution has been the development and analysis of two finite element models of a specific test structure that is representative of an actual design in use for a current flexible display product. The first model is dedicated to determining built in stresses that arise from fabrication and the second model is dedicated to predicting stresses in the thin films when the structure is mechanically bent to a particular radius of curvature.

The third and final contribution of this research is a framework for a methodology of testing and qualifying future multilayer interconnect designs on flexible substrates. This is achieved by a combination of the test system, finite element analysis of the test structure to characterize the failure mechanism, accelerated life testing, and Mean Time to Failure (MTTF) life-stress models.

Figure 8.2-1 shows how one may take the current design as fabricated and experiment with different trace widths and extrapolate their reliability as a function of being subjected to being flexed to a particular radius of curvature.

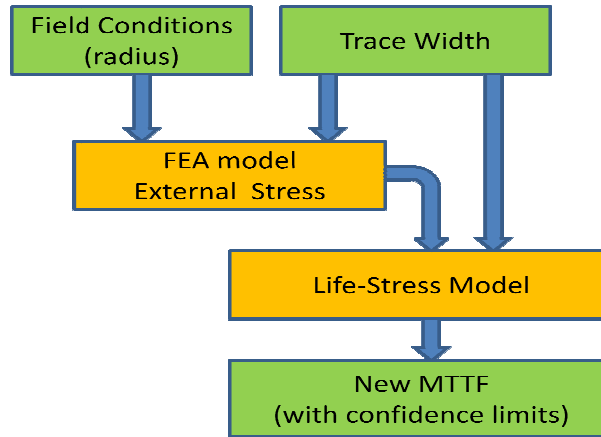


Figure 8.2-1 Impact of field conditions and trace width on MTTF

This work provides the framework for qualifying new designs that may include novel materials, unique device geometries, and/or lower processing temperatures. The approach of this qualification method is outlined in Figure 8.2-2.

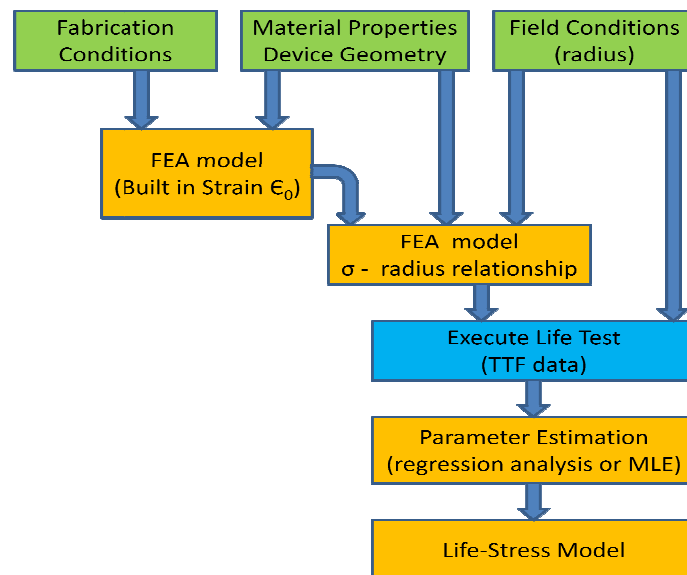


Figure 8.2-2 Method for qualifying potential future interconnect designs

8.3. Future Research

With respect to future research, there are several main categories that future work may fall into. The first category is the continuation of understanding of the understanding of this particular failure mode with respect to other failure mechanisms. This research focused on mechanical forces that placed the traces in tension. If the display were bent or rolled up in the other direction, then the traces would be placed in compression instead of compression. Chapter 2 touched on this topic slightly, but this failure mechanism is completely different in that there are situations of de-bonding of the traces from the substrate and eventual buckling of the traces.

The second category involves improving on the robustness of the gate line reliability though areas such as using new materials in the stack up (substrate, buffer layers, gate line interconnect layer). There is exiting research in the area of using carbon nanotubes [Hu 2010] in place of traditional materials such as aluminum, molybdenum, and ITO. Device geometry also can play an influence with respect to trace width and height.

Another potential area to investigate to improve the robustness of traces would be to run parallel traces to isolate cracks that initiate in one parallel trace and prevent them from propagating across the other parallel traces. Figure 8.3-1 is a sample diagram showing this strategy.

In all of the above mentioned areas for potential future research, the qualification process outlined herein would become the foundation for performing these works.

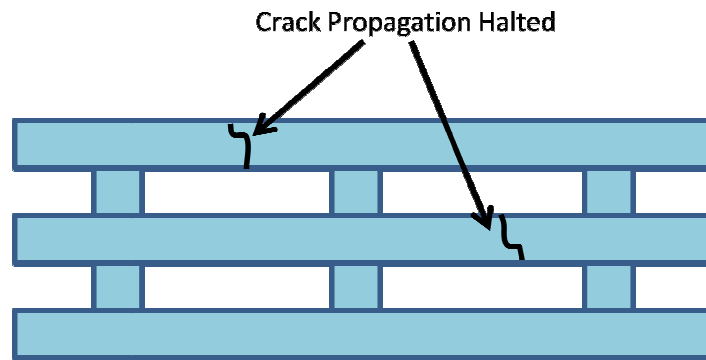


Figure 8.3-1 Redundant parallel lines mitigates the impact of crack propagation

The third category of future research involves the investigation of completely different failure modes. This research isolated one particular failure mode – that of the gate line interconnects. There are numerous failure modes associated with the source lines, the thin film transistors, the electro-optical material, the encapsulation/barrier layer to name just a few. In any case the end user is most interested in the reliability of the flexible display so one shall need to determine the impact of these multiple failure modes.

For instances of multiple failure modes, the dominant failure mode is a mode that is most likely to cause the first failure in the system. These failure modes will compete for failure of the system. The concept of “competing failure modes” can be addressed probabilistically as shown in Figure 8.3-2 which depicts time to failure distributions and their means arising from three competing failure sources [IEEE 2002]. In this

instance, the first failure could be attributed to any of the three failures modes, however failure modes one is clearly dominant.

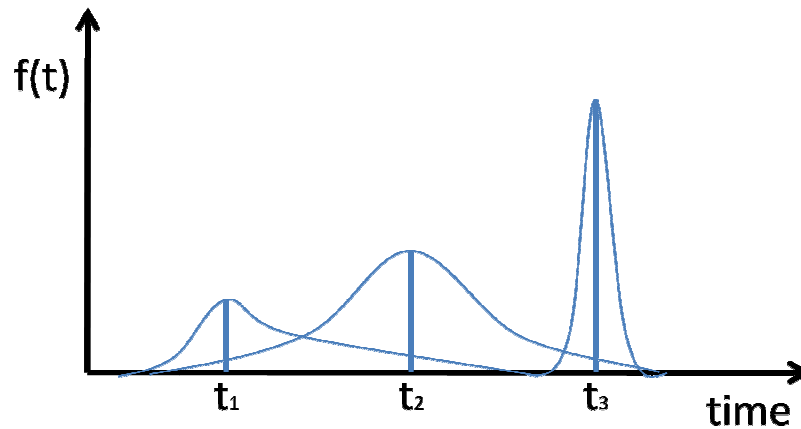


Figure 8.3-2 Probability density functions of three competing failure modes

Another way of viewing the competing failure mode data is to independently plot the cumulative density function of unreliability $F(t)$ versus time for each of the failure modes. Figure 8.3-3 is an example of two failure modes plotted on Weibull paper using Reliasoft's Weibull++ program.

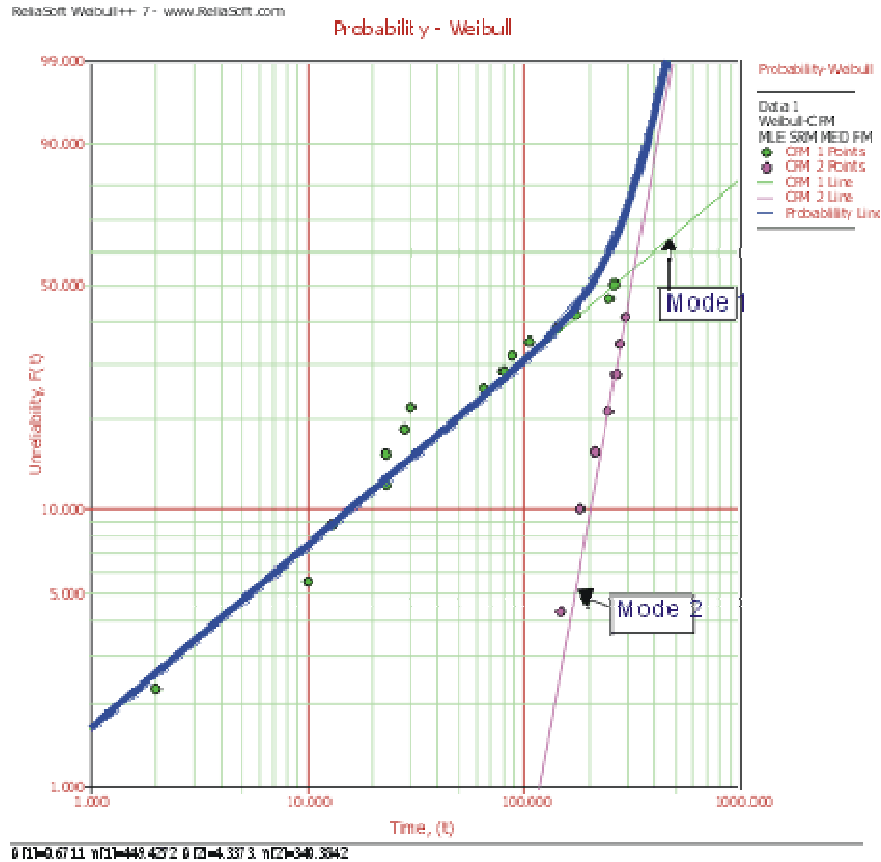


Figure 8.3-3 Weibull plot of two competing failure modes

Using system reliability theory practices, the reliability of the entire flexible display can be viewed as a system of (n) components. The reliability block diagram would view each of these elements as being in series and therefore the reliability of the system would be defined by equation 8.3.-1 with $R_s(t)$ being the reliability of the system.

$$R_s(t) = R_1(t) \times R_2(t) \times \dots R_n(t) \quad (8.3-1)$$

Applying this approach, the pdf of the system with two competing failure modes may resemble that shown in Figure 8.3-4.

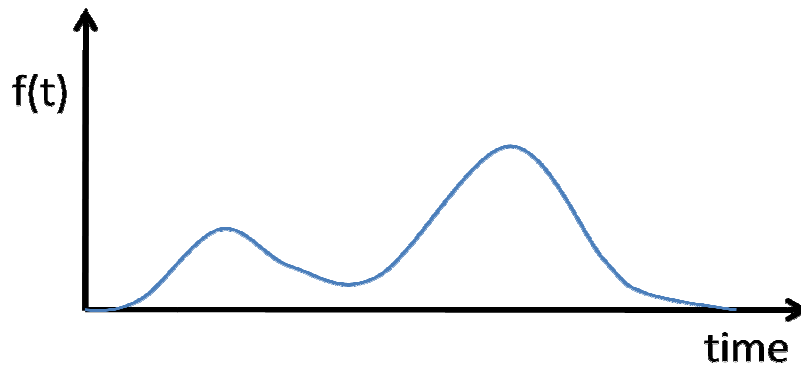


Figure 8.3-4 PDF of a system with competing failure modes

8.4. Closing Remarks

The evolution of display technology has moved from cathode ray tubes, to flat panel displays, and now to making displays flexible. This major paradigm shift has not only opened up new avenues for display applications, but also significant hurdles with respect to reliability.

A whole new set of aspects are required when considering field use conditions since there are brand new failure modes resulting from unique failure mechanisms never before encountered with traditional style displays. Due to continuous advancements in flexible display technologies, from novel materials to unique fabrication techniques, it is imperative to have a qualification method that allows for a rapid assessment of their impact on reliability from a myriad of inter-related conditions. It is the intention of this work to allow for a foundation for future research in this area.

Appendix A

Table Appendix-1 Simulated Cycles to Failure Data

Trace Number	Trace Width	R1 cycles to failure	R2 cycles to failure	R3 cycles to failure
#	um	k cycles	k cycles	k cycles
31	5	45.22	22.15	10.18
32	5	40.78	27.65	12.98
33	5	38.95	22.43	14.55
34	5	32.66	21.91	6.01
35	5	58.42	24.51	5.06
36	5	55.05	30.47	9.88
37	5	33.09	18.79	7.56
38	5	31.97	12.96	15.69
39	5	55.14	18.01	11.91
40	5	42.35	19.72	8.72
41	7.5	36.18	17.72	8.14
42	7.5	32.62	22.12	10.38
43	7.5	31.16	17.94	11.64
44	7.5	26.13	17.53	4.81
45	7.5	46.74	19.61	4.05
46	7.5	44.04	24.38	7.90
47	7.5	26.47	15.03	6.05
48	7.5	25.58	10.37	12.55
49	7.5	44.11	14.41	9.53
50	7.5	33.88	15.78	6.98
51	15	28.94	14.18	6.52
52	15	26.10	17.70	8.31
53	15	24.93	14.36	9.31
54	15	20.90	14.02	3.85
55	15	37.39	15.69	3.24
56	15	35.23	19.50	6.32
57	15	21.18	12.03	4.84
58	15	20.46	8.29	10.04
59	15	35.29	11.53	7.62
60	15	27.10	12.62	5.58

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