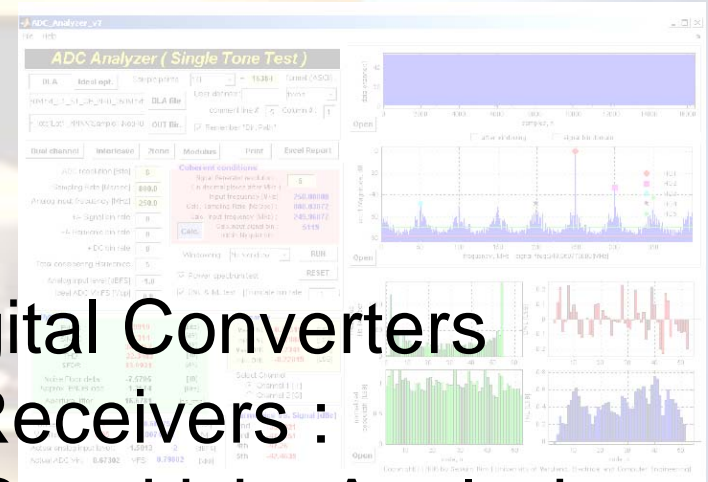




High-Speed Analog-to-Digital Converters for Modern Satellite Receivers : Design Verification Test and Sensitivity Analysis



Ph.D. Dissertation Exam
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Seokjin Kim

Analog & Mixed-Signal System Design Lab.
Electrical and Computer Engineering
University of Maryland, College Park



Acknowledgements

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- Analog & Mixed-Signal System Design Laboratory



Agenda

- Motivation & objective
- Contributions & publications
- Overview of analog-to-digital converters (ADCs)
- Design verification test (DVT) outline
- High-speed ADC architecture: **New result**
- ADC design verification test (DVT) software
- ADC DVT methodology
- Production test checklist
 - Automated test equipment (ATE)
- ADC corner lot study as a sensitivity analysis
- Conclusions



Motivation & Objective

- Motivation:
 - To provide a cost-effective test stand capable of evaluating high-speed ADC systems in a modern satellite receiver
 - To help many of high-speed ADC design/test engineers in both industry and academia
- Objective:
 - to develop full production–ready cost effective design verification test methodology for a high-speed ADC
 - Case study for a high-speed ADC:
 - Design-for-Test (DfT) enhanced approach
 - Testability
 - Develop concurrent engineering design verification test (DVT) procedure
 - DVT program (test flow, test plan) – VTS suite
 - Cost-effective ATE solutions



Contribution

- To provide detailed and generalized High-speed ADC testing methodology
 - Improved methodology for dynamic performance testing of ADCs for satellite communications
- Verification tool development: ADC verification test software (VTS) Suite
 - provide enough background of High-speed ADC
 - ▶ ATE ready
 - ▶ Technician level or entry-level engineer can run accurate ADC test
 - someone who is not familiar with ADC or RF testing could understand it
- Integrated Design-for-Test (DfT) concept as a part of process
 - Important case study for a high-speed ADC design
- RF design & measurement techniques
 - Socket design
 - Prototype device characterization & production-ready
 - Device interface board (DIB) design for high-speed mixed-signal applications
 - Intermodulation and IP3
- First time high-speed ADC design parameters sensitivity analysis → corner lot study
 - To determine the impact of process variations and to analyze the sensitivity of the ADCs to critical process parameter variations
 - Manufacturing yield



Related Publications

- **Published:**

- **Seokjin Kim**, Radmil Elkis, and Martin Peckerar, “Device Verification Testing of High Speed ADCs in Satellite Communications Systems,” in *IEEE AUTOTESTCON (System Readiness Technology Conference)*, 2007

→ **IEEE Instrumentation & Measurement Society (IMS)
Best Student Paper Award**



- **Seokjin Kim**, Radmil Elkis and Martin Peckerar, “Corner Lot Process Variation Effects on High Speed ADCs for Satellite Receivers,” in *IEEE ISDRS*, 2007
- **Seokjin Kim** and Martin Peckerar, “High Speed Analog-to-Digital Converter Design Verification Tests in Satellite Receivers,” in *IEEE ISCIT*, 2007

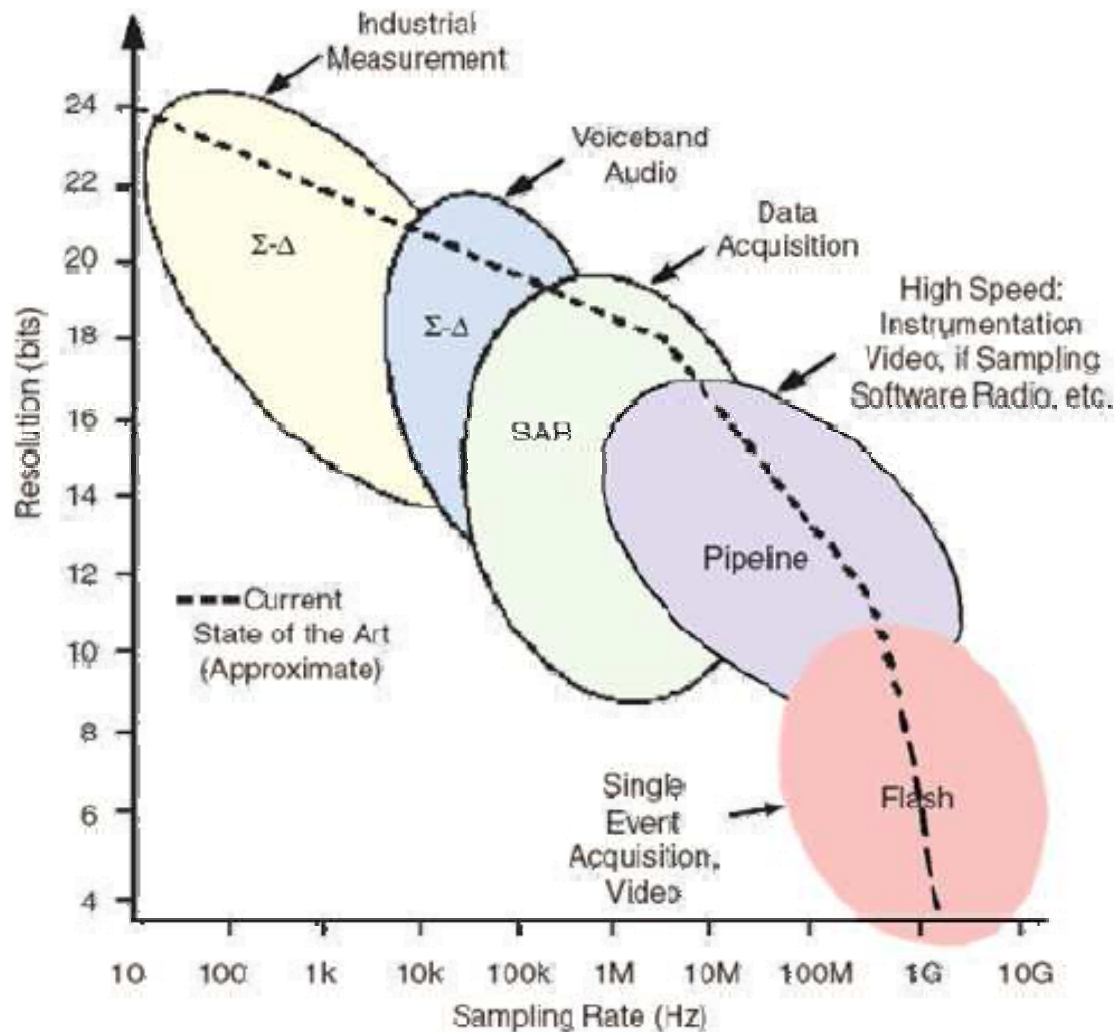
- **Accepted for Publication:**

- **Seokjin Kim**, Radmil Elkis, and Martin Peckerar, “Device Verification Testing of High Speed ADCs in Satellite Communication Systems,” in *IEEE TIM, special-issue*, 2008
- **Seokjin Kim**, Kwangsik Choi, Martin Peckerar and Aris Christou, “Line-spike Induced Failure in Integrated Circuit Bond-wires,” in *IEEE IRPS*, 2008



Overview of ADCs

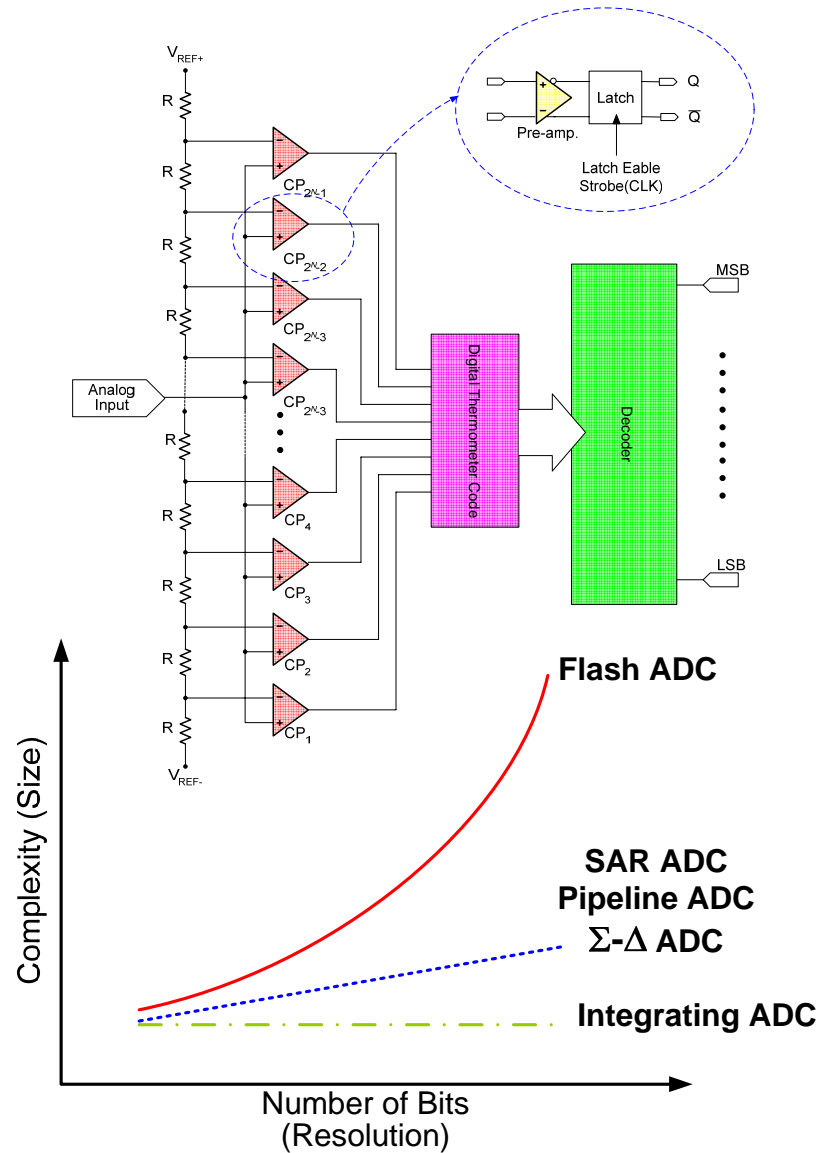
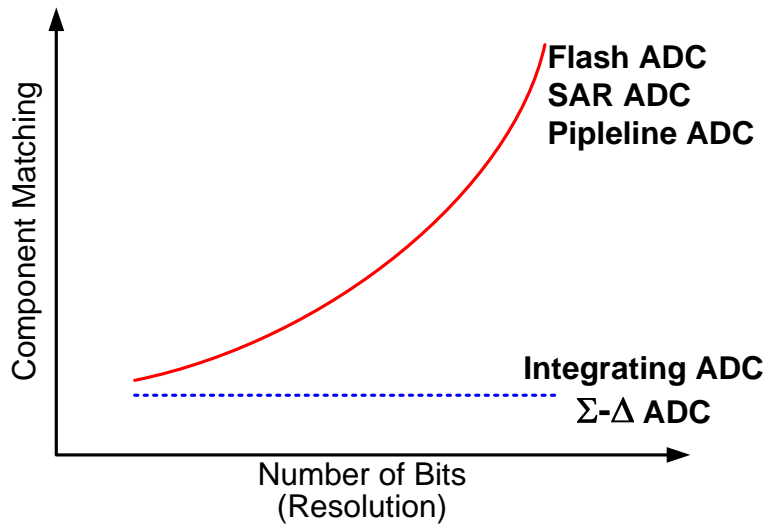
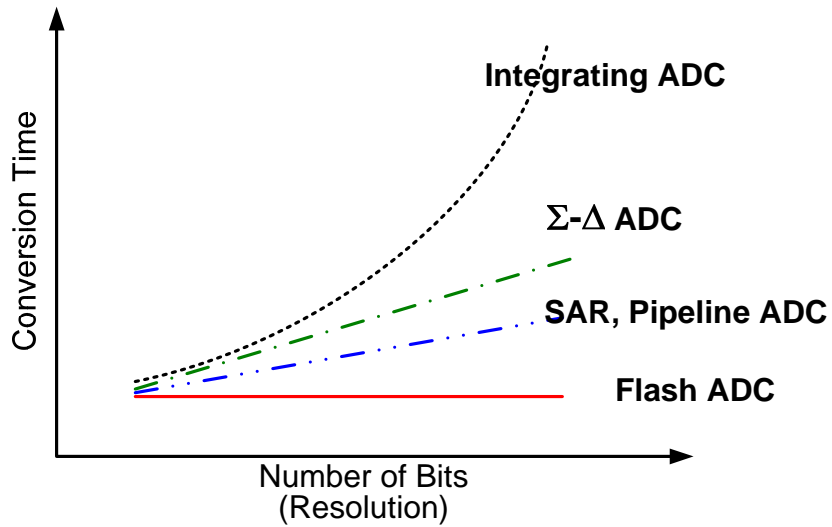
ADC architectures, applications, resolution, and sampling rates



S. Rapuano, and et al., "ADC parameters and characteristics," Instrumentation & Measurement Magazine, IEEE, vol. 8, no. 5, pp. 44-54, 2005



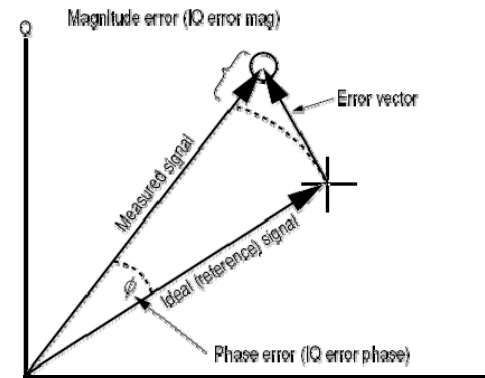
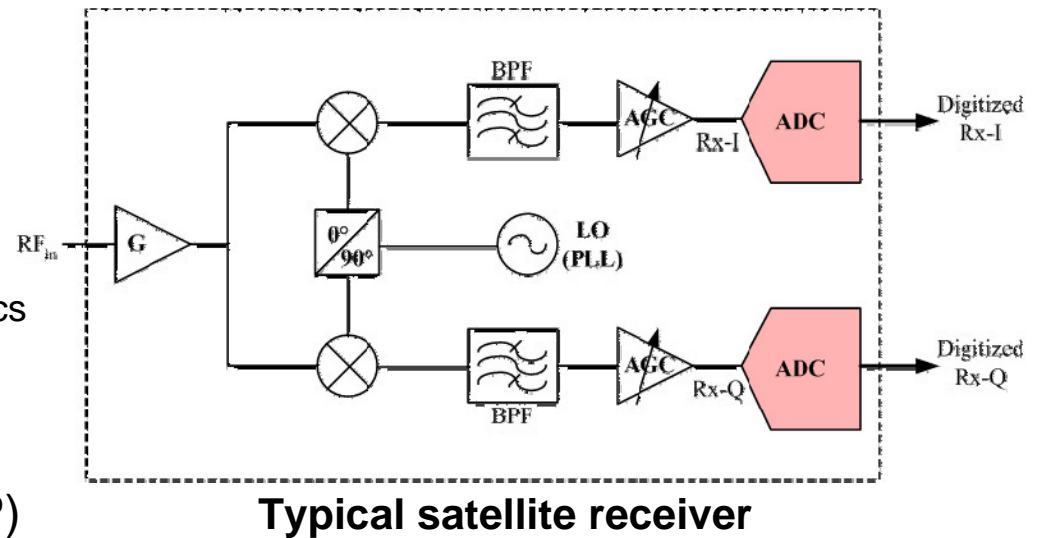
ADC Architectural Tradeoffs





ADCs for Modern Satellite Communications

- Challenges for the ADC verification testing at high speed
 - Mixed-signal IC test
 - Difficulty to apply traditional metrics to validate system-on-chip (SoC) solutions
 - Mixed-signal buffering interfaces
 - Digital signal processing (DSP) based testing
 - Design-for-test (DfT)
- Accurate sampling channel testing (for satellite tuner)
- High-speed ADC testing methodology for a modern satellite receiver
 - Static/**Dynamic** ADC testing
 - Test program
 - Verification test software (VTS) suite

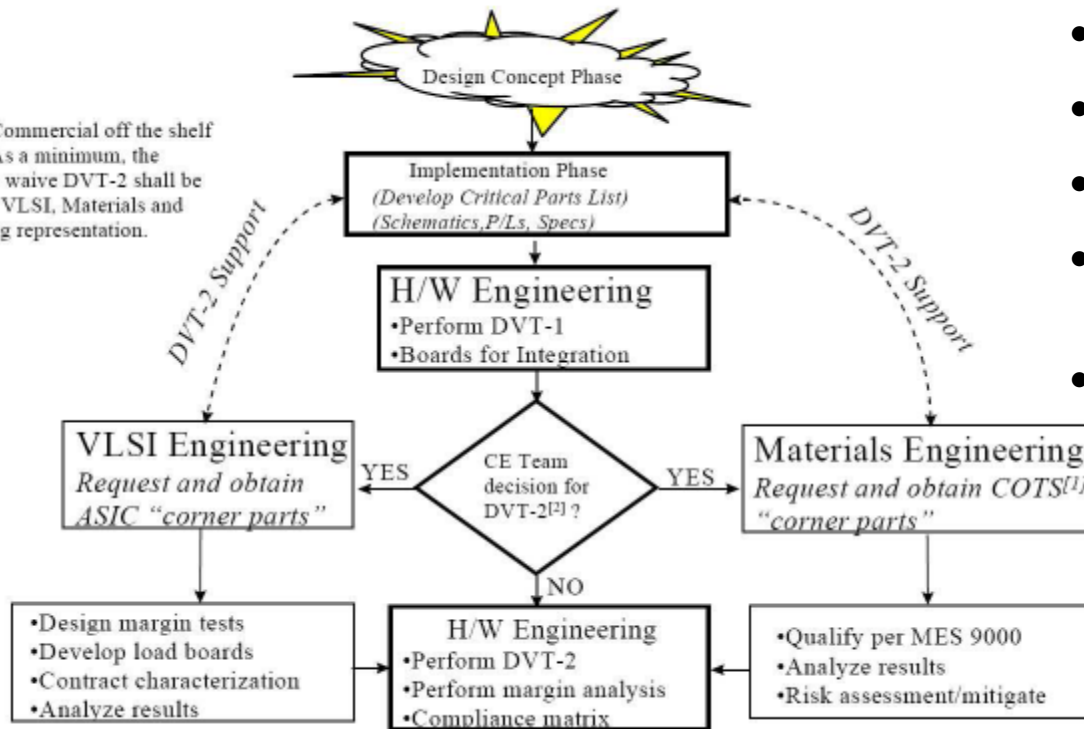


Error vector magnitude (EVM) and related quantities



Design Verification Process Outline

Note [1]: Commercial off the shelf
Note [2]: As a minimum, the decision to waive DVT-2 shall be made with VLSI, Materials and Engineering representation.

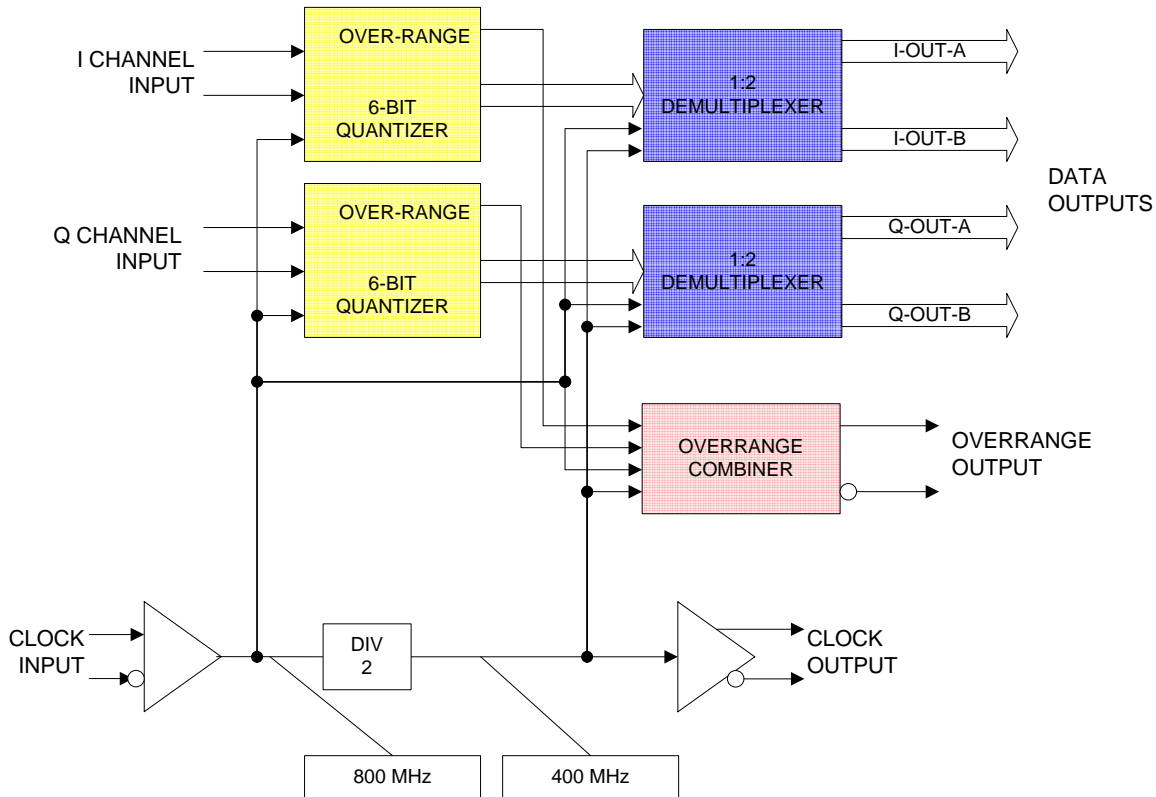


Capital expensive items:

- Test programs
- Test equipment
- Rack & stack
- Automated test equipment (ATE)
- Interfacing
 - ✓ Handlers
 - ✓ Load Board
 - ✓ Contactor Socket
 - ✓ Wafer probing
 - ✓ Packaging
- Calibration
- Accuracy, repeatability, and correlation
- Design-for-Test (DfT) and built-in-self-test (BIST)



High-speed ADC Characterization: New Results



	Conditions
Resolution	6-bit dual channel
Analog Input Range	800 mV _{pp}
Sampling	800 MSamples/ sec
Output Format	2's complementary Code
Output Condition	LVDS Output with R _{load} = 100 Ω
Output Data Rate	400 MHz
Supply	Digital 3 V Analog 5 V LVDS 5 V
Package	80-pin TQFN

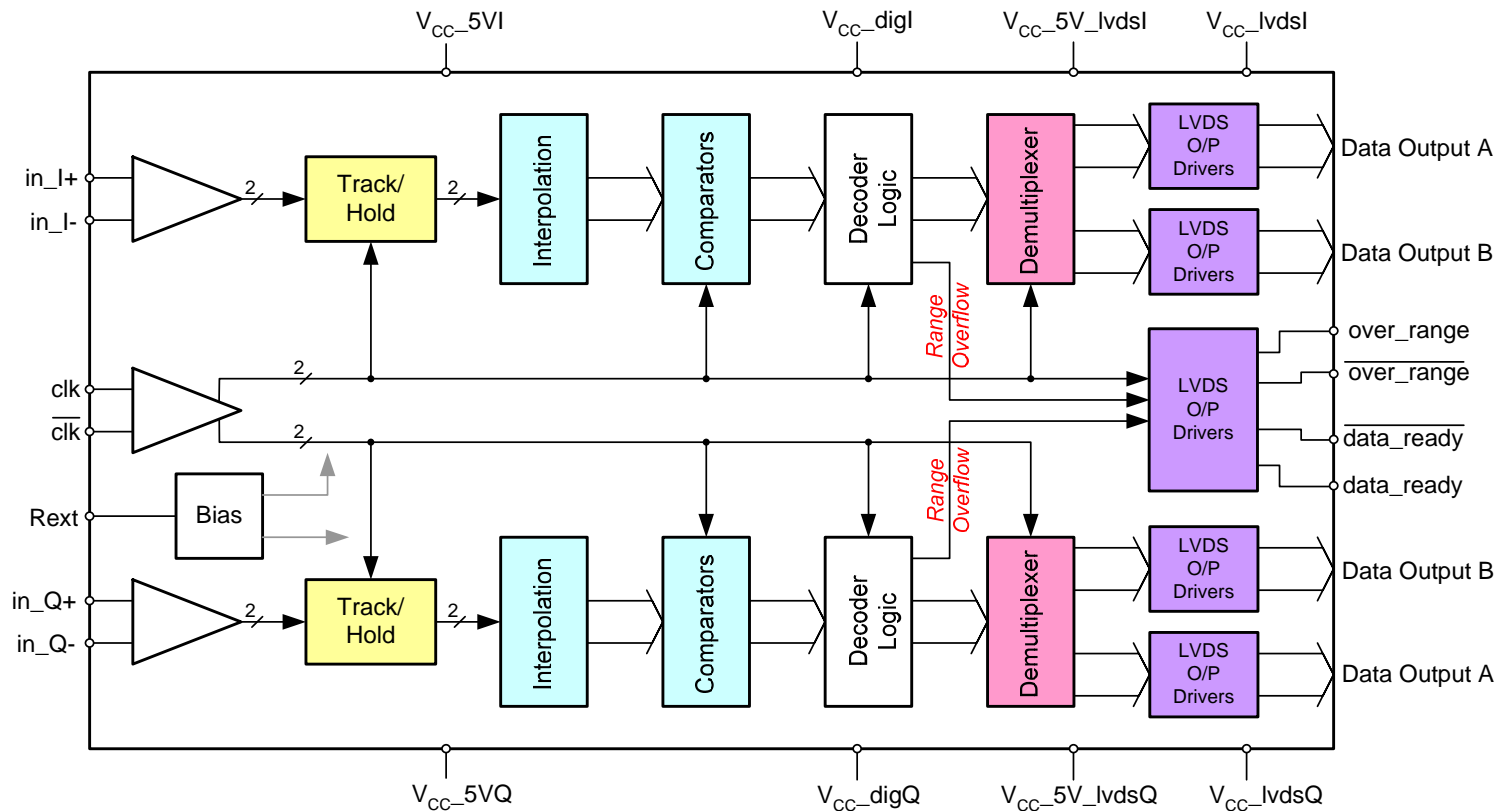
ADC top level function block

Hughes Network System (Germantown, MD)
 → THAMES ASIC project



High-speed ADC Architecture

- Flash type ADC for a speed (800 MS/s)
- Fabricated in Atmel's AT46000 BiCMOS technology
- Two identical 6-bit ADCs on a chip
 - Application to a modern satellite base-band receiver



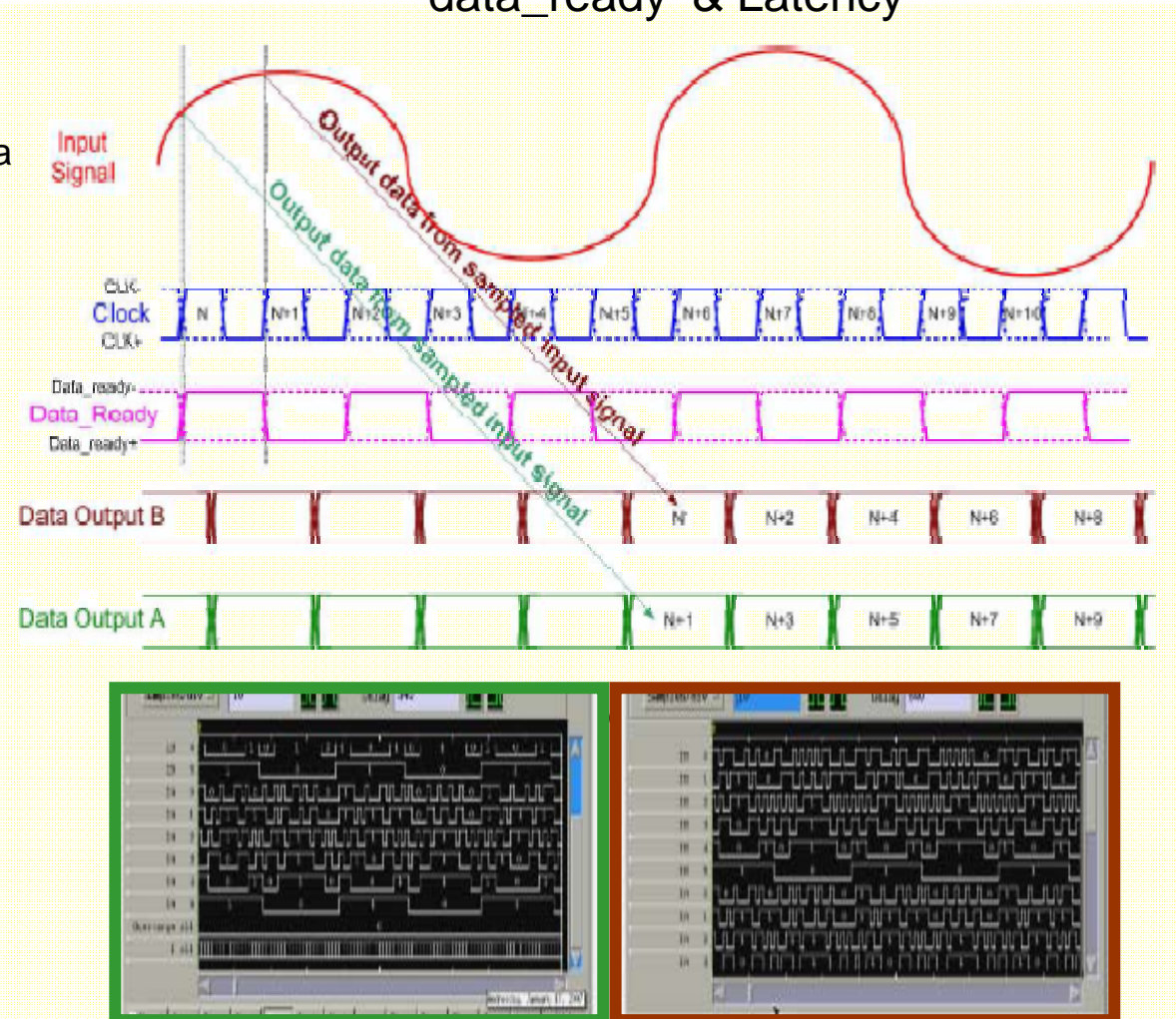
High Speed ADC Architecture – *Thames* (Designed by HNS)



Design-for-Test Philosophy

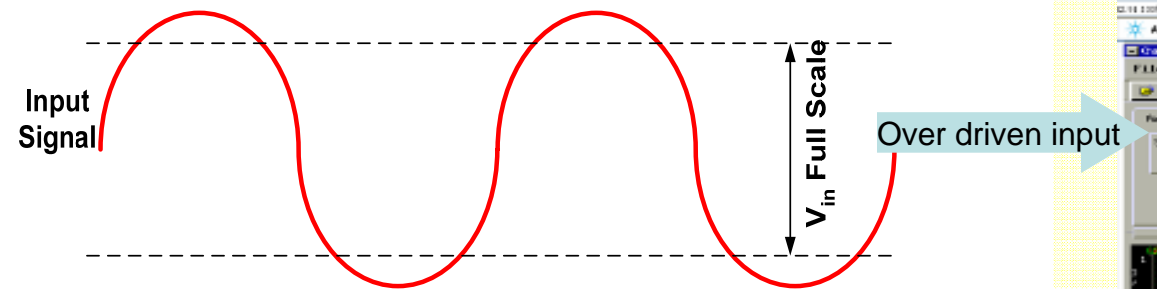
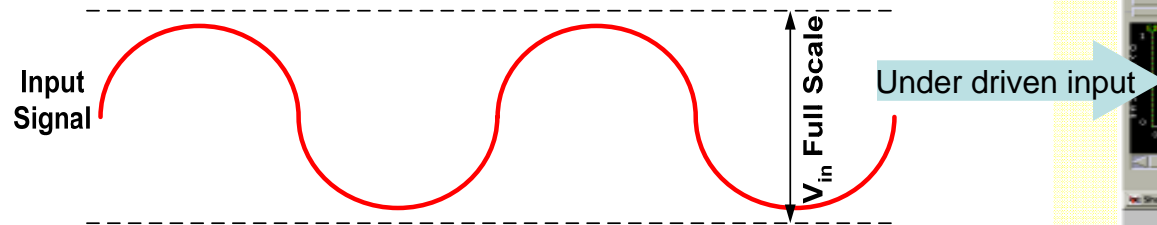
- Common input sampling clock
- Demultiplexed (6:12) digital output
 - ‘data_ready’ – lower speed data transfer
 - ‘over-range’ – over flow
- Two’s complement outputs compliant with IEEE LVDS Std.1596.3-1996
- Temperature sensing and control
- External bias setting resistor
- Separated voltage supply and ground pinouts for each analog, digital, buffer sections

‘data_ready’ & Latency

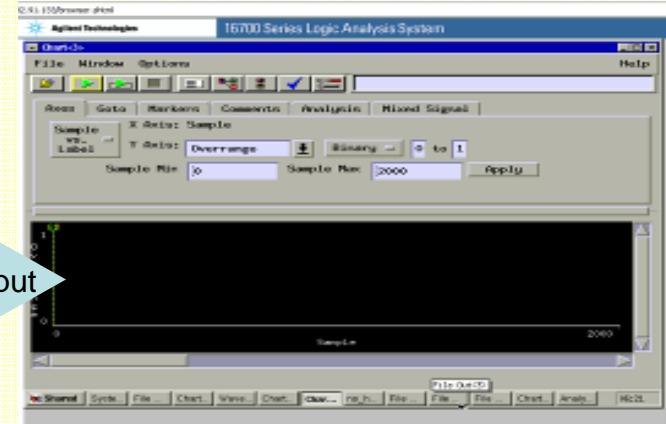




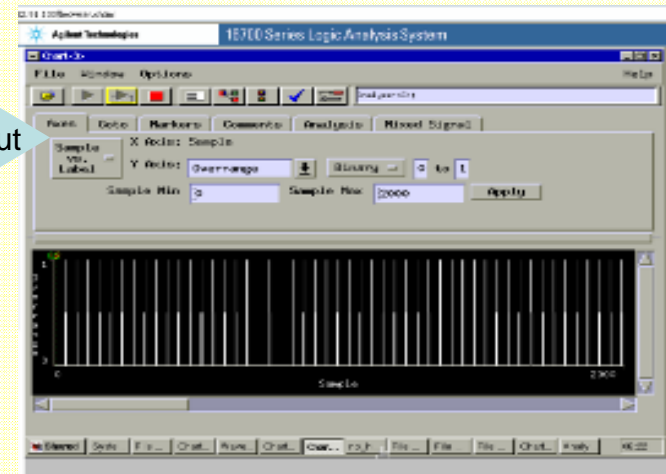
Design-for-Test Philosophy



'over_range' & input voltage



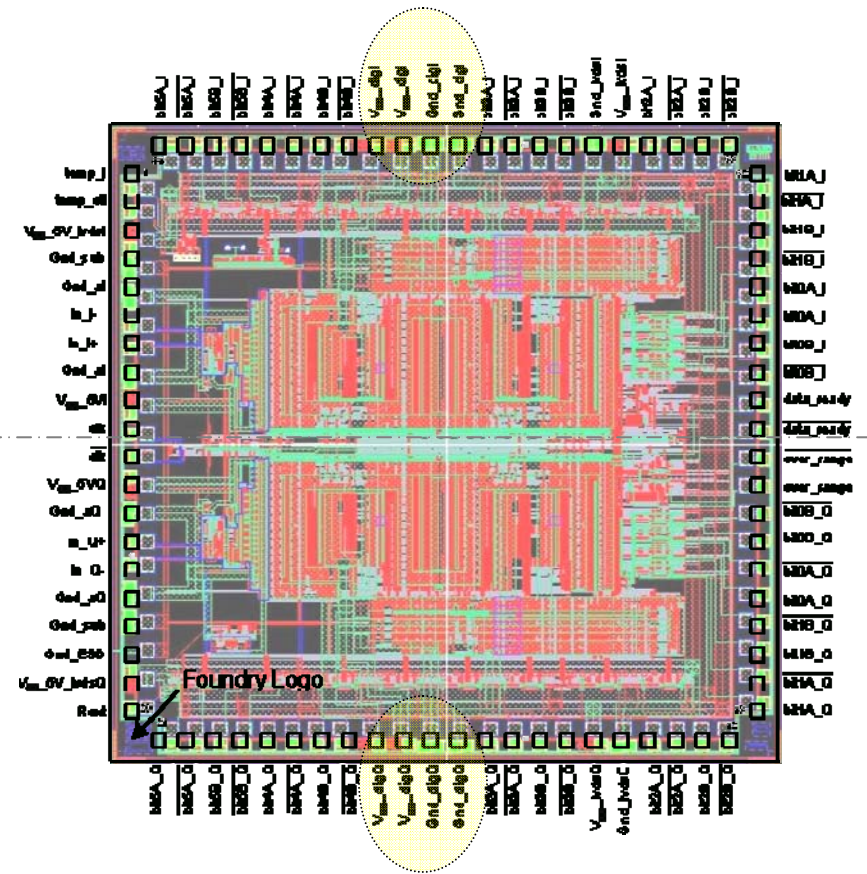
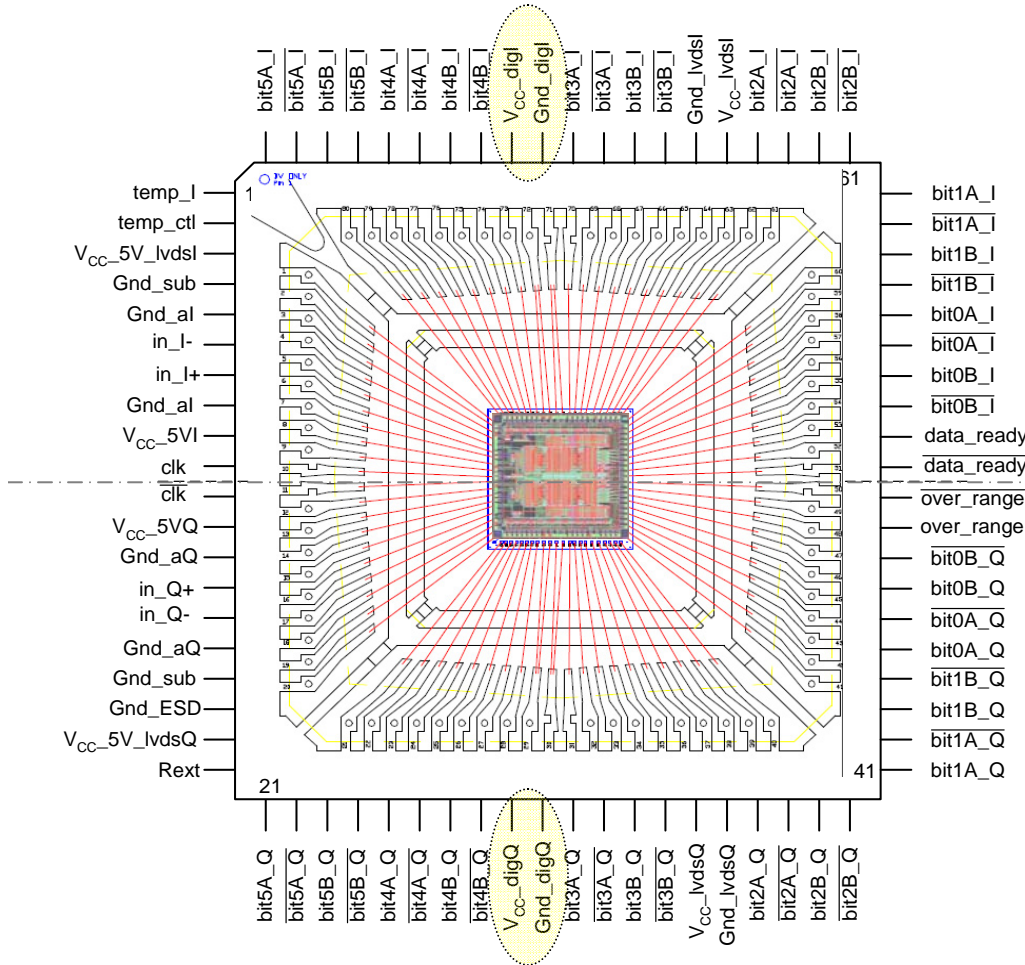
**'over_range':
monitoring ADC input fullscale**





Test Fixture - Packaging

Fabricated in Atmel's AT46000 BiCMOS technology



Packaging:

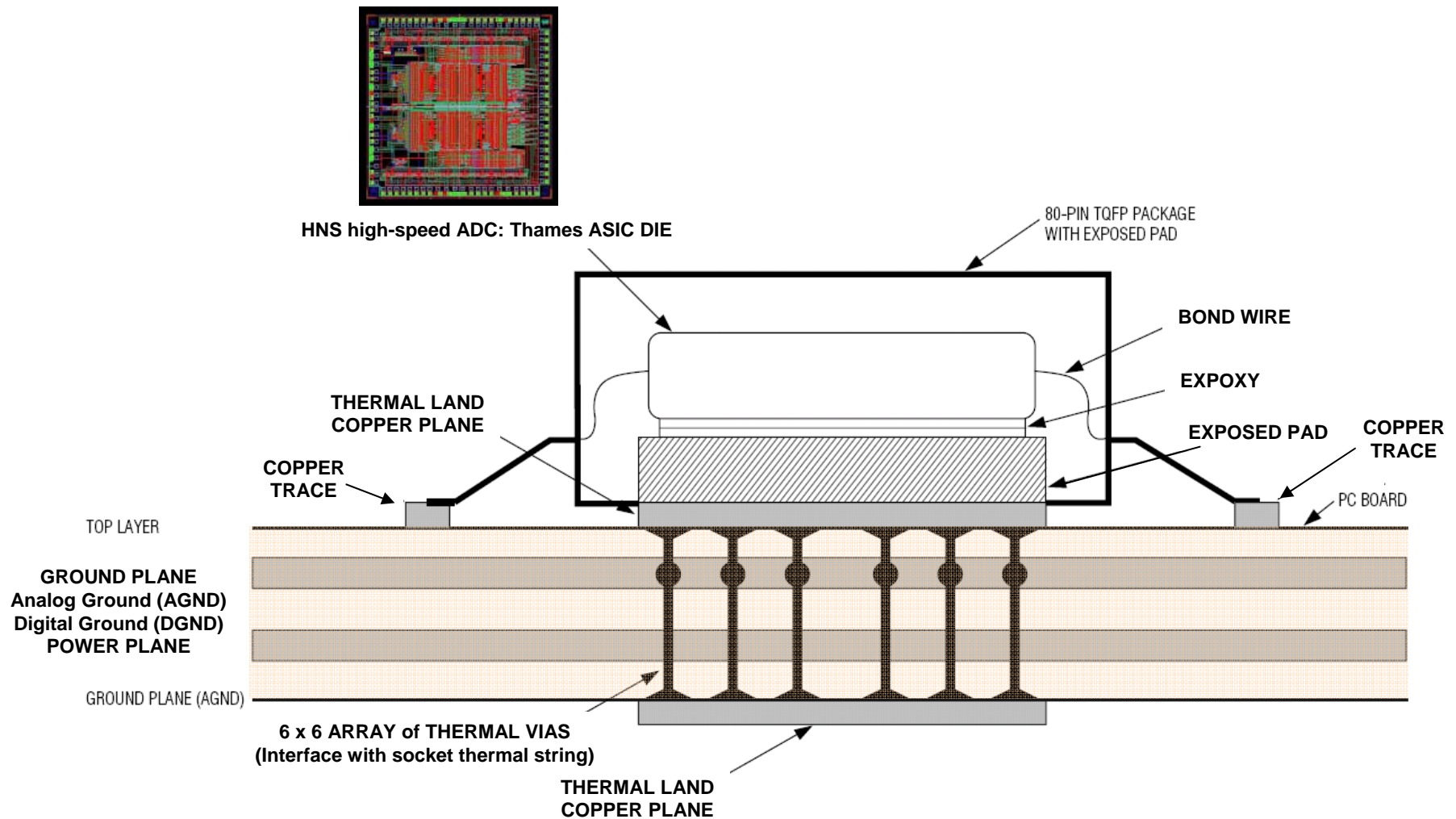
Thermally enhanced thin quad flat 80-pin package
(0.5 mm pitch, 12 X 12 mm² body)

Bare-die:

3.2 x 3.2 mm² 84 pin-pad

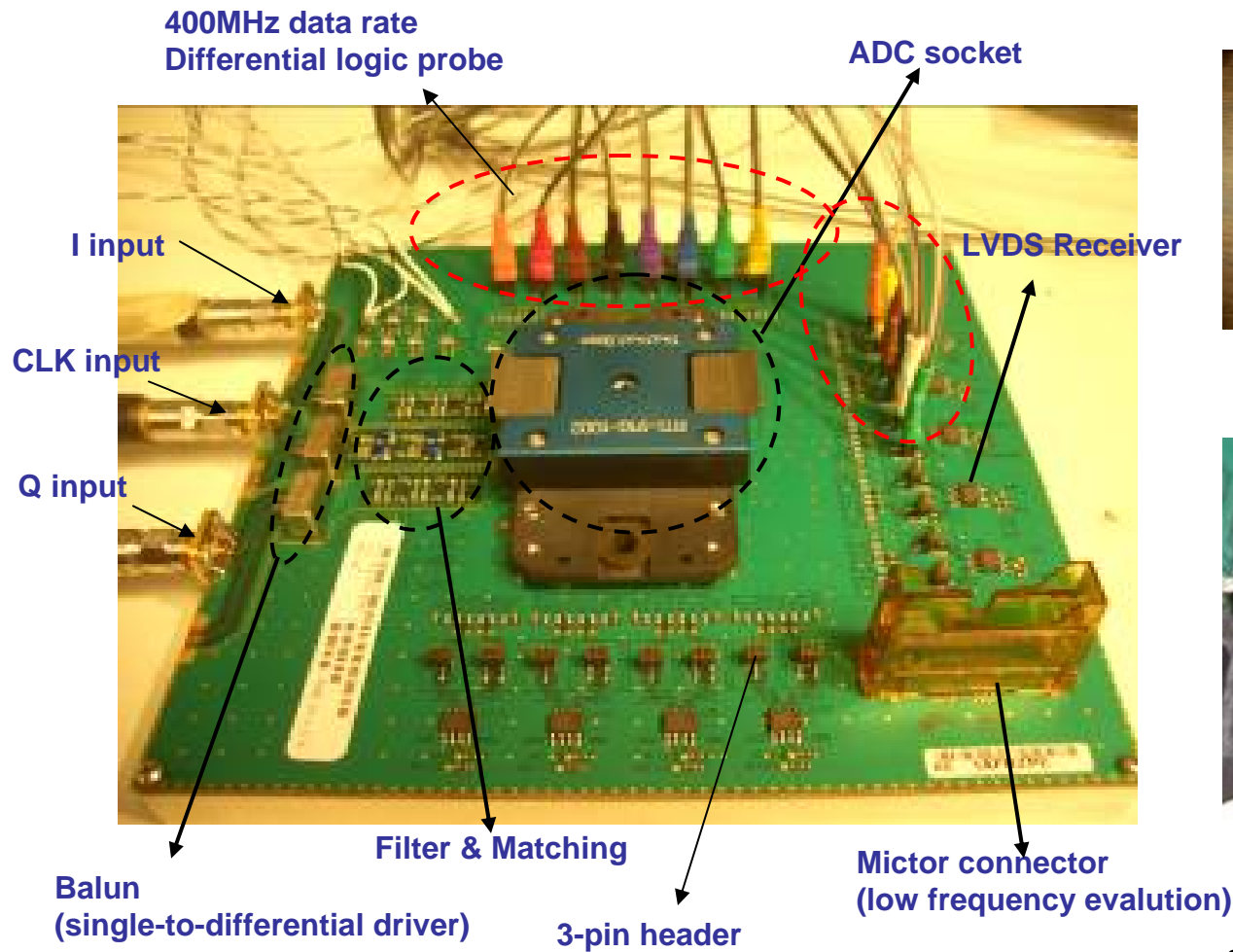


Test Fixture - Packaging Thermal Issue





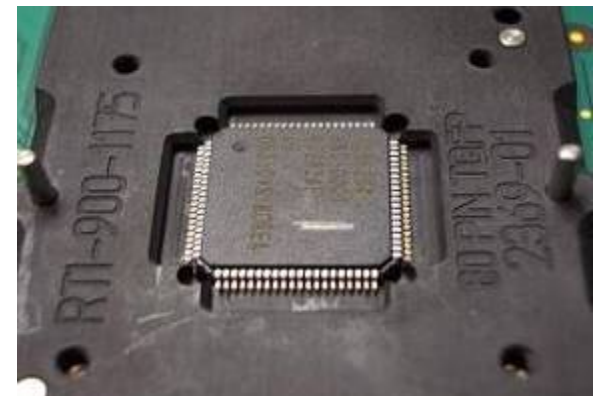
Test Fixture & Handler



HNS high speed ADC verification test fixture



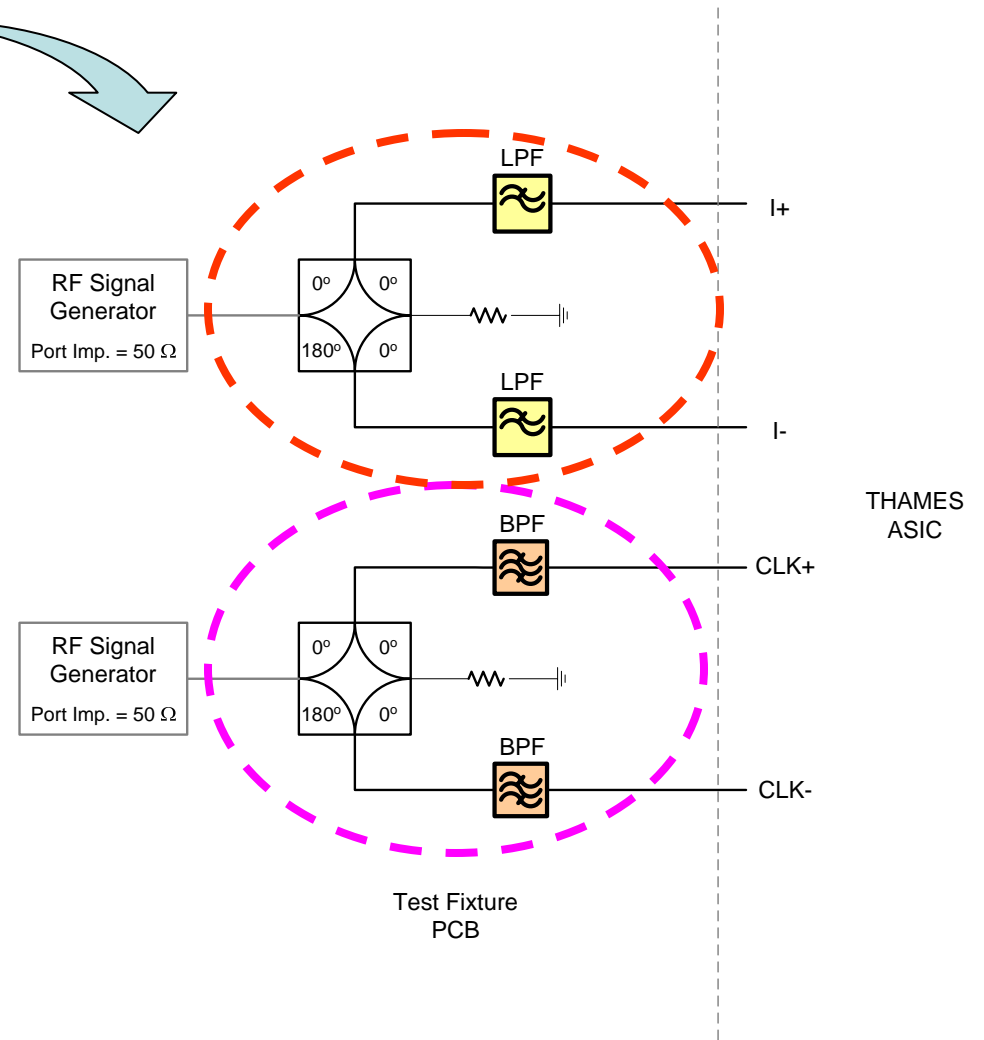
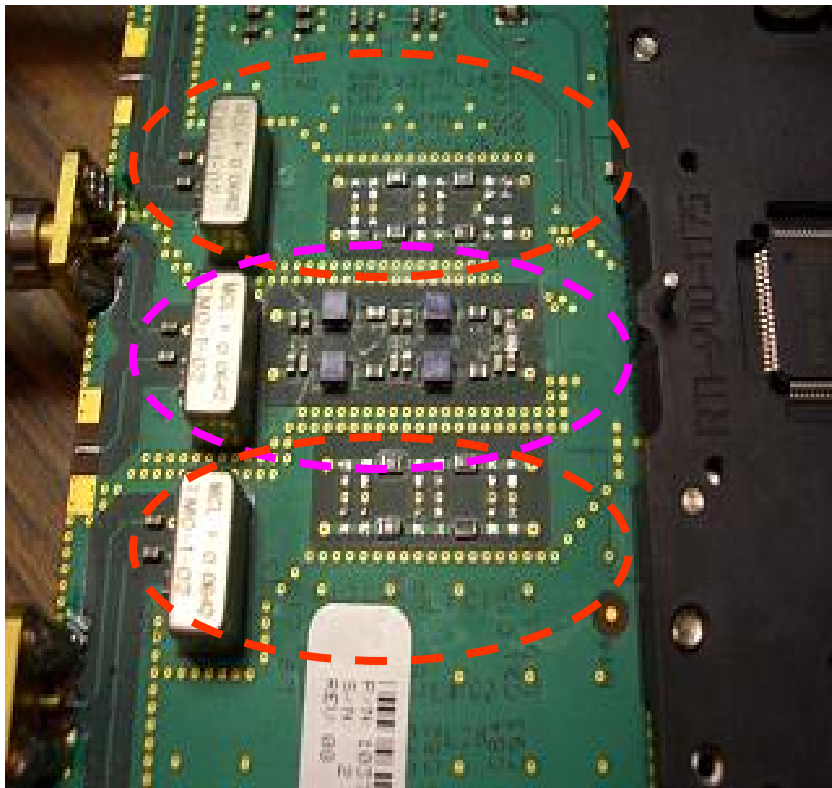
DUT handler



Loaded DUT on the socket
without latch cover

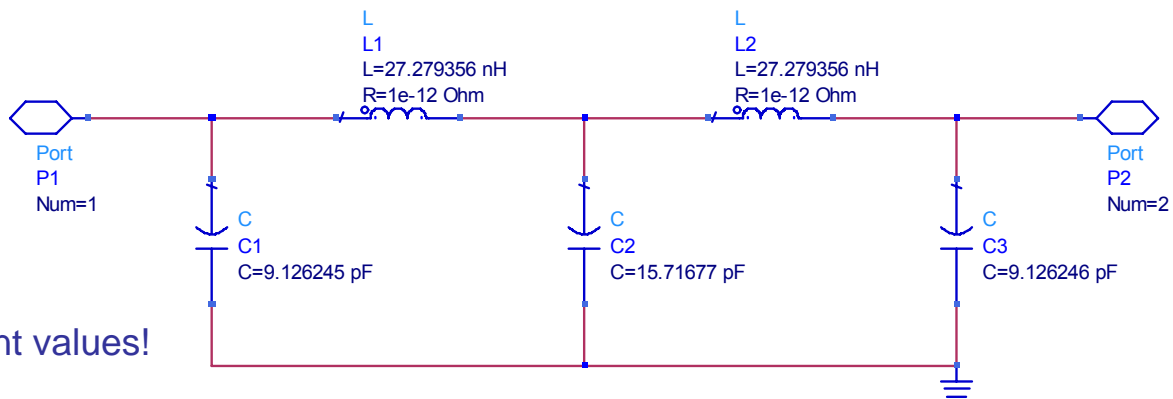
Spring loaded 80-pin pogo pin Socket

RF Input to "Thames"



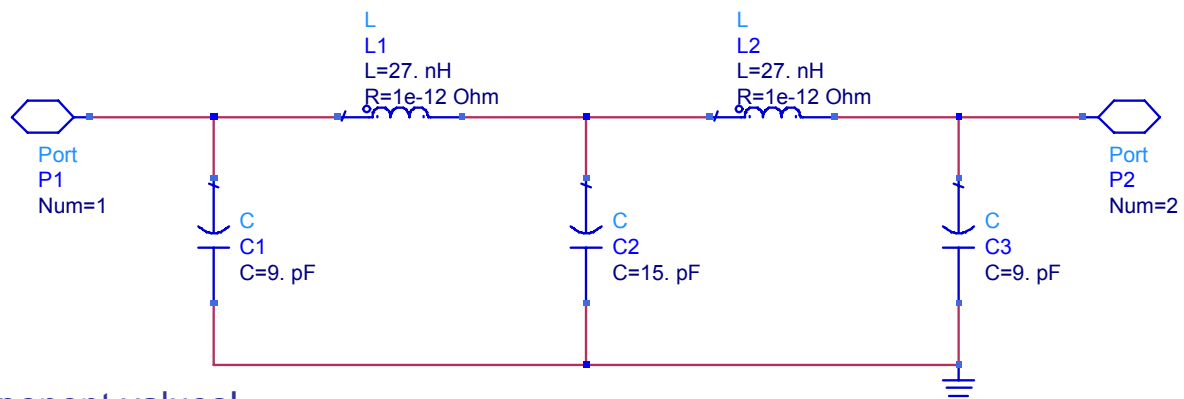


I/Q channel LPF



Ideal component values!

Ideal design

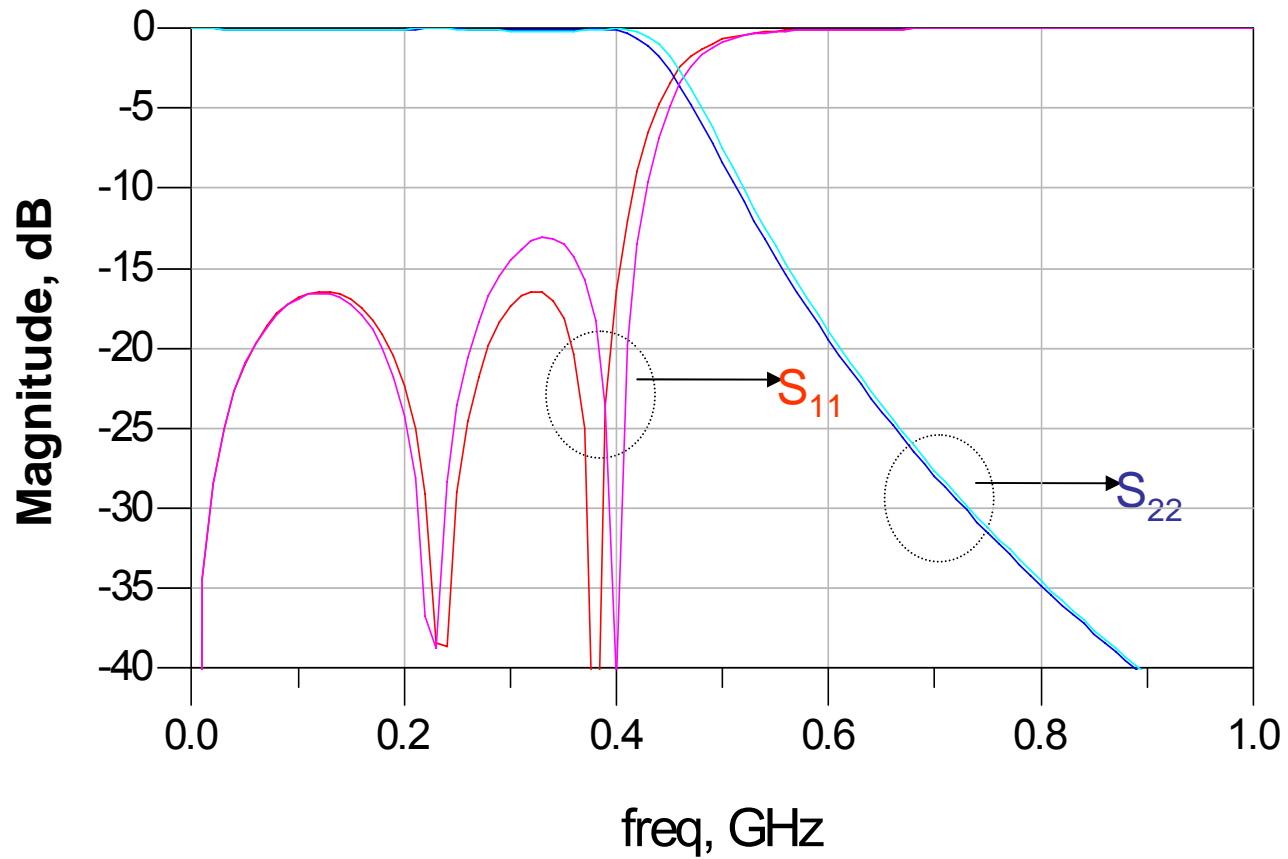


Available component values!

Practical design

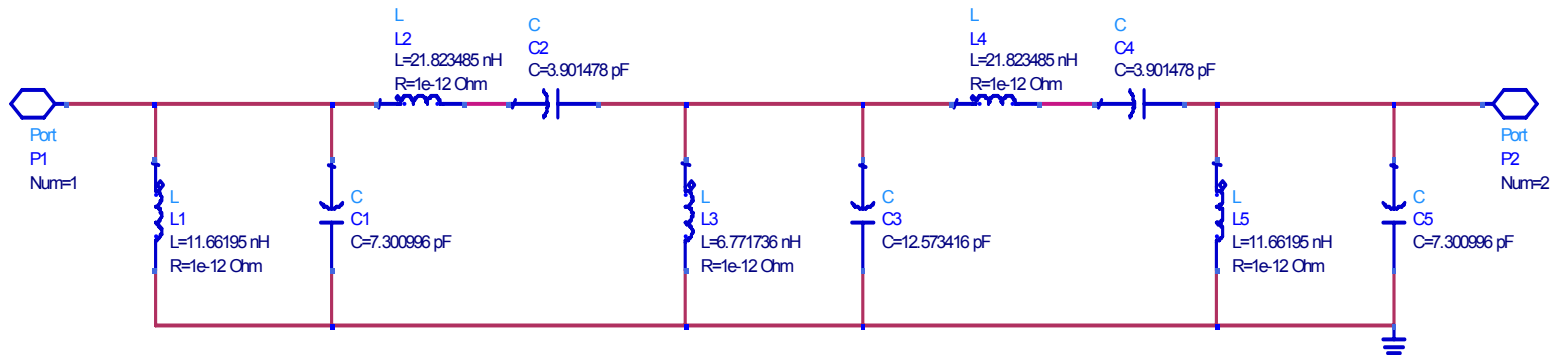


I & Q Channel LPF Characteristics



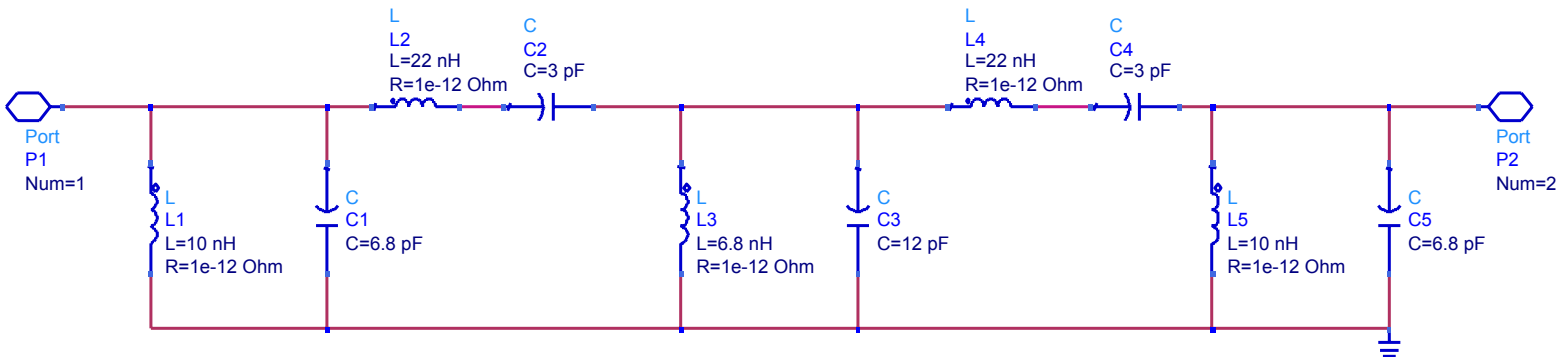


CLK BPF



Ideal component values!

Ideal design

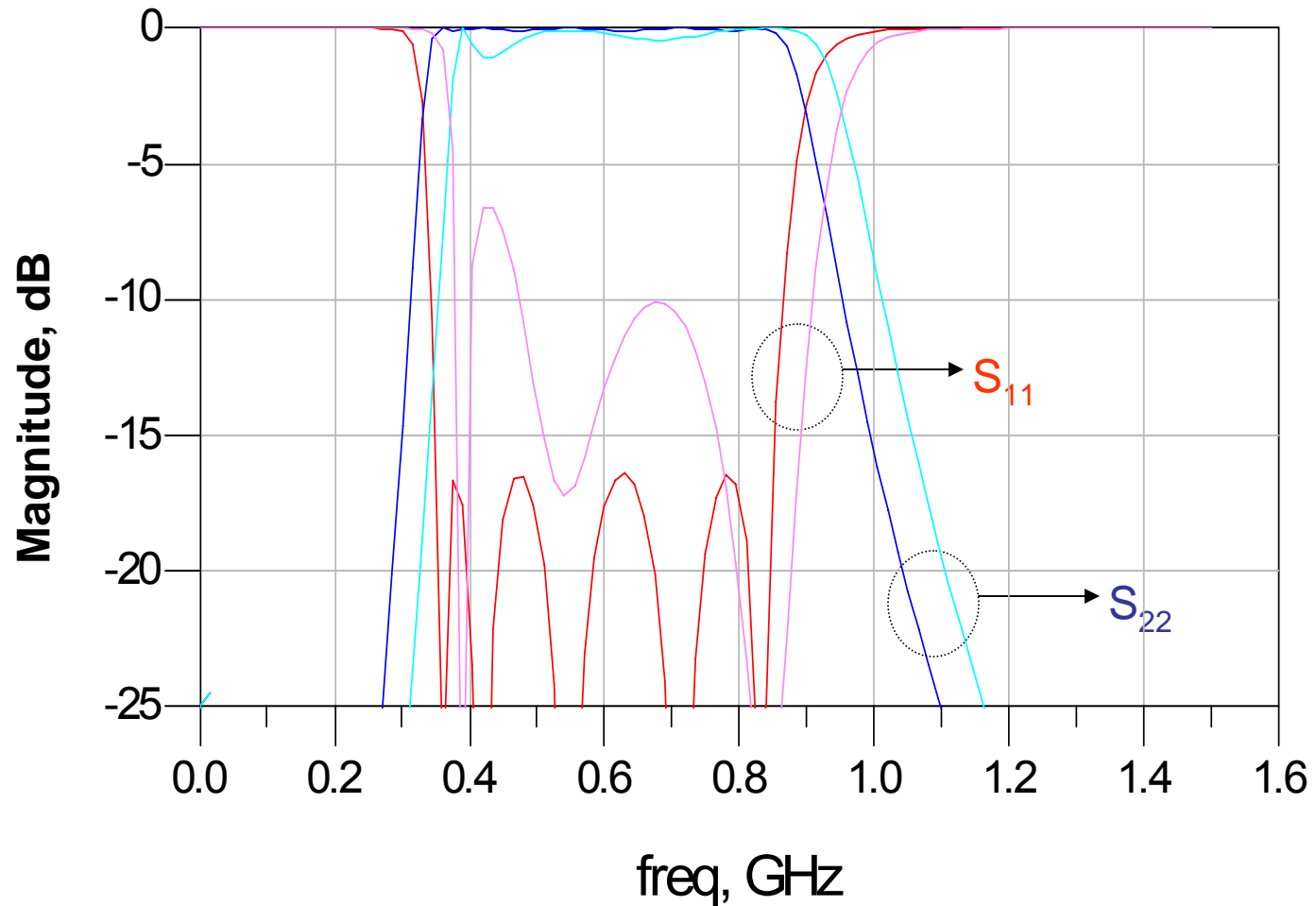


Available component values!

Practical design

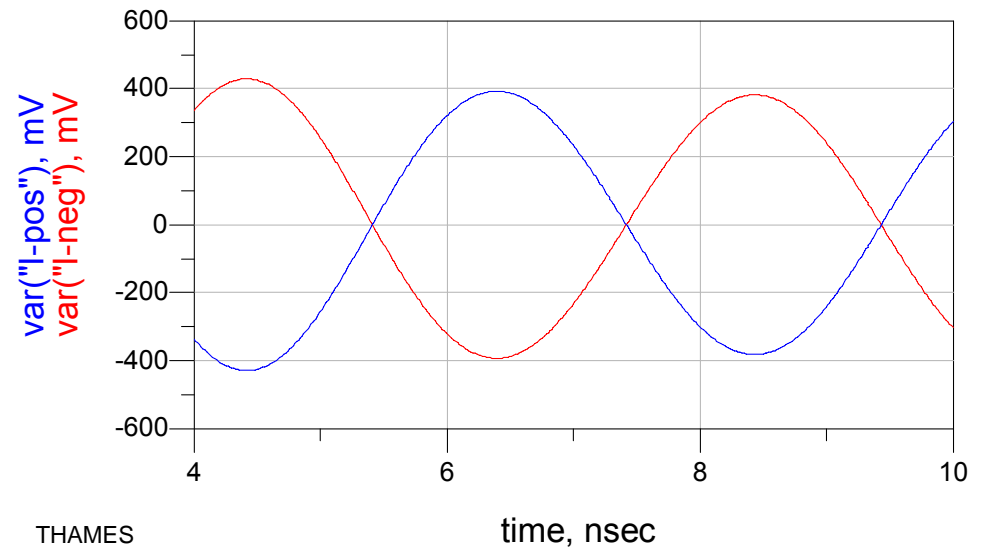
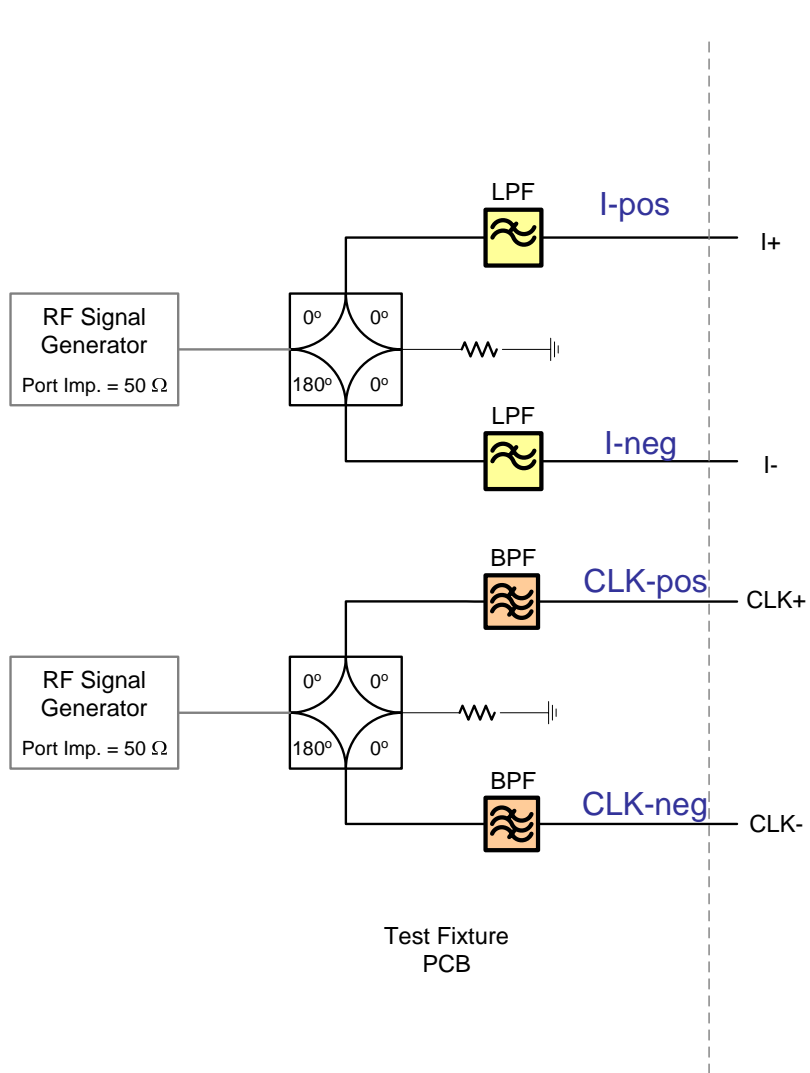


CLK BPF Characteristics

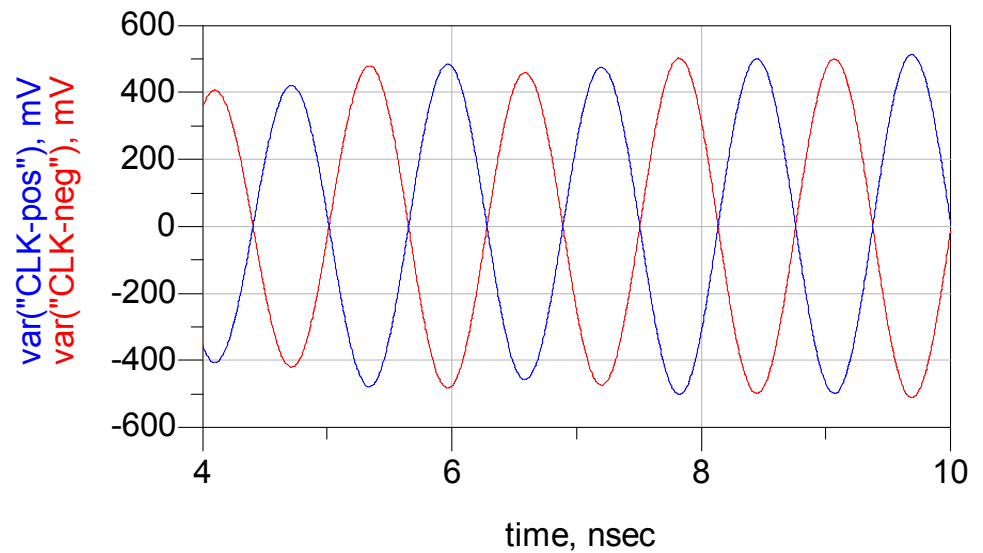




Time-domain Characteristics

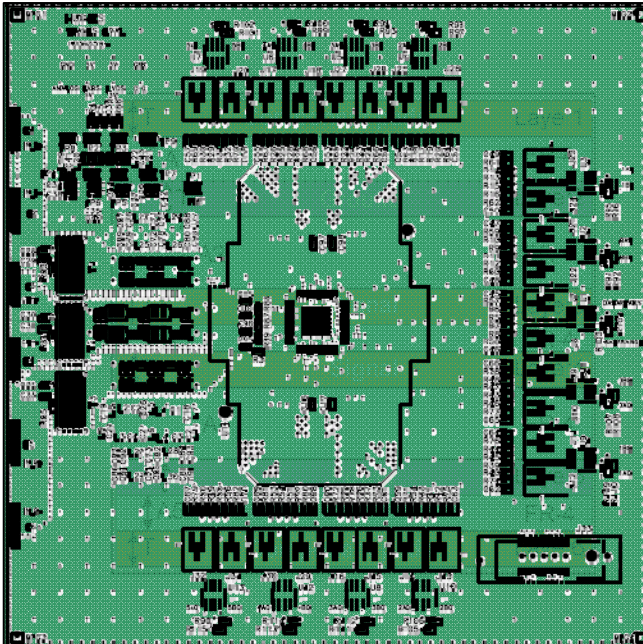


THAMES
ASIC





Test Fixture - Device Interface board (DIB)

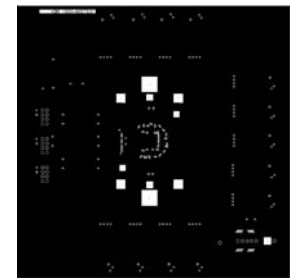
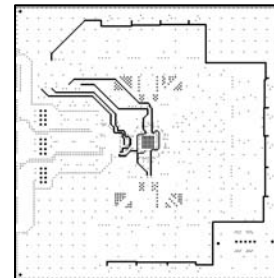
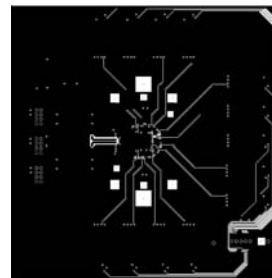
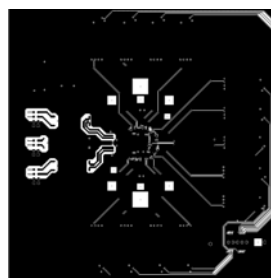
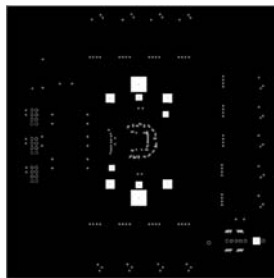
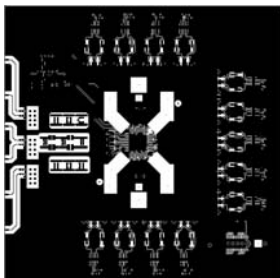


Total DIB (PCB) thickness: ~ 64.4 mil
PCB material : FR-4 → 6 layer PCB
($64.4 \times 25.4 / 1000 \approx 1.64$ mm)

Routing high speed digital signal traces away from the sensitive analog traces, clock, and reference lines → Minimize undesirable crosstalk

Optimizing routes for the clock and analog input → Minimize unwanted signal skew and phase mismatch

Keep symmetrically disposing the differential-analog-input subsystems → Balancing all parasitics





Test Rack (Test Bench)

Spectrum Analyzer

Digital Logic Analyzer

Temperature Chamber

Power Supply

Test Fixture

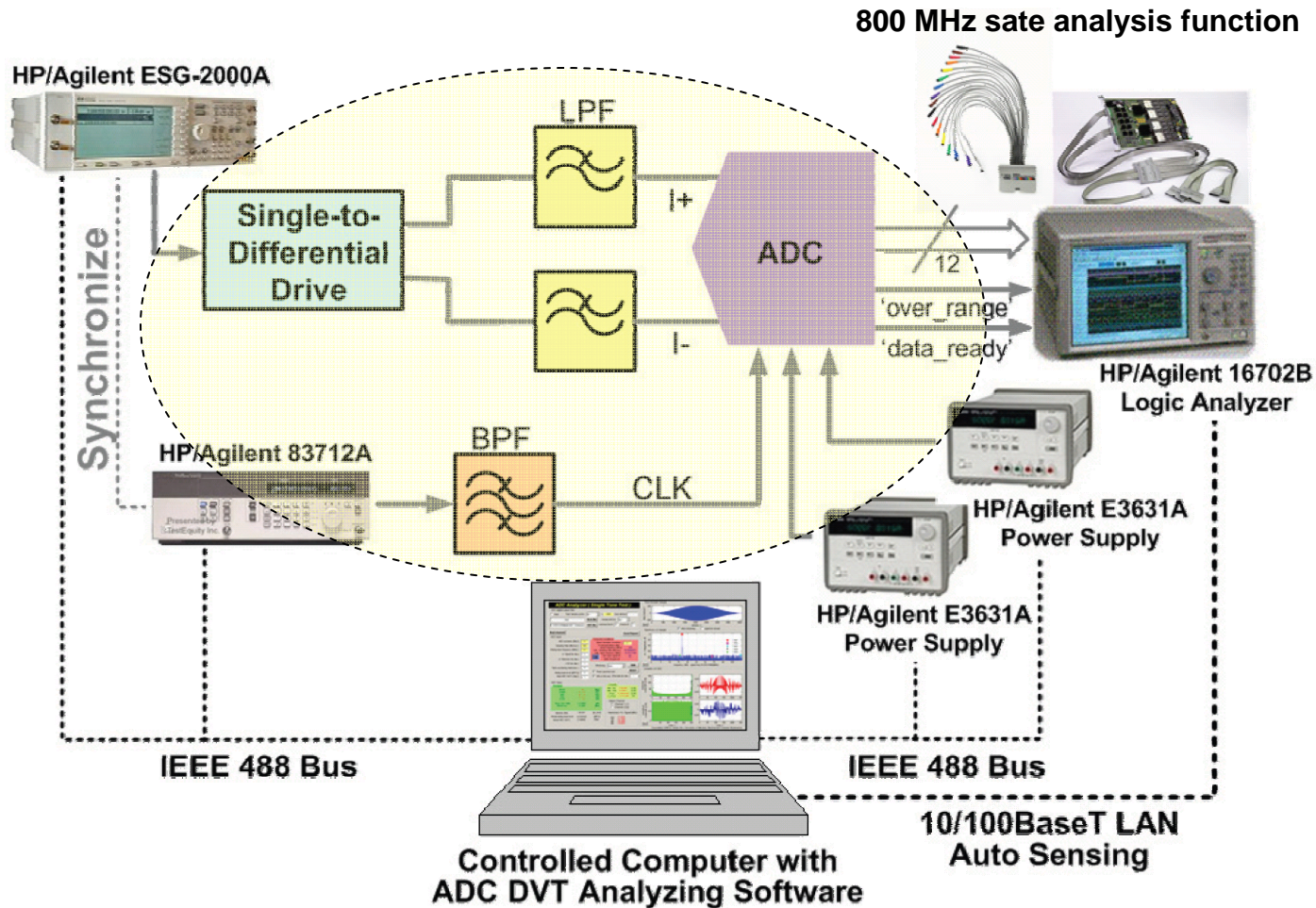
Host Computer

Digital Mutli-meter



RF Balun

DVT Configuration



Configuration for the HNS high speed ADC verification tests

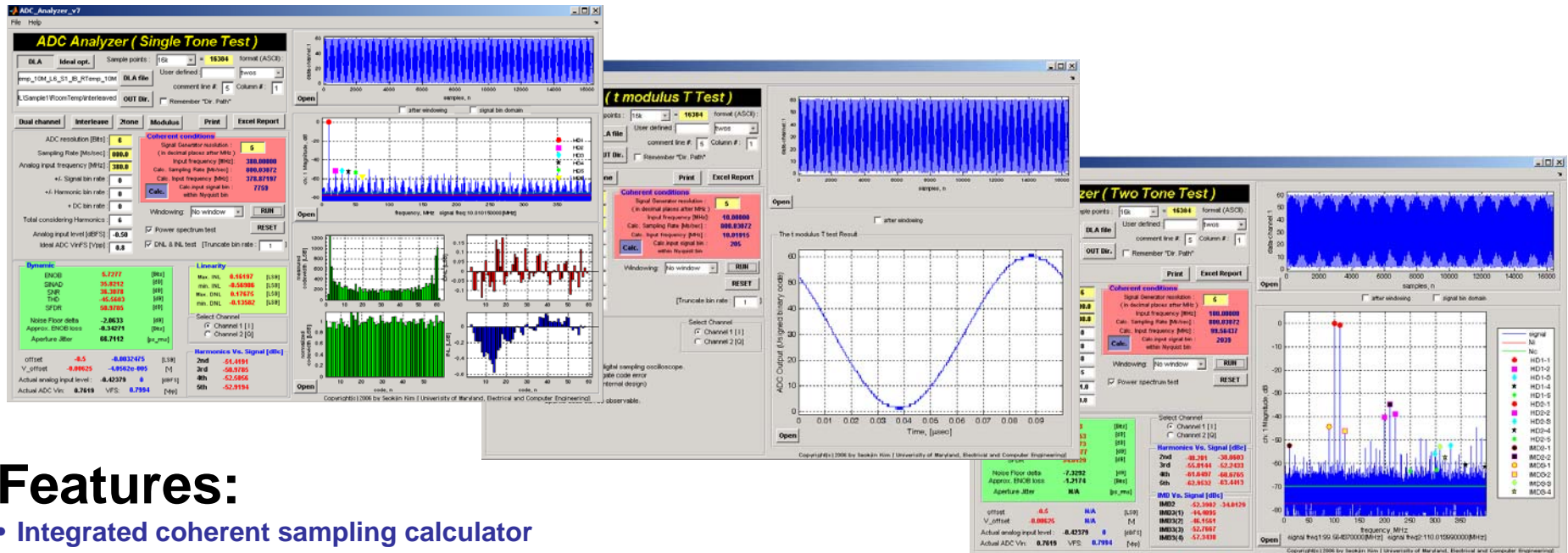


High Speed ADC DVT Methodology

- Test program: ADC verification software suite (VTS)
 - Single-tone ADC tester
 - Two-tone ADC tester
 - Fast Fourier transform based
 - Auto test equipment (ATE)
 - Post processing parameter extraction → performance analysis
- Static/**Dynamic** ADC test
 - Static
 - Ramp-based method to determine the ADC output transition levels
 - Time consuming
 - Can not verify a real ADC performance for modern satellite receiver application.
 - **Dynamic**
 - Critical ADC parameters for the receiver
 - Only obtained by under dynamic drive conditions
 - Fast Fourier transform module as a foundation of dynamic ADC testing
- High quality, high volume, low-cost production test applications for a modern satellite receiver



Verification Test Software (VTS) Suite



Features:

- Integrated coherent sampling calculator
- Integrated ideal ADC simulator
- Integrated windowing function for the input signal
- Fast ADC function parameter extractions
 - **ADC Dynamic Performance**

Signal-to-Noise Ratio (SNR)
 Signal-to-noise and distortion ratio (SINAD)
 Effective number of bit (ENOB)
 Spurious free dynamic range (SFDR)
 Total harmonic distortions (THD)
 Code-width and offset

- Differential nonlinearity (DNL)
- Integral nonlinearity (INL)

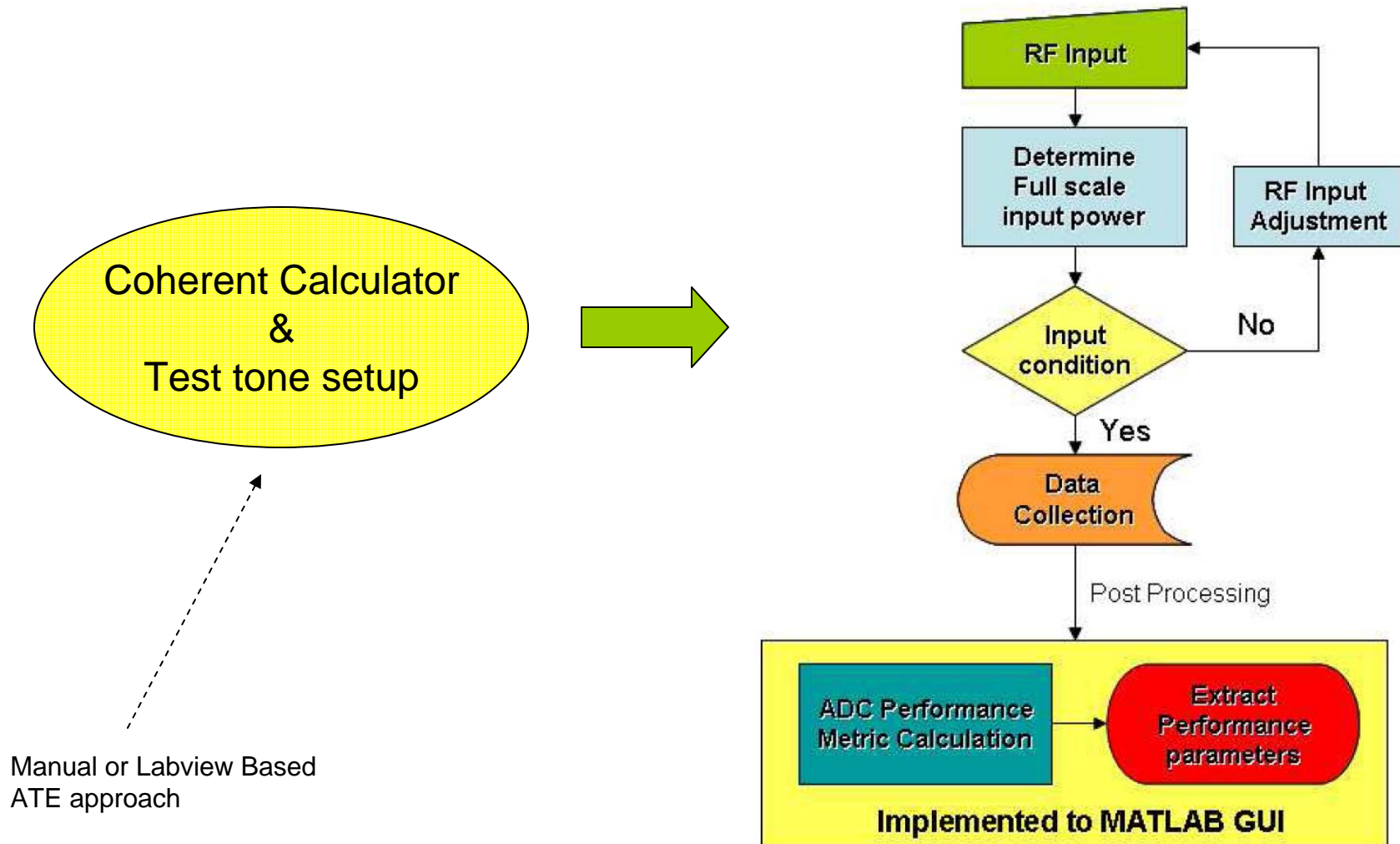
 Inter-modulation distortion (IMD) & 3rd order Intercept point (IP3) and two-tone SFDR

Uniqueness:

- Full input channel sampling diagnosis
 - Handling ADC input signal frequency leakages
 - VTS can be extended to characterizing the full input channel sampling.
- **Sampling signal windowing function & Leakage handling**
 - Hanning, Hamming, Blackman, Kaiser and etc.
 - Adding cost effective ATE setup for input signal generator for higher resolution ADCs (> 8bits)
- **Matlab GUI for easy program access and handling**
 - Advanced mixed-signal testing features are mostly integrated to this VTS suite so that any of test engineer can run the testing and verification.

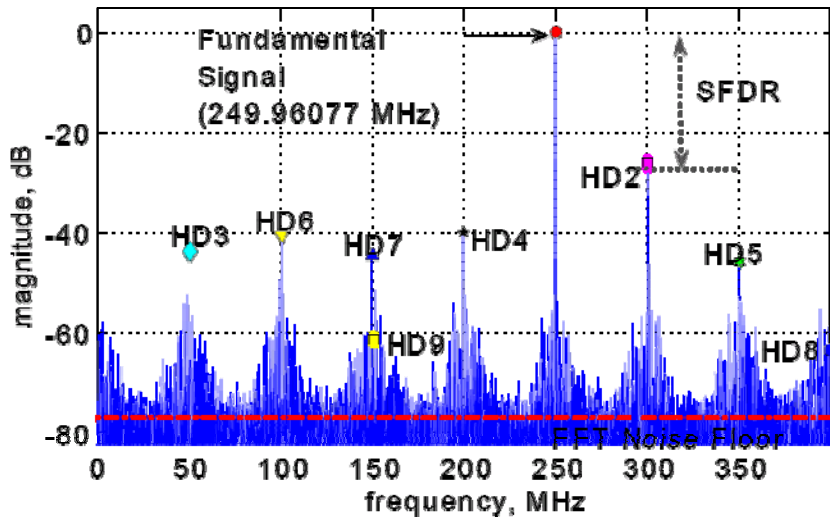
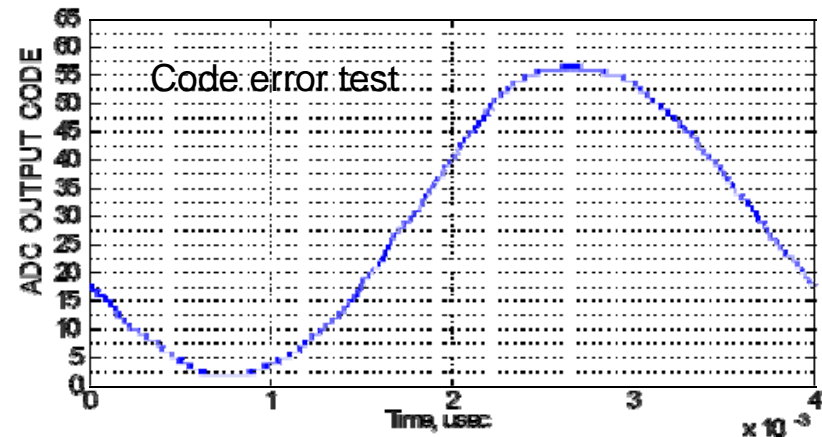
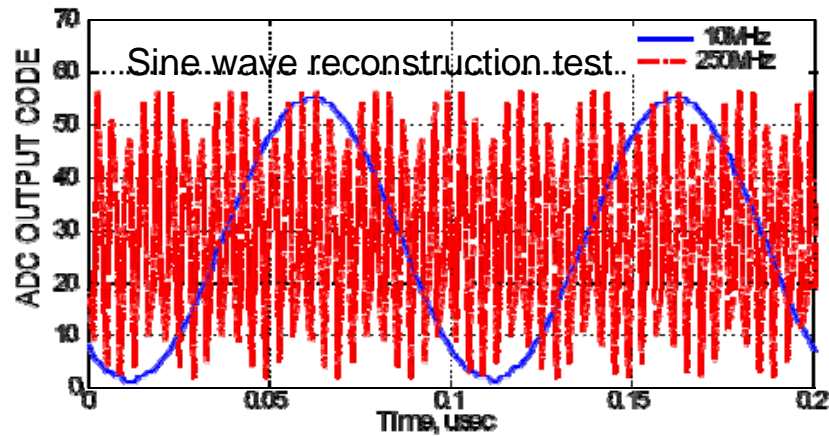


How VTS Suite Works?

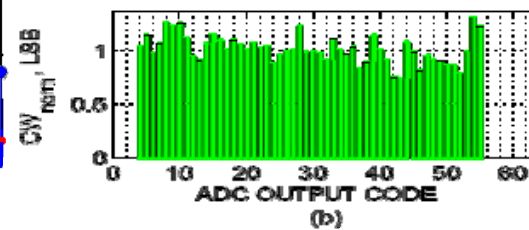
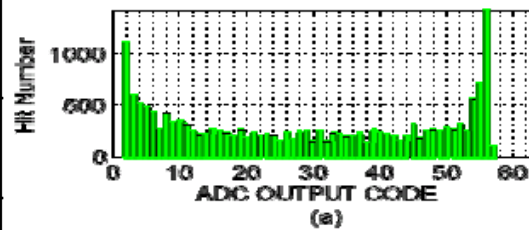




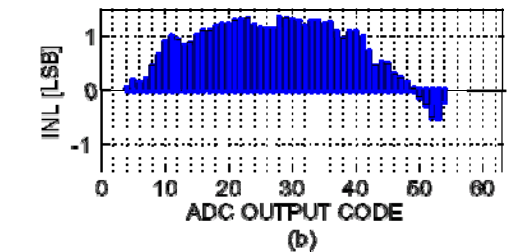
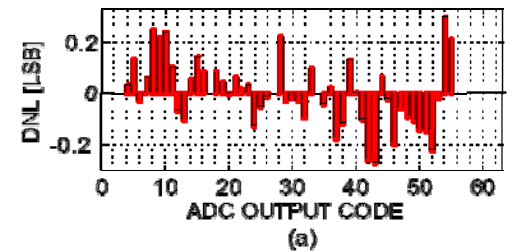
ADC DVT with a Single-tone



Power spectrum test



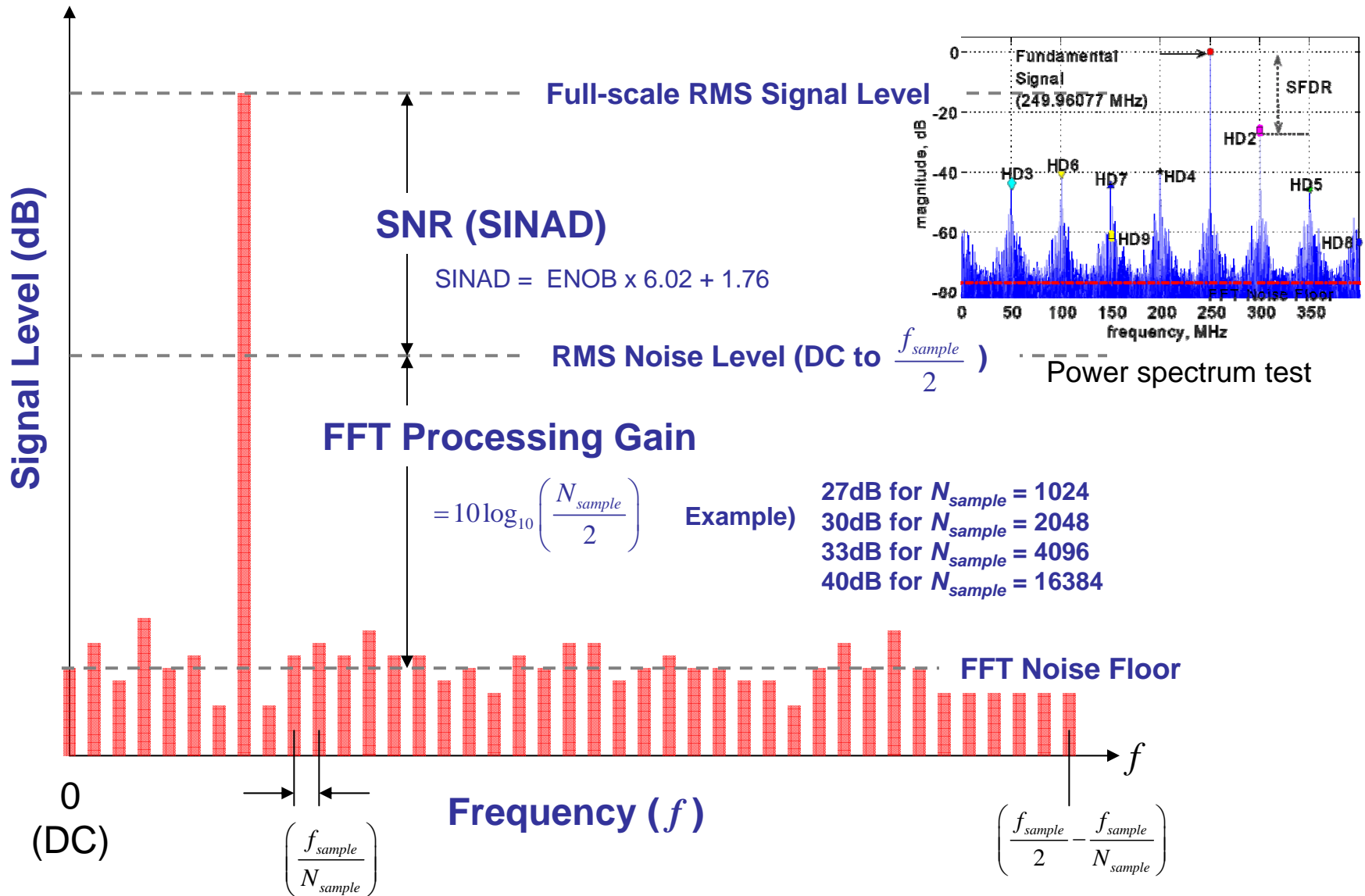
Code density test



Linearity test



Fast Fourier Transform – Mixed-signal Test





VTS data capture & FFT Enhancement

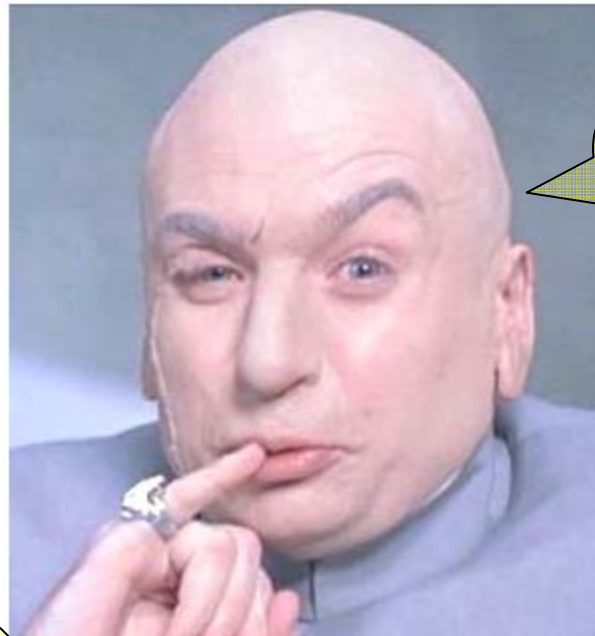
- Conventional Mixed-signal FFT
 - Capture node voltage
 - Convert to dBV unit after carefully consider measuring V_{RMS}
- Drawback:
 - V_{RMS} is may not easy to monitor under the load impedance is unknown.
- Thesis approach
 - Just capture quantized samples
 - Directly, process the quantized decimated signal (no-voltage conversion)
 - No-additional binary digitized signal to V_{RMS} Conversion
 - Normalized to input signal after FFT
 - Calculate all dynamic parameters



Spectral Leakage and Harmonics

Ideal sine wave

- No leakage !!
- No Harmonics !!



Mini-me, Corrupt
Test tones and fixture!

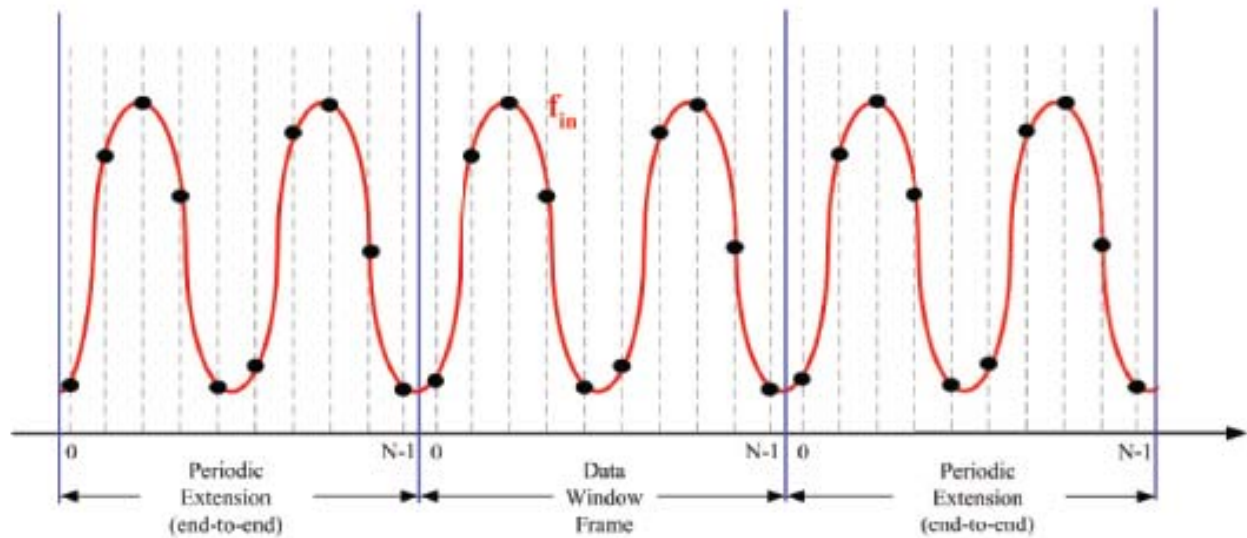


I will do a windowing!
Groovy, Baby!





Coherent Sampling and FFT

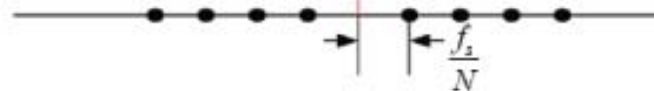


$$\frac{f_{in}}{f_s} = \frac{M}{N}$$



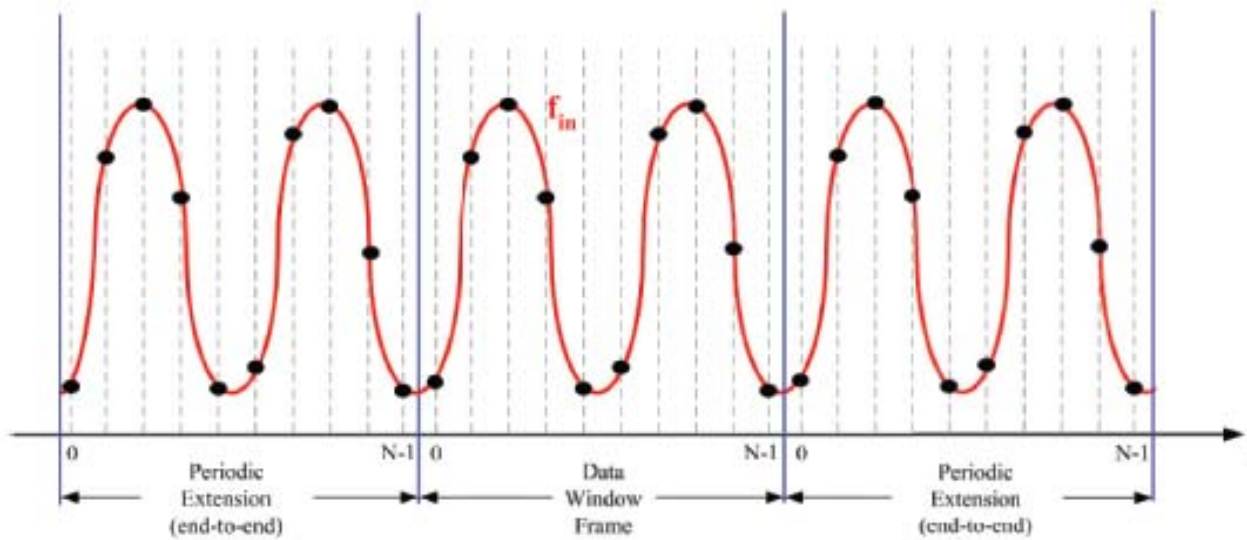
f_{in}

$N =$ Record Length
 $M =$ Number of Cycles
in Data Window Frame





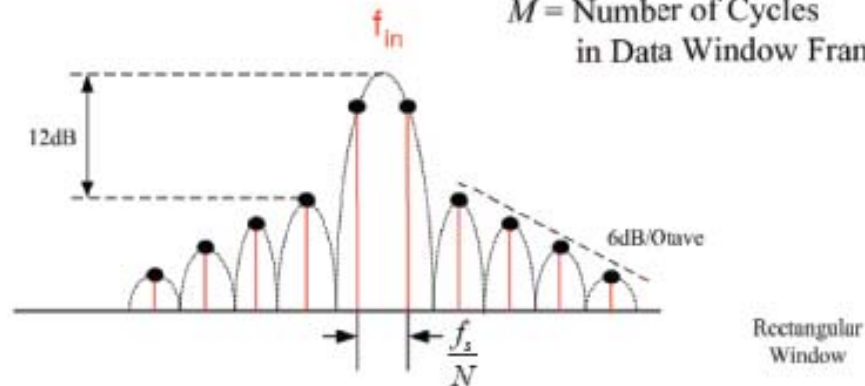
Non-coherent Sampling and FFT



$$\frac{f_{in}}{f_s} \neq \frac{M}{N}$$

FFT

N = Record Length
 M = Number of Cycles in Data Window Frame





Handle Leakages by Windowing

Window Function	3dB BW (Bms)	6dB BW (Bms)	Highest sidelobe (dB)	Sidelobe rolloff (db/Octave)
Rectangle	0.89	1.21	-12	0
Hamming	1.39	1.81	-43	0
Blackman	1.68	2.35	-58	18
Hanning	1.44	2.09	-32	18
Minimum 4-term Blackman-Harris	1.99	2.72	-92	0

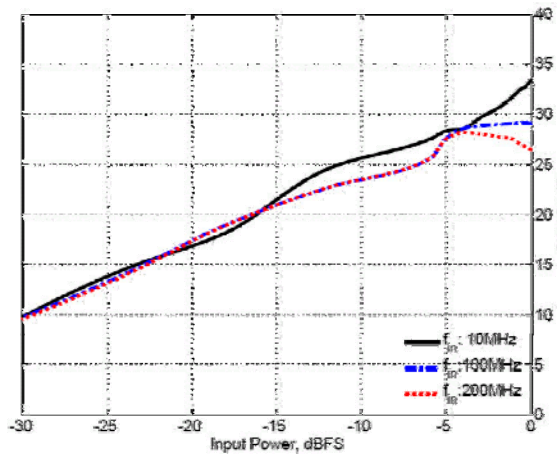
- Strong interfering frequency component from the test tone
→ Blackman or Hanning
- Strong interfering frequency component closed to the test tone
→ Blackman
- Interest frequency band contains 2 or more signals close to each other
 - Increase spectral resolution
 - Narrow main lobe → Rectangular or Hamming



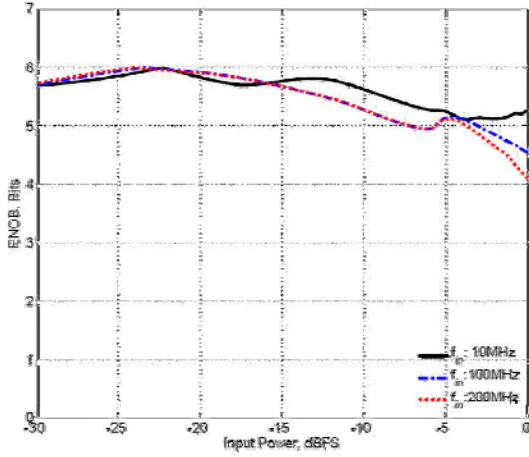
ADC DVT with a Single-tone Sinewave

ADC Input Power & Bandwidth Test

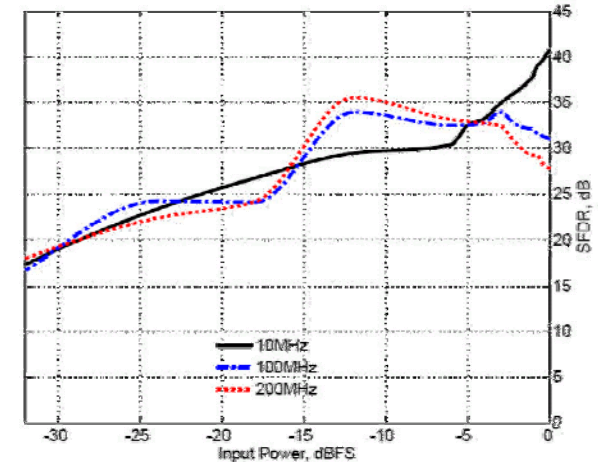
single-tone sine wave sampling at 800 MS/s



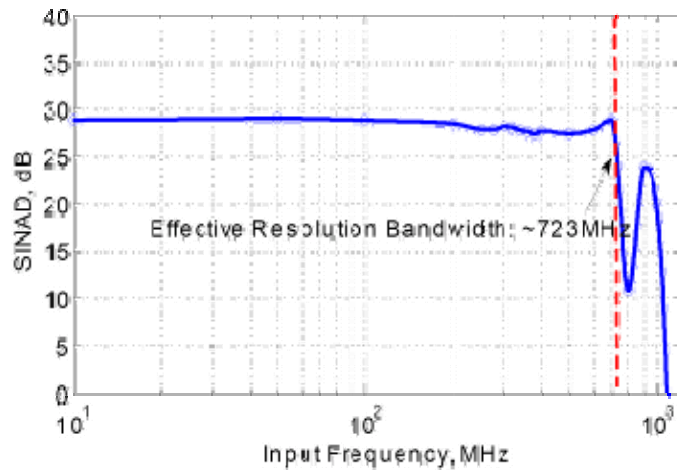
Signal-to-noise-and-distortion vs. input power



Effective-number-of-bit vs. input power



Spurious-free-dynamic-range vs. input power

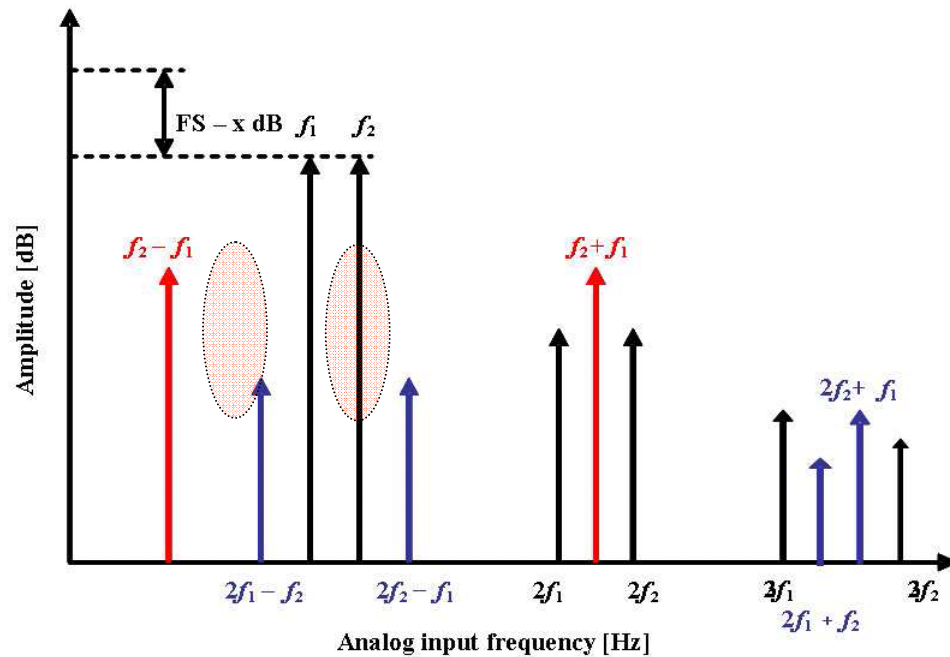


Effective resolution bandwidth – SINAD vs. Analog input frequency

Is this enough for verify the design and its system applications for communication?



System Non-linearity & Distortion



f_1, f_2

$f_1 \pm f_2$

$f_2 \pm 2f_1, 2f_1 \pm f_2, \text{ etc.}$

FS - x dB

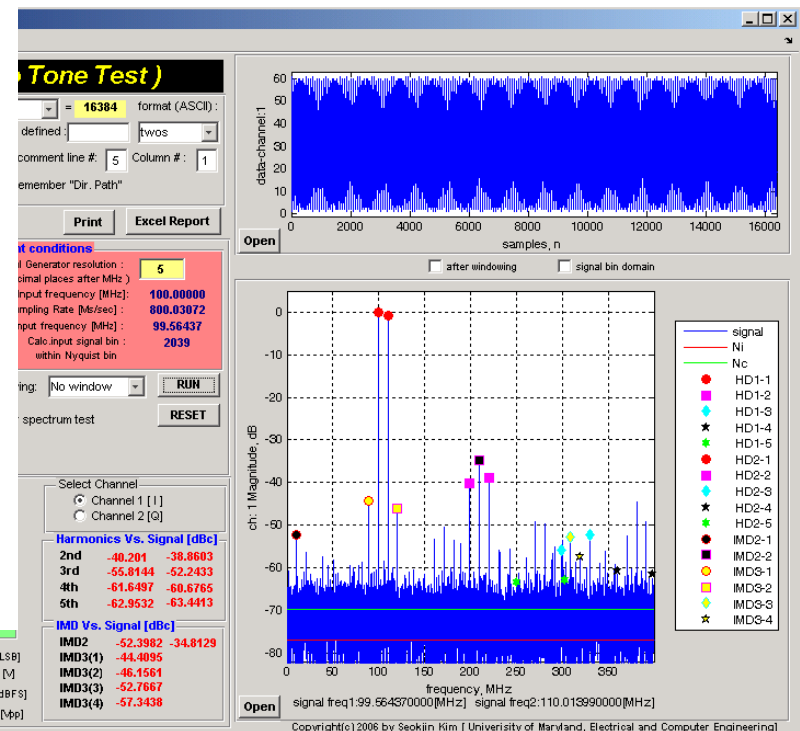
Fundamental signals

2nd order harmonics

3rd order harmonics

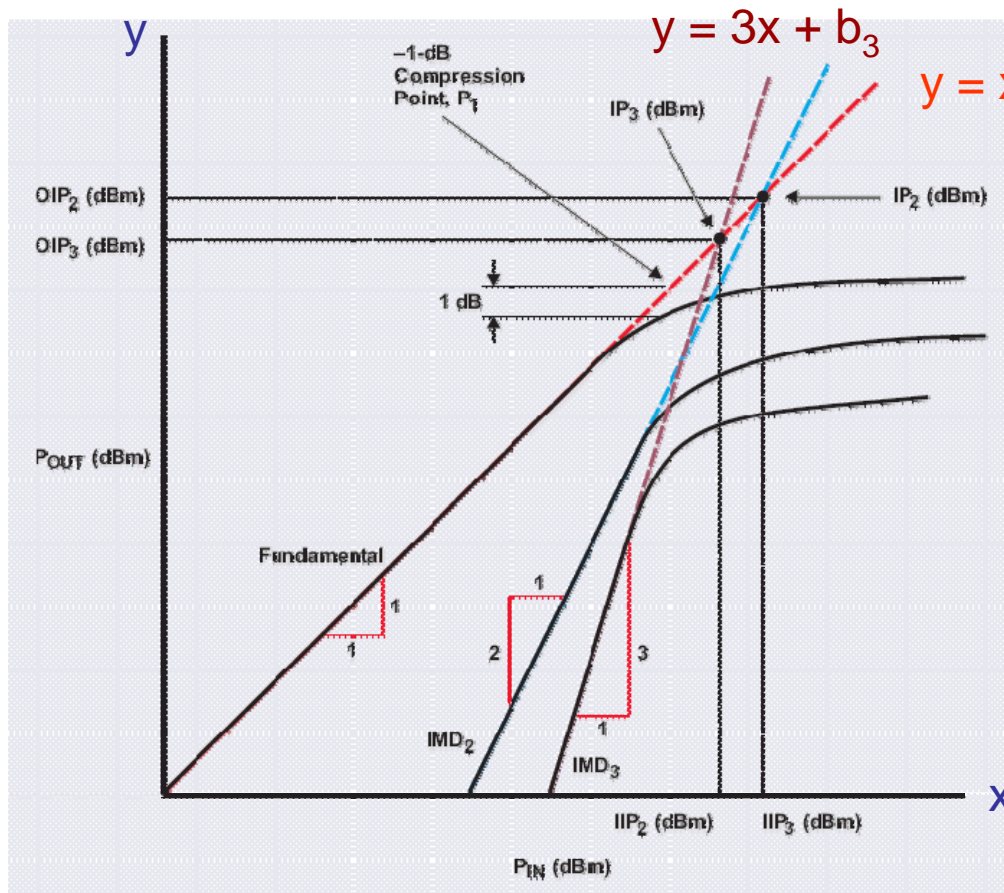
Input test signal amplitudes with respect to FS

offset	-0.5	N/A	[LSB]
V_offset	-0.00625	N/A	[mV]
Actual analog input level:	-0.42379	0	[dBFS]
Actual ADC Vin:	0.7619	VFS: 0.7994	[Vpp]





Amplifier Power Plot – P_{in} vs. P_{out}



Amplifier Linearity!

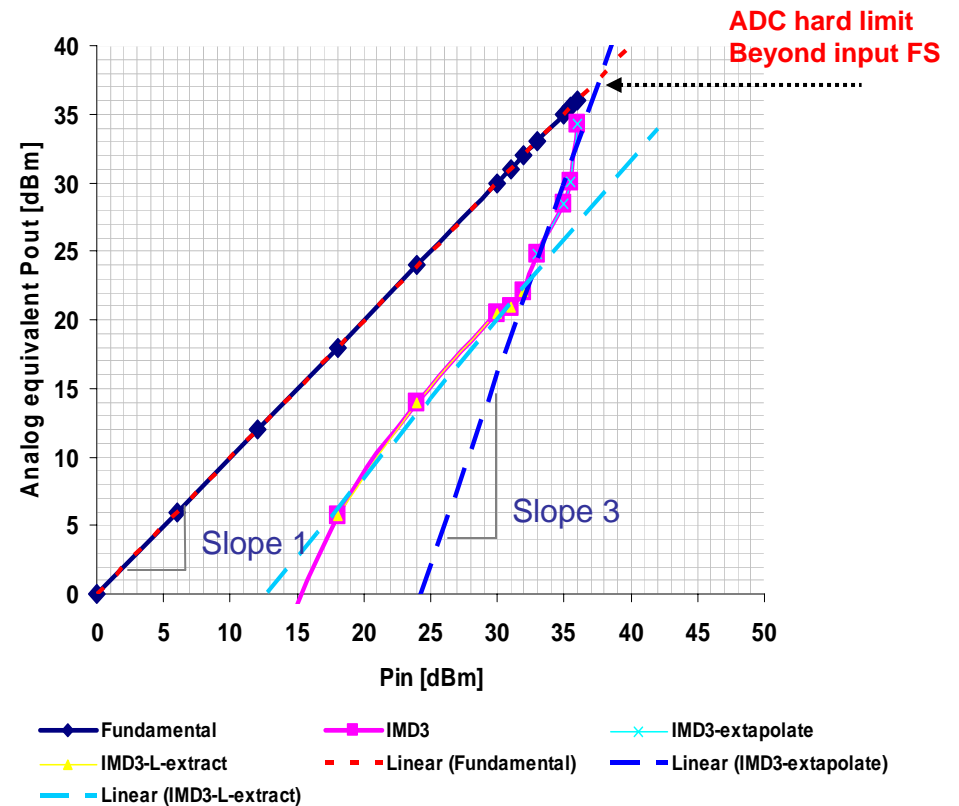
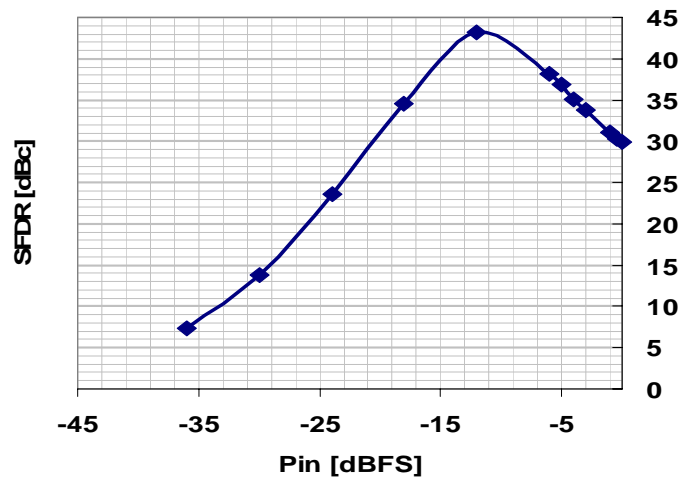
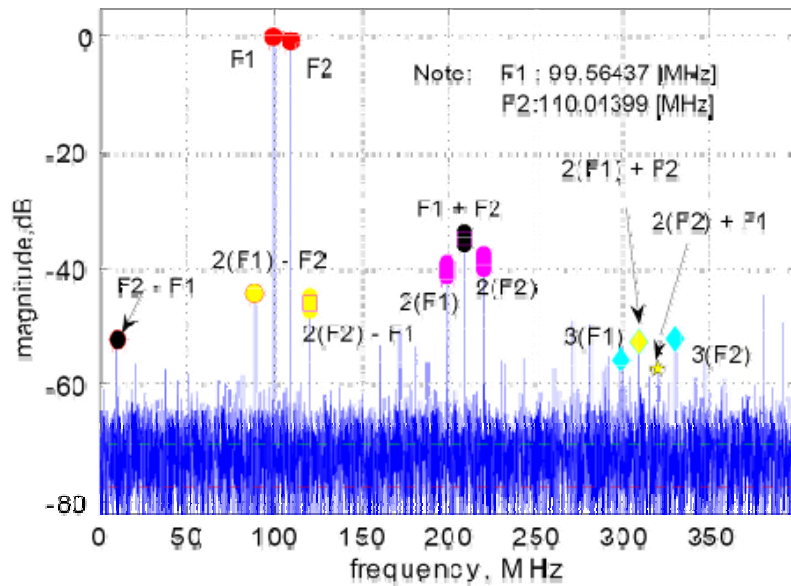


T/H Amps. & Comparators

- .
- .
- .



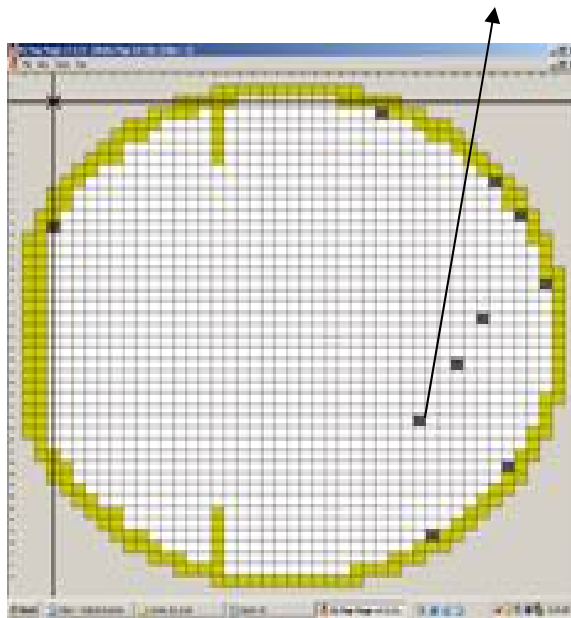
ADC DVT with 2-tone Signal



two-tone sine wave sampling at 800 MS/s

Production Tests

Continuity & IDDQ testing failed die



Wafer Map

Black squares are Continuity & IDDQ testing failed dies

Test	Wafer	Final
ESD and Continuity Checks		✓
Supply Current	✓	✓
Quiescent Voltage: Inputs	✓	✓
Input Full Scale (Over_range)	✓	✓
Input Full Scale (Under_range)	✓	✓
LVDS driver output logic level		✓
Input offset	✓	✓
'OVER_RANGE' output parameters		✓
'DATA_READY' Test		✓
Code Density Test: Low frequency		✓
ENOB Test: Low frequency		✓
Code Density Test: High frequency		✓
ENOB Test: High frequency		✓

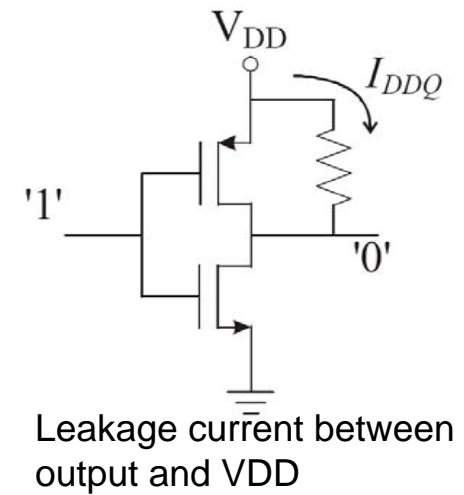
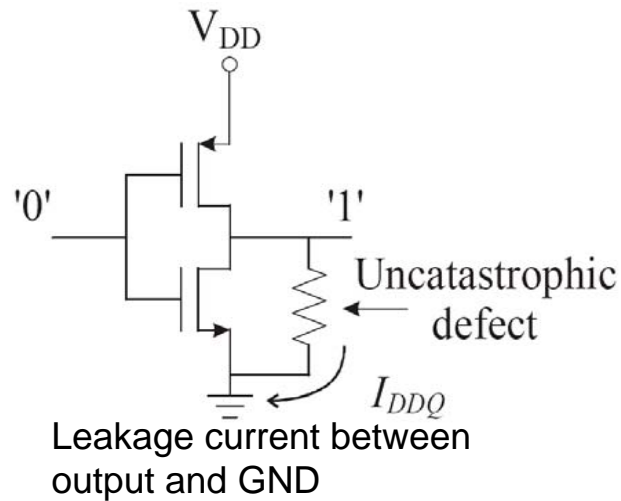
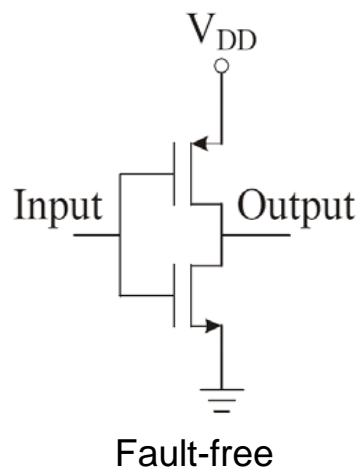
High-speed ADC

– wafer & final production test list



I_{DDQ} Test – Leakage Current

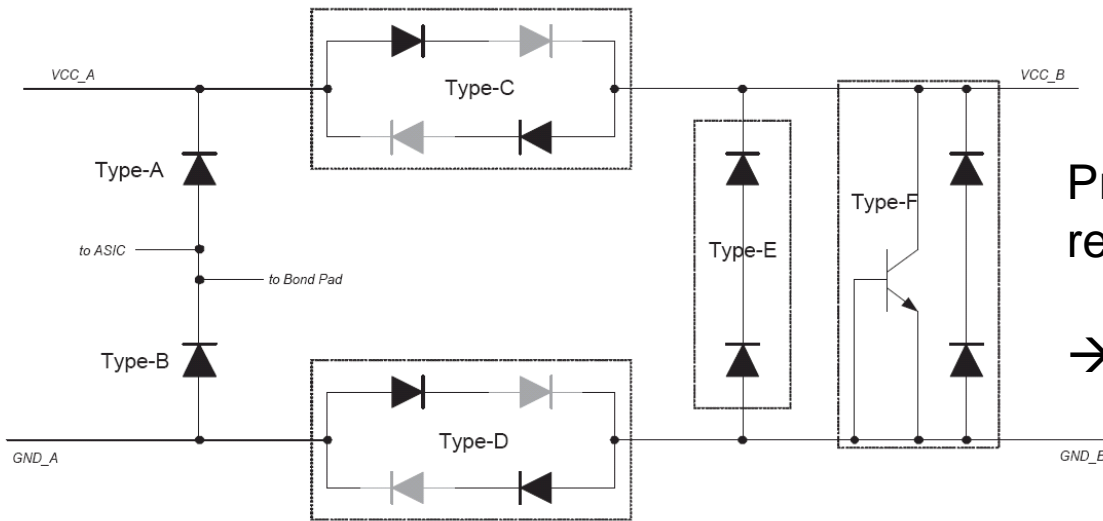
Digital I_{DDQ}



Part of Go/NoGo Test

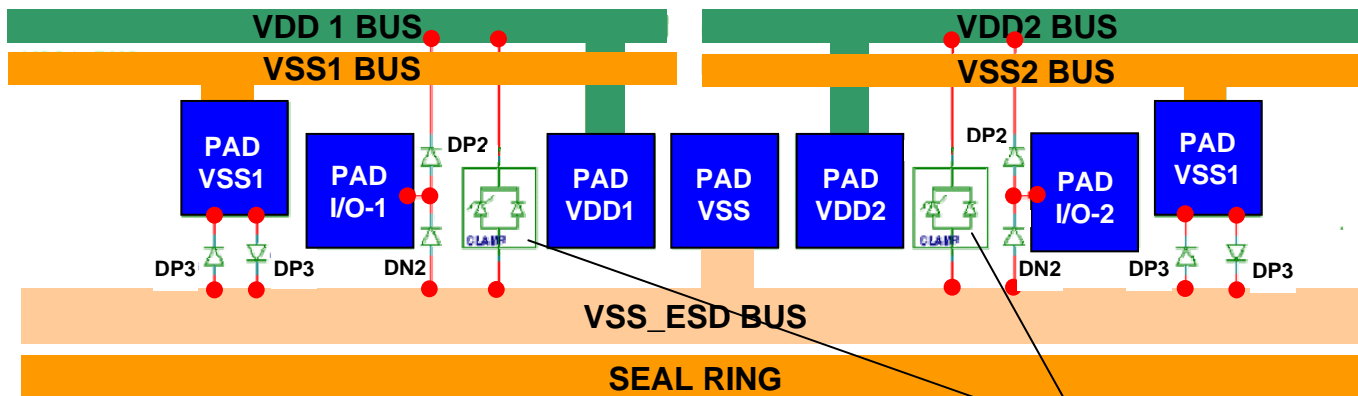


ESD diode leakage Current



Process Design Kit (PDK)
recommended ESD protection

→ Providing p-cell libraries



Power Clamp



Summary of Test Results

- Measurement range are targeting within the application signal bandwidth from 10 MHz ~ 250MHz
- DUT (HNS high speed ADC) operates mostly linearly under the input power level below 5 dBFS
- Code error test is useful to determine the presence of the timing error
- Testing in the temperature extremes at 250 MHz (ENOB at -40 °C: 4.99 [Bits], ENOB at +80 °C : 3.35 [Bits])

Frequency	10 MHz		100 MHz		200 MHz		250 MHz	
Channel	I	Q	I	Q	I	Q	I	Q
ENOB [Bits]	5.62	5.40	4.60	4.43	4.08	3.95	3.82	3.81
SINAD [dB]	34.55	33.58	28.43	27.72	25.37	24.80	25.56	23.96
SNR [dB]	35.68	35.81	34.83	34.91	33.66	33.72	33.11	32.95
THD [dB]	-41.89	-38.18	-29.63	-28.87	-26.13	-25.41	-25.27	-24.56
Offset [LSB]	-2.2	-1.0	-1.8	-0.9	-1.0	-0.3	-0.5	0.4
INL _{MAX} [LSB]	0.45	0.88	0.86	0.98	1.85	1.34	2.01	1.76
DNL _{MAX} [LSB]	0.21	0.28	0.26	0.28	0.33	0.29	0.13	0.35



Sensitivity Analysis of High-speed ADC

- Definition of “corner lot”

→ a wafer fabrication where the process is deliberately skewed to produce a certain wafer, so that ASIC performance can be physically evaluated at process extremes

- Temperature, process parameters, etc.

→ **Design Maturity and process stability**

- Hypothesis :

THAMES ADC consists of major two subcomponent devices – passive & active

Passive – resistors Active – BJT gain (β) and emitter area size

ADC performances are affected by over-all passive and active component behavior!

- Corner study test description:

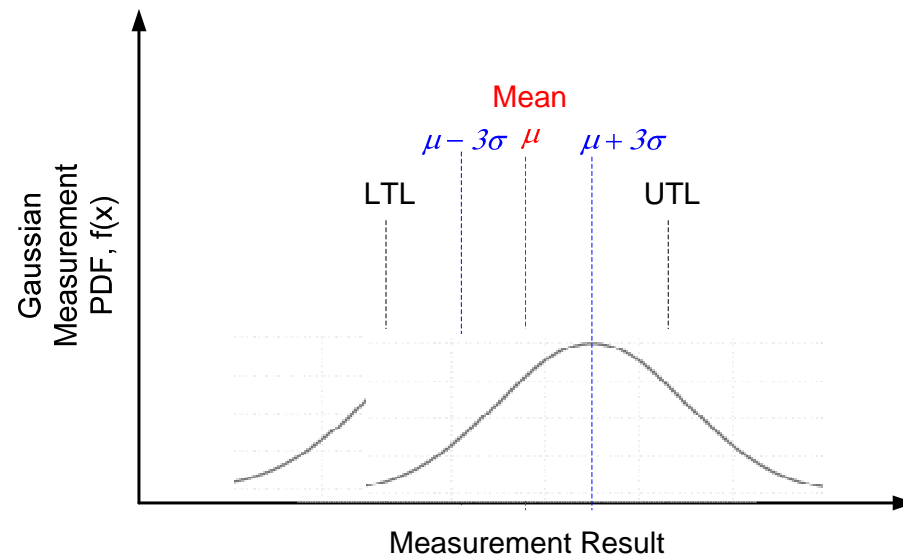
- ADC Functional DC tests and dynamic performance tests
- Numerous testing and statistical data analysis



Corner Lot Splits

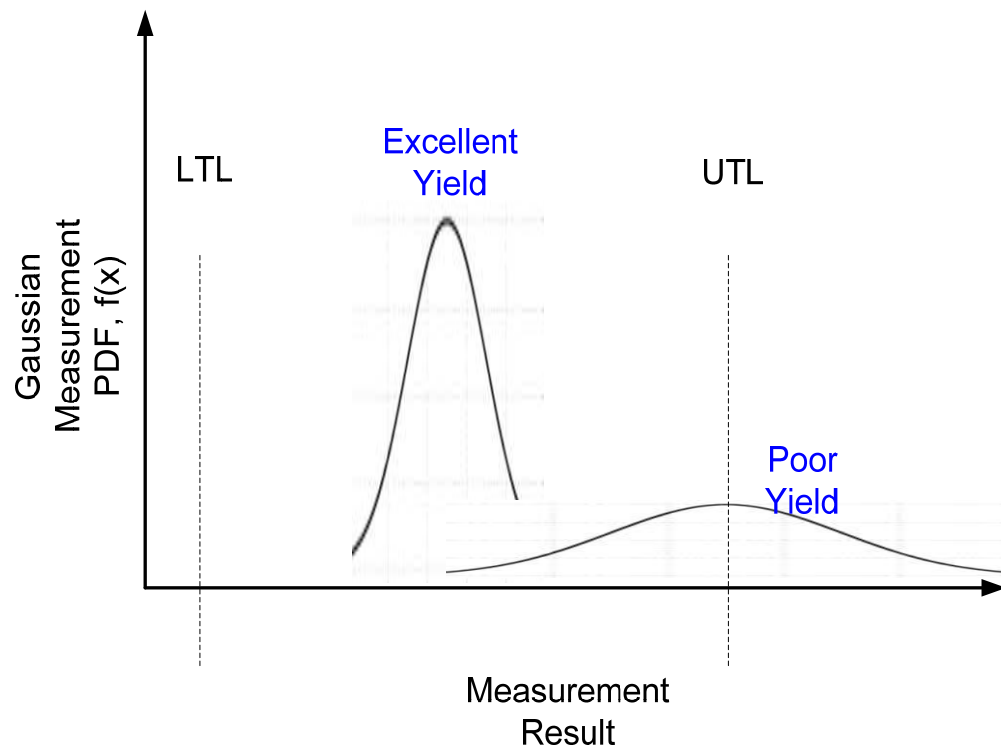
Corner Lot Split	Wafers	Lot Designation	REpoly Rsheet	RNpoly Rsheet	BJT- β	BJT Emitter Area
1	1, 10	A, J	Nominal	Nominal	Nominal	Nominal
2	2, 11, 19	B, S	High	High	Nominal	Nominal
3	3, 12, 20	C, L, T	High	Low	Nominal	Nominal
4	4, 13, 21	D, M, U	Low	High	Nominal	Nominal
5	5, 14, 22	E, N, V	Nominal	Nominal	High	High
6	6, 15, 23	F, Z, W	Nominal	Nominal	High	Low
7	7, 16, 24	G, P, X	Nominal	Nominal	Low	High
8	8, 17, 25	H, Q, Y	Low	Low	Low	Low
9	9, 18	I, R	High	High	High	High

AT46000 BiCMOS Technology





High-speed ADC Yield

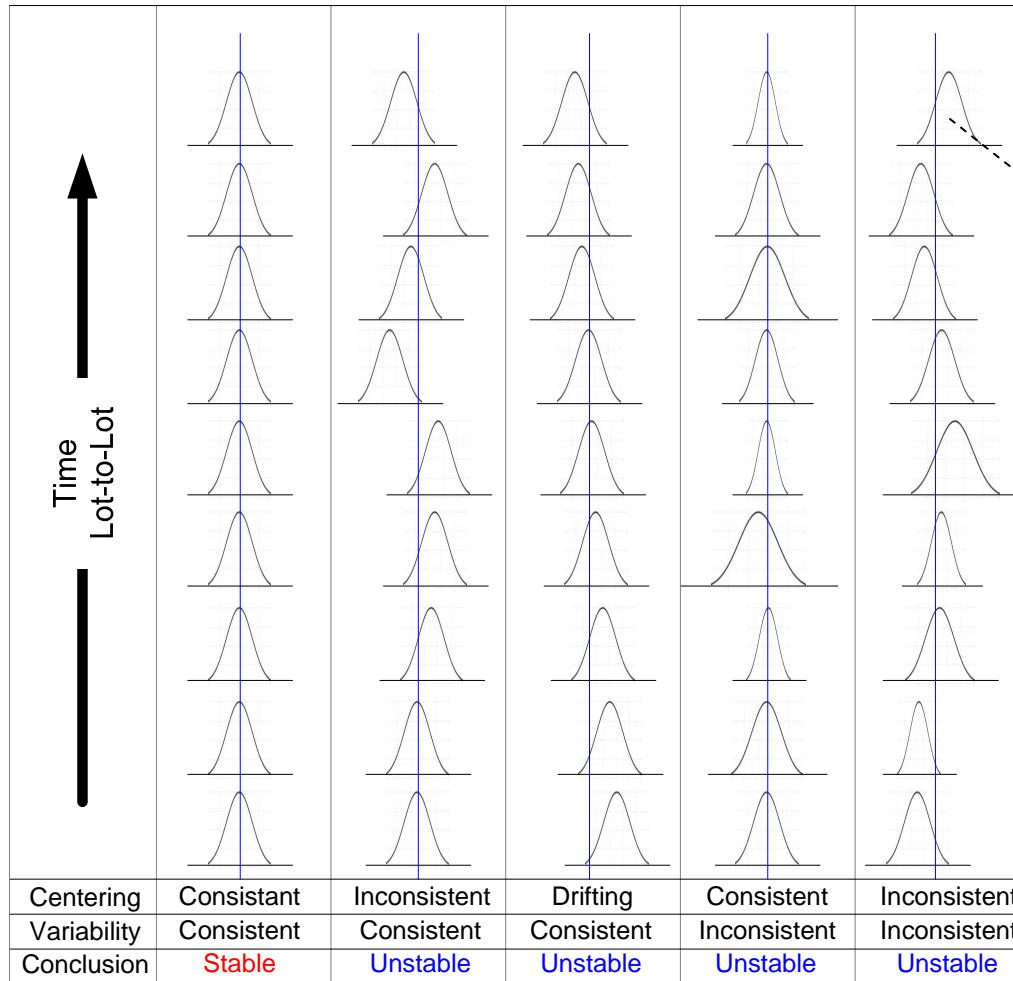


LTL: lower test limit
UTL: upper test limit

→ DUT-to-DUT mean and standard deviation determine yield



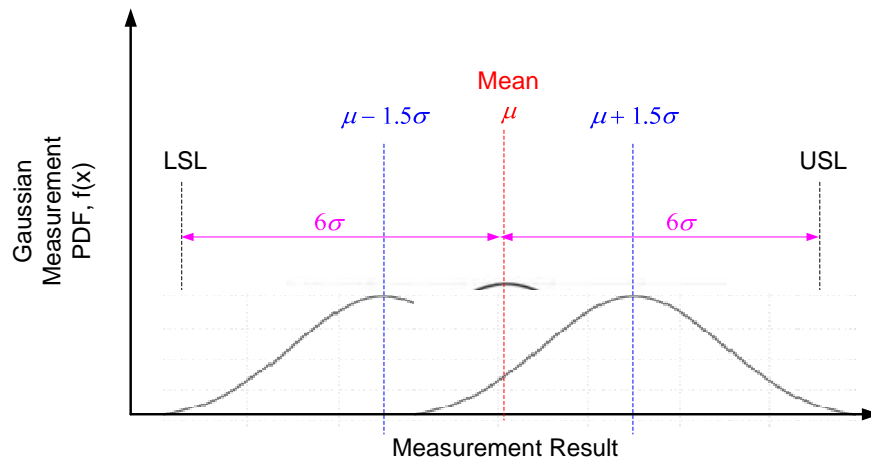
Process Stability & Design Maturity



Statistical Measurement
Gaussian distribution



Process Capability, C_p



$$C_p = \frac{USL - LSL}{6\sigma}$$

USL : upper specification limit
LSL : lower specification limit

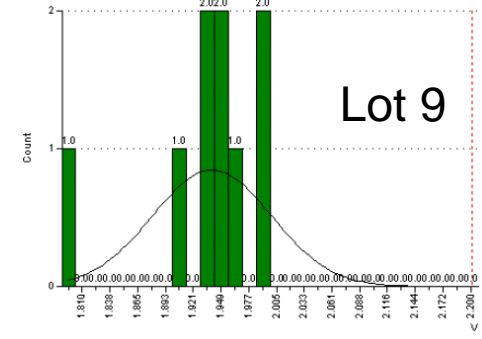
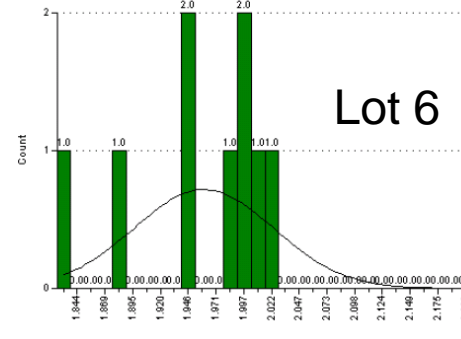
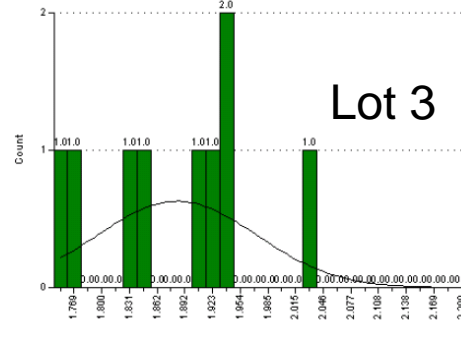
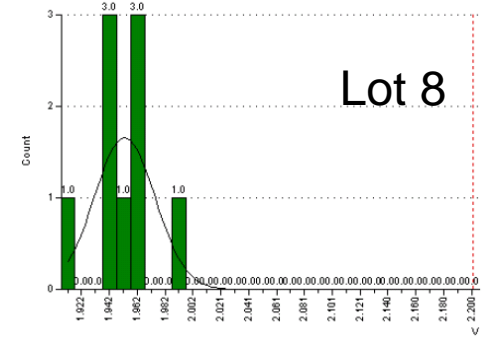
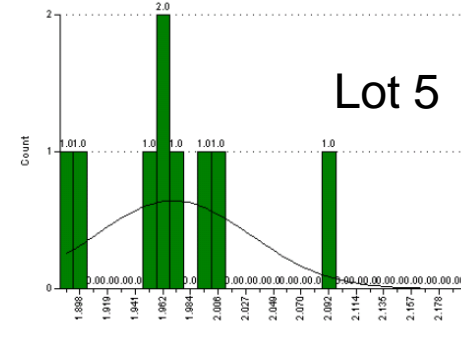
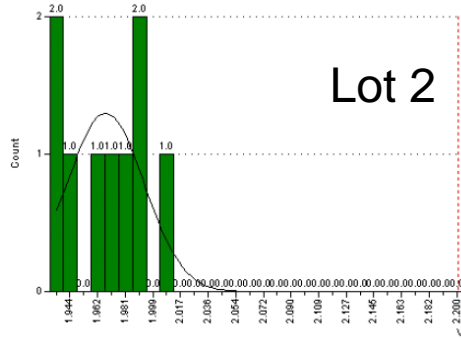
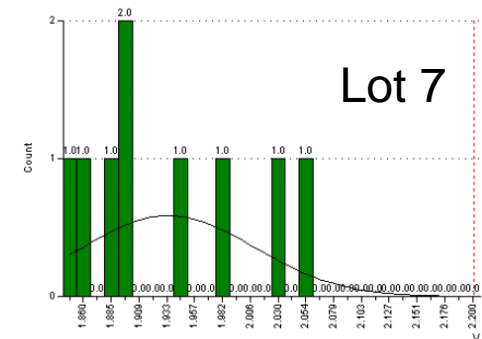
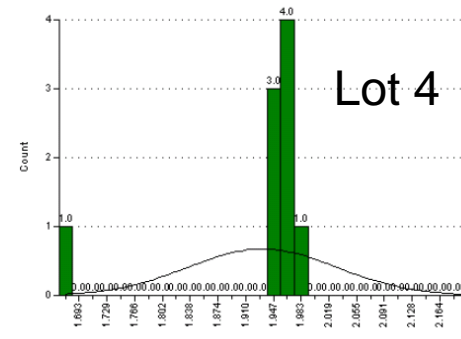
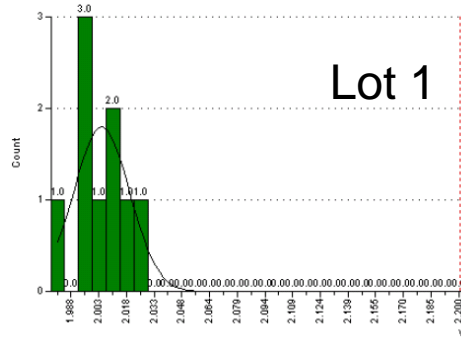
6- σ quality standard \rightarrow low defect rates (< 3.4 defect parts per million)

THAMES ASIC: $C_p > 4 \rightarrow$ Marginal rating!



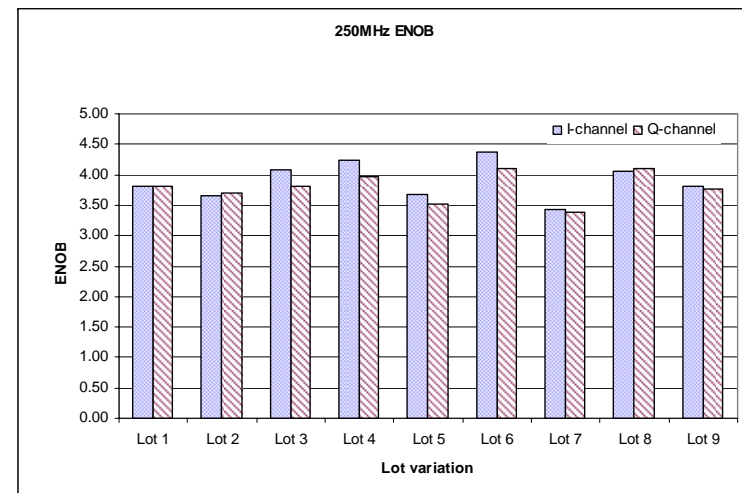
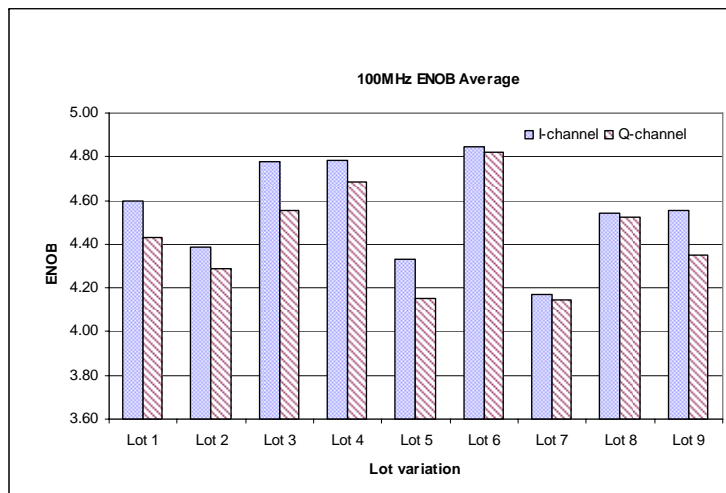
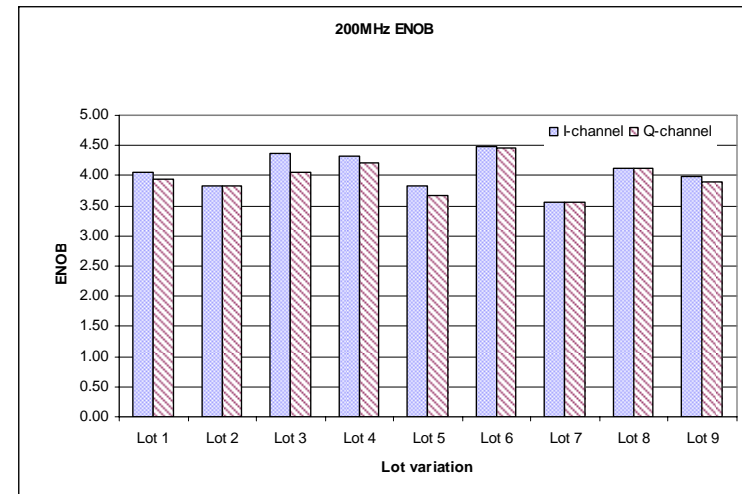
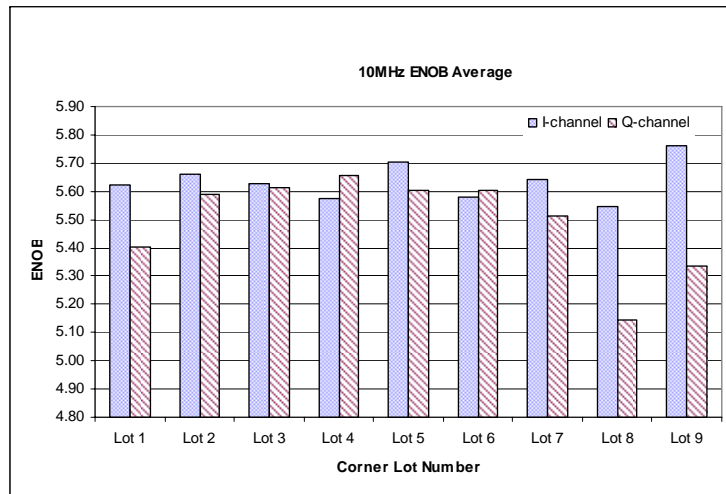
$V_{in_RF(I-)}$ bias voltage measurement

Statistical Measurement Example





ENOB for Each Lot Split





Summary

- ENOB Corner lot study result:
 - Lot 6 split has the best performance
 - Normal value (μ) of passive components
 - UTL of BJT- β (high gain)
 - LTL of BJT emitter size (low parasitic junction C)
 - Linearity of the active component effect !!
- Statistical process control ← corner lot study
 - Evaluate the quality of the process for high-speed ADC manufacturing
 - ADC test and measurement equipment effect included
 - Stability of high-speed ADC manufacturing process

Conclusions

HUGHES



Actual ADC mounted on
Spaceway indoor receiver

Achievements:

- Enhancements due to DfT:
 - Testability
 - Calibration and on-bench debugging
 - Cost effectiveness of testing in manufacturing.
 - A step-by-step sequence of operations for dynamic performance testing of high speed ADC (dual channel, 6-bit, 800 MS/s)
 - Test methodology for reducing test costs and overcoming test hardware limitations
-
- Verification tool development – VTS suite
 - High-speed ADC design parameter sensitivity
 - Corner lot study
 - Production test ready (approach to ATE)





THANK YOU

&

Questions?

