

## ABSTRACT

Title of Document: GALLIUM NITRIDE NANOWIRE BASED  
ELECTRONIC AND OPTICAL DEVICES.

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Gallium nitride nanowires have significant potential for developing nanoscale emitters, detectors, and biological/chemical sensors, as they possess unique material properties such as wide direct bandgap (3.4 eV), high critical breakdown field, radiation hardness, and mechanical/chemical stability. Although few results of individual GaN nanowire devices have been reported so far, most of them often utilize fabrication processes unsuitable for large-scale nanosystems development and do not involve fundamental transport property measurements. Understanding the transport mechanisms and correlating the device properties with the structural characteristics of the nanowires are of great importance for realizing high performance devices.

Focused ion beam induced metal deposition was used to make individual GaN nanowire devices, and assessment of their electrical properties was performed. The nanowires were grown by direct reaction of Ga and NH<sub>3</sub>, with diameters ranging from

80 nm to 250 nm and lengths up to 200  $\mu\text{m}$ . Dielectrophoretic alignment was used to assemble these nanowires from a suspension on to a large area pre-patterned substrate. A fabrication technique, utilizing only conventional microfabrication processes, has been developed for realizing robust nanowire devices including field effect transistors (FETs), light emitting diodes (LEDs), Schottky diodes, and four-terminal structures. Nanowire FETs with different gate geometries were studied, namely bottom gate, omega-backgate, and omega-plane gate structures. Utilizing omega-backgated FETs, transconductance as high as  $0.34 \times 10^3 \mu\text{S mm}^{-1}$  has been obtained. Room temperature field effect electron mobility in excess of  $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  have been exhibited by a nanowire FET, with a 200 nm diameter nanowire and Si substrate as the backgate. The observed reduction of mobility in the GaN nanowire FETs with decreasing diameter of the nanowire is attributed to the surface scattering. Electron beam backscattered diffraction revealed that the grain boundary scattering is present in some of the nanowires. Temperature dependent mobility measurements indicated that the ionized impurity scattering is the dominant mechanism in the transport in these nanowires. GaN nanoLEDs have been realized by assembling the n-type nanowires on a p-GaN epitaxial layer using dielectrophoresis. The resulting p-n homojunctions exhibited 365 nm electroluminescence with a full width half maximum of 25 nm at 300 K.

GALLIUM NITRIDE NANOWIRE BASED ELECTRONIC AND OPTICAL  
DEVICES

By

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Dissertation submitted to the Faculty of the Graduate School of the  
University of Maryland, College Park, in partial fulfillment  
of the requirements for the degree of  
Doctor of Philosophy  
2007

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## Preface

This dissertation contains 8 chapters. Most of the results discussed here have been published and presented in numerous referred journals and conferences. Significant details have been added to the chapters 4 and 6, besides the published results. The publications and conference presentations germane to the results are listed chapter wise.

### **Chapter 2: Gallium Nitride Nanowire Growth and Characterization**

M. He, **A. Motayed**, and S. N. Mohammad, “Phase separations of single-crystal nanowires grown by self-catalytic chemical vapor deposition method,” J. Chem. Phys. 26, 064704 (2007).

### **Chapter 3: Focused Ion Beam Assisted Fabrication of Nanowire Devices**

-**A. Motayed**, A. Davydov, M. Vaudin, I. Levin, J. Melngailis, and S. Mohammad, “Fabrication of GaN-based Nanoscale Device Structures Utilizing Focused Ion Beam Induced Pt Deposition,” J. Appl. Phys. 100, 024306 (2006).

-**A. Motayed**, A.V. Davydov, M. Vaudin, J. Melngailis, and S. N. Mohammad, “Fabrication and Characterization of Nanoscale Devices from Gallium Nitride Nanowires Utilizing Ion Beam Induced Metal Deposition Techniques,” 47<sup>th</sup> Annual Minerals, Metals & Materials Society Electronic Materials Conference, Santa Barbara, CA, USA, 2005.

**Chapter 4, 5, and 6: Electric Field Assisted Alignment of Nanowires, Fabrication of Nanowire Devices and Process Optimization, and GaN Based Nanowire Electronic Devices**

-**A. Motayed**, M. He, A. V. Davydov, J. Melngailis, and S. N. Mohammad, “Realization of Reliable GaN Nanowire Transistors Utilizing Dielectrophoretic Alignment Technique,” J. Appl. Phys. 100, 114310 (2006).

-**A. Motayed**, A. Davydov, M. He, J. Melngailis, and S. Mohammad, “A Simple Model for Dielectrophoretic Alignment of GaN Nanowires,” JVST B. 25, 120 (2007).

-**A. Motayed**, M. Vaudin, A. V. Davydov, J. Melngailis, M. He, and S. N. Mohammad, “Diameter dependent transport properties of gallium nitride nanowire field effect transistors,” Appl. Phys. Lett. 90, 043104 (2007).

-**A. Motayed**, A. V. Davydov, J. Melngailis, and S. N. Mohammad, “Large Scale Assembly of GaN Nanowires Using Dielectrophoretic Alignment,” International Semiconductor Device Research Symposium, Bethesda, MD, USA, 2005.

#### **Chapter 7: Gallium Nitride Nanowire-substrate UV Light Emitting Diodes:**

-**A. Motayed**, M. Vaudin, A. V. Davydov, J. Melngailis, M. He, and S. N. Mohammad “365 nm Operation of n-GaN nanowire p-GaN substrate homojunction light emitting diodes,” Appl. Phys. Lett. 90, 183120 (2007).

-**A. Motayed**, A. V. Davydov, M. He, J. Melngailis, and S. N. Mohammad, “Dielectrophoretic Alignment and Fabrication Technique for Realizing GaN Nanowire Devices,” Materials Research Society Spring Meeting, Boston, MA, USA 2006.

## **Dedication**

*To the memory of my parents,  
who showed me how to dream,  
and  
to my wife, Urmi, for being there with me.*

## **Acknowledgements**

During past six years I have had the pleasure of knowing and working with many wonderful and remarkable people. Without their help, guidance, and support, I would not have been able to finish what I started. I would like to thank Dr. John Melngailis for being so supportive of me and my research. His constant encouragement and guidance were truly invaluable. He always made himself available whenever I needed his suggestion or help. I express my sincere gratitude to Dr. S. N. Mohammad, for giving me the very first opportunity to prove myself. Without him, nothing of this would have been possible. His constant inspirations were the most invaluable.

This dissertation would never have been successful without the support of the wonderful people at the National Institute of Standards and Technology. Special thanks go to Dr. Daniel Josell, Dr. William Boettinger, Dr. Frank Gayle, and Dr. Carol Handwerker for giving me such a wonderful opportunity. Working under Dr. Albert Davydov at NIST was such a memorable experience. He has been a wonderful mentor and a friend. He taught me numerous aspects of materials science and many other things, which made this project possible. My appreciation goes to Dr. Norman Sanford, Dr. John Schlager, and Dr. Chris Bertness for their help. Special thanks to Dr. Babak Nikoobakht, Siddarth Sundaresan, and Sandy Clagett for helping me with various things.

My sincere gratitude to my committee members, Dr. Salamanca-Riba, Dr. Newcomb, and Dr. Murphy for their time and valuable suggestions.

My deepest appreciation goes to my wife, Urmi, for supporting me through all these years. She made the most difficult times of my life quite livable. I am thankful



to my family, especially my uncle, Asok Motayed, for providing me the much needed support.

I express my gratitude to Mr. John Barry of IREAP for teaching me how to use the FIB tool. University of Maryland administrative officials, especially Dr. Dan Ballon, Maria Hoo, and Nancy L. Gong deserve recognition for helping me with quite a few important things.

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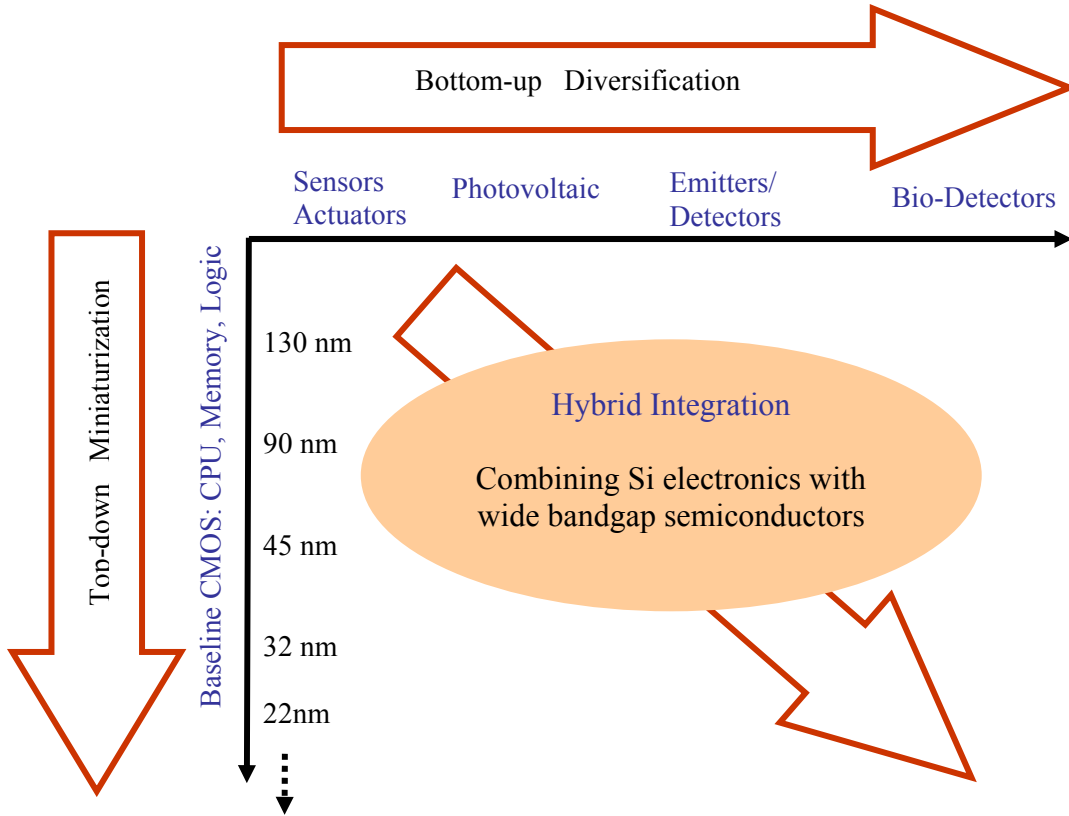
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## **Chapter 1: Introduction**

Nanoscience and nanotechnology is playing the very similar role in shaping the 21<sup>st</sup> century as the advent of printing press played in progressing the human civilization into the renaissance or the invention of steam engine in ushering the industrial revolution. Nanomaterials and nanostructures are defined as having at least one critical dimension of 100 nanometers or less, which is about the size of an average virus. Nanotechnology - the creation, manipulation, and application of materials at the nanoscale involves the ability to fabricate, control, and exploit the unique chemical, physical, and electrical properties of these nanostructures. At the nanoscale levels, the physical, chemical, and biological properties of materials differ in fundamental and quite often valuable ways from the properties of bulk matter [1]. These properties enable development of highly complex and multifunctional materials and systems, which have tremendous potential in improving our lives in numerous ways.

Since 1989, when IBM researchers demonstrated a scientific breakthrough by constructing a 35-atom depiction of the company's logo using a Scanning Tunneling Microscope (STM) [2], the aspiration to control materials at the nanometer level is sweeping industry and academia alike. The power of nanotechnology emerges from the fact that at nanometer scale new and exciting properties emerge in materials that are not possible or not exhibited by those same materials when they have much larger dimensions. These include (but not limited to) optical, electronic, magnetic, chemical, and mechanical properties—depending on the particle, any or all of these can be altered at the nanoscale.

Two different philosophies exist when it comes to realizing these nanostructures: top-down and bottom-up (Fig. 1.1).

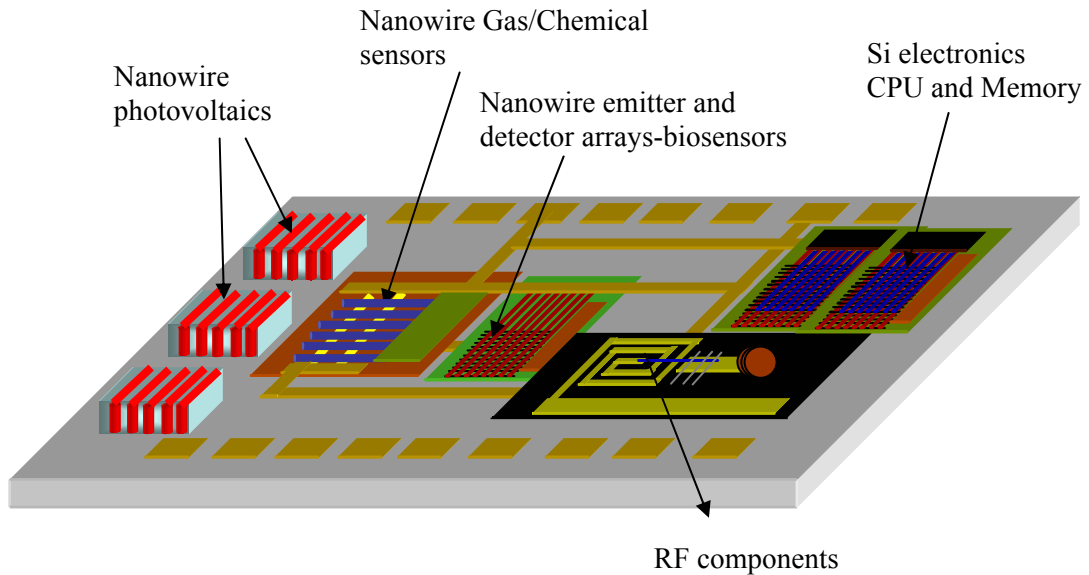


**Figure 1.1:** Top-down versus bottom-up approach towards nanotechnology.

Bottom-up paradigm focuses on the design and synthesis of nanoscale building blocks, elucidation of the fundamental electronic, optical, and other physical properties of these building blocks, and development of methods for hierarchical organization of these building blocks into increasingly complex integrated assemblies. On the other hand, the top-down approach attempts to scale down the dimensions by pushing the limits of conventional micro-manufacturing. Top-down approach has been quite successful in terms of reducing the gate lengths (current state-of-the-art CMOS devices have 65 nm nodes) and packing densities [3]. Top-

down techniques work by improving the existing microfabrication processes and innovating new techniques to achieve smaller critical dimensions.

In order to exploit the wide array of material properties and integrate them with existing Si technology, to produce complex and highly functional systems, we have to develop efficient bottom-up techniques. We can consider one scenario where the bottom-up technique has its own advantage. Direct bandgap semiconductors such as gallium nitride (GaN), gallium arsenide (GaAs), and indium phosphide (InP) are often used to realize optical elements (lasers diodes, light-emitting diodes, detectors, etc) due to their efficient recombination and generation properties [4], [5]. To this date, optical elements are either produced as stand-alone devices or integrated with the drive electronics of the same material system. These devices or systems are interfaced with Si microelectronics using off-chip fiber optic connections. Using bottom-up techniques, we can integrate optical nanowire devices directly onto a Si drive electronics chip. This would increase data communication speeds and provide a platform to develop all optical networks. This technique could be extended to integrate nanowires of different material systems, each performing a specific task, with standard Si computing and memory elements. This could eventually lead to highly functional systems such as autonomous sensor clusters (Fig. 1.2) with biological/chemical sensors and RF communication elements integrated with Si electronics, capable of detecting environmental parameters and transmitting the information over a communication link. Integrating nano-photovoltaics will make these systems truly self-sufficient.



**Figure 1.2:** An example of hybrid integration – smart, autonomous sensor node. With on-board Si processor, chemical/biological sensors realized from nanowires, communication components, and photovoltaic cells to generate power, they could work without human intervention for indefinite period of time.

## 1.1 Nanowires and Nanotubes

Nanowires and nanotubes are structures that are cylindrical in shape, with length to diameter ratios often greater than  $10^3$ . Unlike nanowires, nanotubes are hollow structures with single or multi walls (like carbon nanotubes). Nanowires and nanotubes are highly functional structures with unique properties arising from their low dimensionalities [6]. As they are often grown without any substrates, lattice mismatch and thermal expansion coefficient mismatch problems are not present in these structures. This could mean achieving materials that are free from strain, dislocations, and other structural defects. Due to their high surface to volume ratio, the conduction through these nanowires is strongly affected by the chemical species adsorbed on their surfaces [7]. This would enable us to develop nanoscale, extremely



efficient chemical and biological sensors. Their large surface to volume ratio also enables effective heat removal in these devices. Photo-generation and light extraction are also enhanced due to large surface area in these structures. As nanowires and nanotubes can be placed on any substrate after the growth is completed, they could be integrated with any platforms, including flexible substrates. Once they are placed on pre-determined positions on a substrate, it is relatively simple to apply the conventional fabrication processes to realize electrical and optical devices [8]. This opens up possibilities of integrating exotic III-V compound semiconducting nanowire devices with conventional Si microelectronics. Reduced dimensionality enhances electronic, mechanical, chemical, and optical properties in these nanowires. For nanowires and nanotubes with diameters less than 10 nm, discrete energy levels are formed, which could lead to ballistic transport of electrons through the nanowire [9]. These nanowires and nanotubes are ideal material systems to study fundamental transport properties such as conductance quantization, universal conductance fluctuations, coulomb blockade, etc [10] - [12].

## **1.2 Semiconducting Nanowires and Nanorods**

With all its advantages, carbon nanotubes suffer from one major drawback - lack of control in selective growth of semiconducting and metallic nanowires [13]. A convenient method to separate metallic and semiconducting nanowires does not exist to this date. Also, carbon nanotubes do not allow control of their bandgaps, hence opportunities of making multi-spectral optical elements using carbon nanotubes are limited. Semiconducting nanowires, especially compound semiconductors provide

greater flexibility as their bandgaps and doping properties can be controlled by alloy and impurity concentrations, respectively. Heterostructures like core-shell structures can be only formed in semiconducting nanowires, by growing a shell of different bandgap on a nanowire [14], [15]. These kinds of heterostructures are extremely important, as through bandgap engineering we can realize high performance devices such as high electron mobility transistors, resonant tunneling diodes, and laser diodes from these nanowires.

### **1.3 Gallium Nitride and Related Alloys**

The group III nitrides (AlN, GaN, and InN) and their ternary and quaternary alloys are important class of semiconductors with unique properties such as a direct bandgap spanning the whole solar spectrum (from 0.7 eV for InN to 6.2 eV for AlN), high carrier saturation velocity, high breakdown electric field, and excellent mechanical/thermal stability [16]. As a result nanostructures and nanodevices made from GaN and related nitrides can be utilized to achieve nanoscale ultraviolet (UV)/visible light emitters, detectors, high-speed/high-power transistors and radiation hard, high- temperature electronic devices. Integrating these nitride nanodevices with Si microelectronics could eventually lead to single chip solution for complex optical communication elements, biodetection, chemical sensing systems, etc.

GaN has an energy gap value that approaches 3.4 eV at room temperature (Fig. 1.3) enabling GaN devices to support peak internal electric fields about five times higher than silicon or gallium arsenide (GaAs). Wide bandgap results in lower thermal electron-hole pair generation, hence GaN devices can work at high

temperatures. Due to the larger cohesion energies of its constituent atoms, GaN is chemically robust material, less vulnerable to attack in caustic environments, and more resistant to radiation damage. Various physical properties of different semiconductors in comparison to Si are shown in Table 1.1.

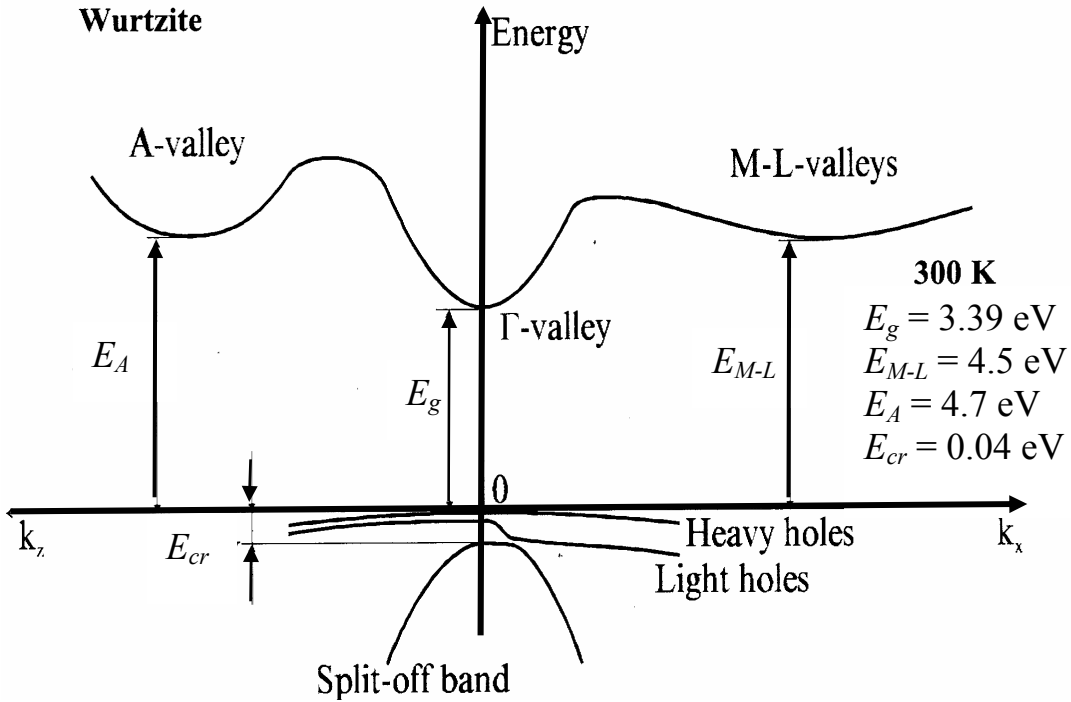
**Table 1.1:** Physical properties of Si and other important wide bandgap semiconductors [17].

Property	Si	GaAs	GaN	4H-SiC
Band gap, $E_g$ (eV) (300K)	1.12	1.43	3.4	3.26
Dielectric constant, $\epsilon_r$	11.9	13.1	9	10.1
Electric breakdown field, $E_c$ (kV/cm)	300	400	2000	2200
Electron mobility, $\mu_n$ ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ )	1500	8500	1250	1000
Hole mobility, $\mu_p$ ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ )	600	400	115	850
Thermal conductivity, $\lambda$ ( $\text{W cm}^{-1} \text{K}^{-1}$ )	1.5	0.46	1.3	4.9
Saturated electron drift velocity, $v_{sat}$ ( $\times 10^7 \text{ cm s}^{-1}$ )	1	1	2.2	2

\*  $\epsilon = \epsilon_r \epsilon_o$  where  $\epsilon_o = 8.854 \times 10^{-12} \text{ F m}^{-1}$

Bandgap of the ternary alloy  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  can be tuned with varying the mole fraction of Al. This provides means of growing heterostructures with potential wells for carrier confinements. Two-dimensional electron gas can be produced at the interface

of GaN and  $\text{Al}_x\text{Ga}_{1-x}\text{N}$ , because of their bandgap difference. Separating electrons from the donors increase their mobility and results in increased high frequency operation of the device.

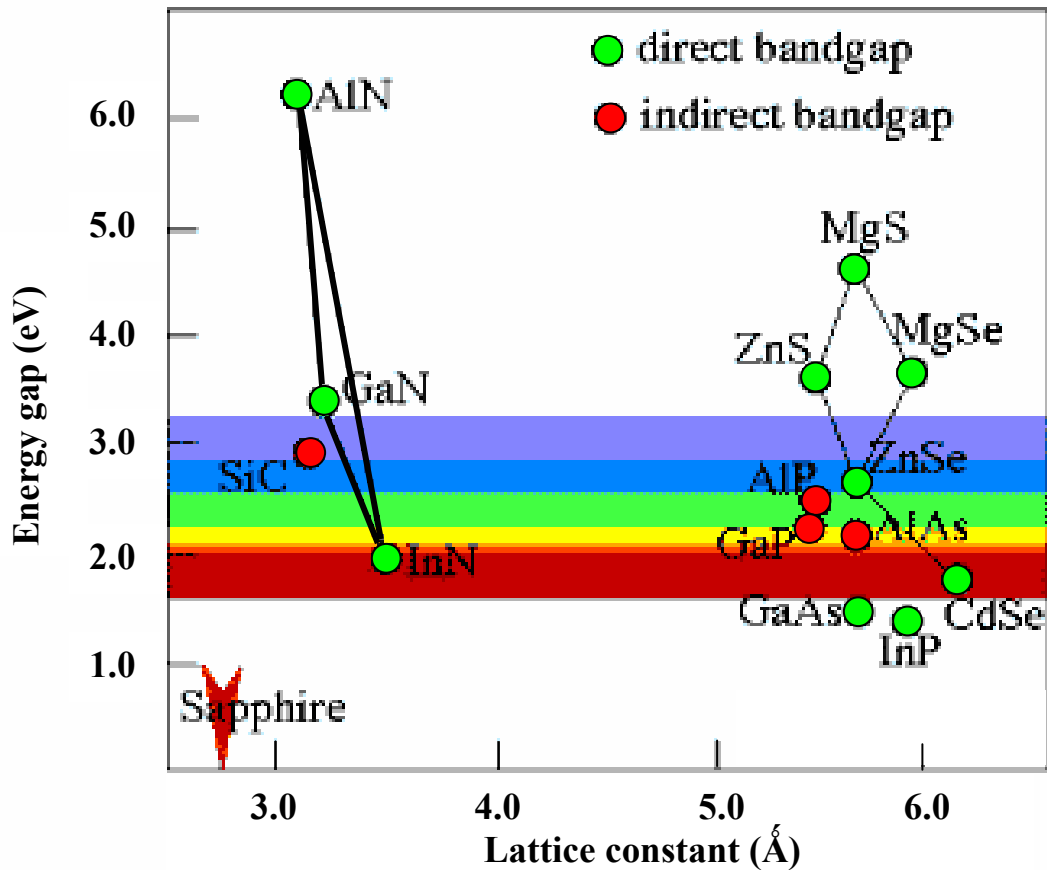


**Figure 1.3:** Energy band diagram of wurtzite GaN. Direct energy gap is 3.39 eV at 300 K.

Due to its direct bandgap, generation and recombination of electron-hole pairs are efficient. The bandgap of GaN corresponds to an emission wavelength in 360 nm range. This makes the nitride suitable for developing UV/ blue LEDs and Laser diodes.

## 1.4 Strategies for Developing Nanowire Devices

Successful realization of nanowire devices and complex nanosystems would require effective solutions to numerous challenges. Nanowire growth is still at its infancy. Growth methods are not fully understood and often lack dimensionality and orientation control. Also doping issues, both in-situ and ex-situ, have not been addressed in detail for nanowires.



**Figure 1.4:** Lattice constants and bandgap energy for different semiconductors at room temperature [18].

Characterization techniques (structural, optical, and electrical) normally used to characterize thin film semiconducting materials, are not readily applicable to the

nanowires. For example, x-ray diffraction technique which is often used to assess the crystalline qualities of a material cannot give an indication of the individual nanowire properties as it would require focusing of the x-ray beams with spot sizes of 200 nm or less. Thus more time consuming techniques like transmission electron microscopy (TEM) has to be used, which require elaborate sample preparation. Electron backscatter diffraction (EBSD) is a structural characterization technique that provides an easier alternative for individual nanowire structure determination, and as will be shown chapter 2 it can also be used to correlate structural properties with individual nanowire device characteristics.

One of most difficult challenges is developing a reliable assembling technique that is substrate and nanowire material independent. Controlling nanowire placement with reliability and repeatability is the key in producing hierarchical systems. Novel nanowire device designs are essential if we want to fully exploit their enhanced properties. For example, cylindrical-gate nanowire field-effect transistors (FETs), with the gate oxide and gate metal deposited conformally as a shell on the nanowire, will enhance the device performances dramatically. To realize these novel structures, innovative fabrication processes (conformal deposition techniques such as atomic layer deposition, liquid-phase deposition) are required. Device characterization and extraction of material properties (resistivity, mobility, and carrier concentration) are specially challenging for nanowires. Analytical relationships relating the device characteristics with structural properties often does not exist. Simple models and assumptions are generally employed. In order to understand the device properties, fully numerical techniques like finite element analysis are required. Correlating

device properties with structural characteristics of these nanowires will ultimately increase our understanding of the transport processes in these nanostructures, which will enable us eventually to realize superior performing nanowire devices. Understanding fundamental carrier transport properties and scattering mechanisms will complete our understanding of these nanostructures.

## **1.5 Contributions and Accomplishments**

This dissertation represents the research which has resulted in numerous publications in referred journals and contributed talks in national and international conferences. The nanowires used for this study was provided by Dr. Maoqi He of Howard University, Washington DC, under a project with joint collaboration between Dr. John Melngailis (University of Maryland, College Park) and Dr. S. N. Mohammad (University of Maryland, College Park). Transmission electron microscopy presented in chapter 2 was performed by Dr. Warren MoberlyChan of Lawrence Livermore National Laboratory (LLNL). The photoluminescence experiments on these nanowires were performed by Dr. Norman Sanford and Dr. John Schlager of National Institute of Standards and Technology (NIST). The cathodoluminescence measurements were performed by Dr. Joseph W. Tringe of LLNL.

Except the above mentioned results, experiments and results presented in this dissertation are obtained solely by the candidate. The significant accomplishments of this research are listed below:

1. Detailed structural characterizations have been carried out revealing important information about the nature of growth and structural defects in these nanowires.
2. Simple nanowire devices were demonstrated using focused-ion beam induced deposition technique, which enabled rapid estimation of the material properties. Interaction of focused-ion beam with GaN nanowire has been studied
3. Electric field was used to assemble these nanowires on a pre-patterned substrate. The alignment process has been studied in details, which lead to improved designs of the alignment electrodes and a systematic approach towards the development of the alignment process.
4. A general fabrication scheme utilizing only batch fabrication processes has been implemented, which is suitable for any material system. This type of fabrication scheme is quite advantageous over most of the reported methods as it provides a means for integrating nanodevices with conventional silicon microcircuitry.
5. We have designed and realized novel nanowire transistors with performances comparable to the state-of-the-art thin film and nanowire devices. This is quite encouraging as it indicates that with improved designs and materials these nanosystems could meet or exceed expectations of the future device or system designers.
6. Temperature dependent resistivity measurements indicated that the impurity concentration is quite high in these nanowires, which is possible due to oxygen or other structural defects. Temperature dependent mobility revealed that the



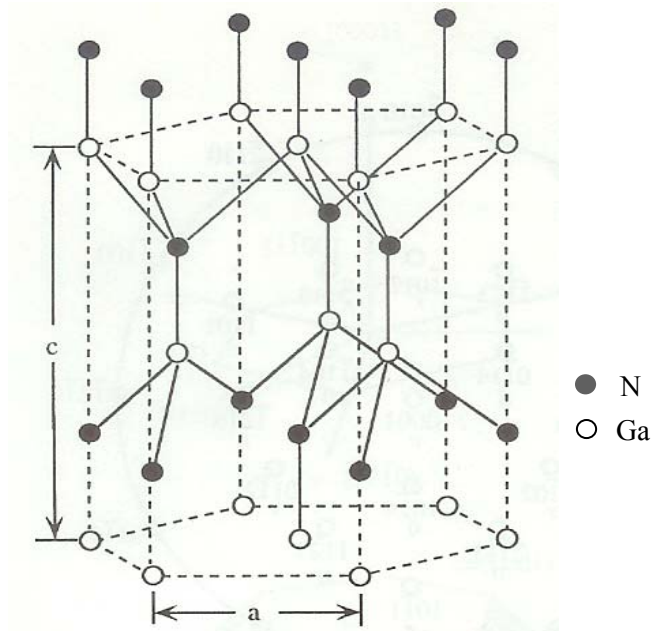
charged impurity scattering is the dominant mechanism in transport through these nanowires. These types of measurements are crucial in understanding the basic conduction processes in the nanowires.

7. Diameter-dependent mobility measurement in nanowire transistors indicated the evidence of surface scattering is smaller diameter nanowires. Using reverse engineering and microstructural characterization technique (electron backscattered diffraction), we were able to correlate the structural characteristics of these nanowire devices with their measured electrical properties. To the best of our knowledge, this type of study has not been reported before.

8. Ultraviolet nanowire light-emitting diodes (LEDs) have been realized by assembling GaN nanowires on p-GaN substrate, forming mechanical p-n junctions. These LEDs exhibited 365 nm emission with excellent thermal stability. This technique provides a simple technique for realizing wide-area emitting sources and multispectral emitter arrays. Emission from homojunctions of GaN nanowires has not been demonstrated before.

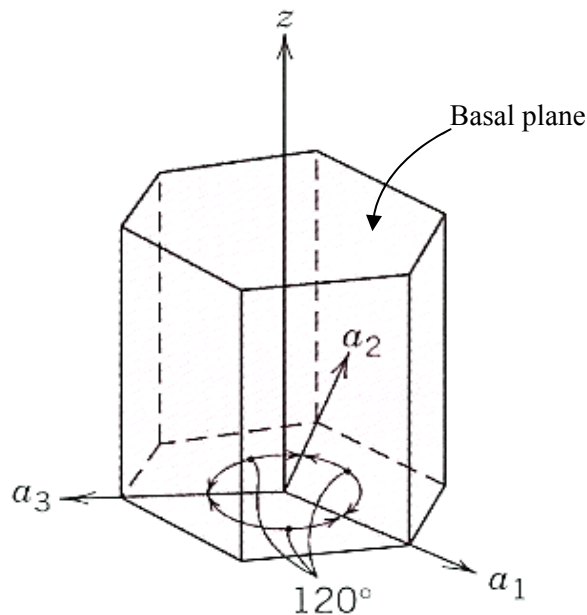
## Chapter 2: Gallium Nitride Nanowire Growth and Characterization

Gallium nitride (GaN) is a compound semiconductor which has a direct bandgap of 3.4 eV at room temperature. GaN and related nitrides have excellent material, optical, and electrical properties. There are three common crystal structures shared by the group-III nitrides: a) wurtzite, b) zincblende, and c) rocksalt structures. Under ambient conditions, the most thermodynamically stable structure is wurtzite for bulk AlN, GaN, and InN. The wurtzite structure has a hexagonal unit cell and thus two lattice constants,  $c$  and  $a$ . The wurtzite structure consists of two interpenetrating Hexagonal Close Packed (HCP) sublattices, each with one type of atoms, offset along the  $c$  axis of  $5/8$  of the cell height [16].



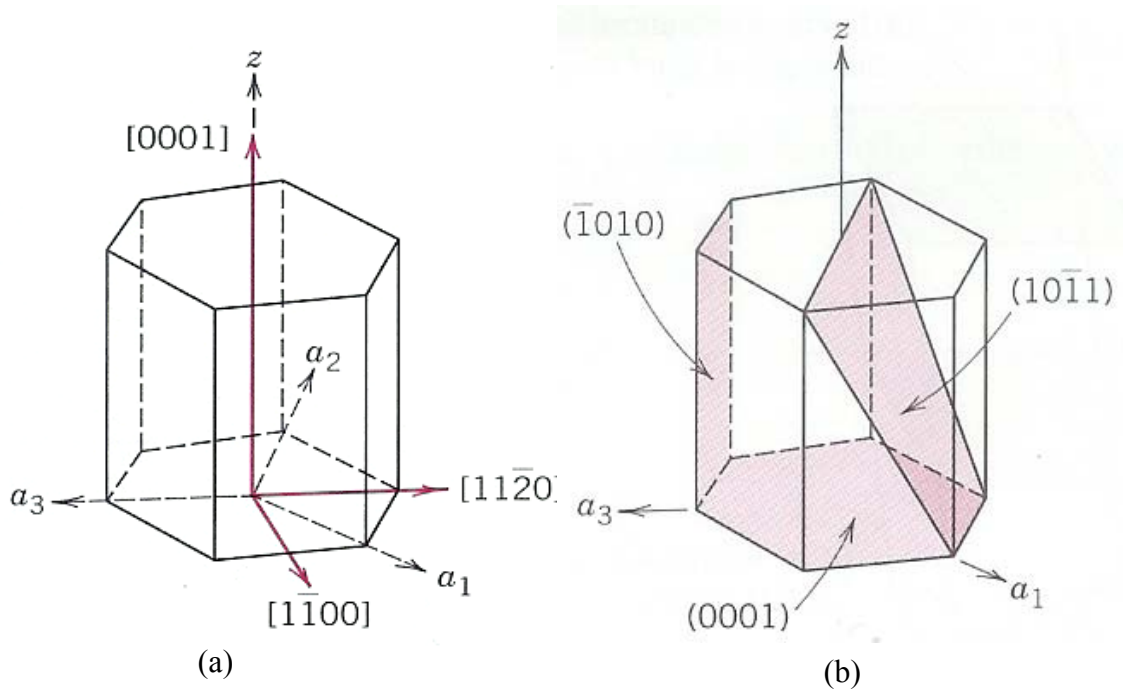
**Figure 2.1:** Crystal structure of wurtzite GaN. Basis unit cell is hexagonal closed pack (HCP) structure with alternating layers of Ga and N atoms.

The wurtzite crystal structure of GaN is shown in the Fig. 2.1, where the stacking order of Ga atoms (white) and N atoms (black) can be seen. In order to understand the growth and material properties of a semiconductor it is imperative to have a good understanding of its crystal structure. In order to interpret the results of structural characterization techniques, such as x-ray diffraction, transmission electron microscopy (TEM), and electron backscattered diffraction (EBSD), understanding of the crystal directions and planes is extremely helpful. In order to identify various crystallographic directions in a hexagonal system, a four-axis coordinate system, called Miller-Bravais system, is employed [19]. The three  $a_1$ ,  $a_2$ , and  $a_3$  axis are all contained within a single plane (called basal plane), and at  $120^\circ$  angles to one another (Fig. 2.2).



**Figure 2.2:** Four axes Miller-Bravais coordinate system for HCP structure [19].

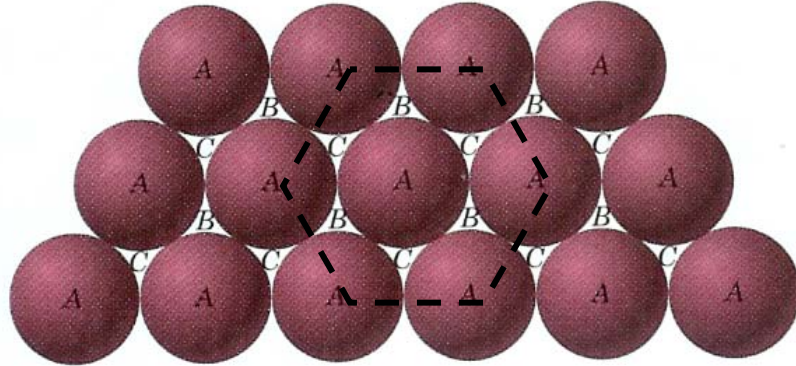
The  $z$  axis is perpendicular to this basal plane. Crystallographic directional indices are denoted by four indices, as  $[hkil]$ ; by convention, the first three indices pertain to projections along the respective  $a_1$ ,  $a_2$ , and  $a_3$  axes in the basal plane, and  $l$  is for the  $z$  axis [Fig. 2.3(a)]. The crystallographic planes in a hexagonal crystal are identified by three Miller indices as  $(hkl)$ , where  $h$ ,  $k$ ,  $i$ , and  $l$  are the reciprocal of the planar intercepts of for each axis [Fig.2.3 (b)] .



**Figure 2.3:** (a) Different crystallographic direction of the HCP structure. (b) Different crystallographic planes for the HCP structure.

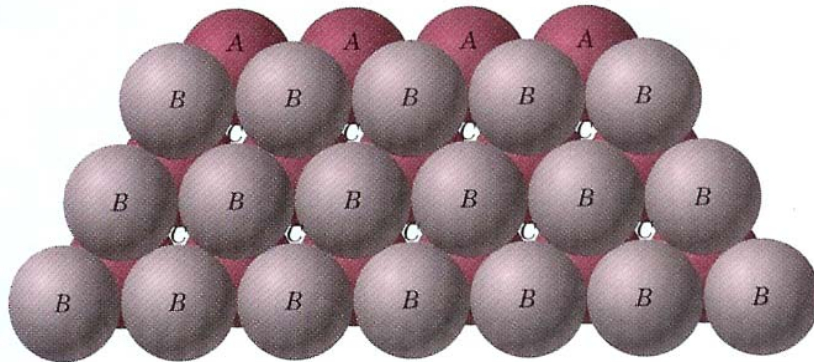
For the wurtzite structure, the stacking sequence (order of Ga and N atoms layered on top of another) in  $c$ -direction is  $Ga_A N_A Ga_B N_B Ga_A N_A Ga_B N_B \dots$ , which could be understood looking at the packing of spheres in Fig. 2.4-2.6. Centers of all atoms in one close-packed plane is labeled  $A$ . Associated with this plane are two sets of equivalent triangular depressions formed by three adjacent atoms. One can arbitrarily

mark the depressions pointing up as *B* and those pointing down as *C* (Fig. 2.4). A second close-packed plane may be positioned with centers of its atoms over either *B* or *C* sites; at this point they are identical. If position *B* is chosen then the stacking sequence is termed as *AB*, which is illustrated in Fig. 2.5.



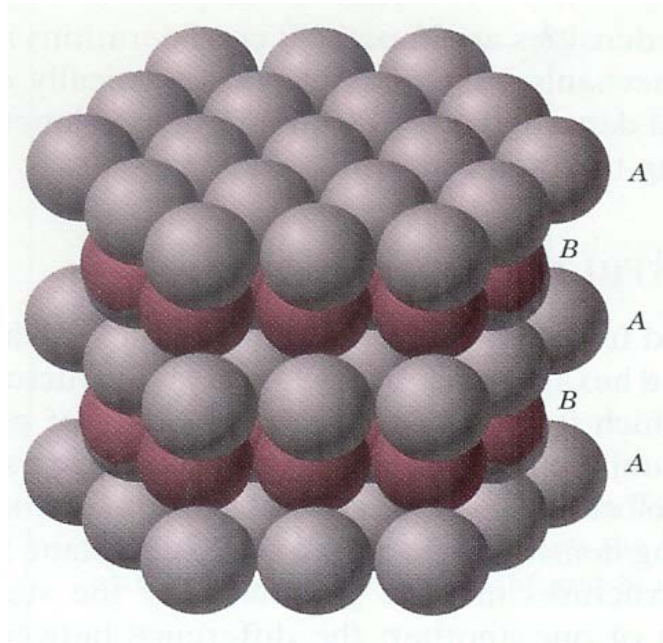
**Figure 2.4:** The first layer of atoms in a closed packed configuration. A, B, and C positions are indicated.

For the third close-packed layer, in the case of hexagonal system, centers of the atoms are aligned directly above the original *A* positions. This gives the stacking sequence of *ABA*, as shown in Fig. 2.5. When this is repeated over and over again we get the *..ABABAB...* sequence.



**Figure 2.5:** The AB stacking sequence for closed-pack atomic planes.

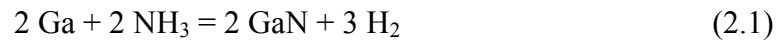
For GaN wurtzite crystal structure, the layer *A* represents both Ga and N atoms stacked on top of another in the *A* position, then Ga and N stacked on the B position, followed by Ga and N in A position (Fig. 2.6).



**Figure 2.6:** Close-packed plane stacking sequence for HCP structure.

## 2.1 Growth of Nitrides

GaN was first synthesized more than 50 years ago by Jhonson et al. [20] and by Juza and Hahn [21] by passing ammonia over hot gallium. The reaction is



This method produced small needles and platelets. It was in 1969 when Maruska and Tietjen [22] used chloride vapor transport technique to realize epitaxial large-area layer of GaN on sapphire. Since then epitaxial growth of GaN has seen many dramatic improvements. Regardless of the growth method employed, the major

difficulty in growing GaN and related alloys arises from having to incorporate stoichiometric quantities of nitrogen in the film. This is accomplished in vapor-phase processes at high substrate temperatures by decomposing a nitrogen containing molecule, such as ammonia, on the substrate surface. It can be also accomplished at lower temperatures in MBE growth by increasing the reactivity of nitrogen or ammonia through remote plasma excitation or ionization. For the nanowire growth, another critical issue is to kinetically promote anisotropic growth.

The first group ever to report the growth of GaN nanowires was by Han *et al.*, where they produced GaN–carbon composite nanorods by arc discharge in nitrogen atmosphere [23]. Over the past few years, various research groups have made significant progress in GaN nanowire growth. Although numerous variations of growth methods exist in the literature, GaN nanowire growth can be classified into these major categories:

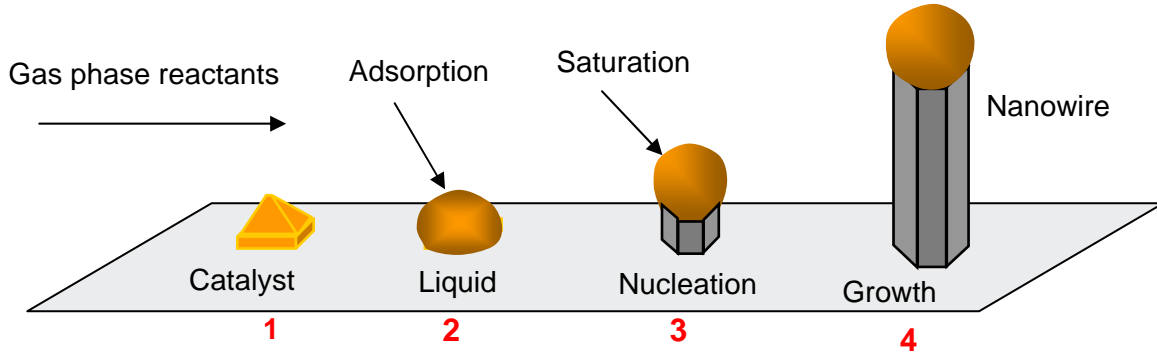
1. Laser assisted growth: Duan and Lieber were the first to report GaN nanowire growth by laser-assisted catalytic growth, where they obtained wurtzite phase single crystal GaN nanowires by laser ablation of Fe/GaN target [24]. Shi *et al.* showed a synthesis by 248 nm laser ablation of GaN powder mixed with gallium oxide ( $\text{Ga}_2\text{O}_3$ ) [25].
2. Chemical vapor deposition: Peng *et al.* synthesized the GaN nanowires from the reaction of Ga/ $\text{Ga}_2\text{O}_3$  mixture with  $\text{NH}_3$  using hot filament CVD [26]. He *et al.* grew GaN nanorods and nanowires by direct reaction of Ga vapor with flowing  $\text{NH}_3$  [27].

3. Anodic alumina template synthesis: Cheng *et al.* formed the GaN nanowires in anodic alumina membranes by the reaction of Ga/Ga<sub>2</sub>O<sub>3</sub> mixture with NH<sub>3</sub> [28].
4. Molecular beam epitaxy: Yoshizawa *et al.* grew self-organized nanocolumns on Al<sub>2</sub>O<sub>3</sub> substrates using radio-frequency radical source MBE. [29]

All the above-mentioned growth processes can be performed with or without a metal catalyst. It has been generally found that chemical vapor deposition technique usually results in nanowires growing along the a-axis of the wurtzite phase. Whereas the c-axis growth of GaN nanowires has been mainly achieved using MBE techniques. Presently, the growth mechanisms routinely employed to grow GaN nanowires and nanorods can be categorized into two main categories: a) Vapor-Solid-Liquid (VLS), b) Vapor-Solid (VS). In a VLS growth technique, growth proceeds from liquid metal catalyst [30], as shown in Fig. 2.7. Here one can envision the catalyst as a cluster that defines the diameter of the structure and localizes the reactants at the end of the growing nanowire. A nanometer sized metal catalyst is deposited on a suitable substrate with technique such as laser ablation, electrochemical deposition, thermal annealing, colloidal dispersion, etc. The liquid metal cluster serves as a preferential site for adsorption of reactants (i.e, there is a much higher sticking probability on liquid than solid surfaces) and, when supersaturated, the nucleation site for crystallization. Although VLS mechanism provides enormous advantage of controlling the diameter of the nanowires, it also introduces sources of contamination from the catalyst. On the other hand, the VS mechanism is free from catalysts, hence



results in better materials in terms of longer minority carrier lifetimes and less point defects.

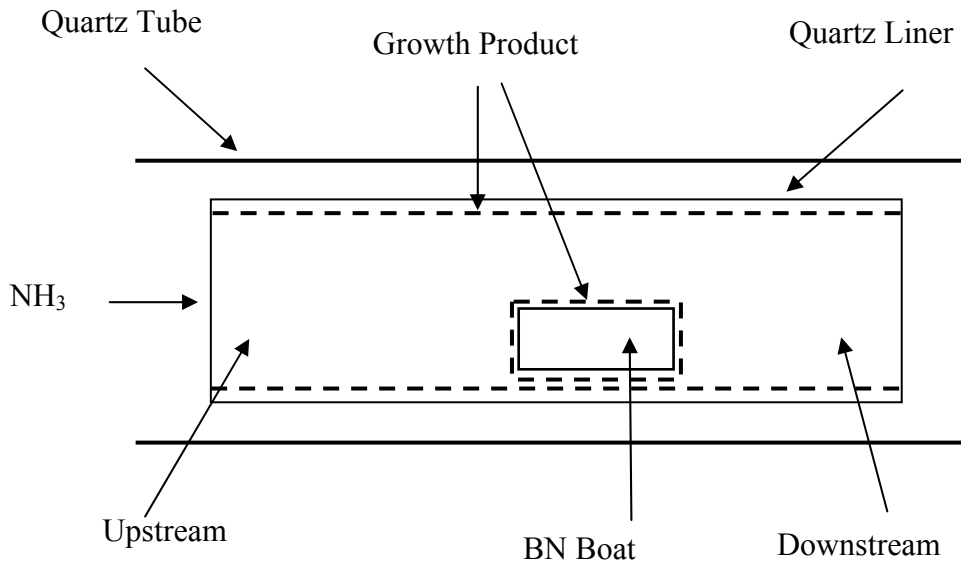


**Figure 2.7:** Schematic diagram representing growth steps in VLS growth mechanism.

## 2.2 Description of Catalyst Free Nitride Nanowire Growth

Free standing gallium nitride nanowires used in this study was grown by direct reaction of Ga vapor with ammonia ( $\text{NH}_3$ ), without the use of any metal catalyst. In this technique, nanowires are grown from direct reaction of Ga vapor with N supplied by decomposition of  $\text{NH}_3$  at high temperatures [27]. This vapor phase reaction results in solid phase GaN crystalline nanowires, hence it can be termed as Vapor-Solid or VS technique. Schematic diagram of the growth system is shown in Fig. 2.8. About 3 g of pure Ga (99.999%, metals basis, Alfa AESAR Inc.<sup>®</sup>) was put in a small boron nitride (BN) boat and placed at the bottom of a liner. The liner is made of boron nitride or quartz for collecting samples and protects the quartz tube of the oven from contamination during growth. A water-cooled Cu block was also put at the downstream end of the oven for sample collection. Ammonia (99.999%, MG Industries<sup>®</sup>) was introduced into the quartz tube through a mass-flow controller (MKS

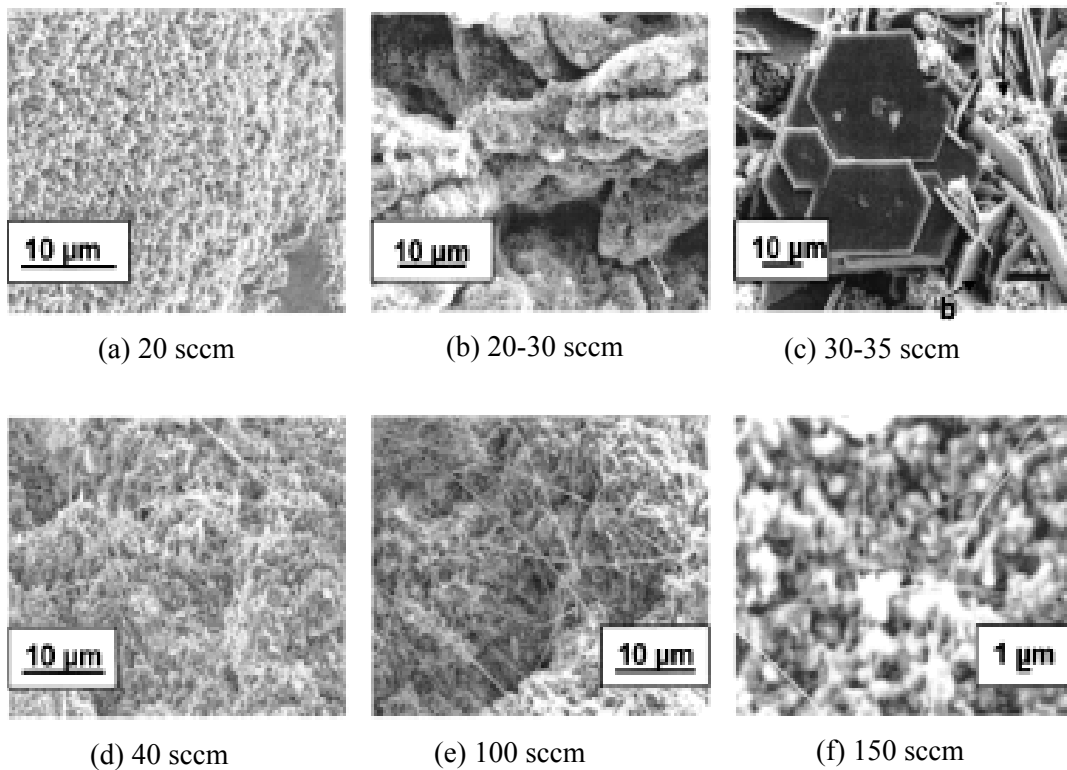
Instruments, Inc.<sup>®</sup>, model 1259B) at rates of 50–100 sccm (standard cubic centimeter per minute). During growth, the total pressure (mostly ammonia) upstream was kept at 15 Torr as measured by a capacitance manometer (MKS Instruments, Inc.<sup>®</sup>, model 220CA). The temperature of the oven (Sigma Inc.<sup>®</sup>, temperature program controlled) was set between 850 and 900 °C for 3–4 h to allow the GaN nanowires to crystallize.



**Figure 2.8:** Schematic diagram of the GaN nanowire growth system.

The overall reaction is given by  $2 \text{ Ga} + \text{NH}_3 = 2 \text{ GaN} + 3 \text{ H}_2$ , and one expects it to be influenced by availability of ammonia and Ga at the growth surface. Nanosized GaN crystals formed spontaneously without intentional nucleation in this experiment. At the end of the reaction, samples were collected from the walls of the BN boat, the liner, and the surface of the cooled Cu block for measurements. A series of experiments were conducted to study the effect of varying the NH<sub>3</sub> flow rate on the shape, size, and density of the nanowires [31]. Keeping the chamber pressure constant

at 15 Torr and the temperature at 900 °C, the NH<sub>3</sub> flow rate was varied between 20 and 150 sccm. At a flow rate of 20 sccm, only shiny Ga metal was detected [Fig. 2.9 (a)] As the NH<sub>3</sub> flow rate was increased to 30 sccm, some polycrystalline platelets were also produced as evident from Fig. 2.9(b), single crystal platelets with diameters of 20–40 nm began to appear at a flow rate of 30–40 sccm [Fig. 2.9 (c)]. This was clear evidence of the preferential formation of big platelets at lower NH<sub>3</sub> flow rates. GaN nanowires started growing only when the flow rate reached about 40 sccm.



**Figure 2.9:** Scanning electron microscope (SEM) images of nanowire growth matrix for different ammonia flow rates. (a) 20 sccm, (b) 20-30 sccm, (c) 30-35 sccm, (d) 40 sccm, (e) 100 sccm, and (f) 150 sccm.

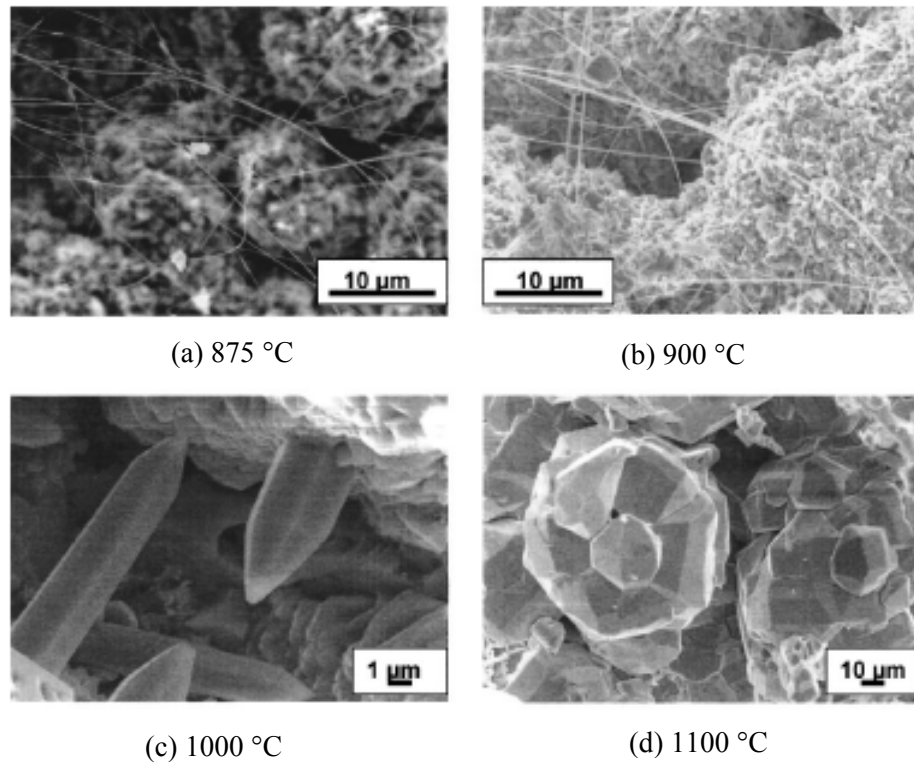
Figures 2.9 (d) and (f) show the SEM images of these nanowires grown in the flow rate range of 40 to 150 sccm. The wires had lengths up to several hundred

micrometers and diameters in the range of 80–300 nm. The same series of experiments were conducted by setting the temperature to 1000 and 1100 °C, respectively. Essentially the same growth pattern of GaN platelets was observed for lower flow rate, with the exception that one had to decrease the flow rate much lower than 30 sccm to obtain the GaN platelets. When we resorted to higher flow rate growth, microrods were the dominant products at a temperature of about 1000 °C, and micrograins were the dominant products at a temperature of about 1100 °C.

A series of experiments were also carried out to study the effect of varying the temperature on the shapes and sizes of the GaN products. These shapes and sizes of the growth products were found to change considerably on varying the temperature between 875 and 1100 °C, but keeping the NH<sub>3</sub> flow rate constant at 100 sccm and the chamber pressure at 15 Torr. GaN wires were grown between 825 and 875 °C with diameters of 20–130 nm, and between 875 and 950 °C with diameters of 80–300 nm. Nano- and mesowires grown at 875 and 900 °C are shown in Fig. 2.10(a)-(b). As the temperature was increased, the size increased, and microrods with diameters of 2–7 μm and lengths of 30–100 μm were produced at a temperature around 1000 °C [Fig. 2.10(c)]. As the temperature was increased further to about 1100 °C, the growth of three-dimensional micrograins set in [Fig. 2.10(d)]. The size of these micrograins was about 50–100 nm.

### **2.3 Growth Mechanism**

Unlike the VLS mechanism, the growth mechanism for VS is not as well understood. In case of VLS mechanism, the liquid metal catalyst droplets serve as the site for reactant species absorption.



**Figure 2.10:** Scanning electron microscope (SEM) images of nanowire growth matrix for different growth temperatures. (a) 875 °C, (b) 900 °C, (c) 1000 °C, and (d) 1100 °C.

Presence of metal droplets on the top of VLS grown nanowires indicate this fact. Absence of the Ga droplets on top of these nanowires indicates that a preferential diffusion is most probably responsible for the quasi-one dimensional growth. The growth process can be divided into three major steps:

(1) Initial stage: nearly amorphous Ga-rich GaN matrix formation

Once the temperature in the system exceeds 30° C the solid Ga becomes liquid and begins to diffuse over the surfaces of the BN boat and quartz liner forming a Ga layer. At higher temperatures, the Ga vapor pressure becomes significant. Ga vapor can adsorb onto, or desorb from the surface of the BN boat and quartz liner. Some NH<sub>3</sub> molecules adsorb on the Ga-coated surfaces where they can dissociate into N and H

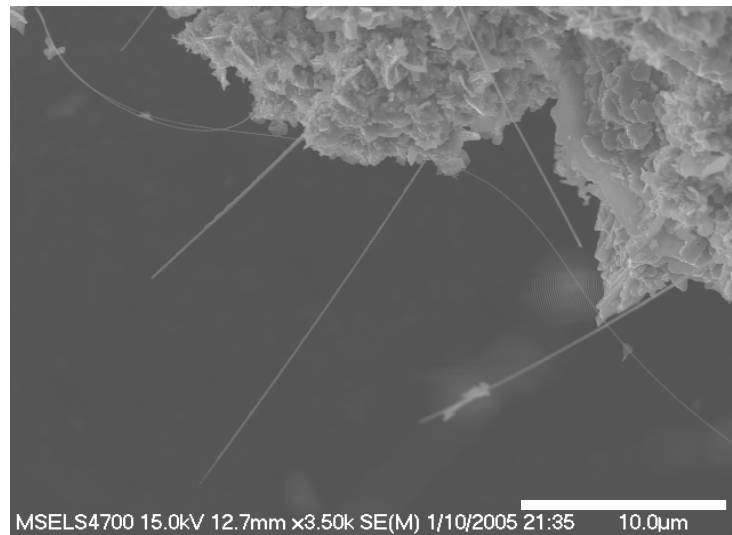
atoms [26,27] and some of the N atoms will react with Ga atoms to form GaN molecules. The surfaces of the BN boat and quartz liner do not have sites suitable for nucleation of GaN nanowires or crystals. Thus, it is not surprising that the matrix formed in the initial stage is nearly amorphous. However, the GaN matrix offers many sites favorable for formation of small crystal particles. Both the nearly amorphous GaN and the small crystal particles play important roles in the next growth stage.

(2) Second stage: formation of polycrystalline hillocks

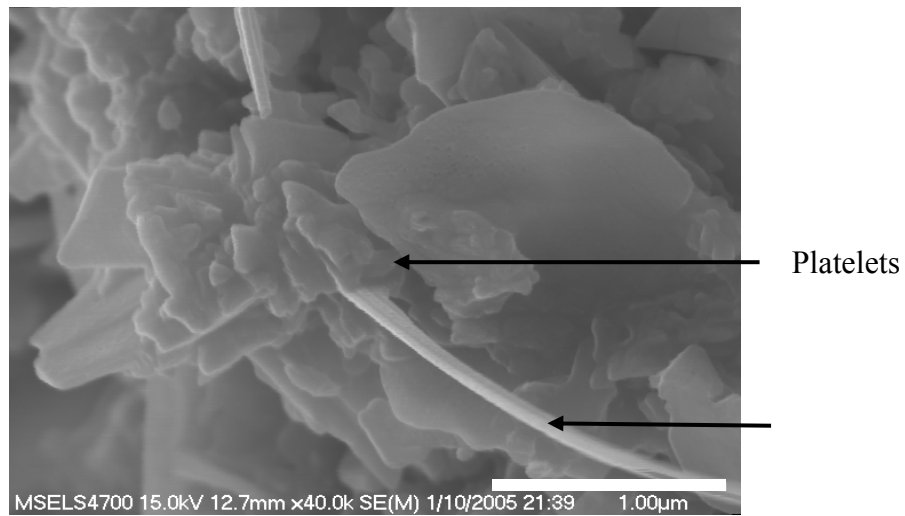
With time, the tiny crystals in the matrix grow into crystalline hillocks, which in turn are needed for nanowire growth. The SEM image in Fig. 2.11 shows how the hillocks and nanowires grow on the matrix. It is easier to see that the hillocks are built out of small, interconnected hexagonal crystal platelets of different sizes and orientations by looking at Fig. 2.11(b).

(3) Final stage: nucleation and growth of nanowires

Except at the highest temperatures used in this experiment growth of the crystal platelets in the [0001] direction is very slow. Mostly, the plates grow from the edges out or by formation of additional thin platelets on top of older ones or at other sites on the matrix. It is possible at the optimum growth temperatures (875 – 900 °C) and III-V ratio (NH<sub>3</sub> flow rate 40 – 100 sccm) Ga diffusion length is longer so that Ga can move from the basal plane to the side facets. For appropriate growth temperatures side facets of these crystalline platelets serve as nucleation sites for the nanowire growth.



(a)



(b)

**Figure 2.11:** (a) Field emission SEM (FESEM) scans of growth matrix after collecting from the growth chamber. (b) FESEM scans of nanowires growing from the edges of the GaN platelets.

Probably at these temperatures and III-V ratios the growth along the a-direction is much faster than the c-direction growth. The growth is most likely effected by the supply of N atoms at the surface and diffusion lengths of Ga.

## **2.4 Characterization of GaN Nanowire**

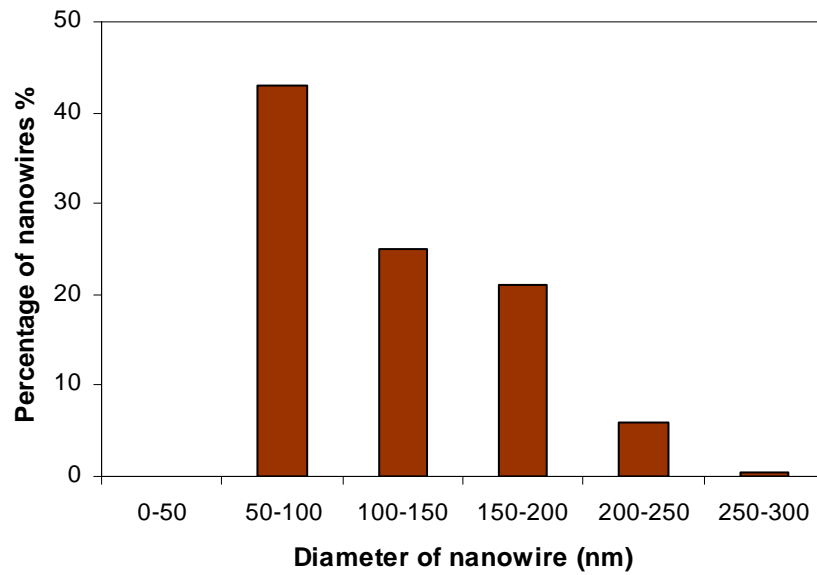
Detail characterizations including structural and material properties have been carried out after the completion of the growth. These characterizations are an important aspect of device realization as it gives us indications of the material quality, defects, and growth mechanisms. This is important for estimating device performances, and in turn improving the materials quality.

### **2.4.1 Field Emission Scanning Electron Microscopy**

In order to quantify the effectiveness of the growth method, it is important to study the statistical distribution of the diameters and structural nature of the nanowires in a growth matrix. A low resistivity Si sample was prepared with nanowires dispersed on it. Dispersion was obtained by sonication of the growth product in isopropanol, forming a suspension of the nanowires. Using FESEM, the diameters of 100 nanowires were measured at different parts of the sample. Figure 2.12 is the diameter distribution as observed on the growth matrix used for this study. It is quite clear that majority of the nanowires had diameters in the range of 50 nm to 100 nm. Only few nanowires were observed with diameters in excess of 200 nm.

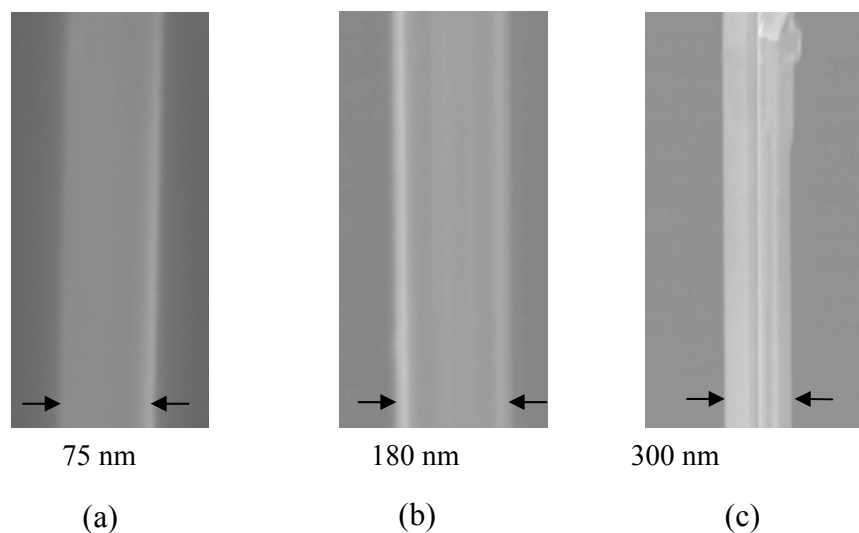
It was interesting to note that the structural quality of the nanowires showed significant variations with their diameters. As shown in Fig. 2.13(a), the nanowires with diameters in the range of 50 nm to 100 nm had circular cross-sections with no observable defects. For nanowires with diameter above 150 nm [Fig. 2.13(b)], the defects in their structure are clearly visible in SEM scans. Larger diameter nanowires [Fig. 2.13(c)] represented a bundle of several crystals featuring similar growth direction parallel to the wire axis.





**Figure 2.12:** Diameter distribution of nanowires as observed in the growth matrix.

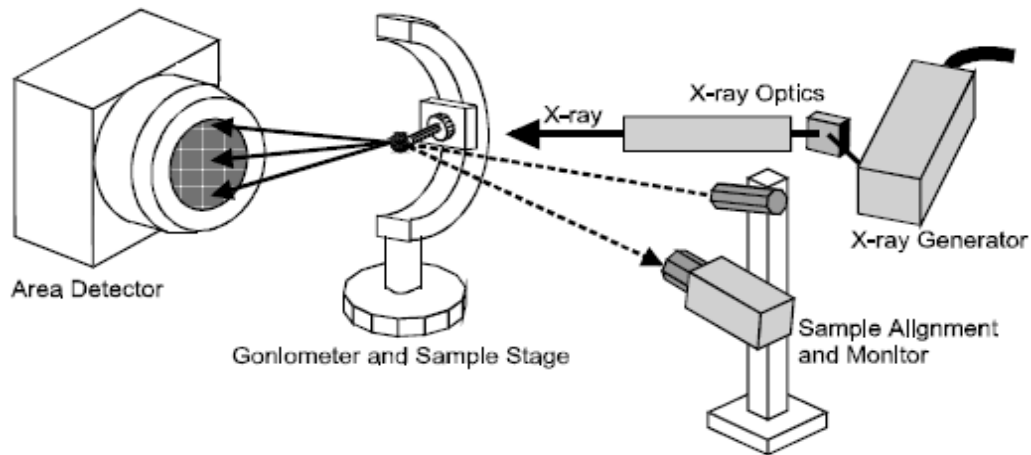
The complex crystallography exhibited by these multiple crystal assemblages within the individual nanowires are of significant importance, as will be discussed later.



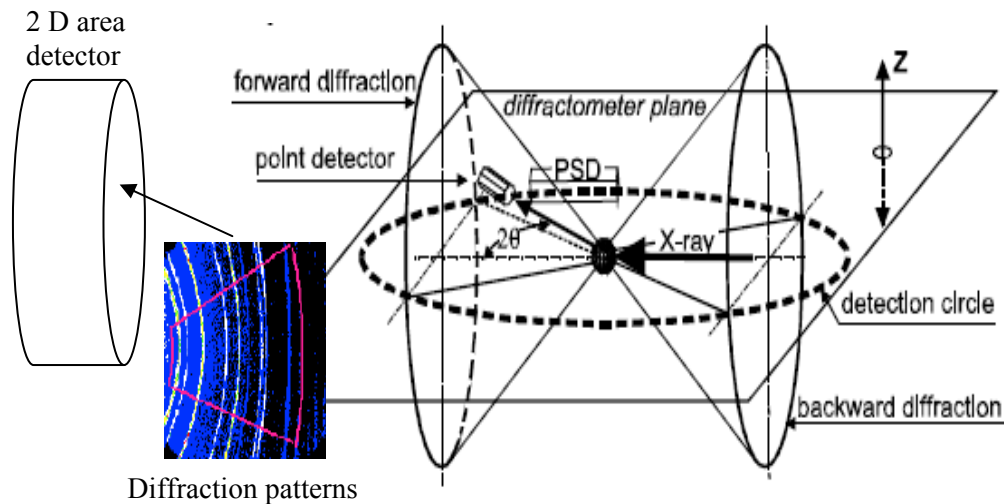
**Figure 2.13:** Representative structural characteristics of nanowires observed in different diameter ranges (a) 50 nm – 100 nm, (b) 150 nm – 200 nm, (c) 250 nm – 300 nm. Diameters of the nanowires are indicated below.

## 2.4.2 X-ray Diffraction

Two-dimensional x-ray diffraction (2D XRD) refers to x-ray diffraction applications with two dimensional (2D) detector and corresponding data collection and analysis. A two-dimensional x-ray diffraction system consists of two-dimensional detector, x-ray source, x-ray optics, sample positioning stage, sample alignment, and monitoring device (Fig. 2.14) [32]. The diffraction pattern from a polycrystalline (powder) sample forms a series of diffraction cones if large number of crystals, oriented randomly in the space, are covered by the incident x-ray beam (Fig. 2.15). Each diffraction cone corresponds to the diffraction from the same family of crystalline planes in all the participating grains. A point detector makes  $2\theta$  scan along a detection circle. With a 2D detector, the measurable diffraction is no longer limited in the diffractometer plane. Instead, the whole or a large portion of the diffraction rings can be measured simultaneously, depending on the detector's size and position. This greatly enhances the resolution and reduces data acquisition time. A 2D area diffraction scan can be integrated in  $\chi$ - direction to give general  $\theta$ - $2\theta$  scan.

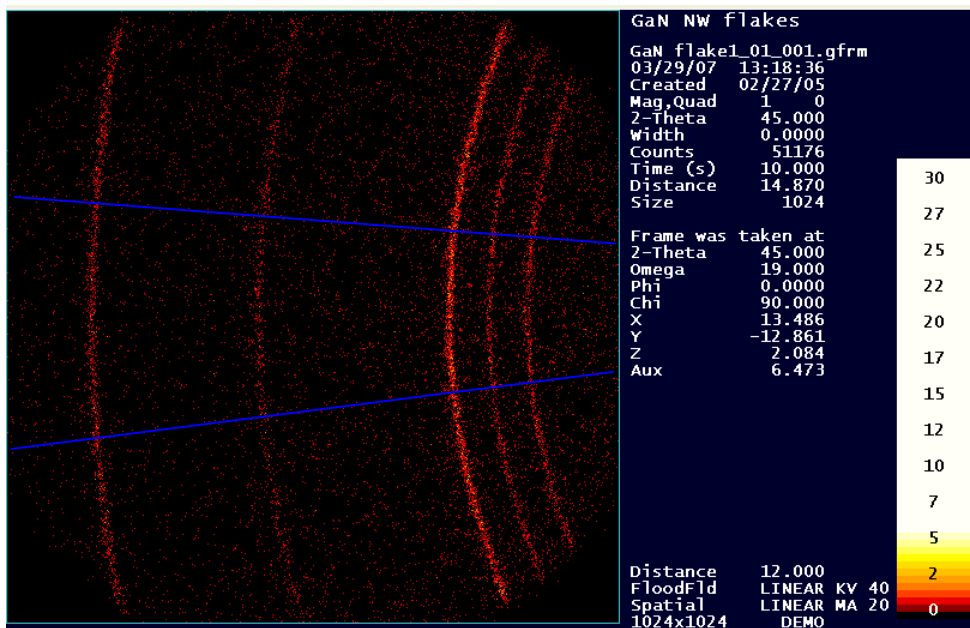


**Figure 2.14:** The schematic representation of a typical 2D XRD system.

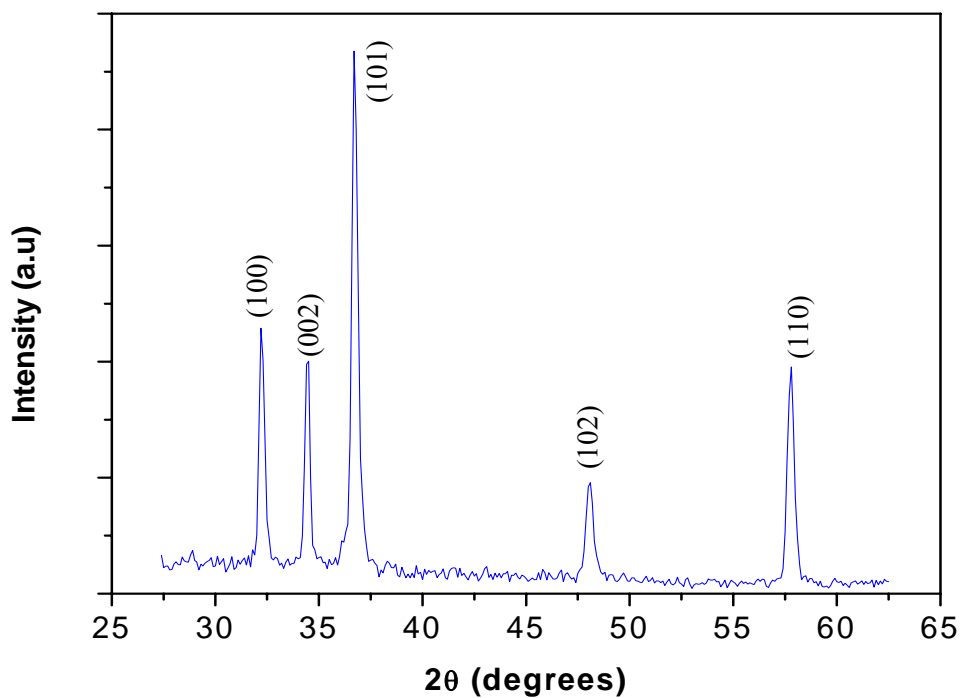


**Figure 2.15:** The diffraction pattern from a polycrystalline sample. The intercepts of the diffraction cones by the 2 D detector are visible as arc on the detector plane.

A Brukeraxs<sup>®</sup> D8 2D diffractometer was used with GADDS<sup>®</sup> data acquisition software to obtain 2D x-ray diffraction from GaN flakes with the nanowires (Fig. 2.16). As expected, arcs corresponding to different crystallographic planes are seen in the diffraction. As the nanowires and platelets are randomly oriented, diffraction from same family of planes in all the platelets and the nanowires give rise to a diffraction cone. Integrating the diffraction spectrum in chi direction resulted in the  $\theta$ - $2\theta$  scan, where peaks associated with respective crystal planes of the flake are shown. Using JADE<sup>®</sup> software these peaks can be matched to that of GaN powder diffraction spectra. The peaks associated with different lattice plane of GaN wurtzite structure is shown in Fig. 2.17.



**Figure 2.16:** The 2D area diffraction pattern from GaN flake with nanowires on Brukeraxs<sup>®</sup> D8 2D diffractometer. The blue lines indicate the chi direction integration.

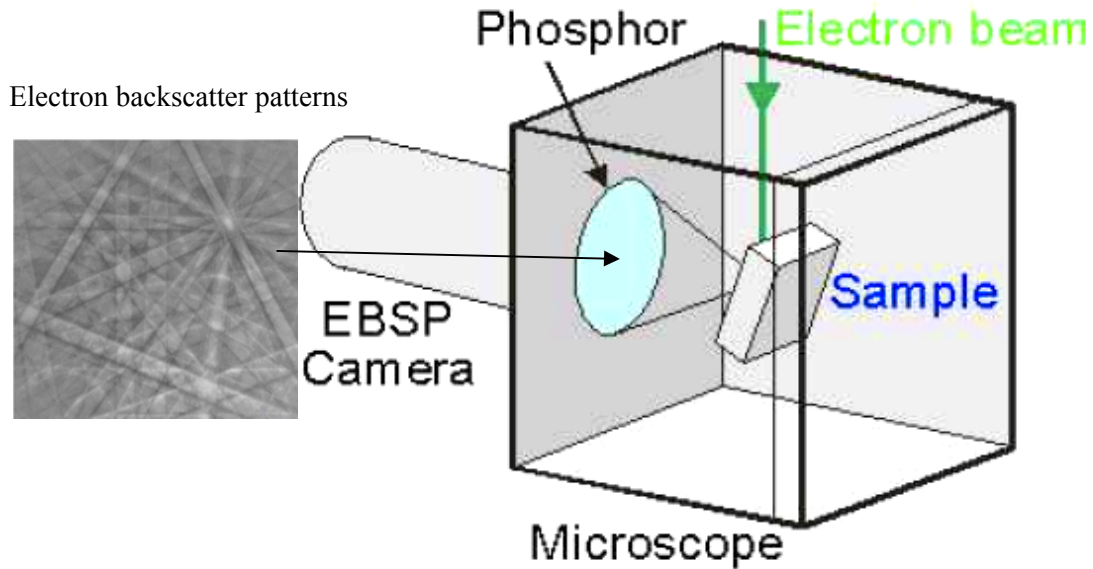


**Figure 2.17:** The  $\theta$ -2 $\theta$  diffraction of the flake after integrating the 2D spectrum in the chi direction (shown by blue lines in Fig. 2.16).

### 2.4.3 Electron Backscattered Diffraction

Electron backscatter diffraction (EBSD), also known as backscatter Kikuchi diffraction (BKD) is a microstructural crystallographic technique used to study the crystallographic texture or preferred orientation of any crystalline or polycrystalline materials. EBSD can be used to index and identify the seven crystal systems, and as such it is applied to crystal orientation mapping, defect studies, phase identification, grain boundary and morphology studies. Experimentally EBSD is conducted using a scanning electron microscope (SEM) equipped with a backscatter diffraction camera (Fig. 2.18). The diffraction camera is essentially a focal plane CCD coupled with a phosphor screen, which is inserted into the specimen chamber of the SEM at an angle greater than or equal to  $90^\circ$  to the pole piece. The specimen is placed into the normal position in the specimen chamber, but is highly tilted ( $\sim 70^\circ$  from horizontal) towards the diffraction camera. When the electrons impinge on the specimen they interact with the atomic lattice planes of the crystalline structures, many of these interactions satisfy Bragg conditions and undergo backscatter diffraction. Due to the angle of the specimen these diffracted electrons are directed towards and impinge upon the phosphor screen of the diffraction camera causing it to fluoresce, this fluorescent light is then detected by the CCD. The diffracted electrons form an image termed a diffraction pattern on the diffraction camera called electron backscatter diffraction pattern (EBSP). This pattern is unique to the microstructural-crystallographic properties of the material. Using computer aided interpretation reveal crystal structure and crystal orientation. Each diffraction pattern will show several intersecting lines termed Kikuchi bands, these correspond to each of the lattice diffracting planes and

can be indexed individually by the Miller indices of the diffracting plane which formed it [33].

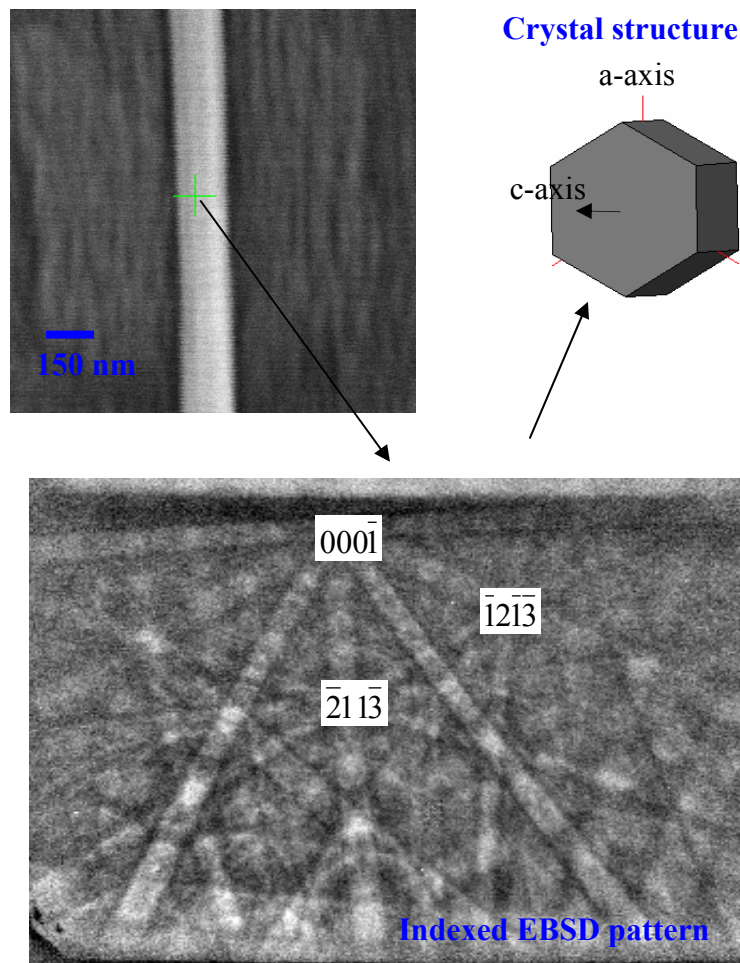


**Figure 2.18:** The schematic representation of an EBSD system. The technique is carried out inside an SEM chamber.

The formation of an EBSP can be described as follows:

- a) The electrons strike the specimen, and within the pattern source point (PSP) they are inelastically scattered, losing  $\sim 1\%$  of their energy.
- b) These scattering events generate electrons travelling in all conceivable directions in a small volume which is effectively a point source.
- c) Electrons that satisfy the Bragg diffraction condition for a particular plane are channeled differently to the other electrons - thus producing a change in intensity.
- d) For each crystallographic plane, these electrons form two cones (with large semi-apical angles of  $90^\circ$  - Bragg angle, i.e. almost flat discs) that intersect the imaging plane (phosphor) as hyperbolae.

In the Fig. 2.19 the indexed EBSD pattern from a nanowire is shown. The important zone axes are shown on the pattern. The crystal structure solution generated by the software analyzing the pattern is shown in the right. The growth direction is along the axis of wurtzite structure, which is also confirmed by the TEM. The c direction is normal to the surface as indicated in the solution.

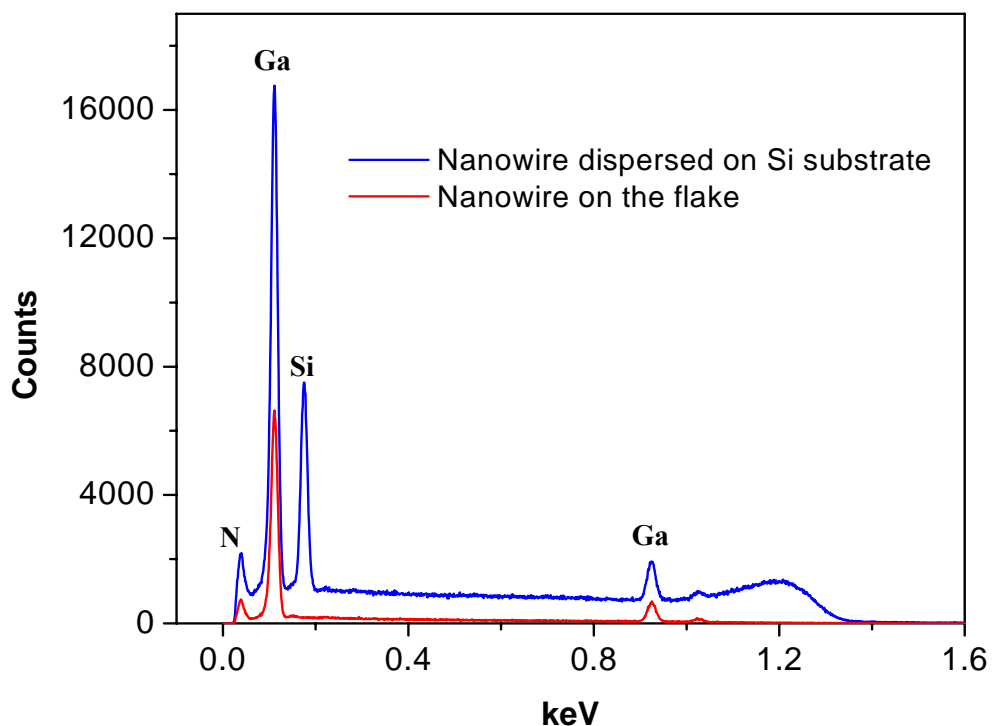


**Figure 2.19:** EBSD pattern from a GaN nanowire (shown in the top). Important zone axes are pointed. The crystal structure solution is shown on the right hand side

#### **2.4.4 Energy Dispersive X-ray Analysis**

Energy Dispersive Spectroscopy (EDS) is a standard procedure for identifying and quantifying elemental composition of sample areas as small as a few cubic micrometers. The characteristic x-rays are produced when a material is bombarded with electrons in an electron beam instrument, such as a scanning electron microscope (SEM). Detection of these x-rays can be accomplished by an energy dispersive spectrometer, which is a solid state device that discriminates among x-ray energies [34]. The detector used in EDX is the Lithium drifted Silicon detector. When an x-ray photon strikes the detector, it will generate a photoelectron within the body of the Si detector. As this photoelectron travels through the Si, it generates electron-hole pairs. The electrons and holes are attracted to opposite ends of the detector with the aid of a strong electric field. The size of the current pulse thus generated depends on the number of electron-hole pairs created, which in turn depends on the energy of the incoming x-ray. Thus, an x-ray spectrum can be acquired giving information on the elemental composition of the material under examination. Figure 2.20 shows an EDX spectrum from a nanowire dispersed on a Si substrate, and from a nanowire attached to the growth matrix. Both the curves are similar except for the Si peak in the case of dispersed wire which is generated by the Si substrate. This elemental analysis confirms the presence of Ga and N in the nanowires and no other elements with significant volume fractions.



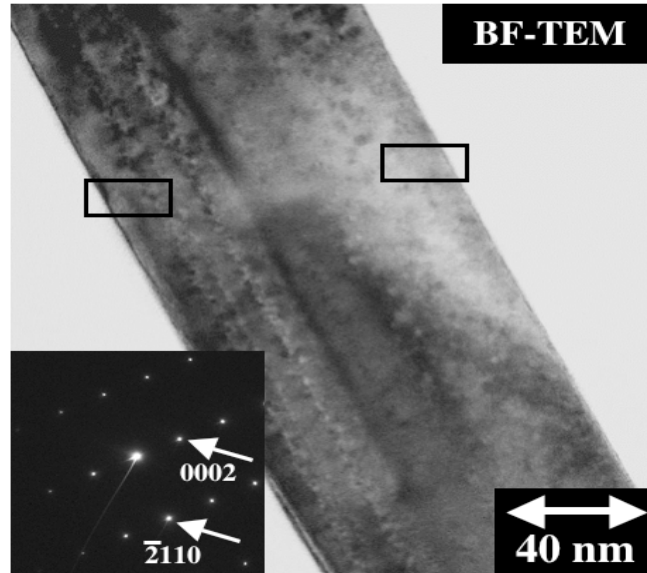


**Figure 2.20:** EDX spectra from GaN nanowires. The red curve is from nanowire on the flake and the blue is from nanowire dispersed on a Si substrate.

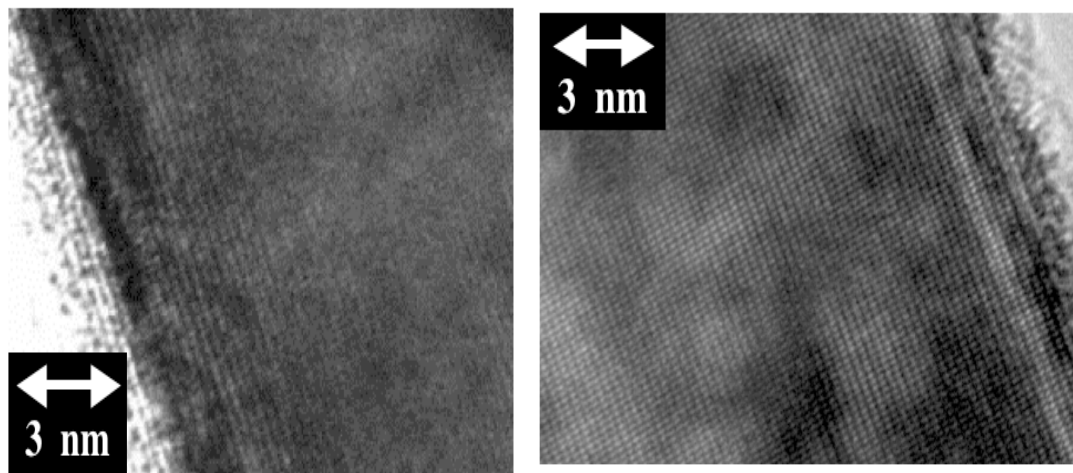
#### 2.4.5 Transmission Electron Microscopy

A transmission electron microscope (TEM, FEI CM300-FEG<sup>®</sup>) was used to determine the crystal structure, growth direction and the extent of defects in the wires. Nanowires were dispersed on a holey carbon grid from suspension in isopropanol. A double tilt holder was used to tilt nanowires  $\pm 30^\circ$  in two orthogonal directions in order to establish the actual flat direction for each nanowire. Once this orientation was established, the nanowires were rotated about their long axis of growth until crystallographic zone axes of low indices were achieved. Figure 2.21 represents such

a double-tilted condition for a  $\sim 100$  nm diameter wire, and presents data acquired at the  $[0\bar{1}10]$  zone axis.



(a)

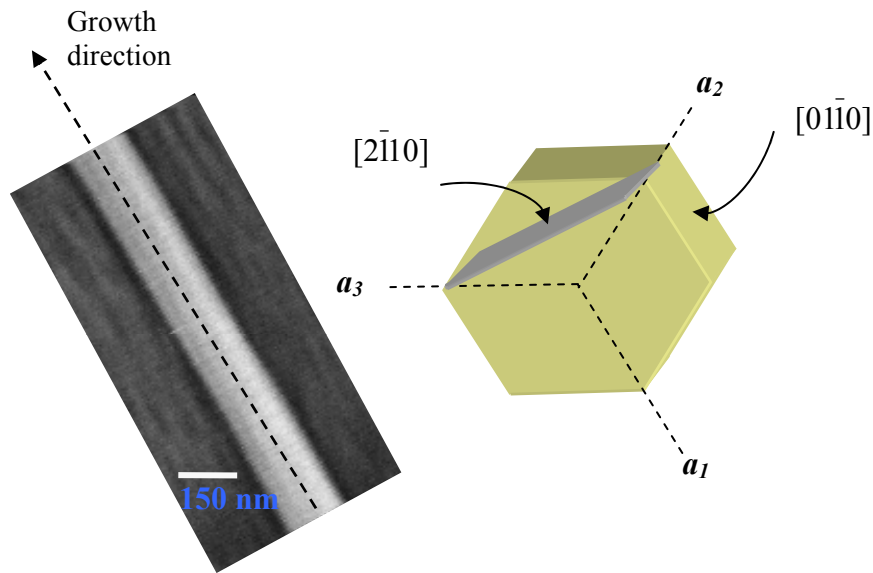


(b)

(c)

**Figure 2.21:** (a) Bright-field TEM image of GaN nanowire acquired at the  $[0\bar{1}10]$  zone axis, (inset) selected area diffraction (SAD) pattern acquired with an effective aperture of  $\sim 200$  nm, (b) and (c) high-resolution lattice images (HR-TEM) acquired of the left and right sides, respectively, of the crystal as marked in (a).

Figure 2.21(a) is a bright field image (BF-TEM) across the wire diameter. Figure 2.21(a) inset is selected area diffraction (SAD) pattern acquired with an effective aperture of  $\sim 200$  nm, thereby ensuring diffraction data across the entire nanowire diameter. The singular nature of the pattern suggests it may be indexed as a single crystal, with the long growth axis of the crystal aligned with the  $[\bar{2}110]$  direction. The growth direction of the nanowire as interpreted from TEM images is illustrated in Fig 2.22.



**Figure 2.22:** Growth direction of nanowire as explained by the hexagonal structure, with  $c$  axis pointing out the plane of the paper. The  $a$ -plane ( $2\bar{1}10$ ) is denoted by the gray line, and the nanowires grow normal to that plane.

Figures 2.21(c) and (d) are high-resolution lattice images (HR-TEM) acquired of the left and right sides, respectively, of the crystal. To a first approximation the HR-TEM also may suggest a single crystal across the entire diameter. One major difference between thin film growth and nanowire growth is that former usually takes place on  $c$  direction  $[0001]$ , where as the later is shown to be growing along the  $a$  direction.

## 2.4.6 Polarization-resolved Photoluminescence Spectroscopy

In a conventional photoluminescence (PL) spectroscopy, a sample is excited with a monochromatic optical source (typically a laser with  $h\nu > E_g$ ), generating electron-hole pairs that recombine by one of the several mechanisms: band-to-band recombination, free exciton recombination, bound exciton recombination, and defect related recombination. For the case of polarization-resolved photoluminescence measurements, the emitted spectra can be polarized with the direction of the electric field vector  $E$  parallel or perpendicular to the  $c$  direction of the wurtzite structure.

The nanowire samples were placed in a continuous-flow cryostat that enabled close optical access, and stable sample temperatures from 2.8 to 296 K. Samples were excited with a continuous-wave HeCd laser operating at 325 nm (3.815 eV) that was focused with a singlet lens to a spot diameter of 4  $\mu\text{m}$ . PL spectra were collected with a 0.5-m monochromator that dispersed the photoluminescence onto an UV-sensitive photomultiplier tube [35]. The nanowires mounted in the cryostat were imaged indirectly in phase contrast and their axial orientation was determined. With the wire axial orientation determined, an UV polarizer placed at the entrance slit of the monochromator was then oriented to select PL conforming to either the  $E$  parallel or perpendicular to the growth axis of the nanowire. The PL spectrum collected at 3 K is shown in Fig. 2.23. If the growth direction was along the  $c$  axis, then  $E \parallel c$  and  $E \perp c$  spectrum would be different. This polarization anisotropy results from dipole-forbidden nature of polariton generation from A excitons for the  $E \parallel c$  -polarization case and are expected in ideal wurtzite crystals [36]. It is clear from the spectra that changing the polarization from  $E$  parallel to the wire axis to  $E$  perpendicular does not

cause a change in the PL spectrum. This independently verifies that the growth direction is along the  $a$ -axis, as for an  $a$ -axis nanowire the  $c$ -direction can not be determined un-ambiguously. The peak emission at 3.466 eV corresponds to the strain free acceptor and donor bound A excitons (3.466 and 3.472 respectively). Due to their broad linewidths it is difficult to resolve them.

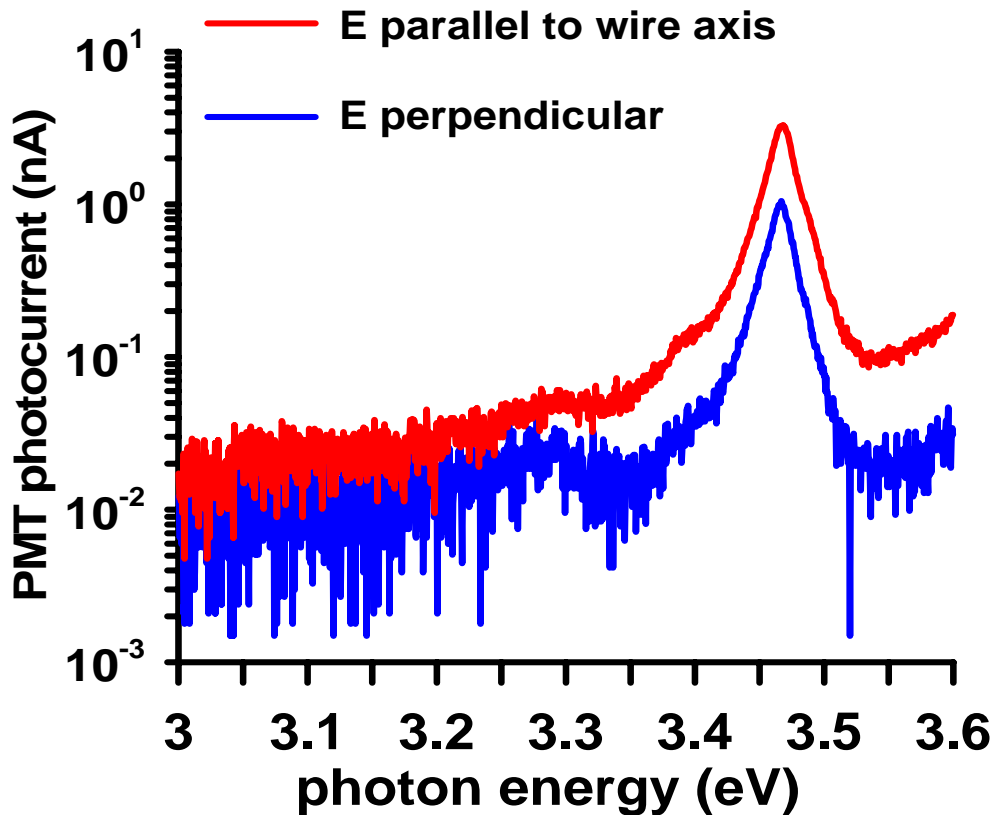
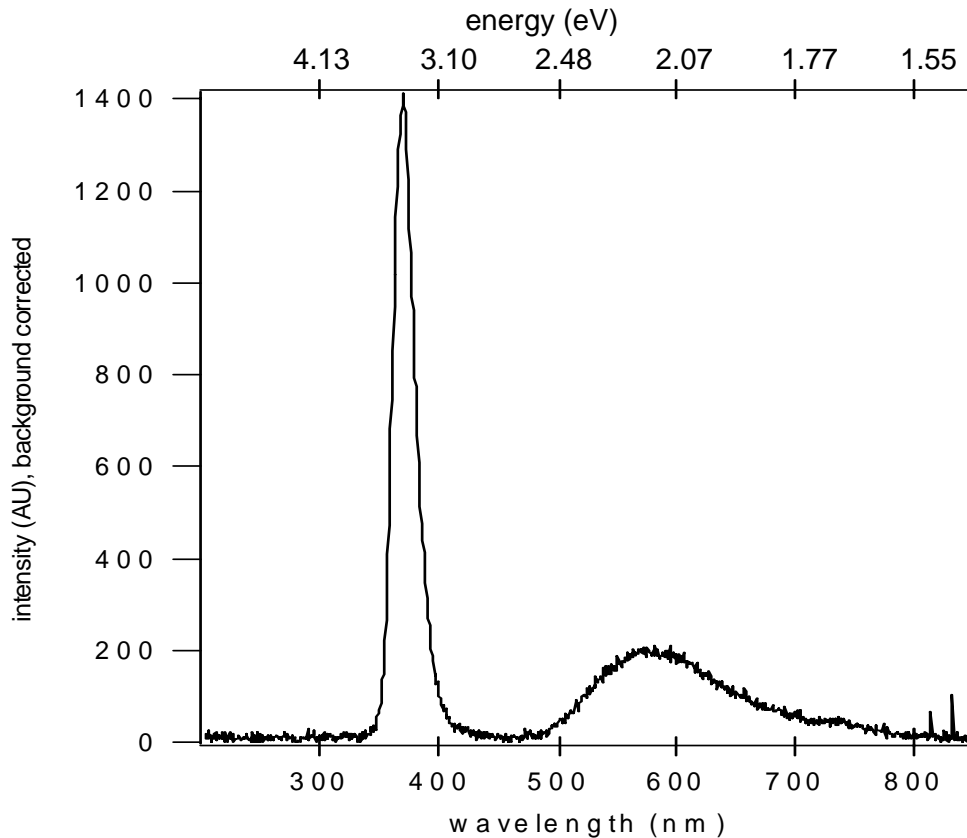


Figure 2.23: Polarization-resolved PL of a GaN nanowire at 3 K.

#### 2.4.7 Cathodoluminescence Spectroscopy

Scanning electron microscopy was used for imaging, cathodoluminescence (CL) characterization. The nanowires were excited by 10 kV electrons with a nominal beam current of  $15 \pm 3$  nA. Electron-induced optical signals were collected with a 5

mm collimating lens positioned  $\sim 20$  mm from the sample during excitation and transported out of the SEM vacuum chamber to a cooled spectrometer with UV-visible optical fibers. Light analyzed by the spectrometer was generated by the entire nanowire and substrate volume directly or indirectly excited by the electron beam. Background-subtracted signal was integrated for 60 s during every measurement. CL spectrum for a GaN nanowire is shown in Fig 2.24. The narrow peak at 370 nm is due to excitonic transitions; the broad peak centered at 575 nm is produced by defect-related processes [37].



**Figure 2.24:** CL spectrum from a GaN nanowire at 300 K. The narrow peak at 370 nm ( $\sim 3.39$  eV) is associated with excitonic transitions in GaN, while the much broader peak centered at 575 nm (2.2 eV) is due to defect-related emission processes.

## **Chapter 3: Focused Ion Beam Assisted Fabrication of Nanowire Devices**

The first step towards realizing electronic or optoelectronic devices from nanowires is the formation of reliable metal contacts to the nanowires (both ohmic and Schottky). Thin film characterization techniques such as hall measurements, mercury probe, four-probe measurements are not easily applicable to these nanowires. Thus, in order to assess the material properties, it is also essential to fabricate simple devices such as FETs, 4-T resistivity measurement structures. Forming reliable electrical contacts to nanowires pose significant challenges.

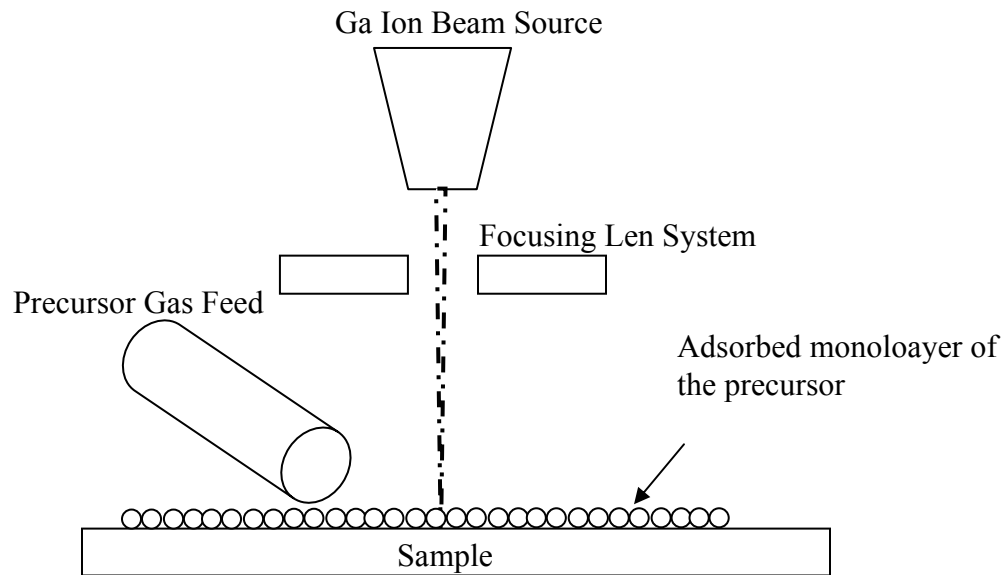
Although significant progress has been made in semiconducting nanowire growth [27], [38], [39], further optimization of the growth processes is still required. Positioning them on a suitable substrate for device fabrication often involves complex aligning procedures such as electric field assisted aligning [40], micro-fluidic aligning, and chemical patterning [41]. These procedures are time consuming and require elaborate substrate pre-patterning. Perfecting these alignment techniques is necessary in order to realize hierarchical assembly for large-scale nano-system development. However, for growth optimization and study of transport properties of individual nanowires, versatile fabrication methods suitable for random nanowire orientations are quite useful.

In this chapter we have demonstrated that by utilizing focused ion beam (FIB) induced metal deposition techniques, we can fabricate simple nanowire devices and extract material properties of individual GaN nanowires, such as resistivity and electron mobility, without elaborate alignment and fabrication techniques. This

chapter focuses on the viability of FIB metal deposition technique for rapid prototype device structure fabrication using GaN nanowires.

### 3.1 Focused Ion Beam Induced Metal Deposition Technique

The construction and operation of a focused ion beam (FIB) system is very similar to a scanning electron microscope except the fact that former uses typically a focused Gallium ion beam derived from a liquid metal ion source (LMIS) to perform various functions such as imaging, ion induced localized sputtering, and material deposition. This technique is maskless and enables us to deposit material including metals such as platinum and aluminum on predetermined patterns. The simplified block diagram of a FIB system is shown in Figure 3.1, where  $\text{Ga}^+$  ion beam is accelerated and focused on a substrate by a suitable lens assembly.



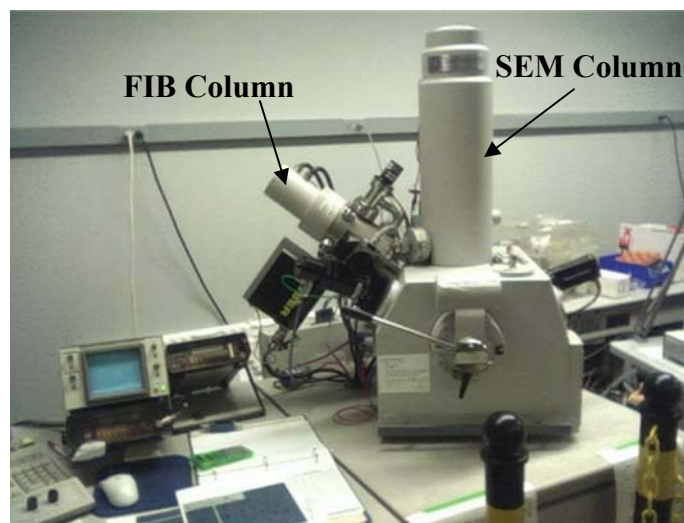
**Figure 3.1:** Schematic diagram of focused ion beam (FIB) system.



FIB induced deposition is a three step procedure: a) precursor gas is adsorbed on to the surface forming a monolayer, b) energetic Ga<sup>+</sup> ions dissociate the precursor gas via collision cascade energy transfer process leaving non-volatile material deposited on the substrate, and c) the volatile reaction products are desorbed and removed by the vacuum pump.

### 3.2 Experimental Details

After completion of the growth, the GaN matrix with nanowires was collected from the inner lining of the furnace, and then sonicated in isopropanol to achieve a dilute suspension of nanowires. The suspension was then dispersed on SiO<sub>2</sub> (150 nm thick) coated Si substrate (p<sup>++</sup>,  $\rho = 0.5\Omega \cdot \text{cm}$ ) with pre-defined Cr/Au pads. Locations of the nanowires with respect to the pads were noted with an optical microscope. A dual beam FEI 620 FIB/SEM tool (Fig. 3.2) was used with (Trimethyl)methylcyclopentadienyl-platinum (STREM Chemicals<sup>®</sup> 99 %) as an organometallic precursor to deposit Pt contacts to these nanowires.



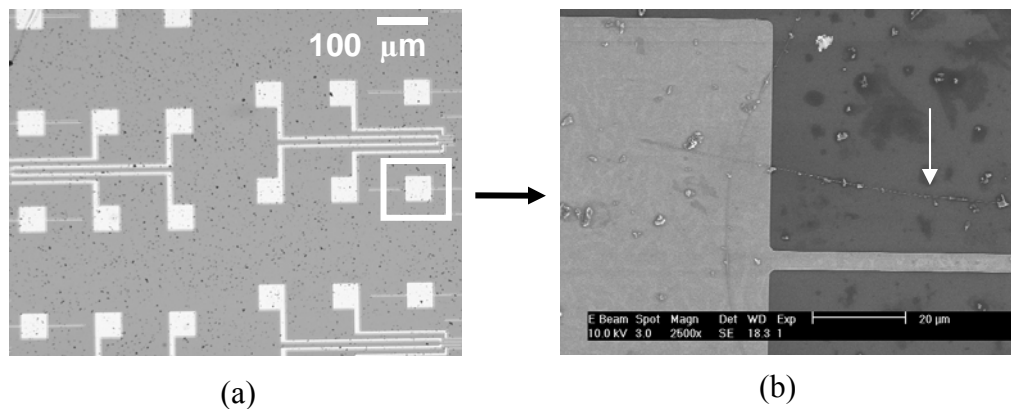
**Figure 3.2:** FEI 620 Dual Beam (FIB/SEM) system.

A 30 KeV Ga<sup>+</sup> ion beam was used with 7 pA current aperture during ion beam deposition. It was observed that using higher current apertures causes significant sputtering of the nanowires before metals start depositing. Dwell time and overlap for the Ga<sup>+</sup> ion beam were 0.4 μs and 0 % respectively. Using these deposition parameters, Pt contacts with nominal dimensions of 2 μm in width, 20 μm in length, and approximately 1 μm in height were routinely deposited.

In order to achieve linear I-V characteristics, the FIB-deposited Pt contacts were annealed at 500 °C for 30 s in UHP-grade argon using a rapid thermal annealing furnace. I-V characteristics of the GaN nanowire were measured using a HP4140B picoammeter. A Keithley 238 source measure unit was used to measure the four terminal resistivity of the nanowire. Schottky diode to GaN nanowire was realized by using as-deposited Pt contact. The Ohmic contact for the diode was formed by annealing another Pt contact, which was FIB-deposited prior to the Schottky contact. The barrier height and ideality factor for the diode were extracted from the I-V characteristics. MOSFET type of transistor action was obtained from individual GaN nanowire with source and drain contacts formed by annealed FIB Pt contacts and Si substrate as the global backgate. A Hitachi S4700 Field emission Scanning electron microscope (FESEM) was used to study the morphology of the metal-nanowire contact region. Simulation of 30 KeV Ga<sup>+</sup> ions impinging on GaN nanowires was carried out using SRIM 2003 [42] software to study the interaction of Ga<sup>+</sup> ions with the nanowire. Electron beam induced deposition of Pt on nanowires was carried out using the same dual beam FEI system to investigate the effect of heating in the nanowires under the charged particle beams.

### 3.3 Results

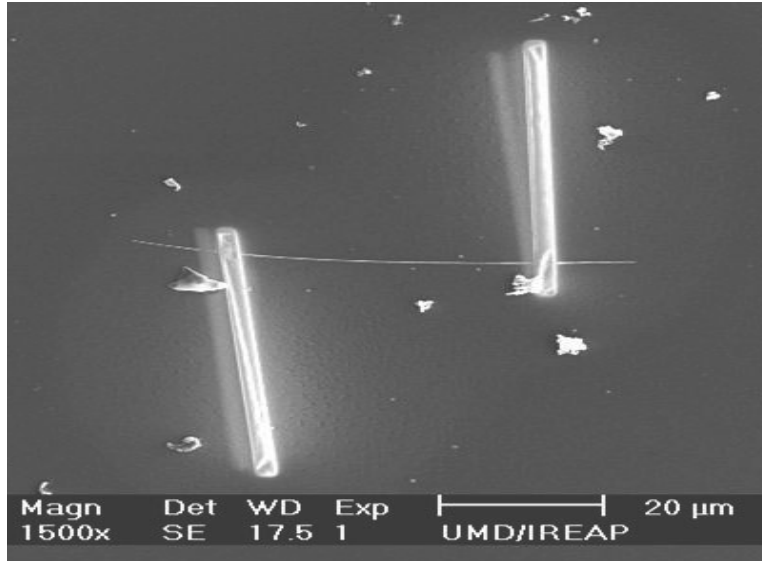
After sonication and dispersion of the nanowires on the pre-patterned substrates, the nanowires were found to have a tendency to lie on or close to the metal pads as shown in Fig. 5. We can speculate that this was due to the difference in the evaporation rates of the solvent over the pad and the SiO<sub>2</sub> substrate, which causes the wires to deposit close to the pads.



**Figure 3.3:** (a) Optical image of pre-patterned substrate with Cr/Au patterns. (b) SEM image of nanowires dispersed close to the pads (indicated with a white arrow).

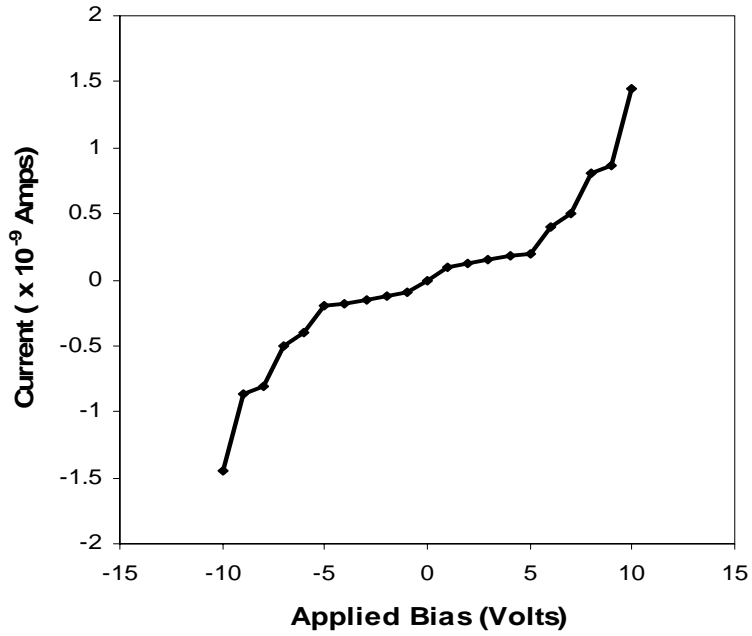
Alternatively the surface charges of the nanowires can give rise to image charges inside the metal, hence creating an electrostatic force of attraction between the metal and the nanowire. After the nanowire lands on the pad and the solvent dries out, Van der Waals forces might hold the nanowires to the substrate.

After dispersion of the nanowires, the FIB was used to deposit Pt pads to contact these nanowires. Figure 3.4 shows a single nanowire contacted at the ends using two FIB-deposited Pt lines. Current-voltage characteristics of the nanowire measured using the as-deposited Pt contacts were non-linear, with current level in range of  $1.5 \times 10^{-9}$  A for 10 V bias as shown in Fig. 3.5 (a).

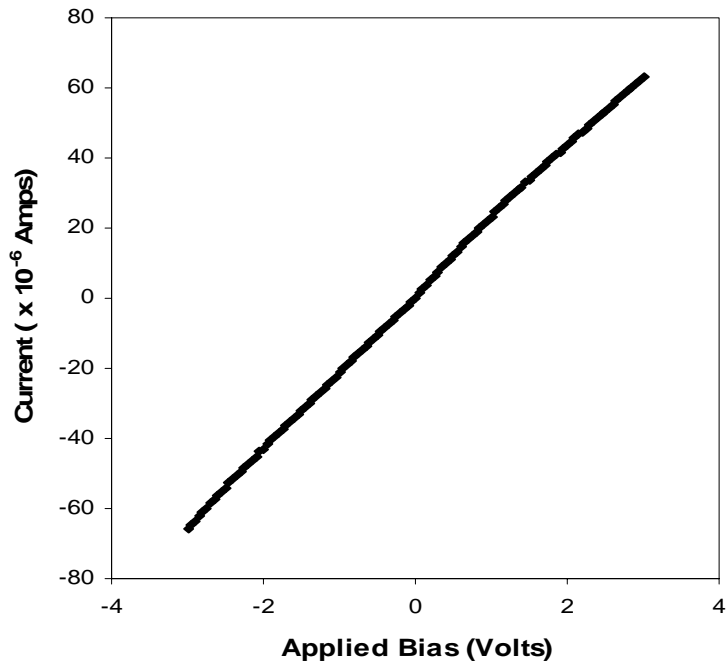


**Figure 3.4:** SEM image of a GaN nanowire with FIB deposited Pt metal contacts at the two ends.

This is expected, as it has been observed that Pt, with workfunction of 5.65 eV, when deposited on n-GaN generally forms Schottky contacts [43]. Although it is suitable to have a low workfunction metal such as Ti or Al for making low resistance ohmic contacts to n-GaN [44], it has been demonstrated that annealing metals like Ni, with a workfunction of 5.15 eV, can make ohmic contacts with fairly low specific contact resistance [45]. Similarly, in our case, annealing the contacts in UHP argon at 500 °C for 30 s resulted in linear contact behavior, as seen in Fig. 7 (b). Notably, the current level increased four orders of magnitude after the anneal. We speculate that the annealing of the Pt contacts formed Ga-Pt intermetallics. Indeed, formation of intermetallic phases like  $\text{Ga}_3\text{Pt}_5$  has been observed when Pt on GaN was annealed at 600 °C [46]. Formation of Pt gallides may lead to lowering of the contact barrier height due to the lower work function of the Ga-Pt intermetallics, which should lower contact resistance.



(a)

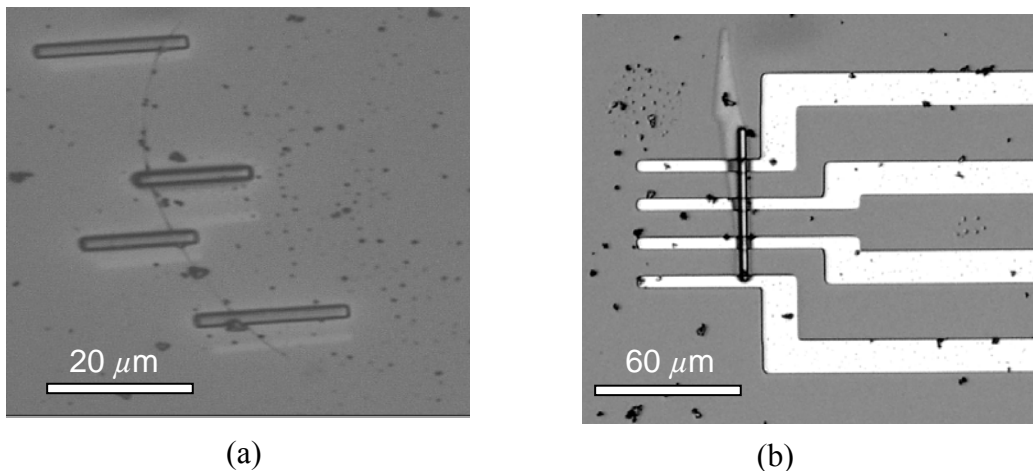


(b)

**Figure 3.5:** (a) Measured I-V characteristics of GaN nanowire with as-deposited FIB deposited Pt contacts. (b) Measured I-V characteristics of the same nanowire after annealing the Pt contacts at 500 °C for 30 s in UHP Argon.

Also, when Pt reacts with GaN, it will create defects in the crystal structure underneath the contact area, thus enhancing the conductivity via tunneling through the defects. It might be possible that both factors contributed to the lowering of the contact resistance. From the I-V characteristics of the nanowire with annealed contacts shown in Fig. 3.5 (b), the calculated two-terminal resistance was 50 kohm. The current densities recorded in the nanowires are in the region of  $5.0 \times 10^5 \text{ A cm}^{-2}$  for bias voltage of 3 V which is significantly higher than what has been reported so far [47], [48]. Higher current densities are beneficial for realizing efficient light emitting devices. Contact characteristics were very stable, with no Joule heating observed in the contacts with prolonged current flow.

Figure 3.6 (a) is an optical microscope image of a GaN nanowire with FIB-deposited four-terminal Pt contact structure, which was used to measure the resistivity of the nanowire.



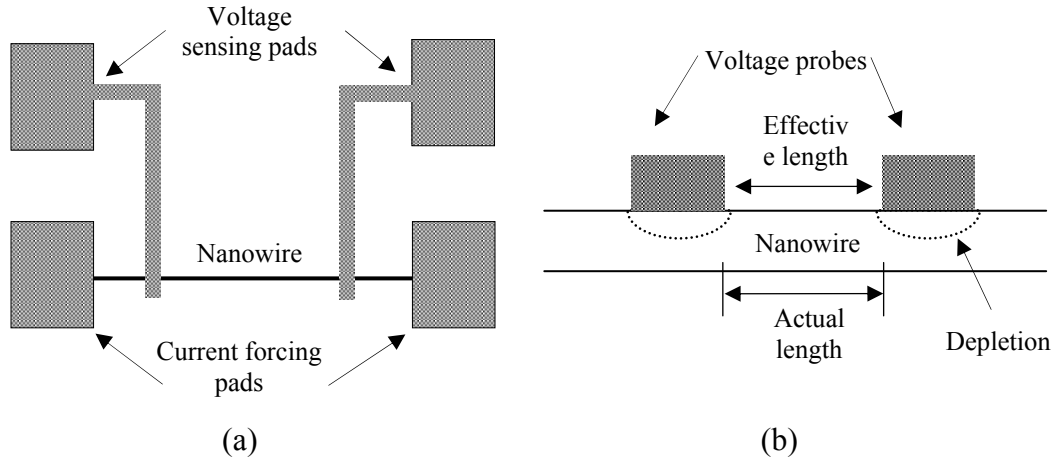
**Figure 3.6:** (a) Optical microscope image of a GaN nanowire with FIB-deposited four-terminal structure. (b) Optical microscope image of a FIB-deposited Pt line on a Cr/Au pre-patterned four-terminal structure.

Current was forced through the end contacts, and subsequently the voltage drop was measured using two inner electrodes (termed as voltage probes). The resistivity of the GaN nanowire measured using the four-terminal configurations was in the range of  $5 \times 10^{-3} \Omega \cdot \text{cm}$ . Although these nanowires are not intentionally doped, the lower value of the resistivity observed in these nanowires compared to bulk GaN, could be due to the nitrogen vacancies or residual contaminants like oxygen, which contribute to the background carrier concentration. High background carrier concentrations has been often noticed in these types of growth chambers [49].

In order to understand the effect of the resistance of FIB Pt contacts on the electrical characteristics of the nanowires, we measured the resistivity of FIB deposited Pt contacts utilizing a four-terminal configuration. It is well accepted that the resistivity of the FIB-deposited Pt is around  $5.0 \times 10^{-4} \Omega \cdot \text{cm}$  [50] which is generally an order higher than the value of bulk Pt ( $1.06 \times 10^{-5} \Omega \cdot \text{cm}$ ). Using similar deposition parameters as used to make contacts to the nanowires, we deposited a Pt line  $2 \mu\text{m}$  wide,  $60 \mu\text{m}$  long and  $1 \mu\text{m}$  thick, onto a pre-patterned four-terminal Cr/Au structure as shown in Fig. 3.6 (b). The resistivity of FIB-Pt obtained was  $9.0 \times 10^{-4} \Omega \cdot \text{cm}$ , which is a little higher than the accepted value. The resistivities of FIB-deposited metals are known to have a sensitive dependence on the deposition parameter [51].

Figure 3.7 (a) is a schematic diagram of the four-terminal structure used for resistivity measurement of nanowire. Although similar type of structure has already been used to measure the resistivity of both the metallic [52] and semiconducting nanowires [53], [54] the effect of the voltage probes in the resistivity measurement of

these nanowires has not been investigated. For metallic nanowires voltage probes will not have any significant effect on the resistivity measurements.

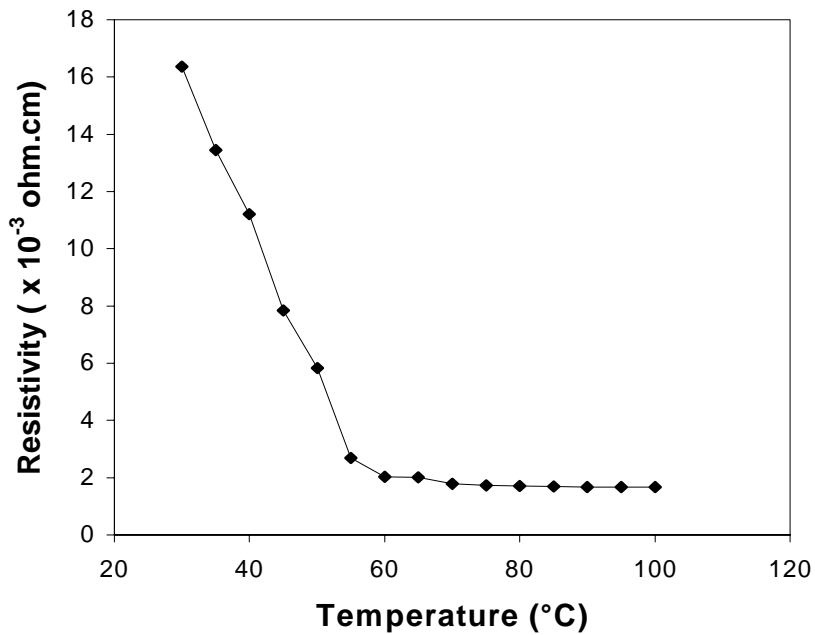


**Figure 3.7:** (a) Schematic diagram of the four-terminal structure used to measure the resistivity of the nanowires. (b) Schematic of the nanowire with the voltage probes, the depletion region associated with the voltage probes shown by the dashed line.

Generally the metals deposited to make contacts to the nanowire using electron-beam deposition, FIB, or any other technique will always cover most of the nanowire periphery. This induces depletion effect over the entire cross sectional area of the nanowire, which will extend laterally beyond the contact periphery as shown in Fig. 3.7 (b). This will reduce the effective length of the nanowire used for calculating the resistivity, thus leading to overestimation of the resistivity. One possible way to minimize this error is to cover the nanowire in a dielectric layer (i.e.  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ) and to use vias to make contact between the voltage probes and the top part of the nanowire. In this way the depletion width associated with the probe will be limited to only the top portion of the nanowire, thereby reducing the error in resistivity measurement.



In order to understand the nature of the transport through the nanowires we conducted temperature dependent resistivity measurement of the nanowire. Figure 3.8 is the plot of the resistivity of a GaN nanowire as a function of the temperature from 30 °C to 100 °C. Semiconducting behavior is clearly seen from the nanowire, the resistivity decreasing with increasing temperature, with a weak temperature dependence of the resistivity.

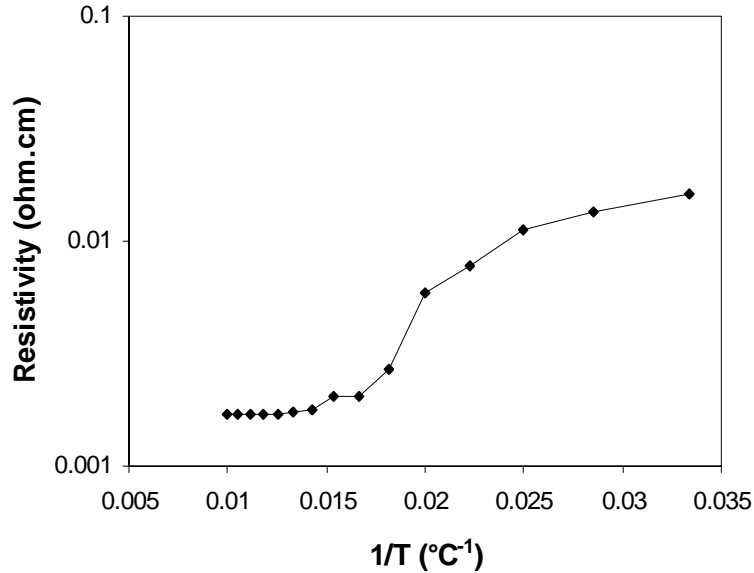


**Figure 3.8:** Plot of resistivity ( $\rho$ ) vs. temperature of a GaN nanowire.

For metallic conduction, the resistivity should have increased with the temperature. Although it is evident from the activation energy plot in Fig. 3.8 that the transport can not be simply described using the simple thermal activation energy resistivity model as given by

$$\ln \rho = \ln \rho_0 + \left( \frac{E_a}{k} \right) T^{-1} \quad (3.1)$$

where  $\rho$  is the resistivity of the nanowire,  $\rho_0$  is a characteristic constant, and  $E_a$  is the activation energy, yet some important features of the transport through the nanowire can be qualitatively pointed out from these results.



**Figure 3.9:** Activation energy plot of resistivity as a function of inverse temperature.

Two distinct slopes representing two different activation energies can be clearly seen in Fig. 3.9. In the range of 30 °C to 60 °C, the activation energy  $E_a$  is 20.0 meV, and for the range 60 °C to 100 °C the  $E_a$  is 2.4 meV. At higher temperatures (above 60 °C) the thermal generation of excess charge carrier across the bandgap may lead to a stronger electron-electron, and electron-phonon interactions thus leading to less variation in the resistivity of nanowire with temperature. The weak temperature dependence of the resistivity of the nanowire may be a signature of the electron-electron interactions in a two-dimensional disordered system, since the nanowires used for this study has structural defects and impurities. In order to gain a better

understanding of the transport properties of these nanowires, the resistivity measurements has to be performed at lower temperatures (liquid He 4.2 K).

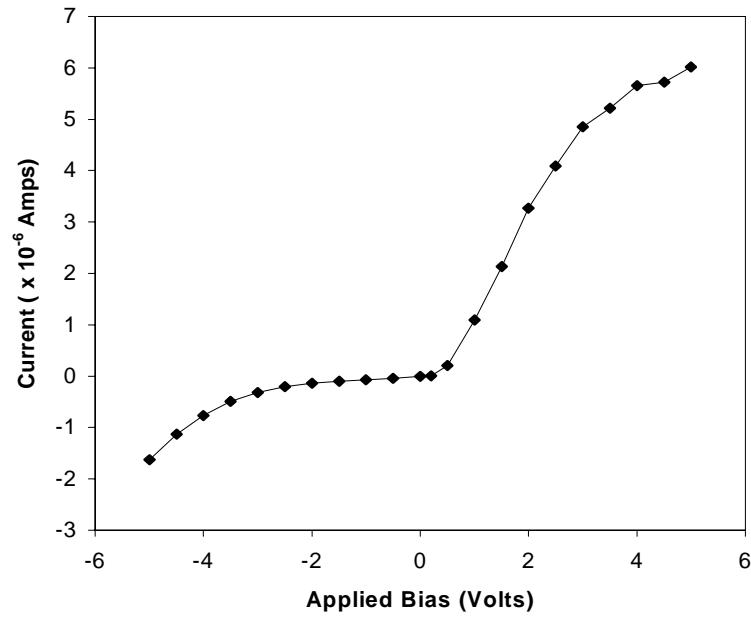
We have fabricated FIB deposited Pt Schottky contacts to these GaN nanowires, with pre-fabricated Ohmic contact formed by annealing FIB Pt contacts at 500 °C for 30 s in UHP argon. Measured I-V characteristics of the Pt-GaN nanowire junction from which we derived the ideality factor and the barrier height, is presented in Fig. 3.10 (a). Figure 3.10 (b) is a semi-log plot of the measured I-V curved of the Pt-GaN nanowire diode. From the I-V characteristics it is evident that the FIB-deposited Pt-GaN nanowire diode suffers from large reverse bias leakage current with reverse breakdown voltage around 4 V. This diode had low forward turn-on voltage (0.8 V) and soft reverse breakdown characteristics, which indicated that the tunneling mechanism might be the dominant mode of conduction in this diode. Current density  $J$  through a Schottky barrier junction resulting from the conventional thermionic emission can be expressed as

$$J = J_0 \left[ \exp\left(\frac{qV}{\eta kT}\right) - 1 \right] \quad (3.2)$$

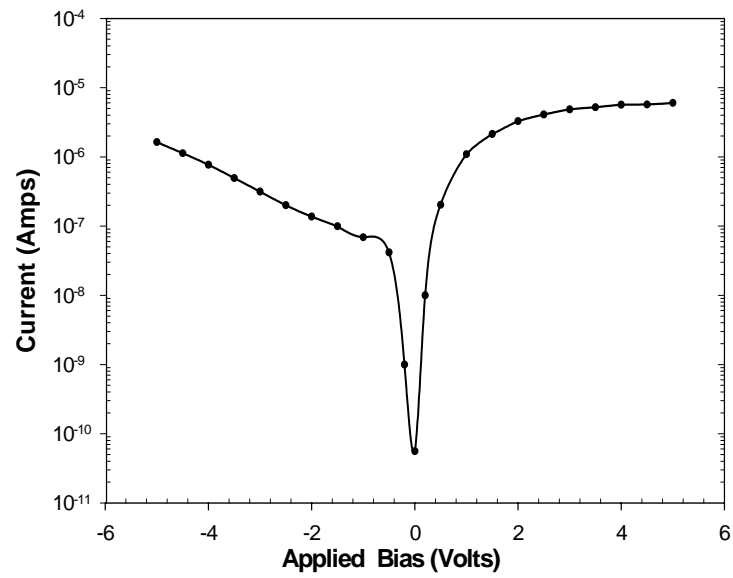
where  $J_0$  is the reverse saturation current density given by

$$J_0 = AT^2 \exp\left(\frac{q\phi_b}{kT}\right) \quad (3.3)$$

and  $A$  is the Richardson constant (assumed to be  $26 \text{ A.cm}^{-2}.\text{K}^{-2}$  for GaN) [55]  $V$  is the applied voltage,  $q$  is the electronic charge,  $T$  is the absolute temperature of the metal-semiconductor junction,  $\phi_b$  is the Schottky barrier height of the metal-semiconductor junction, and  $\eta$  is the ideality factor which represents the extent of non-ideality of the metal-semiconductor junction.



(a)



(b)

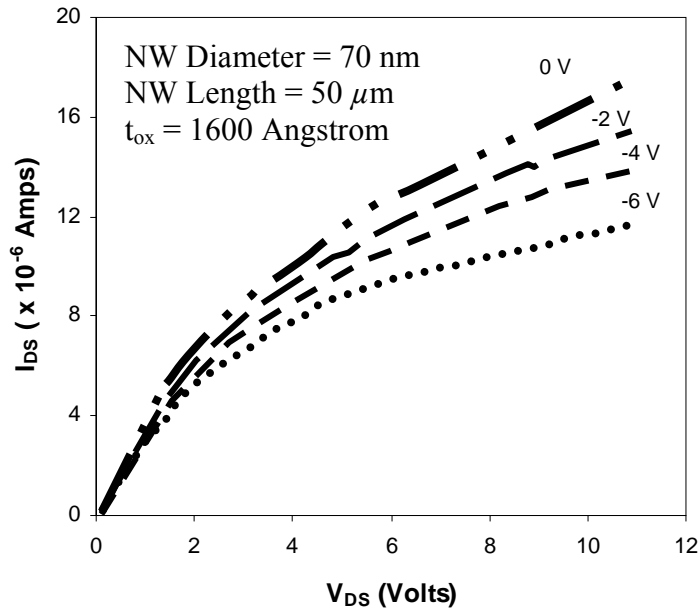
**Figure 3.10:** (a) I-V characteristics of FIB-deposited Pt-GaN Schottky diode (b) semi-log plot of I vs. V of the diode.

Using Eqs. 3.2 and 3.3 and the plot in Fig. 3.10 (b), the ideality factor  $\eta$  and the barrier height  $\phi_b$  were calculated to be 18 and 0.2 eV respectively, which is

reminiscent of the fact that these diodes are non-ideal probably due to the ion damage occurring during FIB deposition at the surface of these nanowires.

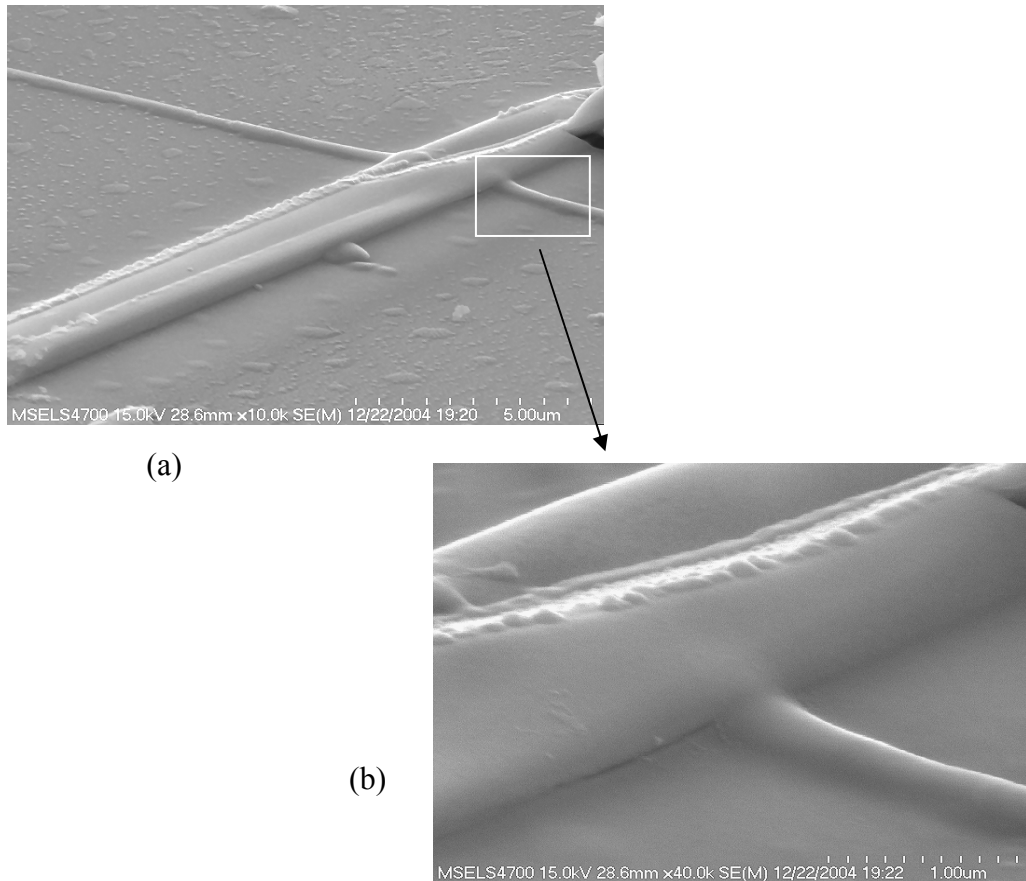
The detrimental effects of the ion damage on the electrical properties (increase in leakage current and reduction in reverse breakdown voltage) of Schottky diodes fabricated on epitaxial nitrides has been already demonstrated [56]. Thus we believe that the ion damage and the excess  $\text{Ga}^+$  implantation during Pt deposition resulted in higher leakage current and lower barrier height of these diodes. Mechanism of Ga implantation damage will be investigated in later section.

Metal-oxide-semiconductor FET (MOSFET) type transistor action from these nanowires has been achieved by depositing Al metal on the backside of the Si substrate. Annealed FIB deposited Pt contacts served as the source and drain contacts.



**Figure 3.11:**  $I_{\text{DS}}$  versus  $V_{\text{DS}}$  as a function of the gate voltage ( $V_{\text{G}}$ ) applied to the Si backgate. Gate voltage is indicated on each curve.

Figure 3.11 is plot of the source-drain current ( $I_{DS}$ ) vs. source-drain voltage ( $V_{DS}$ ) as a function of different gate voltages for a single GaN nanowire (diameter 70 nm, length 50  $\mu\text{m}$ ). It can be clearly seen that the device exhibits an n-type depletion mode behavior, which is due to the unintentional n-type background concentration (more on this will be discussed in chapter 6). Normalized transconductance was calculated to be around 10ms/mm with mobility in the range of  $20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . The mobility is low compared to the bulk mobility of GaN, which is expected due to the disordered nature of these nanowires.

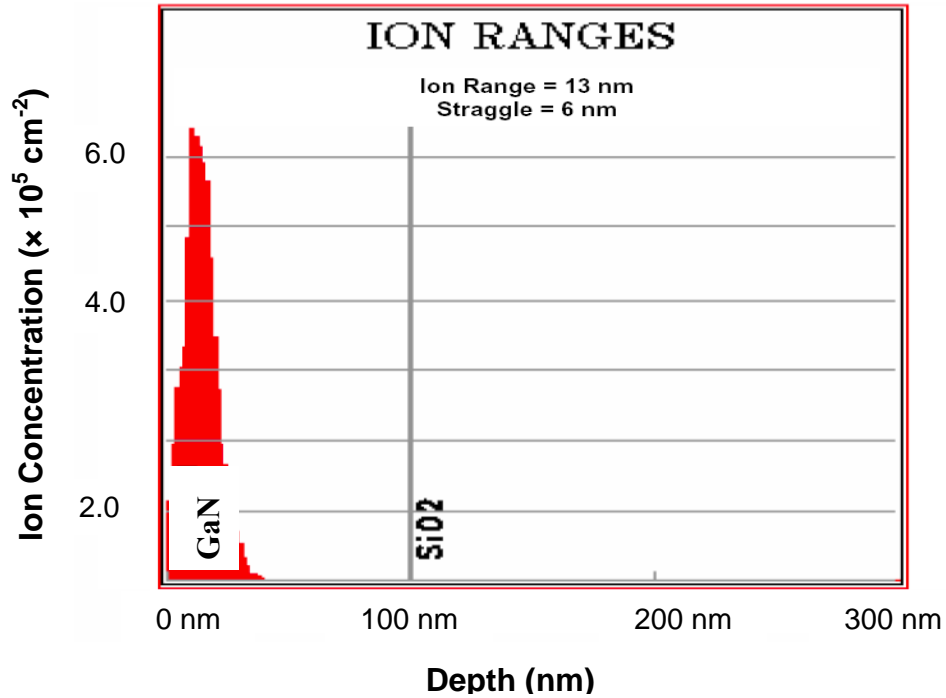


**Figure 3.12:** (a) SEM image of a FIB deposited Pt line on GaN showing the volume swelling underneath the contact region. (b) High resolution SEM scan showing the swelling of the nanowire underneath the contact region.

Careful investigation of the FIB Pt-GaN nanowire contact areas under SEM revealed an interesting feature. From Fig.3.12 (a)-(b), noticeable swelling of the nanowire underneath the FIB-deposited Pt contact can be clearly seen. Although similar nanowire swelling underneath the FIB deposited contacts was observed in other experiments [57], [58], the reasons for this effect has not yet been discussed. The study on Ga<sup>+</sup> self-implanted GaN nanowires [59] has revealed the formation of “nanoblister” and volume expansion of the nanowires after Ga<sup>+</sup> ion irradiation of the nanowires. Volume swelling and lattice damage of the GaN nanowires observed in the study was correlated to the large scale disintegration of Ga from the lattice and partially accumulation inside the nanoblister.

In order to gain a better understanding of the interactions of Ga<sup>+</sup> ion with GaN nanowires, we conducted simulation of the implantation of Ga<sup>+</sup> ions into the nanowires using Monte Carlo based STRIM<sup>®</sup> code (Fig. 3.13). Simulations showed that for implantation of 30 KeV Ga<sup>+</sup> ions into GaN, the nuclear energy loss mechanism is the dominant one with nuclear stopping power about 1.96 KeV nm<sup>-1</sup> which was an order of magnitude higher than the electron stopping power. The projected range for 30 KeV Ga<sup>+</sup> was about 15 nm, which indicates that most of kinetic energy of these ions is transferred to the GaN nanowire lattice (Fig. 3.13). This could lead to a significant rise in temperature of the nanowire. The heat generation in the nanowire during the FIB induced Pt deposition could also contribute to the structural deformation observed in the nanowires. A simplified quantitative calculation has been performed to calculate the temperature rise of the nanowire

during Pt deposition, using the amount of charge needed to deposit the small area of the contact immediately over the nanowire.

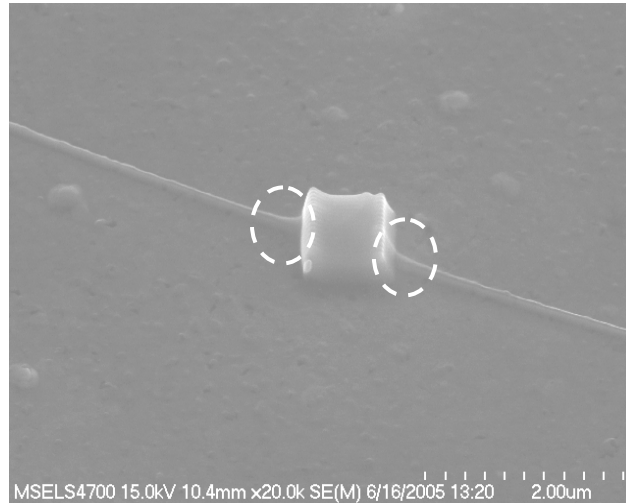


**Figure 3.13:** Implantation profile for 30 KeV Ga<sup>+</sup> ions in GaN.

Assuming very fast scan rate and negligible loss of energy of the Ga<sup>+</sup> ions during decomposition of the precursor, we calculated the total charge needed to deposit the small section of Pt line immediately over the nanowire (0.2 μm<sup>2</sup>). The energy associated with that amount of charge was  $1.485 \times 10^{-6}$  J, which according to the calculations could lead to a temperature rise of about 400 °C in the nanowire. Although this temperature rise is not significant, it could lead to the partial decomposition and melting of GaN nanowire, which is partially damaged due to Ga<sup>+</sup> ion implantation. In order to reveal the true nature of the effect of volume swelling of the nanowires, we conducted a parallel experiment and deposited Pt contacts to nanowires by electron beam induced deposition. Figure 15 shows the electron beam



induced deposited Pt contacts ( $0.8 \mu\text{m} \times 0.8 \mu\text{m}$ ) to the nanowire. The electron beam energy was 10 keV, with 200  $\mu\text{A}$  current aperture during the deposition. Close inspection revealed that there occurred a very similar swelling of the nanowire underneath Pt contacts deposited by electron beam. Although, small volume swelling is reported in electron-irradiated SiC due to the displacement of C and agglomeration of Si in the interstitial or antisite defect sites [60], but the energy used in that study was 1 MeV. It is unlikely that the electrons with 10 keV energy are capable of causing that type of lattice damage.



**Figure 3.14:** Electron beam induced deposited Pt contact to GaN nanowire. Swelling of the nanowire at the ends of the contacts is indicated by white broken circles.

It is most likely that the heat generated by the focused  $\text{Ga}^+$  beam during deposition was the main cause of the swelling of the nanowires underneath the contact area. Further studies are to be performed to determine the nature of the interaction of ions with these nanowires.

## **Chapter 4: Electric Field Assisted Alignment of Nanowires**

Results of individual GaN nanowire devices reported so far [47], [61], [62], utilize fabrication processes, which require individual nanowire manipulation and registration to form metal contacts. These processes often involve time consuming serial techniques like electron beam lithography, scanning probe techniques, and atomic force microscope manipulation. Such techniques are unsuitable for large-scale batch fabrication. To this date, assembly of nanowires without individual registration has been attempted mainly using electric field assisted aligning [63], chemical patterning, or microfluidic aligning [41]. Although simple assemblies have been obtained using these techniques, so far the most complex hierarchical nanowire network has been assembled utilizing the Langmuir-Blodgett (LB) technique [64]. Even though LB technique is quite successful in creating dense networks of nanowires with repeatability and significant yield, it requires addition of surfactants to the nanowire suspension and complex compression procedures for the monolayer formations. This makes LB process incompatible with the CMOS processing technology.

This chapter focuses on the assembly of the nanowires and methods of realizing reliable nanowire device structures without the use of serial fabrication techniques such as e-beam lithography, focused ion beam techniques, atomic force microscope manipulation etc. In order for any assembling technique to be effective and successful, it should address following issues:

1. Large-scale simultaneous placement of nanowires
2. Positioning nanowire at the pre-determined patterns without individual nanowire

registration and manipulation

3. Reliable, reproducible and compatible with Si processing technology.

In this chapter we will discuss electric field assisted alignment technique, which is termed as dielectrophoresis. We will look into the theoretical understanding of the electric field assisted alignment process by developing a simple model describing the alignment of gallium nitride nanowires suspended in a solvent. The variation in the dielectrophoretic force experienced by the nanowire in different dispersing solvents has been calculated. Using commercial software packages, we have investigated different alignment pad designs, and implemented them in the assembly. We will also discuss the experimental setup used to perform dielectrophoresis and results.

#### **4.1 Dielectrophoresis – Theoretical Background**

A neutral particle placed in a non-uniform electric field experiences a force due to the interaction of the induced dipole moment with the divergent electric field. This force is called the dielectrophoretic (DEP) force, and the translational motion of the neutral particle caused by this force is termed as dielectrophoresis [65]. Aligning or manipulating particles using the dielectrophoretic force relies on the difference in the polarizability of the particle and the medium used for suspending the particles. Generally the suspending medium is an organic solvent such as isopropanol (IPA), ethanol, acetone etc. The force experienced by a neutral particle in such a solution due to the non uniform electric field is given by the relationship (bold faced letters indicate vector quantities)

$$\mathbf{F}_{\text{DEP}}(\mathbf{t}) = (\mathbf{p}(\mathbf{t}) \cdot \nabla) \mathbf{E}(\mathbf{t}) \quad (4.1)$$

where  $\mathbf{F}_{\text{DEP}}(t)$  is the time dependent dielectrophoretic force experienced by the particle,  $\mathbf{p}$  being the induced dielectric moment vector, and  $\mathbf{E}(t)$  is the time varying applied electric field. The dipole moment vector, for the simple case where the body is isotropically, linearly, and homogenously polarizable, depends on the applied electric field as such

$$\mathbf{p}(t) = \alpha V \mathbf{E}(t) \quad (4.2)$$

where  $\alpha$  is the polarizability tensor for the particle and  $V$  being total volume of the particle. It can be shown that the time averaged DEP force is given by the equation [67], [68]

$$\langle \mathbf{F}_{\text{DEP}} \rangle = \Gamma \varepsilon_m \text{Re}\{k_f\} \nabla |\mathbf{E}_{rms}|^2 \quad (4.3)$$

where  $\Gamma$  is the particle geometrical factor,  $\text{Re}\{k_f\}$  is the real part of the Clausius-Mossotti factor which depends on the shape of the particle,  $\varepsilon_m$  is the real part of the complex permittivity of the medium, and  $\mathbf{E}_{rms}$  is the root mean square value of the electrical field. The complex permittivity is given by

$$\varepsilon^* = \varepsilon - i \frac{\sigma}{\omega} \quad (4.4)$$

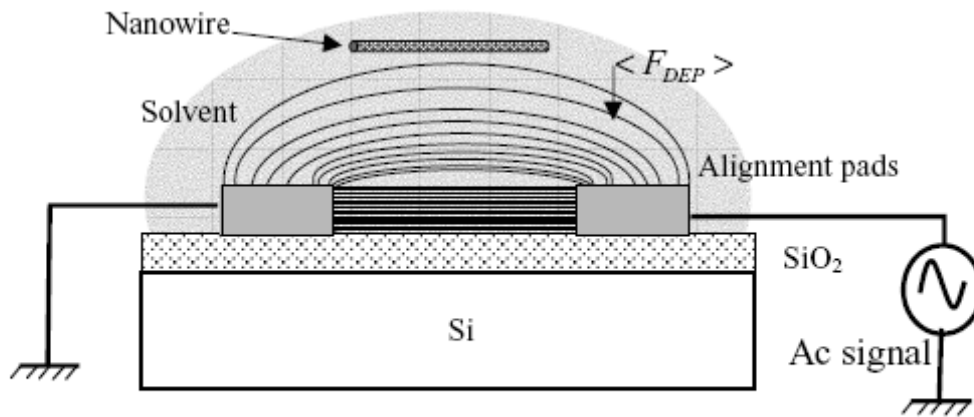
The  $\varepsilon$  is the real permittivity,  $\sigma$  is the conductivity, and  $\omega$  is the angular frequency of the applied electric field. For a cylindrical particle with length  $l$  and radius  $r$  where  $l \gg 2r$ , the  $k_f$  and  $\Gamma$  are given by

$$k_f = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_m^*}, \quad (4.5)$$

$$\Gamma = \frac{\pi}{6} r^2 l \quad (4.6)$$

where  $\epsilon_p^*$  and  $\epsilon_m^*$  are the complex permittivities of the particle and the medium respectively.

Figure 4.1 schematically explains the working principle of the dielectrophoretic alignment of the nanowires. In order for dielectrophoresis to work the nanowires has to be suspended in a solvent. This is usually done by sonicating the growth matrix in a glass vial containing suitable solvent.



**Figure 4.1:** Schematic representation of dielectrophoretic alignment of nanowires using a solvent medium.

The energy from the ultrasound breaks the nanowires from the growth matrix and releases them into the solvent. Due to their minuscule weight ( $\sim 10^{-15}$  kg), their settling times are large, hence a suspension of nanowires is formed. A pre-patterned substrate, in this case SiO<sub>2</sub> coated Si substrate, is used with metal pads formed by lithography on the surface. When the nanowire suspension is dispersed on a sample with voltage applied between two metal pads, the divergent electric field interacts with the induced electric dipole moment of the nanowire. The DEP force experienced

by the nanowire is normal to the sample surface. In case of a positive dielectrophoretic force (determined by the difference in the dielectric permittivities of the nanowire and the dispersing solvent), the nanowires will bridge the pads with complete evaporation of the solvent.

## **4.2 Designing the Assembly Process**

The factors that determine the effectiveness, and subsequently the yield of the alignment process are:

- a) Frequency of the applied voltage
- b) Solvent used for dispersion of the nanowires
- c) Diameter and length of the nanowire
- d) Presence of microplatelets (from the matrix layer)
- e) Alignment electrode design including geometry and thickness
- f) Amplitude of the applied voltage and configuration time

In order to reproducibly align the nanowire it is important to determine the optimum alignment conditions (above listed factors) using a theoretical approach rather than trial and error method. Following sections describe the analytical calculations and software simulations performed to achieve a high-yield alignment process.

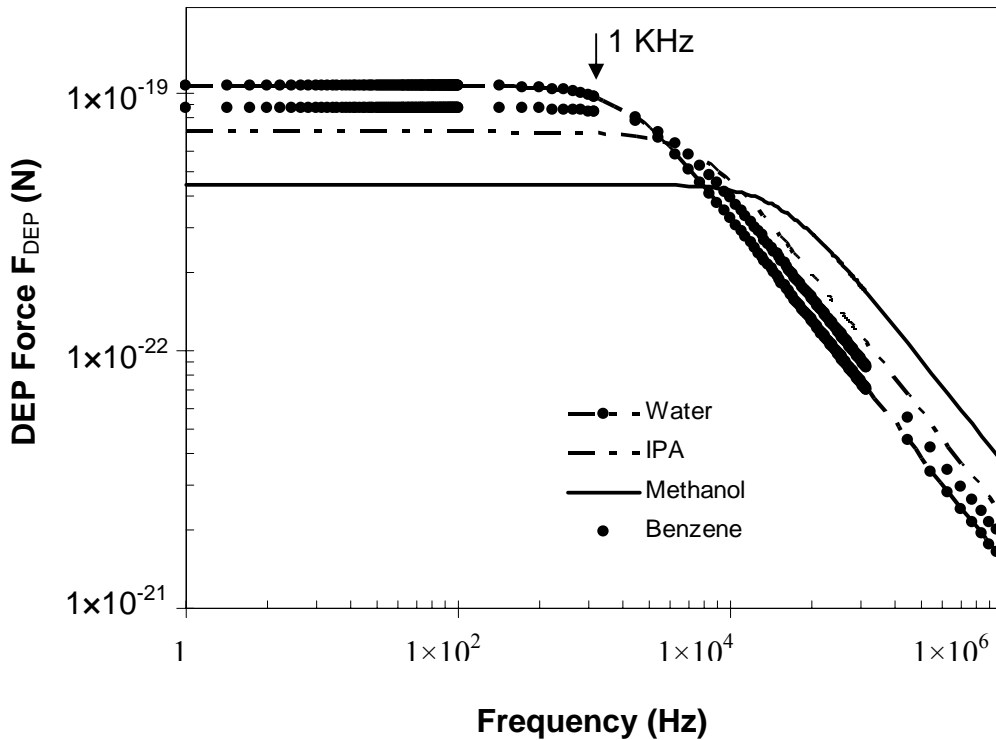
### **4.2.1 Numerical Calculations – Solvent and Frequency Choice**

In order to estimate the effect of different solvent and frequency we have to model the physical situation by assuming that the nanowires are perfectly cylindrical particles (with  $l \gg 2r$ ). Using Eqs. 4.3-4.5 and Eq. 4.6, the relative DEP forces experienced by

a GaN nanowire in the presence of different dispersing media can now be calculated. The real part of the Clausius-Mossotti factor for a cylindrical particle from Eq. 4.5 is given by

$$\text{Re}\{k_f\} = \frac{\omega^2 \varepsilon_m (\varepsilon_p - \varepsilon_m) - \sigma_m (\sigma_m - \sigma_p)}{\omega^2 \varepsilon_m^2 + \sigma_m^2}. \quad (4.7)$$

Fig. 4.2 shows the relative dielectrophoretic force variations for a 100 nm radius and 50  $\mu\text{m}$  long nanowire in water, isopropanol, ethanol, and benzene respectively as a function of the bias frequency. Table 4.1 lists all the parameters used for calculating the DEP forces.



**Figure 4.2:** Calculated DEP force experience by <sup>(a)</sup> a nanowire (100 nm diameter and 50  $\mu\text{m}$  in length) in different dispersing medium as a function of the alignment voltage. The drop in the DEP force for different solvents starts around 1 KHz.

For simplifying the calculations the plot is for unit  $\nabla |\mathbf{E}_{rms}|^2$ . The conductivity of the GaN nanowires used for the calculations was  $2.0 \times 10^4 \Omega^{-1} \text{ m}^{-1}$ , as obtained in chapter 2. The relative dielectric permittivity for GaN used for the calculation was 9.7.

**Table 4.1.** Physical parameters used for the calculation of DEP forces for a nanowire in different solvents.

Medium	Relative Dielectric Constant $\epsilon_m / \epsilon_0$ *	Conductivity $\sigma(\text{S.m}^{-1})$
Water	80.0	$7.6 \times 10^{-6}$
Methanol	32.9	$4.4 \times 10^{-5}$
Isopropanol	18.6	$6.0 \times 10^{-5}$
Benzene	2.3	$4.0 \times 10^{-7}$

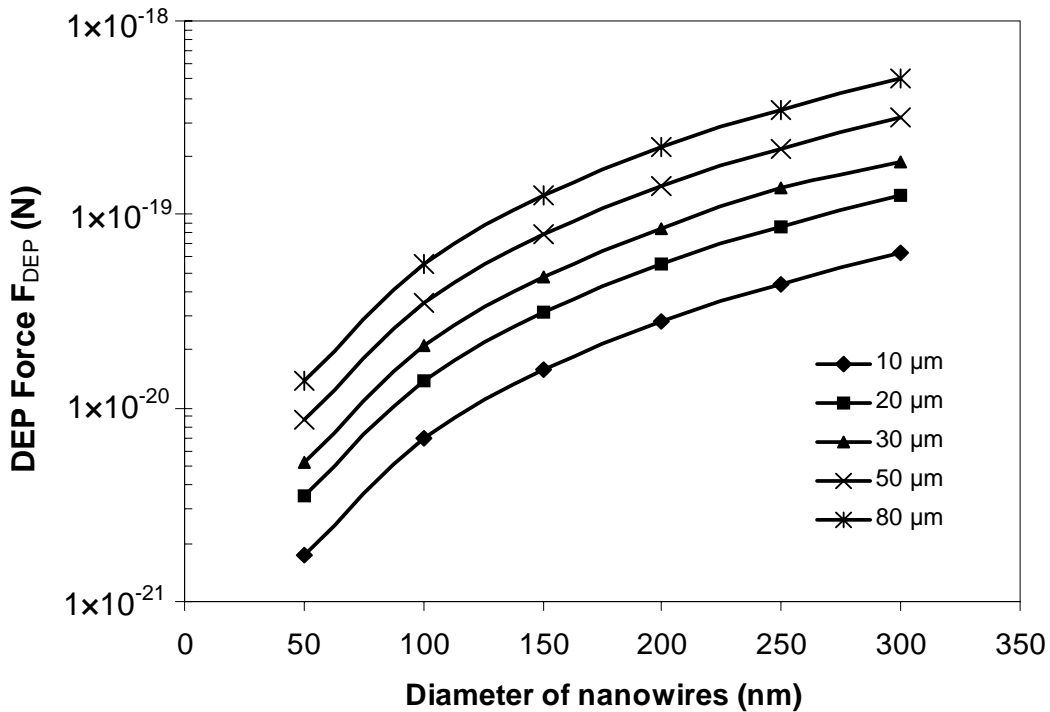
\*  $\epsilon_0$  denotes the dielectric constant of vacuum =  $8.854 \times 10^{-12} \text{ F.m}^{-1}$

From the Fig. 4.2 it is clear that at low frequencies, between 1 Hz and 1 kHz, the DEP force is constant with the frequency for different dispersions. From Eq. 4.7 it can be seen that at low frequencies the DEP force is determined by the difference in the conductivities of the particle and the dispersing medium, whereas at high frequencies the DEP force is proportional to the difference in their permittivities. Water, although having the largest DEP force factors out of the four dispersing medium, is not a good choice for DEP alignment, as maintaining high resistivity and low ionic conduction is challenging for water. Benzene appears to be a reasonable alternative to water with its DEP force factor comparable to water. Above 1 kHz, all the curves for different



dispersing medium experiences a roll off associated with the dielectric relaxation of the medium and the particle. The calculated maximum frequency of alignment (about 1 kHz) as obtained from the graph agrees well with the experimentally observed yields.

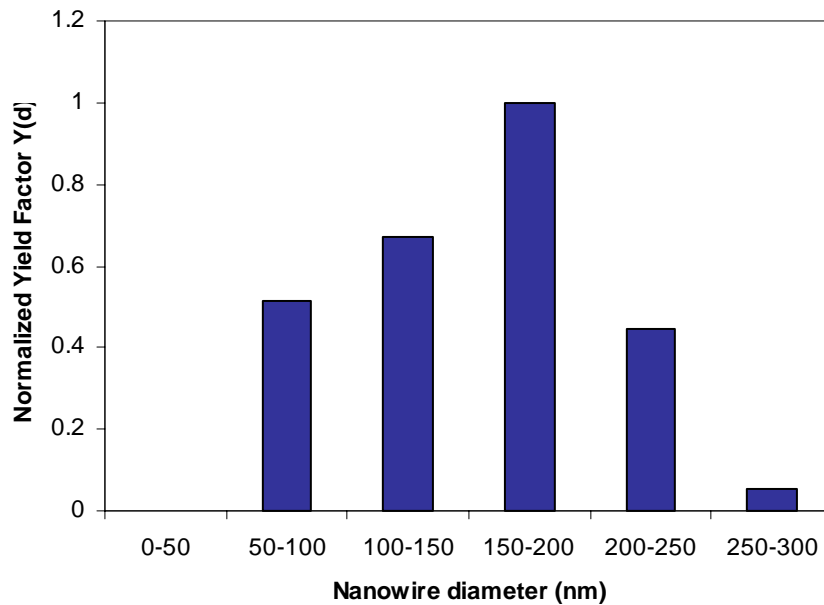
Fig. 4.3 is a plot showing the DEP forces experienced by nanowires in IPA as a function of the diameter of the nanowire for different lengths of the nanowires. The alignment frequency is 1 kHz with peak to peak voltage of 20 volts.



**Figure 4.3:** Calculated DEP force variation as a function of nanowire diameter and length. The alignment frequency is set to 1 KHz and the dispersing medium is IPA.

It is clear that the thicker nanowires experience larger DEP force than the thinner nanowires. Also there is about one order of magnitude increase of the DEP force with the increase in length of the nanowires from 10 μm to 80 μm. This

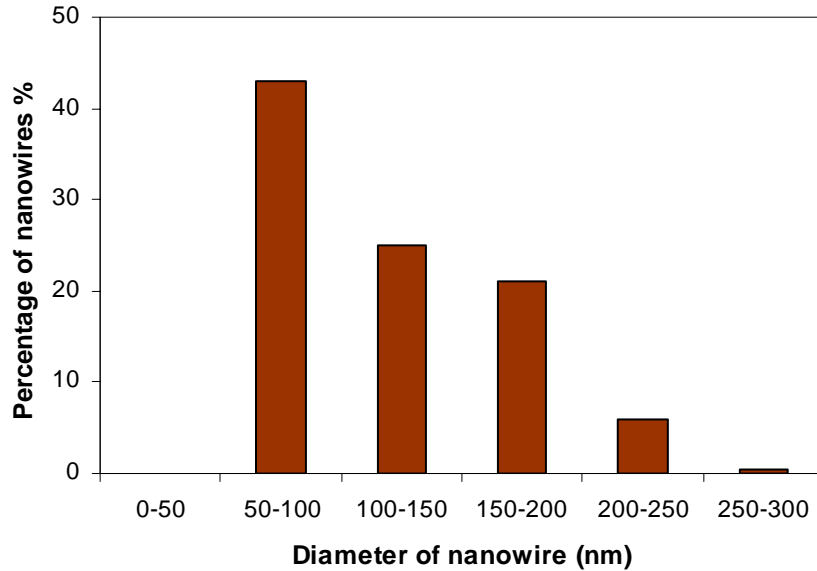
variation in DEP forces experienced by nanowires of different dimensions can be utilized for selective alignment of nanowires. In chapter 2 the distribution of the nanowire diameters in the growth matrix was discussed. A qualitative yield parameter  $Y$  (yield as a function of nanowire diameter) can be obtained as:  $Y(d) = f(d) \times F_{DEP}(d)$ , where  $f(d)$  and  $F_{DEP}(d)$  represents the diameter distribution and the DEP force factor. This factor serves as an indicator of the nature of nanowire devices that can be expected from the assembly process (Fig. 4.4). The normalized yield factor tells us the fraction of nanowires of different diameters we can expect in the assembly process.



**Figure 4.4:** Normalized yield factor as a function of nanowire diameter for DEP process in IPA.

For comparison purposes the nanowire diameter distribution in the growth matrix is shown here again (Fig. 4.5). This yield factor enables us to estimate the

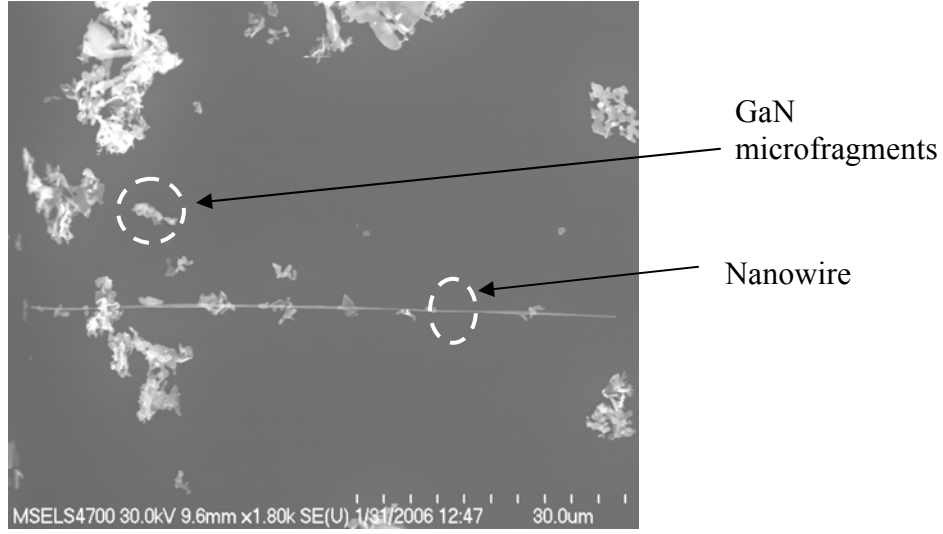
nature of the electrical system assembled using dielectrophoresis prior to the assembly.



**Figure 4.5:** Diameter distribution of nanowires as observed in the growth matrix.

One major problem associated with DEP alignment of GaN nanowire is the presence of GaN microparticles. The growth product used for assembling is a dense network of GaN nanowires emerging from a thin layer of randomly oriented GaN microplatelets, which is sonicated in a solvent to form a nanowire suspension. Unfortunately the sonication process also releases the microparticles into the suspension. Thus the suspension used for dispersion contains both the nanowires and the GaN microplatelets or fragments, as seen in Fig 4.6. The microplatelets are GaN crystallites with diameters ranging from  $2 \mu\text{m}$  to  $20 \mu\text{m}$  possessing the similar materials properties. These microparticles also experiences the DEP force hence movement towards the aligning pad. These particles make the photoresist coatings for lithography non-uniform. They can also form parasitic pathways for conduction. It is therefore necessary to investigate in detail as to how these microparticles interact with

the alignment field. We have calculated the DEP forces experienced by these GaN microfragments assuming they are perfectly spherical.



**Figure 4.6:** GaN nanowires and platelets as seen on a Si substrate, which is characteristic of the dispersion.

For a cylindrical particle ( $r$  radius)

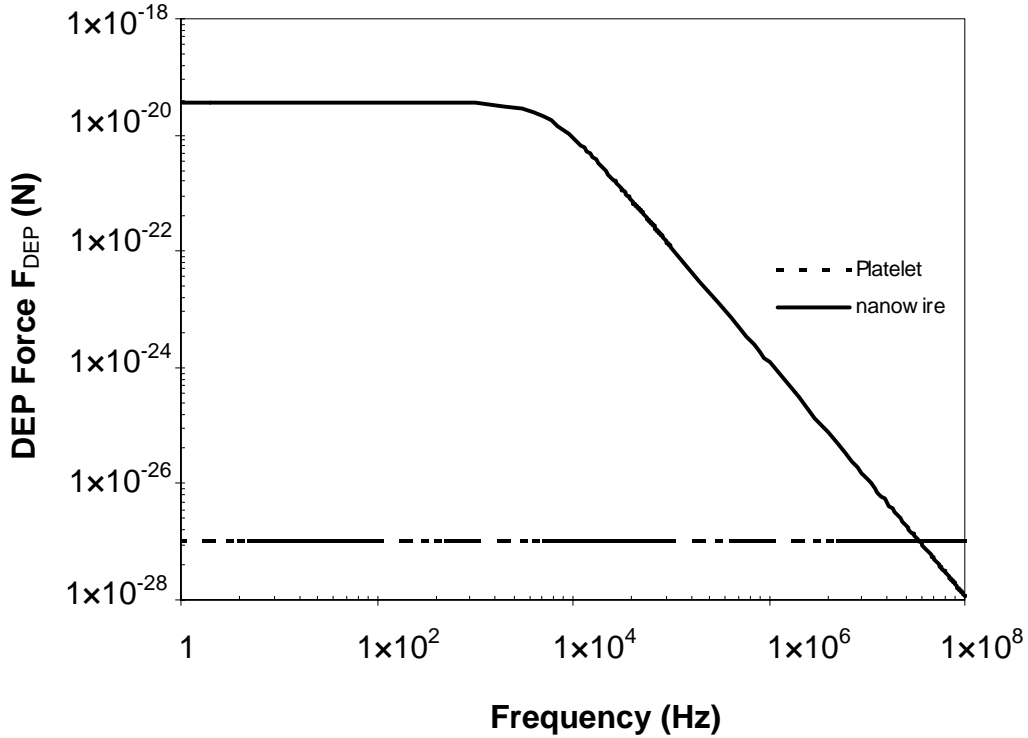
$$k_f = \frac{\epsilon_p^* - \epsilon_m^*}{\epsilon_p^* + 2\epsilon_m^*} \quad (4.8)$$

$$\Gamma = 2\pi r^3 \quad (4.9)$$

Using Eqs. 4.8 - 4.9 the real part of the Clausius-Mossotti factor for a spherical particle is calculated as:

$$\text{Re}\{k_f\} = \frac{\omega^2(\epsilon_p + 2\epsilon_m)(\epsilon_p - \epsilon_m)}{\omega^2\epsilon_m^2 + \sigma_m^2} - \frac{\omega^2(\epsilon_p + 2\epsilon_m)(\epsilon_p - \epsilon_m)}{\omega^2\epsilon_m^2 + \sigma_m^2}. \quad (4.10)$$

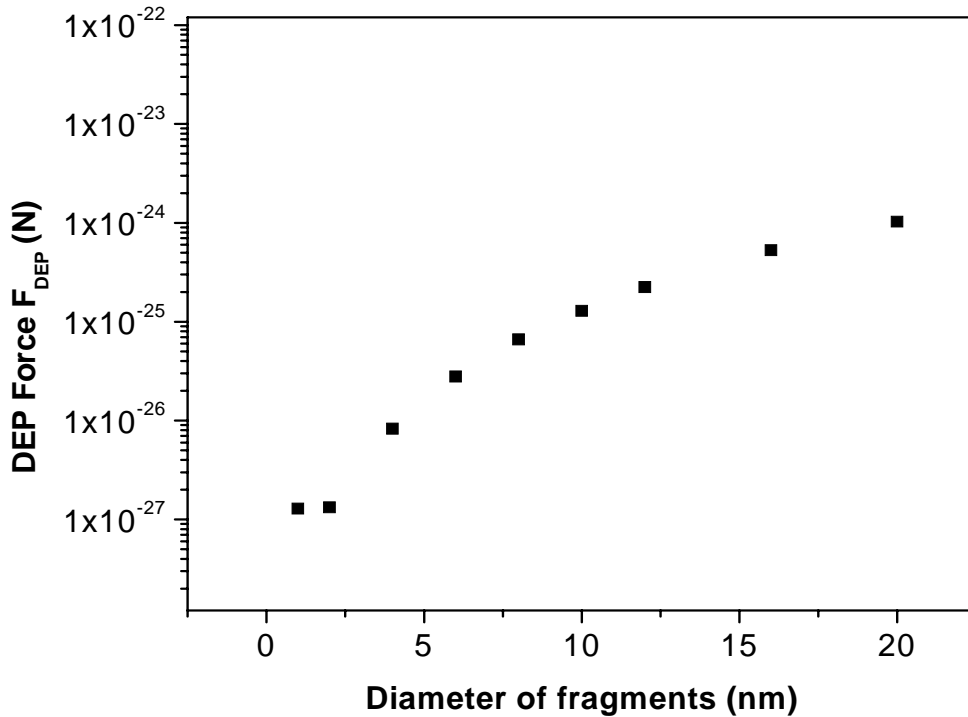
Fig. 4.7 is the plot of the variations of the DEP force experienced by a nanowire (100 nm diameter and 50  $\mu\text{m}$  length) and a spherical GaN fragment (2  $\mu\text{m}$  diameter) in IPA as a function of the frequency of the aligning field.



**Figure 4.7:** Calculated DEP force experience by a nanowire (100 nm diameter and 50  $\mu\text{m}$  in length) and a spherical fragment (2  $\mu\text{m}$  diameter) in IPA with alignment frequency at 1 KHz.

It is interesting to note that in the low frequency range, a perfectly spherical particle experiences negligible DEP force compared to a nanowire. Due to their large conductances, the spherical GaN microfragments do not exhibit significant variations in DEP force with the frequency. This factor might be beneficial in selective alignment of nanowires over the fragments. We have not investigated the effects of the irregular shapes of these fragments on the DEP forces experienced by them,

although Fig. 4.8 shows a plot of the DEP force experienced by spherical particles of different diameters.



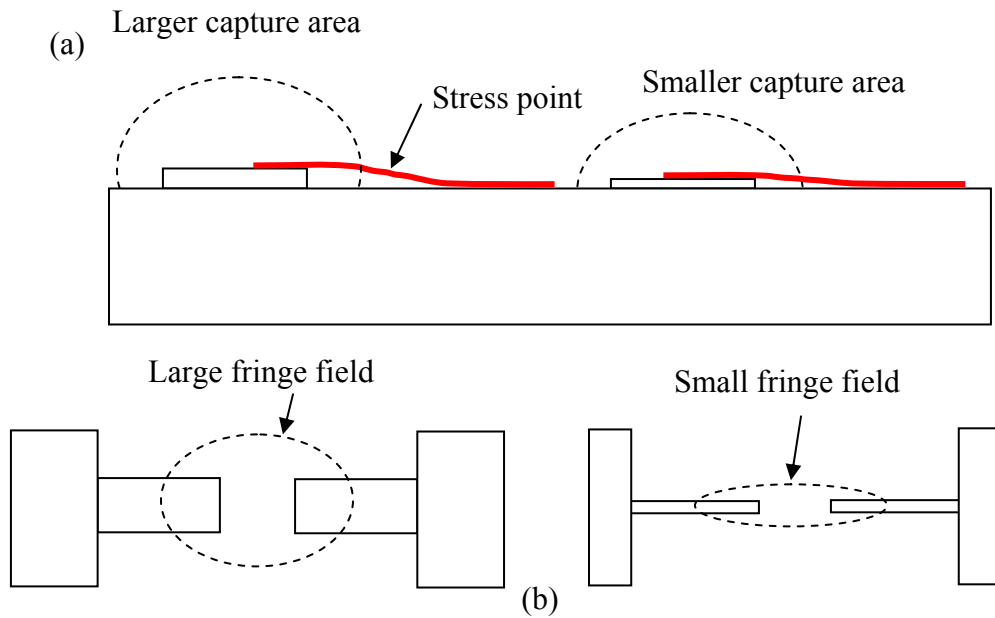
**Figure 4.8:** Variations of the DEP force experienced by spherical GaN microfragments in IPA as a function of their diameters, with alignment frequency set to 1 KHz.

From the plot it is clear that the larger size fragments (15  $\mu\text{m}$ ) experience DEP forces comparable to those experienced by the nanowires. Although these simplified calculations show that the GaN fragments are less attracted by the alignment field, in experiments it is found that after alignment the nanowires had these fragments attached to them. We believe this is due to the fact that the nanowires, when bridged between two alignment pads have a strong radial electric field surrounding them. Due to their small diameters, the electric field gradient normal to the surface of the

nanowires is quite large and is capable of attracting these fragments on to the nanowire surface.

#### 4.2.2 Alignment electrode design – Electrostatic Simulations

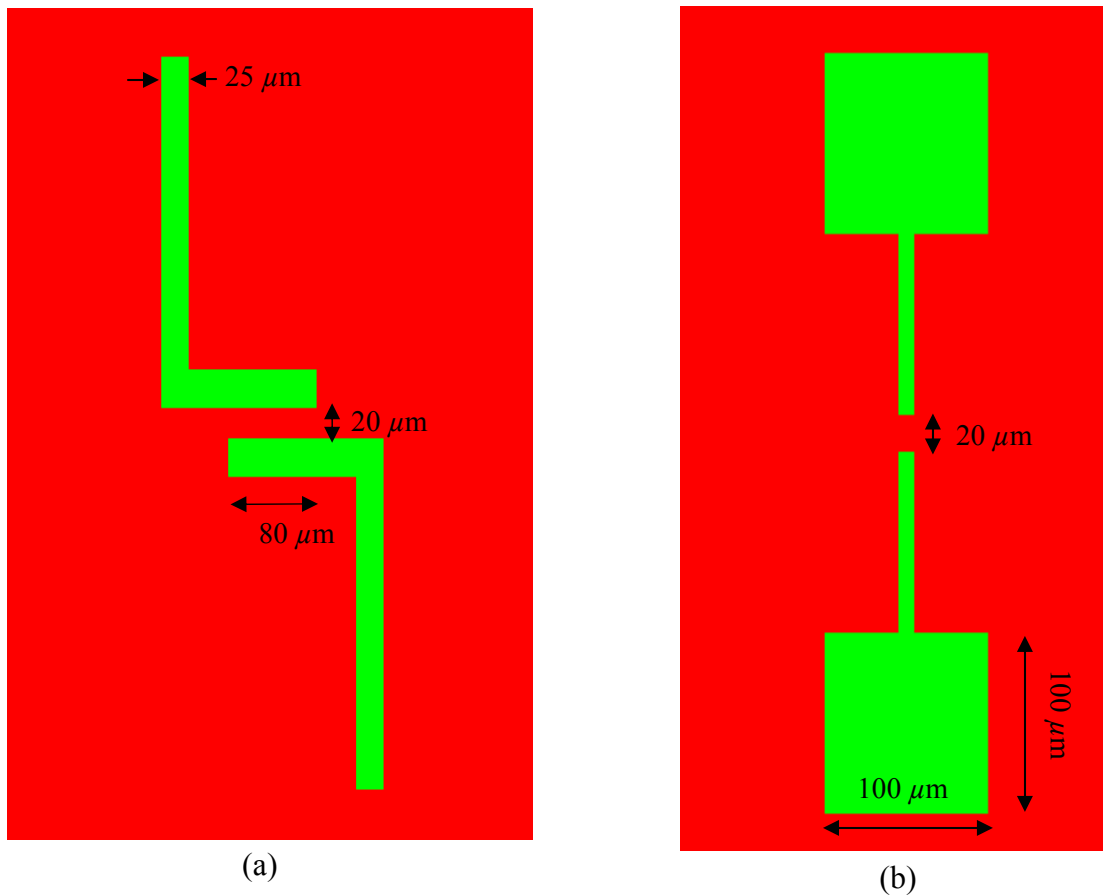
Alignment electrode geometry determines the how efficiently nanowires can be trapped in a pattern. This electrode geometry has also to be compatible with the type of device, which is going to be realized from the nanowires. Two important aspects of the alignment electrode design are a) the height of the electrode, and b) the shape of the electrode. Fig. 4.9 illustrates the necessity of optimum electrode design. Alignment electrode with large height has higher capture area associated with it but would results in larger stress in the nanowire due to bending.



**Figure 4.9:** (a) Bending of the nanowire across the edge of the electrode. (b) Large area patterns versus small area patterns.

Large area electrodes also has higher capture probability but at the cost of large fringe fields which can attract debris and more than one nanowire. This degrades the

precision of the alignment. Commercial electrostatic simulation package Maxwell<sup>®</sup> is used to estimate the effectiveness of various alignment electrode designs. Two different electrode designs (Fig. 4.10) have been studied. In the first design [design 1, Fig.4.10 (a)], the electrodes are interdigitated with the capture area in the middle ( $20 \mu\text{m} \times 80 \mu\text{m}$ ). In the second design [design 2, Fig.4.10 (b)], the electrodes were facing each other directly. The red area is the  $\text{SiO}_2$ , while the green represents the metal in the design.

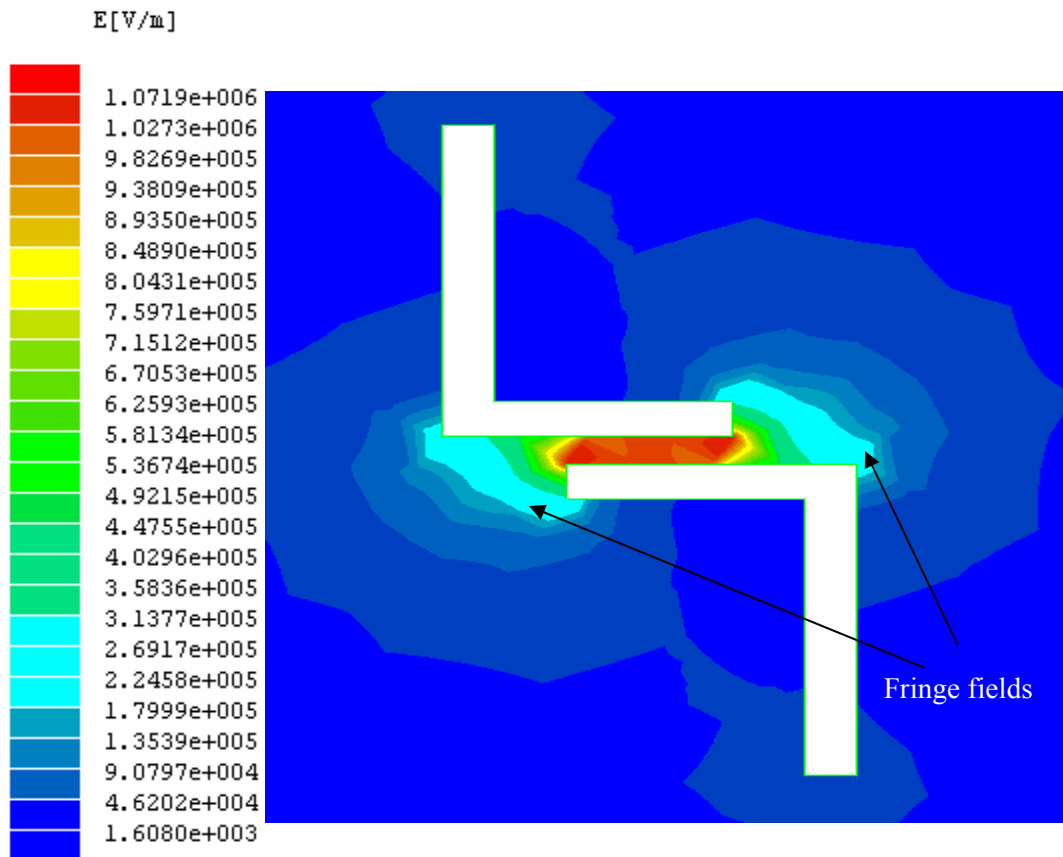


**Figure 4.10:** (a) Electrode design 1. (b) Electrode design 2.

The contour plot of electric field strength in  $\text{V/m}$  is shown in the x-y plane for the design 1 in Fig. 4.11. This plot is generated with  $-10 \text{ V}$  and  $+10 \text{ V}$  bias applied to the



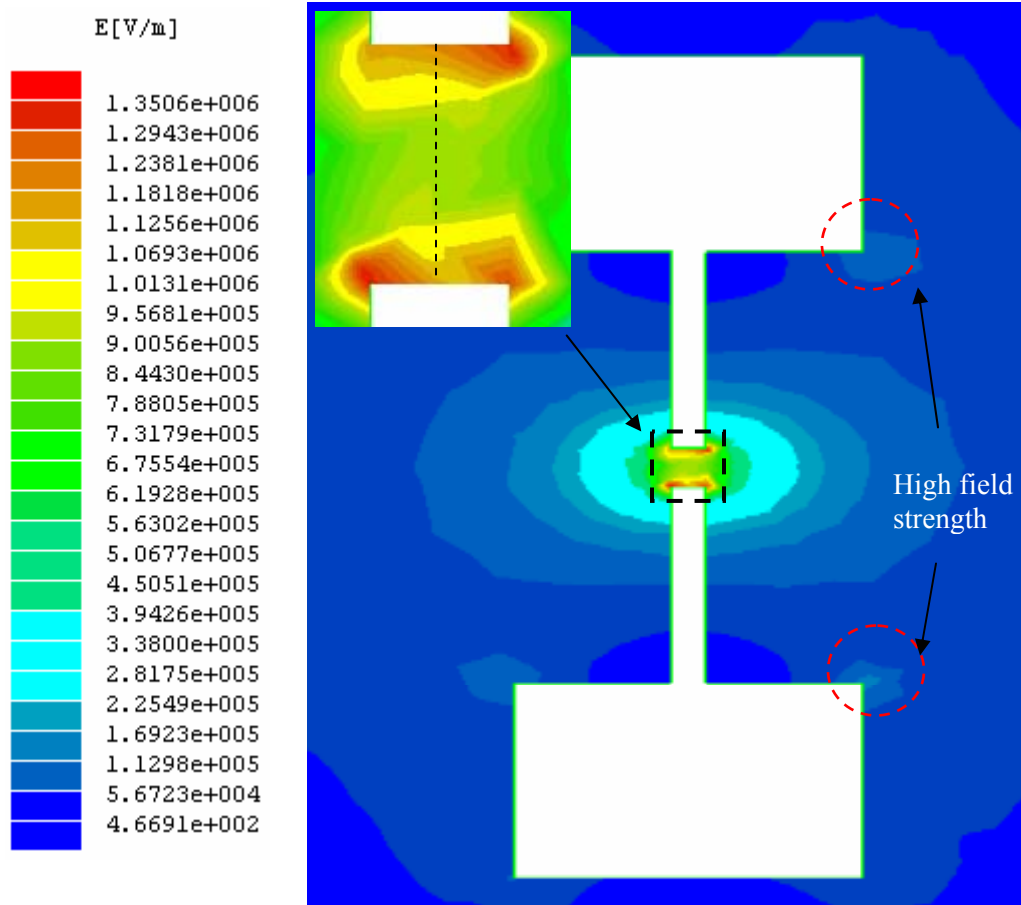
upper and lower electrode respectively. Field strength as high as  $1 \times 10^6$  V/m is seen to appear in the middle of the capture area. Although the field strength is quite uniform inside the capture area, the extent of the fringe fields on the side of pattern (as shown by arrows in the Fig. 4.11) is highly undesirable. It will be shown in the result section that these fringe field regions result in nanowire capture along the edges of the electrodes.



**Figure 4.11:** Electric field intensity for design 1 on the substrate plane (x-y plane) for +10 V and -10V connected to top and bottom electrode respectively.

For the second design (design 2) the contour plot of electric field strength (Fig. 4.12) shows major improvement (for +10 V and -10V connected to the top and bottom

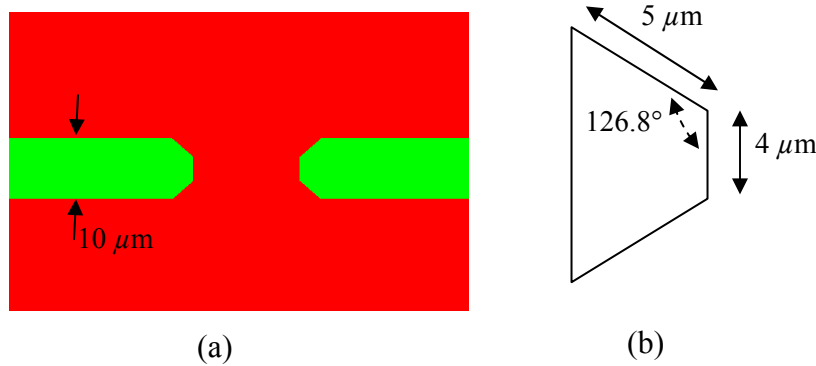
electrode). The high field region is concentrated in the middle thus resulting in smaller capture area and better alignment precision.



**Figure 4.12:** Electric field intensity for design 2 on the substrate plane (x-y plane) for +10 V and -10V connected to top and bottom electrode respectively. (inset) Field intensity in the region marked by the black box.

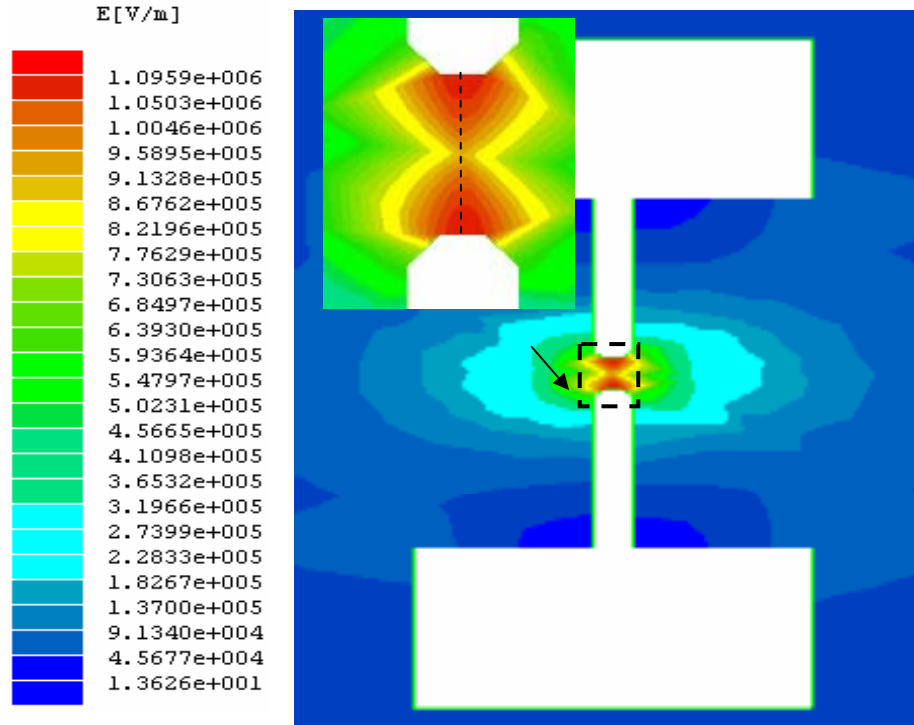
Although this design produces better defined capture area, the field strength inside the capture area is not uniform as seen on the magnified plot of the center of the pattern (inset of Fig. 4.12). Also corner high field regions are present (red circles in the Fig. 4.12), which will produce non-uniform field gradients capable of attracting nanowires. It has to be noted that these plots represents the field strength for a pattern on the x-y plane. As the DEP force is proportional to gradient of the  $|E|^2$ , in order for

the nanowire to experience only downward DEP, the gradient along the x-y plane should be minimal in the capture area. In order to achieve more uniform field gradients an improved design with beveled edges on the alignment electrode is studied. The angle and the dimensions are shown in Fig. 4.13.

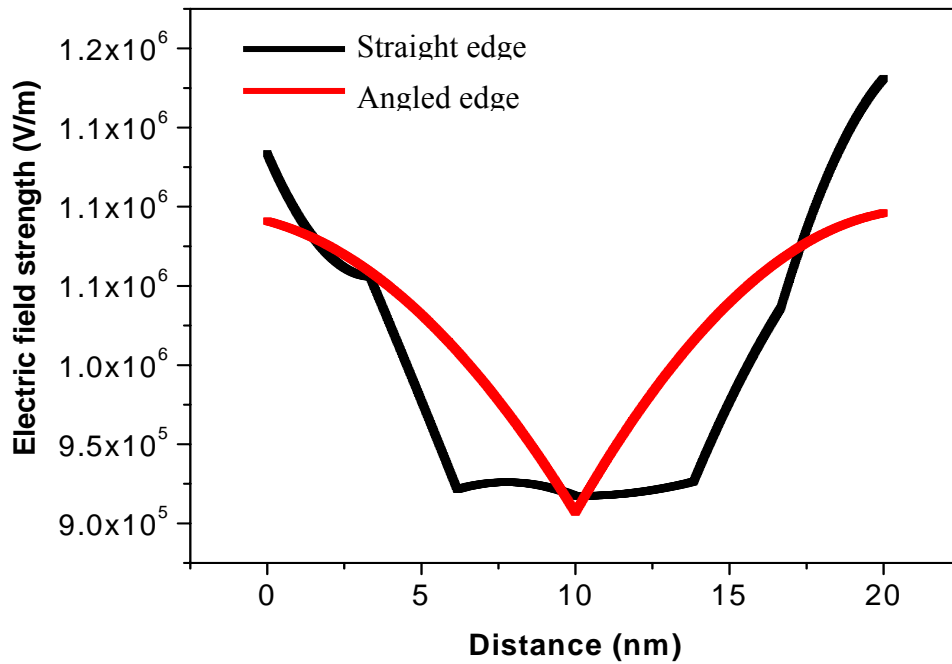


**Figure 4.13:** (a) Improved electrode design with beveled edges. (b) Dimensions and angles of the edge.

The contour plot of the field strength for the improved design is shown in Fig. 4.14. It is clear from the plot that the high field regions around the corners of the big pad areas do not exist. Also the electric field inside the capture area is much more uniform than the earlier design (inset of Fig. 4.14). The uniformity of the field is demonstrated by the 1-D line plot of the field strength (Fig. 4.15) along a line running parallel to the length of the electrodes (denoted by the dotted black lines in the insets of Fig. 4.12 and Fig. 4.14). For the angled edge design the field strength gradually changes whereas for the straight edge design the field strength sharply decays as we move away from the straight edges and attains a minimum value for majority of the central capture area.

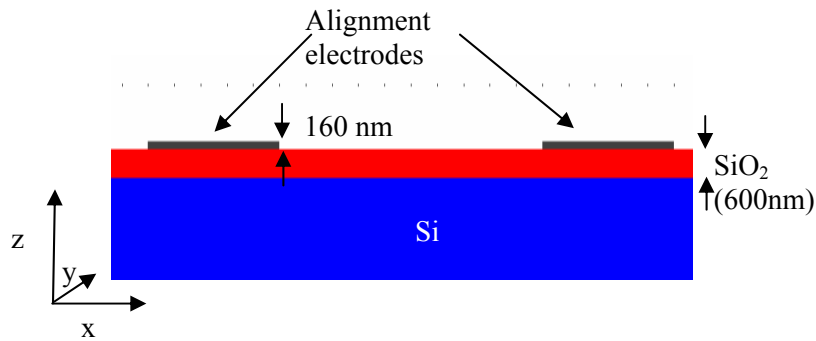


**Figure 4.14:** Electric field intensity for beveled edge design. (inset) Field intensity in the region marked by the black box.



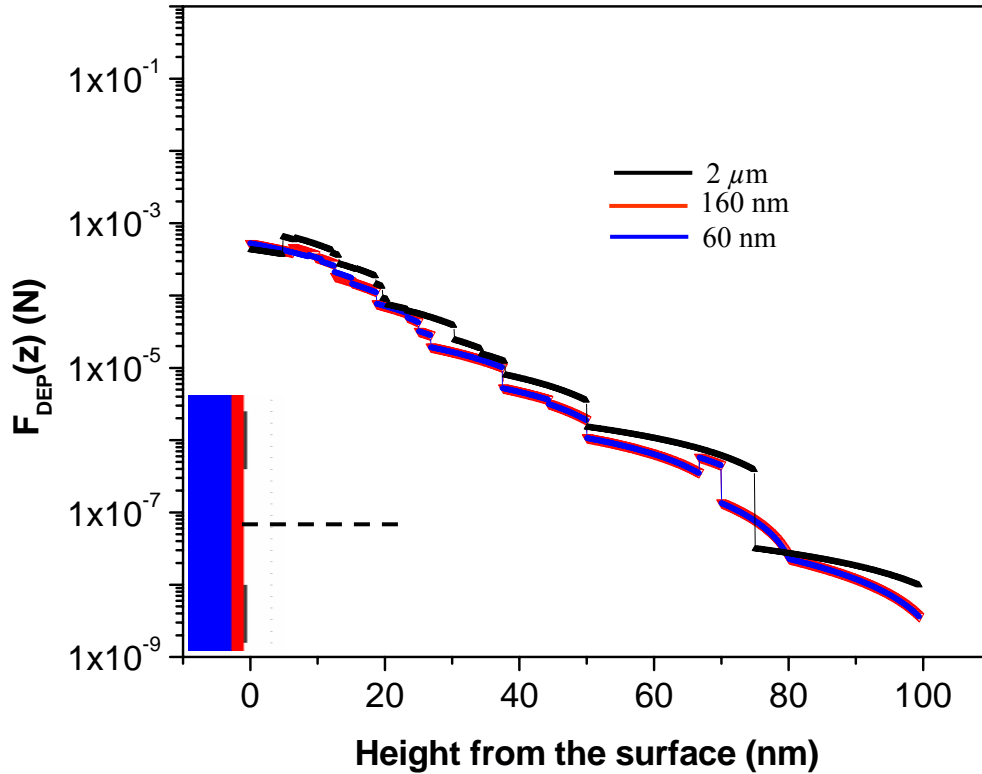
**Figure 4.15:** 1D plot of electric field intensity for straight edge and beveled edge design.

In the result section we will demonstrate the effectiveness of the beveled edge design. After the layout of the electrode is optimized, attempt was made to optimize the thickness of the electrodes. As shown before (Fig. 4.9) thicker electrodes will cause unwanted stress in the nanowire devices. In order to estimate the optimum thickness of the electrode we simulated the electric field configuration in space (z direction) above the electrodes for the geometry shown in Fig. 4.16.



**Figure 4.16:** Electrode geometry for field intensity calculation in z direction.

The plot of the magnitude of the z component of the DEP force for two different metal pad thicknesses is shown in Fig. 4.17. It is clear that there is no significant difference between  $|F_{DEP}(z)|$  for the 160 nm thick and 60 nm thick metal pads. Increasing the pad thickness to 2  $\mu\text{m}$  increased the DEP force marginally. Thick metal pads are disadvantageous as unwanted stress is developed due to bending of the nanowires at the contact edges. On the other hand very thin metal films (less than 10 nm) are not mechanically stable under the probe pressure. Ideal design would include the alignment pad deposition and then planarizing the surface with a thin layer of SiO<sub>2</sub> and exposing only the contact pads.



**Figure 4.17:** Electric field intensity as a function of the metal pad thickness in the z direction for 20 V bias applied between the pads as shown in the inset.

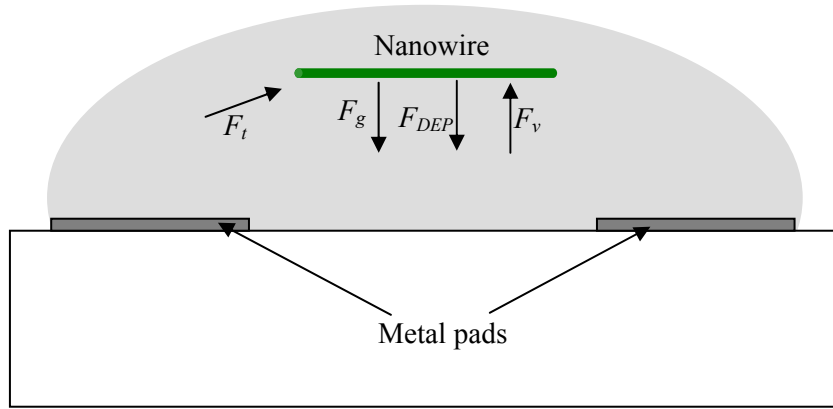
### 4.2.3 Configuration time

The time that it takes for a nanowire in the dispersion to be aligned by the DEP force field and finally settle down on the pattern is the configuration time for the process. Estimating this time is important as this gives an indication about the effectiveness of the process parameters. In order to do that one has to consider the different kinds of forces acting on the nanowire in the suspension and derive an equation of motion for the nanowire under the DEP force. It is intuitive that the nanowire will attain a terminal velocity under the DEP force. Determining this velocity will enable us to determine the configuration time. In the Fig the important forces acting on a nanowire dispersed in solvent are shown. This will be used to derive the equation of motion for

the nanowire. The force due to gravity  $F_g$  estimated for a GaN nanowire (100 nm diameter and 25  $\mu\text{m}$  length) is approximately  $10^{-15}$  N. The DEP force for the same wire is about  $10^{-5}$  N. Hence one can safely neglect the force due to gravity. For DEP force to be effective it must dominate over the random thermal motion of the particle, which can be treated as a random force whose maximum value is given roughly by [68]:

$$F_t = k_B T / \sqrt{V} \quad (4.11)$$

where  $k_B$  is the Boltzmann constant,  $T$  the absolute temperature, and  $V$  the particle volume. Considering the same nanowire with 100 nm diameter and 25  $\mu\text{m}$  length, the thermal voltage  $F_t$  at 300 K is in the order to  $10^{-15}$  N. Therefore the only two dominant forces experienced by the nanowire are the  $F_{DEP}$  and  $F_v$  (viscous drag).



**Figure 4.18:** Dominant forces acting on a nanowire floating in a suspension, with electric field applied to the alignment pads.

The equation of motion for the nanowire considering the fluid at rest is

$$m \frac{dv}{dt} = F_{DEP} - F_v \quad (4.12)$$

where  $m$  and  $v$  are the particle mass and velocity respectively. The frictional force is opposite to the DEP force and is usually given by relationship  $F_v = bv$ , where  $b$  is the friction factor. Solving this first order linear different equation we get the velocity

$$v = \frac{F_{DEP}}{b} \left[ 1 - \exp\left(-\left(\frac{b}{m}\right)t\right) \right] \quad (4.13)$$

The terminal velocity  $v_T$  is then given by

$$v_T = \frac{F_{DEP}}{b} \quad (4.14)$$

Assuming the nanowire to be prolate ellipsoid the friction factor  $b$  is given by

$$b = \frac{6\pi\eta L}{\ln(2L/r)} \quad (4.15)$$

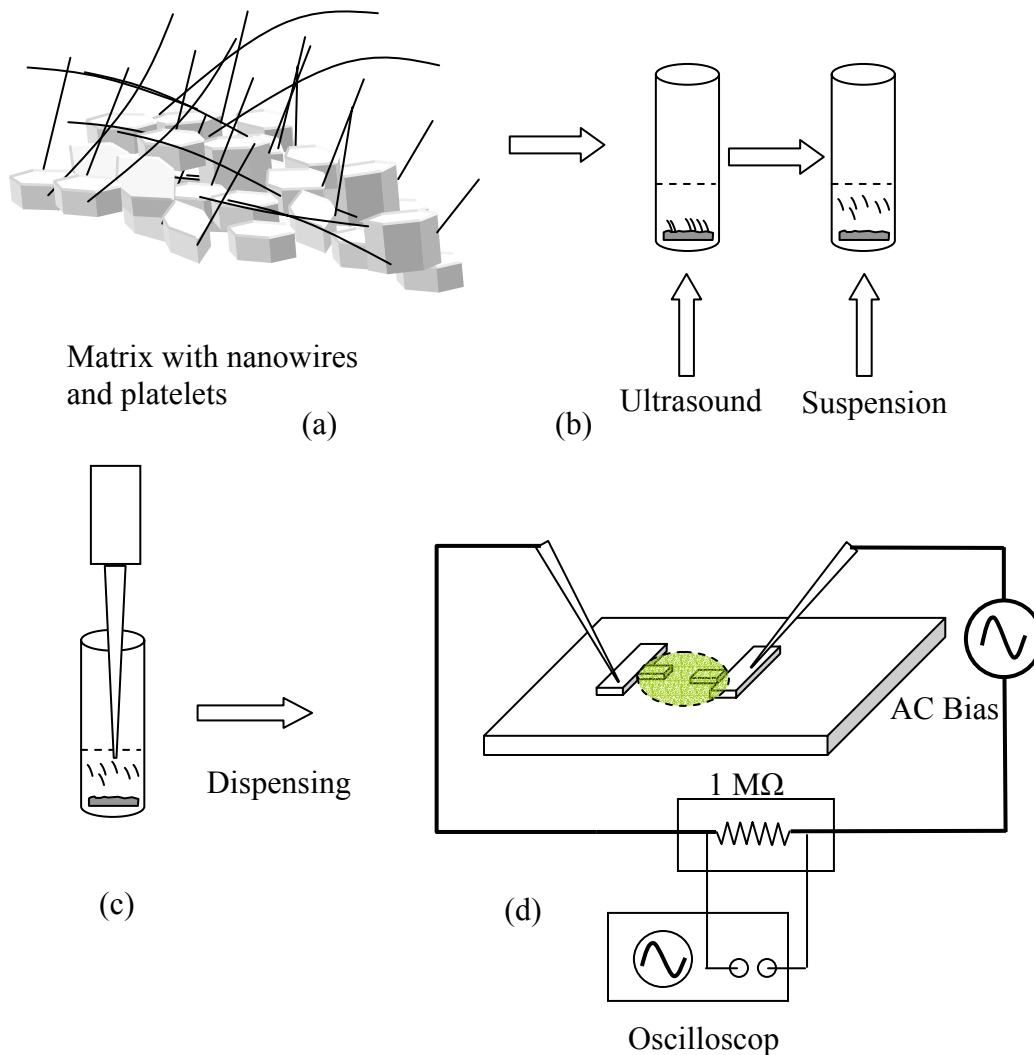
where  $\eta$  is the fluid viscosity and  $L$  is the length of the nanowire. For a nanowire (100 nm diameter and 25  $\mu\text{m}$  length) dispersed in isopropanol ( $\eta = 1.77 \times 10^{-3}$  Pa s) the terminal velocity is about 0.1  $\text{m s}^{-1}$ . If we assume that we use 10  $\mu\text{L}$  of isopropanol and using experimentally observed size of the drop on the surface (2 mm radius), we can calculate the maximum height of the nanowire in the solution which is about 800  $\mu\text{m}$ . So the reconfiguration time is about 8 ms considering  $F_{DEP}$  about  $1 \times 10^{-6}$  N. This gives us an estimate of the time during which we have to apply the bias. Generally the alignment process can be monitored by the monitoring the ac current by an oscilloscope through the circuit as will be discussed in the next section.

### 4.3 Experimental Techniques for Dielectrophoretic Alignment

The growth matrix as collected from the growth chamber is sonicated in a solvent (isopropanol) using short ultrasound pulses to create a suspension of nanowires. Two



different types of substrates were used to implement the assembly process: SiO<sub>2</sub> (600 nm, thermal oxide) coated Si substrates (n<sup>++</sup>,  $\rho = 0.02 \text{ } \Omega \text{ cm}$ , Silicon Quest International<sup>®</sup>) and (0001) oriented sapphire substrates. The substrates were cut into 10 mm  $\times$  10 mm pieces and were cleaned using standard cleaning procedure. Photolithography was carried out, followed by metal deposition and liftoff to form the alignment pads. After formation of the metal pads, the samples were coated with hexamethyldisilazane (HMDS) before dispersing the nanowires. HMDS forms a monolayer making the SiO<sub>2</sub> surface hydrophilic. This step ensures that the nanowires adhere to the oxide surface and not move during subsequent processing. The nanowires are dispersed on the sample using Hamilton<sup>®</sup> microliter syringes. Usually 10  $\mu\text{L}$  of the dispensing solution was used for the alignment. The electric field alignment was performed in a regular probe station with 7  $\mu\text{m}$  diameter W probes and the solution dispensing syringe needle is placed right over the pad area. The ac bias is applied using a Stanford Research Systems<sup>®</sup> DS360 ultra low distortion function generator. A 1 M $\Omega$  resistor is connected in series with the bias generator. This resistor serves two purposes, first it prevents large current flow through the nanowire once it bridges the gap, and second it enables us to monitor the capture process in real time without having to look through a microscope. An oscilloscope connected across the resistor would indicate the capture as it would be associated with a voltage drop across the resistor. The schematic of the dielectrophoretic alignment steps and setup is shown in Fig. 4.19.



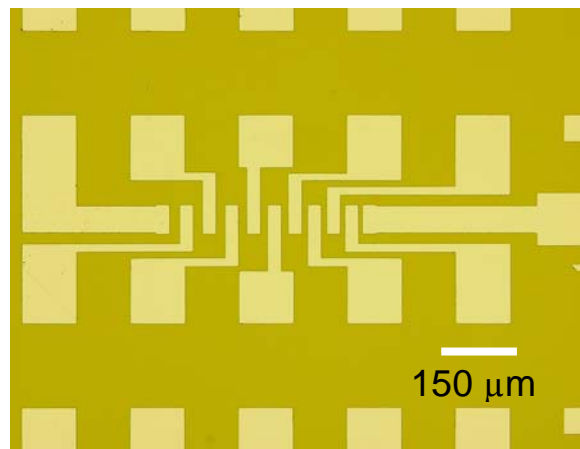
**Figure 4.19:** (a) Growth matrix, nanowires and the micro-platelets, (b) formation of the suspension through sonication, (c) dispensing the solvent, and (d) setup for DEP alignment.

These pads not only serve as alignment electrodes but the also act as bottom contacts for the nanowires. So it is necessary to select a metal scheme, which is suitable for making Ohmic contacts to the nanowire material system. Forming Ohmic contacts to nitrides require annealing at temperatures as high as 750 °C. For n type GaN, Ti/Al/Ti/Au metal scheme has been proven to be low resistance and extremely reliable [44]. For the purpose of forming the bottom contact, Au is intentionally

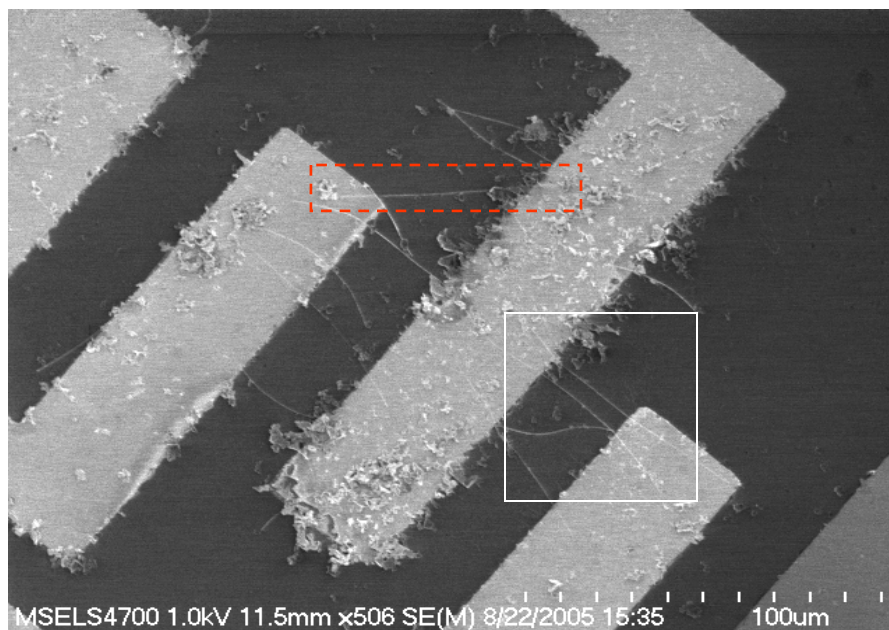
avoided from the metal stack, as otherwise the nanowire will be in direct contact with Au after bridging the alignment pads. Annealing the pads for Ohmic contact formation will form Au-GaN reaction products, which are proven to be detrimental to the contact properties [45]. Having both the bottom and top contacts for the nanowire devices not only ensures reliable device structures, but also enables us to estimate the material and contact properties more accurately [54].

#### 4.4 Results of Dielectrophoretic Alignment

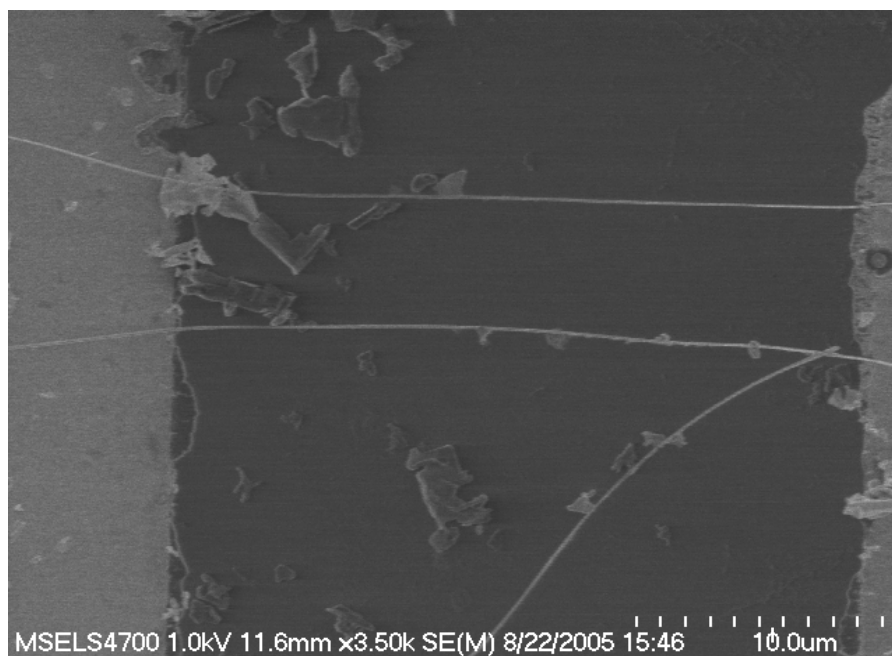
One of the two different geometries used for the alignment is shown in Fig 4.20. The first pattern is a simple interdigitated electrode array with large capture area as shown in design 1 [Fig. 10 (a)]. This was used to experimentally test the effectiveness of the DEP process. The spacings between the electrodes are 30, 28, 26, 24, 22, 20, 18, 16, 14  $\mu\text{m}$  respectively.



**Figure 4.20:** Optical microscope image of interdigitated electrode configuration as in design 1.



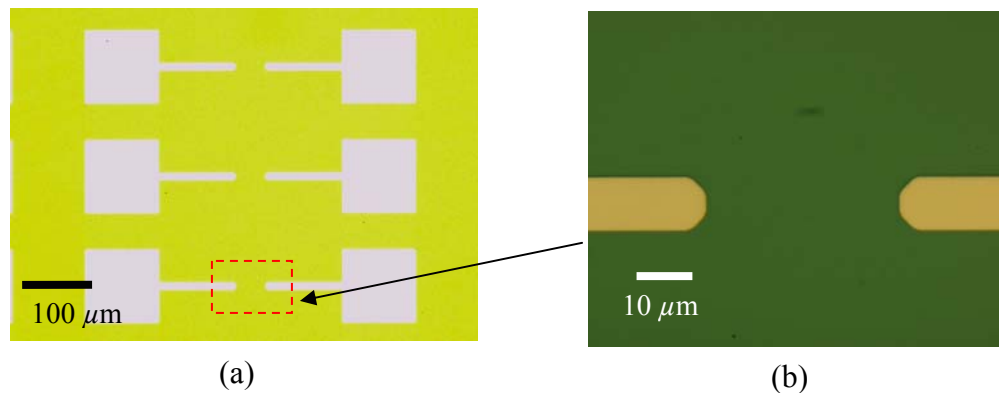
(a)



(b)

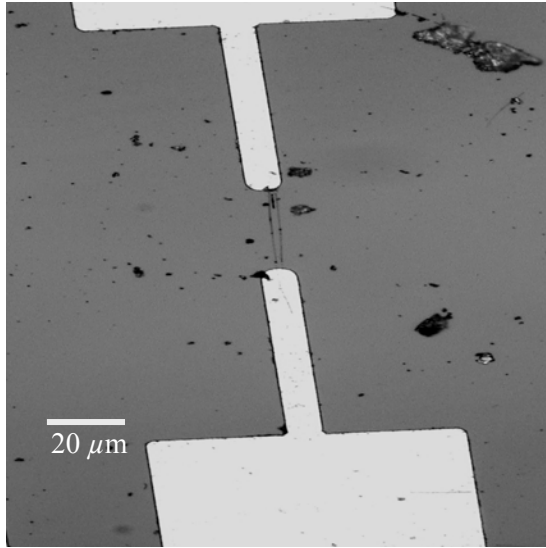
**Figure 4.21:** FESEM images of GaN nanowires aligned on Ti/Al/Ti pads using DEP force (a) nanowires aligned using 1 KHz 20 volt peak-to-peak ac signal (b) Magnified image of the area surrounded in (a) with the white box.

Fig. 4.21 is the FESEM scan of aligned nanowires utilizing 1 KHz, 20 volts peak-to-peak ac signal applied between the adjacent pads. The best possible alignment is obtained utilizing 1 KHz alignment frequency. As predicted by electrostatic simulation (Fig. 4.11) the fringe fields are strong enough to capture nanowires (shown by the red broken box in Fig. 4.21 (a) with a nanowire within the box). Although devices have been successfully realized using this pattern, a better design implementing the beveled edges as shown in Fig. 4.2 is realized. Figure 4.22 shows the optical image of the beveled edge alignment pads. Variations of this configuration result in different types of devices such as FET, four-terminal measurements.

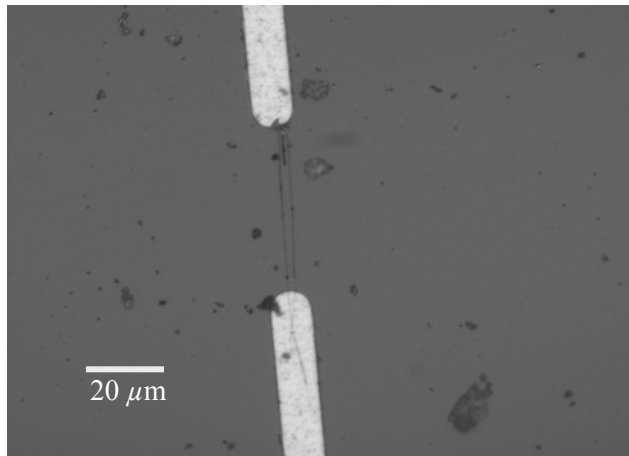


**Figure 4.22:** (a) Optical microscope image showing basic structure of the design 2, (b) Magnified image of the area surrounded in (a) with the red box, the beveled edges can be clearly seen.

The alignment results are significantly improved with this new design. As the capture area is smaller more precise alignment (where only one or at most two wires are present) is obtained (Fig. 4.23). As the electrostatic simulations predicted that the fringing fields are minimal in this design (see Fig. 4.14) we do not generally observed nanowires outside the designed capture area.



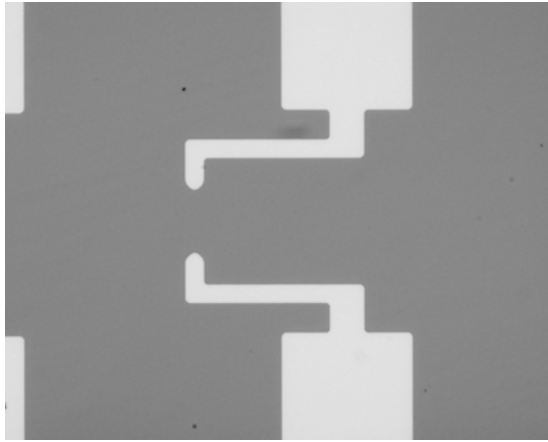
(a)



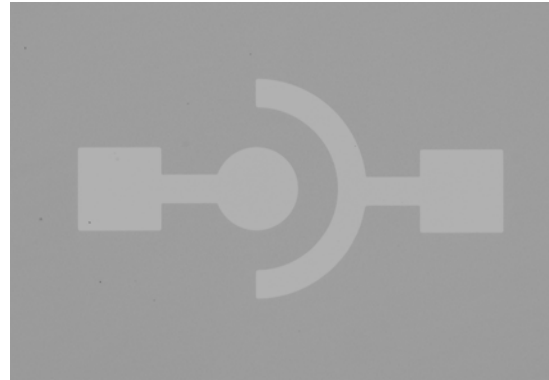
(b)

**Figure 4.23:** (a) Optical microscope image showing two nanowires captured with 12 V peak to peak ac bias (1 kHz frequency) (b) High magnification of the image in (a).

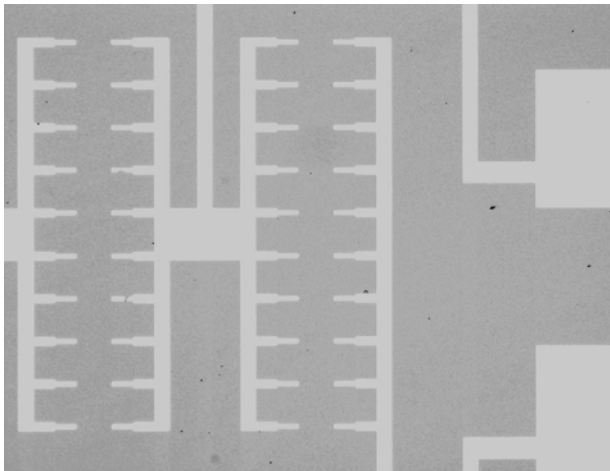
The variations of the basic designs are shown in Fig. 4.24. The circular alignment electrode design shown in Fig. 4.24 (b) is useful for top-gate FET transistors as will be shown in the next chapter. The array design is desirable if we want to realize sensing architectures with multiple nanowires aligned in parallel in a array fashion to increase the sensing surface area and hence output signal.



(a)



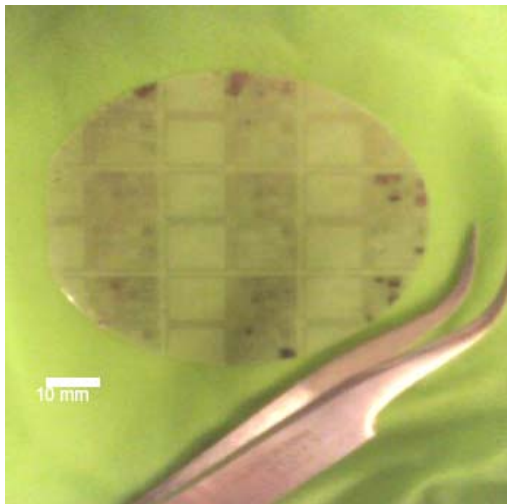
(b)



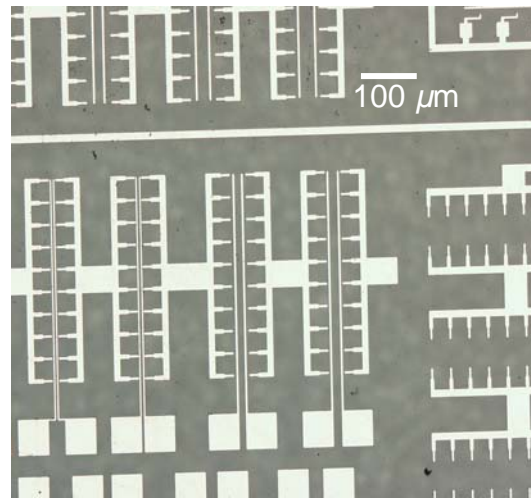
(c)

**Figure 4.24:** (a) Optical microscope image of modified pattern for design 2, (b) circular electrode design, and (c) array geometry.

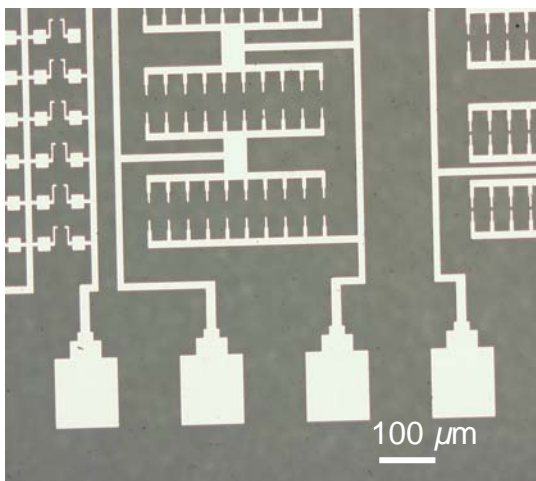
The mask layout combining the new design is for a full two inch wafer (Fig. 4.25). So, ideally one can perform the alignment over the entire wafer all at once. The array patterns are connected by a bus line which carries the bias from the outer pads to the patterns inside the wafer.



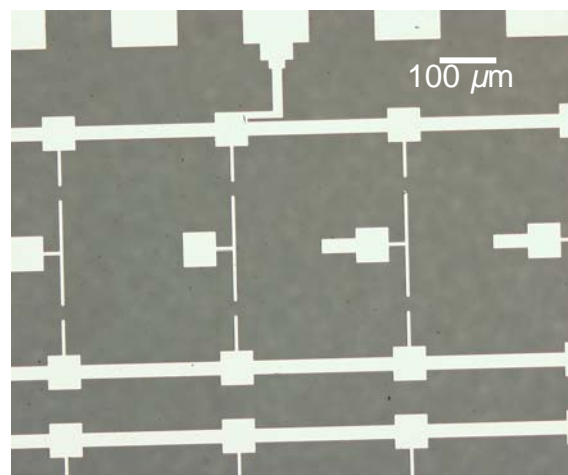
(a)



(b)



(c)



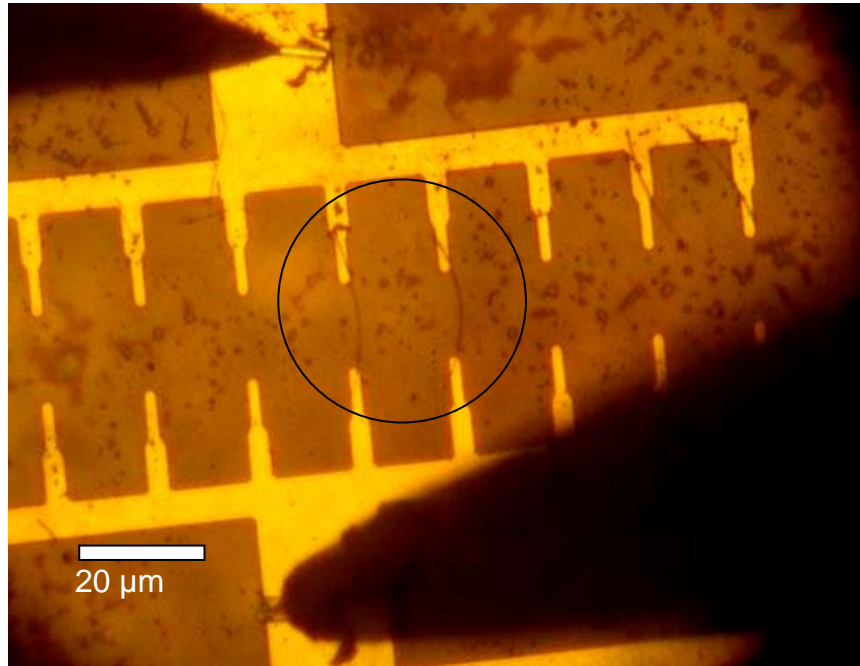
(d)

**Figure 4.25:** (a) Optical microscope image of full 2 inch sapphire wafer with alignment electrodes, (b) four-terminal structures, (c) bus lines carrying connecting the bias pads with the array patterns, and (d) pattern for realizing logic gates.

The alignment of nanowires using an array pattern in a probe station is shown in Fig. 4.26, where two nanowires are clearly seen captured by the alignment process. This type of structure is especially suitable when we are trying to get multiple nanowires channels such as in sensors and optical emitter/detector arrays. Both the density of



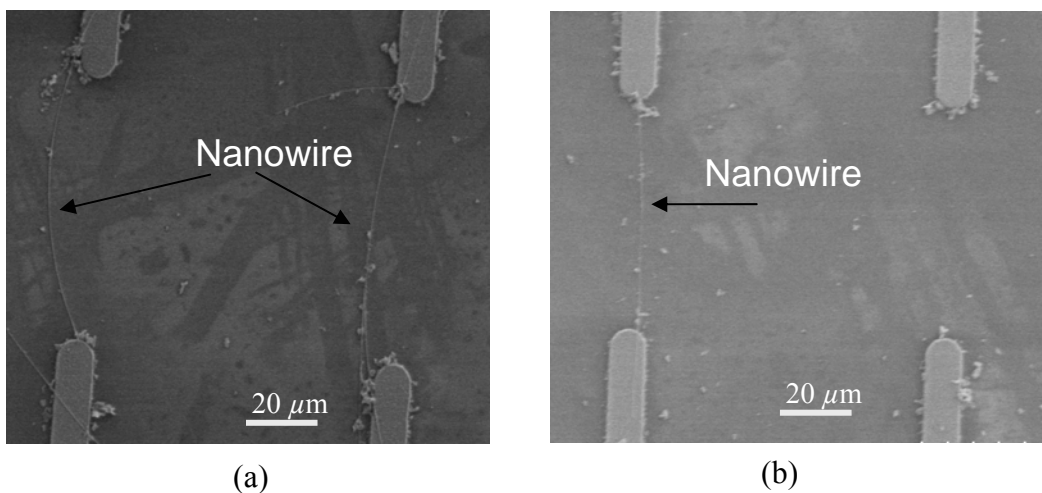
nanowires in the suspension and the field strength determines the capture efficiencies for the array design.



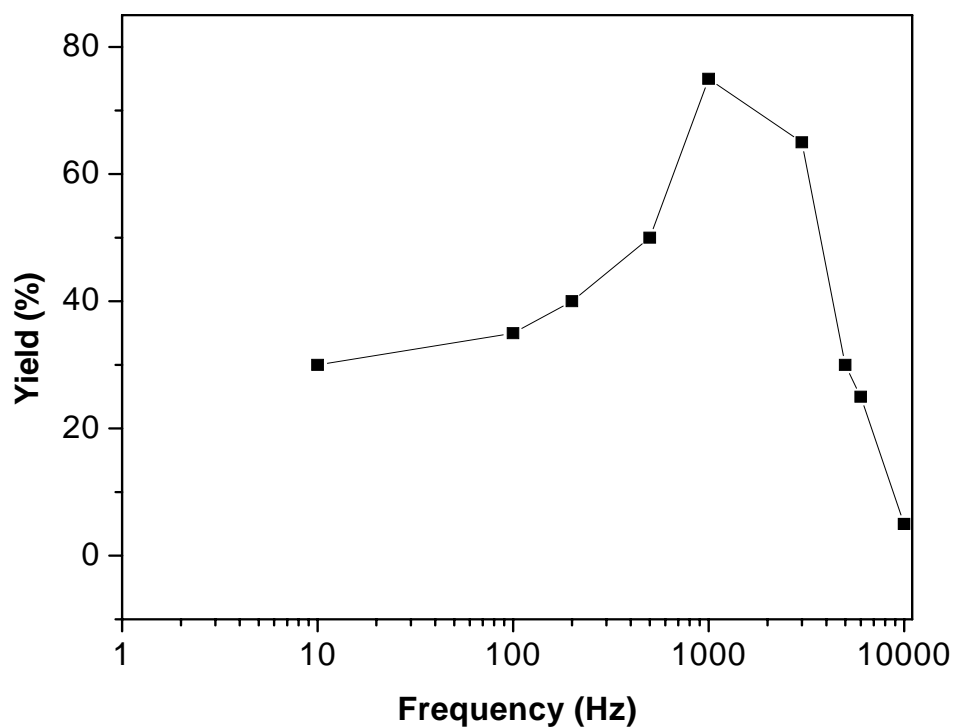
**Figure 4.26:** Optical microscope image of nanowires after alignment in a array pattern, the nanowires are seen inside the black circle and the tips of the probes on two sides are also visible.

This present design is clearly superior as it allows for better control and accuracy for placement of the nanowires. The control and accuracy is clearly demonstrated in Fig. 4.27 (a) and (b). Using optimized process parameters we were able to discriminate the placement of nanowires within 100 μm.

This process is highly reproducible. The yield of this process with the new design as a function of the applied bias frequency is shown in Fig. 4.28.

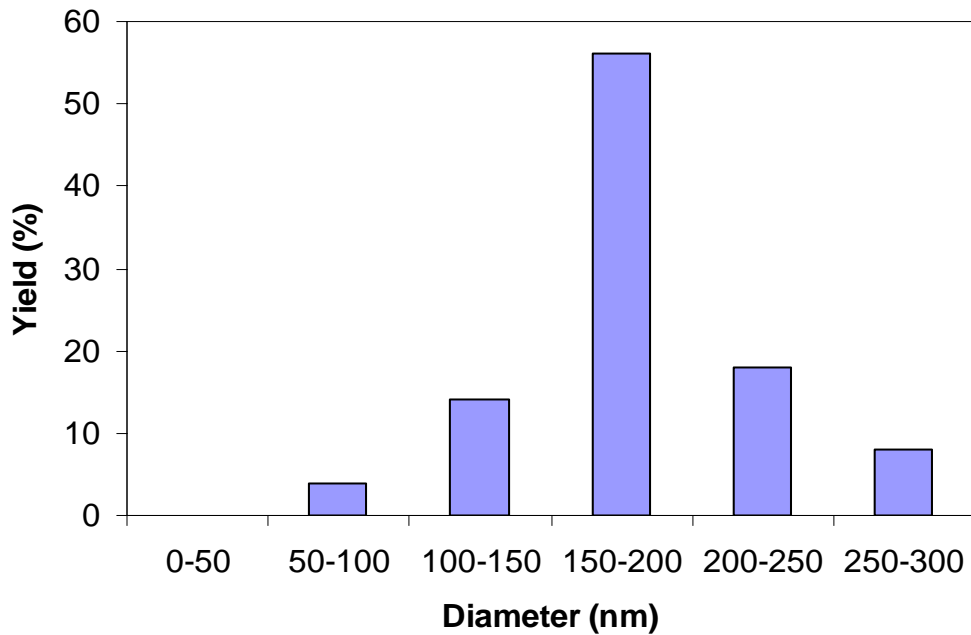


**Figure 4.27:** (a) FESEM image of two nanowires captured on two adjacent patterns by applying the same bias to both, (b) FESEM image of nanowire on aligned one pattern, the adjacent pattern was not biased. This clearly demonstrates the effectiveness of the present design in controlled placement of the nanowires. The bias and frequency of the applied voltage used for this process was 12 V peak to peak and 1 kHz respectively.



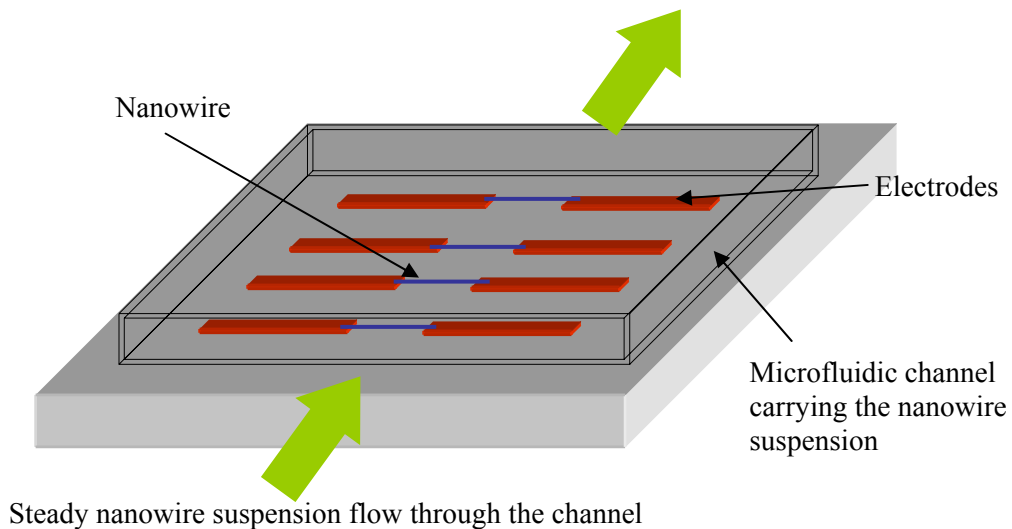
**Figure 4.28:** Plot of experimental yield of alignment as a function of applied bias frequency. The voltage is kept constant at 20 V peak to peak, and the electrode separation is 20  $\mu\text{m}$ .

The plot shows that at low frequencies the yield is often low as strong dc field are cause various unwanted effects like electrophoresis, convection flow due to localized heating, which adverse effect the alignment yield. The yield reaches maximum at 1 kHz frequency and decreases with increasing frequency as expected from plot. The yield is also a complex function of the voltage of the applied bias. Strong field are capable of attracting more than one nanowire thus increases the yield but decreases the alignment precision. Strong fields would also attract the microfragments. The density of the nanowires in the dispersion solution affects the alignment yield and presence of microfragments on the substrate. Thus alignment process is complex balance of density of nanowires, alignment voltage, and the frequency.



**Figure 4.29:** Plot of experimental yield of alignment as a function of nanowire diameter. The voltage is kept constant at 20 V peak-to-peak, the electrode separation is 20  $\mu\text{m}$ , and the frequency 1 kHz.

The experimental plot of the alignment yield as a function of nanowire diameter (Fig. 4.29) shows qualitative argument with the yield factor prediction (see Fig. 4.4). This type of calculation is quite effective in estimating the nature of alignment.



**Figure 4.30:** Schematic representation of advanced DEP technique where a micro-fluidic channel carrying nanowire suspension is placed right over the alignment electrodes.

Improving the alignment precision and yield would require tighter control of the nanowire dimensions and also implementing various techniques to control the movement of the nanowires due to random fluid movements. Placing a microfluidic channel carrying the nanowire suspension over the alignment electrode (as shown in Fig. 4.30) would improve the yield and accuracy of the DEP process by minimizing unwanted fluid movements.

## **Chapter 5: Fabrication of Nanowire Devices and Process**

### **Optimization**

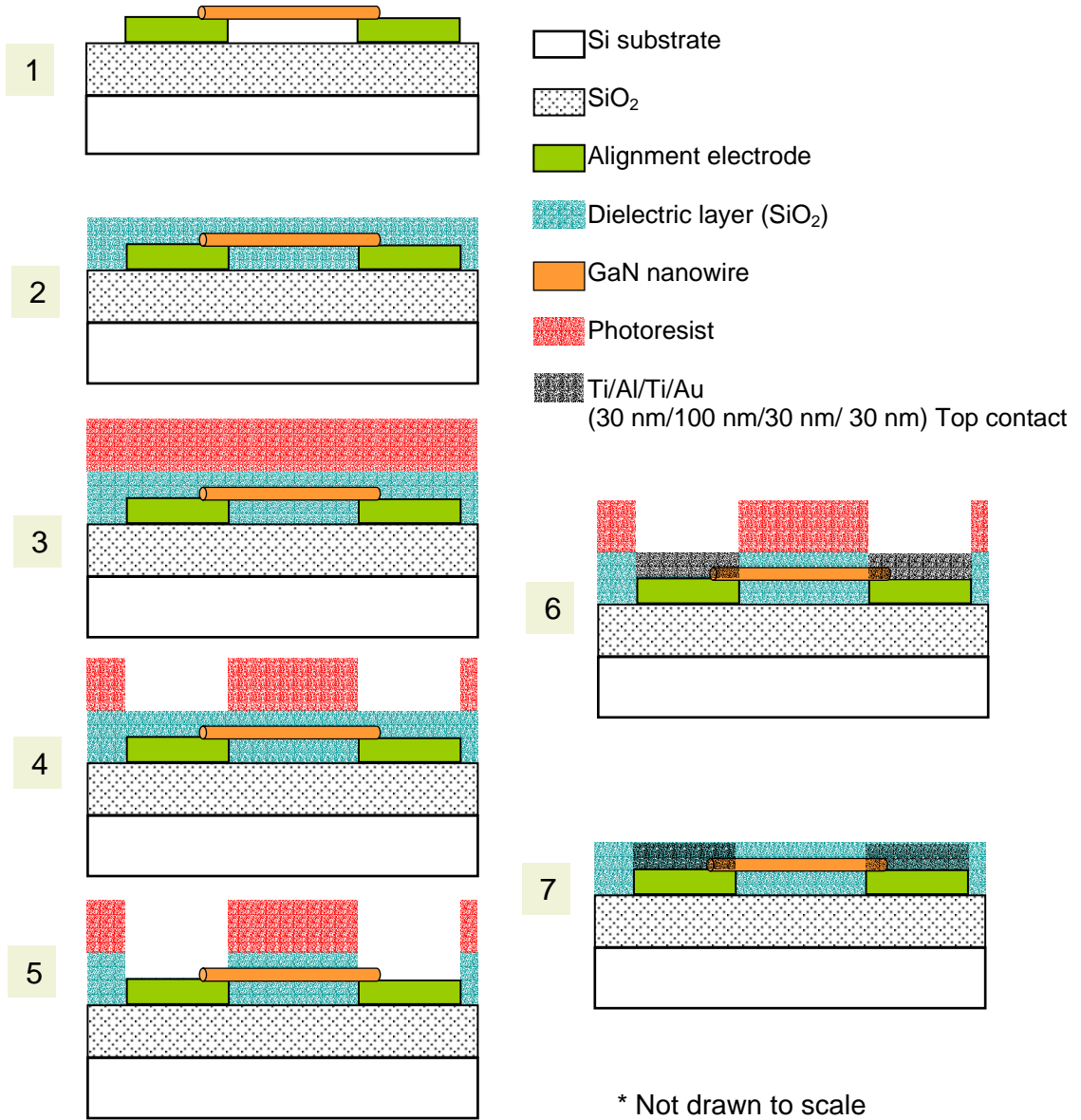
#### **5.1 General Fabrication Scheme**

The key issues in successfully realizing nanowire devices are yield and reproducibility. All of the earlier papers reporting nanowire FETs used e-beam lithography, FIB techniques, or AFM manipulation. In order to develop rapid prototype device structures, a general fabrication technique is needed with desired characteristics such as:

- (a) batch fabrication
- (b) Si microfabrication technology compatible
- (c) suitable for any nanowire material system
- (d) suitable for any type substrate

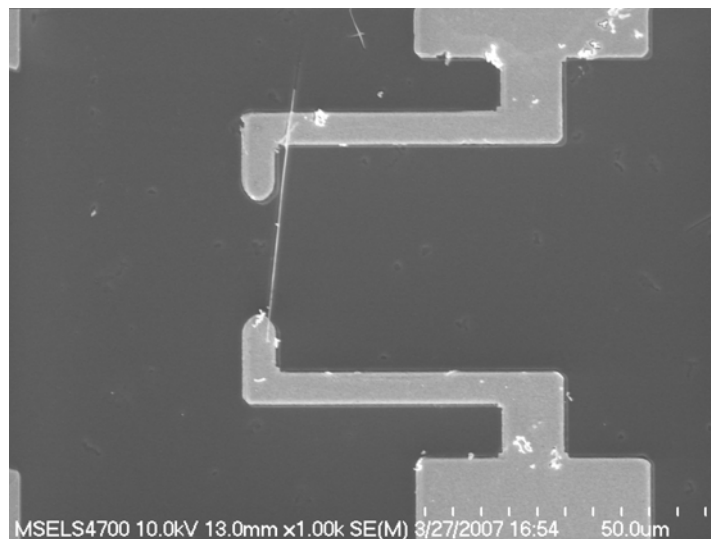
We have developed a fabrication technique which poses all the above mentioned characteristics. The schematic of the fabrication sequence is presented in the Fig 5.1. It starts with nanowires assembled on Ti/Al/Ti alignment electrodes. After the alignment is complete, the sample is cleaned using oxygen plasma (25 % O<sub>2</sub> in Argon, 20 mTorr, 50 W, 1 min) to remove the organic residue left after evaporation of the solvent. The sample is then annealed using a rapid thermal annealer at 500 °C for 30 sec in ultra high purity argon (1<sup>st</sup> step anneal). This annealing step ensures that the contacts between the nanowires and the alignment pads are mechanically stable. Using plasma enhanced chemical vapor deposition (PECVD) technique, 30 nm-50 nm of SiO<sub>2</sub> is deposited on the sample with the substrate temperature kept at 300 °C.

After the oxide deposition, a second photolithography was performed to align the same pattern on the sample.



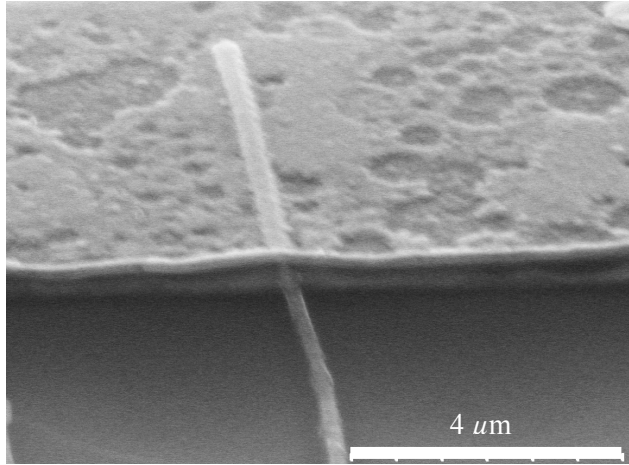
**Figure 5.1:** Schematic representation of the complete fabrication process flow for realizing nanowire devices, which are aligned on pre-determined positions on a substrate utilizing dielectrophoretic force.

Etching the oxide through the photoresist mask in buffered HF etching solution is performed to open the windows on the SiO<sub>2</sub> right over the preexisting alignment metal pads. A metal deposition was followed with a liftoff in acetone. The deposition sequence is Ti/Al/Ti/Au (300 Å/ 1000 Å / 300 Å/ 300 Å) with Au being the topmost layer. The sample is then annealed in UHP Ar at 500 °C to 750 °C for 30 s (2<sup>nd</sup> step anneal). Figure 5.2 is a SEM image of a complete nanowire device fabricated utilizing the above mentioned process. In Fig. 5.3 a nanowire is seen in between the bottom and the top metal contacts. The PECVD oxide is etched for SEM imaging purposes.



**Figure 5.2:** SEM image of complete nanowire device with source and drain contacts.

This process results in the robust nanowire device structures, which are embedded in a protective PECVD SiO<sub>2</sub> layer. This oxide can be removed for specific device applications like sensor arrays or detectors etc. Without the oxide coating, some nanowires were detached from the substrate during the lift off for the second metal pad.



**Figure 5.3:** SEM image showing a nanowire with both top contact and bottom alignment electrode.

The yield of the nanowire devices with the PECVD oxide coating was close to 80 percent. Variations of this fabrication process results in different device types. For a top gate transistor, we could use the passivation layer as the gate dielectric and deposit a metal gate in between the two Ohmic contacts.

## **5.2 Process Optimization**

The general fabrication sequence described above involved various steps which needed to be optimized for the GaN nanowires. Below we describe the optimization procedure that was done to increase the yield of the fabrication procedure.

### **5.2.1 Choice of Substrate**

Although any substrate can be used for the alignment purpose, subsequent annealing step and the type of application determines the choice of substrates. It was revealed that using thick Si substrates with SiO<sub>2</sub> resulted in the largest yield. Sapphire substrates had equal device yields before annealing, but after the annealing step, 50%



of the operating devices failed. This could be explained by looking at the linear thermal expansion coefficients ( $\alpha_T$ ) of different materials presented in table 5.1.

**Table 5.1:** Linear thermal expansion coefficients of different materials.

Material	Linear thermal expansion coefficient $\alpha_T$ ( $K^{-1}$ )
GaN	$5.59 \times 10^{-6}$ (along a-axis)
Si	$2.5 \times 10^{-6}$
SiO <sub>2</sub>	$0.5 \times 10^{-6}$
Al <sub>2</sub> O <sub>3</sub>	$0.03 \times 10^{-6}$

The strain generated in film on a substrate due to change in the temperature is roughly given by the relationship:

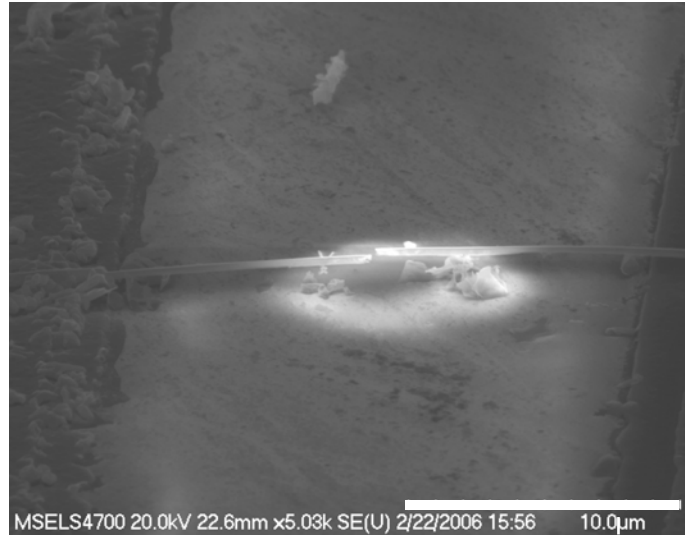
$$\varepsilon_f = (\alpha_{fT} - \alpha_{sT})(\Delta T) \quad (5.1)$$

where  $\varepsilon_f$  is the strain developed in the film,  $\alpha_{fT}$  and  $\alpha_{sT}$  are film and substrate linear thermal expansion coefficients, and  $\Delta T$  being the temperature change. Let us consider the thermal annealing step at 500 °C. Hence the strain developed in a GaN nanowire ( $\varepsilon_{nw}$ ) on a sapphire substrate due to the thermal annealing ( $\Delta T \approx 473$  K) is about  $2.6 \times 10^{-3}$ . As the nanowires are one-dimensional structures, this would result in a uni-axial stress, which is given by:

$$\sigma_{nw} = Y_{GaN} \times \varepsilon_{nw} \quad (5.2)$$

where  $\sigma_{nw}$  is the uni-axial stress,  $Y_{GaN}$  the young's modulus for GaN (181 GPa). Using Eq. 5.1 and 5.2 we calculated the stress in the nanowire resulting from the annealing step, which is approximately 476 MPa. The yield stress for GaN thin films are approximately 100 MPa – 200 MPa [69]. The stress generated due to annealing is much higher than the yield stress for GaN. Hence it is not surprising that the nanowire

devices could suffer fracture due to the thermal stress developed during annealing as shown in Fig. 5.4.



**Figure 5.4:** FESEM image of the nanowire with end contacts after annealing of the 2nd metal stack. The break in the nanowire is clearly visible, which is probably caused by the thermal stress during annealing. This nanowire is aligned on a sapphire substrate with no PECVD protective oxide coating.

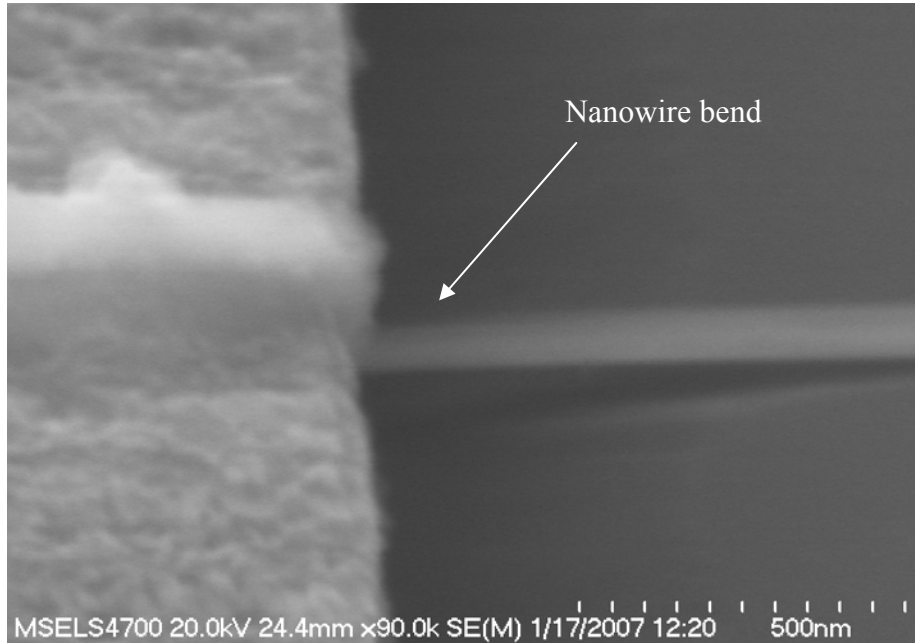
For Si substrate the stress generated in the nanowire for the same annealing temperature is about 260 MPa, which is about half of the stress generated for a sapphire substrate. Stress level during annealing is still present for the case of Si substrate, which could be reduced by changing the annealing rate.

Also, for the temperature dependent device characteristics measurements, using Si substrates was more effective as the nanowire devices stabilized to the substrate temperatures faster than the sapphire substrate.

### 5.2.2 Alignment Electrode Thickness

As described in the last chapter, the thickness of the first level alignment electrodes does not influence the alignment force significantly, but during the process of

alignment thin metal layers (<10 nm) tend to peel off under the probe pressure. On the other hand thick metal pads create unwanted stress in the nanowire due to bending as they cross from the metal contacts to the substrates (as shown in Fig 5.5).



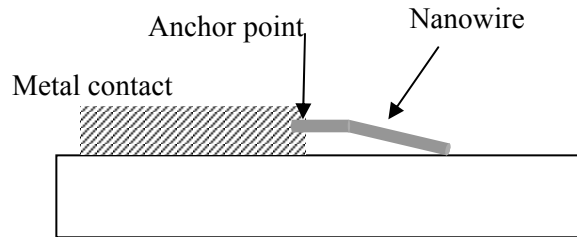
**Figure 5.5:** FESEM image of a nanowire with top and bottom contacts with a bend caused by the bottom electrode.

Accurately calculating the stress developed in the nanowire due the bending at the metal contact edge is difficult, but one can estimate approximately the stress in the nanowires by approximating the nanowire as a thin long rod and applying the Euler-Bernoulli beam equation [70]. The bending stress  $\sigma_{bending}$  in a rod which is cantilevered as shown in Fig. 5.6 is given by the relationship [70]

$$\sigma_{bending} = \frac{My}{I} \quad (5.3)$$

where  $M$  is the bending moment,  $y$  is distance from the neutral axis, and  $I$  is the second moment of area. For a circular rod with diameter  $d$  this is simplified as:

$$\sigma_{bending} = \frac{M}{\left(\frac{\pi d^3}{32}\right)} \quad (5.4)$$



**Figure 5.6:** Schematic representation of a nanowire cantilevered from a contact. The nanowire is bent at the anchor point.

In this case we are assuming that the wire is bending due to its own weight, which is uniform along the length of the nanowire. From the Fig. 5.5, it is easy to estimate the angle of the bend, and hence the bending moment for a nanowire with 200 nm diameter over a metal thickness of 160 nm. The bending stress estimated for a 200 nm diameter nanowire coated with PECVD oxide is about 2 Pa.

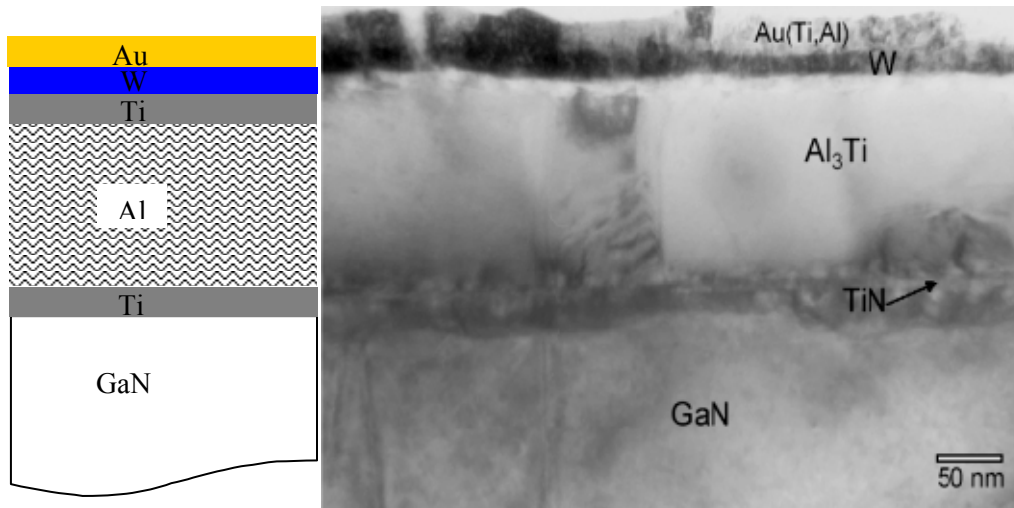
Annealing might cause an increase in the stress, resulting in a fracture in the nanowire at the stress points. Reducing the thickness of the first level metal from 160 nm to 30 nm increased the device yield by 20%. Also, it was revealed that there is no significant variation in the device performance, when using just Ti as the first level metal instead of using Ti/Al/Ti.

### 5.2.3 Metal Contact Schemes

General metal contact schemes to semiconductors often use multilayer stacks with each layer satisfying a definite purpose. The first layer which is in contact with the semiconductor is called the contact layer, and it is often a metal which has good sticking coefficient to the semiconductor surface. The work function of the contact metal has to be matched closely with the electron affinity of the semiconductor to form low resistance contacts. The second metal layer with low resistivity is used to reduce the bulk resistance of the contact. A top metal layer, usually Au for compound semiconductors, which prevents the contacts from oxidation and corrosion, is deposited at the very end. For semiconductor-metal contacts requiring high temperature processing to reduce their contact resistance, a diffusion barrier layer is placed between the top layer (Au) and the bulk layer to minimize diffusion (both in and out diffusions) between the metal layers [Fig. 5.7(a)].

Titanium and aluminum based metallization schemes have been successfully used to form Ohmic contacts to GaN. For n-GaN Ti with a work function of 4.33 eV is the closest match to the electron affinity of GaN, which is about 4.1 eV. Ti provides good adhesion to the GaN surface, producing reliable and reproducible lift-off. GaN surfaces have a very high chemisorption affinity for oxygen. As a result, a native oxide is usually always present on the surface of GaN. This layer acts as an insulating barrier between the metal and the semiconductor. Ti is especially advantageous because Ti can reduce the GaN native surface oxide upon alloying. Ti has the ability to dissolve small amounts of oxygen and still remain in stable  $\alpha$ -Ti phase with oxygen in solid solution with the metal. Solid phase reactions between Ti

and GaN forming TiN is possible since the heat of formation of TiN and GaN are 2265 and 2110.9 kJ mol<sup>-1</sup>, respectively. During annealing N out-diffuses from the GaN lattice to form TiN and nitrogen vacancies are formed in the GaN without decomposing the crystal structure. N vacancies act as shallow donors in GaN. The interfacial region thus becomes heavily doped, reducing the contact resistance. The existence of a thin TiN layer at the interface between the metal contact and GaN has been observed by a transmission electron microscope as shown in Fig. 5.7(b). Al is used as a bulk current carrying layer in Ti/Al based contacts.



**Figure 5.7:** (a) Schematic representation of different metal layers in a standard Ti/Al/Ti/Au metal contact to n-GaN, (b) Cross sectional TEM image of a Ti/Al/Ti/W/Au contact to n-GaN, annealed at 750 °C for 30 s in rapid thermal annealed in argon. The bulk layer is Al<sub>3</sub>Ti which is the reaction product of the Ti/Al/TI layer. In this design an extra barrier metal (W) is incorporated in the standard metallization. The W layer is clearly seen to be intact after the annealing. This advanced metallization is capable of withstanding operating temperatures in excess of 400 °C [71].

There are few problems associated with Ti/Al based contacts: (a) out-diffusion of Ti/Al, (b) rough morphology, and (c) oxidation of both Ti/Al. Rough morphology of

Ti/Al based contacts result from melting of Al during annealing (melting point of Al is 660 °C). In order to minimize the oxidation of the Ti–Al alloyed contacts and out-diffusion of the metals, a barrier layer is usually incorporated between the top Au layer and Ti/Al layer. In previous studies, metals such as Ni and Pt, which are resistant to oxidation, were placed on the top of the Ti/Al contacts to prevent the oxidation of the contacts during alloying. These metals are not efficient as barrier layers as Ti/Al still could diffuse out through these barrier layers. The present contact scheme uses a reactive barrier layer which is a Ti layer placed on the top of the standard Ti/Al layer. As a result, during high temperature annealing (750 °C), the Ti and Al layers are expected to undergo enhanced reactions producing  $Ti_xAl_{1-x}$  intermetallic alloys. Such an alloy produces low resistance contacts. Formation of these intermetallic alloys are extremely beneficial, as this reduces free Al and Ti concentrations in the layer and these intermetallic alloys are also thermally stable. This results in a low resistance and extremely reliable Ohmic contact to n-GaN. Low specific contact resistance in the range of  $3.0 \times 10^{-6} \Omega \text{ cm}^2$  has been obtained for this metallization scheme.

#### **5.2.4 Annealing Process**

In order to reduce contact resistances of Ohmic contacts to GaN layers, a rapid thermal annealing step is usually employed after the metal contacts are deposited. This step produces the necessary reactions between the metals and the nitride to form a low resistive contact. Lowest specific contact resistance obtained from Ti/Al/Ti/Au (30nm / 100 nm / 30 nm / 30 nm) contact was  $3.0 \times 10^{-6} \Omega \text{ cm}^2$ , after annealing at 750 °C for 30 s in argon. In a rapid thermal annealer, the sample is placed inside a thin

quartz chamber with halogen lamps surrounding it. As the volume of the chamber is small, the rise rate is extremely high. Rise rate of 25 °C/s is usually used for thin film nitrides. Numbers of working nanowire devices were quite low when we used standard rise rate. Rapid rise in temperature during annealing generates stress in the nanowire devices. As these nanowires are embedded in a oxide with two ends anchored to the metal contacts, there should be a critical stress limit after which the nanowires suffer structural breakdown. As Eq. 5.1 suggests that the stress generated is proportional to the temperature difference, one can reduce the thermal stress by reduce the rise rate. A slower rise rate ensures that the substrate and the nanowire are given enough time to equilibrate, hence the stress levels are always kept below the critical limit. Table 5.2 shows the effect of rise rate on the overall device yield.

**Table 5.2:** Rise rate for the metal contact annealing, and corresponding device yield.

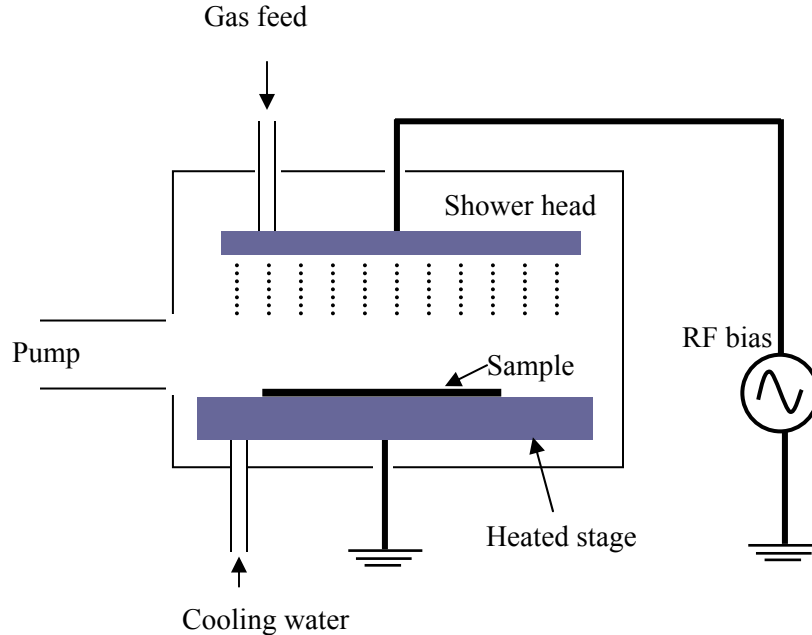
Rise rate (°C/s)	Device yield (%)
25	10
15	20
1.6	70

### 5.2.5 Passivation Techniques

In order to deposit a passivation/encapsulation layer, it is important to select a deposition process that is compatible with the GaN nanowires. General chemical vapor deposition (CVD) techniques used for deposition of SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> uses high temperatures (700 – 900 °C) to dissociate the precursor gases. GaN nanowires would not be able to withstand temperatures as high as that. Plasma-enhanced chemical vapor deposition (PECVD) is a technique commonly used in microfabrication to



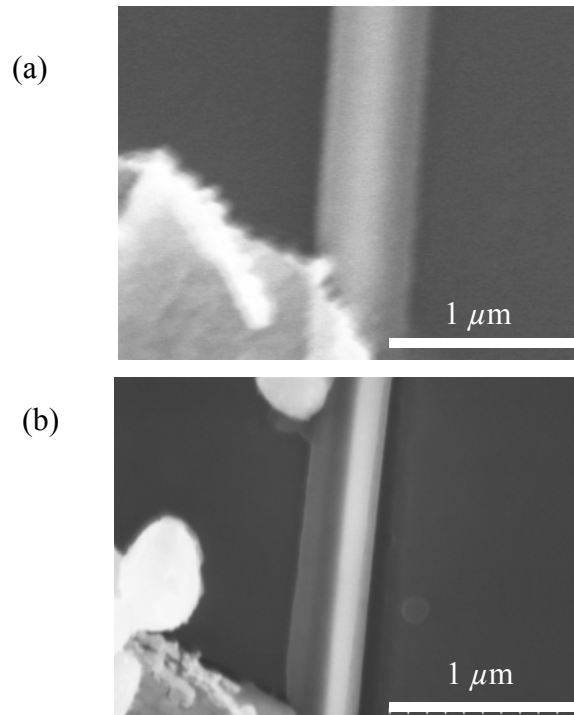
deposit layers of insulating materials and amorphous or polycrystalline silicon. PECVD uses energetic electrons from the plasma to dissociate the precursor gases. The PECVD system uses the parallel plate capacitor geometry to produce the plasma discharge. The top electrode has a fine showerhead through which the reactant gases are introduced into the chamber (Fig. 5.8). The sample is placed on a heated stage (300 °C) inside the chamber under vacuum. Radio frequency (RF) ac voltage (13.5 MHz) is applied on to the top electrode, while the sample grounded. For producing and sustaining the plasma, a critical pressure is required inside the chamber.



**Figure 5.8:** Schematic diagram of PECVD system.

PECVD is relatively cold process with deposition temperature kept at 300 °C. Another advantage of PECVD films is that they are less stressed than CVD films. Thus PECVD films would be helpful in reducing the stress in these nanowire devices. There are few disadvantages also associated with PECVD films. Just like CVD techniques they do form conformal deposits (conforming to the contour of the

depositing surface. Although PECVD oxides can not be deposited on the underside of the nanowire, from Fig. 5.9 we can say the top coating conforms quite well with the nanowire.



**Figure 5.9:** (a) SEM image of nanowire with the 200 nm PECVD SiO<sub>2</sub>, (b) same nanowire with the oxide removed.

Leakage current through these PECVD oxides are known to be higher than high temperature CVD processes. This is generally not a problem for our case as we have used more than 40 nm thick oxide layers. It will be shown later that the leakage current through these oxides are marginal compared to the device currents. Thus the SiO<sub>2</sub> deposited using PECVD could be used as a gate dielectric for nanowire field effect transistors. The process parameters and conditions used to deposit SiO<sub>2</sub> for this study are shown in table 5.3.

**Table 5.3:** Deposition parameters for PECVD SiO<sub>2</sub>.

Base pressure (Torr)	Deposition temperature (° C)	Gas flows (sccm)		RF power (W)	Deposition rate (Å/s)
		SiH <sub>4</sub> (10%)	N <sub>2</sub> O <sub>2</sub>		
900	300	400	900	30	14.5

Advanced techniques such as atomic layer deposition, pulsed laser deposition, etc are capable of depositing conformal high k dielectric materials. These techniques together with advanced materials will be necessary to realize high performance nanowire devices.

## Chapter 6: GaN Based Nanowire Electronic Devices

The fabrication sequence discussed in the earlier chapter presents a very general route for realizing stable contacts to the nanowires with reliable electrical properties. It is important to extensively characterize these devices, as developing nanosystems would involve complete understanding of the electric transport properties of these devices.

Nanowire electronic devices have various usages:

1. Sensors: chemical/biological sensors, gas sensors, pH sensors etc.

Nanowire devices are well suited for the sensing applications as the surface effects dominate the nanowire conductance. The basic sensing mechanism is the change of the conductance of the nanowire channel by an adsorbed species, which could be biological or chemical in nature. The electronic charge configuration of the species adsorbed changes the conductance by changing the depletion width of the channel.

2. Nanoscale machines: actuators and transducers

Piezoelectric and piezoresistive materials such as GaN nanowires can be effectively used to realize nanoscale actuators and transducers that could be capable of nanoscale motion for different applications.

3. Flexible electronics:

Nanowire devices have the capability of being assembled on flexible substrates such as plastic, which will enable realization of wearable electronics and electronic skin for robotic applications.

4. Hybrid integration:

Nanowire devices provide a remarkable advantage over conventional thin film devices that they can be assembled on-chip with Silicon microcircuitry. This provides us the opportunity to develop highly functional systems such as optical computing integrated circuits, optical data communication modules, and compact chip scale bio/chemical sensors and analyzers etc. Nanowire devices such as light emitting diodes of different material system could be assembled on the same chip to form a multispectral emitter/detector array, which could possibly revolutionize communication, environmental sensing, and medical diagnostics.

5. Thermoelectrics: thermoelectric refrigerators, power generators, heat pumps

Energy generation using nanowire devices with high thermoelectric power factor could lead to more efficient energy sources for chip scale machinery and biomedical applications. Nanoscale heaters and coolers could be used to target and destroy malignant body cells.

6. Photovoltaics:

Nanowire solar cells could be used for self sustained compact systems such as sensor clusters monitoring battlefields, which would need minimum human intervention and small amounts of power.

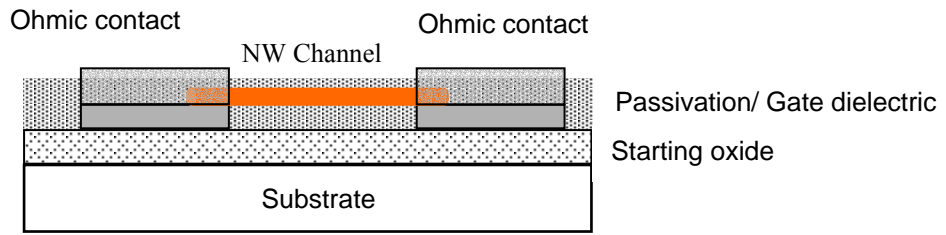
7. Nanoscale drug delivery:

Nanotubes and nanowires could be manufactured to seal drugs in their structure and release at a control pulse at the target site.

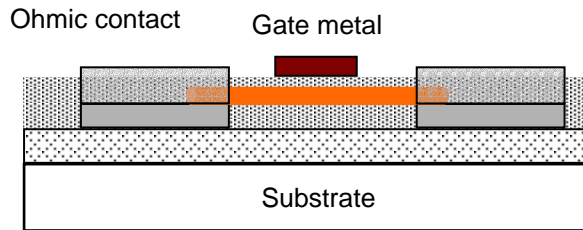
8. Fundamental transport properties:

Nanowire devices also provide us a way to study the fundamental transport properties of electrons in reduced dimensionality systems. It is well known that electrons in these types of confined systems exhibit strongly correlated behavior, whose manifestations are universal conductance fluctuations, conductance quantization, Aharonov-Bohm oscillations etc. In these nanoscale systems, phonons are also confined which gives anomalous charge and heat transport properties. These devices help us in understanding the conduction mechanisms in reduced dimension systems thus enabling us to develop high performance nanoscale devices.

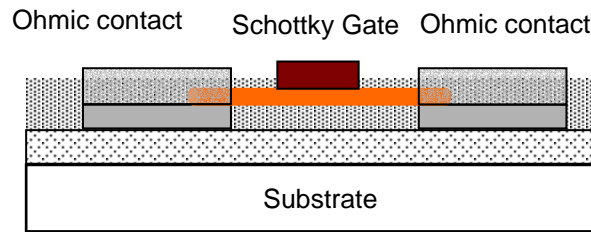
Basic two-terminal structure was presented in the earlier chapter 3. Variations of the same structure as shown in the Fig. 6.1 could provide means for realizing different device geometries which could be configured for different applications. Although the two-terminal configuration [Fig. 6.1(a)] can be used as a metal-oxide semiconductor field-effect transistor (MOSFET) with the substrate acting as a global back-gate, a top gate structure as shown in Fig. 6.1(b) would result in better performance in terms of device characteristics (transconductance, threshold voltage, subthreshold swing). Gate capacitance is higher in a top gate structure which results in higher gate modulation of the channel current and hence better performances. Variations of top gate structures (omega, cylindrical etc) will be discussed in later sections. Etching the gate oxide and depositing a high workfunction metal (Pt, Ni) would result in a Schottky gate structure [Fig. 6.1(c)] which would be a metal-semiconductor field-effect transistor (MESFET). A four-terminal structure [Fig. 6.1(d)] could be used for resistivity measurement of these nanowires.



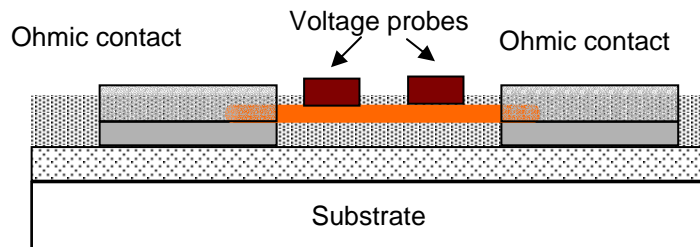
(a) Two terminal configuration



(b) Three terminal configuration- top gate structure



(c) Three terminal configuration- top Schottky gate

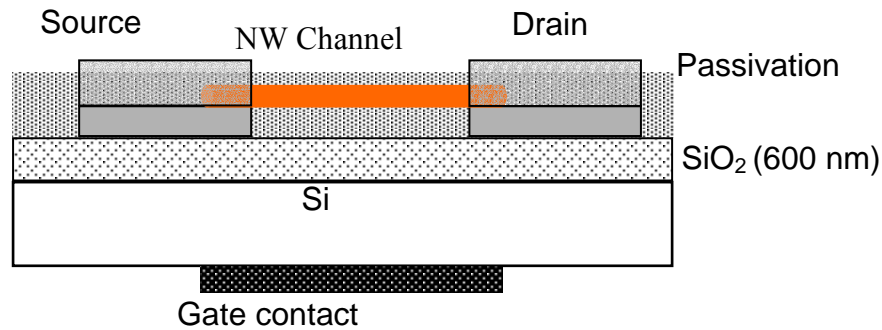


(d) Four terminal configuration

**Fig. 6.1:** Basic nanowire device configurations.

## 6.1 Bottom Gate Devices

Basic configuration of the bottom gate device is shown in Fig. 6.2. After complete fabrication of the two-terminal structure, Al is deposited on the backside of the wafer to form the metal contact for the back-gate. As the Si substrate used in this structure is degenerately doped (with resistivity in the range of  $0.1 \Omega \text{ cm}$ ), it acts such as a metal with negligible depletion region at the oxide-Si interface. The nanowire and the substrate forms a capacitance with the gate dielectric as the insulator in between.



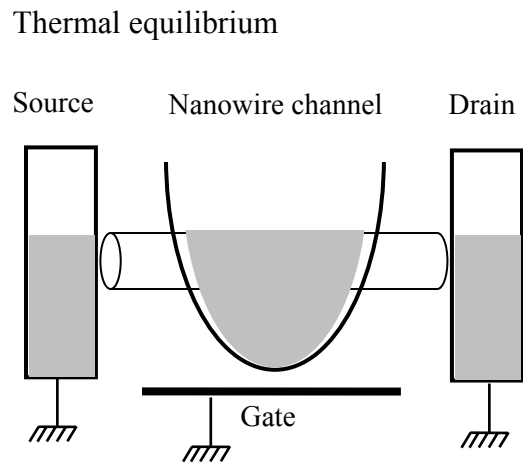
**Fig. 6.2:** Two-terminal configuration with back-gate.

When a gate voltage is applied at the bottom electrode, the electrostatic energy of the nanowire channel is modified via the gate-nanowire capacitance, resulting in conductance modulation. This conductance modulation gives rise to channel current variation with the gate voltage modification. In order to reduce the parasitic source and drain resistances, it is important to have ohmic contacts with low specific contact resistances at the source and drain end. In this study, 600 nm of thermal oxide is used as a gate dielectric, which would reduce the gate-channel capacitance leading to lower transconductance. However, it ensures that the oxide will survive the high



temperature source and drain metal contact annealing process, and the gate leakage current will be minimal.

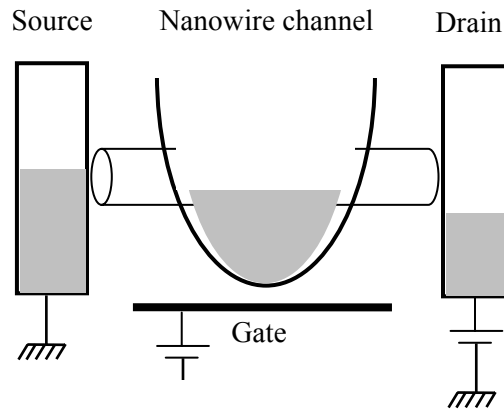
We will consider the channel to be of n-type for this discussion as it is for our case. In order to understand the operation of a nanowire FET transistor with a backgate, we have to consider the band diagrams of the nanowire FET system. Figure 6.3 considers an ideal situation where a nanowire channel is at thermal equilibrium with two perfect electron reservoirs (source and drain contacts). At thermal equilibrium, the chemical potentials are equal through out the system. As the nanowire channel is capacitively connected to the gate, applying a bias to the gate will modify the channel potential and hence carrier concentration. At equilibrium, the channel has a conductivity which is determined by its activated chemical dopant density. If a positive potential is applied to the drain with respect to the source end, electrons will start flowing from the drain end to the source end.



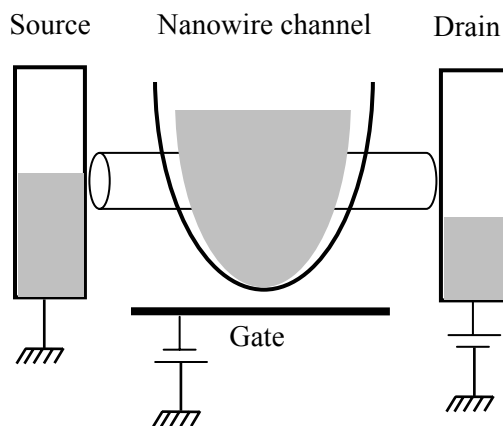
**Fig. 6.3:** Schematic representation of the energy band diagram for a nanowire FET under thermal equilibrium.

When a positive gate bias is applied, the channel potential energy decreases, resulting in an increase in the electron concentration (Fig. 6.4). Thus for an n-type channel nanowire FET the positive gate bias increases the channel current and negative gate bias reduces it. If the channel is lightly doped then by applying sufficient negative gate bias we can deplete the entire channel. Increasing the gate bias beyond that point would result in channel inversion

(a)  $V_{GS} > 0, V_{DS} > 0$



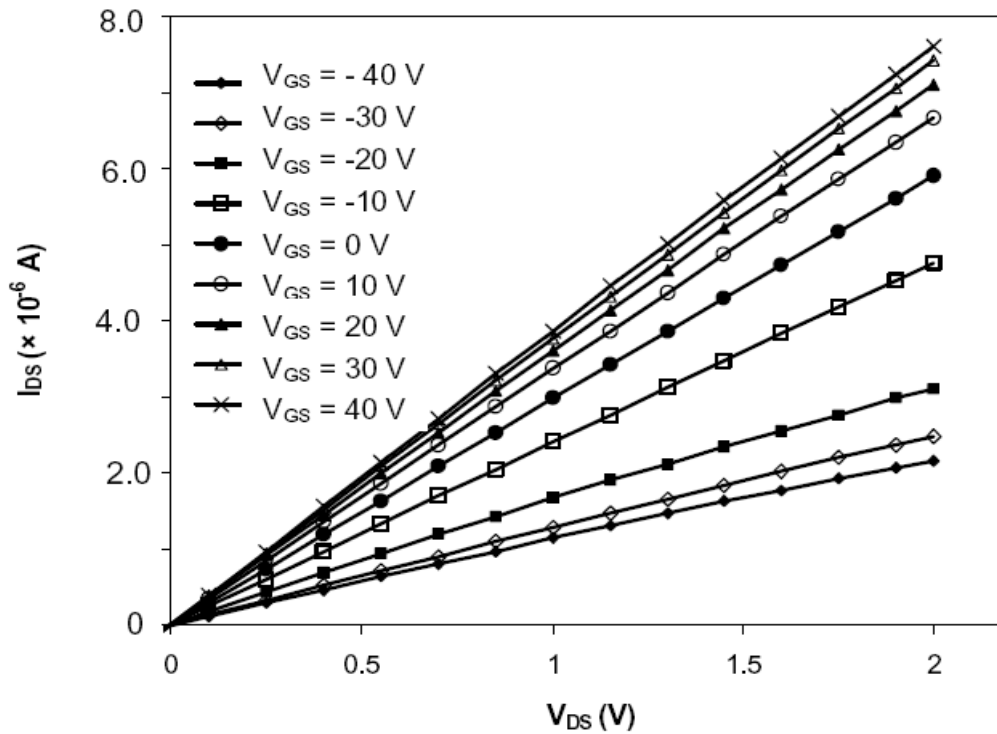
(b)  $V_{GS} < 0, V_{DS} > 0$



**Fig. 6.4:** Energy band diagram for a nanowire FET under different bias conditions. (a)  $V_{GS} > 0$ , (b)  $V_{GS} < 0$ .

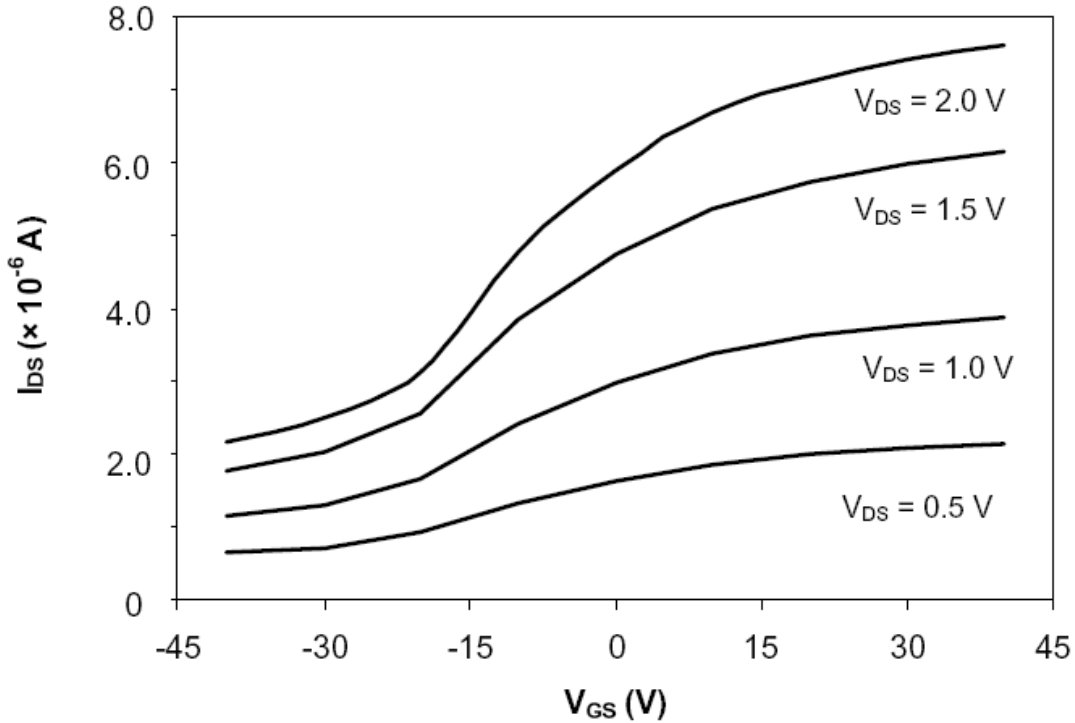
### 6.1.1 Back-gated FET Characteristics

As expected, depletion mode behavior with  $n$ -type conductivity is observed in all devices (shown previously in chapter 3). Presence of lattice defects and contaminants such as oxygen are the likely sources of  $n$ -type background concentrations often found in these types of growth methods. Detailed electrical characterizations over many devices revealed a general trend. Majority of the nanowire FETs (termed type I), showed no pinch-off characteristics, with high drain-source current ( $I_{DS}$ ) levels in the range of  $10^{-6}$  A to  $10^{-5}$  A for 1 V drain-source voltage ( $V_{DS}$ ) and 0 V gate-source voltage ( $V_{GS}$ ). Figure 6.5 shows the plot of  $I_{DS}$  vs.  $V_{DS}$  for a nanowire device of type I (diameter 200 nm, length 44  $\mu\text{m}$ ) with  $V_{GS}$  varied from  $-40$  V to  $+40$  V. For these types of devices, the channel current does not saturate even at high values of  $V_{DS}$  ( $\pm 4$ V).



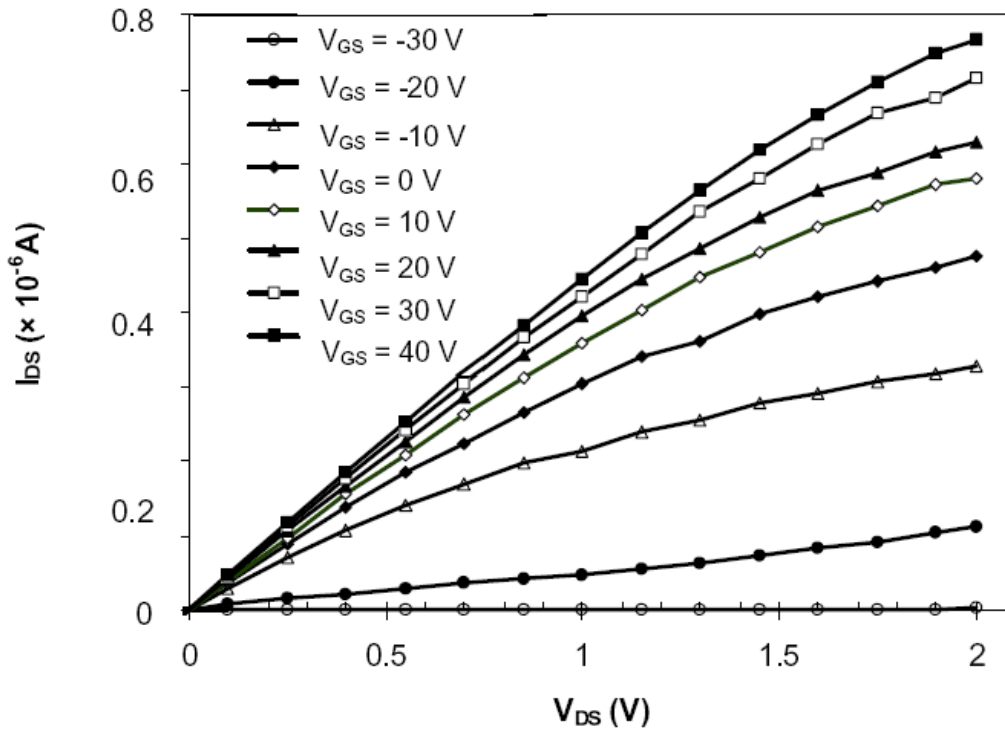
**Fig. 6.5:**  $I_{DS}$  of vs.  $V_{DS}$  plot for a nanowire device of type I (diameter 200 nm, length 44  $\mu\text{m}$ ) with  $V_{GS}$  varied from  $-40$  V to  $+40$  V.

The transconductance plot ( $I_{DS}$  vs  $V_{GS}$ ) of the same device is shown in Fig. 6.6. For large diameter nanowires channel depletion is not observed even at large negative gate biases ( $V_{GS} < -45$  V). The reason for this will be discussed in the later section.



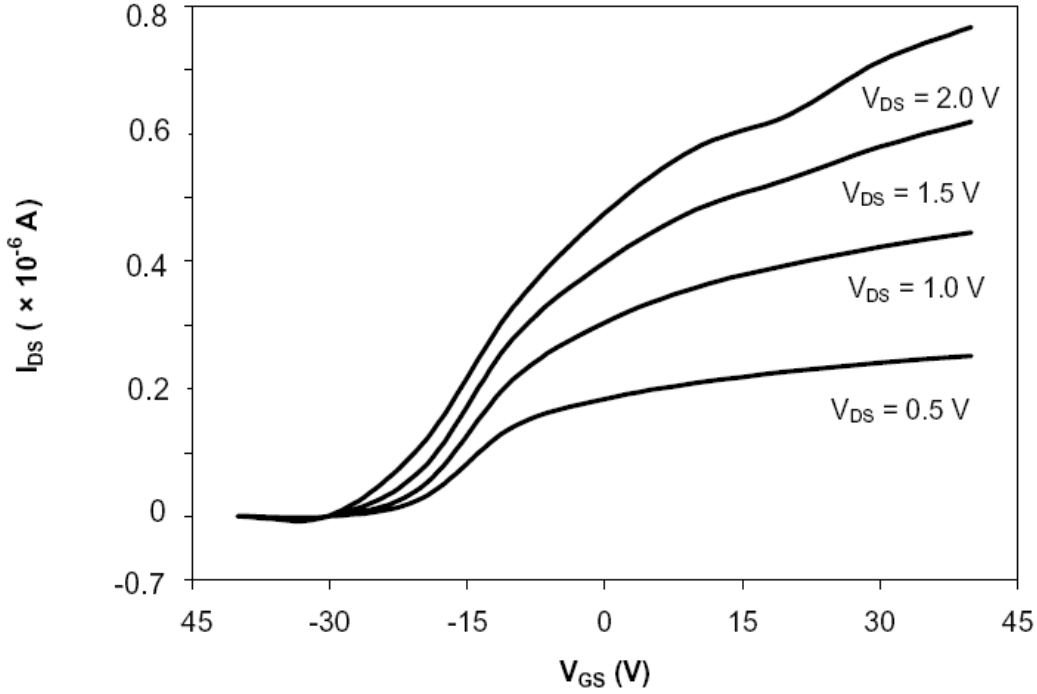
**Fig. 6.6:**  $I_{DS}$  of vs.  $V_{GS}$  plot for the nanowire device of type I (same device as in Fig. 6.5, diameter 200 nm, length 44  $\mu\text{m}$ ) with  $V_{DS}$  varied from 0.5 V to 2.0 V.

The other type of device (type II) had lower current levels ( $10^{-7}$  A to  $10^{-6}$  A for 1 V  $V_{DS}$ ), and showed complete channel depletion at  $-40$  V to  $-30$  V  $V_{GS}$  with on-off current ratio about  $10^7$ . FESEM revealed that these devices had diameters about 100 nm and less. Figure 6.7 shows the plot  $I_{DS}$  vs.  $V_{DS}$  of a nanowire device of type II (diameter 95 nm, length 35  $\mu\text{m}$ ) with  $V_{GS}$  varied from  $-30$  V to  $+40$  V.



**Fig. 6.7:** Plot of  $I_{DS}$  vs.  $V_{DS}$  of a nanowire device of type II (diameter 95 nm, length 35  $\mu m$ ) with  $V_{GS}$  varied from  $-30 V$  to  $+40 V$ .

The saturation effect observed in these smaller diameter nanowire FETs is due to the fact that for large enough drain voltage, the depletion region at the drain end starts to extend, which leads to the reduction in channel conductivity. For this particular device with  $-30 V$  threshold voltage, the complete saturation condition (given by  $V_{DS} \geq V_{GS} - V_T$ ) gives  $V_{DS} = 30 V$  for  $0 V$  gate bias. So complete saturation at low drain biases are only observed at high negative gate bias. Transconductance plot of the same device shown in Fig. 6.8 clearly demonstrates that the channel is depleted completely at  $-30 V$  gate bias. For large diameter nanowire this voltage is much higher, and would result in significant gate leakage and gate breakdown.



**Fig. 6.8:**  $I_{DS}$  of vs.  $V_{GS}$  plot for the nanowire device of type II (same as in Fig. 6.7, diameter 95 nm, length 35  $\mu\text{m}$ ) with  $V_{DS}$  varied from 0.5 V to 2.0 V.

### 6.1.2 Parameter Extraction

For any device to be useful as a circuit element, evaluating the parameters describing its performance is necessary. Characteristics of these nanowire devices are compared by using standard device parameters as described below [72]:

a) Transconductance per unit gate width is defined as:

$$\frac{g_m}{W} (S\mu\text{m}^{-1}) = \frac{1}{W} \left( \frac{\partial I_{DS}}{\partial V_{GS}} \right)_{V_{DS}} \quad (6.1)$$

Transconductance (rate of change of the channel current with the gate voltage) for a transistor gives indication to its intrinsic amplification factor. This parameter is

normalized with respect to the gate width so that comparison between different nanowires with different diameters can be made.

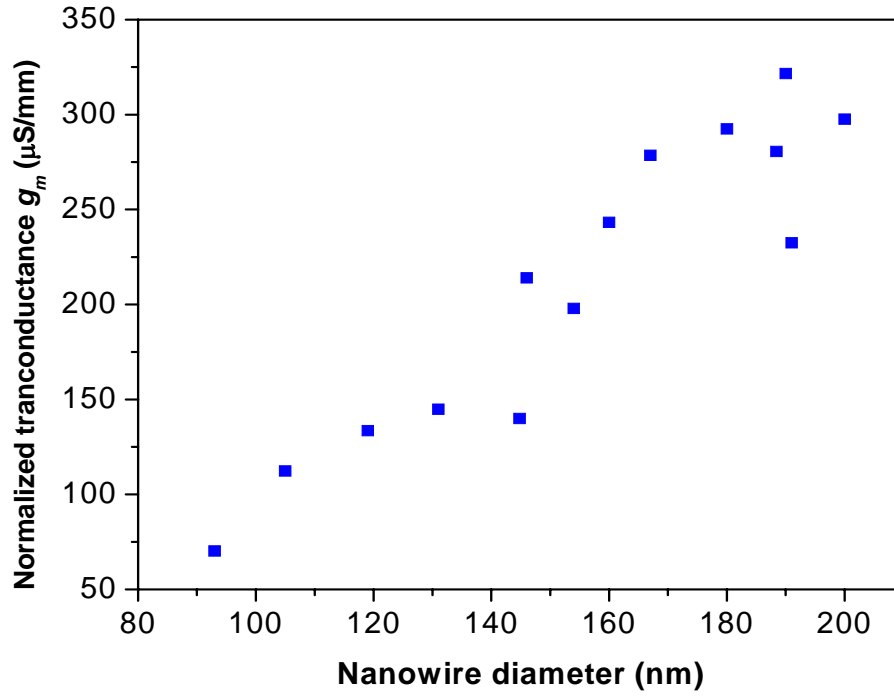
- b) Threshold voltage  $V_T$  is defined as the voltage where the channel stops conduction. For a n-type depletion mode FET this voltage is negative. As will be shown later carrier concentration can also be deduced from this voltage.
- c) Sub-threshold slope is defined as:

$$S = \left( \frac{\partial V_{GS}}{\partial \text{Log}_{10} I_{DS}} \right)_{\text{subthreshold}} \quad (6.2)$$

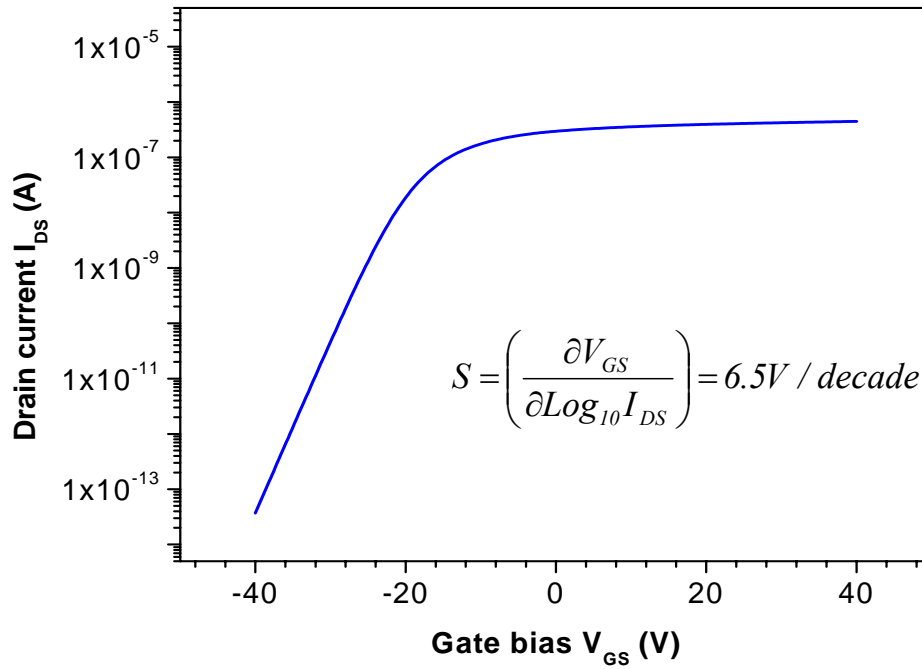
As described by the relationship above, sub-threshold slope indicates how fast we can turn off the transistor. It is defined as the variation of the gate voltage needed for producing 1 decade of change in the channel current. This is usually done by finding the inverse slope from a semi-log plot of  $I_{DS}$  vs  $V_{GS}$  at turn off.

- d) On-off current ratio  $I_{on}/I_{off}$  describes the transistors effectiveness as a switch

The plot of normalized transconductance of nanowire FETs with varying diameter in Fig. 6.9 (a) exhibited a trend. Normalized transconductance increases gradually with increase of the nanowire diameter. It will be clear below that this increase in transconductance is due to the fact that the gate capacitance increases with nanowire diameter, which increases the gate modulation of the channel current. Sub-threshold slope and threshold voltage are only defined for nanowires with complete channel depletion. Figure 6.9 (b) shows the semi-log plot of sub-threshold drain current with gate voltage with  $S= 6.5$  V/decade for a 95 nm diameter nanowire. On-off current ration for the same device is about  $10^7$ .



(a)



(b)

**Fig. 6.9:** (a) Normalized transconductance of backgated nanowire FETs with varying diameters. (b) Semi-log plot of drain current with gate voltage for a 100 nm diameter nanowire FET. The sub-threshold slope is shown inside the plot.



These parameters are related to two important material properties namely mobility and carrier concentration. In order to extract these material properties from the device characteristics, it is necessary to establish the relationships between the device parameters and the intrinsic material properties. For that it is necessary to have the analytical expressions for the channel current  $I_{DS}$  as a function of source-drain voltage and source-gate voltage. This could be expressed mathematically as  $I_{DS} = I_{DS}(V_{DS}, V_{GS})$ . As the channel charge is capacitively coupled to the gate, establishing the above mentioned relationship would require an analytical solution for the gate-channel capacitance. Unfortunately a correct analytical expression for the capacitance of a nanowire channel and backgate does not exist. We will discuss later how we can assume a simplified capacitance relationship later. For now if it is assumed that we have the capacitance expression then the whole problem could be reduced to that of a conventional thin film MOSFET devices. The current-voltage relationship of an n-channel MOSFET is given below [72]:

Linear region:  $V_G \geq V_T, V_{DS} < V_{GS} - V_T$

$$I_{DS}(lin) = \frac{\mu_n C_{ox}}{2} \cdot \left(\frac{W}{L}\right) \cdot [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (6.3)$$

Saturation region:  $V_G \geq V_T, V_{DS} \geq V_{GS} - V_T$

$$I_{DS}(sat) = \frac{\mu_n C_{ox}}{2} \cdot \left(\frac{W}{L}\right) \cdot [(V_{GS} - V_T)^2] \quad (6.4)$$

In the above equation  $\mu_n$  is the electron field effect mobility,  $C_{ox}$  is the gate capacitance per unit area, and  $W/L$  is the width to length ratio of the device. For a nanowire device with a global back-gate, the length of the gate “ $L$ ” is the total length

between the source and drain end, and the width of the gate “ $W$ ” would be the diameter of the nanowire.

Due to large thickness of the back-gate oxide and higher doping densities of these nanowires, the threshold voltage (at which the nanowire stops conduction) is usually large for these devices, about -30 to -40 V. Hence the saturation behavior is only observed at large negative gate biases. If one examines the linear region characteristics governed by the Eq. 6.3 and performs a partial derivative with respect to gate voltage one obtains the relationship:

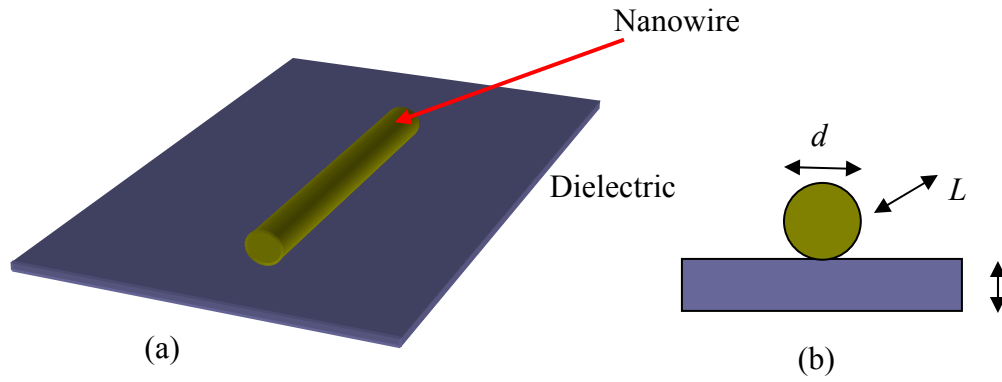
$$\frac{\partial I_{DS}(lin)}{\partial V_{GS}} = \mu_n C_{ox} \cdot \left(\frac{W}{L}\right) \cdot V_{DS} \quad (6.5)$$

Upon rearrangement which yields:

$$\mu_n = \left(\frac{\partial I_{DS}(lin)}{\partial V_{GS}}\right) \cdot \frac{1}{C_{ox}} \cdot \left(\frac{L}{W}\right) \cdot \frac{1}{V_{DS}} \quad (6.6)$$

This relationship establishes a way to determine the electron field effect mobility from the measured transistor characteristics. If one assumes that gate capacitance is known and its variations with gate voltage is negligible then the factor  $(\partial I_{DS}/\partial V_{GS})$  is the transconductance which could be directly measured in the linear region or obtained through differentiation of the transconductance curve.

The usability of the Eq. 6.6 depends on estimating the nanowire capacitance with a suitable simplified assumption.. The capacitance of the nanowire FET is modeled by a thin metallic cylinder on an infinite dielectric plane as shown in Fig. 6.10.



**Fig. 6.10:** (a) Cylinder on an infinite dielectric plane model for determining nanowire gate capacitance, (b) Cross section showing the dimensions of the nanowire and the oxide.

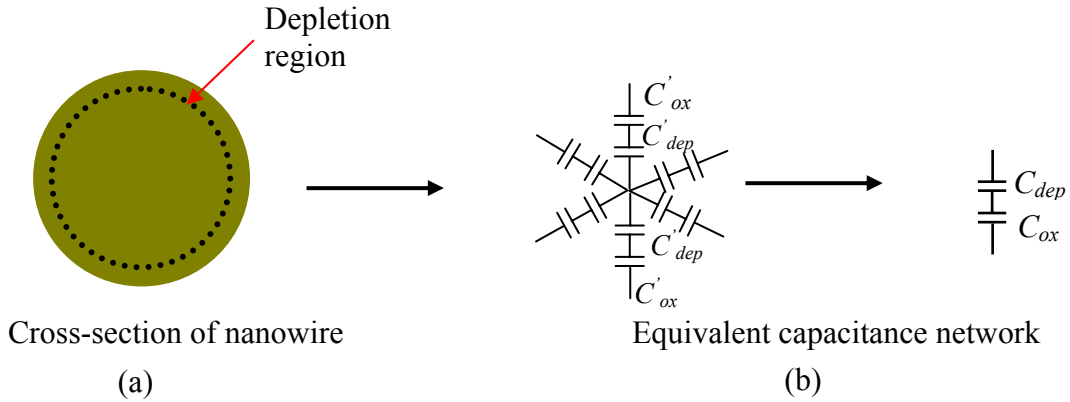
Basic electrostatic analysis will show that the capacitance of the system is given by the relation [73]:

$$C = \frac{2\pi\epsilon_0\epsilon_{SiO_2}L}{\ln\left(\frac{4t_{ox}}{d}\right)} \quad (6.7)$$

where  $\epsilon_0$  is the dielectric permittivity of free space,  $\epsilon_{SiO_2}$  and  $t_{ox}$  are the relative permittivity and thickness of the of  $SiO_2$  (dielectric layer in nanowire FET system) layer respectively,  $L$  and  $d$  being the length and diameter of the nanowire respectively. Capacitance per unit area  $C_{ox}$  is obtained by dividing Eq. 6.7 by the gate surface area ( $d \times L$ ).

Strictly speaking Eq. 6.7 is only valid for metallic such as nanowires and nanotubes with small diameters such as the case for carbon nanotubes FETs where the doping densities are fairly highly. Semiconducting nanowires on other hand would have depletion region associated with them and hence forth the capacitance of the total nanowire oxide system will be the capacitance of the simple metal-oxide system together with the depletion capacitance in series (Fig. 6.11). Hence the Eq. 6.7 overestimates the capacitance of the system in depletion region or in the negative gate

bias region for an n-type doped nanowire. We will revisit the problem of nanowire-gate capacitance in a later section.



**Fig. 6.11:** (a) Nanowire cross-section showing the depletion region, (b) Equivalent capacitance model for a nanowire cross-section.

As we have obtained an analytical expression for the nanowire-gate capacitance, we can now substituting Eq. 6.7 into Eq. 6.6 with  $W$  replaced by  $d$  to obtain the relationship:

$$\mu_n = \frac{g_m}{V_{DS}} \frac{L \ln \left( \frac{4 t_{ox}}{d} \right)}{2 \pi \epsilon_o \epsilon_{SiO_2}}. \quad (6.8)$$

where transconductance ( $g_m$ ) is the slope  $\partial I_{DS} / \partial V_{GS}$  calculated from the  $I_{DS}$  vs.  $V_{GS}$  plot in the linear region,  $L$  and  $d$  are the length and diameter of the nanowire respectively,  $t_{ox}$  is the oxide thickness (600 nm),  $\epsilon_o$  is the permittivity of free space and  $\epsilon_{SiO_2}$  is the permittivity of silicon dioxide for the present case. The carrier concentration (volume density of electrons) is calculated using the relationship [72]:

$$n = \frac{V_{th} C}{qAL} \quad (6.9)$$

Substituting Eq. 6.7 into Eq. 6.9, we get

$$n = \frac{\epsilon_o \epsilon_{SiO_2} V_{th}}{qr^2 \ln\left(\frac{4t_{ox}}{d}\right)} \quad (6.10)$$

Using Eq 6.8 and transconductance ( $g_m$ ) calculated from the  $I_{DS}$  vs  $V_{GS}$  plot, mobility has been obtained for number of backgated nanowire devices. For the particular device (diameter 200 nm, length 44  $\mu$ m) calculated mobility was 230  $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ , where as for the smaller diameter nanowire device (diameter 95 nm, length 35  $\mu$ m) it was about 40  $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ . Mobility as high as 319  $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  has been obtained for a nanowire with 195 nanometer diameter. Details of diameter dependent mobility values will be presented in a later section. The mobility obtained in this study for larger diameter nanowires are significantly higher (by an order of magnitude) than the majority of the results published so far [62], [74], [75]. Mobilities in this range were found in majority of our devices. The only report of GaN nanowire FET mobilities higher than the present result is by Huang *et al.* [47], where they reported mobilities in the range of 640  $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  and 300  $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  in a batch of ten devices. Higher mobility in the present nanowires could be due to the fact that these nanowires are grown without the use of catalyst. Common catalysts such as Ni, Au, and Fe used in most of the other growth methods usually form deep level states in the bandgap of GaN, which can adversely effect the carrier life times and mobility. These catalysts can be incorporated into the nanowire lattice during the growth. The electron density is calculated for nanowires with smaller diameters for which the threshold voltages can be determined unambiguously. For the 100 nm diameter nanowire ( $I_{DS}$  vs  $V_{GS}$  shown in Fig. 6.8) with a threshold voltage of -30 V, we have calculated an electron

density in the range of  $2 \times 10^{18} \text{ cm}^{-3}$ . We will compare the performance of the GaN nanowire FETs with different thin film and nanowire devices later.

### 6.1.3 Numerical Simulation of Nanowire-Gate Capacitance

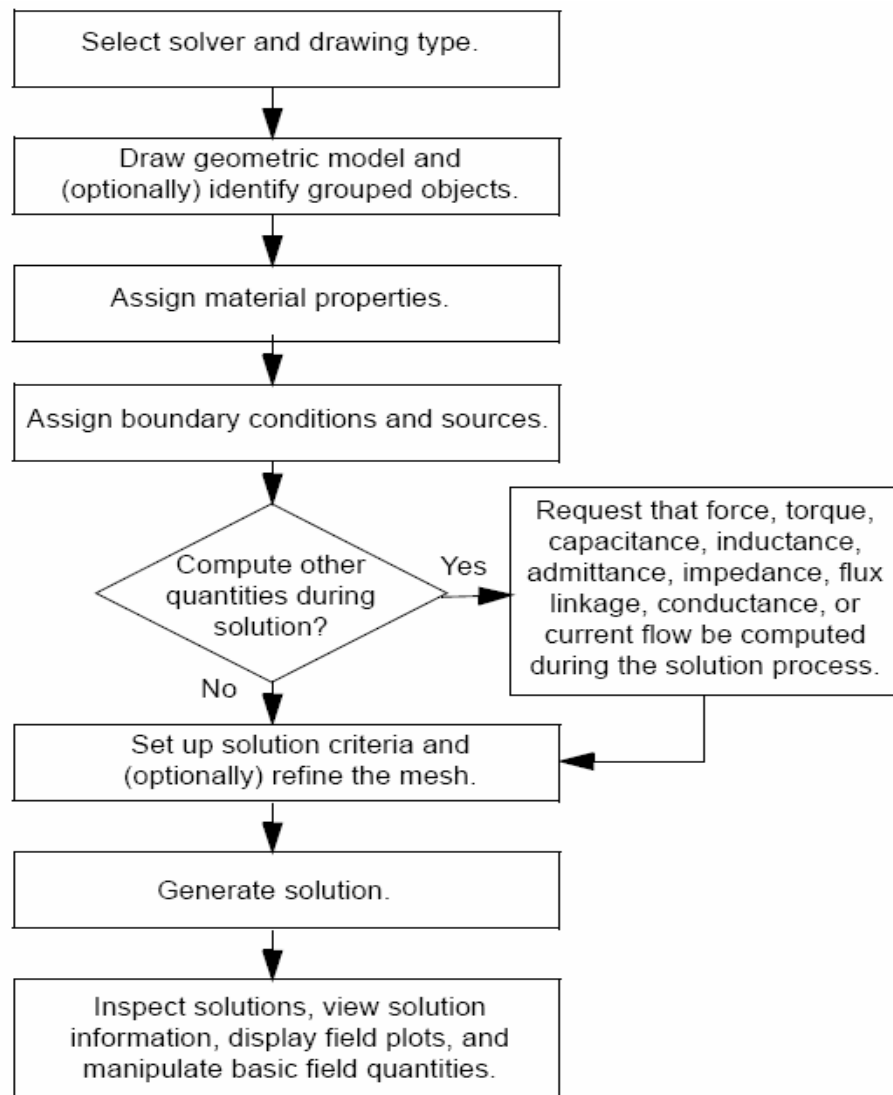
As shown before that the nanowire capacitance, as given by the Eq. 6.7 do not take into account the diameter of the nanowire nor the depletion capacitance associated with it. Nanowire channel-gate capacitance as modeled by Eq. 6.7 assumes that the nanowire is a cylinder, with small diameter and metallic conductivity. In our case this is not completely valid assumption as the diameters of these nanowire devices, as shown in chapter 2, ranges anywhere from 80 nm to 300 nm, with conductivities having significant variations over the diameter range and from one growth run to another. Another source of error in the analytical expression is that it assumes that the nanowire is bare as shown in the Fig. 6.12 (a), where as in actual devices the nanowire is passivated with a thin layer of  $\text{SiO}_2$  [Fig. 6.12(b)].



**Fig. 6.12:** (a) Nanowire geometry used for analytical capacitance expression, (b) Actual nanowire device geometry used for this study.

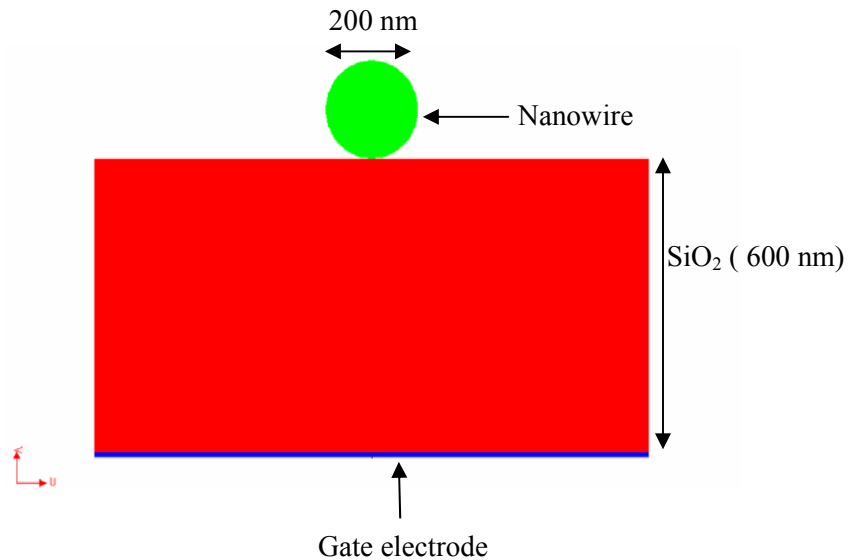
As the current voltage characteristics of these nanowire devices are dominated by the capacitance of the system, it is important to numerically evaluate the capacitance of nanowire channel-gate system and quantitatively identify the difference in the analytical and numerical results. In order to numerically calculate the capacitance of

the given problem we have used the Maxwell<sup>®</sup> simulation software. It is an electrostatic/magnetostatic finite element modeling software that automatically creates the finite element mesh on the desired geometry and iteratively calculates the desired electrostatic field solution and special quantities such as capacitance, energy etc. It also provides a 2D Modeler which can create the desired geometry which we are attempting to solve. Steps for generating a solution for a given geometry is summarized below:



**Fig. 6.13:** Flow chart representing the steps for solving a problem in Maxwell<sup>®</sup>.

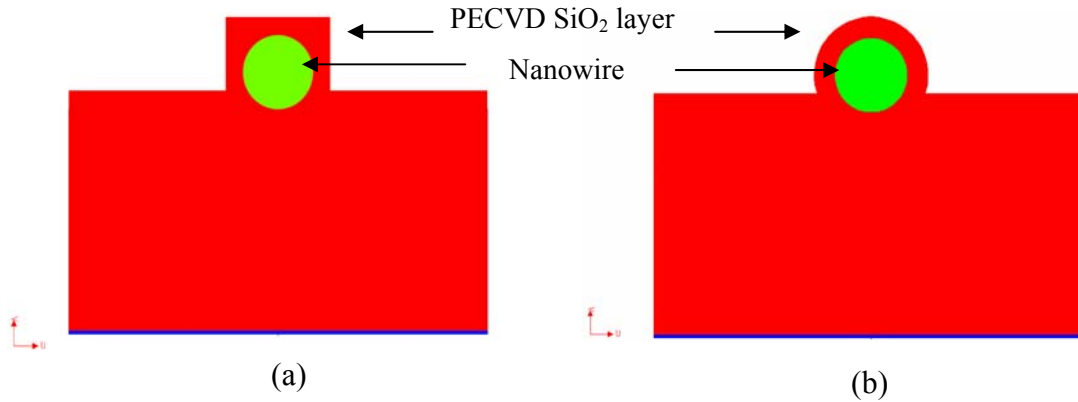
Obtaining numerically calculated capacitances of simple structures and comparing them with the value given by Eq. 6.7 for the same parameters will help us in understanding the impact of capacitance evaluation in the device characteristics. We have used three simple structures and obtained their numerical capacitance value and compared them with the analytical values. All three structures have the nanowire with same diameter and same oxide thickness. The first simplified geometry as shown in Fig. 6.14, where a 200 nm diameter nanowire is placed on 600 nm SiO<sub>2</sub>.



**Fig. 6.14:** Simplified geometry used for analytically calculating nanowire-gate capacitance.

This is the simplified geometry, whereas for an actual device the nanowire is passivated with a 35 – 50 nm of PECVD SiO<sub>2</sub>. It is well known that the oxides deposited using PECVD technique do not form a conformal coating. Although the actual nature of the coverage of the PECVD oxide is not well known but one can assume it is in between the two configurations shown in Fig. 6.15. We solved for capacitances for all three structures (as shown in Fig. 6.14 and 6.15) using Maxwell<sup>®</sup>.



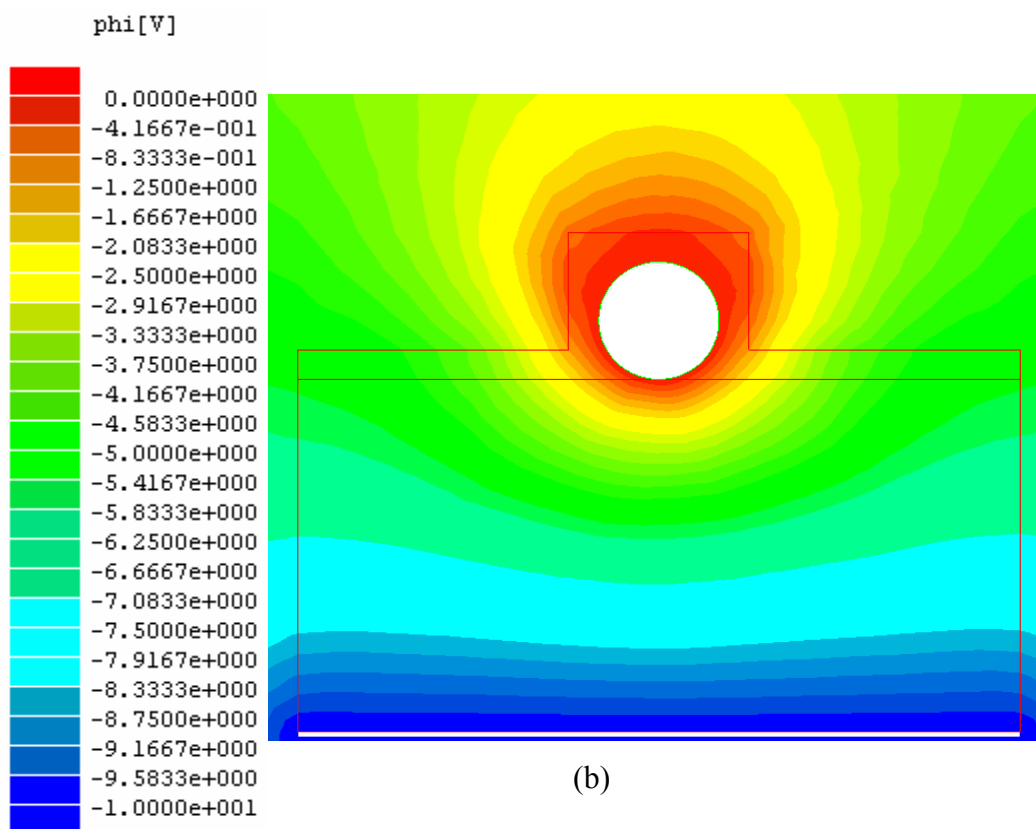
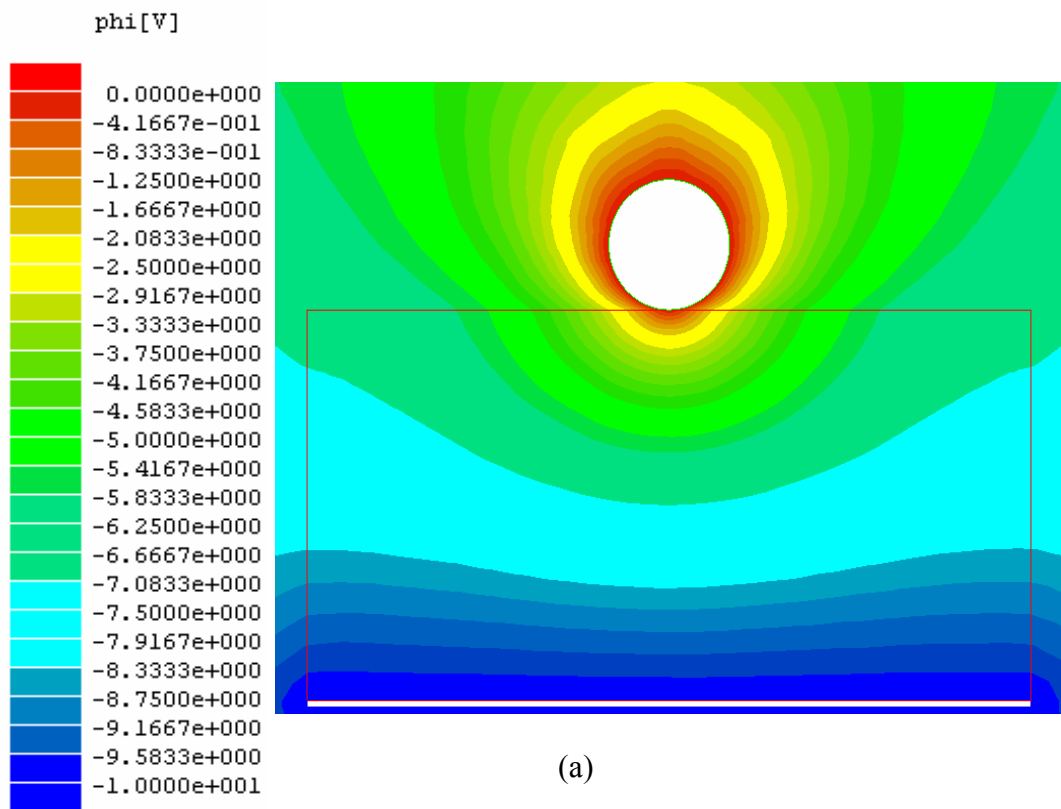


**Fig. 6.15:** Simplified geometry of nanowire devices coated with PECVD oxide (a) assuming a square PECVD SiO<sub>2</sub> profile, (b) a round profile.

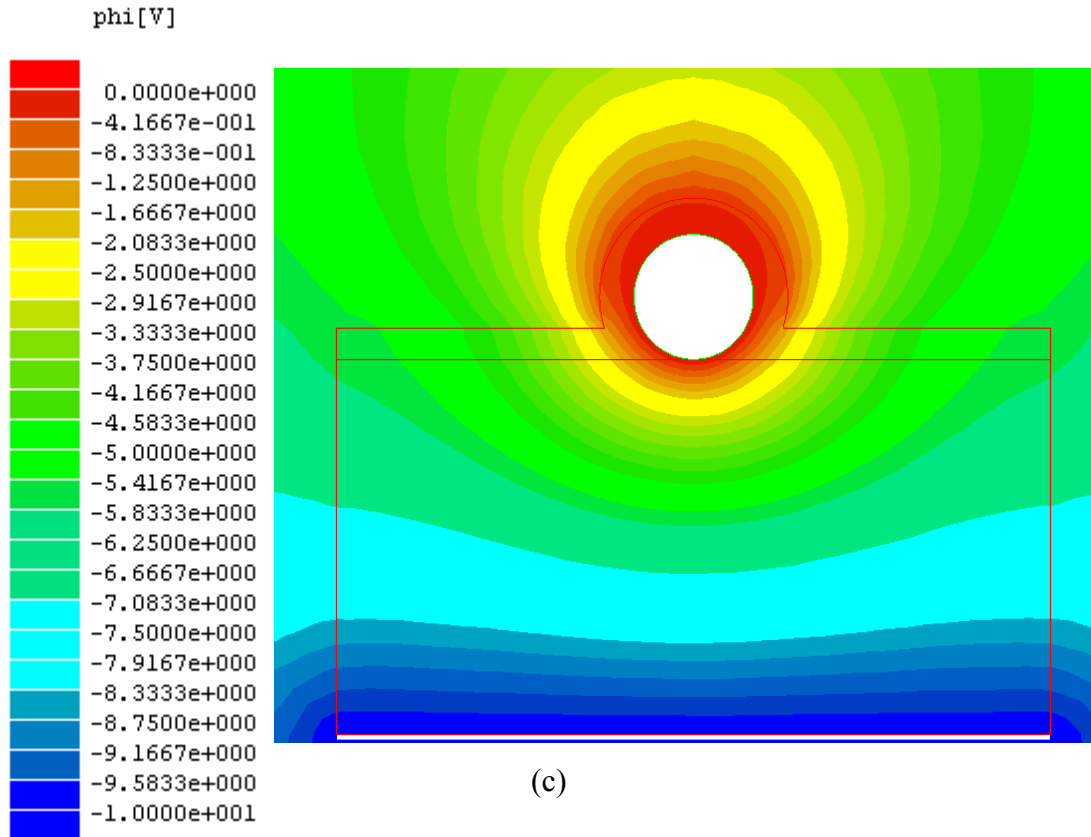
For all three structures, the diameter of the nanowire and the thickness of the backgate oxide are kept constant. The parameters for all three the structures are given in the table 6.1. The capacitance of the above mentioned structures were obtained by assigning constant boundary condition at the nanowire oxide interface. The nanowire is kept at 0 V. Electrostatic simulation of all the three structures with -10 V gate bias is shown in Fig. 6.16 (a)-(c).

**Table 6.1:** Parameters used for capacitance calculations in Maxwell<sup>®</sup>.

Parameter	Value
NW diameter (nm)	200
Gate oxide thickness (nm)	600
PECVD oxide thickness (nm)	50
NW relative permittivity	8.9
NW conductivity (S m <sup>-1</sup> )	$2 \times 10^4$



**Fig. 6.16:** 2-D plot of voltage (a) bare nanowire, (b) nanowire coated with PECVD oxide with a square profile.



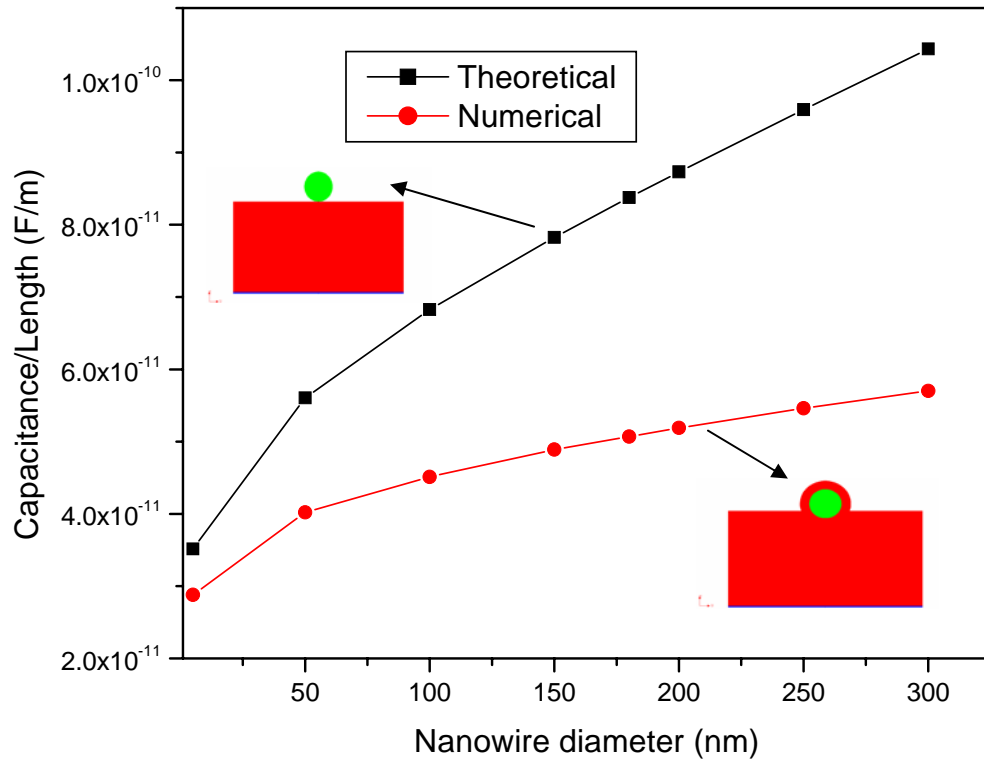
**Fig. 6.16:** (c) nanowire coated with PECVD oxide with a circular profile.

From the electrostatic solution of the voltage, we can calculate the capacitance per unit length ( $C/L$ ) for all three structures. From table 6.2, it is clear that although the presence of PECVD  $\text{SiO}_2$  layer modifies the capacitance, the nature of the passivation does not have a significant effect on the capacitance of the system. Presence of a dielectric layer (50 nm  $\text{SiO}_2$ ) around the nanowire channel increases the capacitance of the system. It is also evident that the analytical expression for the same geometry gives substantially higher value (almost double for the 200 nm diameter nanowire). As we now have an idea that the nanowire-gate capacitance is fairly dependent of the coverage of the PECVD layer, we can compare the numerical capacitances for the

conformal structure for different nanowire diameters with the analytical value for a bare nanowire (Fig. 6.17).

**Table 6.2:** Comparison of analytical and numerical capacitances for structures shown in Fig. 6.14 and 6.15.

Geometry	Capacitance (F/m) Numerical	Capacitance (F/m) Analytical
No PECVD oxide	$4.2 \times 10^{-11}$	$8.7 \times 10^{-11}$
Sqaure PECVD oxide	$5.03 \times 10^{-11}$	N/A
Conformal PECVD oxide	$5.19 \times 10^{-11}$	N/A



**Fig. 6.17:** Comparison of numerically and analytically determined capacitances for the structures shown above each plot.

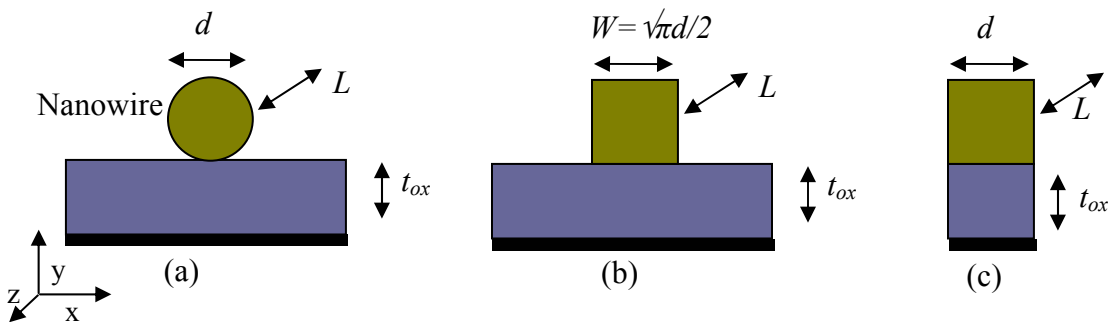
For smaller diameter nanowire the difference between the numerical capacitance value and capacitance calculated using the Eq 6.6 is quite small. As the diameter increases this difference between the numerical and analytical capacitance value becomes quite significant. This indicates that the analytical capacitance expression is only valid for those nanowires whose diameters are small compared to the oxide thickness. Larger diameter nanowires modify the electric field configuration hence affect the capacitance of the system. It is thus seen that even without taking the depletion capacitance into consideration, the capacitance of the nanowire channel is significantly different from the analytical expression. As mobility is inversely dependent on the capacitance, using numerical capacitances (lower than analytical capacitances) in Eq. 6.4 would result in even higher mobility in our devices.

#### **6.1.4 One-Dimensional Modeling**

As shown in the previous section the analytical expressions of the channel current for a nanowire FET are difficult to generate, due to complex nature of the capacitance and the geometry of the problem. Estimating and modeling the channel current is essential if one has to realize reliable nanowire systems. Simulating the channel current  $I_{DS}$  as a function of drain and gate voltages are quite difficult requiring complex three dimensional modeling, which is usually done by device simulators. A complete nanowire FET simulation would involve self-consistent solution of the Poisson's equation and the continuity equations for the specified geometry with proper boundary conditions. This process requires discretization of the differential

equations and converting them to linear equations and then solving those using numerical techniques. This process is repeated on a grid (3 dimensional for the whole devices) to get the complete solution for the problem. This 3-D problem is highly complex and needs huge computing resources. In this section we will describe a simple one dimensional modeling tool developed using C++, which is capable of simulating the channel conductance as a function of the gate voltage. This tool is capable of computing the channel conductance, hence one can estimate the channel current with some confidence in the linear region of the device operation.

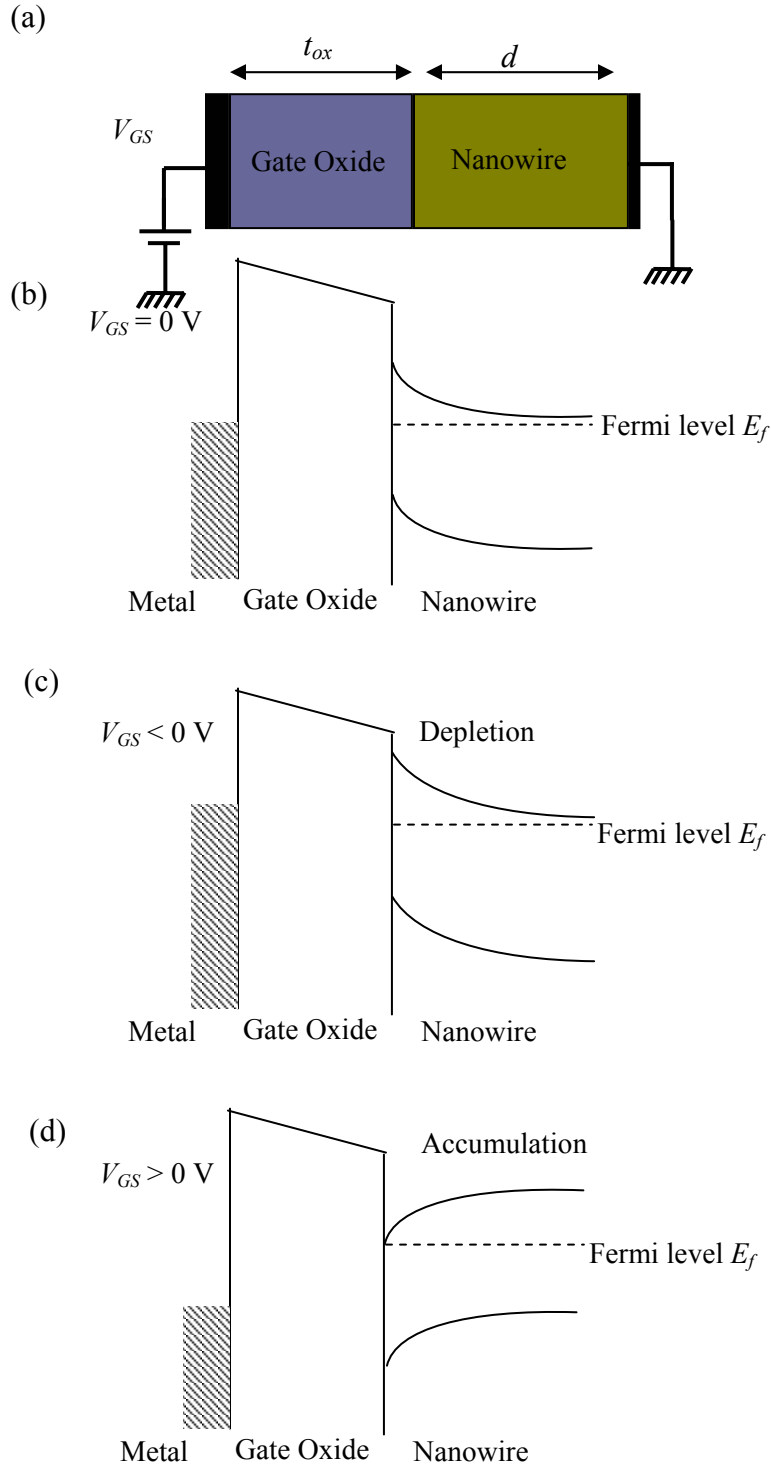
In order to model the gate modulation of the channel charge we have used a very simplified geometry to solve the 1-D Poisson's equation in the nanowire channel. We assumed that the nanowire is of square cross-section rather than circular as shown in Fig. 6.18(a) and 6.18(b). The structure can be further simplified to Fig. 6.18(c), where it is assumed that the gate is present only under that nanowire, in other words neglecting the fringing fields of the gate electrode.



**Fig. 6.18:** (a) Circular cross-section of a nanowire FET, (b) square cross-section with  $W$  scaled to match the surface area of the circular FET, (c) 1-D model neglecting gate in  $x$  direction.

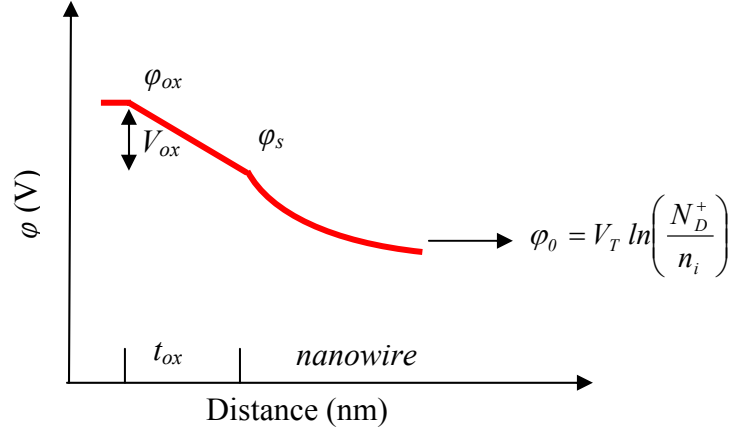
The simple structure in Fig. 6.18(c) represents that MOSFET capacitor where that metal gate electrode represents that Si wafer as a back gate. The structure is shown in

Fig. 6.19(a). The energy band diagrams for this system are shown in Fig. 6.19(b)-(d) for different gate biases.



**Fig. 6.19:** (a) 1-D MOSFET capacitor (MOS-CAP), (b) energy band diagram for MOS-CAP in thermal equilibrium, (c) for  $V_{GS} < 0$  V, and (d) for  $V_{GS} > 0$  V.

In order to compute the channel conductance one needs to know the channel carrier concentration. When a gate bias is applied, it is distributed along the MOSFET capacitor as shown below in Fig. 6.20 [76].



**Fig. 6.20:** Potential profile for a 1-D MOSFET capacitor with gate bias.

Where gate bias  $V_G$  is given by the relationship:

$$V_G = V_{ox} + \varphi_s - \varphi_0 \quad (6.11)$$

where  $V_{ox}$  is the voltage drop across the gate oxide,  $\varphi_s$  is the semiconductor surface potential, and  $\varphi_0$  is the bulk potential. The carrier concentration in the channel at any given gate bias is given by the relationship:

$$n = n_i \exp\left(\frac{\varphi}{V_t}\right) \quad (6.12)$$

$$p = n_i \exp\left(\frac{-\varphi}{V_t}\right) \quad (6.13)$$

where  $n$ ,  $p$  are the electron and hole concentrations,  $n_i$  is the intrinsic carrier concentration for the semiconductor and  $V_T$  is the thermal voltage ( $k_B T/q$ ). Thus finding effective carrier concentration for the channel for any applied gate bias is



essentially dependent on finding potential inside the semiconductor. This is given by the 1-D Poisson's equation:

$$\frac{d^2(\varphi)}{dx^2} = -\frac{q}{\varepsilon}(-n + p + N_D^+ - N_A^+) \quad (6.14)$$

where  $\varphi$  is the potential,  $n$  and  $p$  are the electron and hole concentration respectively,  $N_D^+$  and  $N_A^+$  are the ionized donor and acceptor concentrations respectively, and  $\varepsilon$  is the dielectric permittivity of the medium. Now substituting Eq. 6.12 and 6.13 in Eq. 6.14, we get the non-linear Poisson's equation relating the channel potential to the carrier concentration [77]:

$$\frac{d^2(\varphi)}{dx^2} = -\frac{q}{\varepsilon} \left[ -n_i \exp\left(\frac{\varphi}{V_t}\right) + n_i \exp\left(\frac{-\varphi}{V_t}\right) + N_D^+ - N_A^+ \right] \quad (6.15)$$

Substituting  $2\sinh(x) = \exp(x) - \exp(-x)$  in Eq. 6.15, we get:

$$\frac{d^2(\varphi)}{dx^2} = -\frac{q}{\varepsilon} \left[ -2 \sinh\left(\frac{\varphi}{V_t}\right) + N_D^+ - N_A^+ \right] \quad (6.16)$$

For heavily doped n-type semiconductor with  $N_D^+ \gg N_A^+$  this equation simplifies to

$$\frac{d^2(\varphi)}{dx^2} = \frac{q}{\varepsilon} \left[ 2 \sinh\left(\frac{\varphi}{V_t}\right) - N_D^+ \right] \quad (6.17)$$

This is a second order non-linear differential equation. We can discretize this differential equation and convert it into a system of coupled linear equations on a uniform grid. This is done by approximating the derivatives by their finite differences using Taylor series as (neglecting third order terms):

$$f(x + \Delta x) = f(x) + \frac{df(x)}{dx} \Delta + \frac{d^2 f(x)}{dx^2} \Delta^2 \quad (6.18)$$

$$f(x - \Delta x) = f(x) - \frac{df(x)}{dx} \Delta - \frac{d^2 f(x)}{dx^2} \Delta^2 \quad (6.19)$$

Using these two equations we can discretize Eq. 6.17 for every single point on a uniform 1D grid as:

$$\frac{\varphi_{i+1} - 2\varphi_i + \varphi_{i-1}}{\Delta^2} - \frac{q}{\varepsilon} \left[ 2 \sinh\left(\frac{\varphi_i}{V_t}\right) - N_{Di}^+ \right] = 0 \quad (6.20)$$

where the index represents value of the parameter at point  $i$  in the grid. Expressing this equation as a function  $f(\varphi_{i-1}, \varphi_i, \varphi_{i+1})$  we obtain:

$$f(\varphi_{i-1}, \varphi_i, \varphi_{i+1}) = \frac{\varphi_{i+1} - 2\varphi_i + \varphi_{i-1}}{\Delta^2} - \frac{q}{\varepsilon} \left[ 2 \sinh\left(\frac{\varphi_i}{V_t}\right) - N_{Di}^+ \right] \quad (6.21)$$

The function  $f$  can be solved using Newton's method, where the solution condition is expressed as:

$$f(\varphi_{i-1}, \varphi_i, \varphi_{i+1}) - \frac{\partial f}{\partial \varphi_{i-1}} \Delta \varphi_{i-1} + \frac{\partial f}{\partial \varphi_i} \Delta \varphi_i + \frac{\partial f}{\partial \varphi_{i+1}} \Delta \varphi_{i+1} = 0 \quad (6.22)$$

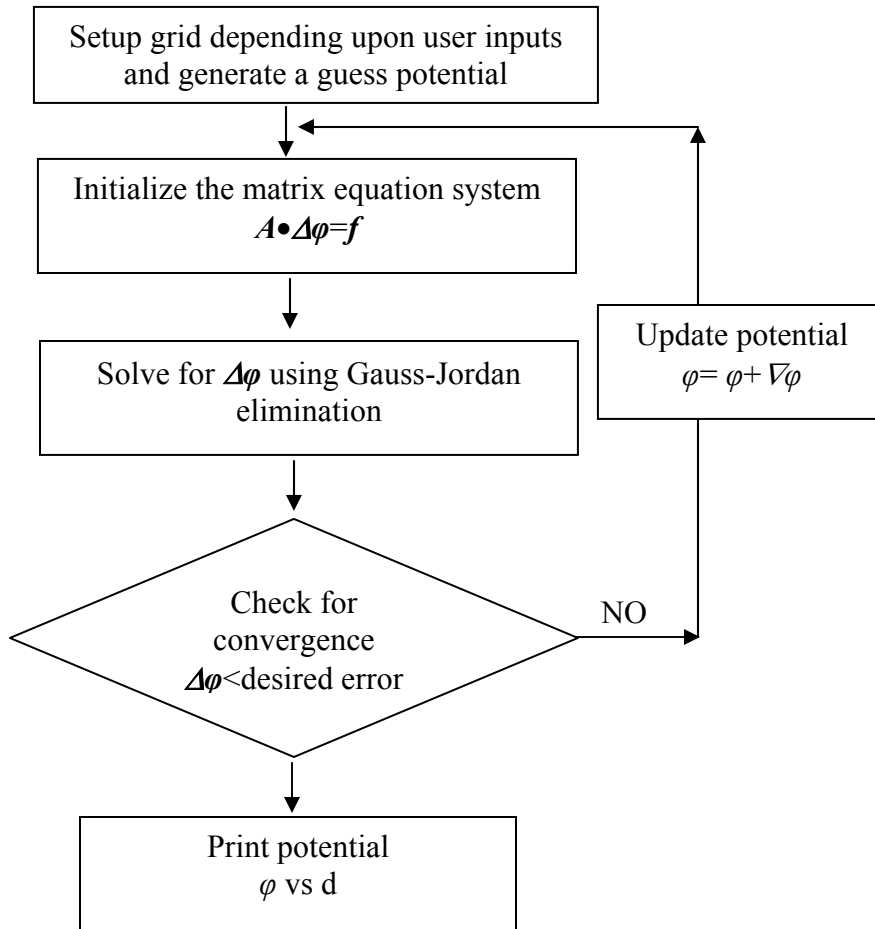
Comparing Eq. 6.22 and Eq. 6.21,

$$\begin{aligned} \frac{\partial f}{\partial \varphi_{i-1}} &= \frac{1}{\Delta^2} = a_{i-1} \\ \frac{\partial f}{\partial \varphi_i} &= -\frac{2}{\Delta^2} - \frac{q}{\varepsilon V_t} \left[ 2 \cosh\left(\frac{\varphi_i}{V_t}\right) \right] = b_i \\ \frac{\partial f}{\partial \varphi_{i+1}} &= \frac{1}{\Delta^2} = c_{i+1} \end{aligned} \quad (6.23)$$

This helps us to transform the nonlinear second order differential equation into a coupled linear equations, which can be expressed in matrix form as:



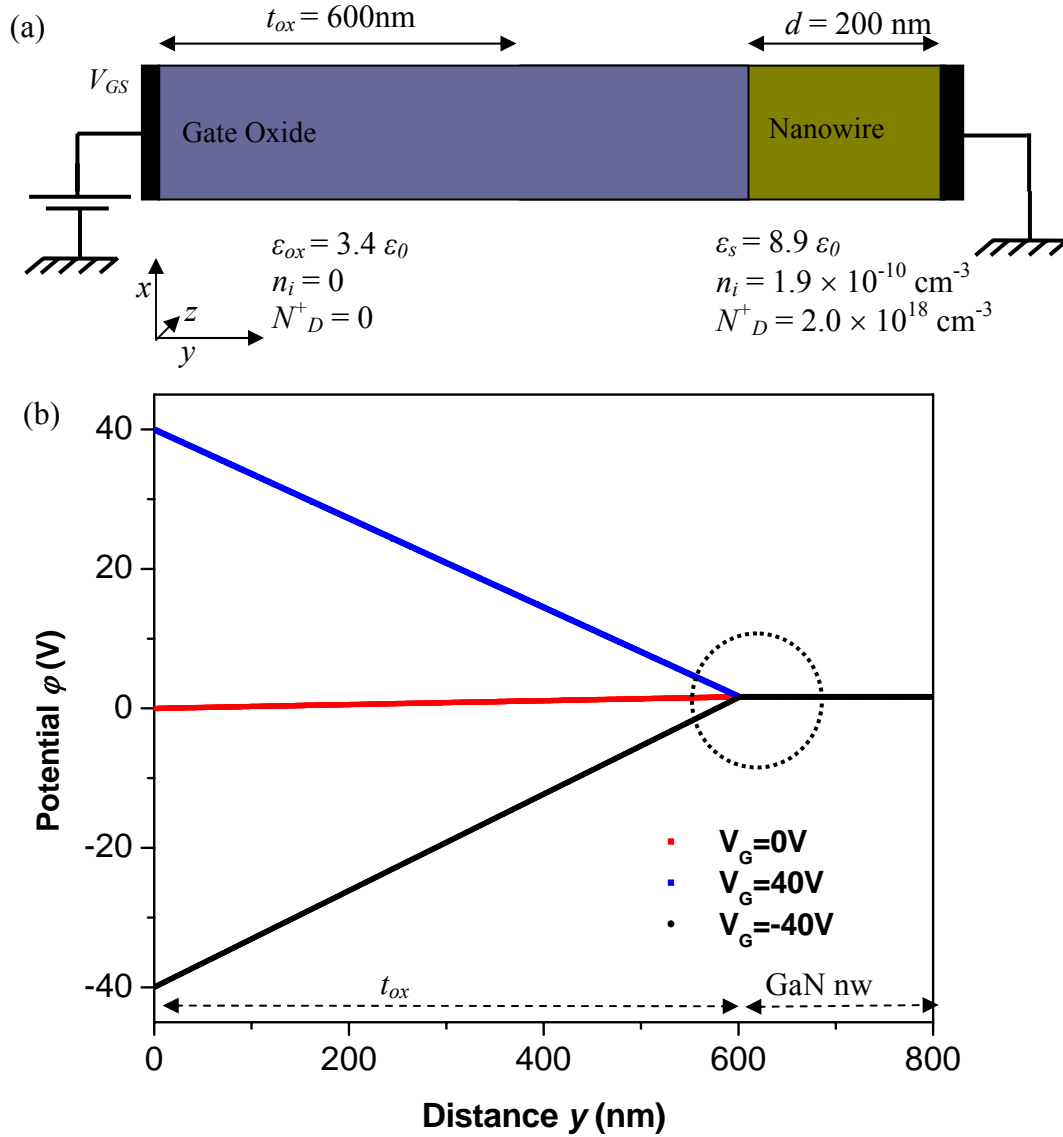
With every iteration, we compute  $\Delta\phi$  and update  $\phi$  with  $\phi+\Delta\phi$  for the next iteration. Convergence is achieved when  $\Delta\phi < (1 \times 10^{-5} \times V_t)$ . The flow chart for the algorithm is shown in Fig. 6.22.



**Fig. 6.22:** Flow diagram showing the implementation of the 1-D Poisson solver for MOSCAP.

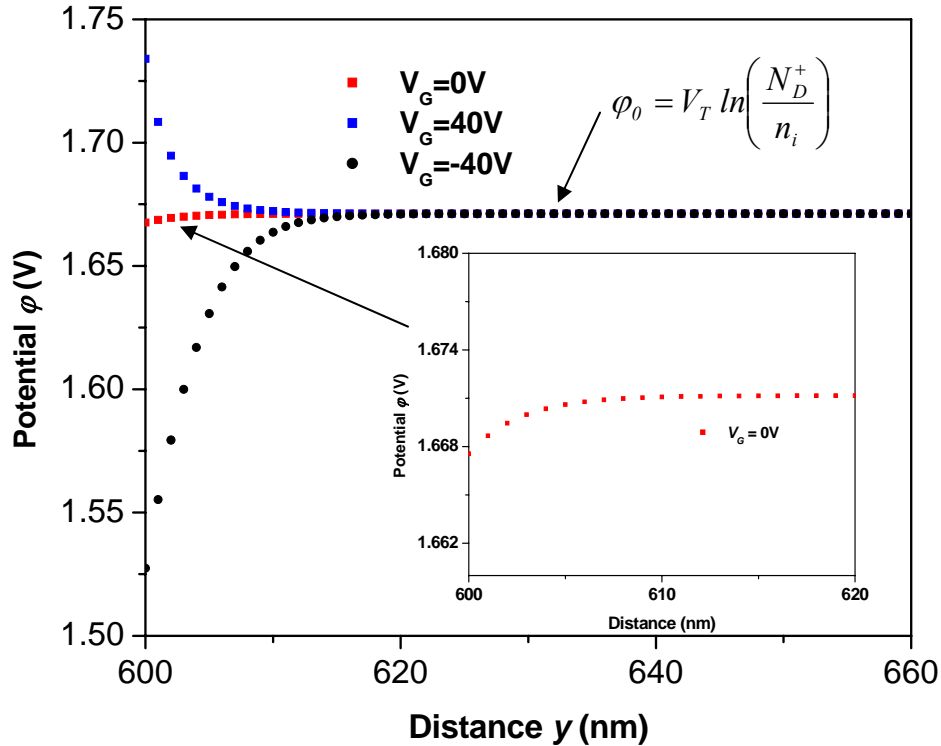
The numerical solutions for the potential for different applied gate biases are shown in the plot below in Fig. 6.23. We have simulated the back-gate devices where for gate oxide we have used 600 nm of  $\text{SiO}_2$ . The potential drop across the Si wafer is not considered in the calculation as it is negligible due to its heavy doping level.

The nanowire is assumed to be of 200 nm diameter and with a doping density of  $2 \times 10^{18} \text{ cm}^{-3}$  as obtained in section 6.1.2.



**Fig. 6.23:** (a) 1-D nanowire MOSCAP with dimensions as indicated in the figure, (b) numerically calculated potential profile for the MOSCAP for different gate bias. It can be seen that most of the potential drop occurs in the oxide, which is expected due to its thickness. The potential in the nanowire region, as indicated by the broken black line, is shown in the next figure.

In order to get a feel for the potential drop in the nanowire drop we plot the potential only in the nanowire region (as indicated by the broken black line in Fig. 6.23) in Fig. 6.24.



**Fig. 6.24:** Potential profile in the nanowire region for different gate bias levels. (inset) the potential profile for zero gate bias showing the depletion associated with fermi level alignment through out the system. The thermal equilibrium potential is also shown in the plot.

One can clearly see that channel potential is changing with the applied gate bias. One can assure that the model is working properly as it correctly predicting the thermal equilibrium depletion region. This is inherent to any metal-semiconductor system due to realignment of the fermi level. Once we have simulated the channel potential as a function of the gate voltage, we now can determine the channel carrier concentration as a function of distance with different gate voltages. In the liner region the channel current can be related to the current density by the relationship:

$$I_{DS}(lin)(z) = \int_0^W \int_0^W J(z) dx dy \quad (6.25)$$

where  $J(z)$  is the current density in the  $z$  direction,  $W$  is the width of the nanowire in  $x$  and  $y$  directions. Substituting for  $J(z)$  in the relationship:

$$I_{DS}(lin)(z) = \int_0^W \int_0^W n q v_d dx dy \quad (6.26)$$

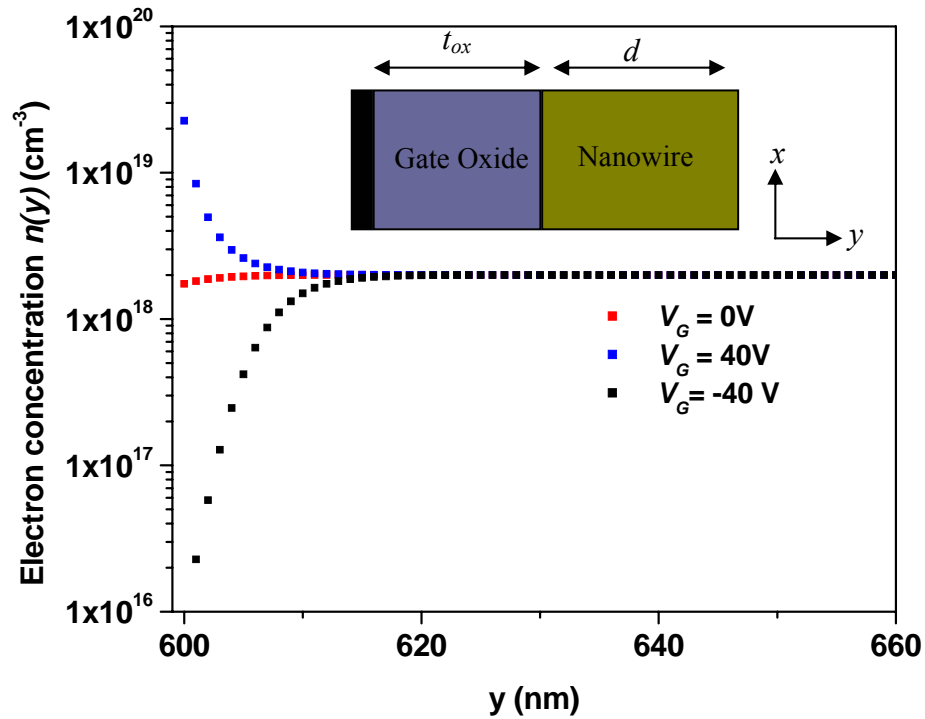
where  $n$  is the majority carrier concentration,  $q$  is the electronic charge, and  $v_d$  is the electron drift velocity. For our case  $n$  is a function of  $y$  only, hence the equation simplifies to:

$$I_{DS}(lin)(z) = q v_d \int_0^W dx \int_0^W n(y) dy \quad (6.27)$$

As drift velocity is given by the relationship  $v_d = \mu_n E_z = \mu_n V_{DS}/L$ , substituting that into the Eq. 6.27, we get

$$I_{DS}(lin)(z) = q \mu \frac{V_{DS}}{L} W \int_0^W n(y) dy \quad (6.28)$$

Once we have the numerically computed  $\phi(y)$ , we can compute the electron concentration profile as both are related by the Eq. 6.12. Once we have the electron concentration profile, integral in Eq. 6.28 can be calculated numerically. The numerical calculation is done using the Origin<sup>®</sup> plotting program. The plot in Fig. 6.25 shows the electron concentrations in the  $y$  direction for different gate voltages. Depletion for negative gate voltages and accumulation for positive gate voltages can be seen in the plot.

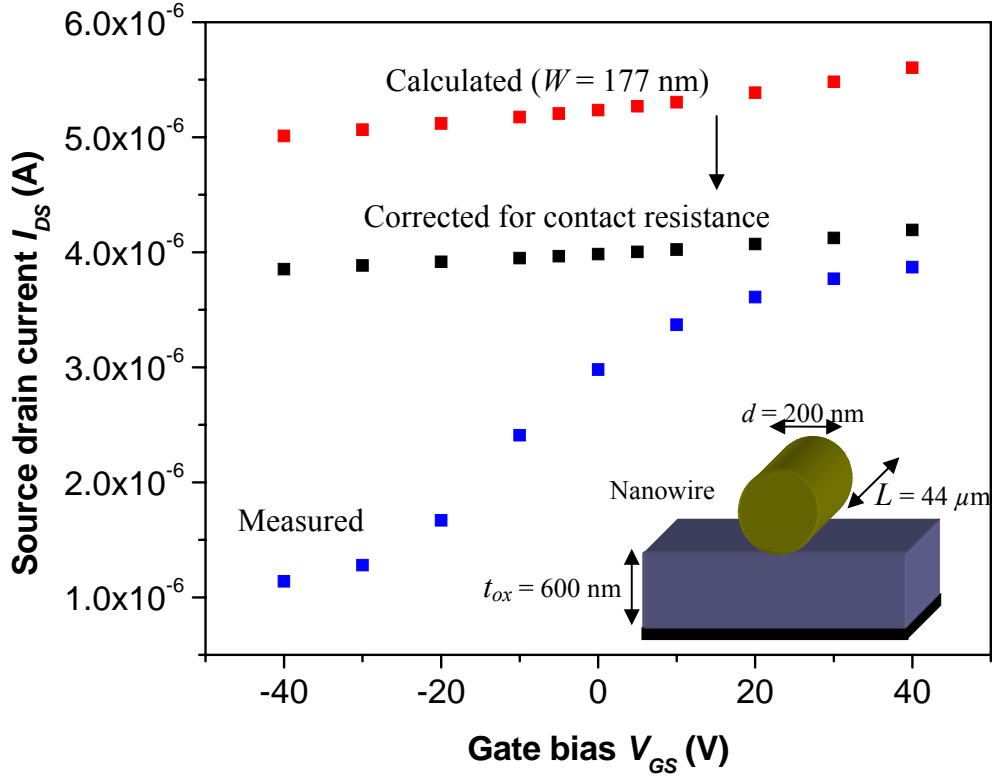


**Fig. 6.25:** Electron concentration as a function of distance in  $y$  direction for different applied gate bias. Depletion and accumulation for negative and positive gate voltages respectively can be seen in the plot.

In order to compute the channel current using Eq. 6.28, we substitute the measured mobility, and carrier concentration. We also assume a square cross-section of the nanowire as shown in Fig. 6.18 (c) instead of a circular cross-section., with width  $W$ , which is related the diameter of the nanowire by  $W = \sqrt{\pi d}/2$ . This ensures that the cross-sectional area for the square and circular geometry is equal. The 1-D numerical solution of the channel current for 1 V source drain bias for a nanowire FET is shown together with the measured value in Fig. 6.26. The numerically calculated channel current as shown in Fig. 6.26 (red squares), is higher than the measured value (blue squares). This is probably due to the fact that we have simulated the potential in only



one dimension, whereas the channel potential is affected by the gate in both the dimensions. The effect of contact resistances are also not taken into the account in calculating the channel current.



**Fig. 6.26:** Comparison of numerically calculated channel current (red squares) and measured channel current (blue squares) for a nanowire FET with 1 V  $V_{DS}$ . The calculated channel current is also corrected for the contact resistances (black squares).

We can correct for the contact resistances as explained here. The channel current with the contact resistance can be expressed as:

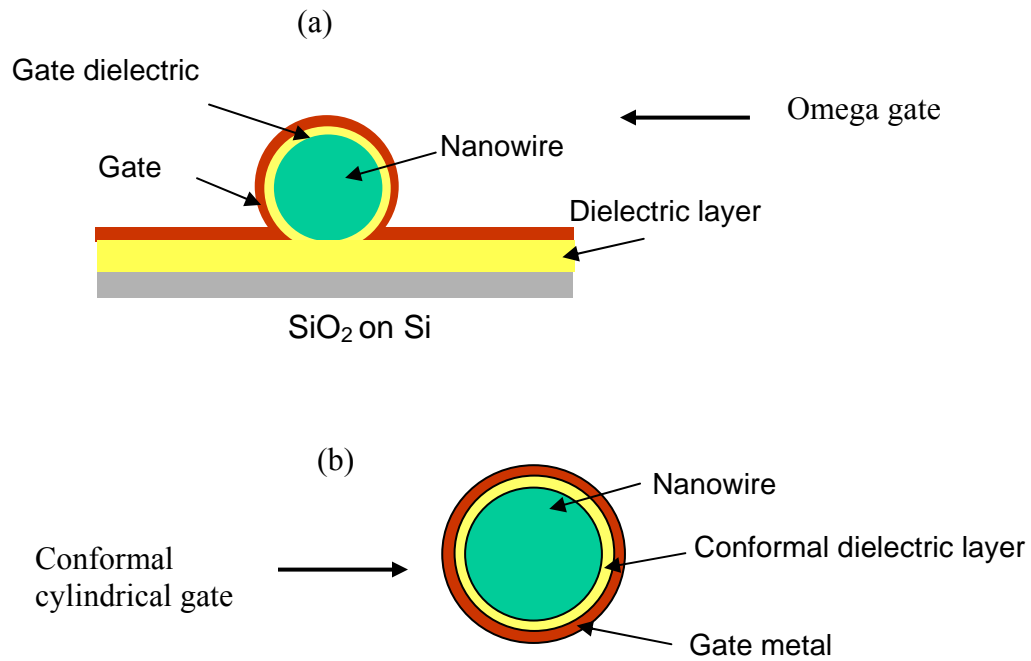
$$I_{DS} = [2R_C + R_{ch}(V_{GS})] \times V_{DS} \quad (6.29)$$

where  $R_C$  is the contact resistance. In later section we will describe how we can estimate the contact resistances for a Ti based contacts to a GaN nanowire. Assuming that the contact resistance is in the order to  $30 \times 10^3 \Omega$ , we plot the calculated channel

current corrected for contact resistance. Corrected channel current at high gate biases are in good agreement with the measured channel current. At negative biases the corrected calculated channel current is much higher than the measured value, which is expected with the one dimensional simulation. In order to accurately compute the channel current, we have to compute the channel charge for the whole cross-section.

## **6.2 Top Gate Devices**

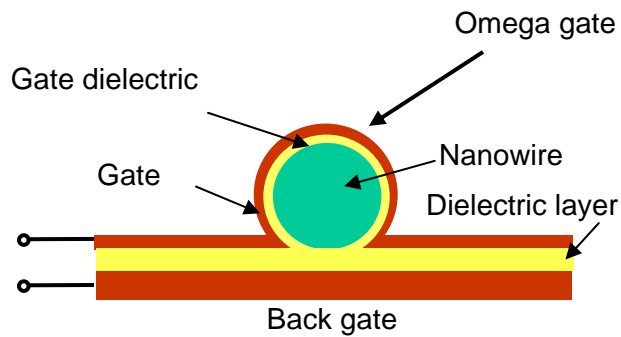
As we have seen in the previous section that the transconductance of a bottom gate device is quite low. One reason for this is the thick gate oxide and other is the less effective gate geometry. One can reduce the gate oxide thickness and use more effective gate geometry to increase the device transconductance. Many different types of gate geometries have been used for nanowire devices with two most important being omega shaped gates and conformal cylindrical gates (as shown in Fig. 6.27). Conformal cylindrical gate is the ideal gate geometry as it provides the highest gate capacitance. Nonetheless conformal gate metals are difficult to deposit as techniques for depositing conformal materials such as atomic layer deposition techniques are well suited for depositing oxides but not for metals. Also in the case of GaN nanowires with conformal gate geometry, with the gate oxide and gate metal being deposited before the source drain contact formation, one has to ensure the thermal stability of the gate stack during the high temperature annealing for source drain Ohmic contact formation. In this section we will discuss two different fabrication methods to obtain circular gate geometries, utilizing only standard photolithography, oxide deposition (PECVD), and etching.



**Fig. 6.27:** (a) The omega shaped gate structure, (b) conformal cylindrical gate.

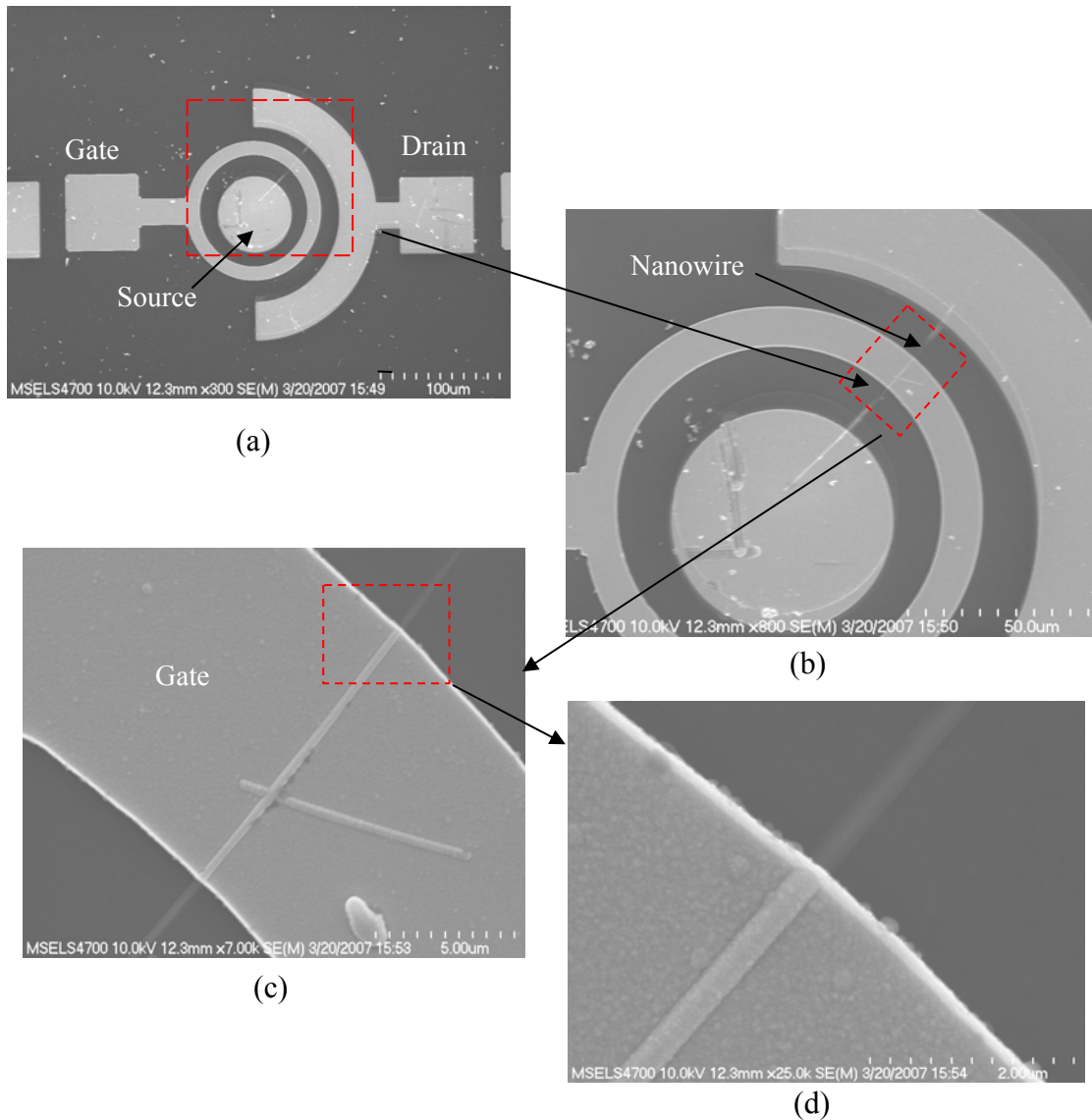
### 6.2.1 Omega-Backgate Geometry

We have used the heavily doped Si substrate as a back-gate in conjunction with a regular omega shaped gate to achieve a structure which is termed as an omega-backgate FET. The schematic of the device is shown below in Fig. 6.28.



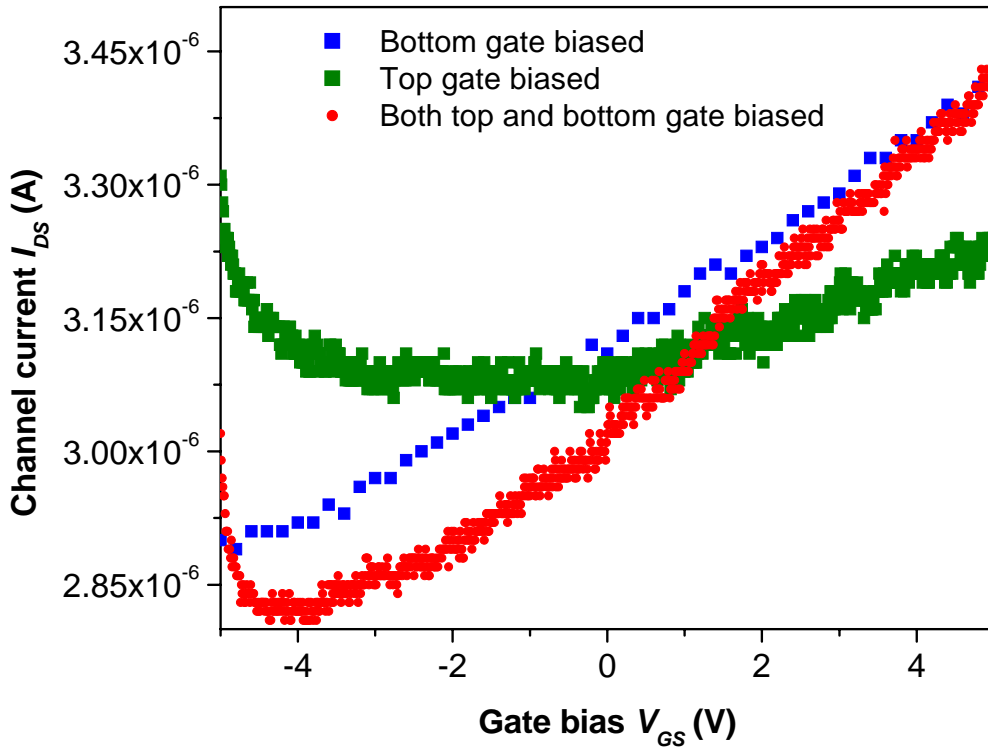
**Fig. 6.28:** Schematic representation of the omega-backgate structure.

As the top gate and the bottom gate are externally connected, this configuration has a unique advantage. This device can be operated in three distinct configurations: a) top gate biased and bottom gate floating b) top gate floating and bottom gate biased and c) both top and bottom gate biased. A SEM image of a complete device is shown Fig. 6.29.



**Fig. 6.29:** FESEM image of an omega-backgate device. (a) The complete device with source/drain and gate contacts, (b) high magnification scans of the area with the nanowire, (c) the gate on top of the nanowire, and (d) the omega shape of the gate is clearly visible.

For this device, we deposited 85 nm of SiO<sub>2</sub> on heavily doped p-Si substrate. This was followed by the standard procedure for source drain formation. After the nanowire alignment, another layer of SiO<sub>2</sub>, 85 nm thick was deposited using PECVD. This layer is the top gate oxide. This was followed by source/drain contact formation as described in chapter 5. Top gate was formed by lithography and metal deposition (Ni/Au -30/50 nm).



**Fig. 6.30:** Transconductance plot ( $I_{DS}$  vs  $V_{GS}$ ) for the omega-backgate device with different configurations of the top and back gate. The diameter of the nanowire is 205 nm.

The plot shown in Fig. 6.30 is for all three combinations of the gate biasing as described earlier. The omega top gate produces less drain current change than the bottom gate as the top gate covers only a portion of the nanowire, whereas the bottom gate extends along the entire length of the nanowire between the source and

the drain contacts. The largest gate modulation is produced by biasing both the top and the back gate. Transconductance per unit gate width for three different gate configurations are presented in the table below for the omega-backgate FET (Table 6.3).

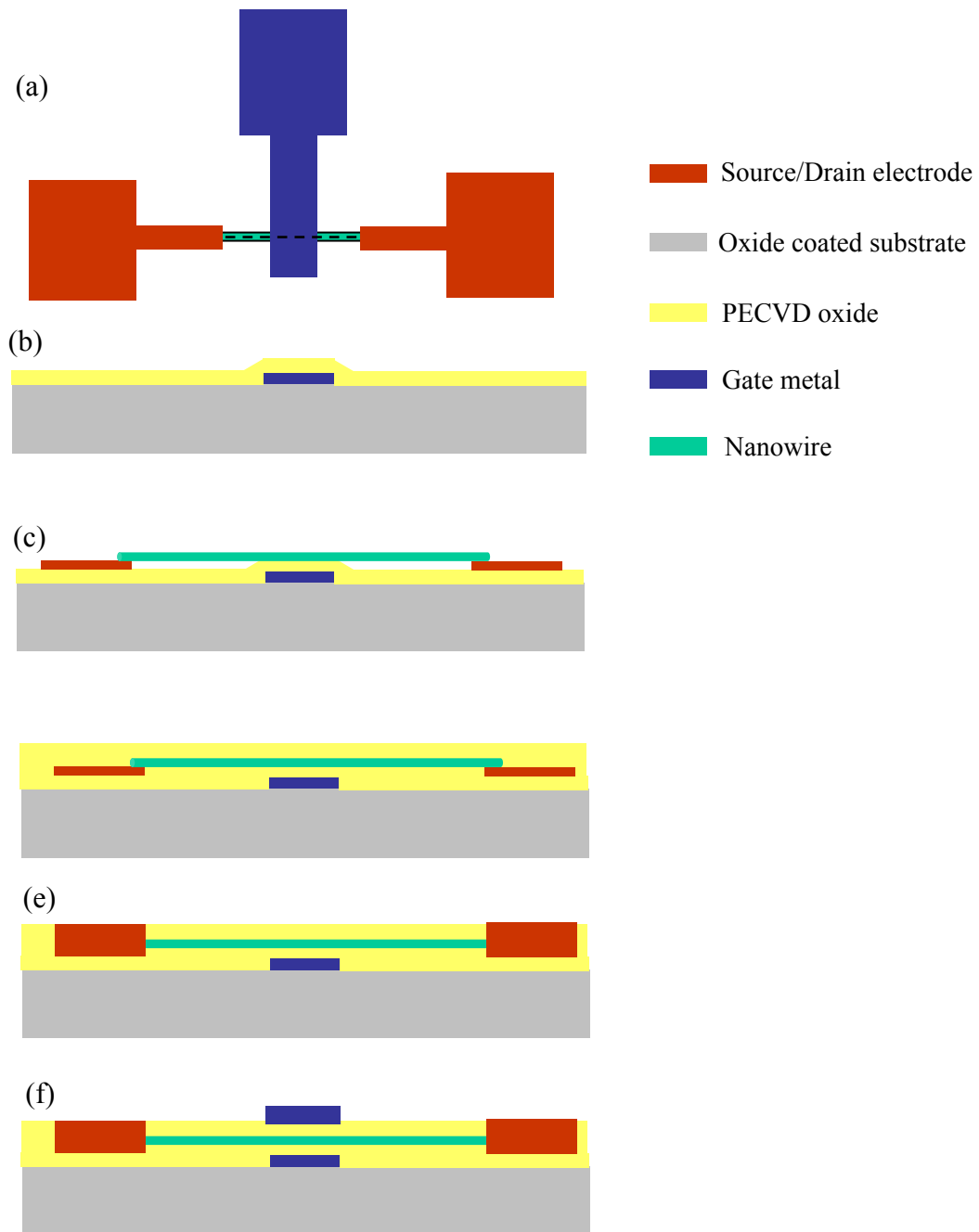
**Table 6.3:** Comparison of transconductances, and normalized transconductances for the omega-backgate FET, with 200 nm diameter nanowire.

Gate configuration	Transconductance $g_m$ (S)	Normalized transconductance $g_m/W$ ( $\mu\text{S}/\text{mm}$ )
Top gate floating-bottom gate biased	$5.7 \times 10^{-8}$	285
Top gate biased-bottom gate floating	$3.2 \times 10^{-8}$	160
Both top and bottom gate biased	$6.9 \times 10^{-8}$	345

It is clear that applying bias to both top and bottom gate results in increased transconductance as compared to the case where bias is applied to either one of them. When the bias is applied to the backgate it affects the entire nanowire, hence the conductance change is large. For the top-gate configuration, the source and drain parasitic resistances are quite large as they are comprised of the contact resistances and the resistance of the un-gated portions of the nanowire. Thus for a top-gate configuration the FET performance is limited by the source and drain resistances.

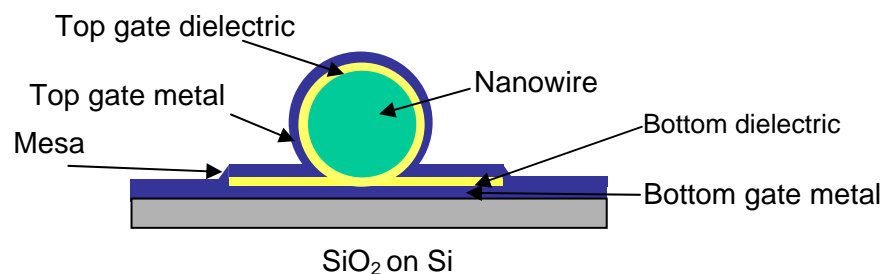
### 6.2.2 Omega-Plane Gate

In this design we have used a plane metal bottom gate, formed by photolithography and metal deposition, together with an omega shaped top gate connected around the nanowire to form a circular gated nanowire FET structure.



**Fig. 6.31:** Schematic fabrication process flow for omega-plane gate FET. (a) The plan view of the structure, (b) bottom gate stack formation, (c) nanowire alignment, (d) PECVD oxide coating, and (e) top gate formation.

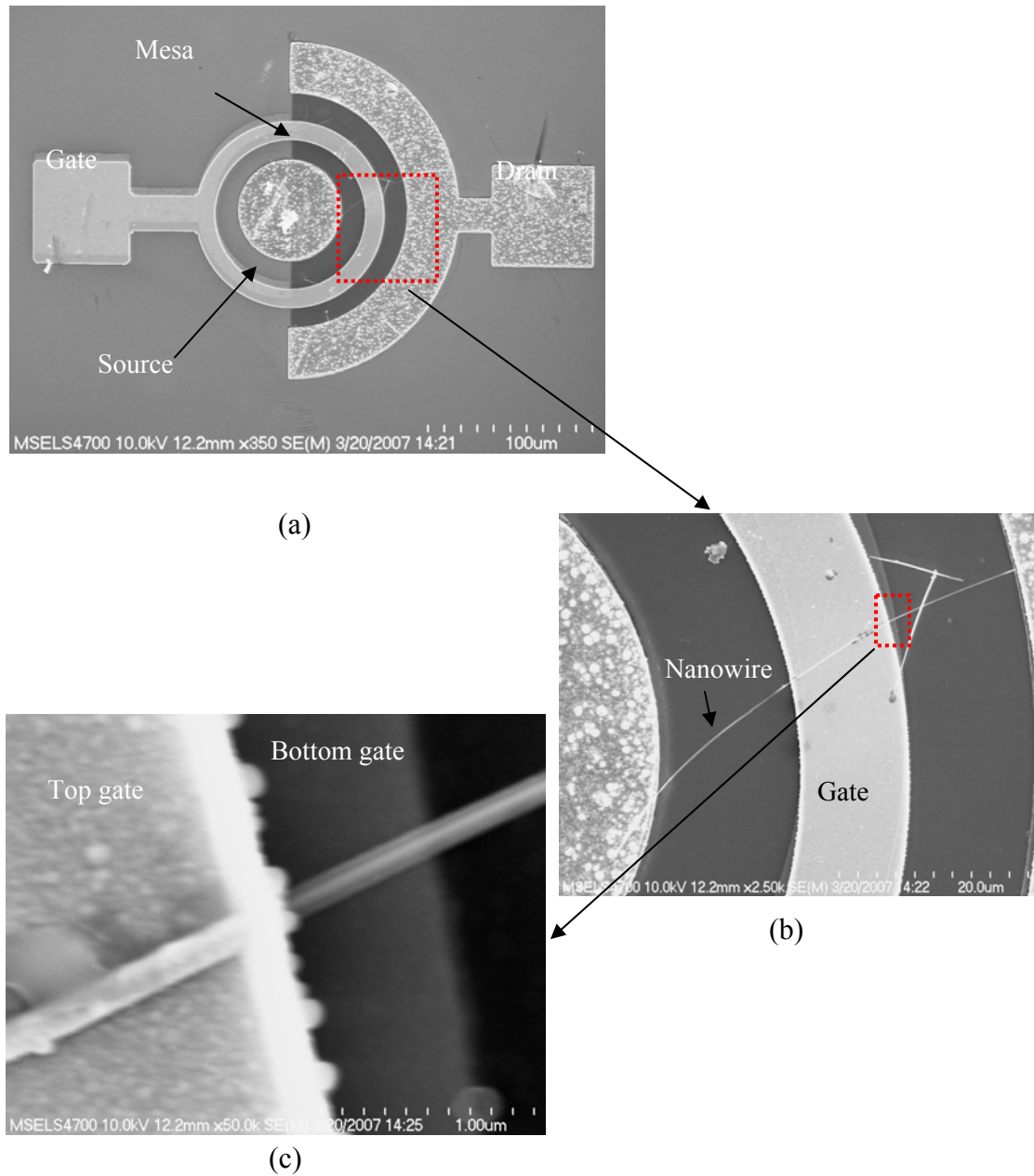
The complete fabrication sequence for developing an omega-plane gate FET is shown in Fig. 6.31. For developing this omega-plane gate geometry we started with a standard 600 nm SiO<sub>2</sub> coated Si wafer with the gate electrode pattern defined by optical lithography. A 50 nm of Ni is deposited followed by lift-off to form the first layer gate metal [Fig. 6.31(b)]. Using PECVD then we deposit 50 nm of SiO<sub>2</sub>, which serves as the bottom gate oxide. Next we form the source drain alignment electrodes by lithography and lift-off and align nanowires between the source drain electrodes using DEP [Fig. 6.31(c)]. A second 50 nm SiO<sub>2</sub> is deposited then forming the top gate oxide layer [Fig. 6.31(d)]. A mesa is developed using reactive ion etching and photoresist as a mask, to remove the top oxide everywhere except along small square area right over the nanowire. This ensures that the top and bottom gate will be connected. A fourth photolithography and metal deposition (Ti/Al/Ti/Au-30/100/30/100 nm) forms the source drain contacts [Fig. 6.31(e)]. A slow anneal step at 500 °C is performed to make the contacts Ohmic. A low temperature anneal is chosen to ensure the thermal stability of the lower gate stack. A fifth photolithography step defines the top gate electrode, followed by Ni/Au (30/50 nm) deposition [Fig. 6.31(f)]. Schematic of the cross-section of a completed omega-plane gate FET is shown in Fig. 6.32



**Fig. 6.32:** The schematic cross-section of omega-plane gate FET.

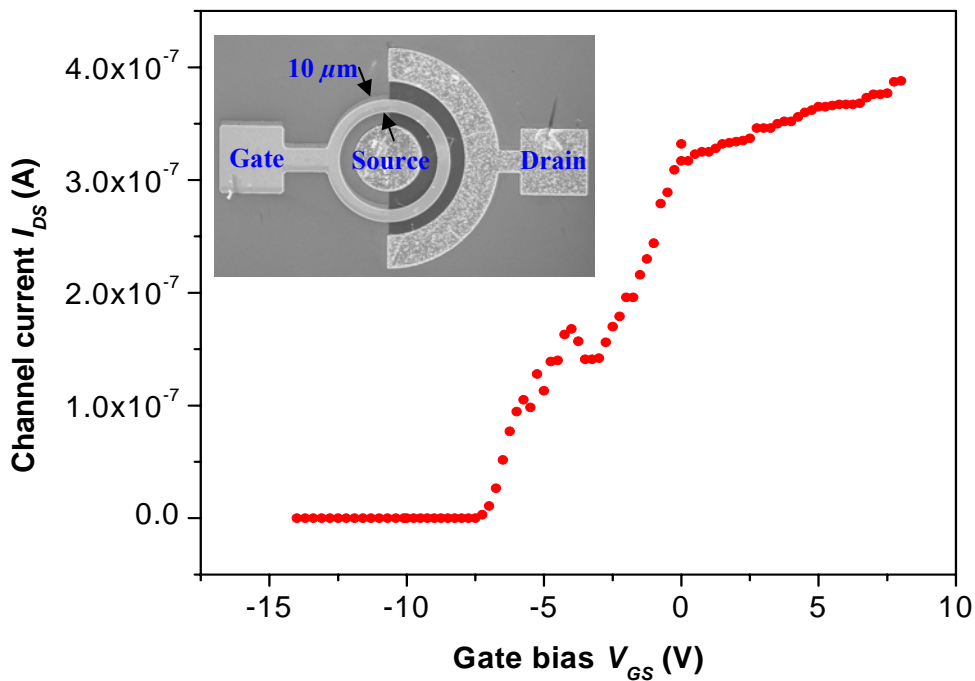


A complete device with a nanowire with both top and bottom gates are shown in Fig. 6.33. The diameter of the nanowire was 130 nm.



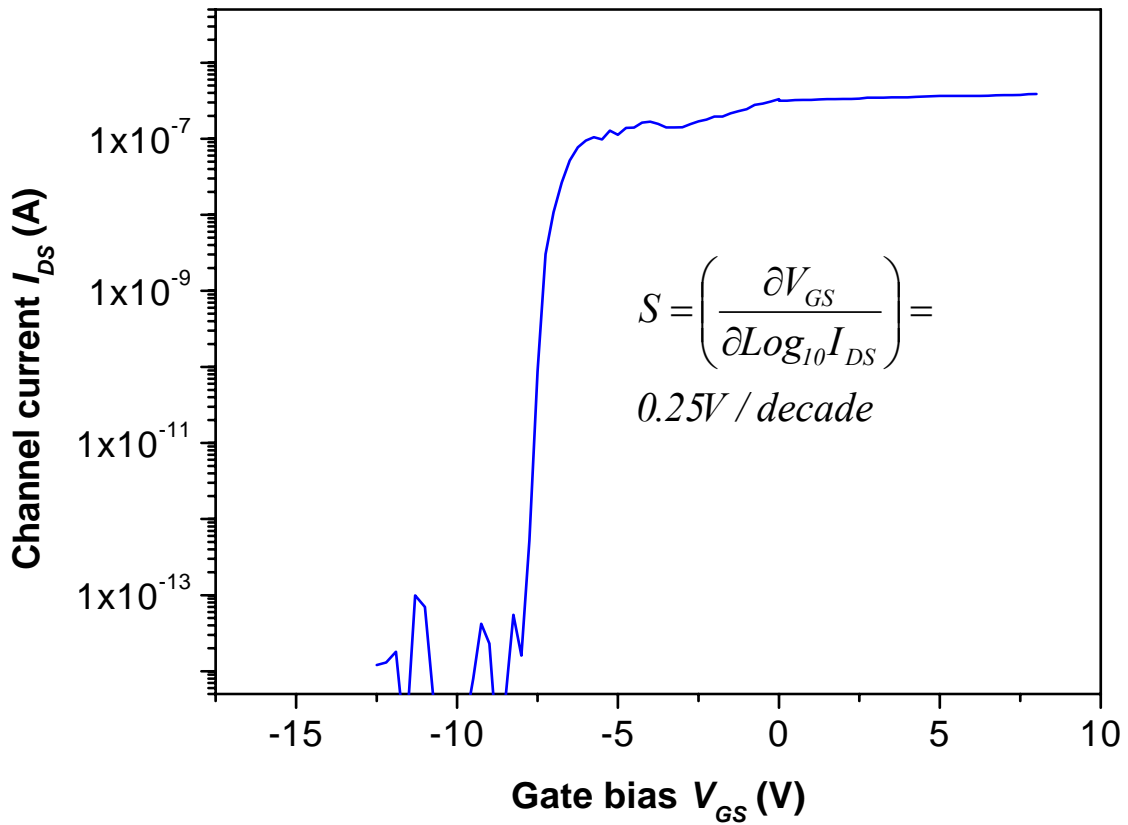
**Fig. 6.33:** FESEM image of an omega-plane gate device. (a) The complete device with source/drain and gate contacts, (b) high magnification scans of the area with the nanowire, (c) both top and bottom gates are visible due to a small misalignment of the two lithography steps.

The gate length for this device is about  $10\ \mu\text{m}$ . Due to a small lithographic misalignment, the bottom and top gates are clearly visible in Fig. 6.33(c). This device could be completely turned off at a gate bias of  $-8\ \text{V}$  (Fig. 6.33), which is about an order of magnitude lesser than the nanowire FETs with  $600\ \text{nm}$  backgate oxide. A linear version of this also fabricated (not shown here). Transconductance per unit gate width is about  $301\ \mu\text{S}\ \text{mm}^{-1}$ , which is about double for the same diameter nanowire with  $600\ \text{nm}$  of back gate oxide (see Fig. 6.9).



**Fig. 6.34:** Transconductance plot ( $I_{DS}$  vs  $V_{GS}$ ) of an omega-plane FET with a nanowire of diameter  $130\ \text{nm}$  and gate length of  $10\ \mu\text{m}$ . The source drain bias  $V_{DS}$  is  $6\ \text{V}$ . (inset) SEM image of the device with source, drain, and gate electrode shown.

From the transconductance plot for the device, it is clear that the gate modulation of the channel current is much higher than the back-gated device of the same diameter range (compare Fig. 6.8 and Fig. 6.34). The semi-log plot of channel current as function of gate voltage is shown in Fig. 6.35. The on-off current ratio for this device was  $10^6$ .



**Figure 6.35:** Semi-log plot of the channel current of the omega-plane FET, with the sub-threshold voltage indicated. Transconductance plot of the device is shown in Fig. 6.34.

The sub-threshold slope for this particular device was 0.25 V/decade which is an order of magnitude lower than bottom gate devices with similar diameters (see Fig. 6.10). For estimating the effectiveness of this design and comparing it with that of the omega-backgate geometry, we have to fabricate devices with different diameters and

different gate oxide thicknesses. Transconductances for this geometry ( $301 \mu\text{S mm}^{-1}$ ) is little lower than the omega-backgate devices ( $3450 \mu\text{S mm}^{-1}$  with both the gate connected), which is probably due to the high source/drain parasitic resistances. Carrier concentration for this device can be calculated using the calculated Eq 6.9. For the capacitance we have to use the standard formula for the cylindrical capacitance given in the Eq. 6.30.

$$\frac{C}{L} = \frac{2\pi\epsilon_0\epsilon_{ox}}{\ln\left(\frac{d+t_{ox}}{d}\right)} \quad (6.30)$$

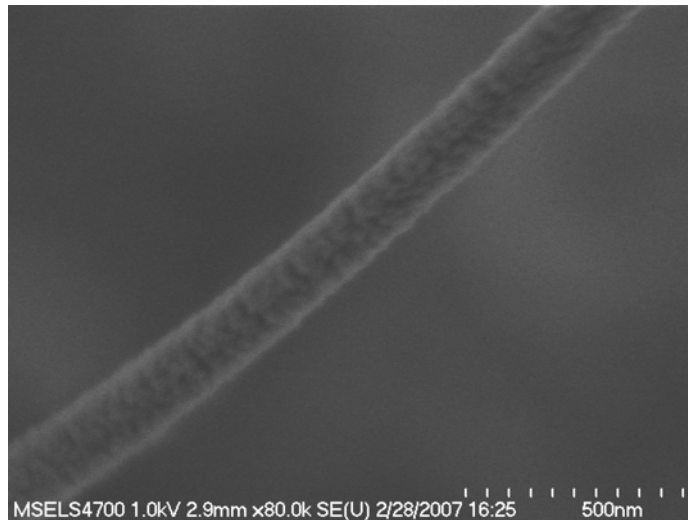
In this equation  $L$ ,  $d$ , are the length and diameter of the nanowire respectively and  $t_{ox}$  is the thickness of the oxide. For this device the calculated carrier concentration was about  $2.5 \times 10^{18} \text{ cm}^{-3}$ . This value is similar to the doping density calculated for 100 nm diameter nanowire FET with backgate. This indicates that the material properties are quite consistent in our nanowires.

Comparing the performances of preset nanowire FET device designs with various conventional thin film MOSFETs and nanowire MOSFETs is quite helpful as it indicates the future directions and possibilities for our device. Table 6.4 presents such a comparison. It is clear that the transconductances are lower for the present devices. There could be number of reasons for this. Most dominant is the parasitic source and drain resistance due to incomplete coverage of the gate. The thickness and shape of the gate are also crucial parameters. Using thinner gate oxide we could be able to increase the transconductance, but it would also increase the gate leakage. Figure 6.36 is a SEM image of a GaN nanowire coated with  $\text{Al}_2\text{O}_3$  using pulsed laser

deposition system, which used a pulsed laser to ablate a solid target of  $\text{Al}_2\text{O}_3$  to deposit the conformal coating of the oxide.

**Table 6.4:** Comparison of FET parameters for convention thin film MOSFETs, Carbon nanowire and Si nanowire FETs, and GaN nanowire FETs obtained in the present study.

FET Parameters	Conventional thin film MOSFETs [78]		Nanowire FETs [79],[80]		GaN nanowire FETs (present study)		
	SOI Si FET	GaN FET	Carbon nanotube FET	Si nanowire FET	Back-Gate	Omega-backgate	Omega-plane
Transconductance ( $\mu\text{S mm}^{-1}$ ) $\times 10^3$	650	15	30	17	0.2	.34	0.30
Sub-threshold slope (V/decade)	0.07	0.4	1	0.17	6.5	-	0.25
On-off current ratio ( $I_{on}/I_{off}$ )	$7.0 \times 10^4$	$1 \times 10^7$	$1 \times 10^5$	$1 \times 10^3$	$1 \times 10^7$	-	$1 \times 10^6$
Field effect mobility ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ )	-	160	2000	230	320	-	-

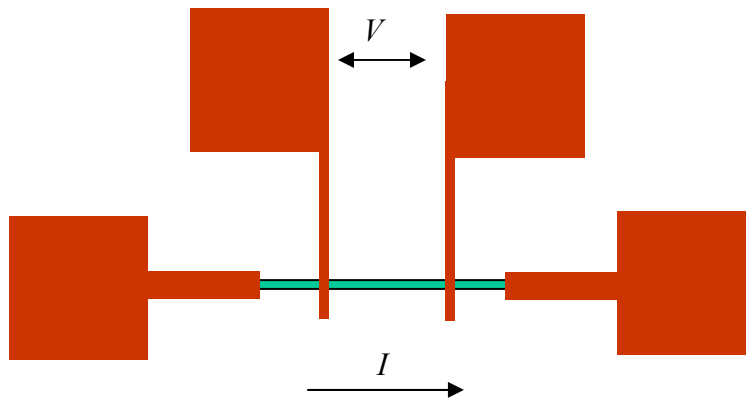


**Fig. 6.36:** Pulsed laser deposited  $\text{Al}_2\text{O}_3$  on GaN nanowire. The conformal coating of the oxide is clearly visible.

Using these techniques we can deposit high dielectric constant gate materials ( $\text{HfO}_2$ ,  $\text{TiO}_2$ , etc) with a conformal coverage, which can enhance the device performances dramatically.

### 6.3 Four-Terminal Resistivity Structures

Determining the resistivity of semiconducting material accurately is important as it enables us to estimate various intrinsic material properties that are important for device realization and usage. Four-terminal structures as shown in Fig. 6.37 are usually used to measure resistivity of any material, where current is forced between the outer two pads and voltage drop due to the current flow is measured between the inner two pads. This geometry ensures that the contact resistances are not included in the intrinsic material resistance.



**Fig. 6.37:** Four-terminal structure for nanowire resistivity measurements.

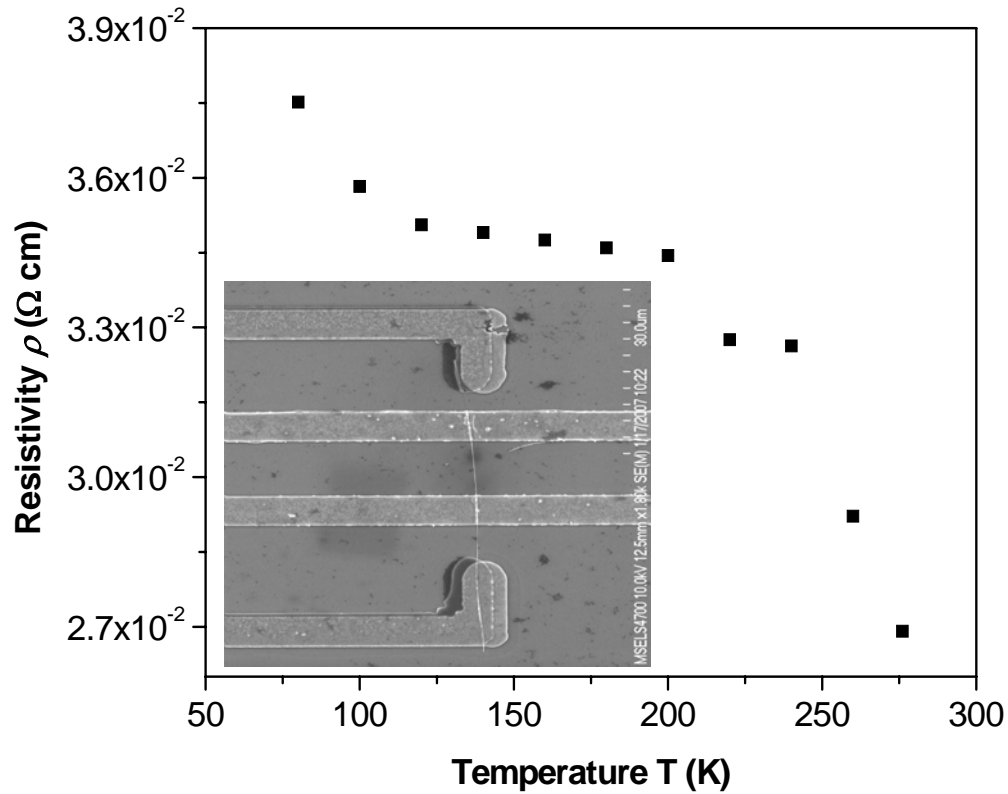
Utilizing this structure we can measure host of different material properties such as:

- (a) independent determination of carrier concentration or mobility from the resistivity measurement
- (b) contact resistance
- (c) temperature dependent resistivity measurements, which provides the activation energy of the dopants, and
- (d) temperature dependent mobility using the inner two contacts and the back gate.

The SEM image of a 4T structure is shown in the inset of Fig. 6.38. The diameter of this nanowire was 132 nm and length between the inner two pads was 8.9  $\mu\text{m}$ . The resistivity for this nanowire from 4T measurement was  $2.69 \times 10^{-2} \Omega \text{ cm}$ , which is quite close the value obtained utilizing FIB deposited 4T structures as described in chapter 3. With the inner two contacts acting as source and drain electrode and the Si substrate as a backgate, we determined the mobility for this nanowire at 270 K, which was around  $65 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . Using the measured resistivity and mobility, we calculated the carrier concentration for this nanowire using EQ, which is about  $3.5 \times 10^{18} \text{ cm}^{-3}$ . This value is remarkably close to the value obtained from threshold voltage calculation. Contact resistance can be calculated by measuring the 2T resistivity using the inner two contacts and then subtracting the resistance of the nanowire, which is known from the resistivity of the nanowire. For this particular nanowire the contact resistance calculated was around 150 k $\Omega$ , which results in a specific contact resistance of about  $5 \times 10^{-5} \Omega \text{ cm}^2$ . Specific contact resistance of standard Ti/Al/Ti/Au contacts to GaN thin films annealed at 750  $^\circ\text{C}$ , is in the range of  $3.0 \times 10^{-6} \Omega \text{ cm}^2$  (as discussed in chapter 5). The higher specific contact resistances for these contacts to the GaN nanowires could be due to the lower annealing temperatures than thin films.

Temperature dependent resistivity measurement was carried out on this nanowire from room temperature (276 K) down to liquid nitrogen temperature (77 K). It is clear that the resistivity is weekly dependent on the temperature for these nanowires (Fig. 6.38). The temperature dependent resistivity does not fit the activation energy model. Activation energy of 1.1 meV is calculated for this

nanowire. As these nanowires are unintentionally doped, point defects such as impurity (oxygen), and nitrogen vacancies are the likely sources of the excess carrier concentration.



**Fig. 6.38:** Resistivity of a GaN nanowire as a function of temperature. (inset) SEM image of the 4T structure for measuring the resistivity.

Un-intentionally doped GaN thin films are always n-type, with nitrogen vacancies and other structural defects such as dislocations acting as shallow donors. Oxygen is a shallow donor with ionization energy of 28 meV, and nitrogen vacancy has activation energy of 30 meV. This weak dependence of the resistivity of the present nanowire is only possible if the ionization energy of the dopants is negligible small. Impurities in semiconductors are generally represented as a localized level at a fixed energy with



respect to the valence or conduction bands. This model breaks down when impurity concentration approaches the conduction band or valence band density of states. It is a well know observation in other semiconductors that the ionization energy decreases with increasing impurity concentration. The ionization energy goes to zero at the impurity concentration where metallic impurity conduction occurs. This transition has been predicted to occur when the ratio of average separation  $r$  of the impurity atoms to the radius of the hydrogen-like impurity  $a^*$  is about 3 [81]:

$$r/a^* \approx 3.0 \quad (6.31)$$

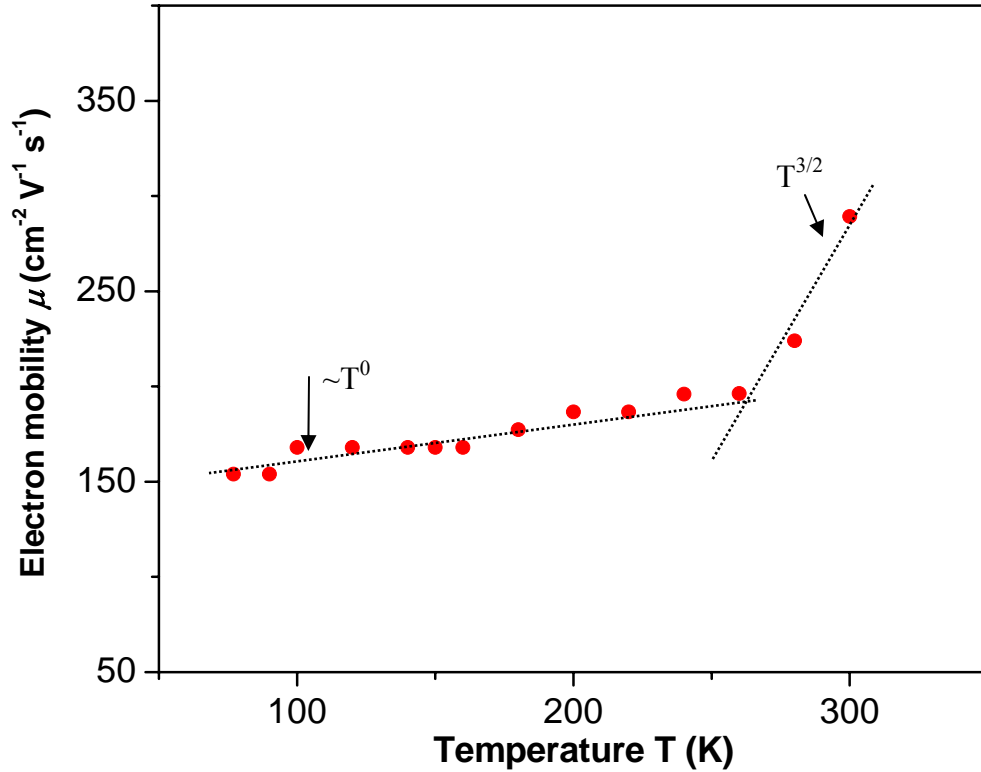
where  $r$  and  $a^*$  is given by the relations

$$r = \frac{3}{4\pi N}, \quad a^* = \left( \frac{\epsilon_s}{\epsilon_o} \right) \left( \frac{m_o}{m^*} \right) 0.5 \times 10^{-8} \text{ cm} \quad (6.32)$$

$N$  is the dopant concentration,  $\epsilon_s$  and  $\epsilon_o$  are the dielectric permittivity of semiconductor and vacuum respectively,  $m_o$  and  $m_s$  are the free electron mass and electron effective mass in the semiconductor. For GaN with  $\epsilon_s/\epsilon_o = 8.9$  and  $m_s/m_o = 0.2$ , the dopant concentration  $N$  which satisfies the Eq. 6.32 is about  $8 \times 10^{17} \text{ cm}^{-3}$ . In the previous section we have seen that the donor concentrations in these nanowires are in excess of  $1 \times 10^{18} \text{ cm}^{-3}$ . Thus with the ionization energy extremely small, the resistivity is only weakly dependent on the temperature for these nanowires.

Temperature dependent mobility measurement on the 2T structure is carried out to reveal the dominant scattering mechanisms in these nanowires. Plot of mobility of a 200 nm diameter nanowire as function of temperature is shown in Fig. 6.39. In thin film enhancement mode MOSFET devices the field effect mobility is always smaller than the drift mobility, as the charge conduction takes place at the oxide-

semiconductor interface region, where the scattering is usually enhanced. Due to high carrier concentrations in these nanowires, the majority of the channel conduction occurs in the un-depleted portion of the nanowire; hence the field effect mobility would closely resemble the drift mobility in these nanowires.



**Fig. 6.39:** Measured field effect electron mobility of a GaN nanowire (diameter 200 nm) as a function of the temperature. Dotted lines represent the non-degenerate and degenerate dependences.

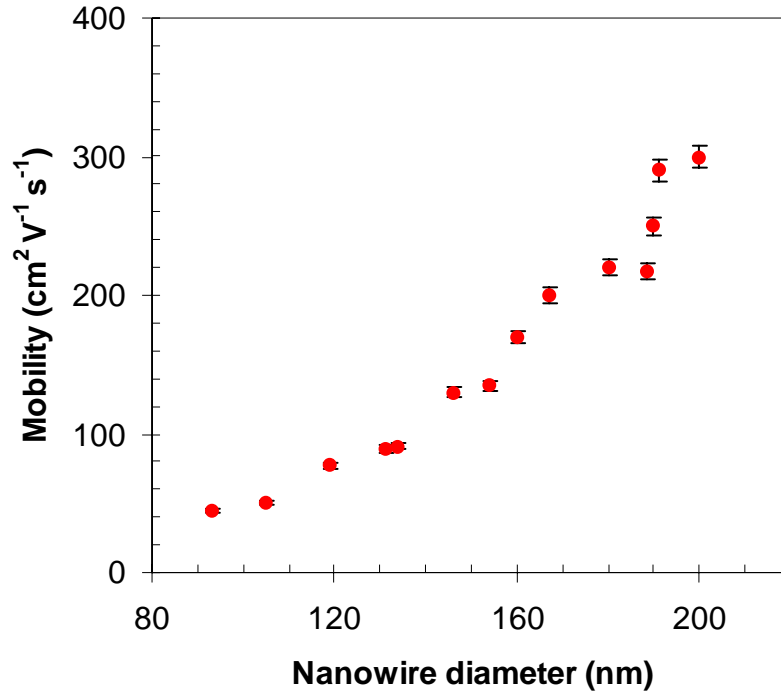
In high quality non-degenerate GaN thin films and bulk crystals, mobility is dominated by polar optical phonon, piezoelectric acoustic phonon, and ionized impurity scattering at high, moderate, and low temperatures, respectively. Electron mobility initially increases with decreasing temperature, and the transition to ionized impurity dominated scattering is accompanied by a maximum in the mobility curve.

For lower temperatures, the mobility has a  $T^{3/2}$  temperature dependence. For our case we do not observe a regime where mobility increases with decreasing temperature, meaning that the ionized impurity scattering is the dominant process in the temperature range studied. Brooks-Herring ionized impurity scattering predicts  $T^{3/2}$  and  $T^0$  dependences assuming asymptotically non-degenerate and degenerate distributions [82], respectively, and the measured field-effect mobility fits these dependences well in the high temperature and low temperature limits (Fig. 6.39). Degeneracy at low temperatures can be explained as follows. Density of states (DOS) in GaN has a temperature dependence of  $T^{3/2}$ . As inferred from the Fig. 6.38, the carrier concentration for these nanowires has weak temperature dependence. For GaN at 300 K the effective density of states in the conduction band is  $2.23 \times 10^{18} \text{ cm}^{-3}$ . Thus at low temperatures (at 200 K effective conduction band DOS is  $1.2 \times 10^{18}$ ), the carrier concentration in the nanowire can cross the degeneracy level, and hence exhibit  $T^0$  dependence of the measured electron mobility.

## **6.4 Fundamental Transport Properties and Correlation to Structural Characteristics**

In this section, we will discuss the results of mobility extraction from transistor characteristics of nanowires with varying diameters. The electron back scattered diffraction (EBSD) was used to study the effect of grain boundaries on the transport properties of these nanowires. Plot of electron field effect mobility of nanowires with varying diameter is shown in Fig. 6.40. Diameter dependent electron mobility measurements revealed that larger diameter nanowires exhibited significantly higher

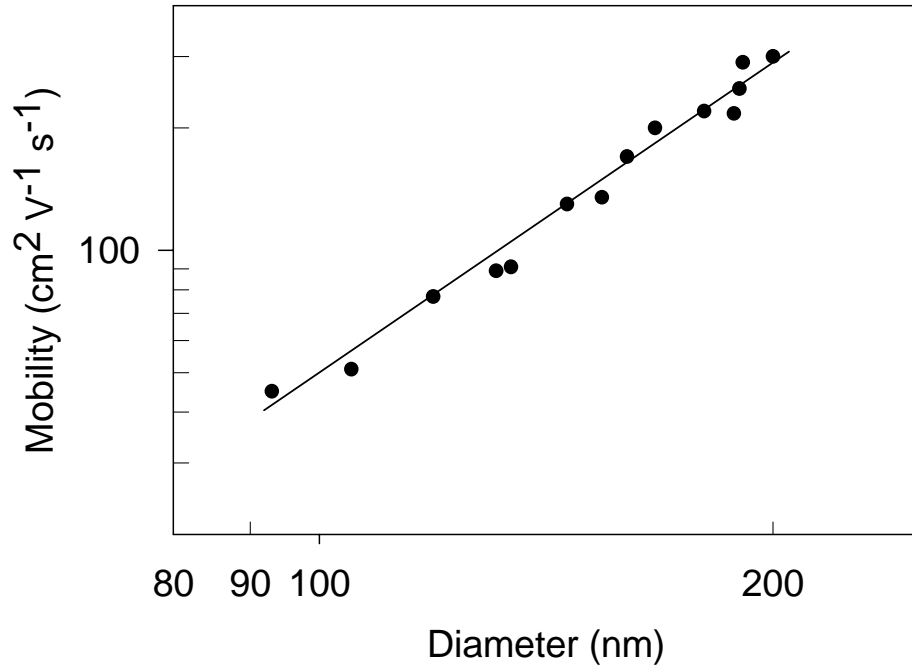
mobility than nanowires with smaller diameters. Lower mobility in smaller diameter nanowires could be explained by enhanced surface scattering.



**Fig. 6.40:** Measured field effect electron mobility of GaN nanowires with varying diameters.

The effect of sidewall scattering in the overall mobility in these nanowires can be modeled using a simple “continuous surface model” [83]. In this model, increased scattering at the surface is accounted for by a surface layer of width  $w$  in which the relaxation time is considerably smaller than in the interior of the wire. Assuming that surface depletion and surface defects give rise to this surface layer, the width of this layer should remain constant for different wires with the same carrier concentration. The ratio of inner volume to the surface layer volume of a nanowire will be greater in larger diameter nanowires than their smaller diameter counterparts. Hence effective

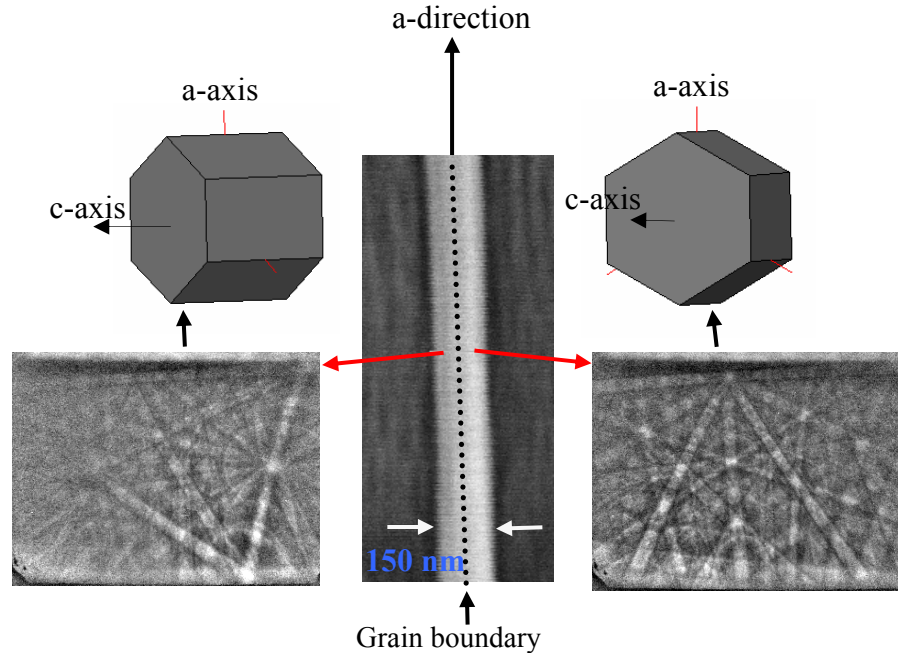
mobilities calculated by averaging the geometric distribution of the relaxation time weighted by the relative carrier concentration will be larger in wider nanowires.



**Fig. 6.41:** Logarithmic plot of measured mobility vs nanowire diameters with slope of 1.3.

The electron mobility of nanowires as a function of diameter is shown in the Fig. 6.41 plotted on logarithmic axes. Use of a  $\mu \propto d^p$  relationship yields a least squares fit with  $p = 1.3$ . An attempt is underway to understand the physical origin of this relationship. In order to be physically realistic, the plot should asymptotically approach the bulk GaN mobility for larger diameters, with a negative curvature. It is a possibility that additional factors are reducing the mobilities of intermediate diameter nanowires ( $120 \text{ nm} \leq d \leq 160 \text{ nm}$ ). In order to investigate such a possibility, after electrical measurements the oxide was completely etched and EBSD was used to study the microstructural properties of all the nanowires devices. It was observed

that some of the low mobility nanowires with diameters above 120 nm were bicrystals with grain boundaries running parallel along the length of the wire.



**Fig. 6.42:** EBSD patterns from two different points on the surface of a 150 nm diameter nanowire. From these patterns, the crystal orientations of the two halves of the bicrystal were determined, as illustrated by the crystal schematics. The a axis of each crystal is parallel to the growth direction but there is a  $42^\circ$  rotation between the c-directions about the common a-axis. The dotted line on the nanowire indicates the grain boundary as inferred from the patterns.

Figure 6.42 shows the Kikuchi diffraction patterns and the crystal orientations from two different points of a 150 nm diameter nanowire FET device (with mobility  $120 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) using EBSD technique. The diffraction patterns did not change when the electron beam was moved along the length of the wire, whereas the diffraction patterns from two different points along the diameter corresponding to the left and right side of the wire clearly indicated the presence of bicrystals with their a-axes parallel to the growth direction (as shown in chapter 2) but with a  $42^\circ$  angle of rotation between the c-directions about the common a-axis. Higher mobility

nanowires studied using EBSD did not reveal the presence of grain boundaries. Grain boundaries were also absent from smaller diameter nanowires.

## **Chapter 7: Gallium Nitride Nanowire-substrate UV Light**

### **Emitting Diodes**

Multifunctional integrated photonic systems for biological/chemical detection, optical communication, and optical storage require nanoscale photonic building blocks such as light emitting diodes (LEDs), lasers, detectors, and waveguides. Electrically excited nanoscale deep ultraviolet (UV) lasers and LEDs operating in the 350 nm to 370 nm range are particularly important for data storage technology and biological applications including UV light induced autofluorescence technique for detecting airborne pathogens. Direct bandgap group III-Nitride (Al/Ga/In-N) semiconducting nanowires with their unique properties [4] (bandgap spanning the whole electromagnetic spectrum, existence of ternary and quaternary alloys, and high thermal stability) are emerging as the most promising candidates for realizing these types of devices.

Nanowire LEDs realized so far can be classified into two broad categories: epitaxial and non-epitaxial. Non-epitaxial techniques involve either a crossed nanowire junction architecture formed by crossing two nanowires of different conductivity types [47], [63], [84],[85] or a nanowire-bulk surface assembled p-n junction, where an n-type nanowire is positioned on a p-type substrate to form the p-n junction.[61], [86] In most of the cases, individual nanowire registration and contact fabrication using electron beam lithography or focused ion beam (FIB) technique is employed. The crossed nanowire junction is simple in terms of assembly and fabrication, yet effective and versatile as demonstrated by the 365 nm electroluminescence (EL) from a n-GaN/p-Si nanowire crossed junction [85] As

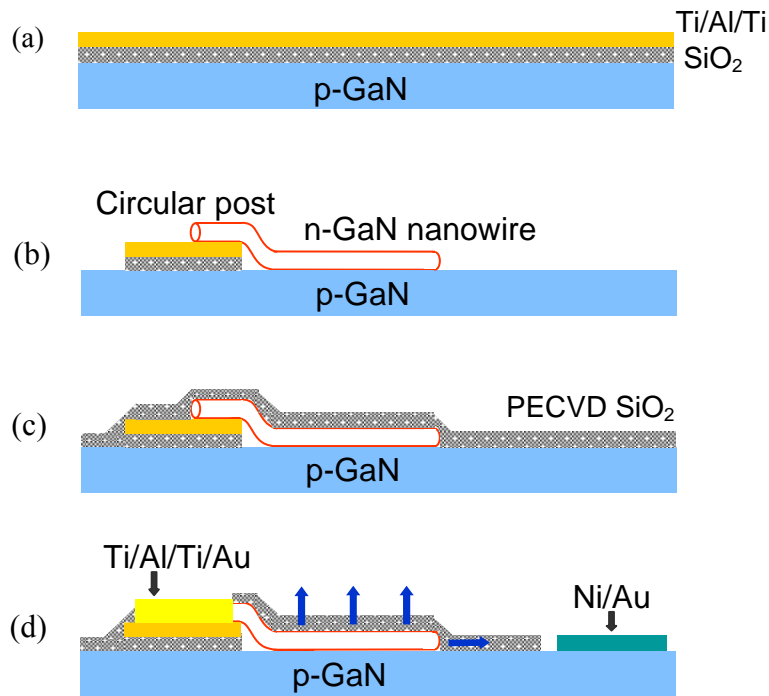


injection and emission occur predominantly at the nanometer scale junction (crossing point of the two nanowires), this architecture suffers from low internal efficiency, which is further lowered by the band offsets in the heterojunction case. Epitaxial techniques involve two very distinct configurations: (a) a core-shell structure where a cylindrical p-n junction is formed by growing a p-type shell on a n-type nanowire or vice versa [14], [15] and (b) a lateral p-n junction on the same nanowire [87], [88] formed by reversing the dopant during the growth. As injection occurs radially along the length of the nanowire, very high external quantum efficiencies have been achieved utilizing the core-shell structure [15]. Although FIB etching was successfully used to remove the outer shell for making contact to the core, reactive ion etching (RIE) is more suitable batch fabrication alternative, but absence of selectivity and isotropy would make the plasma etching of the shell technically challenging.

We have demonstrated electrically excited 365 nm emission from n-GaN nanowires and p-GaN substrate homojunction LEDs, which were assembled utilizing dielectrophoresis and fabricated using batch fabrication processes such as photolithography, wet etching, and metal deposition. Uniqueness of the proposed method is its simplicity, self-alignment (not requiring individual nanowire registration and contact formation), and compatibility with any nanowire and substrate material system, including nitrides requiring high processing temperatures (750 °C).

## 7.1 Fabrication Procedure for n-nanowire p-substrate GaN Homojunction

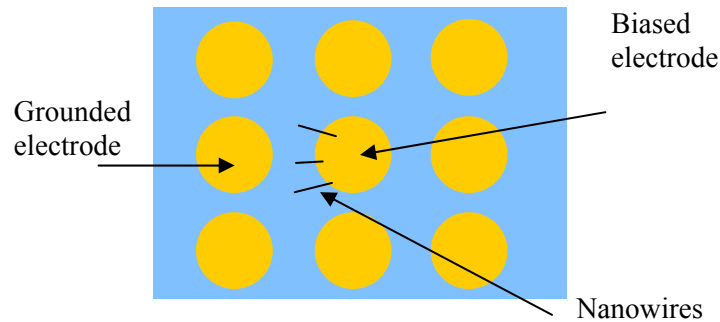
The p-GaN epilayer used for this study was 4  $\mu\text{m}$  thick, grown by hydride vapor phase epitaxy on a c-plane sapphire substrate with Mg as the p-type dopant (hole concentration =  $2.5 \times 10^{18} \text{ cm}^{-3}$ ). A 65 nm thick  $\text{SiO}_2$  layer was deposited using plasma enhanced chemical vapor deposition (PECVD) on the p-GaN epilayer. This was followed by the deposition of Ti/Al/Ti (30 nm/100 nm/30 nm) layer using electron beam evaporation [Fig. 7.1(a)].



**Figure 7.1:** Schematic representation of the process of aligning and fabricating n-GaN nanowire/p-GaN epilayer LED.

Utilizing photolithography and wet etching, 300  $\mu\text{m}$  diameter circular, insulated metal contact pads with 500  $\mu\text{m}$  pitch were obtained on the surface of the p-GaN

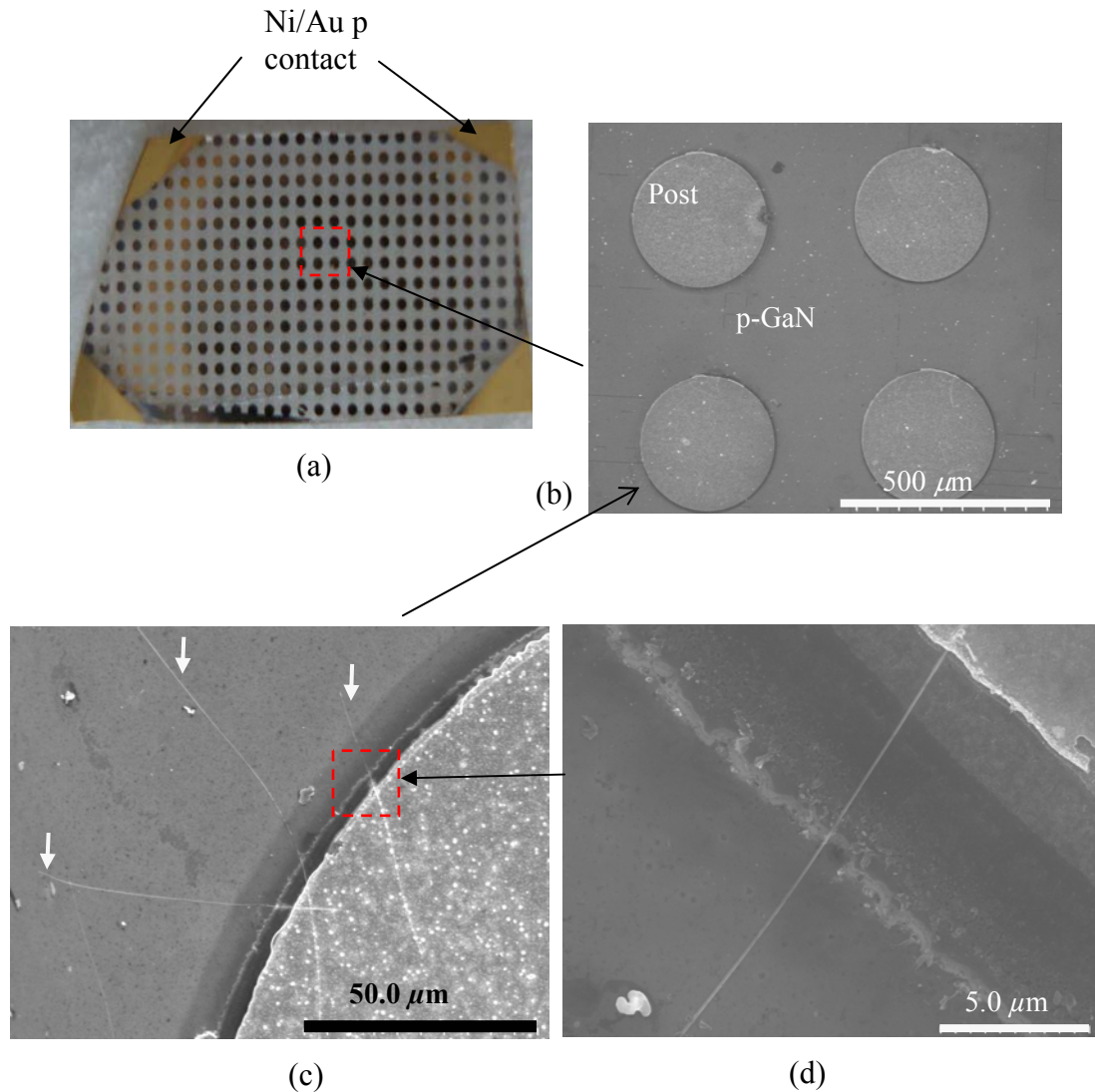
epilayer. A suspension of the GaN nanowires in isopropanol, formed by sonicating the growth matrix, was dispersed onto the substrate with the insulated metal contact pads. In order to align the nanowires dielectrophoretically, a 10 V peak to peak, 1 kHz sinusoidal voltage was applied on one post while grounding the adjacent post. Nanowires aligned themselves in a diverging pattern from the biased post towards the grounded post (Fig. 7.2).



**Figure 7.2:** Schematic representation of the process of aligning n-GaN nanowire on the insulated posts fabricated on p-GaN substrate.

The majority of the aligned nanowires had only 10 % of their total length lying on top of the pads and the rest was in contact with the p-GaN layer forming the p-n junction [Fig. 7.1(b)]. Next, 40 nm of SiO<sub>2</sub> was deposited using PECVD, covering the entire sample [Fig. 7.1(c)]. A second photolithography and etching resulted in 250  $\mu\text{m}$  diameter circular contacts on top of the first level contacts. Ti/Al/Ti/Au (30 nm/100 nm/30 nm/ 30 nm) was deposited followed by a liftoff to form the top contact to the nanowire. Having both top and bottom contacts reduces the contact resistances of these nanowire devices. The smaller diameter of the top contact relative to the bottom one would ensure that even with photolithographic alignment tolerance, the top metal contact would not come in contact with the p-layer, thus eliminating the possibility of

parasitic Schottky contact emission. For contact to the p-GaN layer, Ni/Au (30 nm/30 nm) layer was then deposited [Fig 7.1 (d)] at the four corners of the sample by a shadow mask. Complete fabricated sample is shown in Fig. 7.3 with SEM image of the post and a magnified image where nanowire emerging from the post can be clearly seen. The optical image [Fig. 7.3(a)] of the sample shows the placement of the Ni/Au contacts to the p-GaN.

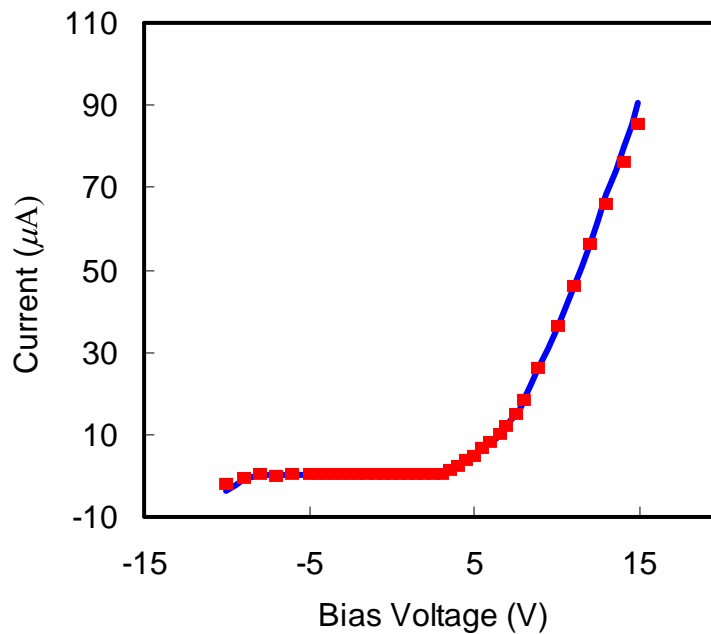


**Figure 7.3:** (a) Optical image of the p-GaN with the posts with nanowire LEDs, (b) SEM image of insulated posts, (c) nanowires (indicated with the white arrows) aligned from a post, (d) SEM image of a nanowire cantilevered from a post touching the p-GaN substrate. Sidewall of the post is visible in the image. The PECVD SiO<sub>2</sub> is removed for the SEM imaging.

## 7.2 Results

### 7.2.1 Electrical Characteristics

Over 40 contact pads, each with nanowire junctions were tested, and as-fabricated devices showed very low current levels with no detectable emission between 10 V and 12 V. This is expected since forming low resistance ohmic contacts to the nitrides require annealing at temperatures as high as 750 °C. These devices showed significant increase in the forward current after annealing in argon for 500 °C for 30 s (Fig. 7.4).



**Figure 7.4:** Current vs voltage characteristics of a single GaN nanowire/substrate junction LED at room temperature. Blue curve represents the characteristics of the device after annealing at 500 °C for 30 s in argon, and red squares represent the characteristics of the same device after a second anneal of 750 °C for 30 s.

Sharp onset of forward conduction started at 3.5 V, which is consistent with the bandgap of GaN. Current through an ideal p-n homojunction diode is given by the celebrated Shockley equation [5]:

$$I = I_s \left( \exp\left(\frac{qV}{k_B T}\right) - 1 \right) \quad (7.1)$$

where  $I_s$  is the reverse saturation current,  $V$  is junction voltage,  $k_B$  is the Boltzmann constant, and  $T$  being the absolute temperature. The  $I_s$  is given by the relationship:

$$I_s = A \times \left( \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \right) \quad (7.2)$$

where

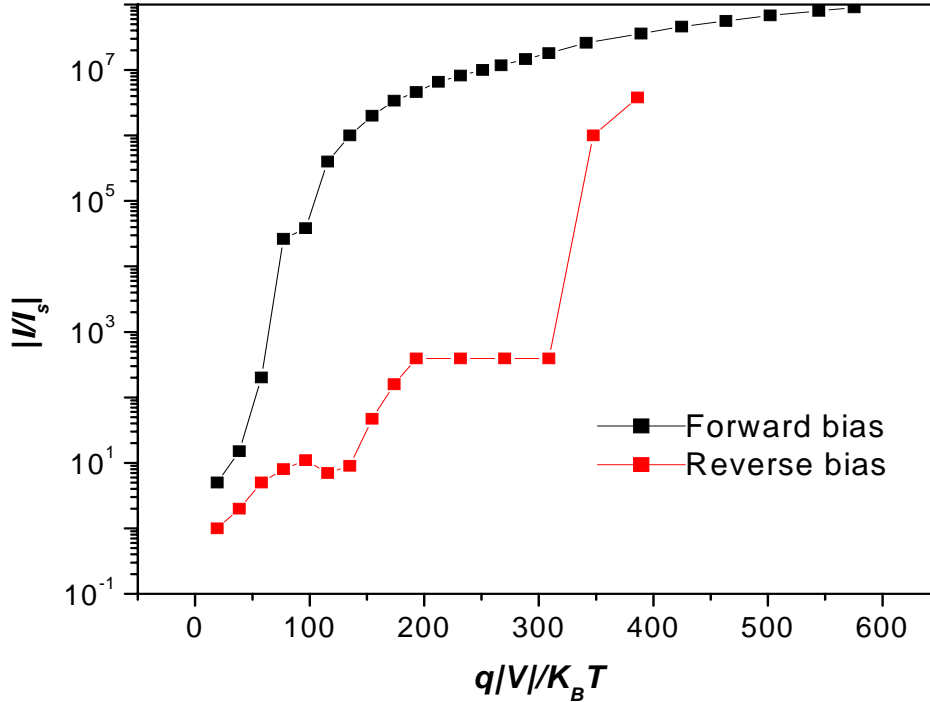
$$L_p = \sqrt{D_p \tau_p}, \quad L_n = \sqrt{D_n \tau_n} \quad (7.3)$$

In the above equation  $A$  is the cross-sectional area of the junction,  $D_n$  and  $D_p$  are the diffusion coefficients for the electrons and holes respectively,  $p_{no}$  and  $n_{po}$  are the thermal equilibrium hole and electron densities on the n and p side respectively. The  $\tau$  represents the minority carrier lifetime. From this ideal equation deviations can result mainly due to: (a) recombination via surface states, (b) presence of generation and recombination in the depletion region, (c) tunneling of carriers between states in the bandgap, (d) high injection condition, and (e) series resistance. In order to take in effect the non-idealities introduced by all of the above mentioned factors the ideal p-n junction current equation is modified with an ideality factor  $\eta$ :

$$I = I_s \left( \exp\left(\frac{qV}{\eta k_B T}\right) - 1 \right) \quad (7.4)$$

This ideality factor indicates the dominant transport mechanism in a p-n junction.

From the equation it is clear that plotting  $I/I_s$  on a logarithmic scale as a function of  $qV/k_B T$  would enable us to calculate the ideality factor of these diodes (Fig. 7.5).

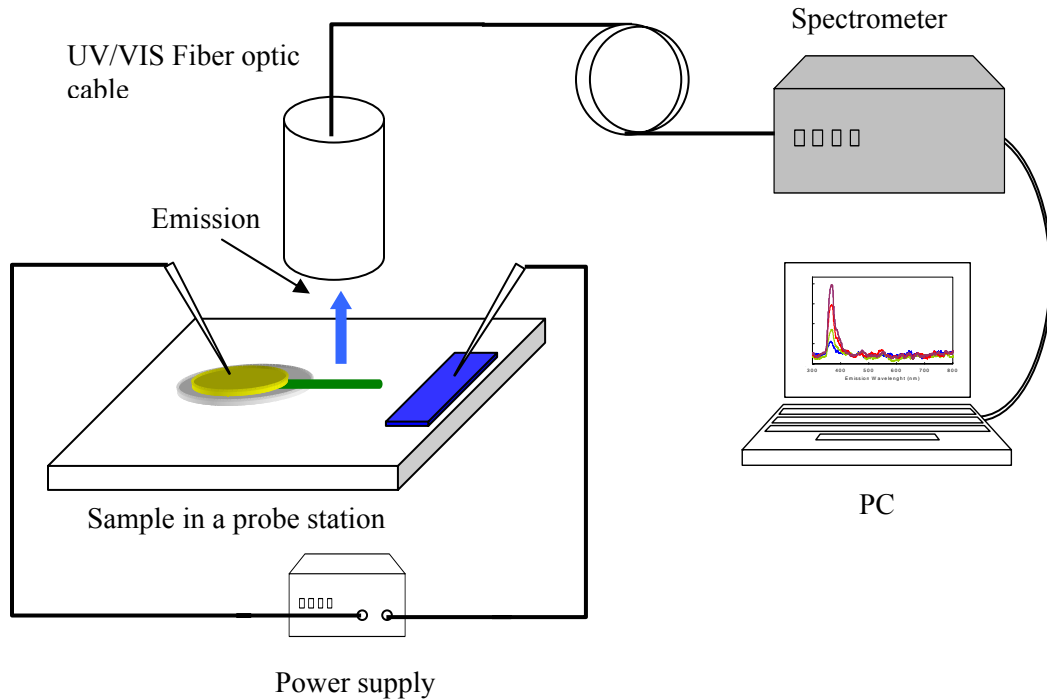


**Figure 7.5:** Semi-log plot of current vs voltage characteristics of a single GaN nanowire/substrate junction LED at room temperature. The p-n junction is annealed at 500 °C.

The ideality factor calculated from the low bias region of the forward curve is about 17 indicating the fact that the diode is highly non-ideal, which is not surprising considering the fact that these p-n junctions are mechanically formed. Presence of high series resistance is evident from the curve, which includes the contributions from both p and n contacts. For GaN, p contact resistances prove to be the determining factor, as the resistances of p-type contacts are often higher than the n-type contacts. Presence of surface states on both nanowire and the p-type epilayer would also contribute to the non-ideal diode characteristics.

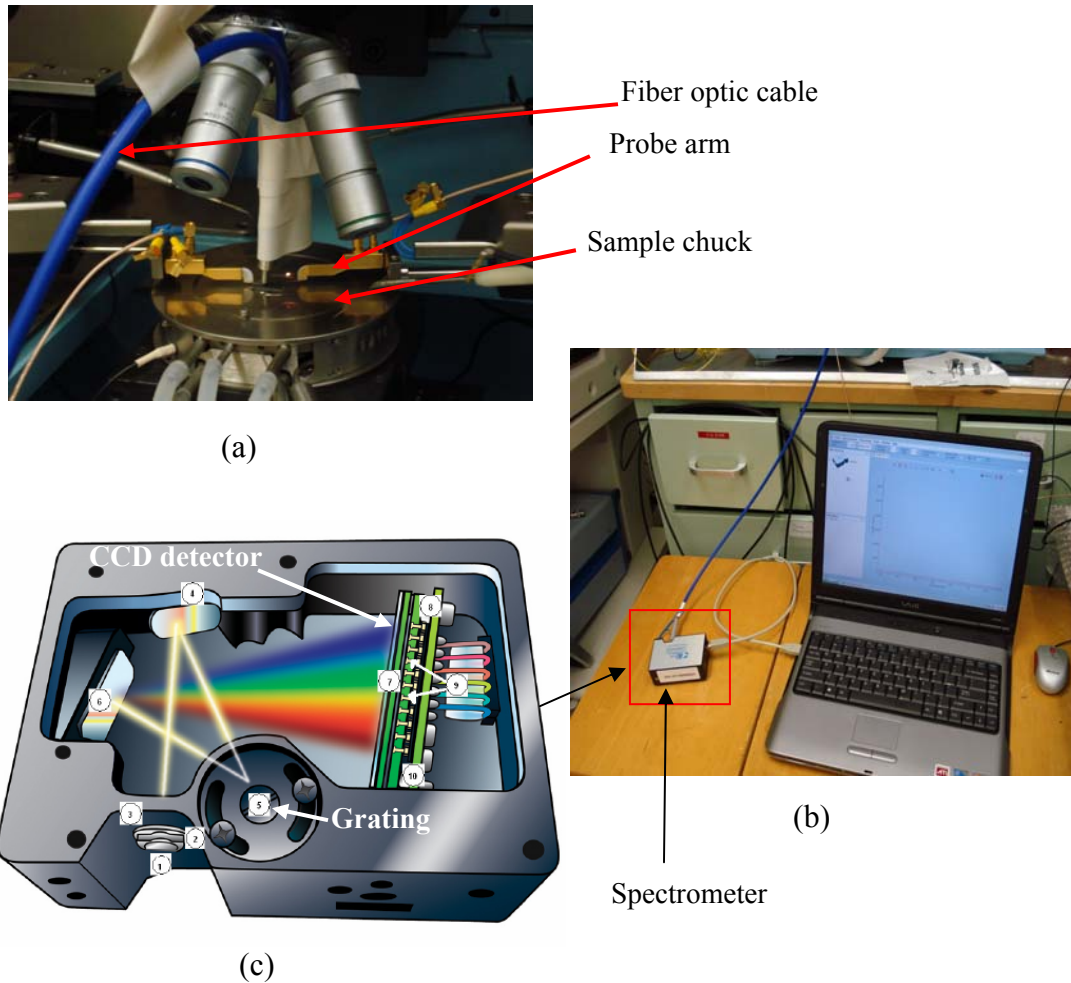
## 7.2.2 Electroluminescence Measurement Setup

Electroluminescence from the nanowire LEDs was measured using a benchtop spectrometer from Ocean Optics<sup>®</sup> interfaced with a PC. This spectrometer has a fixed grating and linear CCD detector array with 2248 elements. The sample is placed on a probe station and biased with DC power supply. A 200  $\mu\text{m}$  diameter UV/VIS solarization resistance optical fiber is placed about 5mm from the sample and light is collected and fed to the spectrometer. Schematic of the measurement setup is shown in Fig. 7.6 and the actual setup is shown in Fig. 7.7.



**Figure 7.6:** Schematic of the electroluminescence measurement setup.





**Figure 7.7:** Electroluminescence measurement setup. (a) Probe station with the sample under bias, fiber optic cable is placed right over the sample, (b) UV/VIS spectrometer connected to the computer for data acquisition, and (c) Schematic of the spectrometer.

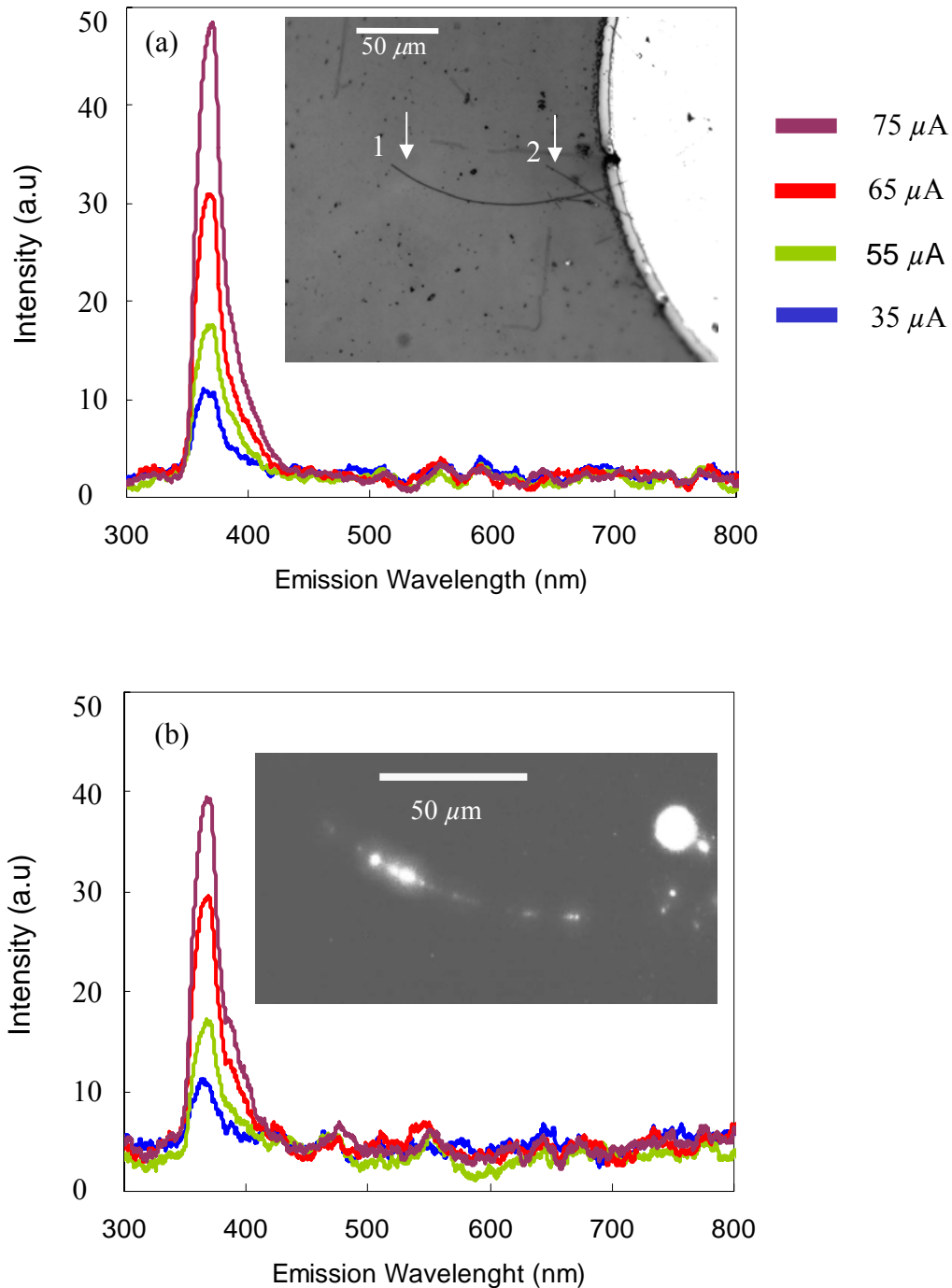
In order to efficiently collect light it is important to align the fiber optic output so that the pattern which is emitting is within the acceptance cone of the fiber. The fiber used had numerical aperture of 0.22 which makes the acceptance angle of  $25^\circ$  in air. The fiber is placed 5 mm above the sample, which makes the acceptance area of about 5 mm on the sample surface. The fiber is aligned above the individual pattern using a

light source on the spectrometer end of the cable. As the intensity of the emission is low, it is necessary to use a large integration time ( $500 \mu\text{s}$ ) and data averaging. Due to the large integration time the noise level of the spectrum is high. In order to increase the signal to noise ratio the background spectrum is subtracted from the raw spectrum for each pattern with nanowire.

### 7.2.3 Electroluminescence Characteristics

As mentioned before as-deposited nanowires do not emit detectable emission. Electroluminescence is only observed from the annealed nanowire junction at 8 V forward bias with  $18 \mu\text{A}$  current. Under forward bias the emission from the nanowire occurs along the length of the wire, consistent with the injection in the nanowire-epilayer junction along length of the nanowire in contact with the p-layer, with occasional brighter regions probably due to local non uniformities in the nanowire (Fig. 7.8 (a) and (b) inset). Bright emission from the tips of some nanowires is observed demonstrating waveguiding capabilities of these nanostructures. Room temperature electroluminescence for different forward bias current levels is shown in Fig. 7.8 (a) from a single n-GaNnw/p-GaN junction device annealed at  $500 \text{ }^\circ\text{C}$ .

In order to establish the absence of parasitic emission from the “posts” (contacts without nanowires), electroluminescence is also measured from the posts with different bias levels. No detectable emission is observed from the posts at bias levels as high as  $75 \mu\text{A}$ . Peak emission occurs at 365 nm with 25 nm fwhm at  $50 \mu\text{A}$ . This is consistent with the bandedge emission from high quality MOCVD grown n-GaN epilayer (3.46 eV) [89], and also with the photoluminescence measurements performed on these nanowires.

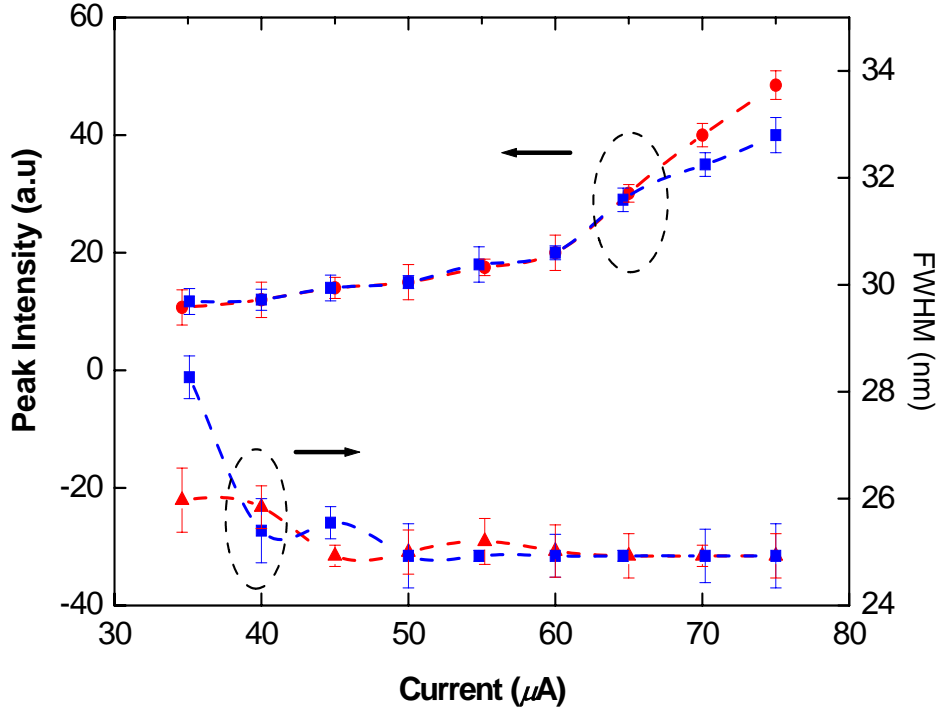


**Figure 7.8:** (a) EL of a single nanowire LED after annealing at 500 °C for 30 s in argon. (inset) Grayscale optical image of a complete nanowire device with the end contact. A shorter nanowire is visible crossing the longer wire (ends of the two wires are numbered and indicated with white arrows). (b) EL of the same device after a second anneal of 750 °C for 30 s, (inset) Optical image of the same device under forward bias with 75  $\mu\text{A}$  injection current. Wire 1 and wire 2 had 200 nm and 160 nm diameters, respectively.

At higher injection levels ( $65 \mu\text{A}$ ), 385 nm emission is also observed in these devices, which could be due to recombination via defects and impurity levels present in the p-GaN. Absence of a 415 nm emission peak (associated with the recombination via Mg related deep levels in p-GaN) indicates that the emission is dominated by recombination in the nanowire [84]. Absence of low energy emissions such as yellow or red bands in the EL, which are often attributed to presence of dislocations in nitrides, indicates that the nanowires are free from major defects and surface related parasitic recombinations.

In order to investigate the reliability of these nanowire LEDs, the operating devices are subject to a second anneal at  $750 \text{ }^\circ\text{C}$  for 30 s. No deterioration was observed in the electrical properties of these devices after the annealing (Fig. 7.4). Emission properties did not show any significant changes [Fig. 7.8(b)]. For higher injection currents it was observed that after the second anneal, the emission at the 385 nm is increased marginally. This indicates that the 385 nm emission might be due to surface related effects originating at the oxide nanowire interface. Peak emission intensity of these nanowire devices is approximately linear with the current, which is crucial for modulation purposes (Fig. 7.9). Light intensity and the fwhm did not deteriorate after annealing the devices at  $750 \text{ }^\circ\text{C}$ , which demonstrates the robustness of the present device structures. The devices showed no signs of degradation even after significant length of operation (more than 2 hours) at room temperature. Excellent thermal stability of the nanowire devices can be attributed to the top and bottom contact pads along with the oxide layer covering the nanowire. The oxide

provided mechanical strength to the device structure and also passivated the nanowire surface, which resulted in reliable operation.

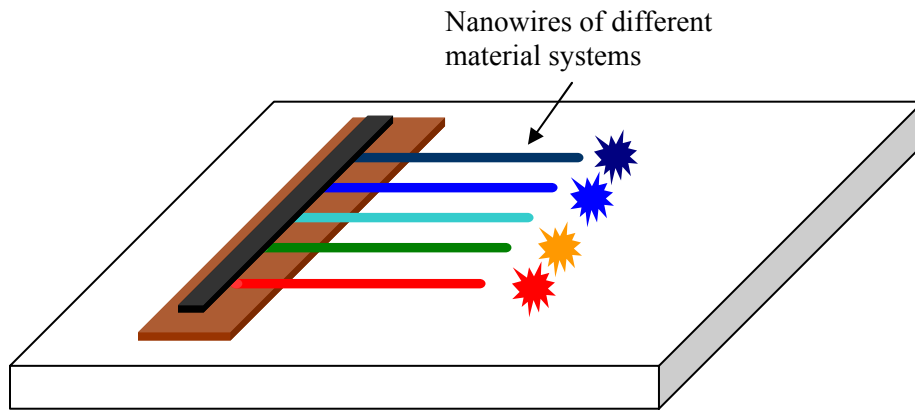


**Figure 7.9:** Peak emission intensity and fwhm of nanowire devices under forward injection condition. The red curve indicates the characteristics of the devices after 500 ° C anneal and the blue curve indicates the trend after a second 750 ° C anneal. The error bars represent the standard deviations of the data over 30 nanowire devices with diameters in the range of 180 nm to 220 nm.

Light extraction from the nanowire LED is also improved using the oxide layer instead of the bare wire as the critical angle  $\theta_c$  for the nanowire-oxide interface is larger than nanowire-air interface ( $\theta_c = \sin^{-1}(n_1/n_2)$ , where  $n_1$  and  $n_2$  represent the dielectric constants of the oxide/air and semiconductor respectively) [5]. Using passivations such as AlN with higher dielectric constant promises to improve the extraction efficiencies.

### 7.3 Discussions and Future Directions

We have demonstrated operation of GaN nanowire/bulk UV light emitting diodes, utilizing dielectrophoretic alignment and simple fabrication techniques. The devices are stable with reliable operation at 365 nm wavelength. The present technique can be applied to other nanowire system, and is suitable for applications requiring large area nanoscale light sources. This technique would also allow us to assemble nanowires of different materials (with different emission wavelengths) on a single substrate (Fig. 7.10) in an array fashion. These types of structures could open up possibilities in chemical/biological detection, environmental sensing and optical systems.



**Figure 7.10:** Schematic representation of multi-spectral nanowire emitter array for biological detection and chemical sensing applications.

Attempts are currently on the way to develop p-n junctions on the same nanowire through Mg diffusion from a solid source. This will give us the ability to form p-n junctions through lithographically defined patterns.

## Chapter 8: Summary and Conclusions

This dissertation focuses on the bottom-up approach to realize various electronic and optical devices from free-standing gallium nitride nanowires. We have developed the basic building blocks, such as field-effect transistors (FETs), Schottky diodes, and light-emitting diodes (LEDs) from these nanowires, which are essential for realizing complex nanosystems.

Detailed structural characterizations performed in these nanowires show that they have wurtzite structure with growth directions along the  $a$  axis. Microstructural chemical analysis did not reveal any other element except Ga and N, indicating the chemical purity of the nanowires. Spectroscopic measurements (photoluminescence and cathodoluminescence) showed band-edge transitions indicating absence of mid-gap states.

Focused ion beam induced metal deposition technique was used to deposit metal contacts to these nanowires, randomly dispersed on a substrate from a suspension. Devices realized using this technique helped us to assess the viability of this nanowire system for device realization, including resistivity and mobility evaluation. Gallium ions interacted with the nanowires, leading to swelling of the nanowires underneath the contact area. For the purpose of minimizing the damage to the nanowires we attempted to use electron beam to dissociate the per-cursor gas for the metal deposition. Surprisingly, electron beam induced deposition also resulted in swelling of the nanowires, which supports the idea that the heat generated during the deposition actually results in the structural damage of the nanowires.

Utilizing dielectrophoresis (translational motion of neutral bodies in presence of a non-uniform electric field), nanowires were assembled on pre-patterned substrates for device fabrication. This technique enables us to simultaneously manipulate large number of nanowires and control their placements without individual nanowire manipulation and registration. This process was studied in detail to reveal the effects of different solvents, frequency of the alignment voltage, and designs of the alignment electrodes on the yield and precision of this technique.

A novel fabrication method, involving only standard microfabrication techniques (photolithography, oxide deposition, metal deposition, and chemical/plasma etching), is developed for realizing reliable GaN nanowire devices. We have designed and realized various novel geometries for nanowire FETs, which demonstrated encouraging performances. Field-effect electron mobility as high as  $312 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  was recorded for these nanowire transistors. We definitely believe that the absence of metal catalyst in the growth method resulted in higher mobility in these nanowires. Utilizing omega-backgate and omega-plane gate geometry we were able to achieve transistor performances (normalized transconductance =  $0.3 \times 10^3 \mu\text{S}/\text{mm}$  and sub-threshold slope =  $0.2 \text{ V}/\text{decade}$ ) comparable to state-of-the-art nanowire and thin film transistors.

We have attempted to understand the basic transport mechanisms in these nanostructures, which will enable us to optimize the growth processes to yield better quality materials. Correlating the material properties to the nanowire device characteristics provided us important insights into the scattering processes in these nanostructures. In order to further improve the device performances, we have to



reduce the background carrier concentration. Due to high un-intentional doping levels in these nanowires the ionized impurity scattering dominated even at room temperatures. Diameter dependent mobility measurements indicated that the surface scattering is dominant scattering mechanism in smaller diameter ( $d < 100$  nm) nanowires.

Mechanically formed GaN nanowire-epilayer homojunction exhibited UV electroluminescence at room temperature. Absence of low energy emission in the electroluminescence is further testament to the superior material quality of these nanowires.

## **8.1 Concluding Remarks and Future Prospects**

This study demonstrates some exciting results that indicate the remarkable prospects of GaN nanowires. The general assembling and fabrication techniques described here can be applied to nanowire of different material systems. Combining microfluidic techniques with dielectrophoresis appears to be very promising for developing complex nanowire architectures. Better designs would improve the performances of these nanowire devices dramatically. Presently we are exploring conformal deposition techniques such as atomic layer deposition for gate stack deposition. Combining conformal oxides with high  $k$  dielectric materials would tremendously boost the performances of these devices. Controlling dopant types and densities are crucial if we want to achieve high-performance nanowire emitters and detectors. Currently we are investigating the possibilities of spatially controlled doping, using both ion-implantation and diffusion. If this is accomplished it would represent a significant milestone in nanowire device research. Also GaN nanowires grown by molecular

beam epitaxy, grown vertically aligned on a substrate, are also being investigated. We plan to significantly extend our research in studying the transport properties of these nanostructures, to reveal the basic conduction mechanisms.

## Appendices

### Appendix A. Standard Cleaning Procedure

Step 1: 3 min heated ultrasonic bath in trichloroethylene

Step 2: 3 min heated ultrasonic bath in acetone

Step 3: 3 min heated ultrasonic bath in methanol

Step 4: 3 min heated ultrasonic bath in isopropanol

Step 5: Rinse in de-ionized (DI) water

Step 6: 1 min dip in heated bath of  $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$  (1:1:5 ratio)

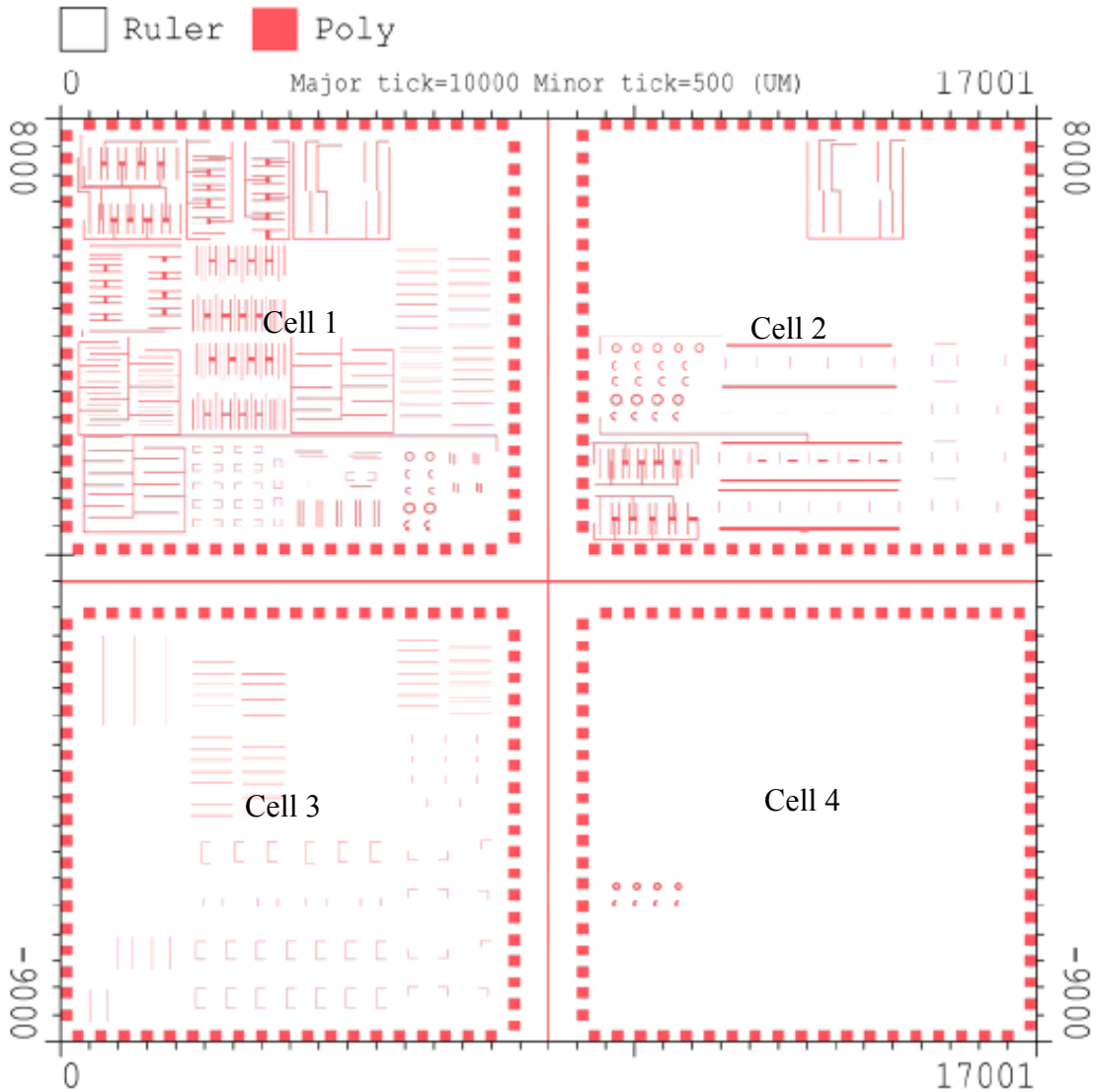
Step 7: Rinse in de-ionized water

Step 8: 1 min dip in heated bath of  $\text{HCl} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$  (1:1:5 ratio)

Step 9: Rinse in de-ionized water, and blow dry with  $\text{N}_2$ .

## Appendix B. Photolithography Mask Layout

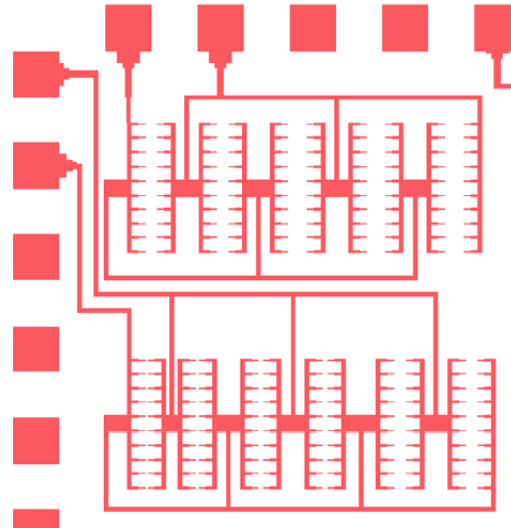
The mask design incorporating the improved geometry is shown here. The entire is design is divided in four cells, with all the levels of the processes described in this design arranged within these four cells. The basic four-cell layout is shown below.



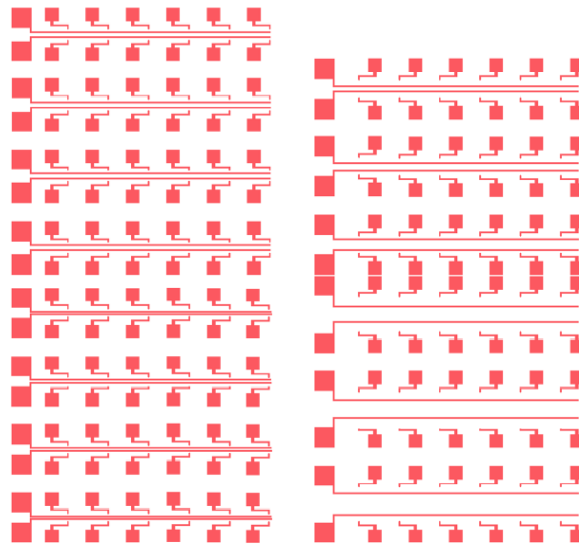
**Figure B.1:** Mask layout showing the four-cell design.

The upper two cells are the source and drain electrodes for various configurations, whereas the bottom left cell is for the gate level and the bottom right contains the mesa patterns. Individual important patterns within cell are shown below:

Cell 1: Source and drain electrodes



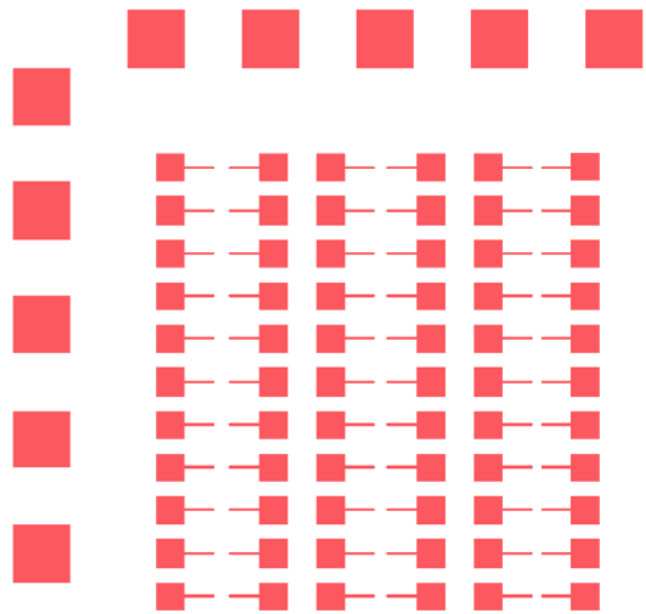
(a)



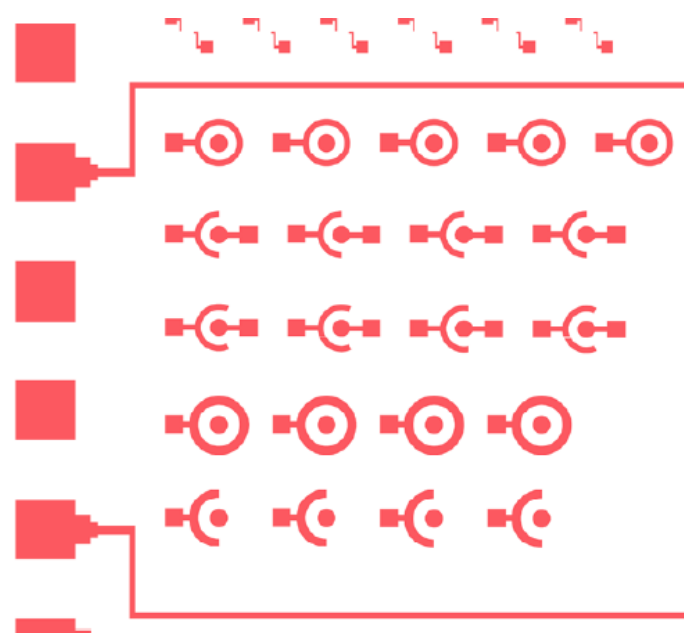
(b)

**Figure B.2:** (a) Array layout, (b) four-terminal layout.

Cell 2: Source and drain electrodes



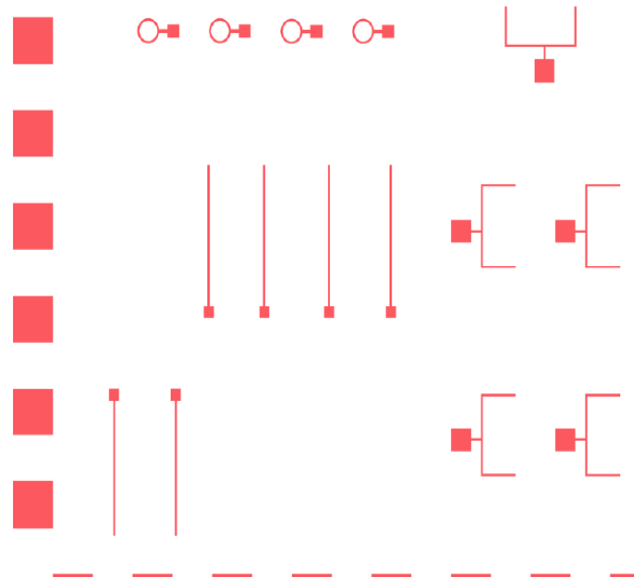
(a)



(b)

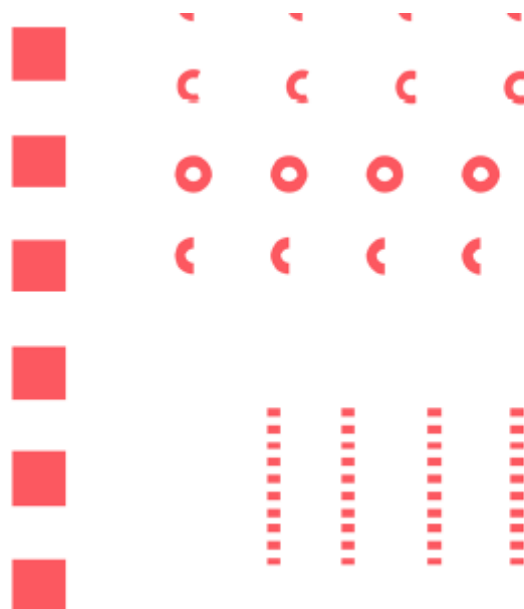
**Figure B.3:** (a) Linear source-drain, (b) circular layout.

Cell 3: Gate



**Figure B.4:** Linear and circular gate designs.

Cell 4: Mesa



**Figure B.5:** Mesa level.

## **Appendix C. Photolithography Process Details**

### **C.1 Dual Resist Lift-off Process**

Process recipe for Shipley<sup>®</sup> 1813 Positive Photoresist with Lift-off Resist

Step 1: Spin coating - Lift-off resist

Spin speed [rpm] 400 for 5 s

Spin speed [rpm] 4000 for 45 s

Step 2: Prebake - 170°C, 5 min, hotplate

Step 3: Spin coating – S1813

Spin speed [rpm] 400 for 5 s

Spin speed [rpm] 4000 for 45 s

Step 4: Prebake - 115°C, 1 min, hotplate

Step 5: Exposure - broadband and monochromatic h- and i-line

Exposure dose ~ 150 mJ/cm<sup>2</sup>

Step 6: Development – MF319 for 1 min

Removal - PG remover

### **C.2 Image Reversal Resist for Mesa Formation**

Process recipe for AZ 5214 Image reversal photoresist

Step 1: Spin coating –Hexamethyldisilazane

Spin speed [rpm] 4000 for 40 s

Step 2: Spin coating – AZ5214

Spin speed [rpm] 400 for 5 s

Spin speed [rpm] 4000 for 45 s



Step 3: Prebake - 95°C, 1 min, hotplate

Step 4: Exposure - broadband and monochromatic h- and i-line

Exposure dose ~ 60 mJ/cm<sup>2</sup>

Step 5: Reversal bake - 120°C, 2 min, hotplate (critical)

Step 6: Flood exposure - broadband and monochromatic h- and i-line

Exposure dose ~ 150 mJ/cm<sup>2</sup>

Step 6: Development – AZ-400K with DI water (1:4) for 90 s

Removal – AZ-400T

## Appendix D. 1-Dimensional Poisson Solver

### D.1 Gauss Jordan Elimination Technique

The Eq. 6.24 represents the system of  $N$  linear equations, which could be expressed as:

$$\begin{aligned}
 b_1 v_1 + c_1 v_2 &= d_1 \\
 a_2 v_1 + b_2 v_2 + c_2 v_3 &= d_2 \\
 a_3 v_2 + b_3 v_3 + c_3 v_4 &= d_3 \\
 &\dots\dots\dots \\
 a_i v_{i-1} + b_i v_i + c_i v_{i+1} &= d_i \\
 &\dots\dots\dots \\
 a_{N-1} v_{N-2} + b_{N-1} v_{N-1} + c_{N-1} v_N &= d_{N-1} \\
 a_N v_{N-2} + b_N v_{N-1} &= d_N
 \end{aligned} \tag{D.1}$$

Comparing Eq. C.1 and Eq. 6.24 we can relate  $d_i$ 's to the  $f_i$ 's,  $v$ 's with  $\Delta\phi_i$ 's, and  $(a, b, c)$ 's with  $(c, b, a)$ 's respectively. The matrix of coefficients  $a, b,$  and  $c$  is called the tridiagonal matrix. The system is readily solved using Gaussian elimination method as described. We first establish a recursion relationship of the form:

$$v_i = \gamma_i - \frac{c_i}{\beta_i} v_{i+1} \tag{D.2}$$

in which the constants  $\beta_i$  and  $\gamma_i$  are to be determined.

Substitution into the  $i$ th equation of Eq. C.1 gives

$$a_i \left( \gamma_{i-1} - \frac{c_{i-1}}{\beta_{i-1}} v_i \right) + b_i v_i + c_i v_{i+1} = d_i. \tag{D.3}$$

That is,

$$v_i = \frac{d_i - a_i \gamma_{i-1} - \frac{c_i v_{i-1}}{b_i - \frac{a_i c_{i-1}}{\beta_{i-1}}}}{b_i - \frac{a_i c_{i-1}}{\beta_{i-1}}}, \quad (\text{D.4})$$

which verifies the above form, subject to the following recursion relations:

$$\beta_i = b_i - \frac{a_i c_{i-1}}{\beta_{i-1}}, \quad \gamma_i = \frac{d_i - a_i \gamma_{i-1}}{\beta_i}. \quad (\text{D.5})$$

Also, from the first equation of Eq. C.1

$$v_1 = \frac{d_1}{b_1} - \frac{c_1}{b_1} v_2 \quad (\text{D.6})$$

where  $\beta_1 = b_1$  and  $\gamma_1 = d_1/\beta_1$ . Finally, substitution of the recursion solution in the last equation of Eq. C.1, yields

$$v_N = \frac{d_N - a_N v_{N-1}}{b_N} = \frac{d_N - a_N \left( \gamma_{N-1} - \frac{c_{N-1}}{\beta_{N-1}} v_N \right)}{b_N} \quad (\text{D.7})$$

where

$$v_N = \frac{d_N - a_N v_{N-1}}{b_N - \frac{a_N c_{N-1}}{\beta_{N-1}}} = \gamma_N. \quad (\text{D.8})$$

To summarize, the complete algorithm for the solution of the tridiagonal system is

$$v_N = \gamma_N, \quad v_i = \gamma_i - \frac{c_i}{\beta_i} v_{i+1}, \quad i = N-1, N-2, \dots, 1, \quad (\text{D.9})$$

where the  $\beta$ 's and  $\gamma$ 's are determined from the recursion formulas:

$$\beta_1 = b_1, \quad \gamma_1 = d_1 / \beta_1,$$

$$\beta_i = b_i - \frac{a_i c_{i-1}}{\beta_{i-1}}, \quad i = 1, 2, \dots, N, \quad (\text{D.10})$$

$$\gamma_i = \frac{d_i - a_i \gamma_{i-1}}{\beta_i}, \quad i = 1, 2, \dots, N, \quad (\text{D.11})$$

## D.2 C++ Implementation of 1-D Poisson Solver

```

1: //1D Poisson Solver for MOS capacitor
2: //Abhishek Motayed
3:
4: #include <math.h>
5: #include <iostream>
6:
7: using namespace std;
8:
9: int main ()
10: {
11: char quit;
12: int GRID_POINTS;
13: double GRID_RES;
14: double k;
15: double X_Well;
16: double t_ox;
17: double NA; //dopat concentration
18: double X_TOTAL;
19: double VG; //gate voltage
20: //Basic constants
21: double q = 1.60218e-19; //elimentary charge
22: double EpSi= 9.7*(8.85418e-14); //dielectric permittivity of GaN
23: double EpOx=3.9*(8.85418e-14); //dielectric permittivity of gate
oxide
24: double no= 1.9e-10; //intrinsic carrier concentration for GaN
at 300 K
25: double VTH=0.0259; //thermal voltage at 300 K
26:
27:
28:
29:
30:
31: quit = '\0';
32: while (quit != 'q')
33: {
34: cout << "This is 1-D Linear Possion Solver for MOS Capacitors In
Equilibrium" << endl;
35: cout << "Specify the dimension of MOS capacitor in centimeters"
<< endl;
36: cout << "Specify the thickness of p-Well" << endl;
37: cin >> X_Well;

```

```

38: cout << "Specify the thickness of Oxide" << endl;
39: cin >> t_ox;
40: cout << "Specify the total number of grid points" << endl;
41: cin >> GRID_POINTS;
42: cout << "Specify doping density of the well" << endl;
43: cin >> NA;
44: cout << "Specify gate voltage" << endl;
45: cin >> VG;
46:
47: //Compute the resolution
48: X_TOTAL= X_Well + t_ox;
49: GRID_RES = X_TOTAL/GRID_POINTS;
50: k = 1/(GRID_RES*GRID_RES);
51:
52: //Initial guess
53: double PHI [GRID_POINTS];
54: double DEL_PHI[GRID_POINTS];
55: double BETA[GRID_POINTS];
56: double GAMMA[GRID_POINTS];
57: double SUB_DIAG[GRID_POINTS];
58: double DIAG[GRID_POINTS];
59: double SUPER_DIAG[GRID_POINTS];
60:
61:
62: //Initialize the arrays with 0
63: for (int i=0;i<GRID_POINTS;i++)
64: {
65: DEL_PHI [i]= 0;
66: }
67:
68: for (int i=0;i<GRID_POINTS;i++)
69: {
70: BETA [i]= 0;
71: }
72:
73: for (int i=0;i<GRID_POINTS;i++)
74: {
75: GAMMA [i]= 0;
76: }
77:
78:
79:
80:
81: //Initialize the PHI array with initial guess
82:
83: for (int i=0;i<=600;i++)
84: {
85: PHI [i]= VG ;
86: }
87:
88: for (int i=601;i<GRID_POINTS;i++)
89: {
90: PHI [i]= VTH*(log(NA/no));
91: }
92:
93:
94: //Compute initial function func array

```

```

95: //where f= PHI'' + q/e *(-no*2*sinh(PHI/VT) + ND-NA))
96: //PHI'' indicates second derivative
97: double func [GRID_POINTS];
98:
99: for (int i=0;i<GRID_POINTS;i++)
100: {
101: func [i]= 0 ;
102: }
103:
104:
105: Loop1:
106: //For frist time we use initial PHI but from second run we use
update
PHI
107:
108:
109: func[0] = 0;
110: PHI[0]= VG ;
111: PHI [GRID_POINTS-1]= VTH*(log(NA/no));
112:
113: for (int i=1;i<600;i++)
114: {
115:
116: func[i] = ((PHI[i+1]-2*PHI[i]+PHI[i-1]))/(GRID_RES*GRID_RES));
117: }
118:
119: func[600] = ((EpSi*PHI[601]- (EpOx+EpSi)*PHI[600]+
EpOx*PHI[599]))/(GRID_RES*GRID_RES); //This if for the oxide
120:
121: for (int i=601;i<(GRID_POINTS-1);i++)
122: {
123:
124:
125: func[i] = ((PHI[i+1]-2*PHI[i]+PHI[i-1]))/(GRID_RES*GRID_RES))+
((q/EpSi)*((-2)*no*sinh(PHI[i]/VTH)+(NA));
126:
127: }
128: func[GRID_POINTS-1] = 0;
129:
130:
131: //Iteratively solving the tridaigonal equation using Gauss
Jordan
elimination
132: //Assign value to sub and super diagonal elements
133: for (int i=0;i<600;i++)
134: {
135:
136: SUB_DIAG[i] = 1/(GRID_RES*GRID_RES);
137: DIAG[i] = -2/(GRID_RES*GRID_RES);
138: SUPER_DIAG[i] = 1/(GRID_RES*GRID_RES);
139:
140: }
141:
142:
143: SUB_DIAG[600] = EpOx/(GRID_RES*GRID_RES);
144: DIAG[600] = -(EpOx+EpSi)/(GRID_RES*GRID_RES);
145: SUPER_DIAG[600] = EpOx/(GRID_RES*GRID_RES);

```

```

146:
147:
148:
149: for (int i=601;i<(GRID_POINTS-1);i++)
150: {
151: SUB_DIAG[i] = 1/(GRID_RES*GRID_RES);
152: DIAG[i] = (-2/(GRID_RES*GRID_RES))-
((q/(Epsi*VTH))*(2*no*cosh(PHI[i]/VTH)));
153: SUPER_DIAG[i] = 1/(GRID_RES*GRID_RES);
154: }
155:
156:
157:
158: BETA[0]= DIAG[0];
159: GAMMA[0]= -func[0]/BETA[0];
160:
161:
162:
163: for (int i=1;i<GRID_POINTS;i++)
164: {
165:
166: BETA[i]=DIAG[i] - ((SUB_DIAG[i]*SUPER_DIAG[i-1])/BETA[i-1]);
167: GAMMA[i]= (-func[i]- (SUB_DIAG[i]*GAMMA[i-1]))/BETA[i];
168:
169: }
170:
171: //Compute DEL PHI
172: DEL_PHI[GRID_POINTS-1]=GAMMA[GRID_POINTS-1];
173:
174:
175: for (int i=(GRID_POINTS-2);i>=0;i--)
176: {
177: DEL_PHI[i]=GAMMA[i]-((SUPER_DIAG[i]*DEL_PHI[i+1])/BETA[i]);
178:
179: }
180:
181:
182:
183:
184:
185: //Check for convergence
186: for (int i=0;i<GRID_POINTS;i++)
187: {
188: if(abs(DEL_PHI[i])>((1e-5)*VTH))
189: {
190: goto Update; //Convergence not achieved
191: }
192:
193: }
194: goto Final;
195:
196: Update:
197: for (int i=0;i<GRID_POINTS;i++)
198: {
199: PHI[i]=PHI[i]+DEL_PHI[i];
200: cout<< i << " " << DEL_PHI[i]<< " " << PHI[i]<< endl;
201: }

```

```
202: goto Loop1;
203:
204:
205: // Convergence achieved
206: Final:
207: for (int i=0;i<GRID_POINTS;i++)
208: {
209: cout << i << " " <<PHI[i] << endl;
210:
211: }
212:
213:
214:
215: cout << "Press q to quit " << endl;
216: cin >> quit;
217: }
218:
219: return 0;
220: }
221:
222:
```



## Bibliography

1. G. Timp, *Nanotechnology*, 1<sup>st</sup> ed., American Institute of Physics Press, New York, Chap. 1, (1999).
2. D. M. Eigler and E. K. Schweizer, "Positioning single atoms with a scanning tunneling microscope," *Nature*, vol. 344, 524 (1990).
3. "International Technology Roadmap for Semiconductors," Executive summary, page 9 (2000).
4. S. Nakamura, S. J. Pearton, and G. Fasol, *The Blue Laser Diode: The Complete Story*, Springer, Berlin (2000).
5. P. Bhattacharya, *Semiconductor Optoelectronic Devices*, 2<sup>nd</sup> ed., Prentice-Hall Inc., New Jersey (1997).
6. B. Bhusan, *Springer Handbook of Nanotechnology*, 1<sup>st</sup> ed., Springer, Berlin (2004).
7. P. G. Collins, K. Bradley, M. Ishigami, and A. Zettl, "Extreme oxygen sensitivity of electronic properties of carbon nanotubes," *Science*, vol. 287, 1801 (2000).
8. Y. Cui and C. M. Lieber, "Functional nanoscale electronic devices assembled using silicon nanowire building blocks," *Science*, vol. 291, 851 (2001).
9. S. J. Tans, M. H. Devoret, H. Dai, A. Thess, R. E. Smalley, L. J. Geerligs, and C. Dekker, "Individual single-wall carbon nanotubes as quantum wires," *Nature (London)*, vol. 386, 474 (1997).
10. S. J. Tans, M. H. Deverot, R. J. A. Groeneveld, and C. Dekker, "Electron-electron correlations in carbon nanotubes," *Nature*, vol. 394, 761 (1998).
11. M. Bockrath, D. H. Cobden, J. Lu, A. G. Rinzler, R. Smalley, L. Balents, and P. I. McEuen, "Luttinger-liquid behaviour in carbon nanotubes," *Nature*, vol. 397, 598 (1999).
12. C. Schönberger, A. Bachtold, C. Strunk, J. -P. Salvetat, L. Forró, "Interference and Interaction in multi-wall carbon nanotubes," *Appl. Phys. A.*, vol. 69, 283 (1995).
13. P. J. F. Harris, *Carbon Nanotubes and Related Structures - New Materials for the Twenty-first Century*, Cambridge University Press, Cambridge (1999).
14. F. Qian, Y. Li, S. Gradečak, D. Wang, C. J. Berrelet, C. M. Lieber, "Gallium Nitride-Based Nanowire Radial Heterostructures for Nanophotonics," *Nano Lett.* vol. 4, 1975 (2004).

15. F. Qian, S. Gradečak, Y. Li, C.-J. Wen, C.-J.; C. M. Lieber, "Core/Multishell Nanowire Heterostructure as Multicolor, High-Efficiency Light-Emitting Diodes," *Nano Lett.*, vol. 5, 2287 (2005).
16. H. Morkoç, *Nitride Semiconductors and Devices*, Springer-Verlag, Berlin, (1999).
17. M. Levinstein, S. Rumyantsev, and M. Shur, *Handbook Series on Semiconductor Parameters*, vol. 1,2 World Scientific, London, (1996, 1999).
18. E. F. Schubert, *Light Emitting Diodes*, Cambridge University Press, Cambridge (2006).
19. W. D. Callister, Jr., *Materials Science and Engineering - An Introduction*, 5<sup>th</sup> ed., John Wiley & Son, Inc., Canada (1999).
20. W. C Johnson, J. B Parsons, and M. C. Crew, "Nitrogen Compounds of Gallium," *J. Phys. Chem.*, vol. 234, 2651 (1932).
21. R. Juza and E. Hahn, *Zeitschrift fur anorganische und allgemeine Chemie*. vol. 239, 282 (1938).
22. H. P. Maruska, J. J. Tietjen, "The preparation and properties of vapor-deposited single crystal GaN," *Appl. Phys. Lett.*, vol. 15. 327 (1969).
23. W. Han, S. Fan, Q. Li, and Y. Hu, "Synthesis of Gallium Nitride nanorods through a Carbon nanotube-confined reaction," *Science*, vol. 277, 1287 (1977).
24. X. Duan and C. M. Lieber, "Laser-Assisted catalytic growth of single crystal GaN nanowires," *J. Am. Chem. Soc.*, vol. 122, 188 (2000).
25. W. Shi, Y. Zheng, N. Wang, C.-S. Lee, and S.-T. Lee, "A general synthetic route to III-IV compound semiconductor nanowires," *Adv. Mater.*, vol. 13, 591 (2001).
26. H. Y. Peng, X. T. Zhou, N. Wang, Y. F. Zheng, L. S. Liao, W. S. Shi, C. S. Lee, and S. T. Lee, "Bulk-quantity GaN nanowires synthesized from hot filament chemical vapor deposition," *Chem. Phys. Lett.*, vol. 327, 263 (2000).
27. M. He, I. Minus, P. Zhou, S. N. Mohammed, J. B. Halpern, R. Jacobs, W. L. Sarney, L. Salamanca-Riba, and R. D. Vispute, "Growth of large-scale GaN nanowires and tubes by direct reaction of Ga with NH<sub>3</sub>," *Appl. Phys. Lett.*, vol. 77, 3731(2000).
28. G. S. Cheng, L. D. Zhang, Y. Zhu, G. T. Fei, L. Li, C. M. Mo, and Y. Q. Mao, "Large-scale synthesis of single crystalline gallium nitride nanowires," *Appl. Phys. Lett.*, vol. 75, 2455 (1999).

29. M. Yoshizawa, A. Kikuchi, M. Mori, N. Fujita, K. Kishino, "Growth of Self-Organized GaN Nanostructures on Al<sub>2</sub>O<sub>3</sub> (0001) by RF-Radical Source Molecular Beam Epitaxy," *Jpn. J. Appl. Phys.*, vol. 36, L459 (1997).
30. R. S. Wagner and W. C. Ellis, "Vapor-Liquid-Solid Mechanism of Single Crystal Growth," *Appl. Phys. Lett.*, vol. 4, 89 (1964).
31. A. M. S. ElAhl, M. He, P. Zhou, G. L. Harris, L. Salamanca-Riba, F. Felt, H. C. Shaw, A. Sharma, M. Jah, D. I. Lakins, T. Steiner, and S. N. Mohammad, "Systematic study of effects of growth conditions on the (nano-, meso-, micro) size and (one-, two-, three-dimensional) shape of GaN single crystals grown by a direct reaction of Ga with ammonia," *J. Appl. Phys.*, vol. 94, 7749 (2003).
32. B. B. He, U. Preckwinkel, and K. L. Smith, "Fundamentals of two-dimensional x-ray diffraction (XRD<sup>2</sup>)," *JCPDS-International Center for Diffraction Data 2000, Advances in X-ray Analysis*, vol. 43.
33. K. W. Andrews, D. J. Dyson, S. R. Keown, *Interpretation of Electron Diffraction Patterns*, Hilger & Watts Ltd., London (1967).
34. D. C. Bell, *Energy Dispersive X-ray Analysis in the Electron Microscope*, BIOS Scientific Publishers Ltd., Oxford (2003).
35. J. B. Schlager, N. A. Sanford, K. A. Bertness, J. M. Baker, A. Roshko, and P. T. Blanchard, "Polarization-resolved photoluminescence study of individual GaN nanowire grown by catalyst-free molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 88, 213106 (2006).
36. P. P. Paskov, T. Paskove, P. O. Holz, and B. Monemar, "Polarized photoluminescence study of free and bound excitations in free-standing GaN," *Phys. Rev. B.*, vol. 70, 035210 (2004).
37. S. O. Kucheyev, M. Toth, M. R. Phillips, J. S. William, and C. Jagdish, "Effects of excitation density on Cathodoluminescence from GaN," *Appl. Phys. Lett.*, vol. 79, 2145 (2001).
38. M. H. Huang, Y. Wu, H. Feick, N. Tran, E. Weber, and P. Yang, "Catalytic Growth of Zinc Oxide Nanowire by Vapor Transport," *Adv. Materials*, vol. 13, 113 (2001).
39. J.-R. Kim, H. M. So, J. W. Park, J.-J. Kim, J. Kim, C. J. Lee, and S. C. Lyu, "Electrical transport properties of individual gallium nitride nanowires synthesized by chemical-vapor-deposition," *Appl. Phys. Lett.*, vol. 80, 3548 (2001).
40. D. R. Bowler, "Atomic-scale nanowires: physical and electronic structures," *J. Phys.: Condens. Matter*, vol. 16, R721 (2004).

41. Y. Huang, X. Duan, Q. Wei, and C. M. Lieber, "Directed Assembly of One-Dimensional Nanostructures into Functional Networks," *Science*, vol. 291, 630 (2001).
42. J. F. Ziegler and J. P. Biersack, Computer codes SRIM 2003, <http://www.srim.org>.
43. K. Suzue, S. N. Mohammad, Z. F. Fan, W. Kim, O. Aktas, A. E. Botchkarev, and H. Morkoç, "Electrical conduction in platinum-gallium nitride Schottky diodes," *J. Appl. Phys.*, vol. 80, 4467 (1996).
44. A. Motayed, R. Bathe, M. C. Wood, O. S. Diouf, R. D. Vispute, and S. N. Mohammad, "Electrical, thermal, and microstructural characteristics of Ti/Al/Ti/Au multilayer Ohmic contacts to n-type GaN," *J. Appl. Phys.*, vol. 93, 1087 (2003).
45. A. Motayed, A. V. Davydov, L. A. Bendersky, M. C. Wood, M. A. Derenge, D. F. Wang, K. A. Jones, and S. Noor Mohammad, "High-transparency Ni/Au bilayer contacts to n-type GaN," *J. Appl. Phys.*, vol. 92, 5218 (2002).
46. J.-S. Jang, S.-J. Park, and T.-Y. Seong, "Metallization scheme for highly low-resistance, transparent, and thermally stable Ohmic contacts to p-GaN," *Appl. Phys. Lett.*, vol. 76, 2898 (2000).
47. Y. Huang, X. Duan, Y. Cui, and C. M. Lieber, "Gallium Nitride Nanowire Nanodevices," *Nano Lett.*, vol. 2, 101 (2002).
48. G. Cheng, A. Kolmakov, Y. Zhang, M. Moskovits, R. Munden, M. A. Reed, G. Wang, D. Moses, and J. Zhang, "Current rectification of single GaN nanowire with well-defined p-n junction," *Appl. Phys. Lett.*, vol. 83, 1578 (2003).
49. J.-R. Kim, B.-K. Kim, I. J. Lee, J.-J. Kim, J. Kim, S. C. Lyu, and C. J. Lee, "Temperature-dependent single-electron tunneling effect in lightly and heavily doped GaN nanowires," *Phys. Rev. B*, vol. 69, 233303 (2004).
50. Focused Ion Beam Workstations User Guide (Technical Publication Dept. FEI Company, Hillsboro, 1994).
51. J. Melngailis, "Focused ion beam deposition: a review," *Proc. SPIE*, vol. 1465, 36 (1991).
52. J.-F. Lin, L. Rotkina, and J. P. Bird, *Proc. 2nd Quantum Transport Nano-Hana Int. Workshop* 5, 17 (2004).
53. J. Goldberg, D. J. Sirbuly, M. Law, and P. Yang, "ZnO Nanowire Transistors," *J. Phys. Chem.*, vol. B 109, 9 (2005).

54. S. E Mohny, Y. Wang, M. A. Cabassi, K. K. Lew, S. Dey, J. M. Redwing, and T. S. Mayer, "Measuring the Specific Contact Resistance of Contacts to Semiconductor Nanowires," *Solid State Electron.*, vol. 49, 227 (2005).
55. M. Khan, T. Detchprohm, P. Hacke, K. Hiramatsu, and N. Sawaki, "The barrier height and interface of Au-n-GaN Schottky diode," *J. Phys. D*, vol. 28, 1169 (1995).
56. A. Motayed, A. Sharma, K. A. Jones, M. A. Derenge, A. A. Iliadis, and S. N. Mohammad, "Electrical characteristics of  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  Schottky diodes prepared by a two-step surface treatment," *J. Appl. Phys.*, vol. 96, 3286 (2004).
57. Y.-J. Ma, Z. Zhang, F. Zhou, L. Lu, A. Jin, and C. Gu, "Hopping conduction in single ZnO nanowires," *Nanotechnology*, vol. 16, 746 (2005).
58. C. Y. Nam, J. Y. Kim, and J. E. Fischer, "Focused-ion-beam platinum nanopatterning for GaN nanowires: Ohmic contacts and patterned growth," *Appl. Phys. Lett.*, vol. 86, 193112 (2005).
59. S. Dhara, A. Datta, C. T. Wu, K. H. Chen, and Y. L. Wang, S. Muto and T. Tanabe, C. H. Shen, C. W. Hsu, and L. C. Chen, and T. Maruyama, "Mechanism of nanoblister formation in  $\text{Ga}^+$  self-ion implanted GaN nanowires" *Appl. Phys. Lett.*, vol. 86, 203119 (2005).
60. N. Asaoka, S. Muto, and T. Tanabe, "Formation of Si clusters in electron-irradiated SiC studied by electron energy-loss spectroscopy," *Diamond and Relat. Mater*, vol. 10, 1251 (2001).
61. X. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, "Single-nanowire electrically driven lasers," *Nature (London)*, vol. 421, 241 (2003).
62. J.-R. Kim, H. M. So, J. W. Park, J.-J. Kim, J. Kim, C. J. Lee, and S. C. Lyu, "Electrical transport properties of individual gallium nitride nanowires synthesized by chemical-vapor-deposition," *Appl. Phys. Lett.* 80, 3548 (2002).
63. X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature (London)*, vol. 409, 66 (2001).
64. D. Wang, S. Jin, Y. Wu, and C. M. Lieber, "Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems," *Nano Lett.*, vol. 3, 1255 (2003).
65. H. Pohl, *Dielectrophoresis: the behaviour of neutral matter in nonuniform electric field*, Cambridge University Press, Cambridge, New York, Chap 2 (1978).
66. M. Dimaki and P. Boggild, "Dielectrophoresis of carbon nanotubes using microelectrodes: a numerical study," *Nanotechnology*, vol. 15, 1095 (2004).

67. N. G. Green and H Morgan, "Separation of submicrometer particles using a combination of dielectrophoretic and electrohydrodynamic forces," *J. Phys. D: Appl. Phys.*, vol. 31, L25 (1998).
68. T. B. Jones, *Electromechanics of Particles*, ed. 1, Cambridge University Press Cambridge, New York (1995).
69. I. Yonenaga, K. Motoki, "Yield strength and dislocation mobility in plastically deformed bulk single-crystal GaN," *J. Appl. Phys.*, vol. 90, 6539 (2001).
70. E. A. Witmer, "Elementary Bernoulli-Euler Beam Theory," MIT Unified Engineering Course Notes: pp. 5-114 to 5-164 (1991).
71. A. Motayed, A.V. Davydov, W. J. Boettinger, D. Josell, A.J. Shapiro, I. Levin, T. Zheleva, and G.L. Harris, "Realization of improved metallization-Ti/Al/Ti/W/Au Ohmic contacts to n-GaN for high-temperature application," *Phys. Stat. Sol. C. 2*, 2536 (2005).
72. S. M. Sze, *Physics of Semiconductor Devices*, 2<sup>nd</sup> ed., Willey-Interscience Publication, New York (1981).
73. S. Ramo, J. R. Whinnery, and Th. van Duzer, *Fields and Waves in Communication Electronics*, 3<sup>rd</sup> ed., Willey, New York, Chap 7 (1993)
74. E. Stern et al., "Electrical characterization of single GaN nanowires," *Nanotechnology*, vol. 16, 2941 (2005).
75. H. -Y. Cha, H. Wu, M. Chandrashekar, Y. C. Choi, S. Chae, G. Koley, M. G. Spencer, "Fabrication and characterization of pre-aligned gallium-nitride nanowire field-effect transistors," *Nanotechnology*, vol. 17, 1264 (2006).
76. M. Shur, *Physics of Semiconductor Devices*, Prentice Hall, New Jersey (1990).
77. N. Goldsman, *Physics and Simulation of Semiconductor Devices*, Lecture Notes, University of Maryland, 2004.
78. R. Chau, "A 50 nm depleted-substrate CMOS transistor (DST)," *Proc. IEDM 2001*, 621.
79. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, "Single- and multi-wall carbon nanotubes field-effect transistors," *Appl. Phys. Lett.*, vol. 73, 2447 (1998).
80. Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High Performance Silicon Nanowire Field Effect Transistors," *Nano Lett.*, vol. 3, 149, 2003.
81. G. L. Pearson, and J. Bardeen, "Electrical Properties of Pure Silicon and Silicon Alloys Containing Boron and Phosphorus," *Phys. Rev.*, vol. 75, 865 (1949).

82. D. C. Look, *Electrical Characterization of GaAs Materials and Devices*, Wiley, New York, Chap. 1, pp-76-80 (1989).
83. V. S. Sundaram and A. Mizel, "Surface effects on nanowire transport: a numerical investigation using the Boltzmann equation," *J. Phys.: Condens. Matter*, vol. 16, 4697 (2004).
84. Z. Zhong, F. Qian, D. Wang, and C.M. Lieber, "Synthesis of p-Type Gallium Nitride Nanowires for Electronics and Photonic Nanodevices," *Nano Lett.*, vol. 3, 343 (2003).
85. Y. Huang, X. Duan, and C.M. Lieber, "Nanowires for Integrated Multicolor Nanophotonics," *Small*, vol. 1, 142 (2005).
86. J. Bao, M. A. Zimmler, F. Capasso, X. Wang, and Z. F. Ren, "Broadband ZnO Single-Nanowire Light-Emitting Diode," *Nano Lett.*, vol. 6, 1719 (2006).
87. H.-M. Kim, T. W. Kang, and K. S. Chung, "Nanoscale Ultraviolet-Light-Emitting Diodes Using Wide-Bandgap Gallium Nitride Nanorods," *Adv. Mater.*, vol. 15, 567 (2003).
88. H. -M. Kim, Y.-H. Cho, H. Lee, S. I. Kim, S. R. Ryu, D. Y. Kim, T. W. Kang, K. S. Chung, "High-Brightness Light Emitting Diodes Using Dislocation-Free Indium Gallium Nitride Multiquantum-Well Nanorod Arrays," *Nano Lett.*, vol. 4, 1059 (2004).
89. M. Smith, Y. J. Lin, H. X. Jiang, M. A. Khan, "Room temperature intrinsic optical transistion in GaN epilayers: The band-to-band versus excitonic transistions," *Appl. Phys. Lett.*, vol. 71, 635 (1997).