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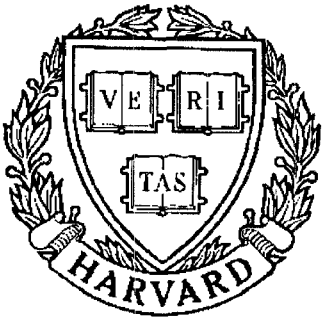


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# Area-Efficient Switched Capacitor Filters: Very Large Time-Constant Circuits

*by J. Lin, T. Edwards, and S. Shamma*

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# Area-Efficient Switched Capacitor Filters: Very Large Time-Constant Circuits

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**Abstract**

The detailed theoretical analysis of very large time-constant (VLT) integrators which use either charge elimination (T-cell and Huang's integrators) or charge cancellation (Nagaraj's and charge-differencing integrators) are described. Using a new area-efficient design, the *charge-differencing* (CD) integrator, the capacitance spread ratio can be easily reduced to less than the reciprocal of the square root of the product of the pole frequency and the sampling period. Non-ideal effects of op-amp like finite DC gain and offset voltage can also be compensated by employing offset storing capacitor operating only with the bi-phase clocking scheme.

# 1 Introduction

Conventional first-order or biquad designs[1, 2] require a minimum capacitance spread ratio of approximately $1/(\Omega_0 T)$, where $\Omega_0$ is the pole frequency and $T$ is the sampling period. For the low frequency application, the ratio becomes very large and impractical to use such circuits. One approach to overcome this problem is to reduce the sampling frequency. However, the choice of the clock frequency is the need to maintain the compatibility with the rest of the SC circuits and this is not always feasible. The other factor to use high clock frequency is to make the area of the anti-aliasing filters and smoothing filters smaller. Therefore, to facilitate the on-chip integration, new circuits designed to reduce the capacitance spread called very large time-constant (VLT) circuits are pursued.

# 2 VLT Integrators

To reduce the capacitance spread, VLT circuits use input signal attenuation, that is, the signal will be attenuated in either in a single phase or in two different phases. Several approaches have been explored for realizing the very large time-constant integrators in an area-efficient way and their principle of

operations will be investigated below.

## 2.1 T-Network VLT integrator

A simple way to attenuate the signal in the SC circuits is to use the capacitor divider. A circuit based on this approach is called the T-network. A lossless inverting integrator is shown in Fig. 1, where the input attenuator comprises the capacitors $C_1$, $C_2$, and $C_B$. A small effective input sampling capacitor

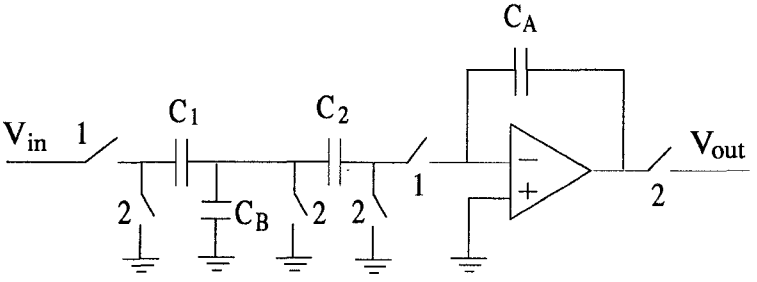


Figure 1: T-network inverting integrator.

is generated, thus a large time-constant can be achieved. In this circuit, the input signal is attenuated twice in only a single phase. It can be easily shown the transfer function is

$$H(z) = -\frac{C_1 C_2}{C_A(C_B + C_1 + C_2)} \frac{z^{-1/2}}{1 - z^{-1}}. \tag{1}$$

The time-constant is determined by the product of two capacitor ratios not just a single ratio and this can reduce the spread ratio approximately down to $1/\sqrt{\Omega_0 T}$ when this integrator is used to design first-order or biquadratic filters. In the same analysis, the lossless non-inverting T-network integrator shown in Fig. 2 has the same transfer function as above except the sign is changed. The advantage of T-network circuits is that it can be combined

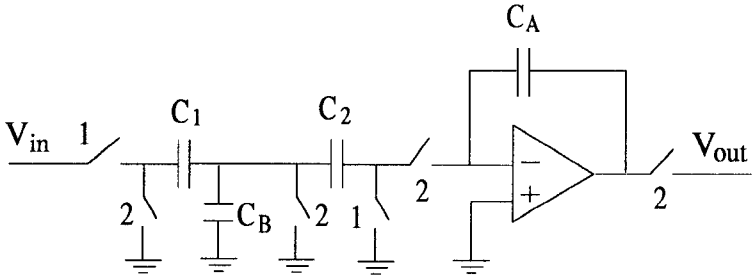


Figure 2: T-network non-inverting integrator.

with the conventional SC circuits easily. However, it suffers from a strong sensitivity to the stray capacitance. From the Fig. 1 or Fig. 2, it is known that any parasitic capacitance from the T-junction to ground will directly add to the values of $C_B$. Furthermore, if there is any wiring parasitic capacitance between the LHS plate of $C_1$ and and the RHS plate of $C_2$, this appears in shunt with the small effective capacitance and significantly deviate the time-constant of the integrator. These parasitics can cause the time constant to

change by as much as 10%[3]. Besides, two large capacitors $C_A$ and $C_B$ are needed in such a circuit, thus, this is not very area-efficient.

## 2.2 Huang's VLT integrator

The outputs of op-amps are only sampled in one of the clock phases and are idle in the other phase in the conventional SC circuit design. Due to this observation, it is instructive to exploit such an idle phase in order to reduce either the influences of op-amp's non-ideal effects (such as offset voltages and finite DC gains) on circuit performance or capacitance spread. A circuit based on this is shown in Fig. 3[4]. During the phase 1, $C_1$ is the input sampling capacitor, while $C_B$ and $C_2$ are the integrating capacitors. The input voltage is attenuated to $-[C_1 V_{in}(z)]/(C_B + C_2)$. During the clock phase 2, only capacitors $C_2$ and $C_A$ form an inverting integrator and the charge stored in $C_2$ is then transferred to $C_A$. These procedures are used to attenuate the input signal in the two different phases, therefore the VLT can be achieved by much smaller capacitance spread ratio. The transfer function is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1 C_2 z^{-1/2}}{C_A(C_B + C_2)(1 - z^{-1})}. \tag{2}$$

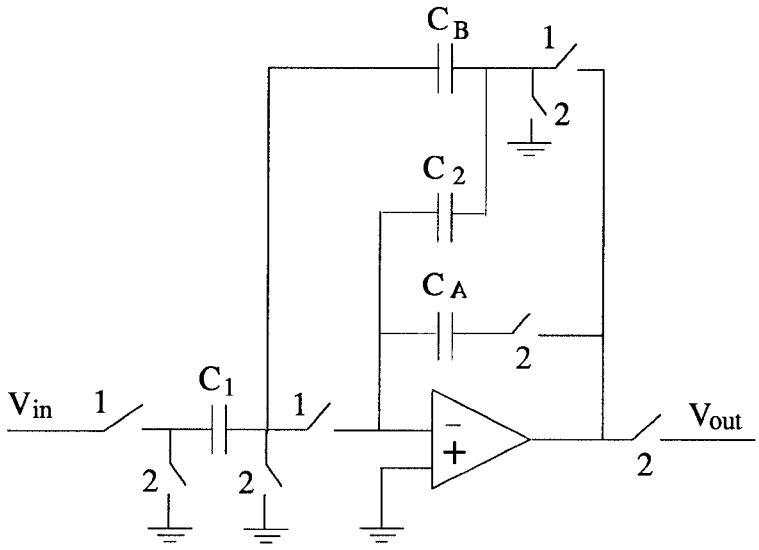


Figure 3: Huang's inverting integrator.

In the same analysis, the non-inverting integrator can be designed as shown in Fig. 4. Due to the inevitable two half delays, it can only realize a forward Euler transformed integrator and the transfer function can also be shown as

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1 C_2 z^{-1}}{C_A(C_B + C_2)(1 - z^{-1})}. \tag{3}$$

This kind of integrators is stray-insensitive and does not suffer the parasitics problem which T-network encountered. However, such integrators still need two large capacitors $C_A$ and $C_B$ and require more switches than T-network integrators. Especially, if a fast op-amp is used, there is a glitch between two clock phases. This is due to that there is no feedback during

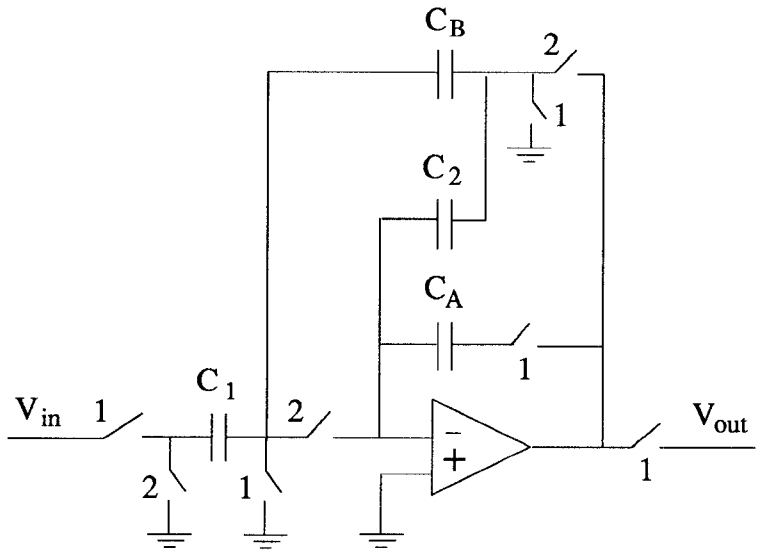


Figure 4: Huang's non-inverting integrator.

the non-overlapping periods and the op-amp is open-circuited. One additional capacitor $C_m$ can be added between the output of op-amp and the RHS plates of $C_B$ and $C_2$ to eliminate such a problem.

Both T-network and Huang's integrators use the charge elimination approach to achieve the large time constant. The operational principle of this approach is to attenuate the signal by several capacitors in one phase. Then, using the charge elimination to discharge the un-wanted charges and transfer the needed charge to the output in the other phase. It is obviously that more switches are usually required and the large capacitors can not be shared by

using such a scheme.

## 2.3 Nagaraj's VLT Integrator

The VLT integrators which are discussed so far need two large capacitors and this is not very area-efficient. A integrator shown in Fig. 5 [3] was proposed by Nagaraj to share the large capacitor, thus only one large capacitor is required. The operational principle of this circuit is as follows. During the

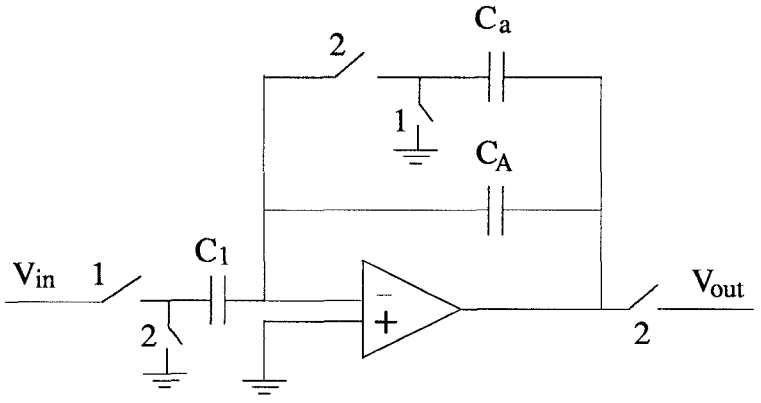


Figure 5: Naragaj's inverting integrator.

phase 1, a charge $C_1 V_{in}$ is transferred from $C_1$ to $C_A$ and the output voltage is sampled by $C_a$ at the same time. In this step, the input voltage is attenuated by the factor of $C_1/C_A$, because $C_A$ is the largest capacitor in the VLT circuit application. During the phase 2, $C_1$ withdraws the charge $C_1 V_{in}$ back from

$C_A$, while $C_a$ redistributes its charge with $C_A$. In the other words, the signal is attenuated again in this step. Functionally, the entire operation can be thought of as attenuating the input voltage by a factor $C_1/C_A$ in the phase 1 and then integrating it onto $C_A$ through the capacitor $C_a$ in the phase 2. Therefore, the input signal is attenuated in two consecutive phases and the large capacitor is also shared in such a design. The capacitor $C_A$ is used as both attenuating capacitor and integrating capacitor, thus, making such a circuit very area-efficient. The transfer function of this integrator can be obtained as

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1 C_a z^{-1/2}}{C_A(C_A + C_a)(1 - z^{-1})}. \tag{4}$$

The non-inverting integrator can also be designed and analyzed in the same way. This integrator is stray-insensitive and does not have the glitch problem during the non-overlapping periods. Besides, it can save about 50% in the total capacitance when compared with the T-network or Huang's integrators.

## 2.4 Charge-Differencing (CD) VLT Integrator

In some applications which have high sampling frequency and very low pole frequencies, Nagaraj's integrator may still require a lot of capacitance area,

because a large capacitor is always needed. To overcome such a problem, a CD integrator was design and shown in Fig. 6 [5]. Its operational principle

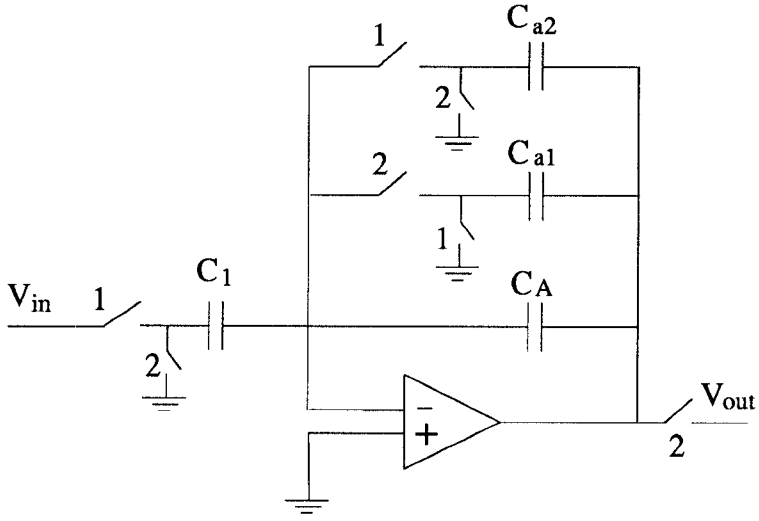


Figure 6: Charge-Differencing integrator.

can be stated as follows. When switches 1 are closed, the charge $V_{in}(n)C_1$ is accumulated in the capacitors $C_A$ and $C_{a2}$. The output voltage is sampled by $C_{a1}$ simultaneously, i.e., the charge $[V_{in}(n)C_{a1}C_1]/(C_A + C_{a2})$ is transferred into $C_{a1}$. When the switches 2 are closed, a charge $V_{in}(n)C_1$ is effectively pulled back to ground from capacitors $C_A$ and $C_{a1}$. Since $C_A$ received the charge $[V_{in}(n)C_AC_1]/(C_A+C_{a2})$ in the previous phase, $C_{a1}$ has to compensate the net difference charge $[V_{in}(n)C_{a2}C_1]/(C_A+C_{a2})$ before it redistributes the

charge received in the previous phase with $C_A$. The transfer function

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1(C_{a1} - C_{a2})z^{-1/2}}{(C_A + C_{a1})(C_A + C_{a2})(1 - z^{-1})} \tag{5}$$

can be obtained.

The charge differencing technique is based on both the difference of capacitors and ratio of capacitors, thus the capacitance spread ratio can be made very small. The inverting and non-inverting integrators can be obtained by choosing the appropriate capacitor values of $C_{a1}$ and $C_{a2}$. This integrator is stray-insensitive, glitch-free, and only one medium capacitor is needed. From the Fig. 5 and Fig. 6, we can observe that Nagaraj's integrator is just a special case of the CD integrator and both use the charge cancellation approach to achieve very large time constant. This is conceptually different from the charge elimination approach used in T-network and Huang's Integrators. In terms of area-efficiency, charge-difference integrator is much preferred. Note that due to using the difference of two capacitors in charge differencing technique, the difference between two capacitors should not be arbitrarily chosen very small. Let us consider the quantity $c = a \pm b$. The sensitivity of $c$ with respect to $a$ is $S_a^c$=(d$c$/$c$)/(d$a$/$a$)=$a/(a \pm b)$. If $a \approx b > 0$, it is obvious that the case of differencing give higher $S_a^c$. Fortunately, the capacitor ratio

can be easily controlled within 0.1% if the layout is carefully done. Then, the variability (or relative change) would not become too large. Taking a reasonable choice of $C_{a1} = 1.5$, and $C_{a2} = 1.0$, the total capacitance is about 30% less than using Nagaraj's integrators but the sensitivity only increases by a few times.

# 3 GOC CD VLT Integrators

It is known that the performance of switched capacitor circuits will be degraded due to the non-ideal effects of op-amps such as offset voltages and finite DC gains. Since these non-ideal effects can usually be improved simultaneously, the circuits with gain- and offset-compensation are called GOC circuits. The discussion here will concentrate on the GOC VLT circuits using the CD integrator, since this is the most area-efficient design.

Due to the charge cancellation approach which the CD integrator uses, we have to maintain the connection between the right-hand-side (RHS) plate of $C_1$ and the left-hand-side (LHS) plate of $C_A$ in both phases. Thus, the charge can be pumped into the charge integrator in one phase and be pulled back in the other phase. From this observation, GOC CD inverting integrator was

designed and shown in the Fig. 7[5]. Note that capacitor $C_{a1}$ is chosen bigger

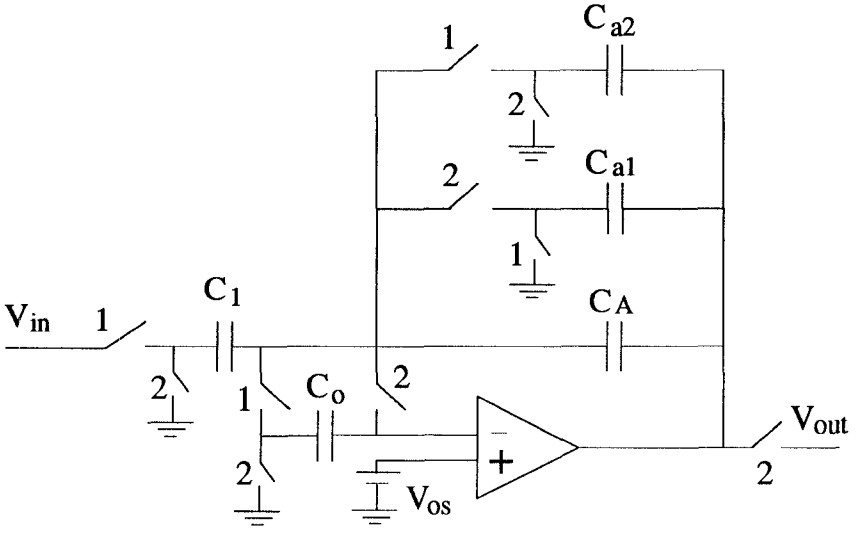


Figure 7: GOC Charge-Differencing inverting integrator.

than $C_{a2}$ in the inverting integrator.

When the phase 2 is on, the LHS plate of capacitor $C_o$ is connected to ground. Therefore, this capacitor stores the offset voltage $-V_{os}$. During the phase 1, the LHS plate of $C_o$ is connected to the RHS plate of $C_1$ and the LHS plates of $C_A$ and $C_{a2}$. Since the RHS plate of $C_o$ is only connected to the negative terminal of op-amp, the charge held in this plate is preserved. Consequently, the LHS plate of $C_o$ acts like the virtual ground. Note that the arrangement of clock phases surrounding the capacitor $C_o$ is very important

and the choices will depend on the clock phases associated with the integrating capacitors $C_{a1}$ and $C_{a2}$. In the above case, the virtual ground exists in the phase 1. If the switch phases surrounding the capacitor $C_o$ are changed, the virtual ground will appear in the phase 2 and this will affect the effects of GOC dramatically in some cases. The details will be elaborated below.

Suppose the $V_{in}$=0, gain=$\infty$ and the offset voltage is $V_{os}$. When the phase 1 is on, the LHS plate of $C_o$ is connected to the junction of $C_1$, $C_{a2}$, and $C_A$. The voltage in this junction is equal to zero. However, the voltage of this junction is changed to $V_{os}$ when the phase 2 is on. Conceptually, this is like the input voltage $V_{os}$ exists. As the same analysis as the CD integrator does, $[C_1(C_{a2} - C_{a1})V_{os}]/[(C_A + C_{a1})(C_A + C_{a2})]$ can be expected in the output voltage. Besides, $C_{a2}$ sampled the output voltage in the phase 2 and redistributed the charge with $C_A$ in the phase 1. This charge will be held in the $C_A$, thus, $(C_{a2}V_{os})/(C_A + C_{a2})$ is also expected in the output voltage. Using the time domain analysis,

$$\begin{aligned} V_{out}(n+\frac{1}{2}) &= \frac{C_1(C_{a2}-C_{a1})}{(C_A+C_{a1})(C_A+C_{a2})}V_{in}(n) + V_{out}(n-\frac{1}{2}) \\ &+ (\frac{C_{a2}}{C_A+C_{a2}} + \frac{C_1(C_{a2}-C_{a1})}{(C_A+C_{a1})(C_A+C_{a2})})V_{os} \end{aligned} \quad (6)$$

can be obtained. This satisfies the previous conjecture. Comparing with the

equation of the non-GOC CD integrator which has the effective offset voltage

$$(\frac{C_{a1}}{C_A + C_{a1}} + \frac{C_{a2}}{C_A + C_{a2}})V_{os} \tag{7}$$

a factor of more than 2 can always be achieved. In the especial case of $C_{a2} = 0$, the output voltage of the GOC CD integrator due to the $V_{os}$ is approximately inversely proportional to ${C_A}^2$. Thus, the offset voltage is even much reduced. In the typical VLT application, a factor of more than 10 can be obtained easily.

As claimed before, the switch phases associated with the offset storage capacitor $C_o$ is very important. If these switch phases are changed, the effective offset voltage becomes

$$(\frac{C_{a1}}{C_A + C_{a1}} + \frac{C_1(C_{a1} - C_{a2})}{(C_A + C_{a1})(C_A + C_{a2})})V_{os}. \tag{8}$$

When $C_{a2} = 0$, the offset voltage term of output equation, in fact, becomes slightly worse instead of getting improved when compared with the non-GOC CD integrator.

From above discussion, we know that when to choose the virtual ground is critical. Note that in the charge-differencing circuits shown in Fig. 6, we do the sampling in both phases, therefore, the gain and offset-compensation

is not so effective as the special case when $C_{a2} = 0$. Fortunately, the effective DC gain of op-amp is high when used in the low frequency application (assume the output signal does not change abruptly). If such performance can not be satisfied, the other GOC circuits have to be pursued.

In the same way, the GOC CD non-inverting integrator is shown in Fig. 8, where, $C_{a2}$ is larger than $C_{a1}$. The time domain analysis gives

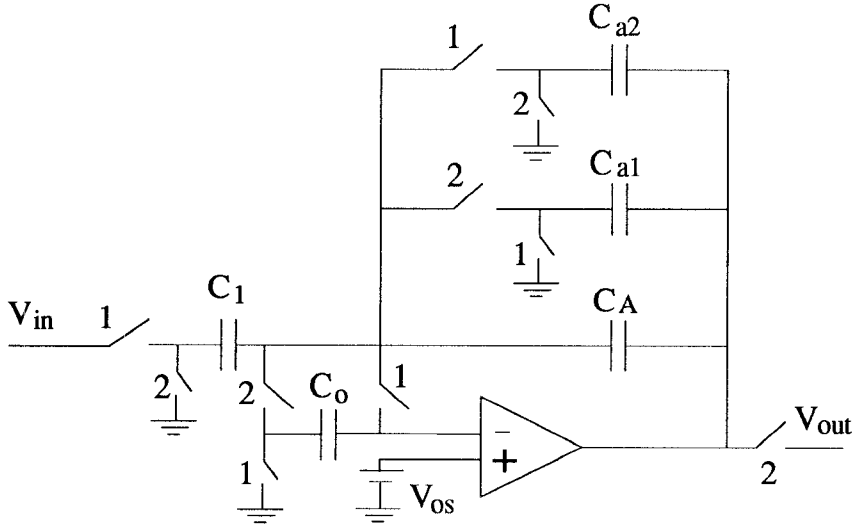


Figure 8: GOC Charge-Differencing non-inverting integrator.

$$V_{out}(n+\frac{1}{2}) = \frac{C_1(C_{a2}-C_{a1})}{(C_A+C_{a1})(C_A+C_{a2})}V_{in}(n) + V_{out}(n-\frac{1}{2}) + (\frac{C_{a1}}{C_A+C_{a1}} + \frac{C_1(C_{a1}-C_{a2})}{(C_A+C_{a1})(C_A+C_{a2})})V_{os}. \quad (9)$$

It is noted that the switch phases associated with $C_o$ are different from those

of Fig. 7.

# 4 First Order Section Design

After the GOC CD integrators have been designed, first order filter can be built based on these circuits. The negative first order filter is shown in Fig. 9, where the capacitor $C_{a1}$ is chosen to be larger than the capacitor $C_{a2}$. From

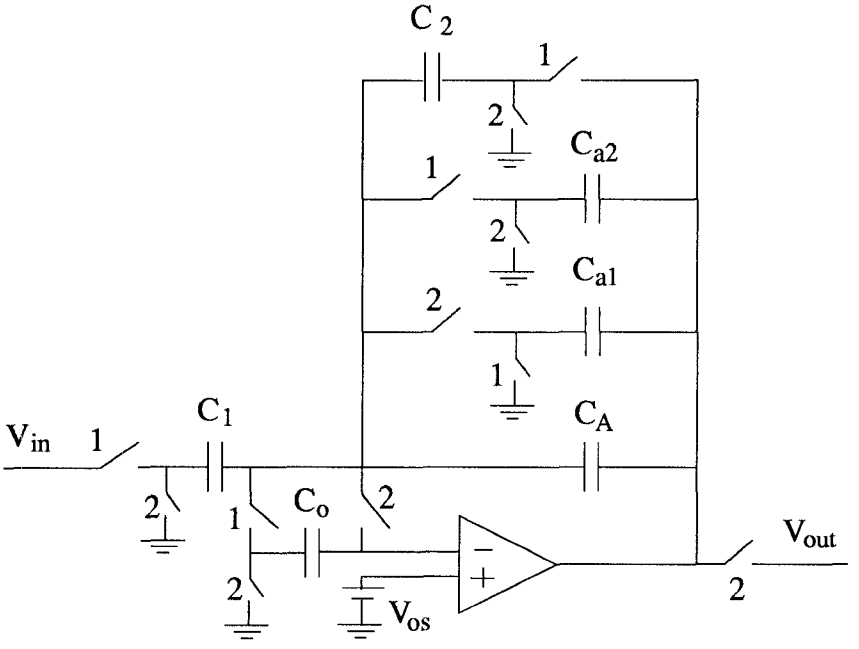


Figure 9: GOC CD inverting first-order filter.

the time domain analysis, the following equation can be obtained

$$\begin{aligned} V_{out}(n+\frac{1}{2}) &= \frac{C_1(C_{a2}-C_{a1})}{(C_A+C_{a1})(C_A+C_{a2}+C_2)}V_{in}(n) \\ &+ \frac{(C_A+C_{a1}+C_2)(C_A+C_{a2})}{(C_A+C_{a1})(C_A+C_{a2}+C_2)}V_{out}(n-\frac{1}{2}) \\ &+ \frac{C_{a2}(C_A+C_1+C_2)-C_{a1}(C_1-C_{a2})}{(C_A+C_{a1})(C_A+C_{a2}+C_2)}V_{os}. \end{aligned} \tag{10}$$

Due to the choices of $C_{a1}$ and $C_{a2}$,

$$\frac{(C_A+C_{a1}+C_2)(C_A+C_{a2})}{(C_A+C_{a1})(C_A+C_{a2}+C_2)} < 1. \tag{11}$$

The location of pole is inside the unit circle, therefore the stability can be always assured. Consider the transfer function in the s-domain,

$$H(s) = -k\frac{1+s/\Omega_1}{1+s/\Omega_0}. \tag{12}$$

Setting $x_0 = 2/(\Omega_0 T)$, $x_1 = 2/(\Omega_1 T)$, and perform the bilinear transformation, the transfer function in the z-domain is

$$H(z) = -k\frac{(1+x_1)-(1-x_1)z^{-1}}{(1+x_0)+(x_0-1)}. \tag{13}$$

Comparing the coefficients,

$$\frac{2}{1+x_0} = \frac{C_2(C_{a1}-C_{a2})}{(C_A+C_{a1})(C_A+C_{a2}+C_2)}. \tag{14}$$

For the lowpass filter, assume $\Omega_0 T \ll 1$, $\Omega_1 = -2f_s$ ($f_s$ is the sampling frequency), unit gain ($k = 1$), and $C_{a1} - C_{a2} = \delta$, the capacitor values can

be chosen as

$$C_1 = C_2 = 1 \tag{15}$$

$$C_A = C_B = K \approx \frac{\delta}{\sqrt{\Omega_0 T}}. \tag{16}$$

That is, the capacitance spread ratio is just about $\delta/\sqrt{\Omega_0 T}$.

In the same way, the non-negative first order section can be designed and shown in Fig. 10. Note that the phases associated with $C_o$ has been changed

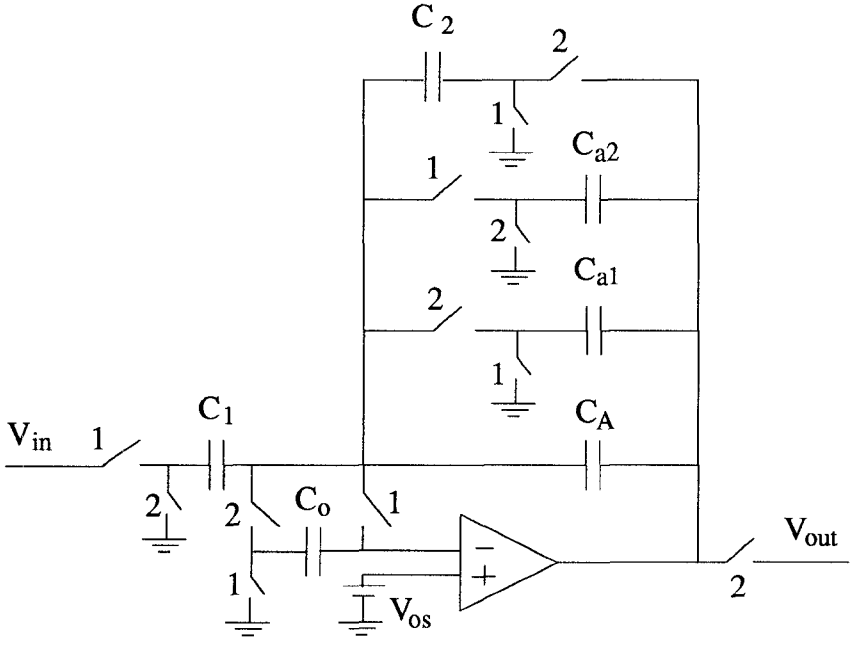


Figure 10: GOC CD non-inverting first-order filter.

and the capacitor $C_{a2}$ is larger than the capacitor $C_{a1}$ to assure the system

stability. The time domain analysis gives

$$\begin{aligned} V_{out}(n+1/2) &= \frac{C_1(C_{a2}-C_{a1})}{(C_A+C_{a2})(C_A+C_{a1}+C_2)}V_{in}(n) \\ &+ \frac{(C_A+C_{a1})(C_A+C_{a2}+C_2)}{(C_A+C_{a1}+C_2)(C_A+C_{a2})}V_{out}(n-1/2) \\ &+ \frac{C_{a1}(C_A+C_1+C_2)-C_{a2}(C_1+C_2-C_{a1})}{(C_A+C_{a1}+C_2)(C_A+C_{a2})}V_{os}. \end{aligned} \quad (17)$$

# 5 Biquadratic Section Design

With the above GOC charge-differencing Integrator, two type of biquads (referred to as the E and F circuits in [1], and Type-I and Type-II biquads here) can also be built[5] and shown in Fig. 11 and Fig. 12 respectively. Type-I biquad gives simpler design equations, while those of Type-II biquad are slightly more complicated. Using the signal flow graphs (assume $V_{os} = 0$) shown in Fig. 13 and Fig. 14 respectively, the transfer functions can be obtained[6]

$$\begin{aligned} H(z) &= \frac{V_{out}(z)}{V_{in}(z)} \\ &= -\frac{A-(A+B-C)z^{-1}+(B-D)z^{-2}}{E-(E+F-G)z^{-1}+(F-H)z^{-2}}. \end{aligned} \quad (18)$$

Where,

$$A = \frac{C_6}{C_1}\left(\frac{C_B+C_{b1}}{C_{b1}-C_{b2}}\right) \quad (19)$$

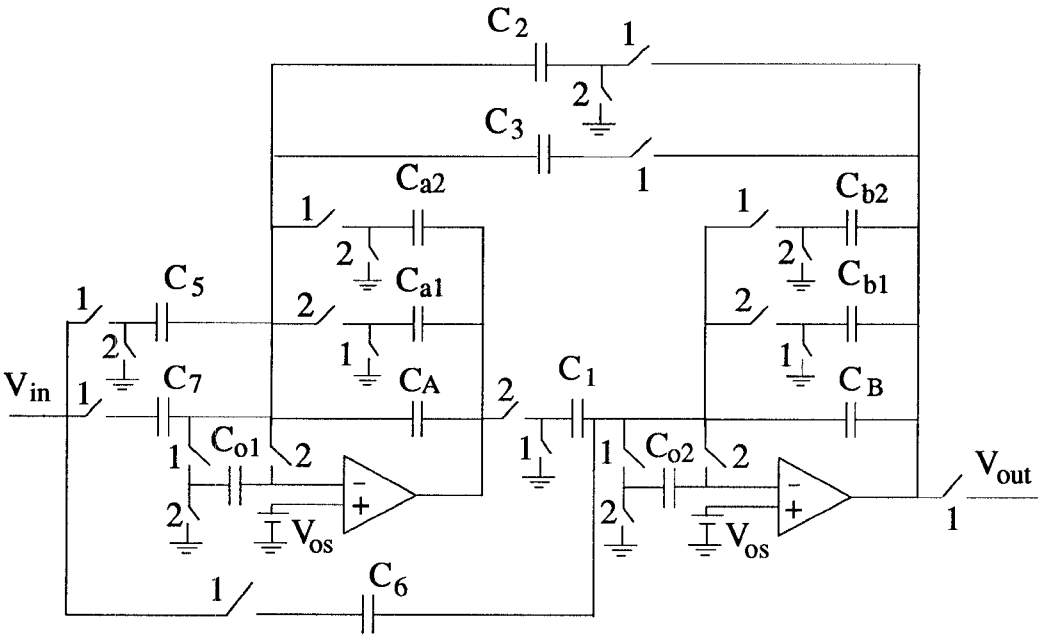


Figure 11: GOC CD Type-I second-order filter.

$$B = \frac{C_6}{C_1}\left(\frac{C_B + C_{b1}}{C_{b1} - C_{b2}}\right) + \frac{C_5}{C_A + C_{a1}} \tag{20}$$

$$C = \frac{C_5 + C_7}{C_A + C_{a2}} \tag{21}$$

$$D = \frac{C_5}{C_A + C_{a1}} + \frac{C_7}{C_A + C_{a2}}. \tag{22}$$

For the Type-I biquad,

$$E = \frac{(C_B + C_{b1})(C_B + C_{b2})}{C_1(C_{b1} - C_{b2})} \tag{23}$$

$$F = \frac{C_2}{C_A + C_{a1}} + \frac{(C_B + C_{b1})(C_B + C_{b2})}{C_1(C_{b1} - C_{b2})} \tag{24}$$

$$G = \frac{C_2 + C_3}{C_A + C_{a2}} \tag{25}$$

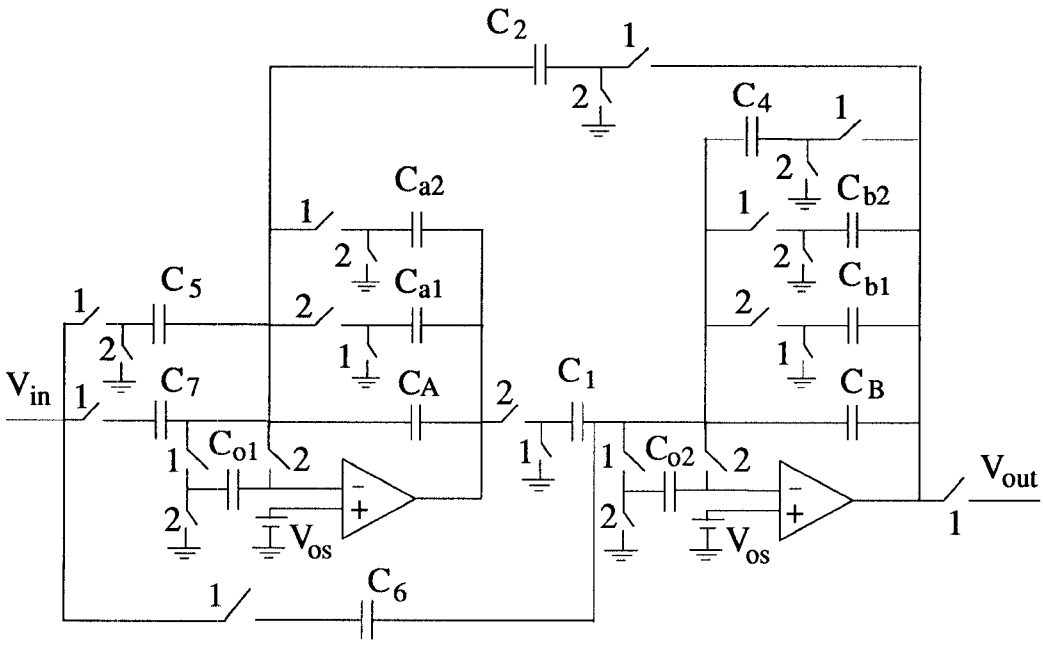


Figure 12: GOC CD Type-II second-order filter.

$$H = \frac{C_2}{C_A + C_{a1}} + \frac{C_3}{C_A + C_{a2}}. \tag{26}$$

For the Type-II biquad,

$$E = \frac{(C_B + C_{b1})(C_B + C_{b2} + C_4)}{C_1(C_{b1} - C_{b2})} \tag{27}$$

$$F = \frac{C_2}{C_A + C_{a1}} + \frac{(C_B + C_{b1} + C_4)(C_B + C_{b2})}{C_1(C_{b1} - C_{b2})} \tag{28}$$

$$G = \frac{C_2}{C_A + C_{a2}} \tag{29}$$

$$H = \frac{C_2}{C_A + C_{a1}}. \tag{30}$$

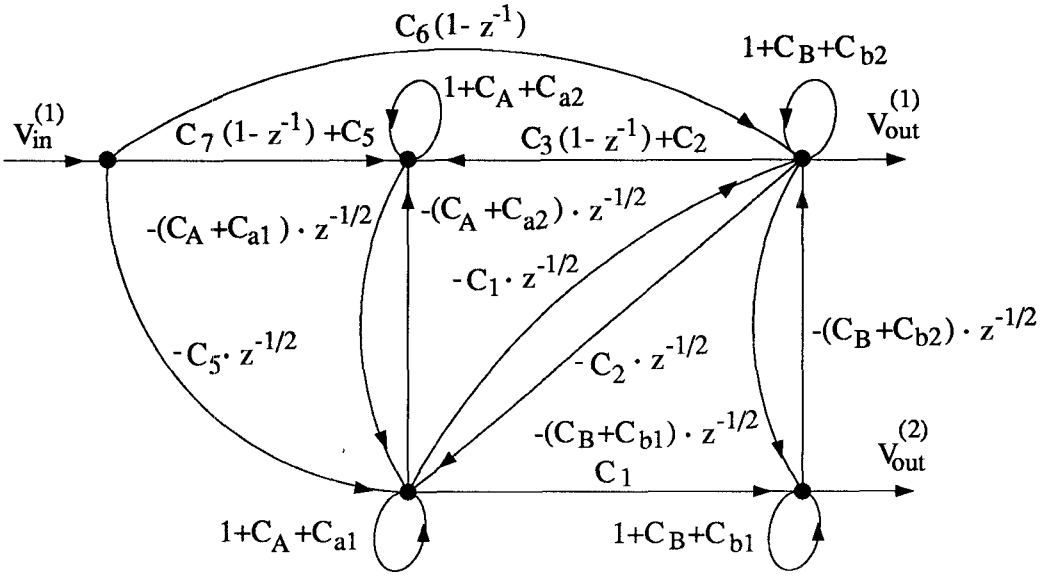


Figure 13: SFG of Type-I second-order filter.

Consider a second order lowpass notch (LPN) filter in the s-domain[7],

$$H_a(s) = \frac{1 + s^2/\Omega_1^2}{1 + s/(Q\Omega_0) + s^2/\Omega_0^2}. \tag{31}$$

Performing the bilinear transformation, where $T$ is the sampling period, the z-domain transfer function is given by

$$H(z) = \frac{(x_1^2+1) - (2x_1^2-2)z^{-1} + (x_1^2+1)z^{-2}}{(x_0^2 + x_0/Q + 1) - (2x_0^2-2)z^{-1} + (x_0^2 - x_0/Q + 1)z^{-1}}, \tag{32}$$

where $x_1 = 2/(\Omega_1 T) \gg 1$ and $x_0 = 2/(\Omega_0 T) \gg 1$. Also defining

$$\alpha = 4/(x_0^2 + x_0/Q + 1) \approx (\Omega_0 T) \tag{33}$$

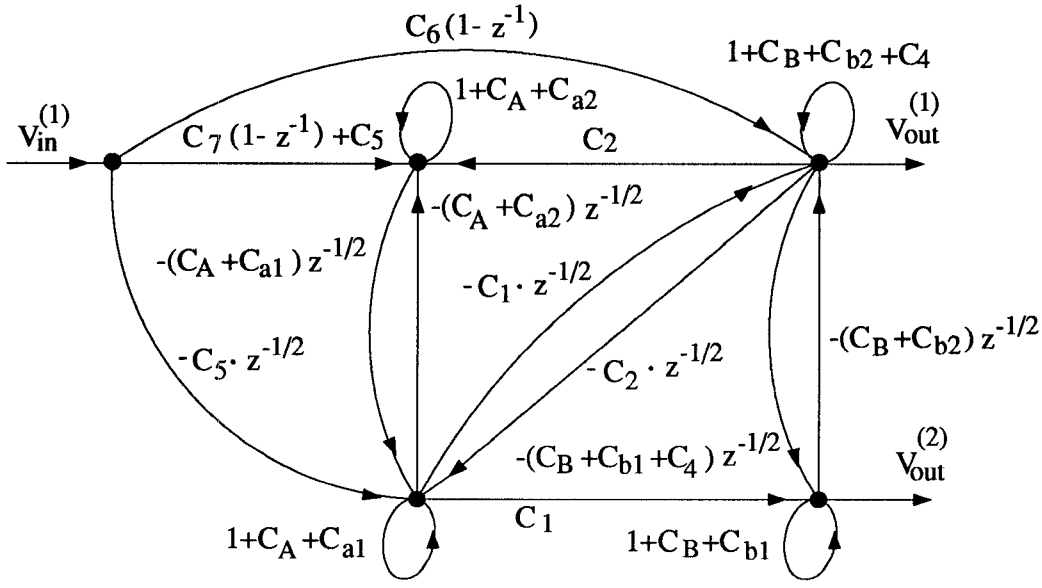


Figure 14: SFG of Type-II second-order filter.

$$\beta = (x_0/2Q)[4/(x_0^2 + x_0/Q + 1)] \approx \Omega_0 T/Q \tag{34}$$

$$\gamma = 4/(x_1^2 + 1) \approx (\Omega_1 T)^2. \tag{35}$$

Note that $\alpha \ll \beta \ll 1$ in general. The transfer function becomes

$$H(z) = \frac{(\alpha/\gamma)(1 - (2-\gamma)z^{-1} + z^{-2})}{1 - (2 - \alpha - \beta)z^{-1} + (1-\beta)z^{-2}}. \tag{36}$$

For the Type-I implementation, the following equations must be satisfied

$$\alpha = \frac{C_1 C_2 (C_{a1} - C_{a2})(C_{b1} - C_{b2})}{(C_A + C_{a1})(C_A + C_{a2})(C_B + C_{b1})(C_B + C_{b2})} \tag{37}$$

$$\beta = \frac{C_1 C_3 (C_{b1} - C_{b2})}{(C_A + C_{a2})(C_B + C_{b1})(C_B + C_{b2})} \tag{38}$$

$$\gamma = \frac{C_1 C_5 (C_{a1} - C_{a2})(C_{b1} - C_{b2})}{C_6 (C_A + C_{a1})(C_A + C_{a2})(C_B + C_{b1})}. \tag{39}$$

To minimize the capacitance spread, a reasonable choice is

$$C_1 = C_2 = C_{a2} = C_{b2} = C_{o1} = C_{o2} = 1 \tag{40}$$

$$C_{a1} = C_{b1} = 1 + \delta \tag{41}$$

$$C_A = C_B = K, \tag{42}$$

where $\delta$ should not be too small for the acceptable sensitivity. The capacitor values can be solved as,

$$K = \sqrt{\delta/\sqrt{\alpha} + (\delta/2)^2} - 1 - \delta/2 \approx \sqrt{\delta/(\Omega_0 T)} - 1 \tag{43}$$

$$C_3 = (\beta/\alpha)(\delta/(k + 1 + \delta)) \approx Q. \tag{44}$$

For the unity gain,

$$C_2 = C_5 = 1 \tag{45}$$

$$C_6 = (\Omega_0^2/\Omega_1^2)(K + 1). \tag{46}$$

Note that the dynamic scaling and minimum capacitance scaling should be performed by the suitable software. In the same analysis, if the Type-II implementation is chosen[6],

$$\alpha = \frac{C_1 C_2 (C_{a1} - C_{a2})(C_{b1} - C_{b2})}{(C_A + C_{a1})(C_A + C_{a2})(C_B + C_{b1})(C_B + C_{b2})} \tag{47}$$

$$\beta = \frac{C_4(C_{b1} - C_{b2})}{(C_B + C_{b1})(C_B + C_{b2} + C_4)} \tag{48}$$

$$\gamma = \frac{C_1 C_5 (C_{a1} - C_{a2})(C_{b1} - C_{b2})}{C_6(C_A + C_{a1})(C_A + C_{a2})(C_B + C_{b1})}. \tag{49}$$

The capacitor values can be assigned as follows:

$$C_{a2} = C_{b2} = C_1 = C_2 = C_{o1} = C_{o2} = 1 \tag{50}$$

$$C_{a1} = C_{b1} = 1 + \delta \tag{51}$$

$$C_A = C_B = K, \tag{52}$$

to reduce the capacitance spread, then $K$ is the solution of

$$(K+1)^4 + 2(K+1)^3\delta + (K+1)^2\delta^2 + \frac{(K+1)\beta\delta}{\alpha} - \frac{\delta^2(1-\beta)}{\alpha} = 0. \tag{53}$$

For unity DC gain, $\Omega_0 T \ll 1$ and $\Omega_1 T \ll 1$, it can be shown,

$$K \approx \sqrt{\delta/(\Omega_0 T)} - 1 \tag{54}$$

$$C_2 = C_5 = 1 \tag{55}$$

$$C_4 = (\beta\delta)/(\alpha(K+1+\delta)(K+1)) \approx 1/Q_0 \tag{56}$$

$$C_6 = (\alpha/\gamma)(K+1+C_4) \approx (\Omega_0^2/\Omega_1^2)(K+1+C_4). \tag{57}$$

From the above analysis, it has been showed that Type-I is suitable for high Q (quality factor $\geq 1$) application and Type-II should be used in the low Q circuits in terms of small capacitance spread.

# Acknowledgements

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