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Component Placement on PWB'S For Routability and Reliability

by

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Abstract: The placement of components on a printed wiring board (PWB) affects reliability, manufacturability, maintainability, and cost. In the past, placement techniques have been developed solely on the basis of minimizing the total wirelength necessary for the complete interconnection of the components. This paper presents techniques to improve placement based on reliability as well as routability. The approach discusses an innovative coupled force-directed methodology.

Key Words: Layout, placement, routability, reliability

Introduction: Placement of electronic components onto a printed wiring board (PWB) is a complex problem which involves a number of tradeoffs between several often conflicting goals. A good placement configuration provides sound thermal management, high reliability, and the ease of producibility. For these reasons, placement procedures must help maintain cooling paths on the board, minimize the failure rate of components due to the thermal response of the system, maintain track sizes and widths at prescribed levels to minimize wire build-up, cross-talk, and signal degradation, minimize the number of layers on which routing paths are layed out, minimize the number of vias necessary to interconnect layers, and reduce congestion (or wire cross-overs). In effect, the placement configuration should reduce the life cycle cost of manufacturing and maintenance in the field. Layout engineers are thus faced with the task of examining a large amount of data on the characteristics of individual components, the logic design of the system, the electical constraints, the thermal control being employed, and physical constraints placed on the size, shape, and weight of board, as well as the environmental characteristics to which the electronic system will be exposed.

The layout stage of an electronic system design is the link between the creative logical design of a viable electronic system and the practical design which must go into physically realizing the system. The layout process incorporates partitioning, assignment, placement, and routing. In the partitioning and assignment stage, a logic diagram is partitioned into logic elements which have assigned to them electronic components which perform the desired functions. On the basis of the given logic design, groups of electrically common pins, refered to as signal sets, are interconnected to form nets. Since electronic components contain a number of pins, it is common for individual components to belong to more than one distinct net. Furthermore, due to electrical considerations, such as timing signals, some signal sets may be more critical than others. After the signal sets are assigned, the components must be placed on the board. The board provides the physical support for the components and a base on which the interconnection paths are routed.

The most common measure used to determine the success in placement is based on an approximation of the total wirelength necessary to route the board. Minimizing the

total wirelength generally reduces the wiring area, congestion, and the number of vias necessary for routing. At present, there are many placement techniques based on minimizing the wirelength [1-13].

When considering the component placement problem, it is clear that no one method can satisfy the large number of goals and constraints which can be applied. In fact, placement for one goal can have an adverse effect on some other goal. For example, if components are placed strictly for reliability, the routability of the board may become unacceptable. Thus, any placement procedure must allow for a certain amount of sacrifice on some or all of the placement goals. If tradeoffs are not made, then the design may never reach maturity.

In the placement of electronic components on a PWB, reliability prediction and analysis have typically been treated as post-processes. However, design for reliability should be up-front in the design process. In particular, Pecht, Palmer, and Naft [22] have examined placement for reliability on convectively cooled boards and developed placement routines for determining near optimum placement configurations. Dancer, Pecht, and Palmer [20] compared several optimization schemes for convectively cooled PWBs for computational accuracy and speed. Mayer [23] has examined optimizing reliability and life-cycle cost based on the thermal design of avionic electronics. In addition, the MIL-HDBK-217E [17] and the Reliability Design Handbook [27] stress the importance of reliability considerations in the design of all electronic systems.

In this paper, a method of combining placement for reliability and routability is discussed. The method consists of a coupled force-directed placement procedure which is modified to include reliability and routability placement information. An example is given to demonstrate the use of the procedure and to show the trade-off capabilities between placement for reliability and routability. Details of this work can be found in [29].

Placement for Reliability: In the design of electronics for reliability, there are a number of handbooks, specifications and guidelines which can be employed. The Military Handbook MIL-HDBK-217E [17], is one standard for the military and is commonly employed in industry. The failure rate, λ_i, for an individual component can be expressed in terms of the Arrhenius model in the form

$$\lambda_i(Tjc_i) = D_i + B_i e^{-A_i \left\{ \frac{1}{Tjc_i + 273} - \frac{1}{298} \right\}} \qquad (1)$$

where B_i and D_i are constants determined by the package type, electrical and thermal characteristics for component i, and Tjc_i is the component junction temperature. The reliability of a PWB is dependent on the failure rates of all the components mounted on it. The failure rate is a monotonically increasing function of the component junction temperature, which is dependent on the heat dissipation, the locations of the components, and the cooling technology employed. Thus, although individual component reliabilities improve with the reduction of temperature, optimizing the placement for thermal response does not necessarily guarantee optimal reliability [22,23]. Since individual components have different heat dissipations, thermal resistances, and reliability sensitivities, the total failure rate must be considered as a criterion for effective PWB placement.

When the components of the PWB are assumed to be serially interconnected, the total failure rate, λ_T, of the PWB is

$$\lambda_T = \sum_{i=1}^{N} \lambda_i(Tjc_i) \qquad (2)$$

where N is the number of components on the board. The objective is to improve the total reliability of the PWB by minimizing the total failure rate of the board. The concept employed in the solution of the problem is based on an innovative interpretation of the scheduling problem addressed by Rothkopf [24,25], and McNaughton [26]. They found that if the cost function is a linear or exponential function of some variable t, then a priority ordering scheme exists which guarantees an optimum solution. Since the failure rate prediction equations are exponential with respect to the component junction temperature, the problem is to develop the placement scheme to include the heat transfer equations of the cooling mode being applied to the board.

Force-Directed Placement for Reliability and Routability: The Reliability placement procedures can be used to achieve placement configurations that have near minimum total failure rates for conduction and convection cooling models. Using a force-directed placement methodology, a global placement procedure for both routability and reliability is developed. To apply the force-directed placement procedure to the problem of placement for reliability, the reliability placement procedures are used to produce a placement pattern on the board based on the number of rows or columns desired on the board and the dimensional constraints of the board and the components. A fictitious connectivety matrix is then generated to yield the same placement configuration under force-directed placement processing. The fictitious connectivity matrix is called the position-adjacent matrix. The actual connectivity matrix, is developed from the interconnection nets or signal sets following the procedure of Quinn and Breuer [6].

Tc show the applicability of the coupled force directed placement procedure, an example is given. Components were selected from the MIL-HDBK-217E [17]. The values of the π factors used in the calculation of the component failure rates were: $\pi_Q = 0.25$, $\pi_L = 1.0$, $\pi_E = 1.0$, and $\pi_V = 1.0$. The coupled force-directed placement procedure was applied for both convection and conduction cooling models using weighting factors, ω, of 0, 0.25, 0.5, 0.75, and 1.0. A weighting factor of $\omega = 1$ represents placement for routability while $\omega = 0$ represents placement for relizability. When $\omega = 0.5$ the force constants are equal for routability and reliability. The final placement arrangements was set in array form on the board from the rough placement configurations resulting from the coupled force-directed placement procedure.

Once the components were positioned on the board, the placement was analyzed in terms of the approximate total wirelength (TWL) and the total failure rate (λ_T). To approximate the total wirelength, the center to center Manhatten distance was measured between each pair of interconnected components and summed over all interconnections. This procedure yields a measure of the complete graph needed to connect all components in the various signal sets. In the convection case, the working fluid was air with an inlet fluid temperature of 20°C and an average outlet temperature of 40°C. Although, the rows are not physically independent this treatment yields results with only marginal errors. The conduction cooling analysis was performed using a finite difference model on the board. The boards had sinks at opposite ends along their lengths. The sink temperature was set at 30°C. The sides of the boards were assumed to be insulated. From the thermal and reliability analysis, the component junction temperatures and the total failure rate were calculated for each placement arrangement. Figure 1 gives the input data for the 10 component example.

The ten components were placed on a convectively cooled board that is cooled from left to right through a fin structure attached to the bottom of the board. In the reliability placement procedure, the placement configuration was set to have 3 rows parallel to the flow direction. The convection placement procedure results are given in Figure 2. From these results, the position-adjacent matrix can be established. For example, since component U1 is adjacent to component U8, a 1 is placed in the position adjacent matix in row 1 column 8 and row 8 column 1. Since component U7 is in column 1 and row 2 on the board as a result of the placement procedure, it is adjacent to components U6 and U9 which are also placed in column 1 on the board and component U5 which is to be positioned in row 2 and column 2 on the board. Entries are made in the position adjacent matrix based on these facts. Since component U7 is in column 1 on the board which is on the inlet edge, an entry is made in the position-adjacent matrix at column 7 and row 7. The entire position-adjacent matrix is established and presented in Figure 3a. The corresponding replusive matrix is given in Figure 3b. The entries are given as 1 since for this particular case only the reliability placement is tested. In the coupled placement procedure, the two matrices presented in Figure 3 are multiplied by the average connectivity matrix entry.

The connectivity matrix is generated from the net list given in Figure 1, and the connectivity matrix is depicted in Figure 4. The results of placement for convection and conduction cases are shown in Figures 5 and 6. The total wirelength (TWL) and the total failure rate (λ_T) are defined as the percentage off of the minimum value calculated for each example. For example, if λ_{Tmin} is the minimum calculated failure rate and for a particular weighting factor, λ_{Tcal} is calculated, then the percent off is given by

$$\lambda_{Tpercent} = \frac{\lambda_{Tcal} - \lambda_{Tmin}}{\lambda_{Tmin}} \times 100 \qquad (3)$$

The same procedure is employed to caculate the precent off the total wirelength. Examining the graphs in Figures 5 and 6, we note that the total wirelength experiences a smooth transition of TWL while increasing the weighting factor.

The coupled force-directed placement procedure allows the layout designer to place components for either reliability or routability depending on the selected weighting factor. In addition, the placement procedure can be used as a tool to place components and then determine the tradeoffs which can be made in placing for reliability and routability. As the weighting factor is increased to 1 (towards placement for routability), the total wirelength decreases as expected. The total failure rate generally increases when increasing the value of the weighting factor. The rate of increase in the total failure rate with the increasing weighting factor is generally more erratic than the rate of decrease in the total wirelength. The problem is that the position-adjacent matrix models a final reliability placement configuration, which when combined with the routability placement procedure loses some of the physics of the reliability placement procedures.

When applying the force-directed placement procedure to highly connected systems, the components tend to cluster and the resolution of components into positions on the board becomes difficult. In some cases, the placement procedure must be performed in several stages. Initially, all components are allowed to move freely on the board until the system converges. Then, components on the outer edge of the clusters are assigned board slots relative to their positions with the other components on the board. Once the components are assigned border locations, these components are locked in place and the force-directed placement algorithm is repeated. If

overlapping is still a problem, more components on the outer edge of the clusters are assigned positions based on their relative positions to the other components on the board. These components are then locked and the force-directed placement algorithm is repeated. The procedures described above are continued until all components positioning are resolved.

All programs were written in Borland's TURBO BASIC and run on the IBM AT personal computer. The force-directed placement algorithm required from three to five minutes depending on the problem size. The resolution of overlap was performed using the assignment algorithm developed by Munkres [28]. Placement resolution required four to eight minutes depending on the problem size.

Summary: The methodology for placement of electronic components presented here is based on minimizing the total failure rate of the system and on minimizing the total weighted wirelength. A coupled force-directed placement procedure was developed to combine placement for reliability and routability.

The methodology of placement for reliability differs from existing methods of placement in that it addresses the physics of the problem rather then methodically guessing at better placement configurations. For a placement procedure to be totally effective, consideration of other electrical and mechanical constraints must be included in the hierarchy of the placement system.

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References:

1. R. Collett, "Board layout systems grapple with advanced technology", Digital Design (January 1986), pp.55-58.

2. M. Hanan and J. Kurtzberg, "Placement techniques" in Design automation of digital systems: Theory and Techniques, Ed. M. A. Breuer, New York, Prentice-Hall, (1972), chp. 5.

3. G. Odawara, K. Iijima, and K. Wakabayashi, "Knowledge based placement technique for printed wiring board", 22th Design Automation Conference, (1985), pp. 616-622.

4. G. Wippler, M. Wiesal, and D. Mlynski, "A combined force and cut algorithm for hierachical VLSI layout", Pro. 19th Automation Conf. (1982), pp.671-677.

5. M. Hanan, P. Wolff, and B. Agule, "A study of placement techniques for computer logic graphs", Proc. 13th Design Automation Conf., (June 1976), pp. 214-224.

6. N. Quinn and M. Breuer, "A force directed component placement procedure for printed circuit boards", IEEE Trans. CAS, vol. CAS-26, no.6, (1979), pp.377-388.

7. N.R. Quinn, "The placement problem as viewed from physics of classical mechanics", Proc. 12th Design Auto. Conf., June 23-25, 1975, pp. 173-178.

8. L. Steinberg, "A backboard wiring problem: A placement algorithm", SIAM Review, vol. 3, no.1, (Jan. 1961), pp.37-50.

9. L. Corrigan, "A placement capability based on partitioning", Proc. 16th Design Automation Workshop, 1979, pp.406-413.

10. D. Schweikert, "A 2-dimensional placement algorithm for the Layout of electrical circuits", Proc. 14th Design Automation Workshop, 1976, pp. 408-416.

11. B. Kernnighan and S. Lin, " An efficient heuristic procedure for partitioning graphs", Bell Systems Technical Journal, (Feb. 1970), pp. 291-307.

12. D. Schmidt and L. Druffel, "An iterative algorithm for placement of intergated circuits", Proc. 12th Design Automation Workshop, (1975), pp.361-368.

13. Design Automation of Digital Systems: Theory and Techniques, Ed. M.A. Breuer, New York, Prentice-Hall, (1972).

14. M. Breuer, "General survey of design automation of digital computers", Proc. of the IEEE, vol. 54, no.12, (December 1966), pp. 1706-1721.

15. R. Burden and J. Fairs, Numerical Analysis 3rd Ed., Prindle, Weber, & Schmidt, Boston, Mass., (1985).

16. J. Sloan, Design and Packaging of Electronic Equipment, Van Nostrand Rienhold Company Inc.., New York, New York, (1985).

17. "Reliability Prediction of Electronic Equipment", MILITARY HANDBOOK MIL-HDBK-217E, Rome Air Development Center, Feb. 1987.

18. M. Osterman and M. Pecht, "A placement methodology for reliablity on a convectively cooled printed wiring board", June 1987, submitted to Transactions of ASME Journal of Engineering for Industry.

19. M. Osterman and M. Pecht, "Placement of integrated circuits for reliability on conductively cooled printed wiring boards", Dec. 1987, ASME Winter annual Meeting, Division of Electrical and Electronic Packaging, Boston, Mass.

20. D. Dancer, M. Pecht, M. Palmer, "Reliability optimization scheme for convection cooled printed circuit boards", submitted to IEEE Transaction on Reliability, March 1987.

21. M. Pecht, "Computer aided design for PCB reliability", Proc. 33rd Annual Institute of Environmental Sciences Conference, May 2-5, 1987.

22. Pecht, Palmer, and Naft, "Thermal reliability management in PCB design", Proc.: 1987 Annual Reliability and Maintainability Symposium, Jan. 27-29, 1987.

23. Mayer,A., "Computer-aided thermal design of avionics for optimal reliability and minimum life-cycle cost", AFFDL-TR-7848, Mar. 1978.

24. M.H. Rothkopf, "Scheduling independent tasks on parallel processors", Mgmt. Sci., vol. 12, no. 8, (Jan. 1966), pp. 437-447.

25. M. Rothkopf and S. Smith, "There are no undiscovered priority index sequencing rules for minimizing total delay costs", Operation Research, vol.32, no.2, (March-April 1984), pp.451-456.

26. R. McNaughton, "Scheduling with deadlines and loss functions", Mgmt. Sci., vol.6, no.1, (Oct. 1959), pp.1-12.

27. Research Analysis Center, March 1976, Reliability Design Handbook, Cat. No. RDH-376, IIT Research Institute, Chicago, IL.

28. J. Munkres, "Algorithm for the assignment and transportation problems", J.SAIM, vol. 5, no. 1, March 1957, pp.32-38.

29. M. Osterman and M. Pecht, "Coupled force-directed placement for failure rate and wire length optimization," SRC Technical Report, University of Maryland, Aug. 1987.

Comp Name	Type	Heat Diss (W)	R_{jc} °C/W	A_i	C_1	C_2	Com-plex-ity	# of pins	Connections
U1	00108-C	0.24	50	4635	0.01	0.0048	6G	14	U2,U6,U8
U2	00404-C	0.18	50	4635	0.01	0.0048	3G	14	U6,U7
U3	02601-C	0.04	50	5214	0.01	0.0048	4G	14	U8,U9,U10
U4	02802-C	0.12	50	5214	0.01	0.0048	3G	14	U5,U9,U10
U5	65001-C	0.30	50	6373	0.01	0.0048	4G	14	U7,U10
U6	40301-J	1.00	40	5794	0.16	0.0090	16384B	24	U1,U2,U7,U8 U10,U10,U10
U7	23105-E	0.94	50	5214	0.025	0.0056	1024B	16	U2
U8	08101-C	0.48	50	5214	0.01	0.0048	2G	14	U1,U3
U9	10104-C	0.40	50	7532	0.01	0.0048	29T	14	U3,U4,U10
U10	07904-E	0.34	50	5214	0.01	0.0056	15G	16	U3,U4,U5,U6 U6,U6,U10

Figure 1. Component Data for Placement Example TN10

U9	U3	U8	U1
U7	U5	U2	
U6	U4	U10	

Figure 2. Convection Placement Results

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10
U1	0	0	0	0	0	0	0	1	0	0
U2	0	0	0	0	1	0	0	1	0	1
U3	0	0	0	0	1	0	0	1	1	0
U4	0	0	0	0	1	1	0	0	0	1
U5	0	1	1	1	0	0	1	0	0	0
U6	0	0	0	1	0	1	1	0	0	0
U7	0	0	0	0	1	1	1	0	1	0
U8	1	1	1	0	0	0	0	0	0	0
U9	0	0	1	0	0	0	1	0	1	0
U10	0	1	0	1	0	0	0	0	0	0

a) Position-Adjacent Matrix

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10
U1	0	0.286	0.286	0.286	0.286	0.286	0.286	0	0.286	0.286
U2	0.286	0	0.286	0.286	0	0.286	0.286	0	0.286	0
U3	0.286	0.286	0	0.286	0	0.286	0.286	0	0	0.286
U4	0.286	0.286	0.286	0	0	0	0.286	0.286	0.286	0
U5	0.286	0	0	0	0	0.286	0	0.286	0.286	0.286
U6	0.286	0.286	0.286	0	0.286	0	0	0.286	0.286	0.286
U7	0.286	0.286	0.286	0.286	0	0	0	0.286	0	0.286
U8	0	0	0	0.286	0.286	0.286	0.286	0	0.286	0.286
U9	0.286	0.286	0	0.286	0.286	0.286	0	0.286	0	0.286
U10	0.286	0	0.286	0	0.286	0.286	0.286	0.286	0.286	0

b) Position-Adjacent Replusive Matrix

Figure 3. Reliability Placement Matices for Example

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10
U1	0	1	0	0	0	1	0	1	0	0
U2	1	0	0	0	0	1	1	0	0	0
U3	0	0	0	0	0	0	0	1	1	1
U4	0	0	0	0	1	0	0	0	1	1
U5	0	0	0	1	0	0	1	0	0	1
U6	1	1	0	0	0	0	1	1	0	3
U7	0	1	0	0	1	1	0	0	0	0
U8	1	0	1	0	0	1	0	0	0	0
U9	0	0	1	1	0	0	0	0	0	1
U10	0	0	1	1	1	3	0	0	1	0

a) Connectivity Matrix

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10
U1	0	0	0.731	0.731	0.731	0	0.731	0	0.731	0.731
U2	0	0	0.731	0.731	0.731	0	0	0.731	0.731	0.731
U3	0.731	0.731	0	0.731	0.731	0.731	0.731	0	0	0
U4	0.731	0.731	0.731	0	0	0.731	0.731	0.731	0	0
U5	0.731	0.731	0.731	0	0	0.731	0	0.731	0.731	0
U6	0	0	0.731	0.731	0.731	0	0	0	0.731	0
U7	0.731	0	0.731	0.731	0	0	0	0.731	0.731	0.731
U8	0	0.731	0	0.731	0.731	0	0.731	0	0.731	0.731
U9	0.731	0.731	0	0	0.731	0.731	0.731	0.731	0	0
U10	0.731	0.731	0	0	0	0	0.731	0.731	0	0

b) Replusive Matrix

Figure 4. Interconnection Matices for Example

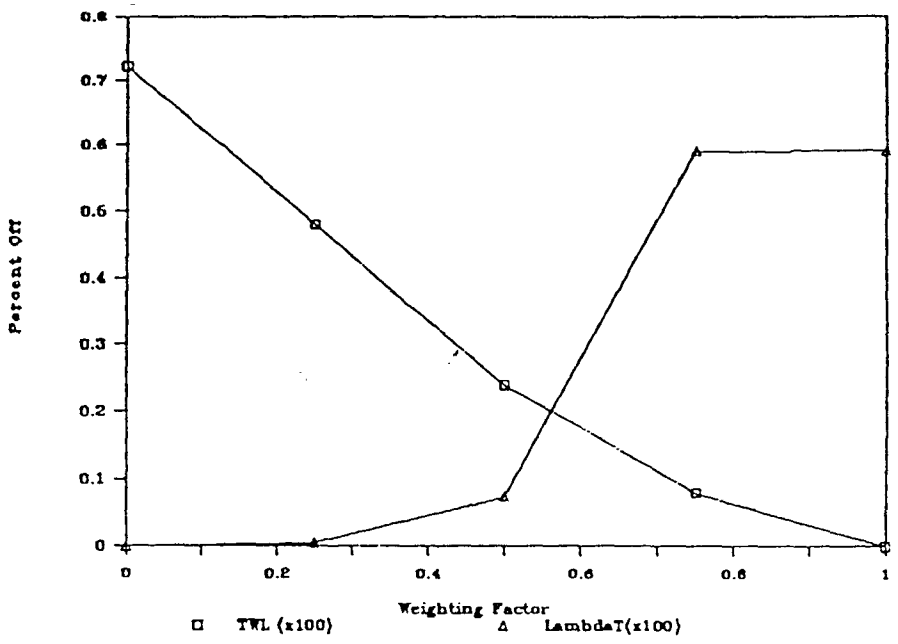

FIGURE 5: Convection Case

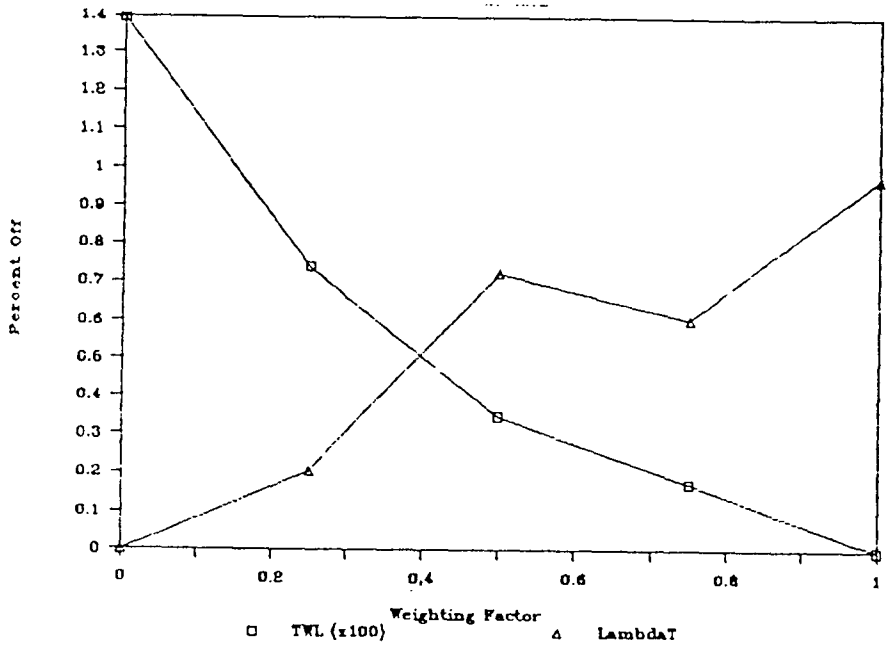

FIGURE 6: Conduction Case

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