ABSTRACT

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Because of technological advancement, transistor dimensions are approaching the length scale of the electron Fermi wavelength, on the order of only nanometers. In this regime, quantum mechanical phenomena will dominate electron transport. Using InAs single quantum wells, we have fabricated Y-shaped electron waveguides whose lengths are smaller than the elastic mean free path. Electron transport in these waveguides is ballistic, a quantum mechanical phenomenon. Coupled to the electron waveguide are two gates used to coherently steer the electron wave. We demonstrate for the first time that gating modifies the electron's wave function, by changing its geometrical resonance in the waveguide. Evidence of this alteration is the observation of anti-correlated, oscillatory transconductances. Our data provides direct evidence of wavefunction steering in a transistor structure and has applications in high-speed, low-power electronics.

Quantum computing, if realized, will have a significant impact in computer security. The development of quantum computers has been hindered by challenges in producing the basic building block, the qubit. Qubit approaches using semiconductors promise upscalability and can take the form of a single electron transistor. We have designed, fabricated, and characterized single electron transistors in InAs, and separately in silicon, for the application of quantum computing.

With the InAs single electron transistor, we have demonstrated one-electron quantum dots using a single-top-gate transistor configuration on a composite quantum well. Electrical transport data indicates a 15meV charging energy and a 20meV orbital energy spacing, which implies a quantum dot of 20nm in diameter. InAs is attractive due to its large electron Landé g-factor.

With the silicon-based single electron transistor, we have demonstrated a structure that is similar to conventional silicon-based metal-oxide-semiconductor field effect transistors. The substrate is undoped and becomes insulating at low temperatures. There are two layers of gates that when properly biased define the single electron transistor potential profile. The measured stability chart at 4.2K indicates a charging energy of 18meV. Our silicon-based single electron transistor is promising, because spin coherence times in silicon are orders of magnitude longer than those in GaAs.

QUANTUM TRANSPORT IN NANOSCALE SEMICONDUCTOR DEVICES

By

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Dedication

To my wife and parents.

Acknowledgements

The accomplishments detailed in this thesis would not have been possible without the help of many individuals. Although I cannot hope to thank everyone, I feel it is important to acknowledge those who had the most significant impact.

First and foremost, I would like to thank my advisor Chia-Hung Yang. Chia-Hung leads by example. His dedication and extraordinary work ethic demonstrate the level of commitment that is necessary to succeed in our field. Furthermore, his hands-on approach has been the primary catalyst in helping me to achieve significant experimental results in so little time. I have no doubt that my experiences in Chia-Hung's courses and laboratory will have a positive and lasting influence on my future work.

Next, I would also like to thank Ming Jey Yang who provided us with the InAs samples that made many of these devices possible. In addition, Ming Jey helped us to refine our device processes and worked tirelessly to help us characterize many of the devices presented in this thesis. I would also like to thank my past and present group members including Andy Cheng who taught me how to process devices and Binhui Hu who provided support in the development of data acquisition programs and device simulation.

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Kenton Brown and Kevin Eng. Kenton and Kevin have not only provided me with their silicon processing experience, they have also been friends who have helped me to moderate my stress level when the pressures of work seemed overwhelming.

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Chapter 1: Introduction

1.1 Motivation

Downscaling metal-oxide-semiconductor field-effect-transistors (MOSFETs) can enhance the performance of integrated circuits and increase the circuit complexity. However, this approach faces unprecedented challenges. Immediate problems include excess heat dissipation and short channel effects. As a result, there has been interest in alternative approaches to MOSFETs such as molecular transistors, or carbon nanotubes. However, as emerging technologies, these proposals must still overcome many significant difficulties before they can realistically be implemented.

On the other hand, as a MOSFET becomes nanometers in size, electron transport is dominated by quantum phenomena. These quantum phenomena include tunneling, size quantization, phase coherence, and ballistic transport. Because modern fabrication technology exists to make artificially patterned semiconductor nanostructures, we take on the task of studying devices whose dimensions are small enough that quantum effects dominate their electronic behavior. We exploit quantum mechanics for transistor applications, because quantum wavelike phenomena are known to respond fast and consume little power. The Y-branch switch (YBS) is one such proposed device. In the YBS, a lateral electric field perpendicular to the direction of electric current in the source waveguide steers the injected electron wave into two drains simultaneously. The YBS offers several advantages, including THz speed switching and switching voltage 40-80 times lower then today's conventional electronics. The Y-branch switch will be discussed in detail in chapter 3.

In view of the limits in the von Neumann computer architecture, quantum computing has attracted significant attention. Algorithms using quantum computers are proven to be much more efficient in factoring large numbers and sorting large lists. Various approaches for a quantum computer have been proposed and investigated. Semiconductor-based single electron transistors are researched as a possible building block for solid state quantum computing, because it is expected that they can be up-scaled into a fully functional quantum computer more easily than other proposals.

In a single electron transistor, electrons are confined on an island, and the number of electrons is controlled by a capacitively coupled gate. This gate can force the addition or subtraction of individual electrons from the island. Isolation of only one electron on the island of a single electron transistor is the first milestone in producing a semiconductor spin-based qubit. In chapters 4 and 5, we report two such single electron transistors, from concept to physical realization, and provide their measurement characteristics with analysis.

1.2 Organization of Thesis

Chapter 2 will introduce the basic physics pertaining to low-dimensional quantum phenomena. Chapter 3 focuses on transport in a one-dimensional electron waveguide known as the Y-branch switch. Chapters 4 and 5 will discuss single electron transistors fabricated in InAs and silicon respectively.

Chapter 2: Low-Dimensional Physics

The primary purpose of this chapter is to introduce the basic mechanisms of quantum transport in semiconductor low-dimensional devices. For a basic treatment of solid state physics and device physics, please refer to the popular textbooks by Kittel,[1] Aschroft and Mermin,[2] and Sze.[3] For a comprehensive review of two-dimensional (2D) and one-dimensional (1D) transport, see, Ando, Fowler, and Stern[4] as well as the texts by Y. Imry[5] and S. Datta.[6] The zero-dimensional (0D) transport section follows the reviews of Kouvwenhoven,[7,8] Ono[9] and Hadley.[10]

2.1 Two-Dimensional Electron Systems

Consider first free electrons traveling in three-dimensional space. When the physical movement becomes confined in one direction, the system is analogous to the "particle in a box" problem in quantum mechanics. Such physical confinement of the electrons causes the electron's kinetic energy in the direction of confinement to be quantized into discrete states. These discrete energy levels are also called the transverse modes. As the confinement dimension is reduced, the quantization energies and their spacing are increased. Such energy quantization becomes significant if the length scale of confinement is on the same order as the electron Fermi wavelength. When only the lowest energy subbands are occupied, the electrons display many properties that can be best understood by a strictly two-dimensional electron gas (2DEG) model, despite a small but finite wavefunction span in the confinement direction.

One example of 2DEG is the metal-oxide-semiconductor (MOS) capacitor system. In the MOS sample system, the electrons (or holes) confined at the Si/SiO_2 interface fill the lowest 2D subbands. (See Figure 2.1) The two-dimensional density of states can be verified by photoluminescence,[11] or by the quantum hall effect (QHE).[4] Note that photoluminescence characterization is only applied in direct-bandgap semiconductors, thus not useful for silicon.

2.2 One-Dimensional Systems

In semiconductors, once a two-dimensional system is formed we can create tight confinement in an additional dimension, using either electrostatic gating or etching techniques.[12] Verification of the 1D density of states can be performed by using photoluminescence techniques[13] or by transport.

One specific case of 1D quantum wire is the quantum point contact[14] (QPC). A quantum point contact is a narrow constriction of a two-dimensional electron gas. Typically the constriction is formed by electrostatically depleting the two-dimensional carriers. Figure 2.2 shows a schematic representation of a QPC structure that uses electrostatic gating to define a 1D quantum wire. When the length dimension of the QPC is shorter than the elastic mean free path, and the width is on the order of the Fermi wavelength, electrons will traverse from source to drain without scattering. This unscattered, phase coherent transport is referred to as “ballistic.” The resulting conductance through the QPC is quantized,[15] and any addition (or subtraction) of 1D subbands increases (or decreases) conduction in steps. The conductance of the 1D wire

becomes a direct measure of the number of populated 1D subbands. Observing the quantized conductance verifies the presence of ballistic transport.

The quantized conductance of a QPC can be derived as follows. The current through a quantum point contact can be written as

$$j = nev_F, \tag{2.1}$$

where n is the electron concentration, e is the elementary unit of charge and v_F is the Fermi velocity. This expression can be rewritten as

$$j = (DOS)(\delta\varepsilon)e\frac{\hbar k_F}{m^*}, \tag{2.2}$$

where DOS is the 1D density of states $\frac{m^*}{2\pi\hbar^2 k_F}$, $\delta\varepsilon = qV_{applied}$ (the bias applied across the QPC), $\hbar = h/2\pi$ where h is Plank's constant, k_F is the Fermi wavevector, and m^* is the electron effective mass. Inserting the DOS and $\delta\varepsilon = eV_{applied}$ the expression becomes:

$$j = V_{applied}\frac{e}{h}e \text{ , that is,}$$

$$\frac{j}{V_{applied}} = G_{QPC} = \frac{e^2}{h}, \tag{2.3}$$

where G_{QPC} is the conductance of the QPC. Finally, we multiply the conductance by 2 to account for spin degeneracy in the system. As more subbands are introduced the 1D wire the conductance becomes

$$G_{QPC} = n\frac{2e^2}{h}, \tag{2.4}$$

where n is the total number of occupied subbands in the QPC. As the number of one-dimensional subbands is modified in the QPC, the conductance forms a series of plateaus

called the quantum staircase. A schematic of the quantum staircase is shown in Figure 2.3.

2.3 Zero-Dimensional Electron Systems

A zero-dimensional system or quantum dot (QD) can be defined as a small region of semiconductor where the confinement length in all three directions is on the order of the Fermi wavelength. The easiest way to understand the semiconductor QD system is to again adopt the "particle in a box" picture. The quantized energy levels in the QD are commonly referred to as 0D states. Zero-dimensional confinement in QDs has been verified by photoluminescence[16] as well as through magnetotransport using a device known as a single electron transistor (SET).

The SET structure is similar to a conventional field-effect transistor, but now the conducting path under the gate is broken by two tunneling barriers into three sections known as the "source," the "island," and the "drain."[17] (Figure 2.4) Transport through the SET is governed primarily by a classical phenomenon called Coulomb blockade. Coulomb blockade occurs because charges on the island repel each other through Coulomb force. The addition of a single charge to the island, referred to as the charging energy $E_{C,}$ requires energy of $e^2/2C_\Sigma$ where C_Σ is the total capacitance of the island to the outside world and e is the fundamental unit of charge. If the potential difference between the gate and electron gas is V_G, the electrostatic energy of the total charge on the island is given by

$$E_{Island} = -eV_G + e^2 / 2C_\Sigma . \qquad (2.5)$$

The first term is the attractive interaction between the positively charged gate electrode and the charge on the isolated island. The second term is the repulsive Coulomb interaction of all the charges on the island to each other. When sweeping the gate voltage, current will only flow at the certain discrete values that cause the Fermi level and quantized electron energy levels to be aligned. The transfer relation, that is, the drain current versus the gate voltage under a constant drain bias, shows a sequence of peaks, reflecting the Coulomb blockade phenomenon. Figure 2.5 shows a schematic of the SET transfer relation as a function of applied gate voltage.

Under the condition that the thermal energy of the system, k_BT, is smaller then the 0D energy level spacing of the system, we can use transport through the SET to probe the discrete energy levels of the QD. Because the energy levels in the QD are size quantized, to add an additional electron, the electron must overcome ΔE and E_C where ΔE is the 0D energy level spacing. Figure 2.6 shows the energy band diagram of a SET with quantized 0D energy levels. In the approximation that every electron on the island is repelled equally by every other electron regardless of energy state, the total ground state potential energy (U_{Total}) of a quantum dot with no applied magnetic field becomes

$$U_{Total}(N) = \frac{[e(N - N_o) - C_G V_G]^2}{2C_\Sigma} + \Sigma E_N \qquad (2.6)$$

where N is the number of electrons on the island at an applied gate voltage V_G, N_o is the initial number of electrons on the island with no applied gate voltage, and ΣE_N is the sum of the occupied energy states of the quantum dot. $C_G V_G$ is determined by the gate voltage applied to the dot over the gate capacitance. The electrochemical potential of the dot is given by

$$\mu_{dot} = U_{Total}(N) - U_{Total}(N-1) \qquad (2.7)$$

Combining equations 2.4 and 2.5, a solution for the electrochemical potential of the dot can be rewritten as

$$\mu_{dot} = (N - N_O - 1/2)E_C - e(C_G / C_\Sigma) + E_N \qquad (2.8)$$

The energy necessary to add a single electron to the quantum dot, known as the addition energy E_A, can be solved using the electrochemical potential of the dot by finding the difference of the electrochemical potentials at the N and N+1 state.

$$E_A = \Delta\mu(N) = \mu_{dot}(N+1) - \mu_{dot}(N) \qquad (2.9)$$

$$E_A = E_C + E_{N+1} - E_N$$

$$E_A = e^2 / C_\Sigma + \Delta E \qquad (2.10)$$

In this case the addition of an electron to the island becomes the sum of the charging energy and the energy difference between two discrete states ΔE.

Application of a sweeping dc bias to the SET drain while stepping the gate voltage produces a transfer relation called a stability chart or "diamond chart." (Figure 2.7) The stability chart can be used to characterize the SET tunneling barrier capacitances as well as the size of the quantum dot by the "Orthodox Theory."[18] Using this approach, the height (e/C_Σ), the width (e/C_{gate}), and the slopes defining the diamond (C_{gate}/C_{drain} and $-C_{gate}/C_{source}$) uniquely determine the SET addition energy. By finding these capacitances, we can model the dot as a disc of radius *r* and solve for the radius using

$$C_\Sigma = 8\varepsilon r, \qquad (2.11)$$

where ε is the semiconductor dielectric constant. Using the radius of the dot the 0D energy level spacing can be estimated. In Figure 2.7 the diamonds labeled by a single number represent the Coulomb blockaded regions, while the diamonds labeled with two numbers are regions where tunneling through the SET occurs.

When the semiconductor island is small enough and becomes quasi-zero-dimensional, it is possible to operate the SET in a regime where there is only one electron confined in the QD. The one-electron regime is necessary in order to use the electron trapped on the SET island as a qubit.

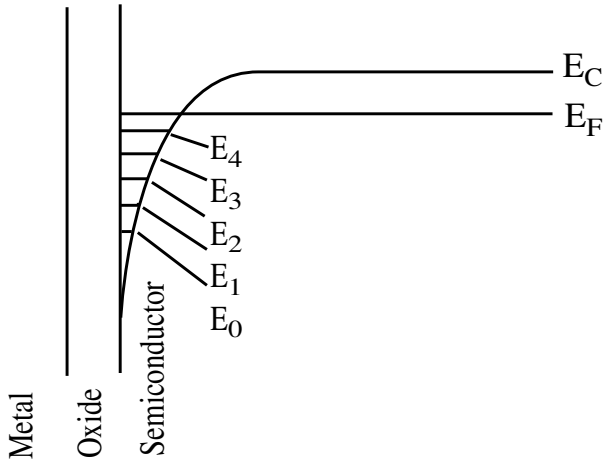


Figure 2.1: Schematic of MOS energy band bending illustrating the formation of two-dimensional electrons (2DEG) confined in the z-direction at the Si/SiO_2 interface. In MOS, the electrons or holes confined at the Si/SiO_2 interface reside in quantized two-dimensional states and exhibit 2D transport characteristics such as the quantum hall effect.

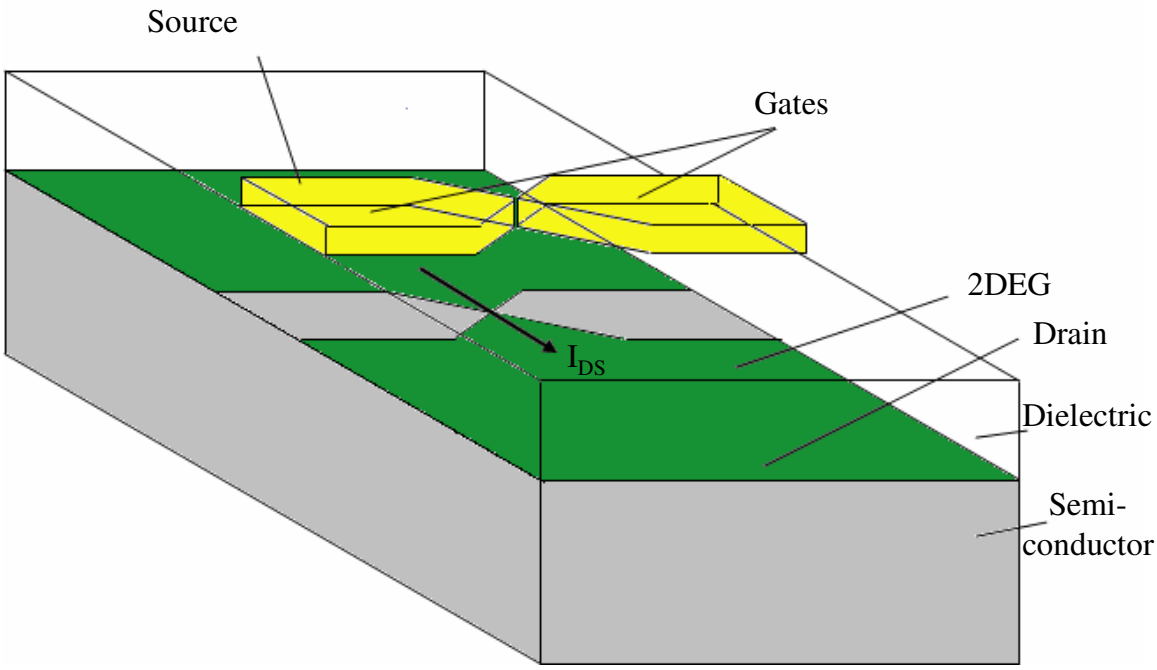


Figure 2.2: Structural schematic of a quantum point contact where 2D carriers are electrostatically depleted by the application of bias to capacitively coupled gates.

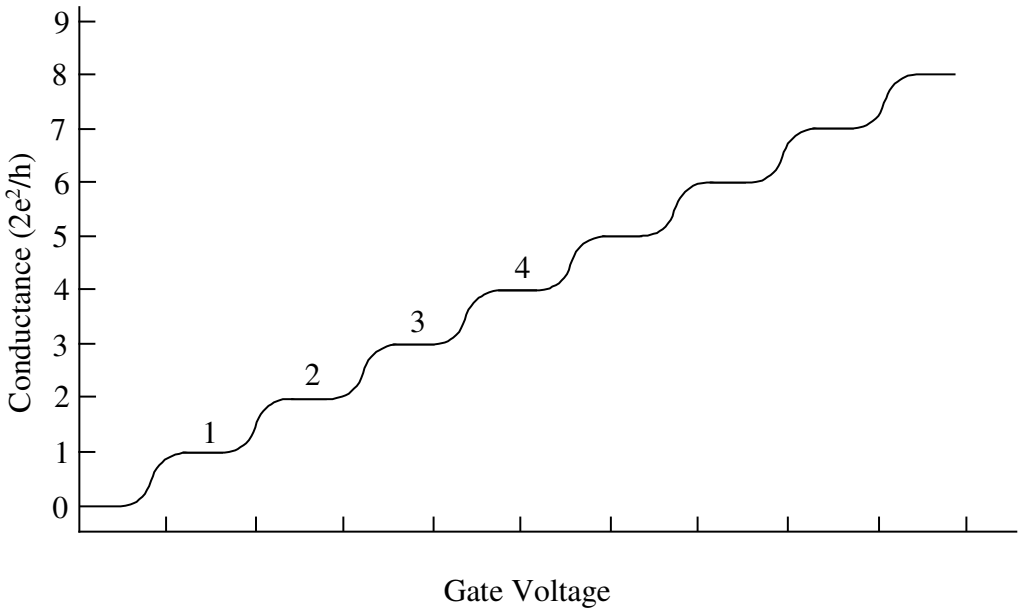


Figure 2.3: Schematic of the conductance through a quantum point contact. Typically in a QPC the number of occupied 1D subbands is tuned by applying bias to the electrostatic gates that form the 1D constriction. As the gate voltage is swept, a series of plateaus develop in the conductance through the device. This transfer relation is known as the "quantum staircase."

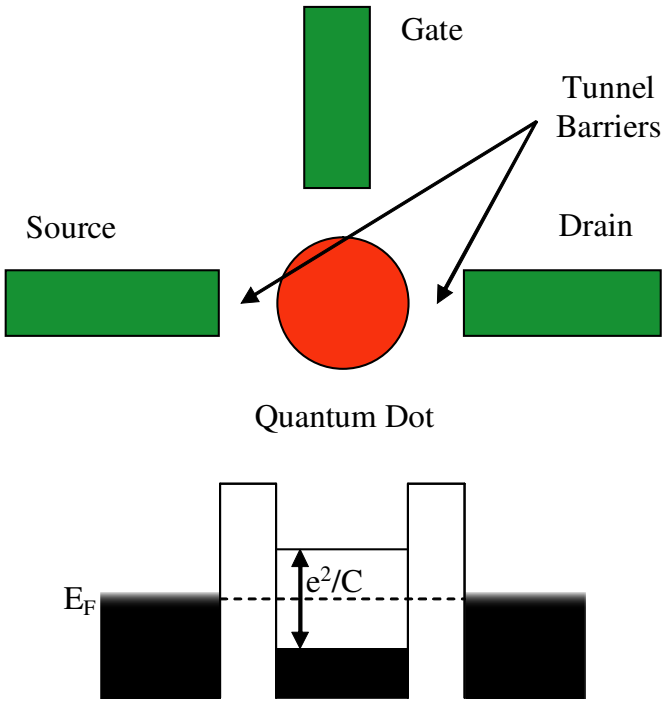


Figure 2.4: (Top) A schematic of the single electron transistor (SET) structure. A small area of semiconductor is isolated from its surroundings by two tunneling barriers. A gate is capacitively coupled to the island with the intention of modifying the island's electrochemical potential. (Bottom) Energy band diagram of the SET showing the Coulomb blockade energy that must be overcome to add an additional electron to the quantum dot.

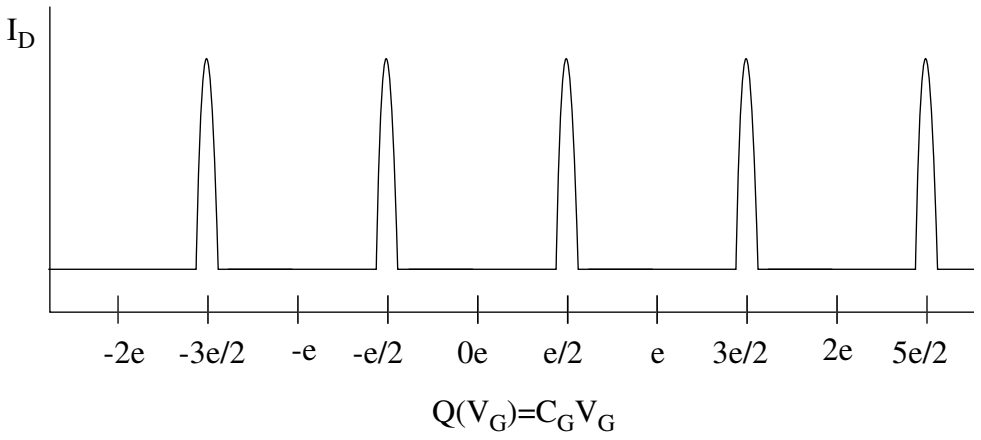


Figure 2.5: Schematic representation of Coulomb blockade oscillations. Conductance peaks correspond to the intersection of diamonds in the stability chart shown in Figure 2.7.

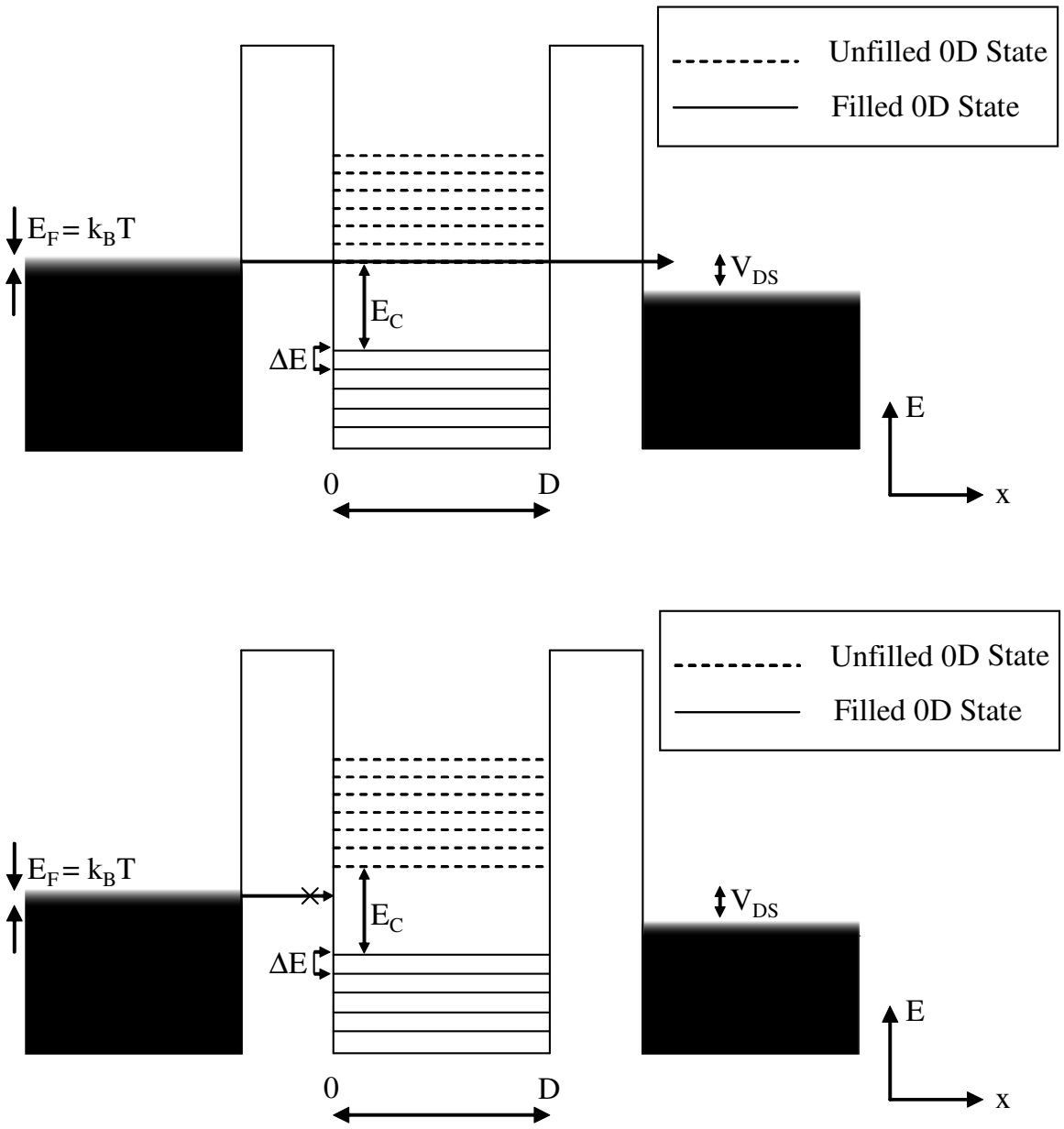


Figure 2.6: Energy band diagram of a single electron transistor during different operating points. (a) Without the proper gate voltage, electron tunneling is blocked by Coulomb Blockade. (b) Applying enough gate voltage to overcome the addition energy E_A will align the Fermi energy with the next unpopulated state in the single electron transistor, allowing tunneling onto the quantum dot. Under a small applied bias, electrons can tunnel out to the drain allowing conduction through the device.

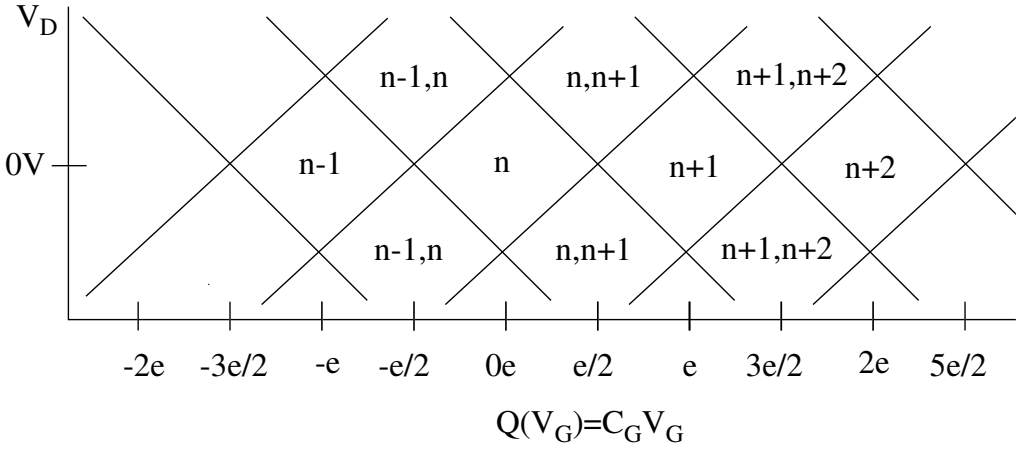


Figure 2.7: A schematic representation of the SET stability chart. The diamonds in the stability chart labeled with single numbers represent regions where the number of electrons trapped on the SET island is stable. Diamonds labeled with two numbers are bias conditions where electrons are tunneling through the SET. By electrostatically depleting the quantum dot, a stable state with one trapped electron can be achieved.

Chapter 3: InAs Y-Branch Switch

Quantum coherent devices exploit the electron's wavelike properties by incorporating the electron wave mechanics into the device operating principle. It has been speculated that quantum coherent devices may provide low power operation as well as faster response time than classical metal-oxide-semiconductor field-effect transistors (MOSFETs).[19] There have been various proposals of quantum coherent devices, such as the Aharonov-Bohm (AB) interferometer,[20] quantum ratchet rectifier,[21] resonant tunneling diode,[22] spin-FET,[23] and Y-branch switch.[27] All of the aforementioned devices take advantage of the wavelike nature of electrons. For example, the quantum ratchet[24] is a small asymmetric cavity patterned in high-mobility 2DEG. As coherent electrons propagate through the ratchet, the asymmetry in the geometrical shape of the cavity causes the transmission of electrons to be asymmetric as well. In quantum ratchets, the rectification of an ac current has been observed.[21] Another device whose operating principle relies on electron phase coherence is the AB interferometer.[25] An AB interferometer is a small ring that displays constructive and destructive interference patterns in its conductance. We have previously studied the AB rings[26] using one-dimensional (1D) quantum wires in InAs quantum wells. In the following chapter I will discuss our experimental demonstration of a phase coherent transistor, the Y-branch switch (YBS).

3.1 InAs Y-Branch Switch Introduction

The original proposal of the Y-branch switch (also commonly referred to as Y-channel transistor, or YBS)[27] came from an electron wave analogy to the fiber optic coupler. The semiconductor version of YBS has a narrow electron waveguide patterned into a "Y" configuration with one source and two drain terminals. (See Figure 3.1) When patterned with a symmetric Y geometry, an electron wave packet traveling from the source to drains will flow into both drains with equal quantity, as illustrated in 3.1 (a)-(c). When a lateral electric field is applied perpendicular to the direction of electric current in the source, the YBS steers the injected electron wave packet in the direction opposite to the electric field, altering the conductance to the two drains simultaneously. (Figure 3.1 (d)) Thus, the YBS behaves like a quantum mechanical version of the classical differential pair amplifier formed by two conventional transistors. The YBS has been theoretically modeled by using the beam propagation method.[28] Figure 3.2 shows the simulated wave packet propagation, taken from the paper by Palm and Thylen.[27]

In theory, YBS offers several advantages as a fast switch. Based on the following estimation, we anticipate that the YBS should be able to operate in the THz regime. Assuming a Y-splitting region of 100nm, an electron wave packet with a Fermi velocity v_F of 1×10^7 cm/sec should traverse the switching region with a transit time of τ_t=1ps and a theoretical device operation frequency of $f = (1/\tau_t)$ = 1THz. Another interesting feature of the YBS occurs for the case of single mode occupation, where theoretically the switching can be accomplished by a voltage of the order of $\hbar/(e\tau_t)$ = 0.6579mV for τ_t=1ps.[29] The switching voltage applied to the gate of a YBS can in principle be smaller than the thermal voltage, k_BT/e = 25.9mV at T = 300K, as opposed to 40-80 times of

k_BT/e needed for the current MOSFETs.[30] Here k_B is the Boltzmann constant and T is the absolute temperature. Switching at low voltages would allow such devices to operate with less noise and consume less power than conventional electronics, though at the expense of speed.[31]

Prior to the research in this thesis, the experimental results on YBS's and other similar devices reported had yet to demonstrate the proposed quantum switching. In almost all of the efforts, such as those in T-branch,[32] Y-junction,[33,34,35] and ballistic rectifiers,[21,36] the electrical characterizations were carried out at a source-drain bias significantly larger than k_BT/e. As a result, the transport mechanism of these devices deviates too much from the (near) equilibrium condition, which is necessary to maintain long phase coherence length. Therefore, coherent transport plays no significant role in the characteristics of devices reported so far. In fact, a recent Monte Carlo simulation on the above-mentioned devices further indicates[37] that all of the reported main features can be described classically without involving ballistic (and coherent) transport.

This chapter describes the first experimental demonstration of a YBS operated in the quantum regime. The YBS is produced using InAs electron waveguides. All transport characteristics reported here are acquired with an excitation voltage less than the thermal energy in order to keep the system near equilibrium. The characteristics of our YBS's show significant deviation from classical transport features.

3.2 InAs Single Quantum Well

The practical difficulty in realizing a YBS has been in fabricating nanometer-scale electron waveguides without depleting electrons in the narrowest portions of the

waveguide. Most research has been performed using the mature GaAs/$Al_xGa_{1-x}As$ heterostructure system. But the edge depletion width at the GaAs/$Al_xGa_{1-x}As$ sidewall is not controllable, resulting in a conducting wire that has built-in randomness in the transverse length dimension. We have overcome this problem by using InAs. Two-dimensional electron gas (2DEG) in InAs quantum wells can have a long mean free path, l_e,[38] and thus long coherence length. Furthermore, the InAs/AlSb system has a number of properties that are advantageous for nanofabrication and for studying low-dimensional physics. First, it is possible for the surface Fermi level pinning position in InAs to be above its conduction band minimum, allowing for the physical width of InAs conducting wires to be only nanometers with no edge depletion.[39,40,41] This allows us to overcome the main practical difficulty in fabricating a YBS that plagued previous research efforts. A second consequence of having the Fermi level pinned above the conduction band minimum of InAs is that the formation of ohmic contacts to the 2DEG is much simpler than in GaAs, where metal contacts have to be deposited and annealed to form spiked alloy domains which contact the 2DEG. With InAs we simply deposit metal directly on the InAs surface, forming non-alloyed ohmic contact with the electrons in the quantum well. Lastly, the small InAs electron effective mass (0.023 m_0) leads to large size quantization.

Our transistors are built on InAs single quantum wells grown by molecular beam epitaxy. Grown on GaAs substrates, a typical structure has a 2 μm undoped AlSb buffer, GaSb/AlSb smoothing superlattice, a 100nm AlSb bottom barrier, and a 17nm InAs quantum well (QW). The structure is shown in Figure 3.3 (a). Figure 3.3 (b) shows a schematic of the InAs QW band bending, and 3.3 (c) shows the InAs/AlSb energy band

alignment. Magnetotransport studies were used first to calibrate the 2D electron concentration (n_{2D}) and mobility (μ_{2D}) of the as-grown sample. Quantum Hall plateaus and Shubnikov de Haas oscillations, signatures of a high-quality 2D electron system, are clearly observed on photo-lithographically patterned Hall bars.

We obtained two-dimensional electron concentrations (n_{2D}) of 3.09×10^{12} cm^{-2}, 2.08×10^{12} cm^{-2} and 1.08×10^{12} cm^{-2}, and two dimensional electron mobility's (μ_{2D}) of 1.06×10^{4} cm^2/V-s, 1.67×10^{4} cm^2/V-s and 1.54×10^{4} cm^2/V-s, at 300K, 77K and 4.2K, respectively. The corresponding Fermi wavelength, Fermi energy, and mean free path length were calculated to be 14nm, 140meV, and 307nm at 300K, 17nm, 114meV, and 397nm at 77K, and 24nm, 85meV, and 264nm at 4.2K, respectively. These values can be found in Table 3.1.

3.3 InAs Fabrication

Fabrication of quantum wires in the bare InAs quantum well system is performed using standard electron beam lithography (EBL) and wet etching techniques. See Appendix A for the exact process details. Figure 3.4 illustrates the process steps necessary for formation of nanoscale features using this process. Using EBL, small thin wires are drawn into electron-beam sensitive resist and developed to produce a mask for wet etching. Wet etching removes the quantum well so that different regions (terminals) can be electrically insulated from each other.

For this work it is important to create "smooth" wires to reduce backscattering and improve ballistic transport. Here, the smoothness is referring to the lack of potential fluctuation at the boundary. A smooth boundary was achieved by using a homemade low-

molecular-weight electron beam resist that we call PMMA 120k T1, in combination with wet etching. The PMMA T1 mixture is made by dissolving a dry powder form of 120kg/mol PMMA in the solvent Toluene to 1% concentration. The mixture was then filtered for particulates by using a Teflon filter attached to a glass syringe, both of which are insoluble in Toluene. The filtered mixture was transferred into clean glassware for storage. Toluene was selected because it has a lower surface tension then other typically used solvents, such as Anisole or Chlorobenzene, so when spin-coated with a comparable spin-rate, it produces a thinner layer. The T1 used for this experiment was measured by alpha step to be 20nm thick when spun at 5kRPM for 45 seconds. We chose a lower molecular weight PMMA to reduce the roughness of the EBL defined features. Reducing the size of the polymer strands reduces the roughness of the EBL features transferred into the InAs at the exposure boundary. Reducing the roughness of the electron waveguide reduces backscattering and increases transmission in the lithographically defined lines.

Wet etching, rather than dry reactive ion etching (RIE), is chosen because using RIE to transfer the EBL features into the semiconductor produces damage, creating potential fluctuations near the edge of the defined wire. One difficulty with wet etching e-beam defined lines is that isotropic etching will also take place at the resist boundaries, undercutting the resist and increasing the feature width. The wet etch rate and lateral etch rate can vary from wafer to wafer, so for our specific wafer, these rates were precisely determined by a series of wet etch trial runs. The EBL patterns were then modified to account for this undercut which typically would increase the line-width from 70nm to roughly 250nm. In this work we define the nonconductive regions using EBL and wet etching, leaving behind narrow conducting wires of InAs, so typically the device's

conducting channel-widths were increased to allow for undercutting. Figure 3.9 shows an atomic force microscope (AFM) scan of a wet etched quantum point contact, a device that will be discussed in section 3.5. This scan shows clearly a thin wire surrounded by a slightly less deep side band. The thin wire is the original EBL-defined-feature and sideband is where the subsequent undercutting took place. In all the red regions, the QW has been completely removed, creating an insulating barrier. To produce this ~150nm channel, a channel width of roughly 400nm was programmed to account for undercutting.

In most cases, substrates are chosen to have a low background doping concentration, such that the carriers in the substrate freeze out at low temperatures, but conduct at room temperature. Higher purity substrates are only necessary for the substrate to be insulating at room temperature. The original purpose of the InAs QW wafer used for these experiments was to demonstrate ballistic transport at room temperature, so the substrate was chosen to be insulating even at room temperature. But the high resistivity substrate presented a problem during e-beam lithography. A good ground loop must be maintained during EBL. If this loop is not properly maintained, electrons can build up a charge density at the surface, causing the features to be overexposed. When performing EBL on high-resistivity samples, one practice is to use a thermally evaporated Al layer on top of the resist to form a conductive path to ground.[42] In addition, when e-beam writing on high-resistivity or non-conductive substrates, we hand-solder two indium points directly to the quantum well at the corner of the sample. The resistivity between the two points can be measured using a multimeter to verify whether the indium has successfully created a low resistance path to the quantum well. Typical two terminal measurements produced a resistivity of roughly 1-3 kΩ. It is important that the indium is applied before

the first resist coating, otherwise the resist is heated by the soldering process creating unpredictable lithographic results. When the e-beam writing is performed, the spring which holds the sample onto the sample holder is positioned to be in direct contact with one of the indium bumps, and the resistivity between the sample holder and the other indium bump are again measured to verify that the contact resistance between the spring and indium bump is minimized.

The final critical issue in successfully patterning this InAs QW wafer is to minimize the exposure of the AlSb layer to room air. Once the AlSb is exposed to the oxygen, the aluminum begins to oxidize. When the Al oxidizes it expands in volume and the increased volume creates stress in the QW nearby. Over time, Al oxidization will create cracks in the QW, destroying small, lithographically defined features. This leads to a finite device lifetime, which can only be prolonged through oxygen-free storage. One way to reduce exposure to room air is to leave a coating of resist on the surface, physically blocking oxygen. Also the sample was always stored whenever possible in a dry nitrogen environment where no oxygen exists to accelerate the damage. During fabrication, caution was taken to reduce exposure to room air for prolonged periods even though resist covered the majority of the surface during most processing steps.

3.4 InAs Cross Junction

To fabricate a YBS, two basic requirements must be independently verified. The semiconductor system in which the YBS is fabricated must have an electron mean free path that is long relative to the junction length of the YBS drain-coupling region. Also, because the operation of a YBS requires lateral electric field across to the branch

junction, it must be proved that a capacitively coupled gate can function without leakage. First, to measure the elastic mean free path we have used standard Hall effect longitudinal magnetoresistance measurements. To further verify ballistic transport on short length scales, we used EBL and wet etching to fabricate nanometer scale cross junctions for a type of ballistic transport measurement known as bend resistance measurements.[43]

Unlike quantum point contacts, bend resistance measurements use magnetic field rather than external gating to verify ballistic transport. Figures 3.5, 3.6, and 3.7 display the fabricated cross junctions via optical microscopy and atomic force microscopy, respectively. The dark blue region in 3.5 and dark red regions in 3.6 and 3.7 are nonconductive and have been etched off using selective wet etching. The light blue regions in 3.5 and yellow regions in 3.6 and 3.7 are where QW remains and electron transport takes place.

Figure 3.8 (a) shows a cross junction of the type used for bend resistance measurements. If the mean free path of the electrons is short compared to the junction length (not ballistic), electrons would be injected from the source, scatter in the junction, losing kinetic energy, and then be driven by the applied bias into the drain lead. In this case the voltage difference read from the two terminals opposite to the source and drain ought to be 0V. However when electrons have a mean free path with length larger than the junction length, there is a nonzero probability that they traverse the cross junction without scattering. This is referred to as ballistic transport. Since no scattering event occurs in the junction, this event is also phase coherent, that is, the phase of the electron is unaltered while passing through the junction. Electrons that traverse the junction

ballistically will build up in the opposite terminal before eventually energy relaxing with the local Fermi electrons. This ballistic transport process produces a steady state solution where the voltage reading between that opposite terminal and common will become negative. When a perpendicular magnetic field is applied during transport, the ballistic electron's trajectory can be magnetically focused away from the opposite terminal, restoring the negative voltage back to zero. This phenomenon is referred to as "negative bend resistance."[44] Figure 3.8 (b) shows a simulation of magnetic field on ballistic electrons using the "semiclassical" billiard ball approach.

Using a lock-in amplifier, a 1μA ac current is applied to two adjacent terminals of the cross junction. (Figures 3.8 and 3.9) The 1μA current is generated by applying $1V_{ac}$ from the output of the lock-in amplifier across a 1MΩ resistor in series with the device source and drain. Since the 1MΩ resistor is several orders of magnitude larger than the device resistance, the 1MΩ resistor and the ac voltage source behave effectively like an ac current source. Using a phase lock loop, the lock-in amplifier's differential input reads the voltage difference from the opposite two terminals of the cross junction, measuring whether or not a negative voltage develops.

At 77K, $k_BT = 6.63mV$, and the ac voltage applied to the device must be less than k_BT to meet the criteria for quantum coherent transport. Since the resistance of the cross junction is several orders of magnitude smaller than the 1MΩ resistor and the two are in series, the majority of the $1V_{ac}$ voltage drop is over the 1MΩ resistor, maintaining a voltage drop of less than 6.63mV over the device. Therefore the cross junction is still within the regime of quantum coherent transport. For example, a 1μA current over a 1kΩ

device would result in a voltage drop of 1mV, well below the criteria for quantum coherent transport at 77K.

Since the InAs QW is sensitive to electrostatic shock, it is very important that the constant current source from the lock-in is connected to the device while the current is turned off. The current is to be ramped up from 0 to 1μA, and back to zero, manually, thus eliminating the risk of any static buildup during connection. Before this precaution was taken, static charge buildup was found to permanently damage devices. Once damaged, a previously working device never produced negative differential resistance again.

Devices were characterized at room temperature and 77K, and at both temperatures, the 300nm cross junctions displayed negative voltage. The negative signal could be destroyed by magnetic focusing in a perpendicular magnetic field, confirming ballistic transport in our cross junctions.[45] Since the device is symmetric, it is expected that a symmetric measurement configuration (as shown in Figure 3.9) where the measurement is identical but rotated 90 degrees to be on different terminals of the cross junction, e.g., I(11,10)V(8,13) and I(10,8)V(13,11), should also produce a negative signal. The two numbers in the parentheses depict the current and voltage polarities. For example, in I(10,8), pin10=I_+, and pin8=I_-; in V(13,11), pin13=V_+ and pin11=V_-. The "pin" number refers to terminals matching a 14-pin carrier, and are assigned as shown in Figure 3.5. Both measurements should produce negative bend resistance, but it is important to verify transport symmetry in order to exclude other possible origins.[46]

Figure 3.10 shows transport characteristics for a typical 300nm device at 77K under application of an external magnetic field. At zero magnetic field, the device

displays a negative differential resistance of roughly 85μV. As magnetic field is applied perpendicular to the sample, the electrons are bent back toward the drain. As expected, the differential voltage is reduced when magnetic field is applied. In this case the signal was reduced by greater than 60% to approximately 30μV. Application of higher electric field should theoretically reduce the negative differential resistance to zero, and this was witnessed in some larger devices. However, with the 300nm size junction, at the time of this particular measurement, limitations in the magnet's power supply output restricted the ultimate achievable magnetic field. Figure 3.10 also shows the negative bend resistance of the same cross junction while source-drain bias was applied through a 90-degree rotation of the terminals. The combination of the device displaying the same negative signal regardless of bias orientation, as well as reduction of the signal under perpendicular magnetic field, unequivocally proves that the negative voltage is produced by ballistic transport through the cross junction.

3.5 InAs Quantum Point Contact

The second requirement for successful operation of a YBS is the production of a lateral electric field across the branch junction by electrostatic gating. In order to verify the gating effect and to obtain insight into our sample system, we fabricated quantum point contacts (QPCs) using an in-plane gate structure,[47] in which two isolated, coplanar, conductive regions on the opposite sides of the quantum point contact channel are used as the two side-gates. (Figure 3.11) When we short the two side-gates together and apply bias, electrons are induced or depleted in the channel through capacitive coupling. When the wire width is on the order of electron mean free path l_e, the transverse energy

subbands are quantized, forming 1D channels. The 1D channels can be depleted or populated by increasing or decreasing the applied side-gate voltage. (Section 2.2)

Characterization of the QPC devices was performed using a standard low-excitation lock-in technique at 4.2K. (Figure 3.12) The two side-gates are shorted for a common-mode measurement. In the common-source configuration, the ac excitation voltage at the drain is kept low at $30\mu V_{rms}$ to avoid the undesirable "self-gating" effect,[48,49] and to satisfy the requirement for "quantum transport," where the excitation must be less than k_BT. (362μeV at 4.2K) The drain current is fed to a transimpedance amplifier with input impedance less than 10Ω and a gain of 1MΩ or 10MΩ. The ac conductance is recorded as the gate voltage is swept from -1V to 1V. Figure 3.13 shows the typical current-voltage characteristics of a QPC and its numerical derivative. As expected, a series of plateaus, made more distinctive by additionally plotting their derivative, are observed. The measured conductance may be expressed as $G_N = 1/[1/(N \cdot \frac{2e^2}{h}) + R_S]$, where N is the number of one-dimensional spin degenerate channels and R_S is series resistance. (See section 2.2.)

As shown by horizontal lines in Fig. 3.13 with R_S=1150Ω, the calculated G_N fits well with the measured data and is in excellent agreement with the peak position in the derivative. This successful observation of the quantized conductance not only verifies the gating effect, but also demonstrates that the fabricated QPCs are indeed smaller than the electron mean free path l_e. Subsequently the YBS's which utilize the same basic gate geometry as the QPCs also will be smaller than l_e.

3.6 InAs Y-Branch Switch

Figure 3.14 shows optical microscope and AFM images of a finished YBS device. The neck of the device was measured to be 76nm using AFM. The gate geometry is intentionally the same as was used in the quantum point contact. However, now an additional insulating barrier is fabricated on the drain side that splits the drain in to two halves at the neck of the 1D channel. The operation of YBS requires a lateral electric field. Using the same in-plane gate structure as the QPC, we apply bias to these two side-gates differentially, forming a lateral electric field, perpendicular to the symmetry axis of the Y-junction.

Because of the ballistic coherent transport, the characteristics of gated YBS are expected to be drastically different from their classical counterparts. To measure the YBS, we utilized the same measurement technique as was used for the QPC except now the signal from each drain was fed into a separate low-impedance preamplifier and simultaneously measured by separate lock-in amplifiers. The measurement technique is shown in Figure 3.15.

Figure 3.16 shows the transfer characteristics of our YBS with 76nm wide junction. There is no measurable gate leakage current (< 0.1pA) in our measurements. The transconductances through Drain1 and Drain2 are shown as a function of the sweeping differential gate voltage: $-0.83V < V_{gate1} < 0.83V$, with $V_{gate1} = -V_{gate2}$. When V_{gate1} and V_{gate2} are swept, the electric field in the lateral direction steers the wavefunction and the interference pattern of the injected electrons. Under such differential gating, the Drain1 and Drain2 conductances show peaks and valleys. These oscillatory features are anti-correlated as shown in Figure 3.16 (a). The sum and the

difference of the two measured conductances are shown in Figures 3.16 (b) and 3.16 (c) respectively.

3.7 InAs Y-Branch Switch Analysis

The oscillatory transconductance is a manifestation of phase coherence in a multi-mode one-dimensional electron waveguide. Using a model InAs wire structure with a QW thickness of 17nm and width of 76nm, we estimate that there are nine 1D modes populated under equilibrium at 4.2K. The conductance through Drain1 in our device is slightly bigger than that through Drain2, as shown in Figure 3.16 (a). Such asymmetry is a non-universal feature, resulting from variation in confinement potential, impurity distribution, surface roughness, and contacts in the device. The overall potential profile in the device defines the oscillatory conductance features, and the scale of these features is a fraction of $2e^2/h$. This type of mesoscopic behavior is no surprise for devices with sizes smaller than the phase coherence length.[50]

We now qualitatively explain the features shown in Figure 3.16 (b). Here, the sum of the two drain conductances increases with increasing lateral electric field in either polarity. The eigenenergies of the transverse 1D modes, the corresponding wave functions, and the longitudinal component of the electron wave functions are defined by the given device potential. Electrons in the N^{th} transverse channel propagating in a waveguide from the source can be reflected back with amplitude r_N, transferred to the Drain1 waveguide with amplitude ε_{1N} and transferred to the Drain2 waveguide with amplitude ε_{2N}. If the YBS is patterned with perfect symmetry with respect to the axis of

the source waveguide, an odd number of transverse modes will have a maximum in the wavefunction at the center of the source channel. When scattering between transverse modes is ignored, the sum of the Drain1 and Drain2 conductances is given by $G_\Sigma = \sum_N \frac{2e^2}{h}\left(\varepsilon_{1N}{}^2 + \varepsilon_{2N}{}^2\right) = \sum_N \frac{2e^2}{h}(1 - r_N{}^2)$. If there is no transverse electric field, the reflection amplitude for an odd-numbered channel is maximal because electrons are strongly scattered by a beam splitter that separates Drain1 from Drain2. As a result, the corresponding contribution of odd-numbered channels to conductance is at its minimum. However, when a lateral electric field is applied, electrons are more likely to propagate into either Drain1 or Drain2, and are less scattered by the splitter. Therefore, reflection becomes weaker, and the sum of the conductances through Drain1 and Drain2 becomes bigger. For even-numbered modes, scattering off the beam splitter would likely increase with electric field, causing the reflection amplitude to grow, and correspondingly, the conductance to decrease. However, because in our structure the total number of modes is odd, (in this case 9 nodes exist) the gating effect in the odd channels prevails, and the sum of the conductances through the two drains increases by a fraction of $2e^2/h$.

An alternative explanation of the observed behavior of G_Σ is the increase of the number of conducting channels contributing to the current by one in the presence of transverse electric field. If the lateral confinement potential is parabolic, the energies of all transverse states decrease with applied electric field, resulting in more transverse states below the Fermi energy and an increased conductance. However, this is in fact not possible. For rectangular confinement, the quantization energy of the ground state decreases, but energies of all other levels increase, and no addition of channels should be allowed. The sensitivity to device geometry in the transport characteristics of these

mesoscopic devices underscores the importance of realizing specific confinement and impurity potentials for such structures.

3.8 InAs Y-Branch Switch Simulation

The observation that the conductances through Drain1 and Drain2 are predominantly out of phase agrees well with the notion that electric field steers the wave functions from one drain into the other. The individual Drain1 and Drain2 conductance characteristics are determined by the resonant transmission through quasi-localized states formed around the beam splitter. Figure 3.17 shows a simulation result of the quantum wave function in a narrow wire with 9 modes of random phase. By using a wave function with nine terms of the form

$$\Psi_n = \Psi_1(x)e^{iR_1} + \Psi_2(x)e^{iR_2} + \ldots , \qquad (3.1)$$

we can solve for the local electron density in a cross section of the channel using

$$\sigma(x,y) \propto |\varphi|^2 = |\Sigma_n[\Psi_n(x)\Psi_n(y)]|^2 \quad . \qquad (3.2)$$

The simulation illustrates how quasi-localized nodes of conductance exist in the channel. The location of the nodes is determined by the specific potential profile of the wire. Under application of lateral electric field the individual nodes nearest to the splitter may be steered back and forth between Drain1 and Drain2. Because each node is a superposition of 9 quantized conductance channels each node should have amplitude of roughly 1 unit of quantized conductance. This agrees well with our transport result in Figure 2.16 (c) where we see that the difference in conductance between Drain1 and Drain2 is on the order of 1 quanta of conductance.

3.9 InAs Y-Branch Switch Conclusion

In conclusion, we have fabricated and measured a coherent Y-branch switch. The YBS exhibits oscillatory transconductances that are always out of phase in the case of multiple modes. [51,52] Our measurements provide strong evidence that the electron wave packet is being steered by an external electric field and that the switching mechanism is quantum mechanical. Although the gate is capacitively coupled to the YBS as in classical transistors, the modulation of the drain current is a result of directly steering the electron wave function in the 1D channel. Our observation of the quantum steering of electron wave functions in a semiconductor waveguide opens up possibilities for further studies of quantum switches with multiple-terminal, nanometer-scale structure. This device should operate at THz speed, because the dwell time of an electron packet near the "Y" split is only on the order of 1ps. We have qualitatively explained the observed oscillatory transconductance by simulating a multi-mode device.

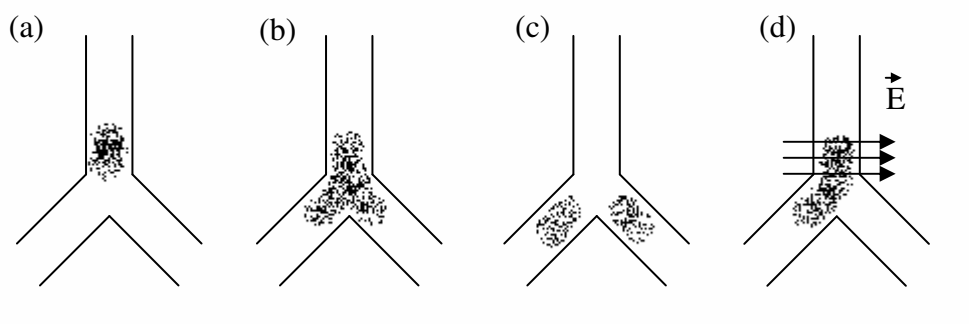


Figure 3.1: Schematic of a Y Branch Switch. (a)-(c) illustrate the symmetric injection of a Gaussian wave packet of electrons from source into two coupled drains. (d) When electric field is applied the electron wave packet can be steered to either the left or the right drains, depending on the direction of the lateral electric field. In (d), the electric field points to the right, and the wave is steered to the left.

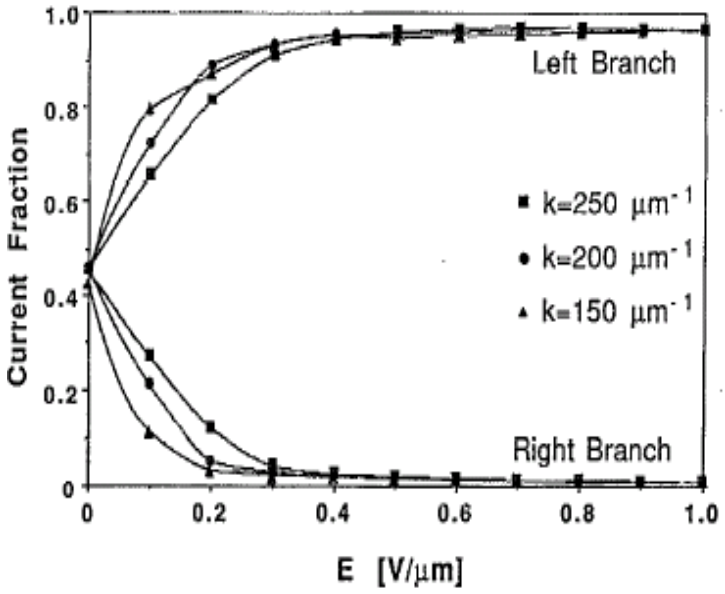


Figure 3.2: Calculated transport for a YBS from the original YBS proposal by Palm and Thylen.[27] Under application of transverse electric field the conductance to one drain is reduced as conductance to the other is increased. The change in conductance saturates at a moderate electric field, of about 0.3V/μm. Although there are some kinks in the conductance, full oscillations are not predicted.

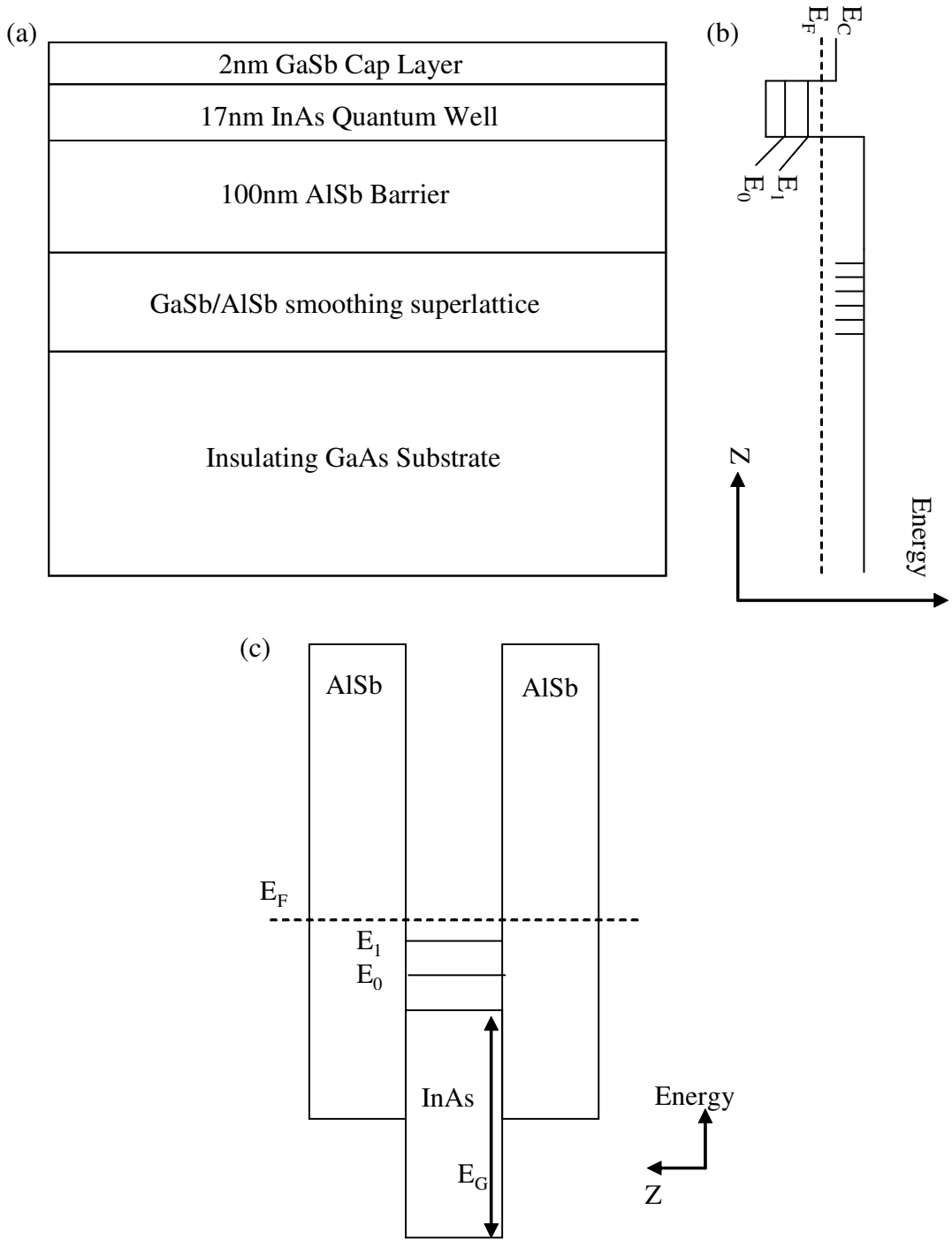


Figure 3.3: InAs single quantum well structure. (a) Shows the specific growth structure used to fabricate the YBS. (b) A schematic of the conduction band minimum of our specific MBE structure aligned to the growth schematic layers. (c) InAs and AlSb energy band alignment. InAs and AlSb form a type II heterojunction interface. When the InAs layer is thin enough electron energy states in the z direction become quantized as is displayed. E_0 and E_1 represent the populated 2-D subbands in the z direction.

Temperature	n_{2D}	μ_{2D}	λ_F	E_F	l_e
300 K	3.09×10^{12} cm^{-2}	1.06×10^{4} cm^2/Vs	14 nm	140 meV	307 nm
77 K	2.08×10^{12} cm^{-2}	1.67×10^{4} cm^2/Vs	17 nm	114 meV	397 nm
4.2 K	1.08×10^{12} cm^{-2}	1.54×10^{4} cm^2/Vs	24 nm	85 meV	264 nm

Table 3.1: Properties of the 2D electron gas in InAs quantum well. Here n_{2D} is the two dimensional electron concentration of the InAs single quantum well. μ_{2D} is the electron mobility, λ_F is the Fermi wavelength, E_F is the Fermi energy and l_e is the electron mean free path length.

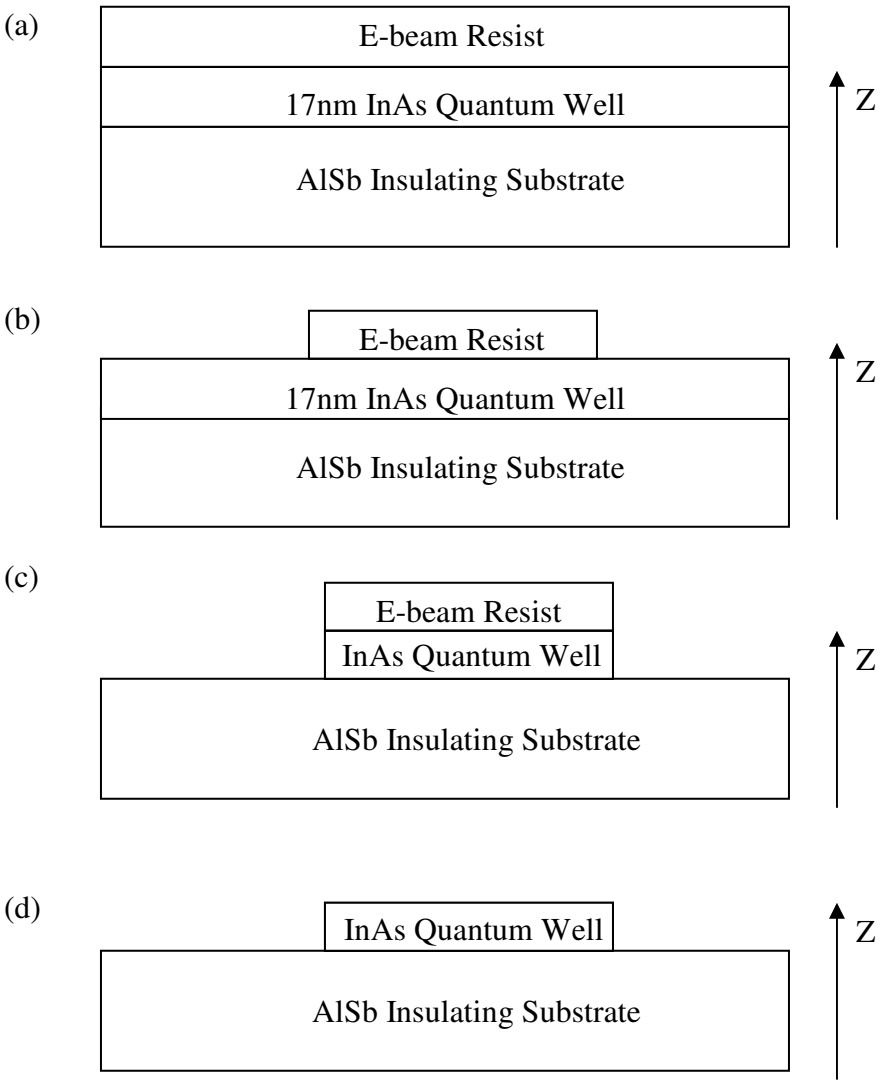


Figure 3.4: Standard process for fabrication of 1D wires using electron beam lithography. (a) Spin coating of electron beam sensitive resist (b) Exposure and wet chemical development of resist. Development removes only the exposed regions of resist. (c) Selective wet etching is used to remove InAs quantum well in the exposed areas. (d) Removal of resist using resist solvent such as acetone cleans the semiconductor surface.

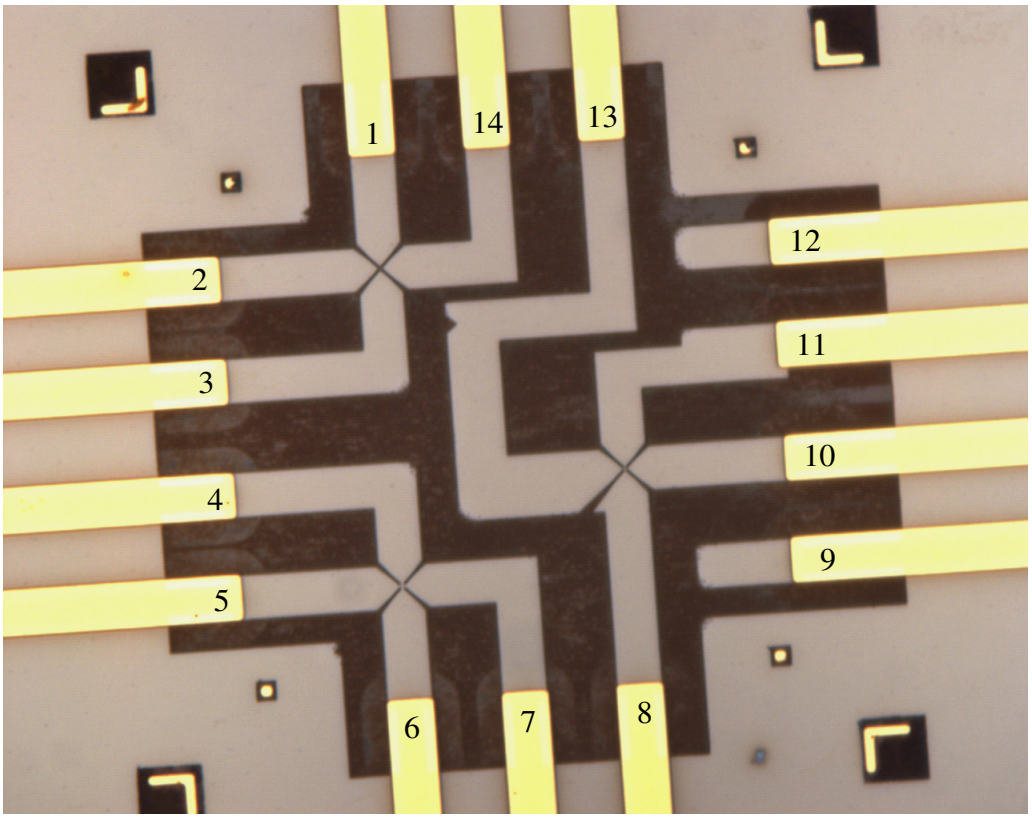


Figure 3.5: Cross junction devices fabricated on InAs. Above is an image of fabricated cross junction devices taken via optical microscope. The dark areas are where the InAs quantum well has been removed by wet etching. Subsequent exposure to the environment oxidizes the exposed AlSb layer causing the etched area to become dark. The gold leads are patterned using photolithography and the cap layer is etched so that they are in direct contact with the cross junction at each of the 4 inputs. Wet etching appears to have totally removed the quantum well connecting the four ohmic contacts in the top two junctions. However further investigation by AFM reveals that they are still viable. Device leads are arbitrarily assigned pin numbers. This numbering is the convention for any electrical measurement described in later sections.

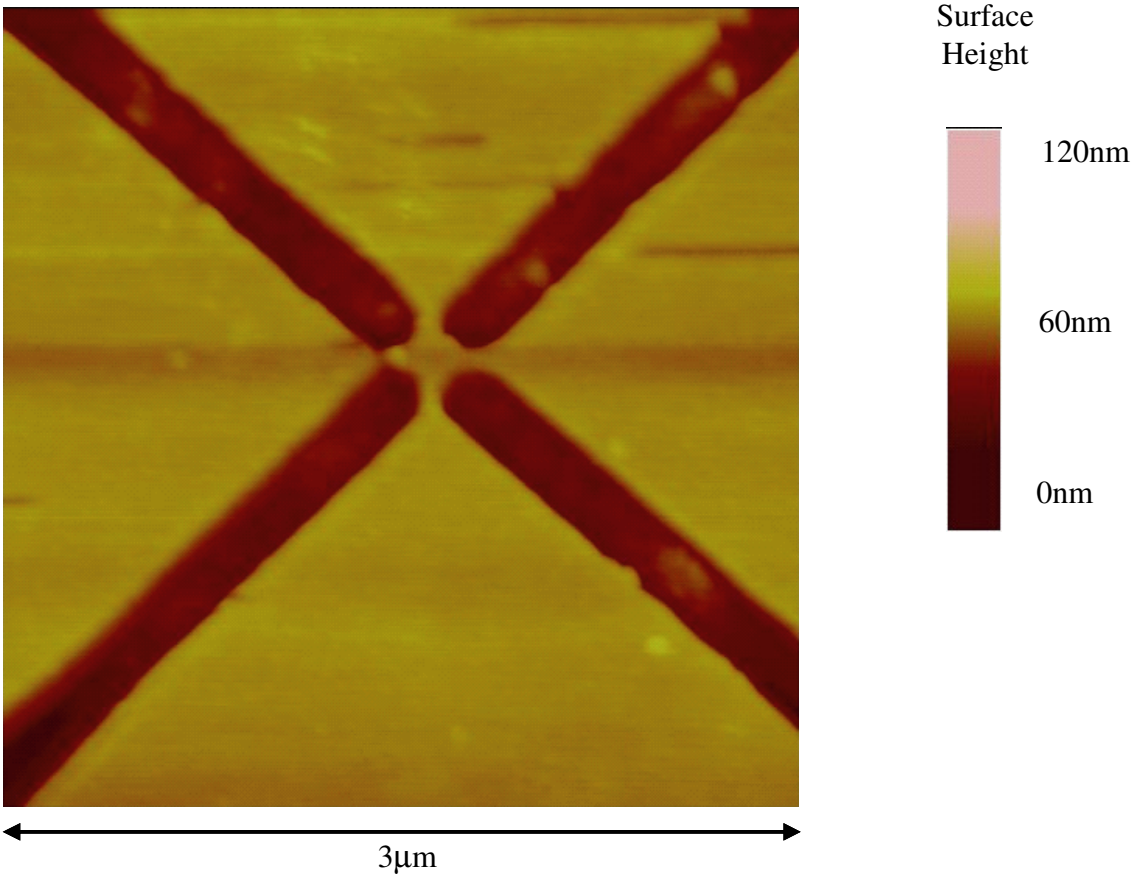


Figure 3.6: Cross junction devices imaged by atomic force microscopy (AFM). The scanning range is 3µm×3µm. The red regions are where InAs quantum well has been removed by lithography and wet etching. The yellow regions contain InAs quantum well populated by 2DEG. The length scale on the side shows the height difference of the red and yellow regions.

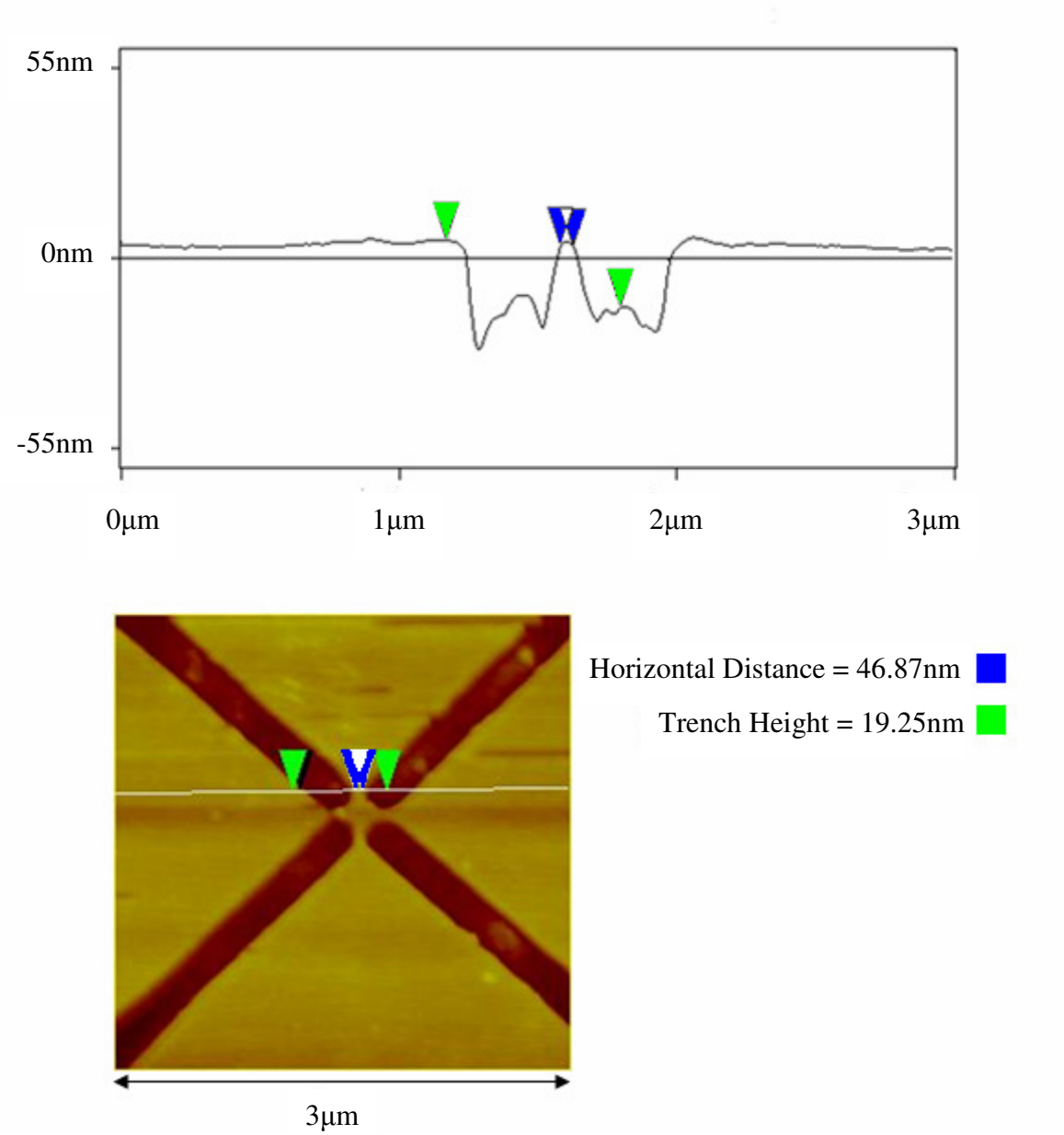


Figure 3.7: (Top) A cross-sectional AFM scan reveals constrictions of approximately 45-50nm width and a total cross junction cavity length of approximately 150nm. The blue triangles represent the horizontal dimension of the InAs constriction, while the green triangles measure the height difference between etched and unetched regions. By Verifying the height is greater than 17nm we can determine that InAs quantum well is totally removed in the red colored regions. (Bottom) AFM image illustrating the location of the cross section analyzed above.

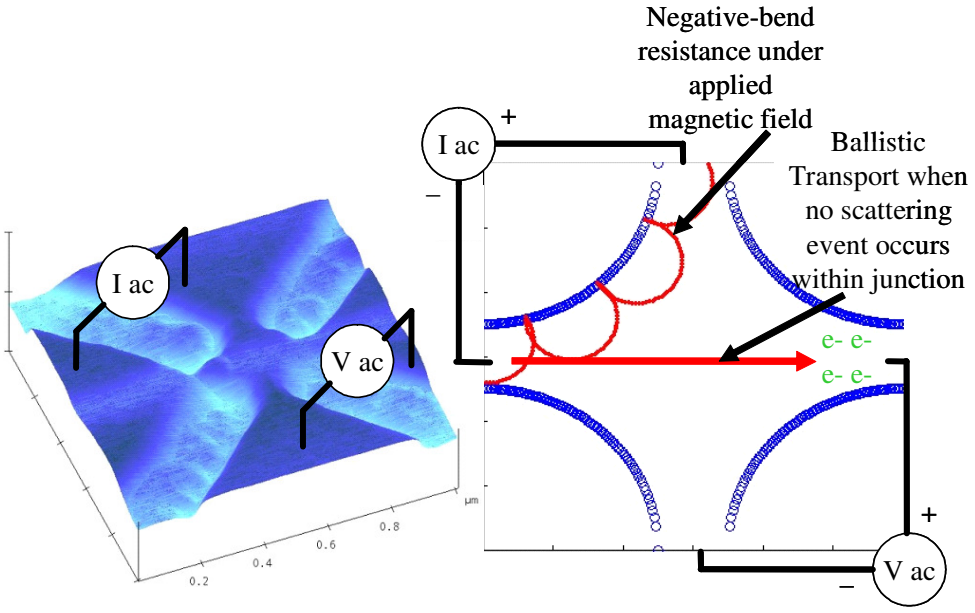


Figure 3.8: The AFM image on the left shows the application of the current source and voltmeter for negative bend resistance measurements on cross junction devices. (Right) Simulation of the negative bend resistance based on a cross junction using a billiard ball model. Transport with and without magnetic field in the cross junction are depicted by the red arrows.

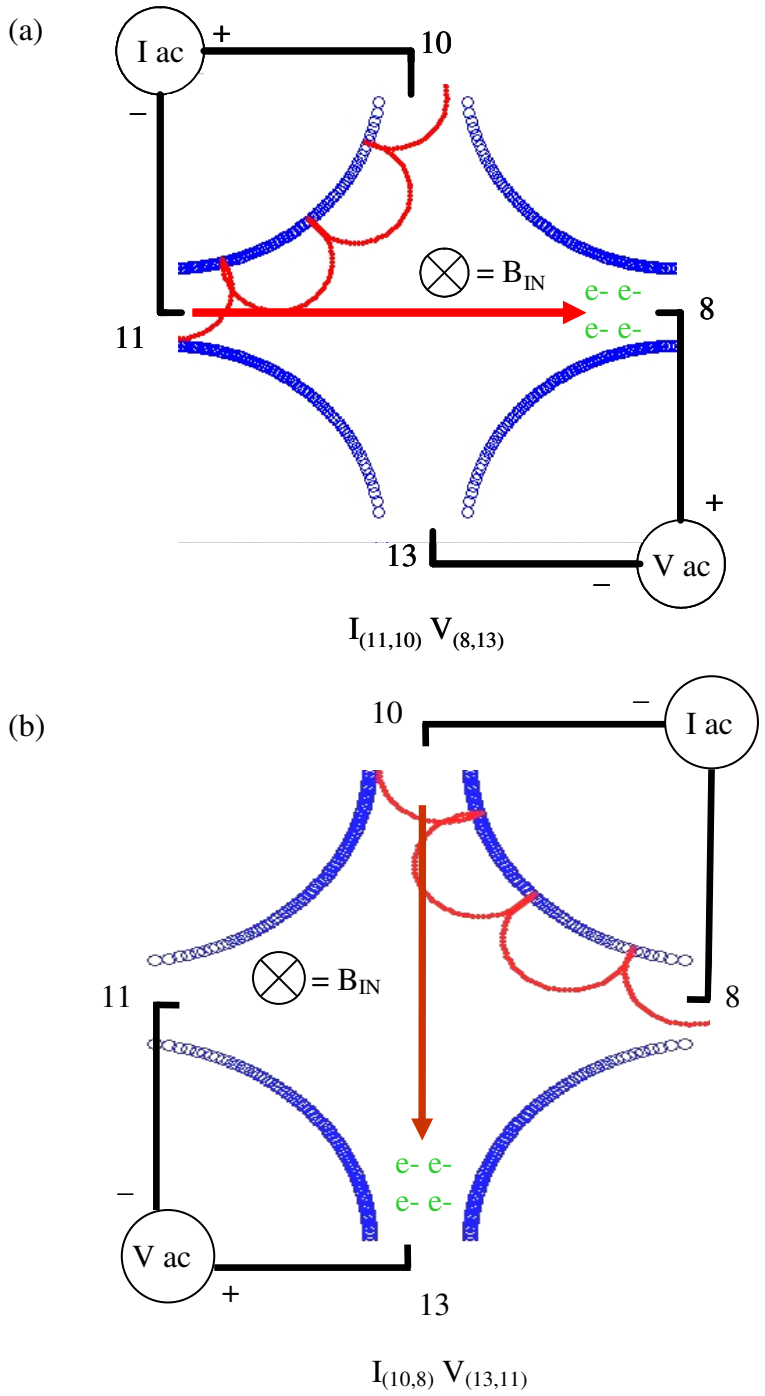


Figure 3.9: Measurement of 300nm cross junction device performed in symmetric manner on different terminals. If ballistic transport occurs in the cross junction, negative voltage should be measured by the lock-in amplifier's differential input with no applied magnetic field regardless of measurement orientation (a) Depicts the device in the I(11,10)V(8,13) measurement configuration. Here the pin numbers refer to the assignment defined in Figure 3.5. (b) Depicts the device in the I(10,8)V(13,11) measurement configuration.

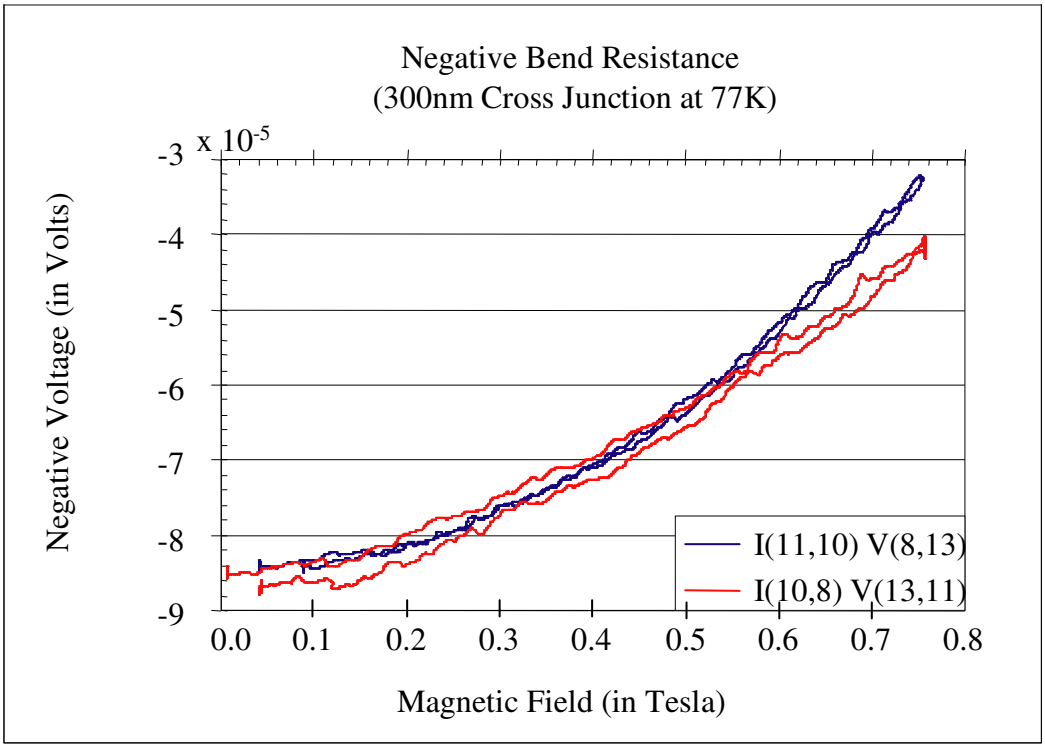


Figure 3.10: Data taken from a 300nm cross junction at 77K. In both of the two different measurement configurations, the cross junction shows ballistic transport which can be destroyed by applying a perpendicular magnetic field.

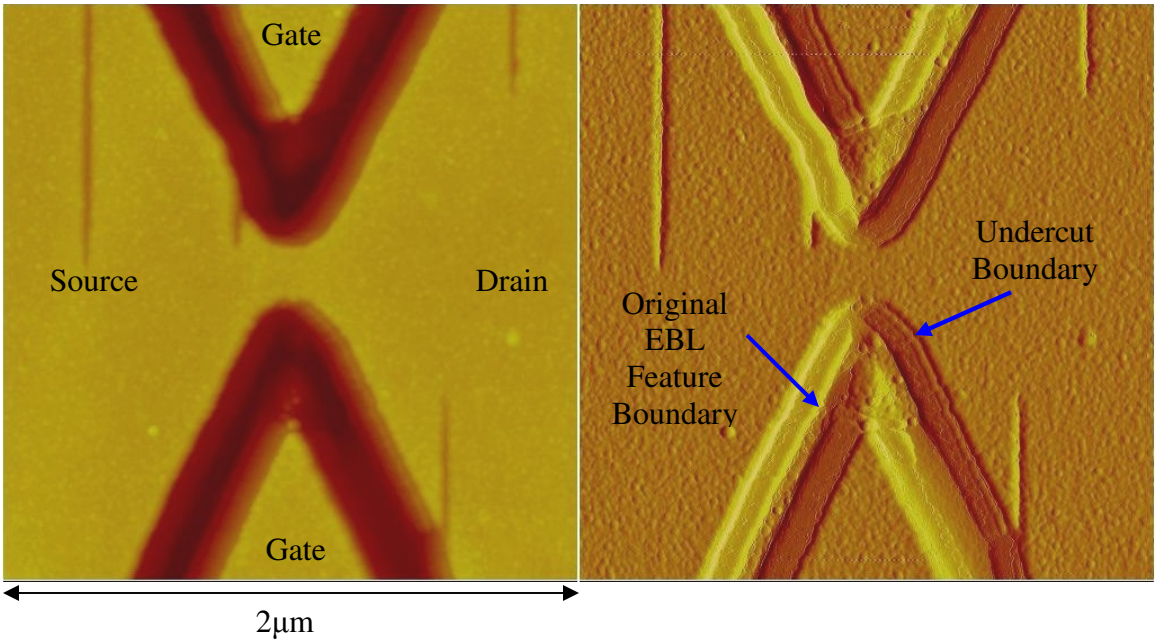


Figure 3.11: AFM image of an InAs quantum point contact. InAs QW has been removed in the red colored regions isolating the gates from the channel. Voltage is applied to the triangular gate regions producing an electric field across the neck of the QPC. Capacitive coupling of the gates to the narrow neck can deplete electrons in the 2DEG between source and drain. In the right window, arrows indicate the boarders of the original EBL defined feature and the undercut region after wet etching.

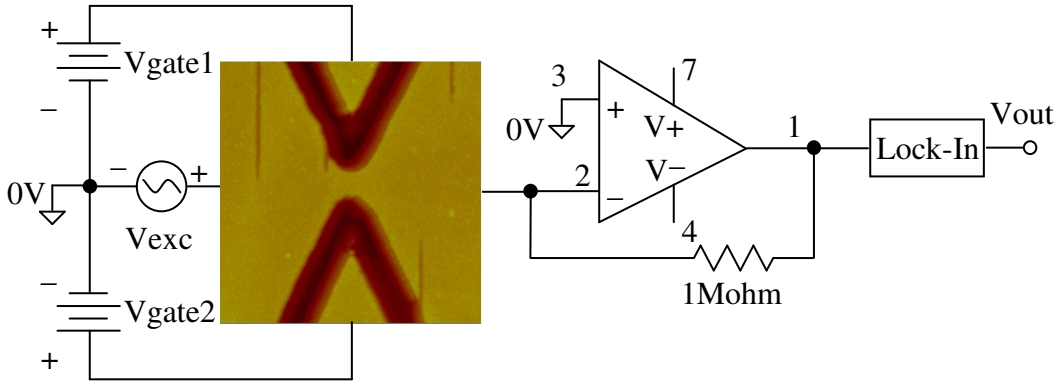


Figure 3.12: QPC Measurement using low excitation measurement where $V_{exc} = 30\mu V_{rms.}$ Gate voltages are applied to the triangular gate regions, electrostatically depleting electrons in the QPC neck. The signal is fed into a homemade transimpedance amplifier with 1 MΩ gain. The amplified signal from the quantum point contact drain is measured by a lock-in amplifier.

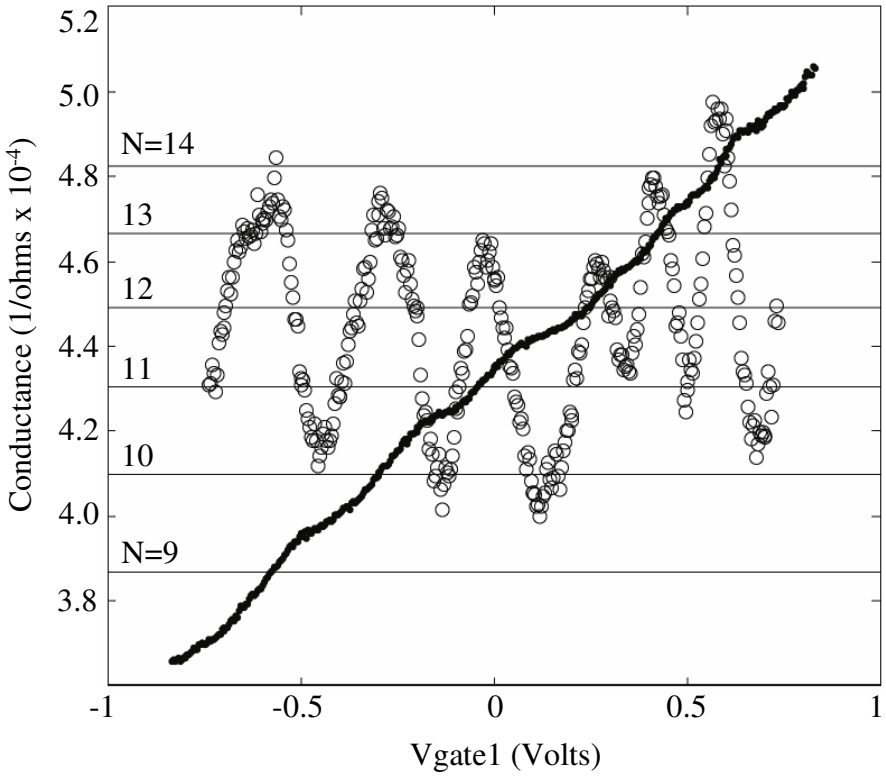


Figure 3.13: InAs QPC 4.2K measurement. Quantum point contacts fabricated in InAs display the expected quantized conductance, verification of one-dimensional ballistic transport in the QPC. Verification of ballistic transport shows that the junction length of the QPC and YBS are shorter than the mean free path l_e. The raw data is shown by the solid black dots and the hollow circles are the numerical derivative of the raw data. The N=9 to N=14 horizontal lines label the expected conductance after taking into account a series resistance G_N.

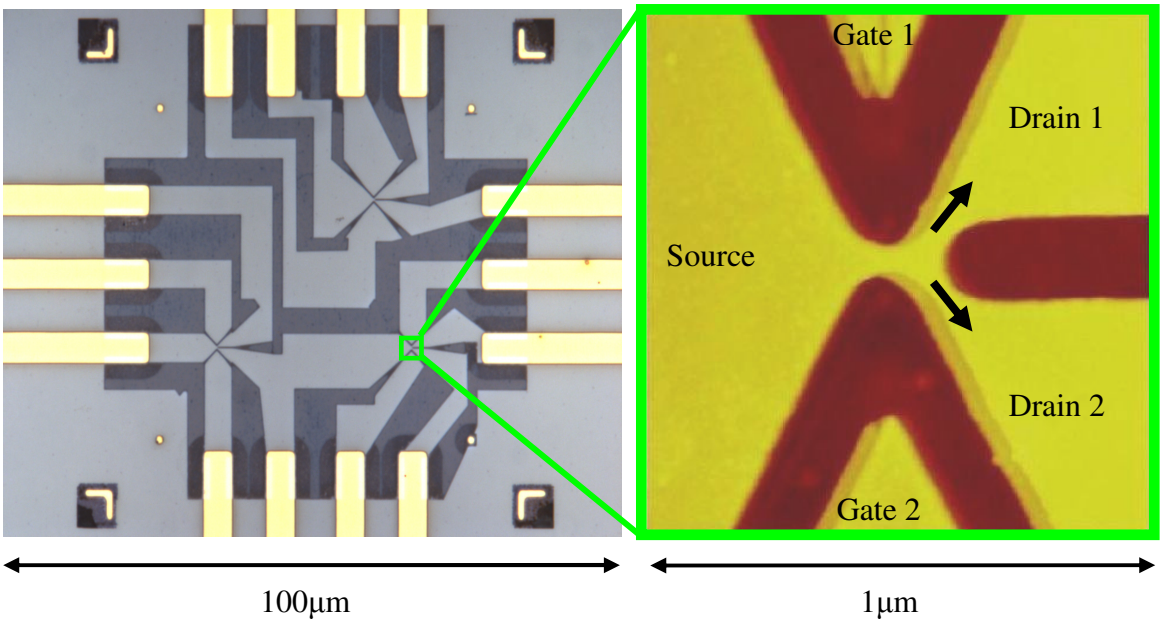


Figure 3.14: Optical microscope image (left) and atomic force micrograph (right) of a finished YBS, where the narrowest neck has a width of 76nm. The dark blue regions (left) and red regions (right) are where the InAs quantum well has been removed by wet etching and the AlSb buffer is revealed. InAs quantum well remains intact in the light blue and yellow regions. The terminals for electrical measurement are labeled.

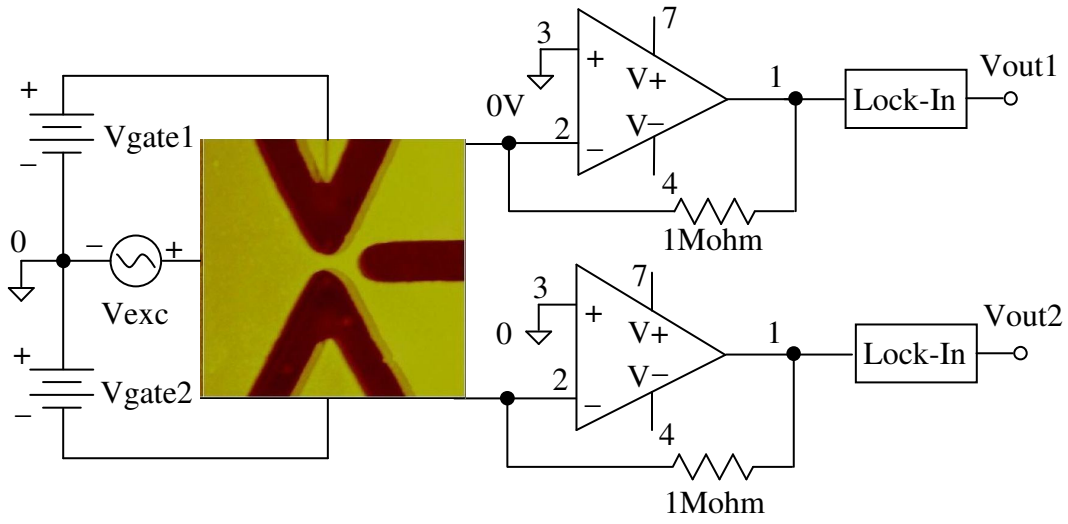


Figure 3.15: YBS Measurement Setup. The drain current from each drain is fed to separate homemade transimpedance amplifiers with input impedance less than 10Ω and a gain of 1MΩ. The ac conductance from both drains is simultaneously recorded by two separate lock-amplifiers as the gate voltage is swept.

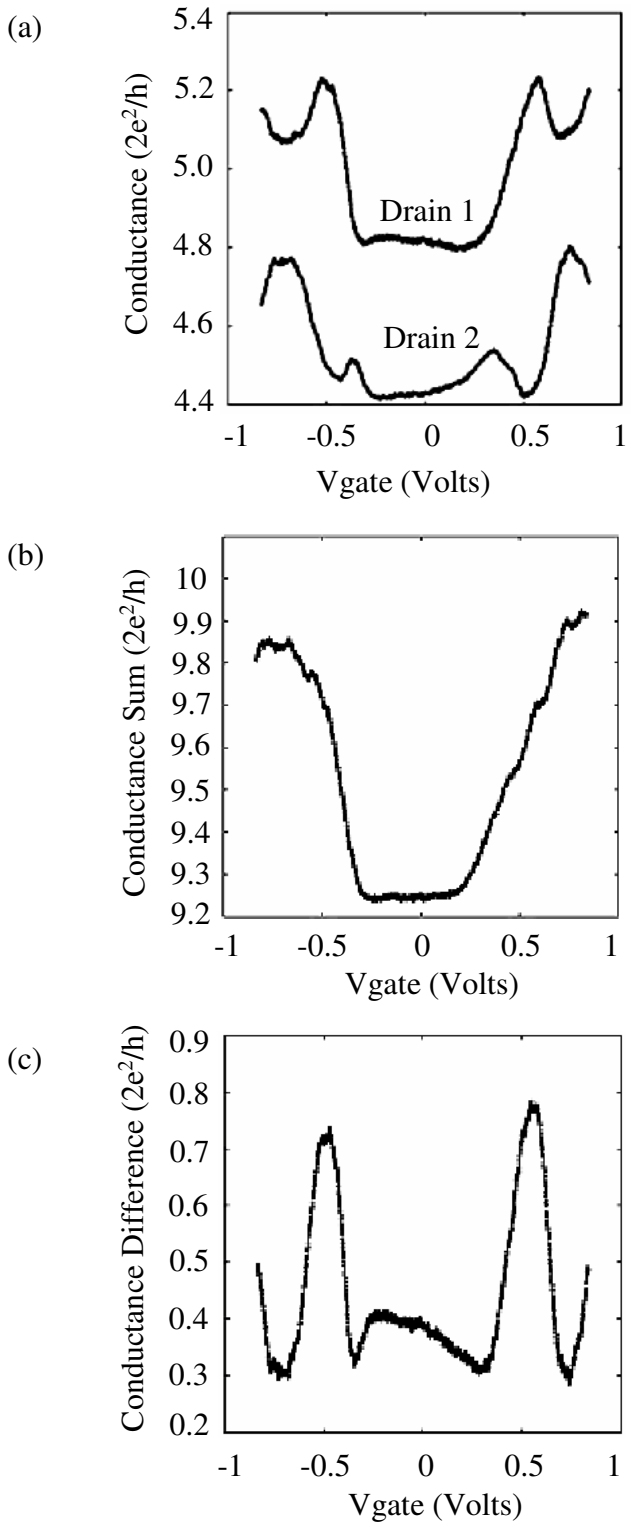


Figure 3.16: Conductance Measurements of the InAs Y-branch switch at 4.2K. (a) The conductance of Drain1 and Drain2 under differential gating. (b) Sum of the conductance of Drain1 and Drain2. (c) Difference between the conductances of Drain1 and Drain2.

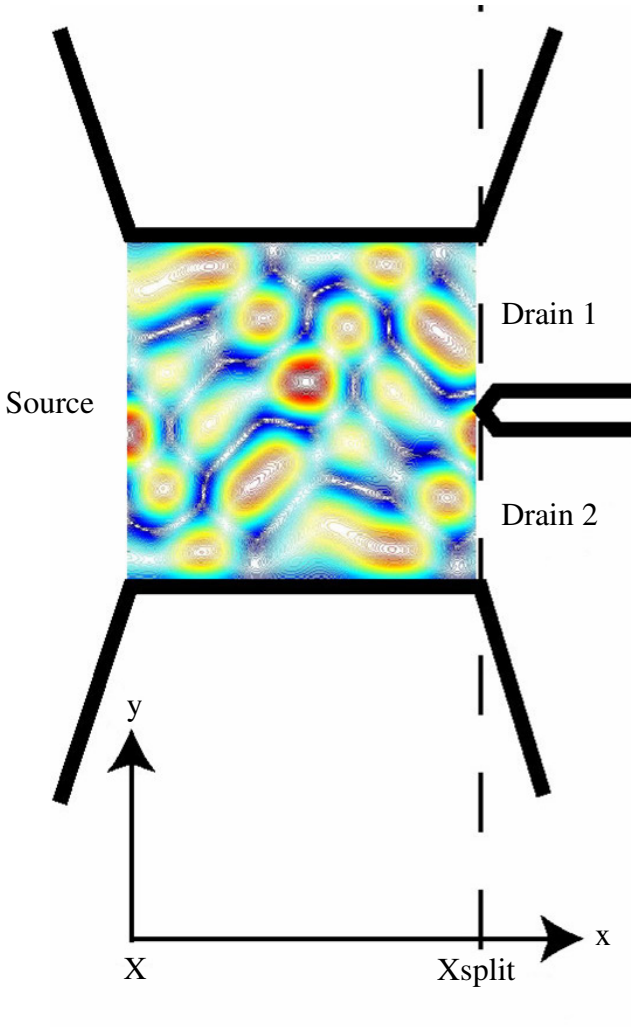


Figure 3.17: Simulation result of a 1D potential with 9 conducting modes of random phase orientation. Dark blue regions indicate areas of low electron density while red regions indicate high electron density. Nodes near the split between Drain 1 and Drain 2 can be coherently steered by applied electric field modifying the conductance to each drain by a value close to the quantum of conductance.

Chapter 4: InAs Single Electron Transistor

Single electron transistors (SET) that were discussed in chapter 2.3 are of interest for downscaling because they dissipate minimal energy. The manipulation of merely one electron is the ultimate downscaling of classical metal-oxide-semiconductor field-effect-transistors (MOSFETs). SETs can sustain size reduction since the Coulomb blockade effect (the SET's basic operating mechanism) is enhanced as the devices are downscaled.[53] Various proposals have been made for the integration of SETs into conventional electronics by using them to form conventional logic gates[9] and memory devices.[18] However, use of SETs to solve the downscaling problem faces two hurdles. The first is that the requirement for using SETs reliably at room temperature demands a SET charging energy of at least $E_C \sim 100 k_B T$,[54] which would require sub-nanometer island fabrication with tight uniformity in the feature size. But, this requirement is beyond the capability of currently available lithographic technology. Even small variations in the island size will result in large variations in the SET threshold voltage. The second difficulty is that SETs are very sensitive to background charges in the substrate. The charging and discharging of electrons from charge traps in proximity to the SET island can generate significant random fluctuation of the SET threshold voltage.

Other non-conventional circuit applications have also been proposed for SETs, such as quantum computation (QC). In a classical computer the basic unit of data, called a "bit," takes the state of either 0 or 1. Data is represented by the state of bits, and data processing is done by binary logic operation of these bits. The quantum computing analogue to the classical bit is referred to as the quantum bit, or, "qubit." The qubit is

defined to be the linear combination of a two level quantum system, as shown in equation 4.1 below:

$$\Psi = \alpha|0\rangle + \beta|1\rangle \ . \qquad (4.1)$$

Unlike a classical bit, the qubit is a superposition of the two states $|0\rangle$ and $|1\rangle$. A quantum computer requires fewer steps to solve certain problems than would be required by a classical computer. Using a quantum computer, a few specific tasks, such as Shor's algorithm for factorization,[55] can be performed with a polynomial number of logic operations. In contrast, using a classical computer to perform the same computation would require an exponentially large number of operations. If the clock frequencies at which these operations are performed are comparable, a quantum computer would obtain the desired solution much faster than a classical one. A quantum computer, if realized, will have significant impact in the area of computer security. Using Shor's algorithm, a quantum computer could promise to make currently available encryption techniques obsolete.

4.1 InAs SET Introduction

Various physical implementations have been proposed for a qubit, such as, electron charge position, flux state, photon circular polarization, ion energy levels, nucleus spin state, and electron spin state.[56] The two Zeeman states of an isolated electron spin in a quantum dot (QD) provide a promising candidate for a qubit,[57] known as a spin qubit. Under magnetic field the spin states of an electron become energy resolved. The two spin states split with a magnitude of $[2s_z(g\mu_B B_z)]$, where s_z is the spin projection in the z-axis, g is the Landé g-factor of the electron in the semiconductor, μ_B is the Bohr

magneton, and B_z is the magnetic field, traditionally assigned to be in the z-direction. (See Figure 4.1) Because SETs can be used to confine and detect one single electron charge, research on spin qubits has focused on fabrication of semiconductor based SETs.

A major challenge for practical quantum computing is scaling quantum systems up to a large number of coupled logical qubits. Solid state implementations of qubits offer the potential advantage of being scalable, and in particular, those based on semiconductors are expected to be conveniently integrated using existing technologies. To demonstrate this possibility, there have been two successful approaches for fabrication of single electron transistors using semiconductors. These two experimental approaches are briefly reviewed below. Both SET approaches reach the one-electron regime by first forming a multi-electron quantum dot and then expelling electrons until a single electron remains.

The first SET approach is a vertical tunneling SET structure.[58] The vertical SET utilizes multiple semiconductor layers to create a dot sandwiched between thin nonconductive layers that act as tunneling barriers. Ohmic contact is made to the top and bottom of the double-barrier tunneling structure. The tunneling probability and dot size are modified by applying voltage to a side-gate (see Figure 4.2). This structure was used to demonstrate a single trapped electron for the first time in history. The primary difficulty vertical dots face is that to perform quantum computing gating operations, there is a need to tune the exchange energy between the two electrons in neighboring quantum dots. But, in these vertical structures, the tunneling barrier is grown by MBE and cannot be physically tuned. To address this issue, fabrication of two laterally-coupled vertical dots is in progress at University of Tokyo and NTT, Japan.[59]

The other popular SET approach uses lateral quantum dots, and it provides a better opportunity for scaling. Spins in lateral QDs in the GaAs/AlGaAs single electron transistors (SETs) have been extensively investigated.[60,61] In the lateral structure, (Figure 4.3) multiple Shottkey gates are placed on the surface of the GaAs/AlGaAs heterostructure. Through electrostatic gating, the single electrons in the QD can be coupled to the 2DEG by two tunneling barriers. A plunger gate is used to electrostatically deplete the SET island, until only a single electron remains. Structures with multiple dots coupled together have also been fabricated, where the exchange energy of two electrons can be modified through electrostatic gating. Considerable progress has been made in SET development as qubits and in performing quantum gating by two coupled qubits.[62,63]

On the other hand, in the case of lateral dot structure, there are complications in verifying the number of electrons in the quantum dot. The current practice calls for the use of an additional quantum point contact (QPC) adjacent to the SET to serve as an electrometer. The transconductance of the QPC is constantly monitored, and a sudden change in the transconductance is used to determine that the number of electrons in the QD has changed by one. This dependence of the transconductance change on gate biases is used as the evidence to identify that only a single electron remains in the dot.[63] The necessity for QPCs to verify the presence of a single electron in lateral SET structures potentially hinders scaling.[64,65,66,8] Furthermore, the GaAs material system is characterized by small energy level spacing and small (−0.44) g-factor. This results in considerable mixing of the electron orbital levels. Finally, the nuclei spin of Ga and As atoms dephase the qubit electron through hyperfine interaction, which in theory is the dominant effect at low temperatures below 100mK. As a result of hyperfine interaction,

the electron coherence time in GaAs is limited to about 1μs.[63,67] In this chapter, we demonstrate a lateral SET in InAs, which based on its quantum well structure, can be operated by a single electrostatic gate and the presence of one electron on the QD can be verified without QPCs.

4.2 InAs Composite Quantum Well

The two previously mentioned successful approaches for fabrication of single electron transistors were performed on GaAs and $In_xGa_{1-x}As$. In contrast, the InAs semiconductor system has material attributes that would be useful for practical implementation of a spin qubit via a SET. InAs quantum dots are characterized by large orbital splitting, therefore, Coulomb blockade effects can be observed at higher temperatures. In addition, for quantum computing, it is particularly important that InAs system has a large g-factor (g-factor ~ −15). With semiconductor quantum dots, qubit manipulation is achieved by application of microwave frequency pulses known as Rabi pulses. The duration of Rabi pulses is controlled by the product of g-factor in the dot and the applied ac magnetic field. Therefore, the 30 times larger g-factor of InAs versus GaAs allows for the use of smaller ac magnetic fields with InAs to achieve an equivalent duration of Rabi oscillations. If smaller magnetic field is required, the integrated wires on the sample that transmit magnetic field will carry smaller ac current, and heat dissipation of the wires into the qubit will be reduced.[68] Minimizing heat dissipation in a quantum computer is of paramount importance because heating could lead to computational errors as heating may cause electron decoherence due to an electron-phonon scattering event.

One common problem with the InAs QW system is gate leakage current, caused by the defects produced during crystal growth. Lattice strain in the InAs system produces defects that propagate from the buffer layer to the surface, providing a leakage path between the quantum well and the Shottkey gates on the surface. However, if the InAs growth is controlled properly, defect count can be minimized to where device gates have a low probability of overlapping a defect. Additionally, our InAs SETs rely on a thermally evaporated SiO_2 layer between the surface $Al_xGa_{1-x}Sb$ dielectric capping layers and gate metal that reduces gate leakage current to negligible levels.

The samples used in this work to demonstrate a SET are InAs/GaSb composite quantum wells (CQWs), a complicated heterostructure system with unique attributes.[69] In this system a thin InAs quantum well layer (4nm) is sandwiched together with a slightly thicker GaSb quantum well layer (16nm) between p-doped $Al_xGa_{1-x}Sb$ insulating layers. The doping can be altered to achieve a specific band bending that facilitates the device operation. Under zero bias the InAs quantum well is free of electrons and the adjacent GaSb layer is populated with 2D holes. The InAs/GaSb heterojunction has a staggered energy band alignment, known as Type II alignment, as shown in Fig. 4.4. By varying the thickness of the InAs and GaSb layers, the CQW effectively becomes a narrow-band gap semiconductor, whose bandgap is tunable by the thicknesses of the two QWs. The effective bandgap is measured from the GaSb valence band minimum to the InAs conduction band minimum. As the thickness of the InAs quantum well is reduced, the quantized energies in the InAs QW are increased, increasing the conduction band minimum of the InAs layer. The result is an increase in the effective bandgap of the

CQW. The specific CQW wafer that we used for fabrication has an effective bandgap of approximately 100meV.

The InAs CQW can be lithographically patterned into one-dimensional and zero-dimensional systems with arbitrary geometry. Wet etching is used to remove the InAs and GaSb quantum well layers to create sidewall potential barriers. Either side-gates or top-gates can be applied to create tunable electrostatic confinement and to vary the quantum dot's energy levels and tunnel couplings.

Figure 4.5 shows the schematic of a generic transistor fabricated using the InAs CQW system. A top-gate is defined on the CQW surface that when biased with a voltage (V_{gate}), controls the carrier population, as well as the type of carriers, in the CQW. At $V_{gate} = 0$, the transistor conducts via the 2D holes in the GaSb layer. As the top-gate is biased to be more positive, the 2D holes in the GaSb QW are gradually depleted until no carriers remain. Further increase of the top-gate bias results in the formation of 2DEG in the InAs layer. The following section presents experimental evidence of the transition from 2D hole accumulation, through hole depletion while electrons are still depleted in the InAs layer, to 2D electron inversion in the InAs QW.

4.3 InAs Hall Bar

The growth parameters such as doping concentration and layer thickness of the CQW were optimized to achieve the proper band bending necessary for successful fabrication of SETs. The first step in this optimization process was to model the CQW self-consistent band bend bending using various combinations of layer thickness and doping profiles. Using the simulation as a starting point, many different wafers were

grown, each with slightly different quantum well thickness and doping profiles, then tested to find the a wafer with optimum properties for fabrication of SETs. These properties include high-mobility low-resistivity 2D carriers, low defect count, formation of low resistance ohmic contacts without high temperature annealing, and gateability. All of these qualities were verified by fabricating Hall bars on a piece of each different CQW wafer, then the wafer whose properties were judged to be closest to ideal was selected for SET fabrication. Most of the wafers that we tested failed in one or several of these areas. Some formed high quality 2D layers but had very large contact resistance. Others could not be gated to form electrons in the InAs layer. Some even had carriers in both quantum wells under no externally applied gate bias. Once a suitable wafer is found, many devices can be fabricated from one wafer, and many transistors made from the same fabrication run should exhibit similar transport characteristics.

Figure 4.6 shows an optical microscope picture of one of the working Hall bars. Using photolithography, a Hall bar mesa with 10μm channel width and 100 μm channel length was defined on the CQW. The field (darker blue rough area) was wet etched away using a four layer selective wet etch to remove both the InAs and GaSb quantum wells. Again using photolithography, a metal gate was deposited over the Hall bar channel. To reduce gate leakage current between the InAs surface and metal gate, a 100nm thick layer of SiO_2 was thermally evaporated. Finally the first two layers of InAs were removed at the bonding pad areas of the Hall bar mesa and a Titanium/Gold layer was evaporated directly onto the InAs quantum well for ohmic contact. The dc current-voltage characteristics of the Hall bars were measured at 4.2K in the common-source configuration. Figure 4.7, shows the I-V characteristics of one of the successful Hall bars.

Inset is a schematic showing the potential profiles along the source-drain direction for the three operating regimes. As expected, the Hall bar conductance is found to be large when there are either 2D electrons or 2D holes in the CQW under the gate area. When both quantum wells are depleted, conductance is low because there are no carriers in the Hall bar channel. Both the gate leakage current and the drain current in the depletion region are less than the measurement resolution (0.1pA) during device operation.

The basic operating principle of the InAs SET relies on gating the composite QW system from hole accumulation into electron inversion. With the operating principle verified by Hall bar measurements, we can shrink the device's lateral dimensions and fabricate single electron transistors. In the next section, I will discuss the structure and expected transport characteristics of single electron transistors made of the InAs/GaSb composite quantum wells.

4.4 InAs SET Structure

In contrast to the previously discussed depletion-mode lateral[60 above] and the vertical[64] SETs, where both types reach the one-electron regime by expelling electrons from multi-electron QDs, our "enhancement-mode" SET takes the opposite approach. The concentration of electrons in the CQW can in principle be controlled through electrostatic gating to be arbitrarily small. By fabricating a single gate with small enough dimensions, we ought to be able to form a quantum dot with just one electron under the gate. The operating procedure is described below. Initially, an empty QD is formed by electrostatically gating a region of semiconductor that contains no electrons. As the gate voltage is increased the band bending causes potential barriers to form. As the band

bending increases further, 0D energy states begin to develop between the potential barriers that electrons can tunnel into one by one. We utilize this design concept to fabricate an InAs SET.

Figure 4.8 shows a schematic of the proposed InAs SET. Using electron beam lithography and wet etching, we fabricate a mesa with a narrow neck between the source and the drain ohmic contacts. In comparison with the lateral GaAs approach which uses multiple gates, our SET structure uses a single top-gate to create two symmetric tunnel barriers where electrons tunnel into the empty QD one at a time. The gate is fabricated over the narrowest portion of the neck so that a combination of the quantum well confinement, electrostatic tunnel barriers, and neck constriction, restrict the electrons in the quantum dot in all three dimensions.

The next section discusses simulation of the InAs quantum dot. These simulations were performed to investigate how design parameters such as gate size and dielectric thickness affect the electrostatic confinement of electrons for our device. The simulation is used to verify that the one-electron state could be formed and populated by a gate size within our lithographic capability.

4.5 MIS Simulation

It is critical to the operation of an SET that when the quantum dot potential forms the first 0D electron state that the tunneling barriers be thin enough to allow electrons to tunnel into the quantum dot. To this end, our group member Binhui Hu has performed numerical simulation to help us estimate how the shape of the confining potential and tunneling barrier thickness vary as a function of the gate size. These simulations also

produce an estimate of the proper gate voltage range for our SET. The model structure, as depicted in the left inset of Figure 4.9, is a standard MIS capacitor, but the gate here is chosen to be a small metallic cylinder with a diameter (D) of 50, 70 or 100 nanometers. In a conventional MIS capacitor with a p-type semiconductor, a gate bias can change the system from an accumulation of holes to an inversion layer of electrons.[3] With a nanoscale gate area, the inversion electrons will reside in a quantum dot directly below the gate.

For a particular V_{gate}, we solve the Poisson equation:

$$\nabla^2(x, y, z) = \frac{\rho(x, y, z)}{\varepsilon(x, y, z)} \qquad (4.2)$$

where $\varepsilon(x, y, z)$ is the local dielectric constant and $\rho(x, y, z)$ is the net charge, including the free holes, free electrons, and the ionized acceptors. The solution is the potential $V(x, y, z)$ as a function of V_{gate}. The solution is obtained numerically using Femlab, a Matlab-based software that solves three-dimensional electrostatic problems based on the defined geometry, boundary conditions and material parameters. Further details of the simulation can be found elsewhere,[70] where the specific dielectric constants have been modified to model this system. The right inset of Fig. 4.9 shows an example of the simulation assuming an effective CQW bandgap of 100meV and a 2D hole density of 1×10^{12} cm^{-2} in the GaSb layer.

We find that for a smaller gate diameter, the confinement potential is steeper and the size-quantization energies are larger, although it takes a higher gate voltage to induce the first available electron energy state. For example, when a single electron resides in the QD, the quantization energy is 13meV, 15meV and 17meV, for D = 100nm, 75nm and 50nm, respectively. (See Figure 4.10) The 50nm gate width is the minimum feature size

within our lithographic capabilities so we did not model smaller dots. However, based on the results, we should be able to engineer different quantization energies by varying the gate width.

Another key operating principle, substantiated through the simulation, is that the transmission coefficient of this band-to-band tunneling barrier is not sensitive to the top-gate bias for the first few electrons, as illustrated in Figure 4.9. The height and width of the tunneling barrier are primarily dependent on the bandgap of CQW and 2D hole density, respectively. The difference in gate voltage necessary to change the electron population by a few electrons produces little change in the band bending. In other words, the tunneling transmission coefficient in enhancement-mode QDs is determined primarily by the potential profile of the heterostructure, similar to the depletion-mode vertical QDs. Since numerical modeling shows that the tunneling barriers that define a QD are, to the first order, insensitive to variation in the top-gate voltage in the few-electron regime, it is possible to identify the first electron state purely from the conductance measurement. No additional quantum point contacts are necessary to verify the single electron regime.

4.6 InAs SET Fabrication

For the fabrication of SETs, we have used electron-beam lithography and wet etching to fabricate transistors with a gate length down to a few tens of nanometers. A detailed process sheet can be found in Appendix B. This section will serve to highlight the fabrication issues specific to the InAs SET that were vitally important in fabricating a successful device.

Because the Fermi level is pinned above the conduction band in n-type InAs, edge depletion does not develop at lithographically defined boundaries and is not usually a concern with InAs devices. However, like GaAs, edge depletion does form in the GaSb QW at lithographically defined boundaries. Since the magnitude of edge depletion varies with the growth parameters, it will vary with each individual CQW wafer and must be determined. Therefore we must account for this edge depletion in our SET design.

The SET design calls for a mesa etch with a narrow neck at the point where the gate induces electrons. The narrowing of the neck restricts the size of the quantum dot in the transverse dimension. If the restriction is made too narrow, the entire area under the gate will be depleted due to edge depletion. If the restriction is made too wide, then the dot will be large and asymmetric. We prefer for the dot to be as small as possible because the spacing of the energy levels in the dot is inversely proportional to the dot size. Large spacing is preferable since it allows for higher temperature operation as well as well as increasing coherence time due to the reduction of electron-nucleus spin hyperfine coupling. To find the optimum neck width, transistors were fabricated by performing a mesa etch where various channel widths were wet etched into narrow necks between source and drain ohmic contacts. When the channel width was reduced to approximately 700nm, devices show a complete depletion of 2D holes, indicating a surface depletion of 350nm at the sidewall in the GaSb layer. See Figure 4.8.

Although the optimum neck width was determined, obtaining the optimum neck width consistently was still challenging. Etching off the cap layers produced etching downward as well as laterally underneath the resist. This undercutting caused the dimensions of the neck to be reduced from those that we lithographically defined.

Therefore, the neck width had to be programmed to be larger than the intended result. The etchant was mixed fresh before every step to ensure that the H_2O_2 in the mixture did not evaporate changing the etch rate. Mixture of the wet etchant had to be precisely controlled, down to the drop of acid and base, otherwise the etching rate could vary significantly. It was also crucial that the etch times were strictly adhered to since the variation by even a half-second could have a compounding effect over 4 layers, significantly changing the neck width. Since no etch barrier existed below the fourth layer, the last step in the mesa etch had to be implemented with exact timing so that the field did not become etched too deeply, otherwise our evaporated gate would not climb up onto the mesa in one continuous film. Maintaining a continuous gate was of the utmost importance, thus controlling the depth was the primary concern. Therefore in each run, three different neck widths were programmed with the hope that one would be of optimum width when the mesa etch was complete.

Early on, ohmic contacts were fabricated by wet etching off the top two cap layers so that thermally evaporated metal could be deposited directly on top of the InAs quantum well layer. Ohmic contacts were fabricated as close to the neck of the transistor as possible in order to theoretically reduce the series resistance in the device. The ohmic contact layer also faced problems due to wet etching undercut. Since the same mask was used for the wet etch and metal evaporation, a small band around the edge of the feature developed where wet etching occurred but no metal was deposited. We believe that this narrow band contributed to an increased series resistance. The ohmic contact step was removed from the process when it was determined that a comparable quality ohmic

contact could be achieved simply by hand soldering indium to the source and drain leads, puncturing the top two layers and directly contacting the InAs QW.

After mesa etch, small metal gates were fabricated over the narrowest portion of the neck between the source and the drain. To solve the leakage problem of the dielectric top layers in the InAs composite quantum well, the smallest overlap possible was used to minimize the possibility that the gate lay on top of a defect. Also a thermally evaporated dielectric layer of SiO_2 was deposited between the composite quantum well surface and the gate metal to ensure dc leakage current could be eliminated. The maximum thickness of thermally evaporated SiO_2 could only be 100nm, or strain in the film would cause the dielectric to become cracked and to leak under applied bias. Also, thermally evaporated oxide deposits with a solid angle rather than conformally. Therefore, it was necessary to maintain a height difference between the mesa and the field of less than 100nm, otherwise the oxide film would not isolate the gate metal from the channel. The gate was patterned to extend over the SET neck and onto the field on the opposite side to anchor the fragile gate from being ripped off during liftoff and future processing steps.

Initially, SETs did not operate as expected. Leakage between source, the drain, and the gate as well as between devices was observed by dc measurement at 4.2K. The Hall bar demonstrated that with proper design, leakage could be eliminated. The primary structural difference between the Hall bar and the original SET design was in the field. With the Hall bar, the CQW field had been removed before the gate had been added to the device. Removing the field prior to the deposition of the gate pads reduced the SET leakage to below 0.1 pA, as well as fully electrically insulating each device from its neighbors. Once this problem was resolved devices began to operate as expected.

Figure 4.11 shows a completed die, hosting 6 SETs. Each die has 14 metal bonding pad leads. Typically 12 such die's were fabricated during each week long processing run. Figure 4.12 shows a close-up view of one transistor with a final channel width of roughly 1 micron. It is clear from this image that the gate metal is continuous as it climbs up from the mesa-etched region over the neck of the SET. This device was patterned before the ohmic contact step was removed and a clear sideband can be seen around the ohmic contact metal as was described in the processing steps.

4.7 InAs SET Characterization at 4.2K

Following fabrication, transistors were characterized through low temperature electrical transport. Data taken from one transistor that shows typical results is presented here. At 4.2K the SETs display the expected Coulomb blockade. Figure 4.13 shows the data taken at 4.2K, where the dc drain current is measured at a fixed drain voltage of 1mV. At $V_{gate} = 0$, the system is in the accumulation regime, and the transistor shows ohmic conductance via 2D holes under the gate. As the gate voltage increases, the drain current drops because the transistor goes from accumulation to the depletion regime. In the depletion regime, the drain current is smaller than our noise floor of roughly 0.1pA.

When the gate voltage bias is increased further to 6.2V, the lowest single electron quantum state beneath the gated region is aligned with the Fermi level, resulting in a current peak. As the gate voltage becomes more positive, the current peaks due to the second and the third electron occupation are observed near $V_{gate} = 7.0$ V and 8.4 V, respectively. It is important to note that the peak heights occur with roughly the same order of magnitude for the first three peaks indicating that the amplitude of conductance

is of a similar order of magnitude. Since the conductance is a strong function of the tunneling barrier thickness, this observation proves the assertion made by simulation that the tunneling barrier thickness is only a weak function of the gate voltage. Further more it proves that the first peak is indeed the addition of the first electron.

To investigate the operation of this enhancement mode InAs SET further, we have carried out the standard stability measurement: the drain current is measured as a function of a stepping gate voltage and a sweeping drain bias. Fig. 4.14 shows the contour plot of the drain current using linear scale. As a manifestation of single electron transport in the Coulomb blockade regime, the contour plot shows a series of diamond-shaped blocks. The dashed lines highlight the boundaries of the blocks and are labeled by N = 0, 1, 2, 3, and 4, referring to the number of electrons in the QD.

According to the "orthodox" theory[71] of the Coulomb blockade, the height (e/C_Σ), the width (e/C_{gate}), and the slopes defining the diamond (C_{gate}/C_{drain} and $-C_{gate}/C_{source}$) uniquely determine the SET charging energy. Applying this standard analysis procedure, we have calculated for the capacitances and addition energies of the 1st, the 2nd, and the 4th diamonds, as listed in Table 4.1. We obtained an addition energy of 15meV for the first block, 35 meV for the 2nd, indicating that the level spacing due to size quantization effect is 20 meV. Compared to our potential simulation, the obtained quantization energy implies a QD less than 50nm in diameter. If we model the QD as a disc with a radius r, the obtained capacitance of our QD suggests an effective diameter of about 20nm. Here, we use $C_\Sigma = 8\varepsilon r$ and the dielectric constant of InAs ε=12.3. We notice that the 3rd diamond contains several spikes. We attribute them to single electron traps in the vicinity of SET that happen to be activated under specific operating conditions. The size of the

3rd diamond should therefore be smaller than the apparent result shown in Fig. 4.14. For that reason we have not calculated for its charging energy in Table 4.1.

4.8 InAs SET Analysis

The observations of relatively large Coulomb and size-quantization energies are significant. The criteria for observing single electron tunneling characteristics are that the Coulomb energy (e^2/C_Σ) be larger than the thermal energy (k_BT), and that the tunneling conductance be smaller than the conductance quantum e^2/h. Consequently, SETs in the many-electron regime have been demonstrated in a variety of systems, including $In_xGa_{1-x}As$, GaAs, Si, carbon nanotubes, and metal-based structures. However, the experimental requirement is more stringent for observing the size quantization effect, due to two additional criteria: the Fermi wavelength should be comparable to the island's size, and the system should be in the few-electron regime. Thus far, depletion-mode lateral and vertical SETs were the only two systems reported that had shown size-quantization effects, and the reported values were typically a few meV.

Larger quantization energy allows for SET operation at a higher temperature, as evident from 4.2K operating temperature of our SET versus 10-50mK in depletion-mode SETs.[61,62,63,64] Larger quantization energy is also important for quantum computing from the vantage point of spin decoherence. The most important factor in the decoherence mechanisms is the admixture of electron states due to spin-orbit interactions. Such admixture is reduced as a result of large orbital level energy spacing, mainly removing the effect of strong spin-orbit interaction in InAs. Furthermore, other effects related to admixture of the excited electron levels, including their virtual occupation by other

electrons, are also suppressed, making the ground state of InAs quantum dot close to an ideal two-level system. The observed large quantization energy is due to a combination of the small electron effective mass in InAs and a steep confinement potential resulting from the band-to-band tunneling design. We note that the steep confinement potential also makes it possible to place QDs in close proximity needed for stronger exchange coupling between dots and for constructing an array of QDs capable of transporting qubits via the paths of empty QDs.

4.9 InAs SET Conclusion

In conclusion, we have proposed an enhancement-mode SET and demonstrated it using InAs/GaSb composite QW. The CQW effectively produces a QW with a narrow tunable bandgap. By patterning small transistors with a single gate, we achieved the one-electron regime in a 20nm InAs quantum dot with an orbital energy spacing of 20meV. This approach combines the advantages of the previous lateral and vertical SET structures, and is advantageous for applications in quantum information technology because it includes lateral configuration, a single top-gate design, steep potential confinement, large g-factor, and a significant reduction in device heating. Furthermore, we proved through simulation and experimental data that the identification of a single electron can be achieved without independent charge sensors located near the quantum dot reducing fabrication complexity, and producing stronger exchange coupling between the dots through increased packing density.

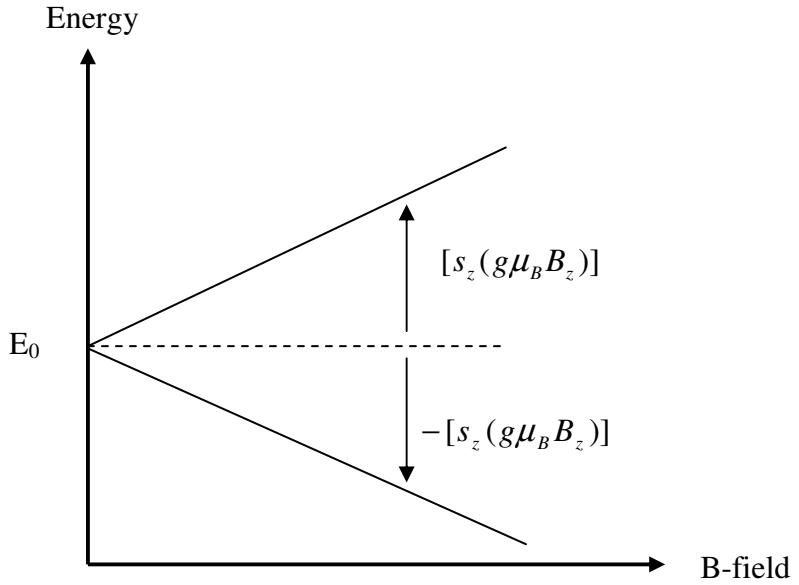


Figure 4.1: Zeeman splitting of the E_0 electron energy state in the z-subband under magnetic field. The two Zeeman states of an isolated electron spin in a quantum dot (QD) provide a promising candidate for a qubit. Under magnetic field the spin states of an electron become energy resolved. The two spin states split with a magnitude of $[2s_z(g\mu_B B)]$, where s_z is the spin projection in the z-axis, g is the Landé g-factor of the electron in the semiconductor, μ_B is the Bohr magneton, and B_z is the magnetic field, traditionally assigned to be in the z-direction.

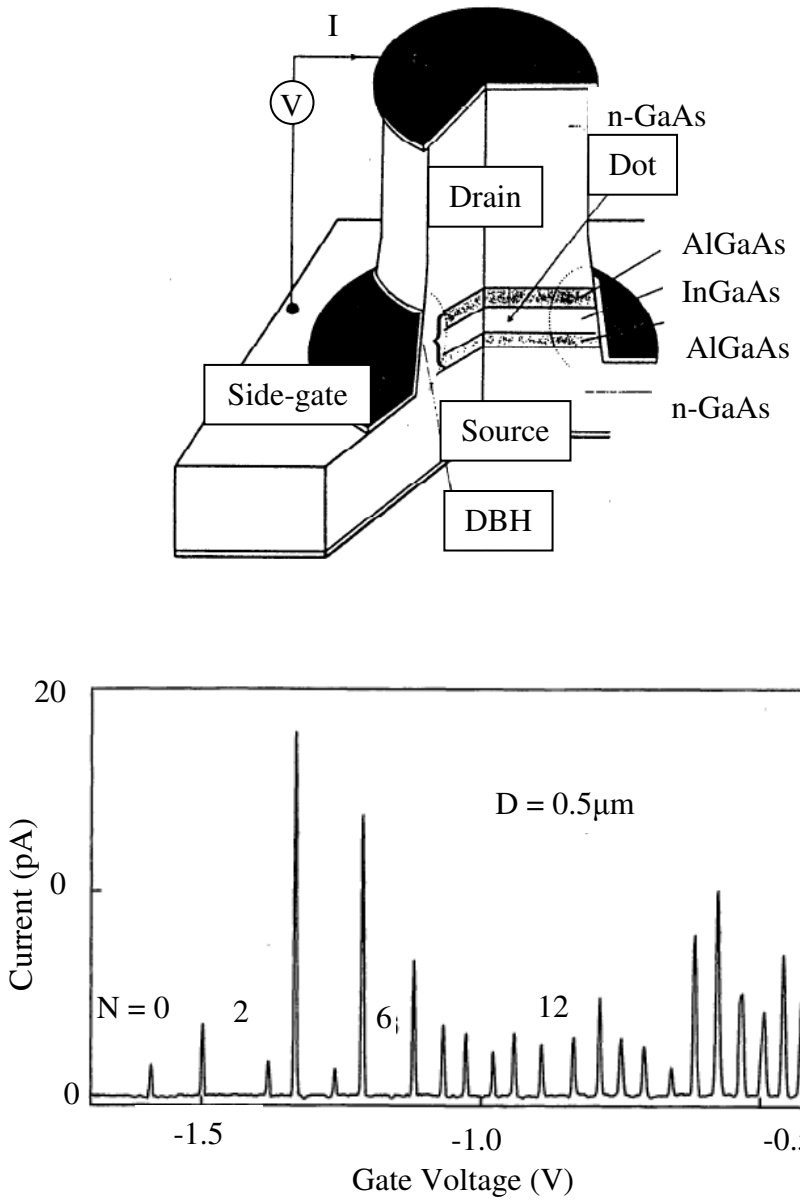


Figure 4.2: Vertical Tunneling SET structure (top) and data taken from a device (bottom) of this structure.[59] Here N is the number of electrons trapped on the SET island and D is the pillar diameter. This work performed by Tarucha et al., demonstrated single electron trapping for the first time. Because the tunneling barriers are fixed, the single electron state can be identified without external quantum point contacts. However fixed barriers pose difficulties for using this structure in a quantum computer.

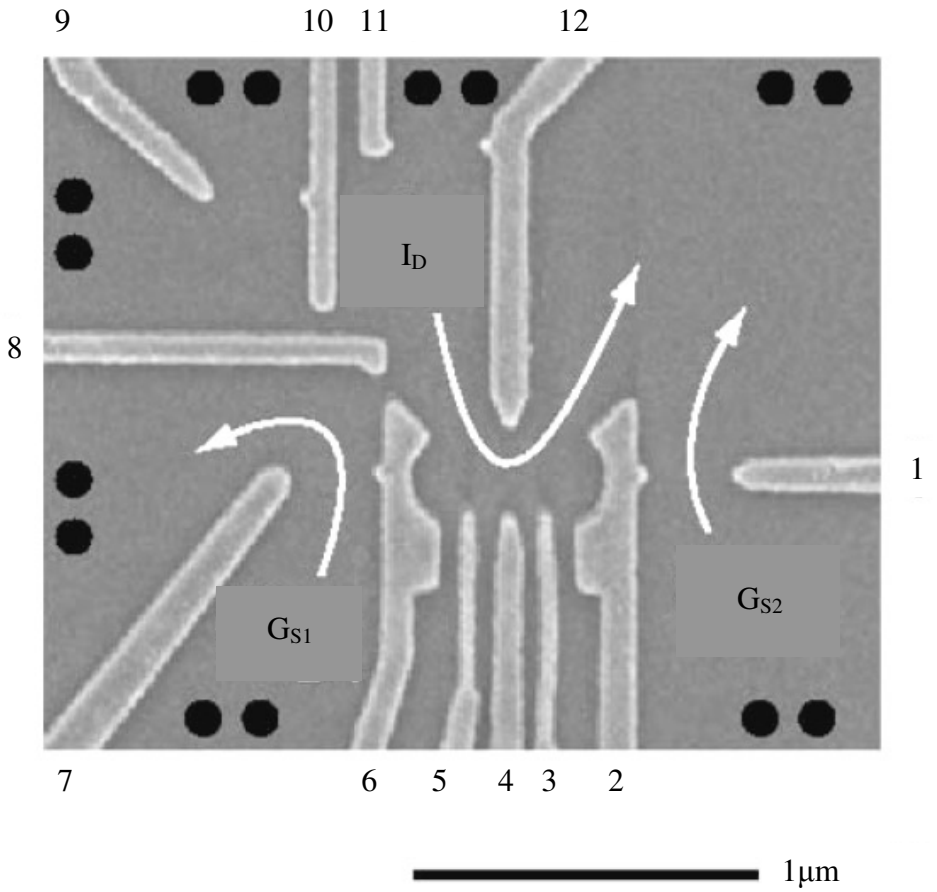


Figure 4.3: SEM micrograph of a lateral double-dot SET in GaAs. To date this work by Marcus et al., represents the state of the art in semiconductor qubit experimental achievements. The light grey features are metal gates used to deplete electrons in the 2DEG. Note the large amount of area as well as the large number of metal leads (12 total for this particular device) are necessary to fully control two individual electron spins in space. Gates 7 and 1 are used to form the QPC necessary for sensing the presence of individual charges in the left and right sides of the double quantum dot.

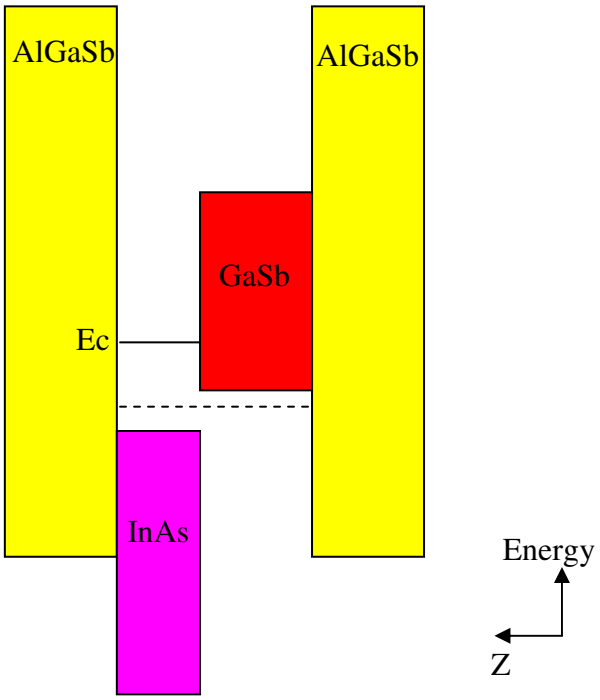


Figure 4.4: Energy band diagram of the composite quantum well. In this system a thin InAs quantum well layer (4nm) is sandwiched together with a slightly thicker GaSb quantum well layer (16nm) between p-doped $Al_xGa_{1-x}Sb$ insulating layers. The doping can be altered to achieve a specific band bending that facilitates the device operation. Under zero bias the InAs quantum well is free of electrons and the adjacent GaSb layer is populated with 2D holes. The InAs/GaSb heterojunction has a staggered energy band alignment, known as Type II alignment. By varying the thickness of the InAs and GaSb layers, the CQW effectively becomes a narrow-bandgap semiconductor, whose bandgap is tunable by the thicknesses of the two QWs. The specific wafer CQW that we used for fabrication has an effective bandgap of approximately 100meV.

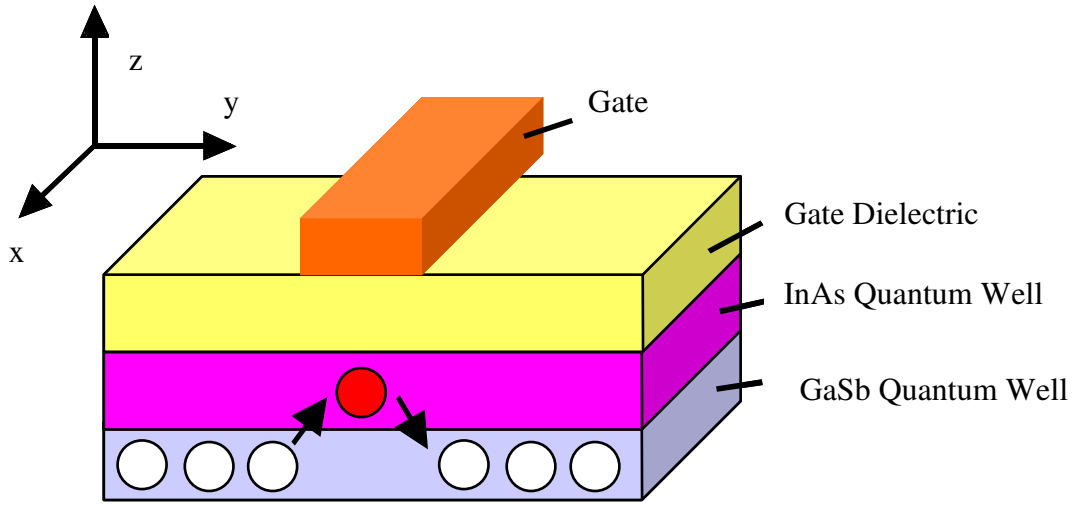


Figure 4.5: Schematic of the enhancement-mode single electron transistor, where one electron is induced in the InAs layer by a top metal gate. By applying positive voltage to the top-gate holes in the GaSb layer, represented by the white circles, are depleted. Upon further application of voltage the conduction band of the InAs layer is bent below the Fermi level allowing electrons to populate the InAs layer under the gate. Electrons tunnel from the GaAs layer into the InAs layer through the band gap between the InAs conduction band and the GaSb valence band.

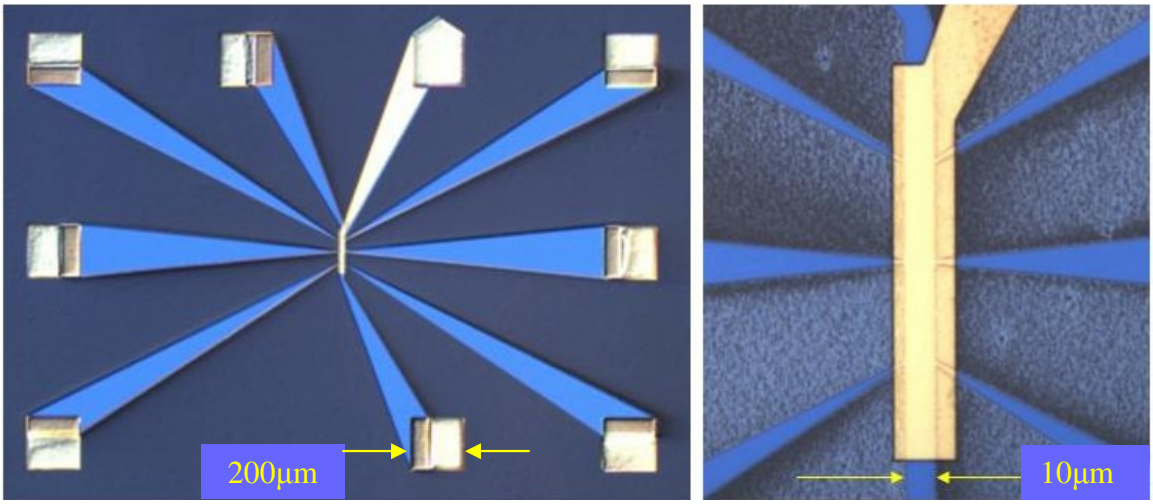


Figure 4.6: Optical microscope images of a 10µm wide InAs Hall bar at various magnifications. The light blue area is where InAs quantum well remains while the rougher dark blue region is where the quantum well has been wet etched off. InAs Hall bars were used to test the operating principle of SETs on a micrometer scale and was used to select the most favorable CQW wafer for InAs SET fabrication. The length scales in both pictures are symmetric.

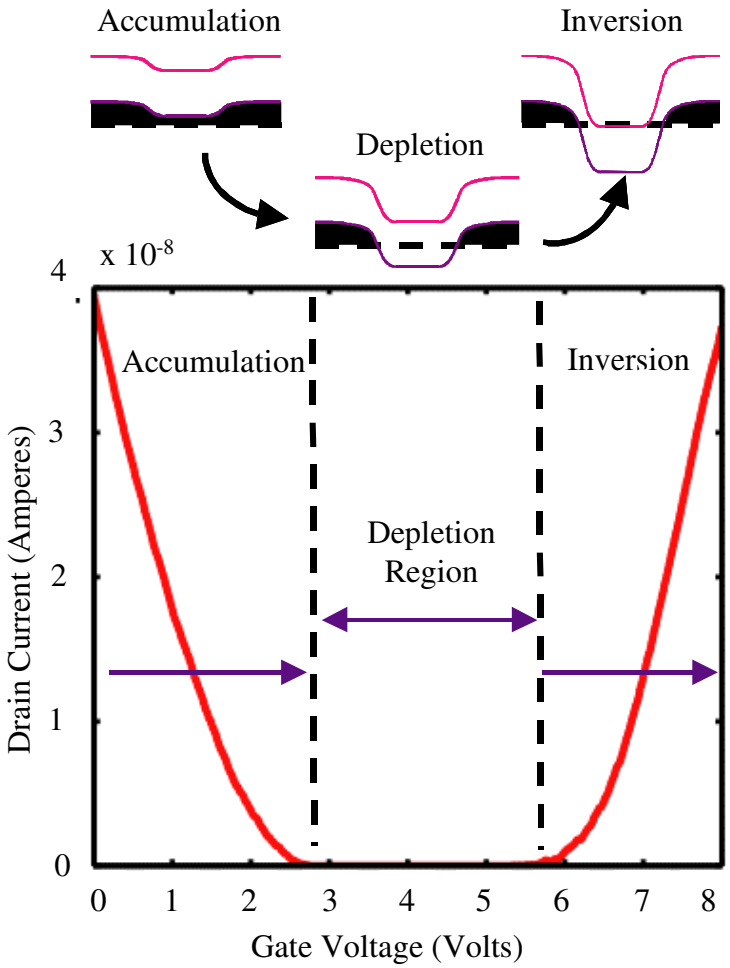


Figure 4.7: The measured dc current-voltage characteristic of a gated Hall bar transistor. The top schematic displays the potential profiles along the current direction for three operating regimes. In the schematics the purple line represents the GaSb valence band and the red line represents the InAs conduction band. As positive gate voltage is applied to the top-gate, holes in the GaSb layer are depleted reducing the conductance through the Hall bar (accumulation). Once holes are totally depleted no conduction occurs through the Hall bar (depletion). Eventually the area under the gate is populated with electrons and conduction resumes (inversion).

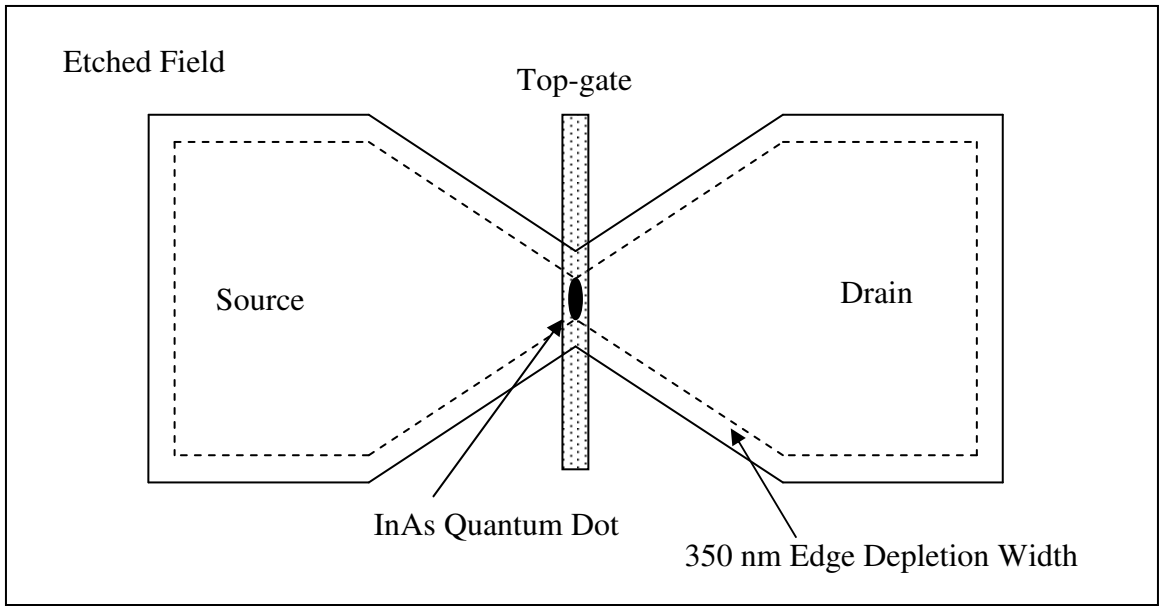


Figure 4.8: Schematic of the single electron transistor structure. A mesa etch is performed, forming a narrow neck between source and drain. Using a single top-gate a quantum dot containing one electron is formed. The mesa etch and edge depletion of the GaSb layers produces the transverse confinement and the gate creates two symmetric tunneling barriers in the lateral direction, forming a quantum dot.

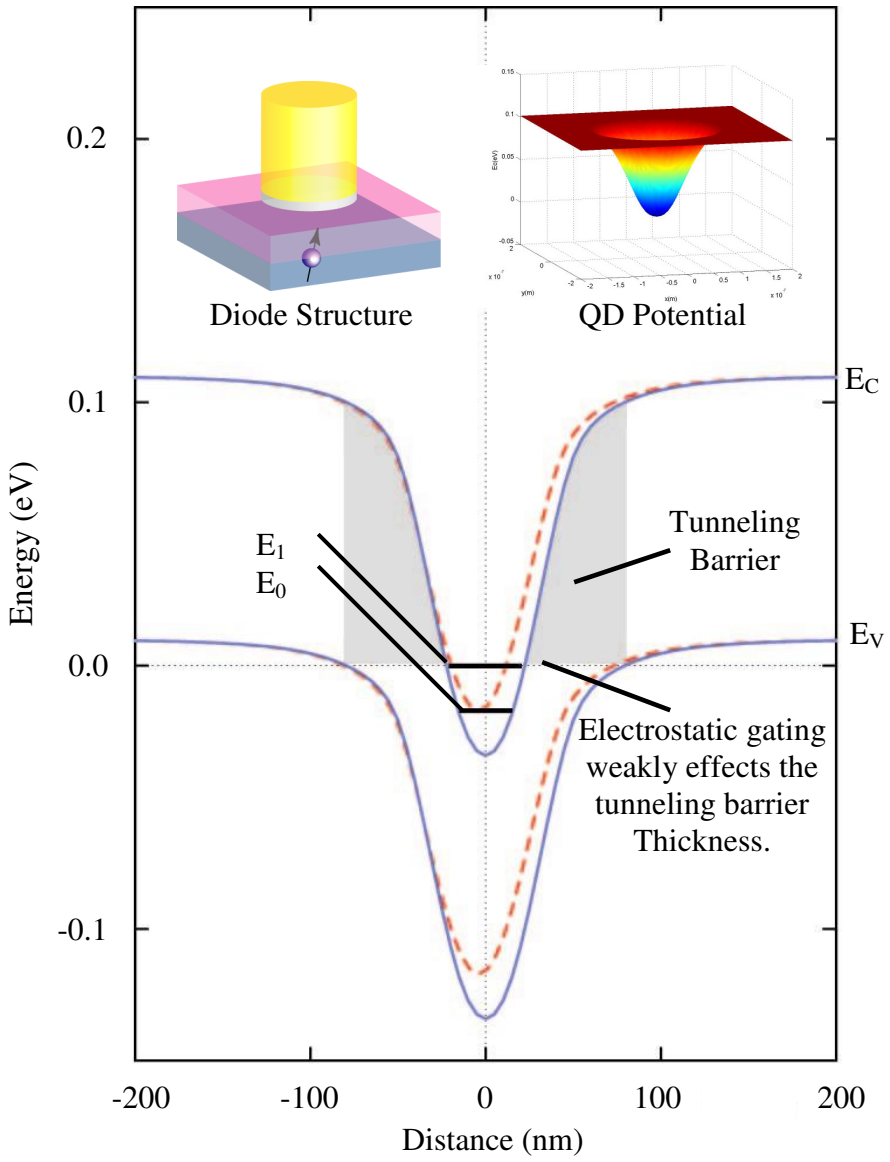


Figure 4.9: Calculated potential profiles for a MIS capacitor. Inset in the upper left is the model used. The second quantization level is aligned with the Fermi level. Here the Coulomb charging energy is excluded and the shaded areas illustrate the tunneling barriers. The right inset shows the 3D potential plot. Using this simulation the tunneling barrier thickness was determined to be a weak function of the top-gate voltage.

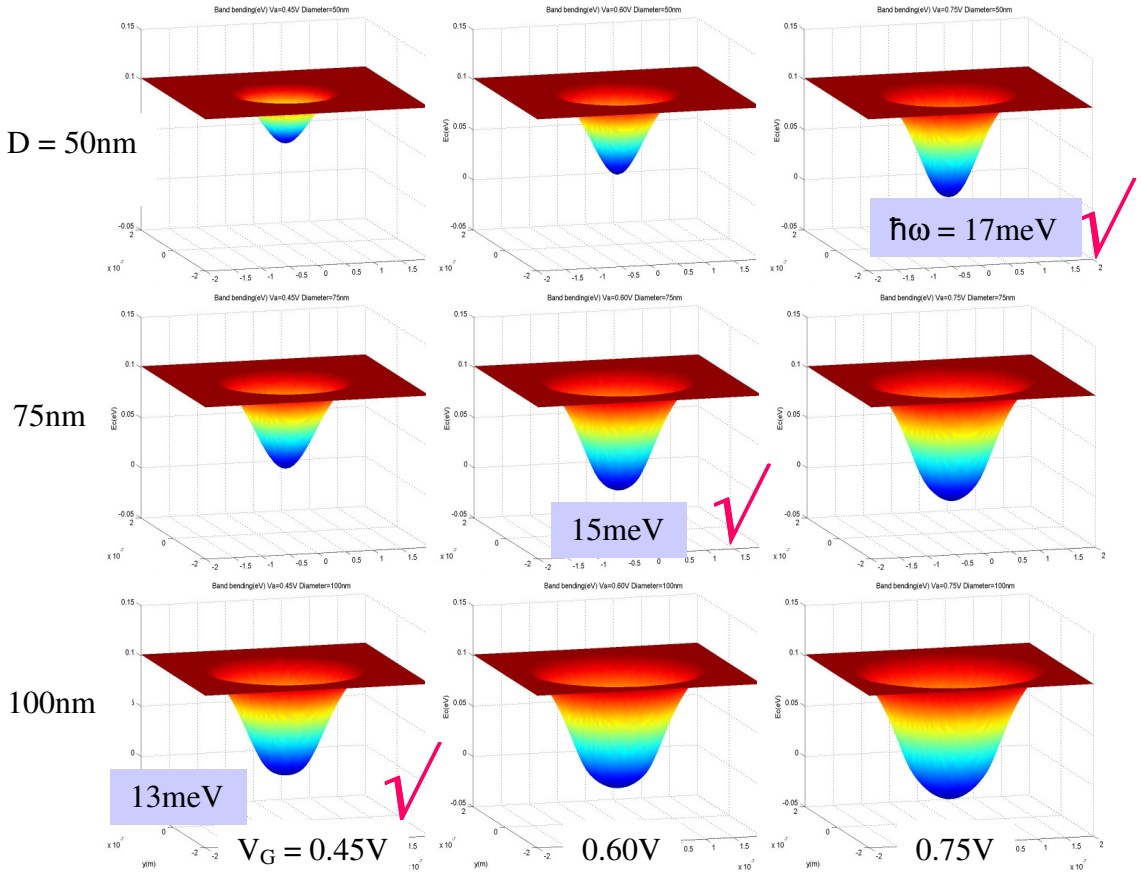


Figure 4.10: Simulation of the potential profiles for pillar gates of varying diameter. The gate diameters modeled are 50nm, 70nm, and 100nm, respectively. Each gate diameter is modeled for various top-gate voltages. Profiles with check marks have reached a depth necessary to confine a single electron. From this simulation we learn that reducing the diameter of the gate produces a steeper potential well. At the same time, a higher applied voltage is necessary to induce the first electron state.

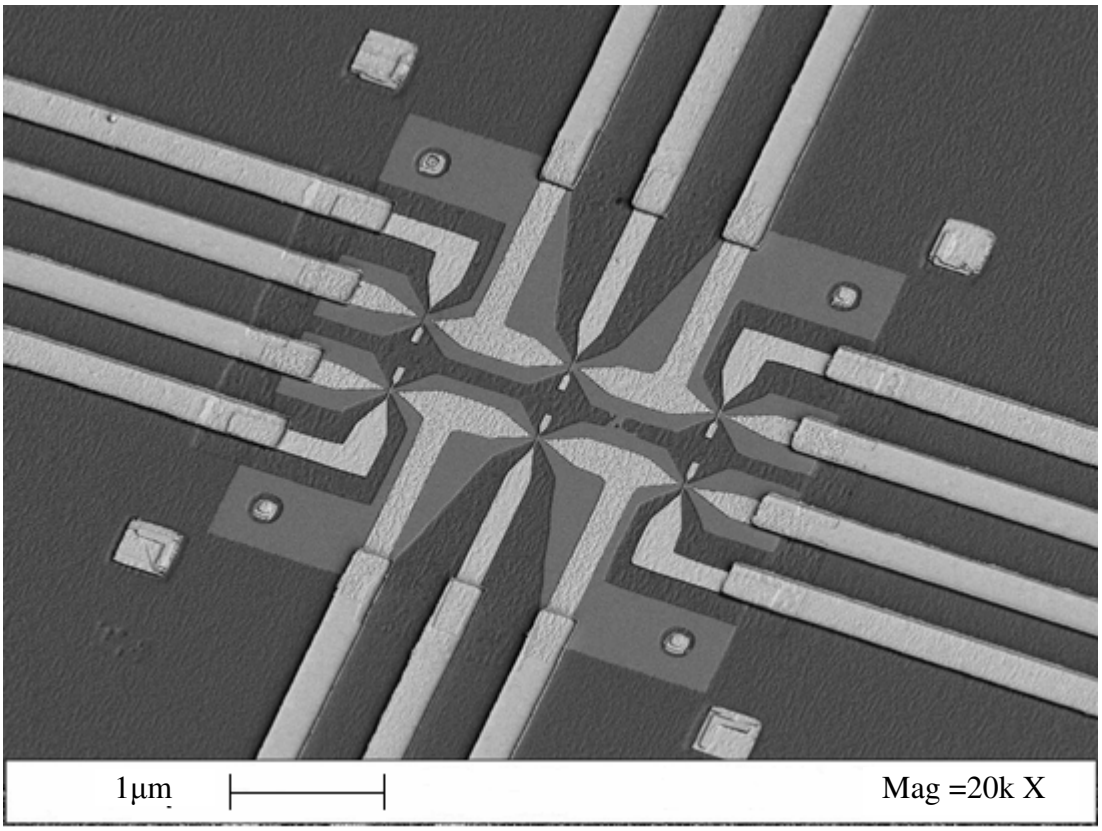


Figure 4.11: SEM micrograph of a finished set of six InAs single electron transistors at 20k X magnification. The darkest regions are where the InAs CQW has been wet etched off. The medium grey areas are where CQW has left behind. The lightest grey areas are evaporated metal used to make gates and ohmic contacts to the SETs. The length scale is symmetric in the horizontal and vertical directions.

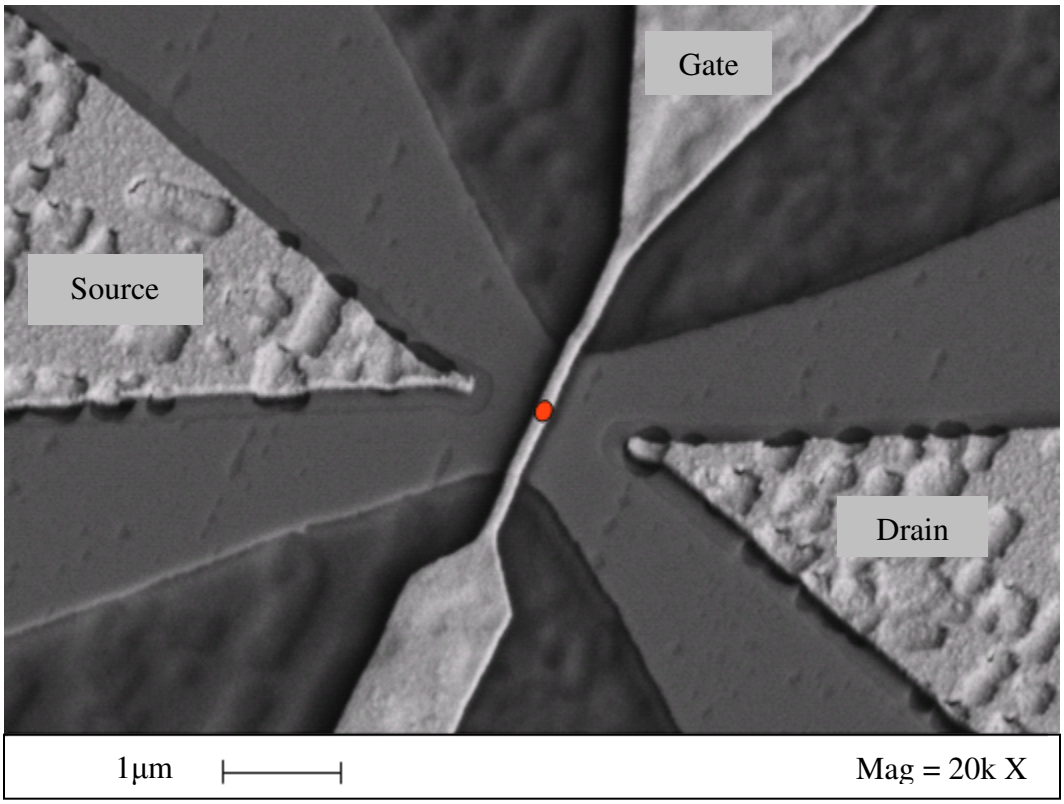


Figure 4.12: SEM micrograph of a finished InAs enhancement mode single electron transistor on composite quantum well. Metal ohmic contacts (labeled source and drain) were fabricated directly on the InAs quantum well. A gate is fabricated on etched insulating field to cover the narrowest portion of the source drain mesa, forming two symmetric tunneling barriers and a quantum dot. The QD location is indicated schematically by the red dot.

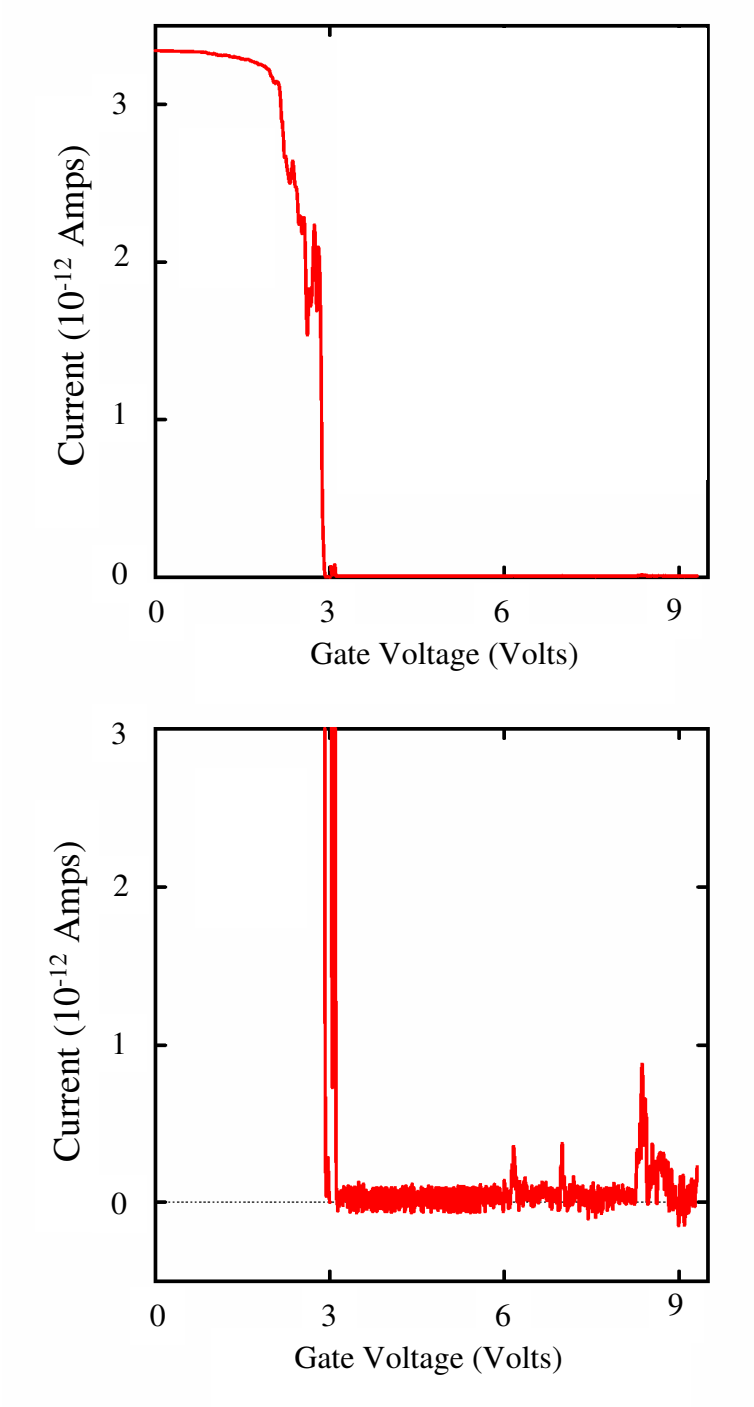


Figure 4.13 Single electron transistor current-voltage curve taken at 4.2K. Coulomb blockade oscillations are clearly observed. The peak heights are similar for the first three electrons indicating that the tunneling probability is only a weak function of gate voltage as expected from simulation.

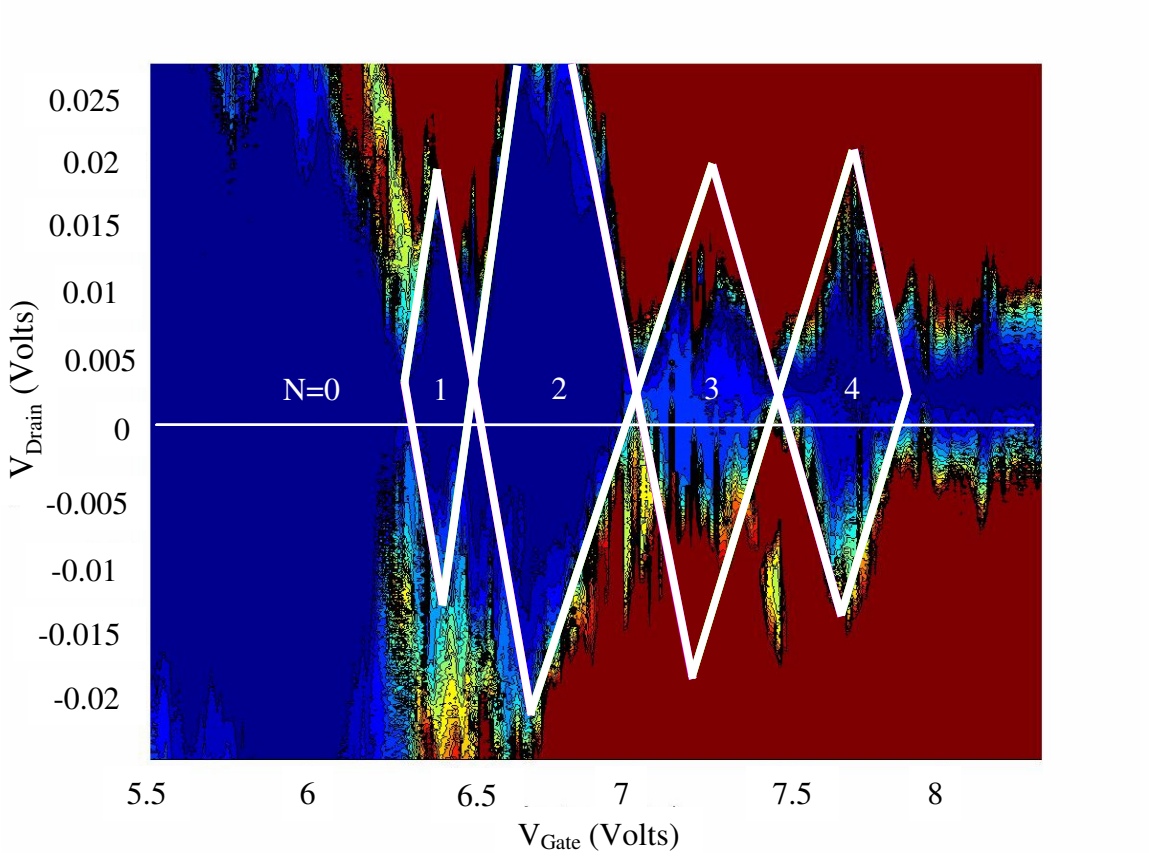


Figure 4.14: Stability chart of the enhancement mode InAs SET at 4.2K. N denotes the number of electrons present in each diamond. Lines are inserted to guide the eye to the diamond shapes. From the slope of the diamonds the capacitance of the tunneling barriers and size of the dot can be determined by the "orthodox theory" fully characterizing our quantum dot for different electron populations.

N	1	2	4
C_{gate}	0.69 aF	0.29 aF	0.37 aF
C_{drain}	4.7 aF	1.7 aF	5.1 aF
C_{source}	5.4 aF	2.6 aF	4.4 aF
E_c	15 meV	35 meV	16 meV

Table 4.1: Characteristics of the InAs Quantum dot derived from the diamond slopes. N refers to number of electrons trapped on the quantum dot. The third diamond was not characterized due to noise. Once the tunneling and gate capacitances are known, the orthodox theory for can be used to solve for the charging energy and dot sizes.

Chapter 5: Silicon Single Electron Transistor

A number of physical implementations for qubits have been proposed and investigated as the bases for quantum computing.[56] As was noted in the 4.1, Solid state implementations have potential in upscaling to large numbers of qubits and quantum gates. In particular, the two Zeeman states of an electron spin in a semiconductor quantum dot (QD) present a promising qubit candidate.[57] As already discussed in Chapter 4, semiconductor SETs come in two varieties, lateral and vertical. Because of the fabrication techniques available, lateral arrays of quantum dots provide a better opportunity for upscaling when compared with vertical tunneling structures.

In III-V compound semiconductors such as GaAs, the dominant mechanism of spin decoherence at low temperatures is the hyperfine interaction, where an electron spin couples to the randomly oriented nuclear spins of the surrounding atoms in the crystal lattice. Currently, electron spin coherence times have been measured in compound semiconductor quantum dots to be roughly 10ns and can be improved by a microwave pulsing technique, known as spin-echo, to be 1μs.[63] One electron confined in a silicon QD is expected to have a spin coherence time many orders of magnitudes longer than that in compound semiconductors, due to its zero nuclear spin.[72]

5.1 Introduction

In principle, lateral quantum dots in silicon could potentially be incorporated into the existing large-scale integrated circuits using current CMOS processing techniques. Nonetheless, there are considerable challenges in fabrication of quantum dots in silicon. Since the first observation of Coulomb blockade tunneling in silicon,[17] most experimental

efforts have focused on the depletion-mode field effect transistor (FET) scheme, using SOI (silicon-on-insulator)[73] wafers and Si/SiGe quantum well structures.[74, 75, 76] In these approaches, the as-grown sample already contains two-dimensional electrons (2DEG) from donors in the system prior to nano-fabrication. The surface Schottky gates or in-plane side-gates are used to define quantum dots and to deplete electrons in QDs from many down to one. Although this depletion-mode approach is reliably applied in the GaAs single electron transistors,[77] the fabrication of silicon based SETs still suffers from problems that stem from material properties. For example, gate leakage current due to dislocations in Si/SiGe quantum wells frequently disrupts the single electron transport. In SOI approach, the defects at the silicon/buried oxide interface cause strong localization of electrons and result in a noisy environment.

In view of the great promise of silicon for quantum computing, we have developed an enhancement-mode silicon SET. In this chapter we report demonstration of a metal-oxide-semiconductor single electron transistor (MOS-SET) which could be useful for spin quantum computation in silicon. Due to its unique structure, the MOS-SET avoids many of the existing materials problems in other silicon SET structures.

5.2 Silicon SET Device Structure

Our ultimate objective is to confine single electrons in an environment with a minimal concentration of impurities. In order to precisely define the location of a single spin and to consistently control the shape of the confinement potential by gating, the sample system should be free of random potential variations resulting from ionized impurities.[78] An impurity-free environment will also reduce telegraph noise and spin

decoherence caused by hyperfine interaction with impurity nuclei. To achieve this goal, high purity, isotopically enriched silicon wafers should be used, removing impurity scattering and potential variations from donors.

But at cryogenic temperature, high purity wafers become non-conducting, due to the lack of thermally generated carriers. Because of the non-conducting initial state of our devices, we employ a bilayer-gated configuration to fabricate enhancement-mode MOS-SETs. As illustrated in Fig. 5.1, the top-gate, which laterally overlaps the ohmic contact regions, induces 2D electrons at the silicon/thermal oxide interface similar to an enhancement mode FET.[79] In addition, multiple metal side-gates, located below the top-gate and above the thermal oxide, are used to screen the electric field from the top-gate, depleting only the electrons below the side-gates. Proper biasing to these gates defines the potential profile of an SET, including the source and drain leads, two tunneling barriers, and the quantum dot in between. This bilayer design offers the flexibility in device layout and allows independent control over the 2D electron density, the tunneling conductance and the electron population in the quantum dot.

5.3 Silicon Ohmic contacts

Our design requires doped ohmic contacts that serve as the SET source and drain. Before implantation we simulated the conditions necessary to produce a degenerately doped ohmic contact using a shareware program called SRIM.[80] Using a model of silicon with a 27nm SiO_2 layer on the surface we modeled the implant profile for many different implant energies. We wanted an implant depth that placed the majority of the dopants directly below the Si/SiO_2 interface and 40keV was determined by SRIM to produce this

profile. Figure 5.2 shows the 40keV SRIM simulation. Ohmic contacts were characterized by implanting phosphorous in a Hall bar pattern with implant energies of 20, 30 and 40keV, at a density of 7×10^{14} dopants/cm^2, and a 7° implant angle, through a 27nm sacrificial oxide layer on the silicon surface. The recipe targets a dopant density of 7×10^{18}/cm^3, which is well above the Silicon metal insulator transition. Degenerate doping of the ohmic contacts causes them to conduct at 4.2K. Samples were annealed at 1000°C and measured at 4.2K. It was determined that the 40keV recipe was the best because it provided the lowest sheet resistivity of 63Ω/square.

5.4 Characterization of the BCB Dielectric

For the dielectric between the SET side-gates and top-gate we chose to use a spin on dielectric called Benzocyclobutene (BCB). BCB can withstand an electric field of 5.6×10^6 V/cm at room temperature.[81] However, BCB has never been tested at 4.2K and it was important to verify that BCB would not leak at low temperatures or crack during thermal cycling. To verify these points we fabricated metal/BCB/silicon diodes for low temperature testing.

BCB was spun onto 3 inch silicon wafers at 5kRPM producing a 1μm thick layer. The BCB was cured at 210°C for one hour in a nitrogen environment and cooled slowly (over several hours) to reduce stress on the BCB layer during cooling. Allowing oxygen into the environment during curing reduces the quality of the dielectric. Capacitors for characterizing BCB were formed using a shadow mask technique. The shadow mask technique is a quick lithography process used to make large features in a regular array. See Figure 5.3. The wafer is placed face down on a metal plate with regularly spaced

2mm diameter holes. When metal is evaporated onto the wafer the areas left exposed by the shadow mask form the top electrodes of the capacitors. The bottom contact is made directly to the back of the silicon wafer, and the front metal is connected to a thin gold wire by conductive epoxy. We choose to use epoxy since soldering might cause rapid heating and cooling of the dielectric, possibly creating stress and altering the dielectric properties.

Using dc voltage we applied up to +/- 100V to the diodes at room temperature and 4.2K. No dc leakage current was observed within this range. Since, the dielectric was approximately 1μm thick, 100V should produce an electric field of 1MV/cm demonstrating that BCB maintains its dielectric properties at 4.2K. A capacitance measurement confirms the thickness of the BCB and the low frequency dielectric constant of 2.65, the same as what described in the manufacturer's specifications.

5.5 Silicon Hall Bar

According to the parallel plate capacitor concept employed in MOSFETs, when a positive voltage greater than the threshold voltage V_t is applied to a MOS top-gate, electrons will be induced at the Si/SiO_2 interface. Before fabricating SETs we fabricated Hall bars with two dielectric layers, identical to the structure that we planned to use for SETs. Fabricating the Hall bars served several purposes. First we were able to verify that using two different dielectric layers, we could induce 2DEG and obtain an approximate threshold voltage. Secondly, we were able to use a fabrication process similar to but simpler than the SET process, to trouble shoot for problems in our proposed SET structure.

Hall bars were fabricated by spinning 1μm BCB on top of a silicon wafer with implanted ohmic contacts and a 27nm thermally grown SiO_2 layer. Top-gates were evaporated on the surface. Finally, via holes were opened in the BCB and SiO_2 to make contact to the silicon ohmic contacts.

The Hall bars were measured using dc bias in common-source mode. Initially the Hall bars did not induce high-density 2DEG before dc leakage current was observed between the gate and either the source drain. It was determined that carriers leaked from the source or drain underneath the top-gate out through the gate bonding pad because carriers are induced under the entire top-gate at the Si/SiO2 interface. See Figure 5.4. In GaAs this problem is alleviated by forming a mesa around the devices isolating the quantum well from leaking to the gates. However, fabricating a mesa in silicon would not stop electrons from flowing out because there is no quantum well structure to etch off.

In a MOSFET the concentration of electrons in a gated region is proportional to the electric field applied to the semiconductor. To reduce electron concentration in an area, the dielectric thickness can be increased to reduce electric field and which thereby reduces the electron concentration in that region. In the silicon region under the gate leads and away from the device region, we dry etched narrow, 0.5μm deep trenches into the silicon. See Figure 5.5. By spinning on our gate dielectric with a 1μm thickness, the trenches were completely filled producing a region under the trench with a 1.5μm thick dielectric rather than the 1μm thick dielectric that covers the device region. This extra-thick dielectric region causes the electric field in the trench to be reduced and within a certain gate voltage range this region will not be populated with electrons. Effectively,

the trench blocks dc leakage current path from the 2D interface to the gate bonding pad. See Figure 5.6.

Once we implemented the trench etch into the device process we were able to produce working Hall bars. The threshold voltage varied from device to device but was found to be approximately 35-40V. This variation is most likely due to non-uniformity in the BCB dielectric thickness. We characterized the Hall bars at 4.2K under magnetic field. The 2D electron concentration was tunable within a range of $4.5\text{-}5.6\times10^{11}/cm^2$ and the mobility was determined to be $\sim2000 cm^2/V\text{-}s$. The mobility was much lower than expected. We have yet to carry out new experiment, showing that this method can indeed produce 2D electrons of high mobility.

5.6 Silicon SET Fabrication

Applying our design concept, we have fabricated MOS-SETs that show no measurable gate leakage current (<10fA) and display single electron tunneling phenomena. For the work reported here, we used substrates p-doped to approximately $10^{15}/cm^3$ as a proof-of-principle demonstration. Higher resistivity wafers would further reduce impurity-induced disorder.

The ohmic contact patterns for the SET are long leads extending from 3μm-wide lines in the immediate SET device area, to the 250μm square bonding pads. Implants were doped with the 40keV recipe. A subsequent annealing for implant activation is carried out concurrently with the growth of thermal oxide. We choose to grow the thermal oxide at 1000°C for 20 minutes in dry oxygen and the resulting thermal oxide thickness is 27nm. Afterwards, the SET side-gates are defined by electron-beam

lithography, metal evaporation (aluminum and gold) and lift-off. Fig. 5.7 (a) shows an optical microscope picture after deposition of side-gates. Figure 5.8 is an SEM micrograph of the side-gates at the device center.

After the surface gates are fabricated BCB is applied to electrically isolate the top-gate from the surface gates. The polymer was spun at 5kRPM and cured in a nitrogen environment at 210°C for 1 hour as described in section 5.4. Next the top-gate is defined by photolithography using negative tone resist on the top of the second layer of gate dielectric. See Figure 5.7 (b). Finally, via holes are opened in the BCB to expose the bonding pad regions of the ohmic contacts and the metal side-gates. For the exact process details see Appendix C.

We encountered some difficulties fabricating silicon devices that are worth discussing. Although we had very specific recipes for our photolithography steps, the exposure time for SiO_2 on silicon wafers is significantly different than either GaAs or InAs. Roughly 50% more UV exposure is necessary to fully expose the photoresist used for fabrication of gates and large features. This is because SiO_2 is less reflective than GaAs or InAs so less backscattered UV light is produced, reducing exposure.[82] After increasing the exposure time, development times remain unchanged because ultimately the total resist exposure is unchanged.

Each lithographic step of our process must be aligned to an alignment mark on the wafer defined by one or more previous lithography steps. Our concern here is that the oxide growth and dopant activation require high temperatures that would destroy metals used for alignment marks. For the MOS-SETs discussed here, we solved this problem by using RIE dry etching to create alignment marks 0.5μm deep in the silicon wafer before

ohmic implantation and oxide regrowth. These marks are visible by optical inspection after multiple layers of oxide regrowth, and are still usable even after the spin on gate dielectric is applied.

5.7 Silicon SET Transport Characteristics at 4.2K

The MOS-SETs were characterized at 4.2K. While the source-drain, side-gates and the top-gate were dc biased by automated digital to analog converters, the source-drain conductance was measured by an ac technique using a 37Hz, 0.1-1mV excitation voltage. The drain-source current was fed into a transimpedance amplifier with a gain of 100Mohm, and read out by a lock-in amplifier. We first sweep the top-gate voltage (V_{G1}) and monitor G_{56} (the conductance between ohmic contacts 5 and 6 shown in Fig. 5.9 (a)). The onset of strong inversion occurs at $V_{G1} = 44V$. In contrast, due to the depletion under the four side-gates, $G_{21}=0$ for $V_{G1} < 48V$. For $50V \leq V_{G1} \leq 55V$, Coulomb blockade oscillations dominate the G_{21} versus V_{G1} characteristics. Figure 5.9 (b) shows an example of the Coulomb blockade oscillations, where G_{21} versus the top-gate voltage is measured at $V_A=V_B=V_C=V_D=0V$ and $V_{21}=8mV$ (source-drain dc bias). Figure 5.9 (c) presents another example, where the top-gate voltage is fixed, and G_{21} was measured against the sweeping side-gate voltages. Figure 5.9 (d) shows the dependence on drain bias.

Figure 5.10 displays the stability chart of a MOS-SET. The stability chart produced.is a contour plot of the drain conductance (G_{21}), versus the dc component of the drain-source bias (V_{21}). For this plot the side-gate voltages were set to 0V ($V_{G2}=V_A=V_B=V_C=V_D=0V$), while sweeping V_{G1}. The unused ohmic leads were left open. As a manifestation of single electron transport in the Coulomb blockade regime, the

contour plot shows a series of diamond-shaped blocks. A similar stability chart, shown in Figure 5.11 is produced by holding the top-gate V_{G1} =54.25V while holding two side-gates (V_{G2}=V_A=V_B=0V) and sweeping V_C=V_D. Finally a third stability (Figure 5.12) chart is produced by holding the top-gate at a fixed voltage and biasing side-gates 1-3 to zero volts (V_A=V_B=V_C=0V) while sweeping the fourth side-gate V_D=0 to -0.45V. In this stability chart fine detail including regions that represent excited electron states are visible.

5.8 Silicon SET Analysis

We model the SET by the equivalent circuit shown in Figure 5.13, which consists of a source (1), a drain (2), a QD, a top-gate (G_1), and a side-gate (G_2). There is capacitive coupling between the QD to other electrodes, including through the source (C_1), the drain (C_2), the top-gate (C_{G1}), and the side-gates (C_{G2}). To allow for tunneling current, two conductors connect the QD to the source (R_1) and the drain (R_2).

Applying the "orthodox" theory to the data shown in Fig. 5.11, the half height of the diamond (ΔV_{21}=e/C_Σ) is a measure of the charging energy $E_C = e^2/C_\Sigma$, where C_Σ = C_1+C_2+C_{G1}+C_{G2}. A charging energy of 18meV is observed. The half height, the full-width, and the two slopes defining the diamond uniquely determine the respective capacitances: C_1 = 4.3aF, C_2 = 3.4aF, C_{G1} = 0.08aF, and C_{G2} = 1.3aF. If we model the quantum dot as a disc with a diameter *d*, the obtained capacitance of our silicon quantum dot suggests an effective diameter of about 20nm. Here, we use $C_\Sigma = 4\varepsilon d$ and ε=11.9 for the dielectric constant of silicon. The QD, resulting from electrostatic confinement, can

be further downsized by using a thinner thermal oxide, narrower side-gates, and smaller gaps between side-gates.

For qubits applications, large energy level spacing is preferred because it lessens the mixing of orbital states via spin-orbit coupling, and consequently, reduces spin dephasing. If we approximate the QD potential to be a 2D harmonic oscillator, with a ground state wave function spread of 20nm, the energy level spacing is ~7.8meV. Compared to the GaAs SETs, this energy spacing is large, despite the larger electron mass in silicon ($0.19m_0$ vs. $0.067m_0$). The large energy spacing is mainly due to the smallness of our quantum dot. Note that the spin-orbit coupling in silicon is three orders of magnitude smaller.[83] In other words, any spin dephasing mechanism via spin-orbit coupling[84] is three orders weaker in pure silicon, leading to a much longer spin lifetime.

On the quantum dot, we estimate that there are at most a few electrons under the reported operation condition. Based on the capacitive coupling between the top-gate and the Si/SiO_2 interface, the induced 2D electron concentration is calculated to be 1.4×10^{10} cm^{-2} per volt. The top-gate threshold voltage is 44V, indicating that at V_{G1}=54.25V, (the bias used in data shown in Figure 5.10) there is only one electron per 26nm×26nm area, which is on the same order as the size of the QD confinement The correctness of this estimate is also supported by the large charging energy.

5.9 Silicon SET Conclusion

In conclusion, we have demonstrated experimentally a silicon single electron transistor with only a few electrons in the quantum dot. Our structure does not suffer from problems such as gate leakage current or severe disorder in the environment that are

reported in other silicon approaches. The key features of this design include (1) the use of undoped substrates for removing impurity disorder that causes strong localization, and (2) a MOSFET-like structure, where electrons residing at the Si/SiO_2 interface are induced and manipulated by two layers of gates. We demonstrate that the top-gate and the nano-fabricated side-gates can be properly biased to create a single electron transistor with a large charging energy. Because the two layers of gates control the single electron population and the tunneling barriers independently, this approach provides flexibility in regulating the number of electrons in the quantum dot.

Future improvements include using a lower background impurity concentration (e.g., $< 10^{12}/cm^3$) and more refined thermal oxide growth technique to further reduce the electron traps in the system. Ultimately, ^{28}Si enriched substrates should be used to maximize electron coherence times. This work suggests that using the bilayer gating approach on undoped silicon, one can produce the highest possible quality, low-dimensional electrons. Both the top-gate and the side-gates can be nano-scaled so that the patterned electrons at the two-dimensional interface can form one-dimensional quantum wires or zero-dimensional quantum dots. Because the sample system is nearly free of impurities, or, as low as the fabrication technology allows, the electron spin coherence time is expected to be long[72] enough for quantum computing applications.

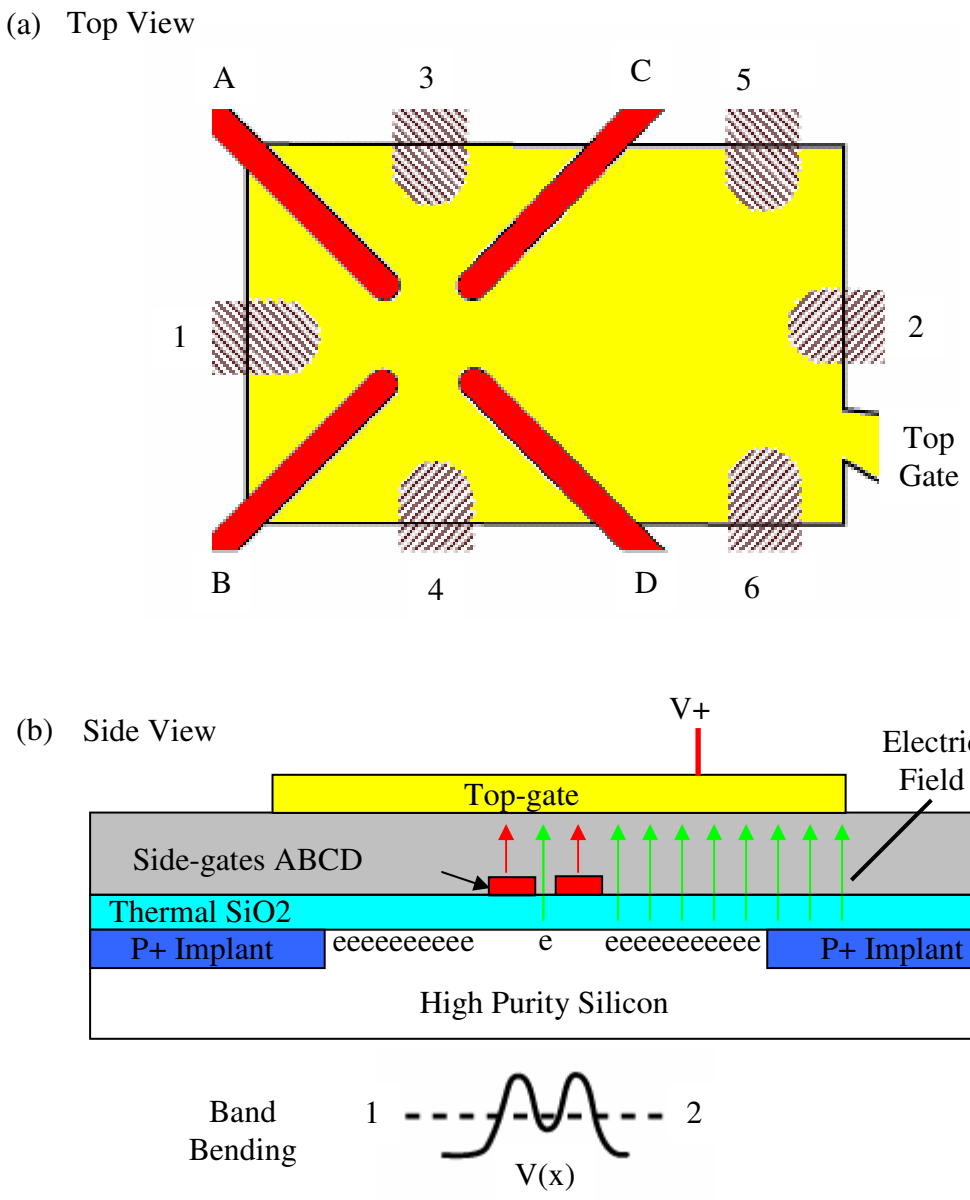


Figure 5.1: Schematics of (a) the top view and (b) the cross sectional view of our silicon single electron transistor structure. In (a), the solid thick line, shaded regions, and the rectangular area depict the side-gates, phosphorous-implanted ohmic leads, and the boundary of the top-gate, respectively. The schematic potential profile along the 1-2 direction under the single electron tunneling condition is shown as an inset (lower center) in (b). Arrows depict the electric field lines created by gating. The metal side-gates screen the top-gate electric field defining the SET potential profile.

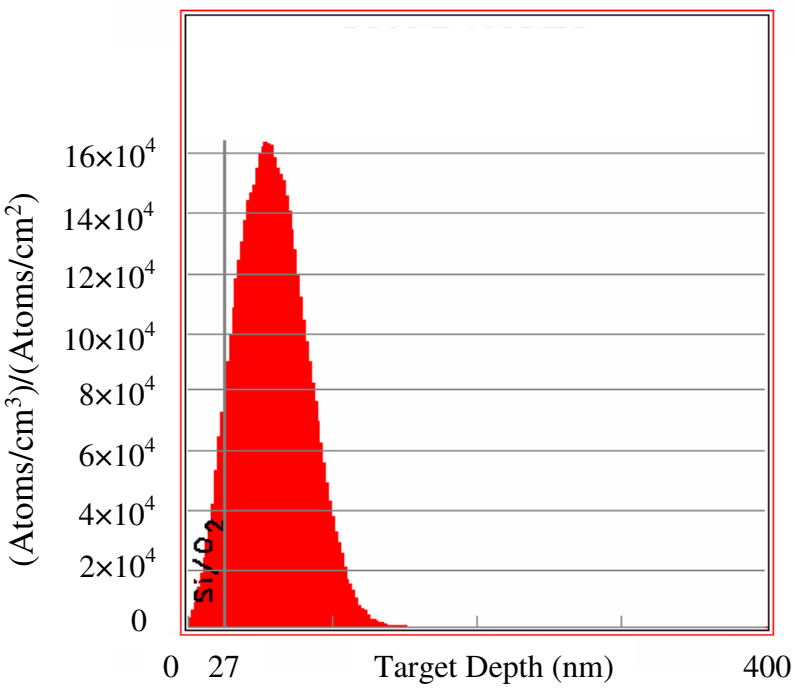


Figure 5.2: SRIM simulation of the density of phosphorous atoms as a function of depth in silicon. The phosphorous implantation energy is 40keV, and the surface has a 27nm SiO_2 implant mask.

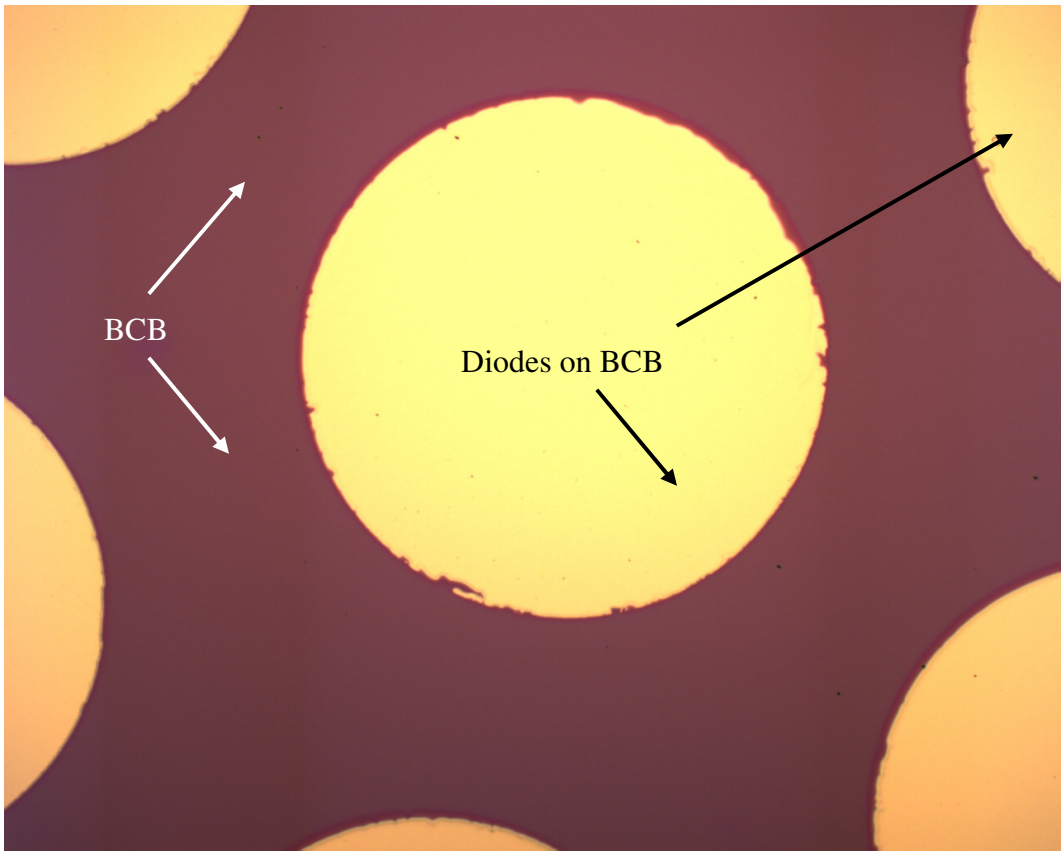


Figure 5.3: Metal/BCB/silicon diodes formed by the shadow mask technique. The dark red region is exposed BCB on a p-type silicon wafer. The gold colered regions are metal film defined on top of the BCB layer by shadow mask. The metal/BCB/Si capacitors are approximately 2mm in diameter.

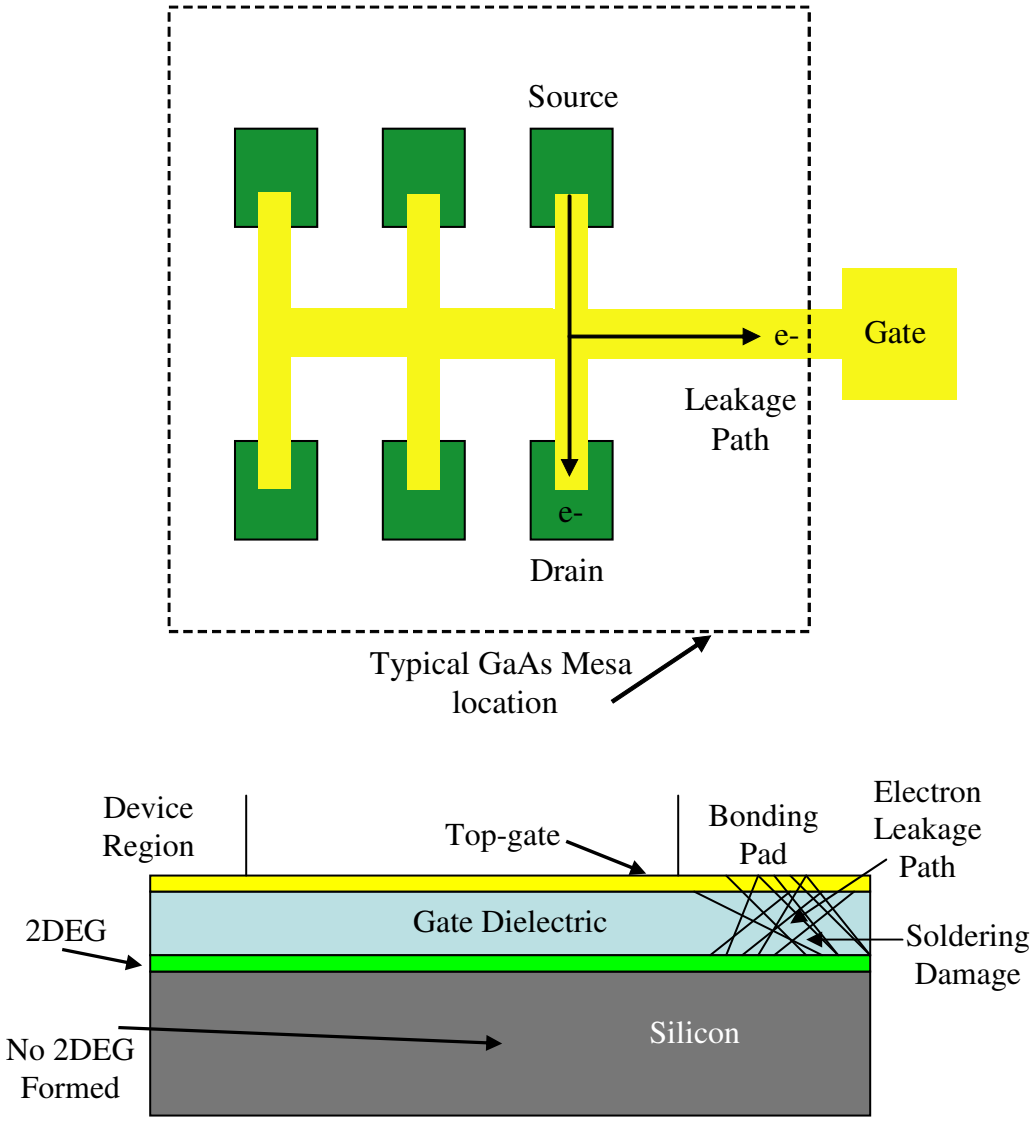
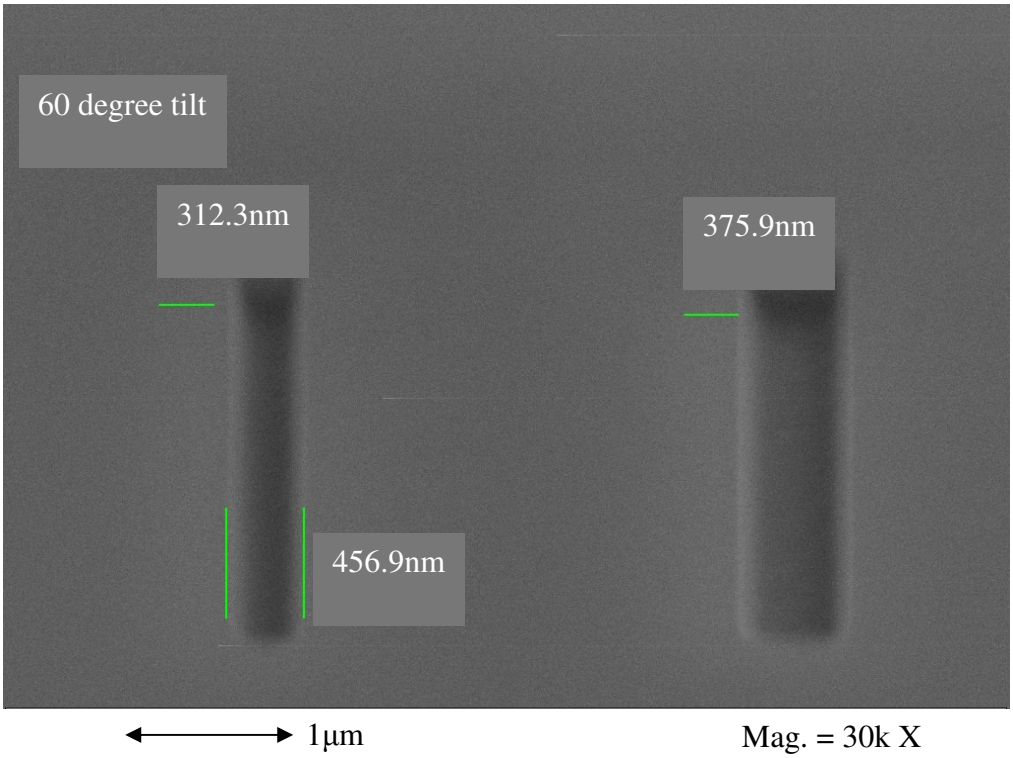


Figure 5.4: Schematic of the silicon Hall bar and leakage problem. If electrons are induced under the top-gate and the gate dielectric is of unifrom thickness, electrons will flow from the device to the gate bonding pad, where leakage occurs due to unavoidable damage caused by wirebonding or hand soldering. Typically GaAs Hall bars are produced with a mesa etch to avoid this difficulty.



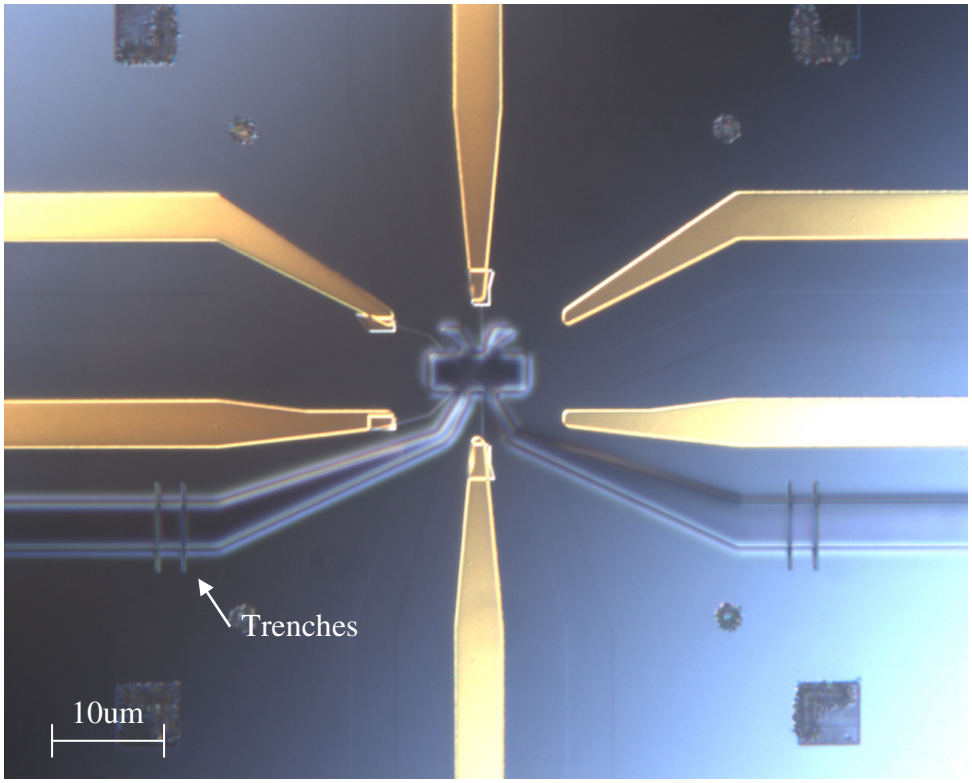


Figure 5.5: Trenches etched in silicon used to block gate leakage current. The top figure is a test run performed with different e-beam defined wire widths. The bottom figure shows the trenches after the top-gate has been defined but before metal evaporation.

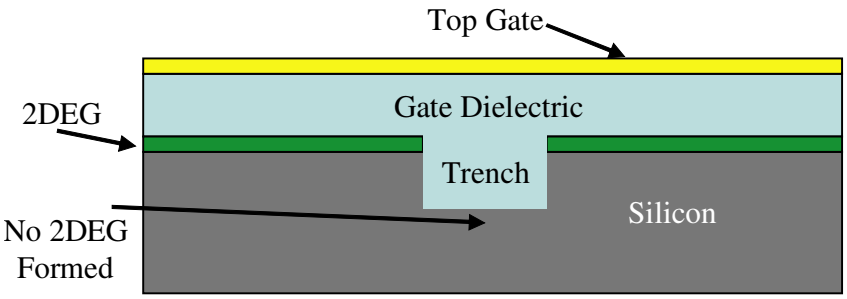
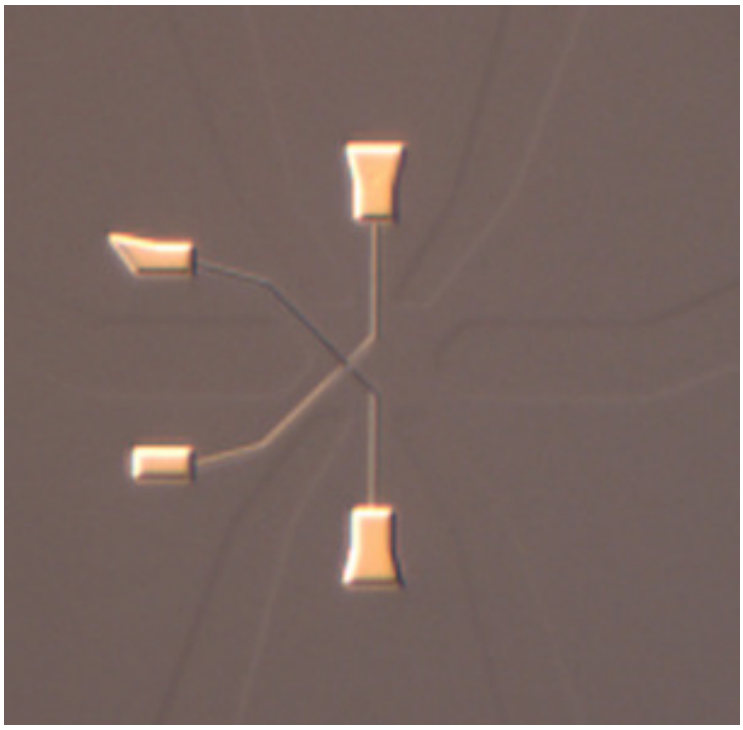


Figure 5.6: Schematic of how gate leakage is blocked by forming trenches. The BCB spin-on dielectric in principle can planarize the wafer surface, forming a thicker layer locally at the trench. After the planarization process, the dielectric above the trench is thicker than that in the field, locally reducing the electric field intensity at the trench. Therefore, 2DEG will not be induced in the trench.

(a)



(b)

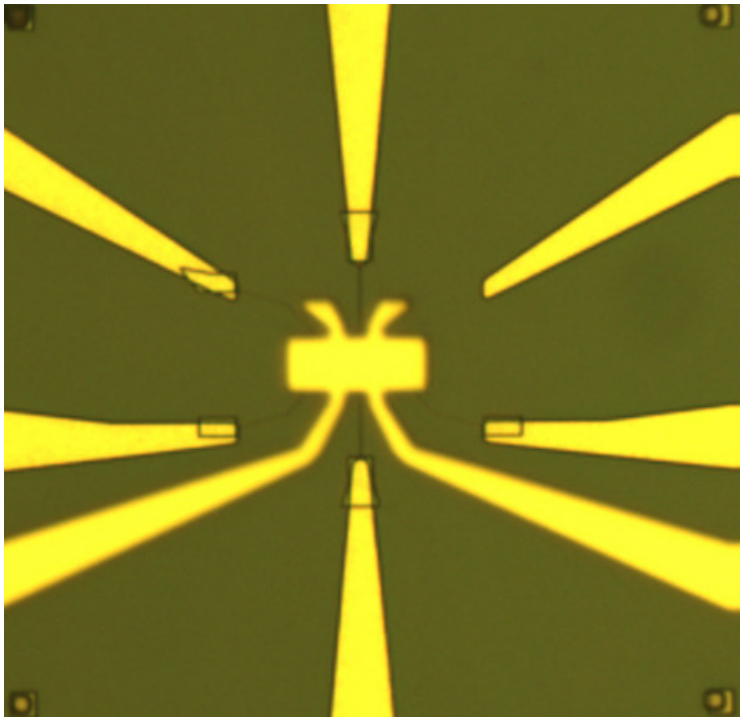


Figure 5.7: Optical microscope images of the SET device during processing. (a) 25μm×25μm optical micrograph of the SET side-gates after metal film evaporation and liftoff. Also visible are the six implanted regions. (b) 30μm×30μm image of the SET after the BCB layer and top-gate have been added to the SET. Gold colored regions are metal films. The top-gate appears slightly out of focus illustrating the 1μm height difference between the side-gates and top-gate.

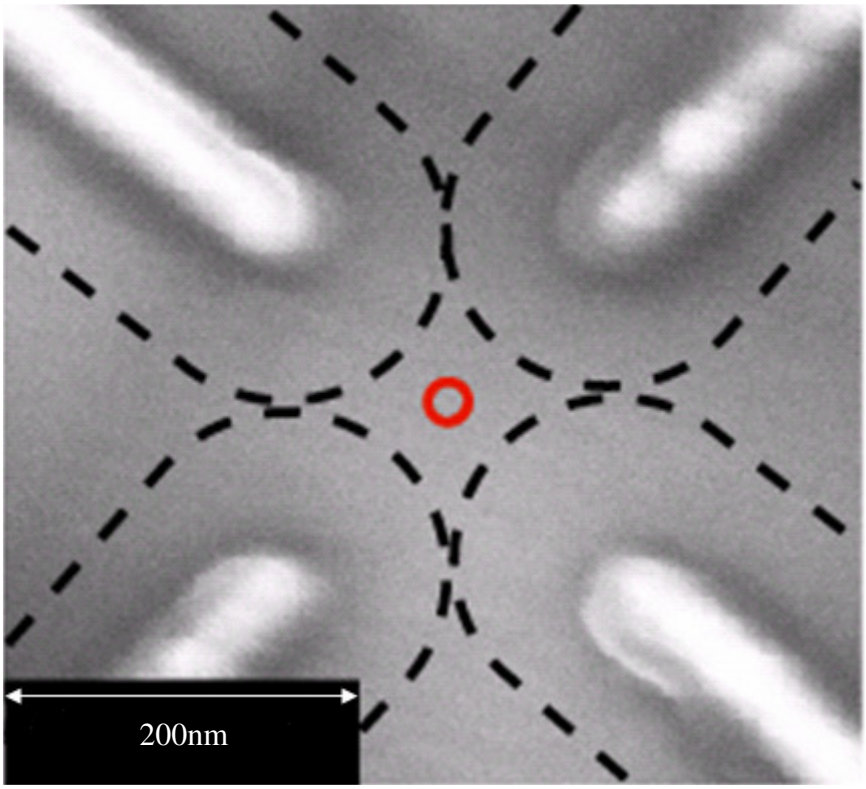


Figure 5.8: Scanning electron micrograph of 70nm wide side-gates defined by electron-beam lithography, taken before the top-gate is defined. The gap between neighboring side-gates is ~160nm. The dashed lines illustrate the depletion region under the single electron transistor operating condition. The circle, 20nm in diameter, depicts the location of the quantum dot, as discussed in text.

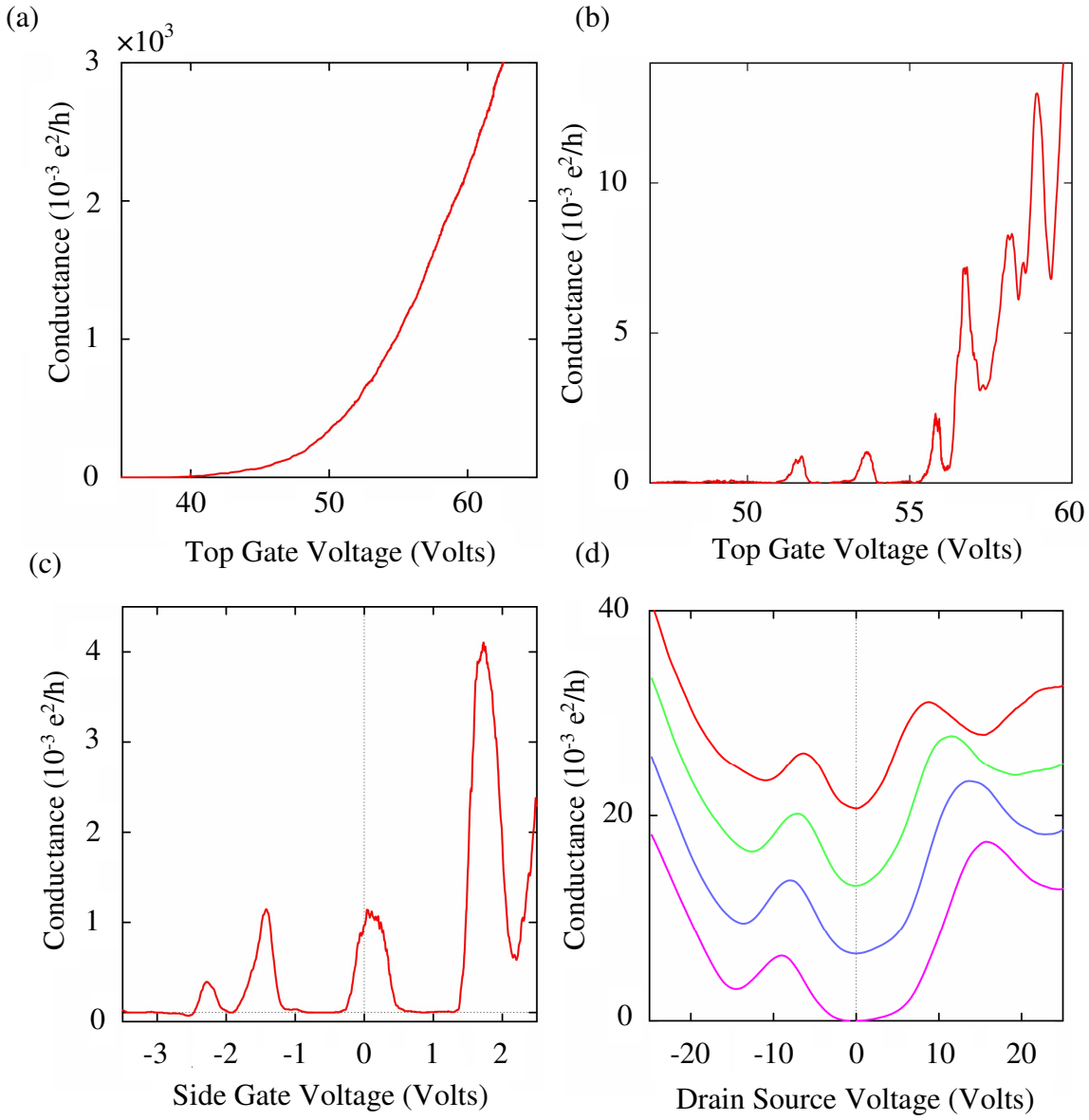


Figure 5.9: (a) FET transfer characteristic through induced 2DEG under top-gate. (b) Transfer characteristics versus the top-gate voltage, at $V_A=V_B=V_C=V_D=0V$ and $V_{21}=8mV$. (c) Transfer characteristics controlled by the side-gate voltage, at $V_{G1}=54.25V$ and $V_{21}=8mV$. (d) Transfer characteristics as a function of swept source-drain bias with a top-gate voltage of 60V. Different scans represent the side-gate biases. From the top scan to the bottom scan the side-gate biases are -0.226V, -0.213V, -0.2V, and -0.187V respectively.

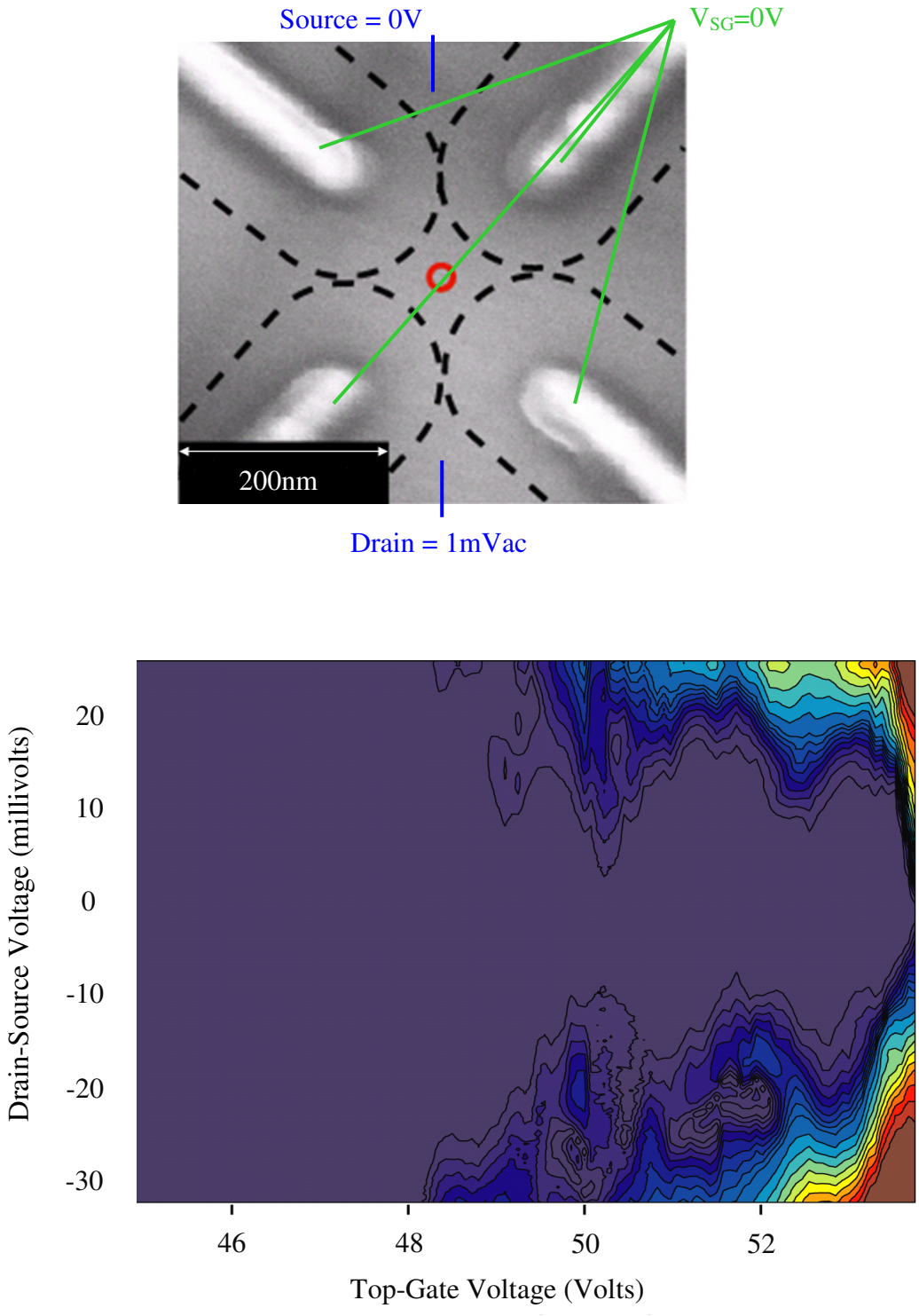


Figure 5.10: The stability chart taken with all side-gates shorted to zero, and V_{TG} is swept between 44.75V and 53.75V. At the top is a schematic of the measurement voltages used to produce the stability chart.

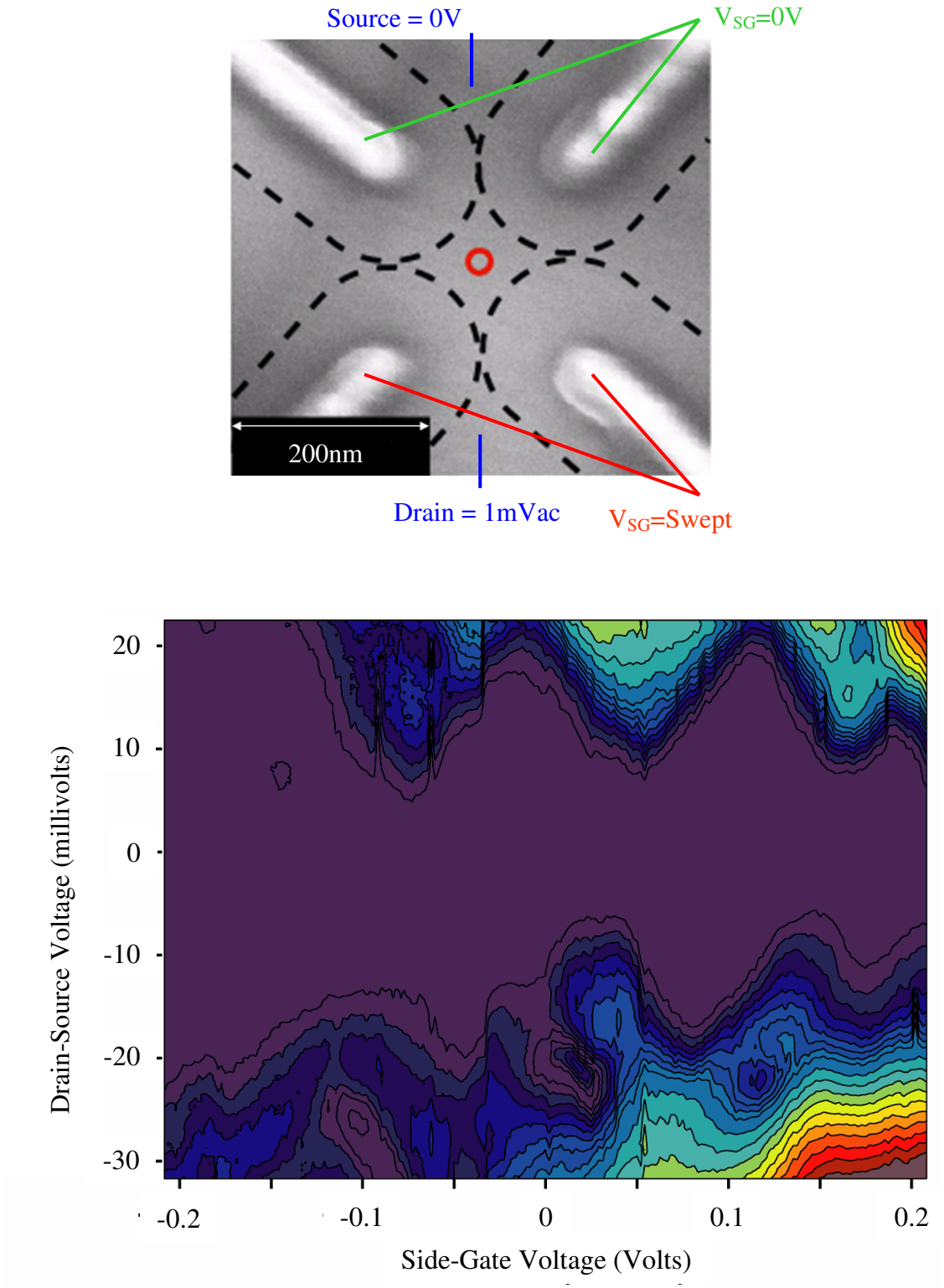


Figure 5.11: The stability chart taken with V_{G1} = 54.25 V. The side-gates were swept between −32 mV to +22 mV. The top schematic shows the measurement voltages used to produce the stability chart.

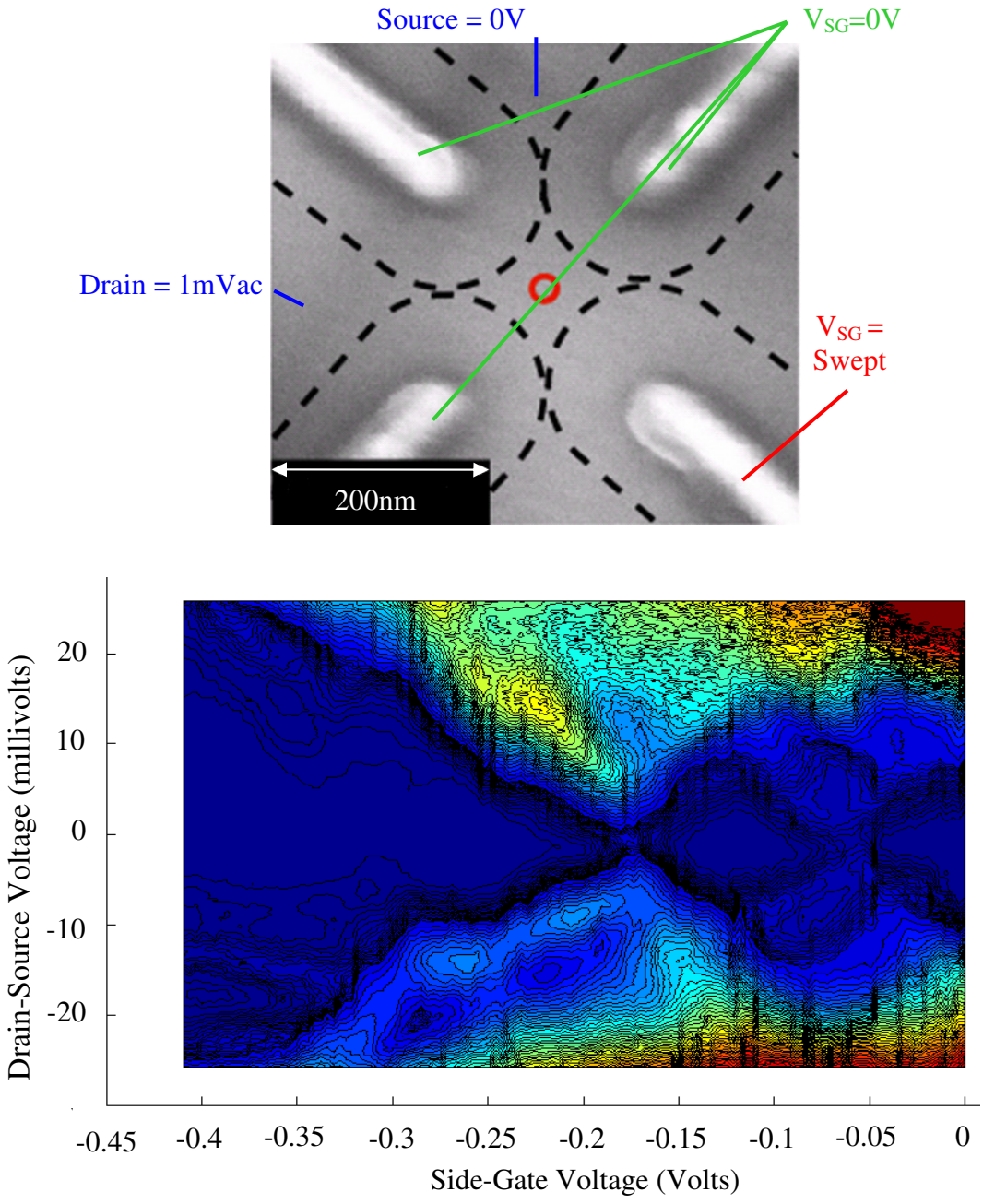


Figure 5.12: Stability diagram using a single side-gate as a "plunger." On top is a schematic of the measurement technique used to produce the stability chart. The chart is produced by holding the top-gate at a fixed voltage and biasing side-gates 1-3 to zero volts (i.e. V_A=V_B=V_C=0V) while sweeping the fourth side-gate V_D=0 to -0.45V. In this stability chart fine detail is visible, including regions showing excited electron states.

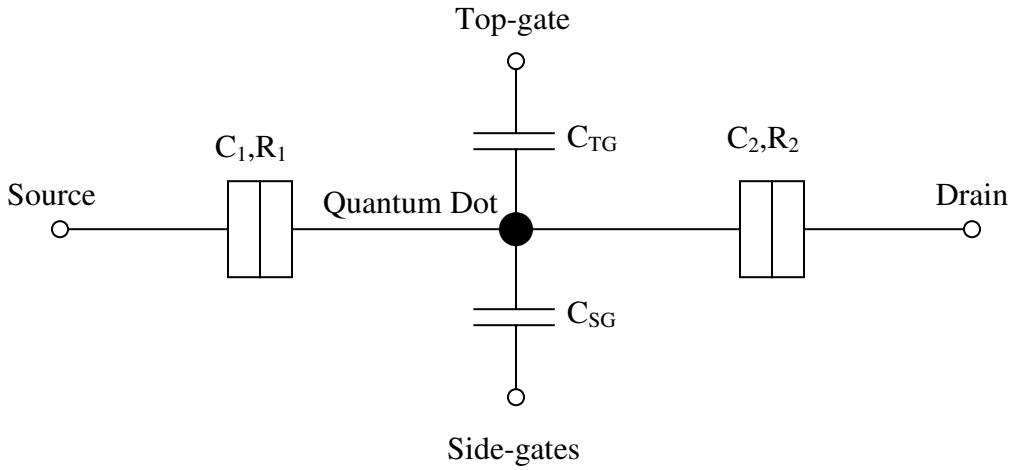


Figure 5.13: The SET equivalent circuit used in the analysis of the SET.

Chapter 6: Conclusion

I have reported our recent experimental work on three nanometer-scale quantum devices. With the Y-Branch Switch (YBS) we have demonstrated switching of the electron wavefunction in a transistor structure. Successful fabrication of a YBS requires producing narrow undepleted wires where the channel length is shorter than the electron mean free path. This is accomplished by lithographically defining ultra-small transistors in InAs quantum wells. One natural extension of this work would be to produce a device where only one individual conductance channel is occupied. In this extreme quantum limit, one would expect to observe a monotonic transconductance change when switching. Another direction would be to design experiments for verifying that the switching frequency of the electron wave can be as high as THz.

With the InAs single electron transistor (SET), we achieved the one-electron regime in a 20nm InAs quantum dot with an orbital energy spacing of 20meV. Confinement of the electron is produced by a single top-gate and no external measurement technique is necessary to verify the one-electron state. This work provides the third unique demonstration of a single confined electron in semiconductor and is the first such work in InAs. Future experiments with the InAs quantum dot involve the coupling of two one-electron quantum dots and demonstrating Rabi oscillations.

Finally, with the silicon MOS-SET, we proposed and demonstrated a bilayer gating approach to making a quantum dot in pure undoped silicon. Through transport measurements the quantum dot is proven to be already in the few-electron regime. Future research with this device involves definitive proof of a single trapped electron in silicon, a milestone for quantum computing since the electron spin-coherence time in silicon is

expected to be many orders of magnitude higher than that of III-V compound semiconductors. Once a single electron state is demonstrated, the future experiments will also be to couple two one-electron quantum dots and demonstrate Rabi oscillations.

One last area for future research might be to combine the bilayer enhancement mode silicon device concept with the YBS work, to produce a coherent YBS in silicon. By using the enhancement mode approach single mode operation may be more easily achieved than in InAs. In InAs the carrier concentration is fixed due to the InAs quantum well doping levels and we must lithographically fabricate a device with a dimension small enough to produce a single mode. However, with the silicon approach we can tune the 2D electron concentration with the top gate, and this feature enables additional control of the Fermi level. Furthermore, this fabrication method might improve on previously studied silicon devices such as quantum point contacts, as well as leading to fabrication of devices not previously achieved in silicon, such as the AB interferometer.

Appendix A

PMMA 1% in Toluene Lithography procedure For Ballistic Transistors (X-junction, QPC, YBS)

Sample Preparation

Time: _____

□ Solder In dots for secondary electron emission collection and check resistance (approximately 3k Ohms)

□ Spin PMMA T1: 5kRPM, 45sec

□ Pre-bake: 180°C, 90 seconds on hot plate with vacuum.

(Actual bake temperature = _____°C, bake time = _____)

(estimated thickness ~ 20nm)

E-Beam Writing

Time: _____

1.4pt focusing :

□ Drop one drop gold solution at each corner of the sample

□ Check resistance between spring and other In dot (~ 60 ohms typical)

□ Pinhole current : _____ pA for CC = ____

_____ pA for CC = ____ before focusing

□ Focus at each point and run 4pt2.exe to get the fitting plane function

2.E-beam Writing : **Runfile name : _____ .rf6**

Line dose : __2.5nC/cm___, c-t-c = 43 Å, current ~ 12 pA

Point dose : _____, current ~ 10 pA

Area dose : _225uC/cm^2, c-t-c = 101Å, line spacing = 101 Å, current ~ 12 pA

□ Pinhole current : _____ pA for CC = ____

_____ pA for CC = ____ before writing

□ Check when using global correction : _____ degree

□ Pinhole current : _____ pA for CC = ____

_____ pA for CC = ____ after writing

E-Beam Resist Development

Time: _____

□ Develop: MIBK/IPA (1:3) for 35 seconds

□ Overlap Rinse: IPA 40 seconds

□ Overlap Rinse: DI water 80 seconds

□ Blow dry: compressed nitrogen gas

Wet etching Time: _____

InAs etchant (acetic acid, hydrogen peroxide and DI water=5:10:100) ~25A/sec

GaSb etchant (hydrogen peroxide: HF: lactic acid .5:.5:100) – 20-25A/sec

InAs: _____ Å Time: _____5_____ sec
AlSb/GaSb:_____ Å Time: _____4_____ sec
InAs: _____ Å Time: _____17_____ sec

□ Alpha Step to make sure field is properly etched (Measured _____ Å)

Remove Resist

□ Clean using heated Acetone 60 minutes (Actual dip time: _____ hr) + Isopropyl Alcohol. No DI water to reduce oxidization.

□ Alpha Step to check etch depth.

Step 2: Ohmic Bonding Pads Date:_____

I. Sample Preparation Time: _____

□ Spin positive PR **OiR 906-10** (1μm) at 3 krpm, 60 sec
□ Bake wafer at 90°C, 60sec
□ UV exposure using 5x stepper .With vacuum.
exposure time 0**.16 s** (check)
focal number **0**
525μm thick chuck
□ Post-exposure bake at 120°C, 60 sec
□ Develop in **OPD 4262** 40 sec (check)
□ DI water rinse 3 min

II. Evaporation Time: _____

□ Evaporate: Titanium 10nm/ Gold 200nm

III. Liftoff: Using heated AcetoneCE 60min (Actual dip time: _____ hr) + Isopropyl Alcohol

Step 3: Field Etch Date:_____

I. Sample Preparation Time: _____

□ Spin positive Photoresist **OiR 906-10** (1μm) at 3 krpm, 60 sec
□ Bake wafer at 90°C, 60sec
□ UV exposure using 5x stepper .With vacuum. Mask No: 2 (2865030A00)
exposure time 0**.17 s** (check)
focal number **0**
□ Post-exposure bake at 120°C, 60 sec
□ Develop in **OPD 4262** 45 sec
□ DI water rinse 3 min

II. Wet etching **Time: _____**

InAs etchant (acetic acid, hydrogen peroxide and DI water=5:10:100) ~25A/sec
GaSb etchant (hydrogen peroxide: HF: lactic acid .5:.5:100) – 20-25A/sec

InAs: _____ Å	Time: _____5_____ sec
AlSb/GaSb:_____ Å	Time: _____4_____ sec
InAs: _____ Å	Time: _____17_____ sec

□ Alpha Step to make sure field is properly etched (Measured _____ Å)

III. Cleaning: Using heated Acetone 60min (Actual dip time: _____ hr) + Isopropyl Alcohol.

□ Alpha step to verify etch depth

Appendix B

Procedure for InAs SET on Composite Quantum Well

Step 1: Channel and Gate Isolation Trench

I. Sample Preparation Time: _____

□ Solder In dots for secondary electron emission collection and check resistance
□ MAA EL11 5 krpm 60 sec (expected 380-420nm)
□ Pre-bake: 150°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)

II. E-Beam Writing Time: _____

1. 4pt focusing :
□ Check resistance between spring and other In dot (2k Ohms typical)
□ Drop one drop gold solution at each corner of the sample
□ Global angle correction : _____ degrees
□ Focus at each point and run 4pt2.exe to get the fitting plane function
2. E-beam Writing : Runfile name : _____ .rf6 (marker and alpha step)
Line dose : 2.5nC/cm, c-t-c = 43 Å, current ~ 12 pA
Area dose : 225uC/cm^2, c-t-c = 101Å, line spacing = 101 Å, current ~ 12 pA
Actual dose : _____
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ before writing
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ after writing

III. Development Time: _____

□ Develop: MIBK: IPA (1:1) 60 seconds
□ Overlap Rinse: IPA 80 seconds
□ Overlap Rinse: DI water 60 seconds; Blow dry with nitrogen gas

IV. Wet etching Time: _____

InAs Etchant

Recipe: (acetic acid: hydrogen peroxide: DI water / 5:10:100)
Etch Rate: 2.5nm/sec

AlSb/GaSb Etchant

Recipe: Hydrogen Peroxide: 49%Hydroflouric Acid: Lactic Acid / 0.5:0.5:100)
Etch Rate: 2.0-2.5nm/sec
Note: AlSb/GaSb etchant must be stirred just prior to use since the etchant is a suspension that will separate if left unstirred.

InAs: _____ Å Time: _____ sec
Al/GaSb: _____ Å Time: _____ sec
InAs: _____ Å Time: _____ sec
GaSb: _____ Å Time: _____ sec
(AlSb : _____ Å) NO etching here
comments:_____

Rinse etchant between each step and after completion with DI water
Alpha step after each etch to verify etch depth

V. Liftoff: Using heated Acetone 60min (Actual dip time: _____ hr) + Isopropyl Alcohol.

Step 2: Ohmic Contacts and Interconnect Date :_____

I. Sample Preparation Time: _____

□ PMMA-MAA EL11 Spin: 3kRPM, 60sec (thickness ~ 570nm-600nm)
□ Pre-bake: 150°C, 60 sec. w/ vac. (Actual Temp = _____°C, Time = _____s)

II. E-Beam Writing Time: _____

1. 4pt focusing :
□ Check resistance between spring and other In dot (~ 2k ohms typical)
□ Drop one drop gold solution at each corner of the sample
□ global correction : _____ degree
□ Focus at each point and run 4pt2.exe to get the fitting plane function
2. E-beam Writing : Runfile name : _____ .rf6 (marker and alpha step)
Line dose : 2.5nC/cm, c-t-c = 43 Å, current ~ 12 pA
Area dose : 225uC/cm^2, c-t-c = 101Å, line spacing = 101 Å, current ~ 12 pA
Actual dose : _____
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ before writing
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ after writing

III. Development Time: _____

□ Develop: MIBK: IPA(1:1) 60 second
□ Overlap Rinse: IPA 80 sec
□ Overlap Rinse: DI water 60 sec
□ Blow dry: by dry nitrogen gas

IV. Wet etching Time: _____

InAs etchant (acetic acid, hydrogen peroxide and DI water=5:10:100) ~25A/sec
GaSb etchant (hydrogen peroxide: HF: lactic acid .5:.5:100) – 20-25A/sec

InAs: _____ Å Time: _____ sec
Al/GaSb: _____ Å Time: _____ sec
Comments:_____
Rinse etchant between each step and after completion with DI water
Alpha step after each etch to verify etch depth
(This wet etch is performed so that the ohmic contacts can directly contact the quantum well without high temperature annealing)

V. Evaporation Time: _____

□ Evaporate: Germanium 40nm/ Nickle 10nm/ Gold 200nm

VI. Liftoff: Using heated Acetone 60min (Actual dip time: _____ hr) + Isopropyl Alcohal. DI water is not used because water may oxidize the AlSb substrate.

Step 3: Top-gate Name _____Date:_____

I. Sample Preparation Time: _____
□ MAA EL11 3 krpm 60 sec (expected 570nm-600nm)
□ Pre-bake: 150°C, 60 sec. w/ vac. (Actual Temp = _____°C, Time = _____s)

II. E-Beam Writing Time: _____
1. 4pt focusing :
□ Check resistance between spring and other In dot (2Kohms typical)
□ Drop one drop gold solution at each corner of the sample
□ global correction : _____ degree
□ Focus at each point and run 4pt2.exe to get the fitting plane function
2. E-beam Writing : Runfile name : _____ .rf6
Line dose : 2nC/cm, c-t-c = 43 Å, current ~ 12 pA
Area dose : 200-225uC/cm^2, c-t-c = 101Å, line spacing = 101 Å, current ~ 12 pA
Actual dose : _____
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ before writing
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ after writing

III. Development Time: _____
□ Develop: MIBK: IPA (1:1) 60 seconds
□ Overlap Rinse: IPA 80 seconds
□ Overlap Rinse: DI water 80 seconds
□ Blow dry: by dry nitrogen gas

IV. Etch InAS : _____

V. Evaporation Time: _____

Caliberate SiO_2 thickness using test wafer and using reflectance analyzer to verify thickness. The thickness cannot exceed 100nm or the dielectric will crack.
□ Evaporate: SiO_2 100nm / Titanium 10nm /Gold 50nm

V. Liftoff: Using heated Acetone (Actual dip time: _____) + Isopropyl Alcohol. DI water is not used because it may oxidize the wafer.

Alpha step

Step 4: Ohmic Bonding Pads Date:_____

I. Sample Preparation Time: _____
□ Spin positive PR **OiR 906-10** (1μm) at 3 krpm, 60 sec
□ Bake wafer at 90°C, 60sec
□ UV exposure using 5x stepper .With vacuum.
exposure time 0**.16 s** (check)
focal number **0**
525μm thick chuck
□ Post-exposure bake at 120°C, 60 sec
□ Develop in **OPD 4262** 40 sec (check)
□ DI water rinse 3 min

II. Evaporation Time: _____
□ Evaporate: Germanium 40nm/ Nickle 10nm/ Gold 200nm

III. Liftoff: Using heated ACE 60min (Actual dip time: _____ hr) + IPA

IV. Cleaning: Using heated ACE (Actual dip time: _____) + IPA

Step 5: Field Etch Date:_____

I. Sample Preparation Time: _____
□ Spin positive Photoresist **OiR 906-10** (1μm) at 3 krpm, 60 sec
□ Bake wafer at 90°C, 60sec
□ UV exposure using 5x stepper .With vacuum. Mask No: 2 (2865030A00)
exposure time 0**.17 s** (check)
focal number **0**
□ Post-exposure bake at 120°C, 60 sec
□ Develop in **OPD 4262** 45 sec
□ DI water rinse 3 min

II. Wet etching Time: _____

InAs etchant (acetic acid, hydrogen peroxide and DI water=5:10:100) ~25A/sec
GaSb etchant (hydrogen peroxide: HF: lactic acid .5:.5:100) – 20-25A/sec

InAs: _____ Å Time: _____ sec
Al/GaSb: _____ Å Time: _____ sec
InAs: _____ Å Time: _____ sec
GaSb: _____ Å Time: _____ sec
Comments:_____

□ Alpha Step to make sure field is properly etched (Measured _____ Å)

III. Cleaning: Using heated Acetone 60min (Actual dip time: _____ hr) + Isopropyl Alcohol.

Step 6: Gate Bonding Pads Date:_____

I. Sample Preparation Time: _____

□ Spin positive PR **OiR 906-10** at 3 krpm, 60 sec
□ Bake wafer at 90°C, 60sec
□ UV exposure using 5x stepper.With vacuum.
exposure time 0**.17 s**
focal number **0**
□ Post-exposure bake at 120°C, 60 sec
□ Develop in **OPD 4262** 40 sec
□ DI water rinse 3 min

II. Evaporation Time: _____

□ Evaporate: Titanium 10nm/ Gold 250nm

III. Liftoff: Using heated Acetone 60min (Actual dip time: _____ hr) + Isopropyl Alcohol.

Appendix C

Procedure for Intrinsic Silicon Hall Bar with Electron Beam Defined SET

Summary: EBL bottom gates with Photolithography defined top-gate on BCB with Silicon trenches to eliminate gate leakage current

Name:_____ Sample #:_____ Run Name: _____

Step 1: Top-gate Trenches (Device Isolation)

I. Sample Preparation Time: _____

□ Solder In dots for secondary electron emission collection and check resistance
□ Spin PMAA A4 5 krpm 60 sec (expected thickness 180-200nm)
□ Pre-bake resist: 180°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)

II. E-Beam Writing Time: _____

1. 4pt focusing :
□ Check resistance between spring and other In dot (1000 ohms typical)
□ Drop one drop gold solution at each corner of the sample
□ Global angle correction : _____ degree
□ Focus at each point and run 4pt2.exe to get the fitting plane function
2. E-beam Writing : Runfile name : _____ .rf6 : _____ .rf6 : _____
.rf6 : _____ .rf6 : _____ .rf6 (marker and alpha step)
Line dose : 2.5nC/cm, c-t-c = 43 Å, e-beam current ~ 12 pA
Area dose : 2250uC/cm^2, c-t-c = 101Å, line spacing = 101 Å, current ~ 12 pA
Actual dose : _____
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ before writing
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ after writing

III. Development Time: _____

□ Develop: MIBK: IPA(1:1) 80 seconds
□ Overlap Rinse: IPA 80 seconds
□ Overlap Rinse: DI water 80 seconds ;
Blow dry with compressed nitrogen.

V. Dry Etch Time: _____

□ Process "SI1DRH" 1 minute targeting 0.5um depth

VI. Clean Resist: Acetone dip 60 minutes (Actual dip time: _____) + Isopropyl Alcohol rinse +Distilled water rinse. Blow dry with Compressed nitrogen.

Step 2: Surface Gates (Skip if fabricating Hall Bar)

I. Sample Preparation Time: _____

□ Spin MAA EL11 5 krpm 60 sec (expected 380-420nm)
□ Pre-bake: 150°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)
□ Spin PMAA A4 5 krpm 60 sec (expected 180nm)
□ Pre-bake: 180°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)

II. E-Beam Writing Time: _____

1. 4pt focusing :
□ Check resistance between spring and other In dot (1000ohms typical)
□ Drop one drop gold solution at each corner of the sample
□ global correction : _____ degree
□ Focus at each point and run 4pt2.exe to get the fitting plane function
2. E-beam Writing : Runfile name : _____ .rf6 : _____ .rf6 : _____
.rf6 : _____ .rf6 : _____ .rf6 (marker and alpha step)
Line dose : 2nC/cm, c-t-c = 43 Å, current ~ 12 pA
Area dose : 200uC/cm^2, c-t-c = 101Å, line spacing = 101 Å, current ~ 12 pA
Actual dose : _____
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ before writing
□ Pinhole current : _____ pA for CC = ____
_____ pA for CC = ____ after writing

III. Development Time: _____

□ Develop: MIBK: IPA(1:1) 80 seconds running time (1:20)
□ Overlap Rinse: IPA 20 sec running time (1:40)
□ Develop: MIBK: IPA(1:2) 90 seconds running time (3:10)
□ Overlap Rinse: IPA 80 sec running time (4:30)
□ Overlap Rinse: DI water 30 sec ; running time (5:00)
Blow dry with nitrogen gas.

V. Evaporation Time: _____

□ Evaporate: Process # (49) Aluminum 60nm / Titanium 20nm/ Gold 120nm

VI. Clean Resist: Acetone dip 60 minutes (Actual dip time: _____) + Isopropyl Alcohol rinse +Distilled water rinse. Blow dry with Compressed nitrogen.

Step 3: Surface Gate Leads

I. Sample Preparation Time: _____

□ Spin NR-7 1500PY (1.5μm thick) 4000 RPM (Negative resist)

□ Pre-bake: 120°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)

II. Photolithography Time: _____

□ UV exposure using 5x stepper .With vacuum. HB/QPC/Cross "Side-gates":
exposure time: **0.74 sec**
focal adjustment: **0**
450μm thick Chuck
□ Post-bake: 120°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)
□ Develop in **RD-6** 8 sec (this step must be performed with exact timing)
□ DI water rinse 1-2 min

III. Evaporation Time: _____

□ Evaporate: Process # (9) Ti 10nm/ Au 200nm

IV. Liftoff: RR2 resist remover in beaker on hot plate heated to 100C for 10 min. Remove metal with DI spray, Soak another 5 min in heated RR2, Rinse 3 min with DI (repeat 5min soak followed by DI spray until resist is fully removed may take up to 30 min to liftoff properly or if not heated well)

Spin Coat and Bake BCB:

□ Spin AP3000 Adhesion Promoter: Ramp 250rpm/sec to 500RPM. Spin 500rpm for 10sec while applying AP3000 using a fresh glass pipet; Ramp 1000RPM/sec to 3000 RPM for 30 sec)
□ Spin BCB 3022-35 ~1.1um thick (Ramp 250rpm/sec to 500RPM. Spin 500rpm for 10sec while applying BCB using a fresh glass pipet; Ramp 1000RPM/sec to 5000 RPM and spin for 30 sec)
□ Bake: 210°C in N2 oven 60 min (Ramp up to 210°C in 45 min; Bake 60 minutes. Allow sample to cool in tube furnace by ambient heat loss. Should take roughly 4-5 hours total. Leave a note if overnight.

Step 4: Top-gate Photolithography

I. Sample Preparation Time: _____

□ Spin NR-7 1500PY (1.5μm thick) 4000 RPM (Negative resist)
□ Pre-bake: 120°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)

II. Photolithography Time: _____

□ UV exposure using 5x stepper .With vacuum. HB/QPC/Cross "Top-gates":
exposure time: **0.74 sec**
focal adjustment: **0**
450μm thick Chuck
□ Post-bake: 120°C, 60 sec. w/vac. (Actual Temp = _____°C, Time = _____s)

 Develop in **RD-6** 8 sec (this step must be performed with exact timing)
 DI water rinse 1-2 min

III. Evaporation Time: _____
 Evaporate: Process # (9) Ti 10nm/ Au 200nm

IV. Liftoff: RR2 resist remover in beaker on hot plate heated to 100C for 10 min. Remove metal with DI spray, Soak another 5 min in heated RR2, Rinse 3 min with DI (repeat 5min soak followed by DI spray until resist is fully removed may take up to 30 min to liftoff properly or if not heated well)

Step 5: Bonding Pad Via Holes Date:_____

I. Sample Preparation Time: _____
 Spin positive Photo Resist **OiR 908-35** at 3 krpm, 60 sec (4μm thick)
 Bake wafer at 90°C, 3 min
 UV exposure using 5x stepper .With vacuum. Mask No: 2 (2865030A00)
exposure time **0.37sec** (check)
focal number **0**
 Develop in **OPD 4262** 90 sec
 DI water rinse 3 min

II. Dry Etch Time: _____

 Remove BCB using "5C20O300" for 4:30 min
Check under optical microscope to verify that BCB is completely removed.

III. Wet Etch for ohmic
 Wet Etch BOE 6:1 for 75 seconds (no longer than 2 min or the photoresist mask will be compromised) Make sure Air bubbles are gone from surface at features.

IV. Clean Resist: Acetone dip 60 minutes (Actual dip time: _____) + Isopropyl Alcohol rinse +Distilled water rinse. Blow dry with compressed nitrogen.

References

[1] C. Kittel, Introduction to Solid State Physics 7'th Edition, John Wiley and Sons, Inc. (1996).

[2] N.W. Ashcroft, N.D. Mermin, Solid State Physics, Saunders College Publishing, (1976).

[3] S.M. Sze, Physics of Semiconductor Devices 2'nd Ed., John Wiley and Sons, 1981

[4] T. Ando, A. B. Fowler and F. Stern, *Electronic properties of two-dimensional systems* Rev. Mod. Phys. 54, 437–672 (1982).

[5] Y. Imry, Introduction to Mesoscopic Physics, Oxford University Press, 1997

[6] S. Datta, Electronic Transport in Mesoscopic Systems, Cambridge University Press, 1995.

[7] L.P. Kouwenhoven, C.M. Marcus, P.L. Mceuen, S. Tarucha, R.M.Westervelt, N.S. Wingreen, "Electron Transport in Quantum Dots," to be published in the proceedings of the Advanced Study Institute on *Mesoscopic ElectronTransport*, edited by L.L. Sohn, L.P. Kouwenhoven, G. Schön (Kluwer 1997).

[8] L.P. Kouwenhoven, D.G. Austing and S. Tarucha, "Few-electron Quantum Dots," Rep. Prog. Phys. 64, 701-736 (2001).

[9] Y. Ono, A. Fujiwara, K. Nishiguchi, H. Inokawa, Y. Takahashi, "Manipulation and detection of single electrons for future information processing," *Jap. J. Appl. Phys.* 97, 031101 (2005).

[10] P. Hadley, Günther Lientschnig, and Ming-Jiunn Lai, "Single-Electron Transistors," Proceedings of the International Symposium on Compound Semiconductors (2002).

[11] M. S. Skolnick, K. J. Nash, S. J. Bass, P. E. Simmonds and M. J. Kane, Photoluminescence study of the density-of-states between Landau levels in the quantum hall effect system," *Solid State Communications*, vol. 67, pp. 637-641 (1988).

[12] M. Prunnila et al., "Silicon quantum point contact with aluminum gate," Materials Science and Engineering B vol. 74 pp. 193-196 (2000)

[13] A. S. Plaut, H. Lage, P. Grambow, D. Heitmann, K. von Klitzing, and K. Ploog "Direct magneto-optical observation of a quantum confined one-dimensional electron gas," Phys. Rev. Lett. 67, 1642–1645 (1991).

[14] G.L. Timp, R.E. Howard, *Quantum Mechanical Aspects of Transport in Nanoelectronics* Proceedings. Of The IEEE, **79**, no 8 1118-1207 (1991).

[15] B. J. van Wees et al., "Quantized Conductance in a Two-dimensional Electon Gas," *Phys. Rev. Lett.* vol. 60 pp. 848-850 (1988).

[16] K. Brunner, U. Bockelmann, G. Abstreiter, M. Walther, G. Böhm, G. Tränkle, and G. Weimann, "Photoluminescence from a single GaAs/AlGaAs quantum dot," Phys. Rev. Lett. vol. 69, pp. 3216–3219 (1992).

[17] M.A. Kastner, "The Single-electron Transistor," Rev. Mod. Phys. vol. 64, pp. 849–858 (1992).

[18] K. K. Likharev, "Single Electron Devices and their Applications," *Proc. IEEE* vol. 87, pp. 606-632, (1999).

[19] S.M. Goodnick, and J. Bird, "Quantum-Effect and Single-Electron Devices," *IEEE Transactions On Nanotechnology,* vol. 2, pp. 368-385 (2003).

[20] J. Nitta, F. Meijer, Y. Narita, and H. Takayanagi, "Gate voltage-dependent Aharanov-Bohm experiment in the presence of Rashba spin-orbit interaction," *Physica E,* vol. 6, pp. 318-321 (2000).

[21] A.M. Song, A. Lorke, A. Kriele, J.P. Kotthaus, W.Wegscheider, and M. Bichler, "Nonlinear electron transport in an asymmetric microjunction: A ballistic rectifier," *Phys. Rev. Lett.,* vol. 80, pp. 3831–3834, (1998).

[22] L.L. Chang, L. Esaki, and R Tsu, "Resonant tunneling in semiconductor double barriers,**"** *Appl. Phys. Lett.,* vol. 24, pp. 593-595 (1974).

[23] S. Datta, and B. Das, "Electronic analog of the electro-optic modulator," *Appl. Phys. Lett.*, vol. 56, pp. 665-667, Feb. 1990.

[24] H. Linke, et al. "Quantum ratchets and quantum heat pumps," *Appl. Phys. A,* vol.75, pp. 237-246, (2002)

[25] Y. Aharonov and D. Bohm, "Significance of Electromagnetic Potentials in the Quantum Theory," *Phys. Rev.* vol. 115, pp. 485-491 (1959).

[26] C. H. Yang, M. J. Yang, K. A. Cheng, and J. C. Culbertson, "Characterization of one-dimensional quantum channels in InAs/AlSb," *Phys. Rev. B* vol. 66, pp. 115306-115313 (2002).

[27] T. Palm and L. Thylén, Analysis of an Electron-wave Y-branch Switch, App. Phys. Lett. 60, pp. 237-239 (1992).

[28] L. Thylen, and C. M. Lee, *Beam-propagation method based on matrix diagonalization,* J. Opt. Soc. Am. A,Vol. 9, No. 1, pp. 142-146 (1992).

[29] T. Palm, L. Thylen, O. Nilsson, and C. Svensson, "Quantum interference devices and field-effect transistors: A switch energy comparison," *J. Appl. Phys.* vol. 74, pp. 687-694 (1993).

[30] L. Thylen, and O. Sahlen, "Switch energy analysis of quantum interference directional couplers," *IEEE Journal Quant. Electron.* vol. 28, pp. 31-32 (1992).

[31] E. Forsberg, "Influence of space charge on gate control of electron waveguide Y-branch switches in the coherent regime," *J. Appl. Phys.* vol. 93, pp. 5687-5690 (2003).

[32] I. Shorubalko, H. Q. Xu, I. Maximov, P. Omling, L. Samuelson, and W. Seifert, "Nonlinear operation of GaInAs/InP-based three-terminal ballistic junctions," *Appl. Phys. Lett.* Vol. 79, pp. 1384-1386 (2001).

[33] L. Worschech, B. Weidner, S. Reitzenstein, and A. Forchel, "Investigation of switching effects between the drains of an electron Y-branch switch,"*Appl Phys. Lett.* vol. 78, pp. 3325-3327 (2001).

[34] L. Worschech, H. Q. Xu, A. Forchel, and L. Samuelson, "Bias-voltage-induced asymmetry in nanoelectronic *Y*-branches," *Appl Phys. Lett.* vol. 79, pp. 3287-3289 (2001).

[35] K. Hieke and M. Ulfward, "Nonlinear operation of the Y-branch switch: Ballistic switching mode at room temperature," *Phys. Rev. B* vol. 62, pp. 16727-16730 (2000).

[36] A.M. Song, P. Omling, L. Samuelson, W. Seifert, I. Shorubalko, and H. Zirath, "Operation of InGaAs/InP-Based Ballistic Rectifiers at Room Temperature and Frequencies up to 50 GHz," *Jpn. J. Appl. Phys.* vol. 40, L909-L911 (2001).

[37] J. Mateos, B. G. Vasallo, D. Pardo, T. González, J.-S. Galloo, S. Bollaert, Y. Roelens, and A. Cappy, "Microscopic modeling of nonlinear transport in ballistic nanodevices," *IEEE Tr.* Ed. 50, pp. 1897-1905 (2003).

[38] S. J. Koester, B. Brar, C. R. Bolognesi, E. J. Caine, A. Patlach, E. L. Hu, and H. Kroemer**, "**Length dependence of quantized conductance in ballistic constrictions fabricated on InAs/AlSb quantum wells," *Phys. Rev. B,* vol. 53, pp. 13063-13073 (1996).

[39] K. A. Cheng, C. H. Yang, and M. J. Yang, "Nanometer-scale quantum channels defined by reactive ion etching in InAs/AlSb heterojunctions,"*Appl. Phys. Lett.* vol. 77, pp. 2861-2863 (2000).

[40] K. A. Cheng, C. H. Yang, and M. J. Yang, "Nanometer-size InAs/AlSb quantum wires: Fabrication and characterization of Aharonov–Bohm quantum rings," *J. Appl. Phys.* vol. 88, pp. 5272-5276 (2000).

[41] T. H. Chang, C. H Yang, and M. J. Yang, "STM Observation of Single Electron Charging in 70 nm InAs Quantum Dots," *Physica Status Solidi B,* vol. 224, pp. 693-696 (2001).

[42] A. Yasaka, "Feasibility Study of Spatial-Phase-Locked Focused-Ion-Beam Lithography," Master's Thesis, MIT pp. 31 (1995).

[43] G. Timp, H.U. Baranger, P. deVegvar, J.E. Cunningham, R. E. Howard, R. Behringer, and P.M. Mankiewich, **"**Propagation around a Bend in a Multichannel Electron Waveguide," *Phys. Rev. Lett.* vol. 60, pp. 2081-2084 (1988).

[44] G. M. Jones, M.J. Yang, and C.H. Yang, private communication.

[45] C. W. J. Beenakker and H. van Houten, *Solid State Physics*, vol. 44, Eds. H. Ehrenreich and D. Turnbull, (Academic Press, Boston 1991).

[46] It is possible that a large asymmetry in the device might produce a negative voltage through purely classical transport.

[47] K.K. de Vries, P. Stelmaszyk, and A.D. Wieck, "Intrinsic and extrinsic capacitances of in-plane-gated transistors," *J. Appl. Phys.* vol. 79, pp. 8087-8090 (1996).

[48] J-O. Wesstrom, "Self-Gating Effect in the Electron Y-Branch Switch," *Phys. Rev. Lett.* vol. 82, pp. 2564-2567 (1999).

[49] S. Reitzenstein, L. Worschech, P. Hartmann, M. Kamp, and A. Forchel, "Capacitive-Coupling-Enhanced Switching Gain in an Electron Y-Branch Switch," *Phys. Rev. Lett.* vol. 89, pp. 226804-226807 (2002).

[50] Mesoscopic Phenomena in Solids, edited by B.L. Altshuler, P.A. Lee and R.A. Webb. (North-Holland, Amsterdam, New York, 1991).

[51] T. Palm, "Self-consistent calculations of an electron-wave Y-branch switch," *J. Appl. Phys.* vol. 74, pp. 3551-3557 (1993).

[52] T. Palm, "Prediction of sawtooth oscillations in an electron Y-branch switch," *Phys. Rev. B* vol. 52, pp. 13773-13775 (1995). This simulation of a multiple mode YBS

shows an in-phase oscillatory conductance versus a sweeping gate bias, and this feature is explained by mode occupation. In contrast, we observed out-of-phase oscillatory conductances in the presence of multiple modes.

[53] Y. Takahashi, Y. Ono, A. Fujiwara, H. Inokawa, "Silicon Single-electron Devices," *J. Phys.: Condens. Matter* vol.14, pp. R995–R1033 (2002).

[54] K. K. Likharev, N. S. Bakhvalov, G. S. Kazacha, and S. I. Serdyukova, "Single-electron tunnel junction array: an electrostatic analog of the Josephson transmission line," *IEEE Trans. Magnetics*, 25, pp. 1436–1439, (1989).

[55] P.W. Shor, *J. Sci. Statist. Comput.* vol. 26, pp. 1484 (1997).

[56] M. A. Nielsen, I. L. Chuang, "Quantum Computation and Quantum Information," Cambridge University Press, (2000).

[57] D. Loss and D. P. DiVincenzo, **"**Quantum computation with quantum dots," *Phys. Rev. A* vol. 57, pp. 120-126 (1998).

[58] T. Hatano, M. Stopa, T. Yamaguchi, T. Ota, K. Yamada, and S. Tarucha, "Electron-Spin and Electron-Orbital Dependence of the Tunnel Coupling in Laterally Coupled Double Vertical Dots," *Phys. Rev. Lett.* vol. 93, pp. 066806 (2004).

[59] S. Tarucha, D. G. Austing, T. Honda, R. van der Hage and L. P. Kouwenhoven, "Atomic-Like Properties of Semiconductor Quantum Dots," *Japan. J. Appl. Phys.* vol. 36, pp. 3917-3923 (1997).

[60] M. Ciorga, A. S. Sachrajda, P. Hawrylak, C. Gould, P. Zawadzki, S. Jullian, Y. Feng, and Z. Wasilewski**, "**Addition spectrum of a lateral dot from Coulomb and spin-blockade spectroscopy," *Phys. Rev. B* vol. 61, pp. R16315-R16318 (2000).

[61] J. M. Elzerman, R. Hanson, J. S. Greidanus, L. H. Willems van Beveren, S. De Franceschi, L. M.K. Vandersypen, S. Tarucha, and L.P. Kouwenhoven, "Few-electron quantum dot circuit with integrated charge read out," *Phys. Rev. B* vol. 67, pp. R161308-R161311 (2003).

[62] T. H. Oosterkamp, S. F. Godijn, M. J. Uilenreef, Y. V. Nazarov, N. C. van der Vaart, and L.P. Kouwenhoven, "Changes in the Magnetization in a of a Double Quantum Dot," *Phys. Rev. Lett.* vol. 80, pp. 4951-4954 (1998).

[63] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, A. C. Gossard, "Coherent Manipulation of Electron Spins in Semiconductor Quantum Dots," *Science* vol. 309, pp. 2180-2184 (2005).

[64] S. Tarucha, D.G. Austing, T. Honda, R.J. vander Hage, and L.P. Kouwenhoven, "Shell Filling and Spin Effects in a Few Electron Quantum Dot," *Phys. Rev. Lett.* vol. 77, pp. 3613-3616 (1996).

[65] L.P. Kouwenhoven, T.H. Oosterkamp, M.W.S. Danoesastro, M. Eto, D.G. Austing, T. Honda, and S. Tarucha, "Excitation Spectra of Circular, Few-Electron Quantum Dots," *Science* vol. 278, pp. 1788-1792 (1997).

[66] T. Fujisawa, T.H. Oosterkamp, W.G. van der Wiel, B.W. Broer, R. Aguado, S. Tarucha, and L.P. Kouwenhoven, "Spontaneous Emission Spectrum in Double Quantum Dot Devices," *Science* vol. 282, pp. 932-935 (1998).

[67] R. de Sousa, and S. Das Sarma, "Electron spin coherence in semiconductors: Considerations for a spin-based solid-state quantum computer architecture," *Phys. Rev. B* vol. 67, 033301-033304 (2003).

[68] L.M.K. Vandersypen, R. Hanson, L.H. Willems van Beveren, J. M. Elzerman, J.S. Greidanus, S. De Franceschi, L. P. Kouwenhoven, http://arxiv.org/abs/quant-ph/0207059.

[69] M.J. Yang, F.C. Wang, C.H. Yang, B.R. Bennett, and T.Q. Do, "A Composite Quantum Well Field-Effect Transistor," *Appl. Phys. Lett.* vol. 69, pp. 85-87 (1996).

[70] B.H. Hu, C.H. Yang, and M.J. Yang, "On-Demand Single-Photon Source using a Nanoscale Metal-Insulator-Semiconductor Capacitor," *Nanotechnology* vol. 16, pp. 1354-1357 (2005).

[72] G. Feher, "Electron Spin Resonance Experiments on Donars in Silicon. I. Electronic Structure of Donars by the Electron Nuclear Double Resonance Technique," *Phys. Rev.* vol. 114, pp. 1219-1244 (1959); A. M. Tyryshkin, S. A. Lyon, A. V. Astashkin, and A. M. Raitsimring, "Electron Spin Relaxation Times of Phosphorus Donors in Silicon," *Phys. Rev. B* vol. 68, pp. 193207 (2003).

[73] A. Fujiwara, Y. Takahashi, and K. Murase, "Asymmetric tunnel barrier in a Si single-electron transistor, MicroelectronicEngineering," Microelectronic Engineering vol. 47, 197-199 (1999).

[74] L.J. Klein, K.A. Slinker, J.L. Truitt, et al., "Coulomb Blockade in a Silicon/Silicon-Germanium Two-dimensional Electron Gas Quantum Dot," *Applied Physics Letters* vol.84, pp. 4047-4049 (2004).

[75] K.A. Slinker, K.L.M. Lewis, C.C Haselby et al., "Quantum Dots in Si/SiGe 2DEGs with Schottky Top-gated Leads," New J. Phys. vol. 7, pp. 246 (2005).

[76] M.R. Sakra, H.W. Jiang, E. Yablonovitch, and E. T. Croke, "Fabrication and Characterization of Electrostatic Si/SiGe Quantum Dots with an Integrated Read-out Channel," *Applied Physics Letters* vol. 87, pp. 223104 (2005).

[77] F. H. L. Koppens, J. A. Folk, J. M. Elzerman, et al., Science 309, 1346-1350 (2005); and J.R. Petta, A.C. Johnson, J.M. Taylor, E.A. Laird, A. Yacoby, M.D. Lukin, C.M. Marcus, M. P. Hanson, A.C. Gossard, "Coherent Manipulation of Electron Spins in Semiconductor Quantum Dots," *Science* vol. 309, pp. 2180-2184 (2005).

[78] B.E. Kane, L.N. Pfeiffer, and K.W. West, "High mobility GaAs heterostructure field effect transistor for nanofabrication in which dopant-induced disorder is eliminated," Applied Physics Letters 67, 1262 (1995).

[79] B.E. Kane, L.N. Pfeiffer, and K.W. West, "Variable density high mobility two-dimensional electron and hole gases in a gated GaAs/Al*x*Ga1–*x*As heterostructure," Applied Physics Letters 63, 2132 (1993).

[80] Software downloaded from http://www.srim.org/

[81] Data sheets can be found at http://www.dow.com/cyclotene/solution/elecprop.htm

[82] See website http://mail.mems-exchange.org/pipermail/mems-talk/2006-May/140077.html

[83] The deviation (Δg) of electron g-factor from its free-electron value, g=2.0023, is due to spin-obit coupling, and consequently, is one measure of spin-obit coupling strength of the system. That is, $g= g_0-\Delta g$. For bulk silicon, the g* value is around 2, i.e., $\Delta g \sim 0.0023$. In comparison, the electron g-factor in GaAs is –0.44, indicating $\Delta g \sim 2.44$. R. J. Elliot, Phys. Rev. 96, 266 (1954).

[84] I. Zutic, J. Fabion, S. Das Sarma, "Spintronics: Fundamentals and applications," Section III of Rev. Mod. Phys. 76, 323 (2004) and references therein.