

## ABSTRACT

Title of dissertation: MEASUREMENTS OF CHARGE MOTION IN SILICON  
WITH A SINGLE ELECTRON TRANSISTOR: TOWARD  
INDIVIDUAL DOPANT CONTROL

Kenton Randolph Brown, Doctor of Philosophy, 2005

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I present the results of experimental investigations into single electron transistors made on doped silicon substrates, with the ultimate goal of individual dopant manipulation at millikelvin temperatures. The sensitivity of single electron transistors to local charge motion should enable observations of single donor ionization. Here I formulate a model for the electrostatic control of a donor electron near an oxide interface and describe a device geometry that should enable its measurement. I give data from several Al-AlO<sub>x</sub>-Al single electron transistors below 100 mK that provide evidence for field-induced dopant ionization, as well as for the motion of individual charges whose origins are not yet understood. I also describe a cryogenic scanning force microscope that I built to measure large arrays of single electron transistors.

MEASUREMENTS OF CHARGE MOTION IN SILICON WITH A SINGLE  
ELECTRON TRANSISTOR: TOWARD INDIVIDUAL DOPANT CONTROL

by

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## Chapter 1

### Introduction

#### 1.1 Manipulating and sensing charges on the atomic scale

The continued scaling down of semiconductor device technology to the nanometer scale and smaller is rapidly approaching a regime in which the location of individual dopants, rather than their spatial density alone, will play a critical role.[1] Appealing quantum computing proposals have been put forward that rely on the sensing and manipulation of individual impurities as quantum bits.[2, 3] Experiments whose goals include the control and measurement of distinct impurities also have merit as tests of semiconductor physics at the atomic level. One such experiment would be the controlled electric field ionization, recapture, and sensing of a phosphorus donor electron near an oxide interface in silicon.

At temperatures much lower than the binding energy of the donor and in zero electric field an electron will remain confined near the impurity nucleus for long periods of time. Upon application of sufficient electric field the electron will be ripped from the nucleus; if nothing exists to block its passage the electron will then be accelerated by the field and will escape. If instead a barrier were placed in its path the electron would stop and remain localized near the barrier until the electric field was reduced, at which point it would return to the donor site. A nearby single electron transistor (SET), one of the most sensitive electrometers invented, should be able to measure this transfer of just one electron between the donor site, the barrier, and back again.

A single electron transistor is a three terminal electronic device of nm dimensions that is exceedingly sensitive to its local electrostatic environment. It consists of a metallic island weakly coupled via tunnel junctions to source and drain leads and capacitively cou-

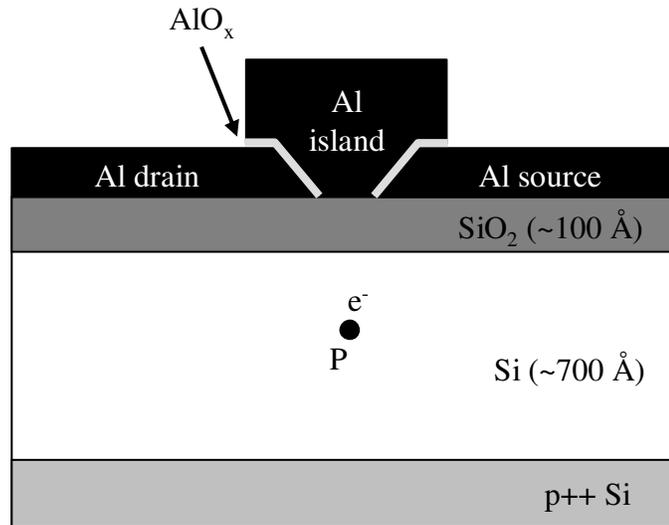


Figure 1.1: Schematic of a P donor in Si measured with an SET. The P atom is embedded in an intrinsic region of Si which is isolated from the metallic SET above it by a thin barrier of SiO<sub>2</sub>. A voltage applied between the heavily doped Si substrate below and the SET above creates an electric field that can ionize the donor and transfer one of its electrons to the Si/SiO<sub>2</sub> interface. (Modified from Reference [4].)

pled to one or more gates. The island is made small enough that at low temperatures the energy required to add one more electron to it exceeds the energy of thermal fluctuations, so that at small drain-source biases there can be no current in a phenomenon known as Coulomb blockade. In this operating regime the current through the device is strongly modulated by the voltage on the gate and by the movement of nearby charges, such as the motion of an adjacent donor electron.

My efforts to measure the controlled ionization of isolated donor electrons in Si using a metallic SET on the wafer surface constitute the bulk of this dissertation. I was motivated by the structure shown in Figure 1.1, consisting of an Al SET directly above a P impurity in Si and separated from the bulk crystal by a thin layer of SiO<sub>2</sub>. The simplest (albeit least controlled) method of creating this structure is to fabricate a large number of SETs on a randomly doped wafer and, by measuring each SET in turn, to look for those SETs that are properly aligned above a donor. This is the route I chose to

pursue, simply because I do not have available a technology for single dopant placement or imaging. There was also some hope when these experiments began that this would be the quickest path to creating a working device, and this is still the case, as no one has yet unambiguously demonstrated control and sensing of an isolated donor in Si. There are a number of challenges that must be surmounted to reach the goal of sensing an individual donor which include: measuring a large number of SETs with high bandwidth over a reasonable span of time, designing a device geometry that allows for independent control of the SET and of the donor, including in the design some way of insuring that the donors are occupied at low temperatures, and ruling out other sources of charge motion near the SET that could disguise the signal of interest. All of these are discussed in the following chapters.

## 1.2 Dissertation outline

Chapter 2 starts with a brief introduction to quantum computing and qubits. I give a synopsis of some existing ideas for using P donors in Si as qubits and for measuring spins of impurities in semiconductors by way of spin-charge conversion and charge measurement with an SET. These ideas are the driving stimulus for our efforts to measure individual donor ionization. Then I present a more thorough discussion of the difficulties such an experiment must surmount and review the relevant literature showing progress in certain areas.

In Chapter 3 I give an abbreviated presentation of the effective mass theory for P donors in Si, and I solve the Schrödinger equation for an electron near a barrier in a constant electric field. Combining these two I obtain an estimate of the electric field required to ionize a donor 30 nm below the barrier, and I find good agreement with a more thorough theoretical result that was published only recently.[5] Using a quadratic approximation for the potential, I get an estimate of how strongly an electron near a barrier

is confined in the lateral direction by an ionized donor nucleus beneath it, and here too I obtain good agreement with a more careful treatment. These estimates are important to show that it is at least theoretically possible to control the motion of an electron between donor and interface states with an electric field. Then I change topics and discuss some considerations for the single electron transistors I used to try to measure this motion. In particular I discuss how to gate an SET for maximum sensitivity without affecting a donor beneath it and how to apply a uniform electric field to donors in a randomly doped substrate. I finish with a prediction of how sensitive our SET will be to the motion of nearby charges, supporting the idea that signals from a donor will not be obscured by noise.

In Chapter 4 I present our recipe for making SETs and associated gating structures on a doped Si substrate. Most of the fabrication steps are relatively standard, but I have developed a novel resist/metallization stack that enabled me to combine photolithography and electron beam lithography during a single evaporation, and I cover that in some detail. I outline my recipe for making a back gate by implanting a dense layer of acceptors, and I present a technique for gating the SETs with a macroscopic gate far above the wafer surface. The chapter closes with a brief discussion of our refrigerator, wiring, instrumentation, and measurement techniques.

Chapter 4.3.3 starts with some data from an early SET design, on various substrates, which give some indication of gross charge motion under an applied electric field. I also show data obtained from these SETs using a lock-in technique that provides evidence for the motion of *individual* charges. I then present some capacitance-voltage measurements of large capacitors and compare the results to those from a newer SET design with a back gate. These results confirm earlier estimates of the back gate doping level in these samples, and they show that the SET geometry has capacitances close to expected values. Next I introduce P donor doping into this newer geometry and see how that changes things; while there is clear qualitative evidence that the doping has an effect at higher

densities, lower densities are less conclusive. I find some hints of the motion of individual charges in all of these samples, but I conclude with some data that I believe rules out donor electrons as the source of this charge motion.

Chapter 5 is a digression from the other chapters. Here I present a design for a millikelvin scanned probe, based on a quartz tuning fork, that we built in order to measure large numbers of SETs. The design incorporates a low noise cryogenic transimpedance amplifier that we also designed. I discuss some of the complications involved in force imaging with this tuning fork probe, show an image taken with the microscope at 190 mK, and present measurements of an SET taken with the probe at 60 mK. I finish with some thoughts on obstacles that will need to be overcome before this scanned probe becomes a practical technology.

Chapter 6 is the conclusion to the dissertation. I discuss what facts we can confidently extract from the data, consider the challenges that remain, and give some ideas for future directions of investigation.

## Chapter 2

### Quantum computing motivations and literature review

#### 2.1 Quantum computing

The idea of trying to build a computer that explicitly takes advantage of the quantum nature of the world is an idea that has developed rapidly in the past decade, although it is not a new one. Both Paul Benioff and Richard Feynman were already toying in the early 1980's with the idea that the principles of quantum mechanics could have applicability toward computation.[6, 7] David Deutsch is generally credited with presenting the first real model for what we would today call a quantum computer.[8] Yet it was not until 1994, when Peter Shor proposed a quantum algorithm for factoring integers,[9] followed shortly by Lov Grover's search algorithm in 1996,[10] both of which were far more efficient than their classical counterparts and have applicability to real-world problems, that the field of quantum computing really took off.

A quantum computer in its simplest form is a quantum mechanical system with a tunable Hamiltonian. It is prepared in some arbitrary quantum state and allowed to evolve according to a possibly time-dependent and adjustable Hamiltonian, resulting in some final state. The state is then measured or "read-out". In general there can be a number of possible results from measurement of the final state, each of which could be measured with a certain probability, according to the principles of quantum mechanics. This is in contrast with a classical computer, which is a classical system that also evolves according to some tunable Hamiltonian, but which ends in a well-defined classical state whose measurement would always lead to the same result.

In practice we imagine a more concrete form for the quantum computer that consists of many quantum bits, or qubits, manipulated and coupled together with quantum gates.

The qubits are the fundamental building blocks of the computer, analogous to the bits of a classical computer. Each qubit is a two-level quantum system. In contrast with classical bits a qubit is allowed not only the states  $|0\rangle$  and  $|1\rangle$  but also any arbitrary superposition  $\alpha|0\rangle + \beta|1\rangle$ . The quantum gates are analogous to the gates in a classical computer, with single qubit gates acting on the state of only one qubit and two qubit gates acting on two qubits simultaneously. Physically the gates are time-dependent controlled perturbations of the system Hamiltonian which change the time evolution of the qubit states.

The difficulties involved in fabricating a practical quantum computer stem from the fragile and sensitive nature of the state of the qubits. In theory the qubits are assumed to be isolated quantum systems whose dynamics are completely determined, to arbitrary precision, the gating operations. In reality it seems that any system of quantum gates will have design imperfections that limit the precision to which the qubits can be manipulated. Furthermore, no quantum system can ever be completely isolated from its surrounding environment, which acts as an additional perturbation to the system Hamiltonian. Due to these unwanted effects, which we call decoherence, the state of a qubit may differ greatly from the desired state after a certain number of gate operations or a certain period of time. This characteristic time period for which the system has been phase coherent is called the decoherence time of the qubit.

Until 1996 it was believed by a few researchers that decoherence would make a practical quantum computer impossible to build. That was a landmark year for the field, when a series of papers showed that fault-tolerant quantum computation would be possible with appropriate error correcting codes, provided that the decoherence rate was not too high.[11] Since that time there has been an explosion of experimental research in the area of quantum computing, with different groups trying to show if a particular qubit candidate has a low decoherence rate and is “scalable”, meaning that building a computer with many qubits should not be exponentially more difficult than building a system with only a few. All of this interest has provided fertile ground for the study of simple quantum

mechanical systems, both theoretically and experimentally, as well as for research into the fundamental quantum properties of a wide range of systems.

## 2.2 Qubit proposals and comparisons

Researchers have proposed everything from the atomic levels of an atom in a trap[12] to the quantum states of an electron floating on a liquid helium surface for use as a qubit,[13] and almost every week there seems to be another qubit proposal. One reason there have been so many qubit ideas is that there are several requirements that must be met for a physical system to be a good qubit, and some of these requirements are conflicting. The system needs to be well isolated from its environment to insure a long decoherence time, yet the better isolated it is the harder it becomes to manipulate and to measure its quantum state. Furthermore, it is not enough to build a single qubit with a long decoherence time and a fast measurement time; to build a useful quantum computer it must be possible to assemble many qubits into a form in which they can interact efficiently: the system must be scalable. As an example of a qubit that works well only in small numbers consider the beautiful experiment by Vandersypen *et al.* from 2001, in which they factored the number 15 using a seven qubit quantum computer based on nuclear magnetic resonance.[14] Nuclear spins are nearly ideal qubits from the perspective of decoherence, with coherence times even as long as days at low temperatures, but they are very difficult to measure because their magnetic moment is so tiny. This experiment and others of its type have been successful because they used a large ensemble of molecules in solution, not a single molecule, to make their measurements, which amplifies the signal from the spins, but such a computer is not scalable. The molecule they used to factor 15 was tailor made with seven nuclei carefully arranged to have favorable interaction strengths. Adding another nucleus to increase the number of qubits would be nearly impossible without redesigning the entire molecule.

Many researchers believe that the first useful quantum computer will be built instead in a solid state system, perhaps because it is easier to imagine using the fabrication technology of today's microprocessor industry to build quantum circuits in solids than it is to imagine inventing a completely new technology for, say, individually manipulating many ions in a trap with lasers. From this perspective, the spins both of electrons and of nuclei associated with substitutional impurities in Si are compelling for several reasons. Foremost is that Si processing is the most well-established computer fabrication technology today, with a near monopoly on the microchip industry. Furthermore, spins in Si can have a relatively long coherence time compared with other semiconductors: recent measurements on ensembles of spins have shown that the coherence time of electron spins for P donors in isotopically enriched  $^{28}\text{Si}$  is as long as 62 ms,[15] while for the nuclei it should be even longer. Measuring such a long coherence time was only possible because the Si had been enriched with  $^{28}\text{Si}$ , an isotope without any nuclear spin. In contrast, a different measurement, now in isotopically enriched  $^{29}\text{Si}$  which has nuclear spin  $\frac{1}{2}$ , gave a coherence time under  $10\ \mu\text{s}$  due to decoherence from nuclear spins interacting with the electrons.[16] A coherence time as long as tens of ms will be more difficult to achieve in GaAs, another popular semiconductor for qubit experiments and the closest competitor for Si in the microchip industry, because there exist no nuclear spin-free isotopes of Ga or As. The spin-orbit interaction is also much weaker in Si than in GaAs, as evidenced by gyromagnetic ratios of 2.0 and -0.4 respectively, and this will lead to even more decoherence in GaAs. On the other hand, GaAs has a major advantage in that it can be lattice matched with AlGaAs to form a nearly defect-free barrier to confine electrons, while the best barrier that can be built for Si today is amorphous thermal oxide, which has a large density of defects associated with it. These defects may prove to be a serious disadvantage for Si as a qubit environment, and at least one group is investigating SiGe as a possible alternative to  $\text{SiO}_2$  for a low-defect barrier compatible with Si technology.[17]

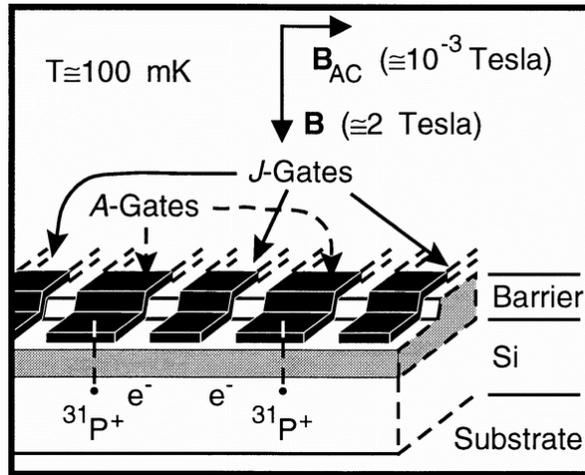


Figure 2.1: Schematic of the Kane quantum computer. A two-dimensional array of P donors in Si is separated by a barrier from metal control gates on the surface. The A gates control the position of the donor electrons relative to their nuclei, while the J gates control the electron-mediated coupling strength between adjacent nuclei. (Reprinted from Reference [2].)

### 2.3 P donor qubits in Si

Encouraged by the many advantages that he saw for using P donors in Si as qubits, Bruce Kane published a landmark paper in 1998 in which he laid out a proposal not for just a single qubit but for an entire scalable quantum computing architecture founded upon Si microfabrication technology.[2, 3] In Figure 2.1 I have reprinted from that paper a schematic of the architecture he envisioned. In this architecture the nuclear spin of the P donor represents the qubit, while interactions between the nuclear and electronic spins represent the gates. Operating the computer at temperatures below 100 mK ensures that the electrons occupy a non-degenerate ground state in the 2 T static magnetic field. Each A gate controls the hyperfine interaction between a donor's electron and its nuclear spin; the hyperfine transition frequency is brought into resonance with an applied AC magnetic field to induce nuclear spin flips, which process represents the single qubit gate operation. The J gate controls the overlap between adjacent donor electrons and thereby mediates

the exchange interaction between them. Combined with the hyperfine interaction, turning on and off the exchange coupling causes selective rotation of one nuclear spin based on the state of the other, which process represents the two qubit gate. The final state of each qubit is read out using a two step process. First the nuclear spin state is transferred to two adjacent donor electrons via the hyperfine interaction and appropriate gate biasing, so that the spin up and down states of the nucleus evolve into spin singlet  $|\downarrow\downarrow\rangle$  and triplet  $|\uparrow\downarrow - \downarrow\uparrow\rangle$  states of the two electrons, respectively. Second, the spin state of the electrons is determined by looking at the polarizability of the two electron system. In the case that the electrons are triplet, it is possible for both of them to become bound to the same donor nucleus in a weak  $D^-$  state, but no such state exists for a spin singlet. Appropriate biasing of the gates can therefore lead to charge motion of the electrons between donor sites in the case of a spin triplet only, so that a measurement of this charge motion would determine the spin state through “spin-charge conversion”. In Kane’s original paper he observes that this motion could be observed via sensitive capacitive techniques involving a HEMT.[18] Since Kane’s original paper it has become clear that single electron transistors (SETs) are far more sensitive charge detectors than HEMT’s and are thus potentially better suited to measuring such a small charge signal.

Verifying the feasibility of the spin-charge conversion measurement scheme is a clear initial priority toward establishing the practicality of a Kane quantum computer, and in 2000 Kane and others proposed a simpler experiment using an SET for that purpose.[4] Rather than trying to measure the spin of a single P donor in Si by coupling it to its neighbors, they imagined instead differentiating the singlet/triplet state of a Te double donor through a similar technique. The system they proposed, schematically shown in Figure 2.2, is difficult to fabricate but simple to imagine. It comprises an SET on an oxidized Si substrate. 150 Å beneath the oxide is a Te impurity, and 500 Å beneath that is an abrupt interface separating the intrinsic Si crystal from a heavily p-doped region below, used as a back gate. Te in Si is a two-electron donor with a spin-singlet ground state, each

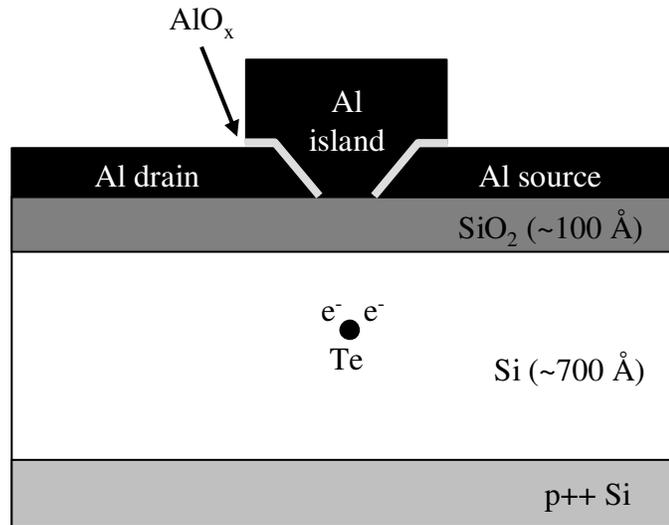


Figure 2.2: Schematic of a Te double donor in Si measured with an SET. The Te atom is embedded in an intrinsic region of Si which is isolated from the metallic SET above it by a thin layer of  $\text{SiO}_2$ . A voltage applied between the heavily doped Si substrate below and the SET above creates an electric field that can ionize the donor and transfer one of its electrons to the Si/ $\text{SiO}_2$  interface. (Modified from Reference [4].)

electron lying 200 meV below the conduction band. It can reasonably be thought of as an artificial He atom with a much larger effective Bohr radius. The first excited orbital lies more than 150 meV above the ground orbital and is correspondingly more easily ionized in an electric field. If the two donor electrons are in a triplet spin state then one must occupy the excited orbital according to the Pauli exclusion principle, while if they are in a singlet spin state they can both occupy the ground orbital. In the architecture envisioned here an electric field would be applied between the p-doped region below the Te impurity and the SET above it, and the SET would sense the motion of the electron between the donor and the oxide interface above. Because the critical field required for this transition depends on the orbital state, which in turn depends on the spin state of the two electrons, a measurement of the critical ionization field will uniquely determine the singlet/triplet spin state.

## 2.4 Experimental description, challenges, and literature review

An even simpler experiment than the one just described involves replacing the Te double donor with a P donor and using an SET to observe the motion of this single donor electron. Although the critical field in this case should not depend on the spin of the electron, this experiment still represents a logical first step on the road toward a measurement of donor spin, and my efforts to design and measure such a system constitute the bulk of this dissertation. Designing the structure in Figure 2.2 is replete with challenges, the greatest of which is the alignment of the SET above the donor. Although control of an impurity's depth within a narrow range is possible with modern ion implantation technology, without a mask of some sort there is no control of the position in the  $x$ - $y$  plane. There are therefore three routes that can be pursued in trying to align an SET above a donor. One is to invent a new technology for individual dopant placement with nm precision. Another is to invent a technology that identifies the position of individual impurities in a randomly doped substrate, to register the positions to alignment marks, and to fabricate an SET aligned to those marks. Still another possibility is to randomly dope a substrate in the  $x$ - $y$  plane, make a large number of SETs on the surface, and measure each SET in turn until one is found lying above a donor due to sheer chance.

At least three groups are actively working on different technologies for nm scale dopant placement in Si. Simmons *et al.* have developed a technique for lithographically placing individual dopants on a Si surface with an STM.[19, 20] They use a H-passivation layer on the surface as a resist which they selectively remove with the STM in UHV. When  $\text{PH}_3$  gas is subsequently admitted to the vacuum chamber it binds only to the H-free regions on the substrate, thereby placing a P dopant with atomic precision. The difficulty with using this technique for the architecture in Figure 2.2 is that it requires subsequent overgrowth of the intrinsic Si region and the oxide, both of which would cause substantial segregation and diffusion of the atomically placed dopant. Another group is working

on placing single dopants with ion implantation.[21] They use a polymethylmethacrylate mask containing an array of 20 nm diameter holes, exposed using e-beam lithography, to allow ions to impact the substrate only in certain locations, and they detect the single ion impacts by collecting the resulting electron-hole pairs in the substrate. Schenkel and coworkers have developed a different ion implantation technology with single ion sensitivity by observing the secondary electrons generated during the impact of highly charged ions.[22, 23, 24] They control the position of the impact to within about 10 nm by directing the beam through a small aperture in a scanned probe tip. The disadvantage of these two techniques for single ion placement is that the spatial accuracy is limited by the hole diameter, by range straggle during implantation, and by diffusion during the required high temperature activation anneal.

There has also been progress in the area of imaging individual dopants in a Si crystal. For example, several groups have successfully located individual P or B atoms in the top few layers using STM.[25, 26, 27, 28] However, because they are only able to image dopants in the top monolayers, using this technique to fabricate the structure in Figure 2.2 has the same disadvantages that the method of STM dopant placement has: the dopants will diffuse and segregate upon subsequent Si overgrowth and oxidation. Other groups have successfully determined the locations of individual dopants using scanning transmission electron microscopy, but this method requires extremely thin samples that may not be compatible with subsequent processing.[29, 30]

As I briefly touched upon in Chapter 1, the simplest but least controlled method of creating the structure in Figure 2.2 is to fabricate a large number of SETs on a lightly and randomly doped wafer, and then to look for those SETs that are properly aligned with a donor by measuring each in turn. This is the path I chose to follow, because I do not have available a technology for single dopant placement or imaging. There are several obstacles that must be faced to reach our goal which include:

1. Measuring a large number of SETs with high bandwidth in a reasonable time pe-

riod,

2. Designing a device geometry wherein the operating point of the SET can be changed without changing the electric field on the donor beneath it,
3. Including in the design some way of varying the Fermi level to insure that donors are occupied at low temperatures,
4. Being confident that the electric field does not ionize the donor so completely that its electron disappears to infinity,
5. Ruling out other sources of charge motion near the SET that will disguise the signal of interest.

The challenge of measuring a large number of SETs in a reasonable time was the first one I tackled, and my solution is discussed at length in Chapter 5. There I describe the millikelvin scanned probe I built which allows measurement of an array of SETs using a high-bandwidth amplifier. The two routes that other groups have pursued for measuring SETs with high bandwidth include the rf-SET[31] and a cryogenic amplifier near the SET.[32, 33] While one group has succeeded in using frequency multiplexing to extend to two the number of SETs that can be measured with a single coax using rf-SET techniques and claims that this technique could be extended to much higher numbers of devices,[34] I have not found in the literature any other SET multiplexing technologies and believe that our scanned probe was the first tool capable of measuring a large number with high bandwidth.

The goal of making a design in which the SET and donor can be controlled independently might seem overly stringent, but for realistic devices with flicker noise and large charge offsets it is the only practical way to consider arranging things. For imagine that the proper voltage had been applied to the p++ substrate to just ionize the donor, but right before it ionized a charged defect moved near the SET island, changing the SET's operating point. In the worst case this unwanted charge would place the SET on top of a Coulomb blockade peak, where it is entirely insensitive to nearby charge motion. We

would then be forced to change the voltage on the p++ substrate to bring the SET back to its bias point, but this would alter the field on the donor away from its ionization value! If instead of changing the voltage on the substrate we changed the voltage on a different nearby gate, say on the surface, this would still change the field on the donor, unless the geometry had been designed so that the gate was completely screened at the donor site. While we can imagine a situation where a counteracting voltage was applied to the substrate as the voltage was changed on the gate, thereby correctly biasing the SET while leaving the donor unaltered, this situation could only be realized if the electrostatics at the donor site were known precisely, and this in turn would require knowledge of the donor position, which we don't have. Consequently it was necessary to design a gate for the SET that would induce a negligible field at all conceivable donor locations of interest. Our approach to this problem is covered in detail in Chapters 3 and 4. If it were possible to say unambiguously that an observed charge signal was coming from donor charge motion then this requirement could be relaxed.

Having confidence that the donors of interest are in fact occupied with an electron at low temperatures is also important. For example, a Si(100) surface interfacing with simple vacuum has a huge density of dangling bonds that yield states whose energies lie inside the bulk band gap.[35] These states could swallow up the electrons from any nearby donors. While the density of states in the gap can be reduced substantially in the case of a carefully H-passivated Si/SiO<sub>2</sub> interface, the best values are still about  $5 \times 10^8 / \text{cm}^2$ , [36] and typical values are often orders of magnitude higher than this. For a review of Si/SiO<sub>2</sub> defect physics see references [37] and [38]. Or the substrate could be p-type as envisioned in Figure 2.2, so that donor electrons would be consumed by a high density of acceptors. Or there could be some charge contamination in the oxide that bends the bands upward near the surface, thereby depleting the donors. Band diagrams of these three situations are depicted in Figure 2.3. In principle at low temperatures these situations can be addressed, provided that there exists some way to create electron-hole pairs and to collect charges

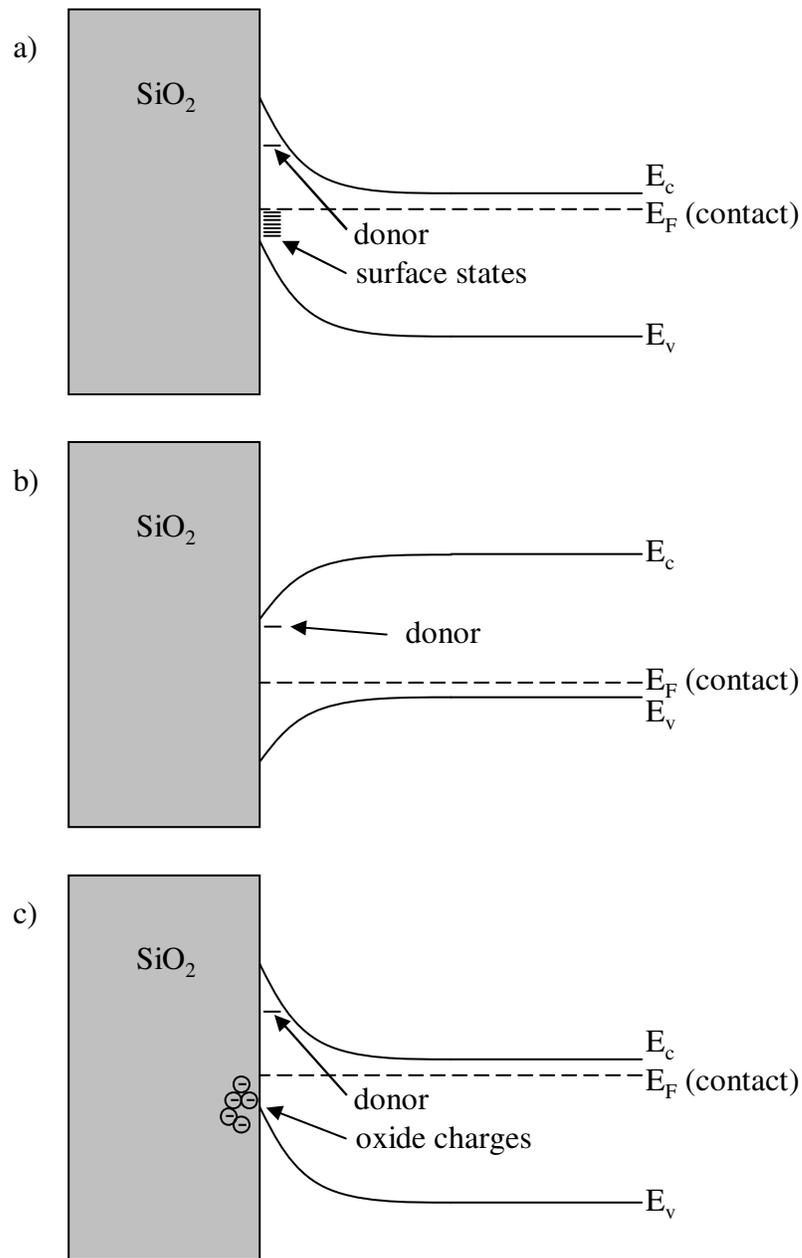


Figure 2.3: Band diagrams illustrating why a donor might not be occupied at low temperatures. a) Band bending due to a high density of interface states in the band gap. These bend the bands upward so that the nearby donor state lies above the Fermi energy, even in the case that the substrate is n-type as shown. b) Diagram showing that, with a p-type substrate, if the donor density at the interface is not high enough, the bands will not bend far enough downward to keep the donors occupied. c) Band bending due to unwanted charge in the oxide, in this case negative, that pushes a nearby donor state above the Fermi energy even for an n-type substrate.

at a different point in the substrate, because it is possible to arrange metastable situations with extremely long lifetimes. Take Figure 2.3b for example: if we illuminate the sample to create electron-hole pairs the electrons will flow to the left, filling the donors there, and the holes will flow out the contact the right. Provided that the donors are much farther than a tunneling length away from the contact, the electrons cannot recombine at low temperatures, and we have succeeded in populating the donors.

The situations in (a) and (c) are slightly more complicated. In these cases it is necessary to apply a sufficiently negative voltage to the contact to make the bands flat at the interface. Then upon illumination holes will flow to the contact and electrons to the surface, populating the donors there. This explains why we wouldn't want to try the experiment by applying electric fields through a contact on the oxide alone: there would be no way to add or subtract carriers from the sample. I describe our substrate contact in more detail in Chapters 4 and 4.3.3.

Once we are confident that the donors are occupied we will need to apply an electric field to ionize them toward the SET, say in the  $z$  direction. When the field becomes strong enough the electron should move from the donor site to the interface. If the electric field were solely in the  $z$  direction then the electron would remain confined in the  $x$ - $y$  plane at this point by the residual attraction from its donor nucleus. But unless great care is taken in the design, the electric field will have some component in the  $x$ - $y$  plane which might push the electron away from its donor. We must design the gating structure with careful attention to this fact so that the electron is not completely lost when it ionizes. I did some finite element modeling of our geometry to get an idea of the fields we should expect, with the results given in Chapter 3. As an additional concern, if the donor density becomes too high then the wave functions of donor electrons at the interface would begin to overlap, an electron from one donor might be captured by another, and we would no longer be able to treat each donor as an isolated system. I address this issue in Chapter 3 as well.

Perhaps the greatest challenge this experiment faces is distinguishing between the signals of interest, coming from donor charge motion, and unwanted signals coming from other mobile charges near the SET island. There are at least four other possible sources of charge motion that must be eliminated or accounted for: unintended charged defects or impurities in the bulk Si, charges at the Si/SiO<sub>2</sub> interface, charges within the bulk oxide, and charges moving on the substrate surface or in the SET AlO<sub>x</sub>. Most of these other signals can be ruled out by comparing samples with and without a donor implant, as the number of relevant signals should be proportional to the donor density. But there are other ways of distinguishing between signal sources as well. For example, different gates near the SET should have different effects on a given charge depending on its location. If we design the geometry so that we have two gates, one which affects donors beneath the surface and one that does not, charge signals which are affected by voltage changes on either gate can be ruled out as coming from donors. Similarly, if we charge up the Si/SiO<sub>2</sub> interface with a large density of electrons or holes to create a 2DEG, that 2DEG should shield the SET from any charge motion beneath it, and any signals we see in this case must be coming from above.

There has been some prior research into the nature of charges associated with defects near metallic SETs on various substrates.[39, 40, 41, 42, 43] Several groups have attempted to locate the defects in space by using multiple gates or multiple SETs, although there is as yet no real consensus concerning the source of these signals.[44, 45, 46] Partly this stems from the fact that there are two different noisy behaviors of interest common to metallic SETs: typical  $1/f$  noise present in most electronic devices, and charge offset jumps or telegraph noise. While  $1/f$  noise may prove to be a problem later on for our experiments into individual donors, the problem of charge offset jumps is more immediate, as these jumps can easily be confused with the signals we would expect from a moving donor electron. In the literature charge jumps have been reported that correlate precisely with the applied gate voltages, that don't correlate at all with the gate voltages, or that cor-

relate only somewhat. And the explanations for these signals have ranged from charges in the tunnel barriers to charges in the substrates. There is evidence that the presence of these anomalies in SETs can depend both on the material used to make the device as well as on the substrate.[47, 48, 49] Furthermore, flicker or random telegraph noise has been exhaustively studied in MOSFET's, and even in these much more comprehensively studied and understood devices the sources of such noise are a bit mysterious.[50]

To date there has been little progress toward measuring the charge signal due to the controlled ionization of individual dopants in Si. Hofheinz *et al.* have reported observations of charge motion near a silicon nanowire SET that they attribute to individual As impurities nearby, but the evidence they give in favor of impurities versus some other trapping mechanism is not strong, and their measurement geometry is not designed specifically for this purpose.[48] Buehler and coworkers have given strong evidence for the transfer of individual electrons between metallic *clusters* of P donors, but not between the individual donors themselves.[51] Their evidence is convincing, but the road from clusters to individual impurities is a long one. There have been more studies of the ionization of impurities in bulk samples, and these point to around 10 kV/cm as the required electric field.[52, 53, 54, 55, 56, 57] Note that this field will depend strongly on the distance from the interface if, as in our experiments, the donor electron will be tunneling into an interface state instead of into the continuum.

## Chapter 3

### Measuring the field ionization of Si:P

As discussed in Chapter 2, the ultimate goal of this research was to measure the controlled motion of a single electron in Si between a donor site and a nearby Si/SiO<sub>2</sub> interface under the influence of an applied electric field. The measurement would be made with a very sensitive electrometer, the single electron transistor. A single electron transistor (SET) is a three (or more) terminal device consisting of a nanometer dimension island weakly tunnel-coupled to source and drain leads and capacitively coupled to one or more gates. When biased appropriately the current flowing from drain to source depends strongly on the electric potential in the vicinity of the island. So the change in island potential due to the motion of a nearby donor electron toward an SET will cause a change in drain-source current. In this chapter I lay out in greater detail the theory behind electron transfer from donor site to interface in an electric field. I also present some simulations relevant to observation of that motion with an SET.

#### 3.1 P donor in an electric field near an interface

The basic idea is outlined in Figure 3.1 with a corresponding energy-band diagram in Figure 3.2. From an experimental perspective we need to be confident that we can load the system with one, and only one, electron, that both the interface and donor states are well localized, and that the transfer of the electron between these two locations happens quickly enough for us to measure it over a reasonable timescale. We would also like an estimate of the electric field required to effect the transfer and of the signal we can expect in our detector.

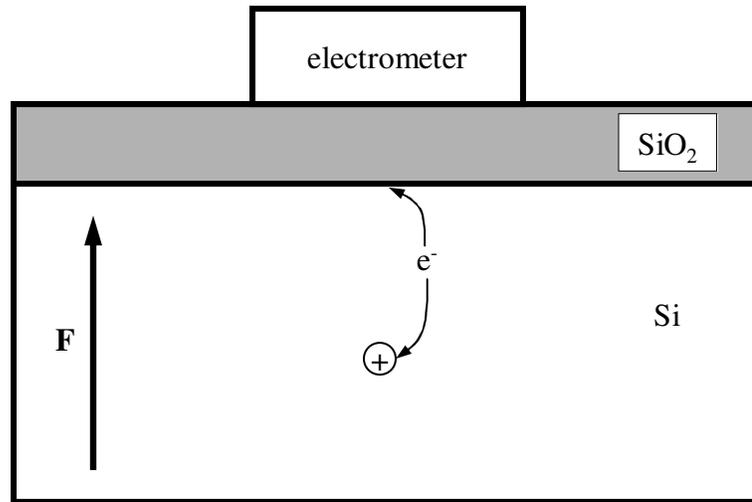


Figure 3.1: Layout of a donor in Si near an electrometer. The metal electrometer is isolated from the Si crystal by a thin layer of oxide. The electron moves between the donor site and the Si/SiO<sub>2</sub> interface under an applied electric field  $F$  as shown by arrows. These different charge configurations are distinguished by the electrometer.

### 3.1.1 Hydrogenic model of donors in Si

It is well known that various impurities in semiconductors can often be treated approximately as artificial hydrogen atoms, where the mass of the electron and the dielectric constant of the vacuum are replaced by the effective mass  $m$  and the dielectric constant  $\epsilon$  of the semiconductor host.[58] To lowest order this is a reasonable model for P impurities in Si, because the P atom has one more electron in its outer shell compared with Si, and its nucleus has one extra proton, although the description is slightly complicated because of the anisotropic effective mass of the Si conduction band, whose constant energy surfaces are shown in Figure 3.3. These give an effective mass  $m_{\parallel} = 0.92 m_e$  along the  $\langle 100 \rangle$  directions and  $m_{\perp} = 0.19 m_e$  in the other two orthogonal directions. If we take these two values for the effective mass and the dielectric constant  $\epsilon = 11.8 \epsilon_0$  for Si then we

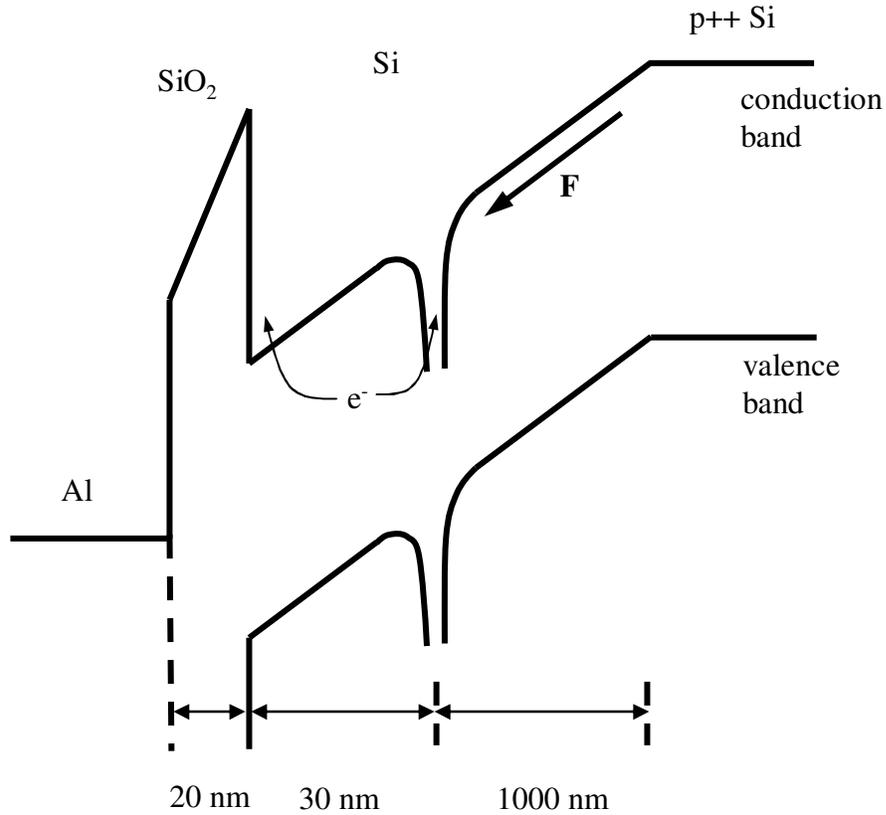


Figure 3.2: (Not to scale) Simplified energy-band diagram of the layout shown in Figure 3.1. The field  $F$  is applied between a heavily doped layer in the substrate and the Al SET on the surface. When sufficient field is applied the electron tunnels from the donor site to the interface as shown by arrows. The heavily doped region must be doped with acceptors to avoid flooding the region near the donor with carriers.

calculate a hydrogenic binding energy

$$E_0 = \frac{\alpha^2 mc^2}{2\epsilon_{rel}^2} \quad (3.1)$$

$$= 90 \text{ meV} \quad (m = m_{\parallel}), \quad (3.2)$$

$$= 19 \text{ meV} \quad (m = m_{\perp}). \quad (3.3)$$

The electron is thus much more weakly bound to the donor site in a semiconductor than it is in a true hydrogen atom, where the binding energy is 13.6 eV, but at dilution refrigeration

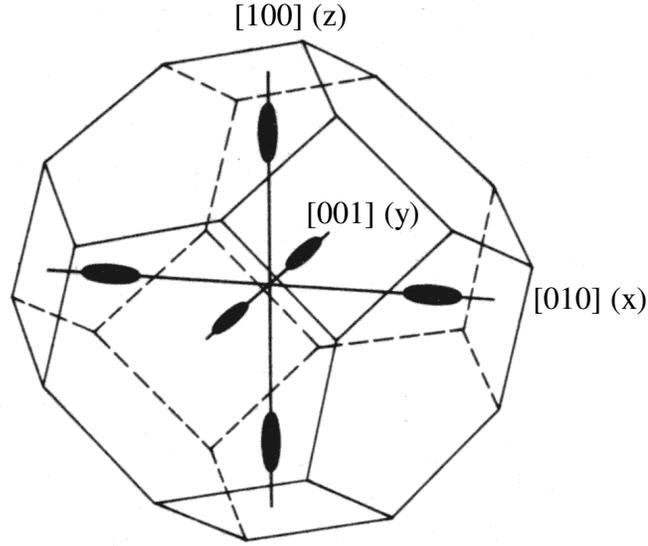


Figure 3.3: Constant energy surfaces for electrons in the Si conduction band. There are six equivalent valleys along the  $\langle 100 \rangle$  directions. The stretched dimension yields an effective mass  $m_{\parallel} = 0.92 m_e$ , while the other two directions give  $m_{\perp} = 0.19 m_e$ . (Modified from Reference [59].)

erator temperatures ( $T \lesssim 100$  mK) the probability is extremely small for a donor electron to be thermally excited. More worrisome from an experimental perspective, as already discussed in Section 2.4, is the possible presence of a significant number of traps, either in the bulk crystal or at the Si/SiO<sub>2</sub> interface, that could capture the donor electron, or of some other built-in field that could ionize it. This issue will be most easily addressed experimentally, by adding or subtracting enough electrons from the sample that the Fermi level near the interface lines up with the donor energy.

The sixfold degenerate nature of the Si conduction band, with minima along the six equivalent  $\langle 100 \rangle$  directions, yields a sixfold degenerate ground state in effective mass theory, but in fact the valley-orbit and central cell corrections,[60] which more carefully treat the electron close to the impurity nucleus that breaks translational symmetry, partially lift this degeneracy and ensure a nondegenerate ground state. Experimentally one

finds that the ground state lies 45.6 meV below the conduction band. The first excited state lies 11.7 meV above the ground state, followed by an infinite number of other bound states analogous to the excited states of the hydrogen atom,[61] shown schematically in Figure 3.4. The lack of spherical symmetry for the ground state means that the effective Bohr radius is no longer a good measure of the size of the electron cloud. Instead we can calculate two effective Bohr radii to obtain an order of magnitude estimate of the extent of the wave function, again using the effective mass and dielectric constant for Si:

$$a_0 = \frac{4\pi\epsilon\hbar^2}{me^2} \quad (3.4)$$

$$= 7 \text{ \AA} \quad (m = m_{\parallel}), \quad (3.5)$$

$$= 33 \text{ \AA} \quad (m = m_{\perp}). \quad (3.6)$$

The electron state at the donor site is thus nondegenerate and localized to within a few nm.

### 3.1.2 Interface electrons in an electric field: triangle well potential

While it is now clear that the wave function of a donor electron is localized on the nm scale, it is not so obvious that the electron will stay localized after it is transferred to the interface. To describe an electron at the interface we turn to solutions of the Schrödinger equation for the triangle well potential, which in this case is formed by the electric field near the Si/SiO<sub>2</sub> interface. My experiments were done using an interface of thermal SiO<sub>2</sub> on the <100> surface, so that particular crystal orientation will be assumed throughout the following discussion, although similar qualitative results should still apply for other Si surfaces. The Si conduction band lies about 3.5 eV below the conduction band of SiO<sub>2</sub>,[62] so for states with energies much less than 3.5 eV above the Si conduction band it is a good approximation to treat the Si/SiO<sub>2</sub> interface as an infinite barrier. If we ignore the perturbing effect of the donor nucleus for the moment this problem is one-dimensional

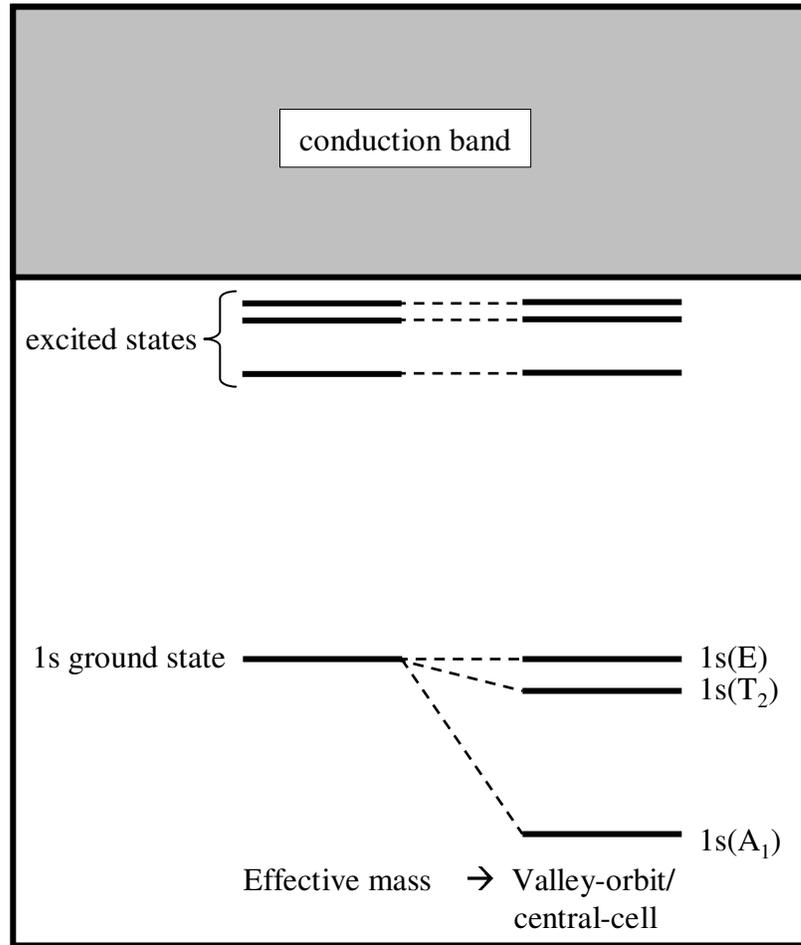


Figure 3.4: Energy diagram showing bound states of the P donor below the continuous conduction band in Si. The 1s ground state, which is sixfold degenerate in the effective mass theory, is in fact split by the central-cell potential into a singlet 1s(A<sub>1</sub>), a doublet 1s(E), and a triplet 1s(T<sub>2</sub>). The 1s(A<sub>1</sub>) ground state lies 45.6 meV below the conduction band.

and can be solved exactly.[63] For an electron in an electric field  $F$  in the  $z$  direction, effective mass  $m$ , and Si/SiO<sub>2</sub> interface at  $z = 0$  the Hamiltonian is

$$H = \frac{-\hbar^2}{2m} \partial_z^2 + eFz. \quad (3.7)$$

The Schrödinger equation becomes

$$H\psi = E\psi \quad (3.8)$$

$$\frac{-\hbar^2}{2m} \partial_z^2 \psi + (eFz - E)\psi = 0. \quad (3.9)$$

We change variables, defining

$$\xi \equiv \left( \frac{2meF}{\hbar^2} \right)^{\frac{1}{3}} \left( z - \frac{E}{eF} \right). \quad (3.10)$$

In terms of this new variable we find

$$\partial_\xi^2 \psi - \xi \psi = 0. \quad (3.11)$$

This is the differential equation defining the Airy functions  $\text{Ai}(\xi)$  and  $\text{Bi}(\xi)$ :[64] however,  $\text{Bi}(\xi)$  is not a physically allowed solution because it blows up for  $z \rightarrow \infty$ .

The boundary condition  $\psi = 0$  at  $z = 0$  determines the allowed energies in the well. This is because  $z = 0 \Rightarrow \xi = - \left( \frac{2m}{\hbar^2 e^2 F^2} \right)^{\frac{1}{3}} E$ , so that if  $\xi_i$  are the zeros of  $\text{Ai}(\xi)$  then the allowed energies are

$$E_i = - \left( \frac{\hbar^2 e^2 F^2}{2m} \right)^{\frac{1}{3}} \xi_i. \quad (3.12)$$

The  $\xi_i$  are -2.33811, -4.08795, -5.52056, ... and can be approximated to within  $\sim 1\%$  by

$$\xi_i = - \left[ \frac{3\pi}{2} \left( i + \frac{3}{4} \right) \right]^{\frac{2}{3}}, \quad i = 0, 1, 2, \dots \quad (3.13)$$

We see that the ground state energy of the well and the splitting between levels near the bottom of the well are of order

$$\Delta E = \left( \frac{\hbar^2 e^2 F^2}{2m} \right)^{\frac{1}{3}}. \quad (3.14)$$

We can determine the approximate field necessary for ionization by considering that the electron must regain from the electric field its donor binding energy during its transfer to the interface. For a donor 30 nm from the interface this gives  $F = 45.6 \text{ meV} / 30 \text{ nm} = 15.2 \text{ kV/cm}$ . Later I will show that a better estimate gives  $F = 17.7 \text{ kV/cm}$ . With this field and the effective mass  $m = m_{\parallel}$  the ground state energy from Equation 3.12 lies 11.8 meV above the conduction band minimum at  $z = 0$ , separated from the first excited state by 8.9 meV. The ground state wave function and the energy levels are plotted in Figure 3.5, where we see that the electron is localized to within a few nm. These energies correspond to electrons residing in the two valleys parallel to the field. The states of electrons in the four valleys along the perpendicular directions are much higher in energy due to the strong  $1/m$  dependence in Equation 3.12.

In the absence of disorder an electron in one of these interface states is entirely delocalized in the  $x$ - $y$  plane, and the states are infinitely degenerate. However the nearby donor, although far from the interface on the scale of the effective Bohr radii, is still close enough that its long range Coulomb potential can confine the electron at reasonably low temperatures. For a donor sufficiently far from the interface, at distance  $z_0$ , we can to good approximation consider the electron fixed at  $z = z_0$ . Then the potential depends only on  $x$  and  $y$ , and it becomes

$$U(x, y) = -\frac{e^2}{4\pi\epsilon_{\text{eff}}} (x^2 + y^2 + z_0^2)^{-\frac{1}{2}} \quad (3.15)$$

We take into account the image charge of the donor nucleus arising from the Si/SiO<sub>2</sub>

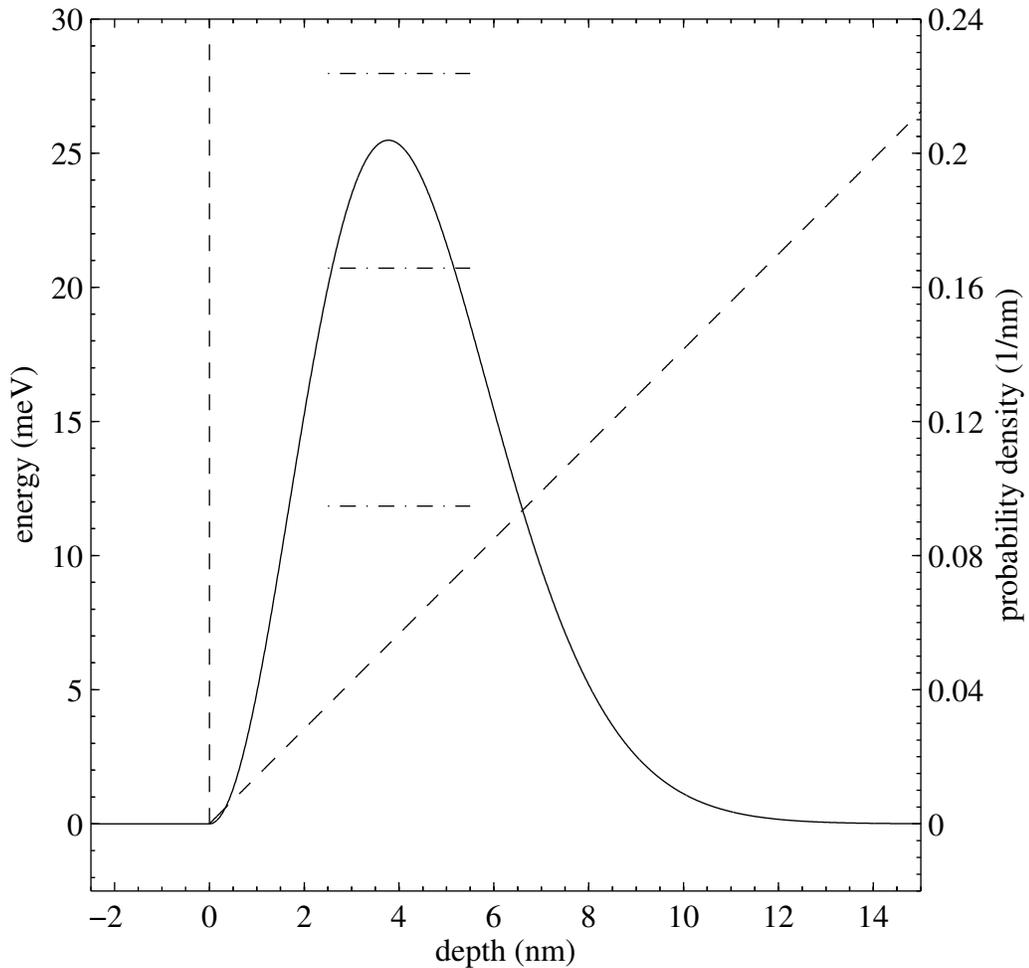


Figure 3.5: Analytical solution of the triangle well potential. The long dashes show a potential well formed by a hard wall at  $z = 0$  and an electric field of 17.7 kV/cm. The solid curve is a plot of the absolute square of the ground state wave function. The dashed-dotted lines show the energies of the lowest lying states.

interface with an effective dielectric constant. I note that the electron's own image charge does not contribute to the potential in the  $x$ - $y$  plane because it always acts back on the electron in the  $z$  direction. Because the dielectric constant of Si is higher than that of SiO<sub>2</sub>, the image charge of the nucleus is in fact positive and therefore acts to further attract the electron. To account for this we use an effective dielectric constant[65]

$$\epsilon_{\text{eff}} = \frac{1}{2} (\epsilon_{\text{SiO}_2} + \epsilon_{\text{Si}}) \quad (3.16)$$

$$= 7.9 \epsilon_0. \quad (3.17)$$

The Schrödinger equation for the potential given by Equation 3.15 is not solvable analytically. Nevertheless, we can get an order of magnitude estimate for the energies and wave functions by approximating the potential with a harmonic potential. If we expand the potential to 2nd order in  $x$  and  $y$  we find

$$U(x, y) = \frac{e^2}{4\pi\epsilon_{\text{eff}}z_0^3} \left( \frac{x^2}{2} + \frac{y^2}{2} \right) - \frac{e^2}{4\pi\epsilon_{\text{eff}}z_0} \quad (3.18)$$

$$= \frac{m\omega^2}{2} (x^2 + y^2) - U(0, 0), \quad (3.19)$$

where

$$\omega = \frac{e}{\sqrt{4\pi m \epsilon_{\text{eff}} z_0^3}}. \quad (3.20)$$

The relevant mass for electrons in the valleys parallel to the field is  $m = m_{\perp}$ . The second term on the right hand side of Equation 3.19 is a constant offset that does not contribute to the binding in  $x$  and  $y$ . The energies in the harmonic approximation are given by the sum of two harmonic oscillators:

$$E_{\perp} = \hbar\omega(n_x + n_y + 1) + U(0, 0), \quad (3.21)$$

where  $n_x, n_y \geq 0$ . Figure 3.6 shows a plot of  $\hbar\omega$  as a function of donor depth. This represents an estimate of the binding energy of the electron in the  $x$ - $y$  plane at the interface, and for a donor depth  $z_0 = 30$  nm we find  $\hbar\omega = 1.6$  meV. Calderon, Koiller, and Das Sarma have recently done a more sophisticated variational calculation of this quantity, and they find  $\hbar\omega = 1.1$  meV for  $z_0 = 30$  nm,[5] just 30% less than the harmonic value.

A single harmonic oscillator has the ground state wave function

$$\psi_0(x) = \left(\frac{m\omega}{\pi\hbar}\right)^{\frac{1}{4}} \exp\left(-\frac{m\omega x^2}{2\hbar}\right). \quad (3.22)$$

So the wave function for two harmonic oscillators of equivalent frequency, one in  $x$  and the other in  $y$  is

$$\Psi_0(x, y) = \left(\frac{m\omega}{\pi\hbar}\right)^{\frac{1}{2}} \exp\left(-\frac{m\omega(x^2 + y^2)}{2\hbar}\right) \quad (3.23)$$

$$= \left(\frac{m\omega}{\pi\hbar}\right)^{\frac{1}{2}} \exp\left(-\frac{m\omega r^2}{2\hbar}\right), \quad (3.24)$$

where  $r = \sqrt{x^2 + y^2}$ . The probability density for the electron to be found at a given radius  $r$  is then given by

$$P(r) = \int r |\Psi_0(x, y)|^2 d\theta \quad (3.25)$$

$$= \frac{2m\omega r}{\hbar} \exp\left(-\frac{m\omega r^2}{\hbar}\right). \quad (3.26)$$

Figure 3.7 shows this probability, superimposed on the potential assuming a 30 nm donor depth.

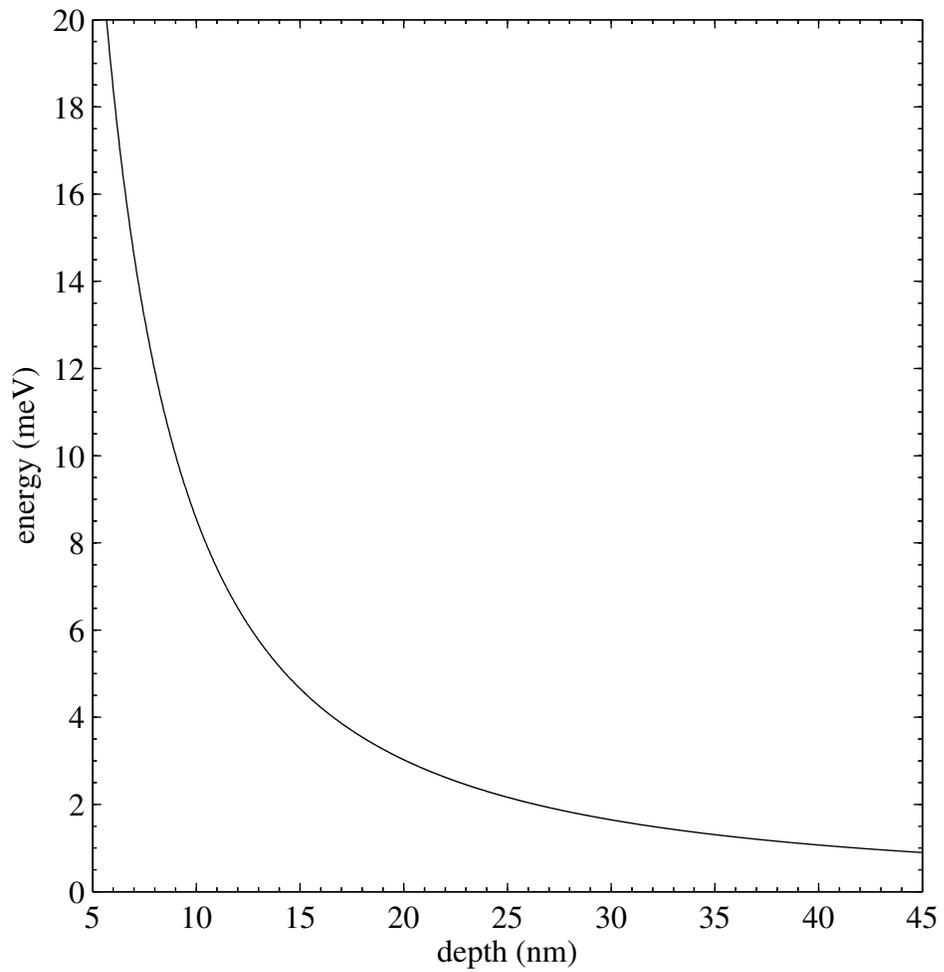


Figure 3.6: Separation between ground and first excited states of an electron bound in the  $x$ - $y$  plane by a nearby donor potential. I have used the harmonic approximation for the potential, valid at large donor depths.

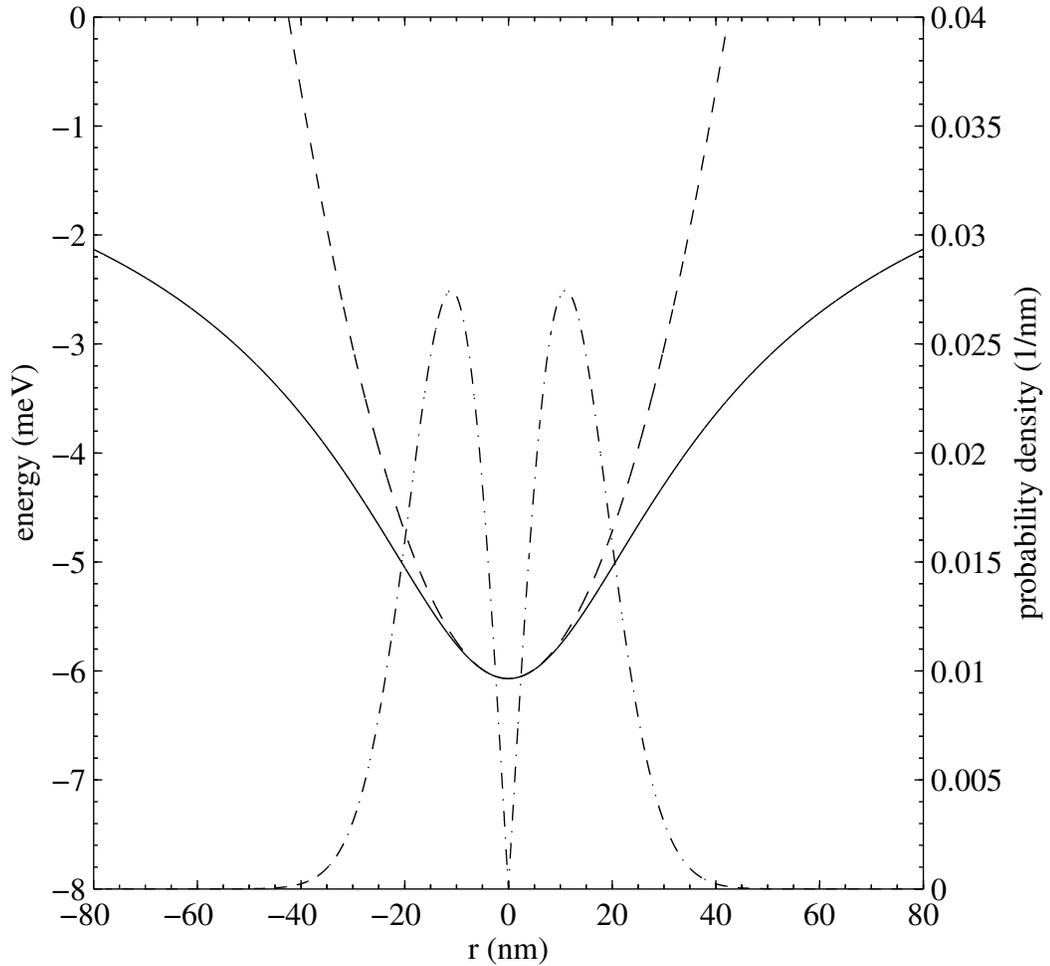


Figure 3.7: Potential and probability density in the  $x$ - $y$  plane for an electron at the Si/SiO<sub>2</sub> interface near a donor at 30 nm depth. The solid line and dashed line shows the potential and its harmonic approximation, respectively. The dashed/dotted line shows the probability density for the electron to be at a given radius.

The approximate extent of the wave function is given by

$$\sigma = \sqrt{\frac{\hbar}{m\omega}} \quad (3.27)$$

$$= \left( \frac{4\pi\hbar^2 \epsilon_{\text{eff}} z_0^3}{me^2} \right)^{\frac{1}{4}} \quad (3.28)$$

which for a donor at 30 nm is 15.6 nm. This agrees within a few percent with the variational calculation by Calderon, Koiller, and Das Sarma.[5] I have plotted the dependence of  $\sigma$  on depth in Figure 3.8; I note that this size is important because it ensures that individual donor wave functions do not significantly overlap for electrons at the interface, which would form a 2DEG as I discuss in Section 3.1.4.

I note that the ground state of the electron at the interface is in principle twofold degenerate due to the two equivalent valleys of the Si conduction band that remain symmetric in the presence of the electric field. However, the effective mass theory I have used here is not strictly applicable in the presence of the abrupt Si/SiO<sub>2</sub> interface, which violates the assumption that the potential changes only slowly on the scale of a lattice constant. Sham and Nakayama[66] have extended the theory to more correctly include the effect of a sharp boundary, and they estimate a valley splitting

$$\delta E = eF \times 0.43 \text{ \AA}, \quad (3.29)$$

which for  $F = 17.7 \text{ keV/cm}$  gives  $76 \text{ } \mu\text{eV}$ . The actual magnitude of this effect is still a topic of ongoing research.[67, 68]

### 3.1.3 Coupling between donor site and interface states

With no applied electric field the interface states do not exist. As the electric field is slowly increased from zero, the interface states appear and gradually spread apart in energy as discussed in Section 3.1.2. For a given donor depth there exists a critical field

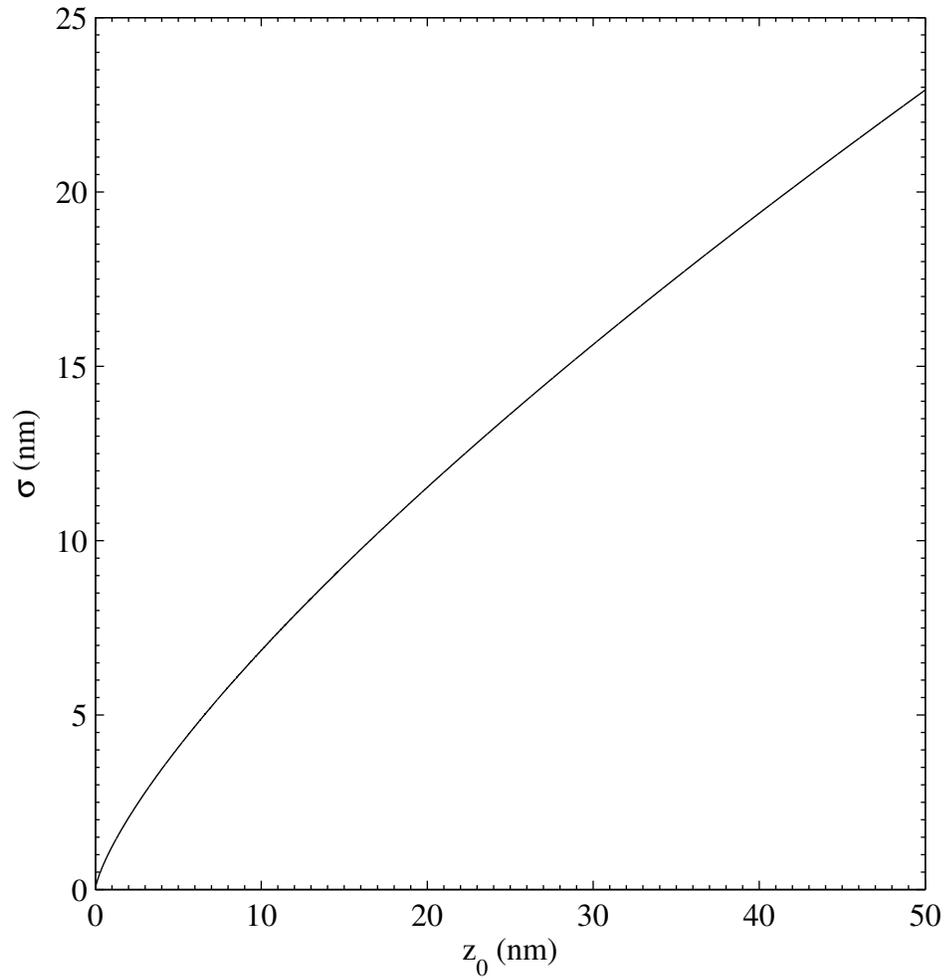


Figure 3.8: Wave function extent in the  $x$ - $y$  plane for an electron at the Si/SiO<sub>2</sub> interface versus donor depth  $z_0$ .

beyond which the energy of the interface state falls below the energy of the donor site. This is illustrated schematically in Figure 3.9.

Provided that the field is increased slowly enough, when the two states are brought into resonance the electron will move out of the donor state and into the interface state. We can now make a better estimate of the critical field using a semiclassical argument. Assume that the donor is deep enough beneath the interface that its contribution to the field there is small compared to the critical field. We will check this assumption for validity after we solve the problem. We know the ground state energy at the interface in the  $z$  direction from Equation 3.12. The energy in the  $x$ - $y$  plane is given by  $\hbar\omega$  from Equation 3.20, while the energy is shifted downward by the nearby donor potential, given by  $U(0,0)$  in Equation 3.19. On the other hand, to lowest order the energy of the donor is still  $E_d = -45.6$  meV, to which we add the  $F \cdot z_0$  contribution from the field. Therefore the critical field is given approximately by

$$-\left(\frac{\hbar^2 e^2 F_{\text{crit}}^2}{2m_{\parallel}}\right)^{\frac{1}{3}} \xi_0 + \frac{\hbar e}{\sqrt{4\pi m_{\perp} \epsilon_{\text{eff}} z_0^3}} - \frac{e^2}{4\pi \epsilon_{\text{eff}} z_0} = E_d + F_{\text{crit}} \cdot z_0. \quad (3.30)$$

For  $z_0 = 30$  nm the solution is  $F_{\text{crit}} = 17.7$  kV/cm. In contrast, the field at the interface due to the donor 30 nm away is

$$F = \frac{e}{4\pi \epsilon_{\text{eff}} z_0} \quad (3.31)$$

$$= 2.0 \text{ kV/cm}, \quad (3.32)$$

so our initial assumption that  $F \ll F_{\text{crit}}$  is good.

Knowledge of the critical field tells us nothing about the rate at which the electron tunnels from the donor to the interface state. For an electron many Bohr radii away from the interface the critical field could be infinitesimally small, and the tunneling rate would become very small. To estimate the tunneling rate requires calculating the transition ma-

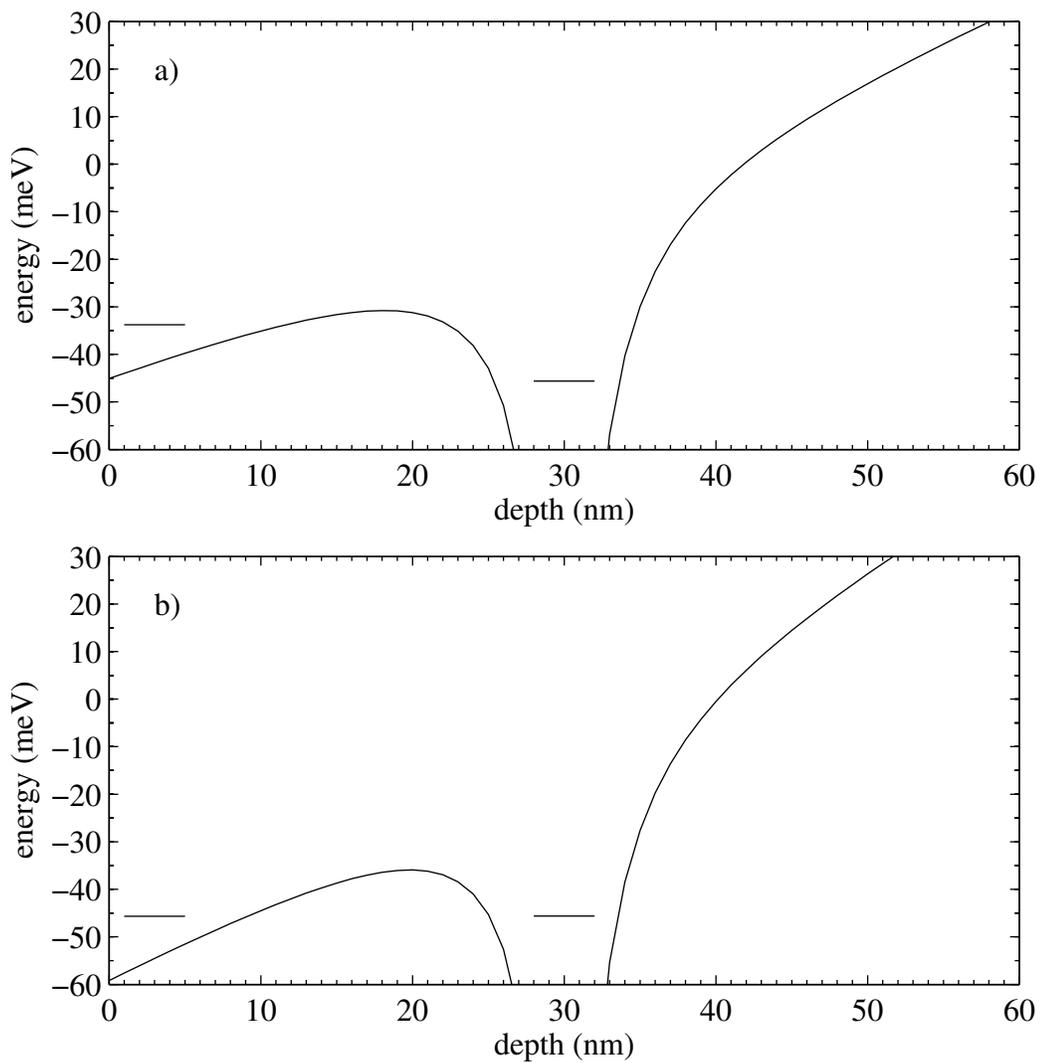


Figure 3.9: Schematic of electron transfer between a donor site and a nearby interface under an applied electric field. In a) the field is not above its critical value, and the donor energy still lies below the ground state at the interface. In b) the field has reached its critical value, so that the donor and interface states come into resonance.

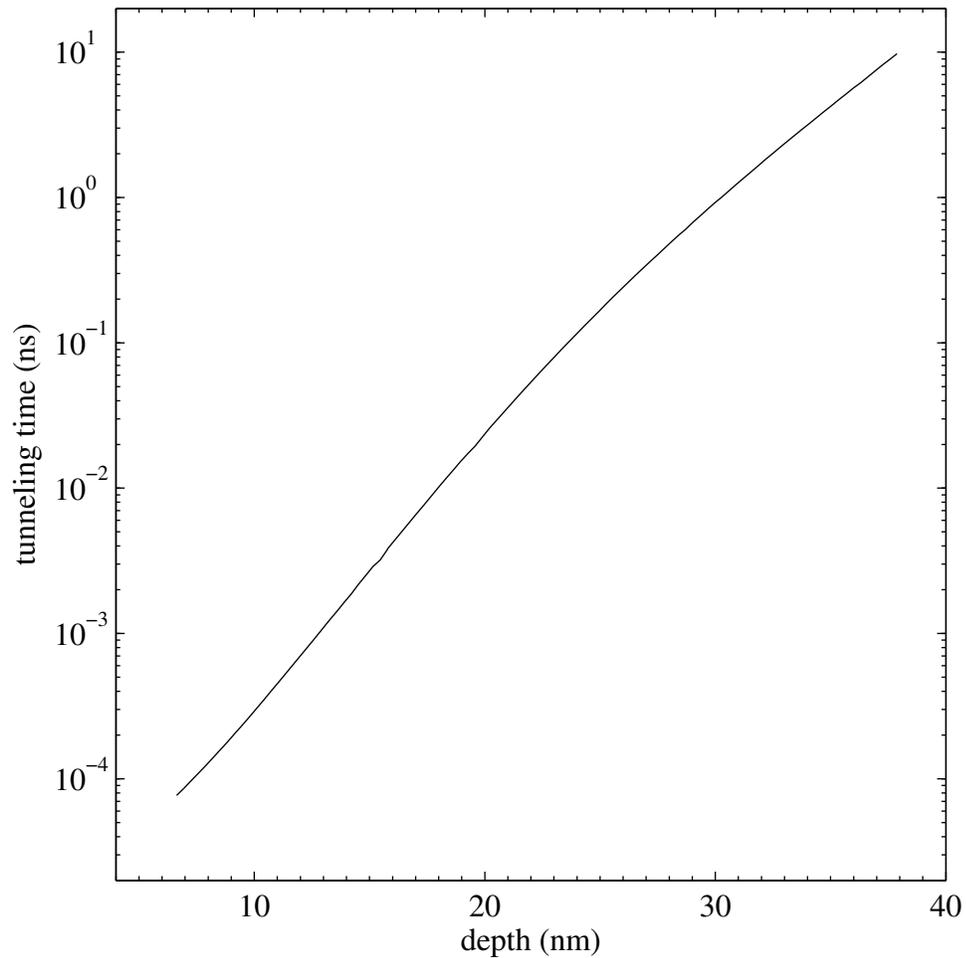


Figure 3.10: Tunneling time on resonance between a donor state and an interface state as a function of donor depth. Calculation by Calderón *et al.*[5]

trix element between the donor state and the interface state, a difficult calculation that I shall not attempt here. Calderón *et al.* have done this calculation numerically, and their results are plotted in Figure 3.10.[5] For a 30 nm donor depth they find a tunneling time of 1 ns. The strong exponential dependence of this tunneling time on depth means that the donor must not be placed much deeper than  $\sim 50$  nm if we want tunneling to occur at the ms timescale or faster.

### 3.1.4 Summary

What conclusions can be drawn from this theoretical background? Theoretically we have no way of ensuring that a donor will be occupied at low temperatures (e.g.  $T < 100 \text{ mK} = 8.6 \mu\text{eV}$ ) because it could be captured by nearby traps. Instead we will need a way of fixing the local Fermi level to place a single electron at the donor site. However, P donors have a nondegenerate ground state, and the closest excited state lies 11.7 meV above that: we can be confident that the electron, once placed in the ground state, will not be thermally excited. Furthermore, for a doping density around  $2 \times 10^{16}/\text{cm}^3$ , or a mean separation of 37 nm, typical for our experiments, the electron wave functions of neighboring donors, with a 2-4 nm extent, do not significantly overlap.

Upon application of a 17.7 kV/cm static electric field which brings the donor and interface energies into resonance, the electron should move from the donor site to the interface on a ns timescale. Application of a small ac field of frequency  $f \ll 1 \text{ GHz}$  should cause the electron to transfer back and forth between the 30 nm deep donor site and the interface, in phase with the applied field. Increasing the static field beyond 17.7 kV/cm should confine the electron to the interface.

The electron, once it has transferred from the donor site to the interface, remains confined in the  $x$ - $y$  plane by about 1.6 meV. While this would at first glance seem strong enough to keep it from escaping at  $T < 100 \text{ mK}$ , it does not represent a realistic situation because it neglects the presence of other nearby donor sites. A typical areal doping density used in these experiments was  $10^{11}/\text{cm}^2$ , corresponding to a mean separation between donors of 30 nm, while the extent of the interface orbital in the plane is  $\sim 15 \text{ nm}$ . There is therefore significant overlap between the wavefunctions of adjacent interface electrons, and it is rather probable that a given electron would escape to a different donor site during the timescale of the measurements. If the overlap is strong enough a ground plane might even form at the interface. This conducting plane would screen the SET from charge

motion in the substrate, completely obscuring the desired signal. Just how detrimental these effects might be is an open theoretical question. The overlap could be made smaller by decreasing the doping density, but this would lead to two problems. First, at a doping density of  $10^{11}/\text{cm}^2$  there are on average 2.5 donors beneath a  $50 \text{ nm} \times 50 \text{ nm}$  SET island. Substantial reduction in the density would lead to a corresponding reduction in the number of donors per SET, which would mean that many more SETs would need to be measured before one was found properly aligned with a donor. Second, these doping densities are approaching the range of densities we might expect for defects at the Si/SiO<sub>2</sub> interface. Substantial reduction in the doping density, therefore, might mean that we would see more effects from defects than we would from the intentional doping.

The ground state at the interface is still twofold valley degenerate in the effective mass approximation I have used, while better estimates give a splitting around  $100 \mu\text{eV}$ . This splitting is barely large enough to ensure that the electron occupies a single valley interface state for  $T < 100 \text{ mK}$ . While this degeneracy would presumably change our calculation of the tunneling time by only a small factor, and so would have negligible impact on the experiments described here, from the perspective of quantum control and coherence it may be a more serious issue.

## 3.2 Electric field simulations

As I outlined earlier in Section 2.4, single electron transistor measurements of isolated donors require two gates: one to influence the donor and one to bias the SET for maximum sensitivity. The measurements are greatly simplified if voltages applied to the the biasing gate (hereafter just the “gate”) have little influence on the donors compared with their influence on the SET, and vice versa for the other gate (hereafter called the “substrate”.) Also the measurements are easier to understand if the substrate provides a uniform electric field to influence donors. One way to achieve these goals is to have

a parallel plate geometry, with metallization on the wafer surface comprising one plate and a heavily doped Si region several hundred nm beneath the surface forming the other plate. While there are other geometries that could also satisfy our constraints, this was the one we eventually decided to try, largely because the electrostatics of a parallel plate capacitor are so simple to analyze. The metallization on the top surface was formed by the leads and island of the SET, while the doped region several hundred nm below the surface formed the gate for influencing donors above it, as diagrammed in Figure 3.11. Provided that any gaps in the metallization layer itself or between the metallization layer and the doped Si region were kept as small as possible, we were confident that this geometry would shield donors beneath the surface from external fields. Therefore I designed the SET to have very wide source and drain leads separated only by a narrow (50 nm) gap as shown in the figure. To quantify and determine the effectiveness of the level of shielding I did finite element modeling of the geometry. I also studied the uniformity of the electric field applied to the donors by the substrate, and I studied the sensitivity of the SET to charge motion in its vicinity. The latter number is important to insure that the signal from a moving donor electron would in fact be large enough to observe. The modeling was done using the FEMLAB package from Comsol.[69]

### 3.2.1 Shielding donors and field uniformity

To quantify the degree to which donors should be screened from gate-induced electric fields we need a physically meaningful figure of merit. We can assume that during our measurements the voltage on the gate will not change by more than  $e/C_g$ , where  $C_g$  is the capacitance between the gate and the island of the SET, because voltages that differ by  $e/C_g$  are equivalent operating points for the SET. A good figure of merit, then, is how much we need to change the potential on the substrate to restore both the field on a donor and the operating point of the SET to their former values given a  $1 e$  shift of the gate voltage. The smaller this change in substrate potential (normalized by the substrate

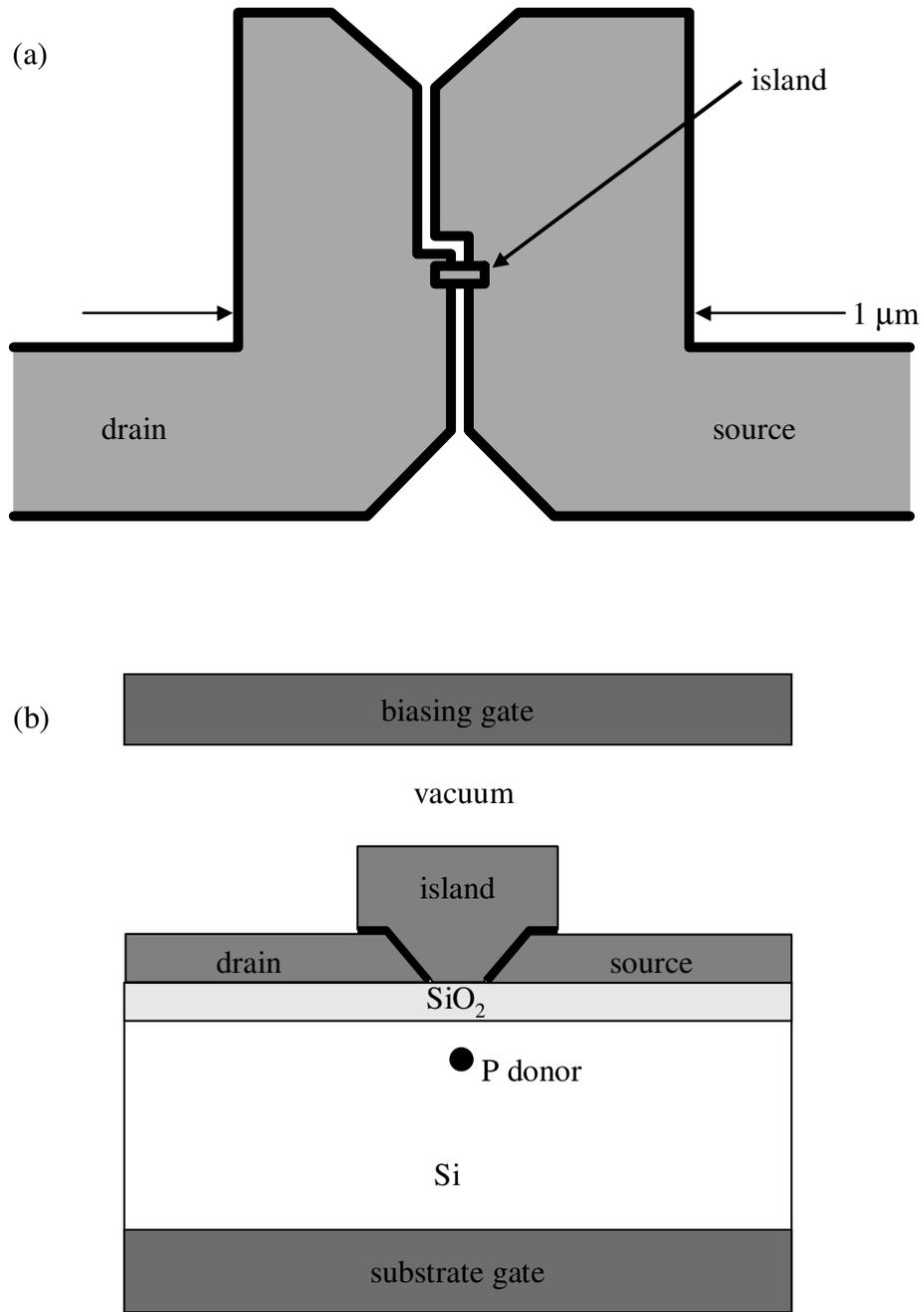


Figure 3.11: SET forming a parallel plate geometry with a conducting region in the substrate. This should screen donors sandwiched between the plates from electric fields induced by the biasing gate. (a) View of the Al pattern from the top showing wide leads separated by a 50 nm gap. The island is 50 nm wide and 150 nm long, but only 50 nm of this length are in contact with the substrate. (b) View from the side showing the gate, SET, and substrate. From this view it becomes clear how the leads and island of the SET will shield the donor from the gate above.

capacitance) compared with  $1 e$ , the better the screening.

Let  $V_g$ ,  $V_s$ ,  $C_g$ , and  $C_s$  be the gate voltage, substrate voltage, gate-island capacitance, and substrate-island capacitance respectively. Assume that changing  $V_g$  and  $V_s$  by equal amounts leads to changes in field at the donor site  $\Delta E_g$  and  $\Delta E_s$  respectively and define

$$\alpha \equiv \Delta E_g / \Delta E_s. \quad (3.33)$$

We would like to calculate our figure of merit in terms of  $C_g$ ,  $C_s$ , and  $\alpha$ . Now assume that a charge moves near the SET island, changing its operating point by  $Q^0$ . To restore the operating point to its former value requires a change on the gate of

$$V_g^0 = -Q^0 / C_g. \quad (3.34)$$

This change in gate potential changes the field at the donor site, so that to restore the field to its former value requires a change in substrate potential

$$V_s^0 = -\alpha V_g^0. \quad (3.35)$$

Of course, changing the substrate potential by this amount again shifts the operating point of the SET by an amount

$$Q^1 = C_s V_s^0 \quad (3.36)$$

$$= \alpha \frac{C_s}{C_g} Q^0, \quad (3.37)$$

which requires further compensation on the gate, and the process continues. Taking this process to its logical conclusion yields a geometric series for the total change in voltage

on the substrate:

$$V_s^{\text{total}} = (-\alpha V_g^0 - \alpha V_g^1 - \alpha V_g^2 + \dots) \quad (3.38)$$

$$= \frac{\alpha}{C_g} (Q^0 + Q^1 + Q^2 + \dots) \quad (3.39)$$

$$= \frac{\alpha}{C_g} \left( Q^0 + \alpha \frac{C_s}{C_g} Q^0 + \left( \alpha \frac{C_s}{C_g} \right)^2 Q^0 + \dots \right) \quad (3.40)$$

$$= \frac{\alpha Q^0}{C_g} \frac{1}{1 - \alpha \frac{C_s}{C_g}}. \quad (3.41)$$

To find a figure of merit I normalize by the substrate capacitance and find:

$$q = \frac{\alpha Q^0}{C_g} \frac{C_s}{1 - \alpha \frac{C_s}{C_g}} \quad (3.42)$$

$$= \frac{Q^0}{\frac{C_g}{\alpha C_s} - 1}. \quad (3.43)$$

We see that to achieve good shielding, that is  $q \ll Q^0$ , we need to maximize  $C_g$  while minimizing  $\alpha C_s$ .

To evaluate  $\alpha$  for our geometry I began with the approximation that the SET and leads are a patterned two-dimensional sheet of conductor. Including the thickness of the metal in the model would only lead to a greater degree of shielding, so that this approximation gives at least an upper bound to how much the gate field influences the donors. The substrate and gate were modeled as infinite conducting sheets  $1 \mu\text{m}$  below and above the SET, respectively. With the substrate grounded and  $1 \text{ V}$  on the gate as the boundary conditions, I calculated the electric field  $50 \text{ nm}$  below the surface. This is the approximate depth at which the donors were located in the experiments ( $30 \text{ nm}$  below a  $20 \text{ nm}$  oxide). I normalized this by the field obtained with the boundary conditions reversed, giving  $\alpha$  by definition, and obtained  $\alpha = 0.01$  beneath the SET island. This geometry and results for  $\alpha$  are shown in Figure 3.12.

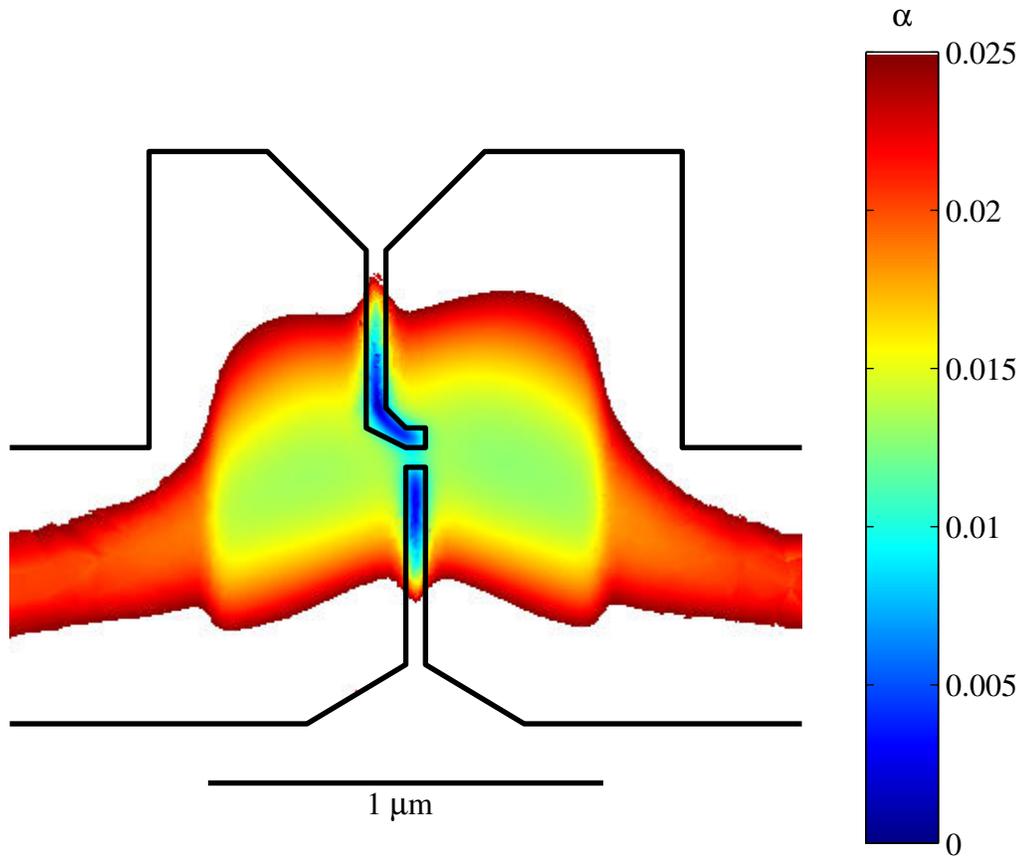


Figure 3.12: Plot of screening ratio  $\alpha$  vs. position in the  $x$ - $y$  plane, 50 nm below the surface of the wafer. The substrate and gate are modeled as conducting sheets 1  $\mu\text{m}$  below and above the SET. The leads and island are outlined in black, with the island consisting of a small 50 nm strip near the center connecting the two leads. In this region  $\alpha = 0.01$ .

In contrast with  $\alpha$ ,  $C_s$  and  $C_g$  depend very strongly on the geometry of the SET island, so that approximating the SET island as a rectangular block of conductor is not necessarily an accurate approximation when calculating the capacitances. Nevertheless I made this approximation, treating the island as a  $50 \text{ nm} \times 50 \text{ nm} \times 100 \text{ nm}$  block on top of the leads. With this geometry the FEMLAB model gave  $C_s \approx 0.5 \text{ aF}$  and  $C_g \approx 0.25 \text{ aF}$ . We can compare these with approximate parallel plate values:

$$C_s = \frac{\epsilon A}{d} \quad (3.44)$$

$$= \frac{12\epsilon_0 \times (50 \text{ nm})^2}{1 \mu\text{m}} \quad (3.45)$$

$$= 0.26 \text{ aF} \quad (3.46)$$

and

$$C_g = \frac{\epsilon A}{d} \quad (3.47)$$

$$= \frac{\epsilon_0 \times 50 \text{ nm} \times 100 \text{ nm}}{1 \mu\text{m}} \quad (3.48)$$

$$= 0.044 \text{ aF} \quad (3.49)$$

The estimates for  $C_s$  differ by a factor of 2, mostly because the parallel plate value underestimates the field concentration near the island. The values for  $C_g$  differ by a factor of 5, both because the parallel plate value underestimates the field concentration near the island and because it neglects field lines terminating on the sides of the island. As a further check I can compare these values with those obtained experimentally. As I discuss in more detail in Sections 4.7 and 4.8, I obtained typical values of  $C_s \approx 1\text{-}2 \text{ aF}$  and  $C_g \approx 2.5 \text{ zF}$ . We need to scale these by the appropriate dielectric separation for proper comparison. In practice the substrate was  $300 \text{ nm}$  below the surface instead of  $1 \mu\text{m}$ , so that the comparable capacitance would be  $0.3\text{-}0.7 \text{ aF}$ , a value that agrees well with the

simulated 0.5 aF. The gate was about 25  $\mu\text{m}$  above the surface, so that a comparable capacitance would be 0.06 aF, a value that lies closer to the parallel plate estimate than to the simulation.

Substituting  $\alpha = 0.01$ ,  $C_s \leq 0.7$  aF, and  $C_g \geq 0.06$  aF into Equation 3.43, I find  $q/Q^0 \leq 0.1$ . So this geometry goes a long way toward shielding the donors from the control gate, but there is definite room for improvement.

Figure 3.13 shows a plot of simulated electric field magnitude in the  $y$ - $z$  plane with 1 V on the substrate. The field 50 nm below the wafer surface is uniform to within a few percent, but becomes significantly less uniform near the Si/SiO<sub>2</sub> interface. This is because the wafer surface is not uniformly covered with metallization: there is necessarily a gap between the leads. Even with a gap as narrow as 50 nm it is clear that there will be nonuniformity in the field at distances less than 50 nm from the gap. This may be a problem if the field components in the  $x$ - $y$  plane are too strong, because the confinement of an ionized donor electron at the interface, discussed in Section 3.1.2, is relatively weak. If the the potential minimum does not lie near the SET island/donor system the electron may be lost permanently.

### 3.2.2 Single electron transistor charge sensitivity

SETs are known to be very sensitive charge detectors, with charge sensitivity approaching the quantum limit.[70] The SETs I fabricated for this work had a charge sensitivity  $\sim 100 \mu\text{e}/\sqrt{\text{Hz}}$  around 1 kHz even when measured with room temperature electronics. However, this charge sensitivity refers to charge induced on the island of the SET, not to charge moving near the island. I used FEMLAB to get an estimate of the charge that should be induced on the SET island by an electron moving between its donor site and the Si/SiO<sub>2</sub> interface.

The most satisfying result would be to obtain a plot of the induced island charge as a function of the electron's stipulated position. In principle this could be achieved by

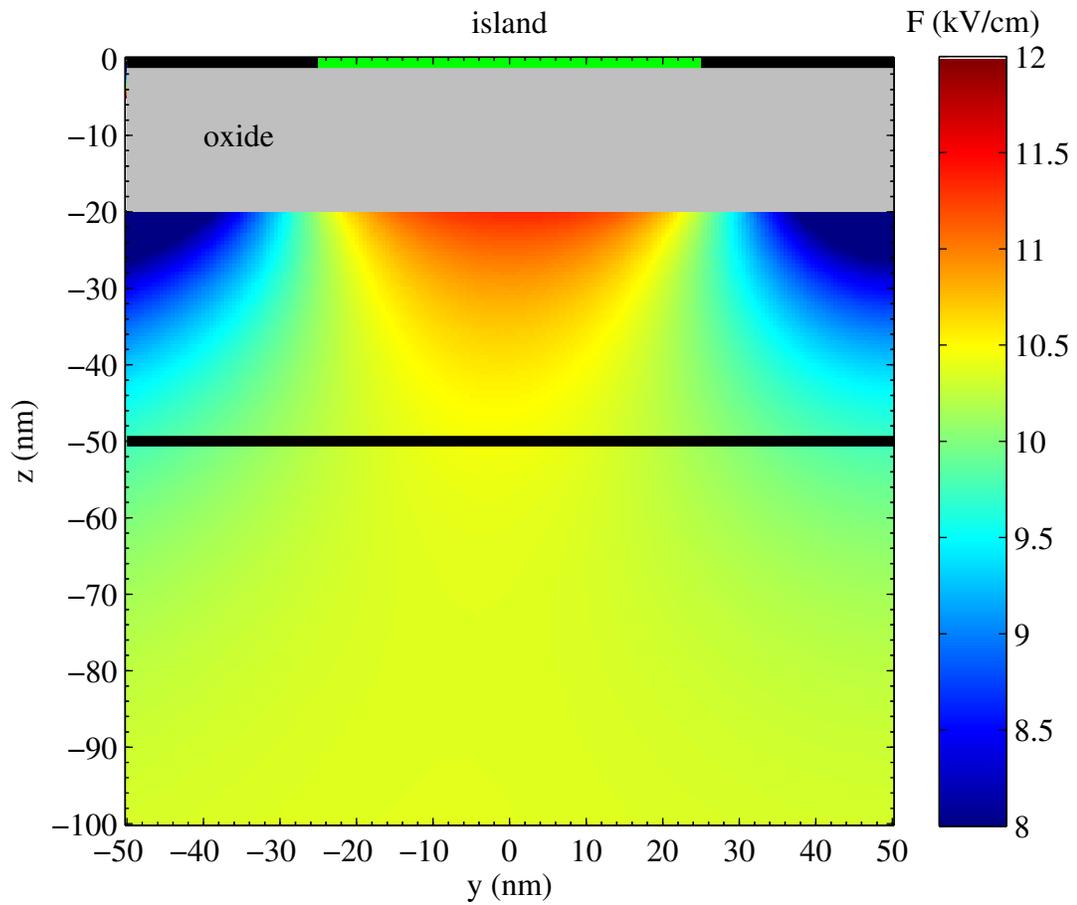


Figure 3.13: Plot of electric field magnitude in the  $y$ - $z$  plane beneath the SET island with 1 V applied to the substrate. The horizontal line at 50 nm represents the approximate depth of P donors. The field is uniform to better than 10% at the donor depth, but only to about 40% near the Si/SiO<sub>2</sub> interface, where the gap between the SET leads has a larger effect.

treating the electron as a point particle and solving Poisson's equation for every possible electron location. Integration of the resulting island surface charge density would then give the induced island charge for an electron at that particular point. However, this method would be time consuming and computationally intensive, and there is an easier way to solve the problem which I will outline now.

Consider a system of isolated conductors  $\{i\}$  in two different configurations; in the first configuration they contain charges  $Q_i$  at potentials  $V_i$ , and in the second charges  $Q'_i$  at potentials  $V'_i$ . Then Green's reciprocity theorem states

$$\sum_i Q_i V'_i = \sum_i Q'_i V_i. \quad (3.50)$$

I have not found a satisfactory proof of this in the literature so I reproduce my own proof here.

$$\int_{\Omega} \mathbf{E} \cdot \mathbf{D}' d^3 r = \int_{\Omega} (-\nabla\phi) \cdot \mathbf{D}' d^3 r \quad (3.51)$$

$$= \int_{\Omega} \phi \nabla \cdot \mathbf{D}' d^3 r - \int_{\Omega} \nabla \cdot (\phi \mathbf{D}') d^3 r \quad (3.52)$$

$$\int_{\Omega} \phi \nabla \cdot \mathbf{D}' d^3 r = \int_{\Omega} \phi \rho d^3 r \quad (3.53)$$

$$= 0 \text{ (because } \rho = 0 \text{ in the bulk.)} \quad (3.54)$$

$$\int_{\Omega} \nabla \cdot (\phi \mathbf{D}') d^3 r = \int_{\partial\Omega} \phi \mathbf{D}' \cdot \hat{\mathbf{n}} dA \quad (3.55)$$

$$= \int_{\partial\Omega} \phi \sigma' dA \quad (3.56)$$

$$= \sum_i V_i \int_{\partial\Omega_i} \sigma' dA \quad (3.57)$$

$$= \sum_i V_i Q'_i. \quad (3.58)$$

However we see also that

$$\int_{\Omega} \mathbf{E} \cdot \mathbf{D}' d^3r = \int_{\Omega} \epsilon \mathbf{E} \cdot \mathbf{E}' d^3r \quad (3.59)$$

$$= \int_{\Omega} \mathbf{D} \cdot \mathbf{E}' d^3r \quad (3.60)$$

*QED*

Now consider a particular set of conductors: the leads and island of a single electron transistor, any other nearby conductors, and a nearby electron modeled as a small conducting sphere centered at  $\mathbf{x}$ . Assume that all conductors except the SET island and the electron are grounded at all times. And consider the following configurations:

	$Q_{\text{island}}$	$Q_{\text{electron}}$	$V_{\text{island}}$	$V_{\text{electron}}$
unprimed	$Q$	$e$	$0$	???
primed	$Q$	$0$	$V$	$V\psi(\mathbf{x})$

The unprimed situation corresponds to an electron at  $\mathbf{x}$  inducing a charge  $Q$  on the island of the SET, which is grounded. The potential at the electron is left undefined. The primed situation corresponds to removing the electron from  $\mathbf{x}$  but isolating the island of the SET, so that the island charge remains  $Q$  but its potential changes to  $V$ . Because in this case all conductors are grounded but the island, with  $V_{\text{island}} = V$ , the potential at  $\mathbf{x}$  is the solution to Laplace's equation, which I call  $V\psi(\mathbf{x})$ . By Green's reciprocity theorem we have

$$QV + eV\psi(\mathbf{x}) = Q \cdot 0 + 0 \cdot ??? \quad (3.61)$$

$$= 0 \quad (3.62)$$

$$Q = -e\psi(\mathbf{x}). \quad (3.63)$$

Thus the charge induced on the SET island by an electron at position  $\mathbf{x}$  is just the solution to Laplace's equation at  $\mathbf{x}$  given a unit potential on the SET island with all other conductors grounded and the electron absent. We can therefore calculate Laplace's equation a

single time for a given SET geometry and know the charge induced on the SET island by an electron at any position. The result for my SET geometry is shown in Figure 3.14. Although this simulation included the effect of the conducting substrate  $1\ \mu\text{m}$  beneath the surface, it is nearly irrelevant because the substrate is much farther away than the island dimensions. For an electron directly beneath the SET island that moves from its donor site  $50\ \text{nm}$  below the surface to the interface  $20\ \text{nm}$  below, the change in induced island charge is  $0.15\ e$ . To distinguish this motion above the  $100\ \mu\text{e}/\sqrt{\text{Hz}}$  noise of a typical SET at  $1\ \text{kHz}$  would require an averaging time of  $\sim \left(100\ \mu\text{e}/\sqrt{\text{Hz}}/0.15\ e\right)^2 \sim 0.5\ \mu\text{sec}$ .

### 3.3 Synopsis

To recap, the SET geometry I have designed, with wide leads and a nearby back gate, should shield donors from  $90\%$  of the effects of the SET biasing gate. While this represents a reasonable first try, significant improvement could be realized with even wider leads. The substrate-induced field in this design is uniform to around  $10\%$ , which means that the critical ionization voltage for donors at a uniform depth beneath the SET is also uniform to  $10\%$ . The signal measured using this design should exceed  $0.1\ e$ , large enough to substantially exceed the noise in our experimental setup.

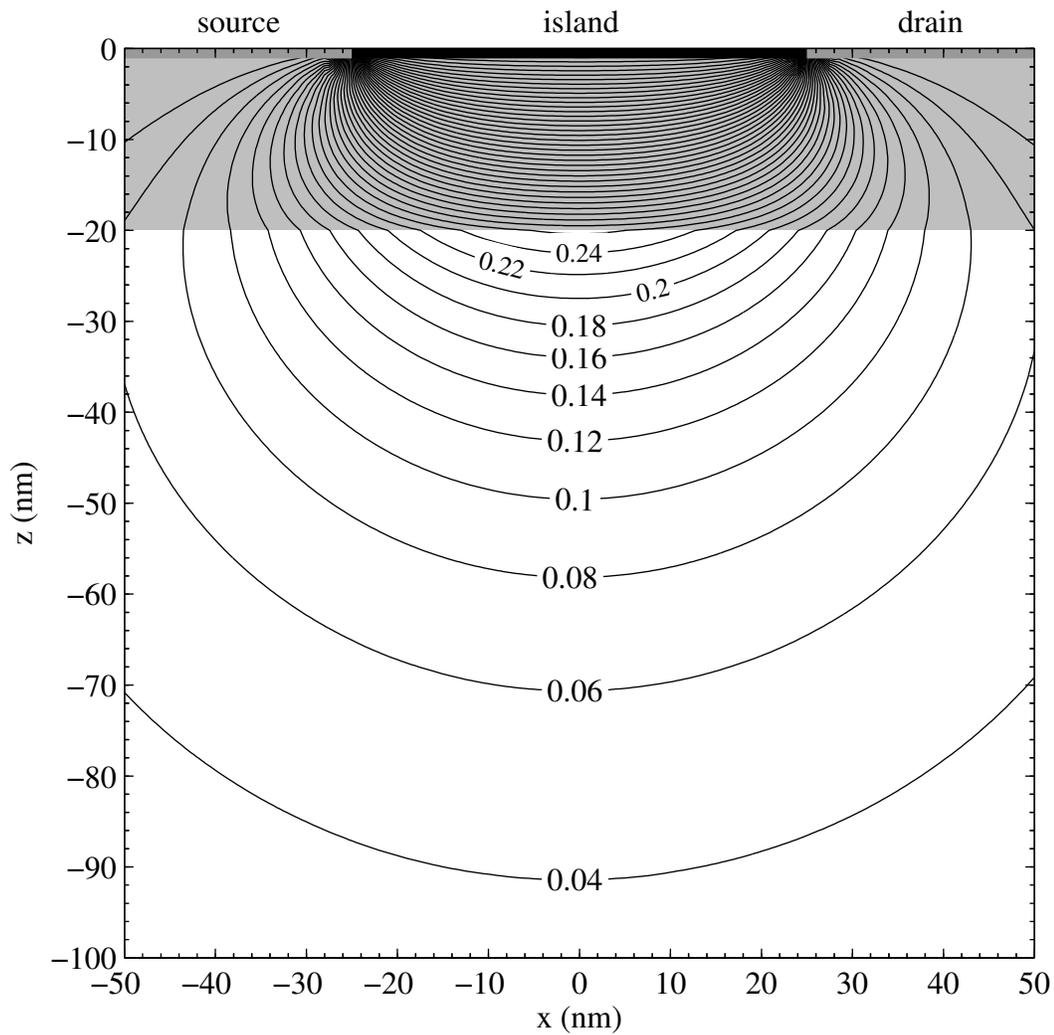


Figure 3.14: Contour plot in the  $x$ - $z$  plane of charge induced on the island of our SET by a nearby electron as a function of the electron's position. The unit is one electron. The gray area represents the  $\text{SiO}_2$  layer.

## Chapter 4

### Fabrication and measurement of SETs coupled to individual donors

#### 4.1 Configuration of an SET coupled to an individual donor

Each of my devices consists of several Al SETs fabricated on the surface of a doped, oxidized Si wafer. The Si oxide is 20 nm thick. The wafer is heavily doped with B acceptors about 1  $\mu\text{m}$  below the surface to form a back gate (which I call either the back gate, or more simply the substrate). The P donors we want to study are much shallower, about 50 nm below the surface, and the doping density is low enough that only a few donors lie beneath the SET island. Each SET has an island whose contact area with the substrate is about 50 nm  $\times$  50 nm, and it has very wide leads close together that act to shield the donors below from external fields, as discussed in Section 3.2.1. There is a gate above the surface of the wafer which controls the operating point of the SET and in the ideal situation the fields from this gate should be kept out of the substrate in the vicinity of the SET island by the ground plane formed by the wide SET leads. An equivalent circuit model of the device is shown in Figure 4.1, with a more realistic diagram of the layout in Figure 4.2.

#### 4.2 Fabricating an SET coupled to an individual donor

Fabrication of these samples consumed the largest part of my time, and the recipe grew ever more complicated as the research progressed. I will give a correspondingly detailed account of that recipe now, including how to avoid some common pitfalls. The recipe can be divided into four distinct steps: doping and oxidizing the substrate, photolithography for the leads and bond pads, e-beam lithography and Al evaporation for the

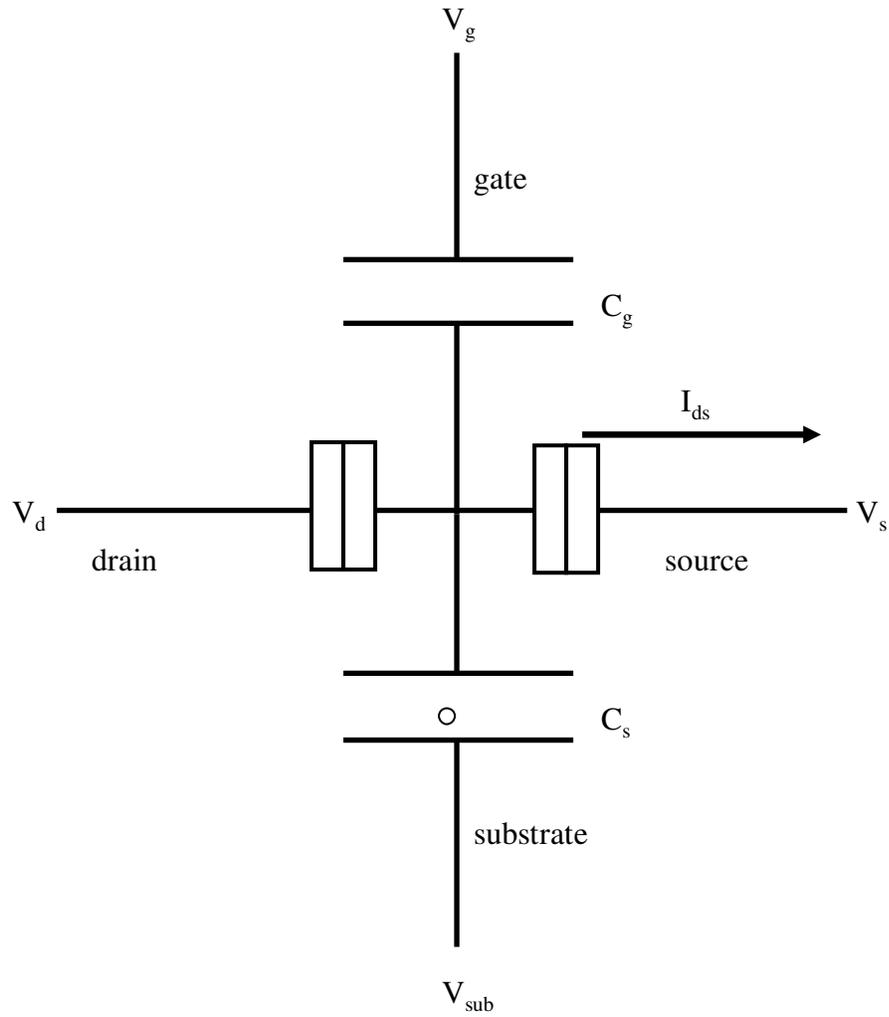


Figure 4.1: Equivalent circuit diagram of a single electron transistor coupled to a single P donor in Si. Source and drain electrodes are attached to the island by small tunnel junctions. Both the gate and the substrate couple to the island capacitively and modulate the drain-source current. The circle between the substrate and the island represents a donor. When the electric field between substrate and island reaches some critical value the donor electron ionizes, increasing the effective polarizability of the dielectric and changing the conductance of the SET.

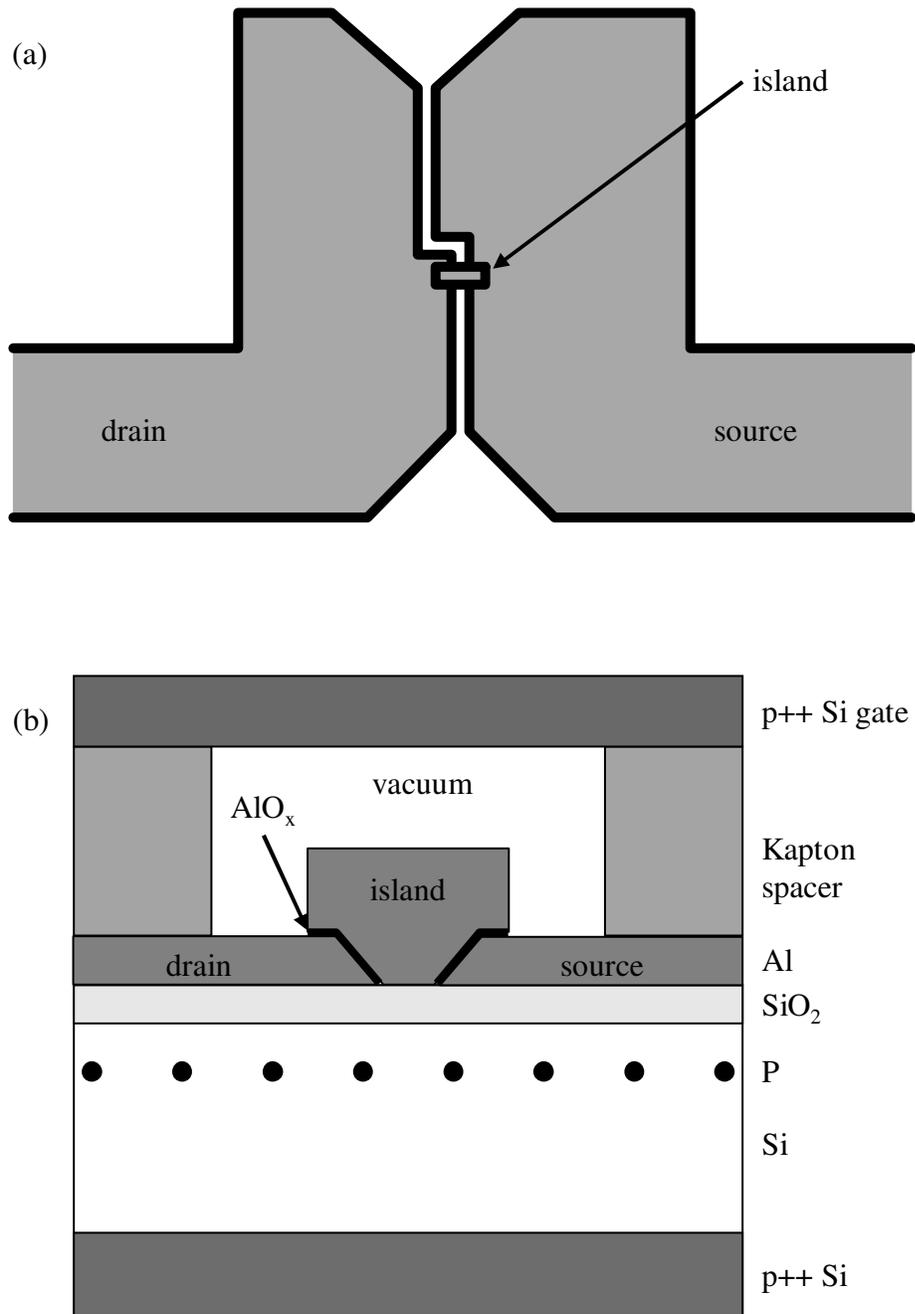


Figure 4.2: Layout of a single electron transistor coupled to a few P donors in Si. (a) Top view of the Al pattern showing the wide leads separated by a 50 nm gap. The island is 50 nm wide and 150 nm long, but only 50 nm of this length are in contact with the substrate. (b) Side view showing the gate, SET, and substrate. The gate is separated from the substrate by Kapton spacers at either end, about 25  $\mu\text{m}$  thick.

SETs, and wiring.

## 4.2.1 Doping and oxidizing the substrate

### Back gate

Application of an electric field to the donors requires fabrication of a suitable gating structure. We chose to use a back gate created via high energy ion implantation of B to a depth of  $1\ \mu\text{m}$ . While it is possible in principle to gate the donors with a metallic gate near the SET on the surface of the wafer, a back gate will produce a more uniform and easily understood electrostatic field than a side gate configuration. So although I used metallic side gates in my earliest experiments, I soon switched to a p<sup>++</sup>-Si back gate. While it is also possible to metallize the back surface of the wafer to create a back gate, this arrangement is far from ideal because it substantially lessens the screening of the donors from external fields; the screening is most effective when the dimensions of the Al metallization on the wafer surface are much larger than the distance to the back gate. Having a back gate so far away also introduces all of the impurities between the back and front of the wafer into the experiment, which is clearly something that we would like to avoid. To be quantitative about that, consider the best wafer we can hope to obtain, having a resistivity  $\sim 10\ \text{k}\Omega\text{-cm}$ . For a p-type wafer this yields a lower bound for the impurity concentration of  $10^{12}\ \text{/cm}^3$ .<sup>[71]</sup> For a  $300\ \mu\text{m}$  thick wafer this gives a 2-D density of  $3 \times 10^{10}\ \text{/cm}^2$  which approaches the density of P donors I used in this experiment. Perhaps more importantly, use of a back gate  $300\ \mu\text{m}$  away necessarily would require much larger applied voltages to achieve similar electric fields, voltages which could easily lead to a destroyed device if the surface oxide broke down even in a small region.

Sample fabrication begins with a 2-inch, <100>, float-zone, n-type wafer, resistivity  $10\ \text{k}\Omega\text{-cm}$ . Before any lithography is done I need alignment marks. The recipe for these is:

1. Spin HMDS adhesion promoter, 4000 rpm, 60 sec.
2. Spin OiR 908-35 positive photoresist,[72] 4000 rpm, 60 sec. For all resist spinning steps I suggest ramping up the spin speed at  $\sim 1000$  rpm/sec to get a more uniform layer.
3. Bake on hot plate, 90°C, 3 min.
4. UV expose through mask, 12 mW power, 13 sec.
5. Develop in OPD 4262,[73] 60 sec.
6. Rinse in deionized water, 30 sec.
7. Blow dry with N<sub>2</sub> gas.
8. Etch alignment marks in reactive ion etcher. Use process *dansix* for 1 min. and *mesasix* for 5 min. These are pure SF<sub>6</sub> etches.
9. Ultrasonicate in acetone, methanol, and isopropanol, 5 min. each.

Next I fabricate the back gate. As mentioned earlier, this is done with ion implantation of B. To avoid large parasitic capacitances between the back gate and the Al leads of the single electron transistor, I use a mask for this step which confines the doping to a small region. The recipe for this mask, made of Al, is:

1. Evaporate Al in e-beam evaporator, 1500 nm.
2. Spin HMDS adhesion promoter,[74] 4000 rpm, 60 sec.
3. Spin OiR 908-35 positive photoresist, 4000 rpm, 60 sec.
4. Bake on hot plate, 90°C, 3 min.
5. UV expose through mask, 12 mW power, 13 sec.
6. Develop in OPD 4262, 60 sec.
7. Rinse in deionized water, 30 sec.
8. Blow dry with N<sub>2</sub> gas.
9. Etch in JT Baker 80-15-3-2 Al etchant,[75]  $\sim 60$  min.
10. Flowing rinse in deionized water, 5 min.
11. Blow dry with N<sub>2</sub> gas.

12. Ultrasonicate in acetone, methanol, and isopropanol, 5 min. each.
13. Blow dry with N<sub>2</sub> gas.

The wafers are then sent to Core Systems[76] for ion implantation of B at an energy of 400 keV and a density of  $2.5 \times 10^{14}$  /cm<sup>2</sup>. This is the maximum energy that Core Systems can provide. Earlier samples were sent to Implant Sciences,[77] who can provide a 500 keV acceleration. The areal density of the implant was chosen to insure that the peak acceptor concentration would exceed the metal-insulator transition and so conduct at low temperatures.

## Oxidation

There is a trade-off in these experiments between the desire to have as thin an oxide as possible, thereby maximizing the sensitivity of the SET to charge motion beneath the oxide, and the desire for a thick oxide, which is generally more ideal, more robust to damage, and more free of defects. In the end we chose 20 nm, which has a relatively high breakdown voltage near 20 V, but is also thin enough for good charge sensitivity as described in Section 3.2.2. After the wafers have been implanted with B they are oxidized as follows:

1. Etch in JT Baker 80-15-3-2 Al etchant, ~ 60 min to remove implant mask.
2. Flowing rinse in deionized water, 5 min.
3. Blow dry with N<sub>2</sub> gas.
4. Ultrasonicate in acetone, methanol, and isopropanol, 5 min. each.
5. Blow dry with N<sub>2</sub> gas.
6. Piranha soak, 10 min. This consists of 150 ml of concentrated H<sub>2</sub>SO<sub>4</sub> heated in a 200 ml beaker on a 120°C hot plate to which I added 50 ml of 30% H<sub>2</sub>O<sub>2</sub> right before introducing the wafer.
7. Flowing rinse in deionized water, 5 min.
8. Blow dry with N<sub>2</sub> gas.

9. Dip in HF/H<sub>2</sub>O 1:10, ~ 5 sec.
10. Dip in deionized water, ~ 5 sec.
11. Blow dry with N<sub>2</sub> gas.
12. Anneal in a tube furnace, 950°C in O<sub>2</sub> for 25 min., 950°C in N<sub>2</sub> for 30 min., 450°C in forming gas (H<sub>2</sub>+N<sub>2</sub>) for 30 min.

This gives an oxide thickness of 180 Å with uniformity ~ 5 Å across the wafer, as measured with an ellipsometer. The high temperature steps also activate the implanted acceptors.

Figure 4.3 shows a Monte Carlo simulation of the implanted B distribution (assuming a 500 keV implant) before oxidation and secondary ion mass spectrometry (SIMS) data from an actual sample after the oxidation step. The spreading of the SIMS distribution compared with the simulation is most likely due to diffusion during oxide growth.

## P donor implantation

The goal of these experiments was to see differences between SETs with and without a P donor layer beneath them. To achieve this while controlling as many other variables as possible, I used a mask for the P implant. Instead of an Al mask, as is used for the B implant, I use a simple photoresist mask. The Al mask is necessary for the acceptors because higher density and energy implantation hardens a resist mask, making removal nearly impossible. This is not the case for the lower density and energy P implants. The recipe for this mask was:

1. Spin HMDS adhesion promoter, 4000 rpm, 60 sec.
2. Spin OiR 908-35 positive photoresist, 4000 rpm, 60 sec.
3. Bake on hot plate, 90°C, 3 min.
4. UV expose through mask, 12 mW power, 13 sec.
5. Develop in OPD 4262, 60 sec.
6. Rinse in deionized water, 30 sec.

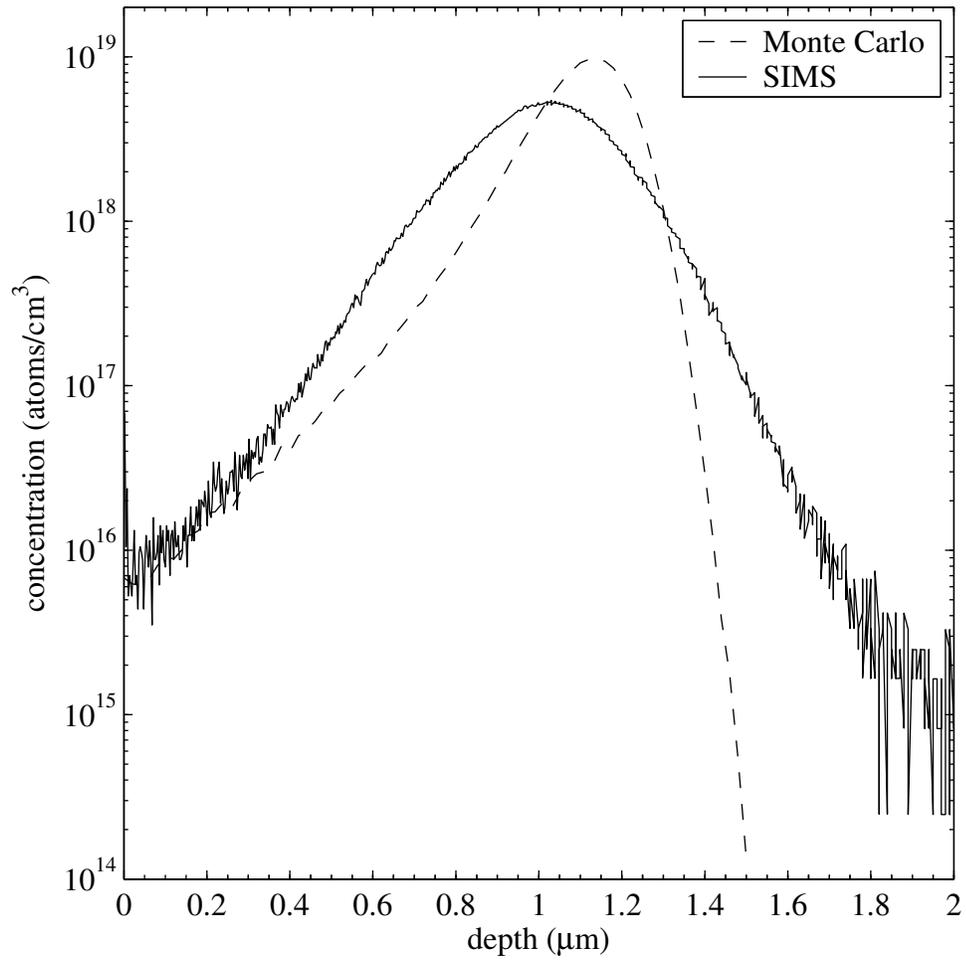


Figure 4.3: B concentration as a function of depth beneath the surface for a sample implanted at 500 keV and at a density of  $2.5 \times 10^{14} / \text{cm}^2$ . The solid curve shows SIMS data from an actual sample after growth of a 200 Å thermal oxide. The dashed curve shows the result of a Monte Carlo simulation. The spreading of the SIMS distribution compared with the simulation is most likely due to diffusion during oxide growth.

7. Blow dry with N<sub>2</sub> gas.

The wafers are then sent to Core Systems for ion implantation of P at an energy of 35 keV. I made two sets of samples, the first at a density of 10<sup>12</sup> /cm<sup>2</sup> and the second at a density of 10<sup>11</sup> /cm<sup>2</sup>, and data from these samples is presented in depth in Chapter 4.3.3. Figure 4.4 shows a Monte Carlo simulation of the depth of this implant, from which we can see that the peak density should lie below the metal-insulator transition ( $3.5 \times 10^{18}$  /cm<sup>3</sup>) even for a sample implanted at 10<sup>12</sup> /cm<sup>2</sup>. This distribution was not checked with SIMS because Si-H molecules near the surface, with a mass nearly that of P, complicate such a measurement. The resist is then stripped and the dopants activated:

1. Ultrasonicate in acetone, methanol, and isopropanol, 5 min. each.
2. Blow dry with N<sub>2</sub> gas.
3. Anneal in a rapid thermal annealer, 950°C for 5 sec.

The anneal temperature was chosen based on an earlier test. I sent a high resistivity wafer out for implantation of P at the 10<sup>12</sup> /cm<sup>2</sup> level and annealed pieces of it at 850°C, 950°C, and 1050°C, each for 5 sec. Each piece then had a measured resistivity of  $\sim 5$  k $\Omega/\square$  at room temperature, while an unannealed piece had resistivity 1 M $\Omega/\square$ . I concluded that annealing at higher temperatures did not increase the activation ratio. If we assume full activation we calculate a mobility of 1250 cm<sup>2</sup>/V-s, a reasonable value for the room temperature mobility of electrons in bulk Si at this impurity concentration.[78] There is some evidence that P diffuses very quickly near a SiO<sub>2</sub> interface due to excess interstitials there.[23] If this is truly the case then it would be worthwhile investigating other column V donors for use in these experiments.

#### 4.2.2 Photolithography for leads and bond pads

My e-beam lithography is too slow to be practical for fabrication of the leads and bond pads for SET devices. The most widely used technique for contacting Al SETs is to fabricate a pattern of leads and bond pads with photolithography. It is necessary

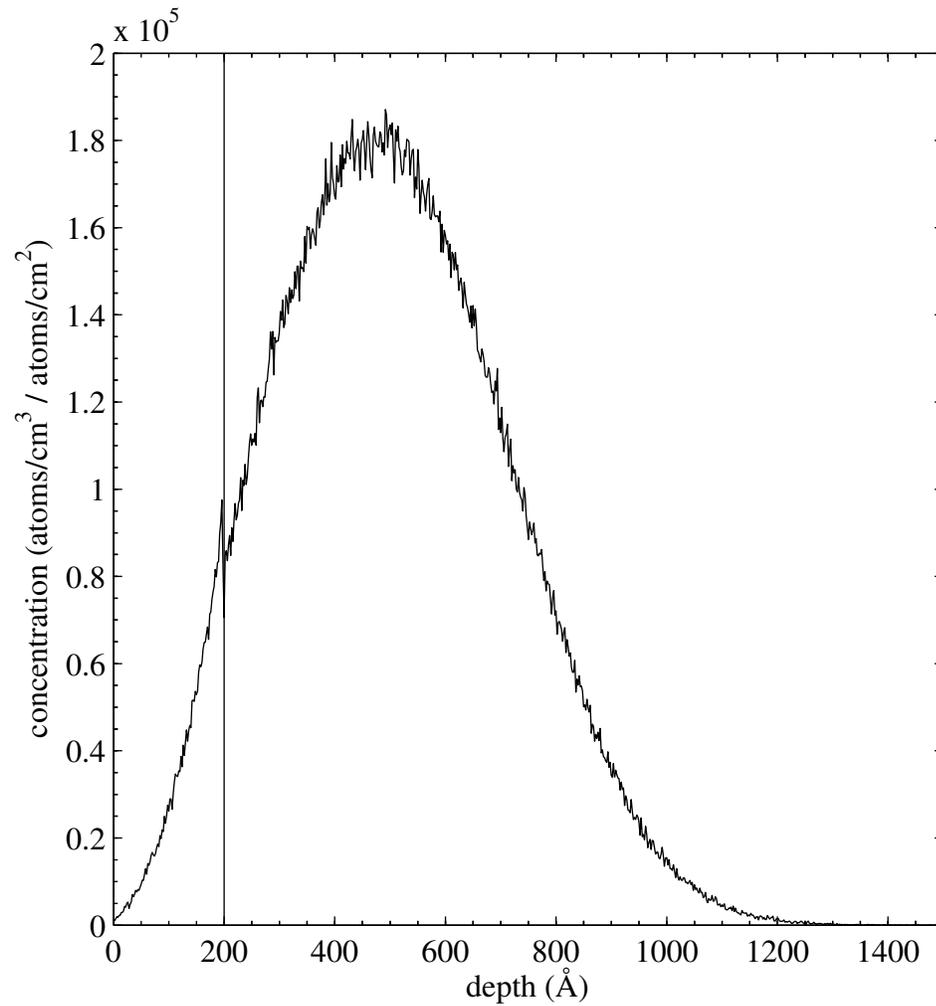


Figure 4.4: Monte Carlo simulation of P concentration as a function of depth beneath the surface for a sample implanted at 35 keV. The vertical line marks the SiO<sub>2</sub>/Si interface at a depth of 200 Å.

to use a metal that does not oxidize, usually Au, so that there can be good electrical contact between the leads and the Al SETs which are evaporated later. This was the route that I took for my initial experiments, and it worked well. Nevertheless it turned out that it did not meet my needs in the long term because we wanted to do subsequent high temperature processing of our samples. In particular we wanted to do a forming gas anneal at 425°C, a standard process in the CMOS industry that passivates dangling bonds at the Si/SiO<sub>2</sub> interface. When I tried this anneal with our Au/Pt/Ti leads I saw strange black coloration appearing where the Pt overlapped with the Al. I solved the problem by completely eliminating all metals but Al from the chips, developing a recipe to combine the photolithography for the bond pads and the e-beam lithography for the SETs into a single Al evaporation step. In brief, the recipe I developed uses photolithography to define the leads and bond pads in a layer of photoresist *above* the e-beam resist. This pattern is then transferred to the e-beam resist layers beneath it via reactive ion etching. The photoresist is selectively removed so that only the e-beam resist stack remains. The detailed recipe is:

1. Spin PMGI SF8 resist,[79] 5000 rpm, 60 sec.
2. Bake on hot plate, 180°C, 15 min.
3. Evaporate Ge in a thermal evaporator, 300 Å, ~ 5 Å/sec, base pressure < 2 × 10<sup>-6</sup> Torr.
4. Spin 2200PMMA A1 resist,[80] 3000 rpm, 60 sec.
5. Bake on hot plate, 180°C, 5 min.
6. Evaporate Au in a thermal evaporator, 150 Å, ~ 5 Å/sec.

These first steps put down what I call the e-beam resist stack. I will discuss its use in detail in Section 4.2.3. The recipe continues with the photolithography steps:

1. Spin HMDS adhesion promoter, 3500 rpm, 60 sec.
2. Spin OiR 906-10 positive photoresist,[81] 3500 rpm, 60 sec.
3. Bake on hot plate, 90°C, 60 sec.

4. UV expose through mask, 12 mW power, 5 sec.
5. Bake on hot plate, 120°C, 60 sec.
6. Develop in OPD 4262, 60 sec.
7. Rinse in deionized water, 30 sec.
8. Blow dry with N<sub>2</sub> gas.
9. Dip in GE-8148 Au etchant,[82] 4 sec.
10. Rinse in deionized water, 30 sec.
11. Blow dry with N<sub>2</sub> gas.
12. Ash using DESCUM (1.75 Torr O<sub>2</sub> at 100 W) in Matrix asher, 2 min.

The photolithographically defined pattern has now been transferred through both the Au layer on top of the e-beam resist stack and the PMMA. Etching stops at the Ge layer. The remaining steps remove the photoresist and coat the sample with a new layer of resist to protect it while it is diced into smaller chips:

1. UV expose without a mask, 12 mW power, 10 sec.
2. Develop in OPD 4262, 60 sec.
3. Rinse in deionized water, 30 sec.
4. Blow dry with N<sub>2</sub> gas.
5. Spin OiR 906-10 positive photoresist, 3500 rpm, 60 sec.
6. Bake on hot plate, 90°C, 60 sec.
7. Dice wafer into 6.4 mm × 11 mm rectangles using a wafer saw.

Figures 4.5 and 4.6 show how all of the doping and photolithography steps are aligned with each other.

### 4.2.3 E-beam lithography and Al evaporation

What remains is to write the SET patterns with e-beam lithography, use double-angle evaporation to make the junctions, lift off the remaining resist, and do a final forming gas anneal for Si/SiO<sub>2</sub> surface passivation.

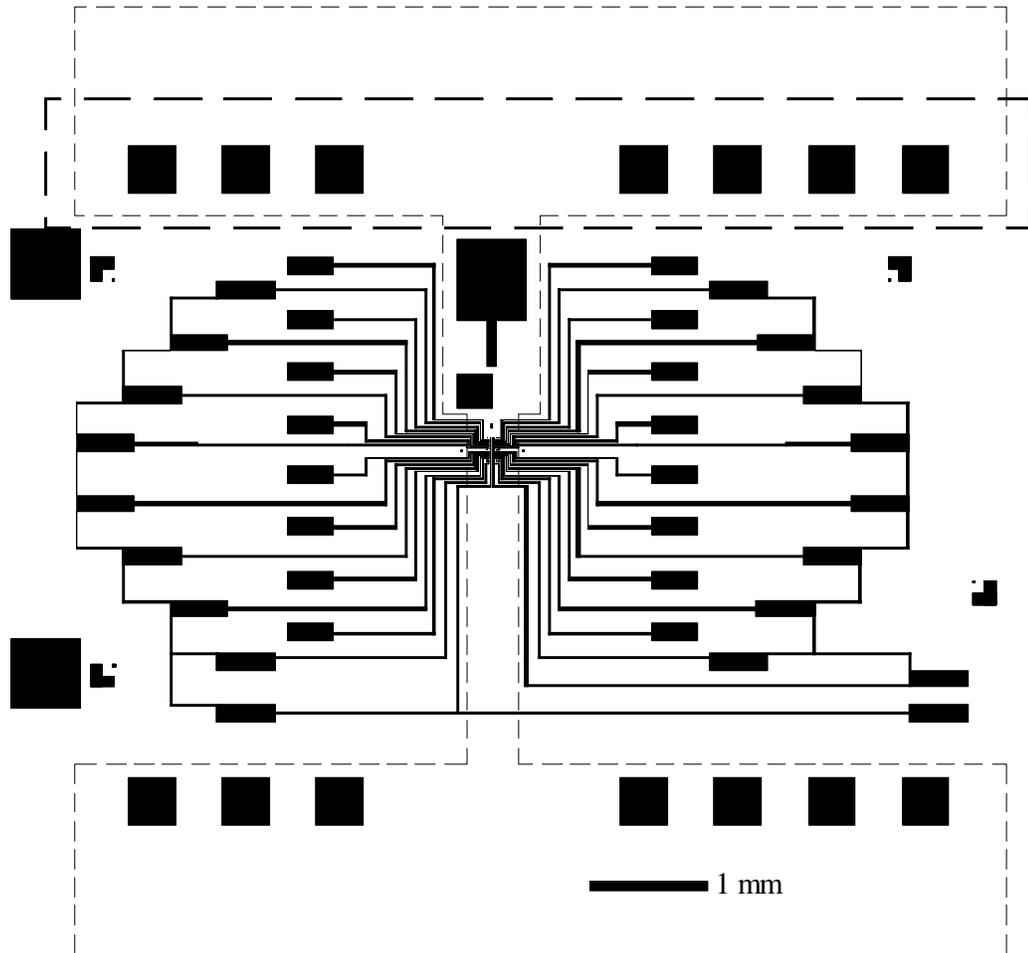


Figure 4.5: Three photolithography masks superimposed. Solid black areas will become an Al layer, comprising 14 capacitors (black squares) on the top and bottom, as well as the leads and bond pads of the SETs. The bond pads of the SETs are shorted together to provide protection from electrostatic discharge during wirebonding - these shorts are opened after wiring up the devices. The area outlined by the smaller dashes is implanted with B acceptors to form a back gate. The area outlined by longer dashes is implanted with P donors, so that there are a total of eight SETs with donors beneath them and another eight without.

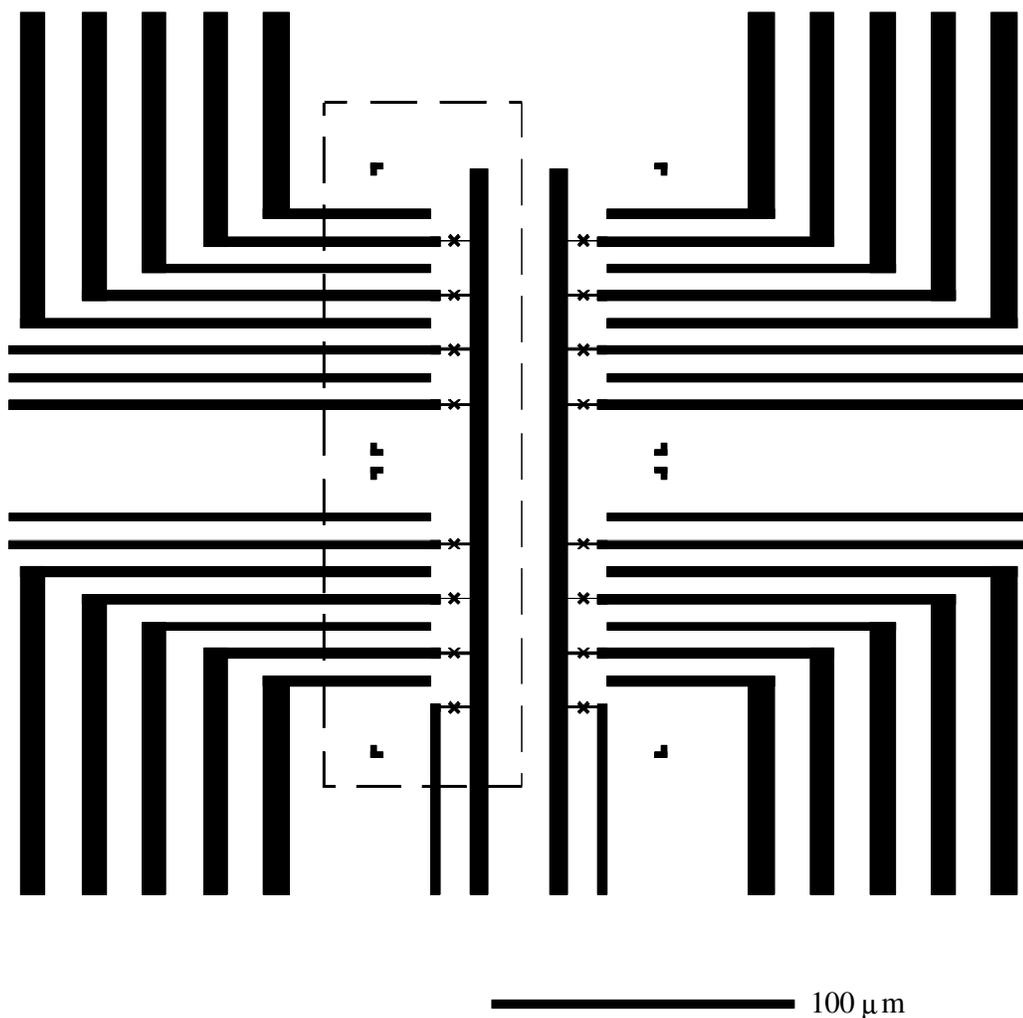


Figure 4.6: Magnified view of the center of Figure 4.5 showing Al leads in solid black, approximate SET positions marked with crosses, and an area implanted with P donors outlined with a dashed line. The B acceptor back gate lies beneath this entire pattern.

## E-beam lithography

1. Take one of the 6.4 mm × 11 mm diced chips.
2. UV expose without a mask, 12 mW power, 10 sec.
3. Develop in OPD 4262, 60 sec.
4. Rinse in deionized water, 30 sec.
5. Blow dry with N<sub>2</sub> gas.

This removes the protective layer of resist to expose the underlying e-beam resist stack.

1. E-beam expose the pattern. Further details at the end of this section.
2. Dip in GE-8148 Au etchant, 4 sec.
3. Rinse in deionized water, 30 sec.
4. Blow dry with N<sub>2</sub> gas.
5. Develop in MIBK/IPA 1:3, 60 sec.
6. Dip in IPA, 60 sec.
7. Blow dry with N<sub>2</sub> gas.
8. Etch pattern in reactive ion etcher using process *dansix* for 18 sec.
9. Ash using DESCUM (1.75 Torr O<sub>2</sub>) at 100 W in Matrix asher, 2 min. Repeat this step two more times, waiting for the sample to cool each time.

The e-beam has no trouble going through the 150 Å layer of Au. The Au serves two purposes: it contains e-beam alignment marks etched during the photolithography, and it provides a way of focusing the SEM near the writing area. By placing the e-beam in point mode, so that it stops rastering the beam and directs it toward a single point, it is possible to “burn” a hole into the resist which is good for focusing. I found that this was only possible with a metallic layer above the PMMA, and I chose Au instead of another metal because it provides good contrast for the alignment marks.

I use a JEOL 6500 SEM with Joe Nabity’s NPGS system to do the e-beam exposure. A typical e-beam pattern for one SET is shown in Figure 4.7. I use doses of 2.3 nC/cm

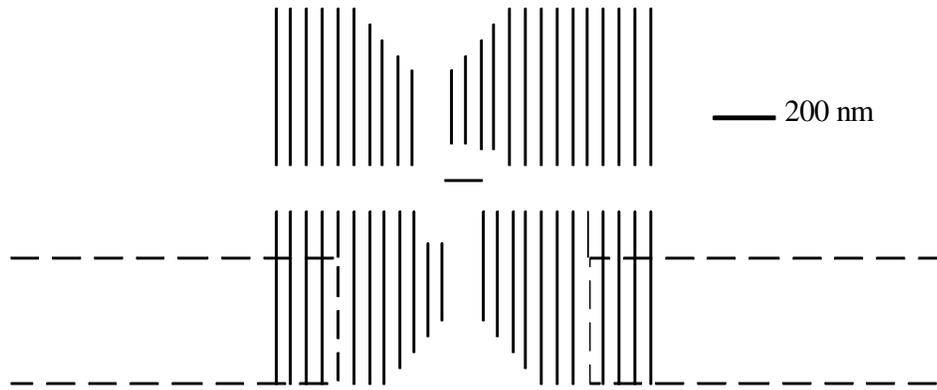


Figure 4.7: CAD file for e-beam writing with NPGS. The solid lines represent single traces of the beam. The areas outlined by dashed lines will be filled in by a serpentine sweep of the beam. Although the top and bottom groups of lines are disjoint, they will be electrically connected during the double angle evaporation.

for the lines and  $500 \mu\text{C}/\text{cm}^2$  for the areas. I use lines for the fine features to allow me more control over exactly how the features are written.

I note that GE-8148 etches Ge as well as Au, so that the photolithographically defined features (already transferred to the PMMA layer) will be broadened if the sample is immersed for too long. The pattern is developed in MIBK/IPA and then transferred via reactive ion etching to the Ge layer. The ashing steps create an undercut in the PMGI which is a necessary component of the double-angle evaporation used to create the SET tunnel junctions. The undercut rate appears to be a function of temperature, so I allow the sample to cool between the ashing steps. I prefer to use a dry etch for the undercut because it doesn't expose delicate structures in the Ge layer to the surface tension of a wet etch.

### Al evaporation and forming gas anneal

I use the standard technique of double-angle evaporation to fabricate the tunnel junctions of the SETs.[83] Briefly, a first layer of Al is evaporated at one angle through the Ge mask. This layer is then oxidized in a pure  $\text{O}_2$  atmosphere, and a second layer

of Al is evaporated at a different angle to form the junction. The evaporator should be as clean and baked out as possible for reproducible results using this technique. I did not consistently get the resistances I wanted for the SETs until I stopped using a diffusion pumped evaporator that was vented before each evaporation. Instead I built a turbo pumped evaporator with a load-lock system so that the chamber would be well pumped out and outgassed before every evaporation, reaching a base pressure  $\sim 10^{-7}$  mbar. With this system SET resistances became reproducible in the 50% range from run to run. The evaporation steps are:

1. Evaporate 300 Å Al, 5 Å/s, +15.5°.
2. Introduce 30 mTorr of pure O<sub>2</sub> into the chamber, wait 3 min.
3. Pump out the chamber to high vacuum again.
4. Evaporate 800 Å Al, 5 Å/s, -15.5°.

I typically do not start the evaporations until the pressure in the chamber is well below  $10^{-6}$  mbar, although it may rise as high as  $3 \times 10^{-6}$  mbar during evaporation due to heating of adsorbed gases on the chamber walls. The lift-off and annealing steps are:

1. Immerse in N-methyl pyrrolidone (NMP), 80+°, until the Al film peels off, about 10-20 min.
2. Spray with isopropyl alcohol.
3. Blow dry with N<sub>2</sub> gas.
4. Anneal in a tube furnace, 425°C in forming gas, 30 min.

The lift-off typically requires some “encouragement” by scraping along the edge of the sample with tweezers. This is because some Al adheres during double-angle evaporation to the edges of the sample where there is no resist. Figure 4.8 shows a scanning electron micrograph of an SET I built using this procedure.

The annealing changes the resistances of the tunnel junctions. Because the geometry of the SETs was changed simultaneously with the addition of the forming gas anneal to the process, it is difficult to compare resistances from samples before and after I started

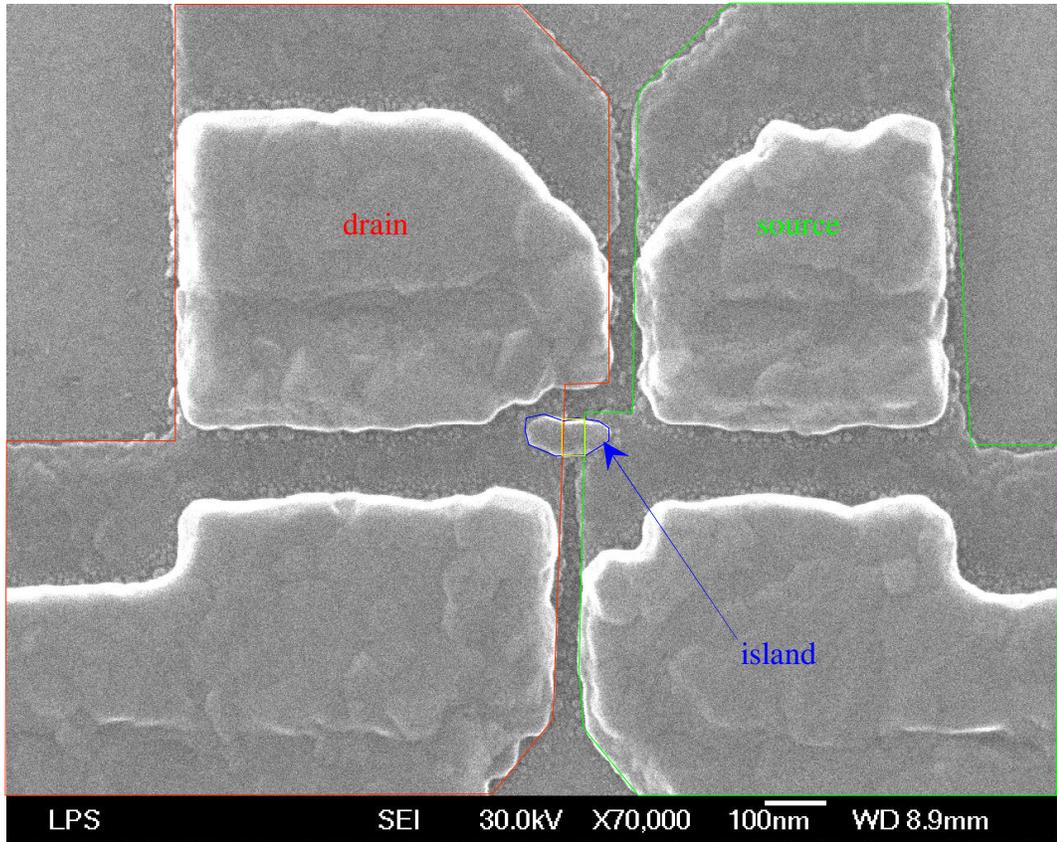


Figure 4.8: SEM image of one of my SETs showing the wide leads separated by a 50 nm gap and the 150 nm long island. The area of the island in contact with the substrate, outlined in yellow, is about 50 nm  $\times$  60 nm.

doing this anneal step. I can say with confidence that the resistance rises by a factor of 5-10 from the anneal. This agrees reasonably well with another published result.[84] I do not believe that the capacitance of the junctions changes by more than a few tens of percent.

#### 4.2.4 Wiring

It is not possible in practice to gate the single electron transistors I have described using a traditional gate on the substrate surface. This is because the island is shielded effectively by the wide SET leads, as desired. For a gate placed right in proximity with the leads the  $1 e$  period is still over 20 V! Such a voltage is unacceptable because it will very likely lead to breakdown of the surface oxide. Instead I use a gate separated from the sample by a thin, 25  $\mu\text{m}$  (1 mil) Kapton spacer. Kapton has a dielectric strength greater than 2 kV/mil, so breakdown should not be a problem even for the  $\pm 450$  V potentials I apply. The gate itself is a 0.5 mm  $\times$  6 mm piece of n++-doped Si that still conducts for  $T \rightarrow 0$ . Si was chosen instead of metal in order to most closely match the thermal contraction of the substrate.

I start by placing the sample, patterned side up, on a heat stage underneath an optical microscope. I cut small,  $\sim 0.5$  mm wide, rectangles of adhesive-free Kapton and place one at either end of the sample by hand with tweezers, taking care not to let them touch any of the Al metallization. I then place the gate lengthwise across the Kapton pieces, making sure that it overlaps with the center of the sample where the SETs are located. Using an XYZ $\theta$  translation stage with tweezers attached I apply gentle pressure to the gate so that it lies flat against the spacers. Too much pressure will bend the gate all the way down to the sample surface. I apply an extremely small quantity of Epo-Tek H72 epoxy[85] at either end using a piece of 1 mil diameter wire and cure it at 100°C for 20+ min.

After gluing the gate above the sample I use In solder to attach 10  $\mu\text{m}$  Au wires to

it and to the heavily doped substrate. The In diffuses enough during soldering to make good ohmic contact to both pieces of Si. Then I use a black wax to mount the sample on a 14-pin DIP header.

Wiring up Al single electron transistors is the most common time for them to be damaged. The small tunnel junctions are extremely sensitive to static electricity, and every effort must be taken to ensure that no large potentials appear across them. My lithography pattern includes shorts between the drain/source leads of each SET so that they are constantly protected. During sample wiring the DIP header is held in a DIP socket with all leads shorted together and to ground. I use a wedge bonder to attach Al wires, bonding directly from the Au-plated DIP header pins to the Al bond pads on the chip. Then while the leads are still shorted together and to ground I use a fine diamond scribe to cut through the Al shorts on the chip. I found that this scribing step by itself can destroy SETs if the leads are not shorted together by the DIP socket. Beyond this point I use extreme care when transporting the sample, never moving it without having all the leads shorted. Figure 4.9 shows a photograph of a representative sample after mounting on its chip header and wiring up.

### 4.3 Experimental techniques

I made a variety of measurements on these samples, from simple measurements of the SET resistance at room temperature to more complicated ac measurements using feedback in a dilution refrigerator. The following sections describe the measurement techniques I used.

#### 4.3.1 Resistance characterization

The easiest sanity check, and the first measurement I would make after sample fabrication, was a simple measurement of the SET resistances at room temperature. I

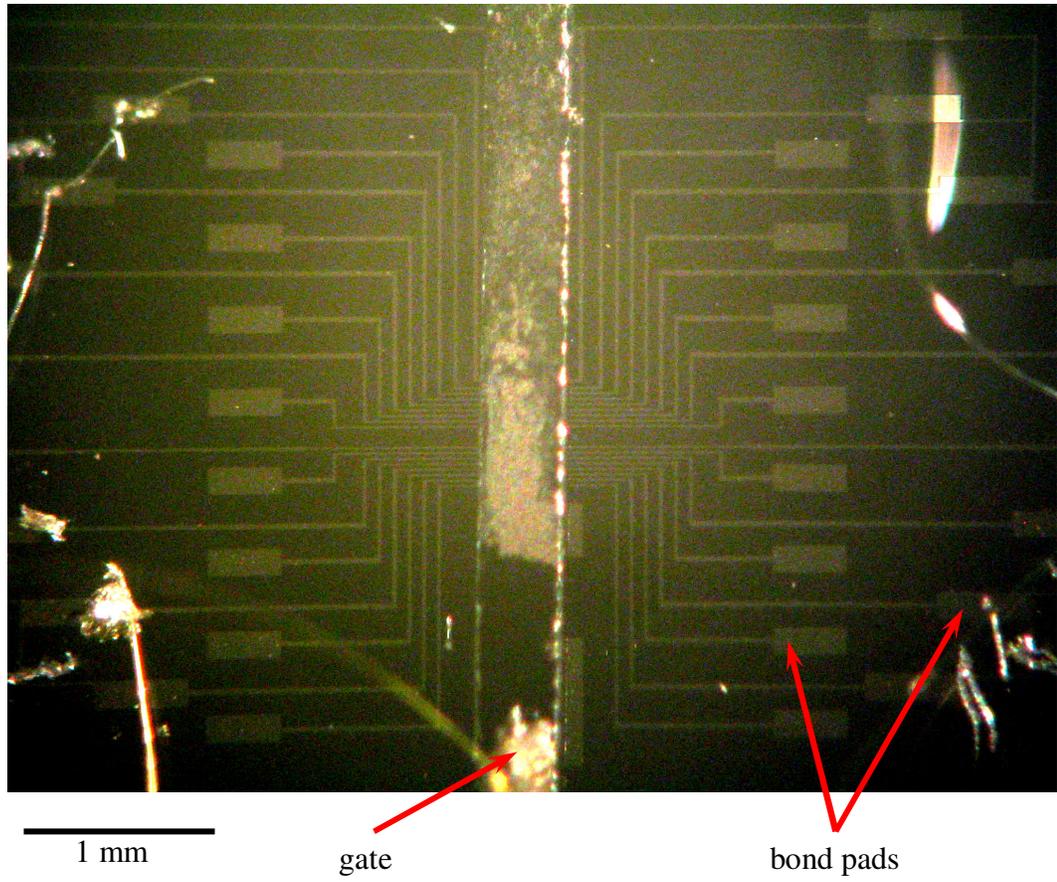


Figure 4.9: Photograph of a typical sample showing the long, rectangular gate and bond pads.

would also check for leakage between the substrate and the SET leads, and between the gate and the substrate. SET resistances at room temperature give a good idea of the quality of the SETs. SETs with too low a resistance ( $< 20 \text{ k}\Omega$ ) will not show good Coulomb blockade characteristics, while SETs with too high a resistance will not give good signal to noise ratio. I aimed to have resistances in the 50-100  $\text{k}\Omega$  range.

The resistances change by a few tens of percent upon cooling to 4.2 K. Also, wire bonding damages the thermal oxide on the surface of the Si wafer, so that the leads are typically shorted with a few 10's of  $\text{k}\Omega$  to the substrate. This means that the resistances I measured at room temperature were not very representative of what I would measure in the dilution refrigerator, but they would at least tell me whether it was worth cooling the sample at all. If the resistance was only a few  $\text{k}\Omega$  I could be sure that the junctions had broken down, and if it was more than a few hundred  $\text{k}\Omega$  I could be reasonably sure that the SETs had blown up completely. If the SETs seemed alive at room temperature I repeated the resistance measurements at 4.2 K in a vacuum dip stick with exchange gas. The dip stick has ten unshielded wires on a ribbon cable and three unfiltered coaxial lines connected to a 14-pin DIP socket. At liquid He temperature the substrate is an insulator for weak electric fields, so the leads of the SETs were no longer shorted by substrate leakage. The resistances were measured with a Fluke 87-III handheld DVM on the  $\text{M}\Omega$  scale. Keeping the DVM in this range ensures that it doesn't source enough current to blow up the  $\text{Al}/\text{AlO}_x/\text{Al}$  junctions.

### 4.3.2 CV measurement

Along with rough resistance measurements I also made rough capacitance-voltage (CV) measurements to characterize the doping in the substrate, both at room temperature and at 4.2 K. Simultaneously with the fabrication of the SETs I made large ( $400 \mu\text{m} \times 400 \mu\text{m}$ ) Al pads on the substrate for this purpose. I wired them to a pin on the DIP header using In solder and Au wire, as with the substrate and gate. Care must be taken during this

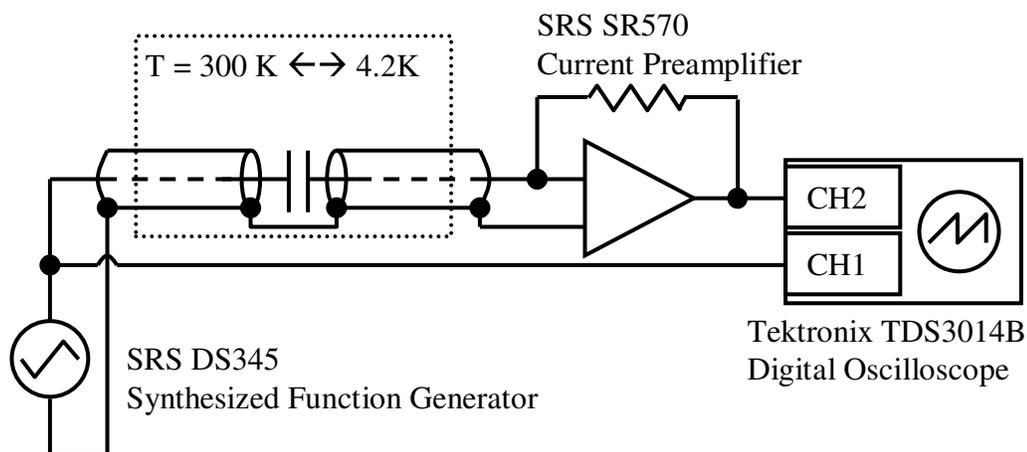


Figure 4.10: Schematic of CV measurement. A triangle wave is applied to the substrate, and the resulting current through the substrate-pad capacitor is measured with a transimpedance amplifier.

soldering not to push too hard on the Al pad, thereby punching through the underlying silicon oxide.

The CV measurements were much easier with the three coaxial cables on the dip stick than with the unshielded lines due to the lower parasitic capacitance. Measurements in the dip stick were made by applying a triangle wave to the substrate and measuring the resulting current to the Al pad with a transimpedance amplifier (see Figure 4.10). The capacitance can be extracted via the relation

$$I = C \frac{dV}{dt} \quad (4.1)$$

where  $I$  is the measured current and  $dV/dt$  is the ramp rate. The data was recorded with a digital oscilloscope and transferred to a computer with a floppy disc. For CV measurements of a sample in the dilution refrigerator the function generator and oscilloscope were replaced with a computer-controlled DAC and ADC, respectively.

### 4.3.3 Measurement of charge motion with SETs

Provided the SETs looked alive and the substrate doping looked reasonable from the CV measurements I would cool the sample to 15 mK in an Oxford Kelvinox 100 dilution refrigerator. Our refrigerator is wired with seven coaxial cables and several twisted pairs. The coaxial cables are filtered with PI filters at the top, heat sunk to a 4.2 K plate, to the 1 K plate, and powder-filtered at the mixing chamber. The twisted pairs are heat sunk at 4.2 K, 1 K, and at the mixing chamber, but they have no powder filters. The seven coaxial cables terminate on a 14-pin DIP socket, as in the 4.2 K dip stick, so that samples are interchangeable between the dip stick and the dilution refrigerator. There is also a red LED in vacuum at the top of the fridge connected to a fiber optic cable that winds down a 4.2 K finger and points directly at the sample. I used this to create electron-hole pairs in the Si via illumination.

I made a sequence of basic measurements to characterize the SETs before launching into more complicated measurements of charge motion. I would sweep the drain-source voltage for each SET and record the resulting current. This gives a reasonable estimate of the charging energy of the SET and therefore of the optimal  $V_{ds}$  to apply for maximum charge sensitivity. Then I would fix  $V_{ds}$  and sweep the voltage on the gate to get a measure of the gate-island capacitance for each SET. The  $1 e$  period using this gate could be as high as 50 V or more, so it was necessary to use a high voltage amplifier: I use an RHK HVA-2000 which allows input voltages of  $\pm 10$  V and has a gain of 45.[86] I would then sweep the substrate potential to get a measure of the (voltage-dependent) substrate-island capacitance.

Measurements of smaller signals required a more sophisticated technique. SETs are extremely sensitive charge detectors, but they are also highly non-linear and need to be biased properly for maximum charge sensitivity. For example, if the voltage on the gate was set to place the operating point directly on top of one of the Coulomb blockade

peaks, where the slope is flat, the charge sensitivity would be zero! On the other hand, to search for charge motion in the substrate requires application of at least several hundred mV to the substrate itself. With my SETs the  $1 e$  period with respect to the substrate potential was  $\sim 100$  mV, so that sweeping the substrate over a range of several hundred mV constantly changes the operating point of the SET. My solution was to use a feedback circuit, acting on the gate above the sample, to maintain a constant  $I_{ds}$ , therefore keeping the charge sensitivity of the SET constant.

Another complication was that, because the SETs are such sensitive detectors of charge, they are sensitive not only to the signals we wanted to measure but also to every other charge moving in the vicinity of the island. Much of the observed charge motion is random in time or moves only slowly in response to an externally applied field, but we are only interested in the charges that move rapidly in applied fields. By applying an ac dither to the substrate and looking for changes in the current through the SET at the dither frequency we could isolate the interesting charges. The dither frequency was chosen low enough to be within the bandwidth of our current preamplifier but high enough that it was outside the bandwidth of the feedback response. Therefore the response of the feedback circuit gives a measure of the quasi-dc changes in charge near the SET while the signal at the dither frequency measures only fast-moving charges. A schematic showing this measurement configuration is given in Figure 4.11.



chapterData and analysis In this chapter I will describe my experiments in more detail, and I will present the data and results from some of those experiments. All of the measurements were made below 100 mK in a 1 T magnetic field to maintain the SETs in the normal state, unless specified otherwise.

#### 4.4 Traditional design: quasi-dc measurements

My first efforts to measure single donor ionization used a much simpler design and geometry than the one described in Chapters 3 and 4. Rather than using the wide leads of the later design, I used a more traditional SET design where the Al leads consisted of lines as narrow as the island itself,  $< 100$  nm wide, the substrate had no doping to create a back gate, and an Al surface gate near the SET island, the “local” gate, was used to apply fields to the donors. A wire suspended above the sample, the “remote” gate, was used to bias the SET onto the steepest part of the Coulomb blockade peak for maximum charge sensitivity. Figure 4.12 shows a picture of a typical SET of this type. The samples were fabricated starting with high-resistivity ( $> 10$  k $\Omega$ -cm) Si on which I grew 200 Å thermal oxide. The wafer was then sent to Core systems for a P implant at 35 keV. The implant was annealed at 850°C in N<sub>2</sub> for 30 min. to activate the donors and at 450°C in forming gas to passivate the Si/SiO<sub>2</sub> interface. I used standard photolithography with negative resist to define an array of Au/Pt/Ti bond pads and leads using a liftoff process, followed by electron beam lithography and double-angle evaporation to create the SETs. Unlike my later design, this design incorporated different metals in contact with each other where the Al layer came in contact with the Au/Pt/Ti, and I found it impossible to anneal these junctions at 450°C without intermetallic reactions. Therefore I was unable to do a surface passivation anneal in forming gas after lithography. As it is possible that the e-beam lithography creates defects at the interface, this explains why I chose to move to an all Al process in my later design as described in Chapter 4. I have included in Tables 4.1 and

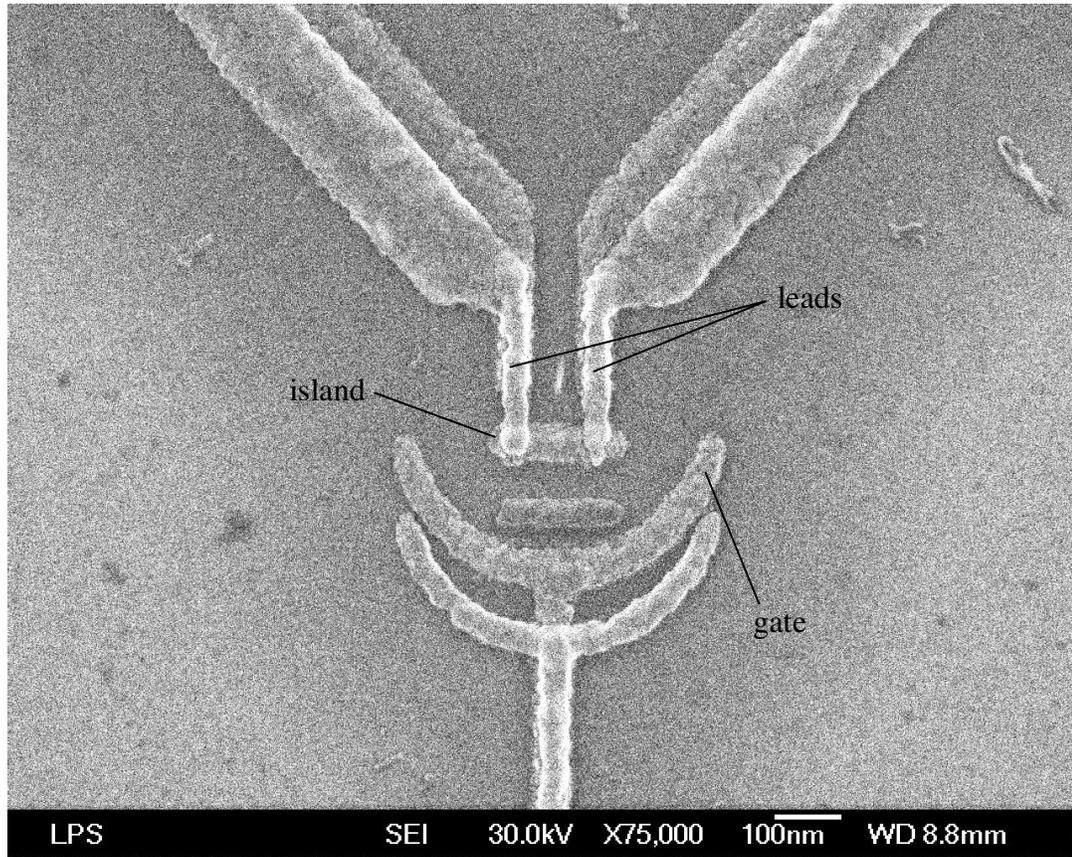


Figure 4.12: SEM micrograph of my early SET design showing Al leads, island, and side gate. All the features have slightly offset identical copies due to the double-angle evaporation.

4.2 a synopsis of the samples I will discuss in this chapter, including the type of SET on each substrate (traditional or wide-lead/back gate) and the P donor density.

To look for gross charge motion involving large numbers of electrons in the substrate I performed quasi-dc measurements on these samples. Starting with the local gate grounded, I swept it to negative voltages, generating fields in the substrate up to  $\sim 100$  kV/cm. Simultaneously I had a feedback circuit (described in Section 4.3.3) connected to the remote gate, trying to keep a constant drain-source current through the SET. If we assume that the remote gate has very little effect on charge motion within the substrate, (a bad assumption as it later turned out) then the response of the feedback loop tells

name of substrate	type of SET	P donor density (atoms/cm <sup>2</sup> )
#1	traditional/side gate	0
#2	traditional/side gate	10 <sup>11</sup>
#3	traditional/side gate	10 <sup>12</sup>
#4	wide-lead/back gate	10 <sup>12</sup> or 0 depending on location
#5	wide-lead/back gate	10 <sup>11</sup> or 0 depending on location

Table 4.1: Substrates discussed in this chapter. For individual devices on a given substrate see Table 4.2.

name of device	type of SET	P donor density (atoms/cm <sup>2</sup> )
SET1-1-9	traditional/side gate	0
SET4-2-2	wide-lead/back gate	0
SET4-2-7	wide-lead/back gate	10 <sup>12</sup>
SET5-1-5	wide-lead/back gate	10 <sup>11</sup>
SET5-1-8	wide-lead/back gate	10 <sup>11</sup>
SET5-2-5	wide-lead/back gate	0
SET5-2-6	wide-lead/back gate	0

Table 4.2: SET devices discussed in this chapter. The first number in the SET name refers to the substrate it was on; the second to what column of the SET array it was in; the third to the row, counting from the bottom.

us directly about that charge motion. More specifically, if there were no charge motion in the substrate then for every change  $V$  on the local gate there should be a corresponding change  $-V \frac{C_{\text{local}}}{C_{\text{remote}}}$  on the remote gate, where  $C_{\text{local}}$  and  $C_{\text{remote}}$  are the capacitance between the SET island and the local and remote gates, respectively. Deviations from this linear behavior are an indication that additional charges beyond the usual polarization of Si are moving near the SET island.  $C_{\text{local}}$  and  $C_{\text{remote}}$  can be determined by the Coulomb blockade peak spacing near zero potential if we assume that there is no charge motion in this regime.

Unfortunately the true situation was not quite so simple because the range of the remote gate was restricted for two reasons. First, to keep the SET operating on the same Coulomb blockade peak while sweeping the local gate by 1 V (the approximate voltage needed to ionize donors in this geometry) would have required application of a few kV to the remote gate. This was impossible because our setup only gave me a few hundred V to work with. Furthermore, although we anticipated that the remote gate would have only a small influence on the charges within the sample, it nevertheless seemed a good idea to minimize its influence as much as possible by restricting its range. I accomplished this by “resetting” the feedback circuit by several  $e$  when the remote gate voltage reached extremal values within a predetermined range. As I have shown schematically in Figure 4.13, what I mean by this is that I would have the feedback circuit pick a new operating point, equivalent to the previous operating point in the sense that each corresponded to the same drain-source current, but at a lower voltage. This was only possible because the drain-source current of an ideal SET is periodic in the gate potentials. When the feedback loop was operated this way the resulting record of the remote gate potential was a sawtooth instead of a simple line, but the line could be reconstructed by splicing together the teeth of the sawtooth. However, let me stress that the equivalence of this spliced dataset with a dataset that would have been acquired without any feedback resets is founded on the (now known to be wrong) assumption that the remote gate has only

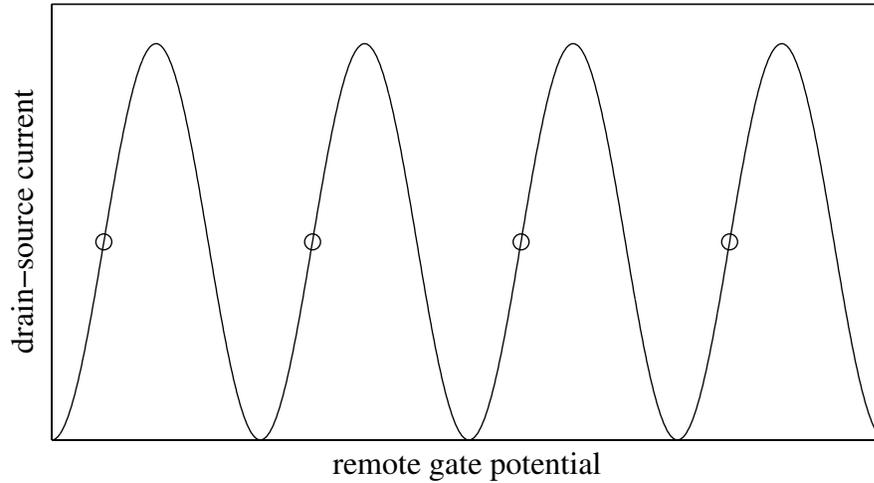


Figure 4.13: Simulated Coulomb blockade peaks as a function of remote gate potential. Four equivalent operating points for the feedback loop, spaced by  $1 e$ , are marked with circles. The feedback loop can be moved between these points without changing any of its parameters.

small effect on substrate charge motion.

I followed this procedure for several SETs on a substrate without any intentional doping (substrate #1) as well as on substrates doped with P at the  $10^{11}/\text{cm}^2$  and  $10^{12}/\text{cm}^2$  levels (substrates #2 and #3 respectively.) For example, Figure 4.14 shows Coulomb blockade peaks from SET1-1-9 on substrate #1. The local gate capacitance is  $6.21 \pm 0.04$  aF, obtained from a least squares fit to the peak spacing. Figure 4.15 shows two quasi-dc datasets from this SET obtained by sweeping the local gate in opposite directions and recording the feedback response on the remote gate. I have subtracted a linear background from the data as described on page 82, so that the data points represent additional charge induced on the SET island beyond that expected from a simple capacitive model. There are several interesting features. Starting at  $V = 0$  and moving to more negative potentials we see that there is almost no charge moving near the SET island until about  $-0.5$  V. This is partly by design of course, because it was precisely this portion of the data to which I fit a line in order to subtract a linear background. Beyond  $-0.5$  V the

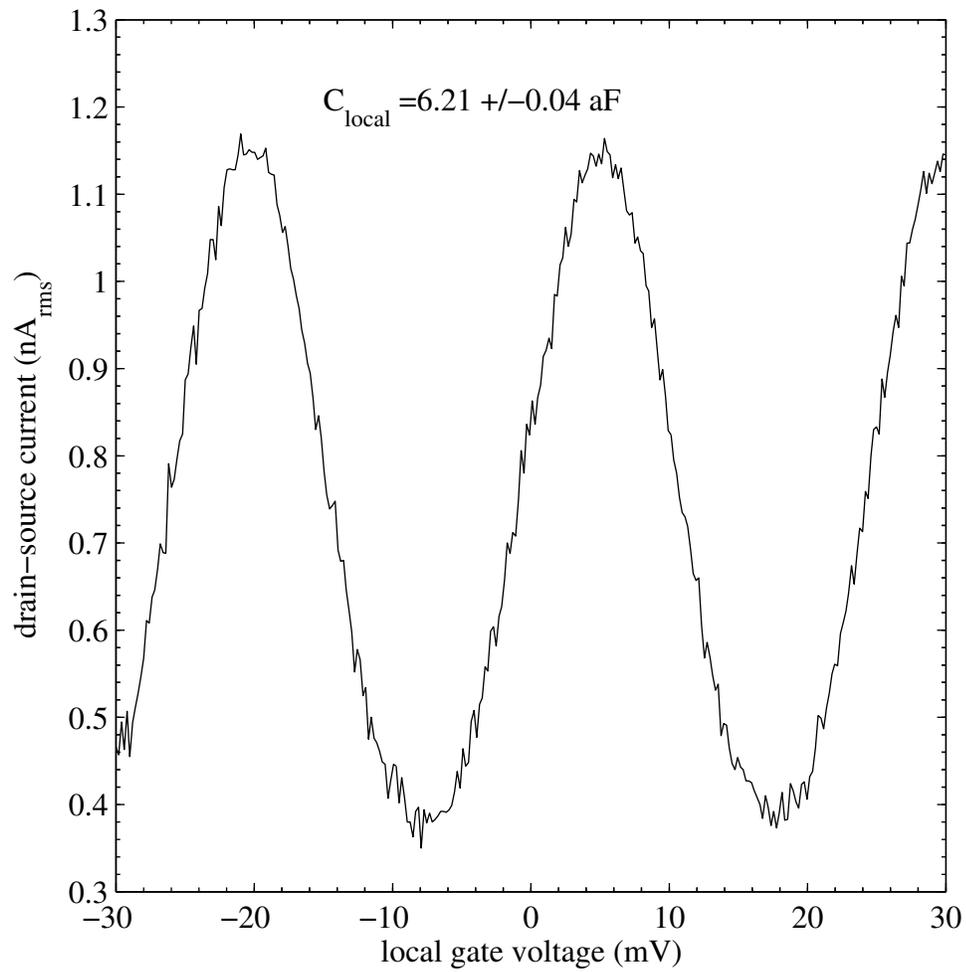


Figure 4.14: Coulomb blockade peaks near zero voltage for an SET on substrate #1 without any intentional doping.

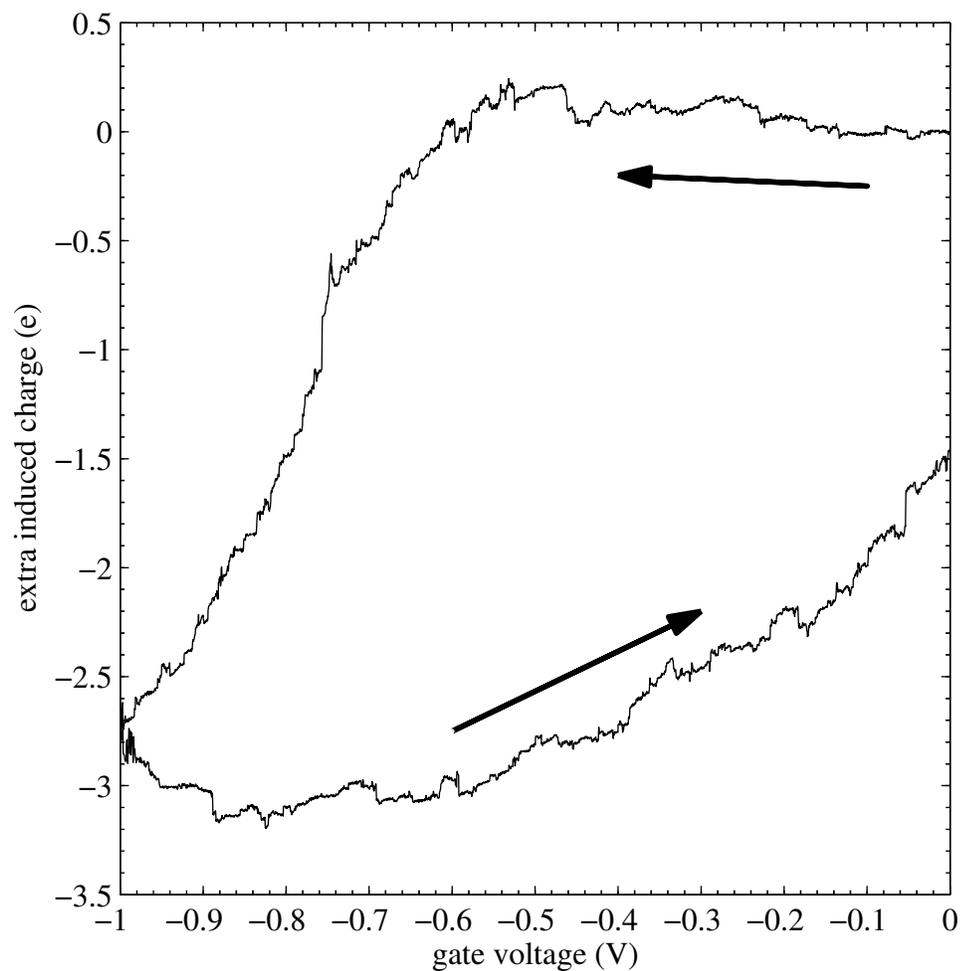


Figure 4.15: Charge motion near an SET on substrate #1 without any intentional doping as a function of local gate potential. The actual sawtooth waveform that was recorded has been spliced together to obtain a nearly linear dataset. For this plot, the slope of the linear dataset was then determined near zero potential and subtracted from the entire dataset. What remains represents charges induced on the SET island beyond what is expected simply from linear polarization of the dielectrics. The y axis has been normalized by the remote gate capacitance to units of 1 e.

data acquire a different slope, so that by the time the local gate reaches -1.0 V there are an extra 2.7 e on the island. Reversing the direction of the sweep the data become almost flat again, but the initial trend is downward. This was my first hint of really time-dependent behavior in these samples, because a downward trend is a continuation of the trend from the first sweep direction. Furthermore, when the voltage has returned to ground there is still an induced charge of 1.5 e; the two datasets do not form a closed loop. This means that even though the gate voltage has returned to its initial value, some charges that were moving in the substrate have not returned to their initial locations.

I suspected that this hysteretic behavior was time dependent and did a simple test experiment. I initialized the sample by fixing the local gate voltage at -1 V for 5 min. Then I abruptly changed the potential to 0 V and recorded the time response of the remote gate feedback loop while keeping the local gate fixed. I did a similar experiment in the other direction, starting at 0 V and moving to -1 V. The results are plotted in Figure 4.16. The voltage step induces a clear relaxation of charges within the sample that lasts for hundreds of seconds. As there were very few donor or acceptor impurities in this substrate, nominally  $< 10^{12} /\text{cm}^3$ , it is probable that this charge motion is associated with defects at the Si/SiO<sub>2</sub> interface, rather than with charges inside the Si itself.

I took quasi-dc data sets under nearly identical conditions as above for SETs on substrates #2 and #3 between 0 V and -1 V. I have plotted some results from substrate #3 in Figure 4.17, superimposed on the results from the intrinsic substrate. The quasi-dc behavior of substrate #2 was very similar to the intrinsic substrate, so I haven't plotted it here. Following the red curve to the left we see that there is little charge motion until the local gate reaches -0.1 V. This voltage corresponds to an electric field of  $\sim 5$  kV/cm, which should be plenty strong to ionize donors farther than 100 nm from the island; it is not surprising to see charge motion begin at this voltage. By the time the local gate reaches -1.0 V this SET has an extra induced island charge of almost 25 e, and the charge has returned to 0 e when the gate voltage returns to 0 V. While this is encouraging, there

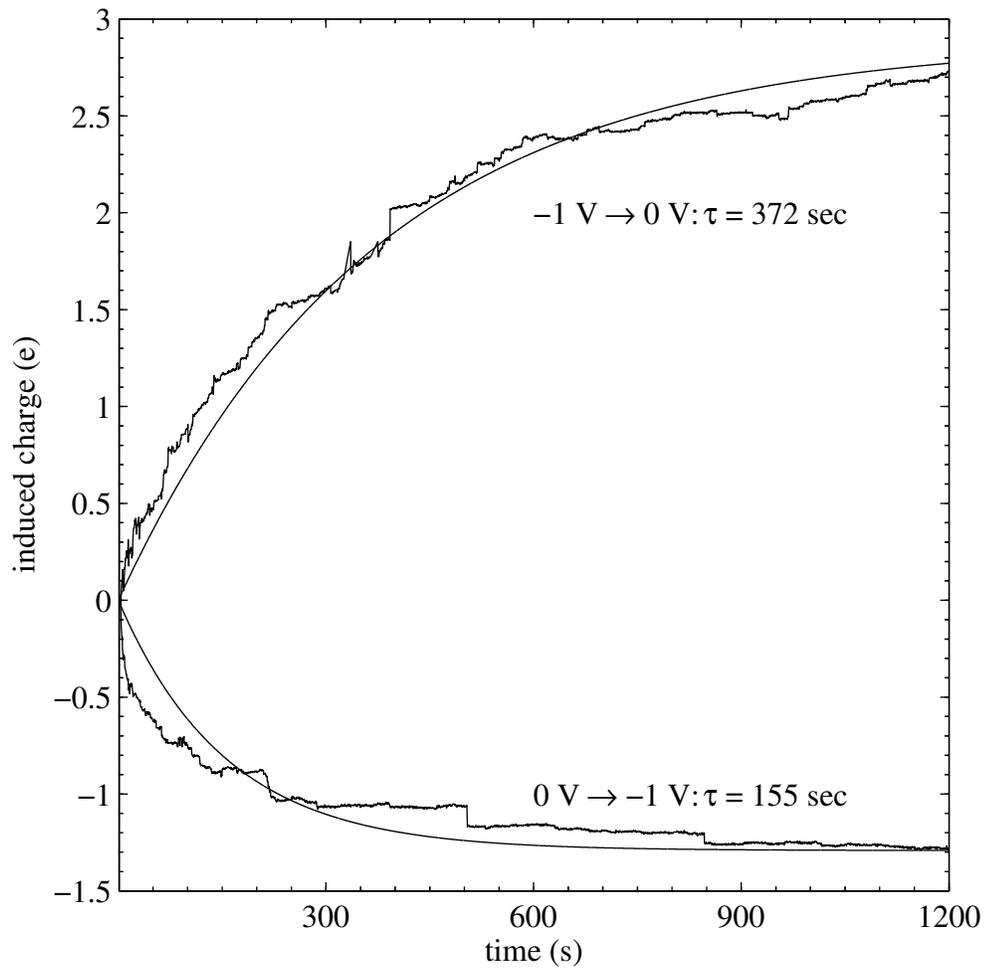


Figure 4.16: Time dependent charge relaxation near an SET on undoped substrate #1 after a step change on the local gate. Charges do not move instantly after a change in voltage, but instead relax back with a time constant of a few hundred seconds. The smooth curve is a least-squares fit of the data to an exponential decay.

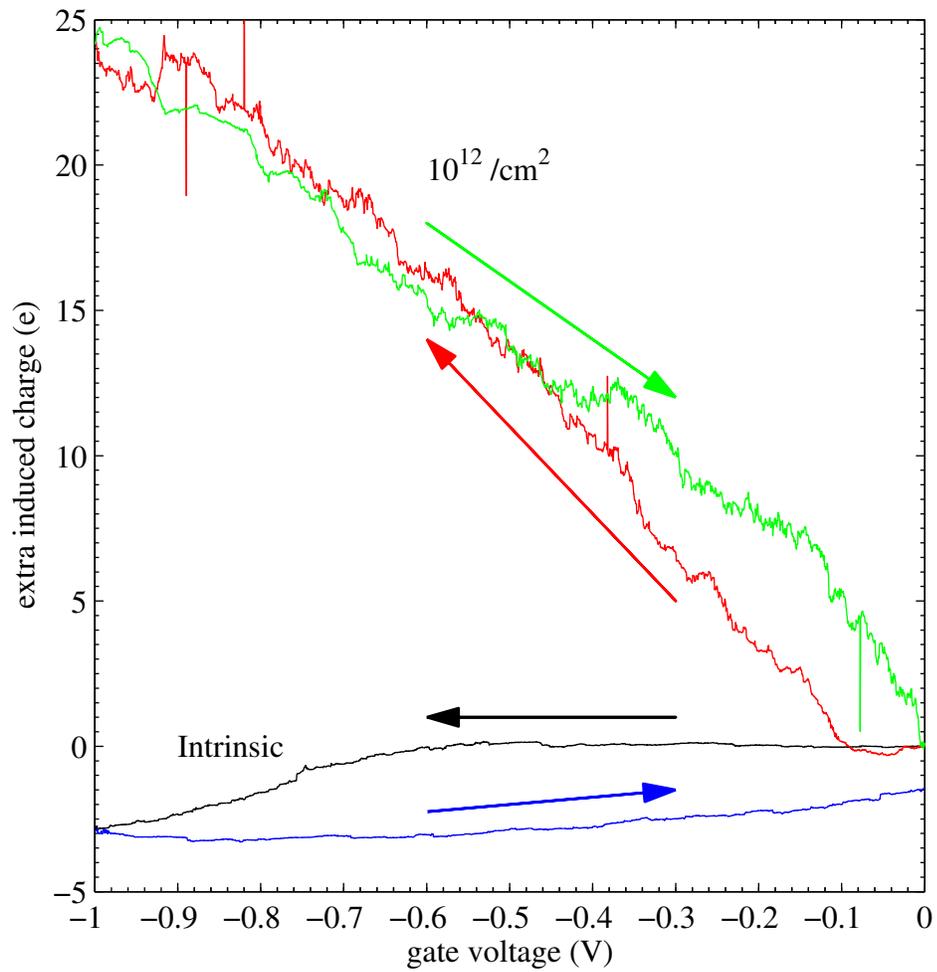


Figure 4.17: Quasi-dc charge motion near two SETs, one on nominally intrinsic substrate #1, the other on substrate #3 implanted with P at  $10^{12} /\text{cm}^2$ . The arrows give the direction of the voltage sweep.

is a real problem in the analysis of the data from this substrate (#3): the slope of the feedback voltage as a function of local gate potential was never really constant, unlike the way it was on the intrinsic substrate (#1). If you compare the two data sets you see that the data from the intrinsic substrate (#1) is quite a bit flatter and quieter than the data from the  $10^{12}$  /cm<sup>2</sup> (#3) sample. Because I determine the “extra” induced island charge by subtracting a linear characteristic from the data, whose slope is determined by the behavior at low gate voltage, it is essential to have some region where the slope is relatively constant, and that was not the case with this implanted sample. Therefore I am very suspicious of the quantitative accuracy of these results.

Furthermore, it was becoming clear during the course of these experiments that the effect of the remote gate potential on charge motion in the substrate was far from negligible, as I had assumed initially. For one thing, the slope of the feedback response would often change discontinuously when the feedback loop reset to a different Coulomb blockade peak, and this could only happen if some charges were being affected both by the local gate and by the remote gate. But as I will describe next, I had even more convincing quantitative evidence that the remote gate was affecting charge motion in the substrate.

## 4.5 Traditional design: lock-in measurements

From Section 3.1.3 we know that the charges I am interested in observing, electrons moving between donor sites and the Si/SiO<sub>2</sub> interface, should make the transition on a ns timescale, much faster than the timescale for relaxation that I was seeing in these experiments. The slowly moving charges must have been coming from something else, either from (undesired) impurity electrons moving much farther away than just to the nearby interface, and therefore requiring a longer time to come back, or from electrons slowly moving between other states such as defects associated with the silicon oxide. In

an attempt to isolate only the fast moving charges I tried a new experiment using a lock-in technique described in further detail in Section 4.3.3. Briefly, I used the same feedback circuit on the remote gate as I had used in the quasi-dc experiments to maintain a constant drain-source current through the SET while sweeping the local gate. But simultaneously I applied a small (several mV) dither at 200 Hz to the local gate. The idea was that when the dc field approached that value which brought the donor into resonance with the interface state, the electron would be forced to tunnel back and forth between donor and interface in phase with the ac field, which would yield an enhanced signal in the SET at the dither frequency. In these early experiments I also applied a cancellation signal to the remote gate, 180° out of phase with the ac field, to null the response of the SET when there was no charge motion.

The most interesting measurements of this type came from substrate #2, doped at  $10^{11}$  /cm<sup>2</sup>, although I obtained similar results with all three substrates. In Figure 4.18 I have plotted the SET response to a dither at 200 Hz for gate voltage sweeps in opposite directions. For this SET I obtained a charge sensitivity of  $1.6 \times 10^{-4} e/\sqrt{\text{Hz}}$  at 200 Hz, and the time constant for the data in Figure 4.18 was about 1 ms (I didn't record the actual value). This gives an integrated noise of 2.5 me, which value agrees well with the 1.8 me RMS noise of the data. The two resonant peaks have amplitudes of 10.3 me and 16.2 me, clearly distinguishable above the background noise. What is striking about the two data sets is how closely the red one retraces the blue. I found that this was not always the case, and the main problem turned out to be the remote gate feedback loop.

From Section 3.2.1 I know that the position of a resonant peak in the space of local gate voltage may be shifted by voltages on the remote gate according to Equation 3.41. At the time the data in Figure 4.18 were taken, I had not yet done the calculation leading to Equation 3.41, and was acting instead on the assumption that the remote gate would have little effect on donors in the substrate. To test this assumption I changed the operating point of the feedback loop by 1 e increments (so that the drain-source current would

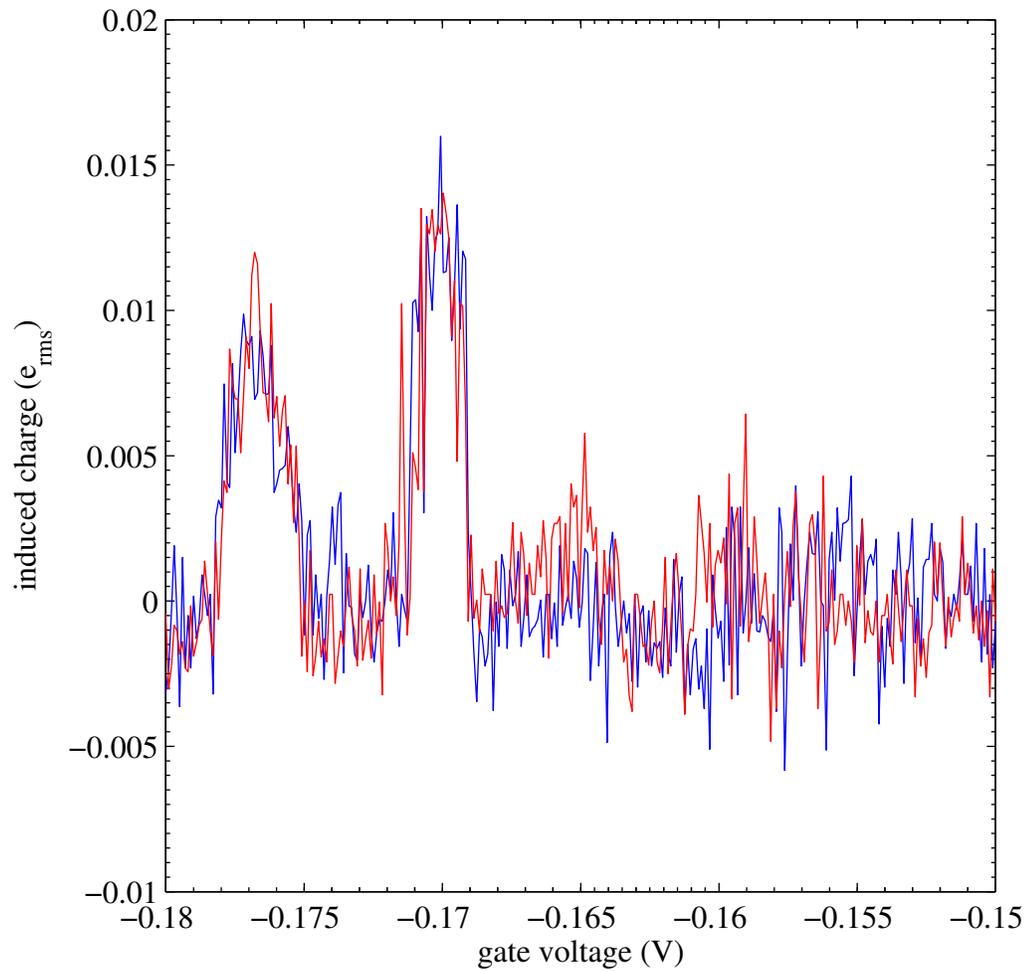


Figure 4.18: Driven charge motion at 200 Hz near an SET on substrate #2 doped with P at  $10^{11} / \text{cm}^2$ . Red and blue datasets correspond to different directions for the dc voltage sweep.

not change) and retook the data each time. Contrary to my initial hypothesis it became obvious that the remote gate had a huge effect on these two resonant fluctuators. In Figure 4.19 I have plotted the position of each fluctuator as a function of both the local and remote gate potentials. The slopes of these two lines are  $(2.3 \pm 0.1) \times 10^{-4}$  and  $(3.3 \pm 0.1) \times 10^{-4}$ . In terms of Equation 3.33, these slopes are equal to  $-\alpha$ . The local and remote gate capacitances for this SET were  $16.62 \pm 0.06$  aF and  $8.56 \pm 0.06$  zF, respectively. Therefore the shielding of these two fluctuators (given by Equation 3.43) is  $q/Q^0 \approx -0.3$  and  $q/Q^0 \approx -0.4$ . The desired situation with  $|q/Q^0| \ll 1$  is clearly not achieved. More intriguing is the sign of the slopes - a positive slope means a negative  $\alpha$ , but this means that the local and remote gates counteract each other, driving a given fluctuator in opposite directions! It is difficult to envision where these fluctuators must reside; the only area where the field from the local gate is directed opposite to the field from the remote gate is near the local gate itself, but this is not a location where we would expect charge motion to give measurable signals in the SET. Furthermore, I saw similar distributions of fluctuators at all three substrate doping levels, so that it is difficult to ascribe them to donors. One possibility is that these two fluctuators resided on the “phantom” island seen in Figure 4.12, between the gate and the SET island, although this is pure speculation.

## 4.6 Macroscopic capacitors: CV measurements

The preceding results pushed us to design a new single electron transistor and gate geometry. In particular it became clear that we needed to rethink the shielding of donors from the feedback gate if we wanted to minimize its effect on them, and simultaneously we needed to design a geometry whose field configuration would be simple to model if we wanted to localize where our signals were coming from. The phantom island was worrisome because it represented a floating potential, so we wanted to fix its voltage

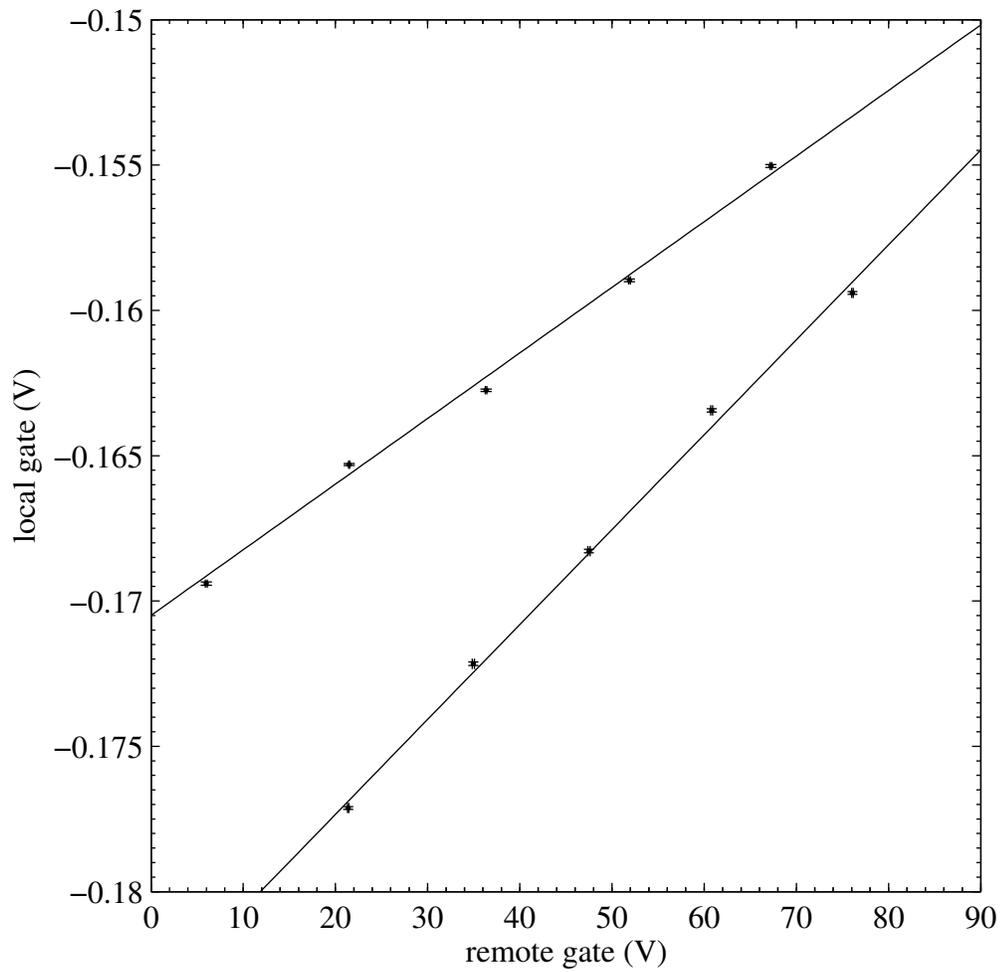


Figure 4.19: Effect of the remote gate on the local gate switching voltage for the two fluctuators in Figure 4.18. The data agree well with a linear model, although I have perhaps underestimated the errors on the data points.

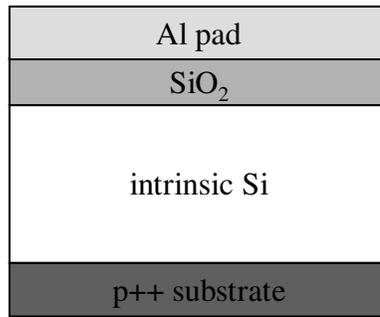


Figure 4.20: Diagram of an MOS capacitor consisting of a p<sup>++</sup>-doped Si substrate (the back gate), a nearly intrinsic n-doped Si region above that, an SiO<sub>2</sub> dielectric, and an Al pad on the surface.

somehow. And we realized that the ability to tune the Fermi level in the substrate would be a tremendous advantage, as it would allow us to selectively populate or empty the donors. The fruit of this rethinking was the design I discussed in Chapters 3 and 4 with very wide leads and a doped substrate for a back gate. As an added benefit this geometry allows a nearly direct comparison with results from a macroscopic (several hundred  $\mu\text{m}$  dimension) capacitor.

Capacitance-voltage (CV) measurements of semiconductor structures are tremendously useful because they are easy to make yet provide much of the information, such as dopant distribution, that we would otherwise have gotten only through more difficult SET measurements. CV measurement is a standard technique for characterizing semiconductor devices, including metal-oxide-semiconductor (MOS) structures, and is abundantly described in the literature, so I won't give many of the details here.[87] However, I will give a brief outline of what I was looking for. Consider a capacitor, diagrammed in Figure 4.20, consisting of a p<sup>++</sup>-doped Si substrate (the back gate), a nearly intrinsic n-doped Si region above that, an SiO<sub>2</sub> dielectric, and an Al pad on the surface. If we apply a large negative potential to the substrate, an electric field will build up between the Al pad and the p<sup>++</sup> contact. The field will be directed toward the substrate, so that no holes will

escape the p++ Si and move into the intrinsic region. The capacitance we measure will be the series combination of the oxide dielectric and the intrinsic Si dielectric (assumed nearly empty of carriers.) If we now increase the voltage on the p++ contact far enough the situation will reverse, so that the field becomes directed away from the substrate. If the voltage is increased further still there will come a time when holes are emitted from the contact into the valence band of the intrinsic region. They will flow under the influence of the applied field to the Si/SiO<sub>2</sub> interface, effectively shorting the p++ contact to that interface. In this situation we will measure a different capacitance than before, the capacitance of the oxide dielectric alone. If we then start decreasing the substrate voltage we will measure the oxide capacitance until all of the holes have been depleted from the interface, at which point we will measure the series intrinsic/oxide capacitance as before. Measuring these two capacitances gives us the thickness of the oxide and of the intrinsic regions, assuming we know the area of the Al pad.

I made just this sort of structure by implanting B at 500 keV through the front side of an intrinsic Si wafer with a density of  $2.5 \times 10^{14} / \text{cm}^2$ , as described in Chapter 4. On the surface I grew  $272 \pm 10 \text{ \AA}$  of oxide, which results in a dopant distribution like the one plotted in Figure 4.3, and I evaporated 400  $\mu\text{m}$  Al square pads. I measured the capacitance at 4.2 K (no magnetic field) by sweeping the voltage on one of the pads and measuring the current which flowed in and out of the substrate. This current is directly proportional to the capacitance, and the results are plotted in Figure 4.21. The blue curve shows a sweep starting with positive potential on the substrate and therefore with holes occupying the Si/SiO<sub>2</sub> interface. As the voltage is decreased holes flow from the interface to the substrate, and the measured capacitance is  $187 \pm 2 \text{ pF}$ . From this I calculate an oxide dielectric constant  $\epsilon = 3.6 \pm 0.2$ , which agrees reasonably with the accepted value of 3.9. (The error here is dominated by the error on the Al pad area which was written with e-beam lithography and not well calibrated.) At 2.8 V the interface has been depleted of holes and the capacitance begins to drop; it continues to drop as the depletion region

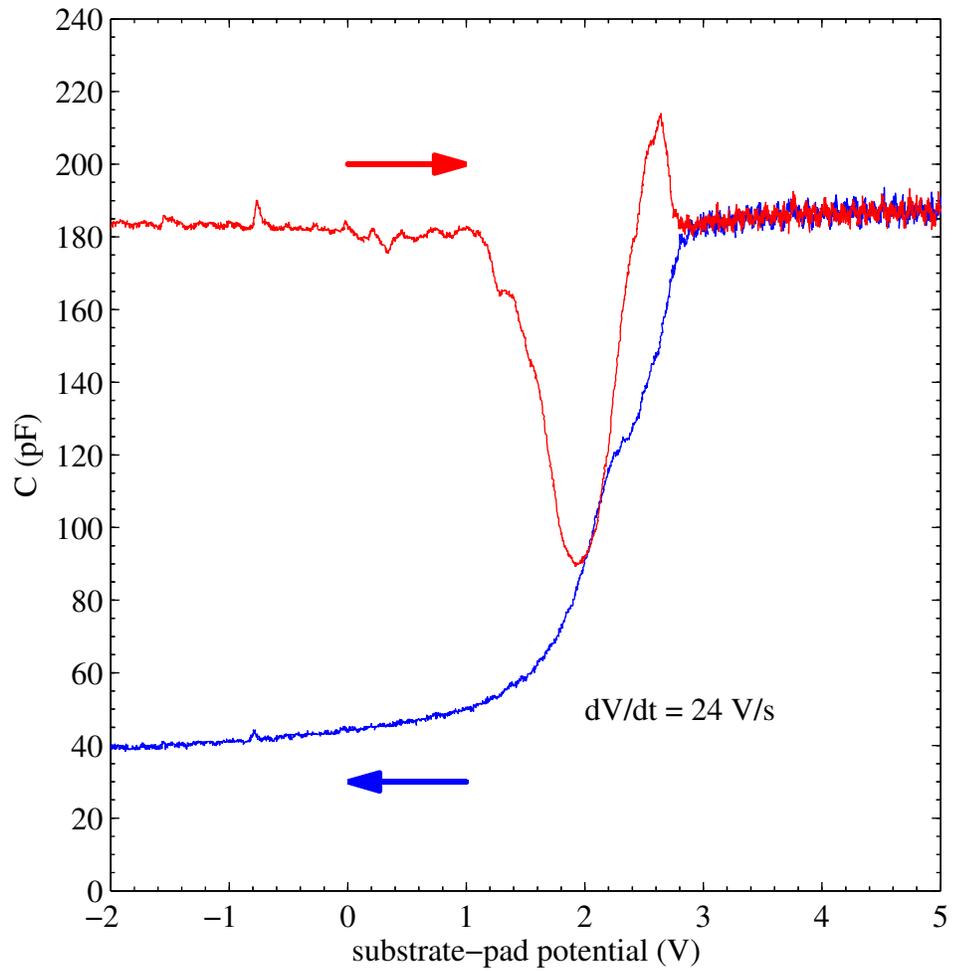


Figure 4.21: Capacitance at 4.2 K of an MOS structure fabricated via ion implantation, thermal oxidation, and metal evaporation. The data were acquired in two different sweep directions as marked with arrows.

between the surface and the p++ contact widens.

From this data I can estimate the doping density of the B implant as a function of depth as follows. Ignore the oxide capacitance for the moment and treat the intrinsic Si region as a parallel plate capacitor with capacitance  $C$ . Then the depletion depth is given by

$$d = \frac{\epsilon A}{C}, \quad (4.2)$$

where  $A$  is the pad area. Similarly the doping density at depth  $d$  above is given by

$$n(d) = \frac{2}{e_0 \epsilon A^2 \frac{d(1/C^2)}{dV}}, \quad (4.3)$$

where  $e_0$  is the charge of an electron. I can subtract out the oxide series capacitance from the CV data to get the capacitance appropriate for Equation 4.2 and thereby calculate the depletion depth as a function of voltage. The results are given in Figure 4.22. Notice that the depletion depth initially grows very quickly with voltage as the potential is decreased below 3 V, because there are fewer impurities to deplete near the surface, but that the rate of depletion slows down as it extends into more highly doped regions. What is perhaps surprising is that, even with a few volts applied, the substrate is only depleted to a depth of 350 nm. Considering that the acceptors were implanted to a depth of 1  $\mu\text{m}$ , I can conclude that I am only depleting a small fraction of them at these voltages, and that furthermore I have not nearly depleted the surface to a depth where the doping becomes metallic ( $3.5 \times 10^{18} / \text{cm}^3$  - see Figure 4.3). The noise on the data in Figure 4.21 makes it difficult to extract a smooth curve for  $n(d)$ , but I can at least get some approximate values. Note that the calculation of  $d(1/C^2)/dV$  in Equation 4.3 must consider the voltage drop across the semiconductor only, not the total voltage drop across semiconductor and oxide. Between 100 nm and 200 nm below the surface the acceptor density is about  $1.5 \times 10^{16} / \text{cm}^3$ , and

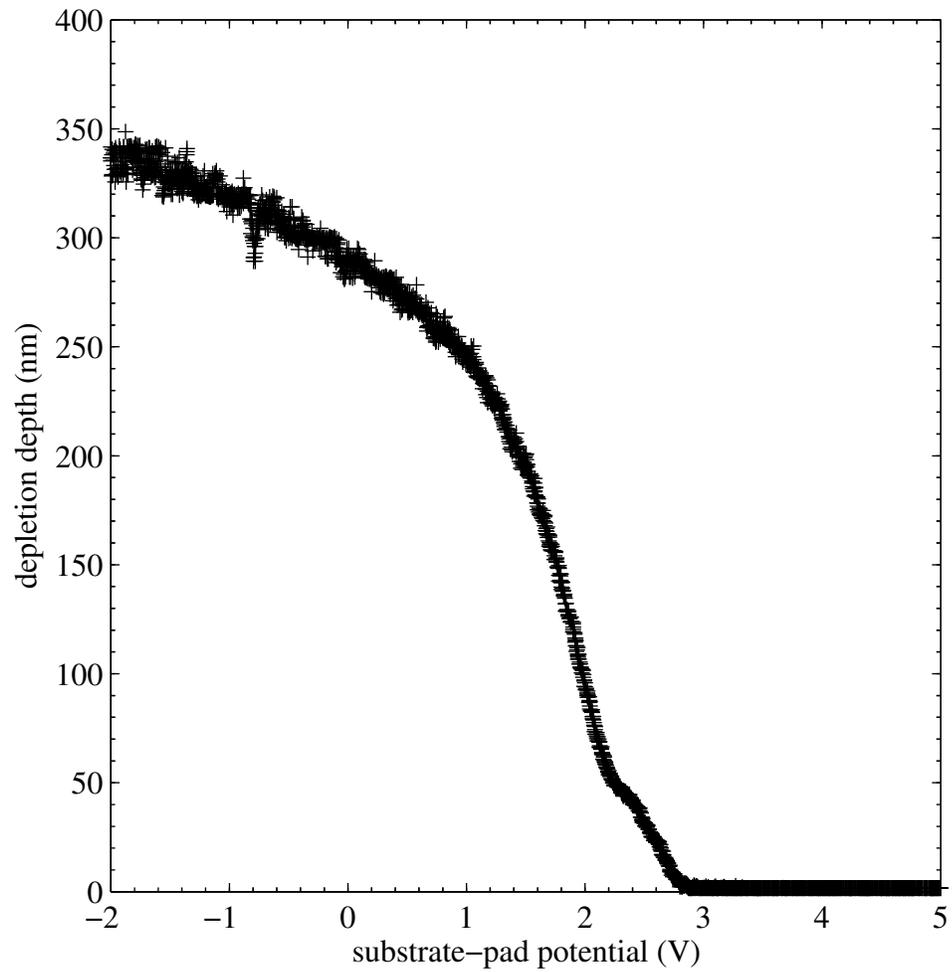


Figure 4.22: Measured depletion depth of a MOS capacitor on a p++-implanted substrate as a function of voltage.

between 200 nm and 350 nm it rises to  $6.5 \times 10^{16} /\text{cm}^3$ . Comparing these values with those obtained via SIMS in Figure 4.3 (about  $10^{16} /\text{cm}^3$  between 100 nm and 200 nm and rising to  $5 \times 10^{16} /\text{cm}^3$  by 350 nm) we see relatively good agreement. This means that, even though the long tail of acceptors that exists up to the surface is below metallic doping concentration, nevertheless these impurities are still ionized at moderately large potentials and contribute to the electric field distribution. They cannot be ignored, as I had originally hoped.

Another important number that we can extract from this data is the electric field at the interface. As I showed in Section 3.1.3, the critical field for ionization of a donor 30 nm below the interface is  $\approx 20$  kV/cm. We can calculate the electric field as a function of applied voltage from the CV data to see how large a voltage is necessary for donor ionization. The field is given by

$$\mathbf{E} = \frac{Q}{\epsilon_{Si}A} \quad (4.4)$$

$$= \frac{\int C dV}{\epsilon_{Si}A}. \quad (4.5)$$

The one subtlety in applying Equation 4.5 lies in the choice of where to start integrating the charge  $Q$ . The integration should start at the “flat-band” voltage, i.e. the voltage for which there is no electric field in the Si. We can reasonably say that the flat-band voltage occurs when the capacitance begins to fall dramatically from its oxide value, which in this case occurs at 2.8 V; this fall in capacitance means that all of the holes have been depleted from the interface, so that they must be experiencing a field there. The electric field resulting from this analysis is plotted in Figure 4.23.

The red curve in Figure 4.21 shows a sweep in the opposite direction starting from a different initial condition; namely I had applied a large enough negative potential to the substrate that electrons, through some unknown mechanism, were created and accumulated at the interface. Note that I was also able to create electrons in these experiments

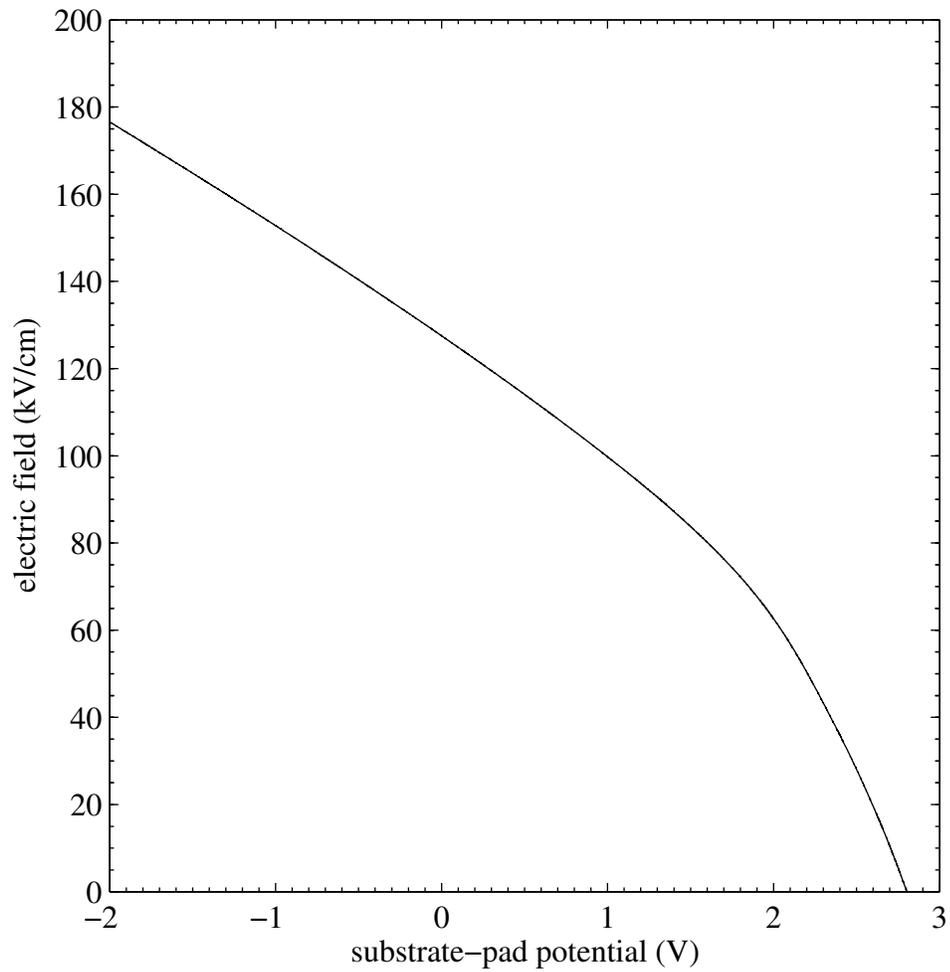


Figure 4.23: Electric field at the Si/SiO<sub>2</sub> interface of a MOS capacitor on a p<sup>++</sup>-implanted substrate as a function of voltage.

by applying a negative potential and illuminating the substrate. It is the depletion of these electrons from the interface upon increasing the substrate potential that again gives us the oxide capacitance in Figure 4.21,  $183 \pm 2$  pF, because they effectively short the interface to the substrate as the holes did before. Presumably as the electrons leave the interface and move into the substrate they will populate any unoccupied donors. Conversely, by applying a large positive potential to the substrate we flood the surface with holes, which will empty any occupied donors. This then was my scheme for filling and emptying the donors we would study.

#### 4.7 Wide lead SETs: CV measurements

As I discussed in Section 3.2, an SET with wide leads separated by only a narrow gap and gated by a wide planar gate beneath it has approximately the same electrostatic configuration as a parallel plate capacitor. To test this idea and to look for possible signatures of individual donors I fabricated wide lead SETs on two substrates, #4 and #5. Each substrate had a planar back gate created via ion implantation of B; they were subsequently implanted through a mask with P at  $10^{12}$  /cm<sup>2</sup> and  $10^{11}$  /cm<sup>2</sup>, respectively, to create selectively n-doped regions for study. In Figure 4.24 I have plotted two different but related data sets from substrate #4. The blue curve is CV data acquired as before from a macroscopic ( $400 \mu\text{m} \times 400 \mu\text{m}$ ) capacitor. The red data is “CV” data acquired from an SET, and the data sets were acquired *simultaneously*. Both the capacitor and the SET were fabricated over areas of the substrate that had not been implanted with P. What I mean by CV data in the case of the SET is the following: if we sweep the voltage on the substrate without applying any counteracting potential to the remote gate of the SET, the drain-source current of the SET modulates. Each time the current crosses some threshold in the upward direction corresponds to another electron moving onto the SET island. By recording these voltages I get island charge as a function of substrate potential,

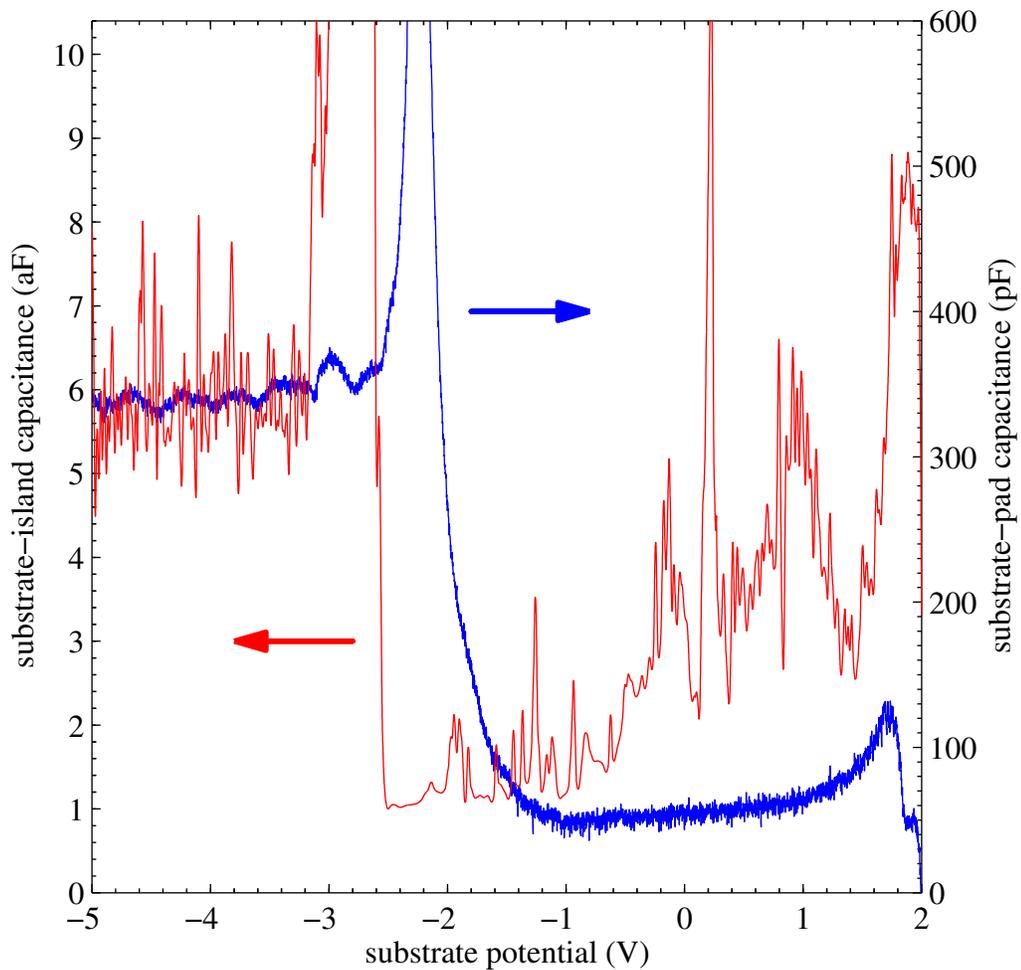


Figure 4.24: CV of a macroscopic capacitor compared with CV of an SET as obtained by counting the individual electrons moving onto the island. I have intentionally forced the two CV curves to coincide toward the left side of the figure in order to show their correspondence more closely.

and by definition the derivative of this charge gives the substrate-island capacitance. This derivative is what is plotted in Figure 4.24.

I have intentionally forced the two CV curves to coincide toward the left side of the figure in order to show their correspondence more closely. The data show the same broad features that we saw before in Figure 4.21, with a larger oxide capacitance on the left side of the graph and a smaller depletion capacitance to the right. A complicating factor in the understanding of this data is that it was impossible, due to some leakage currents with this sample, to sweep the substrate potential much beyond 2 V. Therefore, although we see a rise in capacitance on the right hand side of the graph, the voltage never really reaches a value where we might see strong accumulation of holes at the interface. On the other hand, at negative potentials, where there was no leakage problem, there is still an unknown mechanism that creates electrons at the surface, and this is where the oxide capacitance is evident. From the ratio of the two oxide capacitances (338 pF/5.88 aF) and the area of the macroscopic capacitor, I estimate that the area of the SET island in contact with the substrate is  $2.78 \times 10^{-15} \text{ m}^2$ , or about  $50 \text{ nm} \times 50 \text{ nm}$ . Comparing this result with the SEM image of a representative sample in Figure 4.8 we see very good agreement. Furthermore, the ratio of oxide to depletion capacitance, or in simpler terms how much the capacitance changes from its maximum to its minimum values, is in reasonable agreement between the two devices. However, the capacitance as measured by the SET is clearly noisier, especially in the depletion region between -2.5 V and 1.6 V, probably because it is more sensitive to locally moving charges.

## 4.8 Wide lead SETs: gating

In the previous section I showed how the gross behavior of a single electron transistor on a doped Si substrate can be explained with a capacitance-voltage model no different from the model used to understand much larger devices. However, this model assumes

that charge is a continuous quantity, not a discrete one, and the goal of these experiments was to look for evidence of individual charge motion in a doped Si substrate. I saw hints of the sensitivity of the SET to discrete charges in the large but non-uniform noise on the data in Figure 4.24. As was the case with my earlier SET design, to investigate these signals further I wanted to use a lock-in technique to single out those charges which moved reproducibly between two states. And this required that I have another gate, in addition to the doped substrate back gate, to bias the SET onto its points of maximum sensitivity. The wide leads and back gate of this new design provided such good shielding for the island from side gates that it proved impossible to use a surface gate similar to the one in Figure 4.12: I found that I needed to apply more than 10 V to such a gate 1.8  $\mu\text{m}$  away from the SET to induce even a single extra electron on the SET island, and voltages above about 10 V can be lethal to the oxide on the Si surface. A back-of-the-envelope calculation of the expected 1 e period given this 1.8  $\mu\text{m}$  separation, an island area of 150 nm  $\times$  50 nm, and assuming all the field lines go through the vacuum dielectric gives about 4 V, in order of magnitude agreement with the measured value.

To circumvent this problem I tried a different idea entirely, using as a gate a piece of metallic-doped Si suspended above the sample by 25  $\mu\text{m}$  Kapton spacers at either end; further details of its fabrication were described in Section 4.2.4. Si was chosen instead of a simple metal in order to match the thermal contraction with the substrate. Even though this 25  $\mu\text{m}$  spacing is much larger than 1.8  $\mu\text{m}$ , the breakdown voltage of the Kapton is high enough that I can apply a sufficient potential to gate several extra electrons onto the SET island without damaging the underlying substrate. Figure 4.25 shows some Coulomb blockade oscillations taken using a gate of this type. The measured gate capacitance is  $2.51 \pm 0.03$  zF, compared with a parallel plate capacitor estimate of 2.7 zF (again assuming an island area of 150 nm  $\times$  50 nm.) This close agreement means that I understand the electrostatics of the new design well, and that most of the field lines really are excluded from the substrate near the SET island. I will refer to this gate simply

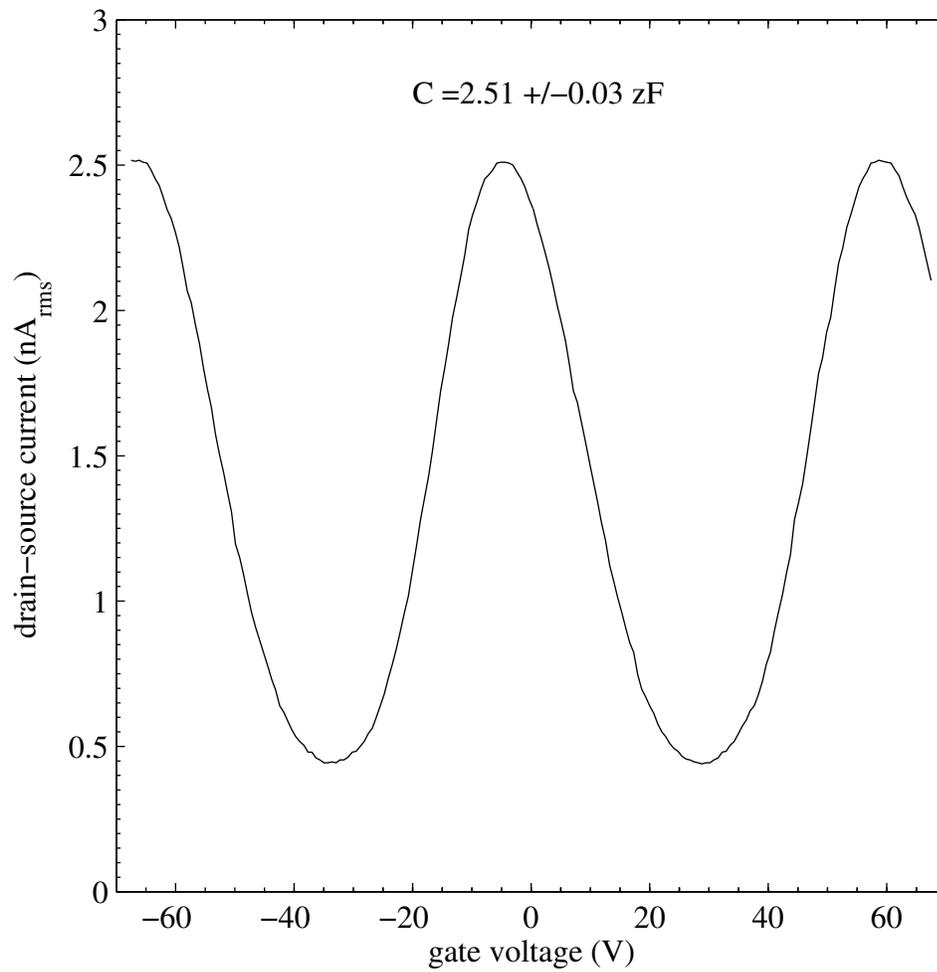


Figure 4.25: Coulomb blockade peaks of a wide lead SET obtained by sweeping the potential on a conducting plane  $25 \mu\text{m}$  above the substrate.

as the “gate”, while I will refer to the substrate back gate as the “substrate”.

## 4.9 Effects of donor doping

Now that I was armed with a feedback circuit acting on the gate to bias the SET for maximum charge sensitivity, I was able to look for resonances in the response to a sinusoidal ac dither as in Section 4.5, and I found several. I suspected that these resonances were coming from the motion of individual donor electrons, so I expected to observe an order of magnitude more of them in substrate #4 than in substrate #5, while I expected to observe only a very small number for the SETs over those areas of the substrate that had not been implanted with P. Moreover, to show that the resonances were coming from donors instead of acceptors I thought that I would be able to make them disappear by flooding the substrate with holes, thereby emptying the donors of their electrons.

I made measurements of two SETs on substrate #4, one above an area that had been implanted with P at  $10^{12}$  /cm<sup>2</sup> and which I call SET4-2-7, and one above an area that had not been implanted, SET4-2-2. For both SETs I swept the dc potential on the substrate from 1 V to -1 V and measured the response to a 1 kHz, 9 mV<sub>rms</sub> ac dither. I took data starting from two initial conditions, one for which I put 3.5 V on the substrate to flood it with holes and one for which I put -5.0 V to flood it with electrons. The qualitatively striking results are plotted in Figures 4.26 and 4.27. With each plot I have included the RMS deviation of the data about their mean. The arrows indicate points where the feedback circuit shifted from one Coulomb blockade peak to another, as explained in Section 4.4. It seems clear from visually comparing Figures 4.26 and 4.27 that the P doping has an observable effect on the response of the SET, and the numbers bear this out: the RMS deviation of the data from the SET on the undoped region of the substrate is less than half the RMS deviation of the SET over the doped region. Furthermore, it also seems that flooding the substrate with holes instead of electrons serves to eliminate some of this

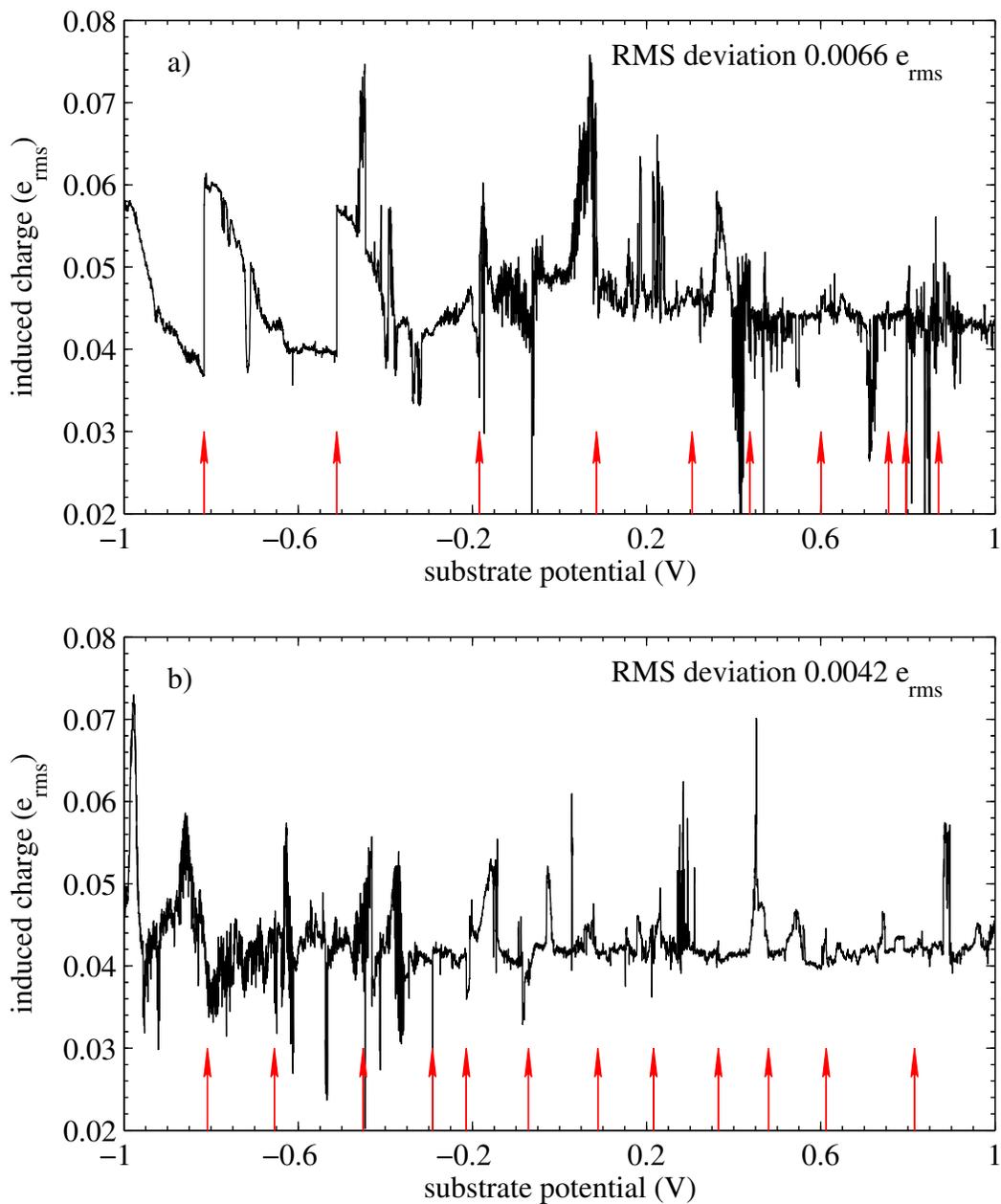


Figure 4.26: Response of SET4-2-7, fabricated on a Si substrate implanted with P at  $10^{12}/\text{cm}^2$ , to an ac dither on the substrate, as a function of dc substrate potential. a) After flooding the substrate with electrons. b) After flooding the substrate with holes. The sweeps were from positive to negative dc potential. The arrows correspond to points where the feedback circuit moved to a different Coulomb blockade peak.

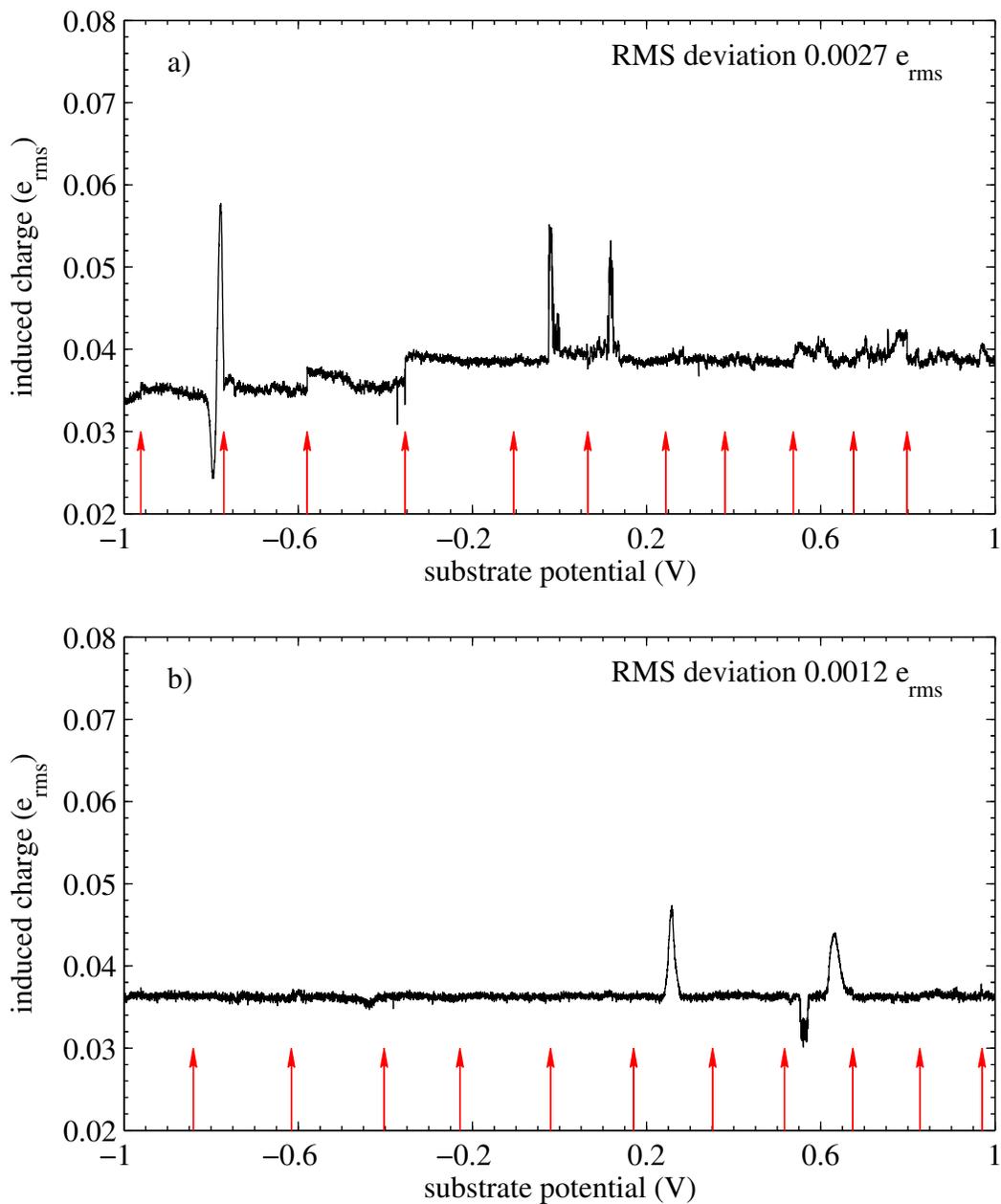


Figure 4.27: Response of SET4-2-2, fabricated on a Si substrate without P implant, to an ac dither on the substrate, as a function of dc substrate potential. a) After flooding the substrate with electrons. b) After flooding the substrate with holes. The sweeps were from positive to negative dc potential. The arrows correspond to points where the feedback circuit moved to a different Coulomb blockade peak.

activity, although here the data aren't as conclusive. While there are three clear resonant peaks in Figure 4.27b that probably correspond to a single charge moving between two different locations, identifying such isolated peaks in the other data sets is more difficult. I suspect that, in the case of the SET over the doped region, the doping density was so high that what we are actually seeing is the collective motion of many electrons between many locations rather than the motion of single electrons between isolated locations.

Furthermore, there is an observable effect that large changes in gate voltage, marked by arrows in the figures, have on the behavior of the SET, but this effect is more pronounced in the case that the sample has been flooded with electrons instead of holes. Consider for example the large changes in SET response near -0.8 V and -0.5 V in Figure 4.26a. It looks as if decreasing the substrate potential is more strongly coupling the substrate to the SET until the feedback resets at these points, when the response returns to its former value. Perhaps there is a 2D electron system forming just at the Si/SiO<sub>2</sub> surface which is being modulated by the gate. Similar behavior is observed in Figure 4.27a, but not in Figures 4.26b and 4.27b. This new geometry, then, did not completely solve the problem of isolating the substrate near the island from perturbations of the gate, but perhaps this reflects my lack of understanding of the charge configuration in the substrate. As I will discuss in the next section, I made more extensive measurements of the effects that the gate had on substrate #5.

#### 4.10 Characterizing the observed charge fluctuators

Substrate #5 was implanted with P at  $10^{11}$  /cm<sup>2</sup>, and my hope therefore was to observe more isolated resonances than we see in Figure 4.27a yet not the truly noisy and chaotic behavior seen in Figure 4.26a; this would have confirmed that the resonances were coming from donors. Unfortunately this was not observed; I could not really see any difference between the SETs on the implanted and non-implanted regions of substrate #5.

I did, however, observe charge fluctuators or resonances in all four SETs that I measured on this substrate, just like the resonances I had observed in previous samples. And I found that with care it was possible to track the positions of these resonances in substrate voltage as a function of gate voltage and of charge density at the Si/SiO<sub>2</sub> interface. This gave me a wealth of information about their positions in physical space.

It became clear from all the experiments I have described so far that observing one of the resonances in a reproducible way was not as simple as returning the substrate potential to where I had observed it before. I now knew that the gate above the sample was having an effect on the substrate under the SET island, even though the SET geometry had been designed to minimize this. I also noticed that where a resonance appeared actually depended somewhat on the starting voltage of the sweep, and this was not something I had expected. Therefore I concluded that if I wanted to observe a particular resonance after changing the substrate potential or gate potential by some reasonably large amount I would need to meticulously create the same initial conditions. I wrote a Labview VI to do just that as follows:

1. Set the substrate potential at some negative potential, say -2.0 V, to establish an electric field pointing away from the Si/SiO<sub>2</sub> interface.
2. Illuminate the sample with a red LED to create electron-hole pairs. The holes flow into the substrate contact and disappear, but the electrons accumulate at the interface until no electric field remains within the Si substrate. In addition, any donors and acceptors become occupied.
3. Return the substrate potential to some voltage greater than -2.0 V. This removes some of the electrons from the interface, and for a large enough potential even forces holes to the interface instead. It also sets the initial condition for the sweep.
4. Sweep the dc substrate voltage back to -2.0 V while recording the ac response with a lock-in. Observe some resonances in the response.
5. Repeat this entire process again, starting the sweep from some slightly higher po-

tential in step #3. Observe how the position of each resonance shifts due to this change in initial voltage.

Using this procedure gave me the ability, for the first time, to monitor a given resonance over a period of hours or even days; before then there had been too many unknown variables. And I certainly observed some interesting behavior. Figures 4.28 and 4.29 show four data sets of this type, each for a different SET on substrate #5. While there is certainly some rich structure in these data sets, just a moment's reflection leads inevitably, for several reasons, to the conclusion that the resonances observed there are not due to donors in the substrate. Firstly, there is not a much greater number of these resonances in the two SETs that were fabricated above implanted areas than in the SETs without an implant. In fact, a doping density of  $10^{11}$  /cm<sup>2</sup> corresponds to only 2.5 donors on average beneath a 50 nm × 50 nm SET island, and we observe more resonances than this in all the SETs, including the SETs without an intentional donor implant. The second reason is a bit more complicated, and has to do with the initial conditions. As I mentioned in step #2 above, each data sweep was initialized with the substrate being illuminated by a red LED while its potential was set to -2.0 V, creating a 2D electron system at the Si/SiO<sub>2</sub> interface whose charge density was  $\approx 2 \times 10^{12}$  /cm<sup>2</sup>. Then the voltage was returned to -0.5 V or higher to remove some of those electrons, but I know from other measurements that the electrons at the interface were not fully depleted until about 0.2 V. This means that there was in fact still a conducting sheet at the Si/SiO<sub>2</sub> interface until the voltage reached 0.2 V, and such a 2DEG would significantly change the electrostatics of the system. For example, it is impossible that any of the resonances we observe in these data sets could have come from anything in the Si substrate, because the SET island would have been completely screened from any charge motion in the Si substrate by the conducting sheet. This conclusion is supported by the fact that the data get much noisier for voltages above about 0.2 V on the substrate, as the SETs suddenly do become sensitive to charge motion below the interface, a trend which is most evident in the bottom of Figure 4.29.

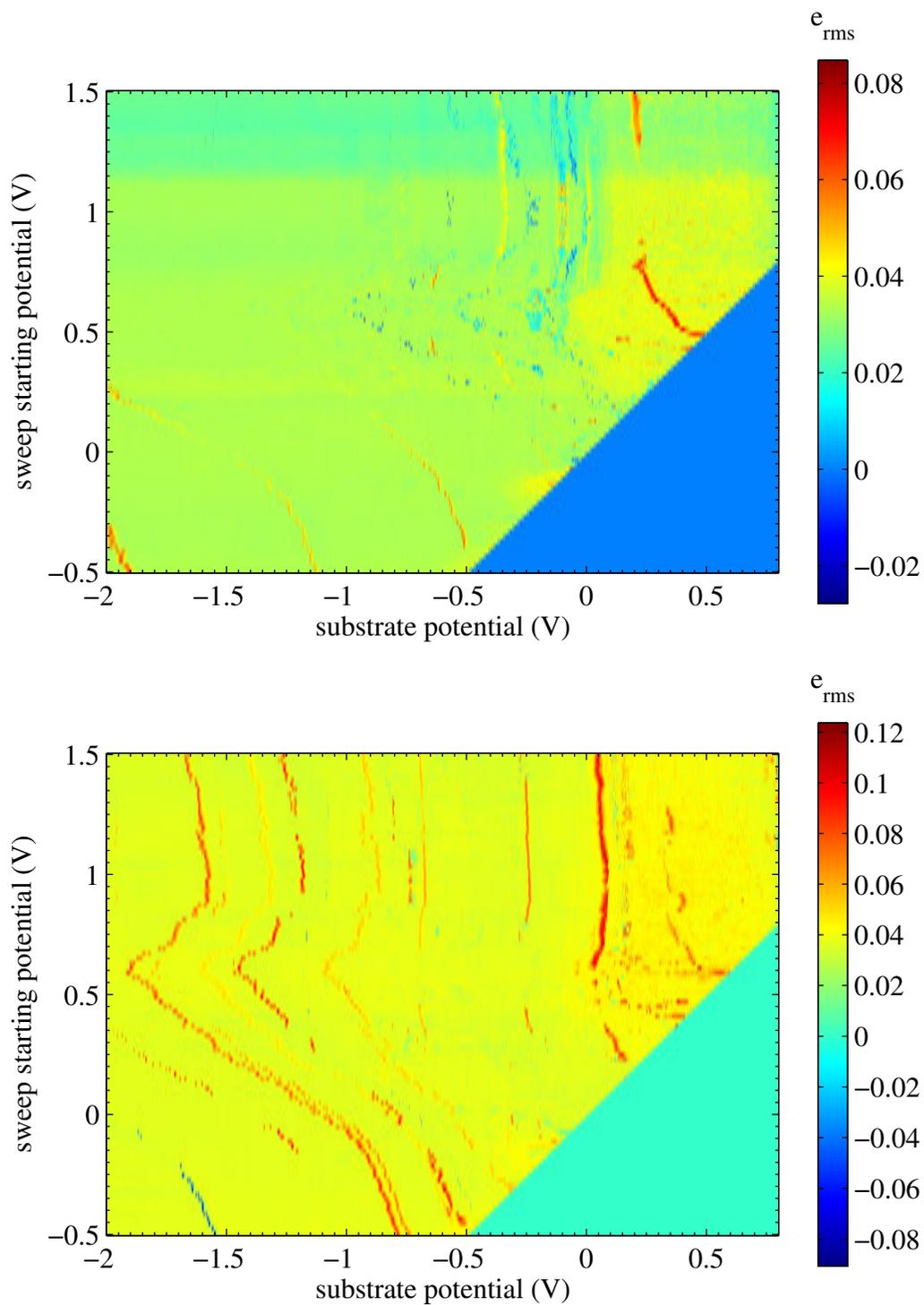


Figure 4.28: Response of two SETs fabricated on a Si substrate implanted with P at  $10^{11}/\text{cm}^2$  to an ac dither on the substrate, as a function of dc substrate potential and starting voltage. Bottom: SET5-1-5. Top: SET5-1-8.

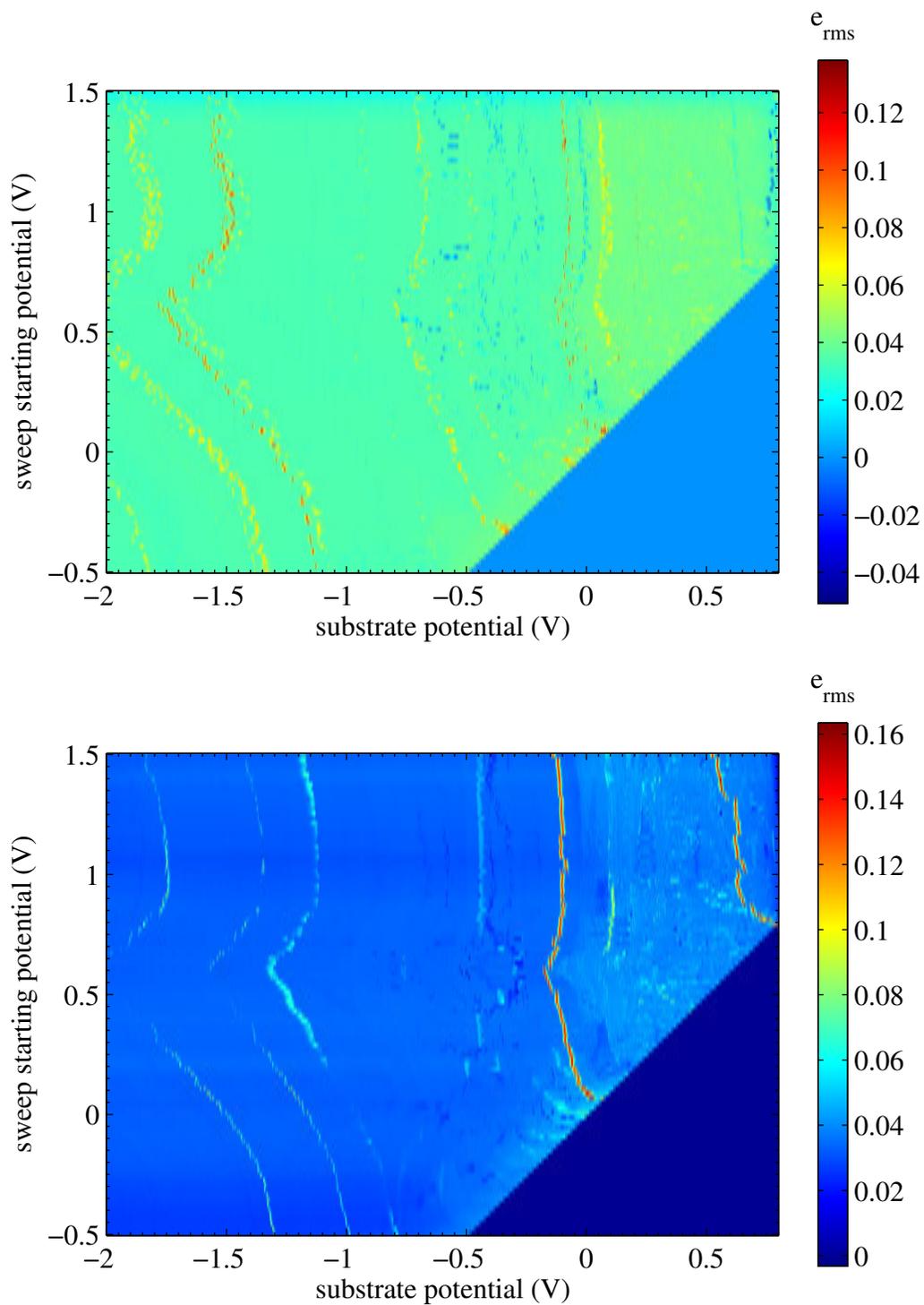


Figure 4.29: Response of two SETs fabricated on a Si substrate not implanted with P to an ac dither on the substrate, as a function of dc substrate potential and starting voltage. Bottom: SET5-2-5. Top: SET5-2-6.

The third reason these resonances could not come from donors has to do with how the positions of the resonances in substrate voltage change as the initial sweep potential is changed. As the initial sweep voltage is increased from -0.5 V to 0.2 V electrons are being removed from the interface and flowing into the substrate contact. This serves to decrease the voltage drop across the oxide while keeping the bands flat within the semiconductor. If there were a resonator within the Si, then, we should expect its position to shift to higher substrate voltages as electrons are removed from the interface, because the electric field in the Si depends only on how much the voltage has changed from flat band, and flat band in the substrate is given by the initial sweep potential provided electrons remain at the interface. On the other hand, if there were a charge fluctuator above or at the Si/SiO<sub>2</sub> interface we should expect its position to shift to more negative potentials, because the removal of electrons from the interface decreases the electric field strength above the interface, so that a more negative potential is required to achieve the same field. This is just the behavior that is observed for all of the resonators, with each SET, up to sweep starting voltages of at least 0.2 V, when the electrons are presumably depleted from the interface. However, in all four data sets there is a kink in the curves near a starting voltage of 0.6 V, when the position of the resonance begins to move back to more positive voltages. This suggests that there is some charge motion within the oxide itself that is affecting the fluctuator!

I did further experiments to investigate the influence of the gate on these resonators. In particular I initialized the sample with the LED and a negative substrate voltage as before; then I applied 1.5 V to the substrate to empty it of electrons, and I took a sweep from -0.5 V to -2.0 V. Then I repeated this process several times, each time changing the range of possible remote gate potentials. The results are plotted in Figure 4.30, which shows four obvious resonators moving in substrate voltage as the gate potential is changed. As in Figure 4.19 (where the axes are reversed from those in Figure 4.30) the ratio of change in substrate voltage to change in gate potential for a given resonator gives  $-\alpha$ , which

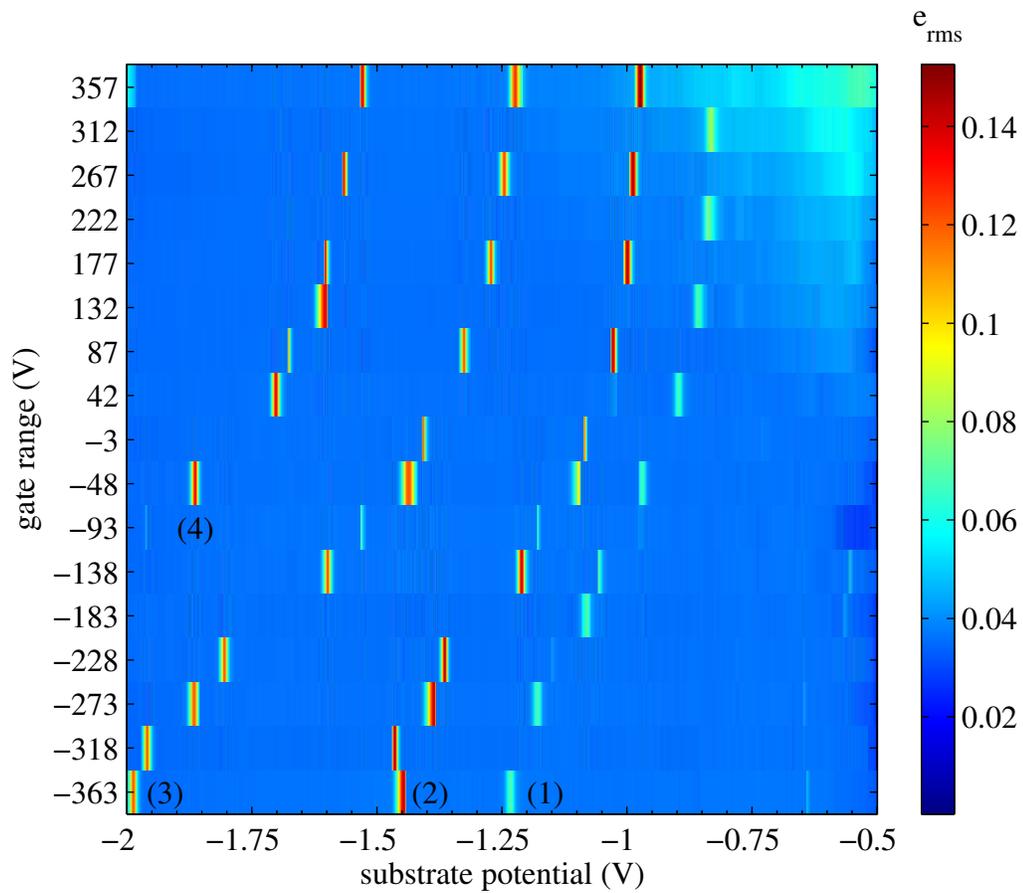


Figure 4.30: Response of SET5-2-5 to an ac dither on the substrate as a function of dc substrate potential and gate voltage. The labels on the y-axis actually represent  $\pm 85$  V ranges of gate potential.

in the case of Figure 4.30 depends on the voltages themselves. As an example I have carefully determined the position of resonator #3 in voltage space and plotted the result in Figure 4.31 along with approximate values of  $\alpha$ ;  $\alpha$  changes by almost an order of magnitude over the 900 V range of gate potentials, from  $-3 \times 10^{-3}$  to  $-4 \times 10^{-4}$ . In Section 3.2.1 I found, by solving Laplace's equation numerically, that for a similar SET geometry  $\alpha = 0.01$ , but that was for the gate and substrate 1  $\mu\text{m}$  above and below the surface. If we scale that result by the true values of 25  $\mu\text{m}$  and 300 nm we obtain a scaled theoretical value  $\alpha = 1.3 \times 10^{-4}$ , certainly smaller than the experimental value for these resonators. The change in  $\alpha$  is more modest for resonators #1, #2, and #4 in Figure 4.30, but still a factor of three or so. Furthermore I note that  $\alpha$  is negative, as it was in the data from my traditional SET design, which means again that the substrate and the gate act on these charge fluctuators in opposite directions. This is not really possible for an electron beneath the Si/SiO<sub>2</sub> interface, where fields from the gate and substrate should be nearly parallel. It seems more likely that the resonators reside in the oxide or at the surface, where it is possible that the two fields would be opposed.

In Figure 4.32 I have plotted the same data as in Figure 4.30 using the actual gate voltages instead of just the gate ranges. The resonators are harder to see in this kind of plot, but it makes some trends evident that aren't present in Figure 4.30. In particular, we can see the dc offset on the feedback loop as it crosses a resonance, compensating for the charge motion associated with that resonance. We can also see that some regions of the plot have a more linear change in gate voltage with changes in substrate potential: the lower left area of the plot is far more linear than the upper right area.

I also wanted to investigate whether the motion of these resonators was discrete or continuous, because we would expect the motion of an electron between a donor site and the interface to be discrete. If an electron were moving discretely in phase with the applied ac potential of frequency  $f$  and amplitude  $A$ , then it would induce a square wave response in the SET with the same frequency  $f$  but with a fixed amplitude independent

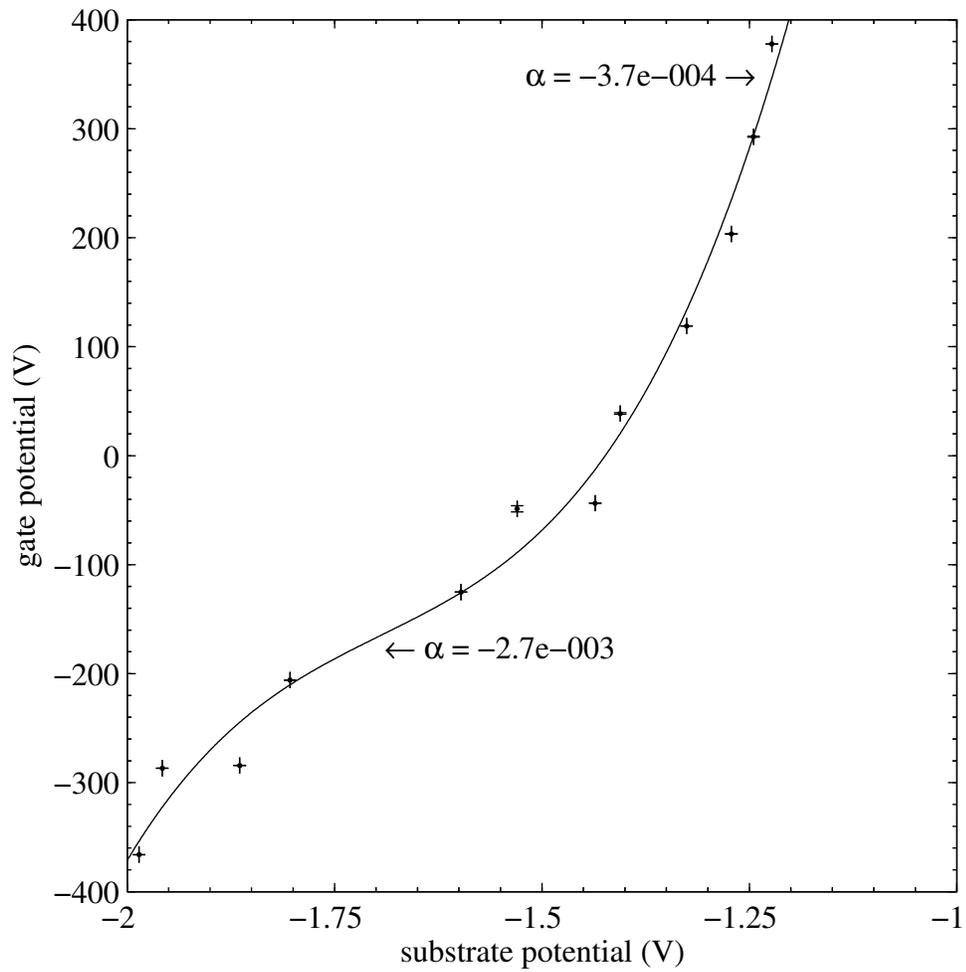


Figure 4.31: Effect of the gate on the substrate switching voltage for resonator #3 from Figure 4.30. The line is a polynomial fit to guide the eye and to provide very approximate values of  $\alpha$  only.

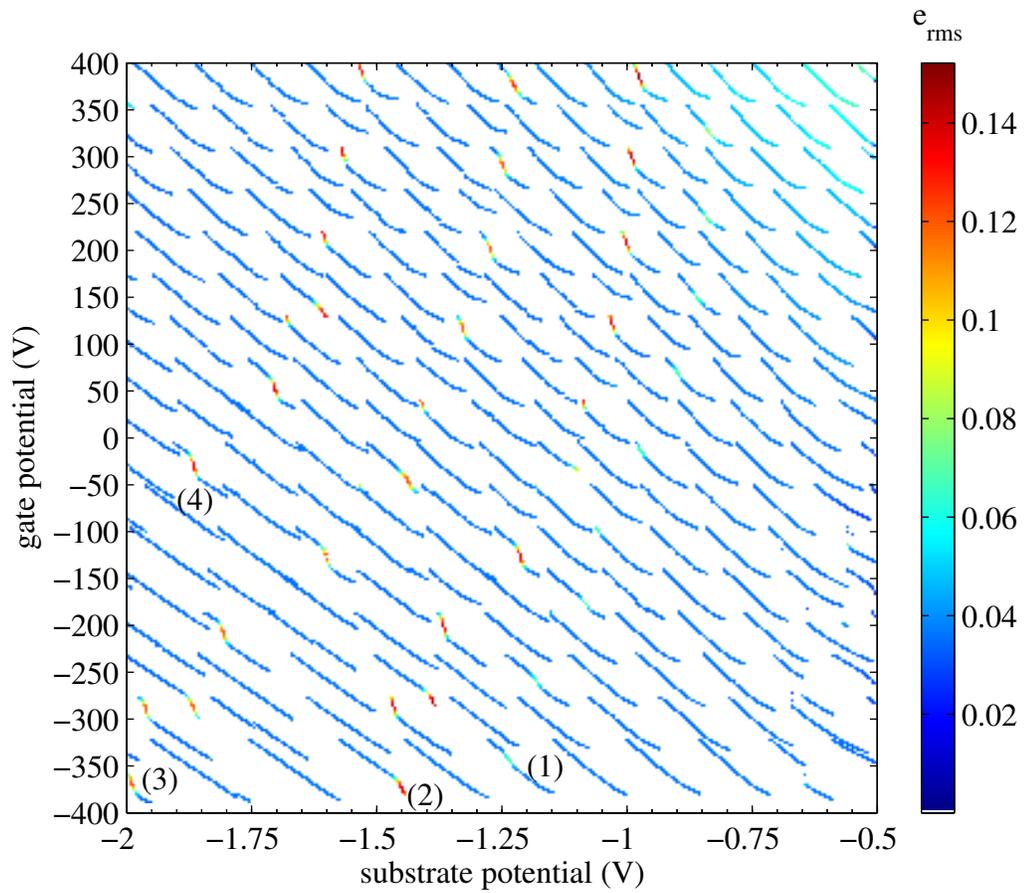


Figure 4.32: Response of SET5-2-5 to an ac dither on the substrate as a function of dc substrate potential and gate voltage. This is the same data as in Figure 4.30.

of  $A$ . Therefore its Fourier component at  $f$  as measured by a lock-in amplifier would also not depend on  $A$ . In contrast, if the motion of the electron were continuous instead of discrete, it would induce a response in the SET at the same frequency  $f$  but with an amplitude that depended on  $A$ . To test this theory I took the data in presented Figure 4.33, sweeping over resonator #2 from Figure 4.30 multiple times, changing the value of  $A$  between each data set. For each data set I fit a gaussian with a linear background and extracted the peak response and width of the resonator as a function of driving amplitude; the peak response is plotted in Figure 4.34 with a linear extrapolation of the first four data points. The peak response extrapolates to zero for zero driving amplitude; it becomes nonlinear at large drive amplitudes, but this is due to the nonlinearity of the SET. More surprisingly the peak width, as measured by the standard deviation of the fitted gaussians, is a constant  $8.5 \pm 0.1$  mV independent of driving amplitude! These two facts mean that the charge motion is continuous, not discrete, and that it has extremal locations. This becomes obvious if we look at the inset to Figure 4.33, showing the feedback circuit on the gate compensating for the moving charge when the substrate voltage sweeps over the resonance; even with no dither applied it takes a few mV to fully move the charge from one location to the other. There are three possible explanations for this broadening: noise on the bias lines, thermal fluctuations, and quantum tunneling. The sheer size (8.5 mV) of the broadening rules out noise, as we know from the observed Coulomb blockade that our bias lines are quieter than a few hundred  $\mu\text{V}$ . I cannot rule out thermal fluctuations, because I did not study the effect of temperature on the peak width, nor can I rule out quantum tunneling. Imagine two tunnel coupled charge traps, coupled strongly enough that there is significant wave function overlap between them and therefore that charge transfer happens not discretely but continuously. For a small enough applied field all of the charge is localized in one of the traps, and for a large enough bias it is all in the other. In between these two values lies a regime where some of the charge lies in each trap, and the proportion depends on the applied field. Or imagine that the two traps were weakly

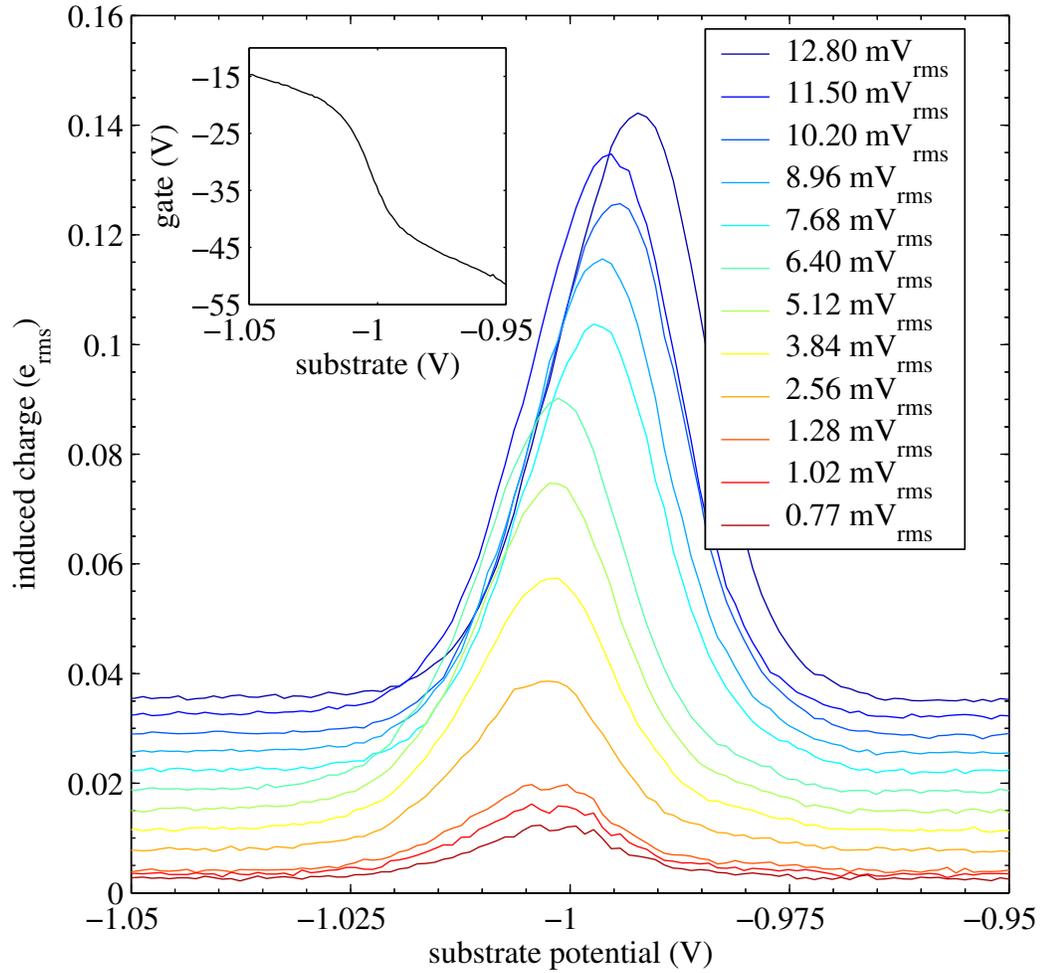


Figure 4.33: Response of a charge fluctuator to an ac dither with various amplitudes. The curves are plots of the SET induced charge as a function of substrate dc bias; each curve corresponds to the ac driving amplitude given in the legend. Inset: response of the feedback circuit on the gate when crossing the resonance.

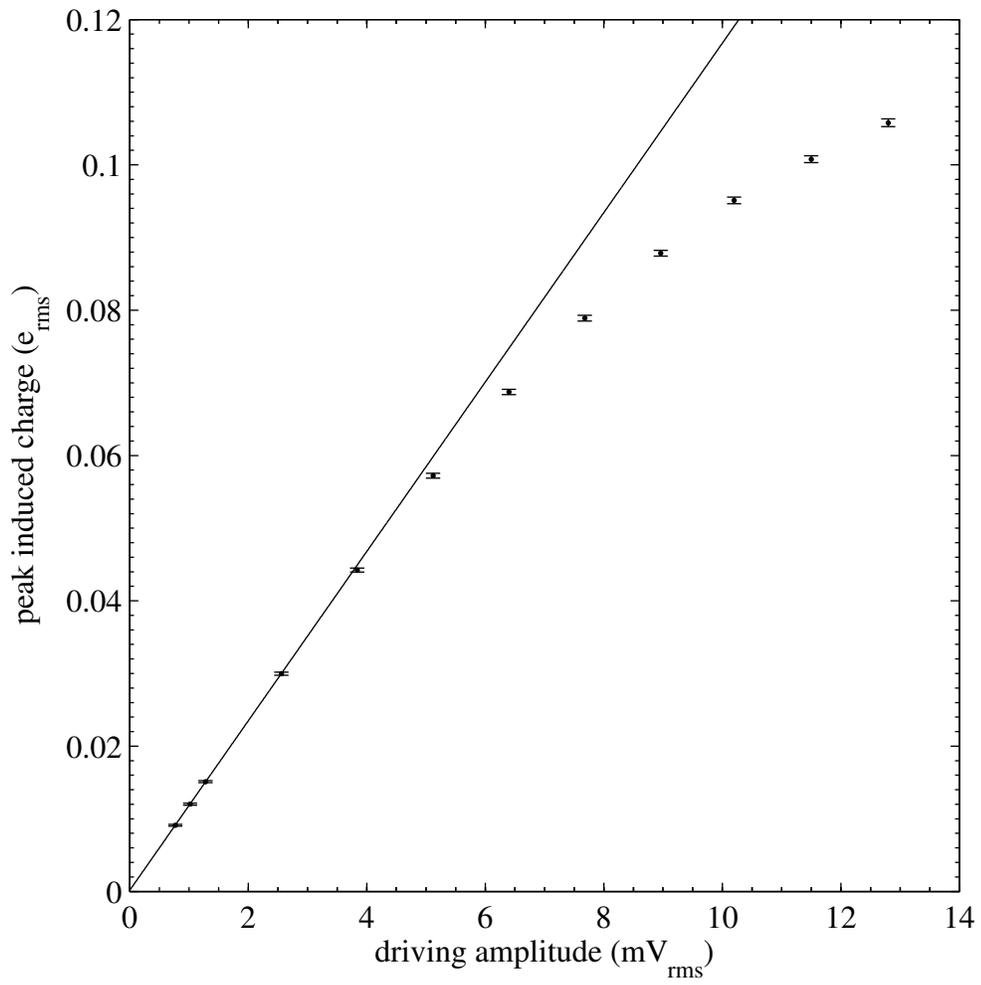


Figure 4.34: Dependence of the amplitude of motion of a resonator on driving amplitude. The line is a fit to the first four data points.

coupled, but that the charge transfer between them was thermally assisted and therefore also broadened. These models, rather than that of a donor weakly coupled to the Si/SiO<sub>2</sub> interface, are a better match to the data in Figure 4.33. It could still be explained as a donor only a few Bohr radii from the interface and therefore strongly coupled to it, but this seems unlikely in light of the reasons I have already given.

Figures 4.33 and 4.34 give us another clue to the location of these resonators from the sheer size of the charge motion they represent. The peak amplitude is  $0.106 e_{\text{rms}}$ , corresponding to a peak-to-peak charge motion of  $0.3 e$ . Referring way back to Figure 3.14, it becomes clear that this signal is too large to be coming from single charge motion in the substrate, for which the largest signal we could possibly expect is  $0.26 e$ , corresponding to an electron moving all the way from beneath the island to infinity. Furthermore, the sensitivity gradient in the oxide beneath the island is  $\approx 3.7 \text{ me}/\text{\AA}$ , so that a  $0.3 e$  signal corresponds to  $80 \text{ \AA}$  of motion. I cannot think of an obvious mechanism for a single charge to move quickly and reproducibly by such a huge distance through SiO<sub>2</sub>.

Perhaps the best explanation for the source of these signals is that they are due to charges moving between grains of Al on the surface of the wafer. Consider Figure 4.35, a highly magnified SEM image of an SET with this geometry, which shows the island of the SET surrounded by 5-10 nm size Al grains. There are five obvious grains suspended on the lead to the right of the island and separated from it by less than 5 nm. These come from the second of two evaporations in the double-angle technique, while the lead they sit upon comes from the first. So they are separated from that lead by the same tunnel oxide as makes up the SET tunnel junctions. Such grains near the island could fit the behavior of the fluctuators outlined in this section well. They lie above the oxide surface; they reside in an area where the fields from the gate and from the substrate could be opposed and where the fields from the gate certainly are not shielded; an electron moving from one grain to another could induce a large fraction of an electron on the island; and the motion could be relatively continuous instead of discrete, either from

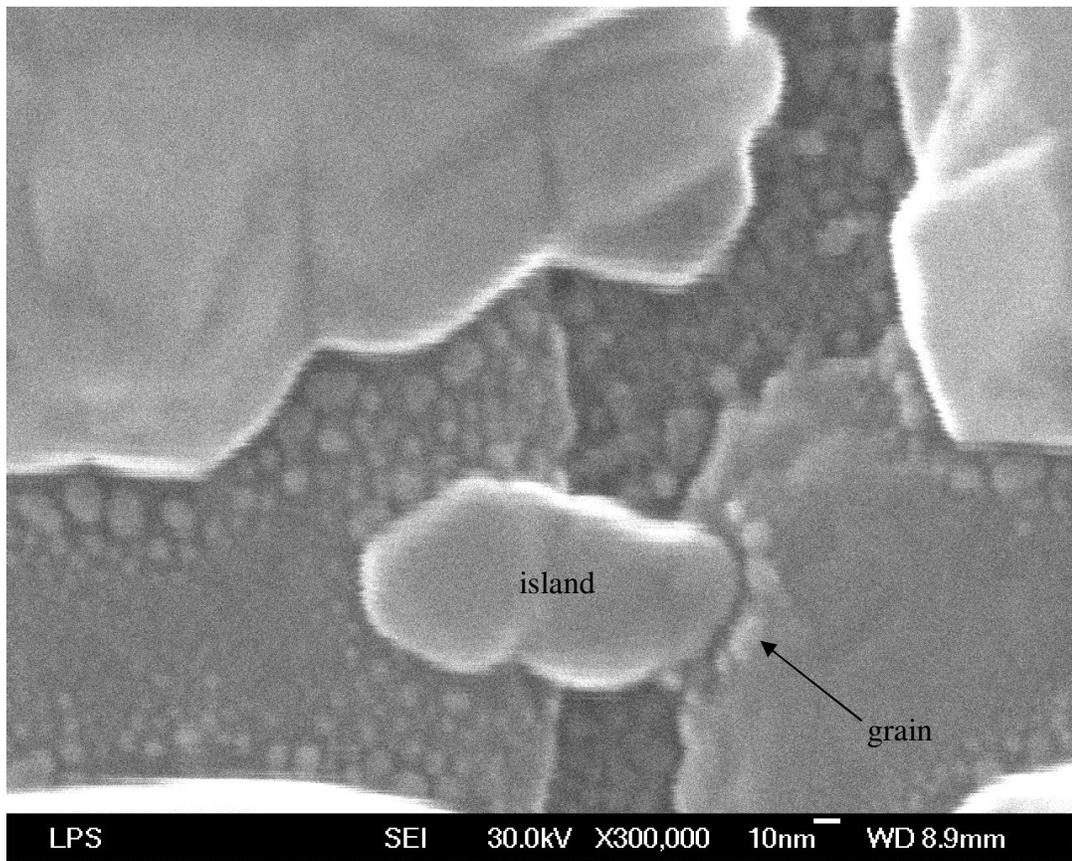


Figure 4.35: SEM close-up of an SET island showing nearby Al grains.

tunnel coupling or from thermal broadening. Furthermore, because these grains are so much smaller than the SET island we would expect the grain-substrate and grain-gate capacitances to be correspondingly smaller: for a  $5 \text{ nm} \times 5 \text{ nm}$  grain the substrate and gate capacitances should be about 10 zF and 10 yF, respectively, whose ratio agrees reasonably with the measured values for  $\alpha$ . The corresponding substrate 1 e period is 18 V, too large to observe more than a single charging event for a given grain in the voltage range I examined in Figures 4.28 and 4.29. This would explain why we do not see a regularly repeated charging of the same fluctuator in these datasets. Furthermore, if I assume that the total capacitance of these grains is at least greater than 1 aF, and that the electronic temperature is about 100 mK, I would expect a broadening of order

$$\Delta V_s = \frac{C_\Sigma k_B T}{C_s e} \quad (4.6)$$

$$\approx \frac{1 \text{ aF}}{10 \text{ zF}} (86 \mu\text{V/K})(100 \text{ mK}) \quad (4.7)$$

$$\approx 1 \text{ mV} \quad (4.8)$$

This is a bit small to explain the observed 8 mV broadening, but considering the approximate nature of the calculation, perhaps not surprisingly so.

In fact, such an explanation for these poorly understood signals is not so incredible when one realizes that there have already been many studies of the electronic states of metallic nanoparticles. For example, Yadavalli *et al.* have measured the charging and discharging of a floating Al island through a 5-10 nm gap with the goal of using it as a memory device,[88] while D. C. Ralph and coworkers studied the discrete electronic states of aluminum nanoparticles about 10 nm in diameter.[89] Of course, there are also several groups working to make a qubit from the Cooper pair box, which is just a superconducting nanoparticle connected via a tunnel junction to a lead.[90]

## 4.11 Conclusions

In summary, I have observed evidence for gross charge motion in more heavily doped substrates ( $10^{12}$  donors/cm<sup>2</sup>), using SETs both of a traditional design and of a more radical wide lead geometry. There were no discernible effects from donors at lower doping levels ( $\leq 10^{11}$  donors/cm<sup>2</sup>) in any sample. However, even nominally intrinsic substrates show some time-dependent charge relaxation worthy of further investigation. Comparison of CV measurements from a large capacitor with those from a wide lead SET indicate that the electrostatics of this new design are well characterized, but they also show that the implanted p++ region is far from ideal as a gate because it leads to hysteresis and drift. The SET biasing gate above the substrate in this geometry has a capacitance that fits a simple parallel plate model, but it clearly still influences charge motion near the SET despite that it was designed to prevent this. Finally, lock-in measurements of all the samples reveal resonances that cannot come from donors, but most likely come instead from small, isolated Al grains on the wafer surface.

## Chapter 5

### Millikelvin scanned probe for measurement of nanostructures

#### 5.1 Introduction

This chapter, based upon a paper that I published in *Review of Scientific Instruments*, is a bit of a digression from the earlier chapters, in that it is not really concerned with SETs and donors at all.[91] Instead it covers my attempt to address an issue that has been present since Kane first proposed a measurement of individual donors using an SET on a randomly doped Si substrate: how to measure a large number of SETs during a single experimental run. The issue is even more pressing in light of the previous chapters, from which it has become evident that we will need to move towards more lightly doped substrates than we have used in the past to ensure that the donors are not interacting. This is not a challenge that we would face if we had fabrication capabilities with atomic precision; in that case we would simply place a donor in the Si substrate where we wanted it and make an SET directly above that donor. While there are groups working on technologies for atomically precise doping, we do not have such a technology available to us.[19, 20, 22, 23, 24, 21] The technology we do have readily available is ion implantation, possibly through a mask, which places donors randomly in the  $x$ - $y$  plane and at a depth beneath the surface with large statistical uncertainty. Now it is certainly possible to implant a substrate with a large enough density of donors that each SET fabricated on the surface will have a sizeable number of donors beneath it. But for a  $50 \text{ nm} \times 50 \text{ nm}$  SET island this corresponds to a donor density  $> 10^{11} / \text{cm}^2$ , and as we saw in Chapter 3 there is significant wave function overlap at the interface for donor electrons at this density, and they will not behave as individual electronic systems. The solution is to lower the implant density to a level ( $< 10^{10} / \text{cm}^2$ ?) where the individual donor wave functions do

not overlap much, but this means that each SET will no longer have a reasonable number of donors beneath it: for a  $50 \text{ nm} \times 50 \text{ nm}$  SET this doping level only places a donor beneath one in every four SETs! This doesn't even take into account the statistical uncertainty in donor depth during implant and the fraction of donors which properly occupy substitutional sites, both of which only serve to lower the number of SETs with a measurable donor nearby. Increasing the size of the SET island is not a good solution, either, because the sensitivity of the SET to the motion of a nearby electron goes down with increasing size. I can only conclude that to observe an individual donor with an SET on a randomly implanted substrate will require measurement of a very large number of SETs to find those that are aligned properly, or a movable SET.

Measuring a large number of SETs with high bandwidth on a single chip is not trivial. An SET will not show Coulomb blockade, and therefore will not be a good electrometer, if its resistance is not  $\gtrsim h/e^2 \approx 25.9 \text{ k}\Omega$ . [92] Furthermore, avoiding thermally excited transitions between up/down spin states of the donor electron, separated by  $230 \mu\text{eV}$  in a 1 T magnetic field, requires temperatures well below 2.5 K, and therefore requires that the experiments be done in a cryostat. The high resistance of the SET combined with the inevitably high capacitance ( $\gtrsim 100 \text{ pF}$ ) to ground of the cables extracting its signal from the cryostat form a low-pass filter with a cutoff frequency  $< 60 \text{ kHz}$ , and this is a conservative upper bound. In our dilution refrigerator the cable capacitance is closer to 1 nF which brings the measurement bandwidth down by another order of magnitude. Schoelkopf *et al.* have devised a clever way to circumvent this problem, the rf-SET, that uses a resonant tank circuit to match the impedance of the SET to the  $50 \Omega$  impedance of a microwave transmission line. [31] The rf-SET requires careful engineering of the tank circuit, microwave transmission line, and SET resistance, so that using rf-SET technology to measure a large number of SETs on a single chip would be a serious engineering challenge by itself, although frequency domain multiplexing rf-SETs have been demonstrated with small numbers of devices. [34] A different solution is to use a cryogenic amplifier

within the cryostat itself, placed close enough to the sample that the stray input capacitance is significantly reduced.[32, 33] In theory the capacitance could be reduced below about 10 pF for an off-chip amplifier, while it could be reduced even further if the amplifier were integrated on the same chip as the SET. Use of a cryogenic amplifier to measure many SETs still requires some sort of multiplexing technology to determine which SET is measured at any particular time. One can imagine a multiplexer based on FET's that works at low temperatures, but we chose instead to test the idea of using a low temperature scanned probe connected to the amplifier to individually address the SETs of an array. Although we used this idea to measure SETs, it could be used to measure almost any array of high impedance nanostructures with high bandwidth and low noise.

The scanned probe we built is a scanning force microscope (SFM), based upon a quartz tuning fork, that operates below 100 mK and in magnetic fields up to 6 T. The microscope has a conducting tip for electrical probing of the nanostructures of interest, and it incorporates a low noise cryogenic amplifier to measure both the vibrations of the tuning fork and the electrical signals from the nanostructures. At millikelvin temperatures the imaging resolution is below 1  $\mu\text{m}$  in a  $22 \mu\text{m} \times 22 \mu\text{m}$  range, and a coarse motion provides translations of a few mm. In the following pages I will show data locating an SET within an array and measuring its Coulomb blockade with a sensitivity of  $2.6 \times 10^{-5} e/\sqrt{\text{Hz}}$ .

There exists a variety of scanned probe techniques that have been adapted or developed to study nanostructures and transport at cryogenic temperatures, including atomic force microscopy,[93, 94] scanned gate microscopy,[95] scanning capacitance microscopy,[96] and Kelvin probe microscopy.[97] Crook *et al.* recently even reported a technique for nanolithography using a scanned probe at dilution refrigerator temperatures.[98] In our scanned probe the imaging capability of the SFM located a particular SET within an array, and the conducting probe tip provided an electrical connection between that SET and a cryogenic preamplifier.

## 5.2 Experimental setup

Figure 5.1 shows the physical layout of the microscope. The force sensor is a quartz tuning fork (Raltron R38-32.768-12.5) with a sharpened W tip glued to one of its tines.[99] The sub-pW power dissipation of the fork has no measurable effect on the base temperature of our refrigerator, and the laser-free piezoelectric detection scheme avoids problems with light sensitive samples. The scanner is a commercial cryogenic STM scan head (Omicron's CryoSXM[100]) modified for SFM and mounted on the baseplate of an Oxford Kelvinox 100 dilution refrigerator.[101] The microscope incorporates a cryogenic amplifier for maximum sensitivity and bandwidth. We use a phase-locked loop (Nanosurf easyPLL)[102] to excite the fork.

Piezoelectric quartz tuning forks have been used as force sensors in scanning probe microscopy for several years now. Mechanical and electrical models predict that forces acting on a fork change its resonant frequency and  $Q$ . [103, 104, 105, 106] Frictional forces change  $Q$  while conservative forces change the frequency. Our microscope uses the frequency shift as the force dependent signal, varying the tip height to maintain a constant shift while rastering over the sample surface.

Figure 5.2 shows a block diagram of the microscope's operation. The tuning fork is excited with an ac potential applied to one of its electrodes. The other electrode is held at virtual ground by the input of a cryogenic transimpedance amplifier, discussed below. We use a bridge circuit[103] to eliminate the effects of stray capacitance between the two electrodes. Measuring the current flowing between the two electrodes with the transimpedance amplifier is a simple but effective way to measure the motion of the fork.

We use a phase-locked loop (PLL) to monitor the frequency of the fork and to insure that it is always driven on resonance.[107] This PLL has a nominal sensitivity of 5 mHz in a 1 kHz bandwidth, but we obtained a sensitivity less than this in practice, typically a few tens of mHz. This sensitivity was limited primarily by white noise from the cryogenic

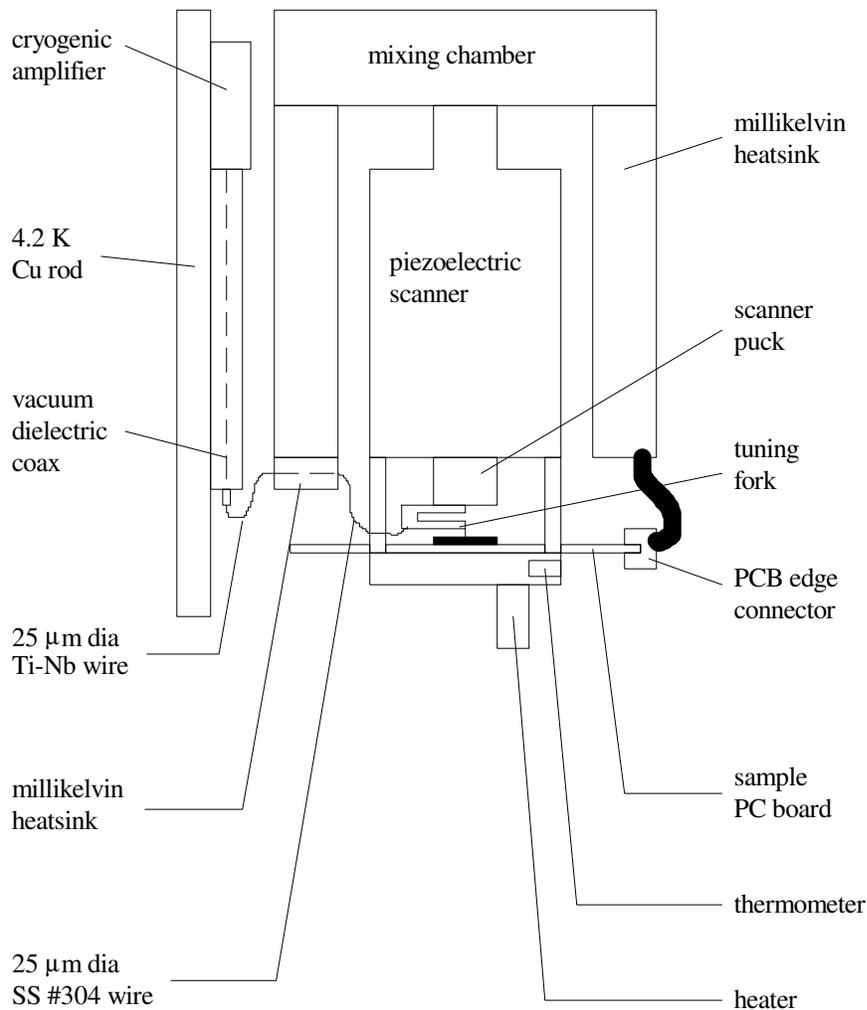


Figure 5.1: Physical layout of the scanning force microscope. The piezoelectric scanner is attached to the mixing chamber of the dilution refrigerator, and the sample is mounted on a printed circuit board suspended below the scanner. All the leads to the sample are heatsunk to the mixing chamber. The cryogenic amplifier is attached to a 4.2 K finger that comes down alongside the scanner, and the tuning fork is connected to the amplifier via 25  $\mu\text{m}$  diameter wires. The vertical distance between the tuning fork and the amplifier is approximately 20 cm, placing the amplifier outside any applied magnetic field. The entire setup is at cryogenic UHV pressure inside the dilution refrigerator vacuum can.

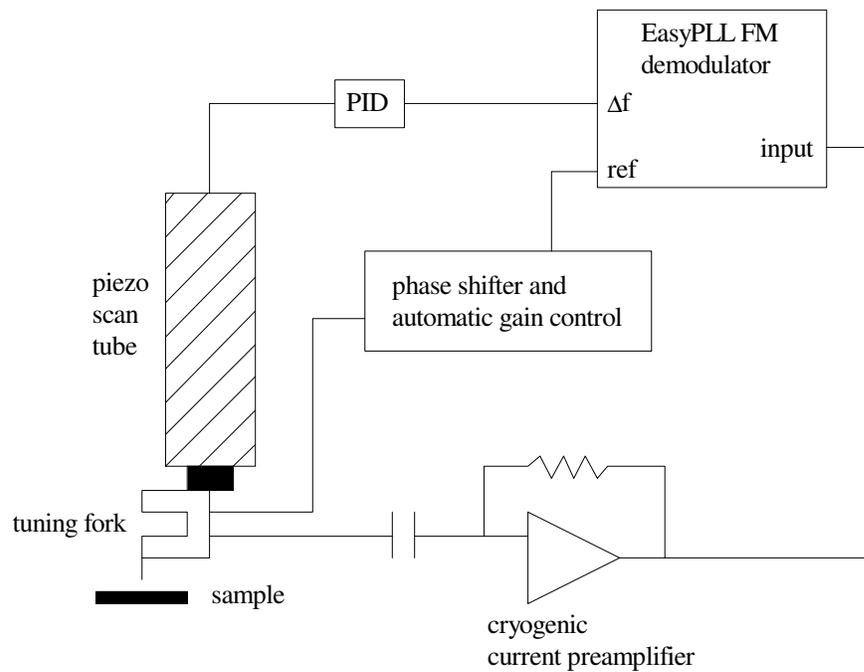


Figure 5.2: Block diagram of the cryogenic scanning force microscope. Proportional-integral-differential circuitry controls the scan piezo to maintain a constant frequency shift of the tuning fork. The fork is driven by the reference output of the easyPLL with a suitable phase shift and automatic gain control. The response is measured with a cryogenic amplifier and sent to the input of the easyPLL. The cryogenic amplifier is simultaneously connected to the metallic tip on the tuning fork and to the tuning fork electrode.

amplifier near the resonant frequency.

The scanner was originally designed for STM at 4.2 K in a helium exchange gas environment. We have detached the scan head from its original mounting rod and attached it to the base plate of the dilution refrigerator. The high-voltage signals for piezoelectric control are carried on twisted pairs from room temperature to 4.2 K and on superconducting twisted pairs from 4.2 K to the mixing chamber, thereby minimizing heat load on the refrigerator. There is more discussion of our refrigerator wiring in Chapter 4. In contrast with Omicron's intended configuration of scanning the sample, we scan the tuning fork with the sample fixed. This allows us to connect multiple leads to the sample and to control its temperature more easily.

The maximum  $\pm 135$  V scan voltage provided by the Omicron electronics gives a range of  $35 \mu\text{m} \times 35 \mu\text{m}$  at room temperature. This decreases to  $7 \mu\text{m} \times 7 \mu\text{m}$  at 4.2 K and below because there is a smaller piezoelectric response, and this range is frequently too small to be useful. The  $z$  range similarly decreases from  $2.7 \mu\text{m}$  to  $0.5 \mu\text{m}$ . To increase the scan range at low temperatures we have added an additional high-voltage amplifier (RHK HVA-900)[108] that provides scan voltages up to  $\pm 450$  V, yielding a maximum scan range of  $22 \mu\text{m} \times 22 \mu\text{m}$  and a maximum  $z$  range of  $1.8 \mu\text{m}$  below 4.2 K. The scanner also provides a slip-stick based coarse motion both in the  $x$ - $y$  plane and in the  $z$  direction. Motions of a few mm in  $x$  and  $y$  and up to a few cm in  $z$  are possible. However, we have at times found coarse motion in the  $x$ - $y$  plane to be unreliable. It would at times get stuck or move in seemingly random directions.

### 5.3 Cryogenic amplifier electronics

The microscope requires a transimpedance amplifier to measure the current through the tuning fork while scanning. The same amplifier measures the current through an SET while probing. To decrease the unavoidable parasitic capacitances in these measurements

we have constructed a *cryogenic* transimpedance amplifier and placed it near the sample on a copper rod heat sunk to 4.2 K. As an added benefit the cryogenically cooled current-sensing resistor has significantly lower Johnson noise than it has at room temperature. The amplifier is based upon a low-noise silicon junction field effect transistor (JFET-Moxtek MX120, gate capacitance 1.7 pF, input-referred voltage noise  $\sim 3 \text{ nV}\sqrt{\text{Hz}}$ ,  $1/f$  knee below 1 kHz) that stops working below  $\sim 60 \text{ K}$ . [109] In order to maintain most of the circuit at 4.2 K while allowing the JFET to heat above 60 K we have designed the circuit with two printed circuit boards. The lower board contains most of the circuit elements and is held at 4.2 K. The upper board containing the JFET is mounted to the lower one with 1/16 in. diameter nylon standoffs. All connections between the two boards are made with 25  $\mu\text{m}$  diameter stainless steel wire to minimize thermal loading. The amplifier dissipates  $\sim 20 \text{ mW}$  during operation and raises the base temperature of the refrigerator by less than 0.5 mK to about 15 mK. To achieve such a small thermal load on the mixing chamber it is crucial that the copper box enclosing the amplifier is leak-tight, light-tight, and well heat sunk to the 4.2 K bath. A charcoal sorb inside the box captures residual gas that otherwise would prevent the JFET from heating properly in such close proximity to the cold walls.

The input to the amplifier is capacitively coupled via a 4.7 nF capacitor and a coaxial cable to one of the tuning fork electrodes, and via the metallization on the tuning fork to the conducting probe tip. We capacitively couple the signal to avoid problems with dc offsets. For thermalization at the mixing chamber the coax has a 2 cm length of Stycast 2850FT [110] as its dielectric, which contributes  $\sim 18 \text{ pF}$  stray capacitance to ground. The remainder of the coax has a vacuum dielectric to minimize its capacitance, so that the total stray input capacitance, including the gate capacitance of the JFET, is only  $\sim 35 \text{ pF}$ . This means that for a 50 k $\Omega$  SET the bandwidth of measurement is limited to  $\sim 100 \text{ kHz}$ . Higher speeds are possible only at the expense of further noise.

## 5.4 Scan modes

For the purposes of locating micron-sized pads and contacting a large number of them in a reasonable period of time, scan speed rather than scan resolution is the critical factor. We would ideally like to scan the entire  $22\ \mu\text{m}$  range of the scanner in a few minutes. We have investigated three different force regimes or scan modes: a short-range repulsive force mode, a weaker attractive force mode, and a long-range electrostatic force mode. The repulsive mode, corresponding to positive frequency shifts of a few Hz, yielded the highest resolution images but was the least useful for our purposes. The very small tip-sample separation and highly nonlinear frequency versus separation dependence made optimization of the feedback loop difficult and led to frequent tip crashes at reasonable speeds. Faster scanning was possible with a weaker attractive force, corresponding to negative frequency shifts of a few hundred mHz, because it corresponds to a larger tip-sample separation. However, with this scan mode we were only successful using smaller, more sensitive forks that have other disadvantages as explained below in Section 5.7. The fastest scanning was obtained by charging up the tip through a diode, so that it felt a strong attractive force from the image charges in the sample.[111] The resulting force is of sufficient range to have easily measured effects even with tip-sample separations greater than 50 nm. This scan mode works on insulating substrates (e.g.,  $\text{SiO}_2$ ) provided that the dielectric constant of the substrate differs from that of the vacuum, and yielded scanning speeds of  $20\ \mu\text{m/s}$  or more.

## 5.5 Samples and measurement techniques

My samples consisted of a  $100\ \mu\text{m} \times 100\ \mu\text{m}$  array of about 100 Al-AlO<sub>2</sub>-Al SETs fabricated with standard e-beam lithography and double-angle evaporation.[83] Each SET had a small ( $150\ \text{nm} \times 50\ \text{nm}$ ) island weakly coupled to source and drain leads via oxide tunnel barriers and capacitively coupled to a gate. A schematic of the sample layout is

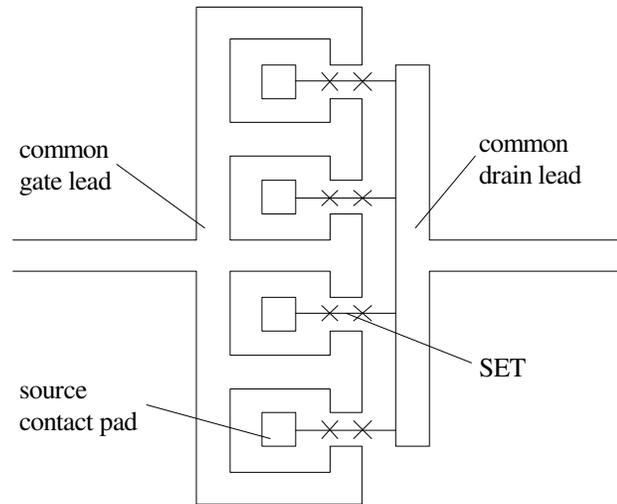


Figure 5.3: Schematic of an array of four SETs showing common gate and drain leads. Each SET has a contact pad attached to its source terminal so that it may be measured with the scanned probe.

shown in Figure 5.3. Within the array, all of the SET gate terminals were wired to a single coaxial lead, and all of the drain terminals to another. The source terminal of each SET was connected to its own  $3\ \mu\text{m} \times 3\ \mu\text{m}$  Pt contact pad.

Sample fabrication involved three layers of lithography on an undoped Si substrate. First the common gate and drain leads as well as the source contact pads were patterned with photolithography. A trilayer consisting of  $30\ \text{\AA}$  Ti,  $120\ \text{\AA}$  Pt, and  $2500\ \text{\AA}$  Au was evaporated using NR7-1500PY resist as a mask. Second, we masked the Au bond pads with another layer of photolithography and etched the Au away near the sample center to expose the Pt layer.[82] This left a thick Au layer for the bond pads but a thin Pt layer for the SET array. The metallization for the array needs to be both thin and oxide free. Thin metallization allowed us to increase the scan speed of the microscope, because it alleviated problems with tip crashes at step edges. The metal surface must also be oxide free to insure low resistance contact between it and the Al SET lithography, as well as to insure low resistance contact between the contact pads and the microscope tip during probing. This means that we could not use my now standard all-Al process, described

in Chapter 4, if we decided to do more experiments with the scanned probe, because the probe tip cannot push through native  $\text{AlO}_x$ . We would instead have to wirebond from the Al chip to a separate chip that the scanned probe could contact. In the third fabrication step I used standard e-beam lithography to write the SETs and ashed the sample to remove any residual organics on the metal surfaces. The sample was attached with a spring clip to a printed circuit board, and Au wires were attached to the lithographically defined leads. It is important that the wires all come off the sample in a single direction, away from where the scanned probe will be, so as not to obstruct its motion.

Typical measurements proceeded in two sequential steps. First I would scan the surface of the sample until I found an SET of interest. Then I would turn off the tip-sample feedback loop and establish electrical contact between the probe tip and the Pt contact pad (lightly crash the tip). An ac voltage (50-100 kHz) was applied to the drain lead, and the current through the SET was monitored with the cryogenic amplifier and a lock-in.

The only topographic information required for these measurements is the location of the contact pads. These are large and separated from the surrounding lithography by  $2 \mu\text{m}$  on all sides. Therefore the required resolution of the SFM is only about  $1 \mu\text{m}$ . This fact is important as the probe resolution tends to deteriorate over time with repeated probing and cleaning.

## 5.6 Results and discussion

Figure 5.4 is an image taken at millikelvin temperature showing part of an SET array. The image clearly demonstrates resolution below  $1 \mu\text{m}$  at a scan speed of  $15 \mu\text{m/s}$  and a scan range of  $22 \mu\text{m}$ . Although we observe no extra heating of the refrigerator while the scan piezo is held motionless, there was enough heating during scanning to raise the temperature of the sample from 15 mK to 190 mK. The amount of heating depends

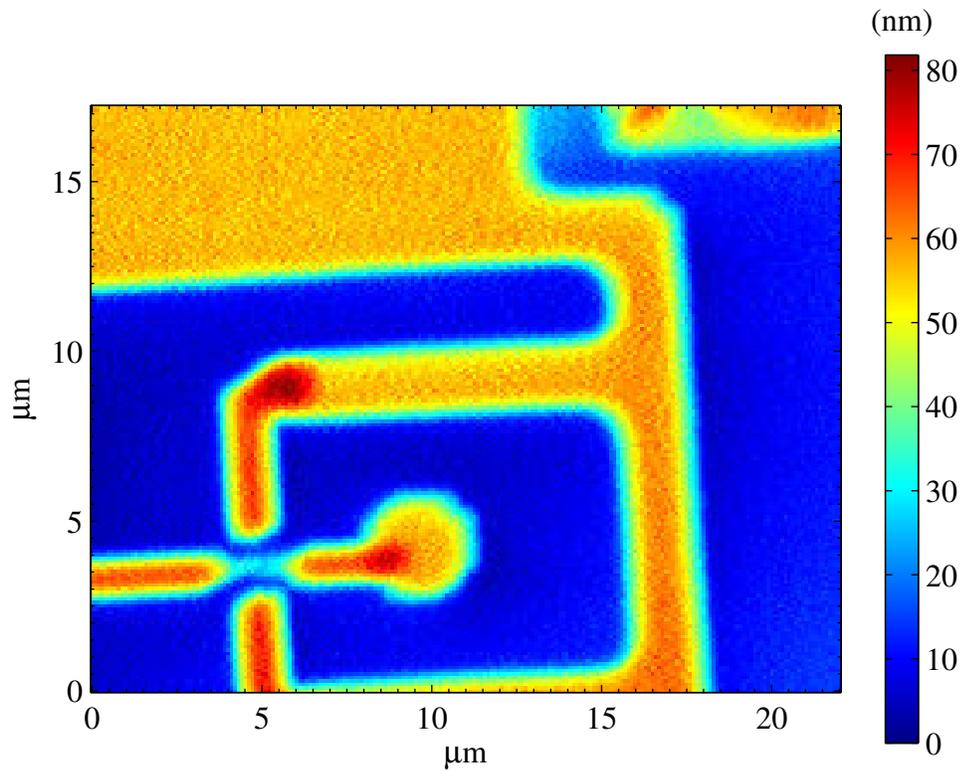


Figure 5.4: SFM scan showing Pt (orange) and Al (red) features lithographically defined on an oxidized silicon substrate (blue). The scan was taken with  $V_{\text{tip}} = -40$  V and  $\Delta f = -0.5$  Hz at a speed of  $15 \mu\text{m/s}$ . During scanning the sample temperature rose to 190 mK and the mixing chamber temperature rose to 35 mK. The  $3 \mu\text{m} \times 3 \mu\text{m}$  Pt square near the center of the image is the contact pad of the SET.

strongly on the scan size and speed. For example, scanning a range of  $10\ \mu\text{m}$  at a few  $\mu\text{m/s}$  keeps the temperature well below 100 mK. In practice this heating should not cause problems because the piezo is held motionless while probing an SET.

I have electrically probed several SETs on multiple samples. Figure 5.5 shows characteristic Coulomb blockade oscillations of one. To obtain this data a 100 kHz,  $100\ \mu\text{V}$  rms voltage was applied to the drain lead, and the in-phase component of the resulting ac current was measured by a lock-in. The SET was kept in the normal state by a 1 T magnetic field. The current never drops all the way to zero on the modulation curve because the  $100\ \mu\text{V}$  rms drain-source voltage was larger than the Coulomb blockade plateau for this SET.

I also made measurements of the charge sensitivity of the SET/amplifier configuration. Applying a known amount of charge to the gate of the SET and measuring the response at the output of the lock-in calibrates the gain. Comparing this gain with the noise measured at the output of the lock-in gives the charge sensitivity. For a different device than the one in Figure 5.5, with resistance  $\sim 80\ \text{k}\Omega$ , I measured a charge sensitivity of  $2.6 \times 10^{-5}\ e/\sqrt{\text{Hz}}$  near 10 kHz. This sensitivity was limited by the Johnson noise of our feedback resistor ( $20\ \text{nV}/\sqrt{\text{Hz}}$ ) and by the input-referred voltage noise of our amplifier. The equivalent current noise values are  $20\ \text{fA}/\sqrt{\text{Hz}}$  and  $38\ \text{fA}/\sqrt{\text{Hz}}$ , comparable to the intrinsic  $\sim 10\ \text{fA}/\sqrt{\text{Hz}}$  shot noise of the SET.

## 5.7 Experimental challenges

There are several challenges that this technique for measuring a large number of SETs still faces for it to become practical. As I mentioned earlier, the coarse positioning capability of our Omicron scan head was very unreliable, and this kept us from really being able to measure a large number of SETs in an array. I successfully measured three SETs in an array, but never more than that. However, this is an engineering problem, and

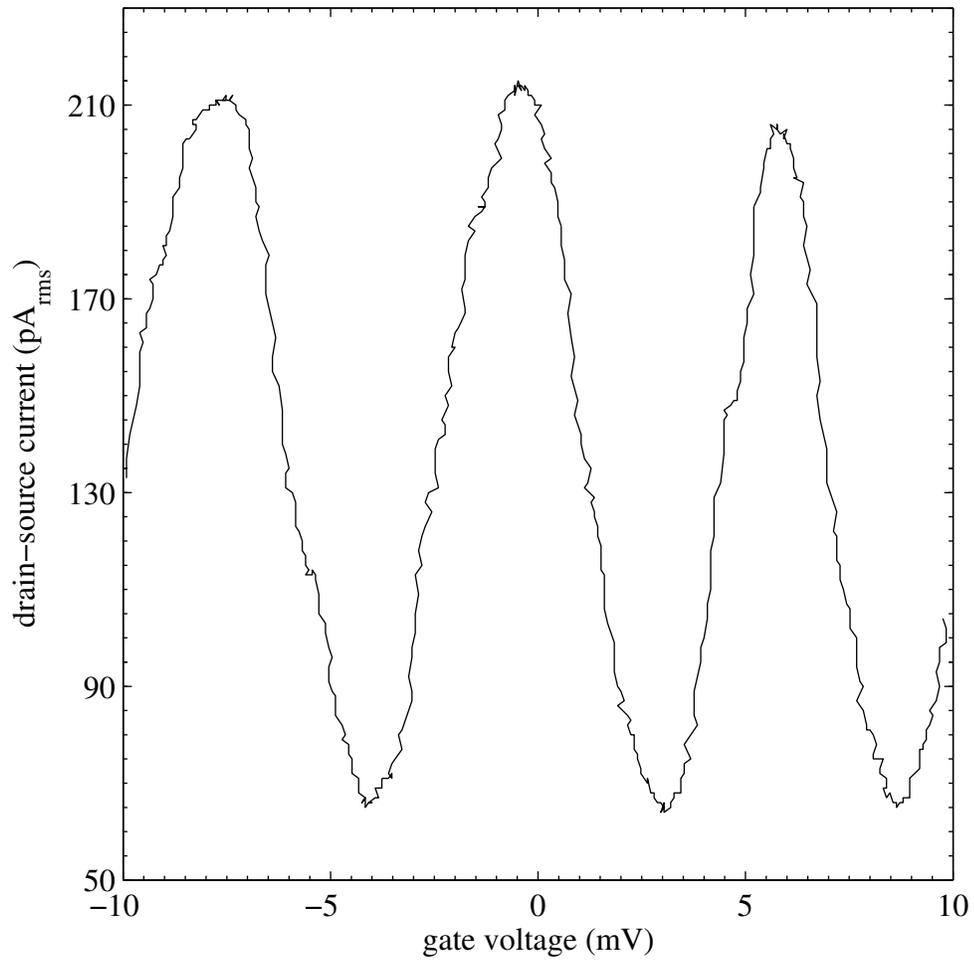


Figure 5.5: Coulomb blockade oscillations of the current through a single electron transistor, as measured with the cryogenic scanned probe. The data were measured at 60 mK with  $B = 1$  T and  $V_{ds} = 100 \mu\text{V}$  rms at 100 kHz.

I believe it can be fixed with a custom-designed scanner and a more carefully designed coarse motion drive.

A more serious issue is that of which scan mode, repulsive, attractive, or electrostatic (see Section 5.4) to use for imaging. While the repulsive mode gave the highest resolution, it was very slow, because it forced the tip to track every detail of the sample surface without crashing. Instead I was able to get faster scans using the weak attractive mode by following the advice of Giessibl.[112] In this case I used smaller forks with an entire prong glued down. The smaller spring constant of these smaller forks should yield higher force sensitivity, and gluing down an entire prong should give a  $Q$  independent of the mass of the tip, while for a fork glued only at its base the tip mass breaks the symmetry of the tines and leads to dissipation. However, even though I at times obtained beautiful images with these smaller forks, they had a greater problem: I found that tuning forks with an entire prong glued down exhibited a strong coupling to the piezoelectric scan tube. This manifested itself as seemingly random shifts in the fork resonant frequency when the scan tube expanded or contracted, making scanning difficult or impossible. I observed no similar shifts using forks glued only at the base, presumably because in this case the vibration is decoupled from its support. In contrast, a fork with its entire prong glued down incorporates its support structure into the system, and we should expect that small changes in the support structure could strongly affect its vibrations. The larger forks glued at the base are not sensitive enough to feel the weak attractive forces that are present before tip-sample contact. This explains why eventually I was forced to charge up the tip to obtain a stronger electrostatic tip-sample force. This electrostatic mode has problems of its own in that the 40 V I applied to the tip was often lethal to the SETs if it got too close. More than one time I allowed the tip to get too close to an SET and the entire sample was destroyed from the discharge.

Another challenge was the establishment of low-resistance contacts reliably and repeatably between the Pt contact pads and the probe tip. I had moderate success with

both PtIr and W tips and repeatably achieved contact resistances less than 1 k $\Omega$ , although I was most successful using W tips. I expected to have no difficulties with PtIr tips due to the lack of native oxide, but I found that they were contaminated easily. Therefore I inevitably needed to clean the tip with field-emission into the sample before making the first contact after cooldown. To clean a tip I would position it  $\sim$ 1 nm away from a grounded area of the sample surface and apply successively more negative voltages until I saw an abrupt increase in the tip-sample current, indicating a clean tip. To maintain a clean sample surface while cooling the refrigerator I took care to maintain the sample temperature above that of the walls of the vacuum space, insuring that any contaminants condensed on the walls instead.[94] Nevertheless, I often found that I had to push much harder with the tip into the contact pad than I would have expected, and I believe that this is due to a residual layer of contamination, perhaps frozen water, that was still present on the sample surface. I suspect that the sample would need to be heated to a very high temperature while the refrigerator was cooled to really keep its surface clean, and this might be detrimental to the SETs or to the refrigerator itself.

As a final challenge, my newest recipe for SETs on Si (see Chapter 4) only uses Al for the source and drain leads instead of Pt. This is important, because it allows a final fabrication step to passivate the Si/SiO<sub>2</sub> surface with a 450°C anneal in forming gas, without having any eutectic formation between the Al and other metals. Nevertheless, such a recipe is probably incompatible with the scanned probe measurement scheme outlined here, because the scanned probe may not be able to push through the native AlO<sub>x</sub> without damaging the tip. This problem could be circumvented by one of two methods. The easiest would be to find a metal that doesn't react with Al below 450°C, and that also has no native oxide, but so far I have been unable to find such a metal. The more difficult method would be to have two separate chips, or perhaps two widely disparate regions on a single chip, one with SETs and one with contact pads. The two chips could be connected with wirebonds or traces, one per SET. While the SET chip would still be restricted to Al

metallization, the other chip could have Pt or Au contact pads as before.

## 5.8 Summary

In conclusion, I have successfully modified a commercial low temperature STM for use as a tuning fork based scanning force microscope, and by using a metallic tip it acts as a cryogenic scanned probe. Because the instrument incorporates a cryogenic amplifier, it is capable of measuring SETs with at least a 100 kHz bandwidth at millikelvin temperatures. I showed an image of an SET taken with the microscope and Coulomb blockade peaks from an SET measured with the probe at 60 mK. This demonstrates the possibility of using a scanned probe to measure large arrays of nanostructures in a cryostat.

## Chapter 6

### Summary and future directions

#### 6.1 Conclusions

I have presented, analyzed, and begun to pursue one of many imaginable routes toward the electrostatic control of an individual impurity electron in Si. As outlined in Chapter 2, this level of control is an important first step toward evaluating the true feasibility of constructing a quantum computer based on donor arrays in semiconductors, as well as representing an interesting experiment on its own merits as a test of semiconductor physics at the atomic level. I outlined the challenges such an experiment would face, chief among them that of aligning an individual donor with a detector, such as an SET, to sense its ionization. While there are a number of other groups working toward alignment of a donor with an SET, we chose to pursue the measurement using randomly doped samples.

Measuring a single donor with an SET on a randomly doped sample at very low doping raises the issue of how to measure a large enough number of SET/donor combinations to find one properly aligned. I addressed this challenge by constructing a millikelvin scanned probe, described in Chapter 5, capable in principle of measuring hundreds of SETs in an array with low noise and high bandwidth, and I demonstrated the probe's abilities by imaging an SET in an array and measuring its Coulomb blockade. The measurement bandwidth was limited to about 100 kHz with a charge sensitivity of  $2.6 \times 10^{-5} e/\sqrt{\text{Hz}}$  near 10 kHz, limited only by the measurement electronics. This scanned probe was one of the world's first scanning force microscopes operating at millikelvin temperatures.

In Chapter 3 I presented a model to describe the transition of an electron between a donor site and a Si/SiO<sub>2</sub> interface 30 nm above it. At 100 mK the electron is localized

within less than 3 nm from the donor site when there exists no electric field. When an electric field of order 20 kV/cm is applied the electron should move abruptly toward the interface where it should stop, confined to about 3 nm in the direction perpendicular to the interface and to about 15 nm in the direction parallel to the interface. This transition should happen on the timescale of 1 ns or faster. For an SET with an island 50 nm  $\times$  50 nm the associated charge motion should induce a signal 0.15 e, well within the limits of our sensitivity.

There must be a gate to bias the SET to its operating point of maximum charge sensitivity, but changing the voltage on this gate will change the electric field on a nearby donor unless the system is engineered carefully to screen the impurity. In Section 3.2.1 I outlined a good figure of merit to evaluate the screening effectiveness of a given SET/gate geometry. I also presented a novel design consisting of a back gate and SET with wide leads above it that should shield a donor beneath the island from at least 90% of the electric field from the biasing gate. In Chapter 4 I discussed my recipe to fabricate prototype devices of this geometry using ion implantation to create the back gate and an Al SET on the surface. The fabrication incorporates two key ideas. First, it combines e-beam and photolithography into a single Al evaporation step, which allows for subsequent high temperature processing without the formation of intermetallic compounds. Second, Ge is used as the mask for this evaporation instead of the usual PMMA, because it is strong enough to support the fragile, high aspect ratio structures needed to make an SET with wide leads.

In Chapter 4.3.3 I presented the results of several experiments with SETs looking for evidence of charge motion in the underlying Si substrate. I showed how I could track the amount of dc charge accumulated on an SET island of traditional design by using a feedback circuit connected to a gate above the substrate. Applying an electric field near the SET, I compared the amount of charge moving in three different substrates: one free of dopants, one implanted with P at the  $10^{11}$  /cm<sup>2</sup> level, and one implanted at  $10^{12}$  /cm<sup>2</sup>.

While I saw little difference in the behavior of the first two substrates, the  $10^{12}$  /cm<sup>2</sup> substrate showed a significantly larger induced charge than the others, which difference I attribute to donors ionizing under the applied electric field. Using an ac electric field and lock-in detection I found resonances that I attribute to individual electrons. I was not able to identify signals due to the ionization of single donors, however, presumably because the doping density was high enough in this case to form a nearly conduction region.

I then gave results from SETs built to my new design incorporating wide leads on two different substrates. By measuring the density of Coulomb blockade peaks I was able to show a direct correspondence between CV measurements made on a large capacitor and CV measurements made with an SET. I was also able to gate the SET with a planar gate above the surface and found good agreement between experiment and a parallel plate model for the capacitance in this case. These results proved that the SET was sensitive to the charge configuration in the substrate and that the overall electrostatics of the device were well understood. Again using a lock-in technique, I observed greater noise by a factor of 3 in an SET fabricated above an area implanted with P at  $10^{12}$  /cm<sup>2</sup> compared with one above an area without any P implant, but as in the results from the traditional SETs I could not distinguish an effect from a P implant at  $10^{11}$  /cm<sup>2</sup>.

By carefully initializing the sample in a nearly identical state each time I was able to take a series of data tracking the position of several charge fluctuators in four SETs as a function of the charge residing at the Si/SiO<sub>2</sub> interface. I also tracked the fluctuators as a function of voltage on the SET biasing gate and studied their behavior with different driving amplitudes. The data conclusively eliminated the Si substrate as the source of these fluctuators. Instead, the data suggested that something on the surface was responsible. My best guess is that the charge motion was due to electrons shuttling onto and off of isolated Al grains near the SET island. This theory could be tested by shrinking or eliminating these grains, perhaps by cooling the sample stage during the Al evaporation.

## 6.2 Problems and future directions

Despite the successes outlined above, observing the motion of individual dopant charges still faces some real challenges. Although a large array of SETs could in principle be measured with the scanned probe I designed, there were unresolved problems with making low resistance contacts between the probe tip and the SET pads. I suspect these arose from residual frozen contamination or water on the pad surfaces that remained, even under high vacuum conditions. There were also serious problems with the coarse motion capability required to move between devices in the array, and it was difficult to image the sample quickly enough without damaging the SETs.

I believe a much simpler way to measure many SETs would be to design an electrical multiplexing circuit to connect a given SET to the cryogenic transimpedance amplifier. This multiplexer could be placed on a different nearby chip to which the SETs were connected with wirebonds, or if it were composed of Si MOSFET's it could be placed directly on chip and connected to the SETs with metallic interconnects.

There are conflicting requirements for the density of implanted donors. On one hand we need a reasonable density of donors to ensure that some sizable fraction of SETs will lie properly aligned above an impurity. For example, at a doping density of  $10^{11}$  /cm<sup>2</sup>, my wide lead SETs (island dimensions 50 nm  $\times$  50 nm) have on average 2.5 donors beneath each island. Furthermore, I never characterized the true density of defects at my Si/SiO<sub>2</sub> interface, although the value could easily be as high as  $10^{11}$  /cm<sup>2</sup>. Both of these considerations kept me from reducing the implant density much.

On the other hand, the lateral size of the wave function (see Figure 3.8) is 15 nm (for an electron at the interface above an ionized donor 30 nm away). To really be confident that there is no overlap between adjacent donor electrons at the interface would require a nearest neighbor separation much greater than 15 nm, say at least 30 nm, corresponding to an implant density less than  $10^{11}$  /cm<sup>2</sup>. Clearly, the experiment is walking

a fine line between forming a 2DEG at the interface and not having enough donors to measure. While we could decrease the implant density while increasing the SET island area to compensate, this has the disadvantages that the SET charge sensitivity scales inversely with island dimensions and that we will not be able to simultaneously decrease the interface defect density.

While it clearly seemed a good idea when we first tried it, I now believe that creating the donor gating structure via ion implantation was a mistake, because it introduced too many other impurities and defects into the vicinity of the donors. When using this structure as a gate there was a huge amount of hysteresis due to the long tail of the acceptor distribution all the way up to the wafer surface. Figure 4.22 makes this clear, as it shows that we never operated the back gate in a regime where the acceptor tail was fully depleted. There were also problems with unanticipated leakage at higher voltages (see Figure 4.24 and accompanying text). While a back gate is attractive because it shields the donors and makes the electrostatics easier to understand, it will only work well if the transition from metallic conduction to intrinsic Si is made *much* sharper, a goal that will be difficult to achieve via doping. On the other hand, traditional SETs with a side gate on the surface, which provide a very sharp transition from metallic to insulating regions, do not effectively shield charges underneath, and more importantly they don't provide any mechanism for fixing the Fermi level in the substrate. We must have a way to fix the Fermi level at the interface to ensure that the donors there are occupied.

The combination of a wide lead SET, Schottky gates on the surface, and metalization on the back of the wafer, rather than just a nearby doped back gate, may provide a good compromise: shielding can be achieved with such a geometry through careful design, and a Schottky contact should provide a channel for the addition and subtraction of carriers from the system, yet it should be abrupt enough to avoid the problems of hysteresis present with a doped gate. However, care must be taken to avoid leakage when using a Schottky gate. Furthermore, the electric field in the  $x$ - $y$  plane must not be too great, or the

donor electron, once ionized, will escape. For a donor at a depth of 30 nm, the interface electron is bound by an electric field  $\sim 0.5$  kV/cm at a radius of 15 nm. It will probably be necessary to keep the field components in  $x$  and  $y$  significantly smaller than this.

In addition, it will most likely be necessary to mask the P implant further, restricting the implant to a small region beneath the SET island. If this is not done, there will be a large number of donors between the gate and island of the SET that ionize before the donor that lies directly beneath the island. If there are enough of these they may form a 2DEG at the surface, and again it will not be possible to treat each donor as an isolated system.

I also have not shown experimentally that our new device geometry will shield a donor from the gate. While the FEMLAB simulations from Chapter 3 and data from Chapter 4.3.3 support the notion that it should do just that, we have not shown it with a direct measurement. In fact I've seen just the opposite; for those signals that I attribute to single electrons in Figures 4.19 and 4.31 the shielding is a factor of at least three or four worse than predicted. Furthermore the gate acts in a direction opposite what would be expected for a donor underneath the island. Both observations support my conclusion that the signals do not come from donor electrons. We will not be able to experimentally verify that the shielded design behaves as expected without identifying some signal as coming from charges beneath the SET island. Another route toward shielding substrate charges from the effects of the biasing gate could be to significantly increase its coupling to the SET island while not changing its coupling to charges below. This could be achieved via a gate made to overlap with the island but separated from it by a thin, strong and insulating dielectric.

Despite the difficulties outlined above, I still firmly believe that measuring the spin of a donor using an SET on the surface is possible. Each of the problems can be addressed with current technology. To eliminate electronic wave function overlap at the interface will probably require an implant density around  $10^{10}$  /cm<sup>2</sup>. Let me discuss how to solve

the issues in this case.

If the SiO<sub>2</sub> trap density were reduced below 10<sup>10</sup> /cm<sup>2</sup>, then we could reduce the P implant density to 10<sup>10</sup> /cm<sup>2</sup> without traps capturing a significant fraction of donor electrons. Achieving such a trap density is definitely possible.[36] It would also be important to characterize the density of unwanted impurities near the Si/SiO<sub>2</sub> interface, especially impurities that may be introduced during oxidation. A P implant density of 10<sup>10</sup> /cm<sup>2</sup> corresponds to a bulk density of 2 × 10<sup>15</sup> /cm<sup>3</sup> (see Figure 4.4). The background impurity density should be kept well below this value. However, Si wafers are available commercially with background densities < 10<sup>13</sup> /cm<sup>3</sup>, so this problem reduces to ensuring an extremely clean thermal oxide growth.

With an implant density of 10<sup>10</sup> /cm<sup>2</sup> there would be a P donor beneath only one in four SETs. Measurement of at least 10 and perhaps 100 devices would then be required for reasonable statistics, so that an SET multiplexing capability would become important. I have already mentioned at least one multiplexing technology (a cryogenic MOSFET multiplexer) that could enable measurement of 100 devices. Alternative technologies include a scanned probe or frequency multiplexed rf-SETs.

Regardless of the implant density, it will be necessary to reliably establish a given electric field at a donor site beneath the SET. This should be possible with Schottky gates. Lastly, masking the P implant to a narrow region beneath the SETs will be difficult, but certainly possible using e-beam lithography and careful alignment.

An immediate priority should be to establish the quality of my thermal oxides and the purity of the Si beneath them. The next priority should be an experiment that establishes the flat band condition under an SET with Schottky gates, because the electric field there cannot be determined without knowledge of this unique zero point. This data point will in turn enable future experiments to concentrate on a greatly reduced range of gate potentials, i.e. only those that are near the flat band condition. Flat band determination can only be made by placing a large number of free electrons at the Si/SiO<sub>2</sub> interface and

then depleting them until they are gone; this depletion can be measured with the SET. Such an experiment was difficult to do with gates only on the oxide surface, as I had in my earliest design, because in this configuration there is a hole created for every electron during sample illumination, and keeping these oppositely charged carriers well separated is a challenge. It was also difficult to do with the implanted back gate, because the long tail of impurities in these substrates washed out the flat band transition.

The next priority should be to study the Coulomb blockade peak spacing between flat band and about 50 kV/cm, even without any doping in the substrate. Any variation in the peak spacing with gate voltage, whether uniform or random, would be interesting physics by itself, and there have been a number of theoretical studies on the expected statistical distribution of these peak spacings. Variations in peak spacing would also tell us about unknown charges moving in the sample, charges that we will need to understand before we search for signatures of donor ionization. Only when these two experiments have been well characterized would it make sense to implant a sample with donors for comparison. At that point it would also make sense to consider alternative SET multiplexing technologies, and to investigate techniques for masking the P implant to a smaller region beneath the SET.

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