ABSTRACT

Title of Document: CHARACTERIAZTION OF ELECTRICALLY ACTIVE DEFECTS IN ADVANCED GATE DIELECTRICS

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As the gate oxide thickness of the metal-oxide-semiconductor (MOS) Field Effect Transistor (FET) is continuously scaled down with lateral device dimensions, the gate leakage current during operation increases exponentially. This increase in leakage current raises concerns regarding device reliability. Substitute dielectrics with high dielectric constant (high-k) have been proposed to replace traditional SiO_2 to reduce the leakage current in future devices. However, these high-k dielectrics also have reliability issues due to the large amount of intrinsic trapping centers.

In this work, electrically active defects generated during electrical stress of ultrathin SiO_2 dielectrics are characterized and studied. The mechanism of oxide breakdown is studied by investigating the contributions of hot holes to device time-to-breakdown (t_{bd}). The proper extrapolation of t_{bd} from accelerated testing conditions to normal device operating conditions is also studied. The factors that affect this extrapolation are discussed. Another important device reliability parameter, threshold

voltage shift (ΔV_{th}), is also investigated in this work. The dominant mechanisms causing this shift is studied using both simulation and experimental results.

The current primary reliability issue with high-k dielectrics is the large amount of intrinsic traps located in the dielectric stack. Therefore, the electrical characterization of high-k dielectrics in this work is focused on these initial as-fabricated trapping centers. A methodology based on 2-level charge pumping (CP) measurements at different frequencies is used to study the spatial profile of these trapping centers. The correlation between device fabrication data and measurement results indicates this methodology is accurate and reliable.

CHARACTERIZATION OF ELECTRICALLY ACTIVE DEFECTS IN ADVANCED GATE DIELECTRICS

By

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Table of Contents

List of Figures

Chapter 1

Introduction

1.1 Introduction

Ever since the first transistor was introduced by Shockley and Pearson in 1948 [1], the device with metal, oxide and semiconductor stacked structure has dramatically affected and changed the world. Today, the Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) is the basic building block of modern integrated circuits and can be found everywhere from kitchen appliances to the space shuttle. The remarkable capability of the MOSFET comes from the voltage-modulated conductance of the semiconductor surface underneath the oxide layer. When a gate voltage is applied to the metal layer (or highly doped poly-silicon layer), minority carriers from the source and the drain are either accumulated or depleted at the semiconductor surface. This drives the device into the “on” and “off” states, accordingly. The key issue of this voltage-controlled characteristic of the MOSFET is attributed to the existence of the oxide layer sandwiched between the metal and the semiconductor layers. The oxide layer serves as an insulation layer by blocking the current between the gate electrode and the semiconductor when mobile carriers are accumulated at the semiconductor layer surface.

Silicon dioxide (SiO_2) has been used as this insulation material for more than three decades [2]. The success of the Si-SiO_2 system is because of the unique features of SiO_2 such as high band gap energy, high thermal stability, and the excellent compatibility with the Complementary MOS (CMOS) technology. Furthermore, the high quality interface between the thermally grown SiO_2 and Si substrate makes the Si-SiO_2 system possess relatively high electron and hole mobilities and low interface states. These outstanding properties make the Si-SiO_2 system irreplaceable in the past decades.

Because of the improvement of process integration technology, the device density of integrated circuits has doubled for approximately every two years, according to Moore's Law [3]. As shown in Figure 1.1, Intel has predicted that the number of transistors per integrated circuit will reach one billion by the year 2005 [4]. As the device density of the integrated circuits increases, all of the device dimensions are scaled downward. As device dimensions are scaled, the operating voltage, V_{DD}, is also scaled by the same factor as the device dimensions. The substrate doping density must then be increased in order to reduce short-channel effects. To keep the driving current for proper circuit operation, the gate oxide capacitance (C_{ox}) must be increased [5]. Historically, this has been accomplished through a reduction of the gate oxide thickness (t_{ox}) [5, 6]. The 2004 International Technology Roadmap for Semiconductors (ITRS) predicts that the equivalent gate dielectric thickness will be reduced to approximately 7 Å by 2010, as shown in Figure 1.2 [7].

With the scaling of t_{ox}, SiO_2 will no longer be able to block leakage current effectively. The exponentially increasing gate leakage current with decreasing t_{ox} has been considered as the essential factor limiting the future scaling of t_{ox}. The gate leakage current will increase the device standby power consumption [8] and also affect the circuit performance [9]. For $t_{ox} \leq 4$ nm, it is found that the gate leakage current increases by approximately one order of magnitude for every 0.2-0.3 nm of oxide thickness reduction [10], as shown in Figure 1.3. The maximum tolerable gate leakage current is suggested to be between 1 (A/cm^2) and 10 (A/cm^2), which correspond to an oxide thickness between 1.2 and 1.5 nm [11-13].

The gate leakage current not only causes a power dissipation problem, but also raises concerns regarding the reliability of the gate oxide. It is known that electrically active defects are generated when electrons or holes tunnel through the gate oxide [6,9-12]. These defects cause shifts in V_{th} and degrade the channel carrier mobility impacting the device performance. When the generated defects reach a critical amount, they cause the gate oxide to breakdown. Although the reliability of ultra-thin SiO_2 has been heavily studied, the exact physical mechanisms of defect generation of breakdown are still unknown.

To reduce the large gate leakage with the scaling oxide thickness, substitute materials with high dielectric constant (high-k), such as Al_2O_3, HfO_2 and ZrO_2, have been proposed to replace SiO_2 [14-22]. The principle of replacing SiO_2 with these high-k materials is to keep C_{ox} the same while permitting a physically thicker dielectric. C_{ox} for SiO_2 and high-k materials can be expressed as

$$C_{ox} = \frac{\varepsilon_{SiO_2}\varepsilon_0}{t_{SiO_2}} = \frac{\varepsilon_k \varepsilon_0}{t_k} \cdots\cdots\cdots\cdots\cdots\cdots (1.1)$$

where ε_0 is the vacuum dielectric constant, ε_{SiO_2} and ε_k are the relative dielectric constants for SiO_2 and high-k dielectrics respectively, while t_{SiO_2} and t_k represent the physical thickness of SiO_2 and high-k dielectrics respectively. In order to compare high-k dielectrics with SiO_2, equivalent oxide thickness (EOT) is defined for high-k dielectrics as the equivalent thickness of SiO_2 which results in the same capacitance as the high-k. From equation (1.1) it is easy to show that EOT can be expressed as

$$EOT = t_{SiO_2} = \frac{\varepsilon_{SiO_2}}{\varepsilon_k} t_k \cdots\cdots\cdots\cdots\cdots\cdots (1.2)$$

Since the typical value for ε_k is between 10 and 25, which is larger than ε_{SiO_2} (=3.9), the physical thickness of high-k dielectrics can be relatively thicker (~ 3 nm) while keeping EOT as small as 1 nm. Because the physical thickness of high-k materials is much thicker than SiO_2 for a given capacitance, the tunneling current is expected to be reduced significantly for high-k gate dielectrics [23, 24]. Figure 1.4 shows the comparison of the gate leakage current density (J_g) between SiO_2 and HfO_2 gates at different EOT. It is obvious that J_g is reduced significantly for the HfO_2 gate dielectric as compared to SiO_2.

The search of proper high-k dielectrics to replace SiO_2 has proven to be extremely challenging. Problems associated with these dielectrics include thermal instability on silicon, instability with gate electrode materials, large tunneling currents, and lower than expected dielectric constants of the deposited films. Furthermore, unlike the Si-SiO_2 system which shows a high quality interface with low interface state density and high channel carrier mobilities, the Si-high-k system generally has large interface state density and low channel carrier mobilities. [25-30].

To obtain a high quality interface with Si substrate while using a substitute high-k gate dielectric, a SiO_2-like interfacial layer can be grown before the high-k dielectric is deposited. This interfacial layer provides a transition region from the Si substrate to the substitute high-k dielectrics and is required to form high quality interfaces with both Si substrate and high-k dielectrics. This high-k and interfacial layer stacked gate structure makes the high-k dielectric system even more complicated to characterize.

There has been a lot of recent research related to high-k dielectrics [14-22]. The main issue related to the high-k gate dielectrics themselves is the large amount of fixed charges and charge trapping centers compared with SiO_2 [31]. The charge trapping centers are believed to exist at the interface with gate electrode [32], the interface with SiO_2-like interfacial layer [33] and inside the bulk dielectric. These trapping centers and intrinsic charge defects make high-k dielectrics much more complicated than the traditional SiO_2 gate dielectric.

1.2 Purpose and Approach

The overall goal of the research presented in this thesis is to provide detailed electrical characterization and fundamental understanding of electrically active defects in advanced gate dielectrics, including the traditional ultrathin SiO_2 and HfO_2 dielectrics. The detailed approach to achieve this goal is described in the following.

The initial work involved the study of MOSFETs with ultrathin SiO_2. Since SiO_2 is relatively free of initial defects, the focus was on defect generation mechanisms. Proposed mechanisms of defect generation and oxide breakdown from the literature were studied by injecting different carriers (electrons and holes) during stress. The behavior of the time-to-breakdown (t_{bd}) and charge-to-breakdown (Q_{bd}) of the devices was used to compare and eliminate less likely mechanisms. Attention was then turned to the relation between the defect generation and the injected charges by using an interrupted-stress method. The understanding of how to perform proper extrapolation and the correct interpretation of the data from electrical characterization results was the focus of this study.

The understanding and characterization methodologies developed in ultrathin SiO_2 were then applied to MOSFETs with HfO_2 gate dielectrics. Since the main problem associated with HfO_2 is the relatively large amount of initial defects, the focus of this research was to understand how to properly characterize these initial defects. The initial defect characterization was conducted through measurements of the spatial as well as the energy distributions of defects in HfO_2 using charge-pumping. By changing the measurement conditions, defects at different energies and depths in HfO_2 can be characterized.

1.3 Preview of Thesis

This thesis is organized into seven chapters.

Chapter 2 provides background information for the rest of the thesis. It starts with the introduction of the percolation theory that connects the microscopic defect generation to the macroscopic gate oxide degradation phenomena and the eventual breakdown. The three major models proposed in the literature to explain defect generation mechanisms are then introduced. The success and controversies of these models are discussed in detail. The statistics of breakdown is then introduced followed by the description of the electrical characterization techniques such as stress induced leakage current (SILC) and charge-pumping (CP) measurements that are used to monitor the dynamic defect generation during a stress.

Chapter 3 describes my research on possible defect generation models for SiO_2 by studying the effect of injected substrate hot holes on defect generation and t_{bd}. It is found that pre-injected substrate hot holes have no effect on the t_{bd} for the subsequent constant voltage stress (CVS). The results suggest that holes are not responsible for defect generation and breakdown during CVS. The results also suggest that different types of defects may be generated during the CVS as compared to substrate hot hole injection.

Chapter 4 describes defect generation mechanisms in SiO_2 by inspecting defect generation as a function of injected charges. A non-linear relationship between the generated defects and the injected charges are revealed. This non-linear relationship raises the concern of extrapolating the t_{bd} from stress conditions (high voltage) to device normal operating conditions (low voltage) correctly. The possible mechanisms that cause this non-linear relationship are also investigated and it is found that the changes of carrier capture cross sections during stresses can not explain this non-linear relationship.

Chapter 5 investigates the dominant mechanism that causes the threshold voltage (V_{th}) shifts in n- and p-channel MOSFETs. The results suggest that mobility degradation can be an important component of threshold voltage shift. The results suggest that proposed oxide degradation models based on the I_d-V_g measurements of V_{th} may not be accurate.

In Chapter 6, the focus is changed to the HfO_2 gated MOSFET. The spatial and energy distributions of the initial defects in HfO_2 are characterized by using CP. The fraction of defects probed by CP at a given energy and depth within the dielectric is simulated. By changing CP measurement conditions, the spatial and energy profiles of defects in HfO_2 can be characterized. The simulation results are compared with experimental data to extract the initial defect distribution in the HfO_2 dielectric.

Finally, Chapter 7 provides the summary of this thesis and some possible future work.

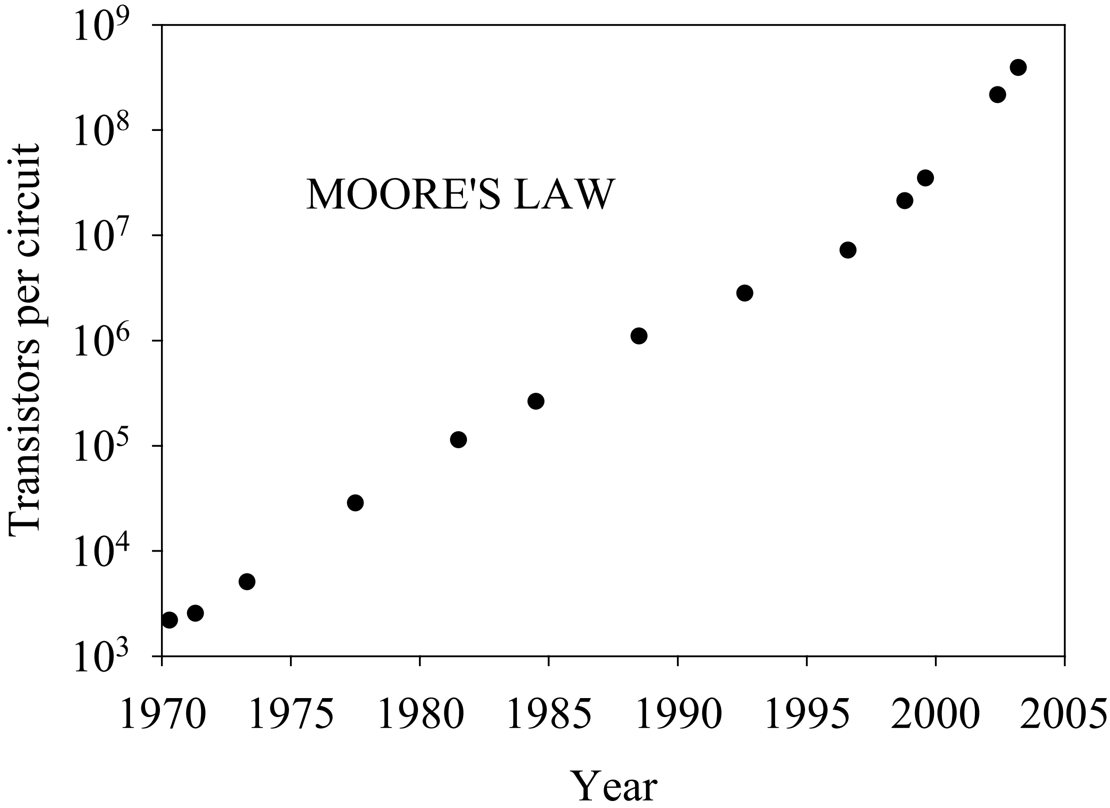

Figure 1.1 The extension of Moore's law made by Intel. It is predicted that the number of transistors per integrated circuit will reach one billion by the year 2005 [4].

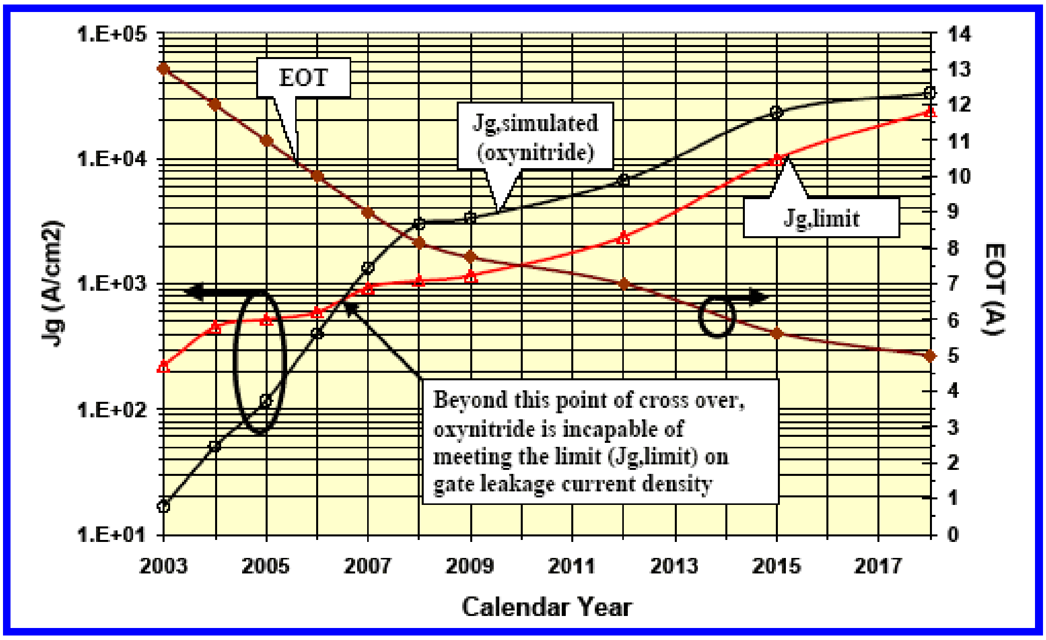

Figure 1.2 A plot from the 2004 ITRS showing future projected EOT and limit of gate leakage current density [10].

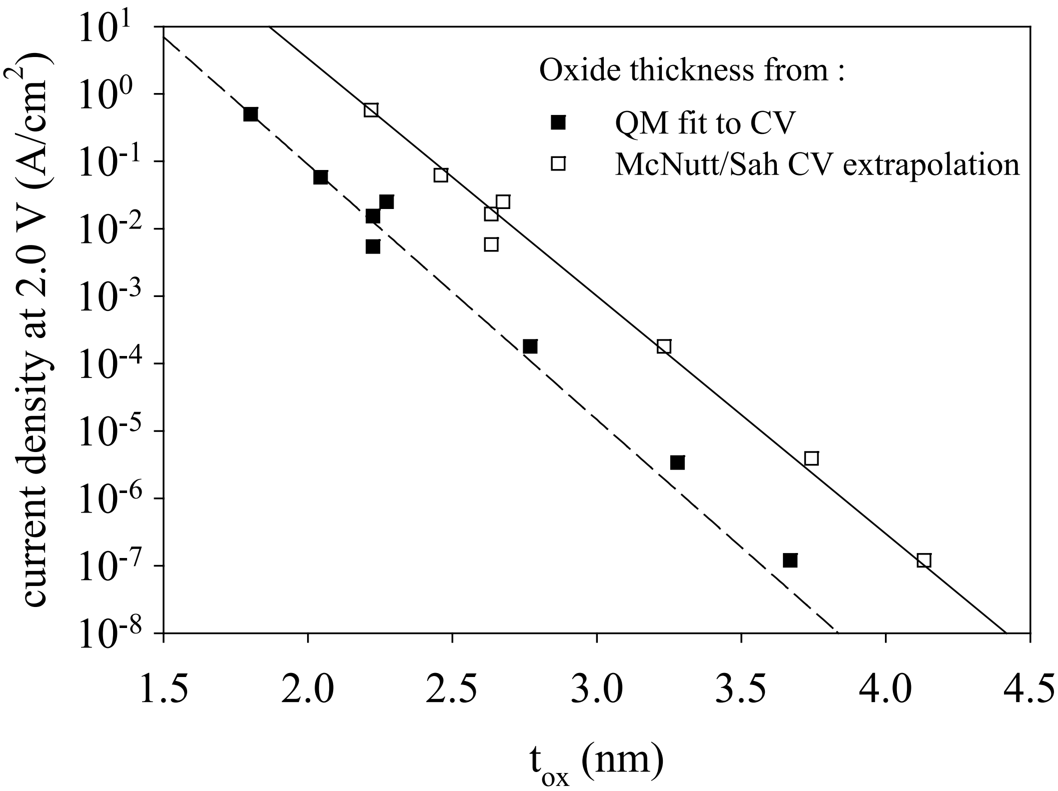

Figure 1.3 The gate tunneling current for SiO_2 with $t_{ox} \leq$ 4nm. The tunneling current increases exponentially with reducing oxide thickness [13].

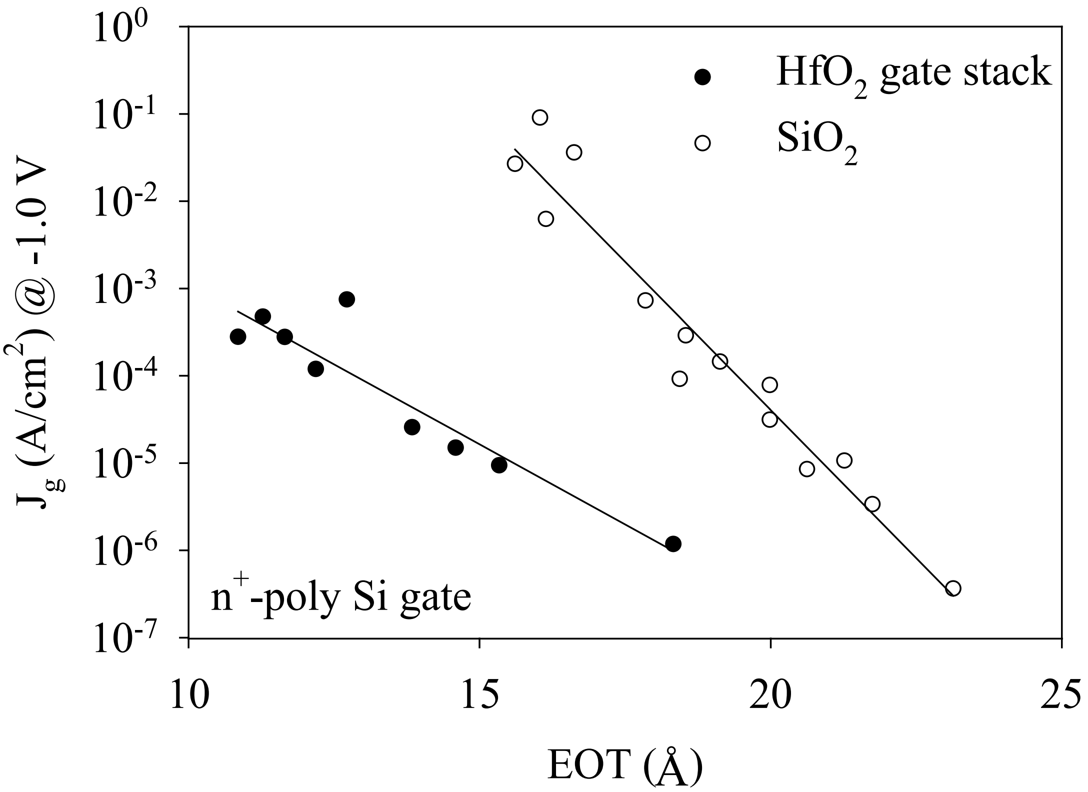

Figure 1.4 The comparison of gate leakage current density between SiO_2 and HfO_2 gates at different EOT. The leakage current is significantly reduced for HfO2 gate dielectrics when EOT is reduced [26].

Chapter 2

Background

2.1 Overview

The goal of this chapter is to provide the background that will be helpful to read the rest of this thesis. Macroscopic gate oxide degradation phenomena and eventual breakdown are first explained through percolation theory. The three major proposed empirical models for defect generation are discussed in detail, including the success and controversies of these models. The statistics of breakdown and electrical characterization techniques such as stress induced leakage current (SILC) and charge pumping (CP) will then be introduced.

2.2 Percolation Theory

Gate oxide degradation and eventual breakdown are due to the generation of defects during stresses. To explain how electrical defects cause oxide breakdown, Degraeve proposed the percolation theory in 1995 [34]. It suggests that electrical defects are generated randomly in the gate oxide during a stress, as the open circles schematically depict in Figure 2.1. The energy levels of these defects are located within the silicon band gap and thus provide additional intermediate tunneling paths for electrons and holes. These tunneling paths degrade the oxide insulation ability and increase gate leakage current. As the defects are continuously generated, they have a chance to connect to each other electrically and form a conducting path. Once the conducting path connects the poly-Si gate to the Silicon substrate (as the shaded circles show in Figure 2.1), an electrical short across the oxide is found. This conducting path surges a large current that causes permanent structural breakdown of the oxide.

Percolation theory successfully explains how the defects degrade and cause eventual oxide breakdown. The number of defects at breakdown (N_{BD}) and the effective defect size (or the effective number of defects that causes the breakdown) can also be calculated by fitting this theory with experimental data [34-36]. The theory also successfully explains the dependence of N_{BD} on oxide thickness and area. However, percolation theory does not explain how these defects are generated.

2.3 Defect Generation Models

To explain how the defects described in percolation theory are generated, several physical models have been proposed in the literature. Three major proposed models, the thermo-chemical electric field model, the anode hole injection (AHI) model and the hydrogen release (HR) model, will be introduced in the following sections.

2.3.1 Thermo-Chemical Electrical Field Model

The thermo-chemical electric field model was developed based on the observation of t_{bd} as a function of electrical field [37-39]. It suggests that defects are generated due to the interaction between the electric field and the oxide lattice [40]. When an electric field is applied across the SiO_2 layer, it interacts with the weak Si-Si bonds associated with oxygen vacancies in the SiO_2 layer. The applied electric field eventually breaks the weak bonds and creates permanent defects which lead to breakdown [41, 42]. This electric field driven model is no longer accepted as recent studies conclusively showed that defect generation is related to electron fluence and cannot be explained by the interaction of the SiO_2 lattice with electrical field [43-46].

2.3.2 Anode Hole Injection Model

The Anode Hole Injection (AHI) model suggests that hot holes are generated at the anode due to energetic electrons injected from the cathode. These holes can then tunnel back into the oxide and generate defects that cause gate oxide degradation [47-49]. Figure 2.2 shows illustratively the processes of the energetic tunneling electron, the anode hole generation, and the anode hole injection for an n-channel MOSFET. The oxide breakdown happens when a critical hole fluence (Q_p) is reached [50]. The AHI model was later modified to include anode holes generated through minority ionization, which makes the anode hole generation possible at the low gate bias condition [51, 52].

The AHI model is based on experimental observations of thicker oxides that the number of defects generated in the gate oxide is uniquely correlated to the anode hole fluence, independent of the gate stress voltage and the oxide thickness [50]. The hole fluence is assumed to be equal to the measured substrate current which is proportional to the gate current during stress [53]. The AHI model can also explain the polarity dependence observed from both n-channel and p-channel devices stressed at opposite polarity bias conditions [54-56]. This model is supported by the observation that Q_p is independent of the gate stress voltage (V_G) and t_{ox} [53]. The AHI model also shows that the voltage acceleration factor (γ), which is defined as the negative derivative of the logarithm of t_{bd} respect to the stress voltage ($-\partial \ln t_{bd} / \partial V$), should increase with decreasing gate voltage, as observed from experiment [57].

Nevertheless, the AHI model is challenged by other observations. First, Q_p is found not to be a constant for low electron injection conditions [58]. It is also found that Q_p decreases with the decreasing oxide thickness [49], and shows a temperature dependence [59, 60]. Furthermore, physical mechanisms other than anode hole injection can also contribute to the measured substrate current [61, 62]. Other observations also indicate that even though the injected anode holes are efficient in generating electrical defects, these defects are inefficient in causing oxide breakdown [60].

2.3.3 Hydrogen Release Model

The other model that tries to explain defect generation is the hydrogen release (HR) model. The HR model is similar to the AHI model but suggests that hydrogen species are generated at the anode by energetic electrons and do damage when they drift or diffuse into the gate oxide [60]. It is suggested that atomic hydrogen can attack Si-O bonds and cause the damage. Hot electrons can also break Si-H bonds, which are believed to be one of the sources of oxide degradation [57, 63, 64]. It is also found that the voltage dependence of the H atom desorption rate from the silicon surface is similar to the voltage dependence of the defect generation rate (P_g) in the gate oxide [65]. The HR model can also possibly explain the large exponent value (n~ 44) in the t_{bd} power law dependence of the stress voltage [65-67].

The HR model has been questioned because some results suggest that Q_{bd} is not improved if the deuterium is used to passivate the Si-SiO_2 interface [68], as shown in Figure 2.3. It has been reported that deuterated oxide films have suppressed hydrogen desorption from the Si interface and, therefore, improved the immunity to the interfacial trap generation during channel hot carrier injection [69]. Nevertheless, it is also reported from other groups that deuterated oxide does improve device reliability [70, 71]. Therefore, the debate remains.

2.4 Statistics and Characterization Techniques

Percolation theory explains the oxide degradation process in terms of the defect generation from a microscopic point of view. To study how defects are generated, however, we can only rely on either observed statistical phenomenon or macroscopic electrical characteristics to correctly analyze the experimental data and link them to the defect generation mechanism. To analyze statistical phenomenon such as time-to-breakdown (t_{bd}) (also known as time-dependent-dielectric-breakdown TDDB) and charge-to-breakdown ($Q_{bd} \approx t_{bd} \bullet J_g$, where J_g is the current density during a stress), proper statistics is necessary; while for characterizing electrical properties such as interface state density (N_{it}) generation and gate tunneling current increase, electrical characterization techniques are needed. In the following sections, available statistics and electrical characterization techniques that are used to study the defect generation mechanisms from different aspects will be introduced separately.

2.5 Weibull Statistics

Percolation theory proposes that the formation of an electrical conducting path triggers oxide breakdown. However, since the formation of a percolation path is a random process, N_{BD} (or macroscopically, Q_{bd} and t_{bd}) for different devices can vary by orders of magnitude. Therefore, statistics is required to describe the failure distribution and define N_{BD} as well as t_{bd} quantitatively.

Consider a system with N identical devices under the same electrical stress condition. The total number of failed devices at any given time can be defined as $N_f(t)$ and the ratio of $N_f(t)$ to N is defined as the cumulative distribution function (CDF), F(t). Figure 2.4 (a) shows the general behavior of F(t). It is noticed that F(t) is zero initially and goes to one when time approaches to infinity. The counterpart function of F(t) is the reliability function R(t), which is defined as R(t) ≡ 1-F(t), as shown in Figure 2.4 (b). Meanwhile, R(t) can also be mathematically expressed as

$$R(t) = e^{-\left(\frac{t}{\theta}\right)^{\beta}} \quad \cdots\cdots\cdots\cdots\cdots (2.1)$$

where β is called the shape parameter and θ is called the scale parameter [72].

By using the definition of R(t) and equation 2.1, the following expression can be derived,

$$\ln(-\ln(1-F(t))) = \beta \ln(\tfrac{t}{\theta}) \quad \cdots\cdots\cdots\cdots (2.2)$$

where ln(-ln(1-F(t))) is the Weibull distribution function. By plotting the Weibull distribution function with respect to the natural logarithm of the t_{bd} of the N devices, the slope of the curve is equal to β. The scale parameter θ, which corresponds to 63% of the failure, is the modal value of the t_{bd} of the N devices and can be defined as the t_{bd} of this N-device system, as shown in Figure 2.5. Similarly, the functions F(t) and R(t) could be defined as functions of stress injected charge instead of stress time and the Weibull distribution for Q_{bd} can then be obtained.

The β value of the Weibull distribution indicates the spread of the t_{bd} distribution. It is found that oxide breakdown caused by extrinsic defects (non-stress related) and intrinsic defects (stress related) would result in different β values [73]. Therefore, it is possible that β value can be used to identify different defect species generated by stress. On the other hand, the modal value of t_{bd} from the Weibull distribution is directly affected by the stress conditions. Therefore, by comparing the β value and the modal value of t_{bd}, the effect of gate oxide fabrication process and applied stress conditions on breakdown can be revealed.

Historically, the lognormal distribution [78] has also been used to fit experimental data to describe t_{bd} distribution. However, recent reports have indicated that that Weibull distribution can better fit t_{bd} data for large number of samples. This permits more accurate extrapolation of t_{bd} to low percentile values [74, 75, 79-81], as shown in Figure 2.6.

2.6 Characterization Techniques

Another strategy for studying defect generation mechanisms is characterizing electrically active defects during a stress. To achieve this goal, it is required to interrupt a stress periodically and perform electrical measurements. These results can then be linked to microscopic defect generation. This interrupted-stress strategy can reveal the relation between stress-induced defects and stress time (or injected electrons and/or holes). The most basic requirement of this strategy is that no further defects are generated during the measurement. Therefore, available measurement techniques must be carefully chosen and measurement conditions should be optimized.

Two techniques commonly used to electrically characterize gate oxide reliability are charge pumping (CP) measurements [83-90] and stress induced leakage current (SILC) [91-95] measurements. The relative change of maximum CP current (I_{CP}) is used to monitor the interface state density at Si-SiO_2 interface [83-85] and the SILC is used to measure the bulk oxide defect density [91-93].

2.6.1 SILC Measurement

During SILC measurements, a sense voltage (V_{sense}) is applied to the gate while all the other terminals of an MOSFET or a capacitor are grounded. V_{sense} should be smaller than the stress voltage to avoid any further stress during the measurement [91]. The gate leakage current measured during SILC measurement is thought to be the electrical conducting path due to the generation of neutral-defect sites [96] or oxygen vacancies [92] inside the bulk oxide. It has been suggested that SILC can be described using the following equation [95],

$$J_G = q\, N_{TS} \frac{c_L\, c_R\, (f_L - f_R)}{c_R\, f_L + c_L\, f_R} \cdots\cdots\cdots\cdots\cdots\cdots (2.3)$$

where J_G is the SILC, N_{TS} is the defect concentration, c_L and c_R are the defect capture rates at the cathode and anode respectively, and f_L and f_R are the Fermi distributions at the cathode and anode respectively. Therefore, by measuring the change of the SILC between successive stresses, the defect generation inside the bulk oxide due to a stress can be explored.

2.6.2 Charge Pumping Measurement

The experimental setup for CP is shown in Figure 2.7 [86]. A periodic ac pumping signal is applied to the gate, and the source and drain are either applied a small reverse bias or grounded. The substrate is also grounded and a dc CP current is measured from the substrate [85]. When performing the CP measurement a trapezoidal wave with the fixed amplitude (ΔV_A) and frequency, which is widely chosen as the pumping signal, is applied to the gate. During the measurement, the lower output voltage level of the trapezoidal wave (V_{base}) as well as the upper output voltage level of the trapezoidal wave (V_{top}) is ramped up, as shown in Figure 2.8. Figure 2.8 shows the typical measured CP current (I_{CP}) for a n-channel MOSFET as a function of V_{base}. The relative position of the gate pumping signal voltage level with respect to the device flat-band voltage (V_{FB}) and threshold voltage (V_{th}) is also shown in the figure and five different characteristic regions can be distinguished during the voltage ramp-up.

In region 1, where V_{top} ($V_{top} = V_{base} + \Delta V_A$) is higher than V_{th} while V_{base} is lower than V_{FB}, a significant dc current from the substrate due to the electron and hole recombination is measured and is denoted as $I_{CP,MAX}$ [83, 84]. This recombination happens because the device was in the accumulation state initially when the voltage applied to the gate was equal to V_{base}, which is lower than V_{FB}. All the interface states are occupied by holes at this moment. When the pulse passes through, the voltage applied to the gate switches to V_{top}. Since V_{top} is higher than V_{th}, the device is turned into the inversion state instantly. Electrons from the source and drain flush into the channel region and fill the interface states while holes are expelled from the channel area. For the holes occupying the interface states, however, they are “trapped” and cannot move back to the substrate during the short transition of the states. As a result, they are recombined with the electrons.

Similarly, after the pulse passed by the voltage applied to the gate came back to V_{base} again and the device went back to the accumulation state with holes refilling the channel region. However, since the electrons trapped the at interface states cannot move back to source or drain so quickly, they are recombined with the holes. These two recombination currents from interface states contribute to the measured dc $I_{CP,MAX}$ [83-85].

In region 2, since both of the V_{base} and V_{top} are lower than the V_{FB}, the interface states are always filled with holes. In region 3, when V_{base} and V_{top} are both higher than the V_{th}, the interface states are always filled with electrons. As a result, no recombination happens in these two regions and the charge pumping current is zero.

The equation for $I_{CP,MAX}$ in terms of interface state density is [90]:

$$I_{CP,MAX} = q\, N_{it}\, f\, A_G \cdots\cdots\cdots\cdots\cdots\cdots(2.4)$$

where,

$I_{CP,MAX}$	is the maximum charge pumping (Amp),
q	is the electron charge (Coul),
N_{it}	is the total interface state density (cm^{-2}),
f	is the pumping signal frequency (s^{-1}), and
A_G	is the device channel area (cm^{-2}).

Furthermore, Nit can be expressed as

$$N_{it} = \int_{E_1}^{E_2} D_{it}(E)\, dE \cdots\cdots\cdots\cdots\cdots\cdots(2.5)$$

where D_{it} (E) is the interface state density at energy level E (cm^{-2}-eV^{-1}), and E_1 and E_2 are the lower and upper energy limits of the interface state density distribution, respectively [84]. By using equation (2.5), equation (2.4) can be rewritten as

$$I_{CP,MAX} = q\, f\, A_G \int_{E_1}^{E_2} D_{it}(E)\, dE$$

.

$$= q^2\, f\, A_G\, \overline{D_{it}}\, \Delta\psi_s \cdots\cdots\cdots\cdots\cdots\cdots(2.6)$$

where $\overline{D_{it}}$ is the averaged interface state density and $\Delta\psi_s$ is the energy range of the interface states. It is shown that $\Delta\psi_s$ can be expressed as [83, 84]:

$$\Delta\psi_s = -q\,(E_{em,e} - E_{em,h}) \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2.7)$$

and therefore,

$$E_{em,h} = E_i + k\,T\,\ln(v_{th}\;\sigma_p\;n_i\;t_{em,h} + e^{(E_F,acc - E_i)/kT}) \quad \cdots\cdots\cdots\cdots (2.8)$$

$$E_{em,e} = E_i - k\,T\,\ln(v_{th}\;\sigma_n\;n_i\;t_{em,e} + e^{(E_i - E_F,inv)/kT}) \quad \cdots\cdots\cdots\cdots (2.9)$$

$$t_{em,e} = \frac{|V_{FB} - V_{th}|}{|\Delta V_A|} t_f \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2.10)$$

$$t_{em,h} = \frac{|V_{FB} - V_{th}|}{|\Delta V_A|} t_r \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2.11)$$

where

$E_{em,h}$ is the energy level for the trapped holes (eV),

$E_{em,e}$ is the energy level for the trapped electrons (eV),

E_i is the silicon intrinsic Fermi level (eV),

k is the Boltzman constant (eV/K),

T is the absolute temperature (K),

v_{th} is the thermal velocity (cm^2/s),

σ_p is the hole capture cross section (cm^2),

σ_n is the electron capture cross section (cm^2),

n_i is the silicon intrinsic carrier density (cm^{-3}),

$t_{em,h}$ is the hole emission time (s),

$t_{em,e}$ is the electron emission time (s),

$E_{F,acc}$ is the Fermi level in the accumulation state (eV),

$E_{F,inv}$ is the Fermi level in the inversion state (eV),

t_r is the rise time of the trapezoidal wave (s), and

t_f is the fall time of the trapezoidal wave (s).

Then finally, $I_{CP,MAX}$ can be expressed as

$$I_{CP,MAX} = 2\ q\ \overline{D_{it}}\ f\ A_G\ k\ T\ \ln\left(v_{th}\ n_i\ \sqrt{\sigma_p \sigma_n}\ \frac{|V_{FB} - V_{th}|}{|\Delta V_A|} \sqrt{t_r t_f} \right) \cdot (2.12)$$

From equation (2.12) it can be seen that if $I_{CP,MAX}$ is plotted as a function of $\sqrt{t_r t_f}$, then the slope will be proportional to $\overline{D}_{it}$, and the intersect with the x-axis will be proportional to the geometrical mean of electron and holes capture cross section ($\sqrt{\sigma_p \sigma_n}$) [87].

Meanwhile, if equation (2.5) is differentiated with respect to t_f, it is shown that

$$\frac{d\,I_{CP,MAX}}{d\,t_f} = q\ f\ A_G\ [\ D_{it}(E_2)\frac{d\,E_2}{d\,t_f} - D_{it}(E_1)\frac{d\,E_1}{d\,t_r}\ ] \cdots\cdots\cdots\cdots (2.13)$$

Since E_1 is independent of fall time [84] and also from equation (2.9), it is found that

$$\frac{dE_2}{dt_f} = -\frac{kT}{t_f} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdot(2.14)$$

Therefore, by using equation (2.13) and (2.14), the interface state density at trap energy level E_2 can be expressed as

$$D_{it}(E_2) = -\frac{t_f}{q\,A_G\,f\,kT}\frac{d\,I_{CP,MAX}}{d\,t_f} \cdots\cdots\cdots\cdots\cdot(2.15)$$

Similarly, the defect density at E_1 can be expressed as

$$D_{it}(E_1) = -\frac{t_r}{q\,A_G\,f\,kT}\frac{d\,I_{CP,MAX}}{d\,t_r} \cdots\cdots\cdots\cdots\cdots(2.16)$$

Therefore, by measuring $I_{CP,MAX}$ at various t_r and t_f, the energy distribution of interface states can be extrapolated, as shown in Figure 2.9 [84].

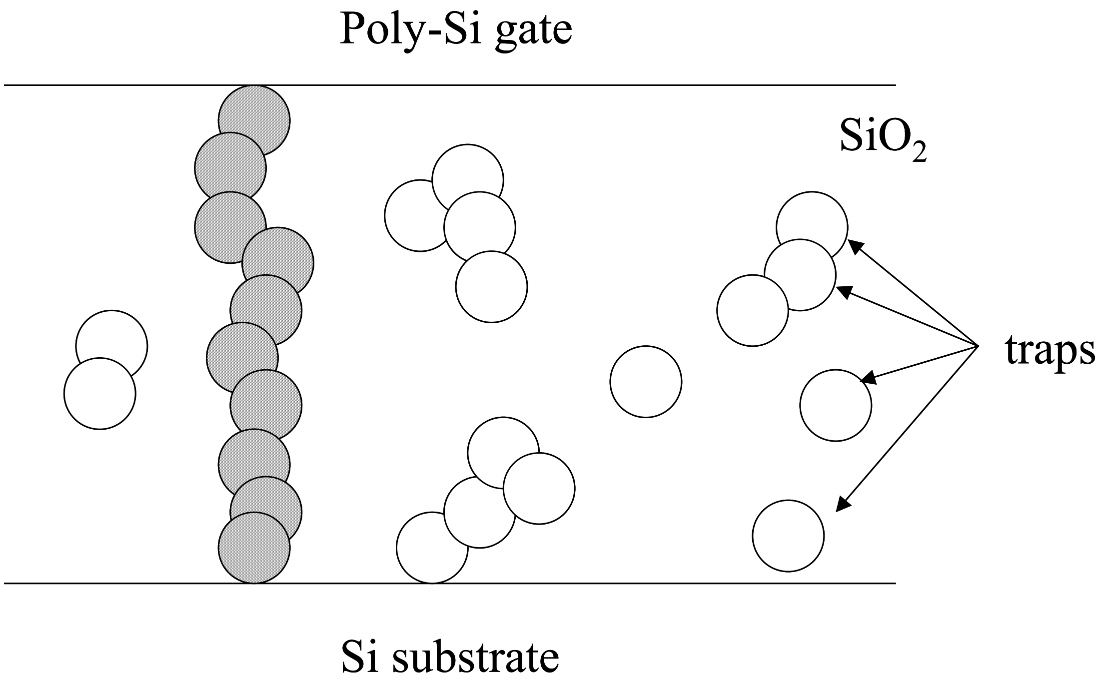

Figure 2.1 Schematic illustration of oxide breakdown proposed by percolation theory [34]. As indicated, the open circles represent the randomly generated electrical defects during stress. When these defects electrically connect the poly-Si and Si-SiO_2 interfaces (shaded circles), they cause oxide breakdown.

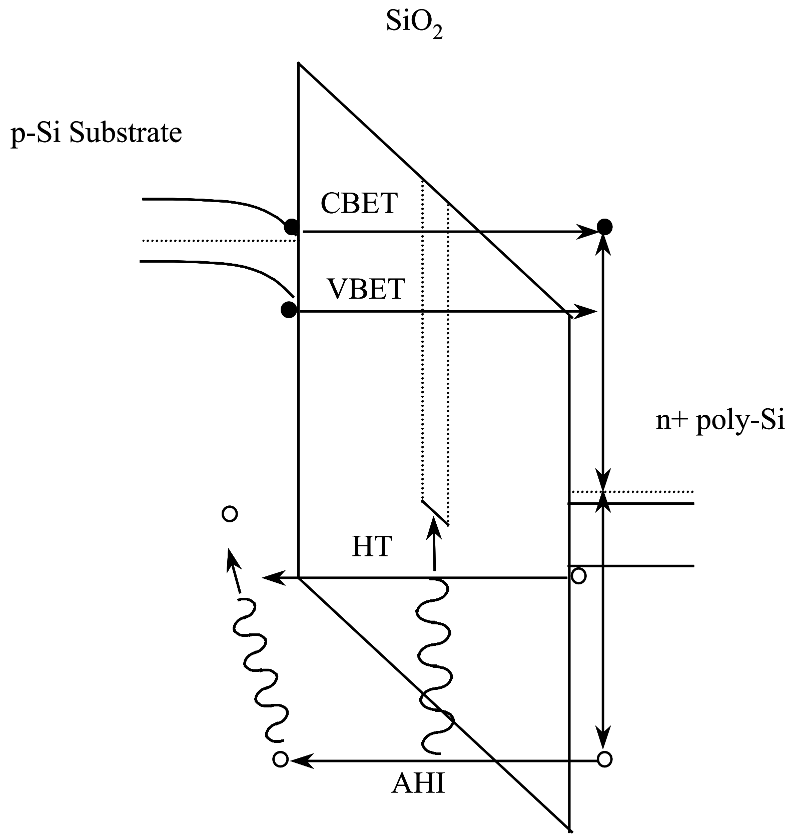

Figure 2.2 Illustration of AHI model for n-channel MOSFET. Energetic electrons are injected from cathode (n-channel) and then tunnel into anode (n+ poly-Si). Holes are generated at anode and tunnel back into oxide due to gate bias.

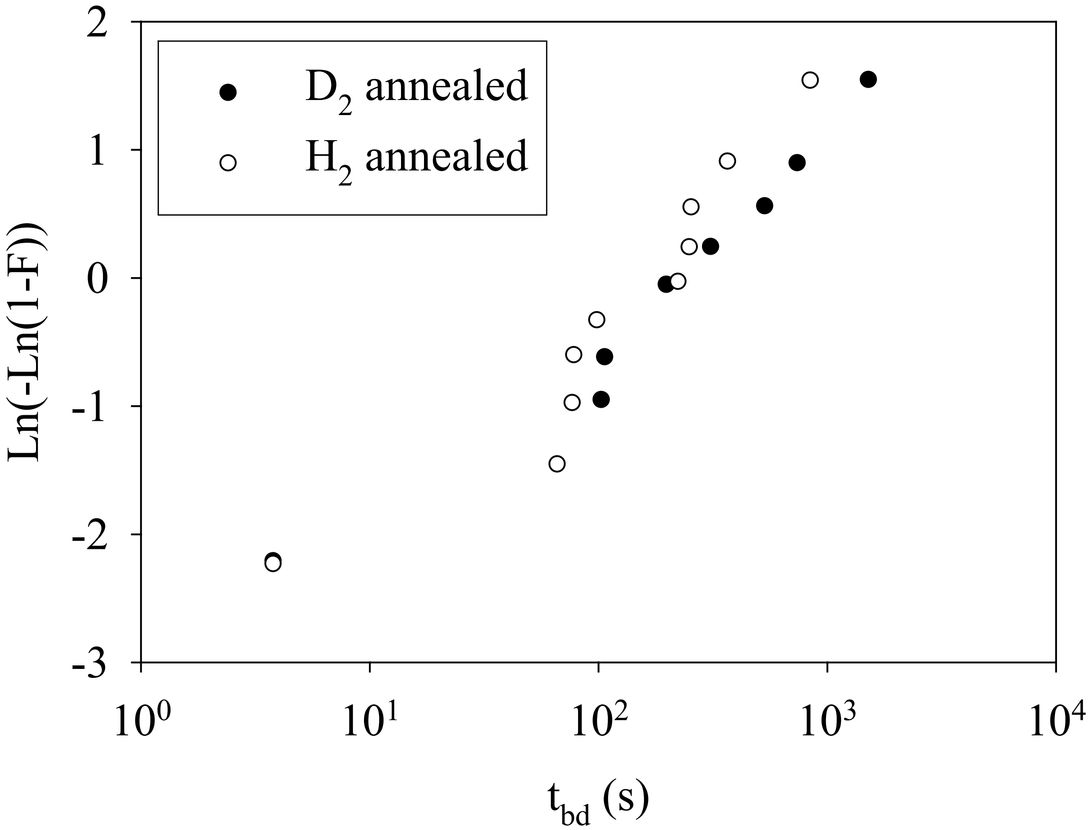

Figure 2.3 The time-to-breakdown comparison between devices with H_2 annealing and D_2 annealing [68].

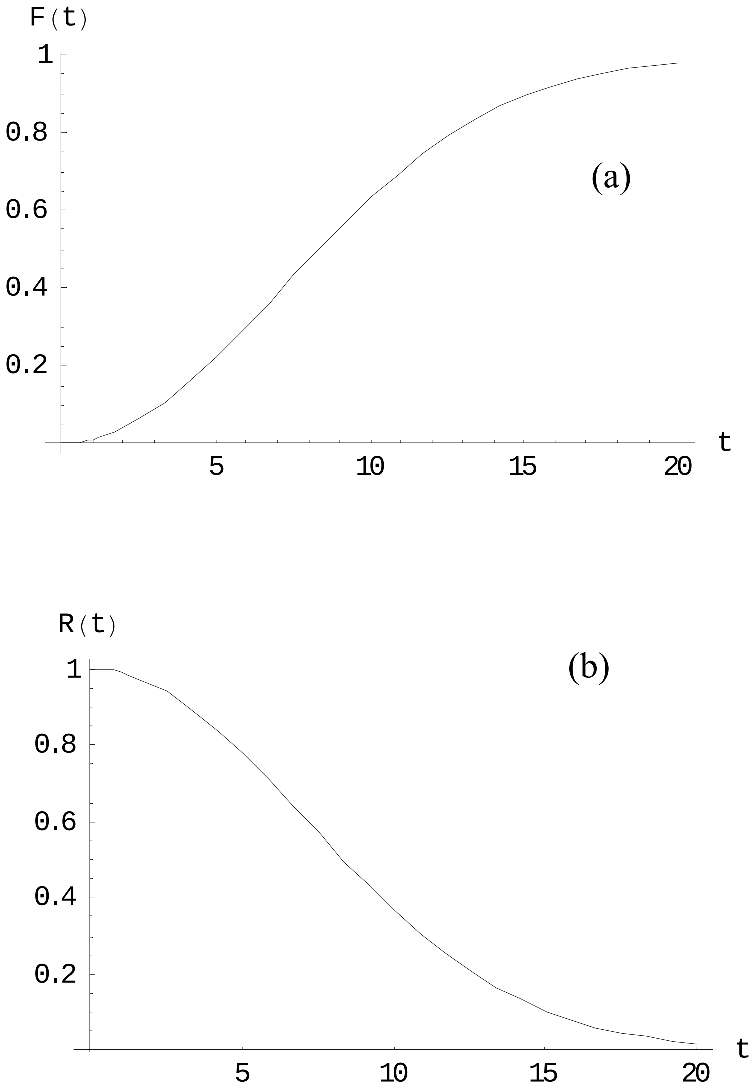

Figure 2.4 Illustration of the general statistical functions. (a) cumulative distribution function (CDF), (b) reliability function [72].

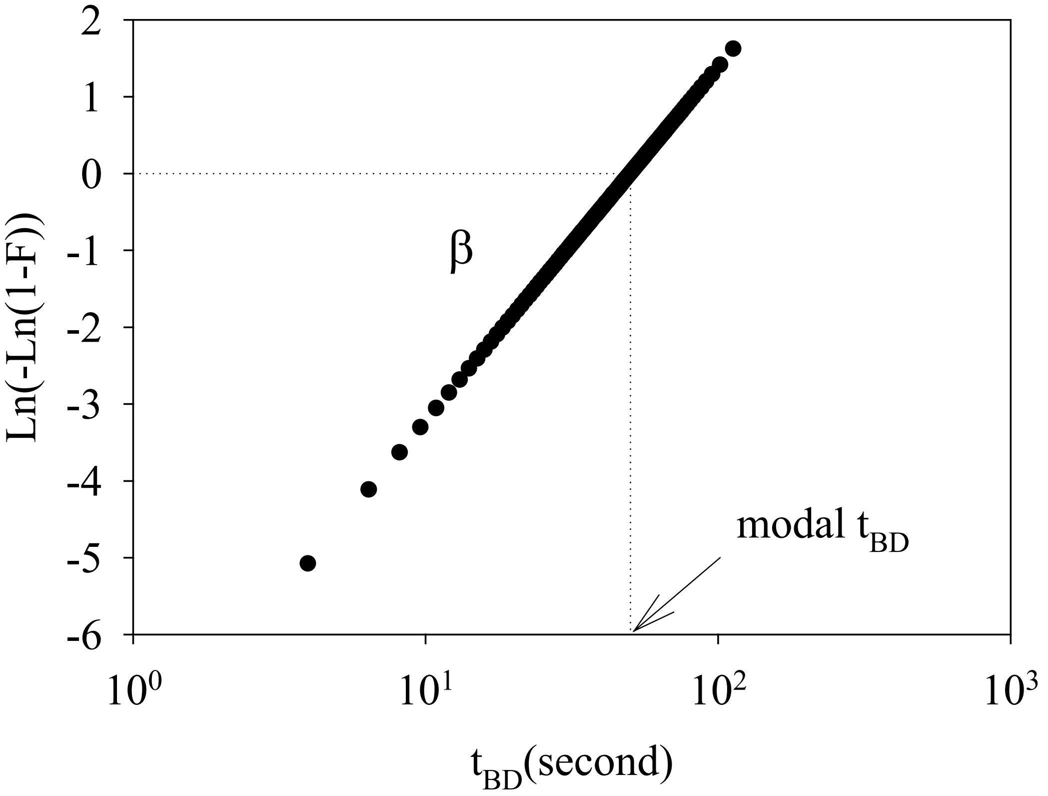

Figure 2.5 Example of statistic Weibull distribution plot of t_{BD}. The slope of the curve is the shape parameter, β. The t_{BD} value of which logarithm value is corresponding to Ln(-Ln(1-F)) = 0 (or F=63%) is usually defined as the time-to-breakdown of the system.

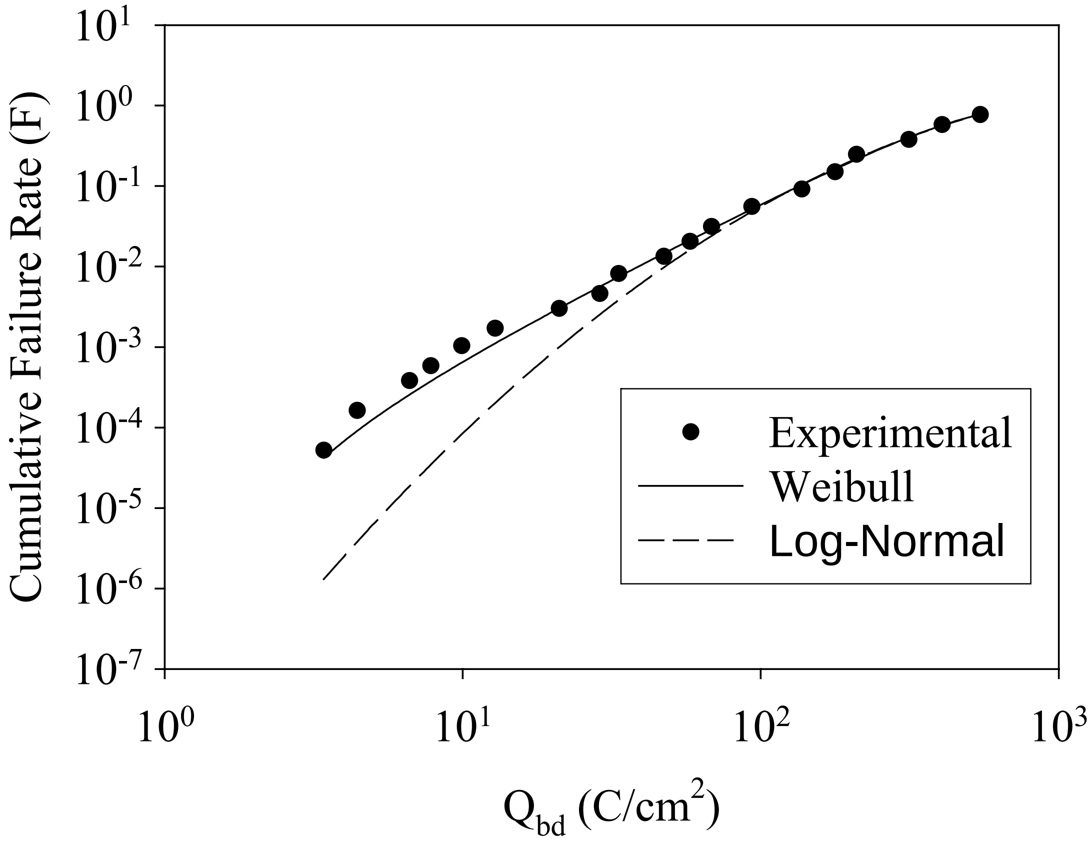

Figure 2.6 Comparison of Weibull distribution and lognormal distribution. Both distributions have been used to fit experiment data but Weibull can better fit experiment data, especially at low percentile [79].

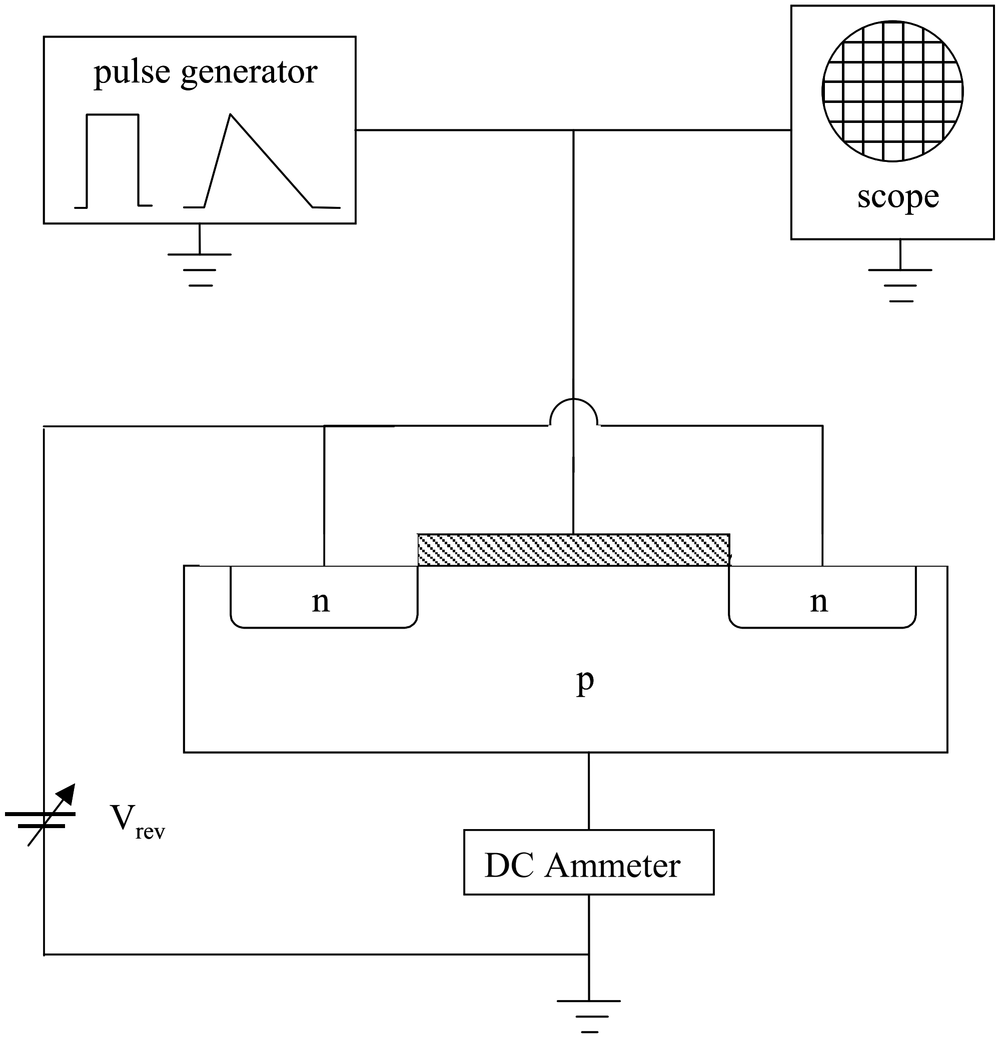

Figure 2.7 The experimental setup for CP measurement. The ac bias is applied to the gate while the source and drain can be grounded or applied small reverse bias. The CP current is measured from the grounded substrate [86].

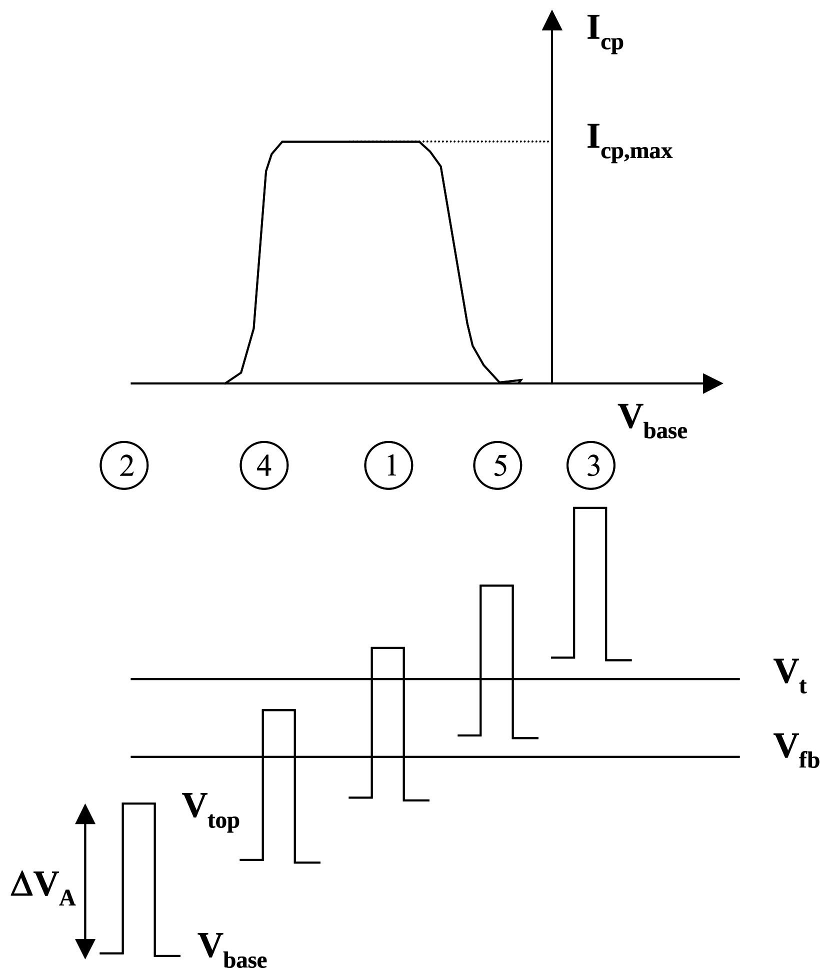

Figure 2.8 The measured I_{CP} as a function of the ramped V_{base} and the relative position of the pumping signal respect to the device V_{FB} and V_{th}. The averaged interface state density is proportional to the I_{CP} measured in region 1 [86].

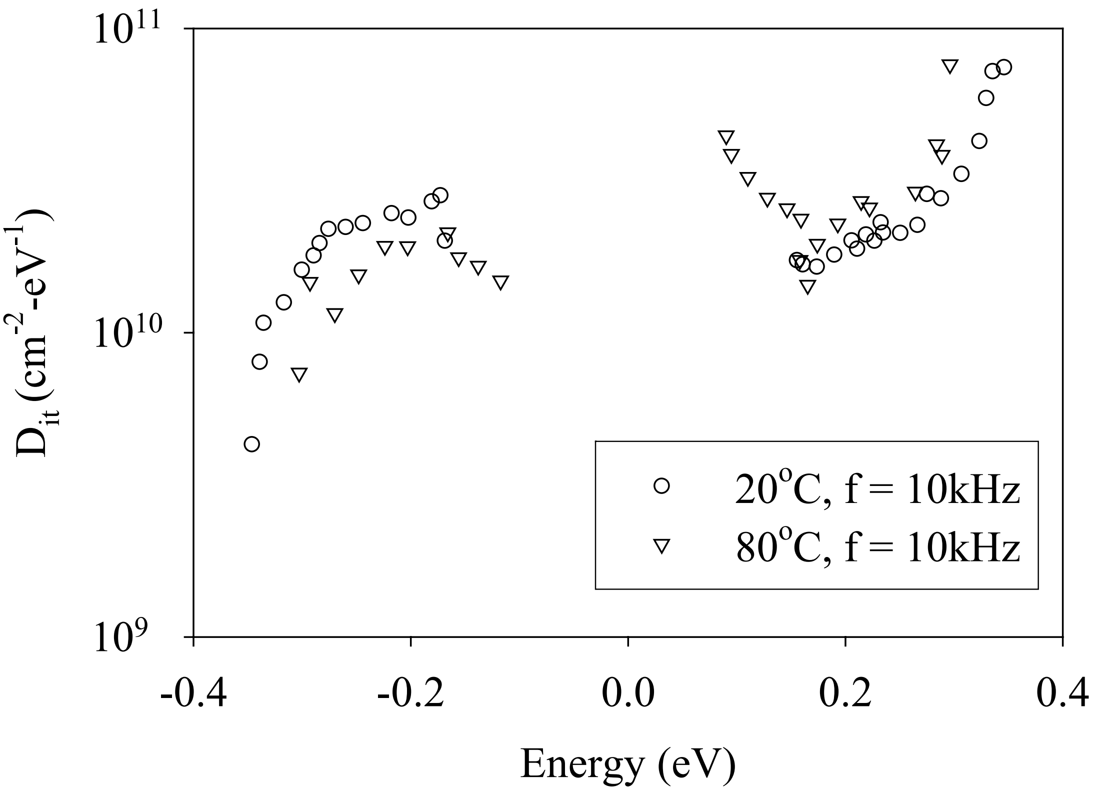

Figure 2.9 The energy distribution of interface trap density for n-channel MOSFET measured by CP method with varying t_r and t_f [84].

Chapter 3

Substrate Hot Hole Injection Experiment

3.1 Overview

Recent work has suggested that the thermo-chemical electric field model cannot explain oxide breakdown. However, it is not clear whether anode hole injection or hydrogen release is the likely mechanism. To determine the more likely model that can describe the gate oxide breakdown, the impact of hot holes on gate oxide breakdown is studied by investigating devices under constant voltage stress with different amount of pre-injected substrate hot holes. The results show that oxide breakdown is independent of the amount of those pre-injected hot holes. This suggests that defects generated by hot holes are not directly related to oxide breakdown during constant voltage stress conditions.

3.2 Introduction

The degradation of the silicon dioxide gate dielectric in Metal-Oxide-Silicon Field Effect Transistors (MOSFETs) has been an interesting and important research topic for several decades [97-101]. Understand the gate oxide breakdown mechanism of MOSFETs is becoming more and more important as the oxide thickness scales down. It is known that electrically active defects are generated when the oxide is under either constant current or voltage stress. Oxide breakdown is believed to be triggered when these defects overlap and form a conducting path connecting the two interfaces of gate oxide [102, 103].

To describe the defect generation, three major models have been proposed: the thermo-chemical electric field model, the hydrogen release model, and the anode hole injection model. For the electric field model recent studies have conclusively shown that defect generation is related to electron fluence and can not just be explained by lattice and electric field interaction. As for the hydrogen release (HR) and anode hole injection (AHI) models, the current controversy between them is whether released hydrogen or generated anode hot holes cause oxide breakdown. A strategy to resolve this controversy is verifying the contributions of either one of these two carriers to oxide degradation.

3.3 Experiment

To focus on the effects of hot holes to oxide degradation, the substrate hot hole injection (SHHI) stress method has been previously used [104, 105]. Under this stress condition, holes are injected from a separate p^+-doped region, which is called injector, into a p-channel MOSFET substrate. These holes are then accelerated toward the Si-SiO_2 interface using a high substrate bias. When they reach the interface, some of these holes can be tunneled or injected into the gate oxide.

It has been shown that the number of defects generated per injected carrier for SHH stress is much higher than constant voltage stress (CVS) by at least one order of magnitude, which suggests that SHHs are much more efficient in generating or activating defects than electrons [104]. However, it was also reported that charge to breakdown (Q_{bd}) for devices under subsequent CVS was not changed by pre-injected SHHs, which suggests that defects generated by holes are not directly linked to oxide breakdown [104]. One possible explanation for this contradiction is the amount of pre-injected SHHs may have been too small to show significant effects. The main purpose of this work is to inject different amounts of SHHs to determine their effectiveness in causing breakdown.

The devices under test in this work are p-channel MOSFETs in a n-well on a p-type substrate as shown in Figure 3.1. The p-type substrate serves as the hole injector. The gate oxide thickness is approximately 3.5 nm and the device area is 2.5 μm^2. Stress induced leakage current (SILC) [106, 107] and charge pumping (CP) measurement [108, 109] are used to monitor the number of defects generated inside the bulk oxide and at the Si-SiO_2 interface, respectively. The stress conditions for SHH injection are V_G =-3 V, $V_S = V_D = 0$, V_{SUB} = 6 V, and V_{inj} = 7 V; while for CVS, the stress conditions are V_G = -5.2 V, V_S=V_D=V_{SUB}=0. All the stresses and measurements are performed at room temperature.

Figure 3.2 shows the characteristic CP data for the device under SHH stress and subsequent CVS. CVS is applied to the devices right after SHH stress is terminated (within seconds) to reduce the impact of charging/discharging effect of the traps. It can be seen that defects are generated much faster during SHH stress as compared to CVS, which is consistent with previous reports [104]. Previous work has shown that the defects generated during the subsequent CVS are not due to the interaction of low-energy tunneling electrons with trapped holes in ultra-thin silicon [104, 110]. It has also been shown that defect generation is dependent on electron energy but is independent on hot hole energy. This is because electrically active defects generated by holes are created by hole trapping whereas defects generated by electrons are create by the release of hydrogen [104]. The SILC data (not shown) showed results similar to the CP data.

Figure 3.3 shows the Weibull distribution for injected hot-hole-charge-to-breakdown (Q_{bd}^{hh}) taken from a group of devices under SHH stress only. This data is used to determine the density of SHHs to be pre-injected for subsequent CVS. From this data, two SHH injections were chosen to be used in subsequent CVS: a high injection corresponding to 80% device failure under SHH stress and a low injection corresponding to 10% device failure under SHH stress. Devices which did not undergo breakdown during the SHH stress were used in the subsequent CVS. The CVS Q_{bd} for devices with two different amounts of SHHs were compared to the CVS Q_{bd} for fresh devices (without pre-injected SHHs). By choosing these two different SHH injection levels, it is expected to see a large decrease in modal Q_{bd} with increasing injected SHHs due to the large number of defects created by the holes, if hot holes have any direct effects on CVS oxide breakdown.

Figure 3.4 shows the Q_{bd} Weibull distributions of devices under CVS with different amount of pre-injected hot holes. The confidence intervals of modal values for each Q_{BD} are also calculated and shown [111]. It can be clearly seen that there is no significant change in either Weibull slopes or modal values in these distributions, which suggests that defects generated by hot holes are very inefficient in causing breakdown during CVS.

The results suggest that although hot holes are efficient in generating defects, these defects are inefficient in causing breakdown during CVS. However, previous reports [104] have shown that breakdown occurs during SHH stress within limited stress time and with a high N_{BD}. To explain this apparent contradiction, one speculation is that different defects are generated under CVS and SHH injection and these defects do not interact with each other. An observation that the Weibull distribution slope for devices under SHH stress is higher than CVS (comparing Figures 3.3 and 3.4), also suggests that different breakdown mechanisms may dominate or different defects are generated under these two different stress conditions. It is clear that if different defects are generated during SHH stress and CVS, it should be expected to see different Weibull slopes and N_{BD}. If these defects do not interact with each other, it should be expected to see the ineffectiveness of pre-injected SHHs to Q_{bd} for subsequent CVS, as reported in this section.

3.4 Conclusion

The results presented here clearly show that defects generated by hot holes have little or no influence on breakdown during CVS. This has important implications in determining the correct physical model for oxide breakdown. Future work will provide further insight as to why defects generated/activated by SHH stress do not cause oxide breakdown during CVS.

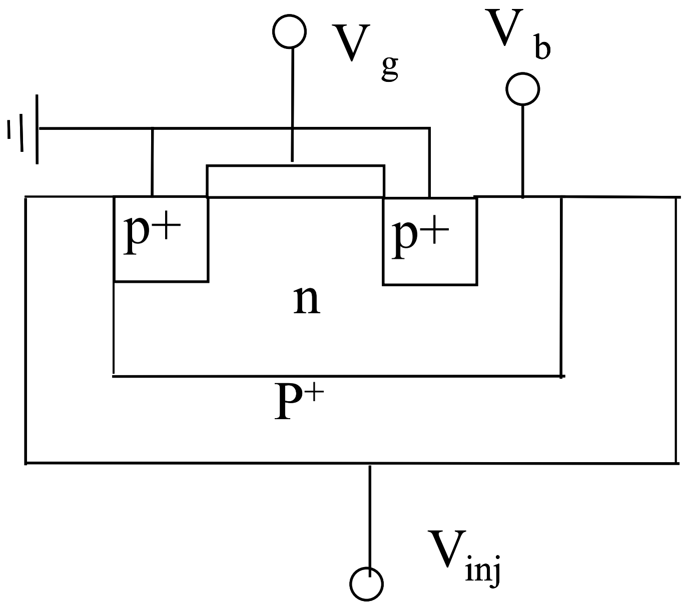

Figure 3.1 Schematic illustration of device structure in this work.

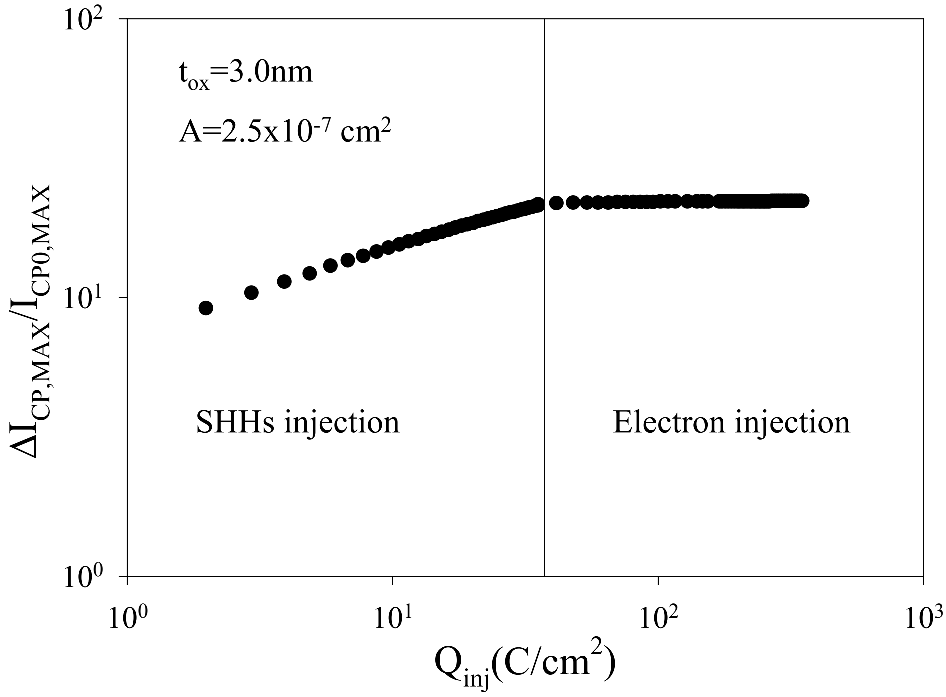

Figure 3.2 Characteristic interface defect generation (CP data) under SHH injection and subsequent CVS.

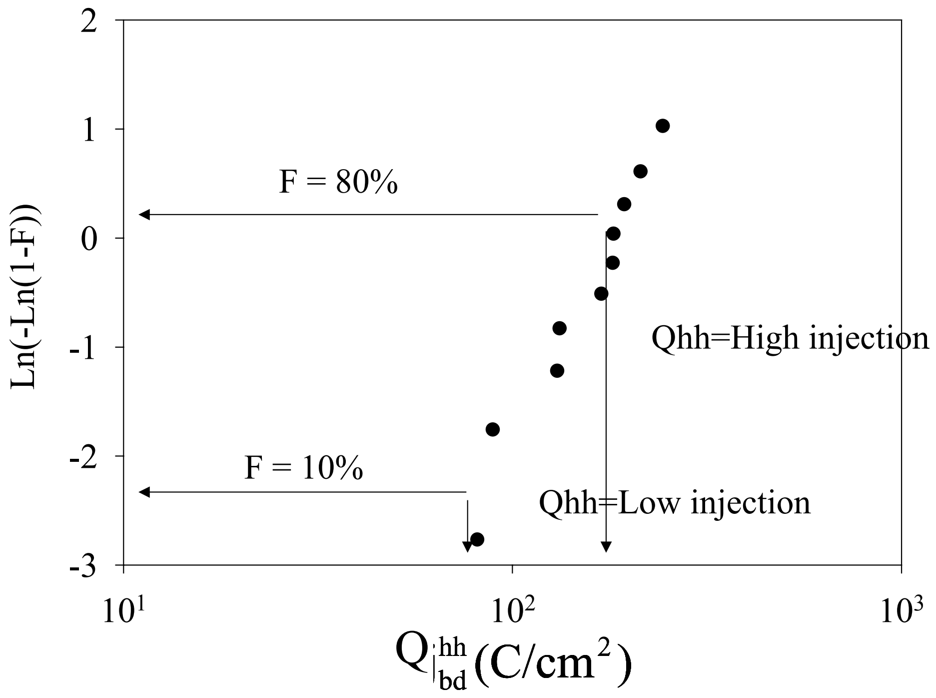

Figure 3.3 Weibull distribution function versus injected-hot-hole-charge-to-breakdown (Q_{bd}^{hh}) under SHH stress.

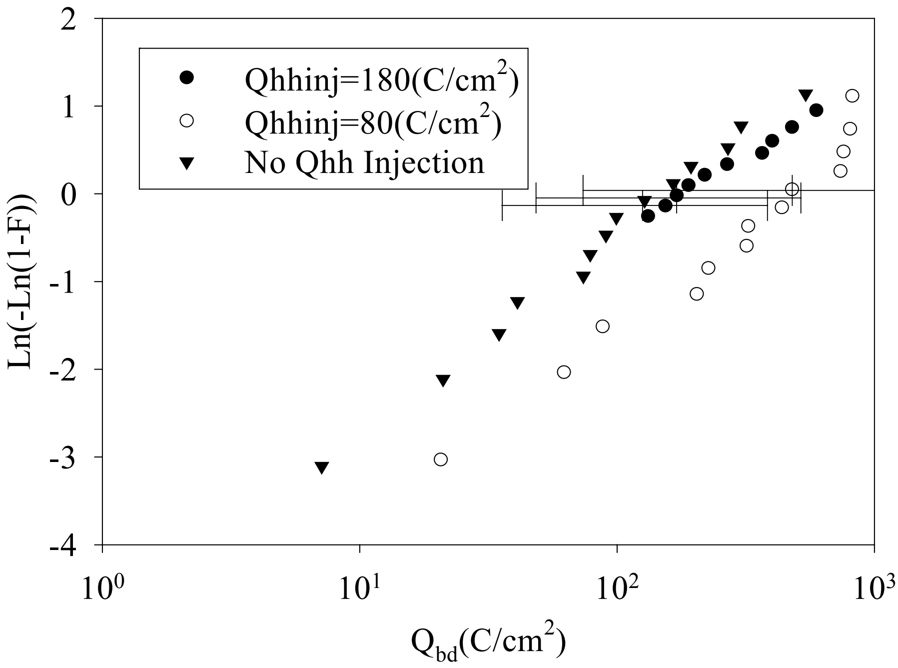

Figure 3.4 Weibull distributions of Q_{bd} for devices under CVS with different amount of pre-injected hot holes by using SHH stress. The bars indicate the 95% confidence intervals for modal Q_{bd}s.

Chapter 4

Sigmoidal Defect Generation

4.1 Overview

The goal of this chapter is to investigate the defect generation as a function of injected charges. The defect generation rate (P_g), which is defined as the derivative of generated defects respect to the injected charges ($\Delta N_{it}/\Delta Q_{inj}$), during constant voltage stress (CVS) is investigated by using short-time voltage pulses over large fluence range. It is found that P_g is not constant during CVS and the voltage acceleration of P_g in the linear defect generation regime is similar to that of the reciprocal of Q_{bd}. Possible mechanisms that can cause the nonlinear defect generation behavior is discussed and the effect of the change of carrier capture cross (σ) during CVS to this nonlinear behavior was investigated. From this study it is conclusively shown that the change of P_g during CVS can not be explained by the change of σ. However, the results conclusively indicate that the linear region of defect generation must be used to extrapolate Q_{bd}.

4.2 Introduction

As mentioned in section 2.4, device lifetimes or t_{bd} are of great interests in both industry and reliability research [112-114]. However, since the oxide degradation is a gradual process, it usually takes years for the gate oxide to breakdown at normal device operating conditions. Therefore, to study the oxide degradation process within a limited time frame, the gate oxide is usually stressed at accelerated conditions (higher stress voltage or current). The critical reliability parameters such as t_{bd} and Q_{bd} are then extrapolated from the accelerated conditions to operating conditions. Although t_{bd} at operating conditions cannot be measured directly, it can be extracted by measuring P_g value. If one assumes a linear rate of defect generation, P_g, which is defined as $\Delta N_{it}/\Delta Q_{inj}$, is also equal to N_{bd}/Q_{bd}. Then Q_{bd} can be found as $Q_{bd}=N_{bd}/P_g$. Since N_{bd} is weakly dependent on the gate voltage (V_g) [112], Q_{bd} (and therefore t_{bd}) can be extrapolated if the voltage dependence of P_g is known [114].

However, since P_g is found not a constant during a stress [115], inconsistent extrapolations can be obtained using this method. Figure 4.1 shows the extrapolation of t_{bd} from the stress condition (high stress voltage) to the normal device operating condition (low stress voltage) assuming linear and nonlinear defect generation [114]. The results show that different extrapolation methods can cause several orders of magnitude variations in the predicted t_{bd} at normal operating condition. Therefore, understanding defect generation and its relationship to the oxide breakdown is important in the prediction of device lifetime. Moreover, it is also interesting to understand what mechanisms cause P_g value changes during a stress.

4.3 Determination of Defect Generation Rates

To understand how P_g value changes with Q_{inj}, short-time voltage pulses with constant amplitude have been used to stress devices and the defect generation over large fluence range is observed. The pulses used in this work are uni-polar square pulses with constant voltage amplitude between 5.2 volts and 6 volts, and the frequency is between 100 Hz and 100 kHz. The devices used are n-channel MOSFETs with channel area 30 um^2 and gate oxide thickness approximately 3.5 nm. Charge pumping (CP) [116, 117] and stress induced leakage current (SILC) [114, 118] measurements are performed to determine the average interface state density (D_{it}) and oxide bulk trap density (N_t), respectively. An additional 50-Ω resistor is connected in parallel to the gate probe during pulse stress to match the circuit impedance and maintain the square pulse waveform at the probe end as shown in Figure. 4.2.

From the CP theory introduced in section 2.4.3, it demonstrated that the peak CP current, $I_{CP,MAX}$, is linearly proportional to N_{it}. Since the defect generation rate is proportional to the number of existing defects at any moment [119, 120], the relative increase of interface state density ($\Delta N_{it}/N_{it0}$) instead of the absolute value of N_{it} is generally used in the study of defect generation mechanisms. Therefore, the relative change of $I_{CP,MAX}$ ($\Delta I_{CP,MAX}/I_{CP0,MAX}$) instead of $I_{CP,MAX}$ itself is plotted respect to Q_{inj} for comparison.

Figure 4.3 shows the relative increase in peak CP current ($\Delta I_{CP,MAX}/I_{CP0,MAX}$) as a function of Q_{inj} at different frequencies. It can be seen that the pulse frequency does not affect the defect generation rate, which is consistent with previous report [121]. The frequency independent defect generation means that this pulse stress technique can be used to obtain defect density at extremely small Q_{inj}. The linear defect generation curve is also shown in Figure 4.3 for comparison. It can be seen clearly that defect generation changes from a linear regime at low Q_{inj} (for Q_{inj} ~ 0.1 C/cm^2) to a saturated regime at high Q_{inj} (for Q_{inj} >10 C/cm^2). The same result is also observed from SILC data (not shown).

The nonlinear defect generation curve has also been observed by other research groups and its effects on t_{bd} extrapolation at device operating voltage have been discussed [114]. In order to determine which P_g value can be used to extrapolate t_{bd} or Q_{bd} correctly, the voltage accelerations of P_g value in different regimes are compared. At first, a linear regression is used to fit the defect generation data, which is obtained by stressing a group of 10 devices at a certain stress voltage, as shown in Figure 4.4. This fitting curve represents the characteristic defect generation behavior at each stress condition and therefore, all fitting curves obtained from different stress voltages are compared, as shown in Figure 4.5. From this figure it can be seen that defect generation curves at different stress voltages all show the same saturated tendency at high Q_{inj}.

To investigate the change of voltage acceleration of P_g in different regimes in detail, the same fitting method used in Figure 4.5 is used to plot P_g as a function of Q_{inj}, as shown in Figure 4.6. In the linear regime, significant voltage acceleration of

P_g is observed. However, this voltage acceleration becomes less significant in the saturation regime where all defect generation curves tend to converge. Moreover, it is also noticed that P_g in the "linear" regime is not constant either but changes relatively slower than in saturation regime.

Since P_g is not a constant during a stress, it is necessary to determine which P_g value in different regimes could be used for Q_{bd} or t_{bd} extrapolation. It is reminded that P_g is in proportional to the reciprocal of Q_{bd} by definition under the constant P_g assumption. Therefore, the voltage accelerations of P_g in the linear regime and in the saturation regime with the voltage acceleration of the reciprocal of Q_{bd} are compared, as shown in Figure 4.7. The P_g values compared in certain regime (linear or saturated) are chosen at the same Q_{inj} in different voltages. It can be seen that P_g in the linear regime has similar voltage acceleration as the reciprocal of Q_{bd}, but P_g in the saturation regime is less dependent on voltage. This result suggests that the P_g value in the linear regime can be better used to extrapolate Q_{bd} than that in the saturation regime. To conclusively confirm this point, further work is required on this issue and more experimental data is needed.

4.4 Discussion of Possible Mechanisms for the Nonlinear Behavior of Defect Generation

The non-linearity of defect generation has drawn attention from researchers and different theories have been proposed to explain it. Patrikar *et al*. suggested that the nonlinear defect generation is because the trapped electrons/holes are de-trapped and this trapping/de-trapping reaction will slow down the defect generation at high injection fluence [122]. Hu suggests that the nonlinear behavior is because hydrogen atom diffuses from the broken silicon bond, and therefore it should follow a power law behavior [123]. Sune *et al*. suggest that the non-linearity observed from CP data is because σ changes during stresses [124]. Some of other researchers think the non-linearity is due to the inadequacy of the measuring techniques [112].

Figure 4.8 compares the characteristics of de-trapping model and hydrogen diffusion model with experimental data. The Hydrogen diffusion model requires that the power law exponent be between 0.5 and 1 but the experimental data shows that the exponent in the saturation regime is about 0.3. For the de-trapping model, it shows that the defect generation rate at high Q_{inj} is almost zero, which has never been observed from experiments. Therefore, neither of these two models can explain the defect generation over the whole fluence range. As for the effect of σ change on the observed nonlinear relative increases of peak CP current and SILC, it is suggested that since σ is found not a constant during stress, the relative increases of peak CP current and SILC are not really proportional to D_{it} and N_t, respectively. Therefore, the nonlinear relative increases of peak CP current and SILC may still lead to linear D_{it} and N_t generations due to this σ change effect [125]. In the following part of this section, this issue will be addressed. However, since it is difficult to extract σ from SILC data, in the following analysis σ will be extracted from CP data only and the behavior of σ inside bulk oxide is assumed to be similar to that at the interface.

By using the standard two-level charge pumping method with sinusoidal waveform as the pumping signal, both σ and D_{it} could be extracted at the same time [117, 125]. In this work, pulse stresses are interrupted periodically when the CP measurement is performed and σ and D_{it} are extracted. Therefore, σ and D_{it} could be monitored as a function of injected charge. Figure 4.9 shows σ as a function of Q_{inj}. As it can be seen, σ does change during voltage stress and it decreases with Q_{inj}. However, the nonlinear generation behavior of D_{it} is still observed, as shown in Figure 4.10. It suggests that the change of σ can not explain the non-linearity of defect generation.

To show the effect of σ change on defect generation over Q_{inj}, the relative change in D_{it} assuming constant σ with that in which σ changes with Q_{inj} are compared, as shown in Figure 4.11. The linear defect generation curve is also shown in this figure for comparison. It is shown that the D_{it} generation with changing σ is closer to linear generation than the data with constant σ at low Q_{inj}. However, a similar power law saturated behavior of D_{it} is still observed at high Q_{inj}. This result suggests that the saturated behavior of defect generation is unlikely to be explained by the change of σ. It is also noticed from Figure 4.11 that the difference between D_{it} curves with constant σ and changing σ is small, except at very small injected fluence. Therefore, the general assumption that the relative increase of peak CP current is proportional to D_{it} generation is still valid and the conclusion obtained in section 4.3 still holds.

To get a better idea of how possible it is for the change of σ to be fully responsible for the saturation of defect generation at high Q_{inj}, the experimental CP data and the linear D_{it} generation curve are used to calculate the necessary corresponding σ over Q_{inj}. The result is shown in Figure 4.12. The experimental measured σ as shown in Figure 4.9 is re-plotted and also shown for comparison. It can be seen that in order to obtain linear D_{it} generation from the measured saturated CP data, σ has to increase instead of decrease as observed from experiment. Also, it has to increase to an unreasonable large value. This result suggests it is unlikely that the saturation of defect generation can be explained completely by the change of σ.

4.5 Conclusion

In this chapter, it has been shown that the voltage acceleration of P_g in the linear generation regime is closer to the voltage acceleration of the reciprocal of Q_{bd} than that in the saturation regime. This result suggests the P_g value in the linear regime can be better used for Q_{bd} and t_{bd} extrapolation to device normal operating conditions. It is also shown that the saturated behavior of defect generation can not be solely explained by the change of σ. Further work is necessary to determine the reason behind the fluence dependence of P_g.

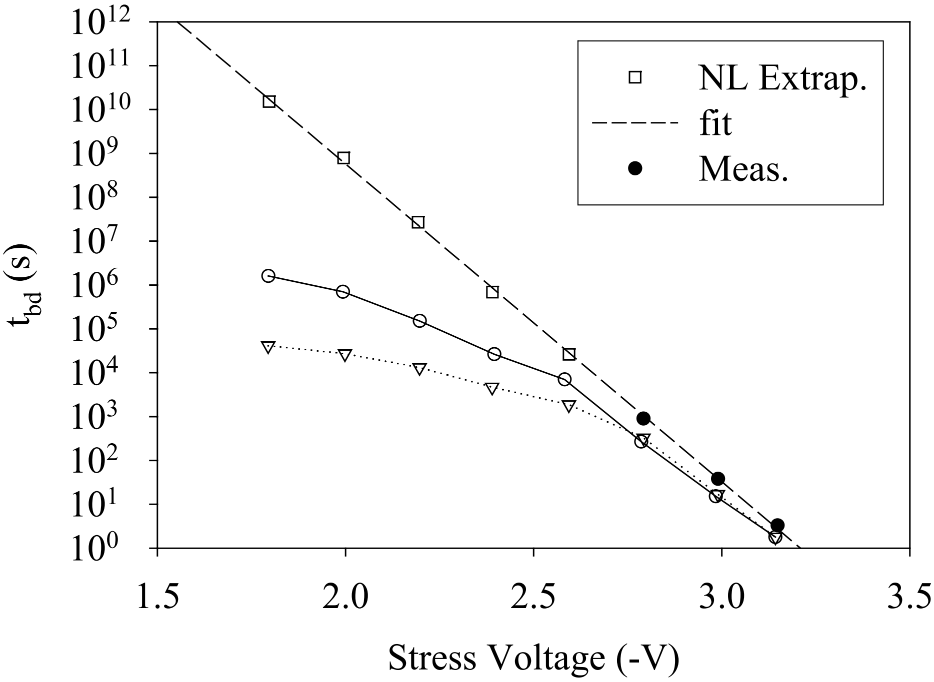

Figure 4.1 Extrapolation of t_{bd} to device normal operating condition (low stress voltage) from accelerated stress condition (high stress voltage). It shows different extrapolations can cause the variations in predicting device lifetime (t_{bd}) as large as several orders of magnitude [114].

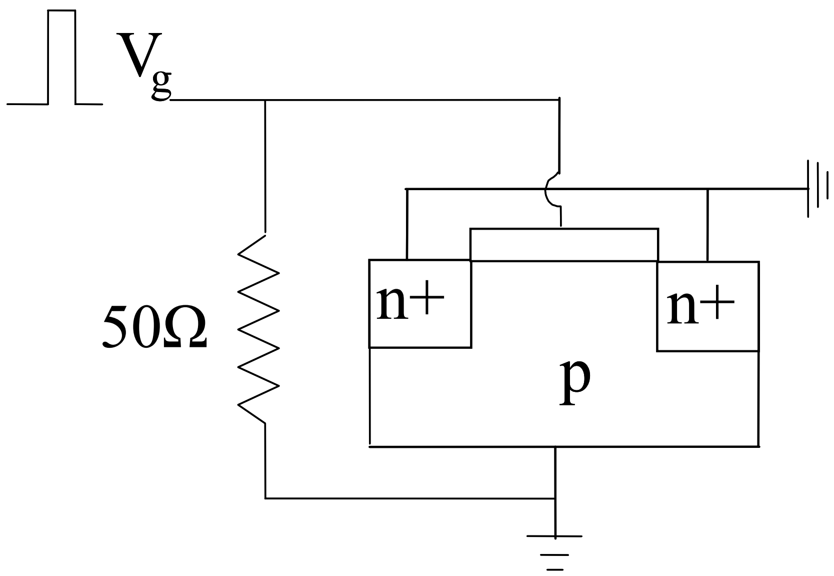

Figure 4.2 Illustration of experimental setup for the pulse stress experiment.

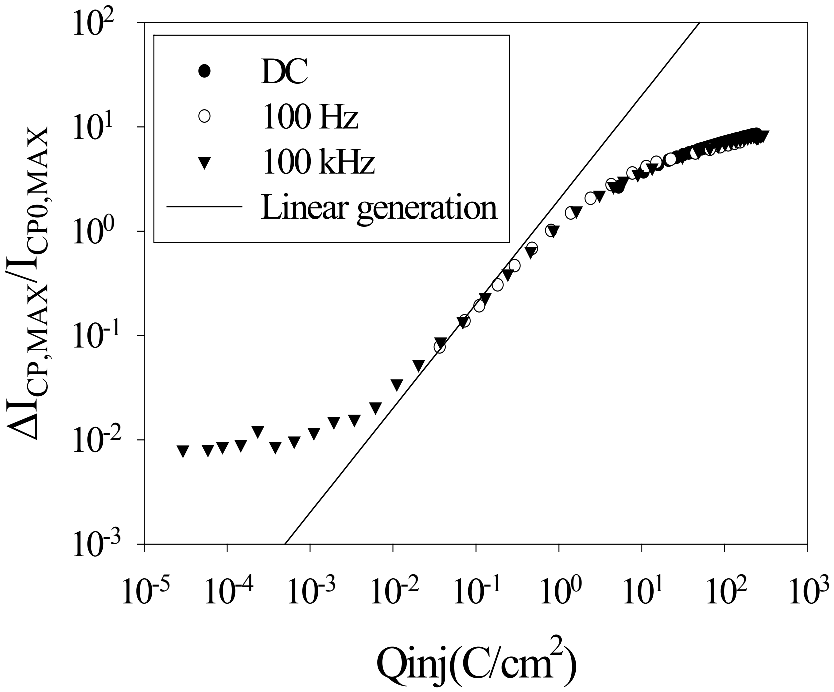

Figure 4.3 Defect generations at different frequencies under pulse stress. The overlaps of these curves showed that this technique can be used to measure defect density at a large range of fluence.

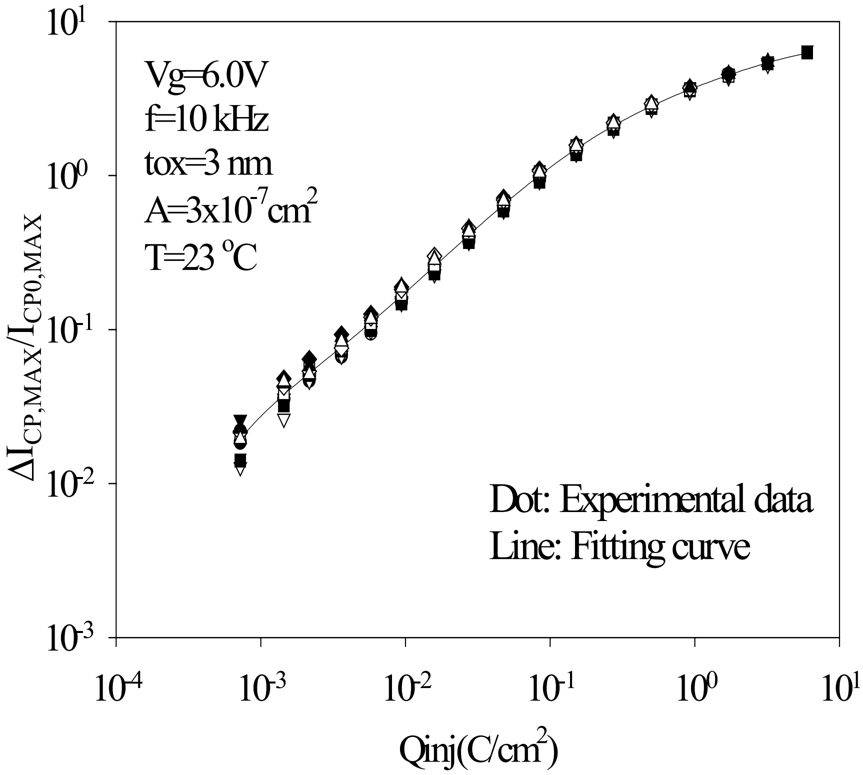

Figure 4.4 Illustration of linear regression fitting curve of defect generation at certain stress voltage.

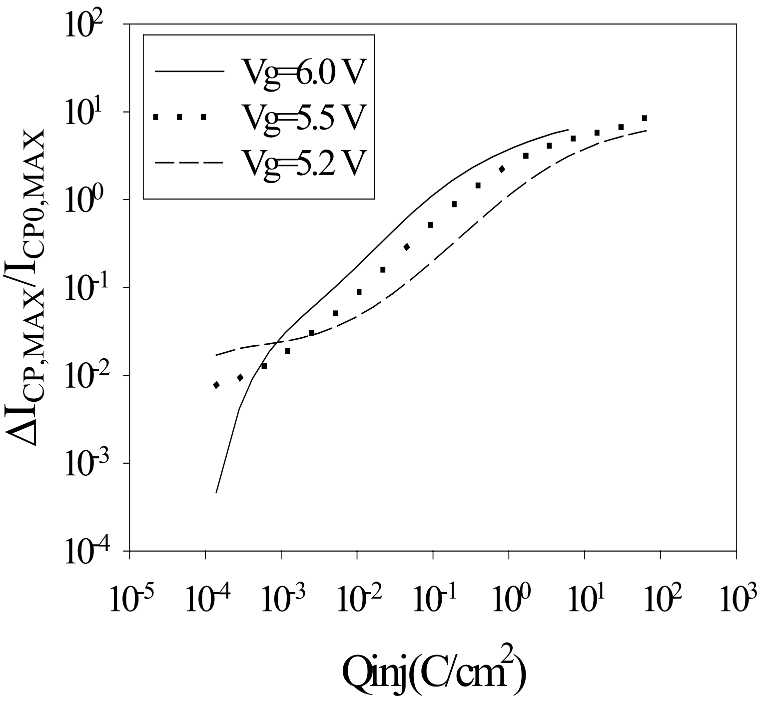

Figure 4.5 Comparison of linear regression fitting curves of defect generations at different stress voltages.

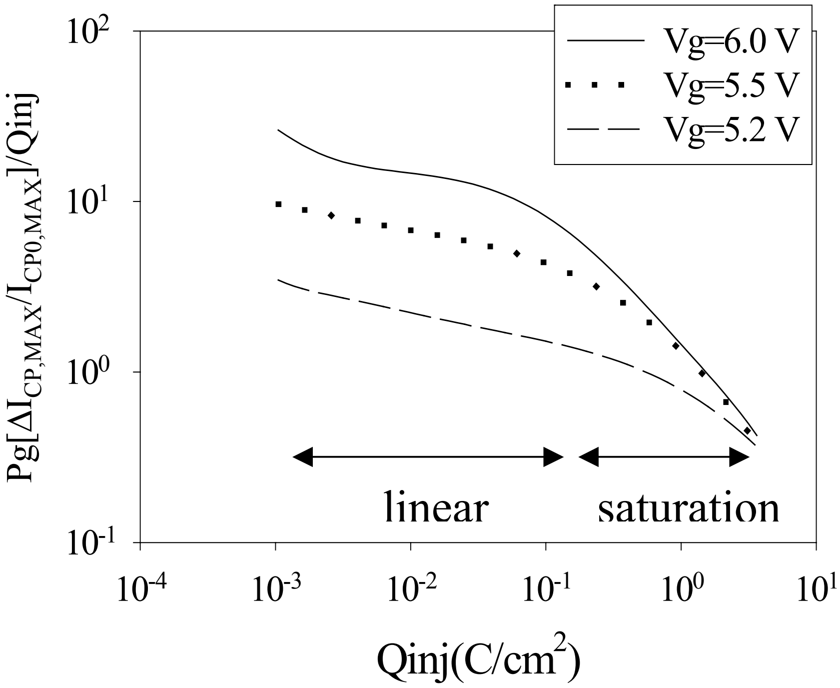

Figure 4.6 The comparison of linear regression fitting curves of P_g at different stress voltages.

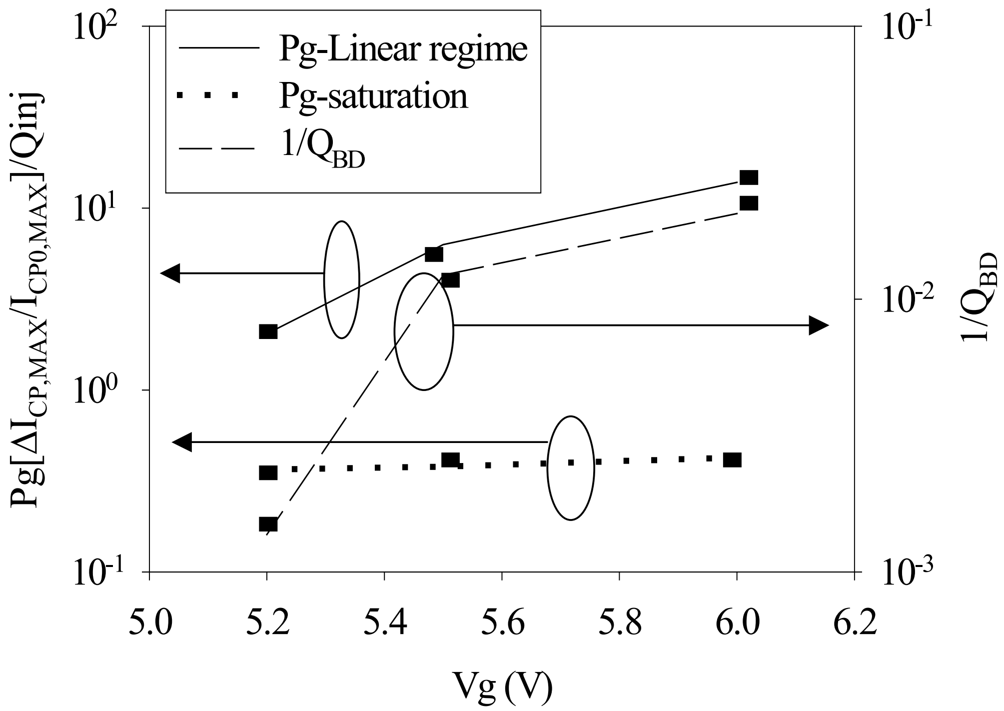

Figure 4.7 Comparison of voltage accelerations of P_g in linear regime, saturated regime and the reciprocal of Q_{inj}.

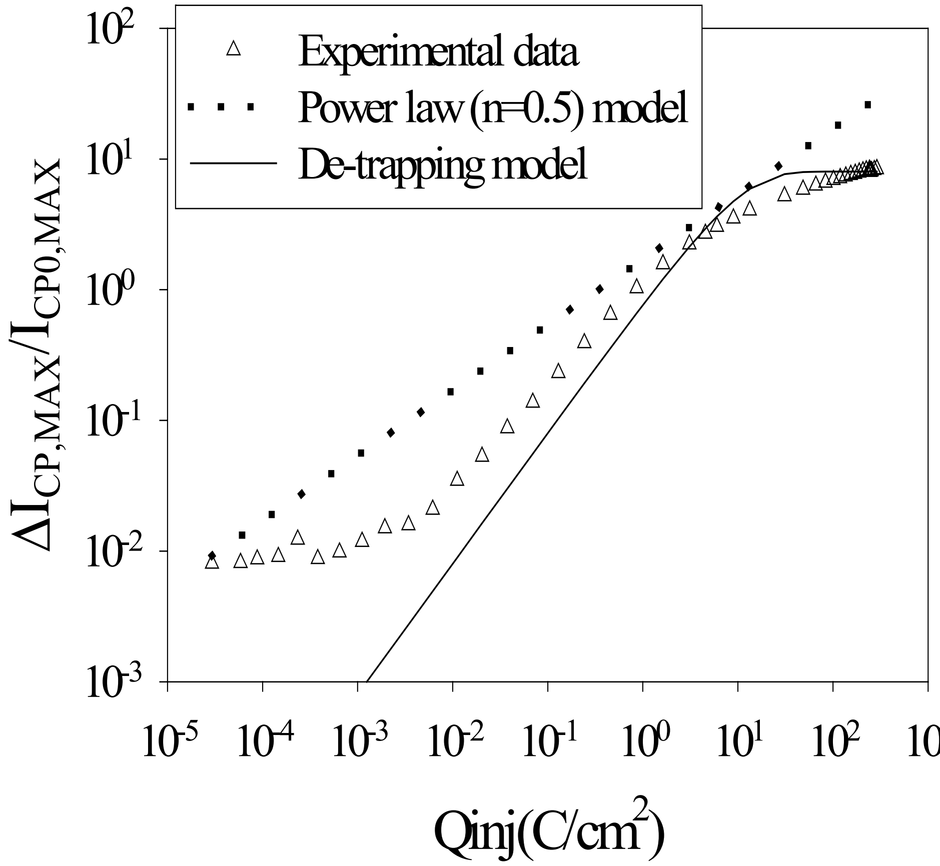

Figure 4.8 Comparison of defect generation of de-trapping model, hydrogen diffusion model and experimental data.

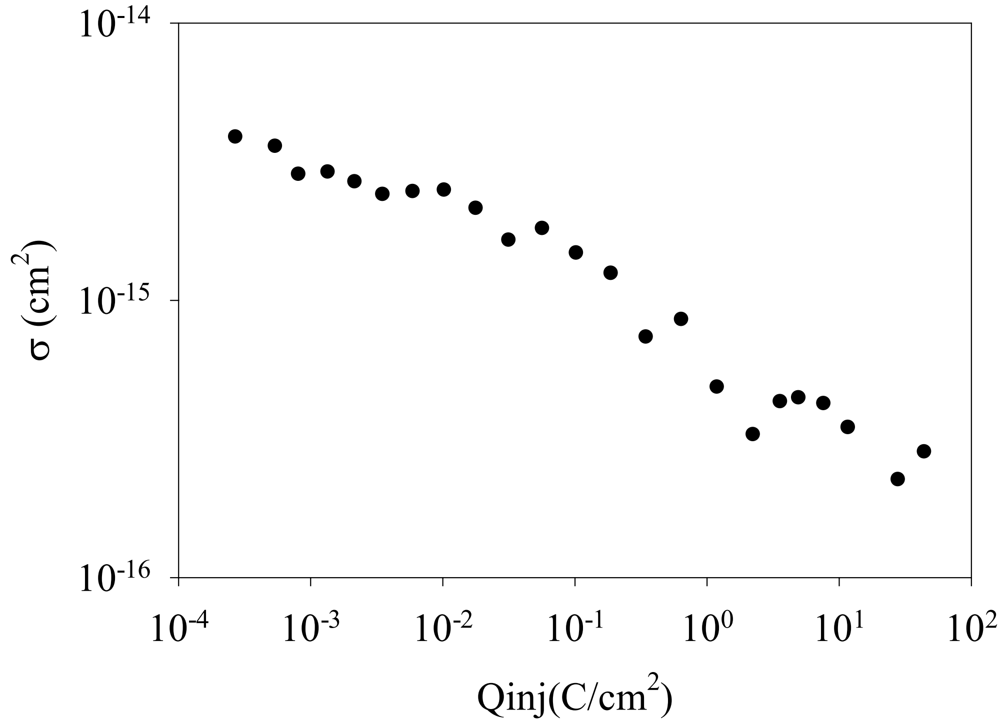

Figure 4.9 Extrapolated carrier capture cross section change over injected fluence.

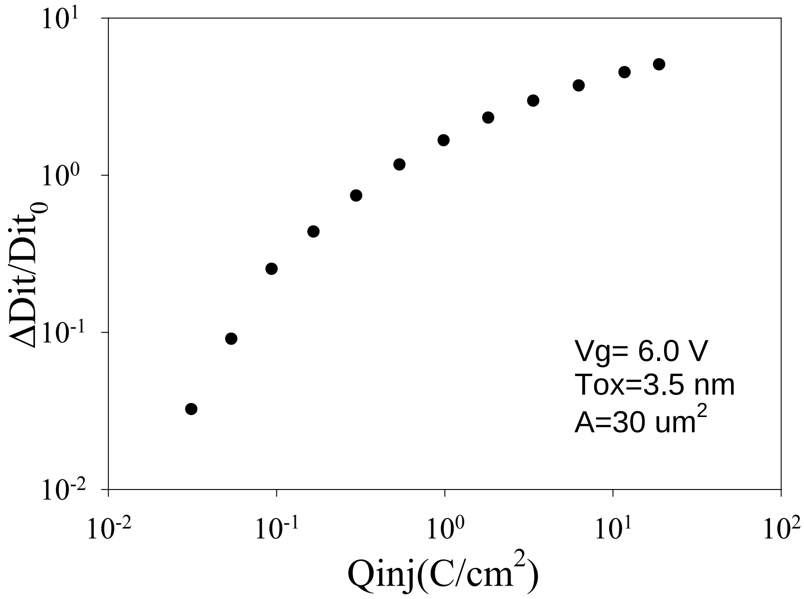

Figure 4.10 Extracted averaged interface state density change over injected fluence.

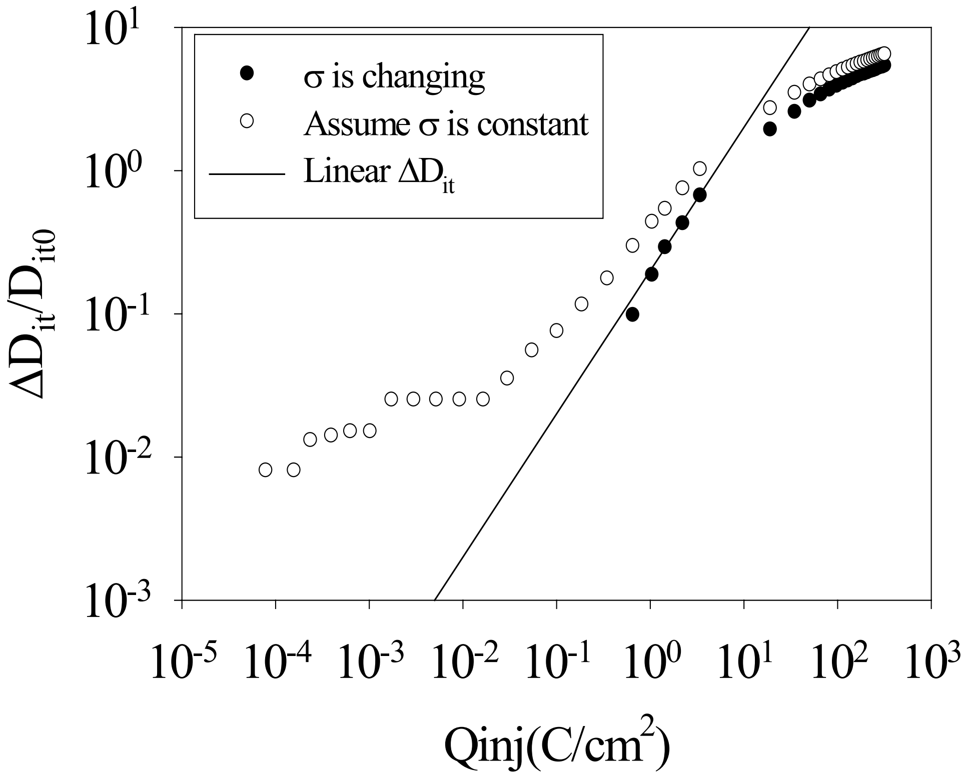

Figure 4.11 Comparison of CP data curve (σ is assumed constant) and D_{it} generation curve (σ is changing with Q_{inj}) with linear defect generation curve.

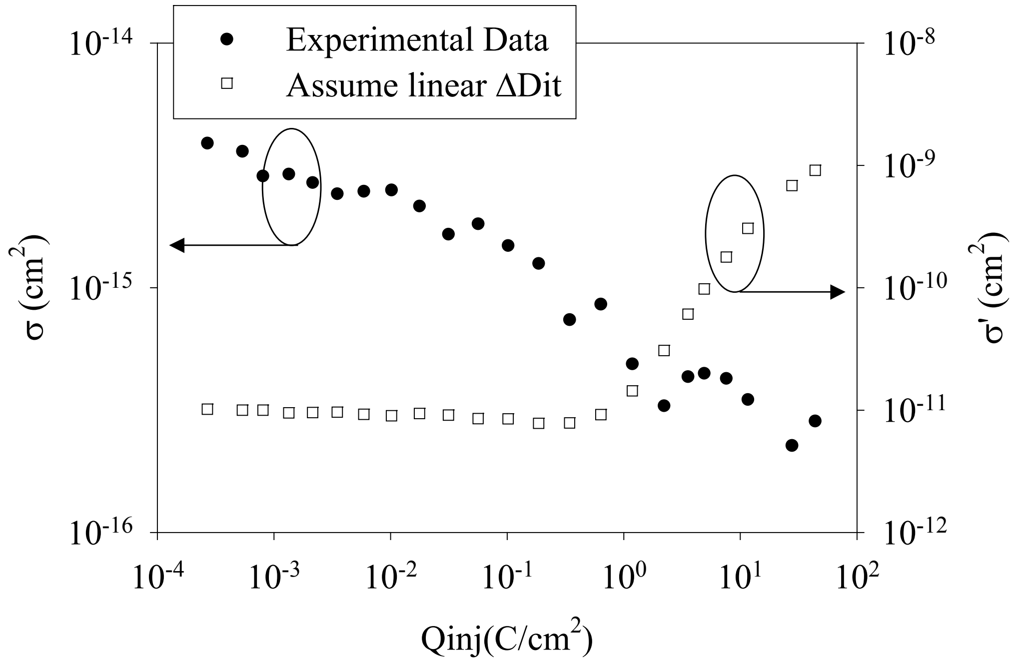

Figure 4.12 Comparison of carrier capture cross sections over injected fluence: experimentally extrapolated (σ) and calculated from linear defect generation assumption (σ').

Chapter 5

The Effect of Mobility Degradation to Threshold Voltage Shifts for Ultrathin Gate Oxides

5.1 Overview

In the previous chapter, the stress-induced defects as a function of injected charges are studied by using interrupted short-time pulse stress method and the nonlinear relationship is revealed. These generated defects affect device parameters such as gate leakage current density (J_g), carrier channel mobility (μ), and device threshold voltage (V_{th}) through various mechanisms. These parameters are used not only to monitor oxide degradation but also as the bases for building up empirical oxide degradation models. To ensure these models are correct, it is important and necessary to study the mechanisms that affect these parameters.

Therefore, the goal of this chapter is to investigate the dominant mechanism that causes device threshold voltage (V_{th}) shift. V_{th} shifts of p- and n-channel MOSFETs during a stress are analyzed from both experiment and simulation. The result of the analysis showed that V_{th} shift is mainly induced by the carrier channel mobility degradation. This result can explain the polarity dependence of V_{th} shifts in p- and n-channel MOSFETs. Besides, it suggested that the commonly accepted idea that V_{th} shifts are due to Coulombic charge generation in the oxide affecting the surface potential is not accurate. It also suggested that proposed oxide degradation mechanisms based on V_{th} shifts measured using I_d-V_g may not be accurate.

5.2 Introduction

The degradation of the gate oxide of metal-oxide-semiconductor field effect transistors (MOSFETs) during an electrical stress is an extensive issue in device reliability and has been investigated from various aspects for many years [126-128]. The proposed empirical models for the oxide degradation mechanisms based on experimental observations are monitored by using various techniques such as charge pumping (CP) [129, 130], stressed induced leakage current (SILC) [131-132], DCIV [133], gate leakage current [134-136], and I_d-V_g [132, 137-139], etc. The device V_{th} shift measured by using MOSFET I_d-V_g characteristics is commonly assumed to be due to shifting of the characteristics by Coulombic charge build-up ($\Delta Q/C_{ox}$) in the dielectric [137-139]. However, the contribution of the carrier channel mobility degradation to V_{th} shift is not well characterized. Therefore, to distinguish the contributions of Coulombic charge effect and the carrier channel mobility degradation to V_{th} shift is the main focus of this work.

5.3 V_{th} and V_{FB} Shift Measurements

The devices under test were fully processed p- and n-channel MOSFETs with an area 50x50 μm^2 and gate oxide thickness of 2 nm. Constant voltage stress (CVS) was applied at room temperature, and V_{th} was measured periodically during the stress. In order to explore the mechanisms causing V_{th} shifts, V_{th} shift measured using the I_d-V_g method is compared with flat band voltage (V_{FB}) shift measured by Capacitance-Voltage (C-V) method. For devices which V_{FB} shifts were measured and calculated from the C-V method using a LRC meter, they were also stressed by using the same instrument to reduce noise. Accordingly, both p- and n-channel devices were divided into two groups in this work. In the first group, CVS was applied by using a HP4156B semiconductor analyzer at ±3.7 V, and V_{th} was measured by using the I_d-V_g SPICE method [132, 136]. In the second group, CVS was applied by using a HP4248A LCR meter with DC bias at ±3.7 V, and the oscillation voltage amplitude was 5 mV at 10 Hz. V_{FB} shifts of devices in this group were obtained by first measuring the capacitance change (ΔC) at a chosen measurement voltage ($V_{measured}$) and then being divided by the derivative of the initial C-V curve (dC/dV) at $V_{measured}$, as shown in Figure 5.1. The frequency and oscillation voltage amplitude for V_{FB} measurement were 100 kHz and 50 mV, respectively.

Figure 5.2 shows the comparison of V_{th} shifts using I_d-V_g method and V_{FB} shifts using C-V methods in n-channel MOSFETs stressed in inversion condition.

Each measurement was repeated seven times after each stress and three different devices were tested. The variances between the maximum and minimum experimental data values were smaller than the plotted symbols. It can be seen clearly that V_{th} shift measured by the I_d-V_g method is much larger than V_{FB} measured by the C-V method. Figure 5.3 shows the measurement results for p-channel MOSFETs and similar conclusions are obtained. Although it is not shown, it should be noticed that the general behaviors of measured V_{th} and V_{FB} shifts for both channels of MOSFET stressed in accumulation condition are similar to those observed in inversion condition.

It is believed that the V_{th} shift measured by the I_d-V_g method can be induced by Coulombic charge in the oxide affecting the surface potential or the degradation of the carrier channel mobility causing a decrease in the drain current at a given gate bias. On the other hand, the measured V_{FB} shift is believed to be completely due to the Coulombic charge accumulation inside the oxide. Since the measured V_{th} shift from I_d-V_g method is much larger than V_{FB} shift from C-V method, it suggests that the mobility degradation during CVS should have a larger effect than the Coulombic charge accumulation inside the oxide on V_{th} shift measured by I_d-V_g method.

5.4 Simulation of V_{th} Shift

To verify the hypothesis and determine the dominating mechanism causing V_{th} shifts, the North Carolina State University (NCSU) Mod2D mobility extraction program was used to simulate V_{th} shifts. In this program, the interface scatter density (N_{scat}) is used to model Coulombic scattering (and, hence, mobility reduction). The fixed oxide charge density (Q_{ox}) is used to model the Coulombic charge in the oxide affecting the surface potential. To distinguish the contributions from N_{scat} (mobility degradation effect) and Q_{ox} (Coulombic shift effect) on V_{th} shift, three different scenarios that cause V_{th} shift were simulated: 1) N_{scat} and Q_{ox} increasing at the same rate, 2) N_{scat} increasing at a certain rate with Q_{ox} constant, and 3) Q_{ox} increasing at a certain rate with N_{scat} constant. The initial N_{scat} and Q_{ox} are assumed to be the same and equal to each other in all cases. The simulation results for n- and p- channel MOSFETs are shown in Figures 4 and 5, respectively.

The simulation results clearly show that V_{th} shift due to N_{scat} is much higher than Q_{ox} in both n- and p-channel MOSFETs. It suggests that the carrier channel mobility degradation is the main mechanism causing V_{th} shifts in both types of MOSFET. This simulation result can explain the polarity dependence of V_{th} shifts in n- and p- channel MOSFETs without assuming charges of opposite polarities are generated at the same fabricated oxide in both types of MOSFET. Since the carrier channel mobility degraded during a stress [140, 141], it requires more positive (negative) gate voltage for the n-channel (p-channel) MOSFET to keep up the drain current. As a result, the absolute values of V_{th} in both types of MOSFET are increased, which automatically induces the polarity dependence.

It should be reminded that the simulation results are based on the assumption that the initial N_{scat} and Q_{ox} are equal to each other. However, since the effective N_{scat} and Q_{ox} at Si/SiO_2 interface are affected by the physical location and distribution of defects, the effective N_{scat} and Q_{ox} at interface may not be the same. Therefore, their contributions to V_{th} shifts may change. Nevertheless, the results of this simulation suggest that the commonly accepted idea that V_{th} shifts are due to Coulombic charge generation in the oxide affecting the surface potential may not be accurate. It also suggests that proposed oxide degradation mechanisms based on V_{th} shifts measured using the I_d-V_g method may not be accurate.

5.5 Conclusion

In this work, it is shown by using modeling that the dominant cause of V_{th} shift measured using I_d-V_g is not shifting of the characteristic by Coulombic charges, but is instead due to modification of the I_d-V_g characteristic by mobility degradation if the effective quantity of N_{scat} and Q_{ox} at interface are the same. This result can explain the polarity dependence of V_{th} shifts in p- and n-channel MOSFETs. Moreover, it suggests that oxide degradation mechanisms based on V_{th} shifts measured using I_d-V_g may not be accurate. Finally, it has important consequences on interpreting data and developing an understanding of dielectric reliability physics.

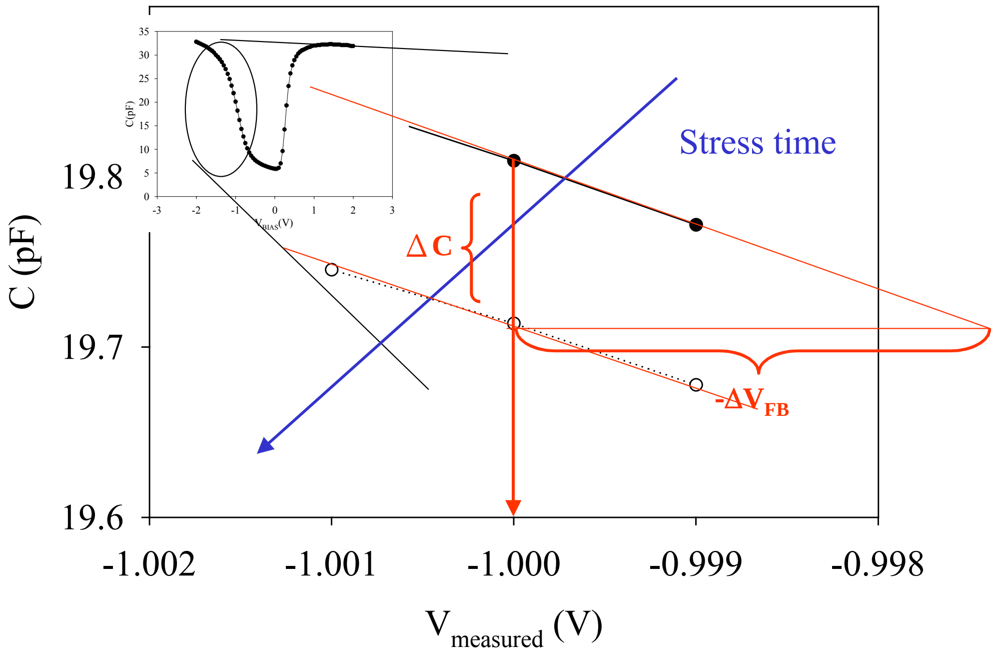

Figure 5.1 Illustration of extraction method of V_{FB} shifts for devices measured by using the C-V method. The insert is the complete C-V curve, and the figure showed the magnified part around V_{FB}.

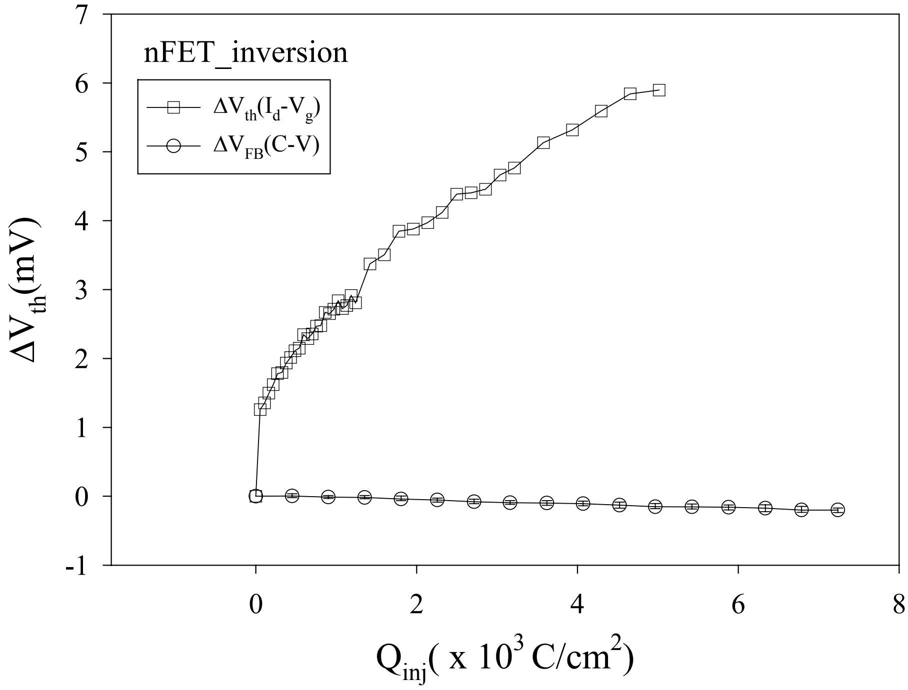

Figure 5.2 Comparison of V_{th} shifts measured by I_d-V_g and V_{FB} shifts measured by C-V methods for n-type MOSFET stressed in inversion.

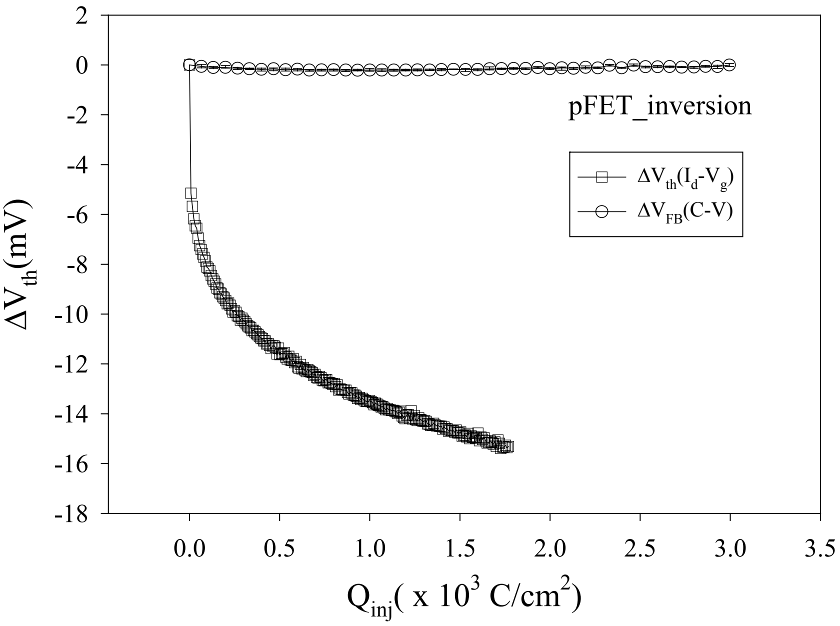

Figure 5.3 Comparison of V_{th} shifts measured by I_d-V_g and V_{FB} shifts measured by C-V methods for n-type MOSFET stressed in inversion.

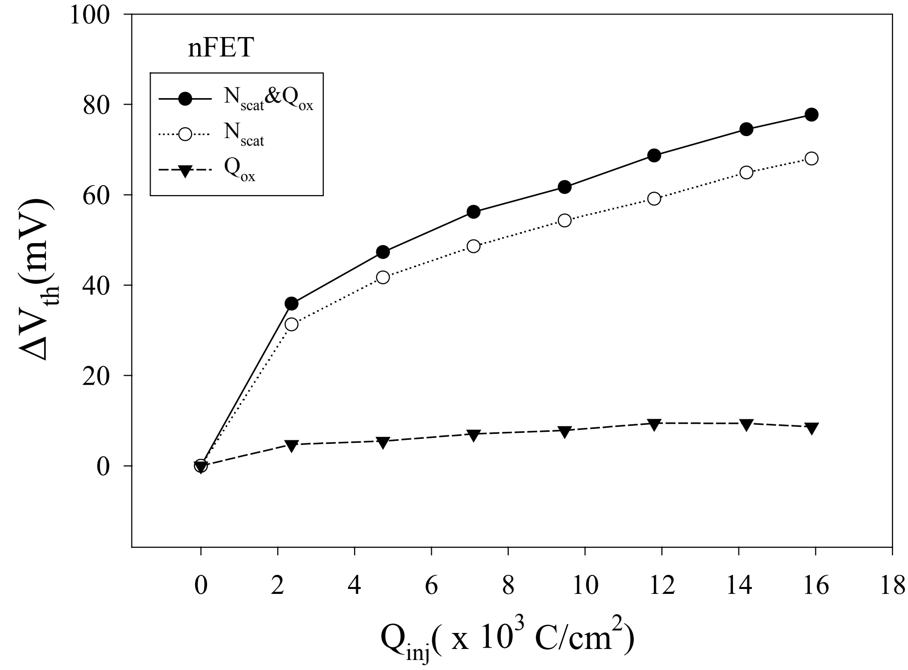

Figure 5.4 Simulation results of V_{th} shifts in n-type MOSFET at different trap generation conditions.

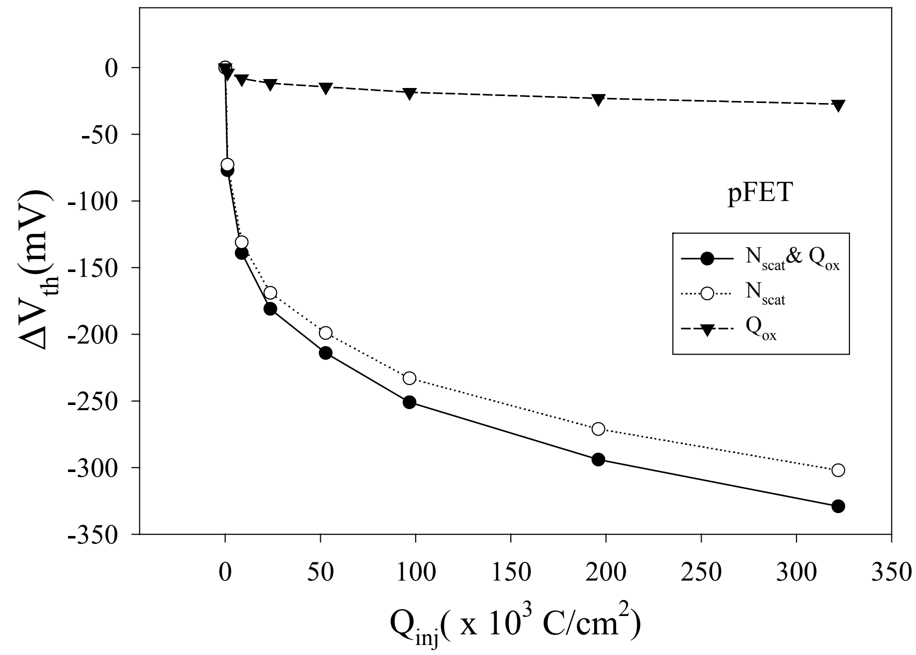

Figure 5.5 Simulation results of V_{th} shifts in p-type MOSFET at different trap generation conditions.

Chapter 6

Electrical Characterization of Spatial Distributions of Trapping Centers in HfO_2/SiO_2 Stacked Dielectrics

6.1 Overview

As mentioned in Chapter 1, high-k dielectrics will be used to replace SiO_2 as the gate material for future MOS devices to reduce leakage current. It is known that high-k dielectrics have significant amount of intrinsic defects (trapping centers) and these defects are distributed not only at the interface but also inside the bulk high-k dielectrics. To correctly characterize these defects would be essentially helpful to understand the properties of these traps.

Therefore, the goal of this chapter is to develop a methodology to characterize the spatial distribution of these traps. The methodology is based on charge pumping (CP) measurement and is used to extract the spatial profile of traps inside SiO_2/HfO_2 stacked dielectrics. From simulation results it showed that different parts of the total traps inside high-k dielectrics would be probed during CP measurement by changing measurement parameters. Traps at different locations inside stacked dielectrics are therefore characterized separately and their spatial profile is revealed. From the spatial profiles of traps, SiO_2 region, SiO_2/HfO_2 diffusion region and HfO_2 region in the stacked dielectric are clearly identified. The correlation between the shift of SiO_2/HfO_2 diffusion region and the difference of the interfacial layer thickness of stacked dielectrics demonstrate this methodology is accurate and reliable.

6.2 Introduction

As the gate oxide thickness of the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is scaled down, the gate leakage current increases exponentially raising concerns regarding various reliability issues of the gate oxide [142-150]. To reduce the large gate leakage while further scaling equivalent oxide thickness, substitute materials with high dielectric constant (high-k), such as Al_2O_3, HfO_2 and ZrO_2, have been proposed to replace SiO_2 [151-159]. Among these materials, HfO_2 has been considered as one of the most promising substitute materials due to its thermodynamic stability on silicon, its large dielectric constant (25) and reasonable bandgap (~5.7 eV) [153,157-161]. One major difference between high-k dielectrics and SiO_2 is the large amount of traps in the high-k. These traps are believed to be distributed not only at the interface but also inside the bulk dielectric

[162, 163]. However, the exact spatial distribution of these traps is still not clear. Knowing the spatial distribution of the traps is an important part of understanding of the physical nature of the defects and how they affect device properties. The main purpose of this work is to develop a CP method to characterize the spatial distribution of the traps in high-k dielectrics.

6.3 Simulation of the Probable Range in CP Measurement

CP has been used to study interface and near-interface traps in the Si/SiO_2 system for more than thirty years and has been used widely [164-166]. When performing CP measurement, the source and drain are usually grounded or applied with a small reverse bias. Periodic pulses are applied to the gate and drive the channel region into inversion and accumulation conditions periodically [167]. A dc CP current measured from substrate is attributed to the recombination of trapped electrons and holes. If the pulse amplitude (V_a) is kept constant and the pulse base voltage (V_{base}) is swept from flat band voltage (V_{FB}) to threshold voltage (V_{th}) or vice versa, a maximum dc CP current ($I_{CP,MAX}$) will be observed. Conventionally, $I_{CP,MAX}$ is expressed as [168],

$$I_{CP,MAX} = q\, N_{it}\, f\, A_G \quad \text{..(6.1)}$$

where q (coul) is the unit Coulombic charge, f (s^{-1}) is the frequency of the applied pulses, A_G is the effective channel area (cm^{-2}) and N_{it} (cm^{-2}) is the total number of interface traps per area. In this expression, N_{it} is typically considered to be independent of the distance of traps from the interface. This assumption is valid in Si/SiO_2 system for which most traps are located close to the Si/SiO_2 interface and are probed by the CP measurement at moderate frequencies [169, 170]. However, in high-k dielectrics since traps are not only at the interface but also inside the bulk dielectric, traps located away from the interface may not be probed during CP measurement. To include the effect of the spatial distributions of traps to $I_{CP,MAX}$, equation (6.1) is re-written as

$$I_{CP,MAX} = q\,f\,A_G\,N_{mit} = q\,f\,A_G \int_0^{x_d}\int_{E_{min}}^{E_{max}} N_{it}(x)\Delta F(x,E_t)\,dE_t\,dx \qquad (6.2)$$

where N_{mit} is the measured N_{it} during CP measurement and could be expressed as the double integral of the multiplication of N_{it} and an additional term ΔF . ΔF indicates the probability that a trap can be probed by CP measurement and is a function of the distance from the Si-substrate/gate-dielectric interface (x) and the trap energy (E_t). The upper and lower limits of the double integral are the energy range (E_{max} – E_{min}) and the maximum probable depth (x_d) in which traps inside can be probed. It will be shown in the following that ΔF is strongly affected by the parameters of the pulses applied to the gate during CP measurement such as V_a, pulse on/off time (t_{on}/t_{off}), and pulse rise/fall time (t_r/t_f). From equation (6.2) it can also be seen that N_{mit} and $I_{CP,MAX}$ are functions of ΔF and therefore will be affected by the pulse parameters as well. It suggests that different $I_{CP,MAX}$ may be obtained by using different pulse parameters due to different parts of traps been characterized. It is therefore, crucial to understand how ΔF and $I_{CP,MAX}$ are affected by these pulse parameters during CP measurement.

The explicit expression of ΔF can be obtained by considering the capture and emission processes of electrons and holes at traps described in Shockley-Read-

Hall theory [171, 172]. From Shockley-Read-Hall theory, four different possible emission and capture processes can happen to a trapping center at energy E_t: electron capture, electron mission, hole capture, and hole emission. The corresponding rates for these processes are the electron capture rate (c_n), electron emission rate (e_n), hole capture rate (c_p) and hole emission rate (e_p). The overall rate equation can be express as

$$\frac{dF}{dt} = (c_n + e_p) - (c_n + c_p + e_n + e_p) \cdot F \text{.........................} (6.3)$$

where F is the occupancy function and indicates the probability of a trapping center being occupied by an electron (or hole) at any given time t.

To understand how F changes during CP, it is assumed that trapezoidal pulses are applied to the gate as a function of time and the corresponding F values can be found. However, it is noticed that c_n and c_p are functions of the Si substrate Fermi level (E_f) and therefore are functions of time during t_r and t_f [173]. To simplify the problem and obtain an analytic expression of F, both t_r and t_f are assumed to be negligible, which means the trapezoidal pulses are approximated by square pulses. Under this approximation, c_n and c_p are constant and equation (6.3) is a first-order ordinary differential equation. The solution to this equation is

$$F(t) = F(0) \cdot e^{-(c_n + c_p + e_n + e_p) \cdot t} + \frac{(c_n + e_p)}{(c_n + c_p + e_n + e_p)} (1 - e^{-(c_n + c_p + e_n + e_p) \cdot t}) \text{..........} (6.4)$$

where t is the time and t = 0 is defined as the points at which E_f reaches the quasi-steady state condition.

Figure 6.1 illustrates F as a function of time for a square pulse. It can be seen that during t_{on}, F increases from its minimum value to its maximum value; while during t_{off}, F decreases from its maximum value to its minimum value. Since t in equation (6.4) is the time after E_f reaches quasi-steady state, its origin can be assigned at any edges of the square pulse, as shown in Figure 6.1. The maximum and minimum F values can then be expressed as:

$$F_{\max} = F_{\min} \cdot e^{-(c_{n,on}+c_{p,on}+e_n+e_p)\cdot t_{on}} + \frac{(c_{n,on}+e_p)}{(c_{n,on}+c_{p,on}+e_n+e_p)}(1-e^{-(c_{n,on}+c_{p,on}+e_n+e_p)\cdot t_{on}}) \quad ...(6.5)$$

$$F_{\min} = F_{\max} \cdot e^{-(c_{n,off}+c_{p,off}+e_n+e_p)\cdot t_{off}} + \frac{(c_{n,off}+e_p)}{(c_{n,off}+c_{p,off}+e_n+e_p)}(1-e^{-(c_{n,off}+c_{p,off}+e_n+e_p)\cdot t_{off}}) \quad ...(6.6)$$

where $c_{n,on}$ and $c_{n,off}$ are the electron capture rates during t_{on} and t_{off} and $c_{p,on}$ and $c_{p,off}$ are the hole capture rates during t_{on} and t_{off}.

F_{max} and F_{min} indicate the probabilities that a trapping center is occupied by electrons at the end of t_{on}, and t_{off}, respectively. The difference between F_{max} and F_{min} ($\Delta F = F_{max} - F_{min}$) indicates the probability of a trapping center being occupied by an electron and a hole alternatively (electron-hole recombination) during a complete pulse period. In other words, it indicates the probability a trapping center can be probed during CP measurement and contribute to $I_{CP,MAX}$. By using equations (6.5) and (6.6), ΔF can be expressed as

$$\Delta F = F_{\max} - F_{\min}$$

$$= \frac{(e^{(c_{n,on}+c_{p,on}+e_n+e_p)t_{on}}-1)(e^{(c_{n,off}+c_{p,off}+e_n+e_p)t_{off}}-1)(-c_{n,off}(c_{p,on}+e_n)+c_{n,on}(c_{p,off}+e_n)+(-c_{p,on}+c_{p,off})e_p)}{(e^{(c_{n,on}+c_{p,on}+e_n+e_p)t_{on}+(c_{n,off}+c_{p,off}+e_n+e_p)t_{off}}-1)(c_{p,on}+e_n+c_{n,on}+e_p)(c_{p,off}+e_n+c_{n,off}+e_p)} \quad ..(6.7)$$

In the derivation of ΔF, the input trapezoidal pulses are approximated by square pulses and assumed to have zero t_r and t_f. It implies that E_f changes abruptly from the Fermi level at accumulation condition ($E_{f,acc}$) to the Fermi level at inversion condition ($E_{f,inv}$) when the pulse voltage level (V_{top} or V_{base}) switches. Therefore, the time periods for electrons and holes to occupy traps are exactly t_{on} and t_{off} respectively. As for non-zero t_r and t_f, since now E_f changes gradually during t_r and t_f, the surface electron (hole) density increases exponentially during t_r (t_f). Therefore, the "effective" time period for electrons (holes) to occupy traps will be longer than t_{on} (t_{off}). This effect of t_r and t_f on the trap occupancy by electrons and holes will be considered later.

Non-zero t_r and t_f have other effects on ΔF. Ideally, all traps with energy E_t between $E_{f,inv}$ and $E_{f,acc}$ should be able to be probed during CP since E_f is pinned at these two energy levels during t_{on} and t_{off}. However for non-zero t_r (t_f), trapped holes (electrons) with energies close to $E_{f,acc}$ ($E_{f,inv}$) can be emitted to the substrate (source and drain) instead of being recombined. The effective minimum and maximum trap energy between which recombination occurs are then given by equations (6.8) and (6.9) [168]:

$$E_{em,h} = E_i + k\,T\,\ln(v_{th}\ \sigma_p\ n_i\ \frac{|V_{FB} - V_{th}|}{|V_a|} t_r + e^{\frac{(E_F,acc - E_i)}{kT}}) \quad \text{.........(6.8)}$$

$$E_{em,e} = E_i - k\,T\,\ln(v_{th}\ \sigma_n\ n_i\ \frac{|V_{FB} - V_{th}|}{|V_a|} t_f + e^{\frac{(E_i - E_F,inv)}{kT}}) \quad \text{.........(6.9)}$$

where $E_{em,h}$ ($E_{em,e}$) is the effective maximum (minimum) trap energy level, E_i (n_i) is the intrinsic Fermi level (carrier density), v_{th} is the thermal velocity and σ_n (σ_p) is the electron (hole) capture cross section.

On the other hand, the effective carrier capture cross sections are known as functions of x and can be expressed as [169, 174]

$$\sigma_{n/p}(x) = \sigma_{n/p}(0)e^{-\frac{x}{\lambda_{n/p}}} \text{.................................}(6.10)$$

where $\sigma_{n/p}$ (x) is the electron/hole capture cross section at any depth x, while $\sigma_{n/p}$ (0) is the electron/hole capture cross section at the interface and $\lambda_{n/p}$ is the characteristic tunneling distance of electron/hole. By using equation (6.10), equations (6.8) and (6.9) are re-written as

$$\begin{aligned} E_{em,h} &= E_i + k\,T\,\ln(v_{th}\;\sigma_p(0)\;e^{-\frac{x}{\lambda_p}}\;n_i\,\frac{|V_{FB}-V_{th}|}{|\Delta V_A|}t_r + e^{\frac{(E_F,acc-E_i)}{kT}}) \\ &\approx E_i + k\,T\,\ln(v_{th}\;\sigma_p(0)n_i\,\frac{|V_{FB}-V_{th}|}{|\Delta V_A|}t_r) - \frac{kT}{\lambda_p}x \text{....................}(6.11) \end{aligned}$$

$$\begin{aligned} E_{em,e} &= E_i - k\,T\,\ln(v_{th}\;\sigma_n\;(0)\;e^{-\frac{x}{\lambda_n}}\;n_i\,\frac{|V_{FB}-V_{th}|}{|\Delta V_A|}t_f + e^{\frac{(E_i-E_F,inv)}{kT}}) \\ &\approx E_i + k\,T\,\ln(v_{th}\;\sigma_n(0)n_i\,\frac{|V_{FB}-V_{th}|}{|\Delta V_A|}t_f) - \frac{kT}{\lambda_n}x \text{..........................}(6.12) \end{aligned}$$

By combining equations (6.7), (6.11) and (6.12), a 3-D ΔF simulation contour as a function of E_t and x can be plotted as shown in Figure 6.2. Traps located inside the trapezoidal plateau with ΔF equal to one have the maximum probability to be probed and contribute to $I_{CP,MAX}$ during CP measurement. It can be seen that the detectable trap energy range is narrower at the interface and is expanding with x, as described in equations (6.11) and (6.12). It can also be seen that ΔF drops from one to zero at about 8 Å, and it suggests that all traps beyond this depth can not be detected during CP measurement. Therefore, a probable depth during CP measurement can be defined accordingly. It should be reminded that the contour shown in Figure 6.2 depends on applied pulse parameters during CP measurement. Therefore, by changing the pulse parameters different contours can be obtained, as shown in Figure 6.3. Figure 6.3 (a) and (b) show the 2-D simulation contours of ΔF equals to 0.5 with different pulse parameters. In both contours t_{on} is set equal to t_{off} and is equal to 50 ns in (a) while is equal to 1 μs in (b), and the other pulse parameters are kept the same. It can be seen that at lower frequency (longer t_{on} and t_{off}) the probable depth is deeper which suggests that electrons and holes have longer time to penetrate into bulk dielectric to occupy traps at deeper depth and contribute to $I_{CP,MAX}$.

As mentioned earlier, the effect of non-zero t_r and t_f on the derivation of equation (6.7) is to increase the effective t_{on} and t_{off}, and effectively increases the probing depth. However, since the real probing depth is affected strongly by dielectric parameters (which will be shown in the following), this effect on the increase of effective probing depth is not crucial and the ignorance of this effect is valid without affecting the further semi-quantitive analysis.

6.4 Experiment

The devices used in this work are fully processed MOSFETs with HfO_2/SiO_2 stacked gate dielectrics. High-k gate dielectric transistors were fabricated on 200mm p/p+ epitaxial Si <100> wafers using a standard CMOS process with 1000 °C/10 sec dopant activation anneal. The gate stacks were formed by depositing a 3 nm ALD HfO_2 dielectric on various scaled thermal oxide interface layers (IL) created by the controlled etch-back of a 1.9 nm thermal oxide. The high-k film deposition was followed by a 700 ºC anneal in NH_3 ambient, after which, a gate electrode was formed by CVD TiN with poly-Si cap [175].

CP measurement is performed by applying periodical trapezoidal pulses with fixed t_r/t_f and V_a generated by HP8112A pulse generator to the gate. The electron-hole combination dc current is measured from the substrate by using HP4156B semiconductor analyzer. To probe traps at different depth in the dielectric, t_{on} and t_{off} of the applied pulses are kept the same and change from 50 ns to 100 ms. Figure 6.4 shows $I_{CP,MAX}$ as a function of $t_{on/off}$. It can be seen that $I_{CP,MAX}$ decreases with increasing t_{on}/t_{off} and then saturates at long $t_{on/off}$. This saturation indicates that $I_{CP,MAX}$ is dominated by the gate leakage current instead of the electron-hole recombination current. This leakage current limits the maximum probable depth in dielectrics while performing CP measurement. Meanwhile, the measured $I_{CP,MAX}$ at all t_{on}/t_{off} is corrected by using this leakage current to get the $I_{CP,MAX}$ due to electron-hole combination.

6.5 Results and Discussion

One issue associated with this methodology is to get the probing depth from t_{on}/t_{off}. The conversion between t_{on}/t_{off} and x is affected by theoretical values of dielectric parameters such as effective electron/hole mass inside dielectrics ($m_{e/h}$), effective electron/hole barrier height ($\Phi_{e/h}$), $\sigma_{n/p}$ (0), and V_a [169, 170]. This effect is shown in Figure 6.5. Figure 6.5 shows that N_{mit} is plotted as a function of x by using two different sets of parameters. For the open circle, the used parameters are $m_{e/h}$ = 0.5/0.4 eV, $\Phi_{e/h}$ = 3.1/3.8 eV, $\sigma_{n/p}$ (0) = $10^{-14}/10^{-16}$ cm^{-2}, which are the commonly accepted values for pure SiO_2 [176, 177]. For the closed circle, the used parameters are $m_{e/h}$ = 0.1/0.1 eV, $\Phi_{e/h}$ = 1.3/3.3 eV, $\sigma_{n/p}$ (0) = $10^{-14}/10^{-15}$ cm^{-2}, which are the estimated values for pure HfO_2. These values are estimated so that the location of the plotted curve is consistent with the thickness of SiO_2 interfacial layer from fabrication. In both cases V_a is equal to 1.2 V. It can be seen that by using different sets of parameters, the curve is not only shifted but also stretched out along x-axis. Since the device under test has a SiO_2/HfO_2 stacked gate dielectric, it is expected that the real values of these parameters should be somewhere in between the chosen two set values and they should also change with the probing depth. Therefore, the maximum detectable depth range is from end to end of these two curves which is about 1.6 nm as shown in the figure. However, since the accurate values of these parameters are not clear, the depth shown in the x-axis can only be a reference and only semi-quantitive analysis can be provided. Meanwhile, to simplify the analysis and make it easier to compare experimental results from devices with different interfacial layer thickness, parameters with values for HfO_2 will be used for HfO_2/SiO_2 stacked dielectrics in the following analysis.

Figure 6.6 shows N_{mit} at different x for devices with interfacial layer oxide thickness ranging from 1nm to 2 nm. N_{mit} from pure SiO_2 dielectric is also shown for comparison. It should be reminded that N_{mit} (x) is an accumulation function which counts the total number of traps per area from Si/SiO_2 interface to depth x. With that it can be seen that the values of N_{mit} at the smallest x for all curves are very close, which suggests that all dielectrics have approximately the same amount of traps within a shallow depth. These traps are attributed to the commonly observed interface traps at Si/SiO_2 interface. For SiO_2 dielectric, its curve is flat and keep N_{mit} a constant through out the detectable depth range. It suggests no further traps exist inside the bulk SiO_2 which is expected and is consistent with observations from other groups [169, 170]. As for the curves for HfO_2/SiO_2 stacked dielectrics, N_{mit} increases with depth and the value is higher for the dielectric with thinner SiO_2 interfacial layer at the same depth. It suggests that additional traps are generated inside the bulk SiO_2 due to the diffusion phenomena at HfO_2/SiO_2 interface. For the dielectric with thinner interfacial layer, since HfO_2/SiO_2 interface is closer to Si/SiO_2 interface this diffusion is more prominent so that N_{mit} is higher. As for the curve for the dielectric with the thickest interfacial layer (2nm), it shows similar behavior as that observed from SiO_2 dielectric. It suggests that since the interfacial layer is thick, additional traps inside SiO_2 due to the diffusion at HfO_2/SiO_2 are still beyond the probable depth. Therefore, no additional prominent taps are observed in this dielectric.

To get the trap volume density, N_t (cm^{-3}), the derivative of $N_{mit}(x)$ respect to x is taken and the result is shown in Figure 6.7. Since the dielectric with 2 nm SiO_2 interfacial layer does not show prominent additional traps, only dielectrics with thinner SiO_2 interfacial layers are plotted. It can be seen clearly that both devices show that N_t is low at shallow depth, then increases with x and finally tends to saturate. The result suggests that the probing region changes from pure SiO_2 region, passes SiO_2/HfO_2 diffusion region and then reaches pure HfO_2 region. The saturation of N_t in the HfO_2 region may suggest that the trap distribution is relatively uniform. However, this result needs further work to be confirmed. Meanwhile, it can also be seen that the SiO_2/HfO_2 diffusion regions in these two dielectrics are shifted about 4 Å, which is close to the difference between the SiO_2 interfacial layer thickness of these two dielectrics. It suggests that although the accurate probing depth is unknown, the relative trap spatial distribution is accurate.

6.6 Conclusion

From the simulation result it has been shown that N_{mit} during CP characterization is not equal to N_{it} in high-k dielectrics. It is also shown that the probable range of traps in the dielectrics is affected by pulse parameters. The results are essentially important while comparing experimental results from different electrical characterization techniques. The results are also helpful to understand which portions of traps been probed while study the properties of traps in high-k dielectrics. By using this methodology, trap spatial profiles in the SiO_2/HfO_2 stacked dielectrics with different SiO_2 interfacial layer thickness are also shown in this report. The results clearly showed the change of N_t from SiO_2 layer to SiO_2/HfO_2 diffusion region and reaches HfO_2 layer. Although the accurate depth of traps are not clear due to the undetermined theoretical dielectric parameters, the relative shift of the trap profile is consistent with the difference of the interfacial layer thickness in different SiO_2/HfO_2 stacked dielectrics. It suggests that this methodology is accurate and reliable.

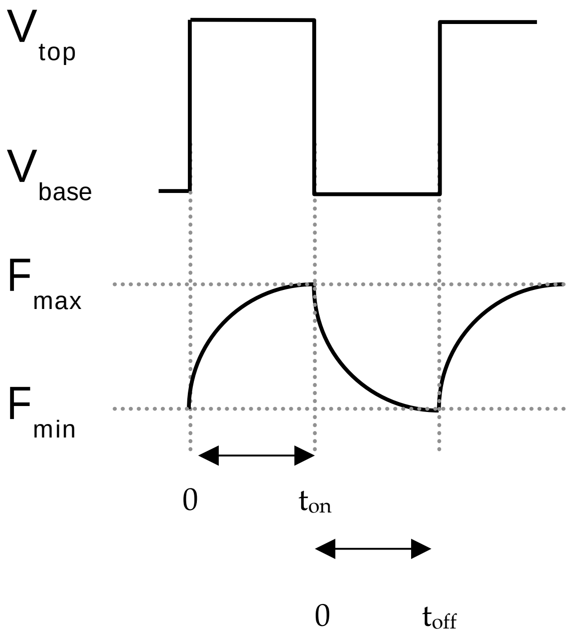

Figure 6.1. Illustration of the change of F value with respect to a square pulse.

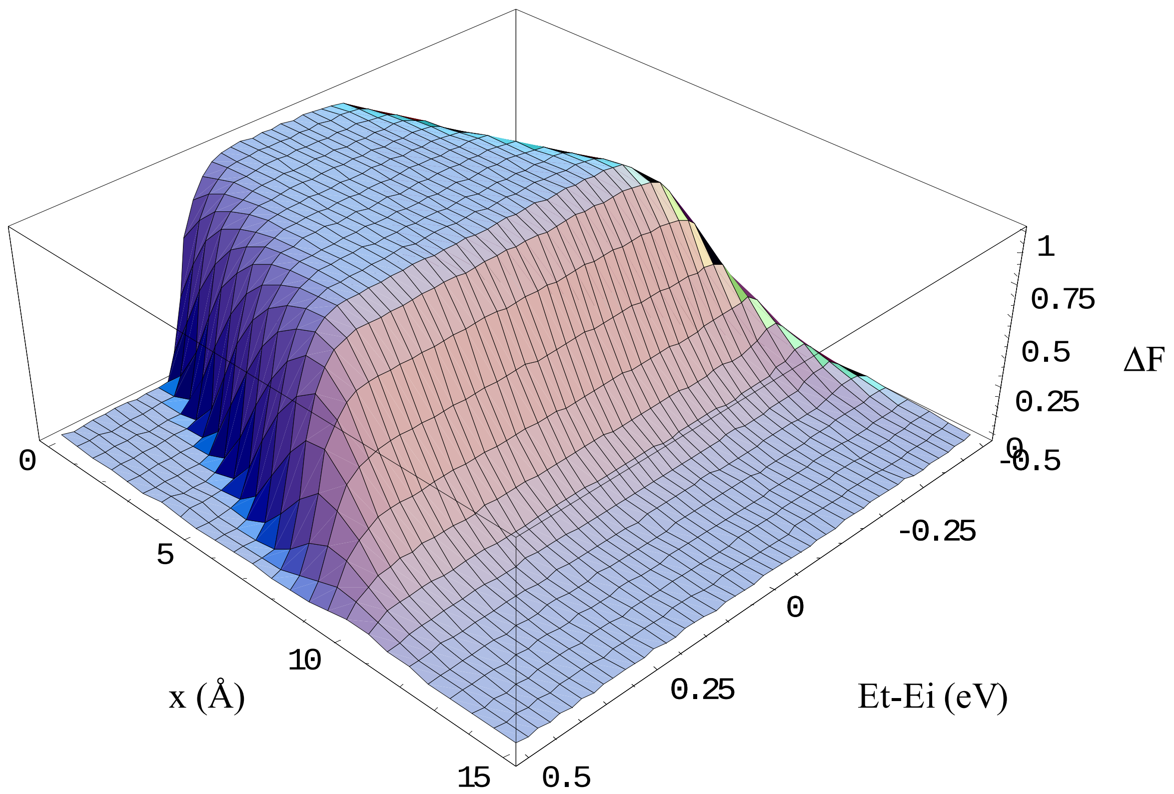

Figure 6.2. 3-D ΔF contour simulation result. ΔF is equal to one within the trapezoidal plateau that indicates the region having the maximum probability been probed.

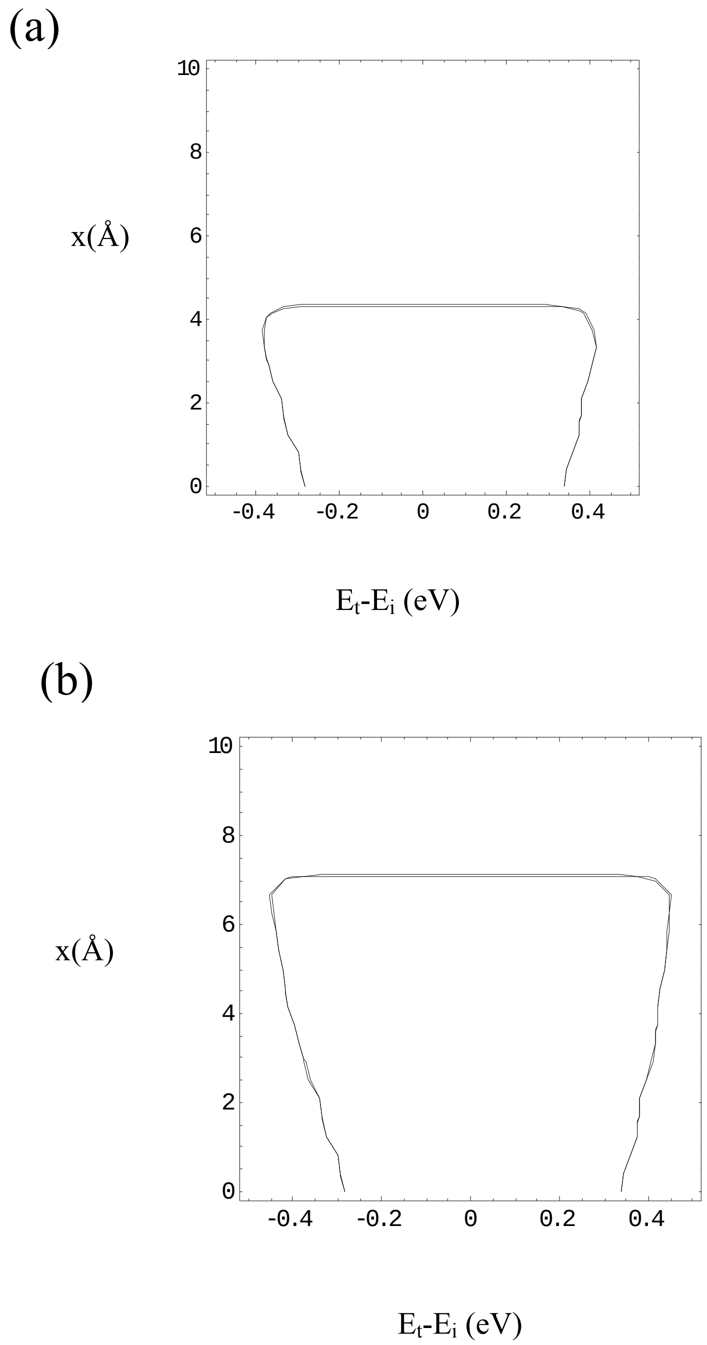

Figure 6.3. Simulation results of pulse parameters dependence of ΔF contour. In (a) both t_{on} and t_{off} are equal to 50 ns, while in (b) both t_{on} and t_{off} are equal to 1 μs. All the other pulse parameters are the same in both diagrams.

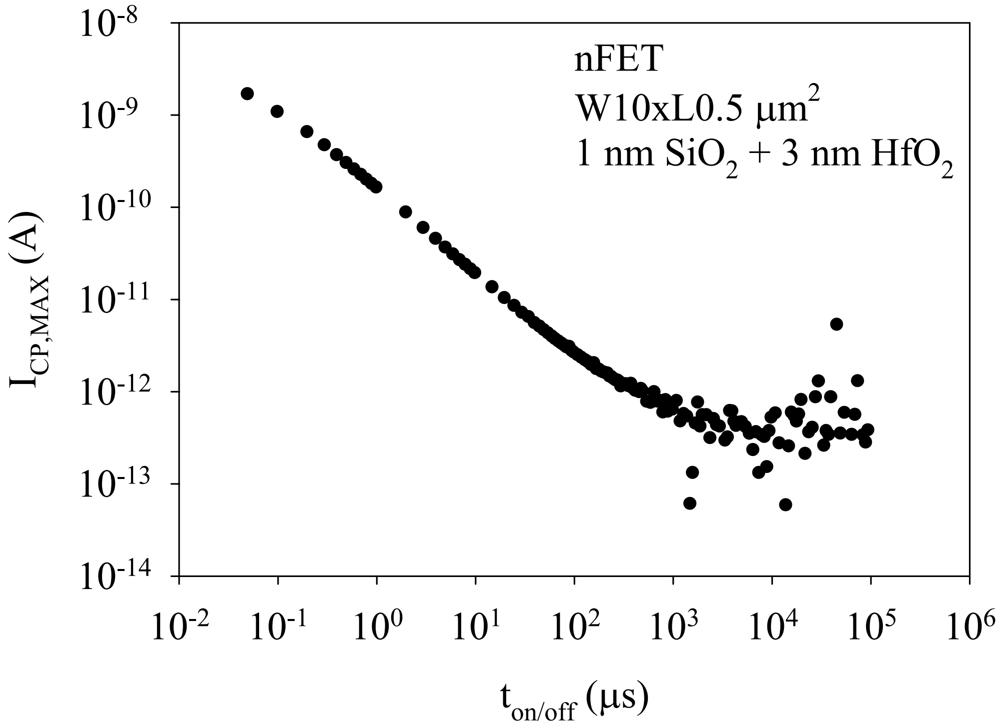

Figure 6.4. $I_{CP,MAX}$ is proportional to frequency. When frequency decreases, $I_{CP,MAX}$ tends to saturate. This saturation indicates $I_{CP,MAX}$ is dominated by gate leakage current instead of electron-hole combination current

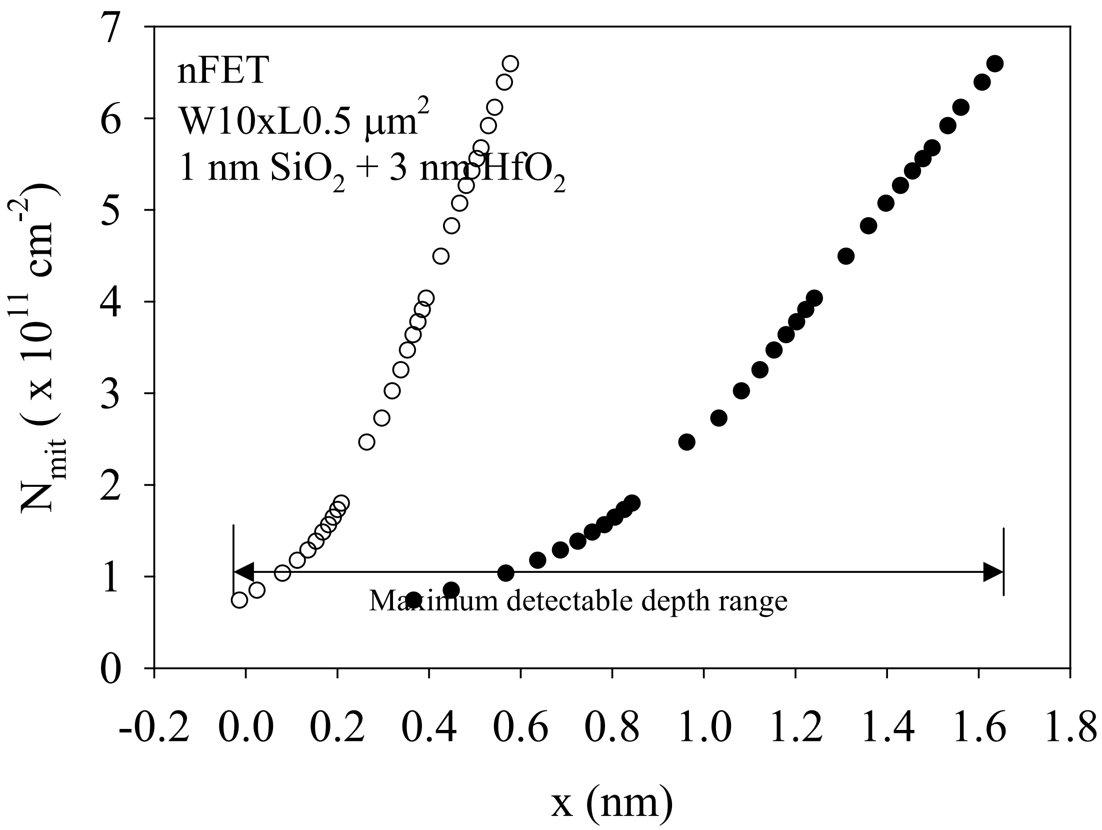

Figure 6.5. The probing depth calculated in this methodology is strongly affected by dielectric theoretical values. For the open circle, the used parameters are $m_{e/h}$ = 0.5/0.4 eV, $\Phi_{e/h}$ = 3.1/3.8 eV, $\sigma_{n/p}$ (0) = $10^{-14}/10^{-16}$ cm^{-2}, which are the commonly accepted values for pure SiO_2. For the closed circle, the used parameters are $m_{e/h}$ = 0.1/0.1 eV, $\Phi_{e/h}$ = 1.3/3.3 eV, $\sigma_{n/p}$ (0) = $10^{-14}/10^{-15}$ cm^{-2}, which are the estimated values for pure HfO_2. In both cases V_a is equal to 1.2 V

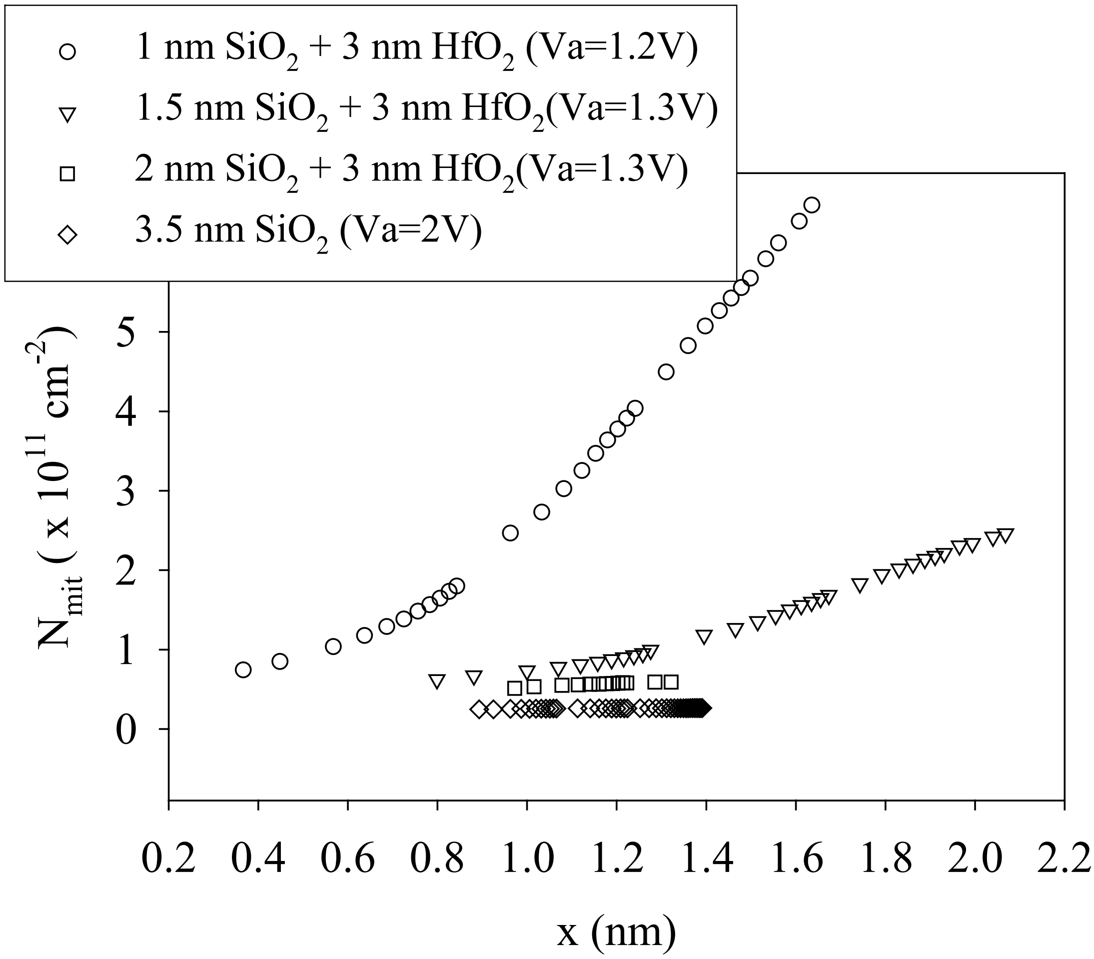

Figure 6.6. The comparison of N_{mit} in dielectrics with different thickness of SiO_2 interfacial layer. It can be seen that at the same depth N_{mit} is higher for the dielectric having thicker interfacial layer. As for SiO_2 dielectric, N_{mit} is constant which indicates no further traps exist in bulk dielectric

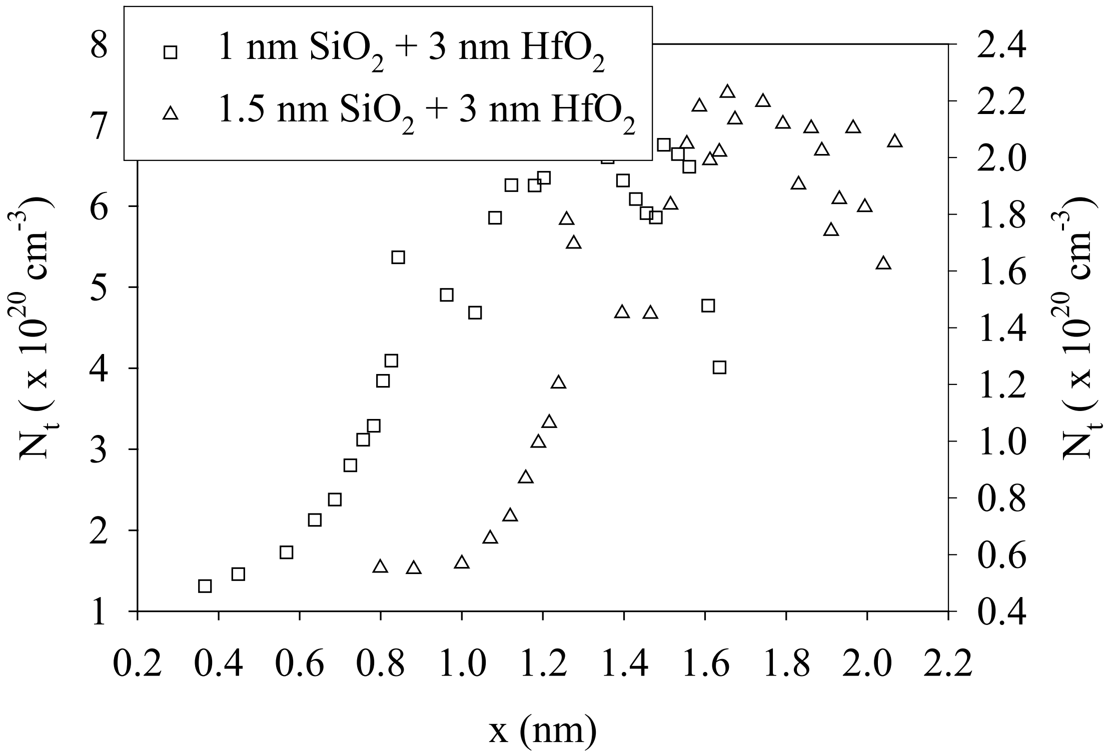

Figure 6.7. The comparison of N_t in dielectrics with different thickness of SiO_2 interfacial layer. The pure SiO_2, SiO_2/HfO_2 diffusion and pure HfO_2 regions can be identified clearly in both dielectrics

Chapter 7

Summary and Future Work

7.1 Overview

Electrical characterizations on both ultra-thin SiO_2 and SiO_2/HfO_2 stacked dielectrics from various aspects are performed in this research work. The goal of this chapter is summarize important results from previous chapters in this dissertation. Possible further extended work will also be discussed in this chapter.

7.2 Summary

In this research work, the generation of electrical active defects in SiO_2 dielectrics during stresses has been characterized from different aspects. It is found that different electrical defects may be generated during CVS and SHH injection. This conclusion is supported by the observation that the Weibull slope for hot-hole-to-breakdown is much larger than that for Q_{bd} during CVS. It is also supported by the other observation that pre-injected hot holes do not contribute to dielectric degradation during the subsequent CVS.

It is also shown in this work that critical reliability parameters such t_{bd} can be extrapolated from accelerated test condition to device normal operating condition by using P_g value. However, since P_g is not a constant during stress, this extrapolation should be done by using P_g value in the linear generation regime. Although the real mechanism causing the non-constant P_g is still not well understood, it is shown that the change of defect capture cross section can not explain this phenomenon.

Meanwhile, the dominant mechanism that causes V_{th} shifts in both n- and p-channel MOSFETs are also investigated in this work. From both experiment and simulation results, it is found that channel mobility degradation is the main mechanism that causes this shift. Therefore, commonly accepted idea that V_{th} shift is due to the Coulombic charge accumulation at the interface is not accurate. This result also indicates that oxide degradation model based on Coulombic charge accumulation may not be accurate.

The electrical characterization on high-k dielectrics in this work was focus on the properties of the initial traps in high-k dielectrics. A methodology based on 2-level CP measurement with various frequencies was used to revel the spatial profile of these traps. From measurement results, the spatial profile of traps in the SiO_2 region, SiO_2/HfO_2 diffusion region and HfO_2 region in the stacked dielectric are clearly identified. Although the exact probing depth in this methodology may not be accurate due to the unknown theoretical dielectric parameters, the correlation between the shift of SiO_2/HfO_2 diffusion region and the difference of the interfacial layer thickness of stacked dielectrics demonstrate this methodology is accurate and reliable.

7.3 Future work

Electrical defect generation in SiO_2 dielectrics has been studied extensively in the past a few decades. Although there is still no conclusive mechanism to describe the degradation process during electrical stresses, it is generally accepted that the generation of energetic carriers (holes or hydrogen species) are the dominant factor. Therefore, continuously focus on how these two species are generated and contribute to oxide degradation during various stress conditions such as CVS, SHH injection and negative bias temperature instability (NBTI) stress will be helpful to construct the whole picture of the physics behind the gate oxide degradation.

Meanwhile, the understanding of oxide degradation process in SiO_2 dielectric will also provide helpful information in studying the defect generation mechanisms in high-k dielectrics. Although there are sill many unknowns about high-k dielectrics, there is no doubt that high-k dielectrics such as HfO_2 will be used to replace SiO_2 in MOS devices in the future based on the need from industry. Therefore, it is expected that more research effort will be put into the filed of studying high-k dielectrics in the future. The future topics in high-k dielectrics shall include not only characterizing and improving the quality of high-k dielectrics but also understanding the defect generation in high-k dielectrics during electric stresses. It would be interesting and crucial to understand how high-k dielectrics degrade during electrics and how it is compared to SiO_2 dielectric. By comparing the characterization results from SiO_2 and high-k dielectrics, it can provide more information of electrical defect generation and oxide degradation in dielectrics.

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