ABSTRACT

Title of Dissertation: FORCE SENSING BY ELECTRICAL CONTACT RESISTANCE IN SOI-DRIE MEMS

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MEMS force sensors employ microfabricated elements to convert applied external forces to electrical signals, typically by piezoelectric, piezoresistive, or capacitive transduction. While existing force sensors based on these sensing principles have commercial success, system dynamics inherent to displacement and strain-based sensing can limit force and frequency ranges. This work explores an alternative force-sensing principle in silicon-based MEMS devices that exploits changes in electrical contact resistance (ECR) during loading between two silicon surfaces, with the aim to determine if ECR can be used to sense force in SOI-DRIE microsystems containing only Silicon and bond pads.

While several analytic models were combined to create an ECR-force model for predicting ECR-force sensitivity in systems containing differing contact geometry, topology, and electrical properties, experimental testing is the focal point of this work. The feasibility of using ECR to sense force in bare DRIE silicon contacts is initially evaluated using force applied by

simple thermal actuation, which indicated that ECR behavior during applied cyclic loading was erratic and occasionally nonmonotonic with increasing load, while absolute contact resistance varied significantly chip-to-chip (200 Ω – 15 kΩ) and increased asymptotically as contact was removed. Results from further investigation using manual spring elongation show a consistent pre-load of at least 5 mN is critical to obtaining repeatable ECR-force curves, "break-in" cycling is required prior to consistent ECR-force behavior, and sidewall fracture occurs in 100 µm line contacts with radii less than 50 µm. Results from testing of packaged chips through inertial acceleration of embedded proof masses show that minimizing contact area during line contact loading reduces relative standard deviation (RSD) and increases sidewall fracture. When normalized to initial contact resistance, chips subjected to inertial loading exhibited linearized sensitivities of 2.0 %/mN and 2.1% hysteresis, with 1.6% RSD.

The use of DRIE, as opposed to additive poly-Silicon-based fabrication, allows a tailorable force range through proof mass sizing and aspect ratio changes, adjustable pre-load through simple design, and integration of an ECR force sensor into existing systems. The successful use of a proof mass to apply force by acceleration indicates ECR between SOI-DRIE interfaces is a viable method to measure acceleration in the future. As with piezo-sensors, calibration of ECR force sensors is expected to improve chip-to-chip repeatability. Compared to commercially available force sensors, the realized ECR force sensor has several advantages (smaller size, lower force range, and simpler fabrication) that may be further leveraged in future development.

FORCE SENSING BY ELECTRICAL CONTACT RESISTANCE IN SOI-DRIE MEMS

by

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Chapter 1: Introduction

Implementation of microelectromechanical systems (MEMS) and the continued evolution of microelectronics has led to the emergence and rethinking of many applications that were once out of reach. Previously impractical products like powered in-situ medical devices, affordable wearable consumer electronics, power-efficient motion tracking devices and micro-scale hybrid sensor suites have emerged as consumer-ready technologies thanks in large part to advancements in new sensing techniques. Among the most common sensing methods in MEMS include accelerometers, gyroscopes, and force sensors. MEMS force sensors employ microfabricated elements to convert applied external forces to electrical signals, where sensing is typically based on capacitive, piezoelectric, or piezoresistive transduction [1].

This work explores an alternative force sensing principle [2] in silicon-based MEMS devices that exploits changes in electrical contact resistance (ECR) during loading between two silicon surfaces. The objective of this work is to determine whether electrical contact resistance can be used to sense force in SOI-DRIE microsystems containing only Silicon and bond pads. Specifically, this work contributes the following to the field:

- Demonstration of sensing force using ECR in SOI-DRIE MEMS
- Characterization of the sensitivity and reliability of a realized ECR-force sensor versus contact force, contact shape and pre-load force in contacting DRIE surfaces
- Characterization of surface fracture in contacting DRIE surfaces versus applied contact force and contact shape in the presence or absence of pre-load
- Development and demonstration of sensing acceleration using ECR in DRIE-SOI MEMS

- Design of three independent tailorable microsystem architectures, and associated design guidelines, for further development of a realized ECR force sensor

1.1 Motivation

MEMS force sensors employ microfabricated elements to convert applied external forces to electrical signals, with transduction typically based on capacitive, piezoelectric, or piezoresistive mechanisms [1]. Capacitive force sensors are displacement-based sensors that are ubiquitous in MEMS applications [3,4], where a physical displacement between conductive elements resulting from an input force produces a change in capacitance that is converted into an output signal. In contrast, piezoresistive and piezoelectric force sensors are strain-based sensors, where strain within the material itself generates a change in resistance or charge, respectively, allowing these sensors to operate over large frequency and force ranges [5,6]. While these sensors have found commercial viability, the use of exotic or rate-sensitive materials with architectures that require complex fabrication limits application, particularly in scaled down or dynamic systems, and results in relatively expensive devices.

In an electrical contact resistance-based sensor, the change in electrical resistance is dictated by the number of contacting nano-asperities, which vary proportionally with elastic surface stress at the contact interface, and is therefore inherently rate insensitive. The change in the contact area, a, within a contacting interface is related directly to the applied force, F, using Hertzian contact where the applied contact pressure $P = F/A$. In high-G environments where reliability of many MEMS devices is still unknown [7,8], rate-independent sensing may allow valuable enhancement of sensor bandwidth.

Understanding the nature of the ECR mechanism in SOI-DRIE MEMS will enable future development of novel microscale force sensors that may be realized using a simple and low-cost

batch fabrication process. Additionally, the introduction of an entirely new sensing principle presents the opportunity for a variety of unforeseen creative developments.

1.2 Background of ECR as a sensing mechanism

ECR as a sensing mechanism was first reported in non-destructive flaw detection [9], and later to measure strain in carbon fiber-reinforced concrete [10]. Fibers of 10 μm diameter were strain-cycled under pressures up to 1.2 MPa within a surrounding concrete matrix, expanding and reducing contact resistance during push-in, and shrinking and increasing resistance during pull-out. Strain sensitivity was high, and fully reversible if kept under half the yield stress. ECR was later investigated in multi-stranded fiber conductors to better predict conductivity [11].

The robotic community has investigated tactile force sensors relying on electrical contact resistance to simultaneously sense force and location as input to a robotic feedback system. Force sensors in these applications are typically produced at the macro-scale using layered thick films fabricated with screen-printing, and packaged using pastes and tape [12,13]. Although not MEMS devices, measurement of ECR in tactile force sensors typically uses a simple voltage divider circuit, and has been shown to show average standard deviation as low as 3%, without the need for adhesives prior to force measurement [12].

Force sensing resistors (FSRs) are pervasive throughout the electronic and music industries as inexpensive methods to sense force and pressure [14]. FSRs are typically comprised of two polymer films, one a conductive surface and the other printed with an electrode pattern that faces the conductive surface. With increasing applied force and therefore increasing contact area between the two polymers, patterned electrodes make successive contact with the conductive layer, discretely reducing overall path resistance with increasing applied force.

Commercial FSRs can experience significant hysteresis and drift (> 17% [14]), although are well-suited for low-cost and low-accuracy applications.

1.3 Background of ECR in MEMS

Electrical contact resistance in MEMS is predominantly investigated within the realm of MEMS relays and micro-switches. Electrical contact resistance is critical in MEMS relays and other devices that rely on repeated contact between surfaces whose electrical properties must be precisely characterized. ECR has been thoroughly investigated to minimize its effects in conductors, and maximize its effects in insulators for use in relays and RF-MEMS [15], but there have been no efforts to treat ECR as a variable and controllable sensing mechanism.

Although not explicitly investigated as a sensing mechanism, the ECR effect has been studied at the microscale using surface micromachined thin film polysilicon MEMS structures [16] for use as a nondestructive diagnostic tool for MEMS contact interfaces. A capacitive parallel plate actuator pulled polysilicon electrodes into contact, monotonically and cyclically, without pre-load, under contact pressures up to 700 kPa. Contact resistance between polysilicon surfaces decreased with increased apparent contact pressure due to an increase in real contact area. Hysteresis was attributed to contacting nano-asperities undergoing varying pile-up or sink-in behavior during increasing and decreasing force. Cyclic loading produced highly erratic ECR behavior despite post-cycling surface imaging revealing only nanoscale surface polishing, indicating inconsistent contact between surfaces. As this was an investigation into using ECR as a non-destructive diagnostic tool, no characteristic behavior relating ECR and applied force was identified.

1.4 ECR-force sensing in DRIE MEMS

For applications in MEMS-based sensing, high aspect ratio patterning of single crystal silicon by deep reactive-ion etching (DRIE) of silicon-on-insulator (SOI) wafers offers several important advantages over polysilicon surface micromachining, including the realization of larger masses, compliant structures with higher out-of-plane stiffness, and structures with nearly vertical sidewalls process. To harness ECR as a sensing mechanism for DRIE structures, an improved understanding of the contact resistance of single crystal silicon surfaces processed by DRIE is needed. While DRIE has been widely employed for the fabrication of sensors utilizing capacitive or piezoresistive sensing, the ECR effect in contacting DRIE structures as a method to sense an external force has not yet been explored. To address this, this work investigates the sidewall contact resistance of high-aspect ratio silicon-silicon interfaces fabricated by SOI/DRIE as a function of contact force. Rather than employing miniature load cells or force sensing probes, *in situ* force methods were employed to characterize ECR-force relationships in fabricated devices. Using three independent methods to apply force between the mating DRIE surfaces, namely direct mechanical probing, direct actuated probing, and inertial loading, the impacts of loading constraints and contact interface geometries on the repeatability and sensitivity of ECR in DRIE microstructures were evaluated. Understanding the nature of the ECR mechanism in DRIE MEMS will enable the future development of novel microscale force sensors that may be realized using a simple and low-cost batch fabrication.

Depicted below in Figure 1-1, the sensing principle is shown using (left) a mechanical probe to apply force and (right) an accelerated inertial mass to apply force. In the former, a manually-actuated probe pulls the released frame downward until the contacting interfaces are touching. Further probe displacement causes the bottom set of springs, which apply the measured

force and are defined by stiffness k, to elongate. Elongation is then measured using an internal Vernier gauge to infer applied force.

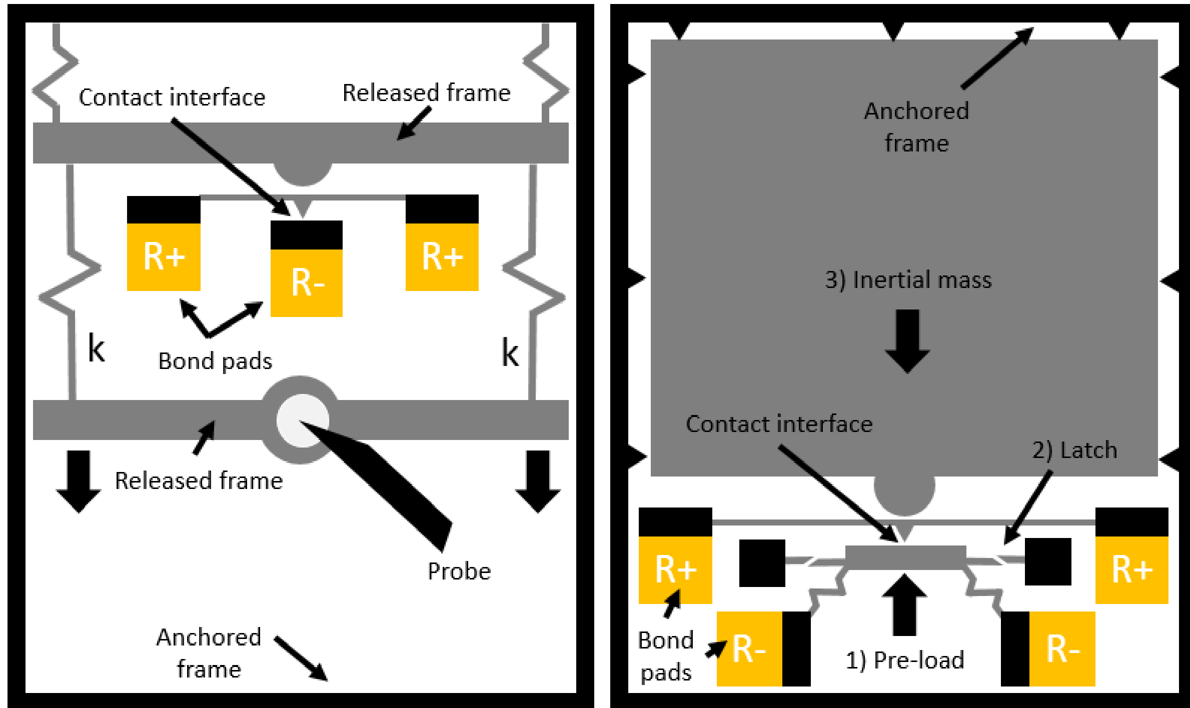


Figure 1-1. (Left) schematic of probe applying contact force between two interfaces via elongation of springs with stiffness k, and (right) schematic of an inertially accelerated mass used to apply force. Resistance is across the contact interface, between R+ and R.

Chips relying on an inertially accelerated mass operate by first manually displacing the bottom structure upwards until it latches, applying a pre-load to the contact interface. Upon latching, contact is also made between the inertial mass and the contact interface. Downward acceleration of the inertial mass causes an increase of contact force at the interface. In both cases, a change in the contact force results in a corresponding change in ECR. In the case of the accelerated inertial mass, the size of the proof mass can be scaled to target a different force regime.

1.5 Dissertation Outline

Chapter 1 discusses the motivation behind using ECR as a sensing mechanism in SOI-DRIE MEMS, the background of ECR as a sensing mechanism and in MEMS, and describes the methodology for obtaining ECR measurements as a function of contact force.

Chapter 2 details the combination of an existing electrical contact resistance model as a function of nano-asperity contact with macro-scale line-on-cylinder contact to determine expected ECR-force output. Analytic and finite element models are used to determine the stiffness of folded serpentine springs and pre-load mechanisms.

Chapter 3 discusses the detailed and iterative design process and experimental methods used for each force application method.

Chapter 4 discusses the microfabrication procedure and related issues.

Chapter 5 details the experimental calibration of spring stiffness and results of experimental testing, citing analysis, imaging and knowledge gained through the process. A characterization of ECR versus force is provided for each method of force application and compared to results from modeling.

Chapter 6 discusses the contact interface topology of tested chips and their mating behavior, fracture and wear at contact interfaces during low-cycle testing, and provides expected fracture behavior of line contacts with varying radius and line contact length.

Chapter 7 concludes with a summary of the knowledge gained, a comparison of the investigated ECR force sensor versus a comparable commercial-off-the-shelf force sensor, and a comparison to existing accelerometer transduction methods.

Chapter 2: Modeling

Prior to designing micromechanical systems for force application, several models were utilized to determine suitable force ranges for each system, and predict how design and fabrication parameters were expected to effect overall ECR-force behavior in line and area contacts. Micromechanical system elements (springs, thermal actuators, pre-load mechanisms) used in the three forcing systems were modeled separately.

Material properties, electrical properties, topology parameters, and geometric parameters are listed below in Table 2-1. Note that specific geometric parameters for each following plot from the ECR-force model are denoted in captions.

Table 2-1. Properties and parameters used during modeling and throughout this work.

SILICON MATERIAL PROPERTIES (BULK, BORON-DOPED)		
Description	Variable	Value
Young's Modulus*	E	125 GPa
Poisson's Ratio	ν	0.27
Density	ρ	2329 kg/m^3
* for bulk doped Si at 15mN loading [42]		
ELECTRICAL PROPERTIES		
Insulator thickness	t	7 - 9 Å
Measurement current	I	1 mA
Measurement voltage	V	< 1 V
Barrier height	φ_0	5 eV
SURFACE TOPOLOGY PARAMETERS		
Fractal roughness	G	Rq^2
Fractal dimension	D	2.2 - 2.3
fractal scaling parameter	γ	1.5
constraint factor	c	2.8
Root mean squared roughness	R_q	0.1 - 0.4 µm
GEOMETRIC PARAMETERS		
Contact type	-	line-on-cylinder
Contact radius	r	5 - 100 µm
Line contact length	l	15 - 100 µm
Contact force	F	5 - 35 mN

2.1 ECR-force

The following combined analytical model assumes full line contact between contacting surface interfaces, perfect alignment and perpendicularity along the entire line contact length, constant native oxide layer thickness (e.g. oxidation has stopped occurring), and identical surface roughness at all contact radii, and does not account for varying small-scale and large-scale roughness caused by DRIE scalloping atop the nominal surface roughness. Many of these

parameters are constantly changing in a real-world scenario, and as such, this model is intended for use as a first-order approximation.

A schematic of the contact interaction is below in Figure 2-1.

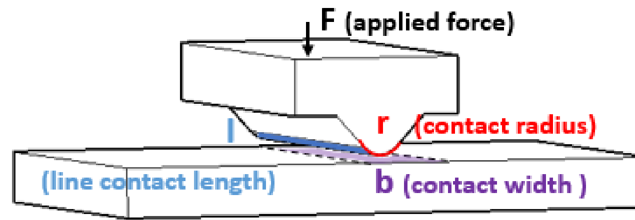


Figure 2-1. Modeled macro-scale cylinder-on-plane contact schematic representative of all modeling. Note this model assumes full contact and perfect alignment along the entire line contact length.

Several existing analytical models were combined into a hybrid ECR-force model to allow prediction of ECR in macro-scale contacting cylinder-on-plane geometries found in this work. The Greenwood-Williamson model for determining equivalent mechanical properties of two contacting surfaces separated by an insulating film is combined with fractal surface modeling to express contact surface topology in terms of truncated real contact area [17]. Hertzian theory for cylinder-on-plane geometry for a given contact radius is used to determine the apparent contact area under a given load, as well as determine the conditions of loading under which the yield strength of Silicon is exceeded, and fracture is expected [18]. Electrical contact resistance for a single microasperity under elastic to fully plastic deformation is integrated over the full contact surfaces to give an expected electrical contact resistance for a given contact force.

2.1.1 ECR between rough surfaces

A general contact model for DRIE surfaces covered with a native oxide film is needed to describe the current flow through micro-asperities at the contact interface. When two conductive surfaces are separated by a sufficiently thin insulating film, current flow can occur through quantum tunneling. Simmons [17] developed a set of tunneling equations to estimate the electrical tunneling resistance between two conducting surfaces with an insulating film barrier with a generalized shape for all applied voltage levels. However, these relationships do not account for the physical behavior of the micro-contacts. Greenwood and Williamson [19] developed a separate model to represent the contact interaction of two rough surfaces as the equivalent of one rough surface in contact with a smooth flat half-space with a reduced effective modulus. Identical insulating films atop the contacting surfaces can then be represented as a single film with thickness $t = t_1 + t_2$ [20]. For very thin films ($t < 50$ Å), the contact mechanics of the film layers can be considered negligible compared to the underlying bulk material mechanical properties [21]. It is also assumed that surface interactions occurring at the contacting spherical asperities are sufficiently separated, thereby neglecting the asperity interactions as secondary [22].

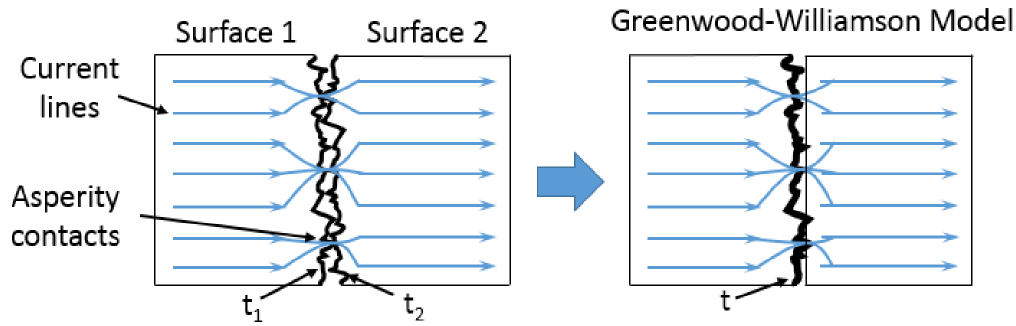


Figure 2-2. Schematic of two contacting DRIE surfaces covered with insulating layers of thickness t_1 and t_2, and the equivalent Greenwood-Williamson model with a single insulating layer of thickness $t = t_1 + t_2$ [20].

2.1.1.1 Fractal surface representation

Through the combination of the Simmons and Greenwood models and representing rough surfaces with fractal geometry, a general ECR model exists for conductive rough surfaces separated by a thin insulating film for elastic, elastic-plastic and fully plastic deformation of the micro-contacts over the full voltage range [20]. Fractal geometry allows representation of a rough surface using two primary parameters, fractal roughness, G, and fractal dimension, D, to describe a fractal surface. The fractal roughness is a height scaling parameter independent of frequency, and the fractal dimension represents the frequency component of the surface. Increasing fractal roughness G increases the height differential between peak and valley, while increasing fractal dimension D increases the number of peaks and valleys in a given surface area. A detailed explanation of the generation of fractal surfaces can be found elsewhere [23–25]. Fractal surfaces are common in topology rendering, and can be easily modeled in MATLAB. To create an accurate fractal representation of the DRIE surfaces in this work, average surface

roughness of the DRIE sidewalls of several chips was first measured by optical profilometry (FRT MicroProf 300, Figure 2-3) using X-Y resolution of 0.25 µm/pixel.

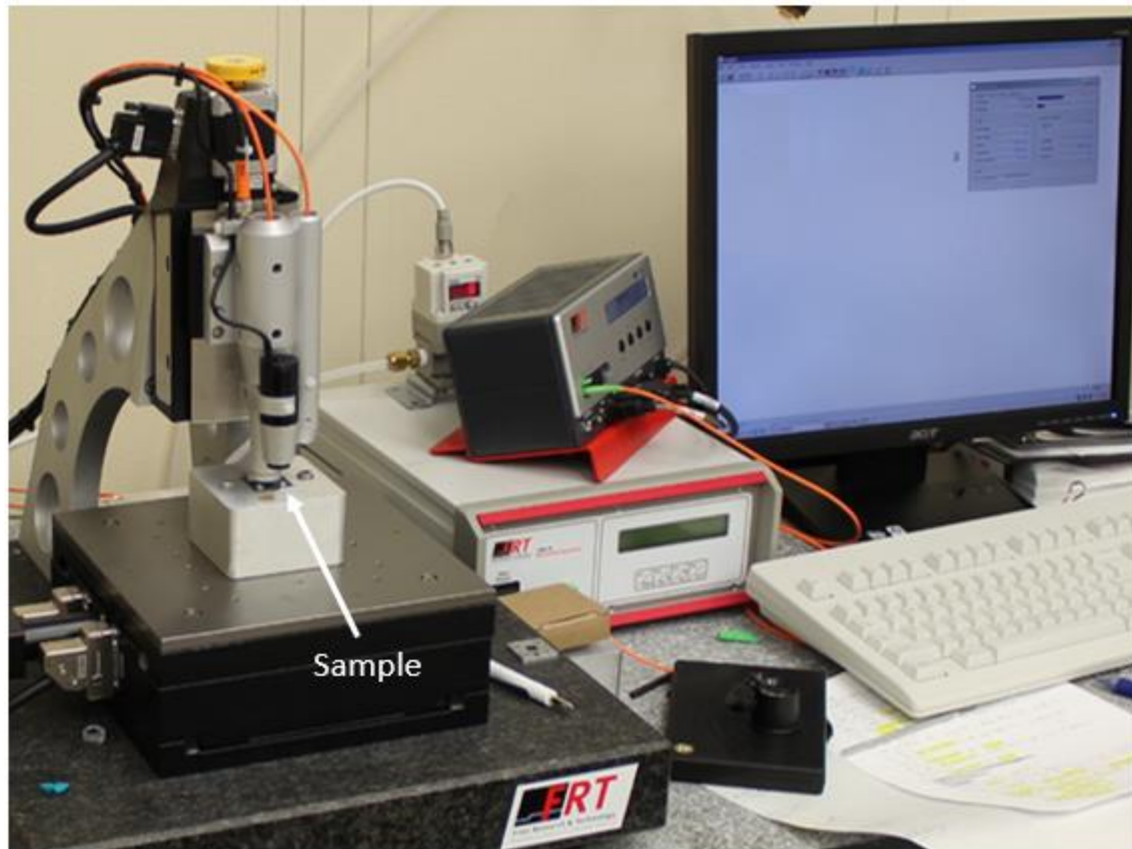


Figure 2-3. FRT measurement setup for obtaining DRIE contact surface topology and roughness parameters.

After applying 3-point surface normalization to account for the mount angle of the test sample, root-mean square roughness, R_q, was measured along the thickness of samples that corresponds to the direction of line contact length (Figure 2-4).

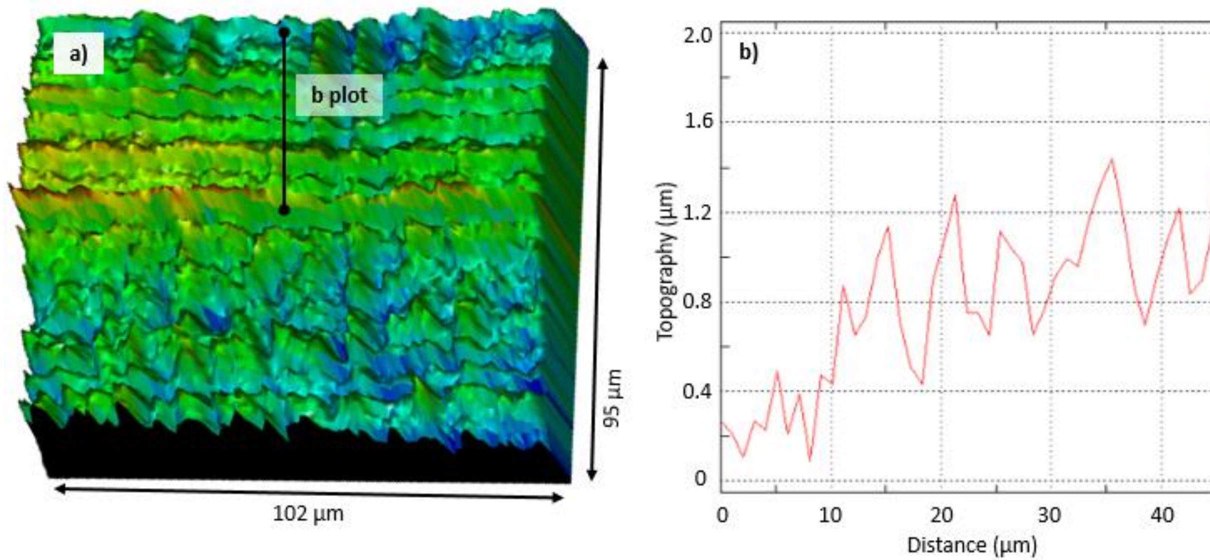


Figure 2-4. FRT surface scan images of the full device layer (100 µm) of a cleaved chip, showing a) typical DRIE sidewall topography and b) roughness profile along the thickness of the interface in the same direction that scalloping occurs. Note that this is the roughness prior to cycling. Roughness after force cycling is expected to vary with applied force, number of cycles, orientation of interfaces, pre-load, and rigidity of constraints.

Root-mean square roughness, R_q, was found to range between 0.1 µm to 0.4 µm along the thickness of the sample where the roughest surface occurs (across DRIE scallops). Because surface topologies were highly non-linear and the actual mating behavior was difficult to predict, average representative surface roughness was determined by using several different values for fractal dimension D. Fracture surfaces of varying D values were generated to represent DRIE surfaces with $G = R_q^2$, length of the topography, L_q, equal to 20 µm, and 128 pixels in x and y (Figure 2-5).

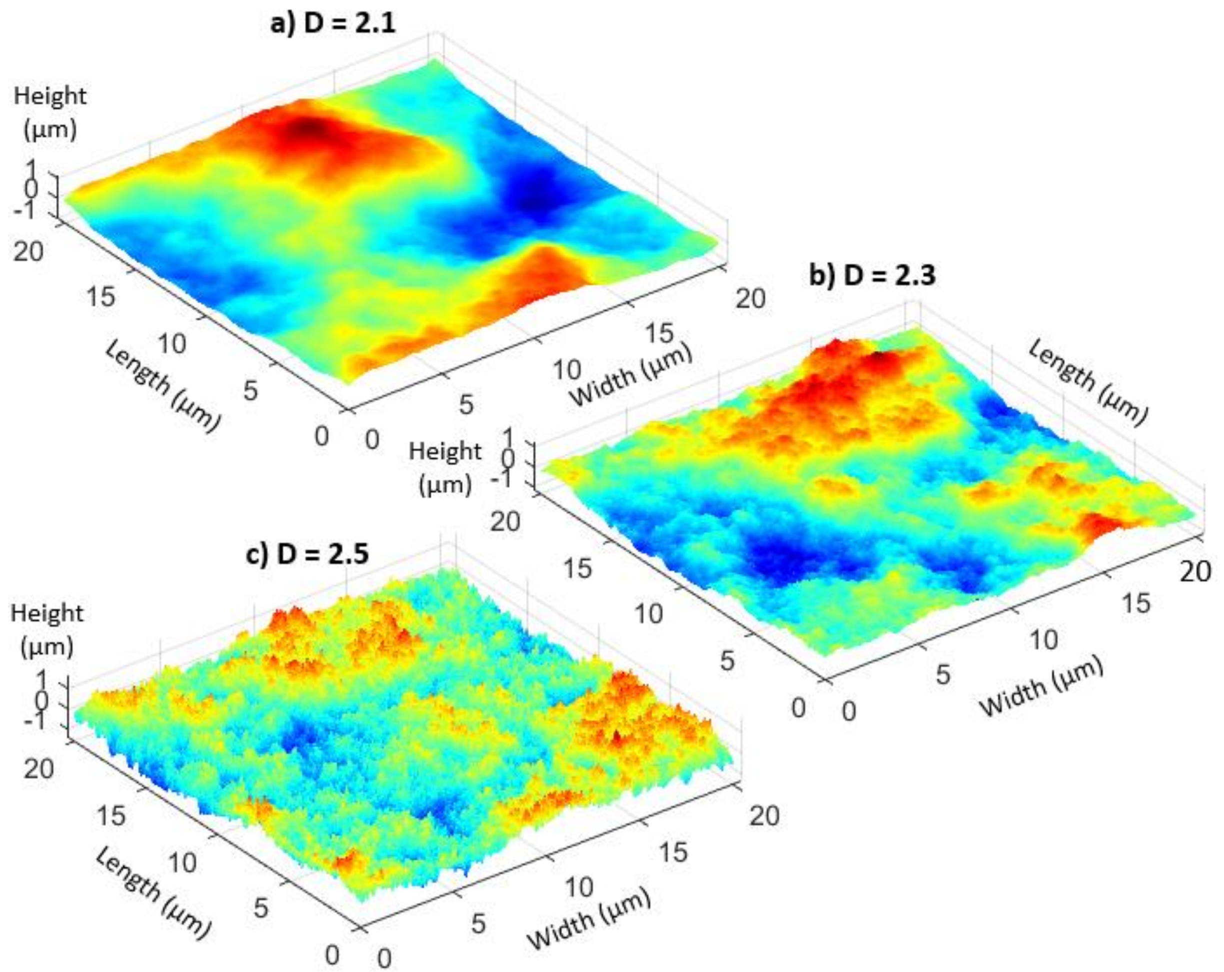


Figure 2-5. Fractal geometry plots for varying fracture dimension, showing a) D = 2.0, b) D = 2.4, and c) D = 2.8. R_q was equal to 0.2 μm in all cases. The final ECR model used D = 2.3 to most accurately represent DRIE surfaces. Note that these surfaces do not include the asymmetry created from DRIE scalloping, and instead assume the same roughness in each surface. Future modeling may benefit from including the effects of scalloping, but curving non-linear sidewalls experienced during DRIE overshadowed this.

2.1.1.2 Conduction through contacting asperities

For fixed current flow and small voltages, it was found that the relationship between real contact area and the ECR of two contacting flat surfaces is independent of the contact load, surface topography and mechanical properties of the contacting surfaces, and dependent on the properties of the insulating film and the portion of contact area between nano-asperities that overlaps [20], which is referred to as the truncated contact area. The total real contact area at the interface is then the sum of the discrete truncated contact areas of each asperity, and the total ECR is the sum of each individual parallel tunneling resistance of said asperities [20]. Note that although ECR is described as independent of the contact load, the truncated contact area varies with applied load, which in turn varies ECR.

For conductive rough surfaces separated by a very thin insulating film, a single microcontact asperity of area a_i, covered by a thin insulating film of thickness t, dielectric contact K, and energy height above the Fermi level of the conductive surfaces, φ_0, experiences a current intensity, I_i, and voltage drop, V_i, given by [20]

$$I_i = \frac{3.16\times10^{10}\varphi_L^{1/2}}{\Delta S}\exp\left(-1.025\,\Delta S\,\varphi_L^{1/2}\right)V_i a_i, \quad \text{for } V_i \cong 0, \qquad (2\text{-}1)$$

where

$$\varphi_L = \varphi_0 - \frac{5.75}{K\,\Delta S}\ln\left(\frac{S_2(t-S_1)}{S_1(t-S_2)}\right), \qquad (2\text{-}2)$$

$$\Delta S = S_2 - S_1, \qquad (2\text{-}3)$$

$$S_1 = \frac{6}{K\,\varphi_0}, \qquad (2\text{-}4)$$

and

$$S_2 = t - \frac{6}{K\,\varphi_0}, \tag{2-5}$$

noting that ΔS is the difference in Fermi levels at the insulating barrier. For the same microcontact area, a_i, the tunneling resistance, R_{ti}, for $V_i \cong 0$ can then be given as

$$\mathrm{R}_{ti} = \frac{\Delta S \exp\left(1.025\, \Delta S\, \varphi_L^{1/2}\right)}{3.16\times 10^{10} \varphi_L^{1/2}\, a_i}, \tag{2-6}$$

where the total ECR across the applied surface is assumed to be equal to the sum of the individual resistances of the contacting micro-asperities. For wafers used in this work (boron doping concentration $n_A = 10^{18}$ atoms/cm^3), the barrier height for valence-band hole flow from doped Si into SiO_2 is expected to be about 5 eV. It was shown [17] that voltage levels through a thin film insulator (t < 50 Å) fall in the intermediate-voltage range when $V < \varphi_0/e$. While this is technically outside the range for the models reported, error is shown to be less than 6% at $V < \varphi_0/e$ and rapidly decrease to less than 1% when $0.75\ V < \varphi_0/e$. Note that the constriction resistance has been shown to be neglected as secondary to tunnel resistance up to and above electrical potentials of 1 V [20]. Specifically, constriction resistance, which is defined by the resistance between two conductors touching over a small circular area [26], can be neglected where

$$\frac{\mathrm{R_{ci}}}{\mathrm{R_{ti}}} = \frac{3.16\times 10^{10} \varphi_L^{1/2} \lambda\, \rho}{\Delta S \exp\left(1.25 \Delta S \varphi_L^{1/2}\right)} \ll 1, \tag{2-7}$$

where ρ = resistivity, λ = average electron mean free path between contacting surfaces, K = dielectric constant. As the voltage drop across the contact interface exceeds 1 V and beyond, the tunnel resistance becomes non-ohmic and decreases with an increase in voltage. However, it is shown in [17,27] that while tunnel resistance decreases by roughly an order of magnitude when

the voltage increases from 0 to 1 V, the ratio of R_{ci} / R_{ti} remains significantly less than 1, and constriction resistance remains negligible. It was also reported [20] that the non-ohmic variation of ECR due to the intrinsic voltage-dependence of tunnel resistance becomes less pronounced with an increase of applied current, particularly at 10 μA and above. Note that all measurements in this work are taken at 1 mA, and with potentials less than 1 V.

The microcontact area, a_i, refers to the real contact area, rather than the apparent contact area, and can be described in terms of a fractal surface, which provides the ability to describe a surface that overcomes the resolution limitations of measuring surface roughness parameters. In defining the real area of contact in terms of fractal surfaces, the fractal roughness, G, and the fractal dimension, D, are required. The fractal roughness G is a height scaling parameter that is independent of frequency and defines the roughness of the surface. Fractal dimension D determines the frequency dependence of the surface profile and defines the size ratio of asperities, with asperities of smaller contact areas as higher frequency components and asperities of larger contact areas as lower frequency components. Fractal roughness G is defined over the range of the smallest to largest microcontact area, typically in the 10's – 100's of nanometers (10^{-17} m < G < 10^{-13} m) for fabricated polysilicon MEMS [24]. Fractal dimension D is defined from 2 < D < 3, where increasing D values correspond to higher frequency surfaces with a majority of smaller asperity areas. For the case of elastic to fully plastic deformation, which includes surfaces with plastic micro-asperities within an elastic medium, the real contact area can be given in terms of fractal parameters by [26]

$$a' = \frac{D-1}{2\,(3-D)} a'_L \left[\left(\frac{a'_c}{a'_L}\right)^{(3-D)/2} - 2\,\left(\frac{a'_S}{a'_L}\right)^{\frac{(3-D)}{2}} + 1 \right] \tag{2-8}$$

where a'_S and a'_L are the smallest and largest truncated microcontact areas, respectively, and a'_C defines the critical truncated area separating elastic from fully plastic microcontact asperity deformation, given by [26]

$$a'_C = \left[2^{9-2D}\pi^{D-2}b^{-1}G^{2D-4}\left(\frac{E}{c\,Y}\right)^2 ln(\gamma)\right]^{1/(D-2)}. \qquad (2\text{-}9)$$

where γ is a fractal scaling parameter (typically equal to 1.5), c is a constraint factor (typically equal to 2.8), E is the Young's Modulus of the mechanical surface, Y is the yield strength of the mechanical surface, and b is given by [26]

$$b = [\pi(0.454 + 0.41\upsilon)/2]^2 \qquad (2\text{-}10)$$

where ν is Poisson's ratio of the mechanical surface. Truncated contact area for a circular microcontact, a′, is defined as the portion of the contact are that is in contact with the opposing surface, given by $a' = \pi(r')^2$, where r′ is the truncated radius of contact. Typically, the smallest truncated area of a surface in contact is defined as six times the lattice parameter of the material, a ($a'_S = 6 * a$). The largest truncated microcontact area can be found implicitly by solving for a′ as a function of the applied load and apparent contact area.

2.1.2 Plotting expected ECR-force behavior

To gain a further understanding of how each parameter affects ECR and normalized ECR versus applied force, several plots were generated for varying parameters. Because the asperity model varies only microasperity contact area, and not macroscale geometry, the apparently contact area in all cases does not vary with changing parameter values.

2.1.2.1 Varying fractal dimension

For a contact interface with surface roughness R_q (fractal roughness $G = R_q^2$) the apparent and real contact area is shown below in Figure 2-6 for several D values over the applied force

range for chips with force applied by accelerated inertial mass between 25 mN and 35 mN, with parameter values given below in Table 2-9. Note that the apparent contact area remains the same for all values of D.

Table 2-2. Parameter definitions and values used in modeling plots

MODELING PARAMETERS		
Definition	Variable	Value
Surface roughness	R_q	0.2 µm
Fractal dimension	D	Variable
Oxide thickness	t	8 Å
Line contact length	l	50 µm
Contact radius	r	5 µm

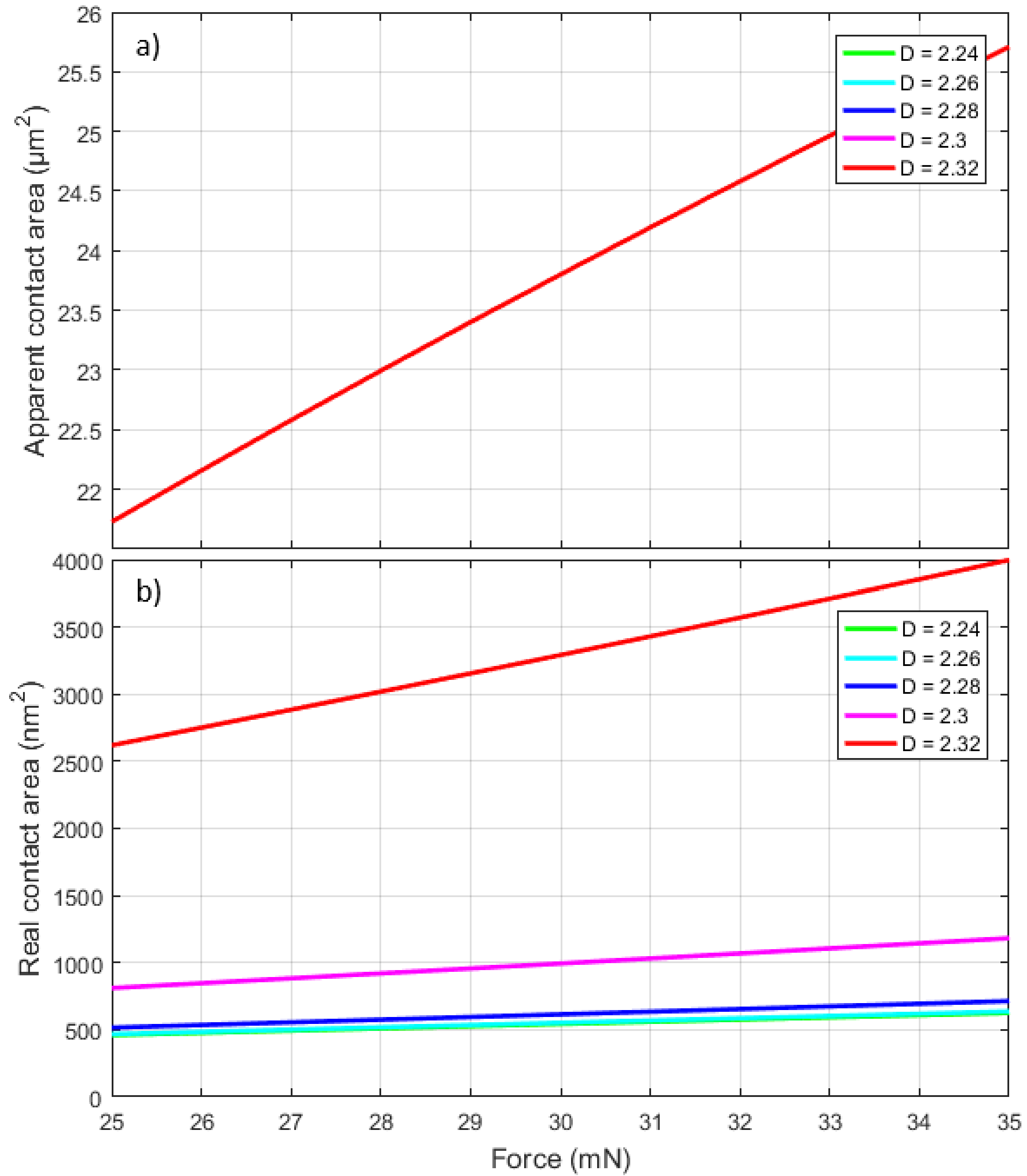


Figure 2-6. Analytic ECR model output showing a) apparent and b) real contact area versus contact force for several values of fractal dimension D over the applied range in experimental testing of inertially accelerated chips, with parameter values given in Table 2-9. Note that curves are completely overlapping in a).

Increasing fractal dimension D (which increases with higher frequency topology) is shown to increase the real contact area. For a given surface roughness, the number of contacting micro-asperities increases with higher frequency topology because more microasperity peaks between interfaces are likely to be in contact. As shown below in Figure 2-7, this means that increasing fractal dimension D decreases the overall electrical contact resistance.

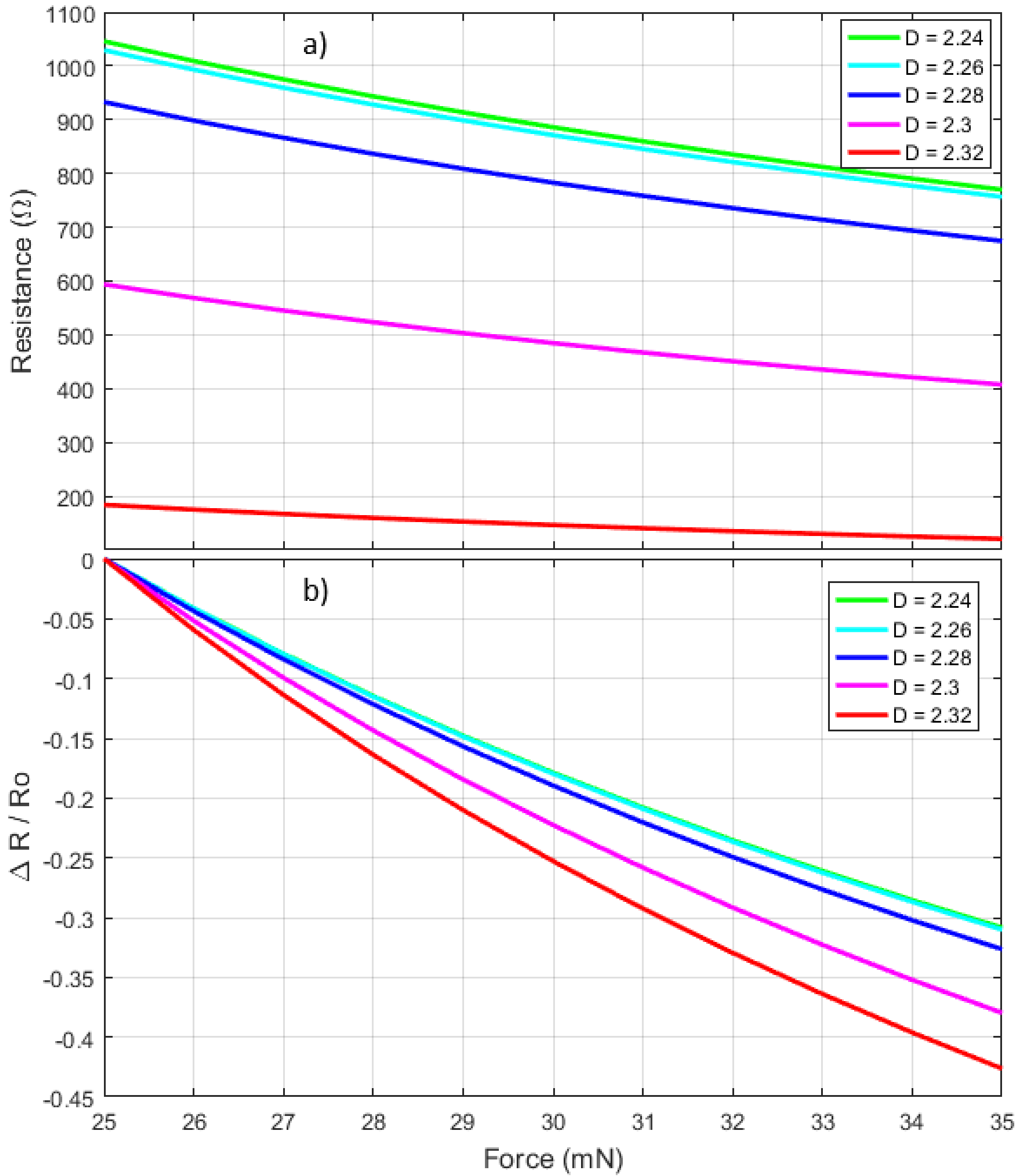


Figure 2-7. Analytic ECR model output showing a) raw absolute and b) normalized resistance versus contact force for several values of fractal dimension D, with parameter values given in Table 2-9. Note that the initial resistance does not include path resistance.

Increasing D is shown to lower initial resistance, and only slightly affects normalized change in resistance.

2.1.2.2 Varying surface roughness

For surfaces with a constant fractal dimension D equal to 2.3 (used in this work), the effect of varying surface roughness, R_q, (where $G = R_q^2$) is shown below in Figure 2-8, with parameter values given in the table below.

Table 2-3. Parameter definitions and values used in modeling plots

MODELING PARAMETERS		
Definition	Variable	Value
Surface roughness	R_q	Variable
Fractal dimension	D	2.3
Oxide thickness	t	8 Å
Line contact length	l	50 µm
Contact radius	r	5 µm

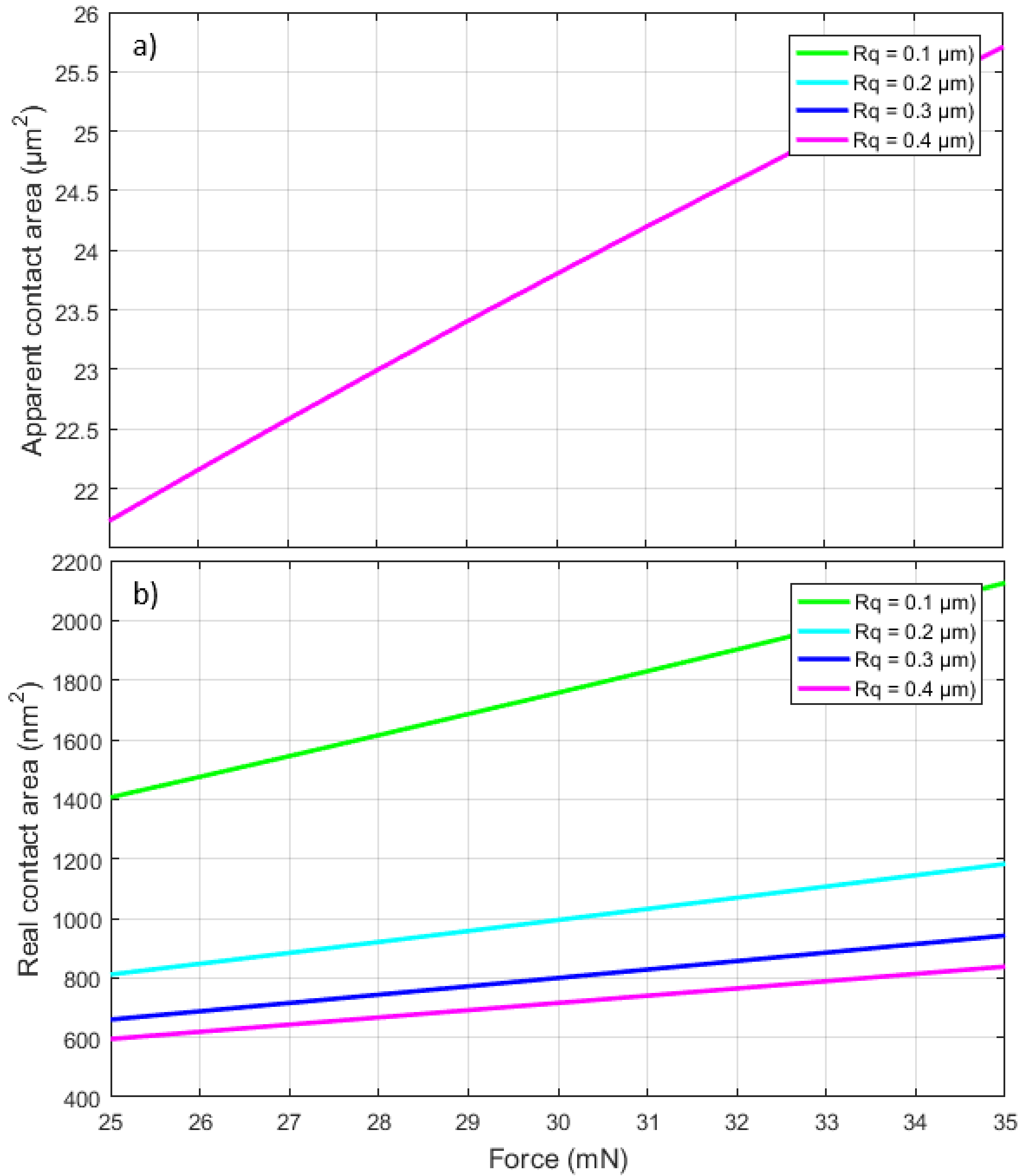


Figure 2-8. Analytic ECR model output showing a) apparent and b) real contact area versus contact force for several values of surface roughness R_q over the applied range in experimental testing, with parameter values given in Table 2-10. Note that curves are completely overlapping in a).

Increasing R_q reduces the real contact area, and therefore will also increase electrical contact resistance, as shown in Figure 2-9 below.

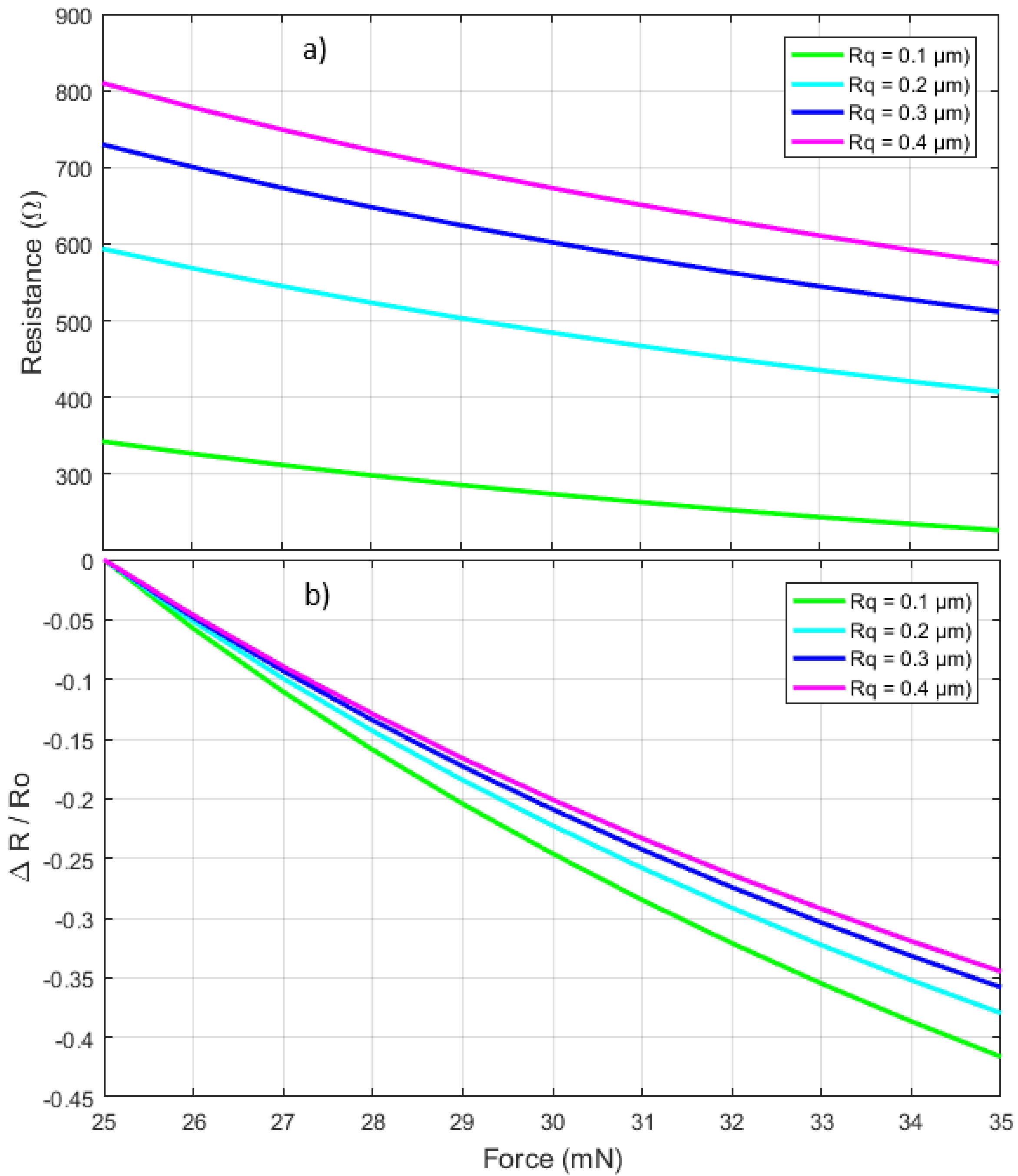


Figure 2-9. Analytic ECR model output showing a) raw absolute and b) normalized resistance versus contact force for several values of surface roughness, with parameter values given in Table 2-10. Note that the initial resistance does not include path resistance.

2.1.2.3 Varying oxide thickness

Oxide thickness of experimentally tested chips was assumed to be 8 Å in all cases. Looking at Figure 2-10 below, which shows native oxide thickness as a function of exposure time to ambient air for p-doped Silicon (all wafers in this work used boron doping concentration $n_A = 10^{18}$ atoms/cm^3), oxide thickness is expected to be ~ 7 - 9 Å for exposure time between 7 days to over 70 days. As all wafers in this work were tested between 1 – 3 weeks after HF exposure, 8 Å was assumed as an appropriate average. Note that for normalized ECR-force, oxide thickness is expected to be negligible, as shown in Figure 2-11.

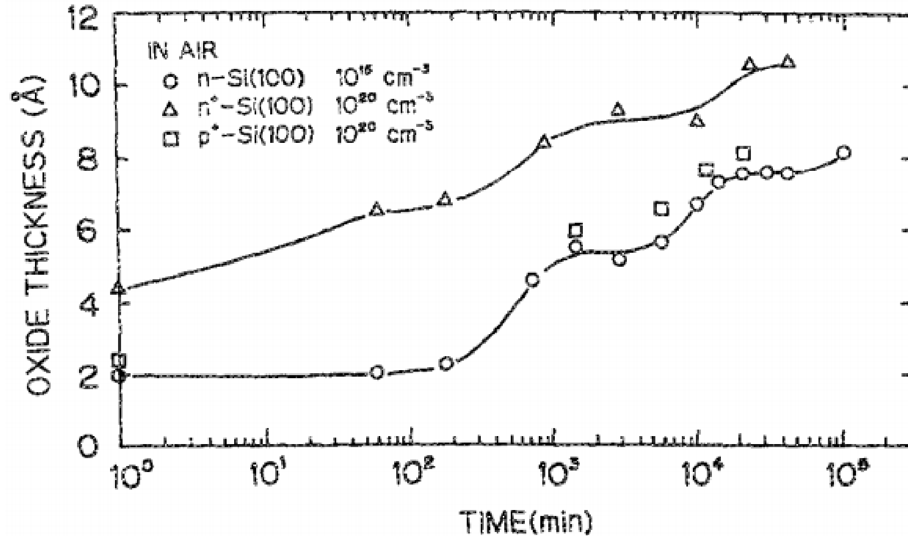


Figure 2-10. Native oxide thickness as a function of exposure time of Silicon wafers to air at room temperature over 69 days [43].

In contacting surfaces where topology and geometry are constant, thickness of the native oxide layer has a significant effect on the absolute resistance, however, has no effect on the normalized resistance (Figure 2-11). The increasing resistance also results in a corresponding increase in sensitivity over the same applied force range. Parameter values are given below.

Table 2-4. Parameter definitions and values used in modeling plots

MODELING PARAMETERS		
Definition	Variable	Value
Surface roughness	R_q	0.2 µm
Fractal dimension	D	2.3
Oxide thickness	t	Variable
Line contact length	l	50 µm
Contact radius	r	5 µm

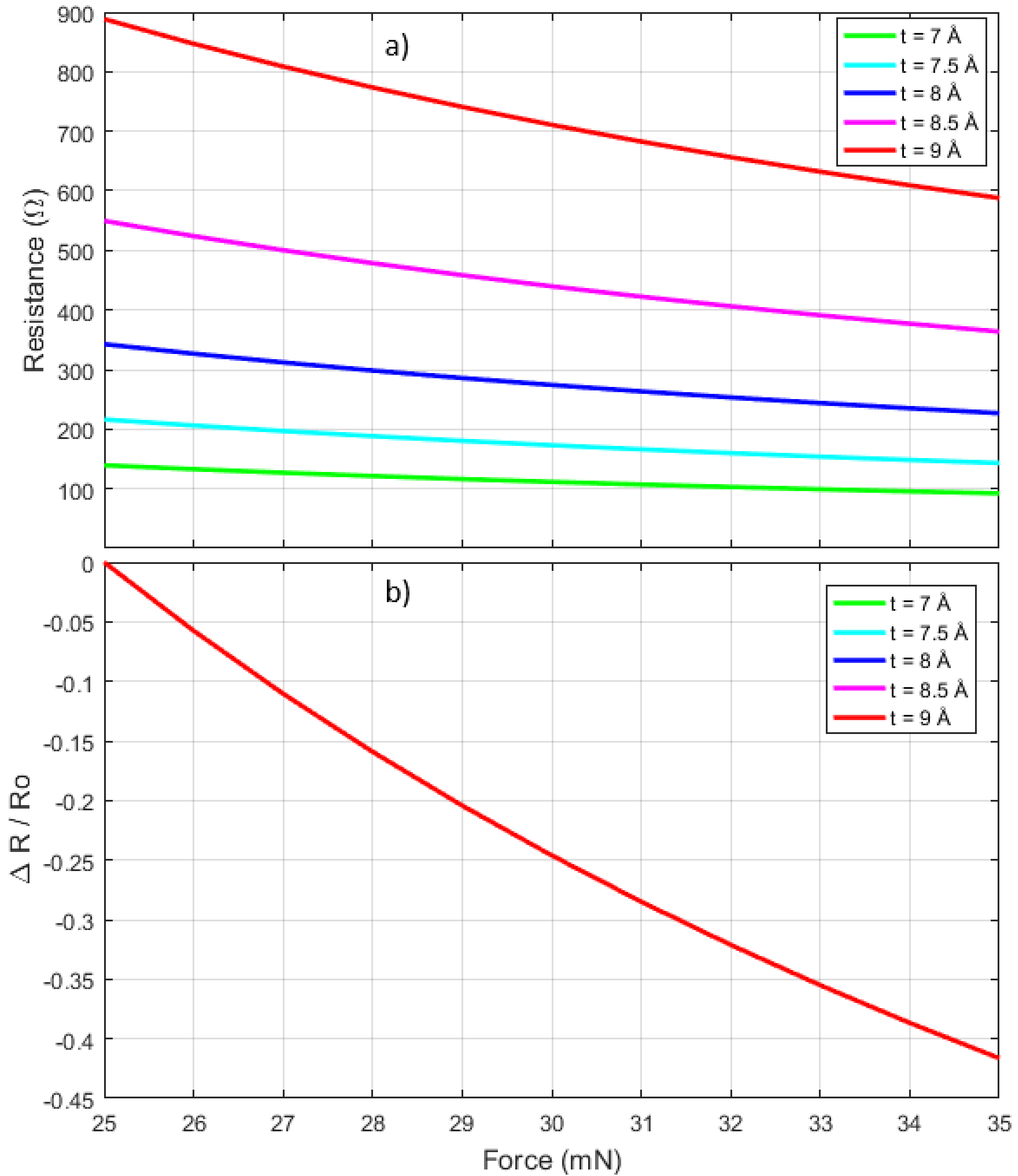


Figure 2-11. Analytic ECR model output showing a) raw absolute and b) normalized resistance versus contact force for several values of native oxide thickness, t, with parameter values given in Table 2-11. Note that the initial resistance does not include path resistance. Note that curves are completely overlapping in b).

Since it is assumed that the real contact area is a small fraction of the apparent contact area, and therefore that there is no microasperity interaction within a surface, Hertzian theory can be used to determine the apparent contact area as it varies with macro-scale parameters (as opposed to microasperity contact radius).

2.1.3 Hertzian contact

On a macroscale, the interaction between line DRIE interfaces is best approximated as a cylinder on a flat plane. Using a Herztian contact model for a cylindrical surface and a flat plane surface in contact under a force, the maximum Hertzian contact pressure, p_{max}, can be calculated using the contact half-width, b, the applied contact force, F, and the line contact length, l, by

$$p_{max} = \frac{2F}{\pi b l}, \tag{2-11}$$

with

$$b = \sqrt{\frac{2F}{\pi l} \frac{\frac{(1-\nu_1^2)}{E_1} + \frac{(1-\nu_2^2)}{E_2}}{\frac{1}{d_1} + \frac{1}{d_2}}}, \tag{2-12}$$

where subscripts 1 and 2 both refer to Silicon, d is the contact diameter, E is the Young's modulus, and ν is Poisson's ratio. For this work, the force range is limited to 5 - 35 mN to correspond to the applied force range during cyclic loading, while the maximum line contact length is the thickness of devices, equal to 100 μm.

2.1.3.1 Varying line contact length

The effect of changing line contact length on the apparent contact area is shown below in Figure 2-12, respectively, including the effect of the changing apparent contact area on the real contact area derived from the Greenwood-Williamson model above. Parameter values used in modeling are given below in Table 2-12. Note that the actual line length in contacting DRIE

surfaces is usually less than maximum (due to taper and undercut), and can vary significantly with applied force due to non-linearly surface topology after DRIE (as shown in Figure 2-4).

Table 2-5. Parameter definitions and values used in modeling plots

MODELING PARAMETERS		
Definition	Variable	Value
Surface roughness	R_q	0.2 µm
Fractal dimension	D	2.3
Oxide thickness	t	8 Å
Line contact length	l	Variable
Contact radius	r	5 µm

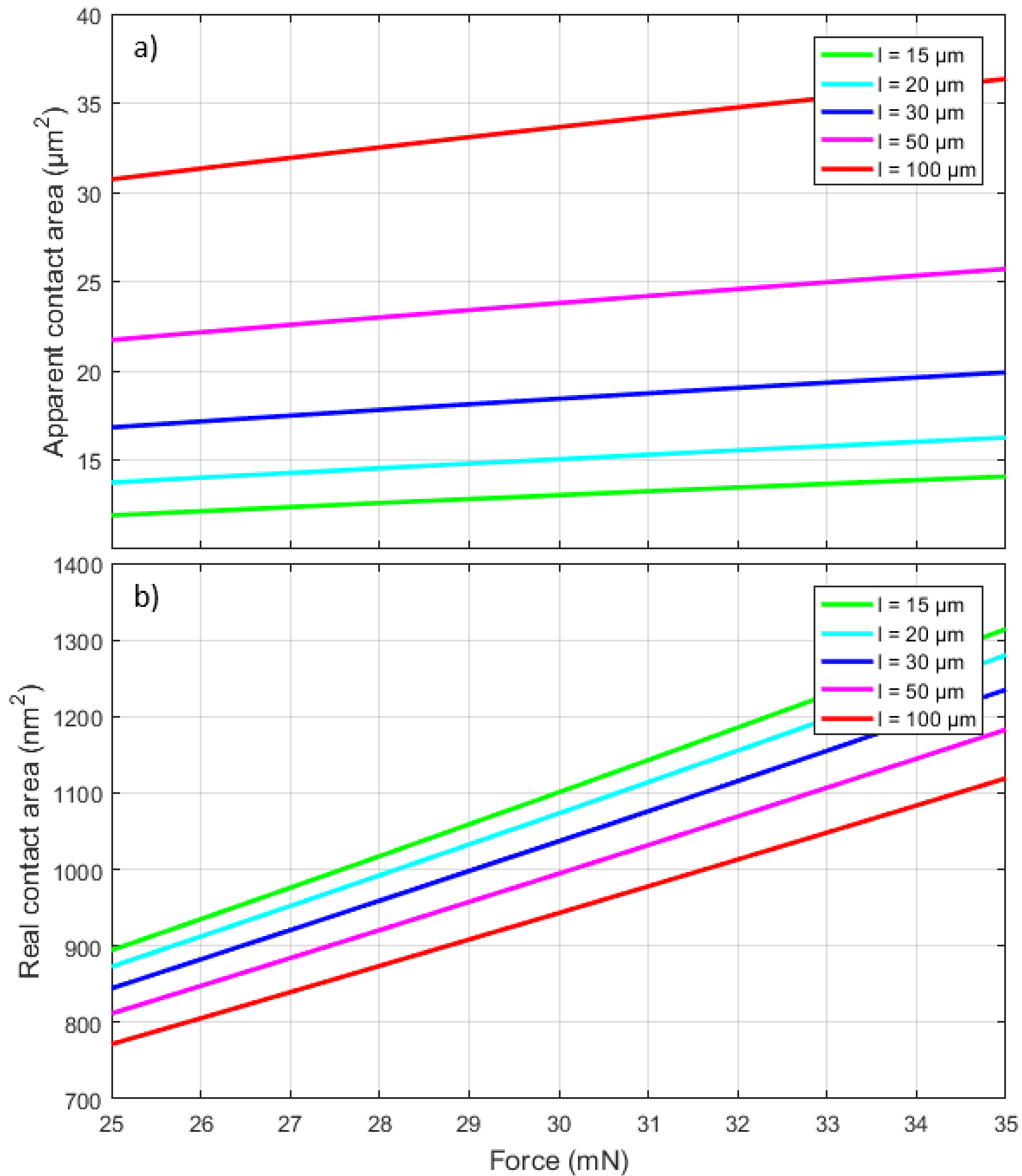


Figure 2-12. a) Analytic Hertzian model output showing the change in apparent contact area versus force resulting from varying line lengths, and b) real contact area versus contact force resulting from the change in apparently contact area, with parameter values given in Table 2-4.

2.1.3.2 Varying contact radius

The effect of changing contact radius on the apparent contact area is shown below in Figure 2-13, including the effect of the changing apparent contact area on the real contact area derived from the Greenwood-Williamson model above. Parameter values used in modeling are given below in Table 2-6.

Table 2-6. Parameter definitions and values used in modeling plots

MODELING PARAMETERS		
Definition	Variable	Value
Surface roughness	R_q	0.2 μm
Fractal dimension	D	2.3
Oxide thickness	t	8 Å
Line contact length	l	50 μm
Contact radius	r	Variable

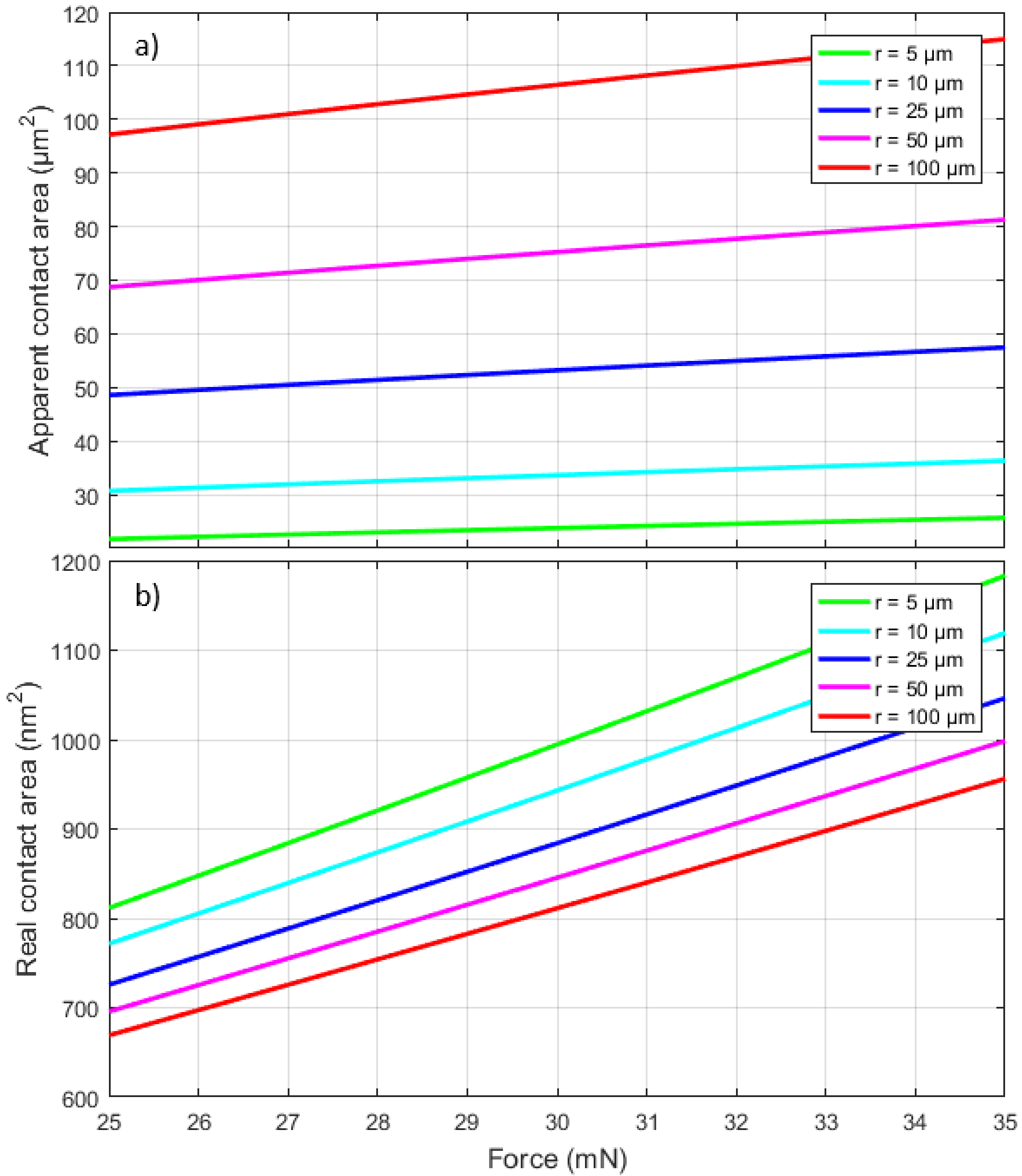


Figure 2-13. a) Analytic Hertzian model output showing the change in apparent contact area versus force resulting from varying contact radius, and b) real contact area versus contact force resulting from the change in apparent contact area, with parameter values given in Table 2-6.

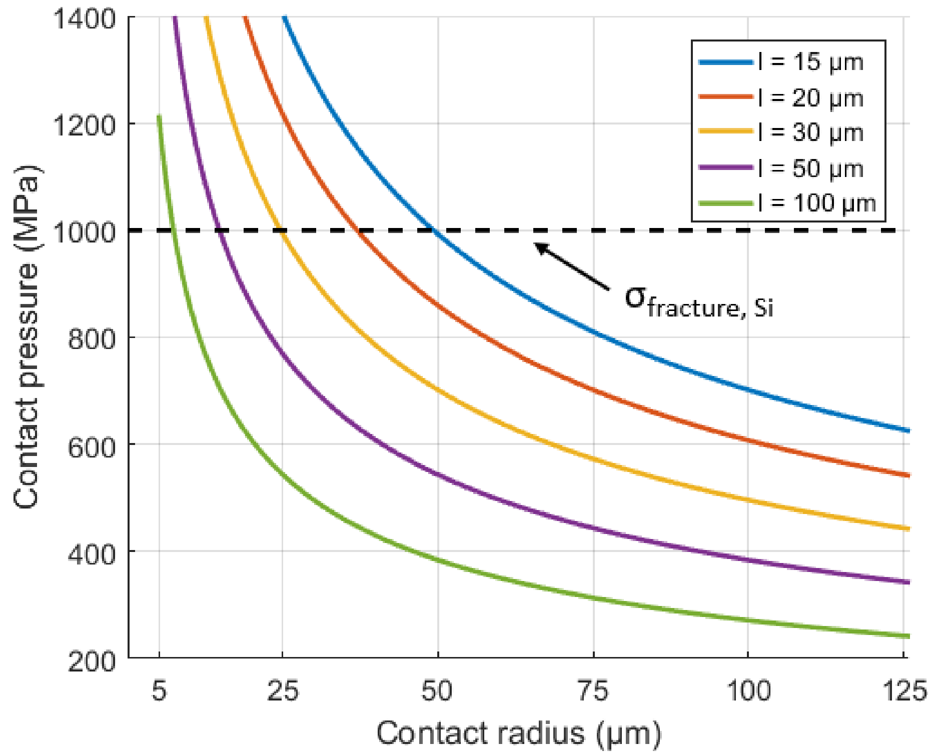


Figure 2-14. Analytic Hertzian model output showing contact pressure versus varying line contact length and varying contact radius under a 25 mN applied force. Note that oxide thickness, fractal dimension, and surface roughness are not used in this model output.

Note that the analytic Hertzian model output showing contact pressure versus varying line contact length and varying contact radius under a 25 mN applied force is discussed further in 6.1.3 as it related to the fracture strength and observed fracture in contacting Silicon DRIE surfaces.

2.1.4 Combined ECR-Hertzian

Using Hertzian theory to derive the apparent contact area (2*b*l), the expected ECR for a given contact load can be found by combining (2-1(2-2(2-3) using an implicit solver (Appendix A: Matlab scripts) to calculate the apparent contact area over the range of applied force for varying line lengths and radius (MATLAB code in Appendix A). For cylinder-on-plane contact surfaces

with surface roughness $G = R_q^2 = 0.2$ µm, fractal dimension D = 2.3, and contact radius r = 5 µm, ECR is shown below in Figure 2-15 for varying line contact lengths up to the 100 µm (the fabricated device thickness within this work) for chips where force was applied by accelerated inertial mass from 25 mN to 35 mN. ECR is shown in Figure 2-16 for varying contact radius, r, between 5 µm and 100 µm.

2.1.4.1 Varying line contact length

The effect of changing line contact length on the apparent contact area is shown below in Figure 2-15, with parameter values given below in Table 2-7.

Table 2-7. Parameter definitions and values used in modeling plots

MODELING PARAMETERS		
Definition	Variable	Value
Surface roughness	R_q	0.2 µm
Fractal dimension	D	2.3
Oxide thickness	t	8 Å
Line contact length	l	Variable
Contact radius	r	5 µm

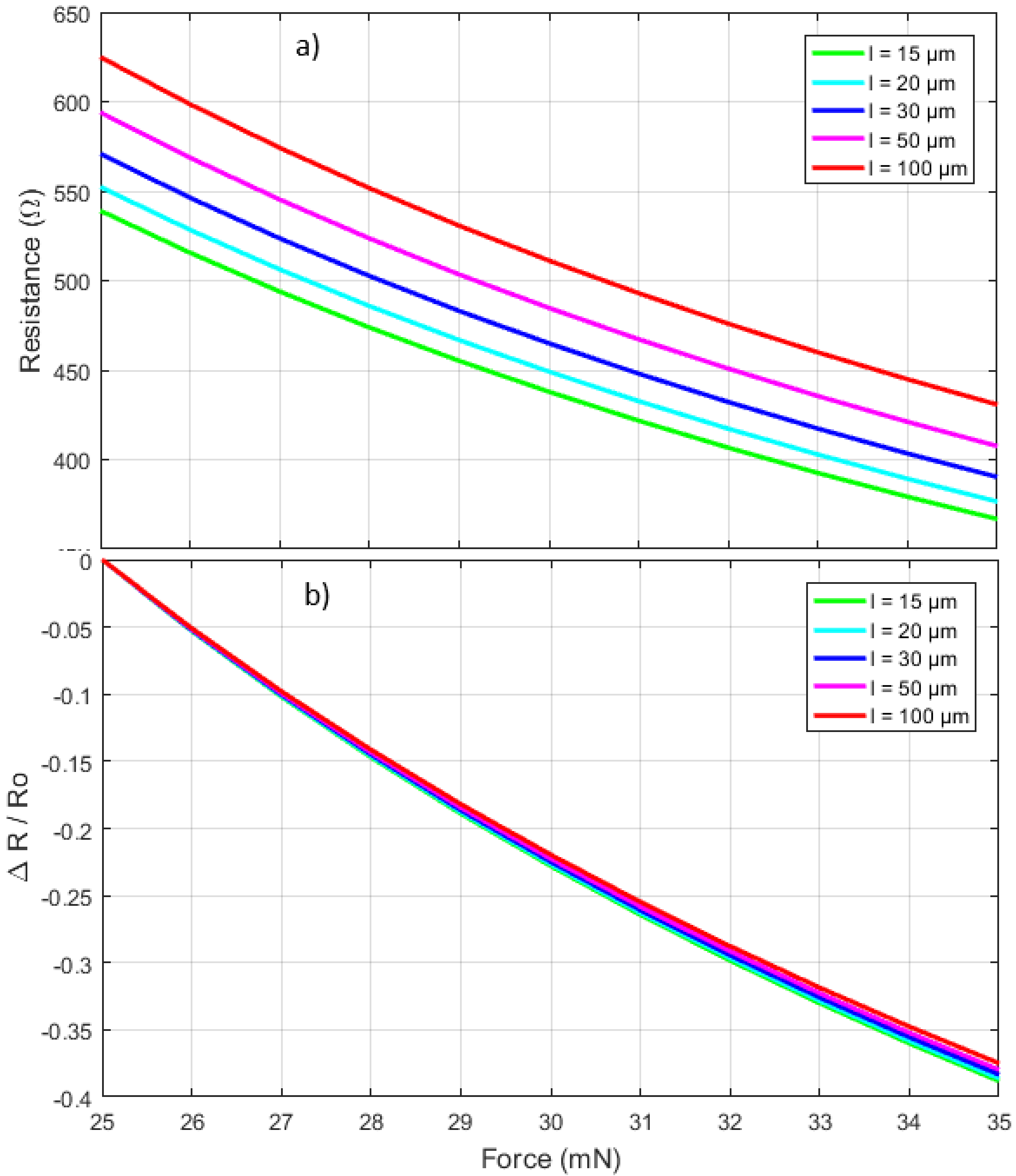


Figure 2-15. Analytic ECR-Hertzian model output showing a) raw absolute and b) normalized ECR versus applied contact force for line contact length, l, between 15 µm and 100 µm over the applied range in experimentally tested chips loaded by accelerated inertial mass. Parameter values are given in Table 2-7, and path resistance is 0 Ω.

2.1.4.2 Varying contact radius

The effect of changing line contact length on the apparent contact area is shown below in Figure 2-16, with parameters given in Table 2-8.

Table 2-8. Parameter definitions and values used in modeling plots

MODELING PARAMETERS		
Definition	Variable	Value
Surface roughness	R_q	0.2 µm
Fractal dimension	D	2.3
Oxide thickness	t	8 Å
Line contact length	l	50 µm
Contact radius	r	Variable

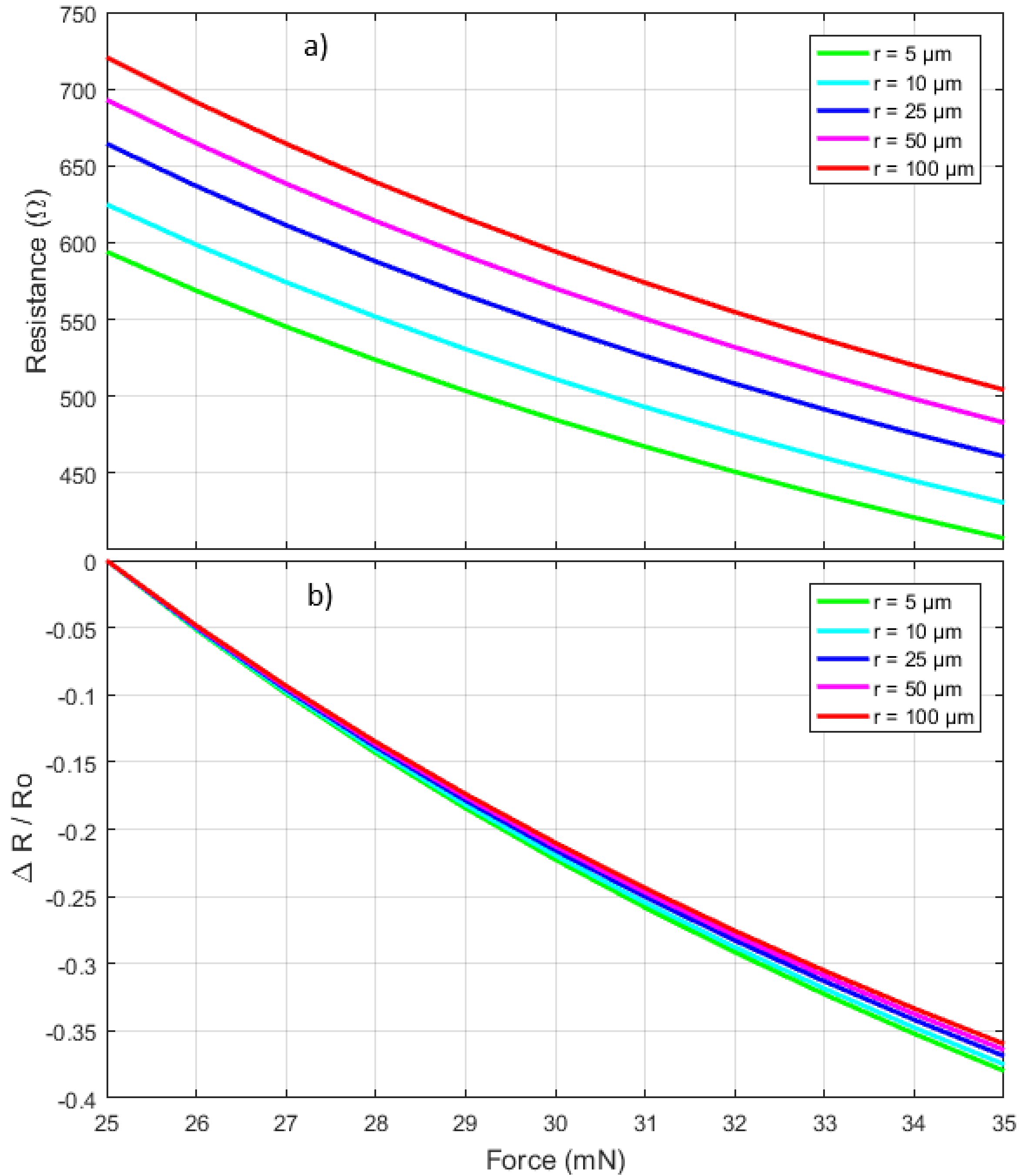


Figure 2-16. Analytic model output showing a) raw absolute and b) normalized ECR versus applied contact force for macro-scale contact radius between 5 µm and 100 µm over the applied range in experimentally tested chips loaded by accelerated inertial mass. Parameter values are given in Table 2-8, and path resistance is 0 Ω.

Increasing D lowers initial resistance, and only slightly affects normalized change in resistance. Increasing G dramatically increases initial resistance, and only slightly affects normalized change in resistance. Decreasing line contact length and decreasing contact radius decreases absolute resistance and slightly improves sensitivity. Modeling indicates the thickness of the native oxide has a large effect on the absolute resistance, but no effect on the normalized resistance. Additionally, the presented models assume no adhesion force and full line contact over perfectly parallel surfaces, however, DRIE sidewalls of fabricated devices showed significant curvature and any adhesion force between surfaces may reduce sensitivity. For analysis, ECR is normalized to initial resistance, and limited to the most reliable case where inertially loaded chips have a consistent 25 mN pre-load.

2.2 Mechanical system

Several mechanical elements were designed using analytical and finite element models, namely folded spring arrays in chips with force applied by manual spring elongation, folded spring arrays for manual pre-load of chips with force applied by inertially accelerated proof mass, and thermal actuators in chips with force applied by thermal actuation. Each mechanical element was designed for a desired stiffness. As DRIE is used to define mechanical structures, geometry is tailorable for future work to accommodate differing force levels after calibration.

2.2.1 Folded spring

Folded springs, sometimes referred to as serpentine springs, were used through this work for either pre-load or force application via spring elongation or compression. The use of folded springs allows for relatively large displacements (up to several mm) while maintaining relatively low values of stress. The folded spring design has been analyzed using both analytical methods and finite element analysis. The analytic model provided a quick method of obtaining desired

design parameters for applied a specified force, while the FEA model was used to verify the analytic model and account for filets. Figure 2-17 shows a basic folded spring.

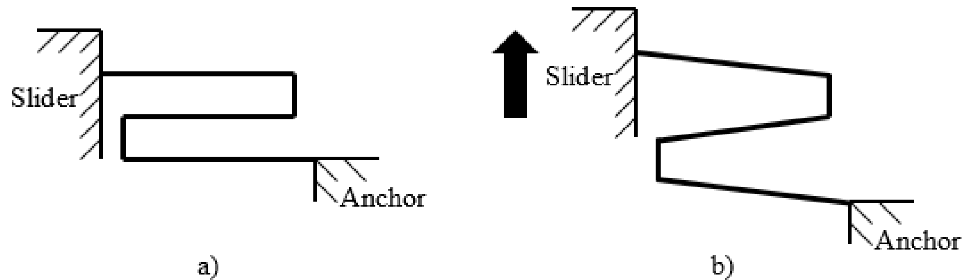


Figure 2-17. Basic folded spring in (a) initial position and (b) deflected.

The folded spring in Figure 2-17 is composed of three folds. Typical MEMS spring designs incorporate between two and five folds, and are used in many MEMS devices including accelerometers, inertial measurement units (IMUs), and magnetic actuators. Note that many more folds are used in this work. To derive an analytic model for calculating the spring constant of a folded spring, each fold is modeled as a fixed-fixed beam. The bending in the shorter (vertical) elements is assumed to be negligible.

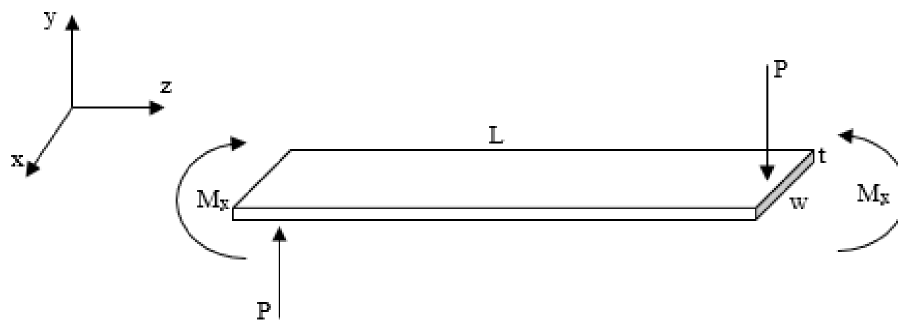


Figure 2-18. Folded spring element

As shown in Figure 2-18, the ends of the folded spring element are constrained to have a slope of approximately zero (remaining horizontal). The force-deflection relationship of each

serpentine spring can be determined using Castigliano's theorem on beam deflection using strain energy methods [28]. The total strain energy in the spring element is a sum of strain energies from bending, axial loading, and shear. The axial and shear energies are negligible when compared to bending, due to the geometry and loading of the spring. The general equation for strain energy due to bending is given below, where U_M is the strain energy and M_x is the moment about the x-axis, which is a function of position along the beam, z.

$$U_M = \int \frac{M_x^2}{2EI_x} dz \tag{2-13}$$

$$M_x = P\left(\frac{L_s}{2} - z\right) \tag{2-14}$$

$$I_x = \frac{h\, w_s^3}{12} \tag{2-15}$$

The deflection at the end of the beam can be found by taking the partial derivative of the strain energy with respect to the force, P.

$$\delta = \frac{\partial U_M}{\partial P} = \frac{\partial}{\partial P}\left(\int \frac{M_x^2}{2EI_x} dz\right) = \frac{PL_s^2}{12EI_x} \tag{2-16}$$

where variable definitions are listed in Table 2-9.

Table 2-9. Variables used in folded spring modeling.

Definition	Variable
Beam length	L_s
Beam width	w_s
Beam height (device thickness)	h
Modulus of elasticity	E
Force	P
Deflection	δ
Bending moment about x-axis	M_x
Moment of inertial about x-axis	I_x
Strain energy due to bending	U_M
Spring constant	k

The force can be divided by the deflection to yield the spring constant, k. Spring constants were also computed via FEA modeling (ANSYS) of fully featured 3D springs used in each case. Shown below in Figure 2-19, the entire spring assembly was exported from AutoCAD as a single 3D stereolithography file with 100 µm thickness into ANSYS.

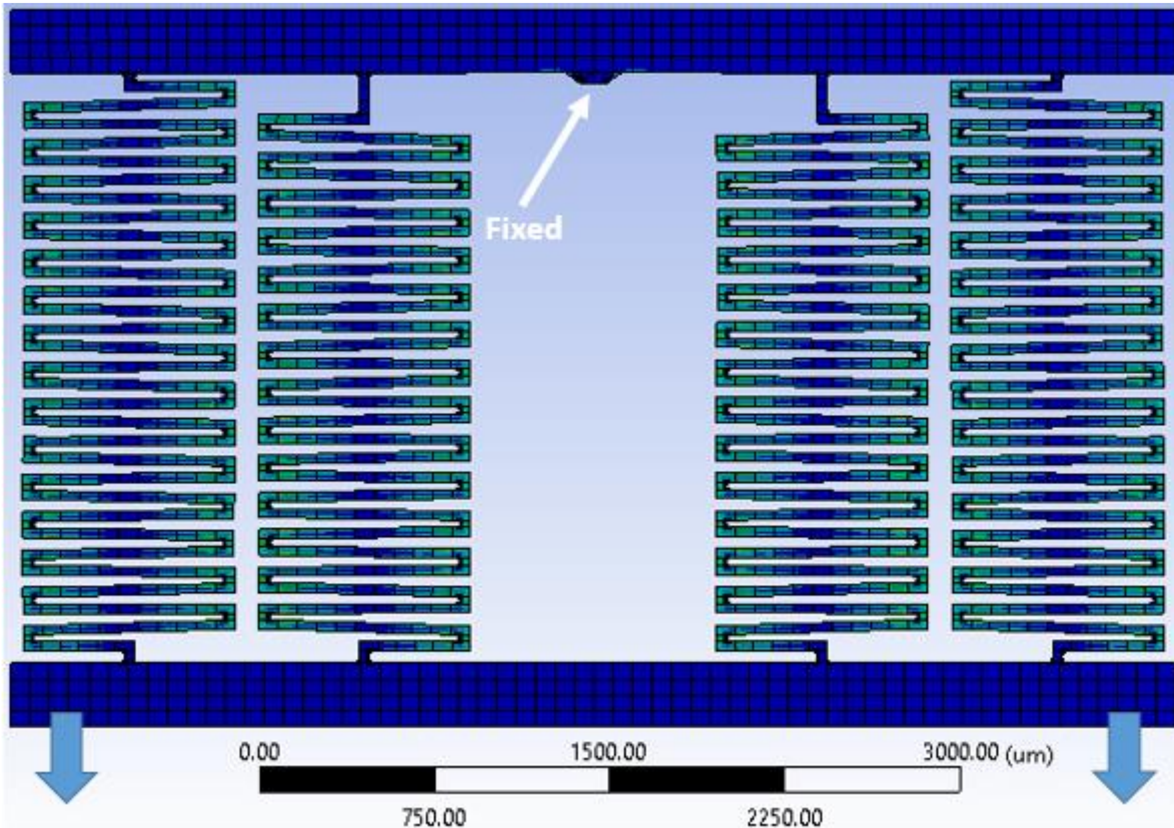


Figure 2-19. FEA ANSYS model of the entire spring assembly used in the final iteration of chips with force applied by manual spring elongation. Model is fixed at the point of contact and elongated downwards as during probe pulling. Large deflection is enabled, and each beam has three elements through the thickness. Note that a single spring showed almost exactly one quarter the stiffness of the four-spring assembly.

As shown in Table 2-10, the FEA model predicted a spring constant of 176.3 N/m, using the parameters listed.

Table 2-10. Design variables, Silicon material properties, and spring constant outputs from analytic and FEA models. Note that spring constant for the analytic model with width reduction of 4 µm total is given to compare to experimentally measured stiffness.

DESIGN VARIABLES		
Definition	Variable	Value
Length	L_s	865 µm
Width	w_s	40 µm
Thickness	t	100 µm
Springs in parallel	n	4
Springs in series	m	29
SILICON MATERIAL PROPERTIES (BULK, BORON-DOPED)		
Young's Modulus* * for bulk doped Si at 15mN loading [42]	E	125 GPa
Poisson's Ratio	ν	0.27
Density	ρ	2329 kg/m^3
MODELED PARAMETERS		
Spring constant (analytic)	k	170.5 N/m
Spring constant (FEA)	k	176.3 N/m
Spring constant (analytic, thinned 2 µm on each side)	k	124.3 N/m

The analytic model provides a valuable tool for quickly calculating force-deflection curves during the initial stages of spring design, and is used later to account for undercut and sidewall tapering of the spring assembly during fabrication caused by DRIE processing.

2.2.1.1 Pre-load mechanism

For inertially accelerated chips that relied on spring compression of folded springs to define a pre-load, geometry was modeled analytically and by FEA. The magnitude of pre-load in all inertially accelerated chips was designed to be identical. Shown below is the AutoCAD layout for a chip with force applied by accelerated proof mass, highlighting the location of the pre-load mechanism.

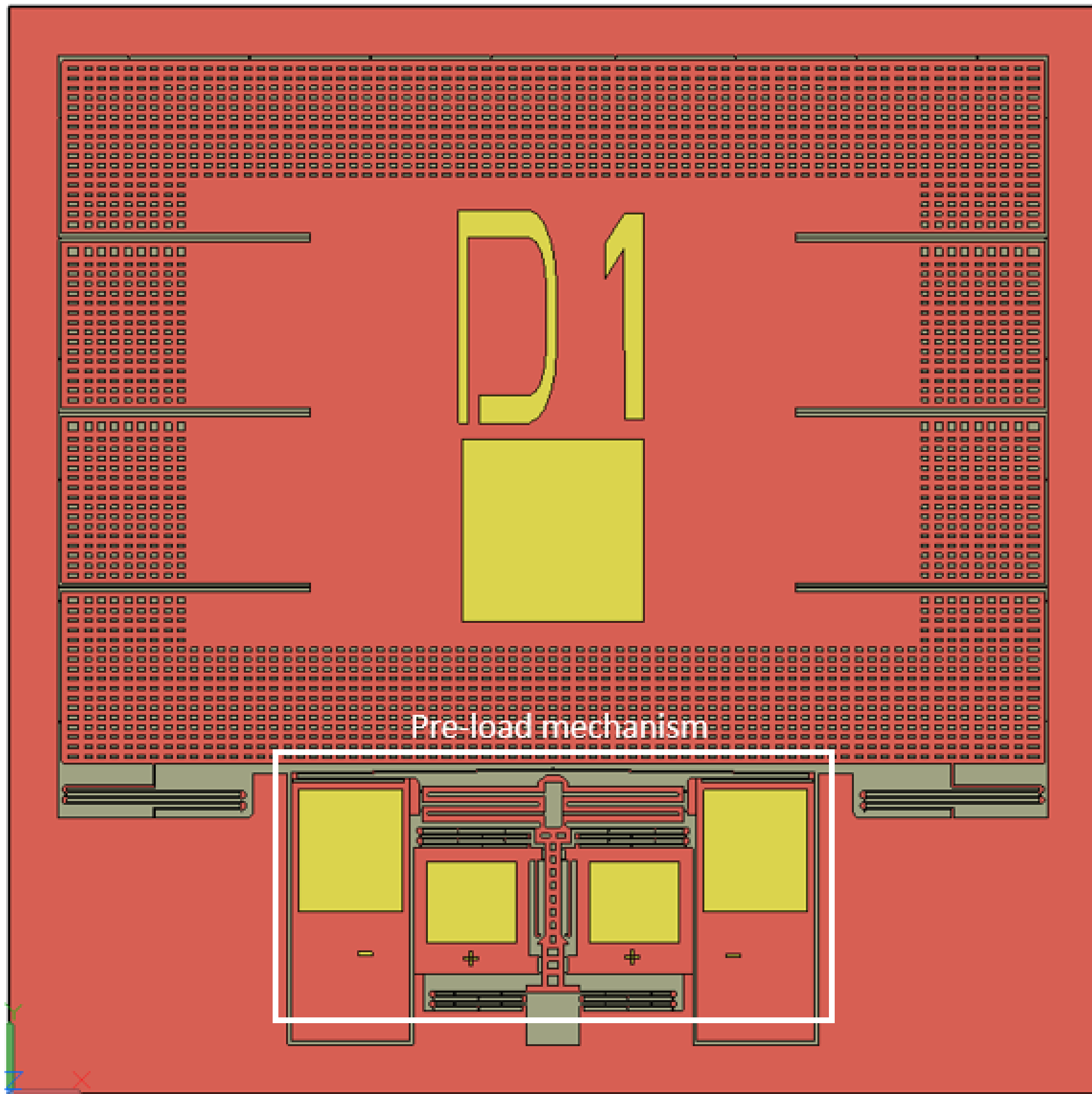


Figure 2-20. For reference, an AutoCAD schematic of a chip where force is applied by inertially accelerated pre-load. Pre-load mechanism is outlined in white.

FEA using ANSYS Workbench is shown below for the pre-load mechanism.

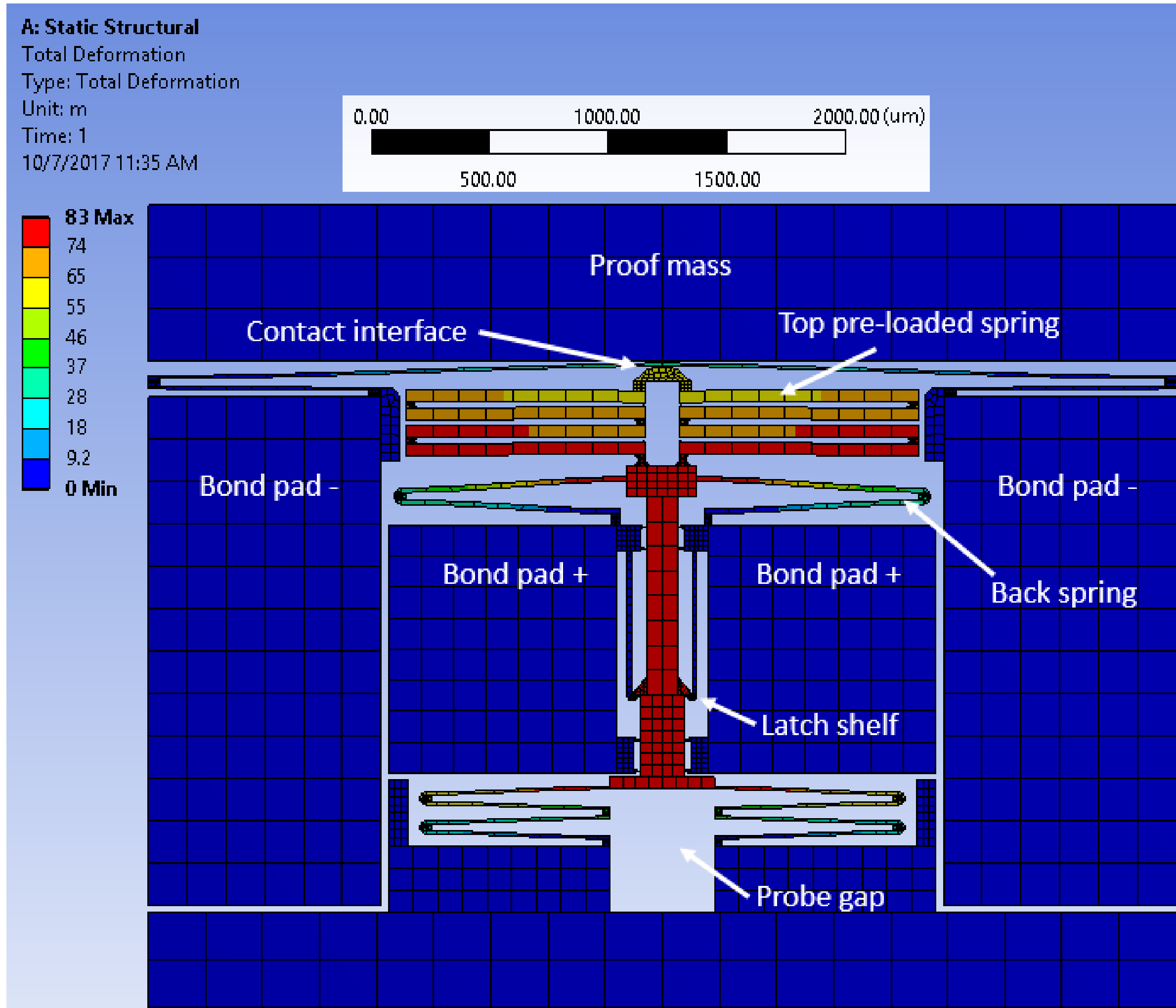


Figure 2-21. FEM of a chip with force applied by inertially accelerated proof mass using ANSYS Workbench. Proof mass is partially modeled at the top, and bond pads partially modeled at the sides. A manual probe (placed in the probe gap) moved the structure upwards until the latch shelf locked, leading to top spring assembly compression.

The position of the pre-load mechanism is shown below in Figure 2-22 for loaded and unloaded states.

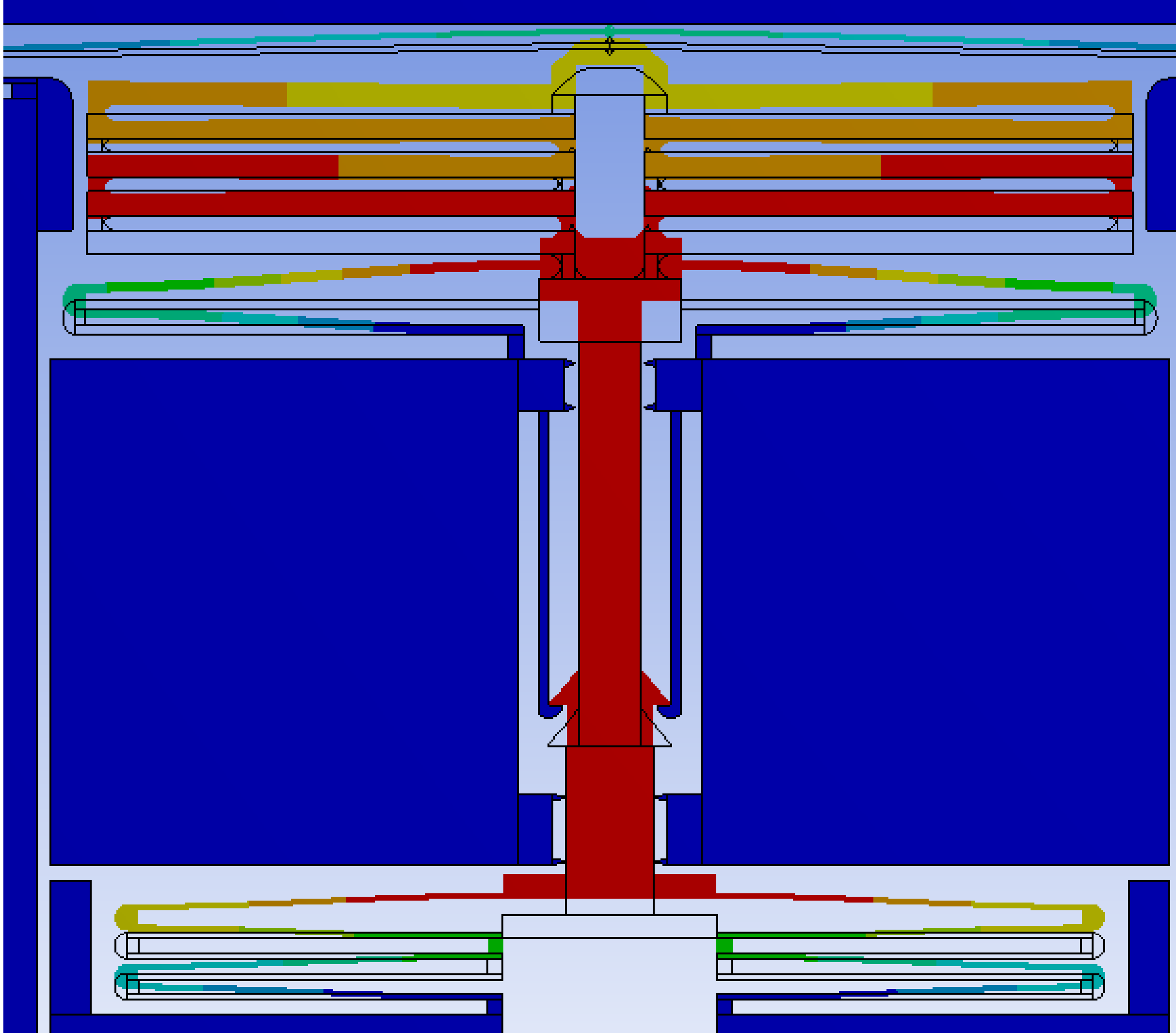


Figure 2-22. FEM of the pre-load mechanism of a chip with force applied by inertially accelerated proof mass. The structure prior to pre-load (as fabricated) is shown in black wireframe.

A comparison of the applied pre-load force between analytic and finite element models is shown below in Table 2-12.

Table 2-11. Parameters used in designing the pre-load mechanism, with a comparison between predicted pre-load force for the FEA and analytic models. Note that spring constant for the analytic model with width reduction of 4 μm total is given to compare to experimentally measured stiffness.

DESIGN VARIABLES		
Definition	Variable	Value
Length	L_s	920 μm
Width	w_s	50 μm
Thickness	t	100 μm
Springs in parallel	n	2
Springs in series	m	4
SILICON MATERIAL PROPERTIES (BULK, BORON-DOPED)		
Young's Modulus* * for bulk doped Si at 15mN loading [42]	E	125 GPa
Poisson's Ratio	ν	0.27
Density	ρ	2329 kg/m^3
MODELED PARAMETERS		
Spring constant (analytic)	k	1003.1 N/m
Spring constant (FEA)	k	995.7 N/m
Spring constant (analytic, thinned 2 μm on each side)	k	781.3 N/m

The analytic and FEA models also predict similar spring constants for the pre-load mechanism.

2.2.2 Thermal actuator

A V-beam thermal actuator consists of a clamped-clamped beam with a slight offset at the midpoint. When electrical current is applied across the beam, Joule heating causes the beam to expand and deflect in the direction of the offset as depicted below in Figure 2-23.

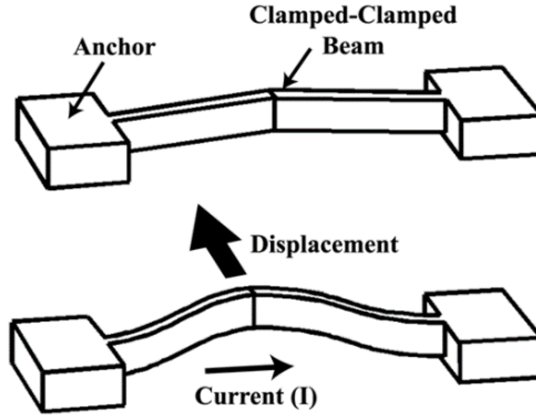


Figure 2-23. Depiction of the operating principle of a V-beam thermal actuator [29].

An actuator with a higher force output can be realized by placing several of the beams in parallel with shared anchors and a central yoke, though it has been found that more than two beam pairs can lead to instability. A model developed by Maloney et al. [29,30] has been used to design and optimize the V-beam thermal actuators. Thermomechanical analysis employing virtual work and linear beam theory was used to determine that tip displacement, u_t, and maximum force, F_t can be given by

$$\frac{u_t}{P} = \frac{\alpha L d}{4 w h k_s m^2 (d^2 + w^2)} \left[1 - \frac{2 tanh(mL/2)}{mL}\right] \tag{2-17}$$

$$\frac{F_t}{P} = \frac{4 \alpha E d}{k_s m^2 L^2} \left[1 - \frac{2\tanh(mL/2)}{mL}\right] \tag{2-18}$$

where

$$m^2 = \frac{S k_a}{k_s g h} \tag{2-19}$$

and

$$P = whLJ^2\rho \tag{2-20}$$

with the parameters in Table 2-12 below.

Table 2-12. Parameters used in thermal actuator modeling and design.

Definition	Variable
Beam length, total	L
Beam width	w
Vertical offset	d
Gap (buried Oxide thickness)	g
Height (device thickness)	h
Young's Modulus	E
Intrinsic temperature of Silicon	T_{max}
Density	ρ
Coeff. of thermal expansion	α
Current density	J
Thermal conductivity, silicon	k_s
Thermal conductivity, air	k_a
Shape factor	S
Tip displacement	u_t
Tip Force	F_t

Chapter 3: Experimental Methods

Rather than employing miniature load cells or force sensing probes, *in situ* force methods were employed to characterize ECR-force relationships in fabricated devices. Many complex microsystems successfully utilize in-situ methods for actuation [31] and measurement within a microsystem [32,33], including with the aid of probe microscopy to measure mechanical properties [34]. The use of integrated elements for applying and measuring forces allowed direct silicon-silicon contact to be monitored under constraints that prevent undesired lateral movement of the contact interface. Additionally, since the ECR relationship between contacting DRIE interfaces is currently not well-understood, the effect of small changes in contact interface mating dynamics due to varied system constraints was unknown. Although the measurement methods used in this work were used for many reasons in an attempt to most repeatably obtain ECR-force measurements, it is important to note that the characterization of ECR-force in this work depends on the measurement procedure, and may produce differing behavior with a different measurement system.

Three independent techniques were developed to apply a defined force to contacting DRIE surfaces *in situ* while measuring the corresponding change in ECR, namely the use of probe-induced manual spring elongation, thermal actuator-induced spring compression, and acceleration of an inertial mass. Two different experimental setups were used for the three force application methods. Chips where force was applied by thermal actuation or manual spring elongation did not require wire-bonding, and were tested using a standard probe station. Chips where force was applied by accelerated proof mass required wire-bonding and packaging, and a spin table for testing and characterization. Each system design was iterated several times as fabrication, testing

and analysis revealed areas for improvement. Design parameters for the three independent forcing methods were chosen based on material properties and mechanical designs.

In all cases, contact resistance measurements were obtained using Labview and a National Instruments USB X-series DAQ (± 10 V, 500 kS/s). A current source applied a constant current, I, of 1 mA across the contacting surface while the resulting voltage, V, was recorded in real-time via the DAQ system. Resistance was calculated via Ohm's law, $R = V/I$.

Preliminary testing revealed two important concerns during force cycling: narrow contact interfaces were susceptible to fracture, and wide contact interfaces were susceptible to slipping. To address this, several different contact interface geometries and varying dimensions were designed and tested. Namely, line contacts, multiple-line contacts, and area contacts (Figure 3-1) were experimentally investigated with varying success.

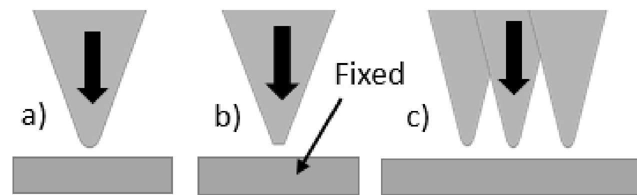


Figure 3-1. Tested contacts with a) line, b) area, and c) multiple line interface geometries.

Line contacts were expected to maintain a consistent point of contact throughout force cycling, at the cost of increased risk to fracture. Area contacts were expected to offer higher sensitivity and be less likely to experience fracture, at the cost of increased likelihood of a shifting contact point. Multiple line contacts were expected to retain high sensitivity and resistance to movement, but offer a sensitivity increase proportional to the number of line contacts. Increasing characteristic dimension of the contact shape (radius for line contacts, and

width for area contacts) was expected to reduce fracture at the risk of contact slip during force cycling.

3.1 Force by thermal actuation

Force was applied by thermal actuators using a probe station (Figure 3-2) and chips containing an embedded spring system.

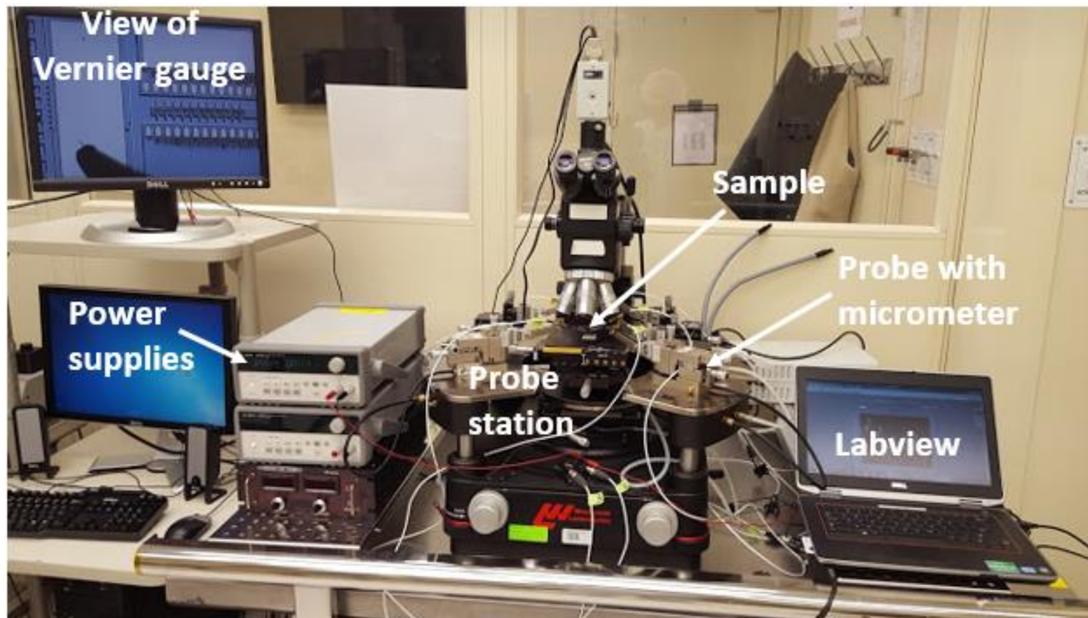


Figure 3-2. Experimental testing setup for chips with force applied by thermal actuation and manual spring elongation.

During operation, a thermal actuator, whose yolk was attached to the tip of the mechanism through a compliant structure, was powered to press two contacting surfaces together. As power through the thermal actuator is increased, thermal expansion causes an attached compliant structure to apply increasing contact force between two mating surfaces. A centrally located Vernier gauge displays displacement, and resistance is measured across the contacting surfaces under a constant current. A schematic of the final system design is shown below in Figure 3-3.

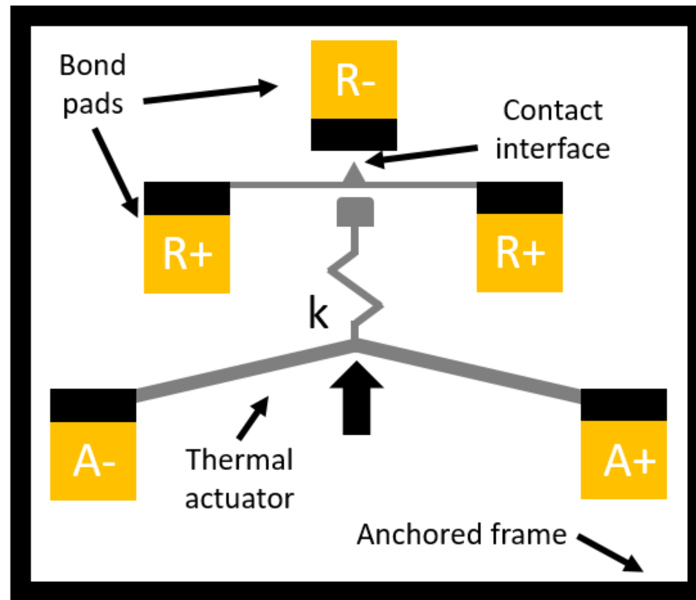


Figure 3-3. Schematic of thermal actuator inducing force via spring compression at the contact interface. Voltage applied from bond pads A+ to A- causes the thermal actuator to deflect upwards, compressing the spring, k. ECR is measured across one R+ bond pad to the R- bond pad.

Current to a thermal actuator was applied by a separate current source to displace the in-situ spring assembly until contact interfaces were touching, followed by increasing current to the thermal actuator to compress the spring assembly to define a pre-load force of 5 mN. Force was then cycled, by further thermal actuator-induced spring compression, up to a maximum value of 20 mN for line contact geometries.

The displacement-power relationship of silicon thermal actuators shows good repeatability below the intrinsic temperature of Silicon (~800 K), and it was expected that this approach would lend itself nicely to programmed power cycling of the thermal actuator to achieve highly repeatable force application from chip-to-chip. This method also used the smallest footprint of the three techniques that were investigated, measuring about 8 mm x 2 mm

per system. Since the thermal actuator would be compressing a spring, total throw of the actuator determined the applied force from the spring, which also required the tip force to be equal to spring force at all times.

3.1.1 1st generation system

The 1st generation thermal actuator system did not utilize a compliant spring, and instead relied on blocking force. Shown below in Figure 3-4, the thermal actuator was powered to press directly into a rigid wall. Resistance was measured from one thermal actuator bond pad to the bond pad atop the rigid structure, subtracting out half of the overall thermal actuator voltage drop to account for the current path.

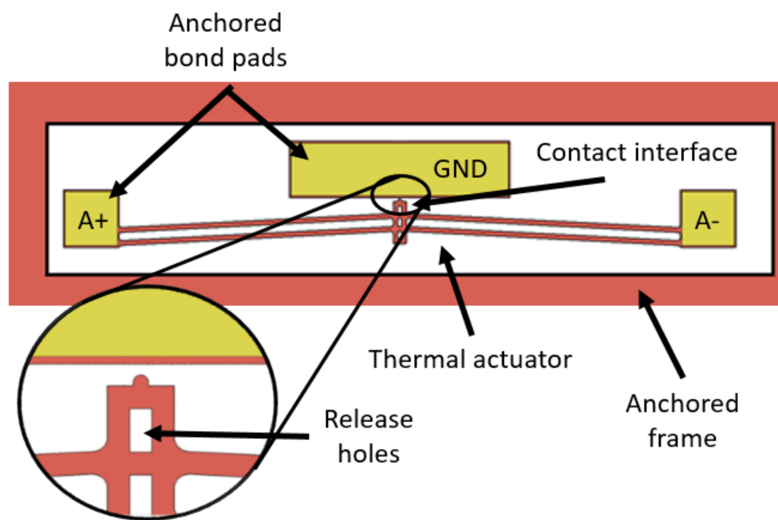


Figure 3-4. AutoCAD layout of 1st generation thermal actuator-induced force mechanism for measuring ECR vs force.

Although modeling was used to roughly predict the output power and tip displacement for the thermal actuator at a given power level, a second chip was also designed to directly measure the actuator force of fabricated devices in-situ. Shown below in Figure 3-5, a compliant

system is attached to the thermal actuator and used to pull in the opposing direction of actuator displacement. As the thermal actuator is powered, the compliant system applies an equal force in the opposite direction. The resulting system was designed for DRIE fabrication on an SOI testbed, utilizing release holes in rigid elements and a highly compliant suspension to support the contact interfaces.

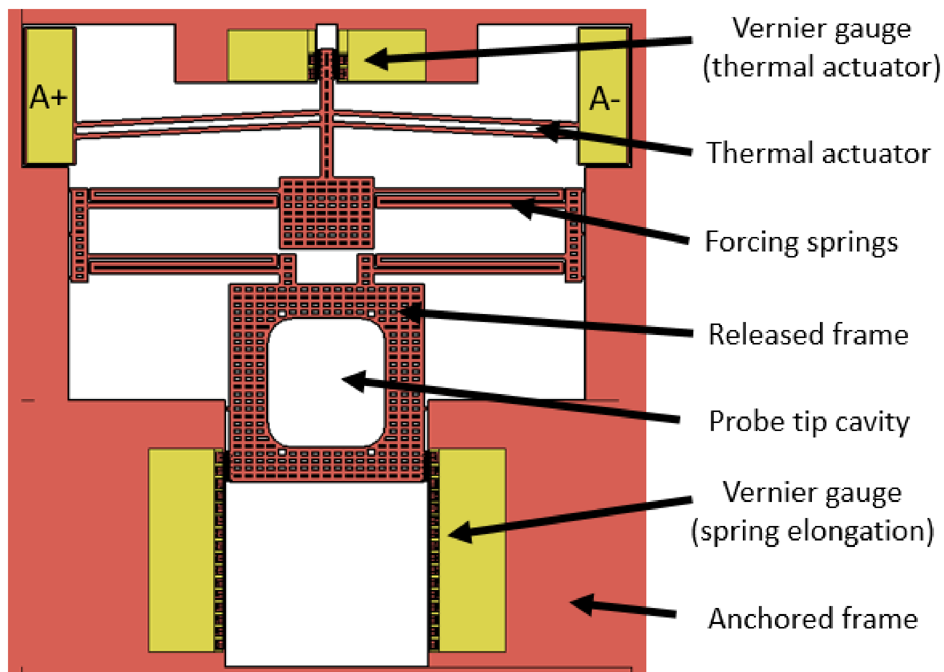


Figure 3-5. AutoCAD layout of the system used to measure thermal actuator force as a function of its input power, determined by spring elongation.

Spring force displacement and thermal actuator tip displacement are both measured using separate Vernier gauges (5 µm resolution). This process to measure thermal actuator force is shown below in Figure 3-6, and the parameters used for calibration are defined below in Table 3-1.

Table 3-1. Calibration chips for 1st generation thermal actuator chips.

Spring					Actuator					
Chip type	Width (µm)	Length (µm)	# parallel	# series	Force @ 500µm (mN)	Length (µm)	Width (µm)	Theta (deg)	Max disp. (µm)	Max force (mN)
B	30	1500	4	3	89	30	4000	1.7	73	79.4
C	30	1500	4	3	89	30	4000	2.9	53.8	132.3

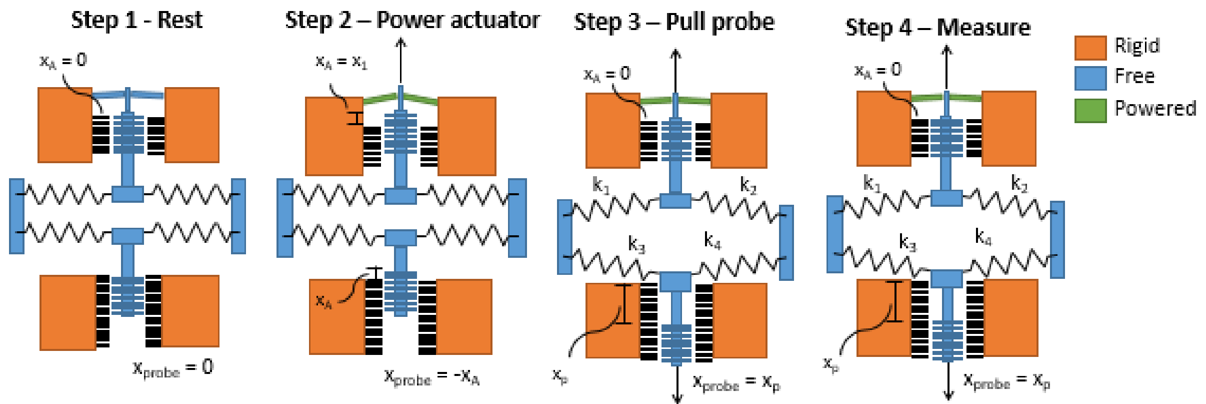


Figure 3-6. Process to measure the applied force of the thermal actuator. Calibration process occurs in the following manner: 1) starts at rest, with both probe displacement, x_{probe}, and thermal actuator displacement, x_A, reading zero, 2) thermal actuator is powered to displacement x1, 3) probe is pulled in the opposing direction until x_A reads zero again, 4) lower Vernier gauge is measured, giving the spring elongation needed to counteract the thermal actuator displacement.

The entire system is initially unpowered and at rest. Vernier gauges of both the compliant spring system and thermal actuator show zero displacement. Next, the thermal actuator is powered, pulling the entire assembly upwards, causing both Vernier gauges to read the same displacement corresponding to the input actuator power. With the actuator still powered, a manual probe is used to pull the compliant systems downwards until the Vernier gauge reads

zero, corresponding to equal opposing spring force to the actuator. Actuator force can then be calculated by reading the spring displacement and calculation via Hooke's law.

After fabrication and testing, this method was proven to be problematic, primarily because the thermal actuator immediately began to buckle. Although contact force increased with increasing actuator input power, the relationship of thermal actuator power to output force was no longer valid. The following iteration was done to apply force via thermal actuator-induced spring compression rather than blocking force.

3.1.2 2nd generation system

The 2nd (and final) generation thermal actuator system applied force via spring compression rather than via blocking force. Since the maximum displacement of a thermal actuator is limited, the forcing spring was designed to be relatively stiff to cover the needed force range, with a spring constant of 2.25 mN/µm of compression (Table 3-2).

Table 3-2. Parameters for the 2nd generation thermal actuator spring compression system.

Definition	Variable	Value
Length	L_s	1190 µm
Width	w_s	60 µm
Springs in parallel	n	2
Springs in series	m	2
Spring constant	k	225 N/m

Preliminary FEA and mathematical modeling was done to create a thermal actuator that fit within one chip (8 mm x 8 mm) and stayed below the intrinsic temperature of silicon (~800 K in this work) throughout actuation. The resulting thermal actuator consisted of two beam pairs of 3500 µm length each, 50 µm width with a 100 µm offset from parallel, with remaining

parameters shown in Table 3-3. Tip force was calculated as 126 mN at a maximum displacement of 131 µm.

Table 3-3. Thermal actuator design parameters for the 2nd generation chips.

Definition	Value
Beam length, total	7000 µm
Beam width	50 µm
Vertical offset	100 µm
Handle thickness	500 µm
Buried Oxide thickness	2 µm
Device thickness	100 µm
Tip displacement	131 µm
Tip Force	126 mN
Max stress @ 60 µm	487 MPa

Due to fabrication constraints requiring etch holes no smaller than 30 µm, the actuator needed to close a 60 µm gap prior to applying any force on the contact interfaces. The attached Vernier gauge allowed for 5 µm resolution reading of displacement, which corresponded to ~ 10 mN. Folded flexures help prevent any lateral movement, while allowing full displacement and compression of the compliant structure attached to the thermal actuator. The resulting system in Figure 3-7 can apply a contact force from 0 mN to 75 mN with thermal actuator input power from 2.5 W to 5.2 W.

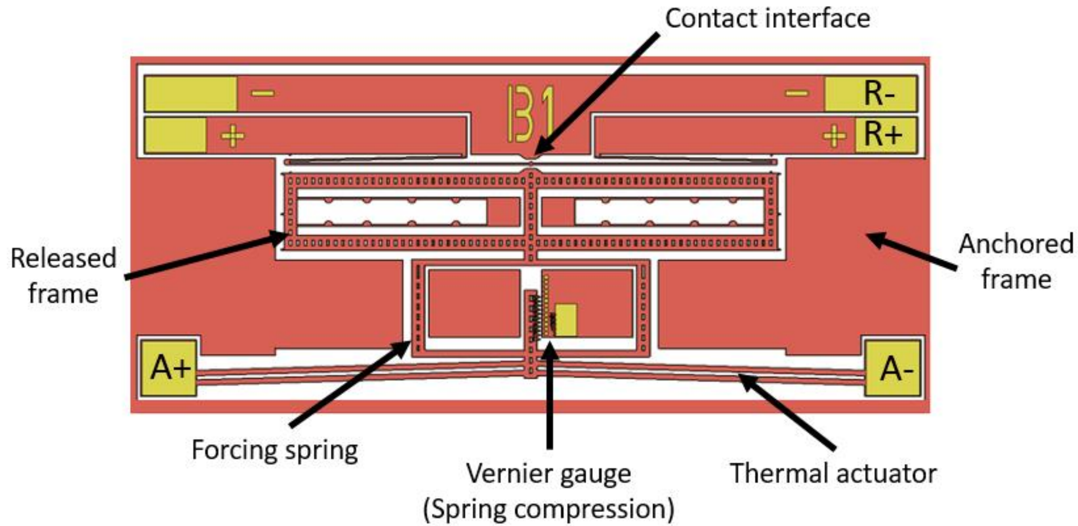


Figure 3-7. AutoCAD layout of 3rd generation thermal actuator design. Note the embedded central Vernier gauge in the middle of the rectangular forcing spring.

Instead of using a separate chip to measure actuator force, a Vernier gauge was built into each chip to measure the spring displacement during thermal actuation. While this increases the footprint of each device, it ensures that the correct force is measured for each chip. This method was used to obtain the best measurements, although repeatability was still lacking even with this system.

3.2 Force by manual spring elongation

Force was applied by manual spring elongation using a probe station and chips containing an embedded spring system. During operation, an external probe tip elongated an embedded spring system by pulling from an etched cavity, deflecting the free end of the spring assembly by up to 250 µm. The attached end of the spring assembly pressed the contact interface together with a force (F) determined from the measured spring elongation (x) assuming a linear spring constant (k) as F = kx. An embedded Vernier gauge (5 µm resolution) visually displayed elongation, and ECR was measured across the contact surface at anchored bond pads, R+ and R-,

using Labview and a National Instruments USB X-series DAQ (± 10 V, 500 kS/s). A current source applied a constant current, I, of 1 mA across the contact interface while the DAQ system recorded the resulting voltage, V, in real-time. Resistance was calculated by Ohm's law, $R = V/I$. A schematic is shown below in Figure 3-8.

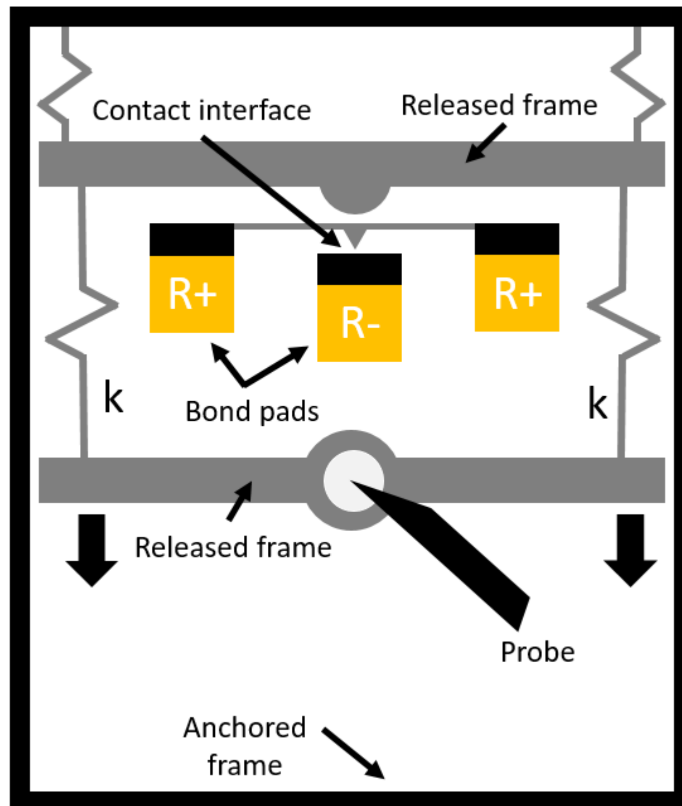


Figure 3-8. Schematic of probe applying contact force between two interfaces via spring elongation. Probe was lowered into the etched cavity and moved downwards to elongate the spring assembly. Contact resistance measured across anchored bond pads, R+ to R-.

3.2.1 1st generation system

The spring assembly for 1st generation chips using a manual probe to induce force was designed to pull contact interfaces together with forces ranging from 0 mN up to 300 mN (note that this was not achieved). The external probe tip elongated a compliant spring system by

pulling on a connected rigid hole, deflecting the system by up to 500 µm. Shown below in Figure 3-9, resistance is measured from a stationary ground bond pad, R-, through the contact interface, through a set of very compliant springs (shown on the left and right) to a stationary R+ bond pad. Elongation length of the forcing spring is read from an embedded Vernier gauge with 5 µm resolution, as in the case of thermal actuation.

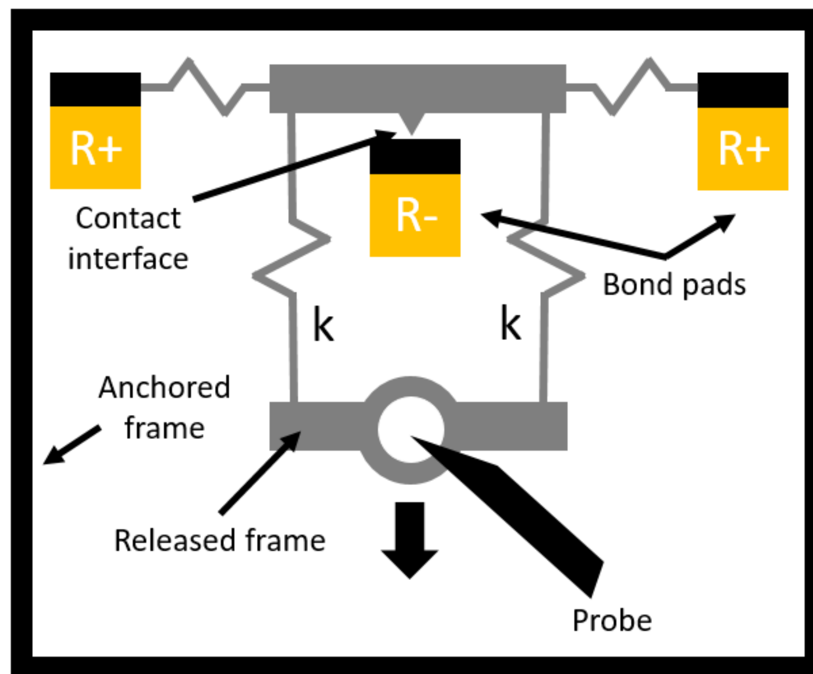


Figure 3-9. Schematic of 1st generation manually probed design. As the probe pulls downward, the springs with stiffness k are elongated, applying force to the contact interface. ECR is measured across R- and R+.

Although direction of movement is restricted by the embedded hole and attached spring assembly, the probe must be moved very carefully to avoid jerky motion that can shift the contact point. Figure 3-10 shows the finalized AutoCAD MEMS layout that was fabricated.

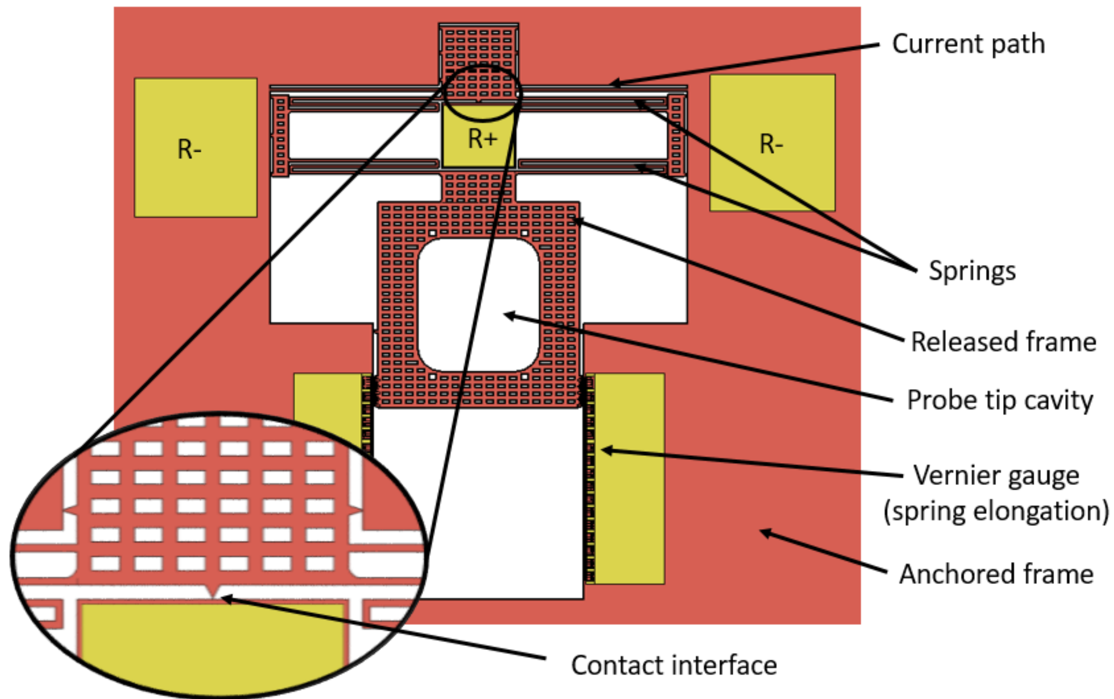


Figure 3-10. AutoCAD schematic of initial design for the direct actuation method for obtaining ECR-force measurements.

Gaps between the rigid top and bottom structures and the sidewalls were minimized, defined by a 3 μm offset between guide pins, which is the smallest allowable gap by the available fabrication tools with a 100 μm device layer. Several variants of the above design were created to test different contact geometry and compliant system parameters. Contact type, radius or width, and angle or number of contact points, were varied to asses contact geometry. Spring width and length, along with the number in parallel and series, were varied to assess maximum allowable force and dynamic behavior during motion. Table 3-4 gives the matrix of the fabricated design variations.

Table 3-4. Design matrix for the 1st generation of manually probed chips.

FORCING SPRING MATRIX						
Chip letter	Width	Length	# in series	# in parallel	Spring constant	Max stress @ 300µm
A	15 µm	1160 µm	7	2	10 N/m	233.9 MPa
B	50 µm	1256 µm	21	2	100 N/m	226.8 MPa
C	60 µm	1130 µm	25	2	200 N/m	282.6 MPa
D	60 µm	780 µm	51	2	300 N/m	292.3 MPa
CONTACT GEOMETRY MATRIX						
Chip number	Contact shape	Radius	Width	# of points	Point separation	Angle
1	multi-line	1 µm	-	2	30 µm	-
2	multi- line	1 µm	-	4	30 µm	-
3	multi- line	1 µm	-	8	30 µm	-
4	multi- line	1 µm	-	16	30 µm	-
5	area	-	10 µm	-	-	0
6	area	-	20 µm	-	-	0
7	area		20 µm			5 °
8	line	1 µm	-	-	-	-
9	line	10 µm	-	-	-	-

Baseline analysis and results obtained from testing show that the contact point tended to shift during testing. There was also great difficulty in fully resolving the Vernier gauge during DRIE etch. Additionally, although stress was modeled to be less than the fracture strength of silicon at maximum displacements, the compliant systems all fractured beyond about 50mN of force, well below the intended 300 mN intended range. Several changes were made in the following design iteration to address these issues.

3.2.2 2nd generation system

In 2nd generation manually probed chips, current path spring stiffness was reduced to minimize their contribution to the applied force by increasing the number of springs in series. A larger gap was added between the forcing spring sides and the rigid sidewall of the chip to

prevent unintended lateral scraping during force application. The Vernier gauge was re-designed to have a larger visible scale, with resolution at 5 µm. The gauge was also moved near to the contact point so that both could be viewed under a microscope simultaneously. Due to the tedious nature of testing these chips, this proved to be a significant time saver. A larger initial separation (30 µm) was added in between the contact pair to ensure that the contacting surfaces were as close to design as possible. While this gap was resolved in fabrication of 1st generation devices, it appeared that DRIE was unable to fully etch the bottom of the gap in some chips. The forcing springs in the compliant system were also re-designed to be much larger. These new springs were modeled using COMSOL to minimize localized stress hot spots. Other rigid structures were also strengthened to ensure fracture was no longer as issue. Note that a similar design matrix was used for 2nd generation manually probed devices. Figure 3-11 shows the updated design baseline used in 2nd generation design variations.

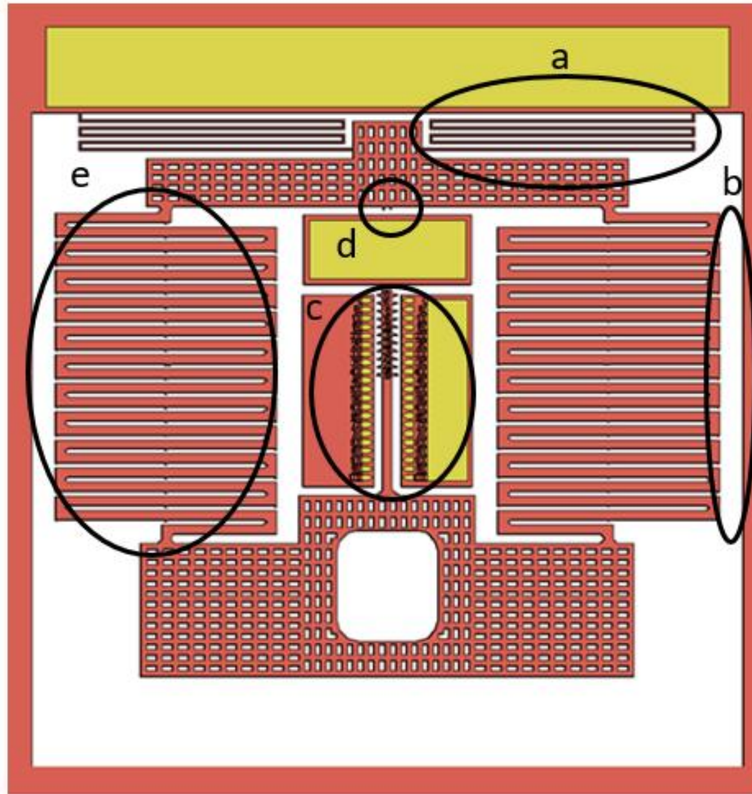


Figure 3-11. 2nd generation design of direction actuation method, showing a) reduced stiffness current path springs, b) enlarged sidewall gap, c) improved Vernier gauge, d) enlarged initial contact gap and e) improved forcing springs.

Testing revealed that the more compliant current path springs were susceptible to lateral motion, which caused the force required for initial contact to vary, as well as impart an unwanted moment to the system at the point of contact. An SEM showing stiction in a fabricated chip is shown below in Figure 3-12.

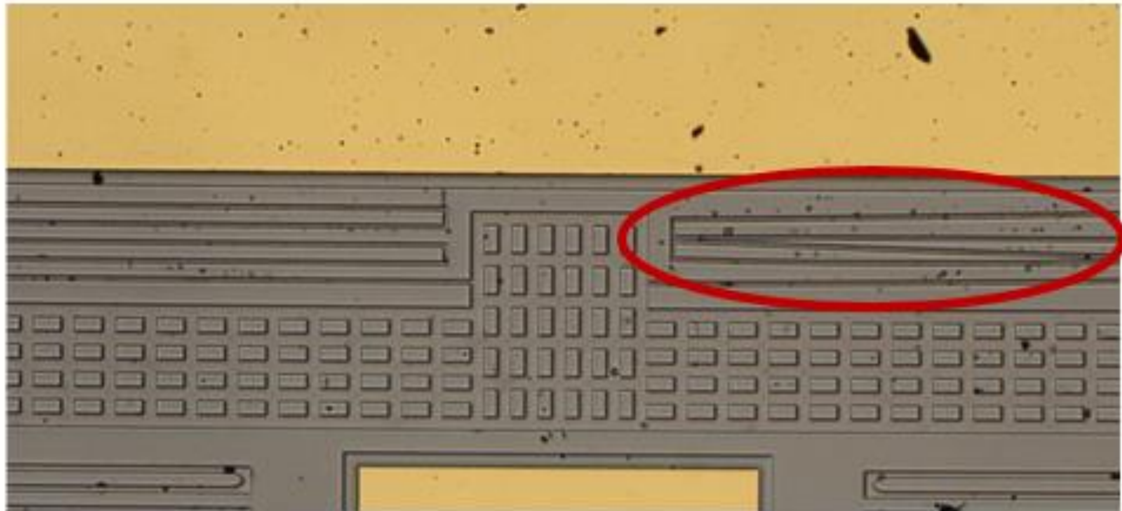


Figure 3-12. Fabrication issues with 2nd generation layout showing a chip with lateral spring stiction on the right and intended behavior on the left.

Repeatable measurements were still difficult to achieve. Even with careful and smooth motion of the probe to pull the forcing spring, electrical contact resistance readings were erratic. A 3rd generation of devices was designed to combat these new concerns.

3.2.3 3rd generation system

The electrical measurement path and corresponding structures were altered to further minimize any effect caused by erratic movement of the complaint system during force application. All electrical bond pads were designed to be rigid, removing the need for a compliant current path. With this improved design, no current flows through movable structures. The 3rd generation device AutoCAD layout is shown below in Figure 3-13.

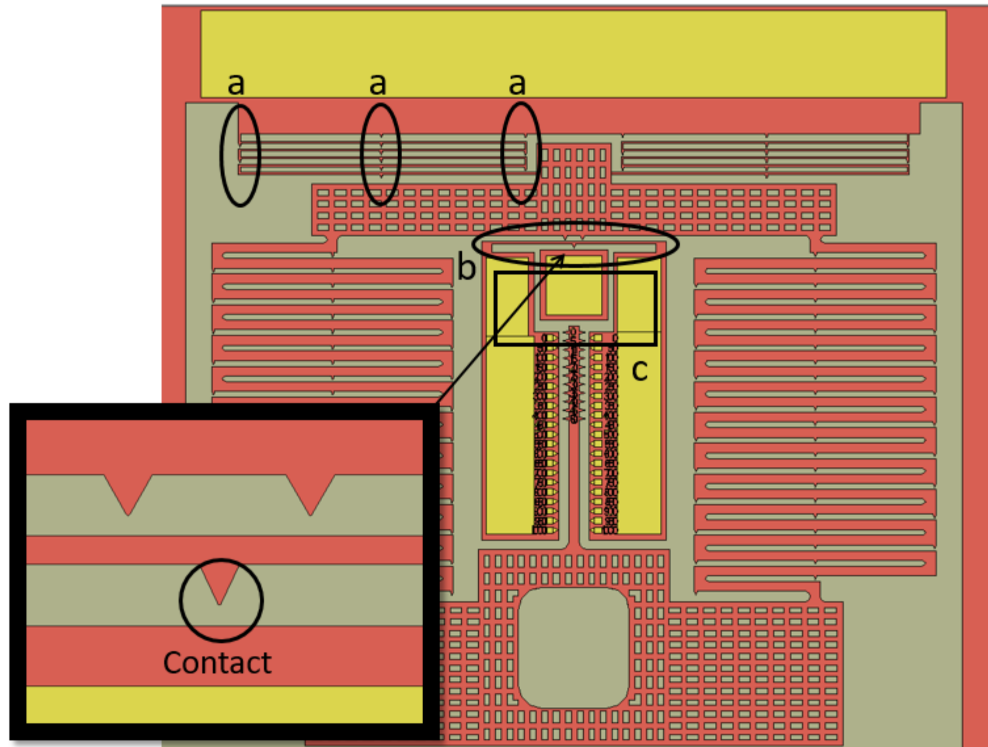


Figure 3-13. 3rd generation design of direct actuator method, showing a) added bumpers, b) built-in c) electrically isolated contacts.

Bumpers to prevent lateral stiction were added to the compliant top springs, which are no longer used as a current path to the bond pads. Built-in contacts were added in the center of the chip near the Vernier gauge. This was shown to greatly improve repeatability obtained during measurement, mostly due to a consistent point of contact. All contacts were electrically isolated from any moving structures to minimize any static build-up and capacitive effects. Finally, only line contact geometry was used to minimize scope and hone in on producing repeatable results. As a result, the design matrix shown in Table 3-5 below is greatly reduced and yield of identical chips was significantly higher.

Table 3-5. Design parameters for the 3rd generation of manually probed chips.

FORCING SPRING	
Parameter	Value
Width	40 μm
Length	906 μm
# in series	29
# in parallel	4
Spring constant	200 N/m
Max stress @ 300μm	255 MPa

LINE CONTACT CHIPS	
Chip number	Radius
1	5 μm
2	10 μm
3	25 μm
4	50 μm
5	75 μm
6	100 μm
7	200 μm

Unfortunately, testing of fabricated chips revealed an oversight in chip design of 3rd generation devices. High stress in the contact geometry support running between the connected bond pads resulted in fracture during testing in most chips. It was clear that there would not be enough testable chips and a 4th generation of chip design was necessary. In addition to this primary shortcoming, further optimizations were made to improve overall reliability of the system.

3.2.4 4th generation system

4th generation manually probed designs were kept largely the same as 3rd generation chips, with a few important improvements. The support bar that suspends the contact geometry was modified to be more compliant in the direction of contact to prevent fracture during force

application. In the same spirit, folded flexures that were laterally stiff, but compliant along the axis of movement, replaced the previously used serpentine springs. Springs were further optimized to utilize the full available space of the chip to minimize stress and maximize contact force. The resulting system is shown below in Figure 3-14.

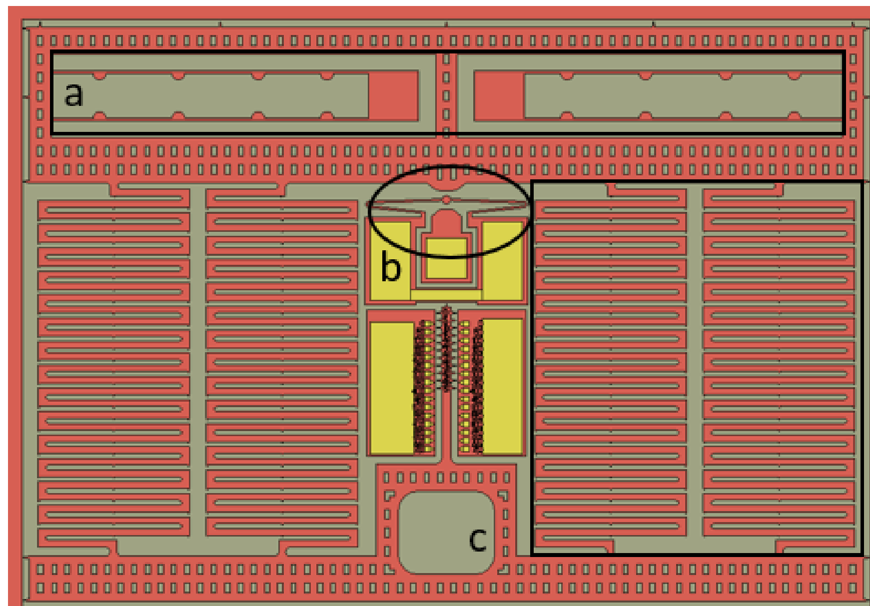


Figure 3-14. 4th generation of direct actuator method, showing a) folded flexures, b) re-designed contacting geometry and c) more robust spring assembly.

Two systems fit into one 8 mm x 8 mm chip. The same spring system was used in each device variation, and line contacts were used in all cases. Note that the design matrix is unchanged from 3rd generation chips. Finalized design parameters used in fabricated devices are shown below in Table 3-6.

Table 3-6. Parameters used in designing the 4th generation probe forcing system.

DESIGN VARIABLES			
Definition	Variable	Value	
Length	L_s	865 µm	
Width	w_s	40 µm	
Thickness	t	100 µm	
Springs in parallel	n	4	
Springs in series	m	29	
MODELED PARAMETERS			
Spring constant (analytic)	k	170.5 N/m	
Spring constant (FEA)	k	176.3 N/m	
Spring constant (analytic, thinned 2 µm each side)	k	124.3 N/m	
CONTACT GEOMETRY			
Chip name	Contact shape	Radius	Width
R5	line	5 µm	-
R20	line	20 µm	-
R50	line	50 µm	-
W5	area	-	5 µm
W20	area	-	20 µm
W50	area	-	50 µm

Testing of fabricated 4th generation chips finally led to repeatable results. Enough chips were fabricated and tested to obtain the sought-after characterization of electrical contact resistance as a function of force. No further design iterations were done to alter manual probe chip designs.

3.3 *Force by accelerated inertial mass*

Force was applied by accelerated inertial mass using a programmable rate table and packaged chips containing an embedded proof mass. As manual testing revealed pre-loading to be essential for obtaining consistent measurements, contact interfaces were first pre-loaded. A spring

assembly was pressed into the contact interface and latched with a prescribed force prior to loading by hand with a pick under a microscope. Chips were then wire-bonded to carriers, small glass shims were cantilevered over proof masses to prevent out-of-plane movement, and large glass lids encapsulated the chip carrier. Chip packages were mounted atop a 3D-printed direct-drive rotatory stage (Aerotech ADRT-100-135) assembly. The center of the proof mass was aligned to the rotational center of the rate table with a fixed 0.26 m moment arm. A Labview DAQ system recorded ECR measurements via wires soldered to the chip carrier, through a top-mounted two-terminal liquid metal slip ring (Mercotac 205-H). The rate table was actuated using a programmable Soloist motion controller (SOLOISTCP20) with pre-defined acceleration ramping via a customized program. Rotational acceleration caused the proof mass to press the contact interface together, applying force given by $F = mr\omega^2$. The ECR is again measured through the contact surfaces from R+ to R-, and electrically isolated from the proof mass. A schematic of the chip is shown below in Figure 3-15, and the testing assembly is pictured in Figure 3-16.

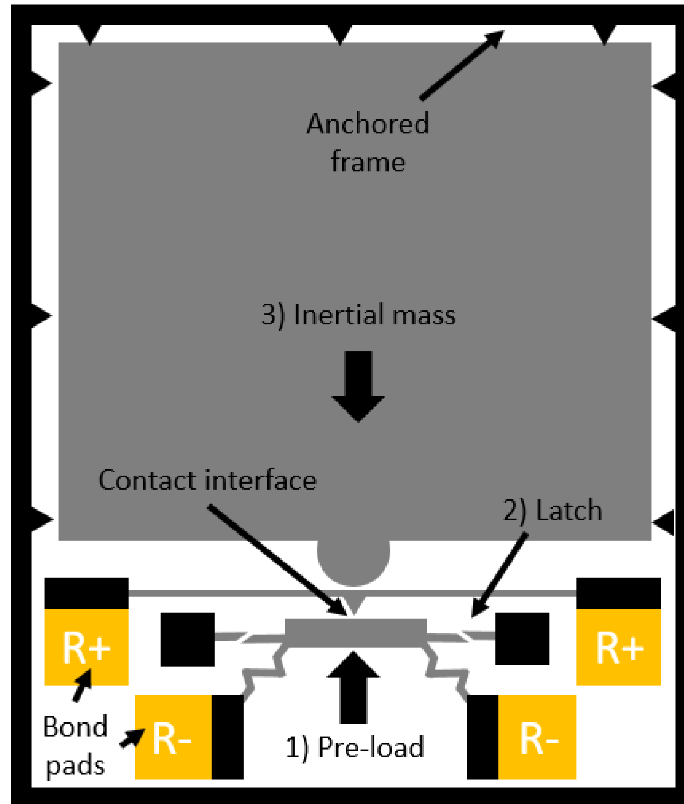


Figure 3-15. Schematic of a chip using an inertial mass to apply force to the contact interface. The bottom structure is manually displaced upwards until it latches, applying a pre-load to the contact interface. Upon latching, contact is made between the inertial mass, R+ and R-. Downward acceleration of the inertial mass causes increasing contact force at the contact interface.

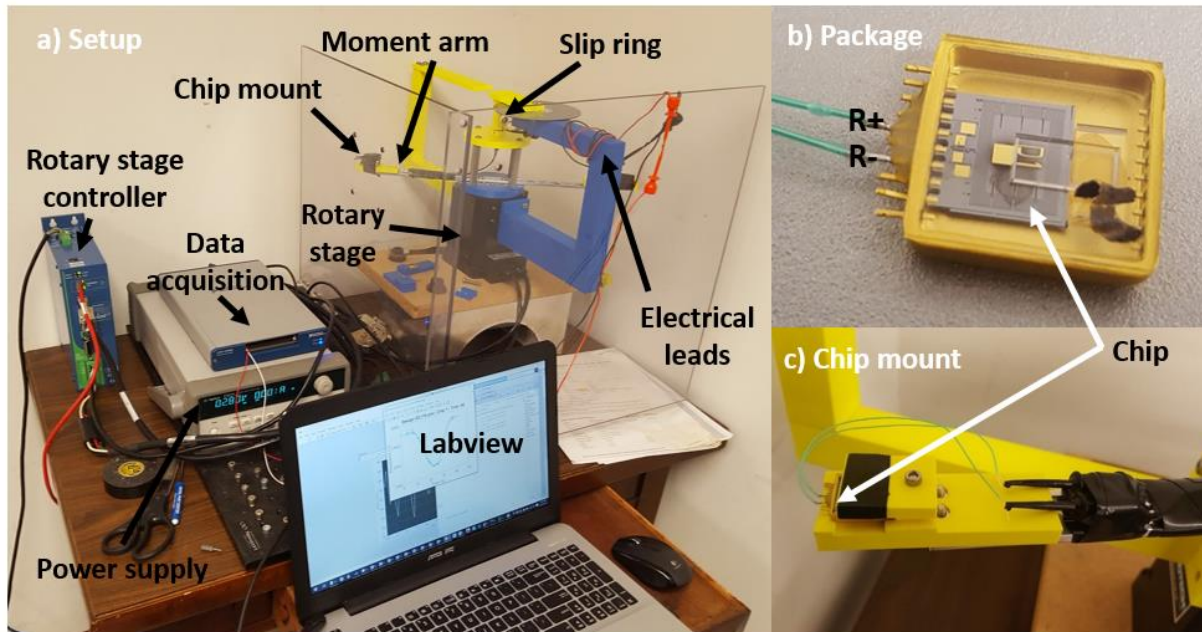


Figure 3-16. (a) Inertial testing setup with close-up views of (b) a packaged chip and (c) the 3D-printed mounting fixture.

The inertial mass was designed to be as large as possible, containing only perimeter front-side release holes, with a solid center (achieved with a back-side etch) to maximize mass. Smaller internal cantilevers and springs of negligible stiffness held the proof mass in-plane during handling. The embedded latching mechanism both pre-loaded the contact interface and applied contact with the proof mass. Acceleration was applied in the same direction as the pre-load. Clearances of 3 µm around the sides and top perimeter of the mass were defined by triangle-shaped guide pins to minimize movement. Bond pads were connected to the contact interface though the preload structure. The system was designed for operation in one direction in a single axis (two-axis dual-direction sensors were designed, but not yet tested). A fabricated chip is shown below in Figure 3-17.

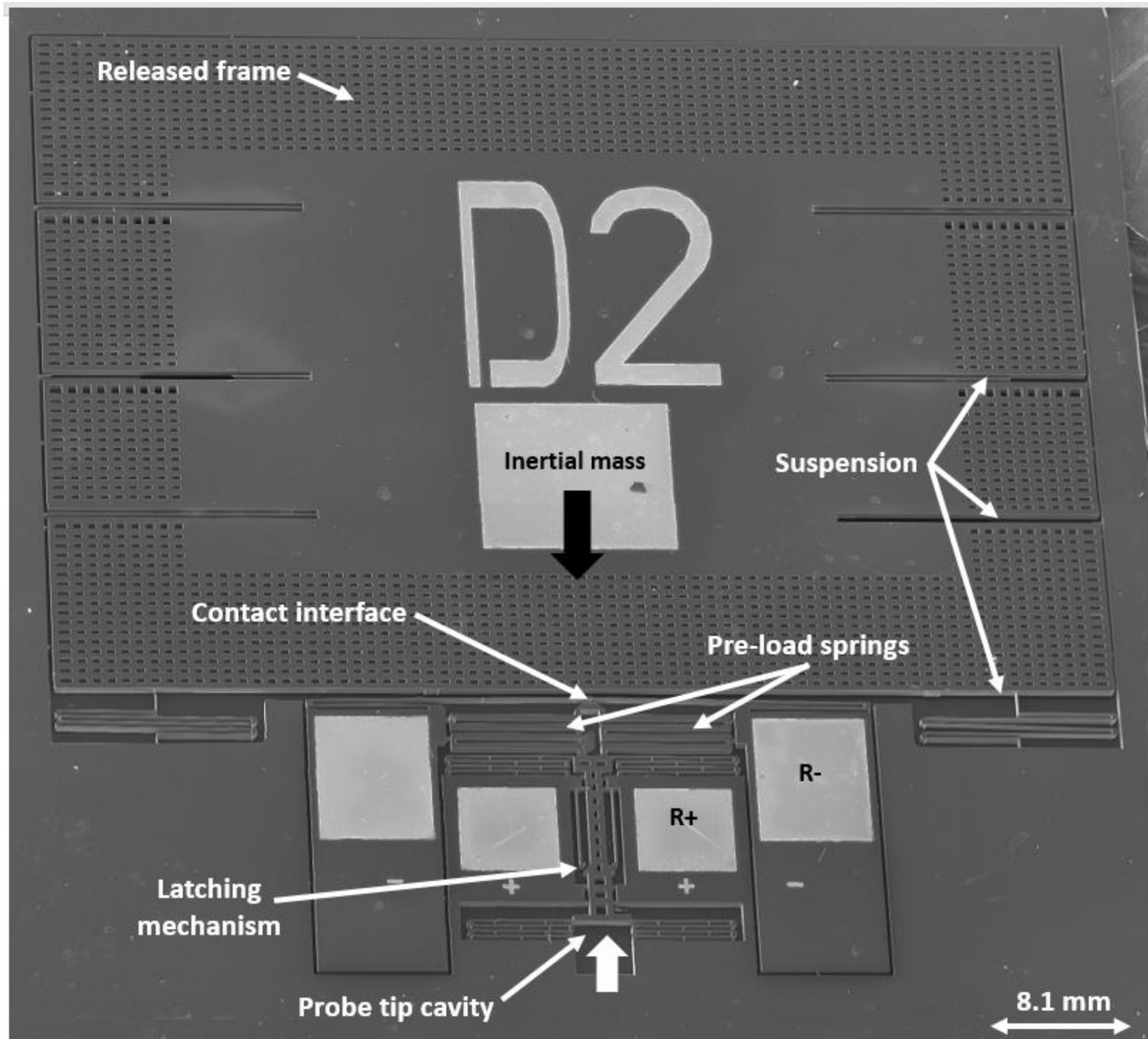


Figure 3-17 Fabricated chip where increasing contact force is applied by accelerated inertial mass.

Both single-axis and dual-axis devices were designed and fabricated, but due to the complexity and limited resources available (namely a slip ring with more than 3 feedthroughs), only single axis devices were characterized.

3.3.1 1st generation system

The proof mass was designed as a large rectangular block with a 30 µm gap between it and the contact point under force, and was designed to maximize mass (and therefore applied contact force) for the given allowable footprint. Back-side holes were etched in the center of mass, with front-side release holes along the perimeter to prevent the mass from deflecting into the etched handle layer. Six internal single-beam guide springs were located inside the mass to prevent out-of-plane deflection during handling and testing. An embedded latching system utilizing a small serpentine spring was manually elongated to apply a 25 mN preload to the contact interfaces and squeeze them in contact with the inertial mass. Once latched in place, contact between interfaces was maintained over the intended force range. The resulting AutoCAD design is shown below in Figure 3-18, which was later fabricated and tested.

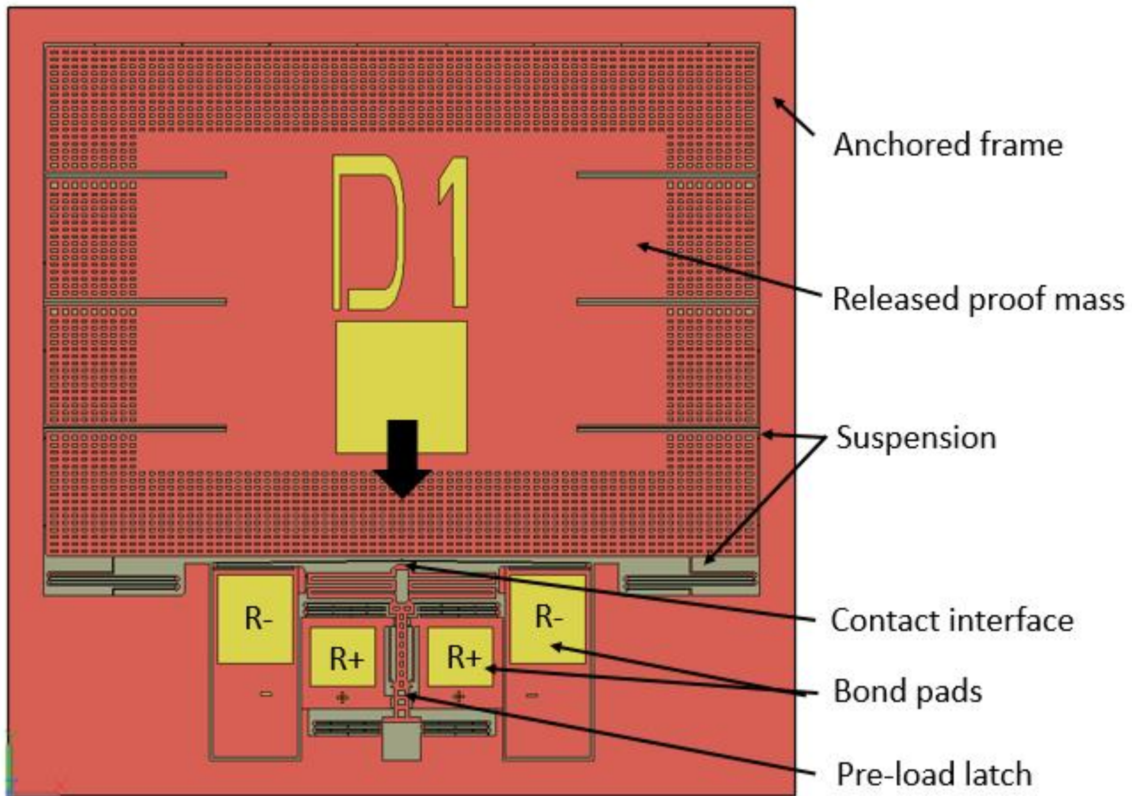


Figure 3-18. AutoCAD design showing the 1st generation chip used for applying loads via accelerated proof mass.

Design parameters for the inertial mass and compliant spring mechanism use to pre-load the contacts are given below in Table 3-7.

Table 3-7. Design matrix for the 1st generation inertially actuated chips. Note force in these chips was not calibrated.

PRE-LOAD SPRING MATRIX						
Chip letter	Width	Length	# in series	# in parallel	Force @ pre-load	Max stress @ pre-load
C	40 µm	906 µm	4	2	50 mN	215 MPa
D	50 µm	1000 µm	4	2	25 mN	133 MPa
Da	50 µm	1000 µm	4	2	25 mN	133 MPa
CONTACT GEOMETRY MATRIX						
Chip number	Contact shape	Radius				
1	line	5 µm				
2	line	10 µm				
3	line	25 µm				
4	line	50 µm				
5	line	100 µm				
INERTIAL MASS MATRIX						
Chip letter	Total solid area	Mass				
C	15.04 mm^2	3.50×10^{-6} kg				
D	41.48 mm^2	9.66×10^{-6} kg				
Da	41.48 mm^2	9.66×10^{-6} kg				
STRUCTURE TYPE MATRIX						
Chip letter	Sensing axis	Sensing direction	# pre-load springs			
C	Dual	+/-	8			
D	Single	+	1			
Da	Single	+	2			

Fabricated chips were delicate. The internal compliant beams in the center of the proof mass were not strong enough to prevent the mass from coming out of plane during handing. As a result, chip yield of these designs was quite low, although enough were salvaged to gather initial

experimental results. A design revision was done to improve chip yield (and fabricate more chips for testing).

3.3.2 2nd generation system

A 2nd generation design was created to improve strength and reliability of the system, without affecting operation or characterization. Minor enhancements were made to several parts of the system, and the resulting AutoCAD layout is shown below in Figure 3-19.

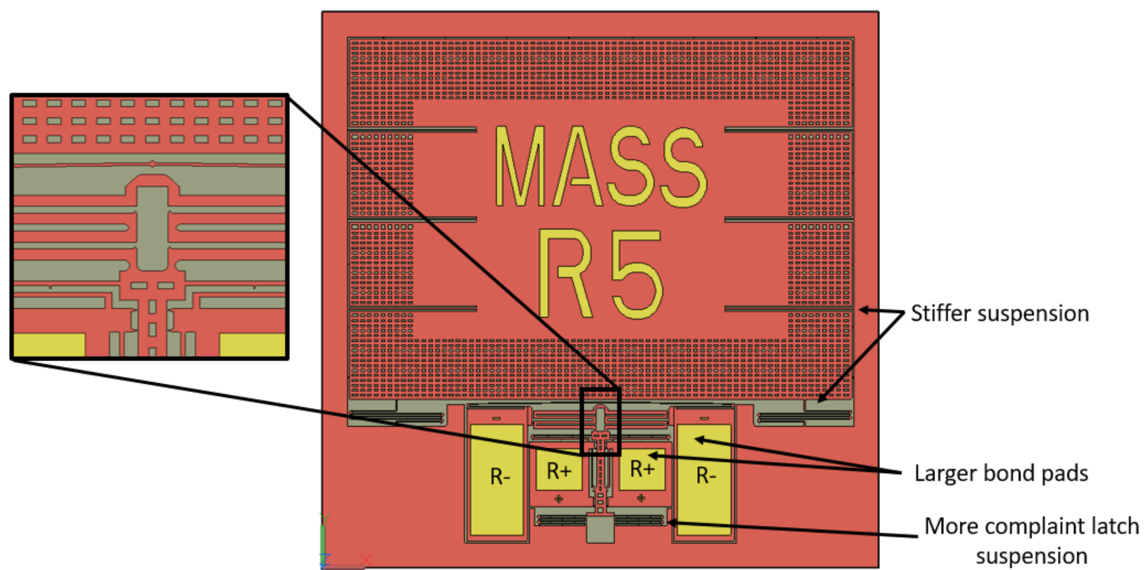


Figure 3-19. AutoCAD design showing the 2nd generation of the single axis single direction chip used for applying loads via accelerated proof mass

Since this design was already verified to be working, only a single design was fabricated to maximize the number of identical chips for repeatability testing. The design matrix is shown below in Table 3-8.

Table 3-8. Design parameters for 2nd generation inertially accelerated chips.

CHIP PARAMETERS	
Contact shape	line
Contact radius	5 μm
Inertial mass	9.66×10^{-6} kg
Total solid area	41.48 mm^2
Total pre-load force	25 mN
Sensing axis	one
Sensing direction	one

Fabricated chips were found to have much higher yield than previous versions. Proof masses no longer fell out of the device and wire bonding was easier due to increased bond pad size. These chips were tested, and were the final design revision fabricated. Shown below is a fabricated inertial chip prior to pre-load (Figure 3-20(a)) and after engaging the pre-load mechanism by hand with a pick (Figure 3-20(b)).

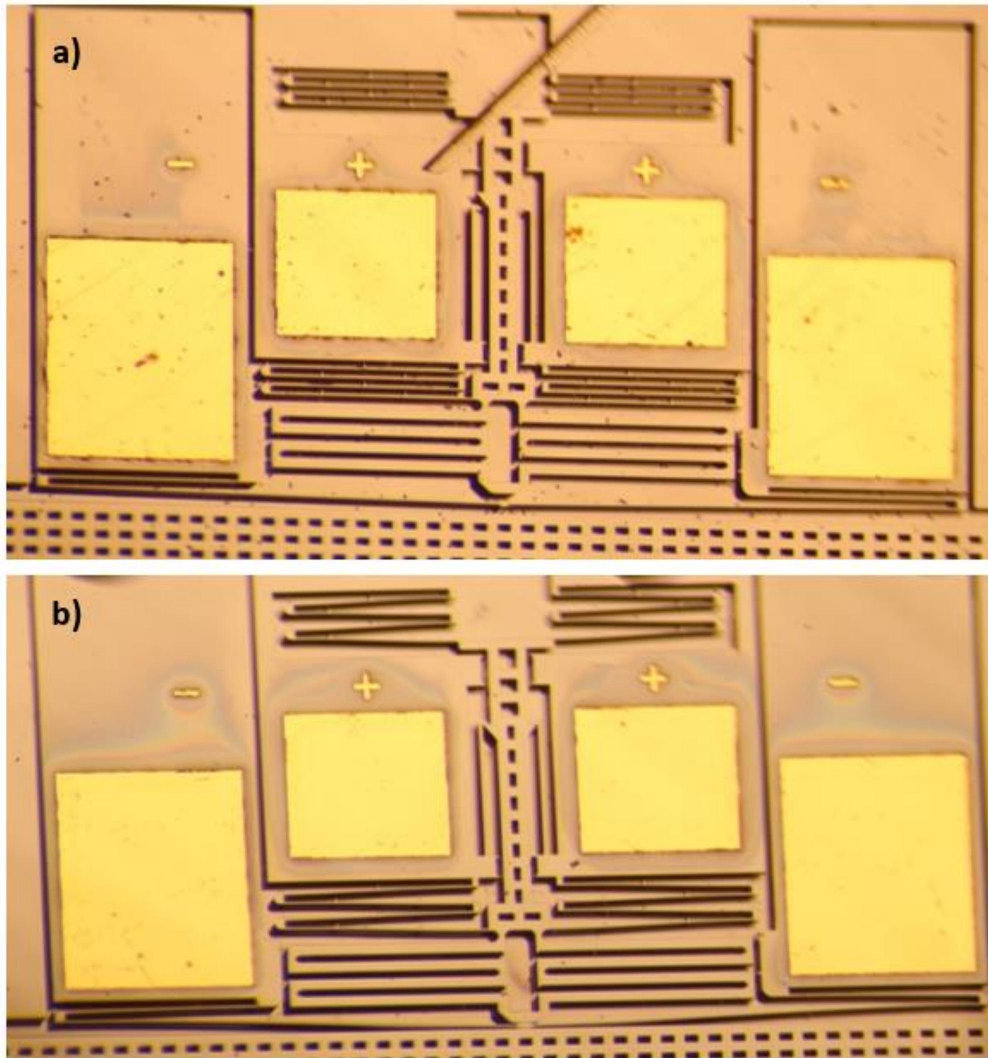


Figure 3-20. Pre-load mechanism of a fabricated inertial chip shown (a) prior to pre-load and (b) after pre-load.

Table 3-9. Parameters used in designing the inertial mass and pre-load spring. Note that the analytic spring constants reported are calculated from the model in 2.2.1.1 adjusted using 4 μm thinner spring widths resulting from DRIE tapering (found through experimental calibration in 5.1)

INERTIAL MASS	
Length	8100 μm
Width	5820 μm
Solid area	41.3 mm^2
Mass	9.66 x 10^{-6} kg
TOP SPRING	
Length	900 μm
Width	50 μm
Springs in parallel	2
Springs in series	4
Deflection	33 μm
Spring constant (analytic, calibrated)	781.3 N/m
TOTAL APPLIED FORCE	
Spring constant (analytic, calibrated)	25.3 mN

3.3.3 Two-axis concept system

More complex designs able to sense force in ± X and Y were created and fabricated, although not tested due to complexity and cost. The AutoCAD layout for fabricated devices is shown below in Figure 3-21.

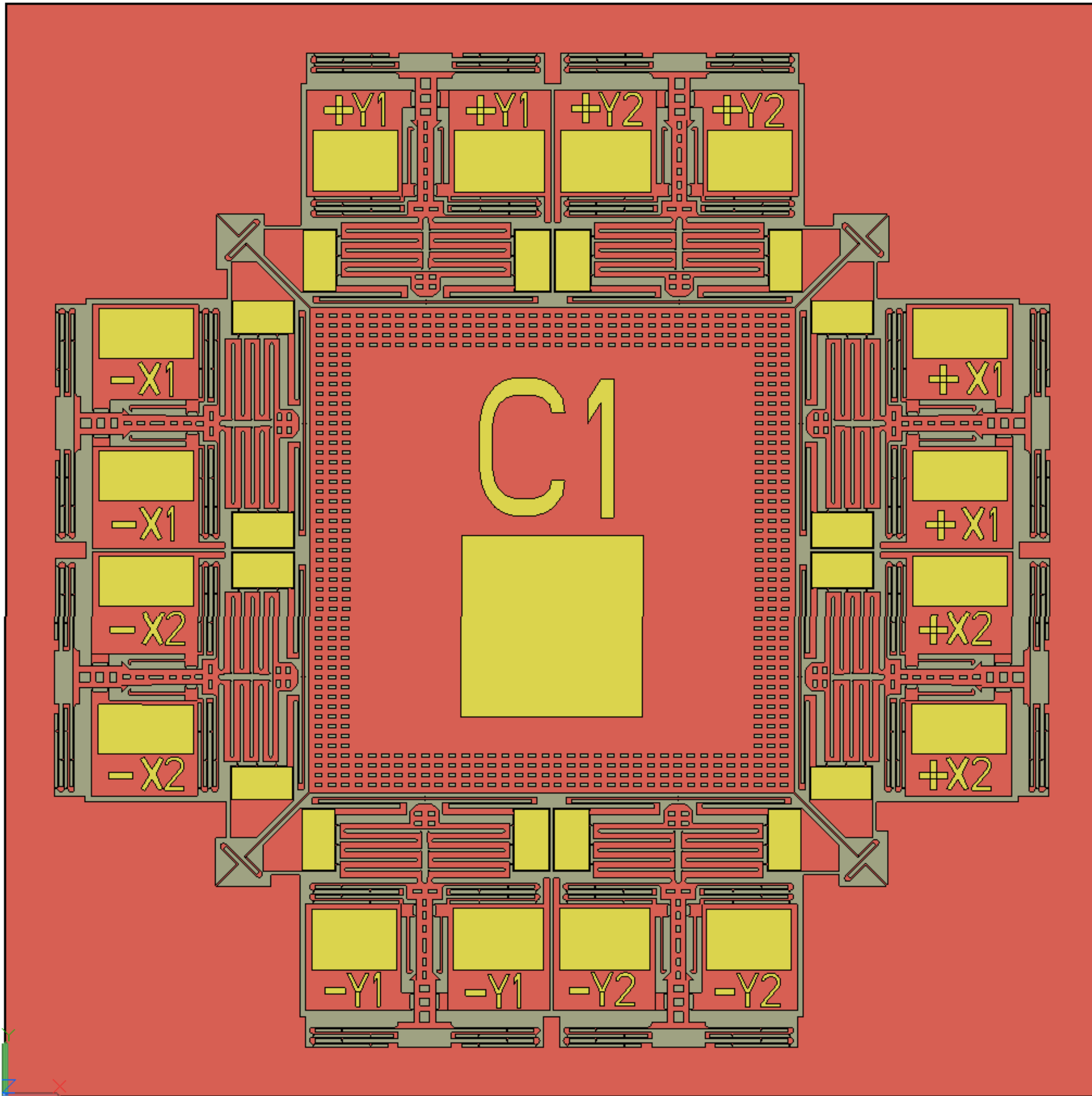


Figure 3-21. AutoCAD layout of conceptual dual-axis inertial chip

These chips were designed as a proof-of-concept to sense in all planar directions, and were not tested.

Chapter 4: Fabrication

All chips were fabricated in an SOI/DRIE process using 10 cm SOI wafers with a 100 µm thick device layer (boron doped at 10^{18} atoms/cm^3, resistivity of 0.005 Ω-cm), 2 µm thick buried oxide, and 500 µm thick handle layers.

Table 4-1. Wafer specifications for all SOI wafers used in this work.

WAFER SPECIFICATIONS	
Diameter	100 ± 0.2 mm
Finish	Double side polished, TTV < 2µm
DEVICE LAYER	
Thickness	20 ± 0.5 µm
Resistivity	< 0.005 ohm-cm
p-type, Boron	<1-0-0> ± 5%
BURIED OXIDE LAYER	
Thickness	2 ± 5% µm
HANDLE LAYER	
Thickness	500 ± 10 µm
Resistivity	> 2000 ohm-cm
p-type, Boron	<1-0-0> ± 5%

All chips were fabricated using similar processes, however, chips for early tested were segmented by dicing saw, and chips for later tested were cleaved using DRIE etch lanes.

4.1 <u>Diced segmentation</u>

A 2-mask fabrication sequence was used to process the first two generations of wafers. Table 4-1 below gives the properties of the SOI wafers used for fabrication.

Wafers were first cleaned of any residual organics using a Piranha mixture (3 H_2SO_4:1 H_2O_2) and then dipped in hydrofluoric acid (49% HF) to remove the accumulated surface native oxide layer to ensure minimal resistance between the upcoming bond pad layer.

Electron beam evaporation (Evatek BAK641, Trübbach, Switzerland) was then used to deposit the metal stack, consisting of a 300Å Cr adhesion layer, 500Å Ni diffusion barrier, and 2000Å Au bond pad surface.

Wafers were subsequently processed to add the top-side metal layer, which functioned as both the bond pad layer and wafer dicing lanes. Wafers were vapor primed with hexamethyldisilazane (HMDS) to promote photoresist adhesion, followed by spin-coating 6 µm of AZ9245 photoresist, which was soft-baked for 120 seconds at 110℃. Contact lithography using a Karl Suss MA6/BA6 mask aligner was used to transfer Mask 1 (top-side metal etch) to the photoresist with a UV exposure time of 60 seconds (250 mW/cm^2) and development time with a mean of 5 minutes. Note that careful balancing of photolithography thickness, exposure time and development time was essential due to the fine resolution Vernier gauges utilized in the chip designs. Following development of the photoresist pattern, the Metroline plasma asher/etcher was used to run a 5-minute descum process (O_2 = 500 sccm, P = 1000 mT, RF = 400 W) to remove any surface organics in lithography trenches. The metal layer was then etched via timed ion milling for 45 minutes (4Wave PSIBE, Sterling, Virginia). Note that initial fabrication runs revealed that charring occurred during the etch process, leaving a residue on the perimeter of the bond pads. To overcome this issue, the under-side cooler plates that held the wafers were set to 10 C to help avoid charring during the high-temperature process. Following etch, the wafers were then placed in a heated PRS3000 bath (80 C) for 1 hour to strip the remaining photoresist. A solvent bath using, in order, acetone, methanol and isopropanol was used to further clear remaining photoresist. Wafers were subsequently placed in the Metroline and plasma ashed for 20 minutes (O_2 = 500 sccm, P = 1000 mT, RF = 400 W) to clear remaining remnants of any organics.

Next, wafers were front-side etched to form the device layer. A 9 µm of AZ9245 photoresist was spin-coated atop the front-side, covering the metal pattern. Note that since the metal layer is less than 1 µm, the photoresist had no issue covering and filling the trenches of the existing topology. Mask 2 (top-side Silicon etch) was applied to the photoresist in the same manner as during bond pad processing, followed again by a surface cleaning 5-minute descum. A 3600-second timed DRIE (Plasma-Therm Versalock 700, Saint Petersburg, FL) was then used to etch the front-side Silicon down to the buried oxide. Following the etch, photoresist was again stripped using PRS3000, acetone, methanol, isopropanol and plasma ash.

In preparation for dicing, wafers were slowly spin-coated in ~30 µm of AZ9245 for protection from debris. The spin-coating was done manually on a spinner at about 500 RPM to ensure full coverage of the wafer, followed by a soft-bake at 110C for 60 seconds. Wafers were then diced into 8 mm x 8 mm chips using a 250 µm thick dicing blade to cut through the 250 µm thick dicing lanes. While still attached to the adhesive film from dicing, diced wafers were given a PRS3000 bath for about 5 minutes, followed by a triple solvent bath and drying process in a convection oven at 80 F for about 20 minutes. Finally, individual chips were placed into a Primaxx HF vapor etcher to release the chips from the underlying buried oxide layer. The resulting chips were used for experimental testing. The fabrication process is shown below in Figure 4-1.

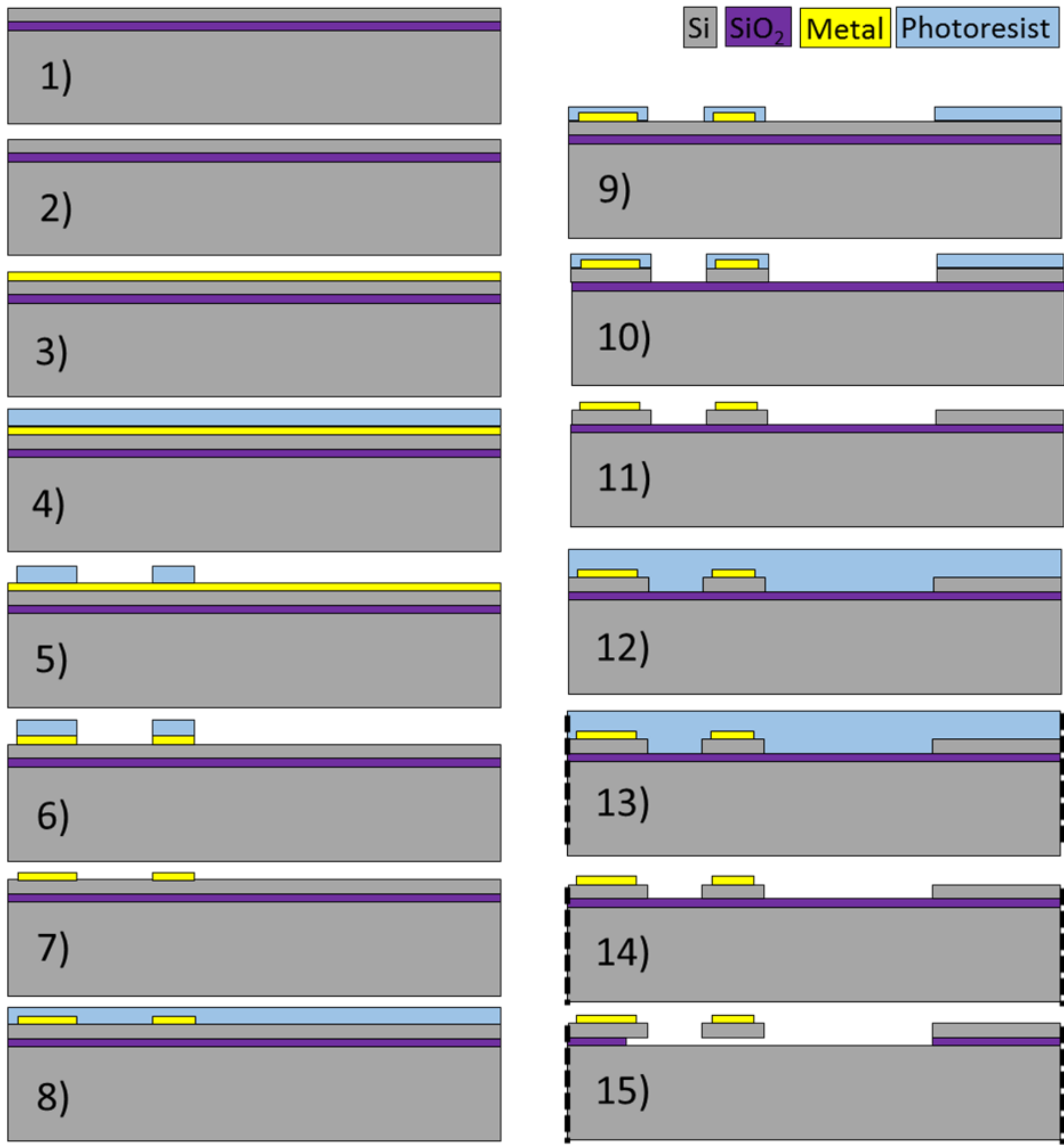


Figure 4-1. Fabrication process flow used in the fabrication of the first two generations of chips.

A typical wafer (1st generation devices) is pictured below in Figure 4-2 after dicing and prior to clean and HF release.

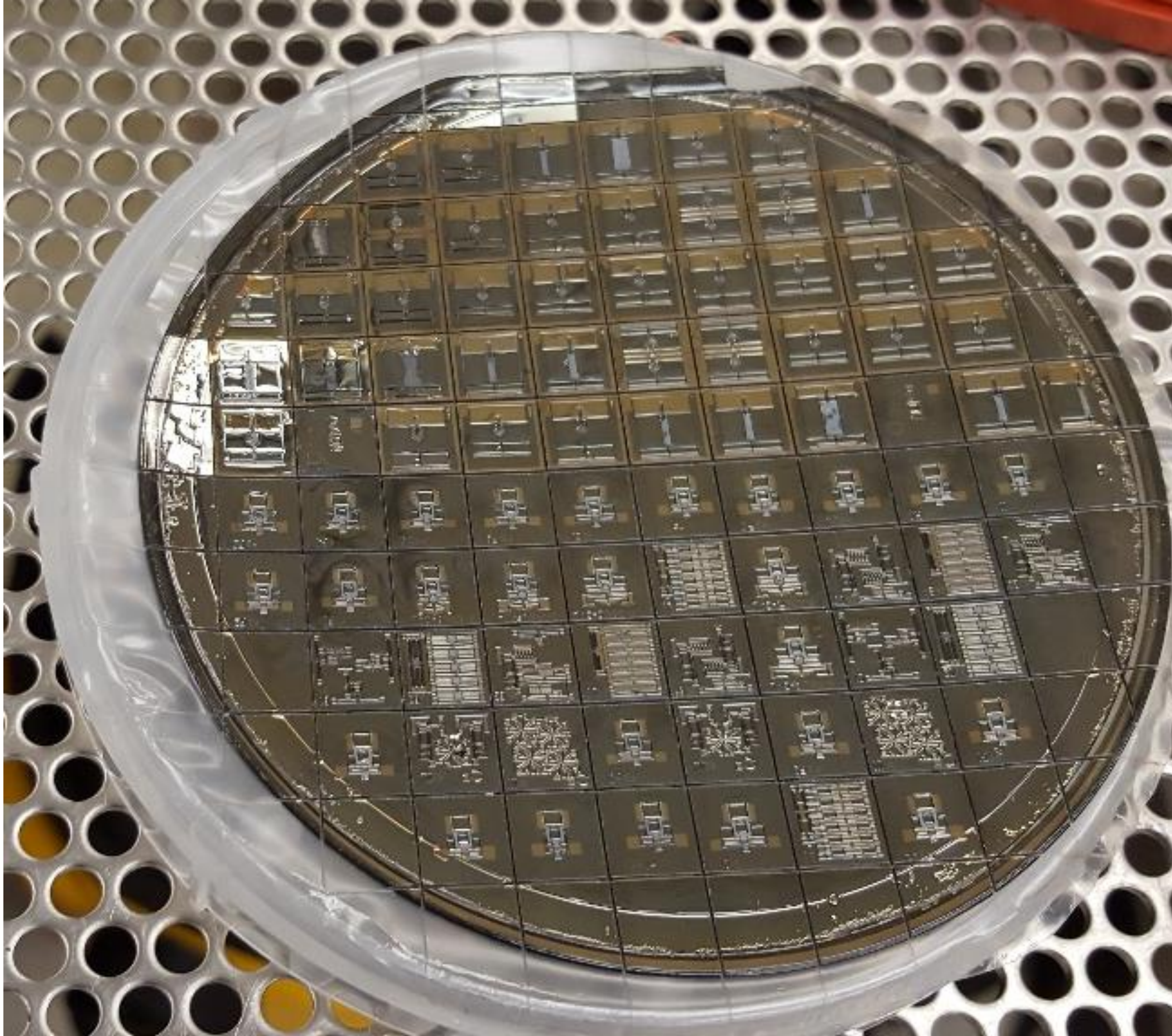


Figure 4-2. Picture of wafer immediately after dicing.

An SEM image is shown below in Figure 4-3 of a fabricated 2nd generation manually probed chip design, which used the same fabrication process.

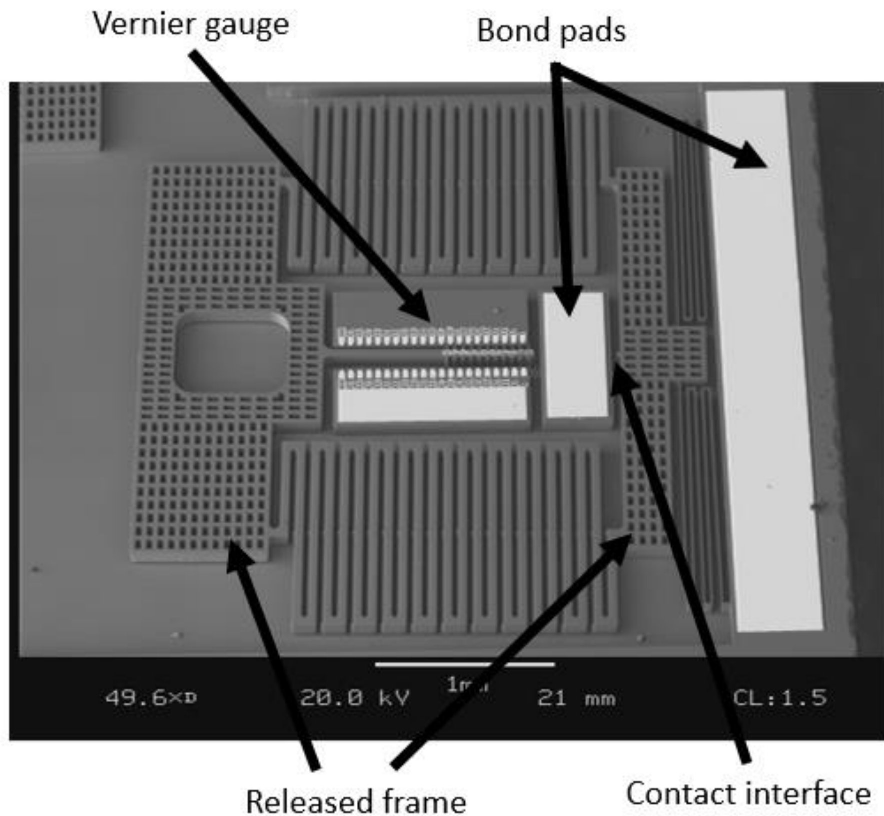


Figure 4-3. SEM image of a fabricated chip utilizing a probe for manual actuation. Note that the probe pulls the left-side frame to the left, elongating the central serpentine springs.

This fabrication process produced relatively good yield. The clear majority of chip loss occurred during cleaning between dicing and release. Between having to clean each individual chip and transfer back and forth between solvent baths, the relatively fragile structures within each chip tended to fracture or fall out of the chip entirely. To mitigate this issue, the dicing saw was abandoned in favor of including cleave lines within the front and back side lithography patterns to allow segmentation by manually applying pressure on the corner of each chip. This proved to be a vast improvement to yield as well as a significant time saver. The downside on this approach is the requirement for an additional back-side DRIE to create the segmentation lanes.

4.2 <u>Cleaved segmentation</u>

Fabrication modified to include a back-side etch for chip segmentation by cleaving as opposed to dicing. Following cleaning, metal layer formation and front-side etch (which now includes trenches for DRIE segmentation), back-side trenches were formed. A thick 16 μm AZ9245 photoresist layer was spin-coated on the back-side of the wafers to account for the upcoming 500 μm back-side through-etch. A 70 second exposure using a third mask, followed by a 5-minute develop and 5-minute descum finalized the back-side lithography. It is nice to note here that the back-side etch eventually incorporated back-side holes into later device designs. A 12500 second back-side DRIE formed the back-side dicing lanes. Resulting dicing lanes were transparent to the naked eye, except for the small break-away tabs holding the chips in place. Remaining photoresist is again stripped using PRS3000, acetone, methanol and isopropanol, followed by a plasma ash to remove remaining organics. Wafers were then released via HF vapor, and simply segmented by pressing on each break-away tab with a scalpel. Segmented chips are shown below in Figure 4-4(a), and the leftover wafer in Figure 4-4(b).

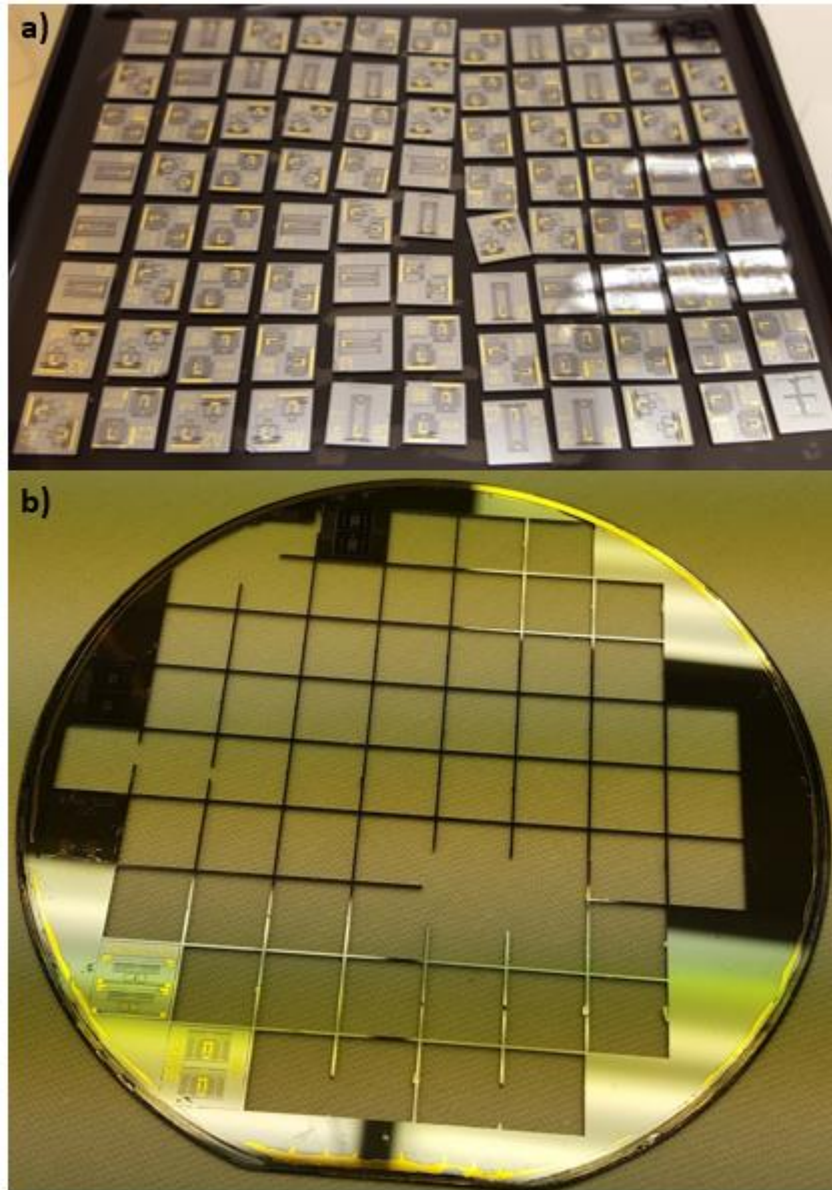


Figure 4-4. Images showing a) segmented chips after fabrication with b) remaining wafer after removal of break-away chips.

Yield using this updated fabrication technique was dramatically increased. This fabrication process was used for all remaining fabrication.

Chapter 5: Experimental results

Experimental testing was done in 3 phases, each of which utilized a different method to apply cyclical contact force to contacting DRIE interfaces during ECR-force measurements. First, the feasibility of using ECR to sense force in bare DRIE silicon contacts was evaluated using force applied by simple thermal actuation. Second, relative performance, effects of varying contact geometry microsystem constraints on ECR-force behavior was investigated using manual spring elongation. Third, sensitivity and repeatability within single chips and groups of chips were quantified using force applied by inertial acceleration of embedded proof masses in packaged chips.

5.1 Measuring stiffness of fabricated spring

Stiffness of fabricated in-situ spring assemblies were experimentally measured to compare with predictions of FEA and analytical models. While planar dimension variance dictated by lithography resolution was not expected to measurably impact stiffness of fabricated structures, commonly occurring undercut and sidewall tapering resulting from DRIE (Figure 5-1) slightly reduced the effective width of all etched structures. Since reported experimental results utilized final device designs that were fabricated using identical fabrication tools, processes, recipes, and parameters, effective width reduction of microsystem elements from DRIE was assumed to be equal in all cases. Variance in stiffness of fabricated chips was still likely due to varying location on wafers and slightly different etchant behavior during processing.

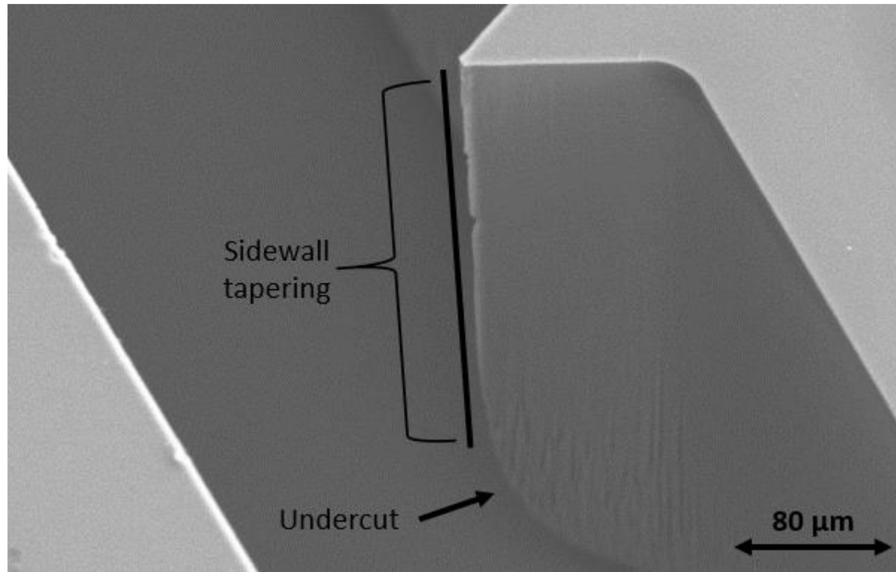


Figure 5-1. SEM micrograph showing commonly occurring sidewall taping and undercut of a contact interface.

As the maximum displacement of stiffness elements in thermally actuated and inertially loaded chips was only 60 µm, manually loaded chips with spring elements that experienced displacements up to 300 µm were best suited for measuring force over a large displacement range to maximized resolution. For this reason, stiffness of fabricated spring elements was measured using a force probe to displace spring structures within manually loaded chips. Stiffness was calculated using Hooke's Law, $k = F / x$, where x is the displacement of, and force applied to, the spring structure by the force probe. A schematic of the testing process is shown below in Figure 5-2, while the entire testing assembly for measuring applied force during displacement of the manually loaded *in-situ* springs is shown in Figure 5-3.

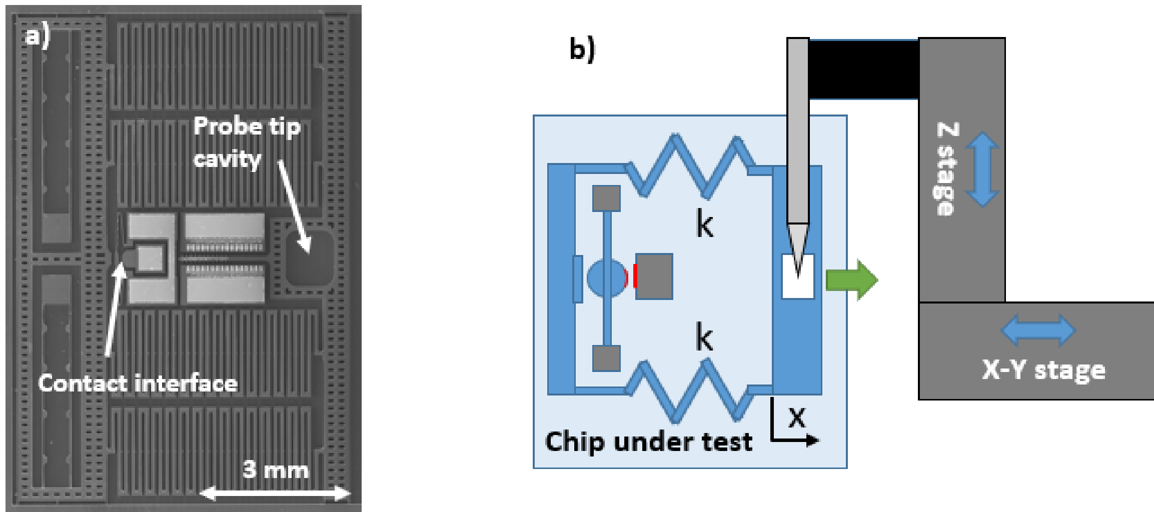


Figure 5-2. a) SEM of the 4th generation chip with force applied by manual spring elongation, and with which stiffness of spring assemblies was experimentally measured, and b) a schematic of the testing procedure.

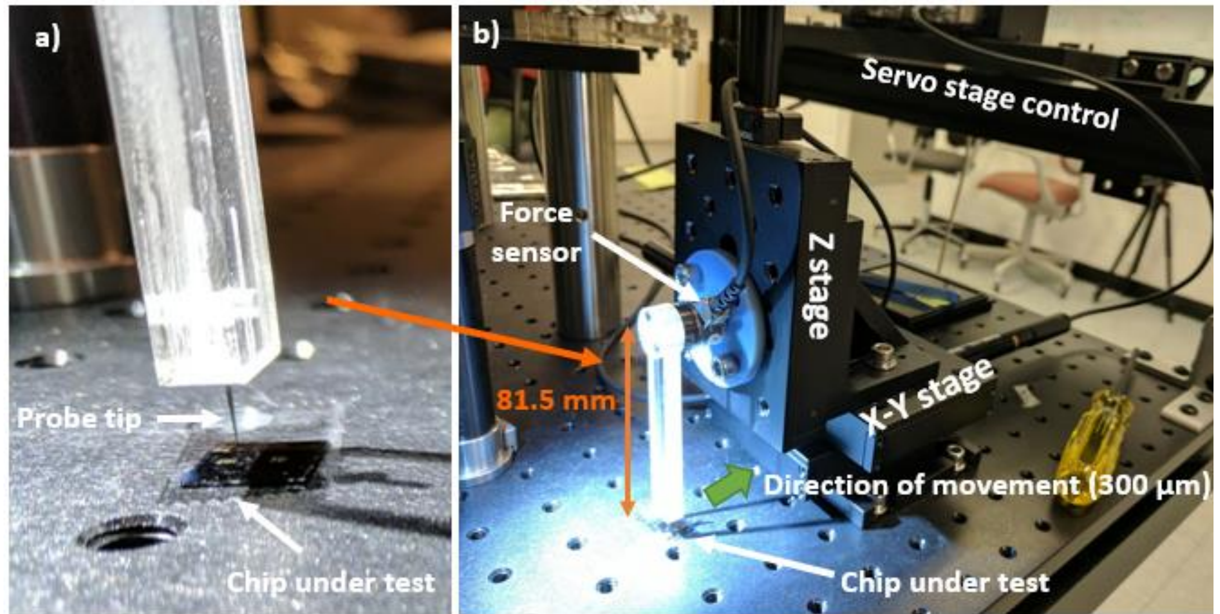


Figure 5-3. Testing setup for measuring the spring force of manually loaded chips, showing a) close-up of the probe tip within the chip cavity, and b) the overall test setup with force probe, servo stage, and the chip under test. Note that the force gauge measured torque, and force was calculated through division of the 81.5 mm moment arm.

Chips were carefully placed on an adhesive layer to prevent movement of the chip during displacement of the spring assembly. The force sensor (ATI Nano17 F/T Sensor, 12 N max, 1/360 N resolution) was mounted vertically to an XYZ servo stage located next to the chip. Chips were aligned to the X-axis of the servo stage by first placing the chip into contact with the side of the stage, and then backing the stage directly away to ensure minimal angle offset during force measurement. The servo controllers were connected to an adjacent PC, and dedicated software was used to step the motor at pre-programmed cycles. A 3D-printed structure was fabricated to attach to the force sensor on one end, and hold a probe tip on the opposite end that was used to physically pull the force spring assembly within the chip. Since the probe tip cavity of the chip was quite small (500 µm x 580 µm), the probe tip was carefully aligned and lowered

into the cavity using the servo stages. Once the tip was inside the cavity, the X-Y stage was cycled in a single direction using pre-programmed 10 µm increments over a 300 µm distance forwards, and then backwards over the same 300 µm distance. Thanks to Abraham Simpson Chen for his invaluable help with this setup and testing in Dr. Bergbreiter's lab

Force was measured from the sensor following contact between the probe tip and inner cavity wall of the chip, indicated by an initial change in force of the sensor. Note that the force gauge measured torque, and force was calculated simply through division of the 81.5 mm moment arm. While force measurements were expected to produce accurate results of each tested chip, unintended variation in applied force likely resulted from several issues that were difficult to control. Force probe misalignment, friction of the probe tip on the bottom surface, stage movement inaccuracy, and underlying debris could have contributed to inaccurate force measurement.

Six 4th generation chips where force was applied by manual spring elongation were force cycled three times each. As with force cycling while gathering resistance measurements, some chips experienced smooth curves, some were bumpy, and some experienced intermittent snagging and movement obstructions. Figure 5-4(a) shows typical force versus displacement behavior for a spring assembly that experienced intermittent movement obstruction (most commonly caused by debris lodged underneath and in between spring folds), and Figure 5-4(b) shows consistently bumpy behavior likely caused by scraping of the probe tip on the inner sidewall of the cavity.

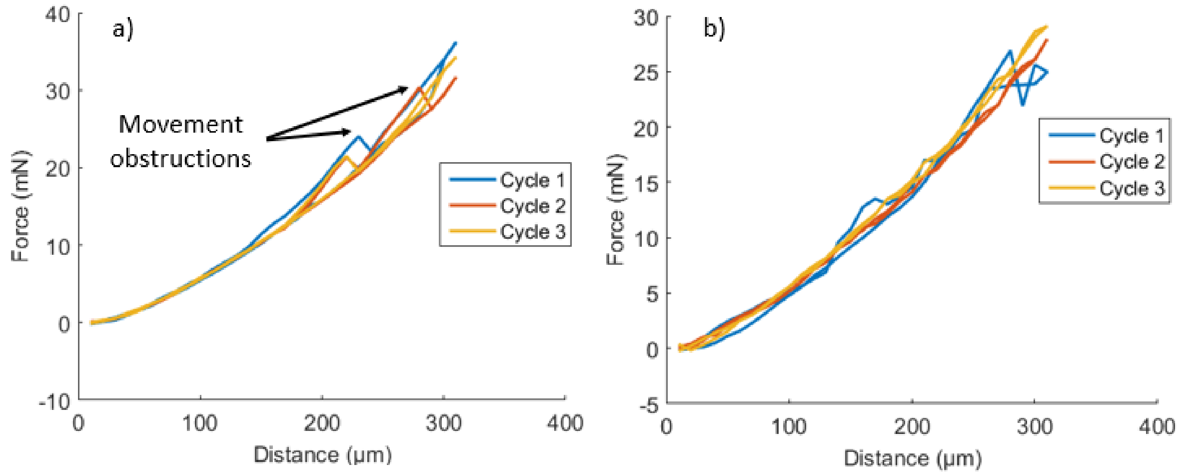


Figure 5-4. Force versus displacement curves for two different chips highlighting a) movement obstructions during spring elongation causing spikes in the force curves, and b) non-monotonic behavior in stiffness curves.

For all six tested chips, the average single-chip relative standard deviation, or the standard deviation divided by the mean (5-1), was 4.0%, chip-to-chip RSD (5-2) was 7.4%, and average single-chip hysteresis (5-3) was 4.5%.

$$single\ chip\ RSD = \sigma_n = \frac{\sigma_{\bar{x},n}}{\bar{x}_n} \cdot 100 \tag{5-1}$$

$$chip - to - \ chip\ RSD = \sigma = \frac{\overline{\sigma_{\bar{x}}}}{\bar{x}} \cdot 100 \tag{5-2}$$

$$single\ chip\ hysteresis = \mathbb{J}_n = \frac{\overline{\Delta x_{FW-REV,n}}}{\bar{x}_n} \cdot 100 \tag{5-3}$$

During ECR-force characterization in the probe station, factors that caused roughness of force-displacement curves were minimized by visually confirming that displacement occurred

smoothly while measurements were recorded. Chips whose spring assemblies displaced smoothly are shown below in Figure 5-5.

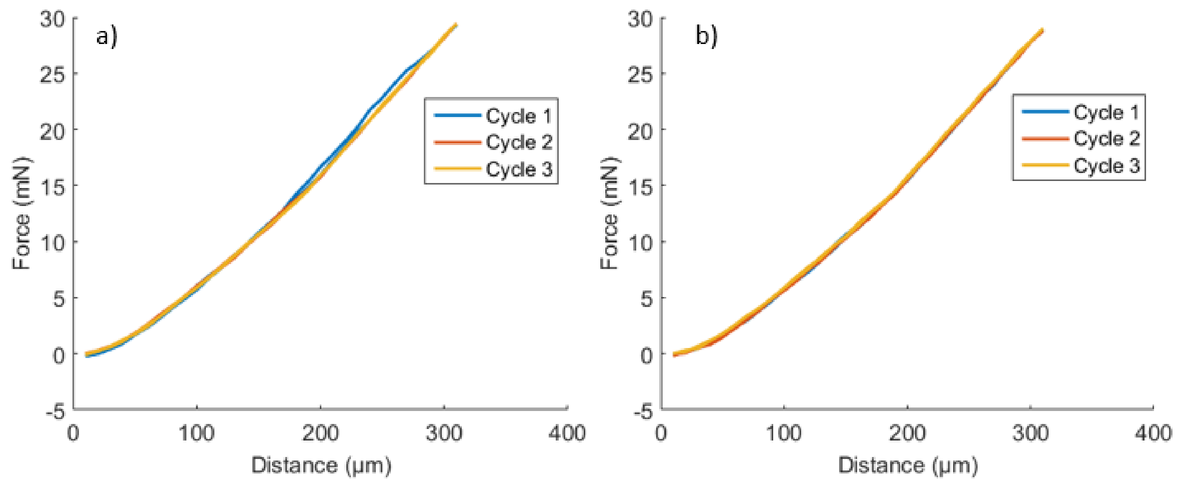


Figure 5-5. Force versus displacement curves for two different chips exhibiting smooth stiffness curves

For the three tested chips with smooth force-displacement curves, average single-chip RSD was 1.7%, chip-to-chip RSD was 6.4%, and average single-chip hysteresis was 1.8%. Maximum standard deviation of experimentally tested chips with smooth force-displacement curves was ± 1 mN, for a total variance of 2 mN. As a result, spring constants and applied force through the work were deemed to be accurate to within 2 mN.

Figure 5-6(a) below shows the overall results from all chips, and Figure 5-6(b) shows the subset of only tested chips that did not experience movement obstructions during force cycling.

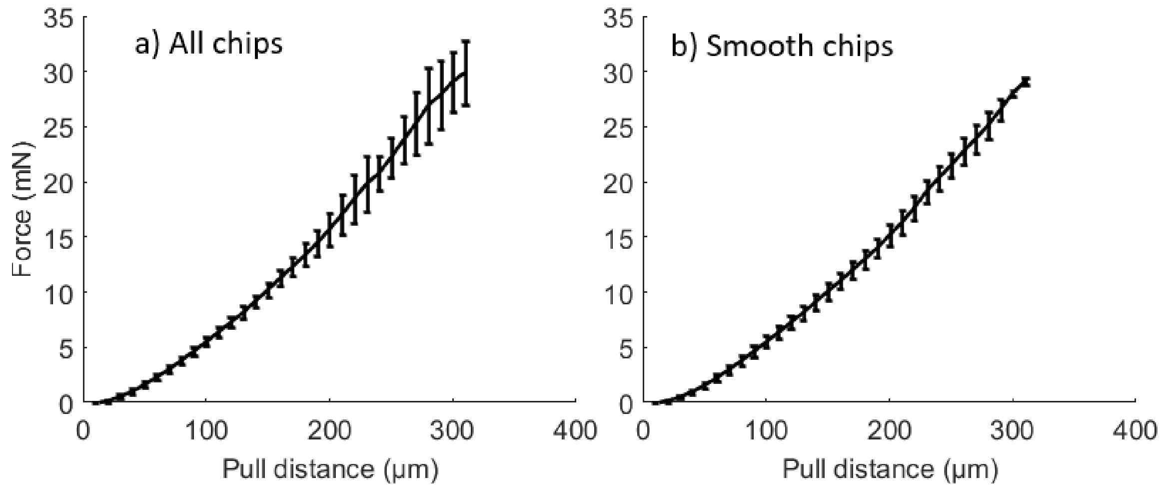


Figure 5-6. Force versus displacement curves with included error bars depicting relative standard deviation for a) all tested chips and b) tested chips with smooth force curves.

For chips that exhibited smooth force-displacement curves, the average spring constant was calculated over pull distances greater than 100 μm (the starting distance at which chips were experimentally tested during ECR-force characterization). A linear fit of the data with corresponding stiffness of k = 120.7 N/m shows close approximation of the obtained results, as shown in Figure 5-7 below.

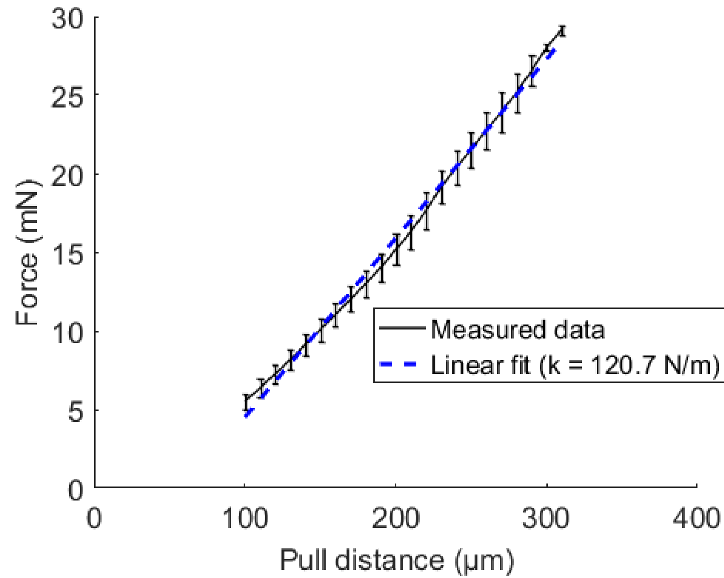


Figure 5-7. Experimental data for chips with smooth force-displacement curves at pull distance greater than 100 µm, showing linear fit corresponding to stiffness of k = 120.7 N/m.

Again, due to the uncertainty in measured spring constants of fabricated chips, the applied force throughout this work is expected to be accurate to within 2 mN at all applied forces.

5.1.1 Comparison with modeling

The average measured spring constant was compared with modeled spring stiffness to determine the effective width reduction of etched structures caused by DRIE tapering and undercut. Again, since reported experimental results utilized final device designs that were fabricated using identical fabrication tools, processes, recipes, and parameters, effective width reduction of microsystem elements from DRIE was assumed to be equal in all cases. Reducing the width of sidewalls in the model was done by simply reducing width, w_s, in (2-15).

The modeled spring constant and modeled spring constant with reduced width (thinned by 2 µm on each side of the spring) are plotted below in Figure 5-8 overlayed on the experimentally obtained spring-force data.

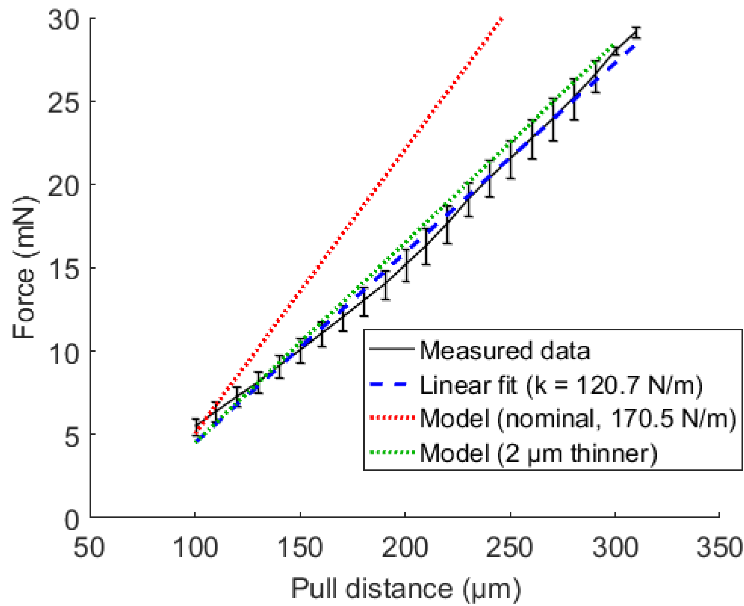


Figure 5-8. Measured data with linear fit shown compared to the nominal analytic model and analytic model with sidewalls thinned by 2 µm on each side.

Average linear spring constant for experimentally tested spring assemblies is compared to the analytic and FEA model predictions in Table 5-1 below.

Table 5-1. Comparison between experimentally measured and modeled spring constant for chips with force applied by manual spring elongation (geometry and material property parameters located in Table 2-10). Maximum standard deviation of measured spring stiffness was 6.7%.

MANUAL SPRING ELONGATION	
Method	Spring constant
Analytic	170.5 N/m
FEA	176.3 N/m
Experimental	120.7 N/m
Analytic (2 µm thinned sidewalls)	124.3 N/m

The reduced spring constant that was found experimentally, as compared to the models, is due to the effective reduction in sidewall thickness caused by undercut and sidewall tapering during DRIE processing. By varying the effective sidewall thickness in the analytic model to reduce the output spring constant, it was calculated that an effective sidewall thickness reduction of 2 µm (or a linear tapering of 4 µm on each side, Figure 5-9) on each side (4 µm total) resulted in agreement between the analytic, FEA, and experimental measurements for the force-displacement behavior in spring assemblies used in manually probed chips.

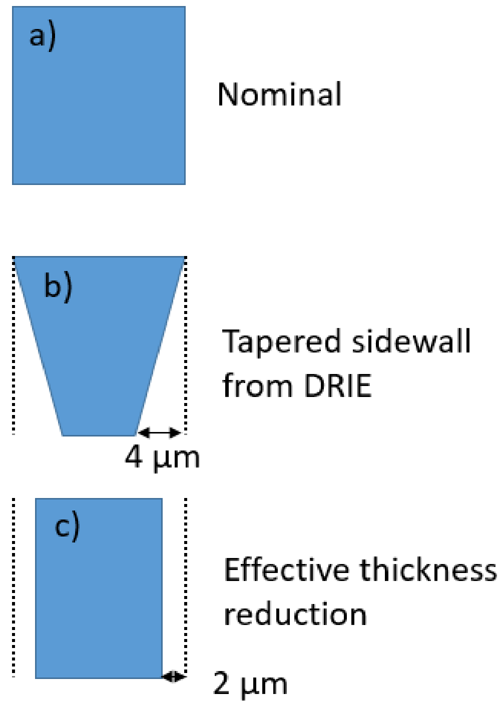


Figure 5-9 Schematics of sidewall cross-section showing a) nominal, b) tapered sidewall resulting from DRIE, and c) effective thickness reduction.

This 2 µm sidewall reduction is also applied to the spring constant calculations used in thermally actuated chips, and inertially loaded chips throughout this work for reasons stated above.

5.2 Force by thermal actuation

The purpose of testing chips using force applied by thermal actuation was to gather sufficient evidence that ECR between bare Silicon interfaces was a capable indicator of applied contact force. As there was no published data of ECR in contacting DRIE interfaces that the author could locate, the feasibility of an ECR-force sensor was initially unknown. Gathering initial data as straightforwardly as possible was the goal during initial measurements, and thermal actuation was a good fit.

5.2.1 Initial experimental evaluation

Initially, chips with line and area contact interfaces were force-cycled to determine whether ECR could be measured as a function of force, observe whether any system dynamics or constraints noticeably affected ECR-force behavior, and quantify the resistance range for a given force range. Analysis of initial experimental measurements revealed several important insights. Most importantly, ECR appeared to be variable and controllable with force. Shown below in Figure 5-10, absolute resistance between contact interfaces was between 200 – 2000 Ω at forces greater than 5 mN in line contacts, and asymptotically increased to infinity as contact was removed. In area contacts, absolute resistances were between 700 – 15000 Ω at forces greater than 5 mN, and ECR-force curves were more sensitive, erratic, and did not increase monotonically with decreasing applied force.

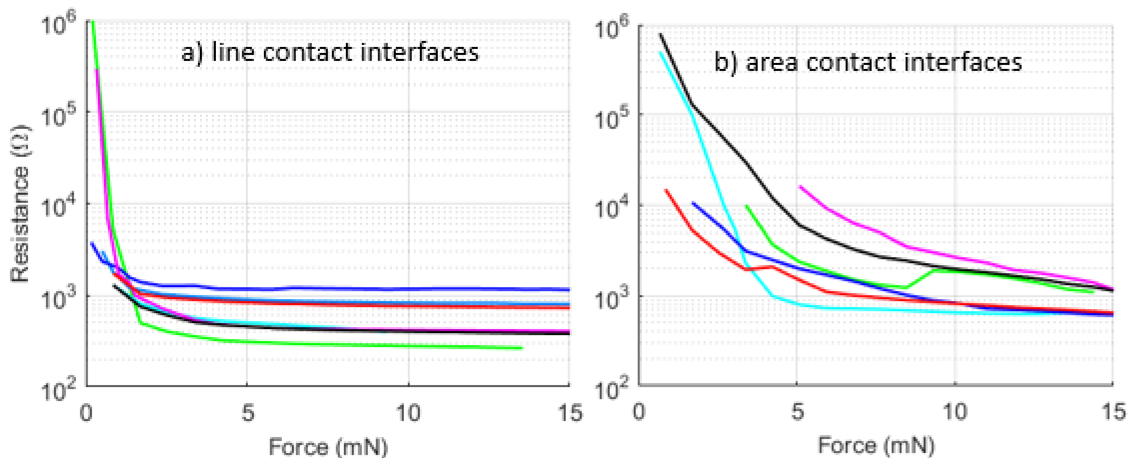


Figure 5-10. Initial experimental results showing absolute resistance versus force measured in separate chips from the same wafer. Force was applied by thermal actuation to a) line contact interfaces and b) area contact interfaces. Absolute resistance was shown to vary significantly chip-to-chip, and asymptotically increased as force decreased below approximately 3 mN in line contacts. Note that the applied force values were estimates based on initial force-power curves of

the defined thermal actuators, and likely shifted during operation near melting point (required for large throw distances), and as such are expected to be accurate within ± 2 mN (double that of other methods).

Absolute resistance varied significantly chip-to-chip, resistance behavior at low force (< 5 mN) was erratic and asymptotic, and ECR behavior in area contacts was frequently not monotonic. While sensitivity was very high at low forces, it was unpredictable. It was expected that maintaining a minimum force by applying a pre-load would be necessary for obtaining repeatable ECR-force measurements in future testing. For the remainder of force cycling using thermal actuation, a 5 mN load was maintained at the contact interface during loading of each chip to provide a margin of safety over the observed 3 mN asymptotic transition.

5.2.2 Initial force cycling data

More than 20 chips, each with line contacts of varying radius, were force cycled by thermally actuated spring compression. Many chips experienced stiction at some point during the force cycling process and greatly impeded the ability to obtain reliable and repeatable measurements. Stiction was likely due to charge build-up in a number structures on the chip acting as capacitors (native oxide, buried oxide, handle layer) during current application, amplified by the high-power nature (> 5 W) of thermal actuators. Stiction was temporarily overcome by using a pick, by hand, to manually separate surfaces, but typically this was for naught as stiction reoccurred shortly afterwards. To minimize the onset of stiction, chips were force cycled a maximum of 5 times during progressive force cycling tests. Unfortunately, most chips did not reach repeatable measurements in fewer than 10 cycles, and so the number of cycles needed to reach single-chip repeatability was not obtainable. However, a few valuable insights were gained to help guide testing by manual probe loading and inertial loading.

It was expected that resistance would decrease during force cycling (as in [16]) because smoothing of the surface during cycled abrasion allowed additional micro-asperity contacts to touch at the interface (this behavior occurs with manually loaded and inertially loaded chips). However, output from thermally actuated chips showed that cycle-to-cycle resistance typically increased with subsequent cycling, as shown below in Figure 5-11.

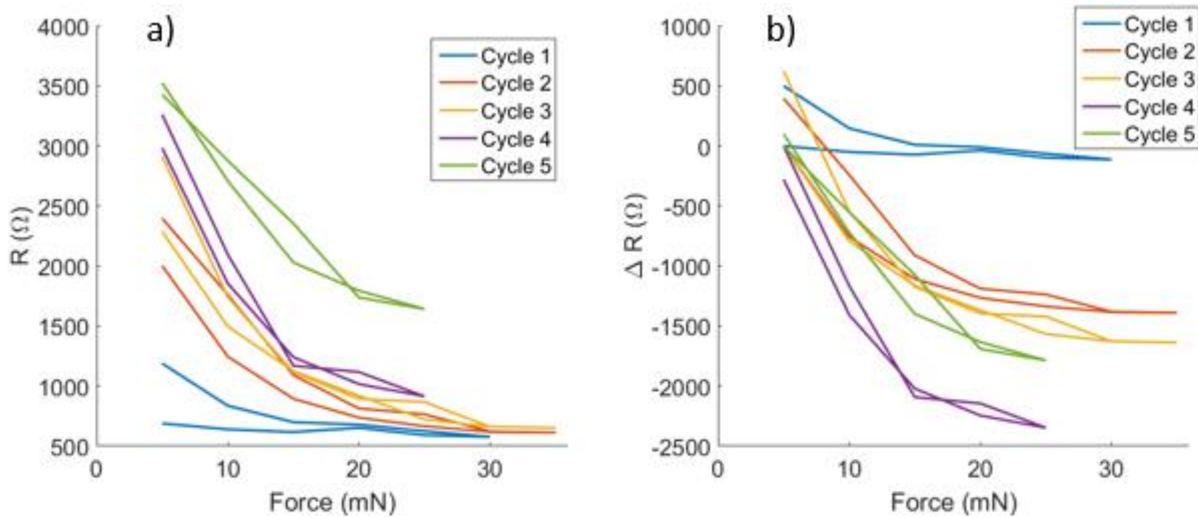


Figure 5-11. Reported change in a typical chip during force cycling applied by *in-situ* thermally actuated spring compression showing a) raw absolute ECR and b) absolute change in ECR versus applied force. Positive changes in resistance at 5 mN are a result of zero-shift upon return cycling, while multiple resistance values within a single chip depict hysteresis during reverse cycling. Note that applied force is expected to be accurate within ± 2 mN (double that of other methods).

In addition to absolute resistance, the absolute change in resistance was also examined. While not particularly elucidating for the datasets shown in Figure 5-11, resistance change was a more useful in future analyses because initial resistance varied significantly across all datasets.

Absolute resistance and absolute change in resistance, where force was applied by thermal actuator, is shown below in Figure 5-12 for all tested chips with line contacts.

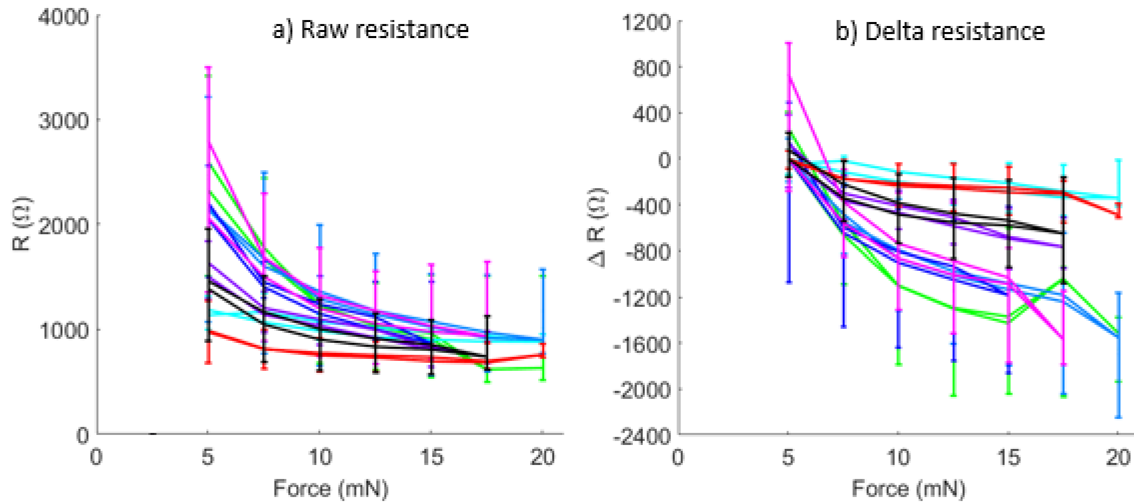


Figure 5-12. Reported change in a) raw absolute ECR and b) absolute change in ECR versus applied force by thermal actuator for tested chips with line contact interfaces, where each color corresponds to a separate chip. Cycles 1-5 of each chip were averaged and plotted, with error bars at each force level denoting standard deviation of each chip. Positive changes in resistance at 5 mN are a result of zero-shift upon return cycling, while multiple resistance values within a single chip depict hysteresis during reverse cycling. Note that applied force is expected to be accurate within ± 2 mN (double that of other methods).

Relative standard deviation (RSD), or the standard deviation divided by the mean, between thermally actuated chips was high, resulting from numerous shortcomings with this method. In addition to fabrication variance, wafer radial asymmetry, initial contact interfacing, and real pre-load variance, measurements were influenced by stiction-related issues, thermal actuator power-displacement variance, and thermal actuator performance creep. The impact of these factors was reduced by normalizing the resistance change by the initial contact resistance

measured for each device, with the resulting normalized ECR-force behavior presented in Figure **5-13**.

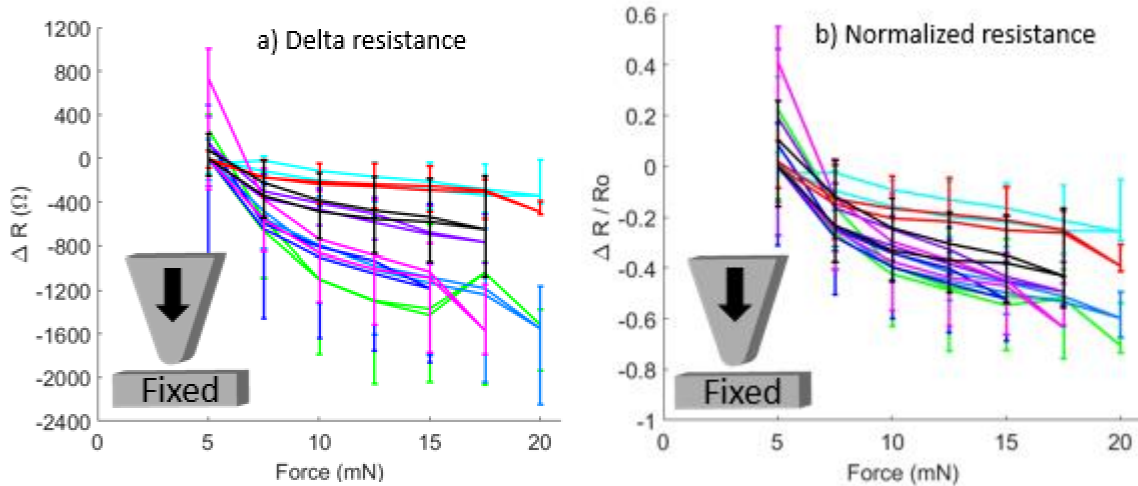


Figure 5-13. Reported change in a) absolute change in ECR and b) normalized change in ECR versus applied force by thermal actuator for tested chips with line contact interfaces. Cycles 1 - 5 of each chip were averaged and plotted, with error bars at each force level denoting standard deviation of each chip. Normalizing the resistance change by the initial resistance reduced RSD. Note that applied force is expected to be accurate within ± 2 mN (double that of other methods).

When normalizing the data, thermally actuated chips with line contact geometry were measured to have single-chip RSD of ± 43%, chip-to-chip RSD of ± 51%, and average hysteresis of 14%. Increasing resistance with increasing force cycling was theorized to be due to the non-linear and time-varying behavior of the thermal actuators near their melting point (necessary to achieve the needed throw of the actuator), which caused the force-power curves of the thermal actuators to reduce with subsequent power cycling, decreasing the applied force at the contacts. The angle of contact between the two interface sidewalls also may have changed if the thermal

actuator experienced asymmetric localized changes. Additionally, the mating of the interfaces may have caused repeated unintentional fracture, freeing small-scale debris and allowing it to become lodged between contact surfaces (although this did not occur with the other loading methods). Charge build-up within the various complex structures during motion, and limited displacement of the thermal actuators made it difficult to accurately gather data with meaningful resolution. Most importantly, however, the onset of stiction prior to the number of cycles needed for repeatability prevented single-chip repeatability. It was deemed that thermal actuators are likely a poor option for repeatedly applying force and measuring a corresponding contact resistance.

5.3 Force by manual spring elongation

The purpose of testing chips using force applied by manual elongation of embedded springs was to gain a quantified understanding of the effects of varying contact geometry on ECR-force behavior, determine relative performance characteristics of tested interfaces, and investigate which microsystem design elements were critical for consistent ECR-force performance. Applying force through manual spring elongation allowed fine control of testing dynamics, improved force accuracy and resolution, simple integration of lateral constraints, and eliminated using high power, which reduced the occurrence of stiction. Additionally, probe-induced manual spring elongation allowed unpackaged testing of chips, visual inspection during static and quasi-static loading, and refinements of the characterization process prior to inertial loading.

An external probe displaced *in-situ* spring assemblies until contact interfaces touched, with further probe movement elongating the spring assembly to define the applied cyclical load. Over 100 chips with line, area, and multi-line contact geometries were tested. The fabricated final iteration of the manually actuated chips is shown below in Figure 5-14.

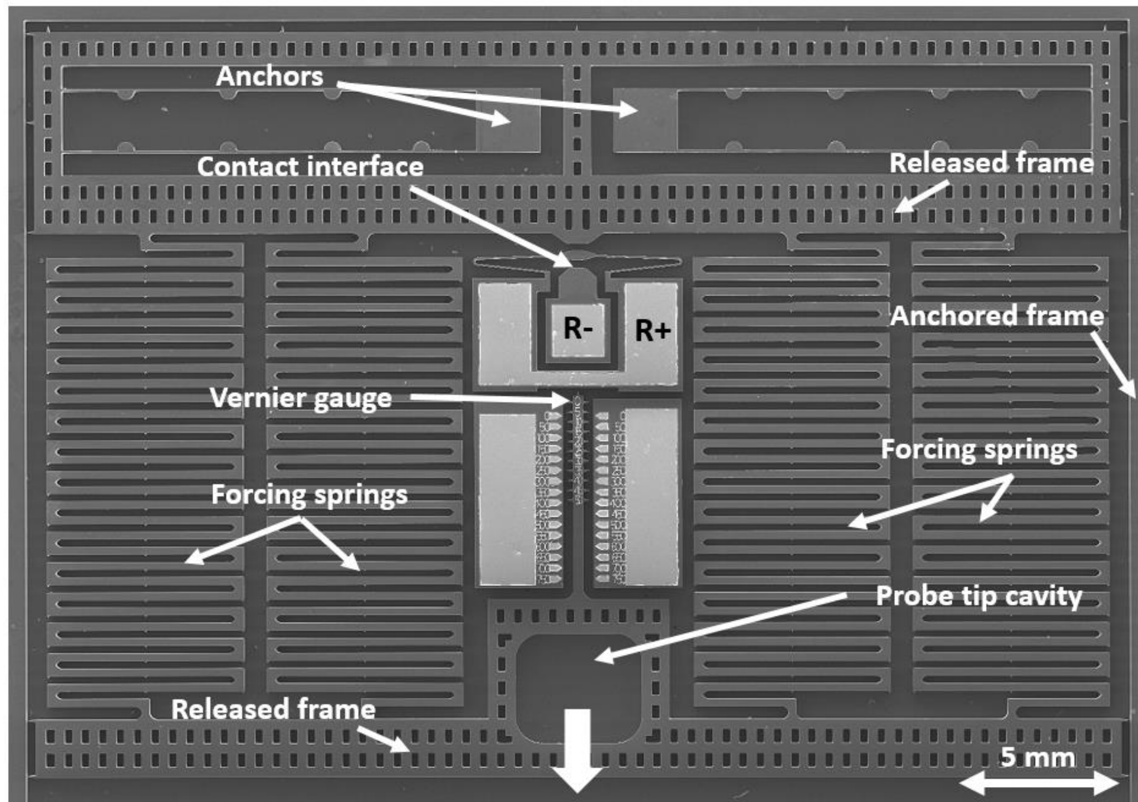


Figure 5-14. SEM of a chip using manually probed spring elongation to apply force. A probe tip is placed within the probe tip cavity and pulled downwards to apply force to the contact interface in the top half of the chip. Contact resistance is measured across R+ and R-. This method offers improved force resolution over thermal actuation because overall spring stiffness is much less. Note that the released structure is held in place by the anchors and anchored frame.

5.3.1 Interface mating and pre-load

Testing with force applied by thermal actuation indicated that a pre-load of at least 3 mN was needed to maintain consistent contact during force cycling, and 5 mN was used as the minimum applied load to add a margin of safety. To understand why this was the case, contact interfaces were analyzed in microsystems where force was applied by manual spring elongation,

which allowed gluing displaced springs in place following elongation to fix the applied force. Following applying glue to the displaced microsystem, chips were analyzed using SEM.

SEM imaging showed curved, rather than linearly sloping, surface topology of DRIE sidewall contacts. Wafers were fabricated in a multi-user cleanroom facility and variance was expected, although change to the overall surface shape, rather than to sidewall angle and undercut, was unexpected. To analyze how curved sidewalls mated during contact, several manually-probed chips were glued in place at differing force levels (Figure 5-15).

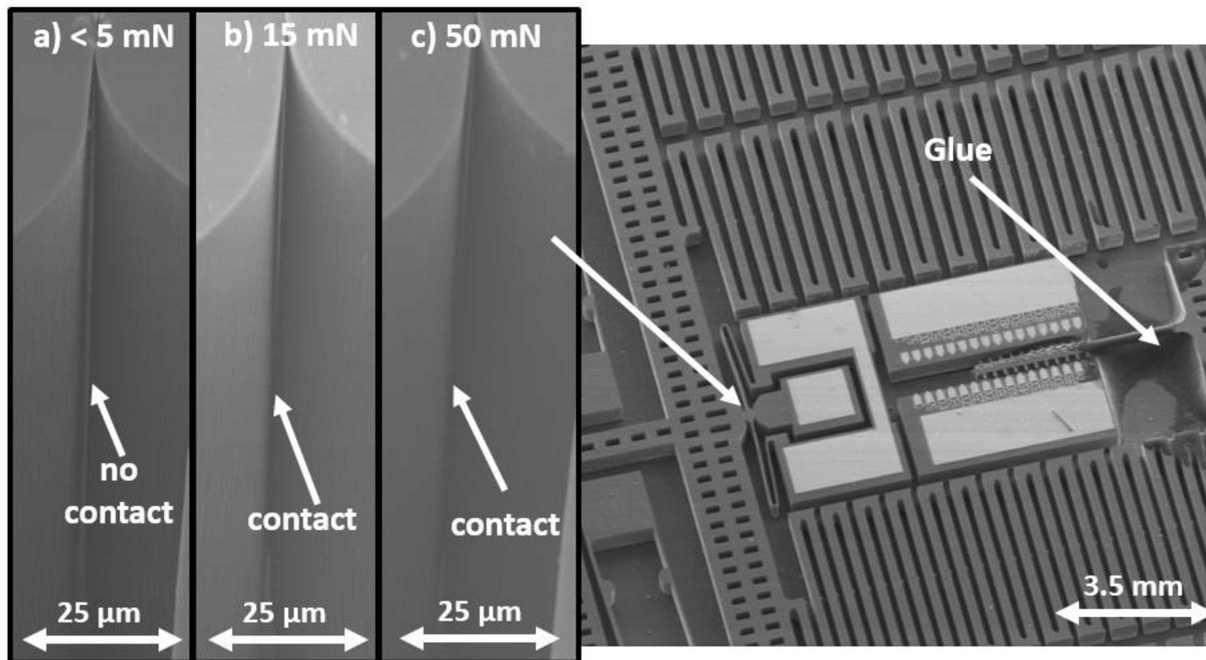


Figure 5-15. SEM images showing contacting interfaces with slight sidewall curvature at (a) < 5 mN, (b) 15mN and (c) 50 mN. Initial contact occurs at top surface, and appears constant after 15 mN. SEM on the right shows one of the chips with a glued forcing mechanism to maintain constant force for analysis.

At initial contact (< 5 mN), interfaces touched at the top surface. At 5 mN and beyond, contact occurred centrally along sidewalls, and appeared consistent up to 50 mN. SEMs showed that full sidewall contact had not yet occurred when applied force was less than 5 mN. Variance

of the 5 mN pre-load in manually-probed chips may have caused sidewall separation during loading where pre-load was less than intended, leading to small impact events. It was presumed that some chips tested by manual spring elongation may require slightly more than 5 mN to maintain macro-scale contact between interfaces. However, pre-load was defined at 5 mN to gather data at as low a force as possible. In the accelerated inertial testing that follows, pre-load was defined at a more conservative 25 mN to ensure macro-scale interface contact in all tested chips. By extension, future SOI-DRIE ECR-force sensors should maintain a pre-load that causes full sidewall contact through force cycling to prevent sidewall separation and minimize impact events, fracture, and wear.

5.3.2 Break-in

Chips were pre-loaded to 5 mN, followed by cycling from 5 mN to 25 mN. ECR measurements during initial force cycling using manual spring elongation revealed that "break-in" occurred in all tested chips, wherein ECR measurements trended towards a final ECR-force curve becoming repeatable, typically after 10 cycles for line contacts and 20 cycles for area contacts (Figure 5-16).

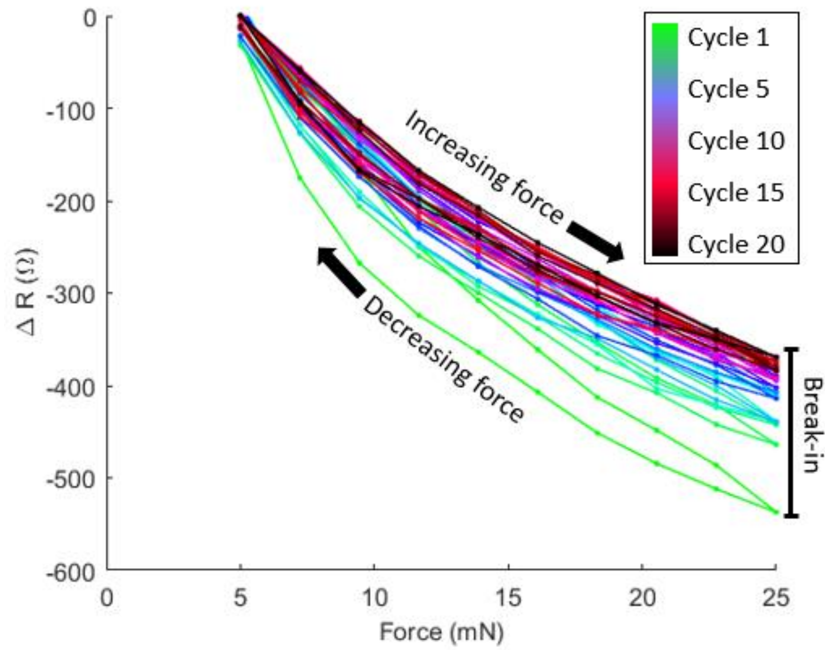


Figure 5-16. Typical ECR-force behavior for DRIE line and area contact interfaces showing "break-in" after about 10 and 20 cycles, respectively. Note that applied force is expected to be accurate within ± 1 mN.

SEM imaging revealed accumulating abrasion at the top surface of contact interfaces during "break-in," indicating localized fracture at the top edges of the upper surfaces (Figure 5-17).

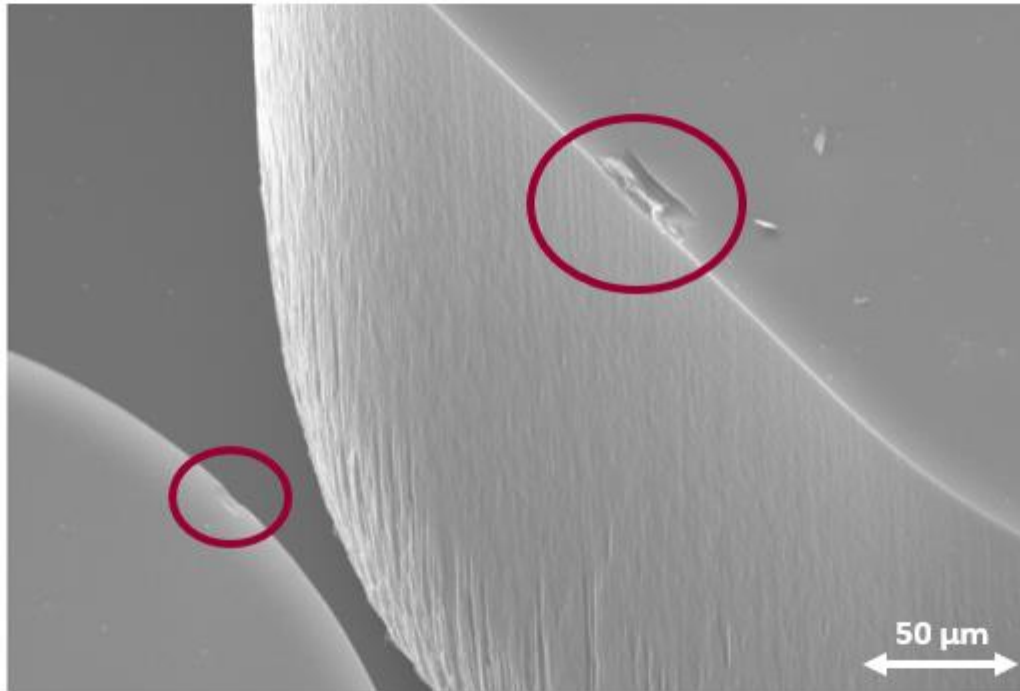


Figure 5-17. SEM image showing abrasion at the top contact surfaces after about ten fully reversed force cycles (5 - 25 mN). Similar abrasion occurs after only a few cycles in contacts with small radii, and is not apparent in contacts with very large radii ($r > 100$ µm).

5.3.1 Initial performance quantification

At least 4 chips of each geometry and dimension were tested, with the resulting average ECR-force behavior shown below (Figure 5-18).

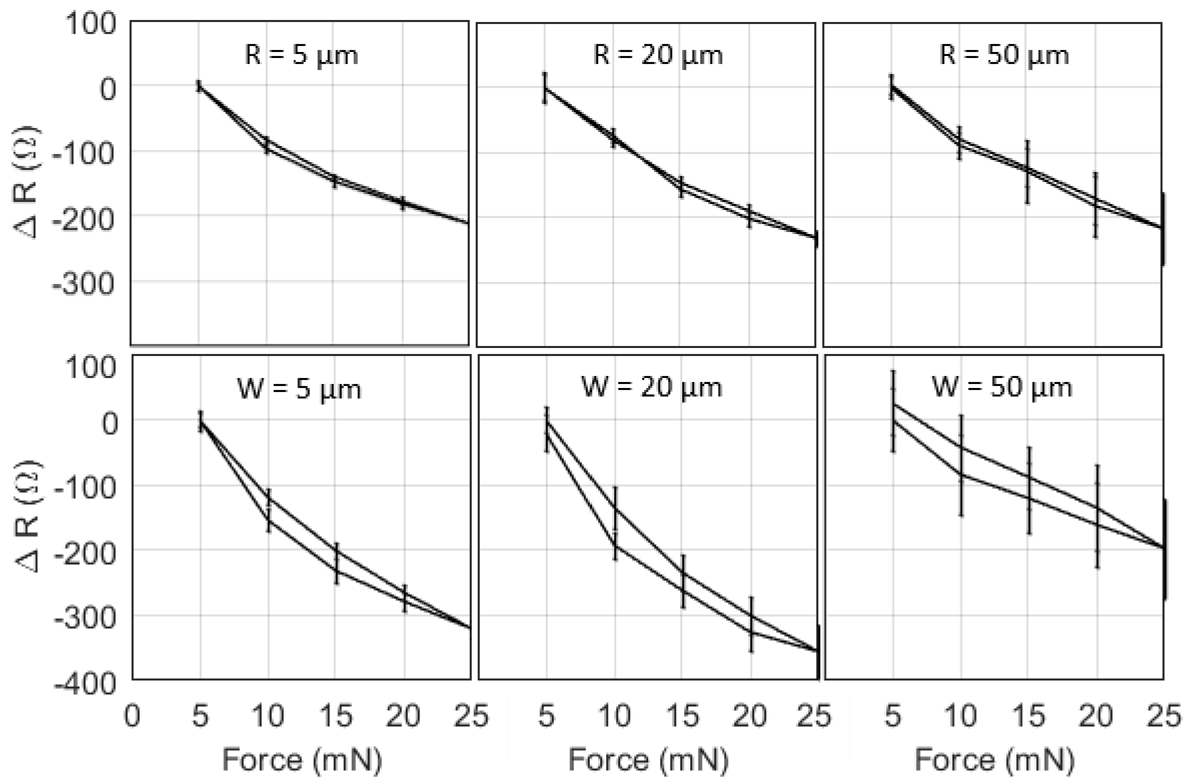


Figure 5-18. Reported change in ECR versus applied force for tested chips with (a) line contacts showing a change in ECR of approximately 200 Ω from 5 to 25 mN for each contact radius, while tested chips with (b) area contacts show a change in ECR of 320 Ω, 350 Ω, and 200 Ω for 5 µm, 20 µm, and 50µm contacts, respectively. Cycles 15 – 20 of each chip were averaged and plotted, with error bars at each force level denoting corresponding average single-chip standard deviation within each group. Positive changes in resistance at 5 mN are a result of zero-shift upon return cycling, while multiple resistance values depict hysteresis. Note that applied force is expected to be accurate within ± 1 mN.

Fabrication variance, wafer radial asymmetry, initial contact interfacing, real pre-load variance and loading orientation reduced chip-to-chip repeatability. The impact of these factors can be reduced by normalizing the resistance change by the initial contact resistance (Figure 5-19).

Note that this effect is more pronounced for datasets where force was applied by accelerated inertial mass.

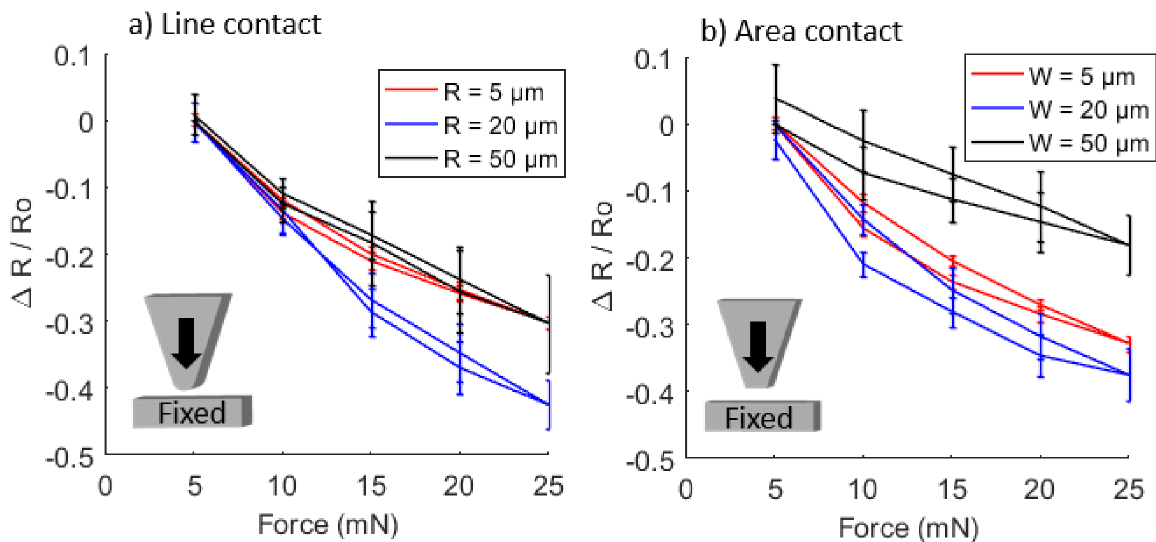


Figure 5-19. Relative change in ECR versus applied force for manually tested chips with (a) line contacts and (b) area contacts of varying characteristic dimension (radius and width, respectively). Cycles 15 - 20 of chips within each characteristic dimension group were averaged and plotted, with error bars at each force level denoting corresponding average standard deviation within each group. Average sensitivity shown for each set of chips with corresponding characteristic dimension size. Positive changes in resistance at 5 mN are a result of zero-shift upon return cycling, while differing resistance values during increasing and decreasing force depict hysteresis. Contact interface shape shown in bottom-left corner. Note that applied force is expected to be accurate within ± 1 mN.

As expected, chips with line contacts of the smallest radius subjected to inertial loading exhibited the best single-chip and chip-to-chip repeatability, and least hysteresis and zero-shift. Chips with 5 μm contact radius showed 1.6 % single-chip RSD, 24.0 % chip-to-chip RSD, 2.1 % hysteresis, and sensitivity of 2.0 %/mN. Increasing radius size most notably increased hysteresis.

Hysteresis was observed in most chips, evidenced by differing behavior during increasing and decreasing force, and may have been caused by temporary surface adhesion or asymmetric mechanical behavior of the serpentine spring. Zero-shift was observed in most chips, indicated by differing starting and ending ECR values within a force cycle. Imaging revealed residue (likely residual passivation polymer from DRIE undercut, Figure 5-20) beneath released structures that appeared to snag the assembly occasionally during motion, resulting in a shifting point of contact and partial restoration of the spring assemblies.

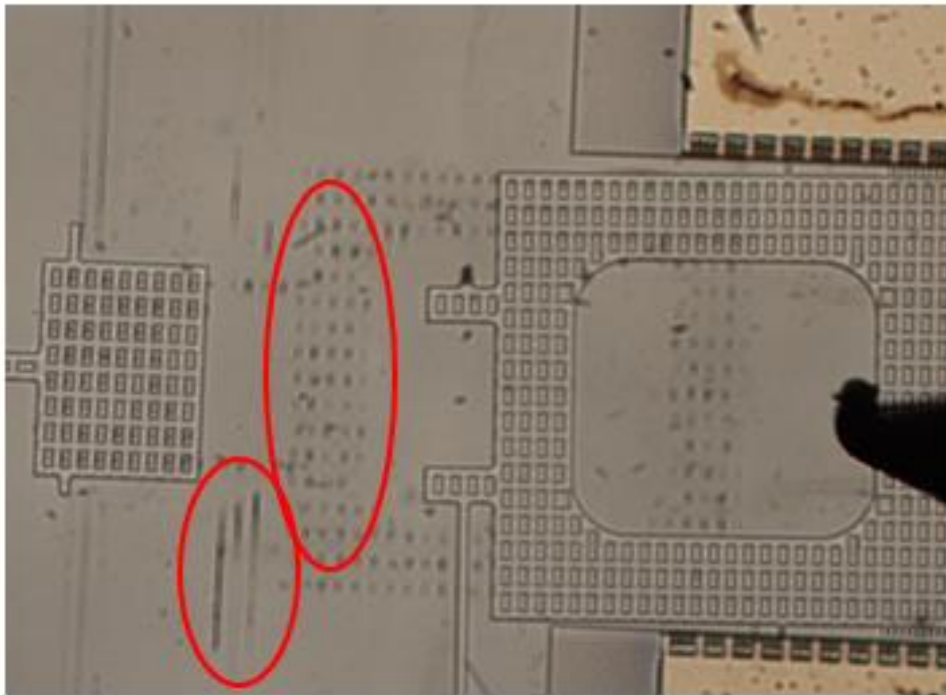
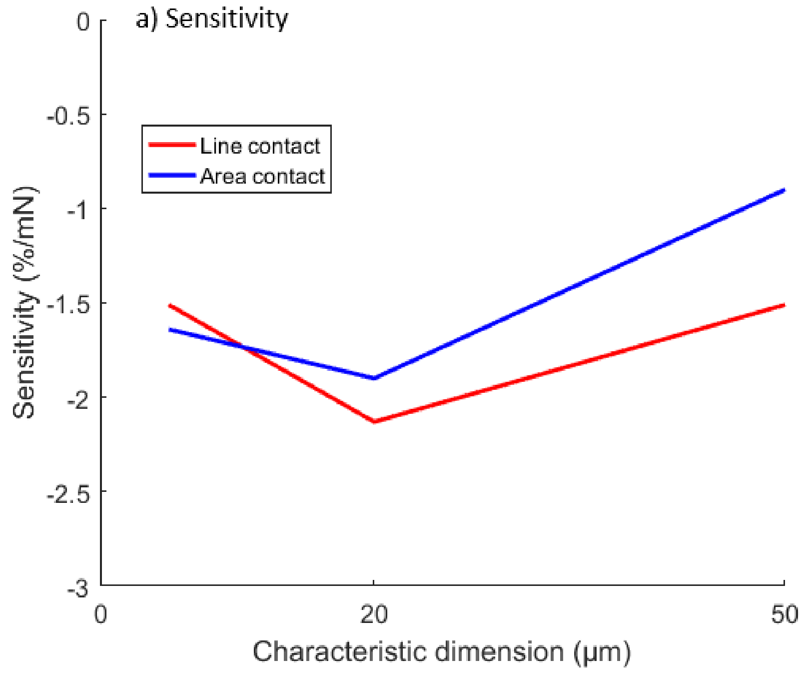
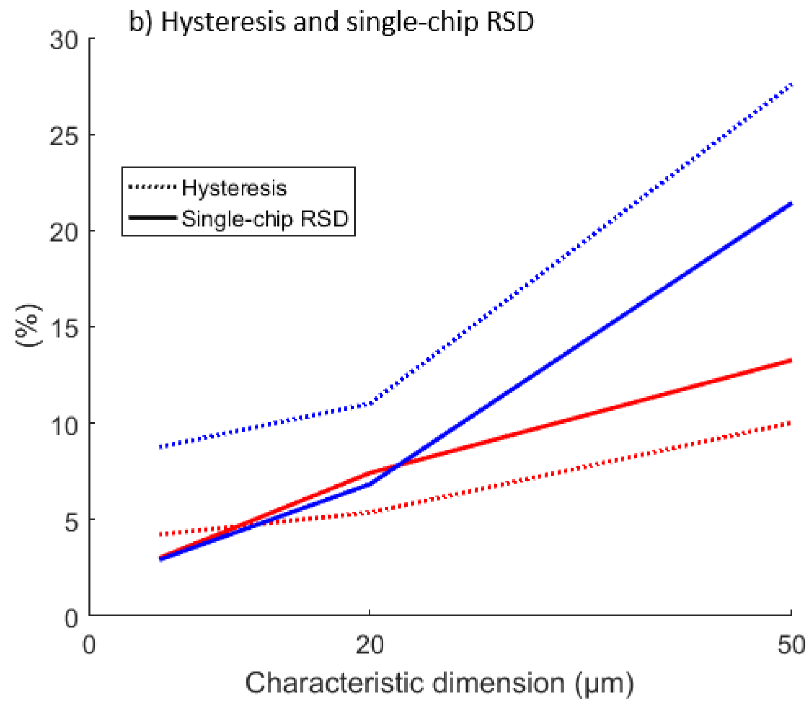


Figure 5-20. Optical image highlighting (in red) the underlying DRIE residue, which likely contributed to zero-shift and hysteresis during force cycling.

Performance of tested chips with line and area contacts was compared (Figure 5-21) to determine best candidates for inertial loading, which was expected to yield more repeatable and reliable results.


a) Sensitivity
Line contact
Area contact
Sensitivity (%/mN)
0
-0.5
-1
-1.5
-2
-2.5
-3
0
20
50
Characteristic dimension (μm)


b) Hysteresis and single-chip RSD
Hysteresis
Single-chip RSD
(%)
30
25
20
15
10
5
0
0
20
50
Characteristic dimension (μm)

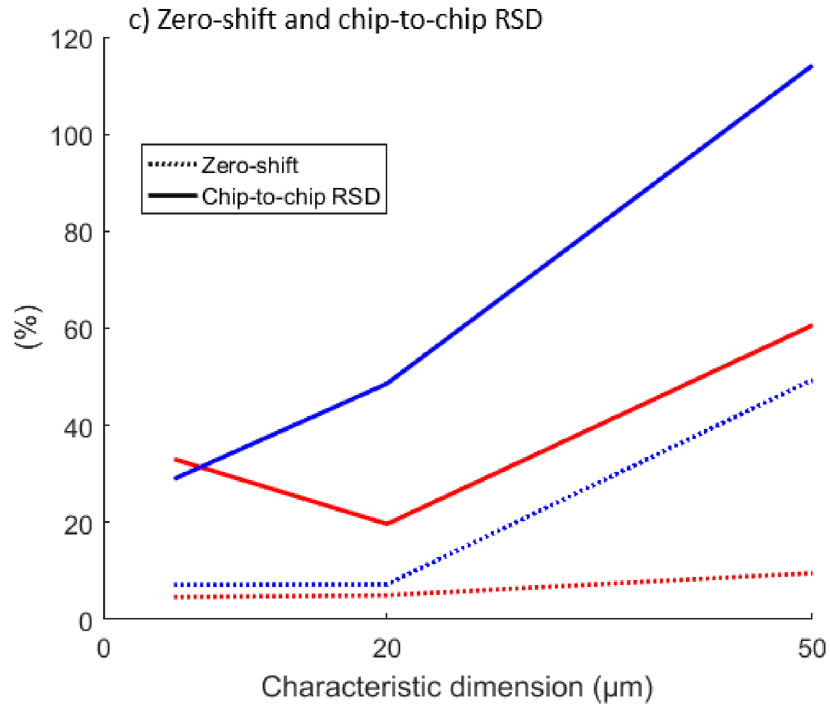


Figure 5-21. Average (a) sensitivity, (b) hysteresis and single-chip relative standard deviation (RSD), and (c) zero-shift and chip-to-chip RSD for experimentally tested chips by manual loading by spring elongation with varying characteristic dimensions (radius and width, respectively).

Normalized data shows increasing hysteresis and zero-shift with increasing contact area, where the smallest radius line contacts and widest area contacts had minimum and maximum hysteresis and zero-shift, respectively. Sensitivity between all geometries was similar. A similar trend occurred with single-chip repeatability, although chip-to-chip repeatability was less predictable. As a result, contact interface geometries with line contacts of a small radius were chosen for inertial loading.

Probe-induced manual spring elongation revealed valuable insights for inertial testing. Rotation and sliding at the contact interface significantly increased ECR variance, removal of contact or failure to maintain pre-load produced discontinuous ECR-force curves, unintentional

spring assembly recoil during motion caused noticeable surface fracture at the contact point, and irregular spring assembly movement occurred during improper alignment or rough motion of the probe. Robust lateral constraints, a consistent contact point, and minimum pre-load were critical to reliable measurement. Manual loading by probe revealed relative performance characteristics between contact geometries without the need for wire bonding or chip packaging, however, irregularities resulting from manual operation during loading, and uncertainty in spring constants of fabricated devices necessitated an automated loading mechanism to obtain acceptable ECR-force relationships in DRIE SOI-MEMS. To this end, the use of inertial loading was explored as an enhanced experimental method.

5.4 Force by accelerated inertial mass

The primary purpose of inertial loading was to investigate the ability to obtain a reliable and repeatable ECR-force measurement across a SOI-DRIE contact interface. While the use of manually probed chips allowed for ECR testing without the need for wire bonding or chip packaging, issues of experimental repeatability, limited force resolution, and cumbersome manual actuation necessitated an alternate method for ECR-force characterization. In addition to providing an independent measurement method, inertial loading allowed automated testing while reducing the potential influence of mechanical misalignment on ECR measurements that occurred during manual actuation. Furthermore, the inertial loading mechanism serves as a simplified test case for use of ECR transduction in acceleration sensing.

Inertially-loaded chips were accelerated to 100 g in increments of 16 g ($F = mr\omega^2$), corresponding to a maximum applied force of 10 mN (not including the 25.3 mN pre-load). An SEM of a fabricated chip is shown below (Figure 5-22).

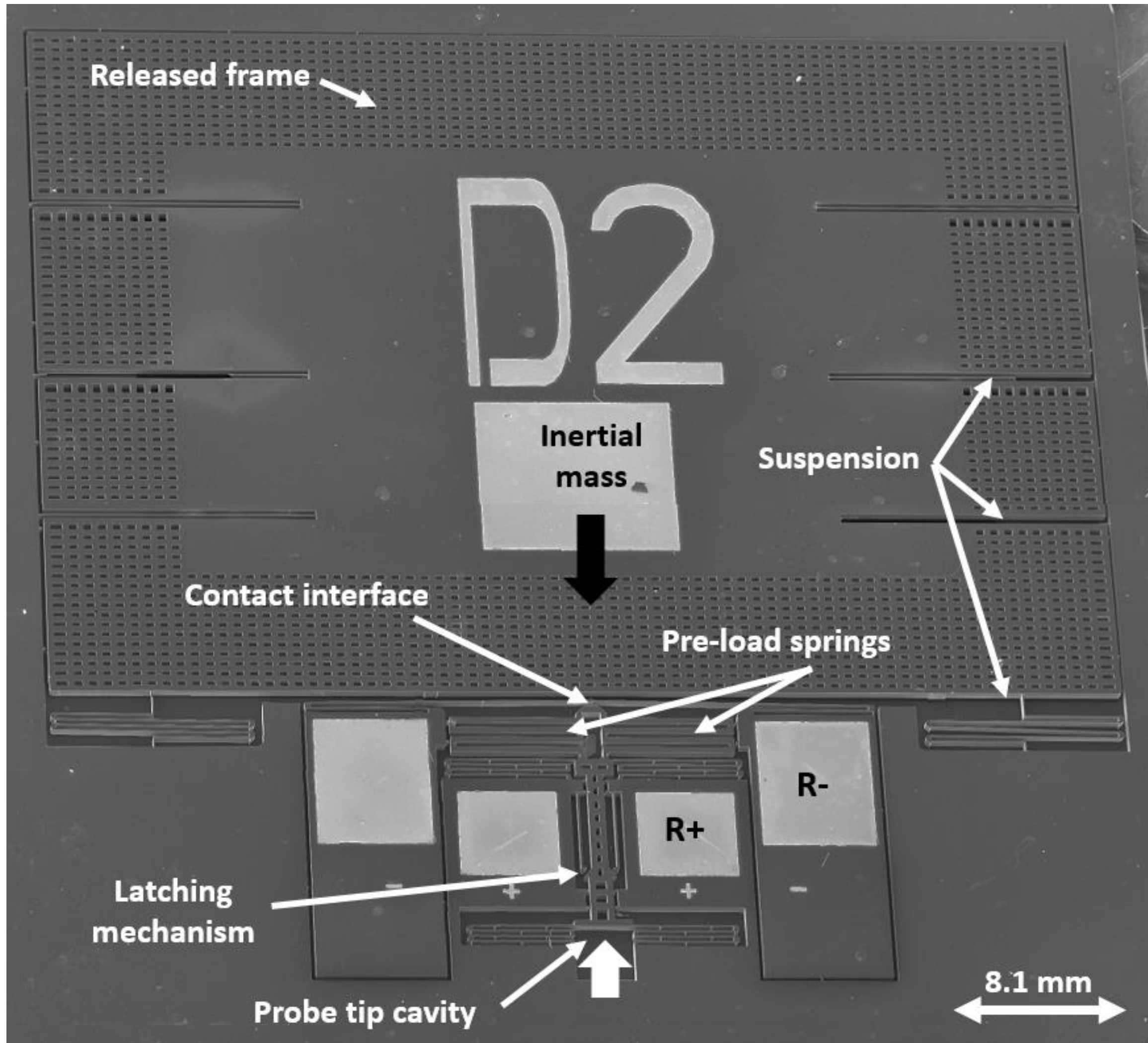


Figure 5-22. SEM of a chip using manually probed spring elongation to apply force. A probe tip is placed within the probe tip cavity and moved downwards to apply force to the contact interface in the top half of the chip. Contact resistance is measured across R+ and R-. Note that the released structure is held in place by the anchors and anchored frame.

Line contacts of the smallest radius were expected to yield the best results, as indicated by manual loading. To verify this, chips with line contact geometries of varying radius were packaged and tested, with resulting absolute ECR-force curves below in Figure 5-23.

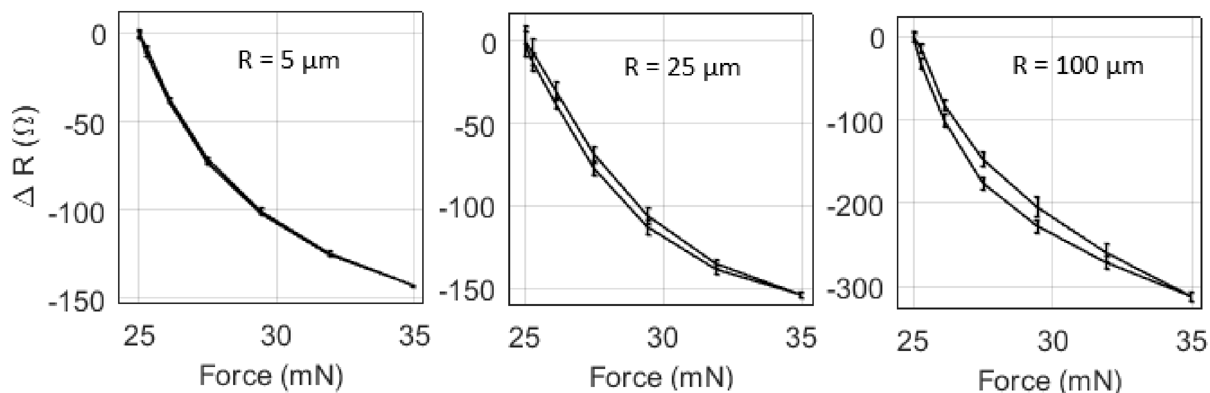


Figure 5-23. Absolute change in ECR versus applied force for inertially actuated chips with line contacts of varying radius. Average sensitivity shown for each set of chips with corresponding contact radius, with line contacts of 100 µm radius showing the highest sensitivity. Cycles 80 - 100 of chips within each characteristic dimension group were averaged and plotted, with error bars at each force level denoting average single-chip standard deviation within each group. Repeatable measurements to within 5% were reached in < 5 cycles (as opposed to > 10 cycles with manually probed chips) for single chips. Inertially actuated chips with line contacts of 5 µm radius exhibited the lowest relative standard deviation (RSD = 1.6%) and hysteresis (2.1%). Note that applied force is expected to be accurate within ± 1 mN.

5.4.1 Comparison between contact geometries

From the data presented above in Figure 5-23, which depicts the absolute change in resistance as a function of applied force within inertially actuated chips, output varied by about 150 Ω for line contacts with a radius of 5 µm and 25 µm, and 300 Ω for line contacts with a radius of 100 µm over the applied force range from 25 mN to 35 mN. Repeatable measurements to within 5 % were reached in < 5 cycles (as opposed to > 10 cycles with manually probed chips) in single chips. A variety of factors contributed to chip-to-chip variance, including fabrication variance,

wafer radial asymmetry, initial contact interfacing, real pre-load variance and inertial mass orientation. The impact of these factors can again be reduced by normalizing the resistance change by the initial contact resistance measured for each device, with the resulting normalized ECR-force behavior for chips force cycled by accelerated inertial mass presented in Figure 5-24.

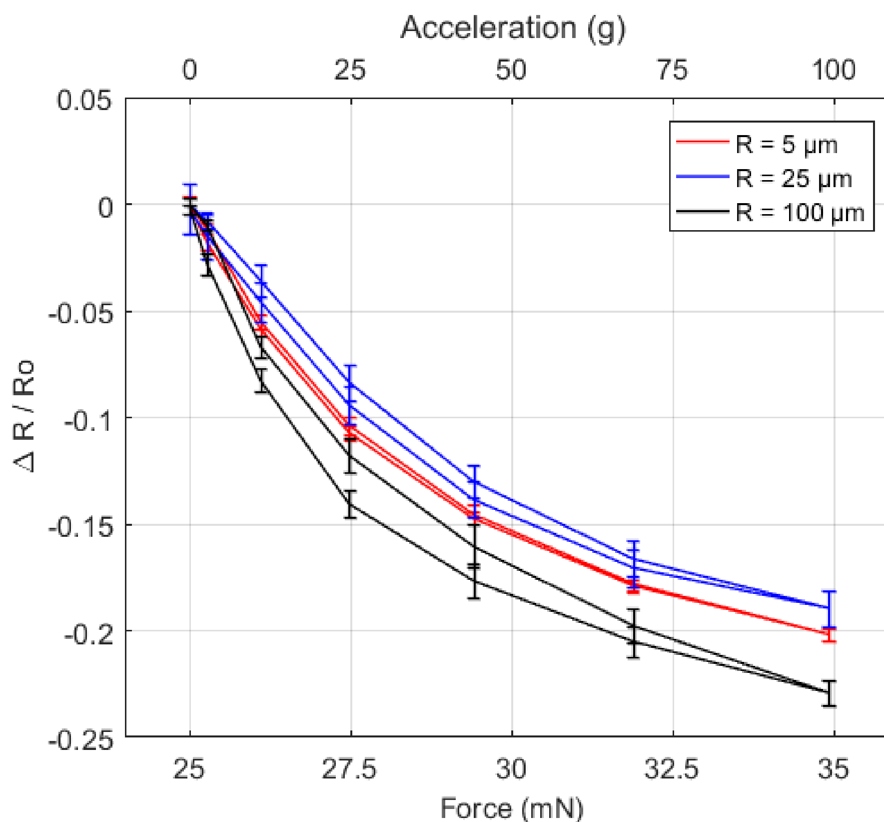
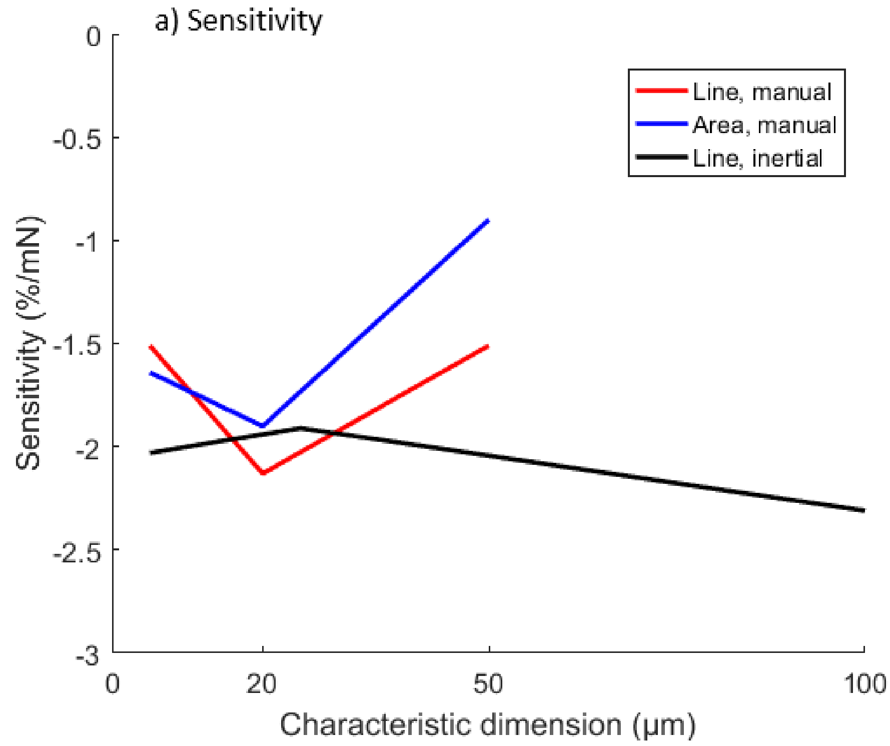
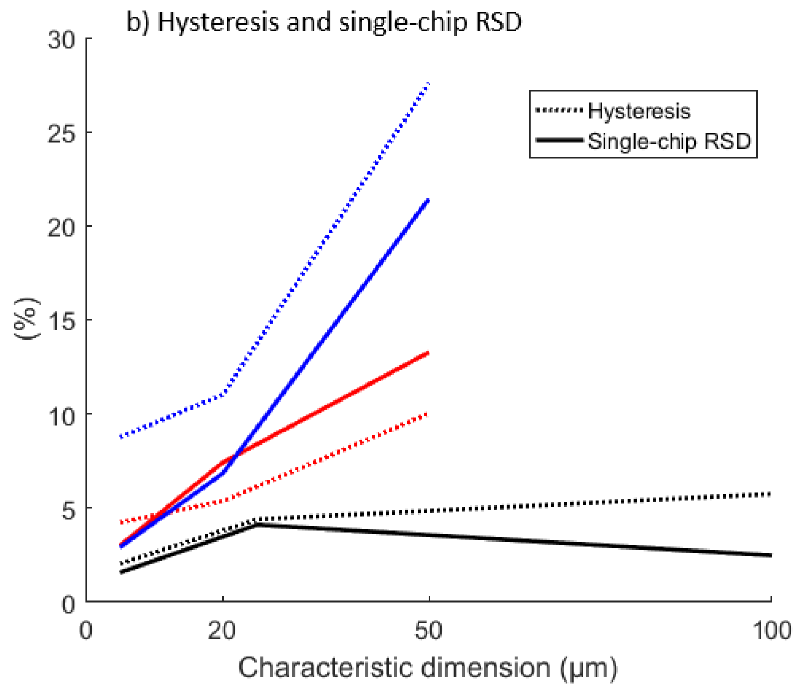


Figure 5-24. Relative change in ECR versus applied force for inertially actuated chips with line contacts of varying radius. Cycles 80 - 100 of chips within each characteristic dimension group were averaged and plotted, with error bars at each force level denoting average single-chip standard deviation within each group. Average sensitivity shown for each set of chips with corresponding contact radius. Repeatable measurements to within 5% were reached in < 5 cycles (as opposed to > 10 cycles with manually probed chips) for single chips. Inertially actuated chips with line contacts of 5 μm radius exhibited the lowest relative standard deviation (RSD = 1.6%). Note that applied force is expected to be accurate within ± 1 mN.

As expected, chips with line contacts of the smallest radius subjected to inertial loading exhibited the best single-chip and chip-to-chip repeatability, and least hysteresis and zero-shift. Chips with 5 μm contact radius showed 1.6% single-chip RSD, 24% chip-to-chip RSD, 2.1% hysteresis, 1.3% zero-shift, and sensitivity of 2.0 %/mN. Increasing radius size most notably

increased hysteresis. Results were also compared with manual probe and inertial loading of all contact geometries (Figure 5-25).





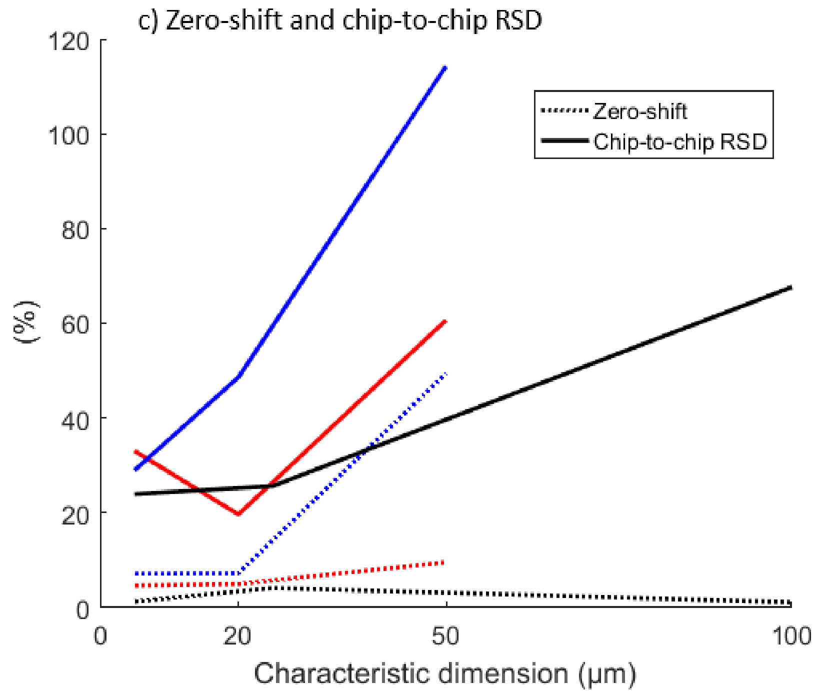


Figure 5-25. Average (a) sensitivity, (b) hysteresis and single-chip relative standard deviation (RSD), and (c) zero-shift and chip-to-chip RSD for experimentally tested chips by accelerated inertial mass with varying characteristic dimensions (radius and width, respectively).

Differences between chips of varying contact size were not as prominent in inertially tested chips compared to manually tested chips, however, contacts interfaces with smaller dimensions remained best performers. Single-chip repeatability, chip-to-chip repeatability, and hysteresis all worsened with increasing contact radius, while zero-shift and sensitivity were largely uncorrelated. ECR-force sensitivity of all chips was between 1 - 2 %/mN, and varied most in area contacts likely due to sliding at the contact interface.

While there was not a significant difference in the average outputs of chips with differing contact geometries, useful information was gained. Single-chip repeatability became worse as line contact radius increased. Normalized output of manually actuated chips with line contacts of 5 µm radius that were force cycled from 5mN to 25 mN showed single-chip repeatability of 3%,

chip-to-chip repeatability of 32%, and average hysteresis of 5%. An overall comparison is given below in Table 5-2.

Table 5-2. Performance comparison as a function of contact goemetry and size.

Method	Contact shape	Contact size	Single-chip RSD	Chip-to-chip RSD	Hysteresis	Sensitivity	# chips
Manual spring elongation	area	5 µm	2.90%	29.00%	8.80%	-1.6 %/mN	6
		20 µm	6.90%	48.60%	11.00%	-1.9%/mN	10
		50 µm	21.40%	114.20%	17.60%	-0.9%/mN	8
	line	5 µm	3.00%	33.10%	4.20%	-1.5%/mN	8
		20 µm	7.40%	19.70%	5.40%	2.1%/mN	8
		50 µm	13.30%	60.70%	10.00%	-1.5%/mN	8
Inertially accelerated proof mass	line	5 µm	1.60%	24.00%	2.10%	-2.0%/mN	8
		25 µm	4.10%	25.70%	4.40%	-1.9%/mN	4
		100 µm	2.50%	67.70%	5.80%	-2.3%/mN	5

5.4.2 Comparison with modeling

Experimental results from inertial chips was compared to the previous ECR-Hertzian models to determine the effect of varying device thickness (Figure 2-15) and topology (Figure **2-8**). To utilize the model, the path resistance between wire bond locations of an inertial chip was first measured. Probe-to-probe resistance was found to be approximately 1 Ω on average, and path resistance from wire bond locations was measured to be approximately 500 Ω. Modeled output with 500 Ω path resistance and line contact length of 50 µm was compared to experimental results for chips subjected to accelerated inertial loading (Figure 5-26).

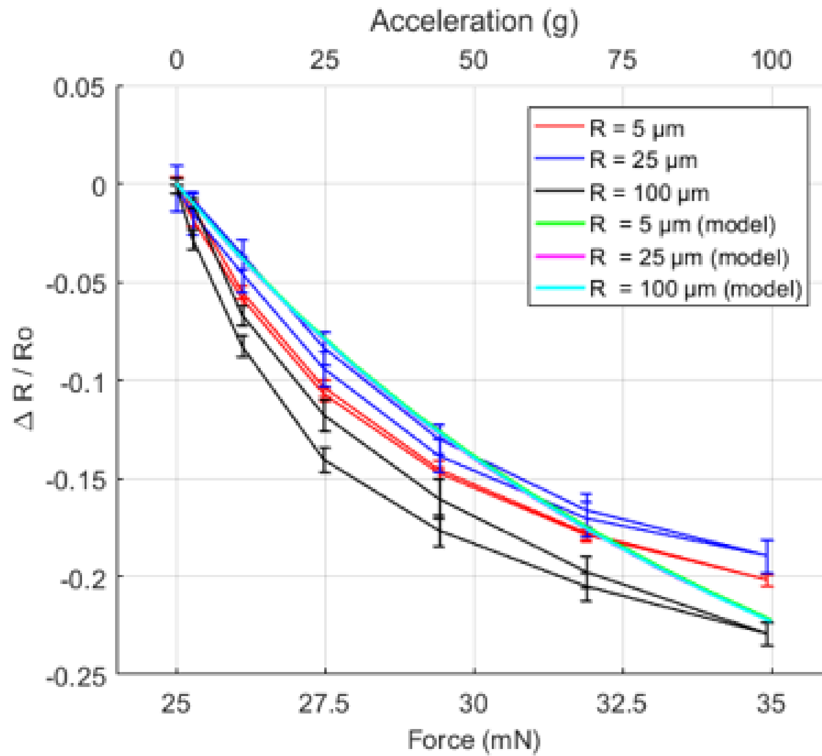


Figure 5-26. Experimental versus model output for the ECR-force relationship for line contact length = 50 μm, fractal dimension D = 2.3, RMS roughness R_q = 0.2 μm, and path resistance = 500 Ω (note earlier modeling did not include path resistance). Again, cycles 80 - 100 of chips within each characteristic dimension group were averaged and plotted, with error bars at each force level denoting average single-chip standard deviation within each group. Note that modeled ECR-force curves are indistinguishable because modeling predicts very similar normalized sensitivity with varying contact radius (Figure 2-15).

Using the Hertzian and ECR models developed prior, the rate of change of ECR as it varies with force should decrease with increasing contact radius. While line contacts with 50 μm radii had the least sensitivity, contacts with radii of 5 μm and 20 μm had similar sensitivities, likely due to variations of surface topology impacting the real contact area.

5.4.3 Packaging

Packaging and centrifuge testing of inertial chips was somewhat difficult and a few problems were encountered. While the compression of the pre-load spring assembly was photolithographically defined, the system was latched manually using a pick by hand, which resulted in varying levels of impact at the contact interface during pre-loading that produced varying contact surface topologies. Proof masses were large, and it was necessary to attach an overhanging glass shim to prevent movement during handling and operation. Since there was not enough open surface area on the chip to place droplets of glue, a shim was glued adjacent to the chip to extend the foundation (Figure 5-27).

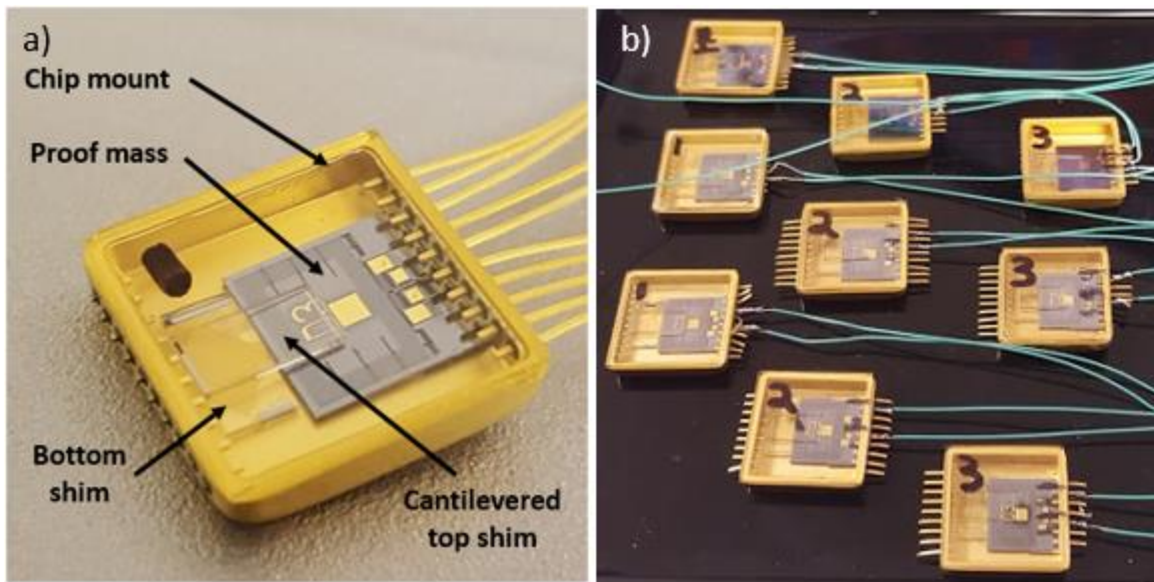


Figure 5-27. Images of a) packaged chip showing location of shims and proof mass and b) an array of tested packaged chips.

Cap chips were glued to the adjacent shim and cantilevered over the inertial chip. However, inspection revealed the shims were not parallel to proof masses after attachment, which allowed slight movement and rotation that altered the real pre-load at the contact interface. Further

microsystem development and corrected packaging techniques are expected to improve future reliability and repeatability.

While transient and dynamic response was deemed outside the scope of this work, several inertial chips were instrumented and slammed against a table top several times to see response time curves. Resistance output appeared to track exactly with the input shock, showing less than 30 μs response time, including the rise time of the shock pulse. A full characterization of the ECR-relationship in dynamic environments may elucidate its potential in the high-g space, and reveal promising design techniques for implementing such a sensor.

Chapter 6: Discussion

6.1 Discussion of results

Several factors affected the ECR-force performance of tested chips. Differences in resistance during force application were subject to influence from initial and varying contact mating orientation (all three axes), sidewall topology variance, fabrication residue, manual actuation error, and pre-load error. Closer inspection of interface geometries revealed important considerations.

6.1.1 Contact interface alignment

Several contact mating issues occurred during testing. In manually probed chips, the angle between the probe tip and inner mass sidewall during pulling often caused the back-side contact interface (electrically isolated) to pivot the adjacent contact interfaces (under test) in relation to each other, depending on whether the probe tip pulled the mass upwards out-of-plane or downwards into the handle layer during motion. The resulting behavior usually occurred consistently per-chip, but differed chip-to-chip due to slight changes in the mounted chip position relative to the probe, as well as the z-axis location of the probe tip on the inner mass sidewall. Since pivoting of the contact surface directly affected the real contact area during ECR measurement, sensitivity variance arising from slight differences in real surface area at a given force occurred within the set of tested chips. It was difficult to avoid this, though further improvement of the measurement microsystem may help reduce error.

In inertially loaded chips, the manual nature of engaging the pre-load mechanism (Figure 6-1) introduced a different set of variables.

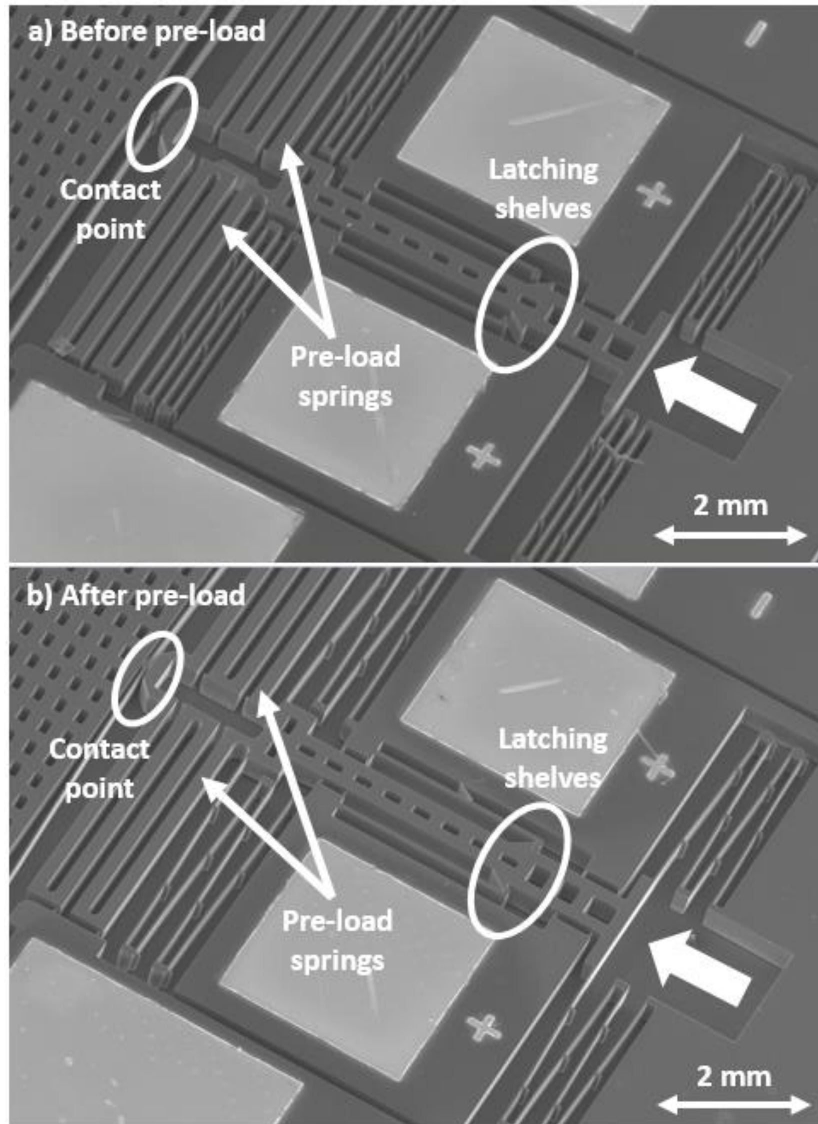


Figure 6-1. SEMs of the latching mechanism in inertially-loaded chips a) prior to pre-load and b) after pre-load. The central yoke was pressed upwards manually using a hand tool under a microscope.

The pre-load mechanism was manually engaged using a hand tool to displace the bottom yoke upwards until latching shelves overlapped. To ensure the latch was fully engaged, the yoke was displaced fully until the contact interfaces, mass, and springs were completely compressed and in contact. The force required to overcome the latch was difficult to precisely apply manually,

and as a result, contact surfaces experienced an impulse load of varying magnitude from chip-to-chip. The resulting contact surface fracture (particularly along the top surface) also varied from chip-to-chip. Additionally, the impulse load into the system from engaging the pre-load occasionally caused the mass to move slightly upwards out-of-plane. In some cases, visible residue appeared on the upper contact surfaces after pre-load and prior to any cycling (Figure 6-2).

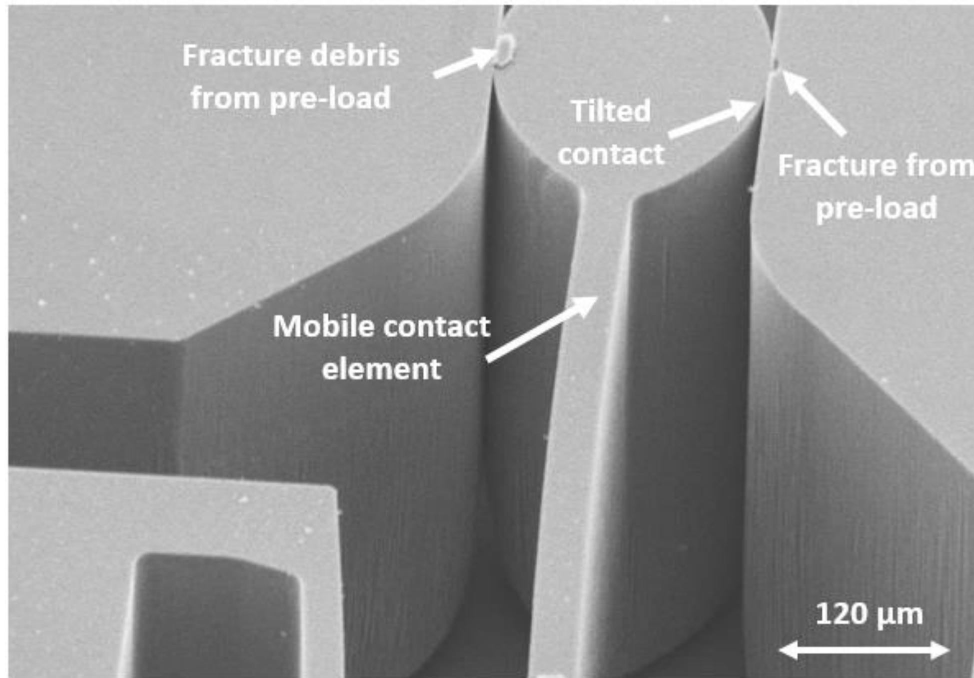


Figure 6-2. SEM image showing mated contact interfaces of an inertially loaded chip. Commonly occurring surface fracture is shown after initial pre-load, but prior to force cycling. The anchored right-side contact wall is raised above the mobile center contact element, indicating that the contact has tilted or slid downwards toward the handle layer. Both phenomena were common, and varied chip-to-chip.

Variance of the initial sidewall fracture was expected to cause both a change in initial contact resistance and an overall sensitivity change, as ECR varies with the change in real contact area, which depends on the contacting topology.

6.1.2 Fracture and wear

Fracture occurred at contact interfaces in most chips and was a particular problem in early testing. Chips where force was applied by thermal actuation typically did not see more than 5 force cycles, making fracture and wear difficult to assess. In early testing of chips force cycled by spring elongation, impact at contact interfaces occurred when underlying debris got caught in the spring assembly and caused a rebound effect. The resulting impact caused surface fracture and movement of the contact point each time, resulting in ECR-force curves varying by up to two orders of magnitude. The effect of repeated impact events on line contacts with narrow radii (2 µm) is shown below in Figure 6-3.

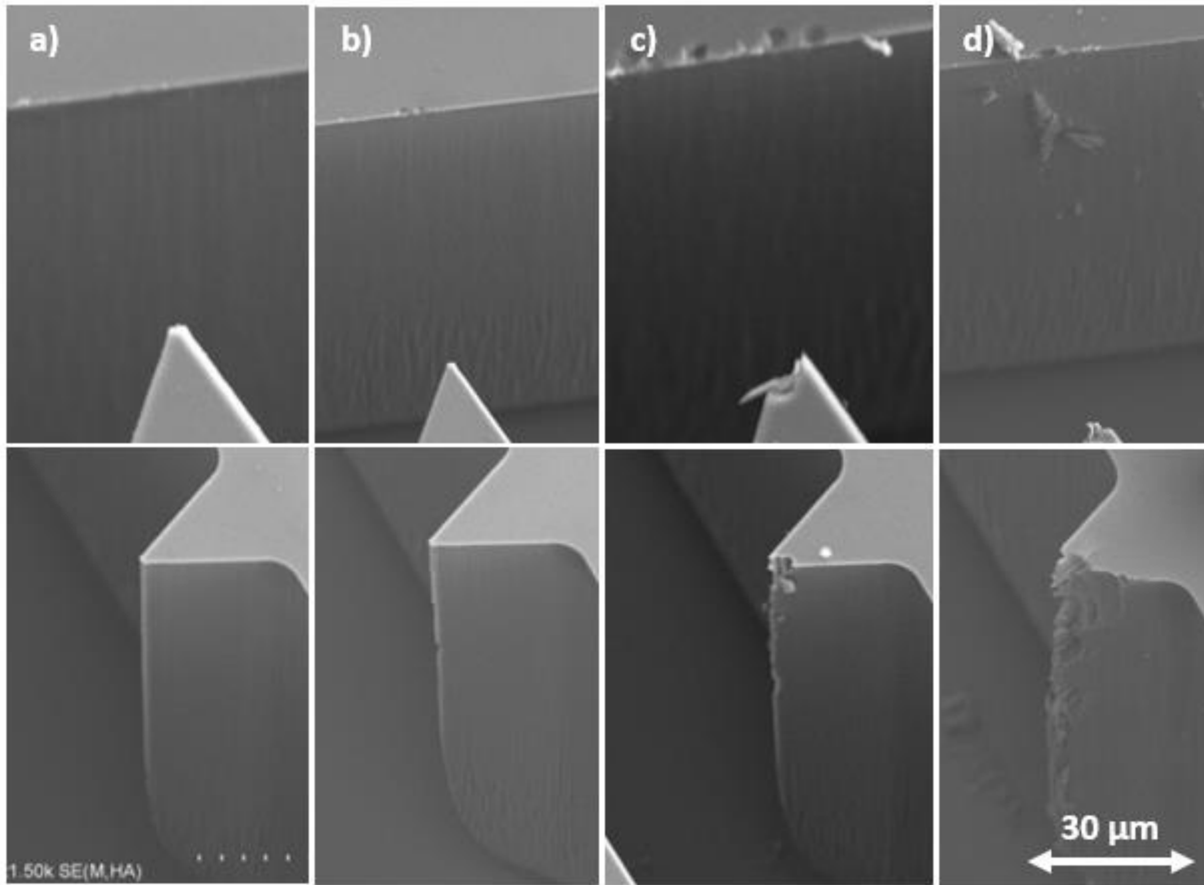


Figure 6-3. SEMs of contact sidewall fracturing, pictured from left to right with increasing cyclical impact loading from 0 to 25 mN. Early testing results showing released contact (bottom) and anchored contact target (top) for impact loading of separate chips with a) 5 cycles with smooth initial contact, b) 20 cycles with smooth initial contact and a snag during movement, c) 20 harsh cycles with repeated initial contact and d) 50 harsh cycles with intentional impact loading. Note that contact was completely removed between each cycle, and the contact radius was 2 µm (lithography limit).

To reduce fracture in subsequent testing of chips with force applied by manual spring elongation, a pre-load was maintained throughout force cycling to minimize impact events at the contact interface, and the minimum line contact radius was increased from the lower lithography

limit (~2 µm) to 5 µm (which was the minimum radius used in all subsequent testing). Adding consistent pre-load and increasing contact radius substantially reduced fracture on sidewalls, however, fracture was still observed at top surface edges. Figure 6-4 below shows sidewalls of two chips that have been force cycled ~ 50 times (5 – 25 mN) under constant pre-load.

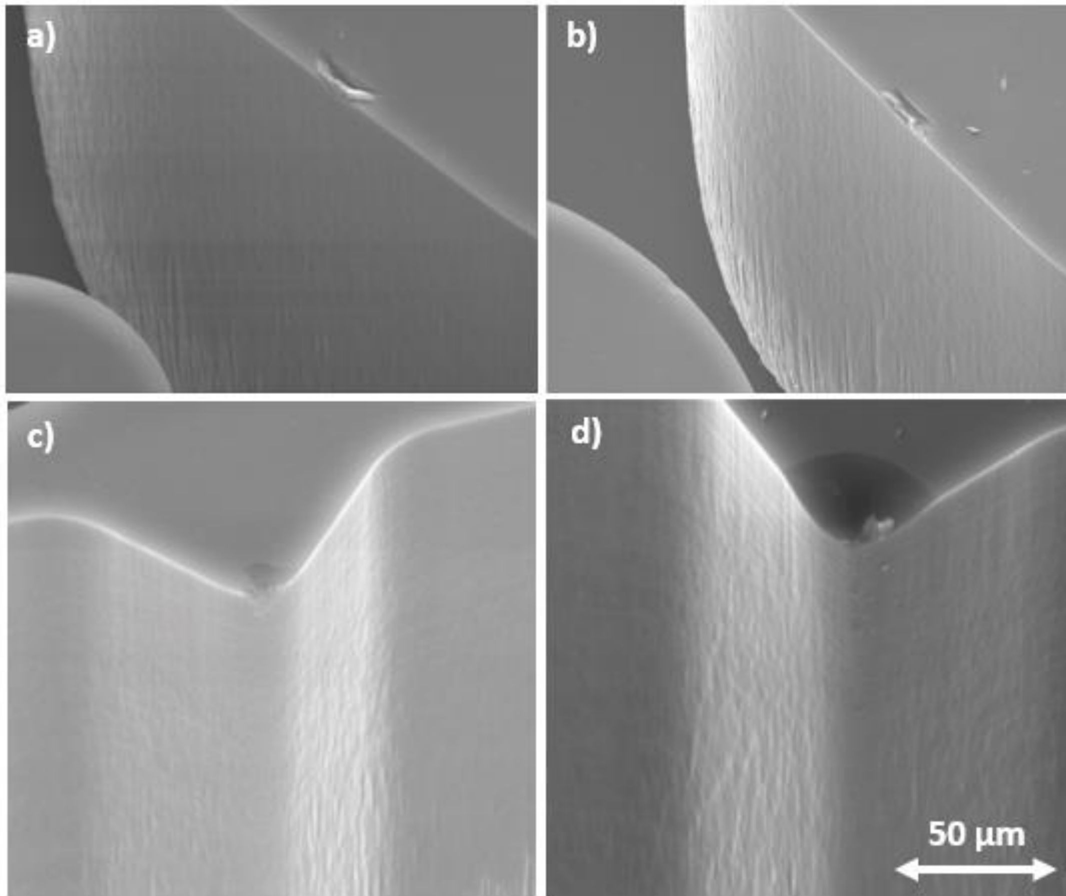


Figure 6-4. SEMs showing surface fracture at the a, b) fixed contact sidewalls and c, b) free contact sidewalls of four manually probed chips force cycled approximately 50 times from 5 mN to 25 mN with contact radius of 5 µm. Fracture occurred along the top edge and top area of the sidewall.

In interfaces of manually loaded chips under constant pre-load that did not experience impacts, sidewall fracture was not as prominent, and decreased with increasing contact radius.

SEM images of contact sidewalls with varying contact radii subjected to approximately 50 force cycles from 5 - 25 mN by manual spring elongation show fracture on the upper sidewall is pronounced with radii less than 20 µm, minimal with radii of 20 µm and 50 µm, and not apparent in radii greater than 50 µm (Figure 6-5).

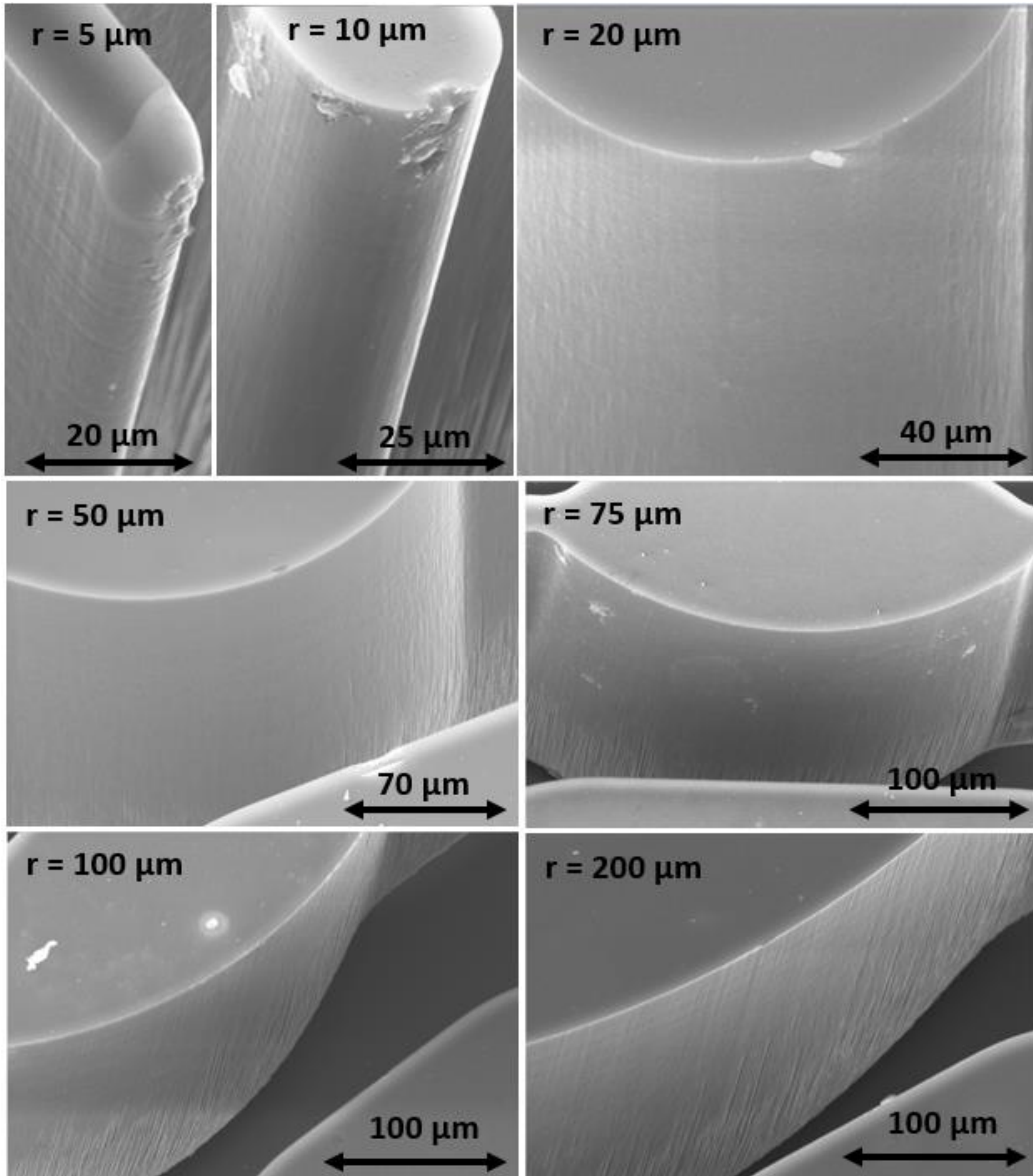


Figure 6-5. SEM images of contact sidewalls with varying contact radii after approximately 50 force cycles from 5 - 25 mN. Fracture on upper sidewalls is pronounced in radii less than 20 µm, minimal in radii of 20 µm and 50 µm, and not apparent in radii greater than 50 µm.

SEM imaging of inertially loaded chips that were force cycled over 100 times from 25 mN to 35 mN show similar fracture patterns (Figure 6-6).

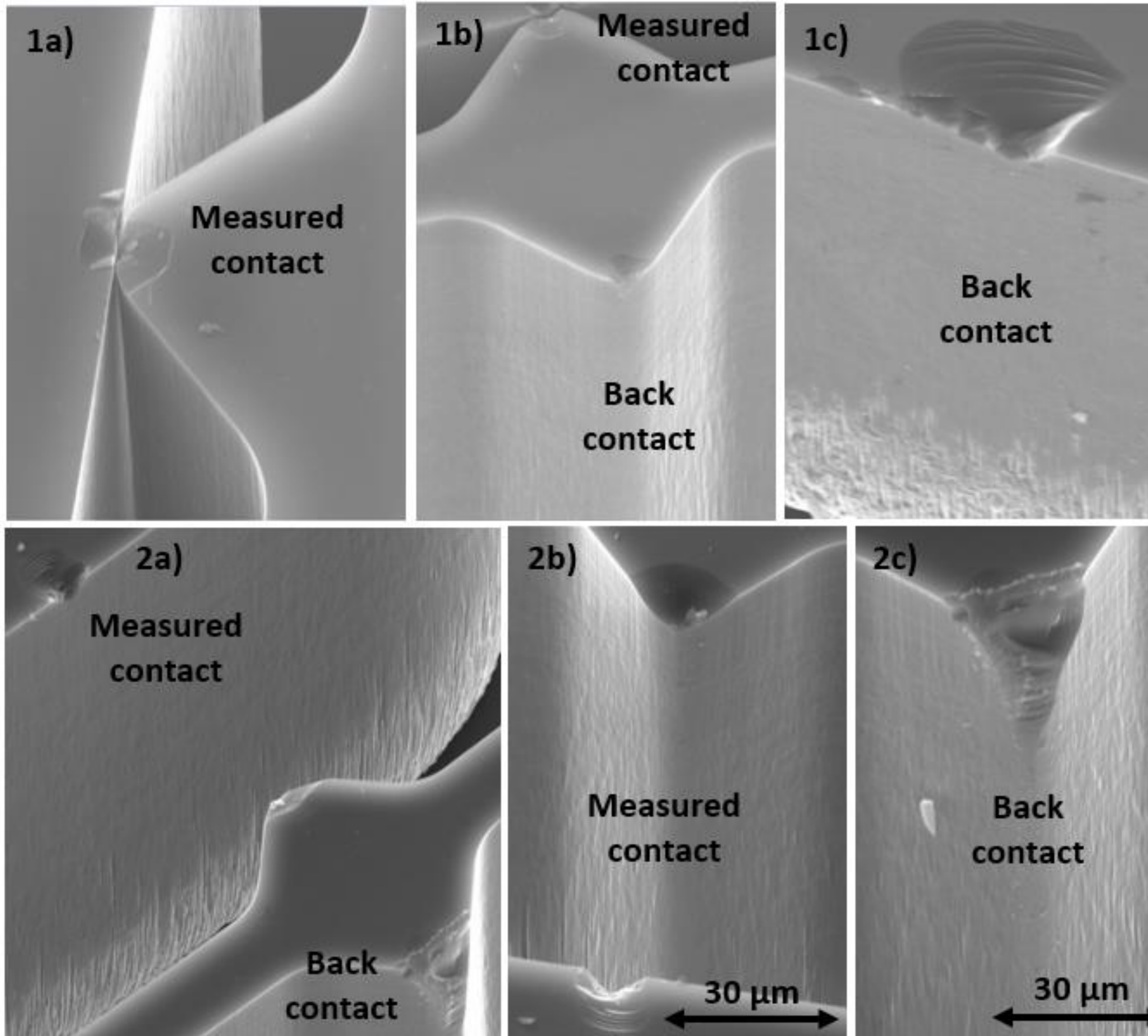


Figure 6-6. SEMs of two unpackaged inertially loaded chips after approximately 100 force cycles from 25 mN to 35 mN. Chip 1 above showing a) surface fracture in the measured interface, b) back-side of the free contact and c) sidewall of the proof mass interface that mated with the back-side free contact. Chip 2 below showing a) fracture at the measured interface (now unlatched) and back-side of the free contact, b) front view of the front free contact sidewall and c) back-side free contact, which mates with the proof mass and is not electrically measured.

Sidewall fracture was revealed in all examined inertial chips. The measured front contact sidewalls show similar wear and fracture to tested manually-probed chips, while the proof mass and back-side contact sidewalls consistently showed comparably more fracture. This was likely a result of the latching dynamics that propagated through the system. During latching, contact is first made at the measured interface, at which point the symmetric latching cantilevers press against the central yoke. Once the yoke is sufficiently displaced, contact is subsequently made between the back-side of the contact interface and the adjacent proof mass wall. Very little tolerance was allowed (~1 µm) to achieve this and thus, the impulse from latches snapping back into place likely caused an impact load at the mass-contact interface.

6.1.3 Hertzian fracture modeling

To better understand why fracture occurred in line contacts with radii less than 20 µm and not radii greater than 50 µm, applied contact pressure is compared to the fracture strength of monocrystalline Silicon. On a macroscale, the interaction between line DRIE interfaces is best approximated using a Hertzian contact model for a cylindrical surface and a flat plane surface in contact under a force. The maximum Hertzian contact pressure, p_{max}, can be calculated using the contact half-width, b, the applied contact force, F, and the line contact length, l, by

$$p_{max} = \frac{2F}{\pi b l}, \qquad (6\text{-}1)$$

with

$$b = \sqrt{\frac{2F}{\pi l} \frac{\frac{(1-\nu_1^2)}{E_1} + \frac{(1-\nu_2^2)}{E_2}}{\frac{1}{d_1} + \frac{1}{d_2}}}, \qquad (6\text{-}2)$$

where subscripts 1 and 2 both refer to Silicon, d is the contact diameter, E is the Young's modulus, and ν is Poisson's ratio.

As contact does not occur over the entire line contact length due to sidewall curvature (Figure 5-15), the actual line contact length lies somewhere between 0 - 100 μm (the thickness of the chip). To determine the real line contact length, contact pressure is plotted over the range of prescribed contact radii for prospective line contact lengths between 15 μm and 100 μm (Figure **6-7**).

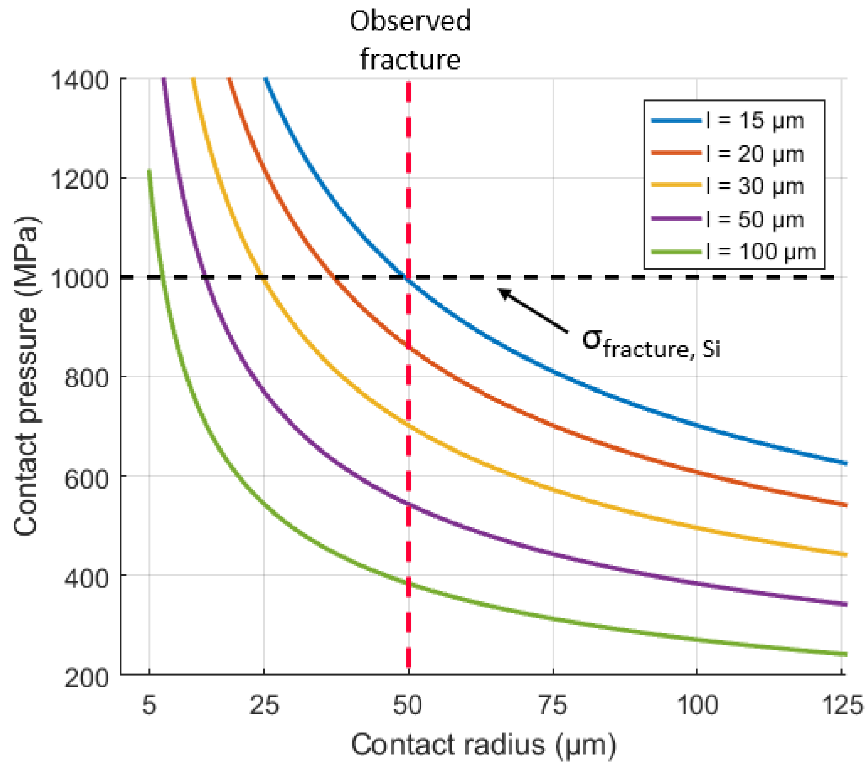


Figure 6-7. Hertzian contact pressure versus contact radius shown for varying line contact lengths under a 25 mN load (maximum in this work). Fracture strength of Silicon shown by dotted black line, above which fracture is likely, and below which fracture is unlikely. The contact pressure of line contacts with radii less than 50 µm and lengths less than 15 µm are shown to exceed the fracture strength of Silicon. Because little fracture was observed in line contacts with radii greater than 50 µm, this indicates that the actual length of the contacting interface during initial fracture (when only the top portion was in contact) was less than 15 µm.

Hertzian contact pressure exceeds the fracture strength of Silicon in contacts with prescribed radii less than 50 µm and line contact lengths less than 15 µm. No fracture occurred in contacts with radii larger than 50 µm, indicating that the minimum real contact length during

loading was 15 μm. In contacts with small radii (< 20 μm), SEM imaging showed fracture was limited to the upper sidewall where contact first occurred (Figure 5-15). No fracture appeared centrally along sidewalls, where contact occurred during loading greater than 5 mN, indicating that line contact length was large enough to result in contact pressure below the fracture strength of Silicon. Several important considerations can be gleaned from this information for future ECR force sensors.

First, fracture is likely to occur in line contacts with small radii, but appears limited to the location of initial contact. Increasing pre-load and keeping it constant will increase the contact line length to reduce the Hertzian contact pressure below the fracture strength and will produce more consistent contact conditions, thereby preventing propagation of cracks along the contact interface.

Second, linearly sloping DRIE sidewall contacts with minimal taper should minimize sidewall fracture. Improved contact topology is also expected to reduce required device thickness, as contact line length increases in more consistent interface mating and better load distribution. Notably, no sidewall fracture was observed in area contacts.

Finally, SEM imaging did not reveal wear along the central area of the sidewall, nor did data of inertially tested chips after 100+ force cycles indicate wear. In micromotor applications, where intermittent contact and friction events are ubiquitous, significant wear between Silicon surfaces can occur during force cycling [35,36], although life of cyclic devices can exceed 700,000 cycles when friction events are minimized [37]. In an extreme case, wear in single crystal silicon was reported after only 5 cycles [38] using a 100 nm radius diamond tip to inject wear scars on silicon surfaces. However, wear in micromotors is caused by intermittent contact

and friction events, whereas contact is more consistent in an ECR-force sensor and is reliant on a change in the number of contacting nano-asperities rather than motion.

6.1.4 Native oxide effect

All chips were experimentally tested within two weeks to two months after fabrication. Modeling and previous work [16] both indicate Silicon dioxide growth on contacting sidewalls increases ECR proportional to layer thickness, however, modeling indicates that normalized resistance as it varies with applied force should not change (Figure 2-11). To test this, two chips were force cycled by manual elongation after two months of oxide build-up (equivalent to 8 Å SiO_2), and then after oxide removal by HF vapor (equivalent to 5 Å SiO_2), removing pre-load between testing. Corresponding ECR-force curves are plotted below (Figure 6-8).

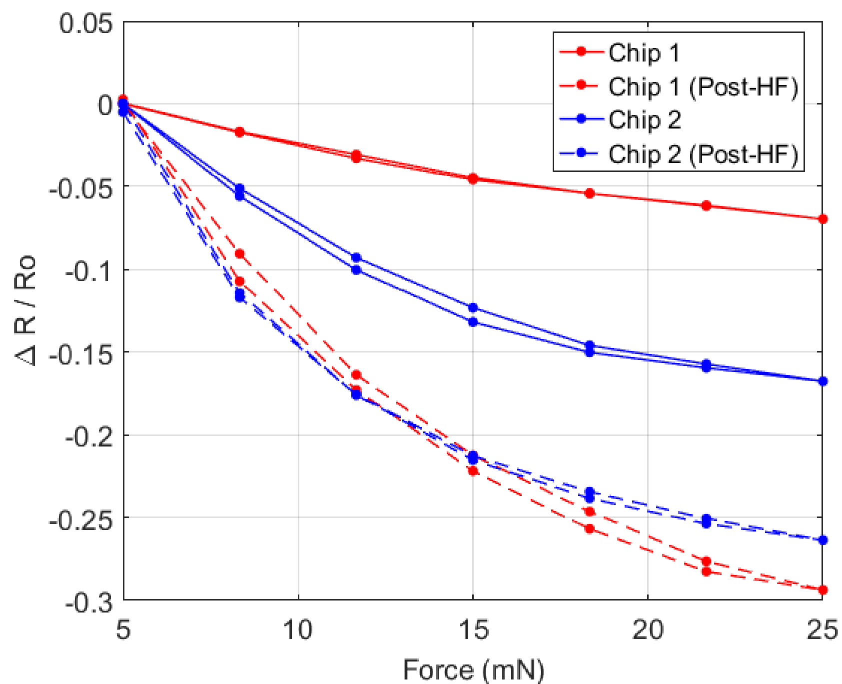


Figure 6-8. Normalized ECR versus force applied by manual elongation for two chips, prior to and after HF vapor exposure following two months of ambient surface oxide growth. Sensitivity is shown to decrease with oxide growth, at differing rates in each chip, while break-in again occurred after about ten cycles. However, it is important to note that pre-load was removed in between testing.

Testing of inertial chips with a constant pre-load periodically over two months, however, revealed no change in ECR-force behavior. Packaged inertial chips were not air-tight, indicating that a consistent pre-load may minimize oxide growth. Future investigation is needed to determine if pre-load is sufficient to overcome the effect of native oxide growth on ECR-force as a sensing technique.

6.1.5 Stiction

Chips with area contact interfaces frequently experienced stiction during testing (Figure **6-9**) that resulted in near-zero change in ECR with applied force, indicating that most of the interface succumbed to and remained in stiction.

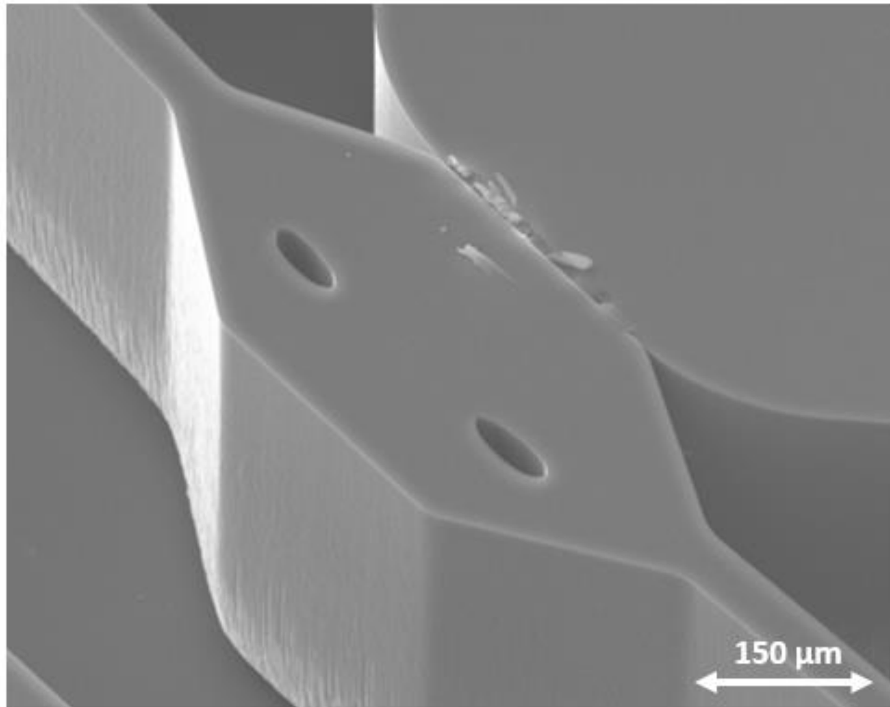


Figure 6-9. SEM of a 50 µm area contact interface under stiction with no applied force. Stiction frequently occurred during force cycling with wide area contacts, which resulting in significantly reduced ECR-force sensitivity.

While stiction was an issue with thermally actuated chips and area contact interfaces, stiction was not observed in chips with line contacts under force by manual spring elongation or inertially accelerated proof mass. Inertially loaded chips under pre-load were tested after 3 months in storage and did not experience stiction. The lack of stiction in line contacts was expected for two primary reasons. First, geometry features with line contacts of small radii are

frequently used to prevent stiction in a variety of MEMS devices [39] due to their inherent small contacting surfaces area. Second, the unintended DRIE sidewall curvature prevented uniform surface contact and likely allowed varying stress along the surface during force cycling, even in areas of surface adhesion. Recovery of stiction-failed MEMS structures has been shown to be overcome with varying stress waves [40], and the unintended sidewall curvature may have induced this effect.

6.2 ECR-based sensor comparison

6.2.1 Gauge factor

As the ECR sensing approach relies on a change in force, and therefore stress, an equivalent gauge factor can be calculated to relate performance to a typical strain gauge. Gauge factor (GF), or strain factor of a strain gauge, is the ratio of relative change in electrical resistance R, to the mechanical strain ε, given by

$$GF = \frac{\Delta R / R}{\varepsilon}. \tag{6-3}$$

Hertzian mechanical strain during cylinder-on-plane contact between two identical materials is given by

$$\varepsilon = \frac{\sigma}{E} = \frac{F}{AE} = \frac{F}{2blE} = \frac{F}{2lE\sqrt{\frac{2F}{\pi l}\frac{\frac{(1-\nu_1^2)}{E_1}+\frac{(1-\nu_2^2)}{E_2}}{\frac{1}{d_1}+\frac{1}{d_2}}}} = \frac{F}{2lE\sqrt{\frac{2Fd(1-\nu^2)}{\pi lE}}} \tag{6-4}$$

with applied force F, contact half-width b, contact line length l, and Young's Modulus of Silicon, E. Using (Eqs. 6-3, 6-4), the gauge factor can then be calculated as

$$GF = \frac{FSF}{\sqrt{\frac{8\,F\,d\,l\,E\,(1-\nu^2)}{\pi}}}, \tag{6-5}$$

where FSF is the force sensitivity factor defined by

$$FSF = \frac{\Delta R/_R}{F} \,. \tag{6-6}$$

For fabricated chips experimentally tested using force applied by embedded proof mass, the ratio of relative change in electrical resistance was 0.2 for applied force from 25 mN – 35 mN. The resulting gauge factor is 3.3 for parameters given below in Table 6-1.

Table 6-1. Parameter definitions and values used in gauge factor calculation, with the resulting gauge factor equal to 3.3. Note that the line contact length of 15 µm corresponds to the estimated length during initial contact of interfaces.

PARAMETERS		
Definition	Variable	Value
Relative change in R	$\Delta R/_R$	0.2
Applied force	F	10 mN
Young's Modulus (Silicon)	E	125 GPa
Poisson's ratio (Silicon)	E	0.27
Contact diameter	d	10 µm
Line contact length	l	15 µm

At higher forces (> 25 mN), the length of sidewall contact appears to be closer to the device thickness (100 µm), as indicated in Figure 5-15. For an ECR-force sensor with a line contact length of 50 µm (a reasonable estimated average value for the measured 0.2 normalized resistance change) and contact radius of 25 µm, the gauge factor is 13.5.

For a common bonded metallic strain gauge, gauge factor is typically around 2 [41]. As resistivity is constant, the gauge factor is also constant, and force sensitivity can only be changed through the geometry of the feature it is placed on (cantilever, serpentine spring, disc, etc.). For the ECR-force sensors in this work, however, the gauge factor is tailorable through alteration of surface roughness parameters (discussed in Chapter 2:), line contact length, and contact radius.

6.2.2 Calibration

Best-performing chips with force applied by inertial loading showed 24% chip-to-chip variance. Varying surface roughness, varying initial surface fracture during pre-load and break-in, varying sidewall topology, and varying initial mating orientation all contribute to varying ECR-force behavior between individual chips. While many of these variances can be minimized, a realized ECR-force sensor will still likely require calibration after fabrication to account for uncontrollable factors, similar to piezo-based sensors. Calibration will need to be done after pre-load, and likely after break-in cycling.

The effect of force application method on ECR behavior is expected to be minimized through proper lateral and mechanical constraints at the contact interface. Calibration after pre-load and break-in is expected to sufficiently capture any small variance in behavior induced by a new environment.

6.2.3 Force sensors

Compared to commercially available force sensors, the realized ECR force sensor has several advantages (smaller size, lower force range, and simpler fabrication) that may be further leveraged in future development. An overall comparison of the ECR force sensor versus a commercial FSR 402 force sensing resistor consisting of an 18.28 mm diameter, 450 µm thick polymer film is shown below in Table 6-2.

Table 6-2. Comparison of ECR-force sensor to a commercially available force sensing resistor.

	ECR Force sensor	FSR 402 Force Sensor [44]
Force range, tested	25 – 35 mN	100 – 10,000 mN
Sensitivity	tailorable by proof mass	10 Ω / g
Force repeatability, single chip	± 2 % RSD	± 2 %
Force Resolution	continuous	continuous
Force Repeatability, chip-to-chip	± 24 %	± 6 %
Size	8 x 8 mm square	18.28 mm diameter
Area	64 mm^2	1050 mm^2
Thickness	0.6 mm	0.2 - 1.25 mm
Hysteresis	2 %	10 %
Rise Time	< 30 μs	< 3 μs
Number of Actuations (tested)	~ 100	10 M
No required laminates / adhesives	yes	no
Single material	yes	no

Utilizing the ECR-force relationship for use as an acceleration may also provide several advantages over existing accelerometers based on common transduction principles, as depicted below in Figure 6-10. ECR-force sensors are also able to sense acceleration by inertially accelerating a proof mass into a contacting pair, allowing simple adjustment over a wide range of acceleration by adjusting the size of the proof mass. As the inertial mass is tailorable to target a desired g-range, the contact radius is also tailorable to allow measurement of higher force ranges, likely above 100 mN (modeling indicates that sensitivity becomes poor > 200 mN).

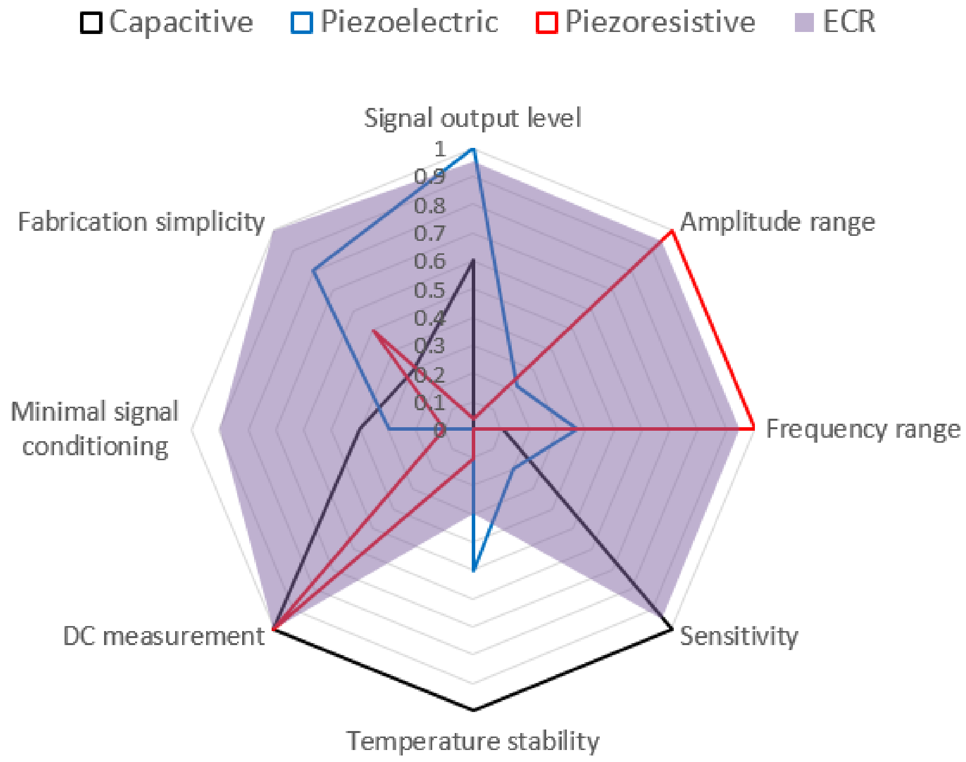


Figure 6-10. Comparison of accelerometer sensing mechanisms.

Chapter 7: Conclusion

A sensing mechanism based on simplistic rate-independent changes in electrical contact resistance (ECR) is explored as an alternative to existing force sensing techniques in silicon-based MEMS devices. The use of DRIE, as opposed to additive poly-Silicon-based fabrication, allows a tailorable force range through proof mass sizing and aspect ratio changes, adjustable pre-load through simple design, and integration of an ECR force sensor into existing systems. The successful use of a proof mass to apply force by acceleration indicates ECR between SOI-DRIE interfaces is a viable method to measure acceleration in the future. As with piezo-sensors, calibration of ECR force sensors is expected to improve chip-to-chip repeatability. Compared to commercially available force sensors, the realized ECR force sensor has several advantages (smaller size, lower force range, and simpler fabrication) that may be further leveraged in future development.

Table 7-1. Summary of SOI-DRIE ECR-force sensor performance

Parameter	Value
Force method	Accelerated proof mass, manual spring elongation
Contact type	line, area
Contact radius	5 - 100 μm
Device thickness	100 μm
Contact force	5 - 35 mN
Single-chip RSD	1.6 - 21.4 %
Chip-to-chip RSD	19.7 - 114.2 %
Hysteresis	2.1 - 17.6 %
Sensitivity	0.9 - 2.3 %/mN

7.1 *Summary*

Several analytic models were combined to create a macro-scale ECR-force model to determine expected ECR sensitivity versus applied force for line contacts of varying radius and line contact length. A Greenwood-Williamson model for determining equivalent mechanical properties of two contacting surfaces separated by an insulating film was combined with fractal surface modeling to express contact surface topology in terms of truncated real contact area. Electrical contact resistance for a single microasperity under elastic to fully plastic deformation was integrated over the full contact surface to give an expected electrical contact resistance for a given contact force. Hertzian theory for cylinder-on-plane geometry for a given contact radius was used to determine apparent contact area under a given load, the conditions of loading under which the yield strength of Silicon is exceeded, and combined with the Greenwood-Williamson model to provide a relationship between applied force and contact radius and line contact length. Mechanical structures used to apply force in each loading technique were modeled analytically and by finite element analysis.

Experimental testing was done in 3 phases, each of which utilized a different method to apply cyclical contact force to contacting DRIE interfaces during ECR-force measurements. First, the feasibility of using ECR to sense force in bare DRIE silicon contacts was evaluated using force applied by simple thermal actuation. Second, relative performance and the effects of varying contact geometry microsystem constraints on ECR-force behavior was investigated using manual spring elongation. Third, sensitivity and repeatability within single chips and groups of chips were quantified using force applied by inertial acceleration of embedded proof masses in packaged chips.

Several design and fabrication iterations were used to arrive at sufficiently capable micromechanical systems for manually loaded and inertially accelerated chips. Devices were

fabricated using simple two-mask SOI DRIE processes. SEM images of fabricated sidewall contact interfaces show that sidewall topology was not linearly sloping as expected, and a Hertzian model with adjusted line contact length was used to account for the reduction in apparent contact area.

Single line contacts were most reliable, multi-line contacts were least reliable, and area contacts intermittently succumbed to stiction. Line contacts showed fracture during loading with contact radii < 20 µm, and no fracture with contact radii > 50 µm, while chips with contact radii > 100 µm intermittently succumbed to stiction. A model was provided for expected fracture behavior of varying contacts with differing line contact lengths to guide future work that may utilize wafers of different thickness or etched DRIE surfaces of varying topology.

Chips where force was applied by inertial loading demonstrated good repeatability of normalized ECR as a function of applied force. With improved packaging techniques and optimized design layouts, further improvement in repeatability is expected to be available. The use of DRIE, as opposed to additive poly-Silicon-based fabrication, greatly enhances the ability for future design improvement and performance tuning by allowing integration of an ECR-force sensor into existing systems, fine-tuning of the force range and applied spring forces by simple adjustment of the aspect ratio, and simple adjustment of the proof mass. Additionally, utilizing a proof mass to apply force under an acceleration allows use of the ECR-force mechanism as a method to measure acceleration in the future. Maximum force range between a single set of contact interfaces is will be dictated by the required number of cycles of a device, where larger force results in higher rate of wear during force cycling, as well as required sensitivity, which decreases with increasing force. Simple calibration of a fabricated ECR-force sensor, as with piezo-sensors, is expected to allow for significant improvement in chip-to-chip repeatability.

7.2 ECR-force performance characterization

Thermally actuated chips with line contacts showed normalized single-chip RSD of ± 43%, chip-to-chip RSD of ± 51%, and average hysteresis of 14%. ECR increased with increased force cycling, indicating potential charge build-up or a reduction in the applied force within the thermal actuator. Charge build-up and limited displacement of the thermal actuators made it difficult to accurately gather data with meaningful resolution. Stiction occurred at less than ten force cycles in nearly every chip, preventing "break-in" from fully occurring. For these reasons, force applied by thermal actuator was shown to be a poor method for measuring ECR-force behavior.

Average resistance varied in manually probed line and area contacts by approximately 200 Ω and 290 Ω (1.7 %/mN and 1.5 %/mN), respectively, from 5 mN to 25 mN. After normalization by division of the initial absolute resistance, manually actuated chips with line contacts showed best single-chip RSD of 3%, chip-to-chip RSD of 20%, and average hysteresis of 4%, while chips with area contacts showed single-chip RSD of 3%, chip-to-chip RSD of 29%, and average hysteresis of 9%. Rotation and sliding at the contact interface significantly increased ECR variance, removal of contact or failure to maintain pre-load produced discontinuous ECR-force curves, unintentional spring assembly recoil during motion caused noticeable surface fracture at the contact point, and irregular spring assembly movement occurred during improper alignment or rough motion of the probe. Robust lateral constraints, a consistent contact point, and minimum pre-load were critical to reliable measurement.

Inertial loading allowed automated testing, reduced the influence of mechanical misalignment on ECR measurements that occurred during manual actuation, and served as a simplified test case for using ECR transduction in acceleration sensing. Average resistance in inertially accelerated chips varied by approximately 150 Ω and 300 Ω in line contacts of 5 µm

and 25 μm, and 100 μm radius, respectively, when subjected to applied force from 25 mN to 35 mN. After normalization by division of the initial absolute resistance, inertially actuated chips with line contacts showed best single-chip RSD of ± 2%, chip-to-chip RSD of ± 24%, and average hysteresis of 2%. Differences between chips of varying contact size were not as prominent in inertially tested chips compared to manually tested chips, however, contacts interfaces with smaller dimensions remained best performers. Single-chip repeatability, chip-to-chip repeatability, and hysteresis all worsened with increasing contact radius, while zero-shift and sensitivity were largely uncorrelated. ECR-force sensitivity of all chips was between 1 – 2 %/mN, and varied most in area contacts likely due to sliding at the contact interface.

7.3 Future work

7.3.1 Recommended design principles for further characterization

While DRIE sidewall topology varied in this work, and is expected to vary in future work, the models and techniques presented allow the possibility of creating a repeatable ECR-force sensor largely independent of fabricated sidewall topology by simply accounting for the adjusted real line contact length via the Hertzian model and post-fabrication calibration.

Isolating bond pads from any moving structures was essential to obtaining repeatable measurements, as charge build-up within the chip was otherwise able to affect measurement. Debris from fabrication and handling, and residue from DRIE undercut were both found to negatively impact the single-chip repeatability of manually loaded chips. Additional care taken to ensure clean chips, perhaps by packaging, is expected to further improve repeatability.

Inertially accelerated chips were tested from 25 mN to 35 mN, but anecdotal testing and analytical modeling show that testing beyond this range should be feasible, given that the contact radius at the interface does not exceed the yield stress of Silicon. Additionally, while the model

predicts increasing sensitivity at decreasing contact radii, it is likely beneficial to maximize the contact radius, up until stiction begins to appear, in order to minimize fracture during cyclic loading. Chips in this work were tested with contact radii of 5 µm, however, it is recommended that future work define contact geometry with 25 µm < r < 100 µm to minimize fracture at small radii and avoid stiction at large radii. Future systems should also maintain a consistent pre-load between contacting interfaces to avoid contact separation.

While the microsystems developed in this work proved sufficient for obtaining repeatable measurements, there remains room for improvement. Fabrication issues combined with the manual nature of force application in chips relying on probe-induced force resulted in zero-shift and hysteresis, while flaws in packaging of chips relying on inertial masses for force application led to less-than-desired repeatability. Further microsystem development and corrected packaging techniques are expected to improve future reliability and repeatability. A realized ECR-force sensor will likely require initial calibration (as with many existing commercial piezo sensors), but is expected to be repeatable afterwards.

7.3.2 Future designs using metamaterial behavior

ECR-based sensors behave similarly to metamaterials, which derive their primary sensing behavior from geometry rather than intrinsic material properties. As such, ECR-based sensor designs may benefit greatly from using metamaterial design. While contact interfaces with multiple contact points were explored initially in this work, focus was on obtaining a repeatable relationship between ECR and force in geometry with minimal complexity. However, future work may reveal that using many contact interfaces in parallel and/or series provide a significant improvement to sensitivity and/or reliability through redundancy or multiplicative effects. Examples of potential future ECR-based sensor designs are given below in Figure 7-1.

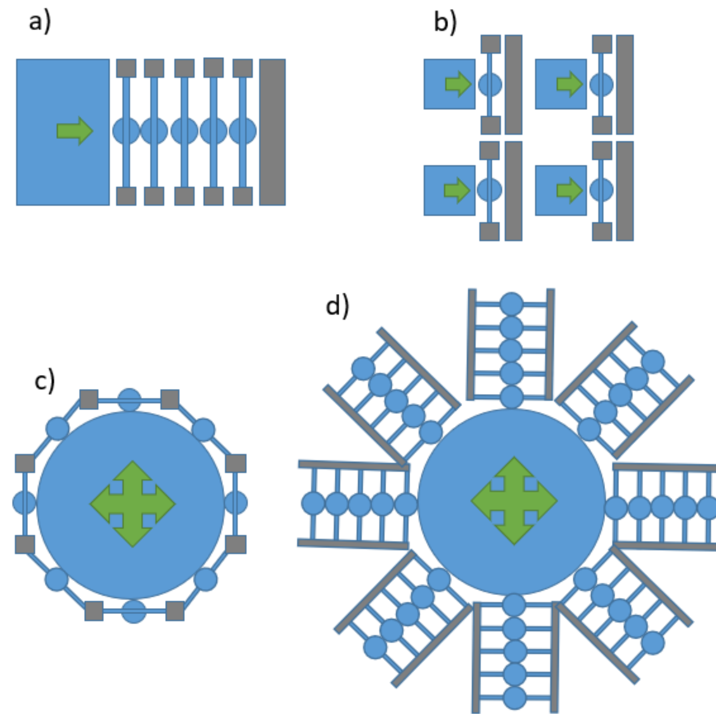


Figure 7-1 Schematics of potential ECR-based sensor designs, showing a) linear series, b) redundant, c) planar, and d) planar series sensing.

7.4 Scientific and Technical Contributions

(1) Developed an analytical ECR-force model for rough contacting DRIE surfaces by combining ECR and Hertzian contact theory

- Established that ECR between DRIE MEMS interfaces is both variable and controllable by applied contact force.
- Previous investigations into ECR in DRIE MEMS either look to minimize its effect, or fail at obtaining repeatable output. Using electrical isolation and an applied pre-load of at least 5 mN, single chips with line contact interfaces showed repeatable force-cycling behavior, with single-chip relative standard deviation less than 2% for force cycles 80 - 100.

- Revealed that normalizing ECR output by dividing the absolute change of ECR by the initial ECR reduced chip-to-chip variance, and reduced the effect of contact size on ECR as it varied with applied contact force. Unpredictable DRIE surface topologies were shown to be largely overcome, indication that future investigations need not to focus attention on fabrication parameters.
- Fabricated using methods that do not require selective doping, thin-film deposition, exotic materials, bonded structures, additional circuitry, or external transducers.

(2) Developed a relationship between contact shape and sidewall fracture in contacting DRIE MEMS surfaces under applied forces up to 35 mN

- Revealed that increasing the contact radius dramatically reduced cycle-to-cycle sidewall fracture. Chips tested with contact radii < 25 μm showed significant upper sidewall fracture after ~ 100 force cycles, while those with contact radii > 50 μm showed minor wear on the top sidewall edge after ~100 force cycles that did not appear to propagate.
- Discovered that area contacts of all tested widths, and line contacts with radii > 75 μm were susceptible to stiction.

(3) Developed a method to sense acceleration using the newly established relationship between contact resistance and force in DRIE-SOI MEMS

- Identified the potential to develop integrated accelerometers with exceptionally high stiffness and resonance frequencies that are easily tailored by proof mass alteration and system design. With applied pre-load, integrated proof masses acting on isolated

contact interfaces show the ability to reliably measure ECR output related directly to acceleration through the proof mass.

(4) Developed three independent flexible microsystem architectures and associated guidelines for future development and characterization of the ECR-force phenomenon in DRIE SOI-MEMS.

- Revealed line contacts to exhibit high repeatability, multi-line contacts to exhibit unpredictable cycle-to-cycle convergence, and area contacts to be susceptible to stiction
- Revealed that testing methods utilizing high power (thermal actuators in this case) will likely induce stiction between contact interfaces.
- Revealed that force applied by inertial loading through an accelerated proof mass allows for a highly repeatable characterization of the ECR-force phenomenon in a fully packaged chip.
- While the ECR-force model predicted that decreasing the contact radius should increase the absolute output sensitivity and initial absolute ECR, there was not enough statistical evidence to validate this claim. Two soluble causes were identified. Variance in surface topography arising from fabrication issues inherent in a multi-user facility require a larger number of chips to be tested, and the variance in initial interface mating after pre-load (from slight shearing and rotation, and real pre-load error) resulted in overall lack of repeatability.

(5) Published a journal article detailing the related scientific contributions of this work in Sensors and Acutators: A [2].

Appendix A: Matlab scripts

I. ECR-Hertzian model

```
% Note that equation numbers are referenced to L. Kogut and K. Komvopoulos:
% "Electrical contact resistance theory for conductive rough surfaces
% separated by a thin insulating film", 2004.
% Need to implicity solve for the truncated contact area (a_prime) (aka
% the fraction of the area between contacting asperities that is actually
% in contact, typically between) at each applied force because the amount
% of area in contact changes for a given load

clear all

% Post-processing constants
global_font_size = 12;
global_marker_size = 18;
global_LW_size = 2;
fig_size2 = [648   224   665   383]; % diss two plots in column stack with
room for capion

figure, fig_ecrforce_norm = gcf;
figure, fig_ecrforce_delta = gcf;
figure, fig_ecrforce_raw = gcf;
figure, fig_forceaa = gcf;
figure, fig_forcear = gcf;
figure, fig_forcepress = gcf;

% Constants
e = 1.6E-19; % constant
c = 2.8; % constant
gamma = 1.5; % constant

% Silicon material parameters
E = 125E9; % Pa, Young's Modulus
Y = 1E9; % Pa, Yield strength
v = 0.27; % Poisson's ratio
path_resistance = 0; % measured 500

% Real contact area parameters
b1 = ((pi()*(0.454+0.41*v))/2)^2;
a = (5.431); % (Angstrom), Lattice constant for Silicon
a = a*1E-8; % (cm), Lattice constant for Silicon

% Fractal parameters
Rq = 0.2E-6; % (m), RMS roughness, found from FRT scan

% Range of variables to loop
D_range = 2.3; % (2<D<3), fractal dimension, higher D is smoother surface
G_range = Rq.^2; % Rq^2; (m^2), higher G is a rougher surface
r_range = [5 5 5 5 5]*1E-6; % Must be same length as l
l_range = [100 100 100 100 100]*1E-6; % Must be same length as r
F_range = [25:1:35]*1E-3;
```

```
t_range = [7 7.5 8 8.5 9];

ColorSet = varycolor(5);
leg_count = 1;
q = 0;
for G_index = 1:length(G_range)
    G_prime = G_range(G_index); % fractal roughness

    for D_index = 1:length(D_range)
        D = D_range(D_index); % fractal dimension

        for i = 1:length(r_range)
            q = q + 1; % Overall index
            % Hertzian parameters to determine apparent contact
            l = l_range(i);
            r = r_range(i); % m
            d = r.*2; % Diameter

            for k = 1:length(F_range)
                F = F_range(k);

                % Hertzian parameters to determine apparent contact
                b2 = sqrt((2.*F/(pi()*l))*(2*(1-v^2)/E)/(1/d)); % (m),
contact area half-width
                Aa = 2.*b2.*l;  % (Angstrom), apparent contact area - found
via hertz equation
                Aa = Aa .* 10000; % Convert to (cm^2)
                Aa_out(k) = Aa;
                cont_pres = 2.*F./(pi().*b2.*l); % (Pa)
                cont_pres_out(k) = cont_pres;

                % Calculate the truncated contact area based on the applied
load and fractal parameters
                G = G_prime.*sqrt(Aa); % (cm), (10E-17<G<10E-13 m), higher G
is a rougher surface
                G_out(i,k) = G;
                % Calculate the critical, smallest, and largest truncated
microasperity areas
                % diameter of the smallest truncated area aS assumed to be
equal to 6x the lattice dimension
                aS_prime = pi()*(a/2).^2; % (cm^2)
                ac_prime = ((2.^(9-2*D).*pi.^(D-2)*b1^-1.*G.^(2*D-
4).*(E/(c*Y))^2*log(gamma))).^2; % (cm^2), critical truncated area

                % Use implicit solver to find the value of aL for given
hertzian applied load (using Eq. 2)
                aL_find(k) = fzero(@(aL) Aa*E*c*Y/E * (D-1)/(3-D) *
(((aL)^2)./Aa) *(((ac_prime./Aa)/(((aL)^2)./Aa))^...
                    ((3-D)/2)-((aS_prime./Aa)/(((aL)^2)./Aa))^((3-D)/2))-
F,a*6);% (cm), largest truncated area
            end
            aL = aL_find;
            aL_prime = (aL_find).^2; % (cm^2)

            % Equation 2
```

```
            P_star = c*Y/E .* (D-1)/(3-D) .* (((aL_prime).^2)./Aa) .*
(((ac_prime./Aa)./(((aL_prime).^2)./Aa)).^...
                ((3-D)/2)-
((((aS_prime).^2)./Aa)./(((aL_prime).^2)./Aa)).^((3-D)/2)); % (cm^2)
            P = P_star.*Aa.*E;

            % Tunneling resistance parameters
            Vi = 1; % (V) Initial Voltage
            K = 4.5;
            t = t_range(i); % (A), thickness
            phi0 = 1; % (A)
            S1 = 6/(K*phi0); % (A)

            % Tunneling resistance calculations - For Vi near zero
            Ar = (D-1)/(2*(3-D)) * aL_prime .* ((ac_prime./aL_prime).^((3-
D)/2)-2.*(aS_prime./aL_prime).^((3-D)/2)+1); % (cm^2)
            S2 = t - 6/(K*phi0); % (A)
            delS = S2-S1; % (A)
            phiL = phi0 - (5.75/(K*delS))*log((S2*(t-S1))/(S1*(t-S2))); % (A)
            Ii = Ar .* (3.16E10/delS)*sqrt(phiL) * exp(-
1.025*delS*sqrt(phiL)) * Vi;
            Ri_zero_Vi = Vi./Ii + path_resistance;

            %% Plotting
            if ~isnan(Ri_zero_Vi(1)) % No legend entry is answer is NaN
                legentry{i} = ['t = ',num2str(t),' Å'];
                leg_count = leg_count + 1;
            end

            R_norm = (Ri_zero_Vi-max(Ri_zero_Vi))./mean(Ri_zero_Vi);

            % Plotting the applied force, which dictates the hertzian
apparent
            % contact area, versus the current integrated over that area

            figure(fig_ecrforce_norm)

plot(F_range.*1000,R_norm,'linewidth',global_LW_size,'Color',ColorSet(q,:));
            hold all
            set(gcf,'position',fig_size2,'color',[1,1,1])
            xlabel('Force (mN)','fontsize',global_font_size)
            ylabel('Resistance (\Omega)','fontsize',global_font_size)
            ylabel('\Delta R / Ro','fontsize',global_font_size)
            title('Normalized ECR vs Applied
force','fontsize',global_font_size)
            grid on
            if ~isnan(Ri_zero_Vi(1)), legend(legentry), end

            figure(fig_ecrforce_delta)
            plot(F_range.*1000,(Ri_zero_Vi-
max(Ri_zero_Vi)),'linewidth',global_LW_size,'Color',ColorSet(q,:));
            hold all
            set(gcf,'position',fig_size2,'color',[1,1,1])
            xlabel('Force (mN)','fontsize',global_font_size)
            ylabel('Resistance (\Omega)','fontsize',global_font_size)
```

```
            ylabel('\Delta R (\Omega)','fontsize',global_font_size)
            title('Delta rECR vs Applied force','fontsize',global_font_size)
            grid on
            legend(legentry)

            figure(fig_ecrforce_raw)
plot(F_range.*1000,Ri_zero_Vi,'linewidth',global_LW_size,'Color',ColorSet(q,:
));
            hold all
            set(gcf,'position',fig_size2,'color',[1,1,1])
            xlabel('Force (mN)','fontsize',global_font_size)
            ylabel('Resistance (\Omega)','fontsize',global_font_size)
            title('Raw ECR vs Applied force','fontsize',global_font_size)
            grid on
            if ~isnan(Ri_zero_Vi(1)), legend(legentry), end

            figure(fig_forceaa)
plot(F_range.*1000,Aa_out*1E8,'linewidth',global_LW_size,'Color',ColorSet(q,:
));
            hold all
            set(gcf,'position',fig_size2,'color',[1,1,1])
            xlabel('Force (mN)','fontsize',global_font_size)
            ylabel('Apparent contact area
(µm^2)','fontsize',global_font_size)
            title('Apparent contact area vs Applied
force','fontsize',global_font_size)
            grid on
            if ~isnan(Ri_zero_Vi(1)), legend(legentry), end

            figure(fig_forcear)
plot(F_range.*1000,Ar*1E14,'linewidth',global_LW_size,'Color',ColorSet(q,:));
            hold all
            set(gcf,'position',fig_size2,'color',[1,1,1])
            xlabel('Force (mN)','fontsize',global_font_size)
            ylabel('Real contact area (nm^2)','fontsize',global_font_size)
            title('Real contact area vs Applied
force','fontsize',global_font_size)
            grid on
            if ~isnan(Ri_zero_Vi(1)), legend(legentry), end

            figure(fig_forcepress)
plot(F_range.*1000,cont_pres_out./1E9,'linewidth',global_LW_size,'Color',Colo
rSet(q,:));
            hold all
            set(gcf,'position',fig_size2,'color',[1,1,1])
            set(gca,'fontsize',global_font_size)
            xlabel('Force (mN)','fontsize',global_font_size)
            ylabel('Pressure (MPa)','fontsize',global_font_size)
            grid on
            title('Contact pressure vs Applied
force','fontsize',global_font_size)
            if ~isnan(Ri_zero_Vi(1)), legend(legentry), end
```

```
        end
    end
end
```

II. Fractal surface plotting

```
%% Fractal plotting
% [z , PixelWidth, PSD] = artificial_surf(sigma,H,Lx,m,n)
% (in SI units)
% sigma: standard deviation , i.e. root-mean-square roughness Rq(m)
% H: Hurst exponent (roughness exponent), 0<= H <= 1, D = 3-H
% Lx: length of topography in x direction.

H = 3-D; % D = 3 - H, Hurst exponent (roughness exponent), 0<= H <= 1, D = 3-
H
Lx = 20E-6; % (m), length of topography in x direction
m = 512; % m: number of pixels in x
n = m; % n: number of pixels in y
[z , PixelWidth, PSD] = artificial_surf(Rq,H,Lx,m,n);
[n,m] = size(z);
x = linspace(0,(m-1) * PixelWidth , m);
y = linspace(0,(n-1) * PixelWidth , n);
[X,Y] = meshgrid(x,y);

figure
mesh(X.*1E6,Y.*1E6,z.*1E6)
colormap jet
axis equal
set(gcf,'position',fig_size2,'color',[1,1,1])
set(gca,'fontsize',global_font_size)
xlabel('Length (µm)','fontsize',global_font_size)
ylabel('Width (µm)','fontsize',global_font_size)
zlabel('Height (µm)','fontsize',global_font_size)
title('Fractal topology','fontsize',global_font_size)
```

III. Data extraction

```
% Matlab script used for data extraction, analysis, and plotting
% Cycle through all output files, assigning them to corresponding names,
% calculating performance, plotting each on the same figure with error bars

clear all
global_font_size = 12;
global_marker_size = 18;
global_LW_size = 1;
fig_size = [174   282   665   505]; % Size for full page single plote

% Grab dataout files in all sub-directories. rdir is in Matlab Central user
repository
D = rdir('**\dataout*');
% Convert to a cell aray
D1 = {D.name}.';
% Correctly sort file names, with natural numbering. sort_nat in Matlab
Central
D1 = sort_nat(D1);
```

```
% Initialize variables
i=0;
allchips_percent_ave = zeros(10,10);
allchips_percent_std = zeros(10,10);
figure, fig_ebar = gcf;
ColorSet = varycolor(length(D1));

% Loop through all of the data output, one i per dataset
for i=1:length(D1)
    % Gather the chip names via REGEX matching
    chipfile = D1{i};
    regsep = regexp(chipfile,'(?<=\\)(.*?)(?=\\)', 'match');
    chiptype = regexp(chipfile,'(?<=\\)(.*?)(?=\-)', 'match');
    chipnum = regsep{1}(end);
    chipvalue = chiptype{1}(2:end);

    % Import the data
    data = importdata(chipfile);

    % Format dataout to move new full cycles into new columns
    cys = find(data==data(1,1)); % Find each row where the distance is the
same as the initial, aka start of new cycle
    for j = 1:length(cys)/2-1
        data(cys(1):cys(2),j+3) = data(cys(j*2+1):cys(j*2+2),3);
    end
    data = data(cys(1):cys(2),:); % now additional columns represent new
cycles

    % Pull out the resistance measurements
    resistance = (data(:,3:end))';
    [rows,loops] = size(resistance);

    % Cycles go across the rows, each column is at a measured force level
    [m,n] = size(resistance);
    Ro = resistance(:,1);

    % Calculate these variables for plotting the lines (calculate the error
bars
    % afterwards, which combines forwards and backwards motion)
    raw_plotting = resistance;

    % Substract the first column from each row to get deltas
    delta_plotting = raw_plotting - repmat(Ro,[1,n]);

    % Divide delatas by fist column from each row to normalize to initial res
    percent_plotting = delta_plotting./repmat(Ro,[1,n])*100;
    force_plotting = (data(:,2))';

    raw_ave_plotting = mean(raw_plotting); % (ohm)
    delta_ave_plotting = mean(delta_plotting); % (ohm)
    percent_ave_plotting = mean(percent_plotting); % (%)

    % Combine the forwards and backwards motion into the same force columns
```

```
    % Averaged over all cycles for each chip - each column represents a
measured force level
    mid_data = round(loops/2);
    percycle_resistance = resistance(:,1:mid_data);
    percycle_resistance(rows+1:rows*2,1:end) =
fliplr(resistance(:,mid_data:end));
    Ro = [percycle_resistance(1:rows,1);percycle_resistance(1:rows,1)];
    [mm,nn] = size(percycle_resistance);
    clear hysteresis
    for l=1:m
        hysteresis(l,:) = percycle_resistance(l,:) -
percycle_resistance(l+mm/2,:);
    end
    % this is the average hysteresis at each force, for each chip
    hysteresis = mean(hysteresis);

    % Raw resistance
    raw_percycle = percycle_resistance;

    % Substract the first column from each row to get deltas
    delta_percycle = raw_percycle - repmat(Ro,[1,nn]);

    % Divide delatas by fist column from each row to normalize to initial res
    percent_percycle = delta_percycle./repmat(Ro,[1,nn])*100;

    distance = data(1:mid_data,1);
    force = data(1:mid_data,2)';
    force_delta = ([0 force(2:end)] - [0 force(1:end-1)]); % (mN)

    [~,ii,v] = find(percent_percycle(:,2:end));
    single_ave = (accumarray(ii,v,[],@mean)); % (%)
    single_percent_ave = (accumarray(ii,v,[],@mean))./force(2:end)'; % (%/mN)
    single_percent_std = (accumarray(ii,v,[],@std)); % (%/mN)
    single_repeatability =
accumarray(ii,v,[],@std)./accumarray(ii,v,[],@mean); % (%)

    allchips_percent_ave(i,1:length(single_ave)) = single_ave';
    allchips_percent_std(i,1:length(single_ave)) = single_percent_std';

    all_percent_ave(i) = mean(single_percent_ave); % (%/mN)
    all_repeatability(i) = abs(mean(single_repeatability))*100; % (%)

    [~,ii,v] = find(delta_percycle);
    single_delta_ave = (accumarray(ii,v,[],@mean))./force'; %(ohm/mN)
    single_delta_std = (accumarray(ii,v,[],@std)); %(ohm/mN)

    [~,ii,v] = find(raw_percycle);
    single_raw_ave = accumarray(ii,v,[],@mean); %(ohm/mN)
    single_raw_std = accumarray(ii,v,[],@std); %(ohm/mN)

    raw_ave = mean(raw_percycle); % (ohm)
    delta_ave = mean(delta_percycle); % (ohm)
    percent_ave = mean(percent_percycle); % (%)

    raw_std = std(raw_percycle); % (ohm)
```

```
    delta_std = std(delta_percycle); % (ohm)
    percent_std = std(percent_percycle); % (%)

    raw_std_plotting = [std(raw_percycle) zeros(1,mid_data-1)]; % (ohm)
    delta_std_plotting = [std(delta_percycle) zeros(1,mid_data-1)]; % (ohm)
    percent_std_plotting = [std(percent_percycle) zeros(1,mid_data-1)]; % (%)

    repeatability_singlechip(i) =
percent_sensitivity_std(i)/percent_sensitivity_ave(i);
    repeatability_chiptochip(i) =
chiptochip_percent_std(i)./chiptochip_percent_ave(i);
    hysteresis_ave(i) = abs(mean(hysteresis./delta_ave));

    figure(fig_ebar)
    % Plot the percents
    subplot(1,2,1)
    hold on
    switch str2double(chipvalue)
        case 5
            errorbar(force-
force(1),percent_ave./100,percent_std./100,'.','linewidth',2,'color','r','mar
kersize',1);
            n1 = plot(force_plotting-
force_plotting(1),percent_ave_plotting./100,'--
','linewidth',2,'color','r','markersize',18);
        case 20
            errorbar(force-
force(1),percent_ave./100,percent_std./100,'.','linewidth',2,'color','k','mar
kersize',1);
            n2 = plot(force_plotting-
force_plotting(1),percent_ave_plotting./100,':','linewidth',2,'color','k','ma
rkersize',18);
        case 50
            errorbar(force-
force(1),percent_ave./100,percent_std./100,'.','linewidth',2,'color','b','mar
kersize',1);
            n3 = plot(force_plotting-
force_plotting(1),percent_ave_plotting./100,'-
','linewidth',2,'color','b','markersize',18);
    end

    set(gcf,'Color',[1,1,1],'position',fig_size)
    ylim([-100 40]./100)
    set(gca,'YTick',[-1.2 -1 -0.8 -0.6 -0.4 -0.2 0 0.2 0.4])
    xlim([-5 26])
    set(gca,'XTick',[0 10 20 30 40 50])
    set(gca,'fontsize',global_font_size)
    xlabel('\Delta Force (mN)','fontsize',global_font_size)
    ylabel('\Delta R / Ro','fontsize',global_font_size)

    % Plot the deltas
    subplot(1,2,2)
    hold on
    switch str2double(chipvalue)
        case 5
```

```
errorbar(force,delta_ave,delta_std,'.','linewidth',2,'color','r','markersize'
,1);
            p1 = plot(force_plotting,delta_ave_plotting,'--
','linewidth',2,'color','r','markersize',18);
        case 20

errorbar(force,delta_ave,delta_std,'.','linewidth',2,'color','k','markersize'
,1);
            p2 =
plot(force_plotting,delta_ave_plotting,':','linewidth',2,'color','k','markers
ize',18);
        case 50

errorbar(force,delta_ave,delta_std,'.','linewidth',2,'color','b','markersize'
,1);
            p3 = plot(force_plotting,delta_ave_plotting,'-
','linewidth',2,'color','b','markersize',18);
    end
    ylim([-1000 400])
    set(gca,'YTick',[-1400 -1200 -1000 -800 -600 -400 -200 0 200 400])
    xlim([0 50])
    set(gca,'XTick',[0 10 20 30 40 50])
    set(gca,'fontsize',global_font_size)
    xlabel('Force (mN)','fontsize',global_font_size)
    ylabel('\Delta R (\Omega)','fontsize',global_font_size)
end

% Add the legend, depending on what contact type it is
switch D1{1}(1)
    case 'W'
        legend([p1,p2,p3],'w = 5','w = 20','w = 50'); % For the W chips
        legend([n1,n2,n3],'w = 5','w = 20','w = 50'); % For the W chips
    case 'R'
        legend([p1,p2,p3],'r = 5','r = 20','r = 50'); % For the R chips
        legend([n1,n2,n3],'r = 5','r = 20','r = 50'); % For the R chips
end

average_repeatability_for_single_chips =
abs(mean(repeatability_singlechip)*100);
average_repeatability_chip_to_chip =
abs(mean(std(repeatability_chiptochip')'./mean(repeatability_chiptochip')')*1
00);

disp(['Average single chip repeatability:
',num2str(average_repeatability_for_single_chips),...
    '% | Mean: ',num2str(mean(percent_sensitivity_ave)),' ohm/mN | StDev:
',num2str(std(percent_sensitivity_std)),' ohm/mN'])
disp(['Chip-to-chip repeatability:
',num2str(average_repeatability_chip_to_chip),...
    '% | Mean: ',num2str(mean(mean(chiptochip_percent_ave')')),' ohm/mN |
StDev: ',num2str(mean(std(chiptochip_percent_ave')')),' ohm/mN'])
disp(['Average hysteresis: ',num2str(mean(hysteresis_ave_singlechip)*100),...
    '% | Max hysteresis: ',num2str(max(hysteresis_max_singlechip)*100),'%'])
```

Appendix B: Aerotech task code

```
* Declare variables
DIM Distance AS DOUBLE
DIM Vel AS DOUBLE
DIM Vel_inc AS DOUBLE
DIM ARate AS DOUBLE

* Default mode, using acceleration rate
RAMP MODE TIME

* Set the last acceleration/deceleration rate
RAMP TIME 1

* Set the velocity increase per repeat (deg/s)
Vel_inc = 360

% Start controller
ENABLE
Vel = 0

% Ramp up the velocity
REPEAT 20
Vel = Vel + Vel_inc
Distance = Vel*10 * Set so that this is never fulfilled
Linear D Distance F Vel * Send signal to motor
DWELL 1 * Hold at each velocity for 1 second
ENDREPEAT

% Ramp down the velocity
REPEAT 20
Vel = Vel - Vel_inc
Distance = Vel*10 * Set so that this is never fulfilled
Linear D Distance F Vel * Send signal to motor
DWELL 1 * Hold at each velocity for 1 second
ENDREPEAT

% Stop controller
DISABLE
```

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