ABSTRACT

Title of Thesis:	EFFECT OF LONG-TERM AGING ON LEAD-FREE SOLDER AND SURFACE FINISH
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Since 2006, commercial electronics manufacturers have been banned from using lead-based materials and other toxic materials in their products due to the RoHS directive from the European Union. This led to industries transitioning to lead-free materials to be used in solder and surface finishes of their products. Although all of commercial electronics industry has transitioned to lead-free materials, some of the reliability and safety critical products used in industries such as defense, aerospace, automobile, and healthcare sectors are still exempted from the lead-free regulation. These industries are hesitant to transition to lead-free due to lack of data and hence the confidence on the long-term reliability of lead-free electronics. Known issues of tin whiskers and solder interconnect fatigue which can arise later in a products life have raised concerns related to the use of lead-free materials in electronic assemblies. To address these concerns, 10 year old lead-free systems were examined to determine the solder interconnect degradation level and tin whisker risk level.

EFFECT OF LONG-TERM AGING ON LEAD-FREE SOLDER (SAC405) AND SURFACE FINISH (PURE TIN)

by

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Dedication

This thesis is dedicated to my mother Mrs. Vijayashree Pandian who has constantly motivated me to let go off my inhibitions and fear and push myself to greater heights that she believes I am capable of. Her belief is my inspiration. I would also like to thank my father Mr. Pandian who gave me space and time to successfully reach my goals.

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Chapter 1: Introduction

Since the Restriction of Hazardous Substances (RoHS) regulations came into effect, lead which was an important alloying element in solders and surface finishes was banned from being used in electronic assemblies of certain applications. This study focuses on assessing the impact of long-term storage and usage on lead-free solders and surface finishes.

RoHS Regulation

In 2002, the European Union (EU) passed the Waste Electrical & Electronic Equipment (WEEE) directive to mandate the reuse, recycling, and recovery of electrical and electronic equipment waste that was being disposed of in European landfills. The goal was to reduce the release of hazardous substances into the environment. The WEEE directive required manufacturers to register their products and implement a plan to recycle in each EU country, and manufacturers were required to provide refurbishment, treatment, and reuse guidelines for each WEEE-compliant product.

Ten categories of electrical and electronic equipment were covered by the WEEE directive, including household appliances, information technology and telecommunications equipment, lighting equipment, electrical and electronic tools (with the exception of large-scale stationary industrial tools), toys, leisure and sports equipment, medical devices (with the exception of all implanted and infected products), monitoring and control instruments, and automatic dispensers. The WEEE

directive was applicable to all of the products falling into the 10 categories placed in the market after August 13, 2005.

Realizing that controlling the waste stream alone would not solve the issues associated with hazardous substances, efforts were made to restrict hazardous substances at their origins [1]. As a result, in 2003, the Restriction of Hazardous Substances (RoHS) directive limited the use of certain hazardous substances in electrical and electronic equipment in EU member states and provided a mechanism for restricting additional substances in the future [2]. The RoHS directive (2002/95/EC) became effective on July 1, 2006, and was applicable to the 10 categories of products listed in the WEEE directive, as well as to electric light bulbs and luminaires used in households.

Effective July 1, 2006, the Restriction of Hazardous Substances (RoHS) directive [3] legislated by the European Union (EU) banned the placement of electrical and electronic equipment containing lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyl (PBB), and polybrominated diphenyl ether (PBDE) flame retardants into the EU region. Of these substances, lead was the most prominent material used in the electronic packaging industry in the form of eutectic tin-lead in solder interconnects as finish coatings for leaded packages. The RoHS directive was updated in July 2011 as RoHS 2 [4], and although it did not restrict any additional materials, the directive provided deadlines for some exempted applications unless a technical reason was provided for continuing the exemption. In particular, the RoHS 2 directive required medical devices and monitoring and control instruments to comply with current RoHS restrictions by July 2014 and industrial control and

monitoring instruments to comply by July 2017. For all other equipment, unless explicitly excluded, compliance is required by July 2019.

In order to comply with the RoHS directive, most electronics part manufacturers have shifted to lead-free systems. Substitute alloys to Sn-Pb alloy were being tested even before the RoHS regulations came into effect. After years of testing across industry and academic research centers alternative tin-based alloys such as Sn-Ag, Sn-Ag-Cu, and Sn-Ag-Cu-Bi and other micro-alloys have been suggested to replace lead-based connections and coatings. Of all these possibilities, tin-silver-copper (SAC) alloy has been widely accepted as the most suitable replacement for eutectic tin-lead alloy [5]-[7] due to its mechanical, electrical, and metallurgical properties, which match closely with Sn-Pb alloy. Although most commercial electronics manufacturers have shifted to lead-free materials in their products, few sectors of products such as defense, aerospace, and automobile have largely stayed out of this transition. They have been either exempted or excluded from RoHS regulations due to reliability concerns with switching to lead-free materials [8]. The electrical and electronic equipment explicitly excluded were equipment used in military and space applications, large-scale stationary industrial tools, large-scale fixed installations, implantable medical devices, transportation applications (except for electric two-wheel vehicles), non-road mobile machinery, photovoltaic panels designed for permanent use, and equipment designed solely for the purpose of research and development [9]. The use of high melting temperature–type solders (i.e., lead-based alloys containing 85% or more lead by weight) remained exempt in the RoHS 2 directive for all applications. However, since all exemptions are bound to expire at

some point in the near future, the electronics industry will need to continually evaluate the options if the exemptions are to expire. Also, some of these manufacturers have been investigating, and in some cases using, lead-free parts because they are the only parts that are affordable and available on the market. For example, it is nearly impossible to purchase high-density ball grid array (BGA) packages in leaded versions [10]. These industries employ products that are expected to stay in operation for many years, sometimes under harsher conditions or in storage for many years before being deployed [11]. In addition, defense equipment manufacturers are procuring and storing components in bulk to counter problems of technology and part obsolescence [12]. Hence these reliability critical and risk-averse industries have been hesitant to make the transition to lead-free electronics due to lack of confidence on long-term reliability of lead-free electronics [13]. Hence, there is a need for studies on analyzing effects of long-term (≥10 years) aging on reliability and properties of lead-free systems and interconnects.

Literature Review

There have been several studies conducted to assess the reliability of lead-free solders under thermal cycling conditions, vibrations, and corrosive environment [14]-[28]. In additions, there have been studies conducted to assess properties of specifically SAC405 solder joints that are exposed to high temperature isothermal aging. Ma et al. [29] aged SAC405 solder samples that were reflowed and extracted from glass tubes at 125ºC for six months. The samples were subjected to tensile testing and after 200 hours the elastic modulus of solder decreased from 41 MPa to 30 GPa, while the ultimate tensile strength (UTS) dropped from 49 MPa to 28 MPa, and

the yield strength decreased from 35 MPa to 21 MPa. Venkatadri et al. [30] studied the effect of different temperatures 70 ºC, 100 ºC, and 125 ºC on the knoop hardness and microstructure evolution of SAC405 solder bumps. Knoop hardness reduced by 32% at the end of 3000 hours depending on the aging temperature. The Ag_3Sn and Cu_6Sn_5 IMC particle sizes were observed to increase at different rates. Hasnine et al. [31] studied the effect of aging on SAC solder bumps at 125 ºC. Single crystal solder bumps were prepared to conduct nanoindentation testing. Hardness and young's modulus were found to decrease considerably after few days of aging. Specifically, the hardness of SAC405 solders decreased from 0.32 GPa to 0.28 GPa. Grain orientation was found to influence the mechanical properties of solders.

Ma et al. [32] conducted room temperature (RT) aging for 63 days on water quenched and reflowed SAC405 samples extracted from glass tubes. When subjected to tensile loading, the properties were found to change at higher rate in the first few days of sample preparation. Water quenched samples were found to have higher variation in their properties after aging than the reflowed samples. The study found the elastic modulus to drop from 40.5 GPa to 37.9 GPa, and ultimate strength dropped from 46.8 MPa to 34.9 MPa for reflowed samples. The pure tin matrix area seemed to have increased while the Ag_3Sn IMCs coarsened and grew longer. Xiao et al. [33] conducted RT aging of cast Sn 3.9Ag0.6Cu alloy samples. After 35 days of aging the tensile strength of solder casts were found to reduce by 25% from 60MPa to 45 MPa. There were no change in Ag_3Sn particle size observed and the pure tin region was found to increase in area. In summary, all these studies report a drop in mechanical

properties that they measured after aging and have mainly attributed this to the IMC particle size coarsening over aging.

Tin whiskers remain a potential reliability risk especially in cases of pure tin finish on leaded packages and connectors. Moon et al. [34] showed that no whiskers were observed for pure electroplated bright tin deposited onto copper substrates after 2 months at ambient conditions. SOIC, SOT, TO-220, and QFN packages with matte tin finish over copper substrates were studied under biased and non-biased condition at 51℃-dry and 51 ℃-85% RH environment for 3000 hours [35]. No whiskers were found until 1000 hours under any condition. However, in the same study, whiskers initiated in some of the samples stored under ambient conditions after a period of nine months. Lin et al. [36] studied tin whiskers on samples with electroless deposited tin stripes ranging from 50 to 200 μm thickness. Some whiskers were formed in as little as 1 hour at 50 ℃ under a current density was 3.6×10^5 A/cm^2. When the current density was reduced to 4.5×10^4 A/cm^2, no whiskers were observed, even after hundreds of hours of current stressing. Many other studies have been conducted under differing stress conditions to understand the mechanism of tin whisker growth. However due to lack of consistency in results across studies, the concern for whiskers still prevail which makes its further research necessary.

Most of these studies have been conducted under accelerated conditions such as high temperature/high humidity conditions. The few studies conducted to understand the effect of ambient conditions have ranged from few days to few months of aging (exposure to conditions that causes degradation). In addition, the samples used to study the isothermal room temperature (RT) aging effect have been either cast or

extracted samples. None of these conditions are representative of a commercially assembled electronic assembly's lifecycle conditions. This study strives to fill this knowledge gap by analyzing lead-free solder joints, and tin finish leads on commercially produced printed circuit boards (PCBs) that have been used and stored for more than 10 years. This study provides us an opportunity to evaluate the effects of usage and storage in room temperature on lead-free electronic assemblies. Henceforth in this paper, RT aging and RT usage and storage will be used interchangeably. Nano-indentation was carried out to characterize the mechanical properties of solders that have been aged by measuring their hardness and elastic modulus. Microstructural analysis was conducted to study the particle size and particle quantity distribution of Ag_3Sn particles over Sn matrix. The microstructure changes along with creep testing results were analyzed to understand the effect of long-term room temperature usage on SAC405 solder joints Based on these results, a qualitative relationship between mechanical properties and the microstructure of the solders has been established. In addition, pure tin coated leads of integrated chips (ICs) on the board were inspected for growth of tin whiskers under RT conditions.

Chapter 2: System Level Reliability Analysis

As mentioned earlier commercial electronics such as computers were the first to switch to lead-free materials and hence they provide us a time line of >10 years that would help us analyze the impact of long-term storage and usage on their reliability. In addition, the computer motherboards can be considered to be representative of other electronic systems as they are made of different component types such as capacitors, resistors, inductors, and integrated chips (ICs) that are part of most electronics.

Lead-free Systems Information

First the seven lead-free computer systems were examined for system level reliability, of which six were manufactured and used from 2006/2007 and one was manufactured in 2007 and never used. These systems were considered as room temperature aged samples going through real-time loading—environment and operation—conditions. Figures 1a and 1b show the systems that were examined. As can be seen the used systems were completely assembled, and the stored system was a bare motherboard that had never been used or assembled with processors and Random-Access Memory (RAM) cards. Analysis of these systems were able to provide an understanding of the degradation modes and mechanisms that can be expected in used and unused lead-free systems that were stored idle in room temperature and humidity conditions.

J9NLCC1 6SJZS91 9RZKXC1

38NLCC1 JNX0YC1 No Service Code

(a)

(b)

Figure 1 (a) Used computers (with service tag) (b) Stored computer (bare motherboard)

The objective of this study was to evaluate the state of health of the lead-free computer systems. These results were compared with the estimates from literature failure models in the later section.

Used System Diagnosis

The computer systems were physically observed for any external defects and damages such as cracks, damages to the casing, CD drivers missing, not powering ON, noise and vibration felt around the casing, etc. The defects were observed and captured using digital camera and documented for possible correlation with other defects found at later stages of evaluation. Once the external hardware issues were documented, the computers were examined for functional soundness of both critical hardware parts such as processors, hard drives, audio cards, RAM, cooling fan, etc. and software operation. DELL computers have in-built sensors that can retrieve status of health (SOH) data for all the parts that are mentioned above. These sensor data were accessed using certain DELL Enhanced Pre-boot System Assessment (ePSA) diagnostic tool that can be run on the system while booting and retrieve information on necessary devices. This diagnosis returns attribute data on the health of the critical components of the system e.g., a system with a faulty hard drive returns failure message when the tool is applied on the hard drive of the system. The diagnosis also provided system temperature and fan speed data based on the availability of corresponding sensors in the system. All abnormal fluctuations and anomalous data were documented and used for system performance analysis. There were cases when the system did not power up, which then posed a challenge in using the tool as it is not possible to run diagnosis on those systems. These cases were compared with the

initial physical examination and find out if any missing components such as RAM or hard drive are causing these start-up issues. These system level state of health data were collected and documented against each system's service tag for future reference and comparison against other systems hardware and performance.

Stored System Diagnosis

The stored system was assembled with new processor and RAM to assess its basic functional integrity as they were never used or assembled during its lifecycle. The system motherboard had most of the critical components such as Northbridge, audio cards, video cards, etc. pre-assembled on them. Hence only the processor and RAM were the remaining components required to power up the system and operate them just like other used systems. The processor and RAM were selected based on the architecture of the motherboard. The board being an Optiplex 755 make, it required Intel Q6700 processor (shown in figure 3 (a)) with 2.66GHz core with 775 connector pads to match the board pins. The required RAM specification was 2GB 800MHz DDR2 (shown in figure 3 (b)). The challenge was to procure these components as these processors are outdated and are seldom used in the current computers. Hence, we had to dig into the legacy market/sellers selling these parts online. Once we got hold of the processor and RAM we needed a working computer which was compatible with the motherboard configuration we had. This enabled us to run the motherboard in the same condition, i.e. with usual fan cooling in an enclosed system, with other accessories such as hard drives, CD-drives operating simultaneously. This would enable us to have confidence over the functional evaluation of the stored

system, as against just powering up with no actual loading on the processor and RAM.

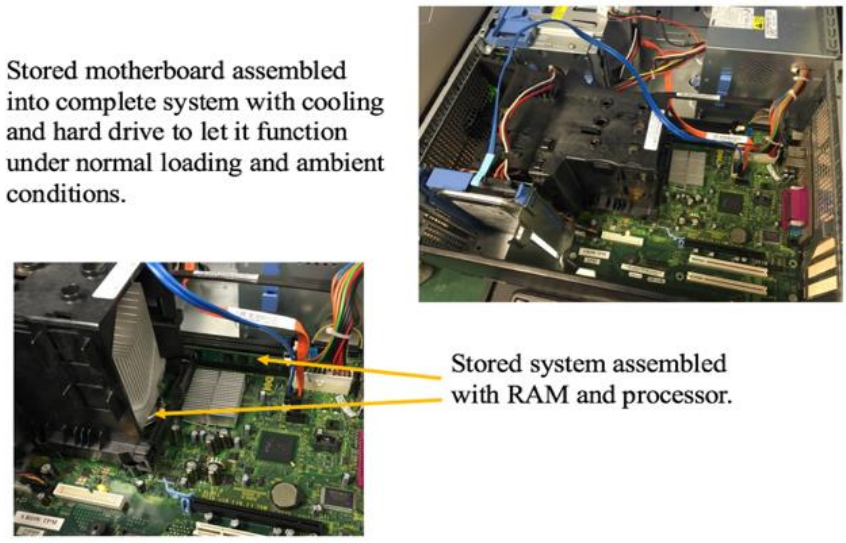


Figure 2 Stored Motherboard Testing

The motherboard of the computer whose auxiliary systems were used was replaced with our stored motherboard. Once the motherboard was replaced, the processor and RAM were assembled on to the stored motherboard (shown in figure 4). The thermal grease was applied over the casing of the processor to provide a smooth thermal transient connection between the processor and the cooler. The cooler also acts as mechanical constraint for tight fit between processor pads and mating pins. Once the assembly was secured the system was powered ON. The system was connected to monitor and the operating system booted without any issues. We were able to browse through the system and perform normal computations without any notable lag or malfunction. This provided a good indication of the functional integrity of the stored system.

Diagnosis of Intermittent Functionality of a Used System

One of the used systems with service id J9NLCC1 did not power ON initially. When the power was supplied it emitted a rhythmic beep sound. It was a periodic four beeps followed by a pause and was accompanied by fan rotating with high sound. When researched into DELL database it was found that these sounds relate to RAM failure. Hence the RAMs of this system were replaced by the new RAM that was installed in the stored system. Once replaced the used system powered ON and booted normally. This confirmed that the issue lied with either RAM cards or RAM slots. To identify where exactly the problem lies, the RAMs that were originally installed in the used system was assembled in another healthy used system. When the healthy used system was powered ON with the J9NLCC1 RAM it booted up normally and didn't exhibit any issues in the functionality. This confirmed the fault site to be located in the RAM slots. After multiple iterations of assembly and removal of RAMs in the faulty used system it was deduced that the system powered ON even with the originally installed RAM, which indicated the presence of an intermittent failure.

Summary of System Level Testing

The seven lead-free computer systems, both stored and used, were subjected to non-destructive analysis. The systems were diagnosed using DELL ePSA diagnostic software to determine the current state of health of the overall system and critical parts such as processor, RAM, hard-drive and other audio-video cards. The stored system was assembled with new processor and RAM to boot it up and examine its health. The diagnosis showed that all the systems, except one used system, were defect free and exhibited healthy functionality in all computational tasks. One system,

which did not boot up was found to have intermittent contact failure between RAM cards and their slot interconnects. However even that system started functioning once the RAM card was pulled out and connected back. Overall, all lead-free computer systems were working fine as intended.

Chapter 3: Solder Reliability FEA Analysis

CalcePWA is a module of CalceSARA (Simulation Assisted Reliability Assessment) software which assesses reliability of interconnects based on physics of failure models. CalcePWA was used to run the reliability analysis on the CAD model of the board to compare our physical inspection results with thermal fatigue model estimations. The solder material (SAC), component standoff height, thickness and number of layers in the board, and 104 components from the board such as surface mount capacitors, inductors, BGA, and QFPs were modeled to make the simulation CAD representative of the actual board. Time to failure of lead-free solder joints under temperature cycling was estimated to see if the reliability model estimates agree with the real-time inspection findings. The simulation was run for room temperature condition (20-30°C) with the dwell time at maximum (30°C) and minimum temperature (20°C) set at 480 minutes while the ramp time set at 240 mins so that the temperature range is set to undergo one cycle per day.

CalcePWA Software Modeling

The CalcePWA software consists of a set of simulation tools that use various thermo-mechanical stress and damage models. Using information on materials, hardware configurations, and expected life cycle loads, CalcePWA simulation can help in:

- Checking whether the boards will pass qualification
- Estimating operational lifetime
- Ranking potential failure mechanisms

- Identifying weak links in assembly design

Design Capture

Design capture is the first step in the virtual qualification process. The goal of this step is to identify and document part and board architecture, material properties, and the expected life cycle loads. In this step the details including physical dimensions, functionality, and constitutive elements (e.g., material properties) of the board and all the components on the board are gathered. Sources of data typically include a bill of materials, manufacturers' data books, part drawings, and board layout CAD files. The PoF methodology requires that all the intrinsic material properties be identified and documented. This includes part information (e.g., substrate material, encapsulants, underfills, leads, and platings), interconnects (e.g., solder composition, conductive adhesives, socket materials), and the makeup of the printed wiring board (e.g., resin system, plating, embedded passives). The properties of the identified materials are then retrieved from the CALCE Materials Database or looked up from references and used for stress modeling.

Life Cycle Loading Characterization

The definition and characterization of the product life cycle environment is often an uncertain aspect of the reliability prediction process. A product's life cycle environment should be characterized in order to describe the severity and the duration of the loading conditions during the non-operational (storage, transport, testing) and the operational conditions of the product. Life cycle loading characterization is carried out to identify and record the operational environments of the product.

Examples of environmental loads needed for life cycle loading characteristics include temperature limits, average temperature, frequency of temperature cycles, mechanical vibration, and electrical loads. The level of these experienced loads should be accompanied with details of rate of change and duration of exposure. Loads experienced by parts during non-operating phases such as assembly, transportation, storage, handling, and rework should be taken into account. Life cycle loads can be obtained based upon interviews with the manufacturer, interviews with the end-user, and the use of sensors placed on the part during operation, or using CALCE's prior experience with similar environments.

Load Transformation

Thermo-mechanical stresses and deformation are the major contributors to interconnect failures. Thermal stresses are usually associated with mechanical (structural) failures (e.g., ductile rupture, brittle fracture, creep, stress relaxation, thermal shock, stress, and corrosion). The load transformation step takes environment and architecture as input and produces the stress fields (e.g., temperature, displacement, and curvature).

Failure Risk Assessment

Failure can occur due to elastic deformation, especially of a slender structure due to overstress. Stresses such as fatigue cause damage in the materials that accumulates irreversibly and causes the product to fail when the damage exceeds the endurance. Accumulated damage does not disappear when the stresses are removed. The failure risk assessment process is accomplished using a failure model consisting of a stress

model and a damage model. Stress models correlate the environmental and operational loads, package architecture, and material properties to stress, strain, and energy distributions within the interconnects. The result of the stress models is a strain hysteresis loop. The energy partitioning model then assumes that the damage to the interconnect over one thermal/vibration cycle is equal to the work dissipated in one hysteresis loop. The damage model roughly determines the number of cycles to failure. In the damage assessment step, the damage for each part is defined in terms of a damage ratio (DR), which, for thermal cycling simulation, is the ratio of the number of cycles applied to the number of cycles (or other equivalent units) it can survive. The times of failure reported represent an estimate of time to 50% failure.

Ranking Potential Failure under Life Cycle Loads and Accelerated Test Plan

CalcePWA gives the potential failure of the components in terms of the damage ratio. The damage ratio is defined as the ratio of the number of cycles experienced to the number of cycles to failure. The components are ranked in decreasing order of damage ratios. The various damage assessment models as applied to individual parts are also listed in the results.

Solder Joint Thermal Fatigue Models

Engelmaier developed the semi-empirical solder joint fatigue model, commonly known as the Engelmaier model, in the early 1980s [37]. The model was given as

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f'}\right)^{\left(\frac{1}{c}\right)} \quad \ldots\ldots\ldots \quad (1)$$

In CalcePWA, the results are reported as damage ratios:

$$D_i = \frac{N_i^{applied}}{N_i^{available}} \quad \text{…….. (2)}$$

where the applied cycles to failure are the cycles specified by the standard, and available cycles to failure are the cycles from the simulation results. Damage ratios are calculated based on Miner's rule which states that if there are k different stress levels and the average number of cycles to failure at the ith stress is N_i, then the damage fraction, D_{total} [38], is:

$$D_{total} = \sum_i \frac{N_i^{applied}}{N_i^{available}} \quad \text{……. (3)}$$

D_{total} >= 1 means damage has produced a failure at the site.

Simulation

The computer board that was modeled for simulation is shown in Figure 3. Not all the components on the real board were modeled for the simulation. However, all the component types such as QFP, through hole connectors, surface mount capacitors, ball grid arrays (BGAs) were included in the model. Power dissipation values of components were provided based on datasheets and knowledge gained from past projects. The three highest power dissipating components were identified to be processor (95W), Northbridge-BGA (10W), and Southbridge-BGA (3.8W). Other components such as capacitors, resistors, and ICs and inductors were provided a value of 0.00018W, 0.0019W, and 0.0114W respectively. Type of thermal management system modeled has a significant impact on the final simulation results. As the heat generated in the computer boards are cooled by fan provided in the systems, forced air cooling mode was selected from the simulation. Air speed of 0.76m/s was

provided based on the thermal design specification of the computers. The final simulated board model is shown in

Figure 4. Other important parameters that were used for modeling were got from physical inspection of cross-sections of board. These parameters include:

- Thickness of the board: 1.5mm
- Number of layers: 7
- Solder thickness: 0.06mm
- Solder type: SAC405

Table 1 Temperature Profile used in simulation

Ambient Temperature range	Dwell Time at max and min temp. (mins)	Ramp time (mins)	No. of cycles
20 to 30°C	480	240	3650

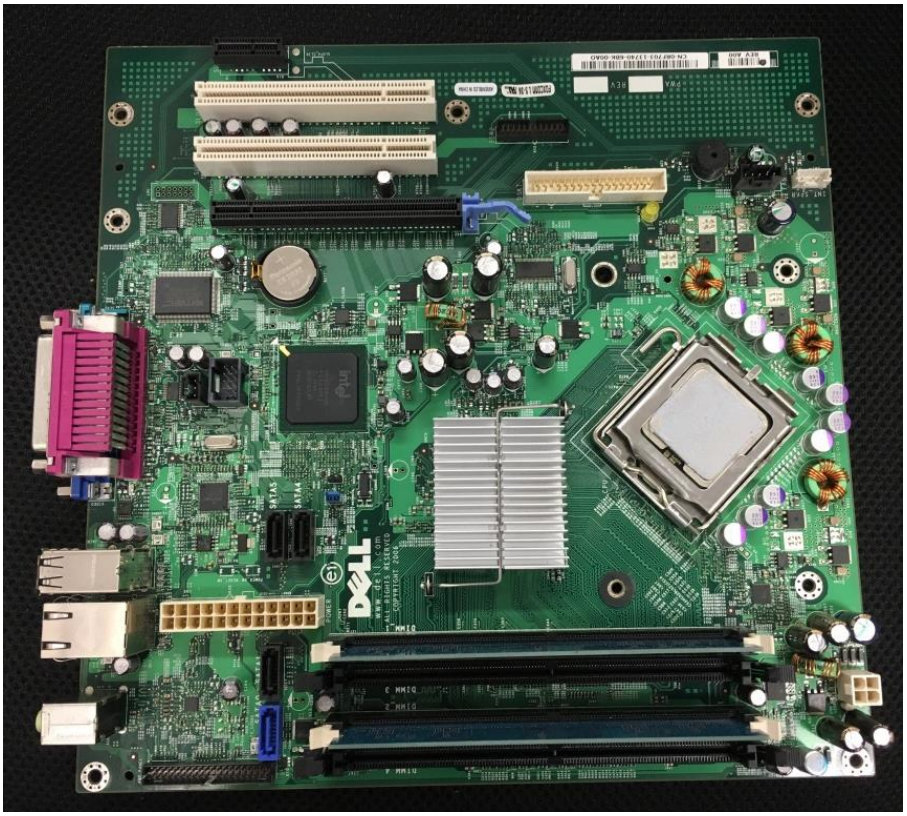


Figure 3 Board that was modeled

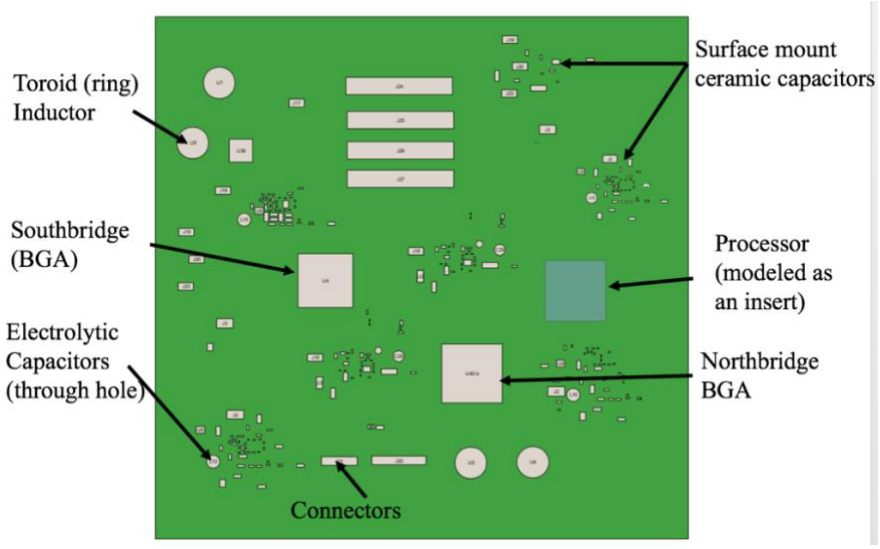


Figure 4 CalcePWA Simulation Model of the Board with Components

The CalcePWA analysis results indicate that the lead-free solder joints survived both the RT conditions for a period of ten years. The simulation result agrees with our system level evaluation, where the computer boards have not failed after being used and stored in RT for 10 years. The simulation results showed that the solder joints of Northbridge BGAs had the highest damage ratio (DR). The 0603 ceramic capacitors that were placed close to Northbridge were found to have the second highest DR. Physical examination of solder joints also showed no signs of degradation such as cracks or voids which matches with the low damage ratio accumulated in the simulation as shown in Table 2.

Table 2 Simulation Results Showing the Components with Top Two Highest DR

Component Type	Damage Ratio (DR)
Northbridge BGA	0.29
Ceramic capacitor (0603)	0.04

Chapter 4: Solder Joint Property Characterization

Since the board level reliability indicated no failures and did not show any degradation signatures, further analysis was conducted to characterize the solder joint mechanical properties and microstructure. Properties of solder can give insight into the evolution of solder material's resistance to certain loading conditions which could be then corroborated with microstructure evolution.

Mechanical Property Evaluation

For new lead-free assemblies, test boards with SAC405 solder and immersion Ag surface finish were designed and assembled in collaboration with Captron Corporation. Solder joints of surface mount ceramic capacitors were used for analysis of aging. Three capacitors were cut out from two aged boards while three capacitors were cut out, one each from one new board, for testing and microstructural analysis. The capacitors were ground along their length to expose the solder joint fillets on either side of the capacitors as shown in Figure 5. The sectioned sample was potted using acrylic and the potted sample was ground and polished using silicon carbide grit papers and diamond suspensions respectively. This provides us with six solder joint samples in both aged and new boards) to measure properties from. The results obtained from solder joints of aged boards were compared with that of new boards to quantify the effect of long-term aging on the microstructure and mechanical strength of solders.

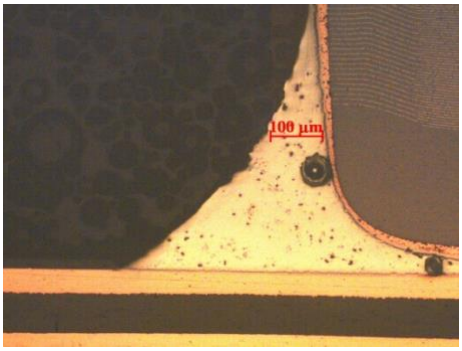


Figure 5 Cross section of 10 years aged solder joint fillet under optical microscope

Nanoindentation

Nanoindentation is a type of indentation tests used to characterize mechanical properties of materials at small scale. Solder joints were subjected to nanoindentation to measure their hardness and young's modulus. The indentation was carried out using Berkovich indenter to a depth of 1000 nm and at a strain rate of 0.05 s-1 on solder joint fillets on both sides of capacitor as shown in Figure 6. The nanoindentation measurements of aged solder are shown in Figure 7 and Figure 8. Figure 7 show the average modulus and hardness values with one standard deviation error bar of 40 indentations over six solder joints in aged solder joint while the Figure 8 shows the average values with one standard deviation error bar.

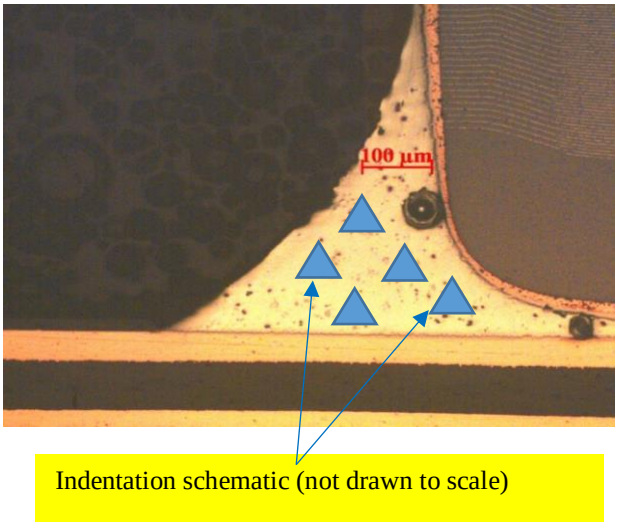


Figure 6 Indentation schematic on solder joint fillet

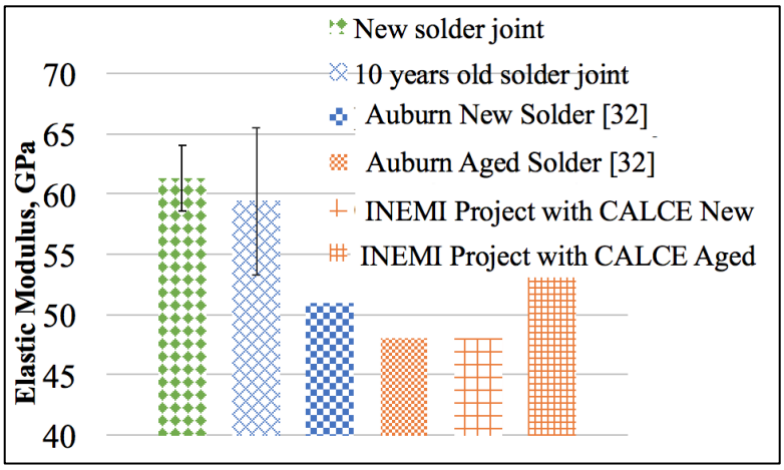


Figure 7 Elastic Modulus of solder joints from our testing and literature reports

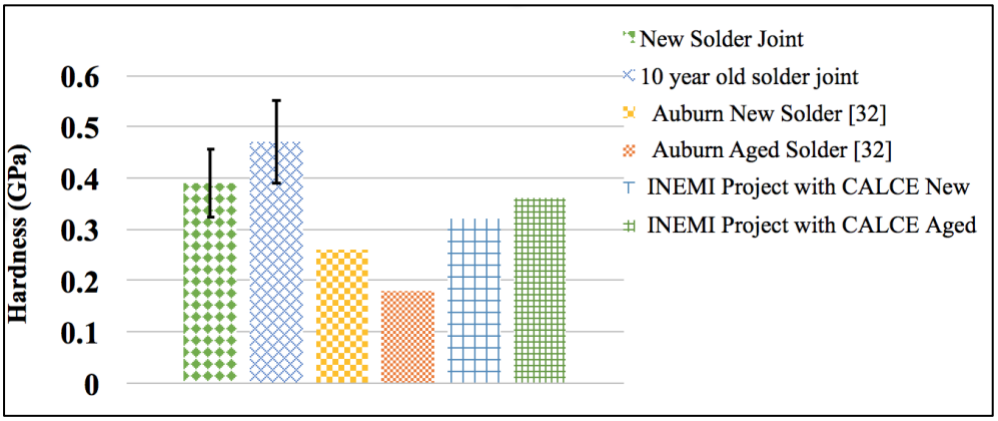


Figure 8 Hardness of solder joints from our testing and literature reports

The hardness and modulus are higher than typical values (40-50 GPa) reported in literature [31]. This could be due to the difference in the type of sample tested. Our study testing solder joint fillet, could have more grains than a solder bump which will result in constituting the effect of grain boundaries thereby increasing the overall modulus and hardness measured. In terms of aging effect, we find the modulus of SAC405 solder joint to decrease from 61 GPa to 59 GPa after ten years of aging. It is seen from the error bar that this drop may not necessarily indicate a change in modulus as it could be only a variation induced by measurement procedure. On the other hand, hardness was found to increase from 0.39 to 0.47 GPa which is similar in magnitude to the change reported in literature but is observed in the opposite direction. Hasnine et al. reported a decrease in hardness by 0.08 GPa after isothermal aging at 125 °C.

Creep Testing

As discussed in the previous section the hardness of the 10 year RT aged (power cycled) solder joint was found to have increased. This is contrary to the literature

findings at elevated temperature aging. Hence creep test was conducted to identify if there has been work hardening that led to increase in hardness of the solder joint. The solder joint was subjected to nanoindentation at constant load to observe the creep property. 10mN constant load was applied on the solder joint for a period of 40 seconds. The average creep displacement curves of 10 indentations each on new and aged solder joint are shown in Figure 9. It is clear that the aged solder joint has creeped lesser than the new solder joint which agrees with the hardness measurements. The creep is calculated based on following equation:

$$C = \frac{h_2 - h_1}{h_1} 100$$

where h_1 and h_2 are the indentation depths/displacement at time t_1 and t_2; t_1 is the time at which the 10mN load is reached and t_2 is any time in the test after t_1. In our testing, the t_1 was 13 seconds and t_2 was taken to be 30 seconds. The average creep of aged solder joint and new solder joint was found to be 0.094 and 0.091.

The aged solder joint being harder than the new solder joint resists the deformation under indentation and hence shows lower displacement as compared to new solder joints. The creep data ascertains the presence of work/cyclic hardening effect on the solder joints. The hardening occurs due to initiation of multiple dislocation points over ten years of aging due to power cycling undergone by the solder joints. These dislocations points trap each other and prevent their relative motion leading to increase in hardness.

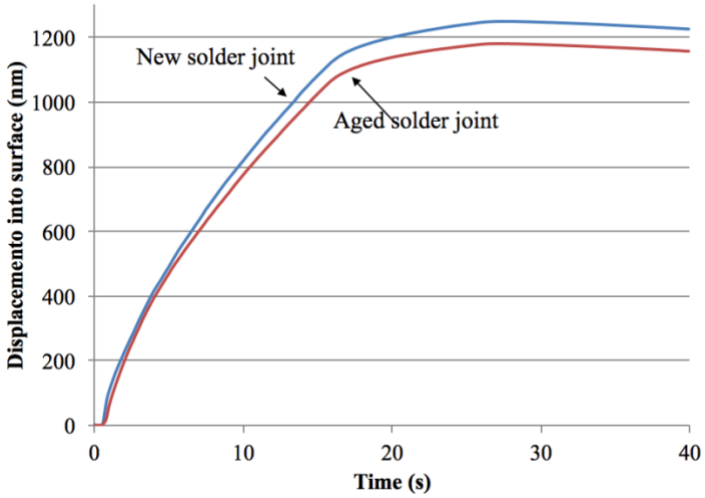


Figure 9 Creep displacement of SAC405 solder joint under 10mN load

Microstructure Analysis

Microstructure of solder joints were analyzed before being subjected to nanoindentation. The bulk solder, away from the interfacial IMCs, were used for this microstructure analysis. The change in size and number of particles of secondary Ag_3Sn particles in the bulk solder have been reported to have impact on mechanical properties of solder. As explained in the introduction section, increase or decrease in hardness is related to finer dispersed or coarsened larger Ag_3Sn particles respectively. The solder joints were inspected under ESEM to analyze Ag_3Sn IMC particle size and quantity. This analysis was conducted to investigate if the Ag_3Sn size evolution agrees with the hardness measurement. Images of six solder joints, one from solder joint on each side of three capacitors were used to analyze the IMC particles.

Quantitative Analysis of IMC particle size

The quantitative analysis of IMC particles was performed using image analysis software ImageJ. High quality ESEM images were taken up for analysis using

ImageJ. Once the ESEM image was imported into the ImageJ tool, the image was calibrated to change the measurement units from pixel to micrometer. For calibration, the image was zoomed into the scale on the bottom right corner of the ESEM image. Then a line was drawn on top of the scale line provided and its length is measured in pixels. Then using the set scale option, the default scale is removed and the measured length in pixels is converted to the value mentioned in the scale of the ESEM image. Once the scale is set, the picture size will change from being displayed in pixels to micrometer. This assures that the calibration has been completed. If all the images are captured under the same magnification, then there is an option called "Global" that can be checked to carry forward the same calibration scale to next images.

Once the calibration is completed, then the image is smoothened to filter the pixels that are not IMC particles. This can be done using multiple filter techniques in-built in the software such as Fast Fourier transformation (FFT) filer and bandpass filter. In our analysis, we used bandpass filter where 20 pixels were smoothened to 3 pixels. When this is done, a change in image quality can be noted as the image appears smoother than previously it had. Then, the smoothened ESEM image of solder joint microstructure was converted to binary image where Ag_3Sn were made black while rest of the image was made white. However, it is important to play with the thresholding option to improve the differentiation between Ag_3Sn particles and rest of the image. After multiple trials, a threshold setting of 99-255 was adopted for further analysis. This setting was carried over to all images later to keep the processing constant and making the comparison between aged and new solder joints fairer. The black Ag_3Sn particles were approximated as circles by the software and

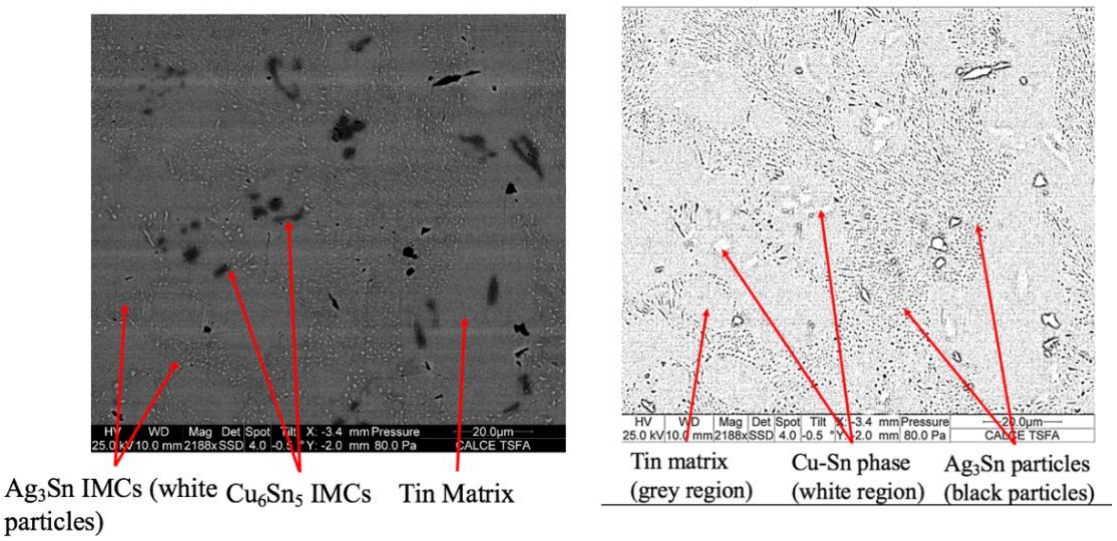
the circles' area (IMC particle size) were output by the particle analyzer. However, the size of pixels where measured initially by zooming in closer and using drawing tool to measure area of pixels which are also in black color. After multiple measurements, it was deduced that the pixels had an average size of 0.15 microns and hence all particles under the size of 0.15 were omitted from the output.

The ESEM image and the corresponding binary image of solder joints are shown in Figure 10 and Figure 11. The results of particle analyzer are shown in Figure 12. The overall distribution did not show any difference between aged and new solder joint. The lack of coarsening could have been due to relatively benign (office) environment the computers were used in. This is not uncommon as SAC405 solders have shown to maintain their IMC particle size and resisted coarsening under temperature cycling [39] [40]. It was reported that the IMC particles in SAC alloys with higher silver content such as SAC405 do not move enough to coalesce and grow in size as compared to low Ag alloys such as SAC105 and SAC205.

To get further confidence on the difference or indifference in the distributions quantitatively, t-test was conducted. Null hypothesis is that there is no effect of aging on the IMC particle size and the alternate hypothesis is that aging has caused significant evolution of IMC particles. The p-value which is a measure of similarity/dissimilarity of the distributions should be <0.05 to reject the null hypothesis. However, for the t-test to be applicable to two distributions, they should have similar variance. This is confirmed by conducted a f-test where the null hypothesis is that the two distributions have same variance and the alternate hypothesis is that the two distributions do not have same variance. The null

hypothesis is rejected if the p-value of f-test is less than 0.05. The f-test was conducted for our distributions and the p-value was found to be 0.1. This confirmed the null hypothesis thereby ascertaining that both distributions have same variance/standard deviation.

Following the f-test, the t-test was conducted and it yielded a p value of 0.4. Since it is more than 0.05 we accept the null hypothesis and ascertain that the aging did not change the microstructure. This finding differs from the literature reports where the Ag_3Sn particles have been observed to increase in size after aging at elevated temperatures.



(a) (b)

Figure 10 (a) ESEM image and (b) Binary image of 10-year-old solder joint

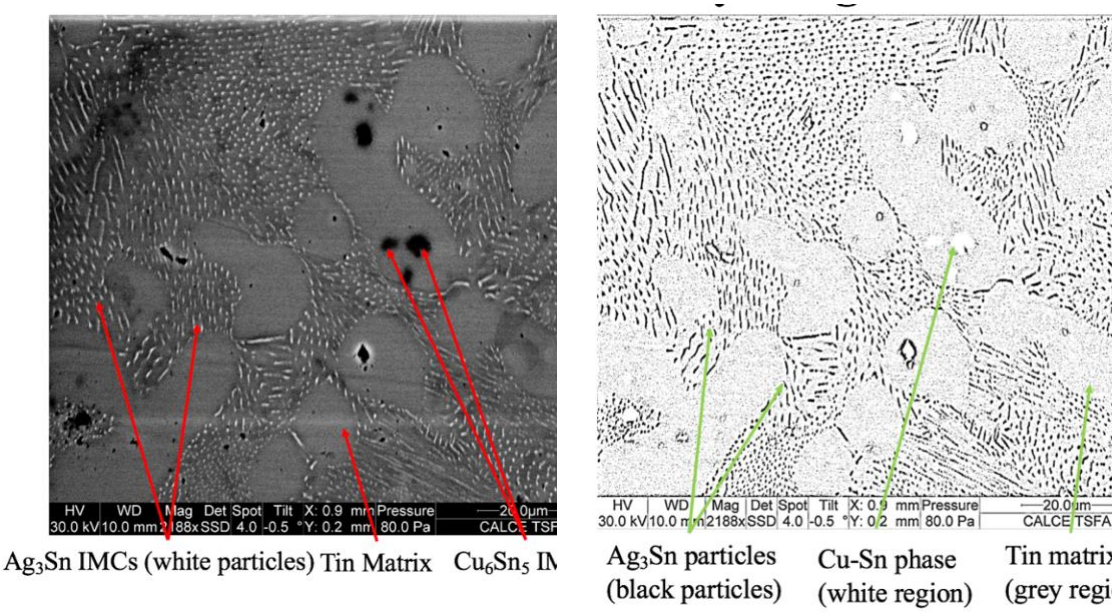


Figure 11 (a) ESEM image and (b) Binary image of new solder joint

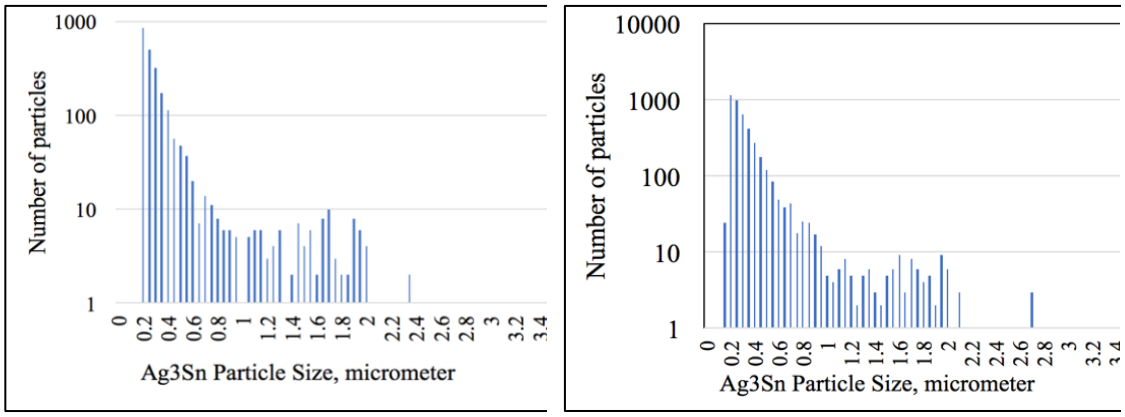


Figure 12 Ag_3Sn IMC particle size distribution of (a) aged and (b) new solder joints

Interfacial IMC Thickness Measurement

Interfacial IMCs have a significant impact on the life of the solder joints as their brittle property causes crack initiation and propagation through them under high strain rate loads. It should be noted that the interfacial IMCs refer to the intermetallic formed during the reflow process between the copper pad and solder to form the assembly. This is different from the bulk solder IMCs that were discussed previously. Interfacial IMCs of SAC/Cu solder-pad assembly are generally comprised of Cu_3Sn and Cu_6Sn_5 and grow in thickness over time. Due to the brittle nature of these IMCs, lower IMC thickness are generally preferred. Interfacial IMC thickness was measured in new and aged solder joints to characterize the effect of room temperature usage on solder joints. Interfacial IMCs of three solder joints each from new and aged boards were measured and compared. As shown in figure, the IMC thickness of new and aged solder joint were found to be 2.5 and 5 µm respectively. This shows that the solder joint's vulnerability to drop loads increases with aging time.

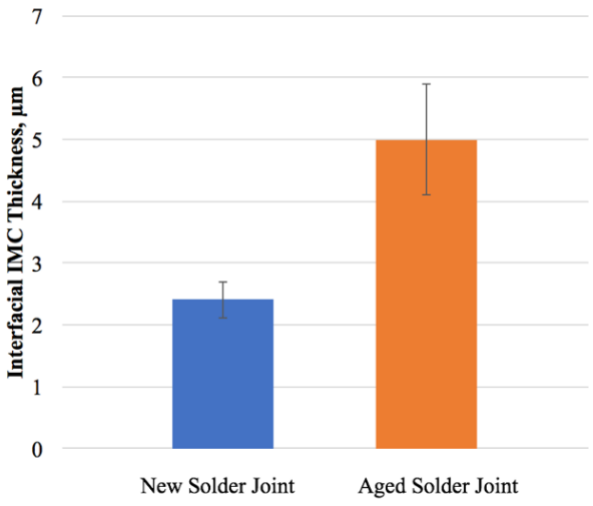


Figure 13 Interfacial IMC Thickness Change

Chapter 5: Tin Whisker

Tin whiskers remain a potential reliability risk, especially for tin-finished products. Tin whiskers are filamentary growths that spontaneously grow from electroplated tin surfaces. Whisker growth starts after an incubation period that varies from seconds to years. Tin whiskers present risks for electrical shorting, metal vapor arcing, and mechanical obstruction failure.

Inspected Samples Information

Leads of ICs (integrated chips) and electrical connectors were studied to identify the effect of room temperature usage on tin whisker formation. The ICs were cross-sectioned to reveal the lead finish and lead material itself. This was performed to confirm the lead finish material, the underlying lead material which helps to characterize their whisker propensity. The cross-sectioned components with leads were taken up for analysis under ESEM-EDS to identify the materials. The EDS showed spectrum of tin when the thin finish material was scanned using EDS, while the lead material itself was confirmed to be copper.

Tin Whisker Inspection

These components before being cross-sectioned were subjected to tin whisker inspection. As per JEDEC Standard 22-A121A, minimum total area of inspection is to be 75 mm^2, and a minimum of 18 leads should be inspected with at least 1.7 mm^2 of area inspected in each lead. In this study, two quad flat packages (QFP) with a total of 126 gull wing type leads and two electrical connectors from one used motherboard were inspected which constitutes an area of over 100 mm^2. The leads were studied

using optical microscope and ESEM/EDS (environmental scanning electron microscopy/energy dispersive spectroscopy) to detect the presence of whiskers.

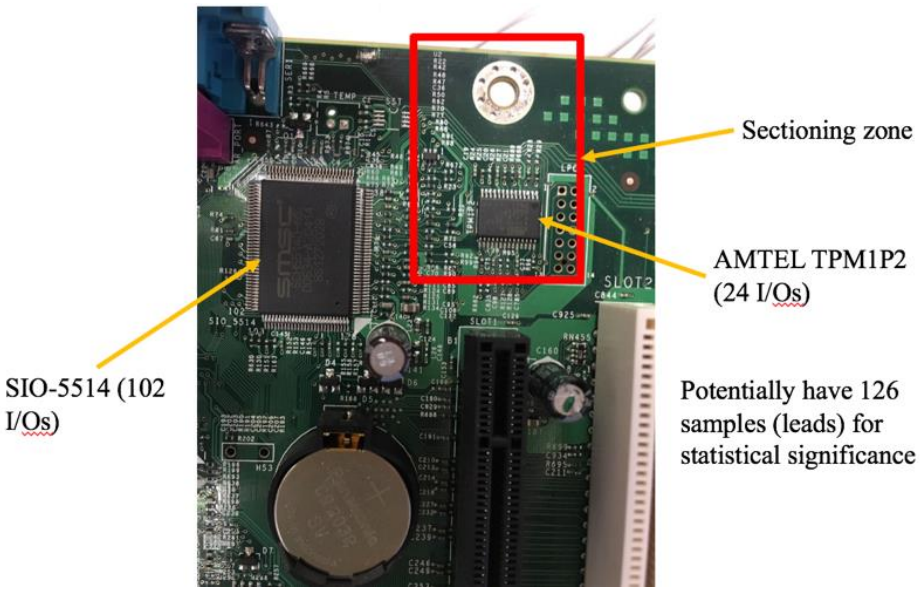
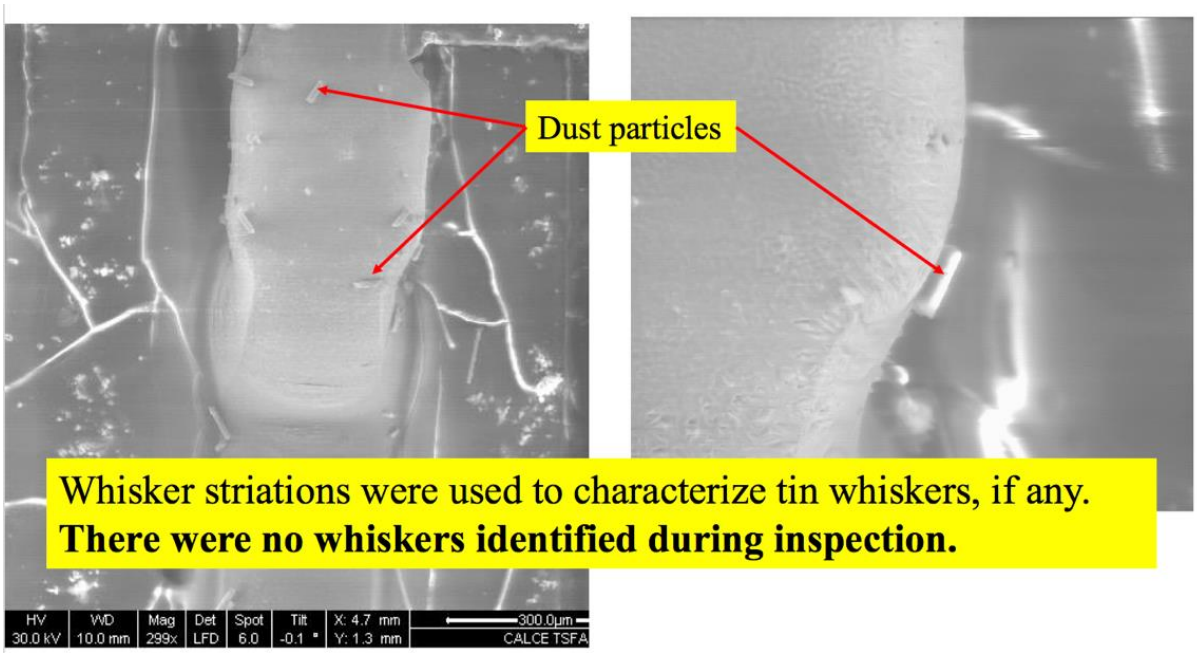


Figure 14 Components inspected for tin whiskers

ESEM images of the lead in Figure 15 (a) and (b) show thin forms over the lead. These were categorized to be not tin whiskers specifically due to the absence of striated patterns that is typical of whiskers. EDS analysis was conducted further to ascertain the presence or absence of whiskers. 85 mm^2 of area was inspected across two leaded components and an additional 40 mm^2 of area was inspected across the two connectors and no whiskers were found through ESEM inspection and EDS analysis.



(a) (b)

Figure 15 (a) ESEM Image at 300X magnification (b) ESEM Image at 1000X

Figure 16 ESEM Image of Connectors

Whisker Risk Estimation

To compare our finding with historical tin whisker growth characteristics, failure probability due to tin whisker shorting was estimated using calceWhiskerRiskCalculator. The probability is computed based on whisker growth characteristics (length and distribution) collected from past experiments and results. The lead spacing, number of leads, and finish material are the inputs to risk analysis. The parameters were collected from datasheets of parts that were inspected.

The following assumptions are made in the CALCE tin whisker risk calculator:

- Full surface area of a conductor is considered.
- Bridging spans shortest distance between conductors.
- Whisker growth can be extrapolated from measured data.

Failure occurs when $l_w \geq l_s$, where l_w is the length of a whisker and l_s is the spacing between the two adjacent conductors. Because whiskers have been observed to change orientation, the growth angle is no longer considered.

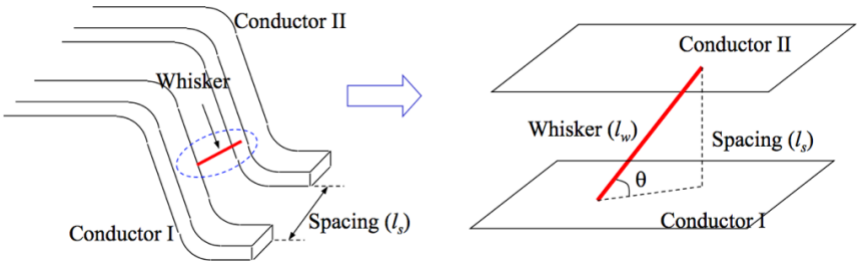


Figure 17 Lead-spacing and Tin-whisker Length

CALCE has measured whisker growth characteristics (length and density distributions) for matte tin over copper and bright tin over brass coupons. Whisker length distributions after 4 years (48 months) were found to follow log normal distributions. The growth rates are estimated based on past and current growth measurement. A potential failure site is defined by the area of tin which can form tin whiskers, the gap length which a whisker must cross to create a short, the growth characteristic of the tin finish, and the percent of the containment offered by an insulating barrier material such a conformal coat. The number of pairs is used to determine the failure probability for a set of same-type failure sites.

Figure 18 shows the distribution of whisker length collected by CALCE for tin coating on copper base and tin coating on brass base. The results from the CALCE Tin Whisker Risk Calculator are provided for each defined failure site in the defined system. For each site, the maximum simulated whisker length is provided along with the probability of failure for the failure site. At the bottom, the system reliability is presented.

$$F_s = 1 - (1 - F_i)^n$$

F_s - site unreliability for n pairs at a single pair unreliability of F_i

$$F_{sys} = 1 - \Pi_i(1 - F_{si})$$

F_{sys} - System unreliability

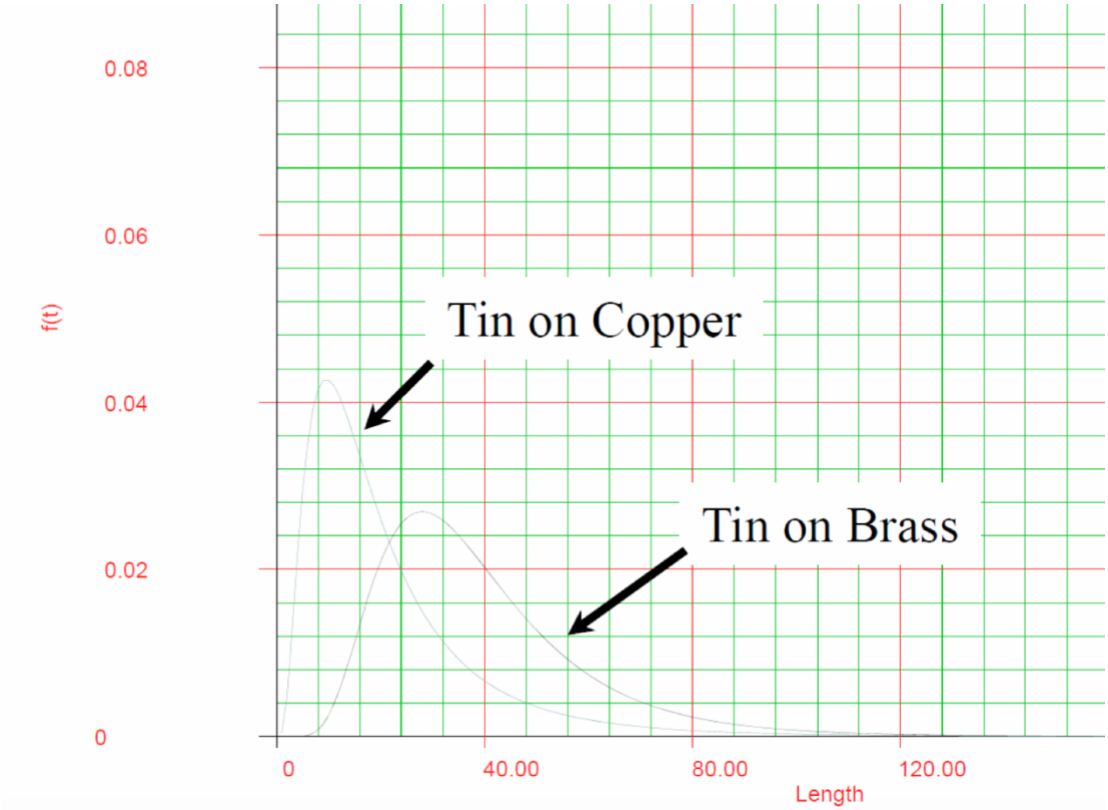


Figure 18 Whisker Growth Distribution

Whisker Risk Simulation Conditions

For our simulation, we considered the finish of leads to be pure tin over copper. The estimator generates a Monte Carlo simulation of different lengths of tin whisker and matches them with lead spacing. Based on the number of iterations we enter in the beginning the number of random length are taken from which the instances which crosses the lead-spacing and forms a short are captured and corresponding probability is calculated. The whisker risk calculator was simulated for 10 years of expected life with pure tin finish and without conformal coating. The longest whisker estimated by the calculator was 0.53mm and the shortest whisker was found to be 0.31mm which is different from our observation where we didn't find any whiskers.

Table 3 CalceWhiskerRiskCalculator Result

S.No.	Number of conductor pairs	Spacing between leads (mm)	Area (mm^2)	Longest Whisker (mm)
1	22	0.41	1.56	0.42
2	124	0.48	3.56	0.53
3	40	0.3	1	0.31
4	60	0.2	0.8	0.39

Chapter 6: Conclusions

Base on the testing conducted on solder joints and investigation performed on the surface finish of leads and interconnects, following are the key points obtained from this study.

Mechanical Properties of Solder Joint

This is one of the first articles to study the effect of long-term (>10 years) room temperature (RT) aging on fully assembled lead-free electronic assemblies over ten years. The effect of RT aging on mechanical properties including hardness and elastic modulus of SAC405 solder joints were characterized. Although modulus dropped by 2GPa, it is not considered significant drop as it is within one standard deviation of the measurement variation. This result is different from the elevated temperature aging results reported in literature as the modulus is expected to drop more as the temperature increases. The change in modulus is attributed to the atomic distance and so the modulus decreases as the atomic distance increases at high temperatures. As our samples have been only exposed to room temperature usage the atomic distance is not expected to have increased enough to cause a significant drop in modulus.

On the other hand, the hardness was found to increase by 20% from 0.39 GPa to 0.47 GPa after 10 years of aging. This again is opposite of what has been reported in literature under elevated temperature aging conditions. The increase in hardness agrees with the creep test results of the solder joints where the aged solder joint creeped lesser than the new solder joint. This is an indication of the presence of work hardening in the solder joints due to continuous power cycling over the ten years of usage.

Microstructure of Solder Joint

Microstructure analysis of the solder joints revealed that the IMC particles had not increased in size significantly. This shows that the Ag_3Sn particles in SAC405 solder do not move enough under RT usage to cause coarsening thereby decrease hardness.

Tin Whiskers

Tin whisker inspection showed no signs of tin whiskers which was backed by the estimates of calceWhiskerRiskCalculator simulation. The inspection results and analysis conclusions show that the long-term room temperature aged solder joints which were power cycled during the computer's usage are reliable and did not fail. These findings provide considerable confidence on the reliability of SAC soldered electronic assemblies which are to be stored or used for many number of years in controlled environment conditions.

From all the analysis conducted at system level and interconnect level, it is evident that lead-free systems do not possess serious reliability concerns under room temperature storage and usage. However, it is important to assess the risk and reliability concerns for new products based on each components materials and feature sizes such as lead spacing, solder ball diameter, and electrical parameters.

Chapter 7: Contributions

This is the first study to analyze the reliability and degradation of commercial produced lead-free electronic assembly. The contributions from the study are summarized below:

Mechanical Properties of Lead-free Solder

Determined the mechanical properties of 10 years room temperature aged SAC405 solder joint.

- Hardness and modulus of SAC405 solder joints were measured using nanoindentation
- Identified the hardness increases after room temperature aging (usage/power cycling) unlike has been reported in literature where the hardness decreases after aging

Microstructure of SAC405 Solder Joint

Evaluated the change in size of Ag_3Sn IMC particles in bulk SAC405 solder joint after 10 years of aging

- Found that the IMC particle size did not change in size after 10 years of aging which is contrary to literature findings where the elevated temperature aging has been found to increase the IMC size

In addition to the above findings, certain additional analysis could be conducted to further explore the effects of long-term aging. Work/cyclic hardening has been postulated as the reason for increase in hardness observed after aging. To confirm the hypothesis, further analysis could be conducted to investigate for presence of

dislocation zones on the bulk solder. For this, a sample of solder could be taken up for transmission electron microscope (TEM) analysis where the solder material could be observed at nano level to look for dislocation regions.

Also, crystallographic study could be conducted to understand the effect of grain orientation on the hardness measurements. The solder joints can be taken up for observation under electron backscatter diffraction (EBSD) analysis to evaluate grain orientations using which the hardness measurements can be normalized to single reference plane direction. This will help in eliminating the effect of harder planes and help identify if grain directions had an impact on the hardness of the solder joints.

Further investigation could be conducted on BGA components of the board to see the effect of higher power dissipations on solder joints. It would reveal if these components underwent higher degradation and show any reduction in strength (modulus and hardness) as they are exposed to higher temperatures than solder joints.

Appendices

Appendix A: Interfacial IMC Measurement

The interfacial IMC thickness was measured using a combination of ESEM and ImageJ image processing software. The same solder joints of surface mount capacitors that were used for nanoindentation were used for IMC thickness analysis. The cross-sectioned and potted solder joint samples were taken up for ESEM analysis to capture images of interfacial IMC which would then be used in ImageJ for quantitative measurements. The solder joint samples in the ESEM were moved progressively after capturing IMC at one point to a different location of the same IMC in the solder-pad interface to capture another image. In this manner six images were captured in each solder joint and in total six solder joints were analyzed in the new and aged boards.

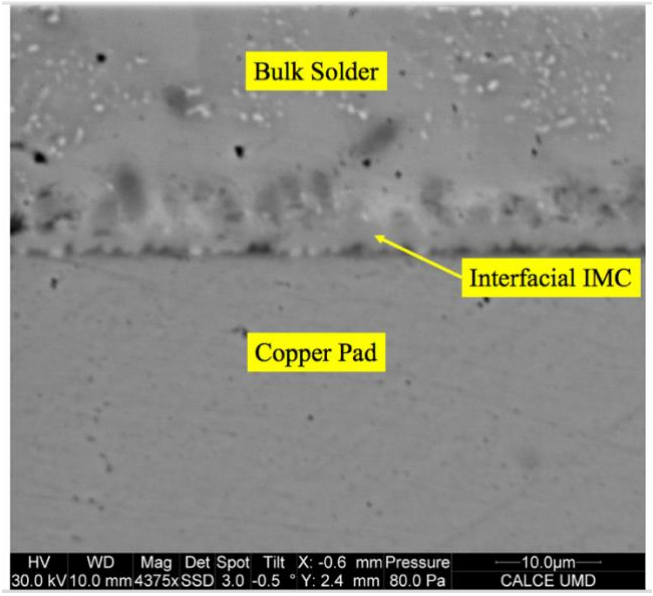


Figure 19 ESEM Image of Interfacial IMC of Aged Solder Joint

The captured ESEM images are then imported into the ImageJ processing software for further quantitative measurements. The imported image is processed further to differentiate different features of the images such as the bulk solder, interfacial IMC, and the solder pad distinctively. To distinguish the features, the images are processed using one of the in-built filters in the software. For this study, a bandpass filter was used where the larger features were approximated to 20 pixels, while the smaller features were approximated to 3 pixels. The filter image was then subjected to thresholding process. This will further ease the measurement process by making the region of interest the desired color and rest of the image to be in a different color. The thresholding can be manually adjusted and fixed at a point which makes the interfacial IMC as different as possible from rest of the image.

Once the desired image quality is obtained, contour tool is used from drawing toolbar to mark the outline of the interfacial IMC as shown in Figure 20. The area of the contour was measured which provides us the area of the IMC. Then a line is drawn to

measure the length of the IMC which is then used to divide the area of the contour to obtain the thickness of the IMC. This is repeated for all the images and the average of all the images is taken to be the thickness of aged and new solder joint.

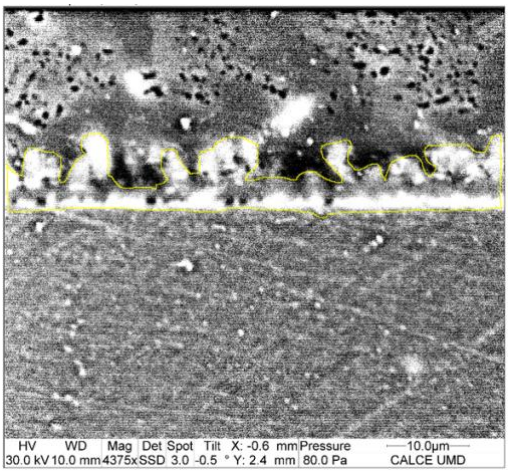


Figure 20 ImageJ Image with the contour in yellow color

Appendix B: Creep Deformation Charts

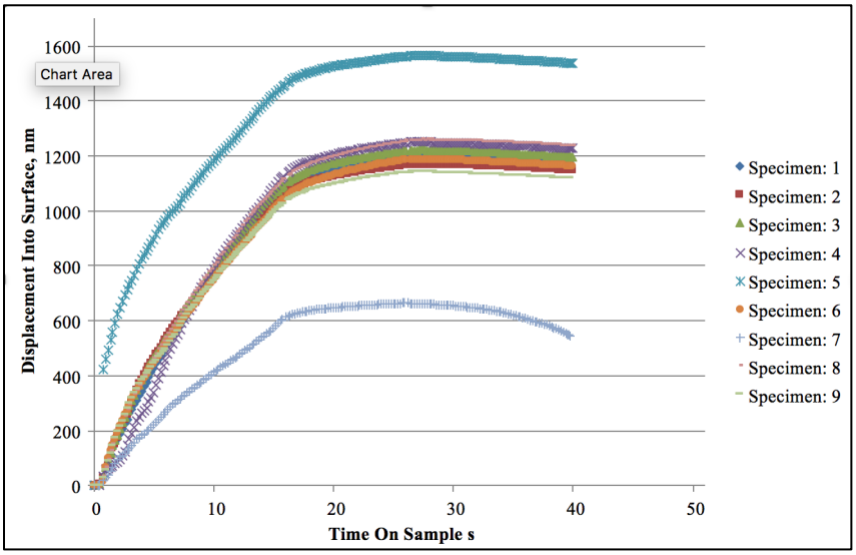


Figure 21 Creep Displacement Curves of New Solder Joints

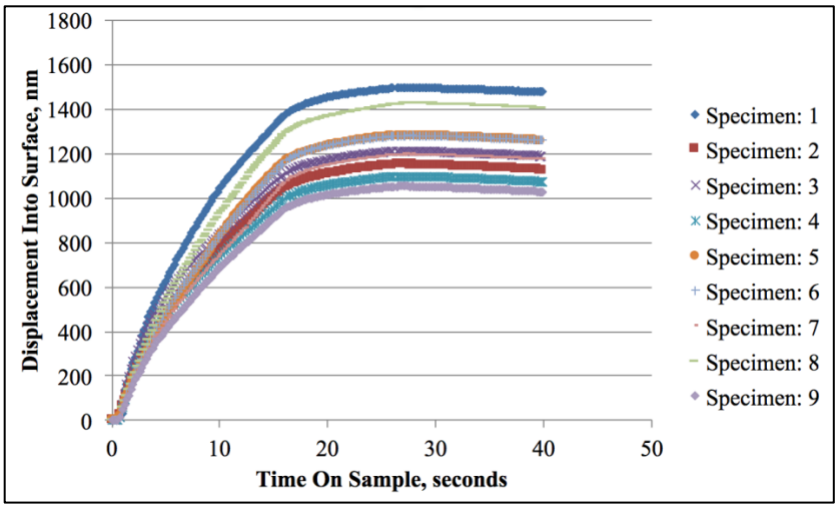


Figure 22 Creep Displacement Curves of Aged Solder Joints

Appendix C: Nanoindentation Measurement Distribution

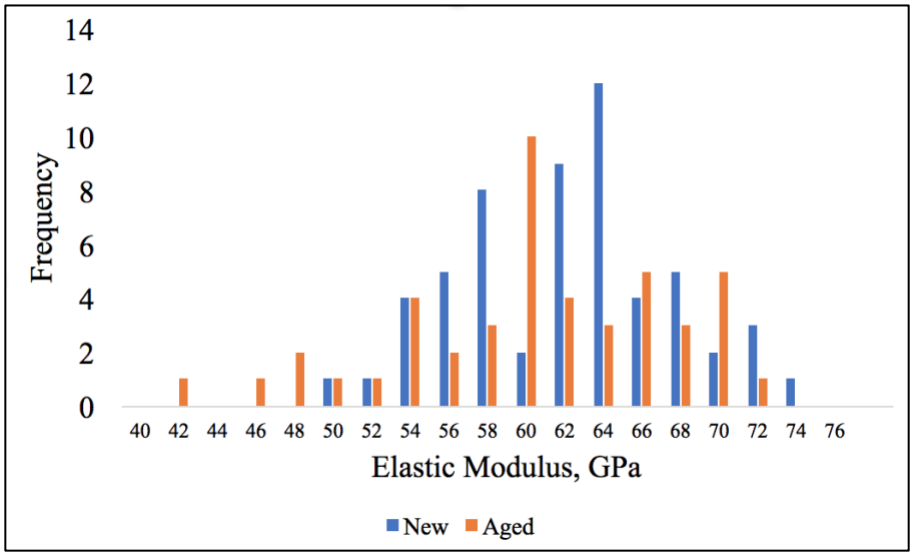


Figure 23 Distribution of Elastic Modulus of New and Aged Solder Joint

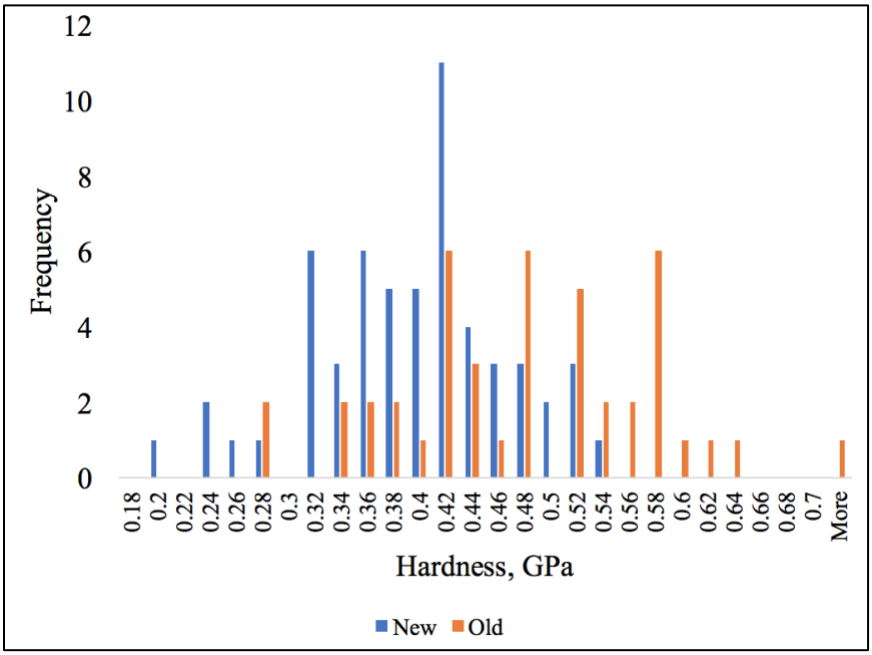


Figure 24 Distribution of Hardness of New and Aged Solder Joint

References

[1] Wellkang Consulting, “Brief introduction of directive 2002/96/EC of 27 January 2003 on waste electrical and electronic equipment (WEEE),” Accessed online: http://www.weeeregistration.com/weee-directive.html, Last accessed: July 15, 2014.

[2] “Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” Official Journal L 037, pp. 19-23, February 13, 2003, Accessed online: http://eurlex.europa.eu/LexUriServ/LexUriServ.do?uri=CELEX:32002L0095:EN:HTML, Last accessed: July 15, 2014.

[3] European Union Parliament, "Directive 2002/95/EC/ on the restriction of the use of certain hazardous substances in electrical and electronic equipment," Official J. Eur. Union, 2003.

[4] European Commission, “Recast of the RoHS Directive,” Accessed online: http://ec.europa.eu/environment/waste/rohs_eee/, Last updated: February 7, 2014, Last accessed: July 15, 2014.

[5] S. Ganesan, and M. Pecht, Lead-free Electronics, John Wiley and Sons, Inc., New York, 2006.

[6] M. Pecht, Y. Fukuda, and S. Rajagopal, “The Impact of Lead-free Legislation Exemptions on the Electronics Industry,” IEEE Transactions on Electronics Packaging Manufacturing, vol. 27, no. 4, pp. 221-232, October 2004.

[7] R. Ciocci, and M. Pecht, “Questions Concerning the Migration to Lead-free Solder,” Circuit World, vol. 30, no. 2, pp. 34-40, 2004.

[8] J. R. Wilson, “Lead-free RoHS on military electronics procurement”, Military and Aerospace Electronics, 2009. [Online]. Available: http://www.militaryaerospace.com/articles/print/volume-20/issue-4/features/special-report/lead-free-rohs-on-military-electronics-procurement.html

[9] European Commission, “Environment: Commission proposes revised laws on recycling and use of hazardous substances in electrical and electronic equipment,” IP/08/1878, Press Release, December 3, 2008, Accessed online: http://europa.eu/rapid/press-release_IP-08-1878_en.htm, Last accessed: July 15, 2014.

[10] S. Mathew, M. Osterman, and M. Pecht, “Evaluation of pure tin plated copper alloy substrates for tin whiskers,” Circuit World, vol. 35, no. 1, pp. 3-8, 2009.

[11] B. Smith, "Preparing for Life Without Lead," IEEE Manufacturing Engineer, Kidsgrove, Vol. 82, No: 6, pp: 44-47, 2004.

[12] R. Solomon, P. Sandborn and M. Pecht, "Electronic Part Lifecycle Concepts and Obsolescence Forecasting," in IEEE Transactions on Components and Packaging Technologies, Vol. 23, No: 4, pp: 707-717, 2000.

[13] J. T. Hanlon, "The Future of Components for High Reliability Military and Space Applications," Sandia National Laboratories, Albuquerque, 1996.
[14] Kester, "Lead-free Hand-soldering – Ending the Nightmares", June 2013. [Online]. Available: http://www.kester.com/kester-content/uploads/2013/06/Lead-free-Handsoldering.Final_.4.19.06.pdf
[15] Q. Zhang, A. Dasgupta, P. Haswell and M. Osterman, "Isothermal Mechanical Fatigue of Lead-free Solders: Damage Propagation and Time to Failure," in International SAMPE Technical Conference, Baltimore, November 2002.
[16] Q. Zhang, P. Haswell and A. Dasgupta, "Cyclic mechanical durability of Sn-3.9 Ag-0.6 Cu and Sn-3.5 Ag lead-free solder alloys." In ASME 2002 International Mechanical Engineering Congress and Exposition, pp. 99-104. American Society of Mechanical Engineers, 2002.
[17] P. Haswell and A. Dasgupta, "“Viscoplastic Constitutive Properties of Lead-free Sn-3.9Ag-0.6Cu Alloy," in MRS Proceedings, San Francisco, 2001.
[18] C. Hunt and M. Dusek, "Lead-free Solders and PCB Finish Effects on Solder Joint Reliability," in Electronics System-integration Technology Conference, Dresden, 2006.
[19] H. Cui, M. Ferrera and M. Micak, "Analysis of Lead Free Tin Whisker Test Methodology and Characterization," in ROCS Workshop, San Antonio, 2006.
[20] J. A. Brusse, G. J. Ewell and J. P. Siplon, "Tin Whiskers: Attributes And Mitigation," in CARTS EUROPE 2002: 16th Passive Components Symposium, 2002.
[21] B. Medgyes, B. Illes and G. Harsanyi, "Electrochemical migration behaviour of Cu, Sn, Ag and Sn63/Pb37," Journal of Materials Science: Materials in Electronics, vol. 23, no. 2, pp. 551-556, 2012.
[22] B. Medgyes, D. Rigler, B. Illes, G. Harsanyi and L. Gal, "Investigating of Electrochemical Migration on Low-Ag Lead-Free Solder Alloys," in IEEE 18th International Symposium for Design and Technology in Electronic Packaging (SIITME), Alba Iulia, 2012.
[23] D. Xie, C. Chin, K. Ang, D. Lau and D. Shangguan, "A New Method to Evaluate BGA Pad Cratering in Lead-Free Soldering," in 2008 Electronic Components and Technology Conference, Lake Buena Vista, 2008.
[24] H. Ma, K.-C. Liu, T.-K. Lee and D. H. Kim, "Effects of PCB Design Variations on Bend and ATC Performance of Lead-Free Solder Joints," in Electronic Components and Technology Conference, Las Vegas, 2010.
[25] B. Medgyes, P. Tamasi, F. Hajdu, R. Muranyi, M. L. varsanyi, L. Gal and G. Harsanyi, "Corrosion Investigations on Lead–Free Micro–Alloyed Solder Alloys used in Electronics," in 38th Int. Spring Seminar on Electronics Technology , Eger, 2015.
[26] F. Song and S. W. R. Lee, "Corrosion of Sn-Ag-Cu Lead-free Solders and the Corresponding Effects on Board Level Solder Joint Reliability," in 2006 Electronic Components and Technology Conference, San Diego, 2006.
[27] G. Zeng, S. McDonald, K. Sweatman and K. Nogita, "Tin pest in lead-free solders? Fundamental studies on the effect of impurities on phase transformation

kinetics," in Electronics Packaging (ICEP), 2014 International Conference, Toyama, 2014.

[28] R. R. Madsen, "Component Reliability After Long Term Storage," Texas Instruments, 2008. [Online]. Available: http://www.ti.com/lit/wp/slva304/slva304.pdf

[29] H. Ma, J. C. Suhling, Y. Zhang, P. Lall, & M. J. Bozack,"The influence of elevated temperature aging on reliability of lead free solder joints." In Electronic Components and Technology Conference, 2007. ECTC'07. Proceedings. 57th, pp. 653-668. IEEE, 2007.

[30] V. Venkatadri, L. Yin, Y. Xing, E. Cotts, K. Srihari, & P. Borgesen, "Accelerating the effects of aging on the reliability of lead free solder joints in a quantitative fashion." In Electronic Components and Technology Conference, 2009. ECTC 2009. 59th, pp. 398-405. IEEE, 2009.

[31] M. Hasnine, J. C. Suhling, B. C. Prorok, M. J. Bozack, & P. Lall, "Exploration of aging induced evolution of solder joints using nanoindentation and microdiffraction." In Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th, pp. 379-394. IEEE, 2014.

[32] H. Ma, J. C. Suhling, P. Lall, & M. J. Bozack, "Effects of aging on the stress-strain and creep behaviors of lead free solders." In Thermal and Thermomechanical Phenomena in Electronics Systems, 2006. ITHERM'06. The Tenth Intersociety Conference on, pp. 961-976. IEEE, 2006.

[33] Q. Xiao, L. Nguyen, & W. D. Armstrong, "Aging and creep behavior of Sn3. 9Ag0. 6Cu solder alloy", Proceedings of Electronic Components and Technology Conference, 54th, Vol. 2, pp. 1325-1332. IEEE, 2004.

[34] K. W. Moon, M. E. Williams, C. E. Johnson, G. R. Stafford, C. A. Handwerker, and W. J. Boettinger. "The formation of whiskers on electroplated tin containing copper." In Proceedings of the fourth pacific Rim international conference on advanced materials and processing. The Japanese Institute of Metals, pp. 1115-1118. 2001.

[35] D. W. Romm, D. C. Abbott, S. Grenney, and M. Khan, "Whisker evaluation of tin-plated logic component leads", Texas Instruments Application Report SZZA037A, 1-27, 2003.

[36] Y. W. Lin, Y. S. Lai, Y. L. Lin, C. T. Tu, and C. R. Kao, "Tin whisker growth induced by high electron current density", Journal of Electronic Materials, 37(1), 17-22, 2008.

[37] W. Engelmaier, "Fatigue Life of Leadless chip carrier solder joints during power cycling", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-6, No. 3, pp. 232-237, 1983

[38] Reliability Hot Wire, "Miner's Rule and Cumulative Damage Models". [Online]. Available: http://www.weibull.com/hotwire/issue116/hottopics116.htm

[39] R. Pandher, and T. Lawlor, "Effect of Silver in common lead-free alloys", Proceedings of the International Conference on Soldering and Reliability, pp. 1-14. 2009. [Online]. Available:

http://www.circuitnet.com/news/uploads/1/Effect_of_silver_in_common_lead-free_alloys_paper_Eng04.23.09.pdf

[40] S. Terashima, Y. Kariya, T. Hosoi, and M. Tanaka, “Effect of Silver Content on Thermal Fatigue Life of Sn-xAg-0.5Cu Flip-Chip Interconnects”, Journal of Electronic Materials, Vol. 32, no. 12, Page 1527-1533, 2003.