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## ABSTRACT

Title of Thesis: RF INDUCED NONLINEAR EFFECTS IN HIGH-SPEED  
ELECTRONICS

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Degree and year: Master of Science, 2004

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*Abstract* - Previous experiments and research have indicated rectification of modulated electromagnetic interference can cause upset effects in digital electronics. Although RF rectification has been observed in discrete components, only speculation of the most sensitive mechanisms causing RF rectification has been proposed.

Through theoretical analysis, experiments, and simulations, the p-n junctions in ESD protection circuits were determined to be very susceptible to rectifying pulse modulated RF signals. Threshold experiments on several logic families of CMOS inverters provided indications to susceptibilities of electronics based on their input ESD protection topology.

High frequency port measurements were performed identifying resonances between 500 MHz and 1.5 GHz due to inductances from bonding wires and the voltage dependent junction capacitances of the ESD protection circuits. Parasitic elements have also been determined to help promote additional effects including bias shifts, state changes, RF gain, and undesirable circuit resonances.

DC and high frequency parameter extraction techniques were used to build diode and generic inverter models including package parasitics in PSPICE. Models were designed which gave good agreement to measured rectification drive curves, input impedance resonances, output voltage bias shifts, and induced spurious oscillations.

**RF INDUCED NONLINEAR EFFECTS IN HIGH-SPEED ELECTRONICS**

by

Todd M. Firestone

Thesis submitted to the Faculty of the Graduate School of the  
University of Maryland, College Park in partial fulfillment

Of the requirements for the degree of  
Master of Science

2004

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## **DEDICATION**

To my family, for supporting my education over the years.

## ACKNOWLEDGMENTS

This research was funded by the Department of Defense under the AFOSR Grant F496200110374 supporting the MURI 2001: Microwave and Chaos Effects on Electronics.

I would like to thank my academic advisor, Victor Granatstein, for inviting me to be one of his graduate students. I am very thankful for him for allowing me to be part of the MURI 2001 project research team and introducing me to such a large group of experts in electrical engineering and physics at the University of Maryland.

Without the drive and inspiration of John Rodgers, none of this work would have been possible. All of the ideas in this paper were initiated or were heavily influenced by John to explore the depth and every aspect of the research. It has been a great pleasure having John as a mentor and working with him over the past three years. Every time I spoke with John he would have a new idea, would talk to great length about any and every subject, or would stay late nights working on experiments and simulations. I am very happy to say the he has been by far the greatest influence on my electrical engineering career.

Discussions with Neil Goldsman and Agis Iliadis provided great insight and inspired several ideas in many areas of this work. I was very pleased when they agreed to be a part of my defense committee.

A large thanks goes to Mark Walters for helping with initial injection testing on the computer DRAM memory modules. I would also like to thank Ronald McLaren for building test boxes for the CMOS inverters, and Jay Pyle and Doug Cohen who provided great technical help.

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## LIST OF ABBREVIATIONS AND DEFINITIONS

C – capacitance  
CAS – column address strobe  
COTS – commercial off the shelf  
DF – duty factor (pulse width/PRI)  
DUT – device under test  
EMC – electromagnetic compatibility  
EMI – electromagnetic interference  
ESD – electrostatic discharge  
 $f_0$  – center frequency, or injected RF signal frequency  
 $f_T$  – transition frequency, or crossover frequency  
ggNMOS – gate grounded n-doped MOSFET  
HPM – high power microwave  
IC – integrated circuit  
L – inductance  
MOSFET – metal oxide semiconductor field emission transistor  
PRF – pulse repetition frequency (1/PRI)  
PRI – pulse repetition interval (1/PRF)  
PW – pulse width  
R – resistance  
RAS – row address strobe  
RF – radio frequency  
RFI – radio frequency interference  
S-parameters – scattering parameters  
Vdd – device power supply voltage  
VNA – Vector Network Analyzer  
Vsp – CMOS Inverter Switching Point Voltage

## CHAPTER 1 INTRODUCTION

The effects of electromagnetic interference on electronics have been directly attributed to the RF signal or to the rectification of modulated RF signals. Previous work in RF injection experiments has examined the propagation delays, logic state changes and latch-up due to the RF signal for frequencies below the transition frequency ( $f_T$ ) of the circuit tested. Above the transition frequency of circuits, errors have been associated with the induced low-frequency voltages due to the rectification effects of the RF. Although rectification has been observed in discrete transistors at microwave frequencies, the most susceptible components in more complex logic circuits have not been identified.

### 1.1. Background

The literature on experiments examining the effects on EMI on electronics have been found to focus on two different frequency ranges: the regions below and above the rolloff frequency of the circuits under test. In these earlier cases, test frequencies were kept under 800 MHz. This range is where the RF had a direct effect on the circuit. And above 800 MHz, the rectification of RF signal was observed to have more of an impact on causing effects in circuits. A brief summary of these studies is provided below to give an idea of the effects observed and the ideas each of the studies proposed as potential problems.

In 1985, Tront injected CW RF signals at frequencies of 100 and 220 MHz into the junction between a NMOS driver stage and a NMOS buffer stage while simultaneously stimulating the driver circuit with logic. The effects observed the logic pulses changing state, logic pulse propagation delay, and circuit latch-up [1]. This research investigated state changes and other effects due to the direct influence of the RF signal, and showed how the relationship of the phase of the RF signal could affect the propagation of logic pulses through digital logic circuits. Laurin examined the effects of inverters by direct injection between CMOS inverter stages and on crystal oscillators [2]. The devices tested were CD4007A inverters arranged in a series to simulate a realistic logic circuit environment using a coupling capacitor soldered in between two inverters to inject RF signals. The direct injection experiments used RF frequencies of 5, 10, and 50 MHz. A



loop antenna was incorporated at the injection point to help the coupling of RF into the system, used for test frequencies up to 200 MHz. Laurin noticed resonances associated with the antenna helping to boost the amplitude of the RF signals which had greater influence on the effects observed in his testing.

Boeing's Integrated Circuit Electromagnetic Immunity Handbook covered the systematic power threshold testing of various logic devices in the late 70's with follow-up testing in 1999 [3]. Experiments cover the frequency range of 10 MHz to 10 GHz with power levels up to 27 dBm. Logic families tested included TTL, LS and ALS. These rigorous experiments injected RF signals into the input, output, and power supply pins of several types of logic devices comparing the threshold power curves for the separate cases when the input was in the low and high logic levels. Susceptibility in the devices tended to be below 1 GHz and at power levels above 20 dBm, indicating increasing required power with frequency.

The effects of microwave and RF signals causing soft-errors by rectification of were investigated as early as 1975 by Richardson who examined rectification by bipolar and field-effect transistors from 1 MHz to 10 GHz [4] - [7]. Simple models for the rectification effects were based on small signal analysis and the characteristic equations for the transistors. Current and voltage rectification sensitivity were determined theoretically and compared with measured results. Richardson mentions the inductance of the bonding wires is approximately 3 nH for his circuit and MOSFET gate capacitances were measured around 0.5 pF. Any effect of resonance due to these components would be well above the 10 GHz range.

A series of experiments performed by Kenneally looked into the effects of ESD protection devices in MOS devices and the susceptibility of CMOS and low power Schottky type logic circuits to injected RF signals [8] - [10]. One set of experiments showed the partial removal of the ESD protection diodes in a 8086 microprocessor led to an increase in the required CW power to cause state changes [8]. Kenneally pointed out the circuits in question had rolloff frequencies around 300 MHz, below which circuits were directly susceptible to RF signals. Kenneally mentions above the transitions frequency ( $f_T$ ) of the circuits tested tended to be susceptible to the induced rectified bias shifts causing

upset and timing errors [8]. Testing about 800 MHz was not performed believing the effect of input inductance would not be a factor until 20 GHz.

## **1.2. Motivation for Study**

Initial high frequency (300 MHz – 2 GHz) testing we performed on computer DRAM memory modules showed RF rectification was induced at the injection points. With increasing power memory bit errors were detected as well as periodic computer failures depending on frequency and power levels. Measured threshold power levels for CW and pulse modulated RF signals with a duty factor of 50 % showed a difference between 7 and 10 dB in peak power to cause effects. These tests agreed with those in the previously found in the literature, pointing to the rectification effects being effective at causing errors in digital electronics. A short discussion on the DRAM memory experiments is provided in Appendix A.

This testing led to interest in performing experiments on the basic logic circuit building blocks to determine why modulated high frequency RF signals had more of effect on the DRAM than in the CW case. We were interested in creating a controlled environment to eliminate the complexities of larger systems, however having the most basic circuitry found in modern electronics. Although several types of discrete circuits have been previously determined to rectify RF, no candidates have been proposed and proven to be the most sensitive to rectification in integrated circuits.

We also wanted to use low duty factor pulse modulated RF to eliminate thermal effects in the devices. Previous studies also tended to focus only on the threshold power levels of high frequency signals to cause effects. This is partially due to the limitations of the equipment at the time including the sampling rates and abilities of available oscilloscopes. Of interest in this study are the reproducible effects that can be caused by low-power RF pulses on electronics, attempting to discover all of the induced behaviors within the circuits and being able to model these effects.

## **1.3. Organization of Thesis**

This thesis focuses on the rectification properties of the input ESD protection circuit and the effects of resonances found at the inputs of CMOS inverters. Several logic families

of CMOS inverters from different manufacturers have been tested to observe and measured the various effects of RF on the circuits and in order to determine the sources of these effects. The goal was to perform very thorough experiments, in depth research of circuit components, and the building of computer models to reproduce the effects observed in our measurements.

Chapter 2 will introduce the fundamental circuits that make up the input circuitry to the CMOS inverter. ESD protection devices are briefly discussed covering different topologies common in modern electronics. The basic equations for the diode were used to determine the parameters, which affect rectification sensitivity an RF signal to cause state changes in digital electronics. Equations based on the operation of the CMOS inverters show insight into the parameters required to cause the inverter to switch.

The results of the measurements used to determine effects and their sources are covered in Chapter 3. Input port characteristics will give insights into the mechanisms dominant to DC and AC stimulus. These measurements were intended to be the basis in building computer models. Power threshold experiments were used to determine the differences in susceptibilities of different input logic states as well as to other circuits.

Finally, the results of simulations in comparison to measured effects are covered in Chapter 4. Models designed from the parameters extracted in the previous section were simulated to match results to the observed measurements.

## **CHAPTER 2 HIGH SPEED CIRCUIT CHARACTERISTICS**

### **2.1. Introduction**

The two main fundamental structures of CMOS inverters are the ESD protection devices, located at the input and output ports of the device, and the inverter itself. ESD protection device topologies differ with almost every different class of logic family available. However, each one of these topologies contains at least one p-n junction, which is the fundamental physical component of a diode. The following sections will focus on the various topologies of ESD protection devices, the basic equations of the ideal diode, and the characteristic equations for the CMOS inverter.

### **2.2. ESD Protection Device Topologies**

Electrostatic discharge (ESD) was recognized as a potential threat to circuits early in the development of digital electronics. Potential differences between chips and insertion devices (human hands and insertion machines) pose as sources for a possible discharge event, which could destroy a circuit before it is even integrated into the destined circuit. Gate oxides can break down with an applied electric field less than 6MV/cm, amounting to 6 V across a gate 10 nm thick oxide [11]. ESD protection devices have been nominally integrated into the input and output ports of all digital devices in order to source or sink current away from the gate oxide during an ESD event.

ESD protection device topologies differ from one logic family to the next and vary with every manufacturer. These devices may contain a single diode, several stages of diodes, in-line resistances to suppress current spikes, or more advanced components such as thick field oxide devices or silicon controlled rectifiers. Although the ESD topologies differ with logic families, the same topologies are normally used within a given logic family [12].

ESD protection devices are placed into two different classifications defined by operation, breakdown and non-breakdown. The non-breakdown components, such as diodes, BJTs and MOSFETs, operate near normal operating parameters, are well understood and the easiest to model. One disadvantage to non-breakdown ESD

components is the size of the device size, which can be on the orders of magnitude larger to the circuits they protect as seen in Figure 1 showing the layout of the ESD protection diodes, bonding wires, CMOS inverter, power supply bus, and ground bus [13].

Manufacturer's datasheets containing block diagrams of the ESD devices found in the circuits tend to use very basic circuits to signify the basic functionality of the protection used. Examples of commonly found ESD protection topologies are shown in Figure 2, demonstrating single diode structures with and without diffusion resistors, gate grounded NMOS (ggNMOS) and the PMOS equivalent, and a topology using zener diodes.

Breakdown devices do not normally work in normal operation of the semiconductor and are designed to handle extreme ESD events. These devices are much harder to model, but are more area efficient. The main mechanisms of these devices are reverse avalanche breakdown or a forward snap-back voltage breakdown. The breakdown devices include [14]:

- Thick Field Oxide (TFO)
- Zener Diodes
- Grounded Gate NMOS (ggNMOS)
- Silicon Controlled Rectifier (SCR)
- PIPE (punch through-induced protection element)
- LVSCR (low voltage SCR)
- GCNMOS (gate-coupled NMOS)
- Bimodal SCR
- Spark Gap

All of these devices realized in semiconductors contain at least one p-n junction. Even though the non-breakdown devices may operate in a region outside of normal operation in the case when an ESD event occurs, they will operate as predicted in normal operating regimes (for example, a zener is sometimes used for its reverse breakdown characteristics, however will operate like a normal diode in its forward biased region).

In normal CMOS operation after the device has been installed into the destination circuit, ESD events are not expected to occur and the ESD protection devices are electrically turned off, or reverse biased.

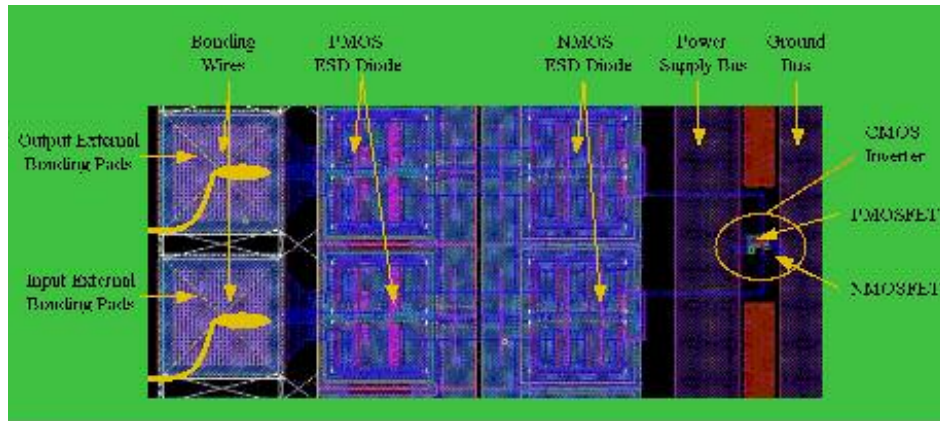


Figure 1. CMOS inverter layout showing the external and internal bonding pads, bonding wires, ESD diodes, and single stage CMOS inverter. Notice the difference in size of the NMOS/PMOS ESD protection structures and the designed CMOS inverter. The bonding wires were added in as a visual aid and may not be to scale [13].

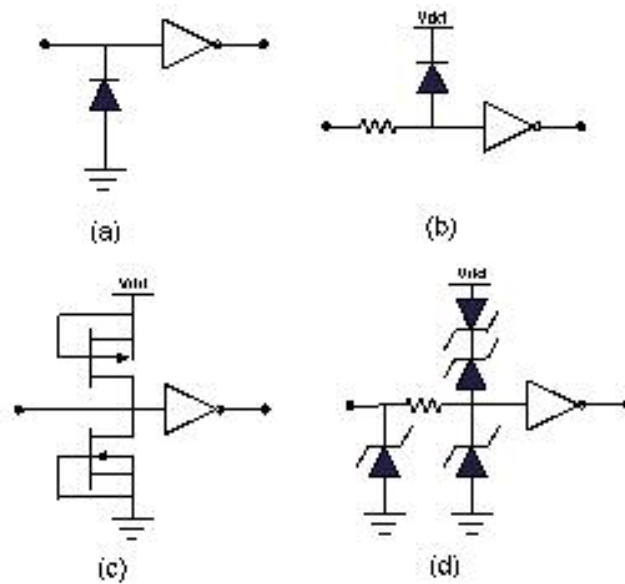


Figure 2. Four examples of ESD protection circuit topologies: (a) ground to signal ESD diode, (b) diffused resistance and signal to Vdd ESD diode, (c) gate grounded NMOS and PMOS, and (d) zener topology with two diodes from ground to signal separated by a diffused resistor and back to back zeners from signal to Vdd.

### 2.3. Diode Characteristics

A diode is formed when layers of p-doped and n-doped semiconductor are fabricated next to each other creating a potential difference between the two layers. Although there are various different types of diodes (p-n, p-i-n, Schottky, Zener, tunneling,

etc), only the p-n diode will be considered in this discussion. In order to allow current to flow through the device a positive voltage must be applied across the p-side (anode) and the n-side (cathode) in order to offset the potential barrier. The voltage to activate the diode may be DC or AC. When AC is applied the terminals of the diode, the AC signal is clipped or “rectified”, since only one polarity of the AC, if large enough to offset the internal potential, will cause the diode to allow current to flow. Diodes have been used to rectify RF in order to “detect” the signal in high frequency circuit measurements. Detection of an RF signal is due to the non-linear effects of the diode, rectifying the RF and converting the RF signal into DC and low frequency components.

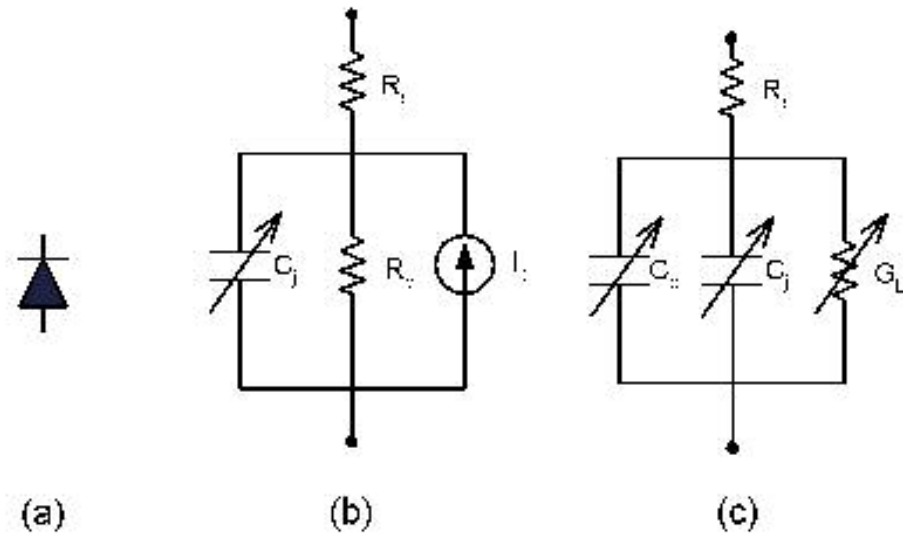


Figure 3. Diode representations: (a) block diagram, (b) reversed-biased lumped element model, and (c) forward-biased model.

### 2.3.1. Ideal Diode Equations

The current through the diode can be modeled by described by the relationship between the current and applied voltage in the ideal diode current equation:

$$I(V) = I_s \left( e^{\frac{V_d}{nV_t}} - 1 \right) \quad (1)$$

where  $I_s$  is the saturation current,  $V_d$  is the voltage difference across the cathode and anode of the diode,  $n$  is an ideality factor, and  $V_t$  is the thermal voltage. The thermal voltage is defined as  $kT/q$  where  $k$  is Boltzmann’s constant,  $T$  is temperature, and  $q$  is the charge of an electron ( $V_t$  is approximately 26 mV at  $T = 300\text{K}$ ) [15].

Applying a small signal AC signal to the continuous wave RF signal has amplitude and frequency and with the addition of a DC voltage, the applied diode voltage and current is described as:

$$V_d = V_0 + v_{rf} \cos(\omega_{rf} t) \quad (2)$$

where  $V_0$  is a DC voltage,  $v_{rf}$  is the amplitude of a sinusoidal signal, and  $\omega_{rf}$  is the frequency of the RF signal. Using Taylor's expansion, the small-signal approximation for the diode current is:

$$I(V_d) = I_0 + i_{rf} = I_0 + v_{rf} \cos(\omega_{rf} t) G_0 + \frac{(v_{rf} \cos(\omega_{rf} t))^2}{2} G_0' + O(v_{rf}^3) \quad (3)$$

with the conductance being defined as

$$G_0 = \frac{1}{R_v} = \frac{(I_0 + I_s)}{V_t} \quad G_0' = \frac{G_0}{V_t} \quad (4)$$

where  $I_0$  is DC current component due to  $V_0$ ,  $i_{rf}$  is the AC current,  $R_v$  is the video resistance, and  $O(v_{rf}^3)$  represents higher order terms [15]. Reducing the second order term in Eq. (3), the new DC current term will create a voltage across the resistance looking out from the cathode of the diode ( $R_{load}$ ) in parallel with the diode video voltage:

$$V_{det} = \frac{v_{rf}^2 I_s}{4V_t^2} (R_{load} \parallel R_v) \quad (5)$$

where  $V_{det}$  is the induced detected DC voltage and  $R_{load}$  is the low-frequency resistance as seen from the input of the CMOS inverter. In Figure 4(a), detected voltages for saturation currents between 1nA and 10 nA for a load resistance of 1 M $\Omega$  show rectified voltages for RF amplitudes up to 1 V. The relation between the detected voltage and  $1/R_{load}$  for a saturation current of 1 nA and RF amplitudes of 0.2, 0.5, 1.0 and 1.5 volts is shown in Figure 4(b). This last relation is important when logic devices such as tri-state buffers, which vary between a low to high output impedance depending on state of operation, are used in ICs.



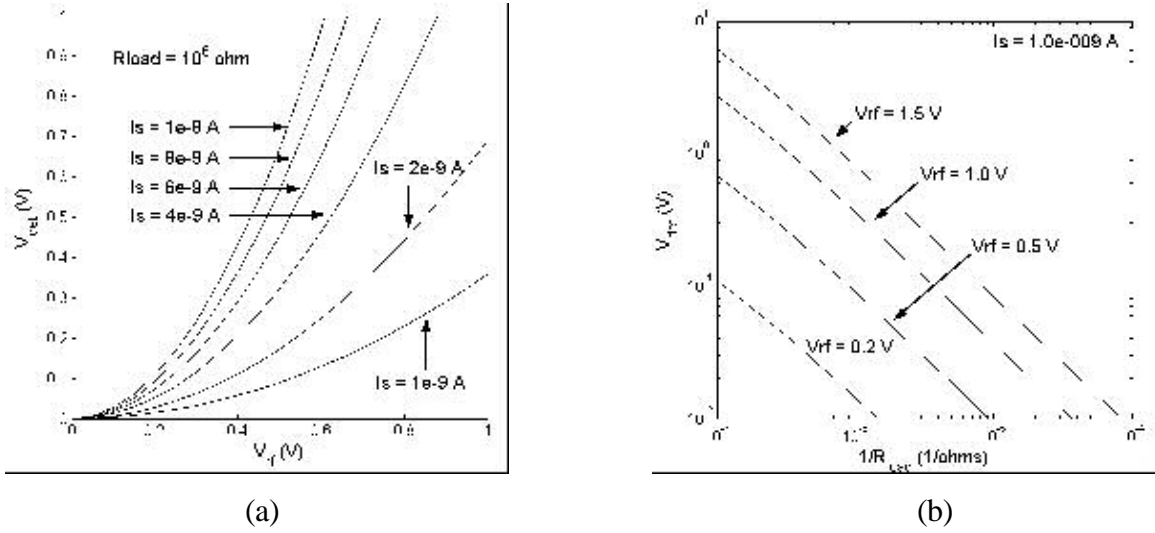


Figure 4. Detected voltages for (a) a diode versus RF amplitude for several values of saturation current and  $R_{\text{load}} = 1\text{M}\Omega$ , and (b) with respect to  $1/R_{\text{load}}$  for a diode with a saturation current of 1 nA and  $V_{\text{rf}}$  of 0.2, 0.5, 1.0 and 1.5 volts.

### 2.3.2. Bandwidth Considerations

The previous equations assumed the RF signal is continuous, and therefore producing a purely DC voltage term. However, in the case where the RF is modulated, the ‘DC’ voltage will have frequency components associated with modulation of the RF signal.

The required bandwidth to view the signal can be determined by starting with a Fourier transform on the cosine function:

$$X(f) = \frac{1}{2} [\delta(f - f_0) + \delta(f + f_0)] \quad (6)$$

where  $f = \omega/2\pi$  and  $f_0 = \omega_0/2\pi$  [16] Although the transform contains negative frequency components, only the positive frequency components will be displayed on a spectrum analyzer (Figure 5a,b).

Modulation is often used with RF signals and comes in different forms including some of the more common types: amplitude (AM), frequency (FM) and pulse modulation. In the case of amplitude modulation, the equation for the signal is defined as:

$$v_{\text{rf}} = v_0 (1 + m \cos(\omega_m t)) \cos(\omega_o t) \quad (7)$$

where  $m$  is the modulation index (normally  $0 < m < 1$ ) and  $\omega_m$  is the modulation frequency. Substituting into the small signal current portion of Eq. (4) and expanding, the AC diode current now becomes

$$\begin{aligned}
i_{rf}(t) &= v_0 G_0 (1 + m \cos \omega_m t) \cos \omega_0 t + \frac{v_0^2}{2} G_0' (1 + m \cos \omega_m t)^2 \cos^2 \omega_0 t \\
&= v_0 G_0 \left[ \cos \omega_0 t + \frac{m}{2} \cos(\omega_0 + \omega_m)t + \frac{m}{2} \cos(\omega_0 - \omega_m)t \right] \\
&\quad + \frac{v_0^2}{4} G_0' \left[ 1 + \frac{m^2}{2} + 2m \cos \omega_m t + \frac{m^2}{2} \cos 2\omega_m t + \cos 2\omega_0 t \right. \\
&\quad \left. + m \cos(2\omega_0 + \omega_m)t + m \cos(2\omega_0 - \omega_m)t + \frac{m^2}{2} \cos 2\omega_0 t \right. \\
&\quad \left. + \frac{m^2}{4} \cos 2(\omega_0 + \omega_m)t + \frac{m^2}{4} \cos 2(\omega_0 - \omega_m)t \right] \tag{8}
\end{aligned}$$

which shows the frequency content of the modulated signal. An additional DC term is added to the term found in Eq. (7), and the lower frequency components related to the modulation frequency are now visible in the spectrum of the signal of the detected signal (Figure 5c).

Pulse modulation can be considered to be a particular type of AM modulation. By using the step function as the simplest model for pulse modulation and using the ‘multiplication theorem’ for Fourier transforms, the time domain function and Fourier Transform pairs (the time domain and the frequency domain equations) for the pulse modulate RF signal are given as:

$$x(t) = u(\tau, t) \cos(2\pi f_0 t) \tag{9}$$

$$X(f) = \frac{\tau}{2} \text{sinc}(\tau f_0) [\delta(f - f_0) + \delta(f + f_0)] \tag{10}$$

where  $u(\tau, t)$  is a step function with  $\tau$  as the pulse width and  $t$  is time. The frequency spectrum of the pulse modulated RF signal with AM modulation would look similar to the CW RF signal with AM modulation with sinc functions of determinable width replacing the delta functions at the same frequencies as found in Eq. (10) and shown in Figure 5(d). The Fourier transform of the pulse modulation case is important in determining the bandwidth required for the input signal and will be discussed in Chapter 3. As a sample calculation, the required frequency bandwidth required to detect the envelope of the pulsed modulated RF with a pulse width of 100 ns will be  $f = 1/100\text{ns} = 10\text{MHz}$ . The previous calculation was for an idealized pulse, albeit in normal pulse modulation, the envelope has

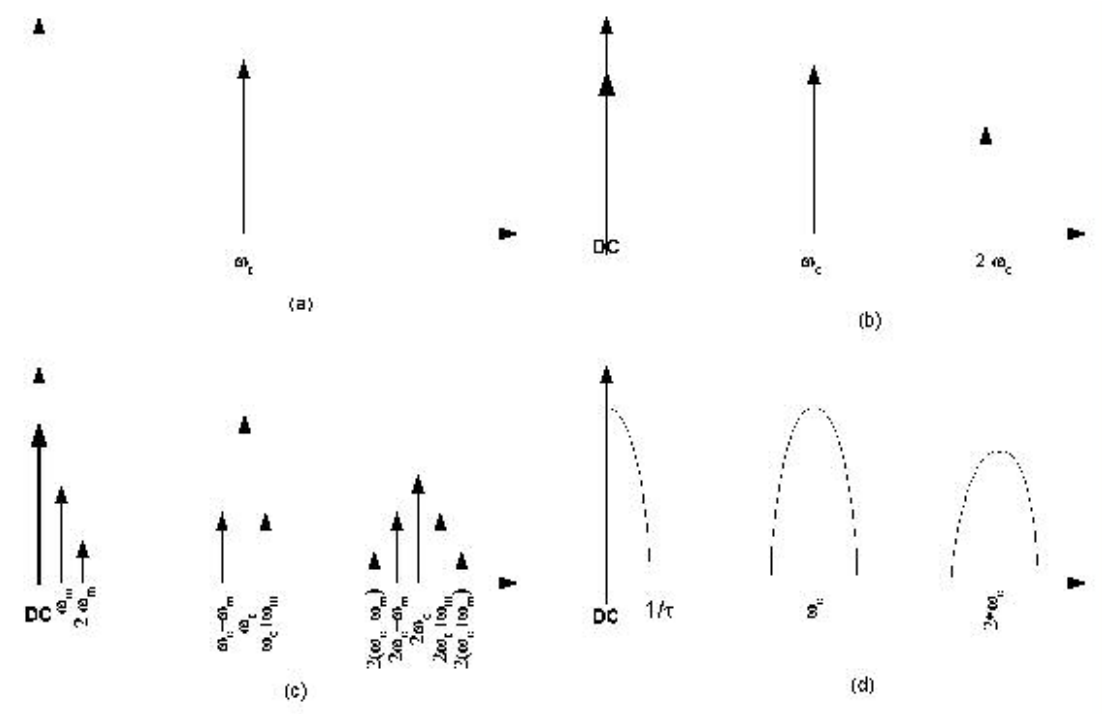


Figure 5. Power Spectrum of (a) single tone RF with frequency  $\omega_0$ , (b) rectified RF CW, (c) rectified RF with AM modulation frequency  $\omega_m$ , and (d) rectified pulse modulated RF. Only the main lobe of the sinc function was used in (d) for simplicity.

a finite rise and fall time which will have higher frequency components in the Fourier spectrum and measurement equipment will require additional bandwidth to detect the signal.

### 2.3.3. Capacitance Model

Returning to the model in Figure 3, the depletion region formed between the p-n layer of the diode is modeled by a voltage dependant capacitance. The capacitance is commonly referred to as the junction capacitance and is modeled as:

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_d}{\phi_{bi}}\right)^m} \quad (11)$$

where  $V_d$  is the applied reverse biased voltage,  $C_{j0}$  is the junction capacitance when  $V_d = 0$ ,  $\phi_{bi}$  is the built-in junction potential, and  $m$  is the emission coefficient.

If a bias voltage is swept over the ESD topologies in Figure 2(a) and (b), excluding inline resistances, the reverse biased capacitances will decrease with increasing voltage

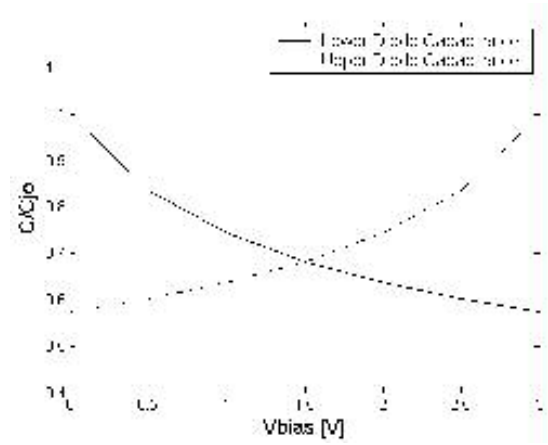


Figure 6. A comparison plot of the voltage dependent capacitances showing variation as a function of bias voltages for an ESD diode from ground to the signal line (Lower Diode) and an ESD diode from the signal line to  $V_{dd}$  (Upper Diode). The diodes were assumed to be matched with  $\phi_{bi} = 0.7$  volts and  $n = 0.5$ .

across the diode. For the lower diode (from ground to the signal line), the change from a low logic state bias to a high bias state will decrease the capacitance as it follows Eq. (11). The junction capacitance in the diode from the signal line to  $V_{dd}$  will decrease capacitance as the bias level goes from high to low, taking into account the diode voltage is now equal to  $V_{dd}$  minus the voltage on the signal line. A comparison of the normalized capacitance changes due to a bias voltage sweep from 0 to 3 volts for the diodes in the previously mentioned configurations is shown in Figure 6 for  $\phi_{bi} = 0.7$  volts and  $n = 0.5$ . The change in capacitance in the case of  $n = 0.5$  for a 3 volt change is 42.6% from the zero bias capacitance.

The reverse bias conditions and equations are dominated by the flow of the majority carriers. The diode model can be modified to include the effects of the minority carriers as the diode is forward biased. As a diode becomes forward biased, minority carriers accumulate in the neutral regions adjacent to the depletion region. The movements of these charges create an effective diffusion capacitance ( $C_D$ ) and conductance ( $G_D$ ). The addition of the diffusion capacitance to the junction capacitance increase very quickly as the voltage becomes forward biased Figure 7.

The capacitance and conductance associated with the minority carrier oscillations are frequency dependent because of the supply and removal of minority carriers is not as rapid as that of majority carriers. Because of this the minority carriers have difficulty staying in sync with the AC signal, thus making the conductance and capacitance both frequency dependent. The equations for the diffusion conductance and capacitance are:

$$G_D = \frac{G_0}{\sqrt{2}} (\sqrt{1 + \omega^2 \tau_p^2} + 1)^{1/2} \quad (12)$$

$$C_D = \frac{G_0}{\omega \sqrt{2}} (\sqrt{1 + \omega^2 \tau_p^2} - 1)^{1/2} \quad (13)$$

where  $\omega$  is the angular frequency of a signal applied to the diode, and  $\tau_p$  is the minority charge absorption time constant [17].

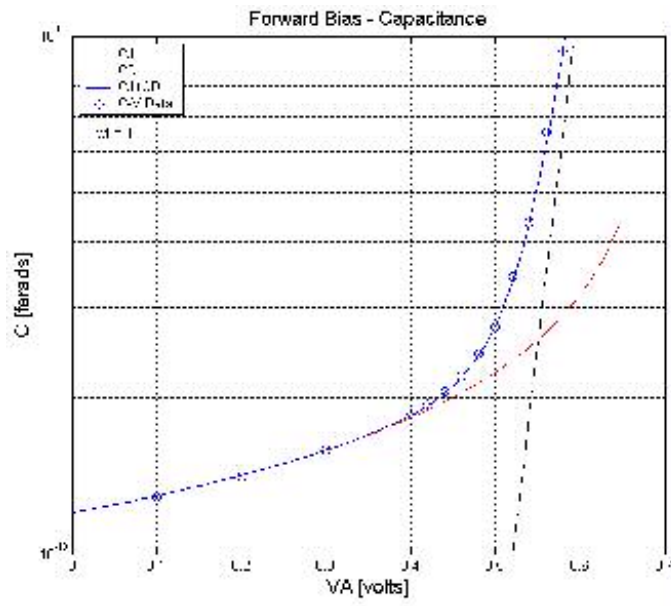


Figure 7. A plot of the forward biased charge conservation capacitance (blue) with respect to diode voltage compared to the ideal diode junction capacitance (red) and the diffusion capacitance (black) [16].

## 2.4. CMOS Inverter Characteristics

Metal oxide semiconductor field effect transistors (MOSFETs) are classified as NMOS (the source and drain regions of the resistor are heavily doped with n-type material) or PMOS devices (the source and drain regions are heavily doped in p-type material). A Complimentary Metal Oxide Semiconductor (CMOS) device is a combination of NMOS and PMOS transistors in series (Figure 8). CMOS devices have become a popular choice in every area of digital circuit design because of the low current consumption, reduction of size, reduction of operation voltages, and large noise immunity.

The basic building block in CMOS digital logic devices is the inverter. In inverter CMOS circuits, the drains of the NMOS and PMOS devices are connected together, the gates are connected together, and the source and substrate are connected to ground and V<sub>dd</sub> for NMOS and PMOS, respectively (Figure 9). Logic topologies use the inverter in different series and parallel configurations, but for ease of analysis, a single inverter stage will be analyzed in this section.

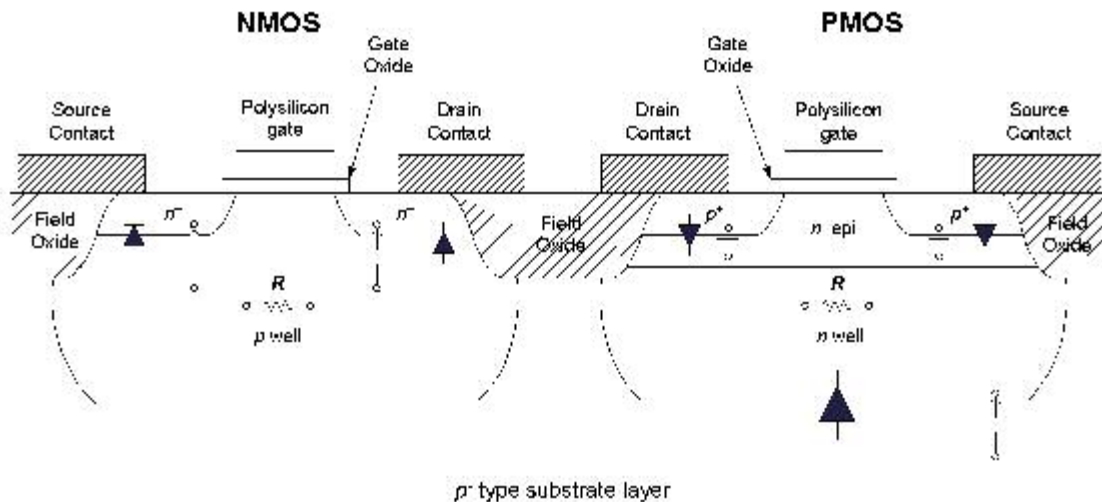


Figure 8. Cross section of CMOS structure showing diode structures formed by p-n junctions, the p-n associated capacitances, and the resistances due to doping of the intrinsic substrate.

The inverter works from applying a voltage to the input of the device which will either cause the NMOS device to turn on when the input voltage is high. The ‘switching point’ is the voltage when the output of the voltage changes from one state to another (high

to low or low to high). This voltage is dependent on  $V_{dd}$ , device size, and threshold voltages for the NMOS and PMOS devices, and is defined as

$$V_{sp} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} V_{THN} + (V_{DD} - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad (14)$$

where  $V_{THN}$  is the threshold voltage for the NMOS device,  $V_{THP}$  is the threshold voltage for

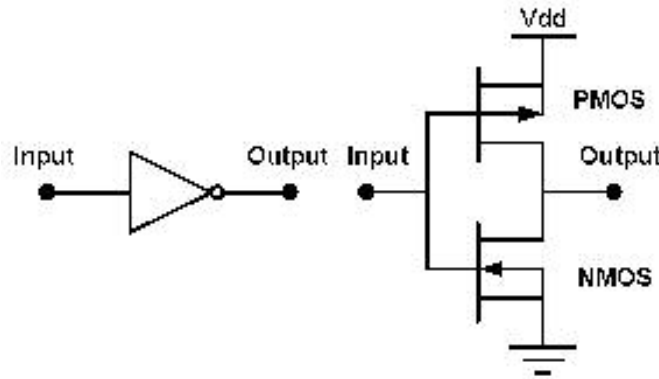


Figure 9. Equivalent representation of a CMOS inverter: (a) block diagram representation and (b) circuit diagram.

the PMOS device, and  $V_{DD}$  is the power supply voltage. The size characteristics of the MOS structures are included in  $\beta_n$  and  $\beta_p$  and defined as:

$$\beta_n = \mu_n C_{ox} \frac{W_n}{L_n} \quad \beta_p = \mu_p C_{ox} \frac{W_p}{L_p} \quad (15)$$

where  $\mu_n$  and  $\mu_p$  are the mobility of the minority carriers in the n- and p- doped concentrated regions, respectively,  $C_{ox}$  is the capacitance of the gate oxide,  $W_n$ ,  $L_n$ ,  $W_p$ , and  $L_p$  are the gate widths and lengths of the NMOS and PMOS devices, respectively [18].

If the devices have equal threshold voltages, and have physical dimensions and mobility such that  $\beta_n = \beta_p$ , then the switching voltage will be equal to  $V_{dd}/2$ . In most devices this is not the case, where it is difficult to determine the mobility of the NMOS and PMOS devices, which is directly proportional to doping levels, and then to scale the dimensions for the mobility offset.

With advancements in circuit design today, additional circuitry is designed to improve noise immunity, to offset the switching voltage and in some cases give the circuit a hysteresis in the switching voltage as in Schmidt Trigger devices. Also for increasing the signal to noise ratio and noise rejection of the circuit, input and output buffer stages are usually added to a circuit [19]. Buffer stages are common in every type of digital logic circuit and one buffer stage is normally a single inverter stage (Figure 10).

Based on the information on CD4xxxB Series logic devices, buffered gates offer a large noise margin, constant output impedance, large AC gain, lower input capacitance, while the unbuffered have faster propagation delay, larger AC bandwidth and not susceptible to output oscillations [19]. The buffer stages provide large DC gain between stages leading to defined transition voltages and faster transition times.

Output oscillations have been observed in buffered logic devices when a slow rising voltage is applied to the input of the circuit, where this effect was not observed in circuits that were unbuffered. Logic manufacturers set limitations on the edge characteristics of logic pulses to prevent excitation of these oscillations.



Figure 10A block diagram of a device under test with input and output inverter buffer stages.

Another method of preventing undesired noise is by using more complex topologies such as “bus hold circuitry” and Schmitt triggers, which uses additional MOSFET stages to provide feedback to input stages to clamp them to desired logic state [20]. Although all of these types of additional circuitry exist and are implemented a large majority of the devices tested they will not be considered in the following analysis and simulations. Simple models of CMOS inverters will be considered including buffer stages and ESD topologies based on datasheets found on the logic circuits.



## CHAPTER 3 RF INJECTION EXPERIMENTS

### 3.1. Introduction

Direct injection and irradiation experiments are the two types of experiments commonly used for determining the effects of electromagnetic radiation in electronics. Direct injection experiments have the advantage of being able to couple the most power into a specific point in a circuit, to exactly know how much power is incident to the device under test, but has the disadvantage of creating a fictitious circuit environment to determine the effects. Irradiation experiments have the advantage of not altering the circuit under test and keeping the integrity of the circuit testing environment as ideal as possible. The disadvantages to irradiation include the requirement for higher power levels, antenna patterns changing with frequency, near-field ambiguities, and difficulties in calculating the exact amount of power incident to a circuit or transmission line.

Direct injection experiments were chosen to determine exactly how much power was required to cause an effect in the DUT. This method can be used to measure precisely how much power is incident to, reflected from and transmitted into the DUT. By using a power coupler, the incident and reflected RF power is measured and the transmitted power calculated from these values. However, this setup can incorporate an unrealistic circuit environment due to loading effects at the injection point.

#### *3.1.1. Experimental Setup*

The equipment setup for the injection experiments followed the basic construction demonstrated in the block diagram of Figure 11 with an RF source fed into an amplifier leading to a bias-tee circuit coupled into the input of the DUT. An oscilloscope was used to measure the induced voltages at the input in between the RF choke of the bias-tee and a pull-up resistor. The output was loaded by a load resistor, which was used to measure changes in the output voltage by an oscilloscope or to determine RF feedthrough by a spectrum analyzer. Because of the variety of experiments performed, the following sections will indicate the specific equipment used for measurement of interest. One consideration to take into account when performing RF injections experiments is the effect the measuring equipment has on the operation of the circuit and in the measurements themselves.

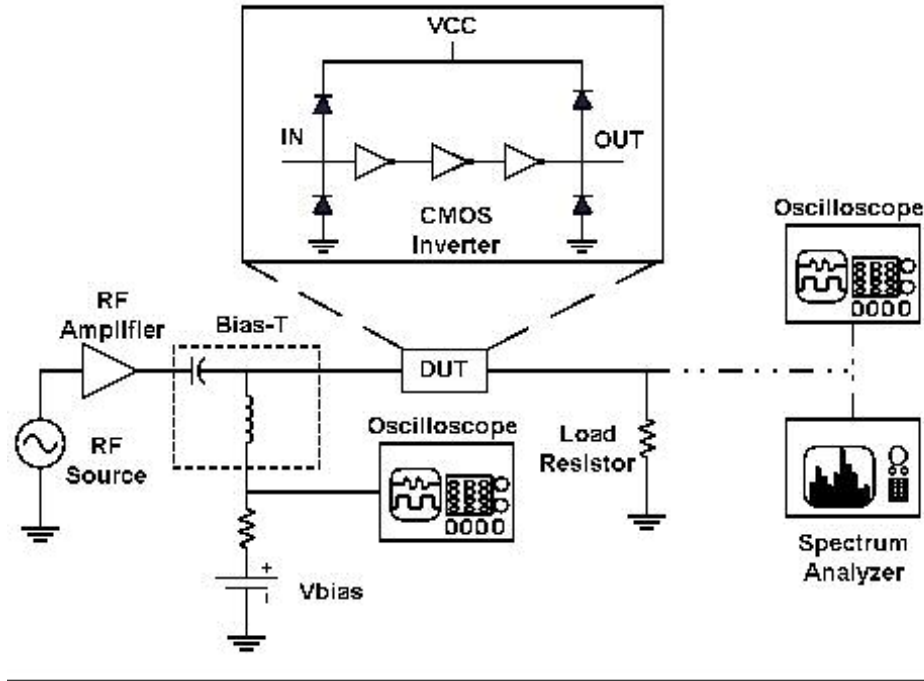


Figure 11. Block diagram for injection testing, including bias-tee and blow-up of device under test as a buffered inverter with ESD components.

### 3.1.2. Loading Effects on the input circuit

Loading problems arise from introducing a direct injection point into a circuit. In an ideal RF injection situation, the circuit under test would be operating under normal circumstances, being a circuit in a series or parallel with other circuits, with RF coupled into the input of the circuit with no change in normal performance of the digital device due to the RF transmission line. In previous direct injection experiments [1]-[10], a bias-tee or a DC-blocking capacitor was used for electromagnetic coupling (Figure 11). In these two cases, the electromagnetic signals were capacitively coupled into the input of the DUT to determine effects.

The coupling capacitor and the impedance of the RF injection transmission line create a single pole high pass filter. If the induced signal at the input of the circuit contains frequency components, which are above the cutoff frequency of the high pass filter, the signal can shunt through the capacitor and be loaded down by the RF transmission line. However, using too small of a value for a capacitor could result in an AC voltage divider between the coupling capacitor and the capacitance of the ESD protection circuits and the input capacitance of the CMOS inverter.

A high-pass filter (HPF) may be used to couple the RF into input of the circuit reducing the loading effects. By increasing the number of poles in the transfer function of the filter (coupling capacitor), the impedance seen at the lower frequencies will be higher and closer to an open circuit, and still pass through the RF frequencies as if it were a matched load (Figure 12).

The DC port of a bias-tee is normally a single inductor. The inductor and the impedance of the transmission line form a single pole low-pass filter (LPF). For DC probing the input of the device, the frequency components of the input DC voltage must be lower in frequency than the cutoff frequency of the LPF. If this is not the case, the signal being probed will look distorted on an oscilloscope, with a inaccurate representation of the rise time, rectified voltage level, pulse width and the fall time of the induced voltage pulse.

One way to avoid the loading problems of the bias-tee is to replace it with multi-pole high-pass and low-pass filters (Figure 12). A high-pass filter with a higher corner frequency than the single capacitor filter and a much steeper roll-off will match the line at RF frequencies, and act like a high impedance transmission line at lower frequencies. A low-pass filter will require a corner frequency high enough to allow the frequency content of the pulse envelope to be measured, while looking like a high impedance transmission line to the RF signal.

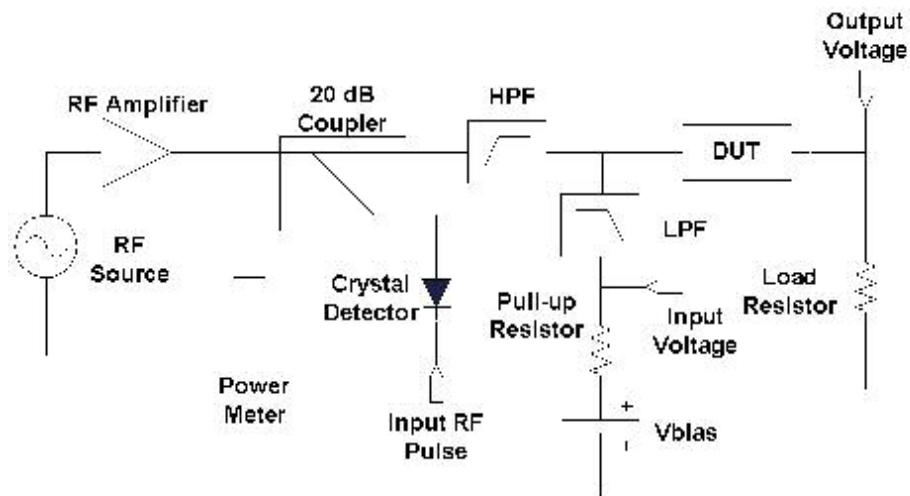


Figure 12 Block diagram for injection testing, incorporating a power coupler and replacing the bias-tee with a high-pass filter and a low-pass filter.

### 3.2. Measured Inverter Port Characteristics

Using a HP4145B Semiconductor Parameter Analyzer, the DC I-V measurements were taken of the HC, HCT, AHC, and AHCT families of inverters to determine if the inputs and outputs ESD protection showed the same diode characteristics as discussed in Section 2.3. Four measurements were taken with the first port acting as the voltage reference: ground to input (ground\_input), input to Vdd (input\_vdd), ground to output (ground\_output), and output to Vdd (output\_vdd) as demonstrated in Figure 13. The HP4145B had the upper and lower current limits set to +/- 50  $\mu$ A, respectively.

The four measurements for the 74HCT04 show the I-V characteristics have different forward and reversed biased attributes (Figure 14). The measurements demonstrate the forward conduction region has a turn on voltage around 0.4-0.7 volts for the ground\_input, input\_vdd, and output\_vdd, and a turn on voltage of 0.1 volts for ground\_output. The reverse biased voltage sweep indicated low reverse breakdown voltages between -0.75 and -2.5 volts. The differences can be attributed to the topology of the ESD protection device as well as to variations in manufacturing the semiconductor.

The I-V characteristics indicate p-n junctions are present at the four measurement points, which supports the hypothesis of the ESD protection devices being the RF rectifiers. Measurements for the 74HC04, 74AHC04, and 74AHCT04 circuits are located in Appendix B. In certain cases such as the 74AHC04, the measurements indicated a p-n junction was not located at a specified port.

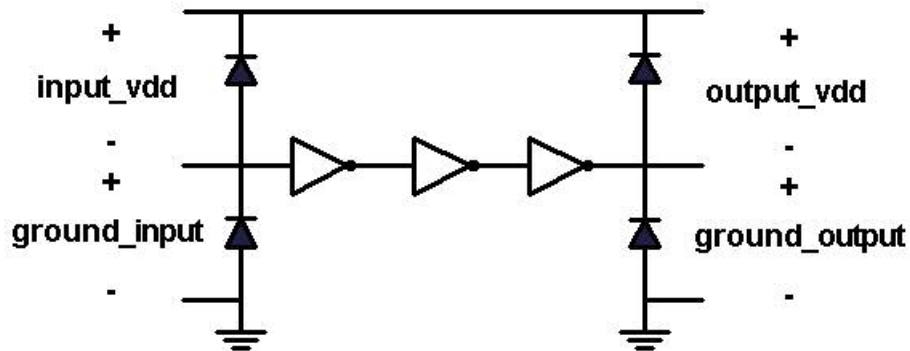


Figure 13. Block diagram of the locations of measurements taken on a HP4145B Semiconductor Parameter Analyzer to measure the I-V characteristics of the ESD protection devices.

To determine the input impedance of the CMOS devices, a HP8722D Vector Network Analyzer (VNA) was used to record the  $S_{11}$  parameters of the HCT, ALVC, LVC, and LVX CMOS inverters. The frequency range of the VNA was set from 50 MHz to 2 GHz for all the devices. The circuits were setup without power to the  $V_{dd}$  pin in order to test the characteristics of the lower ESD diode.

Since the ESD protection circuit contains a voltage dependent capacitance, we were interested in comparing the differences between the input impedance for the low and high logic states to determine the effects of the change in input bias voltage. A DC bias voltage was coupled into the VNA through the bias voltage port while the frequency response was measured for a series of input bias voltage levels. The input impedance test of LVC demonstrates a series resonance in the impedance dependant on the bias voltage (Figure 15a). A shift in the resonant frequency between the low (red) and high (black) state is approximately 125 MHz (Figure 15).

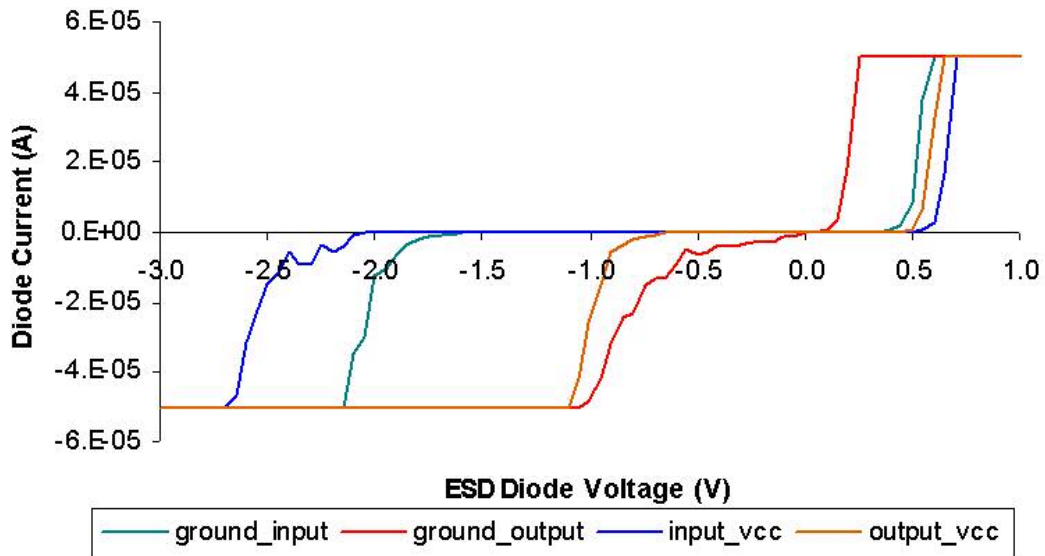
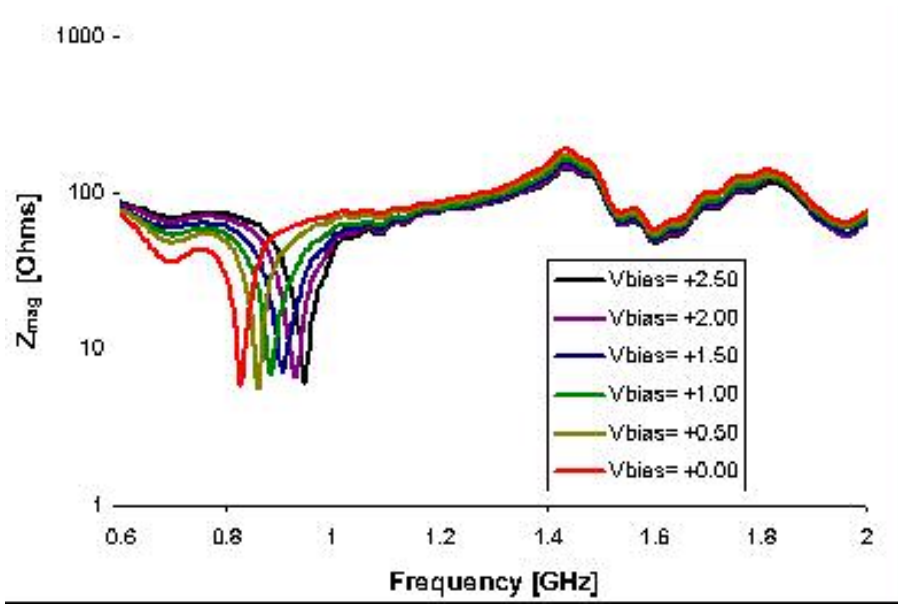
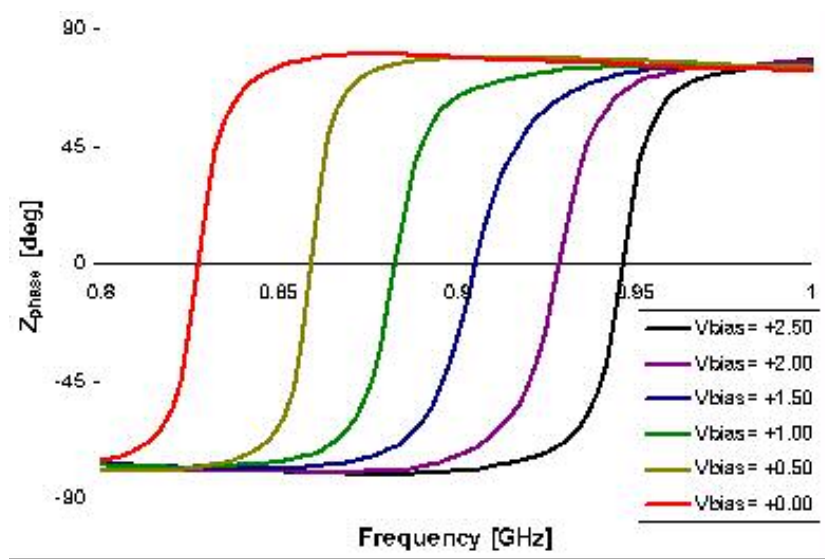


Figure 14I -V characteristics of input and output ESD protection circuits for 74HCT04. Measurements were taken between ground and the input signal line (ground\_input), between the ground and output signal line (ground\_output), between the input signal line and the power supply line (input\_vdd), and between the output signal line and the power supply line (output\_vdd).



(a)



(b)

Figure 15 Input impedance of 74LVC04 in (a) magnitude and (b) phase with respect to frequency and input bias voltages from 0.0 to 2.5 volts in 0.5 volt increments.

The input impedances for the other circuits tested are in Appendix D. Dips in impedance are associated with a resonance caused by an inductance and a capacitance in series. The resonant frequencies for the ALVC, HCT, LVC, and LVX are in Table 1 for the low and high logic state voltages, and a power supply voltage of 3.0 volts.

In later injection experiments, the input resonant frequency was found to decrease in certain circuits after the power supply was connected back up to the circuit. The change in the resonant frequency can be explained by the influence of additional capacitances contributed by other ESD protection components. This influence on the input resonance frequency is discussed further in Section 4.3.1.

To determine the DC I-V characteristics of the lower ESD diode, the CMOS inverter was setup with the power supply pin floating. A bias voltage was applied across the ground to the signal line with a Agilent 34401A 6 ½ Digital Multimeter in series with the power supply in order to measure the current. The input bias voltage was swept in 5 mV steps measuring the current at each interval. The I-V measurements for the LVX are shown in Figure 16 using Eq. (1) to calculate the saturation current to be 5 pA and the ideality factor n as 1.05.

Table 1. Resonant frequencies for the HCT, ALVC, LVC and LVX logic families with respect to input bias voltage. All the devices had a power supply voltage of 3.0 volts.

Logic Family	Low Bias		High Bias	
	Voltage [V]	f <sub>0</sub> [MHz]	Voltage [V]	f <sub>0</sub> [MHz]
HCT	0	940	3	1080
ALVC	0	850	2	993
LVC	0	825	2.5	947
LVX	0	1350	2.5	1450

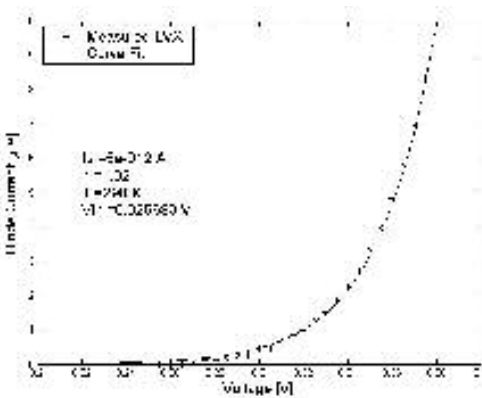


Figure 16. A plot showing the I-V characteristics of the lower ESD diode in a LVX CMOS inverter. The data points were fit with the curve generated using Eq. (1) to determine the saturation current ( $I_s$ ) and ideality factor ( $n$ ).

The input capacitance of a CMOS inverter was calculated by using the S-parameters as measured by the VNA. The high frequency small signal impedance for various bias voltages was measured by recording the S-parameters at each step of increasing voltage. Again the LVX inverter was measured with no power supply voltage applied and the  $V_{dd}$  pin floating. By using the Smith chart display on the VNA, the input was seen to be most capacitive in frequencies around 100 MHz. We wanted to measure the impedance as far away from the input resonance to determine the value of the capacitive element without the effects of other parasitic elements influencing the measurements. The bias voltage was limited to 1.5 volts because of the rapid change in the frequency response due to device beginning to conduct. A small band of frequencies were used to average the values of the capacitance to eliminate noise and fluctuations in the measurements. Using Eq. (11), a curve was generated to match the data points as close as possible (Figure 17) calculating  $C_{j0}$  to be 3.6 pF, the built in potential to be 0.7 volts, and the emission coefficient to be equal to 0.18. Deviations from the curve are most likely due to the effects of the gate capacitances and the capacitance of the upper ESD diode.

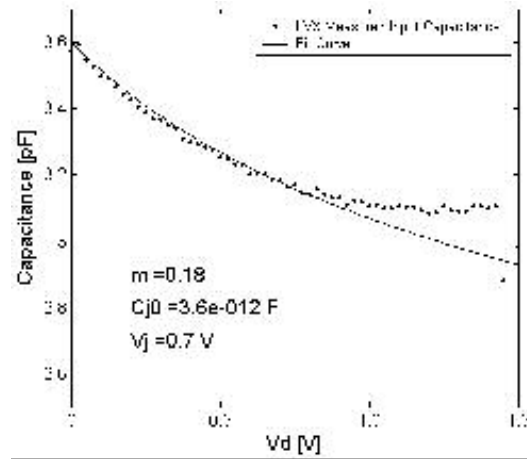


Figure 17. the input capacitance parameters of the p-n junction of the lower ESD protection circuit in a LVX CMOS inverter

### 3.3. Observed RF Injection Effects

The observed effects of the RF pulses injected into inverters varied with every logic family, which included a full state change, partial state change (output voltage shift), state changes with a the output voltage switched after the RF pulse width has terminated, RF



amplification, and induced oscillations. This section covers at least one example of each of these cases with additional examples located in appendices where indicated.

Table 2. Susceptibility in tested logic families according to input in the low or high state. The V<sub>dd</sub> used for the logic families were either 3.3 V (\*) or 5V.

Logic Family	Input Biased Low	Input Biased High
HC		✓
HCT	✓	✓
AC		✓
ACT	✓	
AHC		✓
AHCT	✓	✓
LVC*	✓	✓
ALVC*	✓	
VHC*	✓	✓
LCX*		✓
LVX*		✓

### 3.3.1. Threshold Power Level Experiments

Threshold power levels of pulsed RF signals to cause a state change in the CMOS inverters were measured to determine the susceptibility of the devices with sweeps in the RF signal frequency, power supply voltage, and input bias voltage. The circuit setup for all the circuits tested followed the block diagram in Figure 11. The equipment used for these experiments was a HP 83731B signal generator for the RF source, a HP 83020A RF amplifier, a Mini-Circuits ZFBT-6G bias-tee, a Tektronix TDS-620 Oscilloscope, and a Tektronix P6243 FET probe.

Experiments were performed to determine the susceptibility of several different CMOS inverter logic families with the input DC bias levels in the nominal output voltage of a previous inverter stage for the low (V<sub>ol</sub>) and high (V<sub>oh</sub>) logic states. The devices that were considered susceptible produce a state change at the output, while those that were not susceptible may have shown other effects such as a bias level shift. Threshold power levels

were recorded when the oscilloscope detected a voltage change at the output of the inverter, which exceeded the switching voltage of the device.

As an example of device susceptibility, pulsed RF signal injection into the 74HCT04 device was performed when the input voltage level was in the low and high states. Susceptibility was demonstrated in both input logic states with as little as 0 dBm in the low state (Figure 18). Fluctuations in the plots are due to transmission line and impedance mismatches at the injection point. The threshold levels for the input low logic state show a 20-25 dB difference between the susceptibility of the device when in the input high logic state. The slope of the threshold power levels in the input low logic state is +40 dB/decade, and the average slope of the power levels in the input high logic state seems to remain constant over the entire frequency band. The RF pulse had a pulse width of 100ns and PRI of 1.0 ms for all frequencies.

Plots for threshold power levels for the remaining devices listed in Table 2 are supplied in Appendix D. All the plots showing susceptibility with power versus frequency had the relationship of increased required threshold power level with increasing frequency. Most of the devices (particularly the HCT, ACT, AHC, AHCT, LVC, LCX, LVX and VHC) demonstrated a +40 dB/decade slope in the threshold power levels with respect to frequency, which corresponds to a  $1/f^2$  relationship. In the plots where state changes were not observed, the amplifier had reached its output power limit (~1 watt) before an effect occurred and was recorded as +30 dBm.

The power level of the RF signal required to induce a state change in the 74HCT04 decreased by 5 dB as  $V_{dd}$  was decreased from 5V to 2 V (Figure 19). The RF pulse had a pulse width of 100ns and PRI of 1.0 ms for all frequencies. From Eq. (14), the switching point of the inverter was shown to be linearly dependent on the power supply voltage, which would require a smaller amplitude RF signal to cause an effect. These curves indicate circuits operating at operating in the lower limits of their power supply range and as circuits powered by smaller power supply voltages will be much more susceptible to upset from RF pulses.

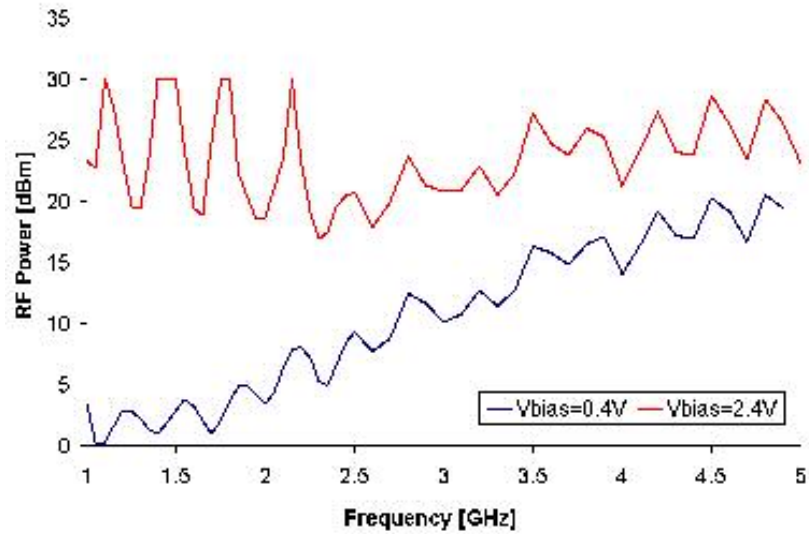


Figure 18. RF power level threshold required to cause state change in 74HCT04 with input biased at  $V_{ol}$  ( $V_{in} = 0.4$  V, in blue) and  $V_{oh}$  ( $V_{in} = 2.4$  V, in red). The RF pulse had a pulse width of 100ns and PRI of 1.0 ms for all frequencies.

To determine the susceptibility of the 74HCT04 inverter with respect to input bias voltage, another set of injection experiments were performed. An RF signal with a frequency of 1.2 GHz, pulse width of 100 ns, and PRI equal to 10 ms was injected into the HCT inverter, recording the RF power threshold levels for different input bias voltages. Experiments were done with the power supply voltage set to 3, 4, and 5 volts (Figure 20). The difference in required power levels to cause a state change was on the order of 8 dB between the cases of the power supply set to 3V and 5V.

RF threshold power levels were measured for the 74AHC04 and the 74AHCT04 for three different power supply voltages with in the operation parameters of the inverters and varying the input bias voltage. In the case of the 74AHC04, the device was most susceptible when the circuit was biased in the high logic state, and for the 74AHCT04 the device was more susceptible when biased with a low logic state. In each of these devices, the switching voltage was measured for each of the power supply voltages (Table 3). The threshold power levels were measured for different values of the input bias level and for the power supply voltages of 3, 4 and 5 volts. The comparison of these three curves for the two different devices in Figure 21 and Figure 22 for the 74AHC04 and 74AHCT04, respectively. These plots show the amount of power required to induce the same voltage

difference for all three power supply values are identical. This implies the rectification of the RF to induce the required voltage to cause the devices to switch is not dependent on the power supply voltage.

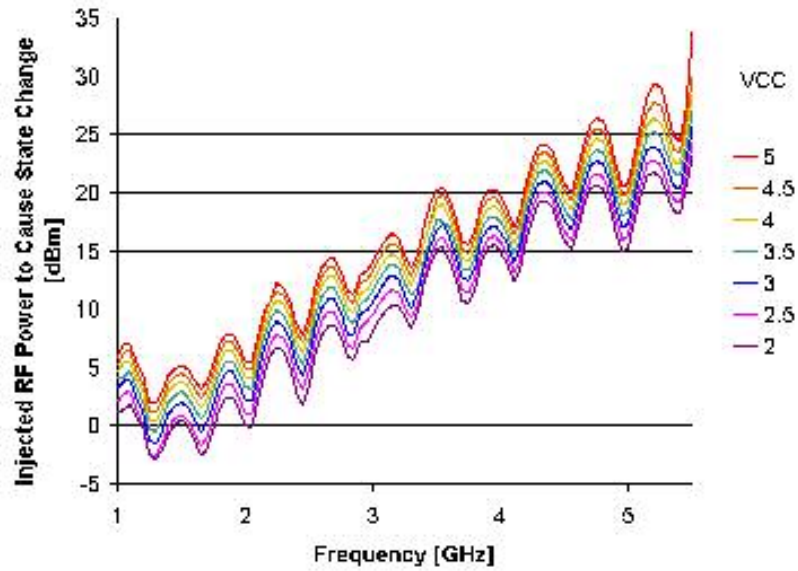


Figure 19 RF threshold power to cause a state change in 74HCT04 with various values of Vdd. The RF pulse had a pulse width of 100ns and PRI of 1.0 ms for all frequencies.

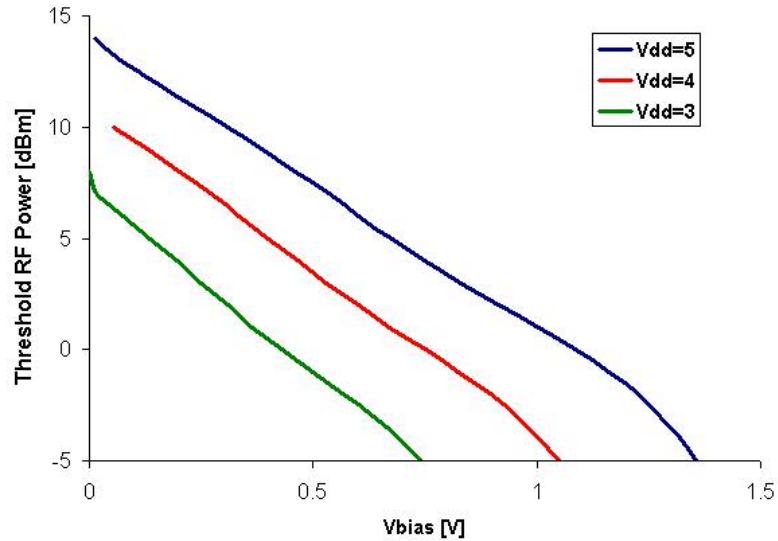


Figure 20. RF Power threshold to cause state change in 74HCT04 with varying Vbias (f=1.2GHz PW=100ns PRI=10ms). Input state was set to Vol.

Table 3. Switching voltages for the 74AHC04 (biased with Voh) and 74AHCT04 (biased with Vol) with power supply voltage was set to 3, 4 and 5V.

Device	Switching Voltage [V]		
	Vdd = 3V	Vdd = 4V	Vdd = 5V
74AHC04 with Voh	1.4	1.9	2.4
74AHCT04 with Vol	1.5	1.3	1

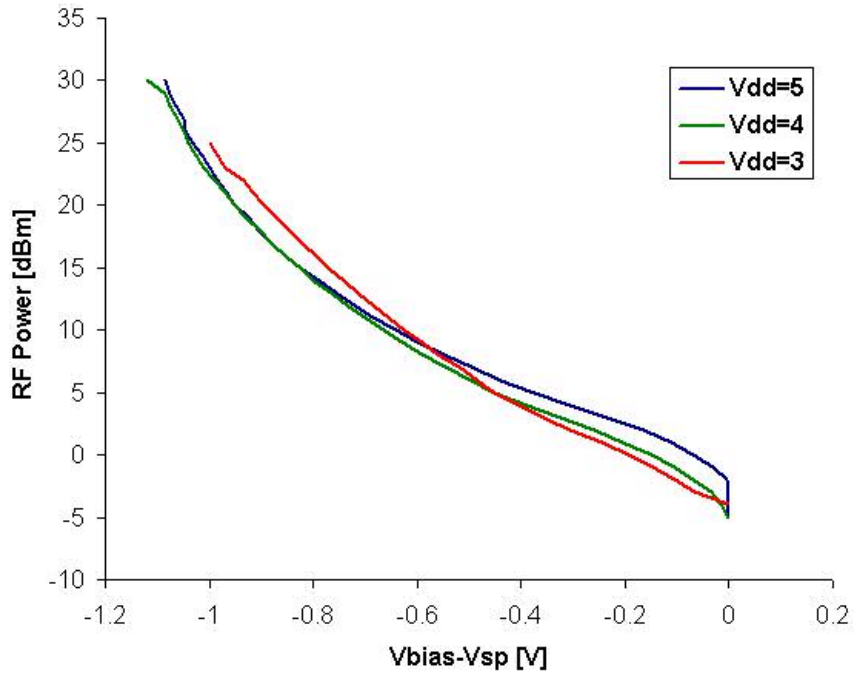


Figure 21 Peak RF power of pulse modulated signal ( $f=1.5$  GHz,  $PW=100$ ns,  $PRI=10.0$ ms) required to cause a state change in a 74AHCT04 with increasing bias towards switching voltage. Input state was set to Vol.

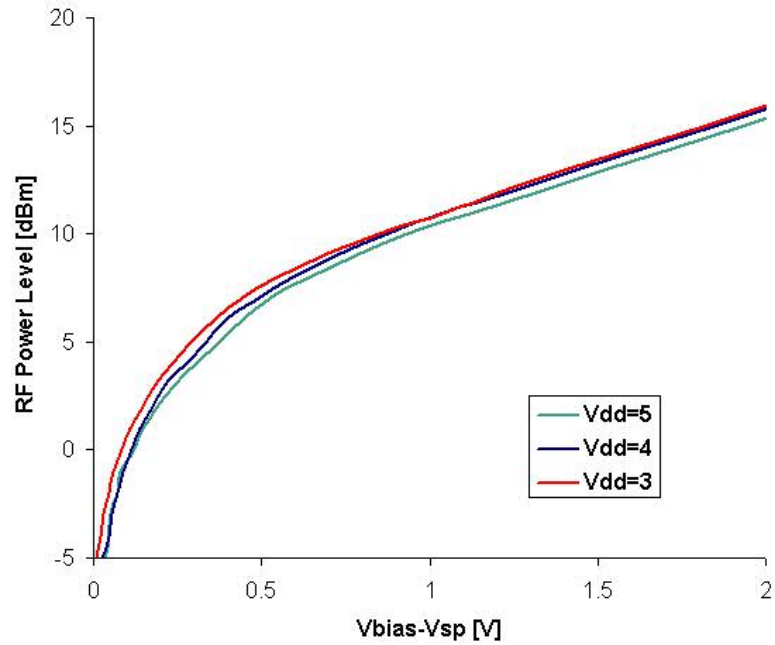


Figure 22 Peak RF power of pulse modulated signal ( $f=1.5$  GHz,  $PW=100$ ns,  $PRI=10.0$ ms) required to cause a state change in a 74AHC04 with increasing bias towards switching voltage. Input state was set to Voh.

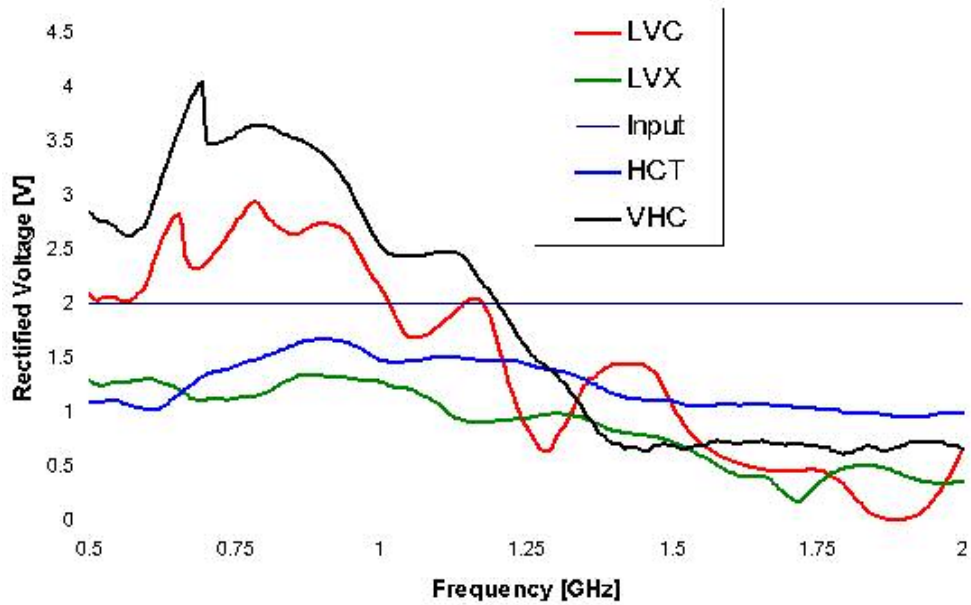


Figure 23. The measured rectified voltages for the LVC, LVX, HCT and VHC CMOS inverters. The RF amplitude was kept constant at 2V.

To determine the frequency dependent rectification sensitivity for a series of logic families, the devices were injected with a constant RF voltage of 2 volts and swept over 500 MHz to 2 GHz. Figure 23 compares the rectified voltages measured for the LVC, LVX, HCT, and VHC CMOS inverters. In the case of the VHC, the induced voltage exceeds the RF amplitude reaching a peak of 4 volts over the frequency range of 500 MHz to 1.2 GHz. Similarly, the LVC device exhibits RF to DC conversions above unity from 500 MHz to 1 GHz. The HCT and LVX had transfer curves more expected of rectification, with a RF signal to DC induced voltage conversion less than unity. The transfer curves of the VHC and LVC devices indicate RF gain occurs within the device allowing for a larger induced rectified envelope voltage.

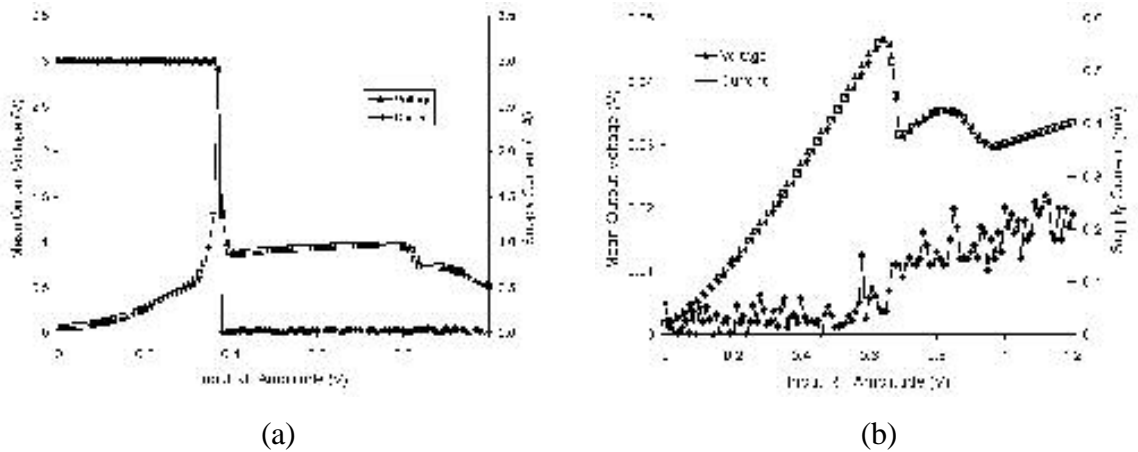


Figure 24. The DC output voltage and DC power supply current of 74HCT04 CMOS inverter due to RF signal with a frequency of the input impedance resonance injected for (a) a low bias of 0.5 V and (b) a high bias of 2.0 V.

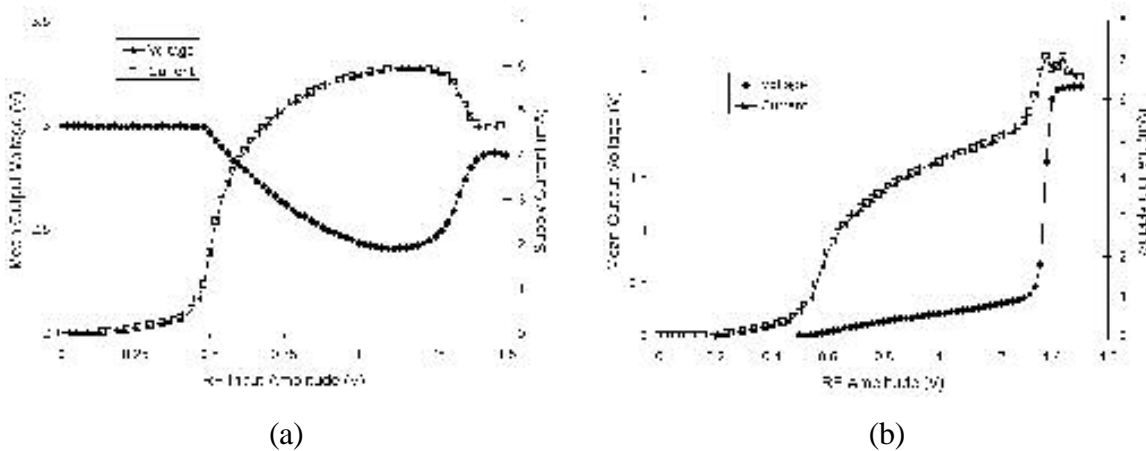


Figure 25 The DC output voltage and DC power supply current of 74LVX04 CMOS inverter due to RF signal with a frequency of the input impedance resonance injected for (a) a low bias of 0.5 V and (b) a high bias of 2.0 V.

Measurements of the power supply current give insight into the effects of RF on the MOSFETs. Since the source of the PMOS devices are all connected to the power supply line, fluctuations in the current can indicate the time when switching occurs in the devices. An experiment injecting RF pulses into a 74HCT04 and a 74LCX04 device biased in a low and high logic state, showed power supply current shifts correlating to measured output voltage changes (Figure 24 and Figure 25).

The RF frequency in this was set to the zero bias input impedance resonant frequency of 1.35 GHz as determined in Section 3.2. The current measurements were taken by increasing the duty factor of the pulse modulated RF signal. Care was taken to ensure thermal effects did not contribute to deviations in measurements of the rectified voltage signal as power supply current was measured. The current variations showed a linear relationship with the changes in duty factor. The average current measurements were divided by the duty factor ratio to give the peak power supply current.

Application notes on various logic families indicate these current spikes are very common but different in magnitude from device to device [21]-[25]. These spikes are indicators the MOSFETs are operating in a Class A configuration as the input bias voltage nears the switching point.

When the input was biased low and the RF frequency was set to 940 MHz, a large current spike was measured as the output of the 74HCT04 switched from high to low with increasing RF amplitude as seen in Figure 24a. A small increase in current was measured with a very small shift in the output bias voltage when the inverter was biased in the high logic state (Figure 24b).

The power supply current exhibited an increase in LVX CMOS circuit in both the low and high bias cases. Figure 25a shows the current in the low bias increase and with changes in the output voltage, however leveling off and decreasing after a RF voltage of 1.25 volts was reached. For the experiment when the LVX was biased high, the current dramatically increased when the output voltage began to shift, finally peaking at the moment the output voltage latched to the high state (Figure 25b).



### 3.3.2. RF Gain

RF feedthrough was observed to appear on the voltage at the output of the inverters tested. Bandwidth limitations of the Tektronix TDS 620B oscilloscope used for measurements limited direct measurement of the RF signals when attempting to view RF pulses with for large periods of time compared to the cycle time of the injection frequency. The voltage detected resulted in aliased voltage readings with frequency components consisting of the difference between the injection frequency and the sampling frequency of the oscilloscope. One method of measuring the RF voltage at the output was to set the oscilloscope to the maximum setting of allowable sample points, zooming into a region where RF was believed to be present, and set the oscilloscope the highest sampling rate. For the TDS 620B the highest sampling rate is 2.5 Gs/s for four channels.

Figure 26 and Figure 27 plot the relations of measured output RF voltage to the amplitude of the injected RF signal for the HCT and LVX inverters, respectively, when the inputs are biased in the low and high logic states. The input RF amplitudes for these plots were determined by the voltage display option on the Agilent E4438C Vector Signal Generator. The logic state dependent input impedance resonance frequencies were used as the injection frequencies for the two CMOS devices.

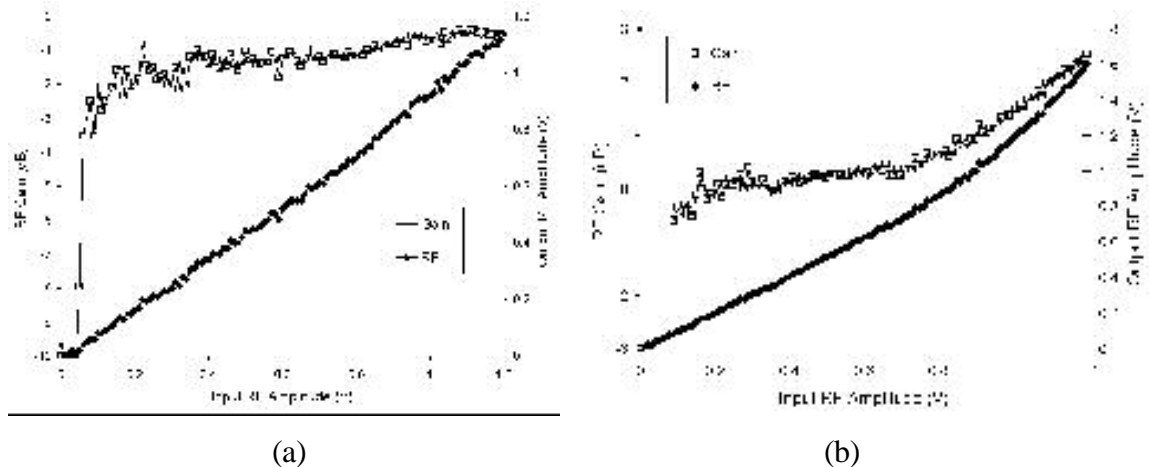


Figure 26 RF gain and output voltage due to RF signal with a frequency of the input impedance resonance for HCT CMOS inverter when the input had a (a) low bias level of 0.5 V and a (b) high bias level of 2.0 V.

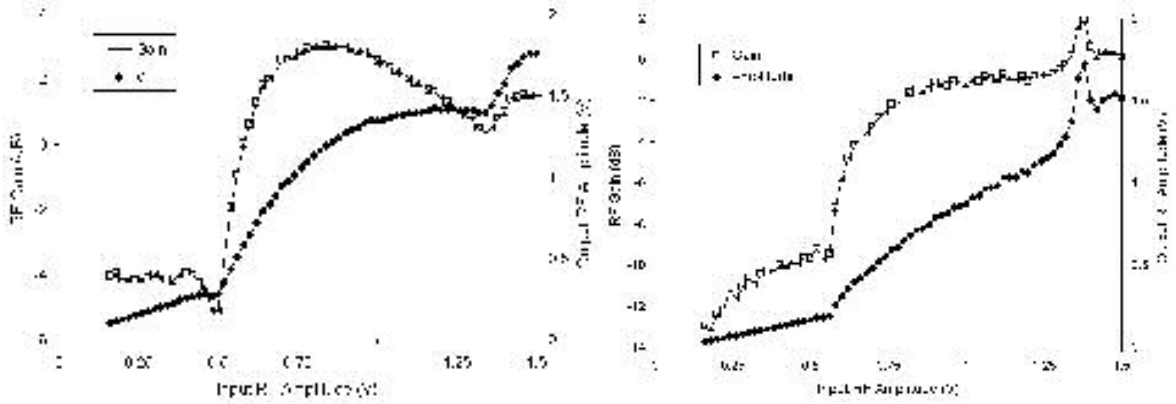


Figure 27. RF gain and output voltage due to RF signal with a frequency of the input impedance resonance for LVX CMOS inverter when the input had a (a) low bias level of 0.5 V and a (b) high bias level of 2.0 V.

A linear response was measured for the low-bias RF gain measurement for the HCT device for the sweep of RF input amplitude from 0 to 1.2 volts, which indicated a small amount of attenuation through the CMOS inverter. When biased in the high logic state, the inverter shows a linear response to 0.8 volts, where the gain of the RF reaches a peak of 2 dB at 1.2 volts. Since the zero-bias resonant frequency for a single diode was used, the most likely explanation for the observed behavior is the resonant frequency was lower than originally thought due to the influence of the upper ESD structures. This would explain the linear less than unity gain in the low bias case, and also the nonlinear increase in high biased case. The injection frequency for the latter case could have been slightly above the input resonant frequency, and as the induced input voltage increased, the resonant frequency also increased changing the RF gain characteristics of the inverter.

Similar arguments could be made for the two gain curves measured in the LVX circuit. The resonant frequency in the low bias case could have been lower than the injection frequency, until the induced voltage caused the resonant frequency to increase up to and past the injection frequency. The gain of the circuit would be highest when the frequencies coincided and began to decrease as the resonant frequency continued to increase.

### 3.3.3. Full State Change

The full state change is characterized by the output of the device changing from a logic low state to logic high state, or vice versa, with a strong correlation to the time the RF

pulse is propagating through the circuit. The output voltage during a full state change looks like a normal DC pulse has caused the device to switch, but has changed state at the same time and for the approximately the same duration of the pulsed RF signal. As indicated in Section 2.3, rectification of a RF pulse induces a DC and a low-frequency voltage signal at the input of the first buffer stage causing it to switch. The switching action of the buffer stage then activates the remaining string of inverters normally, creating a voltage change at the output of the device corresponding to the modulation of the injected RF signal.

The HCT inverter was one device that demonstrated full state changes due to RF pulses. As the power levels were increased while testing the 74HCT04, the output voltage pulse width was observed to change with respect increasing power. Above a certain power level, it was possible to cause the pulse width of the output voltage to exceed the pulse width of the injected RF pulse. Figure 28 shows an example where a 1.0 GHz RF signal has a pulse width of 100 ns, PRI of 10.0 ms and a power level large enough to cause the output voltage to have switched states for 180 ns.

Measurements of the output voltage showed changes with increasing power between difference of the rising edge of the RF pulse envelope and the falling edge of the output voltage, which is defined as the leading edge delay. Likewise time differences between the falling edge of the RF pulse envelope and the rising edge of the output voltage, called the trailing edge delay, were also observed to change with RF power levels.

The measurements of the leading edge delay, trailing edge delay and output pulse width from varying the power levels of an injected RF signal at 3.8 GHz, pulse width of 200 ns, and a PRI of 10.0 ms are displayed in Figure 29. With the exception of the dip in the curves between 23 and 25 dBm, the leading edge delay decreases exponentially with an asymptote near 40 ns and the trailing edge delay looks linear. The output pulse width exceeds the injected RF pulse width off 200 ns approximately at the power level of 26.5 dBm.

A measurement of the induced input voltage showed the classical response of a stepped response to a RC circuit, however the responses of the rising edge and falling edge responded with different RF time constants. These time constants were also observed to change with respect to the RF amplitude indicating the voltage dependent capacitances of the ESD diodes were directly involved in the response.

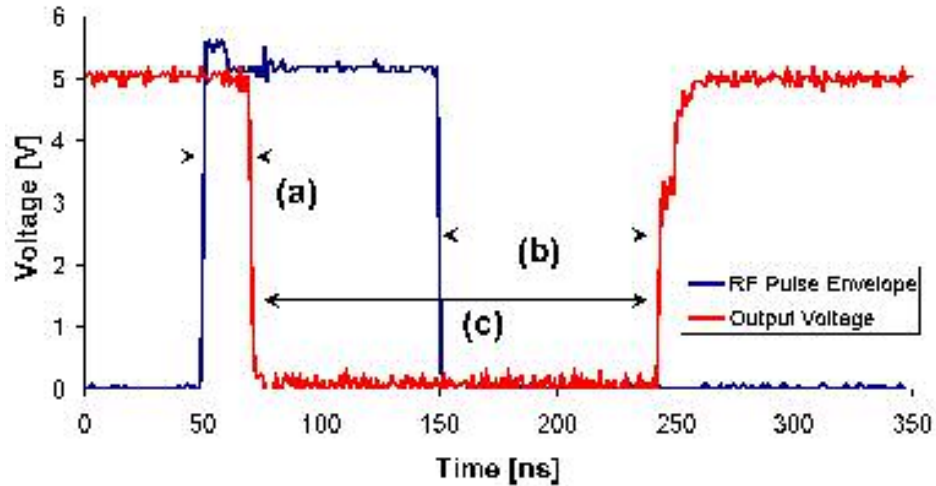


Figure 28. Time domain plot for RF injection experiment on a 74HCT04 inverter corresponding time delays between leading edge of the RF pulse envelope ( $f_0 = 3.8$  GHz, PW = 100 ns, PRI = 10.0ms) and output voltage (a), trailing edge of the RF pulse envelope and output voltage (b) and pulse width of the output voltage pulse (c).

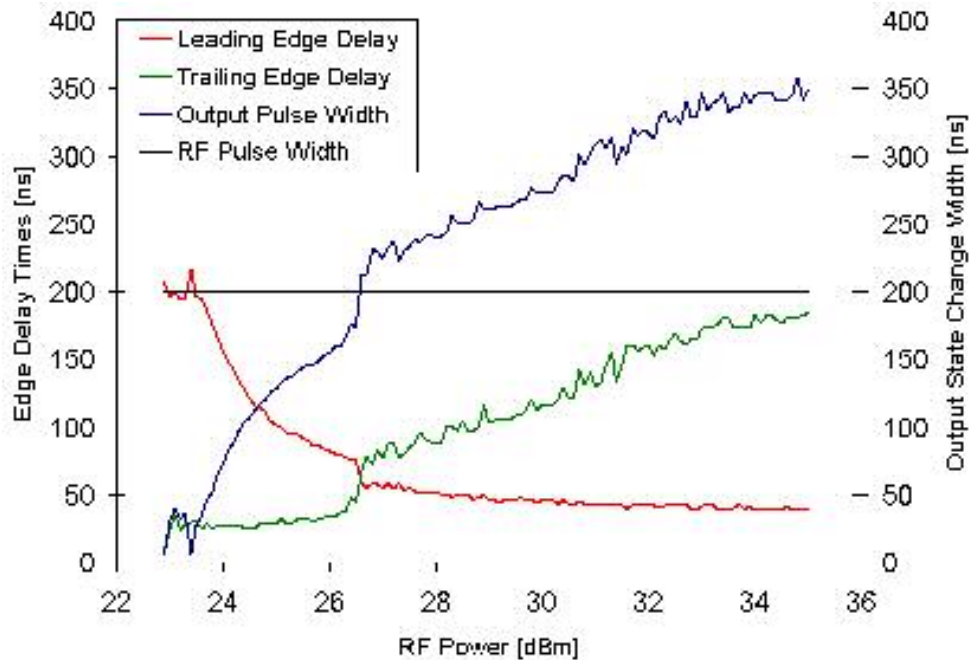


Figure 29 Delay times between the envelope of the injected RF signal and the voltage change at the output. Increasing in RF power leads to a decrease in the leading edge delay (red), an increase in the trailing edge delay (green), and the output voltage pulse width (blue) exceeding the pulse width of the injected RF signal (black).

#### 3.3.4. Partial State Change and Latent Latching

The 74HC04 inverter was a device that showed a partial shift when the input was biased with a low logic level. An Agilent 34401A 6 ½ Digital Multimeter was placed in series with the power supply to measure the changes in the current with increasing RF power during an injection experiment. The output level shift,  $\Delta V_{out} = V_{dd} - V_{out}$ , was measured with respect to RF power (the signal having characteristics of  $f_0 = 2.4\text{GHz}$ ,  $PW = 100\text{ ns}$ , and  $PRI = 10.0\text{ ms}$ ) for three different values of the power supply voltage, and graphed in comparison to the power supply current measurements in Figure 30. The induced voltage levels at the output of the inverter indicate saturation as the RF power increases. This behavior would indicate that the induced input bias level never reaches the switching point of the 74HC04 while it is biased in the in the low logic state.

In some circuits tested, a bias shift was observed during the onset of the RF pulse however switched logic states after the RF pulse ended. The 74ALVC04 CMOS inverter injection experiment was setup as Figure 11, using the same equipment as the previous section including an Agilent 8564C Spectrum Analyzer used to determine the frequency content of the output signal. The plots in Figure 31 through Figure 34, show the RF pulse envelope and power level, measures the induced voltage at the input, the resulting output voltage, and the output signal frequency spectrum. A RF signal with a pulse width of  $3\ \mu\text{s}$  and a PRI of  $100\ \mu\text{s}$  was injected into the 74ALVC with a frequency of  $850\text{ MHz}$  corresponding to the series resonance of the input impedance as described in Section 3.2. The power supply voltage was set to 3 volts, the input bias voltage was set to 0 volts, and the RF power level was swept from  $5.0\text{ dBm}$  to  $30.0\text{ dBm}$  in  $0.25\text{ dBm}$  steps measuring data at each interval. In Figure 31, a RF pulse with a power level of  $12.25\text{ dBm}$  shows the induced input voltage at the input reaching a mean just over 1 volt causing a bias shift at the output from 3 volts to 2 volts. The rise time and fall time of the input correspond to the change in capacitance of the p-n junction of the ESD diode. The output voltage also shows differences in the fall time and rise of the pulse, which varies with the increase in power as shown in the other three figures.

Sawtooth ripples are also apparent in the input and output waveforms. These are due to the effect of the RF gain of the resonant frequency in as seen in the input impedance and the rectification conversion. As the induced bias increases, the resonant frequency

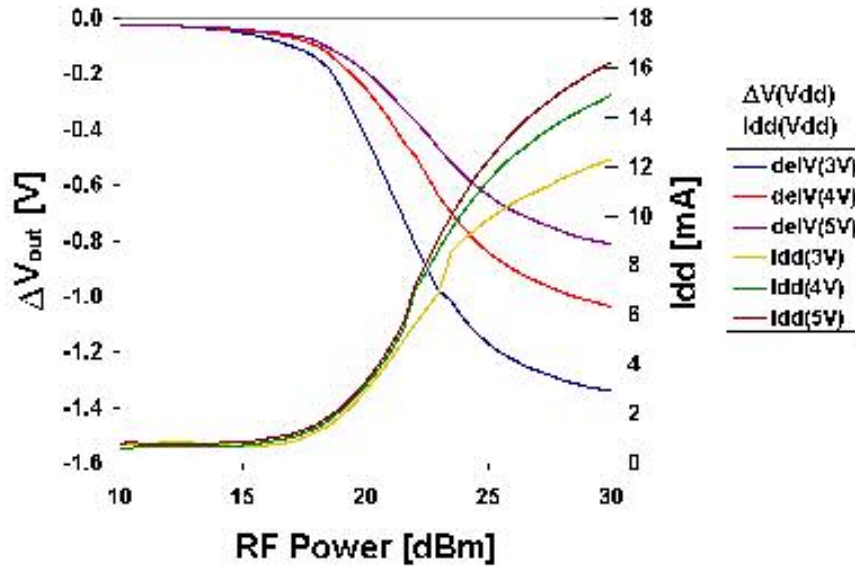


Figure 30. Output voltage and power supply current change in a 74HC04 with applied RF pulses ( $f=2.4$  GHz,  $PW=100$ ns,  $PRI=10.0$ ms) for  $V_{dd}=3,4,$  and  $5$  volts.

begins to increase as was demonstrated in Figure 15. The RF gain due to the resonance will decrease as the difference between the resonant frequency and the injection frequency increases. However, the dip in the RF gain causes the rectified voltage to decrease, allowing the resonant frequency to relax back to the zero bias resonance. These relaxation oscillations change in magnitude and frequency depending on the difference between the injection frequency and the zero-bias frequency, the RF power level, and the quality factor of the resonance.

With an increase in power to 16.0 dBm, the relaxation oscillations begin to disappear on the input and output voltages. Increases in the rise time and fall time of the induced input voltage correlating to changes in the voltage dependent capacitance and RF gains due to the resonance. The output also shows a time period approximately 250 ns long after the RF pulse has terminated to switch to the low state. This latent latch has been attributed to the input bias shift when no RF is present. The bias shift does not latch during the RF pulse period because of RF feedback and phase differences between the gate and source voltages of the MOSFETS and is discussed more thoroughly in Section 4.4.2.

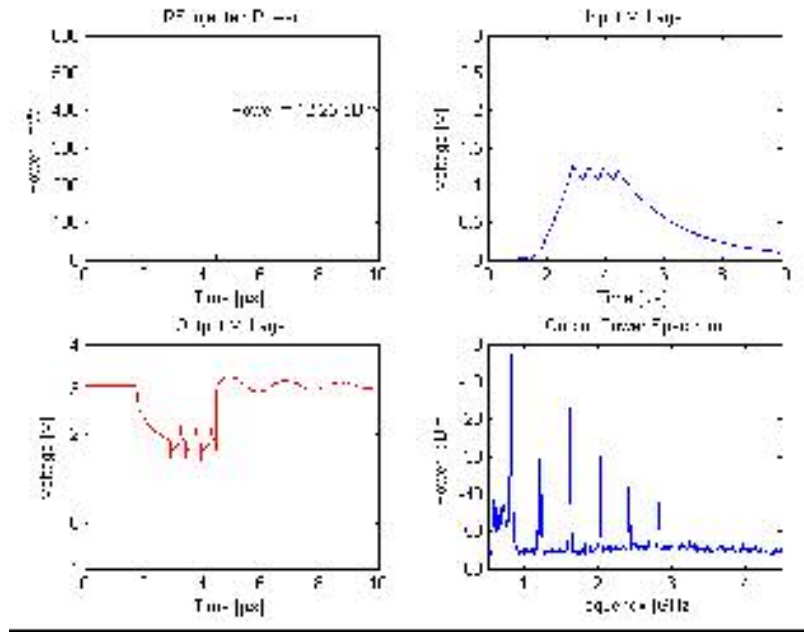


Figure 31 Results of pulsed RF (pulse width = 3 μs, PRI = 100 μs, peak power level = 12.25 dBm) injection into a 74ALVC04 inverter. The upper left plot displays the RF injected power level and pulse width. The upper right plots are the measured induced rectified voltage at the input. The lower left plot is the low frequency output voltage. The lower right plot displays the frequency spectrum of the signal detected at the output.

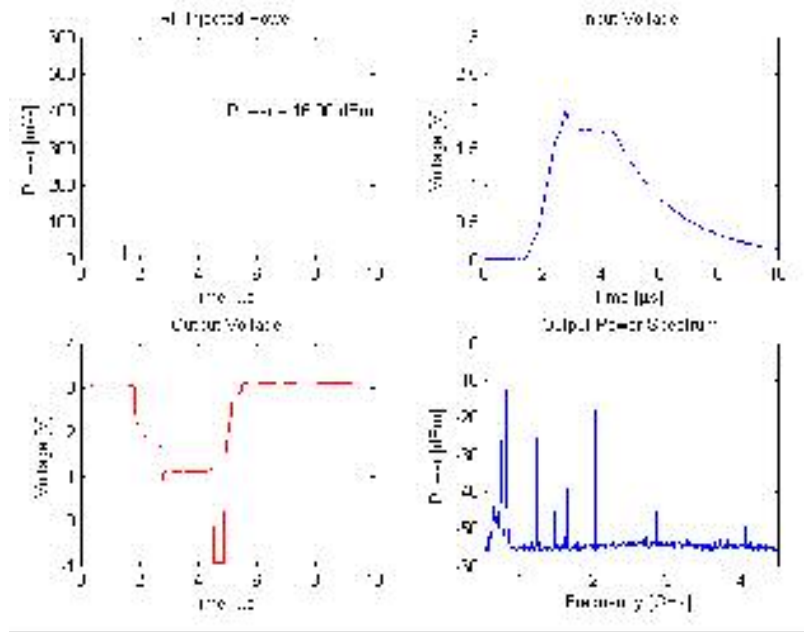


Figure 32. Results of pulsed RF (pulse width = 3 us, PRI = 100 us, peak power level = 16.0 dBm) injection into a 74ALVC04 inverter. The upper left plot displays the RF injected power level and pulse width. The upper right plots are the measured induced rectified voltage at the input. The lower left plot is the low frequency output voltage. The lower right plot displays the frequency spectrum of the signal detected at the output

In this experiment increasing the power to 21.0 dBm decreased the induced voltage, decreased the output bias shift, and eliminated the latent latched state (Figure 33). However, the rising edge of the input and the falling edge of the output voltage decreased in slope looking similar to the envelope of the RF pulse. A low-frequency oscillation due to high frequency aliasing is also present after the output voltage returns to the high logic state of 3 volts.

Finally, in Figure 34, the RF power level was increased to 24.75 dBm, displaying a jump in the induced input voltage to 2.25 volts. The output bias shifts by 2 volts during the RF pulse and indicates a latent latched state for approximately 1  $\mu$ s. The low-frequency oscillation observed in the last data slice is now more pronounced.

### *3.3.5. RF Induced Excited Resonant Frequencies*

The previous section discussed the effects of the time domain effect of a RF injection experiment on a 74ALVC04 CMOS circuit. The spectrum plots in Figure 31- Figure 34 show the frequency responses of the ALVC circuit for the four different RF signals, which consist of more than just the harmonics of the fundamental frequency. The RF injection frequency is the largest spike in all of the spectrum plots at 850 MHz. Below the fundamental frequency, a wideband grouping of low frequency spectral components were observed for all four injection power levels.

The first output frequency spectrum for the RF signal with a power level of 12.25 dBm has frequency components of the fundamental frequency, the second harmonic, the third harmonic, and low frequency components (Figure 31). Frequency signatures also exist at 1.275, 2.125, and 2.975 GHz due to the nonlinear mixing of a lower frequency component with the fundamental frequency.

A latent latch state was observed in Figure 32 when the RF power was increased to 16.0 dBm. The frequency spectrum at this power level shows the higher harmonics have disappeared almost entirely, leaving a spectrum dependent on the fundamental frequency, excited lower frequencies and frequency products from the mixing action of the ESD diode.

A spectrum rich with frequency components was measured in Figure 33. Although the power level was increased to 21.0 dBm, the nonlinear effects of circuit are clearly



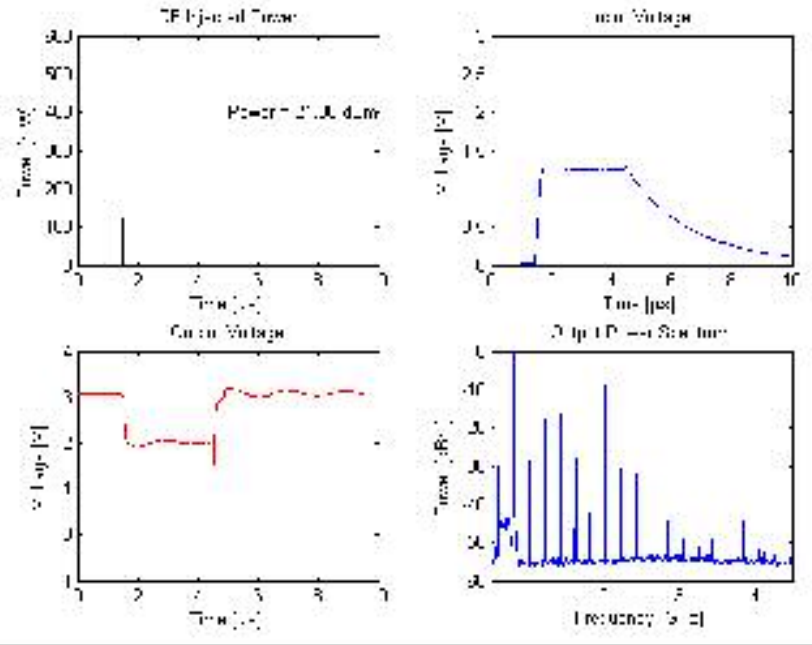


Figure 33. Results of pulsed RF (pulse width = 3 us, PRI = 100 us, peak power level = 21.0 dBm) injection into a 74ALVC04 inverter. The upper left plot displays the RF injected power level and pulse width. The upper right plots are the measured induced rectified voltage at the input. The lower left plot is the low frequency output voltage. The lower right plot displays the frequency spectrum of the signal detected at the output

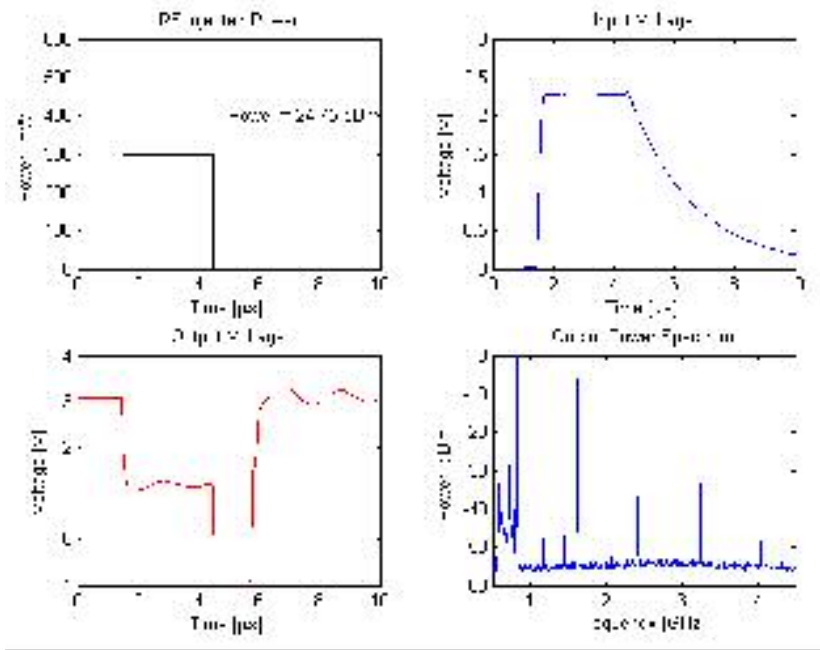


Figure 34. Results of pulsed RF (pulse width = 3 us, PRI = 100 us, peak power level = 24.75 dBm) injection into a 74ALVC04 inverter. The upper left plot displays the RF injected power level and pulse width. The upper right plots are the measured induced rectified voltage at the input. The lower left plot is the low frequency output voltage. The lower right plot displays the frequency spectrum of the signal detected at the output.

shown in this frequency spectrum with a large spike in a lower frequency range creating spectral products almost up to 4 GHz.

Finally, in Figure 34 when the time domain showed latent latching for a 1  $\mu$ s interval, the fundamental frequency and its harmonics measured up to the fifth harmonic dominated the frequency domain with additional components below 850 MHz and up to the second harmonic.

The relevance of these excited oscillations with respect to the effects of RF is twofold: one reason is modulation of the RF signal can have a profound effect in providing low frequency components to produce frequency products from the mixing behavior of the p-n junction, and second the RF is stimulating certain portions of the circuit to cause additional frequency signals unrelated to the RF frequency to oscillate. Since the impedances of the previous circuits showed voltage dependent resonances at various frequencies, the addition of RF and excited oscillations feeding through to the output of the circuit in combination with the propagating induced state change can cause additional problems in the following circuits. The propagating frequency components can potentially excite other resonances causing induced DC voltages and additional oscillations.

## CHAPTER 4 RF EFFECTS MODELING

### 4.1. Introduction

One objective of this thesis was to demonstrate the RF effects on digital electronics could be modeled to simulate the effects measured in experiments. PSPICE was used to determine if the effects could be explained using simple models of the inverters and lumped element circuits for parasitic elements. The diode parameters measured and the block diagrams of the ESD protection topologies found in the data sheets of the inverters were the basis for building the devices used in simulation models.

Although simulations have been performed on almost all the devices tested in this research, only one or two examples will be used in showing an understanding for each of the RF effects observed. Additional information and examples of simulations are included in appendices where noted.

### 4.2. Models derived from measurements

Diode models were designed using the parameters extracting using the methods outline in Section 3.2. A list of the values used for the diode models is given in Table 4 for the different diode models created. The PSPICE circuit models for the CMOS inverter circuits were based on the block diagrams of the ESD topologies given in the data sheets and application notes for specific logic families and on direct measurements to determine the accuracy of the block diagrams [21]-[24]. In certain cases, such as the ALVC CMOS inverter, the block diagram implied an ESD protection element from ground to signal and another element from signal to  $V_{dd}$ , in which case the PSPICE models were modified accordingly.

Since information regarding the MOSFETS in the inverters tested were not available, Level 4 MOSFET models based on 2.0 micron Orbit process at MOSIS were used in all the simulations [27].

Table 4. Diode parameters used for each of the ESD diodes for the various circuits simulated.

Parameter	Units	Diode Models			
		ESD_ACT	ESD_LVX	ESD_LVX_Vdd	ESD_HCT
IS	A	4.00E-15	5.00E-12	5.00E-12	1.00E-12
N		1.121	1.05	1.5	1.05
RS	$\Omega$	13	8	20	8
IKF	A	0	0	0	0
XTI		3	3	3	3
EG	eV	1.11	1.11	1.11	1.11
CJO	F	3.00E-12	3.80E-12	3.80E-12	3.60E-12
M		0.3	0.3	0.3	0.3
VJ	V	0.5	0.7	0.7	0.7
FC		0.5	0.5	0.5	0.5
ISR	A	4.00E-15	1.00E-10	1.00E-10	1.00E-10
NR		2	2	2	2
BV	V	3.5	20	10	20
IBV	A	0.0001	0.0001	0.001	0.0001
TT	s	1.00E-09	1.00E-09	1.00E-09	1.00E-09

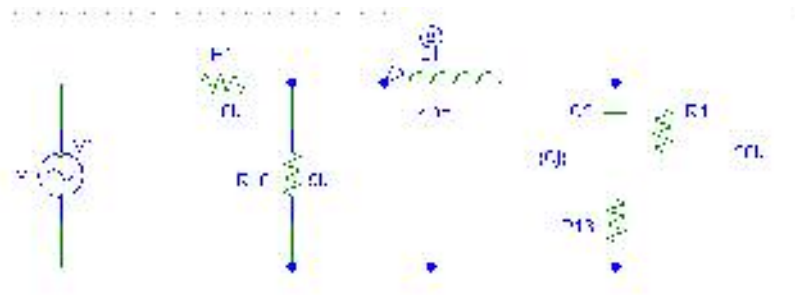
### 4.3. Simulated Port Characteristics

The port characteristics of interest are the input impedance and drive curves (RF to DC conversion curves). Starting with simple circuit explaining input impedance resonance, more complex models based on extracted diode parameters and taking into account parasitic elements were designed to simulate measured input impedance curves. A circuit was then designed and modified to match a measured RF amplitude to DC conversion drive curve.

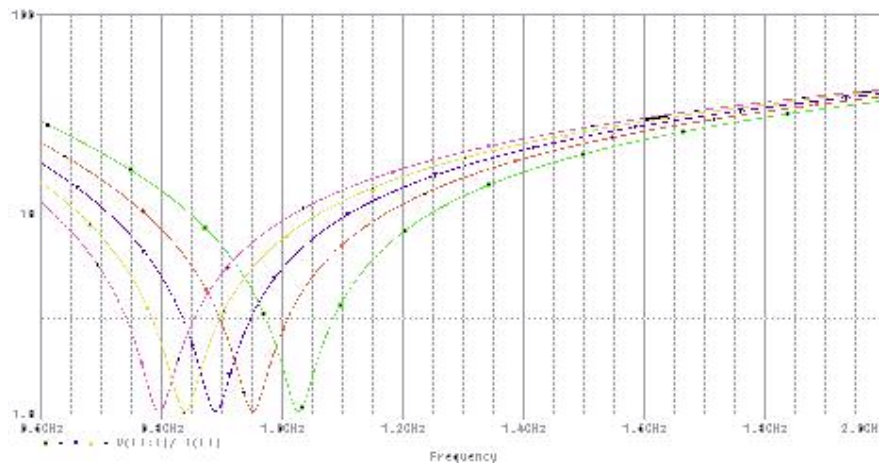
#### 4.3.1. Input Impedance and Resonance

The resonance dips observed in the input impedances measured in the CMOS inverters in Section 3.2 can be explained by the resonance formed by an inductor and capacitor in series. A simple series resonant tank circuit was designed in PSPICE to determine the effects of varying the capacitance to simulate the voltage dependent capacitance of a p-n junction. The circuit simulated is shown in Figure 35(a) using a high valued coupling resistor, bias resistor and load resistor. A value of 4 nH was assigned to the input inductor meant to simulate the inductance due to an package pin and bonding wire. The capacitor  $C_j$  was varied over the values 6-10 pF in 1 pF steps. An AC analysis

revealed as the capacitance decreased from 10 pF to 6 pF the resonances shifted from 800 MHz to just above 1 GHz (Figure 35b). A decrease in capacitance of 40% was shown for a voltage shift from 0 to 3 volts in the voltage dependent capacitance curves of Figure 6, which is reproduced for convenience in Figure 36(a). Measurements and datasheets from manufacturers have shown that inductances in the devices tested had values between 6-8 nH and zero bias capacitances due to the p-n junctions in ESD protection circuits to be between 3-4 pF. The resonant frequencies formed by these reactive elements are in the region of 500 MHz-1.5 GHz. Compared to the input impedance measurement in Figure 15, the location and shift in resonant frequencies are very similar.



(a)



(b)

Figure 35 A simulation showing resonances caused by using (a) a simple circuit with an inductor and capacitor in series creating and (b) the resulting impedance. The capacitor  $C_j$  was varied over the values 6 pF (green), 7 pF (red), 8 pF (purple), 9 pF (yellow), and 10 pF (magenta) to create a change in the resonance frequency of 200 MHz (compare with the measured results in Figure 15).

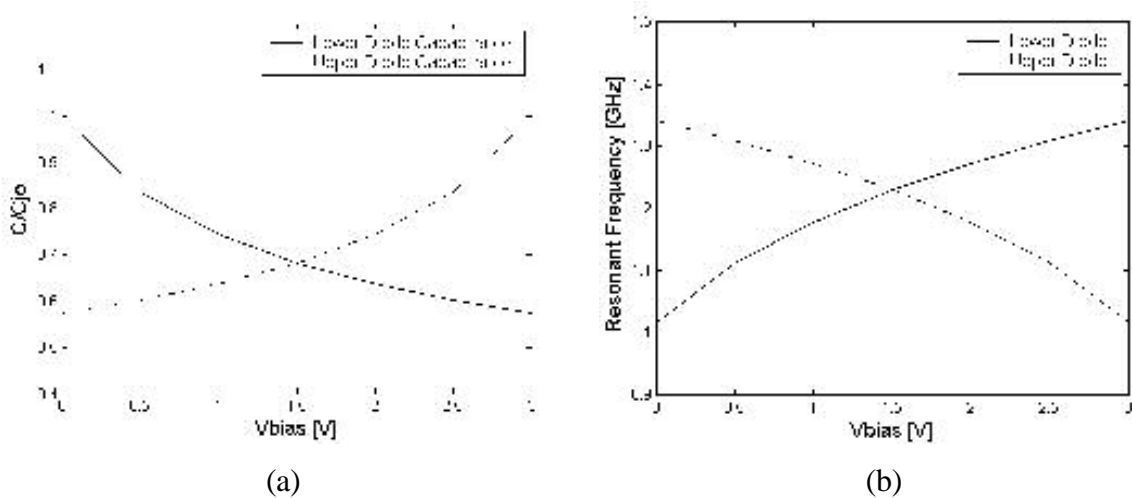


Figure 36. (a) A comparison plot of the voltage dependent capacitances showing variation as a function of bias voltages for an ESD diode from ground to the signal line (Lower Diode) and an ESD diode from the signal line to  $V_{dd}$  (Upper Diode). The diodes were assumed to be matched with  $\phi_{bi} = 0.7$  volts and  $n = 0.5$ . (b) A plot of the change in the resonant frequency of upper and lower diodes with  $C_{j0} = 3.5$  pF and  $L = 7$  nH.

Using a diode with a zero biased capacitance of 3.5 pF in series with an inductor of 7 nH in the equation for the resonant frequency:

$$f = \frac{1}{2\pi\sqrt{L*C(V)}} \quad (16)$$

the voltage dependent resonant frequencies are graphed in Figure 36b, where plots for the resonant frequencies due to upper and lower ESD diodes are compared.

A more advanced model was designed to take into account additional parasitic elements to model the frequency response observed in a 74ALVC04 CMOS inverter (Figure 37b). The elements of the injection point were changed into a 100 pF DC blocking capacitor and a 100  $\mu$ H RF choke. An additional inductor was added between the anode of the diode and ground to take into account the corresponding bonding wire in the actual circuit. To model the effect of the gate capacitances of the MOSFETs, a capacitance of 0.7 pF was added in parallel to the ESD diode. A parasitic capacitor and resistor were added in parallel to the inductors to account for additional package parasitics, which created the resonance at 1.8 GHz. The values for the circuit elements in the simulation were modified in attempts to match the resonances and their quality factors. Differences in the plots are attributed to unaccounted parasitic elements in the simulation model.

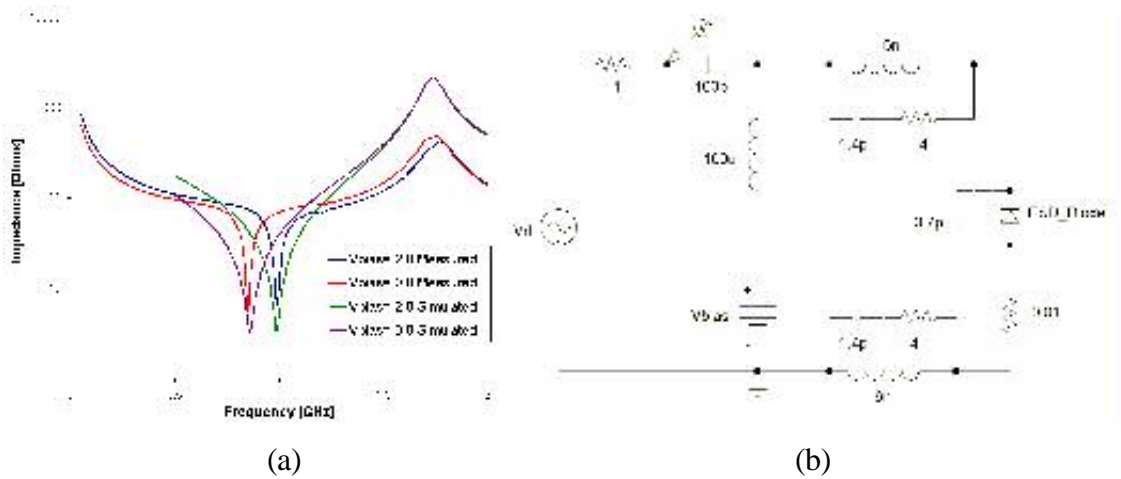


Figure 37. (a) A plot showing the comparison of the input impedance of a 74ALVC04 circuit measurements to the results of the simulation circuit in (b). The measured data for the input bias voltage of 0.0 and 2.0 volts are red and blue, respectively, and the calculate impedance form the simulation are purple and green for bias voltages of 0.0 and 2.0 volts, respectively.

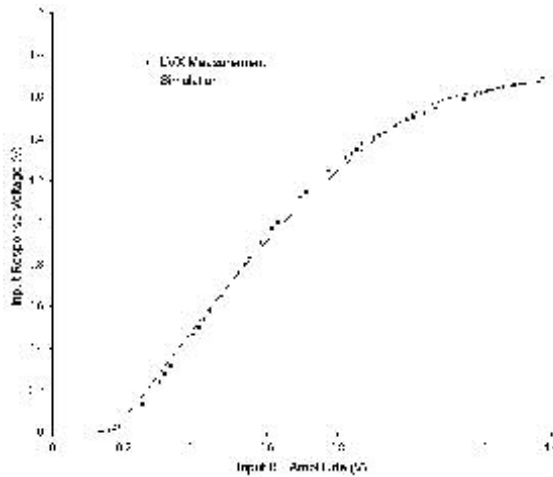
The frequency response of the input ports of the inverters provided insight into susceptibilities as well as excited frequencies from the inverters. As devices are becoming smaller in transistor size and in packaging sizes, the parasitic inductances and capacitances become more of a concern as their resonant frequencies are within the microwave frequency range. The parasitic inductances are due to the bonding wires, which lead from the pins of the packaging from the outside world to the bonding pads located on the substrate of the chip. Parasitic capacitances are related to the bonding pads, power line buses, and from the ESD protection devices located at the input and output ports of the device.

#### 4.3.2. Drive Curves

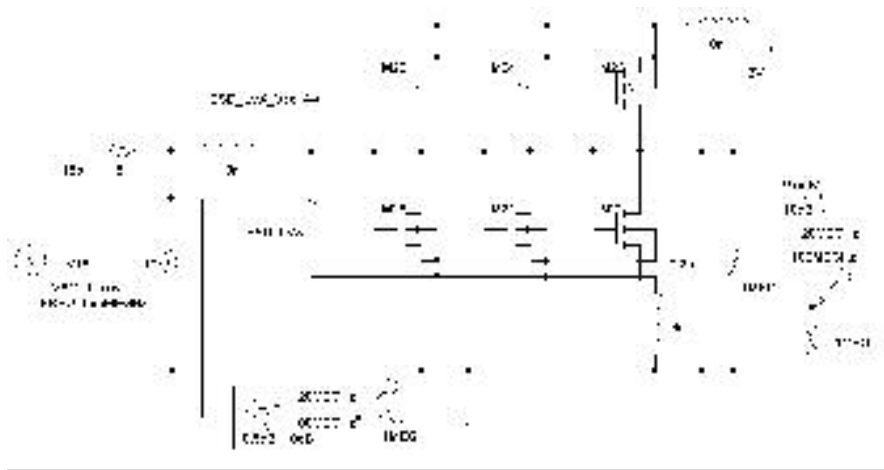
Drive curves were measured and simulated to determine the validity of the ESD diode models. A drive curve is normally associated with amplifiers to determine the transfer response of the input signal to the gain of the output signal with respect to a particular frequency. In this case the drive curve is defined as the transfer function due to rectification of the input RF amplitude in voltage to the induced DC voltage. The experiment performed was set up as in Figure 11 with the circuit in normal operating mode and a power supply voltage of 3 volts. A probe was placed at the input of the inverter to

measure the induced DC voltage across the pull-up resistor. The RF pulse width was set to 2.0  $\mu\text{s}$  with a PRI of 10.0 ms, and the frequency was always the resonant frequency on the device. The measured voltage was the average of the rectified RF envelope.

A PSPICE circuit model of the LVX was made based on the block diagram found in the LVX datasheet where lower and upper ESD protection diodes were shown to exist Figure 38. A drive curve simulation was performed by using a CW RF signal at the resonant frequency of the circuit, delaying the simulation to a time where the rectified voltage had stabilized, sweeping the RF amplitude, and measuring the induced DC voltage. The induced voltage was measured through a low pass filter with an upper cutoff frequency of 100 MHz.



(a)



(b)

Figure 38. (a) RF to DC drive curve and (b) PSPICE circuit used to match simulation results with measurements for the LVX inverter.



#### 4.4. Simulated RF Injection Effects

Basic circuits were designed to simulate the full state change, the partial state change, latent latching, and relaxation oscillations. The pulsed RF signal was generated using a VPULSE source multiplied with a VSIN source. The amplitude of the VPULSE component controlled the amplitude of the RF signal. DC blocking capacitors and RF chokes were used as the injection and bias network.

##### 4.4.1. Full State Change

A simple inverter circuit using a single input inductance and a lower ESD diode from ground to signal showed a full logic state change (Figure 39). An AC analysis determined the resonant frequency of this particular circuit to be 1.1GHz. Figure 40 shows the induced filtered input voltage and the output voltages in comparison with the RF pulses for RF amplitudes of 0.5, 1.0 and 1.5 volts. The induced input voltages show peaking with an enhancement in the RF to DC conversion factor of more than two times the RF amplitude. The input voltage then decays as the resonant frequency of the circuit increases with the induced voltage changing the RF gain characteristics of the circuit. The output voltage clearly shows a full state change and decreasing leading edge delay times with increasing RF amplitude.

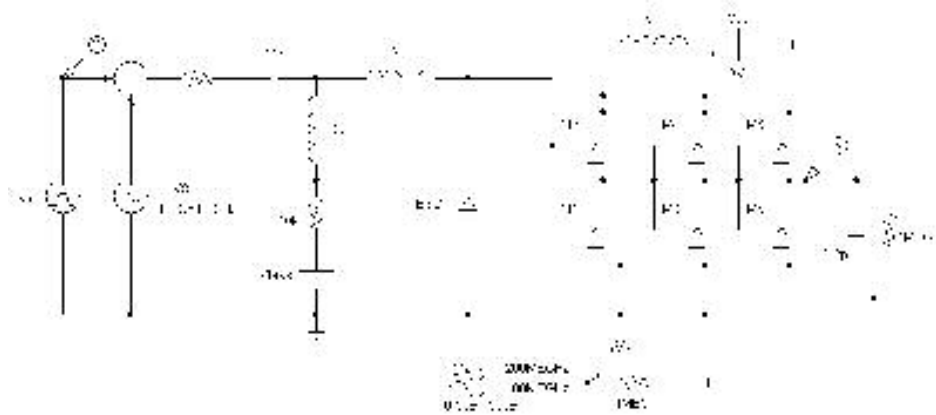


Figure 39. The circuit diagram of the CMOS inverter circuit with a single ESD diode used to simulate rectification effects in the time domain .

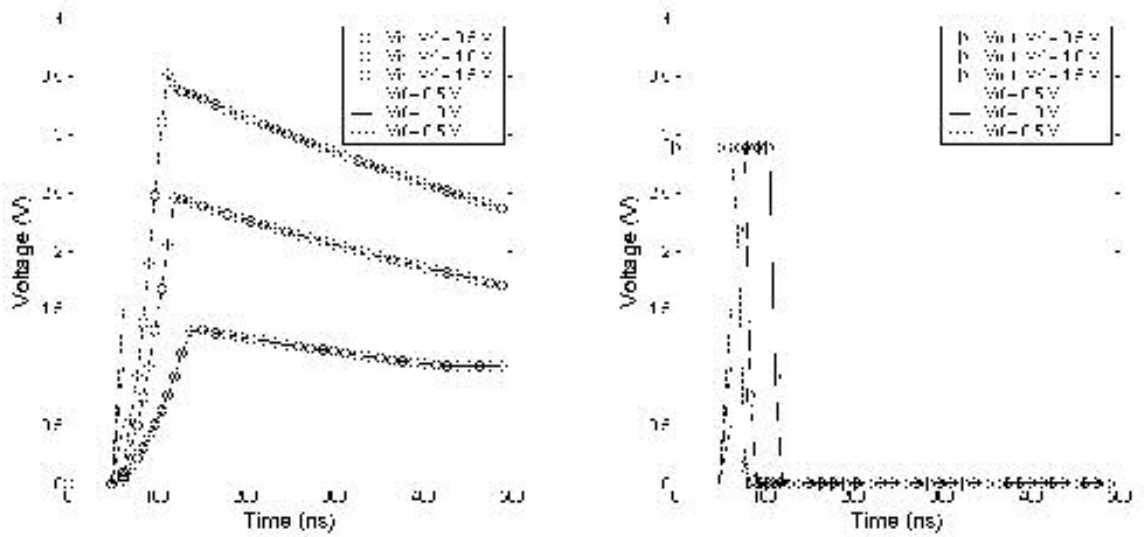


Figure 40. Plots showing the effects of rectification showing the voltage at the (a) input and (b) output for RF voltages of 0.5, 1.0 and 1.5 V.

#### 4.4.2. Partial State Change and Latent Latching

Two simulations were performed to determine the differences between the induced voltage due to a pulsed RF signal and the effects of a DC voltage with the same shape characteristics of the RF average. A simulation circuit was designed based on the ALVC circuit adding in 500 MHz low-pass filters at the input, the output of the first stage, the output of the second stage, and at the load resistor (Figure 43). The first simulation used an RF pulse with a pulse width of 150 ns as the input signal while recording at each of the previously mentioned points the voltages in the circuit and the filtered voltages. In Figure 41 and Figure 42, the plots in blue are the voltages measured within the circuit, and the red plots are the filtered voltages. The second simulation used the filtered voltage at the input (the red signal in the upper picture and the blue signal of the lower picture of Figure 41 are identical) as stimulus. The voltages measured at the input and the output of the first stage are in Figure 41, where the upper pictures are the voltages measured with the RF as the input source and the lower plots are the simulations with the filtered RF signal as the source. Figure 42 has the plots of the voltages measured at the output of the second stage and at the load.

A comparison of the filtered voltages at the output of the first stage in Figure 41b shows distinctly the bias shift due to the RF signal, in the same region the voltage in the DC pulse case has switched entirely to the other state. The RF induced voltage does

indicated a bias shift almost to 0 volts after the RF pulse has terminated, which correlates to the decaying low frequency voltage signal at the input of the first stage.

The voltages at the output of the second stage and across the load in Figure 42 show the distinct difference between the effects of the RF pulse and the filtered average voltage where a only a bias shift is observed during the RF pulse width and latching after the RF has terminated, where the low-frequency pulse has switched the inverter entirely into the low state as long as the input voltage was above the switching point of the first stage. This RF effect is dependent on the inductors from the lower diodes and source terminals of the NMOS devices to ground and the inductor between the upper diodes and source terminals of the PMOS devices to  $V_{dd}$ . The ESD protection topology seems to also have an effect on the sensitivity of the bias shift and latent latching. These elements together form a feedback path from the sources of the MOSFETs back to the diodes at the input of the circuit. The interaction of these circuits with RF entices further investigation.

This simulation provides strong evidence as to why CW RF requires a larger amount of power than pulsed RF to cause errors in certain digital electronics. If a CW RF signal was injected into a device, the output voltage would only show a bias shift as in the previous discussion. A larger amplitude CW signal would be required to shift the low frequency voltage at the output of the first stage to the point of the switching voltage to cause the device to switch. From these figures we can surmise that the termination of the RF pulse, which has induced a DC voltage above the switching voltage of the logic circuit, will switch the device causing an erroneous signal to propagate through the logic.

Sweeping the RF amplitude from 2.0 volts to 3.75 volts, the bias shifts due to the RF and the periods of latent latching are more distinct in Figure 44. Latent latching begins when the RF amplitude is at 2.75 volts. If the switching voltage for the inverter was at 1 volt, the RF amplitude to induce an output voltage bias shift to cause a state change would have to be 3.75 volts. Assuming a 50 ohm transmission line, the RF power increase required to cause an effect would be approximately 3 dB.

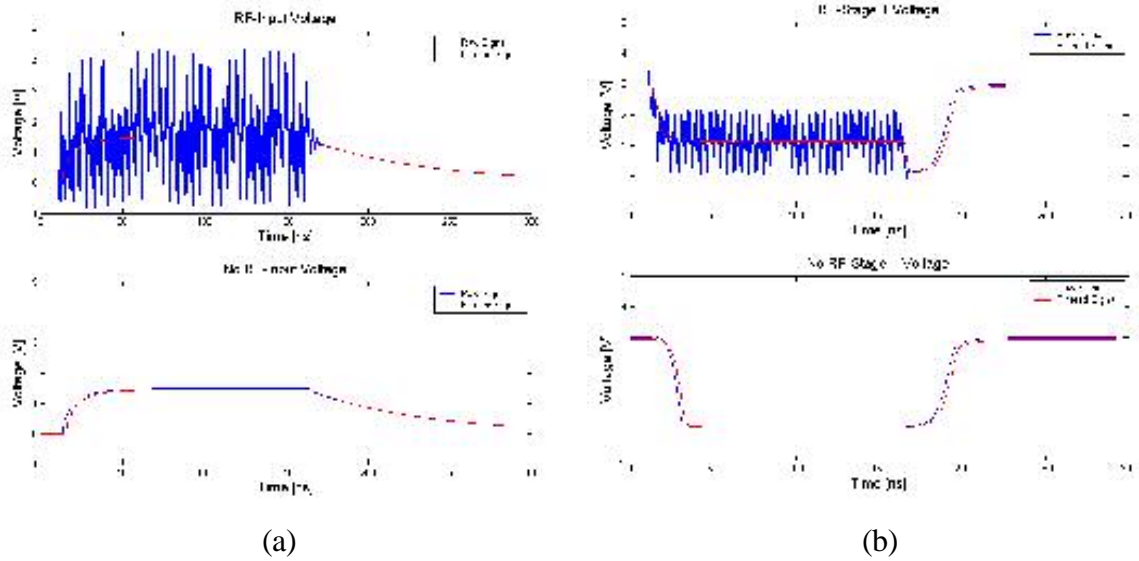


Figure 41. Comparison of the effects an injected RF signal at (a) the input of a model and (b) the output of the first stage of an ALVC circuit. The top picture is of the RF signal (blue) and the mean of the RF pulse (red) as seen through a low-pass filter. The lower picture uses the mean of the RF signal as stimulus (blue) and also shows the mean as seen through a low-pass filter (red).

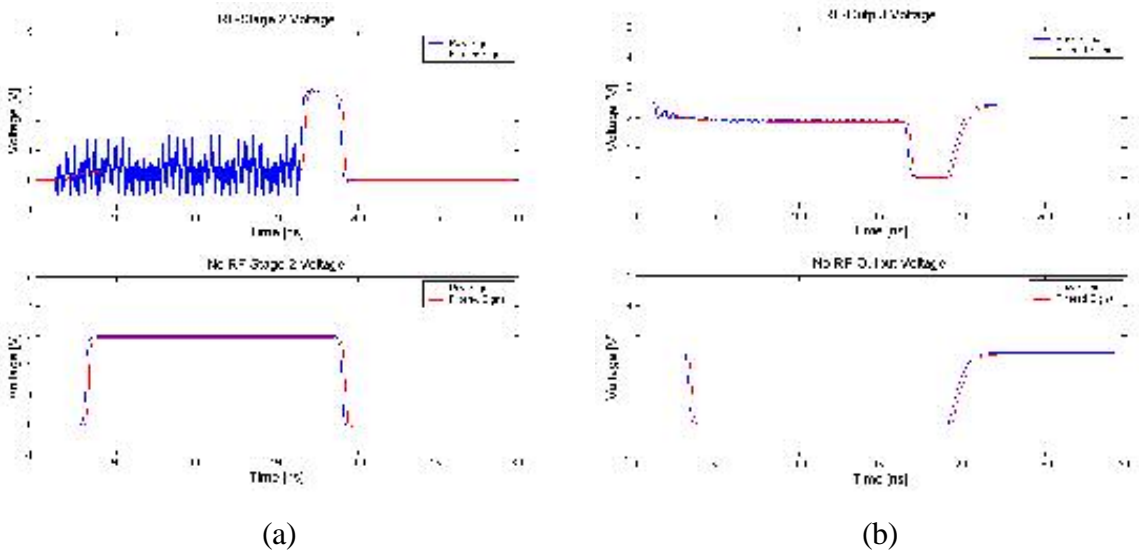


Figure 42. Comparison of the effects an injected RF signal at (a) the output of the second stage and (b) the output of the inverter of an ALVC circuit. The top picture is of the RF signal (blue) and the mean of the RF pulse (red) as seen through a low-pass filter. The lower picture uses the mean of the RF signal as stimulus (blue) and also shows the mean as seen through a low-pass filter (red).

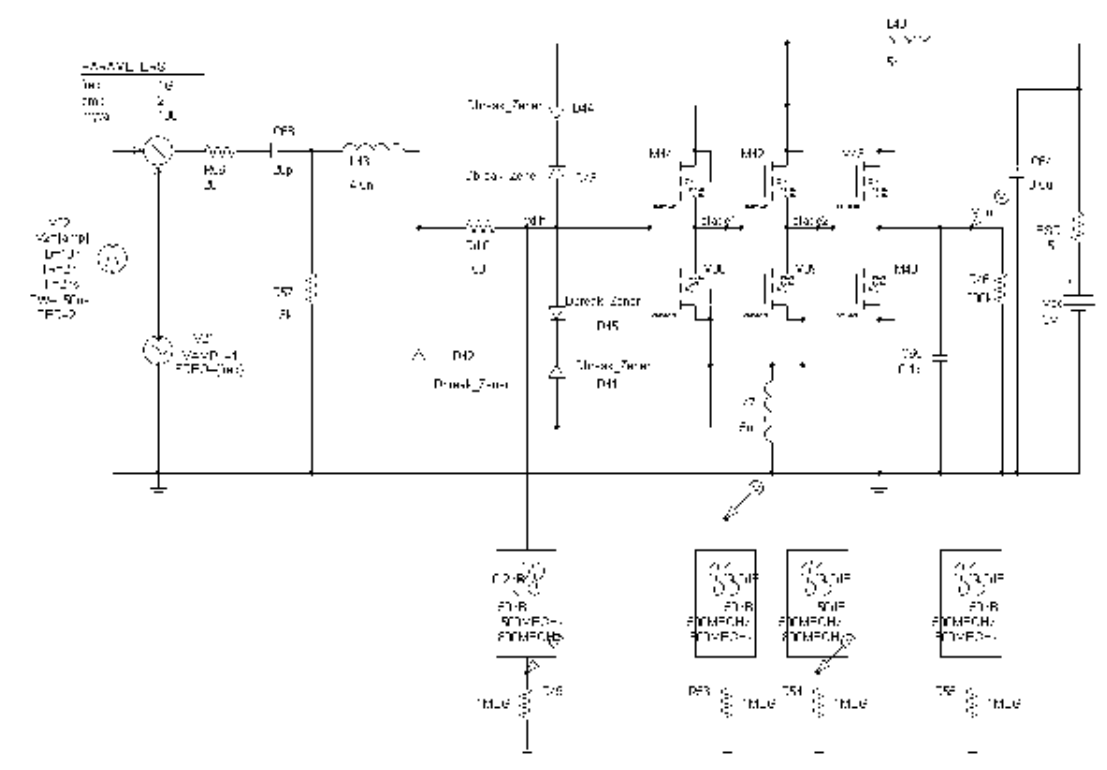


Figure 43. Circuit diagram for the waveforms with RF stimulus in Figure 41 and Figure 42 The circuit diagram for the DC waveforms is similar but replaced the RF source with a file input source.

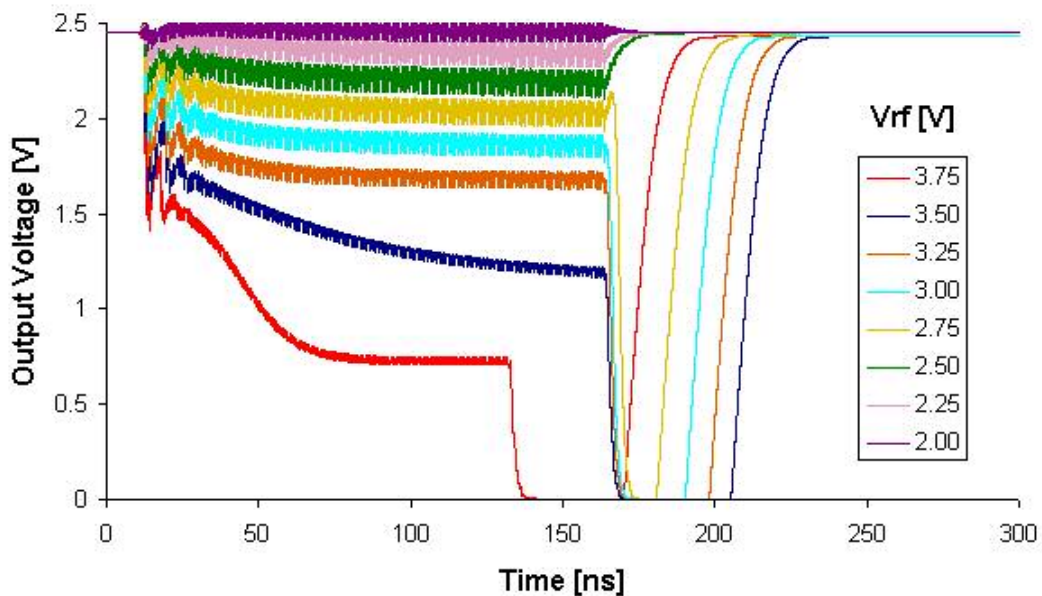


Figure 44. Output voltages of the SPICE circuit model in Figure 43, which show for most RF voltages the device going into hard conduction after the RF pulse. The RF pulse is varied in amplitude from 2.0 to 3.75 volts in 0.25 volt increments. The RF had a center frequency of 1.0 GHz, and a pulse width of 150 ns and was delayed by 10 ns.

#### 4.4.3. RF Gain

A CMOS inverter with an input bias voltage close to the switching will conduct like a Class-A amplifier. While one of the MOS transistors is conducting, the output of the other transistor will act as an active load. Over a range of voltages around the switching voltage, the inverter acts as a linear amplifier with high gain [28]. The general equation for the gain of MOSFET amplifier is given as

$$A_v = -g_m * (r_o \parallel R_d) \quad (17)$$

where  $g_m$  is the transconductance of the MOSFET,  $r_o$  is the output resistance of the MOSFET, and  $R_d$  is the load impedance as seen at the drain. In this case, the drain resistance is the active load of the other MOSFET and the input impedance of the next inverter stage. Since the inverters are buffered, we expect the DC gain of the second and third inverters to be very high, essentially limiting the bias voltages to these stages to ground and  $V_{dd}$ . The MOSFETs would be expected to be operating in their triode regions limiting the Class-A conduction effect of the devices.

To determine the RF gain in between the CMOS stages excluding the effect of the RF enhancement from input impedance resonances, a small signal AC analysis was performed on the circuit in Figure 43 measuring the RF voltage gain between the input and output of each inverter stage, and between the input and output of all three stages. Figure 45 shows the RF gains when the circuit is biased in the low (0.5 volts) and high (2.5 volts) logic states and the AC signal was 10 mV.

An amazing gain of almost 20 dB is calculated for Stage 2 at 700 MHz in the low bias case. However, with the accumulation of effect from all three stages, the peak of -15 dB near 900 MHz is calculated in the low bias case.

The small signal transfer functions for all the three circuits showed drastic changes as the input voltage was swept from 0 to 3 volts, with a huge jump when the input voltage reached the switching voltage. In the high bias case, the transfer functions of all three stages have changed dramatically from the low bias case. The AC transfer curve of the entire circuits showed a gain of almost 0 dB at 1GHz. This simulation shows the potential of no RF loss between the CMOS inverters at certain frequencies.

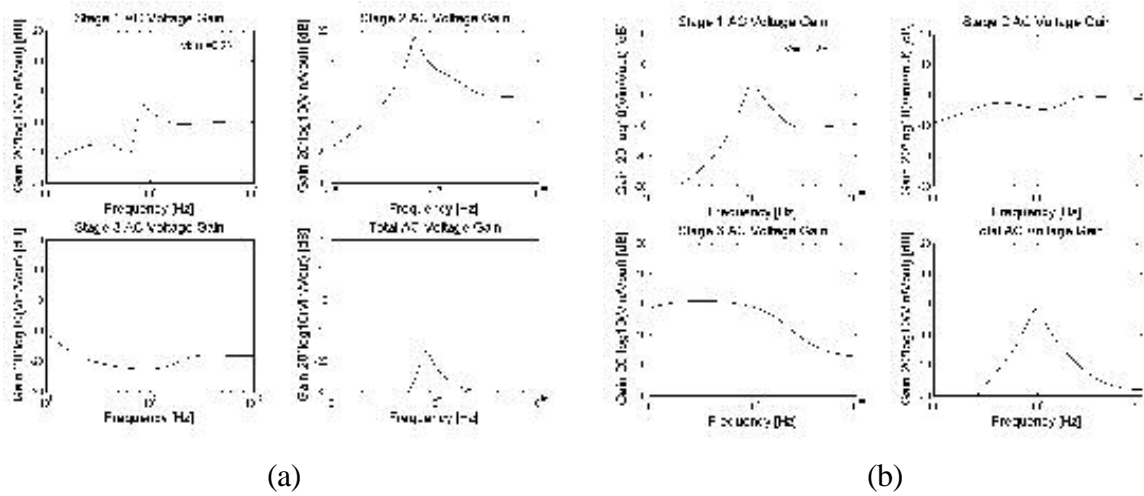


Figure 45 The AC gain between the first stage, second stage, third stage, and the entire CMOS inverter for (a) low logic state ( $v_{bias} = 0.5$  volts) and (b) high logic state ( $v_{bias} = 2.5$  volts).

#### 4.4.4. Relaxation Oscillations

In Section 3.3.4, the ALVC CMOS inverter showed low frequency oscillations referenced as relaxation oscillations. The frequency of the RF signal in that experiment was slightly above the zero-bias resonant frequency of the input impedance. Figure 46 is a basic circuit diagram of the LVC circuit containing a single ESD diode from ground to the signal line and inductors at the input, to the power supply voltage and to ground. The PSPICE input impedance resonance was calculated to be 688 MHz. An RF injection frequency of 850 MHz was arbitrarily chosen for this simulation. For an RF amplitude of 1.5 volts, the filtered input and output voltages of Figure 47 shows the distinct sawtooth waveform of the relaxation oscillations. With increasing RF amplitude in this simulation, the magnitude of the relaxation oscillations increased and the frequency of the sawtooth waveform varied. Several simulations have shown the inductor from anode of the ESD diode and source of the NMOS circuits to ground seems to be a critical component in causing this effect.

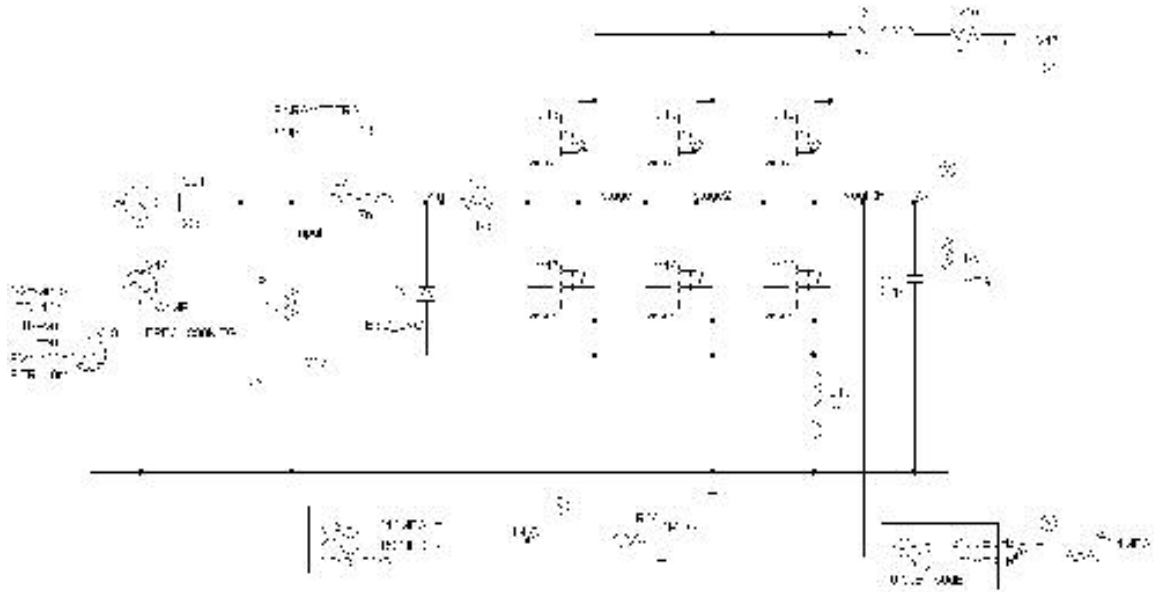


Figure 46. PSPICE circuit of LVC CMOS inverter, which simulated relaxation oscillations as seen in Figure 47

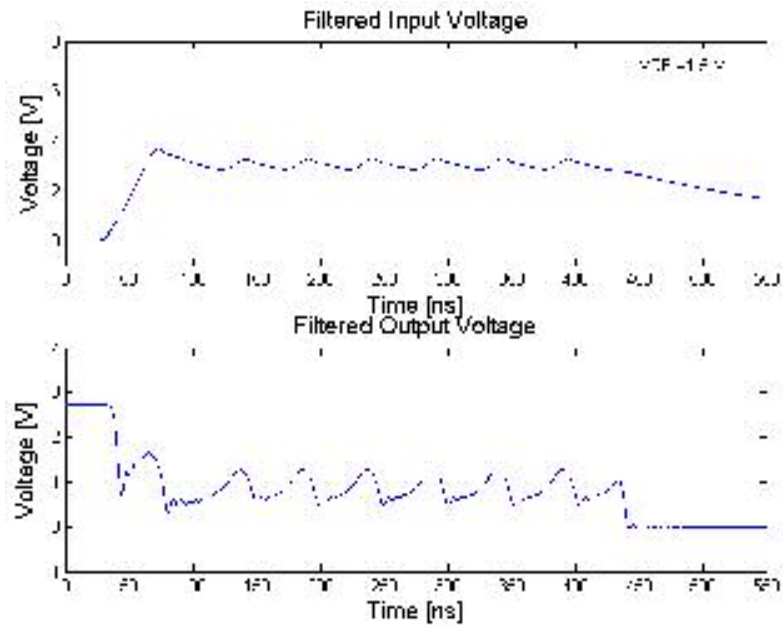


Figure 47 PSPICE simulation output of a LVC type of circuit showing the induced RF at the input with relaxation oscillations and a bias shift at the output including relaxation oscillations and latent latching.



## **CHAPTER 5 CONCLUSION AND FUTURE WORK**

### **5.1. Conclusion**

This thesis focused on the effects of RF pulses on digital electronics. The following is a summary on each of the major points in the chapters.

Theory of the common circuit elements found in CMOS inverter was described in Chapter 2. The input circuit of CMOS inverters includes the ESD protection circuits, which consist of at least one diode or p-n junction. A series expansion of the ideal diode model showed that second order term produces an induced DC voltage. The amplitude of the induced voltage is dependent on the saturation current of the diode, the video resistance in the diode, the RF amplitude, and the load impedance as seen by the diode. Bandwidth considerations for signal detection and measurements were discussed from a frequency point of view and how it should be applied to measurements.

The equations describing the operation of CMOS inverters indicate the switching voltages of the devices are dependent on the power supply voltage and characteristics of the MOSFETS. Logic circuits are also known to have problems with logic pulse characteristics with edges, which are very slow or very fast. The frequency components of the logic pulse can cause oscillations to occur leading to operation instability. Circuitry added to CMOS devices such as Schmitt Trigger device and Bus-Hold Circuitry use additional Inverter stages to feed back DC voltages, potentially leading to feedback loops for RF signal.

Chapter 3 provided details of the results of experimental measurements performed in this research. The circuit setups were described used for a majority of the injection experiments. Bandwidth considerations were taken into account when attempting to measure the induced voltages and finding a method of efficiently coupling RF into the circuits. Loading problems were also discussed playing a large factor in choosing DC blocking capacitors and RF chokes. The injection experiments required blocking capacitors which acted as 50 ohm transmission lines at injection frequency required while acting as a high impedance line at lower frequencies. The RF choke had to be such that the DC pulse with large frequency components (up to 100 MHz) can be measured while blocking frequencies above 200 MHz. A suggested method for enhancing the was by using high pass filters in place of DC blocking capacitors and low pass filters for RF chokes.

The DC and high frequency input port characteristics were measured for several families of CMOS inverters including the AHC, AHCT, HC, HCT, LVC, ALVC, LVC, and LVX. The IV relations for several CMOS inverters were used to determine the existence of a diode type device located at the input of the circuits of interest. The DC diode characteristics were extracted using a sensitive multimeter and used to determine the saturation current and ideality coefficient. Voltage dependent input impedance resonances were found in all of these devices, which varied up to 200 MHz with a change in voltage corresponding to a low logic state to a high logic state. A method to measure and calculate the high frequency capacitance of the variable p-n junction capacitance was discussed and used to incorporate the values into SPICE models.

The results from threshold power injection experiments on several families of logic circuits showed that low powered RF pulses (down to 0 dBm) could cause state changes. The CMOS logic families tested included AC, ACT, AHC, AHCT, HC, HCT, ALVC, LVC, LCX, LVX, and VHC. A  $1/f^2$  relation in the 1-6 GHz range was observed in the required power for most of these circuits. Operating power supply voltages showed a direct correlation to the switching voltage and required threshold hold power levels. Changes in power supply voltages showed a change of 15 dB to cause effects. Input bias levels were also played a role in the threshold power levels for CMOS inverters affecting the susceptibility of a circuit. A change in input logic state change showed a difference up to 20 dB in RF power to cause effects between low and high logic levels. In some cases state changes were never observed.

Changes in the power supply current corresponding to the state changes output voltage bias shifts in CMOS inverters were measured. These shifts indicated regions of input bias levels where the MOSFETs of the inverters enter into Class A conduction operation leading to larger RF gains. The increased RF gains of the MOSFETS also correspond to large variations in the Miller capacitances of the devices potentially affecting the rectification sensitivity of the ESD diodes and the observed input impedance resonance frequency.

RF feedthrough and gain were measured at the outputs of the HCT and LCX devices. The amplitude of the RF measured in the output waveforms depended on RF

amplitude and input bias voltage. RF gains up to 2 dB were measured in the HCT device and 3 dB in the LCX inverter.

Different circuits showed different responses to pulsed RF signals. Depending on the circuit and the input bias devices showed logical state changes during the RF pulse, output voltage bias shifts during the pulse, logical state changes after the termination of the RF pulse, or no response at all. With circuits showing state changes and after the RF pulse, output voltages were shown to potentially switch the inverters longer than the pulse width of the injected RF signal. This latent latching was also observed in devices that only showed output voltage bias shifts during the RF pulse. Latent latching corresponded to the induced voltage level and RC time constant at the input of the device, keeping the device switched until the input voltage dropped below the switching point of the device.

Frequency domain measurements during injection experiments indicated excited circuit resonances occurred. The fundamental frequency, several of its harmonics, low-frequency signals and the IM products of all these signals were recorded at different power levels during the experiment. Induced oscillations were also observed in the time domain, which were seen as sawtooth waveforms at input and output of the devices measured.

Chapter 4 discussed the results of simple simulation circuits designed in PSPICE modeling the effects observed for the CMOS inverters. Block diagrams of the ESD protection circuit topology in data sheets of the various devices were used as the basis for input circuits of the simulation models. Diode models were created based on extracted DC and high frequency characteristics. The resonances measured in the input impedances of CMOS inverters were reproduced using models of inductors in series with variable capacitors. The inductances were attributed to the bonding wires measured in the 4-8 nH range. The p-n junctions of the ESD protection circuits were the sources of voltage dependent capacitances, which caused the resonant frequencies to shift up by 200 MHz as the input bias shift from a low logic level to a high logic level. A simulation model of the input impedance of the ALVC CMOS inverter taking into account various parasitic elements gave very good agreement to measured data for resonance shifts from a low bias input to a high bias input.

To determine the accuracy of the RF signal to DC conversion, rectification drive curves were simulated. The parasitic elements of the circuits for the LVX and ACT CMOS

inverters were modified until good agreement was made between the simulation and measured data.

State changes due to induced rectification at the input were observed in simulation circuits where the bonding wire inductance for the ground and Vdd pin did affect RF rectification. Circuits without an inductor at this junction showed RF gain due to resonance, RF signal rectification and a state change in the logic circuit corresponding to the injected RF pulse. However, when the ground and Vdd inductance was a factor and used as components in simulation circuits, output voltage bias shifts, latent latching and relaxation oscillations were all found to be modeled creating output voltage waveforms predicting behaviors observed in the measured RF injection experiments. The bias shifts in the output voltage during RF pulsed signals that also show latent latching after the RF pulse terminated gave evidence as to why threshold power levels for RF pulse modulated signals to cause effects in circuits can be from 3-10 dB less than the threshold power levels for CW RF signals.

The AC gain was also calculated using a CMOS circuit which demonstrated the input bias has an effect on the RF transfer curves of each stage of the inverter as well as the entire circuit. Depending on the input logic state and the frequency, the RF was shown to potentially pass through a circuit with little or no attenuation.

Theoretical analysis, measurements and simulations have shown that the most sensitive rectification elements in logic circuits are the ESD protection elements. With RF amplitude enhancement from input impedance resonances, induced voltages from ESD diodes, RF feed through, exciting parasitic circuit resonances, low-powered pulsed RF signals have been shown to be able to affect the correct operation of digital electronics.

## 5.2. Considerations for Future Work

This section contains some ideas for follow-up areas of research based on the findings in this paper. Because of the breadth of this subject with so many different avenues of research that can be explored, the following are just some major that could be considered.

A Cascade RF probe station has been setup for the characterization of ESD protection ggNMOS and two-stage inverter designed through MOSIS (Figure 48). The on-chip probing will eliminate the effects of the package parasitic elements. RF injection will also be performed to determine the rectification efficiency of the ESD ggNMOS. Additional commonly used ESD topologies could be designed through MOSIS and modeled to evaluate the susceptibility of these devices. A comparison between inverters with and without ESD protection circuits could also be done to determine the rectification sensitivity between the different circuits.

As a follow-up to the experiments performed by Kenneally in [86], the packages of COTS CMOS inverters could be removed to expose the internal circuitry. By using the Focused Ion Beam (FIB) at the University of Maryland, injection and port characteristic testing could be performed at different stages while severing different portions of the ESD protection devices from the main inverter circuit.

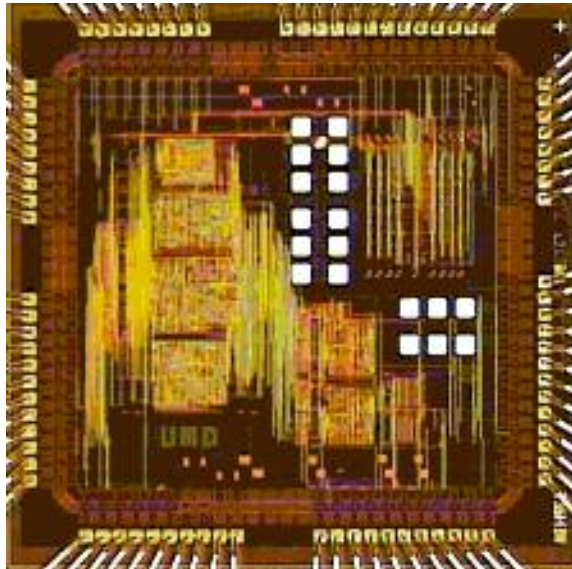


Figure 48. MOSIS chip designed to test S-parameters of ESD structures and to use in RF injection experiments.

Since the lumped element circuits showed very similar characteristics as the measurements, building models and performing simulations in HSPICE or other high frequency circuit simulation package would be the next step in modeling these effects. A more complete analysis can be performed in calculating high frequency effects such as power reflections and potential points of radiation.

RF injection experiments using chaotic or wideband modulated waveform should also be considered. Initial testing showed very promising results in causing state changes and exciting a wide range of resonances. These types of signals could excite a wide variety of input resonances affecting more than one type of circuit. With the aspects of RF gain and feedthrough, a signal covering a very large frequency range will have more of a chance in causing an effect.

Based on all the findings here, one very large area of research could be to determine the probabilities to cause errors in large systems of circuits. Using the basis of different pulse characteristics of interfering signals, the timing issues of latent latching, logic states of the devices under test, and the potential of inducing oscillations the rate of failure or errors could be calculated to determine susceptibility and rate of errors regarding all types of electromagnetic interference.

## Appendix A. RF Injection Testing on Computer DRAM

Initial RF injection testing was performed into an Intel Neptune-ISA chipset 90 MHz CPU computer with 33 MHz Dynamic Random Access Memory (DRAM) as a memory checking program was running simultaneously. The DRAM memory stick consisted of six 20-pin Panasonic 424100 4 Mbyte DRAM memory modules with the pin layouts as shown in Figure A1.



Figure A1. The pin layout of the 424100 4Mbyte DRAM memory module used in RF injection testing [1].

The source of RF was a HP 83731B signal generator connected to a HP 83020A RF amplifier. The RF signals were coupled into the DRAM chip by using a DC blocking capacitor in series with a stripped piece of coaxial cable soldered to the pins of the memory module. A Tektronix P6243 FET Probe attached to a Tektronix TDS 620B Oscilloscope was used to measure the logic and RF induced voltages on the RAS pin of the Panasonic 424100 DRAM memory module. A block diagram of the setup for the RF injection experiments is shown in Figure A2.

The computer consisted of a motherboard, a floppy drive, a VGA video card and the single DRAM memory stick. A program, MEMTEST86, designed to detect errors in the operations of computer memory, was used to determine the effects of RF injection into

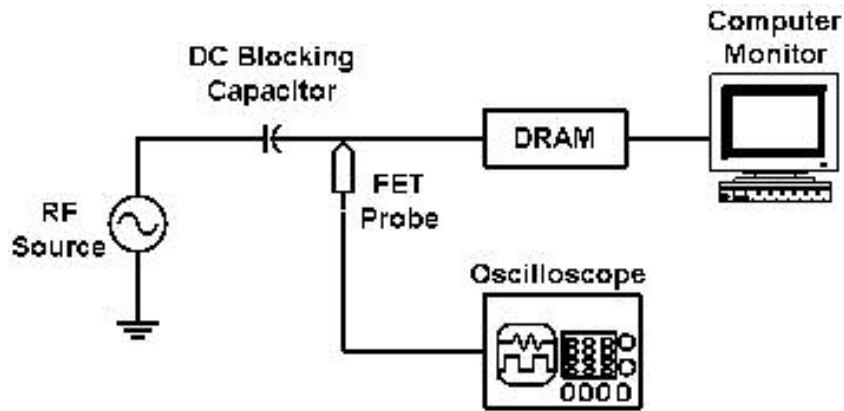


Figure A2. The block diagram of the layout for the RF injection experiment into a Panasonic 424100 DRAM memory module.

the DRAM module [28]. The program works by temporarily writing a series of "0's" and "1's" to different locations in the memory module, and then reads back the data words to determine if any of the memory blocks had been corrupted. Any errors encountered were reported to the monitor displaying the test, which was currently running, and the location in the memory where the error occurred.

The memory module has several different pins associated with the functionality of the device, particularly the write enable pin ( $\overline{WE}$ ), the input data pin (D), the output data pin (Q), the row-address strobe ( $\overline{RAS}$ ), the column-address strobe ( $\overline{CAS}$ ), the address pins (A0-A10), the ground pin (GND), and the power supply pin (VCC). All of these pins were tested for susceptibility to RF, which demonstrated the RAS pin was more susceptible than the other pins by almost 15 dBm. The power supply pin and clock pins were the most robust of all the pins tested and showed no effect of RF power levels up to 25 dBm. Injections into the RAS pin were used for the experiments described below.

Continuous wave (CW) RF signals were injected into DRAM memory module over a range of frequencies and increasing the power level until an error was detected. Power



threshold tests were performed using the on-screen error reporting of MEMTEST 86 as an indicator to bit upset. The RF power levels were increased incrementally until a series of errors appeared on the monitor, the monitor began displayed unusual characters hiding the diagnostics reported by MEMTEST 86, or the system would not respond to external stimulus and required a reboot of the computer to function normally.

Voltage measurements taken at the RAS pin during RF injection demonstrated voltage bias shifts of the digital logic voltages levels. An experiment with CW RF with a frequency of duty factor of 50% and pulse width of 150 ns injected into the RAS pin demonstrated a +1 volt bias shift from the low state and a -1 volt bias shift from the high state as seen during a data pulse (Figure A3). The measurement also showed a sinusoidal signal coupled onto the induced voltage, which had a frequency corresponding to the 33 MHz clock frequency of the memory module.

For a comparison to the effect of pulse modulating, the RF signal was modulated with a duty factor of 50%, a pulse width of 150 ns, keeping the frequency at 1.965 GHz,

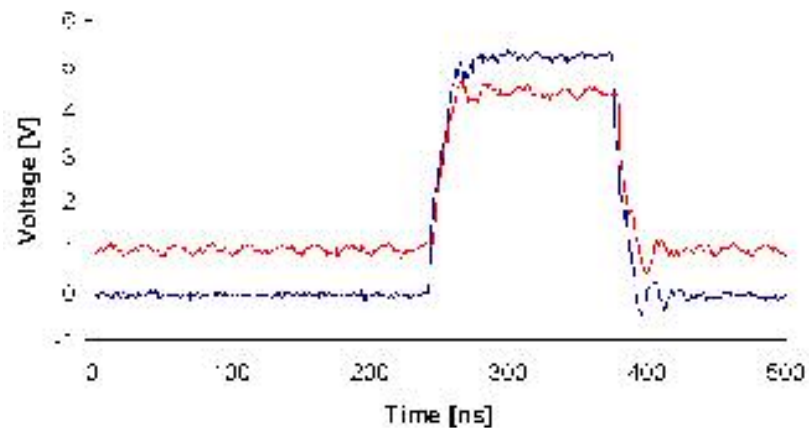


Figure A3. The input voltage measured at the RAS pin (blue) before and (red) after an injected CW signal with a frequency of 1.965 GHz and a power level of 26.0 dBm showing an induced bias shift due to the RF signal. The induced voltage shifted the logic levels by one volt in the low and high logic states and also had the 33 MHz clock signal of the memory module couple onto the voltage line.

but raising the power level to 29.4 dBm. The measurement of the voltage on the RAS pin clearly shows the induced voltage shifts tended to be more susceptible to coupling noise into the system, as seen in the CW injection experiment (Figure A4).

For a final comparison between CW and pulsed modulated RF signals, power threshold curves were measured over the frequency range of 1.0-2.2 GHz. As shown in Figure A5, the average values for the power required to cause an upset between CW (green) and the 50% duty factor, 150 ns pulse-width pulse modulated RF signal (cyan) shows the power required for the pulse modulated signal was 7-10 dBm lower than the CW case. The amplifier reached its power limitations for the CW injection experiment for 2.0-2.2 GHz and no data was recorded.

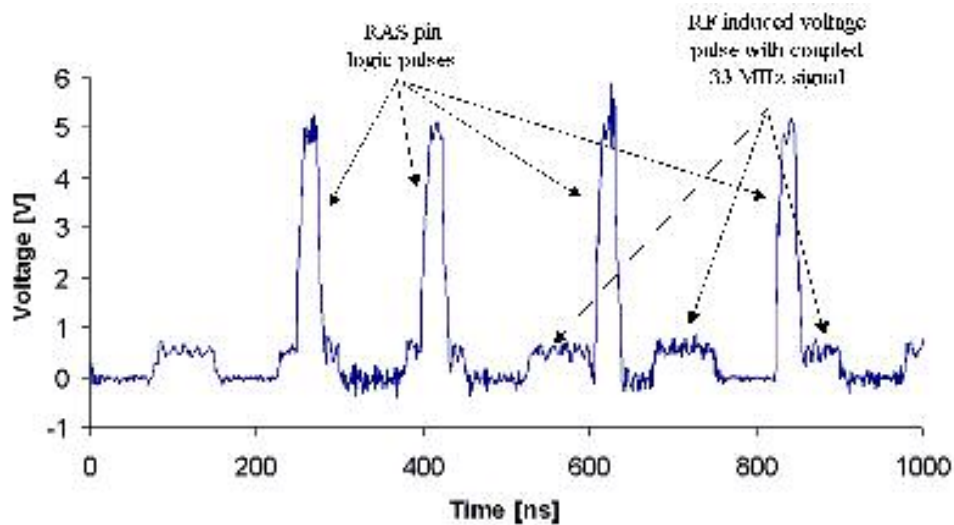


Figure A4. The voltage seen on the RAS pin of a Panasonic 424100 DRAM memory module when a pulsed RF signal at 1.965 GHz with a power level of 29.4 dBm, a duty factor of 50% and pulse width of 150 ns was injected into the pin. The measurement distinctly shows the logic pulses compared to the RF induced voltages, which are coupled with the 33 MHz memory clock signal.

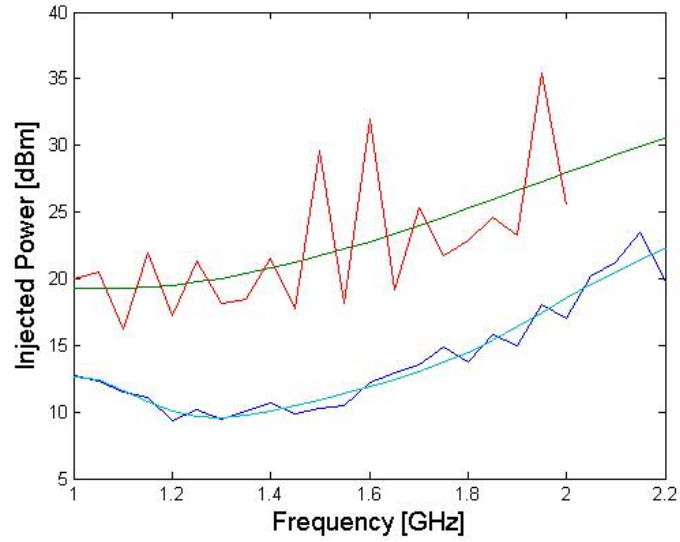


Figure A5. A plot comparing the threshold power levels of (red) CW and (dark blue) pulsed RF signals, which caused errors in a Panasonic 424100 DRAM memory module. The pulse modulation had a 50% duty factor with a pulse width of 150 ns. Third order polynomial fits are also shown for CW (green) and pulsed RF (cyan) signals to approximate the averages of the threshold power levels. The amplifier reached the power limitations for the CW case for 2GHz and above, thus no data was recorded.

## Appendix B. I-V Characteristics of Inputs and Outputs for Various Digital Families

The I-V characteristics of the 74HC04, 74HCT04, 74AHC04, and 74AHCT04 were measured on a HP4145B Semiconductor Parameter Analyzer. Four measurements were taken with the first port acting as the voltage reference: ground to input, input to V<sub>dd</sub>, ground to output, and output to V<sub>dd</sub>. The HP4145B had the upper and lower current limits set to +/- 50  $\mu$ A, respectively.

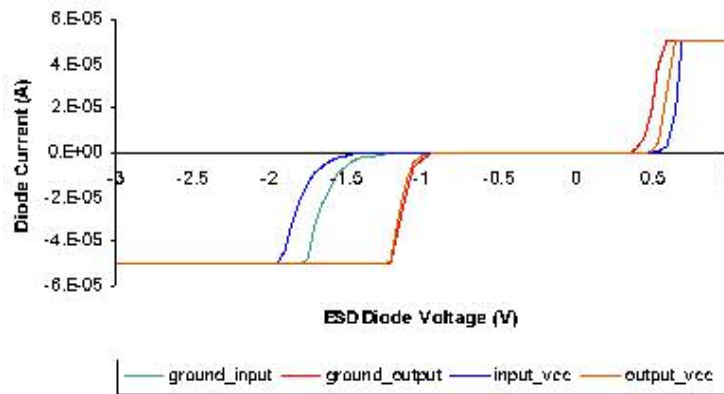


Figure B 1. Input and output I-V characteristics for 74HC04.

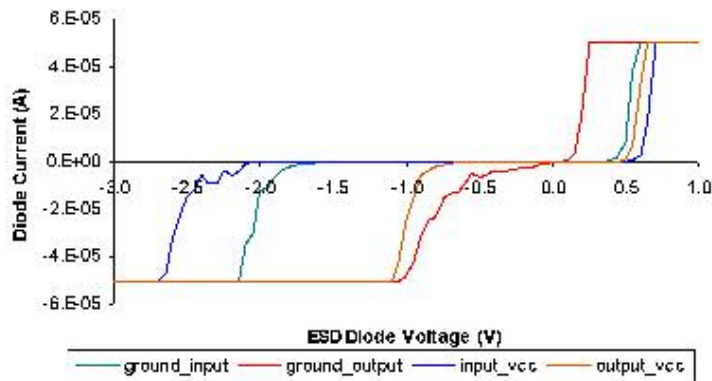


Figure B 2. Input and output I-V characteristics for 74HCT04.

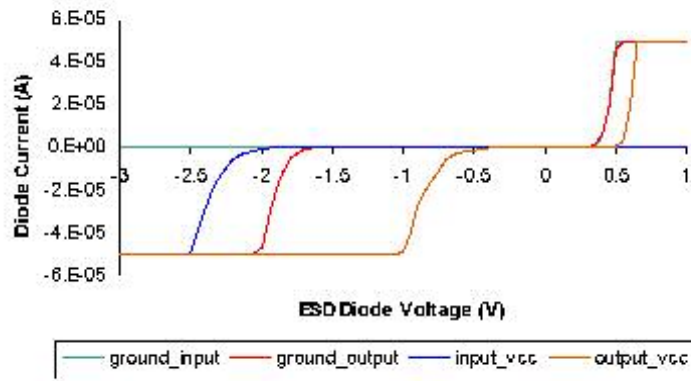


Figure B 3. Input and output I-V characteristics for 74AHC04.

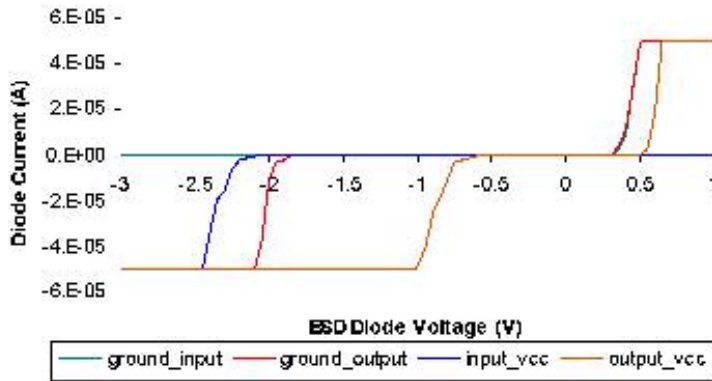
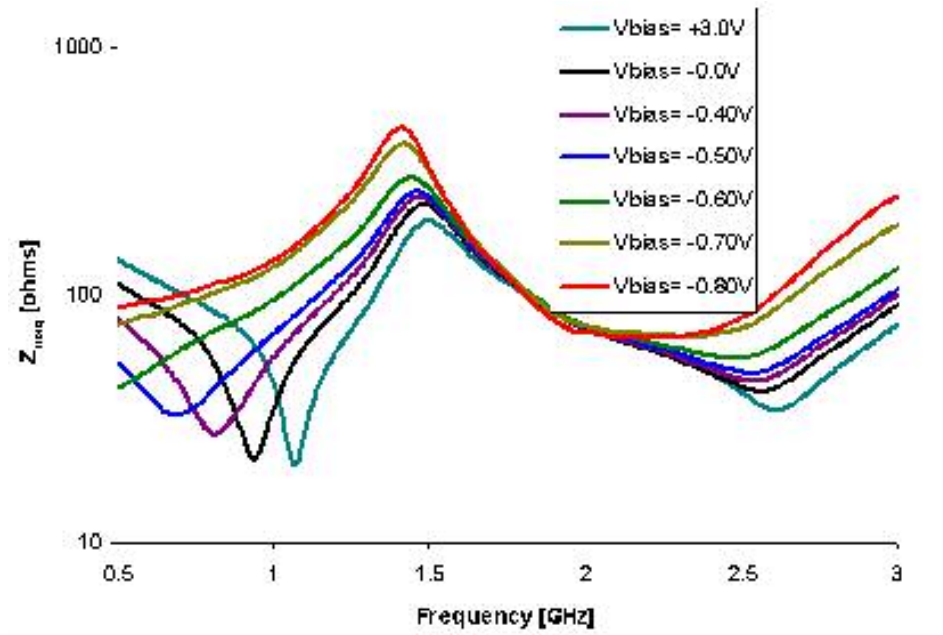
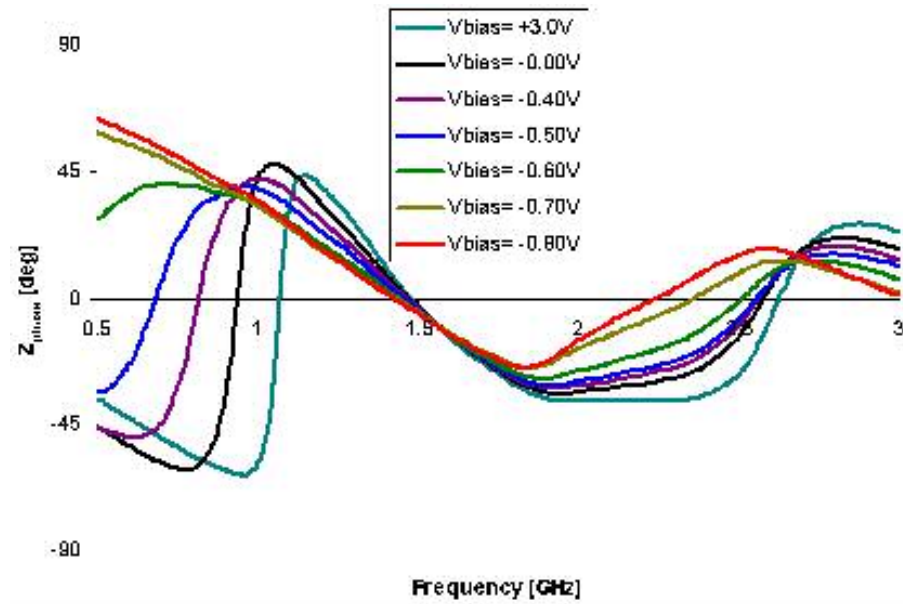


Figure B 4. Input and output I-V characteristics for 74AHCT04.

### Appendix C. Input impedance of various CMOS Inverters

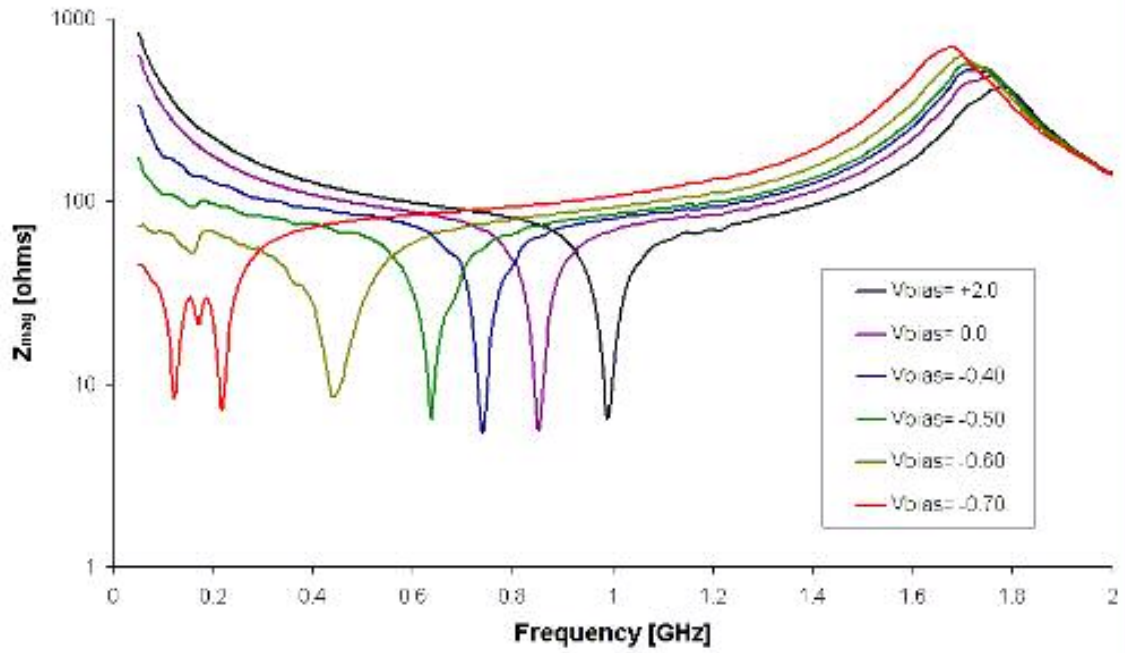


(a)

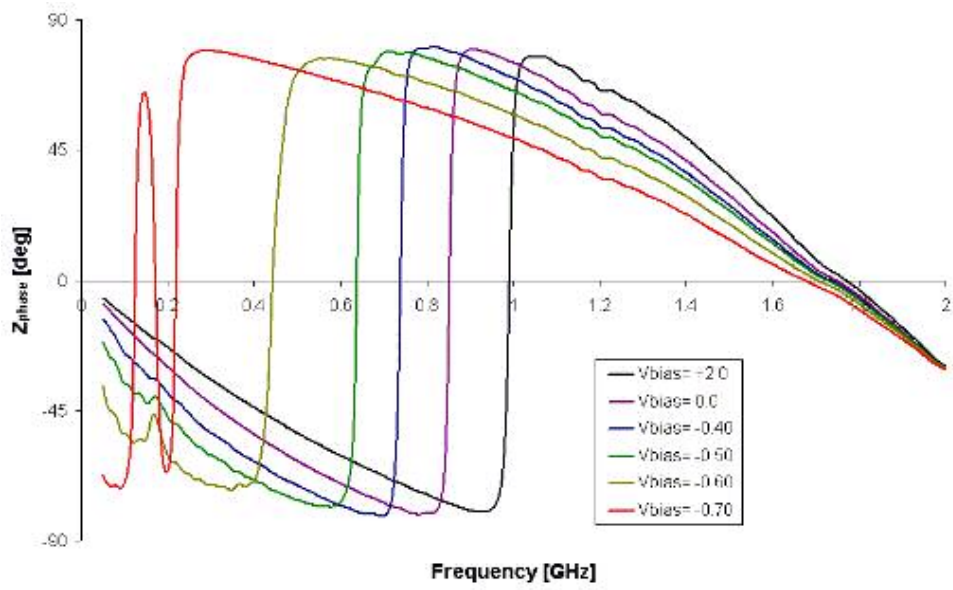


(b)

Figure C 1. Frequency response of the (a) input impedance and (b) phase of the 74HCT04 CMOS Hex inverter.

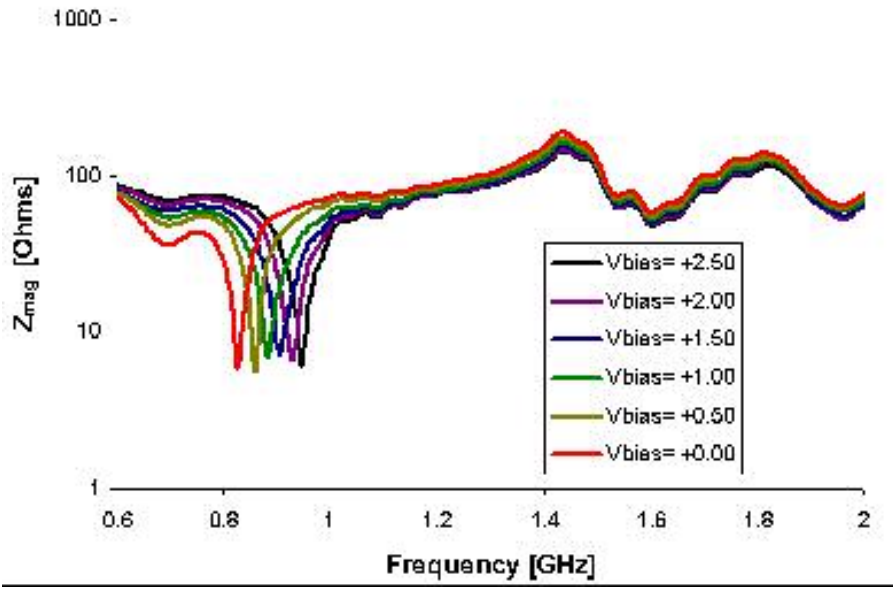


(a)

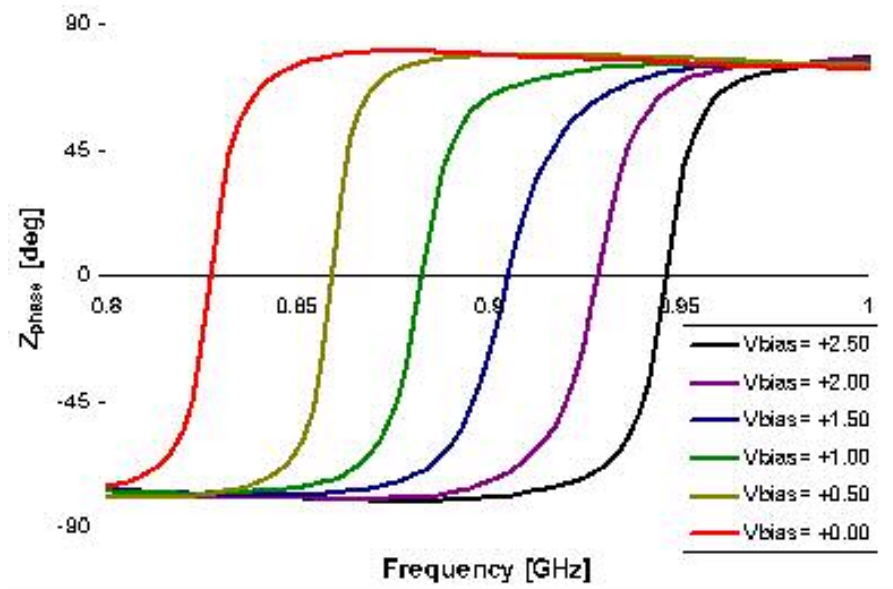


(b)

Figure C 2. Frequency response of the (a) input impedance and (b) phase of the 74ALVC04 CMOS Hex inverter.



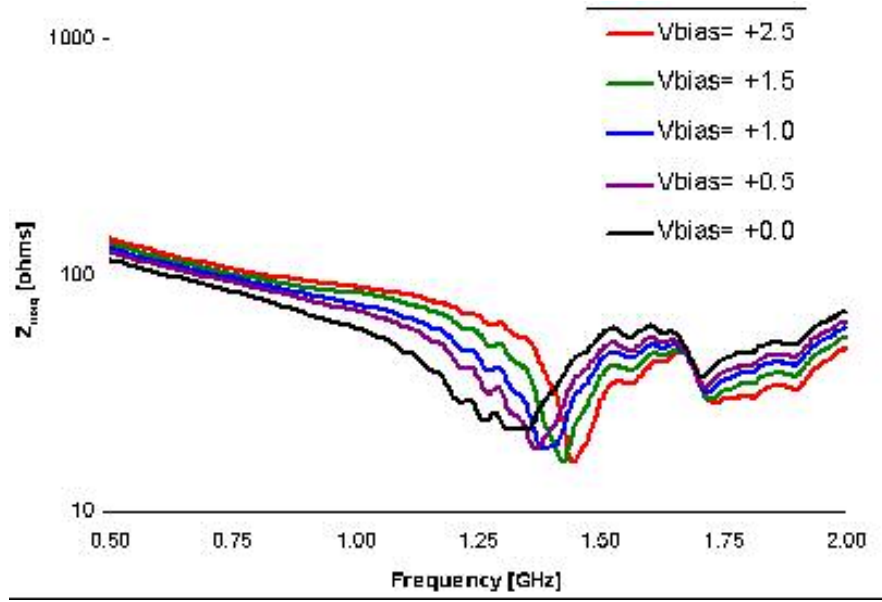
(a)



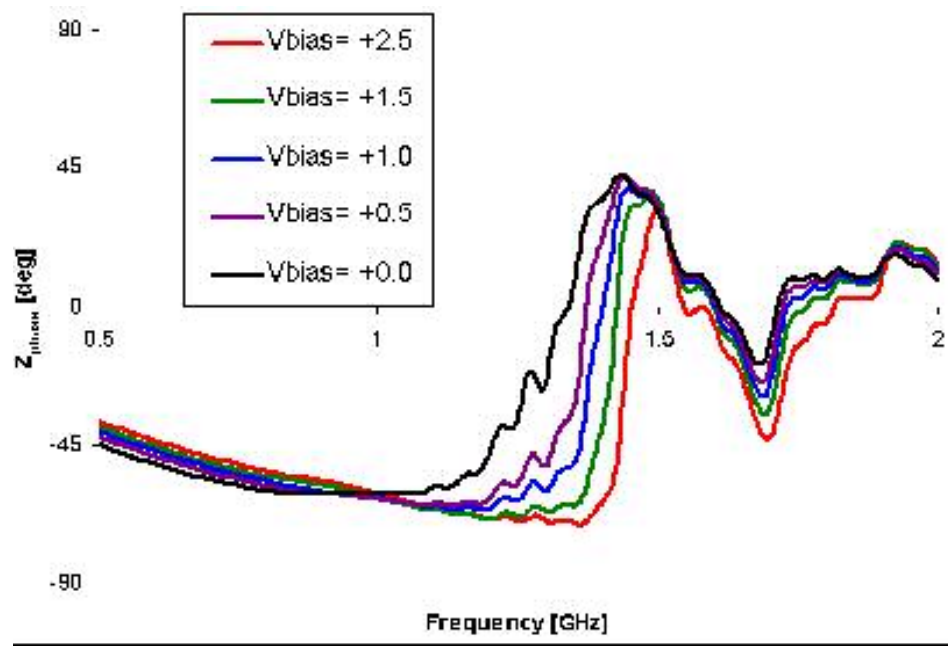
(b)

Figure C 3. Frequency response of the (a) input impedance and (b) phase of the 74LVC04 CMOS Hex inverter.





(a)



(b)

Figure C 4.Frequency response of the (a) input impedance and (b) phase of the 74LVX04 CMOS Hex inverter.

## Appendix D. Threshold Power Levels for Various Digital Circuit Families

The following graphs are the power threshold levels to cause a state change in the associated CMOS inverter. The input of the circuit was biased with the nominal output DC levels for the low ( $V_{ol}$ ) and high ( $V_{oh}$ ) states to simulate the voltages seen by a previous stage. Where only one curve is shown for a device, only the voltage indicated state changes with injected pulsed RF signals. The cutoff power level for the amplifier used was +30 dBm. The curves reaching +30dBm are indicating the threshold for the amplifier and not a state change. The RF signal has a pulse width of 100 ns and a PRI of 1.0 ms. The periodic fluctuations found in all the curves is associated with the mismatch of the injection coaxial junction and the input impedance of the DUT.

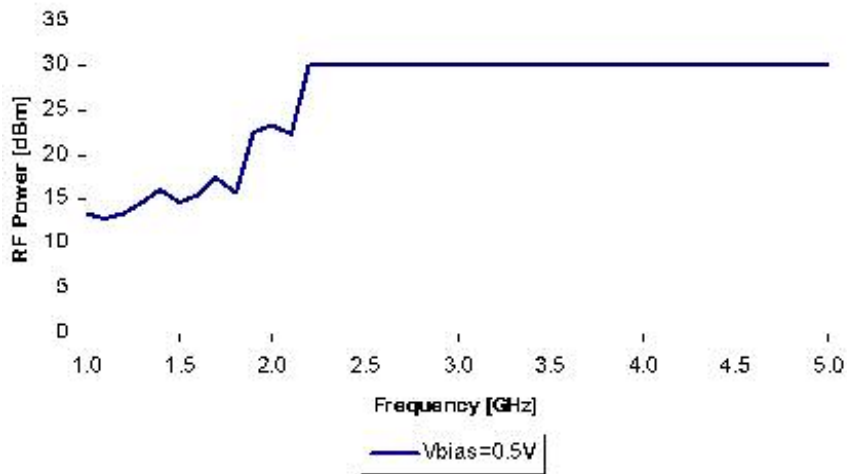


Figure D 1. Threshold power levels for the 74AC04 with the input biased to  $V_{ol} = 0.5V$  (blue) and  $V_{dd} = 5V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

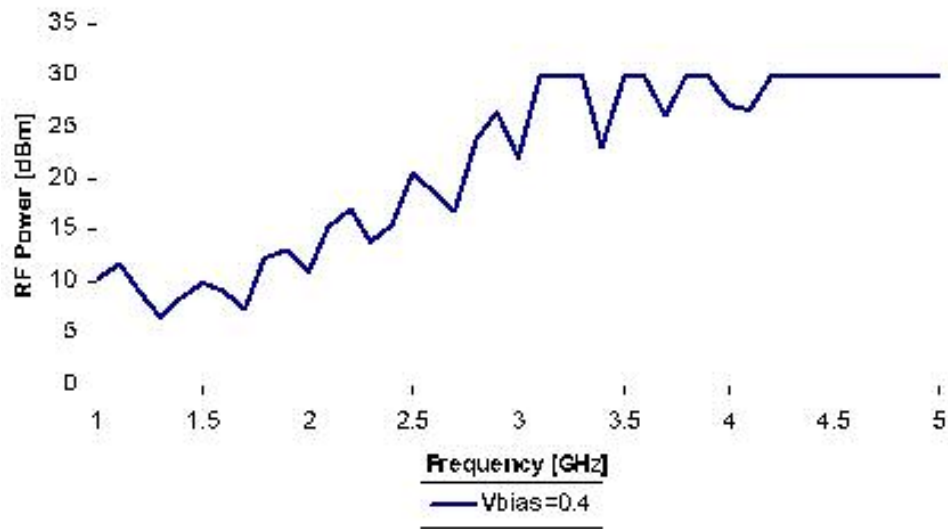


Figure D2. Threshold power levels for the 74ACT04 with the input biased to  $V_{ol} = 0.4V$  (blue) and  $V_{dd} = 5V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

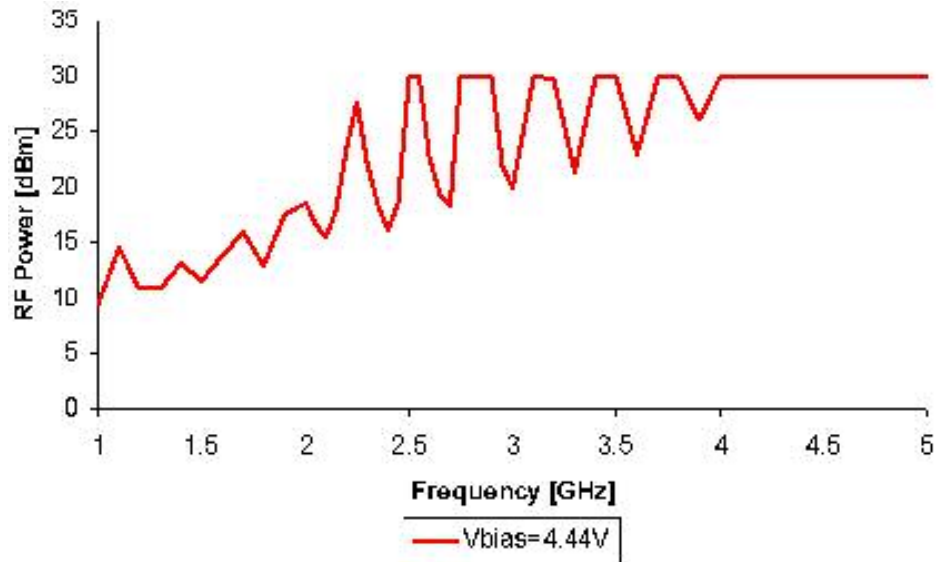


Figure D3. Threshold power levels for the 74AHC04 with the input biased to  $V_{oh} = 0.5V$  (red) and  $V_{dd} = 5V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

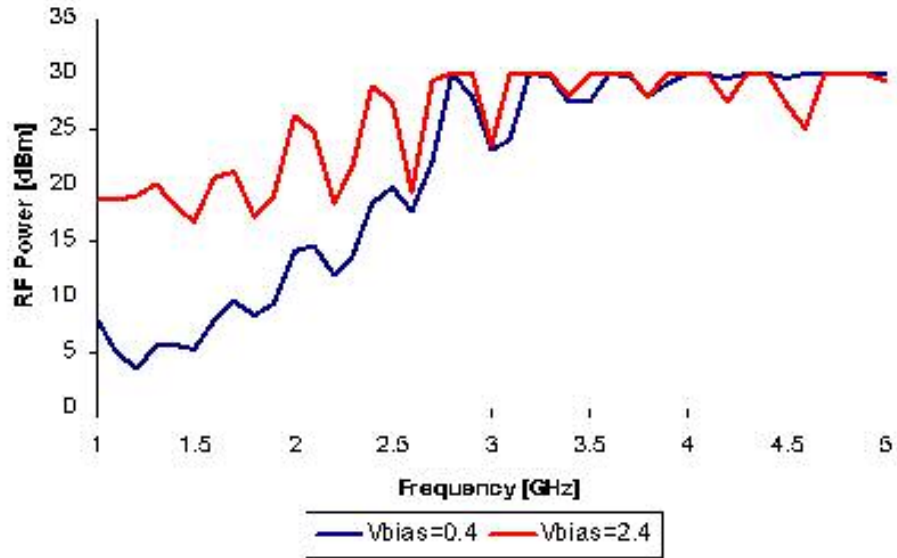


Figure D4. Threshold power levels for the 74AHCT04 with the input biased to  $V_{ol} = 0.4V$  (blue),  $V_{oh} = 2.4V$  (red), and  $V_{dd} = 3.3V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

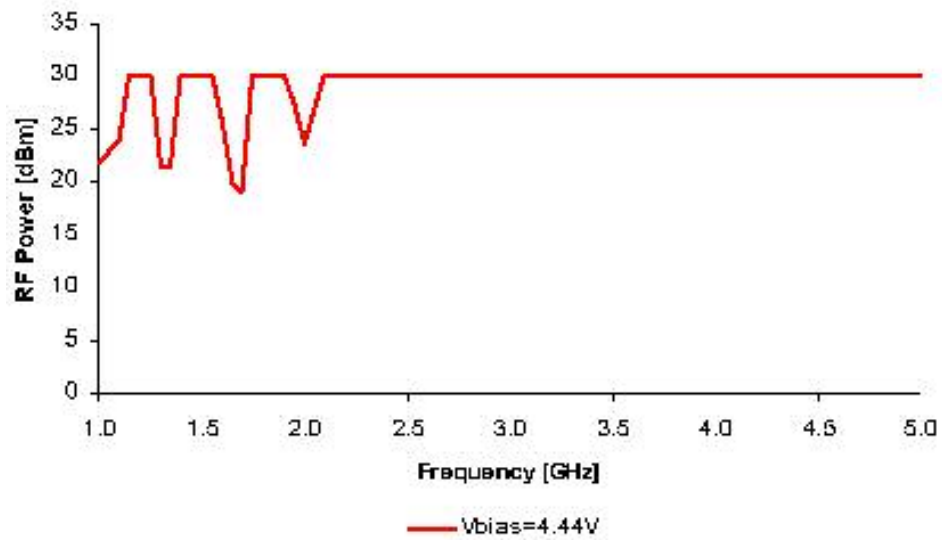


Figure D5. Threshold power levels for the 74HC04 with the input biased to  $V_{oh} = 4.44V$  (red) and  $V_{dd} = 5V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

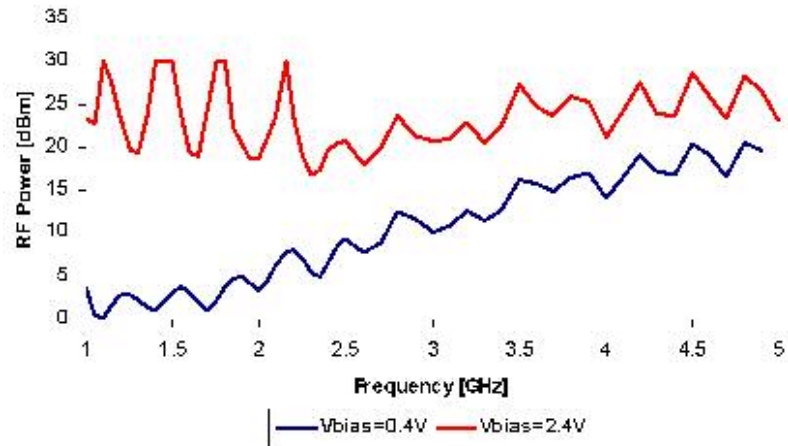


Figure D6. Threshold power levels for the 74HCT04 with the input biased to  $V_{ol} = 0.4V$  (blue),  $V_{oh} = 2.4V$  (red), and  $V_{dd} = 5V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

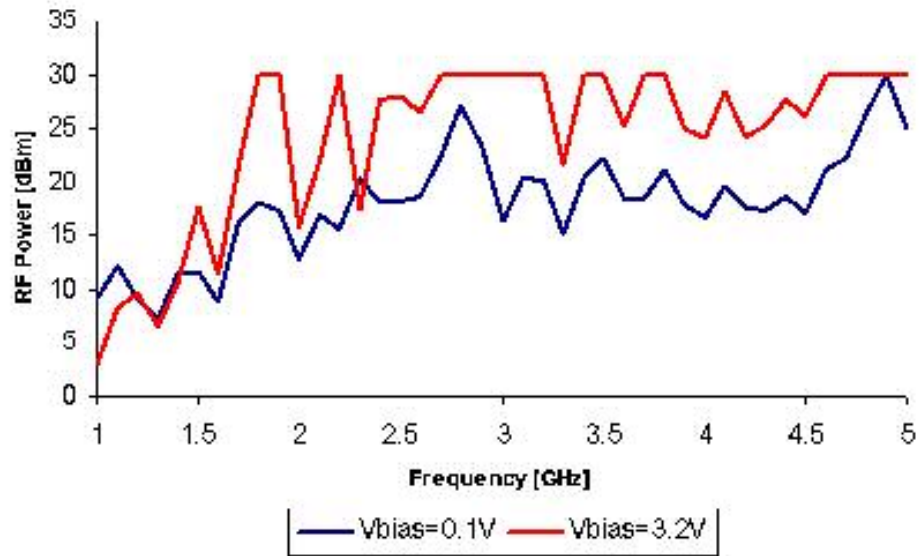


Figure D7. Threshold power levels for the 74ALVC04 with the input biased to  $V_{ol} = 0.1V$  (blue),  $V_{oh} = 3.2V$  (red), and  $V_{dd} = 3.3V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

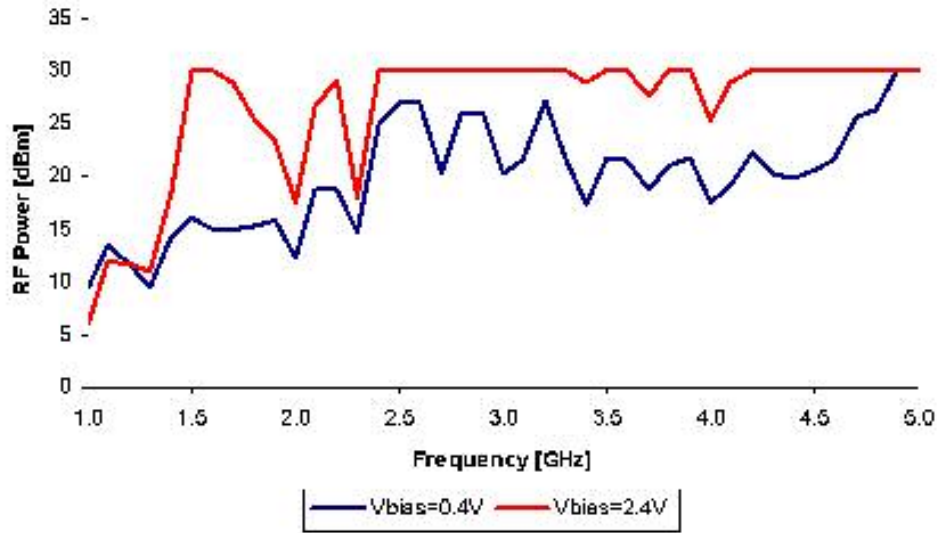


Figure D8. Threshold power levels for the 74LVC04 with the input biased to  $V_{ol} = 0.4V$  (blue),  $V_{oh} = 2.4V$  (red), and  $V_{dd} = 3.3V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

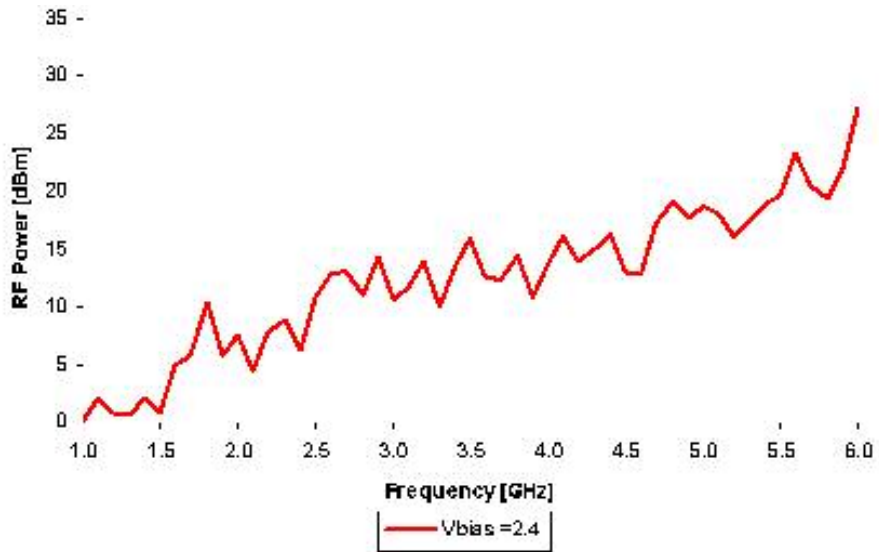


Figure D9. Threshold power levels for the 74LCX04 with the input biased to  $V_{oh} = 2.4V$  (red) and  $V_{dd} = 3.3V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

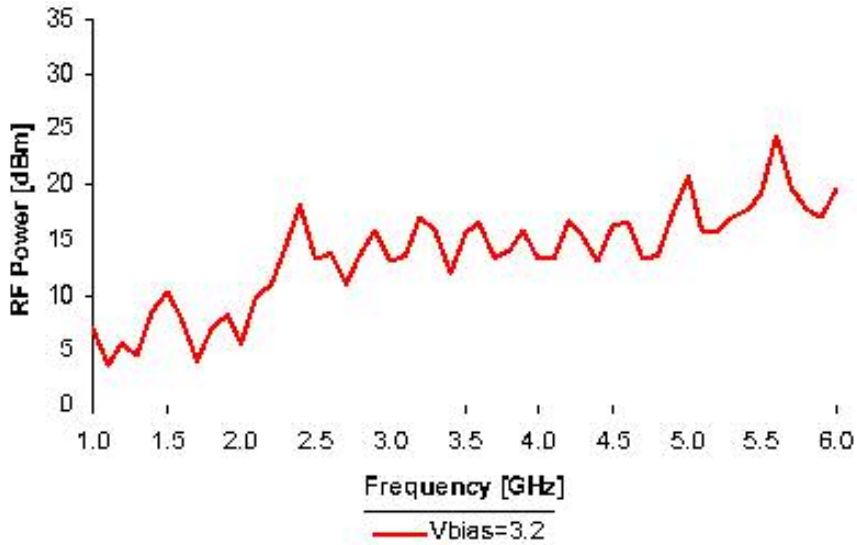


Figure D10. Threshold power levels for the 74LVX04 with the input biased to  $V_{oh} = 3.2V$  (red) and  $V_{dd} = 5V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

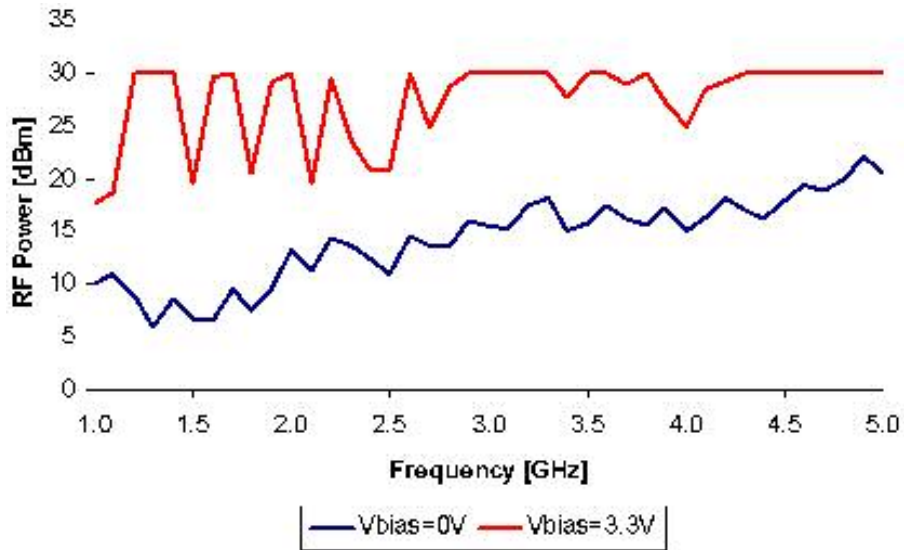
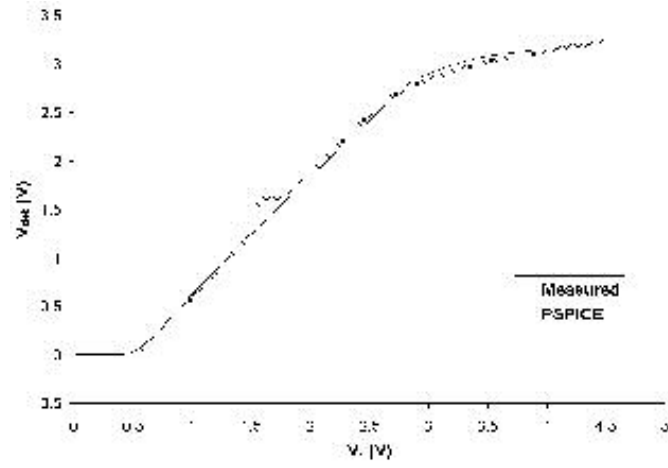
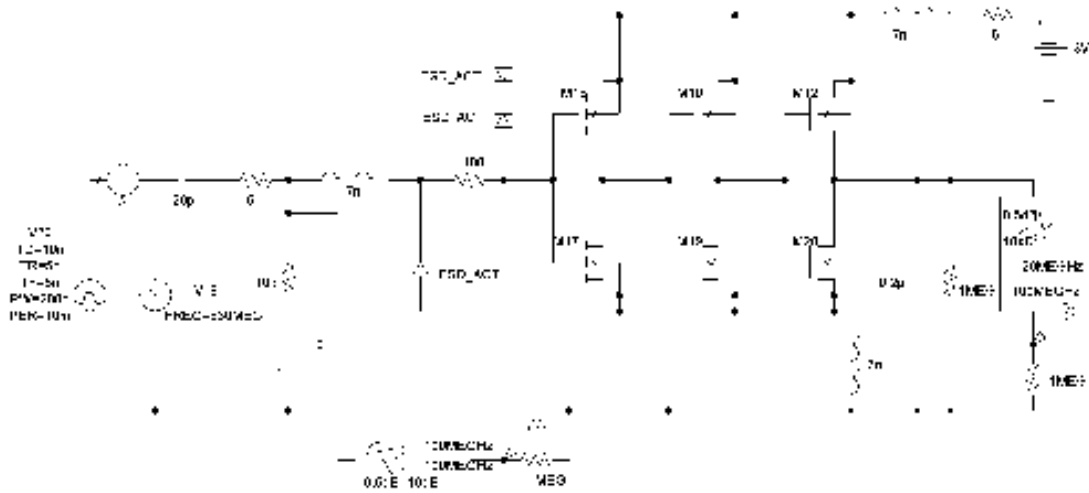


Figure D11. Threshold power levels for the 74VHC04 with the input biased to  $V_{ol} = 0V$  (blue),  $V_{oh} = 3.3V$  (red), and  $V_{dd} = 5V$ . The RF pulse had a pulse width of 100 ns and a PRI=1.0ms.

## Appendix E. Drive Curve for ACT Device



(a)



(b)

Figure E 1. (a) Drive curve for the ACT CMOS inverter and (b) the PSPICE circuit diagram used for the drive curve simulation.



## **Appendix F. CMOS Inverter Characteristics**

The following tables are parameters collected for all the CMOS inverter logic families considered in this thesis. The circuit parameter data was taken from manufacturer's datasheets. The 'High Level Susceptible' and 'Low Level Susceptible' values were extracted from the threshold power plots in Appendix D. The Highest Susceptible Frequency (HSF) is the highest frequency where effects were observed. The Lowest Susceptible Frequency (LSF) is the lowest frequency where effects were observed. The Lowest/Highest Susceptible Power Level (LSPL / HSPL) was the smallest/largest power level recorded that caused an effect. Injection experiments were reaching the power out limit of the RF amplifier where power levels indicated 32 dBm for a threshold power level. The power level as recorded from as the signal generator power level + 30 dB of amplifier gain. The LCX and LVX were tested up to 6 GHz. All other devices were tested to 5 GHz.

Table E 1. Parameter table for the AC, ACT, AHC, and AHCT logic families.

Logic Family	AC			ACT			AHC			AHCT		
<b>ESD Components</b>												
<b>Signal to Vcc</b>	N/A			N/A			In-line resistance, gate grounded and boot			In-line resistance, gate grounded and boot strapped mosfet in cascode		
<b>Ground to Signal</b>							LVTSCR - low voltage silicon controlled			LVTSCR - low voltage silicon controlled rectifier, line resistance, and gate		
<b>Characteristics</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>
Vcc	3	4.5	5.5	4.5		5.5	2	4.5	5.5	4.5	5	5.5
Vil (max)	0.9	1.35	1.65		0.8		0.5	0.9	1.65			0.8
Vih (min)	2.1	3.15	3.85		2		1.5	2.1	3.85	2	2	
Vol [V]	0.1	0.1	0.1	0.1		0.1	0.002	0.001	0.001		0.1	0.36
Voh [V]	2.9	4.4	5.4	4.4	0.1	5.4	2.9	4.4	5.4	3.94	4.5	
Vt	1.5	2.25	2.75		1.4							
dt/dv [ns/V] (rise/fall)		10			8	10	20		100		20	100
Input capacitance [pF]		4.5			4.5			2.8	10		3	10
<b>High Input Susceptible?</b>	No			No			Yes			Yes		
HSF [GHz]								4			4.7	
LSF [GHz]								1			1	
HSPL [dBm]*								32			32	
LSPL [dBm]*								12			18	
<b>Low Input Susceptible?</b>	Yes			Yes			No			Yes		
HSF [GHz]		2.25			4.2						3.75	
LSF [GHz]		1			1						1	
HSPL [dBm]*		32			32						32	
LSPL [dBm]*		15			7.5						5	

Table E 2. Parameter table for the ALVC, HC, HCT, and LCX logic families.

Logic Family	ALVC			HC			HCT			LCX		
<b>ESD Components</b>												
<b>Signal to Vcc</b>	Zener, in line resitance, back to back zener diodes			Diffused diode resistor			Diffused diode resistor, also two stages of inverters			N/A		
<b>Ground to Signal</b>	Zener, in line resitance, back to back zener diodes			Diode			Diode			Diode and other		
<b>Characteristics</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>
<b>Vcc</b>	1.65	2.3	3.6	2	4.6	6	4.5		5.5	2		3.6
<b>Vil (max)</b>	0.35*Vcc	0.7	0.8	0.3	0.9	1.2	0.8	0.8	0.8	0.7		0.8
<b>Vih (min)</b>	0.65*Vcc	1.7	2	1.5	3.15	4.2	2	2	2	1.7		2
<b>Vol [V]</b>	0.45	0.7	0.55	0.1	0.1	0.1		0.2	0.26	0.2	0.4	0.6
<b>Voh [V]</b>	Vcc-0.2	1.7	2.4	1.9	4.5	5.9		3.84	3.98	1.8	2.2	2.4
<b>Vt</b>				1.4	2.25	3		1.4				
<b>dt/dv [ns/V] (rise/fall)</b>		5		400	500	1000	125		500		10	
<b>Input capacitance [pF]</b>		3.5			4	10		5	10		7	
<b>High Input Susceptible?</b>	Yes			Yes			Yes			Yes**		
<b>HSF [GHz]</b>		4.5			2.25			5			6	
<b>LSF [GHz]</b>		1			1			1			1	
<b>HSPL [dBm]*</b>		32			32			32			30	
<b>LSPL [dBm]*</b>		3.1			21			18			3	
<b>Low Input Susceptible?</b>	Yes			No			Yes			No		
<b>HSF [GHz]</b>		4.8						5				
<b>LSF [GHz]</b>		1						1				
<b>HSPL [dBm]*</b>		32						22				
<b>LSPL [dBm]*</b>		5						2				

Table E 3. Parameter table for the LVC, LVX, and VHC logic families.

Logic Family	LVC			LVX			VHC		
<b>ESD Components</b>									
<b>Signal to Vcc</b>	In line resitance, back to back zener diodes			N/A			Inline resistance, and gate grounded mosfet		
<b>Ground to Signal</b>	Zener, in line resitance, back to back zener			N/A			Diode, in-line resistance and gate grounded mosfet		
<b>Characteristics</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>
<b>Vcc</b>	1.65		3.6	2	3	3.6	2		5.5
<b>Vil (max)</b>		0.8		0.5	0.8	0.8	0.5	0.3*Vcc	0.3*Vcc
<b>Vih (min)</b>		2		1.5	2	2.4	1.5	0.7*Vcc	0.7*Vcc
<b>Vol [V]</b>		0.2		1.9	2.9	2.58	0.1	0.1	0.1
<b>Voh [V]</b>	Vcc-0.2	1.2	1.7	0.1	0.1	0.36	1.9	2.9	4.4
<b>Vt</b>		1.5							
<b>dt/dv [ns/V] (rise/fall)</b>		5/10		0		100		100	20
<b>Input capacitance [pF]</b>		5			4	10		4	10
<b>High Input Susceptible?</b>	<b>Yes</b>			<b>Yes**</b>			<b>Yes</b>		
<b>HSF [GHz]</b>		4.3			6			4.2	
<b>LSF [GHz]</b>		1			1			1	
<b>HSPL [dBm]*</b>		32			24			32	
<b>LSPL [dBm]*</b>		8			4			20	
<b>Low Input Susceptible?</b>	<b>Yes</b>			<b>No</b>			<b>Yes</b>		
<b>HSF [GHz]</b>		4.75						5	
<b>LSF [GHz]</b>		1						1	
<b>HSPL [dBm]*</b>		32						25	
<b>LSPL [dBm]*</b>		11						7	

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