ABSTRACT

Title of Dissertation: ADVANCED BACK-END PROCESSING TECHNIQUES FOR INFRARED FOCAL PLANE ARRAYS

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With the continued scaling of infrared focal plane array (FPA) pixel pitch down to the diffraction limit, current backend processing techniques are becoming less viable. For one class of detectors, FPAs are formed when pixels of a detector array are electrically connected to analogous elements on a separate readout integrated circuit (ROIC) chip with malleable In bumps. Currently, these In bumps are formed by a standard thick photoresist liftoff process. Maintaining high connectivity with this process becomes difficult or impossible as pitch is reduced because of liftoff failure due to the increased aspect ratio required of bumps. Another class of infrared FPAs epoxies the detector array to the ROIC. A via is etched through the detector material of each pixel down to ROIC contact pads. Interconnects are currently formed by evaporating metal into the via, linking the detector array to the ROIC. As pixel pitch is reduced, obtaining proper interconnect becomes increasingly difficult due to the line of sight requirement of evaporation.

In this work, two novel techniques to realize reduced pitch interconnects were developed and demonstrated that do not have the limitations of current techniques. For

In-based FPAs, a template transfer process was developed that does not require a thick liftoff process. In this technique, In bumps are formed by electroplating on a separate, patterned template wafer and then transferred to the detector array or ROIC using a flip-chip bonder. A low-friction, amorphous fluoropolymer was used to shape the bumps and encourage transfer from the template wafer. A proof of principle for this process was obtained, demonstrating the transfer of 5.5 μm thick, 10μm pitch In bumps to a mechanical ROIC. For the via-based FPAs, interconnection was achieved by electrochemical deposition of Ni films. Both electroplated and electroless Ni processes were developed for this purpose. After confirming the compatibility of these processes with detector and ROIC materials, Ni was plated into the vias of active HgCdTe photodetectors. This resulted in diffusion limited I-V characteristics that were stable through thermal cycling. Electroless Ni via contacts formed on an active 5 μm pitch FPA resulted in 99.94% connectivity.

Advanced Back-End Processing Techniques for Infrared Focal Plane Arrays

By

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Dissertation submitted to the Faculty of the Graduate School of the
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Dedication

To Tatiana, who has had the 'joy' of emotionally supporting me
while I worked through this process.

Acknowledgements

I would like to start by thanking my advisor, Professor John Melngailis for the support and direction he has given me through the course of my time at the University of Maryland. Each of my colleagues at the U.S. Army's Night Vision Laboratory have also helped me in some way through the course of my research. More specifically, I would like to tank Peter Smith for the amount of time he put in to work with me on the SEM, Dr. Marvin Jaime-Vasquez for collaborating with me for surface analysis data, and Dr. J. David Benson for mentoring me and introducing me to a more Zen approach towards research. Other collaborators I would like to thank include: James Pattison at the Army Research Lab for working with me on ICP etching, the staff at the University of Maryland's FabLab (Tom Loughran, John Abrahams, and Jonathan Hummel) for instructing me on the equipment in the lab and discussing how to improve aspects of my processes, Professor Suk-Ryong Hahn of the Physics Department at the University of Illinois at Chicago for opening his lab space to me, and Dr. Jeremy Bergeson of EPIR Technologies for working with me on the flip-chip bonder,

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Chapter 1

Introduction and Background

1.1 Statement of the Problem and Major Accomplishments

As pixel pitches of infrared focal plane arrays (FPAs) are reduced, aspects of their backend processing present roadblocks in moving the technology forward. More specifically, this refers to the hybridization of detector arrays to readout integrated circuits (ROICs). One interconnection architecture uses roughly 5 to 10 μm tall In bumps for hybridization. Currently, these bumps are fabricated by a thick resist liftoff process with thermal evaporation of In to form them. With further reduction of pixel pitches below 15 μm, this fabrication technique difficult or impossible to implement due to lateral growth of In on the photoresist, obscuring deposition of well formed bumps. Large crystallites tend to form on top of the photoresist, further obscuring the deposition of the bumps. Because of these issues, a process that does not require a thick resist liftoff In bump process is necessary to reduce pixel pitch. Another hybridization scheme makes use of contact metallization deposited on the inside surface of vias to interconnect the detector array to the ROIC. Evaporation is currently used to form this contact, which requires line of sight for deposition. As pitches are reduced and vias are scaled accordingly, meeting this requirement becomes increasingly difficult, resulting in open contacts across an FPA. Because of this, development of a technique that does not require line of sight becomes necessary. The goal of this thesis is to develop a proof of principle

for innovative, previously unused means, to fabricate interconnects at a 10 μm pitch or below that do not have the roadblocks described above.

Fabrication of In bumps was demonstrated for the first time using a template transfer process to realize bumps at a 10 μm pitch, where In bumps were formed on a separate template wafer and transferred to a mechanical ROIC after their formation. Within this effort, a novel hot embossing process was developed to form patterns with a controlled positive sidewall angles in amorphous fluoropolymer films with thicknesses of roughly 6 μm and pitches down to 6 μm. Additionally, an improved In electroplating process was developed that optimized the thickness uniformity, grain structure, and morphology of In bumps. 7% uniformity was obtained for roughly 10 μm thick, 12 μm pitch bumps in a 720p format array with submicron grains and nearly flat bump tops.

For via-based interconnects, a viable electroless Ni contact metallization process was developed and demonstrated for the first time for state-of-the-art 5 μm pitch FPAs with a 99.94% connectivity. Within this effort, characteristics of both electroless and electroplated Ni, including composition, film stress, and resistivity were confirmed to be compatible for via contact metallization. Cryogenically stable contact were demonstrated for active 20 μm pitch test structures with no discernible changes to I-V characteristics compared to the baseline evaporation process.

1.2 Introduction to Infrared Focal Plane Arrays

Currently, infrared sensing for military applications is typically achieved by a two-dimensional staring array of pixels, called a detector array. Collection of incident radiation can be achieved by a variety of mechanisms. One of the main methods is by excitement of electrical carriers in a semiconductor. Given the low energy of infrared radiation, on the order of 100 to 1000 meV, small bandgap semiconductors are required. Both III-V semiconductors, including InSb [1] and $In_{1-x}Ga_xAs$ [2], along with II-VI semiconductors, including $Hg_{1-x}Cd_xTe$ [3], have been used for this purpose. Additionally, bandgap engineered materials composed of semiconductor superlattices to extend the cutoff wavelength of detectors have been developed. Examples of such are quantum well infrared photodetectors (QWIPs) [4] and type-II strained layer superlattices (SLS) [5]. Other methods of infrared collection include thermal collection, where the radiation heats the detector, changing its fundamental properties. Microbolometers are an example of this, where the resistance of the device changes as it is heated by the incident radiation [6]. Materials with a high thermal coefficient of resistance (TCR), such as VO_x or α-Si, typically form the absorbing surface.

This thesis will focus primarily on aspects of fabrication of detector arrays composed of HgCdTe sensing layers epitaxially grown on lattice-matched $Cd_{1-y}Zn_yTe$ substrates, however it is anticipated that the processes developed in this study will be applicable to a broader family of detector types. Such arrays are among the highest performing for a variety of reasons. The primary advantages of HgCdTe over other sensing materials include: a high optical absorption coefficient, high quantum efficiency, and the ability to tune the bandgap for sensitivity across a large portion of the infrared

spectrum (1-20μm) by adjusting Hg content [7]. However, with these advantages come several drawbacks. First of all, HgCdTe is a brittle material due to a weak Hg-Te bond [8]. Additionally, all processing must be performed under 90°C as Hg tends to diffuse out of HgCdTe at higher temperatures, thus changing its fundamental properties [9].

While the detector array has the ability to sense incident photons, it cannot index the amount of light striking each pixel to formulate an image. This information must be read out by a completely separate set of circuitry. Due to the difficulties of processing HgCdTe, this circuitry cannot be monolithically integrated on the same wafer as the detector array. Instead, this circuitry is fabricated on a separate Si wafer called a readout integrated circuit (ROIC). In order to properly read out information from the array to the ROIC, an element by element connection must be made between the two wafers. This linking process is known as hybridization and the result is the formation of a focal plane array (FPA). Depending on type of infrared detector, several schemes are currently used to hybridize the detector array and ROIC. These schemes will be discussed in Section 1.2 below.

Historically, one of the main thrusts of FPA development has been to increase resolution which allows for improved images with the ability of longer range detection. Figure 1.1 plots the number of pixels per array historically, similar to Moore's Law for transistor count on an integrated circuit [10]. This figure shows how the resolution of FPAs has steadily increased over time. Obtaining higher resolution FPAs can be achieved two different ways. The first is to physically increase the size of the FPA, allowing for more pixels to fit on it. While aspects of producing larger arrays are straightforward, several things make it undesirable. To start with, materials costs are high compared to Si

processing. CdZnTe substrates alone cost on the order of $200 per cm^2 compared to less than $1 for Si. In addition, producing high quality, single-crystal CdZnTe substrates is difficult. In many cases, larger substrates have low-angle grain boundaries running through them resulting in poor detection in those regions.

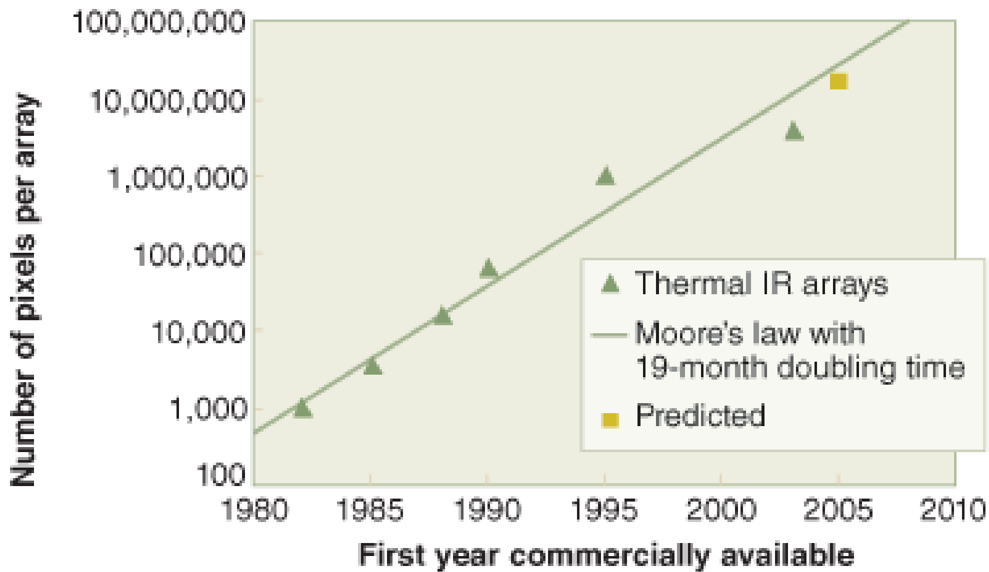

Figure 1.1: A plot of the pixel count on commercially produced infrared FPAs through time. Reprinted from A. Hoffman, Laser Focus World [10].

Consequently, yields tend to be reduced when producing larger arrays. The preferable way to increase resolution has been to reduce the size of pixels in an FPA, thus increasing pixel density. Figure 1.2 plots historical FPA pixel density, showing the steady reduction of pixel size over time [11]. Enabling technologies, such as the use of improved photolithography techniques and replacing isotropic wet-etching with anisotropic plasma based etching to name a few, have allowed for this [12]. State-of-the-art single-color FPAs with a 15µm pitch have been reported [13]. Additionally, two-color mid-wave/long-wave FPAs with a 25µm pitch have been achieved [14]. The reduction of

pixel size will likely continue until it is on the order of the diffraction limit of the radiation to be detected, roughly equal to its wavelength. For shortwave infrared (SWIR) these values are 1-3 μm, for midwave infrared (MWIR) 3-5 μm, and for longwave infrared (LWIR) 8-12 μm. Based on the state-of-the-art, there is still room to reduce pixel sizes further for increased resolution.

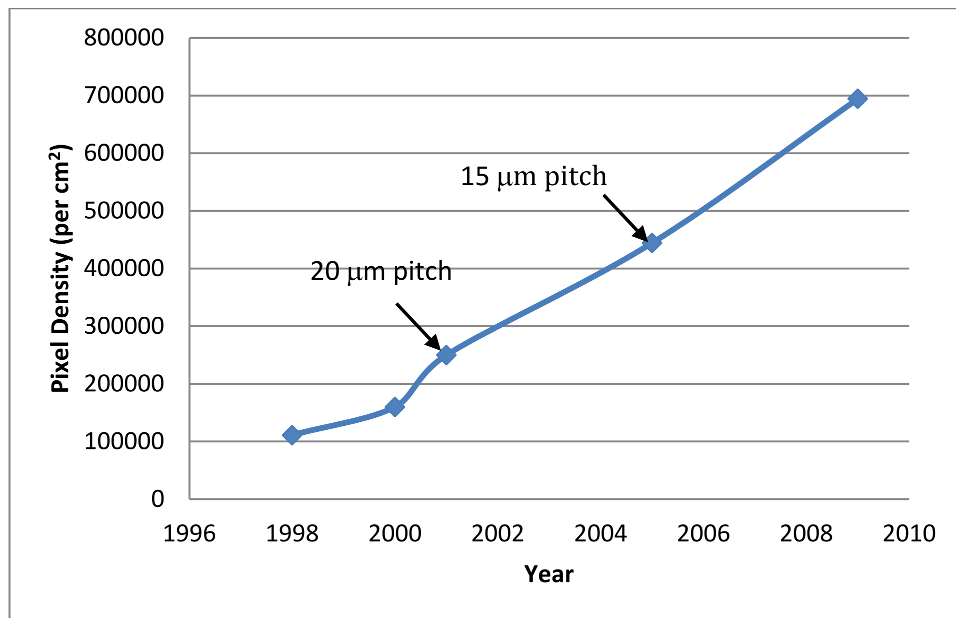

Figure 1.2: A plot of the pixel density found on infrared FPAs through time. Reprinted from P. Bremond, Photonics Tech Briefs [11].

1.3 Backend Processing Challenges of Further Pixel Reduction

In addition to challenges in producing FPAs with smaller pixels and ROICs with smaller unit cell, challenges in backend processing exist that must be overcome to allow for a high yield hybridization process. In this section, the two main types of hybridization

processes along with their limitations in further scaling will be discussed: indium bumps and via contact metallization.

1.2.1 Indium Bump Hybridization

One way to hybridize the detector array to the ROIC is to link each detector to its analogous unit cell on the ROIC with a conducting bump bond. As shown in Figure 1.3, the resulting FPA is backside illuminated. The relatively large bandgap of CdZnTe, given at room temperature by:

$$E_0 = 1.4637 + .49613y + .2289y^2 \quad (1.1)$$

ensures that it is transparent to incident infrared radiation, allowing for the bulk of absorption to occur at the HgCdTe detector [15].

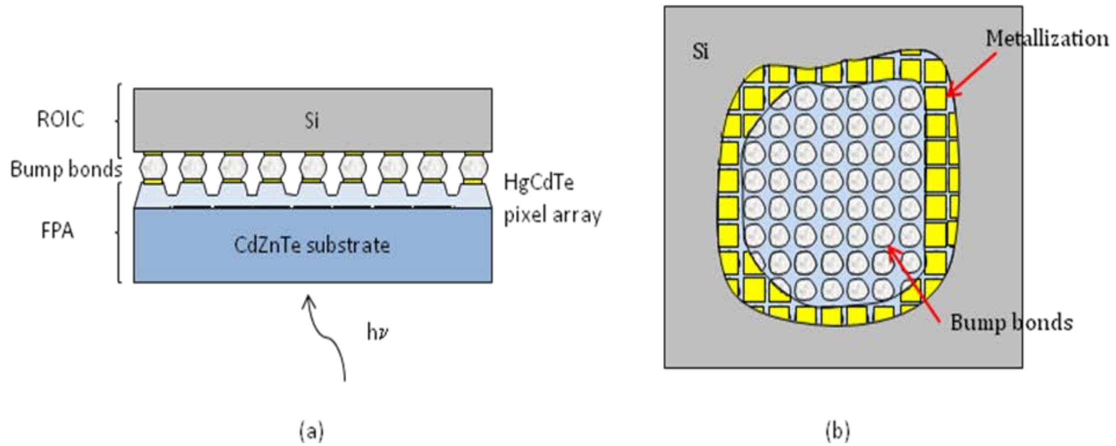

Figure 1.3: Schematic of a backside illuminated FPA hybridized to an ROIC with bump bonds: (a) cross-sectional view and (b) top view.

When attempting to find an optimal bump bonding material to hybridize the two wafers, one critical issue must be considered: HgCdTe and Si have a large difference in thermal coefficient of expansion. Depending on the x-value of HgCdTe, this ranges from 4.3×10^{-6} K^{-1} to 4.8×10^{-6} K^{-1} [16], and for Si, this value is 2.4×10^{-6} K^{-1} [17]. These values were obtained at roughly 280° K. Because HgCdTe is a narrow gap semiconductor, a relatively large number of carriers are thermally generated, leading to greater noise in a resulting image. Suppression of this noise, and hence improved detector performance, necessitates cooling of the detector. This is especially true of MWIR and LWIR sensors, where cryogenic cooling down to 77° K is required [8]. When this cooling takes place, the ROIC and detector array will contract by different amounts due to the differences in thermal coefficient of expansion. The bump bonds must, therefore, have the ability to comply with the stress caused by the different contraction. In, due to its high degree of plasticity, has emerged as the preferred material for this purpose [18].

The standard procedure for fabricating In bumps is performed on both the FPA and ROIC, and is called double-sided bumping. This process is shown in Figure 1.4, where only processing of the ROIC is illustrated for simplicity. A thick layer of negative photoresist is spun onto both the FPA and ROIC. This layer is then defined by a photolithography step with exposure time carefully controlled to produce enough of a negative sidewall slope to permit good liftoff shown in Figure 1.4a. A layer of In is then deposited by thermal evaporation shown in Figure 1.4b [19]. Finally, a liftoff process removes the photoresist layer and excess In shown in Figure 1.4c. After this process, both the FPA and ROIC are loaded onto a flip-chip bonder and held by a vacuum chuck. This device is capable of precisely aligning the two wafers. Once aligned, the flip-chip bonder

heats and presses the wafers together shown in Figure 1.4d. The result is a permanent bond of the In connecting the FPA to the ROIC shown in Figure 1.4e.

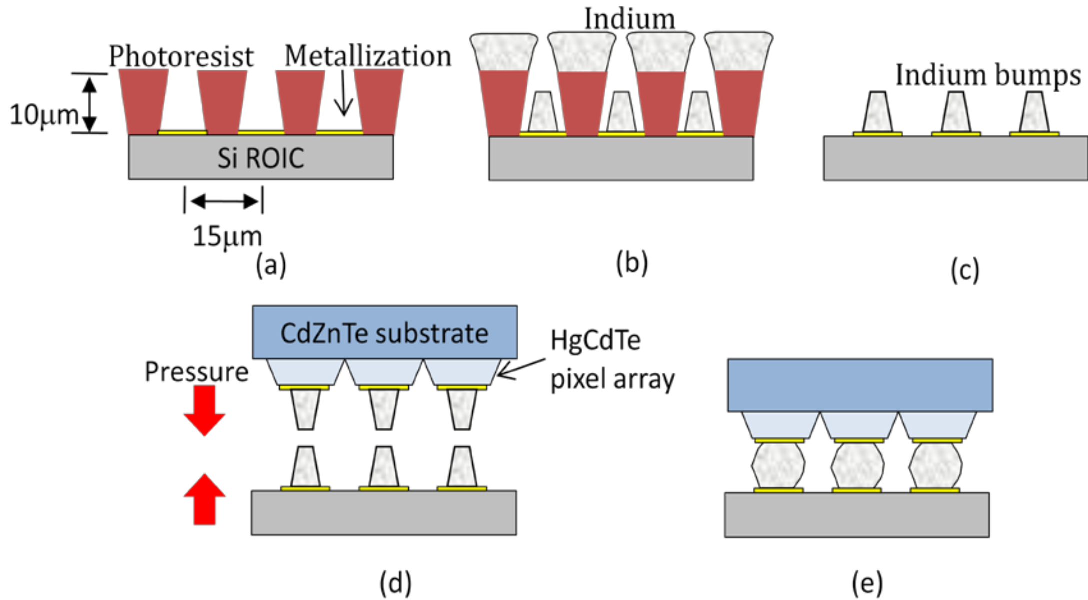

Figure 1.4: Process flow for indium bump bond fabrication and hybridization: (a) photolithography step, (b) evaporation of indium, (c) liftoff step, (d) hybridization and (e) final structure.

The relatively large thickness of the bump bonds is critical for several reasons. First, the bonds must be able to comply with stress due to the different thermal coefficients of expansion of the FPA and ROIC, as already discussed. If the bonds are not thick enough, they may crack or pull away when the hybridized FPA is thermally cycled. Second, there is no final chemical mechanical polishing (CMP) step in the fabrication of FPAs to ensure planarity of pixels across the entire wafer. It is, therefore, necessary for the In bumps to be able to make up for this non-planarity. If the bumps are made too thin, there is some chance that not all pixels will be physically connected to the ROIC after the hybridization step.

As one attempts to scale down the pitch of bumps, the bump height must remain relatively large for successful hybridization, resulting in increased aspect ratios. This is not compatible with the evaporation/liftoff process for several reasons. First, lateral growth of In on the photoresist during evaporation will eventually pinch-off growth of the In bump. The resulting bump will be shorter than expected or malformed. Even if the bump is nearly as tall as required, the lifting off procedure may become impossible as there will be no route for chemicals to dissolve the photoresist. This pinch-off process is illustrated in Figure 1.5.

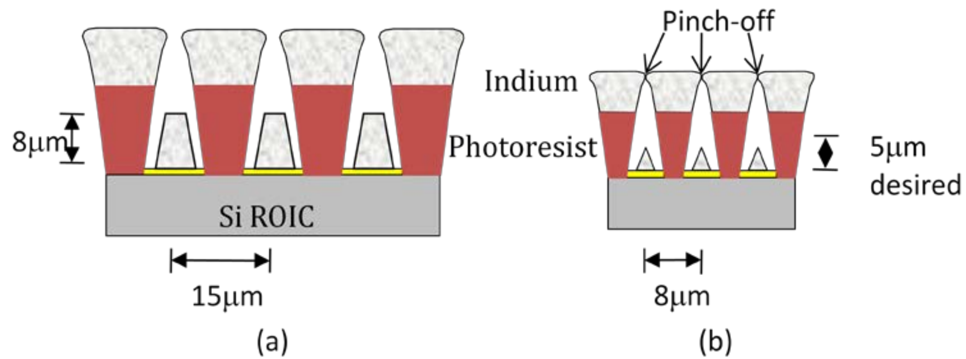

Figure 1.5: Lateral growth of indium during evaporation at two different bump pitches: (a) for current technology and (b) scaled down pitch where growth of the indium bump is inhibited by pinch-off.

In addition to this pinch-off problem, there is another obstacle that puts a lower limit on bond pitch. As previously discussed, a negative sidewall slope is required for good liftoff of excess In. As the bond pitch decreases, bond height can only be scaled in a sub-linear fashion for successful hybridization. Meanwhile, sidewall slope should remain constant for good liftoff. Thus, when scaling down far enough, no cross-linked photoresist will remain in contact with the wafer surface while attempting to satisfy both

of these requirements. The end result is that the entire photoresist layer washes away after development, and no further steps are possible. This problem is illustrated in Figure 1.6.

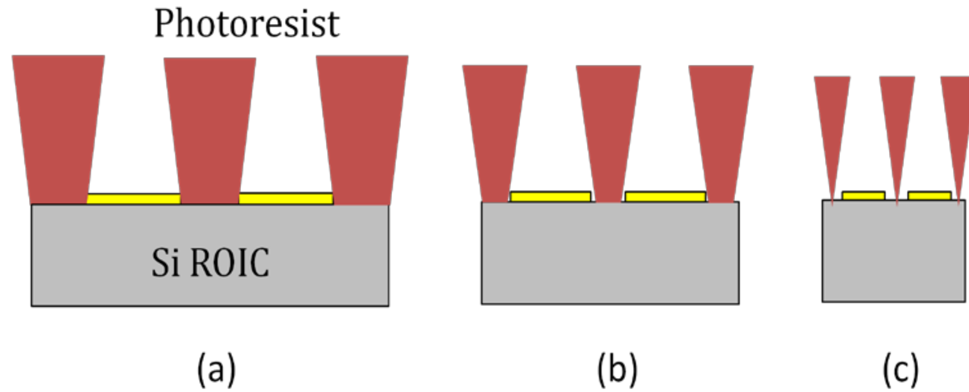

Figure 1.6: The effect of scaling down bump pitch on the amount of cross-linked photoresist in contact with the wafer. Scaling down to (c) could not occur as the photoresist would wash away when developed.

While these difficulties give a hard lower limit to bump pitch using the thick resist liftoff process, there are a variety of other issues that will affect the yield of successful bonds as state-of-the-art bump pitch is reduced. The formation of crystallites occurs during the evaporation process due to high surface mobility of the impinging In [20]. If a crystallite forms at an edge where there is an opening in the photoresist, it can partially block deposition of the In bump bond, as shown in Figure 1.7. While this crystallite may not have much of an effect on the deposition of a larger bump shown in Figure 1.7a, it will block more and more of the bump deposition as pitch is decreased shown in Figure 1.7b. Eventually, as pitch is reduced further, this crystallite blocks off deposition of the bump completely shown in Figure 1.7c.

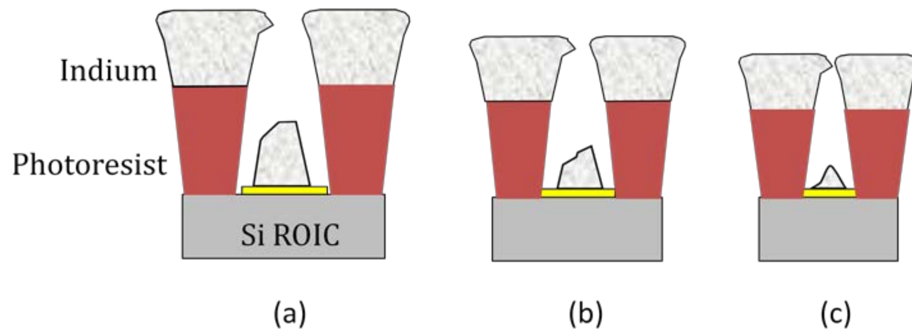

Figure 1.7: The effect of crystallites on bump deposition of different pitches.

An added problem for hybridization with small bump pitches is that the liftoff process can cause damage to In bumps. As bumps are scaled down, they become more fragile and liftoff can smear bumps, making them useless for hybridization. Additionally, as bump size decreases, contact area with the metallization underneath decreases. The result is a bond with smaller total adhesion to the layer below. The liftoff process can also rip smaller In bumps away, diminishing successful bump yield.

1.2.2 Hybridization by Via Contact Metallization

Another hybridization scheme for FPA fabrication is shown in Figure 1.8. This process does not rely on In bumps to connect the detector array to the ROIC. Instead, an entirely different process is used [21]. An HgCdTe layer is first grown on a lattice-matched CdZnTe substrate by liquid phase epitaxy (LPE) or molecular beam epitaxy (MBE). This is followed by the grown of a CdTe passivation layer on the HgCdTe to reduce surface leakage current. A layer of insulating epoxy is then flowed onto the surface of the ROIC. The detector layers are then placed face down with the CdTe passivation in contact with the epoxy and bonded together. After that, the CdZnTe

substrate is removed by a lapping and polishing process, leaving only the active HgCdTe and CdTe passivation layers.

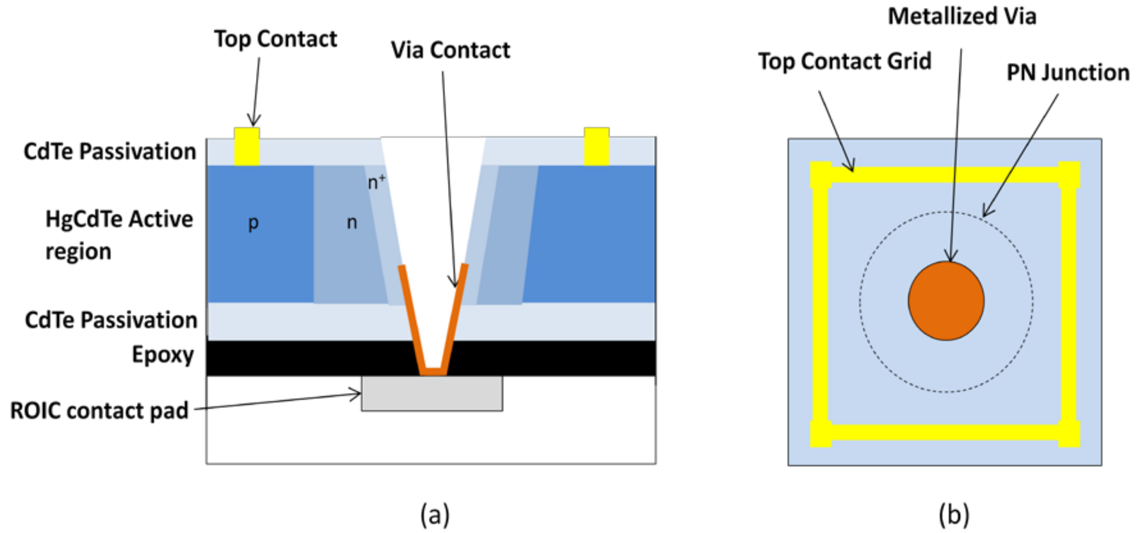

Figure 1.8: Schematic of frontside illuminated diode hybridized to an ROIC by via contact metallization: (a) cross-sectional view and (b) top view.

While HgCdTe is a fragile material, fracturing with low tens of MPa of stress applied versus 5000 – 9000 MPa for Si, the epoxy bond to the ROIC provides mechanical stability to the structure [22, 23]. Additionally, the contiguous epoxy layer binds HgCdTe to the Si ROIC so that it conforms under thermal cycling. After lapping and polishing a second CdTe passivation layer is deposited on the now exposed HgCdTe layer. Next, a milling process is performed, as defined by a photolithography step. This milling process serves two purposes. First, it forms a via that runs through the entire detector structure down to the contact metallization pads of the ROIC. Also, the milling process can type convert the p-type HgCdTe into n-type in a controlled manner. The result is an in-plane pn-junction with a semi-conical shape allowing for photodetection. Finally, contact metallization is made to both the p-type and n-type HgCdTe, as defined by

photolithography. The electrical contacts made to the p-type HgCdTe are made on the top surface of the device after etching of the passivation layer. A metal grid is formed to tie each of these individual contacts together. The electrical contact to the n-type HgCdTe connect each pixel to the ROIC contact pad on the inside of the via, allowing for imaging. Modern contacts are formed by physical vapor deposition (PVD) techniques. Good contact requires the metallization to bridge the epoxy gap between the active HgCdTe and the ROIC.

In continued scaling down of pixels, a contact metallization issue has arisen. Figure 1.9 illustrates the problem. In order to maximize the performance of the FPA, two conditions must be met with regard to absorption of incident radiation. First, a large fill factor is required. This is accomplished by keeping the diameter of the via well below the pitch of the pixel. Second, the active HgCdTe layer must be thick enough to absorb most of the incident radiation. Typically, this requires thicknesses that are on par with the cutoff wavelength of the device; therefore, a reduction of pixel pitch requires the aspect ratio of the vias to increase. The problem arises when depositing the via contact metallization layer. PVD techniques, such as electron beam evaporation, require a line-of-sight to deposit a thin film. For larger diameter vias with a lower aspect ratio, good electrical contact on the inside of the via can be made since shadowing from the via edge is not an issue, as shown in Figure 1.9a. However, at reduced pitched, the narrow high-aspect ratio via can shadow the growth of the contact metallization layer. This end product is an open diode due to the fact that the ROIC contact pad and HgCdTe layers are not electrically connected, shown in Figure 1.9b.

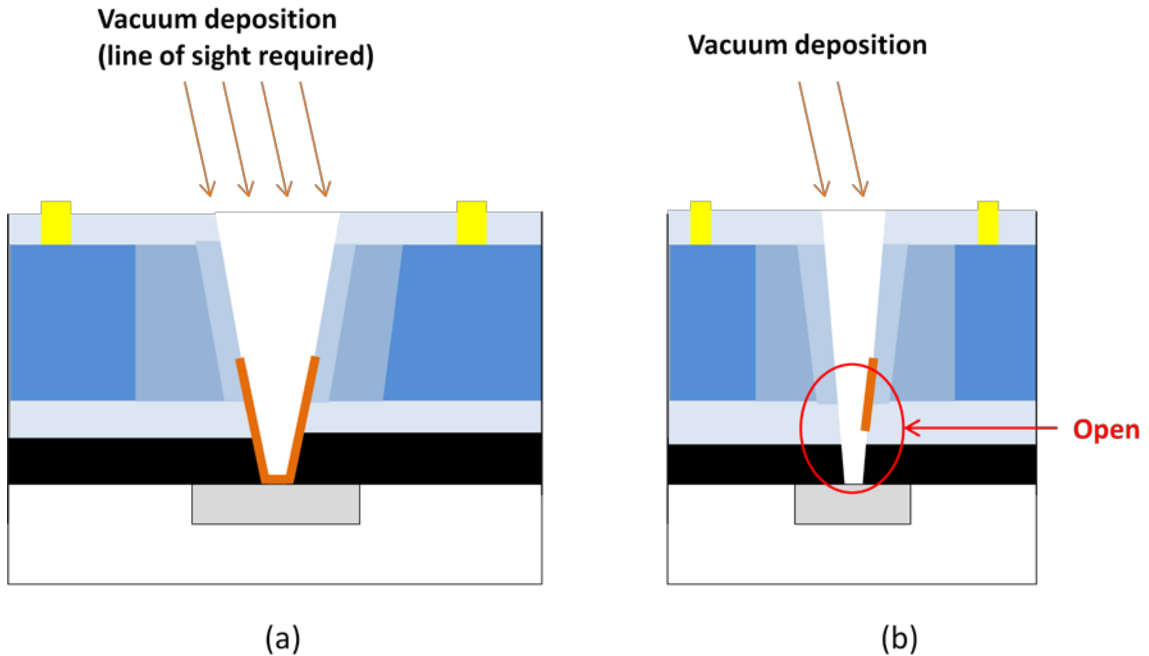

Figure 1.9: Schematic of via contact metallization by evaporation: (a) current pixel pitches resulting in good electrical contact and (b) reduced pitches resulting in open devices.

1.4 Introduction to the Proposed Solutions

A brief discussion of the overall processes developed to solve the statement of the problem is provided for each type of detector array.

1.4.1 In Bump Hybridization Solution

The proposed alternative for In bump fabrication that avoids a thick resist liftoff step is shown in Figure 1.10. The idea behind this process is to fabricate a template wafer upon which In bumps are electroplated. Assuming the template is designed correctly, the bumps could then be transferred from the template wafer to the ROIC by an additional hybridization step. After this step, the ROIC could then be hybridized to the detector.

This process has some similarity to the IBM controlled collapse chip connection new process (C4NP), which has been used to realize Pb-free solder bumps in Si electronics down to a 50 micron pitch in a production environment [24,25]. For the C4NP process, cavities are etched into a glass template wafer using a metal hardmask defined by photolithography.

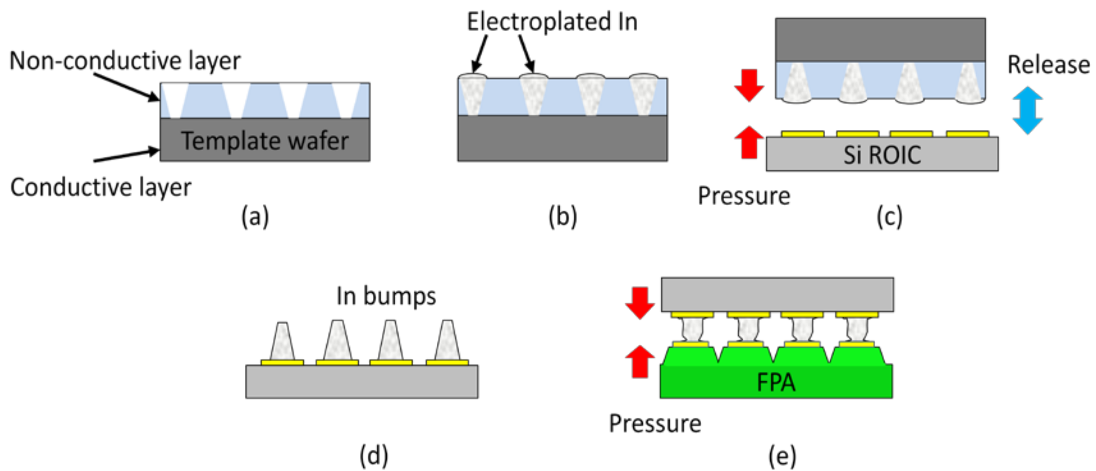

Figure 1.10: Schematic of novel In bump fabrication process: (a) The template wafer, (b) the template wafer after In electroplating, (c) transfer process of In bumps from template wafer to ROIC, (d) transferred bumps on ROIC, and (e) hybridization of FPA to ROIC.

Solder is then precisely flowed into the cavities using a solder injection head by heating its reservoir above the melting point of the solder. After filling each of the cavities, the glass template wafer and chip requiring solder bumps are aligned and clamped together. The wafers are then heated past the melting point of the solder, when the bumps adhere to the chip. After cooling, the two wafers are separated, leaving solder bumps on the chip. Finally, the bumps are reflowed again on the chip to ensure a consistent shape. At first glance, it appears that directly porting the C4NP process to realize In bumps for FPA hybridization would be straightforward. After all, In solder is commercially available [26]. There are several problems with attempting to do this, however. First, In has

adheres strongly to many materials, including glass, metals, and metal oxides [27]. Because of this, the transfer step would be highly unpredictable where some In would likely remain stuck to the glass template wafer. Additionally, the In bumps for FPAs are significantly smaller and more densely spaced than for solder bumps on ball-grid arrays (BGAs). Because of this smaller spacing, the In bumps cannot be spherically shaped as they will short together upon hybridization. Instead, columnar or pyramidal bump shapes are desirable. The current C4NP process produces spherically shaped bumps that would not work well for FPA technology.

For the proposed In bump fabrication process, proper design of the template wafer is critical to the success of the project. Figure 1.10a shows the template wafer prior to electroplating. The wafer consists of a conductive layer core with a patterned non-conductive layer on it. The conductive layer acts as the electroplating base; therefore, In plating initiates anywhere the layer is exposed. The purpose of the patterned nonconductive layer is to shape the deposition of In. Figure 1.10b shows the template wafer after electroplating, where the wafer itself acts as the working electrode for the process. Figure 1.10c depicts the transfer process of bumps from the template wafer to the ROIC. This would be performed by placing the two wafers on a flip-chip bonder, or hybridizer, aligning and pressing them together, and finally releasing them. If done correctly, the In bumps would end up on the ROIC, as shown in Figure 1.10d. In order for this transfer to work properly, several things must be considered. First, the thickness of the plated In must be just above the top surface of the non-conductive layer. Too little deposition and the In will never touch the ROIC for transfer during the press and release step. Too much deposition and adjacent bumps will be smashed together during the press

and release step, resulting in shorting of pixels together. Second, the friction between the nonconductive layer and the In must be kept to a minimum. If the amount of friction at this interface is too high, proper transfer of the bumps will not occur because the In will not release from the nonconductive layer. As discussed above, In adheres well to a variety of materials, so this layer must be carefully chosen. Finally, the sidewall profile of the nonconductive layer must be positive. Because pure In is a ductile material, it will break at the smallest cross-section when being pulled [28]. Thus, having positively sloped sidewalls ensures the smallest In cross-section is at the conductive layer/In interface and not in the middle of the bump. Last, after the transfer of In to the ROIC has occurred, hybridization of the ROIC to the detector array takes place, as shown in Figure 1.10e.

The proposed process has several advantages over the standard In bump fabrication process. In addition to having no thick resist liftoff step, the intention is that the template wafer will be reusable. This reusability is economical and lowers run-to-run variations of the bumps. Another benefit of this process is that no fabrication steps are needed on the detector array or ROIC, outside of the transfer and hybridization steps. This is especially important for the detector array. As discussed above, both CdZnTe and HgCdTe are fragile, so limiting processing steps is desirable. Additionally, electroplating is a more cost-effective means to deposit a material when compared to evaporation due to the amount of material deposited and wasted on the walls of an evaporator's vacuum chamber. Last, the amount of fabrication required to realize the template wafer is relatively small, with no alignment steps needed to form features. One of the main drawbacks of the proposed process is that an additional hybridization step is needed to transfer bumps to the ROIC.

Before developing the In bump fabrication process, several other approaches were considered. Electroplating of In directly onto the detector array or ROIC appears to be a more straightforward approach, however, this process has its own complications. Figure 1.11 illustrates the process steps involved [18]. After completion of the detector array, a lithography step is performed followed by deposition and liftoff of a non-wetting metal layer. This is followed by another lithography, deposition, and liftoff step to form the under bump metallization (UBM) layer.

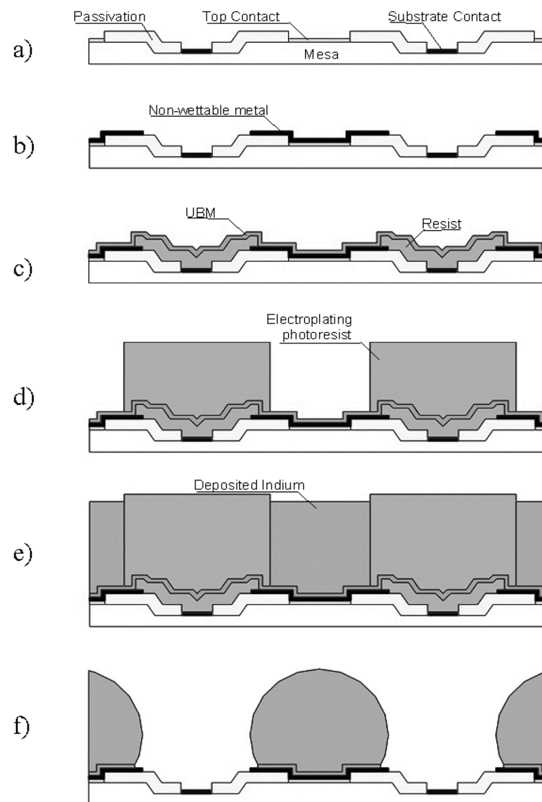

Figure 1.11: Schematic of process to fabricate electroplated In bumps. Reprinted from P. Merken, et. Al. IEEE Transactions on Advanced Packaging [18].

This is the seed layer upon which In is electroplated. Another lithography step is performed. A thick photoresist layer is used to define the shape of the electroplated In.

The photoresist is then stripped away, followed by etching away of any of the exposed UBM. In the end, this process requires three alignment steps for photolithography. Also, etching away the UBM is not straightforward at reduced pitches. Wet etching becomes unfeasible at smaller pitches due to over-etching of the layer laterally. Plasma processing is feasible, however the right chemistry and conditions must be used to ensure that the In bumps themselves are not being significantly etched away while stripping the UBM.

In addition to electroplating, another process was considered which involved using photoresist or definable polyimide as the nonconductive layer of the template wafer. For this process, the pattern definition would be straightforward, involving only a single lithography step with no additional processing required. Once again, the high adhesion of In makes this process unfeasible. Because In adheres well to photoresist, transferring the bumps from such a template wafer to the ROIC would be impossible. This process was attempted but did not succeed.

1.4.2 Via Metallization Solution

Rather than using currently employed PVD techniques for via metallization, several plating processes will be developed, including both electroplated and electroless metallization. For electroplating, the sample is immersed in an electrolytic solution and connected to a power supply as the cathode. The electrolytic solution contains ions of the metal to be plated. A metal anode is also immersed in the solution. Depending on plating chemistry, several anode options are available. For some plating baths, including electroplated Ni [29] and In plated from an indium sulfamate solution [30], the anode is composed of the pure metal to be plated. In this case, the anode replenishes the

electrolytic solution with metal ions. Replenishment only occurs if the electrolytic solution is capable of corroding the anode. For plating baths where this is not the case, such as for Au plating in alkaline cyanide baths [31] or In plated from a cyanide based solution, a different anode material is chosen. In this case, more inert metals are selected so that metals ions from the anode do not dissolve into the electrolytic solution. Depending on the specific application, stainless steel [32] or noble metals such as Pt coated Ti are used [33]. This type of bath requires periodic addition of metal ions to the bath or it will run out, resulting in an inability to plate further. Once properly setup, the power supply is turned on. Metal ions from the electrolytic solution are reduced onto the cathodic sample, forming a plated thin film. For plating to occur, a conductive surface on the sample must be present as no deposition will occur on nonconductive surfaces. Also, each region of the sample must be connected to the power supply because electrically isolated areas will not plate.

As the name suggests, electroless plating does not use an electrical current to drive reduction of metal ions. Instead, the process is autocatalytic. Like electroplating, this process starts with metal ions dissolved in an electrolytic solution. A reducing agent is then added which reacts with the metal ions causing them to deposit the metal. Typically, the bath is in equilibrium at room temperature, with additional heat being necessary to drive the reaction. Depending on the specific process, electroless plating can plate on both conductors and insulators. A variety of metals can be deposited by electroless plating, including Au [34], Cu [35] and Ni [36] to name a few.

Metal plating of macroscale parts is common in many industries, such processes are also used at a microscale in integrated circuits (ICs). Electroplating of relatively large

solder bumps for flip-chip applications has been performed using a variety of metals including Cu, Au, Ni, Sn, and Pb [37-39]. Compared to the scale of the vias metallization to be developed in this thesis, these features are large and do not provide any indication of the feasibility of plating such structures. However, there are several processes that do provide feasibility of the process. The damascene process for Cu interconnects of Si ICs, developed by IBM in the late 1990s [40] involves plating into dielectric trenches to form interconnects between components. By the early 2000s, this process was capable of filling 130 nm wide trenches with aspect ratios of up to 10:1 [41]. Another application of Cu plating is in the 3-dimensional integration of Si chips. This type of integration requires vertical interconnection between chips which is typically done by creating a through silicon via (TSV) by an etching process, followed by filling of the via with a conductor, providing an electrical path between a chip and the chip directly below it. TSVs with plated Cu plugs have been demonstrated for this purpose for vias on the same scale as those required in small-pitch detector arrays [42].

While plating of via contact metallization for detector arrays appears to be feasible, several factors complicate the issue. Determining the proper metal to plate is critical to the success of the process. Metals with high diffusivity in HgCdTe cannot be used due to potential doping of the material. The same can be said of any large amount of impurities that might be plated out in the contact metallization. In addition, the fragility of HgCdTe could present a problem for certain metals. If the plated contact metallization stresses the HgCdTe too much, dislocation may form in the semiconductor, resulting in reduced device performance. Finally, the plating solutions must be chosen so that they do not corrode the CdTe passivation, the HgCdTe active layer, or the ROIC contact pad.

Because of these issues, gaining a fundamental understanding of the plated metal and its interaction with HgCdTe will be a major thrust in developing the process.

Developing both an electroless and electroplating process is potentially useful due to the specific strengths and weaknesses of each technique. Electroplating allows for precise control of plating rate by adjusting the applied current of the power supply. Furthermore, control of the morphology and consistency of the deposition can be achieved by pulsed or reverse plating [43]. On the negative side, the lateral thickness tends to vary due to edge effects associated with the electric field applied between the anode and cathode similar to those seen with a parallel plate capacitor. Additionally, as discussed above, an electrically contiguous conductive seed layer is required to for plating across an entire detector array. Deposition of such a seed layer with the via detector array would not be possible as etching away of this layer to obtain isolation of diodes could not take place. Instead, the ROIC bonded to the detector array has the capability to tie each of the lines together to apply a bias, electrically connecting each diode of the array and allowing for electroplating. For electroless plating, there is no need to bias the ROIC as plating will be initiated by the addition of heat to the bath. Also, because no electrical current is applied, there should be no edge effects associated with the process. On the negative side, good temperature control will be necessary as this is key to obtaining a precise electroless process. Because this is harder to control than applied current, it can be predicted that the electroless process will have higher variability.

Chapter 2

Experimental Methods

2.1 In Bump Process Design

An outline of the novel process to hybridize In bump with a template transfer technique was given previously in Section 1.4.1. This section will discuss major design elements and processes of the technique, along with providing justification for their use.

2.1.1 Template Wafer Outline

A generalized process flow to fabricate the template wafer upon which In will be electroplated is shown in Figure 2.1. The process begins with a substrate, shown in Figure 2.1a, which acts as the mechanical backbone of the template wafer. A conductive seed layer is then blanket deposited on the substrate, shown in Figure 2.1b, which acts as the electroplating base of the wafer and will be physically connected to a power supply as the cathode in the electroplating setup. A nonconductive layer is then applied to the seed layer, as shown in Figure 2.1c. The low conductivity of this layer inhibits electroplating, thus no In growth will occur where it is present. Finally, the nonconductive layer is patterned, shown in Figure 2.1d. The pattern will define the shape of the In bumps. After finishing these steps, the template wafer is complete and ready for In electroplating.

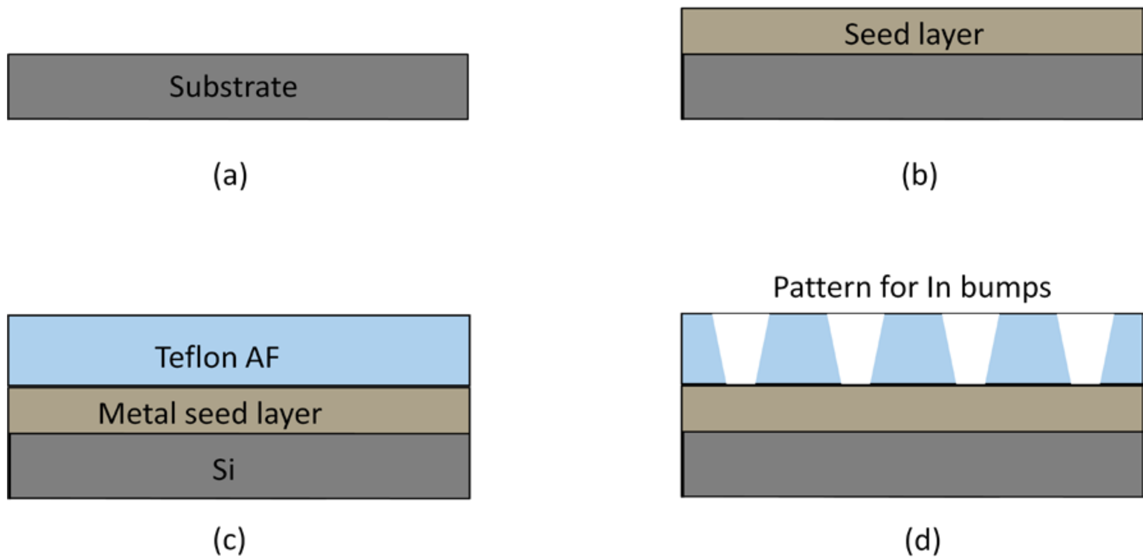

Figure 2.1: General fabrication of the template wafer: (a) the substrate, (b) application of a conductive seed layer, (c) application of a nonconductive layer and (d) patterning of the nonconductive layer.

2.1.2 Template Substrate

Several factors were considered when choosing a proper substrate material. The thickness variation across the sample needs to be limited for the process to work. Large lateral variations would lead to inconsistencies in the transfer process as consistent contact between the template wafer and ROIC or detector array is critical. Additionally, the substrate dimensions and materials must be compatible with microelectronics processing equipment. In particular, large thicknesses may present a problem. Because the substrate provides the mechanical stability of the template wafer, a relatively robust material is required. Based on these requirements, Si was chosen as the substrate material. In additional to its compatibility with processing equipment and favorable mechanical properties, samples with a submicron total thickness variation (TTV) are

readily available. TTVs as low as 40 nm have been reported over 300 mm Si wafers [44]. Other substrate materials such as bulk metal wafers were considered. While such materials could act as both the substrate and seed layer, their dimensions, weight, and thickness consistency were unfavorable for this application.

2.1.3 Template Seed Layer

The seed layer plays three critical roles in the construction of the template wafer and proper choice of material is key to the success of the process. First, this layer acts as the base for the In electroplating process. A highly conductive layer that spreads current evenly across the wafer for consistent lateral plating rates is necessary. While electroplating to high mobility semiconductors such as LWIR HgCdTe is possible [45], the choice of seed layer will be limited to metals. The surface of this layer can also affect the ability to plate features. Reactive metals that quickly form oxides on their surface can be difficult to plate to [46] because an insulating barrier is formed between the plating solution and metal, which inhibits the plating process. Complicated cleaning, pickling, and etching processes may then be required to obtain high quality plated features. Second, the seed layer is the interface between the substrate and nonconductive layers and thus acts as the glue to bind the entire template wafer. Because of this, good adhesion between this layer and the other two is required. High residual stress on the seed layer after its growth could result in catastrophic peeling of the layer from the substrate; and for this reason, such materials should be avoided. The third role the seed layer plays is to allow for the release of In bumps during the transfer process to the ROIC or detector arrays; therefore, low adhesion between this layer and the electroplated In is desired. Materials that readily interdiffuse with In, such as Cu [47] or Au [48] are undesirable.

Such materials form intermetallics that would reduce the predictability of In breaking from the surface upon transfer.

Based on these requirements, Ni was the first material chosen as the seed layer. Ni has a relatively low resistivity or $7x10^{-8}$ Ωm [49]. In also diffuses slowly in Ni and therefore will not form any intermetallics. This diffusion is so slow that Ni films have been used as an In diffusion barrier [50]. In addition to Ni, several other metals were investigated for their suitability as a seed layer, including Ti, Al, and Cr.

2.1.4 Template Nonconductive layer

For successful transfer of In bumps from the template wafer, the bumps must readily pull away from the nonconductive layer without breaking or distorting. The interface between the In and nonconductive layer represents the majority of surface area of the bump; therefore, limiting the adhesion between the two materials is critical. As discussed in Section 1.4.1, a In adheres strongly to a variety of metals, metal oxides, and glass, however, its adhesion to polytetrafluoroethylene (PTFE) was found to be negligible [28]. PTFE is a synthetic fluoropolymer that has found a variety of applications where low friction surfaces are required. Teflon®, developed by Dupont™. is an example of a commercially produced PTFE. For the template wafer application, a 5 to 10 μm thick, blanket layer of PTFE needs to be applied to the seed layer. Several PVD methods, including thermal evaporation [51], RF sputtering [52], and pulsed laser deposition (PLD) [53] have all been used to deposit the material, however, these methods are not ideal for the considerable thicknesses required for this application. Instead, an amorphous fluoropolymer with properties similar to PTFE will be used. Teflon® AF, a product

commercially available from Dupont [54], consists of an amorphous fluorocarbon in perfluorocarbon solution. A baking process is used to drive off the perfoluorocarbon, leaving a solid film of amorphous fluorocarbon on the sample. Depending on concentration, films up to tens of μm can be spun onto a sample. After baking, the glass transition point, T_g is 160 °C and it can be molded at temperatures above 240 °C. Based on Dupont's internal data, this product adheres well to Al, Ti, and electrolytic Cu [55]. In addition to its favorable mechanical properties, this amorphous fluoropolymer is also highly stable and resistant to chemical attack. This property is important as both the surface preparation of the seed layer and the electroplating bath are acidic, as well as other potential processes to be attempted.

2.1.5 Template Pattern Definition

As discussed in Section 1.4.1, features with a positively sloped sidewall are desired in the amorphous fluoropolymer to induce necking of In at the seed layer interface during the transfer step. While there has been research in a variety of microelectronics applications using amorphous fluoropolymer including: gate insulators for thin film transistors (TFTs) [56], cladding for liquid core waveguides [57], thin film multilayer coatings with improved optical properties [58], and as a non-sticking layer to aid release between two wafers in an imprint lithography process [59], it is still an exotic material in the field. As such, there is a limited amount of research focusing on pattern definition of this material. Several sources have reported etching of PTFE or other amorphous fluoropolymers using an inductively coupled plasma (ICP) etching system [60,61] using Ar/O_2 gas mixtures. In both cases a metal hardmask was used to define features in the fluoropolymer as photoresist does not stick to the material. Based on these

results, a process was developed based around plasma etching of the amorphous fluoropolymer layer, shown in Figure 2.2. After application and baking of the Teflon AF, shown in Figure 2.2a, a thin Ti hardmask layer is evaporated onto the sample, shown in Figure 2.2b. Ti was chosen based on its relatively strong adhesion to the fluoropolymer (Ref 12). A photolithography step is the performed to form a pattern on the Ti hardmask, shown in Figure 2.2c. While photoresist will not adhere to the fluoropolymer, its adhesion to Ti is sufficient. After the lithography step, a wet or plasma etch can be performed to define the Ti hardmask, shown in Figure 2.2d. Due to the potential for over-etching, a plasma process is preferable over a wet etch. The amorphous fluoropolymer is then etched in an ICP etching system to define features with positively sloped sidewalls, as shown in Figure 2.2e. Finally, the hardmasking layer is stripped away using a wet etching process, leaving the completed template wafer, shown in Figure 2.2f.

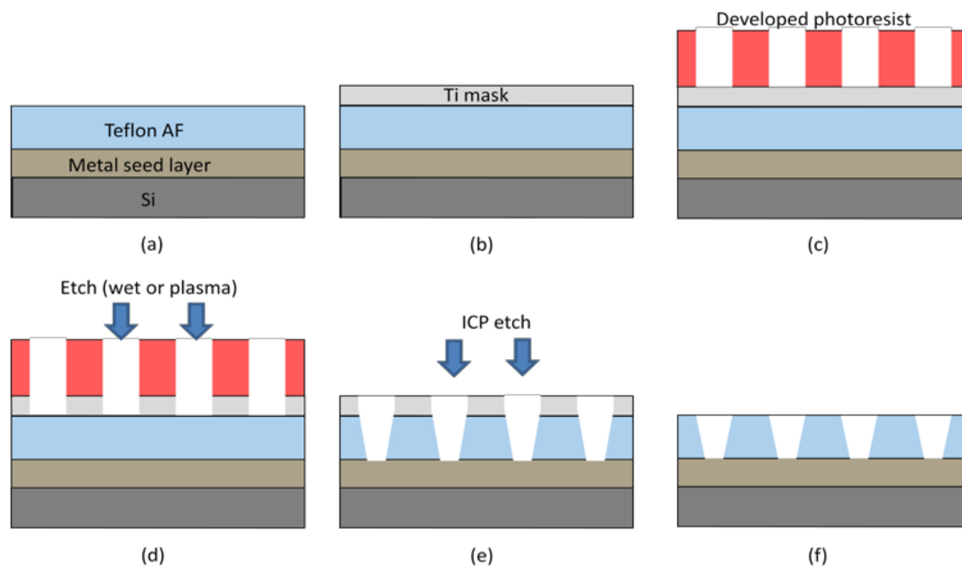

Figure 2.2: Pattern definition of a template wafer through photolithography and etching: (a) unpatterned template wafer, (b) deposition of a thin hardmask, (c) photolithography step, (d) etching of the hardmask, (e) etching of the amorphous fluoropolymer and (f) chemical stripping of the hardmask.

In addition to the more standard lithography and etch process to pattern the amorphous fluoropolymer, another process was developed. This process was based on the nanoimprint lithography technique (NIL) developed by Chou et al. with results published in 1995 [62], which yielded 25 nm trenches in polymethylmethacrylate (PMMA). While a variety of improvements to the technique have been made, allowing for claims of industry level validation at 22 nm [63], understanding the original process allowed for development of an amorphous fluoropolymer imprinting technique for the applications of this thesis. A schematic of the process is shown in Figure 2.3. The process requires two separate wafers, a stamp wafer and a substrate. The stamp wafer consists of SiO_2 coated Si which is patterned by an electron beam lithography step. Features are then etched into the SiO_2 with a reactive ion etch (RIE) step. The substrate is spin-coated with a thin layer of PMMA, on the order of tens of nm. PMMA was primarily chosen specifically due to its low adhesion to SiO_2. After preparation of both wafers, each is heated past the 105 °C T_g of PMMA and pressed to one another. This results in thermoplastic deformation of the PMMA layer. The two wafers are cooled while under compression and then released from each other. A negative of the pattern in the stamp wafer is thus embossed in the PMMA layer. After the NIL step, the PMMA coated substrate can be processed further. The stamp wafer can then be reused to imprint other substrates. Additionally, the process extends to other materials that can be thermoplastically deformed. One key is that the stamp and substrate sufficiently release from one another or the process will not work.

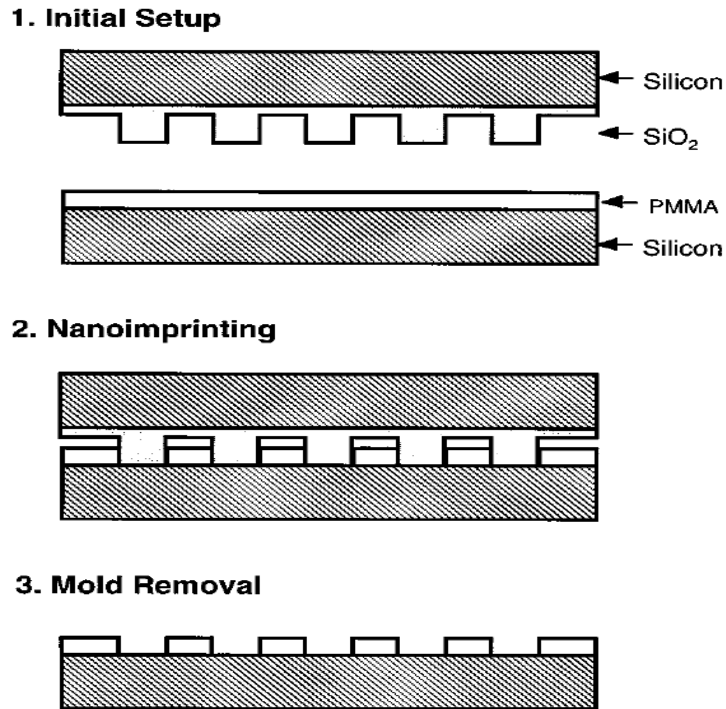

Figure 2.3: Schematic of the NIL technique. Reprinted from S.Y. Chou, et Al. Applied Physics Letters [63].

The process developed for imprinting amorphous fluoropolymer is somewhat different than the NIL process just described. The scale of the process is substantially larger, requiring embossing of polymer films that are several μm thick rather than tens of nm. Additionally, the patterned amorphous fluoropolymer is not a masking feature for further processing of the template wafer. Instead it is a fixture of the wafer that must remain intact throughout the In electroplating step; therefore, attention must be paid to the quality and morphology of features after the imprinting step to ensure that they are in line with process requirements. A schematic of this process is shown in Figure 2.4. Like the NIL process, the imprinting process begins with two wafers, a Si stamp and the template wafer. The Si stamp is patterned through a standard photolithography and etch

step. Positively sloped features in the stamp are required so that the embossed features in the amorphous fluoropolymer have the same morphology. Given the relatively large size of features required for this application, no exotic lithography techniques are required. The template wafer has been coated with the seed layer and amorphous fluoropolymer. The two samples are heated past the 160 °C T_g of the amorphous fluoropolymer and pressed together, cooled, and released from one another. The last step involves the removal of any residual amorphous fluoropolymer from the bottom of the features. Such residual layers have been reported [64,65] and are expected to occur for this process. While this layer appears to be detrimental to the process, it actually acts as a cushioning buffer between the stamp and substrate. This reduces damage that would occur by the two wafers being in direct contact with one another. The benefit of having such a residual layer also allows for a reduction in the pressure required to perform the imprinting process as well. For NIL techniques, this residual layer can be removed by a fast dip in developer or an RIE step, depending on the specific polymer that was imprinted. For the amorphous fluoropolymer, an RIE step will be required to remove the residual layer as there is no way to remove the layer with a wet process. The removal of this residual layer is a critical step in the process to produce a template wafer capable of electroplating In bumps. Just like an oxide on the surface of the seed layer, any remaining insulating amorphous fluoropolymer will inhibit the initiation of In growth. After successful removal of the residual layer, fabrication of the template wafer is complete.

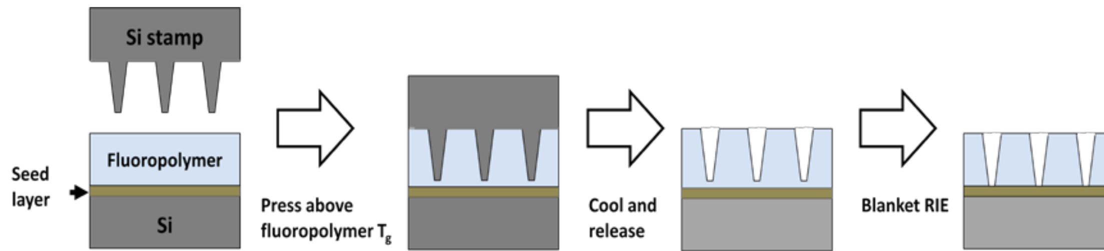

Figure 2.4: Schematic of the imprinting process used to define features in the template wafer.

2.1.6 In Electroplating and Transfer Steps

Once the template wafer is fabricated, the transfer process involves electroplating In into the template wafer and then transferring the bumps to the ROIC or detector array to complete the process. There is little design required in each of these steps and each of these processes will be discussed in detail in the In Bump Process Flow section that follows.

2.2 In Bump Process Flow

This section includes a detailed description of processes and techniques used for the In bump transfer technique process along with theories of operation for any processing equipment used.

2.2.1 Metal Seed Layer Deposition

Metal seed layers of the template wafer, including Ni, Ti, Cr, and Al were all blanket deposited by electron beam evaporation onto a Si substrate. 380 ± 25 μm thick, 100 mm diameters Si wafers were used for the substrate material. Prior to loading the

substrates into the evaporator, cleaning and surface preparation steps were performed. Wafer cleaning consisted of an acetone, methanol, isopropyl alcohol, and de-ionized (DI) water rinse to remove particles from the surface of the wafer. A diluted HF dip was then performed to strip the native oxide from the SI surface, which improves the adhesion between the substrate and seed layer. The Si is dipped in 2% HF in DI water for 1 minute. This is followed by a 20 s rinse in DI, an N_2 blow drying step to remove any remaining water droplets, and immediate transfer and placement under vacuum of the wafer in the evaporator before a native oxide begins to grow again on the Si surface. Because pure Si is hydrophobic [66], removal of the oxide is confirmed by beading of water on the surface of the wafer that is easily removed when blow drying.

A Temescal BJD-1800 electron beam evaporator was used for the seed layer deposition. Vacuum pumping of the system is achieved through mechanical pump/cryo pump stages that can achieve an ultimate vacuum of roughly 3 x 10^{-8} Torr. A four-pocket turret that rotates to line up with the electron beam allows for deposition of four different metals without breaking vacuum. Additional information regarding this series of evaporators in available online [67]. Once in the chamber, the Si substrate was pumped on until a pressure below 2 x 10^{-6} Torr was achieved. Such pressures are necessary to obtain an evaporated metal for several reasons. A reduction in pressure reduces the temperature at which the metal will evaporate, requiring less electron beam current [68]. More importantly, the reduced pressure increases the mean free path of the evaporated metal, given by:

$$\lambda = \frac{kT}{\sqrt{2}\pi d^2 P} \qquad (2.1)$$

where λ is the mean free path, k is Boltzmann's constant, T is temperature, d is the source to sample distance in the evaporator, and P is pressure [69]. Mean free path is the average distance between collisions for a gas particle. For evaporation, the mean free path should be longer than the source to sample distance. By obtaining pressures in the low 10^{-6} range, this is accomplished.

Once the base pressure was achieved, the electron beam was turned on and powered by a Temescal Simba 2 power supply. Power to the electron beam was ramped up slowly, with a series of long soaks to ensure uniform heating of the evaporation source. If uniform heating is not achieved, spitting of the source material onto the sample can occur, resulting in large defects in the deposited film. Once the deposition power was reached, 15 RPM sample rotation is applied to improve film uniformity, and a shutter was opened to allow for deposition to begin. A crystal rate monitor was used to determine deposition rates and total deposition thickness. After reaching the desired thickness, the shutter is closed and power is ramped down. Finally, the sample can be removed once it cools. Table 2.1 includes a summary of deposition parameters for each seed metal.

Metal	Ti	Ni	Al	Cr
Rise 1 time (min)	3	2	3	2
Soak 1 %	10	14	12	9
Soak 1 time (min)	5	3	5	3
Rise 2 time (min)	1.5	1	1.5	1
Soak 2 %	13	19	19.7	12.4
Soak 2 time (min)	7	5	7	5
Deposition rate (Å/s)	4	4	4	4
Ramp down time (min)	3	3	3	3

Table 2.1: Process parameters for the deposition of metals by e-beam evaporation.

Ni seed layers ranging between 100 nm and 1000 nm were deposited by this technique, as confirmed with profilometry and cross-sectional scanning electron microscopy (SEM). After some preliminary testing for adhesion, it was determined that a 100 nm Ti sticking layer was necessary to prevent peeling of the Ni layer. The other seed metals tested did not require this sticking layer. Instead, 250 nm of each layer was deposited on a Si substrate.

2.2.2 Application of the Amorphous Fluorocarbon Layer

As previously discussed, an amorphous fluoropolymer was used as the nonconductive layer of the template wafer. The specific product used was called Dupont Teflon AF 1601S, and consisted of 18% amorphous fluoropolymer diluted in a perfluorocarbon solution. A perfluorocarbon called 3M™ Fluorinert™ FC-770 could also be used to further dilute the Teflon AF. The sample was placed on a Solitec 5110C spinner requiring manual liquid dispensation. After coating the template wafer with amorphous fluoropolymer, a baking procedure was required. First, samples were baked at

112 °C for 15 minutes on a hotplate with a proportional-integral-derivative (PID) temperature controller. The purpose of this low temperature bake is to drive off the perfluorocarbon solvent. FC 770 has a boiling point of 95°C [70]. The temperature was then ramped to 165 °C for 15 minutes, again ramped to 250 °C, and slowly ramped back down to room temperature with the sample remaining on the hotplate. The baking steps above the T_g of the amorphous fluorocarbon have been shown to improve the adhesion of the film to the material below [55]. Additionally, the high temperature bake helps to improve film uniformity as the fluorocarbon is allowed to flow to a minimum energy state at temperatures above T_g. The purpose of the slow ramping temperature is to avoid thermally shocking the sample.

2.2.3 Pattern Definition Using Standard Lithography and Plasma Etching

This process follows the flow of Figure 2.2. The first step in patterning the amorphous polymer layer of the template wafer was to deposit a thin Ti hardmask. This was accomplished using the same procedures used to deposit the metal seed layers by electron beam evaporation in section 2.2.1. No preparation of the fluorocarbon surface was performed although any particulates on the surface were removed with an N_2 blow dry. Thicknesses of the Ti film were 50 nm.

Once deposited, the hardmask allows for adhesion of photoresist and thus pattern definition with a photolithography step, shown in Figure 2.5. First, the sample, shown in Figure 2.5a, was placed on the Solitec 5510C spinner. AZ1529 photoresist was then manually dispensed on the sample directly from the bottle. AZ 1529 is a positive tone photoresist comprised of diazonaphthoquinone (DNQ) photoactive compound (PAC) in

solution with propylene glycol methyl ether acetate (PGMEA). Nominal post-spin thicknesses of 2.9 μm are achieved at speeds of 4000 rpm [71]. After a short spreading step, a spinning step evenly coated the Ti hardmask, shown in Figure 2.5a. A manual edge bead removal step was performed on the sample with polyester swabs and acetone.

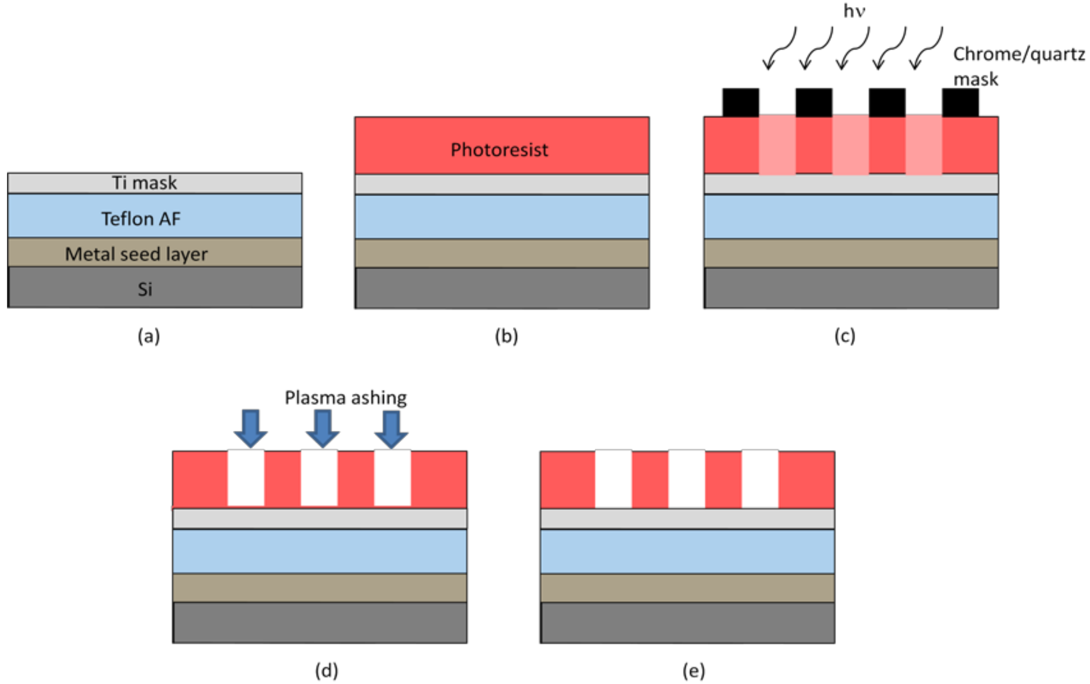

Figure 2.5: Patterning of the Ti hardmask for definition of features in the template wafer.

The sample was then soft-baked on a PID-controlled hotplate to drive off the PGMEA solvent and to harden the photoresist. After the soft-bake, the sample was placed on OAI mask aligner. This system allows for manual alignment of a 4" quartz mask with the sample. It is a contact aligner with a broadband ultraviolet (UV) bulb. A chrome/quartz mask having the required features was aligned with the sample. After proper alignment, the sample was exposed to the UV light. With positive tone photoresist, exposure to UV causes a breakdown of the PAC, resulting in solubility in photoresist developer; therefore, photoresist under transparent regions of the quartz mask become soluble, and

remains insoluble where the mask is opaque. The result of this step is shown in Figure 2.5c. After exposure of the photoresist, the sample was dipped in AZ 300 MIF, a tetramethylammonium hydroxide (TMAH) based developer was used for this purpose which dissolves regions of the photoresist broken down by UV and exposes the layer below [72]. After developing the sample, it was rinsed in DI water to remove any developer residue and dried with N_2.The lithography process concluded with another baking step to fully harden the photoresist. Table 2.2 gives the specific parameters used for this process. Final resist thicknesses were roughly 2.5 μm as measured by profilometry. While the photolithography process is straightforward and repeatable, very thin layers of photoresist may remain bound to the sample that didn't develop out, as shown in Figure 2.5d. Removal of these layers is typically performed by a plasma descumming step. A Nordson March PM-100 barrel asher with an O_2 line was used for this purpose. This system works by igniting a plasma between two electrodes, breaking the O_2 into ionized O free radicals. The highly reactive free radicals bond with the surface of the photoresist and volitalize it. A low power plasma allows for removal of remaining photoresist at the bottoms of features while negligibly etching the rest of the photoresist away. The specific parameters used for descumming the template wafer were as follows: O_2 plasma, 800 mTorr operating pressure, 30 W operating power, and a running time of 3 min. Figure 2.5e shows the resulting template wafer.

Process Step		Process Step	
Resist spread time	5 s	Exposure dose	73 mJ/cm^2
Resist spead speed	50 rpm	Develop time	30 s
Resist spin time	60 s	Rinse time	2 min
Resist spin speed	400 rpm	Hard-bake time	20 min
Soft-bake time	1 min	Hard-bake temp	100 °C
Soft-bake temp.	100 °C	Resist thickness	2.5 μm

Table 2.2: Process parameters for photolithography using AZ 1529 photoresist.

Etching of the Ti hardmask was performed by two separate techniques, a wet etch and plasma etch. Figure 2.6 shows how each type of etch progresses, in general. Most wet etch processes are isotropic and, therefore, tend to undercut the resist, as shown in Figure 2.6a. As the etch progresses, it eventually gets through the Ti layer, exposing the amorphous fluoropolymer; however, undercutting of the photoresist continues until the sample is pulled from the etchant and rinsed, resulting on over-etching of the features. While this is disadvantageous, wet etching is substantially simpler. Good process control is required to limit these deleterious effects. This includes good temperature control, as there is typically a strong correlation between temperature of the solution and etch rate. The progression of plasma etching is shown in Figure 2.6b, where it is assumed that ideal plasma conditions are used. In this case, the process is anisotropic, where nearly all the etching occurs in the vertical direction. For this type of etch, the amount of undercutting is minimized, producing features of the desired size. For wet etching of the Ti hard mask, a H_2O:HF:HNO_3 solution was used. Previous etch rates of 1100 nm/min for a 20:1:1 solution at 20 °C of this etchant were reported [73].

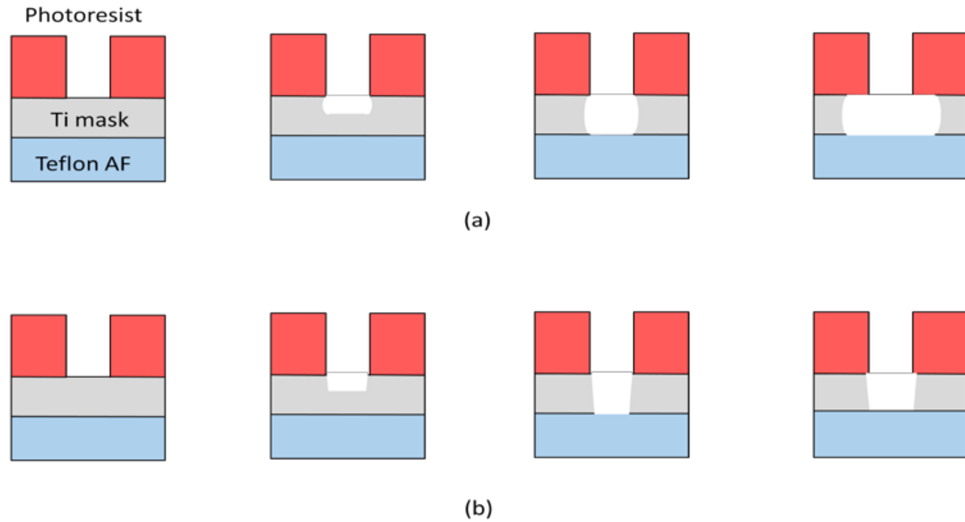

Figure 2.6: General progression of etching a layer by (a) wet and (b) plasma etching.

For plasma etching, a parallel plate RIE system was used. A schematic of a general RIE system is shown in Figure 2.7. The sample is placed on a platen that acts as the bottom electrode. The top electrode, is typically placed several cm away and parallel with the bottom electrode. The top electrode is grounded while radio frequency (RF) power is applied to the bottom electrode. Once the RF power is turned on, a plasma forms, consisting of electrons and various ions. The bottom electrode is capacitively coupled to the RF generator and develops a negative bias. The RF power causes both the electrons and ions to oscillate within the chamber. The ions oscillate slowly compared to the electrons due to their large mass. The attraction to the negatively charged bottom electrode causes them to move toward it, where they collide with the sample. Depending on specifics plasma chemistries, the incident ions etch the sample by sputtering it through physical momentum transfer or by volatilizing the sample surface through a chemical reaction. Typically, a combination of these phenomena occur during etching [74]. A variety of parameters can be controlled for RIE processes. Operating pressure can be

adjusted with higher pressure typically leading to more isotropic etching due to a decreased mean free path of particles. RF power can be adjusted, increasing or decreasing the amount of momentum particles strike the sample with. The process gases also play an important role in etch characteristics. For inert gases such as Ar, the etching is usually a physical process. On the other hand, the reactivity of O free radicals can produce an etch that is more chemical in nature. Tweaking of these parameters can influence etch rate, etched sidewall profile, etch morphology, and etch selectivity, amongst other things. While process optimization is more challenging than for wet etching, plasma etching allows for better control of the etch profile once optimized.

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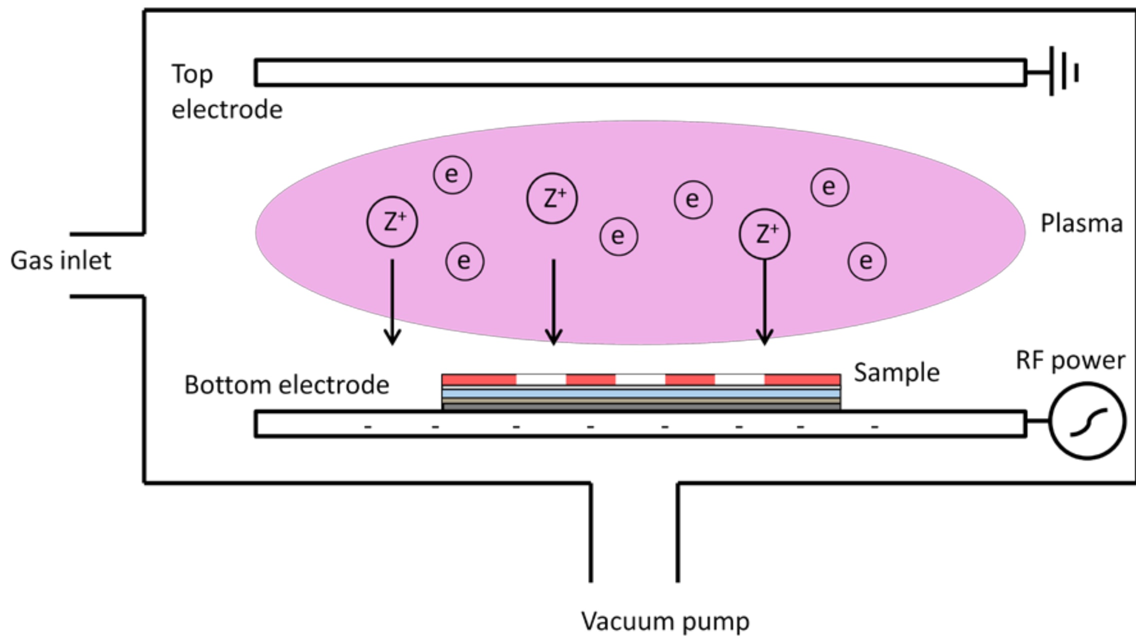


Figure 2.7: Simplified schematic of an RIE system.

Plasma etching of the Ti hardmask was performed in a Trion Phantom III RIE parallel plate system. Vacuum pumping is achieved through mechanical and turbomolecular pump stages. Input gasses are connected to a throttle valve, allowing for

independent control of gas flow and operating pressure. A CF_4 plasma was used, with etching of the Ti layer driven by the following chemical reaction:

$$Ti + 4F(g) \rightarrow TiF_4(g) \quad (2.2)$$

where F radical in the plasma bond to the Ti surface to form the volatile TiF_4 [75]. While the etch may be somewhat isotropic, the Ti hardmask layer is thin enough that the detrimental effects of such an etch will be negligible. The following parameters were used for this process: CF_4 flow was 40 sccm, operating pressure was 150 mT, and RF power was 80 W. Depending on the thickness of the Ti layer, etch time ran between 3 and 7 minutes.

Upon completion of the previous step, the photoresist was stripped in acetone followed by a methanol and isopropyl rinse. Afterwards, etching of the amorphous fluoropolymer was performed. As previously discussed, features with a positively sloped sidewall are desired for this process. Because of this requirement, isotropic wet etching cannot be used for this purpose. Additionally, the amorphous fluoropolymer is so inert that very few chemical etching products are available. Such etchants are highly caustic pastes used for large scale parts unsuitable for microelectronics applications [76]. Instead, plasma etching of the amorphous fluoropolymer was performed using an ICP etching system. The ICP process builds on the concept RIE with the addition of a coil around the chamber, powered by a second RF source, as shown in Figure 2.8. Application of RF power, typically at a frequency of 13.6 MHz, induces a magnetic field in the chamber. This results in a plasma with a substantially higher density of ions and radicals than with standard RIE. This increased density allows for faster etch rates, and it also allows for

processing at lower pressures than possible by RIE. For RIE systems, as pressure is reduced below the 10 mTorr range, too few collisions occur between particles to generate enough electrons for sustaining a plasma. By increasing plasma density, the number of collisions is increased allowing for operation at lower pressures. This fact is critical when developing anistropic etching processes. Improved plasma uniformity is typically improved over RIE processes as well [77]. In addition to these benefits, the ICP RF source adds another plasma parameter to adjust when optimizing a process. Several system configurations can be used depending on whether power is applied to the ICP and/or RF sources. Application of RF power in addition to ICP power provides increased bombardment of ions onto the sample.

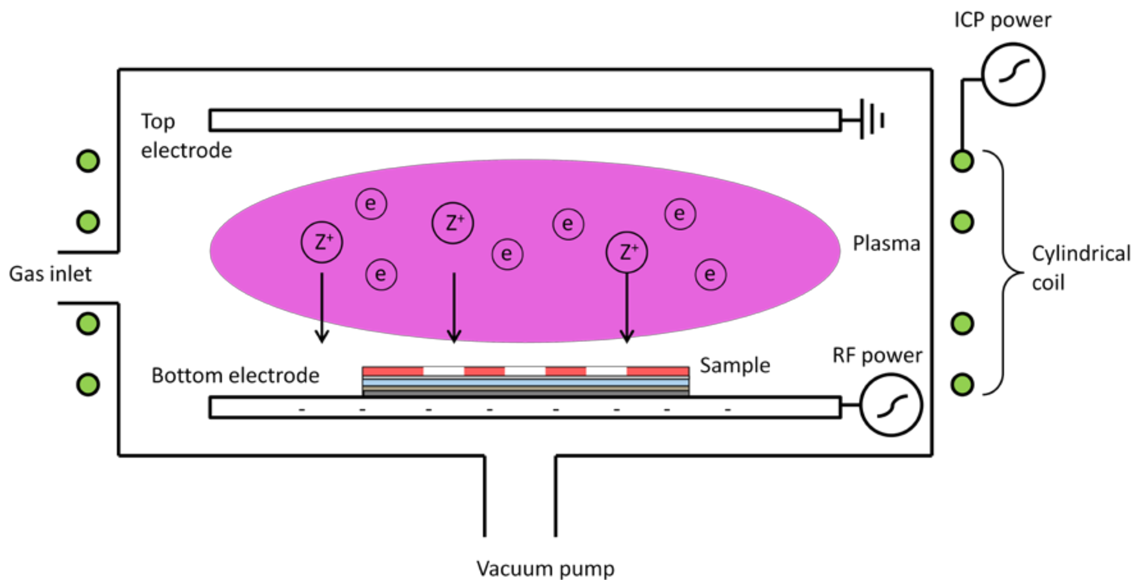


Figure 2.8: Simplified schematic of an ICP etching system.

ICP etching of the amorphous fluoropolymer was accomplished using an Ar/O_2 plasma in an Oxford Plasmalab 100 system which is a load-locked system with the main chamber vacuum attained by a turbomolecular pump. Substrate temperature can be

controlled and is achieved by flowing liquid nitrogen (LN) to the substrate holder. Throttle valves for the input gasses allow for independent control of gas flow and operating pressure. Prior to running experiments on samples, an O_2 plasma step with a dummy wafer was performed to clean the chamber.

Based on previous results, an Ar/O_2 plasma was used to etch the amorphous fluoropolymer [60, 61]. Ar-only etching, caused by sputtering, produced slow etch rates due to a high redeposition rate. The addition of small amounts of O_2 dramatically increased etch rates which was due to chemical reactions between the amorphous fluoropolymer and O ions induced by their impact. The oxygenated products are volatile and do not redeposit. A saturation in etch rate was seen at roughly 10% O_2. Vertical sidewalls were seen in both studies and theorized to be the result of a passivation mechanism. It was theorized that oxygen deficient CF_x molecules emitted from the bottom of features redeposit on the sidewalls and form a protective passivation layer. Because positive sloped sidewalls rather than vertical ones were desired for the template wafer, etching experiments focused on adjusting the O_2 ratio in the Ar/O_2 plasma. By raising the amount of O_2, the idea was to reduce the amount of sidewall redeposition, resulting in a slight horizontal etching component due to a weakened passivation layer. A variety of plasma operating pressures were also attempted to adjust the level of isotropy of the etch, as well as ICP and RF power values.

The last step of this pattern definition process was to remove the Ti hardmask, which was accomplished by blanket wet etching the layer away in the $H_2O:HF:HNO_3$ solution described above. Because the layer is being completely stripped, and the

amorphous fluoropolymer does not react to the etchant, there are no concerns of over etching. After this step, the template wafer was complete.

2.2.4 Pattern Definition Using Imprint Lithography

This process follows the flow of Figure 2.4; however, prior to imprinting the template wafer, the Si stamp must be fabricated. A schematic of this process is shown in Figure 2.9. The process starts with a Si substrate, shown in Figure 2.9a. After a photolithography step, shown in Figure 2.9b, the substrate is then etched, leaving positively sloped pillars shown in Figure 2.9c. Finally, the photoresist is removed, leaving the completed Si stamp shown in Figure 2.9d. While much of this process is straightforward, etching of the pillars is not. Two approaches were attempted to achieve such pillars.

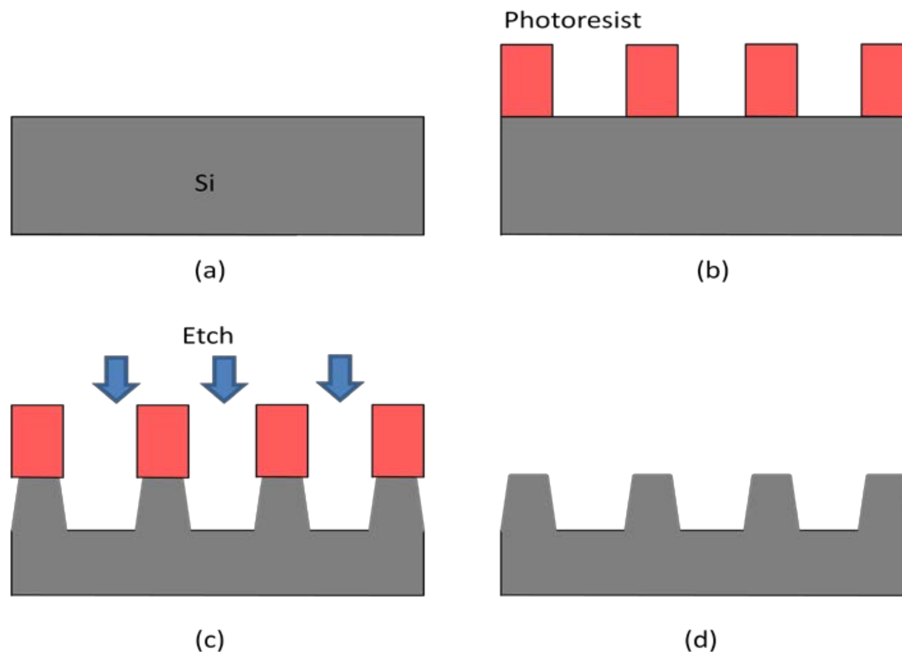


Figure 2.9: Fabrication of the Si stamp: (a) Si substrate, (b) photolithography step, (c) etching of Si pillars and (d) photoresist strip.

The first process made use of a two step etch, where the purpose of the first etch was to form pillars in the Si substrate and the second was to shape the pillars so that they had positive sidewall angles. Deep reactive ion etching (DRIE) via the Bosch Process was used as the first etching step [78]. The steps of this process are shown in Figure 2.10 and makes use of periodic SF_6 and C_4F_8 plasma steps. First, features are defined on a Si substrate, shown in Figure 2.10a. A short SF_6 plasma step is then performed. SF_6 dissociates and isotropically etches Si chemically in the following manner [79]:

$$Si + 4F(g) \rightarrow SiF_4(g) \quad (2.3)$$

shown in Figure 2.10b. After several seconds of etching, the plasma is switched to a C_4F_8 composition. This material is inert with and deposits on the Si sample, forming a passivation layer shown in Figure 2.10c. The process is then iterated. The next SF_6 step sputters the passivation at the bottoms of features without removing sidewall passivation. This allows for etching of vertical structures with high aspect ratios, as shown in Figure 2.10d. Systems are currently available that allow for etching of features with aspect ratios as high as 70:1 [80]. Additionally, etch selectivities over photoresist are 50:1 or better, allowing for patterning with thin photoresist.

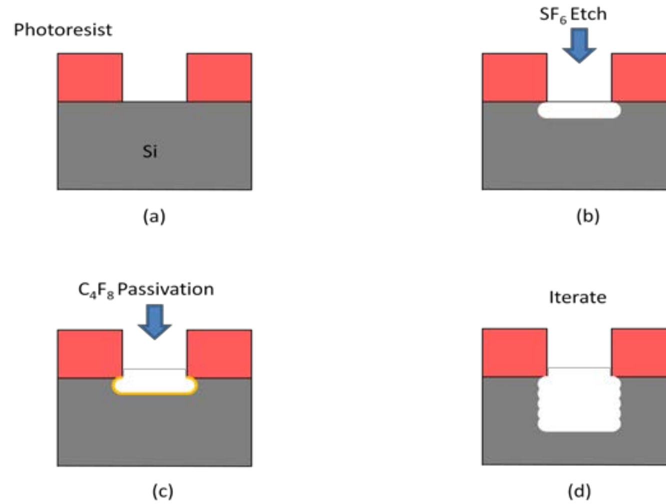


Figure 2.10: Steps of the Bosch process: (a) patterned Si layer, (b) SF_6 etch step, C_4F_8 passivation step and (d) iteration of these steps to realize high aspect ratio features.

Shaping of vertical sidewall features was accomplished by a wet etching step. Several solutions with varying ratios of HF, HNO_3, and H_2O were used for this purpose. This solution is similar to the HF-HNO_3-$HC_2H_3O_2$ (HNA) etch, where both are typically used to isotropically etch Si; however, obtaining some directionality is possible depending on the exact composition of the etchant [81]. Figure 2.11 shows the relationship between the composition of the etchant and the resulting geometry of etched features. This graph has three axes, where the left axis represents the percentage of 49.25% HF in the solution, decreasing towards the bottom left vertex. The right axis represents the percentage of 69.51% HNO_3 in the solution, decreasing towards the top vertex. The bottom axis represents the amount of H_2O added to the solution, decreasing towards the bottom right vertex. The etch is purely isotropic at low concentrations of added water at a ratio of HF:HNO_3 between 65:35 and 15:85. The reaction is diffusion limited in this regime resulting in features with rounded corners and edges due to the increased availability of reagent. The reaction exits this regime as the amount of H_2O

added to the solution is increased. As a result, the directionality of the etch increases. Additional details of the phenomenology can be found in Schwartz et Al. 1976 [81].

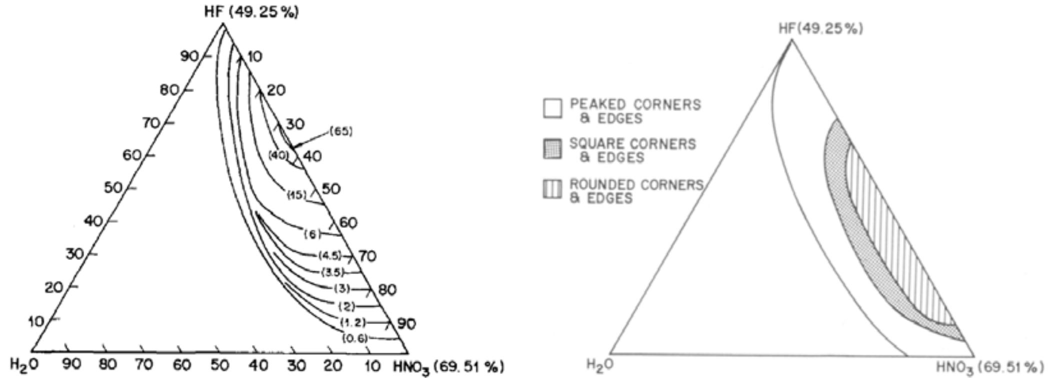


Figure 2.11: Etch rates and regimes for Si etched with various compositions of HF-HNO_3-H_2O. Reprinted from Schwartz et Al. Journal of the Electrochemical Society [81].

For etching of Si pillars using the two step technique, the following procedures were used. AZ 5214e photoresist was spun onto the surface of the sample. While it is capable of image reversal, this resist was chosen because of its low viscosity resulting in thin coatings. The process for producing positive tone features is similar to that for AZ 1529, and process steps are shown in Table 2.3. The resulting photoresist thickness was roughly 1.4 μm. After completing the lithography step, the sample was placed in an STS MESC Multiplex ICP system. This system is optimized for the Bosch process and allows for fast switching of plasmas constituents. Short etch/passivation cycles were attempted to reduce the scalloping typically associated with this process [82]. After the etching step, the photoresist was stripped with acetone followed by a methanol and isopropyl rinse. Upon completion of this step, the Si stamp was ready for imprinting.

Process Step		Process Step	
Resist spread time	2 s	Exposure dose	85 mJ/cm^2
Resist spead speed	50 rpm	Develop time	30 s
Resist spin time	40 s	Rinse time	2 min
Resist spin speed	4000 rpm	Hard-bake time	20 min
Soft-bake time	2 min	Hard-bake temp	100 °C
Soft-bake temp.	110 °C	Resist thickness	1.4 μm

Table 2.3: Process parameters for photolithography using AZ 5214e photoresist.

The second process for fabricating the Si stamp was through a single plasma process instead of using two steps to achieve positive sidewall features. Several plasma chemistries were used for this purpose. Adjustment of the gas ratios of a SF_6/O_2 plasma have been shown to allow for control of sidewall profile [79, 83]. For this chemistry, the SF_6 serves to etch the Si isotropically, as in the Bosch process. The addition of O_2 adds a passivation element to the process; therefore, high SF_6:O_2 ratios theoretically produce isotropic, undercut etched features, while lower ratios allow for increased directionality. In addition to SF_6/O_2, CHF_3 plasmas have been shown to etch Si with controlled sidewall angles [84]. This type of plasma deposits a polymer film on the Si surface. Bombardment of ions incident to the surface remove the passivation and etch the sample. Control of the sidewall angle is obtained by regulating the energy of the bombardment as higher energies tend to produce more isotropic etches.

Attempts at etching the Si stamp were made with patterns of both thick photoresist as well as several metal hardmasks. The photoresist used was AZ 9260 with the same photolithography techniques and equipment as previously describe were used to produce roughly 5 μm photoresist features. Table 2.4 lists each step in the process. After

completing the lithography step, the sample was placed in the same Oxford Plasmalab 100 system previously described. Before each run an O_2 plasma step with a dummy wafer was performed to clean the chamber. The system was plumbed with SF_6, O_2, and CHF_3. A variety of parameters for each type of plasma were varied to obtain positive sidewall angled features. Gas ratios were adjusted based on previous results as an attempt to obtain the desired result. Additionally, operating pressure and RF power were modified to further influence sidewall morphology. For CHF_3 plasmas, adjustment of parameters primarily focused on modifying RF power to increase ion bombardment of the sample; however, operating pressure and ICP power were also tuned to optimize etching. After the etching step, the photoresist was stripped with acetone followed by a methanol and isopropyl rinse. Upon completion of this step, the Si stamp was ready for imprinting.

Process Step		**Process Step**	
Resist spread time	5 s	Exposure dose	630 mJ/cm^2
Resist spead speed	50 rpm	Develop time	210 s
Resist spin time	30 s	Rinse time	2 min
Resist spin speed	5000 rpm	Hard-bake time	20 min
Soft-bake time	3 min	Hard-bake temp	100 °C
Soft-bake temp.	115 °C	Resist thickness	5.0 μm

Table 2.4: Process parameters for photolithography using AZ 9260 photoresist.

Once fabrication of the Si stamp was complete, imprinting of the template wafer could begin. A rudimentary process was used for this purpose, as shown in Figure 2.12. The Si stamp and template wafer were placed on a hotplate with the fluoropolymer of one wafer and the Si pillars of the template wafer facing each other. A weight was then

placed on the samples to provide pressure for imprinting, with a glass plate between the samples and the weight to improve the uniformity of pressure across the sample. The pressure applied to the samples was between 95 kPa and 200 kPa. After applying pressure to the samples, the temperature of the hotplate was ramped up to 300 °C, and held for 1 hr with a PID controller. While the specified molding temperature of the fluoropolymer is 240 °C, the increased temperature lowered its viscosity, decreasing the amount of pressure needed for imprint. The hotplate was then ramped down to room temperature, allowing the wafers to cool with no thermal shock. Once cooled, the samples were separated from one another using another rudimentary process in lieu of sophisticated equipment. Cyanoacrylate glue was applied to the backside of both the template wafer and Si stamp. Glass slides were then pressed to each wafer, allowing a bond to form between them. Once dry, the glass slides were pulled apart from one another, releasing the template wafer from the Si stamp, leaving imprinted vias in the fluoropolymer. Removal of each sample from its glass slide was accomplished by placing each on a hotplate and raising the temperature past the roughly 120 °C melting point of the glue. After removal and cooling of the samples, excess glue on the backside could be cleared away with an acetone swabbing step. Once cleaned, the Si stamp can then be used to imprint more fluoropolymer coated template wafers.

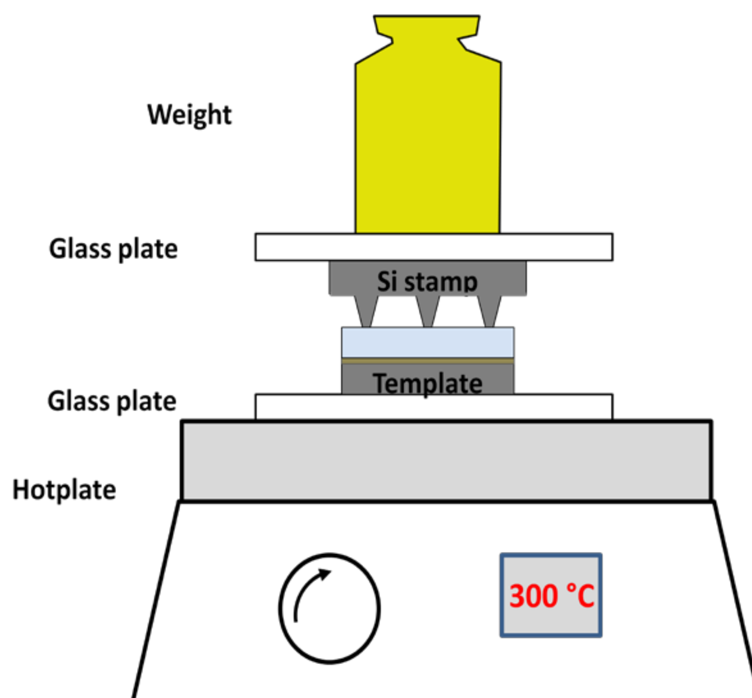


Figure 2.12: Illustration of the setup used to imprint the template wafer.

To remove any residual amorphous fluoropolymer from the imprinted features, a blanket plasma etching process was used. Because this residual layer was thin, an Ar only plasma was used for this purpose. Additionally, the enhanced capabilities of an ICP etching system were unnecessary for this step. Instead, a simple parallel plate RIE system was employed. The specific system used was a Technics West, Inc.® PE II-A system. An operating pressure of 100 mT was used with RF power at 150 W. Depending on the amount of residual amorphous fluoropolymer after imprinting, etch times between 1 and 3 minutes were used for the process. Once the residual layer was removed by this step, fabrication of the template wafer using the imprint lithography technique was completed and ready for In electroplating.

2.2.5 In Electroplating of Completed Template Wafers

Electroplating in general involves the reduction of metal ion M^{n+} in an electrolytic solution at the cathode with the addition of electrons to form a metal, given by the following cathodic reaction:

$$M^{n+} + ne^{-} \rightarrow M^{0} \qquad (2.4)$$

Based on this reaction, an equilibrium potential is given by the following equation:

$$E = E^{0} + \frac{RT}{nF} ln\ [a[M^{n+}]] \qquad (2.5)$$

Where R is the gas constant, T is the temperature, n is the number of electrons in the reaction, F is Faraday's constant, and $a[M^{n+}]$ is the activity of the ion. E^{0} is the standard electrode potential for the reaction. Tabulated values for this are available [85]. When current is applied to the electroplating setup, the field at the electrode, given by E(I) will be altered, resulting in an overpotential, given by the following [86]:

$$\eta = E(I) - E \qquad (2.6)$$

The relationship between current density and field at the electrode is given by:

$$J = aCe^{\frac{bE(I)}{RT}} \qquad (2.7)$$

where J is the current density, a and b are system constants, and C is the concentration of metal ions in the solution [87]. Current density is also defined as the current divided by the area plated at the cathode. Understanding these relationships is important when optimizing electroplating parameters. Good control of current density, hence

overpotential, is critical for obtaining a plated layer with the desired characteristics. Figure 2.13 is a graph of the appearance of plated chrome to the naked eye at various temperatures and current densities [88]. While the descriptions of the appearances given in the graph are somewhat subjective, general properties of the microsctructure can be inferred. The microstructure of the 'Bright' region of the graph likely has high density small grains, increasing reflection of light from its surface, which is optimal for most applications. The appearance of the other regions is due to increased roughening of the surface from either reduced plating density, formation of larger grains, or formation of dendritic structures.

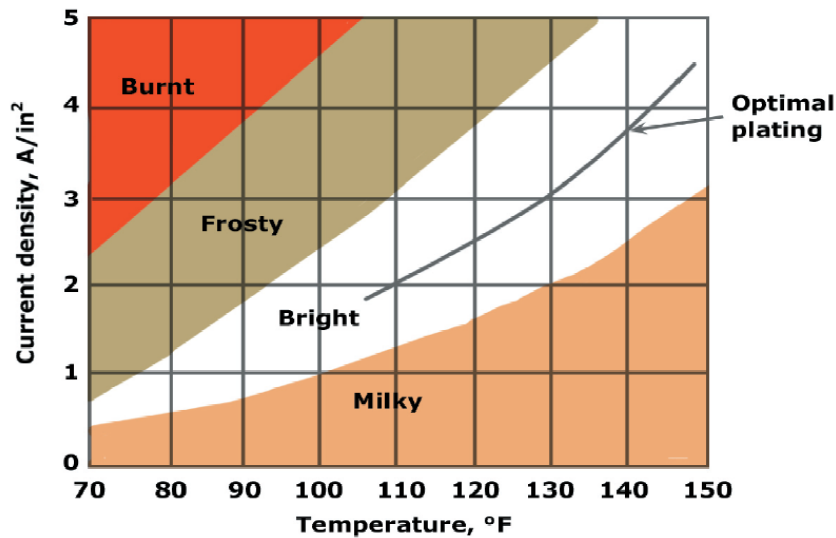


Figure 2.13: The appearance of plated chrome at various current densities and temperatures. Reprinted from http://www.platingbooks.com/HCrSection5secured.pdf [87].

For the application of In electroplating in this thesis, high density films with small grains are desirable. Current densities between 108 and 216 A/m^2 are optimal for such characteristics with In [31]. Current density also plays a role in deposition rate, given by:

$$d = C_E \frac{JN_M}{Fn\rho_M} \quad (2.8)$$

where N_M is the molecular weight of the plated material, ρ_m is the density of the plated material, and C_E is the cathode efficiency of the plating solution. Cathode efficiency is the proportion of current used for actual plating of the material at the cathode. For the In plating bath to be used, this value is .9 [31].

There are several challenges to electroplating In in general as well as for plating of bumps for this project in particular. Compared to other metals, electroplated In films consist of large, irregularly shaped grains even when operating in the optimal current density. Figure 2.14 shows images of electroplated In bumps from various sources [18,89,90] . Reduction of grain size to improve bump to bump consistency is key to developing a good plating process. Additionally, it is difficult to achieve good lateral thickness uniformity with electroplated In. Nonuniformities in electric field, from edge effects or otherwise, and nonuniformities in mass transport play a key role in the thickness uniformity. Determining plating conditions to reduce these effects is also critical. Finally, there are difficulties associated with the aspect ratio of plated bumps. The Peclet Number relates the velocity of agitation of the solution, given by V, to the diffusion coefficient of ions in the solution, given by D_d. This value is given by:

$$P_e = \frac{WV}{2D_d} \quad (2.9)$$

where W is the width of the feature. When plating, the solution is depleted of ions at the surface of the sample. Without agitation, a replenishment of the ions occurs only through

diffusion; thus, a diffusion layer forms near the surface of the sample. The thickness of the diffusion layer is given by:

$$d = (\pi D_d t)^{1/2} \tag{2.10}$$

where d is the diffusion layer thickness, and t is the period of agitation in the bath. As the thickness of the diffusion layer increases, plating become more erratic. To reduce this, increased agitation is necessary. As the Peclet Number approached 100, the thickness of the diffusion layer is sufficiently reduced to achieve efficient plating [87].

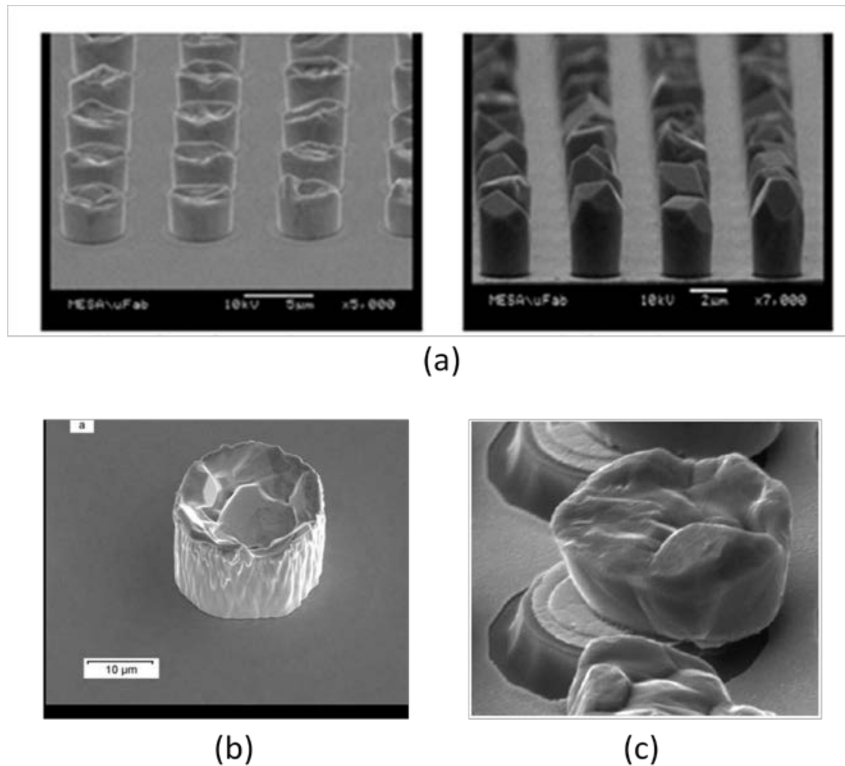


Figure 2.14: Examples of electroplated In from various sources. (a) Reprinted from J.J. Coleman et Al. Proceedings of SPIE, 2010 [89]. (b) Reprinted from Y. Tiang et Al. Proceedings from the Electronic Components and Technology Conference, 2008 [90]. (c) Reprinted for P. Merken, et. Al. IEEE Transactions on Advanced Packaging [18].

To reduce the diffusion layer thickness during In bump electroplating for this thesis, an ECSI IKO™ electroplating system was used. This system uses a reciprocating anode that comes in close proximity to the cathode. The anode is covered in with an insulating layer of fibers that agitate the surface of the sample when it moves closest to the cathode, thus reducing the thickness of the diffusion layer and improving plating control [91]. The system also includes a filtration unit to filter out impurities and improve mass transport. The anode itself has a 70 mm diameter and is composed of a Pt/Ti mesh with In wire interwoven to replenish the ions in the solution. Samples up to 100 mm in diameter can be placed in the system and contacted in three places. The system is equipped with a current controlling power supply capable of DC plating with currents up to 100 mA. It is also capable of pulse and reverse plating with amplitudes up to 300 mA and control of pulses down to a resolution of 10 μs. A commercially available indium sulfamate-based plating solution that contains organic additives to improve plating uniformity without altering In composition was used [92].

While the plating system has the capability to improve the quality of In electroplated into high aspect features, further optimization of plating parameters was necessary to reduce grain sizes and lateral nonuniformity. For this reason, optimization was performed on dummy samples rather than on completed template wafers. These dummy samples were fabricated by performing a photolithography step on a Ni/Si sample. AZ 9260 photoresist was used and follows a similar protocol to Table 2.4; however, features in 8 μm thick resist films were obtained by a 3000 RPM spin and increased exposure times. Deposition of a Ni seed layer follows steps previously described. The effect of plating with different DC current densities on thickness

uniformity was first explored. SEM and optical images were obtained at various locations of each sample to measure In bump thickness and coarseness of grains. Afterwards, adjustment of pulse plating parameters, including amplitude, duty cycle, and period, was investigated using the same characterization methods. Pulse plating has been shown to favor the initiation of grain nuclei, resulting in plated films with finer grains [43].

Once the parameters of the plating process were optimized, template wafers were plated with In bumps. The standard process for this was to electrically connect the sample to its removable holder and spray DI water on the surface for several minutes, allowing for the removal of all bubbles that might form at the Teflon features. After rinsing, the sample and its holder were placed in the electroplating unit and electrically connected to the power supply as the cathode. The sample then sat in the bath with no current applied for 3 minutes, with only the filter and reciprocating anode activated to agitate the solution. This soaking period allowed the electroplating bath to etch away any oxide found at the seed layer, exposing a consistent metallic surface. The power supply was then turned on, allowing for the plating process to begin. Once completed, the power supply, filter, and reciprocating anode were turned off, and the sample was removed. Finally, the sample was taken out of its holder and rinsed for several minutes, leaving a template wafer filled with In bumps.

2.2.6 Transfer of In Bumps from the Template Wafer

After the In electroplating step, transferring the bumps is the last step in the process. A hybrizider, also called a flip-chip bonder, was used for this purpose. The general operation of a hybridizer is to closely align two wafers, and then press them

together in a controlled manner with as little horizontal vibration as possible. For this project an RD Automation M8 flip-chip bonder was used. An illustration of the operation of this piece of equipment is shown in Figure 2.15. First, a sample is placed on the bottom chuck and held by a vacuum. The top chuck, which is on a hinge, is placed face up. The second sample is placed on this chuck and held by a vacuum. The top chuck is then flipped to place down and locked into place to the frame of the hybdridizer. Afterwards, boroscopes, controlled by translational motors, are placed between the two samples. These are simply an optical path with prisms at the end of it that guide light to both samples. The other ends of the boroscopes are attached to cameras. This setup provides an overlaid image of the positioning of the two samples, allowing for precise alignment.

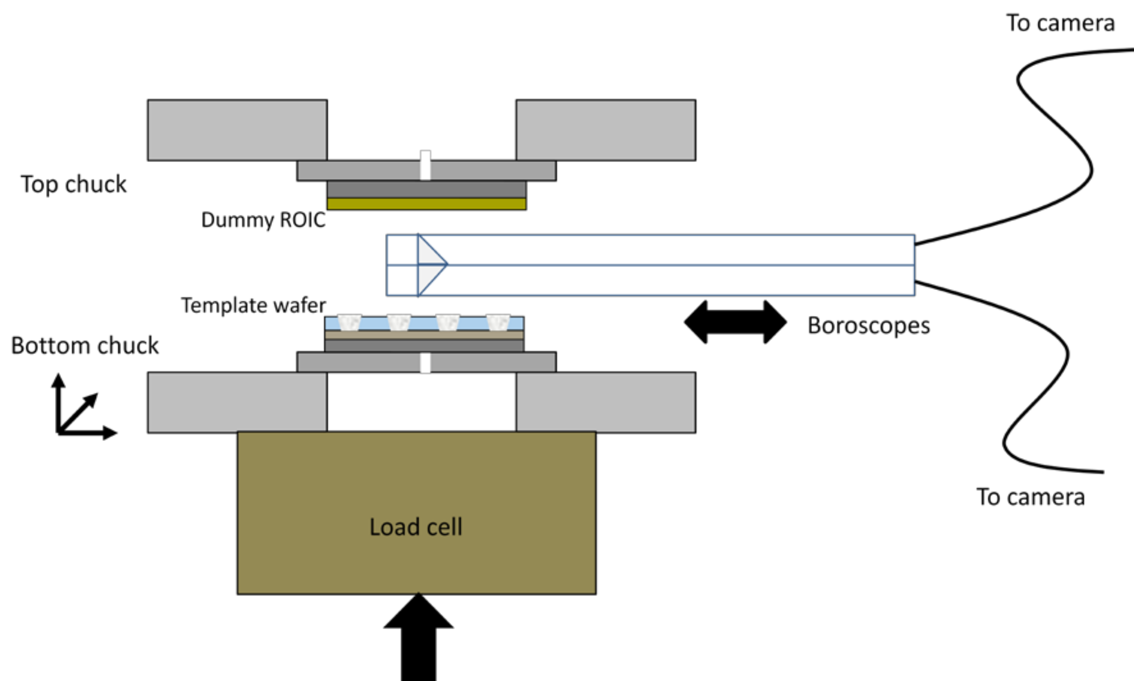


Figure 2.15: Simplified schematic of an RD Automation flip-chip bonder.

Once the boroscope is in place, the bottom chuck can be translated in the X and Y directions, as well as azimuthally. After alignment is complete, the boroscope is removed from in between the two samples. The bottom chuck is attached to a load cell that presses the two samples together. The load cell for this system is capable of providing 500 N force for pressing. Each chuck may be heated separately above the 156.4 °C melting point of In if desired, before and/or during the pressing phase. Samples can be pressed indefinitely, though typical pressing times or on the order of minutes to tens of minutes. The bottom chuck can also be allowed to pivot to provide improved planarity between the two samples. After pressing, the two chucks are separated from one another, the top chuck can be flipped face up, and the samples can be removed from the system.

The procedure for In bump transfer on the hybridizer followed the above procedures. Several process parameters were altered to optimize the process. Bonding force per bump was one of the key parameters altered in the process. Too high a force would result in shorting of adjacent bumps as any In overfill of the template wafer would be squeezed together. Alternatively, too low a force would likely result in no transfer as the In would not deform enough to have intimate contact with the dummy ROIC. Bonding temperature was also varied for the process from room temperature up to and past the 156.4 °C melting point of In. The purpose behind this was to determine whether raised temperature allowed for better adhesion to the dummy ROIC. Finally, pressing time was altered to determine if added time allowed for additional creep of In provided better contact to the dummy ROIC.

For the proof of principle sought for in this thesis, dummy ROICs were kept as simple as possible. These consisted of a blanket MoN_x layer sputtered on a Si substrate.

MoN_x has been used as a material for contact metallization for several reasons. The thermal expansion coefficient of Mo, listed as 4.8 – 5.1 10^{-6}/K [93] closely matches that of HgCdTe, limiting stress between the two layers upon thermal cycling. Additionally, MoN_x is typically used as a diffusion barrier for other metals [94,95]. A diffusion barrier between In and HgCdTe is critical as In is an n-type dopant and diffuses quickly into HgCdTe. While MoN_x is a ceramic, its resistivity remains low enough for contact metallization as N concentration is increased [96]. MoN_x films were deposited by reactive sputtering with N gas in an AJA International ATC-1800V magnetron sputtering system. The operation of a sputtering system is somewhat similar to that for parallel plate RIE. In this case, a sputtering target of the material to be deposited is biased on a plate so that ions strike it. This bombardment causes the molecules of the target material to sputter away. The sample is held closely to the target, where sputtered molecules deposit on the surface. DC sputtering of metals is typically performed to maintain high sputtering rates. The inclusion of a process gas allows for incorporation in the deposited film. For the MoN_x layers deposited in this project, the sputtering target was initially cleaned for 2 minutes in an Ar plasma. The sputtering deposition step was 20 minutes long with the following parameters: 5 mTorr operating pressure, 20 sccm gas flow consisting of an 80:20 $Ar:N_2$ gas ratio, and a plasma power of 200 W.

2.3 Characterization Equipment for In Bumps

In addition to optical microscopy, several other characterization techniques were used to determine various materials properties. These techniques are described in this section.

2.3.1 Scanning Electron Microscopy (SEM)

SEM was used for the bulk of the characterization while developing the transfer process. This included various aspects of the etching steps, imprinting steps, and In bump electroplating, looking at both absolute thicknesses and morphologies. This technique focuses electrons emitted from a source, usually through thermionic emission, with a set of electrostatic lenses. The narrow beam of electrons, typically on the order of several nm wide with an energy in the tens of keV range, is directed onto the sample. Several interactions with the sample and the incident electrons occur, including elastic backscattering, production of x-rays, and the formation of secondary electrons as shown in Figure 2.16. Secondary electrons are those formed by ionization of the material from the incident electron beam. It is these low energy electrons, on the order of 5 eV that are collected to form an image. Such low energy electrons are emitted from the nearest few Å of the sample surface, resulting in an image that reproduces the morphology of the sample [97]. For conducting samples no sample preparation was required; however, samples with insulating layer, including photoresist and amorphous fluoropolymer, require additional preparation since an electrostatic charge will form on them from the incident electrons. A roughly 10 nm thick Au layer was sputtered on the samples to prevent this from occurring, allowing for high quality imaging.

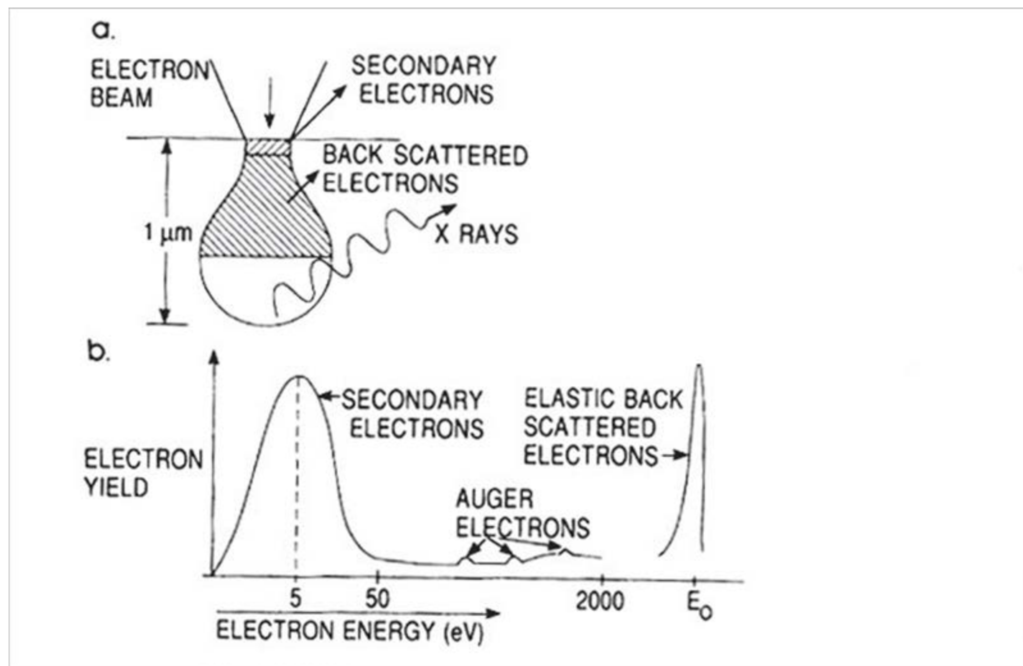


Figure 2.16: (a) Interaction of incident electrons with matter, and (b) the energy spectrum of electrons emitted from the surface of the material. Reprinted from M.C. Ohring, Materials Science of Thin Films [97].

2.3.2 Auger Electron Spectroscopy (AES)

AES is a technique used to measure the chemical composition of the surface of a sample down to about .1 % atomic concentration. It is centered on the formation of characteristic Auger electrons which are formed when an incident electron excites a core shell electron of an atom, leaving a hole. In order to reach a minimum energy state, an electron from an outer shell replaces the core shell electron. The energy released from this process can couple with another outer shell electron, releasing it from the atom if the energy is above its binding energy. This third electron is the Auger electron. Excitation of such electrons can be caused by an incident electron beam with energies around 1.5 – 5 keV. A hemispherical analyzer detects the Auger electrons where it detects only Auger

electrons of a certain energy range based on the bias applied. By sweeping this bias, a spectrum is formed of the Auger transitions present in the sample [98]. AES was used to measure the composition of N in the sputtered MoN_x dummy ROICs. A Phi 5800 system capable of AES, x-ray photoelectron spectroscopy (XPS), and ion scattering spectroscopy (ISS) was used.

2.3.3 X-ray Photoelectron Spectroscopy

XPS is another technique used to measure the chemical composition of the surface of a sample down to about .1 % atomic concentration. For this technique, a beam of x-rays is focused on the sample. These high energy photons excite electrons from the atoms of the sample which emerge with a characteristic kinetic energy. This kinetic energy is equal to roughly the photon energy minus the binding energy of the electron. Additional effects, such as the energy associated with intra-atomic relaxation, slightly alter the kinetic energy of the emitted electron [99]. Like AES, a hemispherical analyzer can be used to obtain a spectrum of the emitted electrons. While AES and XPS have similar sensitivities to atomic concentrations, XPS has the added benefit of determining the chemical state of the sample surface from slight shifts in binding energy due to different types of bonds. For this project, XPS was used to determine the composition of In electroplated using the ECSI IKO system with the indium sulfamate based bath. Like AES, a Phi 5800 system was used for the measurements.

2.4 Sample Preparation for Via Contacts

This section discusses the various types of samples used to develop small-pitch via contacts for FPAs.

2.4.1 Dummy Samples

A variety of dummy samples were fabricated to test the feasibility of Ni plating into high aspect ratio vias. Such samples are necessary due to the relatively high effort and cost involved in fabricating electrically active HgCdTe test structures and FPAs. In order to provide a reasonable prediction of feasibility, the dummy samples should be patterned with vias that have similar geometries to those found in small-pitch FPAs. Ideally, these vias should have aspect ratios greater than 2:1 with diameters less than 2 μm. After establishing feasibility of both the electroless and electroplating Ni processes, the dummy samples can also be used to begin optimizing each process for this particular application.

Figure 2.17 shows the structure of the dummy samples. Like the template wafers process, the samples consist of a Si substrate with a blanket metal seed layer deposited on it for plating initiation. A photolithography process is then performed to define vias in photoresist, followed by an O_2 ashing step to descum the bottoms of the features and to expose the metal seed layer. Initial samples were fabricated using the same techniques as described above in Section 2.2. Electron beam evaporation was used to deposit 100 nm Ni on 25 nm Ti films on HF-dipped Si wafers. AZ P4330 photoresist was used to define vias on the metal seed layers using standard contact photolithography.

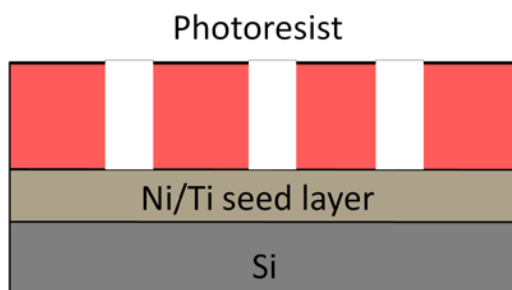


Figure 2.17: Illustration of the structure of the via dummy samples.

The resulting vias were roughly 4 μm tall with a diameter of 3 μm. Vias with smaller diameters could not be produced due to limitations of the photolithography system. A 30 W O_2 descumming step followed using a barrel asher. While these dummy samples were not ideal, they provided a starting point from which to begin Ni plating. Improved dummy samples were provided by a partner in industry. The process to fabricate these samples was similar to that above, however a stepper was used to obtain smaller features in the photoresist rather than using a contact mask aligner. The operation of such a system differs significantly from contact photolithography. Rather than exposing the photoresist to UV light with a mask directly in contact with the sample, UV is passed through the mask and projected onto the sample using complex optics. While such systems are substantially more complex, they offer the benefit of improved resolution over contact photolithography. Additionally, no degradation of the photoresist or mask itself occurs during the process as there is no contacting step required [100]. Figure 2.18 is a cross-sectional SEM image of the resulting structure. 1.1 μm diameter vias were formed in roughly 4 μm thick photoresist, resulting in aspect ratios greater than 3.5:1. Additionally, the positive slope of the sidewalls in the photoresist closely

resembles the shape of vias etched in HgCdTe for FPAs. Based on these dimensions, such features provide a good representation of active small-pitch FPAs.

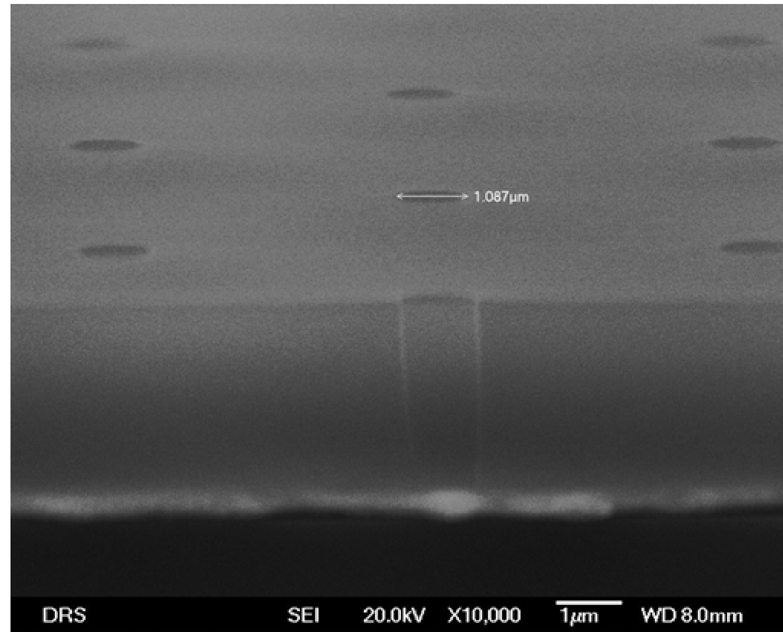


Figure 2.18: Cross-sectional SEM image of a via dummy sample fabricated using a stepper for photolithography.

2.4.2 Mechanical Arrays

Before plating of active test structures and FPAs was performed, Ni via contacts were plated for mechanical arrays, followed by the characterization of the physical aspects of the contacts. These mechanical arrays were provided by an industry partner. The structure of such arrays is similar to that shown in Figure 1.8, however several aspects are simplified. With no need for electrical characterization, the grid contact is removed. Additionally, the ROIC is replaced with a structure consisting of a blanket film of Ni on a Si substrate epoxied to the II-VI detector structure. This structure is substantially simpler than the ROIC and allows for a simple electrical contact scheme for

Ni electroplating. The exposed Ni at the bottom of the vias then acts as the seed layer for electroless and electroplated Ni. A variety of via diameters and pitches were provided on the mechanical arrays. Figure 2.19 is a SEM of a mechanical array with a portion of the sample milled by a focused ion beam (FIB) to reveal the structure of the smallest vias that were formed. These vias had a top diameter of 7.8 μm and were 12 μm thick. While the scale of these vias was larger than desired, they provided a means to determine how the plated Ni interacts with the true materials found on an FPA, including HgCdTe, CdTe, and the epoxy. This could not be accomplished by the dummy samples alone.

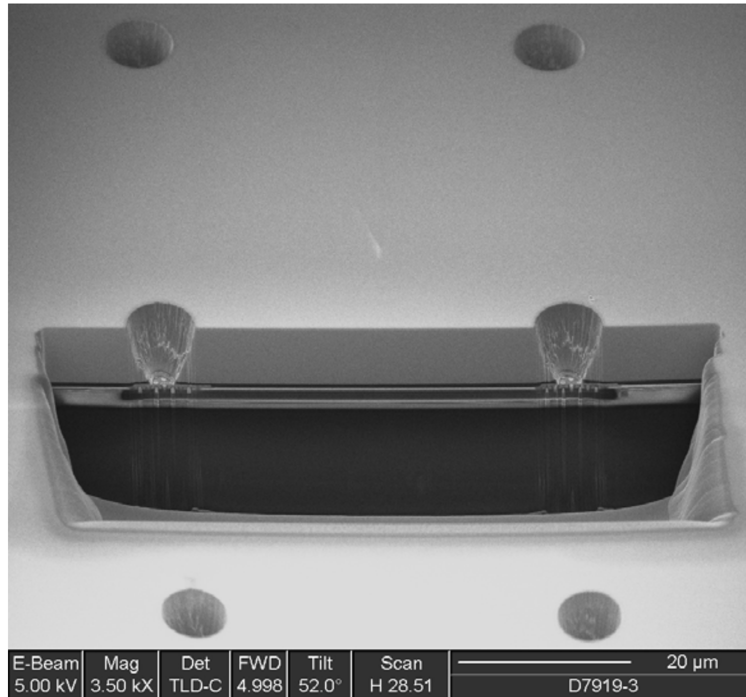


Figure 2.19: SEM/FIB image of several vias of a mechanical array.

2.4.3 Electrically Active Test Arrays and FPAs

Full up test arrays and FPAs were provided by the industry partner, whose simplified structure is shown in Figure 1.8. The test arrays used the same pattern as the

mechanical arrays, with 12 μm thick vias that had diameters down to 7.8 μm. These arrays were epoxied to active ROICs capable of electrical testing of each individual diode. The active layers consisted of LWIR HgCdTe. LWIR material in particular was chosen due to its increased sensitivity to stress as HgCdTe hardness decreases as the x-value of the material decreases [22]. The propensity to form dislocations under the stress of the Ni contact would likely contribute to an increased dark-current of the device. Several small-pitch MWIR FPAs with active ROICs were also provided for Ni plating and characterization. These arrays have a unit cell size of 5μm with a 720 x 1080 format. The vias are formed in material that is 4.75 μm thick, and their diameter is 1.6 μm at the top. While the ROIC pads can be universally grounded to allow for electrical contact to each device in the array for Ni electroplating, this was not provided up to the present; therefore, only electroless Ni contacts were made to the active test and FPA structures.

2.5 Ni Plating of Via Contacts

The following section discusses both the electroplating and electroless Ni processes used for via contact metallization. The electroplating theory follows that laid out in Section 2.2.4

2.5.1 Electroplating Ni

Unlike In electroplating, a wealth of literature exists for various aspects of Ni electroplating [29,101-103] for both industrial and microelectronics applications. Unlike In, Ni can be electroplated with fine grain structure, allowing for better lateral uniformity

of plated films. Because of this, the focus of the plating setup was to optimize the mass transport of Ni ions to the surface of the sample to ensure good lateral uniformity of plated Ni with no voids due to bubbles.

Figure 2.20 is an illustration of the Ni electroplating setup that was constructed for this project. A 1 gallon polypropylene tank was used as the container for the bath. A commercially available Ni electroplating mixture was dissolved in DI water to form the electrolytic solution. This mixture was composed of $NiSO_4$, $NiCl_2$, and boric acid. Ni is reduced from the $NiSO_4$ and $NiCl_2$ components to form the plated film. The boric acid acts as a pH buffer for the bath, helping to maintain optimal conditions for the process [104]. The current density for optimal plating for this bath is 27 – 161 mA/cm^2. Both the cathodic sample and the anode were held by PTFE dippers and suspended from a bar held at the top of the polypropylene container.

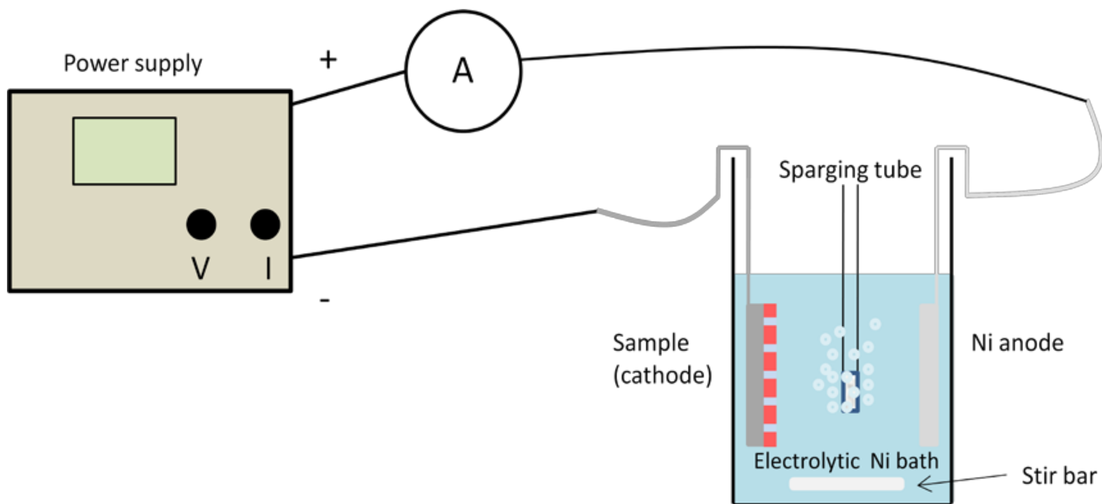


Figure 2.20: Illustration of the electroplating setup used for Ni contact metallization.

This method allowed for maintaining parallelism between the two electrodes. Additionally, precise control of the separation between the two could be achieved. For

this plating setup, the separation was held at 5.1 cm. A soluble anode in the form of a 75 mm, 99.99% purity Ni sputtering target was used to replenish the plating bath of Ni ions. The power supply used for In electroplating and described in Section 2.2.4 was used to provide constant current to the electrodes of the Ni plating bath. Connection between the power supply and anode was achieved through an insulated Pt wire. Pt was chosen in particular due to its inertness in the solution. Connection to the sample was achieved through an insulated Ni alligator clip with limited exposure to the plating solution. A stir bar was placed in the tank, with the entire setup placed on a stirrer, to maintain a well-mixed, consistent solution. Additionally, a sparging tube was placed at the bottom of the tank, connected to a N_2 source, and aligned so that the resulting bubbles passed across the front surface of the sample. When plating on the sample is initiated, H_2 bubbles evolve from the cathodic reaction. These bubbles tend to stick to the surface of the sample, blocking further plating beneath them resulting in is non-uniformity of plated films. Sparging thus becomes necessary to avoid this problem.

Unlike the electroless process to be discussed, a limited parameter space of the electroplating was explored. DC plating of Ni features was found to be sufficient to produce void-free films that had small grains and high lateral uniformity. Pulsed plating was, therefore, an unnecessary complication for this process. One of the key constraints of the process for this application is the current density of plating. ROICs are typically specified with an upper limit for current density so as not to destroy any devices on the chip; therefore, current densities at the bottom of the 27 – 161 mA/cm^2 window will be investigated. Such constraints on the ROIC also make pulsed plating less desirable as there might be potential to damage parts during the transient behavior of the pulses. Bath

temperature can also be adjusted to optimize the electroplated Ni process. While plating rate can be altered by temperature, this is not a critical issue for plating relatively thin features. Bath temperature has been shown to modestly alter grain size for $NiSO_4$-$NiCl_2$ solutions, sitting between 25 and 35 nm over the temperature range studied [105]. Such differences are negligible compared to the size of features being plated. Crystallographic texture of electroplated Ni has also been shown to change as a function of bath temperature [101, 105]. Texture can lead to different internal stresses in the plated film. Stress of plated Ni films will be investigated and discussed further.

2.5.2 Electroplated Ni Experiments

Before any electroplating experiments were performed, the compatibility of the Ni plating bath with II-VI materials was studied, including both CdTe and HgCdTe found in FPAs. The primary concern is that the plating bath might be an etchant of these materials. MBE-grown CdTe/Si and HgCdTe/CdTe/Si samples were first examined using SEM. The samples were then placed in the plating bath with no current applied for 4 hours. After this time, the samples were rinsed and examined using SEM to determine whether etching occurred.

Nucleation of electroplated Ni on electron beam evaporated Ni on Si substrates was investigated using short plating times. After rinsing a dummy sample under DI water for several minutes to remove bubbles formed on the photoresist surface, it was placed on the PTFE dipper and connected to the negative terminal on the power supply. Stirring and sparging were then applied to the bath, and the sample was held for several minutes with no current applied. Current was then applied to the sample with a density of roughly 25

mA/cm^2 for times ranging between 30 s and 5 min. After the plating process, the samples were rinsed for several minutes in DI water and given an N_2 blow dry. Finally, the samples were characterized using both optical microscopy and SEM. Plating of both dummy samples and mechanical FPAs followed this procedure. In addition to plating of Ni onto electron-beam evaporated Ni, which simulates the ROIC contact pad, Ni electroplating directly onto MBE-grown HgCdTe films was investigated. This study was important as the Ni must contact the electrically active HgCdTe layer. Once contacted, the HgCdTe layer may or may not provide another growth surface for plating affecting the shape of the Ni contact plug. The same steps to process the dummy samples were used to pattern HgCdTe/Si samples, including the use of AZ P4330 photoresist. Preparation and plating of these samples also followed the procedure above.

Several surface preparations of both the electron beam evaporated Ni and HgCdTe were investigated to determine their affect on the morphology and nucleation of electroplated Ni. This included both HCl and HNO_3 preparations. An HCl preparation was used for HgCdTe samples as it strips the oxide from the surface leaving bare semiconductor. A 20s dip in 38% HCl in water followed by a DI water rinse was inserted just prior to the plating process described in the previous paragraph. A similar process was used for the removal of any oxide formed on the evaporated Ni surface using diluted HNO_3. For this process, a 10s 10% HNO_3 dip was used.

Compositional analysis of electroplated Ni was performed to determine impurity levels in the Ni films. For PVD techniques such as evaporation, high purity sources are used as the deposition material, ideally resulting in a thin film of similar purity on the sample. In electroplating, any impurities in the bath can potentially plate out with the

desired material onto the sample, resulting in a substantially lower purity. While some types of impurities will likely do little to alter the operation of the HgCdTe diode or contact metal, others could have a major impact. Cu in particular is a fast-diffusing p-type dopant in HgCdTe [106]. Because the Ni contacts directly to the n^+ HgCdTe of the FPA, Cu impurities would compensate or even type convert this region. Such alteration of the electrical characteristics of the diodes would not be acceptable. Blanket Ni films electroplated onto HgCdTe by the techniques described previously were analyzed for composition using XPS with the oxide layer sputtered away and compared to the composition of electron beam evaporated Ni films.

Another important property of the electroplated Ni films is resistivity. Relatively low resistivity is important because the Ni acts to electrically contact the ROIC to the diodes of the detector array. Both impurities and grain structure of the Ni layer can alter this value. Resistivity was measured using the four-point probe technique, which will be discussed further in the Characterization Techniques section that follows. In order to obtain a reliable value for electroplated Ni, the film needed to be isolated from other conductors; therefore, plating directly onto evaporated Ni would not work as the resistivity data would reflect both Ni layers. Instead, Ni was plated onto LWIR HgCdTe. The resistivity of such a layer was approximated by the equation:

$$\rho = \frac{1}{ne\mu} \tag{2.11}$$

where n is the carrier concentration, e is the charge of an electron, and μ is the electron mobility. For the n-type HgCdTe samples tested, the n was measured to be $2\text{x}10^{15}$ cm^{-3} by secondary ion mass spectrometry (SIMS) and μ was measured to be 120000 cm^2/Vs

using the Van der Pauw method. Based on these values, the resistivity of the HgCdTe layer was calculated to be 2.6×10^{-4} (Ωm). This value is substantially higher than the value of 7×10^{-8} (Ωm) given for Ni [49] and, thus, essentially acts as an insulator for the Ni in the resistivity measurement. The electroplating process followed previous procedures.

The stress of electroplated Ni on both Ni films/Si and HgCdTe was studied for several reasons. As discussed in the Introduction, HgCdTe is sensitive to stress compared to other semiconductors. Large stresses upon the material tend to induce dislocations, resulting in the degradation of diode electrical characteristics. Additionally, the Ni features will be plated into vias on Ni pads on a Si ROIC, so determining their stress is important. Large stresses may result in delamination from the ROIC pad, resulting in an open contact. X-ray diffraction (XRD) was used to measure the stress. Details of technique will be discussed in the Characterization Techniques section that follows. Direct measurement of the stress of Ni contact plugs was not possible using XRD. Instead, a 3.5x1 cm tab of each of MBE-grown HgCdTe/CdTe/Si and electron beam evaporated Ni/Si was cleaved off a larger wafer, to be blanket electroplated with Ni films. XRD measurements were first made prior to electroplating for a baseline value. After this initial measurement, three electroplating/XRD measurement iterations followed. This allowed for calculating the absolute value of stress in the Ni film, whether a compressive or tensile stress was present, as well as tracking the stress as the Ni film grew thicker. Additional measurements of electron beam evaporated Ni/Si were also performed for comparison. XRD was also used to measure the crystallinity of electroplated and electron beam evaporated Ni films. Ideally, such measurements allow for determining which crystallographic phases are present in the film, as well as the crystallographic texture of

the film. If large levels of impurities form bonds in the lattice, their presence may be detected by this technique.

2.5.3 Electroless Ni

As previously discussed in Section 1.4.2, electroless plating is an autocatalytic process that results in the deposition of a material by the presence of a reducing agent in the bath, and does away with any external power supply. The resulting reaction follows that of Equation 2.4. Electroless plating of metals can occur on conductors, semiconductors, and even nonconductors with the proper preparation step. In general, several steps are required to deposit a material in a controlled manner using this technique. The process typically starts with a cleaning step to remove any organic contaminants on the surface of the sample. Such contaminants would inhibit plating and reduce overall quality of the plated film. Standard solvent rinses such as toluene, acetone, methanol, and isopropyl alcohol can be used for such a purpose. The sample is then placed in a sensitizer solution that initiates nucleation sites on the surface of the sample for deposition to occur during the catalytic process. An example of a sensitizer is a solution of $SnCl_2$ in water. An activation step follows which removes any oxide layers from the surface and any contaminant from the sensitizing step allowing for more consistent plating initiation and improved adhesion. An example includes a solution of $PdCl_2$ in dilute HCl. In some cases the sensitizing and activation steps can be combined to a single solution. Finally, the sample can be placed in the electroless plating bath which consists of several chemicals that serve different purposes. The source of the plating material is typically composed of a metal salt that provides the metal ions in the plating solution. For Ni, either $NiSO_4$ or $NiCl_2$ could be used. A reducing agent is also

required that supplies electrons to the metal ions in the solution for the reaction in Equation 2.4 to occur. Ideally, the reduction occurs only at the surface of the sample and does not result in precipitation of the deposition material in the bath. A variety of reducing agents exist for electroless Ni, including: $NaBH_4$, NaH_2PO_2, and dimethylamine borane (DMAB) to name a few. To improve qualities of the bath, other additives may be added. Complexing additives, which are chelating agents, help to reduce side reactions away from the sample surface by binding to various ions in the plating bath. Complexing agents include: ethylenediaminetetraacetic acid (EDTA), thiourea compounds, and triethanolamine (TEA). Stabilizers are added to increase the lifetime of the plating solution and to prevent decomposition for an extended period of time. Finally, buffers can be added to a solution to maintain the pH of the bath as the process occurs. Buffering is important in maintaining consistency in the process as plating progresses [107].

A large number of permutations of preparation steps and bath compositions exist for electroless Ni and several have been described in the literature [108-110]. A process described by Tiwari 2011 was selected as the basis for the electroless plating of Ni via contacts for FPAs [111]. This process was used for a similar application: namely high aspect ratio vias in Si with Cu contact pads at the via bottoms. Additionally, high quality Ni features could be plated without the necessity for sensitizing and activation steps; therefore, cleaned samples could be placed directly in the plating solution without the need for additional steps. The baseline electroless Ni plating solution used 42.6 g/L $NiSO_4 \cdot 6H_2O$ in DI water as the ion source. 15 g/L of EDTA dipotassium salt dihydride was mixed in a complexing agent. The reducing agent used for this bath was DMAB at a concentration of 8 g/L. TEA was used as a second complexing agent in the bath at a

concentration of 42.5 mL/L. The addition of TEA was shown to reduce the bath temperature necessary to begin nucleation of Ni. Finally, 4.9 mL/L of NaOH was used as a pH buffer. The plating solution does not contain any stabilizers; therefore, the bath lifetime listed was on the order of tens of minutes, requiring disposal after each use. This is unlike many plating solutions which can be held in a tank and maintained for much longer periods of time.

An illustration of the electroless Ni plating setup used for this thesis is shown in Figure 2.21. A volume of DI water was first measured with a graduated cylinder and poured into a glass beaker which was positioned on the hotplate and heated so that the water was 55 °C as monitored by a thermometer. A stir bar was placed in the beaker to ensure a more uniform temperature throughout the plating solution and for improved mixing of the plating solution. Proper concentrations of each of the constituents of the solution were then measured out using a precision scale for solid components, a graduated cylinder for the TEA, and a calibrated micropipette for the NaOH. Once the water temperature stabilized, each component of the solution was poured into the water and allowed to mix together for 10 minutes. After this time, the sample, held by forceps, was placed into the solution. At this point, Ni plating of the sample is initiated. Periodic manual agitation of the samples was performed to improve mass transport. Additionally, the temperature of the bath was monitored to ensure it did not stray more than 2 °C from the intended value. After plating, samples were rinsed with DI water and dried with N_2. This process, with some variation, was used to plate each of the varieties of samples from dummy samples to active FPAs.

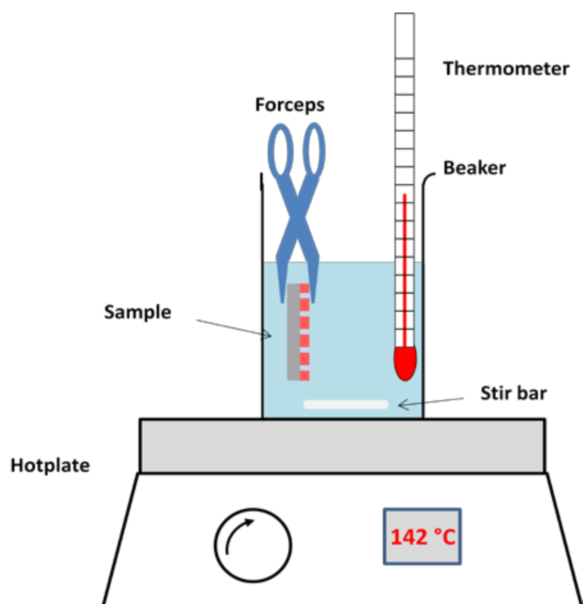


Figure 2.21: Illustration of the electroless plating setup used for Ni contact metallization.

2.5.4 Electroless Ni Experiments

Each of the experiments performed on the electroplated Ni were repeated for electroless Ni. This included: the compatibility of electroless Ni with HgCdTe and CdTe, nucleation studies of electroless Ni on Ni/Si dummy samples, electroless Ni plating directly onto HgCdTe, and the effects of surface preparations on Ni/Si and HgCdTe on electroless Ni nucleation. Characterization of the fundamental properties of the electroless Ni films, including compositional analysis, resistivity measurements, stress and crystallinity were also repeated. Such measurements are key as DMAB-based electroless Ni yield films that contain B in concentrations as high as 11.46% [112]. The addition of B is likely to increase the resistivity of the plated film similar to Ni films that use a P based reducing agent such as NaH_2PO_2. These films incorporate P into the plated Ni and have been reported to increase the resistivity of the film tenfold for films containing 10% P [113]. The stress of the plated film is also likely to vary for different B

concentrations. The effect has been shown for P based electroless Ni where films may be under tensile or compressive stress depending on the P concentration [113]. A B based electroless Ni solution was selected over a P based bath due to compatibility with the n^+ region of the HgCdTe detector array, which is doped with B.

In addition to the experiments listed above, several others were performed to better understand the plating process. Concentrations of the bath constituents were altered to determine how they affected plating rates and the morphologies of plated features. Bath temperature was also altered to determine how it impacts the plating process. Plating was performed at various bath ages to determine how stable the plating solution was over time. Each of these experiments was performed to establish a window in parameter space for which the plated Ni had desirable properties.

As previously discussed, active HgCdTe diode test structures and FPAs were plated using the electroless Ni process to establish contacts inside the vias. The plating procedures directly followed those described above. After plating and cleaning the samples, they were sent to an industry partner for electrical testing of the samples. Dark current I-V measurements were taken of the devices at their facility. For the diode test structures, I-V measurements were compared to those with via contact metallization formed by PVD to look for any degradation due to the plated Ni. Additionally, thermal cycling of samples, followed by additional electrical testing was performed to determine the stability of the contacts. Cryogenic cycling was performed by dunking the samples directly into liquid N_2. This process is essentially a thermal shock test and provides the most pessimistic picture of contact stability. Baking at elevated temperatures for several days was also performed for the same purpose.

2.6 Characterization Equipment for Ni Via Contacts

A variety of characterization equipment was used in developing the Ni via contact process. Like the In bump work, optical microscopy and SEM were heavily relied upon to determine plated Ni morphologies and thicknesses. XPS was also used to determine the compositions of electroplated, electroless and electron beam evaporated Ni. Additional techniques were used to further characterize aspects of the Ni plating processes and are discussed later in this section.

2.6.1 FIB/SEM

FIB milling was used in conjunction with SEM for cross-sectional imaging of plated Ni contacts in mechanical arrays. This technique was used in lieu of cleaving because the Ni contacts themselves were too robust to cleave. Figure 2.22 shows the results of such attempts where Ni plugs appear either fully intact, or fully delaminated from the cleaved edge of the sample. In order to cross section the Ni plugs themselves to get a better idea of how plating growth progresses, a more sophisticated technique was necessary. The operation of an FIB system bears resemblance to an SEM, as illustrated in Figure 2.23 which shows a FIB milling/deposition station. Unlike SEM, where electrons are extracted from a source and focused using electrostatic lenses, ions are extracted from the source in FIB. One common method for extracting ions is with a liquid metal ion source (LMIS). For this type of source a liquid metal, typically Ga, is fed from a reservoir to the end of a sharp W tip. A large field is placed on the tip that emits Ga^{+} ions. The ions can be tightly focused down to the nm to tens of nm range and rastered onto a sample where several interactions occur. Sputtering of the sample can occur from the physical bombardment of

the ions at the surface of the sample. Deposition using FIB can also occur with the inclusion of feeder gases that adsorb on the surface of the sample. If chosen correctly, the gases interact with the FIB, dissociate, and bond on the surface of the sample. Similar to SEM, secondary electrons are produced from the interaction between the FIB and sample. These may be detected to form an image of the sample surface [114].

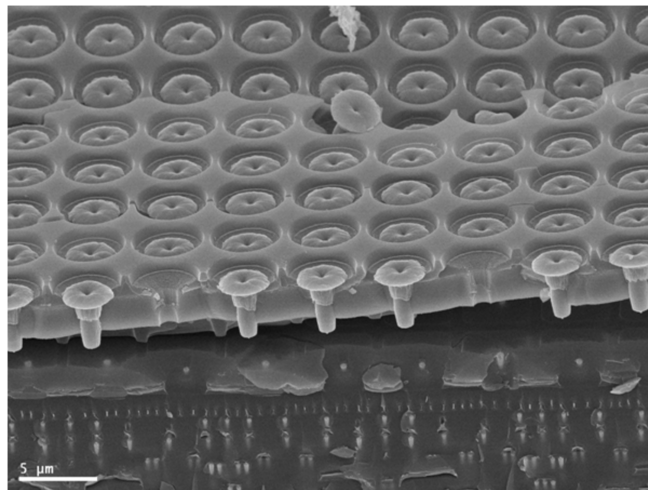


Figure 2.22: SEM image of a cleaved array with Ni contacts either fully intact or removed.

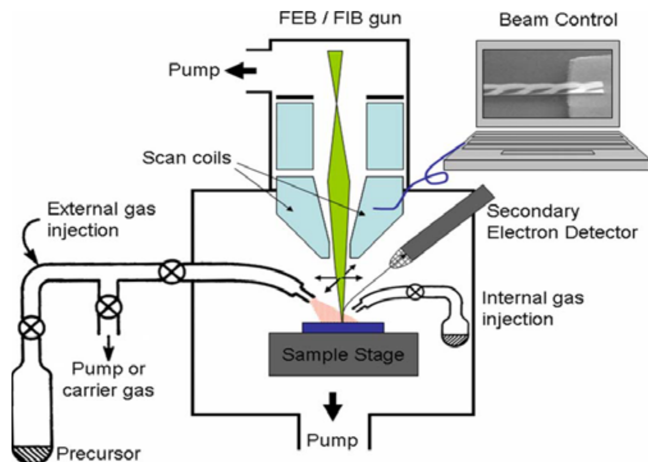


Figure 2.23: Illustration of a FIB/FEB nanofabrication system. Reprinted from I. Utke et Al. Journal of Vacuum Science and Technology B [114].

2.6.2 Four-Point Probe

One method to measure the resistivity of a thin film is by four-point probe. Resistivity values were obtained on electroless, electroplated, and electron beam evaporated Ni to confirm suitability as a contact material. The operation of this technique is illustrated in Figure 2.24. Four probes, typically collinear, are contacted to the sample. A current is passed across the outermost probes while the voltage drop between the two inner probes is measured. Ideally, Ohm's law can be used to obtain the value of sheet resistance; however, geometric factors must be applied to obtain an accurate value. For collinear probes with spacing much greater than the thickness of the film, such as is the case for the Ni samples generated, a multiplicative factor of 4.5325 should be applied [115]. Resistivity of the film is then obtained by multiplying the film thickness by the sheet resistance measured. Sheet resistances were measured using a 4 Dimensions Model 280 four-point probe.

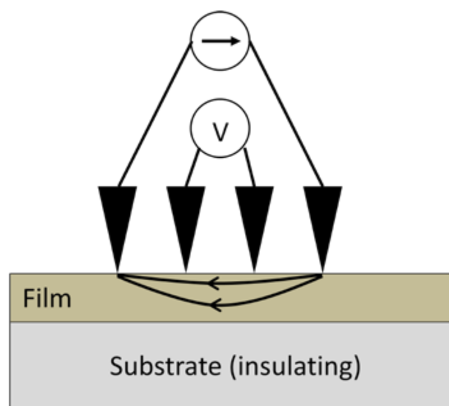


Figure 2.24 Illustration of the four-point probe method for obtaining sheet resistance.

2.6.3 XRD Analysis

XRD was used to measure the stress and crystallinity of plated and electron beam evaporated Ni films. Measurements using this technique are dictated by Bragg's law, given by:

$$n\lambda = 2d\sin\theta \qquad (2.12)$$

where n is the index, λ is the wavelength of the diffracting radiation, d is the interatomic spacing, and θ is the angle of the incident radiation with respect to the surface of the sample. The value if d can be calculated for cubic crystals, including Si, HgCdTe, CdTe, and Ni using the following equation:

$$d = \frac{a}{\sqrt{h^2+k^2+l^2}} \qquad (2.13)$$

Where a is the lattice constant of the crystal and h, k, and l are the Miller indices of the crystalline plane measured. When radiating a sample with x-rays, diffraction from the sample only occurs at angles that meet the conditions for Equation 2.12. An x-ray diffractometer makes use of this by precisely measuring θ to calculate the value of a in the sample [116].

An illustration of the Bede D1 diffractometer used for XRD measurements is shown in Figure 2.25. Radiation is provided by a sealed tube source generating Cu Kα x-rays set to 40 kV and 30 mA on a power supply. A set of slits on the source side cuts down angular divergence of the beam. An asymmetrically cut (110) Ge channel-cut crystal used in four-bounce mode monochromates the x-rays so that only Cu Kα_1

radiation, with a 1.54056 Å wavelength are passed onto the sample. The sample sits on a four-circle goniometer capable of both x and y-axis translation as well as tilt adjustment and azimuthal rotation.

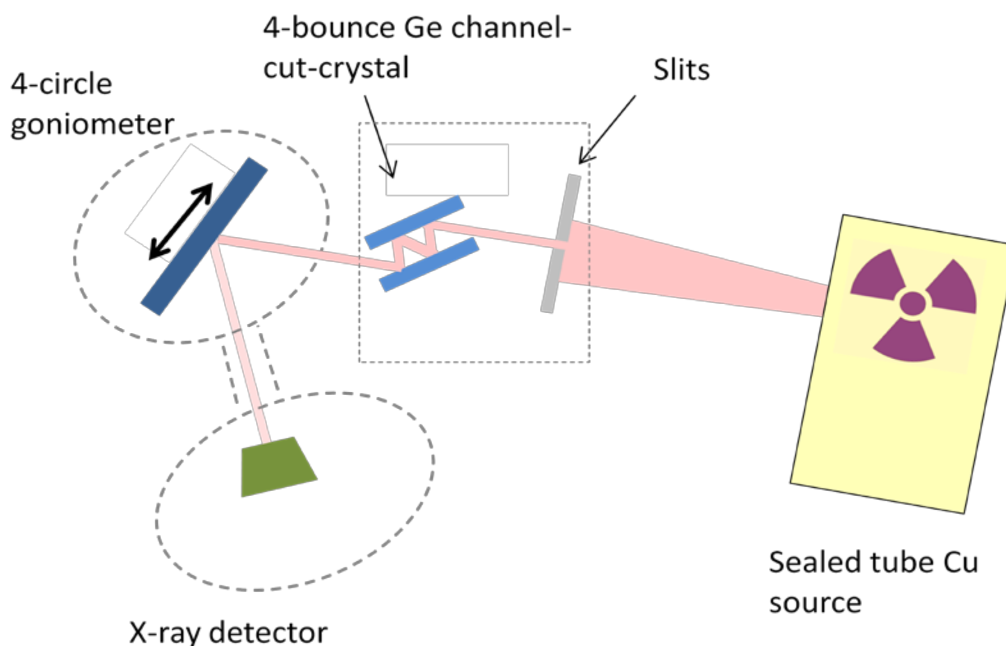


Figure 2.25: Illustration of the Bede D1 system used for XRD measurements.

The goniometer also rotates the sample around its z-axis, and the angle formed between the incident x-rays and the sample surface is known as ω. X-rays diffracted from the sample are collected by an x-ray detector sitting on an arm that rotates around the z-axis of the sample. The angle formed between the incident x-rays and those diffracted from the sample is known as 2θ. Measurement of this value gets plugged into Equation 2.12 to obtain a value for d. The precision of measurement of ω and 2θ for this system is 1 arcsec, allowing for measurement of d down to the ten thousandths of an Å.

Calculation of plated Ni stress was obtained by first taking XRD measurements of a bare substrate prior to Ni deposition as a baseline. This measurement began by finding the location of the symmetric reflection of the substrate. For the <100> Si wafers, the [400] reflection was used and for the <211> HgCdTe/CdTe/Si, the [422] HgCdTe reflection was used. The measurement was taken by stepping the 2θ angle twice as fast as the ω angle to precisely obtain the location of the peak. Peak locations were obtained every 2 mm down the entire 3.5 cm length of the samples. From these measurements, the radius of curvature of the sample can be obtained by the following:

$$R = \frac{x}{\delta\theta_B} \tag{2.14}$$

Where R is the radius of curvature, x is the linear distance between points, and $\delta\theta_B$ is the angular peak shift in radians. After taking the initial set of measurements, Ni was plated onto the sample, and the measurement process was repeated. Ni film thickness was then measured by SEM. Film stress was calculated using Stoney's equation [117], given by:

$$\sigma = \frac{1}{6}\left[\frac{1}{R_{post}} - \frac{1}{R_{pre}}\right]\frac{E}{(1-\nu)}\frac{t_s^2}{t_f} \tag{2.15}$$

where σ is the film stress, R_{post} is the radius of curvature after plating, R_{pre} is the radius of curvature pre plating, E is Young's modulus, ν is Poisson's ratio, t_s is the substrate thickness, and t_f is the film thickness. Positive values of σ indicate tensile stress while negative values are indicative of compressive stress.

Unlike the stress measurements, where diffraction from single-crystal semiconductors was collected, the crystallinity measurements sample polycrystalline Ni.

For polycrystalline material, the direction of the surface planes typically varies from crystal to crystal; therefore, the diffraction condition is met by only a portion of the crystals in the film for any ω and 2θ value. This can result in reduced diffraction intensity, requiring longer integration times to achieve a suitable signal to noise ratio. The measurement itself is performed by stepping the 2θ angle twice as fast as the ω angle over the positive range of angles available for the diffractometer. Any symmetric reflections within the angular range are then detected. These peaks can be indexed by applying Equations 2.12 and 2.13 to determine what materials, crystalline phases, and crystalline texture may be present in the film.

Chapter 3

Patterning of the Template Wafer

3.1 Introduction

The processes and results of pattern definition of the template wafer for the In bump transfer technique are discussed in this chapter. Most of the process development related to this revolved around determining a technique that reliably patterned features in the Teflon AF layer with desired characteristics for this application; namely features with a positive sidewall angle to enhance transfer of In which expose the metal seed layer for electroplating. Because of the challenges involved with this, two different processes were attempted. The first used standard lithography and plasma etching with a hardmask, as shown in Figure 2.2. The second process, shown in Figure 2.4, utilized hot embossing to obtain features in the Teflon AF layer. Each approach will be discussed in the following sections.

3.2 Patterning with Standard Lithography

3.2.1 Layer deposition

As shown in Figure 2.2a-b, the initial steps in template wafer fabrication required the deposition of three layers onto a Si substrate, including the conductive metal seed layer, the nonconductive Teflon AF layer, and the Ti hardmask. The deposition of the metal seed layer was relatively straightforward where the Si substrate was prepared with

an HF dip as previously described. This was followed by the metal layer deposition by means of electron beam evaporation using the parameters found in Table 2.1. Initially, a .5 μm thick seed layer was deposited directly onto the Si substrate. Another approach became necessary since the Ni tended to peel from the Si due to inferior adhesion between the two, along with the internal stress of the Ni film. Instead, a 50 nm Ti sticking layer was deposited before the Ni which successfully limited the peeling of the Ni layer without altering its conductive surface.

Coating of the Ni/Ti seed layer with the Teflon AF nonconductive layer was not entirely straightforward. After performing the dilute HCl dip of the template wafer to strip the Ni oxide, a variety of methods were attempted to coat the wafer with a consistent layer of the amorphous fluoropolymer. Initial spinning of the 18 % Teflon AF using a pipette failed due to the high viscosity of the liquid that caused bubbling when dispensed. When spun, the bubbles produced long-thin raised areas on the films. This problem was solved by dispensing the liquid directly from the bottle, pouring from roughly 2 cm above the sample; no bubbles were produced from the dispensation. While this issue appeared to be solved, large thickness nonuniformities were still observed in the spun layers visible to the naked eye, along with microscopic ripples at the surface of the Teflon layer as seen by optical microscopy. The initial spinning process included a 500 rpm spreading step for 5 s before a faster spin step. Removal of the spreading step eliminated the microscopic ripples. It was determined that a skin was forming on the Teflon AF layer during the spreading step due to evaporation of the FC-770 perfluorocarbon diluent. This spreading step was, therefore, omitted for all Teflon AF coating processes. The issue of thickness nonuniformities was resolved by spin coating Teflon AF that had been further diluted in

FC-770. Two main recipes, shown in Table 3.1, were used to obtain consistent coatings. After the coating process, samples were baked and cooled according to the previously discussed procedures. Both recipes included an initial spin of 2.1 % Teflon AF, which while only resulting in a several hundred nm thick coating, allowed for high thickness uniformity of a second, thicker Teflon coating. Recipe #1 used several 3000 rpm coating steps to build a consistent Teflon layer of the desired thickness. Two iterations of this process resulted in 5.5 μm thick layers while four produced 8.9 μm thick coatings as measured by cross-sectional SEM. The thickness did not double since the FC-770 in the dispensed solution etches back the Teflon layer that has already coated the sample.

Recipe 1			**Recipe 2**	
Teflon 1 Conc.	2.10%		Teflon 1 Conc.	2.10%
Spin Speed 1	3000 rpm		Spin Speed 1	3000 rpm
Spin Time 1	1 min.		Spin Time 1	1 min.
Teflon 2 Conc.	12%		Teflon 2 Conc.	12%
Spin Speed 2	3000 rpm		Spin Speed 2	1250 rpm
Spin Time2	1 min.		Spin Time2	1 min.
	Repeat Teflon 2			

Table 3.1 Recipes used to coat template wafers with Teflon AF. Note: red font refers to steps that were iterated.

A second recipe was developed that used only a single 12 % Teflon coating step utilizing a slower spin speed that resulted in 5.9 μm thick coatings. This recipe was developed to reduce the amount of Teflon wasted in the inefficient spin coating process. Coating iterations to build up a thicker Teflon layer were unsuccessful and resulted in thickness inconsistencies. Interference fringes were observed for the 5.5 and 5.9 μm coatings. Typically, two to three thickness fringes appeared across a sample excluding edges and

corners. The condition for constructive interference of light incident to a thin film, based on matching the phase reflected from the top and bottom surfaces, is given by:

$$2nd\cos\theta = m\lambda \tag{3.1}$$

where n is the index of refraction of the film, d is the film thickness, θ is the angle with respect to the normal of the surface, m is index, and λ is the wavelength of the incident light. Destructive interference occurs at m-½ and is observed as a dark fringe on the sample surface. The value of n for the Teflon AF used is 1.31 [54]. Assuming a λ of 580 nm, based on the yellow filtered light in the cleanroom and a θ of 0, the appearance of each fringe represents a thickness change of about 100 nm in the Teflon film. The appearance of two or three means a lateral thickness uniformity of 200 to 300 nm was achieved across a sample, which is sufficient for this application. While a considerable Teflon AF edge bead formed during the coating process, it could be removed by swabbing the edges with FC-770 which cleared away excess Teflon similar to acetone for a photoresist edge bead removal procedure. Alternatively, the edges could be cleaved off leaving a sample of consistent thickness uniformity.

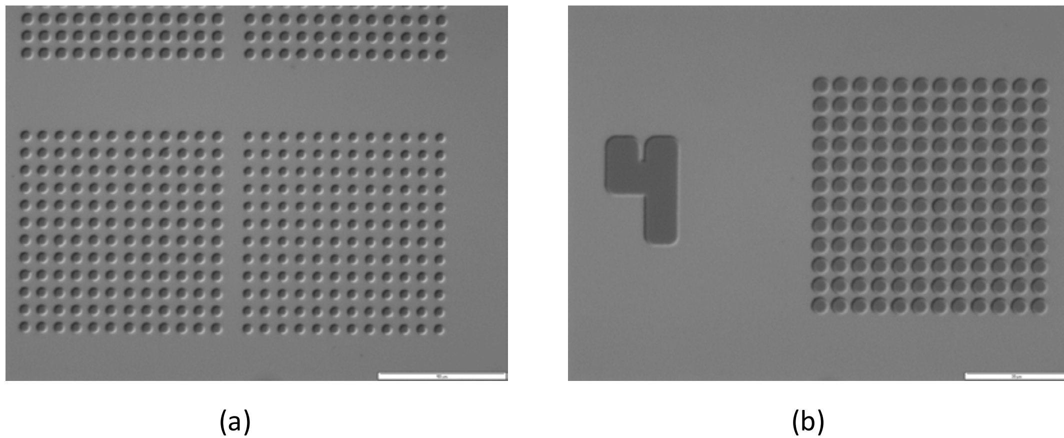
Like the deposition of the seed layer, the hardmask deposition was relatively straightforward. This layer was necessary as photoresist did not adhere to the Teflon AF surface. A 50 nm Ti hardmask was deposited by electron beam evaporation using the parameters found in Table 2.1.

3.2.2 Ti Hardmask Patterning

Patterning of the Ti hardmask to allow for etching of the amorphous fluoropolymer followed the deposition steps, as shown in Figure 2.2c-d. The photolithography step, using AZ 1529 photoresist, was clear-cut and followed the process parameters of Table 2.2. Likewise, the O_2 plasma descumming step was used in case any photoresist remained at the bottom of features in the photoresist. Etching of the hardmask, both by wet chemical and plasma etching, was then performed to form features in the Ti.

As previously described, a solution of H_2O:HF:HNO_3 was used to etch the Ti hardmask. The previously reported etch rates of 1100 nm/min for a 20:1:1 solution at 20 °C of this etchant [73] were too fast to controllably etch a 50 nm layer. Instead, the solution was diluted down to 100:1:1 to slow the etch rate. Samples were held in the solution for 40 s after H bubbles began to evolve from the surface of the sample, upon which the sample was rinsed in DI water to stop the etching process. The etching step typically took about 40 s. Figure 3.1 shows optical microscopy images of successfully etched Ti layers that were deposited directly onto Si. The pitch of features in Figure 3.1a is 7 μm and is 4 μm in Figure 3.1b. While these relatively small features successfully etched through the Ti layer, the chemical etching process was unpredictable to some extent. In some cases the etching step took longer than expected, moreover, there were several instances where the Ti layer was not completely etched through. Ti is highly reactive and readily forms a native oxide when exposed to air [118]. Based on the apparent latency period of the etching process where no H is evolving at the sample surface, it appears most of the time required to etch the Ti layer involves stripping its

native oxide. Because of this, samples with different oxide thicknesses due to longer exposure to air may have drastically different etch rates. In addition, incomplete etches produce a problem since the native oxide grows while the sample is exposed to air while studying it under the microscope. This re-growth of the oxide complicates further etching of the partially etched Ti layer.



(a) (b)

Figure 3.1: Ti/Si hardmasks patterned by wet etching: (a) 7 μm pitch and (b) 4 μm pitch features.

A plasma etching process containing F compounds was developed to both reduce process variability and over-etching associated with wet chemical etching. F has been reported to spontaneously react with Ti at temperatures above 200 °C, and CF_4 plasmas have been shown to etch Ti [75]. Based on the reactivity of Ti with the F atom, both CF_4 and SF_6 were initially considered as possible etchants. Only a CF_4 process was developed since SF_6 has been shown to etch through photoresist several times faster. Maintaining a higher etch selectivity of Ti over photoresist is important for this process in order to avoid wearing through the photoresist entirely, which would result in unwanted etching

of the hardmask, or require using a thicker photoresist which may reduce the resolution of the contact lithography process.

Experimentation using the parallel plate RIE system was focused on determining a recipe that etches through the 50 nm Ti thick hardmask without wearing completely through the photoresist and damaging the entire hardmask. Also, for actual template wafers the Teflon AF layer will not act as an etch stop for the process as CF_4 plasmas have been shown to etch Teflon [51]. Obtaining a tight bound on the time required to etch through the Ti layer was, therefore, key to not etching the Teflon in an uncontrolled manner. 50 nm thick Ti layers deposited by electron beam evaporation onto Si substrates were used as witnesses to develop the process. After some initial experimentation to determine ballpark parameters for Ti etching with an appreciable rate, a series of experiments was run to optimize the CF_4 plasma process. Table 3.2 summarizes the parameters used and results obtained.

Recipe	1	2	3	4	5	**6**	7	8
Operating Pressure (mTorr)	150	150	150	150	150	**150**	150	50
CF_4 flow	40	40	40	40	40	**40**	40	40
Power (W)	200	200	200	50	50	**80**	80	80
Time (s)	30	60	120	240	420	**240**	180	240
Ti etched away?	No	Yes	Yes	No	No	**Yes**	Sometimes	Yes
Photoresist stripped?	No	No	Yes	No	No	**No**	No	No

Table 3.2: Key recipes used for plasma etching of the Ti hardmask.

Out of the eight recipes listed, four had the favorable result of completely etching the Ti layer without damaging the rest of the hardmask due to complete removal of the photoresist layer. Recipe #2 successfully did this but was not chosen due to the relatively small window in time for which the process had a favorable result. Basically, the power

was too high for optimal control of the process. When power was reduced to 50 W, as for recipes #3 and #4, no appreciable etch rate was observed. An 80 W plasma power appeared to be ideal for the process, where two of the recipes used etched the Ti layer with consistently favorable results. Recipes #6 and #8 yielded indistinguishable results. Pumping the chamber of the Trion RIE system was performed by a turbomolecular pump, easily achieving the 50 to 150 mTorr operating pressures used for this set of experiments. RIE systems that only have a mechanical pump for chamber evacuation might have difficulty controllably maintaining a 50 mTorr operating pressure but would likely be able to operate at 150 mTorr. Recipe #6 was chosen as the hardmask etching process due to its higher operating pressure, allowing it to be run on simpler, mechanically pumped RIE systems.

Once the plasma etching process was developed, it was tested on actual template wafers. Figure 3.2 shows several optical microscopy images of etched Ti hardmasks on Teflon AF layers. In Figure 3.2a, a non-optimal process was used where the photoresist was completely stripped during the etch step, resulting in a damaged hardmask. Closer inspection of the image revealed noticeable roughness in the amorphous fluoropolymer indicating the etch process was too long. Figures 3.2b and 3.2c are images taken after performing the optimal etch process where the features are fully etched into the Ti layer without damaging the hardmask. Darkened features appearing on the Ti layer in Figure 3.2b are due to photoresist that was not completely removed from the sample. Features with a 4 μm diameter on a 10 μm pitch are shown in Figure 3.2c.

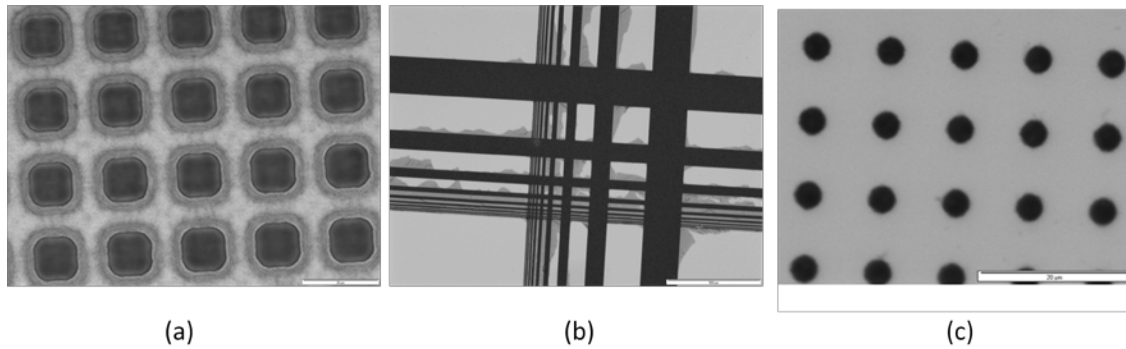


Figure 3.2: Ti hardmasks on Teflon AF layers patterned by CF_4 plasma etching: (a) over-etched hardmask, (b) grid lines showing the resolution of the process and (c) 10 μm pitch features etched in Ti.

3.2.3 Etching the Amorphous Fluoropolymer Layer

A summary of the key Teflon AF etching experiments is shown in Table 3.3, where the process parameters are listed along with the resulting sidewall profile of the etched layer. The experiments are highlighted in four groups each representing a set of parameter changes. The basis for the initial ones used was the previously documented etching of similar layers [60, 61]. These studies found the right set using high-density plasmas to etch features in perfluoropolymers similar to Teflon AF with vertical sidewalls. As previously discussed, the goal for this project was to etch features with a positive sidewall angle to enhance the predictability of In bump transfer. Adjustment of parameters was, therefore, primarily focused on etching features having such a shape with the etch rates being of secondary importance at this point.

Recipe	1	2	3	4	5	6
Ar Flow (sccm)	39 (95%)	39 (95%)	39 (95%)	40 (89%)	40 (80%)	40 (74%)
O_2 Flow (sccm)	1.8 (5%)	1.8 (5%)	1.8 (5%)	5 (11%)	10 (20%)	14 (26%)
Operating Pressure (mTorr)	3	3	3	3	3	3
ICP Power (W)	500	500	500	500	500	500
RF Power (W)	0	6	26	10	10	10
Time (min)	10	10	10	15	15	15
Sidewall	Vertical	Vertical	Vertical	Vertical	Vertical	Vertical

Recipe	7	8	9	10	11	12
Ar Flow (sccm)	40 (67%)	40 (67%)	40 (67%)	0 (0%)	50(50%)	20 (50 %)
O_2 Flow (sccm)	20 (33%)	20 (33%)	20 (33%)	50 (100%)	50 (50%)	20 (50%)
Operating Pressure (mTorr)	10	50	80	30	30	15
ICP Power (W)	500	500	500	2000	2000	2000
RF Power (W)	10	10	10	10	10	10
Time (min)	10	10	10	20	12	12
Sidewall	Vertical	Vertical	Vertical	Isotropic	Isotropic	Isotropic

Table 3.3: Key recipes used for plasma etching of Teflon AF layers.

The first group of experiments, Recipes #1-3, focused on determining the effect of adding an RF bias to the plasma. The 95%/5% Ar/O_2 mixture of process gases was used as an initial best conjecture to obtain positive sidewalls. After etching, the samples were cleaved, and cross-sectional SEM images were taken to determine sidewall angle and etch rate. For each of the recipes, vertical sidewalls were obtained. The addition of the small RF bias, however, drastically altered the etch rate. With no applied bias, the etch rate was .12 μm/min. This increased to greater than .6 μm/min for recipe #2, where only 6 W RF bias were applied. Recipe #3 saw a similar result as the entire 6 μm amorphous fluoropolymer layer was etched within 10 min. The additional momentum imparted by this bias greatly increased the desorption from the surface of the layer. The ratio of gas mixtures was then altered in Recipes #4-6, from 89%/11% Ar/O_2 to 74%/26% Ar/O_2. The

initial expectation was that the additional O_2 would add enough of a chemical component to the etch to add a small horizontal etch component, producing the desired sidewall angle. Instead, the recipes produced features with a vertical sidewall. Figure 3.3 shows SEM images of the etched features using recipe #4. Figure 3.3a shows a cross-sectional view where the vertical sidewall is evident. A slight overhang appears at the top of the structure and is due to the fact that the cleave of the feature occurred near its edge. The angle view in image 3.3b shows an intact Ti hardmask and a clean, Teflon AF free, bottom surface exposing the Ni seed layer. Some degree of curtaining appears in each image, potentially due to slight etch back of the Ti hardmask. Only the etch rate of the processes appeared to be affected by the addition of O_2. The first two recipes etch fully through the Teflon AF layers, while the third etched at a slower rate of .32 μm/min. This result is inconsistent with those in the literature that reported etch rate saturated with the addition of O_2 [61].

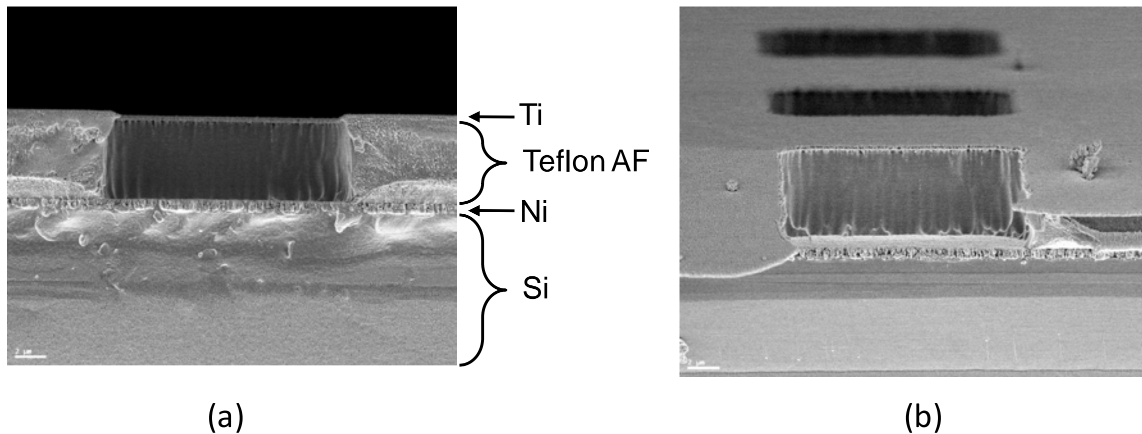


Figure 3.3: SEM images of features etched into Teflon AF using recipe #4: (a) cross-sectional and (b) angled view.

The third group of Recipes, #7-9, went further in trying to produce some degree of isotropic etching by boosting the O_2 content to 33% and by increasing the operating pressure of plasma to increase the number of collisions of the plasma constituents. Once again, each recipe yielded features with a vertical sidewall. Like the addition of O_2, raising the operating pressure reduced the etch rate. This dropped from .3 μm/min for recipe #7, to .08 μm/min for #8, to .04 μm/min for #9. The final three recipes went to the extreme of using O_2 only to see whether the mainly chemical attack component of the gas would produce an isotropic sidewall. A feature etched using recipe #10 is shown in Figure 3.4, displaying the negative sidewall shape. The last two recipes attempted to find a medium between the two types of sidewalls observed. Unfortunately, both recipes #11 and #12 failed to do so and produced similarly isotropic features. When comparing obtained results to the literature, it appears that the subtlety in different types of similar fluoropolymers may have led the differences in obtained results as neither discussed the etching of Teflon AF specifically.

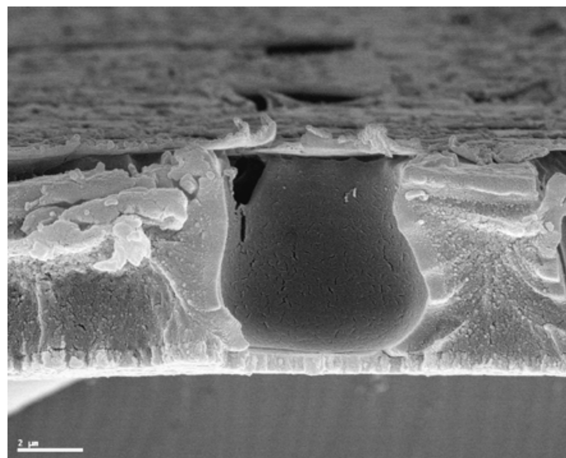


Figure 3.4: Isotropic feature in Teflon AF etched using recipe #10.

After being unable to find a recipe to etch the Teflon AF layers with a positive sidewall angle, a reflow step was attempted to attain the desired sidewall angles. Samples etched using recipe #5, which produced vertical sidewalls, were used for this purpose. Ti hardmasks were first removed using the blanket H_2O:HF:HNO_3 described above, rinsed in DI water, and blow dried with N_2. Samples were then placed on a PID-controlled hotplate and heated above the 160 °C T_g of the amorphous fluoropolymer. After attempting various temperatures and times, a 180 °C reflow for 1 min produced a desirable as well as a reproducible result, shown in Figure 3.5. Sidewalls with a clearly positive angle appear in the nearly cross sectional image of Figure 3.5a. Obtaining a quantitative value for sidewall angle is difficult since it is not constant. As would be expected, the reflow caused rounding of the Teflon AF edges, meaning much of the horizontal movement of the layer occurred at the top and bottom regions. This is desirable because In filling such a feature would be most likely to neck off and pull from the Ni seed layer near the interface. A top down view of a reflowed feature is shown in Figure 3.5b, where the Ni seed layer inside the feature remains free of Teflon.

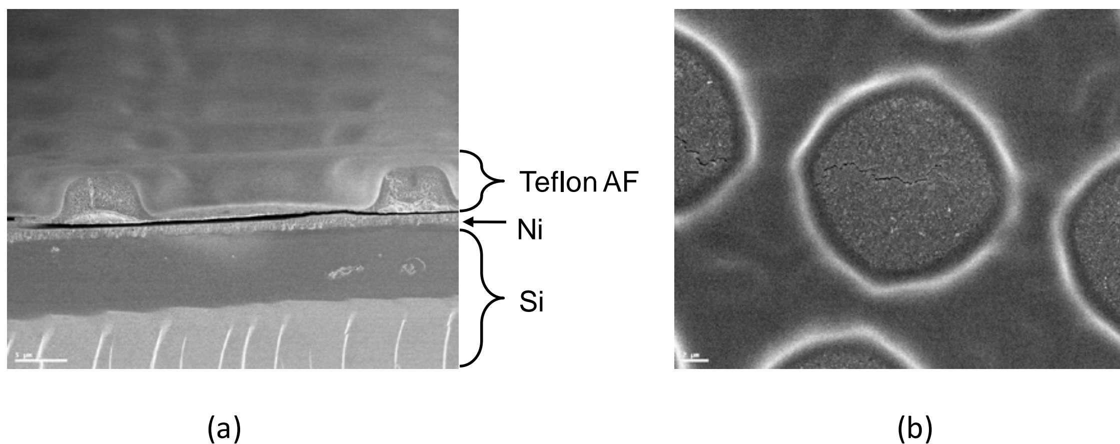


Figure 3.5: SEM images of Teflon AF/Ni/Si reflowed for 1 min at 180 °C: (a) cross-sectional and (b) plan view.

The high viscosity of the amorphous fluoropolymer allowed for controllable results, as such sidewalls were reproducible run after run. While this process appeared to provide a solution to the sidewall problem, there are difficulties associated with scaling down the process. Figure 3.6 shows an angle SEM image of a sample reflowed for 3 min at 180 °C. It is clear that the consistency of the thickness of Teflon AF was lost. The regions of Teflon AF directly between two adjacent bumps lost more thickness than the regions between four bumps due to the rounding down of edges during reflow. Achieving good transfer of bumps likely requires In must be plated thicker than the tallest regions of the amorphous fluoropolymer. In order to satisfy this requirement, adjacent In bumps will tend to short together. This effect would become worse at smaller pitches where features are moved closer together.

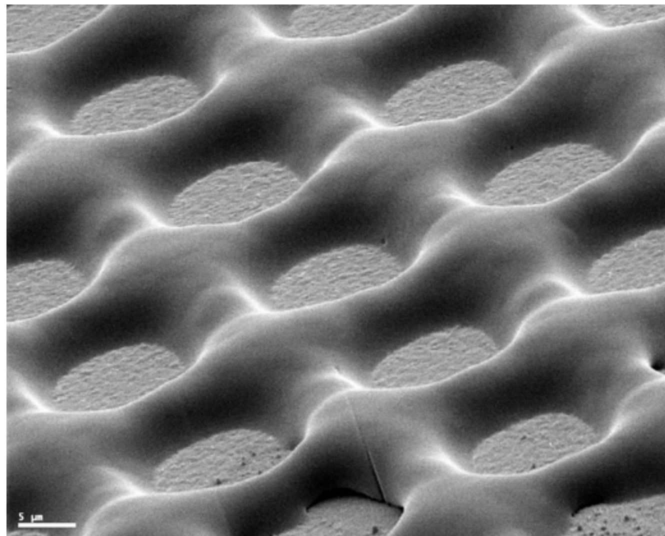


Figure 3.6: Teflon AF/Ni/Si reflowed for 3 min at 180 °C showing the deterioration of thickness uniformity of the reflowed layer.

3.3 Patterning with Imprint Lithography

3.3.1 Si Stamp Fabrication

Fabrication of the Si stamp necessary to imprint an unpatterned template wafer followed the process illustrated in Figure 2.9. After patterning the wafer with photoresist, pillars were etched into the Si stamp. The key characteristic of these pillars was that they needed a positive sidewall angle to imprint such features in the Teflon AF layer of the template wafer. Additionally, relatively smooth features were necessary to limit the surface area and, thus, adhesion to the Teflon AF during the imprinting step.

The two-step Si etching procedure included an initial DRIE step followed by a chemical etch in HF:HNO_3 diluted in DI water. Prior to etching, samples were patterned with AZ 5214e photoresist. This process was straightforward and allowed for patterns of 3 μm features on a 6 μm pitch with a 1.4 μm thickness. Results of Si pillars post DRIE etch are shown in Figure 3.7. The initial DRIE process, which used cycles with a 9.6 s SF_6 etching step with a 7 s C_4F_8 passivation step, resulted in .68 μm/cycle etching of Si. An SEM of pillars obtained with this process is shown in Figure 3.7a. The overall shape of the sidewall was vertical; however, the period used for the process resulted in prominent scalloping of the sidewalls. To reduce the scalloping effects, shorter periods were attempted. The results of etching by means of a 4.8 s SF_6 etching step with a 3.5 s C_4F_8 passivation step are shown in Figure 3.7b illustrating that the sidewalls of the pillars remain vertical with a drastically reduced scalloping effect. The etch rate was reduced to .19 μm/cycle which is larger than expected based on the relative time of the SF_6 etching steps but is likely due to the switching time of the DRIE system and transients associated

with switching from etching to passivation steps. While reduced, the etch rate using the faster cycles is still sufficient for this application.

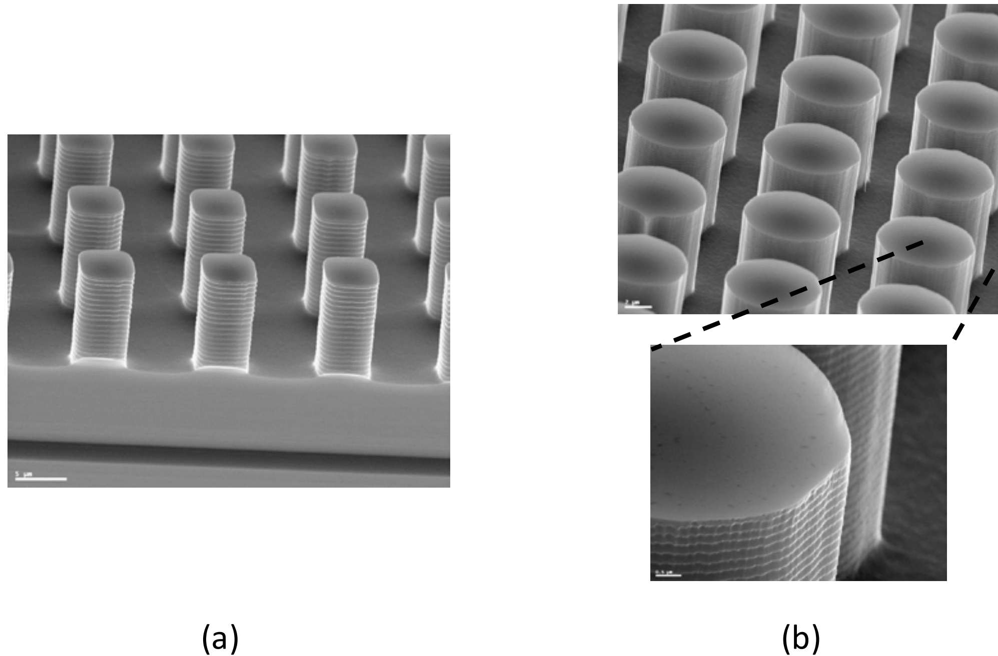


Figure 3.7: SEM images of Si pillars etched by DRIE: (a) initial process and (b) process with reduced cycle times and limited scalloping.

High selectivity of etching Si over photoresist was also observed with Figure 3.8 showing photoresist remaining on top of DRIE etched Si pillars in a cross-sectional SEM image. Only .2 μm of the original 1.4 μm of photoresist was removed while 10.9 μm of Si was etched resulting in a selectivity of 55 where values of roughly 100 have been reported [120]. While lower than reported values, the selectivity is high enough for etching pillars using the relatively thin AZ 5214e photoresist process.

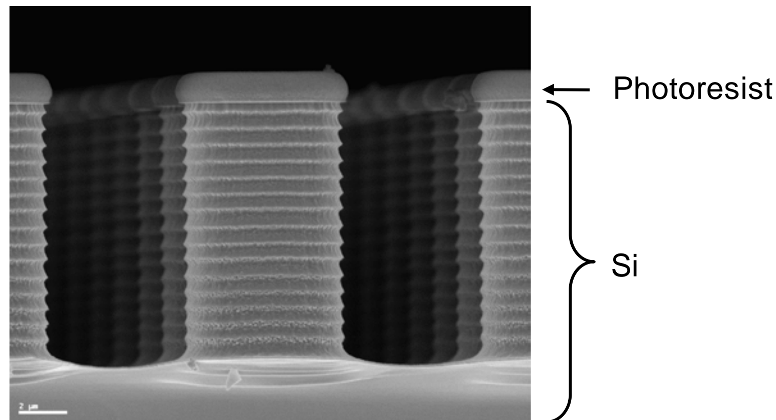
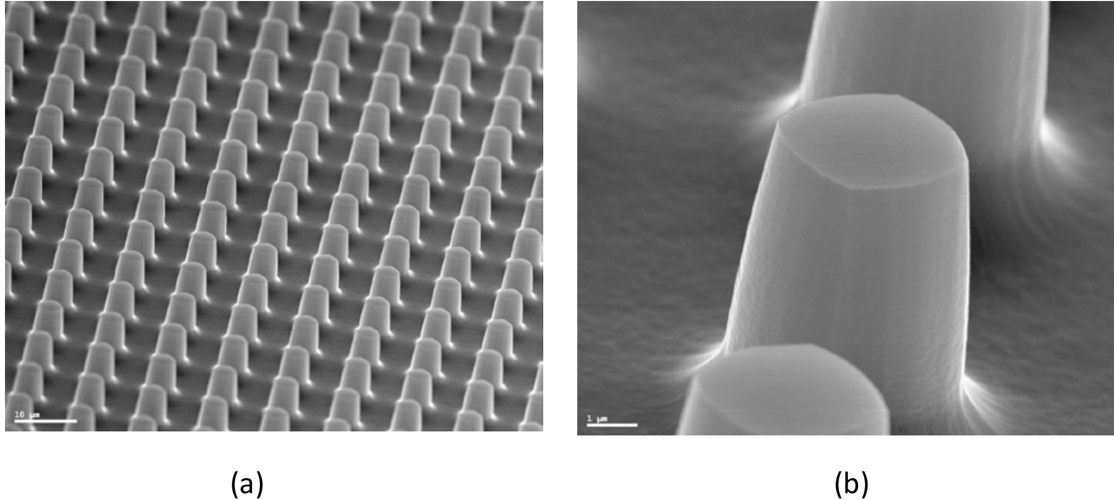


Figure 3.8: SEM image of DRIE Si pillar with remaining photoresist.

After the DRIE etch step, the photoresist removal was straightforward and was followed by the wet chemical etch step. The purpose of this step was to produce features with a positively sloped sidewall from the vertical sidewalls obtained by DRIE, requiring some directionality in the etch. Process development was focused on slight dilution of HF and HNO_3 mixtures in H_2O where Si etching changes from isotropic to anisotropic, as shown in Figure 2.11 and reported in Schwartz et Al. 1976 [81]. Figure 3.9 shows SEM images of post-wet etched pillars. The sample was first etched in a 1:4 solution of HF:HNO_3 for 3 s. It was then dipped for 6 s in a 1:4 solution of HF:HNO_3 diluted by 25% with H_2O. The resulting pillars were 6.1 μm tall with a sidewall angle of 82°. As predicted, there appears to be some directionality in the etching process as the tops of the pillars are slightly squared-off due to the use of the diluted etchant. Upon closer inspection of the pillar sidewalls, faint remnants of scalloping caused by the DRIE step appear. While these are visible, the overall sidewall morphology is smooth.



(a) (b)

Figure 3.9: SEM images of Si pillars after DRIE and $HF:HNO_3:H_2O$ wet etching: (a) an array of 10 µm pitch features and (b) close-up of a single pillar.

Figure 3.10 shows SEM images of the post-wet etched pillars. In this case, the pillars were dipped in the 1:4 solution of $HF:HNO_3$ for 1 s and the diluted solution for 6 s. The resulting pillars are 5.7 µm tall with a sidewall angle of 85°. In this case, the pillars have sharp vertical edges. This directionality is expected as the sample was immersed in the diluted solution for a majority of the time. Specifically, it appears the diluted solution preferentially etches the {110} planes of Si over the {100} planes as the pillars etched further horizontally than vertically, where the vertical sides of the pillars are the {110} set of planes based on alignment to the primary flat of the Si wafer. Good lateral thickness uniformities were achieved with this two-step etching process. A thickness uniformity under 100 nm, as measured from SEM imagery, was obtained across 1 x 1 cm patterns for the roughly 6 µm tall Si pillars. Such uniformity is critical in the embossing process as the yield of successfully realized features drops as uniformity decreases.

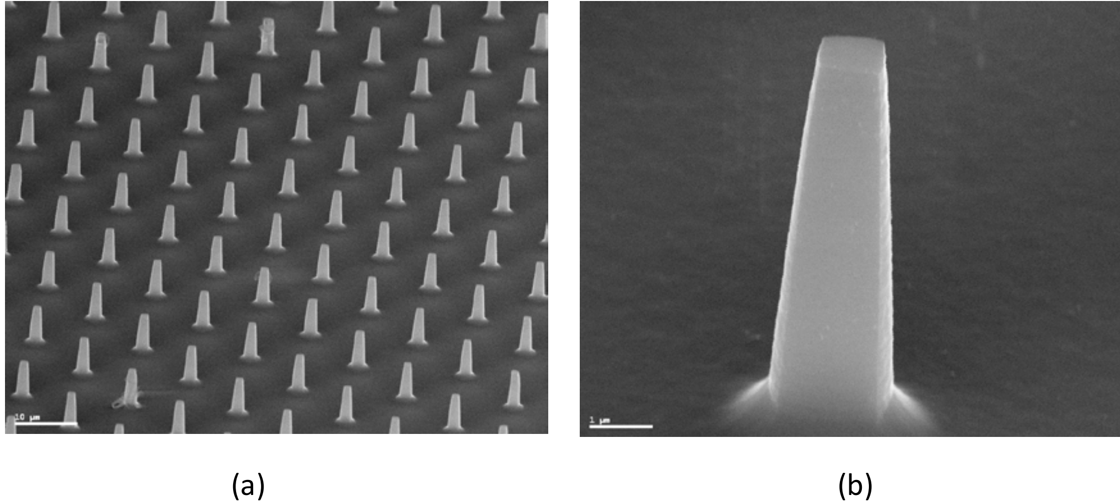


Figure 3.10: SEM images of Si pillars after DRIE and diluted $HF:HNO_3:H_2O$ wet etching: (a) an array of 6 μm pitch features and (b) close-up of a single pillar.

Development of a plasma-only Si etch that achieved features with a positive sidewall angle began with development of an SF_6/O_2 process. Prior to etching, samples were patterned with AZ 9260 photoresist with a 5.0 μm thickness as previously discussed. Patterning with this photoresist was relatively straightforward; however, increased diffraction effects and inconsistent sample to mask contact tended to round and alter the shape of features. Etching recipes and results using the SF_6/O_2 gas mixture are shown in Table 3.4. Prior to the recipes listed, several runs were attempted using only these two gases. After initial ignition of a plasma, the RF bias across the plates of the ICP system quickly fell to zero, causing the plasma to extinguish. This was due to a nearly neutral balance of positive and negative ions in the plasma. Ar was added to the SF_6/O_2 mixture to increase the number of positive ions to maintain the plasma. The addition of this gas increased the physical bombardment of the Si while adding no chemical component to the etch due to its inertness.

Recipe	1	2	3	4	**5**
SF_6 Flow (sccm)	32 (50%)	15 (50%)	45 (69%)	38 (58%)	**52 (80%)**
O_2 Flow (sccm)	32 (50%)	15 (50%)	20 (31%)	27 (32%)	**13 (20%)**
Ar Flow (sccm)	30	10	30	30	**30**
Operating Pressure (mTorr)	100	10	100	100	**100**
ICP Power (W)	500	500	500	500	**500**
RF Power (W)	200	200	200	200	**200**
Time (min)	12	12	12	20	**12**
Sidewall Angle (deg)	51	49	55	49	**87**
Etch Depth (μm)	1.0	Grass	0.75	1.7	**8.0**

Table 3.4: Key recipes used for plasma etching of Si with SF_6/O_2 gas mixtures.

Once a stable plasma was achieved, the recipes listed in Table 3.4 were attempted with SEM images of several results shown in Figure 3.11. Of the various parameters altered, two appeared to have the largest effect on the resulting Si pillars. The RF bias was reduced in Recipe #2 from 200 W to 30 W. This was the only sample that did not have a specular reflection when removed from the chamber and appeared discolored to the naked eye. An SEM image taken of the sample, shown in Figure 3.11a, reveals a large amount of roughness on the etched surface. The formation of micrograss on Si is typically due to a plasma etching process with a large physical sputtering component, such as with an Ar plasma. The sputtered components are then reactive and tend to redeposit on the sample forming micrograss. Reduction of these features can be accomplished with the addition of a chemical etching component, including compound containing F, that bind to the sputtered Si and volatilize it [120, 121].

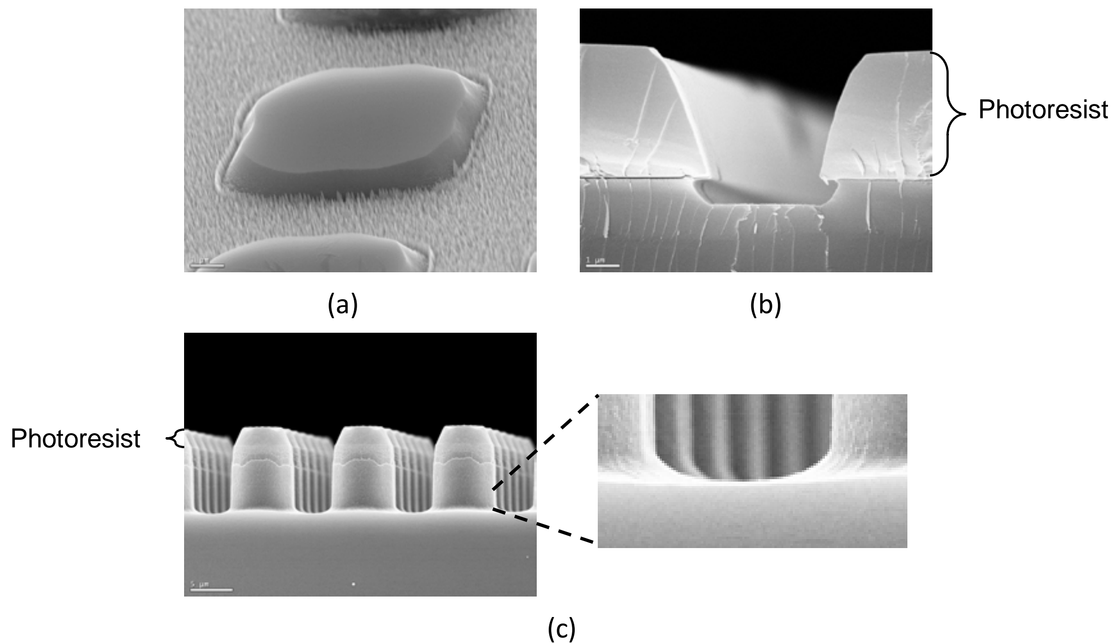


Figure 3.11: SEM images of Si plasma etched by SF_6/O_2: (a) recipe #2 showing micrograss, (b) recipe #3 and (c) recipe #5 with a close-up of the trench profile.

This was not the case for this sample, where a brown haze appeared on the sample after the etching process. This haze could be easily smeared, and the sample had a faint odor of sulfur. This evidence points to the deposition of S-based features on the Si surface during the etch that were not being sputtered away due to the low amount of RF bias used for the run. Larger values of bias were later used to avoid the appearance of such features. The second parameter that affected the Si pillars was the concentration of SF_6 relative to O_2. Recipes #1 and #3-5 had a lower SF_6/O_2 ratio than Recipe #2. While positively angled, the sidewall angle of pillars from these recipes was significantly lower to the point that there was too much of a horizontal component to be useful. Figure 3.11b shows a feature etched using Recipe #3. Recipe #2, however, had a desirable sidewall angle with a 4/1 SF_6/O_2 ratio. The increased etch rate was likely due to the larger amount of SF_6 in the plasma, providing an increased chemical etch. Figure 3.11c shows features etched by this

recipe with photoresist remaining. Faceting of the photoresist is apparent and resulted in a slight inward etching of the top third of the pillars. A close up of the etched Si profile at the bottom of the pillars shows a convex shape with respect to the pillar tops. This shape is not entirely desirable since the resulting imprinted Teflon surface will have a convex shape between trenches which would require In bumps to be grown above this surface, increasing the likelihood of shorting. This issue will be discussed further in the next chapter.

A plasma-only Si etch composed only of CHF_3 was developed in parallel to the SF_6/O_2 process. Previous results [84] had shown an ability to control sidewall angle with proper adjustment of ICP parameters. Initial patterning of samples with 5µm thick AZ 9260 photoresist was not sufficient because the etch selectivity was too low. This resulted in complete removal of the photoresist before Si pillars were etched deep enough. Instead, the AZ 9260 process shown in Table 2.3 was altered to produce an 8 µm thick resist after development. While the photoresist proved to be thick enough, the increased thickness made it more difficult to pattern samples with small pitch features. Several hardmasks, including Ni/Ti/Si and Al/Si with thicknesses up to 1 µm, were attempted as an alternative to processing with thick photoresist but were completely removed before the end of the CHF_3 etching step. The F radicals in the plasma etched these metals too aggressively.

After patterning Si samples with a thicker layer of AZ 9260 photoresist, CHF_3 etching processes were attempted. Table 3.5 summarizes several of the endeavored recipes.

Recipe	1	2	3	**4**
CHF3 Flow (sccm)	25 (100%)	25 (100%)	25 (71%)	**25 (71%)**
Ar Flow (sccm)	0 (0%)	0 (0%)	10 (29%)	**10 (29%)**
Operating Pressure (mTorr)	15	15	15	**15**
ICP Power (W)	600	600	600	**1200**
RF Power (W)	150	75	150	**300**
Time (min)	20	20	20	**20**
Sidewall Angle (deg)	72	55	77	**79**
Etch Depth (μm)	0.2	0.1	0.4	**1.9**

Recipe	5	6	7	8
CHF3 Flow (sccm)	10 (40%)	10 (40%)	25 (71%)	25 (100%)
Ar Flow (sccm)	15 (60%)	15 (60%)	10 (29%)	0 (0%)
Operating Pressure (mTorr)	15	3	30	15
ICP Power (W)	1200	1200	1200	1200
RF Power (W)	300	300	300	300
Time (min)	20	20	20	20
Sidewall Angle (deg)	79	87	81	77
Etch Depth (μm)	2.1	2.7	1.7	0.8

Table 3.5: Key recipes used for plasma etching of Si with CHF_3.

Alteration of RF bias, as performed in Recipes #1 and #2 ended with major changes in the resulting etch. A 50% reduction in RF power resulted in a reduced sidewall angle from 72° down to 55°, along with a 50% reduction in etch thickness. Because the CHF_3 plasma is highly reactive, momentum imparted to the ions with the addition of RF bias acts as main mechanism for adding a physical component to the etch process, explaining the large difference in results. In both cases, however, the etch rate was lower than desired, where Recipe #1 resulted in an etch rate of .6 μm/hr. Ar was added for Recipe #3 to increase the physical attack component of the etch process and resulted in a 1.2 μm/hr etch rate. Additionally, the sidewall angle increased to 77° reflecting this change. While the angle obtained was desirable, the etch rate remained too slow for a feasible process.

Recipe #4 doubled both the RF and ICP power to address the issue of increasing the momentum of ion bombardment and plasma density. These adjustments were successful, as the etch rate increased to a feasible 5.7 μm/hr with a desirable sidewall angle of 79°. Figure 3.12 shows SEM images of features etched using this recipe with some photoresist residue remaining from a non-optimal stripping process. In the angled view shown in Figure 3.12a, some curtaining is evident though the sidewalls are relatively smooth. The cross-sectional view shows a convex trench profile with respect to the top surface. Trenching is responsible for the increased etch rate at the corners, an effect that is caused by the reflection of ions that graze the sidewall of the feature and are then reflected towards the corners [122]. Typically this is a negative effect associated with plasma etching; however, this effect may be useful for the imprinting step for this application. Unlike the pillars obtained with the SF_6/O_2 plasma, the profile imprinted in the Teflon AF layer would be less likely to short as the highest point in the profile would be at the interface with bumps. Recipes #5-8 were attempted to further determine the effects of changing the plasma parameters on the final etched profile. Of particular interest was Recipe #6, which reduced the operating pressure down to 3 mTorr and raised the ratio of Ar to CHF_3 in the plasma. The resulting etch proved to be the fastest at 8.1 μm/hr and had the most anisotropic sidewalls with an 87°. Both the increased physical nature of the process and increased mean free path due to lower operating pressure produced a more anisotropic etch.

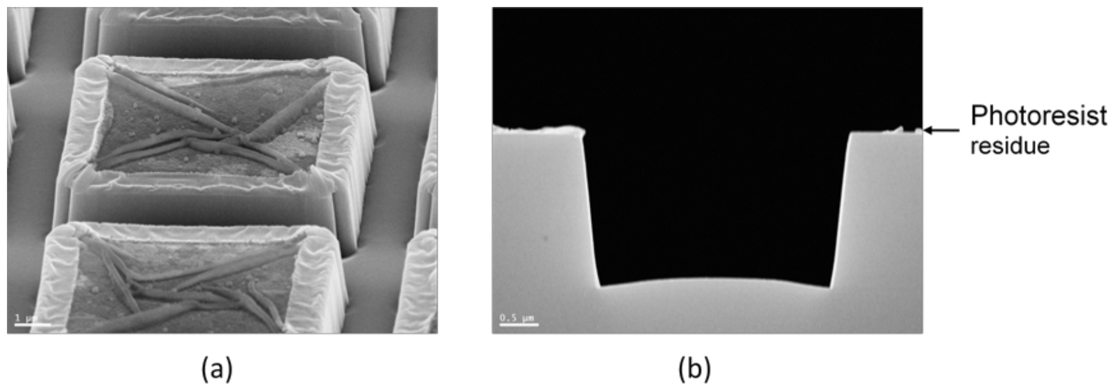
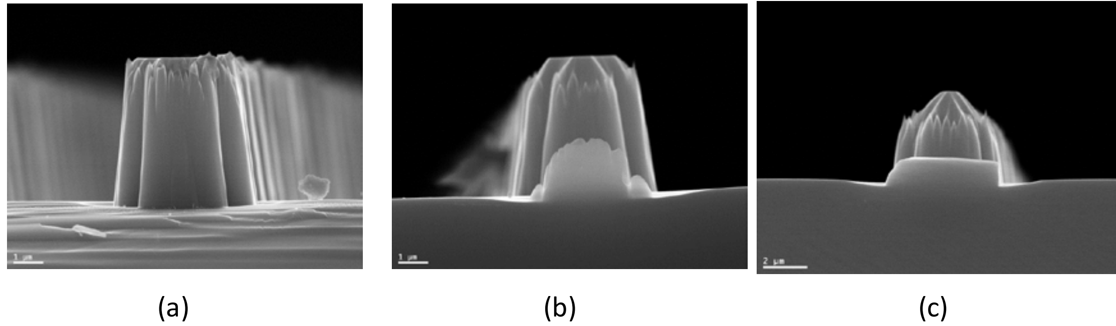


Figure 3.12: SEM images of Si features etched with recipe #4, (a) angled view with photoresist residue visible and (b) cross-sectional view showing trench profile and angled sidewall.

While Recipe #4 provided desirable characteristics for this application, the pillar thickness achieved with the recipe was too small. Longer etches were attempted to obtain the desired thickness with results shown in Figure 3.13. Etch times for Figure 3.13a-c were 70 min, 80 min, 95 min, respectively. For each process the photoresist was stripped completely by the end of the run. Larger amounts of faceting appear in each successive run due to increased sputter etch rates of Si at an incidence angle that is off normal [123]. While thicker photoresist helps to avoid such features, regulating the faceting provides another parameter by which to control sidewall angle. Angles of 81°, 74°, and 68° were obtained when measuring from the edge of the base of the pillar to the top of the facet. This parameter was used for repeatedly producing Si stamps with different sidewall angles.



(a) (b) (c)

Figure 3.13: Si pillars plasma etched with CHF_3 showing increased faceting with increased process time: (a) 70 min, (b) 80 min and (c) 95 min.

3.3.2 Imprinting the Template Wafer

Initial fabrication steps to realize the template wafer followed Section 3.2.1, which resulted in an unpatterned Teflon AF/Ni/Ti/Si sample. Upon completion of the Si stamp, the imprinting process was performed, as outlined in Figure 2.4. This process followed the one previously described in the Experimental Methods chapter. Initial experimentation used Si stamps with pillars that were substantially thicker than the Teflon AF layer. The resulting morphology of the amorphous fluoropolymer was poor, as shown in Figure 3.14. These SEM images show an inconsistent top surface with regions rising adjacent to where the pillars imprinted rising 7 μm above the surrounding areas. Liquid Teflon AF, while raised above its T_g, appears to have crept up the Si pillars during the imprinting step. After several failed attempts using relatively thick Si pillars, Teflon AF imprinting was attempted with pillars that had a comparable thickness to within 1 μm. This technique allowed for planarization of the amorphous fluoropolymer by forcing the stamp down onto it, assuming planarity of the stamp and even force during imprinting. This process also reduced the need for precise thickness control of the Teflon AF layer as

long as it filled the mold during imprinting. Any excess would be pushed past the border of the Si stamp, where it did not affect the imprinted layer.

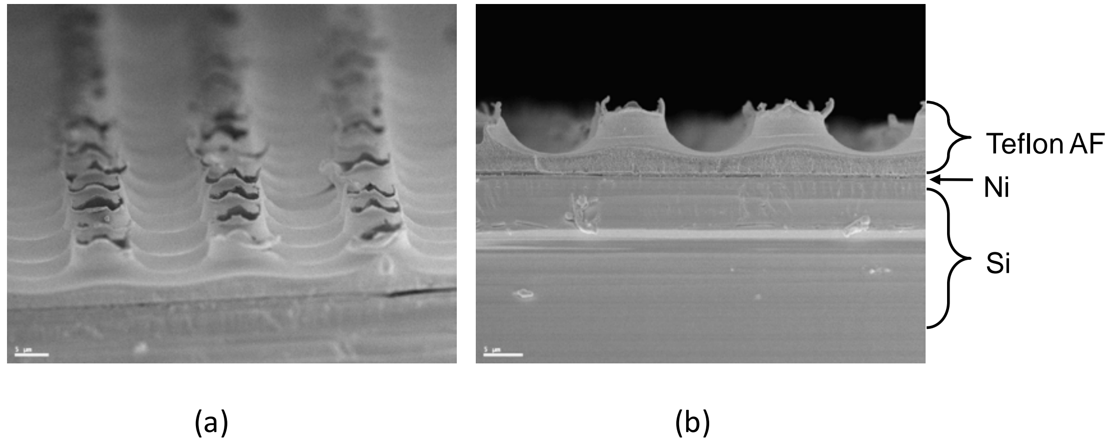


Figure 3.14: Initial attempt at imprinting Teflon AF with thick Si pillars: (a) angled view and (b) cross-sectional view.

SEM images of imprinted fluoropolymer on Ni are shown in Fig. 3.15. Each was obtained from Si stamps etched with the DRIE/chemical etch process. Figure 3.15a is an SEM image of a via imprinted in 5.7 μm thick fluoropolymer. The morphology of the via surface is smooth, indicating the Si stamp released completely from the fluoropolymer while the roughness that appears at the front surface of the fluoropolymer is due to cleaving of the sample. Excess fluoropolymer at the bottom of the via is imperceptible in this image; however, interference fringes appear when focused at the bottom of the vias using optical microscopy, indicating a thin layer of fluoropolymer remains on the Ni surface. Failed attempts to electroplate In directly after the imprinting step without an Ar RIE step confirm the presence of this layer. An area of imprinted vias in 6.0 μm thick fluoropolymer at a 12 μm pitch and a 6 μm pitch are shown in Figures 3.15b-c, respectively.

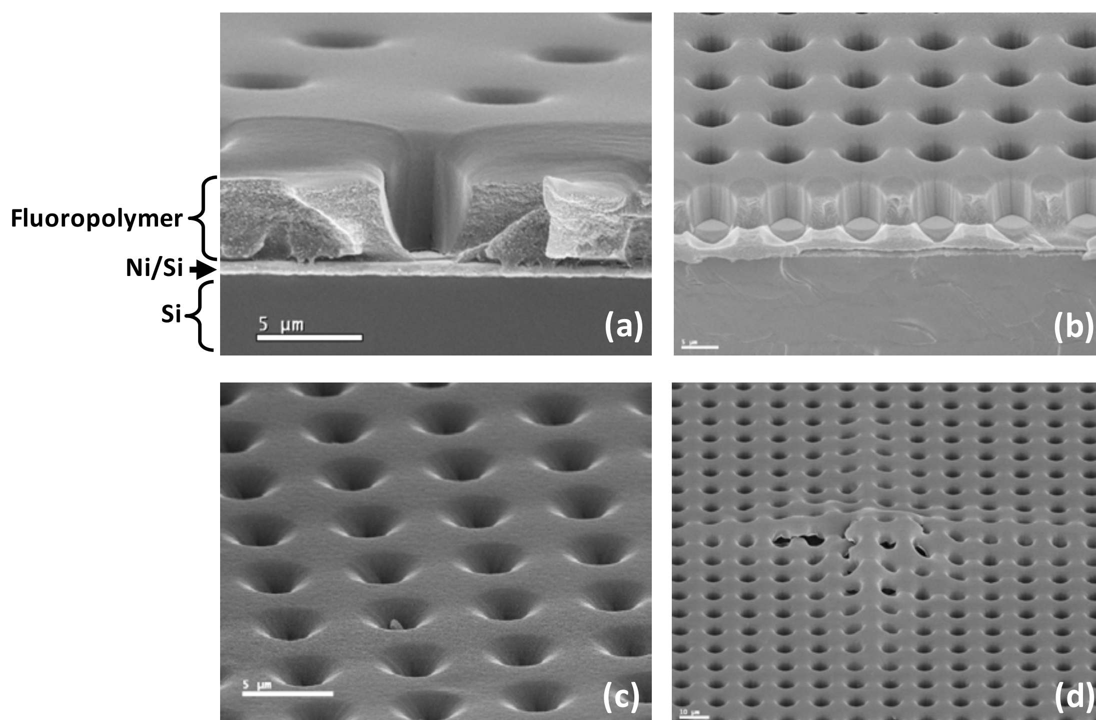


Figure 3.15: SEM images of vias embossed into the fluoropolymer: (a) cross-section of a via, (b) 12 μm pitch vias, (c) 6 μm vias and (d) vias where the fluoropolymer pulled away from the Ni surface.

This angled SEM image shows the consistency of the imprinting process over several vias. The surface of the fluoropolymer once again appears smooth, and each of the exposed vias was patterned almost completely down to the Ni surface. No cracking or large-scale delamination of the fluoropolymer from the Ni film was observed which indicates that differences in the thermal expansion coefficient between the fluoropolymer and the Si substrate and Si stamp were small enough to avoid such defects in the samples studied. While these results were encouraging, the imprinted features were not entirely uniform. Figure 3.15d shows a defective region in the fluoropolymer. In this image, it appears that the fluoropolymer pulled away from the Ni surface. The Si stamp has some adhesion to the fluoropolymer after the imprinting step. It is likely there was locally

insufficient adhesion between the Ni and fluoropolymer, causing this defect to form when the Si stamp was pulled away. As pitch is reduced, the contact area between the Si stamp and fluoropolymer increases resulting in additional adhesion between the two; however, these defects were observed at all pitches attempted. Additionally, no difficulty was encountered in the separation of the Si stamp from the fluoropolymer as the process was scaled down to a 6 μm pitch; therefore, scaling effects due to adhesion between the Si stamp and fluoropolymer were not observed in the range of pitches studied. In order to increase adhesion between the Ni and fluoropolymer interface, a preparation step was inserted into the process. The native oxide found on the Ni was stripped off using a 10 s dip in 15% HCl in DI water. This was followed by a rinse in DI water, an N_2 blow drying step, and a 1 min 100 °C bake on a hotplate to ensure all water was removed from the surface. Figure 3.16 shows the result of imprinted fluoropolymer processed on plasma treated Ni. Optical microscopy was used to image roughly 1400 vias imprinted in 5.7μm thick fluoropolymer at a 12 μm pitch. No evidence of defects or pulling away from the Ni surface was observed, as shown in Figure 3.16a. An SEM image of the same vias at higher magnification is shown in Figure 3.16b. This level of uniformity was achieved for both smaller and larger patterns by area, ranging from .5 x .5 cm up to 1 x 1cm.

Imprinting of template wafers was also demonstrated using plasma-only etching of the Si stamps. Figure 3.17 shows the results of an imprinted wafer. Like the previous results, the surface morphology closely followed that of the Si stamp, resulting in raised regions near the trenches due to the trenching of the pillar etch process. As previously stated, it is anticipated that such features will positively affect the In transfer process. Blowout of features in the Teflon AF appeared in the cross-sectioned sample due to

deformation of its front surface because the material tended to tear when cleaved. Closer inspection revealed trench morphologies that mirrored the Si stamp.

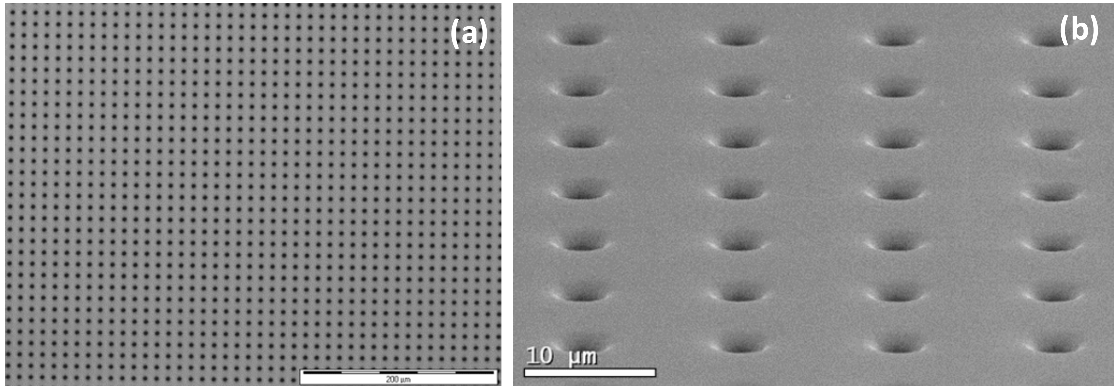


Figure 3.16: Images of defect-free embossing of the fluoropolymer on a roughened Ni surface: (a) low-magnification optical microscopy and (b) higher magnification SEM image of the same vias.

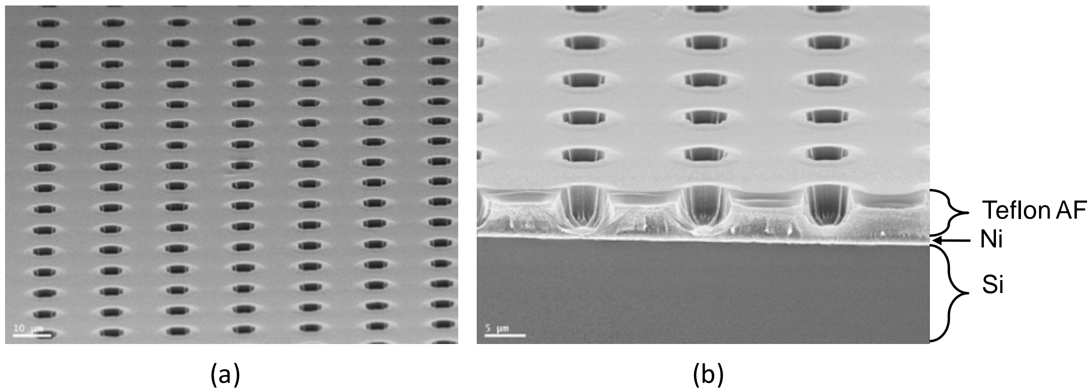


Figure 3.17: SEM images of Teflon AF imprinted with CHF_3-etched Si pillars: (a) angled view and (b) angled view of a cleaved piece.

After patterning the template wafers with the imprinting step, trench bottoms were cleared using the previously described RIE system which exposed the Ni seed layer below for In bump electroplating. Initially, the 150 W, 100 mTorr Ar plasma process was used to blanket etch the samples for 1 min. In most cases, the fringing effects at the

trench bottoms would be cleared, though this was not always the case. Predicting the etch time was possible, however, because the imprinted Teflon AF had interference fringes across it similar to the spun on layer. Prediction of this was important since under-etching would result in unexposed Ni at trench bottoms while over-etching would reduce the entire Teflon AF layer thickness. Equation 3.1 was still valid in determining that each fringe represented a thickness change of 100nm. The appearance of fringing of the imprinted layer was due to nonplanarities in Teflon layer. The most likely cause of such imperfections was particles that ended up wedged between the Si stamp and template wafer during imprinting. Nonuniform Si pillars would have a similar effect, though in nearly all samples, parallel fringes appeared on the imprinted layer indicative of wedging. While most samples contained less than 5 fringes, with as little as 1 observed, a highly wedged sample with 15 fringes was used to determine the time needed to clear each fringe. After running the Ar plasma several times for 1 min, it was found that 1.5 fringes/min were cleared by the process. This process was more useful than attempting to determine an etch rate because the RIE process tended to roughen the surface of the Teflon AF, making a quantitative measurement difficult. After the RIE clearing step, template wafer fabrication was complete.

Chapter 4

Electroplating and Transfer of In Bumps

4.1 Introduction

Upon completion of the template wafer fabrication, two steps remain in the process: electroplating of In to fill the features patterned in the Teflon AF, and the transfer of the bumps to a mechanical ROIC. The first part of this chapter describes the optimization of In electroplating onto dummy photoresist/Ni/Ti/Si samples before any attempts were made on actual template wafers. Once optimized, the electroplating process is demonstrated on the template wafers. Finally, the transfer of bumps to a dummy ROIC is shown along with a determination of the key parameters required to achieve good transfer.

4.2 In Electroplating

4.2.1 Initial Experimentation

Before the ECSI IKO electroplating system was obtained, beaker level experiments were performed to begin optimization of the In electroplating. The setup consisted of a polymethyl methacrylate (PMMA) tank partially filled with an indium sulfamate-based plating solution. A DC power supply with a 1 A upper limit was used

where current was controlled. Crude pulse plating was accomplished with a function generator providing square pulses to a single pole single throw relay, across which the DC power supply was connected. A 3" In sputtering target was connected as the anode with the sample attached as the cathode. Both a stir bar and a sparging tube for N_2 bubbling were added to improve the mass transport of the setup. 8 μm thick AZ 9260 and 4 μm thick AZ 4330 patterns on Ni/Ti/Si wafers, fabricated using techniques previously described, were used for plating experiments. The thinner patterns allowed for definition of slightly finer features while thicker patterns provided aspect ratios similar to the actual template wafers.

Prior to In plating of patterned photoresist features, attempts were made on bare Ni/Ti/Si tabs to determine a process that consistently plated In across the surface. Initially, samples were dunked for 3 min in a commercially available Ni pickling solution containing $NaHSO_4$ and $K_2Cr_2O_7$ to strip the oxide from the sample surface. After this step, samples were rinsed in DI water and immediately placed in the electroplating bath before re-oxidation occurred. Plating was then initiated with current densities maintained between the optimal specified values of 108 and 216 A/m^2. While some In plated on the surface of the tab, its morphology was poor with large sections of the sample remaining bare. After several failed attempts, an initial 1 s strike was added at the beginning of the plating process that raised the current density above 500 A/m^2. This current striking process improves lateral uniformity of the In by increasing its covering power or ability to coat the entire surface of a sample [124]. It also yields a high quality layer but plates too slowly for consideration in most applications; therefore, plating progresses at standard current densities. While the reduced plating rate does not present a problem in

this application, the high current density caused issues when features were plated in photoresist and Teflon AF. Such difficulties will be discussed in the sections to follow. In addition to this strike step, sparging was found to improve the uniformity of plated In. With no sparging, pin holes were observed in the In layers due to the formation of H_2 bubbles that adhered to the sample surface; including sparging removed the pin holes by sweeping the bubbles from the surface. Finally, it was found that the acidic indium sulfamate plating bath was sufficient to strip the oxide from the Ni surface. Once discovered, samples were held idly in the plating bath for 5 min prior to adding current. This step precluded use of the pickling solution eliminating the highly toxic $K_2Cr_2O_7$ from the process.

Initial In plating experiments of patterned photoresist/Ni/Ti/Si extended from what was learned on the bare metal tabs. Several attempts using the procedures described above led to regions of features that did not plate caused by incomplete wetting of the Ni seed layer during the plating process. As the aspect ratio of features increased, pockets of air remained trapped in the photoresist features, cutting off access to the plating solution. These air pockets were especially troubling during the In striking step, which was added to improve the uniformity of the initial In layer. While the use of surfactants could have removed this problem, a simple step was added prior to immersing the sample in the electroplating bath. Instead, simply spraying the sample surface with DI water for 3 minutes, followed by immediate immersion in the plating solution removed the air pockets and resulted in the plating of all features in the photoresist.

The effects of varying DC current on the electroplated In were explored using the basic plating setup with photoresist patterns. Attempts at plating between 110 and 190

A/m^2 produced similar results. Above this current density, near the upper limit of the 216 A/m^2 suggested for the plating solution, the photoresist began to pull from the sample with plated In filling in, as shown in Figure 4.1. This SEM image shows a small region of photoresist that remained on the sample surrounded by plated In where the photoresist had been delaminated. This was caused by underplating of the photoresist due to lateral growth of In during the electroplating process. This lateral growth is a consequence of the migration of In ions through the interface between the photoresist and Ni seed layer, resulting in plating that creates a wedge between the two layers. The rate of underplating can be reduced faster than the vertical plating rate by reducing current density [125, 126]. The reduced vertical plating rate is not desirable for high throughput applications plating large parts but is acceptable for this application. No evidence of underplating during the short 1 s In strike was observed; therefore, this process continued to be used to obtain high lateral uniformity of the initial plating layer.

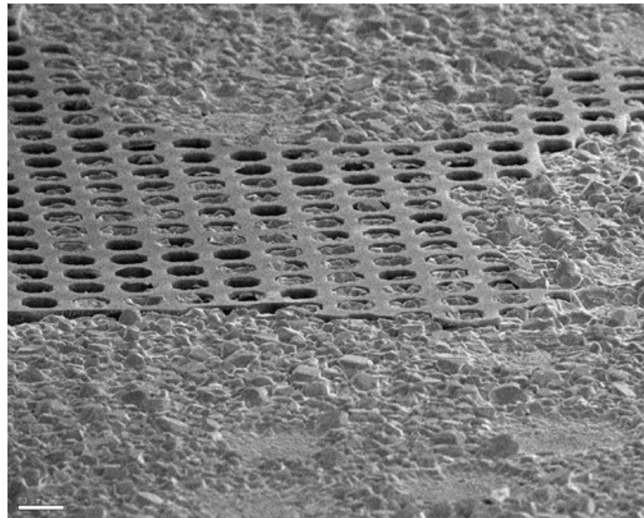


Figure 4.1: SEM image of In underplating a photoresist pattern.

Basic pulse electroplating was attempted using the function generator and relay in conjunction with the DC power supply. The switching time of the relay was 2 ms limiting the pulse frequency. Plating using this technique has been shown to allow for control over a variety of characteristics, including crystallinity and alloy composition, for many different materials systems [127-129]. It has also been shown to reduce the grain size of the plated material, a key parameter for this application. Several mechanisms of the pulse improve the qualities of the plated layer. First, a negative bias forms around the sample when plating, restricting ions from impinging on it. The off portion of the pulse allows for discharge of this layer, allowing ions to flow more freely to the sample. Additionally, localized variations of current density on the sample produce an uneven distribution of ions available to plate the part. Regions of higher current density deplete the plating solution more than lower ones. The off portion of the pulse allows for migration of ions in the solution, evening their distribution and resulting in improved plating qualities [43]. These benefits allow for pulses with a significantly higher amplitude than would be feasible for DC process, producing features with similar qualities to those of the current strike. While a variety of pulse plating experiments were attempted using this setup, discussion will be limited to its effects on In grain size. A detailed set of experiments accompanied by discussion will be included in the next section. Figure 4.2 shows optical microscopy images comparing DC and pulse plating. Figure 4.2a shows a 500x image of a 200 μm feature plated for 4 min with a current density of 110 A/m^2. Figure 4.2b shows a similar feature that was pulse plated with the following parameters: 12 min plating time, 50 ms period, 5 % duty cycle, and a 60 mA amplitude giving a 270 A/m^2 current density. The In thickness for both samples was roughly 8.5 μm. Based on the images, it is

clear that pulse plating reduced the In grain size. The dimensions of the larger grains in each image were measured. Grains of up to 9.0 μm were measured for the DC plated layer, while they were only 3.5 μm for the pulse plated layer. This reduction follows what was described in the literature for other material; however, it should be noted that the grains are still large compared to other electroplated metals. In addition to the grain size reduction, pulse plating resulted in faster deposition when comparing average current of the pulse to DC plating. The DC sample plated In at a 2.1 μm/min rate at 110 A/m^2 while the pulsed sample plated at a rate of .71 μm/min at an average current density of 13.5 A/m^2. When normalized by current density, the pulsed sample plated 2.8 times faster than the DC sample. The increased normalized rate shows the importance of charge dissipation and ion replenishment near the surface of the sample during the off portion of the current pulse. Another important observation of the pulse plating process was that no underplating of the photoresist was evident even with the large amplitude of the pulse. In fact, pulses with current densities as high as 1350 A/m^2 were attempted with no underplating. While the amplitude of such pulses was high compared to DC plating, the average current density of the entire on/off cycle was still well below the limit for where underplating dominated. Further experimentation held the average current density for any pulse plating process below these limits.

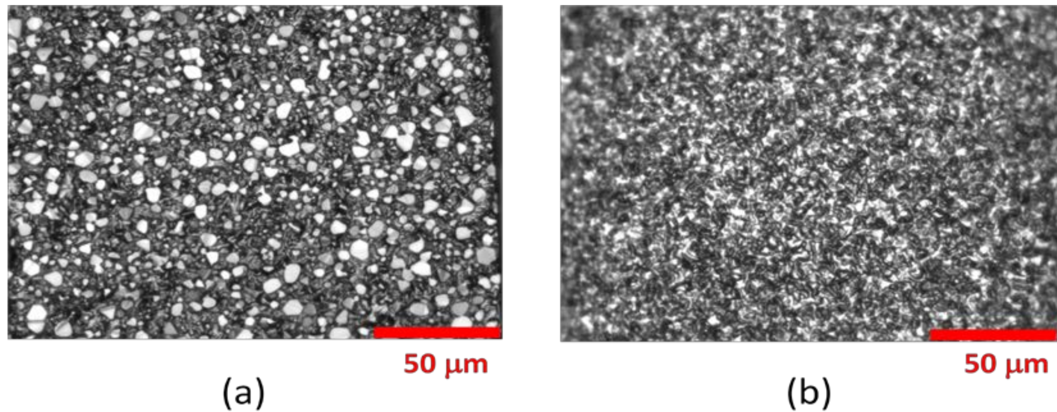


Figure 4.2: Optical microscopy images of electroplated In: (a) DC plated and (b) Pulse plated.

4.2.2 Optimization of Plating Parameters

The basic In electroplating setup used in the previous section was useful in determining several key parameters for the process including: the use of a fast, high-current strike to put down a thin, high quality layer that coated the entire sample, proper pretreatment steps to ensure all features plated, limits on current density to avoid underplating, and the use of pulse plating to reduce In grain size. This knowledge provided an estimate of what the optimal plating conditions are for this process. The ECSI IKO system, described in Chapter 2, was used to fine tune the process. The improved 10 μs switching time of the dedicated pulse power supply, along with improved mass transport and design of the system, allowed for better control of plated layers. The focus of experimentation with this system was to optimize lateral thickness uniformity of the bumps while attempting to achieve as flat a bump as possible. These characteristics are critical for consistent bump transfer.

Standardized photoresist/Ni/Ti/Si samples were used for the optimization process made up of 8 μm thick AZ 9260 on the Ni seed layer patterned by the previously described process. This pattern consisted of a 1 x 1 cm array of 15 μm pitch, nominally 5 μm wide square features. SEM characterization of the process consistently showed that the features with a 6.5 μm dimension on a side were opened in the photoresist down to the Ni seed layer, exposing a total of .19 cm^2 of the Ni, for current density calculations. The initial set of experiments focused on attempting all 8 permutations of low and high values for each of three parameters of the plating process: the current density applied to the sample, the period of each pulse, and the duty cycle of the pulse. The 1 s current strike was included for each process prior to running the pulse process. After plating, the photoresist was stripped, and a set of SEM images was taken uniformly across the sample, with the location of the single point contact to the power supply noted as shown in Figure 4.3. The height of the bumps was measured, and the shape of the bump tops was noted as to whether they were concave, convex, or flat.

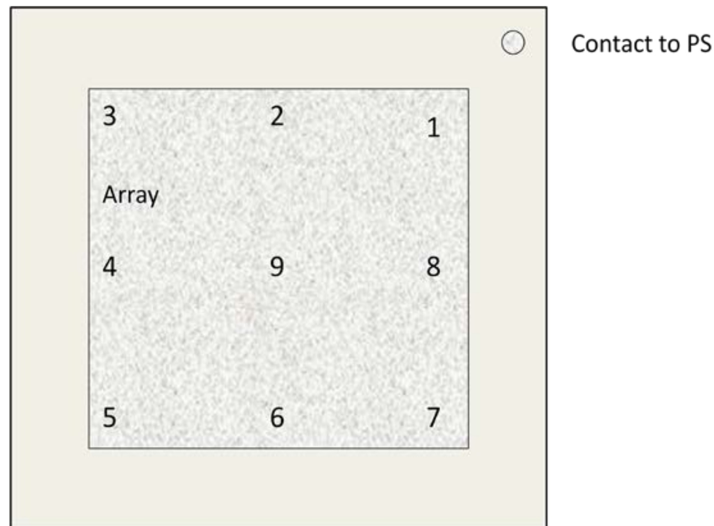


Figure 4.3: Illustration of standard samples for optimization of In electroplating showing the location of thickness measurements taken and electrical contact.

The parameters used for each recipe are summarized in Table 4.1, where high values for each parameter are denoted by green and low values by yellow. The Recipes #1, #2 and #4-6 each successfully plated the samples with no problems. Recipe #3 initially applied 200 mA of current to the sample but resulted in complete underplating of the photoresist. This value was dropped to 125 mA, and no underplating was observed. It is interesting that this recipe initially failed while Recipe #2 resulted in no underplating. Each of the first four recipes used a high current density pulse over an order of magnitude above the suggested DC current density. The small duty cycles used for Recipes #1 and #4 reduced the mean current density to under the 270 A/m^2, which was where underplating was observed using the rudimentary plating setup, so underplating was not expected. Recipe #2 and initial Recipe #3, however, each had large duty cycles, raising their mean current density to roughly 2100 A/m^2. The difference was that the period used for Recipe #2 was relatively short at 5 ms, while for initial Recipe #3 it was 100 ms. It therefore appears that the longer period allowed for the underplating to occur. This effect was not significant enough to cause underplating for Recipe #3 when current was adjusted to 125 mA where mean current density was still well above 270 A/m^2. For Recipes #7 and #8, no plating of In was evident. Each of these recipes had the same combination of low applied current and low duty cycle resulting in mean current densities of 17 A/m^2 which were well below the low end of optimal DC current density of 108 A/m^2. This low current did not impart enough energy into the system to allow for plating to occur.

Recipe	Pulse Current (mA)	Period (ms)	Duty Cycle (%)	Plate Time (s)	Peak Cur. Dens. (A/m^2)	Mean Cur. Dens. (A/m^2)
1	200	5	2	600	10526	211
2	200	5	20	35	10526	2105
3	125	100	20	35	6579	1316
4	200	100	2	600	10526	211
5	16	5	20	480	842	168
6	16	100	20	480	842	168
7	16	5	2	600	842	17
8	16	100	2	600	842	17

Table 4.1: Parameters used for optimization of In electroplating. Green boxes denote high values while yellow denotes low values.

After stripping the photoresist and measuring the In bump thicknesses at the 9 locations specified in Figure 4.3, several conclusions could be drawn. For each sample, the thinnest bumps at the corner occurred nearest to the electrical contact to the power supply, at Location 1. The ratio of the thickness of the bumps at this corner compared to the mean bump thickness measured as a function of applied current pulse is shown in Figure 4.4. It is apparent that the ratio drops as applied current increases, resulting in thinner bumps at Location 1. Based on Ohm's law, the increased current causes an increased voltage between the electrodes of the plating setup especially near the point contact to the sample. This larger voltage depletes the solution of In ions and produces an excess of electrons that reduce water into H_2. The result is a reduced plating thickness from that expected. Table 4.2 compares several statistics of the electroplated bumps.

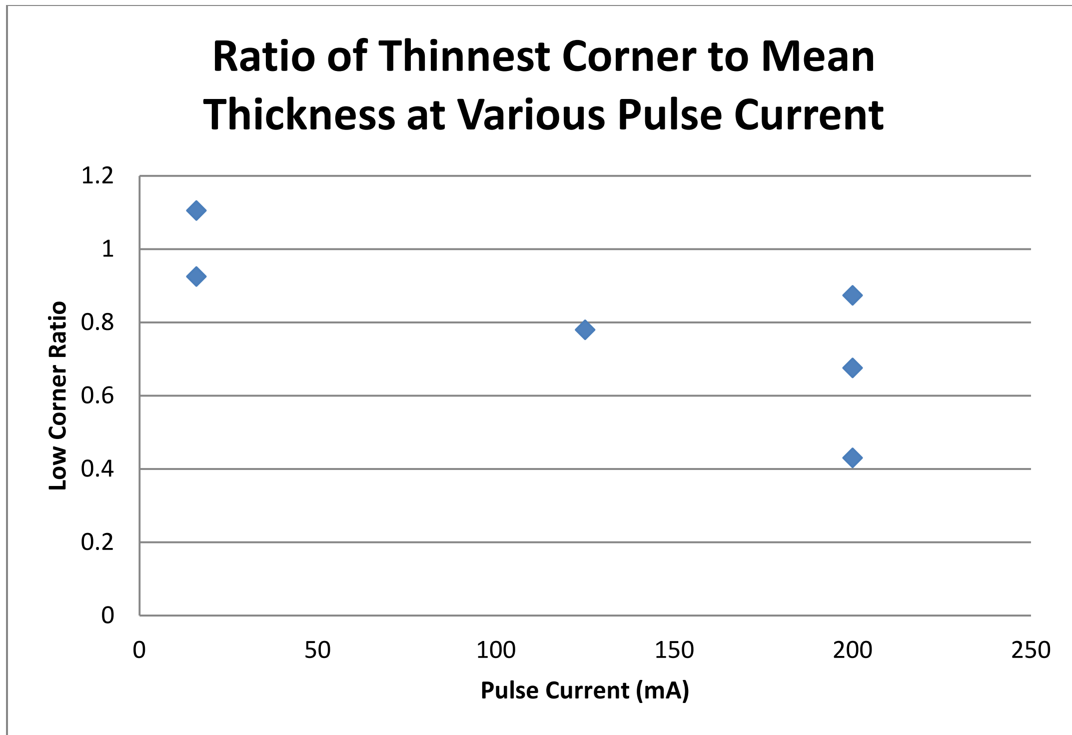


Figure 4.4: Graph displaying plating consistency of In bumps at the thinnest corner versus mean plating thickness.

Recipe	Mean Height (μm)	Normalized Std. Dev.	Mean Rate (μm/min)	Normalized Plating Rate (μm/(min*A/cm^2))
1	6.19	0.13	0.62	2.94E-03
2	4.25	0.37	7.28	3.46E-03
3	3.80	0.28	6.51	4.95E-03
4	5.62	0.43	0.56	2.67E-03
5	6.46	0.14	0.81	4.80E-03
6	4.69	0.23	0.59	3.48E-03
7	-	-	-	-
8	-	-	-	-

Table 4.2: Statistical results of the electroplated In experiments performed in Table 4.1.

The mean height of the bumps measured at each of the nine locations is shown for each recipe. The standard deviation of these measurements normalized by their mean value was listed, along with the mean plating rate for each recipe, and the normalized plating rate. The normalized plating rate is defined as the mean plating rate divided by the

average current supplied to the sample. This value allows for a direct comparison of how much In was plated for each recipe. With no secondary effects, this value would be the same for each recipe. Based on the data from both tables, the period of the pulse appeared to have little effect on the plating process outside of the earlier onset of underplating with longer periods previously discussed. Increased duty cycles, such as those for Recipes #2 and #3, resulted in increased normalized plating rates when compared to reduced duty cycles. The reduction in plating rates for shorter duty cycles was not due to nonideal pulses from the power supply. This was checked with an oscilloscope, and pulses down to .1 ms were nearly square. While some dependence on plating rate appeared, the rates for each recipe were all fast enough for this application. Recipes #1 and #5 appeared to produces the most consistent results based on their low values for normalized standard deviation. Choosing between these recipes for optimal plating of template wafers required a closer look at the bump morphologies. Figure 4.5 shows SEM images of In bumps plated by the two recipes. Bumps plated by Recipe #1, shown in Figure 4.5a, had an uneven top surface with taller regions typically protruding from the edges of the bumps. Increased plating at the edges of features has been found to be caused by a nonlinear diffusion rate of In ions that replenishes them faster than in the middle resulting in an enhanced plating rate at the edges [130]. Figure 4.5b shows In bumps plated by Recipe #5, which have consistently flatter tops than for Recipe #1. The reduced amplitude of current pulses for this recipe did not deplete the plating solution of ions near the sample as much as for Recipe #1. This reduced the requirement for ion replenishment; therefore, differences in ion diffusion rate between the middle and the

edges of the features do not result in large differences in plating rate. Because of this superior morphology, Recipe #5 was selected over Recipe #1.

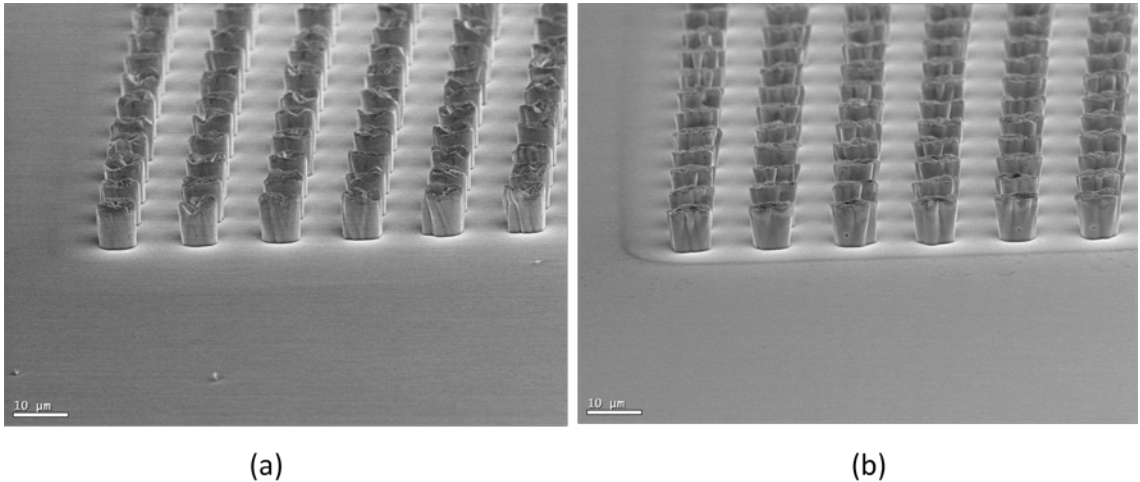


Figure 4.5: SEM images of electroplated In bumps: (a) Large amplitude process with nonuniform tops and (b) reduced amplitude process with improved uniformity.

While the morphology of plated In bumps was optimized, the bumps were relatively inconsistent from the highest corner to the middle of the array where nonuniformity as high as 30% was observed. The faster plating at the edges and corners of the array due to edge effects, however, was extremely localized. Figure 4.6 highlights this fact, where an SEM image was taken at the corner of a plated array. The photoresist was stripped away and shows bumps at the corner that overplated the resist, which is apparent by the lateral growth at the bump tops, appearing similar to a mushroom. This overgrowth disappears completely at four rows in from the corner and the bumps become more consistent going in from the corner. Based on this observation, another type of array was patterned in photoresist. This array consisted of 12 μm pitch bumps in a 720p format with an additional 600 μm of the same pattern surrounding the array. Fifteen equally

spaced measurements were made in a 3 x 5 fashion across the array and listed in Table 4.3. This data shows uniformity of plated bumps across the array to within 7%, demonstrating the localization of edge effects. The thinnest bumps occurred in the center of the array, showing that some drop off in plating rate still occurred away from the edges. This level of uniformity, however, was high enough to proceed with the transfer process. Based on these results, the pattern of the template wafer would be designed to extend past the dimensions of the array. The bumps in this extended region would be nonuniform due to edge effects, leaving relatively uniform bumps that would contact and transfer to the array.

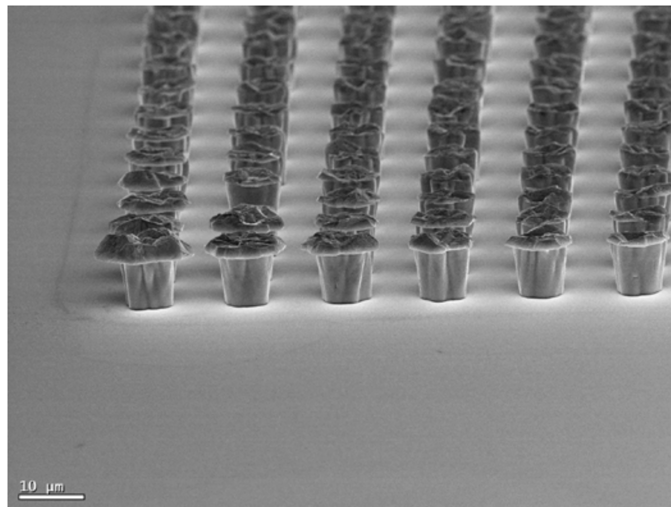


Figure 4.6: SEM image showing the rapid decay of electroplated In thickness from the corner of an array.

Measurement	Height (μm)	Measurement	Height (μm)	Measurement	Height (μm)
1	**10.3**	6	**10.3**	11	**10.3**
2	**10.2**	7	**10.1**	12	**10.3**
3	**10.2**	8	**9.8**	13	**10.3**
4	**10.4**	9	**9.8**	14	**10.3**
5	**10.5**	10	**10.4**	15	**10.4**

Table 4.3: Thickness measurements of electroplated In using optimized patterns across a 12μm pitch, 720p array.

4.2.3 Extension to In Plating of Teflon AF

Electroplating In into the Teflon AF features of template wafers was a straightforward extension of the results of the last section. The optimized recipe described above, with the same current density, was used to plate a variety of template wafers with pitches down to 6 μm. Additionally, the preparation of samples before plating followed that of the photoresist samples, including the DI water wetting step. Although Teflon AF is hydrophobic, voids in the plated pattern were uncommon. Several SEM images of such bumps are shown in Figure 4.7. Figure 4.7a shows a cross-sectional image of two bumps that nearly filled the template wafer. The roughness in the Teflon AF layer was due to the blanket RIE step to open the Ni seed layer. Limiting the amount of time needed for this step to limit roughness is of obvious importance. Preliminarily, however, adhesion between the two appears to be negligible. Figure 4.7b shows an angled view of the tops of two bumps that have separated from the Teflon AF template with no forces applied. Both layers appear to be intact, maintaining the small, high surface area features of the Teflon AF. Significant adhesion between the two layers would not allow for this type of separation.

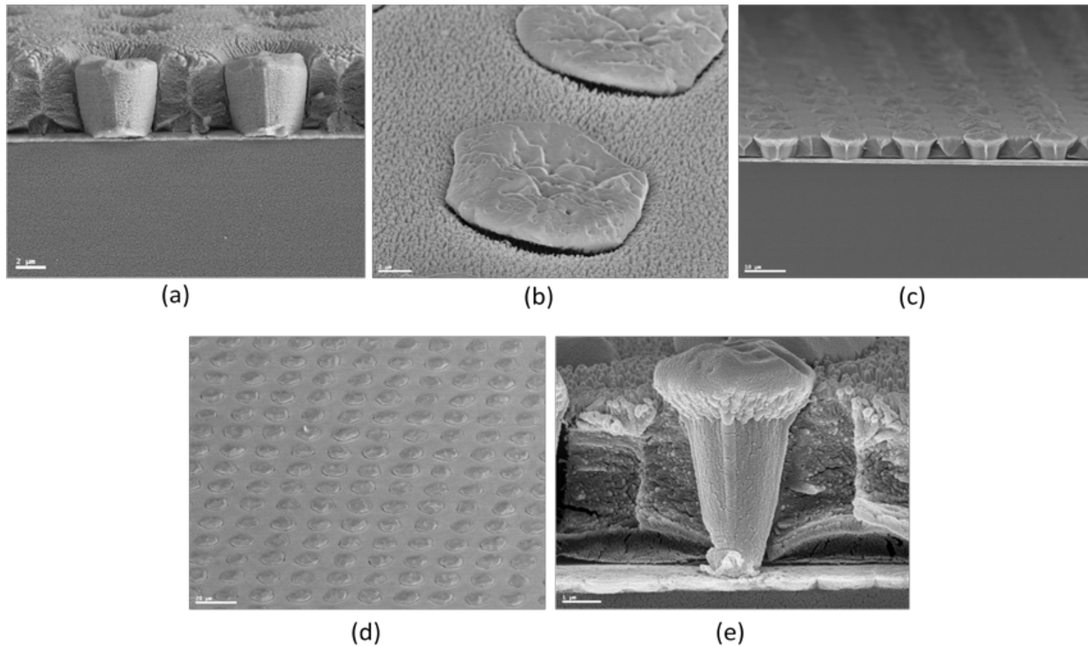


Figure 4.7: SEM images of electroplated In bumps filling patterned template wafers: (a) underfilled features, (b) bump tops showing separation between In and Teflon AF, (c) cross-sectioned array showing overplated features, (d) angled-view of overplated bumps and (e) 6 μm pitch bumps.

The effects of Teflon AF roughness on the In transfer step will be discussed in the following section. The morphology of the bumps is similar to those plated in photoresist, with no evidence of underplating. Additionally, it does not appear that the sidewalls of the Teflon AF were deformed by the plating process, and the In follows their positive slope. Figure 4.7c shows an angled view of a cross-sectioned template wafer. In this case, the bumps slightly overplated the Teflon AF layer. This layer was patterned by the two step DRIE/wet etching with the convex shape of the top of the layer between bumps and illustrates why this shape is undesirable. The bumps flare out as they reach this top surface to fill this shape. While this increases the surface area ratio from bump top to bottom, increasing the likelihood for transfer, the lateral growth increases the likelihood for shorting of bumps during the transfer step. This would become more problematic as

the process is scaled down, and bumps are moved closer together. Figure 4.7d shows another angled view of the bumps, further illustrating the lateral growth of In at the Teflon AF surface. Figure 4.7e shows a cross sectional view of a bump at a 6 μm pitch that overplated the template wafer.

4.3 Transfer of Small Pitch In Bumps

With In electroplated in the template wafer, the last step in the process was to attempt to transfer the bumps to mechanical ROICs. As previously discussed in Chapter 2, blanket MoN_x films on Si were used for this purpose. The recipe used resulted in MoN_x films has an x-value of .48 as measured by Auger electron spectroscopy (AES). Prior to the transfer sequence, each template wafer underwent a surface preparation step to remove the oxide from the In bumps which consisted of a 20 s dip in 5% HCl in DI water, followed by a DI water rinse and N_2 drying step. Samples were immediately placed onto the flip-chip bonder for pressing to the mechanical ROIC. After pressing the template and mechanical ROIC together, they were separated from one another and results were analyzed.

4.3.1 In Transfer Variables and Experiments

In addition to modifying the pressure applied to the samples with the flip-chip bonder, several other variables were investigated to determine an optimal transfer process. This included altering properties of both the template wafer and of the flip-chip bonding processes. Template wafer sidewall angles were altered to change the ratio of

cross-sectional area of the top and bottom of the In bumps. The duration of the blanket Ar RIE plasma step to clear the Teflon AF from the bottom of features was changed. This step induced roughness to the surface of the Teflon film which increased with raised plasma times. By varying this roughness, a determination can be made of the effects of increased surface area between the In and Teflon AF on the transfer process. The amount of In overplating the Teflon AF film was also investigated to determine how much was necessary to properly transfer bumps without shorting. Reflow of In bumps prior to the flip-chip bonder step was also attempted to see whether the reshaping caused by this step improved the properties of transfer. For the flip-chip bonder step, pressure was applied for 5 min for every set of samples. This allowed the In to creep onto the mechanical ROIC for an ample time. The pressure applied to the samples was varied to find the window between where adhesion of In to the mechanical ROIC does not occur due to low pressure and shorting of adjacent bumps due to high pressure. Heating of each sample was adjusted to determine whether raised temperatures allowed for better adhesion of In to the MoN_x film.

Table 4.4 summarizes the parameters used and results obtained from each of the transfer processes attempted using Ni as the template wafer seed layer. The table is split into template wafer and flip chip bonder parameters for readability.

Run	Pitch (μm)	Sidewall Angle (deg.)	RIE time (s)	Overplate (μm)	Notes:
1	15	82	60	1	In solder flux used
2	15	82	60	1	Overplated In scraped,flux used
3	15	82	60	1	Overplated In scraped, no flux
4	15	82	60	1	
5	15	82	60	1	Overplated In scraped
6	15	82	60	1	
7	10	81	180	0.75	
8	10	81	180	0.75	Roughened MoN_x
9	10	81	180	0.75	
10	10	81	180	0.75	
11	10	81	180	0.75	
12	15	81	180	1.25	In reflowed
13	15	81	180	1.25	In reflowed
14	10	68	240	0.5	
15	10	81	240	1	
16	10	74	180	1	
17	10	81	120	1	
18	10	81	120	0	
19	10	81	120	1.75	
20	10	81	180	1.25	
21	15	74	180	1.25	
22	15	81	180	1	
23	15	68	180	0.75	

Run	Force Per Bump (g)	Temperature (°C)	Notes:
1	1.5	158	In pooling
2	1.5	158	In pooling
3	1.5	158	In pooling
4	0.3	23	Transfer occurred, almost entirely shorted
5	0.3	23	Poor transfer
6	0.2	23	Transfer with reduction in shorting
7	0.25	23	Transferred, nonplanarity dominated
8	0.25	23	Poor transfer
9	0.25	140	Transferred, nonplanarity dominated
10	0.25	140	Transferred, nonplanarity dominated
11	0.2	140	Transferred, nonplanarity dominated
12	0.18	140	Transfer occurred, almost entirely shorted
13	0.08	140	Poor transfer
14	0.18	140	Transferred, nonplanarity dominated
15	0.18	140	Transferred, nonplanarity dominated
16	0.18	140	Transferred, nonplanarity dominated
17	0.18	140	Transferred, nonplanarity dominated
18	0.18	140	Transferred, nonplanarity dominated
19	0.18	140	Transfer occurred, almost entirely shorted
20	0.18	140	Transferred, nonplanarity dominated
21	0.18	140	Transferred, nonplanarity dominated
22	0.18	140	Transferred, nonplanarity dominated
23	0.18	140	Transferred, nonplanarity dominated

Table 4.4: Summary of transfer experiments performed on template wafers. The first part of the table shows the parameters of the template wafers used while the second shows parameters of the transfer process and notes about the transfer

4.3.2 In Transfer Proof of Principle

Several images of Mechanical ROICs taken after the transfer process are shown in Figure 4.8. In Figure 4.8a, 15 μm pitch In bumps transferred to a MoN_x mechanical are shown. This SEM image shows a relatively consistent bump morphology and thickness. No shorting between bumps is evident with a roughly 10 μm spacing between adjacent bumps indicating ample room to scale down the process. An SEM image of transferred bumps taken over a larger field is shown in Figure 4.8b. This image shows the successful

transfer of several thousand bumps with no shorting. Transfer of 10 μm pitch In bumps is shown in Figure 4.8c. In this image, roughly a thousand bumps were transferred to the mechanical ROIC. No shorting occurred between bumps.

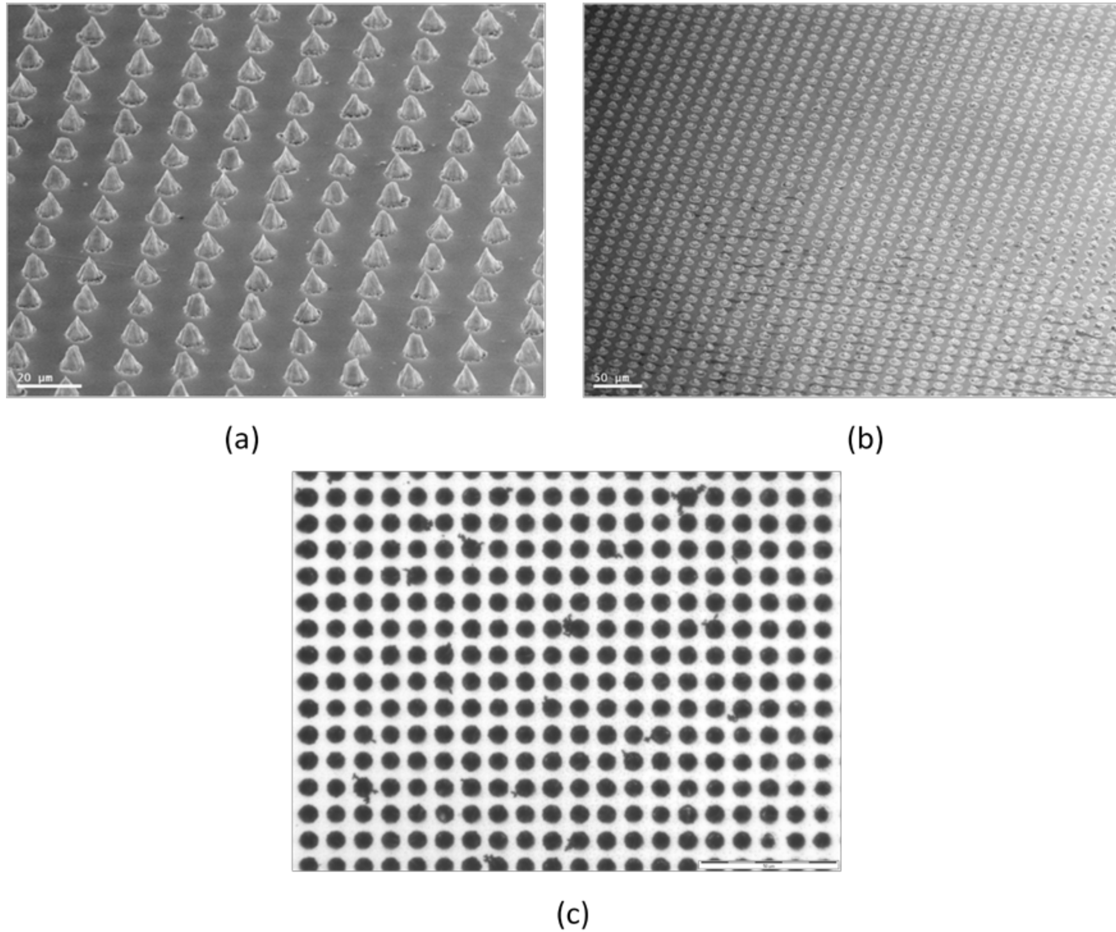


Figure 4.8: Images of In bumps transferred to mechanical ROICs with no shorting: (a) and (b) are SEM images of 15μm pitch bumps while (c) shows an optical image of 10μm pitch bumps.

Figure 4.9 shows SEM images taken of template wafers after the transfer process. In Figure 4.9a, nearly all the bumps were transferred from the wafer with 3 that did not transfer. Partial transfer of In can be seen in several features as well. An image of a separate template wafer in which complete transfer was observed is shown in Figure

4.9b. No In can be seen in the image. Additionally, the morphology of the Teflon AF layer remained intact after the transfer process. The sidewalls of the layer appear to still have a positive sidewall angle with no tearing or alteration evident and the Teflon AF surface also appears to have remained intact. The roughness that appears was due to the blanket RIE process to open up the Ni seed layer for electroplating. Such images give evidence for the potential of reusability of the Template wafer.

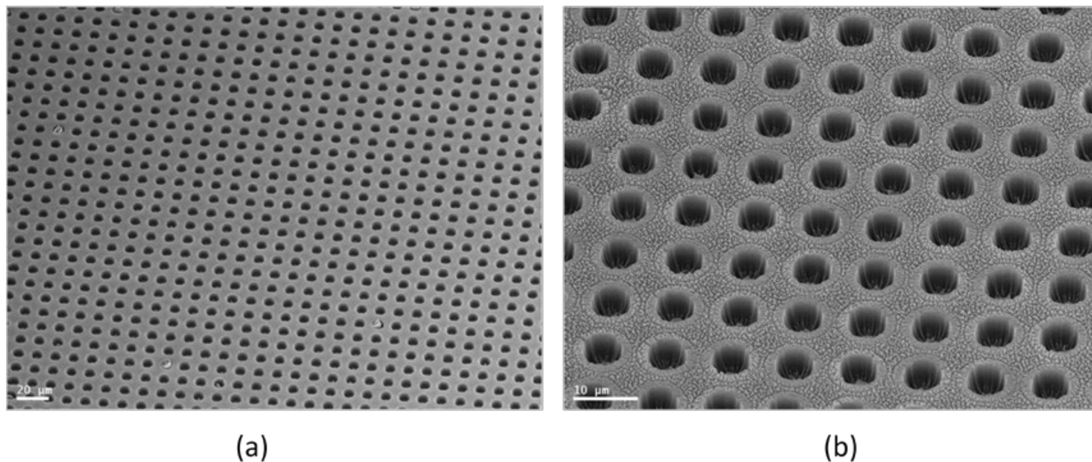


Figure 4.9: SEM images of template wafers after the transfer process.

4.3.3 Nonplanarity During Transfer Process

While a large percentage of In bumps transferred for the runs shown in Table 4.4, obtaining meaningful statistical data of the transferred bumps was difficult. For each mechanical ROIC, regions of shorted bumps appeared next to isolated bumps with good isolation next to sections of poorly transferred bumps. This type of lateral nonuniformity was caused by nonplanarity between the template wafer and mechanical ROIC. For the RD Automation M-8 flip-chip bonder used for this project, a pitch/roll mechanism was used to improve planarity between wafers. This requires the two wafers to be pressed

lightly pressed together, after which a mechanism is released to allow the mechanical ROIC to pivot, ideally such that the surface of the wafers are parallel. Use of this mechanism was attempted before several transfer processes but did not produce improved results. Because of this issue, nonplanarity dominated the experimental results. It was still possible to draw some conclusions about the process, which will be discussed in the following sections.

In moving forward, it would be ideal to attempt the transfer process on a state-of-the-art system, such as the SET FC-150. Rather than using the pitch/roll mechanism described above, laser leveling is employed to optimize the planarity of wafers. The planarity spec given for such a system is 20 μradians. Such planarity would limit the degree of wedging to less than 400 nm over a 2 x 2 cm wafer.

4.3.4 Effects of Sample Heating

Several temperatures were applied to the template wafer and mechanical ROIC during application of pressure by the flip bonder. Each sample was placed on a chuck that had the ability to apply heat in 1° steps to well above its melting point. Initial experiments, including Runs 1-3 of Table 4.4, looked at melting the bumps with the application of pressure and cooling them with pressure applied to reform on the mechanical ROIC. The heating cycle for these samples was as follows: place samples on chucks of the flip-chip bonder and ramp to 140 °C, allow temperature to stabilize for 2 min, apply pressure and raise the temperature above the melting point of In to 158 °C, once achieved, reduce temperature of the chucks to room temperature and release the

pressure. Several different In preparation steps were used including the use of In flux to remove surface oxides and scraping of the overplated In with a sharp blade. In each case, In successfully transferred to the mechanical ROIC with some bump formation; however, bumps were poorly formed and a continuous In film resulted on this wafer. It appears the melted In essentially leaked between adjacent bumps while pressure was applied. Based on the transfer of In from the template wafer, it appears such a reflow process would be feasible if a better seal formed between the Teflon AF layer of the template wafer and the metal layer of the mechanical ROIC. Other heating experiments looked to determine whether temperatures below the melting point of In would improve transfer by increasing its malleability. For these experiments, the temperature of each sample was raised to 140 °C, followed by the application of pressure at this temperature for 5 min after which the samples were cooled to room temperature and pressure released. When comparing transfer at room temperature versus raised temperature, the results were inconclusive.

4.3.5 Effects of Force

Normalized force, in the unit g/bump, was altered to attempt to determine an optimal force for transfer. This unit was based on the number of bumps in contact with the mechanical ROIC during the pressing step as calculated from its area. Establishing a window for this parameter was important. Some deformation of In onto the mechanical ROIC was necessary for bonding and transfer placing a lower bound on the force required. Above the upper limit of this window, too much In deformation occurs resulting in shorting of adjacent bumps. As the pitch of bumps is reduced, this window decreases because shorting is more likely to occur for more closely spaced bumps. Even with wafer nonplanarity dominating the transfer process, forces of .08 g/bump resulted in no In

transfer, helping to map out a lower bound on force required. Forces of .18 g/bump up to .25 g/bump were attempted and both resulted in regions of well transferred, electrically isolated In bumps.

4.3.6 Effects of Overplating

The thickness of In plated above the Teflon AF was varied to determine its effects on transfer. It is obvious after reaching some upper limit, overplated bumps will short out when they are deformed by the application of pressure by the flip chip bonder. This is more problematic due to the means by which the overplating progresses above the Teflon AF surface. Figure 4.10 illustrates this, where substantial overplating occurred. As the In is plated above the Teflon AF layer, its growth is no longer constrained by the feature it fills. This results in an equal amount of growth in both the vertical and horizontal direction; therefore, any overplating necessarily increases the likelihood of shorting between adjacent bumps. This was observed in Run 19 where In was plated 1.75 μm above the Teflon AF surface for bumps at a 10 μm pitch. For this experiment, shorted bumps transitioned directly to poorly transferred bumps, indicating the degree of overplating was dominant over nonplanarity. While overplating reduces the spacing between bumps for the transfer process, it potentially benefits the transfer process since the surface area of the In in contact with mechanical ROIC increases, thus, providing increased adhesion between the two layers. It therefore becomes necessary to determine the lower limit of overplating that allows for good transfer. A variety of different overplating thicknesses were attempted ranging from 1.75 μm down virtually no overplating. High percentage transfer occurred at all thicknesses within this range. The

key result there was that good transfer was observed for Run 18 where no overplating occurred. For this sample, isolated bumps transitioned directly to poorly transferred bumps with no shorted bumps evident. By plating In level to the top of the amorphous fluoropolymer, control of the spacing between adjacent bumps solely by adjusting the dimensions of the bumps themselves, without the added parameter of undesirable lateral deformation during the pressing step. With improved planarity between wafers, this appears to be the most promising path forward for a high yield process.

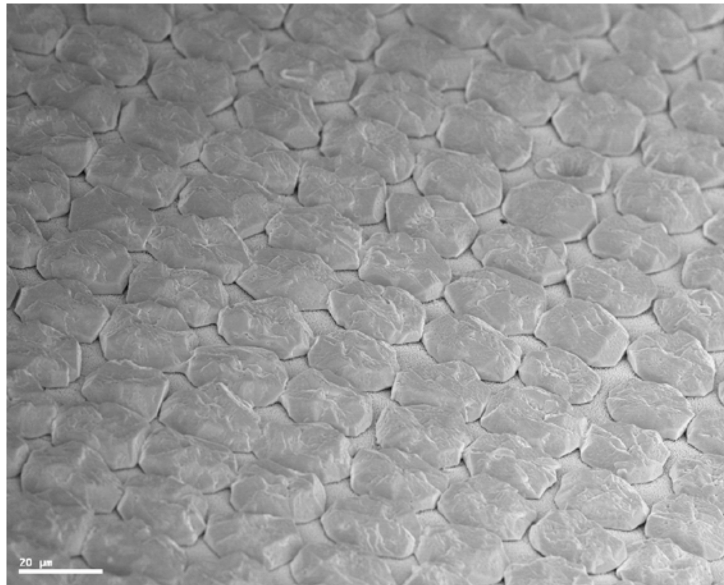


Figure 4.10: SEM image of overplated In bumps showing large amount of lateral In growth.

4.3.7 Effects of Reflowing Prior to Transfer

An In reflow step prior to loading onto the flip-chip bonder was attempted to improve the transfer process. The initial thought behind this was to improve the thickness uniformity of In across the wafer by reducing the large grain structure down to a rounded, minimum energy shape. Oxide removal was accomplished by a 20 s dip in 5% HCl in DI

water, followed by a DI water rinse and a N_2 drying step. This was immediately followed by placing the sample on a hotplate held at 158 °C for 2 min, above the melting point of In but below the T_g of Teflon AF, and cooled to room temperature. SEM images of In bumps in Teflon AF before and after this reflow process are shown in Figure 4.11. As expected, the grain structure of the bumps was almost completely removed, resulting in rounded In overplating. Complete removal of the oxide layer was not achieved on all bumps based on their shape. Transfer following such a reflow process was attempted in Runs 12 and 13 and showed no improvement in the transfer of bumps when compared to other runs. This was likely due to the fact that while the reflowed bumps had a more consistent shape, the volume with or without this step was fixed yielding the same degree of contact and lateral squeezing while pressed by the flip chip bonder. In other words, while the reflow improved lateral thickness uniformity, it had no effect on improving the transfer of bumps.

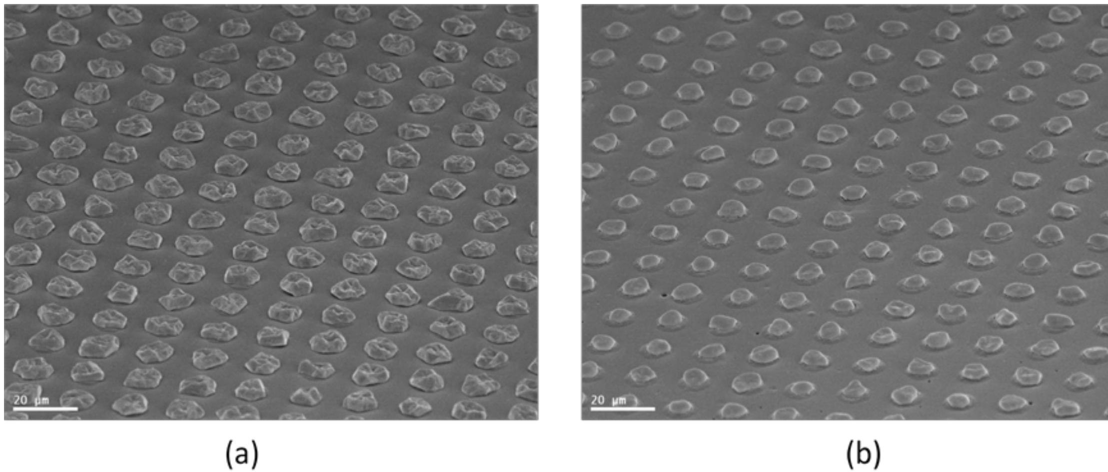


Figure 4.11: SEM images of In bumps grown in template wafers: (a) before and (b) after a reflow process.

4.3.8 Effects of Teflon AF Roughness

As previously discussed, the blanket Ar RIE process to fully open features on the Teflon AF for In electroplating produces a roughened surface increasing its surface with the In bumps. This is potentially problematic since the In may be less likely to transfer from the template wafer. Transfer of In from template wafers was attempted with RIE steps ranging from 60 s to 240 s. The average roughness incurred by the blanket etching step increased almost linearly with time. Roughly 250 nm/min of roughness was produced in the Teflon AF layer by this step. While the roughness at the top surface of the Teflon AF increased with longer RIE steps, sidewall roughness was not affected as much due to the relatively vertical sidewalls used for the template wafers which is logical given the physical nature of the Ar etch. After investigating the template wafers following each transfer step, there was no evidence of adhesion between the Teflon and In. Even for experiments where the transfer of In to the mechanical ROIC was poor, partially transferred bumps such as those shown in Figure 4.13, appear to adhere to the Ni base layer alone. The important conclusion from this set of experiments is that the Teflon AF to In adhesion is negligible when compared to the In to Ni adhesion.

4.3.9 Effects of Sidewall Angle

Transfer of In from template wafers with a variety of sidewall angles, ranging from 68° up to 81°, was attempted. It should be noted that the transfer steps attempted with the 82° sidewall angles were preliminary to obtain a bound on the parameter space of the process. The variation in sidewall angle was done to determine how much the cross-sectional area of the bump in contact with the seed metal had to be reduced to allow

for good transfer. At a sidewall angle of 68°, the dimensions of the bump were reduced to below 1 μm at the seed layer resulting in a ratio of cross-sectional areas below 1/25. Regions of good transfer to mechanical ROICs, limited by nonplanarity, was obtained using template wafers of all sidewall angles attempted indicating that near vertical sidewalls could be used for the template wafer.

Chapter 5

Ni Plating of Via Contact Metallization

5.1 Introduction

This chapter details the results of both electroless and electroplated Ni for via contact metallization of small pitch FPAs starting with plating results on dummy samples to establish feasibility of the processes. Properties of plated Ni films are then investigated to further determine compatibility with II-VI materials and to further optimize the processes. Results of Ni plating of vias of mechanical arrays are also included, whose features and materials provide a close approximation to active FPAs. Finally, data from electroless Ni plating of active test arrays and small pitch FPAs is presented.

5.2 Plating of Dummy Samples

5.2.1 Electroplated Ni

Initial electroplating experiments focused on minimizing the current density of the process for compatibility with ROIC specifications where optimal conditions for the specific bath were listed as 27 – 161 mA/cm^2. Figure 5.1 shows SEM images of stepper-fabricated dummy samples plated with Ni for 20 mins at roughly 25 mA/cm^2 in a room temperature bath. Calculating a precise current density was difficult due to uncertainty in

the exposed surface area of the alligator clip in the bath that was plating along with the sample. A cross-sectional view shows a 2 μm thick Ni with the photoresist remaining. The feature, consistent with others plated using the same process, had a slightly concave top surface. The increased plating rate at the edges of the Ni plug is likely caused by nonlinear diffusion of Ni ions at this region, compared to a linear diffusion rate near the middle of the plug, resulting in an enhanced plating rate [131]. The grain size of the Ni is smaller than the resolution of the image as no grains are evident upon close inspection. This agrees with the 25 – 35 nm grains sizes of electroplated Ni observed in the literature [64]. Instead, roughness of the Ni sidewall correlates with the roughness of the photoresist feature. Several hundred Ni plugs with the photoresist stripped away are shown in an angled view in Figure 5.2. This image shows the lateral consistency of the process where several hundred nearly identical bumps are shown.

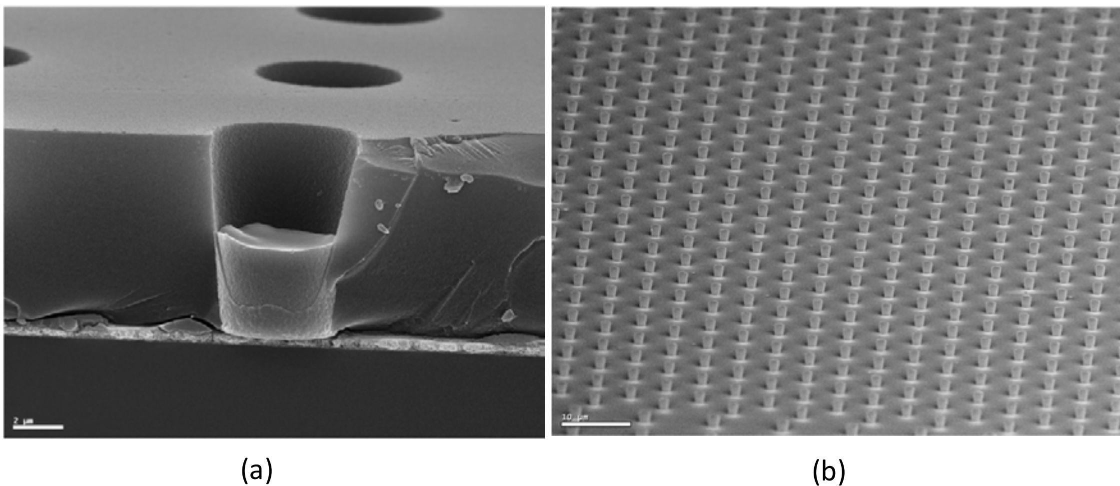


Figure 5.1: Electroplated Ni features: (a) in photoresist and (b) with photoresist stripped.

In Figure 5.2, a 110 min plating process using similar current densities was performed. The resulting Ni plugs were measured to be 6.8 μm tall. Over-plating of the

photoresist resulted in the mushroom-shaped features shown in Figure 5.2a, where photoresist was stripped to expose the entire Ni feature. As the Ni grew out of the photoresist, the free surface allowed for lateral expansion at roughly an equal speed as vertical growth, explaining the semi-spheroidal shape of top of the plug. The reduction in plating rate for this sample can be explained by increased surface area of the Ni plugs as they grew out of the photoresist. With a constant current applied to the sample, the increased surface area results in a reduced current density applied to the sample. Figure 5.2b shows several hundred of these over-plated features with the photoresist intact at one edge of the pattern. Like the bumps plated for 20 min, a high lateral uniformity was observed. The bumps at the edge are only marginally thicker than interior bumps due to electric field edge effects. Such nonuniformity is likely to have little effect on the via contact metallization since plated films thicknesses will be well below that required for over-plating.

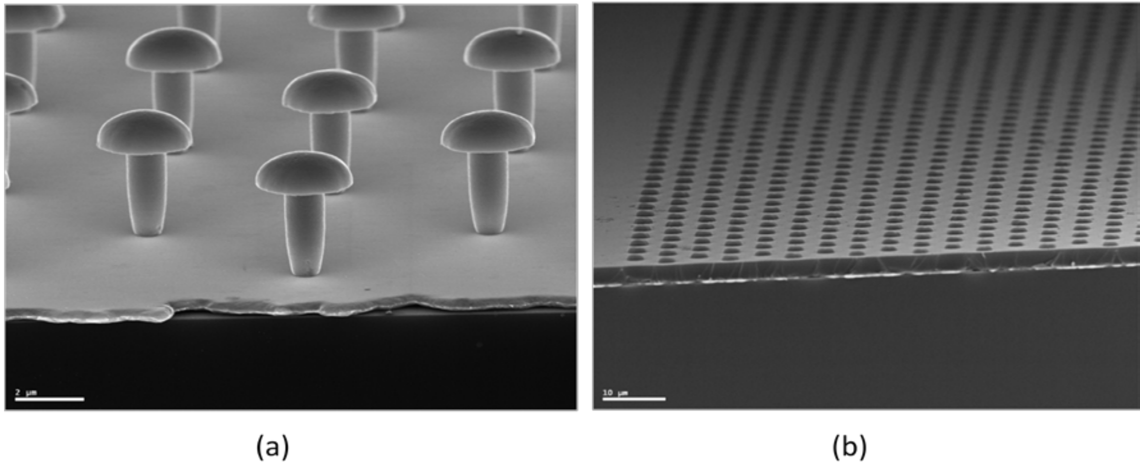


Figure 5.2: Electroplated Ni that overplated the photoresist: (a) with photoresist stripped and (b) with photoresist intact.

With ROIC specifications in mind, Ni films were electroplated at lower current densities. Figure 5.3 shows the results of a 110 min Ni electroplating process with a current density of roughly 5 mA/cm^2 at two different resolutions. The resulting Ni plugs were only about .1 µm tall, yielding a plating rate of about 1 % that of the 25 mA/cm^2 process. At such low current densities at room temperature, weakly bound species at the sample surface such as H or boric acid inhibit Ni growth [132]. These types of low growth rates are not feasible for this via process, therefore current densities were held at roughly 25 mA/cm^2.

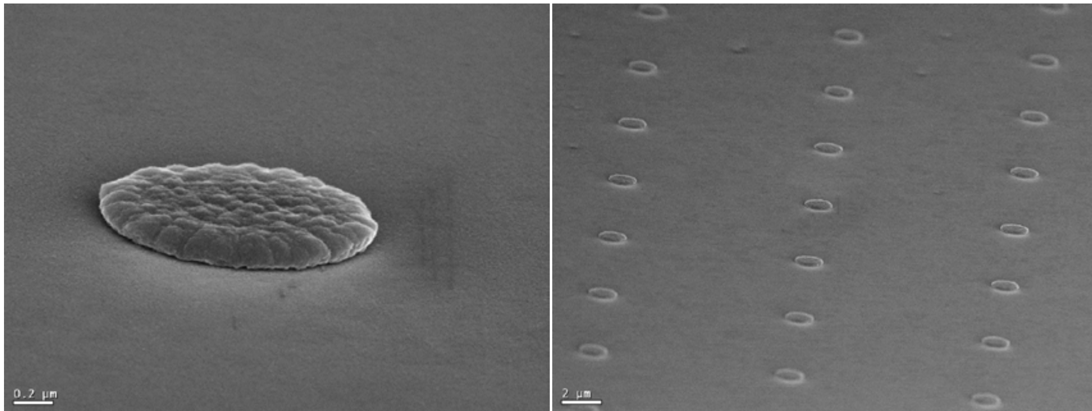


Figure 5.3: Images of low current density electroplating of Ni features with photoresist stripped.

While the consistency of plated Ni across dummy samples was high in general, defective plating was occasionally found in groups of features. Figure 5.4 is an optical microscopy image of about 20 bumps where plating thickness was substantially lower than the surrounding Ni. Based on the nearly round defective area, it is apparent that H bubbles evolved from the electroplating reaction and adhered to the surface of the photoresist. These bubbles cut off Ni deposition to the features underneath since access to

Ni^{+} ions is removed. A simple solution used to remove these defective regions was to sparge the sample surface more aggressively to carry away the H bubbles with the application of N_2 gas.

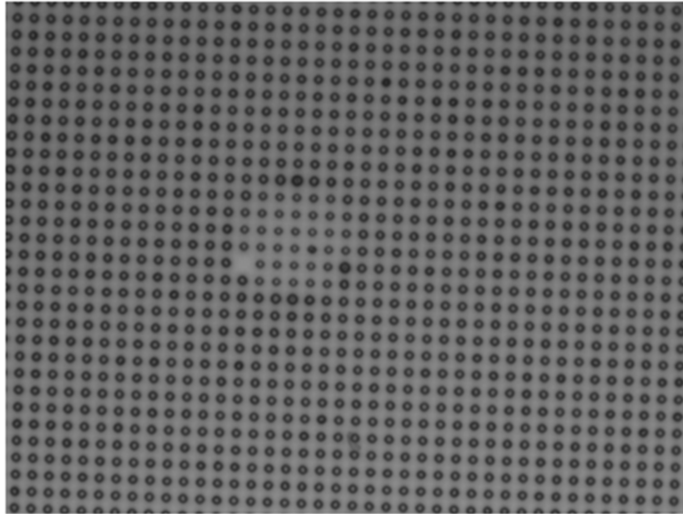


Figure 5.4: Defective region of electroplated Ni features due to adhesion of a bubble.

5.2.2 Electroless Ni

Before any successful electroless Ni plating occurred, some optimization of the process was required with respect to chemical composition and bath temperature. An initial process, as described in Section 2.5.3, was found to favorably plate Ni films within a bath temperature range of 50 to 60 °C. Figure 5.5 shows SEM images of electroless Ni plugs formed with photoresist stripped away. The plug shown in Figure 5.5a was plated for 30 mins at 50 °C while the ones shown in Figure 5.5b were plated for 15 mins at 55 °C. The plugs plated by this technique share several similarities with the electroplated Ni. The plugs are once again concave at the top surface, likely due to a nonlinear diffusion region of Ni ions at the edges of the feature. Lateral uniformity was excellent with no

evidence of edge effects. Such effects from field nonuniformities would not be expected for electroless plating; however, edge effects due to poor mass transport could occur. Additionally, evidence of bubbles sticking to the sample surface during the process was observed. With constant sample agitation, such features were mostly removed. Like the electroplating process, it is anticipated that the addition of aggressive sparging would mitigate electroless Ni defects. While the two types of plugs appear very similar, closer inspection of the top surface of the electroless Ni shows a visible grain structure not present for the electroplated Ni. The grains still appear to be on a substantially smaller scale than the plug; thus, roughness from grains is not an issue for features at this scale. The effects of bath temperature on plating rate are evident based on the two images shown, where the lower bath temperature significantly reduces plating rate. This issue will be discussed in greater detail in the following sections.

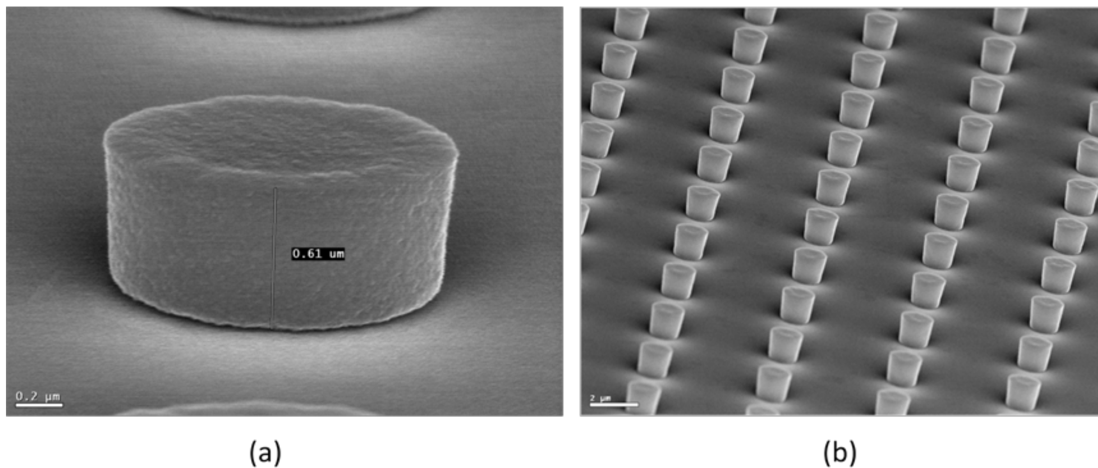


Figure 5.5: Electroless Ni features with photoresist stripped: (a) 30 mins at 50° C and (b) 15 mins at 55° C.

5.3 Properties of Plated Ni

5.3.1 Compatibility of FPA Materials with Plating Chemicals

SEM images of MBE-grown CdTe/Si and HgCdTe/CdTe/Si samples were obtained before and after being dunked in the electroless and electroplated Ni baths for 4 hr, which is roughly an order of magnitude longer than a feasible process for this application. Considerable corrosion of the II-VI materials would not be desirable since it would likely have deleterious effects on diode electrical qualities. HgCdTe samples appeared to be unaffected by both plating baths as well as CdTe in the Ni electroplating bath. On the other hand, the electroless bath appeared to slightly etch the surface of the CdTe. Figure 5.6 shows the images taken of the CdTe surface. The CdTe surface before exposure to the electroless bath is shown in Figure 5.6a, where a roughness pattern appears, potentially due to $[\bar{2}31]$ and $[\bar{2}13]$ slip planes [133]. After immersion, the roughness pattern was altered leaving only one set of visible slip planes. While the morphology of the sample surface changed, no appreciable etch rate was measured. KOH has been found to etch CdTe [134], and likely caused surface changes. Although such changes may be viewed as undesirable, they are unlikely to impact diode performance since the CdTe is the passivant and not the active layer of the device.

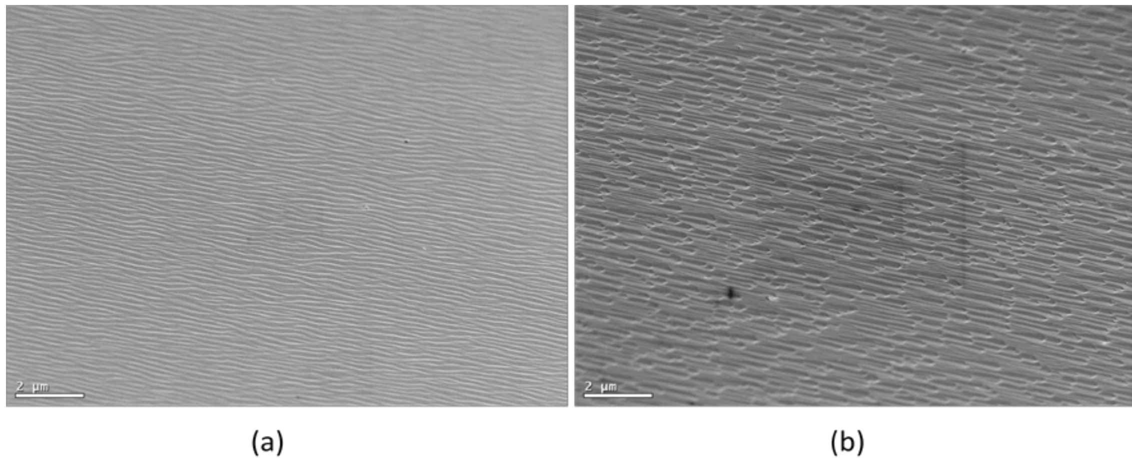


Figure 5.6: SEM images of the CdTe/Si surface: (a) native surface and (b) after 4 hr in the electroless bath.

5.3.2 Nucleation of Plated Ni

Results of the initiation of plating for both types of Ni onto untreated dummy Ni/Si samples are shown in Figure 5.7. The main purpose of this set of experiments was to determine if there was a latency period before plating was initiated, as well as investigating the initial morphology of plated Ni. For electroplated Ni, plating of Ni was observed from 30 s onward, indicating a short, or nonexistent, latency period. Figure 5.7a-c show the progression of Ni growth from small, disparate islands at 1 min that began to merge at 2 min and continued to grow and merge at 5 min. Surface preparations of the Ni/Si dummy sample were performed in an attempt to shed more light on whether oxide on the bare Ni surface may be the reason for such morphology; this sunject will be discussed in the next paragraph. Electroless Ni growth initiation was somewhat different. No Ni plating was observed until Ni was held in the bath for 2 min. Once initiated, Figure 5.7d-f shows the progression of growth. Rather than disparate grains coalescing, the

continuous films of electroless Ni is formed shortly after growth initiated and continues vertically as time progresses.

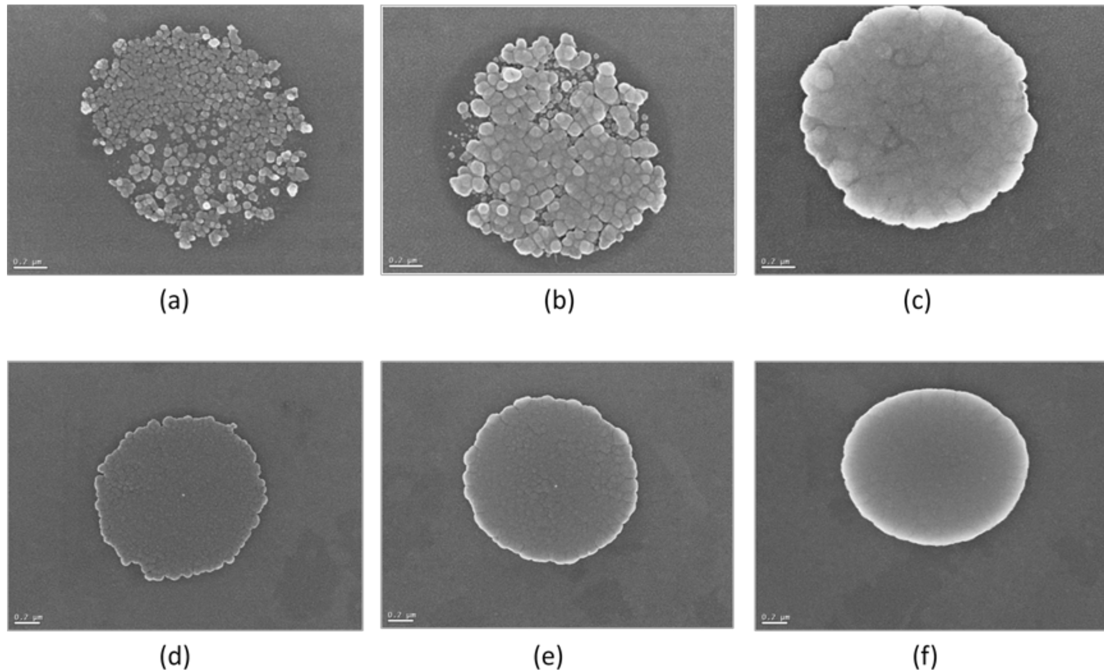


Figure 5.7: Images of the initiation and progression of Ni plating: (a) 1 min electroplated, (b) 2 min electroplated, (c) 5 min electroplated, (d) 2 min electroless, (e) 3 min electroless and (f) 5 min electroless.

The addition of dilute HNO_3 surface preparations of Ni/Si dummy wafers did not affect the outcome of the plating initialization experiments. Similar disparate grains were observed for electroplated Ni. As described in Section 2.5.2, samples were held in the electroplating bath for several minutes with no current applied to ensure removal of bubbles before plating. The room temperature native oxide thickness has been measured to be limited at 10 Å [135]. The boric acid in the bath may have etched away the thin native Ni oxide during this immersion, essentially performing the same function as the HNO_3 preparation step. The nucleation and growth of the electroplated Ni onto untreated Ni/Si dummy samples was, therefore, not inhibited by a surface oxide and instead

followed its natural nucleation and growth process. For electroless Ni, the HNO_3 changed neither the morphology of the initial Ni layer nor the roughly 2 min latency period before plating started. Because of this, the Ni oxide layer does not appear to affect the electroless process; rather, weakly bound species at the sample surface may inhibit the initial Ni growth process [132].

Determining whether Ni plated directly onto HgCdTe was important since much of the exposed surface of the via is HgCdTe. Both the shape and speed at which vias are metallized are impacted by this, which in turn impacts total plating time. Figure 5.8 illustrates the possible outcomes as plating progresses on the same time scale. Figure 5.8a shows the case where no plating occurs on the HgCdTe for either the electroless or electroplating process. This scenario has the slowest progression as Ni only grows in the vertical direction from the ROIC contact pad, and this is essentially how the dummy arrays are plated. The progression of Ni growth, if it electroplates onto HgCdTe, is shown in Figure 5.8b. In this case, plating starts only in the vertical direction from the ROIC contact pad. When the Ni plug reaches the HgCdTe layer, the entire exposed surface begins to plates inward and merges with the vertical plating front, speeding the thickness of the plug. Figure 5.8c shows the progression of electroless Ni growth if it does in fact plate directly onto HgCdTe. This represents the fastest growth, where plating starts both at the ROIC contact pad and the HgCdTe surface of the via, resulting in faster merging of the two growth fronts.

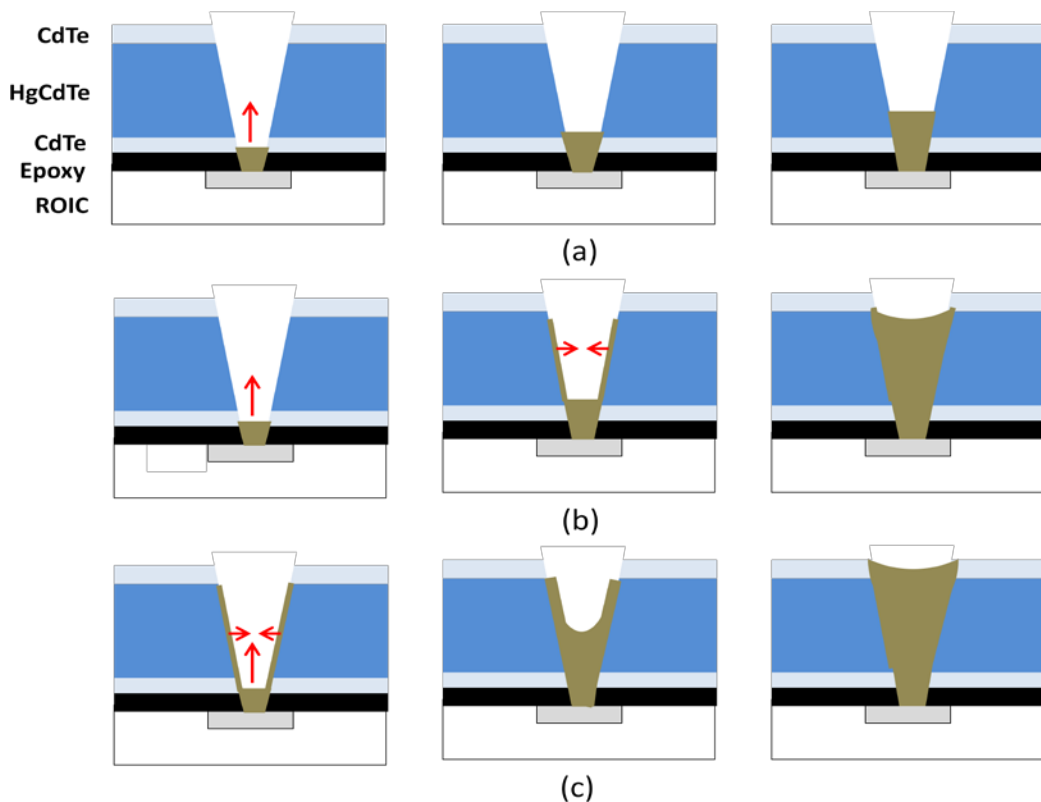


Figure 5.8: Possibilities of the progression of Ni plating: (a) plating occurs only at the ROIC pad, (b) electroplating progression if Ni electroplates directly onto HgCdTe and (c) electroless progression if electroless Ni plates directly onto HgCdTe.

The results of plating Ni directly onto MBE-grown MWIR HgCdTe/CdTe/Si are shown in Figure 5.9. A roughly .6 µm thick electroplated Ni layer is shown in Figure 59a. The striations that appear in the SEM image are due to cleaving slightly off the [110] direction. While MWIR HgCdTe is a semiconductor, its relatively small bandgap of about .25 eV [136] allows for sufficient conduction across its surface for electroplating to occur. Similarly, a roughly .6 µm thick electroless Ni layer grown directly onto HgCdTe is shown in Figure 5.9b. Like the electroplating process, the relatively low conductivity of HgCdTe allows for electroless Ni plating. For the electroless process, the sample still acts as a cathode within the solution even though there is no outside current applied; thus,

a conductive surface allows for electroless deposition in general. Because both Ni processes plate directly onto HgCdTe, filling of both mechanical and active vias will progress faster than for dummy arrays for the reasons described in the previous paragraph. This fact also has an added benefit regarding electrical continuity. If Ni plating did not occur directly onto HgCdTe, good electrical contact would rely upon the physical contact only between the HgCdTe and the Ni layer with no additional bonding process. Because active FPAs are cryogenically cooled for operation, the relatively large Ni expansion coefficient of 12.9×10^{-6} K^{-1} at 300 K [137] would likely cause the plugs to contract from the via surface, producing an open contact. Because both types of Ni plated onto the HgCdTe, various bonds including metallic, ionic, and covalent bonds form between the two giving substantially better adhesion. Epitaxial growth is even possible with plating under the right conditions [29]. The adhesion will help to resist the Ni from pulling away from the HgCdTe under cryogenic cycling, maintaining good contact between the ROIC and HgCdTe diode.

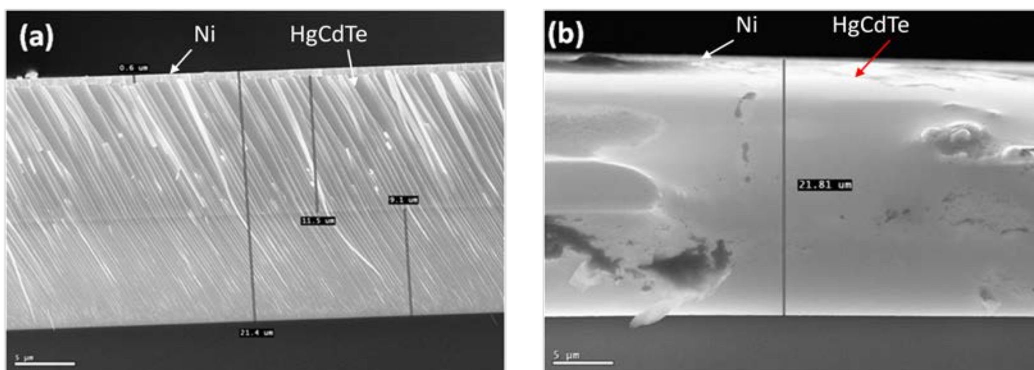


Figure 5.9: Results of plating directly onto HgCdTe: (a) electroplated Ni and (b) electroless Ni.

5.3.3 Effect of Electroless Ni Parameter Variation

The electroplating bath used for this study is composed of a relatively simple mixture of chemicals with room temperature operation; therefore, no parameters outside of changing the applied current density were investigated. The electroless bath, on the other hand, is substantially more complex. This bath is comprised of a more complicated list of chemicals, and plating occurs at an elevated temperature. Because of this, several parameters of the bath were varied to determine their effects on deposition rate and morphology to look for optimal plating conditions.

For electroless processes, temperature is a key catalyst in driving the reactions in the bath past equilibrium into a reducing state. Because this parameter is important to the process, Ni plating at a variety of temperatures was performed, and plating rates are plotted in Figure 5.10. Below 48 °C no deposition was observed, meaning the temperature was not high enough to produce a reducing environment in the bath. On the other hand, bath temperatures above 60 °C resulted in uncontrollable precipitation of Ni from the bath onto all surfaces, therefore, the temperature window for this process is roughly 12 °C. This window is unique to the specific plating bath used since standard operating temperatures for electroless Ni are typically above 60 °C, below which negligible plating occurs [138]. The use of TEA as one of the bath complexing agents lowered the operating temperature which had been previously demonstrated for electroless Cu plating [111]. The upper temperature limit of the bath can be explained by the fact that no stabilizers were incorporated in the solution to prevent decomposition. While the operating window of the bath is relatively small, the low temperature operation is desirable when developing a process that maintains compatibility with HgCdTe.

Within this window, plating at three temperatures was attempted. The results showed a linear increase in plating rate from .6 µm/hr at 50 °C up to 5.1 µm/hr at 60 °C. Based on the steep gradient in plating rate, it is evident that good temperature control of the bath is necessary for consistent Ni plating. 55 °C was determined as the optimal bath temperature to maximize plating rate without running the risk of an uncontrolled reaction.

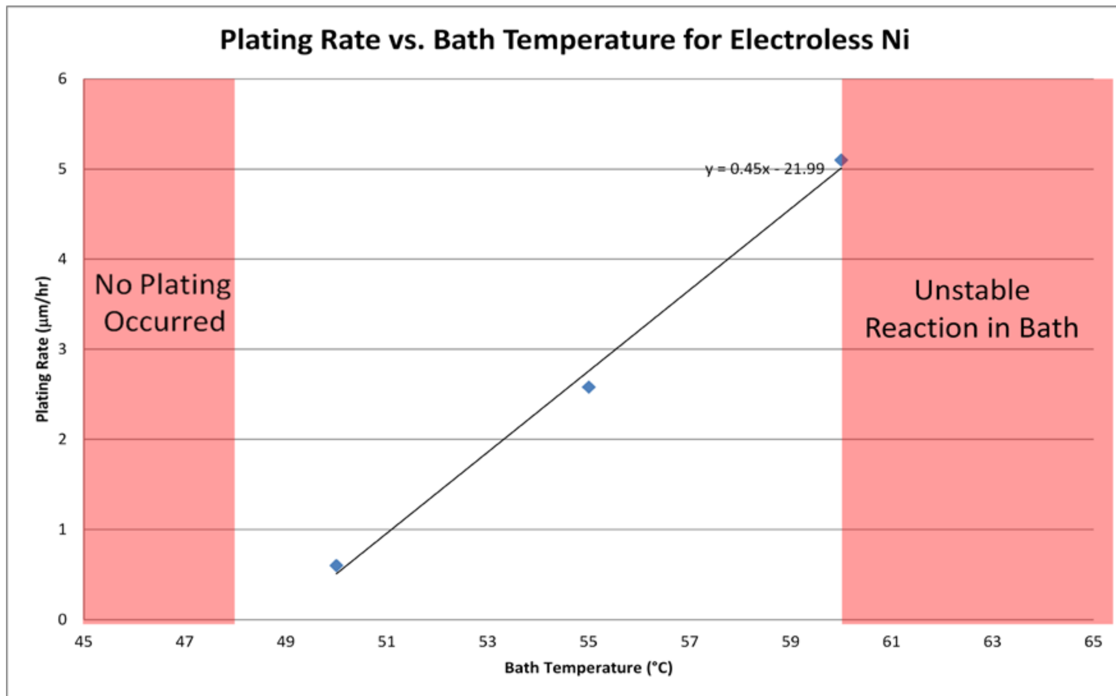


Figure 5.10: Plating rate as a function of bath temperature for electroless Ni.

Other process variations saw less dramatic changes in plating rates, with no visible changes in the morphology of Ni plugs. Figure 5.11 is a graph of plating rate as a function of NaOH added to a 40 mL electroless bath at 55 °C. An appreciable plating rate was occasionally observed with no NaOH added, with several attempts resulting in no plated Ni. The NaOH raises the pH allowing for electroless plating without the necessity of an activation step [111]. The addition of some NaOH is, therefore, key for a

reproducible process. With the addition of NaOH, the plating rate increased and hit a maximum of 1.98 μm/hr when 200 μL of NaOH were added. The rate then dropped slightly as more NaOH was added. After 660 μL was added, the process became uncontrollable with rapid precipitation of constituents out of the bath. Based on the results obtained, 195μL NaOH was chosen as it maximized plating rate while remaining well within the bounds of the process window.

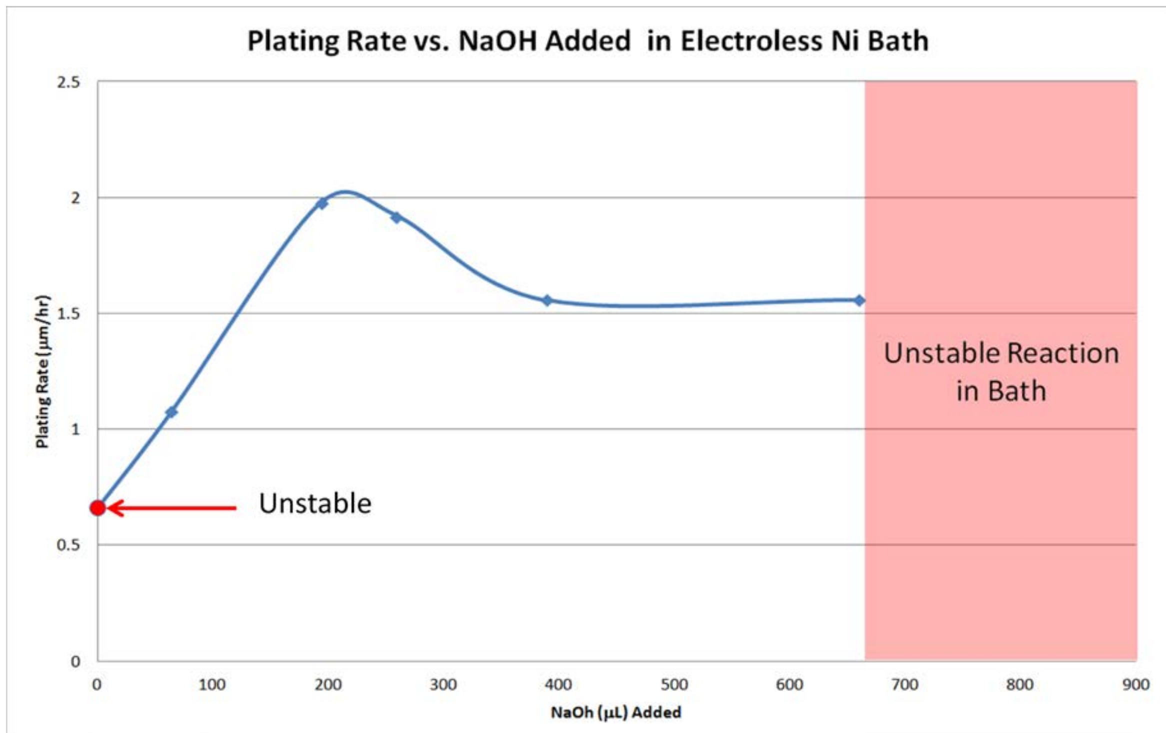


Figure 5.11: Plating rate as a function of NaOH added to a 40 mL electroless bath.

The amount of DMAB added to the bath was also varied, with no changes observed in the morphology of plated Ni features. As previously discussed, DMAB is the reducing agent for the Ni, and is therefore necessary in the plating solution. On the order of several % B is incorporated in the plated Ni, for which DMAB is the only source.

Because DMAB is the only source of B in the solution, it is anticipated that varying its concentration will alter B content in the plated Ni. Some control of the B concentration would likely allow for the ability to adjust the stress of the plated Ni as well as its resistivity. The results of this experiment with regard to surface analysis studies will be discussed below. Plating of several samples was performed with DMAB concentrations below 8 g/L to obtain a lower bound on the amount necessary for plating which was determined to be 3.75 g/L of DMAB in the solution.

Finally, plating as a function of the age of the bath was studied. The lifetime of this particular bath was reported as being on the order of tens of minutes, after which decomposition begins. The relatively short lifetime of the bath is due to the fact that no stabilizers are in the solution. In order to determine how long the bath remained stable, the standard electroless Ni bath at 55°C was mixed together. This was followed by plating of samples for 10 min; the first directly after the creation of the bath, the second 45 min later, and the third 75 min afterwards. No correlation between bath age and plating thickness or morphology was observed; therefore, a reasonable window of time exists where consistent plating occurs that was significantly longer than that previously reported. This increased window ensures that the bath remains stable longer than the amount of time required to plate samples for this application.

5.3.4 Surface Analysis Measurements of Plated Ni

XPS scans were taken on Ni films over a large range of binding energies with Al x-rays at a 25° take-off angle. Each type of Ni, including electron-beam evaporated, electroplated Ni, standard electroless Ni with 8 g/L DMAB, and electroless Ni with 3.75

g/L DMAB was deposited onto an HgCdTe/CdTe/Si tab and scanned by XPS for direct comparison. Figure 5.12 shows the scans superimposed for direct comparison, while Table 5.1 gives the compositional information based on the analysis of positioning and relative height of the peaks. The data shows large amounts of both C and O, as well as substantially less Ni than expected in a Ni film. In addition, several other impurities are present in the Ni at levels ranging from the tenths of a percent up to several percent. Because XPS is truly a surface sensitive technique, only the top several monolayers are sampled. This set of four samples had no preparation steps before the XPS measurements were taken, thus only the NiO top layer along with any impurities that were deposited on the surface were sampled. This information does not answer the question of what types of impurities are present at the Ni/HgCdTe interface on the inside of a via.

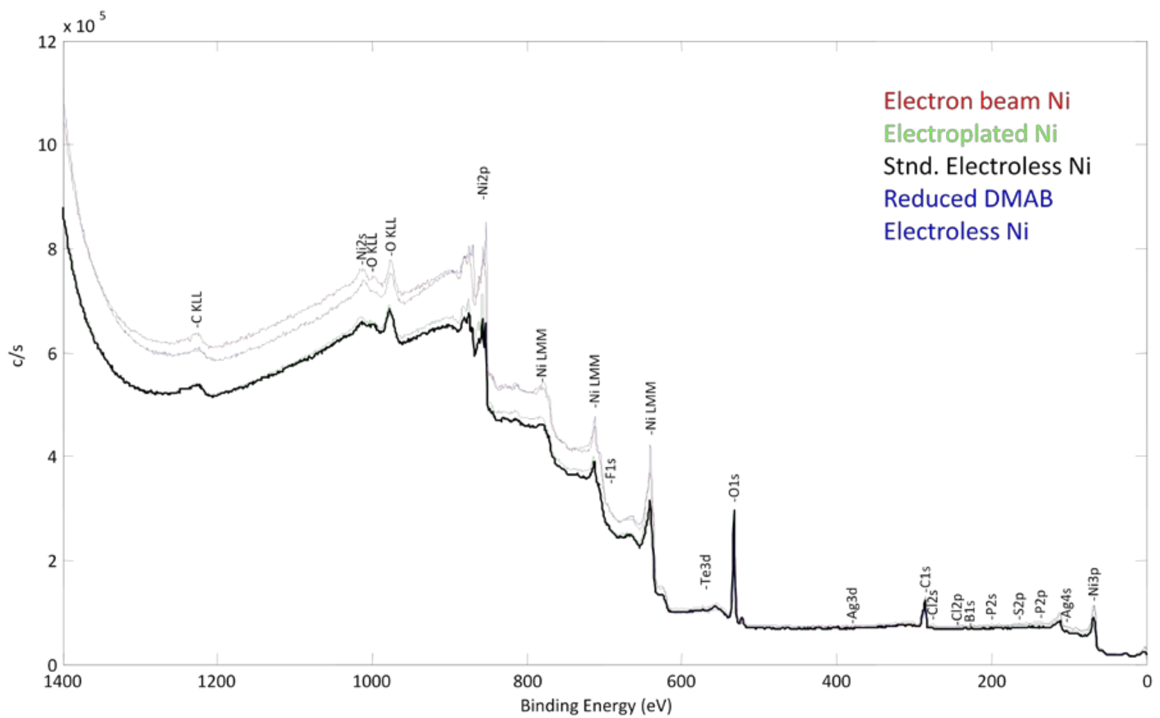


Figure 5.12: Wide XPS scans of Ni films deposited by various methods.

Element / Sample	Electron beam Ni	Electroplated Ni	Stnd. electroless Ni	Reduced DMAB electroless Ni
B	0	0	3.42	2.79
O	42.89	43.47	41.8	44.6
C	25.4	28.1	33.1	31.4
F	0	0.14	0	0
S	0.18	1.8	0.46	0
Cl	0.47	0.62	0.26	0.21
Ag	0.03	0.03	0.05	0.05
Te	0.06	0.07	0.06	0.07
Ni	31.1	25.9	20.7	20.9

Table 5.1: Composition of Ni films deposited by various methods from XPS data.

Measuring bulk impurities would be a better method to obtain this information. This was accomplished by sputtering the surface of the Ni films in-situ using an ion source, followed by taking XPS scans. Because this process occurs in an ultra-high vacuum, growth of an oxide monolayer takes substantially longer than measurement time. Figure 5.13 shows the results of this set of measurements, while Table 5.2 shows the composition of the films based on the analysis. The Ni peaks from these scans are significantly more pronounced than those in Figure 5.12. Additionally, the presence of impurity peaks has diminished leaving smoother curves. Analysis of the data shows the bulk of the films were primarily composed of Ni with several different impurities. The electron beam evaporated Ni had the highest purity, with no impurities reaching the roughly .1 % sensitivity limit of the equipment. This was expected due to the 99.995 % purity of the source material. The next purest film was the electroplated Ni, which incorporated some common elements including C, O, and N into the film. The small amount of Te in the film may be coming from the HgCdTe layer upon which the Ni was

deposited, however the source of the small amount of Ag found in the layer is unknown. Electroless Ni incorporated more C, O, and N than the electroplated film. The standard electroless process also resulted in a 5.8 % incorporation of B in the film which is in line with reported concentrations [71]. The electroless film with a reduced DMAB concentration of 3.75 g/L incorporated only 3.4 % B into the film. This allows for potential control over film stress and resistivity based on controlling B concentration and provides a lower bound on the amount of B incorporated in a film deposited by this technique. Additional analysis of the C peaks also showed they comprised primarily of C-C bonds. Overall, no explicitly detrimental impurities, such as Cu or In, were found in any of the films above the sensitivity level of the technique used. Based on this result, there are no red flags associated with attempting to deposit Ni into HgCdTe vias using either plating process.

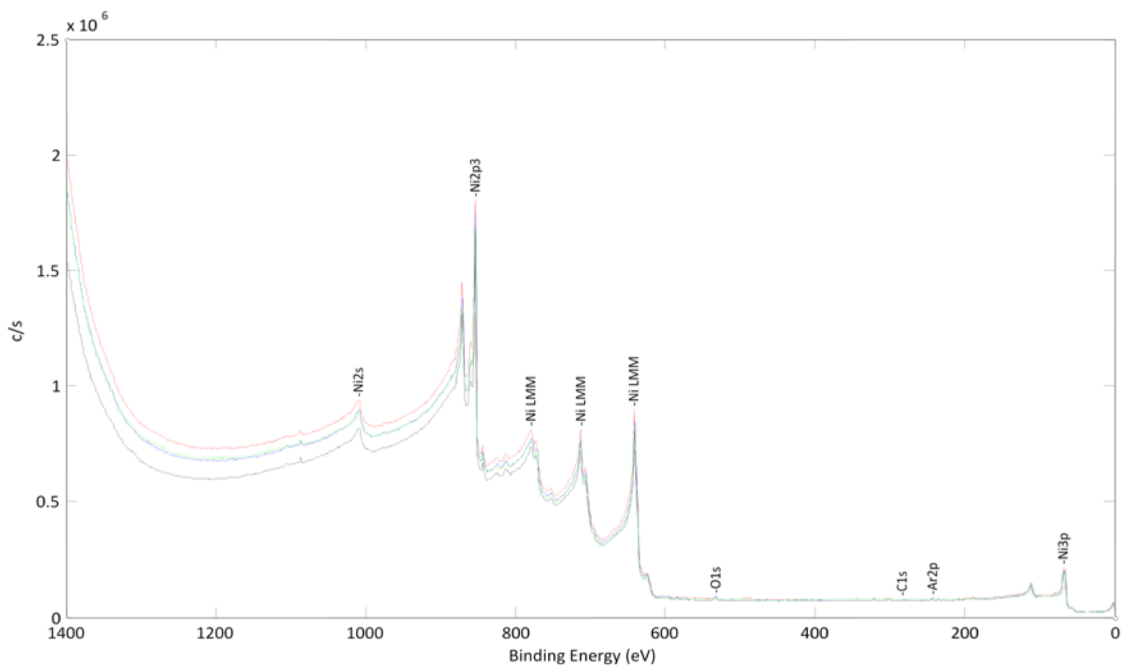


Figure 5.13: Wide XPS scans of Ni films deposited by various methods, post oxide removal.

Element / Sample	Electron beam Ni	Electroplated Ni	Stnd. electroless Ni	Reduced DMAB electroless Ni
B	0	0	5.82	3.36
O	0	2.53	5.84	5.98
C	0	1.73	4.1	7.49
N	0	2.08	1.7	2.27
Ag	0	.10	0.08	0.09
Te	0	.11	0.12	0.23
Ni	100	93.2	82.4	80.6

Table 5.2: Composition of Ni films deposited by various methods, post oxide growth from XPS data.

5.3.5 Resistivity of Plated Ni

Sheet resistance measurements using the four-point probe technique were taken on Ni films deposited directly onto HgCdTe/CdTe/Si. Samples were cross-sectioned and Ni films thickness was measured to calculate resistivity. Each type of Ni plating technique, which included electroplated Ni, standard electroless Ni, and reduced DMAB electroless Ni was tested and compared to electron-beam evaporated Ni as a baseline to ensure that resistivity was low enough to be a useful as a via contact metal. The resistivity measured for e-beam deposited Ni was 1.17 x 10^{-7} Ω-m, which is reasonably close to published values of 6.99 x 10^{-8} Ω-m [49]. The resistivities measured for electroplated, standard electroless, and reduced DMAB electroless Ni were 1.64 x 10^{-7} Ω-m, 1.49 x 10^{-6} Ω-m, and 1.72 x 10^{-6} Ω-m, respectively. The electroplated Ni resistivity was close to the 1.7 x 10^{-7} – 2.2 x 10^{-7} Ω-m values reported in the literature [102]. The

order of magnitude increase over electron-beam evaporated Ni is at least partially due to the inclusion of C, N, and O impurities found in the bulk of the Ni by XPS. The values obtained for electroless Ni were roughly an order of magnitude higher than those found in the literature, where 1.2 x 10^7 Ω-m was measured for a 3% B-Ni film [139]. No specific formulation of the Ni bath was given in the reference; however, this may explain the disparity between values. The increased value of resistivity of electroless Ni compared to other techniques is likely due to the addition of B in the film, which gives the film slight ceramic qualities. The small difference between the resistivity measured of the standard electroless Ni, which had a B concentration of 5.8%, and the low-DMAB Ni, which had a B concentration of 3.4 %, is counterintuitive. It would be expected that the standard electroless Ni film would have a noticeably higher resistivity due to increased B content. It appears that the inclusion of more C in the low-DMAB Ni offsets the reduced level of B with regard to resistivity. While these values are two orders of magnitude above those for electron beam evaporated Ni, all are within specifications for this application.

5.3.6 XRD Analysis of Plated Ni

Calculations of film stress using Stoney's equation, Equation 2.15, were made for each type of plated Ni film on both electron-beam evaporated Ni/Si and HgCdTe/CdTe/Si based on XRD rocking curve measurements. Stress was also tracked as the films grew thicker by several iterations of plating and measuring. Thickness of Ni films was measured from cross-sectional SEM images. The substrate thickness for both Ni/Si and HgCdTe/Si samples was 380 μm. For the (100) Ni/Si, standard values of E and ν for Si were used in the equation, which are 179 GPa for (100) Si [140] and .28 [141],

respectively. For (211) HgCdTe/CdTe/Si, several assumptions had to be made. First, the contributions of HgCdTe and CdTe on the values of E and ν were disregarded. This assumption works because the combined thickness of these layers is substantially smaller than the Si substrate, and they have significantly lower strength, therefore, their contributions are negligible. The second assumption is that the values of E and ν for (211) Si are the same as those for (100) Si. Because Si is an anisotropic crystal, these values differ for different crystalline orientations and directions of applied pressure [142]. Unfortunately, values are not available for (211) Si; therefore, calculations made based on these values are likely to be off, potentially by as much as a factor of 2. R_{pre} and R_{post} in Stoney's equation are calculated from the location of substrate peaks measured by XRD before and after plating. For HgCdTe/CdTe/Si samples, CdTe peaks were used since Si substrate sits well below the penetration depth of the x-rays.

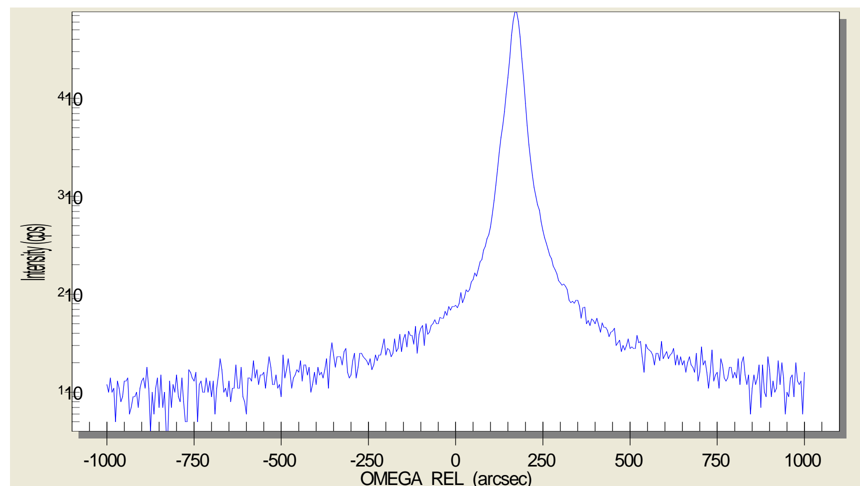


Figure 5.14: XRD rocking curve of the (400) Si peak.

Figure 5.14 is an XRD rocking curve of the (400) Si peak, where the absolute value of ω is 34.505°, and the peak is located at ω-rel of 170". This measurement was

repeated periodically across the sample to generate a map of peak locations, shown in Figure 5.15. The data was then plugged into Equation 2.14 to generate a value of R. Results of these measurements and calculations are shown in Figure 5.16, where the values of film stress for the different types of Ni are plated as a function of film thickness. For e-beam deposited Ni, a large tensile stress in a 1 μm film was measured, the largest magnitude of stress of any type of Ni. Electroless Ni from a solution containing 8 g/L DMAB was also found to be in tensile stress with almost an order of magnitude larger stress on Ni/Si than on HgCdTe/CdTe/Si. Only two measurements were made for electroless Ni on HgCdTe/CdTe/Si before the Ni layer began to crack and peel away, likely due to inferior adhesion with the material. Compressive stress was found in both the electroplated Ni sample grown on HgCdTe and the one on Ni/Si. The relatively low values of stress for films grown directly onto HgCdTe/CdTe/Si are critical due to the fragility of the material, as previously discussed. Based on this set of measurements, the electroplated Ni has superior stress properties when compared to electroless Ni for the application of via contacts. For the case of Ni plugs filling a via, the tensile stress found in electroless Ni will tend to want to pull the plugs in on themselves, resulting in open contacts if the adhesion of Ni to HgCdTe is not sufficient.

Figure 5.15: Si (400) peak location map used to generate a value for R.

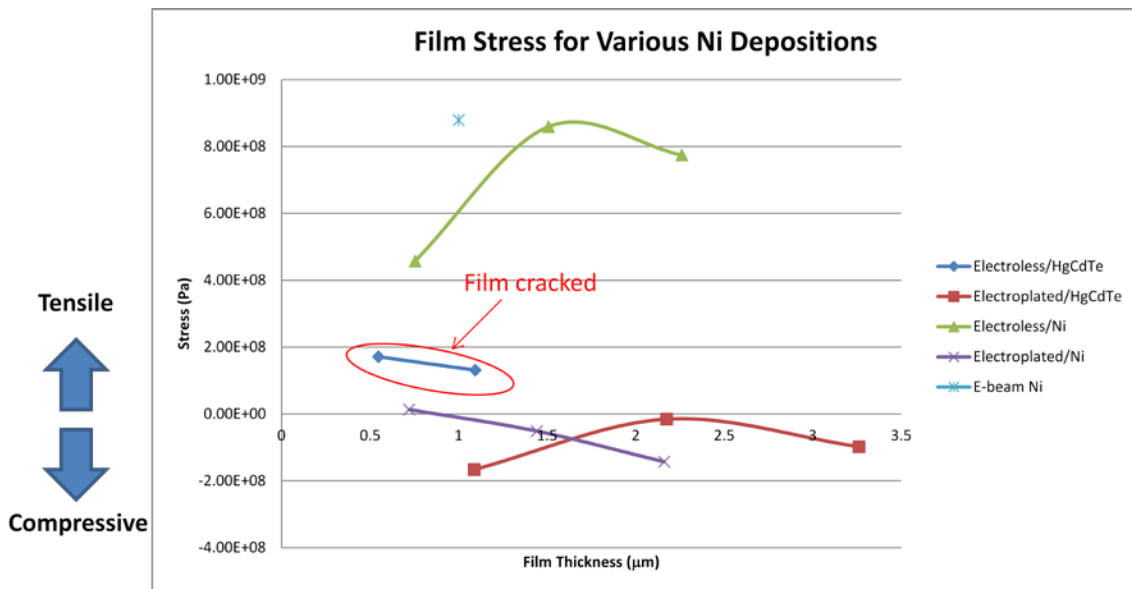


Figure 5.16: Stress as a function of film thickness of Ni deposited by various methods, calculated from XRD measurements.

The results of ω-2θ XRD measurements to determine crystallinity of the various type of Ni are shown in Figure 5.17. This included two measurements of electron-beam evaporated Ni, the first with the sample tilted several degrees. Also included are:

electroplated Ni on both Si and HgCdTe/CdTe/Si, and electroless Ni on both Si and HgCdTe/CdTe/Si. The plots for each type of Ni were offset in intensity to make the figure easier to interpret. Peaks were labeled, and their determination was made by applying Equations 2.12 and 2.13 to their location. For electron-beam evaporated Ni, both Si and Ni peaks showed up in the scans. Several unexpected peaks appeared in the scans, including what was ascertained to be the Si (200) peak. The (200) reflection for diamond cubic materials such as Si is forbidden, however, this peak appears due to double diffraction. Several Fe peaks appeared and were due to the steel plate upon which samples are affixed to. The Fe has a body-centered cubic (BCC) structure where allowed reflections are those for which the Miller indices add up to an even number. Two narrow peaks appear in the second Si scan and they may be due to dynamical diffraction effects from the near perfect Si substrate. The other scans all had Ni peaks, as well as either Si or HgCdTe peaks depending on the choice of substrate material. While the Ni peaks for the plated Ni/electron-beam evaporated Ni/Si may be from the evaporated Ni, the presence of similar peaks on the HgCdTe/CdTe/Si samples confirms that diffraction came from both types of plated Ni. Based on this set of measurements, the structure of both the electroplated and electroless Ni was polycrystalline, attributable to the presence of Ni peaks in the diffraction scans.

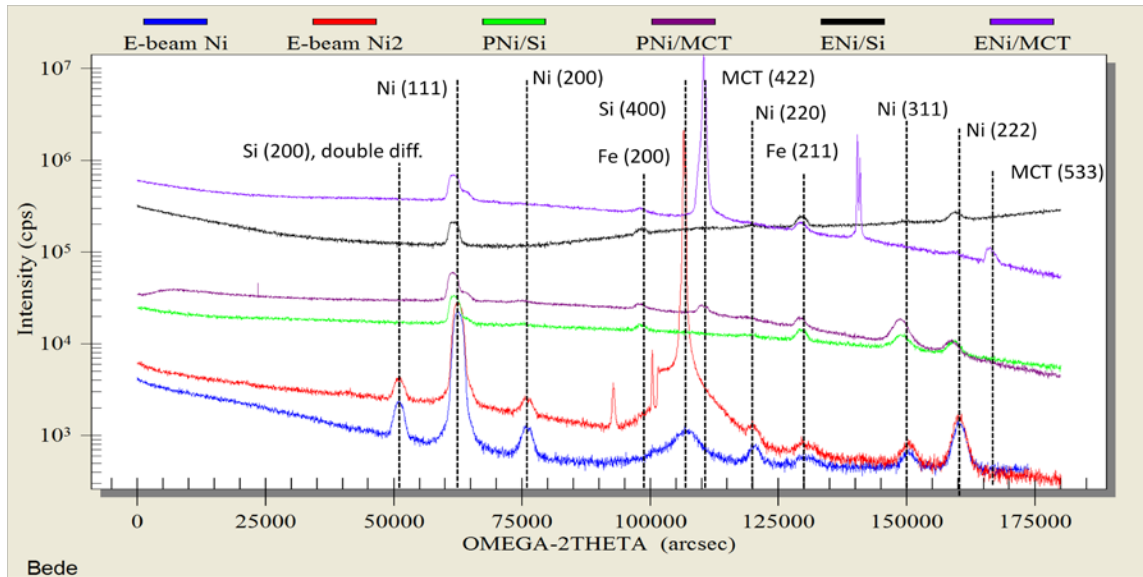


Figure 5.17: ω–2θ measurements of Ni films deposited by various methods on different substrates along with determination of peak reflections.

5.4 Plating of Mechanical Samples

5.4.1 Electroplated Ni

The results of electroplating Ni into the vias of a mechanical array are shown in Figure 5.18, where cross-sectional images were achieved by FIB milling followed by SEM. Figure 5.18a shows the entire region cut out by the FIB milling process with three mechanical vias cross-sectioned. Vertical streaks found on the image are an artifact of the milling process called curtaining, which is caused by changes in the sputtering rate as the ion beam passes over regions of different density [143]. A close-up of one of the Ni contact plugs along with labels of the structure is shown in Figure 5.18b. Photoresist remained on the sample to protect its surface from handling and processing. Like the dummy samples, the Ni contacts had high uniformity and had an increased plating rate at

the edges due to nonlinear diffusion. Good contact appears to have been made between the Ni and HgCdTe inside the via with no evidence of the plug pulling away which is explained by the fact that the plug is in a state of compressive stress based on XRD measurements.

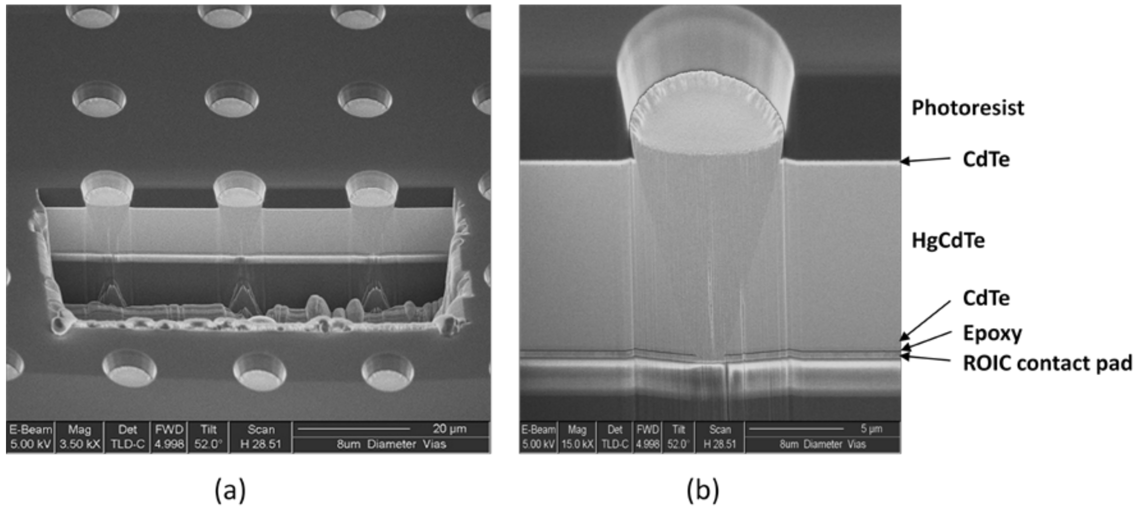


Figure 5.18: FIB/SEM images of an electroplated Ni array: (a) showing the entire milled region and (b) a close-up of one via.

5.4.2 Electroless Ni

Analogous images to those of Figure 5.18 are shown for electroless Ni contacts filling vias in a mechanical array in Figure 5.19. These images also show curtaining from the FIB process and Ni plugs that overplated past the CdTe/photoresist interface. High lateral uniformity was observed across the arrays; however, a faster growth rate was observed at one edge of the plugs. The region of faster plating was common to all the plugs in that it occurred in the upper left hand corner for each in Figure 5.19a. This was likely caused by specific way H bubbles evolved from the vias, based on the fact that the sample was held vertically in the plating solution. In addition to this, the surface topology

of the plugs differs from those formed by the electroplating process. Instead of a slightly concave top surface, the plugs are deeply grooved in the middle. This variation is due to the different way plating initiated on the inside surface of the via when compared with electroplating, as discussed in Section 5.3.2. Upon closer inspection of Figure 5.19b, it is clear that the Ni plug separated from the Ni seed layer below and partially pulled away from the inner surface of the via. Based on XRD results, the electroless Ni is under a tensile stress. Once the growth fronts of the Ni plug merged and continued to grow, the level of strain in the plug was greater than the adhesion to the via. When this strain was relieved by delamination, the plug was allowed to compress to an equilibrium state. Clearly, this is undesirable. Instead, the minimum necessary amount of plating should be performed where the contact metallization only needs to bridge the CdTe/epoxy gap between the contact metallization pad on the ROIC and the active HgCdTe of the array. The Ni would then act as more like a thin film, likely avoiding the strain problems associated with the thicker plug that acts as more of a bulk feature.

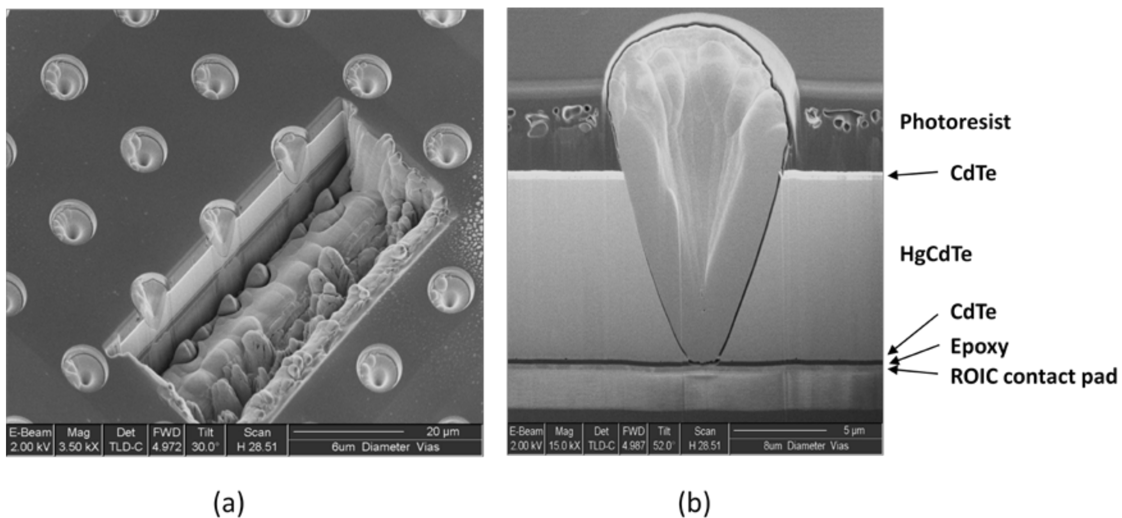


Figure 5.19 FIB/SEM images of an electroless Ni array: (a) showing nearly the entire milled region and (b) a close-up of one via.

5.5 Electroless Plating of Active Arrays

5.5.1 I-V Measurements of Plated Test Arrays

The standard electroless Ni process was used to form via contacts of test arrays. Electroplated Ni was not attempted from this point on because there was no means to connect the global ground pad on the test array to the cathode. As a reminder, the dimensions and structures of devices are the same as those found on mechanical arrays; however, the test arrays were epoxied to active ROICs. The results of I-V measurements taken of LWIR diodes with electroless Ni via contacts taken at 77 K are shown in Figure 5.20, where Figure 5.20a shows the initial data. Thinner Ni than that shown in Figure 5.19 was plated for this sample. Measurements were made with no illuminations to determine the dark current of devices. The data superimposes the I-V characteristics of the devices tested. The devices are diffusion-limited out roughly 250 mV with a low dark current, several are leaky based on the fact that their dark current is order of magnitudes higher. Cryogenic cycling of the sample, consisting of five dunks of the sample in LN, followed by warming back to room temperature, were performed on the sample. This data is shown in Figure 5.20b, where each of the devices maintain good connectivity and the performance of the devices with respect to dark current is unchanged. Finally, the devices were finally baked at 100 °C for five days to simulate a common vacuum bake-out step. Once again, both the status of the connectivity and the performance of the devices remained unchanged. From this data it is apparent that the electroless process successfully made stable contact between ROIC pads and the active HgCdTe of the FPA for high aspect ratio vias that did not alter the dark current performance of the diodes.

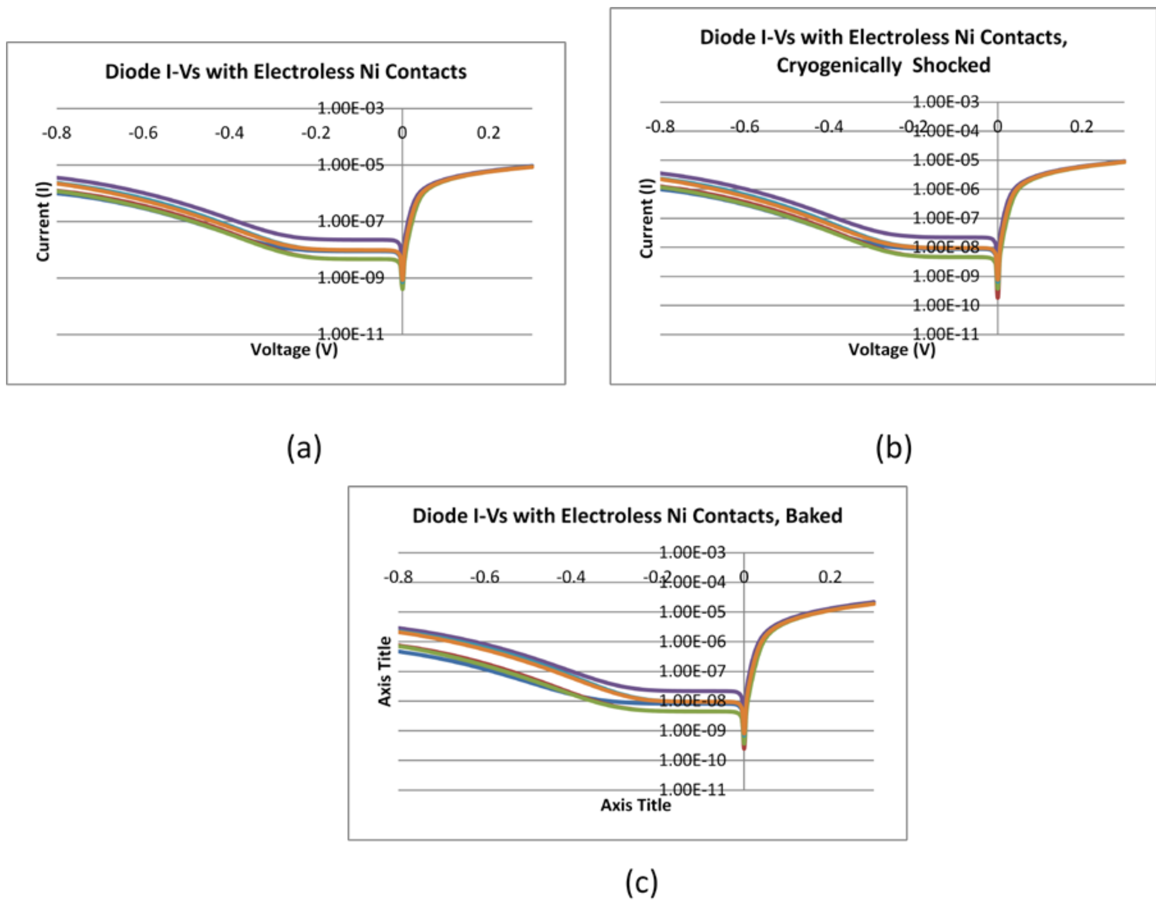


Figure 5.20: Dark current I-V curves of active diodes contacted by electroless Ni: (a) initial measurement, (b) post cryogenic cycling and (c) post 5 day 100 °C bake.

5.5.2 Electroless Ni for Active 5 µm Pitch Arrays

A final test of the electroless Ni process for via contacts involved plating and testing of active 5 µm pitch arrays in a 720p format. SEM images of a sacrificial array plated by this process and cross-sectioned is shown in Figure 5.21. Cleaving of the sample was not ideal due to the different mechanical properties of the layers involved, and FIB/SEM was not available for improved characterization. Figure 5.21a shows good uniformity of plated Ni across several hundred features. In Figure 5.21b, the top region of the Ni is exposed, revealing no evidence of pulling from the HgCdTe surface of the

via. Confirmation of plating down to the ROIC pad was made through a combination of Figure 5.21c-d, where the etch profile of the via through the epoxy is shown in Figure 5.21c. This etch profile is mirrored in Figure 5.21d, where the bottom of several Ni plugs is exposed. Like the mechanical arrays, the electroless Ni layer is thicker than desired due to the previously discussed issue of stress. An active FPA with 5 μm pitch diodes was then plated for a shorter amount of time.

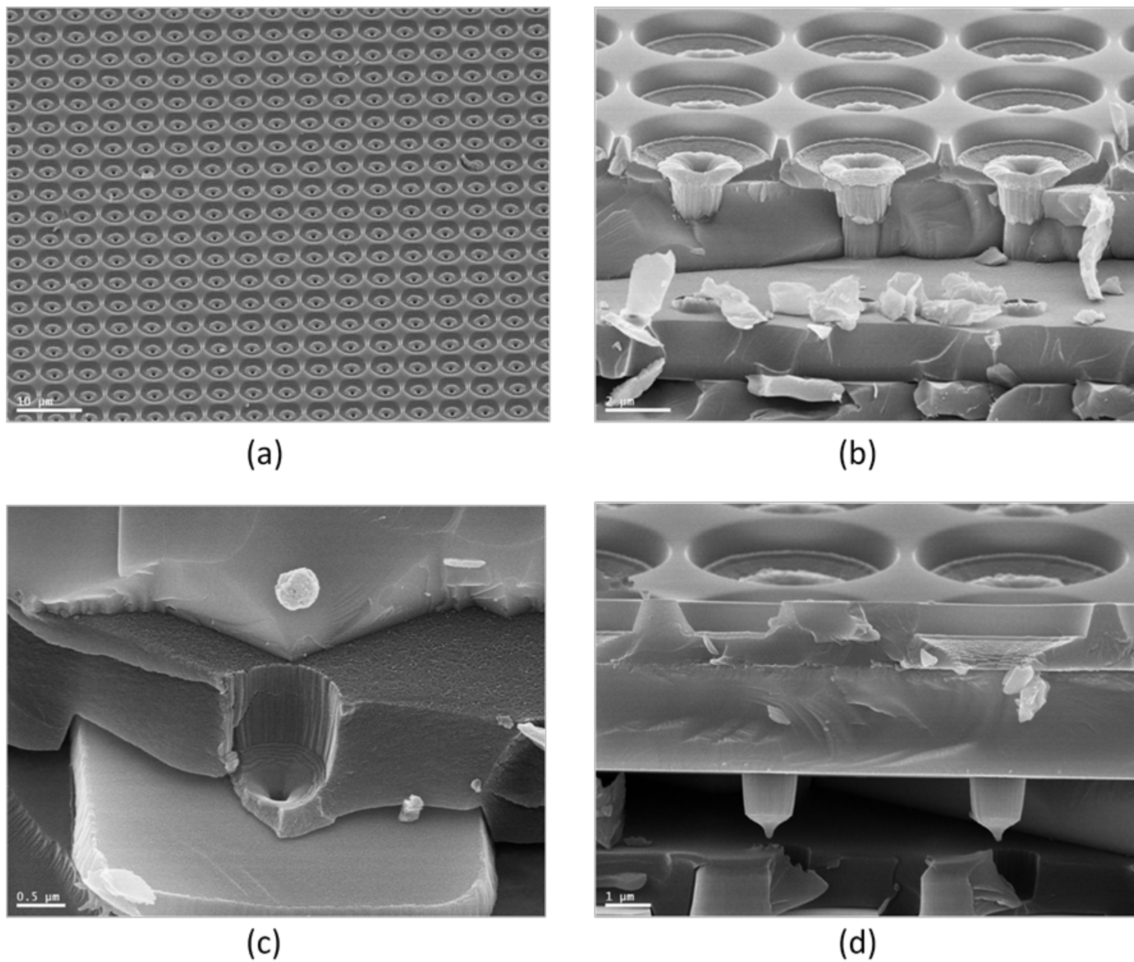


Figure 5.21: Electroless Ni plated sacrificial 5 μm array: (a) Several hundred pixels, (b) partially cross-sectioned vias, (c) cross-section of epoxy layer and (d) Image showing the bottom morphology of Ni plugs.

Figure 5.22 shows the results of optical images of the array before and after plating. Fringing can be seen in both images due to the photoresist left on the surface. From the images it is clear that a consistent ring of Ni appeared in each of the vias after the plating process. Images taken at several regions across the array also showed similar features. The ring filling the vias is thinner than the Ni plugs shown in the previous figure, which is desirable from a stress perspective.

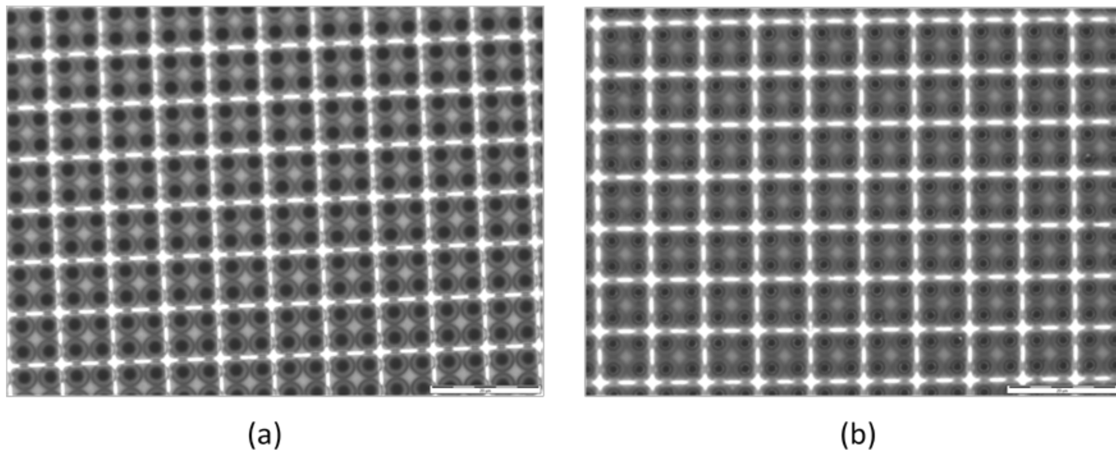


Figure 5.22: Optical image of active 5 μm pitch pixels: (a) before and (b) after electroless Ni process.

The results of electrical testing of an active array are shown in Figure 5.23, which shows the DC output of each pixel on the array. The periodic vertical lines appearing in the image are due to a bad output line on the ROIC, which occurred independently of the plating process. Of the 806,400 remaining pixels, there were 552 pixel outages, resulting in 99.93% connectivity. It is unknown whether these outages were due to the Ni plating process or to other aspects of the FPA fabrication so the connectivity value represents a worst case connectivity of the vias. These results are extremely positive and provide a strong proof of principle to further improve upon the process for manufacturing.

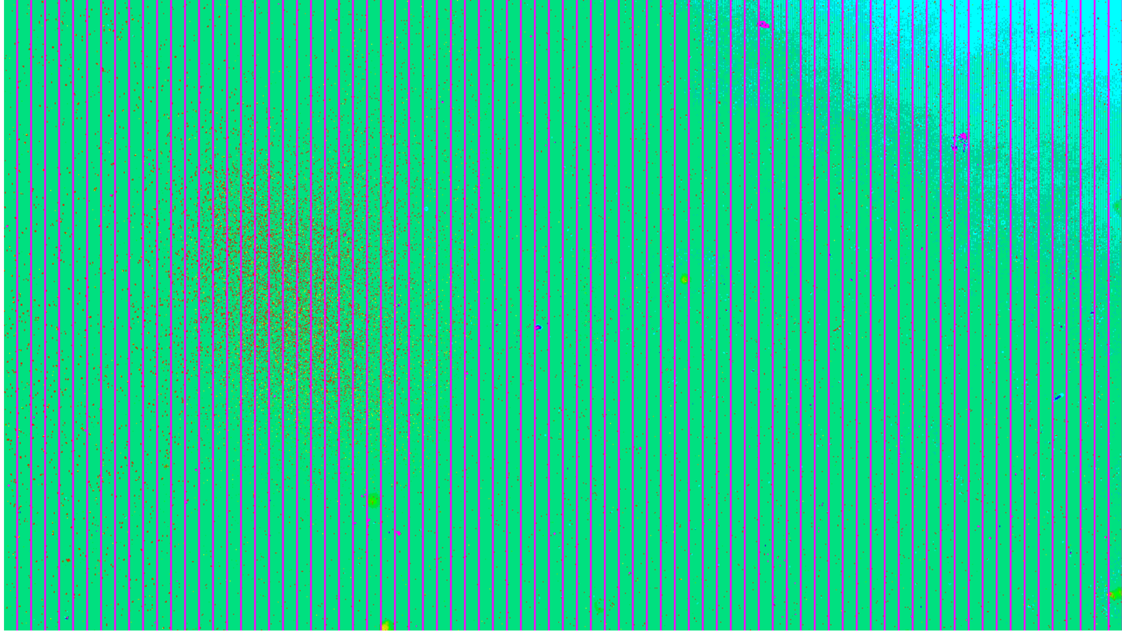


Figure 5.23: DC output of a 720p 5 μm pitch FPA fabricated with electroless Ni via contacts.

Chapter 6

Summary, Conclusions, and Future Work

Two novel backend processing techniques for infrared FPA interconnection were developed in this work. The first of these, for interconnection by In bumps, used a patterned template wafer upon which In bumps were electroplated. After forming these bumps, they could be transferred to the ROIC or detector array by an additional hybridization step, after which FPA hybridization could take place. This process differs significantly from current processing techniques that make use of a thick resist liftoff and evaporation of In to form bumps. A proof of principle for this transfer process was obtained at a 10 μm pitch. The second technique was applied to a class of FPAs with via type interconnects. Rather than using PVD processes to realize interconnect metallization, both electroplated and electroless Ni were investigated as an alternative. Electrical results from active 5 μm pitch FPAs were obtained with electroless interconnects that showed a high connectivity.

The significance of this work is the development of two new processes that allowed for pitch reduction of interconnects, potentially enabling the production of smaller pitch, higher resolution infrared FPAs. For In bump based FPAs, this was done by eliminating the thick resist liftoff step which limited the ability to produce high aspect ratio, small-pitch In bumps due to a variety of limitations. For via based FPAs, the line of sight requirements of PVD contact metallization resulted in a limitation of the minimum pixel pitch. By switching to electrochemical techniques, this limitation was removed.

The focus of Chapter 3 was patterning the amorphous fluoropolymer layer of the template wafer that determined the shape of the In bumps to be electroplated. The main goal of the patterning was to obtain features with a positive sidewall angle at a 10 μm pitch. A standard lithography and plasma etching process was initially investigated. Different Ar/O_2 gas mixtures as well as different plasma conditions did not yield the desired result as only vertical sidewalls and isotropic, undercut features were obtained. Instead, a process that embossed features in the fluoropolymer with a Si stamp was pursued. This required the fabrication of Si posts of the desired size with a positive sidewall angle. Such features were obtained with two different processes. The first one studied patterning of the Si stamp with a two step etching process. A DRIE step obtained pillars in the Si wafer with a vertical sidewall, which was followed by a short $HNO_3/HF/H_2O$ wet etch that allowed for control of the sidewall shape. The second process used a CHF_3 plasma to etch pillars with the desired shape. Both techniques successfully produced Si pillars at a 10 μm pitch with positive sidewall angles. Si stamps fabricated using both techniques were successfully used to emboss features in the amorphous fluoropolymer at pitches down to 6 μm pitch.

In Chapter 4, the remaining steps of the In bump transfer process were discussed. Due to the difficulty of electroplating In, a series of experiments was performed to optimize the lateral uniformity and grain size of the plated material. Pulse-plating was selected over DC plating due to its increased ability to tailor the morphology of plated features. An 84 mA/cm^2, 5 ms period, 20 % duty cycle pulse was found to produce the most laterally consistent bumps with a nearly flat top. After optimizing the electroplating parameters of the In bumps, the transfer of In from completed template wafers to

mechanical ROICs was attempted at 15 μm and 10 μm pitches. Several parameters, including: hybridization force, heating during transfer, In overplating thickness, reflow of In, amorphous fluoropolymer roughness, sidewall angle, and template wafer electroplating seed layer were varied to determine a window for transferring the In bumps from the template wafer. A proof of principle of the process was obtained at a 10 μm pitch. While transfer of bumps occurred using a variety of conditions, nonplanarity of the template wafer with respect to the mechanical ROIC dominated the quality of the In transfer process. Unlike modern flip-chip bonders, the bonder used did not have advanced leveling techniques and resulted in wedging between the two wafers when pressed together. This nonplanarity caused shorted regions adjacent to region with isolated transferred bumps adjacent to poorly transferred bumps, dominating most of the other parameters that were varied during experimentation.

Both electroless and electroplated Ni via contact metallization techniques were investigated in Chapter 5. Initial feasibility of each technique was performed on photoresist patterns with features similar in scale to FPA vias to ensure consistent Ni morphology and filling of features could be obtained. Compatibility of each plating solution to infrared FPA materials was also confirmed. Once feasibility was established, the basic properties of each Ni process were thoroughly investigated. This included: nucleation properties of the Ni to several underlayers, variation of plating parameters and the effect on plated Ni, surface analysis to determine Ni composition, resistivity of plated Ni, and XRD analysis to determine stress of the plated Ni as well as crystallinity. Optimized plating processes were then used to plate Ni contacts in mechanical FPA, followed by plating of active test structures. Good connectivity and thermal stability were

demonstrated for such structures. Finally, the electroless Ni process developed was used to form interconnects to active 5 μm pitch 720 p arrays, resulting in 99.94% connectivity.

Based on the positive results of the via contact metallization, continued development will be focused on improving the electroless Ni setup for improved process control, including improved temperature control, bath filtration, and controlled smaple agitation. Additionally, determination of thermal stability over thousands of thermal cycles of the plated Ni would provide further evidence of its suitability as an interconnect material for infrared FPAs. Outside of this, the loop has been closed for much of the research in this work. Once obtained, the goal of the work will be to transfer the technology for use in the infrared industry.

For the In bump interconnects, all effort will be focused on attempting the transfer process on a modern flip-chip bonder with a 20 μradian parallelism specification. It is anticipated that the use of such equipment would greatly improve the results of the process and allow for better optimization of template wafer parameters. Once accomplished, demonstration of the process on active arrays will be attempted.

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