ABSTRACT

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MICROSTRUCTURAL CHARACTERIZATION AND THERMAL CYCLING RELIABILITY OF SOLDERS UNDER ISOTHERMAL AGING AND ELECTRICAL CURRENT

Preeti S. Chauhan, Doctor of Philosophy, 2012

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Solder joints on printed circuit boards provide electrical and mechanical connections between electronic devices and metallized patterns on boards. These solder joints are often the cause of failure in electronic packages. Solders age under storage and operational life conditions, which can include temperature, mechanical loads, and electrical current. Aging occurring at a constant temperature is called isothermal aging. Isothermal aging leads to coarsening of the bulk microstructure and increased interfacial intermetallic compounds at the solder-pad interface. The coarsening of the solder bulk degrades the creep properties of solders, whereas the voiding and brittleness of interfacial intermetallic compounds leads to mechanical weakness of the solder joint. Industry guidelines on solder interconnect reliability test methods recommend preconditioning the solder assemblies by isothermal aging before conducting reliability tests. The guidelines assume that isothermal aging simulates a "reasonable use period," but do not relate the isothermal aging levels with specific use conditions. Studies on the effect of isothermal aging on the thermal cycling reliability of tin-lead and tin-silver-copper solders are limited in scope, and results have been contradictory. The effect of electrical current on solder joints has been has mostly focused on current densities above $10^4 A/cm^2$ with high ambient temperature ($\geq 100^oC$), where electromigration, thermomigration, and Joule heating are the dominant failure mechanisms. The effect of current density below $10^4 A/cm^2$ on temperature cycling fatigue of solders has not been established. This research provides the relation between isothermal aging and the thermal cycling reliability of select Sn-based solders. The Sn-based solders with 3%, 1%, and 0% silver content that have replaced tin-lead are studied and compared against tin-lead solder. The activation energy and growth exponents of the Arrhenius model for the intermetallic growth in the solders are provided. An aging metric to quantify the aging of solder joints, in terms of phase size in the solder bulk and interfacial intermetallic compound thickness at the solder–pad interface, is established. Based on the findings of thermal cycling tests on aged solder assemblies, recommendations are made for isothermal aging of solders before thermal

cycling tests. Additionally, the effect of active electrical current at 10^3 A/cm^2 on thermal cycling reliability is reported.

MICROSTRUCTURAL CHARACTERIZATION AND THERMAL CYCLING RELIABILITY OF SOLDERS UNDER ISOTHERMAL AGING AND ELECTRICAL CURRENT

By

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Dedication

To my mother Mrs. Kalpana Chauhan, my sister Mrs. Deepika Chauhan Thapar and brother Mr. Digvijay Singh Chauhan for helping me this far in my career – AND my beloved father Late Mr. Bodhpal Singh Chauhan.

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1 Chapter 1: Introduction

Solder joints on printed circuit boards provide electrical and mechanical connections between package electronic devices and metalized patterns on the boards. Solder joint reliability is critical for the reliability of electronic packages [1]. During their usage life, solder joints are often subjected to cyclic loading due to temperature excursions and mechanical loads such as shock and vibration. Thermal cycling tests are conducted to evaluate solder joint reliability under thermal fatigue loading, whereas mechanical tests investigate solder joint reliability under shock, vibration, bend, and torsion. Prior to the ban on the use of lead (Pb) in most consumer electronic products [2], SnPb solder was used in the majority of solder interconnections in electronic equipment. Eutectic SnPb solder offered the advantages of a single melt and solidification point at 183^{o}C and known manufacturing, and reliability characteristics.

Studies on SnAgCu (SAC) solders, which are being used as replacements for SnPb, have shown a greater dependence on the reliability of isothermal aging [3–8]. This dependence on isothermal aging is likely due to the changes in the bulk solder microstructure as well as interfacial IMC growth at the solder-substrate interface due to aging. The evolution of interfacial and bulk IMCs as well as bulk grain structure must be understood when interpreting the influence of various isothermal aging conditions on solder joint reliability.

Sections 2–4 discuss the meaning and purpose of preconditioning and current recommendations presented in industry guidelines and standards on solder

preconditioning. Section 5 discusses the current industry practices for the preconditioning of solders. The effects of preconditioning on solder joint microstructure and reliability are discussed. A summary of the isothermal aging studies conducted by various researchers, including our present work, is provided. The gaps in the current understanding of preconditioning by isothermal aging are discussed in section 6, and recommendations are provided (section 7) based on the literature review and our present work.

1.1 Solder Joint Preconditioning

Preconditioning is a well-established practice adopted in the electronics industry. The purpose of preconditioning is to simulate the conditions of the product life cycle, handling, and aging during storage and service life. According to IEC and IEEE standards [9–10], aging is defined as "the occurrence of irreversible, deleterious changes in systems which affect their serviceability, i.e., their ability to satisfy requested performances." Aging of any kind (temperature, mechanical loading) is assumed to lower reliability. Fellman [11] discussed preconditioning by multiple reflows and its subsequent impact on the reliability of vias under interconnect-stress testing (IST). Many times preconditioning can be a complex multistep process. For instance, the JEDEC-22-A113D standard [12] prescribes preconditioning for non-hermetic surface mount devices to represent a multiple solder reflow operation.

Solder joint preconditioning is a widely adopted industry practice that accommodates the aging effects in solders joint before carrying out reliability tests. The aging of solder joints during storage and operation is referred to as solid-state aging. These environments may involve room temperature and/or high temperature

conditions. Many present-day electronic systems are subjected to long service at high temperature levels [13]. Aging under such conditions may change the bulk and interfacial microstructure, in turn changing the mechanical properties and reliability of solder joints. Current preconditioning practices for solder interconnects include subjecting test specimens to test conditions such as multiple reflows, thermal cycling and isothermal aging. For instance, IPC9701A [14] and GEIA-STD-0005-3 [15] recommend solder joint preconditioning by isothermal aging before conducting reliability tests on the test assemblies. The term "preconditioning" used in this chapter henceforth refers to isothermal aging at elevated temperature.

1.2 Purpose of Solder Joint Preconditioning

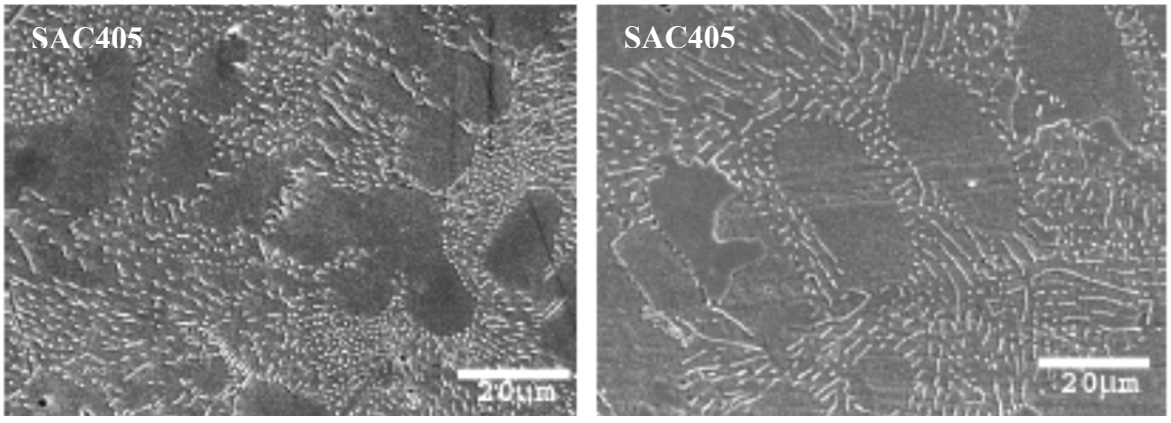
The rationale behind preconditioning solder joints before reliability tests depends on the purpose of the test. Presented below are the two main reasons for preconditioning by isothermal aging: to gain consistency among test solder assemblies, and to accelerate degradation of solder joints to simulate service life.

1.2.1 Gain Consistency among Test Solder Assemblies

Often electronics reliability engineers have to test assemblies from different manufacturing lines. These components often reach the test facility after undergoing different periods of storage. Since the solder microstructure is inherently unstable and undergoes evolution with time, it would result in different microstructures for test assemblies coming from different manufacturing lines. When carrying out reliability tests on these assemblies, it is imperative to bring them to the same state in terms of microstructural evolution and stress state. The standards and industry guidelines

mentioned in the previous section also assume that preconditioning by isothermal aging helps to gain consistency among the test vehicles by helping the grain structures to attain similar characteristics.

Solder joints exhibit a continuously evolving microstructure with time [16]. Because changes in microstructure in formed solder joints occur through solid-state diffusion, the temperature of the solder joint is important. As seen in Figure 1.1(a), the initial microstructure (as reflowed) of SAC405 is extremely fine, but it coarsens significantly within 9 days of room temperature (25^{o}C) aging. Similarly, for SnPb solder (Figure 1.1(b)); both Sn and Pb-rich phases coarsen within 9 days of room temperature (RT) aging. In order to characterize solder joint properties, it is necessary to set a baseline for comparison in terms of temperature and time. Here, preconditioning is used to bring the solder joint samples to the same state in terms of their microstructure properties such as interfacial IMC thickness and IMC phases in the solder bulk.



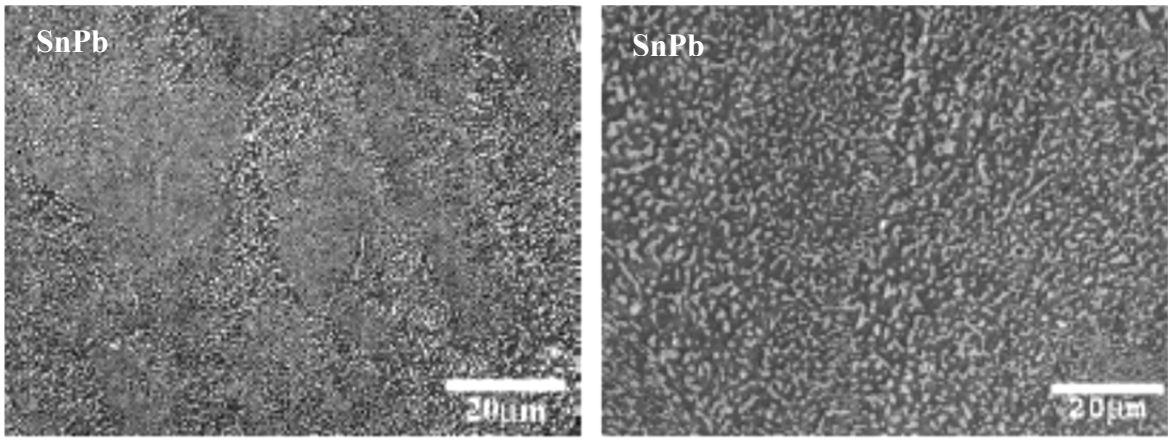


Figure 1.1: **Effect of RT aging (9 days) on microstructure of (a) SAC405 and (b) SnPb solder [16]**

1.2.2 Accelerate Degradation of Solder Joints to Simulate Service Life

In most cases it is not feasible to carry out reliability tests for the entire lifetime of electronic products. Hence preconditioning may be performed to simulate solder joint microstructures that are expected after several years of operating life. This preconditioning often relies on high temperature aging. One of the consequences of high temperature aging is the growth of IMCs in the solder bulk and interfacial regions. Interfacial voiding at the IMC-substrate interface has also been observed with long-term aging at elevated temperatures ($\geq 100^{o}$C). Interfacial voiding along with the thicker interfacial IMCs can cause solder joint failures at the solder–IMC interface [17].

In solder aging studies, changes in the solder characteristics, such as interfacial IMC thickness, and changes in the electrical or mechanical properties of solders are examined as a function of aging. The level of change in the monitored characteristics for a particular temperature and duration is assumed to represent the solder joint working life of a certain number of years. Vianco and Rejent [18] proposed a

methodology to assess the isothermal aging of SnPb solder on the basis of interfacial intermetallic compound thickness and changes in the size of Pb-rich phase. They established a baseline in terms of the interfacial IMC thickness in the "as fabricated" specimens and proposed a model for IMC growth and phase coarsening for aging temperatures up to 100^{o}C. Choubey *et al.* [19] conducted studies in which interfacial IMC thickness at the board side was monitored over the aging time, and the IMC thickness was reported to represent the IMC thickness level obtained after a service life of a few years.

1.3 Recommendations from Industry Standards on Solder Preconditioning

Various industry guidelines and standards call for preconditioning of solders prior to reliability testing. The IPC guideline for accelerated reliability testing of surface mount solder attachments, IPC-SM-785 [20], recommends that FR4-based solder joint test assemblies be subjected to 100^{o}C for 300 hours and that polyimide-based solder test assemblies should be subjected to 125^{o}C for 100 hours. It states that the test vehicles should be assembled and processed in a way similar to the actual product in terms of grain structure, composition, and IMC thickness. Since microstructure changes with time in actual products, it is imperative that test vehicles should start with solder joints that are more representative of solder joints in products after some period of operation. IPC-9701(A) [14] calls for aging at 100^{o}C for 24 hours.

The rationale provided by the above IPC guidelines is that "aging simulates a reasonable use period and accelerates such possible processes as solder grain growth, intermetallic compound growth, and oxidation." IPC-9701 recommends additional aging for "some" additional time at room temperature before fatigue testing to further

stabilize the solder structure. GEIA-STD-0005-3 [15] calls for aging at 100°C for 24 hours. Similar to IPC guidelines, GEIA-STD-0005-3 states that preconditioning is an effective means of replicating the changes that occur during the lifetime of a solder joint. The changes include diffusion-driven voids, segregation, and oxidation, in addition to the changes mentioned by IPC-9701. These documents also assume that isothermal aging helps to gain consistency among test vehicles by helping the solder grain structures to attain similar characteristics.

1.4 Effects of Preconditioning on Lead-free Solders

Current industry practices for preconditioning of solder joints involve choosing aging temperatures in the range of 50–150°C, except for some very high temperature applications such as automotive, military, oil, and aerospace, where aging at temperatures up to 200°C is used. The effect of isothermal aging on solder interconnect reliability is governed by the changes in solder bulk microstructure and interfacial IMC thickness with aging temperature and aging duration. Isothermal aging leads to an increase in IMC thickness at the solder joint interfaces. In the solder bulk, enlargement of Pb and Sn-rich regions occurs in SnPb solders; in SAC solders, coarsening of intermetallic particles (Ag_3Sn and Cu_6Sn_5) occurs.

1.4.1 Changes in the Interfacial IMC Thickness and Bulk Microstructure

It is well established [21–24] that IMC growth is a diffusion-controlled phenomenon highly dependent on temperature. Interfacial IMC bonds the solder to the connecting substrates, resulting in a strong metallurgical bond. On the other hand, bulk IMC stiffens the solder. Solder preconditioning changes the size and structure of

IMCs present in both the bulk and the solder joint interfaces. Figure 1.2 shows a comparison of interfacial IMCs in unaged and aged SnPb solder at the solder-Cu (OSP) interface in 2512 resistors. It can be seen that elevated temperature aging results in smoother and thicker interfacial IMCs compared to those in specimens stored at room temperature. The scallop-like IMC structures become uniform and smooth with aging. Also, high temperature aging results in enhanced growth of additional IMC phase, Cu_3Sn between the copper substrate and the Cu_6Sn_5 IMC, as seen in Figure 1.2. Generally, Cu_3Sn cannot be observed (under SEM) at aging temperatures below 100°C due to slow growth rate.

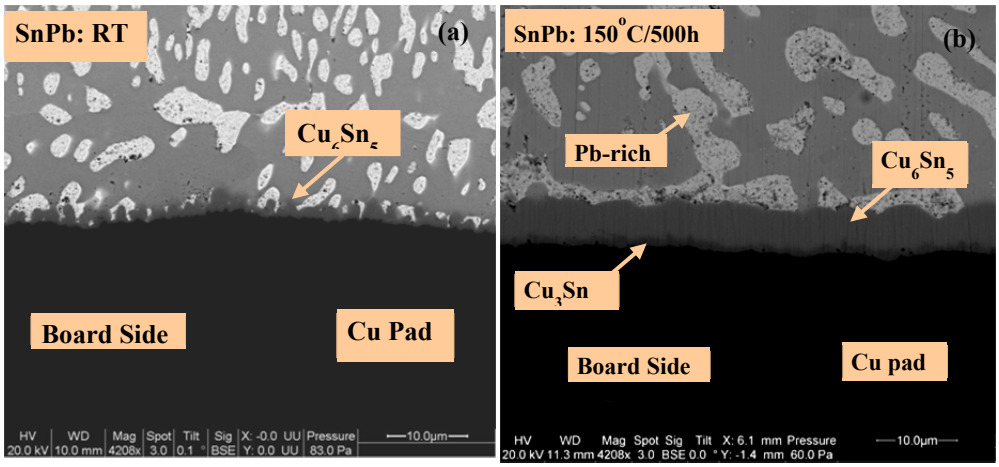


Figure 1.2: SnPb aged at (a) room temperature and (b) 150°C for 24 hours.

As the IMCs grow during solid-state aging, a thick interface between the solder and substrate is formed. The thick interfacial IMC reduces the ductility of the entire joint and can promote interfacial failures. Interfacial failures could be further promoted by the occurrence of interfacial voiding at the IMC-substrate interface. For long-life products and products subjected to sustained elevated temperature, IMC formation and growth can be an important consideration. A comparison of interfacial

IMC thickness in as-reflowed solders reveals that SAC solder joints have thicker IMCs than eutectic SnPb solder joints due to their higher reflow temperature and Sn content. Several researchers have conducted studies on the effects of elevated temperature isothermal aging on IMC formation and growth with various lead-free solders and pad finishes [25–29]. Lee *et al*. [30] aged Sn3.5Ag, Sn3.8Ag0.7Cu, Sn0.7Cu, and eutectic SnPb solder alloys at 125, 150, and 170^{o}C for 500, 1000, and 1500 hours. Since the growth of IMCs is a diffusion-controlled reaction, the rate of growth is expected to be influenced by initial IMC interface, percentage of participating elements, and temperature. In solid-state aging, the growth rate of IMCs in SnPb is faster that in SAC solder, where higher temperature implies higher growth rate. In a study by Chou [25], eutectic SnPb and near-eutectic SAC solder joints on the Au/Ni/Cu substrates in BGA packages were compared after thermal aging treatments at 150 and 170°C. Chou reported that SnPb had a higher IMC growth rate than SAC solder.

Another effect of elevated temperature isothermal aging is the coarsening of solder bulk. Solder bulk in SAC solders on OSP(Cu) substrate typically consists of two types of IMCs: Ag_3Sn and Cu_6Sn_5, as shown in Figure 1.3. Figure 1.3(a) shows the hexagonal structure of Cu_6Sn_5 IMCs in a solder void. Due to the presence of the void, the three-dimensional structure of a Cu_6Sn_5 IMC can be seen. Figure 1.3 (b) shows the Ag-Sn and Cu-Sn IMCs in the solder bulk.

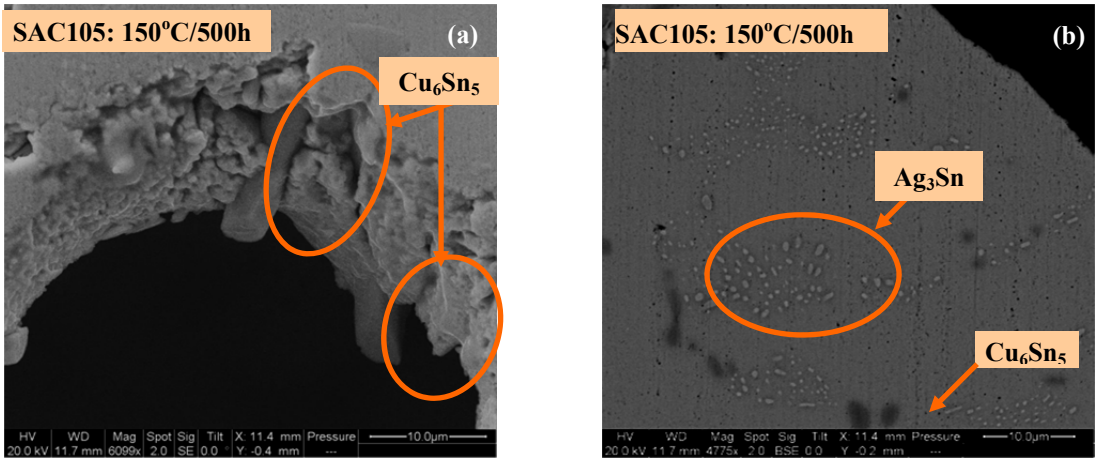


Figure 1.3: IMCs in SAC105 solder (a) and (b).

Several researchers [8, 31-33] have reported the microstructural coarsening effects due to isothermal aging of solders. Tian *et al.* [34] investigated the effects of isothermal aging at 150°C for 4, 48, and 120 hours on SAC BGA parts with SAC305 solder on Au/Ni/Cu finished pads. Due to the presence of Au in the solder pad, $AuSn_4$ was present along with the Ag_3Sn and Cu_6Sn_5 intermetallic compounds in the bulk. It was reported that during aging the coarsening of $AuSn_4$ took place, and its morphology changed from needle-shaped structures to plate-like structures, while no observable coarsening was observed in Ag_3Sn. Xiao *et al.* [8] reported that the microstructure of SAC changed significantly after 35 days of storage at room temperature. Chou *et al.* [25] reported that there was significant phase coarsening in the bulk region of thermally aged SnPb solder joints. Figure 1.4(a-d) shows the results of an isothermal aging study conducted by CALCE on 2512 resistors assembled with SAC305 solder and ENIG(Cu) substrate. Microstructural coarsening was observed in the Sn-rich regions as well as $AuSn_4$ IMCs after aging at 24, 600, and 1000 hours of thermal aging at 150°C. It can be seen that Ag_3Sn IMCs coarsened

with aging at 150°C. The size of Cu_6Sn_5 IMCs did not change much due to aging at 150°C for up to 1000 hours due to the diffusion barrier of nickel at the solder–pad interface.

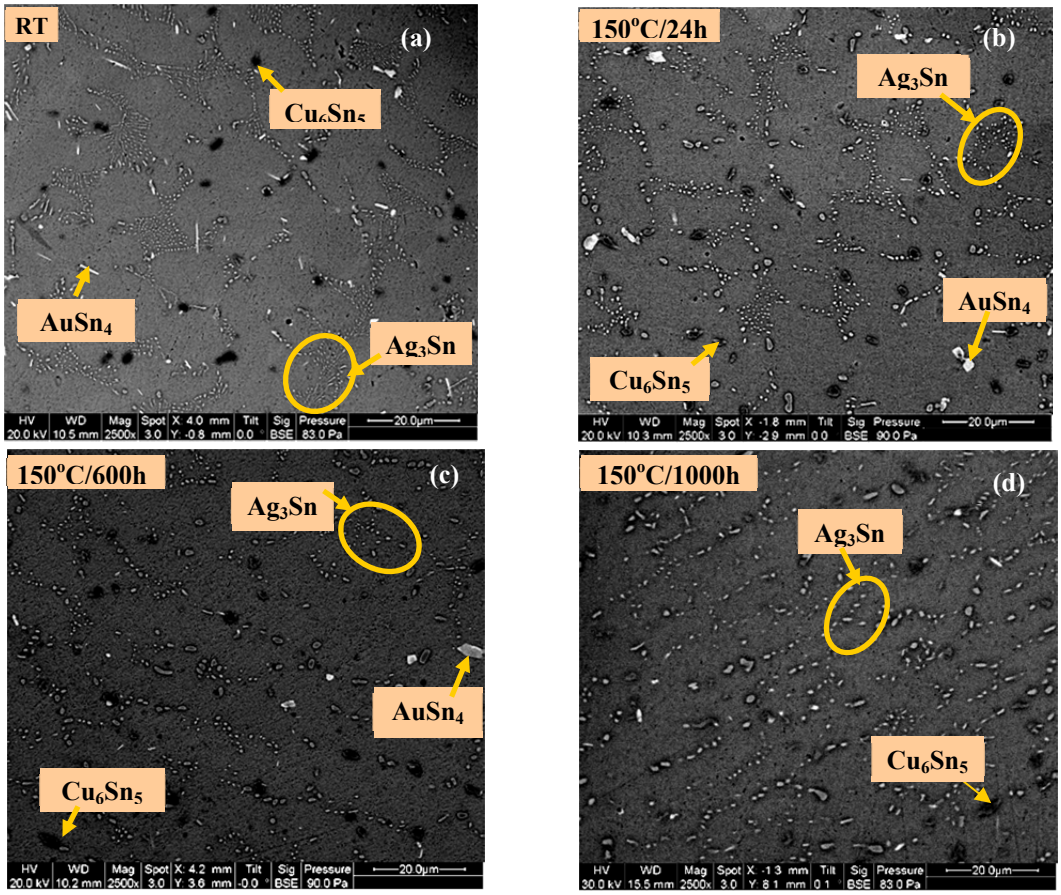


Figure 1.4: SAC305/ENIG aged at (a) RT and 150°C for (b) 24 hours, (c) 600 hours, and (d) 1000 hours.

The microstructural examination of SnPb solder on ENIG(Cu) substrate after long-term aging at 150°C was also carried out. It can be seen in Figure 1.5(a-d) that the SnPb microstructures of the RT and the 150°C/24 hour-aged specimens are similar. As the aging time was increased to 600 hours, a significant coarsening of Pb-rich phases was observed. However, no significant difference in the microstructures of the samples aged for 600 and 1000 hours was observed. This suggests that a

saturation point was achieved somewhere between 600 and 1000 hours, because of which further coarsening of the Pb-rich phase ceased. It can also be seen in Figure 1.5(a-d) that the SnPb microstructure consists of both small and large Pb-rich regions. The coarsening occurs selectively in some regions in the solder bulk.

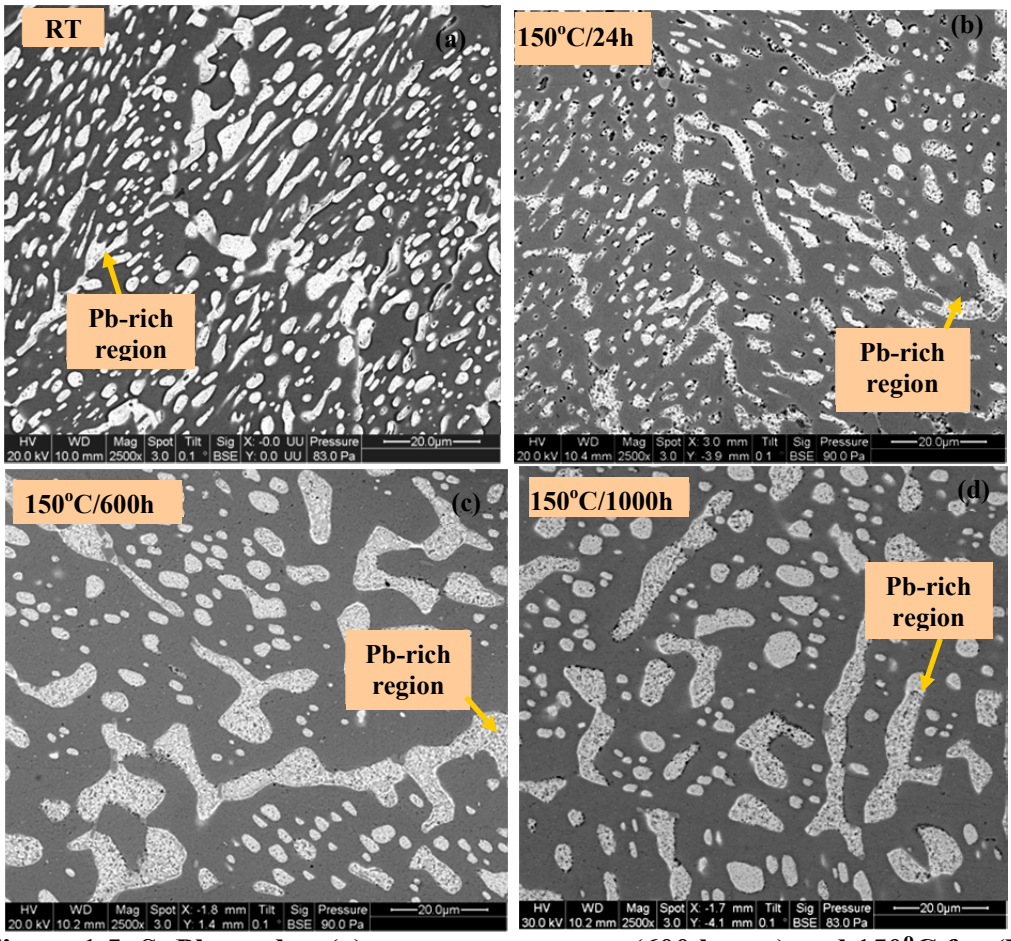


Figure 1.5: SnPb aged at (a) room temperature (600 hours) and 150°C for (b) 24 hours, (c) 600 hours, and (d) 1000 hours.

Choubey *et al.* [32] investigated the effects of isothermal aging at 125ºC for 100, 350, and 1000 hours on mixed solder joints formed by attaching SAC solder balls of a ball grid array (BGA) component using SnPb solder. They reported that the mixed solder joints were more resistant to coarsening phenomena and resulted in joints with

better thermal fatigue resistance compared to eutectic SnPb joints. Other researchers [35-36] have reported similar findings.

IMCs present in the solder bulk can also influence the solder interconnect reliability. These IMCs can act as barriers for crack propagation and therefore can increase the reliability of solder joints under low strain rate loading [37]. Figure 1.6(a-b) shows fatigue cracks in an SAC305 solder interconnect formed between a 2512 tin-finished resistor and OSP(Cu) pad subjected to thermal cycling from -55 to 125^{o}C (15 min dwell at both ends, ramp rate of 10^{o}C/min). IMCs block the crack propagation and divert the path of crack propagation, leading to the branching of cracks. It can therefore be seen that the role of IMCs in solder joint reliability cannot be characterized as being entirely detrimental.

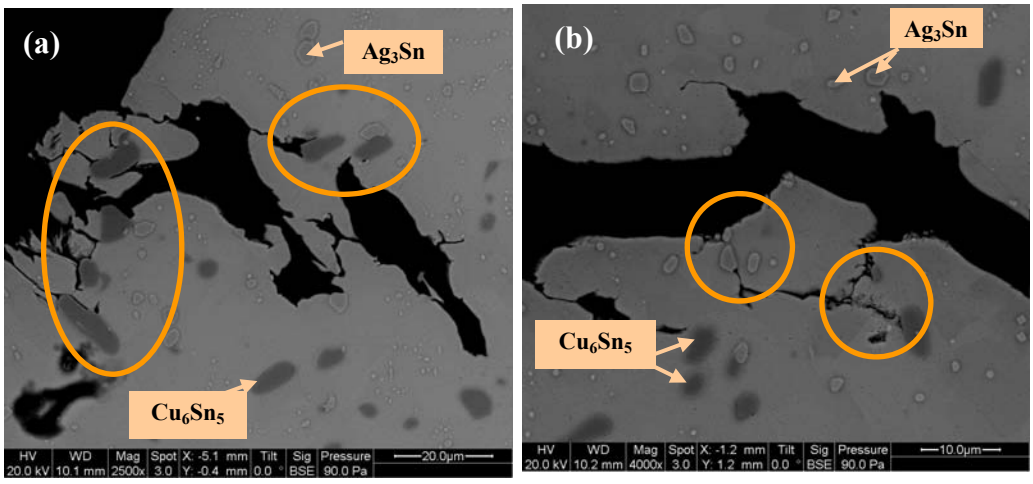


Figure 1.6: Role of IMCs in crack propagation (-55 to 125^{o}C thermal cycling test) in SAC305 solder joints aged 150^{o}C/500 hours.

Another effect often associated with high temperature aging is the formation of Kirkendall voids [38–40] at the Cu_3Sn/Cu interface in solder joints. The formation of Kirkendall voids can be detrimental to solder durability since they make the interfacial IMC layer the primary failure site under reliability tests. While Kirkendall

voiding is a diffusion-driven process, material selection likely plays a significant role. Kirkendall voids were reported to form due to unbalanced Cu-Sn interdiffusion through the interface [38]. However, recently Yu *et al.* reported [41] that Kirkendall voiding is associated with the presence of sulfur in plating from the inclusion of SPS (bisodium sulfopropyldisulfide, $C_6H_{12}O_6S_4Na_2$) in the plating bath during immersion silver coating. This suggests that Kirkendall voiding is mostly a material selection issue. In the present work, aging studies carried out in the temperature range of 50–150^{o}C for up to 1000 hours on SAC305, SAC105, SN100C, and SnPb solders did not report on Kirkendall voiding. Kirkendall voids should not be confused with another kind of voiding observed in solders known as Champagne voiding. Champagne voids occur between the IMC and the bulk solder. These voids form during the solder joint formation process and are associated with ImAg finishes (see Figure 1.7) due to the presence of the organic material added to prevent Ag tarnishing.

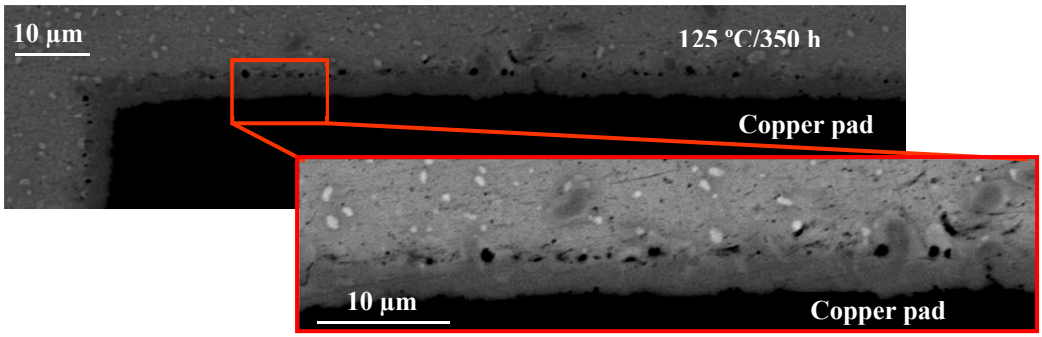


Figure 1.7: Champagne voiding in SAC solder assembled with ImAg board finish

Improved ImAg finishes have been developed to eliminate this type of voiding. In the present work we observed voiding in solders assembled with OSP finish as well. Figure 1.8 shows the interfacial voiding in SAC305 solders aged at 100^{o}C for 2000 hours.

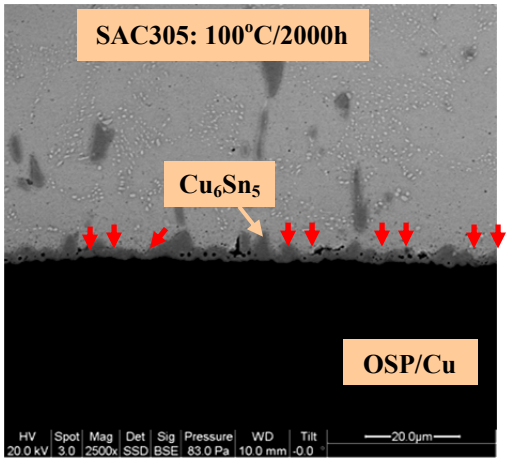


Figure 1.8: Voiding in aged SAC305 solder (arrows indicate voiding).

These voids were present in the solder–IMC interface and also within the Cu_6Sn_5 IMC layer. By the nature of the location of these voids, they cannot be categorized as Kirkendall voids or Champagne voids.

1.4.2 Reliability Implications of Solder Joint Preconditioning

Reliability tests can be broadly classified into two categories on the basis of strain rates: high strain rate tests and low strain rate tests. Vibration, drop tests, and shock tests are classified as high strain rate tests. Tests such as the cold bump pull test and shear tests can be low or high strain rate tests depending on the strain rate. The temperature cycling test, bend test, and torsion test are generally referred to as low-strain rate tests. Elevated temperature isothermal aging may have different effects on the reliability of solder joints under high strain rate and low strain rate loadings. Failures in high strain rate tests occur primarily at the solder–IMC or IMC1–IMC2 interface, whereas the failures in low strain rate tests occur primarily in the solder bulk. Researchers [39, 40] have also reported that in mechanical tests, such as shear

tests and pull tests, the failure can shift from the bulk to the interface by changing the strain rate of the loading.

1.4.3 Preconditioning for Low Strain Rate Reliability Tests

Low strain rate reliability tests aim to determine the life expectancy of solders under low strain rate thermal cycling, bend, and torsion. Failures in such tests are primarily found in the solder bulk since at a low strain rate the stress is not high enough to deform or cause failure in the IMC. The shear test is used to assess the solder strength and quality. In general, thermal aging reduces the solder strength under shear tests [**1**, 31, 42]. **Table 1.1** summarizes the findings from the literature review on the effects of thermal aging on solder reliability under low strain rate reliability/strength tests.

Table 1.1: Preconditioning for Low Strain-rate Strength/Reliability Tests

Paper	Test/ strain rate	Solder/ pad finish /component	Aging temp/duration	Failure site	Results
Oliver *et al.* [1], 2003	Shear	SAC and SnPb NiAu	25, 100 and 150°C for 200, 500 and 1000 hours		1. At 25°C, the shear strength of SnPb solders was higher than that of SAC solders. 2. At 100 and 150°C, SnPb alloys lost their shear strength rapidly. SAC alloys showed a decrease in shear strength but were relatively stable with respect to the increasing aging times.
Chen *et al.* [43], 2006	Shear	Sn3.5Ag and SnPb Ni(P)/Au	150°C for 1500 hours	1. SnPb solder bumps failed in the solder bulk. 2. For Sn3.5Ag solder, most of the solder bumps failed partially inside the	1. Shear strength for both SnPb and Sn3.5Ag solder bump decreased slightly (8.9% for the SnPb and 5.3% for the Sn3.5Ag).

				solder in a cohesive way and partially at the Ni(P)/Au interface in a brittle way.	2. Ni(P)/Au prevented the IMC/solder interface failure mode by inhibiting the Cu diffusion from the substrate. 3. Sn3.5Ag had higher shear strength than SnPb. A possible reason could be the presence of Ag_xSn IMCs.
Anderson *et al.* [44], 2004	Shear	Sn3.9Ag0.6Cu, Sn3.7Ag0.6Cu0.3CoSn3.7Ag0.9Cu, Sn3.0Ag0.5Cu, Sn3.6Ag1.0Cu and Sn3.7Ag0.7Cu0.2Fe on Cu	150°C for 100 and 1000 hours	1. The failure mode for both the as-soldered and 100-hour-aged samples was found to be ductile. 2. For 1000 hours, a weakening of the Cu_3Sn/Cu interface was observed in Sn3.5Ag and SAC alloys, leading to partial debonding during the shear test. 3. The failure did not involve the fracturing of the Cu_3Sn layer. 4. SAC solders modified with Co and Fe did not experience debonding under shear test and experienced only ductile failure.	1. Solders aged for 100 hours exhibited the highest strengths. 2. Alloying of Fe and Co suppressed the diffusion rate of Sn and minimized the coalescence and formation of voids at the Cu_3Sn/Cu interface.
Chan *et al.* [45], 1998	Shear	SnPb, leadless ceramic chip carrier (LCCC)	155°C for 0–16 days	Failure in both unaged and aged solder joints occurred in the solder bulk	A linear reduction in shear joint strength was observed with an increase in intermetallic layer thickness up to ~5.6 μm during aging.
Kim *et al.* [46], 2005	shear	SAC solder and electroless Ni(P) UBM	80, 100, 120 and 150°C for 72, 144, 360, 720, 1200, 1440, and 2400 hours	1. Ductile failure mode during the initial aging period. 2. Brittle interfacial failure at IMC–solder interface during the final stages of aging.	1. Shear strength of the joints decreased during isothermal aging at all test temperatures. 2. The microstructural coarsening of the bulk solder caused an initial decrease in shear strength, while the later decrease in shear

					force was due to the increasing IMC thickness which led to brittle interfacial failure.
Miyazaki *et al.* [47], 2005	Three-point bend	Sn1.0Ag0.1Cu, Sn3.0Ag0.5Cu, Sn1.0Ag0.1P, and Sn1.0Ag0.1In on Cu-OSP and Ni/Au Uniaxial test specimens	125°C for 0 to 480 hours	Interfacial crack initiated inside the IMCs and propagated to Kirkendall voids	1. For Cu (OSP), the cycles to failure for the solders decreased after thermal aging due to increased Cu-Sn IMC thickness during thermal aging. 2. For Ni/Au finished packages, the fatigue strength of Snl.0Ag0.1Cu showed a decrease, while that of Sn1.0Ag0.1In increased. The fatigue strength of Sn3.0Ag0.5Cu and Snl.0Ag0.1P did not change.
Ma *et al.* [48], 2006	Creep	SAC	Room temperature, 125°C for 6 months	-	1. For unaged solders, the creep strength of SAC is higher than that of SnPb. 2. The creep strength of SAC solders became less than that of SnPb after 50 hours of aging at 125°C
Zhang *et al.* [49], 2008	Creep	SAC105, SAC205, SAC305, SAC405, and SnPb	25, 75, 100, and 125°C for 0–12 months	-	1. Degradation in the creep properties with aging. 2. Small particles can block the movement of dislocations and reduce grain boundary sliding, strengthening the materials. 3. Coarser particles cannot block the dislocation movements and grain boundary sliding, thus degrading the creep properties.
Weise [50], 2007	Creep	Sn3.5Ag, Sn3.8Ag0.7Cu and Sn0.7Cu bulk samples (dog-bone-type specimens), PCB samples (Cu pin soldered into through-	125°C for 24–1176 hours	-	1. Aging at 125°C for 24 hours softens the SAC solder significantly. 2. Aging at 125°C beyond 24 hours and up to 1176 hours does not further change the

		hole connections and flip chip joints)			creep behavior of the flip chip SAC solder joints. 3. Cu and Au IMCs strengthen the SnAg and SAC solders. 4. Strengthening is preferably observed in small solder volumes such as flip–chip joints.

Limited studies have been conducted to assess the influence of thermal aging on the thermal cycling reliability of solders [51-52]. Choubey *et al.* [51] reported degradation of thermal cycling reliability of SAC305 solders in PBGA assemblies upon subjecting to thermal aging at 125^{o}C for 350 hours. However, Coyle [52] reported that isothermal aging at 125^{o}C for 500 hours of resistor assemblies did not influence the thermal cycling durability of SAC405, SAC305, SAC105, and SnCu solders. A systematic study investigating the influence of aging temperature and duration on the thermal cycling durability of solders is still lacking.

1.4.4 Preconditioning for High Strain Rate Reliability Tests

Due to the recent shift in the focus of the electronics market from desktop computing to portable applications [53], the industry started focusing on solder-joint failure under high strain rate tests as well. Under high strain rate tests, brittle failure of the interfacial IMC was promoted through the suppression of plastic deformations in the solder bulk. The failure site in such tests is the interfacial IMC region. The cracks may be closer to or at the interfacial IMCs at the solder/substrate surface. Table 1.2 summarizes the findings on the effects of thermal aging on the solder reliability under high strain rate reliability/strength tests.

Table 1.2: Preconditioning for High Strain Rate Strength/Reliability Tests

Paper	Test/ Strain rate	Solder/ pad finish/component	Aging temp /duration	Failure mode/site	Result
Mattila *et al.* [17], 2006	Drop	Sn0.2Ag0.4Cu on bare Cu CSP	125°C for 500 hours	1. Component-side Cu_3Sn layer	1. The drop reliability decreased significantly with aging. 2. Void-assisted cracking of the component side Cu_3Sn layer caused the drop reliability degradation.
Jee *et al.* [54], 2006	Lap shear (0.003 mm/s) and bending	Sn36.8Pb0.4Ag and Sn3.0Ag0.5Cu on Cu(OSP) and electrolytic Ni/Au	150°C for 500 hours	1. For Cu(OSP) specimens, failure occurred at the interface of Cu_3Sn/Cu. 2. For electrolytic Ni/Au, brittle fracture was found between $(Ni,Cu)_3Sn_4$ and $(Cu,Ni)_6Sn_5$ IMCs.	1. For Cu(OSP), Kirkendall voids formed at the Cu_3Sn/Cu interface after thermal aging degraded the mechanical reliability and caused brittle fracture even at very low strain rate lap shear test results. 2. For electrolytic Ni/Au, the growth of $(Ni,Cu)_3Sn_4$ underneath $(Cu,Ni)_6Sn_5$ degraded the bending reliability.
Zeng *et al.* [40], 2005	Shear (1 mm/s) and pull (5 mm/s)	SnPb on bare Cu CSP	150, 125, and 100 °C, respectively, for up to 80 days	1. Shear test at 1 mm/s caused failure in the solder bulk. 2. Pull test at 5 mm/s caused failure at the solder–pad interface.	3. Kirkendall voids at the interface under aging at temperatures above 100°C caused SnPb solder joints to weaken at the interface.
Chiu *et al.* [55], 2004	Drop	SAC on bare Cu CSP	125°C for 3, 10, 20, and 40 days	1. The Cu/Cu_3Sn interface was the failure site.	1. Thermal aging leads to a reduction in drop test reliability. 2. Kirkendall voiding at the Cu to Cu3Sn IMC interface is the main mechanism for the decrease in drop reliability.

Chong *et al.* [56], 2008	Drop	Sn-4Ag-0.5Cu OSP	150°C for 120, 240, and 390 hours	Brittle failure at solder–IMC interface	1. For SAC/OSP, the reliability degraded by more than 50% after 120 hours of aging. 2. After aging for 240 and 390 hours, the reliability reduced to less than five drops due to the thicker IMCs.
Peng *et al.* [57], 2007	Drop	SAC on bare Cu CSP	100–150°C for up to 1000 hours	1. Failure occurred due to cracking at the interfaces of Cu_3Sn/Cu_6Sn_5 and Cu_6Sn_5/solder on the package side.	1. Fracture in the interfacial region was dominant. 2. Kirkendall voiding did not directly contribute to the drop failures. 3. Thermal aging at 175°C improved the drop performance
Chotchakornpant *et al.* [58], 2007	Pull	SAC125 on OSP/Cu and SAC305 on Ni/Au	150°C for up to 1000 hours	2. Failure site for SAC125/OSP was at solder-pad interface. 3. The failure of SAC305-Ni/Au pad occurred in solder only.	1. IMC thickness for SAC125 on OSP(Cu) increased dramatically (~2.45μm to ~6.5μm), while that for SAC305-Ni/Au increased slightly (~1.85 μm to ~2.4 μm). 2. The pull force for SAC125/OSP decreased rapidly with aging time in the initial step of aging and became almost constant at longer aging time from 80 to 1000 hours. 3. For SAC305-Ni/Au, the pull force increased with aging time due to lower IMC thickness and the reformation of solder texture.
Monlevade [53], 2007	Board-level drop	Sn-3.8Ag0.7Cu OSP/Cu BGA packages	100, 125, and 150°C for 50, 75, 100, 200, 400, 600, and 1000 hours	1. Crack propagation paths: bulk solder/Cu_6Sn_5, Cu_6Sn_5/Cu_3Sn, Cu_3Sn/Cu, bulk solder/Ag_3Sn 2. Crack	1. Kirkendall voiding was observed on both the package and board sides but did not affect the crack propagation. 2. No correlation between aging and

				propagation paths seemed to avoid the Cu_6Sn_5/Ag_3Sn interface.	drop reliability was reported.
Lee *et al.* [59],	Shear and cold bump pull	SAC405 on ENIG and OSP	150°C for 100, 200, 500, and 1000 hours	1. Failure modes in ball pull test were ductile, brittle, and mixed failure modes, i.e., quasi-ductile (or <50% area with exposed pad) and quasi-brittle (or >50% area without solder) modes. 2. Ductile and quasi-ductile failure modes were observed in the shear test.	1. Thermal aging caused higher IMC growth rate in solders with OSP finish than those with the ENIG finish. 2. OSP-finished solders had lower solder joint strength than ENIG.

In view of the detrimental effects of Kirkendall voiding on solder reliability under high strain rate tests, researchers proposed ways to reduce the Kirkendall voiding. Chang *et al.* [60] reported that the addition of Ag helped to reduce the formation of Kirkendall voids. The Sn-9Zn-xAg/Cu interface did not show the occurrence of Kirkendall voids after aging at 180°C for 250 hours. The addition of Ag acted as an inhibitor for the formation of Kirkendall voids. A shift in failure sites from bulk to interface in aged solders by changing the strain rate has also been investigated [61-62]. Date *et al.* [61] reported that by changing the strain rate of the shear test from 200 μm/s to 1 m/s, the ductile-to-brittle transition was observed in eutectic SnPb and near-eutectic SnAgCu solder balls on Cu or ENIG pads aged at 150°C for up to 1000 hours.

It is known that high IMC thickness can trigger brittle interfacial failures—even at a low strain rate—because of the weaker interface [54]. In view of such findings, researchers have reported ways to inhibit IMC growth in solders [44, 61, 63, 64].

Amagai [65] in his work reported that plating the substrate pads with nickel could control IMC growth in Sn3.5Ag0.75Cu and Sn1.0Ag0.5Cu solders. Anderson [44] reported a strategy of modifying high Cu-containing SAC alloys with Co and Fe to produce a solder joint with Cu that retains strength and ductility for longer aging times (1000 hours) at high temperatures (150^{o}C). The comparison of IMC thickness after 100 hours of aging revealed that that the growth of the Cu_3Sn layer is the slowest in the Co-modified solder joints and the third slowest in the Fe-modified solder joints.

1.5 Faulty Preconditioning Practices

The current practices of isothermal aging lack the understanding of the effects of isothermal aging on solder microstructure and durability. Some of the critical factors which determine the influence of preconditioning on solder interconnect reliability are not considered in the selection of preconditioning levels. Listed below are several areas of gaps in the current understanding of isothermal aging preconditioning:

1.5.1 Choice of Preconditioning and Interpretation of Effects of Isothermal Aging on Reliability

The biggest concern with current practices in preconditioning is the lack of rationale behind choosing a particular preconditioning condition. Researchers have adopted a wide range of preconditioning conditions for reliability tests without providing insight into the reasons for selecting those conditions. Even the existing industry standards recommend preconditioning without providing a rationale. For instance, IPC guidelines [14] state that preconditioning is conducted “to simulate a

reasonable use period and accelerate such possible processes as solder grain growth, intermetallic compound growth, and oxidation." It is unclear what "reasonable use period," "reasonable grain growth," and "reasonable IMC thickness" mean. Moreover, it is not clear how preconditioning at a certain aging temperature and duration corresponds to the actual storage/use life period. Preconditioning should be chosen based on knowledge of how a preconditioning condition (temperature and time) corresponds to the storage/service life period of the components.

1.5.2 Preconditioning for High and Low Strain Rate Tests

The choice of preconditioning for high and low strain rate tests is a concern. As discussed in the previous sections, in general, the high strain rate and low strain rate tests cause failure at the interfacial IMC layer and bulk, respectively. Isothermal aging affects both solder bulk microstructure and interfacial IMC growth. As a consequence of isothermal aging, the thickness of interfacial IMC increases. For high strain rate tests, such as the drop test and the impact test, the increased interfacial IMC layer thickness at the solder–pad interface can act as a crack initiation site, reducing the reliability of the solder joint. Interfacial voiding, which is often considered to be a high temperature aging effect, further deteriorates reliability under high strain rate tests. However, it needs to be determined if voiding is a process-related issue exacerbated by high temperatures, or if it is a consequence of high temperature aging. Since, the solder joint reliability under high strain rate tests is highly dependent on interfacial IMC thickness and voiding, it is clear that preconditioning degrades solder interconnect reliability under high strain rate tests.

For low strain rate tests, researchers have reported varying results for solder joint reliability/strength under isothermal aging. In general, solder shear strength is reduced due to preconditioning. However, preconditioning studies on the thermal cycling test, which is one of the most common low strain rate tests, are still few in number. Under elevated temperature isothermal aging, coarsening of IMC particles in the solder bulk occurs, which can affect the reliability. Interfacial IMC thickness also increases as a consequence of aging. The increased interfacial IMC thickness can reduce the ductile region of the solder joint, which increases the strain in the bulk solder and reduces low strain rate cyclic fatigue life. So far, it has not been determined if preconditioning should be carried out before the thermal cycling tests. Complicating the issue of isothermally aging test specimens prior to temperature cycling is the natural aging that will occur during the application of the test-imposed temperature cycles. The influence of varying aging temperatures and times on thermal fatigue needs to be studied to decide if preconditioning is required for these tests. Lastly, the decision to carry out or not to carry out preconditioning by isothermal aging is dependent on the reliability tests to be conducted after preconditioning, which in turn depends on the application conditions. This difference has not been taken into account in current industry practices for preconditioning.

1.5.3 Preconditioning Based on Solder and Board Finish

The elemental composition of a solder as well as the solder joint formation process and metallization of the connecting interfaces will govern the microstructural characteristics in terms of bulk and interfacial IMC composition, as well as mechanical and reliability characteristics. For instance, SAC solders on Cu (OSP)

form Ag_3Sn and Cu_6Sn_5 IMCs in the solder bulk and Cu_6Sn_5 and Cu_3Sn (for $\geq 100^oC$) at the solder-Cu (OSP) interface. Whereas the same solders on Cu (ENIG) finish form $AuSn_4$ IMC in addition to Ag_3Sn and Cu_6Sn_5 IMCs in the solder bulk and $AuSn_4$, $(Cu,Ni)_6Sn_5$, and Ni_3Sn_4 IMCs at the solder-Cu interface. Moreover, if SAC or SnCu solders are modified by the addition of elements such as Bi, Ni, Ge, Co, etc., it would result in a different bulk and interfacial microstructure. The resulting different bulks and interfacial microstructures would age differently under preconditioning. Therefore, test vehicles assembled with different solders and board finishes subjected to the same preconditioning might not be at the same state, since the responses of each of those solders would be different. The situation gets more complex if the assembly consists of multiple solder types or if a comparison is made across assemblies formed with different solders. These issues are not addressed in current industry practices on preconditioning. While it might not be feasible to precondition different solder type and board finish combinations, it is nonetheless very important to account for the differences in solder microstructure and interfacial IMC thickness in the solders. The choice of isothermal aging conditions for preconditioning should be made while taking into account the response of these solders to it.

1.6 Conclusions and Recommendations

Preconditioning by isothermal aging is a common practice in the electronics industry prior to conducting reliability tests on solder joints. However, current preconditioning practices do not provide a rationale for the choice of preconditioning conditions. The current standards and industry practices do not provide the relation of preconditioning with storage life or actual operating conditions. The strain rate in

mechanical tests affects the influence of aging on solder joint reliability. Therefore, generalizing preconditioning across loading conditions might be improper. Another factor that has received insufficient attention is the consideration of solder type and board finish type while selecting the aging temperature and duration.

In order to determine the appropriate preconditioning for solder joints, it is necessary to determine the reliability implications of preconditioning at various temperatures and durations. Solder and board finish type and high and low strain rate tests should be considered in order to arrive at an appropriate preconditioning level. Then the acceleration factors must be obtained in order to relate the preconditioning and the subsequent test to use life conditions. The next step is to include these effects in physics of failure (PoF)-based models of solder joint reliability. An appropriate combination of preconditioning and test load specification can lead to a better design of experiments to simulate both the storage and use life conditions of solders in electronics.

Based on the literature review, the following recommendations are made:

a. Preconditioning is recommended for high strain rate tests for high temperature applications, since increased interfacial IMC thickness has a detrimental effect on durability and can simulate aging effects in solder. Interfacial IMC thickness can be used as an aging metric for these tests. The preconditioning level should be chosen by mapping the interfacial IMC growth at the aging temperature with that at working temperature.

b. Further studies need to be conducted to understand the effects of isothermal aging temperature and duration on the temperature cycle fatigue durability of solder interconnects.

c. Studies should be conducted to determine how the preconditioning conditions relate to the actual use conditions, and acceleration factors should be determined.

d. Based on the findings, current physics-of-failure (PoF) based models for solder joint reliability should be updated to take into account the effects of isothermal aging on reliability.

e. Current industry guidelines and standards should be updated to prescribe preconditioning levels (time and temperature) based on the anticipated application condition.

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2 Chapter 2: Methodology to Quantitatively Assess the Aging of Solder Joints

The chapter discusses the development of a methodology to quantify the aging in silver-based, as well as tin-lead solders. SnAgCu solders with 3% and 2% silver, along with eutectic tin-lead solders are analyzed under the aging temperature range of 50–150^{o}C for the aging duration of 24–1000 hours. Solder joint aging is represented by the particle coarsening-based model in terms of size of silver-tin intermetallic compounds, and the distribution of silver-tin intermetallic compounds for SAC solders, and lead-rich phase for tin-lead solders.

2.1 Introduction

The solder joint reliability depends on its microstructure which in turn is a function of the precipitate size and distribution, which in case of SAC solders are Ag_3Sn and Cu_6Sn_5. In order to understand and relate the mechanical and thermomechanical behavior of solders under aging, the evolution of these precipitates with aging needs to be understood. It is known that Cu-Sn and Ag-Sn IMCs strengthen the solder matrix by pinning the dislocations, therefore restricting the dislocation movement. Therefore more widely these IMCs are spread, the better creep resistance they provide. Previous researchers have reported that the size and number of the Ag_3Sn IMCs influence the creep properties of the SAC solders wherein smaller sized Ag-Sn IMCs interact more with the dislocations [1]. The large-sized Ag-Sn IMCs are undesirable since they degrade the reliability of solders [1]. The as-received

or room temperature stored specimens have a larger number of silver-tin intermetallic as compared to a specimen aged at an elevated temperature. Hence the smaller size sized and larger number of precipitates results in a more creep-resistance joint. It has been reported that aging decreases the hardness of the solder joints, and makes them more susceptible to creep and shear failures [2, 3]. The sensitivity to aging was reported to increase with decrease in silver content [3]. Higher silver content means more prevalent silver-tin IMCs hence better ability to block dislocations. The degradation in creep resistance due to aging was also attributed to the decrease in the count of IMCs. With aging, the bigger IMCs grow at the expense of smaller IMCs by a mechanism known as Ostwald's ripening, which is driven by minimization of surface energy. However the aging affect stabilizes after long term aging, as reported by Arfaei [4] in his studies. The comparison of 1000 and 3000 hour aged specimens at 125^{o}C exhibited similar hardness and shear strength values.

However, so far the studies of the aging effect on the microstructure are limited in scope. There is a need to understand the evolution of solder microstructure systematically so that the aging can be related to the solder reliability. To this regard an aging model for solders is needed, which can be related to the solder joint reliability under different mechanical and thermo-mechanical loadings. In this chapter, an aging metric based on the Ag-Sn and lead-rich phase size is developed for SAC and SnPb solders.

2.2 Experiment Details

The test vehicle consists of 2512 resistors mounted on flame retardant (FR4) board (Figure 2.1), the underlying substrate is copper (Cu) on OSP. Three solder types; Sn96.5Ag3.0Cu0.5 (SAC305), Sn98.5Ag1.0Cu0.5 (SAC105), and Sn63Pb37 (SnPb) are analyzed. The Cu substrate thickness was 40 μm and the resistor termination was made of nickel with a coating of matte tin. The reflow temperature for SnPb solder was 216^{o}C, the time above liquidus was 82 seconds, while the ramp up rate was 0.4891^{o}C/sec and the ramp down rate was -3.25^{o}C/sec. Same reflow profile was used for all the lead-free solders, the reflow temperature of 244^{o}C, time above liquidus 50-74 seconds, ramp up rate 0.4825^{o}C/sec and the ramp down rate was -3.41^{o}C/sec. Aging conditions were room temperature, 50, 100 and 150^{o}C for 24, 120, 336, 600 and 1000 hours. An additional set of specimens were aged at 100^{o}C for 2000 hours, to extend the baseline curve at 100^{o}C.

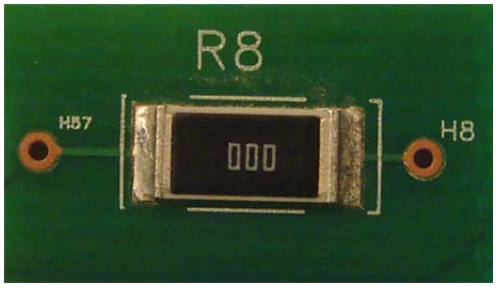

Figure 2.1: Test Specimen

The test specimens (resistors on FR4 board) were cut out from the test board shown in Figure 2.1 and are aged as per the aging conditions listed above. Three specimens per aging condition are analyzed. After aging, the components are mounted in the epoxy, cross-sectioned and polished. Chemical etching is carried out with a solution of 2% HCL, 4% HNO_3 and 94% C_2H_5OH at room temperature. The

solution etches the Sn and IMCs in the solder at different rates, with Sn etching faster than the IMCs. This helps to reveal a distinct IMC layer for measurements. The etching time was kept as 5 seconds for optimum etching. The test specimens are then analyzed under environmental scanning microscopy (ESEM).

2.3 Microstructural Evolution of Solders under Isothermal Aging

The solder microstructural evolution was studied for the select solders. During aging, the Ag_3Sn and Cu_6Sn_5 intermetallics in the solder bulk combine to become bigger wherein the bigger IMCs combine the smaller ones onto themselves by a process known as Ostwald's ripening. As a result of this the average size of IMCs increases with aging, and at the same time they become more uniformly distributed. Figure 2.2-Figure 2.4 compare the solder microstructure as a function of aging temperature. The solder microstructures at 50, 100 and 150^{o}C after 1000 hours of aging are compared. In case of SnPb solders, the average size of lead-rich particles increases with aging duration, the effect being more significant at 150^{o}C. For SAC solders, the effect of aging can be observed as an increase in the size of both Ag_3Sn IMCs as well as the Cu_6Sn_5 IMCs. Another effect of aging is the change in the distribution of IMCs in bulk, which becomes more uniform with aging. More detailed microstructural evolution of the solders can be found in the Appendix.

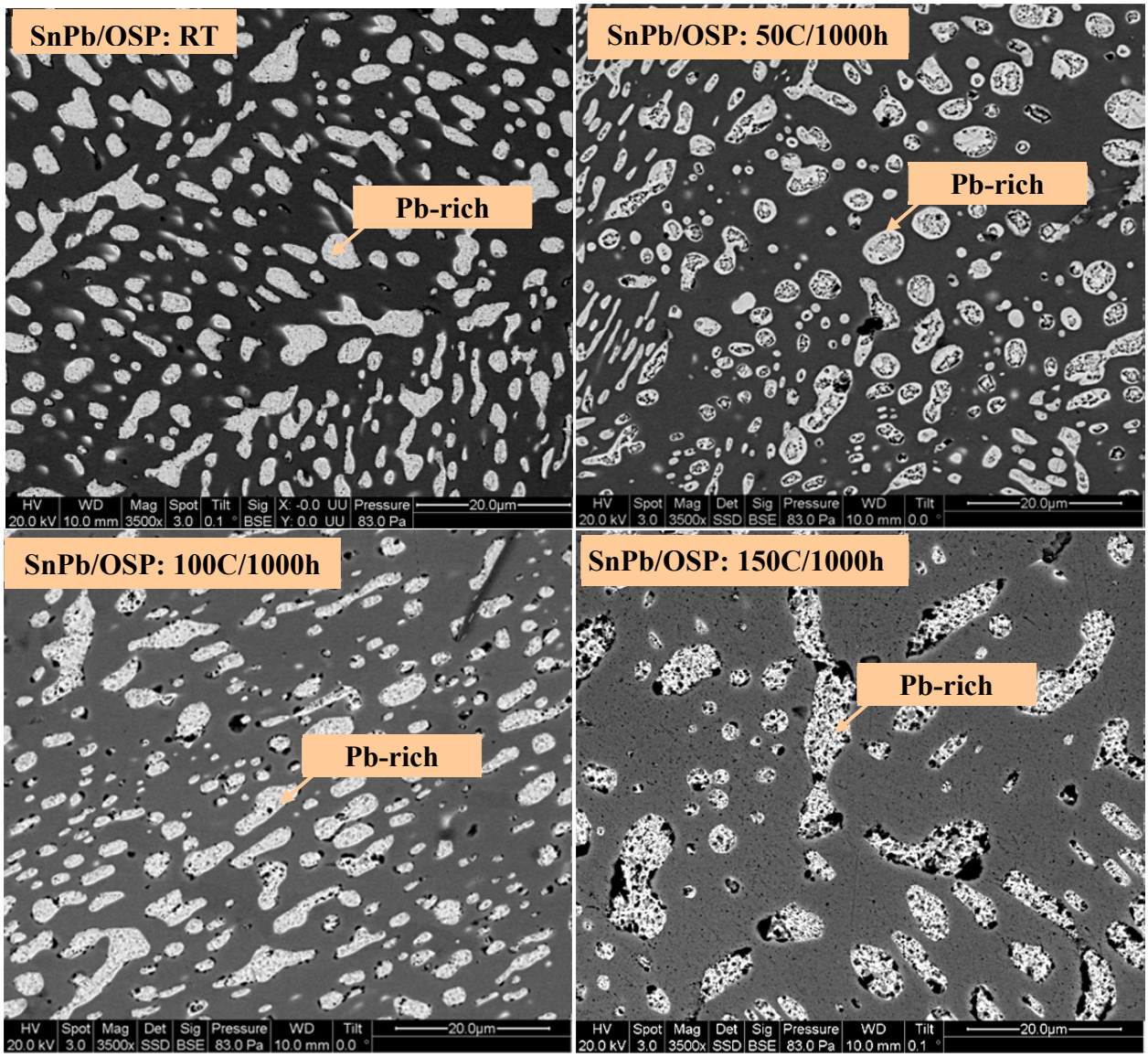

Figure 2.2: SnPb aged at (a) room temperature and (b) 50°C (c) 100°C and (d) 150°C for 1000 hours.

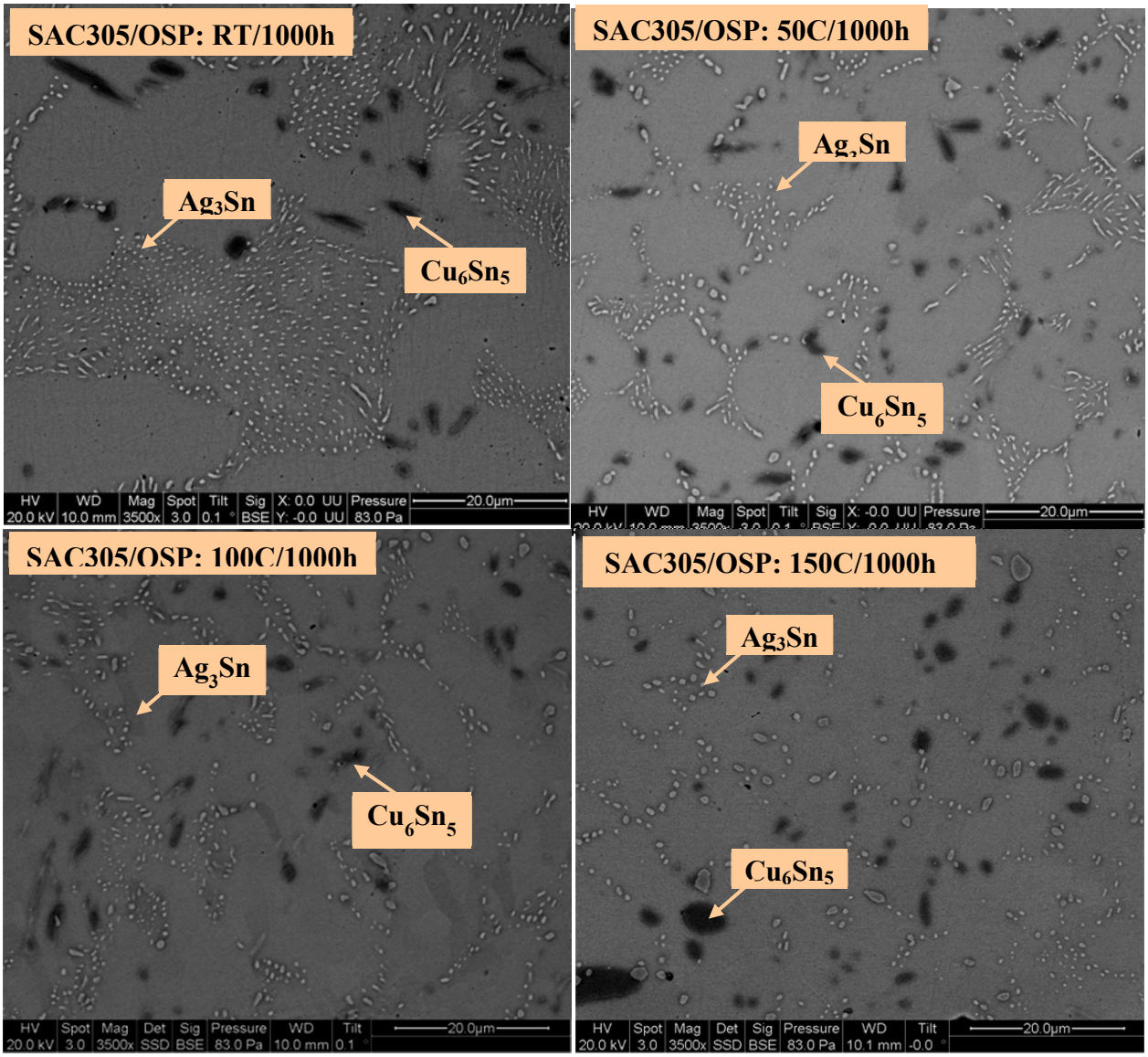

Figure 2.3: SAC305 aged at (a) room temperature and (b) 50°C (c) 100°C and (d) 150°C for 1000 hours.

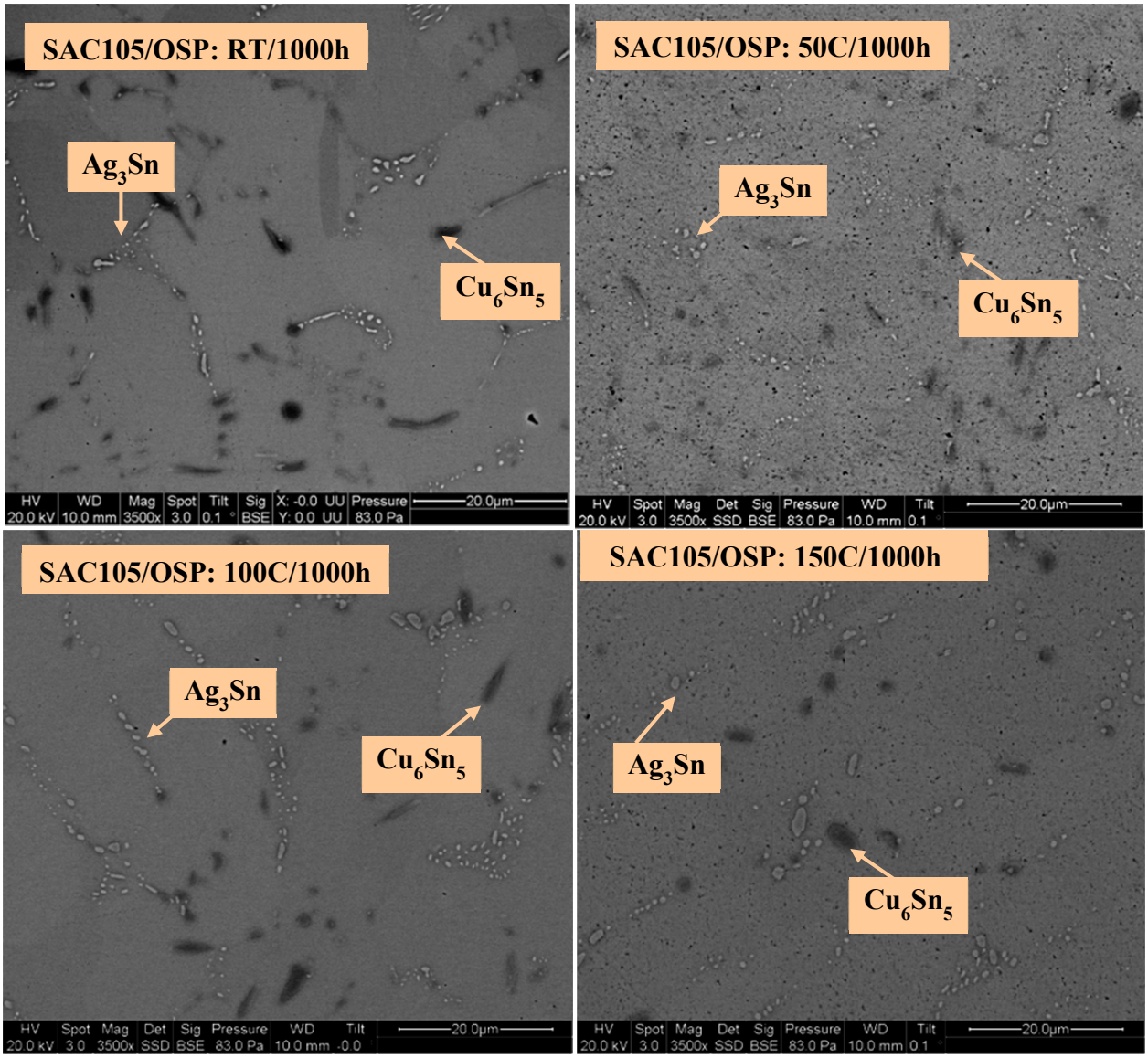

Figure 2.4: SAC105 aged at (a) room temperature and (b) 50°C (c) 100°C and (d) 150°C for 1000 hours.

2.4 Methodology to quantify the aging metric of solders

The microstructural images of the soldiers were analyzed using Image Pro Plus software. Since the accuracy of the data obtained from the images highly depends on the quality of the images, extreme care should be taken in preparing

scratch- and inclusion-free samples. The first step in the image processing is to calibrate the images with the scale given at the bottom of the images. Then the contrast and brightness values of the image are adjusted to clearly bring out the IMCs. Thereafter, the Ag_3Sn IMCs are selected by adjusting the gray scale in the histogram.

(a) Ag_3Sn and Pb-rich phase size measurements

For the Ag_3Sn area, major and minor axis measurements, the outline of the IMCs is selected by adjusting the gray scale of the histogram. It should be noted that the IMCs falling on the boundary of AOI (area of interest) are excluded from the measurements since it is not known what fraction of their area is outside the AOI. Similarly for SnPb solders, the outline of the Pb-rich phases is selected and the particles at the boundary are excluded.

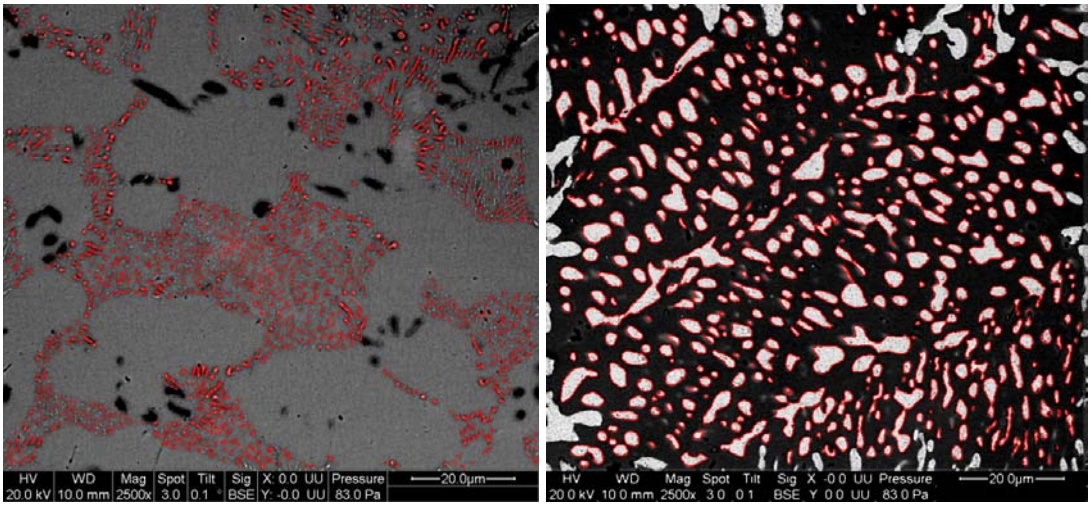

Figure 2.5: Selected (a) Ag_3Sn IMC, and (b) Pb-rich phases

(b) Ag_3Sn and Pb-rich phase distribution

The changes in the distribution of Ag_3Sn IMCs during aging is assessed by using the segmentation and pruning features of the image-pro plus. The image

consisting of the selected areas form the step (a) is subjected to "segmentation" by "thresholding" the image, in which the Ag_3Sn IMCs and the background are separated as two distinct zones (black and white). Thus the original gray scale image is converted to a binary image in which the Ag_3Sn IMCs (in SAC) and Pb-rich phases (in SnPb) are set to black, while the background is set to white. Next, the pruning operation is carried out on the image by constructing a Voronoi diagram.

Voronoi Diagram: "A Voronoi diagram of a point set is a subdivision of the plane into polygonal regions (some of which may be infinite), where each region is the set of points in the plane that are closer to some input point than to any other input point" [6]. The centers of the circumcircles in a Delaunay triangulation can be connected to obtain the Voronoi diagram (see Figure 2.6).

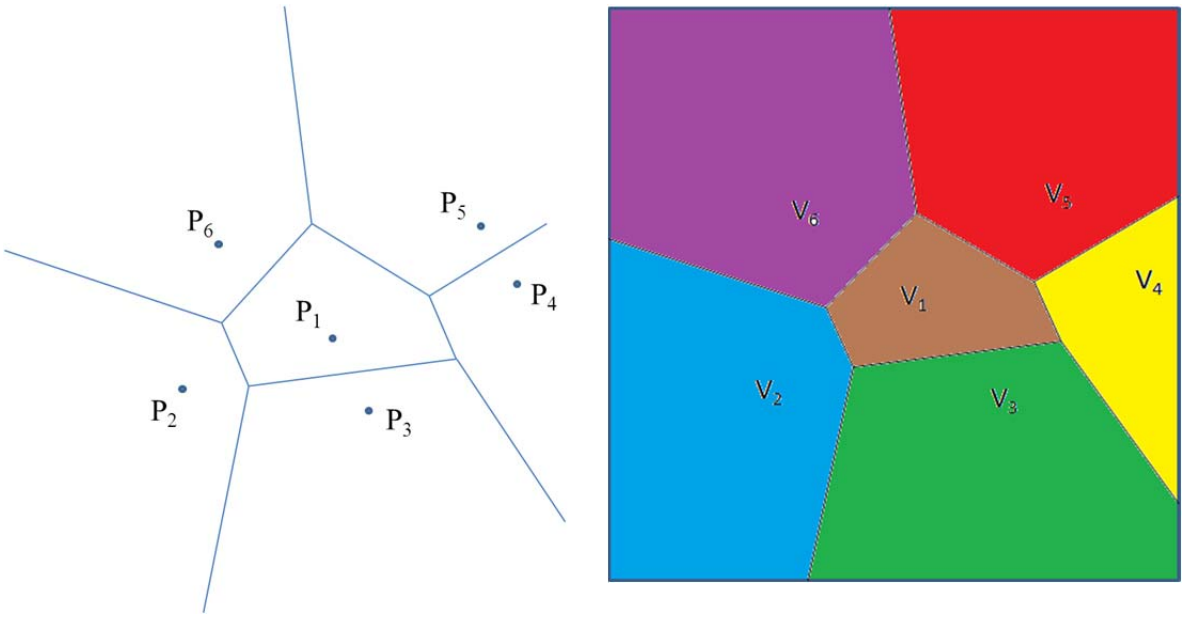

Figure 2.6: (a) Particles P1-P5, and (b) Voronoi cells V1-V6

Delaunay Triangulation Algorithm: Delaunay triangulation is a surface triangulation technique used to analyze the spatial distribution. "A Delaunay triangulation of a set of points is a triangulation of the point set with the property that no point in the point set falls in the interior of the circumcircle (circle that passes through all three vertices) of any triangle in the triangulation" [6].

Each Voronoi cell surrounding an IMC or Pb-rich phase is its area-of-influence and the size distribution of these area of-influences (V1) is an indicator of the homogeneity of the distribution. The lower the standard deviation of the areas, the more uniformly distributed the particles are. Figure 2.7 (a) and (b) shows the Voronoi diagrams for Ag_3Sn IMCs in SAC305 solder and Pb-rich phases in SnPb solder respectively.

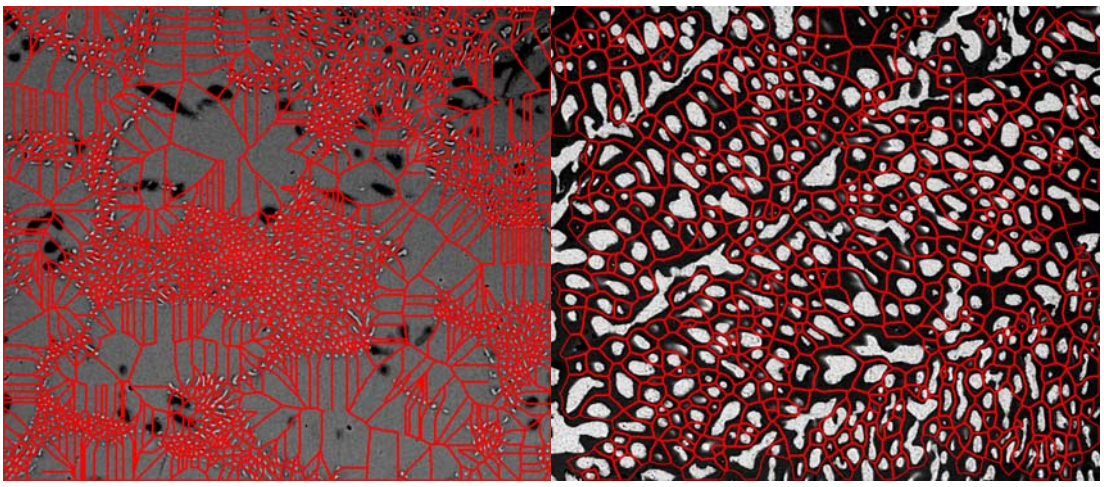

Figure 2.7: Voronoi diagram for selected (a) Ag_3Sn IMC, and (b) Pb-rich phases

2.5 Results

The results of the size and distribution analysis are shown below. As seen in Figure 2.8, for SAC105 solder at 50, 100 and 150°C, the area of Ag_3Sn particles increases sharply upto 336 hours of aging and then slows down. It can also be seen that Ag_3Sn area is higher at 150°C than at 50°C at all aging times, and slightly higher than 100°C. For SAC305 solder, similar trends are observed except that at 150°C, the Ag_3Sn particles show a continuous increase in size with aging time.

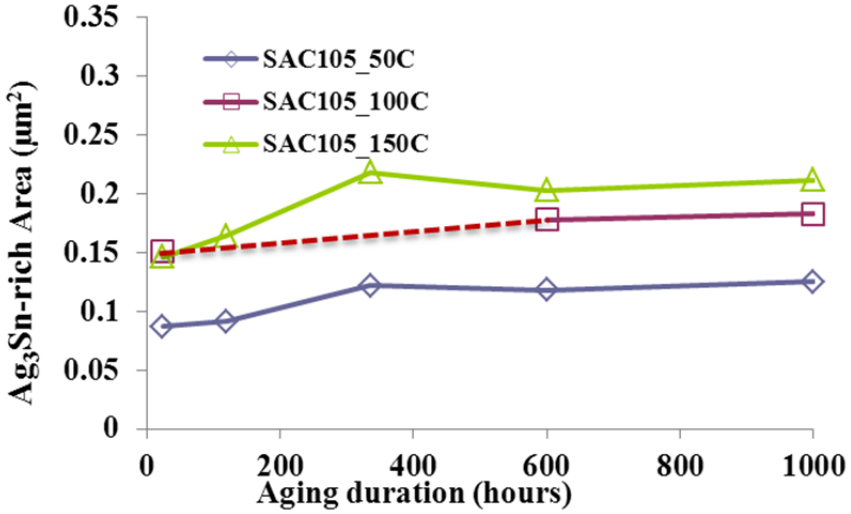

Figure 2.8: Ag_3Sn area in SAC105 solder at 50, 100 and 150°C

Table 2.1: Model constants for Ag_3Sn coarsening in SAC105

Ag_3Sn-rich Phase Coarsening	
E_a (kJ/mol)	45.05
k_0	1.39E-02
n	13.91
R^2	0.99

k ($\mu m^n/hr$)		
50C	**100C**	**150C**
0.72E-9	6.87E-9	3.52E-8

Aging Model – SAC105

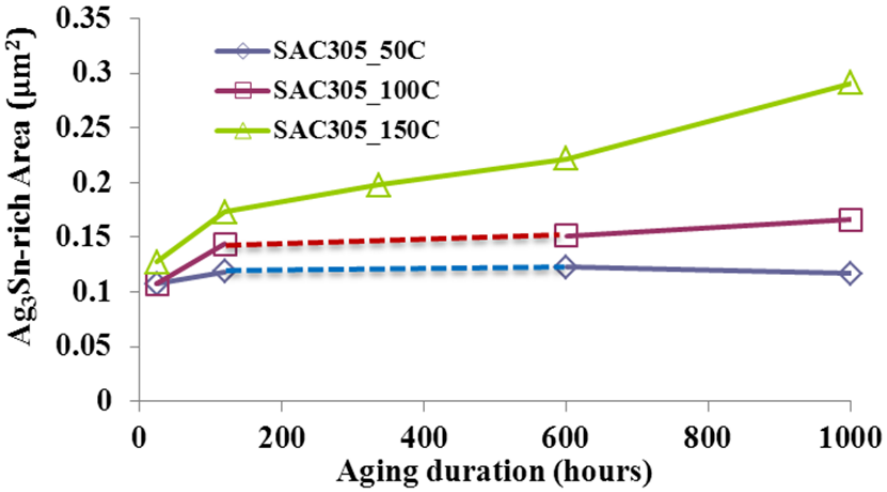

Figure 2.9: Ag_3Sn area in SAC305 solder at 50, 100 and 150°C

Table 2.2: Model constants for Ag_3Sn coarsening in SAC305

Ag_3Sn-rich Phase Coarsening	
E_a (kJ/mol)	48.43
k_0	4.74
n	8.04
R^2	0.95

k ($\mu m^n/hr$)		
50C	**100C**	**150C**
6.98E-8	7.83E-7	4.96E-6

Aging Model – SAC305

For SnPb solders, the size of Pb-rch phases at 150°C is higher than that at both 50°C and 100°C. However, the increase in size is very slow at 50°C. At 100°C, the rate of increase of Ag_3Sn particle size is higher than at 50°C. At 150°C, the rate of increase of Ag_3Sn size is the highest and the IMC size increases rapidly upto 600 hours of aging and then drops down slightly.

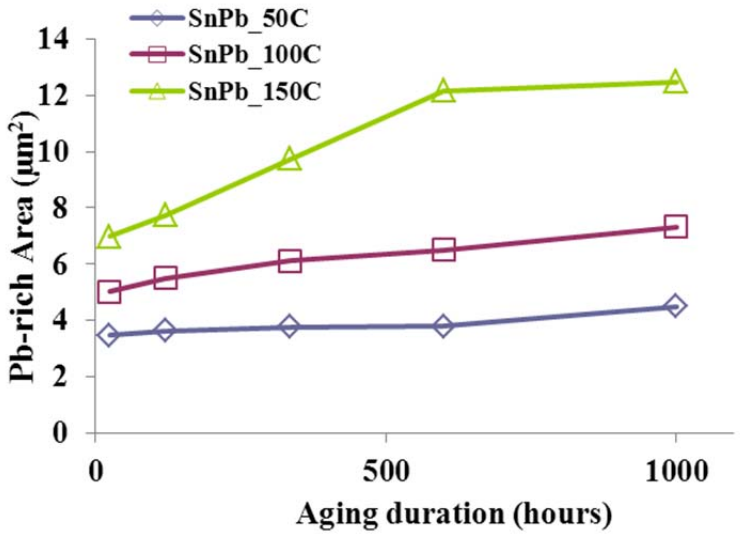

Figure 2.10: Pb-rich phase area variation at 50 and 150°C as a function of aging duration

Table 2.3: Model constants for Ag_3Sn coarsening in SAC305

Pb-rich Phase Coarsening	
E_a (kJ/mol)	55.09
k_0	3.13E+10
n	6.73

k (μm^n/hr)		
50C	**100C**	**150C**
0.04	0.60	4.92

Aging Model-SnPb

$$r^{6.73} - r_0^{6.73} = (3.13 * 10^{10}) * e^{-\frac{55.09}{RT}}(t - t_0)$$

The change in the major and minor axis of the Ag_3Sn IMCs with aging was also compared. Figure 2.11 (a) and (b) show the comparison of major axis size of Ag_3Sn aged at 150°C for 24 and 1000 hours. It can be seen that with aging, the average size of the IMCs increases. The change is more marked in SAC105 as compared to SAC305.

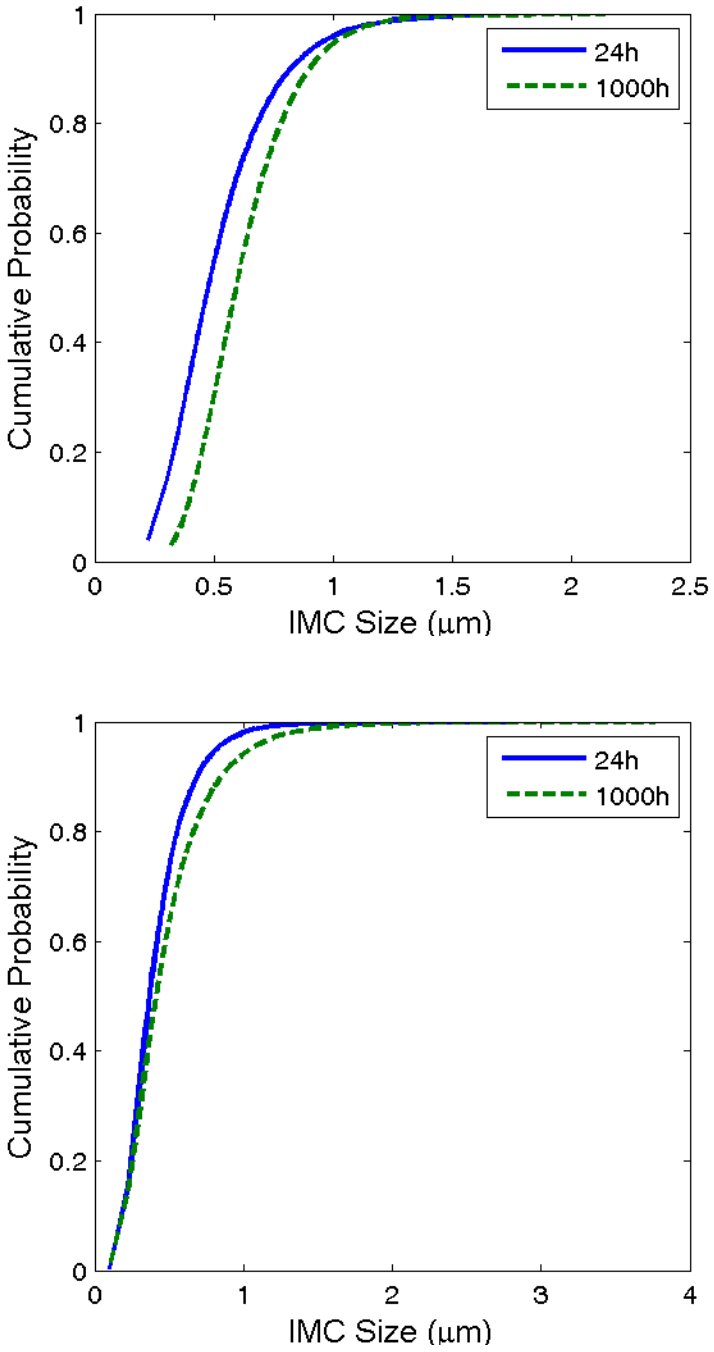

Figure 2.11: Ag3Sn major axis length as a function of aging at 150°C in (a) SAC105, and (b) SAC305

For SnPb solders, at 1000 hours the percentage of Pb-rich phases of size less than 2 microns is similar to that at 24 hours. However, the percentage of Pb-rich

phase size greater than 4 microns is higher at 1000 hours aged specimens as compared to the ones aged at 24 hours.

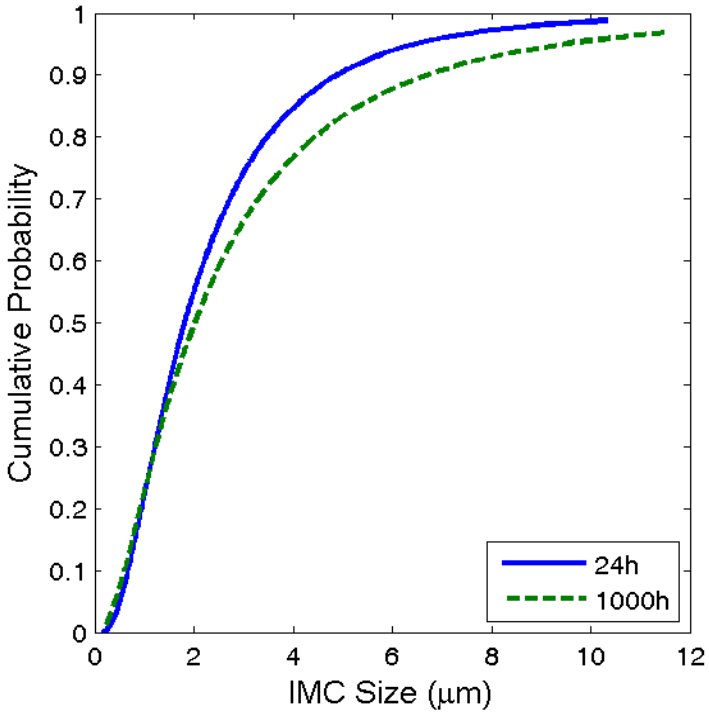

Figure 2.12: Pb-rich phase size as a function of aging at 150°C

The comparison of the standard deviation of the Voronoi areas with aging in Figure 2.13 that for SAC105 and SAC305 solders, the standard deviation of the Voronoi areas decreases with aging duration, which in turn implies that with aging the Ag_3Sn distribution in the solder bulk becomes more uniform with aging.

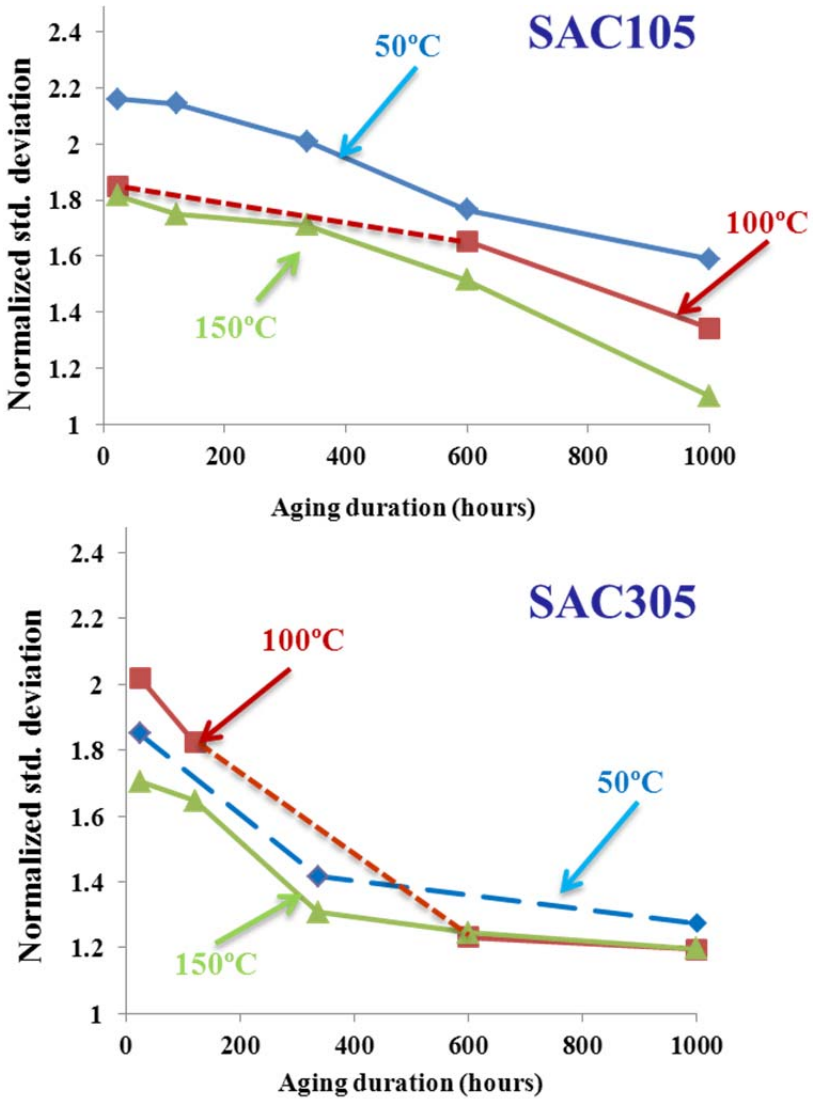

Figure 2.13: The standard deviation of the Voronoi areas in (a) SAC105 and (b) SAC305 solder at 50 and 150°C as a function of aging duration

For SnPb solders, the comparison of the standard deviation of the Voronoi areas with aging shows that for SnPb solders, the standard deviation of the Voronoi areas does not show any trend for all the aging temperatures.

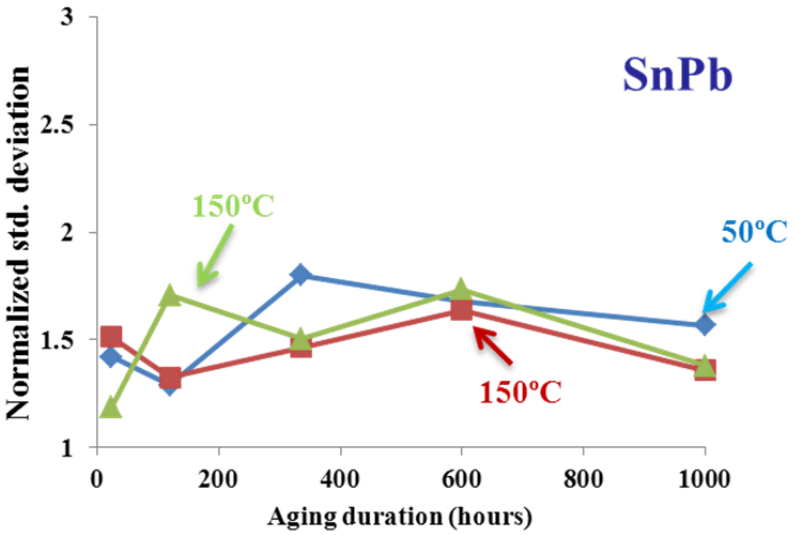

Figure 2.14: The standard deviation of the Voronoi areas at 50 and 150°C as a function of aging duration

2.6 Summary

SAC105 and SAC305 solders:

- The kinetics of coarsening of Ag_3Sn IMCs in solder bulk is found to be

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- The IMC distribution analysis reveals that with an increase in aging time, the distribution of Ag_3Sn IMCs becomes uniform as the standard deviation of the areas of the Voronoi cells decreases.

SnPb solder:

- The kinetics of coarsening of Pb-rich phase is found to be:

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- The distribution analysis of Pb-rich phase reveals that aging has no effect on the distribution of the Pb-rich phase in the SnPb solders.

2.7 References

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5. Shewchuk 1996

3 Chapter 3: Effect of Isothermal Aging on Interfacial Intermetallics at the solder–pad interface

Copper-tin (Cu-Sn) interfacial intermetallic compounds (IMCs) are found extensively in electronic hardware. The interfacial IMC is initially formed during the solidification process under reflow or wave soldering during assembly. After assembly, the IMC thickens due to solid-state inter-diffusion of Cu and Sn atoms. The rate of growth of the interfacial intermetallic compounds (IMCs) is influenced by the composition of the solder joint. With the new tin based solders, the growth rates can be expected to vary. To understand the growth of IMCs, tests samples including SAC305, SAC105, SN100C, and SnPb were examined. Test samples were formed with tin-finished 2512 resistors soldered on to organic solderability preservative (OSP) finished copper pads and subjected to isothermal aging at temperatures of 50, 100 and 150^{o}C and durations of 24, 120, 336, 600 and 1000 hours. The kinetics of interfacial IMC (Cu_6Sn_5 and Cu_3Sn) was investigated. It is found that for the temperature range of (25-50^{o}C), SAC305, SAC105 and SN100C solders, in that order exhibit higher interfacial IMC thickness at solder-substrate interface than SnPb solders for upto 1000 hours of aging. At aging temperatures of 100^{o}C or higher, SnPb solders have higher interfacial IMC growth rate than the lead-free solders. This chapter also determined activation energies of the interfacial IMC growth and discusses the relative comparison of the growth rates of Cu_6Sn_5 and Cu_3Sn IMC phases. The activation energy values of Cu-Sn interfacial IMCs (Cu_6Sn_5+Cu_3Sn) with SAC305, SAC105, SN100C and SnPb for the temperature range of 50-150^{o}C were found to be 60 KJ/mole, 68 KJ/mole, 68 KJ/mole and 59 KJ/mole respectively.

However, reporting activation energy for the combined IMC thickness of Cu_6Sn_5 and Cu_3Sn IMC phases for the temperature range of 50-150^oC is erroneous, since the IMC growth mechanism undergoes a transition due to the growth of Cu_3Sn IMC at 150^oC. At 50^oC SAC solders show higher growth rate of Cu_6Sn_5 IMC than SnPb and SN100C solders. On the other hand at 150^oC, SnPb show highest growth rates for Cu_3Sn phase and SN100C the lowest. For Cu_6Sn_5 phase, SN100C shows the highest growth rate and SAC105 the least.

3.1 Introduction

Intermetallic compounds (IMCs) form when terminals of packaged devices are soldered to metal pads on printed circuit boards. During the wetting reaction in the soldering process, the solder alloy reacts with the base substrate metal to form the IMCs which continue to grow during the solid-state aging. The interfacial IMCs are required to obtain a good metallurgical bond between the solder and metal terminal/pads. The elemental composition of solder and terminals/pads will influence the growth of the IMCs. After solder solidification, it is a widely accepted that the growth of IMCs is a diffusion-controlled reaction governed by temperature and time. High temperature aging thickens IMC in bulk solder and increases interfacial IMC thickness. Studies have been conducted to investigate the impact of aging temperature and duration on the durability and microstructure of solder interconnects. Excessive growth of the interfacial IMC layer can reduce interconnect reliability since these are less ductile than the bulk solder and may initiate failures at the interface [1-4]. IMCs have higher electrical resistivity than solder and substrate material [5]. Excessive

IMC formation changes the electrical characteristics of the solder interconnects which can cause reliability concerns [6-8]. Reliability tests are conducted on isothermally aged test specimens and no explanation on the choice of aging condition is provided. Various industry standards call for preconditioning of solders prior to reliability testing. For example, IPC-SM-785 [9] recommends that FR4-based solder joint test assemblies be subjected to 100^{o}C for 300 hours and polyimide-based solder test assemblies be subjected to 125^{o}C for 100 hours. IPC9701 and GEIA-STD-0005-3 [10-15] call for aging at 100^{o}C for 24 hours. The rationale that above standards provide is that "aging simulates a reasonable use period and accelerates such possible processes as solder grain growth, intermetallic compound growth, and oxidation." Similar to IPC standards, GEIA-STD-0005-3 standard states that preconditioning is an effective means of replicating the changes that occur during the lifetime of a solder joint. These standards also assume that isothermal aging helps to gain consistency among test vehicles by helping the solder grain structures to attain similar characteristics. The influence of aging temperature and duration on solder microstructure and reliability has usually been studied for the SAC solders in the range of 75-175^{o}C for 24-1000 hours [**Error! Reference source not found.**-22]. The IMC growth using aging is a solid state aging and follows the Arrhenius relationship, the model being:

$$y_t^n - y_0^n = A * (t - t_0)$$

$$A = A_0 * e^{-\frac{E_{avg}}{RT}}$$

where y is the IMC thickness at time t, n is the thickness exponent, y_0 is the IMC thickness at time $t = 0$ (start of solid state aging), A is the growth constant, E_{avg} is the average exponential dependence parameter, R is gas constant, T is temperature in Kelvin.

This chapter discusses the interfacial Cu-Sn IMC growth in SAC105, SAC305 and SN100C solders attaching a tin finished 2512 resistor to OSP finished copper pads. IMC thickness at the solder copper interface in these solders is compared to that of SnPb solder.

3.2 Experiments

The test vehicle consists of 2512 resistors mounted on flame retardant (FR4) board (Figure 3.1), the underlying substrate is copper (Cu) on OSP. Four solder types; Sn96.5Ag3.0Cu0.5 (SAC305), Sn98.5Ag1.0Cu0.5 (SAC105), Sn99.3Cu0.70.05Ni+Ge (SN100C) and Sn63Pb37 (SnPb) are analyzed. The Cu substrate thickness was 40 μm and the resistor termination was made of Nickel with a coating of matte tin. The reflow temperature for SnPb solder was 216^{o}C, the time above liquidus was 82 seconds, while the ramp up rate was 0.4891^{o}C/sec and the ramp down rate was -3.25^{o}C/sec. Same reflow profile was used for all the lead-free solders, the reflow temperature of 244^{o}C, time above liquidus 50-74 seconds, ramp up rate 0.4825^{o}C/sec and the ramp down rate was -3.41^{o}C/sec. Aging conditions were room temperature, 50, 100 and 150^{o}C for 24, 120, 336, 600 and 1000 hours. An additional set of specimens were aged at 100^{o}C for 2000 hours, to extend the baseline curve at 100^{o}C.

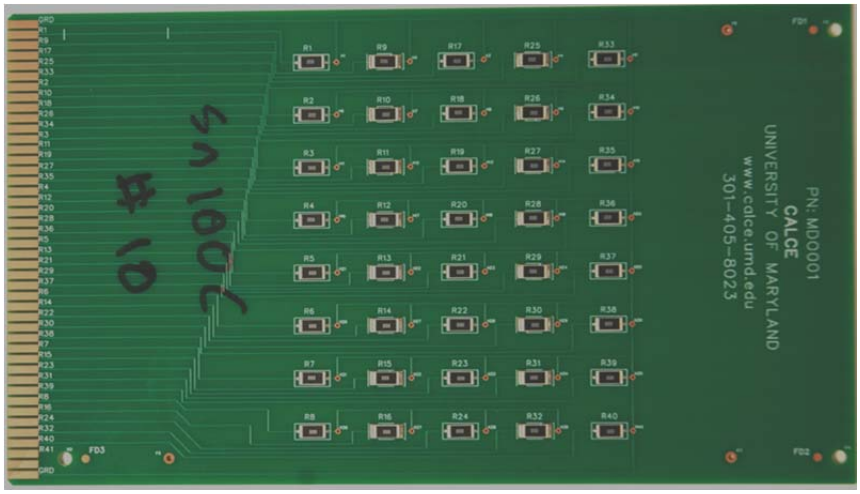


Figure 3.1 : 2512 Resistor board (8 x 4.5 x 0.06 inches, FR4)

The test specimens (resistors on FR4 board) were cut out from the test board shown in Figure 3.1 and are aged as per the aging conditions listed above. Three specimens per aging condition are analyzed. After aging, the components are mounted in the epoxy, cross-sectioned and polished. Chemical etching is carried out with a solution of 2% HCL, 4% HNO_3 and 94% C_2H_5OH at room temperature. The solution etches the Sn and IMCs in the solder at different rates, with Sn etching faster than the IMCs. This helps to reveal a distinct IMC layer for measurements. The etching time was kept as 5 seconds for optimum etching. The test specimens are then analyzed under environmental scanning microscopy (ESEM).

IMC thickness was determined using an area average method. IMC area and horizontal length is measured over the measurement window and the IMC thickness is obtained by dividing the area of the IMCs by the length of the IMCs over the measurement window (see Figure 3.2). Thus, the IMC thickness, IMC_{TK} is defined as

where ‘IMC Area’ is the area covered by the founding region and ‘IMC length’ is the length along the pad for which the area was taken.

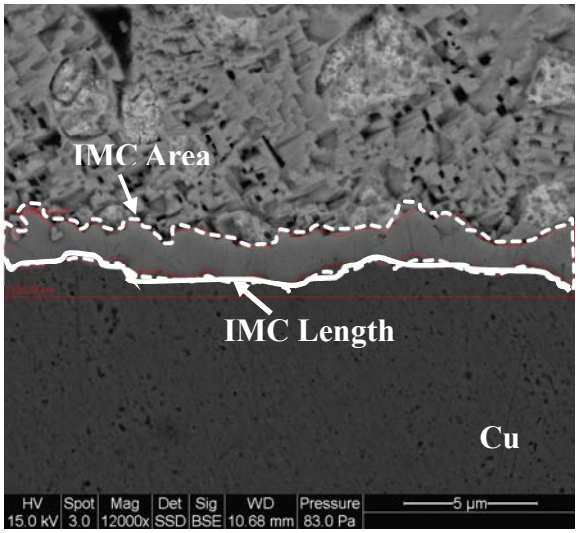


Figure 3.2: Interfacial IMC Thickness Measurement

IMC thickness measurement was facilitated by using imaging software XTDocument on images taken from ESEM. Twelve measurements are made per component (Figure 3.3), six on each side of the solder joint and average of these reading is reported. It should be noted that combined IMC thickness (Cu_6Sn_5+Cu_3Sn) is reported.

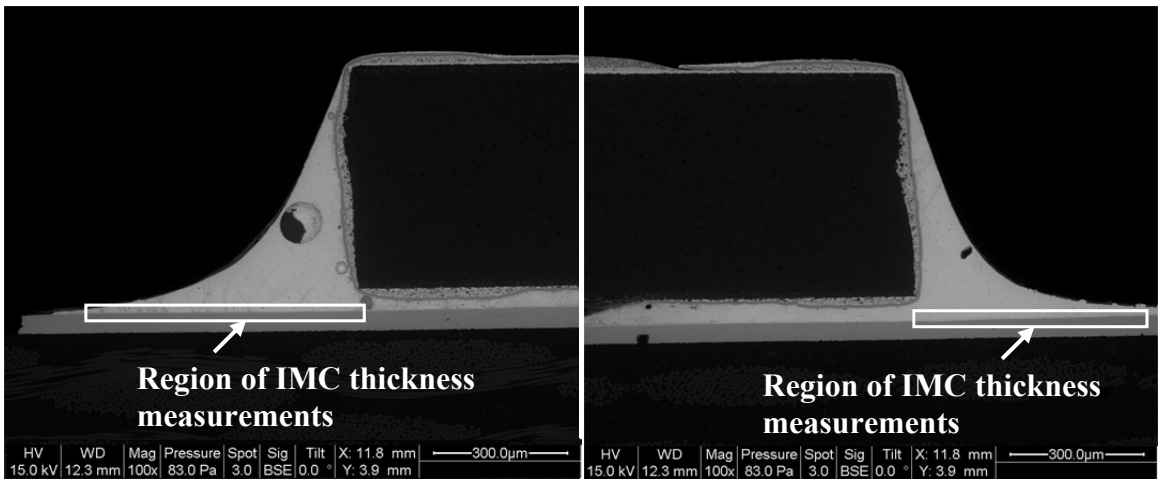


Figure 3.3 : Regions of IMC Thickness Measurement (a) Left Side (b) Right Side of the Component

3.3 Results

The tin-copper interfacial IMC thickness and morphology as a function of aging temperature and duration is documented and the activation energy and growth constants are obtained.

3.3.1 IMC Evolution with Aging Time

IMC formation and growth is a diffusion controlled mechanism driven by temperature. For comparison, the bulk and interfacial IMC for specimens subjected to aging at room temperature and 600 hours at 100^{o}C are examined in Figures 4-7. As expected, elemental analysis of the interfacial IMC reveals Cu-Sn composition. Weight analysis finds 54 copper and 45 tin. This result is consistent with a Cu_6Sn_5 compound. It is observed that the interfacial IMCs formed after reflow and several weeks at room temperature are scallop type and non-uniform.

When subjected to high temperature aging, the IMCs attain higher thickness and more uniform and smooth structure. In addition, a secondary IMC can be observed between the copper and the original Cu_6Sn_5. Weight analysis finds 76 copper and 23 tin. The composition is close to a stoichiometry of Cu_3Sn compound. The smoothing of the IMC is driven by minimization of surface area. During reflow, Cu_6Sn_5 IMC is formed at the solder-substrate interface. Upon aging at 100^{o}C, an additional IMC layer of Cu_3Sn is observed between Cu_6Sn_5 and the bulk solder.

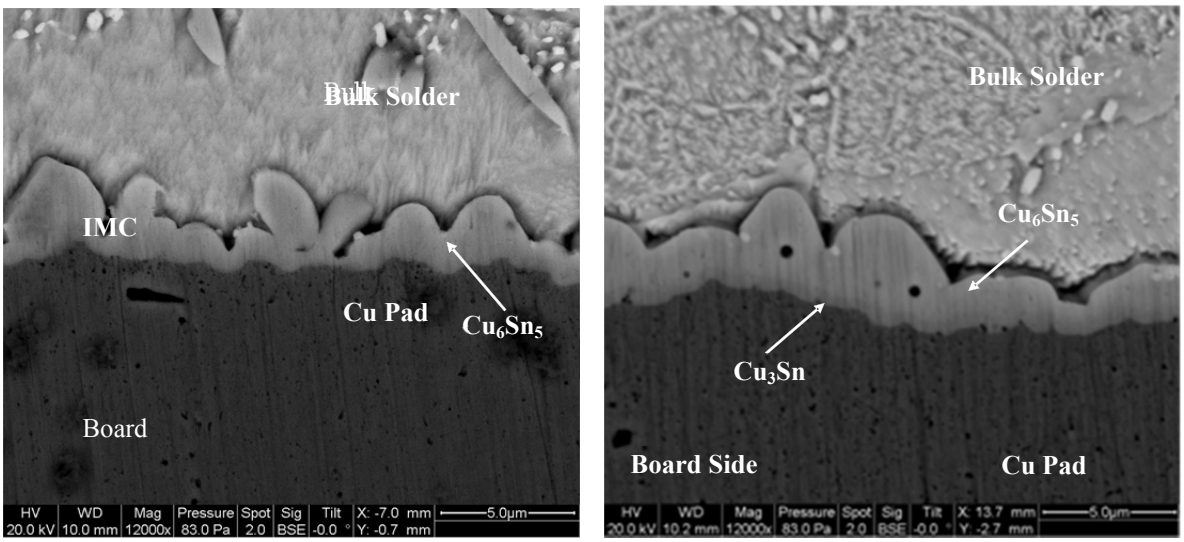


Figure 3.4: a) SAC305 aged at Room Temperature, b) SAC305 aged at 100°C for 600 hours

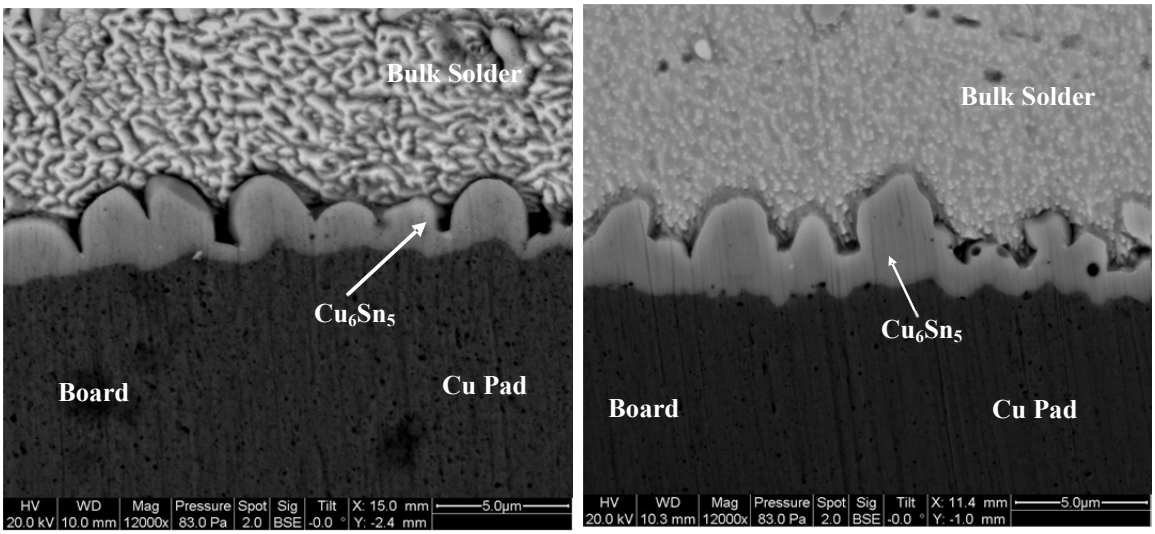


Figure 3.5: a) SAC105 aged at Room Temperature b) SAC105 aged at 100°C for 600 hours

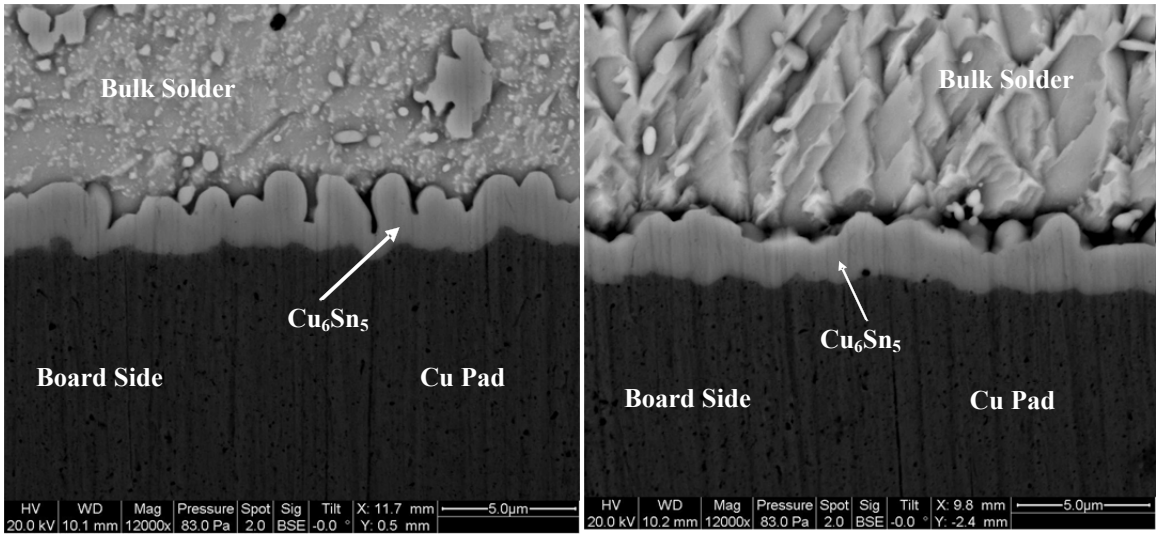


Figure 3.6: a) SN100C aged at Room Temperature b) SN100C aged at 100°C for 600 hours

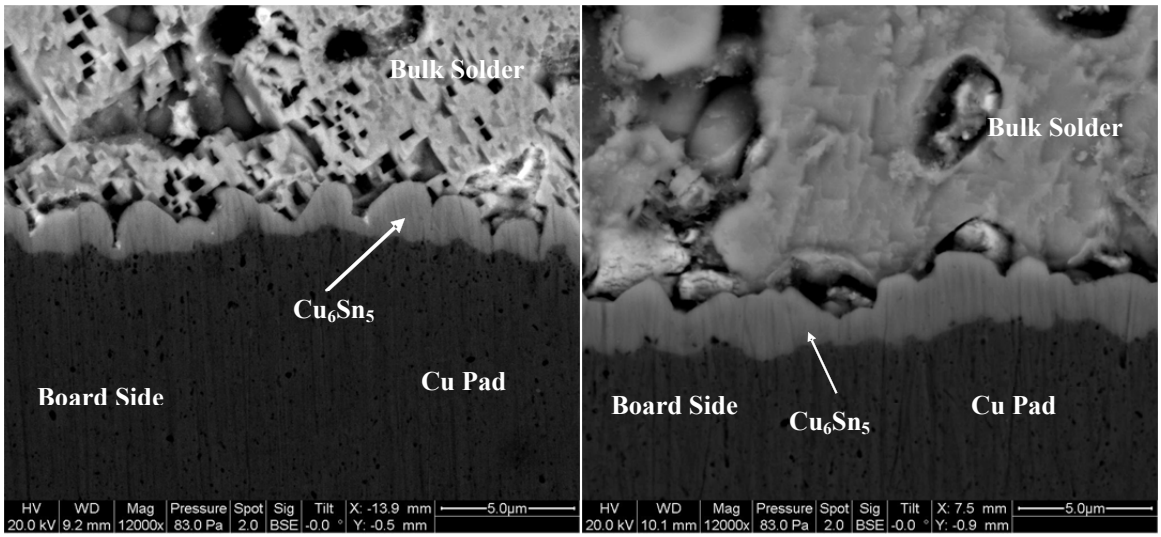


Figure 3.7: a) SnPb aged at Room Temperature b) SnPb aged at 100°C for 600 hours

The scallop shape of the IMCs after soldering and their subsequent smoothening is explained as follows: Researchers have reported that the IMCs formed after reflow are scalloped shaped and explained it with several theories. Most noted ones are by

Hayashi *et al.* [23], and Lord and Umantsev [24] who reported the reason of the scallop formation is due to the faster dissolution of Cu_6Sn_5 along the grain boundaries. Lord and Umantsev [24] provided a more detailed explanation of the scallop formation. They stated that in the initial stages of IMC formation, the IMCs are formed as nucleated grains separated by valleys. These grains grow and merge to form a continuous scallop shaped layer, with the individual layers separated by channels.

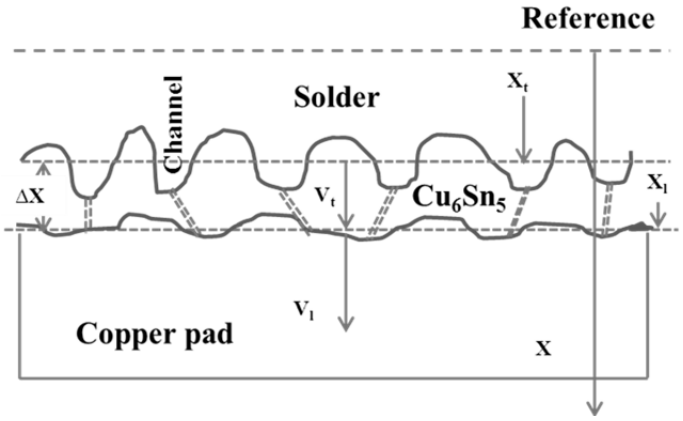


Figure 3.8 : Mechanism of Cu_6Sn_5 IMC growth

The growth of IMCs in Sn-based solders follows a creation-dissolution mechanism wherein in the leading edge (denoted by subscript l) moves towards the copper substrate and creates the IMC and the trailing edge (denoted by subscript t) also moves towards the substrate and dissolves the newly formed compound. The rate of IMC formation is driven by the difference in the rates of movement of the leading and trailing edges. The scallop shape of IMCs is due the dissolution of the grain boundaries. When the solder saturates, the coarsening of IMCs start wherein the

reduction of surface energy is the driving force. This leads to smoothening of the IMC layer to attain a uniform structure.

3.3.2 Results of IMC Thickness Evaluation

Table 3.1 below shows the summary of interfacial IMC thickness (Cu_6Sn_5+Cu_3Sn) evaluation for the solders for the select aging conditions. The results below are the average of twelve readings.

Table 3.1: Mean Interfacial IMC Thickness

Aging Condition	IMC Thickness (μm)			
	SAC105	**SAC305**	**SN100C**	**SnPb**
Room Temp	1.865 ± 0.057	2.064 ± 0.096	1.539 ± 0.233	1.282 ± 0.123
50°C/24h	1.881 ± 0.202	2.078 ± 0.141	1.752 ± 0.108	1.335 ± 0.078
50°C/120h	1.94 ± 0.326	2.127 ± 0.134	1.814 ± 0.112	1.394 ± 0.1
50°C/336h	2.007 ± 0.115	2.256 ± 0.085	1.836 ± 0.097	1.422 ± 0.092
50°C/600h	2.125 ± 0.195	2.346 ± 0.277	1.89 ± 0.265	1.45 ± 0.152
50°C/1000h	2.227 ± 0.279	2.436 ± 0.221	1.998 ± 0.176	1.56 ± 0.092
100°C/24h	1.945 ± 0.251	2.169 ± 0.098	1.698 ± 0.122	1.303 ± 0.054
100°C/120h	2.069 ± 0.249	2.298 ± 0.184	1.724 ± 0.139	1.372 ± 0.06
100°C/336h	2.12 ± 0.158	2.369 ± 0.155	1.896 ± 0.129	1.564 ± 0.082
100°C/600h	2.288 ± 0.114	2.468 ± 0.308	1.939 ± 0.158	1.736 ± 0.065
100°C/1000h	2.364 ± 0.25	2.717 ± 0.129	2.108 ± 0.122	2.089 ± 0.104
100°C/2000h	2.439 ± 0.205	2.975 ± 0.094	2.209 ± 0.094	2.589 ± 0.143
150°C/24h	1.893 ± 0.123	1.952 ± 0.106	2.128 ± 0.205	1.934 ± 0.124
150°C/120h	2.328 ± 0.221	2.322 ± 0.142	2.545 ± 0.301	3.188 ± 0.104
150°C/336h	3.273 ± 0.434	3.328 ± 0.36	3.374 ± 0.286	4.686 ± 0.138
150°C/600h	4.047 ± 0.337	4.236 ± 0.389	4.626 ± 0.324	6.212 ± 0.392
150°C/1000h	5.24 ± 0.368	5.462 ± 0.695	6.148 ± 0.408	7.455 ± 0.233

SAC305 shows highest interfacial IMC thickness values among all the solders under study, followed by SAC105, SN100C and SnPb at 50°C and 100°C for all aging durations. At 150°C SnPb shows highest IMC thickness followed by SN100C, SAC305 and SN100C.

3.3.3 Kinetics of IMC Growth: Activation Energy

Interfacial IMC growth in the select solders is modeled using IMC thickness data. Figure 3.9 shows the IMC growth curves for SAC305 at 50, 100 and 150°C. It can be seen from this plot that the interfacial growth rate at 100°C is only slightly greater than that at 50°C. On the other hand, interfacial IMC growth rate at 150°C is more than 6 times higher than the rate observed at both 50° and 100°C. Similar trends are seen for SAC105 solders (see Figure 3.10).

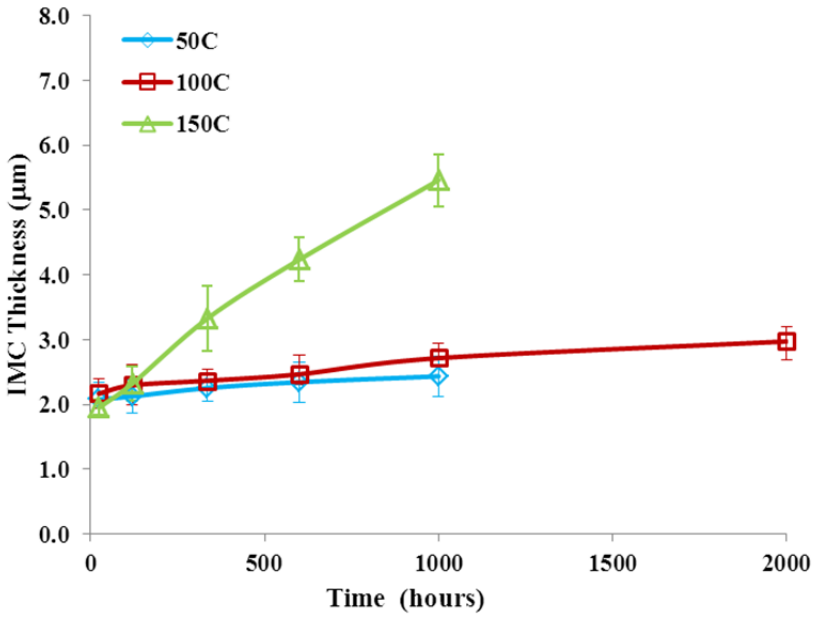


Figure 3.9: IMC growth curves for SAC305 solders.

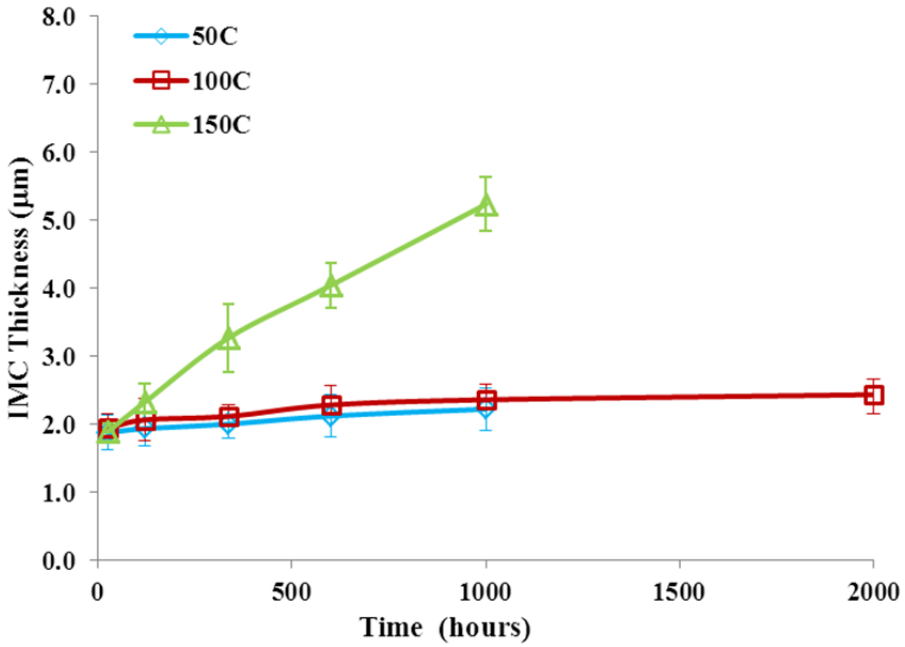


Figure 3.10: IMC growth curves for SAC105 solder.

Figure 3.11 shows the IMC growth curves for SN100C. Here too the IMC growth trends for the three temperature levels follow the same trend as that for the SAC solders. However the growth rate at 150^{o}C for SN100C is higher than that in SAC solders.

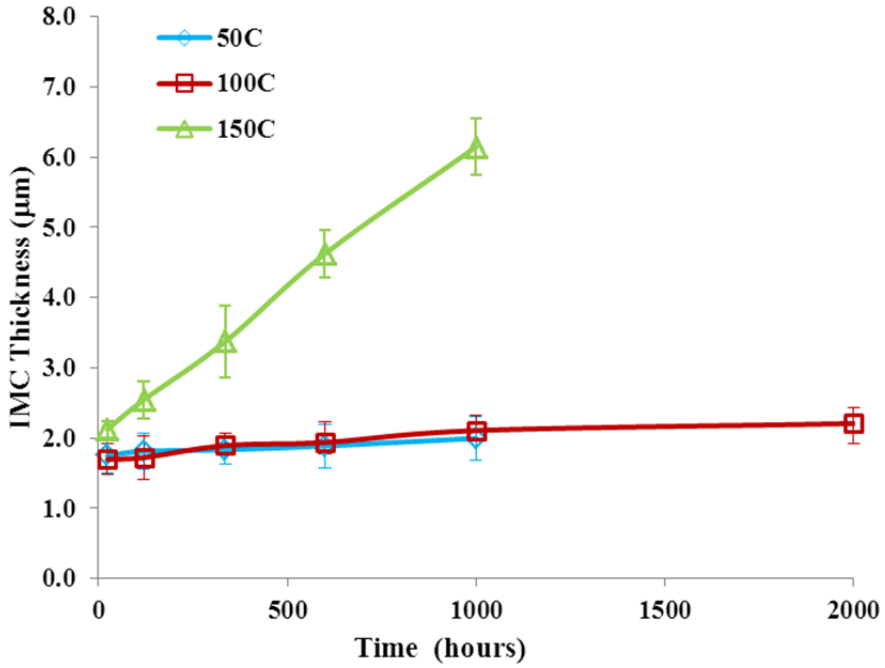


Figure 3.11: IMC growth curves for SN100C solder

For SnPb (see Figure 3.12), the IMC growth at 100°C starts separating out from that at 50°C with aging duration (>336 hours).

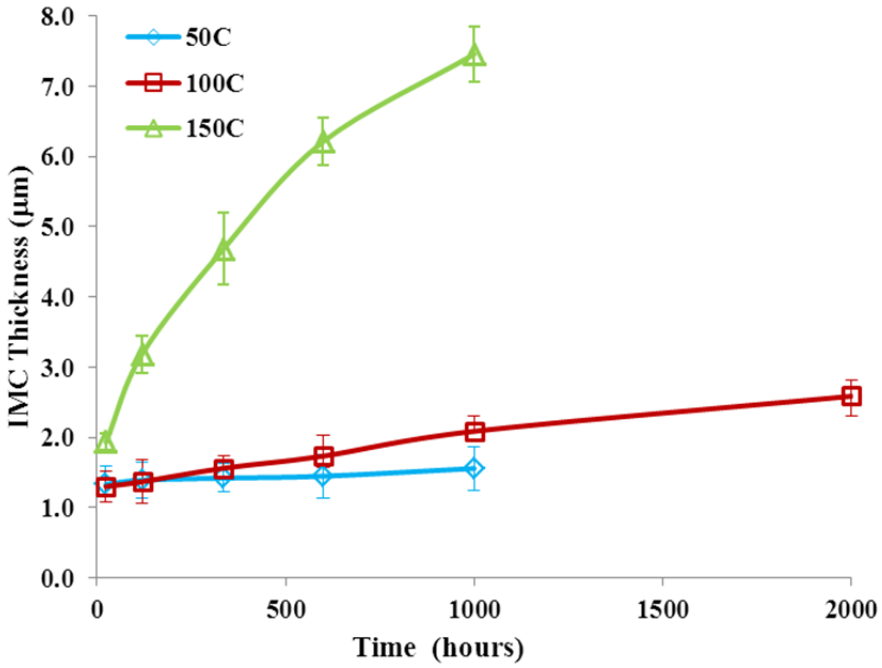


Figure 3.12: IMC growth curves for SnPb solder

At 150°C, the IMC growth rate of SnPb is the highest among all the solders. Figure 3.13-Figure 3.15 show the IMC growth comparison among the solders for the three aging temperatures. At 50°C, IMC thickness for SAC305 solder is the highest among all the solders followed by SAC105, SN100C and SnPb.

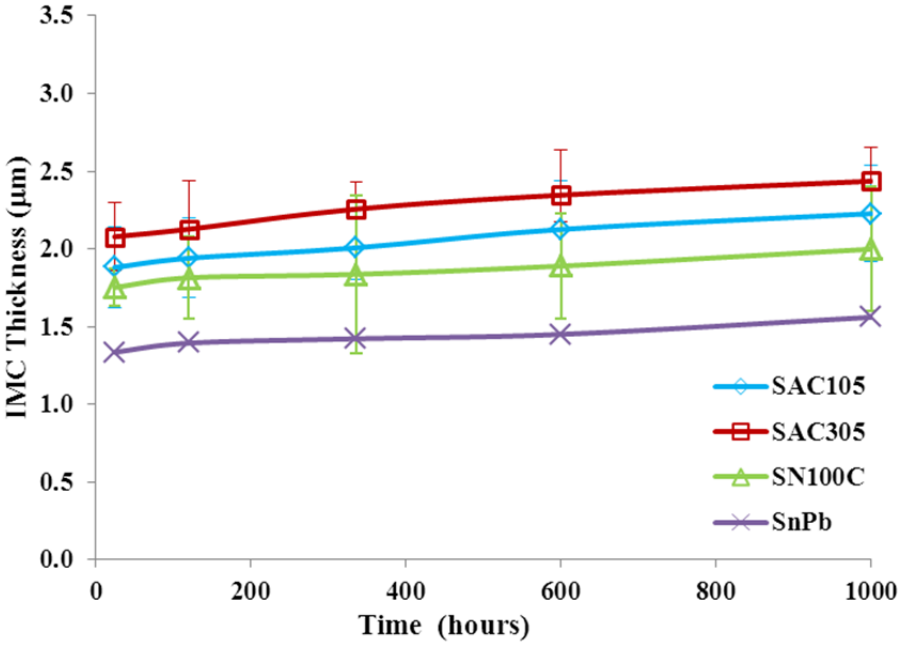


Figure 3.13: IMC growth curves for solders at 50°C.

For 100°C, the IMC growth trends are same as that for 50°C initially. However with aging time the IMC thickness curve for SnPb crosses over the SN100C and SAC105 solders, since it has a higher growth rate of IMCs. At 150°C, the IMC growth rate of SnPb is the highest among all the solders. The documented interfacial IMC growth trends for the lead free solders suggest that aging at 150°C cannot represent long term aging at 50°C and 100°C, since the IMC growth rate at 150°C increases continuously, whereas the IMC growth rate at 50 and 100°C remains constant for the documented length of time.

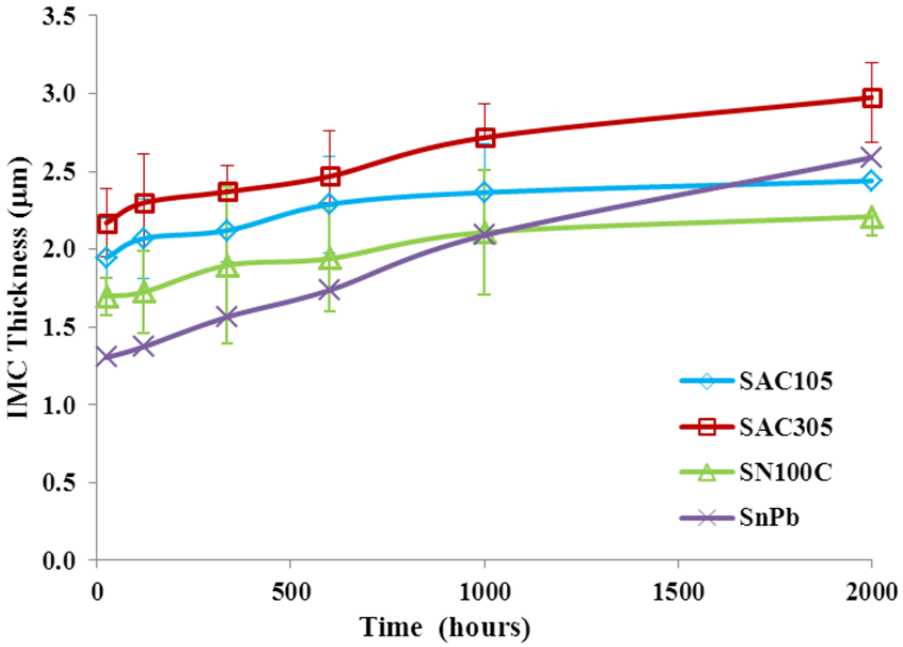


Figure 3.14: IMC growth curves for solders at 100°C.

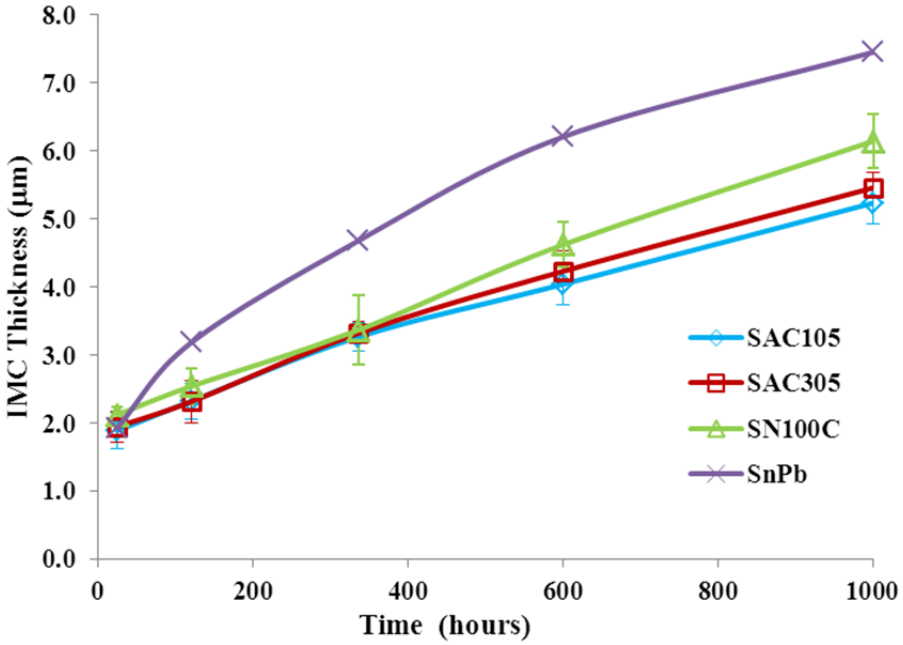
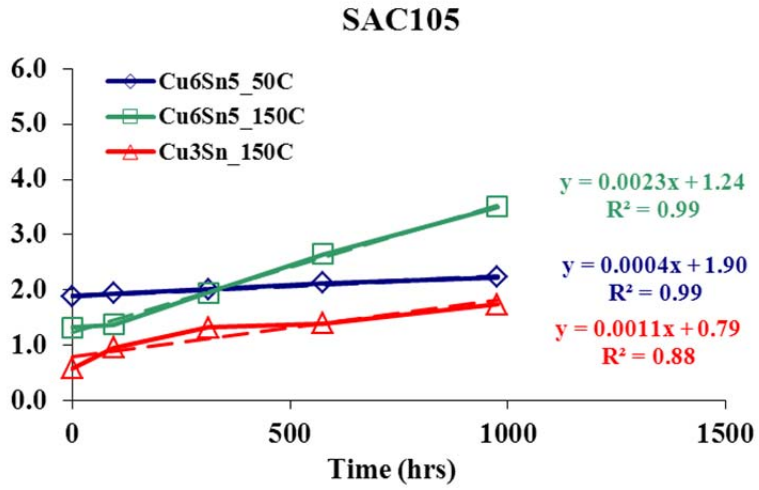


Figure 3.15: IMC growth curves for solders at 150°C.

The growth rates of Cu_3Sn and Cu_6Sn_5 IMCs in SAC105, SAC305, SN100C and SnPb solders was compared at 50°C and 150°C (Figure 3.16(a)-(d)). At 50°C, only

Cu_6Sn_5 IMCs is observed, whereas at 150°C both Cu_3Sn and Cu_6Sn_5 IMCs are observed. For all solders, the growth rate of Cu_6Sn_5 increases with increase in temperature. The increase in growth rates of Cu_6Sn_5 (from 50 to 150C) is highest for SnPb solder followed by SN100C, SAC305 and SAC105. The comparison of growth rates for Cu_3Sn across solders shows that SnPb has the highest growth rate (0.0016 µm/hour), followed by SAC105 (0.0011µm/hour), SAC305 (0.0009 µm/hour), and SN100C (0.0005 µm/hour). Growth rate of both Cu_6Sn_5 and Cu_3Sn IMC phases is highest in SnPb at 150°C due to the enhanced diffusion of Cu and Sn atoms across the interface, because of high homologous temperature. For SN100C solder, the presence of Ni at the solder–pad interface inhibits the diffusion of Cu from the pad into the solder. Hence the growth of Cu_3Sn IMCs, which forms at Cu_6Sn_5-Cu interface is inhibited. Hence, Cu_6Sn_5 grows preferentially and SN100C has the highest growth rate of Cu_6Sn_5 IMC phase among the solders.



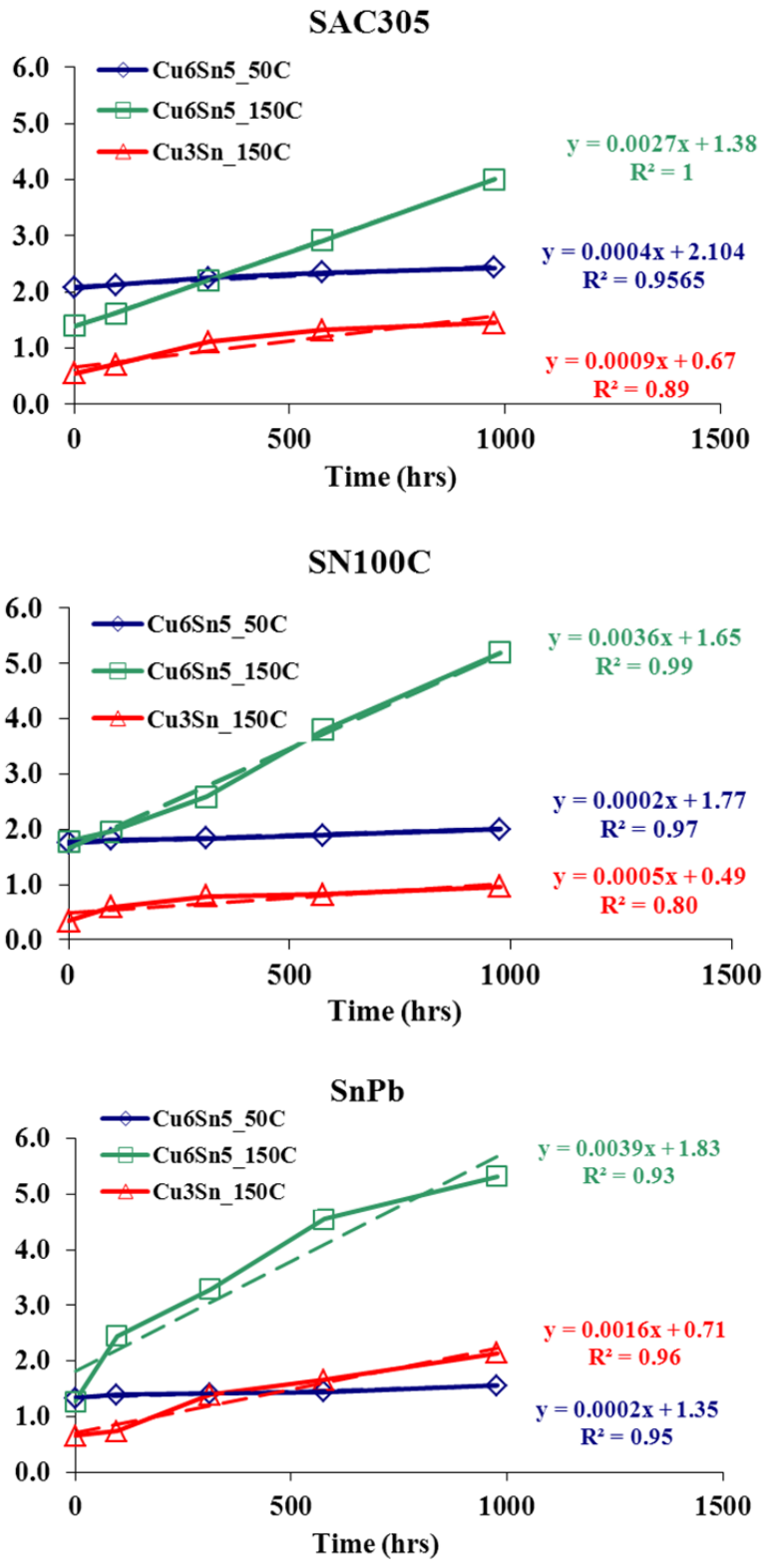


Figure 3.16: Comparison on growth rates of Cu_6Sn_5 and Cu_3Sn IMCs in (a) SAC105, (b) SAC305, (c) SN100C, and (d) SnPb solders

IMC thickness data for the solder alloys was analyzed to obtain the activation energy of Cu_6Sn_5+Cu_3Sn growth. As seen in Table 3.2, the activation energy for interfacial IMC growth at solder–substrate interface is highest for SnPb solders and lowest for SAC305 solder. The time exponent was found to be highest for SAC305 solder (= 0.85) and lowest for SnPb solder (= 0.43).

Table 3.2: Activation energies of SAC105, SAC305 and SnPb

Solder Alloy	Growth Exponent (n)	1/n	E_{avg} (kJ/mole)
SAC105	1.6	0.65	63.63
SAC305	1.2	0.85	50.10
SN100C	1.5	0.67	79.32
SnPb	2.3	0.43	89.55

3.4 Results and Discussion

Interfacial IMC thickness comparison for various aging conditions revealed scalloped formations in room temperature stored specimens. As the temperature increases, the IMCs smoothen to attain a more uniform morphology than at the room temperature. SAC305 shows highest interfacial IMC thickness followed by SAC105, SN100C and SnPb for all aging durations at 50^{o}C. At 100^{o}C, SAC305 has the highest interfacial IMC thickness at all the tested times. However, the IMC thickness in SnPb

crosses over SAC105 after aging at 1000 hours while SN100C shows least IMC thickness. At 150^{o}C, SnPb had the highest IMC thickness at all aging durations. Since the reflow temperature for lead free solders was 28^{o}C higher than that of SnPb and due to higher Sn content, the thickness of lead free solders was higher than that of SnPb. Among the lead free solders, SAC305 has the lowest melting temperature (217-219^{o}C), followed by SAC105 (215-227^{o}C) and SN100C (~227^{o}C). Thus for the same reflow temperature, there are different diffusion rates of Sn and Cu in these solders, being highest in SAC305 and lowest in SN100C. Hence SAC305 shows highest initial IMC thickness followed by SAC105 and SN100C. For specimens aged at 50^{o}C, the trend remains same since the temperature is not high enough to cause enhanced diffusion in the solders. At the aging temperature of 100^{o}C, IMC growth rate of SnPb is faster than the tested lead-free solders. This higher growth rate in SnPb solder interconnects is due to the higher homologous temperature for SnPb ($0.82T_m$) as compared to the lead-free solders ($0.66\text{-}0.69T_{m)}$. Due to the higher growth rate, the SnPb interfacial IMCs exceed those of SAC105 solder at 1000 hours and if the trends are extrapolated, the SnPb interfacial IMC thickness would also exceed the IMC thickness of SAC305 solder. The effect of higher growth rate becomes clearly evident in the specimens aged at 150^{o}C. At this temperature, an increased interdiffusion of Cu and Sn is observed in all the solders, wherein SnPb exhibiting the highest IMC growth. For SN100C solder specimens stored at room temperature and 50^{o}C, the interfacial IMC thickness is higher than SnPb solder owing to higher reflow temperature and higher Sn content. However, due to higher Cu-content in SN100C as compared to the two tested SAC solders, there is lesser tendency for the interdiffusion

of Cu and Sn. Hence SN100C has lower IMC thickness for specimens stored at room temperature and 50^{o}C and also at 100^{o}C. At 150^{o}C, SN100C shows very high growth rate of IMCs. It was found that the variation in the IMC thickness increased with the aging temperature, being highest at 150^{o}C.

Analysis of the individual IMC phases, Cu_6Sn_5 and Cu_3Sn at 50 and 150^{o}C showed that at 50^{o}C, SAC305 had the highest growth rate of Cu_6Sn_5 IMC and SnPb the lowest. At 150^{o}C, SnPb shows the highest growth rate for Cu_3Sn IMC phase owing to the high homologous temperature and SN100C the lowest. SN100C solder shows the highest growth rate for Cu_6Sn_5 because of the preferential growth of IMC phase near the solder side, whereas SAC305 shows the lowest. This happens due to the presence of Ni on the Cu pad, which inhibits the diffusion of Cu towards solder side for the growth of Cu_3Sn phase. Since the failure under high strain rate tests have been often reported at the Cu_3Sn IMC, this might be beneficial for the portable electronics application. Interfacial IMC (Cu_6Sn_5+Cu_3Sn) thickness data was used to estimate constants for the empirical Arrhenius relationship for interfacial IMC growth. The activation energy values of SAC105, SAC305, SN100C and SnPb were found to be 63.63 KJ/mole, 50.10 KJ/mole, 79.32 KJ/mole and 89.55 KJ/mole respectively.

3.5 Conclusions

This chapter examined the growth kinetics and morphology of interfacial IMC (Cu_6Sn_5+Cu_3Sn) formation for SAC105, SAC305, SN100C and SnPb solders over the temperature range of 50-150^{o}C for up to 1000 hours. The analysis of IMC phases

Cu_6Sn_5 and Cu_3Sn at 50°C and 150°C shows that the IMC growth kinetics undergoes a transition due to the growth of Cu_3Sn IMC at 150°C. At 50°C, SAC305 shows the highest growth rate of Cu_6Sn_5 IMC and SnPb the least. On the other hand at 150°C, SnPb and SN100C solders show highest growth rates for Cu_6Sn_5 and Cu_3Sn phases respectively. SnPb shows enhanced growth rates of both IMc phases due to then high homologus temperature. SN100C solder shows a preferential growth of Cu_6Sn_5 phase and lowest growth of Cu_3Sn phase due to the presence of Ni at the Cu_3Sn–Cu interface. Based on the findings, for portable electronics at higher temperature (100-150°C), SAC solders are a more reliable than SnPb solders since they have lower interfacial IMC thickness and growth rates. Reporting activation energy for the combined IMC thickness of Cu_6Sn_5 and Cu_3Sn IMC phases for the temperature range of 50-150°C is erroneous, since the IMC growth mechanism does not remain the same through the temperature range and the transition in the IMC growth cannot be accounted by this approach.

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4 Chapter 4: Effect of Isothermal Aging on Thermal Cycling Reliability of SAC305, SAC105, SN100C, and SnPb Solders

This chapter discusses the impact of isothermal aging on the thermal fatigue reliability of SAC305, SAC105, SN100C and SnPb assemblies. The test structures consist of chip resistors (CR2512 with Sn-finish) soldered to Cu/OSP-finish pads on an FR4 substrate. The test structures were subjected to isothermal aging of 50°C, 100°C and 150°C for 100, 500 and 1000 hours. 100°C/24 hours aged specimens were the reference. Subsequent, the aged structures were subjected to temperature cycling test conditions (-55°C to 125°C, 15 min dwell, ramp rate: 10°C/min) while monitoring electrical continuity. Failure identified as an electrical discontinuity was measured during the temperature cycle exposure and the impact of high temperature aging was documented. Specimens aged at 100°C for 24 hours acted as the controls for the experiment. The thermal cycling reliability of the lead-free solders was compared with that of eutectic SnPb.

4.1 Introduction

Lead-free Lead-free solders are continually being evaluated under various thermal and mechanical tests [**Error! Reference source not found.-Error! Reference source not found.**]. Tin-silver-copper (SAC) solder alloys are one of the favorable choices of the industry for the replacement of SnPb solder. Investigators have studied the effect of varying silver content in the SAC solders [**Error! Reference source not found.**]. It has been found that as the silver content is reduced,

the solder performed better under high strain-rate mechanical tests [**Error! Reference source not found.-Error! Reference source not found.**]. However, reduced silver content in SAC solders has been demonstrated to reduce temperature cycling and low strain rate mechanical cycle fatigue life [2]. Another solder gaining popularity, particularly for wave soldering operations, is the SN100C (SnCu0.7Ni) solder. The reliability performance of SN100C solder is being investigated and at the current state, researchers have reported contradictory results of reliability comparison with SAC solders [**Error! Reference source not found.Error! Reference source not found.-**]. More detailed investigations on this are underway.

One focus of lead-free investigations is the effect of isothermal aging on the solder joint durability. Electronic components undergo isothermal aging during storage and service life. Isothermal aging leads to coarsening of solder microstructure and increase in bulk and interfacial intermetallic compounds size. The effect of isothermal aging on the bulk solder microstructure has been investigated by researchers [**Error! Reference source not found.-Error! Reference source not found.**]. Zhang *et al.* [**Error! Reference source not found.**] reported the degradation of creep properties of SAC105, SAC205, SAC305, SAC405, and SnPb solders upon aging at 25, 75, 100, and 125^{o}C due to coarsening of the secondary intermetallic particles. The growth of interfacial IMCs poses a threat to solder joint reliability under high strain-rate mechanical tests since they are brittle and act as sites of crack initiation. Since growth of IMCs is a diffusion-controlled phenomenon, the time of storage and storage temperature will impact the results of solder interconnect reliability tests. The role of interfacial IMC thickness in solder joint reliability has

been studied by various researchers [**Error! Reference source not found.-Error! Reference source not found.**]. It is known that isothermal high temperature aging will impact the reliability of solder joints under high strain rate loading such as vibration and shock. Mattila *et al.* [**Error! Reference source not found.**] reported a decrease in the number of drops to failures in chip scale packages assembled with SAC solders after aging at 125^{o}C for 500 hours due to void formation and coalescence occurring in Cu_3Sn at the IMC-pad interface.

However, the impact of isothermal aging on reliability of solder interconnects under low strain rate testing, such as temperature cycling has not been a concern for tin-lead solder interconnects. However, material property changes that have been measured for tin-silver-copper solders due to room temperature and elevated isothermal aging raise concerns about the impact of isothermal aging of the solder interconnect fatigue life under low strain rate testing. Temperature cycling tests is a prominent reliability test for solders in electronic equipment [**Error! Reference source not found.-Error! Reference source not found.**]. Temperature cycle induced solder interconnect fatigue is a process of crack initiation and propagation driven by cyclic mechanical strain in the solder arising from the coefficient of temperature expansion (CTE) mismatch between the component and the printed circuit board as well as the solder and the solder interface. Under cyclic strain loading, the tin-silver-copper solders respond differently than tin-lead solders. For tin-lead solder, recrystallization and phase coarsening occurs. For tin-silver-copper solders, recrystallization of Sn grains, and the size and distribution changes of intermetallic particles in the bulk occur. Recrystallization creates grain boundaries which are

weaker compared to a homogenous crystal, especially if there are high angle grain boundaries [**Error! Reference source not found.**]. Changes in the microstructure of solder due to isothermal aging are expected to impact how the solder responds to cyclic strain imposed under a temperature cycling tests. For the temperature cycling test, there is the added complexity of continued microstructure changes due to the applied temperature as well as the imposed cyclic strain. The studies on the effect of isothermal aging on thermal cycling reliability of solders have been limited and contradictory. Choubey *et al.* [**Error! Reference source not found.**] reported the degradation of thermal cycling reliability of SAC305 solders in PBGA assemblies upon subjecting to thermal aging at 125^{o}C for 350 hours. On the other hand, Coyle *et al.* [**Error! Reference source not found.**] reported that isothermal aging at 125^{o}C for 500 hours of resistor assemblies did not influence the thermal cycling durability of SAC405, SAC305, SAC105 and SnCu solders.

To examine the impact of isothermal aging on temperature cycling reliability of solder interconnects, a set of test specimens were assembled and aged under different isothermal aging conditions followed by temperature cycling test. Time to failure of the test specimens was recorded using a common failure criteria and impact of the isothermal aging exposure levels on thermal cycling reliability was examined.

4.2 Experiment Details

Test assemblies were produced using Sn-finished 2512 resistors soldered onto OSP-finished copper pads on the surface of an FR4 substrate (see Figure 4.1). To obtain faster failures, the width of the copper pads were 1/5 the standard size or 0.025

inches wide. For this study, two tin-silver-copper solders, a tin-copper solder, and the eutectic tin-lead solder were examined. The tin-copper solder was commercially available SN100C solder which include trace amounts of nickel and germanium. The tin-silver-copper solders include the more conventional SAC305 which has the composition of 96.5%Sn 3.0%Ag 0.5%Cu by weight and SAC105, which has the composition of 98.5%Sn 1.0%Ag 0.5%Cu by weight. Ten resistors assemblies per solder type per aging conditions were tested.

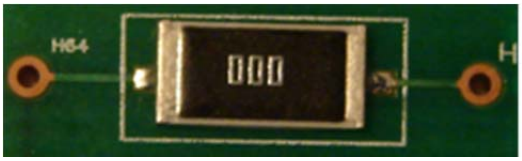


Figure 4.1: FR4 Test board with 2512 Resistors

The individual sets of assemblies were subjected to isothermal aging of 50°C, 100°C and 150°C for 100, 500 and 1000 hours. A separate set of assemblies was aged at 100°C for 24 hours to act as the control for the experiment.

Table 4.1: Test Matrix

Solder Pastes : SAC305, SAC105, SN100C and SnPb			
Temperature (°C)	**Aging Duration (hours)**		
	100	**500**	**1000**
50	√	√	√
100	√	√	√

150	√	√	√

The temperature cycling test condition was set to be -55°C to 125°C with 15 min dwell, ramp rate and approximately 10°C/min ramp. Test specimens are electrically monitored and tests were conducted till all the specimens failed. The failure is defined as the first interruption of electrical continuity that is confirmed by nine additional interruptions within an additional 10% of the cyclic life (IPC-SM-785). The interruptions are defined as the resistance spikes (>25 ohms) for periods greater than 1 microsecond. Individual test specimens were removed from the test chamber after failure was identified. Figure 4.2 shows the thermal cycling profile for the experiment. Total cycle time was 72 minutes.

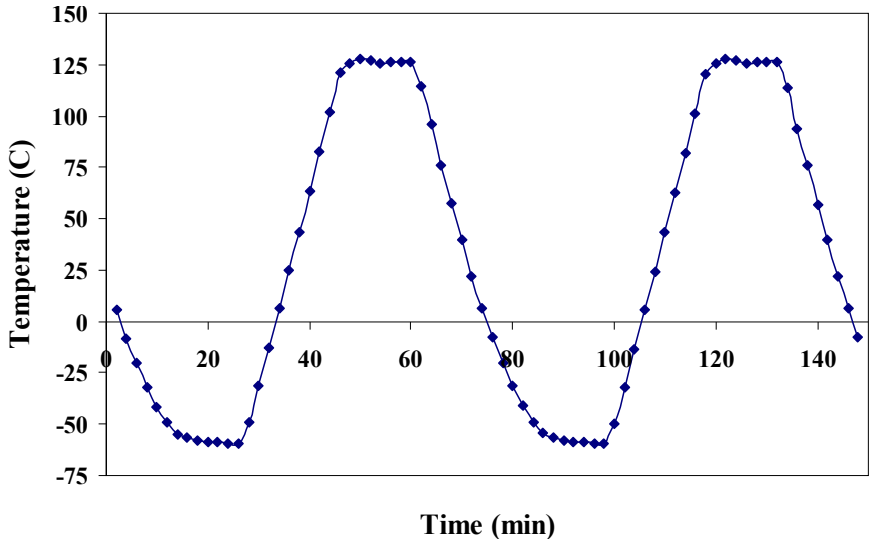
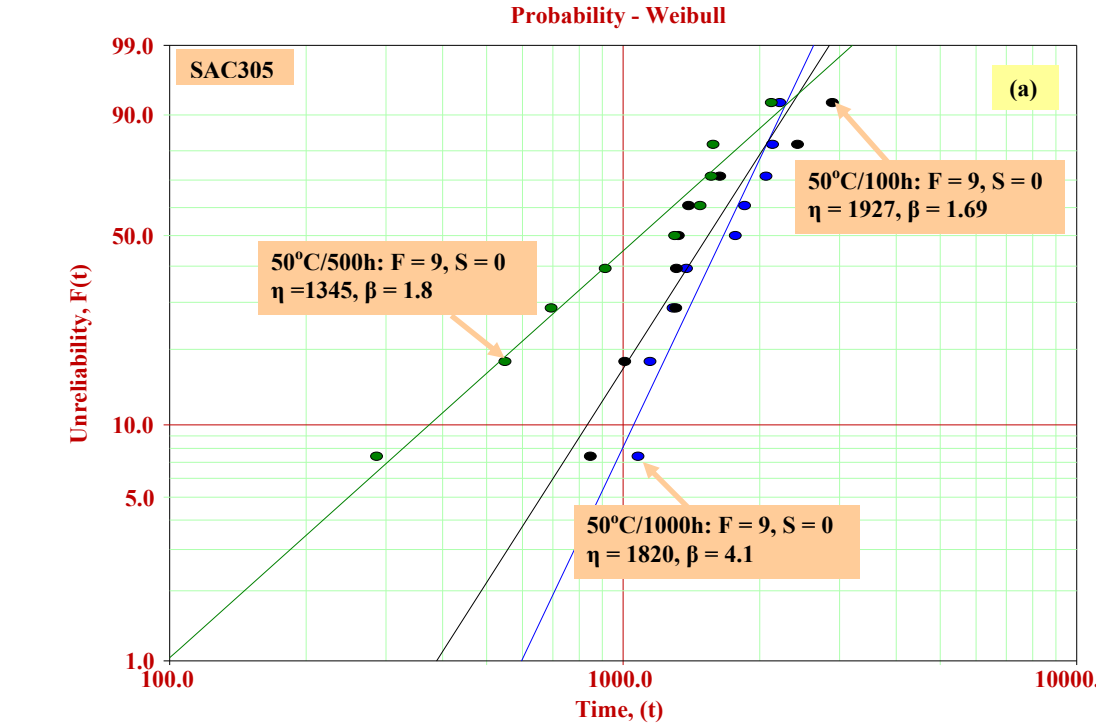
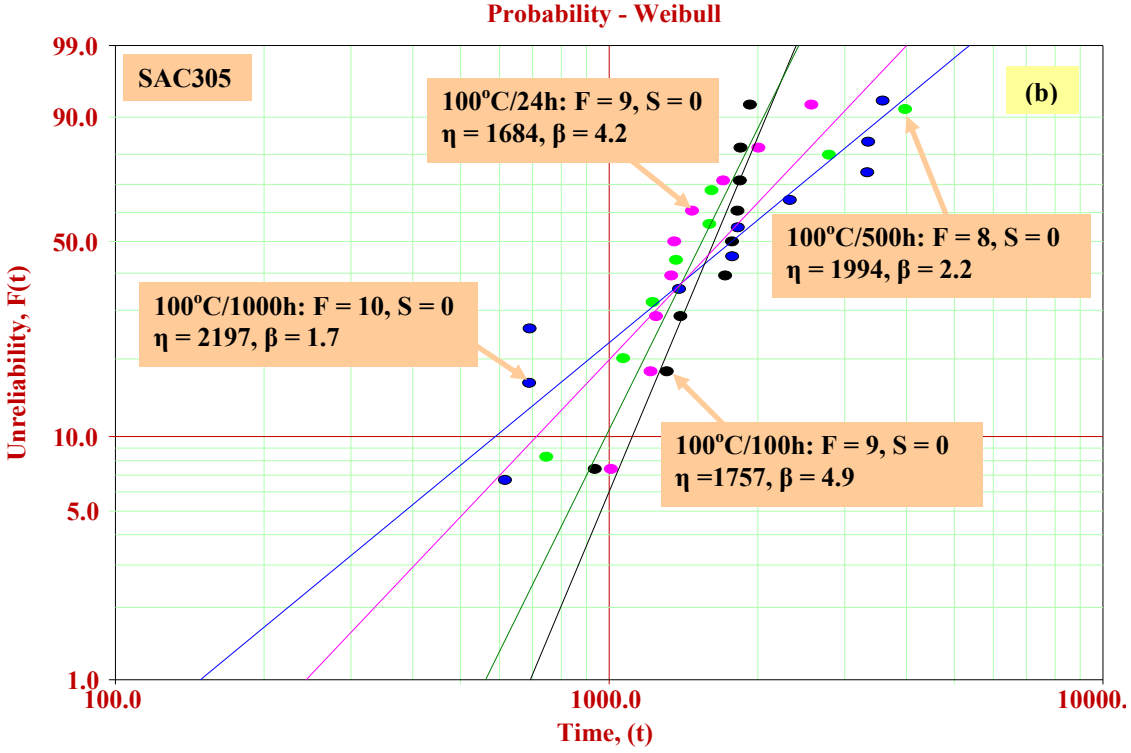


Figure 4.2: Temperature Cycle Profile

4.3 Results

The obtained failure data was plotted using Weibull two-parameter distribution and reliability comparisons were made.





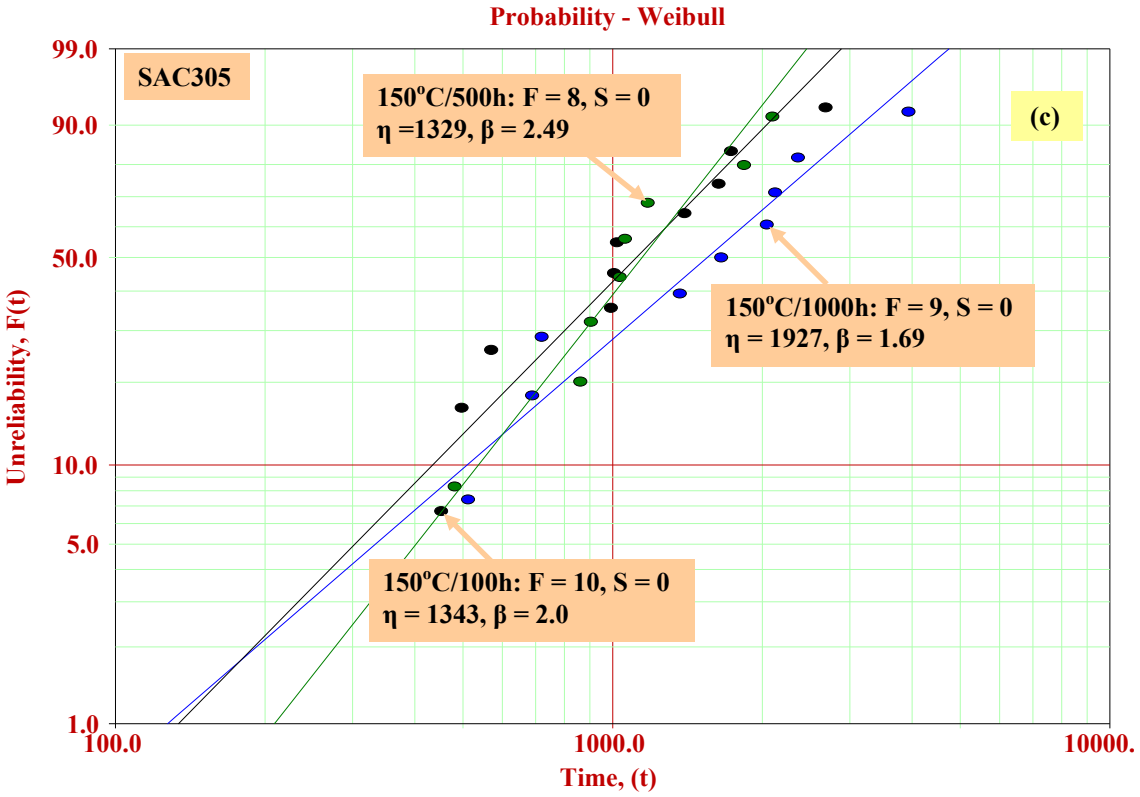
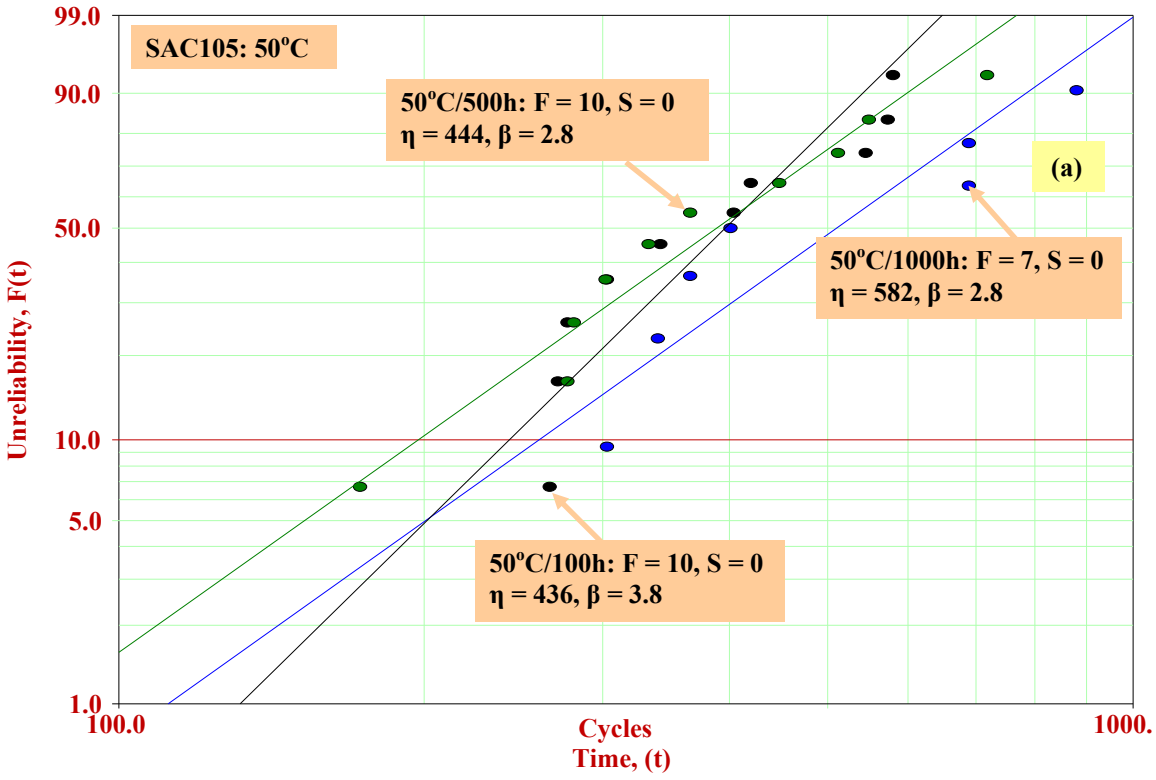
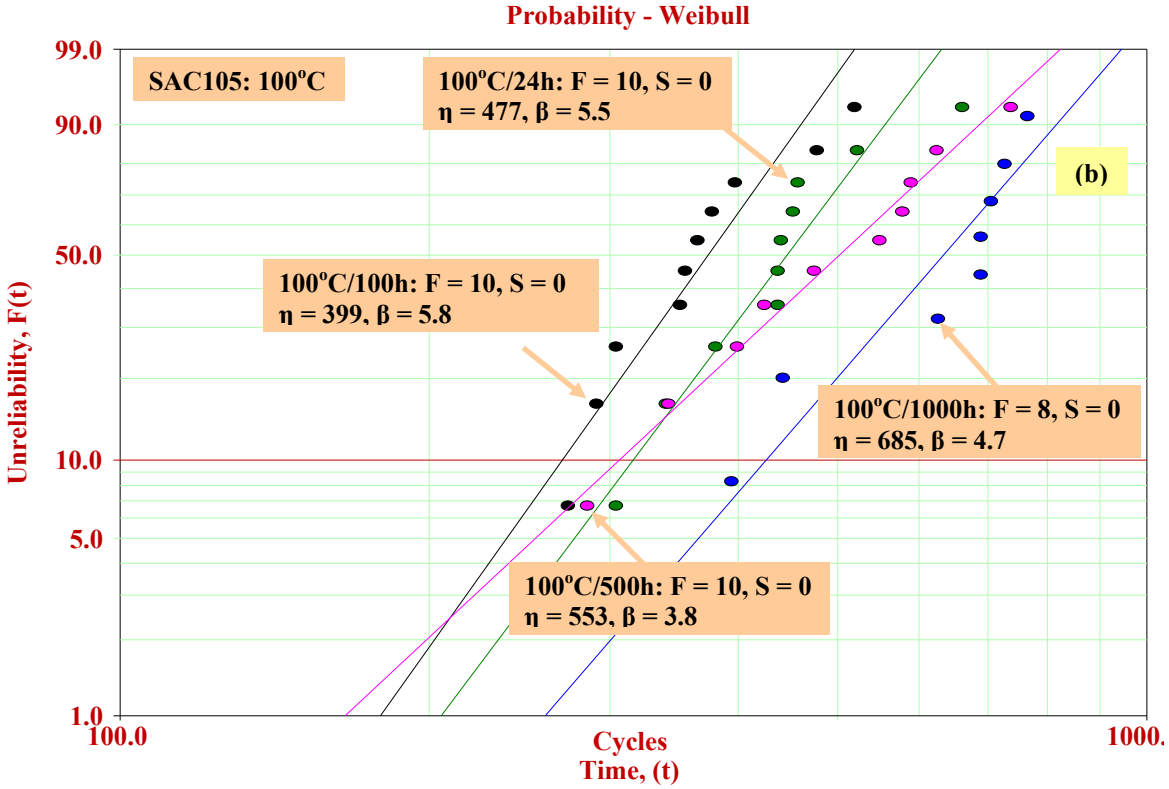


Figure 4.3: Effect of isothermal preconditioning on the thermomechanical reliability of SAC305 solder joints at (a) 50°C, (b) 100°C and 150°C.

Figure 4.3 (a-c) shows the effect of thermal aging at given temperature and durations on reliability of SAC305. The reliability of SAC305 does not change as a result of aging duration for the aging temperatures of 50, 100 and 150°C. Although isothermal aging leads to a coarsened microstructure and higher interfacial IMC growth but this does not seem to have a significant effect on the solder durability. For SAC105 solders, at low aging temperature (50C), aging duration seems to have no effect on the solder durability. As the aging temperature is increased to 100C and 150C, the impact of aging duration on reliability is observed. SAC105 reliability increases with aging (see Figure 4.4 (a-c)).


SAC105: 50°C
50°C/500h: F = 10, S = 0
η = 444, β = 2.8
(a)
50°C/1000h: F = 7, S = 0
η = 582, β = 2.8
50°C/100h: F = 10, S = 0
η = 436, β = 3.8
99.0
90.0
50.0
10.0
5.0
1.0
Unreliability, F(t)
100.0
Cycles
Time, (t)
1000.


Probability - Weibull
SAC105: 100°C
100°C/24h: F = 10, S = 0
η = 477, β = 5.5
(b)
100°C/100h: F = 10, S = 0
η = 399, β = 5.8
100°C/1000h: F = 8, S = 0
η = 685, β = 4.7
100°C/500h: F = 10, S = 0
η = 553, β = 3.8
99.0
90.0
50.0
10.0
5.0
1.0
Unreliability, F(t)
100.0
Cycles
Time, (t)
1000.

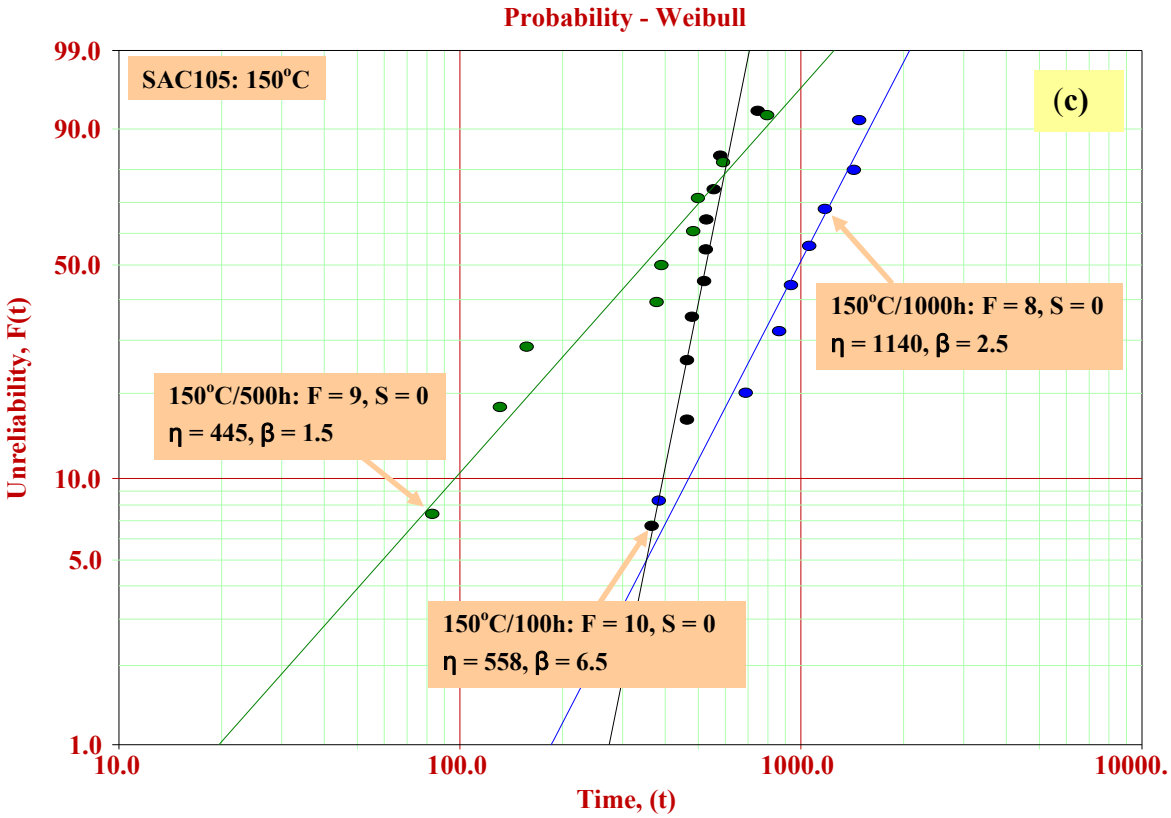
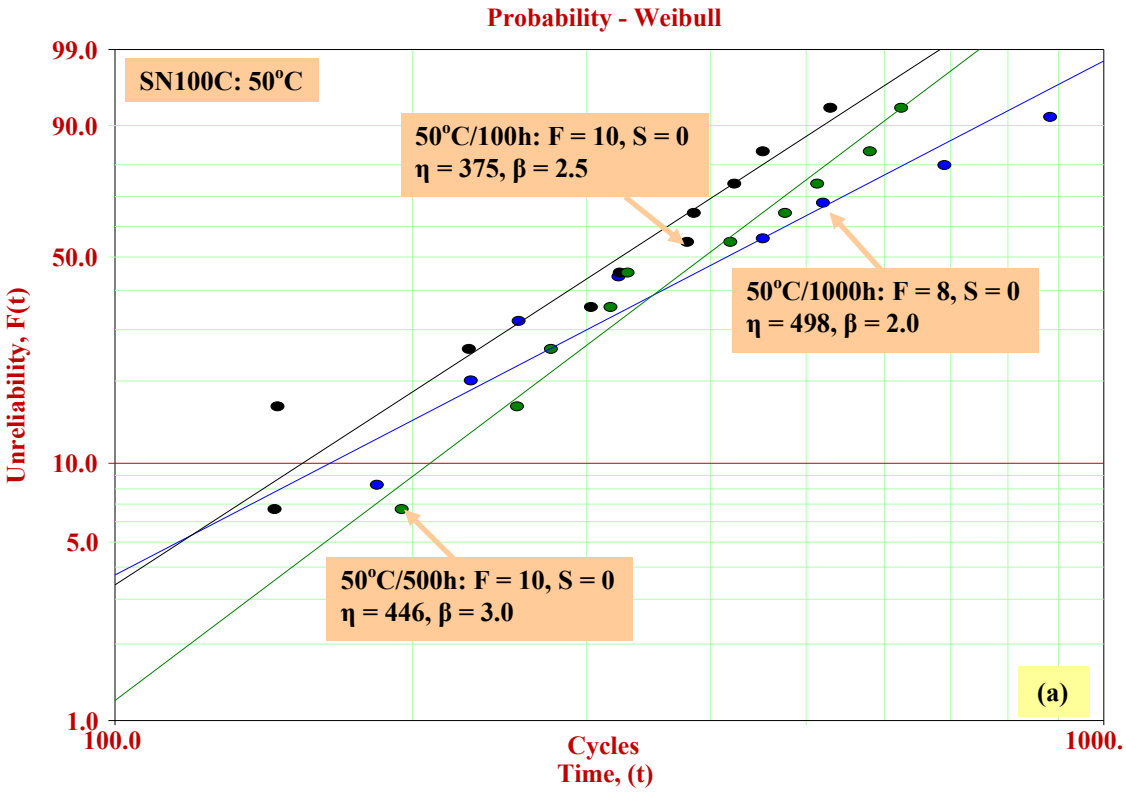
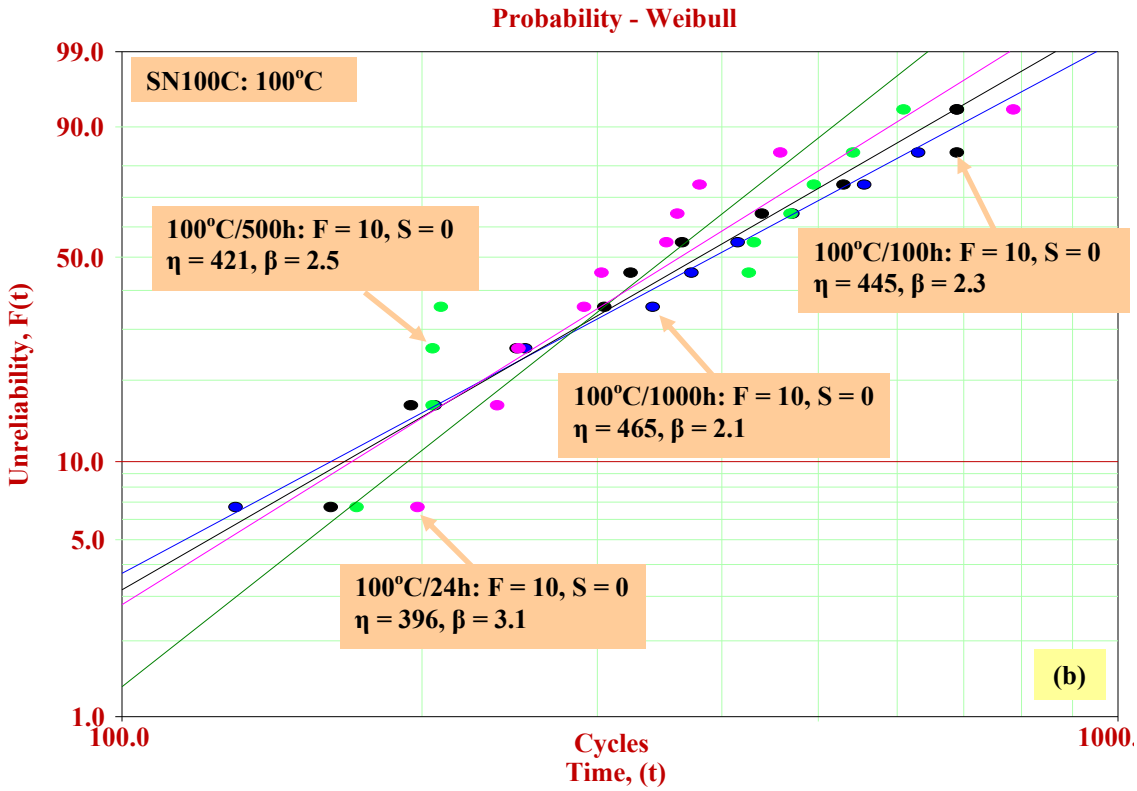


Figure 4.4: Effect of isothermal preconditioning on the thermomechanical reliability of SAC105 solder joints at (a) 50°C, (b) 100°C and 150°C.

For SN100C solders aging at 50, 100 and 150°C for upto 1000 hours does not seem to influence the temperature cycling reliability and the failure times of the population seems indistinguishable (see Figure 4.5).


Probability - Weibull
SN100C: 50°C
50°C/100h: F = 10, S = 0
η = 375, β = 2.5
50°C/1000h: F = 8, S = 0
η = 498, β = 2.0
50°C/500h: F = 10, S = 0
η = 446, β = 3.0
(a)
99.0
90.0
50.0
10.0
5.0
1.0
Unreliability, F(t)
100.0
1000.
Cycles
Time, (t)


Probability - Weibull
SN100C: 100°C
100°C/500h: F = 10, S = 0
η = 421, β = 2.5
100°C/100h: F = 10, S = 0
η = 445, β = 2.3
100°C/1000h: F = 10, S = 0
η = 465, β = 2.1
100°C/24h: F = 10, S = 0
η = 396, β = 3.1
(b)
99.0
90.0
50.0
10.0
5.0
1.0
Unreliability, F(t)
100.0
1000.
Cycles
Time, (t)

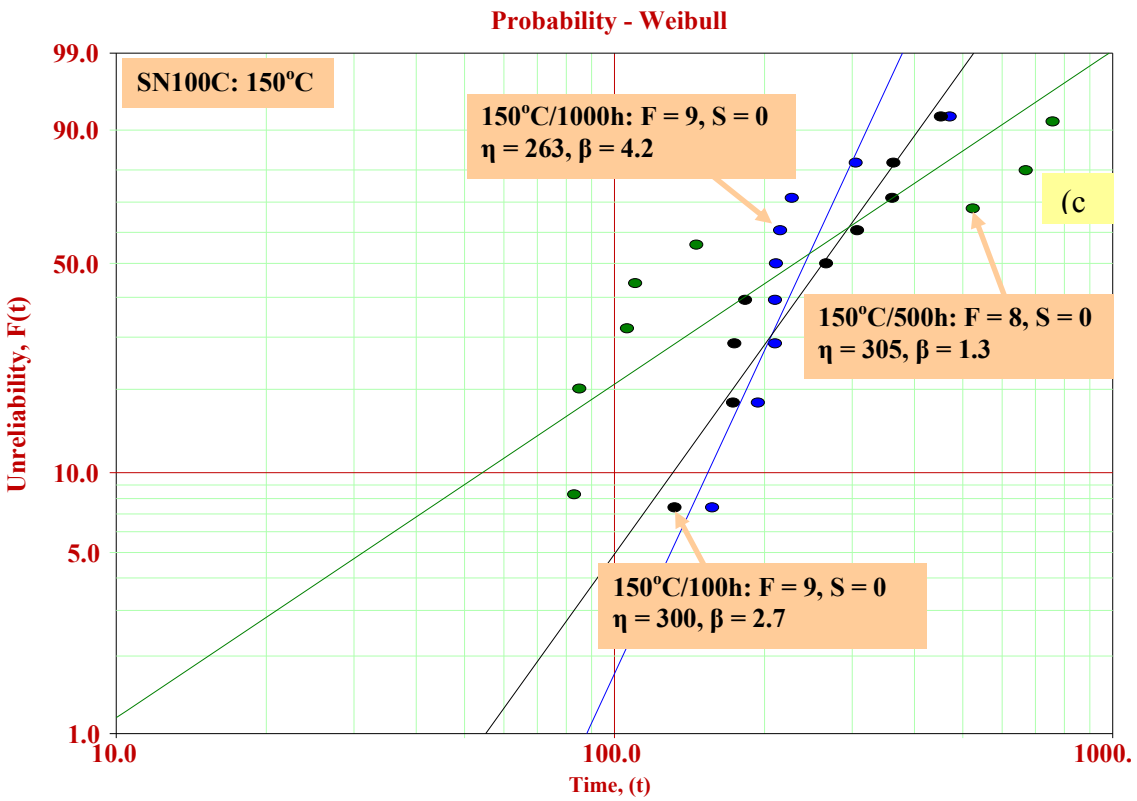
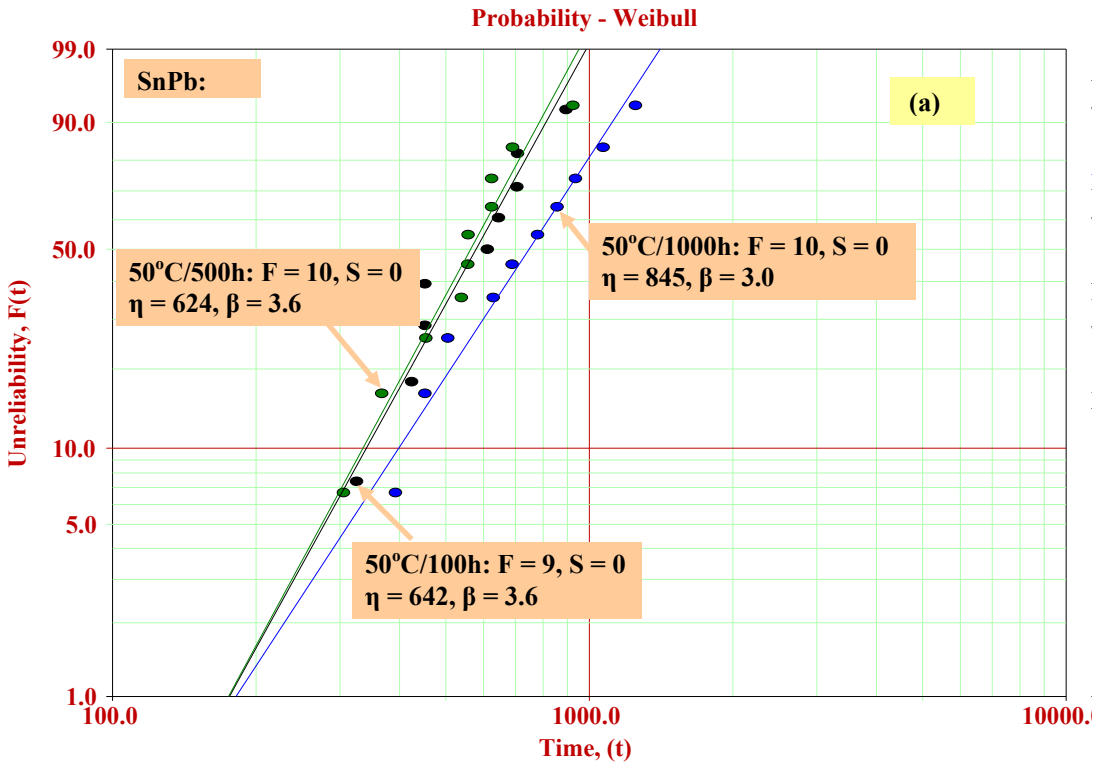
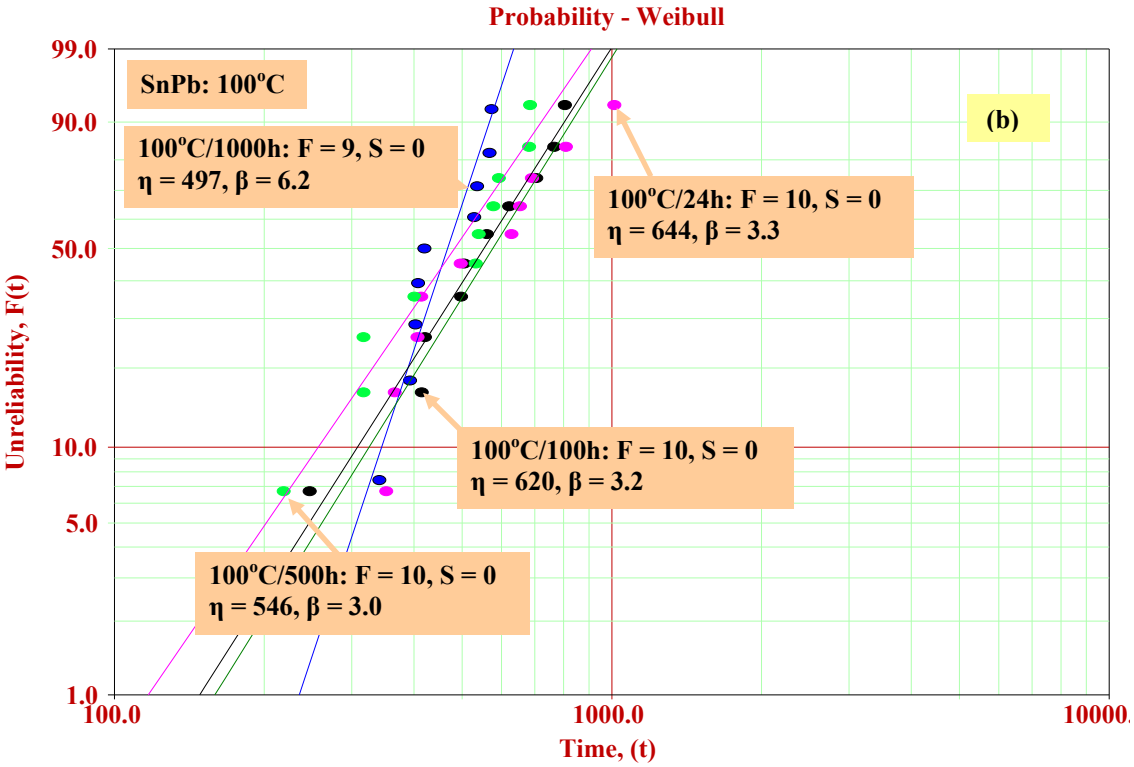


Figure 4.5: Effect of isothermal preconditioning on the thermomechanical reliability of SN100C solder joints at (a) 50°C, (b) 100°C and 150°C.

For SnPb solders, aging for upto 500 hours does not seem to have an influence on the thermal cycling reliability. Aging at 1000 hours seems to have a positive influence on the reliability. For aging at 100°C, there does not seem to be any influence on the reliability. For 150°C aged specimens, reliability improves upon long term aging of 1000 hours (see Figure 4.6).


Probability - Weibull
99.0
90.0
50.0
10.0
5.0
1.0
Unreliability, F(t)
SnPb:
(a)
50°C/500h: F = 10, S = 0
η = 624, β = 3.6
50°C/1000h: F = 10, S = 0
η = 845, β = 3.0
50°C/100h: F = 9, S = 0
η = 642, β = 3.6
100.0
1000.0
10000.
Time, (t)


Probability - Weibull
99.0
90.0
50.0
10.0
5.0
1.0
Unreliability, F(t)
SnPb: 100°C
(b)
100°C/1000h: F = 9, S = 0
η = 497, β = 6.2
100°C/24h: F = 10, S = 0
η = 644, β = 3.3
100°C/100h: F = 10, S = 0
η = 620, β = 3.2
100°C/500h: F = 10, S = 0
η = 546, β = 3.0
100.0
1000.0
10000.
Time, (t)

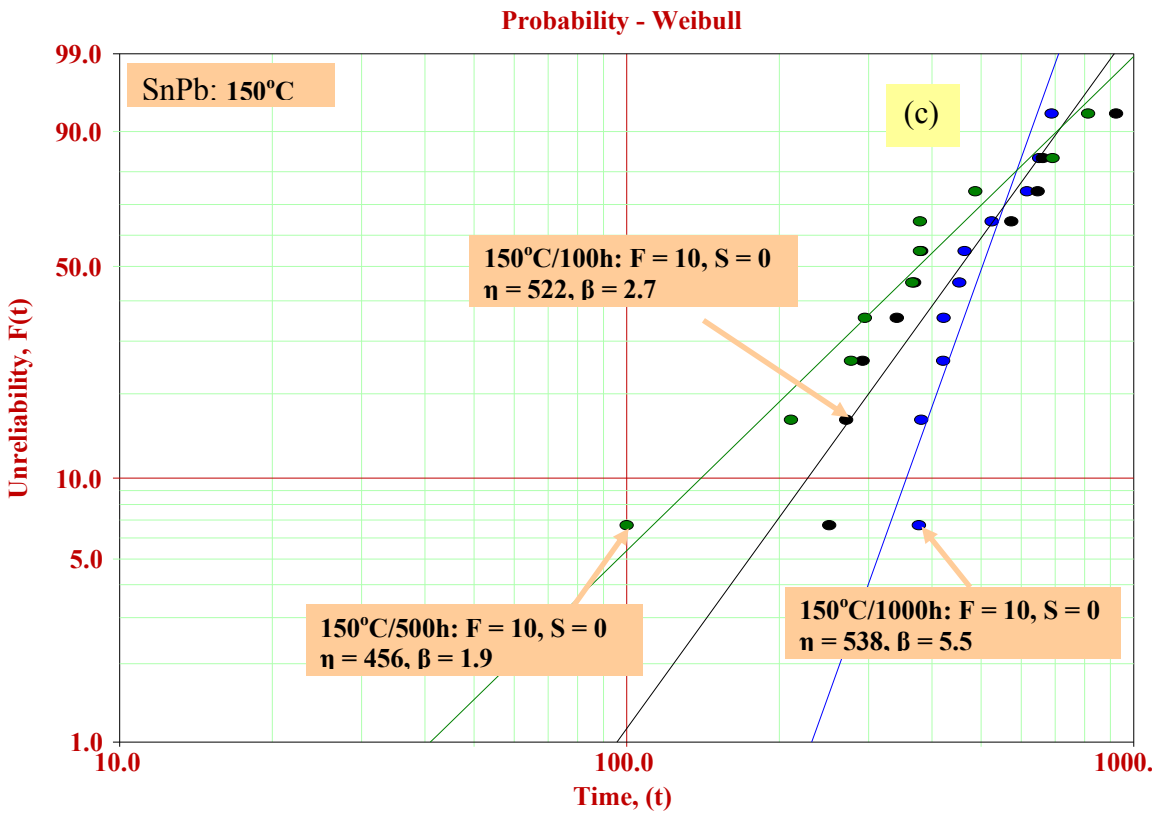


Figure 4.6: Effect of isothermal preconditioning on the thermomechanical reliability of SnPb solder joints at (a) 50°C, (b) 100°C and 150°C.

Above results suggest that temperature cycling fatigue reliability of SAC105 solders improves with aging at select temperature levels. For SAC305 solder the general trend at 150°C is an improvement in reliability. On the other hand, SnPb and SN100C solders see no effect of isothermal aging on their reliability.

Next, the effect of thermal cycling on the solder microstructure is studied. Figure 4.7 show the comparison of preconditioned specimens with the ones subjected to thermal cycling after preconditioning. It is seen that comparison of solder microstructure between the isothermally aged cycled and non-cycled specimens. Significant coarsening is observed as a result of thermal cycling. A comparison between (c) and (d) in Figure 4.7 shows that additional isothermal aging up to 1000

hours only cause very small changes in the size and distribution of then Pb-rich phase. However, the effect of only a few thermomechanical cycles causes a significant change in the microstructure. Figure 4.7 clearly shows grain boundaries which might be used as diffusion paths and cause the faster coarsening especially in the crack region of the solder joint.

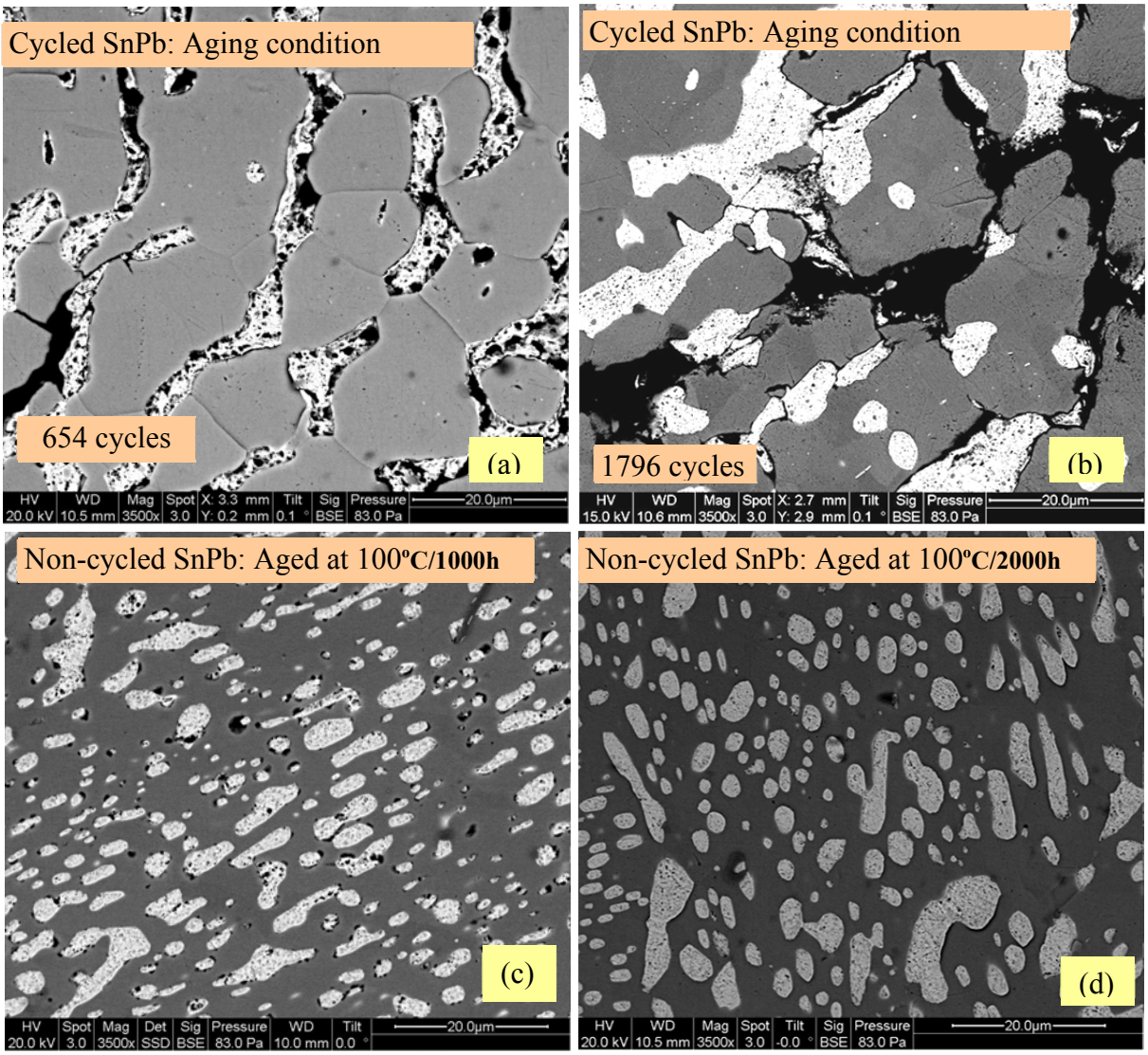


Figure 4.7: SnPb microstructure in non-cycled and cycled aged specimens aged at 100°C/24h

4.4 Failure Analysis

Failures in the temperature cycling test were identified by measured increases in electrical resistance of electrical circuits that included copper board traces, solder, and resistor. Failure analysis was conducted to identify the failure site. Analysis includes electrical probing, optical inspection, and in select circumstances cross-sectioning and electron microscope inspections. Inspections were conducted to determine the cause of early failures and to determine the differences in failure site due to solder material and aging condition.

For the most part, little difference in solder interconnect failures could be determined from electrical probing and optical inspection. Electrical probing isolated the failure to the solder interconnects and resistor. In most cases, a crack in the solder joint was visible under 30X or higher magnification on one or both solder interconnects for each test specimen. To examine the failure in more detail, select specimens were molded in epoxy, cross-sectioned, and examined under an electron microscope. The remainder of this section provides a discussion of the finding from the electron microscope inspection.

SAC105: The SAC105 solder interconnects appear to be composed predominately of tin with minute randomly distribute intermetallic particles. Examination of specimens that failed early in test revealed the presence of large voids. Examples are depicted in the figures to follow.

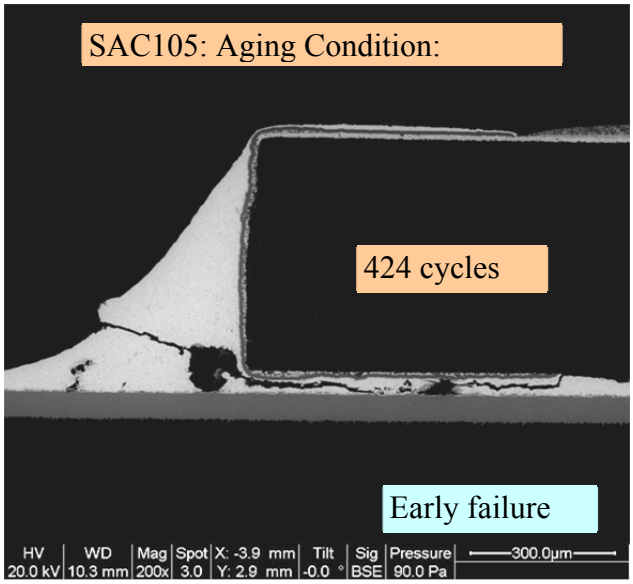


Figure 4.8: Early failure in SAC105 specimen aged at 100C/500h

Void assisted early failures in the samples. The crack propagation in other early failures was at an angle less than 10 degree. Long lasting samples saw a higher angle of crack propagation.

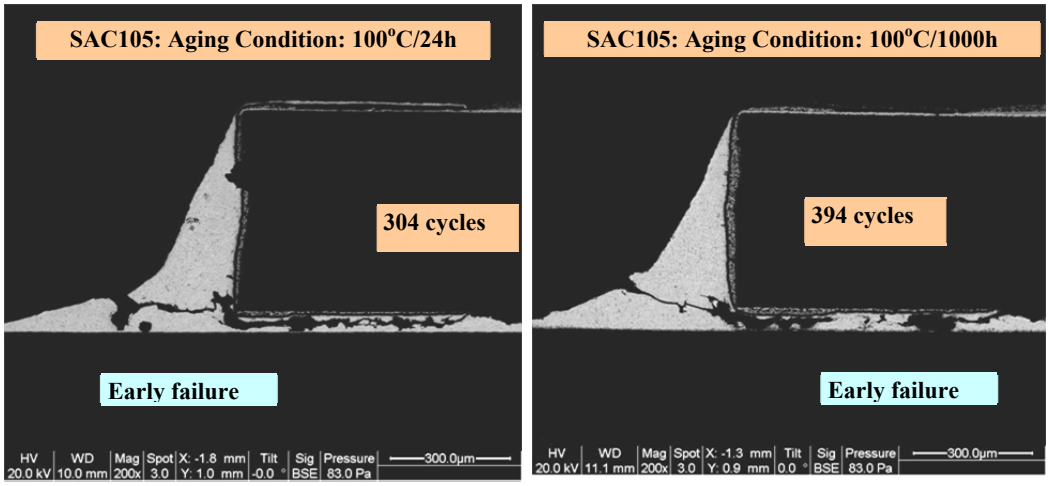


Figure 4.9: Early failures in SAC105 specimen aged at 100C/24h and 1000h

SAC305: Similar to SAC105, early failures in SAC305 were driven by presence of voids in the solder. However, a significant finding from the FA was the angle of

crack propagation in SAC305 solders. All the samples had an angle of crack propagation equal or higher than 45^{o}. Also, SAC305 samples showed multiple weblike cracks instead of one single crack. Typical failures in SAC305 samples occurred in both the joints on the components. All the failures were in the non-interfacial region. SAC305 showed highest angle of crack propagation among all the solders.

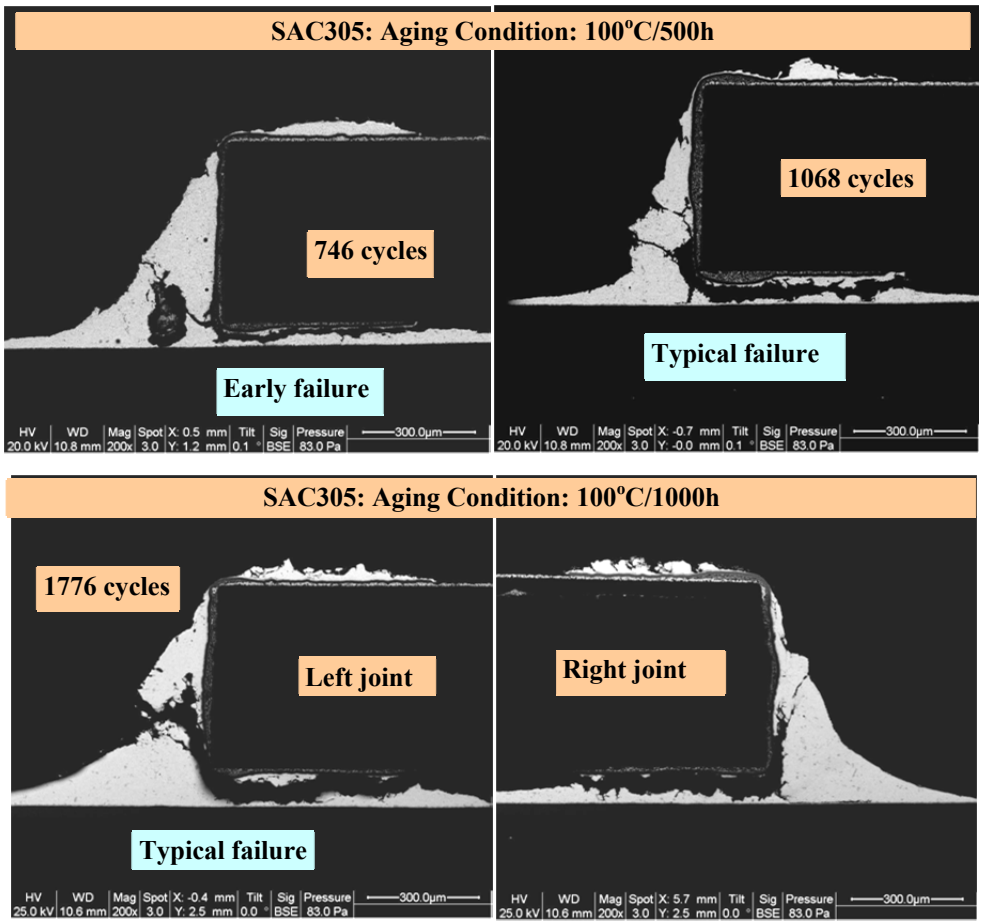


Figure 4.10: Failures in SAC305

SAC305 lasted the longest among all the tested solders. Failure analysis of SnPb solders also revealed that early failures were assisted by the presence of voids in the

solders. Additionally, components failing early follow a lower angle crack propagation path. The long-lasted components exhibited higher angle of crack propagation and multiple crack phenomena as shown by SAC305 solders. All the failures occurred by crack initiation and propagation through the non-interfacial region. SN100C failures occurred by the crack initiation and propagation along the non-interfacial region. The crack propagation in early failures took place at very low angles ($<20^{o}$). The longer the failure time, the higher is the angle of crack propagation.

4.5 Summary of Thermal Cycling Test Results

The effect of isothermal aging on the thermal fatigue reliability of SAC105, SAC305, SN100C and SnPb solders was examined. For solders, aging at 50^{o}C does not affect the thermal cycling reliability since aging at this temperature does not alter both the interfacial and the bulk microstructure. Isothermal aging at 100^{o}C seems to improve the reliability of SAC solders upon long term aging. SAC solders also showed a decrease in the weibull shape parameter with aging which indicates more scatter. SnPb and SN100C see no observable impact in temperature cycling solder interconnect fatigue reliability due to isothermal aging. A comparison of the thermal fatigue durability across the solders at the given aging conditions reveals SAC305 to be the most reliable amongst all the solders for the defined -55 to 125^{o}C temperature cycle. This is due to the higher silver content in the SAC305 solder leading to increased creep and fatigue resistance. After SAC305 at the 100°C/100 hour aging condition, SnPb was found to have the next highest temperature cycle fatigue

resistance followed by SAC105 and SN100C. Like SAC305, the temperature cycling fatigue reliability of SAC105 improves with aging duration. At 500 hours of aging, SAC105 shows similar reliability as that of SnPb followed by SN100C. After 1000 hours of aging SAC105 surpasses the reliability of SnPb, being next only to SAC305whereas SnPb and SN100C show similar reliability. Failure analysis of the components revealed that the presence of voids caused the early failures in the components. It was also observed that the higher the reliability of the component, the higher is the angle of crack propagation in it. Also, SAC305 showed highest angle of crack propagation among all the tested the solders, which correlates well with the thermal cycling results. One very important finding in the failure analysis was the role of solder-Cu pad interface in the crack propagation, wherein the crack propagated through the non-interfacial region. This suggests a very important finding, that the interfacial IMCs whose thickness is a direct consequence of elevated temperature isothermal aging, do not play any role in the reliability under thermal fatigue.

4.6 References

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5 Chapter 5: Evaluation of Current Carrying Capacity of SAC305, SAC105, SN100C and SnPb Solders

The chapter experimentally examines the direct current carrying capacity of Sn96.5Ag3.0Cu0.5, Sn98.5Ag1.0Cu0.5, Sn97.3Cu0.7+0.05Ni and eutectic SnPb solder joints in resistor assemblies assembled on standard and reduced width pad configurations. Copper vias, traces and pads, solder joints and resistor form the electrical path. The current densities in copper traces ranged from 4.07×10^2A/cm^2 to 6.1×10^3 A/cm^2. It was found that Sn96.5Ag3.0Cu0.5 solder had the highest current carrying capacity and lowest temperature rise, followed by Sn98.5Ag1.0Cu0.5, SnPb and Sn97.3Cu0.7+0.05Ni solders. 4-wire resistance measurements revealed that the electrical resistance of test assemblies was independent of the solder composition.

5.1 Introduction

Electronics industry is rapidly moving towards higher integration and miniaturization along with better performance. The I/O numbers are increasing while the size of solder joints is progressively shrinking, leading to the higher current densities in the solder joints. The design rule of packaging requires solder bumps to carry 0.2–0.4 Amps [1]. Hence, for a solder bump with 50 μm diameter to carry 0.2 Amps of current, the resulting current density is of the order of 10^4 A/cm^2. The current density increases further with the decrease of chip voltage and increase of absolute current levels [2]. Common failure mechanisms under high current densities are Joule heating, electromigration, and thermomigration. Joule heating generated by the on-chip metal interconnects is a critical issue in high-density packaging. Due to

their small cross-sectional area, metal traces experience high current densities and hence high joule heating. The high temperatures at the traces in turn lead to increased temperatures in the adjacent solder joints. Solder being a low-melting point component; it is very sensitive to temperature. During the operational life, solder joint temperature might reach around 100^{o}C, resulting in a homologous temperature of $0.8T_m$ and $0.5T_m$ in eutectic SnPb and SAC305 solder respectively. The high current densities along with high homologous temperature of the solder joints lead to diffusion of atoms across the lattices, making electromigration a challenge in the high density packages. Additionally, at the entry and exit locations of the current, current crowding occurs, causing localized heating at those locations. Due to the heat accumulation and differences in conductivities of various parts of the solder circuit, thermomigration is also a concern.

For electromigration studies, the industry focus is primarily on small solder joints such as flip chip solder bumps and wafer level packages for both lead-based and lead-free solders [3-29]. Tu *et al.* [30] reported that the mechanism of electromigration for aluminum, copper and tin-lead is grain boundary diffusion, surface diffusion, and lattice diffusion respectively. Rinne [28] reported that the failure rate due to electromigration depends on alloy composition, operating temperature, and current density. Alam *et al.* [3] reported a review of the high current induced damages in solder joints. Electromigration, thermomigration, intermetallic compound growth, current crowding, under bump metallization (UBM) dissolution, joule heating and solder melting was reported.

Researchers have also investigated the failure modes under current stressing loading [4, 19, 31]. Shao *et al.* [24] investigated the effect of high current stressing on 95.5Sn4.0Ag0.5Cu solder joints in wafer level chip scale package (CSP) subjected to the current levels of 0.5A, 0.6A, 0.7A, 0.8A, and 0.9A, at the ambient temperature of 125^{o}C. They reported the failure modes to be trace aluminum breakage. The trace temperature due to joule heating was not high enough to cause trace melting (T_m of Al is 660^{o}C). Electromigration was the driving phenomenon for trace thinning which in turn was responsible for the increase of Joule heat that led to trace melting and the subsequent failure. Hu *et al.* [7] studied the electromigration failure mechanism in SnPb flip chip solder joints under the current density of 2.5×10^4 A/cm^2 at 100^{o}C. The solder joint failure occurred due to break in electrical continuity due to rapid dissolution of copper at the cathode side enhanced by the current crowding. Nah *et al.* [32] reported the mechanism of electromigration-induced failure in a composite solder joint consisting of Sn3Pb on the chip side and Sn63Pb on the substrate side under the current density of $2.55x10^4$A/cm^2 at 140^{o}C. Failure was reported at cathode side due to copper UBM consumption. They further reported that growth of Cu_6Sn_5 IMCs caused a fast consumption of copper UBM and the accompanying void formation induced the failure. In another study [31], the electromigration behavior of SnAg3.5 solder bumps under the current densities of $1x10^4$ A/cm^2 and $5x10^3$ A/cm^2 at 150°C was examined. At the current density of $1x10^4$ A/cm^2, damage occurred in both the anode/chip side and the cathode/chip side. However, under the current stressing of $5x10^3$ A/cm^2, failure occurred only in the cathode/chip side. The three-dimensional simulation of the current-density distribution revealed that the current-

crowding effect caused the failure at the cathode–chip side. At higher current density ($1x10^4$ A/cm^2), the induced thermal gradient caused the atoms to migrate from the chip side to the substrate side due to thermomigration, contributing to the failure in the anode–chip side. Ye *et al.* [18] investigated the mechanism of electromigration damage in flip chip solder joints. Eutectic SnPb flip chip solder joints were studied under electrical current density of $1.3x10^4$ A/cm^2 at ambient room temperature for up to 37.5 hours. Mass accumulations near the anode and void nucleation near the cathode were observed during current stressing. Yiping *et al.* [23] investigated the effect of under bump metallization thickness on the electromigration failure. They reported that thicker under bump metallization (UBM) layer delays electromigration failure and prolongs mean time to failure in the wafer level chip scale packaging solder joints. Lai *et al.* [9] investigated the effect of copper content on the electromigration reliability of SAC solders. Sn3Ag0.5Cu and Sn3Ag1.5Cu/Sn3Ag-0.5Cu composite flip-chip solder joints with Ti–Ni(V)–Cu UBM were stressed at current density of $5x10^3$ A/cm^2 at 150°C. They reported that Sn3Ag1.5Cu/Sn3Ag-0.5Cu composite flip-chip solder joints had a longer electromigration life than Sn3Ag0.5Cu solder joints. Greater Cu weight content may retard the diffusion rate of Sn towards the UBM, and hence enhance the electromigration reliability.

Other effects of stressing include deterioration of mechanical properties and increase in the interfacial IMC thickness increase. Ye *et al.* [17] reported a deterioration in the mechanical properties of SnPb solder due to current stressing. Nano-indentation tests showed that elastic modulus of solder joint decreased during high current density ($1x10^4$ A/cm^2) stressing. The decrease of modulus was localized

in the area of void nucleation during current stressing. Wang *et al.* [13] studied Sn3.5Ag0.5Cu BGA solder joints at a current density of $2.2x10^4 A/cm^2$ at 180^oC for 11 hours. They compared the IMC thickness of thermal aged samples with samples subjected to current stressing at 180^oC and reported that IMCs at the anode and cathode are both thicker than those in the thermal aging experiment. They also reported a difference in IMC thickness at anode and cathode due to current stressing.

Different lead-free solders are expected to behave differently under high current stressing due to their unique material compositions. At this writing, studies to determine a suitable lead-free solder for high current density applications are very few and limited in scope. So far the studies have focused on determining the effect of temperature and current on electromigration of solders (limited to SnPb, SAC305 and Sn3.5Ag) [12, 22]. Choi *et al.* [26] investigated electromigration in eutectic SnPb and SAC flip chip solder joints and their mean-time-to-failure in the temperature range of 100–140°C with current densities of $1.9–2.75x10^4$ A/cm^2. They reported that the mean time to failure for SAC solder was higher than SnPb solder. They verified current crowding by a simulation of current distribution in the solder joints. With the introduction of new lead-free solders, it is important to understand the current carrying limit of these solders to find a suitable lead-free alternative for high current density applications.

This chapter determines current carrying capacity of the SAC305, SAC105, SN100C soldered resistor assemblies. The current levels are varied from 0.5A–7.5A in the steps of 0.5A and the temperature near the solder joints is recorded.

5.2 Experiment Details

The test assemblies consist of 2512 chip resistors soldered onto copper pads on a FR4 printed circuit board (PCB). The vias, copper traces and pads, solder and resistor form the conductive path. SAC305, SAC105, SN100C and SnPb solders on standard and reduced pad (20% pad width) configurations (Figure 5.1) were examined. The width of standard and reduced pads was 3103.3 μm and 615.8 μm respectively.

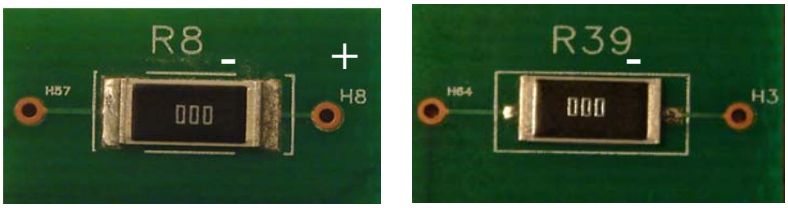

Figure 5.1: Test specimens (a) standard, (b) reduced pad configurations

Table 5.1 shows the cross-sectional area of copper trace and the two configurations of solder joints. It is seen that copper trace has lowest cross-sectional area and thus would experience highest current density for a given current level. Also, reduced pad solder joints would experience higher current density than standard joint.

Table 5.1: Cross-sectional areas of copper trace, narrow and standard pad solder joints

Cross-sectional area (cm^2)	**Cu trace**	**Reduced pad solder joint**	**Standard pad solder joint**
	8.9×10^{-5}	2.44×10^{-4}	1.23×10^{-3}

Table 5.2 shows the resistivity values of the test solders and copper trace and pads along with Sn and Ag as reported in literature. It may be seen that the resistivity of lead-free solders is lower than that of SnPb solder. Also, the resistivity of SAC305, SAC105 and SN100C is similar.

Table 5.2: Resistivity values [33]

Material	**Resistivity (Ωμcm)**
Cu	1.72
63Sn37Pb	14.5
SAC305	13.2
SN100C	13[34]
SAC105	13.3
Sn	12.4
Ag	1.63

Table 5.1 suggests that copper traces would experience higher current density than both standard and narrow pad solder joints and might be the limiting factor in the current carrying capacity of the test assembly. Therefore, the first step is to determine the current carrying capacity of copper traces. Theoretical fusing current of copper trace is given by Equation 1 [35]: where I is current in Amps, ΔT is the temperature rise, W is the width of the trace, T is the thickness of the trace (mil).

$$I = 0.025 \times \Delta T^{0.45} W^{0.79} T^{0.53} \qquad \text{Eqn. 1}$$

The above theoretical formulation is valid for external traces only. Melting point of copper is 1083°C, width of copper trace is 10.00 mils, thickness of copper trace is 1.38 mils, average ambient temperature is 32°C, ΔT = 1083-32 = 1052°C. The obtained current and current density limits are 4.2 Amps and the $4.7 \times 10^4 A/cm^2$ respectively.

The obtained theoretical value of fusing current was compared with the experimental data. Tests were carried out at constant current levels from 0.5–7.5 Amps in the steps of 0.5 Amps at room temperature. Four test specimens per current level were tested. Temperature was recorded on top of the resistor component (the temperature at the top of the component was similar to that at the solder joint) using K-type thermocouples every 10 seconds. Failure was defined as loss of electrical continuity and time to failure of test assemblies was recorded. Failure analysis was performed by means of optical inspection, and scanning electron microscopy (SEM) to identify the failure sites. No failures were observed upto 4 Amps of current levels. Hence the current was ramped to 5 Amps. Figure 5.2 and Figure 5.3 show the temperature vs. time plot for the narrow and standard pad soldered resistors respectively, at 5 Amps.

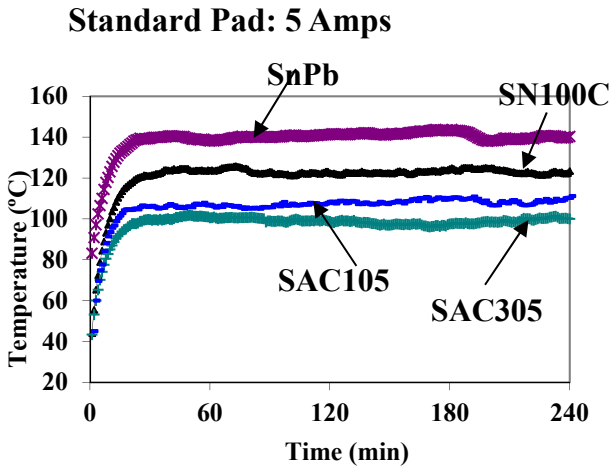

Figure 5.2: Temperature vs. time plot for narrow pad resistors: 5 Amps for 4 hours

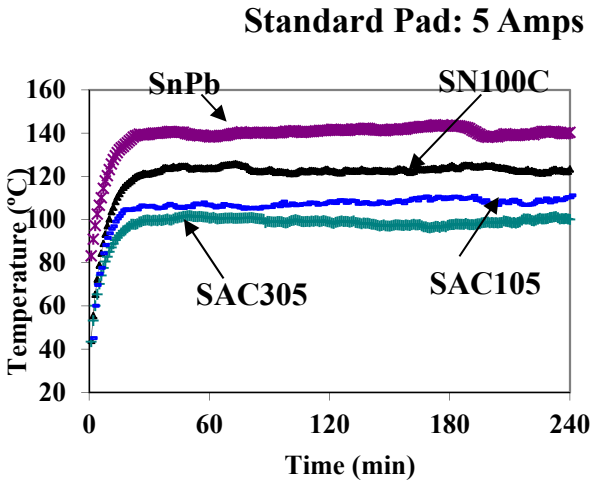

Figure 5.3: Temperature vs. time plot for standard pad resistors: 5 Amps for 4 hours

As seen in Figure 5.2 and Figure 5.3 no failures were observed in test specimens subjected to 5 Amps within the test time of 4 hours. SnPb showed maximum temperature rise followed by SN100C, SAC105 and SAC305. The results indicate that theoretical model underestimates the current carrying capacity of the copper traces. Further testing was conducted at 6, 6.5, 7, and 7.5 Amps on new test specimens to determine the current overstress limits. Table 5.3 shows the current

densities in the three conductive components of the assemblies, copper trace, and narrow and standard pad solder joints. Table 5.4 shows the summary of the findings at 6 Amps. It can be seen that for SN100C solder only narrow pad solder joints fail at the current level of 6 Amps. For SnPb solder both narrow and standard pad resistors fail at 6 Amps. In this case the narrow pad lasts longer than the standard pad. No failures were recorded in SAC solders at this current level.

Table 5.3: Current densities in copper trace and solder joints

	Current density (A/cm^2)		
Current (Amps)	**Cu trace**	**Narrow pad solder joint**	**Standard pad solder joint**
5	$5.62x10^4$	$2.05x10^4$	$4.06x10^3$
6	$6.74x10^4$	$2.46x10^4$	$4.87x10^3$
6.5	$7.31x10^4$	$2.66x10^4$	$5.28x10^3$

Table 5.4: Current overstress experiment results: 6 Amps

Solder type	Pad type	Current (Amps)	Failed (Y/N)	TTF (min)	Max. temp (^oC)
SN100C	***Narrow***	***6***	***Y***	***200***	***183***
	Standard	6	N	-	175
SnPb	***Narrow***	***6***	***Y***	***44***	***233***
	Standard	***6***	***Y***	***38***	***219***
SAC105	Narrow	6	N	-	165
	Standard	6	N	-	145
SAC305	Narrow	6	N	-	114
	Standard	6	N	-	130

Table 5.5: Current overstress experiment results: 6.5 Amps

Solder type	Pad type	Current (Amps)	Failed (Y/N)	TTF (min)	Max. temp (^oC)
SN100C	***Narrow***	***6.5***	***Y***	***56***	***346***
	Standard	***6.5***	***Y***	***20***	***294***
SnPb	***Narrow***	***6.5***	***Y***	***7***	***222***

	Standard	***6.5***	***Y***	***19***	***238***
SAC105	***Narrow***	***6.5***	***Y***	***21***	***256***
	Standard	***6.5***	***N***	***-***	***145***
SAC305	Narrow	6.5	N	-	255
	Standard	6.5	N	-	135

Table 5.6: Current overstress limit in SAC solders

Solder type	Pad type	Current (Amps)	Failed (Y/N)	TTF (min)	Max. temp (^{o}C)
SAC105	***Standard***	***7***	***Y***	***120***	***227***
SAC305	***Narrow***	***7***	***Y***	***240***	***450***
	Standard	7	N	-	190

Table 5.5 shows the results of current stressing at 6.5 Amps. Here, both standard and narrow pad resistors assembled with SnPb and SN100C solders failed. The SAC105 soldered narrow pad specimen failed as well. The SAC105 soldered standard pad resistor and both the SAC305 soldered standard and narrow pad resistors survived. Testing was carried out on new SAC soldered specimens to determine the current carrying limit, SAC soldered samples were exposed to higher currents. The results are summarized in Table 5.6. SAC105 soldered standard and narrow pad resistors, as well as the SAC305 narrow pad resistor failed at 7 Amps. The SAC305 soldered standard resistor failed at the current level of 7.5 Amps after 200 minutes.

4-wire resistance measurements were carried out on SnPb and SAC305 test assemblies to investigate if the resistance was the cause of the different current overstress limits. The measurements were carried out between the trace-pad interface of the anode and cathode sides. Table 5.7 and Table 5.8 shows the resistance

comparison of SnPb and SAC305 with narrow and standard pad resistor configurations respectively.

Table 5.7: Resistance of narrow pad resistor assemblies

Solder	Pad (N/S)	Resistance (mΩ)
SnPb	N	13.61
SnPb	N	13.10
SnPb	N	13.64
SAC305	N	12.23
SAC305	N	14.13
SAC305	N	13.01

Table 5.8: Resistance of standard pad resistor assemblies

Solder	Pad (N/S)	Resistance (mΩ)
SnPb	S	15.13
SnPb	S	15.76
SnPb	S	15.20
SAC305	S	15.07
SAC305	S	15.21
SAC305	S	15.00

It may be seen that the narrow pad assemblies had the lower resistance values than the standard pad assemblies. The current in standard pad resistor has to travel longer distance as compared to that in the narrow pad resistor, since the standard pad is five times wider than the narrow pad. Hence, the standard pad resistor show higher resistance value as compared to the narrow pad resistor. However, no difference in the resistance values was observed among the SnPb and SAC305 assemblies. This suggests that joule heating due to electrical resistance was not the governing factor for the difference in the current carrying capacities of the solders.

5.3 Failure Analysis

Physical analysis was conducted to locate the failure sites and identify the failure mechanisms. Non-destructive testing was carried out on the failed specimens using optical and X-ray inspections. Failure modes observed in the test were Cu dissolution leading to trace breakage, and solder melting. X-ray images revealed more information about the failure site than the optical inspection, therefore the majority of failure analysis section focuses on the X-ray inspection. Figure 5.4-Figure 5.7 shows the result of failure analysis on the select failed narrow pad resistor specimens.

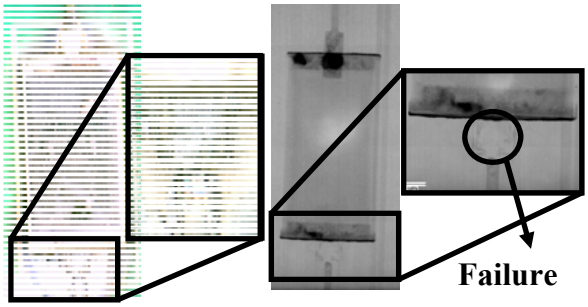

Figure 5.4: SN100C narrow pad resistor at 6.5 Amps

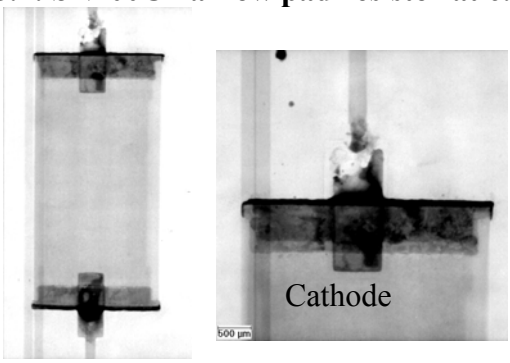

Figure 5.5: SnPb narrow pad resistor at 6.5 Amps

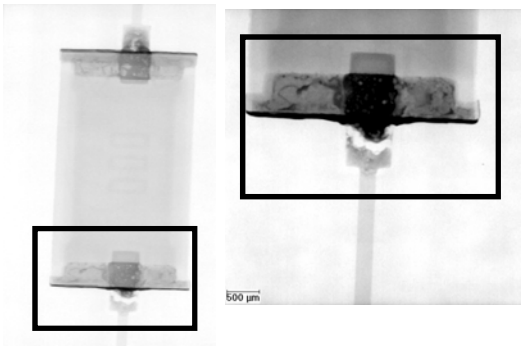

Figure 5.6: SAC105 narrow pad resistor at 7 Amps

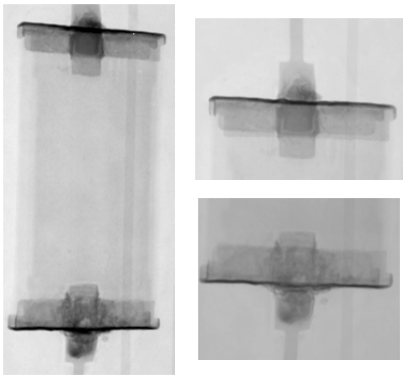

Figure 5.7: SAC305 narrow pad resistor at 7Amps

Figure 4 shows the results of optical and X-ray inspection in failed SN100C narrow pad resistors tested at 6.5 Amps. Failure occurred in the copper pad. It may be observed that a portion of the copper pad between the incoming trace and the 2512 resistor end terminal was absent. Similarly, for SnPb and SAC105 solders, the failure occurred in the Cu pad itself (Figure 5.5-Figure 5.6). However, for the narrow pad resistors assembled with SAC305, the failure occurred by melting of the solder joint (Figure 5.7).

For standard pad resistors, failure occurred at the pad-trace interface (Figure 5.8-Figure 5.11). As seen in the optical image, Figure 8(a), the Cu pad-trace interface is highly stressed. Similar results were observed for SnPb and SAC105 soldered resistors. Again, resistors assembled with SAC305 solders exhibited a different

failure mode. Figure 10 shows the failure in SAC305 standard pad resistor solder joints. The failure occurred by melting of the solder joints.

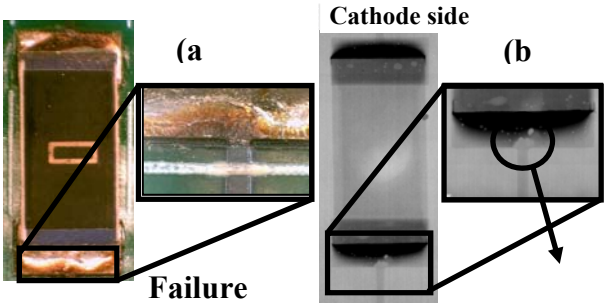

Figure 5.8: SN100C standard pad resistor at 6.5 Amps

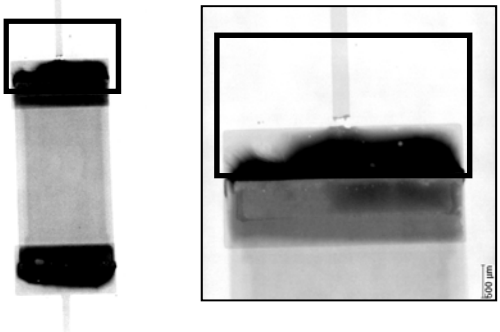

Figure 5.9: SnPb standard pad resistor at 6 Amps

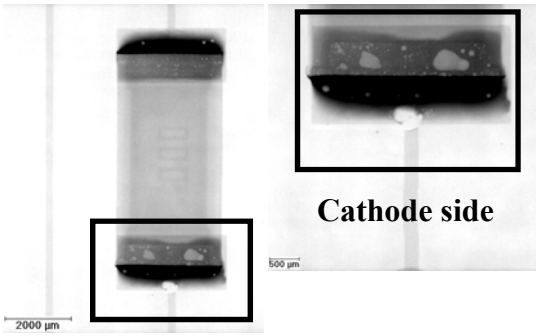

Figure 5.10: SAC105 standard pad resistor at 7 Amps

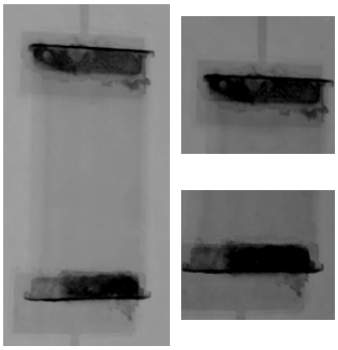

Figure 5.11: SAC305 standard pad resistor at 7.5 Amps

From the observations in Figure 5.8-Figure 5.11, it can be inferred that current overstress limit for the test assemblies is dependent on the solder type. SAC105, SN100C and SnPb assemblies fail by break of trace-pad interface in standard pad assemblies and copper pad in narrow assemblies respectively. For SAC305, the copper traces do not break even at the current levels of 7.5 Amps. Instead the failure occurs by melting of the solder.

Microstructural analysis was carried out to further investigate the failure sites. As seen in Figure 5.12, enhanced diffusion of copper (from the pad) into the solder bulk is observed. The enhanced diffusion is due to very high temperature observed during the test (Table 4-5). Copper diffuses into the solder bulk on both anode and cathode sides to form Cu_6Sn_5 IMCs in the solder bulk (Figure 5.13). This fast dissolution of copper into the solder bulk results in thinning of the copper pad. The thinning of the Cu pad in turn leads to localized joule heating, eventually leading to the melting of the trace. Figure 5.14 shows the copper pad consumption at cathode and anode ends. It can be seen that copper pad is consumed to form the IMCs in the bulk. Copper pad consumption is more severe at the cathode side hence making it the failure site.

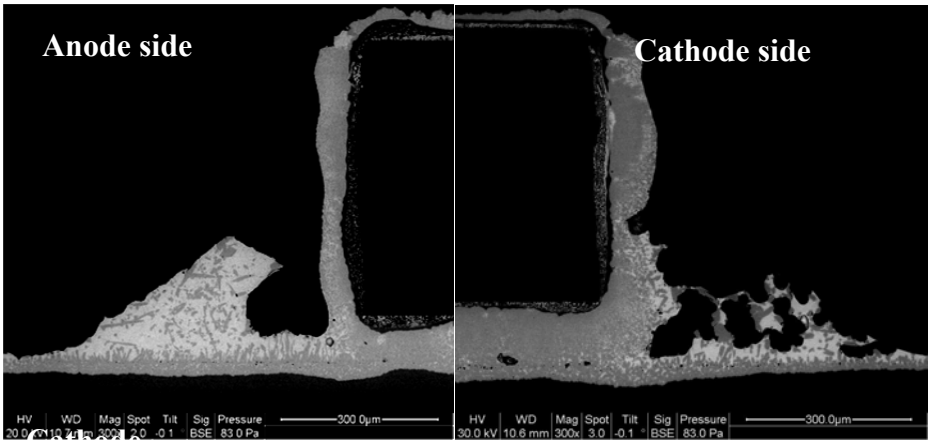

Figure 5.12: SAC305 standard pad resistor at 7.5 Amps

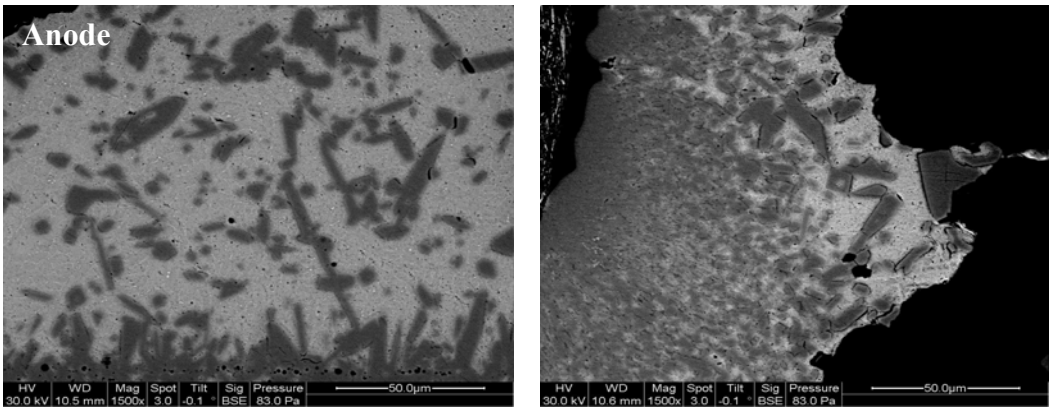

Figure 5.13: Cu_6Sn_5 IMCs in SAC305 solder stressed at 7.5 Amps to failure

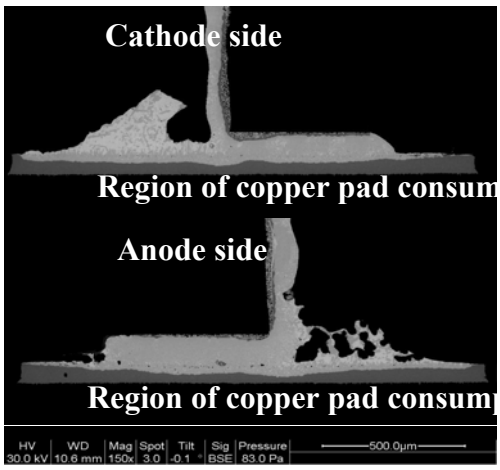

Figure 5.14: Copper pad consumption in SAC305 standard pad solder at 7.5 Amps

Since it was determined in the previous section that resistance of the solder assemblies being similar, it cannot be a factor in determining the current carrying capacity. It is hypothesized that the copper dissolution-assisted trace thinning is dependent on solder type. The diffusion of copper into the bulk solder is a function of the temperature and the solder alloy composition. Temperature being the same, the diffusion is faster for SnPb and SN100C solders as compared to the SAC solders.

5.4 Conclusions

Direct current carrying capacity of SAC105, SAC305, SN100C and SnPb solders was examined using assemblies of 2512 resistors mounted on standard and reduced width (20% of standard pad width) copper pads. The electrical path was formed by via, trace, pad, solder and resistor. Due to their lowest cross-sectional area, traces are considered to be the limiting factor in current carrying capacity of the assemblies. The test assembly was tested in the current levels of 0.5–7.5 Amps to determine the current carrying capacity.

The test results showed that fusing current values of external copper traces given by theory are conservative. When considering termination points, the coefficient and exponents of the formulation have to be adjusted based on the solder material used for interconnection.

It was also found SnPb soldered assembles had the maximum temperature rise and lowest current carrying capacity. Resistor assembled with SAC305 solder showed lowest temperature rise and highest current carrying capacity among all the solders.

Four-wire resistance measurement of the SAC305 and SnPb assemblies showed similar resistance values. It was inferred that the resistance was not the dominant factor in determining the current carrying capacity. It is hypothesized that the copper dissolution-assisted trace thinning is dependent on solder type. The temperature rise due to Joule heating being the same (due to same current level), copper dissolution is faster for SnPb and SN100C solders as compared to the SAC solders.

Failure analysis revealed two failure modes, pad–trace breakage due to copper dissolution, and the solder melting. Pad geometry was also found to influence current carrying capacity. The current carrying capacity of solder assembled with standard copper pads is higher than that of narrow copper pads ($1/5^{th}$ of the width of standard copper pads). Due to lower cross-sectional area, narrow pad specimens experienced higher current densities, and hence high joule heating, leading to faster dissolution of copper in the solder and hence faster failure.

5.5 References

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6 Chapter 6: Impact of Moderate Current Densities on Thermal Cycling Reliability of SAC305, SAC105, SN100C and SnPb Solder Interconnections

This chapter presents the effect of moderate current densities ($1.63x10^3 A/cm^2$) on the thermal cycling reliability of Sn96.5Ag3.0Cu0.5, Sn98.5Ag1.0Cu0.5, Sn97.3Cu0.7+Ni and Sn63Pb solder interconnections. A set of surface mount resistors soldered onto printed circuit board are subjected to a constant direct current of 2 Amperes, at the same time being thermally cycled in the temperature range of -55°C to 125°C. In order to separate the Joule heating effect of electrical current, a separate set of non-powered specimens are heated by an external heater to obtain same temperature rise as the powered specimens, at the same time being cycled in the same thermal chamber. It was found that the moderate current densities of $10^3 A/cm^2$ do not degrade the thermal cycling reliability of solders. Hence, the current densities of 10^3 A/cm^2 need not be considered in the design of reliability tests for solder interconnects. Also, SAC305 solder was found to be the most reliable under thermal cycling, for both powered and non-powered sets, while SN100C the least reliable.

6.1 Introduction

Solder interconnects provide a critical function in electronic products since they are used to form mechanical and electrical connections between electronic devices. As an electrical connector, solder is required to carry electrical current during its operational life. The increasing miniaturization of the electronics has led to high current densities in the solder interconnects. The reliability studies on the effect

of electrical current have hence focused on high temperature (>100^{o}C) and high current densities (of the order of 10^4A/cm^2) in small solder joints (flip chip) [1-11], where electromigration and thermomigration assisted failures can occur.

However, the impact of current densities lower than 10^4 A/cm^2 on solder joint reliability has received less consideration. Studies have been conducted on the specimens with relatively larger sizes, such as resistors, in which only moderate current densities could be reached (10^2–10^3A/cm^2). Researchers [12-14] have reported that at these current densities, no electromigration effect was observed for up to 600 hours of current stressing, even at a temperature of 125^{o}C. However, at these current densities enhanced joule heating may occur due to the cumulative effect of joule heating in solders and the adjacent conductive traces. High Joule heating results in high temperature of solder which might cause accelerated aging of the solders, which includes phase coarsening and intermetallic growth. The phase coarsening and intermetallic growth adversely affects the solder joint reliability. Wu *et al.* [14] studied the effect of current densities of the order of 10^2 A/cm^2 at 125^{o}C on the reliability of ball grid array (BGA) solder joints assembled with Sn63Pb (SnPb) and Sn96.5Ag3.0Cu0.5 (SAC305) solders. They reported that current density of 10^2 A/cm^2 caused massive joule heating causing the local temperatures of the BGA solder joints to rise considerably. While a significant electromigration effect was not observed, the shear strength of the solder joints was found to degrade. The shear strength degradation was attributed to microstructural coarsening and an increase in the interfacial intermetallic compound (IMC) thickness at the solder-pad interface. The effect of moderate current densities on the thermal cycling reliability of solders

has not been investigated. The microstructural changes in the solder joints under current stressing might also influence the thermal fatigue reliability of the solder joints. The present work examines the effect of moderate current densities on the thermal cycling reliability of solders.

6.2 Experiment

In this study, 2512 chip resistors soldered onto copper pads of a FR4 printed wiring board (PWB) were used. Sn96.5Ag3.0Cu0.5 (SAC305), Sn98.5Ag1.0Cu0.5 (SAC105), Sn97.3Cu0.7+Ni (SN100C) and Sn63Pb (SnPb) solders were studied. The cross-sectional areas of trace and solder joints are 8.9×10^{-5} and 1.23×10^{-3} A/cm^2 respectively. Since the copper trace has lower cross-sectional area than the solder joint, it experiences a higher current density than the solder joints under electrical loading. Table 6.1 shows the resistivity of the solder and trace materials. It may be seen that SnPb showed higher resistivity than both SAC and SN100C solders.

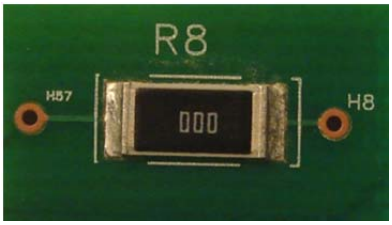


Figure 6.1: Test specimens

Table 6.1: Resistivity of solder and trace materials [15, 16]

Material	Resistivity (Ωμcm)
Cu	1.72

63Sn37Pb	14.5
SAC305	13.2
SN100C	13.0
SAC105	13.3
Sn	12.4
Ag	1.63

6.2.1 Approach

In order to examine the effect of moderate current densities on the thermal cycling reliability of solder interconnects, test specimens were subjected to a constant current while simultaneously being subjected to a temperature cycle loading condition. The current level was selected based on two considerations: (i) temperature rise across all the solder types should be approximately the same, and (ii) current density and temperature rise should not be very high as electromigration and thermomigration might start playing a role in the solder reliability. A set of soldered resistor specimens were subjected to the chosen current level, at the same time being thermally cycled. A separate set of non-powered specimens was externally heated to achieve same temperature rise as the powered specimens, at the same time being thermally cycled in the same thermal chamber.

Prior to the temperature cycle test, a separate set of test specimens were subjected to various current levels to determine temperature rises in the specimens due to Joule heating. Figure 6.2 shows the direction of electron flow in the

soldered resistors. The current enters the copper (Cu) pad region from the Cu trace at cathode side and conducts from the specimen top towards the anode side.

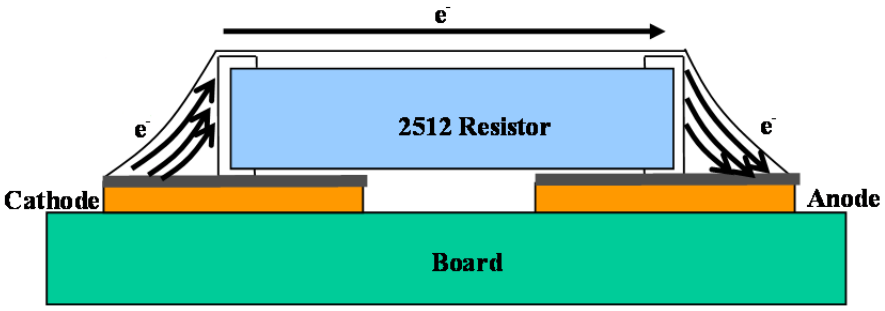


Figure 6.2: Direction of electron flow

Table 6.2: Temperature rise in solders vs. current

Current (Amps)	SnPb (ΔT:ºC)	SAC305 (ΔT:ºC)	SAC105 (ΔT:ºC)	SN100C (ΔT:ºC)
0.5	<5	<5	<5	<5
1	<5	<5	<5	<5
2	10	7	8	10
3	35	19	17	27
4	60	37	45	49

The test specimens were subjected to the electrical current in the range of 0.5–4 Amps. Table 6.2 shows the temperature rise in the solder joints vs. the current level. In this table, the data shown is the average of 4 readings per current level per solder type for 4 hours. SnPb exhibited the highest temperature rise among all solders for the same current level followed by SN100C and SAC105. SAC305 showed the least temperature rise. As seen in Table 6.2, current levels at and below 1 Amp were below 5^{o}C. At current levels above 3 Amps, the temperature rises were higher than 15^{o}C and the variation in temperature between the various solders specimens exceed 5^{o}C. At 2

Amps, all the tested solders showed a similar temperature rise of ~10^{o}C. Therefore, 2 Amps was chosen as the current level for the tests. The current density at 2 Amps was obtained by dividing by the cross-sectional area of the solder joint, and was obtained to be 1.63x10^{3} A/cm^{2}.

6.2.2 Effect of Current Stressing on the Solder Microstructure and Interfacial IMC Growth

Before determining the effect of the chosen current density on the thermal cycling reliability of the solder, the effect on solder microstructure was documented. For this effort, test specimens were subjected to current stressing at 2 Amps for 600 hours inside a thermal chamber maintained at room temperature condition (25^{o}C). After current stressing, the solder joints of the test specimens were prepared for examination under a scanning electron microscope (SEM). Figure 6.3 through Figure 6.6 provide comparisons between of electrically current stressed and isothermally aged SAC305, SAC105, SN100C and SnPb solder interconnects, respectively. The isothermal aging condition was 24 hours at 100^{o}C. Images of the current stressed solder interconnects include sections from both the anode and cathode side of the resistor. These images are oriented so that the solder pad on the board is parallel the bottom edge of each image.

From images in Figure 6.3, it can be seen that the solder microstructure for both powered and non-powered sets in SAC305 was similar. For SAC105 solders, the images in Figure 6.4 show no difference in the microstructure between the 100^{o}C/24 hours preconditioned and current-stressed specimens. Similarly for SnPb and SN100C solder depicted in Figure 6.5 and Figure 6.6 respectively, no particular

orientation or size variation of the Pb-rich phases' regions is observed between the isothermally aged and current stressed solder sections.

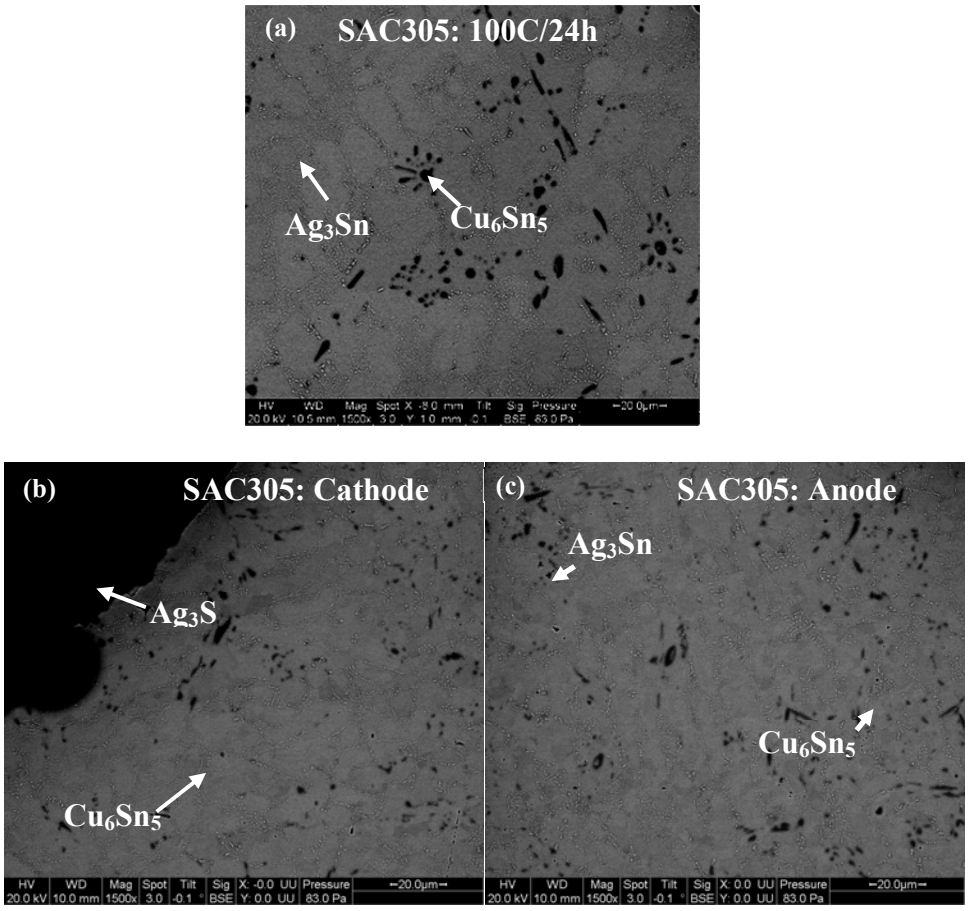


Figure 6.3: SAC305 Solder (a) 100C/24 hours and stressed at 2 Amps for 600 hours: (b) Anode Side and (c) Cathode Side

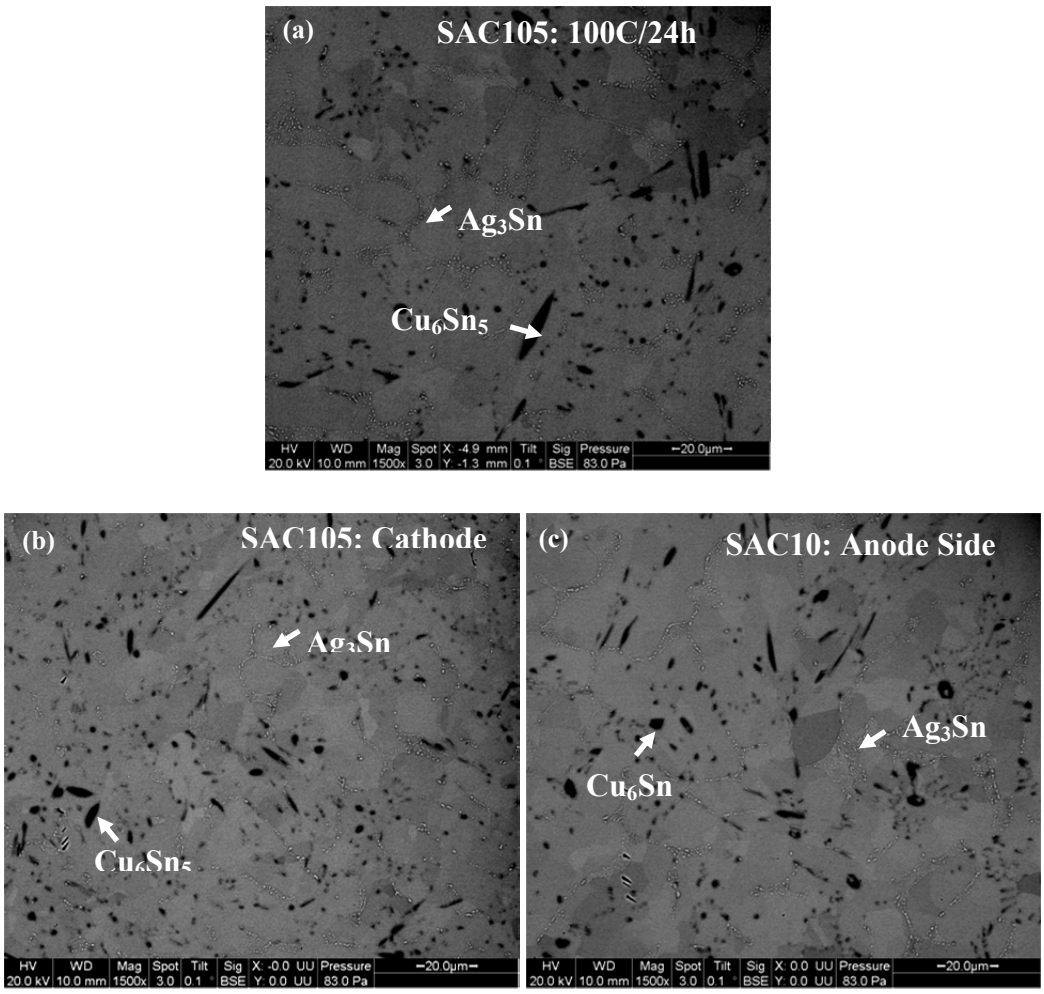
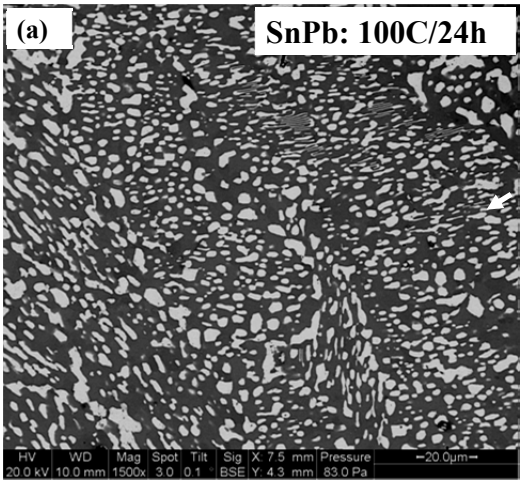


Figure 6.4: SAC105 Solder (a) 100C/24 hours, and stressed at 2 Amps for 600 hours: (b) Anode Side and (c) Cathode Side



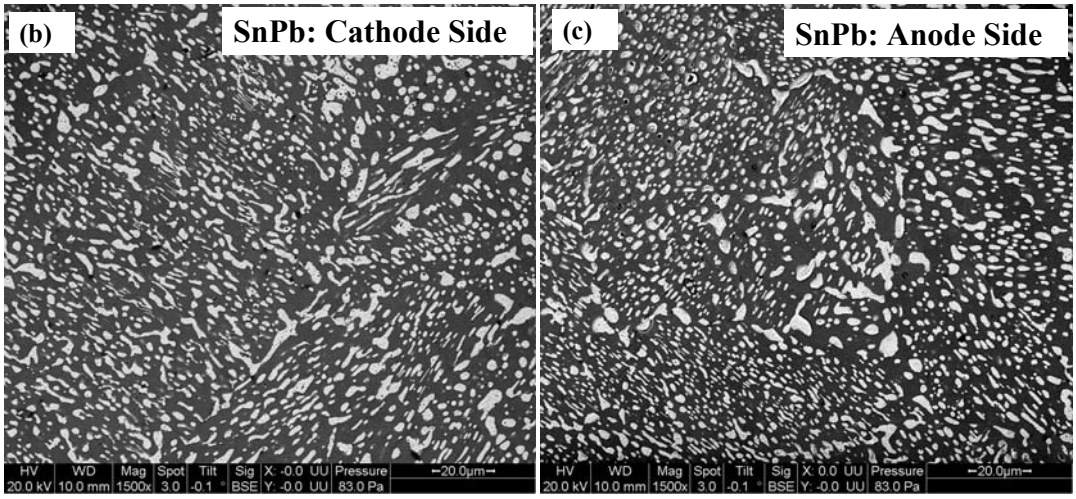
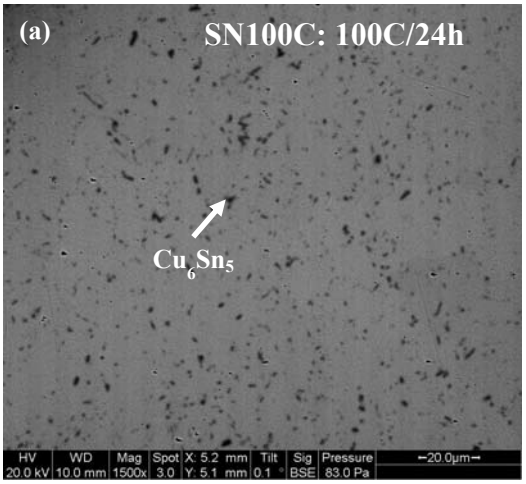


Figure 6.5: SnPb Microstructure (a) 100ºC/24h, and stressed at 2 Amps for 600 hours (b) Cathode Side and (c) Anode Side: Pb-rich region is shown by the white areas and the Sn-rich region is shown by the gray areas.



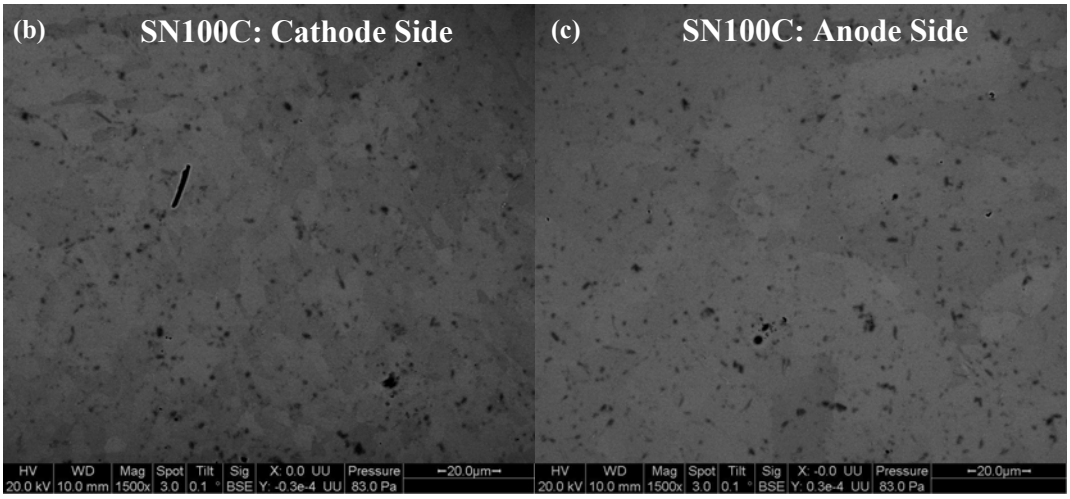


Figure 6.6: SN100C Microstructure (a) 100ºC/24h, and stressed at 2 Amps for 600 hours (b) Cathode Side and (c) Anode Side

In addition to bulk microstructure, the interfacial IMCs were examined. The thickness of the isothermally aged and current stress samples were measured using an area method, wherein the IMC area was divided by the IMC length to obtain IMC thickness. As seen in Figure 6.7, comparison of IMC thickness in isothermally aged and current stressed specimens shows that there is no statistical difference between the two sets. However, the average interfacial IMC growth increases upon current stressing at 2 Amps at room temperature.

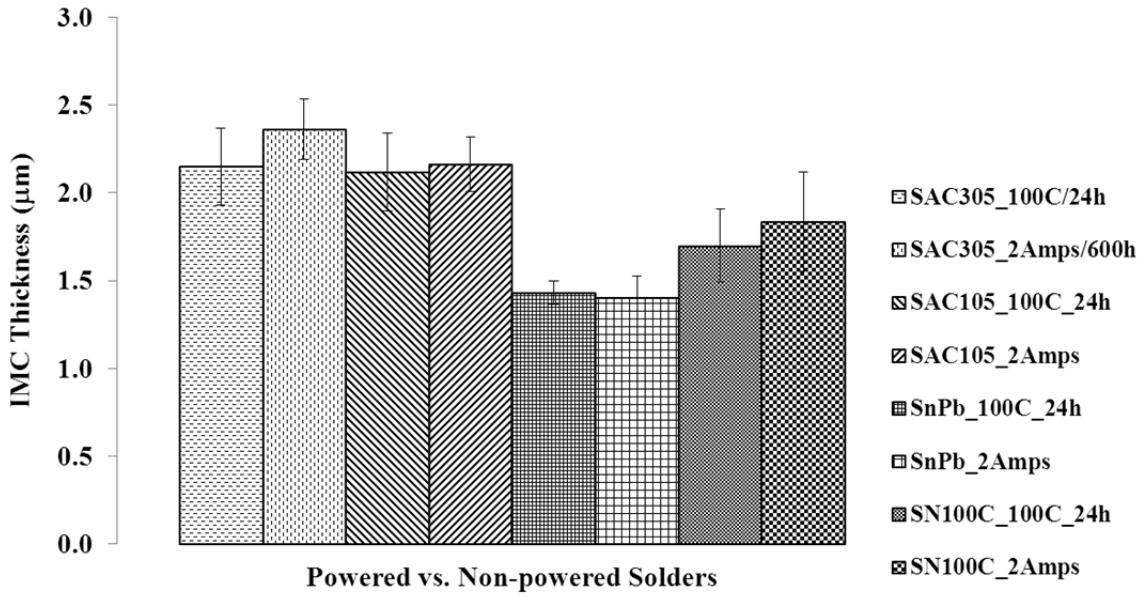


Figure 6.7: Interfacial IMC thickness of current stressed specimens

6.3 Thermal Cycling on Powered and Non-powered Soldered Resistors

Thermal cycling tests were conducted on both powered and non-powered (heated externally) specimen sets. The effect of in-situ current stressing and hence joule heating was assessed by comparing with the specimen set heated externally using kapton heaters for the same temperature rise as the powered sets. Both powered and non-powered sets consisted of ten specimens per solder type. Figure 6.8 shows the schematic of the experimental set up. The powered sets were powered by four-channel power supply wherein each channel supplied power to specimens of one solder type. Voltage measurements of the powered resistor sets were made using 34980A datalogger. For the non-powered sets, resistance measurements were made using 34980A. K-type thermocouples were placed on top of the resistor components to monitor the temperature during testing. Failure

analysis was performed by means of optical inspection, cross-sectioning and scanning electron microscopy (SEM) to identify the failure sites.

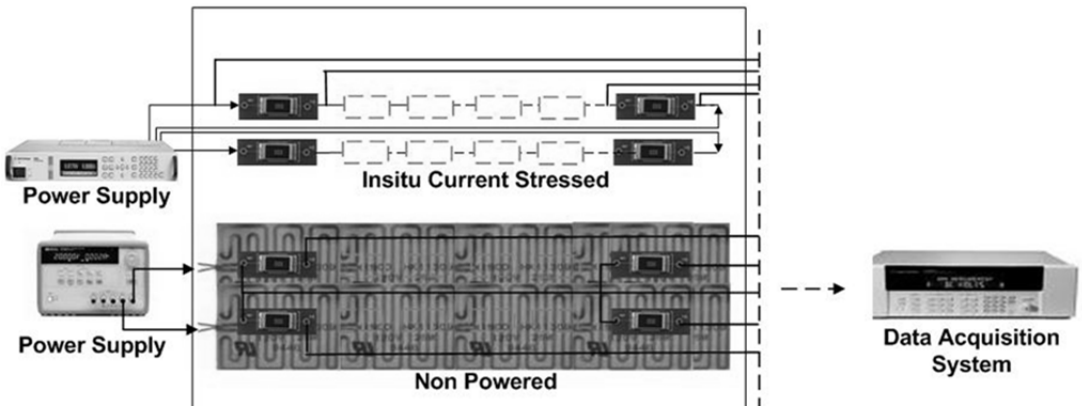


Figure 6.8: Experimental set up

For current stressed components, it is not possible to make a direct measurement of resistance during the test. Hence DC voltage measurement is made in current stressed specimens. Since the current level is known, resistance is obtained by R=V/I. 34980A measures voltage with 6 1⁄2 digits of resolution with 0.004% of accuracy in DC voltage measurements. Since the resistor components are near zero resistors, an accurate measurement of resistance is needed. Hence, for non-powered specimens, 4-wire resistance measurement is adopted to record accurate resistance values, since the 4-wire measurement eliminates the resistance of the wires. Figure 6.9 shows the 4-wire resistance measurement principle.

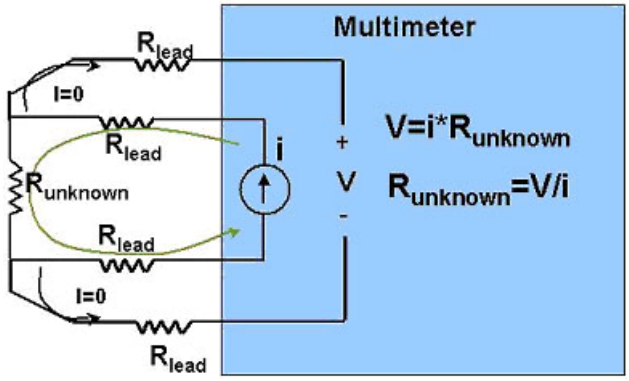


Figure 6.9: Four-wire resistance measurement

Figure 6.10 shows the typical failure signature of powered resistor assemblies soldered with SAC105 solder. The resistance stays constant, for more than 1320 cycles, and increases sharply very close to the failure point. The first spike marking a 50% increase in resistance from the base value is taken as the failure point. The base value of resistance is average resistance value of each test specimen for the first 3 days of test duration.

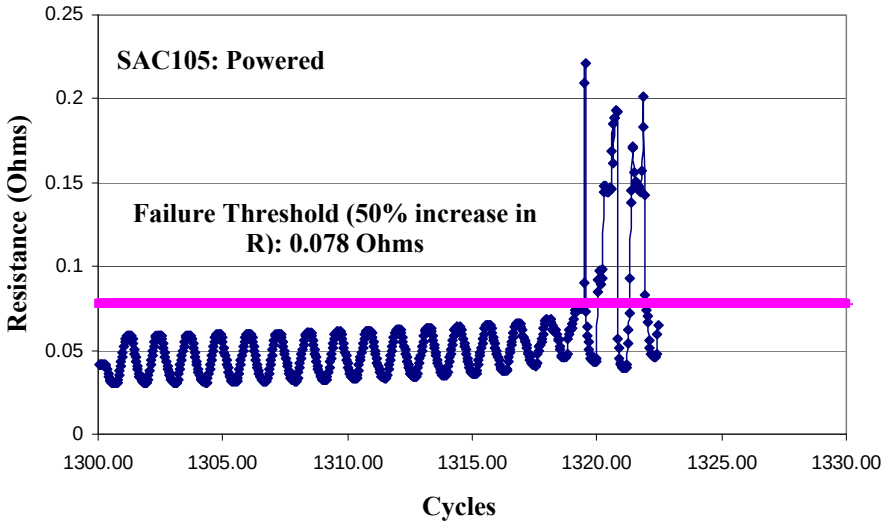


Figure 6.10: Failure signature

6.4 Thermal Cycling Test Results

The recorded cycle to failure data is analyzed using Weibull++ software version 7 [17]. For consistency the data is fit to a two parameter Weibull distribution and the probability of failure versus temperature cycles for the tested solders are plotted in Figure 6.11–Figure 6.15. In some cases, test specimens failed within the first day or two of tests. These specimen failures were attributed to improper wiring and were not considered in the data collection. Figure 6.11–Figure 6.13 show the comparison of failure times of powered and non-powered specimens of SN100C, SAC105 and SnPb solders. At the time of stopping the tests, both powered and non-powered SAC305 solder specimens had 5 survivors each. As seen in Figure 6.11, the comparison of powered and non-powered SN100C soldered resistor assemblies shows that the two sets have similar first failure times. As the test progresses, the reliability of powered sets improves and the separation between the powered and non-powered sets. Powered and non-powered SAC105 soldered resistors also showed similar first failure times (Figure 6.11**Error! Reference source not found.**). However, as the test progresses the reliability of the powered sets shows an improvement. The improvement in reliability is more marked for SAC105 soldered assemblies as compared to the SN100C assemblies. For the SnPb soldered assemblies, the current stressed test specimens show a decrease in cycles to failure compared to the non-current stressed specimens (Figure 6.13).

Reliability comparison was also made across the solders for non-powered sets. It can be seen in Figure 6.14 that SAC305 is the most reliable among the solders

followed by SnPb, SAC105 and SN100C solders. It should be noted that since the tests were time terminated after 5000 cycles, half of the SAC305 assemblies (5) were not failed, for both powered and non-powered sets. A similar trend is observed for the powered sets (Figure 6.15) wherein SAC305 is the most reliable and SN100C the least reliable. However since SAC105 shows improvement in solder reliability as a result of current stressing, the separation between the times to failure distribution narrows down.

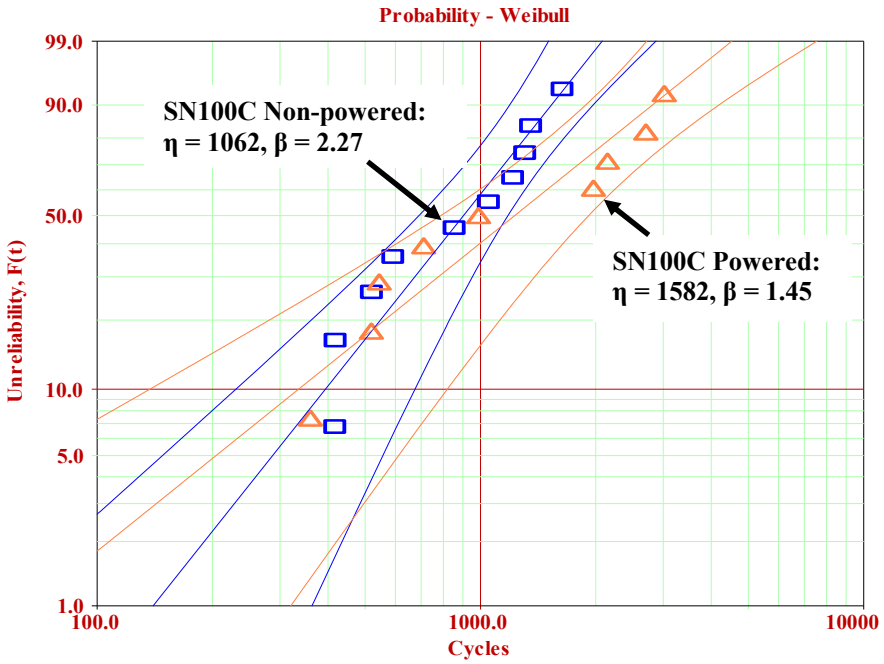


Figure 6.11: Reliability of powered and non-powered SN100C soldered resistors

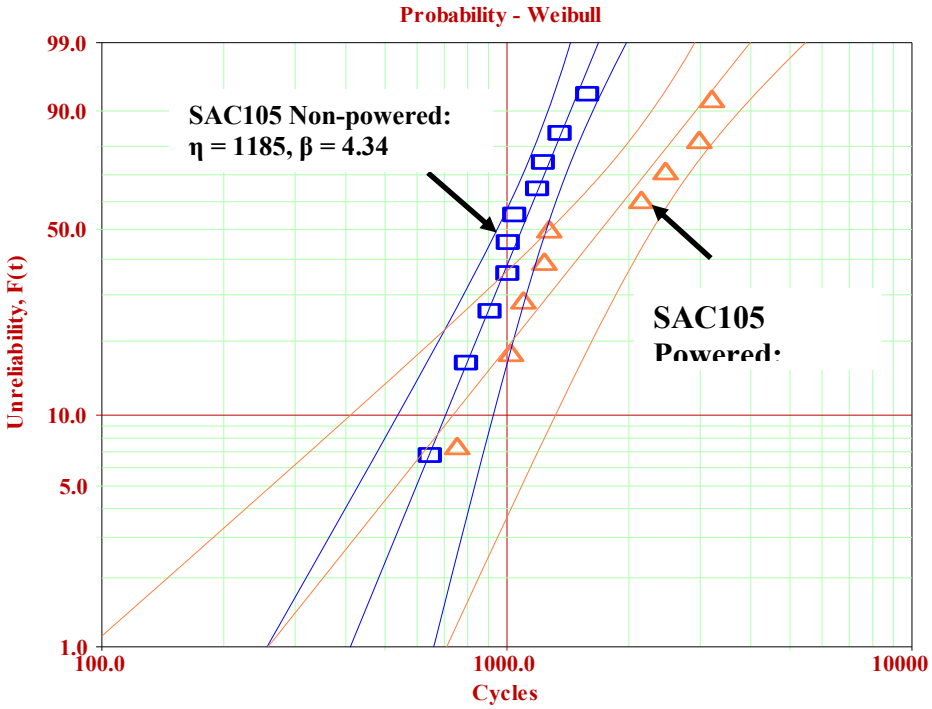


Figure 6.12: Reliability of powered and non-powered SAC105 soldered resistors

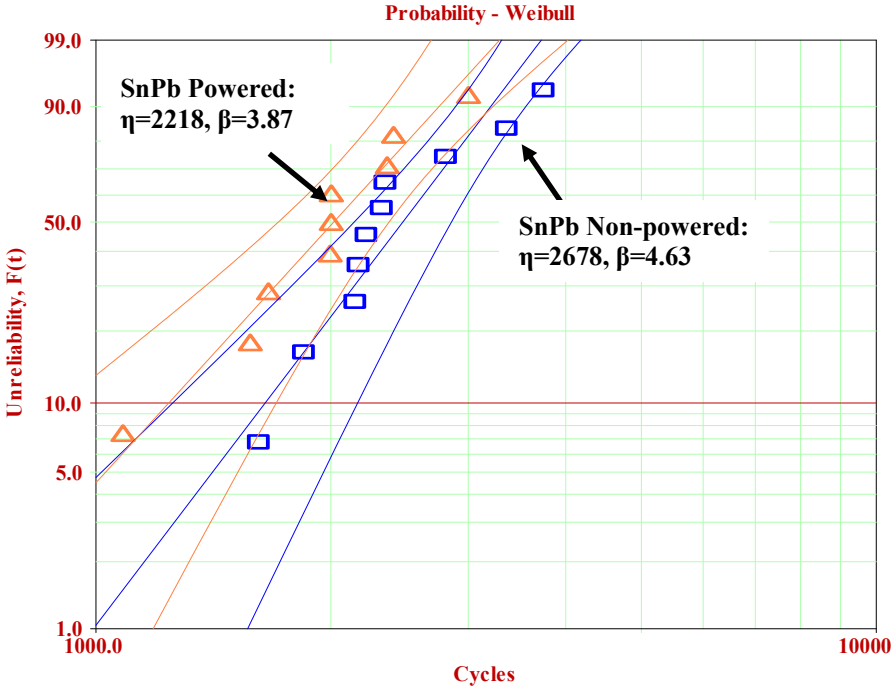


Figure 6.13: Reliability of powered and non-powered SnPb soldered resistors

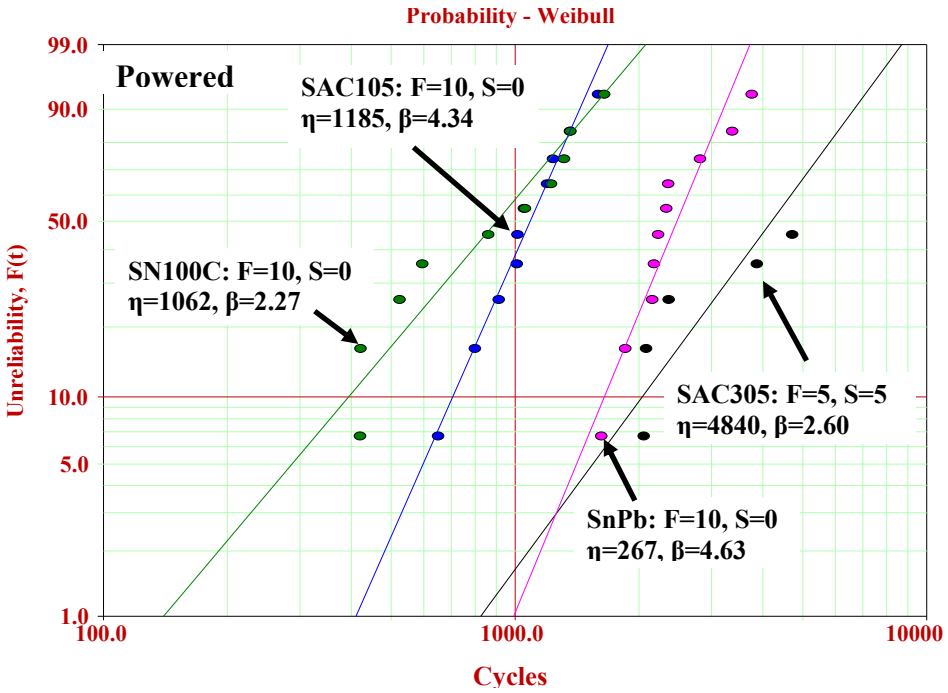


Figure 6.14: Solder reliability in non-powered resistor specimens

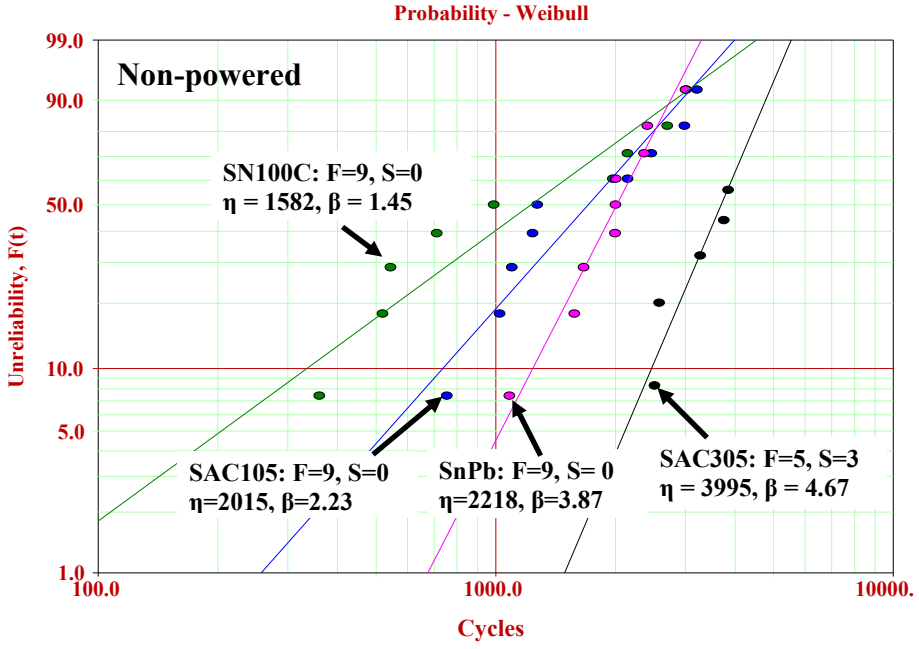


Figure 6.15: Comparison of solder reliability in powered resistor specimens

The failure analysis of the test specimens was carried out to investigate the failure site. It was found that both for powerd and non-powered sets, thermal fatigue failure occurred by crack initiation and propagation under the resistor component and across the solder fillet, as seen in Figure 6.16.

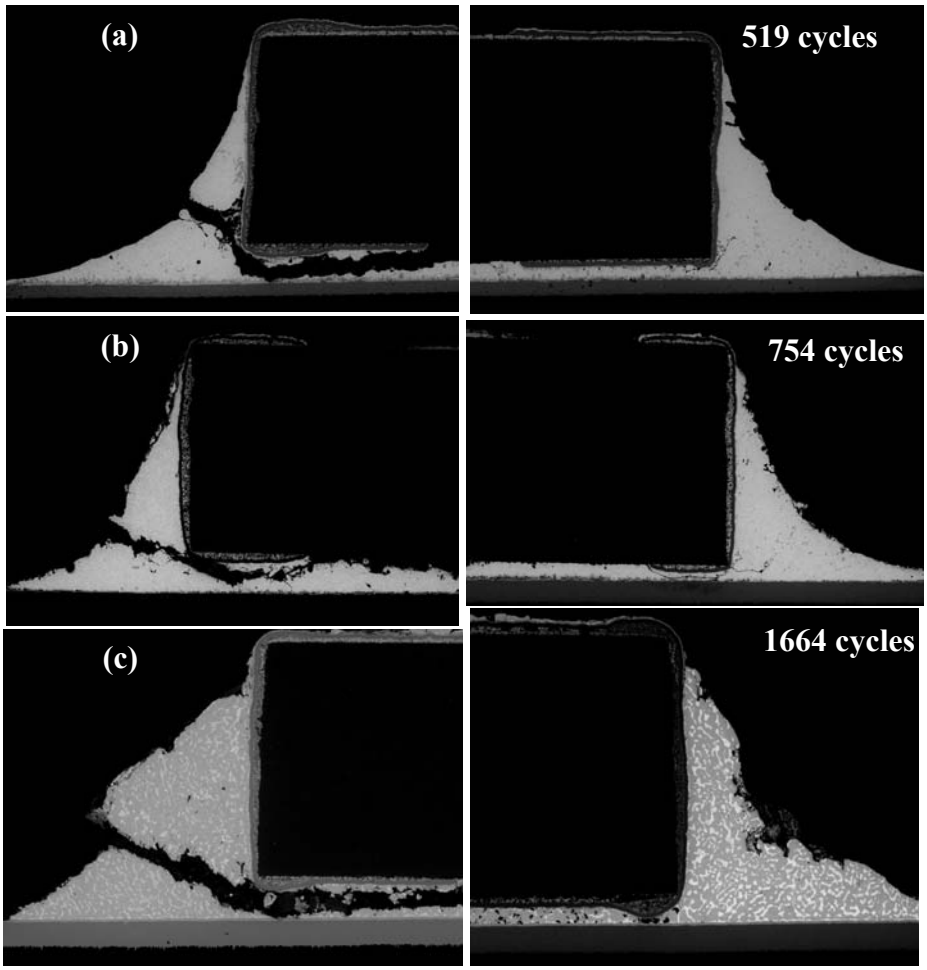


Figure 6.16: Failure Analysis of powered (a) SN100C, (b) SAC105, (c) SnPb specimens

6.5 Summary and Conclusions

This chapter assesses the effect of moderate current densities (1.63×10^3 A/cm^2) on the thermal cycling reliability of SAC305, SAC105, SN100C and SnPb

solder interconnections. Examination of preconditioned and current stressed specimens showed similar microstructures in all tested solders. However, the comparison of average interfacial IMC thickness suggests an increase in the interfacial IMC thickness due to current stressing. Thermal cycling tests conducted on the powered and non-powered solder interconnects show that the current density of 10^3 A/cm^2 does not degrade the thermal cycling reliability of SN100C, SAC105 and SnPb solders. For SAC305 solder, the number of failures was insufficient to draw conclusions on the impact of current stressing. A comparison of thermal cycling reliability across the tested solders shows that SAC305 is the most reliable among the solders followed by SnPb, SAC105 and SN100C solders. From this work, electrical equipment using SAC105, SN100C or SAC305 solder interconnects under moderate current densities ($<1.63 \times 10^3$ A/cm^2) are expected to have comparable reliability with non-powered solder interconnects. Hence, these current densities need not be considered in the design of reliability tests for solder interconnects.

6.6 References

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7 Contributions

Interfacial and Bulk IMC Growth Kinetics

- Developed a methodology of assessing the aging of solder joints based on the size and distribution of bulk phases.
  - First study to report the kinetics of bulk phases in solders and relate to the aging of solders.
  - The aging model can be further related to the solder reliability and mechanical constitutive properties of solders.
- Provided the growth kinetics of the interfacial Cu_6Sn_5 and Cu_3Sn intermetallic phases
  - Determined that aging at 150^{o}C to represent the use life temperatures of 50-100^{o}C is not representative of the solder joint microstructural state due to a transition in the IMC growth kinetics.
  - Determined that the growth of Cu_3Sn phase in SN100C is suppressed due to the presence of nickel, making it a better choice for high temperature (≥150^{o}C) shock applications than SAC105, SAC305 and SnPb solders.

Thermal Cycling Reliability

- Determined that the isothermal aging effect on thermal cycling reliability of the SAC solders is non-monotonic due to the competing effects of the state of solder-pad interface, and bulk solder. On one hand the solder-pad interface reduces the solder ductility, the increase

in uniformity of IMC distribution increases the thermal fatigue strength of the solders.

- Long-term isothermal aging improves the thermal fatigue resistance of SAC105 due to the increase in uniformity of Ag_3Sn distribution.
- SAC305 is less-sensitive to isothermal aging than SAC105 solder. Due to higher cycles to failure (more than twice of SAC105), the microstructural changes due to thermal cycling aging dominate over isothermal aging.
- Isothermal aging is not recommended before conducting the thermal cycling tests on SAC105, SAC305, SN100C and SnPb solders
- The current densities below the electromigration range ($<10^4$ A/cm^2) do not cause changes in the bulk and interfacial IMCs. Hence this current level does not influence the thermal cycling reliability of the select solders and can be ignored in the design of solder joint reliability tests.

8 Appendix

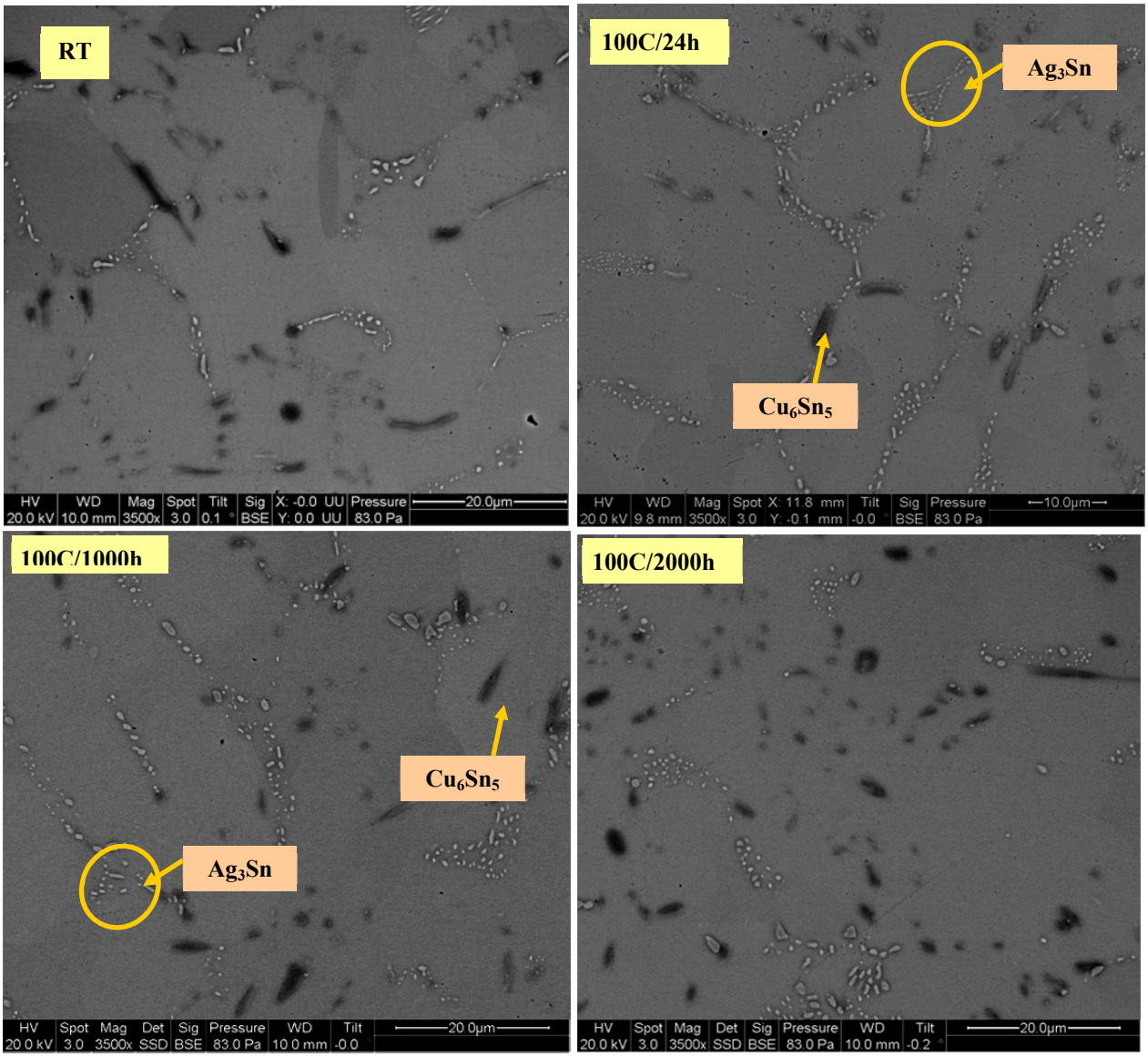


Figure 8.1: Evolution of bulk microstructure of SAC solder aged at 100°C

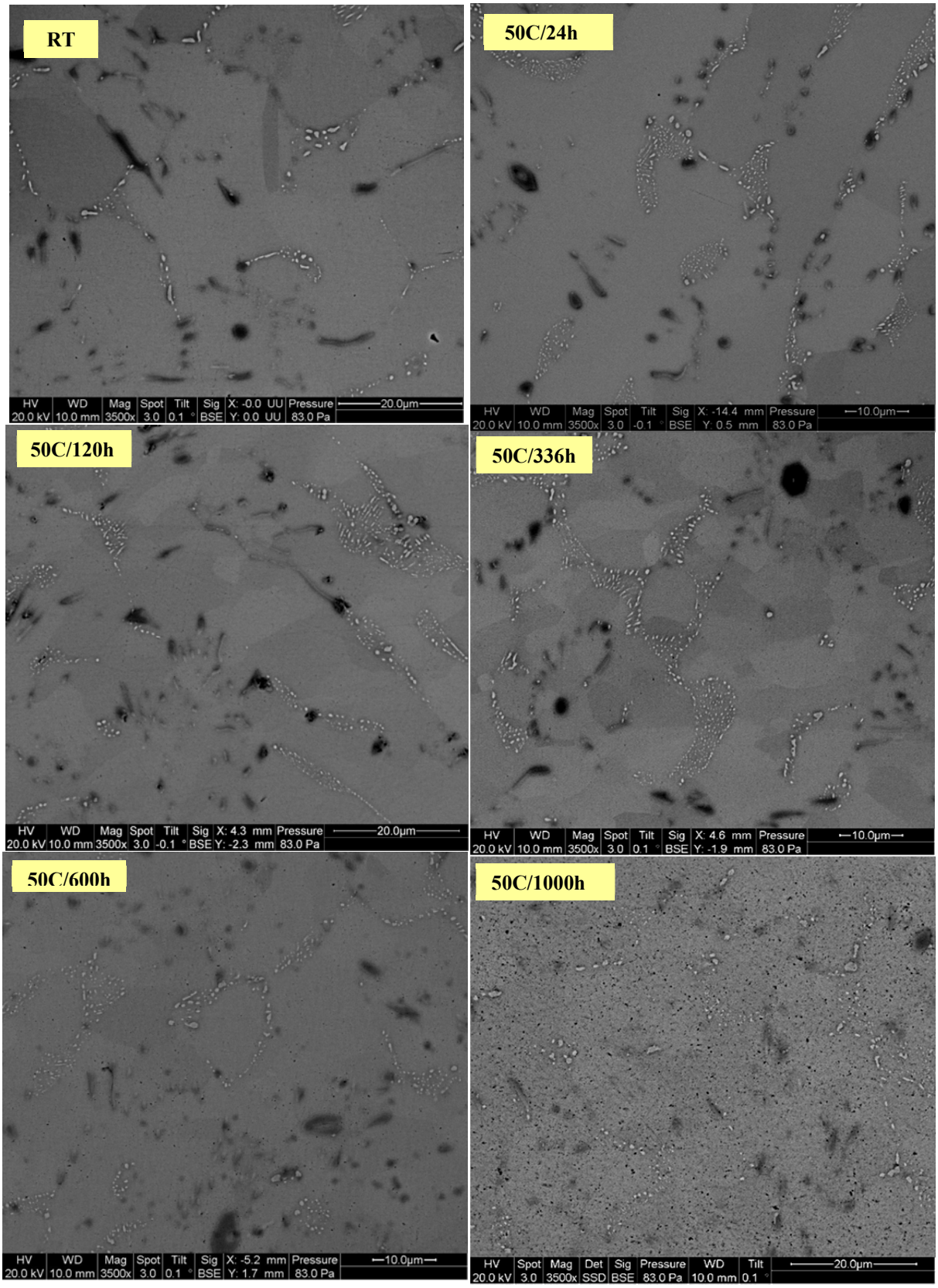


Figure 8.2: Evolution of bulk microstructure of SAC solder aged at 50°C

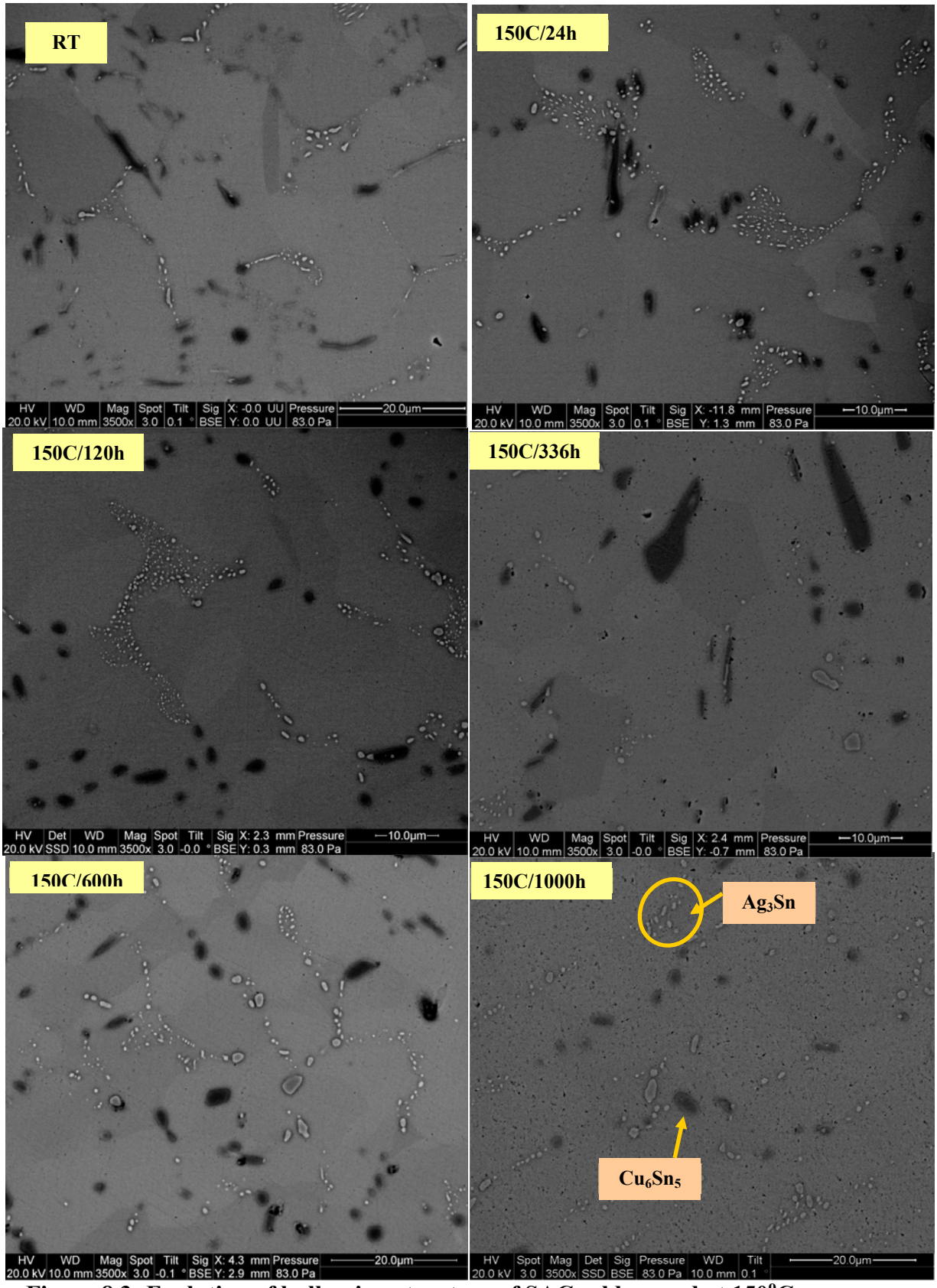


Figure 8.3: Evolution of bulk microstructure of SAC solder aged at 150°C

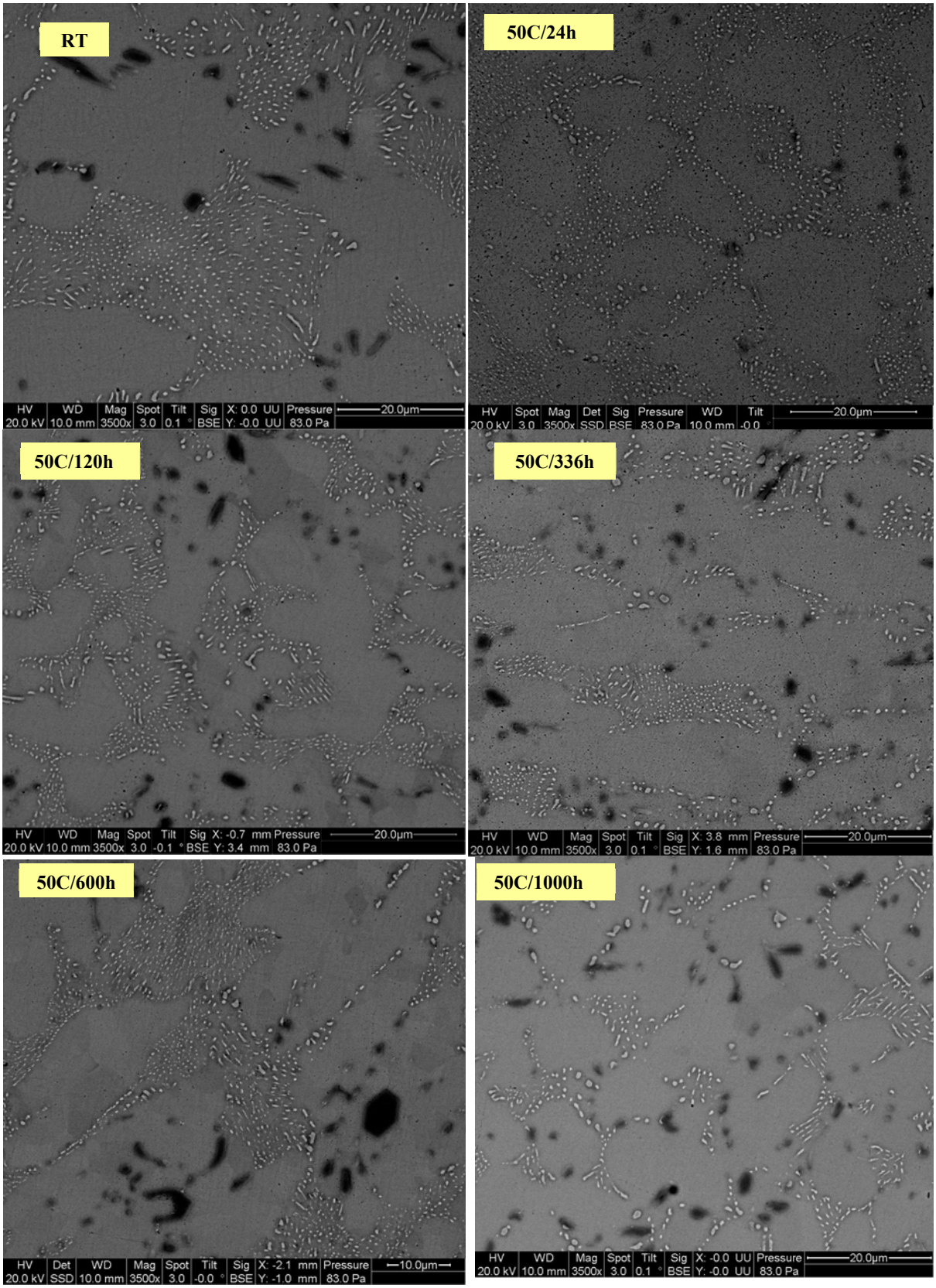


Figure 8.4: Evolution of bulk microstructure of SAC305 solder aged at 50^{o}C

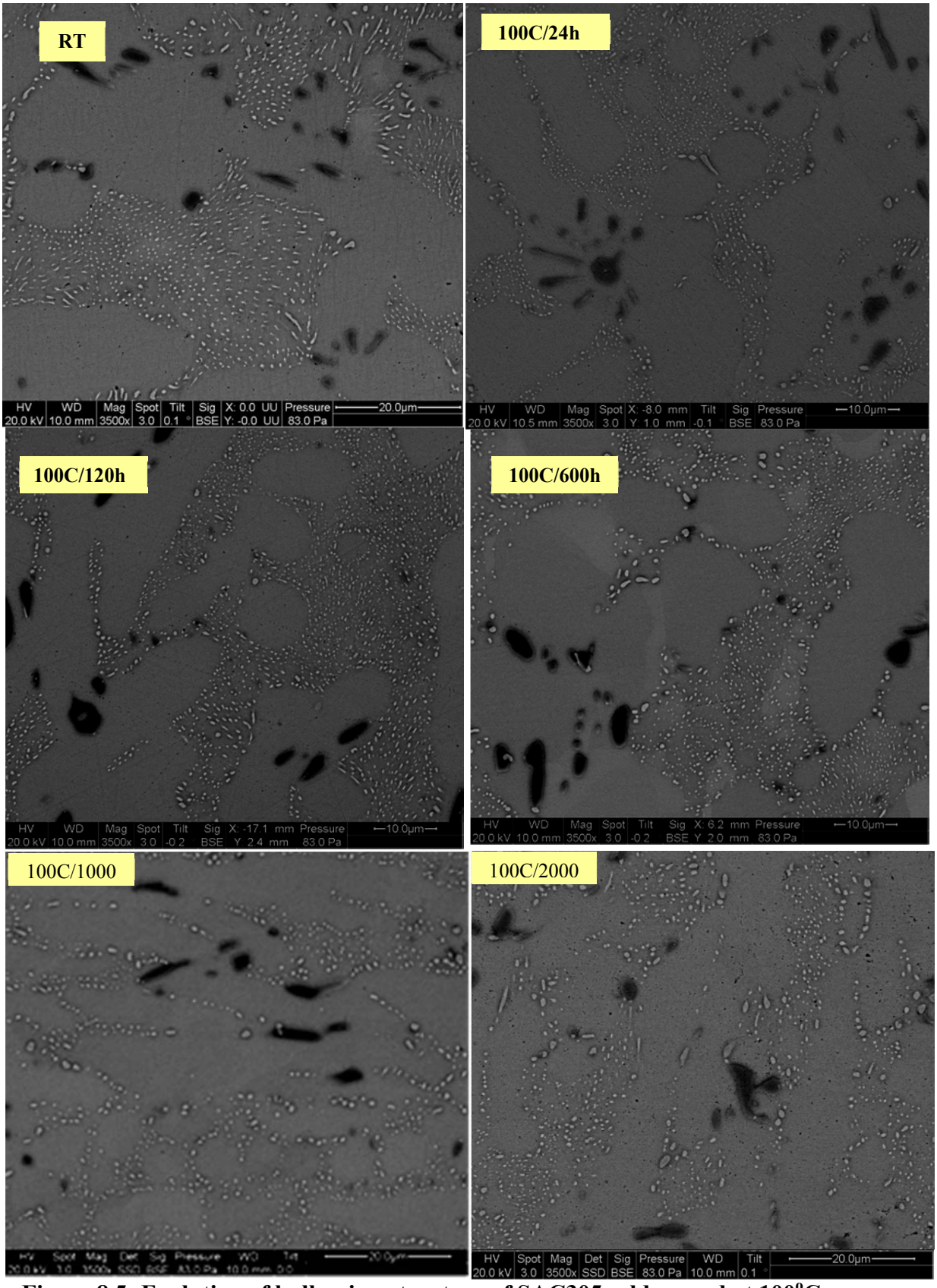


Figure 8.5: Evolution of bulk microstructure of SAC305 solder aged at 100°C

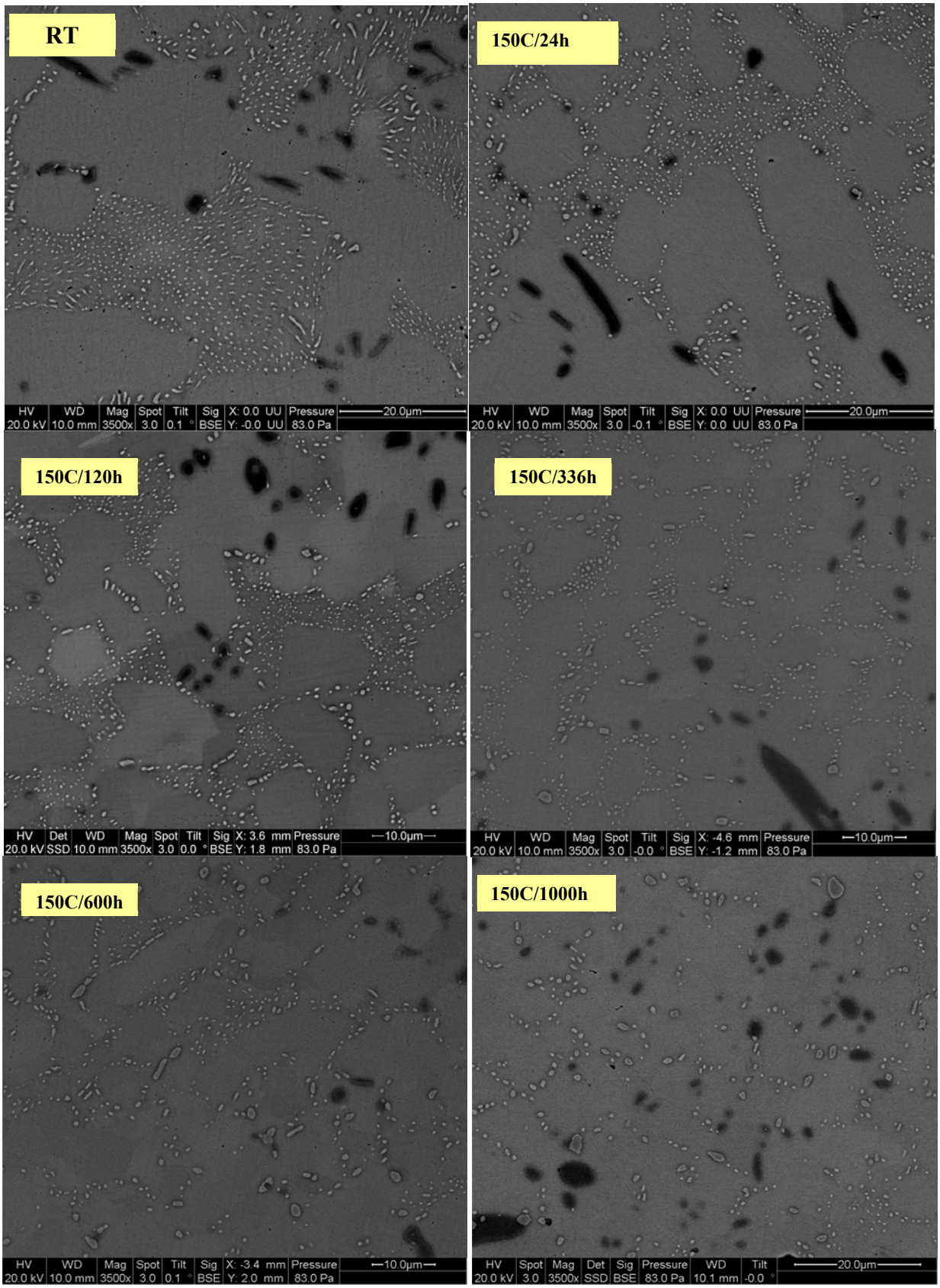


Figure 8.6: Evolution of bulk microstructure of SAC305 solder aged at 150^{o}C

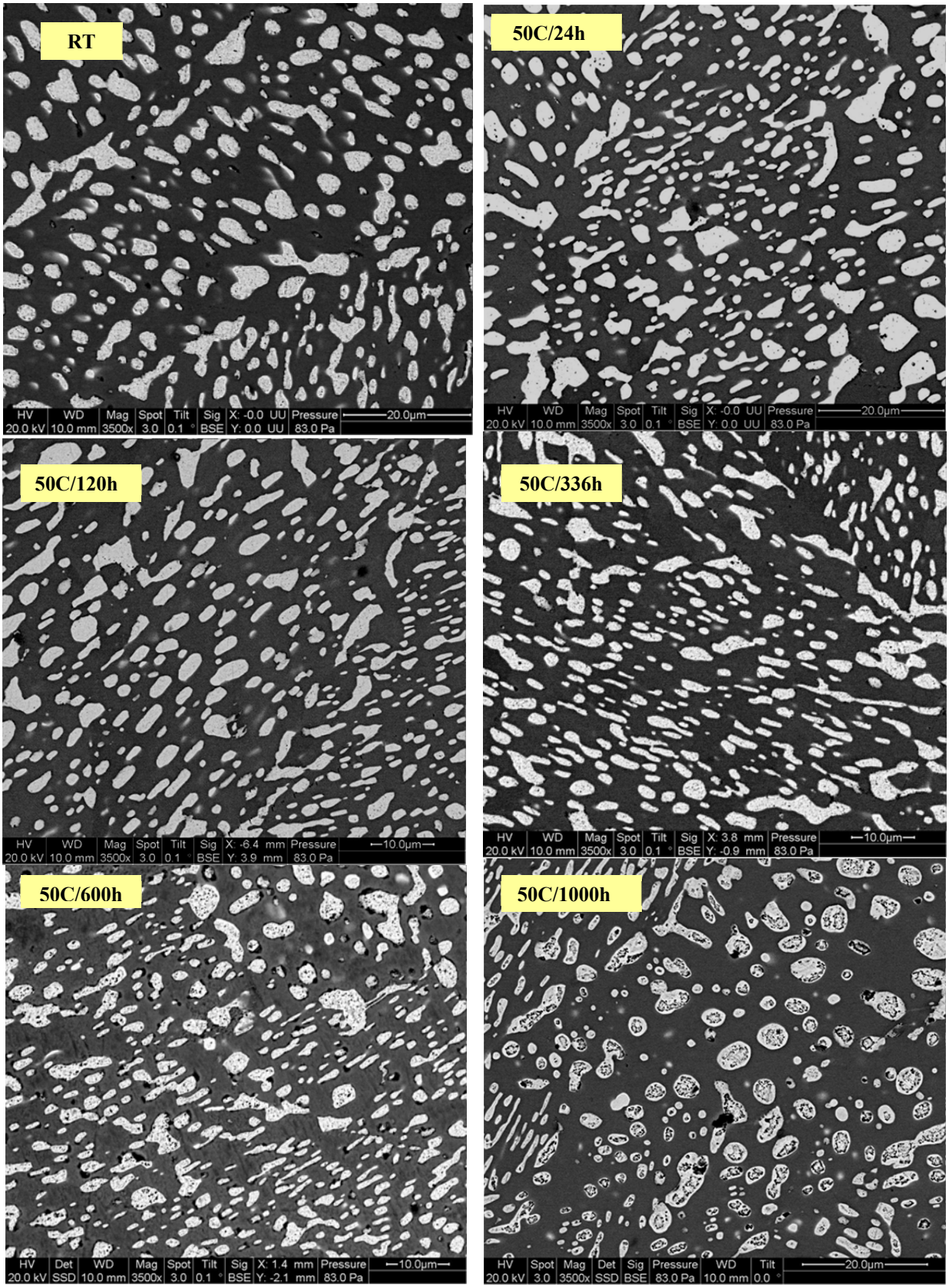
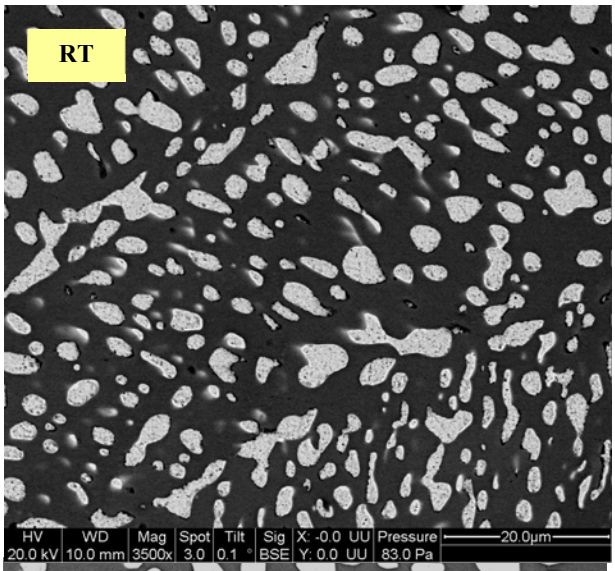
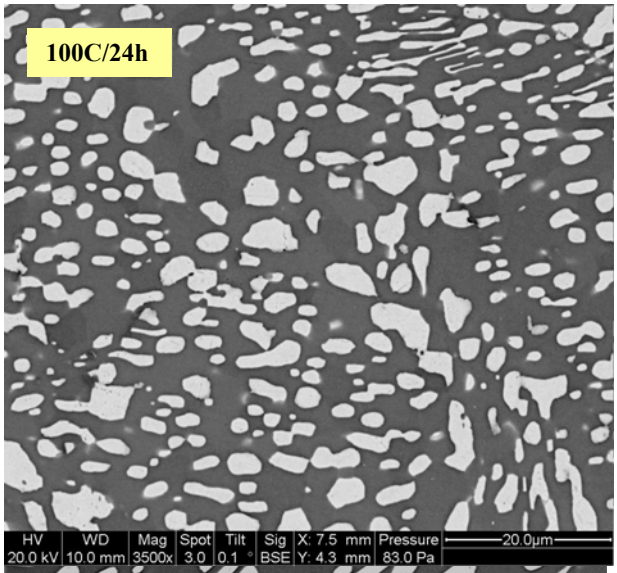
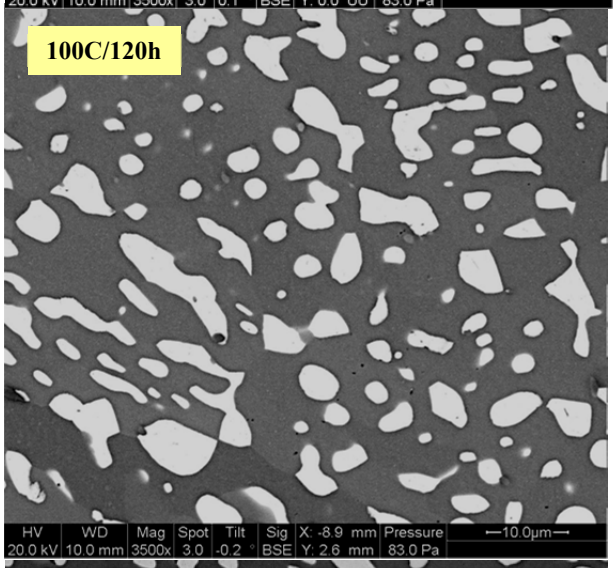
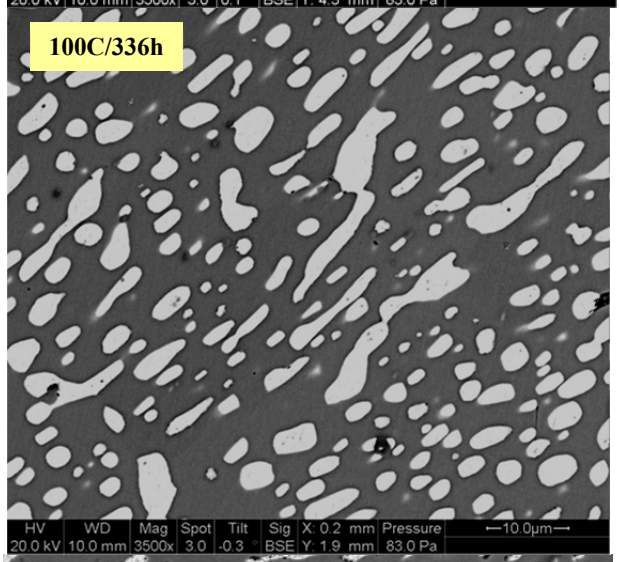


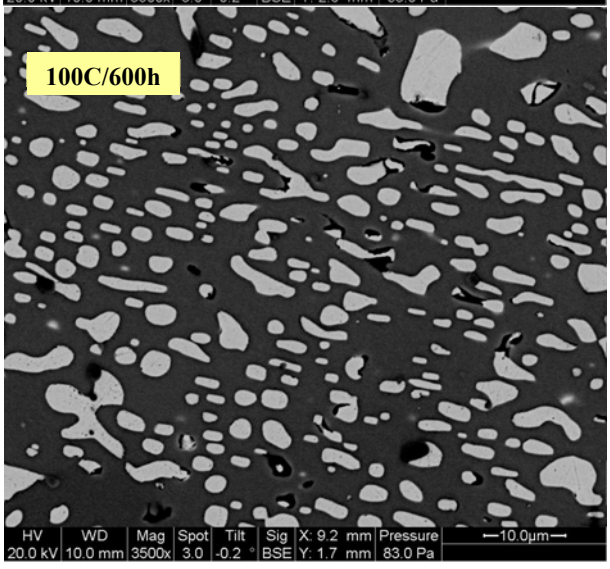
Figure 8.7: Evolution of bulk microstructure of SnPb solder aged at 50°C

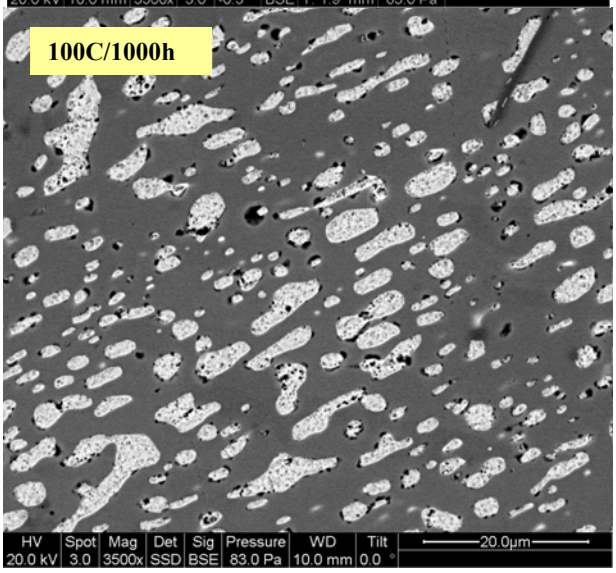

RT
HV 20.0 kV | WD 10.0 mm | Mag 3500x | Spot 3.0 | Tilt 0.1 ° | Sig BSE | X: -0.0 UU Y: 0.0 UU | Pressure 83.0 Pa | 20.0µm


100C/24h
HV 20.0 kV | WD 10.0 mm | Mag 3500x | Spot 3.0 | Tilt 0.1 ° | Sig BSE | X: 7.5 mm Y: 4.3 mm | Pressure 83.0 Pa | 20.0µm


100C/120h
HV 20.0 kV | WD 10.0 mm | Mag 3500x | Spot 3.0 | Tilt -0.2 ° | Sig BSE | X: -8.9 mm Y: 2.6 mm | Pressure 83.0 Pa | 10.0µm


100C/336h
HV 20.0 kV | WD 10.0 mm | Mag 3500x | Spot 3.0 | Tilt -0.3 ° | Sig BSE | X: 0.2 mm Y: 1.9 mm | Pressure 83.0 Pa | 10.0µm


100C/600h
HV 20.0 kV | WD 10.0 mm | Mag 3500x | Spot 3.0 | Tilt -0.2 ° | Sig BSE | X: 9.2 mm Y: 1.7 mm | Pressure 83.0 Pa | 10.0µm


100C/1000h
HV 20.0 kV | Spot 3.0 | Mag 3500x | Det SSD | Sig BSE | Pressure 83.0 Pa | WD 10.0 mm | Tilt 0.0 ° | 20.0µm

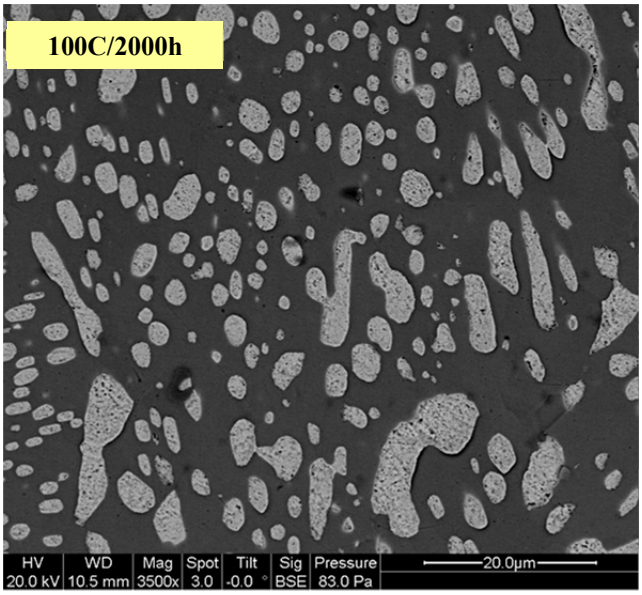


Figure 8.8: Evolution of bulk microstructure of SnPb solder aged at 100^{o}C

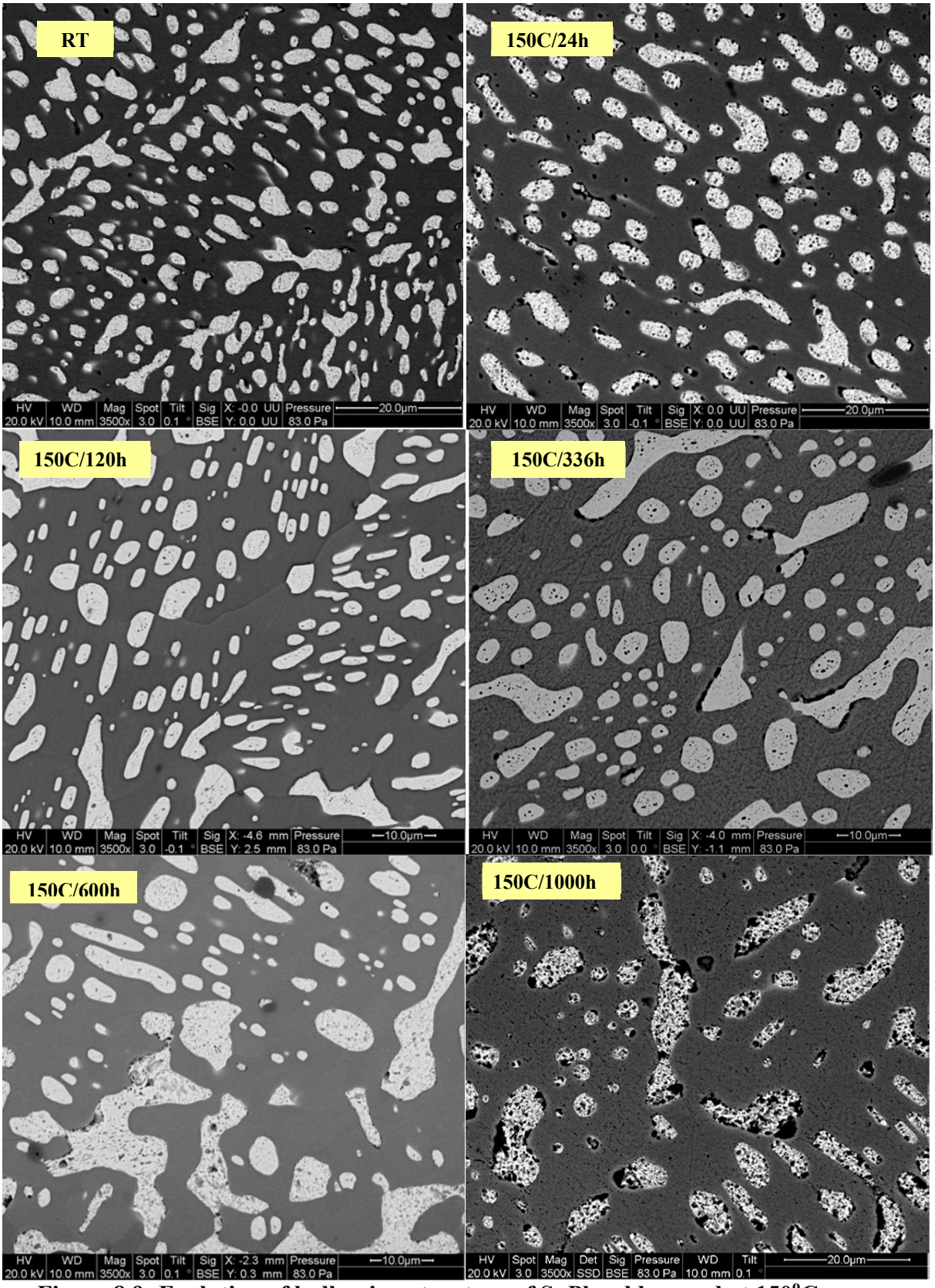


Figure 8.9: Evolution of bulk microstructure of SnPb solder aged at 150°C

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