ABSTRACT

Title of Document:	MODELING THE PHYSICS OF FAILURE FOR ELECTRONIC PACKAGING COMPONENTS SUBJECTED TO THERMAL AND MECHANICAL LOADING
	Gilad Sharon, Doctor of Philosophy, 2011
Directed By:	Professor Donald Barker, Department of Mechanical Engineering

This dissertation presents three separate studies that examined electronic components using numerical modeling approaches. The use of modeling techniques provided a deeper understanding of the physical phenomena that contribute to the formation of cracks inside ceramic capacitors, damage inside plated through holes, and to dynamic fracture of MEMS structures. The modeling yielded numerical substantiations for previously proposed theoretical explanations.

Multi-Layer Ceramic Capacitors (MLCCs) mounted with stiffer lead-free solder have shown greater tolerance than tin-lead solder for single cycle board bending loads with low strain rates. In contrast, flexible terminations have greater tolerance than stiffer standard terminations under the same conditions. It has been proposed that residual stresses in the capacitor account for this disparity. These stresses have been attributed to the higher solidification temperature of lead free

solders coupled with the CTE mismatch between the board and the capacitor ceramic. This research indicated that the higher solidification temperatures affected the residual stresses.

Inaccuracies in predicting barrel failures of plated through holes are suspected to arise from neglecting the effects of the reflow process on the copper material. This research used thermo mechanical analysis (TMA) results to model the damage in the copper above the glass transition temperature (Tg) during reflow. Damage estimates from the hysteresis plots were used to improve failure predictions.

Modeling was performed to examine the theory that brittle fracture in MEMS structures is not affected by strain rates. Numerical modeling was conducted to predict the probability of dynamic failure caused by shock loads. The models used a quasi-static global gravitational load to predict the probability of brittle fracture.

The research presented in this dissertation explored drivers for failure mechanisms in flex cracking of capacitors, barrel failures in plated through holes, and dynamic fracture of MEMS. The studies used numerical modeling to provide new insights into underlying physical phenomena. In each case, theoretical explanations were examined where difficult geometries and complex material properties made it difficult or impossible to obtain direct measurements.

MODELING THE PHYSICS OF FAILURE FOR ELECTRONIC PACKAGING COMPONENTS SUBJECTED TO THERMAL AND MECHANICAL LOADING

By

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Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
2011

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Dedication

To all of those who have helped me along the way, especially the ones who stuck with me until the end.

To my family, the core of support in my life.

To KLF.

Acknowledgements

I gratefully acknowledge the members of my dissertation committee, Professors Barker, Bruck, McCluskey, Al-Sheikhly, and Dr. Azarian, for their support and encouragement. I thank my advisor, Professor Barker, for his invaluable guidance and assistance since I began working at the Center for Advanced Life Cycle Engineering (CALCE). Thanks are due to Professor Abhijit Dasgupta, Michael Freda, and to Srujanbabu Sridharala for introducing me to Hypermesh.

There are many others who made my time at CALCE memorable, including Dr. Barker's former students: James Watkins, Aaron Johnson, Patrice Gregory, Rachel Oberc, Alan Yu, Beth Paquette, and Saifa Hasin. I thank them for their help and for their friendship. I appreciate the generosity and mentorship extended to me by Dr. Muhammad Kehnemouyi, who encouraged me to attend graduate school.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1. Background and Motivation

This dissertation presents three separate modeling efforts to better understand failures of selected electronic components under mechanical and thermal loading. Each of these studies was accepted for publication in peer-reviewed journals in 2011. The studies are related in that the use of detailed finite element modeling is used to shed light on the factors driving the failures. The finite element analyses that were developed can ultimately assist designers and end users to mitigate these failures. The first study addresses cracking within multi-layer ceramic capacitors (MLCCs) that occurs when printed circuit boards are bent.[1] The second study describes efforts to model the failure of the copper barrel in electroplated copper through holes on printed circuit boards during thermal cycling, particularly in thermal cycling when the upper temperature exceeded the glass transition temperature of the board material.[2] The third study describes efforts to model brittle failure within micro-electromechanical (MEMS) accelerometers made of single crystal silicon (SCSi).[3] The capacitor cracking modeling is the primary focus of the dissertation, but the approach taken in this model was common to the models employed in the other

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[1] G. Sharon, D. Barker, "Modeling Stress Responses of Multi-Layer Capacitors Using Varying Termination Geometries," *Journal of Failure Analysis and Prevention*, accepted for publication, 2011.
[2] G. Sharon, D. Barker, "Modeling of Plated Through Hole Reliability and Performance," accepted for publication; to appear in *Multidiscipline Modeling in Materials and Structures Journal*, Vol. 7, No. 3 (2011).
[3] G. Sharon, R. Oberc, D. Barker, "Developing a Test Methodology to Assess the Dynamic Response of MEMS Structures," *International Journal of Structural Integrity*, accepted for publication, 2011.

studies. The primary differences between the modeling studies were the loading (i.e., mechanical or thermal) and the constitutive equations.

The original concern that capacitor manufacturers had was that the stiffer lead-free solder would cause more capacitors to crack in bending. Contrary to this belief, tests showed that lead-free solder was actually better for flex cracking. The theory was proposed that the CTE mismatch between the board and capacitor coupled with higher solder solidification temperatures was the physical driver of this occurrence. The modeling effort contributes to the understanding of this effect.

The plated through hole (PTH) study addresses the concern that processing temperatures above glass transition temperatures together with thicker boards and decreased aspect ratios of plated through holes made it impossible to quantify the damage incurred in the copper. The research presented here improved the qualification procedures for plated through holes, allowed the design of interconnect stress test for greater temperature ranges and improved the useful life predictions of PTHs.

The study of SCSi MEMS structures examined brittle failure of simple structures to find the actual strength of the delivered parts. The strength of silicon used in MEMS devices is related to the amount of damage causes by its fabrication process. A testing method was used to find the amount of weakening cause to SCSi after it was processed in fabrication. The models and testing used the fact that SCSi does not exhibit strain rate dependent properties in dynamic loads to quantify the amount of damage in the “as delivered” MEMS parts.

Each of the studies addressed failures that were known but not yet fully understood with both numerical modeling and physical testing to explain the drivers of failure mechanisms. The studies make use of modeling the physics of failure to confirm an abstract explanation of failures.

1.1.1. Multi-Layer Ceramic Capacitors: Current Challenges

The market for MLCCs is expected to soon exceed $10 billion annually (Zogbi, 2009). MLCCs are often attached using lead-free solders such as tin-silver-copper (SnAgCu, or "SAC"), which have attained widespread use as the industry has shifted from tin-lead eutectic solders in response to far-reaching environmental legislation (Shina, 2008). In contrast, the materials for the electrodes, dielectric, board pads and the printed circuit board (PCB) itself have been largely unchanged. Typically, a printed circuit board might experience three temperature cycles before being put to operational use (Nolte, 2002). The reflow cycle for connecting the capacitors to the printed circuit board depends on the type of solder, where the lead-free solders generally require a relatively higher temperature for processing (McGrath, 2005). In regular use, the board may be subjected to cyclic bending, vibrations, temperature cycles and high-g loading conditions.

Capacitor cracking has plagued the microelectronics industry for decades (Maxwell, 2006). Cracks have tended to appear in the ceramic body of capacitors, located on the bottom of the capacitor close to the termination (Keimasi *et al.*, 2006). As capacitors shrink in size, the appearance of cracks has diminished under certain loading conditions. To mitigate the effects of board bending on capacitor reliability, flexible terminations made of silver-filled epoxy have been used to replace the copper

terminations as the capacitor leads (Ellis, 2008). However, reliability analyses of flexure of boards containing lead-free solder assemblies to produce cracks (i.e., flex cracks) have yielded mixed results (Lai *et al.*, 2005).

The increasing use of capacitors within highly miniaturized electronic products motivates the need for improved performance in lead free assemblies (Keimasi *et al.* 2006). Higher market demand for capacitors in consumer, industrial, automotive, and military applications corresponds to a drive to understand the cause behind capacitor cracking. Once this phenomenon is more clearly understood, cracking can be more accurately predicted, and designers of capacitors will be in a better position to mitigate cracking without sacrificing performance. Correspondingly, capacitor design tools are also in continuous need of improvement. Existing cracking calculators and other analytical tools do not necessarily account for all the factors that can now be examined in reliability models for capacitor cracking. Improving the tools for capacitor design is a key step to extracting higher performance from capacitors.

1.1.2. Description of Multi-Layer Ceramic Capacitors

Multi-layer ceramic capacitors have been studied since the 1960s (Youngs, 1962; Hamer, 1969). A typical; surface mounted capacitor is made of several parallel plates that form the capacitor's electrodes. Encasing the electrodes is a ceramic dielectric serving as both the dielectric and the capacitor body. The capacitor has two leads that connect the electrodes to the pad on the board via a solder joint. These leads are called the terminations of the capacitor. The terminations are made of metallization layers that are connected to the ceramic material and conduct electricity

to the electrodes, as shown in Figure 1. The metallization layers for flexible terminations are made of a silver-filled polymer (SFP) coated with a conductive layer. The capacitors are connected to the printed circuit board using solder, while the solder is in a paste that is applied with a solder mask. The capacitors are placed in their locations and the entire board is placed in an oven for the reflow cycle.

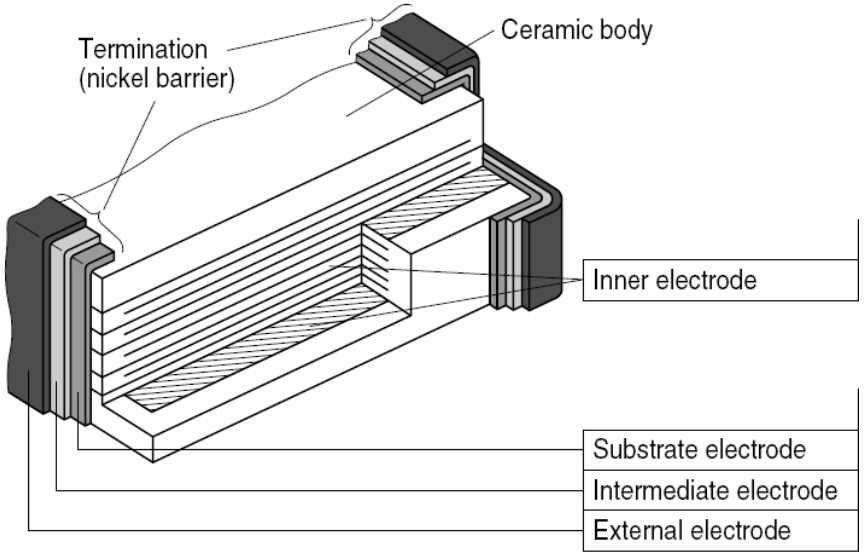


Figure 1: MLCC structure
(adapted from EPCOS B37941 Datasheet, 2006)

1.1.3. Numerical Modeling Approaches

Numerical simulation offers the potential for increased insight into failure mechanisms with greater efficiency and lower costs than time-consuming physical testing (Xie *et al.*, 2008). Particularly for high-reliability electronics, numerical simulations allow for calculation of time-to -failure (TTF) and other reliability metrics and performance characteristics that would normally require long observation periods. However, computationally intensive simulations may be equally expensive and lengthy, and the outputs of the model are only as credible as the model's inputs.

Therefore, this research effort sought to ensure the utility of the models that were created to predict when the components would experience failure.

To overcome the problem of gathering failure data for high-reliability components that would normally experience long lifetimes before failure, various accelerated testing methodologies have emerged (Khatibia *et al.*, 2009; Nelson, 2004). Data derived by following these methods have helped manufacturers in their component qualification and reliability assessment. Manufacturers of electronic packaging components have successfully employed Interconnect Stress Testing (IST) and Highly Accelerated Thermal Shock (HATS) testing in their reliability programs since the late 1990s (Furlong and Freda, 2004). Although these techniques had gained support and acceptance within industry years later, little was known within the electronics industry with respect to efficient and trustworthy methods for analyzing and using the data that these tests produced (Freda and Barker, 2006).

The importance of determining the extent to which a model actually reflects reality with respect to its intended uses has been recognized (Sornette *et al.* 2007). Ho *et al.* (2009) observed that evaluation of models can serve an initial purpose of determining whether a method is suitable for simplified simulated data and can then be repeated as the method evolves. The model that was developed for cracking within MLCCs relied upon some of the same assumptions used in a model that was intended to predict damage to the copper inside plated through holes (PTHs) on printed circuit boards. The plated through hole model possessed some features that were shared by the more complex MLCC model. The model for the plated through holes had some similarities with the MLCC model in two respects. First, they

provided a test case wherein a simplified finite element analysis using a symmetrical model could be performed. This symmetrical modeling scheme was used for the more complex MLCC components on the same scale. Second, a key commonality between plated through holes and MLCCs was that both were susceptible to CTE mismatches between themselves and the printed circuit board, an important suspected failure driver that could be examined through modeling.

It has been established that a two-dimensional model can be used for assessing a three-dimensional phenomenon (Keimasi *et al.*, 2006; Blattau, 2004). This approach has been used to model microelectronic devices, including MEMS (Suresh and Sinha, 2006). In this case, a model was developed on the same scale for the same physical dimensions and temperature range. The modeling approach of using a two-dimensional model to simulate a three-dimensional phenomenon was used for the MLCC model. The thermo-mechanical parameters, both in temperature range and physical dimensions were the same for the plated through holes and the MLCCs. The plated through hole study uses a two-dimensional round cross section to approximate a three-dimensional round component, whereas the MLCC cross section is not round. In this study, the bending load on the capacitor was assumed to be applied in the x and y directions (Keimasi *et al.*, 2006; Blattau, 2004). In addition, the plated through hole study showed that information of value from the thermo-mechanical interactions between laminates and connected components can successfully be extracted from a simple model, unlike the MLCCs, where the cross-sectional geometry is more complex.

The modeling required skills and familiarity with CAD and FEA software (Pro/Engineer, Hypermesh, ANSYS, and Abaqus) to construct test cases from the ground up, and to correlate the model to the physical characteristics. An advantage of the two-dimensional simulation is the ability to receive feedback on several parameters quickly despite constructing neither a three-dimensional Computer Aided Design (CAD) model nor a volume or surface mesh (Suresh and Sinha, 2006). Plated through holes were not appropriate for a brittle failure analysis because the copper material accumulated damage in hysteresis and did not exhibit brittle fracture. A different test case was used to develop a dynamic fracture model on the same scale.

1.2. Objectives

Many steps are needed to close the existing gaps in the body of knowledge about the behavior of surface mounted ceramic capacitors. There is a large amount of information that must be analyzed. Although a variety of techniques have been developed based on experience, some have not been corroborated using established research methods. In this research, the existing knowledge gap in the basic physics-of-failure (PoF) governing capacitor cracking will be addressed. Using a synthesis of proven modeling methods, this research explored the mechanical inner workings of capacitors and recreated the physical experiments in a virtual environment. In addition to providing information to supplement the current research about capacitor cracking, this research can be used to update the existing tools for calculating capacitor cracking. It will supply information about lead-free solder and flexible termination materials that can be incorporated into existing capacitor cracking algorithms.

The number of factors affecting the behavior of capacitors in bending load has increased as the restrictions on material selections have taken effect. The increasing number of lead-free solders is but one contributor. Each manufacturer has different processes for making similar capacitors. Some of the differences, such as different overall product size, can be easily characterized and are easily found by obtaining manufacturer data sheets. Other differences, such as the actual profile of the capacitor termination, can only be seen by examining the inside of a capacitor. The many factors contributing to capacitor performance increase the complexity of the problem and need to be explored comprehensively. In order to find the specific contributions to the physics of failure, these factors must be systematically isolated and accounted for in the modeling effort. The resulting method for analyzing the different loads, materials and geometries was used to study specific test cases. Some of the different geometries, materials and loads were studied in detail with the objective of creating a robust foundation for the exploration of increasingly complex advancements in surface mounted technologies.

1.3. Organization

Following this introductory chapter, the literature discussion in Chapter 2 highlights the major academic and industry work on modeling of capacitor cracking. In addition, Chapter 2 reviews the use of finite element methods for more general efforts to characterize materials and to assess reliability. Chapter 3 describes the capacitor cracking in detail, provides an overview of the finite element model that was developed, and illustrates the results gleaned from the numerical modeling. Chapter 4 focuses on the creation of an axi-symmetric two-dimensional model that

was used to simulate damage in copper plated through holes. Moving to a different test component and finite element model architecture, Chapter 5 presents the results of a modeling effort to examine brittle failure inside SCSi MEMS devices. This model was a three-dimensional system with multiple degrees of freedom subjected to a global gravitational load. Chapter 6 discusses the common themes that emerged from the development of the separate models presented in Chapters 3-5. Chapter 6 summarizes the conclusions and contributions of the research presented, and it suggests areas for future investigation and inquiry.

Chapter 2: Review of Previous Research

A substantial amount of previous work has explored the problem of capacitors cracking. There are many ways to examine the factors that contribute to cracking. The literature review of published research is divided in two parts. The first part is meant to summarize the discussion of capacitor cracking that has been raised by manufacturers and suppliers of capacitors. The manufacturers' literature is generally intended to instruct the end users and customers how to use their products to achieve the best performance. Another concern for manufacturers is competition in the marketplace. The manufacturers must compete for their customers and need to educate them on the advantages of using their products over alternatives.

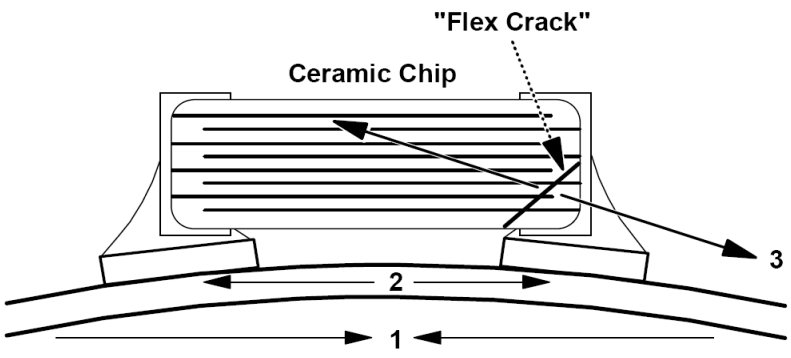
The second part of the literature review describes the ideas and initiatives that have occupied academics working in diverse fields including mechanical and electrical engineering, reliability, computational modeling, and materials science. This academic research is often supported by partners or sponsors from industry. This industry partner may be a customer or supplier of the products in question. Balconia and Laboranti (2006) concluded that academic proficiency in microelectronics research is associated with intense collaboration with industry partners. The academic papers benefit from the added credibility of more references and more comprehensive explanations of the design of experiments. They provide expository information about the design rationales reflected in the part specifications that appear in the technical reviews and notes published by manufacturers. The academic literature has provided objective comparisons of similar products from

different suppliers. This literature review was not only intended to survey the current state of the art but also the historical evolution of the findings.

2.1. Multi-Layer Ceramic Capacitors

2.1.1. Reports from Manufacturers

Bergenthal (1998) reported research efforts at the KEMET Electronics Corporation and advanced a hypothesis for the appearance of cracks in ceramic capacitors on boards subjected to flexure. This report is a manufacturer's explanation and solutions provided to its customers about the appearance of cracks in capacitors when subjected to flexural stress. The paper outlines the resulting crack in the capacitor from the board being bent with tension on the side of the board with the capacitor (in this study, the top of the board) and compression on the side without the capacitor, as shown in Figure 2. This study focused on the strain on the top of the board as the main parameter for determining the likelihood of failure in the capacitor. The approach to flexural (or flex) cracking employed in this case was to find a solution that works even if the root cause is not apparent, i.e., a 'workaround' that would be of interest to users. The importance of this study is to show that strain measured at the top of the board does not paint a complete picture of flex cracking, and that other factors were responsible for the appearance of cracks.



1. Bottom side of board in compressive state
2. Top side of board in expansive state
3. Ceramic in Tension as a result of the applied stress.

Figure 2. Crack profile appearing in capacitors subjected to bending load (adapted from Bergenthal (1998))

At the end of the technical review, the author remained unsure as to how flex cracks appear at some places on boards. An additional complication in this study was the difficulty of determining the root cause when only one or two cracks appeared in the specimens. The question of what had caused the capacitors' failure in the absence of significant flexural stresses was unanswered. Although the capacitors that were removed from the board and analyzed showed signs of flexural cracks, no single convincing explanation accounted for their formation. The KEMET approach was to explore known contributors to cracking in attempting to identify a working solution.

Research conducted by the AVX Corporation examined a variety of cracks that have appeared in capacitors (Maxwell, 1988). The examination of flexural cracking in capacitors found that the cracks are positioned at a 45º angle and that the crack occurs quickly. This study found that a flex crack usually exists in isolation as a single crack and that the ceramic fails in the tensile mode. The author observed that the board flexural forces are not only due to handling of the boards but also due to storage, warping and force fitting in assemblies. This research is significant for its

discovery of the cause of failures based on the shape of the cracks within the body of the capacitor.

The AVX study describes several sources to which it attributes the formation of cracks within capacitors. Thermal cracks are caused by the change of temperature and the coefficients of thermal expansion. Maxwell (1988) defined thermal shock as mechanical damage that is caused by the inability of a given structure to absorb the mechanical stresses that result from large changes in temperature occurring over short time spans. The soldering process was cited as a key contributor for the substantial changes in temperature. Several additional steps during the board manufacturing and handling processes may lead to stresses, including the pick and place machine, the vacuum pick-up bit, the centering jaw, the top jaw and the bottom centering jaw. Once the board comes out of the soldering process, it is subjected to several load conditions that can cause cracks. The board is sensitive to bending during depanelization, testing, final product assembly, connector assembly and component placement. This study organized the information from various sources for the CTEs as shown in Table 1.

Material	**CTE (ppm/°C)**	**δT (W/m°K)**
Alloy 42	5.3	17.3
Alumina	≈7	34.6
Barium Titanate	9.5-11.5	4 to 5
Copper	17.6	390
Filled Epoxy	18-25	≈0.5
Si02	0.57	3.4
Nickel	15	86
Silver	19.6	419
Steel	15	46.7
Tantalum	6.5	55
Tin Lead Alloys	≈27	34

Table 1. CTEs and δTs of component materials (adapted from Maxwell (1988))

The AVX study is notable for its consideration of the stresses that every step of the manufacturing process can impart to the capacitor; viewing these steps along the entire process leads to the conclusion that damage may accumulate in the capacitor from start to finish well before the product reaches the end user. The shape of the cracks can be indicative of the type of mechanism caused the crack. This study was lacking in the amount of analytical information available for the appearance of cracks. Without this information, it is difficult or impossible to compute the probability of a given type of crack appearing, which has to be determined analytically. The author was not able to utilize a sufficient analytical tool to determine this probability.

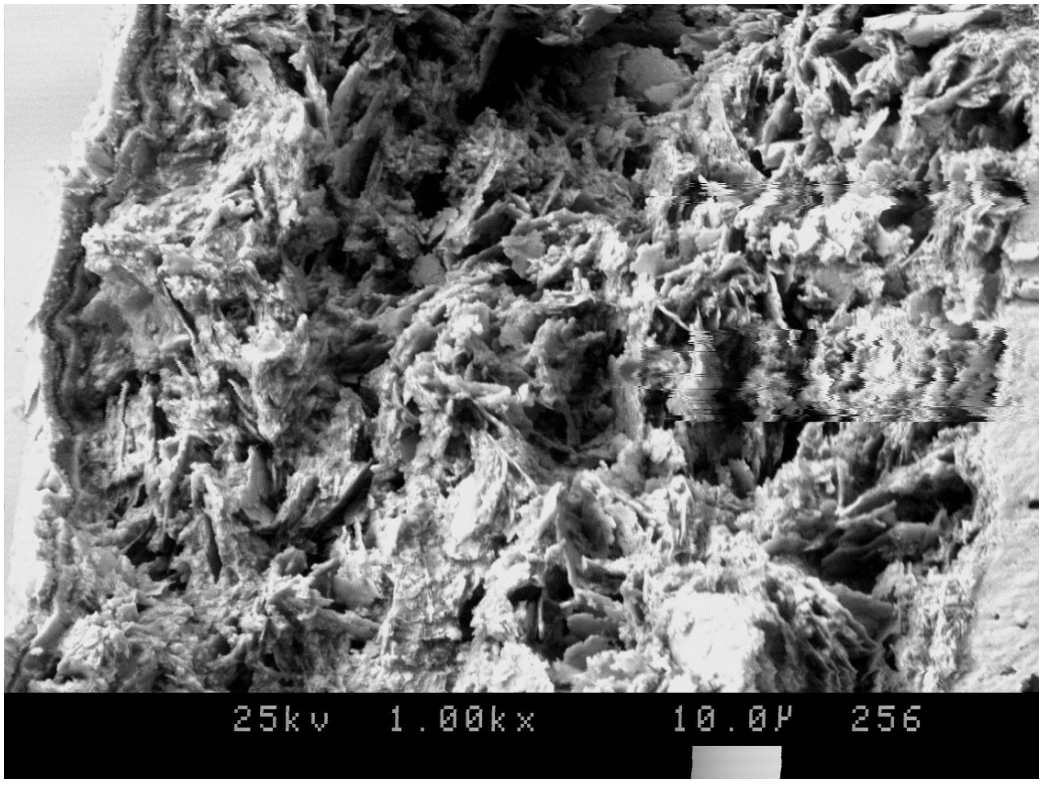


Figure 3. Polymer termination microstructure (adapted from Syfer Tech. Ltd. Report, 2009)

Syfer Technology presented the Silver Filled Polymer (SFP) termination material as the solution for capacitor cracking in board bending (Syfer Report, 2009). Figure 3 is shown to illustrate the basic properties of the polymer termination. Syfer's polymer termination has a fibrous structure and its mechanical and electrical properties remain largely unaffected by extremes of heat and chemical treatments. Following the polymer termination process stage, the capacitors are plated with nickel and tin using the same methods employed for industry standard sintered silver-terminations for capacitors; thus, the soldering characteristics are essentially the same.

An interesting aspect of Syfer's study is the bend test facility used in testing. Figure 4 depicts the test configuration that Syfer employed and shows that the fixture used a "press head" that was 20 mm in width. Notably, this fixture creates a different bending profile than the common three point bend test. The use of this configuration demonstrates that there are different testing schemas used in industry and academic research and underscores the potential differences in defining 'failure' within a particular test regime, a point that was illustrated in the work by England (2006).

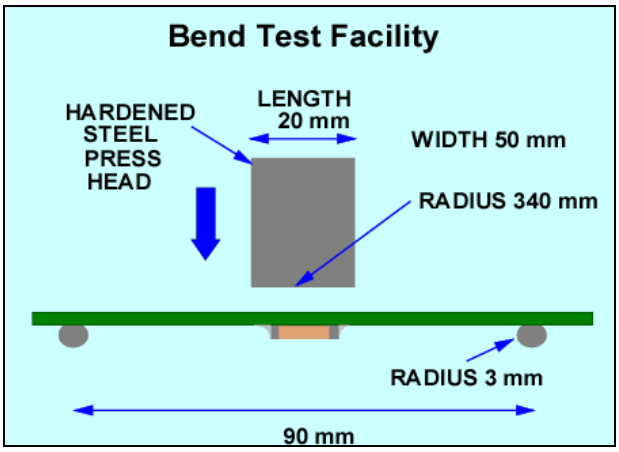


Figure 4. Bend test fixture
(adapted from Syfer Tech. Ltd. Report, 2009)

Syfer additionally contended that its analysis of field failures led to the conclusion that no case could be made for any particular size of chip being especially susceptible to crack-induced failure than its alternatives (Syfer Report, 2008). The study noted the existence of conflicting reports about the effect of capacitor length on the susceptibility of the capacitors to cracking due to board bending.

A technical note by Johanson Dielectrics details the experimental results for failures caused by capacitor cracking due to bending (England, 2006). The test fixture is shown in Figure 5. This experimental procedure used a three point bending fixture in contrast to the test configuration described in the previous technical note and illustrated in Figure 4. In order to obtain a constant strain on the side of the board where the capacitors were located, it would be preferable to use a four-point bend test as described by Keimasi, Azarian, *et al.* (2006).

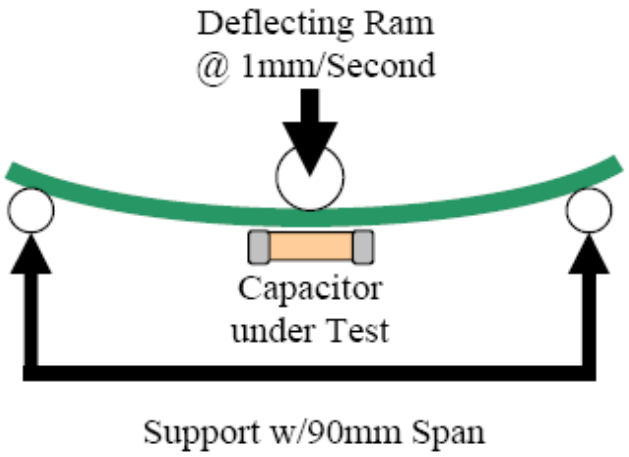


Figure 5. Illustration of three-point bend test (adapted from England (2006))

England (2006) concluded that Johanson Dielectric's flexible Surface Mount Device (SMD) termination, named Polyterm, was useful in reducing or eliminating MLCC failures due to printed circuit board flexure stresses related to board assembly

operations and/or harsh operating environments. Although all components may exhibit some termination separation, there was no degradation observed that would interfere with the operation or performance of the capacitors. The study concluded that the use of the flexible termination in conjunction with proper board layout and handling could greatly reduce or eliminate failures associated with MLCC cracking. The range of sizes examined in this study was 0805 to 2220, mounted in a single line on the board as shown in Figure 6. The failure was defined as either a 10% or 5% loss of capacitance depending on the test. The study's conclusions about flexible terminations have been confirmed elsewhere for medium to low rate bending in which the strain rate of the printed wiring board did not exceed 0.1/sec with a maximum board strain between 260-450 με (Watkins, 2008). Not all testing schemas for capacitors define failure as a factor of loss of capacitance. It is possible to define failure in terms of visible cracking, total separation from board, insulation resistance, and other factors relating to physical characteristics or performance attributes.

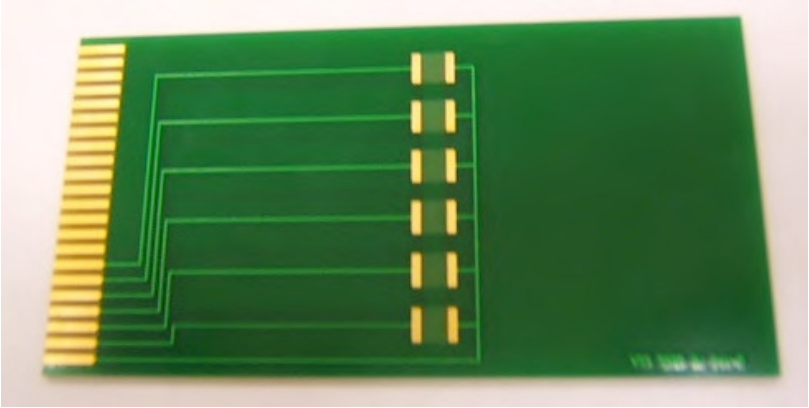


Figure 6. Test board for three-point bend test (adapted from England (2006))

The test board shown in Figure 6 clearly shows that only six capacitors could be accommodated for testing on each board and that the effective area is on the center

of the board. In a four-point bent test, the strain on the board is the same along the entire test surface and more components can be tested per board. The uniformity of strain and the ability to test a larger number of specimens are among the advantages of using a four-point bend test rather than its three-point counterpart. The study showed a correlation between increasing effectiveness of using flexible terminations and decreasing the size of the capacitor.

2.1.2. Academic Research

The academic literature offers numerous hypotheses to explain performance for different combinations of component materials, geometries, and test conditions. For example, Suhling *et al.* (2004) observed that thermal cycling testing has shown that stiff components with high CTE mismatches with the substrate have exhibited poor solder joint reliability for lead-free SAC alloys when the temperature range is large. However, the authors could not correlate the performance of various alloys to any single micro-structural failure. The literature also provides instructive descriptions of test configurations and experimental methodologies to examine researchers' hypotheses.

Keimasi, Azarian, *et al.* (2007) illustrated the use of a four-point bend test for MLCCs situated on printed circuit boards. The test apparatus used in their experiments is shown in Figure 7 to illustrate the positioning of the strain gauge, capacitors and the bending locations. It is apparent that this test geometry allows for the possibility of testing twenty-four capacitors at the same board strain as opposed to the six capacitors, illustrated in Figure 6, from previous experiments using the three-point bend test.

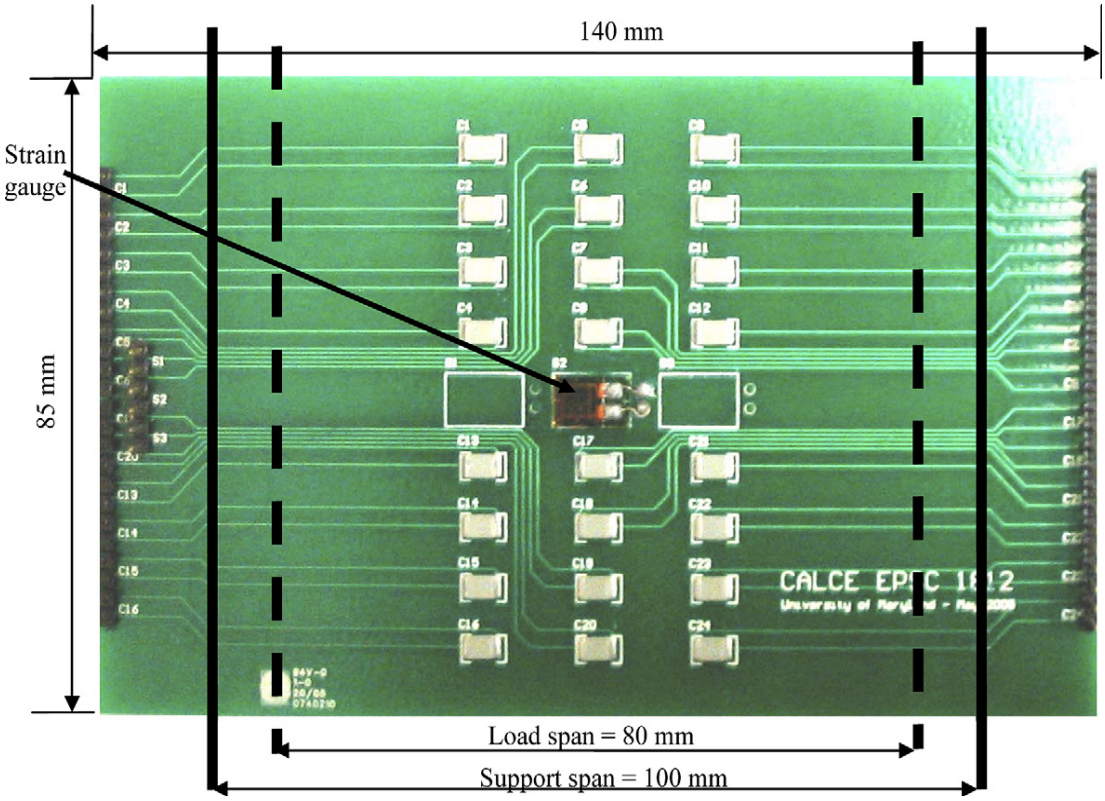


Figure 7. Test geometry for four-point bending apparatus (adapted from Keimasi, Azarian, *et al.* (2007))

The single-cycle four-point bend testing indicated that capacitors mounted with lead-free solder were less likely to exhibit cracking than those mounted with eutectic tin-lead solder. It was theorized that two factors were responsible for the disparity in performance. These factors are the differing elastic-plastic mechanical properties of the solders and the higher residual compressive stresses after solder reflow assembly, which are a result of the higher solidification temperature in the case of the lead-free solder (Sn3.0Ag0.5Cu). From the testing performed on a total of 192 capacitors on eight boards, several significant differences were observed between flexible and standard termination and also between tin-lead solder and lead-free solder. Aging did not appear to affect tin-lead solder assemblies, whereas it was observed to increase the susceptibility to flexural cracking in lead-free solder.

Flexible terminations were observed to have a significantly greater resistance to flex cracking than standard terminations. Several cross-sections were made of flexible terminations and a scanning electron microscope (SEM) was used to capture images of the termination material as shown in Figure 8.

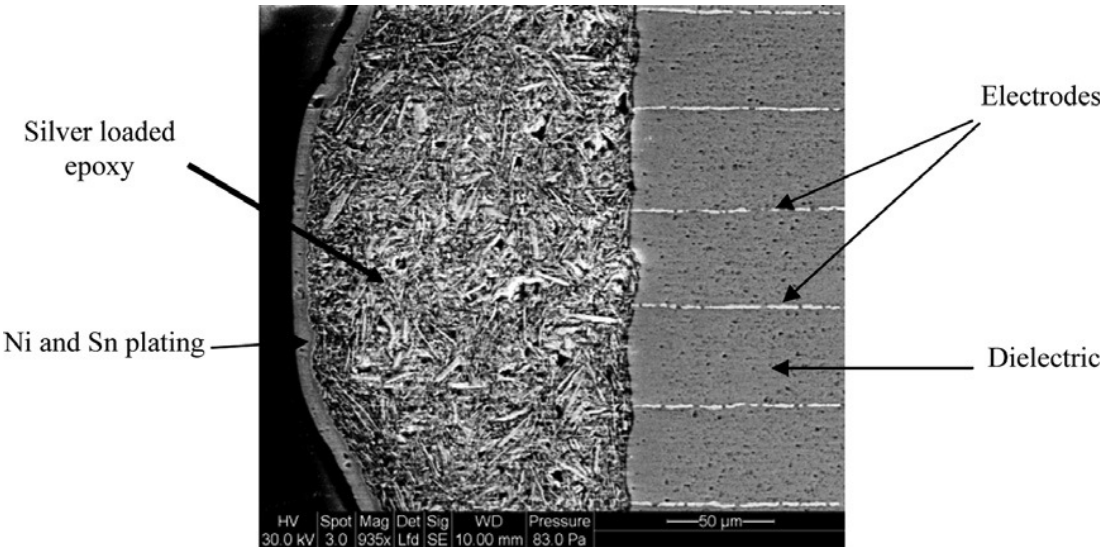


Figure 8. SEM image of the end termination of a flexible termination MLCC (adapted from Keimasi, Azarian, *et al.* (2007))

Some modeling was performed in order to evaluate the stresses in the capacitor body using the strain on the board from the experimental results for failing capacitors. Simplified material properties were used for the termination material. A plasticity model was used for the solders. Although the effect of cooling was modeled, the effects of the creep mechanism were not. A simplified geometry was used in this model as shown in Figure 9. Finite element modeling was performed to recreate the experimental values.

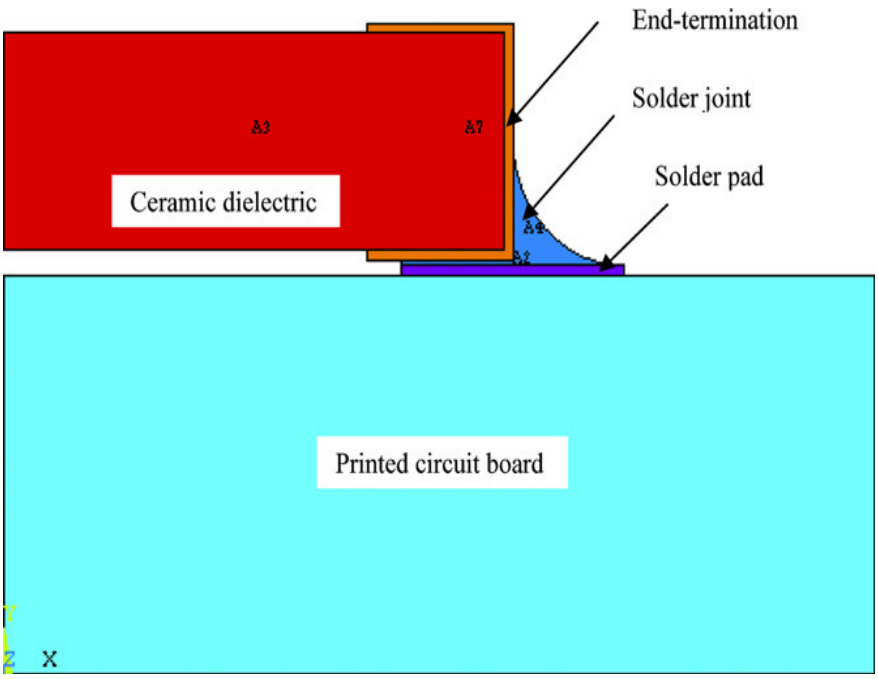


Figure 9. Geometry of the capacitor assembled on a PCB as used in the FEA model (adapted from Keimasi, Azarian, *et al.* (2007))

Jiang *et al.* (2008) developed a three-dimensional theoretical model to estimate the thermal residual stresses in MLCCs based on the effective medium method in micromechanics of composites. The motivation for using this solution methodology arose from a problem encountered with finite element models. Finite element modeling simulation of the sintering process of MLCCs required an extremely large number of discrete elements and an excessive computation time and was deemed impractical for making engineering design decisions. The authors noted the problem of modeling the many dielectric layers in a discrete fashion on the three dimensional space, which creates too many elements to be easily manipulated. Instead, an analytical model was introduced for the body of the capacitor. The body was decomposed to eight parts in order to take advantage of the full symmetry in the ceramic. The following figure shows the further decomposition of the model for the analysis.

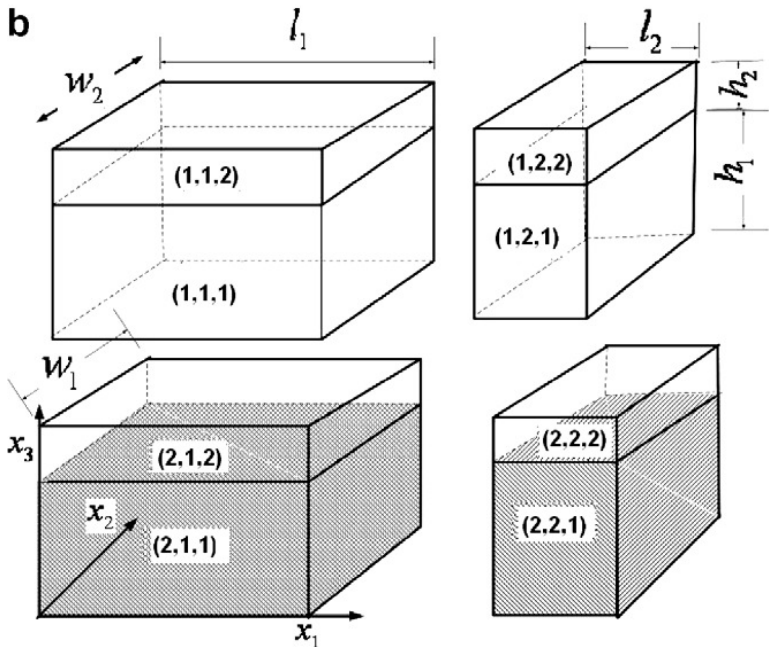


Figure 10. A decomposition of an eighth of an MLCC structure into series and parallel sub-blocks (adapted from Jiang et al. (2008))

The modeling efforts of Jiang *et al.* (2008) yielded computed values for the residual stresses due to cool down from the sintering temperature of the ceramic before the termination is applied to the capacitor. Their research shows that it is possible to use generalized properties to model the ceramic material of the capacitor body with the electrode material. Two observations from this study that were in common with other literature on MLCCs is that both the life cycle of the ceramic itself needs to be considered as well as the existence of many stresses that are introduced through the manufacturing process.

Prume *et al.* (2002) developed a two dimensional finite element model for multilayer capacitors. The model was compared against data from four-point bending tests. The typical cracks appearing in cross-sections of a size 1202 capacitor are shown in the figure below. The cracks were attributed to stresses imparted by bending in the four-point bending apparatus. It is interesting to note that the two

images depict different crack angles propagating from the area where the termination ends along the ceramic capacitor body on the bottom side.

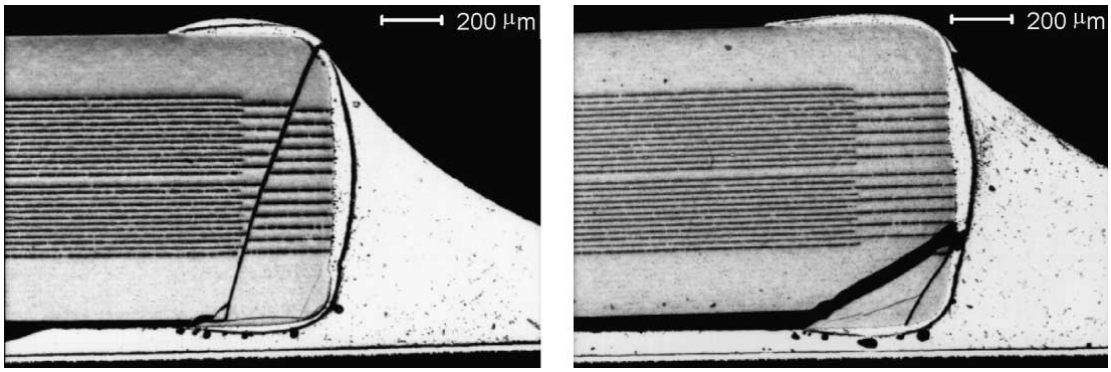


Figure 11. Representative cracks in the polished cross-sections of soldered MLCCs under bending load stress (adapted from Prume (2002))

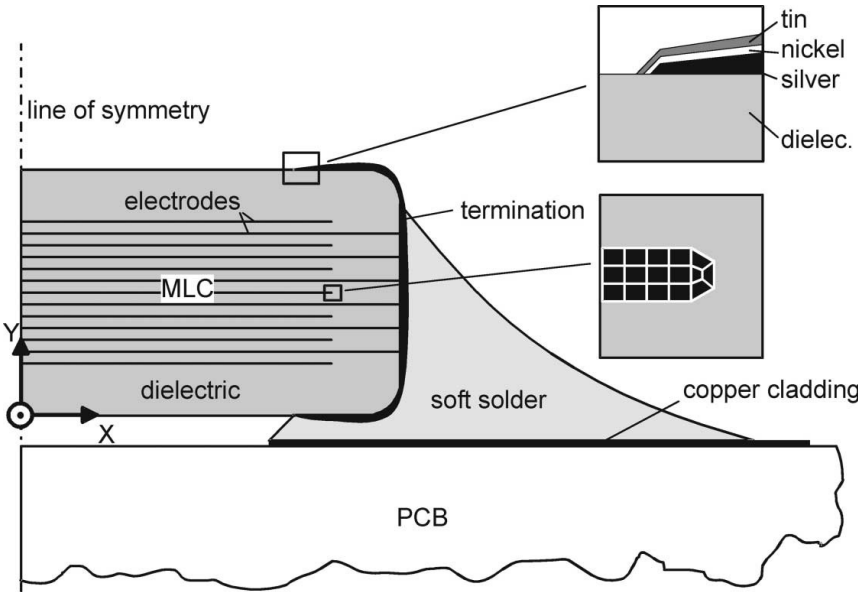


Figure 12. Design of the finite element model of a soldered MLCC (mesh not shown) (adapted from Prume *et al.* (2002))

The finite element model shown in Figure 12 was used to calculate both the bending moment and the stresses in the capacitor body. The solder used was tin-lead and the termination was modeled for the standard silver, nickel and tin layered material. This model also incorporated the electrode layers in the capacitor. Creep

was not modeled in this analysis. Among the discussion of findings in this study, several important areas for future work were suggested. The gaps in existing work were noted by the authors. They noted that improved accuracy in stress calculations and failure predictions would be obtained following a shift to three-dimensional models and the development of a more detailed simulation of the residual stresses.

As later discussed by Jiang *et al.* (2008), three-dimensional modeling has been performed relying on the symmetry of the component of interest. An eighth of the capacitor body was modeled and evaluated based on its symmetry. The finite element method was employed because it was able to produce more detailed information about localized stresses than physical experiments could produce. The study includes a discussion on the importance of comparing the models against experimental results. The model was developed in reliance on the assumption that the layered elements have perfect bonding. This point is significant for the assumption that the whole capacitor body can be modeled as having a single material property. Figure 13 shows the three dimensional one eighth model used for the analysis.

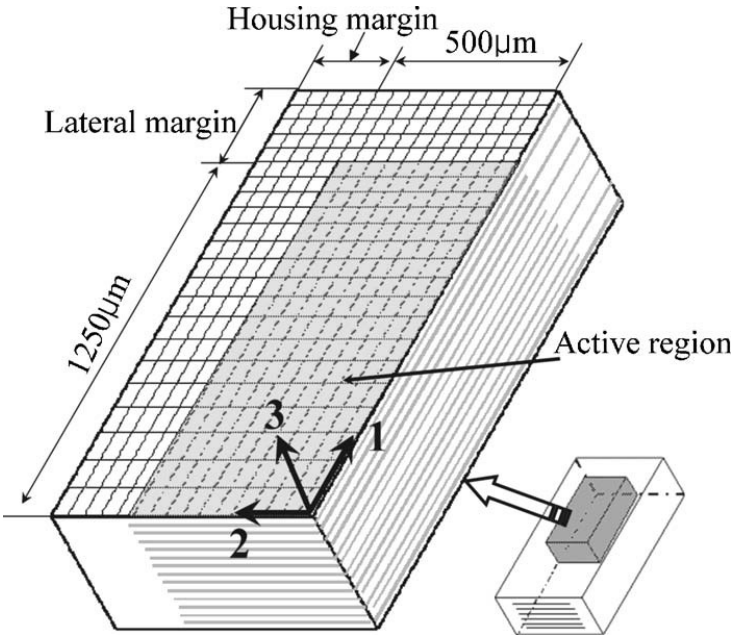


Figure 13. Geometry of MLCC and 3-D model used to calculate residual stress (adapted from Shin *et al.*(2007))

This research focused on the effects of the different geometries of the capacitor body's elements. One of the points emphasized in this study was the recurring problem of not being able to measure the stresses in the capacitor directly. While there is a method for measuring near surface stresses using x-ray diffraction, when the area inside of the capacitor is cross-sectioned, the stresses are relieved and cannot be measured. The literature's focus on finite element modeling reflects pragmatism regarding the limitations of existing tools for direct physical measurement and the potential knowledge to be gained using simulation techniques.

2.2. Finite Element Analyses for Electronic Surface Mounted Components

Finite element models are constructed using simulation methods that incorporate a fixed number of elements to produce numerical and graphical outputs. The number of calculated nodes and the number of dimensions in the model affect the model's complexity. In addition to the simulated portions, developers of finite

element models may use case studies from physical testing to assess their models. One of the disadvantages of finite element models and finite element analyses is that the modeler must be familiarity with both the underlying software package and the relevant algorithms. Building a complex finite element mesh requires systematic and methodical development and continual documentation of assumptions and decisions. Without proper meshing techniques, erroneous results may reduce or completely negate the value of using the model. The finite element analysis is a time intensive process that includes constructing the model, finding detailed information for material properties, and performing extensive post-processing of results to determine appropriate parameters for stress, strain, or other values of interest. Information about the mechanical, material, and geometric properties may be proprietary or unavailable.

The errors that are among the most difficult to detect and correct are the errors that may exist inherently within the simulation package itself; these errors may be propagated throughout a model. Darveaux (2000) used the ANSYS finite element simulation package to produce a generalized model to predict the fatigue life of solder joints for surface mount packages. His results were published before it was realized that the ANSYS 5.2 finite element code contained an error in its algorithm for calculating plastic work that had produced errors in the model (Darveaux, 2000). Even after the plastic work calculation bug was corrected, significant errors skewed the prediction of solder joint fatigue life. This error was attributed to the use of constants for the crack growth algorithm that had been generated using the erroneous

calculations for plastic work. In version 5.6 of ANSYS, these errors had been corrected.

The use of finite element methods to analyze electronic packaging systems has led to the development of techniques and best practices to improve accuracy and efficiency. Darveaux (2000) noted that maintaining consistency in the modeling procedures was essential to producing accurate models. Modeling using simplifications that neglect complex features may be used to obtain preliminary results and to expedite the analysis. Simplification of the model represents a tradeoff between greater and more realistic detail and total modeling time.

Finite element analysis was employed by Sidharth and Barker (1996) to determine the fatigue life of the corner leads in a leaded assembly. The finite element model was found to predict fatigue-induced failure successfully even though it had not been based on experimental test data. The model was later correlated against data derived from experimental testing. Sun *et al.* (2005) made some simplifications in a finite element analyses that was used in tandem with a low cycle fatigue test to obtain constants for Sn37Pb and Sn8Zn3Bi in the Coffin-Manson equation, which is used to predict the number of cycles to failure based on the material constants and the change in inelastic strain per cycle.

The Coffin-Manson equation holds that:

$$N_f = A \cdot \Delta\varepsilon^m \qquad \text{(Eq. 2.1)}$$

Where: $\Delta\varepsilon$ is the inelastic strain range per cycle
N_f is the number of cycles to failure, and
A and m are material constants.

Sun's model included a printed circuit board, solder joint, and the copper pads. Elastic strain was not considered, but a three-dimensional model was incorporated to study edge effects. The model permitted calculation of the shear strain range (Sun *et al.*, 2005).

Finite element analysis has also been applied to the fatigue life of solder joints in printed wiring board assemblies. Zhou *et al.* (2007) characterized the behavior of SAC305 solder and eutectic tin-lead solder following a time domain approach. Detailed local finite element analyses were performed to determine a strain transfer function that was then used to convert between printed circuit board stain and solder strain. The components were tested in a high cycle regime using a narrow-band harmonic vibration test and a low-cycle regime that utilized a broad-band random vibration test. As with Sun (2005), the performance of the solder under low-cycle fatigue was correlated using a Coffin-Manson equation. The solder's performance in the high cycle test regime was modeled by the Basquin relation, which characterizes the fatigue life of elastic materials (Zhou, 2007). The Basquin relation holds that

$$\sigma_a = C \cdot (N_f)^{b} \qquad \text{(Eq. 2.2)}$$

Where: σ_a is the stress amplitude
N_f is the number of fully reversed stress cycles to failure
C is a material constant, and
b is the Basquin exponent, which can be approximated as 0.09.

The model constants were obtained for each type of solder (Zhou, 2007). The strain in the critical solder joints and measured time-to-failure data were then incorporated into a generalized strain-life fatigue model for eutectic tin-lead and SAC305 solder. Physical testing using the destructive failure techniques of cross-

sectioning, polishing, and microscopy confirmed the failure mechanism as solder fatigue.

Wong *et al.* (2002) used finite element analysis to obtain a working understanding of the physics of failure when printed circuit boards were subjected to impact by dropping. The three major events used in the simulation were the velocity impact of the drop assembly, the velocity impact of a printed circuit board, and the velocity impact of a printed circuit board on which a component was centrally mounted. For the impact of the assembly, the system was modeled as a solid element with sub-elements; for the printed circuit boards, the system was modeled as a beam. The finite element analysis indicated that elongation and bending of the interconnects due to the difference in flexure between the packaging component and the board was a key factor affecting failure during board level drop testing. This observation was particularly true for components located near the center of the board.

The analysis revealed that the stress wave upon impact and the inertial forces of the packaging component were also drivers for failure. The stress wave and inertial forces were especially influential for components located near the support structure. The analysis revealed that increasing the height of the drop, the length of the printed circuit board, the stiffness of the components, the dimensions of the component, and the thickness of the fall plate corresponded to higher out of plane stress. Out of plane stress decreased in inverse proportion to solder bump size, height, and number and in inverse proportion to the diameter of the impact cone. The authors observed that higher strain rates generally increase the toughness of ductile materials while inhibiting plastic deformation.

Wang *et al.* (2005) created a detailed finite element analysis that was used in conjunction with drop testing. While drop testing simulation has been adopted in industry, the physical test has not been replaced due to the difficulties of producing credible results. A key concern for the modelers was obtaining sufficient information about the materials and to address each step of the reliability assessment methodology thoroughly. Flip chip packages were tested; however, no failures resulted from physical testing. This illustrates one of the challenges of obtaining failure data for highly reliable electronic components with failures that are difficult to detect. Although the authors had originally aspired to use finite element modeling to simulate the entire sequence of events during the drop testing, the model was simplified to reduce errors.

Shetty *et al.* (2003) examined chip scale packages using finite element analysis to study the effects of three- and four- point bending. A double-sided printed circuit board was used in the physical testing, which employed a Mechanical Test System (MTS) machine. The testing revealed that packages located on the top side of the printed circuit board failed more quickly than their counterparts on the bottom for a given curvature. Based on these results, a finite element model was created to predict when failure due to bending would occur. This model relied on deformation energies using estimates for the average strain energies in the critical solder joints. The specific component was unnamed due to proprietary considerations.

2.3. Gaps in Existing Research

The current research does not encompass modeling of an array of different solders. A variety of geometries have not been modeled. It is currently necessary to

assess models using experiments performed on the same capacitor geometry. A rigorous assessment of models using different termination materials has not been performed, unlike their counterparts in physical experimentation. Modeling efforts must address the entire cool-down stage, including creep and bending. There may be useful information gained by modeling the capacitor from sintering to cracking. A model with a fine mesh may produce useful results for capacitors that do not have experimental data to use as a baseline. As noted, four-point bend data is different from three-point bend data and can be correlated through finite element analysis, but not all three-point bending studies have been repeated using four-point bending.

Chapter 3: Modeling of Stresses in Multi-Layered Ceramic Capacitors under Thermo-Mechanical Loading[4]

3.1. Introduction and Approach

3.1.1. Introduction

This Chapter describes research that was performed to gain insight into the performance of mounted electronic components subjected to thermo-mechanical loading. It summarizes the failure behavior associated with the mounted components that motivated this investigation. It then presents the finite element modeling approach to simulating these failures. Results from the model corresponded to those from physical testing.

Multi-layered ceramic capacitors (MLCCs) were chosen as the component of interest because of their ubiquity and because of their previously observed reliability problems (Maxwell, 1988). The type of failure that this research focused on is caused by single cycle bending of a printed circuit board that has a capacitor mounted to the surface of the board experiencing tension. It has been conjectured that this effect is caused by the cooling experienced by the system during manufacturing (Syfer Report, 2009). The capacitor geometry is believed to affect the location where the cracking occurs. The different material properties in the capacitor termination and solder used are believed to affect the cracking point (deWith, 1993). The research treated the

[4] Portions of this chapter have previously appeared in G. Sharon, D. Barker, "Crack Growth and Reliability Modeling of Multi-layer Capacitors in Microelectronics Applications," *Proc. SPIE Photonics West*, San Francisco, CA, Jan. 22-27, 2011.

cracking point as the point of failure. In the tested printed circuit boards, the strain on the board and the point of continuity loss were monitored. The strain on the side of the bent board experiencing tension was used to correlate the calculations from the simulation against the results from tested boards.

The original concern of manufacturers was that the stiffer solder used for lead free applications would cause more problems in capacitor cracking. The unexpected results from bending tests showed that the capacitors mounted with lead free solders performed better than ones mounted with lead free solder. The proposed explanation was that the higher solidification temperatures of lead-free solders together with the CTE mismatch between the board and capacitor were causing higher residual stresses in the capacitors. This research contributes to the understanding and quantification of this effect.

3.1.2. Stresses in the Capacitor Body During Cool-Down

Before the problem of bending can be addressed comprehensively, the history of the capacitor and the board needs to be taken into account (Franken *et al.*, 2000). The capacitor's ceramic body has already been subjected to multiple processes before the bending moment is applied. Each one of these processes may affect the capacitor in ways that may make it more or less resistant to cracking while the board is being bent. One of the processes necessary to track is the cool down from the solder melting temperature. MLCCs are attached to the copper pads using solder. It was assumed that there is no stress in the solder at its melting temperature. The electronic packaging system containing the MLCCs can be cooled to room temperature at various rates. During the temperature change, stresses will start to build up in the

system. Each material in the system has a different coefficient of thermal expansion (CTE) and the dominant cause of the stress is believed to be the CTE mismatch between the capacitor ceramic and the laminate material used for the printed circuit board (Lee, 2006). The stresses created in the capacitor body can be calculated for various materials and geometries.

As noted by Shin *et al.* (2007), there currently is no single method for directly measuring the stress or strain inside a capacitor. The metric that was used for determining the capacitor failure point in bending is the strain on the board surface. Strain gauges were used on the board and continuity was measured in the capacitors. During reflow and cooling, the stresses and strains had to be found analytically because strain measurements were not taken from the boards.

3.1.3. Effects of Geometry

There are several different facets of the capacitor cracking problem. Each capacitor manufacturer uses different shapes for their capacitors. Even the same manufacturer may use different geometries for capacitors with similar functionality. The board geometry can be assumed to remain constant. The copper pads on the board are rectangular in shape. The thickness of the copper pad is assumed constant, but the width and length can be designed with different values. Although the geometry of the copper pad affects the cracking, this factor is a problem in multiple dimensions that was partially analyzed. The solder profile varies from capacitor to capacitor but in specific cases it can be characterized as “starved” for solder profiles that have less material, “bulbous” for solder profiles that have more material and

"nominal" for profiles that are neither. The following figures depict the three different solder profiles considered.

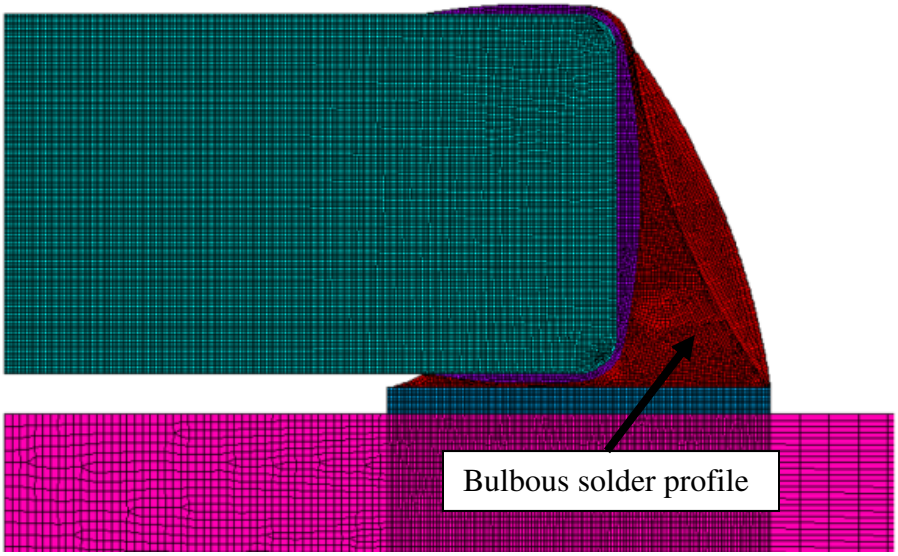


Figure 14. Solder geometry for a bulbous joint profile

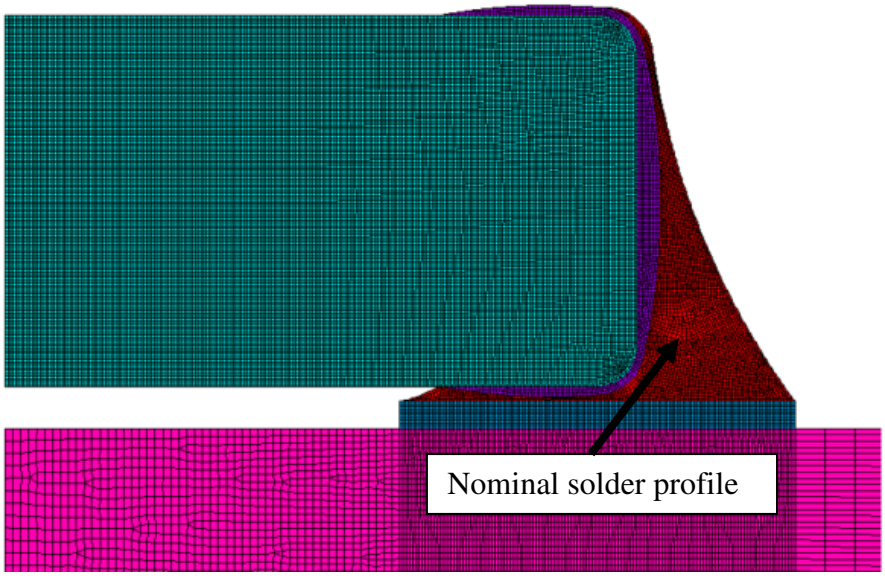


Figure 15. Solder geometry for a nominal joint profile

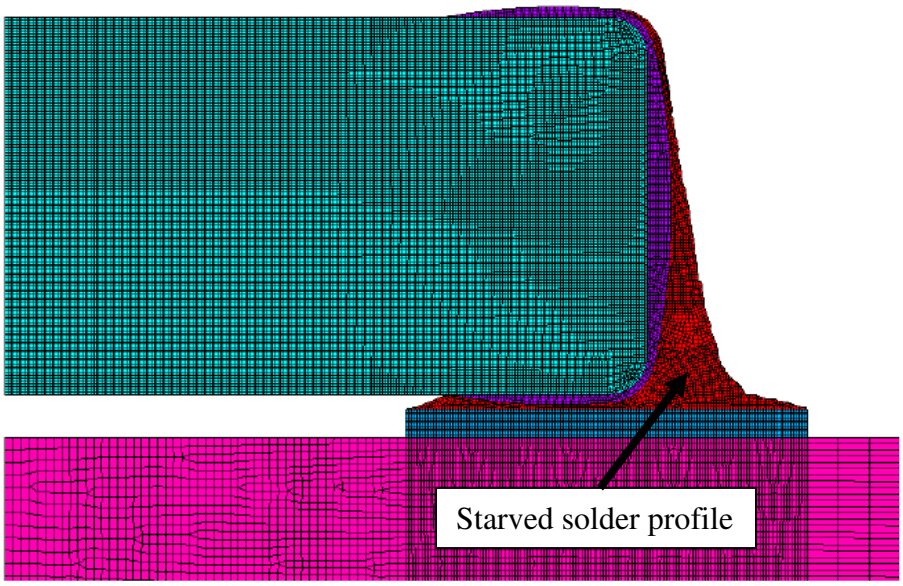


Figure 16. Solder geometry for a starved joint profile

Another factor that changes the solder geometry is the shape of the capacitor termination. Each capacitor model has a different shape for the termination of the capacitor; these shapes can be radically different. This research used capacitors that had the same termination profile for both flexible and standard termination.

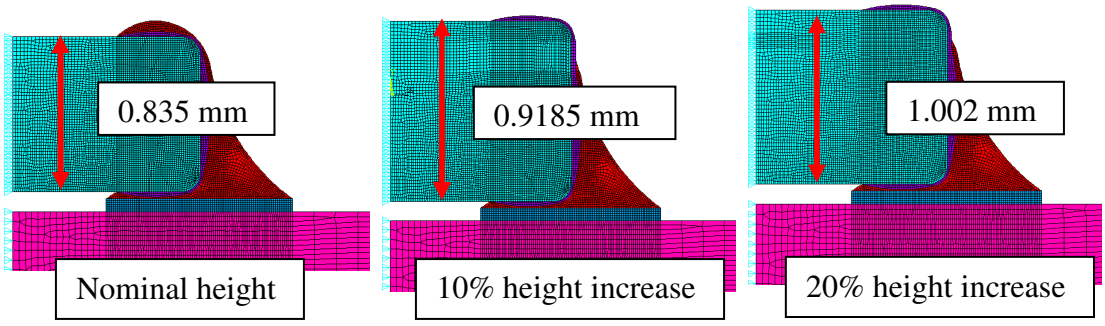


Figure 17. Capacitor geometries for different capacitor thicknesses

Capacitors are becoming increasingly miniaturized and different manufacturers have different shapes for their ceramic bodies. The design of electrodes varies between manufacturers and sizes and was not included in the scope

of this research. A design feature that was studied was the thickness of the capacitor as shown in Figure 17.

The capacitor thickness change represents a ten percent change in the volume of the ceramic body. Although the volume only changes by ten percent the stresses can rise by more than thirty percent. This effect is diminished with decreasing capacitor length. There are several more geometry effects that were explored and they are located in the appendices section of this dissertation. Modeling different geometries provides a wider understanding of factors affecting capacitor cracking in bending. This modeling also allowed the research to focus on the nominal cross sections to prove the existence of residual tresses from the reflow cycles.

3.1.4. Effects of Solder Material Properties.

The scope of this research encompasses eutectic tin-lead (SnPb) solder and a tin-silver-copper (SAC). There are several levels of complexity that were incorporated into the models. Both solders were studied with and without the effects of creep and plasticity. Both creep and plasticity play a role in the mechanical behavior of solders in the cases studied, unlike the rest of the materials in the system that have constant linear elastic properties in the loading conditions and geometries. The properties for both solders have been studied and are assumed as definite values. The model can be expanded to study different solder types with varying properties; however, this study was limited to available solders for which property information was available as shown in Table 2. The table shown here does not incorporate the creep properties used in subsequent modeling. A deeper discussion of creep material properties can be found in the creep modeling section of this dissertation.

Temperature [K]	273	295	320	350	505
SAC_EX [Pa]	5.3E+10	5.124E+10	4.924E+10	4.684E+10	3.484E+10
SAC_NUXY	0.3	0.3	0.3	0.3	0.3
SnPb_EX [Pa]	3.444E+10	3.110E+10	2.73E+10	2.274E+10	2.0E+10
SnPb_NUXY	0.35	0.35	0.35	0.35	0.35

Table 2. ANSYS inputs for the SAC and SnPb solder material properties

3.1.5. Effects of Termination Material Properties.

The purpose of the capacitor termination in the capacitor is to create an electrical connection between the electrodes to the copper trace on the board. The electrical connectivity between the board and the capacitor termination is accomplished using solder. This adds another functional constraint on the termination of having to provide a surface to which the solder can adhere. Standard capacitors use a metal for termination material. This metal in the loading conditions behaves in a linear elastic fashion. Newer flexible termination materials that are made from an epoxy with metal particles suspended in it provide the electrical connectivity to the electrodes. The flexible material is coated with a metal layer in order to provide a whetting surface for the solder.

In this study, the metal layer and the flexible material are examined as having a combined effect. The actual properties of the flexible termination are not known. The properties of the flexible termination require in-depth examination. The material has a high probability for yielding subjected to the loading conditions. It was assumed that the material had a yielding point and exhibited plastic behavior. The plastic behavior assumed in this research conformed to a bi-linear elasto-plastic stress strain curve.

3.2. Design of Finite Element Model

3.2.1. Modeling Methodology.

Because there is no way to measure strain directly on the capacitor surface during cool down from the solder melting temperature, this research took advantage of modeling techniques to construct an approximation of the internal behavior within the capacitor. The material properties for the board, capacitor body and copper pads were modeled as linear elastic; however, the termination and solder exhibited more complex behavior. The effects of creep were accounted for using the unified Anand model for plasticity and creep (Cheng *et al.*, 2000). For creep purposes, the temperature was maintained at 22 ºC for one week.

The temperature cooling profile used is varied from 0.6ºC/sec to 60ºC/sec whereas the cooling rates used by industry differ, but are often between approximately 1-6ºC/second (Swartz, 2010; BeRex Note, 2009; Sirenza Microdevices Note, 2004). The cool down rates are a processing condition that varies considerably across manufacturers. Intel's processing recommendations discuss manufacturers' usual preferences for keeping cooling rates below 3°C/sec (Intel Databook, 2007). Intel's recommendations note that solder joints with cooling rates of at least 1°C/sec are characterized by finer microstructure features and that studies have shown these rates are favorable for long-term reliability. Intel further observed that these cooling rates slow the growth of intermetallic compounds within the bulk solder.

	Temperatures	Cool down time at -1 ºC/sec
Lead-Free	219 ºC to 22 ºC	198 sec
SnPb Eutectic	183 ºC to22 ºC	162 sec

Table 3. Temperature profiles for cool-down of capacitor assembly

There were several factors that needed to be assessed analytically. The height of the capacitor body affects the stresses and needed to be quantified. The different capacitor height adds more material to resist the stresses that build up during bending over the same capacitor length. Because it was not possible to change the thickness of the capacitors during testing, this effect was studied analytically. A theoretical capacitor was modeled with a different height and subjected to the same board strain in bending.

The modeling addressed the shape of the termination, which was believed to have effects that warranted closer examination. Three different termination geometries were considered in this research, but more exist given the wide range of capacitors on the market. The major difference between the termination profiles is the tapering of the edges. The tapered edge gives the solder joint a different stress dissipation profile and appearance, and this tapering may have an effect on the behavior of the system in cool-down and bending.

The shape of the solder joint is naturally related to the amount of solder used to create it, but is also a factor of the geometries of the surfaces to which it is adhered. The solder will adhere to the surface of the capacitor termination and the copper pads on the board. If the geometries of the termination and pads are set, then the solder profile can be categorized according to the amount of solder in the joint. There were three solder profiles considered for the scope of the model. As discussed, the solder profile was categorized as “nominal” for the typical solder profile that is observed when using the exact amount of solder as designed by the manufacturer. The solder profile was considered “starved” or “bulbous” for profiles using less or more solder

respectively than the nominal amount. These different geometries can have an effect on the stress in the capacitor body at the crack initiation site while subjected to the board flexural strain that occurs during bending. The crack initiation site is different for thermal and flexural cracking, as shown in the following figures.

Figure 18. The crack initiation site for flex cracking

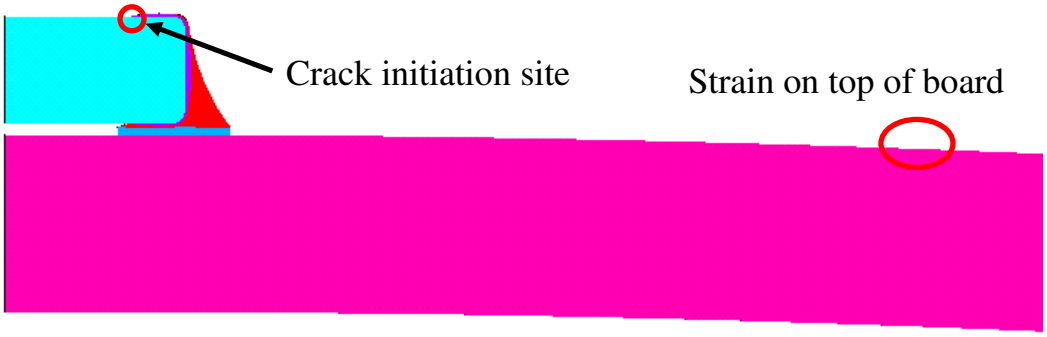


Figure 19. The crack initiation site for thermal cracking.

Thermal cracking was not modeled in this research but it is important to note that each load condition can change the location of crack initiation. The crack initiation site changes location as shown in the studies presented in the appendices. While the site will move slightly in one direction or another, the general location is at the bottom of the capacitor for bending. The crack initiation site can be used to examine failed specimens to determine if their failure mode is caused by bending or thermal cracking. While the crack profiles may look similar, the different initiation sites can indicate the underlying driver of the failure.

3.2.2. Modeling of Geometric Properties

There are several factors in the experimental procedure that cannot be changed readily and other factors that can be designed. The size and shape of the capacitors are determined by the manufacturers. The solder fillet is set by the amount of solder used. The copper pad size and capacitor orientation can be designed for maximum benefit for a particular application. In the analytical model, different variables were controlled in order to quantify the effects of several materials for individual parts of the capacitor system. To use a set geometry, it was efficient to choose a capacitor that had the same cross section for flexible termination material and the standard termination material. The material properties were set as constants in order to compare the effects of multiple geometries. These different geometries are shown in the following table.

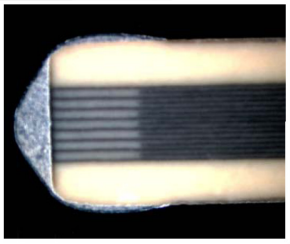
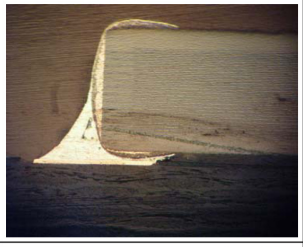
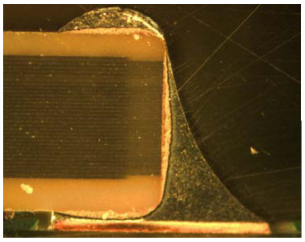
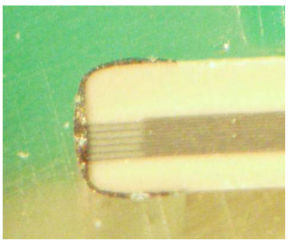
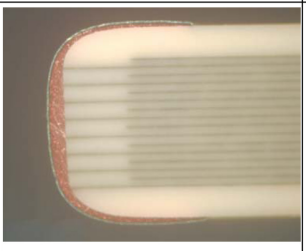
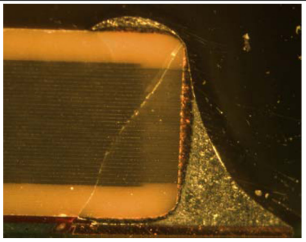
	SYFER 1812	AVX 1812	AVX 0805
Flex			
Standard			
	Same rounded body **Termination geometry is very different**	**Different thickness and corners in body** **Termination geometry is different**	**Same thickness and body** **Termination geometry is similar**

Table 4. Different geometries for capacitors with similar functions

Once the material properties are defined, the different geometries can be explored. One of the more interesting differences explored in this study was the difference in the capacitor body size as shown in Table 5 and Figure 20. The actual thickness in the capacitor was found to be different for capacitors of the same function even for the same manufacturer. Another factor that was considered was the effect of the size of the solder profile on the bending load.

Capacitor dimensions (mm)				
Size	**Length [L]**	**Width [W]**	**Termination width [B]**	**Min. separation [S]**
0603	1.60±0.15	0.80±0.15	0.35±0.15	0.70
0805	2.00±0.20	1.25±0.20	0.50±0.25	0.75
1206	3.20±0.20	1.60±0.20	0.50±0.25	N/A
Thicknesses [B] (mm)				
0603	0.08 with tolerance range of ±0.07 to ±0.15			
0805	Range: 0.06 to 1.25 with tolerance range of ±0.10 to ±0.20			
1206	Range: 0.78 to 1.70 with tolerance range of ±0.10 to ±0.20			

Table 5. Different capacitor dimensions

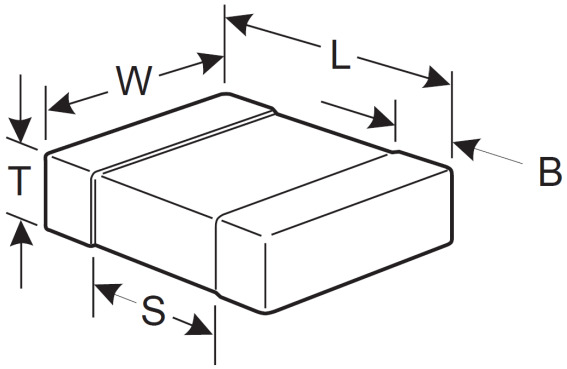


Figure 20. Sketch of capacitor dimensions

3.2.3. Modeling and Assessment of Material Properties

The properties of two materials were compared using the model to analyze known performance discrepancies. The Silver Filled Polymer (SFP) termination material has shown a decrease in cracks appearing in capacitors on boards loaded in

bending in comparison to the harder standard termination (Ellis, 2008; England, 2006). The actual material properties of the SFP were reverse engineered. A bilinear curve for stress and strain was used to model the SFP rather than a lower Young's modulus. The bi-linear curve is theoretical, but it can be used to reverse engineer a material that has a specific yield stress.

The lead free solder has shown a benefit in comparison to the less stiff tin-lead solder (Keimasi *et al.*, 2007). This is in conflict with respect to the results from the different terminations where less stiff materials exhibited preferable performance characteristics. This conflict can be resolved from the work done on the effect of cool down on residual stresses (den Toonder *et al.*, 2003). Both tin lead and lead free solders exhibit creep behavior (Ohguchi *et al.*, 2006; Wiese and Meusel, 2003). Tin-lead solder is more susceptible to creep than lead-free solder (Chinen and Siniawski, 2009; Limaye *et al.*, 2005).

The model was designed to address the total material behavior, including the effects of creep and plasticity. Theoretically, both solders will creep until a certain point where the material's resistance to deformation will effectively cause the material to cease deforming. At this point, the amount of stress in the solder and in the capacitor body will not decrease. This point is different for each solder material.

There are several ways of exploring materials using numerical techniques. The most basic way to model a material's behavior is to consider only the elastic modulus and Poisson's ratio with a coefficient of thermal expansion. This method may be insufficient for some problems. In the case of ceramic capacitor cracking, the two items that need to be considered with particular attention are the solders and the

flexible termination. To calculate the effect of changing materials, the rest of the factors must be set. The cross-section used for the analysis was the AVX 0805 capacitor, which had a similar geometry for flexible and standard terminations and tin-lead and lead-free solders. The finite element mesh had to be fine enough to capture the details in geometry, especially around the area of crack initiation in the capacitor body. The following figure shows the chosen geometry cross-section.

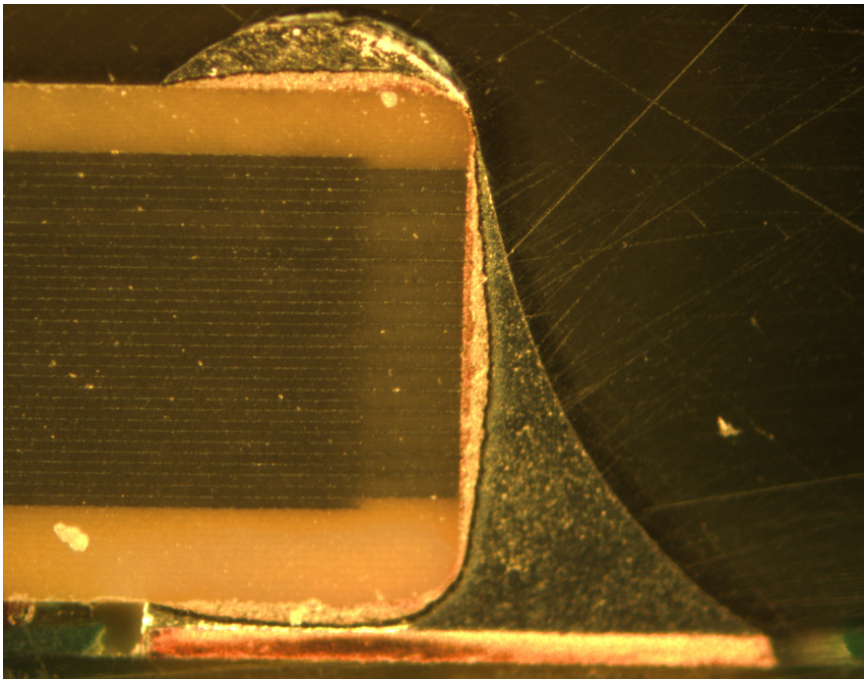


Figure 21. The AVX 0805 geometry used for modeling

It is impossible to eliminate all sources of error when using the finite element method for analysis. One of the techniques that can be followed to mitigate errors is to try to achieve the highest fidelity to the actual geometry as possible. Real capacitors in experimental conditions have a variability built in to the geometry (Prume *et al.*, 2002). Every capacitor is slightly different and there may be small variations in mounting. It is possible to build many different models to try capturing the subtle differences in geometry (Lee and Kim, 1997). The approach taken in this

study was to build a single geometry that is considered nominal and then to calibrate the model using the average experimental values. The experiments that were used in the comparison possessed a statistically significant sample size.

The mesh density or element size used in this case is set by the termination thickness. The termination thickness is the smallest geometry length in the model. In order for a model to be effective in a complex system, the number of elements across a given geometry should be sufficiently large (Li *et al.*, 2008). In this model, there are locations where the termination tapers off and the mesh is only one or two elements across. There is a tradeoff between the element count and mesh density that is also the same tradeoff between the mesh density and the solution time. The following figure shows the mesh used in the material property study.

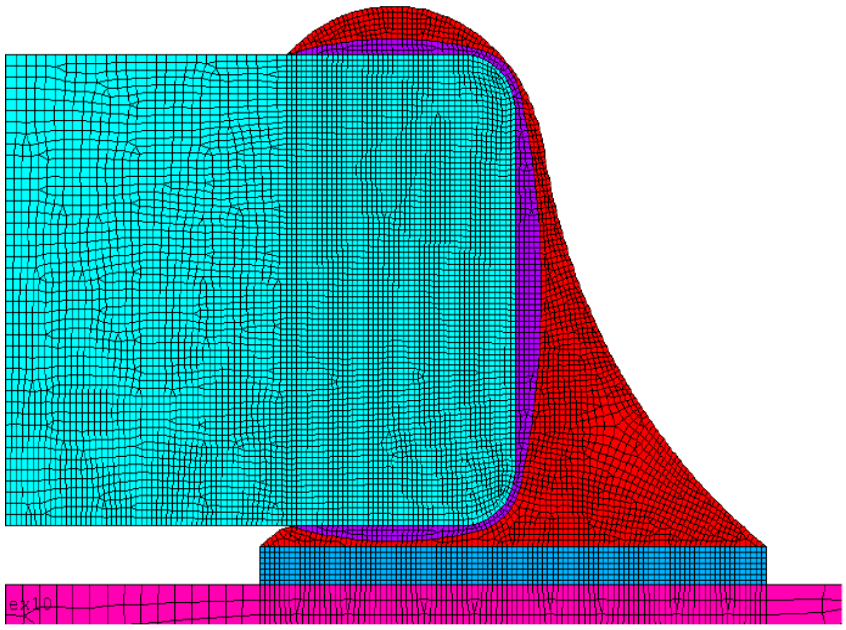


Figure 22. Finite element mesh of the 0805 AVX capacitor

Once the geometry is set, the material properties can be varied. There are two solders considered in this analysis. The properties for the two solders can be studied at various levels. The board, if given a bending moment to a certain strain, can be

modeled with the solder treated as a linear elastic material with no plastic deformation. This can produce a baseline for comparison between the two solders or another solder that might be studied in the future.

The thermal loads are also studied using a plasticity model for the solder with an approximation of material behavior (Cheng *et al.*, 1994). The same analysis is performed using a unified model for plasticity and creep using the Anand relationship (Darveaux and Banerji, 1992). The Anand property inputs used within ANSYS are shown in Table 7. It is also possible to use the same Ramberg-Osgood model for plasticity with a Garofalo model for creep, but this was not performed using this modeling scheme (Ohguchi *et al.*, 2006).

$$\frac{d\varepsilon}{dt} = C_1 [\sinh(C_2 \sigma)]^{C_3} \exp\left(\frac{-C_4}{T(^o K)}\right) \qquad \text{(Eq 3.1)}$$

Garofalo	C1	C2	C3	C4
SnAgCu	441000	5.0E-09	4.2	5412
SnPb	339	6.3E-08	3.3	6360

Table 6. Garofalo properties found for solders (Used with equation 3.1)

Anand	SAC	SnPb
s0	5.0000E+07	5.6330E+07
Q/R	8.4000E+03	1.0830E+04
A	4.6100E+06	1.4900E+07
xi	3.8000E-02	1.1000E+01
m	1.6200E-01	3.0300E-01
ho	3.0900E+09	2.6408E+09
s(hat)	1.0400E+06	8.0420E+07
n	4.6000E-03	2.3100E-02
a	1.5600E+00	1.3400E+00

Table 7. Anand properties found for the solders

The study of the capacitor cool down stresses and stresses caused by bending indicates that the beneficial effects of the cool down include mitigating the formation of cracks in bending, thereby improving overall capacitor reliability. The most advantageous time is directly after the system reaches room temperature because the solder begins to creep. As discussed, when the board surface is in compression, the bottom of the capacitor is likewise in compression, while the top in tension for cool down. When the board surface is in tension, the capacitor bottom in tension and the top is in compression. The stress in the capacitor is essentially akin to bending on the capacitor.

3.3. Test and Simulation Results

3.3.1. Coefficient of Thermal Expansion Mismatch

The disparity in the Coefficients of Thermal Expansion (i.e., the CTE mismatch) between the board and ceramic material imparted stresses in the capacitor assembly. The CTE values are listed in Table 8. The higher reflow temperature of the lead-free solder created a higher residual stress. The residual stresses had the opposite effect as in capacitor bending. At room temperature, the stress in the capacitor at the end of cool down is compressive on the bottom and tensile on the top. When bending is applied to the board, the capacitor is stressed with tension largely on the bottom.

Material	Coefficient of Thermal Expansion (ppm/°C)
FR4 board	15-20
Copper pad	17.6
Eutectic tin-lead solder	24.7
SAC solder	22.4
Capacitor termination	17.6
X7R dielectric	9

Table 8. Coefficients of thermal expansion used in modeling

3.3.2. Finite Element Modeling Results

As noted, the model assumed a one-week creep period to compare the residual stresses in capacitors mounted using lead-free solders to those using tin-lead solder. It was expected that most of the relaxation would occur in the first time intervals. It was further anticipated that in each case the solder would relax to a certain residual stress value and remain there (Darveaux and Banerji, 1992). While it is possible to have materials that continue to creep even at room temperature until all the stresses are relieved, subsequent creeping in excess of one week was not considered for the two solders used.

The numerical simulation used the same program with the same two dimensional model used for the regular bending problem; however, in this instance, the creep models were added for the lead-free and tin-lead solders. In regular single cycle flex cracking, it was assumed that the process was fast enough such that creep would not have sufficient time to produce significant effects. It was further assumed in regular bending that the creep mechanism would not be very effective for solders at room temperature. This simulation sought to capture the residual stresses and the bending stresses in combination. In order to meet this objective, a bending load was

applied to the board immediately after cooling the system from reflow temperature to room temperature. The truncated results from the simulation can be seen in Figure 23.

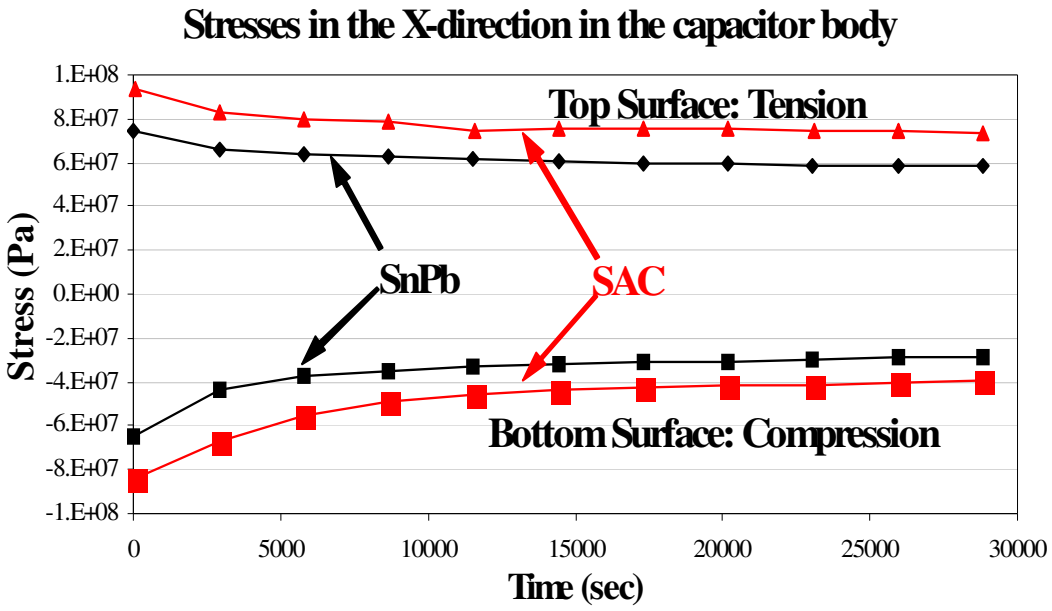


Figure 23. Creep residual stresses for lead-free and tin-lead solders

Figure 23 shows a plot of the stresses present in the ceramic after cool down from solidification temperature in the first eight hours. Only the first eight hours are plotted here because after eight hours and up to one week the stresses were steady. The simulations for the lead-free and tin-lead solders were identical except for the different material properties and different solidification temperatures of each solder. The solidification temperatures were 220°C for lead-free solder and 183°C for tin-lead solder. It can be seen that the lead-free solder had more compressive stresses throughout the process. The difference in material properties and processing temperatures between the solders has been theorized to affect the stresses in the

ceramic. For some time, researchers have identified the need to create numerical models to explore this theory.

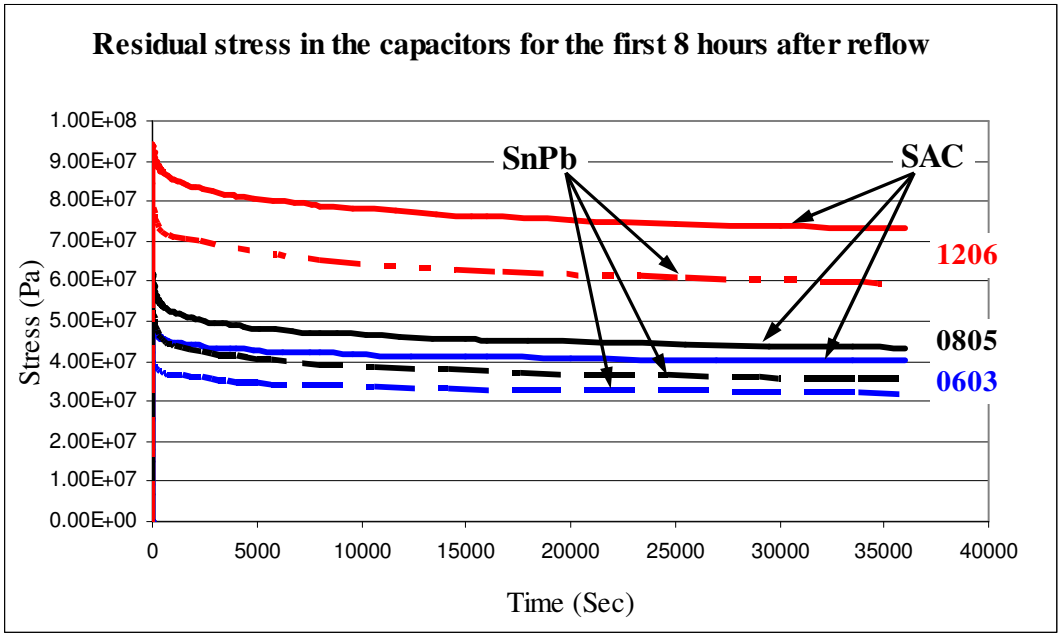


Figure 24. Effect of capacitor size on residual stresses

After finding the residual stresses due to lead-free and tin-lead solder more models were solved in order to find the effect of different capacitor lengths. Figure 24 shows that the smaller capacitors are affected less than the larger capacitors. This figure only shows the effect of 1206, 0805 and 0603 capacitors and a extracting a trend from only three points is not recommended. In all three capacitor lengths, the higher solidification temperature associated with lead-free solder yields higher residual stresses.

The residual stresses in the capacitor body caused in cool down are not permanent; once the solder begins to creep, these compressive stresses become smaller (Jiang *et al.*, 2007; Nakano *et al.*, 2003). This observation suggests that the best time to bend the board and take full advantage of the residual stresses is as soon

as is feasible in a testing environment. Even when the material is allowed to creep for a week, some residual stresses in the system remain (Shin *et al.*, 2005). Theoretically, there exists a stress that will not be relieved at room temperature even at an infinite time.

The following section is a discussion of the methodology used to reverse engineer the material properties of the silver filled polymer. The two dimensional axis-symmetric model used in this analysis is shown in Figure 28. The "flex" capacitors use a layer of silver filled polymer inside the termination to relieve the stresses from the capacitor ceramic body. It was necessary to find the material properties of this layer in order to be able to proceed with the simulations. It is common to employ a multi-linear stress strain inputs when modeling elasto-plastic materials. It is also possible to approximate this complex multi-linear behavior with a bi-linear curve as shown in Figure 25 and Figure 26. In Figure 25, the only parameter to consider is the modulus of elasticity. This figure shows how the modulus of elasticity changes the yield strain. A similar change in yield strain can be achieved using different yield stress values as shown in Figure 26. Both methods are valid and there are others as well. In this case the second method presented here was chosen.

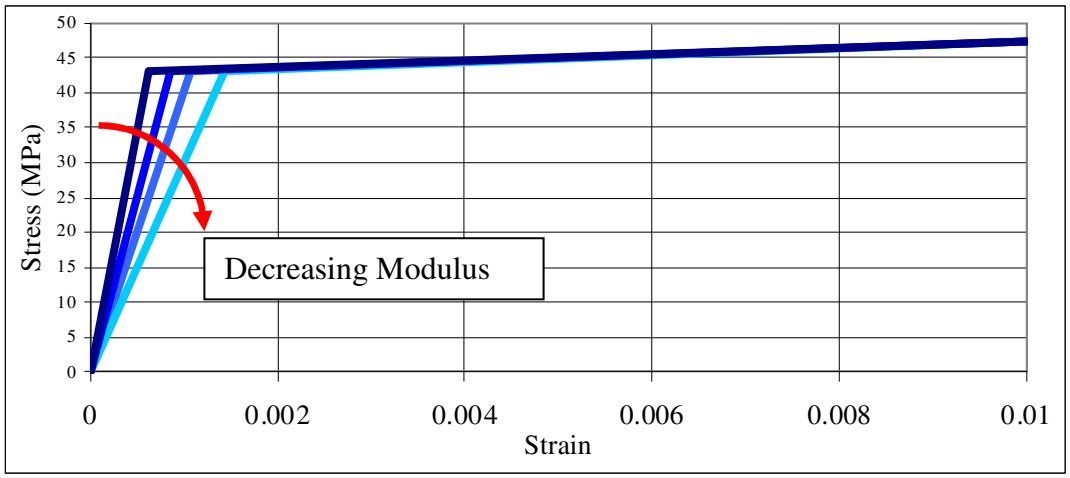


Figure 25. Bi-linear stress strain profile with varying modulus

The following figure shows a bi-linear stress profile that is more consistent with polymer materials. The yield stress is lowered until the desired model result is found. In the investigations by Keimasi and Azarian (2007), it was found that capacitors exhibited a reduction of stress of a factor of two between the flex termination and standard termination where the flex termination stress was the lower one. The board was loaded in bending to a certain strain and the stress at the capacitor area of interest is measured and the different curves are input as the material property. Once a singular yield stress is found for the material, a smoother line can be calculated. The singular value of yield stress can be used to describe the entire curve.

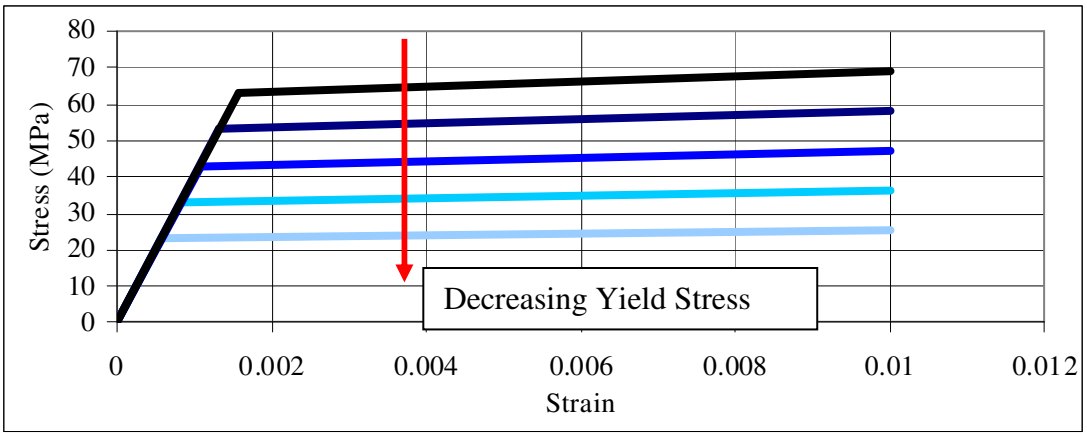


Figure 26. Bi-linear stress strain profile with varying yield strengths

It is necessary to compare this value to other results found in literature or direct measurement. Direct measurements were attempted by using a nano- indenter but the thin profile and small size of the silver filled polymer made it too difficult to get a consistent reading. A comparison to the literature shown in Chapter 1 confirmed that a value of 31 MPa was close to what can be expected of a polymer with embedded metal particles.

From the reaction forces shown in the following figure, it can be seen that the neutral axis of bending for the capacitor mounted on the board gets shifted down. This shift in neutral axis shows that the capacitor is bearing less stress.

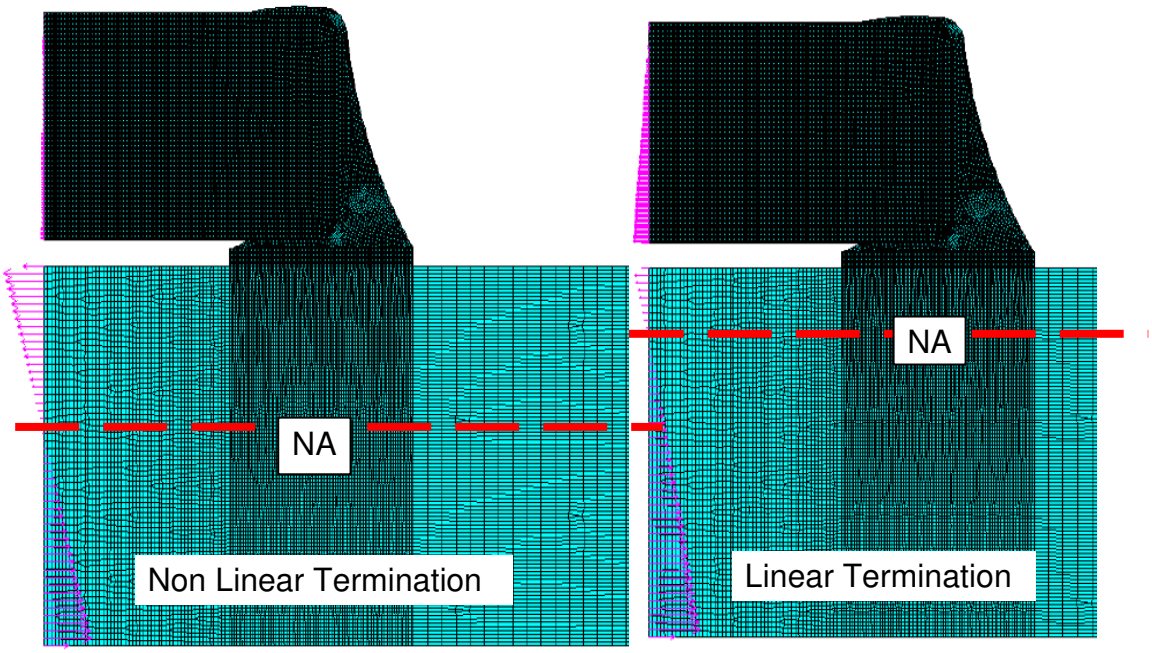


Figure 27. Shift in neutral axis as change in termination material properties

A finite element model was used to explore the effects of the Silver-Filled Polymer (SFP) termination material. This model is illustrated in Figure 28. The 'flex cap' termination, made of SFP, is known to have different properties than regular metallization. In order to find a numerical model for this property, performing nano-indentation on the inner material was attempted without much success. The thin profile of the SFP layer coupled with the metal finish caused difficulty in accessing a good area for direct measurement.

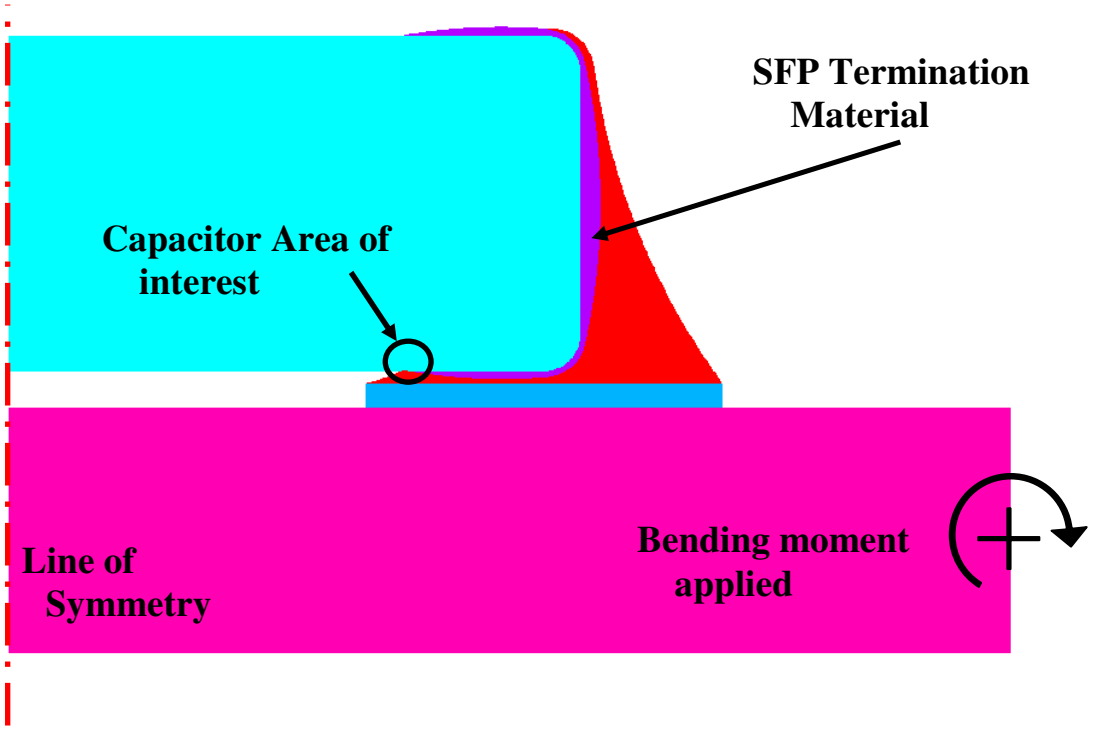


Figure 28. FEA model to determine silver-filled polymer termination material

A different method was needed to find a theoretical material property. A bi-linear stress versus strain curve was used as a theoretical model for a material that yielded at a specific stress. This assumption helped in the next phase together with using experimental values from four point bend testing. From the research performed at CALCE (Keimasi, Azarian, *et al*., 2007) it was determined that for a specific capacitor profile, the flex termination had twice the reduction of stress in the crack initiation area compared to regular termination, as shown in Figure 29.

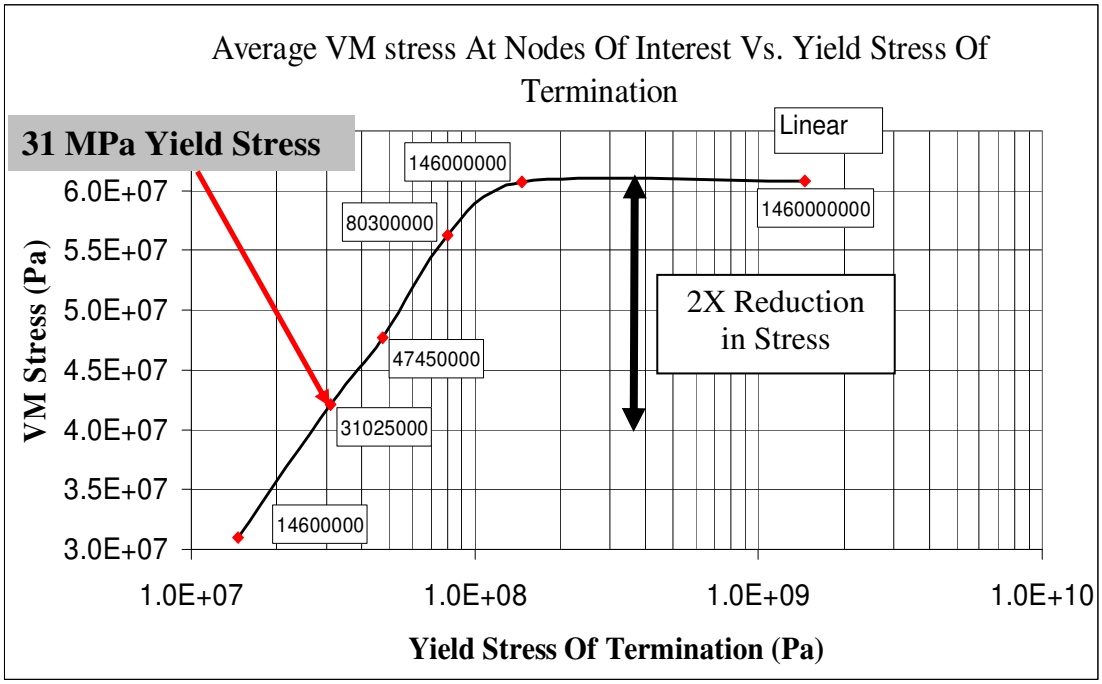


Figure 29. Stress reduction observed for SFP termination

The four point bending applied to the board caused a strain on the top of the board and flex cracks to contribute to the failure of the capacitors. The strain was measured on the board and the appearance of flex cracks was determined with in situ continuity measurements. The measured values were incorporated into the numerical simulation. The only variable was the yield stress in the bi-linear curve. The stress in the capacitor area of interest for different yield stresses was extracted, as shown in Figure 29. From the stress values, it was determined that the SFP flexible termination would yield at approximately 31 MPa.

3.4. Discussion

3.4.1 Observations

This modeling confirmed the results of the analytical studies that have been completed to date that considered the effects of differing geometries. The thickness

of the capacitor reduces the calculated values for the probability of cracks appearing in the capacitor due to board bending. This result can partially explain the better performance of capacitors using a silver filled polymer (SFP) termination. For some manufacturers' products, the difference in termination material is not the only change between capacitors of the same function. If that was not the case, then the higher performance found in testing could easily be attributed only to the termination material. This is one of the reasons why it is important to compare capacitors with the same geometry. The benefits of having a thicker capacitor may seem evident when simple stress strain relationships are explored. For the same amount of loading caused by the solder joint, there is more material and a larger area that is subjected to the load. This relationship is non-linear because most of the effect is experienced on the area closer to the copper pad.

The solder profile has been found to have little effect on the stresses in the capacitor body at the site of crack initiation. The same capacitor was modeled with three different solder profiles with everything else set as constant. The resulting stresses were not significant enough to consider the size of the solder joint as a major factor in capacitor cracking subjected to board bending. This model was a good candidate for consideration because the simulated capacitor shape closely reflected the actual shape of the capacitor body rather than a simplified, geometric conceptualization. The actual effect of the solder profile was not anticipated to be drastic, but it was treated as one of the factors that may affect the variability in capacitor cracking. Another geometrical factor was observed from the experimental results and was not analytically calculated: the capacitor's length to width ratio.

Ceramic capacitors are available in a wide range of length to width ratios and total surface area; while miniaturization efforts continue, their footprints on the board are becoming even smaller and compact.

For a single chosen geometry, it was possible to change the material properties in order to model the different construction materials in the capacitor assembly. The two materials that were examined were the solder and the termination. The printed circuit board, the copper pads and the capacitor body were assumed to be linear-elastic with thermal expansion for the type of loads in the problem. In keeping with prior studies, the silver filled polymer termination material performed better than standard metal layer termination, while the lead-free solder exhibited greater resistance than tin-lead solder. This is counter intuitive in that the SFP termination is more flexible than the standard termination and it would make sense that it would yield rather than break the ceramic material.

The lead-free solder was stiffer than the tin-lead solder and it is unsurprising that the less stiff material (the tin-lead) would have a greater resistance. The solder reflow temperature is a major contributor to these results. Previous studies corroborate the creep resistance observations. Chinen and Siniawski (2009) discuss research showing that lead-free solders exhibited greater creep resistance than eutectic tin lead solder at higher temperatures. The lead-free solder performed more poorly than the tin-lead solder when comparing inelastic strain energy density. Lower creep strain rates combined with higher lead-free stress rates led to higher hysteresis loops that dissipated a greater amount of energy in each cycle.

3.4.2. Summary

Stresses were observed in the capacitor body during the entire cool down cycle for lead-free solder and tin-lead solder with standard terminations. The difference in CTEs between the board and ceramic material led to residual stresses in the ceramic that work against the bending load. The cracks that appeared in capacitors during board bending initiated at the bottom of the capacitor when the capacitor was mounted to the board surface that is in tension and initiated at the top for capacitors mounted to the surface of the board that in compression. The stresses that appeared in the body of the capacitor from the cooling process remain locked in the system.

Factor	Range Studied	Recommendations
Capacitor Thickness	10% and 20% increase in volume	Thicker capacitors are preferable
Solder fillet profile	Bulbous, nominal and starved profiles	No effect found in bending
Solder material	Tin-lead and lead-free	Lead-free is better for bending, especially for longer capacitors
Termination material	Standard and flex termination	Flex termination is better by a factor of 2

Table 9. Summary of effects studied and recommendations

Table 9 presents a summary of the results discussed in this chapter. The benefits of using flexible terminations include allowing increased strains on the board compared to standard termination. The theoretical thicker capacitors perform significantly better even for a ten percent increase in volume. The normal variations in solder fillet profile have no clear effect on the appearance of cracks. Using solders that solidify at high temperatures cause the appearance of residual stresses that are beneficial in flex cracking.

The modeling effort discussed in this Chapter enabled an examination of the relationship between the residual stresses and the bending stresses. The model partially relied on previously developed construction techniques and methodologies, some of which are also described in Chapters 4 and 5. Chapter 4 discusses a similar modeling strategy used for a simpler system where only two materials were considered in a symmetric model. It shares common elements with the methodology applied to the flex cracking simulation, which employed natural geometries, published material properties, and model elements both new and previously developed.

Chapter 4: Finite Element Modeling of the Effects of Material Properties and Thermal Cycling on Ductile Failure for PCBs[5]

4.1. Approach

4.1.1. Introduction

This Chapter describes the development of an axi-symmetric, two dimensional finite element model that simulated the three-dimensional phenomenon of damage to electroplated copper plated through holes on printed circuit boards. This model represents a concentrated effort to model the behavior of a PCB damaging a plated through hole above the glass transition temperature. The non-linear properties of board laminates were found using thermo mechanical analysis in collaboration between CALCE and Sun Microsystems.[6] This study explored the effect of the reflow process on barrel failures in plated through holes.

The reliability of plated through holes is worsened by thicker boards being processed at higher temperatures while their aspect ratios are decreasing. It has become apparent that there is a need to quantify the amount of damage in the plated through hole during the reflow cycles because the temperature exceeds the glass transition temperature (Tg) of the board. The copper plated through hole model

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[5] Portions of this chapter appear in G. Sharon, D. Barker, "Modeling of Plated Through Hole Reliability and Performance," *Multidiscipline Modeling in Materials and Structures Journal*, accepted for publication, to appear in Vol. 7, No. 3 (2011). The findings were presented in conference paper form in G. Sharon, D. Barker, "Reliability Modeling to Enable Damage Assessments for Plated Through Holes," *43rd International Symposium on Micoelectronics (IMAPS 2010)*, Raleigh, NC, Oct. 31 - Nov. 4, 2010.

[6] The author acknowledges with gratitude the efforts of Michael Freda of Sun Microsystems.

illustrated hysteresis in plated through holes using the physical hole geometry and material properties for the copper and board laminate. The finite element model was constructed using a method that incorporated a damage fatigue assessment, non-linear material properties, and symmetrical geometries. The damage fatigue model permitted the estimation of accumulated damage to a plated through hole under the thermal cycling it would experience during the assembly process.

The reliability of plated through holes, also called "through vias," has a direct effect on the aggregate calculation of board-level reliability because they are incorporated into the printed circuit boards before any components are soldered to the board. Predictions of printed circuit board reliability have been found to differ greatly from observed field behavior (Jones and Hayes, 1999). The reliability of plated through holes is critical because it is infeasible to replace them upon failure. A failure may result in the entire board being scrapped or discarded. One of the failure modes for plated through holes results from thermal cycles due to a mismatch between the Coefficients of Thermal Expansion (CTE) of the copper and the board laminate. Various materials are used for the boards, each of which has its own thermal properties, including CTE. A board may undergo several reflow cycles before it is installed in a system and begins regular use. A reliability model must account for the damage in the plated through hole prior to normal operation in order to be both accurate and thorough. Figure 30 illustrates types of failure modes, with the copper material shown in grey and the laminate material in white.

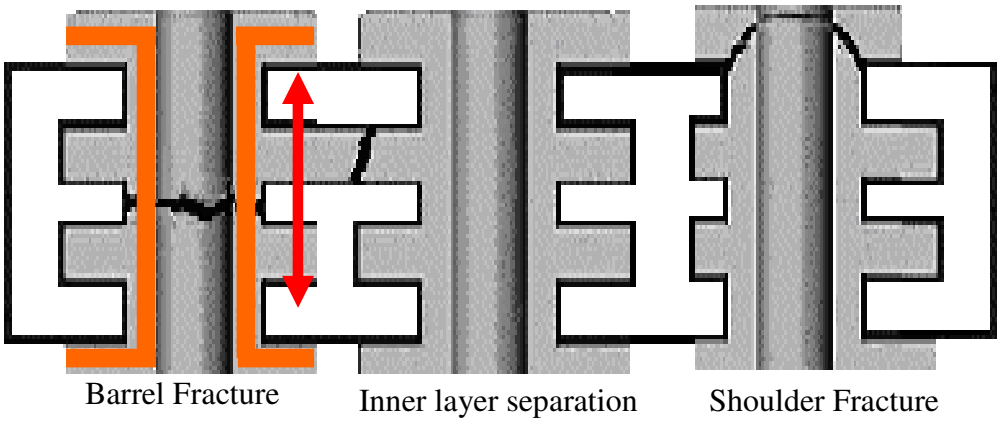

Figure 30. PTH failures: barrel fracture; inner layer separation; shoulder fracture (from left to right)

Each plated through hole has distinct reliability characteristics even on the same board. Variations in geometries, board materials, and load cycles necessitate a separate reliability calculation for each plated through hole on the board. Attempts to produce a comprehensive reliability assessment of plated through holes confront several mechanical issues that are best explored analytically, such as stress and strain measurements inside the copper plating itself. Additionally, the characteristics of plated through holes vary widely depending on the intended application of the boards to which they are incorporated. The difference in barrel lengths and specific geometry may make a specific through hole more susceptible to a given type of failure. The copper metallization can have several thicknesses, lengths, radii, and flange sizes. On a board of a given thickness, there may be different barrel lengths as shown in Figure 31. The arrows show the different via lengths, while the grey color shows the multiple layers of the PCB with white representing copper layers and vias.

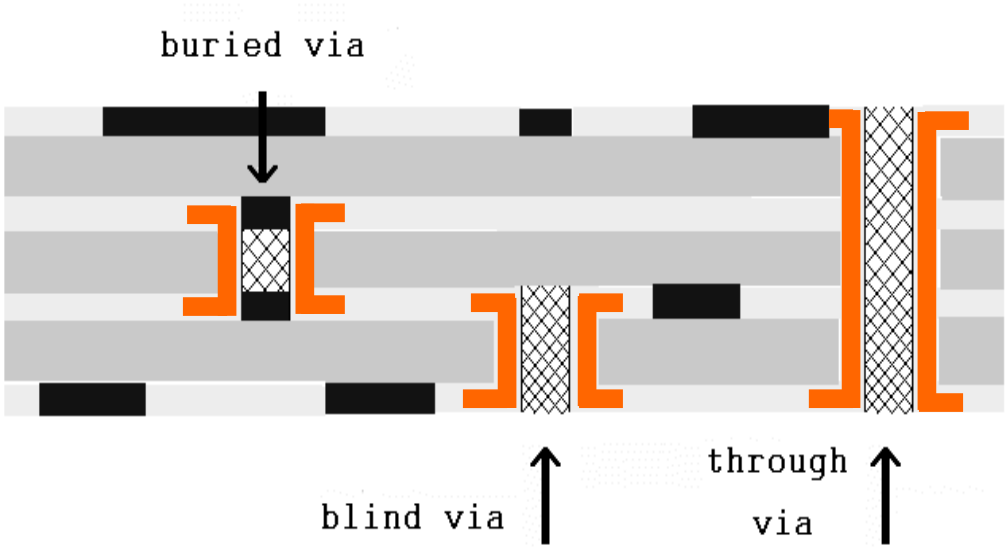

Figure 31. Different barrel lengths of vias on the same board

A high degree of variability exists in the temperature of the board during both assembly and subsequent use over its lifecycle. The reflow process heats the entire board assembly to the same temperature (230°C for lead-free solder and 183°C for tin-lead solder), and each plated through hole is exposed to the same temperature cycle. In regular use, the board will experience different temperatures and mechanical stresses at different locations. The assumption that the board starts with no damage to any of its components — and the inference that such damage need not be addressed in a reliability model — therefore holds true only if each component has not undergone mechanical work during the process of assembly.

Similarly, the assumption that all the components on a board experience the same conditions while in regular use is reasonable if global conditions, rather than localized ones, affect the board (Smetana and Ogle, 2006). Most applications will not have global loading; rather, they will be subjected to source loading such as clamps, resistive heating, and base excitation. During the assembly, and even after the hole

has been plated, there are several processes that may potentially weaken the plating and impair functionality. In these cases, the reliability model needs to account for the entire chain of possible failures.

The plated through holes considered in this study were made of copper (Cu). The correlation between stress and temperature is represented by an inverse power law model because copper is a ductile metal (Shigley and Mischke, 1989). For materials governed by an inverse power law relationship, plots of log-life versus log-stress can be generated. The correlation of interest was the stress versus the temperature of the laminate material. The inverse power law relationship for the copper is:

$$L(V) = \frac{1}{KV^{n}} \qquad \text{(Eq. 4.1)}$$

Following a log-log transformation, Equation 4.1 can be rewritten in the following format:

$$Ln[L(V)] = (-nLn \times V) + (Ln \times K) \qquad \text{(Eq. 4.2)}$$

Where: L is $N_{50\%,}$ the mean life of a plated through hole
K is a model parameter to be determined
n is a model parameter to be determined, and
V is the stress on the plated through hole in MPa.

The use of this plot can aid in testing in less time while obtaining accurate results for an analysis of component life. Once a credible stress versus temperature curve has been obtained, the testing can be reduced to focus on the testing at the low and high temperature extremes. Using this data, an S-N curve for cycles to failure can be generated. This in turn allows for the prediction of plated through hole life over varying temperature ranges.

A finite element model was constructed to predict plated through hole life; it was compared against thermal cycling data that was obtained through physical testing. As part of a collaborative research effort between Sun Microsystems and CALCE, extensive testing and analysis occurred that enabled access to material property data. This testing had produced a sizeable database for temperature and stress data across multiple temperature points. Much of this data was obtained using techniques such as Interconnect Stress Testing (IST). The test methodology that was used for the IST data is described in the Addendum. The analysis methods that were developed for the model could also be applied for other thermal cycling methods.

The finite element model was used to simulate the thermal cycling. It incorporated material properties for the copper and laminate that were readily available and those obtained from the IST efforts. The objective was to quantify the damage in plated through holes subjected to temperatures that were higher than the board's Tg.

4.1.2. Specimen Selection and Modeling Decisions

Several assumptions were made that applied to both the physical experimentation and to the finite element simulation of damage accumulating in plated through holes. For thermo-mechanical analysis along the Z-axis, the preferred sample was from an actual printed circuit board fabrication because the thermal expansion rate and the strain experienced by the plated through hole is a function of the actual cross section of the printed circuit board fabrication. A greater amount of copper in the stack-up reduces the effective CTE because the CTE of copper is lower than the Z-axis CTE of the laminate materials. It was therefore deemed preferable to

use a representative cross section that included the copper and was from the board fabrication being tested. For dynamic mechanical analysis for the expansion rate along the Z-axis, data was obtained from pure laminate samples.

Because the expansion rate of copper has been studied extensively, laminate material data was obtained and subsequently adjusted for the percentage of copper composition in a given stack-up. An accurate value for the expansion rate for the printed circuit board fabrication could then be calculated. In considering values for the material modulus, it was decided to use samples that were pure laminate without copper, in contrast to the thermo-mechanical analysis of the expansion rate that used representative samples containing both laminate and copper. The exclusion of copper was necessary because the laminate materials possess a lower modulus than copper. A decision was made to select samples that were representative of the percentage of resin and the type of glass that would be used in the actual printed circuit board fabrication in order to preserve the fidelity of the model.

4.2. Properties of the Laminate Material and the Plated Through Hole

4.2.1. Material Properties for the Laminate

Two types of laminate were modeled. Laminate A was a non-dicyandiamide (also referred to as 'non-dicy') cured epoxy and glass construction with filler added to lower the CTE along the Z-axis. Laminate A has been used in lead-free testing of printed circuit boards up to 4 mm in thickness. Laminate B is a non-epoxy resin and glass system was a candidate for use in lead-free board fabrications with a thickness in excess of 4 mm. The mechanical properties of Laminates A and B are listed in Table 10. The low expansion percentages of 2.03% and 1.85% at 245°C for

Laminates A and B, respectively, are notable because the majority of epoxy-glass laminates have an expansion percent between 2.5% to 3.5% at 245°C. The modulus of Laminate A significantly exceeds that of Laminate B. The higher modulus results in higher stress due to the incremental stress being the product of strain and the modulus, where the strain occurs because of thermal expansion. Values for Tg using thermo-mechanical analysis and dynamic mechanical analysis were obtained from Sun's data.

Property	Laminate A	Laminate B	Units
Z-axis CTE < T_g	45	50	ppm/°C
Z-axis CTE > T_g	200	180	ppm/°C
T_g -Thermal Mechanical Analysis (supplied)	170	180	°C
Calculated Expansion at 245°C	2.03	1.85	%
Storage Modulus < T_g	18,000-15,000	7,350-6,600	MPa
Storage Modulus > T_g	2,500	1,500	MPa
T_g - Dynamic Mechanical Analysis (supplied)	162	170	°C

Table 10. Mechanical properties of the laminate material

4.2.2. Plated Through Hole Geometry

Two geometries were considered in the finite element of the plated through holes. One geometry featured a board laminate of 3 mm thickness and the other featured a thickness of 6 mm. The drill diameter of the plated through hole was 50 µm thicker for the 6 mm thick laminate. These geometries are listed in Table 11.

Laminate Thickness (mm)	PTH Drill Diameter (µm)	Copper Barrel Plating Thickness (µm)
3	350	30
6	400	30

Table 11. Plated through holes geometries

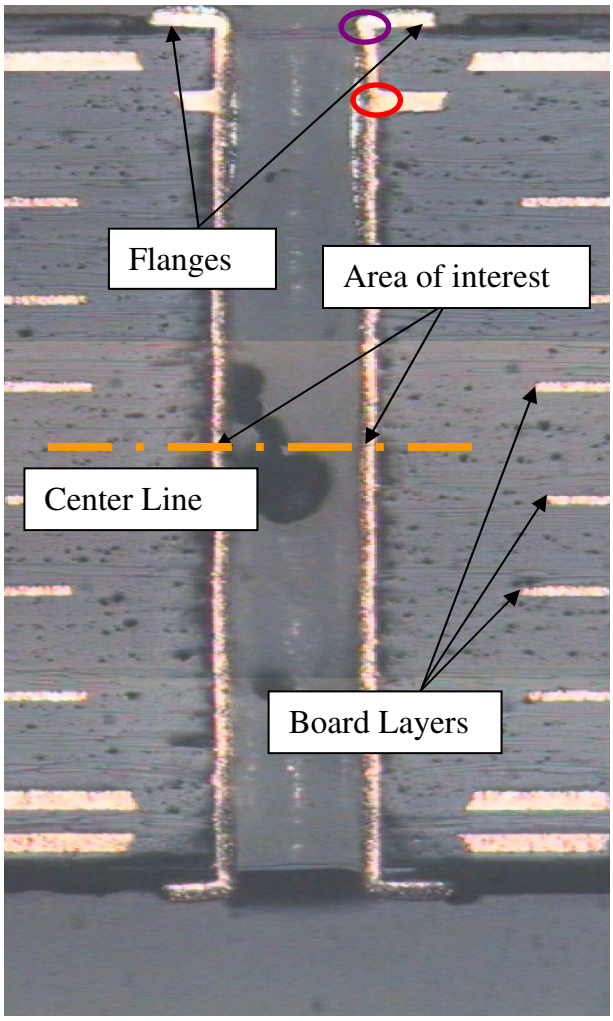

Figure 32. Cross section of long barreled PTH showing several board layers

A representative geometry for a plated through holes is shown above in Figure 32. This cross section image was taken of a multi layered board with the copper layers visible in orange. The through via is empty in the middle and the board material is shown in grey on either side. This plated through hole goes through the entire board, so the barrel length equals the board thickness. The flanges are electroplated with the barrel, but the layer interconnects are built into the board. After manufacturing the whole board with all the layers, the hole is drilled and the copper is plated to create the connection with the layers. There is a difference in the

mechanical connection strength between the flange and the barrel (purple) and the layer interconnect and the barrel (red). The geometrical relationships between the plated through hole and the board were key inputs to the model.

4.3. Finite Element Model Development

4.3.1. Creation of a Model to Predict Failure in Plated Through Holes

As observed by Freda and Barker (2006), unprocessed test data can be used with different modeling approaches to obtain approximate life estimates for plated through holes. A non-linear finite element simulation incorporating the temperature dependent properties of the laminate was developed to calculate the stress and strain within the PTH copper barrel. The ANSYS finite element analysis software package was used for these simulations. The finite element model enabled a comparison of different PTH geometries and laminates with different mechanical properties. The model relied on the ductile nature of copper to predict its fatigue life, which is directly correlated to the strain it experiences. The finite element model enabled a comparison of multiple thermal cycles that occurred below, during, and above the laminate glass transition region.

A convenient method for exploring the work done on plated through holes in reflow cycles is to concentrate on a specific type of failure and to plot the hysteresis curve at the area of interest. Barrel fracture failures were studied in this preliminary investigation. Barrel fractures occur in the copper material along the hoop and cause disconnects from one side of the board to another. The barrel is pulled by the flanges as the board is expanding. Shoulder fractures, in contrast, are the fracture and disconnect of the flange from the barrel. They are caused in an area of geometric

singularity because the drilling process leaves a sharp edge in the laminate where the copper is electroplated. Inner layer disconnects may occur between the layer copper and plated copper, which have slightly different material properties and are not bonded as tightly to each other as to themselves. Inner layer disconnects are affected by the varying loads on the board. These types of failures have been amply documented (Barker and Dasgupta, 1993; Furlong and Freda, 2004).

The mathematical model developed treated this configuration as symmetric and two-dimensional, as discussed below. The maximum effect of the mechanical work was assumed to occur in the center of the barrel exactly at the midpoint of the PCB thickness due to the symmetrical nature of the geometry used in the calculations. These assumptions were made in order to concentrate on the expansion of the board and the stress in the copper alone.

4.3.2. Axi-symmetric Model Geometry for the PTHs

The plated through holes were modeled as axi-symmetric finite elements. The models were constructed to correspond to the samples described in Section 4.1.2. Some parameters was obtained from the IST data or taken from a PCB of nominal thickness. Previous work has examined the lifetimes of plated through holes using finite element methods, as discussed in the Addendum. These studies have indicated that accurate estimations could be obtained without accounting for slight asymmetries and without including a complete treatment of orthotropic properties for the laminate material (Barker and Dasgupta, 1993).

The axi-symmetric model can be conceptualized as a cross-section of the plated through hole spun around its vertical centerline. The axi-symmetric model is

an approximation of a true three-dimensional model in that it uses only the radial r–axis dimension and the out of plane Z-axis. The displacements in the circumferential or θ direction are zero. The axi-symmetric model can also be visualized as a plated through hole in a circular section of the board laminate.

4.3.3. Construction of the Finite Element Mesh

The mesh of the finite element model used five 8-noded quadrilateral elements through the thickness of the laminate and the copper. It was necessary to be particularly methodical to obtain a sufficient number of elements in both the radial axis and z-axis directions such that the mesh element aspect ratio would not be overly large. Subsequent calibrations of the mesh were performed to check that the mesh possessed adequate density to enable simulation of the behavior of the copper barrel to provide meaningful detail.

The plated through hole was modeled as if it were a single hole in an infinite laminate board. Returning to the visualization of the axi-symmetric model as a plated through hole in a round section of a board, the cylindrical section of laminate material was on the order of 6 plated through drill-hole diameters in size. The outer wall of the cylinder of laminate material was constrained to move as a plane by connecting the outer nodes to move together in the radial direction. This modeling constraint was made to reflect findings from previous studies, which have suggested that plated through holes are grouped in array structures, the plated through holes that are the closest neighbors to each other slightly reduce the stress and strain in each hole by working collectively to inhibit expansion of the laminate in the z-direction (Barker and Dasgupta, 1993). Because of the beneficial effects of being located in proximity

to other plated through holes, the worst-case scenario in terms of stress and strain with all other variables held constant would be an isolated plated through hole.

4.3.4. Modeling the Elastic-Plastic Materials of Copper

The copper in the finite element model was a temperature independent ductile elastic-plastic material that could be described by a Ramberg-Osgood constitutive equation (Barker and Dasgupta, 1993):

$$\varepsilon = \frac{\sigma}{E} + \left(\frac{\sigma}{K}\right)^{1/n} \qquad \text{(Eq. 4.3)}$$

Where:

K=0.631 GPa, a Ramberg-Osgood parameter
n=0.15, a Ramberg-Osgood parameter
σ = von Mises stress
ε = effective (von Mises) strain, and
E=120 GPa, the elastic modulus.

The printed circuit board laminate materials were modeled as elastic materials possessing a temperature dependent elastic modulus, E, and a temperature dependent CTE. The Poisson ratio for copper was 0.35 and the copper's CTE remained 17 ppm/°C. The inner plane copper layers of the board were neglected so that the laminate could be modeled as a homogenous material. This simplification was justifiable in that the temperature dependent properties that had been found from Sun's dynamic and thermal mechanical analysis testing were extracted from laminate structures that included copper trace layers.

4.4. Results

4.4.1. Results from Reflow Cycles

The lead-free solders to which manufacturers are currently turning are processed at higher temperatures than tin-lead solders. A commonly used range for tin-lead solder during reflow processing is 208ºC – 235ºC, whereas a typical recommended peak temperature range for SAC solder is 242ºC – 262ºC (Houston *et al.*, 2003). A representative reflow cycle is shown in Figure 33, reaching a peak temperature of 230ºC. In this profile, there is a cool-down to room temperature from the maximum temperature of 6ºC/sec.

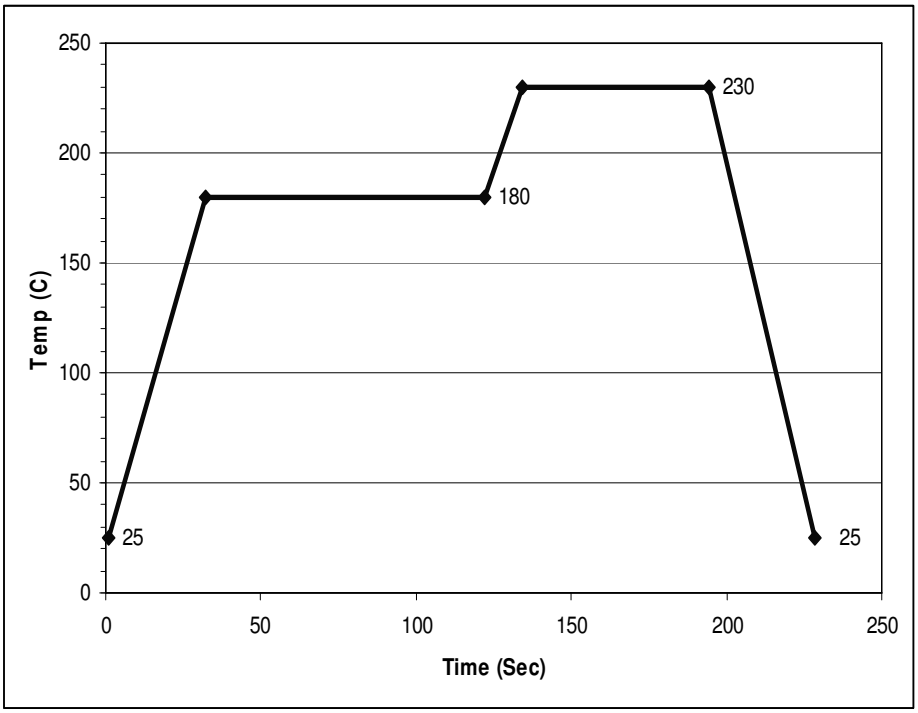

Figure 33. Solder reflow temperature profile

These high temperatures not only increase the amount of expansion in the board, as expected, but also change the board properties themselves. In some laminate materials, the CTE changes as the temperature increases (Vecchio and

Hertzberg, 1986). Figure 34 portrays the results found using TMA and Figure 35 displays the CTE of the board material used for the purpose of this analysis.

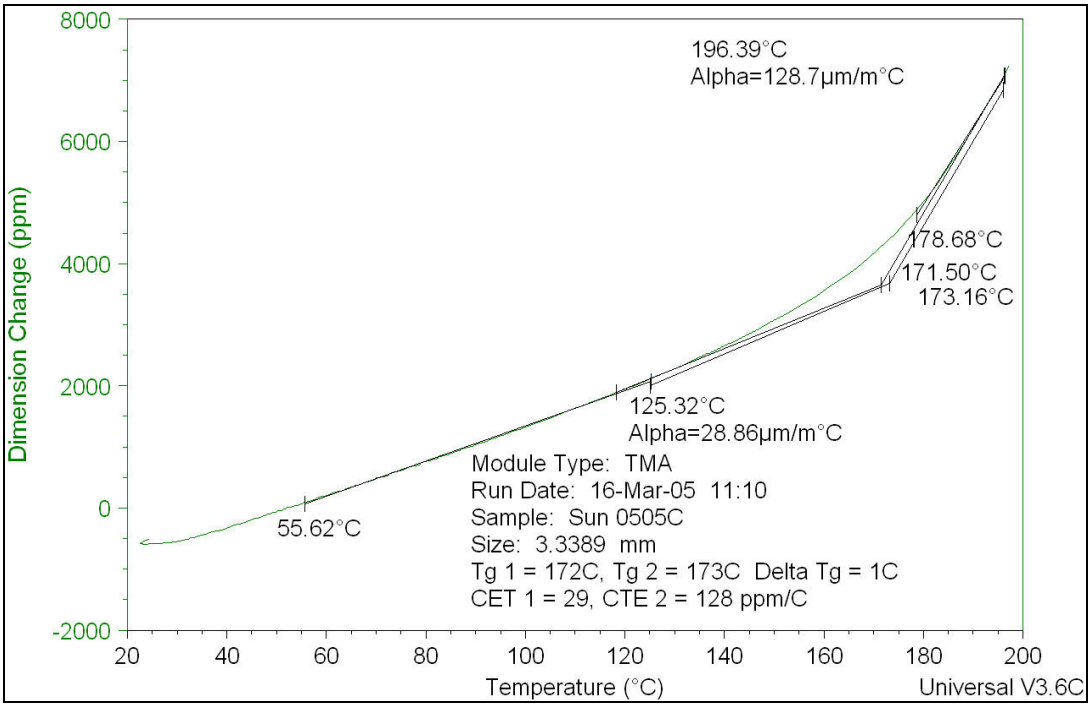

Figure 34. TMA plot of Z-axis expansion versus temperature for board (Freda, Barker 2006)

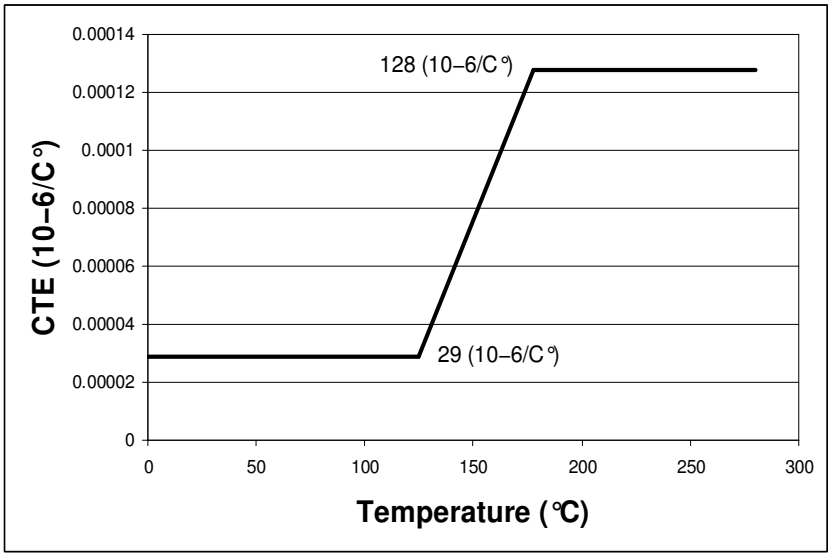

Figure 35. Coefficient of thermal expansion of the PCB

At approximately 150ºC, the CTE increased from 29 to 128 (10^{-6}/ ºC), which were the values used in this analysis. These values were derived from the direct testing previously performed on a batch of boards (Freda and Barker, 2006). Subsequent analyses using different boards necessitate that these values be obtained for each type of board. These properties are important to determine because the CTE mismatch is a key mechanical load as a result of the temperature change (Vandevelde *et al*., 2007).

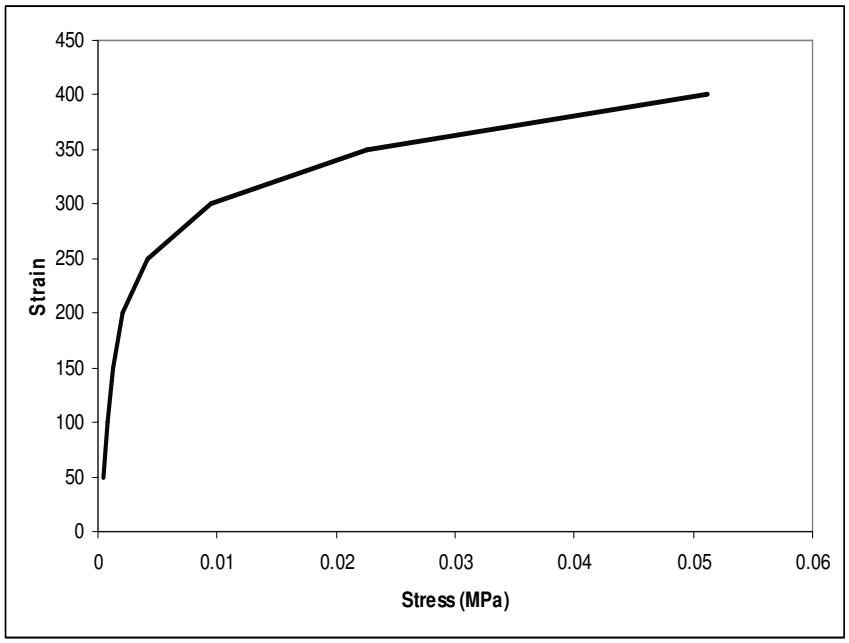

Figure 36. Stress-strain curve for Cu

Board expansion contributes to a 'stretching' of the copper material. Figure 36 shows the stress-strain curve used in the analysis and illustrates both elastic and plastic behavior. The plastic region in the material is used for modeling of hysteresis. Once the reflow temperature profile, the CTE properties of the laminate, and the plasticity in the copper were accounted for, a generalized hysteresis curve was estimated using a finite element model. Three cycles of reflow were solved and plotted in a smoothed curve, as shown in Figure 37. As expected for the three plotted

cycles, the first cycle had the greatest effect on the extent of mechanical work because it imparted the initial load. Each subsequent load cycle followed roughly the same curve. It was therefore inferred that an increased number of cycles corresponded to more work being done on the copper material and to more damage accumulating.

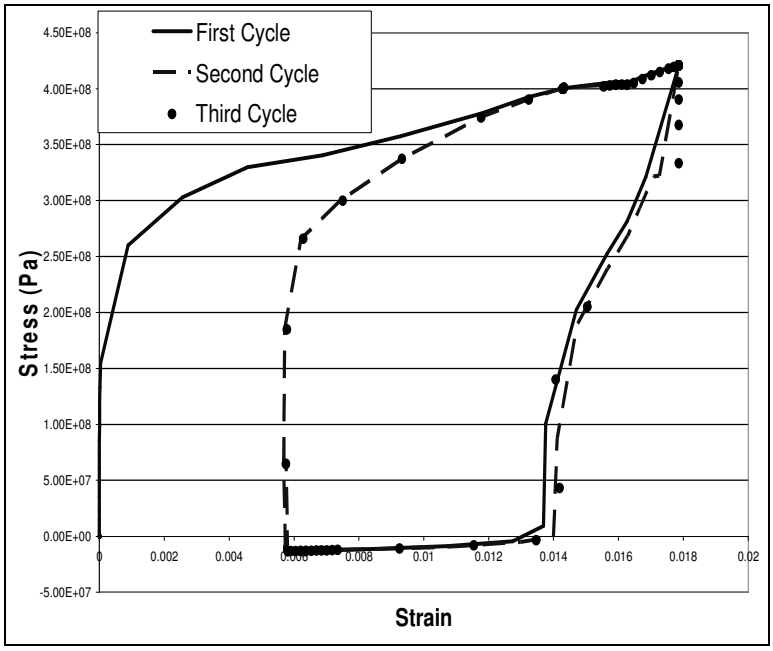

Figure 37. Effective hysteresis loops for the first three reflow cycles.

This model was representative of what any embedded copper plated through holes may potentially be subjected to, whether it is electroplated or deposited. Because it has been shown that through holes made of copper will have intermittent failures in some instances, it may be reasoned that these through holes will reconnect when the temperature is decreased (Freda, 2004). The analysis showed that it is inadvisable to assume simply that a plated through hole has no damage when it begins regular operation, especially at elevated temperatures. The model showed that the center line region of the laminate board corresponded to the maximum strain range in

the copper barrel. This location for the maximum strain range correlated to the location of barrel cracks that were observed in Sun's cross sections of failed samples.

4.4.2. Two-Dimensional ANSYS Model for the Plated Through Hole

The model was solved using the ANSYS package solver with the inputs directly processed through a batch file. Each element was defined by four points. Each element had a total of eight nodes, four at the corners and four bisecting the edges. The geometry was measured using the cross section shown in Figure 32 without the layer interconnects. The element definition in ANSYS is a '2-D 8-Node Structural Solid,' also referred to as PLANE82 inside the program. The elements of this analysis were rectangular. Each element had a predefined material associated with it that was entered separately and varied for the sensitivity analysis. All the elements are connected to one another by shared nodes with a "no slip" condition. It was expected that the interface lines would have some discontinuity in the stress because the deflections were the same on both sides, each with a different modulus. The element outputs were calculated at every one of the eight nodes. The outputs needed were stress and strain. The deflection magnitudes were calculated automatically within ANSYS and could be used to display the motion that occurs with the change in temperature. The temperature dependent properties for the laminate were entered into a lookup table within the ANSYS model.

The finite element model was solved using a non-linear analysis with one hundred sub-steps between each temperature change. The final cool-down to room temperature from reflow temperature employed two hundred sub-steps. When additional reflow cycles were modeled, the hysteresis loops continued to overlap.

Three cycles were modeled in order to correspond to a standard number of cycles that a board may experience.

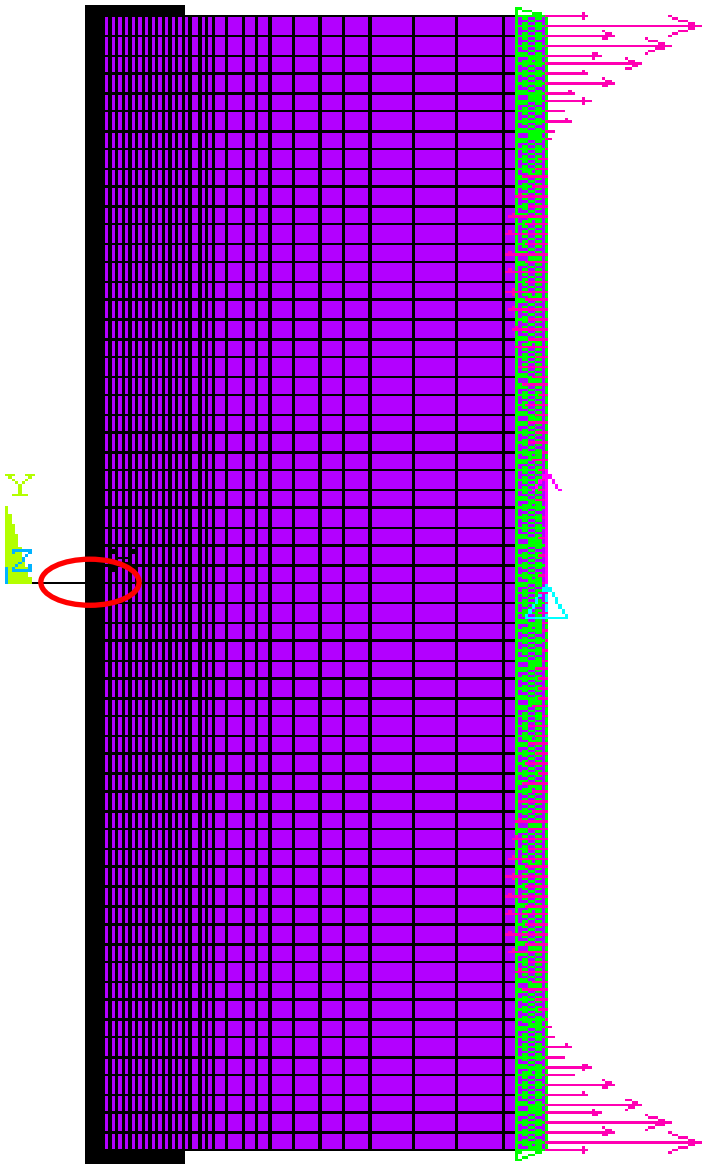

Figure 38. 2-dimensional finite element model depicting the area of interest The PCB is shown in purple and the copper is shown in black. The area of interest is identified in the middle of the PTH with an ellipse mark.

The maximum strain ranges for the copper barrel for various temperature cycles are shown in Table 12 for boards with a thickness of 3 mm. The maximum temperatures listed in Table 12 corresponded to the different thermal cycles.

Maximum Temperature	Plastic Strain Range (%)	Total Strain Range (%)
275°C	2.554	2.739
255°C	2.296	2.505
245°C	2.193	2.399
235°C	2.091	2.304
215°C	1.916	2.114
200°C	1.819	2.025
170°C	1.342	1.540
150°C	0.401	0.604
135°C	0.043	0.221
120°C	0.000	0.101

Table 12. Maximum strain range for copper barrel during thermal cycling (results for a 3-mm thick board made of Laminate A)

4.5. Discussion

The modeling effort for the ductile failure of copper plated through holes showed that a three-dimensional problem could be translated into a two-dimensional axi-symmetric finite element model. This concept was critical for the numerical modeling of the capacitor cracking problem presented in Chapter 3. This analysis showed that it may be unwise to assume that a plated through hole has not experienced damage when it begins regular operation, especially at elevated temperatures. Because the board assembly process imposes mechanical work on plated through holes, the assumption that they exist in an undamaged state at the start of regular use needs to be modified. The amount of damage already undergone by the board should be calculated depending on its unique history to improve the accuracy of reliability assessments. The total damage to the plated through hole before it begins regular operation depends on the specific history of the board. As expected, the first reflow cycle caused the greatest amount of damage and the largest initial plastic deformation. Every subsequent reflow cycle subjected the copper to

additional damage. This analysis was enabled by developing a model of a two dimensional, axi-symmetric multiple layer board with a plated through hole geometry that runs from one side of the board to the other.

The determining factor in a reliability analysis may a small component that is hard to find and a failure that is difficult to see (Feldman *et al.*, 2009; Snugovsky *et al*., 2008). Plated through holes are integral to printed circuit boards and are difficult to monitor once they are manufactured. As noted, the consequences of lowered reliability due to via failure are significant. An entire board may need to be replaced due to the vias failing. It can become extremely expensive to replace a board due to via failure, especially in critical reliability systems. There are substantial ramifications for cost effectiveness and even product liability, including the development of warranties that are predicated on accurate product reliability assessments. Despite these challenges, it is helpful that the effect of the reflow cycles on the plated through hole can be calculated in order to improve estimates of the likelihood of an eventual barrel fracture. Such estimates can be used to modify the reliability model for the overall board. In multi-layered boards, an inner layer separation failure also needs to be addressed.

Each system manufacturer should assess the importance of including the plated through hole in its reliability assumptions. Neglecting the damage worsens the understanding of system reliability. While overdesign of plated through holes to prevent the damage may seem desirable, it would most likely be infeasible to change the manufacturing process or the process by which the plated through hole is connected to the inner layers. As board design becomes more tightly integrated, the

complexity of identifying and modeling on-board component failures increases. It is important to monitor and record seemingly isolated instances of failures because they may indicate the need to modify the materials and components on a particular board.

The model presented here incorporated multi-linear elasto-plastic material properties for copper and temperature dependent CTE for the board material properties. The results of modeling the material properties above the glass transition temperature were used to correlate the damage in the copper to the PTH reliability database and to the IPL/lognormal estimates presented by Sun Microsystems in 2007. This study represents a step towards understanding the reliability of plated through holes with boards that exhibit non-linear properties.

The next section investigates the theory that the strain rate independent behavior of Single Crystal Silicon (SCSi) can be used to quantify the defects introduced into MEMS structures during manufacture. By using finite element models it was possible to show that the brittle failures in MEMS structures can be predicted. The study also shows that the numerical simulation can be used to quantify the amount of defects present in the SCSi after manufacture. This is the third project that modeled the physics of failure of an electronic component to understand the drivers of failure mechanisms using finite element techniques.

Chapter 5: Model for Dynamic Fracture Response in Mounted Small Profile Components[7]

5.1. Introduction

5.1.1. Objectives

This chapter discusses the brittle failure of a micro-electro-mechanical system (MEMS) subjected dynamic or shock load. The models and test were used to explore the theory that the strain rate independent behavior of Single Crystal Silicon (SCSi) can be used to quantify the defects introduced into MEMS structures during manufacture. In this study a MEMS device was subjected to a measured dynamic load in a shock impulse. This acceleration was used in a linear elastic finite element model as a global gravity load applied slowly. The SCSi exhibited brittle fracture behavior and linear-elastic properties.

Creating an accurate model for the strength of materials is a small but important part of the many steps involved in making a credible assessment of the reliability of MEMS structures. The SCSi model was constructed as part of an effort to create a simple, inexpensive test methodology that would use the fracture strength of a MEMS device to predict its reliability, and to evaluate this method through experimentation. As with other electronic packaging systems, simulation-assisted reliability assessment is an important tool in the design and development of MEMS

[7] The study is described in G. Sharon, R. Oberc, D. Barker, "Reliability Testing of MEMS Accelerometers Using Dynamic Stress Response," *International Journal of Structural Integrity*, accepted for publication, 2011.

devices. The knowledge gained from this assessment, which plays a critical role in the virtual qualification of MEMS devices, may lower design costs and reduce the need for time-intensive testing (Zhang, 2003). Assessment of MEMS subjected to dynamic loading requires an understanding of the effect of loading and mechanical properties on the primary failure modes. In this study, physical test data was gathered and used to compare results from a finite element model that was used to predict brittle failure.

5.1.2. Background

SCSi is a building block for many MEMS devices (Yi and Kim, 1999). Its dynamic failure mode is brittle fracture and typically occurs when surface flaws are present. Such flaws are a function of both processing techniques and device feature size (Namazu *et al.*, 2000). The fracture strength of silicon is not only influenced by the presence of these surface flaws but also its crystal plane orientation (Chen *et al.*, 2000). Considerable research has been performed in order to identify the quasi-static fracture strength of micro fabricated silicon structures, yet there continues to be wide variability in the fracture strength data (Suwito *et al.*, 1999; Yi *et al.*, 2000).

Kozhushko *et al.* (2007) and others have identified the dynamic fracture strength of SCSi wafers containing intrinsic flaws. However, the data regarding fracture strength for microfabricated SCSi is limited (Meroni and Mazza, 2003). This data is necessary to determine the influence of processing techniques and device feature size on dynamic fracture strength. Previous research has indicated that fracture strength varies considerably with processing parameters (Chen *et al.*, 2002).

Additionally, the process of deep reactive ion etching (DRIE) has been shown to affect the fracture strength of SCSi (Yi and Kim, 1999).

5.2. Selection of Test Specimen for Brittle Failure Assessment

The device selected as the test subject was a MEMS accelerometer made of SCSI. The compact form factor, accuracy, and low cost of MEMS accelerometers invite many different applications. For example, MEMS devices have been widely adopted in air bag deployment systems (Walraven, 2003). The medical industry has turned to MEMS in surgical devices and medical products to lower risks and improve functionality (Rebello, 2004). Not only are these devices critical to safety, they must function for long periods and in a wide range of operational conditions. Similarly, portable microelectronic devices, such as handheld gaming tablets and mobile telephones, have incorporated MEMS accelerometers for several functions. These applications require different form factors; unlike airbags, they are not critical safety components and there may be no need for redundancy of devices. MEMS component reliability thus plays a role in the overall device reliability and performance for an array of products.

As with standard accelerometers, MEMS accelerometers require a mass and spring for the mechanical function and an electrical sensor to translate the mechanical movement to an electric signal. MEMS accelerometers offer an inexpensive means of measuring vibrations (Albarbar *et al*., 2008). The difference in inertial forces between the mass and the base due to the latter's acceleration can be measured; however, most accelerometers can only measure acceleration in a certain direction. Using two or three mutually perpendicular accelerometers permits the measurement

of acceleration in all three axes. Several MEMS manufacturers have designed a variety of accelerometers, in part due to their relative simplicity of design and the simplicity of the loading and the material properties of SCSi. This simplicity is also beneficial to reduce model complexity and the time intensiveness of the simulation.

As noted, an efficient test technique and a trustworthy numerical model using ANSYS for brittle failure were sought. Numerical analysis for MEMS devices made of SCSi is possible because the properties of Si have been characterized at the micro level, with material models corroborated by experiments (Yi and Kim, 1999). The availability of material property data substantially aids the finite element analysis process. The material used in this investigation was processed using DRIE.

5.3. Testing and Simulation

5.3.1. Finite Element Model of SCSi Under Single Cycle Acceleration

ANSYS software was used to model the MEMS structures subjected to single cycle acceleration. The model used three-dimensional twenty node brick elements with linear elastic properties for the material. A mesh convergence study was performed to determine that the mesh density was sufficient to capture the resulting stresses in the cantilever beam. A global inertial load was applied to the model. The theoretical density of silicon was used in conjunction with the three dimensional volume to model an inertial load. Because silicon in single crystal structures cracks in a brittle fashion, an analysis was performed to find what global inertial load was necessary to cause the maximum stress in the model equivalent to the rupture stress of the SCSi. This analysis was repeated for the three geometry configurations and two acceleration directions. For each geometry configuration, the lengths of the beams

were varied as well to simulate the experiments. An example of one model is shown in Figure 39.

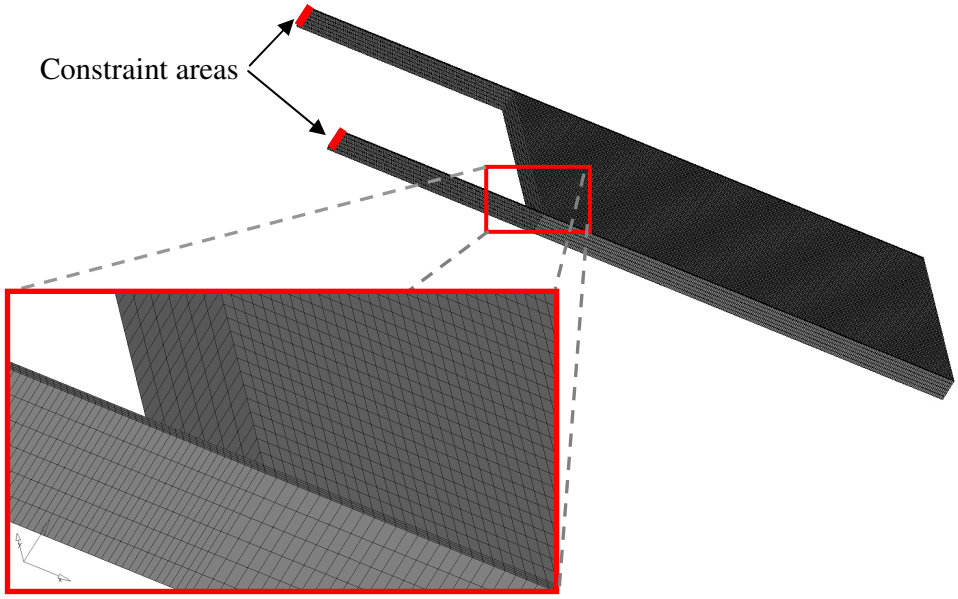

Figure 39. Finite element model of MEMS test structure

As shown in Figure 39, the elements used were three dimensional brick elements. These elements, called SOLID95, were defined as twenty-node structural elements and are widely used in structural analysis. In order to make sure that there are enough elements in the model to capture the effects, a mesh convergence study was needed. Where appropriate, a mesh convergence study may need to be performed for the number of elements, load steps, and material properties. Because the material properties in this study were linear elastic, a convergence study was not necessary. The essential strategy for guaranteeing the sufficiency of the mesh and load steps is the same. For the geometrical mesh, it is logical to begin with elements that have an aspect ratio as close to one as possible and not greater than twenty. There should also be as many elements across any geometry as is feasible. In areas of

interest, such as difficult geometries, areas of calculated values or areas where materials meet each other, it is preferable to have a denser mesh to capture greater detail. It is often practical to start with five elements across any geometry and roughly twenty element nodes in an area of interest.

To begin the convergence study, a coarse mesh was used and the number of load steps was set to fifty. A value for stress in the area of interest was found and the mesh density was increased incrementally. The stress value was found for each mesh density, and the stress value remained constant with the increase in mesh density after several iterations. The same procedure was used to find the load step increments. Beginning with one load step, the steps were increased until the calculated stress at the area of interest did not change for several iterations. If the numbers of load steps necessary for the study had exceeded initial predictions, a new geometric mesh study would have been conducted. It may be sound to assume a higher number for load steps because of the longer time needed to refine a mesh than it does to increase the number of load steps.

The model was then subjected to the global gravity loads and the stress in the area of interest is calculated for each load. The stress from several nodes in the area of interest was extracted and averaged. This average stress over a volume was used to compare to the theoretical values. The free body diagram shown in Figure 40 for an out of plane test specimen was used to calculate a theoretical stress in the cantilever legs.

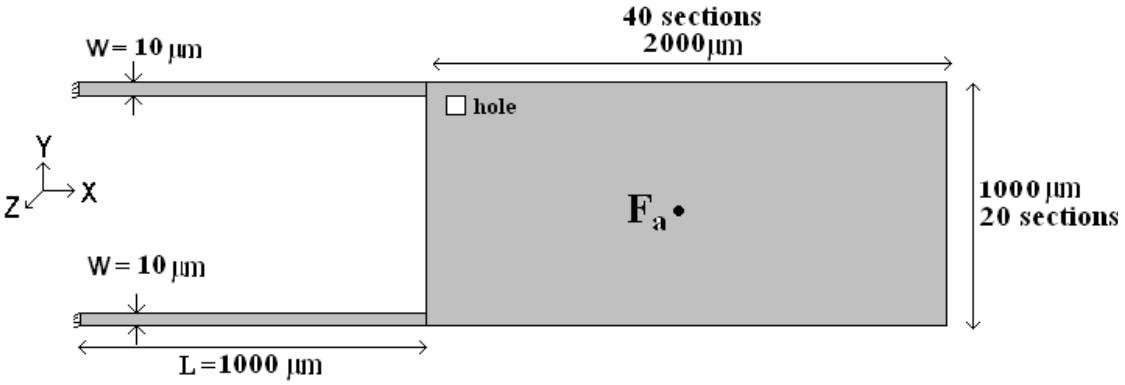

Figure 40. An out of plane test structure and its free body diagram (adapted from Emmel, 2009)

5.3.2. Comparison to Physical Test Setup[8]

The MEMS structures were designed and provided by QinetiQ. Simple MEMS accelerometers with straightforward loading and geometry were chosen rather than using complex functional MEMS devices for testing, because they provided more confidence in the resulting strength data. Two types of test were performed with respect to the orientation of the MEMS structures. The MEMS shock test structures were oriented such that the proof mass would move in the plane of the silicon die (in-plane) or bend in the direction that would take it outside the plane of the die (out-of-plane). Two distinct geometry configurations for the in-plane bending structures were used. One geometry configuration for the out-of-plane structures was used. A set of parametric structures exists for each configuration. Each configuration had a different sized proof-mass; however, the size of the proof-mass was uniform for all test structures with the same geometry. The variability in the in-plane sample geometry configurations was attributed to the range of cantilever beam lengths and

[8] Physical testing was performed by Rachel Oberc (née Emmel) and the author at CALCE in 2008-2009 with the support of Professor A. Dasgupta.

gap widths. Figure 41 illustrates a (110) flat located on one side of the wafer to define the crystallographic planes and directions.

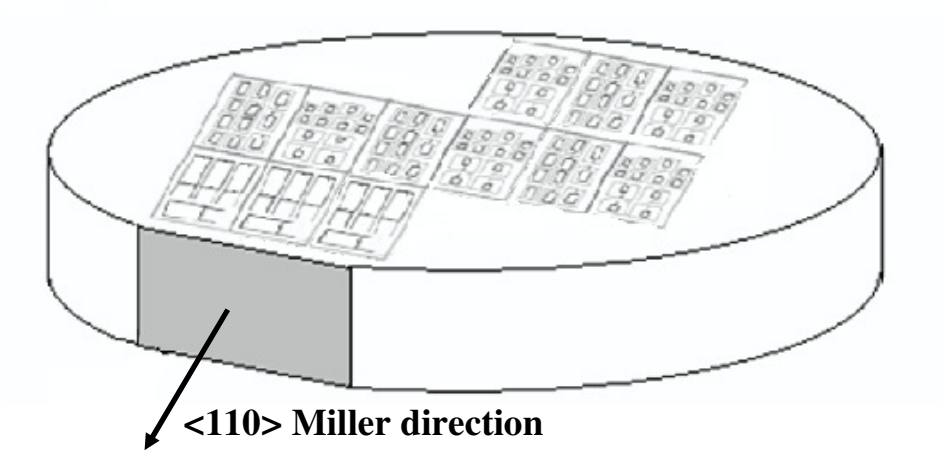

Figure 41. Diagram of MEMS shock test structure layout on silicon wafer

Close examination of Figure 41 reveals that all of the in-plane structure cantilever beams were oriented along the <110> Miller crystal directions. A representative structure from each geometry configuration is displayed in Figure 42. Each of the out-of-plane proof-masses was attached to two cantilever beams. There were four out-of-plane parametric MEMS shock test devices with identical proof-mass and cantilever dimensions but different gap widths (5, 10, 15, and 20 microns) between the cantilever beams and the side walls.

A MEMS specimen fixture was used to affix MEMS dies to the shock tower table. The aluminum specimen fixtures had dimensions of 32 × 32 × 15 mm and contained bolt holes in order to ensure a secure connection to the table. The out-of-plane devices were mounted inside a pocket to allow for full out-of-plane motion and to prevent the shock structures from hitting the drop tower table upon impact. The pocket in the structure also served to create a closed environment for the test to be

able to capture any silicon fragments. The representative shock test structures are shown in Figure 42.

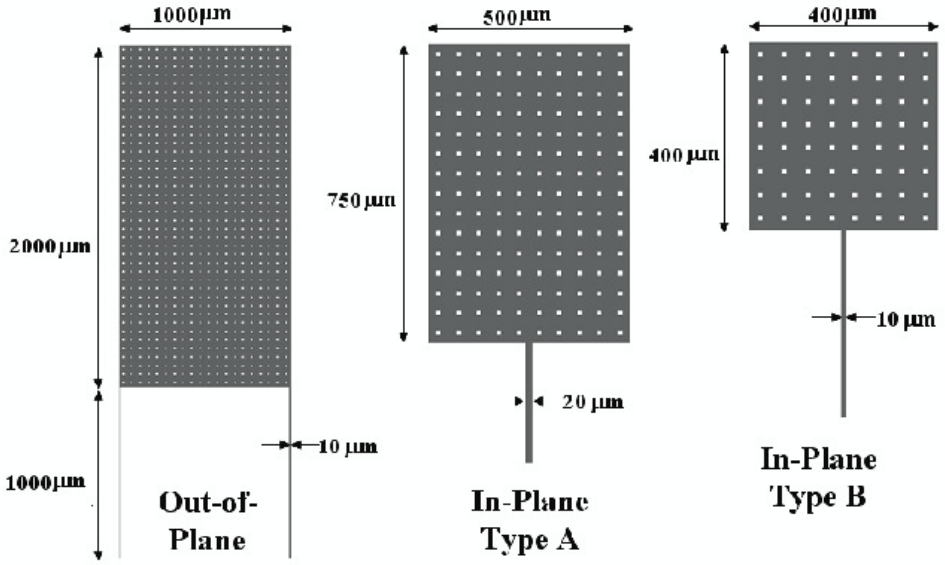

Figure 42. A representative shock test structure from each block type (not to scale) (adapted from Emmel, 2009)

The in-plane type proof masses were attached to a single cantilever beam. Three in-plane type A parametric MEMS shock test structures with cantilever beam lengths of 100, 200, and 300 microns and four in-plane type B parametric MEMS shock test structures with cantilever beam lengths of 100, 200, 300, and 400 microns were used. The MEMS shock test structures were fabricated on silicon-on-insulator (SOI) substrates with handle wafer thicknesses of 425 microns, device layer thicknesses of 100 microns, and buried oxide layer thicknesses of 3 microns. (100) p-type SCSi was used for both the device layer and the handle wafer. The die fabrication process utilized photolithography, DRIE, and isotropic oxide etch techniques. For faster release of the proof-mass from the handle substrate, 10 × 10 micron square holes were used to etch under the buried oxide layer.

Shock towers were used for dynamic testing due to their ease of use, safety, low cost of running experiments, and reproducibility of results compared to other dynamic testing systems (Zhang, 2005). This research utilized two model 23-D Lansmont shock test systems and a MTS IMPAC66 shock test machine for subjecting the MEMS test structures to dynamic loading. The Lansmont towers and the IMPAC66 shock machine achieved accelerations of up to 3000g and 5000g, respectively.

A MEMS specimen fixture was used to affix MEMS dies to the shock tower table. The aluminum specimen fixture, illustrated in Figure 43, had dimensions of 32 × 32 × 15 mm and contained bolt holes in order to ensure a secure connection to the table. Figure 43 displays the in-plane dies mounted on the side. The out-of-plane devices were mounted inside a pocket to allow for full out-of-plane motion and to prevent the shock structures from hitting the drop tower table upon impact. The pocket in the structure also served to create a closed environment for the test to be able to capture any silicon fragments.

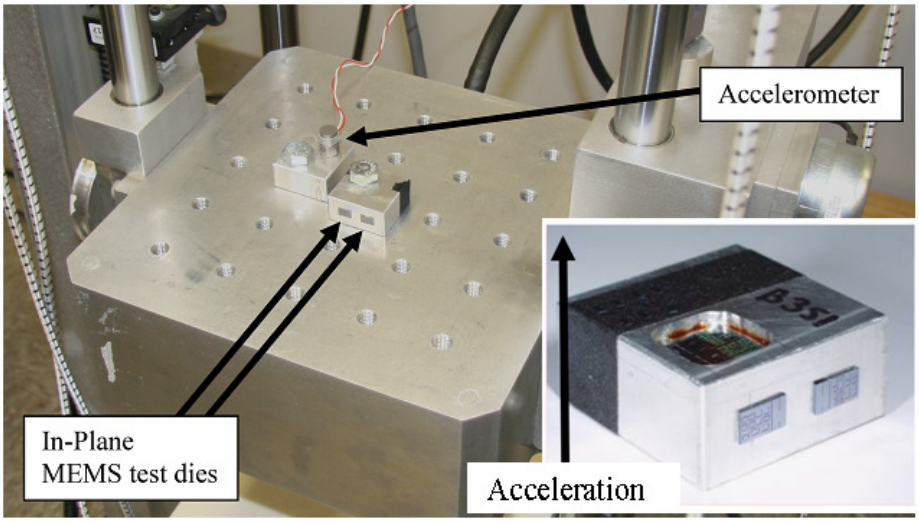

Figure 43. MEMS specimen fixture with in-plane and out-of-plane dies

An accelerometer was bolted directly to an aluminum fixture. Data from this accelerometer was used to plot the base excitation for the experiment. The two fixtures (one for the accelerometer sensor and one for the test specimens) were bolted directly to the drop tower test bed. A representative acceleration pulse profile is shown in Figure 44 for 2743g with pulse duration is 0.45 milliseconds. The noise after the pulse is shown to be less than 500g. The clamping conditions for the fixtures ensured that the accelerometer measured the actual shock profile experienced by the base of the specimens. This accelerometer was limited to measuring the profile in the direction of motion.

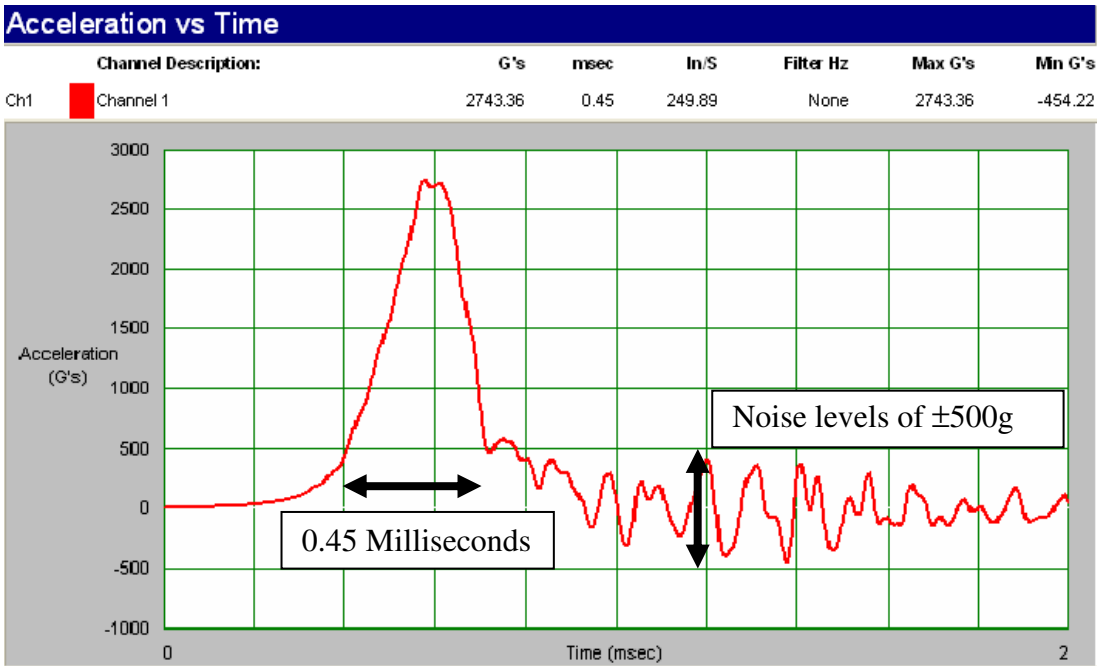

Figure 44. 2743g acceleration pulse profile (adapted from Emmel, 2009)

Adhesive for attaching the MEMS dies to the specimen fixture was selected to ensure that the dies remained attached to the fixture throughout the shock test and during post-testing analysis. EPO-TEK® 353ND epoxy was used because the adhesive bond was required to withstand accelerations exceeding 5000g during

experiments but did not need to be thermally or electrically conductive. It is important to note that the selection of adhesive or mounting compound may affect the overall performance of the device because the MEMS die is not in direct contact with the aluminum fixture. Optical microscopy, environmental scanning electron microscope (ESEM), and x-ray systems were considered as possible failure inspection methods. However, x-ray images of the MEMS dies were of poor quality because silicon and SOI did not provide adequate contrast when subjected to X-Ray inspection. Rather than x-ray, an optical microscope was used for quick inspection of the MEMS die, and ESEM was used for detailed analysis of the structure. The ESEM was the preferred method for inspecting structures and surfaces due to its increased depth-of-field and higher magnification capabilities.

5.3.3. Test and Modeling Assumptions

Several key assumptions were made for analyzing the results from physical experimentation and the simulation. Because this study considered the accelerometer's material properties at the micro-level for evaluating mechanical failures, it was necessary to define failure within this context. A physical break in the accelerometer structure was considered a definitive failure.[9] The accelerometers used were shipped in padded boxes, while any defects introduced during etching, packaging, and shipping itself were assumed to be standard damage that could be expected to occur prior to mounting.[10] This assumption allows for the probability that

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[9] While other device failures may occur without a complete fracture, a full failure modes and effects analysis exceeded the scope of this study.

[10] Additional confounding factors include the difficulty of placing a strain gage on a microscopic structure or adding a voltage bias that might skew the capacitance.

the Si suffered an undetectable defect at any point from ingot to assembly of the device on a chip.

This study implicated more than one degree of freedom for the proof mass in the MEMS structure. Therefore, some deviation between the calculations using shock amplification factor and the test results was anticipated. At higher levels of acceleration, the discrepancy was assumed to be smaller because the stress would be applied in one direction at a much higher level than others. The shock amplification factor method was considered but not employed as a standalone method because its assumptions differed somewhat from the degrees of freedom in the test configuration. Instead, finite element modeling was used to obtain a closer representation of the mass subjected to a uniform acceleration load to cause brittle failure.

5.4. Results

5.4.1. Physical Results Summary

The MEMS structures were subjected to acceleration pulses along their critical loading directions using a shock tower. Structural failures of the test specimens were anticipated. Each of the structures was expected to fail near the wall support, which is the theoretical location of highest stress. The failure mode was considered to be a disconnection of the proof mass from the base. Within each geometry configuration, the structures with the longest cantilever beams were expected to fail first because they should experience the highest levels of stress at any acceleration level. However, when the in-plane devices were subjected to 5000g acceleration pulses along their critical loading directions, the shortest cantilever beams within each block type failed instead, as illustrated in Figure 45.

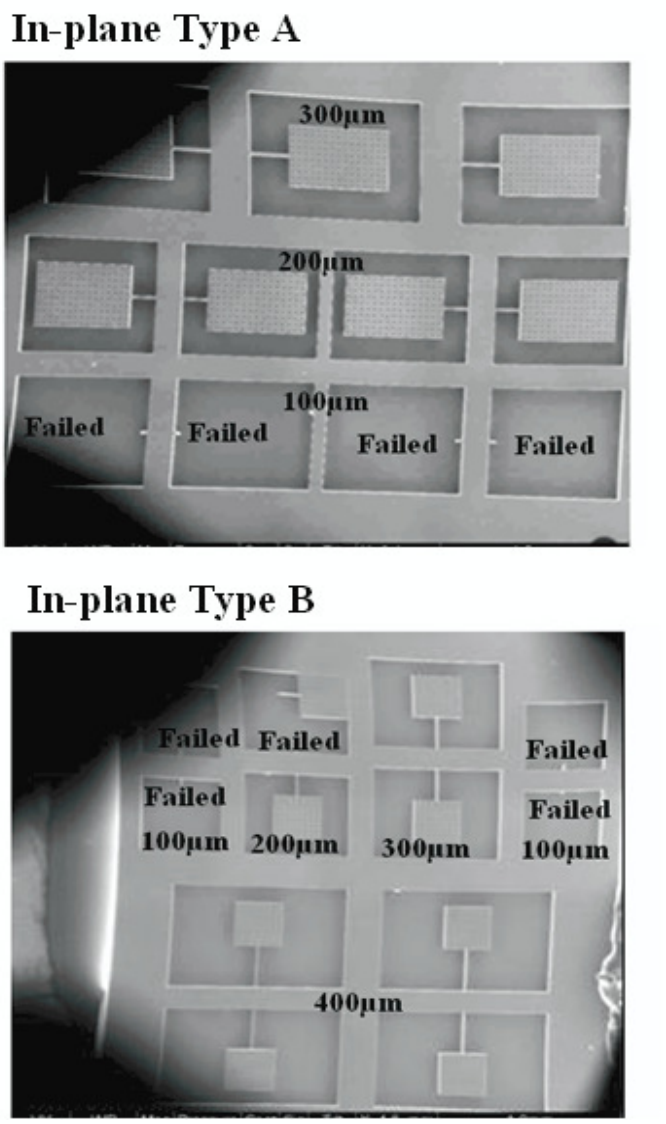

Figure 45. ESEM images of in-plane devices after 5000g acceleration pulse

The results depicted in Figure 45 suggested that the 100 micron cantilever experienced more stress than its longer counterparts. Additional testing demonstrated that when these in-plane dies were subjected to 2500g -3000g acceleration pulses along the critical loading direction using the smaller drop tables, none of the test structures failed. One reason for the unexpected failures of the in-plane structures may be that the proof-masses attached to the longer cantilevers were hitting the side walls, thus preventing maximum stress levels from being reached. By multiplying the

maximum static deflections by a factor of two, the worst-case estimates of dynamic deflection for the longest type A and type B structures were calculated as 105 and 251 microns, respectively. Both of these values are significantly lower than the corresponding gap distances of 250 and 550 microns, suggesting that the proof-masses did not hit the side walls during the test.

The proof masses of the MEMS structures were separated from the bottom of the wafer using a chemical etch process. A problem known to occur in MEMS devices is friction with the etched surface. This may have been a cause of some minor discrepancies between the theoretical and numerical models to the device performance. An imperfect etch can also cause stiction to occur between the moving mass and the rough edges underneath. Stiction is the fundamental property that small devices want to stick to each other. In the case of dynamic shock testing, this would have a larger effect in the initial motion of the mass and it is difficult to predict or measure.

A modal analysis was used to check whether the MEMS structures experienced resonance during the shock loads. The first natural frequencies for each cantilever beam length of type A and type B test structures are listed in Table 13 below. The resulting FFT of the pulse indicated peak frequency content at 9.57 kHz, 10.64 kHz, and 12.34 kHz. These frequencies roughly approximated the first natural frequencies of the 100 micron cantilever beam structures.

Device	Cantilever Length (μm)	f_n (Hz)
In-Plane Type A	100	11,318
	200	7,406
	300	5,578
In-Plane Type B	100	10,387
	200	6,369
	300	4,550
	400	3,486

Table 13. Natural frequencies of in-plane device

Notably, the natural frequencies presented in Table 13 represent approximate values found through modeling of test structures with the dimensions specified in Figure 42. The actual dimensions of each structure vary slightly as the etching processes used during fabrication of the samples may not result in the precise dimensions indicated in Figure 42. Resonance due to the high frequencies present in the acceleration pulse may be a key cause of the failures in the devices with the shortest cantilever beams. This phenomenon may explain why longer cantilever beams with higher calculated stresses but unmatched natural frequencies did not fail. The absence of in-plane device failure from overstressing at high accelerations indicates that the dynamic fracture strength of DRIE processed SCSi for bending around the <100> directions exceeded 1.1GPa.

Out-of-plane structures were subjected to acceleration pulses ranging from 1860g to 3070g along the critical loading direction using the Lansmont shock towers. Failures of these shock structures were anticipated, with increased device failure

percentages resulting from higher dynamic stress levels. A summary of these failures is shown in Table 14.

Acceleration	Max Dynamic Stress	Number of Devices Tested	Percent Failure
3,069g	1.58 GPa	4	100%
2,743g	1.23 GPa	4	100%
2,526g	1.13 GPa	8	88%
2,288g	1.03 GPa	8	63%
2,015g	0.87 GPa	11	36%
1,862g	0.80 GPa	8	25%
2,114g	0.93 GPa	8	38%
2,055g	0.90 GPa	8	63%
1,636g	0.70 GPa	12	25%

Table 14. Out of plane device shock testing summary

Post shock test inspections revealed that the failures occurred along {111} planes as expected. This result was anticipated because the SCSi is arranged in a diamond cubic (DC) crystal structure, a special form of a face-centered cubic (FCC) structure. It has been established that materials containing FCC and DC structures fail on {111} planes because they are the weakest (Lehmann *et al*., 2003). The single crystal silicon structure ruptures when the bond strength between adjacent Si atoms is exceeded. The orientation of the crystal changes the resolved stress value necessary to rupture this bond. In this case, the area of brittle failure was in the cantilever legs, as expected. The maximum tensile stress was in the <110> ("top" surface) direction, but the bond rupture direction was in the <111> direction. It was therefore necessary to calculate the vector sum of this tensile stress in the direction that was perpendicular to the break surface. In the finite element model, this was performed in reverse. The

Si-Si bond strength was known, as were the angles between the rupture direction and applied stress. The numerical model for the Si is linear elastic with failure defined as occurring when the stress in the cantilever beam equals the stress calculated from the bond rupture stress. Furthermore, it was found that fractures occurred at the base of the cantilever beams, as predicted from initial static beam calculations. An ESEM image of a typical fracture site on an out-of-plane device is shown in Figure 46.

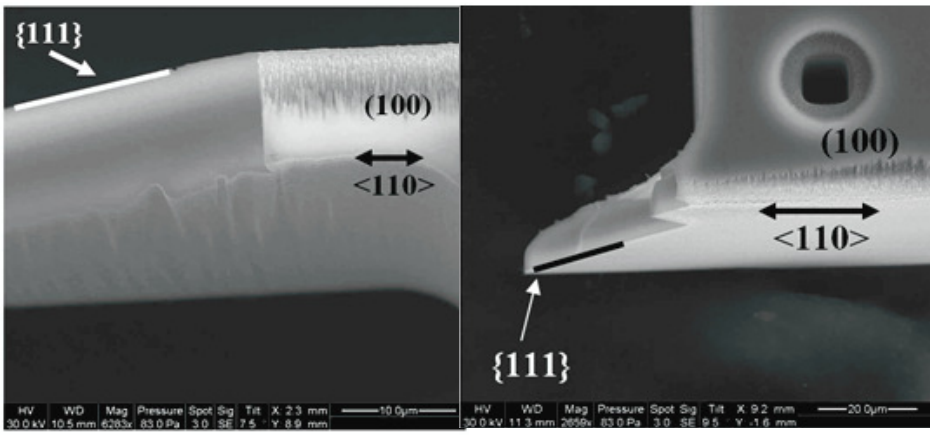

Figure 46. Fracture surfaces resulting from high shock loading

5.4.2. Exploration of Results Using Finite Element Analysis

The finite element model for the material strength of SCSi was compared against results from the physical experimentation. The experimental results were collected for each drop test. The broken pieces of silicon were collected and the failure sites were photographed. A dynamic finite element analysis performed in ANSYS revealed that the single degree of freedom (SDOF) approximation theory and the dynamic finite element analysis resulted in very similar dynamic stress values. Figure 47 depicts the results from the two stress determination methods.

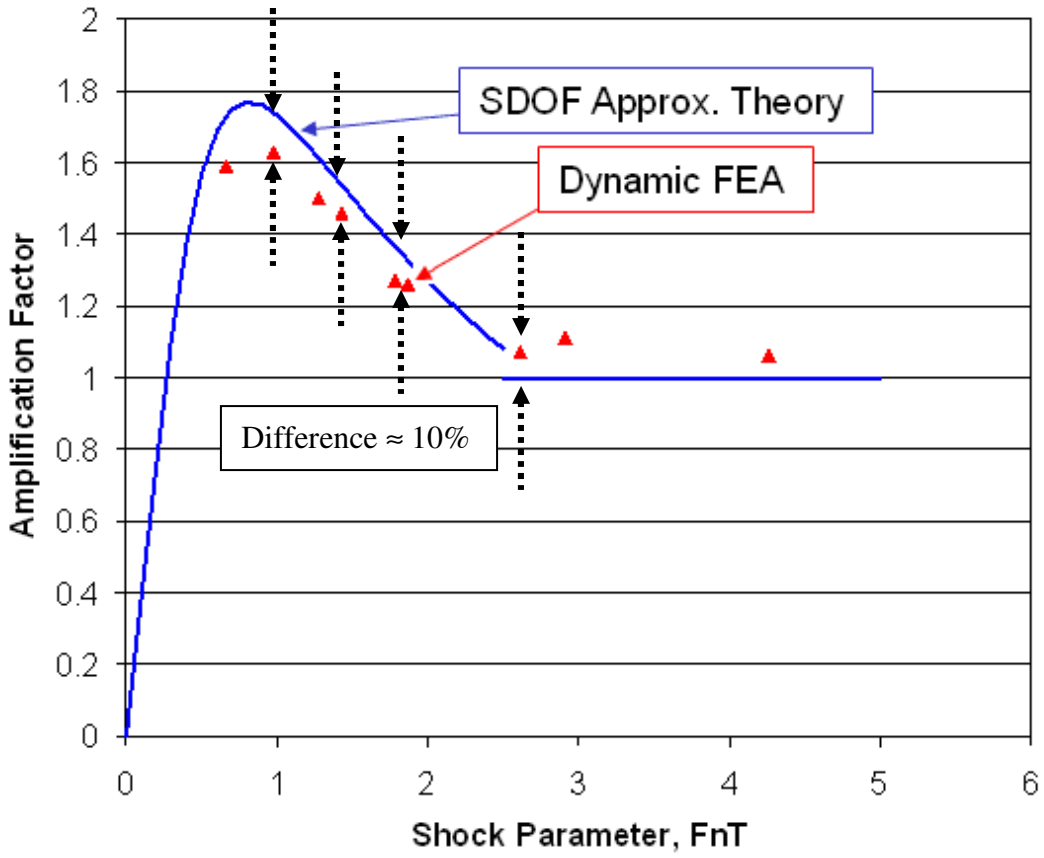

Figure 47. Results of dynamic FEA study

The SDOF approximation theory values and the values obtained from the dynamic finite element analysis are comparable, as shown in Figure 47. The comparison between the models and specimens yielded a minor difference in the dynamic stress values of about ten percent. As expected, the SDOF theory resulted in consistently higher stress values than the theoretical finite element analysis amplification factors. Using either method was found acceptable to predict the probability of failure of MEMS devices subjected to shock loads. Many products use several mutually perpendicular accelerometers. Using the acceleration profile measured by one accelerometer in such a system facilitates the measurement of the out-of-plane shock event experienced by the other accelerometers. Modal analyses of

the in-plane shock test structures were performed using ANSYS to investigate whether resonance was the possible cause for the unexpected failures of the 100-micron cantilever beams. The ANSYS analyses suggested that the structures experienced high-amplitude and high-frequency vibrations for several milliseconds after the initial loading. The correlation between natural frequencies of the 100 micron cantilever in-plane shock structures and the peaks of the Fast Fourier Transform (FFT) plot that was subsequently generated suggested that the resonant frequencies of these devices were excited during testing.

Uncertainties existed with respect to the crystal orientation in the model; however, it was reduced using knowledge from two other parts of the study. It was apparent from the ESEM imaging that the angle between the tensile stress direction and the bond rupture direction could be directly measured from the cracked specimens. It was also possible to obtain a range from the theoretical values by varying the relative angles. The angle values could be varied between ninety degrees and zero in order to get the full range of possible values, but a sensitivity study needs to consider only several degrees from the ideal angles of 34.5 and 54.5 degrees. In this case, the angle was measured from the crack surface.

5.5. Discussion

5.5.1. Advantages of FEA for MEMS Accelerometer Shock Study

The microscopic size and integration into complex components renders it difficult to measure the reliability of MEMS devices through direct experimentation. Several different MEMS accelerometers were tested to measure their dynamic failure response in a shock tower experiment. Results from this testing were compared to a

corresponding finite element analysis. A particular benefit was observed for using finite element methods to simulate the shock tower testing. The shock tower configuration implicated more than one degree of freedom for the proof mass in the MEMS structure. The assumptions underpinning a traditional shock relation known as the Sloan amplification factor are predicated on a single degree of freedom system. The shock amplification factor method could not be employed alone because its assumptions differed from the degrees of freedom in the test configuration. Therefore, the finite element model enabled a closer representation of the mass subjected to a uniform acceleration load to cause brittle failure.

The finite element model successfully predicted the probability of failure of different MEMS structures. Figure 48 shows the probability of failure plot for the out of plane bending of a MEMS structure. The FEA results were instrumental in finding the dynamic fracture stresses.

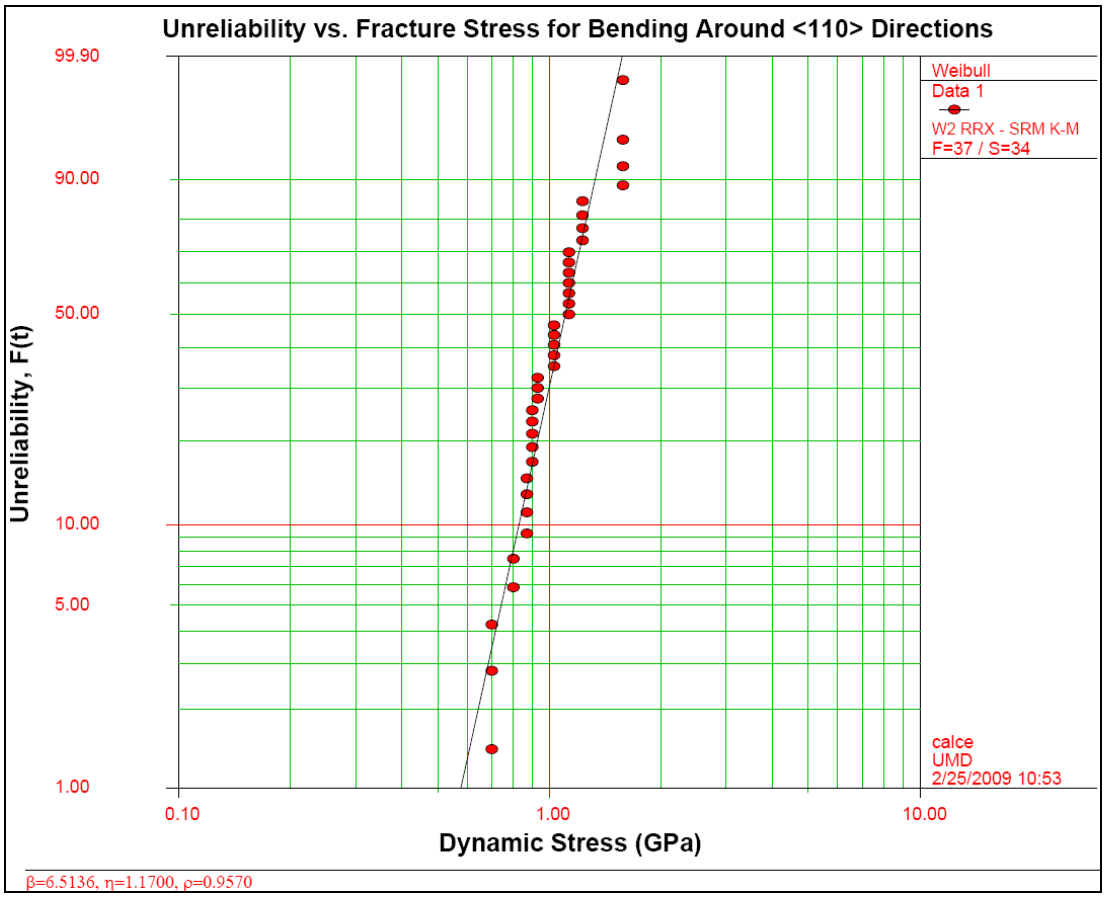

Figure 48. Weibull probability plot for out of plane bending of MEMS structures

From the tests and the FEA models, it is possible to apply this technique to other geometries subjected to shock loads. From the plot and data, it was known that a small probability (P<10%) existed that SCSi structures would fail if the dynamic stress was lower than 0.7 GPa without needing to perform numerical dynamic simulations. It is possible to apply static loads to find the maximum stresses in the structures and to correlate them to the probability of fracture.

The finite element simulation provided insight into the characterization of damage and defects introduced to SCSi during processing. The finite element simulation provided insight into the dynamic shock responses of the accelerometers and provided a basis to measure the amount of damage present in MEMS structures

as a deviation from a theoretical value. The values from the numerical models for the probability of failure of MEMS structures can be used to quantify the amount of defects a certain fabrication method introduces to the SCSi. Additional testing will be needed to ascertain the failure phenomena observed for the in-plane test structures. The relative efficiency of obtaining the out-of-plane acceleration profiles can be leveraged to improve existing predictive reliability models for MEMS devices and to ensure the accuracy of corresponding finite element analyses. Using the multi-axial test configuration with multiple accelerometers was an efficient means of gathering performance data for further use in reliability assessments of SCSi MEMS devices and for calibrating finite element models for reliability predictions. Using numerical methods expedited the assessment of various geometries and materials without a full range of costly experiments. Finite element modeling was a useful and efficient technique to overcome the difficulties of direct measurement of stresses on MEMS devices.

5.5.2. Summary

This chapter discussed the characterization of damage and defects present in SCSi after processing. The method relies on the assumption that single crystal silicon does not exhibit strain rate dependent behavior. The structures were modeled using a quasi-static load and compared to the actual appearance of fractures due to shock load. The discrepancy between the "perfect" model performance and the actual performance is used to quantify the amount of defects introduced during processing. The next chapter discusses the results of the modeling from the three test cases. It

summarizes the conclusions from the research activities presented in Chapters 3-5, describes the research contributions, and outlines potential areas for future work.

Chapter 6: Global Conclusions, Contributions, and Future Work

6.1. Summary of Findings

This dissertation presents three separate modeling efforts performed to understand failures of selected electronic components under mechanical and thermal loading. The studies used a Physics-of-Failure approach to examine the drivers of failure mechanisms and employed simulations for additional insight. The research considered MLCCs, PTHs and MEMS structures. The difference in solder solidification temperatures between normal near eutectic PbSn solder and SAC 305 lead free solder was shown to result in higher residual stresses in MLCCs. These higher stresses in capacitors mounted with lead-free solder are helpful to reduce the probability of flex cracking when the board is later loaded in bending.

For the plated through holes, the high solder reflow temperatures necessitated by the shift to lead-free solders were shown to cause significant damage to the copper plated barrels. The damage model was then used to improve prediction models for useful life of PTHs before barrel fractures appear. This was a concentrated effort to use measured thermo-mechanical analysis (TMA) data to model the interaction between boards and plated through holes above the glass transition temperature (Tg) of the boards.

The MEMS study relied on the assumption that single crystal silicon does not exhibit strain rate dependent behavior. MEMS structures were modeled using a quasi-static load and compared to the actual appearance of fractures due to shock load. The discrepancy between the “perfect” model performance and the actual

performance was used to quantify the fracture strength of the silicon due to defects introduced during processing. The numerical modeling results can be implemented in a qualification scheme for SCSi providers and in fabrication processes.

6.1.1. Model Methodology

The three test cases contained models that allowed for the examination of several parameters of interest. These models shared a common methodology that was instructive with respect to best practices. Wherever possible, natural geometries were used. This was especially critical for the MLCC cross sections where many models use simplified geometries. Complex properties were defined for materials in some instances. For example, solder was modeled with creep parameters, and capacitor flex termination was modeled as bi-linear in the MLCC study. A systematic modeling methodology was followed to reduce the variability of errors and to control the uncertainties present in the finite element simulations.

6.1.2. Global Conclusions

The use of finite element methodology to address fundamental reliability issues offers the potential to reduce testing expenditures, including the number of sample specimens and the use of equipment. These methods enable an enhanced understanding of the reliability of electronic packaging components. Results from finite element analyses can be used to supplement, if not replace, data acquired from testing conducted during manufacturing and in the field. These results may increase the efficiency with which business case analyses can be made for a particular component or assembly.

The benefits from understanding the cracking mechanism with different materials, geometries, and loading conditions include the development of better tools for calculating the probability of capacitor cracking in harsher conditions for smaller capacitors.

6.2. Research Contributions and Impacts

6.2.1. Multi-Layered Ceramic Capacitors

Contribution:

The existence of residual stresses in the capacitor body for different solders is proven to explain the difference in performance between solders. Tensile stresses that caused thermal cracking were shown to exist in the capacitor.

Impact:

The research for this dissertation contributes to the field of electronic packaging reliability. The physical phenomena that give rise to the appearance of cracking in capacitors were explored in greater depth. A numerical analysis showed the definite benefit of using the softer flexible terminations. An analytical method for showing the presence of residual stresses in the capacitor body was developed. The research showed persuasive evidence to suggest that it is beneficial to use solders with higher solidification temperatures to improve performance of capacitors in bending. At the same time, the higher solidification temperature solders increase the propensity for thermal cool down cracks along the upper surface of the capacitor.

6.2.2. Plated Through Holes

Contribution:

The plated through hole study quantified the impact of solder reflow process above the glass transition temperature of the board laminate on plated through hole barrel fracture.

Impact:

The plated through hole study made a concentrated effort to show the effect of the reflow cycle on the interaction of the board and electroplated barrel copper. Previous interconnect stress tests have stayed below the glass transition temperature of the board because of the non-linearity in the board properties. This research demonstrated that the reflow cycles added significant damage to plated through holes that is often not considered in reliability assessments. The models for predicting the useful life of plated through holes were modified and improved by using the results from this study. The results helped create better acceptance qualification procedures and faster testing times for printed circuit boards by allowing larger temperature ranges to be used.

6.2.3. Microelectromechanical Systems (MEMS)

Contribution:

The MEMS study was used to develop a fast probabilistic test technique for SCSI structures to characterize the fracture strength of the as-delivered MEMS devices.

Impact:

The MEMS research provided a faster method for the characterization of damage and defects present in as-delivered SCSi structures. The numerical simulation was used to calculate the fracture strength of the test specimens. This as-delivered fracture strength is an indirect measure of the defects introduced during the fabrication process. The novel testing approach permits simultaneous testing of many structures which allows one to develop a probabilistic failure distribution relatively quickly. The method facilitates comparison of different fabrication providers and processes.

6.3. Areas for Future Work

6.3.1. Multi-Layer Ceramic Capacitors

Future work for MLCCs should encompass an examination of smaller capacitors using detailed finite element analysis. Modeling of the effects of the silver filled polymer on substantially larger MLCCs used in heavy industrial applications and harsh environments should be performed to determine their performance when subjected to temperature and humidity bias testing. Finite element simulations using more complex bending loads, such as torsional loading, should be conducted to provide further knowledge of MLCC performance. Mounting features such as clamps and capacitors placed close to the edge of the boards should be addressed so that models can be more representative of actual use conditions.

An additional area of future work is the use of capacitors at high temperatures. The creep behavior presented here only modeled the stress relaxation at room temperature. More studies need to be performed to explore the effects of replacing

solders completely with conductive composites. The next section discusses this area of research.

6.3.2. Solder Replacement

A promising area for future work is modeling of alternatives to solder or solder replacement technologies. Adhesive manufacturers have sought entry into the solder market since the 1980s (Estes, 1999). Conductive adhesives have garnered considerable interest; however, there are challenges in providing reliable alternatives with sufficient stability (Cheng *et al.*, 2002). Silver-filled adhesives have been developed that possess adequate electrical stability and that represent viable alternatives from a cost and performance standpoint (Cheng *et al.*, 2002). The advantages of silver-filled electrically conductive adhesives include that they do not require cleaning, can be processed at lower temperatures, impart lower substrate stresses, and possess fine pitch interconnect capabilities (Li and Wong, 2006; Estes, 1999). However, compatibility remains an ongoing concern, as do strength, performance in harsh environments, and the ability to provide low resistance electrical and thermal interconnects.

Li and Wong (2006) describe reliability testing that has encompassed conductivity fatigue testing, relative humidity aging testing, impact strength assessments, and testing of current-carrying capability. Drop testing has also revealed performance challenges impairing the reliability of isotropic conductive adhesives (ICAs) (Morris and Lee, 2008). It has been proposed that the use of silver contact pads with silver epoxy composite ICA materials will reduce the probability of corrosion that currently results in the poor performance of ICAs when subjected to

temperature and humidity bias aging testing (Lee *et al.*, 2007). To date, a detailed finite element-based simulation has not compared the performance of ICAs to traditional solder materials. Performing an in-depth simulation may help to isolate the failure drivers currently impacting overall ICA reliability and thus provide useful information for their continued design and development.

6.3.3. Plated Through Holes

Additional work is needed to understand the underlying failure phenomena in plated through holes. High aspect ratio holes do not have straight geometries and a better model needs to be developed to study the effect of the asymmetric surface roughness of the plated copper. Boards with many layers that include different thicknesses and even different materials should be tested. More testing of different boards needs to be done at reflow temperatures. Testing of different hole geometries needs to be performed at reflow temperatures in order to provide a better understanding of the effect of various via geometries on the barrel failures. The effects on barrel failures due to the possibility of the delaminating of the copper flange, the appearance of shoulder cracks and the use of smoother drill profiles were not explored in this study and should be addressed in future research.

6.3.4. Microelectromechanical systems (MEMS)

Additional areas of work to explore are more processing techniques, aging, and resistance to chemical wear of SCSi. This methodology can be used to find the damaging effects on SCSi structures used in special applications where there may be

high humidity, temperature, acidity or other conditions. The research should be expanded to MEMS devices with multiple materials that exhibit strain rate effects.

6.4. Summary

The research presented in this dissertation explored drivers for failure mechanisms in flex cracking of capacitors, barrel failures in plated through holes, and dynamic fracture of MEMS. The studies used numerical modeling to provide new insights into underlying physical phenomena. In each case, theoretical explanations were examined where difficult geometries and complex material properties made it difficult or impossible to obtain direct measurements..

Appendix

A1. Literature Review Addendum

A1.1. Plated Through Hole Reliability Using Interconnect Stress Test Data

Significant research on Plated Through Hole reliability has been conducted using Interconnect Stress Testing (IST) and Highly Accelerated Thermal Shock (HAST) testing, including simulation of preconditioning steps, various Design of Experiments (DoE) factors, and PCB fabrication parameters (Furlong and Freda, 2004). Sun Microsystems first applied IST testing to thick high-aspect PCB fabrications. They later conducted IST using a test component taken from a high-end, high volume server Central Processing Unit (CPU) card known as the CPU Uniboard (Freda and Barker, 2006). These experiments controlled for a greater number of factors, including PCB fabrication and design variables, which permitted a larger sample size per cell. These experiments contained temperature cycling from ambient (approximately 22°C in their testing) to 230°C in order simulate to eutectic tin-lead assembly and rework processes. Sun initially performed time-to-failure (TTF) tests; however, the combination of IST run in six cycles at 230°C and thermal cycling at 150°C resulted in lengthy test times. Data was obtained for copper plated through holes (PTH) and phenolic cured laminate materials. Freda and Barker (2006) sought to use this data to predict the cycles to failure along a temperature range for lead-free assemblies.

The CPU Uniboard contains four dual core processes per card and 32 DIMM sockets allowing for up to 64 gigabytes of Random Access Memory (RAM), with an

additional eight cache memory cards. The CPU board and the IST test specimens were fabricated on the same panel, with 26 layers, 2.8 mm thickness, 0.35 mm minimum drill diameter, with Cu/HASL plating, and phenolic cured FR-4 laminate material. The dimensions of the IST test specimens were 27.9 ×76.2 × 2.8 mm, with a 1.5 mm hole pitch and 144 PTH interconnect holes drilled every 0.35 mm, in an 8:1 aspect ratio. Test results showed an inverse correlation between test temperature and PTH life. An inverse power law relationship was used to model the metallic copper, observing that the high coefficient of thermal expansion of the laminate material created tensile stress on the copper. They observed that if the failure threshold is approached during preconditioning, the wider the variability of the number of cycles to failure.

The authors concluded that testing at temperatures above the glass transition temperature, Tg, was cheaper and more efficient than testing below Tg. The average number of cycles to failure was 39 for temperatures in excess of Tg and as 3,000 for temperatures below Tg. The authors noted the high costs of obtaining data below Tg due to the lengthy TTFs, the large quantities of data needed for an analysis using Miner's Rule, and the difficulty of generating a temperature versus stress curve using results from dynamic and thermal mechanical analyses. Freda and Barker also observed that newer testing methods to produce reliability assessments are still gaining acceptance within industry and that methodologies for using the data based on these methods are not yet as advanced as the techniques used more traditional testing.

Xie *et al.* (2006) conducted testing on plated through holes that indicated that thermal stress testing at the lead-free temperature level of approximately 260°C may potentially precipitate a transition in the failure mode from barrel cracking to barrel-inner-layer interconnection failure. The authors' calculations used an inverse power law relationship, as did Freda and Barker (2006), between cycles-to-failure and temperature to develop life estimates for plated through holes in complex PWB assemblies.

The authors examined the disparity in results from a numerical simulation and physical experimentation, concluding that failing to fully address or account for variability in manufacturing is among the most significant reasons for the gap between model-derived life consumption estimates and predictions generated from testing. Results from this study were parlayed into a separate study that compared life prediction methodologies for plated through holes (Xie *et al.*, 2008). This study analyzed the effectiveness of the methodologies in determining acceleration factors to be used in accelerated thermal stress tests for qualification and reliability assessment of printed wiring boards (PWBs).

A2. Publications

A2.1. Multi-layer Ceramic Capacitors

G. Sharon, D. Barker, "Modeling Stress Responses of Multi-Layer Capacitors Using Varying Termination Geometries," *Journal of Failure Analysis and Prevention,* accepted for publication, 2011.

G. Sharon, D. Barker, "Crack Growth and Reliability Modeling of Multi-layer Capacitors in Microelectronics Applications," *Proc. SPIE Photonics West*, San Francisco, CA, Jan. 22 – 27, 2011.

G. Sharon, "Exploratory Modeling of Cracking Phenomena in Ceramic Capacitors," *Winter Simulation Conference, Ph.D. Student Colloquium*, Baltimore, MD, Dec. 5 – 8, 2010

A2.2. Plated Through Holes

G. Sharon, D. Barker, "Modeling of Plated Through Hole Reliability and Performance," *Multidiscipline Modeling in Materials and Structures Journal*, accepted for publication, 2011.

G. Sharon, D. Barker, "Use of Modeling to Assess Reliability of Plated Through Holes," *Proceedings of the 43rd International Microelectronics Symposium,* Raleigh, NC, Oct. 31 – Nov. 4, 2010.

A2.3. Dynamic Fracture Strength of MEMS

G. Sharon, R. Oberc, D. Barker, "Assessing the Dynamic Failure Response of MEMS Structures," *International Journal of Structural Integrity, accepted for publication*, 2011.

Acronyms

BGA	Ball Grid Array
CALCE	Center for Advanced Life Cycle Engineering
CPU	Central Processing Unit
CTE	Coefficient of Thermal Expansion
DoE	Design of Experiments
DRIE	Deep Reactive Ion Etching
FEA	Finite Element Analysis
FEM	Finite Element Method
FMEA	Failure Modes and Effects Analysis
HALT	Highly Accelerated Life Testing
IST	Interconnect Stress Test
MEMS	Micro-electromechanical Systems
MLCC	Multi-Layer Ceramic Capacitor
MTBF	Mean Time Between Failures
MTS	Mechanical Testing System
PCB	Printed Circuit Board
PWB	Printed Wiring Board
PTH	Plated Through Hole
SAC	Tin-Silver-Copper (SnAgCu)
SCSi	Single Crystal Silicon
SDOF	Single Degree of Freedom
SEM	Scanning Electron Microscope

SFP	Silver Filled Polymer
SMT	Surface Mount Technology
TTF	Time to Failure

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