ABSTRACT

Title of Document: THERMAL CYCLING RELIABILITY OF LEAD-FREE SOLDERS (SAC305 AND SN3.5AG) FOR HIGH TEMPERATURE APPLICATIONS

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Eutectic tin lead was the most widely used solder interconnect in the electronics industry before the adoption of lead-free legislation. But eutectic tin lead solder has a low melting point (183^{o}C) and was not suited for some high temperature applications, such as oil and gas exploration, automotive, and defense. Hence, for these applications, the electronics industry had to rely on specialized solders.

In this study, ball grid arrays (BGAs), quad flat packages (QFPs), and surface mount resistors assembled with SAC305 and Sn3.5Ag solder pastes were subjected to thermal cycling from -40^{o}C to 185^{o}C. Commercially available electroless nickel immersion gold (ENIG) board finish was compared to proprietary Sn-based board finish designed for high temperatures. The data analysis showed that the type of solder paste and board finish used did not have an impact on the reliability of BGAs. The failure site was on the package side of the solder joint. The morphology of intermetallic compounds (IMCs) formed after thermal cycling was analyzed.

THERMAL CYCLING RELIABILITY OF LEAD-FREE SOLDERS (SAC305 AND SN3.5AG) FOR HIGH TEMPERATURE APPLICATIONS

By

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Dedication

I wish to dedicate this thesis to my parents, my brother and my fiancée for their unconditional love and support.

Acknowledgements

I would like to express my sincere gratitude to my advisor, Prof. Michael Pecht, for giving me the opportunity to be involved in this project, and for all his support and guidance. I am also very much indebted to Dr. Diganta Das for his consistent supervision, discussion, and review on my work. I also thank Dr. Michael Osterman for his helpful insights on giving directions to my thesis. I wish to extend my thanks to Prof. Peter Sandborn, Dr. Michael Osterman, and Dr. Diganta Das for serving on my thesis committee and reviewing my work.

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Table of Contents

List of Tables

List of Figures

Chapter 1: High Temperature Thermal Cycling Reliability

1.1 Introduction and Problem Statement

The reliability of electronics used in various devices depends on the environmental conditions experienced during field use. Electronics in oil and gas exploration, avionics, automotive, and defense applications typically have more demanding thermal life cycle environments than consumer electronics [1] [2]. In under-the-hood automotive applications, operating temperatures can be over 150^{o}C depending on the location of the electronic systems in the vehicle [3] [4]. For example, engine control modules mounted directly onto the engine experiences high temperature excursions while in operation.

In oil and gas exploration applications, an estimated 15% of oil wells have ambient temperatures between 150^{o}C to 175^{o}C, and 2%-3% are in the 200^{o}C range or higher [5]. A typical application in oil and gas drilling where the electronics experience thermal cycling is wireline logging as shown in Figure 1 and Figure 2 and . Before the logging tool is lowered into the wellbore the electronics would be experiencing the ambient temperature at the surface of the earth. This can vary from extreme low temperatures e.g. in Siberia to extreme high temperatures e.g. in Sahara. In the first phase of wireline logging, the logging tool is lowered into the open wellbore on a wireline till the end of region of interest. The electronics would be experiencing high temperatures at this stage depending on the location and type of the oil well. In the second phase, the measurements (detailed record of properties) are

taken on the way out of the wellbore. Measurements are taken for the region of interest. After this region is covered, the tool is brought back to the surface in the final phase. The operational time for a traditional wireline logging application can vary from 2 to 6 hours.

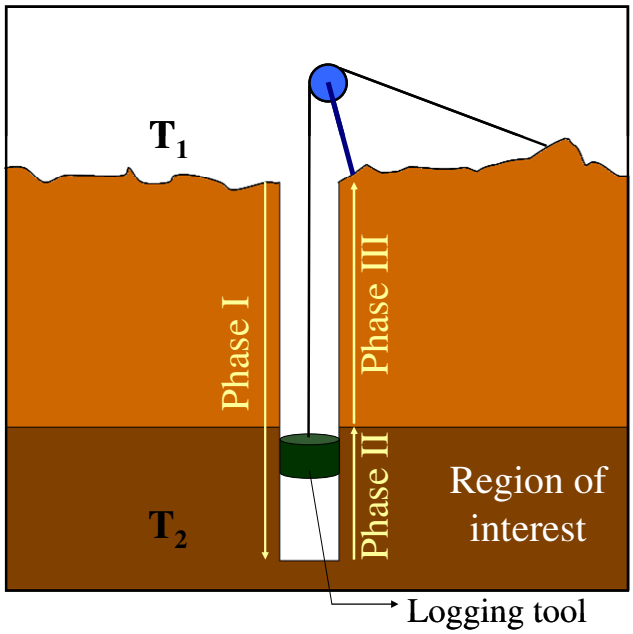

Figure 1. Schematic of wireline logging application

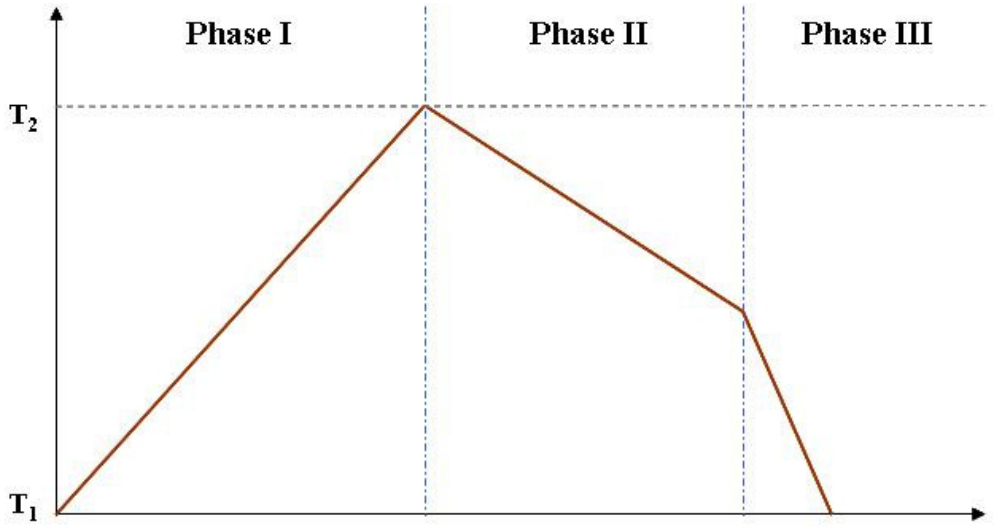

Figure 2. Phases in wireline logging application

In under-the-hood automotive applications, operating temperatures can be over 125°C depending on the location of the electronic systems in the vehicle as shown in Figure 3 [4]. The temperature excursion experienced by the automotive electronics can be divided into three phases as shown in Figure 4. In the first phase the engine is initially not operational and hence experiences the ambient air temperatures. After it is turned on, it achieves the maximum operating temperature. This is the ramp up in phase I of the profile. In phase I, the engine continues to be in operational state. High temperatures are experienced by the electronics during this period and there can be fluctuation in the temperature conditions. Finally, in phase III, once the engine is turned off the electronics return back to the ambient temperatures.

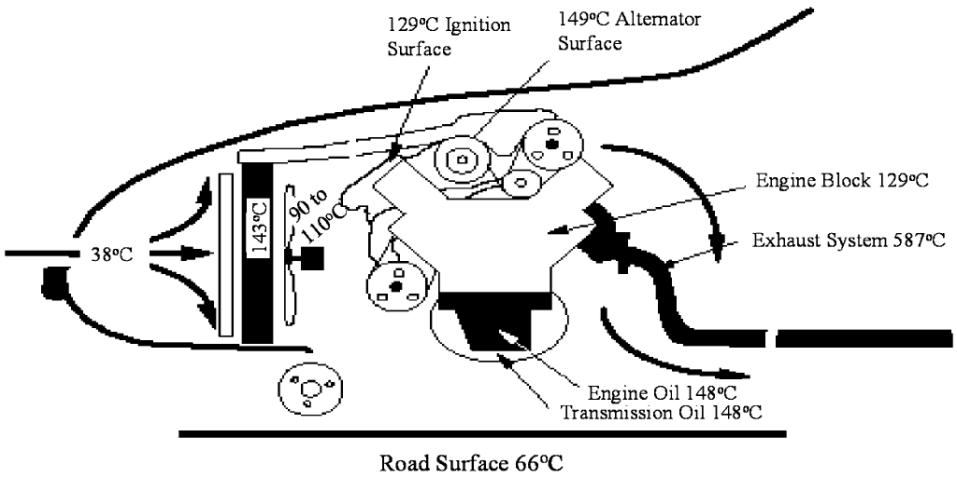

Figure 3. Air temperatures in under-the-hood electronics [4]

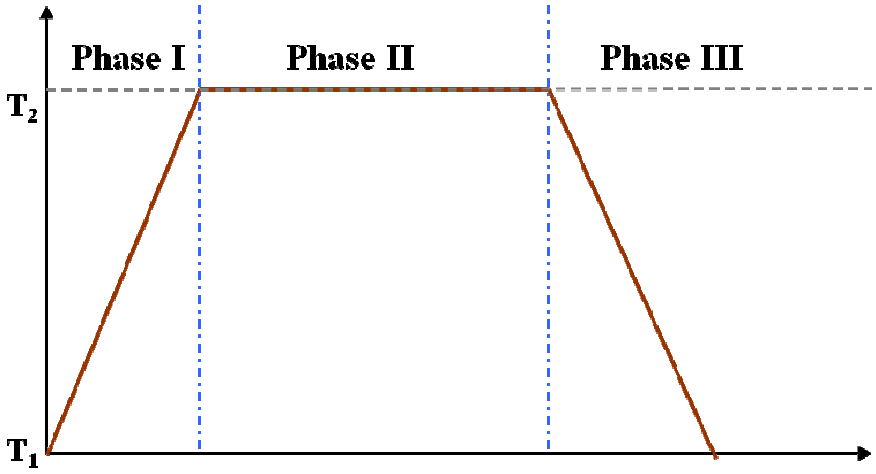

Figure 4. Phases in under-the-hood electronics

High temperatures are encountered in the electronics used in commercial and defense aircrafts and ground military vehicles. A conservative estimate for the highest ambient temperature encountered by actuator-mount electronics (without cooling) in high speed civil transport and supersonic aircraft are ≈ 193°C and 200°C respectively [2]. In mobile ground defense application like battle tank, the temperatures in electric propulsion system can reach up to 200°C [6]. So in aircraft and military applications the environmental temperature follows a profile as shown in Figure 4.

Before the adoption of lead-free legislations eutectic tin lead solder was the most widely used solder interconnect in the consumer electronics industry. However, eutectic tin lead solder is not suitable for these high temperature applications due to its low melting point (183°C). Therefore specialized solders (both lead-based and lead-free) with higher melting points are used. However, the specialized solders are expensive due to high processing and material costs. They are not widely used in the consumer electronics and hence there is little or no literature available on these specialized solders. As a result, these solders are expensive to use and need to be

qualified independently for each application. Examples of the lead-based solder used by the high temperature industry are the high lead-content tin-containing solders like 95Pb-5Sn and 95.5Pb-1Sn-1.5Ag. Although these high lead-content solders have high melting points (300^{o}C and 309^{o}C respectively), they have poor wetting characteristics and low reliability. The lead-free solders used by the high temperature industry include J-alloy and ternary variations of Sn3.5Ag and Sn5.0Sb [2].

With the restriction on the use of lead in a majority of electronic equipment [1] [7], the electronics industry has shifted from eutectic tin lead solder to lead-free solders that have higher melting points. For instance, SAC305 has a melting point of 217^{o}C. This higher melting point presents an opportunity for the manufacturers of high temperature electronics to shift from specialized solders to mainstream lead-free solders that are more commercially and economically viable. In order to shift to mainstream lead-free solders, their reliability needs to be assessed by accelerated thermal cycling tests at high temperature conditions.

Test profiles for accelerated thermal cycling are generally agreed between the customer and the supplier. In most cases, industry standards are adopted or tailored based on the requirement of the customer and application. However, the maximum cycle temperatures in the thermal cycling test standards have been limited to 150^{o}C. IPC [8], JEDEC [9], and Telcordia [10] test standards recommend various temperature cycling profiles based on the nature of the application. In order to standardize accelerated testing, IPC provides a list of mandated test conditions with the maximum recommended temperature being 125^{o}C [8]. JEDEC does not recommend thermal cycling tests over 125^{o}C for tin lead solders and 150^{o}C for lead-

free solders [9]. Furthermore, the literature on the thermal cycling reliability of lead-free solders is limited to 160°C. The publicly available literature discusses the durability of lead-free solders for temperatures ranging from -40°C to 125°C [11]-[14]. However, very few studies in the literature [15]-[17] discuss the reliability of lead-free solders at higher temperatures (>125°C).

1.2 Literature Review

One of the earliest studies to evaluate the durability of lead-free solders for high temperature applications was conducted by the National Center of Manufacturing Sciences [15]. The lead-free solders evaluated were Sn3.5Ag, Sn4.0Ag1.0Cu, Sn4.0Ag0.5Cu (SAC405), Sn2.5Ag0.8Cu0.5Sb, Sn4.6Ag1.6Cu1.0Sb1.0Bi, Sn3.4Ag1Cu3.3Bi, and Sn3.5Ag1.5In. Resistors (0805 and 1206), leadless ceramic chip carriers (20 I/Os), QFPs (120 and 160 I/Os), and PBGAs (256 I/Os) were mounted on a multilayer FR-4 glass epoxy board (T_g > 170°C) with an imidazole-finished copper surface. The boards were subjected to thermal cycling from -55°C to 160°C with a 10°C/minute ramp rate and a 10-minute dwell time. The cycles to failure of PBGA packages were not reported in the study since multiple failure modes and unexpected early failures were observed. No failures were observed in QFP packages and SAC405 performed as well as or better than Sn3.5Ag for resistors and leadless packages. The ternary lead-free alloys for instance those containing bismuth performed as well or better than Sn3.5Ag. However, the implementation of these ternary and higher lead-free alloys require additional costs for startup and qualification.

Schubert *et al.* [16] subjected flip-chip BGAs (with underfill) assembled with SAC405 and eutectic tin lead solders on high T_g FR-4 with Cu/NiAu metal finish to two different temperature ranges (-55°C to 125°C and -55°C to 150°C). In both cases, eutectic tin lead showed better characteristic life than SAC405. There was a greater reduction in the characteristic life of SAC405 at the higher (-55°C to 150°C) temperature cycling range compared to tin lead solder.

Suhling *et al.* [17] thermally cycled 2512 chip resistors soldered with eutectic tin lead, Sn3.8Ag0.7Cu (SAC387), Sn3.35Ag1.0Cu3.3Bi, Sn3.8Ag0.7Cu2.0Bi, and Sn3.0Ag0.5Cu8.0In under two temperature ranges (-40°C to 125°C and -40°C to 150°C). The test board was constructed with FR-406 glass/epoxy laminate and ENIG and HASL finishes. In thermal cycling from -40°C to 125°C, the reliability of SAC387 was comparable to eutectic tin lead. However, in the -40°C to 150°C range, SAC387 had lower reliability than eutectic tin-lead solder. The quaternary variations of SAC solder with small percentages of indium enhanced the high temperature thermal cycling reliability.

Thermal shock test is a type of reliability test to determine the resistance of the component to sudden changes in temperature. Thermal shock tests have quicker ramp rates than thermal cycling tests. In thermal cycling, stresses are generally due to CTE mismatch of the package and board laminate. However, thermal shock can result in additional stresses due to the temperature gradient and is dependent on the thermal behavior of the system [18]. Braun *et al.* [19] thermally shocked flip chip assemblies with lead-free SAC and eutectic tin lead solders to assess state-of-the-art underfill materials. Two different thermal shock profiles from -55°C to 150°C and -55°C to

175°C with a 1 minute transfer time and a dwell time of 15 minutes were applied. The components started to fail after 1000 cycles for the lower temperature cycling test, whereas the first failure occurred after 250 cycles in the higher temperature cycling test. However, the difference in the performance between the SAC and eutectic tin lead solders at the higher temperatures was marginal.

1.3 Objective of Thesis

In [15] and [17], the most durable lead-free alloys were the quaternary variations with small percentages of bismuth or indium. However, these quaternary variants are not widely used in the electronics industry and are expensive due to startup costs and qualification process. Among the mainstream lead-free solders, SAC305 and Sn3.5Ag solder alloys are the most widely used lead-free replacements. However, very few studies [15]-[17] have evaluated the thermal cycling reliability of these mainstream lead-free solders at temperatures greater than 125°C and no studies are available at temperatures greater than 160°C. If these mainstream solders prove to be reliable at temperatures greater than 160°C, they can replace specialized solders in some applications and result in economic benefit.

To obtain a quick estimate of the cycles to failure of electronics packages physics-of-failure (PoF) models are used. Engelmaier model is a semi-empirical solder joint fatigue model developed in the early 1980s as an improvement upon the inelastic strain-range based Coffin-Manson model. Although Engelmaier model is a simplified model with some deficiencies, it is widely used in the electronics industry because it provides a quick estimate of the cycles to failure. While the model was originally developed for eutectic tin lead solder, it was calibrated later to be used for

lead-free solders. If Engelmaier model can be proved to be applicable in the higher temperature ranges then it can be used a quick method to estimate the cycles to failure by the high temperature electronics industry.

In this study, the reliability of a high temperature proprietary Sn-based board finish was compared to the ENIG finish used industry wide. Under high temperature thermal cycling, if ENIG finished boards perform as reliably as or better than the proprietary finished boards, the need for high temperature proprietary board finishes can be reduced. The objective of the research presented in this study was to obtain cycles to failure data, identify failure sites and mechanisms, and assess physics-of-failure (PoF) models for temperature cycling from -40^{o}C to 185^{o}C.

1.4 Overview of Thesis

The Chapter 2 discusses the test vehicle design, test setup and thermal cycling profile. In Chapter 3, the cycles to failure is calculated using a modified cycle counting algorithm and is analyzed using Weibull++ software. The failure analysis techniques and the results are presented in Chapter 4. A detailed microstructure analysis of the various solder joint structures is described in Chapter 5. The simulation using PoF model is compared to the experimental results in Chapter 6. Finally, Chapter 7 summarizes the conclusions from this study and the research contributions.

Chapter 2: Experimental Test Setup

2.1 Test Board Design

The test board design and preliminary results have been published in [20]. The printed circuit board assembly designed for this experiment included the commonly used surface mount package types. The test board design contained an area array (BGA), a leaded (QFP), and a leadless (chip resistor) package type. The test board design provided copper metal traces designed to create electrically continuous resistive circuits called daisy chains with each individually mounted BGA and QFP package. The test boards were assembled using SAC305 (96.5%Sn+3.0%Ag+0.5Cu) or Sn3.5Ag (96.5%Sn+3.5%Ag) solder pastes using a reflow process by the research sponsor company. The material of the BGA solder balls was the same as the solder paste material used during reflow process and hence there were no mixed assemblies. The packages were reflowed at a peak temperature of 250^{o}C, and the time above liquidus temperature (221^{o}C) was approximately 1 min as shown in Table 1 and Figure 5. This reflow process was common for all solder types and board finishes.

Table 1. Reflow profile parameters

Profile Data	Temperature(^{o}C)	Dwell Time (sec)
Preheat	150-200	85
Reflow	>221	62
Peak	250	

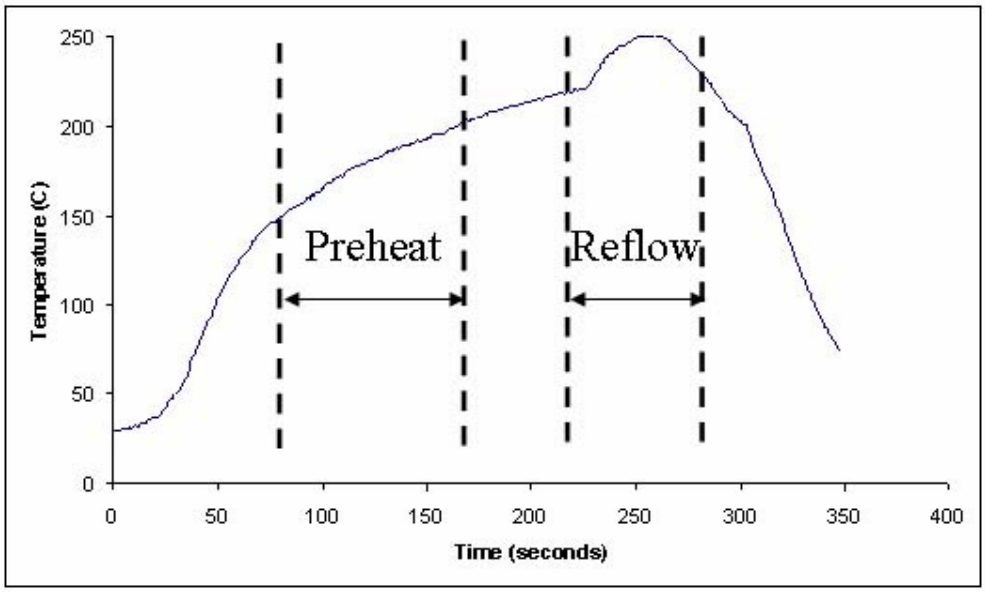

Figure 5. Solder reflow profile

Polyimide (PI) has superior high temperature capabilities and hence had been traditionally used in oil and gas industry. Glass reinforced polyimide resin (glass transition temperature (T_g) greater than 250^{o}C) was used to construct the printed circuit board since temperatures as high as 185^{o}C were planned. The 1.57 mm thick boards had two types of board finishes: industry standard ENIG finish (thickness of Ni layer ≈ 4-7 μm, Au plating ≈ 0.1 μm), and high temperature proprietary Sn-based board finish. The proprietary finish has Sn plating and nickel (Sn over Ni over Cu plating). The tin was electroplated and then dipped in oil and reflowed. In total, eight boards were tested, which consisted of two boards per board finish (ENIG/Sn-based) per solder (SAC305/Sn3.5Ag), as depicted in Table 2. Each board contained eight 1-mm pitch 256 I/O plastic BGAs, eight 1-mm pitch 144 I/O plastic BGAs, four Cu-leaded 100 I/O plastic QFPs, and twenty surface mount 1210 resistors as shown in Figure 6. For continuous monitoring of electrical resistance, one daisy chain net for

each BGA and each QFP package was used. Resistors were connected with ten resistors per resistance network as shown in Figure 7.

Table 2. Board assembly matrix

Solder ball or lead finish	Solder paste	Board finish	Board count
BGA ball - SAC305	SAC305	Sn-based proprietary finish	2
QFP finish - Matte Sn		ENIG	2
Resistor finish - Matte Sn			
BGA ball - Sn3.5Ag	Sn3.5Ag	Sn-based proprietary finish	2
QFP finish - Matte Sn		ENIG	2
Resistor finish - Matte Sn			

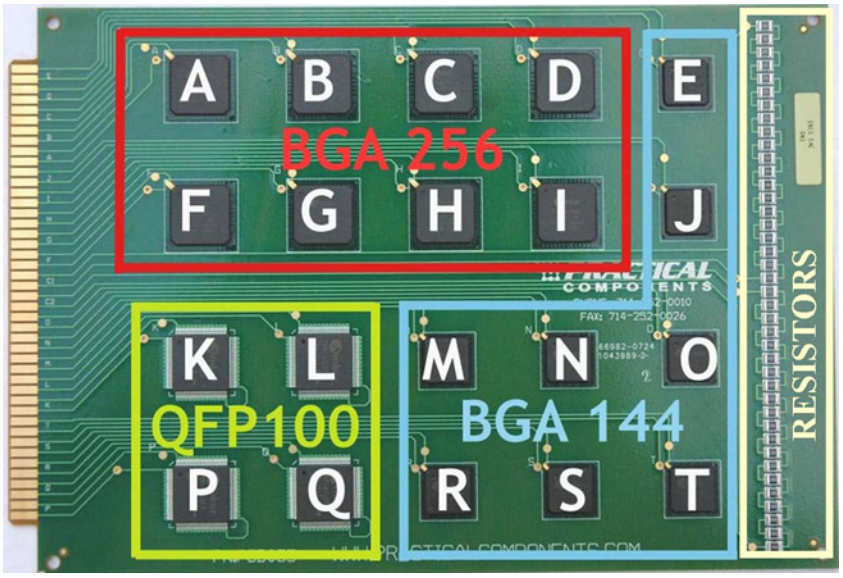

Figure 6. Test board

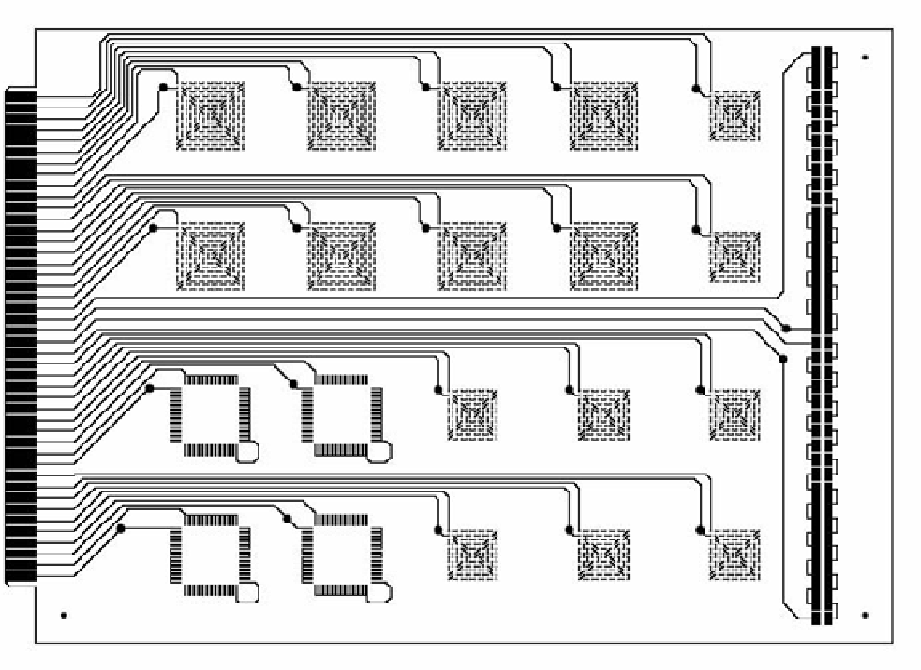

Figure 7. Daisy-chain nets in test board

The 1 mm pitch 144 I/O BGAs were not available with Sn3.5Ag solder balls. Therefore, a set of 144 I/O BGAs without solder balls were obtained and Sn3.5Ag solder balls were attached using the preform ball attach method. The perform ball attach method is a low-to-medium volume ball attach method used in the industry. A solder preform is a specially designed shape of solder adjusted to the package under consideration. The flux is applied on the BGA package. Then it is placed against the preform and put through the same reflow process as shown in Figure 5 [21].

After assembly, the components on all the boards were inspected by X-ray. No die cracks, shorts, and wire bond lift offs were observed in the reflowed packages. Except for voids in some of the solder balls as shown in Figure 8, no other defects were observed. At room temperature, the BGA and resistor daisy chains had resistance lower than 1 ohm per daisy chain and the QFP daisy chain resistance was

around 2 ohms per daisy chain. The initial resistance measurement was carried out using a multimeter. During preconditioning the resistance values of all the packages were monitored to ensure that there was no abnormality in the resistive paths of the daisy chain nets.

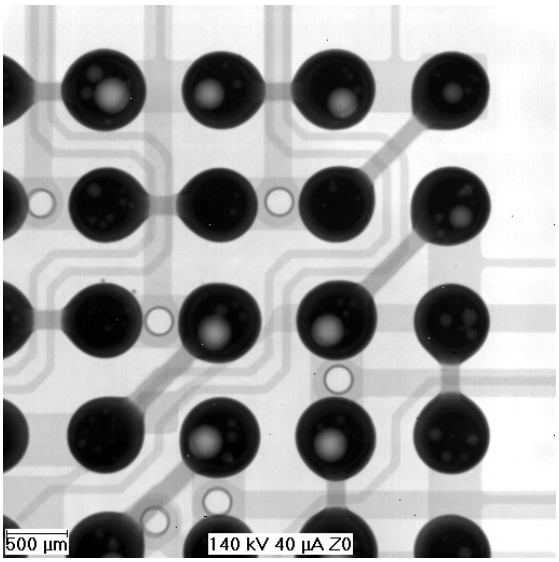

Figure 8. Voids in ENIG board finished SAC305 soldered 144 I/O BGA (courtesy: CALCE)

2.2 Test Setup

The thermal cycling test was carried out in an environmental chamber (BMA TC-4) with a maximum achievable temperature of 225^{o}C. The boards were placed vertically in an unconstrained position such that there was no obstruction to the flow of air across and around each component. Temperature was monitored during the test using three thermocouples (two measuring board temperature and one measuring ambient temperature). Three data loggers (Agilent 34970A) were used to record the resistance values of the daisy chain nets. The entire setup of the thermal cycling test is shown in Figure 9.

Figure 9. Thermal cycling test setup

2.3 Hourglass-shaped joints

In addition to voids in some of the solder balls, hourglass-shaped joints were observed at location A1 (Figure 11) in 28 of the 32 Sn-based finished 256 I/O BGAs and 27 of the 32 Sn-based finished 144 I/O BGAs. An hourglass-shaped solder joint is a slender, near cylindrical shaped joint, as shown in Figure 10. It can be selectively placed at locations of highest stress in a BGA, e.g., corner joints and peripheral joints under the die shadow [22]. Hourglass-shaped joints were observed at location A1 (Figure 11) in 28 of the 32 Sn-based finished 256 I/O BGAs and 27 of the 32 Sn-

based finished 144 I/O BGAs. The hourglass-shaped joint, located underneath the copper gate for molding of the encapsulant material, had the same stand-off height as the other solder joints in the package.

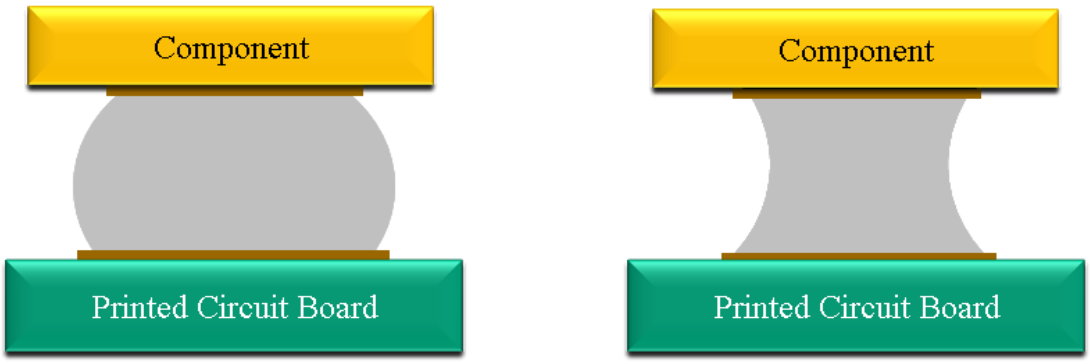

Figure 10. (a) Barrel-shaped solder joint (b) Hourglass-shaped joint

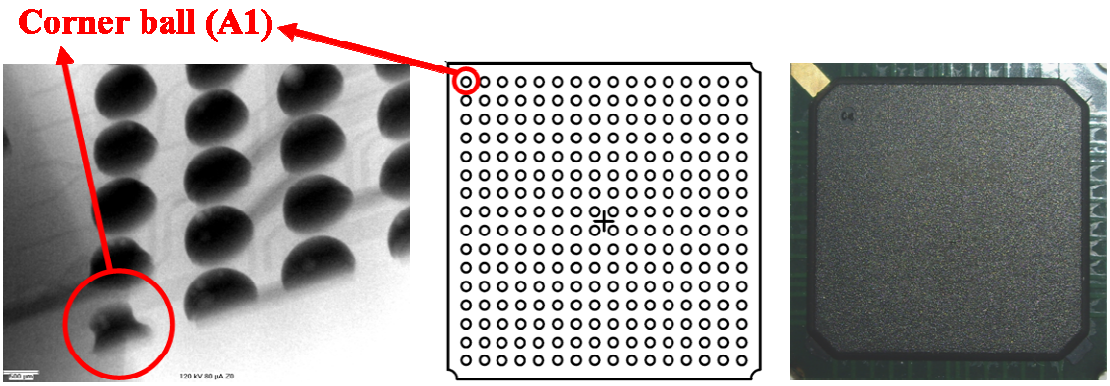

Figure 11. Location of corner ball with hourglass-shaped joint in Sn based finish SAC305 solder (control sample)

Mathematical modeling and testing in the literature have shown that hourglass-shaped solder joints have lower strain and thus better fatigue life than traditional barrel-shaped solder joints [23][24][25][26][27]. Due to lower solder volume, hourglass-shaped joints are more compliant and flexible and therefore exert less average stress on the package substrate and copper pads [23][24]. Contrary to the traditional barrel-shaped solder joints, hourglass-shaped joints have the maximum

stresses at the central plane of the solder joint (bulk solder) where the section is narrowest and not at the package-solder and solder-board interfaces [23][24]. Crack growth at the bulk solder is driven by cohesive failure, which requires more stress than adhesive failure at the interfaces and thus better fatigue life [23][24]. However, the manufacturing process of hourglass-shaped joints is neither robust nor repeatable. Limited manufacturing techniques are available to manufacture these joints [23].

2.4 Test Profile

Before thermal cycling, the test boards were pre-conditioned at 100^{o}C for 24 hours (as illustrated in IPC-9701A [8]). The pre-conditioning allows stress relief to occur in the solder interconnects and provides a common starting point for all assemblies in the test. The thermal cycling test was conducted in an environmental chamber with a target test profile of -40^{o}C to 185^{o}C with a dwell time of 15 minutes at the temperature extremes. The ramp rates were 3.5^{o}C/min for both heating and cooling. The board temperatures and individual resistance daisy chain nets on each board were monitored and collected every minute with a data logger. The boards, connected using high temperature connectors (maximum rating: 200^{o}C), were placed vertically so that there was no obstruction to the flow of air across and around each component. The failure criterion given in IPC-SM-785 [28] was used, where failure is defined as the occurrence of a resistance peak greater than 300 ohms with 9 additional peaks within 10% of the time to first peak. The temperature profile achieved by the chamber is shown by the thermocouple data as shown in Figure 12.

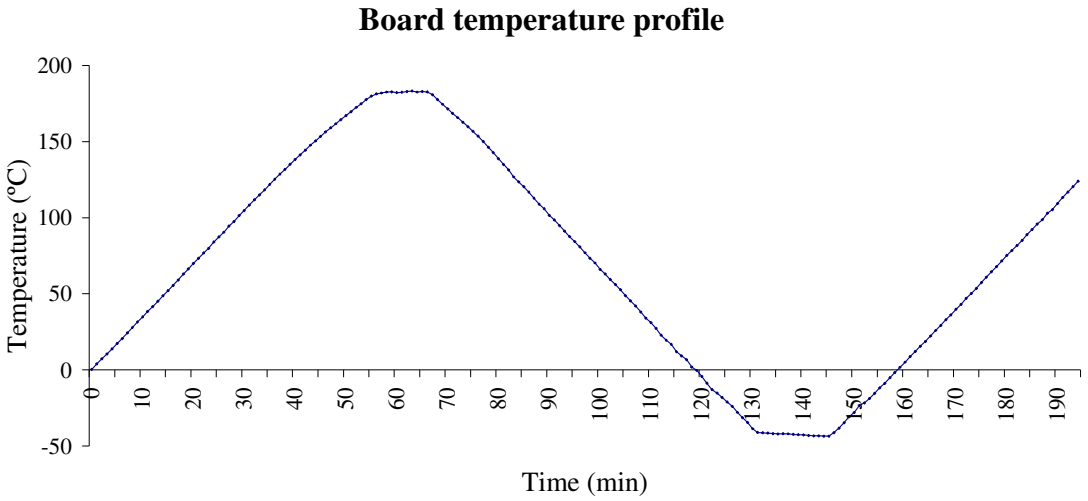

Figure 12. Temperature profile from thermocouple data

JEDEC's Temperature Cycling standard (JESD22-A104-B) recommends a ramp rate of 15°C/minute or less for any portion of the cycle, with a preferred rate of 10°C to 14°C/minute for evaluating the reliability of semiconductor parts and assembly PWBs. The BMA TC-4 thermal chamber capable of achieving a peak temperature of 185°C was unable to maintain the desired peak temperature at ramp rates higher than 3.5°C/min. Although there is no lower limit specified in the standards for the lower limit on ramp rate, the maximum achievable ramp rate of 3.5°C/min was lower than the preferred ramp rates listed in standards. To understand the impact of the low ramp rate on the results, the effect of ramp rate on the thermal cycling reliability was studied. Analysis and literature study on the effect of ramp rate on the reliability was performed.

In a finite element analysis by Zhai *et al.* [29], 64 I/O BGA models mounted on FR-4 board laminate were analyzed under three thermal cycling load profiles with ramp time 3 min, 10 min and 20 min with zero dwell time. The solder joint fatigue

life increased with the increasing ramp time (i.e. decreasing ramp rate). However, the acceleration factor increased only by a factor of 10% when the ramp time changed from 20 min to 3 min as shown in Figure 13. In order to validate the FEA results, three thermal cycling tests were carried out (ramp = 10 min / dwell = 5 min, ramp = 5 min / dwell = 5 min, and ramp = 5 min / dwell = 10 min). Experimental results also showed that there was little or no impact on the solder joint life with the increase in ramp rate as shown in Figure 14.

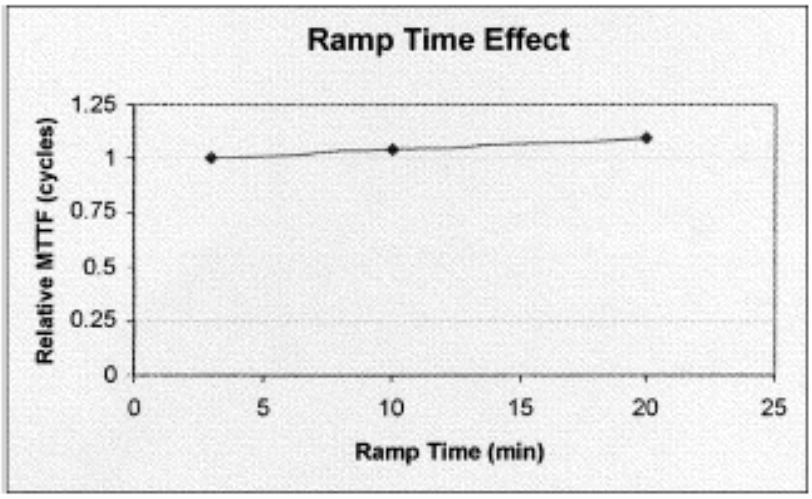

Figure 13. Predicted solder fatigue life (relative MTTF vs ramp time) [29]

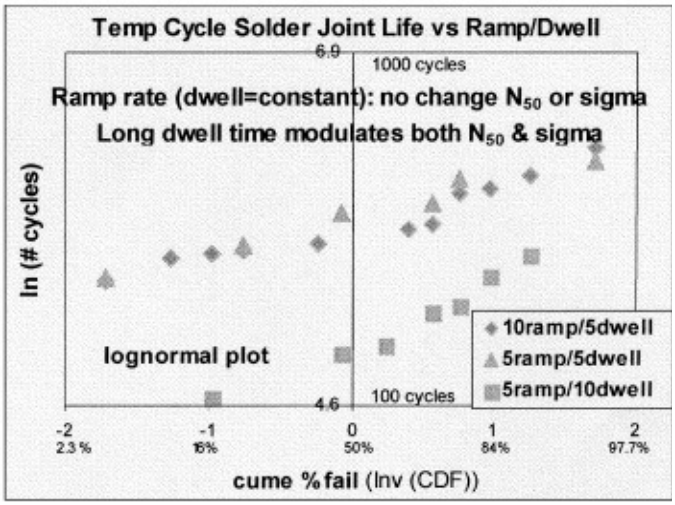

Figure 14. Experimental N_{50} as function of ramp/dwell [29]

In another study by Aoki *et al.* [30], 196 I/O BGAs soldered with eutectic tin lead or SAC305 mounted on FR- boards were thermally cycled under three different ramp rates. The ramp rates were 6, 15 and 35 ^{o}C/min and dwell time was 10 min on either extremes. As the ramp rate was decreased from 35oC/min to 6oC/min, an approximate increase of 10% in cycles to failure was observed. Qi *et al.* [31] thermally cycled 2512 resistors soldered by eutectic tin lead and SAC387 on FR-4 board with ramp rates of 14^{o}C/min and 95^{o}C/min and a dwell time of 5 min. The cycles to failure of SAC387 soldered resistors were comparable for both the conditions as shown in Table 3.

Table 3. Cycles to failure of SAC387 soldered resistors [31]

Test condition	Cycles to failure		
	First failure	10% failure	63% failure
14^{o}C/min	1941	2052	3710
95^{o}C/min	1770	2274	3984

Chapter 3: Data Analysis

3.1 Background

Temperature was monitored during the test using three thermocouples. According to the planned test temperature profile, every cycle should have a temperature range (ΔT) of 225°C (-40°C to 185°C) and a mean cyclic temperature (T_{mean}) of 72.5°C. However, analysis of the thermocouple data identified instances where the target profile was not achieved. For example, in Figure 15 the cycles in the circled region had a temperature range lower than 225°C and a mean cyclic temperature higher than 72.5°C.

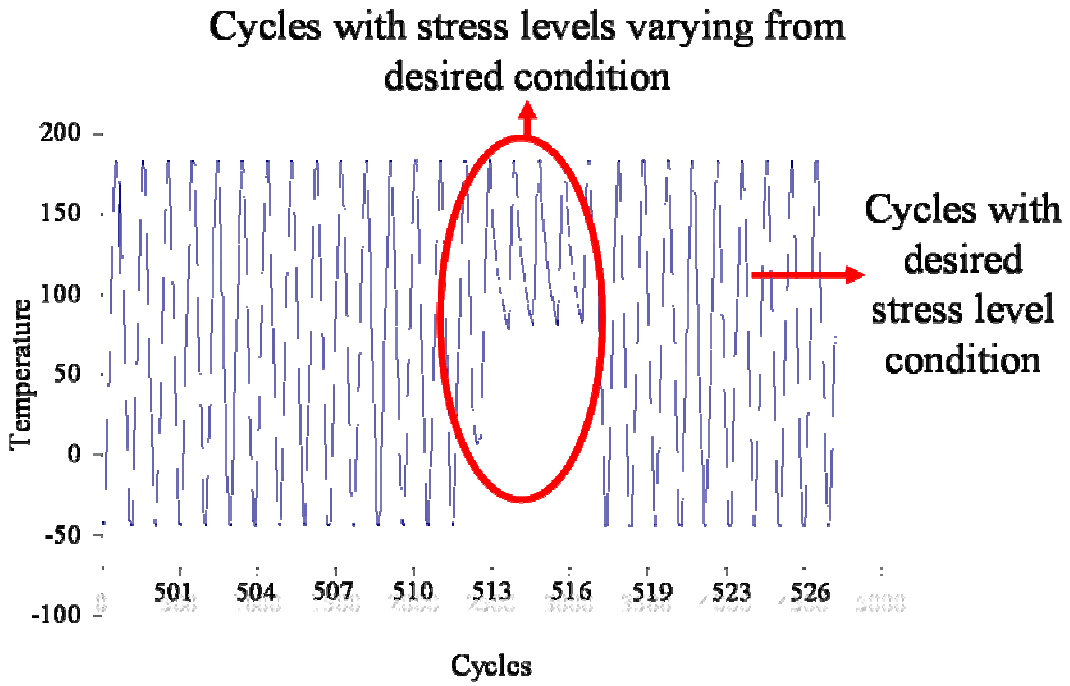

Figure 15. Illustration of temperature excursions observed during test

Although the count of these cycles were significant as shown in Figure 16 of the total number of cycles, they could not be ignored as they induced fatigue damage on the solder joints. The damage caused by a thermal cycle is a function of the temperature range and cyclic mean as shown in Figure 17. Hence the damage due to cycles with stress levels varying from the target test profile cannot be considered the same as the damage due to target stress level cycles.

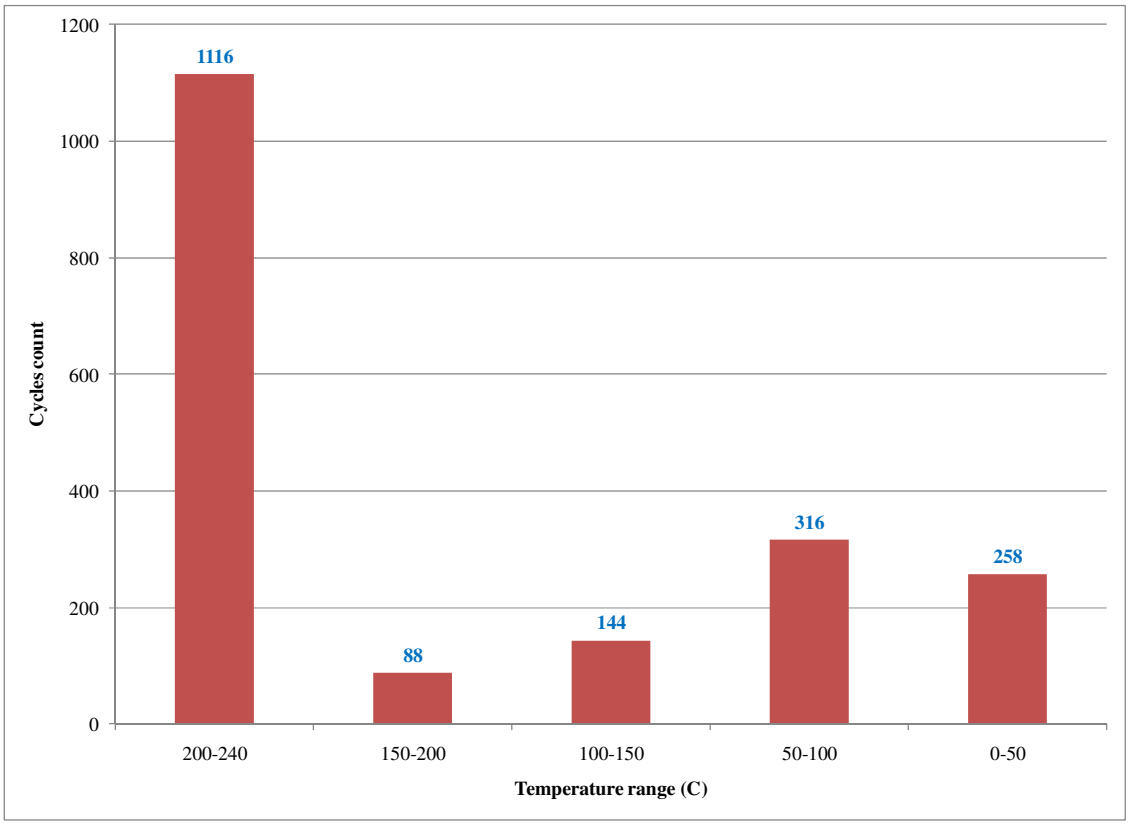

Figure 16. Number of cycles in each temperature range plotted as a histogram

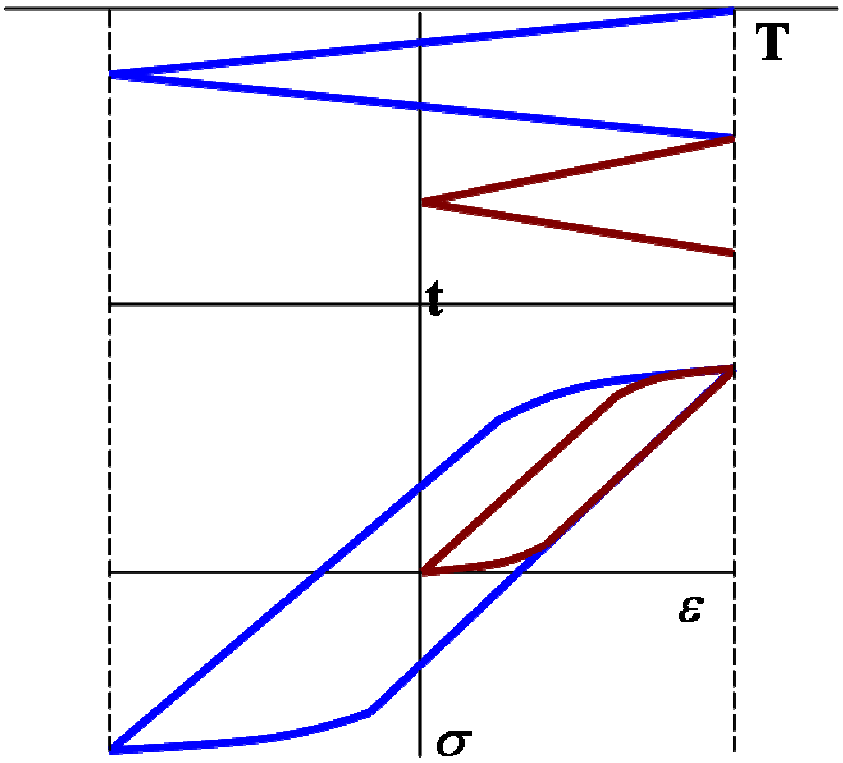

Figure 17. Hysteresis loops of various cycles

3.2 Modified cycle counting procedure

To account for the cycles that could not achieve the target temperature profile, a cycle counting procedure was adopted that was based on the PoF model and Miner's rule of damage accumulation. This procedure considered the impact of temperature range and mean cyclic temperature.

In the first step, the cycles to failure (N_{target}) with the target test temperature profile was determined. A physics of failure (PoF) model was used to calculate N_{target}, where the temperature range (225^{o}C) and mean cyclic temperature (72.5^{o}C) of the target test temperature profile and solder joint parameters were provided as inputs. Many sophisticated PoF models are available for thermal cycling but as a first step the simplest and commonly used Engelmaier model calibrated with lead-free

constants was used in this procedure. Engelmaier model was defined by the following equation:

$$N = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f}\right)^{\frac{1}{c}} \quad (1)$$

where N is the number of cycles to failure, $\Delta\gamma$ is the total shear strain, ε_f is the fatigue ductility coefficient, and c is the fatigue ductility exponent. The total shear strain range for a leadless package is approximated to be:

$$\Delta\gamma = F\left(\frac{L_d \Delta\alpha \Delta T}{h}\right) \quad (2)$$

where F is the model calibration constant, L_d is the distance between the critical interconnect and the neutral point, $\Delta\alpha$ is the difference in CTE between the package and printed wiring board, ΔT is the temperature range of temperature cycling, and h is the effective height of the solder joint. For any solder subjected to temperature cycling loading, the fatigue exponent is defined as:

$$c = c_0 + c_1 T_{sj} + c_2 \ln\left(1 + \frac{360}{t_{dwell}}\right) \quad (3)$$

where T_{sj} is the mean cyclic solder joint temperature in ^{o}C, and t_{dwell} is the dwell time at the temperature extremes. The temperature cycle fatigue model constants are dependent on the solder type. The model constants were developed for lead-free solders by validating with experimental data up to 125^{o}C [42]. However, model constants valid at temperatures greater than 125^{o}C were not available. Hence, in order to calculate the damage, it was assumed that the constants of the Engelmaier model developed in [42] hold up to a temperature of 185^{o}C. Thus, the validity of model constants up to 185^{o}C is an underlying assumption with the cycle counting algorithm.

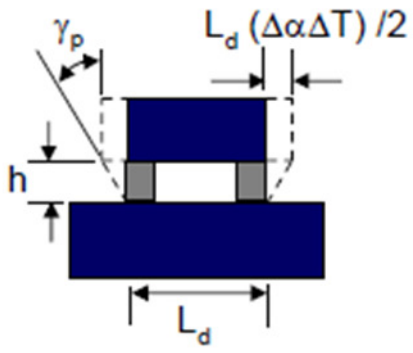

Figure 18. Schematic of a leadless package

In the second step, maxima and minima (i.e., the locations at which the slope of the curve reverses) of the thermocouple temperature data were identified. Noise in the data was reduced using a Moving Average Filter. Then the temperature range and mean cyclic temperature of each individual temperature cycle (i) in the thermocouple data were calculated. For each cycle (i), the cycles to failure (N_i) was calculated using the PoF model. This means that N_i number of i cycles are required for the product to fail. Each of these cycles can be represented as a ratio with respect to the target test temperature profile (N_i/N_{target}). The total number of effective cycles was calculated using Miner's rule given by the following equation:

$$N_{total} = \sum \frac{N_i}{N_{target}} \qquad (4)$$

The cycle counting algorithm is explained further by an illustration. For SAC305 soldered 256 I/O BGAs, the number of cycles to failure of the target test profile (N_{target}) was 1720 cycles. Consider a cycle which could not achieve the target profile condition, for example, with $\Delta T = 130^oC$ (55^oC to 185^oC) and $T_{mean} = 120^oC$. Using the PoF model the time to failure (N_i) was calculated to be 1360 cycles. The

ratio with respect to the target test temperature profile was (N_i/N_{target} = 1360/1720), which is 0.8. Therefore, if there were 5 cycles with ($\Delta T = 130^oC$ and $T_{mean}= 120^oC$), the equivalent number of cycles with ($\Delta T = 225^oC$ and $T_{mean}= 72.5^oC$) would be 5 times the ratio (0.8), which would be 4 cycles. Finally, the total number of effective cycles to failure was calculated using Miner's rule by summation of all the ratios.

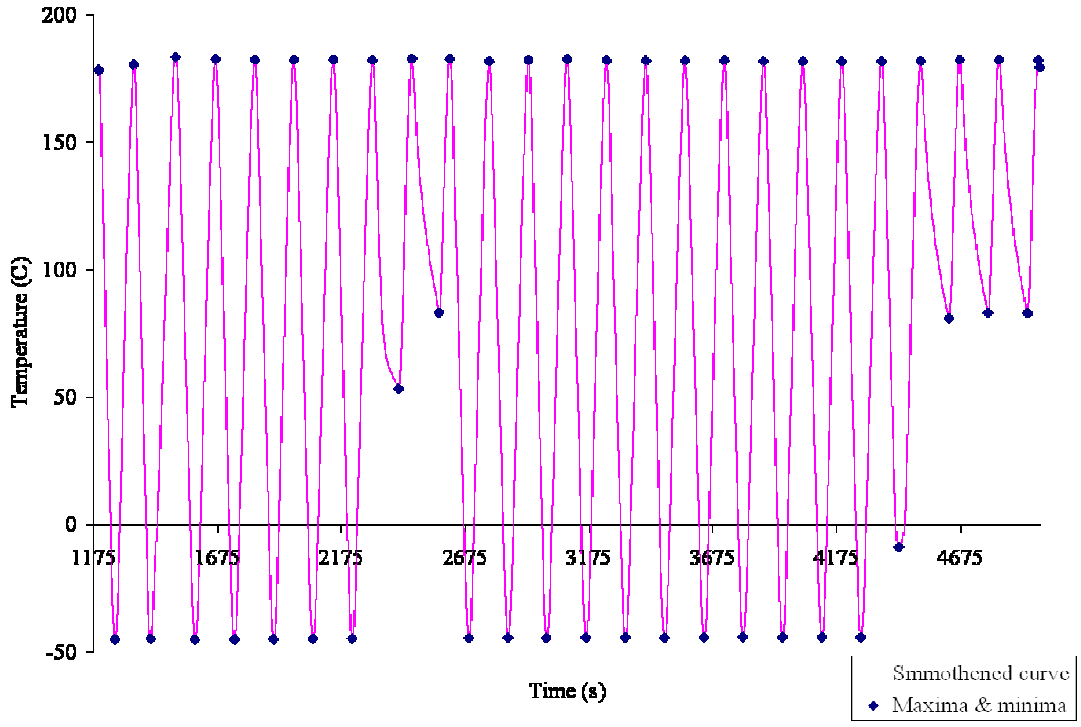

Figure 19. Smoothened curve with maxima and minima

Time	Peak temperatures	Cyclic Range	Cyclic Mean	N_f	Average N_f	Ratio
Ideal condition		225.00	72.50	3436	3436	1.00
669	-44	220	66	4537	4393	0.78
750	178	222	67	4248		
816	-45	223	67	4284	4157	0.83
891	181	226	68	4030		
959	-45	225	68	4026	3873	0.89
1060	183	228	69	3720		
1138	-45	229	69	3729	4010	0.86
1195	178	223	67	4290		
1261	-45	223	67	4284	4157	0.83
1336	181	226	68	4030		
1404	-45	225	68	4026	3873	0.89
1505	183	228	69	3720		
1583	-45	229	69	3729	3768	0.91
1666	183	228	69	3806		
1743	-45	228	69	3804	3814	0.90
1825	182	228	69	3823		
1900	-45	227	69	3821	3823	0.90
1983	182	227	69	3824		

Figure 20. Illustration of calculation of modified cycles to failure

The cycle counting procedure is dependent on the solder material properties and the package dimensions since cycles to failure were calculated using PoF models. The same procedure can be used to analyze the interconnect fatigue life of components subject to actual field conditions, since temperature cycles at varying stress level conditions are likely to occur in uncontrolled field conditions.

3.3 Weibull Analysis

The temperature cycling experiment was time terminated after 4000 hours. At termination, all 256 I/O BGAs had failed according to the defined failure criterion. Two-parameter Weibull analysis was performed on the cycles to failure values for the four sets of 256 I/O BGAs (as shown in Table 4 and Figure 21). For 256 I/O BGAs, the Kruskal-Wallis test showed no statistical difference in the cycles to failure data

between the different board finishes considered, as shown in Table 5. The solder joint reliability was comparable for SAC305 and Sn3.5Ag solders regardless of board finish under high temperature cycling.

Table 4. Weibull parameters for 256 I/O BGAs

Weibull parameter	Sample size (failures/total)	η (Characteristic life in cycles)	β (Weibull slope)	Cycles to 50% failure
Sn-based finish/SnAg solder	16/16	1240	4.9	1151
Sn-based finish/SAC solder	16/16	1245	5.1	1160
ENIG finish/SnAg solder	16/16	1296	5.2	1208
ENIG finish/SAC solder	16/16	1390	5.4	1300

Table 5. p-values in Kruskal-Wallis test for 256 I/O BGAs

256 I/O BGAs	ENIG finish Sn3.5Ag solder	Sn-based finish SAC solder
Sn-based finish Sn3.5Ag solder	0.559	0.895
ENIG finish SAC solder	0.258	0.152

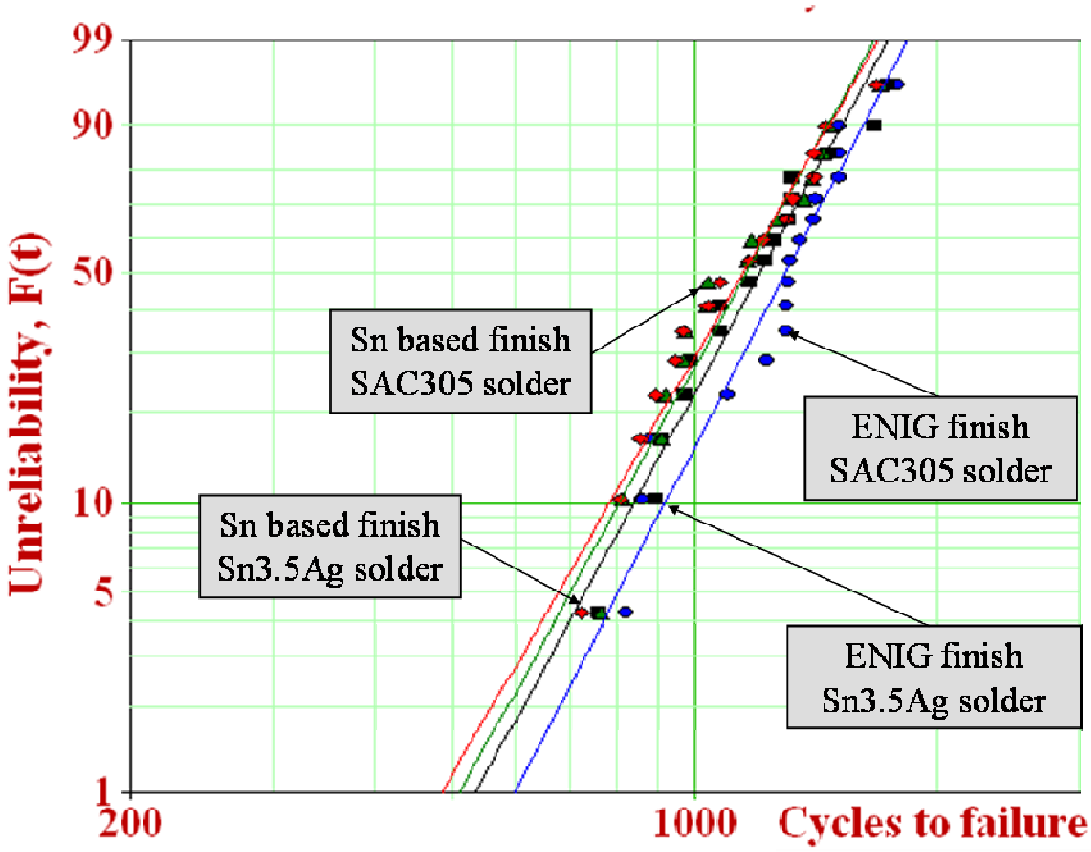

Figure 21. Weibull analysis of cycles to failure data of 256 I/O BGAs

Fifty-five 144 I/O BGAs failed according to the defined failure criterion as shown in Table 6 and Figure 22. SAC305 soldered Sn-based board finished 144 I/O BGAs failed earlier compared to the data sets and were statistically different from the others, as shown in Table 7. This difference was not expected and hence a detailed analysis was performed to determine the cause. The Kruskal-Wallis test showed that ENIG finished Sn3.5Ag-soldered 144 I/O BGAs were statistically the same as ENIG finished SAC305-soldered and Sn-based finished Sn3.5Ag-soldered 144 I/O BGAs. The probability values for the various combinations are listed in Table 7. ENIG finished SAC305 soldered boards had the maximum number of survivors at the termination of the test.

Table 6. Weibull parameters for 144 I/O BGAs

Weibull parameter	Sample size (failures/total)	η (Characteristic life in cycles)	β (Weibull slope)	Cycles to 50% failure
Sn-based finish/SnAg solder	14/16	1654	6.2	1560
Sn-based finish/SAC solder	16/16	1130	10.1	1090
ENIG finish/SnAg solder	15/16	1635	9.2	1572
ENIG finish/SAC solder	10/16	1844	5.6	1729

Table 7. p-values in Kruskal-Wallis test for 144 I/O BGAS

144 I/O BGAs	ENIG finish Sn3.5Ag solder	Sn-based finish SAC solder
Sn-based finish Sn3.5Ag solder	0.326	0
ENIG finish SAC solder	0.506	0

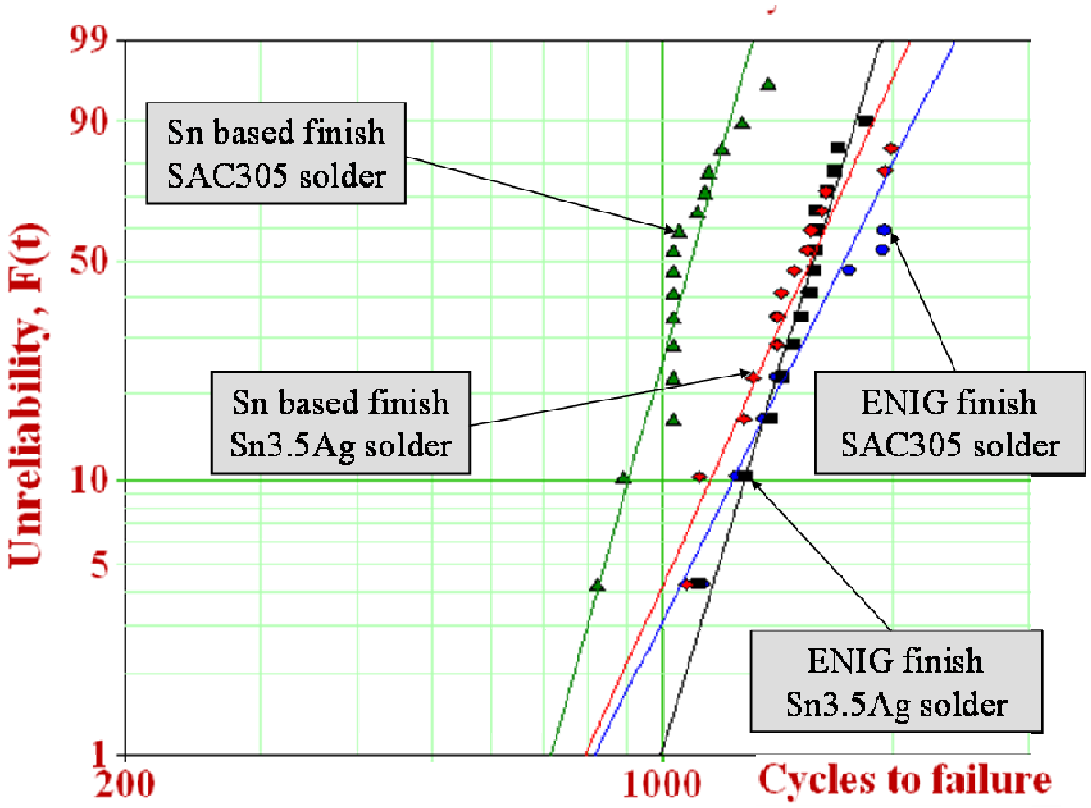

Figure 22. Weibull analysis of cycles to failure data of 144 I/O BGAs

The 144 I/O BGAs had greater characteristic life values compared to 256 I/O BGAs. Solder joints in 256 I/O BGAs had a higher stand-off height (30 microns more) than those in 144 I/O BGAs which improves durability. However, 256 I/O BGA package (17mm×17 mm) had greater distance from neutral plane (DNP) when compared to 144 I/O BGA package (13mm×13 mm) which decreases durability. From the failure data, it is evident that effect of DNP affected the reliability of packages to a greater extent than the effect of solder joint height. The failure data of BGA packages with 256 I/O and 144 I/O test specimens with Sn-based board finish and assembled with Sn3.5Ag solder paste were plotted using a Weibull two-parameter distribution, as shown in Figure 23.

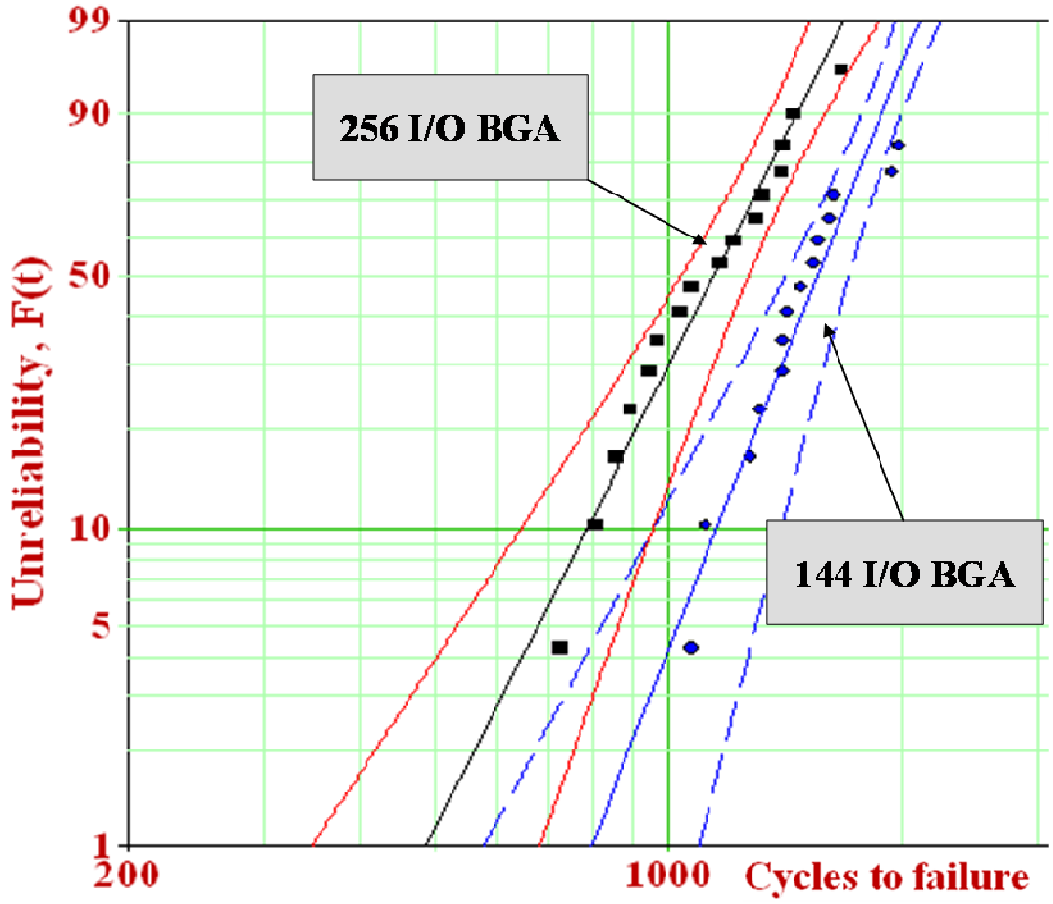

Figure 23. Comparison of 256 I/O BGA and 144 I/O BGA packages (Sn based finish and Sn3.5Ag solder)

None of the QFP packages or resistors failed according to the defined failure criterion at the termination of the test, which agrees with the PoF model predictions for the QFP packages used in this test. Durability data showed that the cycles to failure of 1% of the components was between 405-551 cycles for 256 I/O BGAs and 475-715 cycles for 144 I/O BGAs having a confidence level of 90%. The means for the above distributions were 472 cycles for 256 I/O BGAs and 584 cycles for 144 I/O BGAs.

Chapter 4: Failure Analysis

4.1 Failure site

Non-destructive failure analysis was carried out after the termination of the thermal cycling test. The resistance of tested samples were electrically measured using Fluke TRMS Multimeter (resistance accuracy: 0.05%) to confirm failure in the BGA packages failed according to the defined failure criterion. The samples were inspected under X-ray and compared to the pre-test X-ray images. These packages were inspected under the optical microscope for any abnormalities. Three samples of each solder type / board finish / package type combination were mounted on epoxy and cross-sectioned. They were inspected under Environmental Scanning Electron Microscope (ESEM). Dye and pry analysis was carried out on one sample from each combination.

Post-test X-ray analysis showed no abnormalities in the solder interconnect geometry. Irrespective of the solder paste or board finish used, failures in 256 I/O and 144 I/O BGAs were due to crack propagation at the solder-package interface, as illustrated in Figure 24 and Figure 25. The solder-package interface has the narrowest cross-section in the solder joint due to the effect of gravity during the solder reflow process. Due to the CTE mismatch between the package and the board, thermo-mechanical stress is generated at the solder joint and is the maximum at the solder-package interface as it being the narrowest section. Since the solder paste extends along the periphery of the Non-Solder Mask Defined (NSMD) pads at the board side,

it provides additional adhesion of solder along the circumference known as the "anchorage effect" [22] [35]. The failure sites in this study were similar to those in the literature for thermal cycling at lower temperatures [22][25][36][37].

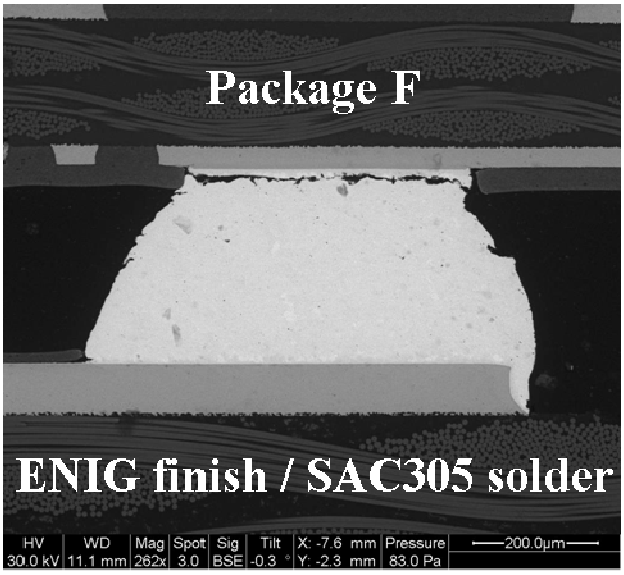

Figure 24. Package side crack on 256 I/O BGA [CTF=1783] (courtesy: CALCE)

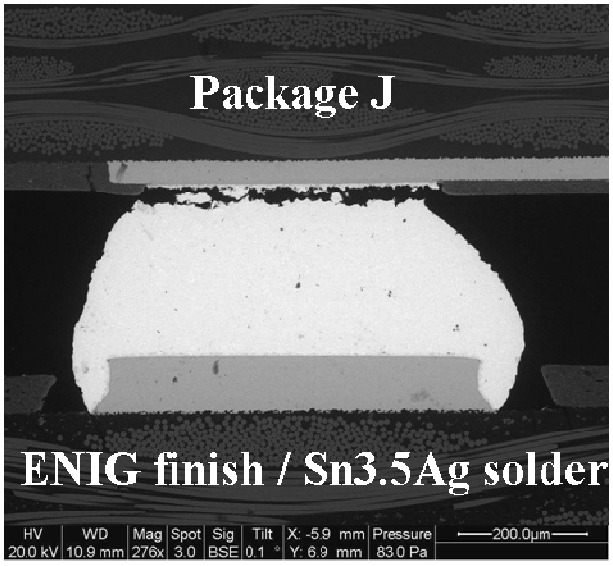

Figure 25. Package side crack on 144 I/O BGA [CTF=1698] (courtesy: CALCE)

The dye and pry process provided a whole-field perspective on failure sites, as shown in Figure 26. As shown in Figure 26, complete cracks were observed on the

corner locations of the outer row of solder joints. The distance from neutral point (DNP) is maximum for solder joints at these locations and therefore have the greatest strain. Complete cracks were also observed in the outer row of solder joints under the die shadow. The presence of dummy die introduces an additional local CTE mismatch and thereby increasing the strain at these locations. The die to package ratio is an important factor in the thermal cycling reliability of BGAs. The new generation CSPs have higher die to package ratio which further lowers the CTE of the package and thus reducing their reliability.

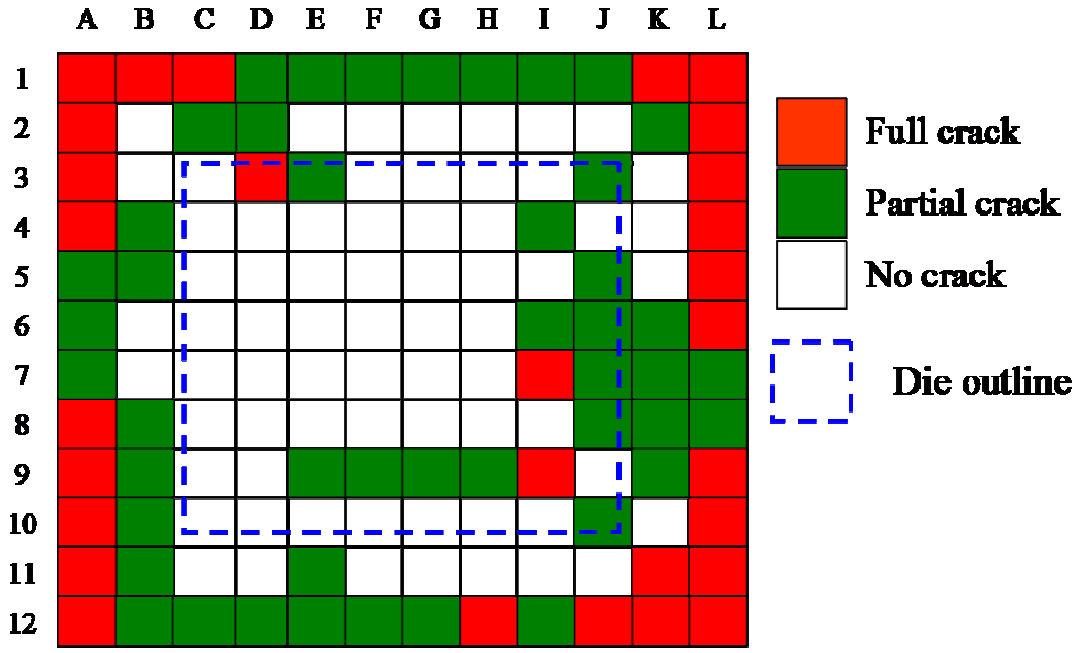

Figure 26. Dye and pry results of Sn based finish Sn3.5Ag solder board – Package E (144 I/O BGA)

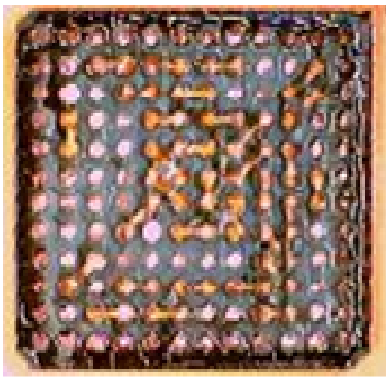

Figure 27. Optical picture of the pried 144 I/O BGA package in Sn based finished Sn3.5Ag soldered board (courtesy: CALCE)

In order to determine the co-planarity of the assembled packages, one 256 I/O BGA and one 144 I/O BGA each was sectioned from all four edges and the solder joint heights were measured. The solder joint height was defined as the distance from the bottom of copper pad at the package side to the top of the copper pad at the board side. Both types of packages were found to be coplanar with no tilt of inclination according to the measured solder joint dimensions.

4.2 Solder mask cracking

Solder mask cracking led to dye penetration onto the board laminate in all the thermally cycled boards during dye and pry process. Solder mask cracking was observed at two locations: 1) between copper traces/pads, and 2) adjacent to the copper pad near solder balls, as shown in Figure 28 and Figure 29. No pad or trace failures were observed in the lateral sections. The solder mask cracking is suspected due to the difference in CTE between the solder mask and the board laminate. During reflow, the solder mask restricts solder exclusively to solder pads and prevents electrical shorts. During field use it protects the board laminate from environmental factors. However, cracks on solder mask can pave the way for moisture ingression.

Moisture can accelerate degradation through corrosion, lower the T_g of board laminate, and assist in conductive anodic filament (CAF) formation and other failure mechanisms under field use conditions.

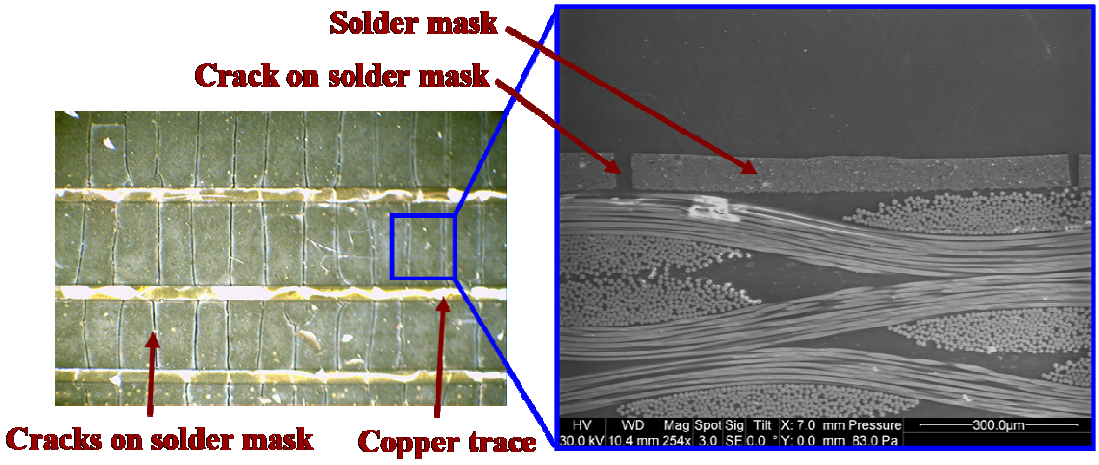

Figure 28. Solder mask cracks on Sn based finished SAC305 soldered board (courtesy: CALCE)

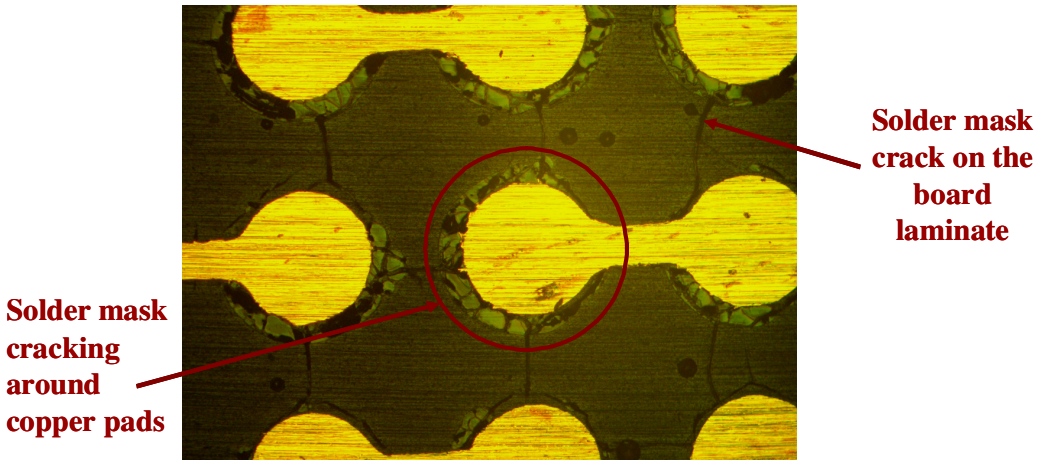

Figure 29. Lateral section of Sn based finish Sn3.5Ag solder Board2 – Package G (256 I/O BGA) (courtesy: CALCE)

4.3 Hourglass-shaped joints

Among the 13 inspected BGAs with hourglass-shaped joint at the corner location, complete cracks were observed only in four cases (Figure 30). In a few

hourglass joints, partial cracks at the package side and micro-cracks at the narrowest section (center) were observed, as shown in Figure 31. The fewer number of full cracks and location of micro-cracks at the center in this experiment were consistent with the results from the literature. FEA simulation of hourglass-shaped joints in the literature [23] showed that the location of highest stress in hourglass-shaped joint (maximum inelastic strain and peak strain density) is in the bulk solder. Cracks can also initiate at the interfaces due to the effect of brittle intermetallics and is not taken into account in FEA simulation. In this experimental study and the experimental study in [23], crack initiation was observed in the bulk solder (Figure 31) and at the interfaces (Figure 30). However, complete cracks were observed at the interfaces due to the brittle intermetallics.

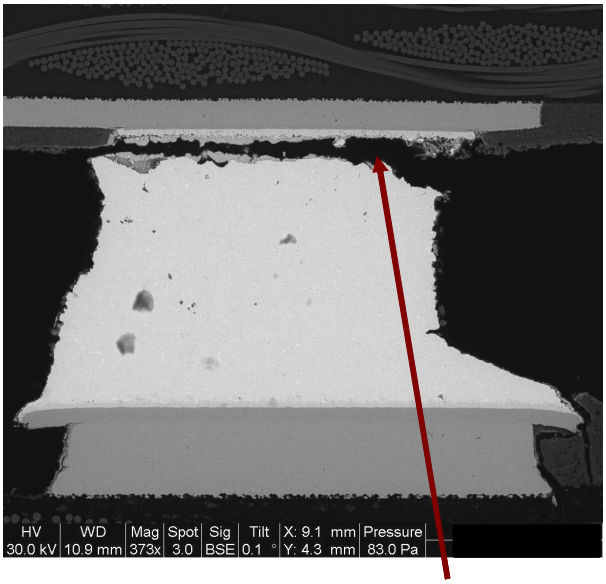

Figure 30. Hour-glass shaped solder joint with complete crack on package side Sn based finish SAC305 solder Board2 144 I/O BGA - Package A [CTF=1114] (courtesy: CALCE)

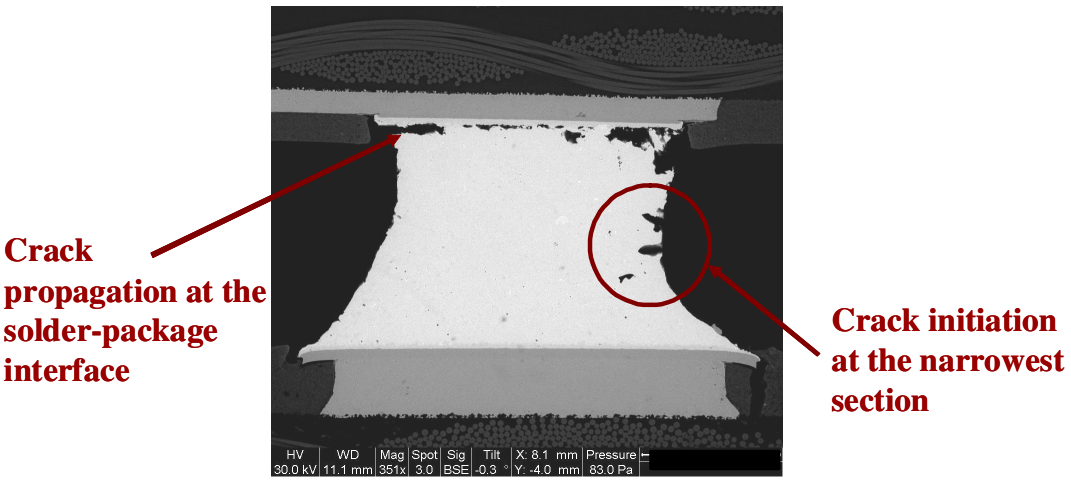

Figure 31. Hour-glass shaped solder joint with partial crack on package side Sn based finish SAC305 solder Board1 256 I/O BGA - Package A [CTF=1697] (courtesy: CALCE)

Chapter 5: Microstructure Analysis

5.1 Introduction

The Kruskal-Wallis test showed that the ENIG finished boards and proprietary Sn-based finished boards performed comparably. The failure analysis showed that the failure site and mechanism were identical in both the cases. In order to further investigate why the two types of board finishes behaved similarly the microstructure of the solder joints were analyzed. Furthermore, Sn-based finished SAC305-soldered 144 I/O BGAs had lower reliability than the rest of the data sets. The dye and pry and cross-sectional analyses showed that the location of failure sites in Sn-based finished SAC305-soldered 144 I/O BGAs was the same as in other data sets. Therefore the intermetallic compound (IMC) composition and thicknesses were analyzed to look for any possible differences.

During reflow, the solder reacts with the finish and pad metals to form the IMCs which ensures a strong metallurgical bond. Prolonged exposure to temperature and time cause these IMCs to grow, and resulting in serious reliability concerns since they are brittle in nature [48]. The IMCs formed in Sn3.5Ag and SAC305 solders with ENIG board finish have been documented in the literature for temperatures up to 175^{o}C [48][49]. In this study, the composition and thicknesses of IMCs formed in Sn3.5Ag and SAC305 solders with ENIG and Sn-based finished BGAs that underwent temperature cycling from -40^{o}C to 185^{o}C were determined. They were compared against the control samples, which were kept at room temperature for a period of 2 years.

One control and one tested sample from each solder type / board finish / package type combination were cut out from the test assembly for micro-structural analysis of the solder joints. The samples were mounted in epoxy and cross-sectioned to the desired finish. The samples were polished with alumina (Al_2O_3) powder and then the solder joint surfaces were etched with a solution containing 5% acid (HNO_3:HCl = 2:1) and 95% ethanol for 5 seconds.

5.2 Sn3.5Ag soldered BGA packages

A Ni layer was observed in between the copper pads and solder joint in all the packages at the board side (Figure 33) and the package side (Figure 35). The Ni_3Sn_4 IMCs formed at the solder-board interface after reflow in ENIG board finished Sn3.5Ag soldered 144 I/O BGA control samples, as shown in Figure 32. Acicular $AuSn_4$ IMCs were observed to be distributed randomly in the solder. Platelets of $(Au,Ni)Sn_4$ phase were seen at the solder-board interface along with Ni_3Sn_4. Another intermetallic compound Ag_3Sn was also observed to be distributed at the Sn-rich phase of the solder. After temperature cycling, the thickness of Ni_3Sn_4 IMCs at the solder-board interfaces increased from 0.5-2 μm to 2.5-6 μm. Ni from the board finish migrated to form $(Au,Ni)Sn_4$ platelets in the bulk solder after temperature cycling loading. These platelets were also found resting on the layer of Ni_3Sn_4. The particle size of Ag_3Sn IMCs increased after the temperature cycling test as shown in Figure 36.

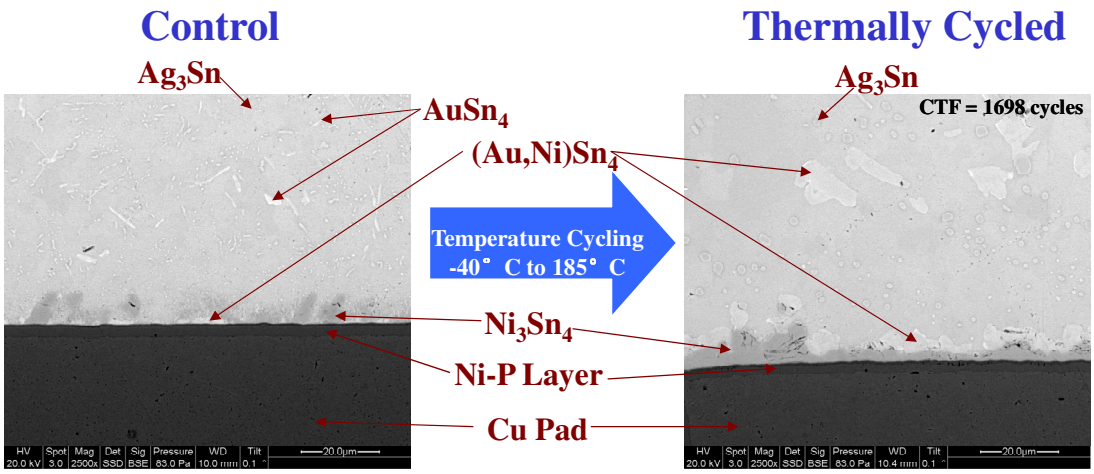

Figure 32. IMCs at solder-board interface in ENIG finished Sn3.5Ag soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

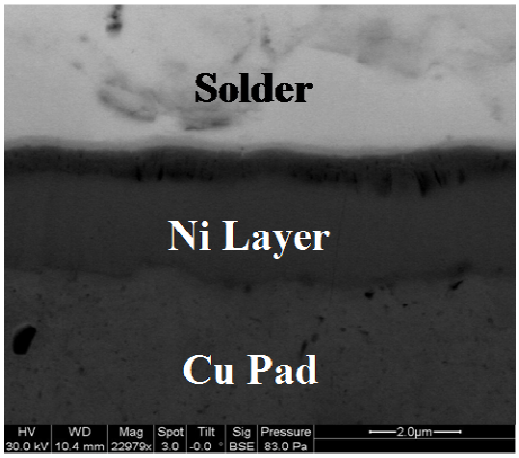

Figure 33. Ni layer at solder-board interface in ENIG finished Sn3.5Ag soldered 144 I/O BGA (courtesy: CALCE)

During failure analysis, it was observed that the failures were due to cracks at the package side. Hence, the microstructure evolution at the package-solder interface was studied. Solder reflow resulted in a layer of Ni_3Sn_4 at the package-solder interface in control samples, as shown in Figure 34. Small pockets of Ag_3Sn intermetallics were observed in the Ni_3Sn_4 layer in control samples. Temperature

cycling resulted in the thickening of the Ni_3Sn_4 layer from 4.5–7 µm to 5-10 µm and the growth of Ag_3Sn IMCs under the Ni_3Sn_4 layer.

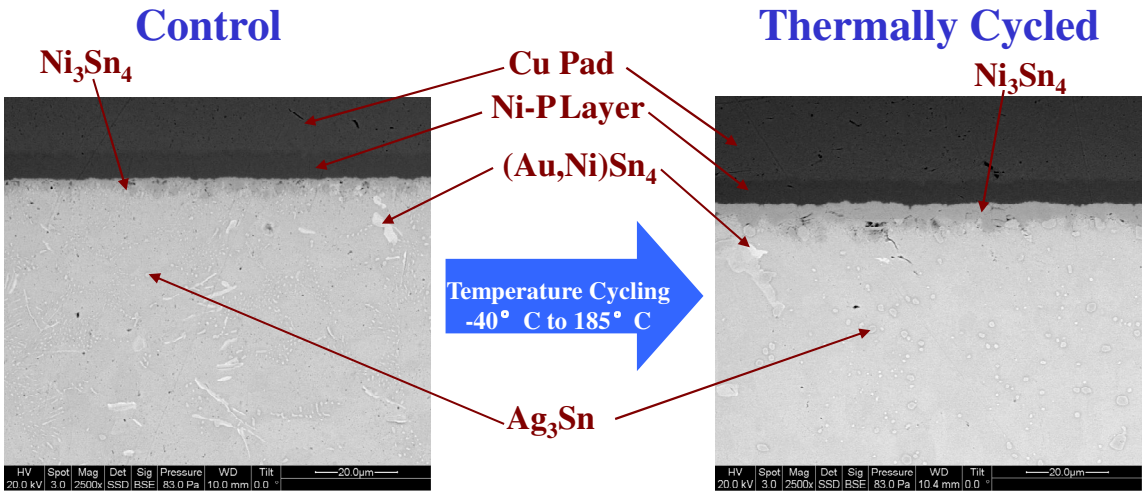

Figure 34. IMCs at package-solder interface in ENIG finished Sn3.5Ag soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

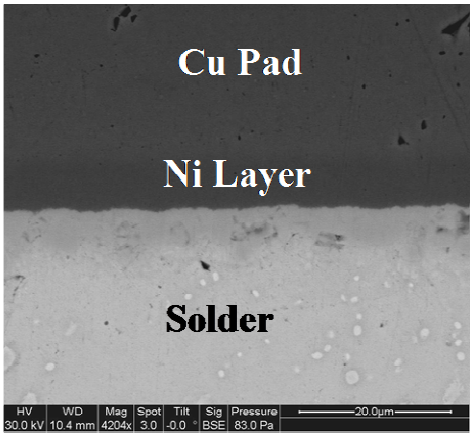

Figure 35. Ni layer at package-solder interface in ENIG finished Sn3.5Ag soldered 144 I/O BGA (courtesy: CALCE)

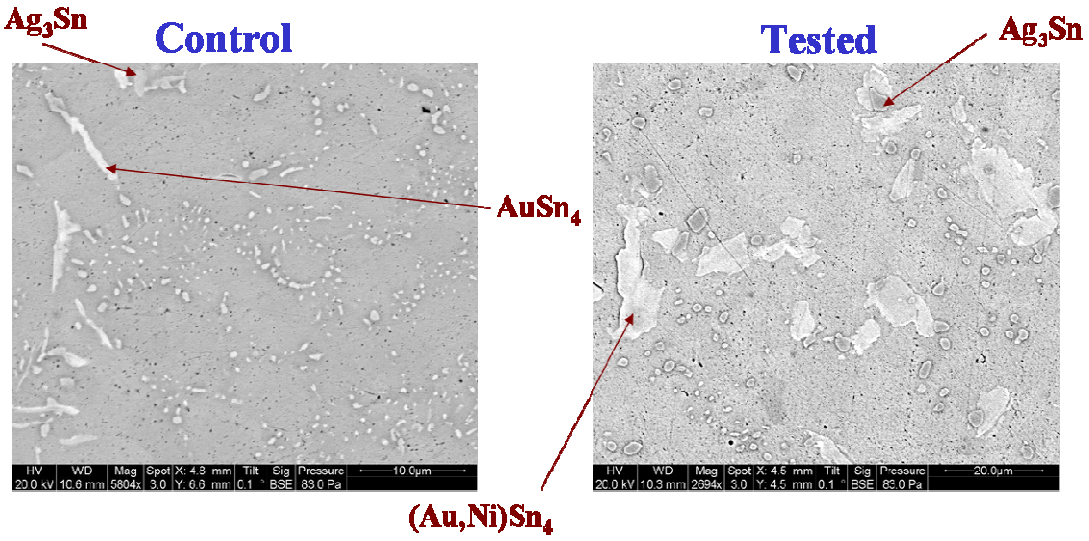

Figure 36. IMCs in bulk solder in ENIG finished Sn3.5Ag soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

5.3 SAC305 soldered BGA packages

In the ENIG board finished SAC305 soldered 144 I/O BGA control samples (shown in Figure 37), the presence of copper in the system resulted in the formation of $(Cu,Ni)_6Sn_5$ IMCs at the interface after reflow. Cu-Sn-Ni-Au phase was observed in the bulk solder and above the $(Cu,Ni)_6Sn_5$ layer. Ag_3Sn IMCs were distributed in the bulk solder in control samples. The thickness of the $(Cu,Ni)_6Sn_5$ layer at the solder-board interface increased from 2.5–6.5 µm to 4.5-13 µm after temperature cycling from -40°C to 185°C. Similar to Ag_3Sn intermetallics found in Sn3.5Ag solder, Ag_3Sn IMCs found in SAC305 solder also grew in size after temperature cycling as shown in Figure 39.

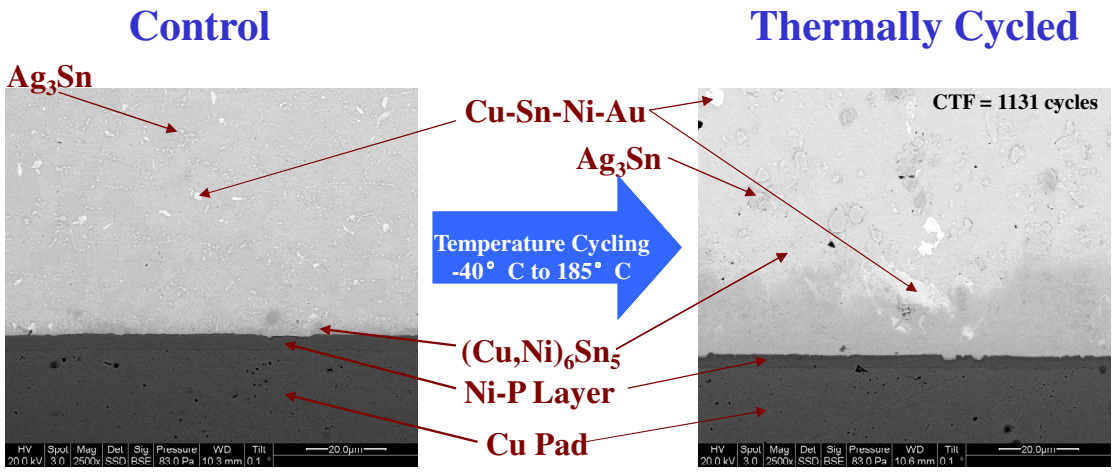

Figure 37. IMCs at solder-board interface in ENIG finished SAC305 soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

At the package-solder interface, $(Cu,Ni)_6Sn_5$ IMCs were observed after reflow. The layer thickness grew from 3–5.5 µm to 5-8 µm after temperature cycling, as shown in Figure 38. Cu-Sn-Ni-Au phase was found below the $(Cu,Ni)_6Sn_5$ layer at the package-solder interface in the control and tested samples.

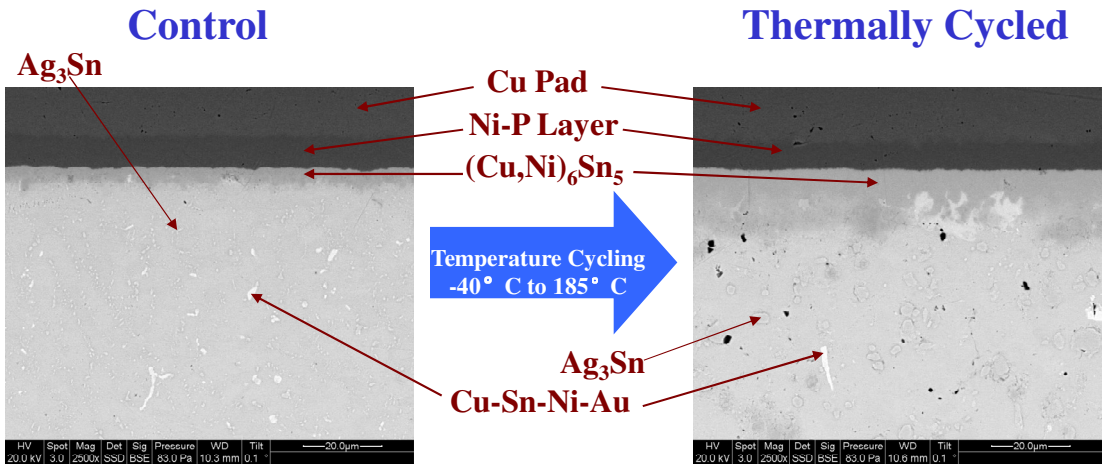

Figure 38. IMCs at package-solder interface in ENIG finished SAC305 soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

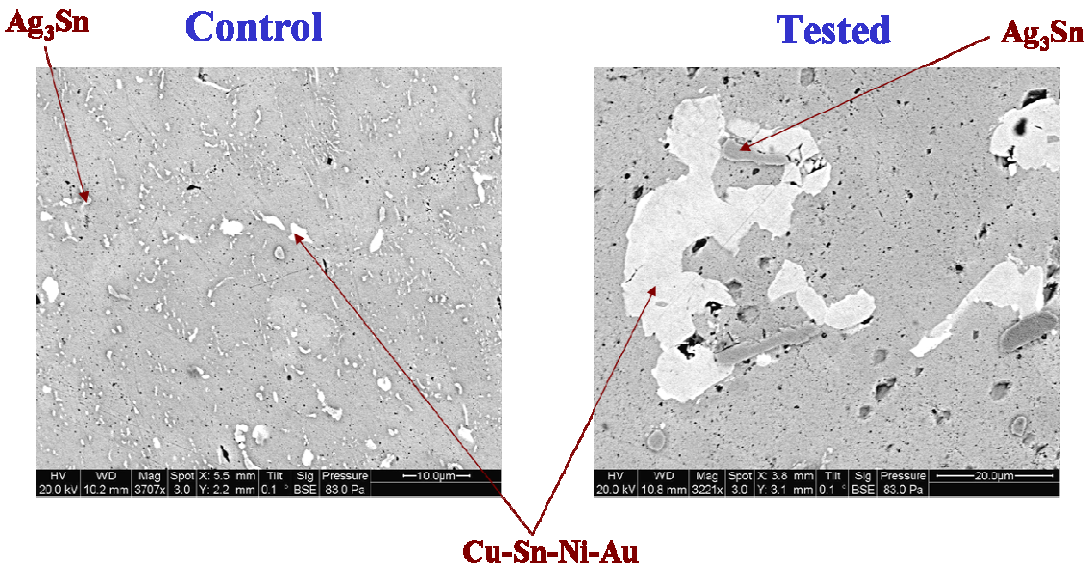

Figure 39. IMCs in bulk solder in ENIG finished SAC305 soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

Identical intermetallics were observed in the Sn-based board finished samples as shown in Figure 40, Figure 41, and Figure 42. The proprietary board finish had a layer of Ni at the solder-board interface. The similarity in the IMCs explains why ENIG finished and Sn-based finished boards had comparable levels of reliability. Compared to studies at lower temperatures the brittle intermetallics were bigger, which can be one of the reasons for lower cycles to failure at 185°C. However, the lower reliability of Sn-based finished SAC305-soldered 144 I/O BGAs could not be explained by microstructure analysis.

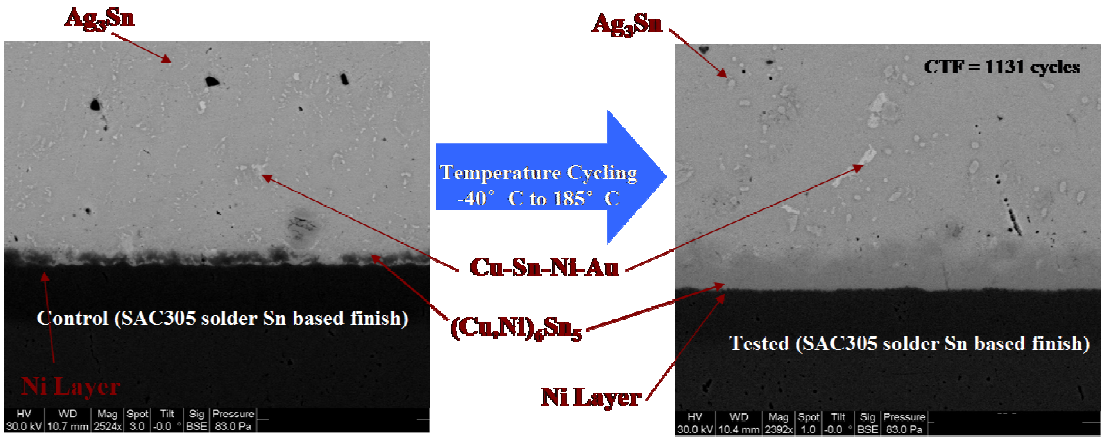

Figure 40. IMCs at solder-board interface in Sn-based finished SAC305 soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

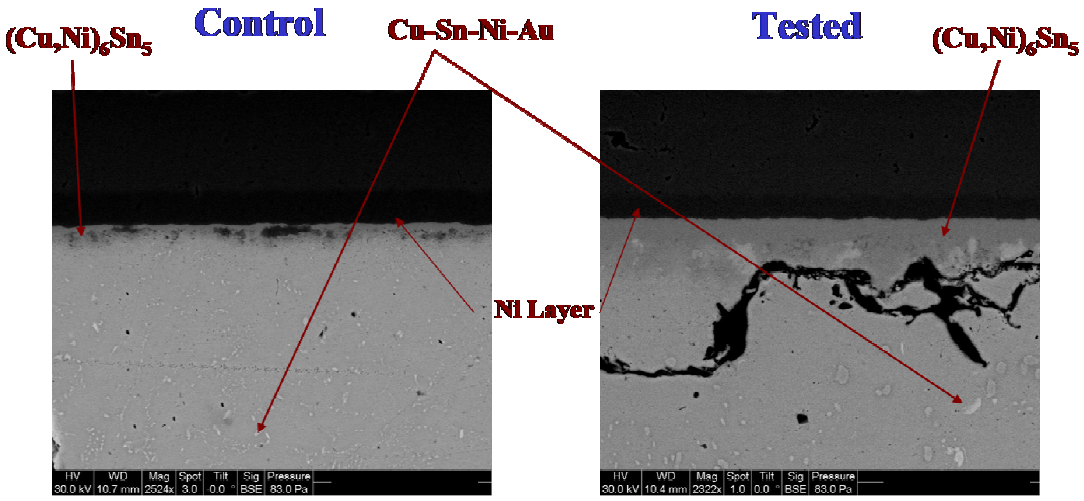

Figure 41. IMCs at package-solder interface in Sn-based finished SAC305 soldered 144 I/O BGA (a) Control (b) Tested (courtesy: CALCE)

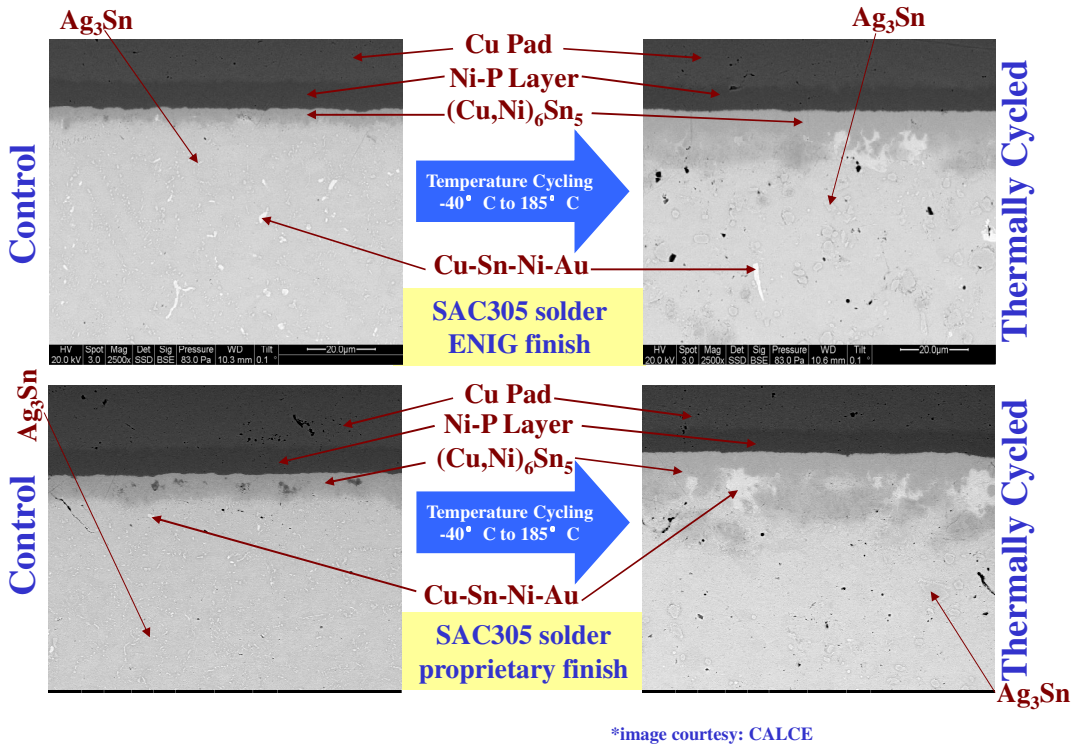

Figure 42. IMCs in ENIG and proprietary finishes at package solder interface (courtesy: CALCE)

Chapter 6: Solder Joint Life Simulation

6.1 Introduction

Previous studies in literature have shown that the fatigue ductility constant in the Engelmaier model is dependent on temperature. In a series of studies by Salmela *et al.* [38][39], it was claimed that the Engelmaier model may lack accuracy in predicting the cycles to failure if it is employed in tests beyond the recommended range (0^oC - 100^oC) mentioned in IPC-SM-785 [28] and IPC 9701A [8]. Since the temperature cycling range in this study is beyond 0^oC - 100^oC, simulation based on Engelmaier model calibrated with lead-free constants and experimental results were compared. This was performed to determine whether the Engelmaier model is valid up to 185^oC. To predict the lifetimes of solder joints under the environmental and operational loads, the test vehicle was modeled using simulation software [40]. The thermal fatigue model for solder interconnects in BGA packages used by the software was based on the Engelmaier model [41] and enhanced with internal calibration [42]. The temperature cycle fatigue model constants for SAC and Sn3.5Ag solders have been previously published for the standard temperature cycling conditions [42]. The estimated cycles to failure from the PoF model was the value for 50% of the components to fail. The Engelmaier model constants were developed for lead-free solders for temperatures up to 125^oC [42]. To determine whether these constants can be used up to 185^oC, the error between model estimate and experimental cycles to failure was calculated.

6.2 PoF model

The printed circuit board was modeled in the software including all the components positioned in the manner shown in Figure 6 with two different solders, SAC305 and Sn3.5Ag. The constants calibrated from previous studies [42] were used by the software for various solder and material properties. Since the PoF model did not consider the effects of the board finish, comparison of the two board finishes was not performed. PoF model evaluations for the QFPs and resistors indicated survival of greater than 30,000 cycles, which could be effectively considered to represent zero failures in the test temperature cycling conditions. The longer life of QFPs was due to the compliant leads. Good agreement (maximum error < 29%) between the simulated results and the experimental results (as shown in Table 8) was observed.

Previous studies have shown that the Engelmaier model is most appropriately used in the temperature cycling range of 0 to 100^{o}C [46]. Engelmaier has reported in his studies that the model does not hold true when large temperature swings are observed [41]. However, the original Engelmaier model [43] was based on the isothermal fatigue data of eutectic tin lead solder by Wild [44]. The caveats mentioned by Engelmaier [28][45] (such as the applicability to small temperature ranges) were based on limited fatigue data of eutectic tin lead solder. To the contrary, lead-free studies at CALCE have shown that Engelmaier model can be effectively used in temperature ranges greater than the ranges defined in the caveats [12]. In the present study the Engelmaier model with constants developed in [42] was used up to a temperature range of 225^{o}C (-40^{o}C to 185^{o}C) within an acceptable error %. Since the error % between the predicted (using Engelmaier model with constants developed

in [42]) and experimental cycles to failure values were low, the same constants defined for lower temperatures [42] can be used up to temperatures of 185^{o}C. Hence, it was not necessary to derive new constants for higher temperatures for the purpose of estimation. The low error % (as shown in Table 8) showed that the Engelmaier model can be used in a wider temperature range than that specified by Engelmaier in his caveat in [28][45]. The applicability to a wider temperature range may be due to the fact that since lead-free solder have higher melting points compared to eutectic tin lead solder, the properties of SAC305 and Sn3.5Ag lead-free solders do not vary significantly over a wide temperature range. The applicability of the Engelmaier model at higher temperatures can be a very useful study for packaging community, as it is well known that the Engelmaier model can provide a quick estimate of cycles to failure for thermo-mechanical fatigue loading.

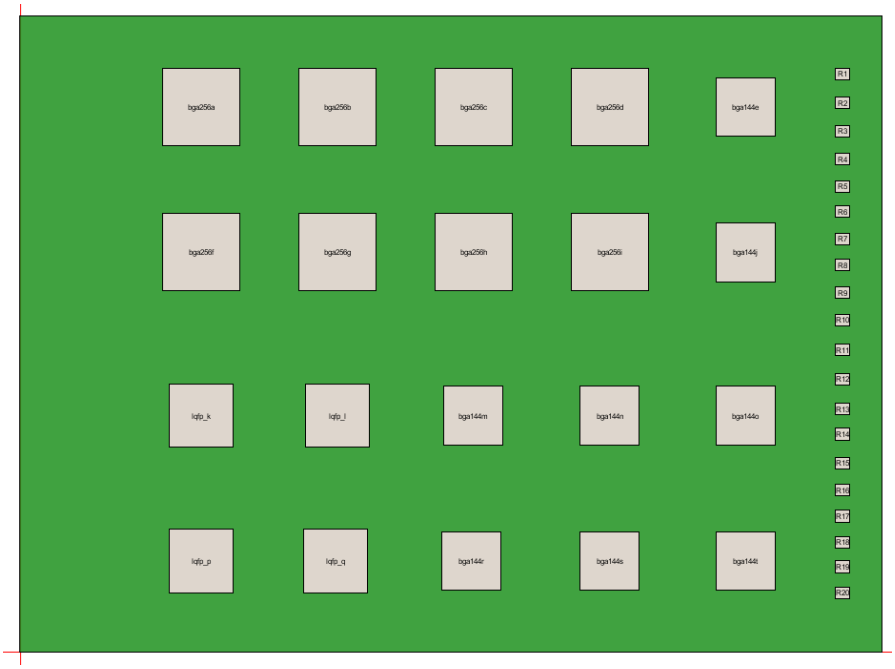

Figure 43. PCB model in simulation software (courtesy: CALCE)

Table 8. Comparison of simulation results with experimental results

Package (BGA)	SAC305			Sn3.5Ag		
	PoF[1]	Experiment[2]	% Error	PoF[1]	Experiment[2]	% Error
256 I/O	1220	1300	6.2	1094	1208	9.4
144 I/O	2226	1729	28.7	1830	1572	16.4

6.3 Effect of board laminate material

Available literature mostly discusses the reliability of lead-free solders on FR-4 board. Hence a direct comparison of the results from this study to the studies in available literature is not valid. A simulation to estimate the cycles to failure for the same packages and solders under the same conditions (-40^{o}C to 185^{o}C) on FR-4 board was carried out using the PoF model (Table 9). This will provide an estimate of the expected reliability if FR-4 boards were used in place of PI boards. Packages on the FR-4 boards were predicted to have lower reliability as the shear strain range on interconnects was greater on FR-4 boards than on Polyimide (PI) boards in the same temperature range due to the higher in-plane Coefficient of Thermal Expansion (CTE) (CTE_{FR4}=17.6 ppm/^{o}C and CTE_{PI}=14.3 ppm/^{o}C) [47]. In order to analyze the impact of board material, a simulation was also carried out for the commonly used test conditions listed in temperature cycling standards (-40^{o}C to 125^{o}C). With all the other parameters and conditions the same as before, when the peak temperature was decreased from 185^{o}C to 125^{o}C there was a considerable increase in cycles to failure. Considerable improvement was observed when a PI board was used. This is evident

[1] calcePWA does not consider the effects of board finish.
[2] Based on Weibull analysis of the cycles to failure data of ENIG finished packages for cycles to 50% failure.

from Table 9 and Table 10. Hence, we can conclude that the selection of a low CTE board is important for high temperature application conditions as it helps in reducing the CTE mismatch between the package and board laminate.

Table 9. Simulation results (-40°C to 185°C) with Polyimide and FR4 board materials

Package type	Board material	Cycles to 50% failure	
		SAC305	Sn3.5Ag
BGA256	Polyimide	1220	1094
	FR4	619	612
BGA144	Polyimide	2226	1830
	FR4	904	846

Table 10. Simulation results (-40°C to 125°C) with Polyimide and FR4 board materials

Package type	Board material	Cycles to 50% failure	
		SAC305	Sn3.5Ag
BGA256	Polyimide	7475	6150
	FR4	3470	3179
BGA144	Polyimide	14760	11040
	FR4	5326	4595

Chapter 7: Conclusions and Contributions

This study reports the high temperature thermal cycling reliability (-40^{o}C to 185^{o}C) of SAC305 and Sn3.5Ag soldered BGAs, QFPs, and resistors with ENIG and an Sn-based proprietary board finish. The tested packages were representative of the commonly used types i.e., area-array, leaded and leadless, in the electronics industry. The cycles to failure of 1% of the packages was between 405-551 cycles for 256 I/O BGAs and 475-715 cycles for 144 I/O BGAs. Therefore, the 256 I/O and 144 I/O BGA packages can be used in high temperature applications which require an approximate life cycle requirement of 400 cycles, for instance, wireline logging applications in oil and gas drilling. The specialized solders used in high temperature applications can be replaced by mainstream solders (SAC305 and Sn3.5Ag) on polyimide boards in applications with temperatures up to 185^{o}C and life requirements of 400 thermal cycles. The shift to mainstream solders and industry standard board finish can result in reductions in material and processing costs, greater availability from suppliers, use of existing reflow and rework process capabilities, widely available literature on material properties, fatigue behavior, and rework capabilities.

Studies in the literature have shown that Sn3.5Ag and SAC305 solder alloys have high mechanical strength with high ductility [50] [51] and perform comparable to each other under thermal cycling up to 125^{o}C. In thermal cycling from -40^{o}C to 185^{o}C also, both lead-free solders performed comparable to each other with no statistically significant difference in durability. Since the ENIG board finished BGAs

performed as reliably as the proprietary Sn-based board finished BGAs, industry can use ENIG finish, which is widely available, instead of proprietary board finishes designed for high temperatures.

In BGA packages, the failures were located at the package-solder interface because it is the narrowest section in a solder joint and hence has the maximum stress. The solder joint at package side is solder mask defined and this results in lower adhesion compared to board side. The failures at the solder joints were due to thermo-mechanical fatigue as a result of the CTE mismatch between the package and the board laminate. The solder mask cracking was observed on all the tested boards, independent of board finish and solder paste. This may be due to difference in CTE between the solder mask and the board laminate. In order to prevent solder mask cracking, the CTE of the solder mask should be close to the CTE of the board laminate.

Very few complete cracks were observed in hourglass-shaped joints. Due to the geometry of hourglass-shaped joint the stress was lower at the package-solder and solder-board interfaces, and resulted in better reliability. Therefore, hourglass-shaped joints can be incorporated at locations with higher strain. The Ni_3Sn_4 IMC formed at the package-solder and solder-board interfaces in Sn3.5Ag soldered packages were similar to those documented in the literature. The Ag_3Sn IMCs were distributed in the bulk solder of thermally cycled solder joints. In SAC305 soldered BGAs, $(Cu,Ni)_6Sn_5$ IMCs were observed at the interfaces. Along with the Ag_3Sn IMCs, a Cu-Sn-Ni-Au phase was also observed in the bulk solder. Similar IMC structures have been documented in the literature. The comparable reliability of ENIG finished and

proprietary Sn-based finished boards was due to the similarity in their microstructure composition and growth.

There was good agreement between the PoF simulation and experimental results. Hence, the Engelmaier model calibrated with lead-free constants can be used to provide a rough estimate to predict the cycles to failure under temperature cycling for temperatures up to 185^{o}C. Further studies need to be carried out to determine the broader applicability of the Engelmaier model under high temperature cycling conditions. Simulation using FR-4 and PI board materials showed that the improvement in reliability under high temperature cycling conditions was due to the use of low CTE polyimide board material. Hence, for high temperature applications, the board laminate should be constructed using PI that has higher Tg and a lower CTE than FR-4 board laminate. The use of lower CTE board laminate can assist in minimizing the CTE mismatch between the package and board.

Contributions

This is the first published study to generate thermal cycling data of mainstream lead-free solders (SAC305 and Sn3.5Ag) for temperatures up to 185^{o}C. The contributions from the analysis of this data are summarized below:

- This study has demonstrated that no statistically significant difference in reliability was observed between mainstream lead-free solders SAC305 and Sn3.5Ag under temperature cycling from -40^{o}C to 185^{o}C.
- High temperature cycling up to a peak temperature of 185^{o}C does not require the use of proprietary high temperature board finish since the commonly

available board finish (ENIG) performed as reliably as the proprietary Sn-based board finish developed for high temperature applications.

- This study established that the failure site and failure mechanism in the BGA packages subjected to maximum cycling temperature of 185^{o}C are similar to those observed at lower temperatures (from literature).
- The Engelmaier model calibrated with lead-free constants was validated for SAC305 and Sn3.5Ag solders under thermal cycling for a peak temperature of 185^{o}C by comparison of PoF simulation and experimental results.

Appendices

Kruskal-Wallis Test

Kruskal-Wallis test is a non-parametric method to test whether two or more independent samples come from identical populations. Since it is non-parametric, it does not require the data to be normal, but instead uses the rank of the data values rather than the actual data values for the analysis. The null hypothesis states that the medians of all the populations are same where the alternate hypothesis states the contrary. In K-W test the data from all populations are ranked (ignoring the population membership) and provides the probability value (p-value) as the output. P-value determines the appropriateness of rejecting the null hypothesis. It ranges from 0 to 1, where 0 indicates that the null hypothesis is false.

Dye and Pry Method

Dye and pry process is used to identify cracks or separations within solder joints. The sample which needs to be analyzed was cut out from the board using a band saw with sufficient allowance to provide space for prying. The sample was dyed using dye penetrant (Dykem 80496© steel red dye) till the complete dye penetration. Once the dye has set-in, the test board is baked on a hot plate at 100°C for 2 hours. The package is pried using pliers and inspected under the optical microscope for the location of cracks. Completely stained fracture surface indicates that the crack was created during test leading to an open circuit. Partial stained fracture surfaces are not failures; and they indicate micro cracks initiated while testing. Fracture surfaces with

no dye stain indicate cracks created during the dye and pry process and are not considered as failed solder joints.

Failure Data

Package ID	ENIG SAC305		ENIG Sn3.5Ag		Sn based SAC305		Sn based Sn3.5Ag	
	Board1	Board2	Board1	Board2	Board1	Board2	Board1	Board2
A	1229	822	1734	912	1697	969	945	726
B	1405	860	973	895	1447	918	895	1219
C	1309	1351	1322	1257	1038	767	809	1677
D	1301	1299	1673	1322	1177	1370	1409	1167
F	1511	1783	1226	1308	1401	1163	855	969
G	1312	879	1171	1075	971	910	1075	1456
H	1511	1511	760	1075	1474	1038	1403	1324
I	1413	1099	991	1466	1265	814	1301	1038

Cross-section Lateral section Die and pry

Figure 44. Cycles to failure 256 I/O BGA packages

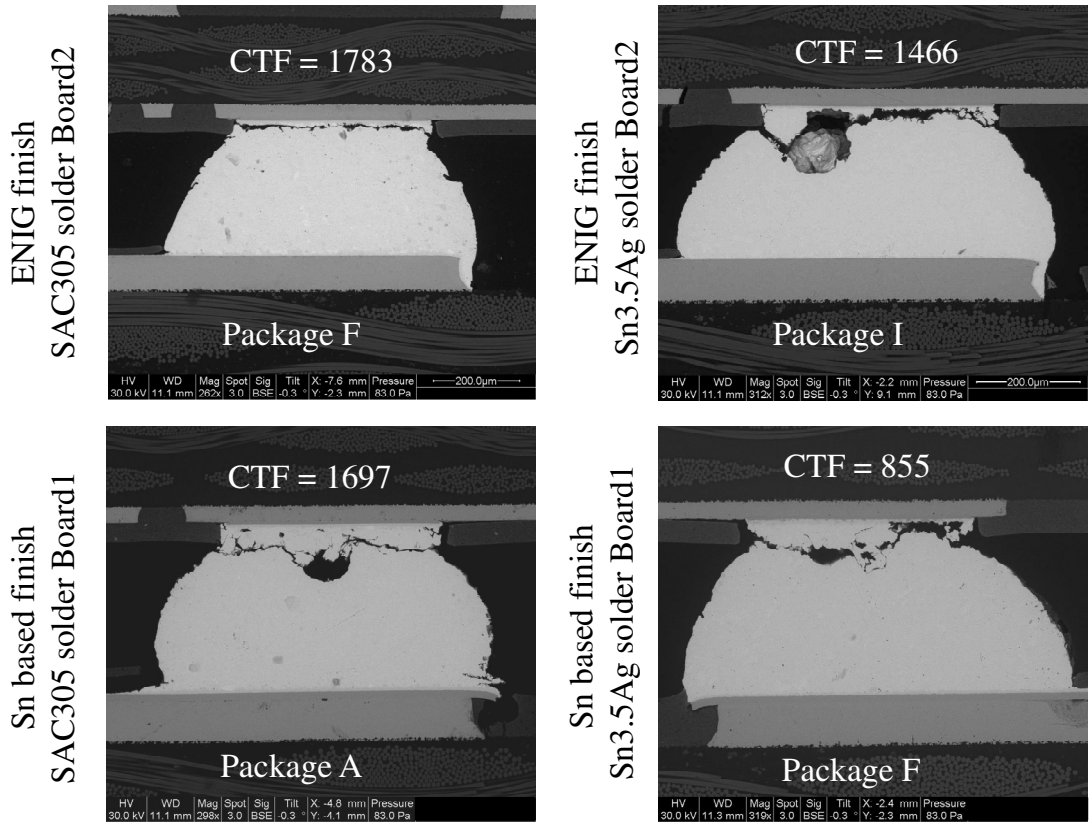

Figure 45. Failure locations in various 256 I/O BGA package types (courtesy: CALCE)

COMPONENT ID	ENIG SAC305		ENIG Sn3.5Ag		Sn based SAC305		Sn based Sn3.5Ag	
	Board1	Board2	Board1	Board2	Board1	Board2	Board1	Board2
E	NF	1411	1848	1524	1275	1114	1992	NF
J	NF	1411	1288	1698	1198	1135	1953	1547
M	NF	1558	1388	1485	1037	1037	1430	1279
N	NF	1358	NF	1439	1037	1153	1075	1615
O	1957	NF	1590	1641	890	1372	1562	1637
R	1754	1131	1120	1589	1037	1053	1120	1490
S	1944	1411	1681	1561	825	1037	1411	1315
T	NF	1251	1588	1583	1037	1037	1411	NF

* NF = Not failed

Cross-section Lateral section Die and pry

Figure 46. Cycles to failure 144 I/O BGA packages

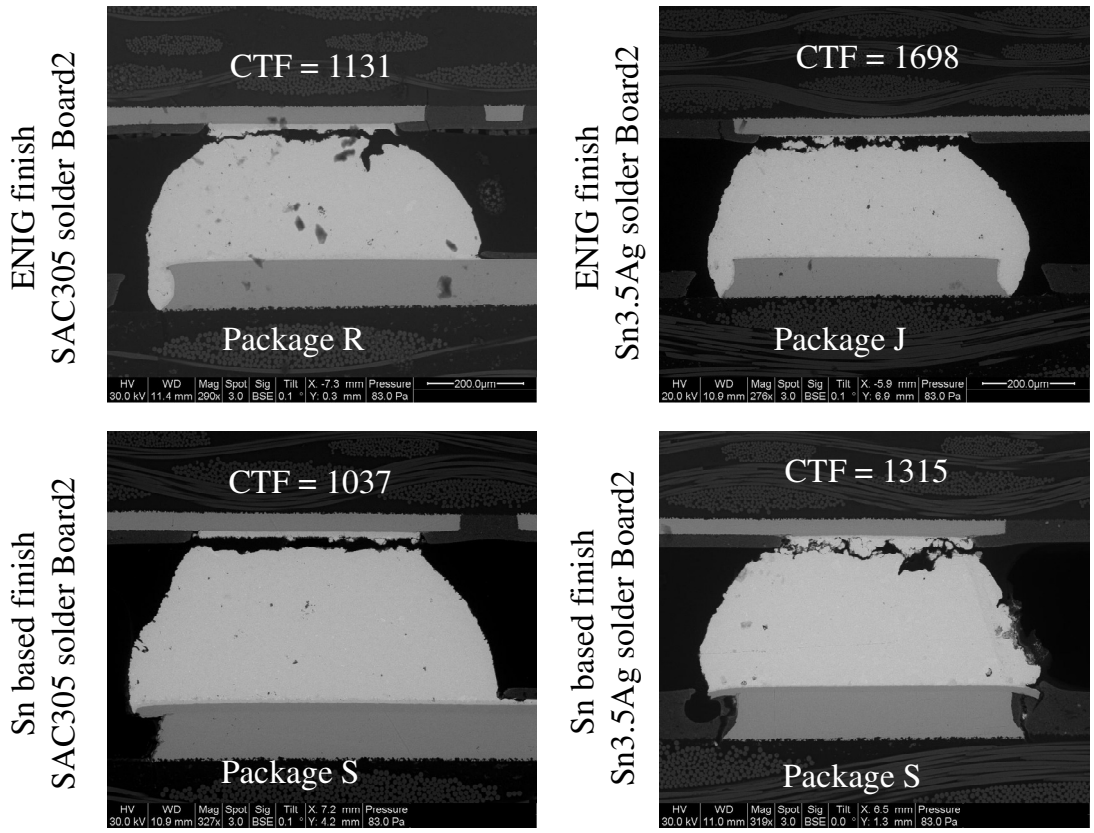

Figure 47. Failure locations in various 144 I/O BGA package types (courtesy: CALCE)

BGA256 - SAC305

COMPONENT ID	ENIG SAC305		Sn based SAC305	
	Bd1	Bd2	Bd1	Bd2
A	0.65	0.43	0.90	0.51
B	0.74	0.45	0.77	0.49
C	0.69	0.71	0.55	0.41
D	0.69	0.69	0.62	0.72
F	0.80	0.94	0.74	0.62
G	0.69	0.46	0.51	0.48
H	0.80	0.80	0.78	0.55
I	0.75	0.58	0.67	0.43
	Mean	0.68	Mean	0.61
	Median	0.69	Median	0.58
	Stdev	0.14	Stdev	0.14

BGA144 - SAC305

COMPONENT ID	ENIG SAC305		Sn based SAC305	
	Bd1	Bd2	Bd1	Bd2
E	0.00	0.41	0.37	0.32
J	0.00	0.41	0.35	0.33
M	0.00	0.45	0.30	0.30
N	0.00	0.39	0.30	0.33
O	0.57	0.00	0.26	0.40
R	0.51	0.33	0.30	0.31
S	0.56	0.41	0.24	0.30
T	0.00	0.36	0.30	0.30
	Mean	0.28	Mean	0.31
	Median	0.38	Median	0.30
	Stdev	0.23	Stdev	0.04

BGA256 - Sn3.5Ag

COMPONENT ID	ENIG SAC305		Sn based SAC305	
	Bd1	Bd2	Bd1	Bd2
A	0.85	0.57	1.17	0.67
B	0.97	0.59	1.00	0.63
C	0.90	0.93	0.72	0.53
D	0.90	0.90	0.81	0.94
F	1.04	1.23	0.97	0.80
G	0.90	0.61	0.67	0.63
H	1.04	1.04	1.02	0.72
I	0.97	0.76	0.87	0.56
	Mean	0.89	Mean	0.79
	Median	0.90	Median	0.76
	Stdev	0.18	Stdev	0.18

BGA144 - Sn3.5Ag

COMPONENT ID	ENIG SAC305		Sn based SAC305	
	Bd1	Bd2	Bd1	Bd2
E	0.52	0.35	0.72	0.41
J	0.59	0.36	0.61	0.39
M	0.55	0.57	0.44	0.32
N	0.55	0.55	0.50	0.58
O	0.64	0.75	0.59	0.49
R	0.55	0.37	0.41	0.38
S	0.64	0.64	0.62	0.44
T	0.60	0.46	0.53	0.34
	Mean	0.54	Mean	0.49
	Median	0.55	Median	0.46
	Stdev	0.11	Stdev	0.11

Figure 48. Total damages in each component when they failed

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