ABSTRACT

Title of Document: MODELING RATE DEPENDENT DURABILITY OF LOW-AG SAC INTERCONNECTS FOR AREA ARRAY PACKAGES UNDER TORSION LOADS

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The thesis discusses modeling rate-dependent durability of solder interconnects under mechanical torsion loading for surface mount area array components. The study discusses an approach to incorporate strain-rate dependency in durability estimation for solder interconnects. The components under study are two configurations of BGAs (ball grid array) assembled with select lead-free solders. A torsion test setup is used to apply displacement controlled loads on the test board. Accelerated test load profile is experimentally determined. Torsion test is carried out for all the components under investigation to failure. Strain-rate dependent (Johnson-Cook model) and strain-rate independent, elastic-plastic properties are used to model the solders in finite element simulation. Damage model from literature is used to estimate the durability for SAC305 solder to validate the approach. Test data is used to extract

damage model constants for SAC105 solder and extract mechanical fatigue durability curve.

MODELING RATE DEPENDENT DURABILITY OF LOW-AG SAC INTERCONNECTS FOR AREA ARRAY PACKAGES UNDER TORSION LOADS

By

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Dedication

To those who have stood by me through all seasons

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I also express my thanks to the students and interns at CALCE, who have been supportive throughout. An extended acknowledgement is available on my facebook profile to express my gratitude in a more explicit manner.

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Chapter 1: Introduction

As portable electronics get more versatile with increased capability with thinner, smaller form factors, the components used to build these devices also need higher processing capability. This has resulted in increased use of area array devices and stacked packages. However, mechanical loads often arise in portable electronics under life cycle conditions. The reliability of area array components under mechanical loads is investigated in this study.

1.1 Problem statement and Objectives

Portables electronics are subjected to a variety of loads in life cycle conditions. These could include mechanical loads resulting from temperature changes (external) or heat generated from operation, and (or) mechanical loads resulting from field conditions such as bend, vibration or accidental abuse (drop) loading on the device (for e.g. transportation and shipping, carrying PDAs or when keys are pressed during operation). Mechanical bends on the device may result in flexure of the PWA in the device. However, based on placement of the component on the PWA and relative position of the supports of the device, the PWA may experience torsion load causing not uniform-flexure in the foot print of the component. While most reliability evaluations on durability of solder interconnects is performed using unidirectional or full reversal bend loads, a board level torsion load is more representative of field conditions. Mechanical torsion has been used to examine the durability of solder interconnects. The quasi static torsion test is performed at significantly lower strain

rates when compared to drop and shock loading while still higher than thermal cycling. The study discusses modeling board level reliability of solder interconnects of area array components under mechanical torsion loading.

Damage model

Current damage models do not account for the changes in material behavior with change in loading rate. Low cycle regime (e.g. thermal cycling) is conventionally modeled using strain-based approach (Coffin-Manson model). High cycle regime (e.g. vibration loading) accounts for elastic damage and is modeled using stress-based approach (Basquin model). Quasi static loads were modeled for Pb-free solder (SAC305) and eutectic SnPb solders were modeled by a combination of the two models in generalized strain-life approach .The damage model constants for SAC105 are determined in this study to understand the behavior of low silver solders.

Strain rate dependency

Material properties (Young's modulus, yield strength) are a function of strain rate and temperature. While the effect on temperature is accounted for in estimating life, the effect of strain rate is often not accounted for while estimating life. One approach to account for strain rate would be to introduce a factor in the empirical damage model. However to implement this approach, literature of failure data at varying strain rates for different strain rates is required. Another approach would be to account for the impact of strain rate on stress and strain determination using finite element analysis. Since, these are used as inputs in the damage model, the final estimate of cycles to failure can capture the impact of strain rate. The solder strain is determined using

strain rate-dependent, elastic-plastic material properties (Johnson Cook model) in the critical interconnect in this study.

Durability of PoP components

With the need for higher processing power in smaller devices, the use of stacked devices in portable electronics has increased. PoP components used in this study consisted of two BGAs configurations stacked on the printed wiring board. It is important to understand the fatigue performance of these devices under board flexure which is more common in life cycle conditions of portable electronics. However, the PoP assembly is not modeled but only tested. Durability of PoP components and BGAs are plotted against the load condition to show the relative performance of the component.

1 2 Background and Motivation

Prior to the RoHS legislation, eutectic SnPb was the solder of choice for most applications. With the advent of RoHS, the tin-silver-copper (SAC) alloy has been the focus of research for replacing tin-lead solder. Early studies focused on 95.5% tin 4% silver 0.5% copper (SAC405) or some similar composition. Later studies focused on 96.5% tin 3% silver 0.5% copper (SAC305). With the conversion imminent, SAC305 appeared to be the preferred lead-free solder [1]. However, mechanical fragility of SAC305 solder joints under drop/shock conditions has resulted in an examination of lower silver content SAC solders [2]. While the reduction in silver appears to improve solder joint reliability under drop/shock, it increased the creep strain under temperature cycling which is expect to reduce solder joint reliability under conditions

of low-strain rate and extended dwells [3].

Literature documents improved interconnection durability of assemblies using reduced-Ag content SAC solder alloys under high strain rate. Results include tests based on drop tests [4-6], high speed bend tests [7], high-speed ball shear [8] and high-speed ball pull [9]. Performance of reduced-Ag SAC solder at high strain rates has been discussed by D. Suh et al [10] and M. Reid [11]. The strain rate commonly observed under these tests at solder level has been described to be in the order of 10^{-2}–10^{-1}με/s [12]. Under high-strain rate mechanical shear loading at board level reduced-Ag SAC has been shown to perform better than SAC305 [13]. While the focus of reduced-Ag SAC solders has been to solve the drop/shock fragility issue, the ability of these new solders to handle low strain rate repetitive cycling has received less attention.

Though reduced-Ag SAC alloys show promise in improving drop/shock fragility, they have a detrimental effect in low strain rate. Available literature on durability of reduced-Ag SAC alloys under low strain rate cyclic loading has been primarily based on thermal cycling tests [14, 15]. The impact of ramp rate (strain rate) in thermal cycling has been discussed by Fan et al [16]. The strain rate under thermal cycling tests at solder level has been estimated to be in the order of 10^{-6}–10^{-5}με/s [17]. As discussed, high strain rate performance of low silver SAC solder joints has been documented [18 - 25] but the low strain rate performance needs further study. Therefore, there is a need to understand board level reliability of reduced-Ag solder joints at low strain rates, especially under mechanical loading. Mechanical torsion has also been used to examine the durability of solder interconnects [19-21]. The strain

rate in solder interconnects under mechanical torsion is estimated to be higher than thermal cycling and lower than drop test for chosen loading conditions. This includes damage models for reduced-Ag solders and failure data to generate these models.

1.3 Literature review

Mechanical torsion tests

Torsion testing on PWAs involves twisting a printed wiring board. The difference in radii of curvature and stiffness between the PWA and packages on the PWA result in shearing of the solder interconnects. Literature [19-21] suggests that torsion loading compares well to Accelerated Thermal Cycling (ATC). The torsion test is used as a qualification test commercially for a variety of products.

Yunus et al. [26] used mechanical torsion tests to evaluate the effect of voids on the reliability of plastic ball grid arrays. In this study, test assemblies were subjected to thermal cycling and torsion testing at elevated isothermal conditions. The load profile of torsion loading, however, was not discussed. Failure criteria used in this study are based on IPC-SM-785 [18]. This was done to allow comparison between thermal cycling and torsion tests.

Ryan et al. [28] performed an evaluation of lead-free solder and compared it with a baseline of SnPb solder. The test determined that lead-free solder had higher durability than SnPb solder. The load profile for the torsion test was a 480-second cycle duration with 180-second dwell periods at either extreme. A 7° twist amplitude was applied to the test sample.

Yee et al. [29] compared different surface finishes on copper such as SnPb coating,

NiAu coating, white Ni coating, silver coating and organic coating. The authors make special mention of the test duration of torsion tests in comparison to accelerated thermal cycling and its advantages for relative comparisons in an expedited manner. Organic solderability preservative (OSP) coating was found to be the better performer on a relative scale.

Filho et al. [30] demonstrated the use of torsion testing as an industrial tool. The test was used to evaluate the reballing process and solder paste volume's impact on reliability. No reduction in reliability was observed as a product of reballing with SnPb or lead-free solder when compared to original assemblies. Solder paste volume was analyzed and a degradation in performance was observed as a result of heterogeneous mixtures in solder paste. Again, the test method's advantage as a comparative tool has been discussed.

Haiyu Qi et al. [24] used torsion loading to generate high cycle fatigue for lead-free plastic ball grid arrays (PBGAs) populated on laptop motherboards. The study focused on determining the strain field for a commercial product, assessing the performance of lead-free solder and finally generating a generic high-cycle fatigue model. A combination of numeric analysis and experimental work was used to arrive at the generalized model based on a Coffin-Manson strain-life model.

Apart from these experimental approaches, analytical studies have been performed to determine damage through bending and torsion loads. Engel et al. [31, 33] discussed torsion loads for leaded packages using an analytical approach. This approach was later validated for leaded components through experiments [33].

Fatigue damage models

Stress based approach:

Basquin damage model, also called stress-life approach, correlates stress amplitude to cycles-to-failure in a power law form using two temperature-dependent material constants, fatigue strength coefficient and fatigue damage exponent. These constants are usually empirically determined [34] [35]. The Equation is listed in Equation 1:

$$N_1 \sigma_1^{\ b} = C \qquad \textbf{Equation 1}$$

where,

C is the fatigue strength coefficient,

b is the fatigue damage exponent.

This approach is suitable for application with high cycle fatigue at constant stress magnitude under completely reversed cyclic loading. The analysis and estimation of temperature dependent material constants in this relationship are easy to determine and allow for expedited life calculations. However, the approach has reduced accuracy for solder life predictions wherein solder experiences elastic and inelastic deformations (including time independent “plastic deformation”, and time-dependent “creep” deformation) for instance under thermal cycling loads.

Strain based approach:

The Coffin-Manson model, also called strain approach, can be expressed as Equation 2 [36] [37]. Here, the completely reversed plastic strain range relates to cycles- to-failure, again in a power law relationship using two temperature-dependent material constants (fatigue ductility coefficient and fatigue ductility exponent) that are

determined empirically.

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma_p}{2\varepsilon_p}\right)^{1/c}$$ **Equation 2**

where,

c is the fatigue ductility exponent,

εf is the fatigue ductility coefficient.

The Coffin-Manson model is typically used in applications such as thermal cycling. This approach is suitable for applications where the plastic damage is the governing factor in damage. This leads to shorter life expectancy commonly referred to as low cycle fatigue.

Generalized strain-life approach:

Combining the elastic strain-life (Basquin's model) and plastic-strain life (Coffin-Manson model) results in the generalized strain-life model that correlates the total strain range (sum of elastic and plastic strains) to cycles to failure. Equation 3 gives the formula for this approach.

$$\frac{\Delta\gamma}{2} = \frac{\Delta\gamma_e}{2} + \frac{\Delta\gamma_p}{2} = \frac{\sigma_f}{E}\left(2N_f\right)^b + \varepsilon_f\left(2N_f\right)^c$$ **Equation 3**

where,

$\Delta\gamma$ is the total strain range,

$\Delta\gamma_e$ is the elastic strain range,

$\Delta\gamma_p$ is the plastic strain range,

E is the modulus of elasticity,

σ_f is stress strength coefficient,

b is the fatigue strength exponent,

c is the fatigue ductility exponent, and

ε_f is the fatigue ductility coefficient.

The generalized strain-life model reduces to Coffin-Manson model at large amplitudes of strain and reduces to Basquin model at small strains. Also, certain modifications can be made to the generalized strain-life model to be sensitive to means stresses when the loading is not completely reversed.

However, the strain based approach cannot account for time-dependent effects (i.e. strain rates, creep damage and so on.) and is insensitive to temperature effect. However, the ease of extraction of model constants, availability of experimental data and ease of use for solder makes this approach very popular. In this study, the generalized strain-life model is used to predict cycles to failure and strain rte dependency is incorporated using finite element analysis while predict solder strains.

Other damage models include energy based techniques which correlate damage from the area of a hysteresis loop to the fatigue life using a power law relationship. These techniques are not discussed in this study due to their relative complexity but are documented by Lee et al [39].

Lead-free solder material properties

Literature on board level reliability tests performed on solder interconnects often report board strains measured using strain gages. However, while modeling solder fatigue performance, solder strain has to be determined. Finite element analysis is often used to determine solder strain. Defining solder material properties is a crucial

aspect of finite element analysis. Solder mechanical properties are temperature and strain-rate dependent. Also, solder has a low homologous temperature, it displays creep phenomenon at relatively low temperatures. Shetty proved that creep damage can be neglected at strain-rates greater than 0.05 sec^{-1} [40]. Hence, in this study, impact of creep is neglected. However, the effect of strain rate has been well documented during both material testing [41] and board level testing [42]. Different approaches to modeling solder in finite element analysis such as elastic, elastic-plastic strain-rate independent and elastic-plastic strain-rate dependent properties (using Johnson-Cook model) are discussed in this study.

Package on package

Package on package (PoP) technology involves vertical stacking of two or more packages to allow better density. PoP configurations typically involve stacked memory chips or integrated memory and logic chips. Memory chips conventionally require fewer IOs when compared to logic chips. For this reason standard configurations involve a low pitch (high density) package with processor on the bottom package and the higher pitch (low density) package with the memory chips (stacked or otherwise) on the top package. Ball grid array (BGA) packages are traditionally used in PoP applications due to their high IO density and reliability [43-45]. A schematic of a BGA package on package is shown in Figure 1.

Figure 1: Package on package technology

Some of the advantages of package on package technology are more efficient utilization of board space, easier routing and lower transmission time between processor and memory chips, better electrical performance with lower noise [43]. In chip scale packages, it is not possible to test the dies individually before stacking. However, in PoPs only "known good" packages can be used since the memory and logic packages can be tested separately and then assembled. This results in improved yields for the stacking process. PoP technology has gained quick acceptance in the cell phone and mobile computing market [46]. Literature on PoP components discusses reliability under thermal fatigue loads (thermal cycling) and overstress loads (drop/shock loading) due to their increased use in mobile devices. It is important to understand the fatigue performance of these devices under board flexure which is more common in life cycle conditions of portable electronics.

1.4 Overview of the thesis

Chapter 2 presents the test setup, test vehicle and monitoring setup used in this study. A detailed description of the components tested and solder compositions is provided in this Chapter. Also preliminary characterization of bare boards is discussed.

Experimental information on the exploratory stress tests performed on BGAs assemblies under multiple loading conditions to isolate accelerated load profile is

discussed in Chapter 3. Test matrix used and failure analysis are also summarized. The post processing of failure data for the two sets of test is presented. Also, the failure data from exploratory stress test used for model constant determination for SAC105 solder is discussed. Results from accelerated life test for BGA and PoP assemblies are presented here along with a comparison on their respective durability.

Chapter 4 presents finite element modeling techniques used in this study. Different material modeling approaches are discussed. The strain range extraction due to two different loadings was then calculated.

Damage modeling using the generalized Coffin-Manson approach using different material modeling strategies for SAC305 test vehicle is discussed in Chapter 5. Also, damage model constants for SAC105 are extracted in this Chapter.

Contributions of the thesis and suggestions for future work are listed out Chapter 6.

Chapter 2: Test Setup

Torsion tests can be conducted using different systems. Torsion tests could be conducted with special fixtures in a universal material test system. Another approach would be to construct specialized torsion test system. The PWA is fixed by clamps and subjected to repetitive cyclic load through defined angles of rotation or torque. These two approaches are shown in Figure 2. Since no standard is available, characterization of the test system has to be performed before board design. A thorough characterization was performed using bare board and is discussed in the appendix.

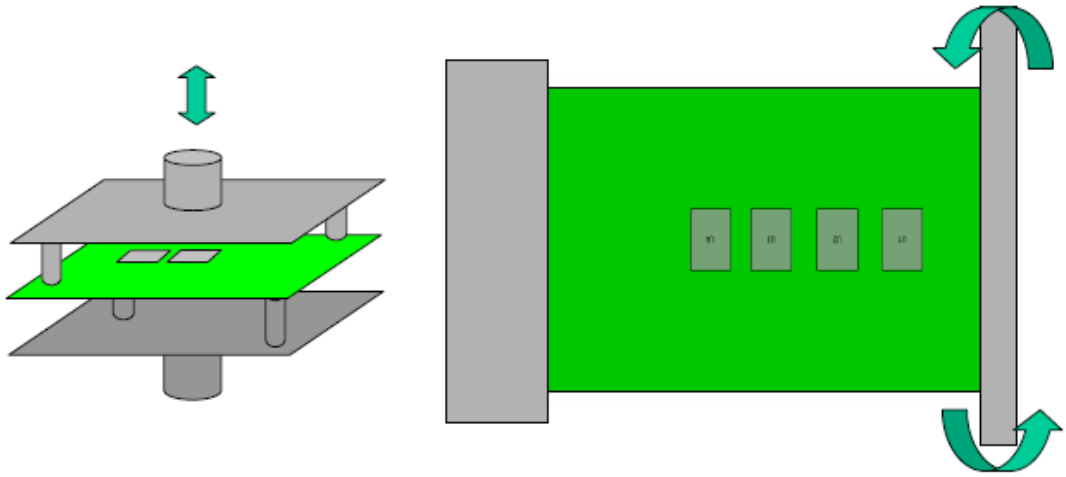

Figure 2: Approaches to performing torsion tests

2. 1 Test setup

The experimental setup involved a torsion tester apparatus, data acquisition systems to monitor resistance and strain from the PWA. The torsion tester apparatus is equipped with one static platform and one rotating platform. The setup can perform

displacement or torque controlled tests. The loading was controlled by peak angular displacements at fixed angular velocity and angular acceleration. The thickness of the printed circuit board is taken into consideration and necessary changes were made to ensure that the axis of rotation passes through the center of the test vehicle. The setup is shown in Figure 3.

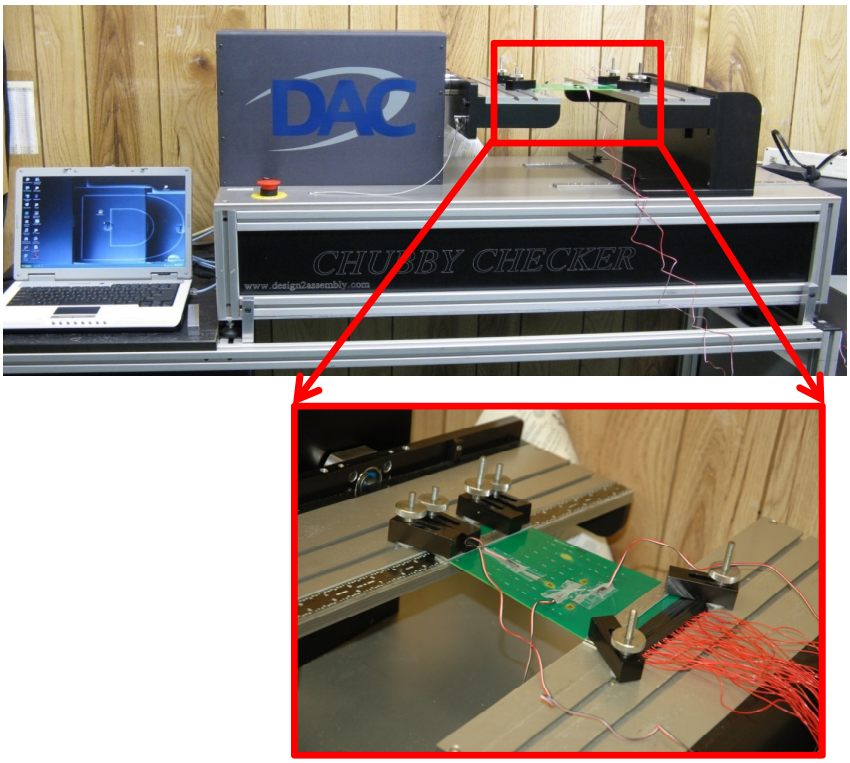

Figure 3: Torsion test setup

Resistance monitoring of daisy chained components was performed using an Agilent 34970A data acquisition/ switch unit and controlled using Bench Link data logging software. Additionally, board strain was measured at select location to ensure board loading was consistent throughout the duration of the test. Strain monitoring was performed using NI-SCXI-1000 Housing with a NI SCXI-1520 universal strain gage input module and NI SCXI-1314 terminal block. Board strain was monitored using

Vishay 062LW-C2A strain gages with a nominal strain of 350Ω.

2.2 Test vehicles

Printed circuit boards of dimensions 8” ×4.5”×62mils made of Polyclad 370HR and organic solderability preservative (OSP) board finish was used. The board was designed with placement options for eight packages into two clusters with quarter board symmetry. These clusters are designated as outer and inner components, as shown in Figure 4.

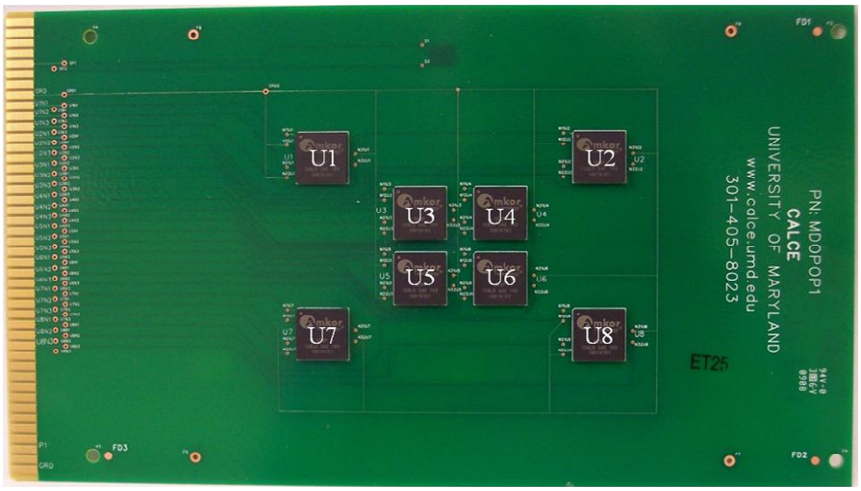

Figure 4: Test vehicle

Three packages were used in this study: 128IO BGAs, 305IO BGAs and PoP components assembled by stacking afore mentioned BGA configuration. A detailed description of the packages is provided in this section. A consistent reflow profile was used for all test vehicles with SAC305 solder paste. The reflow profile for the SAC305 solder has been shown in Figure 5 with thermocouples (T1, T2 and T3) at locations U2, U4 and U7.

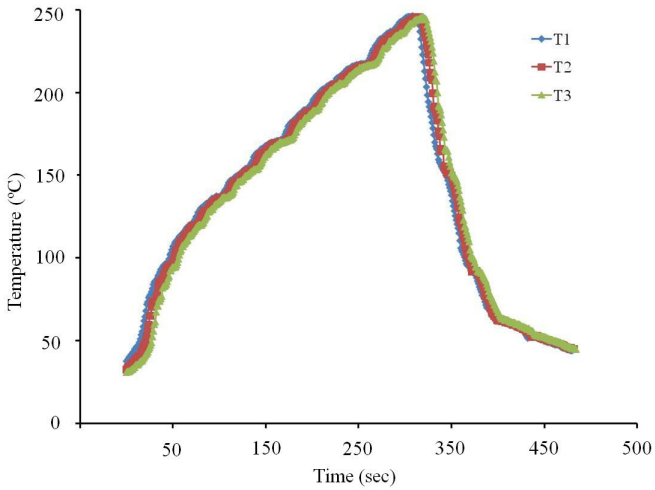

Figure 5: Reflow profile for SAC305 solder paste

The components used in this study were:

a. 128 IO peripheral BGAs (12x12 mm) with a pitch of 0.65 mm in two outer rows and columns of an 18×18 array. Each BGA formed two independent electrical resistance paths that include board and package metallization as well as the solder interconnects. The first electrical resistance (net N2) path included the 12 corner balls (3 balls × 4 corners) and the second electrical resistance path (net N3) included the remaining 116 balls. Both electrical paths were monitored in-situ for each package during the applied test loading condition. The daisy chain layout and X-ray image are shown in Figure 6. The standoff height of the solder interconnect was 0.3 mm. These packages contained two dummy dies stacked to represent conventional memory applications. The bottom die in this configuration had a side of 5.9 mm and thickness of 0.07mm while the stacked die had a side of 4.7 mm and thickness of 0.07 mm. BGA packages were procured with either SAC105 (98.5%Sn + 1.0%Ag + 0.5Cu) or SAC305 (96.5%Sn + 3.0%Ag + 0.5%Cu) solder spheres.

Since SAC305 solder paste was used for all assemblies, the final composition for the SAC105 solder joints would include a higher Ag content than solder sphere composition.

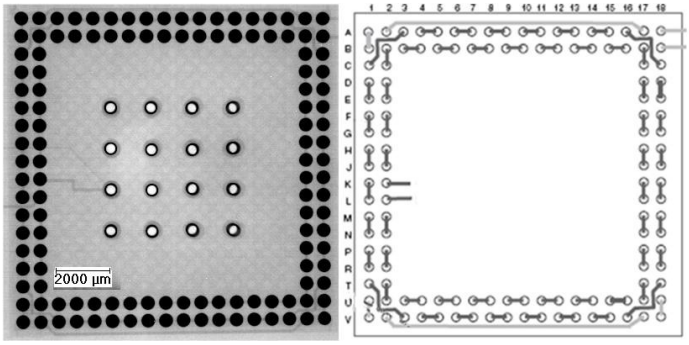

Figure 6: X-ray and daisy chain layout of 128 IO BGA package

b. 305 IO peripheral BGAs (12x12 mm) with a pitch of 0.5 mm in four outer rows and columns of an 23×23 array. Each BGA formed a single electrical resistance path that includes board and package metallization as well as all the solder interconnects (net N1). The daisy chain layout and X-ray image are shown in Figure 7. This daisy chain was monitored in-situ for each package during the applied test loading condition. The standoff height of the solder interconnect was 0.2 mm. These packages contained a single die to represent conventional processor applications with a side of 6.3 mm and thickness of 0.1 mm. BGA packages were procured with either solder spheres of SAC125Ni (98.25%Sn + 1.2%Ag + 0.5%Cu+0.05%Ni) or SAC305. Since SAC305 solder paste was used for all assemblies, the final composition for the SAC125Ni solder joints would include a higher Ag content than solder sphere composition.

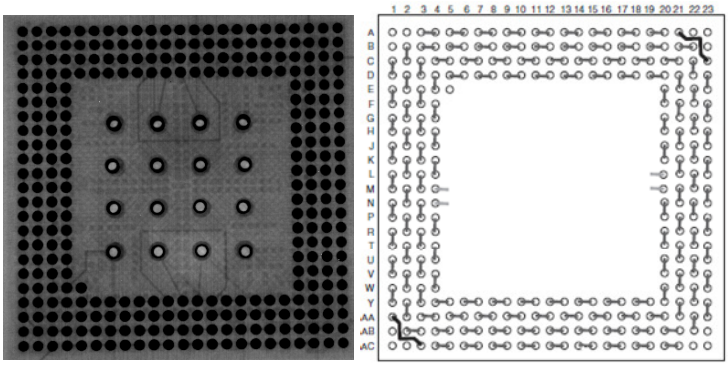

Figure 7: X-ray and daisy chain layout of 305 IO BGA package

c. PoP components (12×12 mm) were used in this study. The top package in the configuration consisted of a peripheral 128 IO BGA package and bottom package used a peripheral 305 IO BGA package. Top-down and oblique views using X-ray were captured and shown in Figure 8. As assembled PoP packages had three daisy-chained nets (nets N1, N2 and N3 as described above) that allow continuous resistance monitoring during test. The two daisy chains from the top BGA were routed down to the PWB through solder interconnects on the interior of the bottom BGA. The daisy chain layout and cross-sectional view are shown in Figure 9. The three nets were monitored independently during testing to allow identification of the first daisy chained net to experience failure in the package.

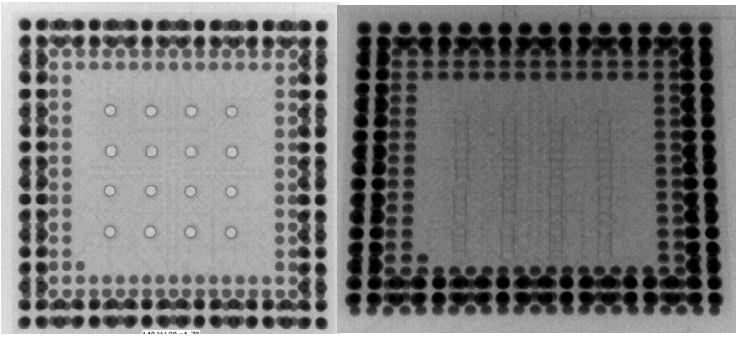

Figure 8: Top down and oblique X-ray images of package on package

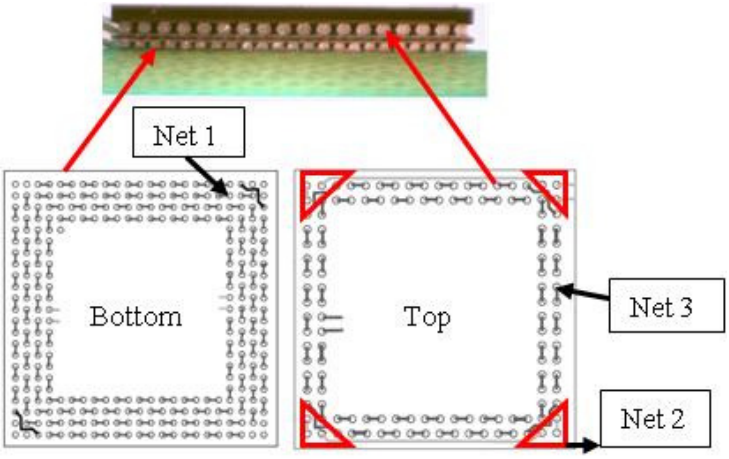

Figure 9: Cross-sectional view and schematic of daisy chain nets

Test vehicles assembled with stand alone BGA components will be referred to as "125BGA-xxx" and "305BGA-xxx". The prefix to the BGA refers to IO count and suffix 'xxx' refers to the solder composition of the solder sphere. For example, a 128 IO BGA with SAC305 solder sphere will be referred to as 128BGA-305. Similarly, PoP components are referred to "PoP-305".

All test vehicles were pre-conditioned at 100°C for 24 hours prior to testing. Preconditioning was intended to stabilize microstructure of the solder interconnects and provide a common starting point for the tests. Static resistance readings were taken before/after preconditioning and no differences were observed. All boards were

x-ray inspected prior to testing and no defects were observed.

Chapter 3: Stress Tests and Data Analysis

3.1 Stress level determination

No standards are available for torsion testing in the electronics industry to provide guidelines on test parameters such as component placement and load levels. Hence, load profile to generate fatigue induced solder interconnect failures was experimentally determined.

Load Matrix

All tests were performed on 128BGA-105 test vehicles. A total of four identical test vehicles were tested at four different load conditions. Two different amplitudes (7.5° and 4.5°) were selected at two different twist rates (60°/sec ; 60°/sec^2 and 1°/sec ; 1°/sec^2). These load levels were selected to generate fatigue-driven failures at primarily the second level solder interconnects. The four load conditions selected for this study are tabulated in Table 1 along with the labels. Also tabulated are the corresponding board strains for these profiles.

A component was considered to have failed once one of the two daisy-chained nets satisfied the defined failure criterion. The failure criterion selected was as per IPC-9701 [26]. An increase in nominal resistance by 20% for five successive cycles was defined as failure. The cycles to failure were fit into Weibull 2-Parameter distributions to obtain characteristic life (η) and shape parameter (β) for ease of comparison. These results are tabulated in Table 2.

Table 1: Load Matrix

Label	Test Profile		Strain Profile	
	Amplitude (°)	**Time Period (seconds)**	**Strain range (μstrain)**	**Strain rate (μstrain/s)**
A	7.5°	≈3	≈1700	≈1000
B	7.5°	≈30	≈1700	≈100
C	4.5°	≈2	≈1000	≈1000
D	4.5°	≈20	≈1000	≈100

Data Analysis

Each test vehicle had four outer components and four inner components. Cumulatively, sixteen components at inner and outer locations were tested. In 11 out of the 16 outer components, the first electrical path (net N2) failed first. In 12 out of 16 inner components, the second electrical path (net N3) failed first. Therefore, the predominant first failure site was net N2for outer components and net N3 for inner components.

Table 2: Weibull parameters for stress determination

Label	Outer Components		Inner components	
	η	**β**	**η**	**β**
A	1360	21.2	1270	8.0
B	1060	7.7	910	11.8
C	9280	2.5	7020	11.6
D	7970	8.8	4740	8.3

Figure 10 shows the impact of placement on durability. A difference in durability is

observed between BGA packages of inner components and outer components, especially in sample D. This result is best explained by findings reported by Wong *et al.* [47]. Most studies obtain a transfer function between the measured strain on the PWA adjacent to the component and the maximum solder stress. However, this study considered the magnitudes of the PWA strain along the four sides of the component (symmetry of flexure) and the corresponding maximum solder stress. The paper reports that the magnitude of the maximum stress at the solder joints was 50%–90% during instances of asymmetric flexure when compared to that of symmetric flexural loading.

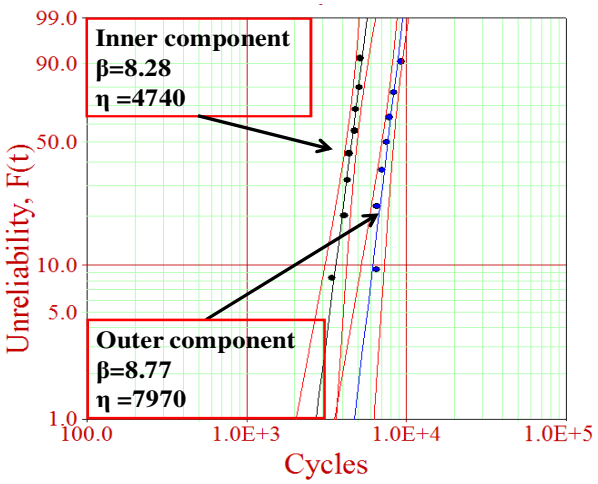

Figure 10: Impact of location on test vehicle D

For the test vehicle in this study, the flexure is more symmetric in inner components when compared to outer components. The symmetric curvatures resulted in higher stresses in the solder joints leading to shorter durability in spite of comparable board shear strain. This was confirmed using finite element analysis, as discussed in the finite element analysis section.

Figure 11 shows the impact of strain rate and placement for a specific strain range of 1700 µstrain units from test vehicles A and B. The durability was higher at quicker rate of loading. It is well documented that the elastic modulus increases with increase in strain rate and decreases with increase in temperature. This has been documented specifically for SAC alloys by Luhua Xu *et al* [41]. Hence for the same strain range, a higher stress is generated at the solder joints. It was observed consistently that outer components had a higher durability than inner components.

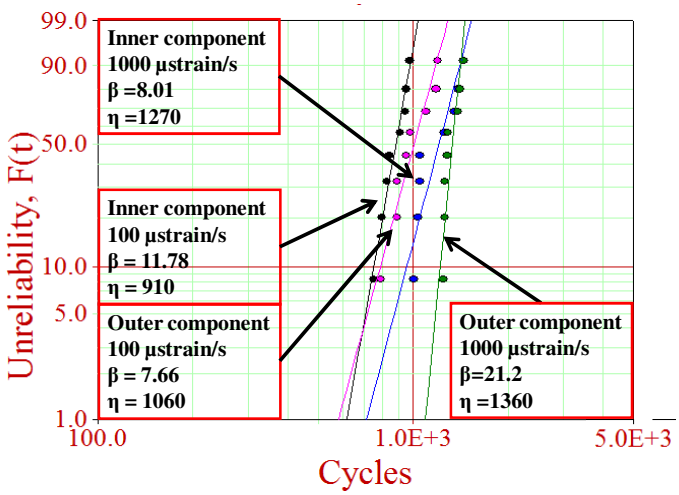

Figure 11: Effect of strain rate and placement

The dependency of cycles to failure on strain rate, demonstrated in this study using torsion loading, is valid for other tests such as bend test. However, the impact of strain rate is largely ignored in the analytical models available in the literature [47]. Also, strain rate should be accounted for in durability data obtained from literature.

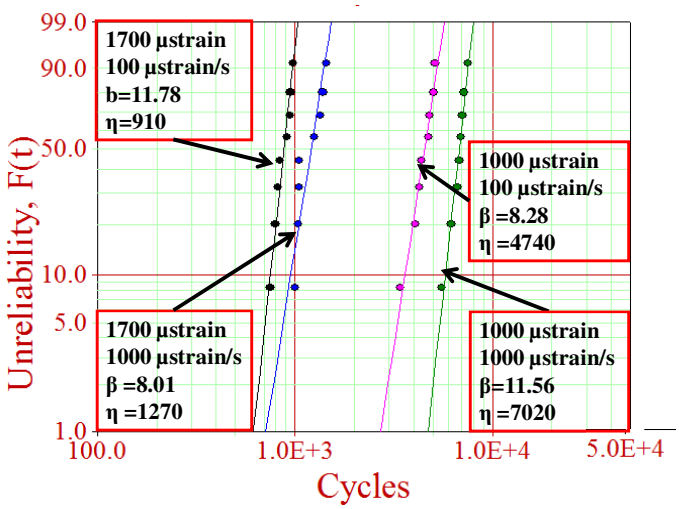

Figure 12: Durability of BGA packages at inner position

Durability of components at inner positions under each of the four loading conditions is discussed in Figure 12. When strain rate was reduced by an order of magnitude at a strain range of 1700 µstrain units (load conditions A and B), a 40% drop in characteristic life was observed. However, at a strain range of 1000 µstrain units (load conditions C and D) a drop in magnitude of strain rate by an order of magnitude resulted in a 50% drop in characteristic life. This suggests that the impact of strain rate is affected by the overall strain range. The impact of strain rate seems more pronounced at lower strain ranges.

Failure Analysis

Failure analysis was performed on test specimens to isolate failure sites. Figure 13 and Figure 14 show E-SEM pictures of sectioned solder interconnect with complete cracks at the component side attachment point. The images were obtained on BGAs with identical placement and solder joints located at the same relative positions. The two samples experienced different strain range loading (tests B and D) at similar

strain rates.

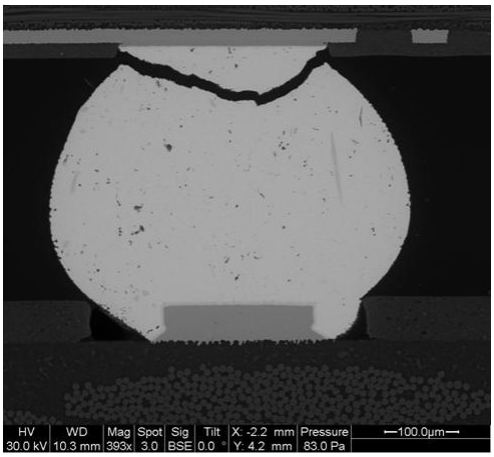

Figure 13: Cross-section of failed sample at inner component from test vehicle B.

Figure 13 shows a complete crack deep in the bulk solder Literature discussing torsion loads on electronic packaging interconnects show failure sites that correspond to either a mode II crack (similar to thermal cycling) as a result of shear stress parallel to plane of crack and perpendicular to crack front or mode III crack where the shear stress is parallel to both the plane of crack and crack front [19-24,28, 30]. However, Figure 13 shows presence of mode I (opening mode) fracture [48], which means the peeling stresses have to be considered while modeling damage. Figure 14 shows a shallow crack close to the package-solder interface. The deep crack is likely due to higher peak to peak strain range 1700 µstrain. The lower strain range did not drive the crack path into the bulk solder.

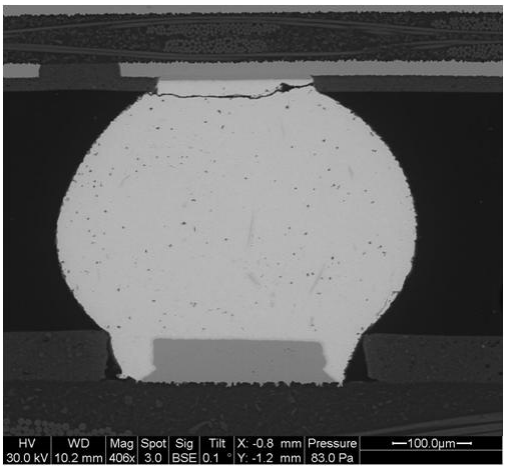

Figure 14: Cross-section of failed sample at inner component from test vehicle D.

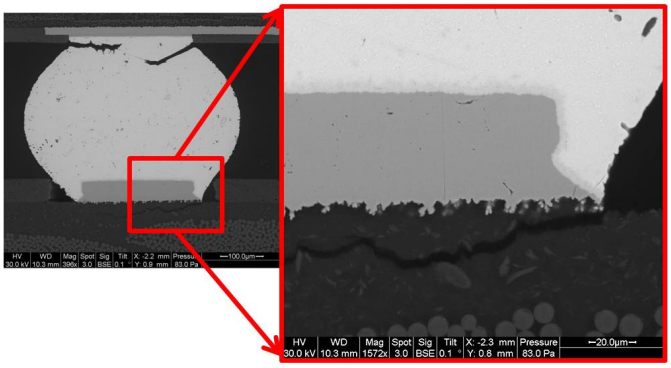

Figure 15: Pad cratering was observed in test vehicle A.

Figure 15 shows a cross-section of a failed sample from test vehicle A. Upon 1500X magnification, a pad crater can be observed underneath the copper pad of the BGA package. Pad cratering is defined as separation in the thin resin-rich region underneath the copper pads and traces [49]. Pad cratering does not directly cause electrical discontinuity. However, if the crack in resin includes the connecting copper trace to pad, an electrical discontinuity will occur. Pad cratering can also lead to other reliability concerns since a crack on the board laminate increases moisture absorption, which could lead to conductive anodic filament (CAF) [50]. Pad cratering follows

two different crack mechanisms. Cohesive cracks involve yielding of the resin while adhesive cracks occur on the interface between resin and glass fibers. The cohesive failure mechanism was the only observed mechanism of pad cratering in the examined test samples.

Pad cratering causes electrical discontinuity only when it results in trace cracking. Not all instances of pad cracking result in trace cracks. To expose trace cracks, a lateral section of the board pads and traces were examined. A lateral section involves grinding away in-plane to the area array device exposing the copper layer on the circuit board. A lateral section allows inspection of daisy chain copper traces at the board surface using an optical microscope. An optical image of a copper trace failure as a result of pad cratering on test vehicle B under an outer component is shown in Figure 16.

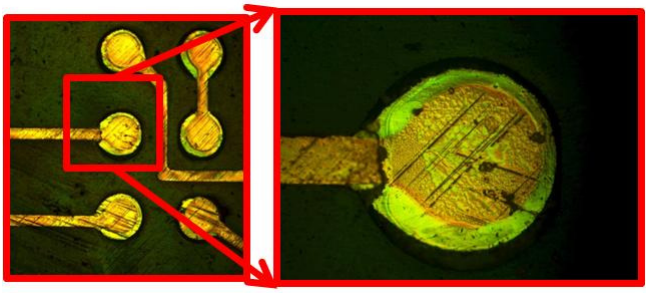

Figure 16: Lateral section of trace failure on test vehicle B.

Traces are conventionally routed at an angle to board flexure to avoid points of stress concentrations in copper traces and laminate. However, under torsion cyclic loading, the direction of board flexure changes and trace routing is likely to be parallel to axis of flexure at some point during the load cycle. Hence, torsion loads present a special concern to copper trace reliability.

The distribution of failure sites across the BGA as a function of loading criteria was studied using the dye-and-pry process. The dye-and-pry process is discussed in the appendix section. The dye-and-pry observations were plotted as a bar graph in the following order: no failure, board side solder failure, component side solder failure and trace damage. Instances of pad cratering were not included as a part of this observation since pad cratering itself does not lead to electrical discontinuity, as discussed earlier. Observations of BGA packages from outer component and inner component are shown in Figure 17 and Figure 18, respectively.

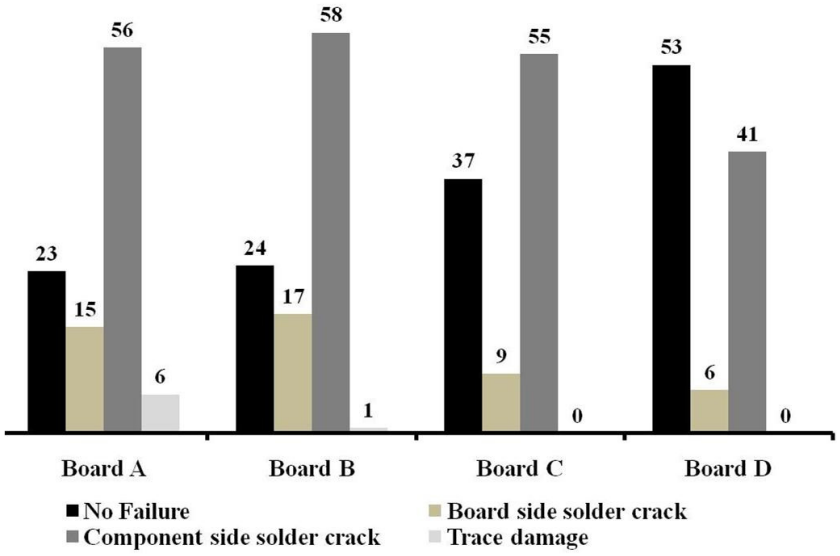

Figure 17: Distribution of failure sites for outer component.

It is clear that trace damage occurs only in the high strain range loading condition and is more common at the higher strain rate. At higher strain rates, the elastic modulus and yield strength of the solder increases. The high out-of-plane deflection causes high stress concentration around the copper pad, resulting in crack formation in resin. Component-solder interface cracks are the most common failure site.

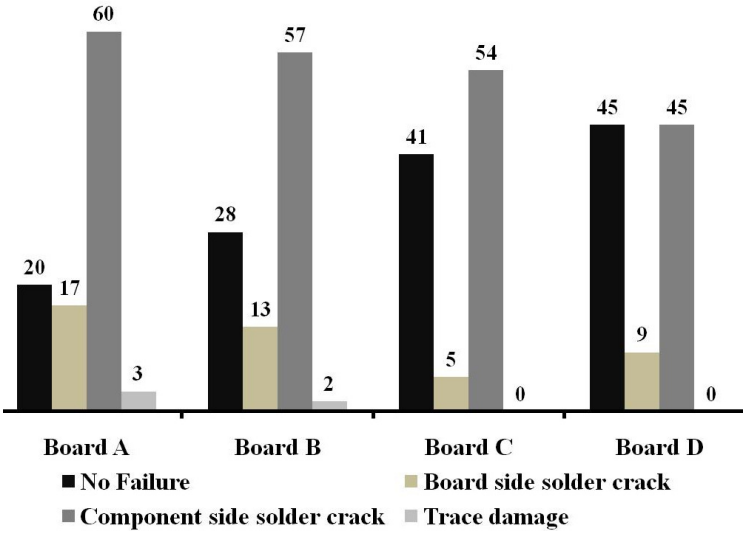

Figure 18: Distribution of failure sites for inner component.

At lower strain range, the nature of damage is more representative of fatigue and shows predominantly component-solder interface failures. There is also clear evidence that the number of cracks on the solder-board interface also reduces with reduced strain range. These observations show a clear trend quantitatively in likely failure sites for area array packages subjected to torsion loads. A case study in the literature also noted that pad cratering was observed more prevalently in SAC solders [51]. The authors suggest use of partial underfill to prevent such failures from occurring.

3.2 Stress test

The durability from previous section clearly show an increased chance of pad cratering and copper trace damage at the high twist condition and high twist rate (A and B). To ensure fatigue-generated cracks on the solder interconnects, the lowest stress condition was selected for performing the stress tests.

Test Matrix

Torsion testing was performed on test matrix outlined in Table 3. The 305 IO BGA was procured with two different solder compositions, SAC305 and SAC125Ni. The 128 IO BGA was procured with the solder compositions SAC305 and SAC105. These allows for comparison of three different lead-free solders and the impact of reduction in silver content under quasi-static mechanical loads. Since, both IO configuration are procured in SAC305, we can also understand the impact of the package configuration. Finally, the impact of stacking can also be observed by comparing the PoP-305 durability to 305-BGA-305 durability. The test matrix also allows us to generate failure data for SAC305, which is used to validate the durability prediction.

Table 3: Test Matrix

Board Type	Solder Alloy	Boards	Parts
305BGA-125	SAC125 Ni	2	16
305BGA -305	SAC305	2	16
128BGA -105	SAC105	2	16
128BGA-305	SAC305	2	16
PoP-305	SAC305(bottom) and SAC105(top)	2	16

Data Analysis

Figure 19 shows the probability of failure plot for the torsion test results with components placed at outer components. In this case the characteristic life (cycles to 63% failure) for the 305BGA-305 components is 29% higher than the characteristic life for the 305BGA-125 components. The 128BGA-305, the characteristic life is observed to be 170% higher than the characteristic life for the 128BGA-105 components. The trend for mechanical torsion fatigue durability is consistent with

thermal fatigue durability reported in literature where a reduction in durability is observed with a reduction in silver content.

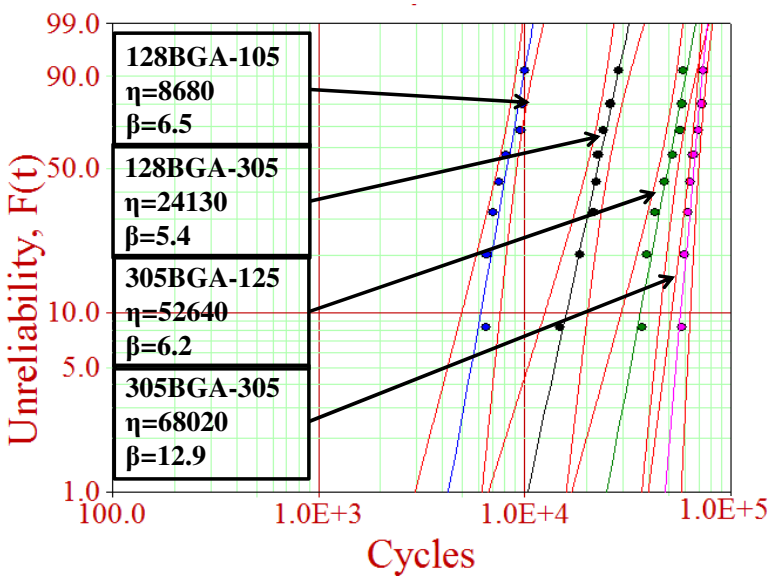

Figure 19: Durability of outer components with variation in Ag content

However, the 305BGA-305 exhibit higher durability than 128BGA-305 by 180%. The increased mechanical torsion durability of the 305BGA component is likely due to increased stiffness from stacked die configuration, reduced package thickness, higher IO count and the absence of the overmold at the perimeter of the package.

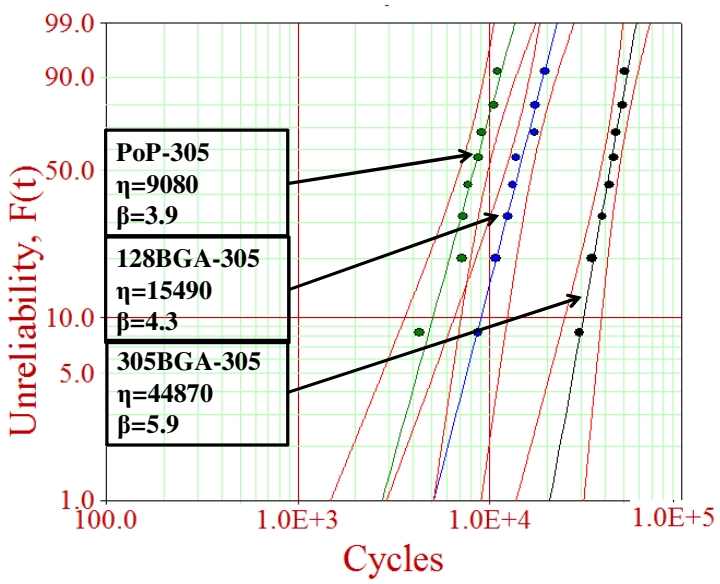

Figure 20: Durability of with different components at inner placement

Figure 20 shows the durability of PoP-305, 128BGA-105 and 305BGA-305 for the inner components. The solder sphere composition of the components is constant and the component configuration is varied. A drop in durability is observed, possibly due to increased stiffness. The stacked die leads to a higher component stiffness for 128BGA and stacked packages leads to a significantly higher component stiffness. The characteristic life of PoP-305 is 40% lower than 128BGA and nearly 80% lower than the 305BGA configuration. The tabulated weibull parameters for the failure data is presented in Table 4. Test results are consistent with previous section, where outer components always exhibit higher durability than inner components. Also noteworthy, the first net to fail for the PoP-305 components was always on the bottom component.

Table 4: Weibull parameters for stress tests

Component	Outer Components		Inner components	
	η	B	η	β

305BGA-125	52640	6.2	33910	6.4
305BGA -305	68020	12.9	44870	5.9
128BGA -105	8680	6.5	5570	4.2
128BGA-305	24140	5.4	15490	4.3
PoP-305	12790	2.8	9080	3.9

Failure Analysis

Failure analysis was performed on failed specimens to confirm failure site and mechanism. Destructive failure analysis yielded complete solder cracks on the component-solder interface for 305BGA packages irrespective of solder types. Figure 21 are E-SEM images of the failed 305BGA samples.

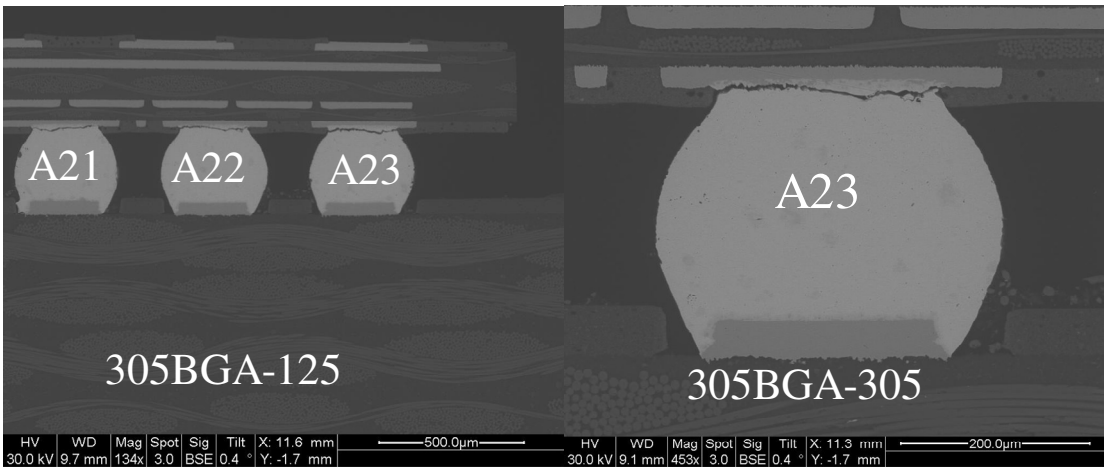

Figure 21: E-SEM image of 305BGA-125 and 305BGA-305

Failure analysis was performed on failed PoP-305 specimens. Figure 22 is the E-SEM images of the failed PoP305 samples. Again component-solder interface cracks are observed. The stress test yielded desired failure sites and extracted failure data can be used to characterize solder interconnect durability through fatigue failure.

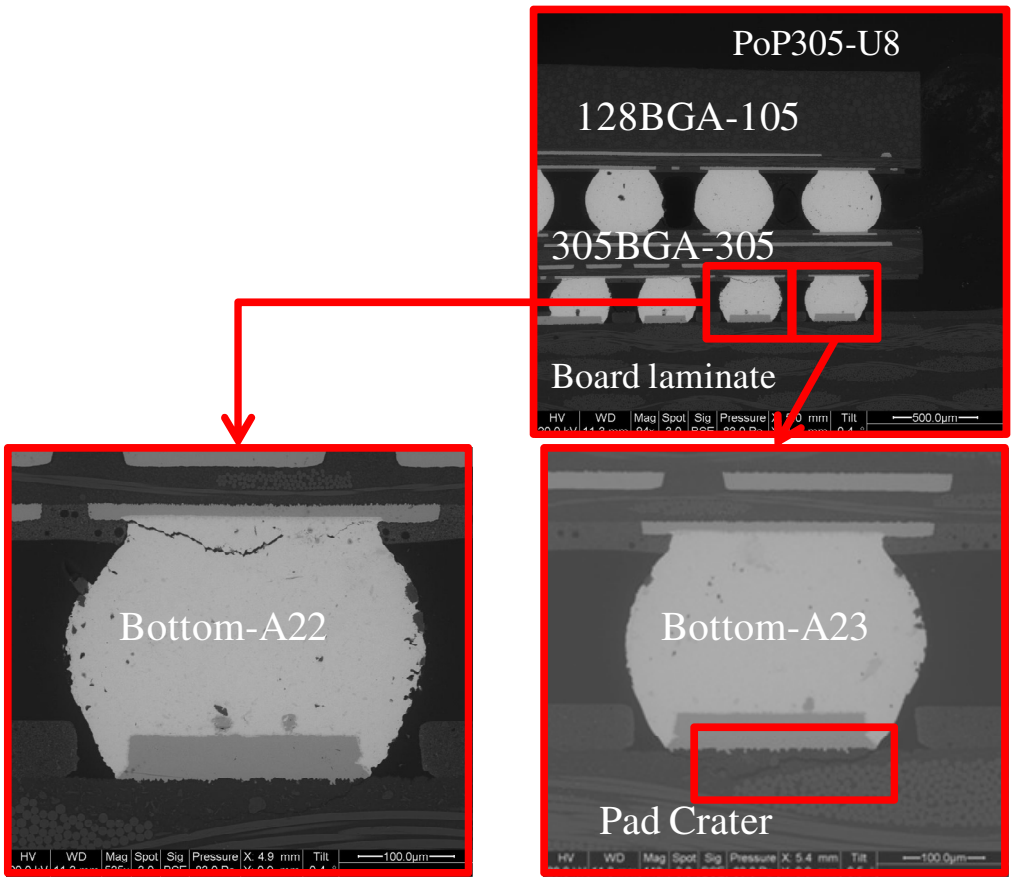

Figure 22: E-SEM image of failures in PoP305

Chapter 4: Approach to Modeling Mechanical Torsion

4.1 Finite element model

The test assembly was modeled in commercially available FEA tool Abaqus 6.9. A finite element model was generated with only four components on the test assembly (two inner and two outer components) and torsion loading was applied to estimate the displacement, stress and strain at the solder interconnects. Board laminate, copper pads, substrate, die and overmold were modeled as 3D solid tetrahedral elastic elements with reduced integration (C3D8R) while the solder interconnects were modeled as 3D solid tetrahedral elastic elements for higher accuracy (C3D8). Material properties were taken from literature [52].

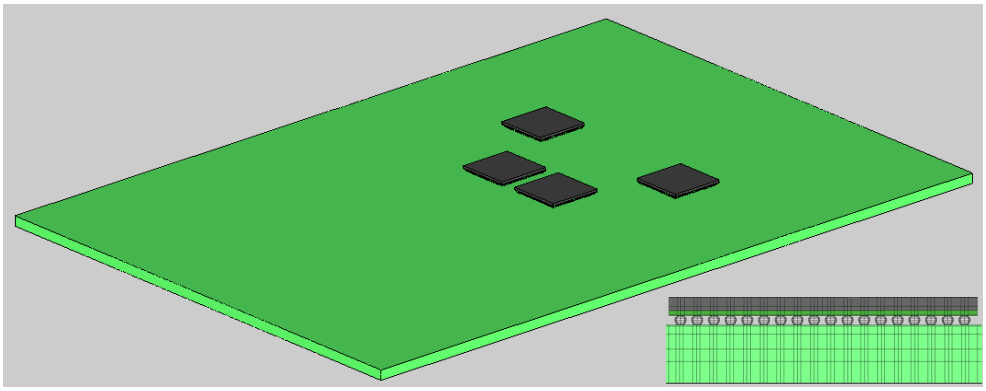

Figure 23: Global model of test vehicle

A global model of the test assembly and a cross-sectional view with the finite element mesh is shown in Figure 23. Figure 24 shows the location of maximum von-mises stress for the inner and outer components and a higher stress at the solder joints of the inner components than outer components. This finding agrees with our experimental

observation on difference in fatigue life between outer and inner components.

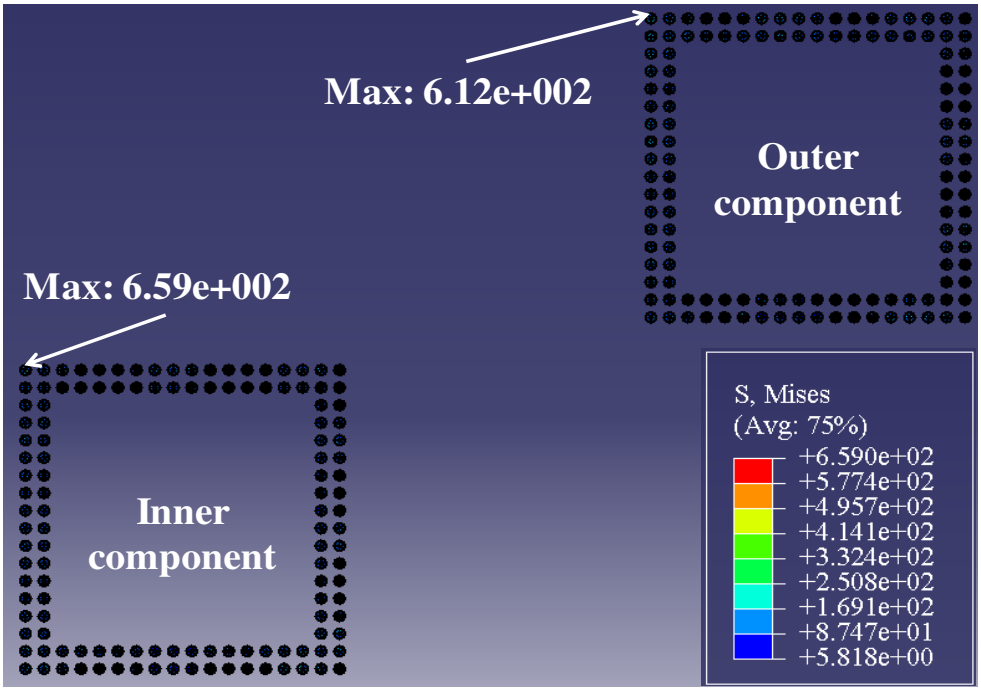

Figure 24: Von-mises stress for inner and outer components

The solder interconnect with the peak von-mises stress was identified in FEA and a sectional view across the solder joint and copper pad for load condition A and C are shown in Figure 25 with the same scale as Figure 24. This was compared to the cross-sectional failure analysis results for the same solder joints. It was observed that increased strain amplitude in load condition A resulted in a crack in bulk solder as predicted by FEA, while load condition C caused a crack parallel to the copper pads, closer to the IMCs.

Treating the solder material as elastic instead of elastic-plastic will lead to an over-estimation of corresponding stresses. Hence, the results from the section are valid qualitatively and not quantitatively. Peak stress beyond yield stress reported in literature [41] for SAC solders (39.5MPa; 10^{-3}/s; 173MPa; 10/s), hence plastic strain

has to be considered

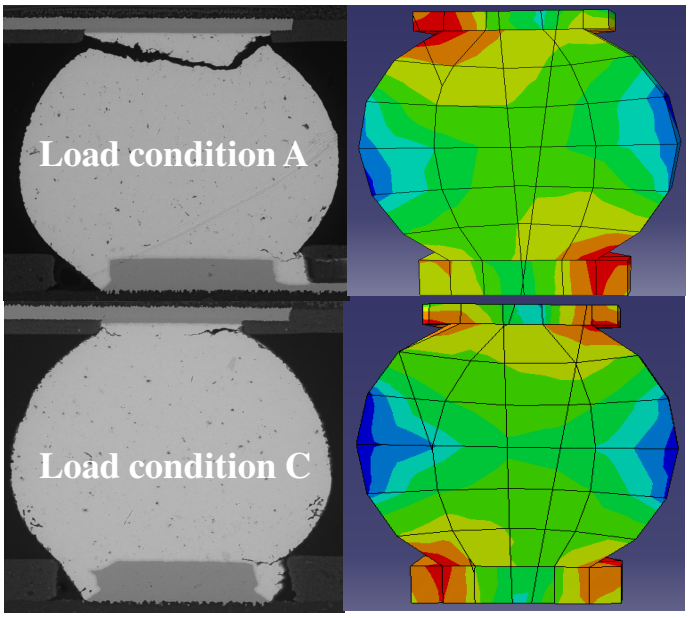

Figure 25: Failure analysis and corresponding sectional view from FEA

Additionally, the material properties were defined as strain rate independent. Hence the FEA analysis could capture the change in strain range between test vehicle A and C, but not discern the difference between test vehicle A and B. Other material modeling strategies are discussed in the following section.

4.2 Approaches to solder modeling

As outlined in the previous section, modeling the solder interconnect using elastic properties is inadequate and plastic damage has to be taken into consideration. Approaches to modeling plasticity have been discussed in this section**.** Failure analysis and elastic models clearly point peak solder strains in the corner solder joints. Hence, a finer mesh was used for the 12 corner solder interconnects for both the packages. Also shown are the models for the solder interconnects for components

128BGA and 305BGA in are shown in Figure 26 and Figure 27. A coarser mesh was used for solder joints other than the corner interconnects.

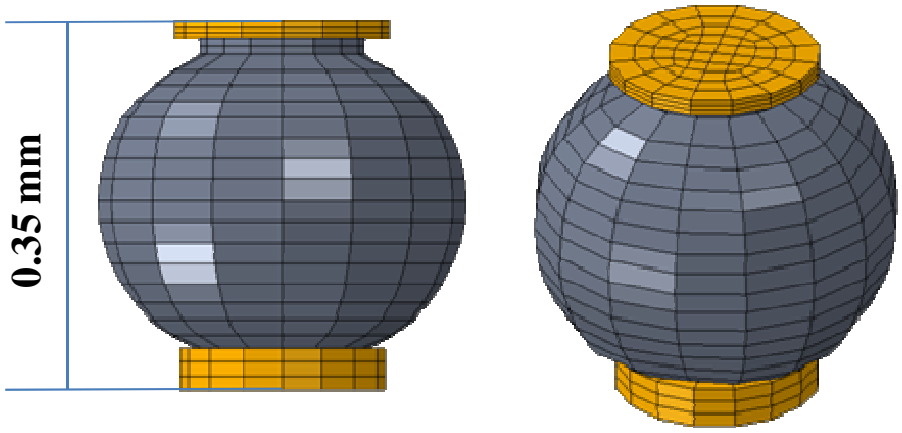

Figure 26: Solder joint and copper pad mesh in 128BGA

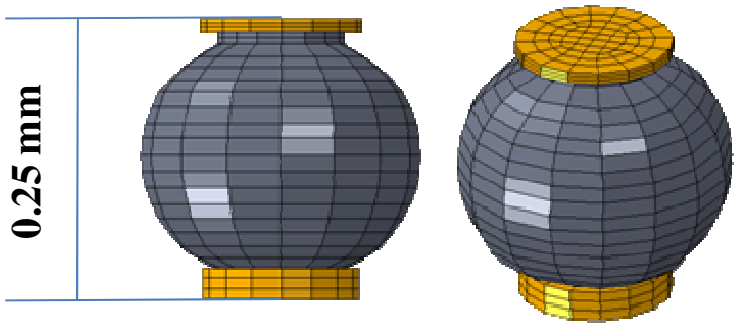

Figure 27: Solder joint and copper pad mesh in 305BGA

Strain-rate independent elastic-plastic model:

Strain-rate independent elastic-plastic model is the most popular approach to modeling plastic behavior and was proposed by Weise and Rzepka [53]. The approach assumes a linear behavior beyond yield stress and can be defined with three line segments. The first line segment characterizes the elastic behavior, while the second line segment characterizes the initial plasticity and the third line segment characterizes the saturated plasticity. This technique provides a more conservative

strain for a given stress for a material when compared to elastic approach. However, since the model is rate-independent the model tends to underestimate in comparison to rate-dependent models. The elastic-plastic properties used in this study are tabulated in Table 5.

Table 5: Rate-Independent Elastic-Plastic Properties

Solder	ε1 (%)	ε2 (%)	σ1 (MPa)	σ2 (MPa)	σ3 (MPa)
SAC305	0.14	0.4	57.4	80	2500

Strain-rate dependent elastic-plastic model

One of the objectives of the study is to characterize the impact of strain rate on durability and provide an approach to implement modeling strain-rate dependent material properties. Test results clearly show that solder performance is strain-rate dependent. The approach to modeling strain-rate dependent elastic-plastic behavior in this study was the Johnson-Cook model.

Johnson Cook model is a constitutive model that correlates flow stress to plastic strain, instantaneous strain rate and temperature. It is given by equation 4.

$$\sigma = \left(A + B(\varepsilon^{p})^{n}\right)\left(1 + C\dot{\varepsilon}^{*}\right)\left(1 - T^{*m}\right) \qquad \textbf{Equation 4}$$

where,

σ is the flow stress

ε^{p} is the equivalent plastic strain

$\dot{\varepsilon}^{*}$ Ratio of plastic strain rate to reference strain rate

T^{*} Homologous temperature

The five constants of the empirical model are *A, B, n, C* and *m.* The first term represents strain hardening. Constant A is the yield stress determined by quasi-static compressive strain-stress data, while terms B and n incorporate the effects of strain hardening. Constant C is used to scale the effect of strain rate and is introduced as a multiplicative constant to the ratio of instantaneous strain rate and reference strain rate. Constant m describes the effect of thermal softening. The effect on material properties caused by the temperature change was assumed to be negligible. Thus, the last factor in the constitutive relationship was neglected. This model is applicable for a wide range of strain rates and studies have shown 8% error during validation. Additionally, Johnson-Cook model can be directly implemented into ABAQUS/Explicit and was hence chosen as the approach to model strain-rate dependent elastic-plastic properties in this study.

Johnson-Cook model constants for SAC105 were not available in literature. Hence, an assumption was made that each constant varies linearly with change in composition of silver and copper. Regression analysis was then used to extract the model constants. The extracted constants are outlined in Table 6. These modeling approaches are used in the following Chapter for durability assessment.

Table 6: Strain-rate dependent elastic-plastic properties

Solders	**A (MPa)**	**B (MPa)**	**C**	**n**
SAC105	33.6255	1167.07	0.0224	0.91425
SAC305	38	275	0.0713	0.71

Chapter 5: Damage Modeling

Generalized strain life model, or the modified Coffin-Manson model is used to estimate damage in this study. The model is expressed by equation 5. The model can be represented as shown in Figure 28.

$$\frac{\Delta\varepsilon}{2} = \frac{\Delta\varepsilon_e}{2} + \frac{\Delta\varepsilon_p}{2} = \frac{\sigma_f}{E}(2N_f)^b + \varepsilon_f(2N_f)^c \qquad \textbf{Equation 5}$$

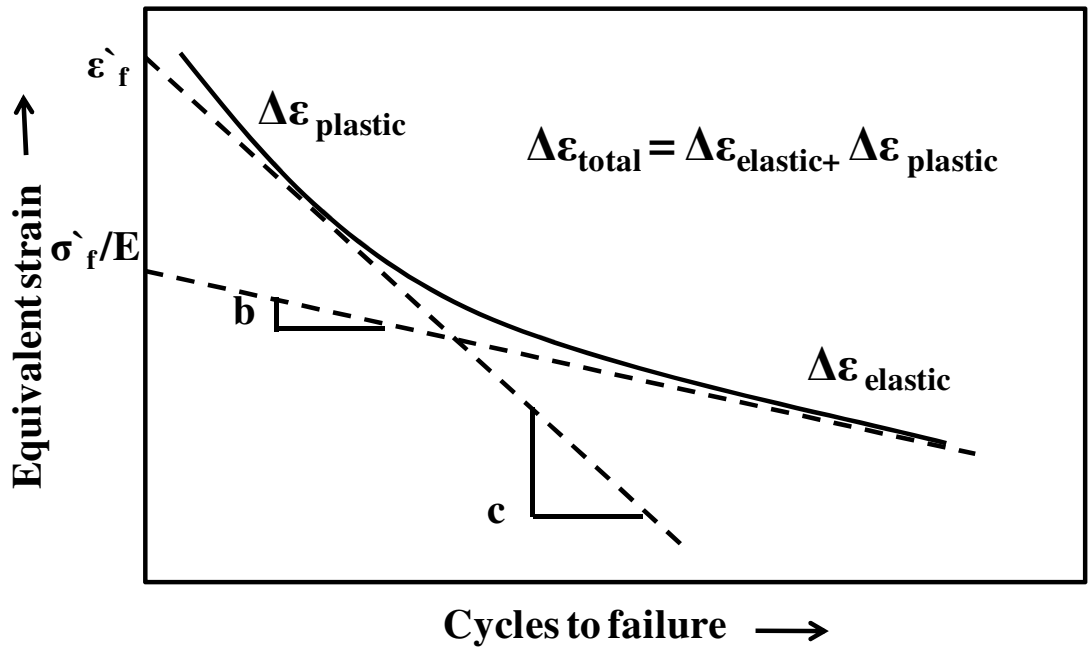

Figure 28: Fatigue damage model

It accounts for both the low cycle regime due to elastic damage through the Basquin model (first term in the equation) and high cycle regime due to plastic damage (second term in the equation).

5.1 Durability assessment for SAC305

A comparison of the elastic-plastic strain-rate independent model and the Johnson-

Cook model was made. The two different modeling approaches were used to predict solder strain for 128BGA-305 and 305BGA-305 components. The extracted solder strains were used in generalized strain-based damage model to estimate cycles to failure in the following Chapter. A comparison is made with test results to determine which approach better captures quasi-static loading. Two global models were generated as discussed in previous Chapter to simulate the tests on 128BGA-305 and 305BGA-305 components. Board laminate, copper pads, substrate, die and overmold were modeled as 3D solid tetrahedral elastic elements with reduced integration (C3D8R) while the solder interconnects were modeled as 3D solid tetrahedral elastic elements for higher accuracy (C3D8). The load profile from the stress test was applied to determine the solder strain at the critical solder interconnect isolated in the previous section. Volume averaging was performed to avoid edge singularity at the solder and copper pad interface [56]. The refined model generated, had a finer mesh at the corner solder joints to extract solder strain from areas of interest. Figure 29 and Figure 30 show the critical solder joint isolated under loading for 305BGA and 128BGA respectively. The highlighted regions in the figures maps the critical region from which solder strain was determined and hysteresis loops were generated to understand accumulated damage under loading.

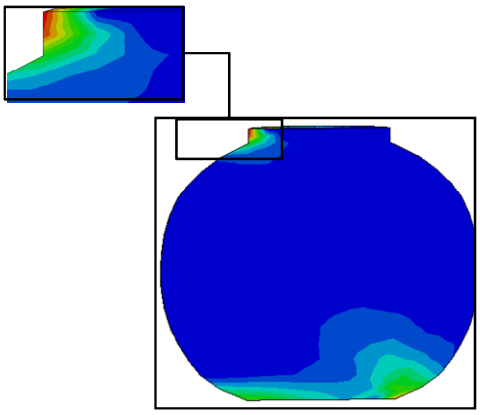

Figure 29: Area of interest from critical solder joint for 305BGA

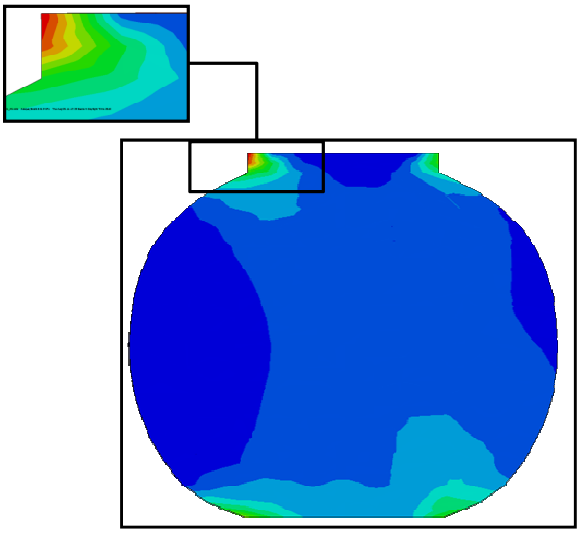

Figure 30: Area of interest from critical solder joint for 128BGA

Elastic-Plastic strain-rate independent approach

The solder joints were defined as elastic-plastic strain-rate independent material as defined in the previous Chapter. Hysteresis plots were extracted for the 128SAC-305, and 305SAC-305 components at two different placements. The estimated elastic strain in comparison to the plastic strain was less than 10% and thus the damage from elastic region was neglected in this study. An illustration of the hysteresis loops is shown in Figure 31 and the $\Delta\varepsilon$ was found to be 0.0125 for this instance. Extracted

strain values using elastic-plastic model are tabulated in Table 7 for 128BGA-305 and 305BGA-305 components.

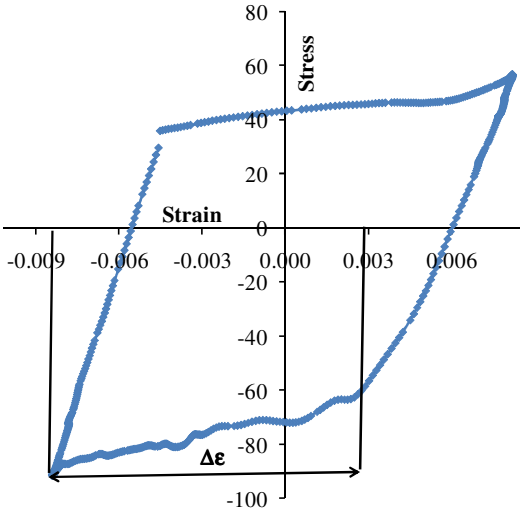

Figure 31: Hysteresis loop for 128BGA-305 in outer placement

Table 7: Extracted strain value using Elastic-plastic properties

Component	Placement	Solder Strain
305BGA-305	Inner	0.0086
	Outer	0.0077
128BGA-305	Inner	0.0142
	Outer	0.0125

Elastic-Plastic strain-rate dependent approach

The solder joints were defined as elastic-plastic strain-rate dependent material using the Johnson-Cook model as defined in the previous Chapter. Hysteresis plots were extracted for the 128SAC-305, and 305SAC-305 components at two different placements. An illustration of the hysteresis loops is shown in Figure 31 and the $\Delta\varepsilon$ was found to be 0.0153 for this instance. Extracted strain values using Johnson-Cook

model are tabulated in Table 8 for 128BGA-305 and 305BGA-305 components.

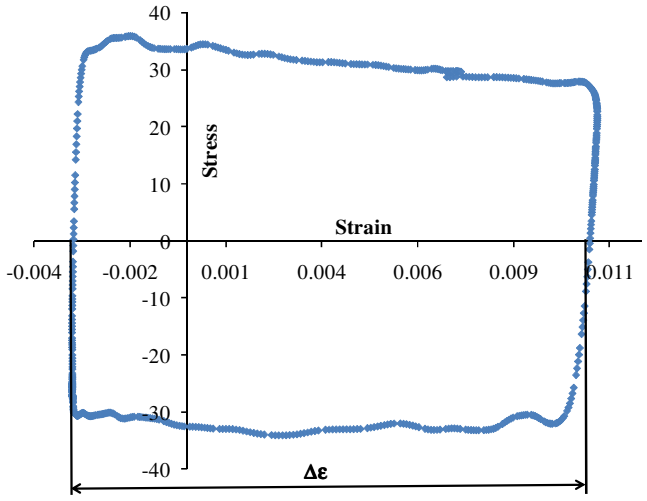

Figure 32: Hysteresis loop for 128BGA-305 in outer placement

Table 8: Extracted strain value using Johnson-Cook model

Component	Placement	Solder Strain
305BGA-305	Inner	0.0084
	Outer	0.0073
128BGA-305	Inner	0.0137
	Outer	0.012

Comparison of the approaches

Damage model constants for SAC305 are taken from literature and shown in Table 9 [55]. The strain ranges determined from the approaches are used to predict the cycles to failure for the components. Since, the elastic strain is negligible in comparison to the plastic strain and hence the high cycle regime term is ignored.

Table 9: Durability model constants [55]

Solder	$\sigma`_f/E$	b	$\varepsilon`_f$	c

SAC305	0.0087	0.7	0.59	-0.44

A plot of experimental cycles to failure and estimate using different model is shown in Figure 33. The results are also tabulated for ease of comparison with the associated errors for the two approaches in Table 10.

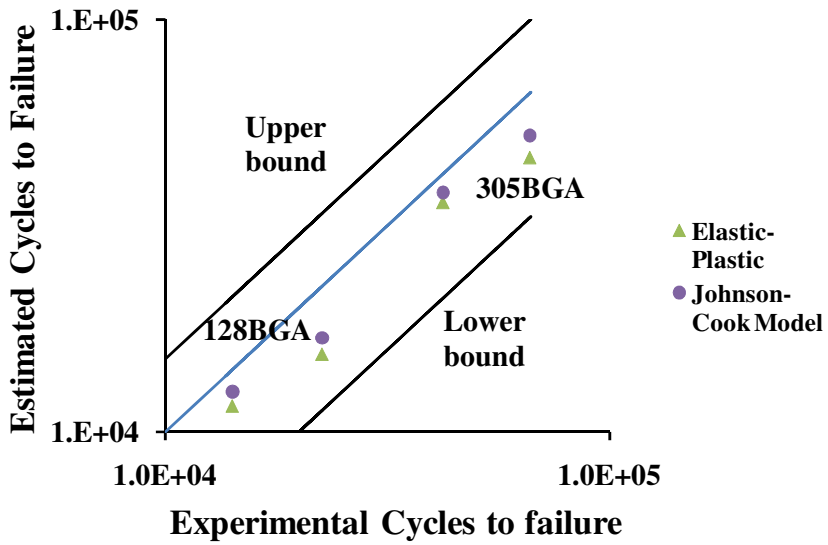

Figure 33: Comparison of estimated and experimental cycles to failure

Figure 33 explicitly shows that both approaches (strain-rate dependent and independent) yield results within the accepted 50% (1-X) uncertainty bounds on both sides. This shows that both techniques are comparable for identical load conditions. However, it is observed that Johnson-Cook model yields lower marginally lower error when compared to N_{50} from test results. Because elastic plastic is more conservative and always predicts a higher strain for a given stress on the material compared to both elastic and Johnson-cook model. Elastic models, as observed in the previous Chapter, tend to over predict the stress in comparison to elastic plastic and Johnson-Cook model. The results also validate the use of Johnson-Cook model for solder materials.

Table 10: Comparison of experimental results and estimated cycles to failure

Component	Placement	N_{50} (Cycles)	Elastic-plastic model		Johnson Cook model	
			N_f (Cycles)	Error (%)	N_f (Cycles)	Error (%)
305BGA	Inner	42170	36030	17.0	38000	11.0
	Outer	66130	46320	42.8	52300	26.4
128BGA	Inner	14180	11530	23.0	12500	13.4
	Outer	22550	15400	46.4	16900	33.4

5.2 Extraction of Damage Model constants for SAC105

Extraction of constants

Literature documents generalized strain-based damage model constants for SAC305 solder but not for SAC105 solder. Using the results from tests performed (on 128BGA-105 components) to determine stress level for testing, we can determine these constants. However, the elastic-plastic model cannot discern different loading rates and hence Johnson-Cook model is used to model solder's material properties as validated in the previous section.

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon_f \left(2N_f\right)^c$$

Equation 6

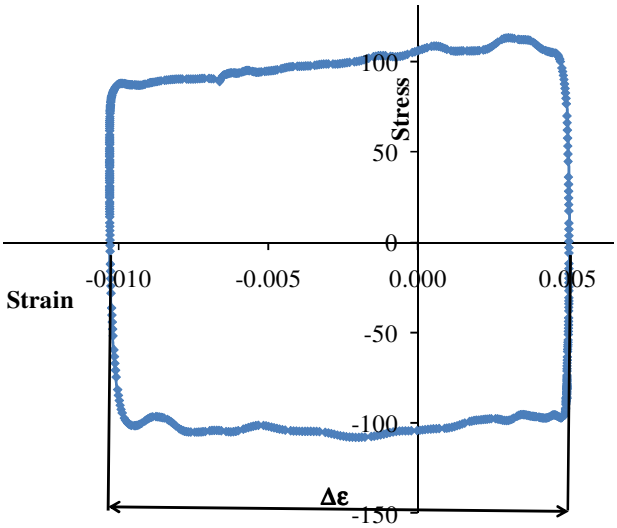

Figure 34: Hysteresis plot for 128BGA-105 in load condition A in outer placement

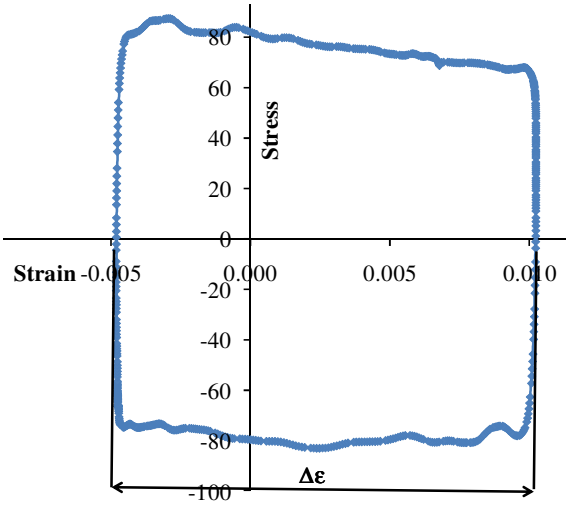

Figure 35: Hysteresis plot for 128BGA-105 in load condition A in inner placement

Hysteresis plots for load condition A for outer and inner placements are shown in Figure 34 and Figure 35. Other hysteresis plots are included in the appendix. Also, strain ranges from all four load conditions for both inner and outer placements are tabulated in Table 11.

Table 11: Strain ranges at different load conditions

Load condition	Placement	Strain range	$N_{63.2}$
A	Inner	0.0153	1270
	Outer	0.015	1360
B	Inner	0.0172	910
	Outer	0.0158	1060
C	Inner	0.0083	7020
	Outer	0.0072	9280
D	Inner	0.00985	4740
	Outer	0.008	7970

Again, ignoring the damage from the elastic strain, only low cycle damage was considered. Strain data and Cycles to failure data for $N_{63.2}$ (63.2% of population to fail) was used to determine the damage constants for load conditions A, B, C and D for outer components and load conditions A and B for the inner components. Load conditions C and D for inner components will be used to validate the model constants.

$$\ln\left(\frac{\Delta\varepsilon_p}{2}\right) = \ln\left(\varepsilon_f\right) + c\ln\left(2N_f\right)$$ **Equation 7**

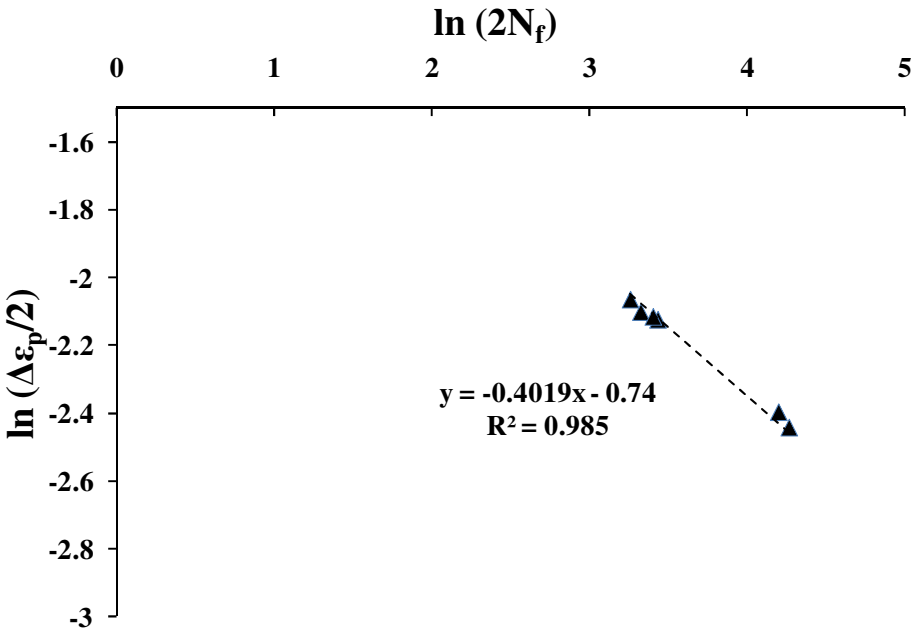

Figure 36: Damage constants extraction

Using log plot to correlate the power-law relationship between cycles to failure with strain data, a linear trend-line was fit as shown in Figure 36. The equation extracted is in the form of Equation 7. The slope and antilog of the intercept help us determine the constants and are tabulated in Table 12.

Table 12: Durability model constants for SAC105

Solder	$\varepsilon`_f$	c
SAC105	0.182	-0.402

Validation of model constants

The resultant damage constants were validated using load condition C and D for the

inner components. The strain range tabulated in Table 11 was used with damage constants shown in Table 12 to yield estimated time to N_{50}. The estimated and experimental cycles to failure are plotted in a bar plot in Figure 37 and an error of less than 20% is observed.

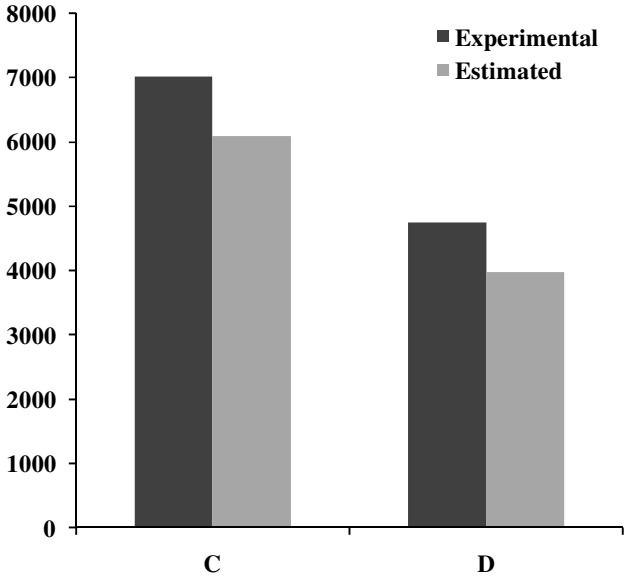

Figure 37: Comparison of estimated and experimental cycles to failure

Chapter 6: Summary and Contributions

Cyclic mechanical torsion loading was used to perform reliability tests on second level solder interconnect. No standards are available for torsion testing due to the positional dependence. Hence, multiple tests at different stress levels were performed on 128 IO BGA with SAC105 solder spheres. The results from these tests were used to extract SAC105 damage model constants and isolate desired stress level for testing. This was followed by tests on 128 IO, 305 IO BGA and PoP305 components to generate failure data. The BGA components were then modeled using to different approaches, strain-rate independent and strain-rate dependent elastic-plastic properties. The extracted solder strain value from critical solder joint was then used in a damage model to assess the effect of the two modeling approaches. The contributions from this work are listed below.

Damage model constants for SAC105

Damage constants for low cycle fatigue damage for generalized Coffin-Manson model for SAC105 were extracted. The damage model was validated for one of the test conditions. The model will allow us to predict the reliability of low silver SAC alloys under mechanical fatigue life once the solder strain during the application is known.

Strain rate dependency

An approach to modeling strain rate dependency was demonstrated where the material properties are defined as strain rate dependent. The generalized Coffin-

Manson model estimates (independent of strain rate) using strain rate dependent properties were observed to have lower error than strain rate independent properties.

Durability of PoP components

Durability of PoP components and BGAs were plotted for same the load condition to show the relative performance of the component. The cycles to failure for the PoP305 components were 40% lower than 128BGA-305 and 80% lower than 305BGA-305. This can be explained by the increased stiffness of the package as a result of stacking components.

6.1 Suggestions for future work

Effect of Dwell time and temperature

The effect of dwell was not modeled in this work. Dwells need to be modeled to simulate conditions of extended durations of constant load in field and the associated damage. It is recommended that these tests be performed at elevated isothermal conditions to accelerate creep damage.

Comparison with other mechanical fatigue tests

The mechanical torsion loading is similar to mechanical bend tests, since origin of solder strain is board flexure. However, there is a strong positional dependence in torsion tests. It would be interesting to perform a comparison on the durability of components under comparable torsion loading and bend tests.

High cycle damage constants for SAC105

This study extracted the low cycle damage constants for SAC105 solder. It would be useful to extract the high cycle model constants using vibration loading to complete the generalized Coffin-Manson equation. This would allow reliability engineers to predict reliability better for both regimes of loading.

Appendices

6.1 Test setup characterization

The printed wiring assembly was then modeled as 3-dimensional deformable laminates on Abaqus Standard using 8-node brick elements. Mesh sensitivity analysis was performed to minimize the effects of mesh size on strain prediction at integration points. The strain values obtained from tests was used to calibrate the board material properties to ensure accuracy in all future predictions. The resultant strain comparison for location L1 in Figure 38 is shown in Figure 39. The values and profile between the simulation and tests agree.

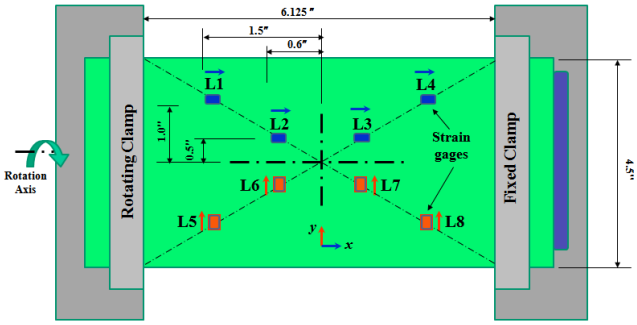

Figure 38: Schematic of unpopulated board test

An unpopulated board similar in dimensions to the test vehicle was tested to understand the load induced across the PWA. Strain gages were placed at locations in orientations shown schematically in Figure 38. Redundant locations were avoided using knowledge of axes of symmetry. A test matrix was formed for a combination of angular displacement and angular velocity while time periods and strain levels across the board were monitored. Figure 39 shows the calibrated FEA results.

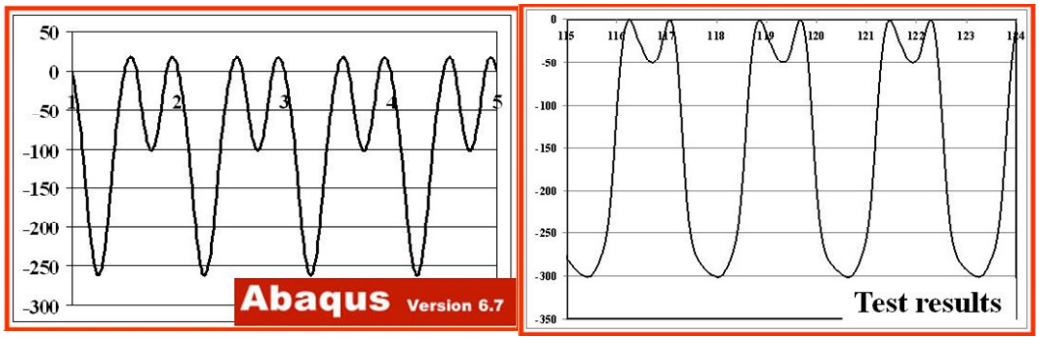

Figure 39: Comparison of FEA and test results

It is to be noted that the normal strains (ε_{xx} and ε_{yy}) were not uniform across the board while the shear component was nearly uniform across the board. Finite element analysis was used to determine the uniform area on the board as shown in Figure 40. It also showed that board level shear strain was higher than either of the normal strain components by almost an order of magnitude.

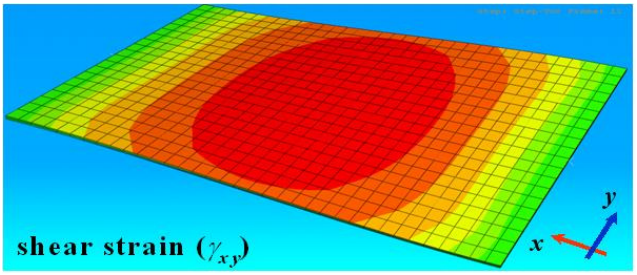

Figure 40: Uniform shear area of test board

6.2 Cycles to Failure Data

Table 13: Cycles to failure data from stress determination tests

Load	Outer components				Inner components			
A	1285	1265	1263	1249	1037	1005	1053	1052
B	1184	951	891	790	752	841	796	825
C	6496	7017	7507	6547	4283	4081	4369	3421
D	3915	6907	7874	5070	6950	5541	7065	6197

Table 14: Cycles to failure data for stress tests

		Outer components				Inner components			
128BGA-105	**I**	6496	7017	7507	6547	4283	4081	4369	3421
	II	9760	9567	10022	8132	8015	5745	4527	6443
128BGA-305	**I**	14783	22778	24139	28615	13765	12459	8714	17200
	II	25981	18501	21562	22247	10784	13168	19441	17253
PoP305	**I**	7623	7432	9441	5565	7168	7682	8737	4303
	II	14357	16263	15604	14831	10504	9087	11021	7262
305BGA-305	**I**	58200	69710	73444	63546	45429	49219	44413	29341
	II	72444	59684	65783	61924	34079	50582	41985	38763
305BGA-125	**I**	58819	47679	58227	37019	22875	35722	34905	33359
	II	42308	52308	39143	56718	31890	28709	26980	38926

6.3 Dye and Pry Technique

Dye and pry process is used to identify cracks or separations within solder joints. This test is typically performed on solder joints of area array packages (BGA components), as the solder joints cannot be inspected readily. However, one can employ this technique on any package. A low viscosity, dye penetrant is applied on the area. Literature suggests that we apply copious amounts of dye and allow surface tension to draw the dye underneath the package. The dye is then allowed to cure by baking the sample.

The top of the component is then pried away from the board. This can be done using a specialized fixture or by shearing the PWB to propagate existing cracks to remove the package. This results in exposing existing failure sites. Once the component has been removed the fractured solder surfaces are examined for evidence of dye penetrant. If dye is present, this indicates that the joint was separated prior to removal from the board. If the dye is not present on the fractured surface, it indicates that the fractured surface was created when the component was pried out of the PWB.

While no standard is available for dye and pry process, it has been described in literature [57]

Approach:

List of material and equipment used:

- Dykem 80496 steel red layout fluid. [58]
- Desiccator jar
- Vacuum pump

- Hot plate (DATAPLATE® Digital hot plate)

Procedure:

- Assembled part samples are selected for dye and pry process. A band saw is used to cut the component of interest in the form a coupon away from the printed wiring board. The component is cut with sufficient allowance to ensure that the component can be held in a fixture while prying the package off the PWB.

- Assembled part on printed wiring board is dyed using dye penetrant (Dykem 80496© steel red dye). The dye is applied using a dropper on the sample with a die bath beneath the test board. The dye is drawn in underneath the package due to surface tension. However, for area array devices with fine pitches, the sample is placed in a desiccator jar and a negative pressure is applied using a vacuum pump. This allows complete penetration.

- Once the dye has set-in, the test board is baked on a hot plate at 100°C for 2 hours. This helps the dye to cure into a permanent thin film that will not crack when the component is pried.

- After baking, two long nose pliers are used to flex the PWB coupon to propagate existing failures into complete cracks. Then the package can be pried away from the PWB. Illustrations of packages post prying are shown in Figure 41.

This is followed by inspection under the optical microscope of the fracture surface on both the package side and board side. A fracture surface completely stained indicates that the crack was created due to stress test leading to an open circuit. Partial stained

circuits are not failures; however they indicate micro cracks created while testing. Some illustrations are shown in Figure 42. Fracture surfaces that do not have any stain indicate cracks created during the dye and pry process. These are commonly interpreted as healthy solder joints since no pre-existing failure was propagated into reveal any failure site.

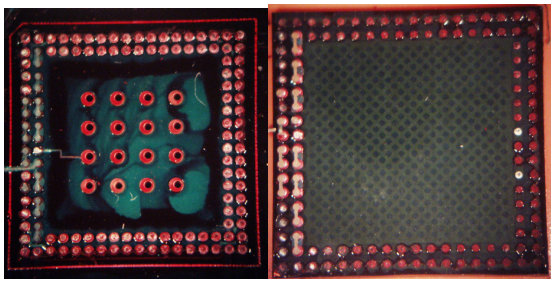

Figure 41: Board side view and package side view of sample after dye and pry

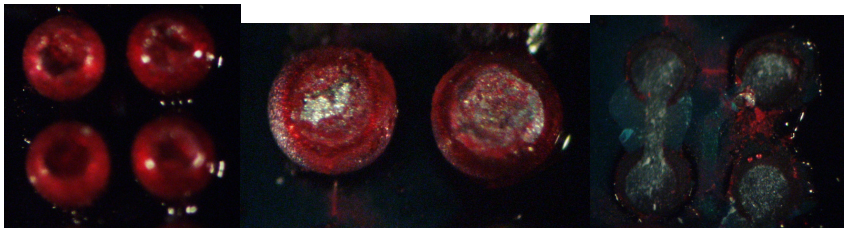

Figure 42: Complete, partial crack and no failure instances

Notes:

Dye and pry process yields useful information on failure sites distribution across the area array of a package. It helps recognize localized trends, for instance, failures under die shadow or package periphery. It allows whole field view as opposed just a sectional view. Also, it is one of the fastest techniques to obtain failure site information.

The challenge with dye and pry process is that the results are dependent on the worker skill and multiple interpretations are possible. Use of standardized samples is

recommended to define failure sites to avoid misinterpretation. It is important to document samples during optical inspection (also, pried samples can easily disintegrate). Multiple failure sites might exist in a single solder ball and may not be visible initially. For instance, both package-solder interface and board-solder interface might exhibit fractures. Hence, after each site is documented one can pry the solder ball away to inspect copper pad, if pad cratering is suspected. New cracks introduced as a result of the vibration while cutting the PWB can be distinguished from the fracture surfaces introduced during stress tests.

6.4 Volume Averaging

Based on failure analysis, the copper pad-solder interface on the package side is observed to be a critical region and the mesh density is increased to capture the strains better. Volume averaging is a common technique used to reduce the effect of edge singularity at these dissimilar interfaces while performing finite element simulations on solder interconnects [59]. In literature, different approaches have been used to perform volume averaging. *Syed et al* [60] use 25 micron thick layer at the interface for his creep strain model. The study reports that at least two layers of mesh have to be used at this interface to achieve convergence. This has been implemented in this study. *Darveaux et al* [61] use 30 micron thick layer in the fracture mechanics based model. *Che et al* [62] prove that use of peripheral elements for the layer in comparison to the entire layer for volume averaging improves accuracy by 57%. This is because of lost sensitivity due to lower stresses within the layer in comparison to outer layer, which is the location of crack initiation. These studies model thermal cycling loading where the stress tensor is largely influenced by shear loading along the interface, and hence selection of an entire layer does not reduce sensitivity. However, under cyclic mechanical loading, the stress tensor is more complex and location of peak strain shifts during loading cycle. Hence, *Zhou* [63] in her dissertation has used 2% solder volume averaging about the site where maximum solder strain (during entire cycle) was used for BGA packages on the copper pad-solder interface. In the same study, LCR2512 packages were also modeled and again volume averaging was performed around the region of maximum strain at the neck of

the solder fillet (during entire cycle).

Also, result value averaging used in Abaqus software needs to be understood. While probing element based values for field output variables, such as stress or strain, the software uses result value averaging. Element values are extrapolated to the nodes. Nodes common to two or more elements will receive multiple contributions from the elements. These contributions are averaged and the user controls this by setting by permitted variation in relative nodal variation. This term is defined as the ratio between difference between maximum and minimum of values at a node and difference between maximum and minimum in the selected region. This threshold was selected as 25% to control discontinuities across different sections.

In this study, the copper pad was modeled with three layers of elements while the solder interface was modeled with two layers to reduce edge singularity. Due to the cyclic nature of loading under torsion, the location of peak stress at the solder joint at an instant during the cycle would vary. Hence, by averaging across an entire slice of the joint, the area under the hysteresis loop will not be representative of test condition and higher than experienced by a specific region. Therefore, solder volume averaging was performed using four elements adjacent to the site where maximum solder strain (during entire cycle) was reported. Physically, the region selected for solder volume averaging was equivalent to 5.5% of solder volume in the interfacial layer in the solder-copper pad interface on the component side.

6.5 Johnson-Cook Model

Johnson Cook model is a constitutive model that correlates flow stress to plastic strain, instantaneous strain rate and temperature [64]. It is given by equation 4. This equation can be split into 3 different parts which each aspect of the relationship is defined. This has been outlined in this appendix.

$$\sigma = \left(A + B(\varepsilon^{p})^{n}\right)\left(1 + C\dot{\varepsilon}^{*}\right)\left(1 - T^{*m}\right) \qquad \textbf{Equation 8}$$

where,

σ is the flow stress

ε^{p} is the equivalent plastic strain

$\dot{\varepsilon}^{*}$ Ratio of plastic strain rate to reference strain rate

T^{*} Homologous temperature

The five constants of the empirical model are *A, B, n, C* and *m*. The first term represents strain hardening. Constant A is the yield stress determined by quasi-static strain-stress data, while terms B and n incorporate the effects of strain hardening. Since the references used in this study for solders are derived from room temperature experiments and were not performed at multiple temperatures, the constants A, B and n can instead be considered as A^{*}, B^{*} and n^{*} were these constants represent room temperature value.

The effect on material properties caused by the temperature change was assumed to be negligible. Thus, the last factor in the constitutive relationship was neglected. The constants T^{*m} and m (to describe the effect of thermal softening) are ignored.

Constant C is used to scale the effect of strain rate and is introduced as a multiplicative constant to the ratio of instantaneous strain rate and reference strain rate at which the quasi-static tests were performed to derive constants A, B and n.

This model is applicable for a wide range of strain rates and studies have shown 8% error during validation [65]. Additionally, Johnson-Cook model can be directly implemented into ABAQUS/Explicit and was hence chosen as the approach to model strain-rate dependent elastic-plastic properties in this study.

Johnson-Cook model constants for SAC105 were not available in literature. Hence, an assumption was made that each constant varies linearly with change in composition of silver and copper. It is common in literature to derive empirical model constants by assuming a linear fit of material constants such as yield stress or Young's constant [66] [67]. Regression analysis was then used to extract the model constants.

To validate the approach, SAC305 model constants were extracted using regression approach and compared with values reported in literature. The error was determined to be 9% for a simple tensile test when both sets of model constants were used. The extracted constants are outlined in Table 15 with source reference or method of determination listed in the final column.

Table 15: Johnson Cook Model properties

Constants			**A (MPa)**	**B (MPa)**	**C**	**n**	**Source**
Sn	**Ag**	**Cu**					
96.5	3	0.5	38	275	0.0713	0.710	[65]

96.5	3.5	0	29	243	0.0956	0.703	[65]
96.3	3	0.7	43	773	0.015	0.76	[68]
99.3	0	0.7	35	1250	0.014	0.96	[68]
96.5	3	0.5	38.12	344.1	0.0403	0.756	Regression
96.5	1	0.5	31.63	667.1	0.0224	0.914	Regression

6.6 Hysteresis plots

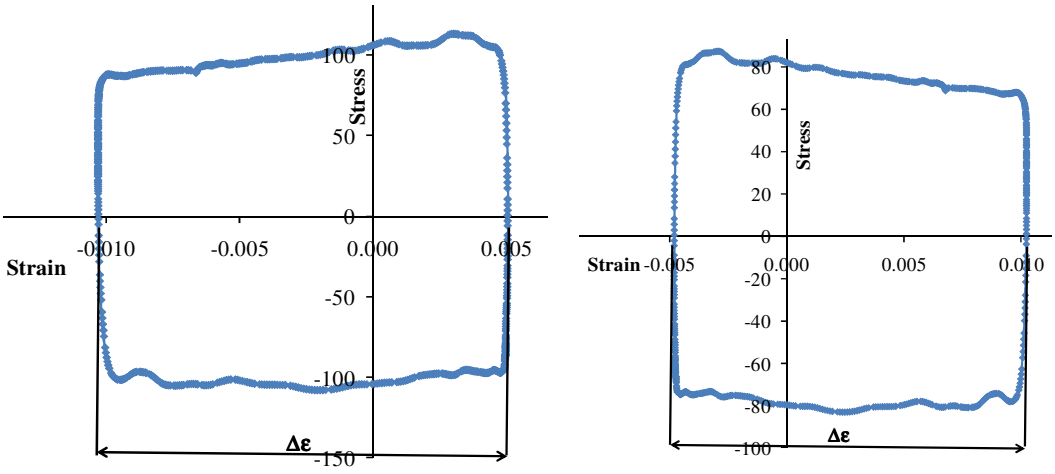

Figure 43: Hysteresis plots for load A for 128BGA for inner and outer placement

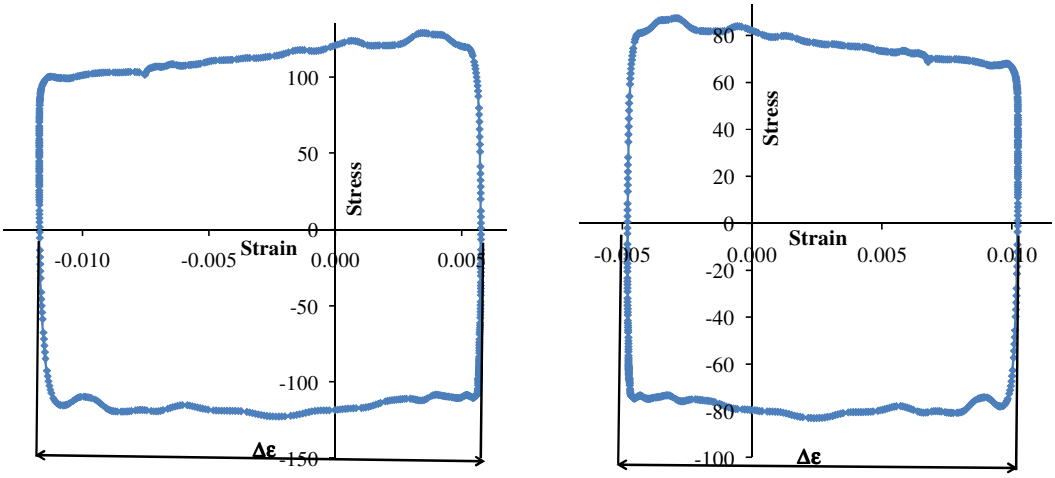

Figure 44: Hysteresis plots for load B for 128BGA for inner and outer placement

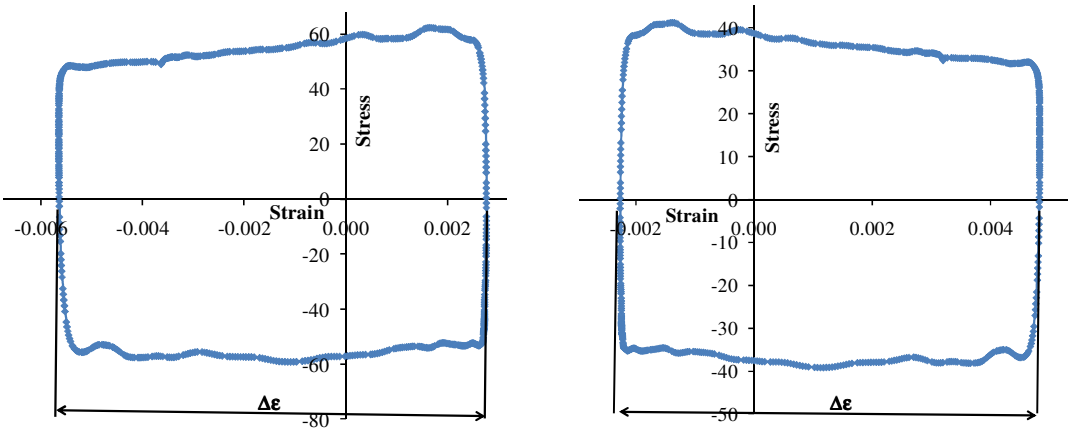

Figure 45: Hysteresis plots for load C for 128BGA for inner and outer placement

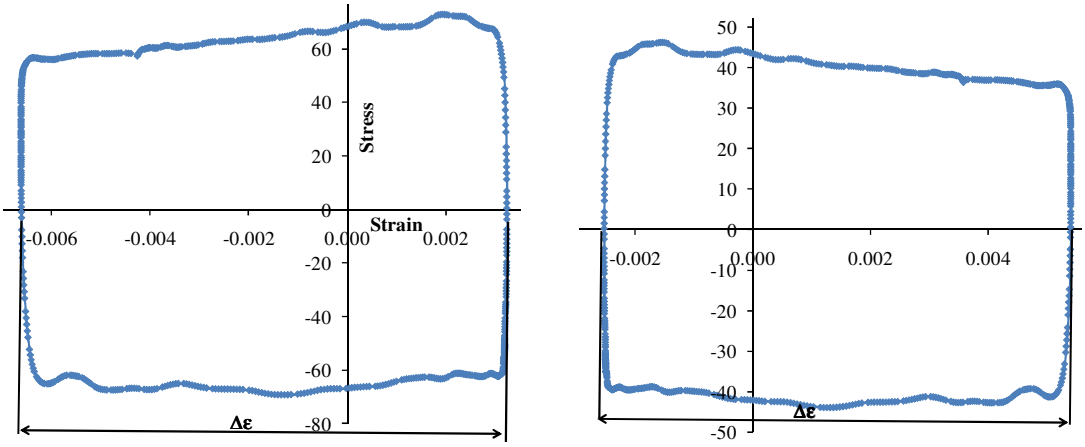

Figure 46: Hysteresis plots for load D for 128BGA for inner and outer placement

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