ABSTRAT

Title of thesis: EVALUATION OF SOLDER-JOINT RELIABILITY FOR A 10MM QUAD FLAT LEADLESS PACKAGE WITH TOP-SIDE PADDLE USING CLASSICAL MODELS FOR A LEADLESS DEVICE AND ACCELERATED LIFE TESTING.

Mark Alan Levin, Masters of Reliability Engineering, 2010

Thesis directed by: Dr. Joseph Bernstein, Professor of Engineering, University of Maryland

The standard QFN package consists of a leadless perimeter array and a bottom solderable thermal paddle. The thermal performance of the package can be improved by moving the paddle to the topside. The soldered surface area of the package reduces by about 80% with a top-side paddle. The soldered-joint life will also reduce due to the significant thermal coefficient of expansion mismatch between the QFN package and the circuit board.

The solder-joint reliability of a large QFN package with top-side paddle is not well understood. This thesis evaluates the solder-joint reliability of a 10mm square leadless

QFN package with top-side paddle. The analysis includes several classical models for a leadless package and compares modeling results to accelerated reliability testing. The accelerated tests include the influence mold compound and lead finish play on solder-joint life and ways to improve solder-joint reliability.

EVALUATION OF PHYSICAL FACTORS INFLUENCING SOLDER-JOINT RELIABILITY OF A 10MM LEADLESS QFN PACKAGE WITH TOP-SIDE PADDLE

By

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Preface

The Quad Flat No lead (QFN) package with bottom-side paddle has been used in the commercial industry for years. The standard package consists of a perimeter array of leadless pads on the bottom-side around the package. For mechanical reliability and improved thermal performance there is a large solderable bottom center thermal pad, called a paddle that is soldered to the circuit board. The paddle is thermally bonded to the die, which provides a low thermal resistance path for heat removal. The primary source for heat removal is through the circuit board. The center paddle accounts for about 80% of the package soldered surface area. Moving the paddle to the top-side of the package improves thermal performance and reduces the soldered surface area that is used for mechanical attachment reliability. The QFN is a flat leadless package which provides little compliance for mechanical stress. The QFN package has a low coefficient of thermal expansion (CTE) and is often soldered to a circuit board substrate with a significantly higher CTE. The CTE mismatch between the package and circuit board is often greater than two to one. Because the QFN with top-side paddle package is new, there is little to no information regarding the mechanical solder-joint reliability due to CTE mismatch.

The purpose of this thesis is to evaluate the solder-joint reliability of a 10mm leadless QFN package with top-side paddle. The analysis will include modeling using classical models for a leadless package and accelerated life testing. In addition, guidance is

provided on the potential solder-joint reliability improvement by changing either package design or circuit board assembly. The QFN package under study consists of 68 leads around the perimeter of the device at a 0.5mm lead pitch. Four physical factors are analyzed to improve package reliability. The four factors are: mold compound, lead finish, adding solder bumps to the leadless pads, and solder mask removal underneath component. The research indicates the relative importance of each factor to package reliability.

Dedication

To my beautiful wife, Dana Mischel Levin, for her endless love, support and patience and to our sons, Spencer and Andrew.

Acknowledgements

I like to thank Romano Annecchiarico for his help in running the daisy-chained thermal cycling life tests, Roland Keene for his help in PCB layout of the daisy-chained test board, Mark Elkins at Flextronics and David Evans at Teradyne.

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List of Acronyms

AOI	Automated Optical Inspection
ASIC	Application Specific Integrated Circuit
ATE	Automated Test Industry
AXI	Automated X-ray Inspection
CDF	Cumulative Distribution Function
CDU	Cooling Distribution Unit
CSMR	Comprehensive Surface-mount Reliability
CTE	Coefficient of Thermal Expansion
EDS	Energy Dispersive Spectroscopy
HALT	Highly Accelerated Life Test
HASS	Highly Accelerated Stress Screen
HFE	Hydrofluoroethers
HQFN	High-Power Quad Flat No Lead
ICT	In-circuit Test
IPL	Inverse Power Law
LCCC	Leadless Ceramic Chip Carrier

MLF	MicroLeadFrame™
PCB	Printed Circuit Board
PMU	Parametric Measurement Unit
POS	Proof of Screen
PPM	Part Per Million
QFN	Quad Flat No-lead
RNET	Resistor Network
SMCSP	Very-Thin Quad Flat No Lead
UTAC	United Test and Assembly
VQFN	Very-Thin Quad Flat No Lead

Chapter 1: Introduction

The semiconductor industry's drive for component miniaturization results in new package innovation that can significantly impact package reliability and requires modeling and testing before implementation. Such is the case for the Quad Flat No-lead (QFN) package with a bottom-side thermal paddle. In recent years, this package has gained wide acceptance in the electronic industry. The QFN package gained wide acceptance and is being used in mobile communication, automotive, consumer products and personal computers. Amkor has shipped over one billion of these packages for electronic products[1]. The QFN package has become very popular due to its small size and package thinness. The QFN package has been classified as the fastest growing package in the semiconductor industry[2].

The QFN package is offered by several package manufacturers in different package versions and under different names. Amkor developed a MicroLeadFrame™ (MLF), United Test and Assembly (UTAC) offers a High Power Quad Flat No lead (HQFN) package, there is a Very Thin Quad Flat No lead (VQFN) and a Smart Metal Chip Scale Package (SMCSP) package. The advantage offered by all these packages is an improvement in performance for high speed performance and high thermal applications.

Heat generated inside the QFN package is dissipated through the bottom thermal paddle. The primary source of heat transfer is from the bottom-side paddle which is thermally bonded to the circuit die. The bottom-side paddle is soldered to the printed circuit board which provides the path for heat removal. The heat generated from the QFN package is dissipated through the circuit board and limited by the amount of heat that can be safely removed through the circuit board. To remove more heat from the QFN package, a different method for heat removal is needed.

To improve the thermal performance of the QFN package, the bottom-side paddle can be moved to the top-side of the device. With this package configuration, the topside paddle can be directly cooled through a heat sink, cold plate or similar higher efficiency thermal transfer mechanism. The top-side paddle is still thermally bonded to the circuit die, but the die has been flipped around. Flipping the circuit die around will result in pin location incompatibility with the old configuration.

The top-side thermal paddle can improve electrical performance because the thermal resistance is lowered resulting in a lower die junction temperature. The lower junction temperature allows the device to provide an increase in power output and can improve reliability. The QFN package with bottom-side paddle has been studied for package reliability and is well understood. The QFN package with top-side paddle is relatively new; there is little package reliability data available. The majority of the reliability research on QFN packages with topside paddle has been for small devices, 5 mm or less.

There is a concern that moving the paddle to the top-side will increase the strain at the solder connection due to a change in temperature. The strain increases at the solder-joint due to two primary factors. First, there is a reduction in soldered surface area that results from moving the paddle to the top side. The second factor is the effect the thermal paddle plays in increasing the effective CTE of the package.

1.1 Project Background

My interest in QFN packages started when thermal modeling for a new ASIC design showed the die running close to its upper operational temperature limit for a 10 year useful life. Package thermal modeling showed that moving the thermal paddle from the bottom to the top-side and cooling the device with a liquid coldplate reduced the junction temperature by over 10 degrees C. Finite-element analysis for the new package design showed that stress to the corner solder joints would increase due to CTE mismatch but solder-joint attachment would not be an issue over the 10-year useful life of the product. Unfortunately, no testing was planned to validate the assumptions made in the finite element model for solder-joint reliability. The QFN with top-side paddle was then designed into the new instrument for the automated test industry (ATE). During production validation testing, a Highly Accelerated Stress Screen (HASS) was defined based on the hard and soft failure limits under environmental stress. The purpose of the HASS screen is to identify manufacturing and component defects plus reliability design escapes before the product ramps to volume production. The upper and lower

environmental stress limits were determined during Highly Accelerated Stress Test (HALT). The environmental stresses that are imposed in HALT and HASS are composed of temperature, vibration and a combination of temperature and vibration while the product is under normal operation. Both the HALT and HASS test are performed while the instrument is actively running with diagnostics software that monitors for proper operation.

Before the HASS profile can be released to production, a Proof of Screen (POS) is performed to verify the usefulness of the HASS profile. The POS applies a repetitive HASS profile composed of temperature cycling, random vibration and combinational temperature and vibration stress to the product in development. The POS test repeats the HASS profile a minimum of 20 times to verify it does not take significant life out of the product or damage good product. It was discovered during the POS test that the QFN package suffered from an intermittent electrical connection that was then traced back to a fractured solder joint. After four HASS cycles, cracks in the corners of the solder joints of the QFN package were discovered (Figure 1). The solder fractures appeared to go completely across the solder connection. A cross section of the failed solder-joint showed an unusually large separation in the Z-plane (Figure 2). It was unclear if the stress causing failure was shear or tensile. If the failure is due to thermal stress from coefficient of thermal expansion (CTE) mismatch, then the stresses are expected to be shear and have little z-plane contribution.

This project analyzes the solder-joint reliability of a 68 pin QFN package with top-side paddle.

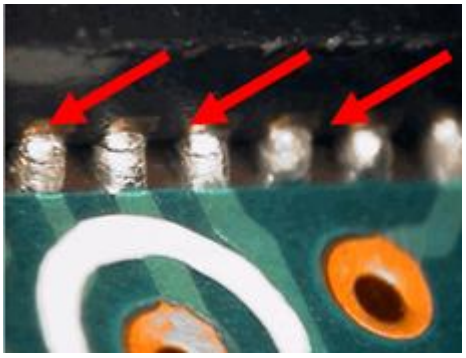


Figure 1 Solder cracks found during HASS/POS testing

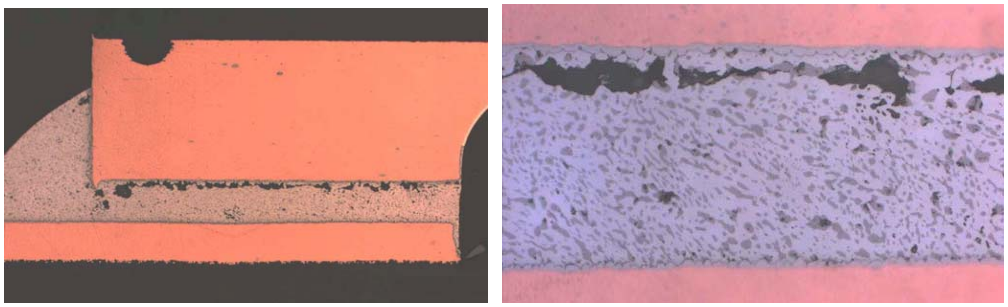


Figure 2 Solder fracture showing cohesive separation in the solder

During design validation, a similar solder-joint failure was discovered in a Highly Accelerated Life Test (HALT). The HALT protocol consisted of temperature step stress from -40^{o}C to +120^{o}C and vibration step stress from 0 Grms to 60 Grms. Each stress is applied individually and then jointly to discover the soft and hard failures in the design

and identify manufacturing and component defects. The HALT failure was attributed to a problem with the manufacturing process. The manufacturer had problems with the vision system used to place the component on the circuit board with solder paste. The parts that were placed incorrectly went through reflow and all had to be reworked. The manual rework process was faulty and resulted in solder opens. The problem was traced to a vision system which confused corner pin with the reference orientation feature on the device. Unfortunately, the manufacturing issues masked the solder-joint reliability problem.

1.2 The QFN Package and Mechanical Properties

The QFN package has gained wide acceptance in the electronics industry. Newer versions are emerging that are extending the package size limits making larger and smaller QFN packages. On the miniaturization side, there are Micro Ultra-thin QFNs that are 1 mm x 1mm in size with the package height dropping from 1.0 mm to 0.5 mm. On the large end, QFN packages are approaching 10 mm x 10 mm in size. As the package size increases, reliability concerns arise regarding the CTE mismatch between the low CTE package and the higher CTE of the circuit board.

The standard commercial QFN package incorporates a center thermal paddle on the bottom-side of the package (Figure 3). The paddle is directly attached to the die through a thermally conductive adhesive. Power, ground and signal I/Os are transferred from the

silicon die to the board through a lead frame. Gold wires are bonded from the die to the paddle and lead frame. The lead frame, die and wire bonds are then encased in plastic mold compound with a relatively low CTE. The bottom of the thermal paddle is exposed and tin plated for solderability. During assembly, the paddle is soldered to a printed circuit board and provides an avenue for heat removal generated in the device through the circuit board. The bottom paddle provides mechanical attachment support to the circuit board. Moving the thermal paddle from the bottom to the top of the package reduces the surface area for solder attachment by 88%. The advantage of the thermal paddle on the top-side of the package is that it provides improved thermal efficiency.

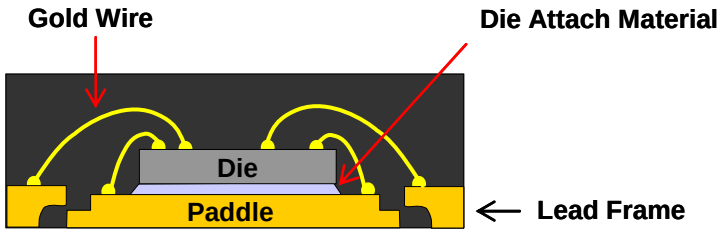


Figure 3 Standard QFN with bottom-side paddle

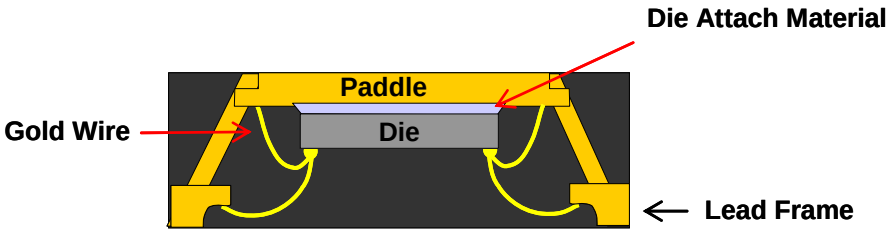


Figure 4 QFN package with top-side paddle

The QFN package with topside paddle is relatively new to the electronics industry and there is little research regarding its solder-joint reliability. There is not a significant amount of published data regarding the long term reliability of this package. One of the major concerns is the role the center paddle plays in the long term reliability of the solder joint. The center paddle provides the largest solderable surface area for the package (Figure 5). Approximately 80 percent of the soldered surface area is under the thermal paddle. The solder paste pattern for this device is shown in Figure 6.

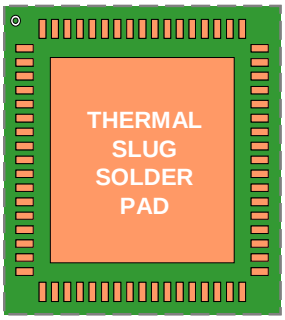


Figure 5 Circuit board land pattern for QFN with bottoms side paddle

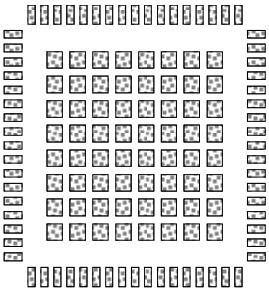


Figure 6 Solder paste pattern for QFN with bottoms side paddle

In contrast, when the paddle is moved from the bottom-side to the top, lead attachment is only around the perimeter of the package (Figure 7). With so much of the soldered surface area removed and the inherent CTE mismatch between the package and circuit board, the larger package size becomes a reliability concern.

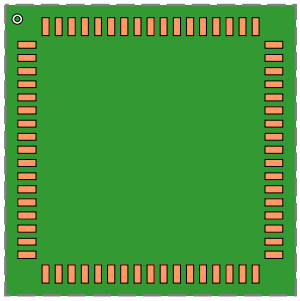


Figure 7 Circuit board land pattern for QFN with top-side paddle

The reliability requirement for the QFN package is 10 years in a customer use environment. The customer use environment is defined as 20^{o}C ambient in the "off state" and 38^{o}C worst case operating condition in a power cycled "On State". The system is power cycled three times per week. This project evaluates the reliability of the solder-joint attachment of a QFN paddle up based on accelerated life testing and stress strain modeling. The accelerated life cycling test data is used to form an acceleration model to estimate the solder-joint reliability based on a 10-year user model.

The QFN package under study is comprised of a metal lead frame that is wire bonded to the silicon die and thermal paddle. The QFN package is 10 mm square in size and manufactured by Maxim, Inc. (Figure 8). The lead pitch is 0.5mm and there are 68 leads

around the perimeter of the device. A 7mm square silicon die is attached to the bottom-side of the paddle and bonded using Ablebond 8200T thermal die attach compound. The lead frame and component leads are tin plated over a C194 copper frame. Gold wires are bonded from the die to the thermal paddle and perimeter leads. The lead frame with bonded die and wire bonds goes through a plastic injection molded process using a Sumitomo low CTE material called G770HCD. The lead frame provides centering alignment during the molding process and is done in a wafer tray. After injection molding, the devices are singulated from the tray into single pieces. The coefficient of thermal expansion for the various materials comprising the QFN package is listed in Table 1 and Figure 9.

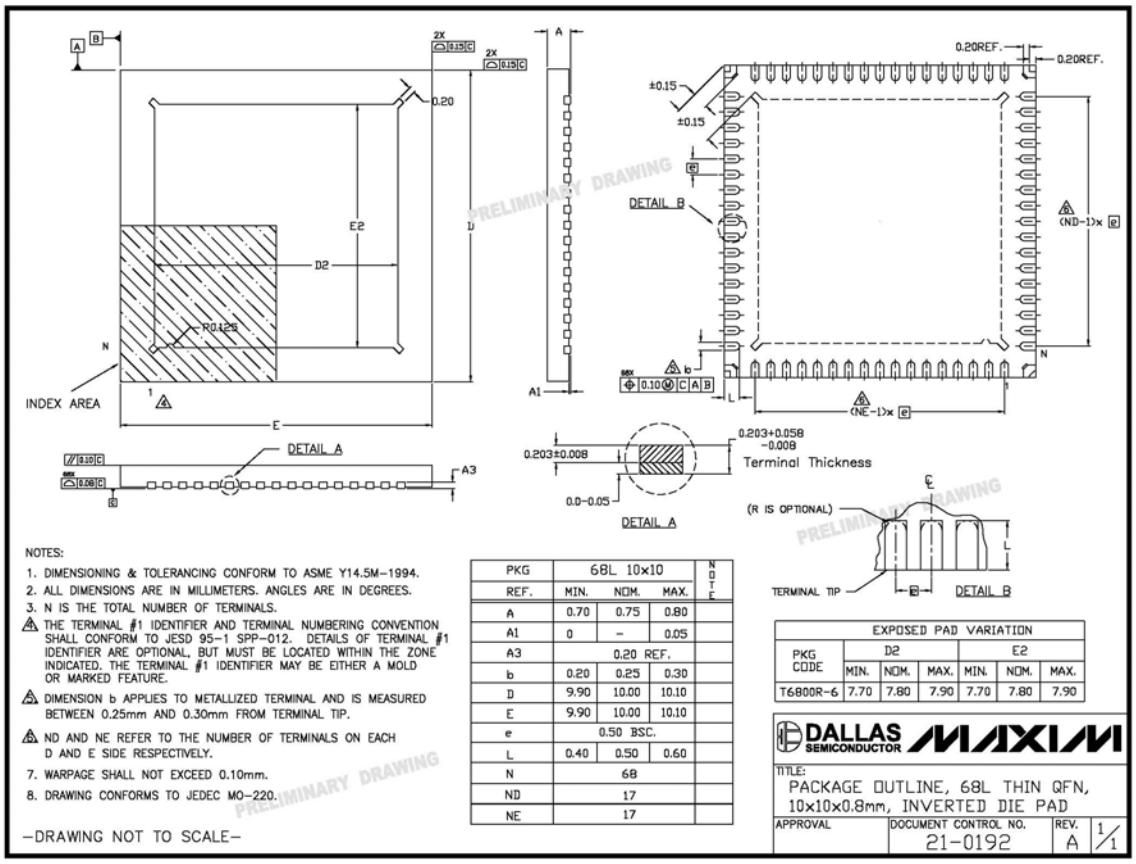


Figure 8 Maxim outline drawing for 10mm QFN package (supplier drawing)

AT23/MAX9979 68L 10x10 QFN Packaging material CTE

MATERIAL	COEFFICIENT OF THERMAL EXPANSION (CTE, um/m/°C, or ppm/°C;)
Lead frame (C194)	**16.7**
Die attach (Ablebond 8200T)	**61 (below Tg), 195 (above Tg), Tg: 83 'C**
Mold compound (Sumitomo G770HCD)	**7 (below Tg), 34 (above Tg), Tg: 135'C**
Silicon die	**3**
Gold wire	**14**
Tin (Sn)	**20.0**
Silver (Ag)	**19.0**
BCB (Benzocyclobutene, spin on Die Coating)	**40-50**

Table 1 Coefficient of thermal expansion for maxim 10 mm QFN package

EME-G770HCD

TYPICAL PROPERTIES:

ITEM	TEST METHOD	UNIT	VALUES
SPIRAL FLOW	SB-U-03-003	Cm	120
GEL TIME (at 175°C)	SB-U-03-005	Sec	40
THERMAL EXPANSION ∝1	SB-U-02-002	X 10^{-5} 1/°C	0.7
THERMAL EXPANSION ∝2	SB-U-02-002	X 10^{-5} 1/°C	3.4
Tg	SB-U-02-002	°C	135
THERMAL CONDUCTIVITY	SB-U-02-004	W/m •°C	100x 10^{-2}
FLEXURAL STRENGTH	SB-U-01-001	N/ mm^2	
(at 25°C)			190
(at 260°C)			28
FLEXURAL MODULUS	SB-U-01-002	X 10^2 N/mm^2	
(at 25°c)			290
(at 260°C)			9.0
SPECIFIC GRAVITY	SB-U-03-018	----------	2.04
VOLUME RESISTIVITY	SB-U-00-004	Ω - cm	1 x 10^{11}
(at 150°c)			
UL FLAME CLASS	SB-U-03-003	UL-94	V-0
WATER ABSORPTION	SB-U-03-002	% weight gain	0.14
(boiling, 24 h)			
EXTRACTED Na^+	SB-U-04-043	ppm	1
EXTRACTED Cl^-	SB-U-04-043	ppm	5

TYPICAL, NOT GUARANTEED PROPERTIES

MOLDING AND POST MOLD CURE CONDITIONS:

	STANDARD	RANGE
TRANSFER PRESSURE	80 x10^5 Pa	70-120 x10^5 Pa
MOLD TEMPERATURE	180°C	175-185°C
CURE TIME (C or A)#	A/90 sec	70-120 sec
POST-MOLD CURE TEMP	175°C	170-180°C
POST-MOLD CURE TIME	6 h	4-8 h

#Conventional or Auto

rev.May. '05

SUMITOMO BAKELITE CO., LTD.
Tennoz Parkside Building, 5-8 Higashi-Shinagawa, 2-Chome Shinagawa-ku, Tokyo 140, Japan

Figure 9 Sumitomo plastic injection mold compound (supplier data sheet)

Chapter 2: Manufacturing process for attaching QFNs to PCB

2.1 Assembly Process for Attachment of QFN to a Printed Circuit Board

The circuit board with QFN is assembled at a contract manufacturer using an automated process. The circuit board has components on both sides, so the assembly process goes through the assembly process twice. The first assembly process places parts on the bottom-side which tend to be smaller and lower profile. The second side assembly (top side) places the larger parts onto the circuit board. The QFN with top-side paddle are all placed on the top-side of the circuit board. A simplified assembly process is shown in Figure 10 and starts with screen printing solder paste onto the circuit board.

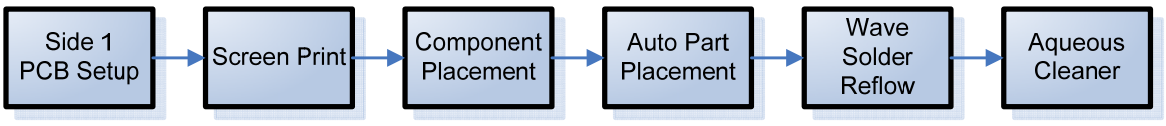


Figure 10 Assembly process flow for side 1

The screen printing process is fully automated and starts with a squeegee that moves solder paste over a stencil with openings in areas where solder paste is desired on the circuit board. The stencil thickness is 5 mils and the aperture openings in the stencil are made with a laser etcher. The solder mask aperture is approximately the same size and

shape as the component lead pads on the circuit board. After solder paste screening, an optical scanner inspects the solder paste to ensure the correct of volume amount of solder paste is dispensed on critical components. The optical scanner also ensures that there is no bridging of solder pastes between circuit pads. A QFN with a 5 mil thick solder paste pad will have between 2.0 and 2.5 mils of solder height after reflow soldering. The solder used is a eutectic Sn63/Pb37. After screening solder paste, the circuit board goes through an automated pick and place process. During this process, parts are automatically selected with a spring loaded vacuum pick up tool. Larger parts are optically inspected and aligned on the pickup tool before being placed onto the circuit board. For the QFN with top-side paddle up, an optical scanner determines pin one orientation for the part before placing it on the circuit board. After the parts are placed on the circuit board, it goes through a 4-stage convection reflow oven where the peak circuit temperature reaches 205^{o}C (Figure 11). The melting temperature for eutectic Sn63/Pb37 solder paste is 183C. The final step is a cleaning process where the boards goes through an aqueous cleaner to remove solder-flux residue.

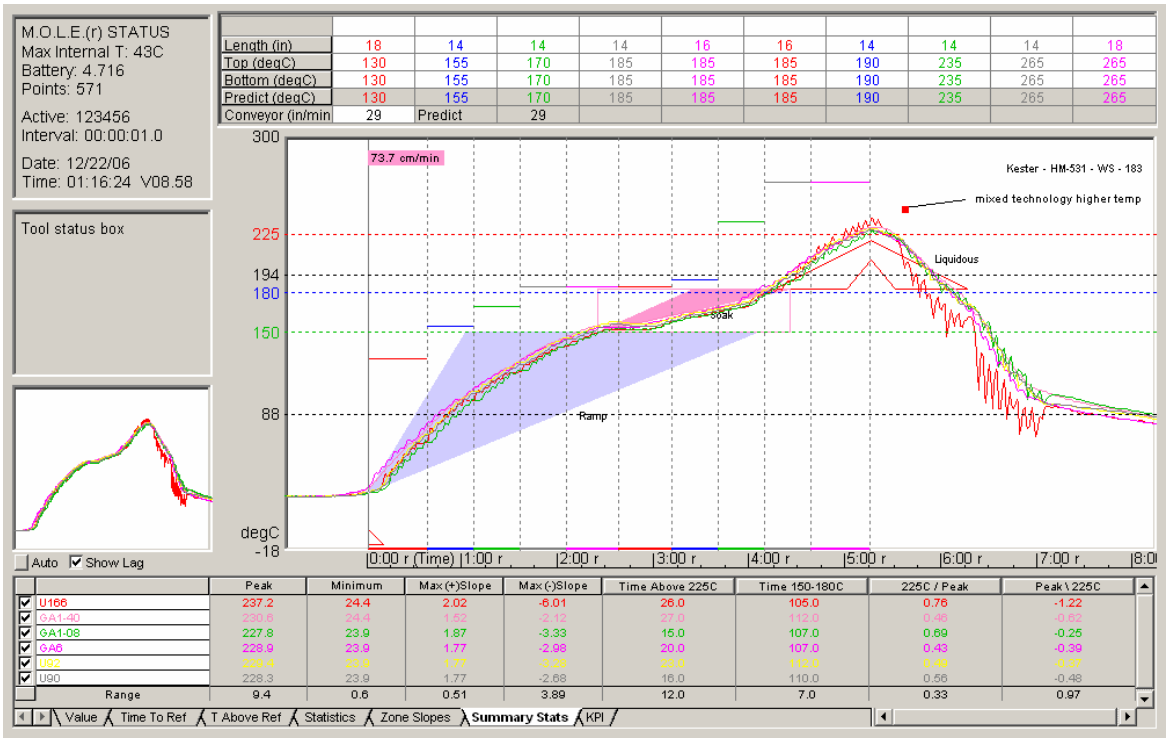


Figure 11 Solder reflow temperature profile through convection oven

After the board is assembled, it goes through a series of inspection and tests processes to ensure reliability (Figure 12). The Manufacturing inspection and test process starts with automated optical inspection (AOI) and automated x-ray inspection (AXI) followed by in-circuit test (ICT) to look for open and short solder connections along with missing and improperly placed components. After the circuit board passes inspection and in-circuit test, it is sent to functional test to verify that the components placed are operating within specification. After the board passes functional test it is sent to final assembly where a coldplate is mounted to the top-side of the circuit board. At this point, it is a complete assembly ready for final test. The circuit board at this stage meets product specifications but has not been screened for latent defects. Two test are performed to precipitate and attack latent defects. The first test is called HASS (highly accelerated stress screening). HASS is environmental stress screening that has two parts. The first part is an accelerated precipitation stress that applies temperature and vibration stress to the board under power and operation. The second phase applies a temperature stress at the upper spec limit along with a low-level tickle vibration. HASS is followed by burn-in at 50^{o}C. During burning the circuit board is tested at the upper and lower voltage margins along with power cycling. The burn in test runs for 48 hours and requires error free operation in order to pass. Before the product is considered complete, a final test to the customer

configuration is performed. The complete manufacturing assembly and test process is illustrated in Figure 12.

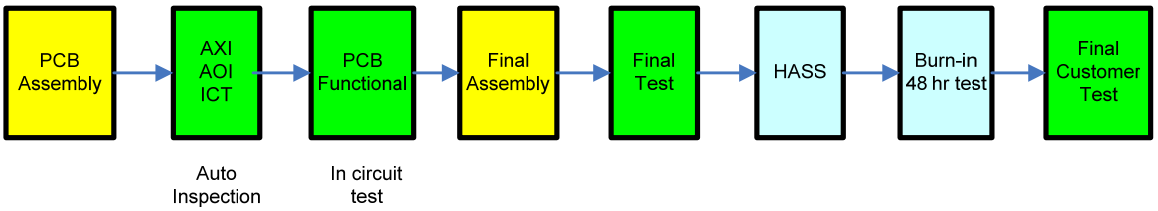


Figure 12 - Manufacturing inspection and test process

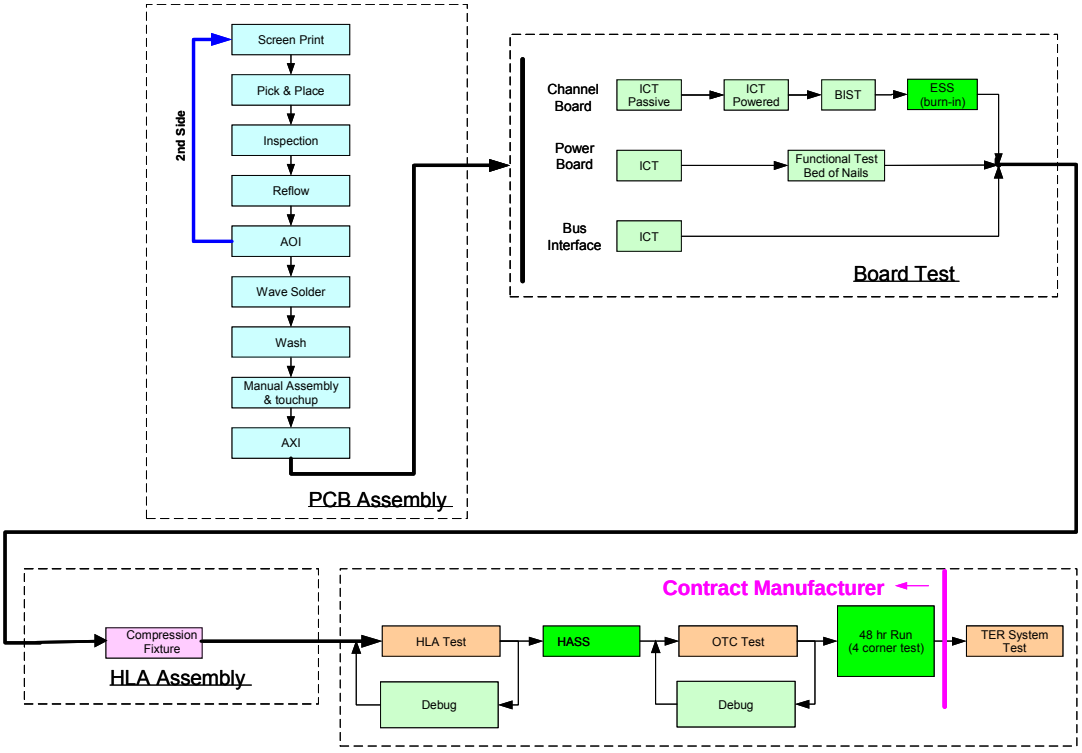


Figure 13 Complete assembly and test process

2.2 Circuit Board Design Information

The QFN package is attached to a 0.125" printed circuit with 28 layers of signal, power and ground planes. The power and ground planes are made up of one and two ounce copper planes. The signal planes are constructed of half-ounce copper. The parts are mounted on a printed circuit board with an outline dimension of 16 inches by 20 inches. The printed circuit board is large and has a significant amount of thermal mass. An illustration of a mounted QFN package is shown in Figure 14. The yellow arrow points to the QFN package with top-side thermal slug. The silver reflective square is the top-side thermal paddle. The QFN's lead pitch is 0.5mm, which prevents making the width of the solder pads wider than the device. It also prevents solder paste over print to increase solder height because the risk of a solder bridge is significant. The printed circuit board is Nelco 4000-13-EP, a fiberglass material with a CTE of $7x10^{-6}/^{o}C$.

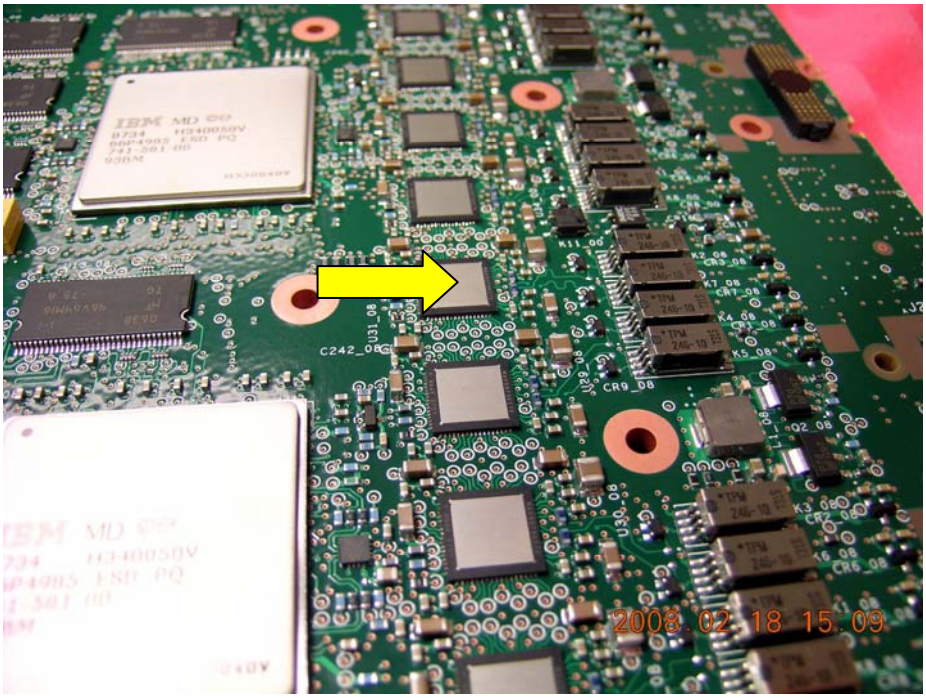


Figure 14 Yellow arrow shows QFN with top-side paddle

The QFN package component land patterned datasheet for the printed circuit board is illustrated in Figure 15. The land patterned data sheet illustrates what the pad pattern looks like on the circuit board. The datasheet includes the size and location for the thermal vias, the lead pad size and location, silk screen pattern and pin one reference location along with package to keep out zones to allow for rework. The component land patterned datasheet is also provided to the contract manufacturer for assembly purposes. The contract manufacturer uses the data sheet to determine package height and pin references to determine component placement.

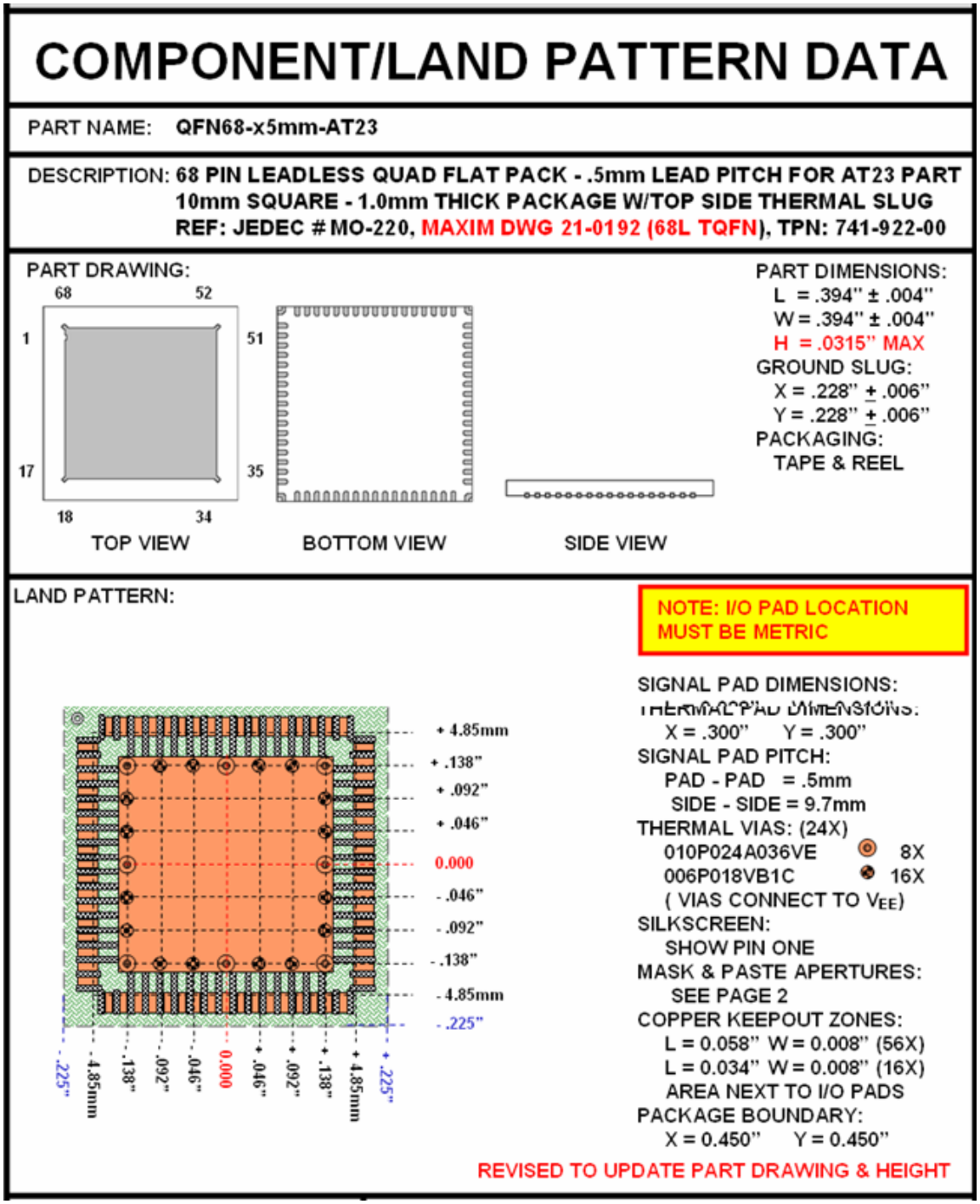


Figure 15 Teradyne data sheet for PCB layout

The part's fine pitch, 0.5mm, prevents making the width of the solder pads wider than the device leads width. It also prevents using solder paste over print to increase the solder height because the risk of a solder short is significant. The printed circuit board is Nelco 4000-13-EP a fiberglass material with a CTE of 7x10-6/^{o}C. The second page of the land patterned datasheet includes the solder mask and solder paste aperture (Figure 16). The component's fine lead pitch does not allow for solder mask between the component leads. This increases the risk of solder bridging between adjacent leads. The solder paste aperture is used by the contract manufacturer to design a stencil for dispensing solder paste.

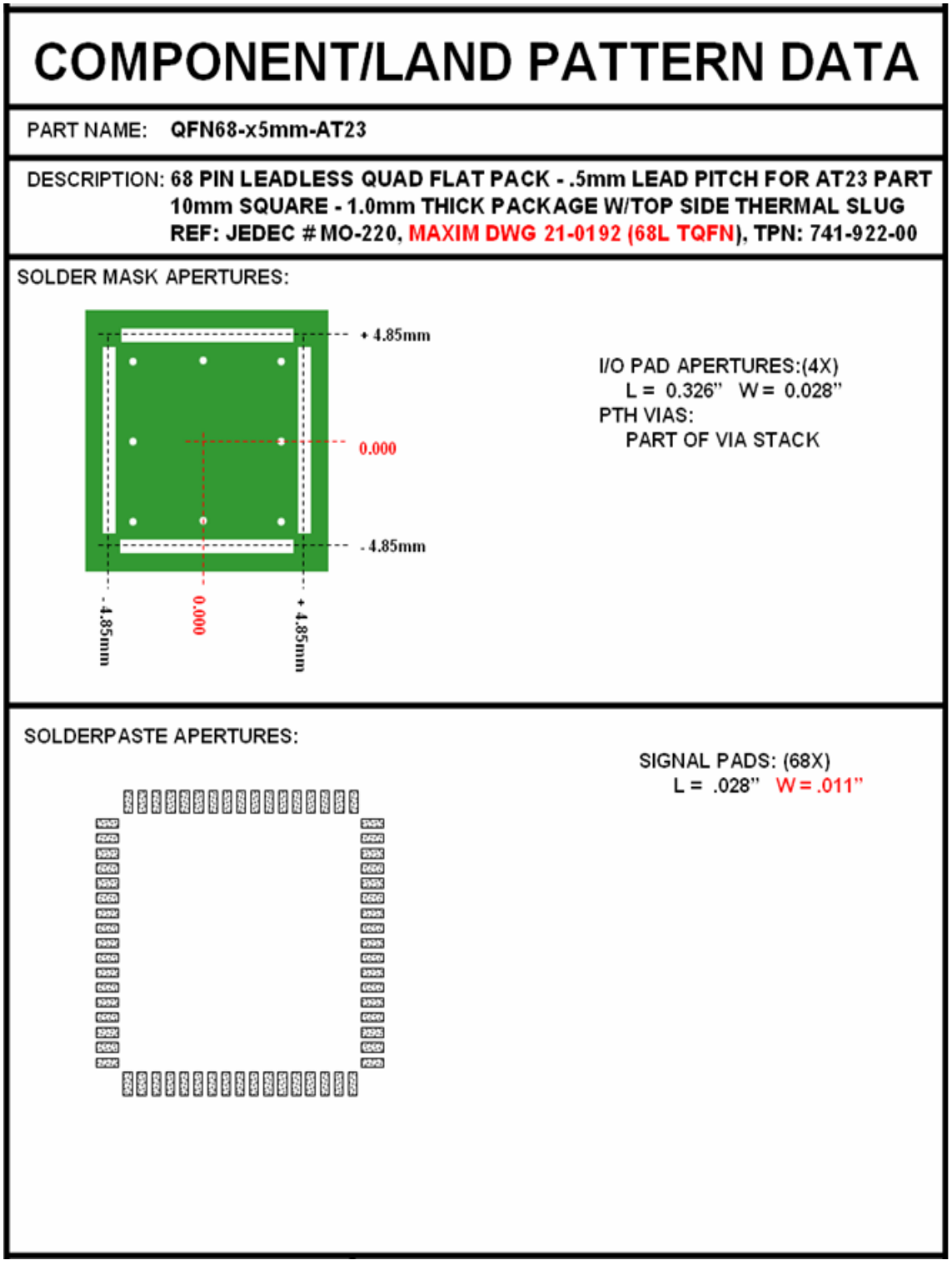


Figure 16 Teradyne data sheet for solder mask and solder paste aperture

Chapter 3: QFN Solder-Joint Life Models

3.1 Introduction

Temperature, vibration and the shock are three most common environmental stresses to impact solder-joint reliability. The solder-joint reliability model is different for each of these stresses. Before an analysis can be performed it is necessary to determine the stress or stresses that are involved in the failure of a solder joint. For my application, shock is not a likely failure because of the limited amount of handling it sees. The greatest level of vibration the product experiences occurs in shipping. A significantly lower source of vibration comes from forced convection fans and liquid cooling running through a coldplate. The vibration level from both of these stresses has been measured and found to be small.

Therefore, the environmental stress the product is most susceptible to under normal operating conditions is temperature change. There are two sources of thermal stress. The first is from power cycling, which results in a worst-case package-temperature increase from 20^{o}C ambient to 38^{o}C. The second thermal cycling stress is from the instrument running test programs that result in a worst case thermal swing of 2^{o}C. An analysis of the local and global strains for the two different thermal stresses will provide an estimate of the amount of damage that can be expected due to thermal mismatch.

The mechanical reason why a solder-joint fails is varied and is influenced by environmental stress factors like temperature, humidity and vibration. How these environmental stresses are imposed on the product plays a significant role in the physics of failure. Stresses that are monotonic have a different influence than cyclical stresses. The time under stress influences factors like solder creep. For solder creep to take place, there needs to be sufficient time for stress relaxation to take place. If the stress is constantly changing, the stress fatigue is less likely to be creep fatigue. Physical factors like intermetallic formations, grain structure and size, solder-joint height, lead compliance and material glass transition and expansion, thermal expansion rates play a significant role.

3.2 Thermal Mismatch Evaluation

There have been numerous published papers describing solder-joint failure mechanism due to thermal cycling materials that expand and contract at significantly different rates. The problem of CTE mismatch is greater when there is little lead compliance to share the load. The combination of significant CTE mismatch, large package size and low lead compliance typically leads to low-cycle fatigue. [3, 4, 5, 6] A cross sectional view of the QFN soldered to the circuit board is shown in Figure 17.

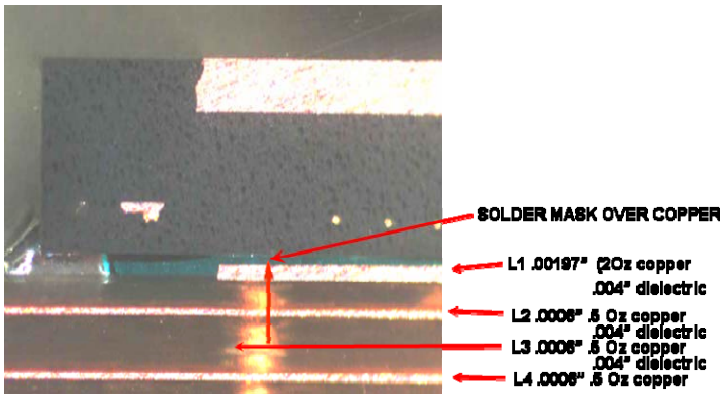


Figure 17 Cross sectional view of a QFN mounted to a printed circuit board

The QFN mold compound, solder and circuit board have significantly different thermal expansion rates. A change in temperature will cause each to expand at different rates and since they are mechanically bonded together stress is induced in the assembly. The weakest link in this bonded assembly is the solder joint, which is the most likely source of failure.

3.3 Stress Strain Effects due to CTE Mismatch

The global strain is due to the mismatch between the QFN and the circuit board. There are two local strains to consider. The first local strain is between the QFN and solder and the second local strain is between the solder and circuit board. A simplified cross section of a soldered QFN package with the expansion rates for the QFN, eutectic solder and PCB is shown in Figure 18.

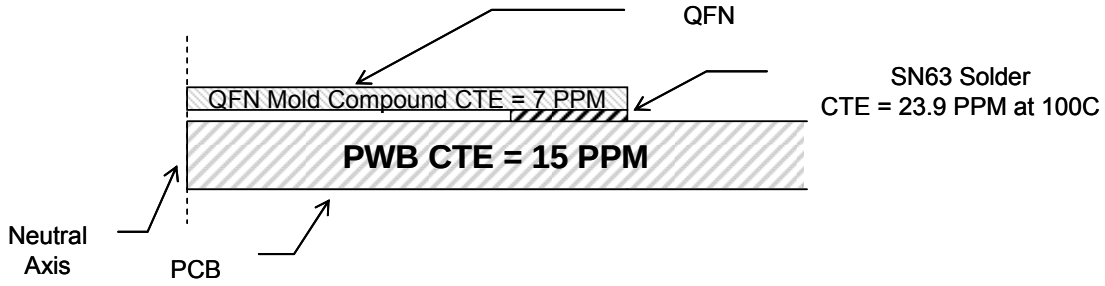


Figure 18 QFN cross sectional view with thermal CTE's

From a simplified perspective, there are three materials involved in the attachment of the QFN package to the printed circuit board. The three materials are: the QFN mold compound, the eutectic solder and the circuit board substrate. These three materials that hold the structure together expand at different rates. The coefficient for thermal expansion for these three materials is shown in Table 2. There are other factors that influence the expansion rate that are better suited for a finite element model. For example, the top copper paddle, silicon die, epoxy adhesive for die attach and copper lead frame all influence the effective CTE of the QFN package. However, it is not possible to account for these factors without using finite element analysis.

MATERIAL	COEFFICIENT OF THERMAL EXPANSION (CTE, um/m/°C, or ppm/°C;)
Nelco 4000-13-EP, fiberglass material	**7x10-6/°C**
Eutectic Sn63/Pb37	**23.9x10-6/°C**
Mold compound (Sumitomo G770HCD)	**7x10-6/°C (below Tg)**
	34x10-6/°C (above Tg), Tg=135'C

Table 2 Coefficient of Thermal Expansion for QFN attachment materials

To calculate the stress and strain values due to the different thermal expansion rates for the soldered QFN package, the physical size and cross sectional area for each element needs to be defined. The physical size of the package and soldered surface area has a strong influence on the amount of stress that is developed due to thermal expansion. Structures that are large will experience greater stress from thermal expansion than smaller structures. This is because the amount of expansion due to temperature is the product of the thermal expansion rate of the material described in PPM/^{o}C, multiplied by the diagonal distance from the neutral point to furthest corner. The two structures whose size needs to be defined are the QFN package and solder-joint land pad.

To determine the change in size to the QFN package due to a change in temperature, the distance from the neutral point to the package end is needed. For a square package, the neutral point is the center of the package. The distance from the center of the package to the corner of the device can be determined using Pythagorean's theorem equation as follows:

$$Z = \sqrt{\left(\frac{x}{2}\right)^2 + \left(\frac{y}{2}\right)^2} \qquad (1)$$

The diagonal distance from the neutral point to furthest corner for the solder-pad and QFN are shown in Figure 19 and Figure 20.

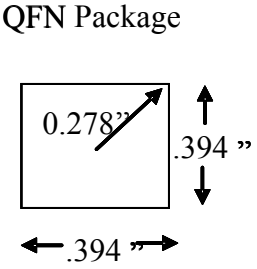


Figure 19 QFN cross sectional view

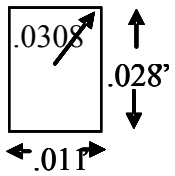


Figure 20 PCB land pad geometry

The equation for global strain γ_G due to temperature expansion is:

$$\text{Global Strain } \gamma_G \leq \frac{L(\Delta CTE)(\Delta T)}{h_S} \tag{2}$$

$$\text{Global Stress}(\tau_G) = \gamma_G \times G \tag{3}$$

Where:

L is diagonal distance from the neutral point to furthest corner

ΔCTE is the thermal expansion rate PPM/^{o}C

ΔT is the change in temperature (^{o}C)

h_s is the height of the solder-joint (inches)

$G =$ shear modulus of elasticity

Two thermal cycling stresses are proposed to develop a model for the failure distribution and acceleration factor. The two tests are:

Accelerated thermal cycling stress test #1 method #1:

High temperature: 70^{o}C

Low temperature: -25^{o}C

Dwell time at set point: 20 minutes

Temperature ramp rate: 60^{o}C/minute

The global strain induced from thermal cycle test #1 is:

$$\text{Global shear strain} = \gamma_G \le \frac{L\left(CTE_{PWB} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S}$$

$$\gamma_G \le \frac{0.2783\left(15\times10^{-6} - 7\times10^{-6}\right)\left(70-\left(-25\right)\right)}{0.0025} = 84.603\times10^{-3} = 8.4\%$$

$$\text{Shear Stress}\left(\tau_G\right) = \gamma \times G = \left(8460\times10^{-3}\right)\left(6909MPa\right) = 58.45MPa > \text{yield stress } 9.6 \text{ MPA}$$

The equation for global strain γ_G due to temperature expansion is:

$$\text{local shear strain} = \gamma_L \le \frac{L_{Solder}\left(CTE_{Solder} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S} + \frac{L\left(CTE_{Solder} - CTE_{PWB}\right)\left(T_{Max} - T_{\min}\right)}{h_S} \tag{4}$$

The local strain from accelerated thermal cycling test #1 is:

$$\text{local shear strain} = \gamma_L \le \frac{L_{Solder}\left(CTE_{Solder} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S} + \frac{L\left(CTE_{Solder} - CTE_{PWB}\right)\left(T_{Max} - T_{\min}\right)}{h_S}$$

$$\gamma_L \le \frac{0.0308\left(23.9\times10^{-6} - 7\times10^{-6}\right)\left(95\right)}{0.0025} + \frac{0.0308\left(23.9\times10^{-6} - 15\times10^{-6}\right)\left(95\right)}{0.0025} =$$

$$= 0.01978 + 0.01042 = 30.02\times10^{-3} = 3.0\%$$

$$\text{Shear Stress}\left(\tau_L\right) = \gamma \times G = \left(3.1046\times10^{-3}\right)\left(6909MPa\right) = 21.45 \text{ MPa} > \text{yield stress } 9.6\text{MPA}$$

Accelerated thermal cycling stress test #1 method #2:

High temperature: 100^{o}C

Low temperature: 0^{o}C

Dwell time at set point: 20 minutes

Temperature ramp rate: 60^{o}C/minute

The global strain induced from thermal cycle test #1 is:

$$\text{Global shear strain} = \gamma_G \le \frac{L\left(CTE_{PWB} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S}$$

$$\gamma_G \le \frac{0.2783\left(15\times10^{-6} - 7\times10^{-6}\right)\left(100-0\right)}{0.0025} = 84.603\times10^{-3} = 8.9\%$$

$$\text{Shear Stress}\left(\tau_G\right) = \gamma \times G = \left(8.908\times10^{-3}\right)\left(6909MPa\right) = 61.53MPa > \text{yield stress } 9.6 \text{ MPA}$$

The equation for global strain γ_G due to temperature expansion is:

$$\text{local shear strain} = \gamma_L \le \frac{L_{Solder}\left(CTE_{Solder} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S} + \frac{L\left(CTE_{Solder} - CTE_{PWB}\right)\left(T_{Max} - T_{\min}\right)}{h_S}$$

The local strain is:

$$\text{local shear strain} = \gamma_L \le \frac{L_{Solder}\left(CTE_{Solder} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S} + \frac{L\left(CTE_{Solder} - CTE_{PWB}\right)\left(T_{Max} - T_{\min}\right)}{h_S}$$

$$\gamma_L \le \frac{0.0308\left(23.9\times10^{-6} - 7\times10^{-6}\right)(95)}{0.0025} + \frac{0.0308\left(23.9\times10^{-6} - 15\times10^{-6}\right)(100)}{0.0025} =$$

$$= 0.0208 + 0.01097 = 30.02\times10^{-3} = 3.2\%$$

$$\text{Shear Stress}\left(\tau_L\right) = \gamma \times G = \left(3.1046\times10^{-3}\right)\left(6909 MPa\right) = 21.96 \text{ MPa} > \text{yield stress } 9.6\text{MPA}$$

Accelerated thermal cycling stress test #2:

High temperature: 70^{o}C

Low temperature: 0^{o}C

Dwell time at set point: 20 minutes

Temperature ramp rate: 60^{o}C/minute

The global strain from accelerated thermal cycling test #2 is:

$$\text{Global shear strain} = \gamma_G \le \frac{L\left(CTE_{PWB} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S}$$

$$\gamma_G \le \frac{0.2783\left(15\times10^{-6} - 7\times10^{-6}\right)\left(70-(0)\right)}{0.0025} = 62.339\times10^{-3} = 6.2\%$$

$$\text{Shear Stress}\left(\tau_G\right) = \gamma \times G = \left(8.908\times10^{-3}\right)\left(6909MPa\right) = 61.53MPa > \text{yield stress } 9.6 \text{ MPA}$$

The local strain from accelerated thermal cycling test #2 is:

$$\text{local shear strain} = \gamma_L \le \frac{L_{Solder}\left(CTE_{Solder} - CTE_{comp}\right)\left(T_{Max} - T_{\min}\right)}{h_S} + \frac{L\left(CTE_{Solder} - CTE_{PWB}\right)\left(T_{Max} - T_{\min}\right)}{h_S}$$

$$\gamma_L \le \frac{0.0308\left(23.9\times10^{-6} - 7\times10^{-6}\right)(70)}{0.0025} + \frac{0.0308\left(23.9\times10^{-6} - 15\times10^{-6}\right)(70)}{0.0025} =$$

$$= 0.01457 + 0.00768 = 22.25\times10^{-3} = 2.2\%$$

$$\text{Shear Stress}\left(\tau_L\right) = \gamma \times G = \left(3.1046\times10^{-3}\right)\left(6909\,MPa\right) = 21.45 \text{ MPa} > \text{yield stress } 9.6\text{MPA}$$

Test #	Thermal Cycling Range	Global Strain	Local Strain
1	-35 °C to 65 °C	8.9%	3.2%
2	-25 °C to 70 °C	8.4%	3.0%
3	0 °C to 100 °C	8.9%	3.2%
4	0 °C to 70 °C	6.2%	2.2%
5	20 °C to 31.5 °C	1.0%	

Table 3 Summary Table for global and local strain

The total strain energy is the sum of the elastic and inelastic strain energy. The inelastic strain has two possible components; they are a plastic strain and creep strain energy. The total strain equation is:

$$\gamma_{total} = \gamma_{elastic} + \gamma_{plastic} + \gamma_{creep} \quad (5)$$

The elastic strain is the least damaging and is dominant when the strains are 1% or less[7]. Above 1% strain, inelastic deformation begins to contribute. The strains from thermal cycling test #1 and test #2 both results in local and global strains that exceed 1%. Therefore, the thermal cycling tests will result in solder-joint failure from inelastic not elastic strain energy. The failures will also be low-cycle fatigue due to the high strain induced from thermal cycling.

There are two inelastic components possible that result in plastic fatigue and creep fatigue. The plastic strains are less damaging that the creep strains. The creep strains become a contributor when there is cyclical stress, dwell time and the temperature exceeds half the absolute melting temperature, T_m, of the material in degrees Kelvin[8]. The melting point for Sn63Pb37 is 456^{o}K. Therefore, creep becomes a contributor to inelastic strain at half its melting point, 228 ^{o}K (-45.15 ^{o}C). The creep fatigue increases with increasing temperature, the higher the temperature the greater the creep fatigue. Both thermal cycling tests are significantly above $0.5T_m$, so creep is considered to be a significant contributor to fatigue. Solder creep also promotes micro-grain structure weakening as the tin and lead regions begin to coalesce, forming larger tin and lead regions. Lead is ductile and provides compliance in the solder-joint structure. The tin is a brittle material. As the grain structure coarsens from thermal cycling, the tin regions

become bigger and make the solder connection more brittle and susceptible to stress fracture.

Based on the strain energy calculation for global and local strains from thermal cycling, previous stress test in HALT and POS, and published articles on solder-joint reliability of leadless devices; the failure model that best applies is a Coffin-Manson Inverse Power Law (IPL) model for low-cycle fatigue. The stress induced due to thermal cycling has three components. There is an elastic strain, a plastic strain and a metal-creep strain. The strains are too high to be elastic, so the primary mechanism is a combination of creep and plastic fatigue.

3.4 Reliability Modeling

There are many different models that incorporate time and temperature dependent behavior to estimate the solder fatigue life for a structure. The models are mostly analytical, but some combine modeling and experimental results, the models are[9]:

Damage Integral Method (Subrahmanyan et al, CHMT 1989)

Energy Partitioning Approach (Dasgupta et al, ASME, EEP, 1993)

Fracture Mechanics Based (Pao, CHMT 1992)

Matrix Creep Model (Shine & Fox, ASTM STP 942)

CSMR Model (Clech et al, 43rd ECTC)

Energy Density Based (Darveaux et al)

Four different models for solder-joint fatigue of a QFN leadless package mounted on epoxy fiberglass circuit board and exposed to thermal cycling are studied here. The first approach uses an Engelmaier's for strain energy model. The Engelmaier model uses an estimate of the strain energy due to temperature to determine the mean useful life of the structure. The second approach uses a Steinberg model that balances the forces present due to a change in temperature. The third approach combines published Amkor reliability data with published Weibull failure distribution plots for a QFN package paddle down to estimate the reliability of a QFN package paddle up. The last approach uses SRS version 1.1 software by Jean-Paul Clech for a leadless package.

The four 1st order modeling methods are:

Engelmaier Model for a leadless surface-mount device

Steinberg Model for a leadless surface-mount device

Published industry data for unsoldered bottom-side paddle

SRS 1.1 software by Jean-Paul Clech

3.4.1 Reliability Model #1: Accelerated Life Analysis Using Engelmaier Model

One of the simplest models for predicating solder-joint life for a leadless ceramic device can be found in IPC-SM785 and IPC-9701A[10], it uses the Engelmaier model for leadless

attachment[11]. The model provides a strain-rate calculation based on the maximum strain at the solder-joint due to a change in temperature and applies for SnPb solders. The model assumes the dwell time is sufficient for complete stress relaxation to take place[12]. This also requires that the dwell times used for accelerated life testing need to be sufficient for relaxation to take place. The Engelmaier model is derived from the generalized form for cumulative fatigue damage for metals by Morrow[13] and the Coffin-Manson plastic strain-fatigue life relationship for low-cycle fatigue [14]:

$$\overline{N}_f = C[\Delta W]^{1/C} = C[\Delta\gamma_P]^{1/C} \tag{6}$$

Where:

N_f= Shear fatigue life in thermal cycles

C is a material constant

c is a value between -0.5 and -0.7 for most metals

ΔW is the visco-plastic strain energy density per cycle

$\Delta\gamma_p$ is the applied cyclic strain range

The Engelmaier model for a stiff leadless surface-mount device modified to include a Weibull statistical distribution is:

$$N_f(x\%) = \frac{1}{2}\left[\frac{F\Delta\gamma_{\max}}{2\varepsilon_f}\right]^{\frac{1}{c}} \left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} \quad (7)$$

Where:

$$c = -0.442 - 6\times10^{-4}\,T_{sj} + 1.74\times10^{-2}\ln\left(1+\frac{360}{t_D}\right) \quad (8)$$

$$T_{SJ} = \left(\frac{T_{\max} - T_{\min}}{2}\right) \quad (9)$$

The Engelmaier strain range equation is:

$$\Delta\gamma_{\max} = \frac{L\Delta\alpha\Delta T}{h_s} \quad (10)$$

The shear strain range in the solder is proportional to the product of the cyclic temperature swing, the thermal mismatch between the component and circuit board, the diagonal distance from the neutral point to the device corner divided by the height of the solder joint. The strain energy represents the maximum strain that is developed in the solder-joint foe very long times. The solder-joint provides the compliance due to global shear strain and increasing solder height improves attachment reliability. A model of a quarter slice of the QFN attached to the printed circuit board is shown in Figure 21.

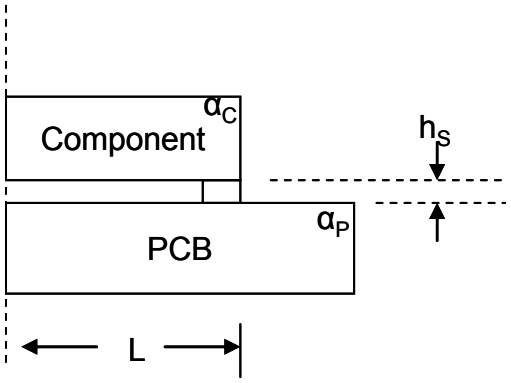


Figure 21 Simplified cross section of QFN attachment to circuit board

The Engelmaier model contains two parts; the first part is the Engelmaier equation for the mean life, which is:

$$N_f(50\%) = \frac{1}{2}\left[\frac{F\Delta\gamma_{\max}}{2\varepsilon_f}\right]^{\frac{1}{c}}$$

Unfortunately, the Engelmaier model provides a single point measure for the mean life. To use the model to predict a failure time that is different than the mean, a distribution modifier is needed. Since the failure mechanism is wearout, the two most appropriate distributions are a lognormal and a Weibull distribution with a shape factor, β that is 4.0 or greater. The

Weibull distribution model is:

$$\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta}$$

Combining the two equations results in a Engelmaier model with a Weibull distribution.

Where:

$\Delta\alpha = (\alpha_P - \alpha_C)$

ε_f' is a fatigue ductility coefficient, $2\varepsilon_f' = 0.65$ for near - eutectic tin lead solder (60Sn/40Pb & 63Sn/37Pb)

$\Delta\gamma_{max}$ is the maximum cyclic shear strain

F is an emperical "non - ideal" factor. Without data F = 1.

L is the distance to the nuetral point from the center of the component = 0.278"

$\Delta\alpha$ is the global thermal mismatch in - plane coeficient of expansion (between package and board)

$\Delta\alpha = (\alpha_P - \alpha_C) = (15\times10^{-6} - 7\times10^{-6}) = 8\times10^{-6}/^{o}C$

α_P is the coeficient of thermal expansion (CTE) for the circuit board

α_C is the coeficient of thermal expansion (CTE) for the QFN

ΔT is the change in temperature

t_d is the half cycle dwell time in minutes

T_{sj} is the mean cyclic solder joint temerature $(^{o}C) = \frac{T_{min} + T_{max}}{2}$ (11)

β is the Weibull shape parameter. If unknown, then 4.0 provides a good estimate for a leadless attachment.

h_S is the height of the solder-joint = 0.0025”

$N_f(x\%)$ is the number of thermal cycles to “x%” failure probability

x is the cumulative failure probability after N thermal cycles and is expressed in percent.

For thermal Cycling test #1 (-25° C to 70° C) :

$$T_{sj} = \frac{-25+70}{2} = 22.5$$

$$c = -0.442 - (6\times10^{-4})(22.5) + 1.74\times10^{-2}\ln\left(1+\frac{360}{20}\right) = -0.404$$

$$\Delta\gamma_{max} = \frac{L\Delta\alpha\Delta T}{h_s} = \frac{(0.2783'')(8.0\times10^{-6}/^{o}C)(95^{o}C)}{0.0025} = 84.6\times10^{-3}$$

$$N_f(1\%) = \frac{1}{2}\left[\frac{84.6\times10^{-3}}{0.65}\right]^{\frac{1}{-0.404267}}\left[\frac{\ln(1-(0.01)(1))}{\ln(0.5)}\right]^{1/4} = 29.2 \text{ cycles to failure}$$

$$N_f(50\%) = \frac{1}{2}\left[\frac{84.6\times10^{-3}}{0.65}\right]^{\frac{1}{-0.404267}} = 77.5 \text{ cycles to failure}$$

$$N_f(63.2\%) = \frac{1}{2}\left[\frac{84.6\times10^{-3}}{0.65}\right]^{\frac{1}{-0.404267}}\left[\frac{\ln(1-(0.01)(62.3))}{\ln(0.5)}\right]^{1/4} = 84.4 \text{ cycles to failure}$$

For thermal Cycling test #1 Method 2 (0^{o}C to 100^{o}C) :

$$T_{sj} = \frac{0+100}{2} = 50$$

$$c = -0.442 - \left(6\times10^{-4}\right)(50) + 1.74\times10^{-2}\ln\left(1+\frac{360}{20}\right) = -0.4208$$

$$\Delta\gamma_{\max} = \frac{L\Delta\alpha\Delta T}{h_s} = \frac{(0.2783")\left(8\times10^{-6}\ /^{o}C\right)\left(100^{o}C\right)}{0.0025} = 89.1\times10^{-3}$$

$$N_f(1\%) = \frac{1}{2}\left[\frac{84.6\times10^{-3}}{0.65}\right]^{\frac{1}{-0.404267}}\left[\frac{\ln(1-(0.01)(1))}{\ln(0.5)}\right]^{1/4} = 20 \text{ cycles to failure}$$

$$N_f(50\%) = \frac{1}{2}\left[\frac{84.6\times10^{-3}}{0.65}\right]^{\frac{1}{-0.404267}} = 56.3 \text{ cycles to failure}$$

$$N_f(63.2\%) = \frac{1}{2}\left[\frac{84.6\times10^{-3}}{0.65}\right]^{\frac{1}{-0.404267}}\left[\frac{\ln(1-(0.01)(62.3))}{\ln(0.5)}\right]^{1/4} = 62 \text{ cycles to failure}$$

For thermal Cycling test #2 (0°C to 70°C) :

$$T_{sj} = \frac{0+70}{2} = 35$$

$$c = -0.442 - \left(6\times10^{-4}\right)(30) + 1.74\times10^{-2}\ln\left(1+\frac{360}{20}\right) = -0.41177$$

$$\Delta\gamma_{\max} = \frac{L\Delta\alpha\Delta T}{h_s} = \frac{(0.2783")\left(8\times10^{-6}/^{o}C\right)\left(70^{o}C\right)}{0.0025} = 62.339\times10^{-3}$$

$$N_f(1\%) = \frac{1}{2}\left[\frac{77.924\times10^{-3}}{0.65}\right]^{\frac{1}{-0.41177}}\left[\frac{\ln\left(1-(0.01)(1)\right)}{\ln(0.5)}\right]^{1/4} = 51.5$$

$$N_f(50\%) = \frac{1}{2}\left[\frac{77.924\times10^{-3}}{0.65}\right]^{\frac{1}{-0.41177}} = 148.5$$

$$N_f(63.2\%) = \frac{1}{2}\left[\frac{77.924\times10^{-3}}{0.65}\right]^{\frac{1}{-0.41177}}\left[\frac{\ln\left(1-(0.01)(62.3)\right)}{\ln(0.5)}\right]^{1/4} = 161.7$$

Based on the Engelmaier model, the number of thermal cycles to failure is:

Test #	Thermal Cycling Range	N_f(1%)	N_f(50%)	N_f(63.2%)
1	0°C to 100 °C	20	56	62
2	-25 °C to 70 °C	29.2	78	84.4
3	0 °C to 70 °C	51.5	149	161.7

Table 4 Cycles to mean failure for Engelmaier model

3.4.2 Reliability Model #2: Accelerated Life Analysis Using Steinberg Model:

The second approach uses a Steinberg model for solder-joint fatigue life for a small surface-mounted Leadless Ceramic Chip Carrier (LCCC) exposed to rapid thermal cycling Figure 22. The Steinberg model [15]sets up an equilibrium equation for evaluation of thermal expansion forces and stresses that are induced in the solder-joint of a LCCC. Although the model was developed for a ceramic package, it applies equally well for a plastic package. Steinberg recommends keeping the CTE mismatch between the component and circuit board to less than 9 ppm/^{o}C to avoid solder-cracking problems. Obviously, the size of the component package plays a significant role in the amount of stress that is induced on the solder joint. In our application, the delta CTE between the circuit board and package is 8 ppm/^{o}C. When the circuit board expands at a greater rate than the package, stress is induced first on the solder-joint and then on the component which is bonded to the circuit board. In this case, the stress is transferred from the solder-joint to the component (Figure 23). The balanced displacement model requires the expansion forces for the circuit board (X_p) must equal the sum of the expansion forces for the solder-joint (X_s) and component (X_c).

$$X_C + X_S = X_P \tag{12}$$

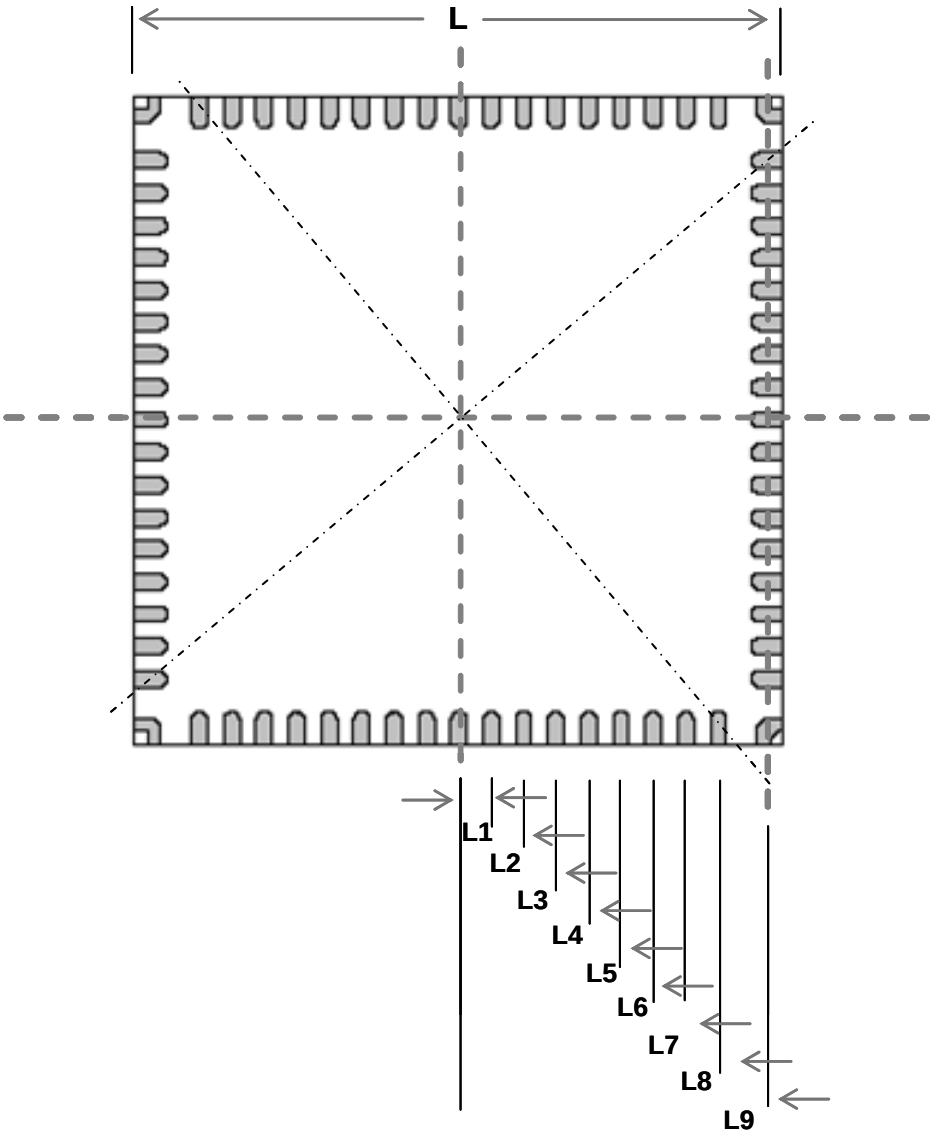


Figure 22 Dimensional Reference for a LCCC

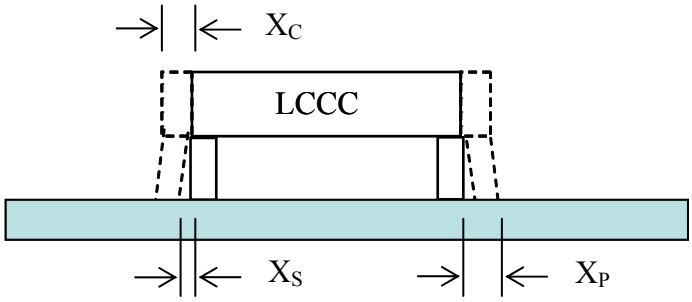


Figure 23 Stress induced from CTE mismatch between circuit board and package

The solder-joint displacement is defined as the product of the shear force (P_S) multiplied by the solder-joint height (h_S) divided by the product of the cross sectional area of the solder-joint (A_S) multiplied by the solder shear modulus (G_S).

$$X_s = \frac{(P_S)(h_S)}{(A_S)(G_S)} \tag{13}$$

The second displacement is due to the change in component package size. The maximum displacement occurs along the diagonal dimension of the QFN package. There are two forces acting to change the size of the package due to a change in temperature. The first is the unrestrained change due to thermal expansion of the package. The change due to thermal expansion (X_{C1}) is the product of the CTE of the component package (α_C), the distance from the component center to a solder-pad (L_C) on half the component and the change in temperature (Δt). There is a correction factor not included here that accounts for the neutral point of the package being the center. For a square device, the correction

factor is the square root of 2. The distance from the component center to the solder pad, L_C, includes all pads on half of the component package starting from the center to the corner. There are two pads at the center along the neutral point; they are not counted because they do not change with temperature. The most critical pad and most likely to fail first is the furthest diagonal pad.

$$X_{C1} = (\alpha_C)(L_C)(\Delta t) \tag{14}$$

The second force influencing expansion is due to the axial force (P_C) exerted on the component due to its thermal expansion (X_{C2}). This force is the product of the axial force (P_C) times the effective length (L_C) divided by the product of the solder-joint area (A_C) times the modulus of elasticity for the component package (E_C).

$$X_{C2} = \frac{(P_C)(L_C)}{(A_C)(E_C)} \tag{15}$$

The total component package displacement is:

$$X_C = X_{C1} + X_{C2} = (\alpha_C)(L_C)(\Delta t) + \frac{(P_C)(L_C)}{(A_C)(E_C)} \tag{16}$$

The final displacement is due the circuit board and it has two opposing components. The first component is the unrestrained change due to thermal expansion of the circuit board. The change in the circuit board size due to thermal expansion (X_{P1}) is the product of the

CTE of the component package (α_P), the length of the circuit board under the component package (L_P) and the change in temperature (Δt). The displacement is negative since it is being restrained by the force of the solder-joint and component package which is bonded to it.

$$X_{P1} = (\alpha_P)(L_P)(\Delta t) \tag{17}$$

The second force influencing expansion is due to the axial board force (P_P) exerted on the board due to its thermal expansion (X_{P2}). This force is the product of the axial board force (P_P) times the length of the circuit board under the component package (L_P) divided by the product of the circuit board area (A_P) times the modulus of elasticity for the circuit board (E_P).

$$X_{P2} = \frac{(P_P)(L_P)}{(A_P)(E_P)} \tag{18}$$

The total circuit board displacement is:

$$X_P = X_{P1} - X_{P2} = (\alpha_P)(L_P)(\Delta t) - \frac{(P_P)(L_P)}{(A_P)(E_P)} \tag{19}$$

$$A_P = (L)(h_2)(1.25 \text{ effective width factor})$$

h_2 is the PCB thickness

Inserting the three displacement forces into equation 11, we get the equilibrium equation for the forces due to thermal expansion.

$$\alpha_C L_C \Delta t + \frac{P_C L_C}{A_C E_C} + \frac{P_S h_S}{A_S G_S} = \alpha_P L_P \Delta t - \frac{P_P L_P}{A_P E_P} \tag{20}$$

L_C = Distance from QFN centroid to all the solder pads on half the component package

$L_P = L_9$

L_9 = length from the centroid of the component to the center of the solder pads on adjacent side

α_c = CTE of QFN

α_p = CTE of PCB

Δt = mean temperature change = $(t_{max} - t_{min})/2$

E_c = QFN modulus of elasticity

E_p = PCB modulus of elasticity

h_s = solder joint height

A_s = Shear area of half the number of solder - 1

A_p = effective board area $\times$ (1.25 effective width factor)

A_c = effective component area

G_S = solder shear modulus

Pad #	Length (in)
L1	0.01965
L2	0.0393
L3	0.05895
L4	0.0786
L5	0.09825
L6	0.1179
L7	0.13755
L8	0.1572
L9	0.187
L	0.3937

Table 5 Component pad distances to the neutral point

Pad #	Distance (in)	Number of Pads	Total
L1	0.01965	2	0.0393
L2	0.0393	2	0.0786
L3	0.05895	2	0.1179
L4	0.0786	2	0.1572
L5	0.09825	2	0.1965
L6	0.1179	2	0.2358
L7	0.13755	2	0.2751
L8	0.1572	2	0.3144
L9	0.187	17	3.179
		33	4.5938
		Lc	0.139206

Table 6 Solder pads on half of the QFN carrier

Steinberg Model for thermal cycling from -25°C to +70°C:

$\alpha_c = 7\ PPM$

$\alpha_p = 15\ PPM$

$\Delta t = (70 - (-25))/2 = 47.5C$

$E_c = 4.21 \times 10^6\ PSI$

$E_p = 2.00 \times 10^6\ PSI$

$h_s = 0.0025\ \text{in}$

$A_s = 6.39 \times 10^{-3} in^2$

$A_p = 6.15 \times 10^{-2} in^2$

$A_c = 5.89 \times 10^{-3} in^2$

$G_S = 1.10 \times 10^6\ PSI$

$$\alpha_c L_C \Delta t = \left(7.0\times10^{-6}\right)\left(0.1392\right)\left(47.5\right) = 4.629\times10^{-5}$$

$$\frac{P_C L_C}{A_c E_c} = \frac{P_C\left(0.1392\right)}{\left(5.89\times10^{-3}\right)\left(4.21\times10^{6}\right)} = 5.621\times10^{-6} P_C$$

$$\frac{P_s h_s}{A_s G_S} = \frac{P_s\left(0.0025\right)}{\left(6.39\times10^{-3}\right)\left(1.10\times10^{6}\right)} = 3.556\times10^{-7} P_s$$

$$\alpha_p L_P \Delta t = \left(15\times10^{-6}\right)\left(0.1392\right)\left(47.5\right) = 9.918\times10^{-5}$$

$$\frac{P_P L_P}{A_p E_p} = \frac{P_P\left(0.1392\right)}{\left(6.15\times10^{-2}\right)\left(2.00\times10^{6}\right)} = 1.131\times10^{-6} P_P$$

$$\sum P = 0, \quad P_C = P_S = P_P \tag{21}$$

$$7.108\times10^{-6} P_S = 5.290\times10^{-5}$$

$$P_S = 7.442 \text{ lb}$$

P_S is the average force on the 33 solder joints for the half-slice model.

$$\text{Average Stress}\left(\text{S}_\text{s}\right) = \frac{P_S}{A_s} = \frac{7.442}{6.39\times10^{-3}} = 1164.31 \text{ lb/in}^2 \tag{22}$$

The maximum solder-joint stress will occur at the solder-pad location that is the furthest along the diagonal of the package. The average solder stress per solder-pad can be scaled to account for the maximum sheer stress. There are two scaling factors involved. The first factor scales the centroid to the diagonal dimension by multiplying the location of the centroid by the square root of two. In essence, it rotates the reference point 45 degrees. The second scale factor is the ratio of the distance from the solder-pad at the edge of the QFN to the corner solder pads (L_9/L_C). The resultant maximum shear stress becomes:

$$\text{Maximum Stress} = \text{Average Stress}\left(S_s\right) \times \left(\sqrt{2}\right) \times \left(\frac{L_9}{L_C}\right)$$

$$S_{Smax} = \left(1164.31\right)\left(\sqrt{2}\right)\left(\frac{0.187}{0.139}\right) = 2211.92 \text{ lb/in}^2$$

With the maximum cyclic stress identified, it can be applied to the eutectic fatigue properties of solder. The fatigue properties for eutectic Sn60/Pb40 solder have been studied for decades and are well understood. The mean failure data describing the stress vs. cycles to failure can be plotted on a Log-log curve and form a straight line (Figure 24). The equation describing the failure rate is:

$$\left(N_1\right)\left(S_1\right)^b = \left(N_2\right)\left(S_2\right)^b \tag{23}$$

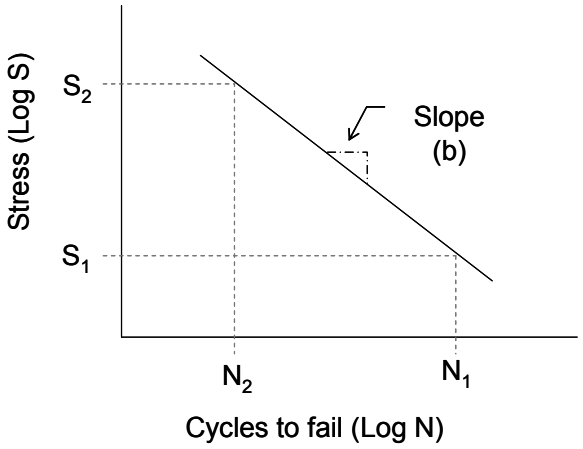


Figure 24 Typical log-log S-N fatigue Curve

Where[16]:

$N_1 = 80{,}000$

$N_2 = \text{Number of cycles to failure}$

$S_1 = 200\ \text{lb/in}^2$

$S_2 = 2248.9\ \text{lb/in}^2$

$b = 2.5$

$$N_2 = N_1\left(\frac{S_1}{S_2}\right)^b = 80{,}000\left(\frac{200}{2211.9}\right)^{2.5} = 197 \text{ cycles to failure}$$

The Steinberg model estimates the mean failure probability, $N_f(50\%)$. To describe the failure distribution model, we can use the same probability as the Engelmaier model for

leadless device. The β value equals four for a stiff leadless device; this is the same value as the Engelmaier model. The failure distribution probability is;

$$\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} \tag{24}$$

The resultant modified Steinberg model for a leadless device is:

$$N_2(x\%) = N_1\left(\frac{S_1}{S_2}\right)^b \left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} \tag{25}$$

For thermal Cycling test #1 (-25°C to 70°C) :

$$N\ (1\%) = N_1\left(\frac{S_1}{S_2}\right)^b \left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{2211.9}\right)^{2.5}\left[\frac{\ln(1-(0.01)(1))}{\ln(0.5)}\right]^{1/4} = 68 \text{ cycles}$$

$$N\ (50\%) = N_1\left(\frac{S_1}{S_2}\right)^b \left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{2211.9}\right)^{2.5}\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/4} = 197 \text{ cycles}$$

$$N\ (63.2\%) = N_1\left(\frac{S_1}{S_2}\right)^b \left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{2211.9}\right)^{2.5}\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/4} = 216 \text{ cycles}$$

Steinberg Model for thermal cycling from 0°C to +100°C:

$$\Delta t = \left(100 - (0)\right)\Big/_{2} = 50C$$

$$\alpha_c L_C \Delta t = \left(7\times10^{-6}\right)\left(0.1392\right)\left(50\right) = 4.872\times10^{-5}$$

$$\frac{P_C L_C}{A_c E_c} = \frac{P_C\left(0.1392\right)}{\left(5.89\times10^{-3}\right)\left(4.21\times10^{6}\right)} = 5.621\times10^{-6} P_C$$

$$\frac{P_s h_s}{A_s G_S} = \frac{P_s\left(0.0025\right)}{\left(6.39\times10^{-3}\right)\left(1.10\times10^{6}\right)} = 3.556\times10^{-7} P_s$$

$$\alpha_p L_P \Delta t = \left(15\times10^{-6}\right)\left(0.1392\right)\left(50\right) = 1.044\times10^{-4}$$

$$\frac{P_P L_P}{A_p E_p} = \frac{P_P\left(0.1392\right)}{\left(6.15\times10^{-2}\right)\left(2.00\times10^{6}\right)} = 1.131\times10^{-6} P_P$$

$$\sum P = 0, \quad P_C = P_S = P_P$$

$$7.108\times10^{-6} P_S = 5.568\times10^{-5}$$

$$P_S = 7.834 \text{ lb}$$

P_S is the average force on the 33 solder joints for the half-slice model.

$$\text{Average Stress}\left(\mathrm{S_s}\right) = \frac{P_S}{A_s} = \frac{7.834}{6.39 \times 10^{-3}} = 1225.59 \text{ lb/in}^2$$

$$\text{Maximum Stress} = \text{Average Stress}\left(\mathrm{S_s}\right) \times \left(\sqrt{2}\right) \times \left(\frac{L_9}{L_C}\right)$$

$$\mathrm{S_{Smax}} = \left(1225.59\right)\left(\sqrt{2}\right)\left(\frac{0.187}{0.139}\right) = 2328.33 \text{ lb/in}^2$$

$N_1 = 80{,}000$

$N_2 = \text{Number of cycles to failure}$

$S_1 = 200 \text{ lb/in}^2$

$S_2 = 2328.33 \text{ lb/in}^2$

$b = 2.5$

$$N_2 = N_1\left(\frac{S_1}{S_2}\right)^b = 80{,}000\left(\frac{200}{2328.33}\right)^{2.5} = 173 \text{ cycles to failure}$$

For thermal Cycling test #1 (0^{o}C to 100^{o}C) :

$$N\ (1\%) = N_1\left(\frac{S_1}{S_2}\right)^b\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{2328.3}\right)^{2.5}\left[\frac{\ln(1-(0.01)(1))}{\ln(0.5)}\right]^{1/4} = 60 \text{ cycles}$$

$$N\ (50\%) = N_1\left(\frac{S_1}{S_2}\right)^b\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{2328.3}\right)^{2.5}\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/4} = 173 \text{ cycles}$$

$$N\ (63.2\%) = N_1\left(\frac{S_1}{S_2}\right)^b\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{2328.3}\right)^{2.5}\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/4} = 190 \text{ cycles}$$

Steinberg Model for thermal cycling from 0°C to +70°C:

$$\Delta t = (70 - (0))/2 = 35C$$

$$\alpha_c L_C \Delta t = (7\times10^{-6})(0.1392)(50) = 3.411\times10^{-5}$$

$$\frac{P_C L_C}{A_c E_c} = \frac{P_C(0.1392)}{(5.89\times10^{-3})(4.21\times10^{6})} = 5.621\times10^{-6} P_C$$

$$\frac{P_s h_s}{A_s G_S} = \frac{P_s(0.0025)}{(6.39\times10^{-3})(1.10\times10^{6})} = 3.556\times10^{-7} P_s$$

$$\alpha_p L_P \Delta t = (15\times10^{-6})(0.1392)(50) = 7.308\times10^{-5}$$

$$\frac{P_P L_P}{A_p E_p} = \frac{P_P(0.1392)}{(6.15\times10^{-2})(2.00\times10^{6})} = 1.131\times10^{-6} P_P$$

$$\sum P = 0, \quad P_C = P_S = P_P$$

$$7.108\times10^{-6} P_S = 3.898\times10^{-5}$$

$$P_S = 5.484 \text{ lb}$$

P_S is the average force on the 33 solder joints for the half-slice model.

$$\text{Average Stress } (S_s) = \frac{P_S}{A_s} = \frac{5.484}{6.39\times10^{-3}} = 857.92 \text{ lb/in}^2$$

$$\text{Maximum Stress} = \text{Average Stress}\left(S_s\right) \times \left(\sqrt{2}\right) \times \left(\frac{L_9}{L_C}\right)$$

$$S_{Smax} = (857.92)\left(\sqrt{2}\right)\left(\frac{0.187}{0.139}\right) = 1629.83 \text{ lb/in}^2$$

$N_1 = 80{,}000$

$N_2 = \text{Number of cycles to failure}$

$S_1 = 200 \text{ lb/in}^2$

$S_2 = 2328.33 \text{ lb/in}^2$

$b = 2.5$

$$N_2 = N_1\left(\frac{S_1}{S_2}\right)^b = 80{,}000\left(\frac{200}{1629.83}\right)^{2.5} = 422 \text{ cycles to failure}$$

For thermal Cycling test #1 (0^{o}C to 70^{o}C) :

$$N\ (1\%) = N_1\left(\frac{S_1}{S_2}\right)^b\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{1629.83}\right)^{2.5}\left[\frac{\ln(1-(0.01)(1))}{\ln(0.5)}\right]^{1/4} = 146 \text{ cycles}$$

$$N\ (50\%) = N_1\left(\frac{S_1}{S_2}\right)^b\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{1629.83}\right)^{2.5}\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/4} = 422 \text{ cycles}$$

$$N\ (63.2\%) = N_1\left(\frac{S_1}{S_2}\right)^b\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/\beta} = 80{,}000\left(\frac{200}{1629.83}\right)^{2.5}\left[\frac{\ln(1-(0.01)(x))}{\ln(0.5)}\right]^{1/4} = 462 \text{ cycles}$$

Test #	Thermal Cycling Range	N_f(1%)	N_f(50%)	N_f(63.2%)
1	0 ^{o}C to 100 ^{o}C	60	173	190
2	-25 ^{o}C to 70 ^{o}C	68	197	216
3	0 ^{o}C to 70 ^{o}C	146	422	462

Table 7 Mean cycles to failure for Steinberg model

3.4.3 Reliability Model #3: Accelerated Life Analysis Based on Industry Data

The third approach combines published Amkor reliability data for a QFN package paddle down[17] with published Weibull failure distribution plots[18]. The Amkor data provided scaling information for various use applications and use conditions, i.e. different mold compound, lead structure and paddle not soldered to circuit board. This approach makes

the assumption that a QFN with an unsoldered paddle to the circuit board provides a good approximation for a QFN top-side paddle. This is similar from a mechanical attachment perspective to moving the paddle from bottom-side to top because the mechanical solder connection from the paddle no longer exists. The center paddle accounts for 88% of the soldered surface area when it is mechanically attached. Moving the paddle to the top-side should have a significant impact on solder-joint life due to thermal cycling.

The Amkor data provided was used to estimate the mean time to failure for the QFN experiment based on the following model factors that can be scaled:

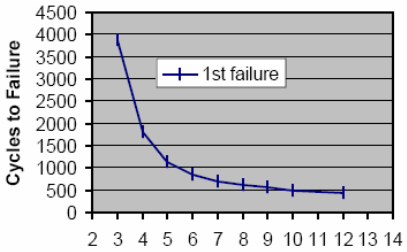
Epoxy mold compound (from Sumitomo G700 to G770)
Circuit board thickness (from .062" to .094")
Lead type (from full to half etched)

Amkor's data provided acceleration scale multipliers for each of the above factors. Missing from the Amkor model is a scale factor for a 0.125" thick circuit board and an estimate of the failure distribution model.

Amkor's baseline time to failure data is shown in Figure 25. For a QFN paddle down with a body style "10" (highlighted in yellow) the mean life and time to first failure are defined. The Amkor data is generated from accelerated life testing. The body style 10 is for a 10mm square QFN package. The package style is the same as the QFN paddle up

which is being evaluated. The main differences between the two packages are mold compound used (G700 vs. G770), fewer leads (68 vs. 72 leads) and smaller die size (7.0 mm vs. 8.0 mm). The time to 1st failure is 498 cycles and the mean life is 830 cycles which is the baseline data that will be scaled for our application and use conditions.

Body	CB	EMC	Leadcount	Die Pad	Die Size	mean life	1st failure
3	Full	G700	16	1.1	1	6456	3874
4	Full	G700	24	2.1	2	3033	1820
5	Full	G700	32	3.1	3	1900	1140
6	Full	G700	40	4.1	4	1432	859
7	Full	G700	48	5.1	5	1185	711
8	Full	G700	48	6.1	6	1039	623
9	Full	G700	48	7.1	7	940	564
10	Full	G700	72	8.1	8	830	498
12	Full	G700	88	10.1	10	722	433



♦ 1st Failure Typically at 60% of Mean Life

Figure 25 Baseline data from Amkor

Table 8 shows the scale factors for mold compound, lead type and paddle not soldered. To scale for a lower CTE mold compound (G770) the time to failure is multiplied by 0.4. The half etched lead reduces solder-joint life by an additional 25% and not soldering the bottom-side paddle further reduces solder-joint reliability by 40%. Taking these three factors into account, the acceleration factor due to differences in the package and how it is mounted to the circuit board is:

Mold compound: $AF_1 = 0.4$

Lead type: $AF_2 = 0.75$

Exposed pad not soldered: $AF_3 = 0.6$

The total package multiplier is = $(AF_1)(AF_2)(AF_3)$ = (0.4) (0.75)(0.6) = 0.18

– Package Multipliers

Variable	Reference	Change	Multiplier
Mold Compound	G700	HF13/G770	0.4
Lead Type	Full	Half Etch Lead	0.75
Lead Type	Full	Plated End Lead with Fillet	2.2
Bumped	No	Sn/Pb Bumped	1.4
Fillet	No	Half solder Fillet	2.4
Fillet	No	Full Solder Fillet	3.6
Exposed Pad	Soldered	Not Soldered	0.6

Table 8 Amkor scale factor for package differences

The Amkor scale factor for circuit board thickness was limited to board thicknesses ranging from 0.8mm to 2.4mm, with 1.6mm being the reference thickness (Table 9). However, the circuit board thickness that the QFN is soldered to is 3.17mm. Board thickness can play a significant role in solder-joint life. Based on the scale factors in table 5, going from a 2.4mm to a 0.8mm thick board improves the solder-joint life by a factor of 5.8. As the board thickness increases, the board becomes stiffer. Stiff boards are less compliant. If the board has compliance, the stress generated at the solder-joint due to a change in temperature can be shared by the circuit board. When the board becomes stiff, the stress is entirely absorbed by the solder connection. To correct for board thickness, test results from a solder reliability life test for a leadless ceramic resistor network (RNET) was used. An RNET is a leadless device with same lead terminations as a QFN.

The RNET package CTE is slightly less than the QFN CTE. Based on the RNET test, the acceleration factor for board with 3.17mm thickness is $AF_4 = 0.5$. Using the scale factor for board thickness, an estimated mean time and time to first failure can be calculated and shown in Figure 26.

Variable	Reference	Change	Multiplier
Board Thichness	1.6mm	0.8mm	3.75
Board Thichness	1.6mm	1.2mm	1.75
Board Thichness	1.6mm	2.4mm	0.65

Table 9 Amkor scale factor for board thickness

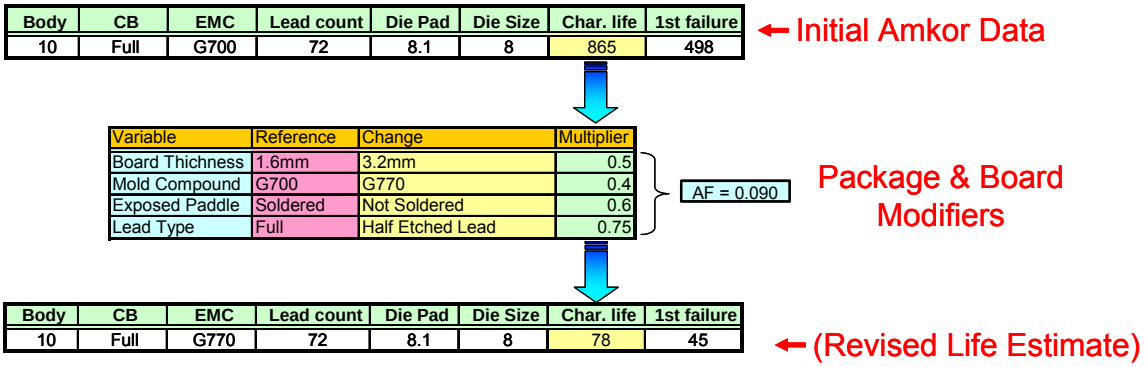


Figure 26 Amkor reliability data scaled for a QFN paddle up configuration

$$\therefore \eta = 78$$

$$R(t) = e^{-\left(\frac{t}{8}\right)^{8.5}}$$

Scaling for board thickness, mold compound, exposed paddle and lead type; the time to first failure is 45 cycles and the characteristic time to failure is 78 cycles. This is based on a thermal cycling profile from -40°C to +125°C. To scale for a different thermal cycling condition, a model for the acceleration rate is required. The inverse power law model provides the best fit for thermal cycling. The inverse power law model is:

$$\eta = \frac{A}{(\Delta T)^n} \tag{26}$$

Where :

η = The characteristic number of cycles to failure

ΔT = The Thermal Cycle temperature swing

n = Inverse power law exponent

A = Characteristice life constant

To use the IPL model, values for A and n need to be determined. To define values for A and n, Amkor reliability data for a QFN paddle down package with multiplication scaling factors for thermal cycling ranges is used (Table 10). The Amkor data is based on the reference thermal cycling profile of -40°C to +125°C, which is the baseline data. Using

the scaling factor for the three temperature cycling tests, the time to first failure and the mean time to failure is calculated. As an example, for test #1 which thermal cycles between 0°C and 100°C, the scale factor is 2. The time to first failure is 90 cycles (45 cycle's baseline times the scale factor 2 = 90) and the characteristic life time is 156 cycles (78 x 2 = 156).

Test #	Variable	Reference	Change	Multiplier
1	Temp. Cylce	-40<>125c	-55<>125C, 2 cycles/hr	0.85
2	Temp. Cylce	-40<>125c	0<>100C, 2 cycles/hr	2.00
3	Temp. Cylce	-40<>125c	-40<>100C, 2 cycles/hr	1.35

Table 10 Amkor scale factor for thermal cycling protocols

Using the Amkor data for the three test protocols above, the mean time and time to first failure is estimated. The failure distribution model has not been defined. The model could be Weibull, normal or lognormal. To select the right distribution model, two published reliability papers for a QFN paddle down were considered[4,5]. Based on these papers, the Weibull distribution provides a good fit since the failure is due to wearout (A lognormal distribution also fits). To use a Weibull model, the shape factor "β" is needed. The failure shape for the Weibull model is estimated based on published Weibull reliability plots for a QFN paddle down. This is a reasonable estimate because the failure mechanism is the same for the QFN. The first reference is for a QFN paddle not soldered to the board, had a Weibull failure distribution with a β=9.55. The second reference had a Weibull failure model with a β=9.42 for a soldered paddle and a board thickness of 1.6mm. Based on these two data points, a Weibull distribution with a β=9.5 was assumed.

The resultant mean life and 1% failure for the three different stress tests is shown in Table 11.

Variable	Reference	Change	Multiplier	1% Failure	Mean life (μ)	Char. life (η)	Beta (β)
Temp. Cylce	-40<>125c	-55<>125C, 2 cycles/hr	0.85	38	64	66	8.5
Temp. Cylce	-40<>125c	-40<>100C, 2 cycles/hr	1.35	61	101	105	8.5
Temp. Cylce	-40<>125c	0<>100C, 2 cycles/hr	2.00	90	150	156	8.5

Table 11 Amkor Weibull model for different thermal cycling protocols

The characteristic life can be calculated from mean life if beta is known. The equation for mean life based on the characteristic life and beta is: Accelerated life model for NiPdAu plated lead and new EME-7730LF mold compound:

Life Stress Relation: Inverse Power Law

$$L(V) = \frac{1}{K \cdot V^n}$$

K =	7.1396E-6
n =	1.4705

Life Distribution:Weibull

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}} \quad where \quad \eta = L(V_i)$$

β =	8.66716457016524
η =	Function of Life-Stress Relation

Use Stress Level Summary

Temperature
300

Plot of Cox-Snell Residuals

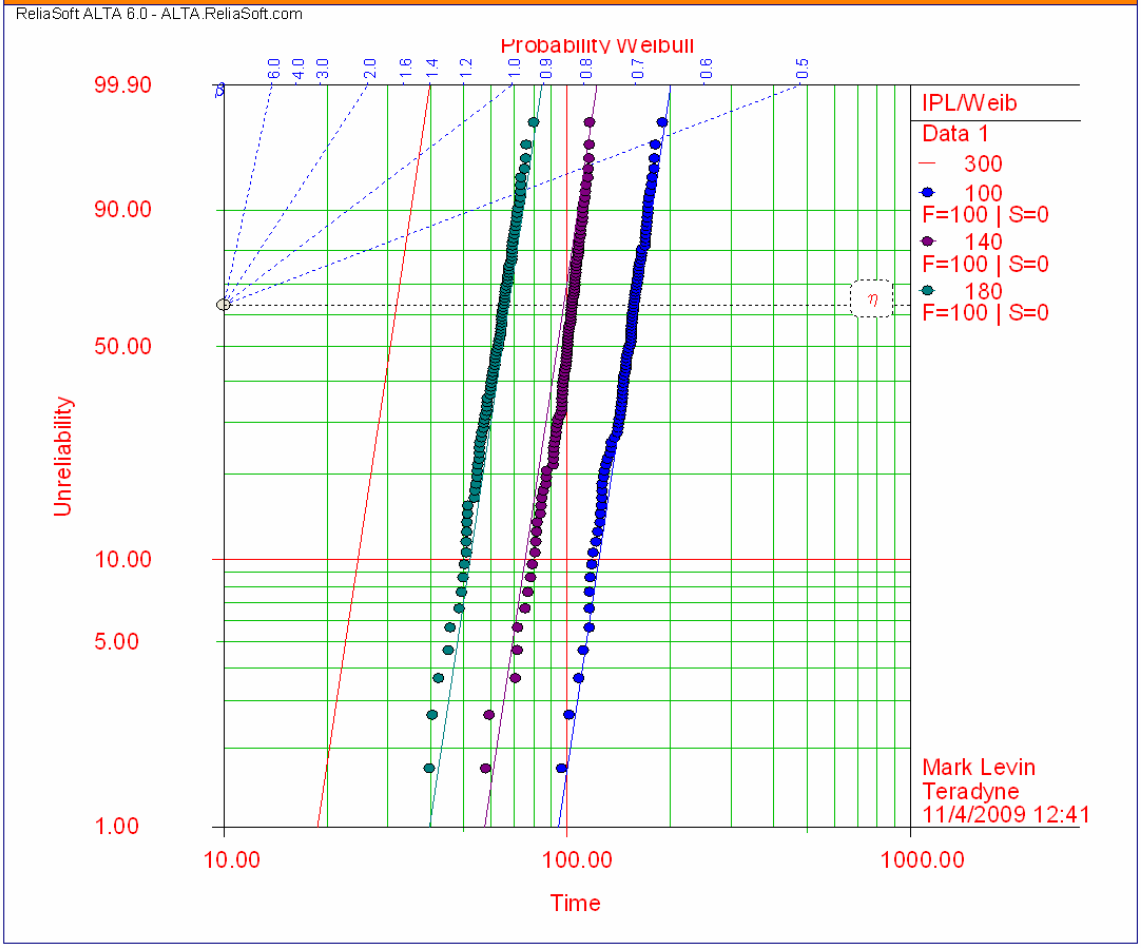


Figure 27 Reliasoft Alta 6.0 parameters IPL-Weibull model

$$\mu = (\eta)\Gamma\left(1+\frac{1}{\beta}\right) \tag{27}$$

$$\eta = \frac{\mu}{\Gamma\left(1+\frac{1}{\beta}\right)} = \frac{\mu}{\Gamma\left(1+\frac{1}{8.5}\right)} = \frac{\mu}{\Gamma(1.1177)}\frac{\mu}{0.9445} = 1.059\mu$$

For a Weibull model with a high β value, there is little difference between the mean life and the characteristic life. Using table 15 and scaling the mean life by 1.059, the Weibull parameters η and β for different thermal stresses is developed (Table 12). Using a Monte Carlo simulation in Reliasoft's Weibull++ 6.0 software, Weibull plots for each of the three thermal cycling tests are created. The three Weibull plots can be used to estimate the IPL parameters A and n. This was accomplished using Reliasoft's Alta 6.0 software. The Weibull plots and accelerated life model is shown in Figure 28. The IPL values for the QFN model are:

$$K = 8.7943 \times 10^{-6}$$

$$n = 1.4087$$

$$A = \frac{1}{K} = \frac{1}{8.7943 \times 10^{-6}} = 114.295 \times 10^{3}$$

Variable	Change	1% Failure	Mean life (μ)	Char. life (η)	Beta (β)
Temp. Cylce	-55< >125C, 2 cycles/hr	31	64	71	9.5
Temp. Cylce	0< >100C, 2 cycles/hr	74	150	166	9.5
Temp. Cylce	-40< >100C, 2 cycles/hr	50	101	112	9.5

Table 12 Simulated Model for Various Thermal Cycling

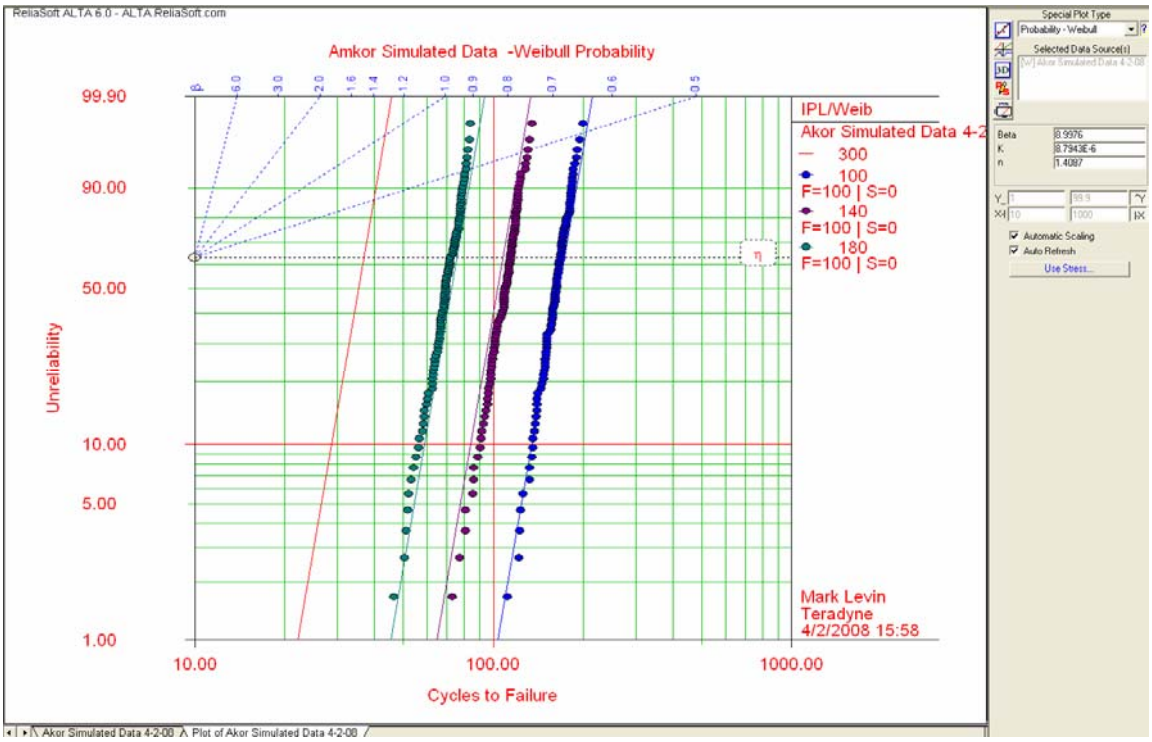


Figure 28 Simulated Weibull data for various thermal cycling

With the values of A and n determined, the reliability model for thermal cycling test #1 and #2 can be evaluated. The acceleration model for the characteristic time to failure is:

$$\eta = \frac{A}{(\Delta T)^n} = \frac{140.39 \times 10^3}{(\Delta T)^{1.4087}}$$

$$\mathrm{R}(t,V) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} = e^{-\left(\frac{t}{\frac{A}{(V)^n}}\right)^{\beta}} \tag{28}$$

Where V = the temperature swing ΔT

The failure rate function is:

$$f(t,V) = \beta A(V)^n \left(A(V)^n t\right)^{\beta-1} e^{-\left(\frac{t}{\frac{A}{(V)^n}}\right)} \tag{29}$$

Using the Weibull model with IPL the time to failure values for thermal cycling stresses #1 and #2 are listed in Table 13.

Variable	Temperature Cycling	1% Failure	Mean life (μ)	Char. life (η)
Temp. Cylce	0< >70C, 1.5 cycles/hr	172	267	285
Temp. Cylce	-25< >70C, 1.5 cycles/hr	111	179	186

Table 13 Simulation results for accelerated test #1 and test #2

3.4.4 Reliability Model #4: Accelerated Life Analysis Using SRS 1.1 Software:

The last modeling prediction method uses SRS (Solder Reliability Solutions) 1.1 software by Jean-Paul Clech to model the time to failure[19]. The software uses a model for a Leadless Ceramic Chip Carrier (LCCC) with the material characteristics changed for a QFN. The SRS 1.1 software is based on a "Comprehensive Surface-mount Reliability (CSMR) methodology[20,21]. The SRS software model for a LCCC uses fatigue life predictions based on strain energy that was validated using accelerated test data to develop a better representative model. The model can account for bending and stretching of the PCB and QFN. The software is limited to package styles that have test data to validate and fine tune the model, so its use is limited to package styles that have been well studied. The package styles that can be evaluated are: LCCC, plastic quad flat pack (QFP), thin small outline plastic package TSOP, ceramic leaded chip carriers (CLCC) and small outline transistors (SOTs).

The model is developed by selecting a component package type from the list of available packages, i.e. LCCC and then editing the package parameters to make it behave like the QFN package. The "Number of Susceptible I/O's" is the total number of pins that are likely to fail first. For a QFN package, the most likely to fail pins are at the corner since this is the greatest distance from the neutral point. For each corner there are two pins, one on each side of the corner, that are equally likely to fail. Therefore, if you include all four corners there are 8 susceptible I/Os. The remaining inputs are straight forward and come from the manufactures datasheet (Figure 29).

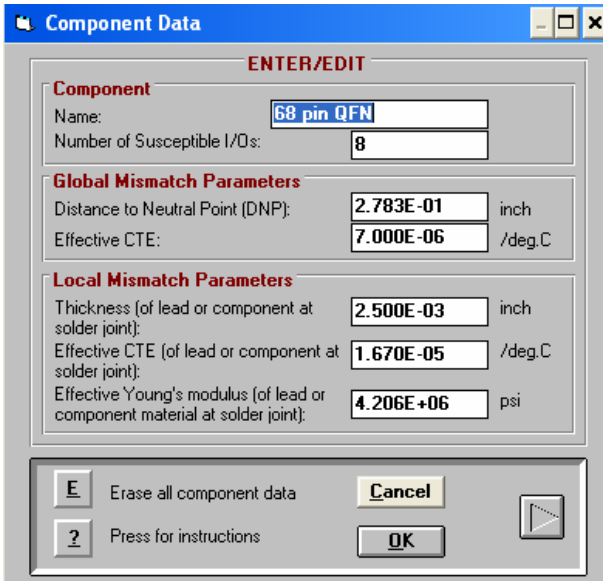


Figure 29 SRS1.1 Component model for QFN

The next required input for the model is the “substrate” parameters for the printed circuit board which are pulled from the manufacturer’s data sheet (Figure 30 and Figure 31). Next, the parallel spring constants for each element in the assembly need to be defined. The spring constants are: K1 (board stretching), K2 (component stretching) and K3 (board/component bending). Based on these three spring constants, the assembly stiffness is calculated. The stiffness results and assembly stiffness is calculated by the model based on the component and substrate inputs (Figure 32 and Figure 33). The final input required is the thermal conditions to be used in the analysis. The model allows for multiple fixed and variable stresses. For this analysis, only a cyclic stress is applied (Figure 35).

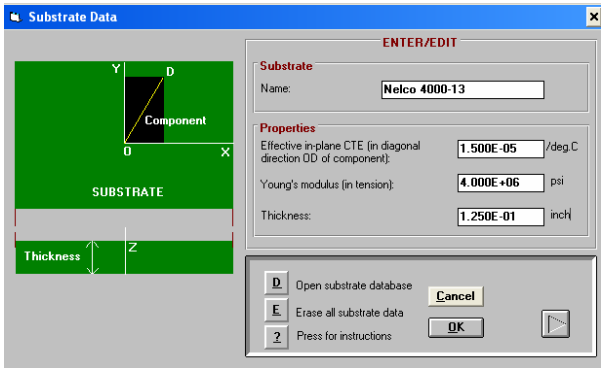


Figure 30 SRS1.1 Substrate model for QFN

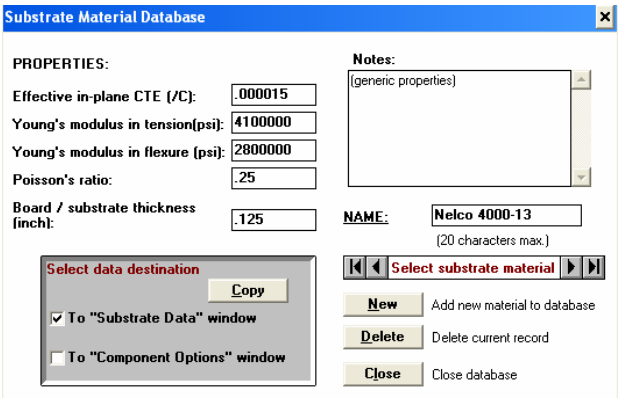


Figure 31 SRS1.1 Substrate model for QFN

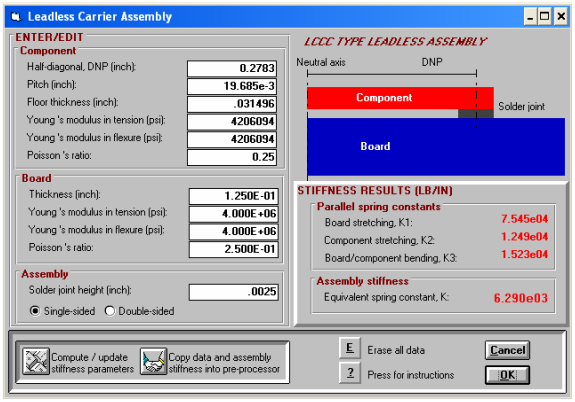


Figure 32 SRS1.1 parallel spring constants

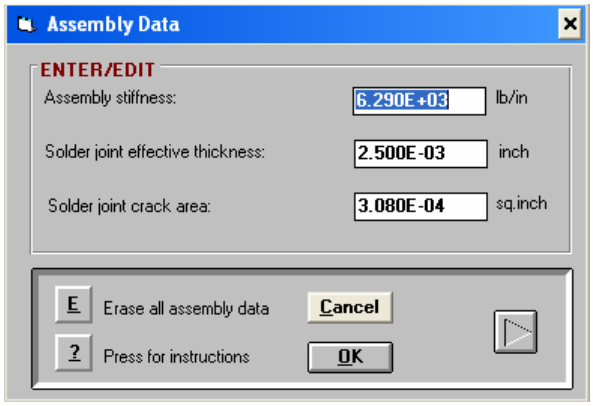


Figure 33 SRS1.1 Assembly stiffness

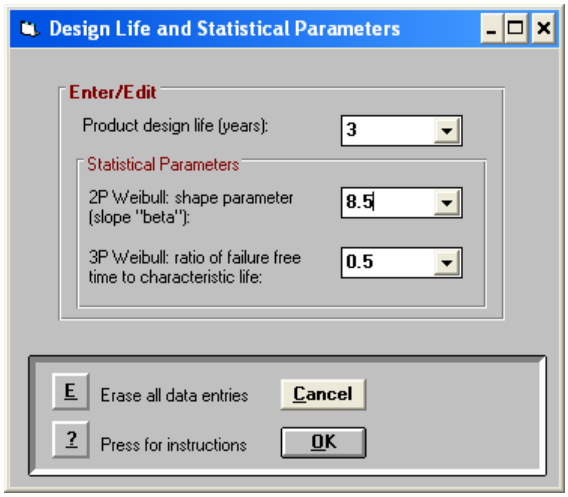


Figure 34 SRS1.1 Model Distribution Selection

After the model inputs have been entered, the software runs a validity check. If the data is valid, it will run the analysis. The output is a list of the inelastic strain energy for the global and local strains defined earlier. It also provides the inelastic cyclic creep strain and stress strain loop chart.

Parameters for the thermal cycling profile for test #1 are shown in Figure 35 below. The dwells were set at 20 minutes at each set point and the cycle type set to variable. The "daily frequency" input is ignored when the "Cycle Type" is set to variable.

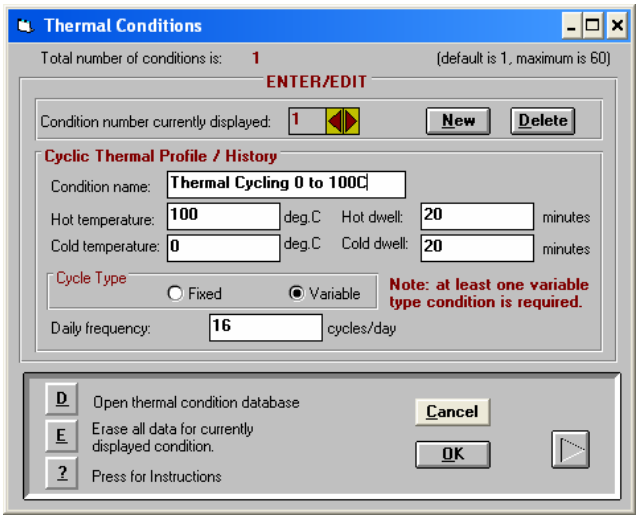


Figure 35 Thermal conditions for test #1

The resultant output from the model for thermal cycling test #1 0°C to 100°C

Inelastic strain energy

Global Strain Energy		Local Strain Energy		Total
PSI	%	PSI	%	PSI
164.2	99.40	.989	0.60	165.14

	Inelastic Strain (width of loop)	Creep Strains	
		Hot	Cold
Global strain	4.817E-02	3.845E-02	2.629E-02
Local strain	7.117E-04	2.823E-04	1.258E-04

Table 14 Output inelastic and cyclic strain for thermal cycling test #1

The modeling analysis for thermal stress test #1 is shown in Table 14 and Figure 36 through Figure 38).

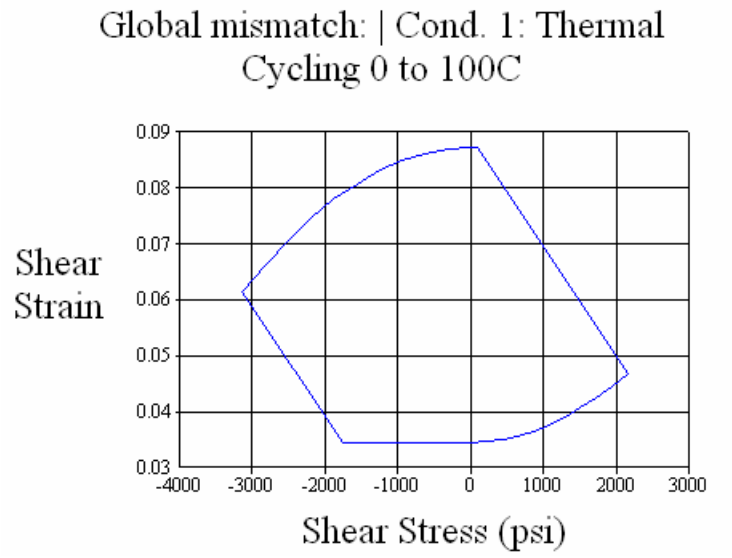


Figure 36 Test #1 global strain

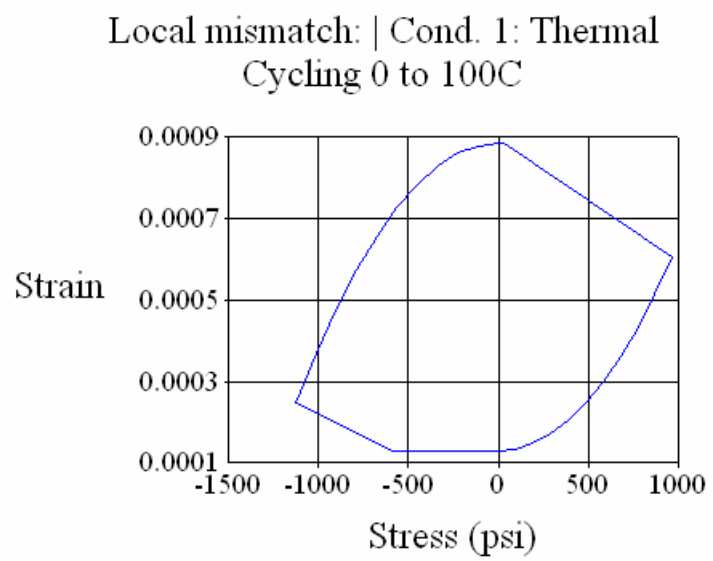
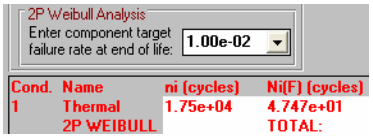
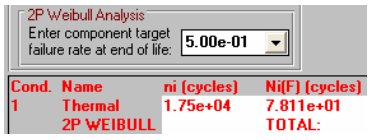
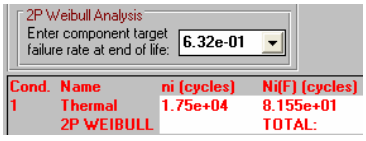


Figure 37 Test #1 local strain







1% failure = 47.5 cycles 50% failure = 78.1 cycles 63.2% failure = 81.6 cycles

Figure 38 Cycles to failure report for thermal cycling test #1, 2-parameter Weibull & β=8.5

The resultant output from the model for thermal cycling test #2 0°C to 70°C

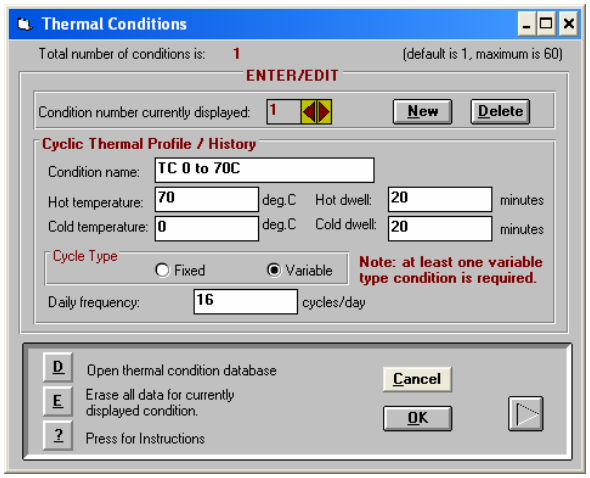


Figure 39 Thermal conditions for test #2

STRESS/STRAIN/ENERGY RESULTS

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Inelastic strain energy

Global Strain Energy		Local Strain Energy		Total
PSI	%	PSI	%	PSI
73.574	99.09	.677	0.91	74.25

Cyclic strain

	Inelastic Strain (width of loop)	Creep Strains Hot	Cold
Global strain	2.624E-02	2.376E-02	1.812E-02
Local strain	4.775E-04	2.476E-04	1.345E-04

Table 15 Output inelastic and cyclic strain for thermal cycling test #2

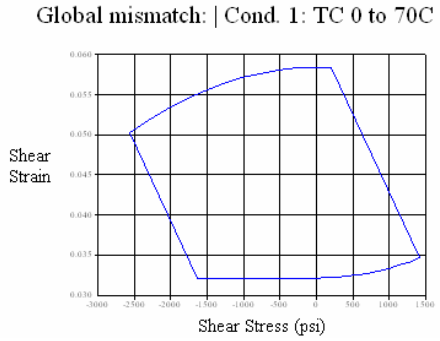


Figure 40 Test #2 Global strain

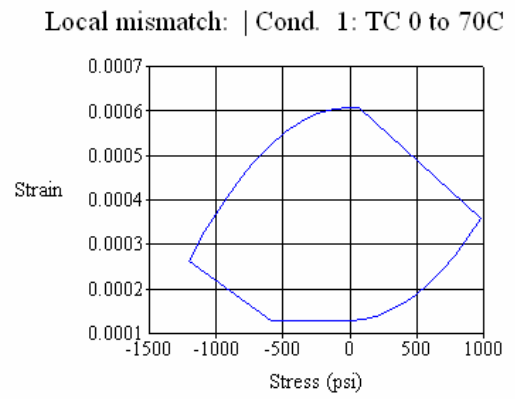
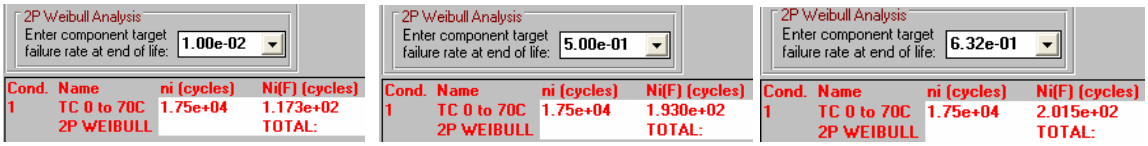


Figure 41 Test #2 Local strain



1%failure=117.3 cycles 50%

failure = 193.0 cycles 63.2% failure = 201. cycles

Figure 42 Cycles to failure "thermal cycling test #2" and 2-parameter Weibull with β=8.5

Comparison of experiment and modeling results (Delta T = 100 °C)	CDF (cycles to failure)		
	1%	50%	63.2%
Modeling Results			
Engelmaier model for LCCC	29	78	84
Steinberg	66	166	206
Amkor published Data	111	179	186
Clech SRS software model	56	87	93

Comparison of experiment and modeling results (Delta T = 70°C)	CDF (cycles to failure)		
	1%	50%	63.2%
Modeling Results			
Engelmaier model for LCCC	52	149	162
Steinberg	141	405	441
Apply industry published papers (Amkor Data)	172	267	285
SRS software model	117	193	202

Figure 43 Summary table for 1st order models to estimate failure probability

Chapter 4: QFN Accelerated Reliability Stress Tests

4.1 Introduction

Accelerated reliability testing was performed in two stages using two different methods to analyze second level solder-joint attachment reliability. The first test method consisted of an accelerated thermal cycling stress test on production instrument boards used in the ATE industry that is functionally good and operational. The circuit board is designed with diagnostic test software that loops continuously on the ASICs to monitor functionality. The diagnostic software records shifts in performance that can be used to identify degradation in device performance. The accelerated thermal cycling stress test is performed on an instrument board under bias power conditions and functionally operated. This solution offers the quickest reliability test results if a reliability qualification board was not designed to evaluate second level attachment reliability. A failure can be due to either a device degradation/failure or due to second level solder-joint attachment degradation. Care was taken to ensure that only failures related to a cracked or degraded solder-joint were used in the reliability analysis. Traditionally, this test is performed using daisy-chained dummy components and the change in resistance monitored to determine second level attachment reliability. A comparison of the two methods is presented at the conculsion to determine the acceptability of this approach.

There are advantages to using product material to qualify second level solder-joint attachment reliability for a package over a custom-made daisy-chained package. The daisy-chained component may not have all the physical features associated with the actual component package. For example, it may not include the silicon die or the die size is different than the actual product. The daisy chain dummy component may be physically the same but manufactured at a different facility designed to accommodate low volume, proto types or custom builds. Not all suppliers will offer daisy-chained components for evaluation, this forces using a third party with a daisy-chained package that closely resembles the one under evaluation. Finally, daisy chain tests require designing custom test boards and the physical properties of the test board may be different in construction than the actual production design.

One compelling reasons to use production material over a prototype test board to evaluate solder-joint attachment reliability is when a lead attachment issue surfaces in product development that was not planned for in risk mitigation. An accelerated thermal cycling life test using a daisy-chained test strategy can take four to six months to design and fab test boards, procure daisy-chained components and assemble test boards. The Thermal cycling test takes another 2 months to complete. Thus, it could be six to eight months before a lead attachment CTE issue is understood. Using production material to run the accelerated life test is more expensive, but it can quickly provide an answer regarding the useful life of the solder connection.

The second test method was to run an accelerated stress test used daisy-chained parts mounted onto a printed circuit board. The daisy-chained parts are very similar in construction to the QFN ASICs used in the previous test method. The daisy chain component has the same mold compound, silicon die size and lead frame as the actual product. The only differences are that the silicon die are rejects from production due to functionality reasons and the silicon die is not wire bonded to the lead frame and topside paddle. These differences are considered to be insignificant in their influence to second-level solder-joint reliability. The daisy chain components were manufactured at the same facility using the same manufacturing process as the ASIC QFN used in test method number one.

4.2 Accelerated Reliability Stress Test Plan

The thermal cycling test protocols for the two accelerated stress methods are different because there is an upper limit for the maximum temperature stress that can be applied to the functional product. Accelerated stress test method number one used functional QFN devices for thermal life cycling. Accelerated stress test method number two used daisy-chained QFN dummy parts. The objective for the two accelerated life tests is the same. Namely, to determine the failure rate, failure distribution and the acceleration factor thermal cycling has on the useful life of the solder joint. To determine the acceleration factor that thermal cycling has on solder-joint life requires two different temperature swings.

Accelerated life tests were performed at two different stress levels. Two test boards were used, one for each accelerated stress test. The accelerated stress test consisted of thermal cycling at two different temperature ranges. The testing consisted of 64 QFN (paddle up) Application Specific Integrated Circuit (ASIC's) soldered onto a printed circuit board that is powered on and continuously looping using a diagnostics program called checkers. The custom ASIC is an integrated, high performance, pin electronics driver, comparator and load (DCL) with Parametric Measurement Unit (PMU) and Level Setters chip for the Memory and SOC ATE market.

Test method number one, used production ASICs packaged in a QFN device with top-side paddle that was biased and operational during the thermal cycling test. Before beginning the accelerated life test, the temperature cycling profile needed to be defined based on the upper and lower operational limits for the product. The upper and lower operational limits were identified using HALT (Highly Accelerated Life test). In HALT, three production boards with ASICs in a QFN packages were temperature step stress to determine its hard and soft failure limits. The soft limit is the upper and lower temperature where the device stops functioning. Once the soft failure point is reached, the thermal stress is reduced to verify that device recovery. If the device does not recover, power is cycled without temperature stress to determine if the device is still functional. If the device does not recover, the failure is defined to be a hard failure. Hard failures require the device to be replaced before the product can be functional again.

After HALT testing, the upper operational limit was determined to be 80°C; this is the upper environmental temperature stress that can be applied to the QFN device and still continue to perform functionally. The lower operational temperature stress limit is -35°C. To account for the fact that the data is based on a small sample size of three instruments, a 10 degree C guard band was added to the upper and lower operational limits to ensure continuous operation during thermal cycling test without having soft failures occur. Although only three instruments were used for HALT, each instrument has 32 QFN's on it. Therefore, the sample size for the stress test is 96 devices. With adequate guard band for thermal cycling, the only failures expected during thermal cycling should be due to second level solder attachment of the QFN device, this component is the weakest link for CTE mismatch. Based on the operational limits identified during HALT, the first test thermal cycling protocol for thermal cycling test number 1 is between -25°C and +70°C. This will provide a 95°C temperature swing. The temperature ramp rate is set to the maximum the chamber can deliver which is 60 °C per minute. The dwell time at the upper and lower temperature set point is 20 minutes; this will ensure there is adequate time for temperature stabilization and creep. The board was thermal profiled to ensure that the dwell time once the board reaches the temperature set point is reached is 10 minutes. The QFNs have a liquid coldplate attached and that is liquid-cooled by design. The temperature in the liquid coldplate is controlled both by the thermal chamber through two large liquid-cooled radiators attached to the top of the temperature chamber. HFE is used to provide heating and cooling through the coldplate and heat exchanger which is

regulated by the same thermal chamber. The coolant that is running through the liquid coldplate is 3M HFE7500, which boils at 130C. The two large radiators are installed in the temperature chamber about 4 inches underneath the chamber outlet air vents to ensure the liquid HFE circulating through the cold plate is the same temperature as chamber ambient. A thermocouple is installed in the radiator outlet that monitors the HFE temperature going into the device under test. Thus, the air and liquid temperature track each other very closely and are controlled by same central source. A pump external to the thermal chamber circulates the HFE through a CDU that maintains constant pressure and has its temperature regulation bypassed. The thermal chamber uses liquid nitrogen to regulate the air temperature. The liquid nitrogen provides fast temperature transitions when going from hot to cold. The thermal chamber has large resistive coils that provide heating that are mounted in the top of the temperature chamber. The chamber is manufactured by Chart Industries.

The temperature protocol for the second test method is from 0 ^{o}C to 100 ^{o}C and for the second thermal cycling test it is from 0 ^{o}C to 70^{o}C. The two test yield time to failure distributions at two different stress levels. The test results are then used to estimate the acceleration factor, failure rate and distribution model for a solder crack. The failure rate distribution model and acceleration rate model can then be applied to a different set of thermal cycling conditions to estimate solder-joint life.

The second thermal cycling test went between the temperature range of 0°C and 70°C. The temperature ramp rate was 60 °C per minute and the dwell time at each temperature was 20 minutes. The two tests differed by 25°C and the test results are used to develop an acceleration model. The customer use environment cycles between 20°C in the off state and 38°C in a powered on "operational" state (Figure 44).

The maximum product upper and lower operating temperature limits were identified during HALT testing. The operating limit is defined as the point where the product continuously functions and passes system checkers. A buffer of 10°C was subtracted from the upper operational limit and added to the lower temperature limit to minimize the risk of other failure mechanisms occurring. Based on the results from HALT, the maximum temperature swing with a 10°C buffer is -25C to 70C. This was the limit that the system would run continuously without failure.

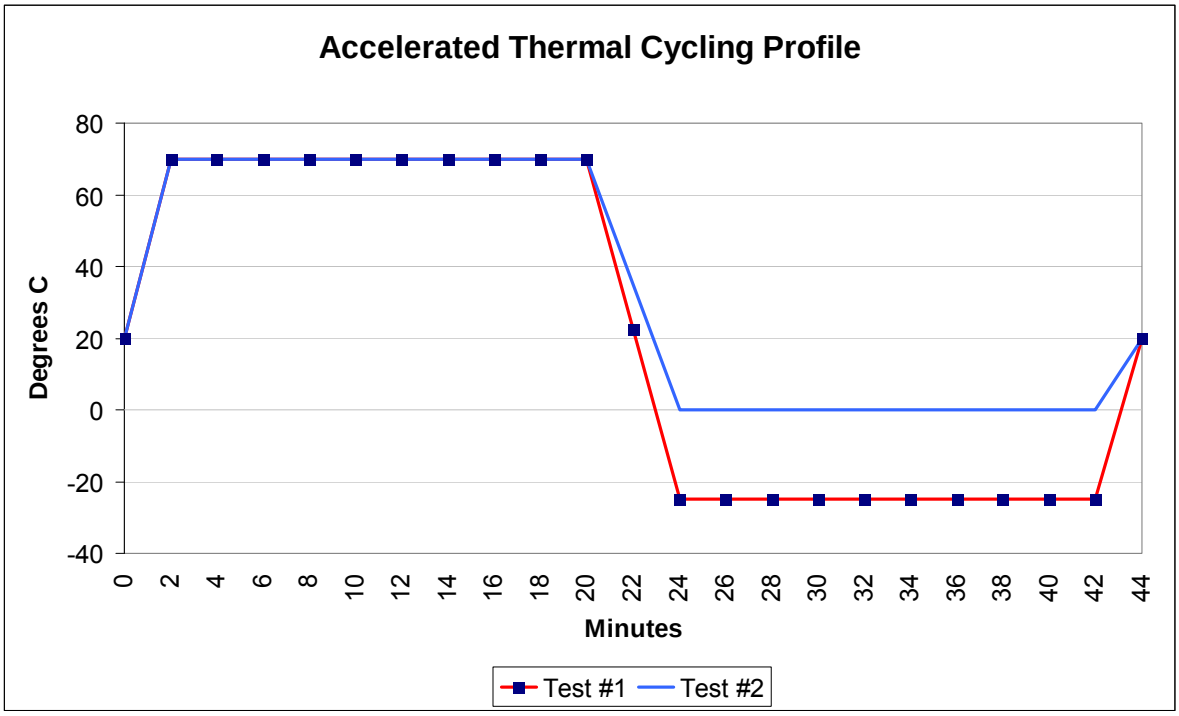


Figure 44 Thermal cycling profiles method #1; test #1 and test #2

A second round of accelerated reliability tests using manufacturer supplied daisy chain parts is described in the follow section. This next round of testing used the same thermal cycling profiles except it was performed in a thermal chamber that used a compressor instead of a HALT chamber that uses liquid nitrogen for cooling. What was unclear was the role oxidation plays in resistance measurements after crack initiation and crack propagation. Does the liquid nitrogen significantly slow the oxidation that takes place at the cracked interface?

The daisy-chained test board consists of five continuity loops per part (Figure 45). There is one continuity loop for each of the four corners of the package and a fifth continuity loop that ties all the middle pins together. This continuity scheme was chosen to allow for an evaluation of where the initial failure site occurs. Having a continuity loop for the middle pins provides an indication of how crack propagation continues towards the center of the package.

The continuity measurements were made using a four-wire resistance measurement set-up with the sense and force lines tied together at the QFN. Custom-built MUXs boards along with custom software were used to measure solder-joint continuity at each temperature set point. The continuity measurements were made 5 minutes after the product reaches the temperature set point.

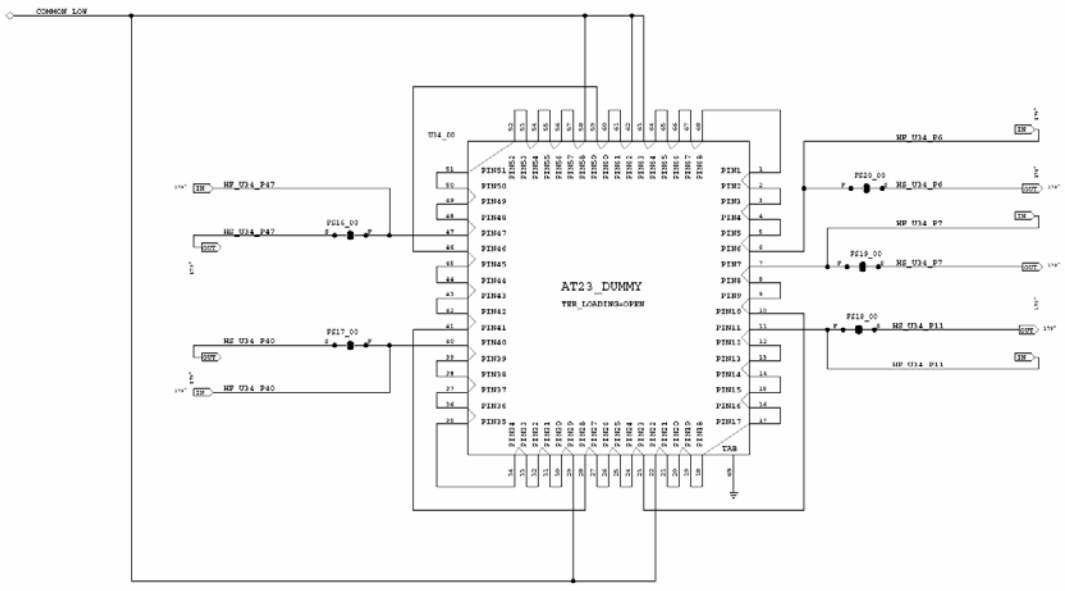


Figure 45 Daisy-chain test pattern

The two stress profiles for the second round of testing with daisy-chained parts are shown in Figure 46 below.

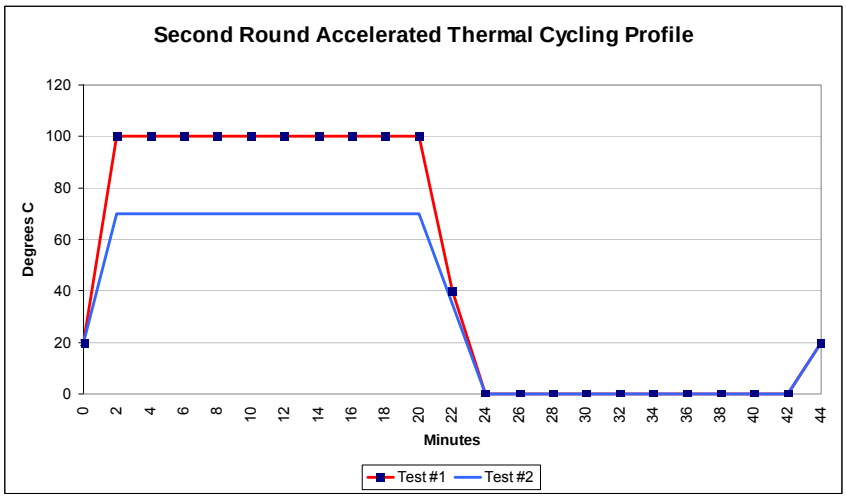


Figure 46 Thermal cycling profiles for method #2; test #1 and test #2

4.3 Reliability Stress Test Method 1

The first accelerated life test started on February 5, 2008 and ended on February 12th after 139 thermal cycles and 81% of the parts failing. The second accelerated life test started on February 14th, 2008 and ended on February 22, 2008 when 73% of the parts had failed.

The testing was performed on actual product and not with daisy-chained "non functional" components to determine the presence of soldered-joint failure. This approach was taken

over daisy-chained parts so testing could start right away. A second round of accelerated life tests will repeat these experiments using daisy-chained parts. The results from the daisy chain test will be compared with these results. The second advantage to using active components and looping diagnostic software over daisy-chained parts monitored by a four-wire Kelvin measurement is that there is no uncertainty about the failure mode. When doing a four-wire measurement, the definition of failure needs to be defined. Is it a 2X increase in resistance, exceeds minimum value (i.e. 300 mΩ) or an increase by a certain amount. The disadvantage to this test method is that a failure could be due to a cracked solder-joint or a faulty ASIC. Unless failure analysis in performed for every failure, there will be risk that other failure mechanisms influenced the test results. A visual inspection was performed on all failed QFN packages to verify that the failure was due to a cracked solder joint. However, visual inspection is not very effective because the device is leadless. Also, FA was performed only on a few devices to confirm failure mechanism.

4.3.1 Reliability Stress Test Method 1: Test #1 Results

Testing was performed on February 5th, 2008 and ended on February 12th, 2008. The test was terminated with 81% of the parts failing. The cycles to failure were entered into Reliasoft's Weibull++ version 6 and a 2-parameter Weibull distribution was assumed. The times to failure are shown in table 12.The table provides the thermal cycle number when it failed, a time and date stamp, number of failures occurring at cycle number. In

addition, the “Part Temp” column provides the internal die temperature at the time of failure and the color shading, red or green, denote the part of the thermal cycle the failure occurred. If the failure occurred at the high temperature set point, the shade is red. If the failure occurred during a cold temperature, the shading is green.

Part Temp	Thermal Cycle #	Date & Time	Failing Channels	Fail Cnt	Part Temp	Thermal Cycle #	Date & Time	Failing Channels	Fail Cnt
-19.1	76	2/8/08 1:26 AM	Channel 5	1	52.5	131	2/12/08 12:26 PM	Channel 32	1
62.9	85	2/8/08 8:18 AM	Channel 71	1	75.5	131	2/12/08 12:42 PM	Channel 50	1
40.8	90	2/8/08 11:49 AM	Channel 102	1	-19.3	132	2/12/08 12:53 PM	Channel 94	1
-13.6	91	2/8/08 12:30 PM	Channel 64	1	-18.4	132	2/12/08 12:54 PM	Channel 24	1
40.5	94	2/11/08 9:48 AM	Channel 30	1	-7.7	132	2/12/08 1:06 PM	Channel 26,28	2
12.0	98	2/11/08 12:18 PM	Channel 126	1	21.4	132	2/12/08 1:07 PM	Channel 72,74,76,118	4
69.5	102	2/11/08 3:42 PM	Channel 122	1	-3.4	133	2/12/08 1:29 PM	Channel 46,57	2
73.0	102	2/11/08 3:52 PM	Channel 112	1	16.6	133	2/12/08 1:50 PM	Channel 67	1
72.5	106	2/11/08 6:37 PM	channel 88	1	32.0	135	2/12/08 3:17 PM	Channel 101	1
15.8	108	2/11/08 7:51 PM	Channel 91	1	54.8	136	2/12/08 3:37 PM	Channel 14	1
53.8	111	2/11/08 9:38 PM	Channel 12	1	29.2	136	2/12/08 4:00 PM	Channel 44, 81	2
-5.6	112	2/11/08 10:23 PM	Channel 111	1	29.5	138	2/12/08 5:04 PM	Channel 40	1
-18.6	112	2/11/08 10:27 PM	Channel 68	1	-21.7	138	2/12/08 5:19 PM	Channel 114	1
-14.1	113	2/11/08 11:07 PM	Channel 48	1					
52.3	114	2/12/08 12:13 AM	Channel 96	1					
55.6	114	2/12/08 12:14 AM	Channel 108	1					
-19.6	115	2/12/08 12:35 AM	Channel 54	1					
66.3	116	2/12/08 1:44 AM	Channel 58	1					
-8.2	117	2/12/08 1:59 AM	Channel 104	1					
-20.3	117	2/12/08 2:08 AM	Channel 4	1					
66.5	120	2/12/08 4:06 AM	Channel 6	1					
-11.9	121	2/12/08 5:11 AM	Channel 92	1					
16.7	121	2/12/08 5:12 AM	Channel 18	1					
-17.1	125	2/12/08 7:48 AM	Channel 42	1					
56.5	125	2/12/08 8:08 AM	Channel 52	1					
65.6	125	2/12/08 8:12 AM	Channel 120,124	2					
-14.8	126	2/12/08 8:28 AM	Channel 36	1					
18.7	127	2/12/08 9:31 AM	Channel 116	1					
58.9	128	2/12/08 10:18 AM	Channel 38	1					
-19.9	130	2/12/08 11:30 AM	Channel 21	1					
-19.5	131	2/12/08 12:05 PM	Channel 0,2,	2					
								Total Failing Channels	52
								Total Channels	64
								Suspensions	12
								% Surviving	19%
								% failing	81%

Table 16 Cycles to failure for accelerated test #1

The cycle time to failure data was entered into Reliasoft’s Weibull++ 6.0. The Reliasoft distribution wizard evaluates the failure and suspension data to determine how well it fits different distribution models like Weibull, normal, lognormal . . . etc. Based on the results from the distribution wizard, the data are best fit by a 2-parameter Weibull plot (Figure 47). The decision to use a two parameter Weibull is consistent with earlier

assumptions and allows easy comparison between results. The two parameter Weibull model is shown in Figure 48. The key values for the Weibull model are the shape factor β=8.11, the characteristic life η=133.7 and the correlation coefficient ρ=0.992 which means the data fits well to the model. The failure rate data is summarized in Table 17.

Figure 47 Failure distribution model ranking

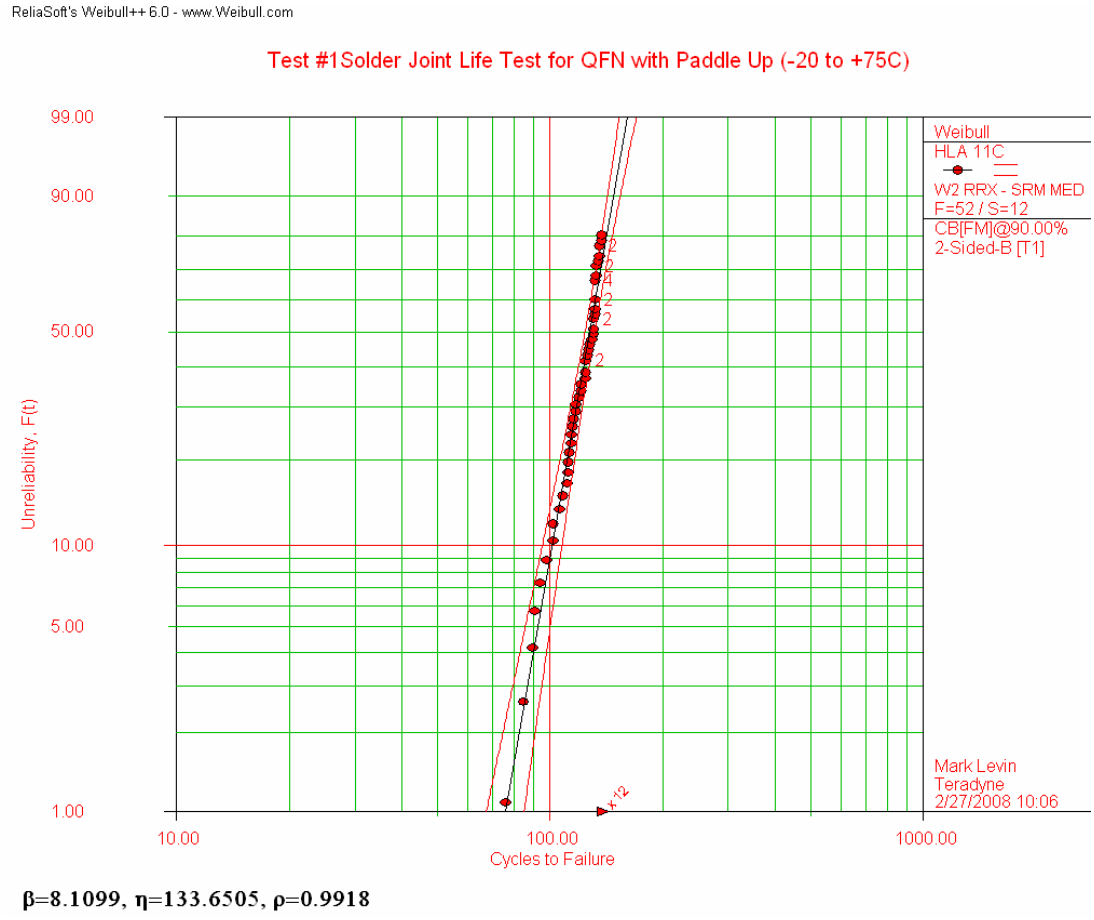


Figure 48 Weibull unreliability distribution for thermal cycling test #1

The resultant Weibull distribution is:

$$f(t)=\left(\frac{\beta}{\eta}\right)\left(\frac{T}{\eta}\right)^{\beta-1}e^{-\left(\frac{T}{\eta}\right)^{\beta}}=\left(\frac{8.1099}{133.7}\right)\left(\frac{T}{133.7}\right)^{8.1099-1}e^{-\left(\frac{T}{133.7}\right)^{8.1099}}$$

Where :

$$f(T)\geq 0,\ T\geq 0,\ \beta>0,\ \eta>0$$

The mean time to failure is:

$$\overline{T} = \eta \cdot \Gamma\left(\frac{1}{\beta} + 1\right) = 133.7 \cdot \Gamma\left(\frac{1}{8.1099} + 1\right) = 133.7 \cdot \Gamma(1.1233) = 133.7 \cdot (.9448) = 126.3$$

The standard deviation is:

$$\sigma_T = \eta\sqrt{\Gamma\left(\frac{2}{\beta}+1\right) - \Gamma\left(\frac{1}{\beta}+1\right)^2} = 133.7\sqrt{\Gamma\left(\frac{2}{8.1099}+1\right) - \Gamma\left(\frac{1}{8.1099}+1\right)^2} =$$

$$= 133.7\sqrt{\Gamma(1.24661) - \Gamma(1.12331)^2} = 133.7\sqrt{0.90711 - (0.94236)^2} = 18.462$$

$$\overline{T} = 126.3 \pm 18.462$$

The unreliability Function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{133.6}\right)^{8.11}}$$

$$\text{Unreliability} = F(T) = 1 - R(T) = 1 - e^{-\left(\frac{T}{\eta}\right)^{\beta}} = 1 - e^{-\left(\frac{T}{133.6}\right)^{8.11}}$$

Test #	Thermal Cycling Range	N_f(1%)	N_f(50%)	N_f(63.2%)	β
1	-25 °C to 70 °C	76	128	134	8.11

Table 17 Failure rate summary using developed Weibull: Method 1 test #1

4.3.2 Reliability Stress Test Method 1: Test #2 Results

Testing was performed on February 14th, 2008 and ended on February 21st, 2008. The test was terminated with 73% of the parts failing. The cycles to failure were entered into Reliasoft's Weibull++ version 6 and a 2-parameter Weibull distribution was assumed. Based on the results from the distribution wizard, the data was best fit by a 2-parameter Weibull plot (Figure 49). The times to failure are shown in Table 13 and the two parameter Weibull model is shown in Figure 50. The key values for the Weibull model are the shape factor β=10.22, the characteristic life η=225.56 and the correlation coefficient ρ=0.9918 which means the data fits well to the model.

Figure 49 Failure distribution model ranking

Part Temp	Thermal Cycle #	Date & Time	Failing Channels	Fail Cnt	Part Temp	Thermal Cycle #	Date & Time	Failing Channels	Fail Cnt
70.4	149	2/19/08 12:42 AM	Ch 126	1	9.2	218	2/21/08 12:50 AM	Ch 46	1
64.9	153	2/19/08 3:28 AM	Ch 124	1	-0.3	218	2/21/08 12:51 AM	Ch 16	1
57.4	162	2/19/08 9:45 AM	Ch 76	1	63.4	219	2/21/08 1:58 AM	Ch 66	1
5.5	174	2/19/08 5:48 PM	Ch 4	1	16.6	222	2/21/08 3:39 AM	Ch 71	1
66.6	175	2/19/08 7:02 PM	Ch 120	1	1.1	224	2/21/08 5:05 AM	Ch 18	1
44.7	181	2/19/08 11:05 PM	Ch 56	1	68.6	228	2/21/08 8:29 AM	Ch 110	1
0.5	187	2/20/08 2:58 AM	Ch 103	1	-1.7	230	2/21/08 9:20 AM	Ch 97	1
3.3	188	2/20/08 3:40 AM	Ch 54	1	-1.6	230	2/21/08 9:28 AM	Ch 101	1
6.7	189	2/20/08 4:22 AM	Ch 123	1	-1.6	231	2/21/08 10:02 AM	Ch 78	1
0.7	189	2/20/08 4:24 AM	Ch 113	1	54.5	231	2/21/08 10:23 AM	Ch 50	1
49.8	190	2/20/08 5:26 AM	Ch 82	1	51.7	238	2/21/08 2:59 PM	Ch 40	1
14.5	194	2/20/08 7:53 AM	Ch 85	1	65.1	238	2/21/08 3:30 PM	Ch 53	1
54.0	195	2/20/08 8:58 AM	Ch 86	1	64.0	239	2/21/08 3:41 PM	Ch 28	1
0.8	196	2/20/08 9:19 AM	Ch 108	1					
-1.3	197	2/20/08 10:05 AM	Ch 62	1					
50.9	199	2/20/08 11:47 AM	Ch 116	1					
-1.9	200	2/20/08 12:15 PM	Ch 81	1					
11.4	202	2/20/08 1:32 PM	Ch 44	1					
28.4	203	2/20/08 2:35 PM	Ch 11	1					
23.3	204	2/20/08 3:17 PM	Ch 119, Ch 115	2					
48.6	205	2/20/08 4:01 PM	Ch 99	1					
19.8	206	2/20/08 4:21 PM	Ch 33	1					
6.3	207	2/20/08 5:04 PM	Ch 48	1					
0.6	207	2/20/08 5:13 PM	Ch 35 **Ch 34**	1					
-1.2	207	2/20/08 5:19 PM	Ch 37	1					
59.5	208	2/20/08 6:10 PM	Ch 39	1					
33.5	210	2/20/08 7:10 PM	Ch 59	1					
-2.8	210	2/20/08 7:29 PM	Ch 2	1					
10.7	211	2/20/08 8:13 PM	Ch 61	1					
39.9	213	2/20/08 9:39 PM	Ch 69	1					
20.1	214	2/20/08 10:00 PM	Ch 15	1					
29.5	215	2/20/08 10:42 PM	Ch 104	1					
4.5	215	2/20/08 11:02 PM	Ch 93	1					
								Total Failing Channels	**47**
								Total Channels	64
								Suspensions	17
								% Surviving	27%
								% failing	73%
								Total Cycles	239

Table 18 Cycles to failure for accelerated test #2

The failure data was evaluated using Reliasoft's Weibull++ version 6.

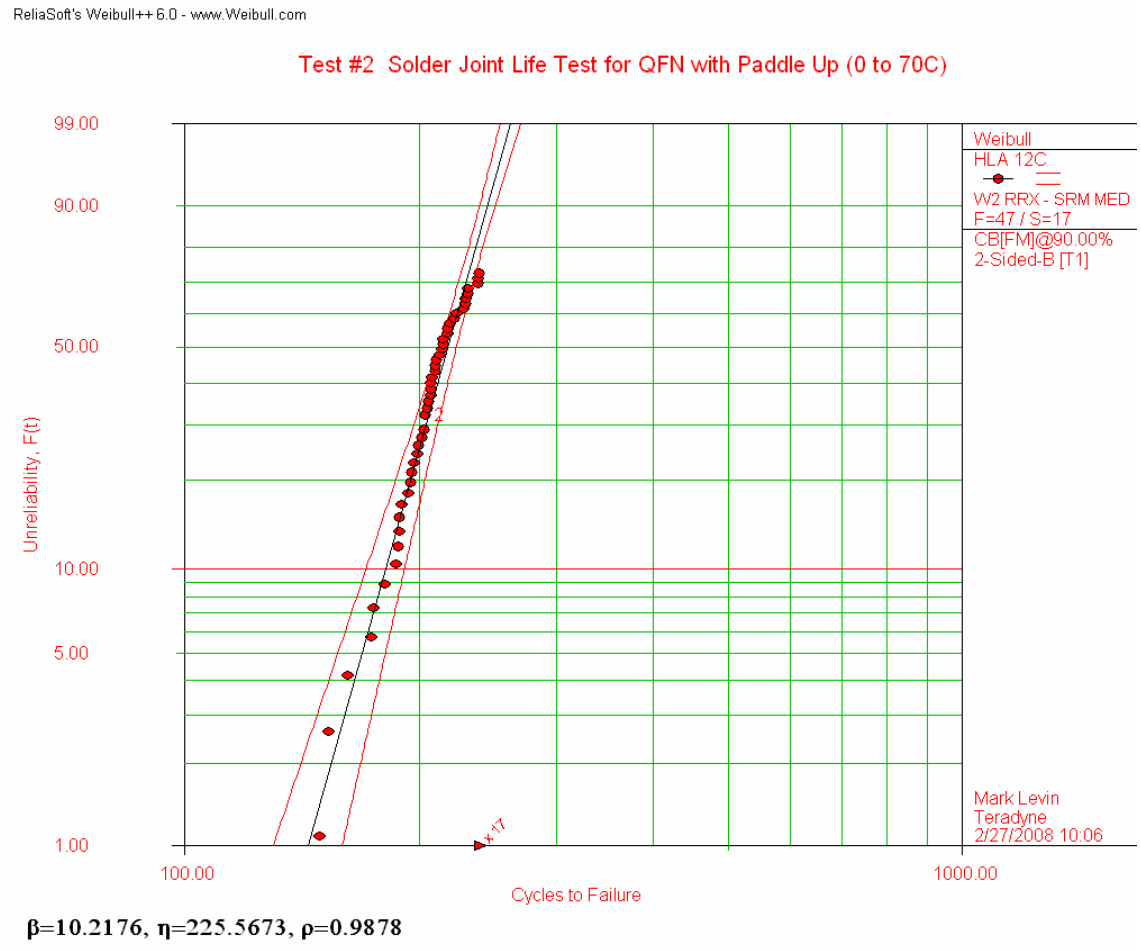


Figure 50 Weibull unreliability distribution for thermal cycling test #2

The unreliability Function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{225.6}\right)^{10.22}}$$

Unreliaiblity = $F(T) = 1 - R(T) = 1 - e^{-\left(\frac{T}{\eta}\right)^{\beta}} = 1 - e^{-\left(\frac{T}{225.6}\right)^{10.22}}$

$$f(t) = \left(\frac{\beta}{\eta}\right)\left(\frac{T}{\eta}\right)^{\beta-1} e^{-\left(\frac{T}{\eta}\right)^{\beta}} = \left(\frac{10.22}{225.6}\right)\left(\frac{T}{225.6}\right)^{10.22-1} e^{-\left(\frac{T}{225.6}\right)^{10.22}}$$

Where:

$f(T) \geq 0,\ T \geq 0,\ \beta > 0,\ \eta > 0$

The mean time to failure is:

$$\overline{T} = \eta \cdot \Gamma\left(\frac{1}{10.2176} + 1\right) = 225.57 \cdot (0.95221) = 214.8$$

The standard deviation is:

$$\sigma_T = \eta\sqrt{\Gamma\left(\frac{2}{\beta}+1\right) - \Gamma\left(\frac{1}{\beta}+1\right)^2} = 225.57\sqrt{\Gamma\left(\frac{2}{10.2176}+1\right) - \Gamma\left(\frac{1}{10.2176}+1\right)^2} =$$

$$= 225.57\sqrt{\Gamma(1.19574) - \Gamma(1.09787)^2} = 225.57\sqrt{0.91931 - (0.95221)^2} = 25.33$$

Test #	Thermal Cycling Range	N_f(1%)	N_f(50%)	N_f(63.2%)	β
1	0 °C to 70 °C	144	218	226	10.22

Table 19 Failure-rate summary using developed Weibull: Method 1 test #2

4.3.3 Solder-Joint Failure Analysis Investigation

Upon completion of the thermal cycling test, cross sections were made into the lead attachment to determine if solder-joint fracture was the root cause of the failure. Two cross sections were made of the failed QFN ASIC (Figure 51).

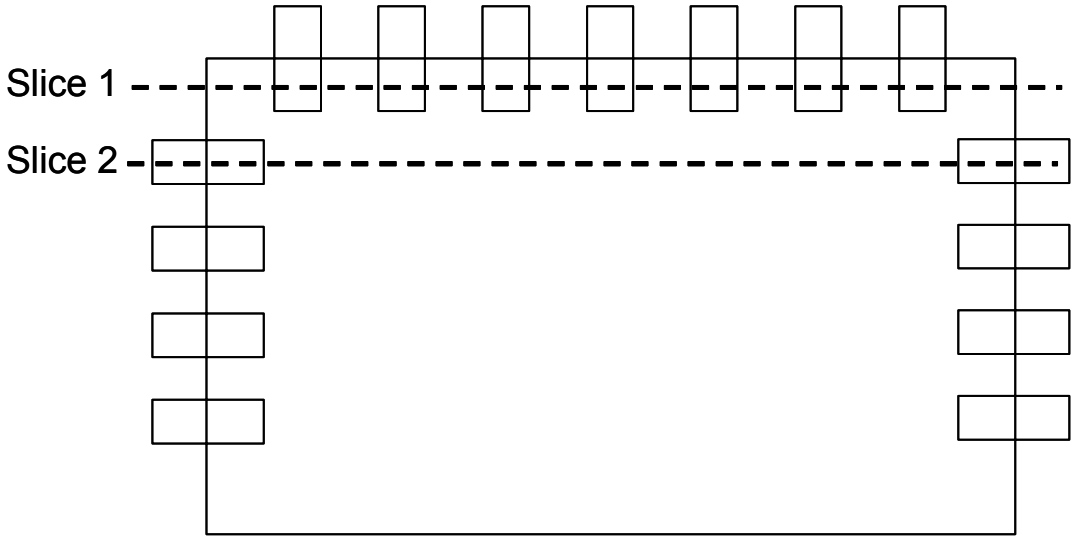


Figure 51 Location of Cross section

As a baseline, a good unstressed QFN solder-joint was cross sectioned (Figure 52). The cross section was made along slice 1, which is a transverse section along all of the solder joints on one edge of the QFN. The cross section showed no evidence of cracking on any of the solder joints. Some voiding can be seen in the solder, the voiding is located at the interface between the QFN and eutectic solder. The intermetallic compounds at the interface all appear normal.

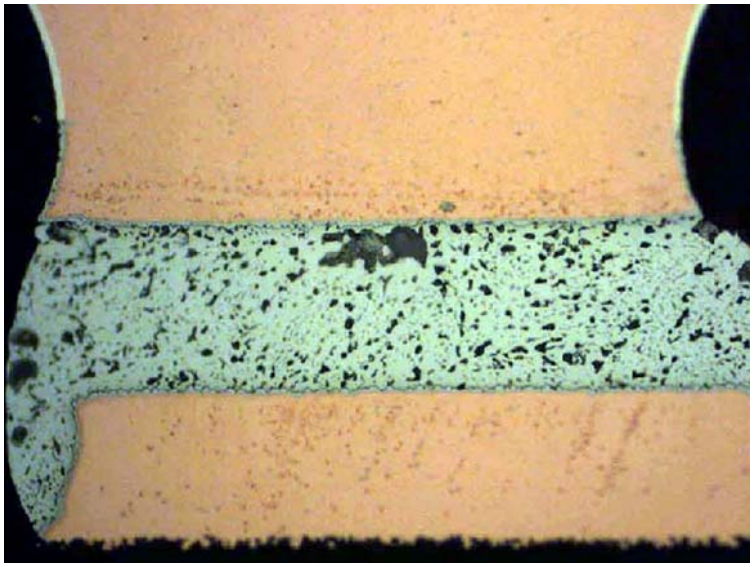


Figure 52 Cross section of an Unstressed QFN Solder connection

Two cross sections of the failed QFN package were performed after completion of thermal cycling using method one test number one. The first cross section clearly shows the presence of a complete solder fracture between the QFN and solder Figure 53). The intermetallic formation at both the circuit board pad to solder and the QFN lead surface to solder appear normal (Figure 54). The fracture runs completely through the solder just below the QFN lead surface. There is also a large vertical displacement in the crack between the solder surface and the QFN lead. The large separation is unusual for a shear solder fracture and suggests that there is a vertical force component contributing to the failure. The vertical force could be due to a preloaded stress in the QFN package, package warping or a dynamic warpage that is temperature dependent and seen cyclically during thermal cycling.

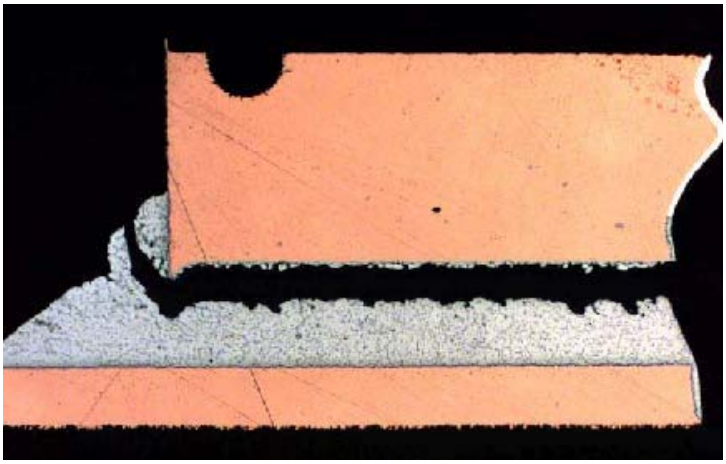


Figure 53 Cross section after completion of thermal cycling (Method 1 test 1)

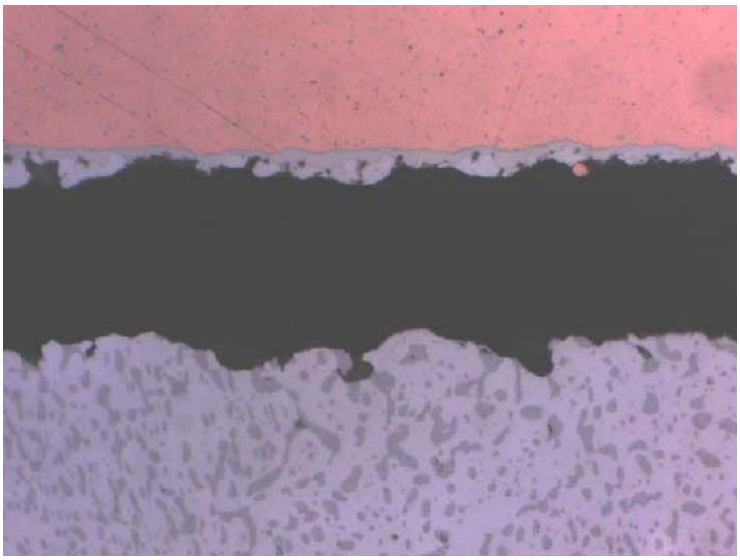


Figure 54 Magnified view of cross section

Cross sectioning a second QFN solder connection occurred along slice number two of Figure 51 above. The cross section exhibits more voiding than was observed in the first

cross section. However, the solder crack is completely through the solder connection and there is a gap indicating a force tending to lift the lead from the circuit bard surface. The intermetallic interface at the mating surfaces appears normal for a eutectic connection. The fracture is primarily through the solder, indicating a mostly cohesive separation.

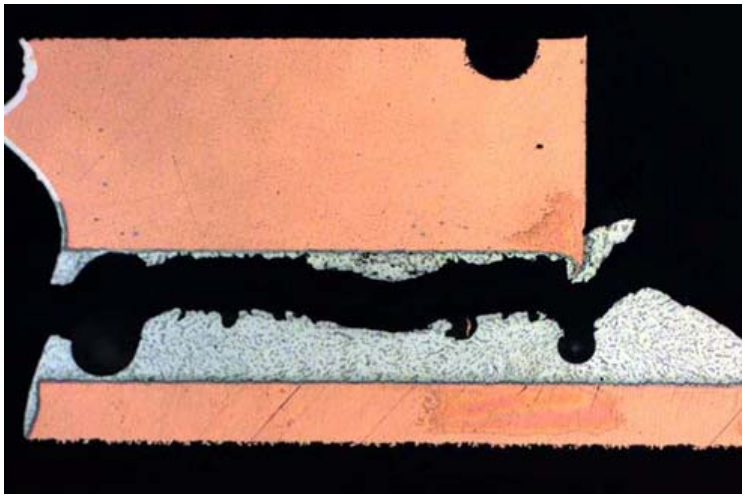


Figure 55 Cross section along the length of the solder connection (slice #2)

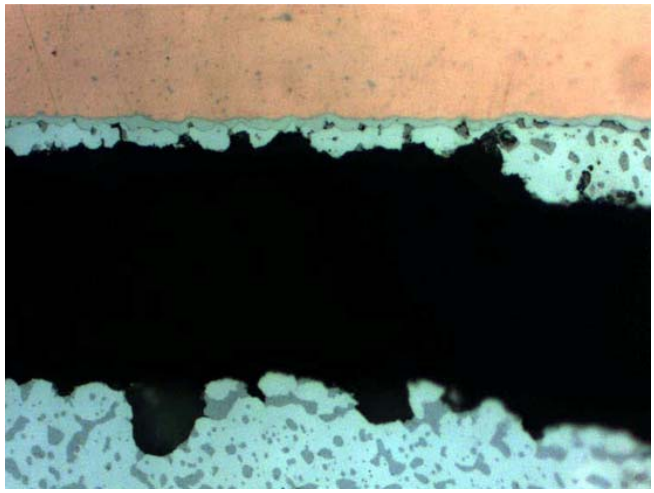


Figure 56 Magnified view of slice #2

4.3.4 Acceleration Model Analysis

Having completed accelerated life testing and Weibull distributions defined, an accelerated life model is developed. The acceleration rate is defined by an inverse power law model. The accelerated life model is constructed by nesting the inverse power law model for different thermal cycling ranges into the Weibull reliability model. The Weibull reliability model is:

$$f(t)=\left(\frac{\beta}{\eta}\right)\left(\frac{T}{\eta}\right)^{\beta-1} e^{-\left(\frac{T}{\eta}\right)^{\beta}}$$

The inverse power law model is:

$$L(V,T)=\frac{1}{A(\Delta T)^{n}}$$

Where:

$L(V,T)=\eta$, the characteristic number cycles to failure

ΔT = The Thermal Cycle temperature swing = $(T_{max} - T_{min})$

n = Inverse power law exponent

A = Characteristice life constant

The Weibull probability distribution function for an inverse power law acceleration rate is:

$$f(t,V)=\left(\frac{\beta}{\frac{1}{A(V)^n}}\right)\left(\frac{t}{\frac{1}{A(V)^n}}\right)^{\beta-1}\left(e^{-\left(\frac{t}{\frac{1}{A(V)^n}}\right)^{\beta}}\right)=\beta A(V)^n\left(tA(V)^n\right)^{\beta-1}e^{-\left(tA(V)^n\right)^{\beta}}$$

The Weibull failure rate for an inverse power law acceleration rate is:

$$\lambda(V,T)=\frac{f(V,T)}{R(V,T)}=\beta A(V)^n(AVT)^{\beta-1}$$

There are four unknowns. They are β, η, A and η. The variables can be solved used Alta 6.0 reliability software from Reliasoft's or using hand equations and graphic plotting. Both methods were pursued. The first variable, β, should not significantly vary for different thermal cycling stress tests. If it does, it is an indication that there could be multiple failure modes involved and that the different failure modes may have different acceleration models. If there are two failure modes, they need to be treated separately. The failure test data would need to be separated into two groups and each failure group modeled separately. The system failure is the summation of the two failure models. If you are describing the failure in terms of the reliability function R(t), then it would be the product of the two reliability equations.

There are several ways to estimate β. One method is average β from the two test results. Since there is only two data points and no prior information regarding the failure shape is

assumed, the averaging method is considered to be the best. For the two stress test, β = 8.1099 and 10.2176. The values are close in value, so it is reasonable to assume that there is only one failure mechanism involved. The average β based on this method is:

$$\beta = \left(\frac{\beta_1 + \beta_2}{2}\right) = \left(\frac{8.1099 + 10.2176}{2}\right) = 9.2$$

The slope n, can be determined graphically by plotting the characteristic life on a life vs. stress chart. The two data points for the characteristic life determined for test one and test two are plotted. For test #1, η=132 with the thermal cycling stress ΔT=70-(-25) =95°C. For test 2, η=226 with the thermal cycling stress ΔT=70-(0) =70°C (Figure 57).

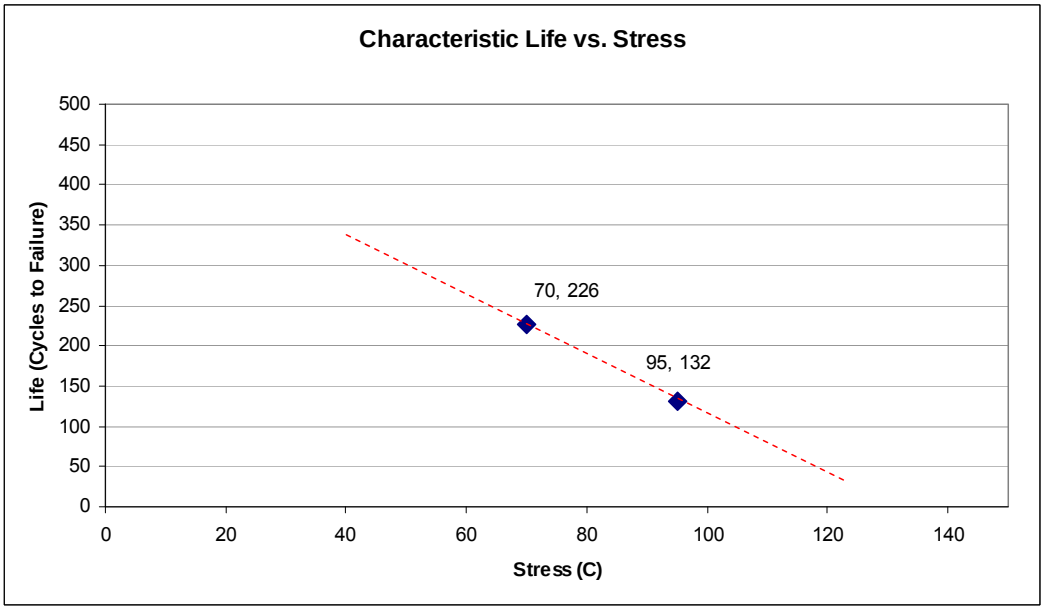


Figure 57 Life stress plot for characteristic life

$$L(V) = \frac{1}{KV^n}$$

$$Ln(L) = -\ln K - n \ln V$$

$$Slope \;\; n = \frac{\ln(T_2) - \ln(T_2)}{\ln(V_2) - \ln(V_2)} = \frac{\ln(226) - \ln(132)}{\ln(95) - \ln(70)} = 1.71$$

Finally, the value of "A" is estimated for the inverse power law model. To calculate the value of A this manually requires knowing the two characteristic failures at the two thermal cycling levels. For test #1, η=132 and ΔT=70-(-25) =95^{o}C, for test 2, η=226 and ΔT=70-(0) =70^{o}C. For each thermal stress the value for η and ΔT are entered into the inverse power law model and the equation is solved for the value of "A". Upon completion, there are two close but different values for "A". Using the same averaging technique used to estimate β, the average value of "A" was determined.

$$\eta = \frac{1}{A(\Delta T)^n} = \frac{1}{(A)(\Delta T)^{1.71}}$$

Where :

η = The characteristic number of cycles to failure

ΔT = The Thermal Cycle temperature swing

n = Inverse power law exponent = 1.1

A = Characteristice life constant

For test #1 : The reliability equation for the percent surviving for number of thermal cycles "t" is :

$$A_{\Delta T=95} = \frac{1}{\eta(\Delta T)^n} = \frac{1}{(132)(70-(-25))^{1.71}} = 3.14\times10^{-6}$$

For test #2 : The reliability equation for the percent surviving for number of thermal cycles "t" is :

$$A_{\Delta T=70} = \frac{1}{\eta(\Delta T)^n} = \frac{1}{(226)(70-(0))^{1.71}} = 3.1\times10^{-6}$$

$$A = \frac{(A_{\Delta T=95} + A_{\Delta T=70})}{2} = \frac{(3.14426\times10^{-6} + 3.0958\times10^{-6})}{2} = 3.12\times10^{-6}$$

Using a hand calculation and graphical plotting the constants for the model are:

β= 9.1637

A=3.12003x10^{-6}

n=1.71The final model based on hand calculations is:

$$L(V,T)=\frac{1}{A(\Delta T)^{n}}=\frac{1}{3.12003\times10^{-6}(\Delta T)^{1.71}}$$

$$R(T)=e^{-\left(\frac{T}{\eta}\right)^{\beta}}=e^{-\left(\frac{T}{\frac{1}{A(\Delta T)^{n}}}\right)^{\beta}}=e^{-\left(\frac{T}{\frac{1}{3.12\times10^{-6}(\Delta T)^{1.71}}}\right)^{9.16}}$$

The alternative method to estimate the values for the constants β, A and n is to use Reliasoft's, Alta 6.0 software. Using Alta 6.0, the values for β, A and n are estimated (Figure 58 and Figure 59):

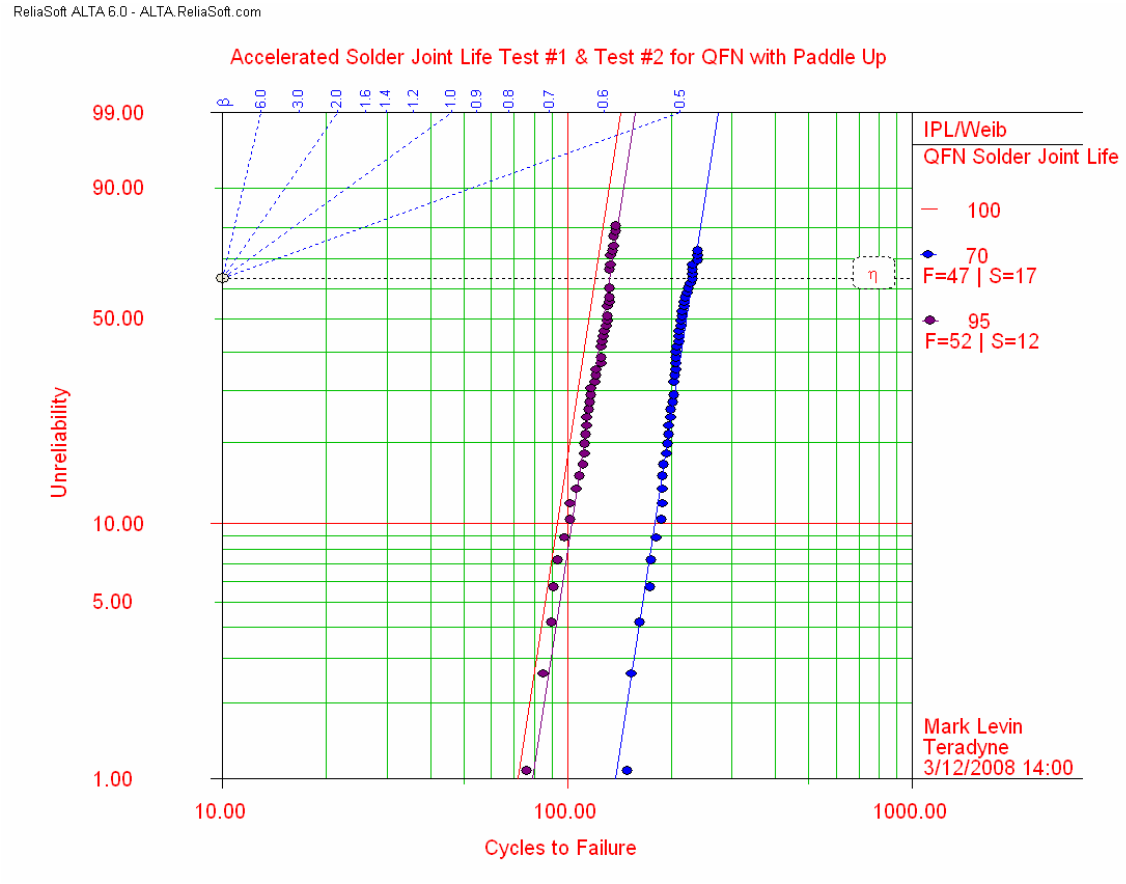


Figure 58 Reliasoft Alta 6.0 plot of accelerated life

Life Stress Relation: Inverse Power Law	
$L(V) = \frac{1}{K \cdot V^n}$	
K =	1.9256E-6
n =	1.8175
Life Distribution:Weibull	
$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}} \quad where \quad \eta = L(V_i)$	
β =	8.9195918606813
η =	Function of Life-Stress Relation

Figure 59 Reliasoft Alta 6.0 parameters IPL-Weibull model

$$\eta = \frac{1}{A(\Delta T)^n} = \frac{1}{(1.9256\times10^{-6})(15)^{1.8175}} = 3{,}783 \text{ cycles}$$

Reliasoft Alta 6.0 estimates "β" using the following maximum likelihood equations:

$$\Lambda = \sum_{i=1}^{F} N_i \cdot \ln\left[\left(\frac{\beta}{\frac{1}{A(\Delta T)^n}}\right)\left(\frac{T}{\frac{1}{A(\Delta T)^n}}\right)^{\beta-1}\left(e^{-\left(\frac{T}{\frac{1}{A(\Delta T)^n}}\right)^{\beta}}\right)\right] - \sum_{i=1}^{S} N_i'(\ )$$

$$\frac{\partial\Lambda}{\partial\beta} = 0,\ \frac{\partial\Lambda}{\partial A} = 0,\ \frac{\partial\Lambda}{\partial n} = 0$$

$$\frac{\partial\Lambda}{\partial\beta} = \frac{1}{\beta}\sum_{i=1}^{F_e} N_i + \sum_{i=1}^{F_e} N_i \ln\left(AV_i^n T_i\right) - \sum_{i=1}^{F_e} N_i \ln\left(AV_i^n T_i\right)^{\beta} \ln\left(AV_i^n T_i\right) - \sum_{i=1}^{S} N_i' \ln\left(AV_i^n T_i'\right)^{\beta} \ln\left(AV_i^n T_i'\right)$$

$\hat{\beta} = 8.9196$ (using Reliasoft Alta 6.0)

$$\frac{\partial\Lambda}{\partial A} = \frac{\beta}{A}\sum_{i=1}^{F_e} N_i + \frac{\beta}{A}\sum_{i=1}^{F_e} N_i \ln\left(AV_i^n T_i\right)^{\beta} - \frac{\beta}{A}\sum_{i=1}^{S} N_i'\left(AV_i^n T_i'\right)^{\beta}$$

$\hat{A} = 1.9256\text{E-}6$ (using Reliasoft Alta 6.0)

$$\frac{\partial\Lambda}{\partial n} = \beta\sum_{i=1}^{F_e} N_i n(V_i) + \beta\sum_{i=1}^{F_e} N_i \ln(V_i)\left(AV_i^n T_i\right)^{\beta} - \beta\sum_{i=1}^{S} N_i' \ln(V_i)\left(AV_i^n T_i'\right)^{\beta}$$

$\hat{n} = 1.8175$ (using Reliasoft Alta 6.0)

Reliasoft model for the confidence bounds are:

$$\beta_U = \hat{\beta} \cdot e^{\frac{A_\alpha \sqrt{Var(\hat{\beta})}}{\hat{\beta}}}$$
$$\beta_L = \hat{\beta} \cdot e^{-\frac{A_\alpha \sqrt{Var(\hat{\beta})}}{\hat{\beta}}}$$

$$A_U = \hat{A} \cdot e^{\frac{A_\alpha \sqrt{Var(\hat{A})}}{\hat{A}}}$$
$$A_L = \hat{A} \cdot e^{-\frac{A_\alpha \sqrt{Var(\hat{A})}}{\hat{A}}}$$

$$n_U = \hat{n} + A_\alpha \sqrt{VAR(\hat{n})}$$
$$n_L = \hat{n} - A_\alpha \sqrt{VAR(\hat{n})}$$

The variances for β, A and n can be estimated from the Fisher Matrix evaluated at $\hat{\beta}$, $\hat{A}$ and $\hat{n}$

$$\begin{bmatrix} Var(\hat{\beta}) & Cov(\hat{\beta},\hat{A}) & Cov(\hat{\beta},\hat{n}) \\ Cov(\hat{A},\hat{\beta}) & Var(\hat{A}) & Cov(\hat{A},\hat{n}) \\ Cov(\hat{n},\hat{\beta}) & Cov(\hat{n},\hat{A}) & Var(\hat{n}) \end{bmatrix} = \begin{bmatrix} -\frac{\partial^2 \Lambda}{\partial \beta^2} & -\frac{\partial^2 \Lambda}{\partial \beta \partial A} & -\frac{\partial^2 \Lambda}{\partial \beta \partial n} \\ -\frac{\partial^2 \Lambda}{\partial A \partial \beta} & -\frac{\partial^2 \Lambda}{\partial A^2} & -\frac{\partial^2 \Lambda}{\partial A \partial n} \\ -\frac{\partial^2 \Lambda}{\partial n \partial \beta} & -\frac{\partial^2 \Lambda}{\partial n \partial A} & -\frac{\partial^2 \Lambda}{\partial n^2} \end{bmatrix}^{-1}$$

Solving for a 90% confidence level using rteliasoft Alta 6.0

$\beta_U = 10.3$

$\beta_L = 7.7$

$A_U = 3.2931\text{E-}6$

$A_L = 1.1260\text{E-}6$

$n_U = 1.9391$

$n_L = 1.6959$

Applying Reliasoft's IPL – Weibull model to the customer use environmental condition, we get:

$$\eta = \frac{1}{A(\Delta T)^n} = \frac{1}{(1.9256\times10^{-6})(15)^{1.8175}} = 3{,}783 \text{ cycles}$$

Where:

η = The characteristic number cycles to failure

ΔT = The Thermal Cycle temperature swing = (35C - 20C)

n = Inverse power law exponent = 1.8175

A = Characteristice life constant = 1.9256×10^{-6}

The reliability equation for the percent surviving for

number of thermal cycles "t" is:

$$\mathrm{R}(\mathrm{t}) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} = e^{-\left(\frac{t}{3783}\right)^{9.5}}$$

The reliability as a funtion of thermal cyclic stress is described by:

$$\mathrm{R}(\mathrm{t}) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} = e^{-\left(\frac{t}{\frac{1}{A(\Delta T)^n}}\right)^{\beta}}$$

The reliability simulation using Monte Carlo provides the following graph (Figure 60):

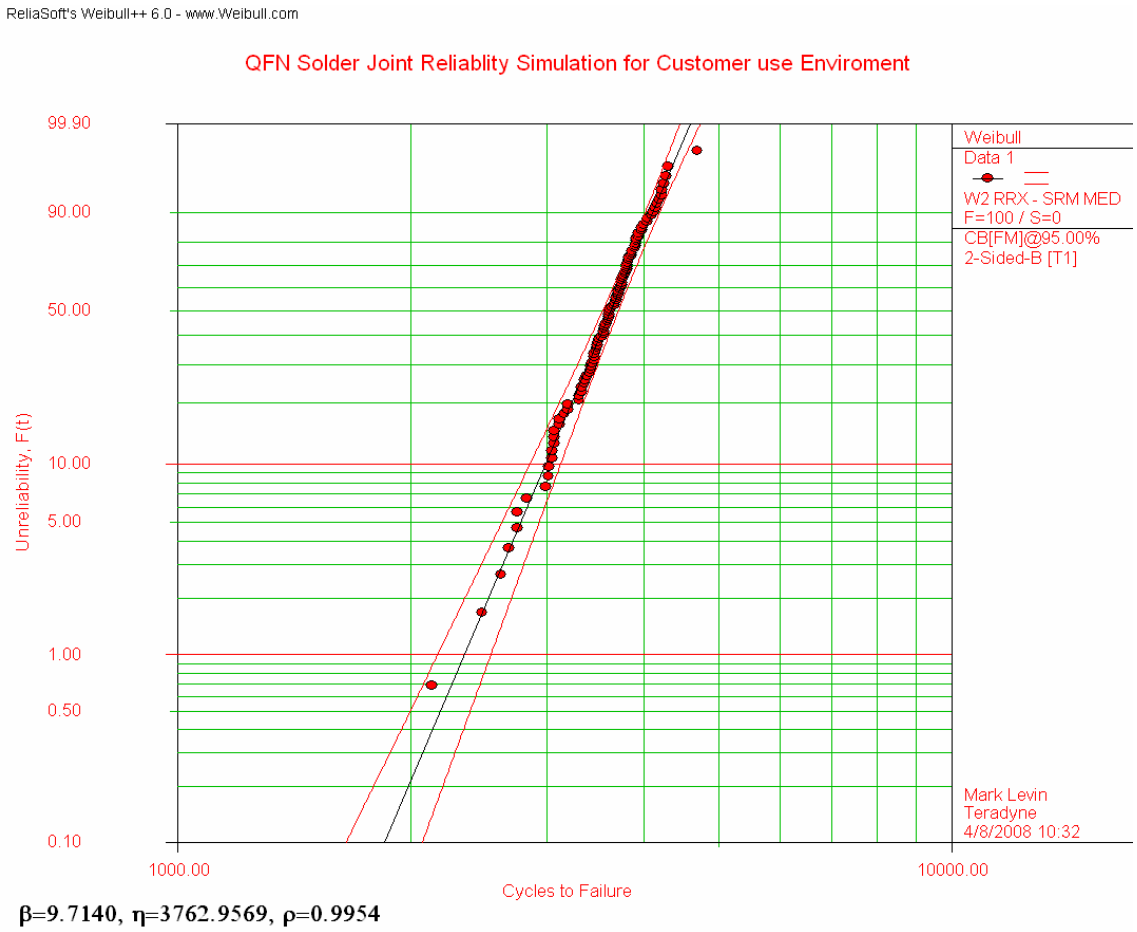


Figure 60 Monte Carlo simulated plot of customer use condition

4.4 Reliability Stress Test Method 2 (Daisy-chained Test Board)

One concern regarding the previous testing is that real parts were used in an operational state to determine when a solder-joint failed. The industry standard for this type of testing is to develop a test board replicating the use conditions and made of similar parts in a Daisy chain pattern. The daisy chain test method measures the change in contact resistance as a function of thermal cycling. This was not performed because an answer regarding the solder-joint reliability of the QFN slug up package was needed right away. Using real QFN ASICs in production material meant no lead time, and testing could start right away. Implementing a daisy chain test takes about three months to develop. Daisy chain parts need to be manufactured by the supplier using real product package and die. Test boards then need to be designed and fabricated. The final step is to have a manufacturer assemble the QFN parts onto the test boards.

In addition to repeating the accelerated life test using daisy-chained parts, an investigation into ways to improve the solder-joint reliability was conducted. Several experiments were conducted. The experiments are:

1) Evaluate the improvement in lead compliance due to the addition of a solder bump on top of the QFN, the solder bump add lead compliance.
2) Evaluate the improvement resulting from increasing the CTE of mold compound to reduce global strain between package and circuit board.

3) Evaluate the influence Sn versus NiPdAu lead finish plating has on solder-joint reliability.

4) Evaluate the improvement from removal of the solder mask clearance underneath the package.

5) Evaluate the improvement resulting from adding epoxy around the perimeter of the package to reduce the stress due to CTE mismatch.

To add a solder bump to each pad, the QFN was flipped around so it was laying flat on the top-side paddle. With the leads exposed, a 5 mil solder paste stencil was used to dispense solder paste onto each pad. After solder paste inspection, the part went through a solder reflow process where the paste would coalesce into a solder bump. The solder bump height is estimated to be 2.5 mils after reflow soldering. A 2.5 mil solder bump increases the solder-joint height by a factor of 2.

The other solution to be evaluated was a higher CTE mold compound to better match thermally with the circuit board. The proposed mold compound is a Sumitomo EME-7730LF compound with a CTE of $9x10^{-6}/^{o}C$. Increasing the CTE of the mold compound better matches it thermally to the circuit board. If the two are perfectly matched, then no stress would be created at the solder-joint from a change in ambient temperature.

4.4.1 Daisy-Chained Circuit Board Design

The daisy chain test boards were designed to be very similar to the production design concept. The daisy chain test board has the same outline drawing as the production design. The test board has the same length, width and thickness as the production design. The test board used the same lamination spec as the production design. Thus, the design has the same number of circuit board layers, layer thicknesses and copper weight as the production design. To achieve this equivalency the product circuit board was used with the top layer modified to incorporate the daisy chain pattern (Figure 61). This ensured equivalency between the two methods used for solder-joint reliability testing. The test board has two rows of QFN devices. Each row contains 16 daisy-chained QFN packages. The reference designators for the 32 to QFN's under test are shown in (Figure 62)

Figure 61 Product circuit board showing QFN's

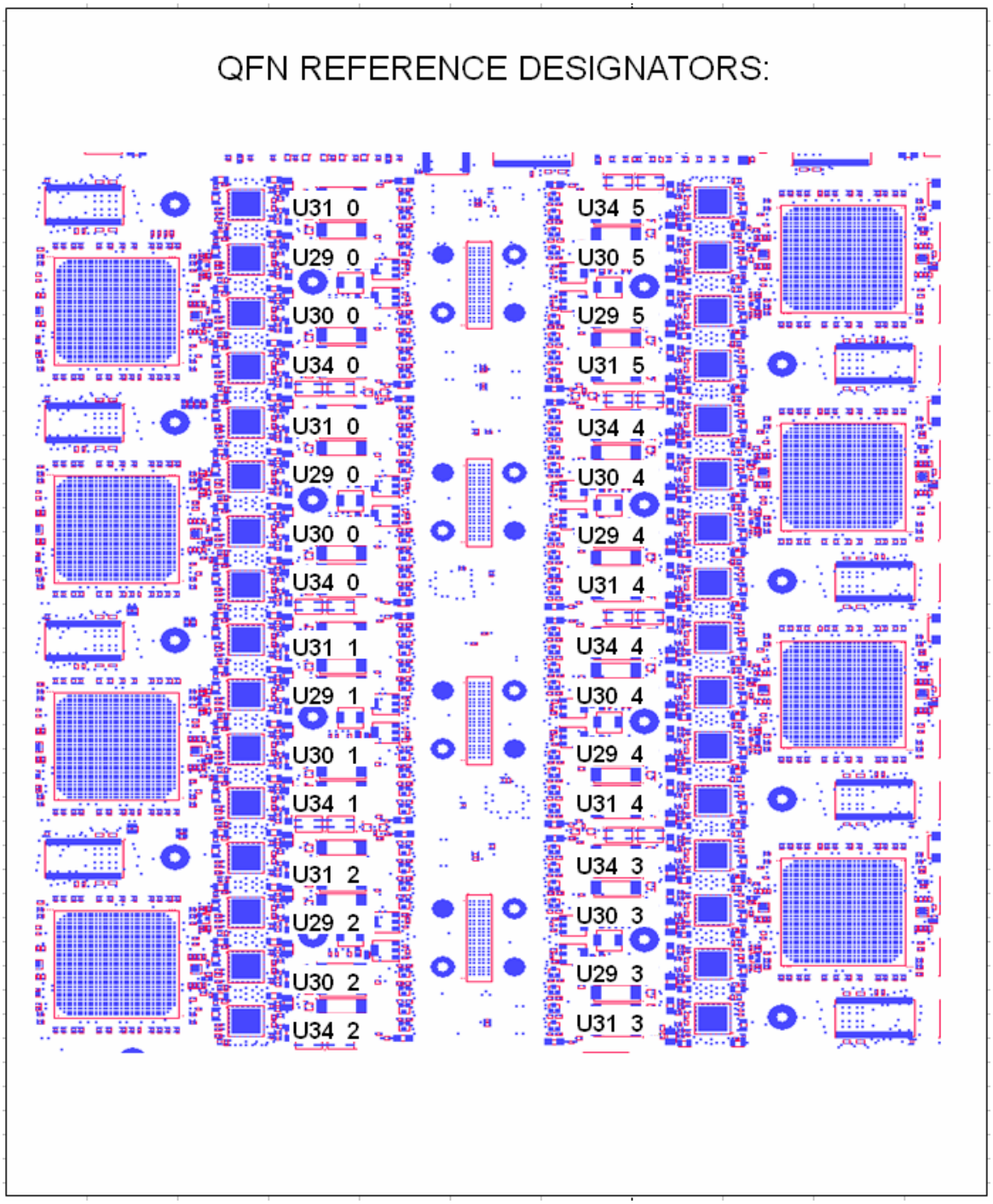


Figure 62 Test board with reference designation for 32 daisy chain QFN's

The daisy chain test pattern consisted of five continuity loops (Figure 63). Four continuity loops were used to monitor the corners of the package. These loops are referenced Loop 1, Loop 2, Loop 3 and Loop 4. Loop 5 measures the middle leads around the four sides of the package. The five test loops will be used to determine the location of the initial failure due to an increase in resistance. This test strategy will show if a particular corner is more likely to fail or if failure is occurring first in the center of the package..

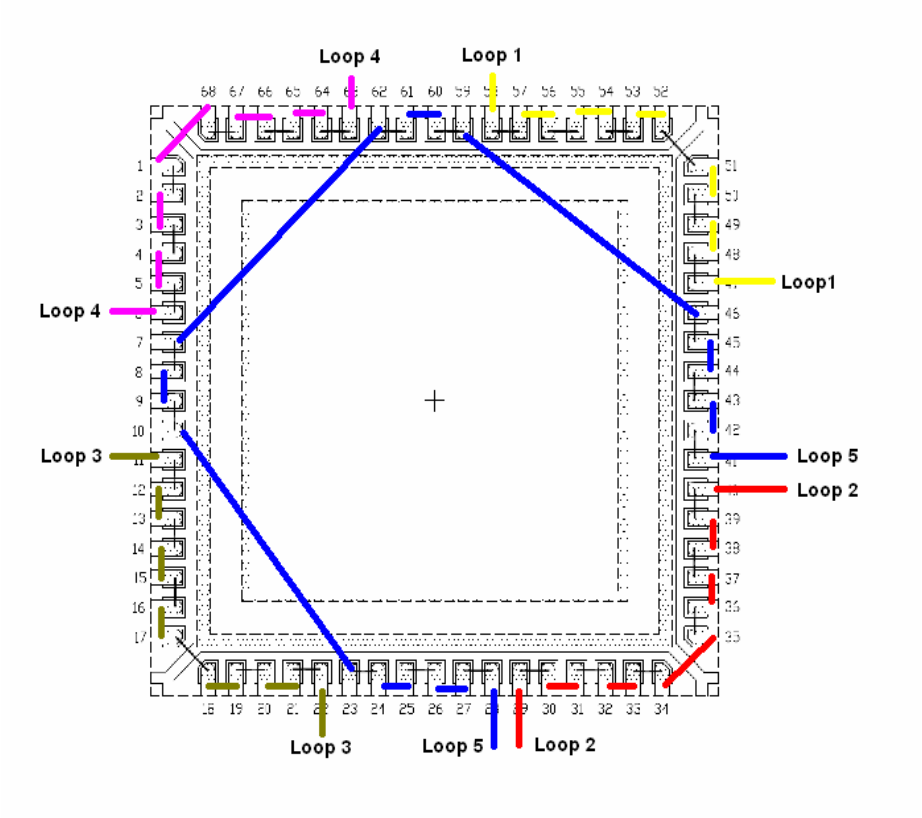


Figure 63 Daisy chain QFN package with five continuity loops

The daisy chain QFN package is based on the same physical package as the production QFN package. The daisy chain package has the same outline drawing, package thickness, pad pattern and material stack up as the production package. The major difference between the two packages is that the die used for the daisy chain QFN package is physically the same but is an electrical reject from wafer fabrication. Every other pad of the daisy chain part is connected internally at the carrier through a one mil gold wire bond (Figure 64).

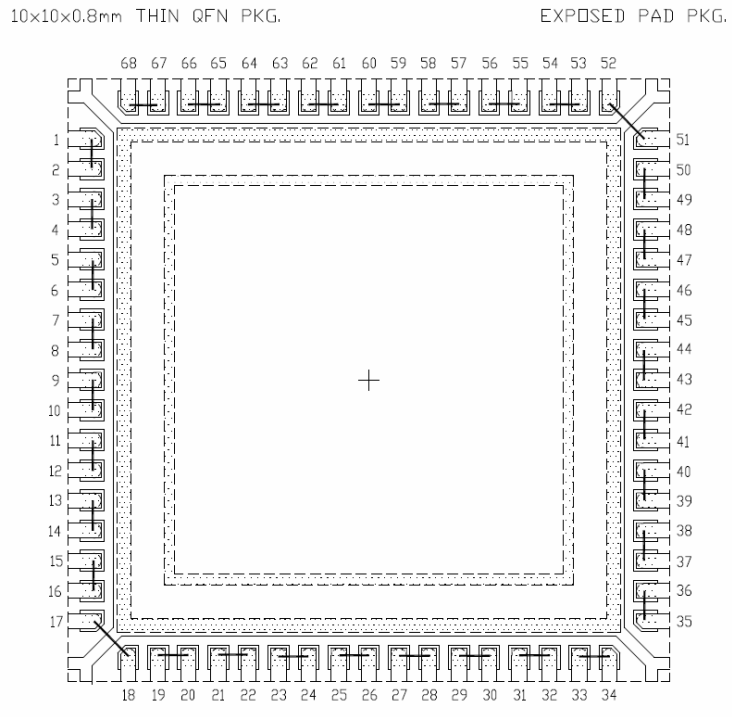


Figure 64 Daisy chain pattern

Resistance measurements were made using a four-wire measurement test set up. The force and sense lines are tied together at the circuit board; this removes the resistance of the cables going to the circuit board and the connector at the circuit board. The resistance path going from the edge of the circuit board through the daisy chain path and back varied between 0.200 and 0.300 ohms. Two base line resistance measurements were made during the first thermal cycle. Base line resistance measurements were made at both the upper and lower temperature limit. The product temperature was determined by placing a thermal couple on the circuit board under test. The base line measurements were recorded five minutes after the product temperature set point was reached. The five minute dwell ensured temperature stability before taking resistance measurements. A failure in the connection was recorded when the change in resistance increased 0.300 ohms.

4.4.2 Reliability Stress Test Method 2: Test #1 (0oC to 100 oC)

Test number one consisted of thermal cycling four test boards between 0^{o}C and 100^{o}C. The four test boards contain the following six experiments:

Experiment #1: Sn lead (tin) plating & solder mask removed in middle area

Experiment #2: Sn lead plating

Experiment #3: NiPdAu (nickel-palladium gold) lead plating

Experiment #4: NiPdAu lead plating & solder mask removed in middle area

Experiment #5: NiPdAu lead plating & new mold compound

Experiment #6: NiPdAu lead plating & perimeter epoxy

Experiment number one evaluated the influence solder mask underneath the middle of the package has on reliability (Figure 65). Removing the solder mask provides an additional couple mils of clearance between the bottom of the QFN package and the top of the circuit board. The removal of the solder mask will provide additional clearance should the package bow during thermal expansion.

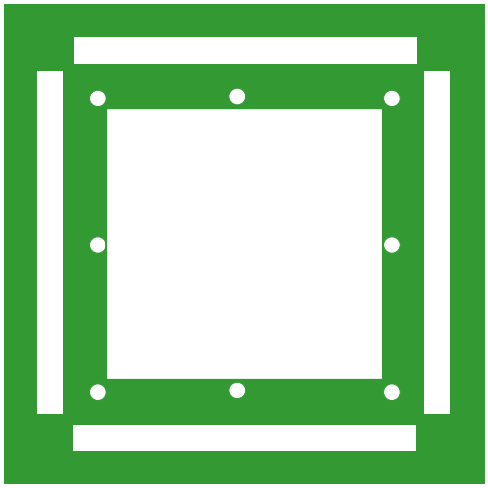


Figure 65 Modified solder mask showing removal solder mask removed in middle

Experiment number two is the baseline for the standard QFN package with tin lead plating. Experiment number three evaluates the improvement in reliability due to nickel-palladium-gold lead plating. Experiment number four will evaluate the improvement in reliability due to nickel-palladium-gold lead plating and solder mask removal underneath the middle of the package. Experiment number five evaluates the reliability improvement

due to nickel-palladium-gold lead plating and a new mold compound with a higher CTE. The new mold compound has a CTE of $9.0x10^{-6}$ which better matches the CTE of the printed circuit board. The final experiment evaluates the improvement in reliability due to nickel-palladium-gold lead plating any perimeter bead of epoxy (Figure 66).

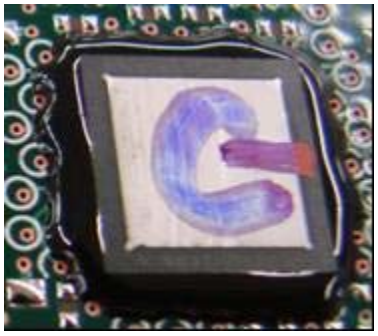


Figure 66 Perimeter bead epoxy

Temperature cycling test was performed on March 26th, 2008 and ended on April 29th, 2008 Testing was terminated after 988 thermal cycles. After 988 thermal cycles, experiments #1 through #5 had 100% of the QFN packages failed for solder-joint reliability. Experiment #6, which had the perimeter epoxy, had zero failures. The cycles to failure data was entered into Reliasoft's Weibull++ version 6 and a 2-parameter Weibull distribution model was used to fit the data. The times to failure are shown in Table 20 and Table 21. The tables show the number of thermal cycles to failure, the increase in resistance and the temperature at which failure occurred. The increase in resistance is noted in the column titled "Delta Value". The column titled "Chain #" references the chain loop where failure occurred. Only the first failure in the part was

recorded. A loop failure is defined as an increase in loop resistance of 0.300 Ohms or greater. The Weibull charts for experiments 1 through 5 are shown in Figure 67 through Figure 71.

Accelerated Reliability Stress Test Method #2: Test #1 (0°C to 100°C)

Exp # 1 Sn & Cleared Solder Mask					Exp # 2 Sn					Exp # 3 NiPdAu				
Temp	Cycle #	Delta Value	U #	Chain #	Temp	Cycle #	Delta Value	U #	Chain #	Temp	Cycle #	Delta Value	U #	Chain #
100	46	0.540389	U29_00	Chain 1	100	32	0.641348	U30_16	Chain 4	100	107	0.876938	U34_56	Chain 4
100	50	1.790511	U31_00	Chain 3	100	34	211000000	U31_24	Chain 1	0	121	0.520811	U31_40	Chain 1
100	61	0.60968	U30_00	Chain 4	100	35	0.301062	U30_24	Chain 3	100	122	0.536913	U29_40	Chain 1
0	70	0.532012	U29_00	Chain 4	0	37	0.502	U29_08	Chain 4	100	123	0.302619	U31_56	Chain 4
0	72	2.890838	U31_00	Chain 1	0	39	10.734418	U34_08	Chain 4	0	126	0.353928	U29_48	Chain 2
100	72	0.307148	U34_00	Chain 4	0	42	0.517546	U29_08	Chain 4	100	126	0.569566	U30_48	Chain 4
100	79	0.526871	U34_00	Chain 3	100	45	14.518699	U31_24	Chain 4	100	130	0.580926	U31_56	Chain 4
100	94	0.652798	U30_00	Chain 3	0	46	0.57865	U29_24	Chain 4	0	138	0.519793	U30_48	Chain 1
					100	47	0.774022	U30_08	Chain 3	100	138	0.470947	U34_40	Chain 2
					0	47	211000000	U29_24	Chain 4	100	138	0.681592	U31_40	Chain 4
					100	48	0.630163	U31_16	Chain 5	0	139	0.421633	U34_48	Chain 4
					100	50	0.477427	U34_16	Chain 5	100	141	0.555188	U34_56	Chain 2
					0	53	0.442077	U34_24	Chain 3	100	142	0.348435	U29_56	Chain 3
					100	53	0.441528	U31_16	Chain 4	100	142	0.451763	U30_56	Chain 4
					100	58	0.950425	U31_08	Chain 4	0	146	0.382737	U29_48	Chain 1
					100	59	1.535227	U30_08	Chain 3	0	153	0.571381	U29_40	Chain 2
					100	59	0.725861	U30_24	Chain 4	0	153	0.939705	U34_48	Chain 2
					100	62	0.637081	U31_08	Chain 3	0	158	0.637537	U34_40	Chain 2
					100	62	0.530844	U34_08	Chain 5	100	162	0.323779	U29_56	Chain 3
					0	63	0.415596	U29_16	Chain 1	100	163	1.854419	U30_40	Chain 2
					100	63	0.401749	U34_24	Chain 4	0	165	0.692816	U30_40	Chain 4
					100	67	0.739843	U29_16	Chain 4	100	172	0.599806	U31_48	Chain 2
					0	72	0.347053	U30_16	Chain 4	100	175	0.430904	U31_48	Chain 4
					100	89	0.43485	U34_16	Chain 4	100	183	0.547935	U30_56	Chain 1
Total Failing Devices				8	Total Failing Devices				24	Total Failing Devices				24
Total Devices				8	Total Devices				24	Total Devices				24
Suspensions				0	Suspensions				0	Suspensions				0
% Surviving				0%	% Surviving				0%	% Surviving				0%
% failing				100%	% failing				100%	% failing				100%
Total Cycles				346	Total Cycles				346	Total Cycles				346

Table 20 Experiments #1, #2 and #3 failure data

Accelerated Reliability Stress Test Method #2: Test #1 (0°C to 100°C)

Exp # 4 NiPdAu & Cleared Solder Mask					Exp # 5 NiPdAu & 7730 Mold Compound					Exp # 6 NiPdAu & EP1325 Epoxy				
Temp	Cycle #	Delta Value	U #	Chain #	Temp	Cycle #	Delta Value	U #	Chain #	Temp	Cycle #	Delta Value	U #	Chain #
100	105	0.750417	U30_32	Chain 4	100	261	0.329356	U34_08	Chain 4					
0	108	0.43331	U31_32	Chain 4	0	264	0.634581	U34_24	Chain 2					
0	118	0.534386	U30_32	Chain 2	100	269	0.380182	U30_00	Chain 4					
0	129	0.499747	U34_32	Chain 4	100	271	0.606381	U30_32	Chain 2					
100	131	0.453654	U34_32	Chain 4	100	295	0.446916	U30_40	Chain 4					
0	132	0.498648	U31_32	Chain 1	100	298	0.306546	U31_32	Chain 4					
0	153	0.40872	U29_32	Chain 3	100	298	0.331352	U34_32	Chain 4					
0	161	0.437293	U29_32	Chain 1	100	299	0.463599	U29_40	Chain 4					
					100	300	0.329141	U30_48	Chain 4					
					100	302	0.702595	U31_48	Chain 1					
					100	310	0.451779	U30_16	Chain 4					
					100	317	0.573773	U29_56	Chain 2					
					100	326	0.329192	U34_48	Chain 1					
					100	332	0.539214	U31_40	Chain 4	No failures				
					0	335	0.700119	U29_48	Chain 1					
					100	337	1.539405	U31_00	Chain 3					
					100	343	1.665067	U34_56	Chain 4					
					0	344	0.747522	U30_08	Chain 4					
					0	350	0.555317	U34_16	Chain 3					
					100	361	0.625414	U29_00	Chain 1					
					0	378	0.386767	U29_24	Chain 4					
					100	394	0.466009	U29_08	Chain 4					
					0	395	1.012432	U29_16	Chain 4					
					0	411	0.325181	U31_16	Chain 3					
					100	412	0.625498	U30_56	Chain 4					
					0	419	0.355383	U31_08	Chain 3					
					100	420	0.386636	U34_00	Chain 4					
					100	429	0.557799	U31_56	Chain 3					
					0	430	0.623764	U29_32	Chain 4					
					100	431	0.3221	U34_40	Chain 4					
					100	445	0.444918	U31_24	Chain 3					
					100	445	0.439272	U30_24	Chain 3					
Total Failing Devices				**8**	**Total Failing Devices**				**32**	**Total Failing Devices**				**0**
Total Devices				**8**	**Total Devices**				**32**	**Total Devices**				**32**
Suspensions				**0**	**Suspensions**				**0**	**Suspensions**				**32**
% Surviving				**0%**	**% Surviving**				**0%**	**% Surviving**				**100%**
% failing				**100%**	**% failing**				**100%**	**% failing**				**0%**
Total Cycles				**346**	**Total Cycles**				**530**	**Total Cycles**				**988**

Table 21 Experiments #4, #5 and #6 failure data

Experiment #1: Sn lead (tin) plating & solder mask removed in middle area

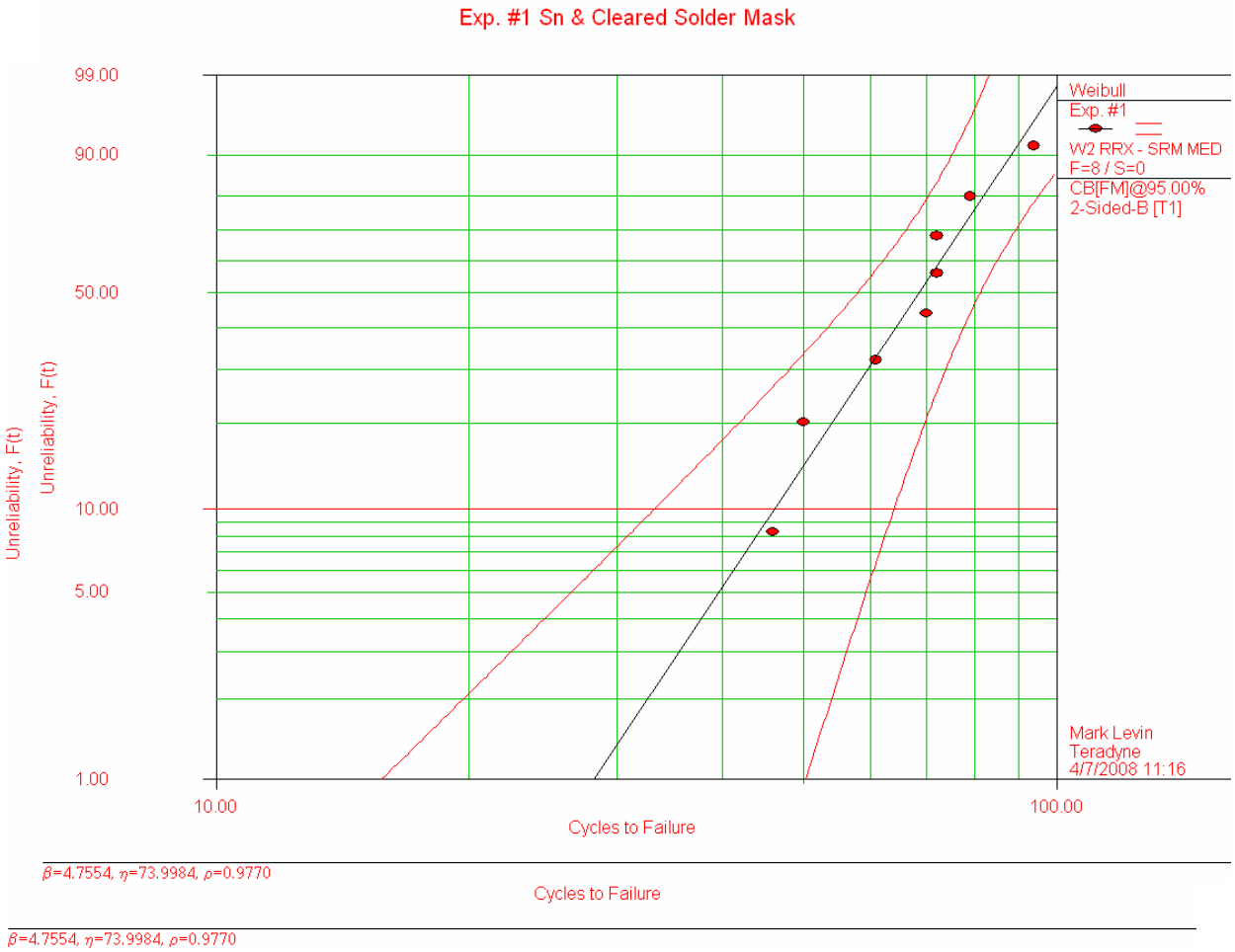


Figure 67 Tin plated lead with solder mask removed underneath part (0 ^{o}C to 100 ^{o}C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{74}\right)^{4.76}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 4.76$

$\eta = 74.0$

Experiment #2: Sn lead plating

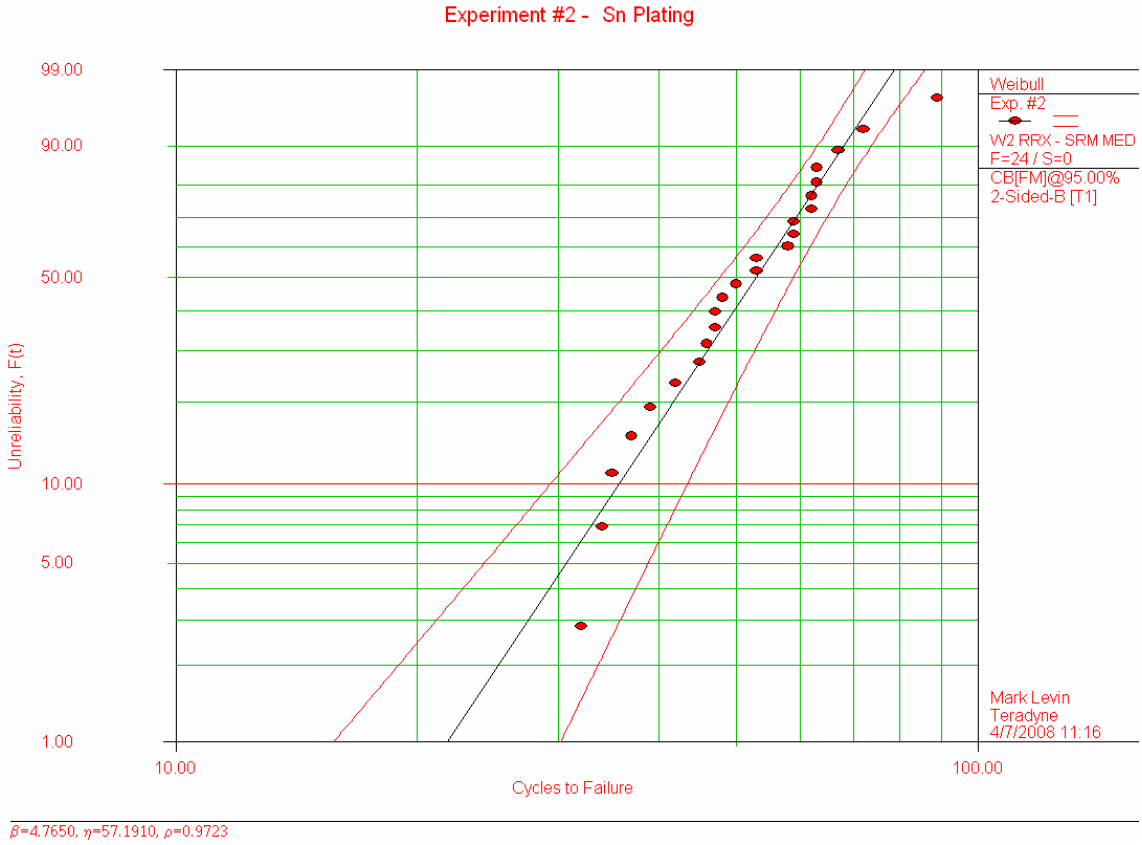


Figure 68 Tin plated lead (0 ^{o}C to 100 ^{o}C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{57.2}\right)^{4.77}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 4.77$

$\eta = 57.2$

Experiment #3: NiPdAu (nickel-palladium gold) lead plating

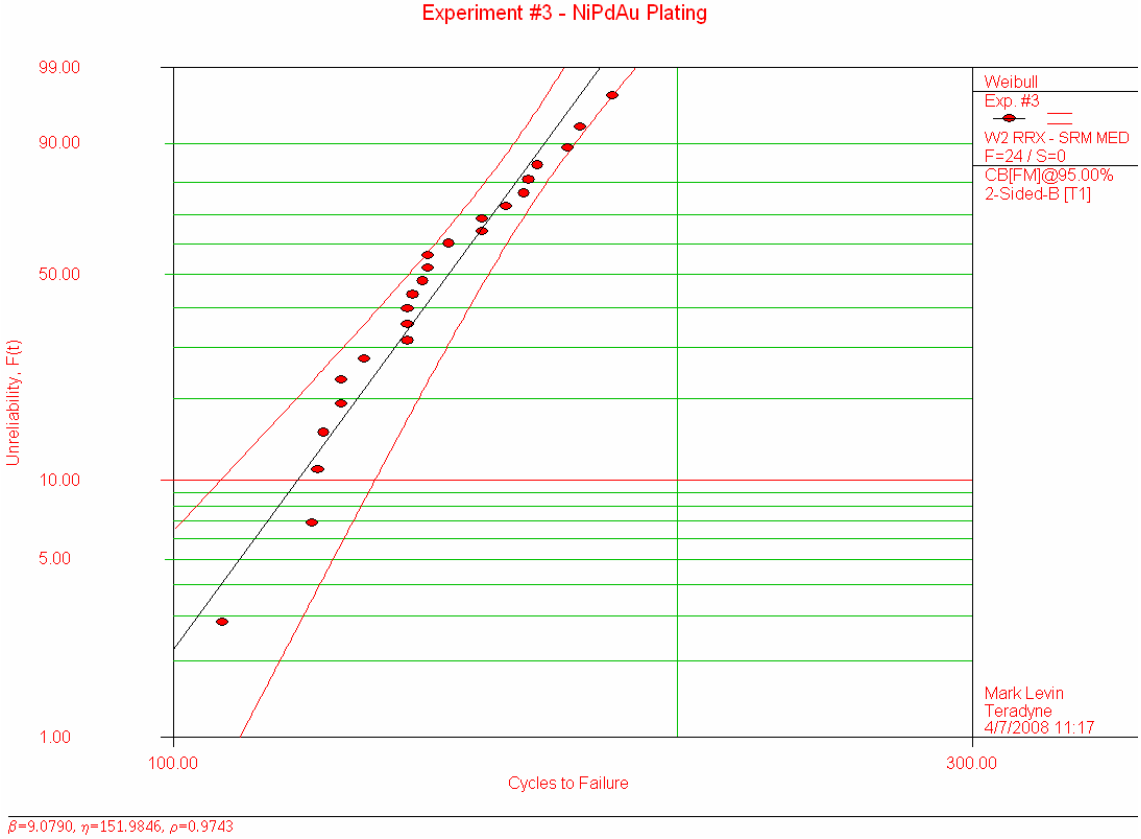


Figure 69 NiPdAu plated lead (0 ^{o}C to 100 ^{o}C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{152}\right)^{9.08}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 9.08$

$\eta = 152$

Experiment #4: NiPdAu lead plating & solder mask removed in middle area

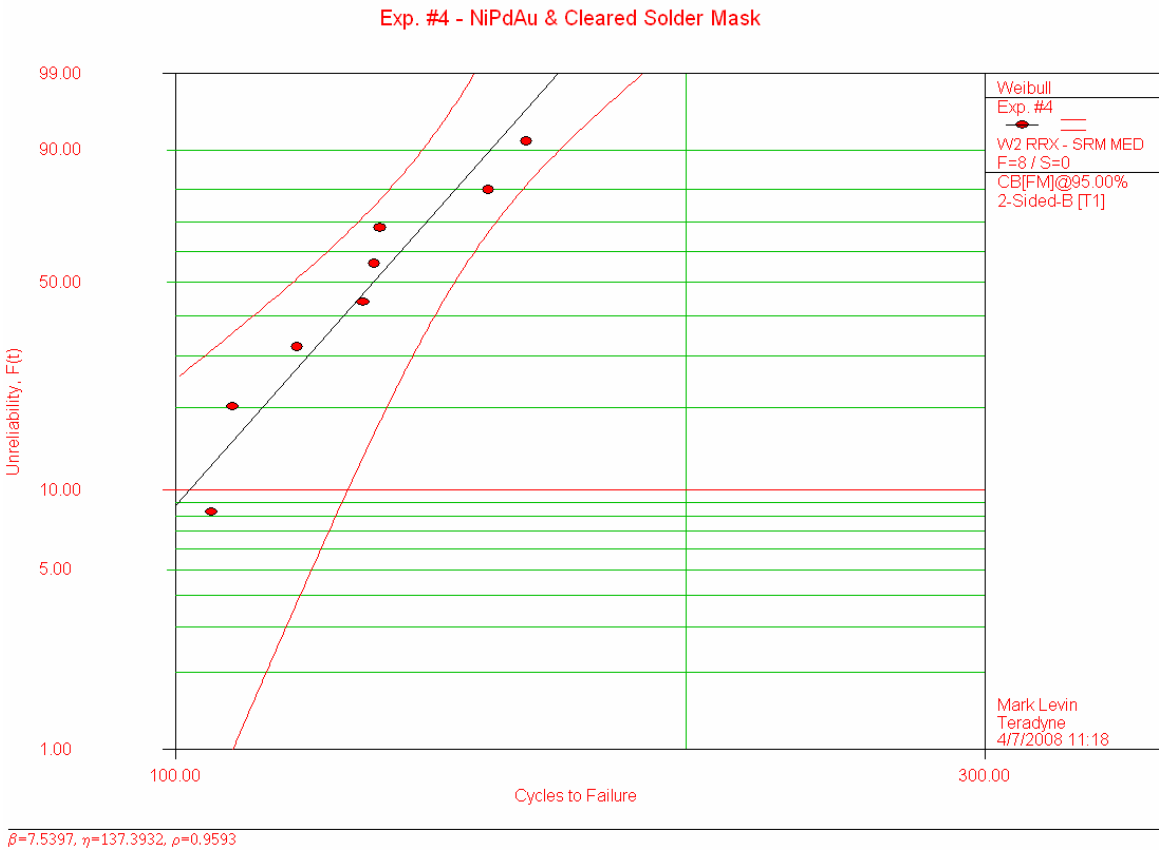


Figure 70 NiPdAu plated lead with solder mask removed underneath part (0 to 100 ^{o}C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{137.4}\right)^{7.5}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 7.54$

$\eta = 137.4$

Experiment #5: NiPdAu lead plating & new mold compound

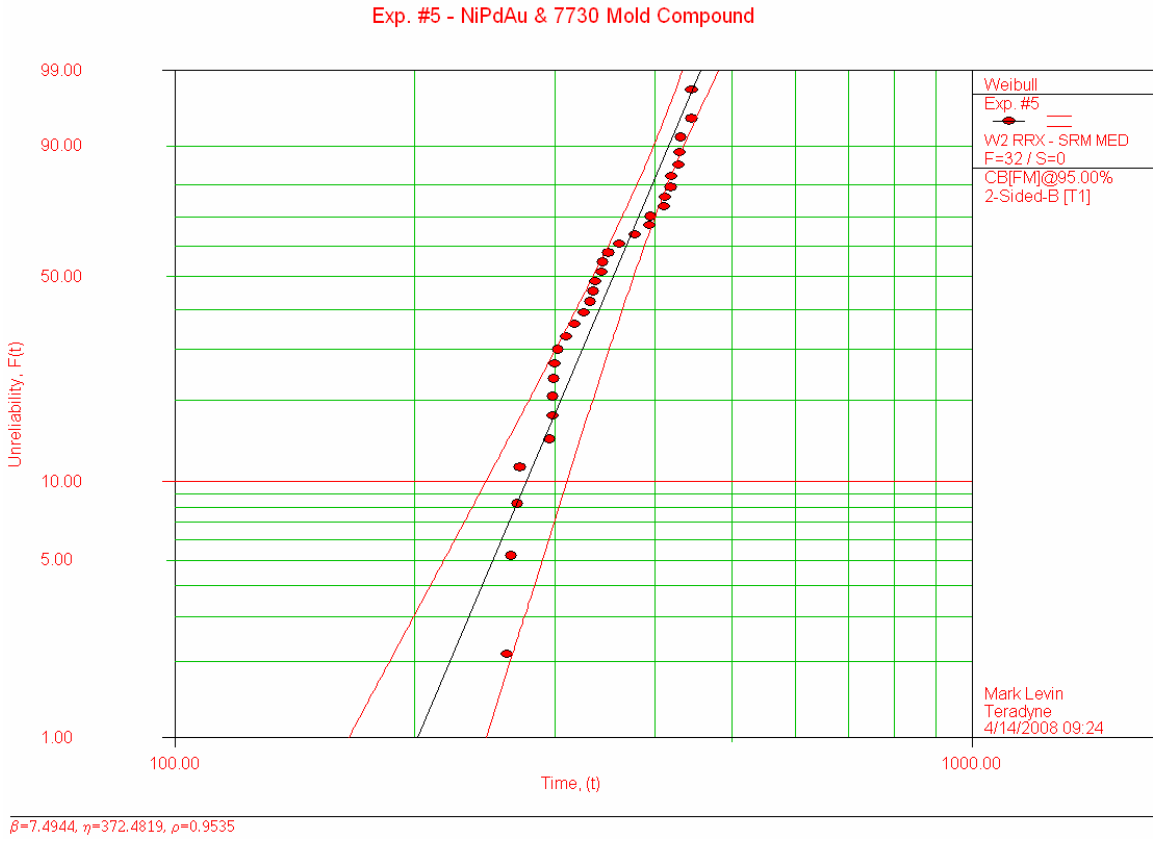


Figure 71 NiPdAu plated lead with EME-7730LF mold compound (0 to 100 ^{o}C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{372.5}\right)^{7.5}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 7.49$

$\eta = 372.5$

Experiment #6: NiPdAu lead plating & perimeter epoxy

There is no Weibull graph for experiment number six, because there were no failures after 988 thermal cycles.

Thermal cycling test results summary, thermal cycling from 0^{o}C to 100^{o}C.

Test #	Experiment description	N_f(1%)	N_f(50%)	N_f(63.2%)	β
1	Sn lead plating & no solder mask	28	69	74	4.76
2	Sn lead plating	22	53	57	4.77
3	NiPdAu lead plating	92	146	152	9.08
4	NiPdAu lead plating & no solder mask	75	131	138	7.54
5	NiPdAu lead plating & new mold compound	202	355	372	7.49
6	NiPdAu lead plating & perimeter epoxy	No failures			

Table 22 Failure rate summary using developed Weibull model: Method 2 test #1

4.4.3 Accelerate Reliability Stress Test Method #2: Test #2 (0 °C to 70 °C)

Test number two consisted of thermal cycling two test boards between 0 °C and 70 °C. The two test boards contain the following three experiments:

Experiment #7: Sn lead plating

Experiment #8: Sn lead plating with solder bump on each pad

Experiment #9: NiPdAu lead plating & new mold compound

Experiments number seven and nine are the same test run previously (Method 2: test#1) that went from 0 to 100 C. Only difference is that the test was run at a lower thermal cycling stress. Experiment number eight evaluated the reliability improvement due to a .003" to .0035" solder bump on each pad.

The thermal cycling test number two started on May 1st, 2008 and ended on May 30th, 2008 after 1002 thermal cycles. After 1002 thermal cycles experiments #7 through #8 had 100% failure of the solder joints from the QFN packages. Experiment #9 had 72% of the QFN packages with a failed solder joint. The cycles to failure were entered into Reliasoft's Weibull++ version 6 and a 2-parameter Weibull distribution was assumed. The times to failure are shown in Table 23. The table provides the thermal cycle number when it failed, the measured resistance, temperature when the failure occurred and the chain loop that failed. Only the first failure in the part was recorded. A loop failure is defined as an increase in loop resistance of 0.300 Ohms or more. The Weibull charts for experiments 7 through 9 are shown in Figure 72 through Figure 74.

Accelerate Reliability Stress Test Method #2: Test #2 (0 ^{o}C to 70 ^{o}C)

Exp # 7 Sn					Exp # 8 Sn & Solder Bump					Exp # 9 NiPdAu & 7730 Mold Compound				
Temp	Cycle #	Delta Value	U #	Chain #	Temp	Cycle #	Delta Value	U #	Chain #	Temp	Cycle #	Delta Value	U #	Chain #
0	111	0.532572	U31_08	Chain 4	0	79	0.445455	U34_40	Chain 2	0	508	0.397191	U34	Chain 5
70	112	0.426588	U34_24	Chain 1	70	288	0.437516	U29_32	Chain 1	0	634	0.378006	U34	Chain 4
70	112	0.314468	U30_08	Chain 4	0	329	0.847315	U29_40	Chain 1	70	635	0.323702	U31	Chain 4
70	127	1.76775	U31_16	Chain 4	70	338	0.422952	U31_48	Chain 5	70	665	0.544949	U29	Chain 4
70	143	0.573138	U29_16	Chain 3	70	372	0.567772	U34_48	Chain 2	70	710	0.414854	U29	Chain 4
70	144	0.689407	U34_08	Chain 4	0	378	0.321565	U31_56	Chain 5	70	730	0.581352	U29	Chain 1
0	160	0.501608	U30_24	Chain 5	0	379	0.603408	U34_32	Chain 2	0	741	0.513831	U34	Chain 4
70	163	0.824113	U31_24	Chain 3	70	387	0.643272	U30_56	Chain 1	0	752	0.949579	U29	Chain 4
70	175	0.692118	U29_00	Chain 4	0	389	0.479155	U29_56	Chain 5	70	754	0.412594	U34	Chain 2
70	182	0.3231	U29_24	Chain 4	0	394	0.372253	U30_40	Chain 5	70	757	0.405724	U34	Chain 4
70	183	0.485916	U30_00	Chain 3	70	414	2.177864	U31_40	Chain 2	70	761	0.469538	U30	Chain 4
0	196	0.487097	U29_08	Chain 4	70	439	0.485766	U30_48	Chain 1	70	771	0.344396	U34	Chain 4
70	209	0.342893	U34_16	Chain 3	70	441	0.362536	U29_48	Chain 1	0	782	0.520193	U31	Chain 3
70	218	0.614476	U31_00	Chain 3	70	465	0.407379	U34_56	Chain 2	70	796	0.340176	U34	Chain 4
70	228	0.37707	U30_16	Chain 4	0	493	0.503772	U31_32	Chain 4	0	798	0.481464	U30	Chain 2
70	259	0.488843	U34_00	Chain 4	0	495	0.543957	U30_32	Chain 5	70	818	0.427184	U30	Chain 4
										70	823	0.50981	U29	Chain 1
										0	824	0.712695	U31	Chain 4
										70	833	0.334075	U29	Chain 1
										0	834	0.470256	U31	Chain 4
										0	910	0.760083	U29	Chain 4
										0	914	0.552494	U30	Chain 4
										0	988	0.318933	U34	Chain 4
Total Failing Devices				16	Total Failing Devices				16	Total Failing Devices				23
Total Devices				16	Total Devices				16	Total Devices				32
Suspensions				0	Suspensions				0	Suspensions				9
% Surviving				0%	% Surviving				0%	% Surviving				28%
% failing				100%	% failing				100%	% failing				72%
Total Cycles				1,002	Total Cycles				1,002	Total Cycles				1,002

Table 23 Failure data from thermal cycling

Experiment #7: Sn lead plating

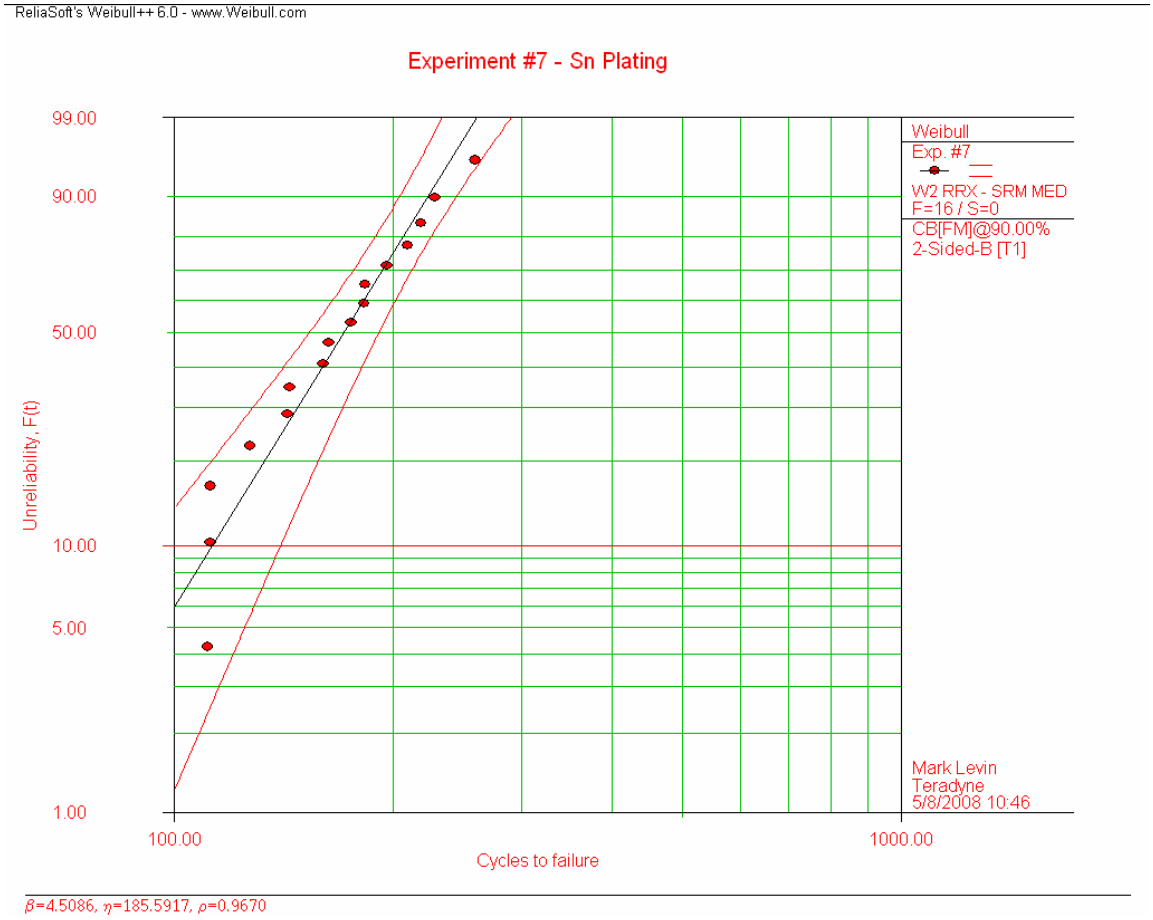


Figure 72 Tin plated lead (0 °C to 70 °C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{185.6}\right)^{4.5}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 4.51$

$\eta = 185.6$

Experiment #8: Sn lead plating with solder bump on each pad

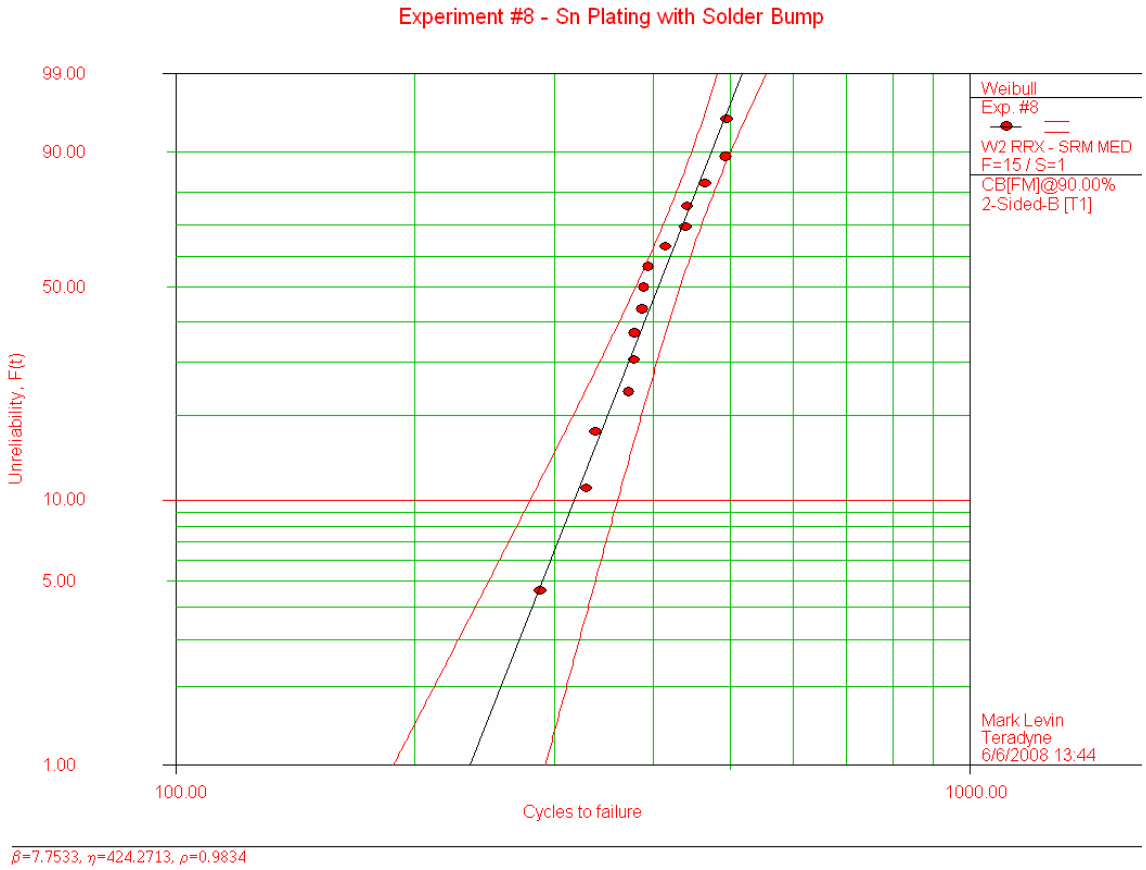


Figure 73 Tin plated lead with solder bump (0 ^{o}C to 70 ^{o}C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{424.3}\right)^{7.8}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 7.75$

$\eta = 424.3$

Experiment #9: NiPdAu lead plating & new mold compound

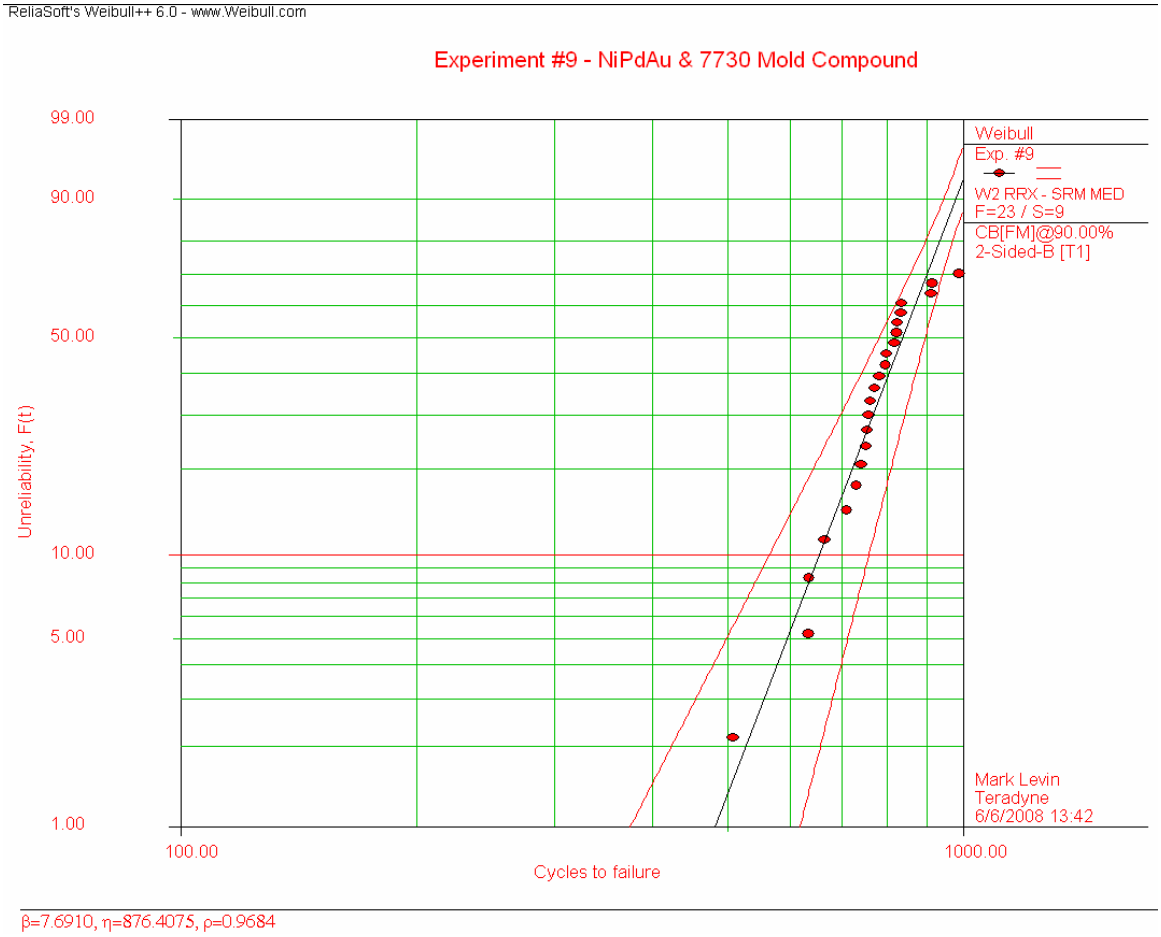


Figure 74 NiPdAu plated lead with EME-7730LF Mold Compound (0 ^{o}C to 70 ^{o}C)

The reliability function is:

$$R(T) = e^{-\left(\frac{T}{\eta}\right)^{\beta}} = e^{-\left(\frac{T}{876.4}\right)^{7.7}}$$

Where the values for β and η are determined from the ReliaSoft chart.

$\beta = 7.69$

$\eta = 876.4$

Thermal cycling test results summary, thermal cycling from 0^{o}C to 70^{o}C.

Test #	Experiment description	N_f(1%)	N_f(50%)	N_f(63.2%)	β
7	Sn lead plating & no solder mask	28	69	74	4.76
8	Sn lead plating	22	53	57	4.77
9	NiPdAu lead plating	92	146	152	9.08

Table 24 Failure rate summary using developed Weibull model: Method 2 test #2

4.4.4 Accelerated Reliability life model for Daisy-chained QFN's

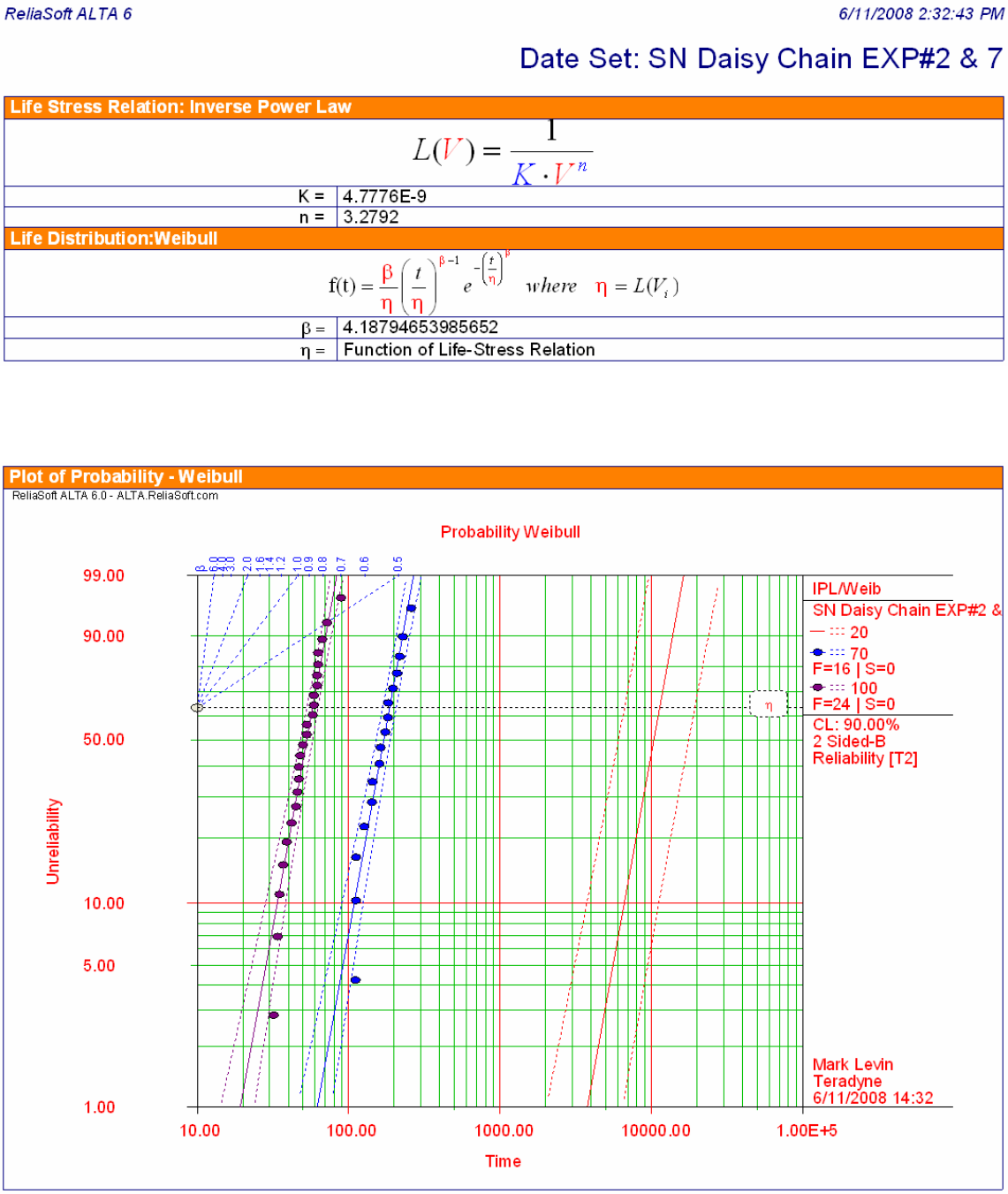


Figure 75 Reliasoft Alta 6.0 parameters IPL-Weibull model

Chapter 5: Sources of Errors

5.1 Contributing Sources of Uncertainty

There are several factors that contribute to the uncertainty in the accelerated life testing analysis and modeling. Method one life test has three relevant sources of uncertainty, they are:

1) A single point failure is due to a different mechanism (i.e. not a solder fracture).
2) Internal self heating of the QFN causes the temperature at the body to be different than the HALT chamber set point.
3) Coldplate attachment normal force

Three assumptions made to the reliability model also contribute to uncertainty, they are:
4) QFN package body treated as a single element with the CTE assumed to be entirely made up of the mold compound. The effective package CTE should include the influence the die, lead frame and paddle have on the CTE for the package.
5) Solder-joint lead attach is assumed to be ideal and does not take into account variability due to manufacturing.

6) Any intrinsic preloaded stress the package has after soldering to the circuit board. Any package warpage would result in additional normal force that will accelerate crack initiation and propagation.

Each of the contributing sources of error is considered below:

1) A failure occurs that is associated with a different failure mode other than solder-joint fatigue at the solder connection. The dominat failure mode is low-cycle fatigue failure due to thermal cycling and high strain from CTE mismatch and solder creep. Cross sections of failed components confirmed this as the dominant failure mode. However, there could be other failure mechanisms that arise and are assumed to be due to a solder-joint fatigue failure. This source of error in failure recording is more likely to occur in test method number one. One reason for this is that test method number one uses working production material. In this case, it is a QFN package for a complex ASIC fully tested as good prior to stress testing. Thermal cycling the ASIC while powered on and operational can cause failures internal to the package. It is possible for the QFN to have an internal package failure which is not the result of a cracked solder joint. The most likely internal package failures are a broken or cracked wire bond, delamination between the die and paddle causing overstress, and a wafer level defect failure.

To minimize this uncertainty, diagnostic software (checkers) was developed to continuously test the ASIC functionally. The checkers does not test every cell in the chip

but it can fully test its functionality. The failure data from thermal cycling was reviewed to verify that the failure signatures were consistent with a degrading or completely cracked solder joint. If other failures mechanism did occur, those failures would be removed from the data set by changing it to a censored data point. However, each failure was not cross sectioned to verify that the presence of a fractured solder joint. The cost to cross section every failure would have made the test too costly. There are also 32 QFN packages on each test board, cross sectioning a device once it fails would destroy the test board and prevent continuing with the thermal cycling test. Upon completion of the thermal cycling test, the solder connections on the QFN package were inspected for a solder fracture signature.

Several other non-destructive inspection methods were explored to see if they could detect the presence of a solder fractures. The inspection methods were X-ray and acoustic scanning microscope. Both methods were determined to be ineffective at identifying the existence of a solder crack. The sonic scan was unable to adequately penetrate through the board (thickness is 0.125") and the components on the bottom side. The x-ray could not get the right angle to view cracking because of it large size, the board is 16 inches by 20 inches.

2) A second source of error is due to internal heating of the powered on and operational QFN ASIC. The QFN ASIC generates 5 watts of internal power at the die level. This raises the top-side paddle temperature to 38^{o}C from ambient (20^{o}C). The junction

temperature of the die is at 77^{o}C (bulk die temperature is between 52^{o}C and 57^{o}C). The internal heat generated by the die causes the package temperature to increase and this temperature adds to the chamber temperature. For example, setting the thermal chamber temperature to cycle between 0^{o}C and 70^{o}C will result in top-side of the paddle to swing between 35^{o}C and 105^{o}C. The error due to internal heating is less than this because the package temperature of interest that is relevant to causing a solder crack is the temperature at the bottom of the package. To determine the temperature at the bottom of the device, the ratio of the heat dissipation between the top and the bottom of the device is needed. Based on input from the thermal design engineer, 90% to 95% of the power dissipates through the top of the device leaving only 5% to 10% dissipating through the bottom and sides. The high thermal efficiency is the result of silicon die thermally bonded with silver epoxy to the back side of the thermal paddle. This creates a very efficient thermal path from the die to the thermal slug on the top side. The top-side of the paddle is connected to a cold plate through a thermal interface material (TIM). Therefore, there is very good thermal efficiency between the regulating Coldplate and the silicon die. In contrast, the epoxy mold compound has very poor thermal conducting properties. An estimate of the heat at the bottom of the package can be determined by considering the die to be a uniform thermal radiator and determining the heat increase on the bottom-side of the package due to internal heating (figure 37). The increase in body temperature at the bottom of the package due to internal heating is 2.46^{o}C.

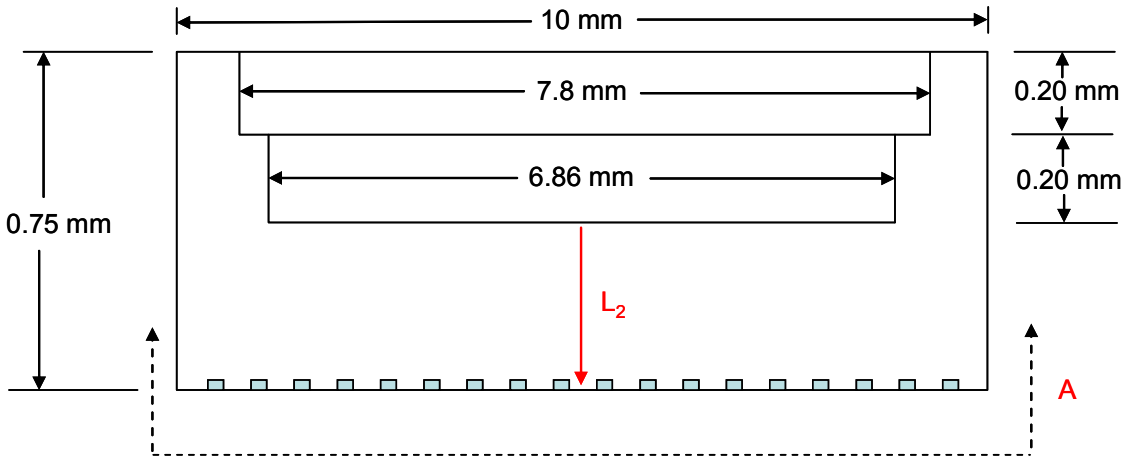


Figure 76 Cross section of QFN assembly

$$\Delta T = \frac{(P_a)(L_2)}{(K)(A)}$$

$$P = 5 \text{ watts}$$

$$P_a = (P)(10\%) = (5 \text{ watts})(.1) = 0.5 \text{ Watts}$$

$$\text{K} = 100\text{x}10^{-2}\left(\frac{W}{m \cdot C}\right)$$

$$\text{L}_2 = (0.75 - 0.2 - 0.2) = 0.35 \times 10^{-3} m$$

$$A = \left(\frac{10 \times 10^{-3} m + 6.86 \times 10^{-3} m}{2}\right)^2 = 71.065 \times 10^{-6} m^2$$

$$\Delta T = \frac{(0.5 \text{ Watts})(0.35 \times 10^{-3} m)}{\left(100\text{x}10^{-2} \frac{W}{m \cdot C}\right)(71.065 \times 10^{-6} m^2)} = 2.46 \text{ C}$$

3) Test method number used a liquid coldplate that is attached to the printed circuit board. The QFN package is sandwiched between the colplate and the printed circuit board. The coldplate has a lower thermal resistance and provides a faster thermal transfer of energy from the thermal chamber to the component. The coldplate also provides a compressive normal force on the component. The compressive force will increase the time it takes for crack initiation to occur and slow down the crack propagation rate.

4) The QFN model for the package assumed it to be composed entirely of the epoxy mold compound. However, the QFN package structure is more complex than that. There is a lead frame (CTE =16.7PPM), silicon die (CTE =3PPM), internal gold wire bonds (CTE =14PPM), silver epoxy (CTE =19PPM) that bonds the die to the lead frame and tin plating over the C194 lead frame (Table 25). All these factors influence the effective CTE of the package and require finite element modeling to evaluate. However, the models presented in this paper do not take these factors into account.

AT23/MAX9979 68L 10x10TQFN Packaging material CTE

MATERIAL	COEFFICIENT OF THERMAL EXPANSION (CTE, um/m/°C, or ppm/°C;)
Lead frame (C194)	16.7
Die attach (Ablebond 8200T)	61 (below Tg), 195 (above Tg), Tg: 83 'C
Mold compound (Sumitomo G770HCD)	7 (below Tg), 34 (above Tg), Tg: 135'C
Silicon die	3
Gold wire	14
Tin (Sn)	20.0
Silver (Ag)	19.0
BCB (Benzocyclobutene, spin on Die Coating)	40-50

Table 25 CTE values for the components making up the QFN

5) Another source of error is from the circuit board manufacturing process which introduces variability in the quality of the solder joints (solder height and wetted surface area). There are two reasons for this uncertainty. First, the QFN device has a lead frame with nickel-palladium-gold finish. However, after QFN manufacturing, mold flash was discovered on the leads. To fix the problem, the manufacturer applied a buffing process

to remove the flash mold material from the lead. The process also removed the nickel-palladium-gold finish. To correct for the removal of the lead plating finish, the manufacturer added a tin plating process making the lead tin plated and not nickel-palladium gold. It is believed that the buffing and re-plating process may have left a residue on the lead that could reduce the solder wetting surface area or create an undesired interface surface. No EDS testing was performed to determine the presence of contamination and X-rays of the soldered surface did not show significant voiding.

A second variable for solder-joint quality is the circuit board manufacturing assembly process. The percent of the wetted surface area between the lead and the pad plays a critical role in solder-joint life. Poor wetting reduces the surface area under the lead that shares the shear load. Reducing the soldered cross sectional area reduces the strength of the termination and reduces the cycle time for crack propagation to become a failure. With a leadless connection, the solder-joint is not visually inspectable. Therefore, techniques like x-ray and acoustic scan are required. Unfortunately, both of these have limitations[22]. Acoustic scan which can detect air gaps did not to penetrate well from the bottom-side to provide an adequate picture. Automated x-ray can show areas of voiding but is susceptible to false failures. The parts were all x-rayed, looking for gross defect like solder bridging and opens. However, a small amount of voiding can influence solder-joint life.

6) Cross-sections of the failed solder connections after thermal cycling showed a large separation in height between the QFN lead and the circuit board. Normally, the separation in height of a failed solder connection due CTE mismatch is small; this is because the force causing failure is sheer. The presence of a large separation in height suggests that there is a normal force contributing to failure. A normal force, if present, will accelerate crack propagation. The contribution of a normal force to fatigue failure is not part of the classical reliability models presented earlier. The source of the normal force, if present, could come from either the QFN package or the circuit board not being flat. The warpage spec for the circuit board is 0.1%. Using the circuit board warpage spec, the worst case warpage under the QFN package can be estimated. For a 10 mm (0.393") square QFN package, the diagonal distance across the package is 0.556".

$$\text{Distance across the diagonal of the package} = (0.393")\sqrt{2} = 0.5558"$$

The worst case warpage is a single node concave or a convex structure. The maximum warpage is measured from neutral point which is the center of package to the farthest corner. Therefore, the maximum distance from the neutral point is 0.2279 inches. If the worst case warpage is 0.1%, then the maximum height due to warpage is 2.78×10^{-4} inches. This maximum height separation due to board warpage is small and not considered a significant factor. Typically, board warpage becomes a factor when the separation in height is 0.001 inch or greater.

The other potential contributor to a normal force at the solder connection is from the QFN package. The thermal model for the QFN package body assumed it to be uniformly made up of a mold compound. However, there is a paddle, die and lead frame that influence the effective CTE of the package and cause residual stress. Stress is created when the components that make up the package body cool at different rates and there is significant CTE mismatch (Figure 77).

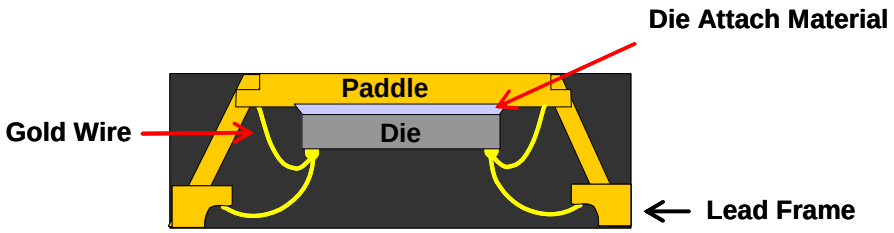


Figure 77 QFN package with topside paddle

The lead frame goes around the perimeter of the package and has four cross beam structures that connect to the top and bottom of the package. The lead frame attaches the leads at the bottom perimeter to the top of thermal paddle. The lead frame is a stamped metal part that has four diagonal bars in the corners that support the paddle and die during molding and keeps the lead frame to the package centered. The copper lead frame has a CTE of 16.7 PPM which matches close to the PCB but is over twice the CTE of the mold compound. A significant CTE mismatch can result in a preloaded stress in the package. A preloaded stress can form from the molding process, which introduces heat to the QFN package during forming. As the package cools, the internal elements cool at different

rates than the mold compound. This is possible because the thermal capacity of the paddle and lead frame is significantly greater than thermal capacity of the plastic mold the compound. The CTE and thermal capacity differences in the package create residual stress in the package after it has cooled. The residual stress affects the flatness of the QFN package which can be measured using a shadow moiré test.

To evaluate QFN package warpage with top-side paddle, three parts were sent to AkroMetrix TherMoiré for a shadow moiré test. A baseline measurement was made on each part to determine component flatness. The modules measured for baseline were not subjected to any preconditioning or pre-baked. The measurements were made on unmounted QFN packages placed on their back with the paddle facing down. This is analogous to placing the QFN with its leads facing up. The baseline measurements will show if there is any warpage in the QFN package indicating the presence of a preloaded stress. The baseline measurements were made at an ambient temperature of 23°C.

After the baseline measurements were made, each part went through a slow temperature ramp up to the peak reflow temperature for eutectic solder (Figure 78). The temperature profile started at 23°C and slowly ramped to 220°C and then back to ambient. A shadow moiré measurement was made every 10°C during the temperature ramp to 220°C and back to ambient. The shadow moiré measurements will show if there are internal strains taking place during solder reflow and provides a graphic three dimensional image of the package flatness. The pictorial view shows the QFN looking from the bottom-side up. It

is like flipping the part on its back and viewing it looking down into the bottom-side of the QFN. The shadow moiré test will also provide an indication if these forces are present in the controlled thermal cycling tests.

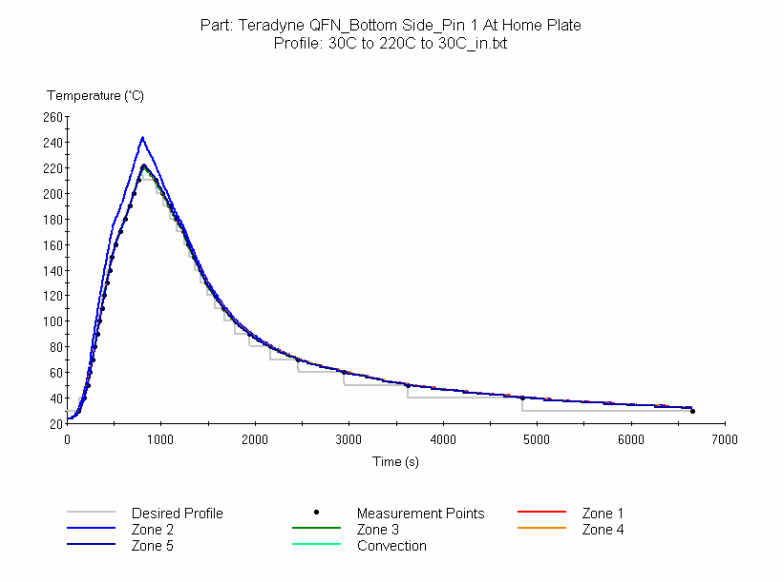


Figure 78 Solder reflow profile for shadow moiré test

The results of the baseline shadow moiré test at room temperature indicated there is an internal residual stress causing the package to warp in the corners. The amount the package is warped is shown in Figure 79. Examination of the raw QFN package before soldering showed there is residual stress built in the package. The view looking up from the bottom of the package (paddle side) showed the center paddle to be low and the corner leads curved up (away from the board) about 2.8 mils above center paddle.

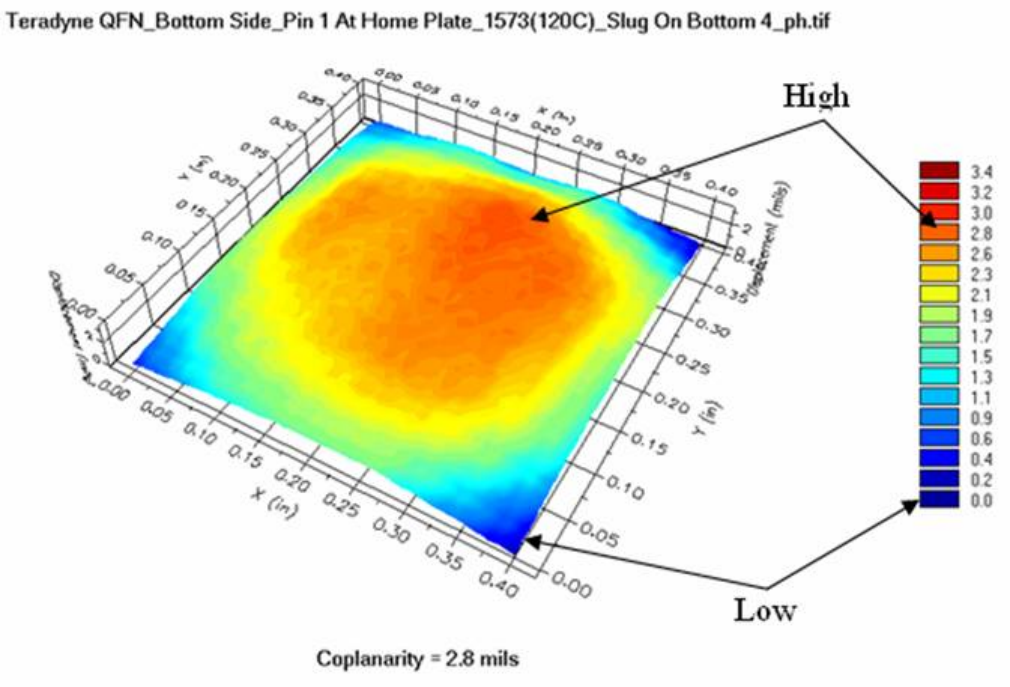


Figure 79 Expanded view of Shadow Moire of QFN package at room temperature

The package warpage may be the result of an internal residual stress created during the transfer molding and singulation process. During transfer molding, heat is generated in the package from the temperature of the injection mold compound. During the cooling process, the internal metal structures cool at a different rate than the mold compound. If the mold compound cools quickly and the lead frame continues slowly, then residual stress develops due to the significant differences in thermal shrinkage rates[23],[24]. This could explain why the package is warped at room temperature.

The results from the shadow moiré temperature cycle test for the three QFN packages exposed to a solder reflow profile is illustrated in figure's Figure 80. The dark red areas

are high points and the dark blue areas are low point. A blue dark color represents a flat plane. All three QFN packages had some degree of internal residual stress at the beginning of the test. The residual stress decreased with increasing temperature and almost completely relaxed above 160°C. However, the residual stress returned when the device cooled back to ambient temperature. There was a reduction in the amount of residual stress after going through a solder reflow profile and returning to ambient temperature. As the device cooled from reflow temperature back to ambient, there are two temperature ranges where the device experiences an increase in residual stress. The first increase in internal stress is between 160°C and 150°C. The peak being about 150°C where there are 2.1 mils of warp at the corners. All three devices tested had an increase in residual stress within this temperature range. As you approach the glass transition of the epoxy mold (138°C) the internal stress relaxes. The second increase in residual stress is around 120°C. At 120°C, the QFN wants to curl up at the corners and how the middle body section wants to push into the circuit board. The two factors work together to cause a normal "pulling" force on the leads. This force acts to pull the corner leads up and away from the circuit board.

The increase in residual stress was more significant in two of the three devices tested. The third QFN showed a modest increase in residual stress within in this temperature range.

The shadow moiré tests showed there was a significant difference in the amount of residual stress between the three parts before and after. QFN number two showed the

greatest amount of residual stress. This QFN had significantly greater residual stress variation during cool down and was the only device of the three to have significant residual stress in the temperature range of 40°C to 30°C.

After the thermal cycling test, the built in residual stress still existed in all three QFN's but at a lower level. The residual stress is at the corners of the package that wants to pull the corner leads up from the board. The residual tensile stress in the package likely accounts for the large separation gap in the fractured solder connection. The residual force will also accelerate crack initiation and crack propagation if the package is thermal cycled.

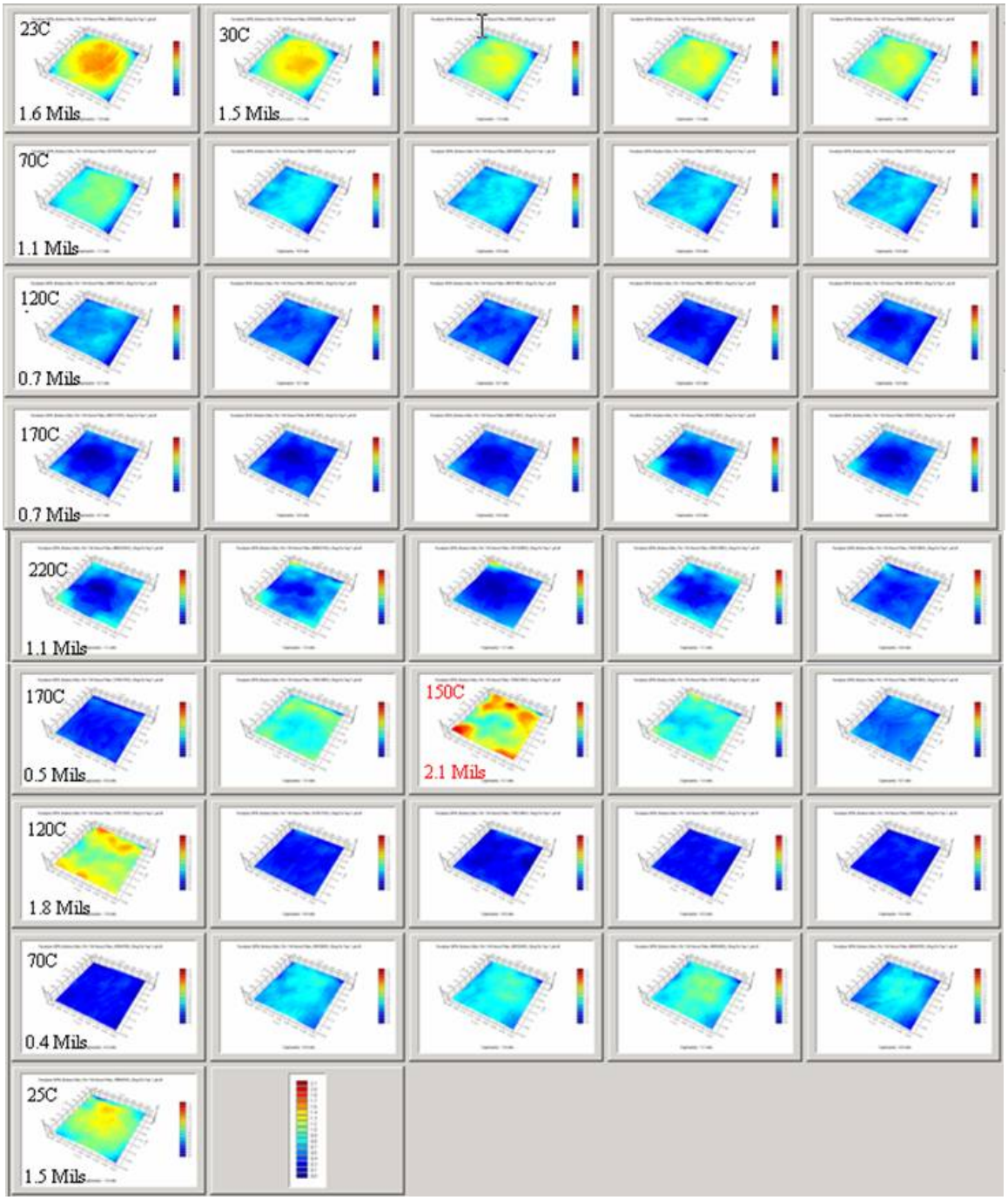


Figure 80 Shadow Moire of QFN package as it goes from solder reflow to room temperature

Chapter 6: Conclusions

6.1 Summary Conclusions

A reliability study was performed on a 10mm QFN package that has a top-side paddle. The standard QFN package has a bottom-side paddle, which is soldered to the printed circuit board. The paddle removes heat from the device through the circuit board via the soldered connection. The soldered paddle connection shares the stress load that results from a change in temperature due to the CTE mismatch between the QFN package and the printed circuit board. Moving the paddle to the top side, allows greater heat removal from the device but 80% of the soldered surface area for the QFN package is removed. For a large 10mm QFN package the shear stress load induced in the solder-joint is significant. A global strain greater than 1% results from an 11.5^{o}C increase in ambient temperature. This research investigated the effect the reduced solder surface area has on solder-joint reliability due to the CTE mismatch and thermal cycling.

Four methods for modeling solder-joint reliability of a leadless 10mm QFN package soldered to an epoxy fiberglass circuit board were used. The reliability models provided estimates for solder-joint reliability due to thermal cycling. The solder used to attach the QFN package to the circuit board was eutectic Sn63/Pb37. The four methods for modeling solder-joint reliability are:

Engelmaier Model for a leadless surface-mount device

Steinberg Model for a leadless surface-mount device

Published industry data for unsoldered bottom-side paddle

SRS 1.1 software by Jean-Paul Clech

The Engelmaier model for a leadless device calculated the maximum strain energy induced on the solder-joint due to a change in temperature. The maximum strain energy was entered into a plastic strain-fatigue life relationship model to determine the mean useful life of the solder joint. The second prediction method used a Steinberg model for a leadless perimeter array package. The Steinberg model balances the forces that result due to a change in temperature. The force balance model determines the maximum stress that results in the solder-joint due to a change in temperature. The maximum force was then applied to a log-log S-N fatigue curve to determine the mean life. The third analysis method used published reliability data for a QFN package with bottom-side paddle to estimate the reliability of a QFN package paddle up. Using published reliability data, scaling factors for mold compound, circuit board thickness and lead type were made. The model also assumed that the bottom-side paddle was not soldered to the circuit board. The last analysis used an SRS software program by Jean-Paul Clech for a leadless package. The SRS software program is based on published reliably tests for a leadless device. The software model uses details about the QFN package, circuit board and solder type to determine the global and local strain energy due to temperature cycling. The

maximum strain energy is then used to determine solder-joint reliability in a method similar to the Engelmaier model. The main difference is that the Clech model uses it own derived constants for strain fatigue relationship model. The results from the four modeling methods are shown in tables below:

Comparison of experiment and modeling results (Thermal cycling = 0°C to 100 °C)	CDF (cycles to failure)		
	1%	50%	63.2%
Modeling Results			
Engelmaier model for LCCC	29	78	84
Steinberg	68	197	216
Amkor published Data	111	179	186
Clech SRS software model	56	87	93

(Thermal Cycling = 0°C to70°C)	CDF (cycles to failure)		
	1%	50%	63.2%
Modeling Results			
Engelmaier model for LCCC	52	149	162
Steinberg	141	422	462
Apply industry published papers (Amkor Data)	172	267	285
SRS software model	117	193	202

Table 26 Summary of reliability models for solder-joint reliability

The results from reliability prediction modeling showed that all four methods for predicting solder-joint fatigue life of a LCCC package provided results within a factor of less than 3X. The Engelmaier model and Clech software program provided results that were similar, both approaches used a similar model with different constant values. All four prediction methods indicated that failures would occur early in the accelerated stress test. The models also show the two strongest factors affecting solder-joint life are lead compliance in the form of solder-joint height and CTE mismatch between the package and circuit board.

Two methods for accelerated stress testing were performed to determine solder-joint reliability of a 68 pin leadless QFN package with top-side paddle. The two tests methods were:

Method #1: Used a functional instrument with 10mm QFN packages attached. The functional instrument had a liquid-cooled coldplate that mated to the QFN ASIC through a thermal interface material. The QFN packaged ASIC was biased and operational during the thermal cycling tests. The functional instrument used developed software checkers that continuously looped on the QFN ASIC device to monitor functionality.
Method #2: The second method used a more traditional of approach of designing a daisy-chained test board with daisy-chained dummy QFN packages and no coldplate. The QFN dummy package was manufactured by the same supplier as the QFN ASIC package. The

dummy parts had non functional die attached that came from wafer level rejects of the QFN ASIC.

The test boards for method #1 and method #2 were the same in respect to circuit board size, layer stack up and copper density. Each accelerated test consisted of thermal cycling between two different stress levels. The higher temperature delta stress test was done at either -25^{o}C to 70^{o}C or 0^{o}C to 100^{o}C. The thermal cycling test for method #1 was performed at -25^{o}C to 70^{o}C which is the maximum stress range the instrument will run reliably with diagnostic checkers looping. The daisy-chained test was thermal cycled from 0^{o}C to 100^{o}C. The temperature delta stress test was done at 0^{o}C to 70^{o}C for both test methods.

Results from accelerated reliability testing method number one which had Sn-plated leads performed fractionally better than the QFN dummy packages with similar lead plating. The improvement is likely due to the coldplate attachment. The coldplate provided a small normal force on the package that worked to slow both crack initiation and crack propagation. The normal force from the coldplate countered the package warpage due to internal residual stress. QFN package had a (instrument level with functional ASICs) performed somewhere between the performance of the Sn-plated and NiPdAu-plated daisy-chained parts. The colplate improved solder-joint reliability of the QFN package about 2.3X.

The results from thermal cycling tests showed good correlation to the models developed to predict solder-joint reliability. The QFN with tin (Sn) plated leads failed significantly earlier than any of the other tests. It was learned from the manufacturer that that there is a buffing process that takes place before Sn plating. After buffing, there is a cleaning process to remove debris and contamination on the leads. It is possible that the cleaning process left residue that resulted in a reduced solder-joint life. No testing was performed to verify the presence of residue. The nickel-palladium-gold (NiPdAu) leads provided 2.1X improvement in solder-joint reliability. Adding a .0025" solder bump to the bottom of the lead provided 2.3X reliability improvement. The higher CTE mold compound with a NiPdAu lead part provided 5X improvement. Thus, a higher CTE mold compound with solder bumps should provide about 11.5X improvement in reliability. Removing the solder mask underneath the QFN had a small and inconclusive effect on solder-joint reliability. Finally, the value assumed for beta that was used in the Engelmaier and Steinberg model was 4.0. This turned out to be low by a factor of about 2X. A summary of the test results acceleration factors is shown in Table 27.

Variable	Reference	Change	Multiplier
Temp. Cylce	0<>100C	20<>40C, 2 cycles/hr	62.4
Temp. Cylce	0<>70C	20<>40C, 2 cycles/hr	24.9
Lead Plating	Sn	NiPdAu	2.1
Mold Compound*	G770	EME-7730LF (New)	5.0
Solder Bump	None	Add .0025" solder bump	2.3

Table 27 Scale factors based on thermal cycling test results

Comparison of experiment and modeling results (Thermal cycling = 0 °C to 100 °C)	CDF (cycles to failure)		
	1%	50%	63.2%
Modeling Results			
Engelmaier model for LCCC	29	78	84
Steinberg	66	166	206
Amkor published Data	111	179	186
Clech SRS software model	56	87	93
Accelerated Life testing results			
Method #1 Instrument level life test with functional QFNs	72	116	120
Tin plated lead	28	69	74
Tin plated lead with solder mask removal underneath QFN	22	53	57
NiPdAu lead	92	146	152
NiPdAu lead with solder mask removal underneath QFN	75	131	137
NiPdAu lead with new mold compound	202	355	371

Comparison of experiment and modeling results (Thermal cycling = 0°C to 70°C)	CDF (cycles to failure)		
	1%	50%	63.2%
Modeling Results			
Engelmaier model for LCCC	52	149	162
Steinberg	141	405	441
Apply industry published papers (Amkor Data)	172	267	285
SRS software model	117	193	202
Accelerated Life testing results			
Method #1 Instrument level life test with functional QFNs	137	221	229
Tin plated lead	67	171	185
Tin plated lead with solder bump	234	405	423
NiPdAu lead with new mold compound	482	836	876

Estimated solder-joint reliability for use condition (Thermal cycling = 20 °C to 40 °C)	CDF (cycles to failure)			
	1%	50%	63.2%	AF*
Engelmaier model for LCCC		3,317		
Steinberg		9,278		
SRS software model	7,420	11,590	12,040	
Method #1 Instrument level life test with functional QFNs	1,339	2,152	2,242	9.7
Tin plated lead	1,747	1,932	2,072	60.8
NiPdAu lead	5,741	9,110	9,485	
NiPdAu lead with new mold compound	12,605	22,152	23,150	24.9
NiPdAu lead with new mold compound and solder bump	25,222	50,455	53,572	

Table 28 Summary of results from accelerated testing and modeling

* Acceleration factor (AF) is based on ΔT=70C stress and ΔT=20C use condition.

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