INTRODUCING THE CONCEPT OF DESIGN REUSE INTO UNDERGRADUATE DIGITAL DESIGN CURRICULUM

Gang Qu

Electrical and Computer Engineering Department and Institute for Advanced Computer Studies
University of Maryland, College Park, MD 20742
gangqu@eng.umd.edu

ABSTRACT

Intellectual property (IP) reuse based system design is becoming an industry standard recently. However, current educational system is not effective in the training of engineers who design by reuse and design for reuse. In this paper, we report our experience at the University of Maryland at College Park (UMCP) in introducing the concept of design reuse into the introductory digital logic design course. We present a practical curriculum innovation plan, which does not increase the teaching load or sacrifices the current curriculum significantly, to implement this idea. Our teaching experience show that students learn the basics of design reuse and enjoy doing IP-based design.

1. INTRODUCTION

Despite the recent boom in reuse-based system design methodology, there is currently a severe national shortage of engineers who actually do design for reuse. One reason is that effective and systematic design for reuse is expensive. Design teams in Synopsys and Mentor Graphics estimate that developing an IP block for reuse takes 2-3 times the effort of designing the same block for single use[2]. Another reason is that the concept of design reuse has not been integrated into the undergraduate curriculum of the existing education system yet.

In recent years, significant efforts have been made to improve this situation. Several business organizations, such as the Virtual Socket Interface Alliance (VSIA)[5], have been persistently pushing for IP-based design standards. In academia, curriculum innovation has also been proposed to focus on the training of IP creators and integrators[1]. However, to the best of our knowledge, there is no reported efforts on teaching design reuse at entry-level design courses.

At the University of Maryland at College Park (UMCP), we have experimented teaching the basic concepts of design resue at introductory level logic design course and we are currently planning a revision of the senior Capstone design courses to facilitate design reuse. Our goal is to train college engineering students to become next generation design reuse oriented engineers.

2. BACKGROUND

The Department of Electrical and Computer Engineering (ECE) in UMCP established the Computer Engineering program in 1996 and the university has made a strong commitment to make it one of the top programs in the nation. Integrating the most up-to-date technology into existing curriculum is on the program's roadmap for excellence. Over the years, we have built a comprehensive program to train engineering students to be system designers. After taking courses on "Basic Circuit Theory" (ENEE 204) and "Digital Logic Design" (ENEE 244), sophomore/junior students will enter the " Fundamental Electric and Digital Circuit Laboratory" (ENEE 206), where they learn the basic skills for electrical laboratories. Then, they have the opportunity to analyze, design and construct electronic circuits (both digital and analog) at transistor and integrated circuit levels (ENEE 302, 306). In their senior year, students can gain hand-on design experience by taking one of the "Capstone Design Project/Course" (ENEE 408A-F). Detailed course description can be found at the department webpage[4]. The concepts of IP-based design should be introduced to students as early as possible.

The sophomore-level "Digital Logic Design" course is where students learn the basics on circuits design and analysis. Traditional undergraduate education emphasizes on design principles, particularly on design from scratch. That is, how to design system from its high level specification using basic logical gates and flip-flops. Such training remains as one of the most important skills a college engineering student should have. However, we believe that this is also the course to teach the concept of design reuse before we train the students to become the engineers that design everything by themselves.

We have experimented this on the sequential circuit design section of this course. After we have experienced several design examples with basic flip flops, we showed the students how to design a sequential pattern generator by reusing a given sequential counter and some combinational logic gates. Next, we revisited the previous design to compare design-from-scratch and design-by-reuse. When similar question was given in the final exam and the students had the option of designing either from scratch or by reuse, surprisingly, more than half of the class chose to reuse.

3. THE CURRICULUM INNOVATION PLAN

Encouraged by the success of the above small experiment, we have prepared an extra chapter on fundamental reuse-based design issues for this entry-level design course. Considered one of the heaviest loaded sophomore courses, this course does not have much room left for any additional materials. We have made a one-week plan (two 75-minute lectures) to introduce the concept of design reuse to the students and give them the chance to experience IP-based design by carefully designed examples, homework, and projects.

The first lecture focuses on the background information:

- why design reuse: Moore's Law, design productivity gap, time-to-market, design reuse as a major design innovation[3].
- what can be reused: the definition of IP, VLSI design IP, soft IP, hard IP, and firm IP[5].
- what is unique in IP-based design: design IP reuse vs. the reuse of small devices to produce large systems. Their difference includes the level of integration, the complexity of reuse, and design targets.

Proceedings of the 2003 IEEE International Conference on Microelectronic Systems Education (MSE'03)
0-7695-1973-3/03 $17.00 © 2003 IEEE

- reuse-based design: a simplified IP-based design model that includes IP selection, verification, integration, and evaluation. A small example such as the design of DCAM-103 digital camera (by LSI Logic Corp.) will be used to explain the key steps.
- challenges for design reuse: non-technical challenges include poor documentation, bad coding style, and lack of commenting among others. Technical challenges are summarized as the enabling techniques by VSIA[5].

The second lecture emphasizes on the practice of design reuse. Although it is impossible to showcase any real life IP-based design examples in such a lower level course and in such a short period, we find that most students can get the feeling of design reuse and indeed enjoy doing reuse-based design after this one-week effort. The basic idea is to demonstrate how to design circuits with existing devices following the IP-based design procedure, which consists of the following steps:

1. IP selection.
   We give students an "IP library" that includes both combinational and sequential systems. The goal is to teach students how to analyze design specification and find similarities between the design requirements and the functionalities provided by the IPs. The "IP library" includes adders, encoders, decoders, multiplexers, comparators, registers, counters, and systems the students implemented earlier.
2. IP verification.
   It is hard to demonstrate IP verification on such a small and simple IP library. Our mission is to reiterate the importance of verification before using any IP so they don't take anything for granted in real life IP reuse. Circuit analysis skills are required at this step.
3. IP integration.
   This step challenges students' design ability. Their job is to "glue" the selected IPs by basic logical gates to deliver the required functionality. Usually this has to be considered simultaneously when IPs are selected.
4. design verification.
   This is the phase of ensuring that all the design requirements are satisfied. Also we should emphasize on the proper documentation of the design (new IP) for later reuse.

We mention that throughout the above process, it is important to remind students the difference between these examples and real-life design reuse. We identify that the sequential circuit design section is the perfect place to add these materials. By this time, the students will have gained sufficient experience on designing (small) combinational and sequential circuits, which can be used as an "IP library". In many standard textbooks, the procedure of circuit design (from scratch) and analysis is first introduced at this stage and students are expected to practice intensively on design examples. It would have been late if we did not introduce design reuse before they get the habit of designing everything by themselves. We list some design problems that can be used, where the IP selection part (we put in parenthesis) should be omitted initially for simplicity:

- a 0-999 counter (using three BCD counters)
- a counter that goes through a given sequence (using standard mod-k counters)
- a pattern recognizer (using a circuit that recognizes another pattern)
- a timer that gives warning signals when $\frac{1}{2}$-, $\frac{1}{4}$-, and $\frac{1}{8}$-way from the set time, and issues the alarm signal at the time set (using counter, shift registers, and comparators)
- home appliances (toaster, microwave, washer and drier) that use the above timer
- a count-down timer with the 7-segment display
- a small ALU that performs the addition, subtraction, and multiplication of numbers between 0 and 9 (using multiplexers and a small ROM)
- a traffic light controller that repeats the pattern of "green-yellow-red" with an additional input signal from the "push-for-crossing-the-street" button
- a substring matcher that detects whether a binary string contains another binary string as its substring
- a vending-machine controller (using a small ROM to store all the price information)

Beyond the entry-level logic design course:

After the students learn the basics on reuse based design methodology, it becomes possible and valuable to implement systems of small/medium complexity in a one-semester lab course like the Capstone design series. Ideally, the first half of the course will be on design for reuse, where the students will re-design certain devices to make them friendly for reuse. The goal is to enforce the design reuse rules such as standard naming convention, proper documentation, and additional features for reuse. The second half will be on implementing rather complex systems by reusing existing components (open cores from *www.opencores.org* for instance). The *Reuse Methodology Manual*[2] and the tool OpenMORE (*www.openmore.com*) by Synopsys and Mentor Graphics will be very good options. We expect both Verilog and VHDL will be used due to the nature of the free IPs. FPGA device will be a realistic design platform as it has already been successfully used in several other senior curriculum innovation for similar purpose. For example, the practical and effective ways for IP training proposed by Bouldin et al.[1].

4. CONCLUSION

The concept of design reuse and fundamentals of IP-based design should be taught at the earliest possible time to undergraduates. Our experience shows that this can be done, and should be done, in the introductory level logic design course followed with a one-semester senior Capstone design lab. We propose a two-lecture material to cover the basic issues on reuse-based design in the entry level design course, where the principles of design-from-scratch is taught. The senior design reuse lab will give students hand-on experience on design by reuse and design for reuse. We argue that this is the only effective solution to train the next generation engineers for design reuse.

REFERENCES

[1] D. Bouldin, S. Natarajan, B. Levine, C. Tan, and D. Newport, "Training IP Creators and Integrators", *IEEE/ACM International Conference on Microelectronic Systems Education (MSE)*, pp. 4-5, July 1999.

[2] M. Keating and P. Bricaud. *Reuse Methodology Manual for System-on-a-Chip Designs*, 2nd Edition, Kluwer Academic Publishers, June 1999.

[3] International Technology Roadmap for Semiconductors (2001), *http://public.itrs.net*

[4] *http://www.ee.umd.edu/Academic/Under/ucourses1.htm*

[5] *http://www.vsia.com/*