Voltage Setup Problem for Embedded Systems With Multiple Voltages

Shaoxiong Hua and Gang Qu

***Abstract*—We formulate the following voltage setup problem: *how many levels and at which values should voltages be implemented on the system to achieve the maximum energy saving by dynamic voltage scaling (DVS)?* This problem challenges whether DVS technique's full potential in energy saving can be reached on multiple voltage systems. In this paper, 1) we derive analytical solutions for dual-voltage system; 2) we develop efficient numerical methods for the general case where analytical solutions do not exist; 3) we demonstrate how to apply our proposed algorithms in system design; and 4) our experimental results suggest that, interestingly, multiple voltage systems with proper voltage setup can be very close to DVS technique's full potential in energy saving.**

***Index Terms*—Dynamic voltage scaling, energy minimization, multiple voltage.**

I. Introduction

Energy consumption has become a major design issue for modern embedded systems, especially battery-operated portable devices. The aggressive push for low-power design has prompted the International Technology Roadmap for Semiconductors to predict that the future system will feature multiple supply voltages ($V_{\rm dd}$) and multiple threshold voltages ($V_{\rm th}$) on the same chip. This enables the dynamic voltage scaling (DVS), an energy reduction technique that varies the clock frequency and supply voltage according to workload at run time. The highest energy efficiency is achieved when voltage can be varied arbitrarily [1], [2]. However, physical constraints of CMOS circuit limit the applicability of having voltage varying continuously. Instead, it is more practical to make multiple discrete voltages simultaneously available for the system [3]–[5].

Most existing work on multiple voltage DVS systems assumes that the voltage setup, which includes the number of voltage levels and the voltage value at each level, is given *a priori* and focuses on developing voltage scheduling algorithms to minimize the system's energy consumption [6]–[8]. However, the multiple voltage DVS system's energy consumption depends on not only the scheduler but also the voltage setup. Raje and Sarrafzadeh [12] used dual-voltage (5.0 and 3.0 V) and three-voltage (5.0, 3.0, and 2.4 V) to demonstrate their multiple voltage scheduling algorithm for data flow graph. Chang and Pedram [11] presented a dynamic programming algorithm for the more general cases and use four-voltage (5.0, 3.3, 2.4, and 1.5 V) in their simulation. Chen and Sarrafzadeh [9] studied the dual-voltage system at gate level, where 5.0 V was used as the high voltage and different voltages from 2.0 to 4.2 V were used as the low voltage. Qu and Potkonjak [7] gave analytical solutions on how to build energy-efficient communication pipelines under latency constraints by voltage scaling and packet fragmentation. Dhar and Maksimovic [10] considered the design of finite impulse response filters with $2\mathrm{N}+1$ voltages for power minimization, where N is the order of the filter.

In this paper, we formulate and provide practical solutions to the system level *voltage setup* problem that seeks the most energy efficient voltage setting for the multiple voltage DVS system design. This work is a novel extension under the DVS research framework. We show that our methods can be used to guide system design and simulation results reveal that the three- or four-voltage system can actually be (almost) as energy efficient as the ideal system that varies voltage arbitrarily.

II. Voltage Setup Problem

We consider the design of an embedded system to perform a set of applications, or a single application with uncertainties in execution time. For simplicity of the discussion, we take the following assumptions.

- The applications are characterized by triple $\langle e_i, d_i, p_i\rangle$ ($i = 1, 2, \ldots, n$), where e_i is the ith application's execution time, d_i is the deadline, and p_i is the probability that the application with execution time e_i and deadline d_i occurs. We mention that the e_i's can be the execution times for different applications or the different execution times for the same application.
- The system supports both DVS technique and the shut-down mechanism for energy efficiency. There are multiple supply voltages $V_1 < V_2 < \cdots < V_m$ physically implemented on the chip. For each V_i, there exist analytic models for the system's power, speed, and energy. We assume that both power and energy functions are convex with respect to voltage.

We formulate the **voltage setup** problem as: *for a set of applications characterized by the triples of $\langle e_i, d_i, p_i\rangle$ ($i = 1, 2, \ldots, n$), determine the voltage values for an m-voltage DVS system such that its energy consumption is minimized without missing any deadlines; furthermore, determine the number of voltages m for the multiple voltage system to achieve the maximum energy saving*.

Unlike the DVS system that uses voltage converter to control the operating voltage at run-time [1], we assume that multiple supply voltages are physically implemented on the chip. Each voltage level is regulated by a dedicated standard voltage regulator. This reduces the system's time/energy overhead on voltage switching, which will be discussed in Section III.

The voltage setup problem exists regardless of how we model the relationships among the system's voltage, delay, power, and energy consumption. We adopt the following for our discussion. However, we mention that our proposed methods are valid for other models and similar results can be expected, as long as the convexity property holds.

Suppose that at the reference voltage $V_{\rm dd}({\rm ref})$ and threshold voltage $V_{\rm th}({\rm ref})$, the processor's power dissipation is $P({\rm ref})$ and needs time $T({\rm ref})$ to complete a fixed computation, then at supply voltage $V_{\rm dd}$ and threshold voltage $V_{\rm th}$, to complete the same amount of computation, the execution time T, power dissipation P, and energy consumption E are

$$T = \frac{V_{\rm dd}}{(V_{\rm dd}-V_{\rm th})^2}\frac{(V_{\rm dd}({\rm ref})-V_{\rm th}({\rm ref}))^2}{V_{\rm dd}({\rm ref})}T({\rm ref}) \qquad (1)$$

$$P = \frac{V_{\rm dd}(V_{\rm dd}-V_{\rm th})^2}{V_{\rm dd}({\rm ref})\,(V_{\rm dd}({\rm ref})-V_{\rm th}({\rm ref}))^2}P({\rm ref}) \qquad (2)$$

$$E = P\cdot T = \frac{{V_{\rm dd}}^2}{{V_{\rm dd}({\rm ref})}^2}P({\rm ref})T({\rm ref}). \qquad (3)$$

III. Solving the Voltage Setup Problem

For the ith application with deadline d_i and execution time $e_i \le d_i$ at the reference voltage $V_{\rm dd}({\rm ref})$, we define its ideal voltage V_i^0 to be the level at which the system will complete the workload e_i at d_i with

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S. Hua was with the University of Maryland, College Park, MD 20742 USA. He is now with Synopsis **<< AUTHOR: PLEASE PROVIDE ADDRESS >>**.

G. Qu is with the Electrical and Computer Engineering Department and Institute of Advanced Computer Study, University of Maryland, College Park, MD 20742 USA (e-mail: gangqu@eng.umd.edu).

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minimum energy consumption [2], [6]. Without loss of generality, we assume that $V_1^0 < V_2^0 < \cdots < V_n^0$ for n applications.

Theorem: (Necessary Conditions): Any solution to the voltage setup problem must satisfy the following conditions:

1) the highest voltage $V_m = V_n^0$;
2) the lowest voltage $V_1 \geq V_1^0$;
3) there exists at most one $V_i \in (V_{k-1}^0, V_k^0]$ for $k > 1$.

This theorem not only identifies the nonoptimal voltage settings, it is also fundamental for our proposed solutions to the voltage setup problem.

A. Dual Voltages Three Applications ($m = 2$ and $n = 3$)

We consider a dual-voltage system ($m = 2$) with three applications ($n = 3$). For simplicity, we assume that each application has one fixed execution time. (This does not lose the generality because one can treat an application with k different possible execution times as k applications.) Clearly, this is the simplest nontrivial case because one can simply use all the ideal voltages if $m \geq n$.

Let $V_1 < V_2$ be the system's two voltages and $V_1^0 \leq V_2^0 \leq V_3^0$ be the ideal voltages for the three applications characterized by $\langle e_1, d_1, p_1\rangle$, $\langle e_2, d_2, p_2\rangle$, and $\langle e_3, d_3, p_3\rangle$. From the above theorem on necessary conditions, we know that $V_2 = V_3^0$ and $V_1 \in [V_1^0, V_2^0]$ (because $V_2 \in (V_2^0, V_3^0]$). Under such voltage setting, we execute the three applications as follows:

- execute the third application at high voltage V_2 until its completion at deadline d_3;
- start the second application with low voltage V_1 and then speed up to high voltage V_2 to meet its deadline d_2;
- execute the first application at low voltage V_1 until its completion.

With this execution scheme, one can calculate the system's energy consumption as a function of voltages V_1 and V_2 as well as their associated threshold voltages $V_{\mathrm{th}1}$ and $V_{\mathrm{th}2}$. The value of the low voltage V_1 can then be found numerically. Furthermore, we have the following theorem.

Theorem: A analytical optimal solution exists for the case of dual-voltage three application when $V_{\mathrm{th}1} = V_{\mathrm{th}2}$.

B. Dual Voltages Multiple Applications ($m = 2$ and $n > 3$)

In this case, we know that $V_2 = V_n^0$, $V_1 \in [V_1^0, V_{n-1}^0]$ and the execution scheme will be as follows:

- execute the nth application at high voltage V_2 until its completion at its deadline;
- for applications with ideal voltages larger than V_1, both voltages will be used to meet the deadlines and save energy;
- for applications with ideal voltages less than or equal to V_1, use only low voltage V_1 until their completion.

Similarly, we can derive the expression of system's total energy consumption (see (4) for the more general case in Fig. 2). We need to determine the value of V_1 that minimizes energy and completes all the applications no later than their deadlines. (See the inequality (5) in Fig. 2 for the deadline constraint in the more general case.) However, this is a well-known hard problem in the context of nonlinear programming, where the nonlinearity comes from the fact that last group of applications finish before the deadline. Fig. 1 depicts our algorithm with linear complexity, $O(n)$, in terms of the number of applications n. It reduces the problem to solvable cases similar to the three application case and conducts a linear search for the optimal value of V_1.

C. Multiple Voltages Multiple Applications ($n > m > 2$)

Even when there are more than two voltages available, the system will still use at most two voltages to execute each application [6]. Define $\delta_{ij} = 1$ if voltage V_j is used during the execution of the ith application and $\delta_{ij} = 0$ otherwise. Consider the portion of the ith application's computation executed under voltage V_j, denote t_{ij} be the required execution time under the reference voltage to complete the same portion of the computation. We can then formulate this general voltage setup problem as a nonlinear programming problem in Fig. 2.

Input: n applications $\{< e_i, d_i, p_i >: i = 1, 2, \cdots, n\}$ with their corresponding ideal voltage levels $V_1^0 \leq V_2^0 \leq \cdots \leq V_n^0$.
Output: the optimal dual voltage setting $\{V_1, V_2\}$.
Algorithm:

```
V_2 = V_n^0;
for each k = 2, 3, ..., n-1
{  assume V_1 ∈ [V_{k-1}^0, V_k^0];
   set the i-th application's completion time to
       its deadline d_i for i = k, k+1, ..., n;
   express the execution time for applications
       i = 0, 1, ..., k-1 in terms of voltage V_1;
   solve for V_1 as in the 3-application case;
   let V_{1,k} be the solution and E_k be the energy;
}
report voltage V_{1,k} that has the least E_k as V_1.
```

Fig. 1. Voltage setup algorithm for the case of $m = 2$, $n \geq 3$.

Find $V_1, V_2, \cdots, V_m$

Minimize
$$E = \frac{P(ref)}{V_{dd}(ref)^2} \sum_{i=1}^{n} p_i \sum_{j=1}^{m} V_j^2 \delta_{ij} t_{ij} \qquad (4)$$

Subject to
$$t_{ij} \geq 0,$$
$$V_j > 0,$$
$$\sum_{j=1}^{m} \delta_{ij} \leq 2, \quad (\delta_{ij} \text{ is 0 or 1})$$
$$\sum_{j=1}^{m} t_{ij} = e_i,$$
$$\sum_{j=1}^{m} \frac{V_j}{(V_j - V_{thj})^2} \frac{(V_{dd}(ref) - V_{th}(ref))^2}{V_{dd}(ref)} t_{ij} \leq d_i. \qquad (5)$$

Fig. 2. General voltage setup problem as a nonlinear programming problem for the case of $n > m > 2$.

As analytical solutions for this general case do not exist and the exhaustive numerical search can be expensive particularly when m is large, we propose an iterative approach and an approximation method based on the convexity of the energy function to speed up the search.

An Iterative Approach:

- Start with the single voltage system with voltage $V_{1,1} = V_n^0$, at which the system has the least energy consumption.
- Apply the algorithm in Fig. 1 to solve for $V_{2,1}$ and $V_{2,2}$, the best voltage setup for dual-voltage system.
- For k-voltage ($k \geq 3$) systems repetitively do the following: let $V_{k,k} = V_{k-1,k-1}$, search $V_{k,i}$ between $V_{k-1,i-1}$ and $V_{k-1,i}$ for the most energy efficient setup such that $V_1^0 \leq V_{k,1} \leq V_{k-1,1} \leq V_{k,2} \leq V_{k-1,2} \leq \cdots \leq V_{k,k-1} \leq V_{k-1,k-1} = V_{k,k} = V_n^0$.

Note that if we know the energy overhead E_k to support k voltages on the system, we can add it to the energy consumption of the best k-voltage system and determine how many voltages we should implement on the system.

An Approximation Method:

- Start with a random m-voltage setup.
- Fix the $(m-1)$ high voltages and compute the lowest voltage V_1 by a procedure similar to that in Fig. 1.
- Determine V_2 by fixing the obtained V_1 and the other $(m-2)$ high voltages.
- Continue until after we update the value of V_{m-1}, the second highest voltage. (This is one round of updating.)

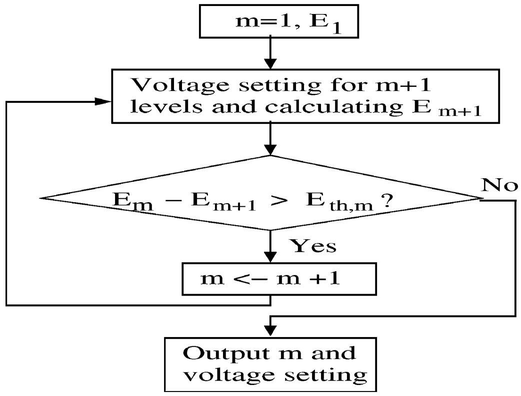

Fig. 3. Flowchart to find the best voltage setup.

- If there is energy improvement, go back to the second step with this new obtained voltage setup.
- Report the optimal voltage setup.

Although we cannot guarantee how many rounds we need to update the voltage setups to reach the optimal values, simulation shows that the voltage setup converges to the optimal solution (calculated by numerical method) after 2–3 rounds.

D. Finding the Best Voltage Setup

Supporting multiple voltages on the same system does require additional hardware and will cause area, delay, and also power penalties. It becomes important to investigate the tradeoff between more voltage levels and the overhead they introduce. Assuming that there is a threshold energy cost $E_{\mathrm{th},m}$ to introduce another voltage on an m-voltage system, Fig. 3 shows a scheme on how to find the best voltage setup, including both the number of voltage levels and the value of each level, to minimize the energy consumption. The threshold $E_{\mathrm{th},m}$ can be measured by the additional hardware cost to have $(m+1)$ voltages over m voltages and can be obtained empirically. We mention that in general this threshold energy cost increases as one attempts to implement more and more different voltages on the same system.

IV. Simulation Results

There are two goals in our simulation: demonstrating the importance of voltage setup problem and validating our proposed approaches. We formulate the voltage setup problem in two occasions for a set of randomly generated applications and the MPEG video encoder. The problems are then solved both analytically and numerically by our approaches. Finally, we compare the energy consumption under different voltage setups obtained by exhaustive simulation in Matlab in order to test the correctness of the results and the effectiveness of our proposed methods. Note in this section the energy is in the unit of energy dissipation in one CPU unit at the reference voltage 3.3 V.

Fig. 4 depicts the flow of MPEG encoding process as a set of subtasks with their triples of $\langle e_i, d_i, p_i\rangle$ as reported in [13]. The two ad hoc applications $\mathcal{A}$ and $\mathcal{B}$ are characterized by their execution time distributions and deadlines in the format of $\langle e_i, d_i, p_i\rangle$:

$$\mathcal{A} : \{\langle 9, 10, 0.03\rangle, \langle 4, 10, 0.18\rangle, \langle 3, 10, 0.39\rangle\};$$
$$\mathcal{B} : \{\langle 6, 8, 0.04\rangle, \langle 4, 8, 0.10\rangle, \langle 3, 8, 0.12\rangle, \langle 2, 8, 0.14\rangle\}.$$

Table I reports the best voltage settings for dual-voltage (solved by the algorithm in Fig. 1), three-voltage, and four-voltage (solved by the approximation method) DVS systems. Their energy consumption is compared with that by the system with the best fixed voltage and the ideal DVS system (also shown in Table I). The energy consumption for

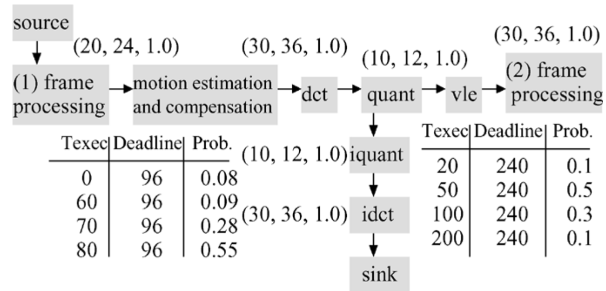

Fig. 4. MPEG video encoder execution time distributions and corresponding deadlines in 10^4 cycles (redrawn from [13]).

TABLE I
Optimal Voltage Settings and Their Corresponding Average Energy Consumption Per Execution

DVS Systems	2 Ad Hoc Applications		MPEG Encoder	
	Voltages	Energy	Voltages	Energy
fixed-voltage	3.0564	2.9536 (+151.1%)	2.8934	26.7125 (+20.1%)
dual-voltage	3.0564 1.8124	1.3833 (-53.2%) (+17.6%)	2.8934 1.8511	23.1478 (-13.3%) (+4.0%)
3-voltage	3.0564 2.0688 1.5514	1.2337 (-58.2%) (+4.9%)	2.8934 1.8558 1.3031	22.4958 (-15.8%) (+1.1%)
4-voltage	3.0564 2.0768 1.8119 1.5509	1.2071 (-59.1%) (+2.6%)	2.8934 2.6374 1.8554 1.3031	22.3020 (-16.5%) (+0.2%)
ideal	–	1.1763	–	22.2506

the ideal DVS system, shown in the last row, is obtained by assuming that the ideal voltages for all the possible execution time are available.

For the first example of two ad hoc applications, multiple voltage DVS systems save a significant amount of energy over the fixed-voltage system. The saving is more than 53% when we carefully choose the second voltage on the dual-voltage system. With the addition of the third and fourth voltage, we see the continuous increase in energy reduction. Finally, we mention that, comparing to the lower bound in the ideal system, the best fixed-voltage setup consumes more than 151% additional energy. But this "energy waste" drops to 17.6%, 4.9%, and 2.6% for the dual-, three-, and four-voltage system, respectively.

We have similar observations from the MPEG encoder example except that the multiple voltage system's energy savings are less significant, albeit a notable 13.3%–16.5%. This is because that majority of the energy is consumed on the deterministic subtasks as shown in Fig. 4. However, we are able to reduce the "energy waste" from 20% to 0.2%. This indicates the effectiveness of multiple voltage DVS system's energy efficiency, which can be very close to the maximal provided by the ideal DVS system.

Finally, we adopt the following method to validate the correctness of our results. We use Matlab to simulate 100 000 iterations of each application under different voltage setups for dual-, three-, and four-voltage systems. We set the highest voltage to go from V_n^0 (3.0564 V for the two ad hoc applications example, 2.8934 V for the MPEG encoder example) to the reference voltage 3.3 V, and other lower voltages to go from 1.0 to 3.3 V, both with an increment of 0.01 V. In all the cases, such "exhaustive" search finds the same solutions as those we report in Table I, within the precision of voltage increment 0.01 V. The Matlab simulation takes hours, our results for dual-voltage system are obtained theoretically and instantaneously, and the results for three- and four-voltage systems are reported by the approximation method in seconds.

V. Conclusion

We consider the voltage setup problem for application specific multiple voltage DVS system design. The problem seeks to determine the number of voltage levels and the voltage at each level to minimize the average energy consumption for a given set of applications. We give optimal solutions in analytic form for the dual-voltage system and develop two heuristics (an iterative approach and an approximation method) for the general case. The hardware overhead to supply multiple voltages, once obtained, can be conveniently integrated into our techniques to solve the voltage setup problem. We apply our methods to the designs of an ad hoc application specific system and the MPEG video encoder. Simulation results show the correctness and efficiency of our approaches. We also observe that multiple voltage system, if the voltage levels are set properly, can indeed achieve energy reduction very close to the full potential by DVS.

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