ABSTRACT

Title of Document: INVESTIGATION OF REACTIVELY STRUCTURED AL/NI MULTILAYER FOILS AND THEIR APPLICATIONS IN HIGH TEMPERATURE DIE ATTACH

Adam Patrick McClure, M.S. Material Science and Engineering, 2008

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This work focuses on using a reactive layered Al/Ni foil as a localized heat source for electronic die attachment purposes. A two pronged approach was used to demonstrate the viability of this material for attaching die to substrates using AuSn braze. Both experimental sample creation and transient thermal modeling were conducted. This thesis will report thermal simulation and experimental results as well as discussing the joining process and the results of shear strength and thermal cycling reliability testing. A new pre-heating method was developed after results revealed that the initial temperature of the system is vital in predicting how successful a joint will be. Thermal cycling results have shown that die cracking is a significant reliability issue but with further study this reactive joining process shows promise.

INVESTIGATION OF REACTIVELY STRUCTURED AL/NI MULTILAYER FOILS AND THEIR APPLICATIONS IN HIGH TEMPERATURE DIE ATTACH

By

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Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
M.S. Material Science and
Engineering
2008

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Acknowledgements

I would like to thank my advisor Dr. McCluskey for all of his help in guiding me and allowing me to complete my research in such an excellent learning environment. I would also like to thank my colleagues, Pedro Quintero, Tim Oberc, and, Rui Wu for their thoughts and assistance. Lastly, I would like to thank my friends and family for their love and support, without which I would never have made it as far as I have today.

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Chapter 1: Introduction

1.1: Research Motivation

One of the most fundamental components of an electronic system is how the chip or die is secured to a lead frame or substrate. Depending on the substrate material, physical size, operating environment and device requirements the choice of attachment material and process may vary greatly. The most common attachment method is called adhesive bonding and typically relies on epoxy thermoset resins to join the die and the substrate. Depending on the application, adhesive die attachment materials can be chosen to be electrically and thermally conductive or insulating [2]. Typically silver is added to epoxies in order to provide an electrically conducting joint. Some advantages of adhesive die attachment include low curing temperatures, low cost, and reduction of die stresses. On the other hand, adhesive die attachment materials are susceptible to outgassing and often times cannot survive harsh environmental conditions (e. g. T > 125° C). Another method that has been extensively used in die attachment is soldering. Soldering is a joining process that uses a filler material with a melting temperature lower than either of the components being joined. As the filler material (i. e. solder) melts, it wets the surfaces being joined and then upon cooling creates a solidified joint. A table with some common solders as well as their melting temperatures is shown below [2,3]. Some of these solders (e. g. 63Sn-37Pb) are eutectic, many are not.

Table 1: Common Solder Materials

Solder Material	Melting Range
60Sn-40Pb	183 °C - 190 °C
95Pb-5Sn	308 °C - 312 °C
Pb-In-Ag	250 °C - 310 °C
65Sn-25Ag-10Sb	233 °C- 265 °C
63Sn-37Pb	183 °C (E)

Solder materials have excellent electrical and thermal conductivities and are typically used to join components in high power electronic devices where the backside of the device is electronically active. In addition to their electrical properties, solder materials typically have sufficient compliance to allow them to absorb stresses associated with expansion mismatch between the die and substrate. Unlike adhesive die attach methods, soldering generally employs high processing temperatures (T > 200° C) as well as requiring the die and substrate to be metallized before the joining process can be carried out. Additionally soldering requires an inert gas atmosphere or flux to be successful. A subset of solder bonding is gold eutectic bonding. A gold eutectic bond is a solder-type bond that is made using a gold-rich high temperature alloy that melts at a lower temperature than any of the individual material constituents. The table below shows the most commonly used gold eutectic materials and their melting points [2,3].

Table 2: Common eutectic solders

Eutectic Material	Melting Temperature
Au97-Si3	363 °C
Au88-Ge12	356 °C
Au80-Sn20	280 °C

Gold eutectic materials offer advantages over non-eutectic soft solder materials due to their instantaneous transition into the liquid phase upon reaching their melting temperatures. Unlike non-eutectic solder materials, eutectic materials do not have a

semi-solid state between solid and liquid that can lead to problems if the joint is moved during cooling. Gold eutectics have excellent electrical and thermal conductivity as well as exhibiting good fatigue and creep resistance. The main disadvantage with eutectic bonding is that high stresses are created in the silicon chip due to coefficient of thermal expansion mismatch between the chip and the substrate and the stiffness of the attach. Glass die attach materials have also been used. The glass is in a paste form and then heated to temperatures above 350° C. The glass forms a low viscosity liquid that wets the die and substrate creating a joint on solidification. Typically silver particles are added to the glass to improve electrical and thermal conductivity. Glass die attachment is a good method in that it has low void content and can usually be accomplished with or without metallization. Glass die attachment is limited by its' high processing temperatures as well as by the fact that it must be carried out in an oxidizing atmosphere. A table summarizing the different types of die attachment methods and their advantages and limitations can be seen below [2,3].

Table 3: Attach Method Summary

Attach Method	Advantages	Limitations
Adhesive die attach	-Ease of automation -Low cost -Low curing temperatures -Reduced die stresses	-Outgassing -Voiding -Sensitive to harsh environments
Soldering die attach	-High thermal and electrical conductivity -Good CTE	-Surfaces need to be metallized -Processing temperatures > 200° C -Needs flux
Gold Eutectic die attach	-Good thermal conductivity -Good fatigue resistance -High operating	-High Si stress -Surfaces need to be metallized -High processing temps.

	temperatures -Instantaneous transition into liquid state	
Glass die attach	-Low voiding -Not dependant on metallization -Good electrical and thermal conductivity	-High processing temperatures -Oxidizing atmosphere is needed

Given the increased demand for electronic systems that can operate above 125º C for applications in automobiles, avionic systems, alternate energy generation, space exploration and various other commercial and military applications it is vital to investigate new materials and processes that can accommodate such high temperatures [1].Silver filled epoxies, used for die attachment in small commercial devices, typically fail at approximately 200º C and are not suitable for high temperature applications [4]. On the other hand, gold based eutectic solders, considered due to their higher melting points (~280º C), require processing temperatures that are above 300º C which can harm other components within the system. In this study, a new method that addresses this issue by using a reactive multilayer foil as a localized heat source to melt the solder materials has been investigated.

1.2: Introduction to Reactive Foils

Reactive multilayer foils are a relatively new class of materials that are typically created by vapor depositing or magnetron sputtering hundreds of nanoscale layers of materials that have high exothermic heats of mixing. By introducing a thermal or electrical pulse across two alternating materials such as nickel and aluminum, it is possible to create a self-propagating controlled reaction. Self-

propagation occurs as the energy from the intermixing layers increases the local temperature sufficiently to create faster intermixing and more energy. These reactions are driven by reductions in chemical bond energies which lead to the release of large quantities of heat that are conducted along the foil [5]. The spreading heat can propagate at speeds up to 30 m/s in some cases [5]. The heat released by the alternating atomic layers can elevate the temperature of the foil to above 1200 ºC in a matter of milliseconds [6]. Self-propagating reactions have been in observed in numerous nanostructured foils including Al/Ni, Al/Ti, Ni/Si, Ni/Ti and Nb/Si [6-12]. Reaction speed is primarily determined by the bilayer period of the alternating materials as well as by the size of the premix region. A schematic below shows a typical multilayer foil with both a bilayer (4δ) and a premix region (4w). [8]

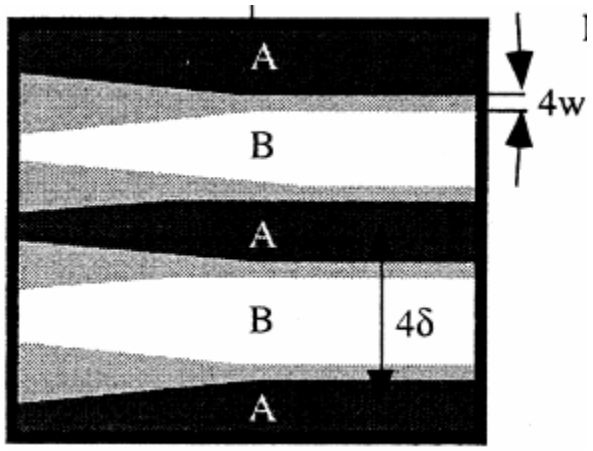


Figure 1: Reactive foil schematic showing bilayers and pre-mix region

Figure 1 illustrates a typical multilayer foil in that the alternating layers, A and B have a uniform thickness of 4δ, and that there is a gray region where materials A and B are in a partial premix (before foil ignition) state with a thickness of 4w. As the

reaction propagates from right to left, the mixed region becomes larger. The existence of this premix region is a consequence of the deposition technique and along with the bilayer thickness can have a significant effect on the average reaction propagation speed. Studies by Jayaraman, Mann, and Reiss et al have shown through experimental and analytical methods that the average propagation velocity increases as the bilayer thickness decreases [8,9]. This phenomenon only applies however when the bilayer thickness is much greater than the thickness of the premix region. As the bilayer period gets closer to the premix region width a critical value is reached and the average propagation velocity decreases to 0 [8,9]. This information is important because it proves that the reaction can be controlled by varying the thicknesses of the deposited materials. Each of the hundreds of alternating layers of material are typically on the order of tens of nanometers so the overall foil thicknesses range in size from 10 to 200 μm. These materials are important to study because they can be used to reactively join two components. By placing a reactive foil and two braze layers between components and then initiating the reaction, it is possible to melt the two solder layers thus bonding the components. This joining method offers distinct advantages over other more traditional methods as it is flux-free room temperature process that can be carried out very rapidly. Additionally with a localized heat source there is less potential for temperature sensitive components to become damaged. This joining method has shown potential with Au-plated aluminum, metallic glass, Au-plated stainless steel, and titanium joints being joined in this way [13-15]. This particular work will focus on the creation and characterization of various electronic joints using an aluminum nickel nanofoil as the reactive layer.

The experimental approach that was used in this work is described in the following sections.

1.3: Sample Constituents

The four main components that were used in this process were the substrate, the solder layers, the reactive foil, and the die. The die was formed by coating the backside of a 4 inch diameter, 500 micron thick mechanical grade silicon wafer with 300 angstroms of chromium, 200 nm of nickel, and then 300 nm of gold. The wafer was then diced into three different die sizes. The "small" dies were 3mm x 3mm, the "medium" dies were 5mm x 5mm, and the "large" dies were 7.5mm x 7.5mm. Samples have been created with dies up 12.7mm by 12.7mm however die cracking was a significant issue in these larger dies. The solder layers were 80 wt% Au-20 wt% Sn preforms and were either 25 microns or 50 microns thick. The reactive layer was a nanostructured Aluminum/Nickel multilayer foil of which various thicknesses were tested. The reactive layer is developed by Reactive NanoTechnologies, Incorporated. Both stainless steel and Al_2O_3 direct bonded copper (DBC) materials were used as substrates. Stainless steel was used due to its availability and as a cost effective method for carrying out preliminary tests with a material of similar thermal conductivity to DBC. The DBC substrates were used in an attempt to create a more realistic process that would have significance in the power electronics industry. Before the joining process was attempted both types of substrates were metalized through e-beam deposition processes. The stainless steel was coated with 400 nm of titanium, 100 nm of nickel, and 300 nm of gold. The DBC alumina substrate was

processed by removing the oxide layer and then depositing 750 nm of gold onto the surface. A schematic of a sample can be seen in Figure 2 below.

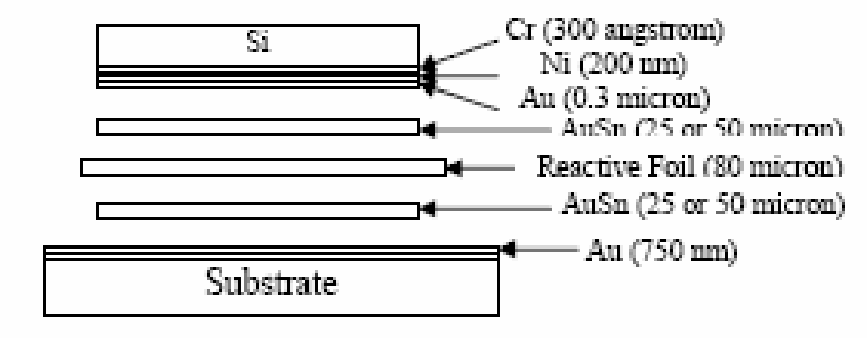


Figure 2: Die stack configuration

1.4: Approach

To better understand this joining process two main approaches were used. One technique was attempting to make the samples themselves, and another technique was to simulate the joining process using finite element modeling. By concurrently examining both theoretical models and experimental samples insight into this particular joining process was gained. In addition to a transient two dimensional thermal model, experimental samples were attempted and analyzed. Samples were initially characterized using x-ray and CSAM as well as tested for die shear strength. Successfully created joints were also exposed to temperature cycling in an attempt to assess joint reliability over time. Simulation and experimental results are discussed and reported below under their respective chapter headings.

Chapter 2: Preliminary Finite Element Modeling

2.1: Basic Physical and Thermal Properties

Given various foil material properties from Reactive Nanotechnologies along with known constitutive properties of the solder, foil, and substrates it is possible to create a two dimensional transient thermal model that will output temperature as a function of time at various positions within the joint. This thermal model will give insight into the potential for forming a quality joint at a given processing condition as well as assisting in the design of joint geometry.

Tables 4 and 5 below, summarize the dimensions of the sample constituents as well as some of the important properties for thermal modeling including density, specific heat, and thermal conductivity [16-17].

Table 4: Physical model properties

	Thickness (mm)	**Sizes (mm x mm)**
DBC-Copper	.300	38.02 x 38.02
DBC-Al_2O_3	.635	38.02 x 38.02
Stainless Steel	1.58	19.05 x 19.05
AuSn Solder	25e-3 or 50e-3	5 x 5 or 7.5 x 7.5
Nanofoil	80e-3	5 x 5 or 7.5 x 7.5
Silicon	.500	5 x 5 or 7.5 x 7.5

Table 5: Thermal modeling properties

	Density (kg/m^3)	**C_p (J/Kg-K)**	**K (W/m-K)**
DBC-Copper	8700	385	400
DBC-Al_2O_3	3965	730	35
Stainless Steel	7850	500	16.3
AuSn Solder	14510	Function of Temp	57
Nanofoil	5080	680	135.35
Silicon	2330	702	124

Within Table 5, it is important to note that the specific heat and thermal conductivity values for the foil were calculated as an average of the values between Al and Ni which are the two materials that made up the reactive foil. The density of the foil was determined through a simple mass and area calculation. Models were created using both DBC Alumina substrates as well as stainless steel substrates. In both cases, the die stack consists of the die, the two solder layers, and the reactive foil. To simplify the simulation, a symmetry boundary condition was employed about the center axis of the die. A schematic of the area that was simulated can be seen below in Figure 3.

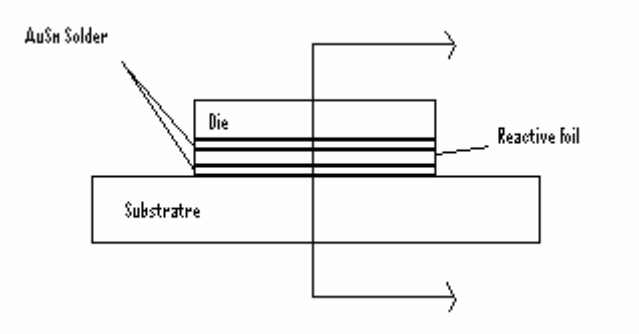


Figure 3: Symmetry condition used for thermal simulation

2.2: Calculated Properties

Two of the most important variables in the thermal simulation are the heating profile generated by the nanofoil, and the specific heat of the solder.

2.2.1: Heating Profile

The volumetric heat generation, or W/m^3 and the time of the heating pulse were determined for the nanofoil using the values for the speed of reaction and the energy released per gram provided by the company that manufactured this particular reactive foil. As an example consider the case where the sample is a 7.5mm x 7.5mm die with an 80 micron thick reactive foil.

Given

Size of Nanofoil = .0075 m x .0075m
Thickness of Foil = 80e - 6 m

Using these dimensions as well as the speed of the reaction, energy released per gram, and calculated density it is possible to obtain the heating profile for this particular

system. The density was calculated by weighing a reactive foil of known volume and then dividing the mass by the volume.

Given

$$\text{Density} = 5080 \text{ kg/m}^3$$

$$\frac{\text{Energy}}{gram} = 1180 \text{J/g}$$

$$\text{Speed of Reaction} = 10 \text{m/s}$$

Calculations

Given the size of the foil and the speed of the reaction propagation the total time for the reaction can be calculated. Additionally, given the density and size of the foil the mass for this particular system was calculated.

$$\text{Time for Reaction} = .\frac{0075 \text{ m}}{10 \text{m/s}} = .00075 \text{ s}$$

$$\text{Foil Mass} = \text{Density} * \text{Volume} = 5080 \text{kg/m}^3 * (.0075m * .0075m * 80e-6m) = 2.286 * 10^{-5} kg$$

$$FoilMass = .0229g$$

With the calculated foil mass and the given energy release per gram the amount of energy that this reaction will release is calculated. This value can then be converted into power by dividing by the time it takes the reaction to complete. To obtain volumetric heat generation the power is divided by the volume of the reactive foil. The calculations to obtain the volumetric heat generation are shown below.

$$\text{Energy} = 1180\text{J/g} \ * \ .0229\text{g} = 27.0220J$$

$$\text{Power} = \frac{\text{Energy}}{\text{Time for Reaction}} = \frac{27.0220\text{J}}{.00075s} = \ 3.6029 * 10^4 W$$

Volumetric Heat Generation = W/m^3

$$\text{Volumetric Heat Generation} = \frac{3.6029 * 10^4 W}{(.0075m * .0075m * 80e-6m)} = 8006500 MW/m^3$$

The heating profile is then 8.0065 x 10^{12} W/m^3 for .75 milliseconds. The loading profile is shown in the Figure 4 below.

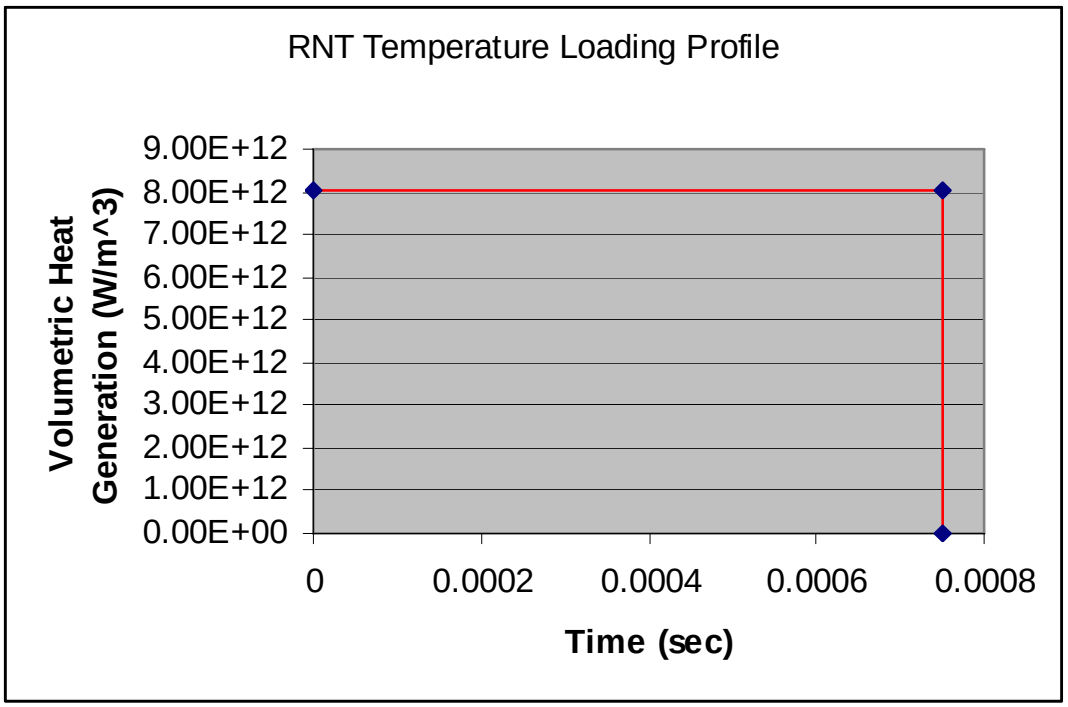


Figure 4: Temperature loading profile

To determine if the total energy in the heating profile is sufficient the following calculation was performed

2.2.2: Heat of Fusion

The heat of fusion calculations follow the work carried out by Wang et al, using the following equation [18].

$$Q = m(T_m - T_{RT})C_p + m\Delta H_f$$

Where:

Q=Heat needed to melt two AuSn solder layers

m=mass of the two solder sheets

Take for example the largest AuSn to be melted which is a 7.5 mm sample with 50 micron thick AuSn :

Given density of AuSn=14.51 g/cm^3 [20]

m = volume x density x 2 (for the two solder sheets)

m = (0.75 cm x 0.75 cm x .005 cm) x (14.51 g/ cm^3) x 2 = .0812 g

T_m=melting temperature of the solder (280 °C)

T_{RT}=room temperature (25 °C)

C_p=heat capacity of the AuSn solder (0.15 J / g °C) [20]

ΔH_f = Heat of Fusion (27 J/g) [23]

$$Q = m(T_m - T_{RT})C_p + m\Delta H_f$$
$$Q = .0812g(280°C - 25°C)(0.15J / g°C) + (.0812g)(27J / g) = 5.3J$$

Given that the energy supplied, 27 J, is greater than the energy needed (5.3 J) to heat the AuSn solder layers to their melting point and fuse them, the heating profile should be sufficient to melt the AuSn solder layers.

2.2.3: Boundary Conditions

The schematic below in Figure 5 details the boundary conditions that were used in this simulation

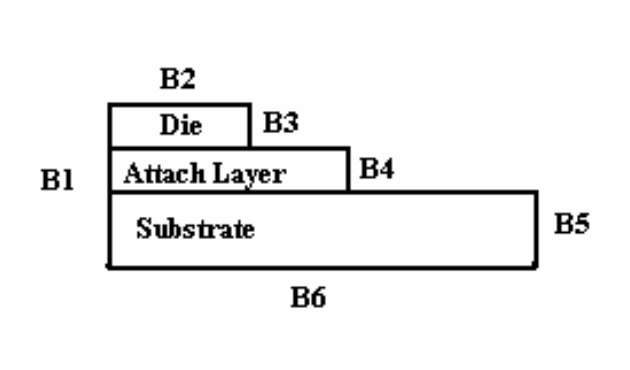


Figure 5: Boundary conditions used for thermal model

Boundary condition B1 exists along the axis of symmetry within the sample and contains the middle of the die, the AuSn layers, the reactive foil, and the substrate. A thermal insulation boundary condition was employed at this interface. Boundary conditions B2-B6 were convective with a convection coefficient of 25 W/m-K [19] with an ambient air temperature of 293 K. Boundary condition B4 actually contains three separate boundary conditions, one each for the two solder layers and the foil layer. It was also important to note that although surfaces B2 and B6 were exposed to the test fixture as opposed to ambient air, air was still used as the boundary condition medium. Given that the substrate essentially functions as an infinite heat sink where heat at large distances from the foil is almost negligible due to extremely rapid

cooling rate [18] the test fixture never comes into play with regards to boundary conditions. On the die side of the sample, air was used as a boundary condition because in most power electronics joining applications the substrate acts as a heat sink so most of the heat would be transferred to the substrate. Very little heat reaches the top of the die. This phenomenon can be observed in Figure 6 and Figure 7 which show temperature contour plots where the top of the die remain as cool as the bottom of the substrate. It is important to note that this simulation assumes that the entire die stack is one continuous entity. In reality there may be small air gaps between the free standing layers that create thermal resistances which alter the simulation results. These thermal resistances were not directly included in the modeling but were considered when analyzing why initial experimental samples may have not been as successful as anticipated. Based upon previous work joining stainless steel samples, the applied pressure was deemed to be sufficient for creating adequately uniform surfaces without air gaps that may have adversely affected joints.

Given all of these values a transient thermal analysis was carried out using COMSOL Multiphysics engine [16]. The finite element analysis was carried out using triangular mesh elements that were automatically generated and meshed by the software. Since the attach interfaces were of particular importance in this study the mesh was further refined using automatically generated mesh elements at these points of interest. In all approximately 4,000 nodes were used for each die configuration. Given the additional mesh refinement at the interfacial layers coupled with the relatively long time to complete a single simulation (approximately 40 minutes), it

was determined that this number of elements would be more than adequate for analyzing thermal response of this particular system. In addition to the results discussed and shown below, additional die stack configurations were modeled and their contour plots and temperature profiles can be seen in the appendices under the appropriate headings. Generally, the samples simulated with the stainless steel substrates remained at higher temperatures longer than samples that were created with DBC substrates.

2.3: Simulation Results

The temperature contour plot in Figure 6 shows a 7.5mm x 7.5mm die configuration with an 80 μm thick reactive foil and 50 μm thick solder layers. Figure 6 shows a thermal simulation with a stainless steel substrate and Figure 7 shows a thermal simulation with an Al_2O_3 DBC substrate. These plots are displayed at the instant when the reactions have completely propagated through the foils.

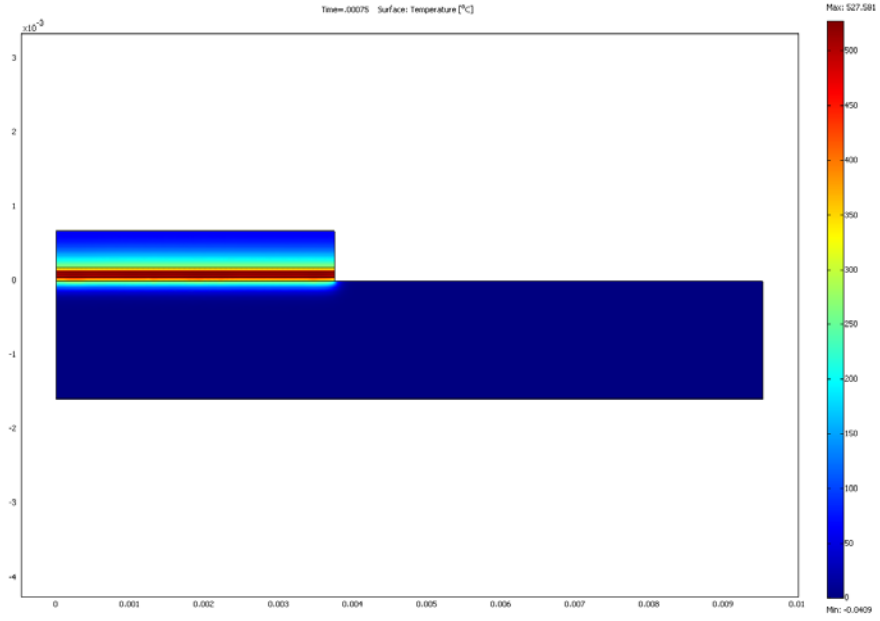


Figure 6: Stainless steel substrate temperature contour plot

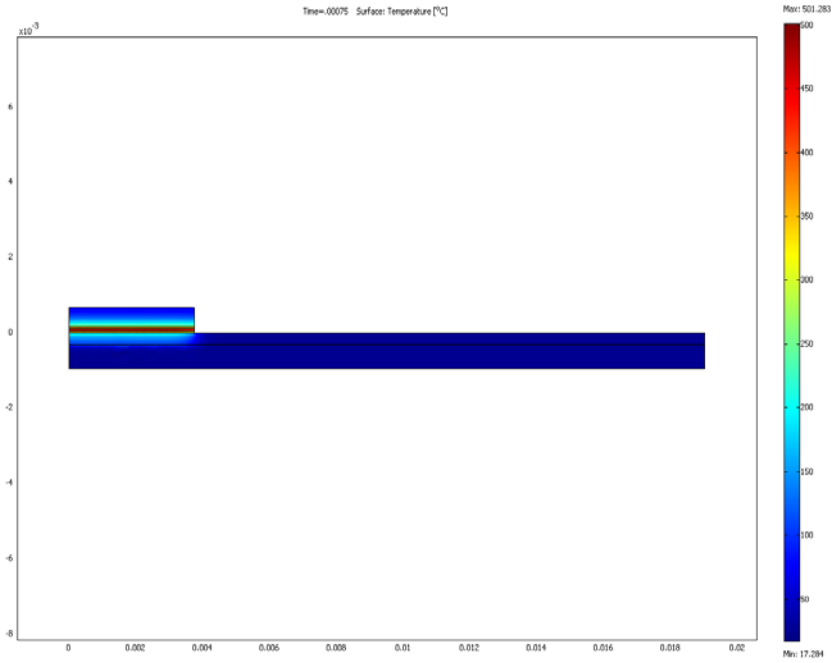


Figure 7: DBC substrate temperature contour plot

The maximum temperature of approximately 530 °C and 500 °C for the stainless steel and DBC substrates respectively occurs in the middle of the foil and corresponds to reaction completion. However, it is even more useful to look at the temperature profile at specific points within the joint over extended periods of time. The most important points to examine are the attach interfaces occurring between the solder layers and either the substrate or the die, as proper joint creation depends on how long each will remain above the melting point of AuSn solder (280 °C). The four figures below show temperature profiles for both substrates at the interfaces between the solder and the die and between the substrate and the solder. Figure 8 and Figure 9 are for the DBC substrate samples and Figure 10 and Figure 11 are for the stainless steel substrate samples.

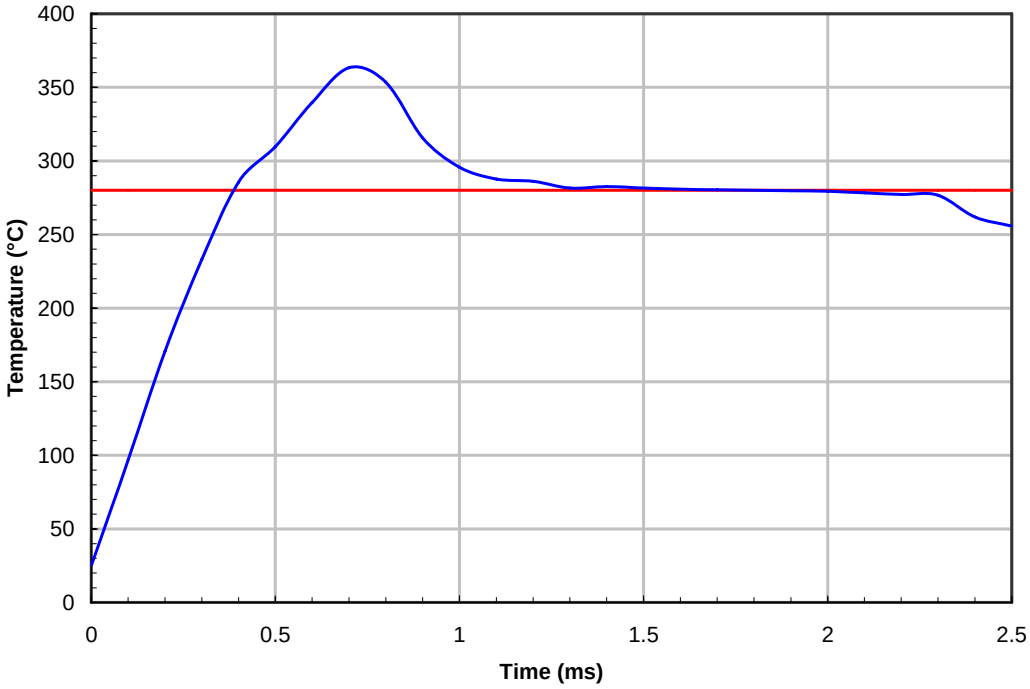


Figure 8: Solder to die interface with a DBC substrate

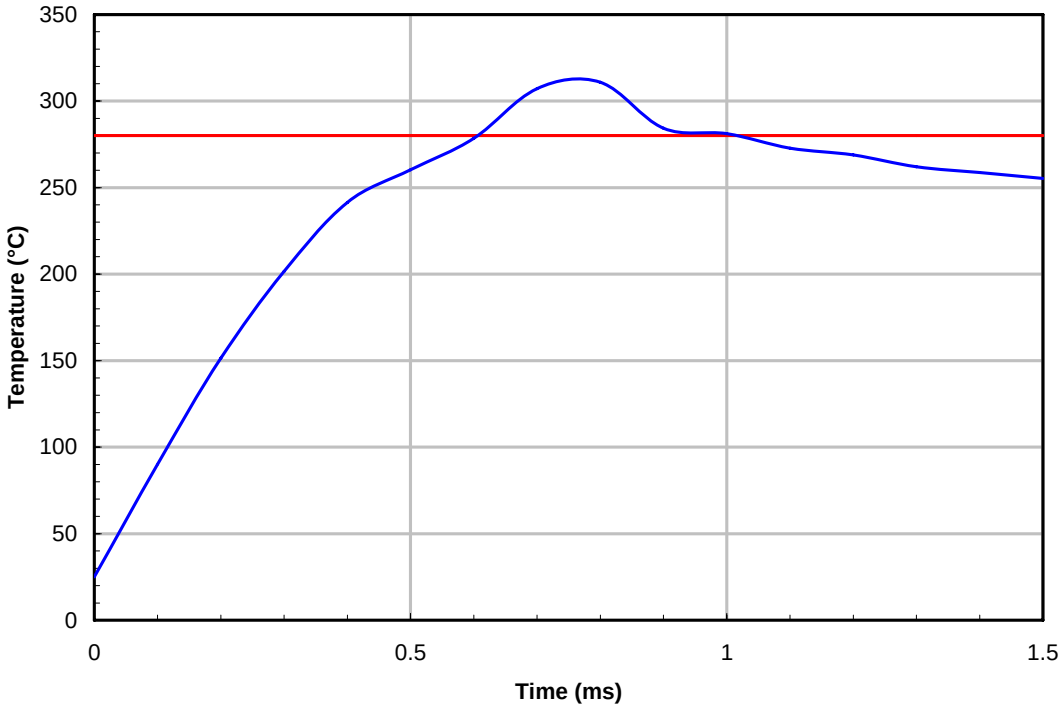


Figure 9: Solder to substrate interface with a DBC substrate

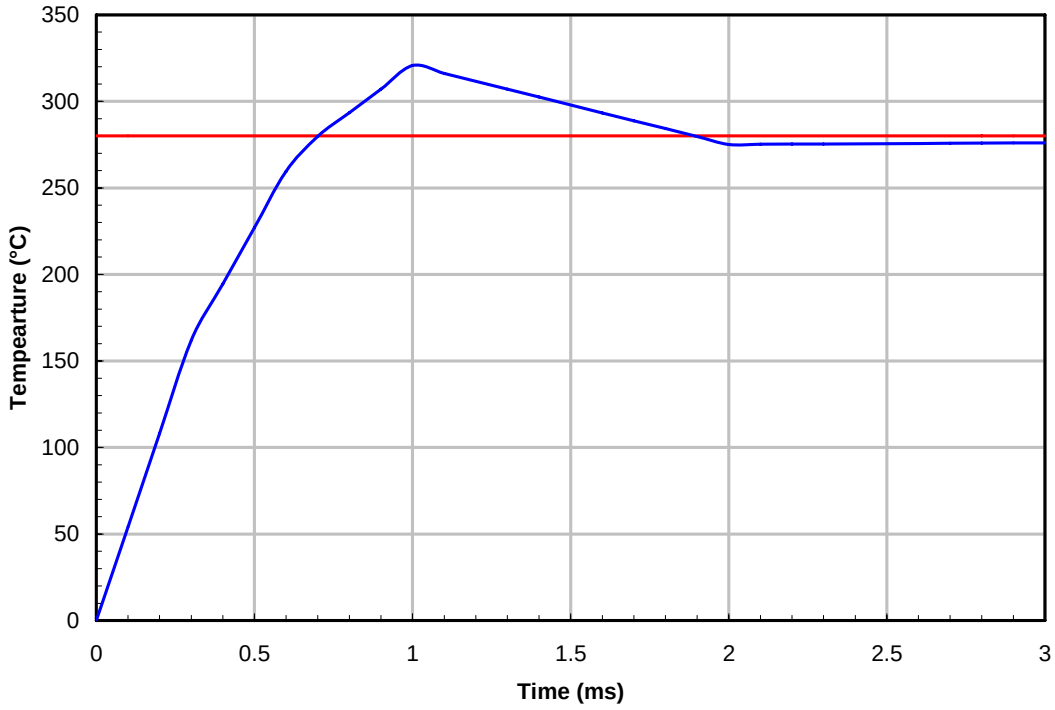


Figure 10: Solder to die interface with stainless steel substrate

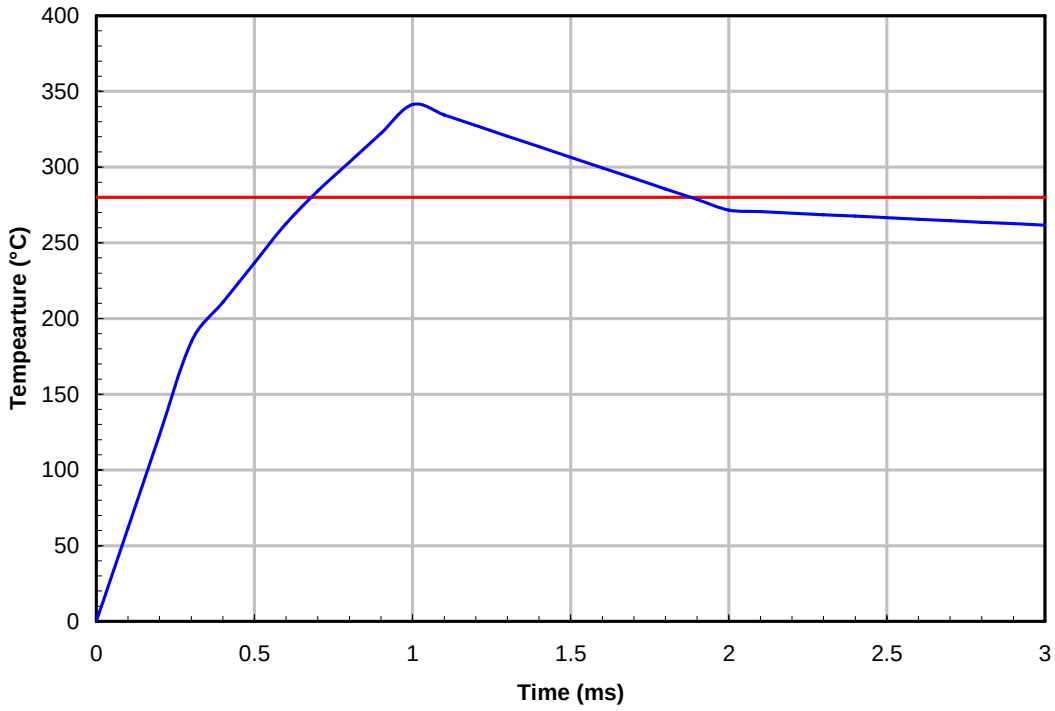


Figure 11: Solder to substrate interface with stainless steel substrate

For both types of substrates the thermal simulation results have shown that the solder to die and solder to substrate interfaces are only above the AuSn melting temperature for very short periods of time (~.0018 seconds and ~.0005 seconds for the DBC and .0012 and .0012 for the stainless steel respectively). Simulations on stainless steel samples show a more even temperature distribution between substrate and die as well as remaining hotter for longer periods of time when compared to the simulations with DBC substrates. This phenomenon can be attributed to stainless steels' lower thermal conductivity. Stainless steel cannot dissipate heat as efficiently as DBC, thus the samples that are created on stainless steel will remain at higher temperatures for longer periods of time. Keeping in mind that more conventional joining processes require solder layers to be above liquidus for 45 to 90 seconds these results helped to explain some of the difficulties with initial experimental samples.

Chapter 3: Preliminary Experimental Samples

3.1: Sample Process

AuSn solder preforms and nanofoil layers were cut to the dimensions of the silicon die (5mm by 5mm or 7.5 mm by 7.5 mm). The solder preforms were cut with scissors and the nanofoil layer, being quite brittle and reactive, was broken apart with plastic tweezers to prevent premature foil ignition. As a consequence of having to use plastic tweezers, the reactive layer was approximately sized and may have been slightly larger than the silicon die depending on how the foil broke into pieces. It was important to make sure that the foil covered at least the same amount of area as the die to ensure a joint was created. After the solder and the foil had been cut to size, all of the pieces in the die stack (Figure 2) were cleaned with acetone, methanol, and isopropyl alcohol. The die stack layers were then assembled with plastic tweezers in the same order as shown in the schematic in Figure 2. Alignment of each constituent was vital in creating the uniformly distributed reaction required to create a satisfactory joint in which the die remained affixed to the substrate. After stacking the constituents, an elastomeric pad was placed on top of the silicon die in an attempt to reduce potential die cracking resulting from non-uniformities in pressure exerted by the load cell. An image of the die stack with the pad is seen in Figure 12.

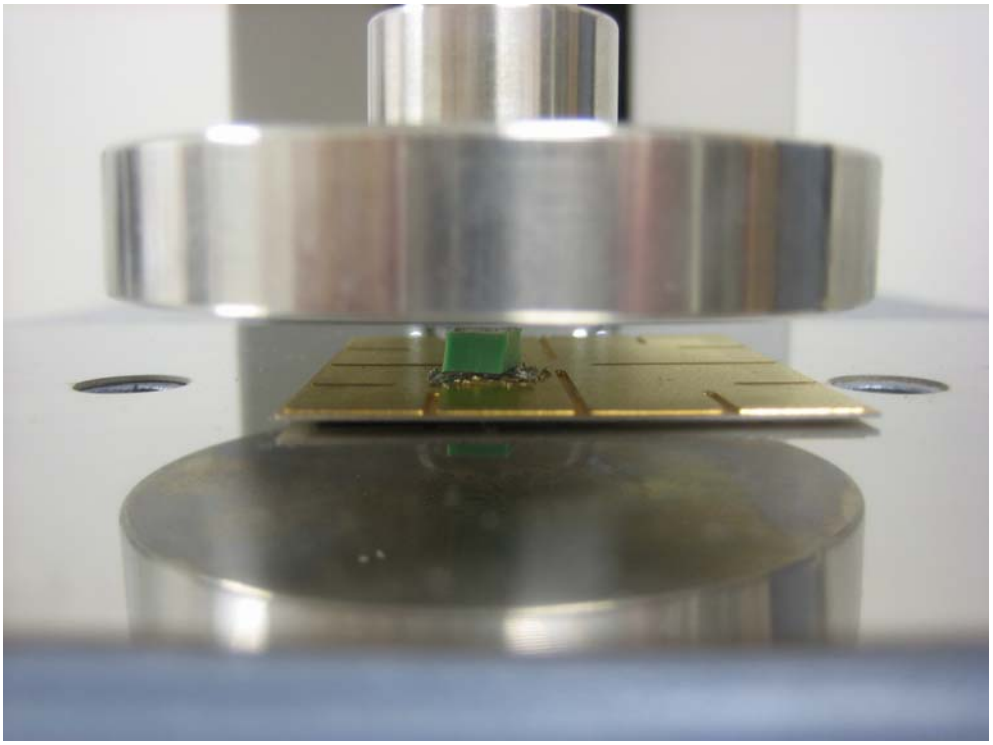


Figure 12: Full die stack including polymeric gel the moment before applying pressure

With the gel in place a pressure load was applied using an IMADA manual load cell

Figure 13: IMADA manual load cell used to apply pressure to samples

The compression measurement was determined from an IMADA DPS-110R force gauge which can display a maximum force of 110 lb (Figure 14).

Figure 14: Digital force gauge (110 lb maximum 0.1 lb resolution)

After the gauge reached the required force the reactive layer was ignited by contacting the foil with wires that were connected to opposite terminals of a 9-volt battery. After ignition, the sample was allowed to sit for approximately 1 minute before the pressure was removed, completing the joining process. A completed sample is shown in Figure 15.

Figure 15: Completed sample

3.2: Preliminary Sample Results

The samples that were created using this initial process seemed to exhibit two consistent failure modes. The first failure mode was the inability to form an initial joint due to incomplete and or poor wetting of the AuSn solder layers. Samples that exhibited this type of failure generally showed no or partial wetting at the solder to substrate and solder to die interfaces and would leave partially melted or un-melted solder layers. The lack of wetting led to unattached dice as well as bare substrates. Figure 16 and Figure 17 show digital images of a joint that was attempted with a 7.5mm x 7.5mm die, 80 μm foil, 50 μm AuSn layers, and an applied pressure of 50 psi. The first image shows a bare substrate with some of the gold removed where the joint was attempted. This indicates that melting occurred with dissolution of the Au into the joint but that there was a subsequent dewetting of the stainless steel surface.

The dark brown spot at the bottom right corner of the removed gold area is where the reaction was initiated. It is clearly visible that neither the die nor the AuSn solder layer remained affixed to the substrate. The second image shows the backside of the silicon die as well as partially fused AuSn and foil layers. The blue-gray colored backside of the die suggests partial wetting but, still some gold can be seen towards the bottom of the die. In the right part of the image, wetting can be seen as some of the silicon remains on the AuSn. It does appear however that the reaction is very limited in area as some of the shiny metallic AuSn (seen on the right side of the image below the wetted silicon) has not been melted.

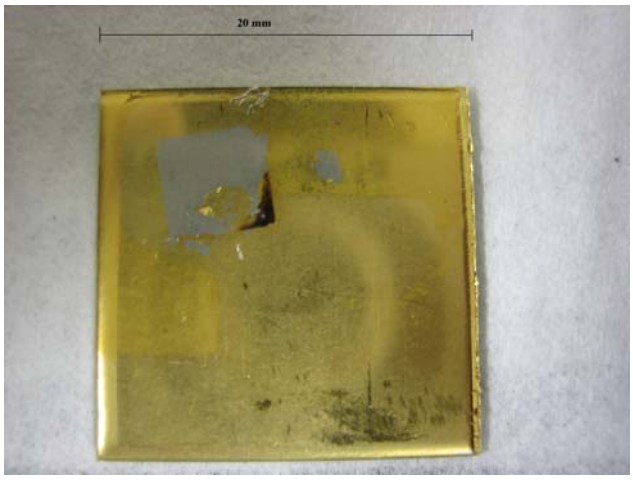


Figure 16: Un-wetted stainless steel substrate

Figure 17: Partially wetted die and solder layers

These catastrophic failures occurred in the majority of the initial samples and a chart summarizing the various pressures, die sizes, and substrate types that were used is seen below. The primary variables that were altered in attempts to create successful joints are listed below the table along with their results.

Table 6: Attempted physical samples

Substrate Type	Die Size (mm x mm)	Foil thickness (microns)	Pressure (psi)	Failure
Stainless Steel	5 x 5	80	50	No Wetting to Substrate
Stainless Steel	5 x 5	80	100	No Wetting to Substrate or Die
Stainless Steel	7.5 x 7.5	80	50	No Wetting to Substrate or Die
Stainless Steel	7.5 x 7.5	80	100	No Wetting to Die
Thin S.S.	5 x 5	80	50	No Wetting to Die

Thin S.S.	5 x 5	80	100	No Wetting to Die or Substrate and Die Crack
Thin S.S.	7.5 x 7.5	80	50	No Wetting to Substrate or Die and Die Crack
Thin S.S.	7.5 x 7.5	80	100	No Wetting to Substrate or Die and Die Crack
DBC	5 x 5	80	50	No Wetting to Substrate or Die
DBC	5 x 5	80	100	No Wetting to die and die cracking
DBC	7.5 x 7.5	80	50	No wetting to substrate or die
DBC	7.5 x 7.5	80	100	No wetting to substrate and die cracking

-Substrate Type: Along with the standard stainless steel substrates, DBC and a "thin" stainless steel (.3mm thick) were also investigated to see if they helped to improve wetting. The theory behind using thinner stainless steel was to allow less heat to be dissipated by the substrate, thus increasing the amount of energy going into wetting the solder layers. Regardless of the type of substrate the same issues with wetting were observed.

-Die Size: Different die sizes were investigated to see if having more or less of a surface area aided in wetting. Although larger dies provided more area to potentially wet to, no improvements were seen.

-Foil Thickness: Previous work has suggested that an 80 micron thick foil would adequately allow wetting in stainless steel based samples so this variable was not altered [18].

-Pressure: Applied pressure was also considered as it was generally believed that a higher pressure would yield more successful joints. This theory proved partially correct as wetting seemed to improve slightly, but with any pressures above 50 psi, die cracking became a significant issue.

This table and information is important because it shows that regardless of the variables, lack of wetting is a primary concern when attempting this joining process. The only configurations that showed adequate wetting were carried out on the standard stainless steel substrates but even then results were varied as often times the successful joints would exhibit a different type of failure.

The second failure occurred as a joint was created but would exhibit die cracking. A typical x-ray image of a joint with a cracked die can be seen below in Figure 18.

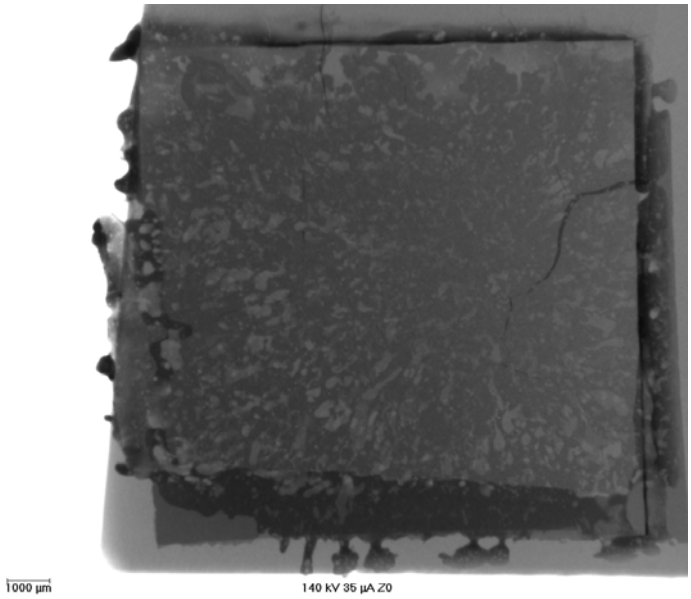


Figure 18: X-ray image of die cracking

This particular sample was a 12.7mm die with an 80 µm foil, 50 µm AuSn layers, and an applied pressure of 100 psi. Although silicon is virtually transparent to x-rays, cracking is clearly seen towards the right center of the image above. In addition to using x-rays to analyze these preliminary samples, many samples exhibited die cracks that were visible to the naked eye ranging in size from .5 mm to 3 mm. The two main variables that affected die cracking were the applied pressure and the die size. The larger the die or the applied pressures (>50 psi), the more likely the sample was to exhibit die cracking.

3.3: Preliminary Sample Discussion

Although preliminary samples were not particularly successful, much insight was gained with regards to improving the process. From initial samples it was clear that the most important factors in controlling die cracking were reducing the applied pressure as well as die size. The most successful samples within the range studied

from a die-cracking standpoint were created with 50 psi of pressure and 5 mm x 5 mm die. Samples without die cracking were also fabricated with 7.5 mm x 7.5 mm die however results were typically more consistent in smaller die sizes. Regardless of die cracking however, the more abundant and devastating failure was the lack of wetting between the die, solder layers, and substrates. Although it is fairly clear from simulations that the energy output from the reactive foil is more than adequate to allow melting in a specific instant, the reaction front in attempted samples is moving too quickly to allow for full melting of the AuSn solder layers.

Chapter 4: Pre-Heated Sample Simulation and Creation

4.1: Pre-Heated Simulation Results

Considering the initial simulation results as well as experimental observations it was determined that the primary cause of failure in the initial samples was a lack of wetting and or un-melted or partially melted solder layers. This lack of melting is believed to be attributed to the extremely short times that the solder layers are above their melting temperatures (approximately 10,000 times shorter than normal reflow processes). To address this process constraint two simulations were carried out. One simulation attempted to examine a slower burning foil and the other determined the effects of pre-heating the entire die stack. Each of these simulations and their respective results are presented in the following sections

4.1.1: Timed Burn Simulations

It was theorized that if reaction times could be increased then the solder interfaces would remain above their melting temperatures for longer periods of time. Simulations were carried out for Al/Ni foils that burned for 5, 10, 25, and 100 times as long as the standard foil. While the times were directly altered within the simulation they are indicative of the types of decreased reaction speeds that would be achieved by using a patterned nanofoil. The two figures below show temperature profiles for the longer burning foils plotted against the profiles of the original foil. Figure 19 shows the substrate to solder interface using stainless steel, and Figure 20

shows the substrate to solder interface using a DBC substrate as this was the un-wet interface.

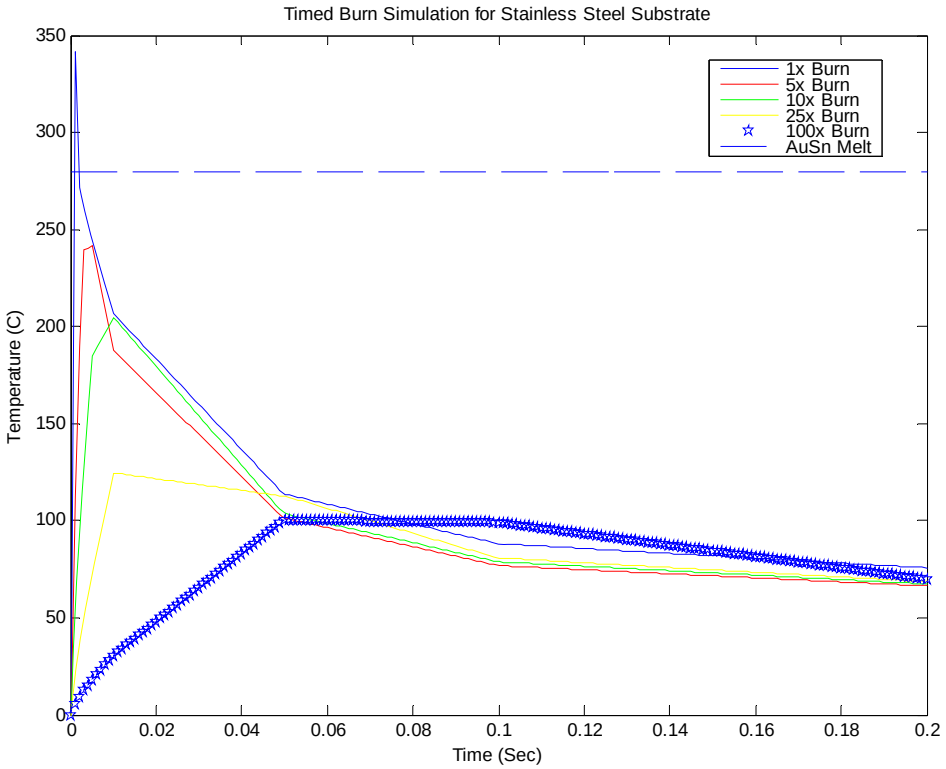


Figure 19: Timed burn simulation for stainless steel configuration

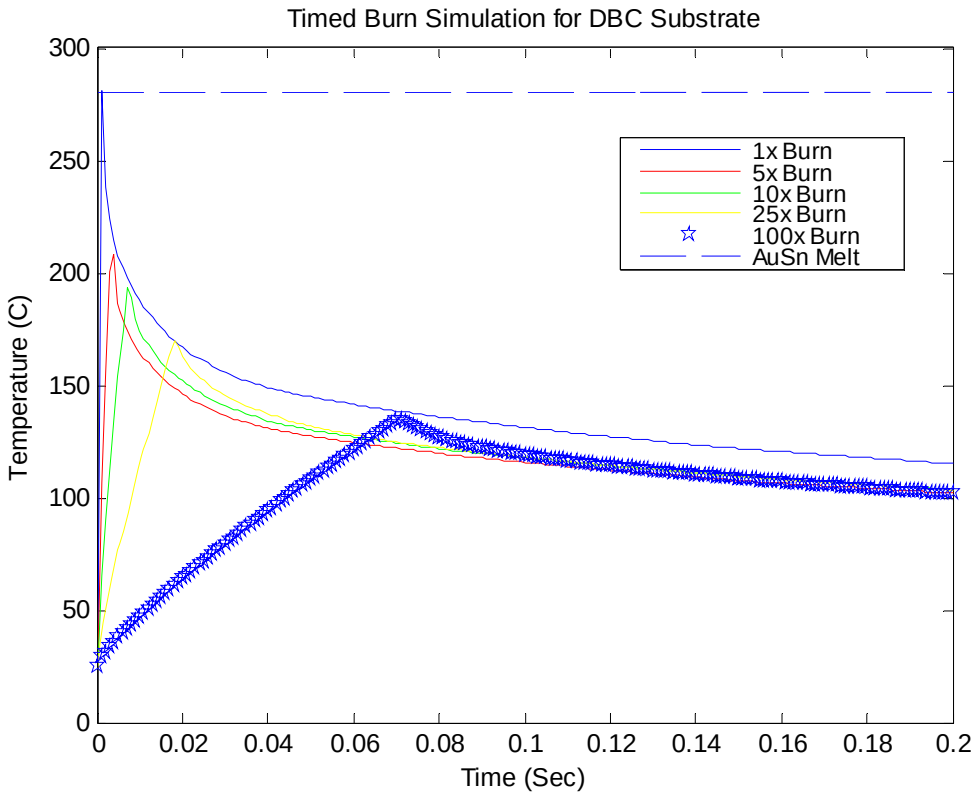


Figure 20: Timed burn simulation for DBC configuration

In an attempt to create a longer reaction the propagation velocity was decreased lengthening the time for energy release and this in turn decreased the power produced. This reduction in power led to a lower volumetric heat generation which is reflected above as none of the slower burning foils reached temperatures above 280º C.

4.1.2: Pre-heated Simulations

Since the primary concern with sample fabrication seemed to involve time above liquidus for the solder layers, a method involving pre-heating the die stack was simulated to see if significant improvements would be seen. Given the simulation properties from chapter 2 and adjusting initial temperatures, new temperature profiles

were obtained. The four plots below show the substrate/solder and die/solder interfaces for both the DBC and stainless steel substrates. Figure 21 and Figure 22 show DBC samples and Figure 23 and Figure 24 show stainless steel samples. These particular samples were preheated to 100º C

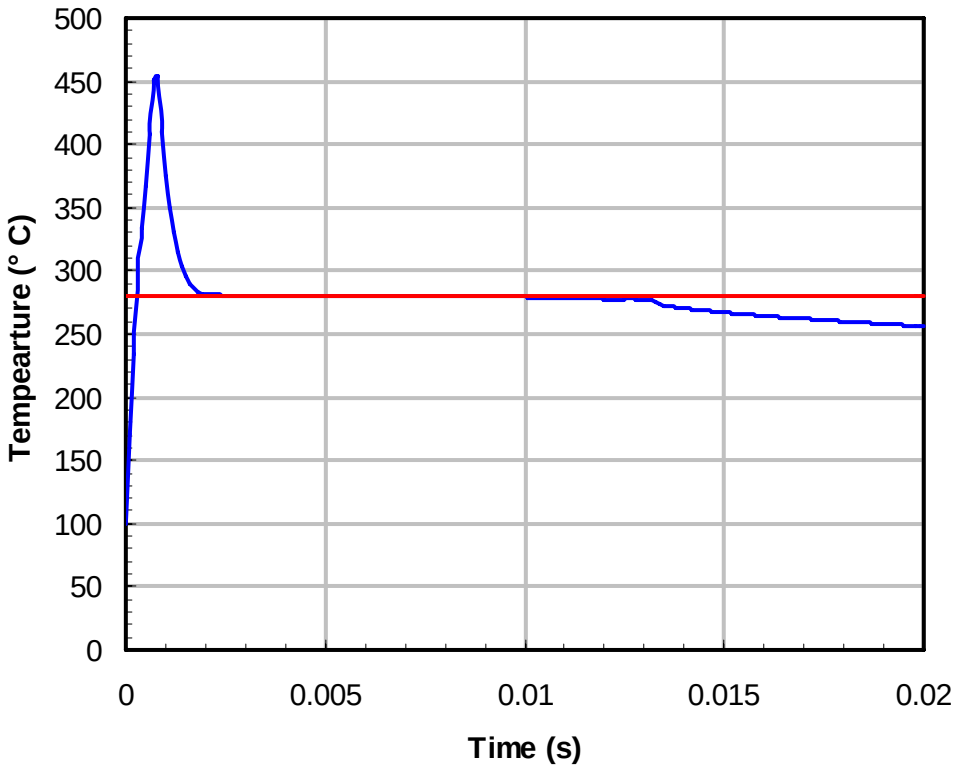


Figure 21: Preheated solder to die interface with DBC substrate

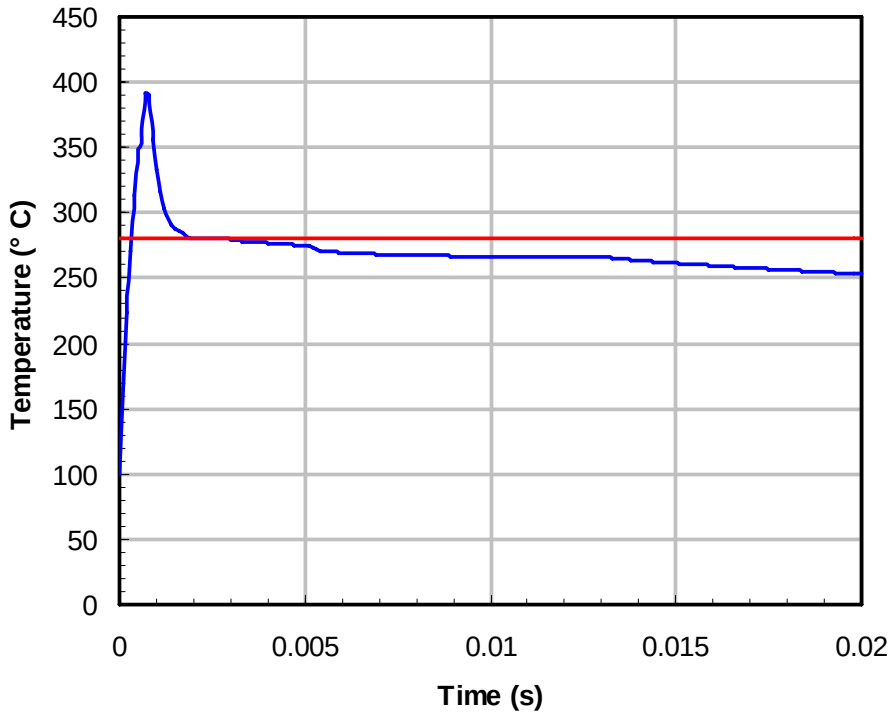


Figure 22: Preheated solder to substrate interface with DBC substrate

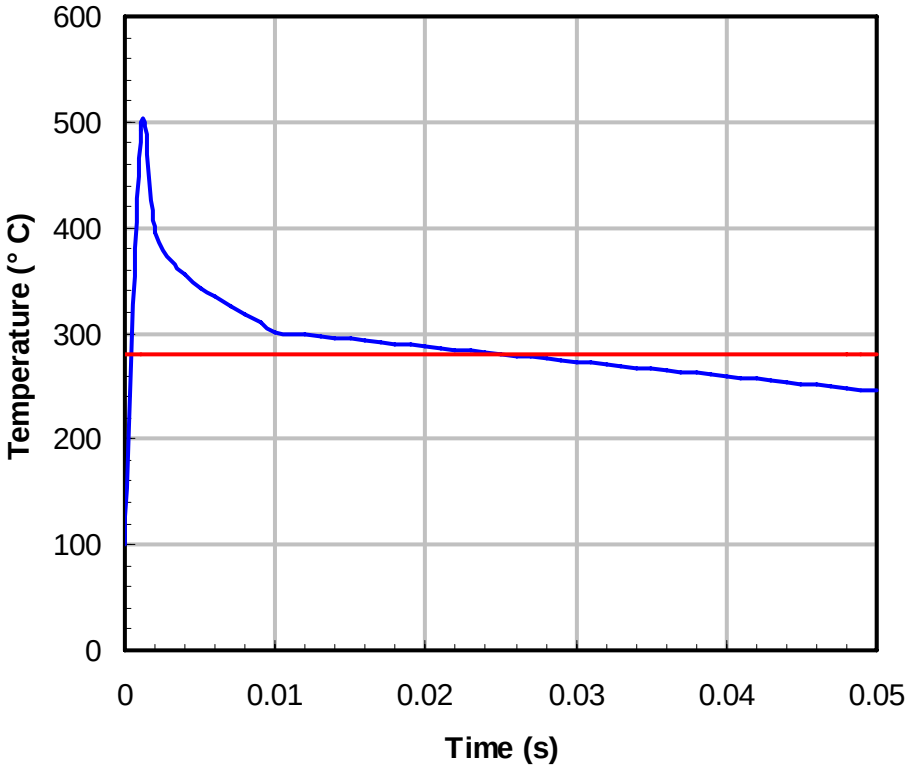


Figure 23: Preheated solder to die interface with stainless steel substrate

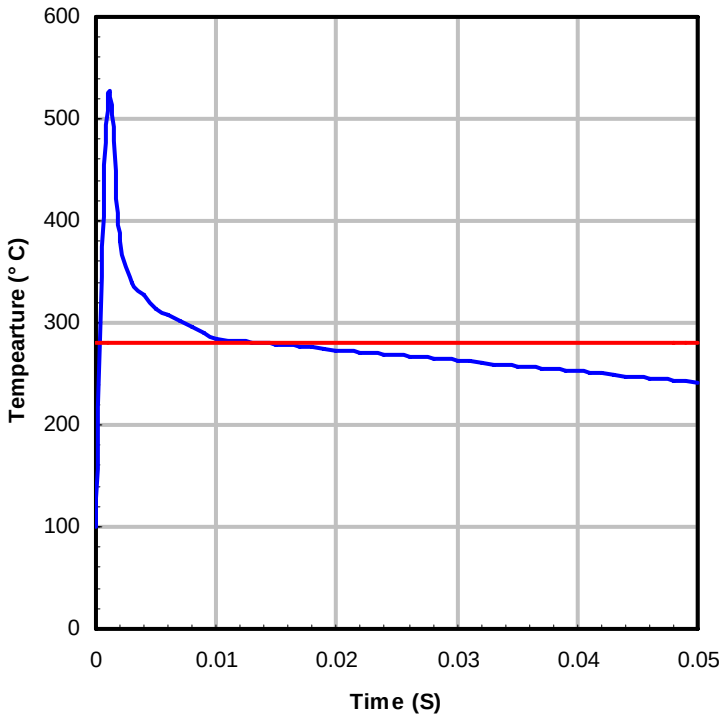


Figure 24: Preheated solder to substrate interface with stainless steel substrate

The preheated thermal simulations show that the solder to die and solder to substrate interfaces are above the AuSn melting temperature for periods of approximately .0097 seconds and .0029 seconds for the DBC samples, and .0266 seconds and .0147 seconds for the stainless steel samples respectively. As compared with the initial simulations, the preheated method keeps the solder layers above 280 ºC for more than 5 times as long in the DBC samples, and over 10 times as long in stainless steel samples. The table below summarizes how the solder interfaces will behave based upon different preheating temperatures.

Table 7: Affect of preheat on time above solder liquidus

	Stainless Steel		**DBC**	
Preheat Temperature (ºC)	AuSn/Sub. (Time above 280 ºC)	AuSn/Die (Time above 280 ºC)	AuSn/Sub. (Time above 280 ºC)	AuSn/Die (Time above 280 ºC)
0	.0012 sec	.0012 sec	.0005 sec	.0018 sec

50	.0026 sec	.0096 sec	.0009 sec	.0030 sec
75	.0048 sec	.0124 sec	.0019 sec	.0059 sec
100	.0147 sec	.0266 sec	.0029 sec	.0097 sec
150	.0430 sec	.0507 sec	.0187 sec	.05 sec
200	.0672 sec	.1049 sec	.2862 sec	.2959 sec

These simulation results show that even a small increase in initial temperature had an impact on the transient thermal properties of the AuSn interfacial layers. The effect of different preheat temperature is shown graphically below in Figures 25 and 26.

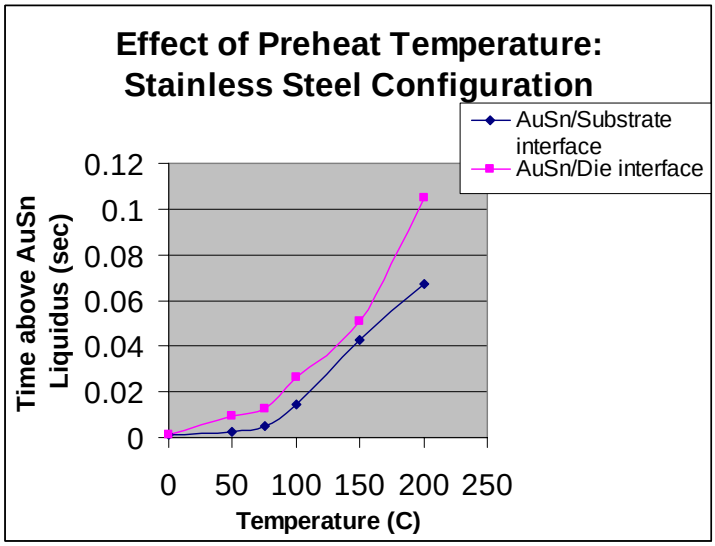


Figure 25: Stainless steel effect of preheat temperature summary

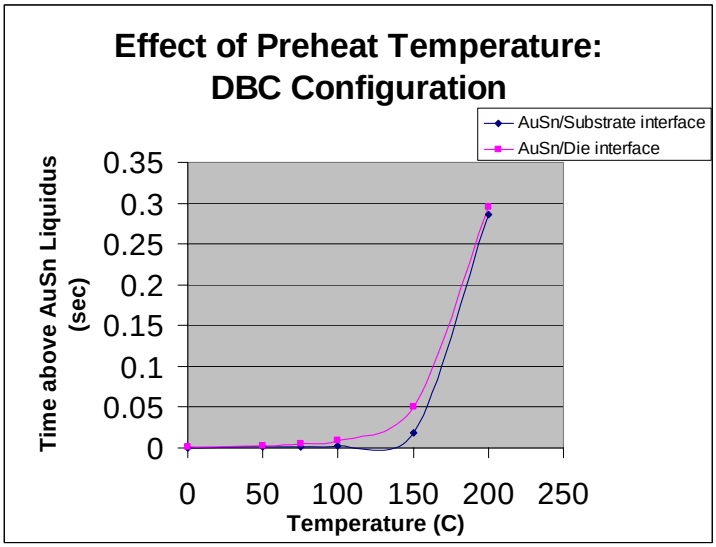


Figure 26: DBC effect of preheat temperature summary

4.2: Pre-heated Sample Creation

In an attempt to improve the joining process and verify the pre-heated simulations a hot plate was used to increase the initial temperature of the die stack. The sample creation process remained the same as previously described except that after the pressure was applied the die stack was allowed to sit on a small hot plate until the sample reached equilibrium at the desired temperature (Figure 27).

Figure 27: Hotplate used to preheat samples

To assure the samples were at the appropriate temperatures an infrared non-contact thermometer was used to take measurements (Figure 28).

Figure 28: Non-contact thermometer

After samples were created the hot plate was turned off and the sample was allowed to cool while remaining on the plate for several minutes (Figure 29). This extra cooling time was taken to minimize the stress to the samples induced through thermal shock due to the temperature gradient between the hot plate and ambient air.

Figure 29: New experimental set up

As expected, the preheated samples showed far greater wetting than the unheated samples. From earlier experimental results it was determined that 50 psi of pressure would be used in all sample fabrication to reduce die cracking. A preheat temperature of 100° C was chosen as it was the lowest temperature that provided enough extra heat to adequately melt the solder layers (observed experimentally). Initially three die sizes (3mm x 3mm, 5mm x 5mm, and 7.5mm x 7.5mm) were going to be examined for reliability however due to difficulty fabricating such small joints by hand only 5mm x 5mm and 7.5 mm x 7.5mm configurations were created. Anything above 7.5 mm x 7.5mm was highly susceptible to die cracking so the 5mm and 7.5mm were the only two configurations that were produced in large quantities. Additionally with the optimized processing characteristics as well as the set preheat temperatures determined, experimental focus shifted towards the power electronics oriented DBC substrates. One of the disadvantages of preheating the sample that was considered was the potential for the Au to oxidize at elevated temperatures. This oxide layer would have adverse affects on joint strength and electrical conductivity. The preheating joining process could have been carried out in an inert atmosphere to eliminate oxide from forming however this was deemed unnecessary as gold is a very noble metal and no adverse effects or oxide layer were observed. The various observations and experiments that were associated with these newly created samples are detailed in the following chapter.

Chapter 5: Sample Testing Results

5.1: Preheated Sample Characterization

The preheated samples were examined using a combination of optical microscopy, scanning acoustic microscopy, and x-ray imaging. Optical microscopy was used to examine the interfaces between the solder layers and the CSAM and X-ray were used to identify cracks and voids within the die stack. The following figures 30-32 show optical images of a joint cross section.

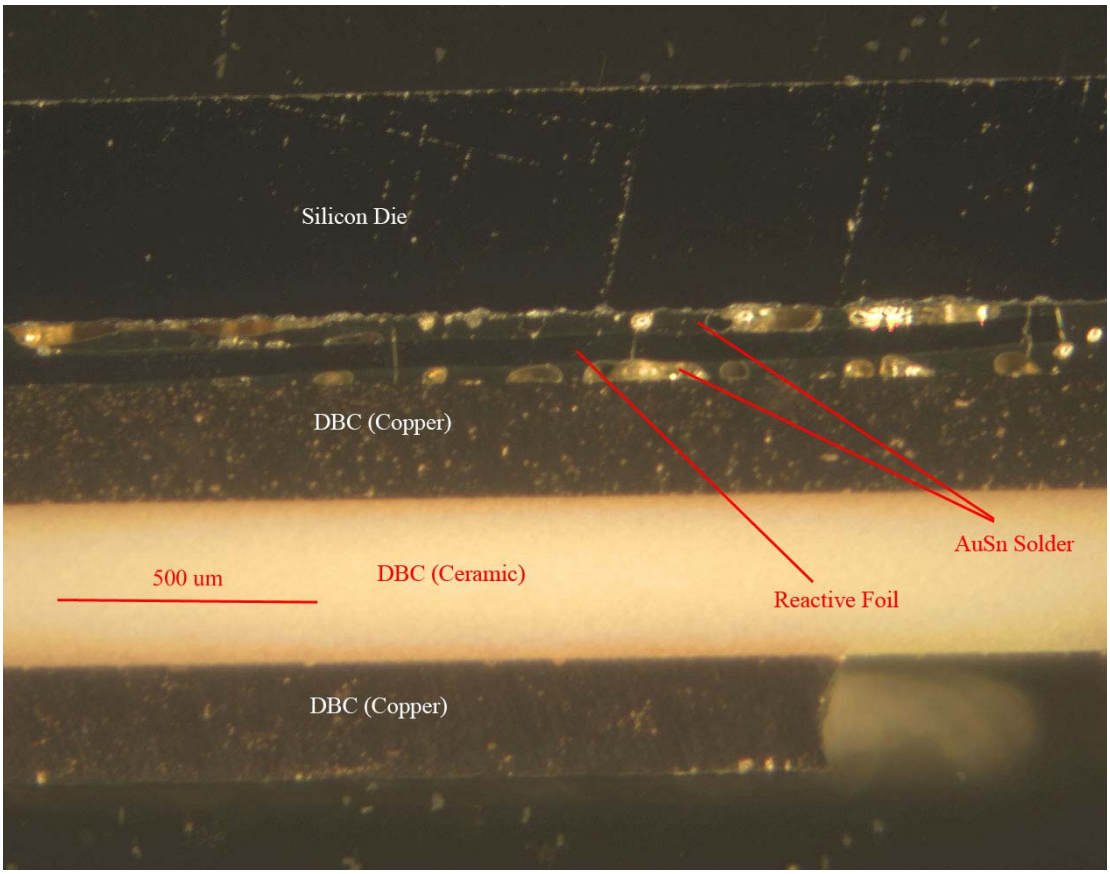


Figure 30: Optical cross section of completed sample

Figure 31: Voiding within completed samples

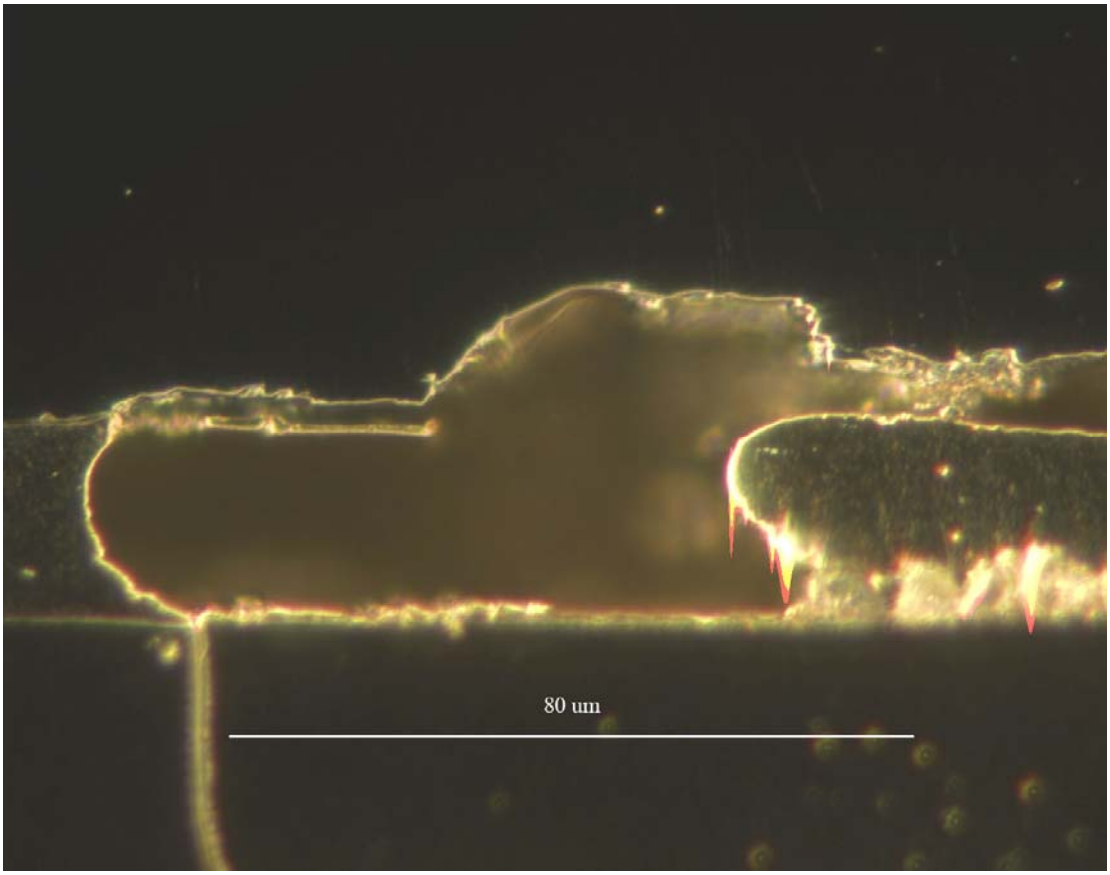


Figure 32: Detailed view of voiding in completed samples

The first optical image, Figure 30, shows the entire die stack with a continuous reacted foil and solder that fills the majority of areas at the die/foil and substrate/foil interfaces. The samples did not show complete bonding however as gaps were observed, particularly between the die and the solder. The gaps ranged in size with the largest being approximately 400 μm long. Figure 31 and Figure 32 show one of these gaps (circled in Figure 31) at different magnifications. The majority of these gaps were seen towards the center of the die, with the outer edges showing better adhesion.

To examine cracking and voiding in the system a combination of CSAM and x-ray were used. The CSAM was used for its' ability to take images at a variety of depths within the die stack and the x-ray was used to get an overall image. Figure 33 shows a CSAM image obtained with a 110 MHz transducer which represents the signal being reflected by the attach layer. Figure 34 is an x-ray image of the same sample.

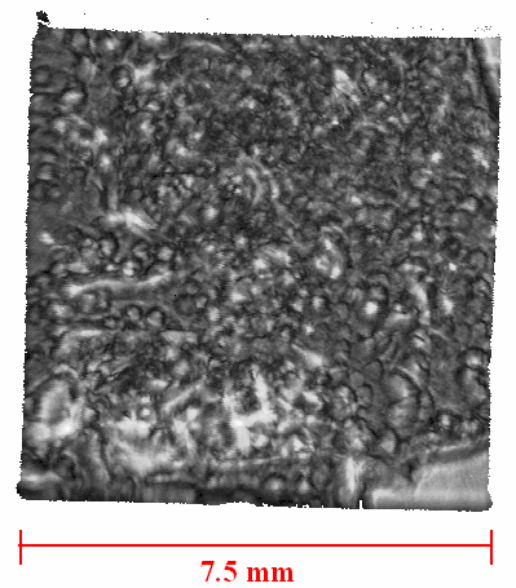


Figure 33: CSAM image of completed sample

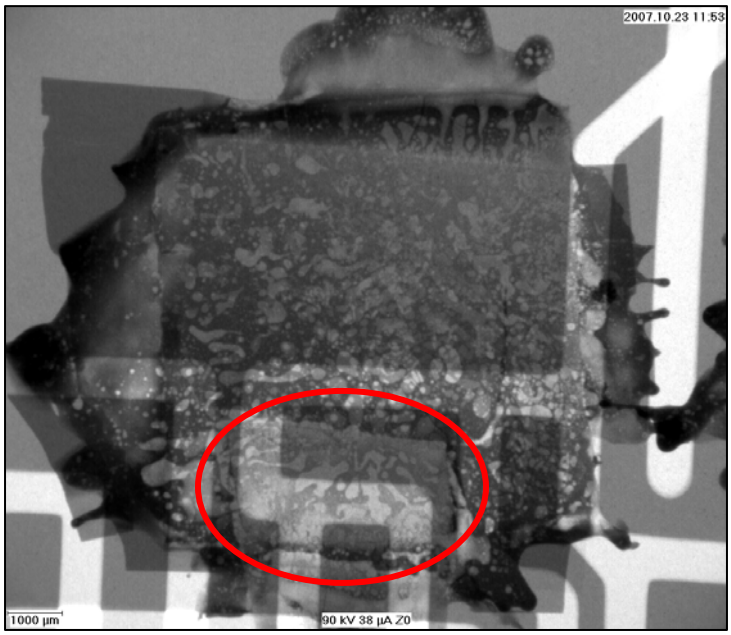


Figure 34: X-ray image of completed sample

Due to the multilayer nature and relatively small thickness of the attachment layer, the features from the CSAM image were very difficult to resolve. The x-ray images provided a much clearer view of the defects within the sample and also show a "fuse" (circled in Figure 34) which was a small piece of reactive foil that extruded out of the die stack to provide an easily accessible ignition point. It is important to note that the large white lines in the x-ray image were the patterning on the backside of the DBC substrate and were not features that were important in analyzing the samples. Although voiding appears fairly significant, samples made with the reactive foil were comparable to similar joints created with a AuSn solder paste and standard reflow profile, as shown in Figure 35 for a sample that was created using 80 wt% Au-20 wt% Sn eutectic solder paste in a furnace. The temperature profile that was used to create this standard reflow sample is also seen in Figure 36. This particular profile was derived from the recommended profile given by Indium Corporation of America for standard reflow processes with eutectic AuSn solder paste [20].

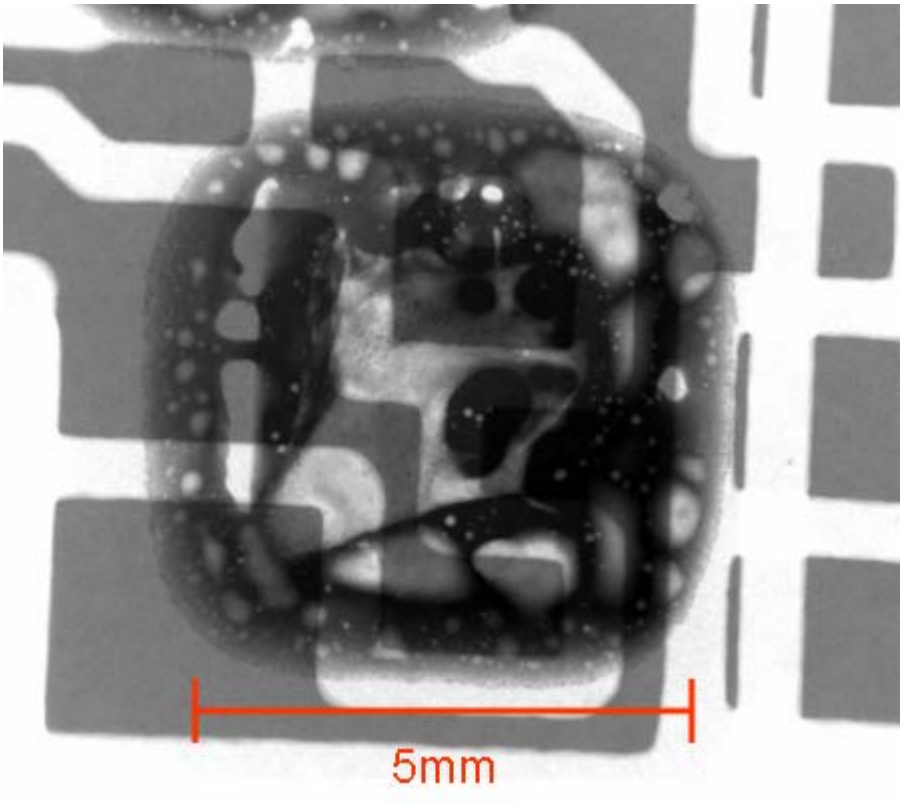


Figure 35: X-ray image of sample created using standard reflow process

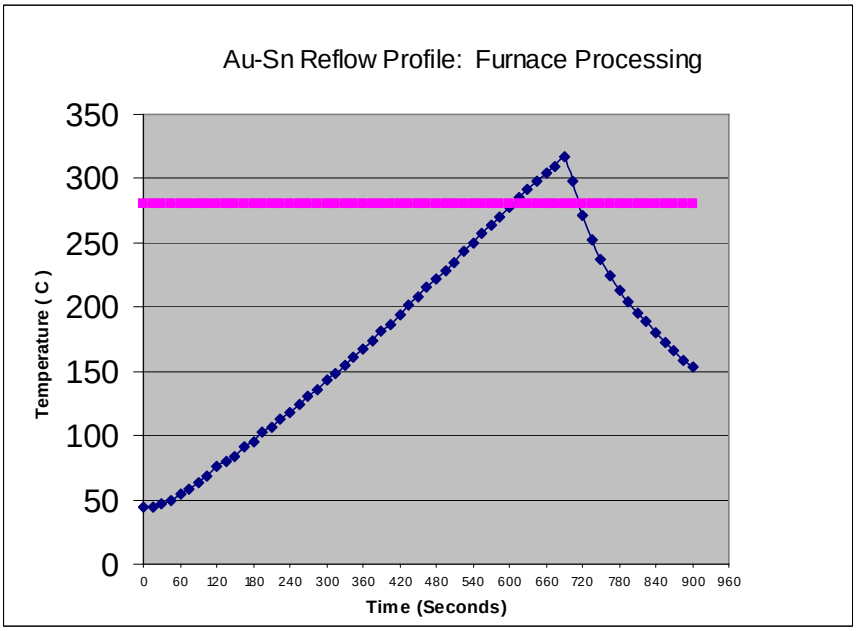


Figure 36: Temperature profile used during standard reflow process

It is important to note that although both the standard reflow process and the reactive joining process show visible defects within the joint, neither one shows a significant advantage with regard to voiding. The voiding within the reactively joined sample appears more widely spread, while the voids are larger in the standard reflow samples. This is a promising result given that standard reflow processes are employed by much of the electronics industry.

5.2: Shear Strength Results:

Initial assessment of joint mechanical integrity was conducted using a die shear test based upon Mil-Std-883 Method 2019. This test determines the strength of adhesion of a semiconductor die to the package's substrate (such as the die pad of a lead frame or the base of a hermetic cavity package), by subjecting the die to a stress that is parallel to the plane of die attach substrate, resulting in a shearing stress at: 1) the die-die attach material interface; and 2) the die attach material-substrate interface [21]. Four 7.5 mm x 7.5 mm and four 5 mm x 5 mm samples were tested by being placed in a Dage 2400 shear tester with a DS 25 kg-F load cell. The test was set to "destructive" with a speed of 200 μm/s and a test height of 200 μm. All eight of the sample readings surpassed the 25kg limit of the load cell and began to show signs of chipping of the silicon die. This phenomenon suggests that the attach layer is quite strong and that the silicon would be the first component to fail under excessive loading. All of the joints that were tested went well beyond the required load threshold for acceptable die attach as outlined in Mil-Std-883 [21].

5.3: Reliability Testing:

To assess the reliability of these samples, they were thermally cycled in an environmental chamber from -55 °C to 150 °C with a 10 minute dwell at 150 °C and a 5 minute dwell at -55 °C. Overall eleven 5mm x 5mm dies and ten 7.5mm x 7.5 mm dies were thermally cycled. A combination of visual inspection and x-ray were used to examine the samples at various cycling intervals throughout the course of this test. After only 50 cycles, the majority of the samples showed significant die cracks that were visible to the naked eye. Although die cracking would be a critical issue in power electronics, samples that showed die cracking but remained affixed to the substrates were noted and then allowed to continue cycling. For the purpose of this test, failure was defined as partial detachment of the die from the substrate. Upon removing the samples from the chamber for visual inspection every 50 cycles, a slight pressure (applied by pushing on the die with a fingertip) would be applied to the remaining affixed die to ensure adhesion. After 200 cycles, 7 out of a total of 21 samples had failed (four 5 mm x 5 mm die and three 7.5 mm x 7.5 mm die), all due to die cracking, with die breaking into several pieces in most instances. At 400 cycles, 13 out of a total of 21 samples had failed, with the remaining 8 samples showing large die cracks (approximately 2mm to 5mm in size) visible to the naked eye. Of these 13 completely failed joints, 9 were the 5 mm configuration and 4 were the 7.5 mm configuration. Cycling was stopped at this point as it was determined that the main cause of failure was due to die cracking as opposed to thermal fatigue of the attach. A digital image of a typical failed sample can be seen in Figure 37.

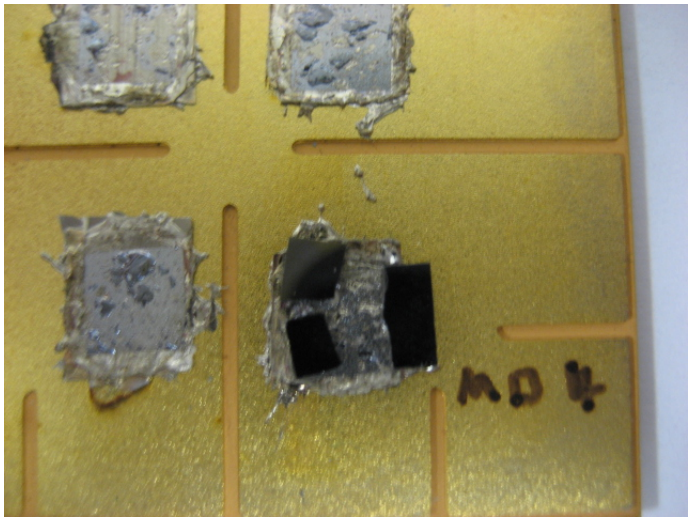


Figure 37: Failed joint after temperature cycling

Although x-ray was used at various time intervals to observe the thermally cycled samples it was deemed unnecessary as cracking occurred in as few as 50 cycles in some joints with failures being easily observed upon visual inspection . The chart detailing when each sample failed can be seen in the appendix. Although the preheated joints were successful as built their inability to withstand thermal cycling suggests several things. The first reason for seeing die cracking after such a low number of cycles may be attributed to the processing of the joint itself. The explosive nature of the reaction in such a confined and pressurized area may be causing incipient micro cracks in the silicon that are not readily visible. When thermally cycled these micro cracks could have grown causing more visible damage to the silicon. After examining the fracture surface of failed samples incipient cracking seems to be a distinct possibility as the backside of the die were pitted and chipped. Also, in the majority of the failed samples the attach layer remained attached to the substrate with the die being the only component to fail. Another possible explanation for this die cracking phenomenon could be due to the nature of the reactive foil itself.

The foil may be acting as a stiffener to the attach, thus transferring the thermal stresses induced by the cycling directly to the die as opposed to remaining in the attach material. Given the Young's Modulus range of both the AuSn solder and the reactive foil a quick calculation can be made to determine the approximate modulus of the combined attach layer based upon the volume percentages of the layers that make up the attach. As the combined modulus is greater than the modulus of the AuSn alone then stiffening due to the addition of the reacted foil may be a reason behind observing die cracking at a low number of thermal cycles. The Young's modulus for the reacted foil was determined using nanoindentation by atomic force microscopy (AFM). AFM is a scanning probe microscopy that generally uses a sharp scanning tip to measure local properties of a material. The AFM tip is driven by piezo-ceramics that expand or contract when in the presence of a voltage gradient [22]. These piezo-ceramics are very important as they allow for very precise positioning of the AFM tip. In contact mode the AFM uses feedback to regulate the force on the sample and tries to maintain a constant deflection between the tip and the surface by varying voltages. By identifying the contact point in force vs. separation dependence, separation can be converted to indentation. This force-indentation dependence can be used to extract the elastic modulus of the material. To obtain the modulus of the reactive foil a free standing piece was ignited and then analyzed using a Hysitron TriboIndenter nanomechanical testing system. The modulus was determined to be 56.35GPa. Given this data and the modulus of AuSn the combined effective modulus is calculated below.

$$Material_1 = AuSn$$
$$Material_2 = RNT$$
$$E_1 = 19.99GPa$$
$$E_2 = 56.36GPa$$

$$Areas\_are\_the\_same\_for\_foil\_and\_solder$$

$$t_1 = 100\mu m$$
$$t_2 = 80\mu m$$
$$t_{total} = t_1 + t_2 = 180\mu m$$

$$Vfraction_1 = \frac{t_1}{t_{total}} = .56$$
$$Vfraction_2 = \frac{t_2}{t_{total}} = .44$$

$$E_{Eff} = Vfraction_1 E_1 + Vfraction_2 E_2$$
$$E_{Eff} = (.56)(19.99Gpa) + (.44)(56.36Gpa) = 35.7GPa$$

$$E_{Eff} > E_1$$

This calculation is carried out assuming equal strain in both the reactive foil and the AuSn. If equal stress is assumed for both the reactive foil and the AuSn solder layers the following calculation can be carried out to obtain the lower bound of the modulus range [24].

$$E_l = Effective\_Modulus$$
$$E_m = AuSn\_Modulus$$
$$E_r = Foil\_Modulus$$

$$E_L = \frac{E_m E_r}{VolFrac_{AuSn} E_m + (1 - VolFrac_{Foil}) E_r}$$
$$E_L = \frac{(19.99)(56.36)}{(.56)(19.99) + (1 - .56)(56.36)} = 31.3Gpa$$

Since the effective modulus of the combined die attach is greater than the individual modulus of the AuSn under both constant strain and constant stress conditions die cracking due to stiffening of the sample is one possible explanation.

Chapter 6: Conclusions

6.1: Conclusions

The results presented in this thesis show that successful joints were created using an Al/Ni reactive foil as a localized heating source. Theoretical and experimental results revealed several important factors with regards to this particular joining process:

1. The amount of time the solder layers stayed above their melting temperatures was critical to propagation of the melting front and wetting. A new preheating method was employed and sample quality was greatly improved. Samples created using this new method were far more successful than joints attempted without a preheat and exhibited much better wetting.

2. Another key issue that this work uncovers is die cracking. Along with the thermally cycled samples, most of the dies with applied pressures over 50 psi exhibited significant die cracking. It is this author's recommendation that 50 psi or less should be used for joining with this process. If the mechanism for die cracking in thermally cycled samples can be fully understood and prevented this joining method could be an excellent method to supplement more traditional soldering techniques.

3. Identified a failure mode in thermal cycling as die cracking. The AuSn solder did not fail and further work on incipient crack mitigation is necessary.

6.2: Suggestions for Future Work

1.) To attempt to reduce failures due to die cracking by examining the effects of introducing an extremely thin layer of a material with greater plasticity than AuSn into the stack. A very soft material such pure Au or In foil may allow the attach layer to be more compliant, thus reducing thermal stresses transferred from the die to the substrate.

2.) To carry out actual electrical testing to see what effects, if any, this joining process has on the electrical properties of this system. Additionally electrical testing would be an excellent way to monitor whether or not incipient die cracks exist within the silicon die after joining.

3.) Investigate directly depositing reactive layers onto the backside of a die or a substrate to see what effect this has on the joint as a whole. Various depositing techniques could be examined and evaluated for potential future use in joining of this nature.

6.3: Contributions

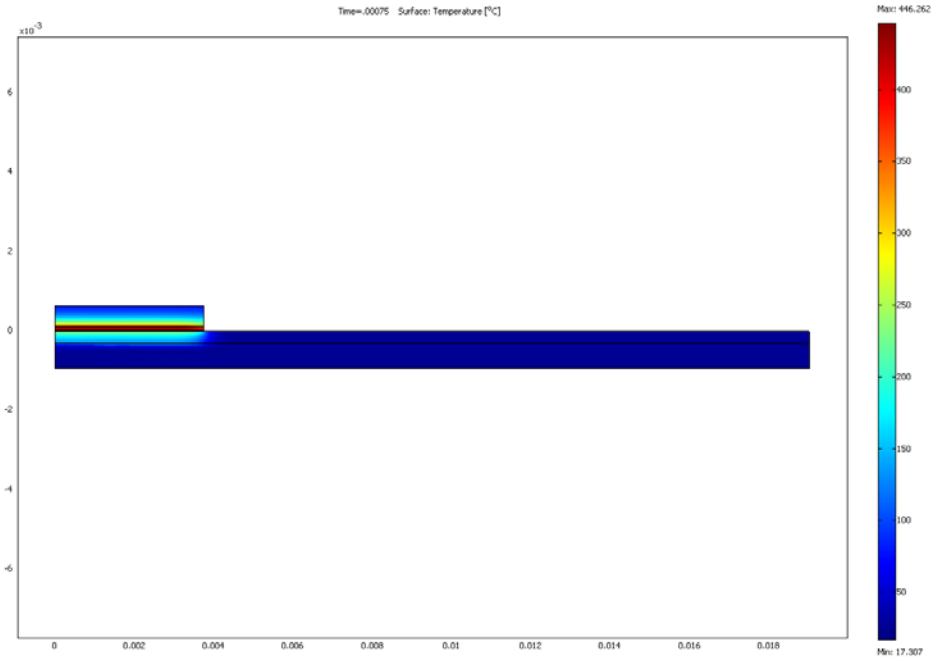
1. First use of reactive foil to form a AuSn high temperature solder joint in an actual power electronics structure (appropriate die size, use of DBC substrate)

2. Developed a preheating process and established pressure parameters to improve joint mechanical integrity using a reactive foil.

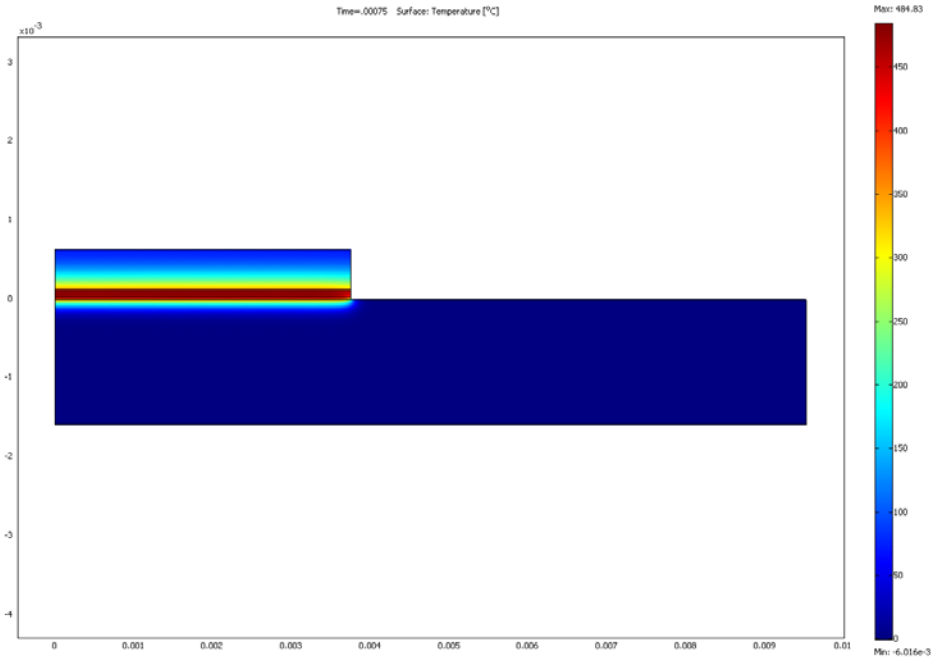
3. First identification of die cracking as a failure mode in thermally cycled joints created using a reactive multilayer foil as a localized heating source.

Appendices

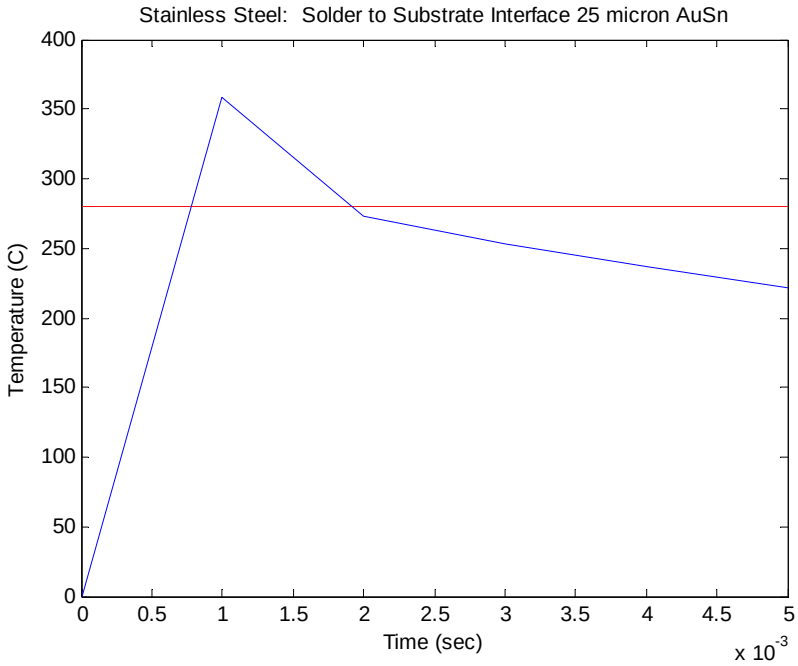
25 Micron AuSn Simulations



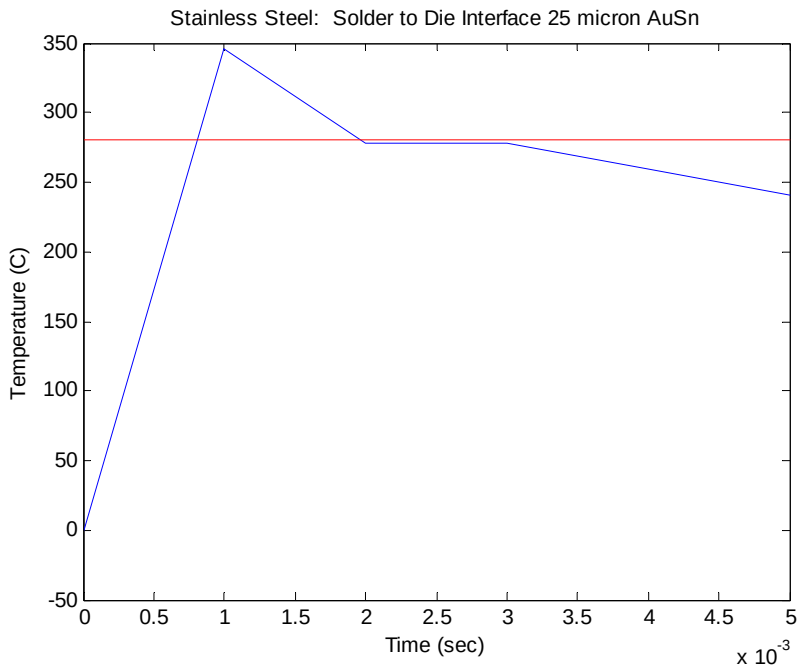
DBC substrate with 25 micron solder at reaction completion



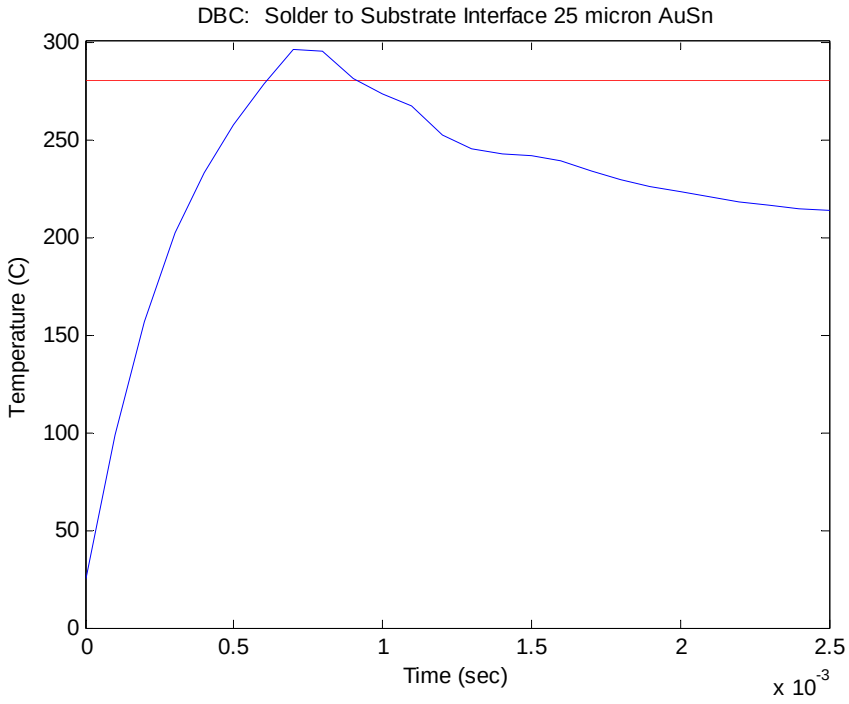
Stainless steel substrate with 25 micron solder at reaction completion



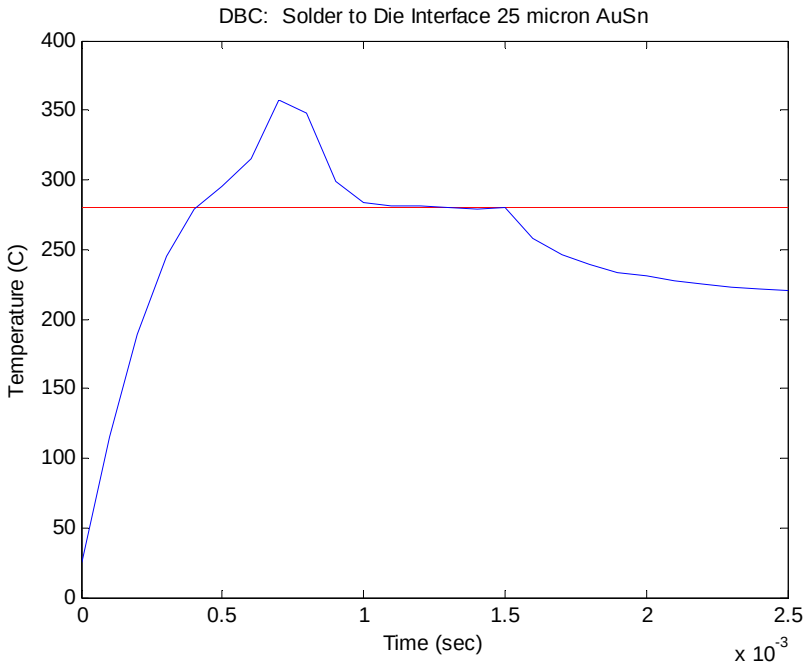
Stainless Steel Solder to substrate interface with 25 micron solder layers and no preheating.



Stainless Steel Solder to die interface with 25 micron solder layers and no preheating.



DBC Solder to substrate interface with 25 micron solder layers and no preheating.



DBC Solder to die interface with 25 micron solder layers and no preheating.

Cycling Raw Data

(LT): Program P4 -55 - 150 (Delta T = 205) 10 min Dwell at Tmax, 5 min Dwell at Tmin, 5C/min, Total cycle time = 1.62 hours, Tmean = 47.5C

Sample	In	Hold	# Cycles	In	Hold	# Cycles	In
S1(MD1)	3-Mar	7-Mar	Failed at 50				
S2(MD2)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S3(MD3)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S4(MD4)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S5(MD5)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S6(MD6)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S7(MD7)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S8(MD8)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S9(MD9)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S10(MD10)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S11(MD11)	3-	7-	50	24-Mar	28-Mar	100	31-Mar

	Mar	Mar					
S12(LD1)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S13(LD2)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S14(LD3)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S15(LD4)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S16(LD5)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S17(LD6)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S18(LD7)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S19(LD8)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S20(LD9)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar
S21(LD10)	3-Mar	7-Mar	50	24-Mar	28-Mar	100	31-Mar

Hold	# Cycles	In	Hold	# Cycles	In	Hold	# Cycles	In
4-Apr	150	7-Apr	11-Apr	Failed at 200				
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	Failed at 250	
4-Apr	150	7-Apr	11-Apr	Failed at 200				
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	Failed at 200				
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	Failed at 200				
4-Apr	150	7-Apr	11-Apr	Failed at 200				
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	200	14-Apr	18-Apr	250	21-Apr
4-Apr	150	7-Apr	11-Apr	Failed at				

				200				

Hold	# Cycles	In	Hold	# Cycles	In	Hold	# Cycles
25-Apr	300	28-Apr	2-May	350	5-May	9-May	Failed at 400
25-Apr	300	28-Apr	2-May	350	5-May	9-May	Failed at 400
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	Failed at 300						
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	Failed at 300						
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	300	28-Apr	2-May	350	5-May	9-May	400
25-Apr	Failed at 300						

Testing at 400 cycles was stopped because all remaining dies showed visible cracks. Stresses were not being transferred through the attach materials.

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