Two Transistor Synapse with
Spike Timing Dependent Plasticity

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Abstract— We present a novel two transistor synapse ("2TS") that exhibits spike timing dependent plasticity ("STDP"). Temporal coincidence of synthetic pre- and post- synaptic action potentials across the 2TS induces localized floating gate injection and tunneling that result in proportional Hebbian synaptic weight updates. In the absence of correlated pre- and post-synaptic activity, no significant weight updates occur. A compact implementation of the 2TS has been designed, simulated, and fabricated in a commercial 0.5 µm process. Suitable synthetic neural waveforms for symmetric STDP have been derived and circuit and network operation have been modeled and tested. Simulations agree with theory and preliminary experimental results.

Figure 1. Biological spike timing dependent plasticity; figure from [1], [2].

I. INTRODUCTION

In biology, spike-timing-dependent-plasticity ("STDP") describes the potentiation or depression of synaptic connections between neurons according to the coincidence of pre- and post-synaptic action potentials. It has been experimentally observed that when a pre-synaptic action potential is followed within some time (typically on the order of ms) by a post-synaptic action potential, the strength of the synaptic connection between the two neurons is increased in proportion to the coincidence of the firing times (or equivalently in inverse proportion to the time between firings). Conversely, it has been shown that when a pre-synaptic action potential follows within some time (typically on the order of ms) a post-synaptic action potential, then the strength of the synaptic connection between the two neurons is decreased in proportion to the coincidence of the firing times (in inverse proportion to the time between firings). These rules which predict the potentiation and depression of synaptic weights and which together give rise to STDP are known as Hebbian learning. The concepts are graphically illustrated in a plot of biological data shown in Figure 1, as adapted from [1] by [2].

While the biological mechanisms of STDP have not been fully elucidated, they represent a ubiquitous and important mode of neural adaptation and learning. Therefore, in order to begin to realize electronic analogues of rudimentary cortica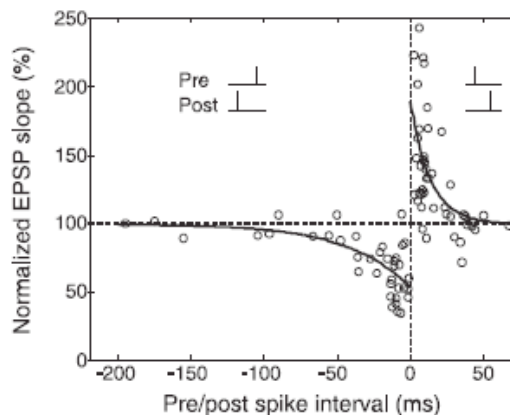l functions, we must develop synaptic mechanisms that incorporate STDP-like behavior. Furthermore, in order to accurately synthesize even the simplest neural architectures, STDP synapses must be realized in ultra-compact form with very high integration density. As a first step down that path, we have developed a two transistor synapse for implementing biologically realistic STDP. Section II of this paper describes the two transistor synapse circuit and physical layout. Section III details the derivation and implementation of the neural waveforms used to induce STDP. Section IV depicts simulation and experimental results, including examples of experimentally demonstrated Hebbian weight updates and a spike sorting application; and Section V concludes and briefly discusses future directions.

II. TWO TRANSISTOR SYNAPSE

A. Circuit Design

There are several reported single, [9], and two-transistor synapses, [4]-[8], some of which are programmable [3], [7], [8]. Further, there are reported STDP synapses that comprise many transistors [10], [11]. However, because the 2TS employs the same control signals to concurrently update

synaptic weights and to pass information between pre- and post- synaptic nodes, as in biological systems, the 2TS is both simpler and smaller than any other integrated STDP realization.

The two transistor synapse ("2TS") comprises two PFET transistors with a floating gate node that is common to both. Figure 2 shows a circuit schematic of one 2TS configuration wherein the "pre"-synaptic signal is asserted at both PMOS sources, and the "post"-synaptic signal defines the potential of the drain of the programming transistor on the left. The PFET on the right passes current generated by "pre"-synaptic spikes to the integration node, or soma, of the post-synaptic neuron (not shown). The body of the programming transistor on the left is connected to the source, while the body of the right transistor is held at a fixed potential.
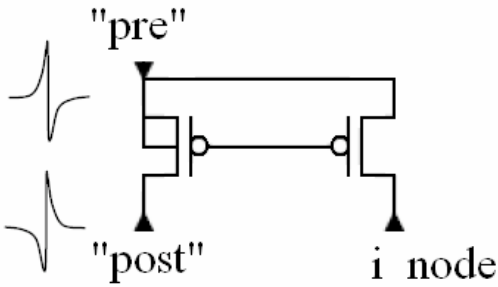

Figure 2. 2TS with labeled nodes and illustrative input waveforms.

In theory, the operation of the 2TS circuit is relatively straightforward. PRE and POST synaptic waveforms are asserted at the corresponding labeled nodes. If PRE occurs first, but POST occurs within some prescribed time of PRE, then PRE and POST will overlap resulting in a large transient difference in the source-drain voltage of the programming transistor causing hot electron injection to decrease the stored voltage on the floating gate and thereby increase the synaptic weight. On the other hand, when POST occurs first, but PRE occurs within some prescribed time of POST, then PRE and POST will overlap at a high voltage causing Fowler-Nordheim tunneling to increase the stored voltage on the floating gate and thereby decrease the synaptic weight. (See Appendix A).

In practice, circuit operation is more intricate. We rely on an implicit injection threshold to avoid significant positive weight updates in the absence of PRE/POST overlap. This operating assumption follows from the characteristic exponential relationship between the injection current and programming transistor source to drain voltage, which we shall discuss in greater detail in Section IV. Likewise, we rely on the fact that when the drain of the programming transistor is held low, a transient PRE overvoltage that is also coupled to the body of the programming transistor will not generate significant negative weight updates. Preliminary experimental results indicate that holding the drain voltage on the programming transistor several volts below the programming threshold voltage reduces the field across the oxide sufficiently to adequately suppress tunneling. As we shall discuss in Section IV, STDP PRE and POST waveforms may be biphasic symmetric, similar to the as in the sketched

waveforms in Figure 2, or alternately may be a combination of uniphasic and biphasic signals.

B. Physical Layout

There are many factors in the physical realization which will impact the layout of the 2TS. Among the most significant of these are the gate length of the programming transistor, which can mitigate short-channel effects, and the doping density of the source and drain regions, which impact local field strength and carrier transport. However, while such considerations are important for optimization of the structure and function, for a proof-of-principle implementation, we have fabricated a simple symmetric 2TS in a commercial 3-metal, 2-poly, 0.5 μm process, as shown in Figure 3. Each of the six terminals of this 2TS is connected to a separate pad for testing.
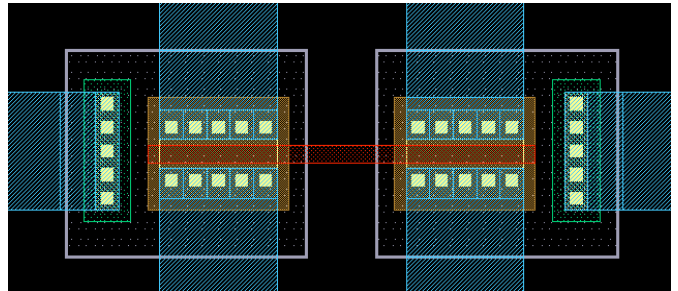

Figure 3. Physical layout of a 2TS in a commercial 0.5 μm process.

The non-optimized proof-of-principle layout has a fairly large footprint at just under 400 μm². However, we estimate that a minimum-sized variant of the 2TS satisfying design rules in a commercial 90 nm process consumes less than 6 μm² of real estate; we have submitted a 90 nm 2TS for fabrication. Allowing both PFETs to share the same well would reduce the minimum dimensions even further; our model simulations and experimental characterizations of tunneling behavior in fabricated devices suggest that it may be possible to place both transistors of the 2TS in the same well without significantly compromising operation. With modern lithographic techniques extending integrated circuit technologies deep into the nanometer regime, a sub-micrometer 2TS is technically feasible.

III. NEURAL WAVEFORMS

There are an infinite number of potential waveforms that will yield positive and negative Hebbian weight updates when asserted across the 2TS, see, *e.g.*, [3]. However, the subset that can accomplish bidirectional Hebbian learning according to biologically realistic STDP rules is considerably smaller. In our work, we have developed and investigated two such classes of waveforms: (1) a uniphasic PRE signal and a biphasic POST signal; and (2) paired, mirror-symmetric biphasic PRE and POST signals. Integrated circuit architectures for implementing these types of signals have been previously reported, see, *e.g.* [11]. Below we describe how these two classes of waveforms yield STDP in the 2TS. We begin by describing the weight update mechanisms, which impose certain design constraints and features on suitable waveforms.

A. Weight Updates: Injection and Tunneling

Synaptic weight updates are accomplished by balanced hot electron injection and Fowler-Nordheim tunneling. Hot electron injection in MOSFETs is a function of transistor source- and gate- drain voltages, and has been empirically shown to obey the following relationship [12]:

$$I_{inj} = \alpha \cdot I_s \cdot \exp\left(-\frac{\beta}{(V_{gd}+\delta)^2} + \lambda \cdot V_{sd}\right) \qquad (1)$$

where α, β, and δ are experimentally derived process dependent constants, I_s is the source-drain current flowing through the transistor, and V_{gd} and V_{sd} are the voltages across the gate-drain and source-drain regions, respectively. For a relatively constant gate voltage, the exponential dependence of the injection current on the source and drain voltages, allows us to determine a threshold voltage below which no significant (< 1% of max.) injection occurs.

Similarly, Fowler-Nordheim tunneling in MOSFETs exhibits an exponential dependence on the voltage across the oxide barrier that is given by [12]:

$$I_{tun} = -I_{tun0} \cdot WL \cdot \exp\left(-\frac{V_f}{V_{ox}}\right) \qquad (2)$$

where I_{tun0} is a pre-exponential current, V_f is a process-dependent constant, and V_{ox} is the voltage across the oxide barrier. For our semi-empirical modeling, we have computed V_{ox}, to first order, as representing a weighted average of source, body and drain voltages. This simplification discounts localized potential differences and barrier reduction to some degree, although experimental data suggests that it is a reasonable approximation in test devices.

B. Waveform Derivation

We constructed waveforms to accomplish STDP on biologically realistic timescales subject to the physical constraints imposed by the learning mechanisms described above. The first class of candidate waveforms we considered comprised pairs of uniphasic PRE and biphasic POST signals, one set of which is illustrated in the top trace of Figure 4. Simulations performed with this class of waveforms using extracted tunneling and injection process parameters demonstrated the desired updates, as illustrated in the bottom trace of Figure 4, where correlated tunneling and injection are precisely balanced over a period with no net change in weight.
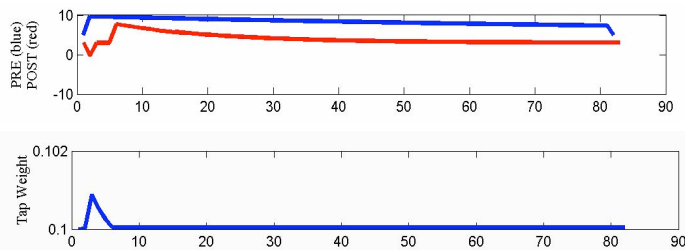

Figure 4. Top: Asymmetric PRE (blue) and POST (red) signals; Bottom: Resulting voltage on floating node represents weight update.
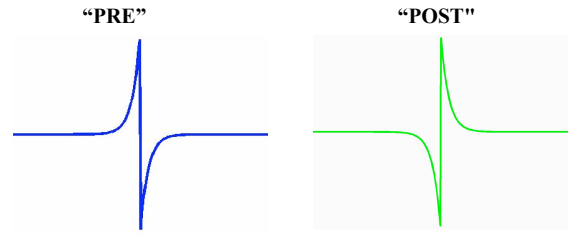

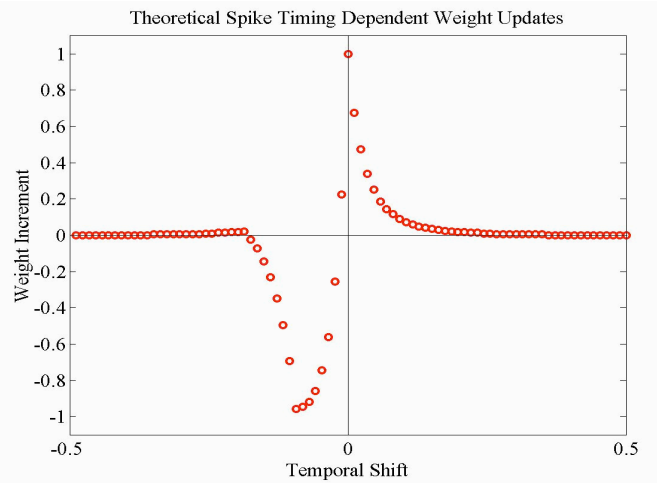Figure 5. Ideal discrete PRE and POST synaptic spike waveforms.

Figure 6. Simulated STDP as a function of biphasic mirror-image input waveforms. Computed weight update is shown in red.

However, the asymmetry and long-time constants of these waveforms did not pose an ideal solution, and so we developed a second class of candidate waveforms comprising mirror-symmetric, biphasic PRE and POST signals. Since tunneling and injection are both exponential functions, a variant of the exponential STDP curve itself was used as a starting point for the PRE signal. Then, in order to produce the desired Hebbian updates – that is, to balance the positive and negative increments for correlated PRE and POST signals, strengthening synaptic connections when PRE precedes POST and weakening them when PRE follows POST – the POST signal was taken as the mirror-symmetric, biphasic version of the PRE signal. This was confirmed by linear analysis; the PRE and POST signals shown in Figure 5 yield the biologically realistic STDP curve shown in Figure 6.

In Figure 6, each point in the STDP curve represents the integration of the injection and tunneling contributions at a single instant in time as the PRE and POST waveforms are convolved past one another. For this simulation, both mechanisms were assumed to contribute currents and corresponding weight updates that increase exponentially beyond the relevant threshold voltage (source-drain voltage for injection and oxide voltage for tunneling). For simplicity, the exponential coefficients were taken to be the same for injection and tunneling although they differ in actual circuits. Likewise, tunneling and injection thresholds for these simulations were selected to balance the positive and negative weight updates and represent theoretical, rather than experimentally derived, estimates. We are presently investigating more realistic empirical models for injection and tunneling.

IV. PERFORMANCE

A. Experimental Hebbian Learning

We have begun to experimentally characterize the performance of the 2TS using floating gate test structures that contain equivalent, but differently sized, transistors to the 2TS. Leaving all unused connections on these test structures (one poly control capacitor, one MOSCAP, and one NMOS follower) floating, see Appendix B, we asserted the biphasic waveforms as shown in Fig. 2 repeatedly at 100 Hz with PRE occurring at a small, fixed (~20 degrees) phase shift ahead of POST. Over 20 s, with an applied peak-to-peak voltage of approximately 10V, we observed the spiking output of the signal at the integration node shown in Figure 7, illustrating a small, but significant weight increment over time; we have highlighted the increment with a red trend line that follows the increase. Thus we see positive Hebbian learning using the biphasic PRE and POST inputs.

When we amplified the PRE and POST signals slightly, to approximately 13 volts peak-to-peak, and asserted them across the 2TS at 10 Hz, with POST preceding PRE by a similar phase shift over 50s, we measured the spiking output of the signal at the integration node shown in Figure 8. This data reflects a small, but significant weight decrement over time, consistent with negative Hebbian learning. Thus we have shown proof-of-principle Hebbian learning using the derived biphasic waveforms. We are presently characterizing the performance of fabricated 0.5 μm 2TS structures.
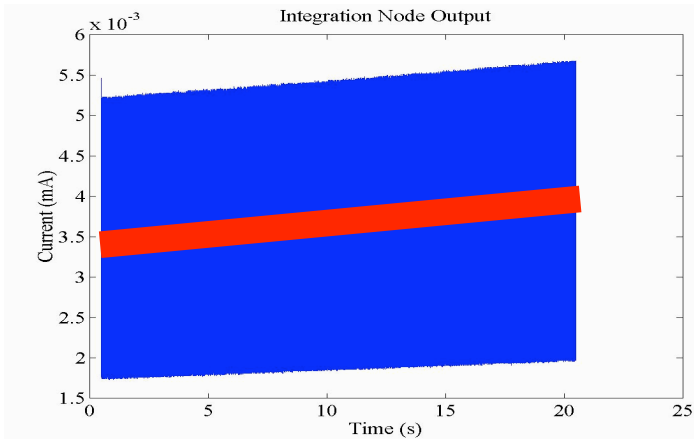

Figure 7. Measured output of circuit integration node as a function of successive positive Hebbian weight updates. Trend line shown in red.
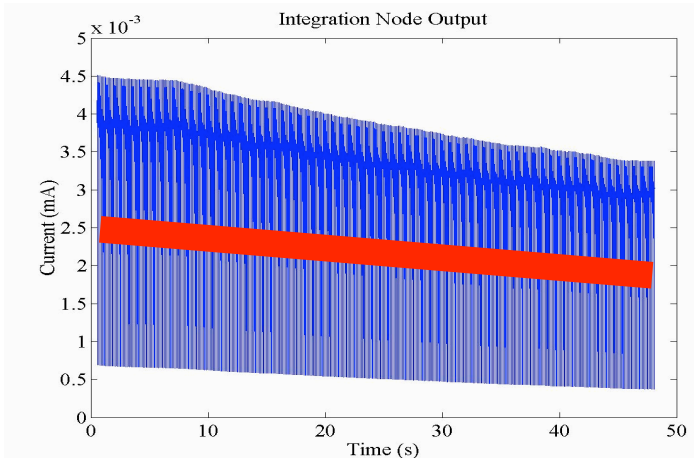

Figure 8. Measured output of circuit integration node as a function of successive negative Hebbian weight updates. Trend line shown in red.

B. Unsupervised Spike Sorting

As we briefly discussed in the introduction, STDP is ubiquitous in nature. One particularly interesting engineering application that leverages this technology is unsupervised template matching. More specifically, it is possible to employ a network of 2TS to register and learn correlations between extracted features of, *e.g.*, neural spikes, in real-time. Previously reported architectures for extracting salient features of neural action potentials and mapping them to biphasic spike trains exist [13]. Building upon this work and classical neural network theory we have begun to evaluate the performance of 2TS networks for unsupervised spike sorting.

V. CONCLUSION

We have presented a novel two transistor synapse that exhibits spike timing dependent plasticity in response to biphasic neural waveforms. We intend to continue this work by fully characterizing the fabricated 2TS circuits, and by further investigating the performance of the 2TS in neural network applications such as unsupervised spike sorting.

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In the case where the PRE synaptic spike occurs first and the POST synaptic spike occurs within some prescribed time of PRE, as denoted in the illustrative schematic Fig. 9a, the large difference in source-drain voltage results in a strong channel current and impact ionization. The vertical field at the drain causes some of these hot electrons to be injected onto the floating gate, see Fig. 9b, thereby decreasing the voltage on the gate and increasing the synaptic weight.
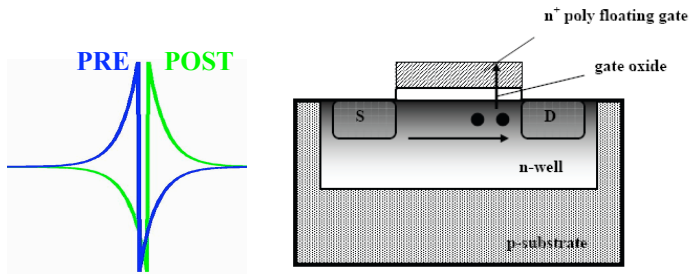

Figure 9: Left, 9a: PRE is applied to source and body of PFET; POST is asserted at PFET drain. Right, 9b: Cartoon of hot electron injection.

In the converse situation, when POST occurs first, but PRE occurs within some prescribed time of POST, as illustrated in the schematic Fig. 10a, then PRE and POST will overlap at a high voltage causing Fowler-Nordheim tunneling, see Fig. 10b, to increase the stored voltage on the floating gate and thereby decrease the synaptic weight.
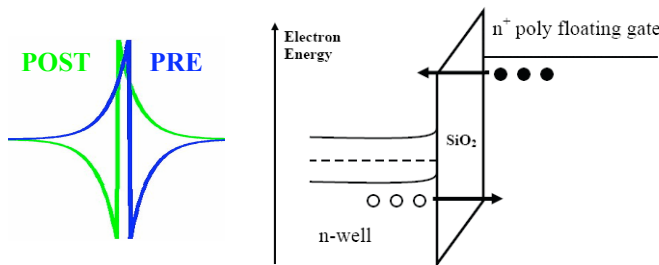

Figure 10: Left, 10a: PRE is applied to source and body of PFET; POST is asserted at PFET drain. Right, 9b: Cartoon of F-N tunneling.

As noted in the body of the text, the brief description and illustrations above do not completely describe the hot electron injection and F-N tunneling weight update mechanisms, nor do they fully depict the field induced carrier transport that actually occurs in fabricated devices. Instead, they represent a high level schematic of the basic operation of the 2TS, and illustrate how it is possible to generate STDP using this architecture. We are presently in the process of refining more realistic carrier transport models to further enhance the design and performance of our fabricated devices.

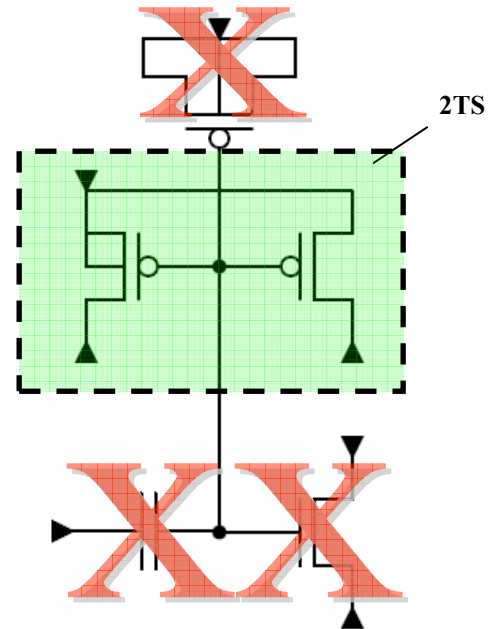A circuit schematic of the test structure we characterized is shown below:

Figure 11: Floating gate test structure characterized. Red X's indicate devices left unconnected, or floating.

Transistors and capacitors which are crossed out (by the red x's) were left floating. We are presently characterizing the fabricated 0.5 μm 2TS.