ABSTRACT

Title of Document: A PLL BASED FREQUENCY SYNTHESIZER IN 0.13 μm SIGE BICMOS FOR MB-OFDM UWB SYSTEMS

Hsin-Che Chiang, Master of Science, 2007

Directed By: Professor Martin Peckerar
Electrical and Computer Engineering Department

With the growing demand for high-speed and high-quality short-range communication, multi-band orthogonal frequency division multiplexing ultra-wide band (MB-OFDM UWB) systems have recently garnered considerable interest in industry and in academia. To achieve a low-cost solution, highly integrated transceivers with small die area and minimum power consumption are required. The key building block of the transceiver is the frequency synthesizer. A frequency synthesizer comprised of two PLLs and one multiplexer is presented in this thesis. Ring oscillators are adopted for PLL implementation in order to drastically reduce the die area of the frequency synthesizer. The poor spectral purity appearing in the frequency synthesizers involving mixers is greatly improved in this design. Based on the specifications derived from application standards, a design methodology is presented to obtain the parameters of building blocks. As well, the simulation results are provided to verify the performance of proposed design.

A PLL BASED FREQUENCY SYNTHESIZER IN 0.13 μm SIGE BICMOS FOR MB-OFDM UWB SYSTEMS

By

HSIN-CHE CHIANG

Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Master of Science
2007

Advisory Committee:
Professor Martin Peckerar, Chair
Professor Neil Goldsman
Professor Pamela Abshire

Table of Contents

List of Figures

List of Tables

Acknowledgements

First of all, I would like to express my gratitude to my research advisor, Professor Martin Peckerar, for his guidance and patience. With his fully trust and constant encourage, not only my technical skills but also my personality grow fast in two years. I would also like to thank committee members, Professor Neil Goldsman and Pamela Abshire for their support and significant comments throughout the period of my research.

I am so indebted to my family and friends, who are always there for me. Especially thanks to my father and mother, Chiang and Lin, who give me full support about my decision in the whole life.

1

Introduction

1.1 Motivation

As the WiMAX standard is developed for "last mile connectivity" in the wireless environment, we will witness a wireless revolution in homes and in offices. In the emerging digital home environment [1], in addition to the personal computing devices, the number of consumer electronics and mobile devices is increasing. Obviously, the interaction among the devices in the digital home is unavoidable. For example, DV camcorders transfer files to the storage devices, and game platforms communicate with set-top boxes. However, currently, the interfaces of different devices are all different, that makes inter-system cable conflicts unavoidable. The only solution to this situation is the wireless connection.

To provide high throughput for multiple connections simultaneously and streaming of high-definition video streams in high speed, the communication with high data rates should be achieved. From the Shannon's capacity limit equation [2],

we know that higher bandwidth can lead to higher channel capacity more readily than higher signal to noise ratio (SNR) can do. Technology with higher bandwidth can get the same channel capacity consuming less power than systems with higher SNR. This implies that wideband technology offer the advantages of high data rate transmission and low power consumption, as compared to narrowband technology. Therefore, Ultra-Wideband (UWB) wireless technology is proposed.

The existing short-range wireless networking technologies are IEEE 802.11b/g (Wi-Fi), Bluetooth and Zigbee technologies. For the future demand of high data rates communication, the Bluetooth and Zigbee technology, which emphasizes on low power, are not well suitable. According to the cost and power hungry, Wi-Fi networking can't be implemented in all consumer electronics and mobile devices. As well, even through Wi-Fi can provide the data rates up to 54 MHz/s, it's not enough to the high speed delivery of high-definition video streams.

UWB technology can provide ease-of-use, low power and low cost wireless solution to the mentioned problems. With the ability of high data rates delivery, UWB will replace universal serial bus (USB) and provide high-speed wireless connectivity between PCs and PC peripherals, such as storage devices. For the multimedia connectivity of consumer electronics and entertainment equipment, UWB will replace IEEE 1394 cables to allow the interoperation among involved devices. As well, with the UWB technology, PCs can also communicate with entertainment clusters. Therefore, high definition audio and video stream can be delivered from personal PCs to the HDTV in the living room and then recorded by DVD recorder wirelessly. Through UWB enabled set-top boxes (STB) and game platforms, consumers can play

high quality internet games via STB fluently. Real-time conferencing can be made by the connection between 3G cell phone and STB.

Presently, there are two different systems for UWB standards. One is direct-sequence impulse UWB (DS-UWB) system, and the other is multi-band orthogonal frequency division multiplexing UWB (MB-OFDM UWB) system. For the DS-UWB system, a narrow impulse in time domain is used to provide very wide bandwidth in spectrum. Because of ultra-wide bandwidth, various broadband techniques should be used to meet the requirements of low noise amplifier (LNA), power amplifier (PA) and broadband impedance matching. To save chip area and power consumption, the MB-OFDM UWB system is a better option. MB-OFDM UWB topology divides the whole operating bandwidth into 14 sub-bands. This relaxes the challenge of broadband component design.

However, fast frequency hopping among the carriers of each sub-band raises design challenge with respect to short switching time. According to the multi-band OFDM alliance (MBOA) proposal [3], the transition time of frequency hopping over the operating sub-bands should be less than 9.5 ns, which prevents traditional phase-locked loop (PLL) based frequency synthesizer from a viable option. Because the operating frequency of Wi-Fi (2.4 GHz and 5 GHz) and Bluetooth (2.4 GHz) technology are around the spectrum of UWB technology, all spurious tones around 2.4 and 5 GHz must be suppressed to be less than some level to avoid the destruction of system SNR. As well, the phase noise of the LO carriers should be below -100 dBc/Hz at 1MHz offset to mainain a high system SNR [4].

In this thesis, the MB-OFDM UWB topology is adopted. As mentioned above, the critical design challenge of MB-OFDM UWB system is the frequency synthesizer. To meet the requirements of ultra-short switching time, small spurious tones and phase noise, a low cost and low power structure of modified PLL based frequency synthesizer is proposed.

1.2 Literature review

Since the United States Federal Communications Commission (FCC) announced UWB regulations at April, 2002, UWB technology has been a research focus world-wide. Due to the benefits of easy implementation and low power consumption, MB-OFDM topology is adopted by most companies for their UWB-enabled products. Various frequency synthesizer architectures for MB-OFDM UWB system were proposed in last few years.

Intuitively, it would seem that three PLLs can be used to generate three carriers for a Mode-1 OFDM UWB system. This approach was presented in [5]. After the start-up and settling down, the switching time among carriers can be less than 1ns. Because of CMOS implementation and inductor-free ring oscillators, the chip area can be reduced. Without the mixer implementation, spurious tones are not introduced by the ganging PLLs. This provides a viable architectural path for frequency synthesizer of MB-OFDM UWB system design. However, the large power consumption result from 3-PLL is an issue. The large chip area needed for 7 carriers makes this architecture not well suited to Mode-2 OFDM UWB system.

A frequency generator composed of two PLLs, a single sideband (SSB) mixer and a band-pass filter was proposed in [6], as shown in Figure 1.1. Using the SSB-mixer, three carriers for Mode-1 operation can be generated from a fixed 3960 MHz carrier with a deviation frequency of 528 MHz. Through the frequency selector, the frequency generator needs only 1ns for frequency hopping. Two integrated LC-oscillators used in the PLLs impose a large chip area penalty. Large power

consumption comes from the combination of two PLLs and four double-balanced mixers included in the SSB-mixer.

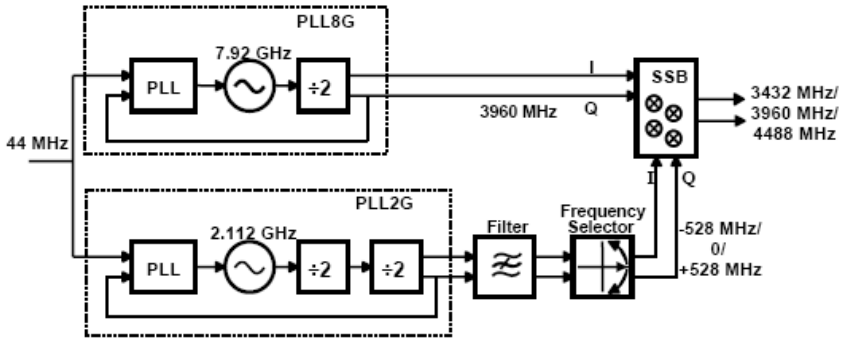

Figure 1.1 Frequency generator presented in [6]

In [7], a direct frequency synthesizer was used to create operating carriers. The presented architecture composed of a quadrature voltage control oscillator (VCO), two SSB-mixers, many divide-by-2 frequency dividers and two switching buffers, shown in Figure 1.2. Even though optimal noise and high frequency performance are achieved by using a SiGe BiCMOS process, two SSB-mixers and many frequency dividers make serious spurious tones an issue. SSB-mixers and frequency dividers also lead to large chip area and power consumption.

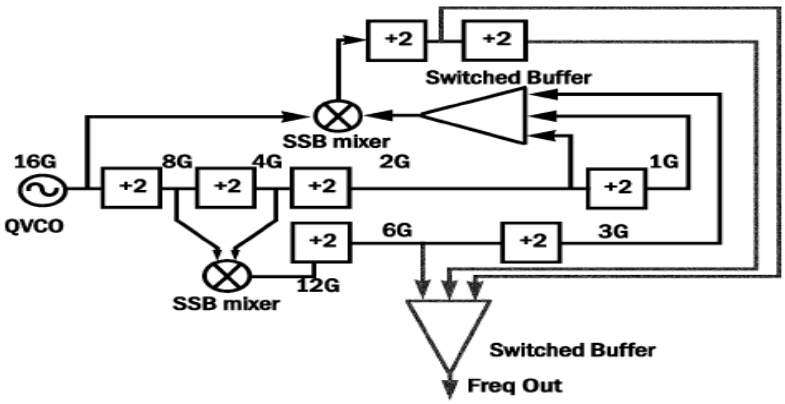

Figure 1.2 Direct frequency synthesizer presented in [7]

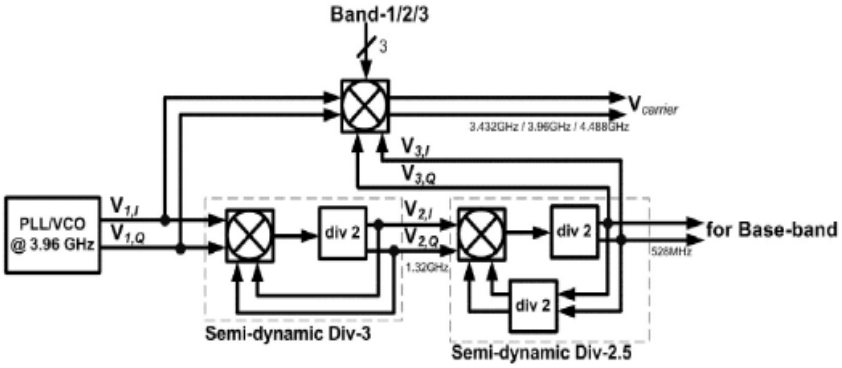

Figure 1.3 Direct frequency synthesizer with semi-dynamic dividers [8]

Similar to the concept of [6], a divide-by-7.5 frequency divider is used in [8] to replace one PLL in [6] to generate deviation frequency, 528 MHz. As shown in Figure 1.3, the divide-by-7.5 circuit is implemented by the combination of SSB-mixers and divde-by-2 frequency dividers. Intuitively it would appear that the chip area should reduce by including only one LC-oscillator in the frequency synthesizer. However, the inductors involved in the SSB-mixers occupy large chip area in the integrated circuit. The non-linearity of two SSB-mixers leads to the issue of spurious tones as shown in [7].

To sum up, with the exception of the architecture shown in [5], the mixers described here lead to poor spectral purity performance at the output of the frequency synthesizers. High-Q RF inductors for LC-oscillators of PLLs make full integration difficult and increase the fabrication cost as well. To achieve low cost, low power and low spur characteristics for the MB-OFDM UWB frequency synthesizers, the architecture composed of two PLLs and one multiplexer is proposed in this thesis, which will be described in detail at Chapter 3.

1.3 Thesis organization

In Chapter 2, the scheme and specifications of MB-OFDM UWB system are introduced. The requirements for frequency synthesizer implementation are derived from the specification of UWB system. Basic concepts of the RF transceiver's architectures and building blocks of the frequency synthesizer are presented in Chapter 3. To comply with the requirements for frequency synthesizer, the design methodology is provided to implement the building blocks of frequency synthesizer in Chapter 4. To verify the performance of proposed architecture, the simulation results of the phase-locked loop and multiplexer combination are given in Chapter 5. Finally, the conclusions are drawn in Chapter 6.

Reference

[1] “Ultra-Wideband (UWB) Technology: enabling high-speed wireless personal area networks”, Intel Corporation 2004 [Online]
Available: http://www.intel.com/network/connectivity/products/uwb/techdocs.htm

[2] James M Wilson, “Ultra-Wideband/ a Disruptive RF Technology?”, Intel Corporation 2002 [Online]
Available: http://www.intel.com/network/connectivity/products/uwb/techdocs.htm

[3] A. Batra *et al.*, “Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a,” doc. IEEE 802.15-03/268r3, Mar. 2004

[4] R. Roovers *et al.*, “An interference-robus receiver for ultra-wideband radio in SiGe BiCMOS technology,” *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2563-2572, Dec. 2005.

[5] B. Razavi *et al.*, “A UWB CMOS Transceiver,” *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2555-2562, Dec. 2005.

[6] D. Leenaerts *et al.*, “A SiGe BiCMOS 1 ns Fast Hopping Frequency Synthesizer for UWB Radio,” *IEEE Int. Solid-State Circuits Conf.*, pp. 202-203, Feb. 2005.

[7] A. Ismail *et al.*, “A 3.1 to 8.2 GHz Direct Conversion Receiver for MB-OFDM UWB Communications,” *IEEE Int. Solid-State Circuits Conf.*, pp. 208-209, Feb. 2005.

[8] C-C Lin *et al.*, “A Regenerative Semi-Dynamic Frequency Divider for Mode-1 MB-OFDM UWB Hopping Carrier Generation,” *IEEE Int. Solid-State Circuits Conf.*, pp. 206-207, Feb. 2005.

2

The MB-OFDM UWB Communication System

2.1 Introduction

In this chapter, the characteristics and principles of Orthogonal Frequency Division Multiplexing (OFDM) are described. According to the Multi-Band OFDM proposal for IEEE 802.15 standard, the specifications of the MB-OFDM UWB transceiver are introduced. Based on the system specifications, the design requirements for the frequency synthesizer, such as settling time, phase noise and spurious tones suppression, are derived. Following the derived requirements, the proposed frequency synthesizer is implemented in chapter 4.

2.2 Orthogonal Frequency Division Multiplexing (OFDM)

Generally, there are two different kinds of signal transmission schemes. One is single carrier transmission, and the other is multi-carrier transmission. Comparing to single carrier transmission, the multi-carrier transmission has the advantage of robustness to frequency-selective fading from multi-path and narrowband interference, as illustrated in Figure 2.2. Orthogonal frequency division multiplexing (OFDM) is kind of multi-carrier system. Different from traditional multi-carrier system, OFDM uses a large number of closely spaced orthogonal sub-carriers to increase the spectral efficiency and reduce Inter Symbol Interference (ISI).

The waveform of the *sinc* function in frequency domain is shown in Figure 2.2. From the Figure 2.1, we can see the nulls in the spectrum occur at the Δf offset from the peak frequency. By setting Δf as the frequency spacing between sub-carriers, the orthogonality can be achieved by OFDM transmission scheme. To generate the OFDM signals mentioned above, the baseband signals should be multiplied by a rectangular waveform, with symbol period equal to T_s. Through Fourier transform, the *sinc* function with Δf equal to $1/T_s$ is obtained in frequency domain.

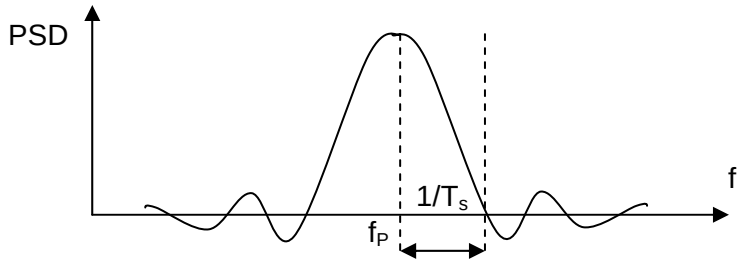

Figure 2.1 *sinc* function in frequency domain

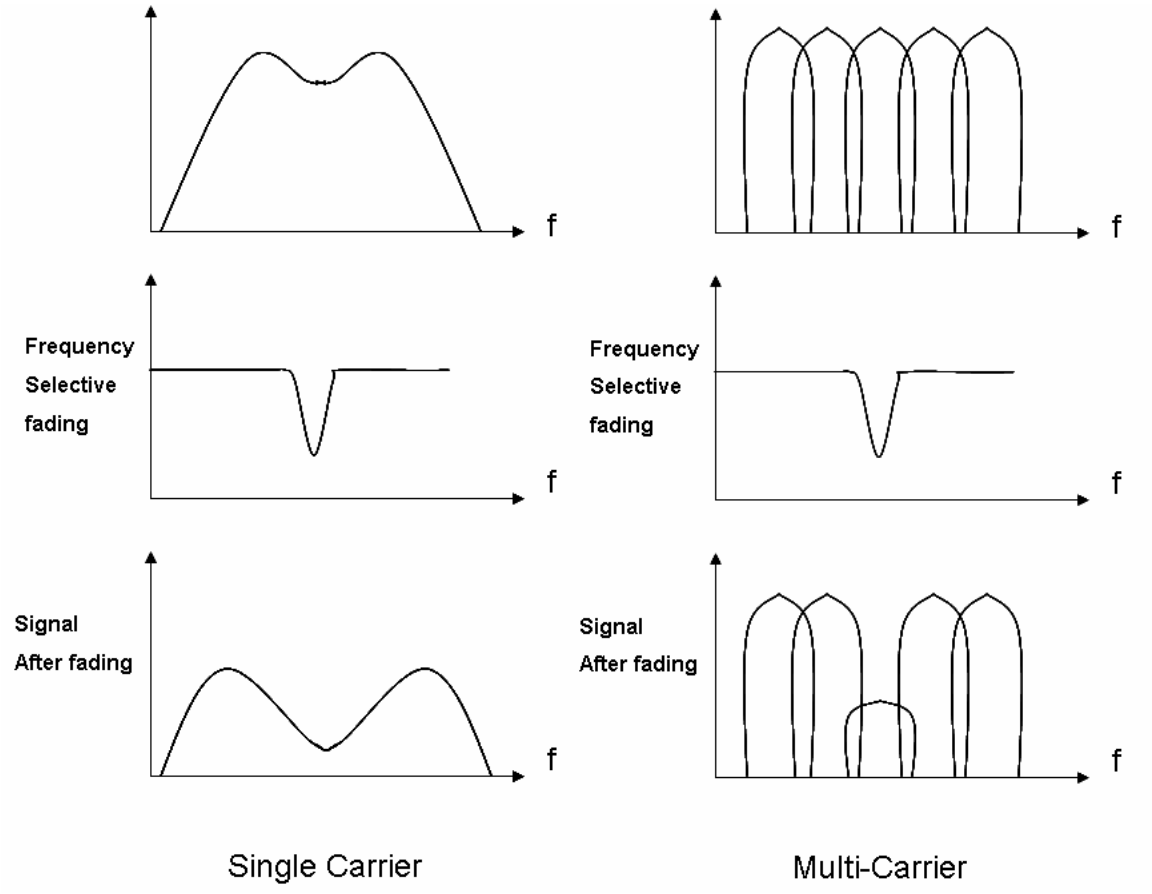

Figure 2.2 single carrier transmissions vs. multi-carrier transmissions

Therefore, the sub-carriers of the OFDM signals will be orthogonal to each other. The time domain OFDM signals in mathematical formula can be described as [1]

$$S(t) = rect\left(\frac{t}{T_s}\right)\sum_{n=0}^{N-1}\mathrm{Re}\left\{\exp(j2\pi(f_P + \frac{n}{T_s})t)\right\}$$

This implies that the OFDM signals can be generated simply through Inverse Fast Fourier Transformation (IFFT), and demodulated by another Fast Fourier Transform (FFT).

2.3 MB-OFDM UWB System Specifications

Due to the advantages of bandwidth utilization efficiency and robustness to frequency selective fading, the OFDM is adopted for Ultra Wideband communication systems. According to the MB-OFDM proposal [1], the UWB systems can operate in the frequency range, from 3.1 GHz to 10.6 GHz, as regulated by the Federal Communication Commission (FCC). The 7.5 GHz spectrum is divided into 14 bands, while each band has 528 MHz bandwidth, shown in Figure 2.3. The center frequency of each band can be calculated by

$$f_C = 2904 + 528 \times N_b$$

where N_b is equal to 1 to 14. A 528 MHz wide OFDM signal band is composed of 128 sub-carriers with 4.125 MHz carrier spacing. Because of wide operating bandwidth, up to 480 Mb/s date rate can be reached by modulating each sub-carrier with Quadrature Phase Shift Keying (QPSK).

Through fast frequency hopping, the multi-band OFDM signals can be delivered efficiently. The switching time after the 312.5 ns symbol period is determined to be less than 9.5 ns. Time-Frequency Codes (TFCs) are used to define the sequence of the operating frequency hopping for different applications. There are up to four different TFCs are defined for each band group in the MB-OFDM proposal. In table 2-1, the TFCs for a group-1 MB-OFDM system are listed.

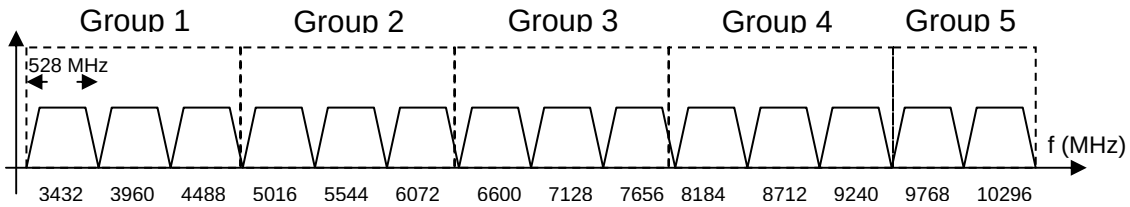

Figure 2.3 MB-OFDM UWB spectrums

Table 2-1 Time Frequency Codes for Group-1 MB-OFDM system

TFCs	Band hopping sequence					
1	1	2	3	1	2	3
2	1	3	2	1	3	2
3	1	1	2	2	3	3
4	1	1	3	3	2	2

To evaluate the noise performance of MB-OFDM UWB systems, sensitivity and Bit Error Rates (BER) are two important specifications. The system's allowable Signal to Noise Ratio (SNR) can be derived from the target BER. By sensitivity and SNR, we can finally determine the allowed noise and interference levels appearing in the system. In [2] [3], the sensitivity and SNR for the target coded BER of 10 are derived to be -73.2 dBm and 7.7 dB for a 480 Mb/s data transmission, respectively. Based on given sensitivity and SNR, the requirements of phase noise and spurious tones for frequency synthesizer are obtained in the following section.

2.4 Design Requirements of MB-OFDM UWB Frequency Synthesizer

Settling time, phase noise and spurious tones are usually used to characterize the MB-OFDM UWB frequency synthesizer. From the system specifications defined in the last section, the derivations of three important characteristics are described in the following sections.

2.4.1 Settling Time

To utilize regulated bandwidth efficiently, fast hopping between operating bands is necessary. To illustrate the behavior of MB-OFDM carrier hopping, the operation of Mode-1 with TFC #1 is shown in Figure 2.4. Band 1, 2 and 3 are involved in Mode-1 operation. The system hops after sampling the OFDM signals in 312.5 ns. The switching time of the band hopping is determined to be 9.5 ns.

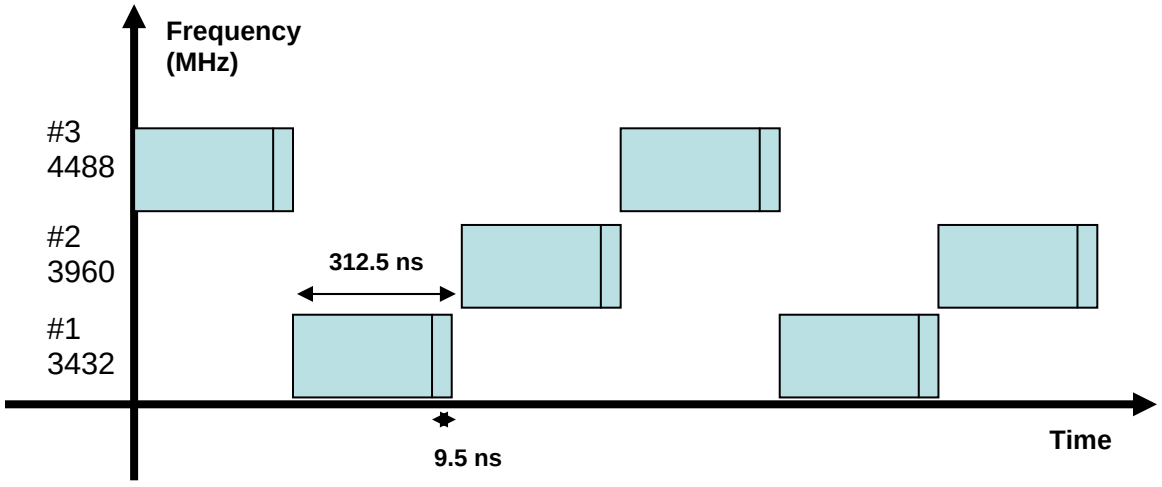

Figure 2.4 Frequency switching of Mode-1 OFDM UWB system

With the characteristics of high integration, low cost and simple structure, the Zero-IF architecture is largely adopted for MB-OFDM UWB systems. The LO frequencies of up and down converting mixers should be equal to the input carrier frequencies in the Zero-IF architecture, which will be described detailed in Chapter 3. This implies that the switching time of the frequency synthesizers has to be less than 9.5 ns to satisfy the requirement of standards.

2.4.2 Phase Noise

Through reciprocal mixing the phase noise of LO signals with in-band and out-of-band blockers, the converted signals will lead to lower system's SNR, and then destroy the BER. For MB-OFDM UWB system, the phase noise requirements of LO is primarily dominated by the strong out-of-band blockers, such as carriers of WiFi, Bluetooth, 802.11a and the adjacent UWB signals. The power and located frequencies of interference sources presented within 3.1-10.6 GHz are illustrated in Figure 2.5, respectively [1].

For a given SNR, the requirement of the LO phase noise corresponding to a certain interference source can be approximated by

$$\begin{aligned} & S_{desired} - S_{block} \geq SNR \\ & S_{desired} - (S_{\text{int}} + L(f_m) + 10\log(f_{bw})) \geq SNR \\ & L(f_m) \leq S_{desired} - S_{\text{int}} - 10\log(f_{bw}) - SNR \end{aligned} \qquad (2.1)$$

As defined in [1], $S_{desired}$, the power level of a desired signal, should be 6 dB above receiver's sensitivity. S_{int} is the power level of interference source, and f_{bw} is the channel bandwidth of UWB systems.

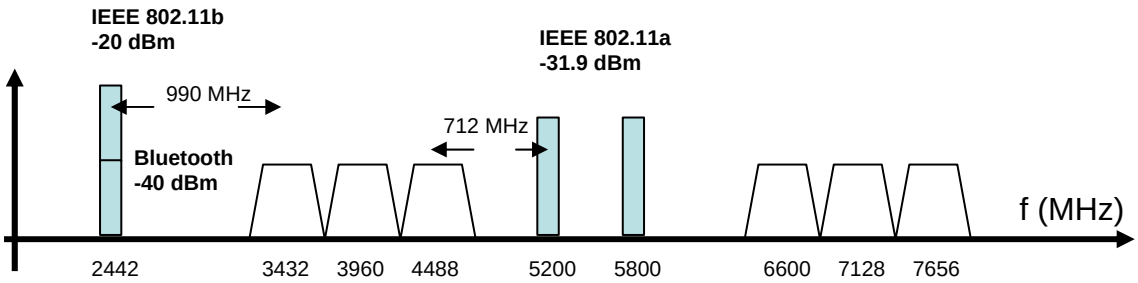

Figure 2.5 Interference spectrum of MB-OFDM UWB system

Assume the phase noise of LO follows the $1/f_m^2$ characteristics, we can normalize the f_m offset phase noise to 1 MHz offset phase noise [4], which can be expressed as

$$L(1\,MHz) = L(f_m) + 20\log(\frac{f_m}{1\,MHz}) \qquad (2.2)$$

From the system specifications determined in section 2, $S_{desired}$ and SNR are equal to -67.2 dBm and 7.7 dB for 480 Mb/s transmissions, respectively. Thus, the phase noise requirement led by Bluetooth interference can be estimated to be

$$L(1\,MHz) \le -67.2 - (-40) - 10\log(528\times10^6) - 7.7 + 20\log(990) = -62.22\,(dBc)$$

The phase noise requirements of the Mode-1 OFDM UWB frequency synthesizer for different transmission standards are listed in table 2-2.

Table 2-2 Phase noise requirements owing to different interference sources

Blockers	Frequency (MHz)	Phase Noise (dBc)
Bluetooth	2442	-62.22
WiFi	2442	-82.22
802.11a	5200	-73.17
adj. UWB	+/- 528	-66.4

2.4.3 Spurious Tones Suppression

Due to non-linearity inside the frequency synthesizer, a number of spurious tones are generated. Just as with phase noise, after reciprocal mixing, out-of-band blockers will shifted into the band of interest by spurious tones. Thus, to co-exist with other standards and tolerate adjacent UWB signal transmissions, the amplitude of spurious tones is also a very important characteristic of the LO generator. Similar to phase noise, the spurious suppression can be approximated by

$$\begin{aligned} & S_{desired} - S_{block} \geq SNR \\ & S_{desired} - (S_{\text{int}} + S_{spur}) \geq SNR \\ & S_{spur} \leq S_{desired} - S_{\text{int}} - SNR \end{aligned} \qquad (2.3)$$

By substituting the system specifications and power levels of blockers, the spurious suppression requirements for different blockers are listed in table 2-3.

Table 2-3 Spurious tones suppression requirements owing to interference sources

Blockers	Frequency (MHz)	Spurious Suppression (dBc)
Bluetooth	2442	-34.9
WiFi	2442	-49.9
802.11a	5200	-40
Adj. UWB	+/- 528	-33.65

Finally, based on the system specifications determined in the proposal of IEEE 802.15 standard, the design requirements of the frequency synthesizer for Mode-1 operation are summarized in table 2-4.

Table 2-4 Summaries of synthesizer requirements

Parameters	**Specification**
Frequency	3432, 3960, 4488 MHz
Settling time	< 9.5 ns
Phase Noise	< 82.22 dBc/Hz @ 1 MHz offset
Spurious Suppression	> 49.9 dBc @ 2.4 GHz > 40 dBc @ 5.2 GHz

Reference

[1] A. Batra *et al.*, Multiband OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a, http://www.multibandofdm.org/papers/, Sept. 2004.

[2] A. Batra *et al.*, "Design of a Multiband OFDM system for Realistic UWB Channel Environments," *IEEE Trans. Microw. Tech. Theory*, vol. 52, no. 9, pp. 2123-2138, Sept. 2004.

[3] C. Mishra *et al.*, "Frequency Planning and Synthesizer Architectures for Multiband OFDM UWB Radios," *IEEE Trans. Microw. Tech. Theory*, vol. 53, no. 12, pp. 3744-3756, Dec. 2005.

[4] P. Zhang *et al.*, "A New RF Front-End and Frequency Synthesizer Architecture for 3.1-10.6 GHz MB-OFDM UWB Receivers," *IEEE Circuits and Systems*, vol. 2, pp. 1119-1122, Aug. 2005.

3

The RF Frequency Synthesizer

3.1 Introduction

In RF transceiver architectures, frequency synthesizers are usually employed to covert the baseband modulated signals to the required operating frequencies. For different architectures, the requirements for frequency synthesizer are different. The performance of frequency synthesizers, such as phase noise and I/Q signals, has a large impact on the whole transceiver. To give us an insight into the behavior of frequency synthesizer, the basic theory and noise analysis are described. Then, we can obtain the optimal parameters for the building components of frequency synthesizer. In this chapter, we start with the introduction of two useful transceiver architectures, and then the system impact of the frequency synthesizer's performance is described.

3.2 RF Transceiver Architectures

Basically, transceiver architectures are separated to two different kinds: Low-IF and Zero-IF architecture [1]. A popular double conversion Low-IF topology, used in GSM and DECT systems, is shown in Figure 3.1 [1]. To increase the selectivity and sensitivity, this topology includes two stages of down-conversion Mixers. First Mixer converts RF signal to large IF, and then the image signal can be filtered by a band-pass filter with limited Q.

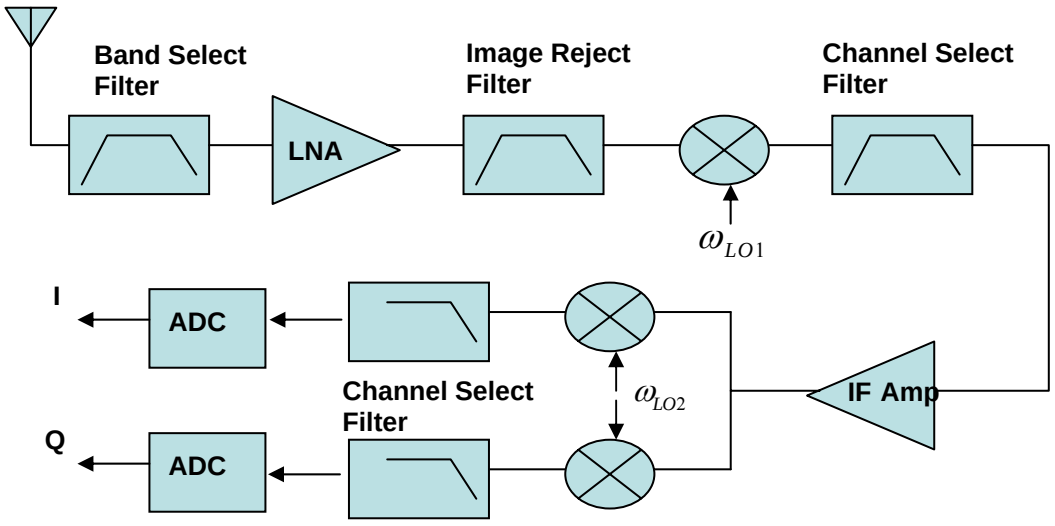

Figure 3.1 Double conversion Low-IF architecture

A lower IF, close to zero frequency, is generated by the second Mixer; good selectivity can be achieved by the high Q low-pass filter. Because we are operating in a low IF, the conversion Low-IF topology is not sensitive to the DC offsets and flicker noise, which are serious problems in Zero-IF topology. In addition, the good selectivity and sensitivity make dual conversion Low-IF topology popular in many

applications. However, the circuit complexity, off-chip band-pass filter, large power consumption and narrow-band image attenuation are obstacles to wideband applications.

To overcome the problem of the image signals locating in the signal bandwidth, the Zero-IF topology is widely used for UWB communication. As shown in Figure 3.2, by the LO frequency the same as RF signal frequency, the Mixers in I/Q paths convert input signals to zero frequency. The issue of image rejection bothering in Low-IF topology is solved. The low-pass filter with high quality factor is used to enhance the selectivity of receiver. Without the high-Q band-pass filter for the channel selection, the power consumption and cost can be reduced, which is important for the low power requirement to the UWB standards. However, as mentioned above, the issues of short settling time, DC offsets, mainly arisen from LO leakage, I/Q mismatch and flicker noises ($1/f$ noise) make Zero-IF topology design a big challenge [1][2].

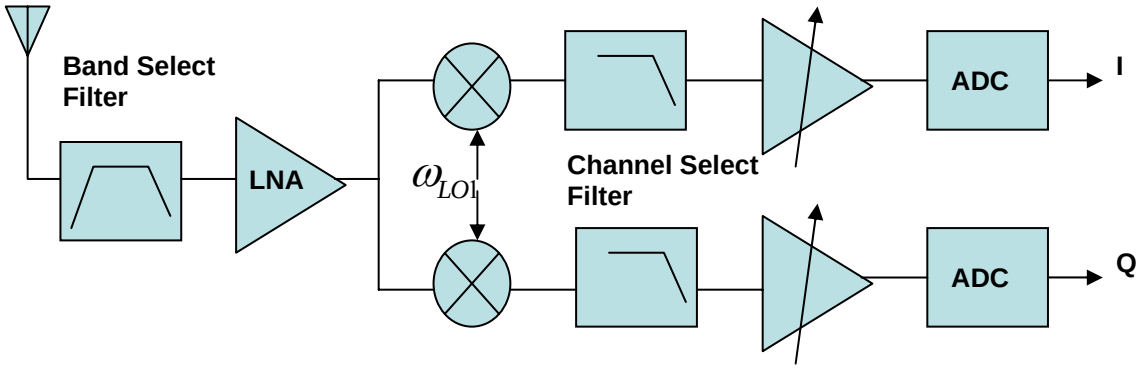

Figure 3.2 Zero-IF receiver architecture

After the introduction of transceiver architectures, the impact of frequency synthesizer on the transceiver is discussed in the following paragraph. Phase noise and I/Q signals mismatch are two significant factors that degrade the signal-to-noise ratio (SNR) of the transceiver. Phase noise is arisen from the random phase fluctuation in the oscillator. With the phase noise the output of the oscillator in time domain can be expressed as [3]

$$S_o(t) = A\cos(\omega_c t + \Delta\phi(t)) \quad (3.1)$$

By substituting the spectral density of phase noise into (3.1), the phase modulation can be transformed to amplitude modulation, shown in Figure 3.3, with the assumption that the phase fluctuation is small enough. How will this phenomena influence transceiver's performance? As mentioned above, the frequency synthesizer is employed to apply LO signals for up or down conversion in the transceiver. Due to phase noise, the interfering signals around the desired signal will be transferred to the same IF as the desired signal, degrading the output SNR.

If the LO signals applied to I/Q paths are imbalance, the signal constellation of the I and Q data streams will be corrupted. This will lead to an increasing bit error rate, destroying the SNR.

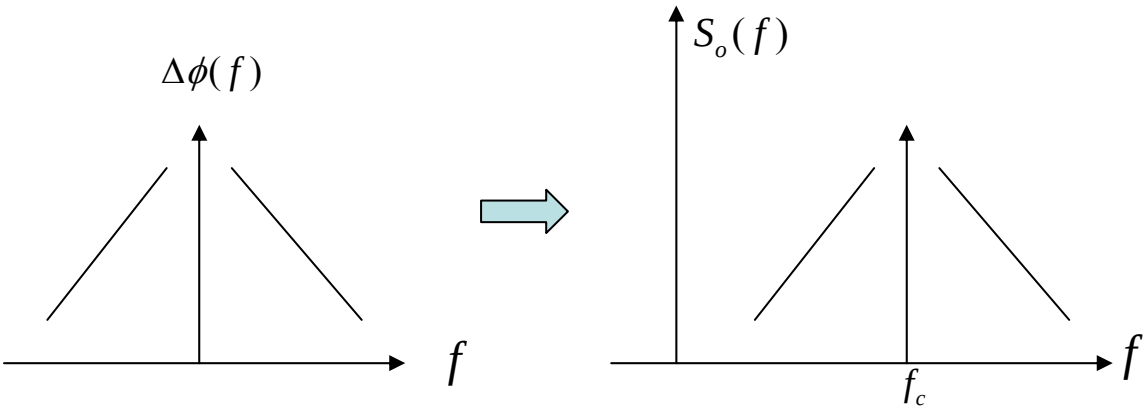

Figure 3.3 Amplitude modulation transformed by phase modulation

3.3 Frequency Synthesizer Architectures

3.3.1 General Description

A frequency Synthesizer is used to provide periodic and accurate signal to wireless transceivers. For some wireless applications, a frequency synthesizer would have to generate different precise signals to make transceivers work on different channels. A comparison between the GSM and UWB systems shows that the channel bandwidth of the former is only 200 kHz, however, that of later can reach to 1.5 GHz. That means the frequency hopping of frequency synthesizer may have control small frequency variations or settle very fast when carriers change significanly. To meet these stringent requirements, such as noise performance, power consumption and settling time, for many different wireless communication standards, the design of the frequency synthesizer becomes challenging.

The phase-Locked Loop is the most common choice to implement the frequency synthesizer in a wireless transceiver. Basically, the Phase-Locked Loop is a negative feedback system that can force the output frequency to be exactly the same as the input frequency. The accuracy of the frequency synthesizer's output frequency is very important to the whole transceiver's performance. Due to the non-linearity existing in all systems, an error will always happen in the input of Phase-Locked Loop if we use the output frequency to track input reference frequency. Therefore, Phase-Locked Loop always works on phase to avoid the frequency variation. The locked condition for the Phase-Locked Loop happens when the phase difference between the input and output signals is constant with time. This means the input and output frequencies are equal.

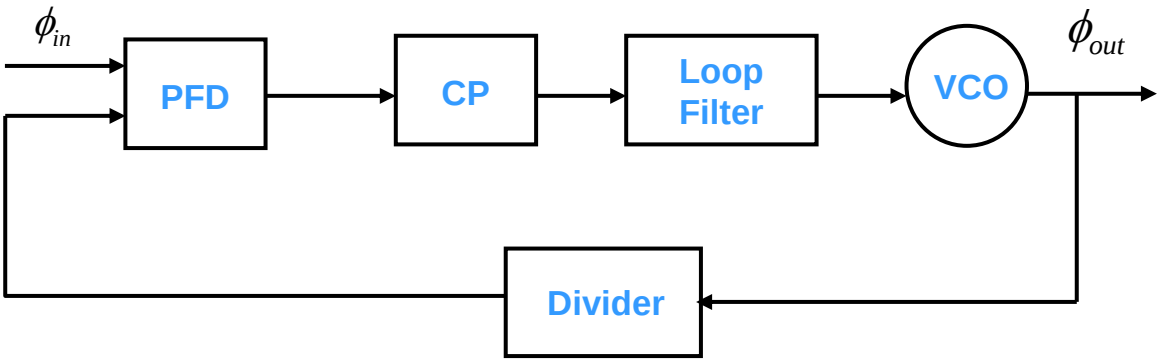

Figure 3.4 Block diagram of Charge Pump PLL

The block diagram of a simple Charge-pump PLL is shown in figure 3.4. The loop consisted of an input reference source, a phase/ frequency detector, a charge pump, a voltage control oscillator and a frequency divider. The PLL based frequency synthesizers can be divided into two different kinds, Integer-N and Fractional-N frequency synthesizer. The Integer-N architecture makes the output signal frequency exactly the same as N times of input reference, which means the channel spacing should be a multiple of input reference frequency. In contrast to Inter-N synthesizer, the Fractional-N architecture has the division ratio with a fractional value. This means it can have a smaller frequency step than the input reference frequency.

Due to its physical properties, the crystal oscillator, oscillating at a particular frequency with an extreme accuracy, is usually employed to be the input reference signal in the PLL. By sensing the phase difference between the input and the divided output signals, the Phase/ Frequency Detector and Charge pump will generate either “UP” or “Down” charging pulses. Then, these charging pulses will be integrated by the loop filter and become the tuning voltage of the voltage control oscillator. Finally,

the tuning voltage changes the output frequency of voltage control oscillator to catch the input reference frequency.

To describe the operation of PLL more clearly, the dynamic response of the PLL is illustrated in Figure 3.5. After the time t1, the frequency of input signal increases. A "UP" charging pulse is output by Phase/ Frequency Detector to response to the phase difference appearing in the input ports. The charging current injected by charge pump circuit is integrated by the loop filter, and then converted to be an increasing tuning voltage. Thereby, an increasing oscillating frequency is generated at the output of voltage control oscillator. After the output frequency become larger, the decreasing width of charging pulse leads to the reduction of the slope of tuning voltage. Finally, the tuning voltage become constant and the divided output frequency will lock at input reference frequency.

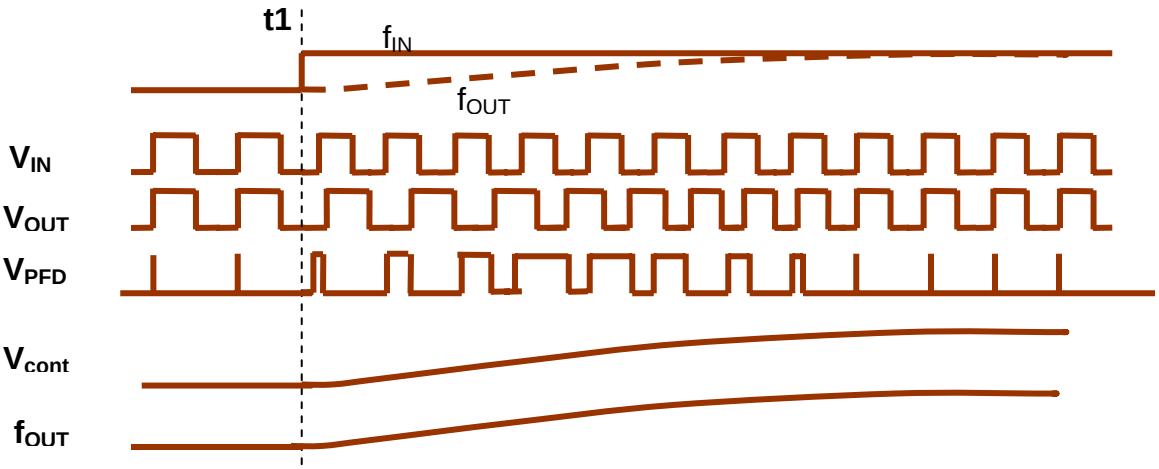

Figure 3.5 Dynamic response of PLL

3.3.2 Proposed Architecture

For the MB-OFDM UWB system's frequency synthesizer, the most difficult design issue is the fast frequency hopping. According to the MB-OFDM proposal described in Chapter 2, the switching time of the frequency hopping should be less than 9.5 ns, which prevents the traditional PLL based frequency synthesizer from a viable structure. However, by utilizing the sampling time of OFDM signals, the architecture proposed in [4], shown in Figure 3.6, can extend the settling time of PLL to 312.5 ns.

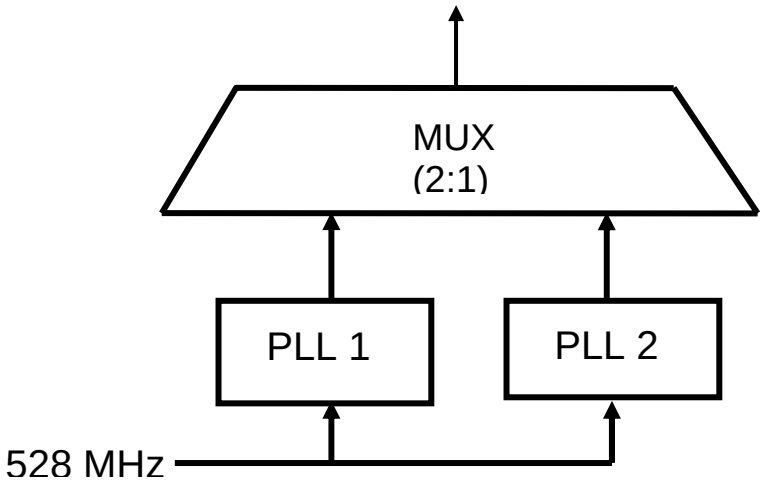

Figure 3.6 Frequency synthesizer for MB-OFDM UWB system

Based on the architecture in [4], we use ring oscillators to implement the VCO of PLL involved in the frequency synthesizer. Due to inherent characteristic of the ring oscillator, low distortion quadrature signals can be generated. As well, much smaller die area is achieved by the ring oscillator than that of LC-oscillator. This makes full integration of the frequency synthesizer relatively easy. Compared to the frequency

synthesizer presented in [4], the proposed structure can provide lower cost and exhibit better spectral performance for the frequency synthesizer implementation.

The operation of the proposed frequency synthesizer is described in the following: First, we let PLL1 lock at current processing frequency and PLL2 handle the next frequency band which is determined by the Time Frequency Codes (TFC). Since the switching time of the multiplexer is always less than 1ns, by hopping the frequencies between two PLLs, the frequency synthesizer can meet the settling time requirement if each PLL could settle down in 300 ns.

Because the proposed frequency synthesizer is based on two PLLs, to obtain the insight into the design issues of frequency synthesizer, the basic theory of each building block of PLL is described in the following sections.

3.4 PLL Building Blocks

3.4.1 The Phase/Frequency Detector and the Charge Pump

The Phase/Frequency Detector is the first block in the Phase-Locked Loop. It is used to sense both phase and frequency difference of the input signals, and then output the error signals. Comparing with phase detectors, such as multiplier and XOR phase detector, the Phase/Frequency Detector has the following advantages:

1. Large pull-in frequency range: Usually, the pull-in frequency range of multiplier and XOR phase detector is relate to the loop parameters
2. Great noise performance: Both multiplier and XOR phase detector work on sensing the phase difference during the whole reference period. This implies the phase detectors will contribute the noise to the system during the whole reference period. Conversely, due to the edge-trigger property, the Phase/Frequency Detector only sense the input signal difference in a small fraction of reference period, and only transfer small parts of noise to the system's output.
3. Insensitive to the signal duty cycles: Since the whole signal period is used for phase detection process, the multiplier and XOR phase detector are very sensitive to the input signal's duty cycle. The "false locked" condition will happen to the PLL possibly. This is because the phase detector could generate the same error pulses for the desired signal and its harmonic signals. Then, the PLL would possibly lock to the harmonics of desired signals. Conversely, due to the edge-trigger property, the Phase/Frequency Detector is irrespective of

the input signal's duty circle. This will make the design of Frequency Divider in the feedback loop become much easier.

For the sake of illustration, the block diagram of the Phase/Frequency Detector and two examples are shown in Figure 3.7. First, we make the divided output signal become phase lag to the input reference signal. The detected lagging information will lead to a voltage pulse generated at the output "UP". Through the operation of other components in the loop, an increasing tuning voltage will build up an output frequency, and then correct the phase error shown on the Phase/Frequency Detector's input. Conversely, the output divided signal with larger frequency than input reference frequency makes the Phase/Frequency Detector to output a signal pulse at "Down", which forces the loop to decrease output frequency eventually.

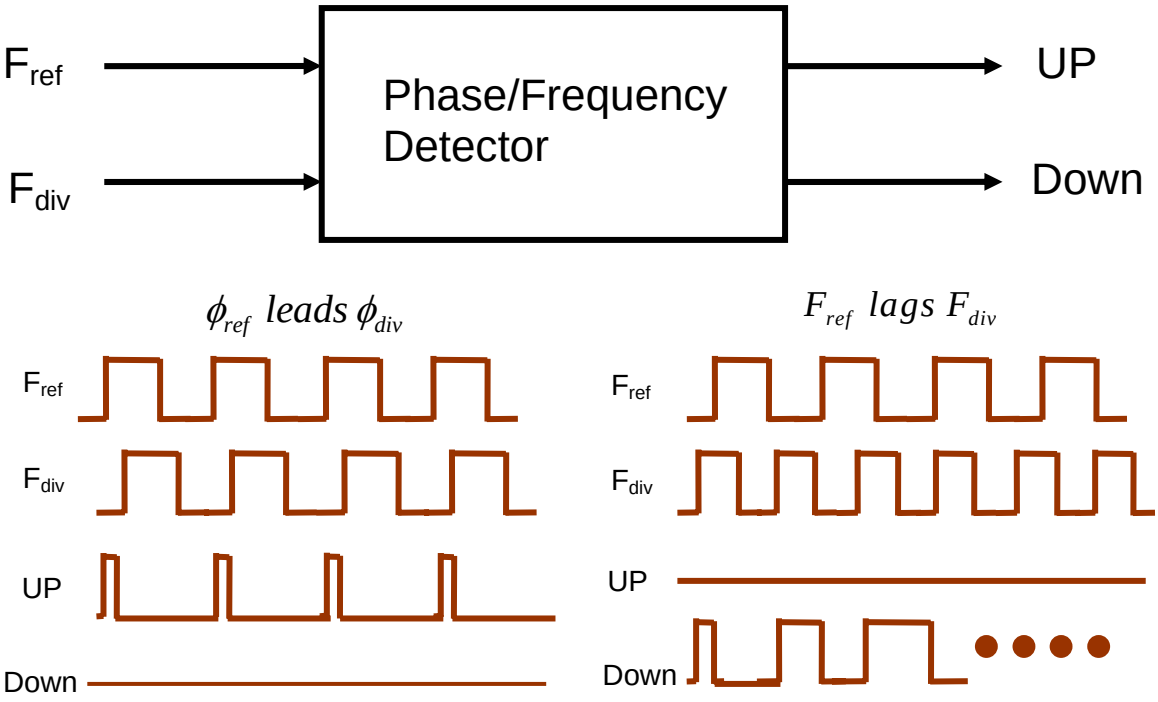

Figure 3.7 Two examples of Phase /Frequency Detector operation

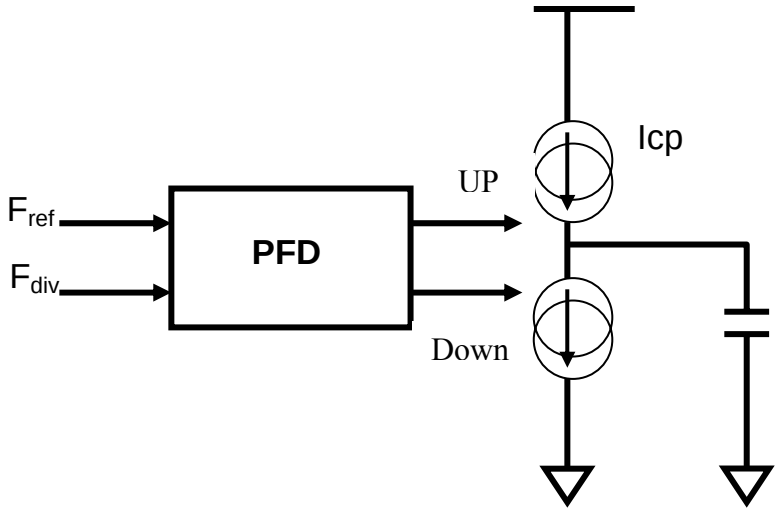

Figure 3.8 Block diagram of PFD/ CP combination

A Charge Pump is usually put just behind the Phase/Frequency Detector and it must sense the difference between "UP" and "Down" voltage pulses. It will either inject or withdraw the current from the following loop filter depending on which sign of pulse is present. The basic concept of the charge pump can be illustrated by the Figure 3.8. Once the "UP" pulse is produced by the Phase/Frequency Detector, the charging loop in the charge pump is closed to inject current into loop filter. Similarly, the "Down" pulses will close the discharging loop in the Charge Pump and take the charge out of loop filter. When the "UP" and "Down" signals are active or inactive at the same time, no current will flow into or out of Charge Pump's output port.

Ideally, if both the charging and discharging switches of Charge Pump are opened, the output resistance of Charge Pump is equal to infinite. This makes the following loop filter become an integrator, which leads to an infinite DC gain of PFD/CP/LPF combination. With infinite DC gain, the zero phase error would appear in the input of PFD to sustain a steady VCO tuning voltage in the phase locked condition.

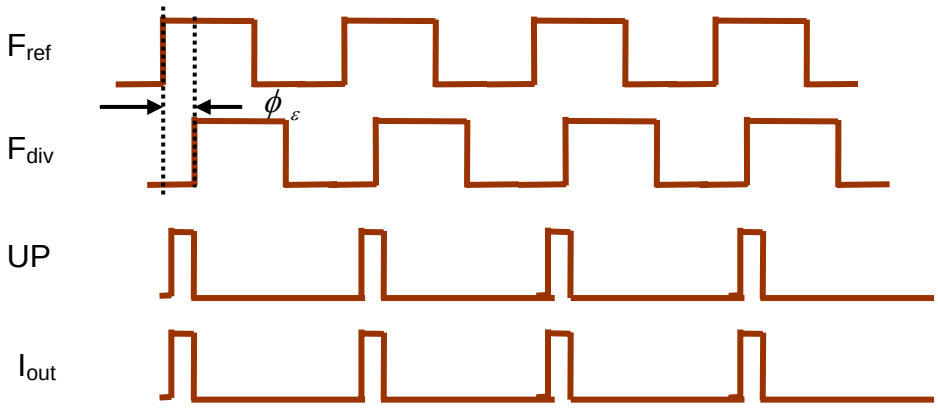

Figure 3.9 Transition behavior of PFD/CP

To get the linear model of PFD/CP combination, we can observe the transition behavior of PFD/CP, shown in Figure 3.9. It is obvious that the pulse width of PFD's output signal, "UP", is proportional to the phase difference, ϕ_ε, between its two input signals. This voltage pulse is used to close the switch in the Charge Pump, and then source the current to the loop filter. Therefore, the average current sourced from the Charge Pump (as related to the input phase difference) can be calculated by

$$\overline{I_{out}} = \frac{I_{CP} \times \phi_\varepsilon}{2\pi}$$

I_{CP} is the current sourced by charge pump. The gain of PFD/CP, defined as K_{PD}, presents the relationship between the input phase differences with the output average current, which can be expressed as

$$K_{PD} = \frac{\overline{I_{out}}}{\phi_\varepsilon} = \frac{I_{CP}}{2\pi} \qquad (3.1)$$

From the equation (3.1), we can see that the output current increases with the increasing phase difference between the inputs of PFD with a slope equal to K_{PD},.

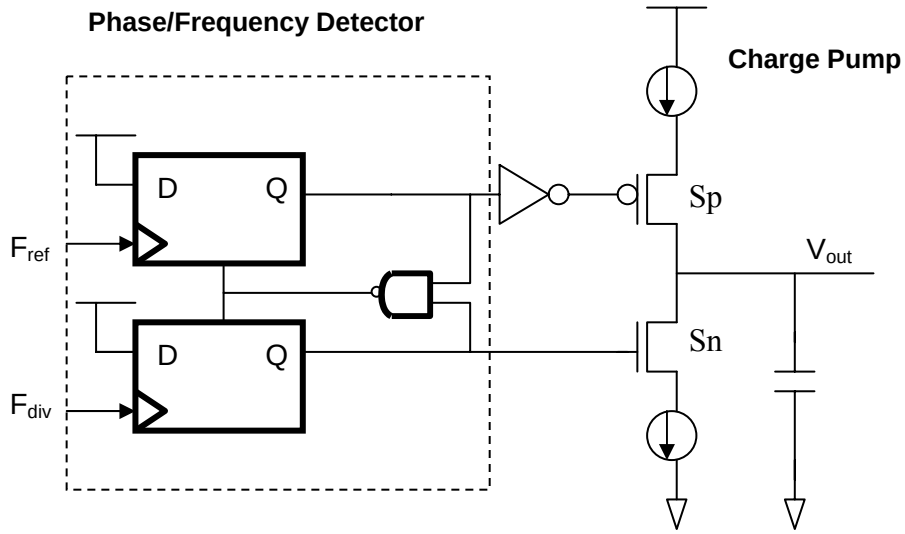

Figure 3.10 PFD/CP circuit

There are many non-linear characteristics existing in the PFD/CP circuit. Most of those are induced by the charge pump circuit and these will make a great impact on the whole PLL. The non-linear characteristics we would like to discuss in the following section including the issues of dead zone, charge sharing and reference feed-through.

The PFD/CP circuit is shown in Figure 3.10. The PFD output is applied to switch the charge pump's current source. If the phase error is too small, the induced output voltage pulse may be not wide enough to turn on the charge pump. This makes the loop become insensitive to the small phase error. The small area existing around the zero phase difference is called a "Dead zone", shown in Figure 3.11. To get rid of the "Dead zone", a delay cell is always inserted between the NAND gate and D-Flip-Flop to increase the duty circle of the output voltage pulse. However, the delay time contributed by the extra delay cell will decrease the maximum operating frequency of

the PFD. Therefore, the trade-off between "Dead zone" and operating frequency range should be taken carefully.

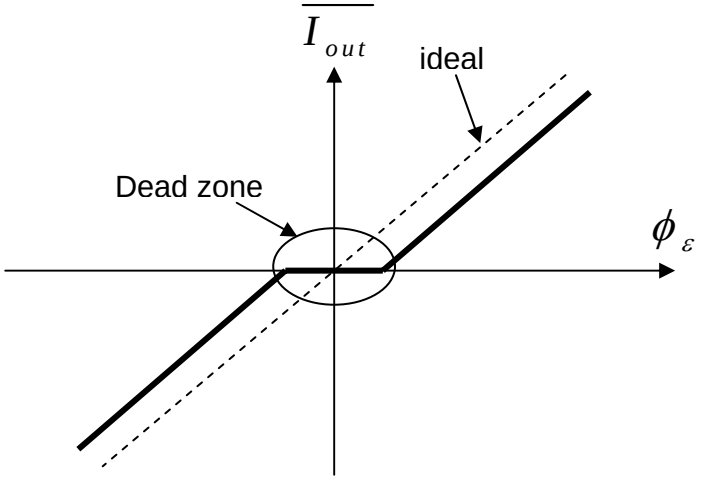

Figure 3.11 Dead zone of PFD/CP combination

Charge sharing is also a very important issue in the PFD/CP design. Due to the parasitic capacitance of the current source in the charge pump, there will be a voltage gap existing between the source ports of switches Sn and Sp, shown in Figure 3.10. When both Sn and Sp are closed, the voltage gap will place extra charges into the loop filter. This results in a variation in the VCO's tuning voltage and a subsequent fluctuation in the output frequency.

The third issue is the reference feed-through. Basically, one of main effects leading to the reference feed-through is the mismatch in the up and down current sources of charge pump. During the reset transition of Phase/Frequency Detector, the narrow voltage pulses will appear in both "UP" and "Down". Ideally, the duty circle of pulses in "UP" and "Down" should be exactly the same, and then the source and

sink current in the Charge Pump can cancel completely. However, in practice, the current-mismatch happens all the time. A net charge induced by current-mismatch will inject into the loop filter and yield a shift on tuning voltage of VCO. Consequently, a frequency correction will be made by the loop. This process will keep going with the frequency the same as input reference frequency. Therefore, an AC signal appears on the voltage control line of VCO. This will make the output signal of the VCO become [5]:

$$v_{out} \approx A\cos(\omega_0 t) + \frac{AV_{ref}K_{VCO}}{2\omega_{ref}}[\cos(\omega_0 + \omega_{ref})t - \cos(\omega_0 - \omega_{ref})t] \qquad (3.2)$$

where K_{VCO} is the gain of VCO. From the equation (3.2), we can see there are two spurs generated, causing a ω_{ref} shift from the desired frequency. Hence, to improve the spur performance of PLL, the current mismatch of charge pump should be reduced as much as possible.

3.4.2 The Voltage Control Oscillator (VCO)

Oscillators are electrical circuits that generate a periodic signal at a particular frequency. Basically, the oscillators can be separated into two different kinds: waveform-based oscillators and resonator-based oscillators. Both these oscillators are made using a feedback systems, as shown in Figure 3.12. Both oscillator need to satisfy the Barkhausen Criteria:

$$|H(j\omega_0)\beta(j\omega_0)| = 1$$
$$\angle H(j\omega_0)\beta(j\omega_0) = 180^0$$

To make the oscillators operate at different frequencies, a tuning mechanism controlled by voltage or current is always used to make the feedback system satisfy these criteria at different frequencies. Ring oscillators, waveform-based oscillators, and LC-tank oscillators, resonator-based oscillators are common oscillators usually adopted to implement Voltage Control Oscillator (VCO). LC-tank oscillators have the advantage of good phase noise, which makes it a good choice for frequency synthesizer. However, the huge area occupied by high "Q" inductor makes it difficult to fully integrate in the monolithic chip. The small tuning range also sets the limits to wide bandwidth application.

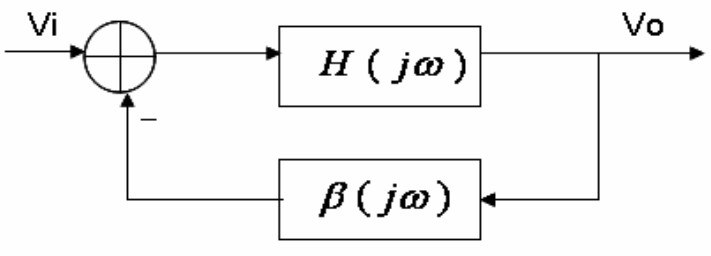

Figure 3.12 Feedback system

Conversely, without the inductor involved in the circuit, the ring oscillator is very suitable to the monolithic integration. The large frequency tuning range of ring oscillators can easily meet the requirement of wide bandwidth communication standards. The only disadvantage of ring oscillator is its worse phase noise performance than the LC-tank oscillators. To obtain the same phase noise as LC-tank oscillators, large power consumption is necessary to ring oscillators. Therefore, depending on the wireless applications, the designer can adopt ring oscillator or LC-tank oscillator to implement VCO of PLL.

The simple structure of ring oscillator is shown in the Figure 3.13. There are two analyses can be used to approximate the ring oscillator's oscillating frequency. First, we use large signal to do the analysis. For a negative feedback system, the delay cells in the ring oscillator should apply the extra 180^0 phase shift to satisfy Barkhausen Criteria. Assuming the ring oscillator includes N stages, the phase shift applied by each stage should be 180^0/N. Therefore, the delay time, τ , of each stage is equal to

$$\tau = \frac{180^0}{N} \times \frac{T}{360^0}$$

Then, the frequency of oscillation can be obtained by

$$f_{osc} = \frac{1}{2N\tau}$$

The delay time, τ , can be estimated by calculating the time taken by the bias current to charge the load capacitor to half of output voltage swing. Hence the oscillation frequency can be expressed as

$$f_{osc} = \frac{1}{2N} \times \left(\frac{I}{C} \times \frac{2}{V_{swing}} \right) = \frac{I}{NCV_{swing}}$$

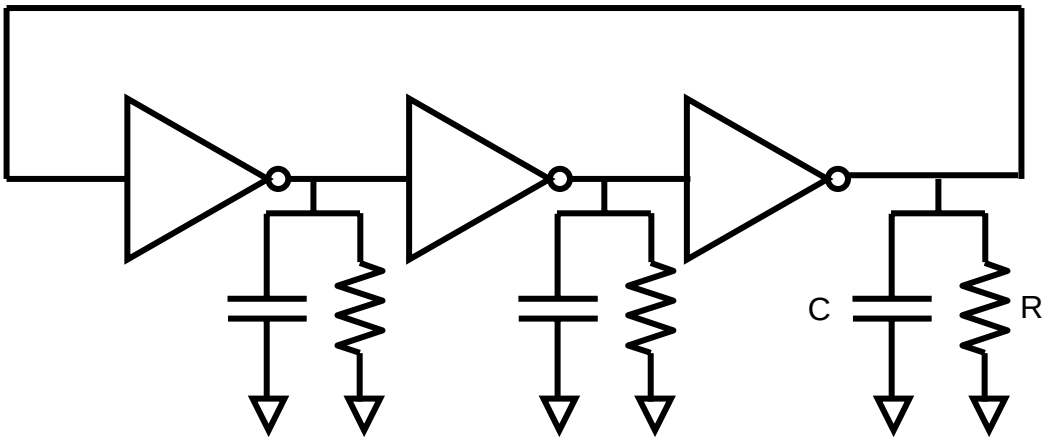

Figure 3.13 Ring oscillator

Small signal analysis can be used to estimate the oscillating frequency as well. The small signal transfer function of each delay cell and can be expressed as

$$G(s) = \frac{A}{s + \omega_p}$$

A is the low frequency gain of delay cell, and the pole, ω_p, is equal to the reciprocal of RC, shown in Figure 3.9. If we take three stages ring oscillator as example, the overall open loop gain is

$$H(s) = G^3(s) = \left(\frac{A}{s + \omega_p} \right)^3$$

To satisfy the Barkhausen Criteria, the extra 180^0 phase shift should be supplied by the loop. Hence, each cell should contribute 60^0, and then oscillating frequency can be estimated as

$$\phi = 60^0 = \tan^{-1}(\frac{\omega_0}{\omega_p}) = \tan^{-1}(\omega_0 RC)$$

$$\omega_0 = \frac{\sqrt{3}}{RC}$$

To get steady oscillation, the loop gain in the oscillating frequency must be equal or larger than one. Therefore,

$$\left|H(j\omega_0)\right| = \left(\frac{A}{\sqrt{\omega_0{}^2 + \omega_p{}^2}}\right)^3 \geq 1$$

$$A \geq 2\omega_p = \frac{2}{RC}$$

Thus, if the gain of delay cells is larger than $2/RC$, the ring oscillator will oscillate at $\sqrt{3}/RC$.

For the VCO, the relationship between the oscillating frequency and input tuning voltage is

$$\omega_o = \omega_{FR} + K_{VCO} \times V_{tune} \tag{3.3}$$

where K_{VCO} is the gain of VCO, defined as the VCO's sensitivity to the variation of the tuning voltage, and the ω_{FR} is the free-run frequency. The control action of the PLL depends on the comparison between the input reference phase and output divided phase. The transfer function of the tuning voltage to the output phase can be derived by

$$\phi_o(t) = \int_0^t \Delta\omega(t)\,dt = \int_0^t K_{VCO} \times V_{tune}\,dt$$

Through the Laplace-transform, it will become

$$\frac{\phi_o(s)}{V_{tune}} = \frac{K_{VCO}}{s}$$

Hence, the VCO acts like an integrator for the output phase, and provide a pole, locating at DC, to the whole PLL transfer function.

Some concerns are more critical han ohers for VCO design. Due to the non-linear characteristics of the PFD/CP/LPF and input noise, a noise signal will exist on the voltage control line of the VCO. This will lead to a variation on the tuning voltage. Then, this variation will be amplified by the K_{VCO}. Consequently, an amplified noise is yielded at the output signal. Therefore, to make PLL less sensitive to the noise, K_{VCO} should be designed as small as possible. From equation (3.3), to achieve wide frequency tuning range of the VCO, a large K_{VCO} is necessary. Thus, there is a trade-off between the frequency tuning range and the noise performance in the VCO design.

Trade-offs among the output voltage swing, supply voltage and power consumption must be fully analyzed in VCO design as well [6]. Invariably, a large output voltage swing is needed to increase the signal to noise ratio (SNR) and decrease the Noise Figure. However, this will set a lowest limit on the supply voltage. The large driving current needed for large voltage swing will cause the large power consumption. Therefore, depending on the requirements for different applications, a careful trade-off study should be made to optimize the VCO's performance.

3.4.3 The Frequency Divider

The Frequency Divider is put in the feedback path of the PLL and it is responsible for the frequency scaling. By tuning the frequency divider ratios, the locked frequency of PLL can be changed among the different channels. Since the control mechanism of the PLL relies on the comparison of phases in the PFD's inputs, the linear model of frequency divider is defined as the phase relationship between the output signals of VCO and the frequency divider's output signals. We assume the input phase in time domain is equal to

$$\theta_{in}(t) = 2\pi f_{in} t$$

f_{in} is the input frequency of frequency divider. After the frequency scaling, the output frequency f_{out} can be calculated as f_{in} / N. The output phase can be derived and expressed as

$$\theta_{out}(t) = 2\pi f_{out} t = 2\pi \frac{f_{in}}{N} t = \frac{\theta_{in}}{N}$$

Therefore, the transfer function of output to input phase of frequency divider is equal to 1/N.

As preceding exposition, the difference between the Integer-N frequency synthesizer and Fractional-N frequency synthesizer is the structure of frequency divider. The pulse-swallow divider, illustrated in Figure 3.14, is the most common structure for the Integer-N frequency synthesizer. By adding an accumulator to the pulse-swallow divider, the fractional divider ratio can be achieved for the Fractional-N frequency synthesizer. The pulse-swallow divider consists of a dual-modulus prescaler, a programmable counter and a swallow counter. The input of dual-modulus

prescaler is right connected to the output of VCO. This implies that the dual-modulus prescaler will operate at a very high frequency, such as 3.1 to 10.6 GHz for the UWB communication system.

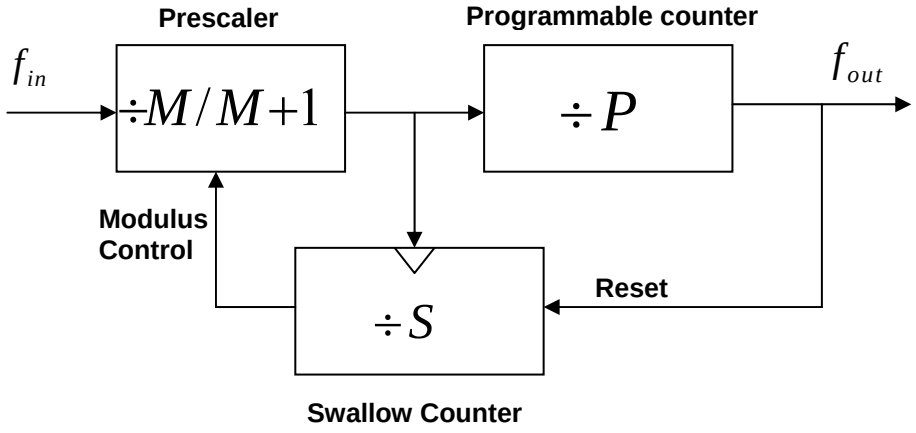

Figure 3.14 Pulse-Swallow frequency divider

Therefore, instead of the traditional digital-logic, much faster circuits should be used to implement the prescaler. The programmable counter can be easily programmed to set the particular divide ratio for different input reference frequencies. The number of pulses swallowed by the swallow counter is defined by the binary input of the swallow counter.

The operation of the pulse-swallow counter is described in the following. In the beginning, the swallow counter is reset to output a low state signal to the prescaler, which makes the prescaler start with a divide-by-M+1. After the swallow counter, (clocked by output signal of prescaler) counts S pulses, a high state signal is sent to prescaler. Then the divide ratio of prescaler becomes M. At that moment, S pulses with a divide-by-M+1 clock are counted by the programmable counter. After that, the

programmable counter will finish its remaining counts, P-S, with a divide-by-M clock. Hence the divide ratio can be expressed as

$$N = S \times (M + 1) + (P - S) \times M = PM + S$$

Once the programmable counter was programmed, the divide ratio "P" can't change any more. Therefore, the divide ratio of frequency divider can only be changed through the value of swallow counter.

3.4.4 The Loop Filter

In the phase locked condition, a steady voltage should be present at the tuning line of the VCO. To make this happen, the loop filter muat work as an integrator and provide infinite DC gain to the PLL. The loop filter is a very important component in the PLL because it determines to the loop's stability, settling time, noise performance and lock range. Basically, loop filters are separated into two categories: passive loop filters and active loop filters. If the tuning range of the PLL is very wide and the tuning voltage of VCO is too big to be provided by the charge pump, the active filter is used to implement the loop filter. For the fully integration purpose, the active filter can also be used to decrease the size of capacitor. However, the poor noise performance and large power consumption are the serious drawback of the active filter. For the sake of easy implement, better noise performance and lower power consumption, the passive filter is adopted in this thesis.

Assuming that the output impedance of the charge pump is infinite, the transfer function of the first-order low-pass filter is equal to

$$V_{out} = I_{CP} \times \frac{1}{sC} \Rightarrow \frac{V_{out}}{I_{CP}} = \frac{1}{sC}$$

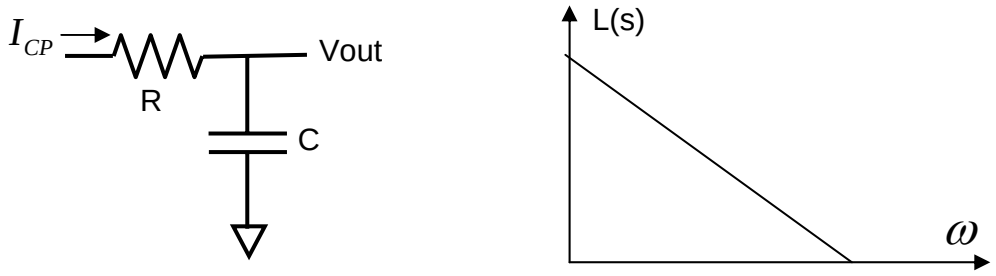

Figure 3.15 First-order low-pass filter

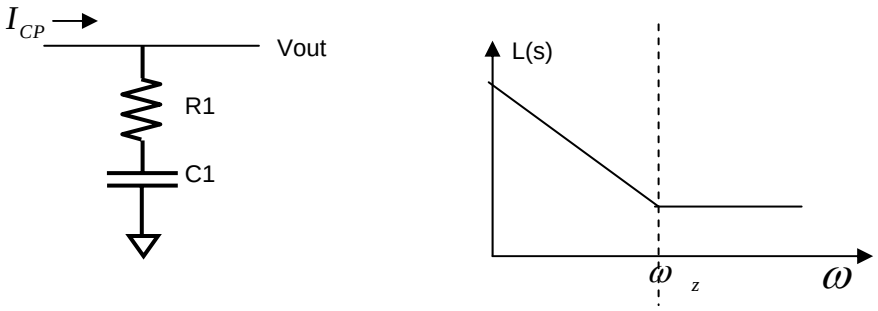

Figure 3.16 First-order low-pass filter with series resister

Its frequency response is shown in Figure 3.15. Due to a pole existing in the loop already, which is applied by the VCO, the second pole added to the loop by the first-order low-pass filter will make the PLL become unstable. By putting a resistor in series with the integration capacitor, a zero is generated to protect the loop from instability. Its frequency response is shown in Figure 3.16.

In addition to system stability, the noise performance of the PLL is also an important issue. The variation of the tuning voltage of VCO impacts the VCO's output spectrum seriously. The reference feed-through resulted from the current mismatch in the charge pump will add a high frequency ac signal on the tuning voltage, which leads to the reference spurs shown in the VCO's output spectrum. To reduce the voltage ripple on the tuning line, a capacitor is placed in shunt to make a second-order low-pass filter. The transfer function of the second-order low-pass filter is derived as follows:

$$V_{out} = I_{CP} \times (R_1 + \frac{1}{sC_1}) // \frac{1}{sC_2} = I_{CP} \times \frac{1 + sC_1R_1}{(sC_1R_1 + 1)sC_2 + sC_1}$$
$$L(s) = \frac{V_{out}}{I_{CP}} = \frac{1}{C_1 + C_2} \frac{1 + sC_1R_1}{s(1 + s\frac{C_1C_2}{C_1 + C_2}R_1)} \quad (3.4)$$

3.5 Frequency Response and Noise performance

3.5.1 Frequency Response of the Charge-pumped PLL

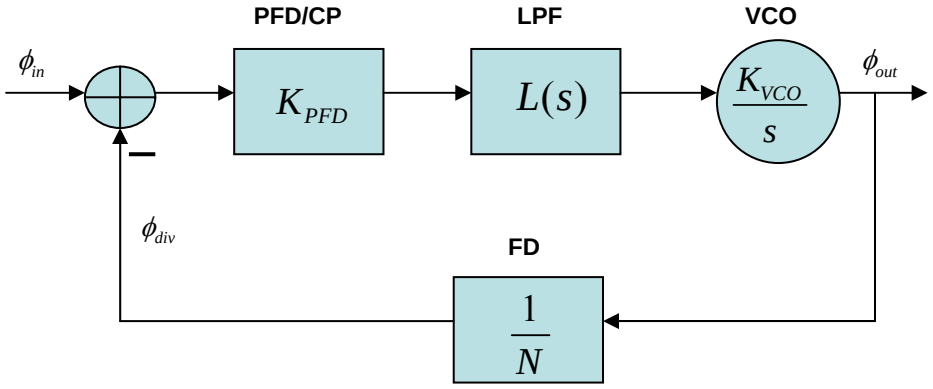

Figure 3.17 Loop diagram of a charge-pumped PLL

The linear model of the PLL in phase domain is illustrated in the Figure 3.13. The PFD/CP combination transfers the excess input phase to the charge current by the gain, K_{PFD}, equal to $I_{CP}/2\pi$. The loop filter coverts the charging current to the tuning voltage with the trans-impedance, $L(s)$. Feeding the output signal back to the input of PLL makes the output signal phase track the reference signal phase, and then achieves the phase locked condition.

If we open the loop by the output of frequency divider, the open-loop gain can be expressed as

$$G(s) = \frac{\phi_{div}}{\phi_{in}} = K_{PFD} \times L(s) \times \frac{K_{VCO}}{s} \times \frac{1}{N} \qquad (3.5)$$

Hence, the close-loop transfer function can be obtained

$$H(s) = \frac{G(s)}{1+G(s)} = \frac{\frac{K_{PFD}K_{VCO}}{N}L(s)}{s+\frac{K_{PFD}K_{VCO}}{N}L(s)} \qquad (3.6)$$

From the equation of loop's open-loop gain, we can see that the infinite DC gain is resulted from the pole, locating at the origin, provided by the VCO. This leads to a unit gain for the close-loop transfer function. That is to say, when the frequency of the variation of the excess input signal phase is low, the infinite open-loop gain forces the output phase variation to track the input phase variation. However, when the frequency goes up to the loop's bandwidth, the degradation of close-loop transfer function makes the excess output phase variation insensitive to that of input signal. This implies the low-pass characteristic of the open-loop gain makes the PLL can only track the slow variation of input signal. To improve the tracking speed, the loop-bandwidth of the PLL must be increased. However, according to [1], to make the Charge-Pump PLL behave like a continuous time system, a stability limit is set to

$$\omega_n{}^2 < \frac{\omega_{in}{}^2}{\pi(RC\omega_{in}+\pi)}$$

where ω_n is the nature frequency of the second-order system. To guarantee the stability of PLL, the loop bandwidth can not be too large (usually smaller than one-tenth of the input reference frequency.)

The settling time is a design parameter that relates to the tracking speed of the PLL. From [1], the settling time can be approximated as

$$t_s = \frac{1}{\varsigma\omega_n}\ln\frac{\Delta N}{N|\alpha|\sqrt{1-\varsigma^2}}$$

Where ς is the damping factor, N is the divide ratio of the frequency divider and α is the settling factor of frequency accuracy. Thus, wider loop bandwidth leads to shorter settling time and higher tracking speed.

Another very important design parameter is stability. To analyze the stability of the PLL, we need to put the loop filter's transfer function into open-loop transfer function of PLL first. From the equation (3.4), we express the second-order loop filter's transfer function as

$$L(s) = \frac{1}{C_1 + C_2} \frac{1 + \frac{s}{\omega_z}}{s(1 + \frac{s}{\omega_p})}$$

$$\omega_z = \frac{1}{R_1 C_1};\ \omega_p = \frac{C_1 + C_2}{C_1 C_2} \times \frac{1}{R_1}$$

Then, the open-loop transfer function can be expressed as

$$G(s) = \frac{K_{PFD} K_{VCO}}{N} \times \frac{s + \omega_z}{s^2 (s + \omega_p)} \qquad (3.7)$$

From the equation (3.7), the Bode plot of the open-loop transfer function is illustrated in Figure 3.18.

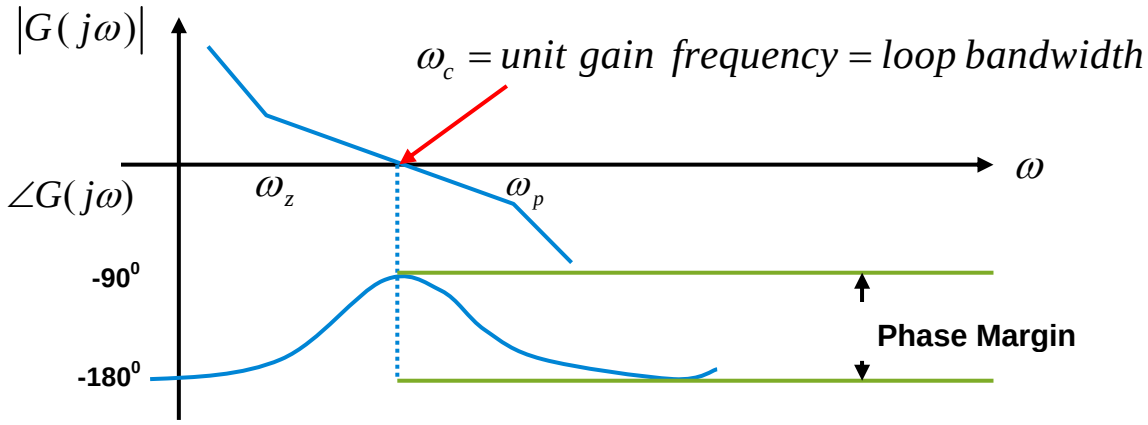

Figure 3.18 The frequency response of second order Charge-Pump PLL

Phase margin, usually used to determine stability, is defined as the difference between the 180 degree and the phase of open-loop transfer function with unit gain. It can be expressed as

$$\phi_M = 180^0 + \arg(G(j\omega_c)) \qquad (3.8)$$

To guarantee the stability of PLL, a phase margin larger than 45 degree is necessary. Through tuning the values of the pole and zero, we can set the location of unit gain frequency, and then optimize the phase margin.

3.5.2 Noise Performance of Charge-Pump PLL

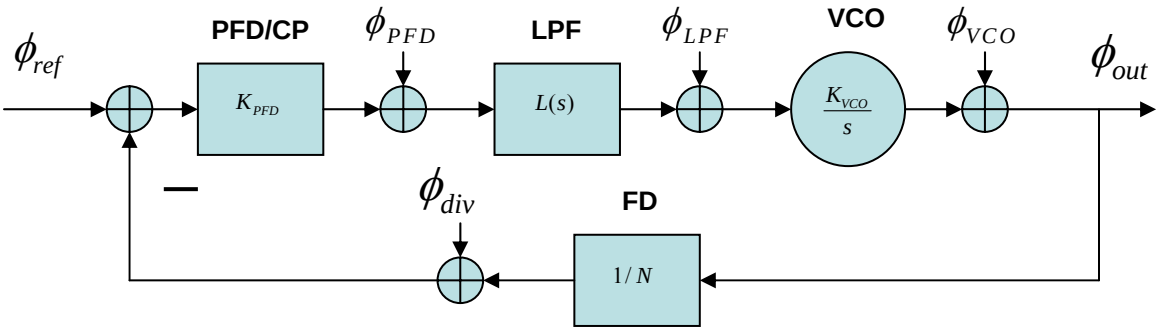

Figure 3.19 Noise sources in the Charge-Pump PLL

The noise sources added to the PLL are shown in Figure 3.19. In the following paragraph, we will talk about the contribution of these noise sources to the PLL's output noise. First of all, we talk about the noise injected by PFD, ϕ_{PFD}. The voltage power noise add to the signals through the registers and logic gates will cause the timing jitter in the logic transitions. The phase noise relates to the timing jitter by

$$S_{\phi PFD}(f_m) \propto \frac{\Delta t_d^{\,2}}{T_{ref}} \propto f_{ref} \qquad (3.9)$$

Figure 3.20(a) shows the "white noise" generated by the PFD. According to the relation (3.9), the amplitude of the white noise is positively related to the input reference frequency [5]. The noise transfer function from the PFD to PLL's output is needed to calculate the contribution of PFD's noise to the system. From the Figure 3.19, the noise transfer function of PFD can be expressed as

$$H_{PFD}(s) = \frac{K_{PFD}K_{VCO}\frac{L(s)}{s}N}{(N + K_{PFD}K_{VCO}\frac{L(s)}{s})K_{PFD}} = \frac{N}{K_{PFD}}\frac{G(s)}{1+G(s)}$$

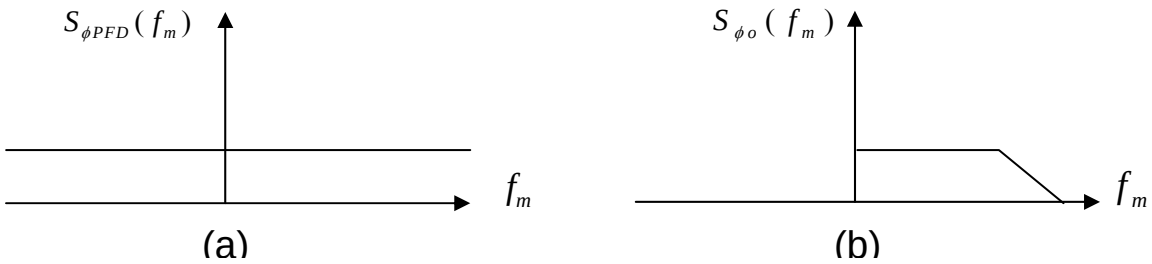

Figure 3.20 (a) white noise generated by PFD; (b) noise of PFD at the output of PLL

where G(s) is the open-loop gain defined in the equation (3.5). Because of the low-pass characteristics of G(s), the PFD's noise is filtered in the PLL and shown in Figure 3.20(b). Similar noise contribution is made by the frequency divider. Its transfer function is

$$H_{div}(s) = -N\frac{G(s)}{1+G(s)}$$

Before talking about the phase noise of the VCO, we start with the timing jitter. The random fluctuation caused by "white noise" in the time domain periodic signal causes a timing error in each period, called as jitter. If these timing errors exist in the VCO's signal, the prior timing errors will be accumulated and lead to the variation of the starting points of next oscillating cycles. By transferring timing jitter to the phase noise domain, we can see the power spectral density (PSD) of VCO's phase noise degrades with increasing offset frequency, f_m. From [5], the PSD of the oscillator is

$$\phi_{VCO}{}^2(f_m) \cong \frac{Fk_BT}{P_{RF}}\left[1+(\frac{f_{VCO}}{2Qf_m})^2\right](1+\frac{f_k}{f_m})$$

Its behavior shows in the Figure 3.17. As PFD's noise, the phase noise transfer function of VCO is used to calculate the VCO's contribution to the PLL's output phase noise. Through Figure 3.19,

$$H_{VCO}(s) = \frac{1}{1+G(s)}$$

A high-pass characteristic shows on VCO's noise transfer function.

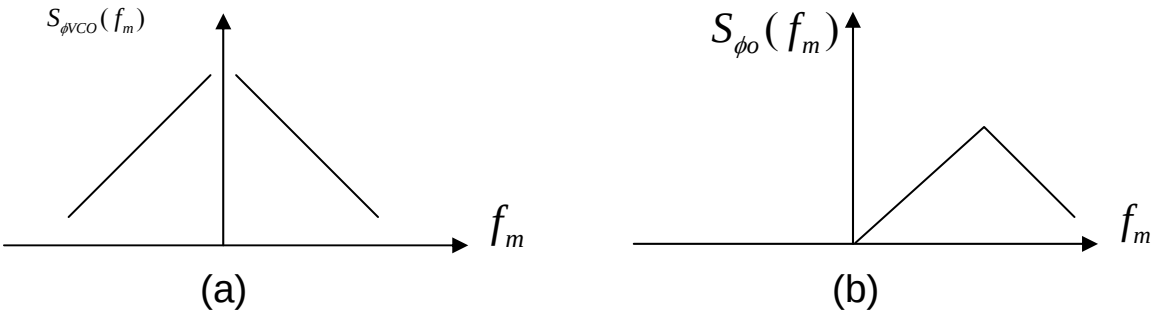

Figure 3.21 Noise contribution of VCO's phase noise

Similar to VCO, the input reference noise generated by crystal oscillator also has a $1/f_m^2$ dependency on the offset frequency, f_m. However, due to the physical structure, the input reference noise is much smaller than that of VCO. Through noise transfer function

$$H_{ref}(s) = N\frac{G(s)}{1+G(s)}$$

, the phase noise of input reference is filtered at high offset frequency. The last noise source is generated by the thermal noise of the series resister in the loop filter. Because the thermal noise is white noise, the loop filter's noise level is flat within the

whole band. Due to the band-pass characteristic of loop filter's noise transfer function, the output phase noise contributed by the loop filter is shown in Figure 3.22.

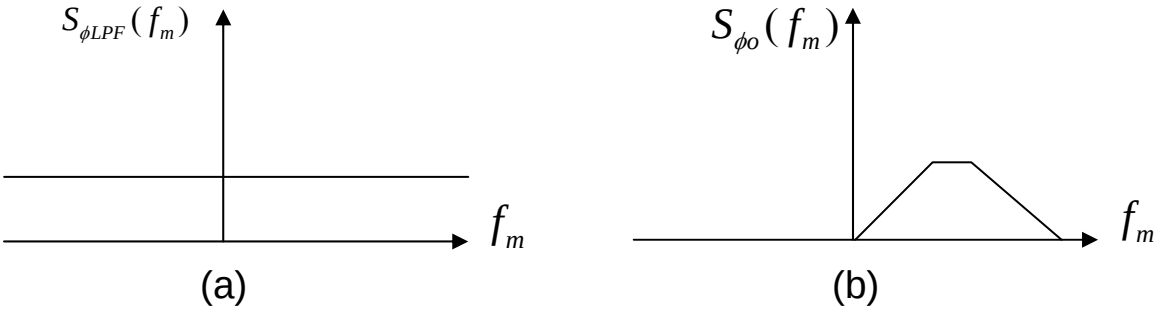

Figure 3.22 The transformed noise of LPF at the PLL's output

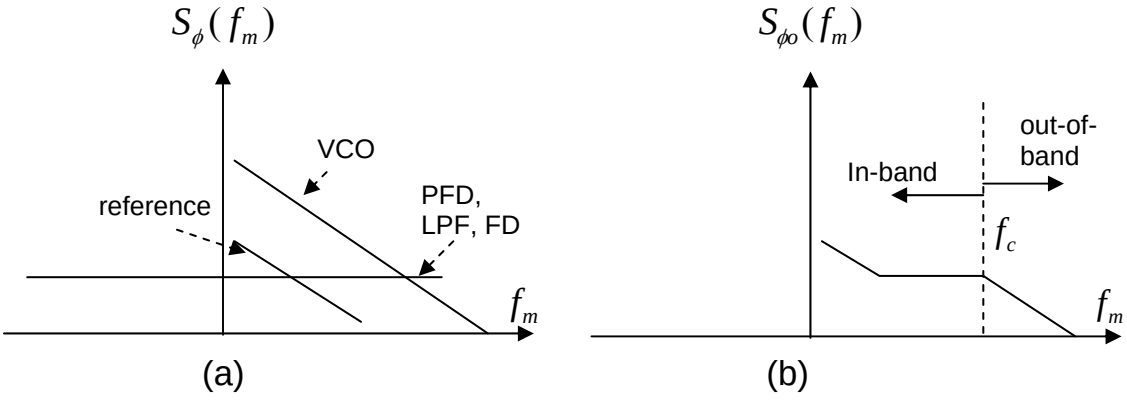

Figure 3.23 The noise appears at the output of PLL

Finally, we combine all the noises together in Figure 3.23. The Figure 3.23(a) shows the original PSD of every noise source. Through the noise transfer function, the output phase noise of PLL is shown in Figure 3.23(b). Because the phase noise of VCO is suppressed when the offset frequency is smaller than the crossover frequency, f_c, the phase noises generated by input reference, PFD and frequency

divider dominate the PLL's in-band phase noise. Conversely, when the offset frequency is higher than crossover frequency, VCO's phase noise will dominate the PLL's output phase noise. By observing the noise transfer functions described in above paragraphs, we can see the crossover frequency, f_c, is determined by the open loop bandwidth of PLL. Therefore, by tuning the loop bandwidth of PLL, we can decide the dominating component of PLL's phase noise.

Reference

[1] Behzad Razavi, *RF Microelectronics*, NJ: Prentice Hall PTR, 1998.

[2] H. Zheng et al., "RF System Architectures and Circuit Techniques for Wideband Transceivers," *IEEE Radio-Frequency Integration Technology*, Nov. 2005, pp. 30-37

[3] Bosco Leung, *VLSI for Wireless Communication*, NJ: Prentice Hall, 2002.

[4] G-Y T. *et al.*, "A 6.3-9 GHz CMOS Fast Settling PLL for MB-OFDM UWB Applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, Aug. 2005, pp. 1671-1679.

[5] Cicero S. Vaucher, *Architectures for RF frequency synthesizers*, Boston: Kluwer Academic Publishers, 2002.

[6] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, New York: McGraw-Hill, 2001.

4

Circuit Implementation

4.1 Semiconductor Technology Comparison: SiGe HBT vs. RF CMOS

Operating frequency, power consumption, linearity, bandwidth, phase noise, noise figure and settling time are the important figures of merit for the building components of the RF frequency synthesizer. For the progressive wireless communication systems, new architectures, communication theories, circuit topologies and semiconductor technologies are developed. Among these, semiconductor technology sets the very beginning limits of system performance. SiGe BiCMOS and RF CMOS are usually used to implement high frequency circuits. To compare these two technologies, some device's figures of merit are discussed in this section.

The key analog figures of merit of RF devices are short-circuit unity current gain frequency (f_T), maximum unity power gain frequency (f_{max}), flicker noise ($1/f$ noise), minimum noise figure ($NF_{\min}$), threshold voltage variation (σ_{th}),

linearity ($IIP3$), breakdown voltage and g_m / I. For high frequency operation, the most important parameter of active device is f_T. It is defined as the frequency interception with the 0-dB current gain. That is to say, f_T determines the highest operating frequency of active devices. The peak f_T of CMOS used to be much smaller than SiGe HBT. However, by the process of the silicon technology, the f_T of CMOS can be comparable with that of SiGe HBT, more than 200 GHz [1].

The maximum unity power gain frequencies, f_{max}, of CMOS and SiGe HBT are given by [2]

$$f_{\max}(CMOS) = \frac{f_T}{2\sqrt{R_{in}(g_{ds} + 2\pi f_T C_{gd})}}$$

$$f_{\max}(HBT) \cong \sqrt{\frac{f_T}{8\pi R_b C_{cb}}}$$

From the above equations, we can see f_{max} is positive proportional to f_T for both technologies. Because of the improved unity gain frequency of CMOS, its maximum unity power gain frequency is also increased to 200 GHz.

For the frequency synthesizer design, the flicker noise ($1/f$ noise) has a series impact on the phase noise of VCO. $1/f$ noise is a low frequency noise source, which is always lower than megahertz range [3]. It mainly results from the surface recombination effect in the transistors. Due to the current flowing along the connecting surface, CMOS is susceptible to the surface recombination effect. Conversely, the driving current of SiGe HBT flows vertically to the substrate, which leads to a much lower value of $1/f$ noise in HBT than CMOS [2].

The minimum noise figure ($NF_{\min}$) determines the degradation of the signal-to-noise ratio (SNR) results from a component. It can be approximated by [2]

$$NF_{\min}(CMOS) = 1 + 2(\frac{f}{f_T})\sqrt{\gamma g_{ds} R_{in}}$$

$$NF_{\min}(HBT) = 1 + \frac{1}{\beta} + \sqrt{2\frac{qI_C}{kT}R_b(\frac{f^2}{f_T{}^2} + \frac{1}{\beta}) + \frac{1}{\beta}}$$

Obviously, the minimum noise figure is dominated by the f_T. For a given noise figure, the component implemented by CMOS will cost a little more power than that made by SiGe HBT [1].

When the transistors work on a particular driving current, the variation of the threshold voltage (σ_{th}) will cause the variation of small-signal behavior. SiGe HBT is a bipolar transistor; its threshold voltage is mostly dominated by the band-gap of semiconductor. Conversely, the threshold voltage of CMOS transistor relies on the doping concentration, oxide thickness and substrate voltage etc. Therefore, the threshold voltage of CMOS is more susceptible to the fabrication variation than that of SiGe HBT.

Basically, the non-linear behavior of the transistors will lead to signal distortion. The third-order intercept point (II$P3$) is used to determine the small-signal linearity of a component. As discussed in [1], the II$P3$ of CMOS is usually larger than that of SiGe HBT. However, the non-linear cancellation effect applied for HBT components makes the third-order inter-modulation signals become much smaller. Therefore, the linearity of HBT components becomes better than CMOS components.

The high f_T of SiGe HBT can be used to trade off for high breakdown voltage and low power consumption [4]. As mentioned in the above paragraph, because of the

progressive technology, f_T of CMOS transistor is comparable to that of SiGe HBT. However, the improved f_T of CMOS is achieved by scaling the size of transistors, which makes large breakdown voltage a challenge due to the thinner gate oxide for each new generation process.

The g_m / I ratio of SiGe HBT is always much larger than that of CMOS. Because of the exponential relation between the driving current and biased voltage, the inherent trans-conductance of HBT is higher. This implies that the HBT has a higher current driving ability than CMOS. Hence, the output buffer is always implemented by HBT.

Because the frequency synthesizer presented in this thesis is used for Ultrawide-Band (UWB) applications, high f_T, f_{max}, g_m / I and low power consumption, phase noise and σ_{th} are necessary. For the concern of low cost, CMOS is always thought as the only choice for System-on-Chip (SOC). However, as reported in [2], the System-in-Package (SIP) could offer the lower cost for RF application than SOC, which means the cost advantage of SiGe BiCMOS is comparable with that of CMOS. Therefore, the SiGe BiCMOS technology is chosen to implement the building blocks of the PLL in this thesis.

4.2 Phase/ Frequency Detector and Charge Pump

4.2.1 Phase/ Frequency Detector Implementation

By detecting the input phase and frequency difference, PFD generates a correction signal to trigger the frequency acquisition in PLL. The pulse width, delay and direction of the generated correction signals will impact the performance of PLL consequently. There are several issues should be taken into account for effective PFD design such as "dead zone", large operating frequency and settling speed requested for wideband applications.

To overcome the "dead zone" problem, an extra delay is usually inserted in the reset path of the conventional PFD, shown in Figure 4.1. However, the inserted delay time will decrease the PFD's speed and maximum operating frequency, which leads to slower settling time of PLL [5]. With the extended reset time, the relation between the phase error and average output voltage is shown in Figure 4.2. While the phase error is in the range between $2\pi - \Delta$ and 2π , the rising edge of the D-FF's input signal will be missed in the reset delay period, which leads to the wrong correction signal in the output of PFD.

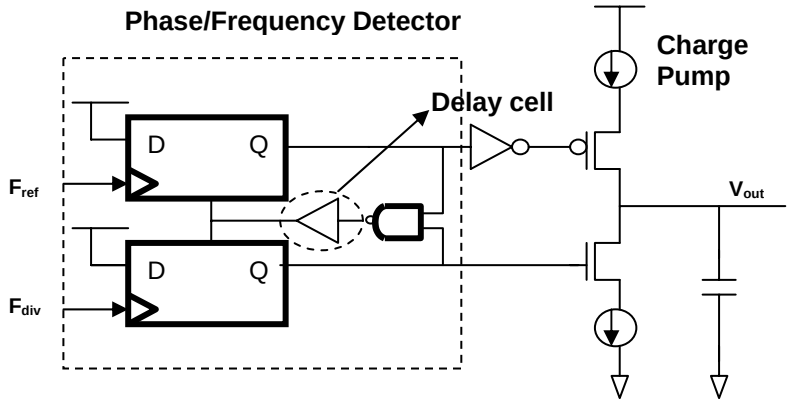

Figure 4.1 The block diagram of PFD/CP with delay cell

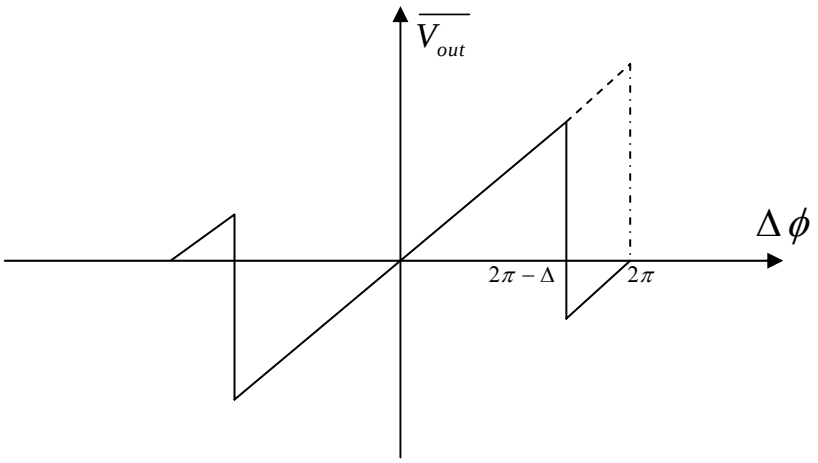

Figure 4.2 Wrong correction signals generated by PFD

According to [5], the radian of reset period (Δ) is

$$\Delta = 2\pi \frac{t_{reset}}{T_{reference}}$$

where t_{reset} is the reset delay time of PFD, and $T_{reference}$ is the period of input reference signal. When the t_{reset} becomes as large as half of $T_{reference}$, the wrong correction signals will be generated in a half period of input reference signal. This results in the failure to achieve frequency acquisition. Hence, the maximum input reference frequency is limited to be less than $1/(2t_{reset})$ [5] [6]. That is to say, to obtain the higher input reference frequency for PFD, which is necessary for the short locking time in the PLL, the smaller delay time of reset path should be achieved.

However, because of the restriction on the "dead zone" problem, the reset time can't be decreased without limit. To figure out the minimum width of voltage pulse necessary to eliminate "dead zone", accurate simulation must be made. Through the Cadence Design Systems simulator, we find that a 250ps voltage pulse is wide enough to turn on the current switches in charge pump. According to above

paragraph, this reset delay makes the operating frequency as high as 2 GHz, which is much higher than the input reference frequency used in this thesis, 264 MHz.

The True Single-Phase Clock (TSPC) positive edge triggered D Flip-Flop is adopted for the proposed PFD, shown in Figure 4.3. Compared with the conventional edge triggered D Flip-Flop made by static complementary logics, TSPC D Flip-Flop has the advantages of high speed, low power consumption and simple structure [7]. The behavior of proposed PFD is shown in Figure 4.4 (a) (b). The width of reset pulse can be measured by the Down pulse in case 1 and Up pulse in case 2. To overcome the two issues for PFD design, speed limitation and dead zone, a particular reset time should be set.

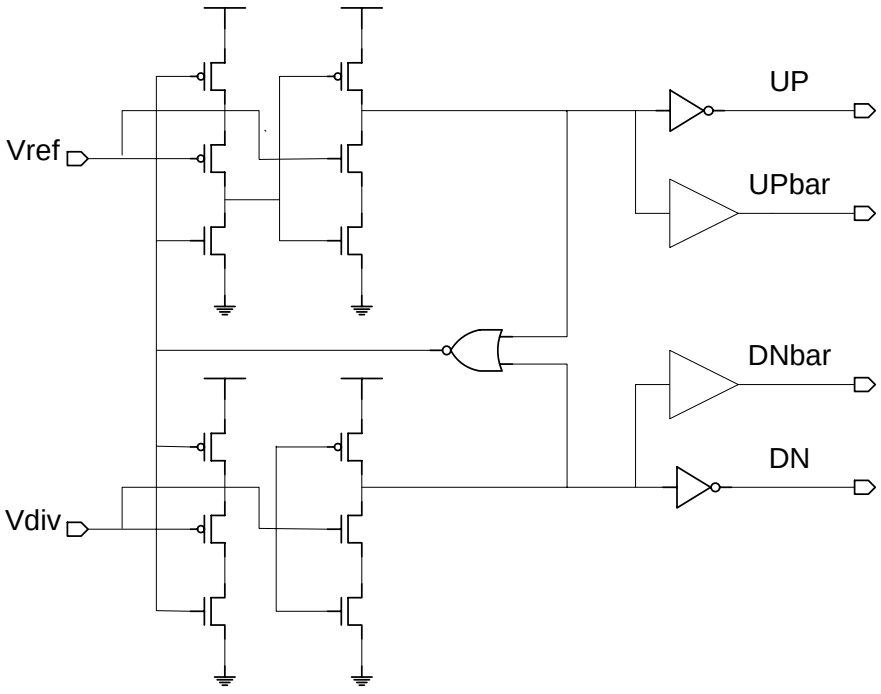

Figure 4.3 Schematic of PFD

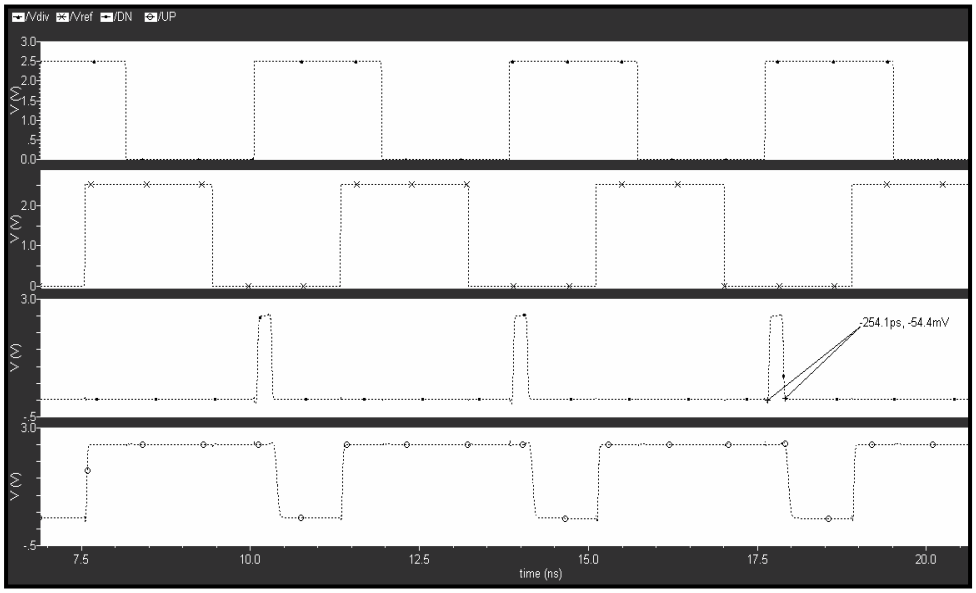

Figure 4.4 (a) divided output signal phase lags input signal phase

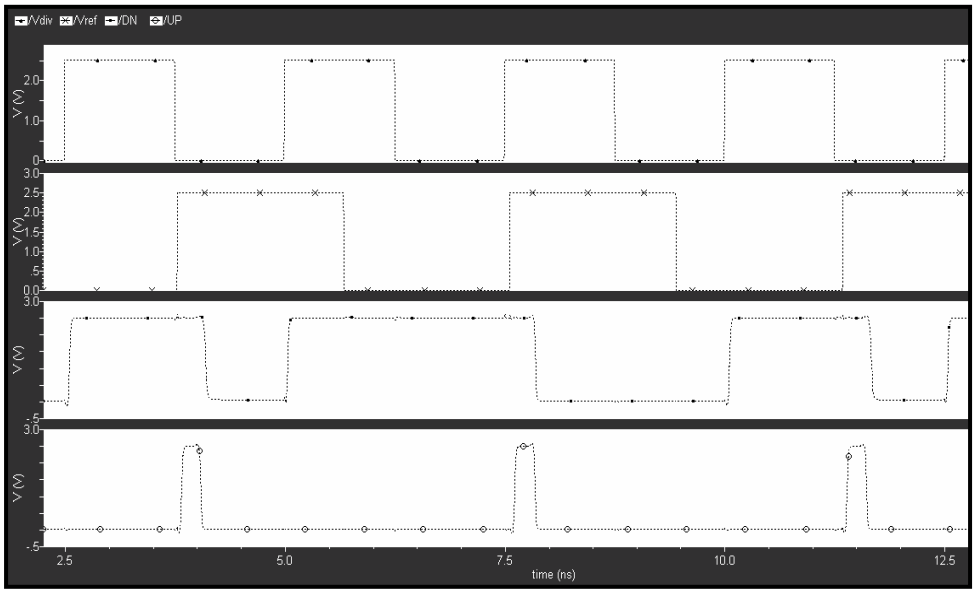

Figure 4.4 (b) divided output frequency is higher than input reference frequency

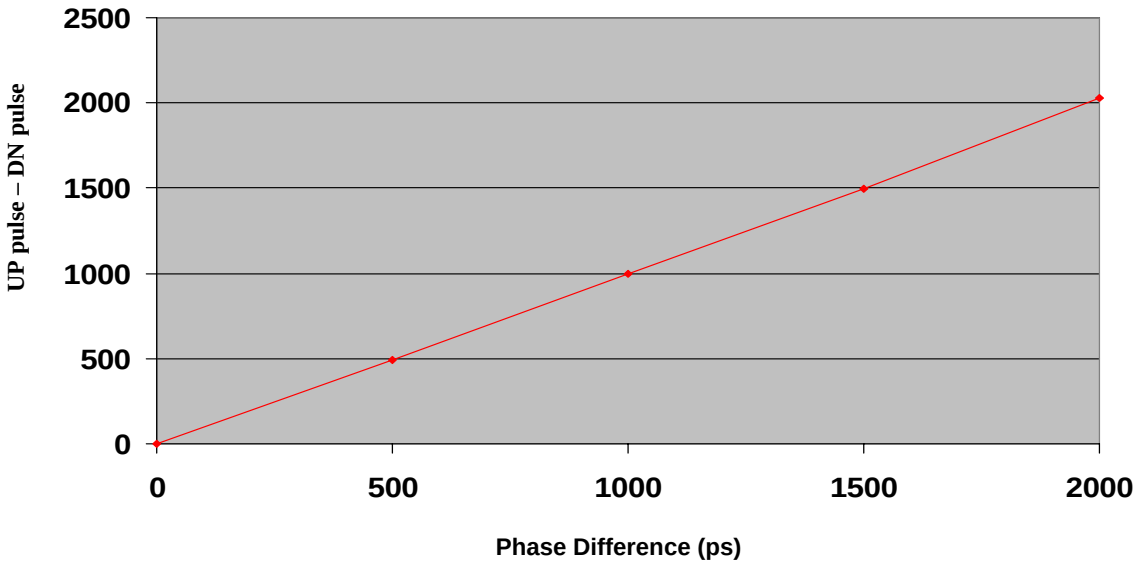

Figure 4.5 Phase difference vs. net pulse width generated by PFD

As shown in Figure 4.4 (a), the reset time is designed to be 250ps. With the 250ps reset time, the relation between input phase difference of PFD and net pulse width of PFD's output is plot in Figure 4.5, simulated by Spectre. Obviously, the dead zone disappears in the proposed design. As well, the differences between Up and Down pulse width show linear response to the input phase difference.

4.2.2 Charge Pump Implementation

Many non-ideal characteristics of the PLL, such as reference spurs and limited tuning range of VCO result from the charge pump circuit. To improve the performance of the PLL, charge sharing, source/ sink mismatch and output voltage range are the issues should be accounted for in charge pump design. In the conventional charge pump circuit, shown in Figure 4.6, the charge sharing problem is dealt with using a unity-gain buffer between the turn-off charge pump output and turn-on charge pump output [8]. The unit-gain buffer forces the turn-off charge pump output to be equal to main charge pump output. Therefore, the jump phenomenon resulted from charge sharing is relieved. However, the cost is an additional rail-to-rail OP amplifier, which will cost large die area and power consumption. As well, the OP amplifier will increase the complexity of the whole charge pump structure [9].

The proposed charge pump structure is shown in Figure 4.7. Without the current sources cascading with input switches directly, there is no charge sharing problem in this structure. The symmetric differential pairs are used to be the Up and Down input stages.

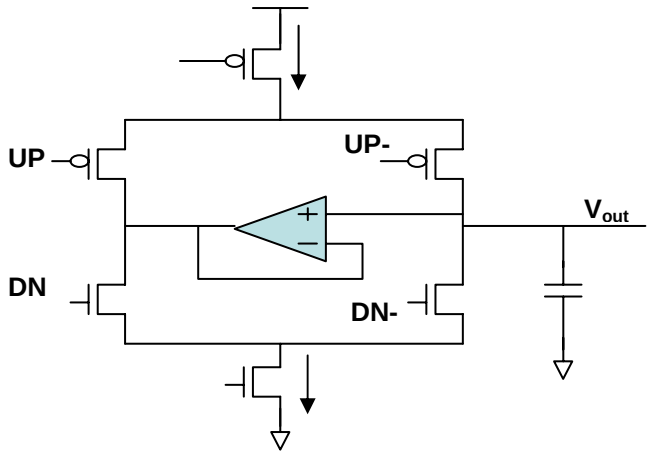

Figure 4.6 Conventional charge pump circuit

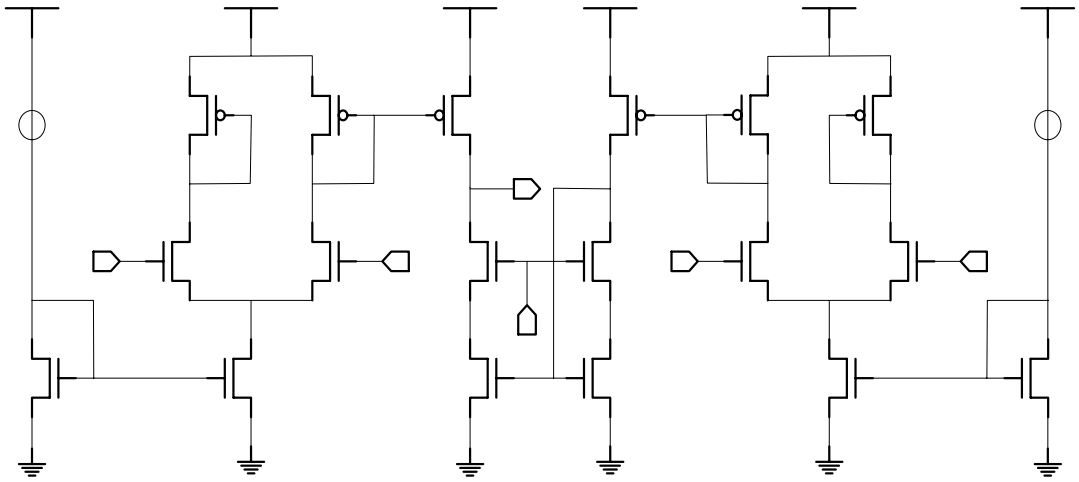

Figure 4.7 Schematic of designed charge pump

UPbar UP

Due to the NMOS differential pairs applied in both inputs, the inherent mismatch of NMOS and PMOS is removed [10]. To obtain good current matching in the output of charge pump, great input switch matching is not enough. Large output impedance is also necessary. If the output impedance of charge pump is not large enough, the output current mismatch will change with different output voltages, which be expressed as [11]

$$\Delta I = 2\frac{(V_{out} - V_{equ})}{r_o} \propto (V_{out} - V_{equ})\lambda I_{DS} \propto \frac{(V_{out} - V_{equ})I_{DS}}{L} \quad (4.1)$$

where V_{equ} is the output voltage that makes the source and sink current become equal, I_{DS} is the bias current, r_o and L are the output impedance and channel length of transistors in current mirror respectively. From equation (4.1), it is obvious that by increasing the channel length of T3 and T4 in Figure 4.7, we can decrease the current mismatch and provide a large output impedance. To understand the importance of the

current matching in the charge pump, we can see the reference spurs in a 3rd-order PLL. The power of the reference spurs can be expressed as [12]

$$Spur = 20\log\left(\frac{\sqrt{2}\frac{I_{CP}R}{2\pi}\times\phi_e\times K_{VCO}}{2f_{ref}}\right) - 20\log(\frac{f_{ref}}{f_{pl}}) = 20\log(\frac{1}{\sqrt{2}}\frac{f_{BW}}{f_{ref}}\times N\times\phi_e) - 20\log(\frac{f_{ref}}{f_{pl}}) \quad (4.2)$$

$$\phi_e = \frac{I_{leak}}{K_{PFD/CP}} = \frac{2\pi}{I_{CP}}\times\frac{\Delta t_{on}}{T_{ref}}\Delta I$$

In equation (4.2), the current mismatch of the charge pump is converted to the input phase error and lead to the reference spur out of PLL.

In addition to noise contribution, the output voltage range is also an issue for charge pump design. In the 3rd-order PLL, the output voltage range of charge pump controls the input voltage range of VCO, hence the output frequency. Therefore, for large input voltage range of VCO, the headroom of current mirrors in the charge pump circuit should be reduced to be as small as possible. The saturation voltage of transistors, T3 and T4, in the current mirrors can be expressed as

$$V_{sat} = \sqrt{\frac{2I_{CP}}{\mu C_{ox}(W/L)}}$$

To keep saturation voltage small, the W/L ratio should be large. Because long channel length is required for large output impedance, large W/L ratio leads to large transistor sizes of current mirrors' transistors. This implies a long switch time will be taken for input differential pair. Therefore, a trade-off between large output range and fast operation frequency exists in the current mirror's transistor design.

The completely switching voltage of input differential pairs is also a design issue. The completely switching voltage can be calculated by

$$V_S = \sqrt{\frac{2I_{CP}}{\mu C_{ox}(W/L)}} \qquad (4.3)$$

Depending on the output swing of PFD, the transistor size of input differential pairs, T5, T6, T12 and T13 in Figure 4.7, should be designed following the equation (4.3).

Figure 4.8 (a) (b) shows the output current and voltage of charge pump in two different conditions: divided output phase lags the input reference phase, and divided output frequency is higher than input reference frequency.

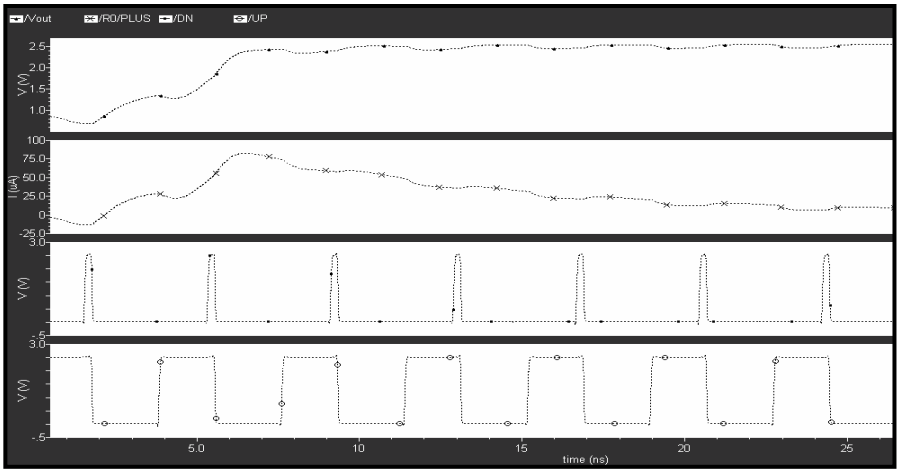

Figure 4.8 (a) divided output phase lags input reference phase

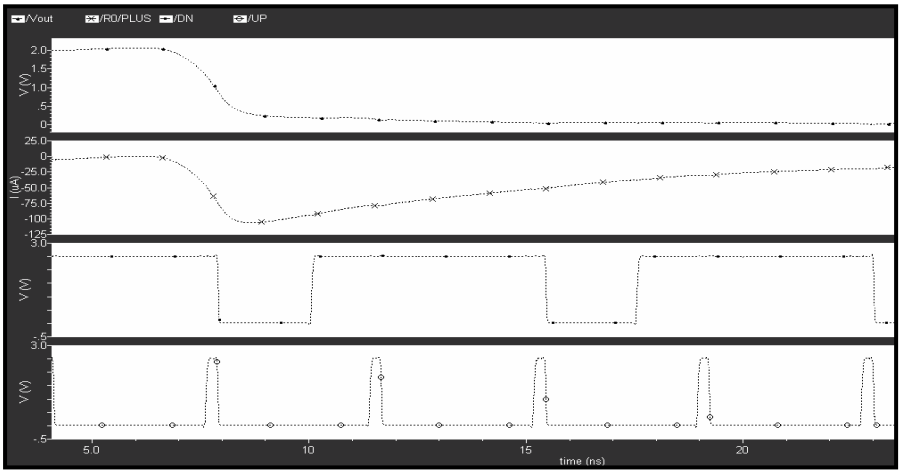

Figure 4.8 (b) divided output frequency is higher than input reference frequency

4.2.3 Noise Performance of PFD/ CP Combination

The shot noise and flicker (1/f) noise in the PFD and charge pump circuits lead to noise current in the output of charge pump. To calculate the phase noise contribution of the PFD/ CP to the PLL, the output noise current should be referred to the input of PFD. The referred phase noise is expressed as

$$\phi_{PFD/CP} = \frac{\Delta I_{noise}}{K_{PFD/CP}} = 2\pi \frac{\Delta I_{noise}}{I_{CP}} \qquad (4.4)$$

From equation (4.4), to reduce the phase noise of PFD/ CP combination, we can source a large current in the charge pump circuit. The price of large charge pump current is the long switching time induced from the large size of the transistors, which will result in phase noise degradation [11]. Thus, to find out the appropriate charging current for optimal phase noise, we need the help of simulation tools.

Through the SpectreRF simulation, the current noise, with 500 uA charge pump current, at the output of charge pump circuit is shown in Figure 4.9. From the Figure 4.9, we can see the unit of current noise is $A/\sqrt{Hz}$. The unit of the power density of input phase noise, $\phi_{PFD/CP}{}^2$, is rad^2/Hz. To convert current noise ($A/\sqrt{Hz}$) to power density of phase noise (rad^2/Hz), we need a translator equal to

$$T = \frac{rad/\sqrt{Hz}}{A/\sqrt{Hz}} = \frac{rad}{A}$$

which can be made by the reciprocal of PFD/ CP gain. This matches the result provided by equation (4.4). By the data extracted from the Cadence simulation result, the referred phase noise can be calculated and plotted by Matlab, shown in Figure 4.10.

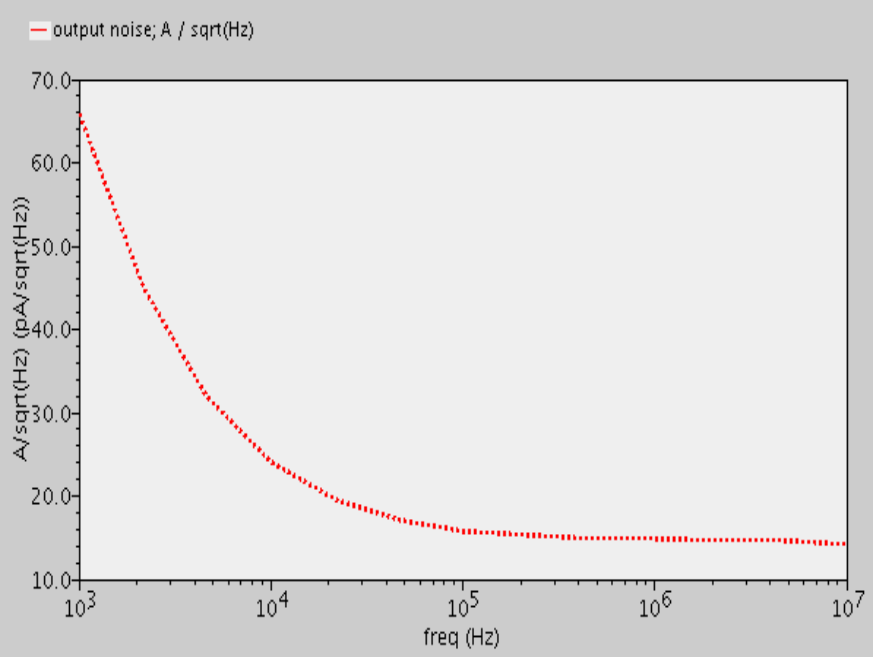

Figure 4.9 Noise current of PFD/CP combination

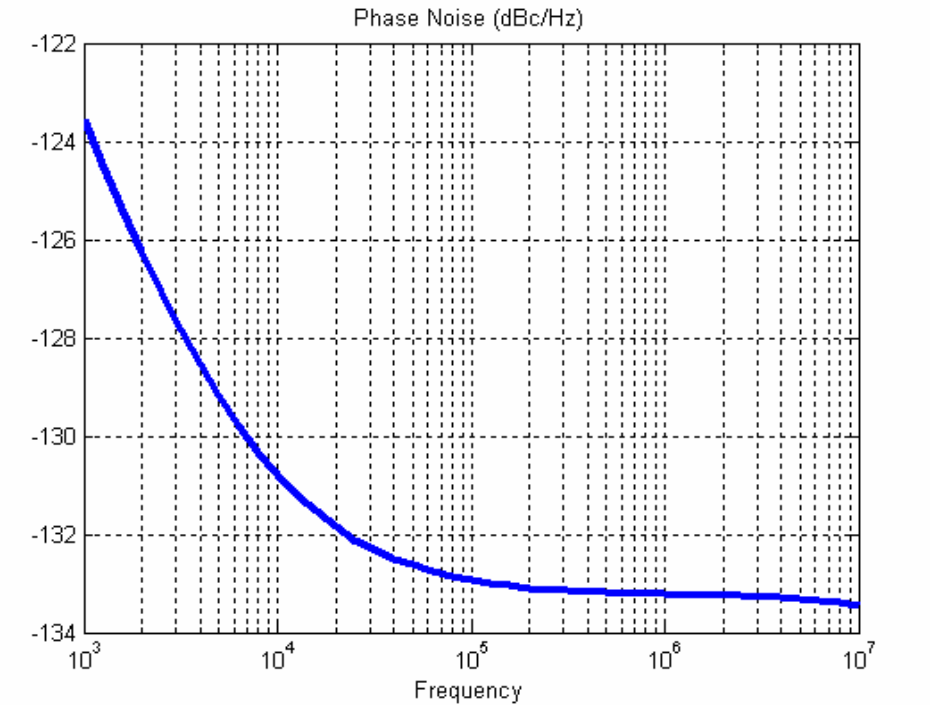

Figure 4.10 Converted phase noise at the input of PFD

4.3 Voltage Controlled Oscillator (VCO)

4.3.1 Ring Oscillator Implementation

To get wide frequency tuning range, small silicon area and low distortion quadrature signals, ring oscillator is employed in this thesis. The main drawback of ring oscillator is the higher phase noise than that of LC-oscillator. For the QPSK modulation scheme, used in the MB-OFDM UWB communication system, the relaxed phase noise requirement can also be satisfied by ring oscillators without large amount of power consumption. Thus, ring oscillator is adopted to implement the VCO in the presented PLL.

As mentioned in Chapter 3, large signal analysis yields an oscillating frequency for the ring oscillator given by:

$$f_{osc} = \frac{1}{2N\tau} \qquad (4.5)$$

where N and τ represent the number of delay stages and delay time of each stage. With 180 degree shift in DC, the forward path of ring oscillator should provide additional 180 degree phase shift for the oscillation. Hence, to obtain the inherent quadrature signals from the ring oscillators, two stages is the most suitable architecture. The quadrature signals could be obtained from the output of each stage, shown in Figure 4.11. The two-stage ring oscillator can save power and reduce chip area.

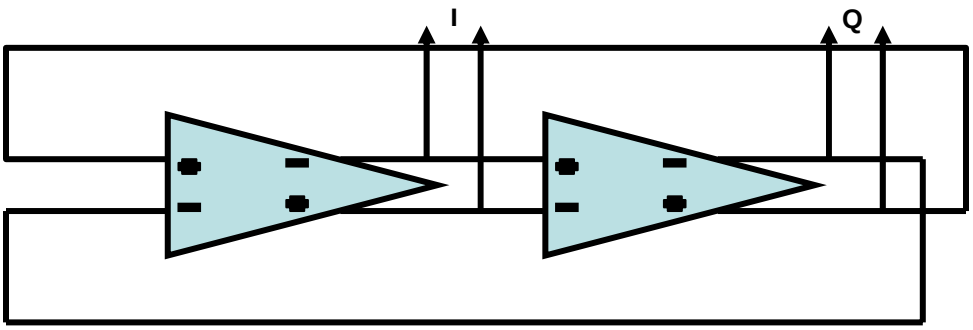

Figure 4.11 Two-stage ring oscillator with quadrature output

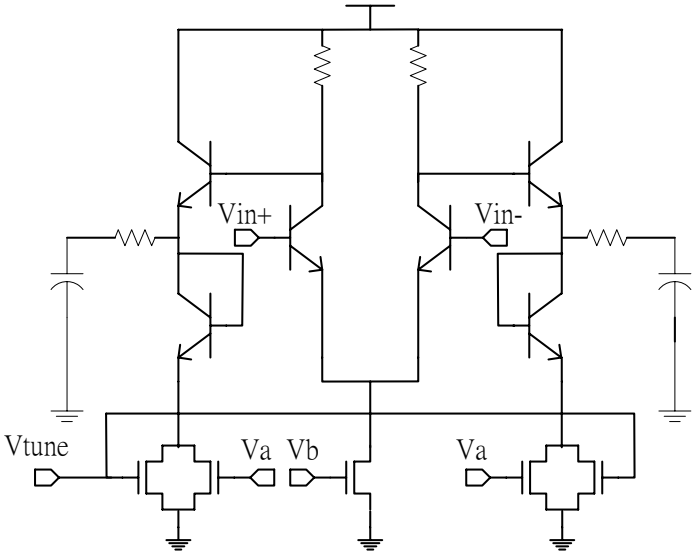

Figure 4.12 Delay stage of ring oscillator

To provide a 90 degree phase shift in each stage of the ring oscillator, a two-pole delay stage is employed, shown in Figure 4.12. The diode-connecting transistors involved in the emitter followers prevent the transistors, Q7 and Q12, from the breakdown. The delay time of the stage is controlled by the biasing current. Therefore, by tuning the tail current of the delay stage, we can change the operating frequency of the proposed VCO as expressed in equation (4.5). The main drawback

arisen from the current controlled mechanism is the variation of oscillating amplitude. In [13], the differential output voltage is approximated by

$$V_o = I_B R_L - V_T \ln\left(\frac{I_B + \frac{V_{c2}}{r_\pi}}{I_B + \frac{V_{c1}}{2r_\pi}}\right) \qquad (4.6)$$

Where I_B, R_L *and* r_π are represented biasing current, loading resistances of differential pair and input resistance of Q1, respectively. To minimize the variation of output voltage in (4.6), the bias current of input differential pair is set to be constant. That is to say, the frequency tuning of the proposed oscillator is made by the current variation in the emitter followers.

The emitter followers connected to the output of input differential pairs provide the second pole to the delay stage. By the open circuit time constant analysis, two poles can be given by [13]

$$\omega_{p1} = \frac{1}{R_L C_{CL}}$$
$$\omega_{p2} = \frac{1}{(r_b + \frac{1}{gm_{7,12}})C_\pi} \qquad (4.7)$$

where C_{CL} is due to the capacitance appeared at the output of differential pair, r_b represents the base resistance of Q7, and C_π is the base-emitter capacitance. Appling above delay stage to the two-stage ring oscillator, shown in Figure 4.13, the oscillation frequency can be approximated by Barkhausen criteria according to the procedure described in Chapter 3, and expressed as

$$\omega_o = \sqrt{\omega_{p1}\omega_{p2}} \qquad (4.8)$$

Substituting (4.7) into equation (4.8), we can write the oscillation frequency as:

$$f_o = \frac{1}{2\pi\sqrt{R_L C_{CL}\left(r_b + \frac{1}{gm_{7,12}}\right)C_\pi}} \qquad (4.9)$$

Therefore, by changing the tail current in the emitter follower, we can tune the operating frequency of the ring oscillator.

If we use the output voltages of the loop filter in the PLL to bias the current circuitry in the delay cell, the current of CMOS transistors grows quadratically with increasing bias voltage, which leads to the non-linear relation between control voltage and oscillating frequency.

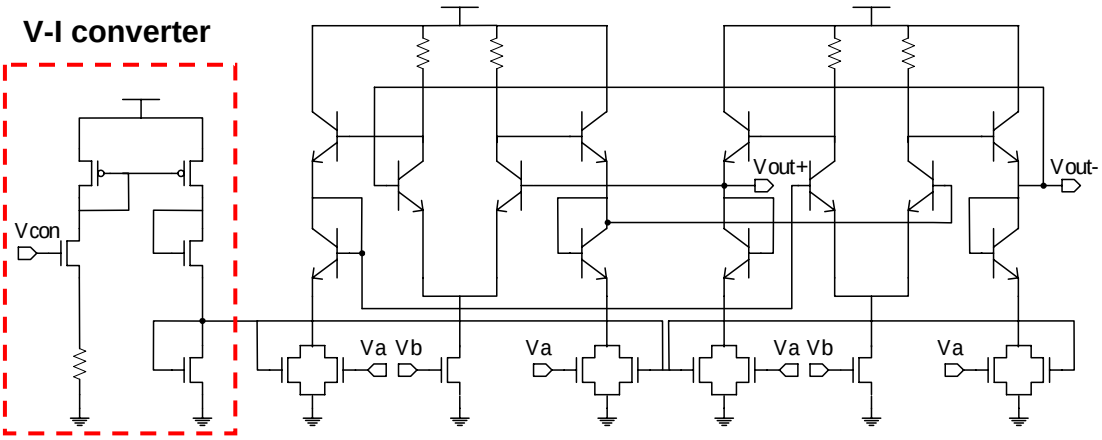

Figure 4.13 Two-stage ring oscillator with V-I converter

To improve the linearity of the VCO behavior, a voltage to current converter, shown in Figure 4.13, is added. With the large W/L ratio of the input transistor in the V-I converter, the induced current can be approximated by

$$I_{bias} = \frac{V_{tune} - V_{th}}{R_s}$$

which implies a linear relation between the input tuning voltage and output oscillating frequency. Figure 4.14 (a), (b) and (c) show the output wave form and spectrum of the three particular carriers, 3432, 3960 and 4488 MHz, by the SpectreRF simulation. The plots of tuning voltage from the loop filter versus corresponding VCO output frequencies are shown in Figure 4.15 and 4.16. Through Figure 4.15, 4.16 and the definition given in Chapter 3, the VCO gain is equal to

$$K_{VCO} = \frac{\omega_o - \omega_{FR}}{V_{tune}} = \frac{4488 - 3432}{2.235 - 0.57} \times 10^6 = 634\ MHz/V$$

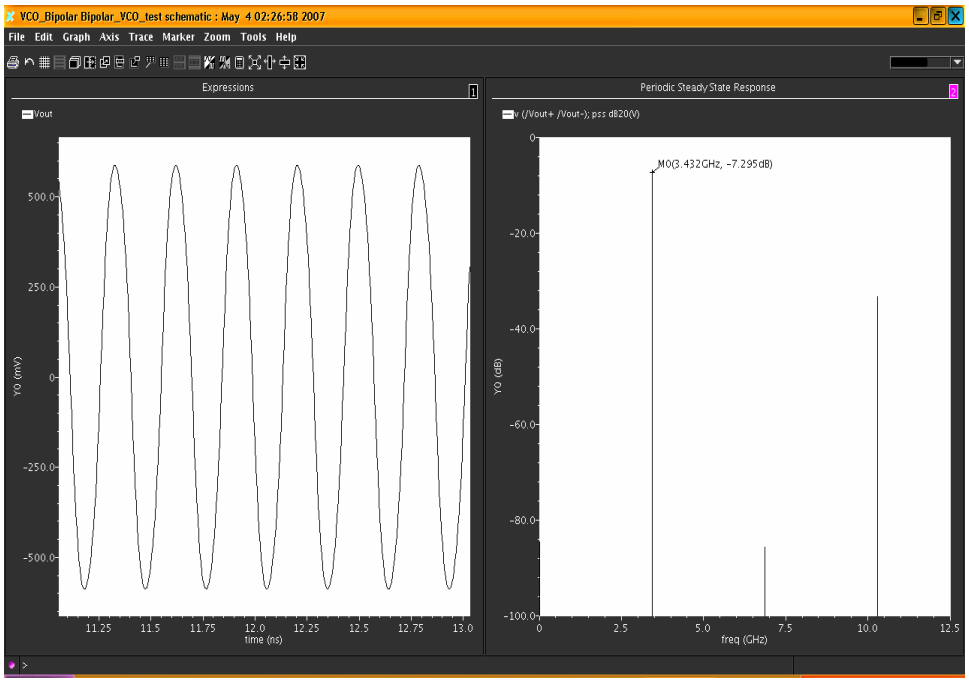

Figure 4.14 (a) the output wave and spectrum of the carrier in 3.432 GHz

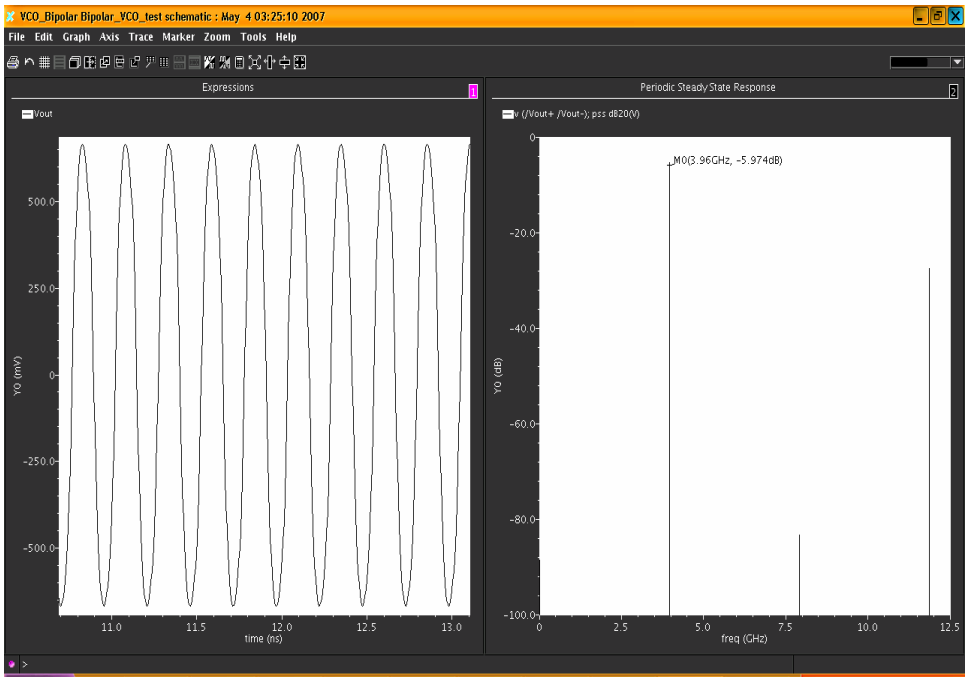

Figure 4.14 (b) the output wave and spectrum of the carrier in 3.96 GHz

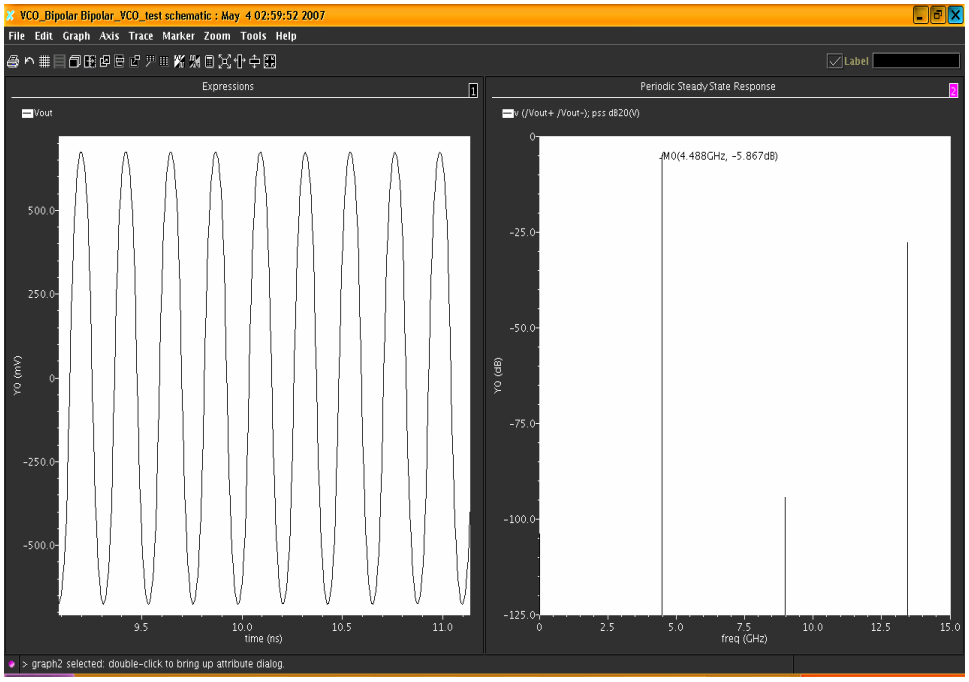

Figure 4.14 (c) the output wave and spectrum of the carrier in 4.488 GHz

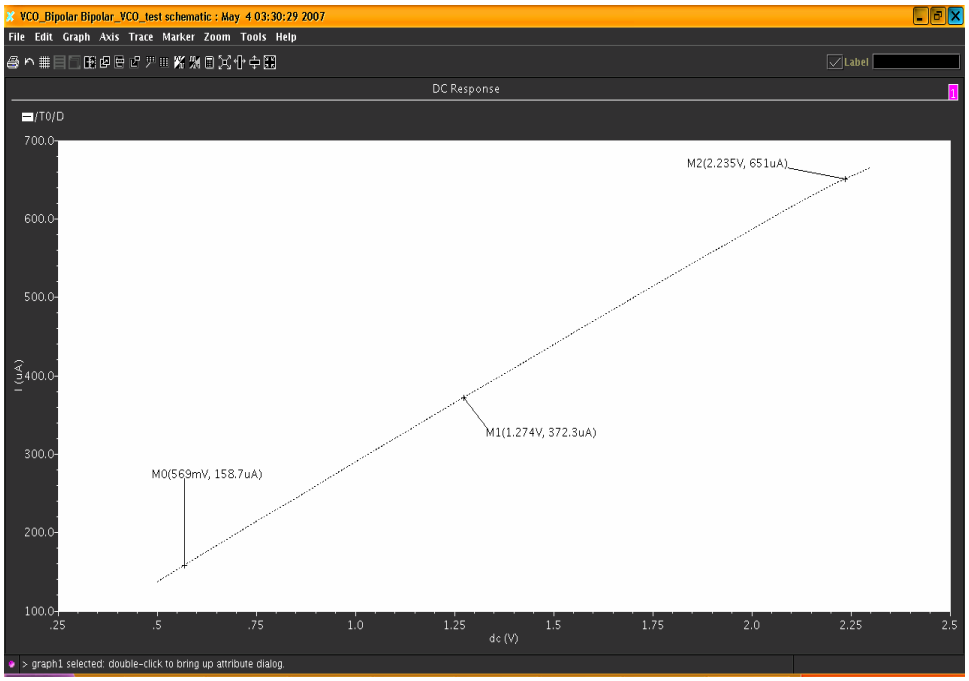

Figure 4.15 tuning voltage vs. induced current in delay stage

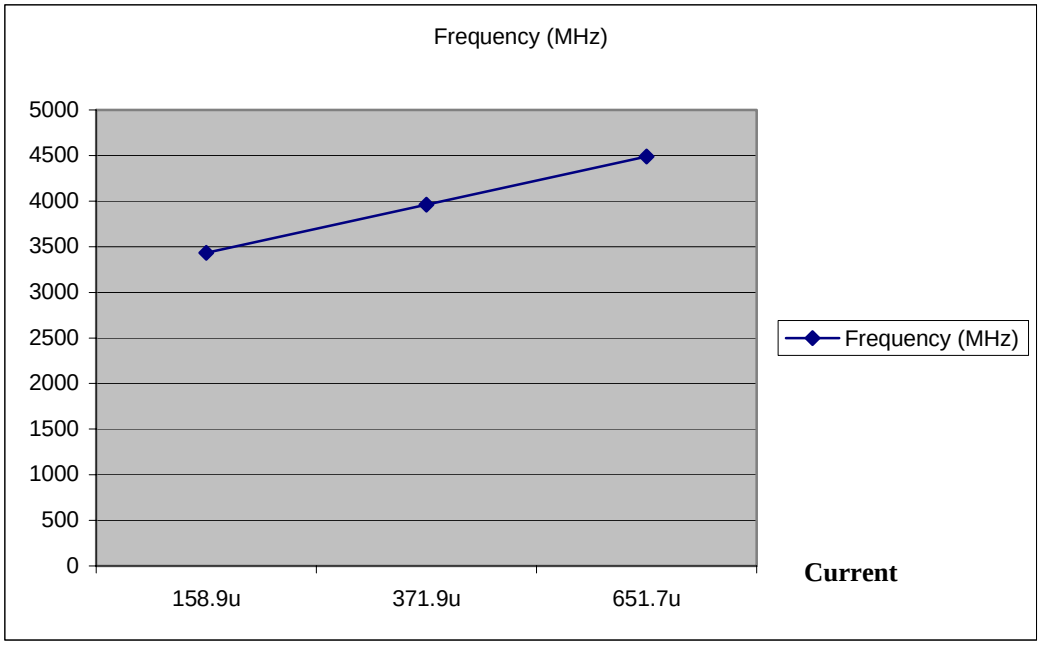

Figure 4.16 tail current vs. output frequency of VCO

4.3.2 Noise performance of VCO

Conventionally, the phase noise of VCO is the most critical requirement for the PLL design. This is because the phase noise of VCO dominates the phase noise of the PLL. However, due to the large open-loop bandwidth of the PLL for the UWB communication, the in-band phase noise of PLL, which is determined by the noise induced from reference source, PFD/ CP and frequency divider, become important. Therefore, the requirement of the phase noise of VCO is relaxed for the applications of UWB communication.

According to [15], the phase noise of the differential ring oscillators can be expressed as

$$L_{\min}\{\Delta f\} = 10\log\left[\frac{8}{3\eta}\times N\times\frac{kT}{P}\times\left(\frac{V_{dd}}{4V_t}+\frac{V_{dd}}{I_{tail}R_L}\right)\left(\frac{f_o}{\Delta f}\right)^2\right] \qquad (4.10)$$

Here, N is number of stages, P is the power dissipation of the oscillator, V_t is the thermal noise and Δf is the offset frequency from the oscillating frequency f_o. From the equation (4.10), it's clear that two-stage is the optimum number of stages for low phase noise ring oscillator with quadrature output signals. The phase noise of ring oscillator inversely corresponds to the power dissipation and voltage swing. This implies a trade-off between the phase noise and power consumption. Since the phase noise requirement is relaxed in our application, we can decrease the power consumption by relaxing the phase noise appropriately.

By carefully designing the transistor size and loading resistance, the phase noise of the ring oscillator, with minimum tail current, at 4488 MHz is shown in Figure 4.17. Assuming that the 20 MHz loop bandwidth is adopted in the proposed PLL, the

contribution of VCO to the phase noise of PLL is located out-off 20 MHz offset from the carrier. From the Figure 4.17, the phase noise at 1 MHz and 20 MHz offset are equal to -85 dBc and -110 dBc, respectively.

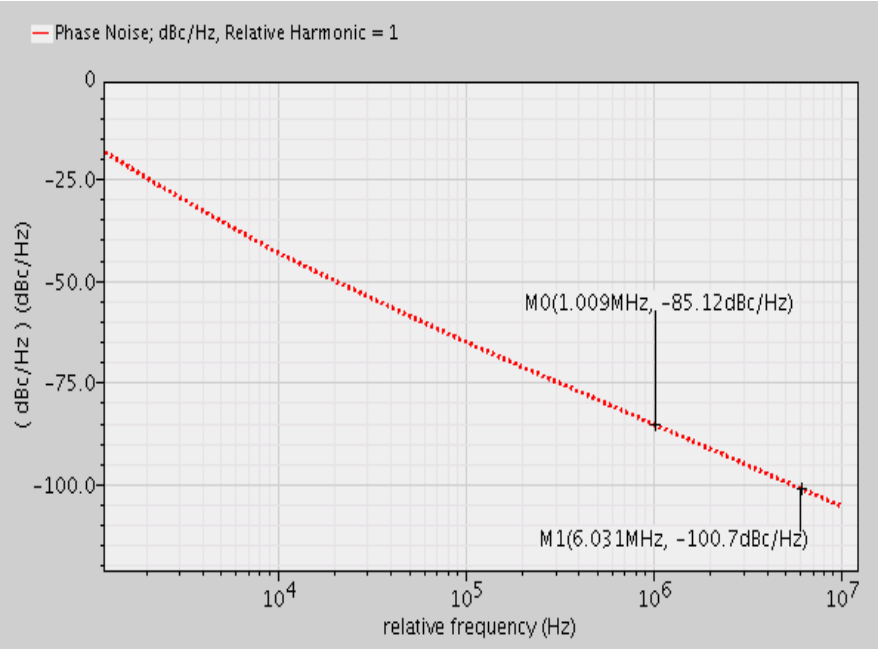

Figure 4.17 phase noise of VCO at 4488 MHz

4.4 The Frequency Divider

4.4.1 Current Mode Logic vs. CMOS Rail-to-Rail Logic

As mentioned in Chapter 3, a pulse swallow frequency divider is employed in the feedback loop of the PLL disclosed in this thesis. Because the prescaler connects to the output of VCO directly, it might need to operate at a frequency as high as 10 GHz for UWB operation. To achieve low power, low delay, low switching noise and good noise immunity, the prescaler is implemented by current mode logics (CML).

CMOS rail-to-rail logic is usually used in digital circuits for the properties of less complexity, high packing density and zero static power consumption. However, the rail-to-rail voltage swing, which leads to large delay time becomes the obstacle to high frequency operation. Conversely, the small voltage swing makes CML a good option for high speed logic circuits. According to [16], the power consumption of the CMOS rail-to-rail logic can be approximated by

$$P = P_{overlap} + P_{dynamic}$$

Where $P_{overlap}$ is mainly caused by static power dissipation, and $P_{dynamic}$ can be obtained by

$$P_{dynamic} = C_L (\Delta V_{swing})^2 f$$

Due to short standby transition for the high frequency operation, the dynamic power dissipation becomes dominant. Thus, above some frequency, the power consumption of CMOS rail-to-rail logic will be larger than that of CML, which dissipates small dynamic power by limiting the output swing.

Because the variation of the supply current occurs at output switching transitions, CMOS rail-to-rail logic generates digital switching noise, known as Vdd bounce. With a constant power supply current, CML can reduce digital switching noise by a factor of 30-300 comparing to CMOS rail-to-rail logic [16] [17]. In addition to the advantages mentioned above, the differential architecture of CML provides great noise immunity and power-supply rejection ratios (PSRR).

The comparison of the some figures of merit among various types of logic is shown in Table 4.1 [11]. From Table 4.1, we can see the bipolar CML (ECL) has the best noise performance and largest maximum speed. Thus, the ECL is adopted to implement the prescaler in the pulse swallow frequency divider.

Table 4.1

Logic Type	Noise Performance	PSRR	Max. Speed	Power at high frequency
CMOS rail-to-rail	Bad	Bad	Moderate	High
CMOS CML	Good	Good	High	Low
Bipolar ECL	Excellent	Good	Very High	Low

4.4.2 Pulse Swallow Frequency Divider Implementation

The architecture of pulse swallow frequency divider is shown in Figure 4.18. As described in Chapter 3, the divide ratio is determined by "PM+S". The frequencies of signals injected by VCO are 3432, 3960 and 4488 MHz. To lock these frequencies with input reference frequency, 264 MHz, the divide ratios should be 13, 15 and 17. Because P must be large than S, 2 and 6 are adopted to be M and P, respectively. Then, we can obtain S = 1, 3 and 5.

D-Flip-Flop (D-FF) is the basic component of the 2/3 dual-modulus divider, the swallow counter, and divide-by-6 programmable counter. Simple divide-by-2 circuit is shown in Figure 4.19 (a). By connecting "Qbar" to the "D" input, the Q output changes its state every circle of the clock. With the combination of two D-FFs, one AND gate and one OR gate, the 2/3 dual-modulus divider can be achieved. When the "Mode Select", in the Figure 4.19 (c), is high, the "B" is high, which makes 2/3 modulus divider become the same circuitry as Figure 4.19 (a). When the "Mode Select" is low, the 2/3 modulus divider works in divide-by-3 mode, like Figure 4.19 (b).

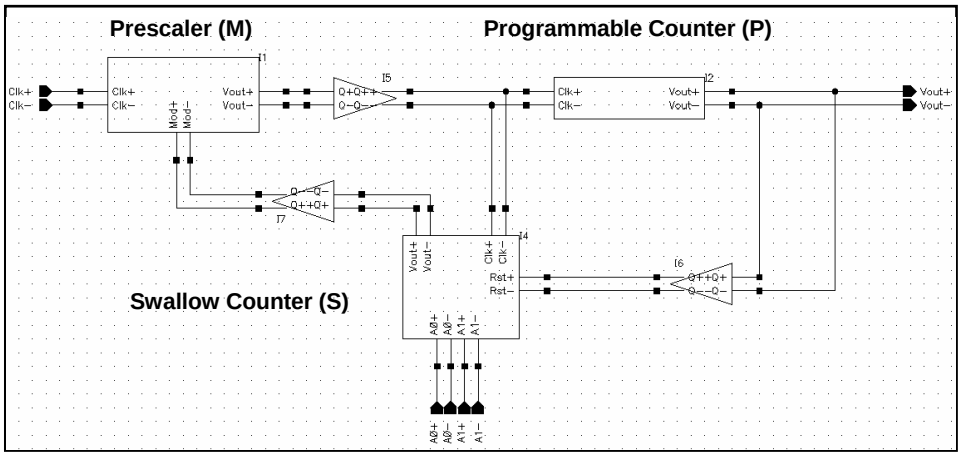

Figure 4.18 Pulse Swallow Frequency Divider

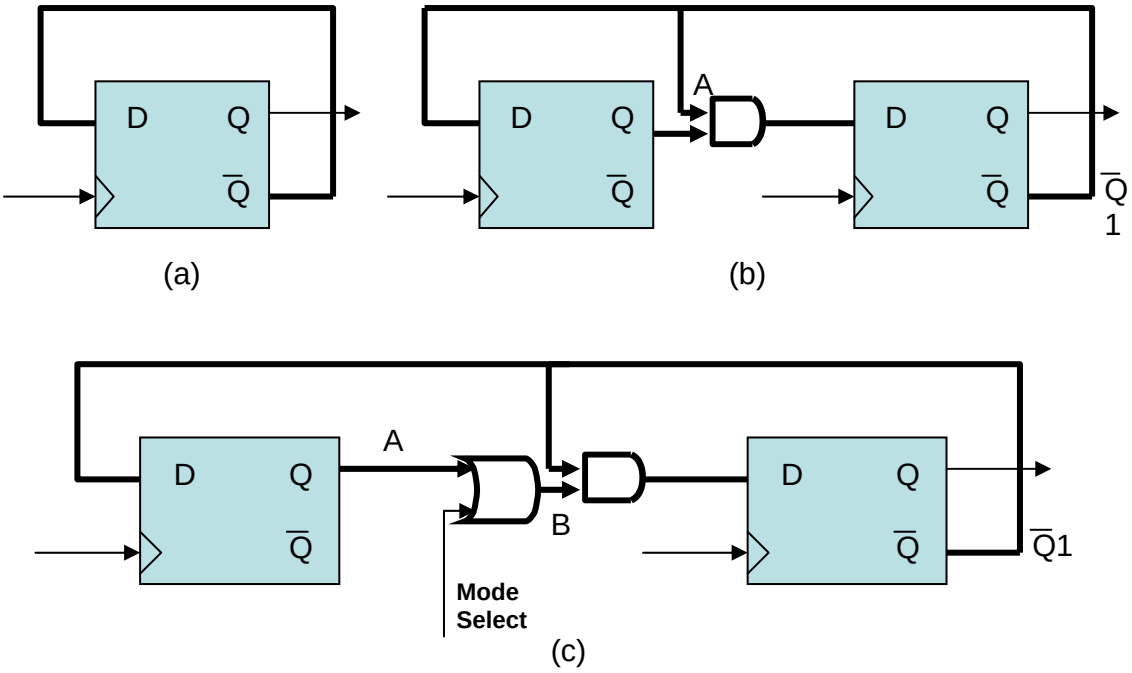

Figure 4.19 (a) divide-by-2 circuit; (b) divide-by-3 circuit

(c) 2/3 dual-modulus divider

The ECL implemented D-FF is shown in Figure 4.20. The MS D-FF composes of two folded D-latch circuits. During the negative phase of clock, the master latch samples the input signals and the slave latch is disabled to keep the D-FF's output constant. At the rising edge of the clock, the master latch is disabled to hold its output value while the slave latch updates D-FF's output at the same time.

Down to the transistor level, there are some considerations should be taken for the ECL implemented D-FF design. First is the supply voltage. As we know, low power consumption is mainly due to low supply voltage. The large base-to-emitter turn-on voltage is an obstacle to the low supply voltage for ECL with many stacks. To reduce supply voltage, NPN current source is replaced by the NMOS current mirrors. By

carefully designing, the overdrive can be as small as 0.2 V, and the supply voltage can be reduced to be 2.5 V.

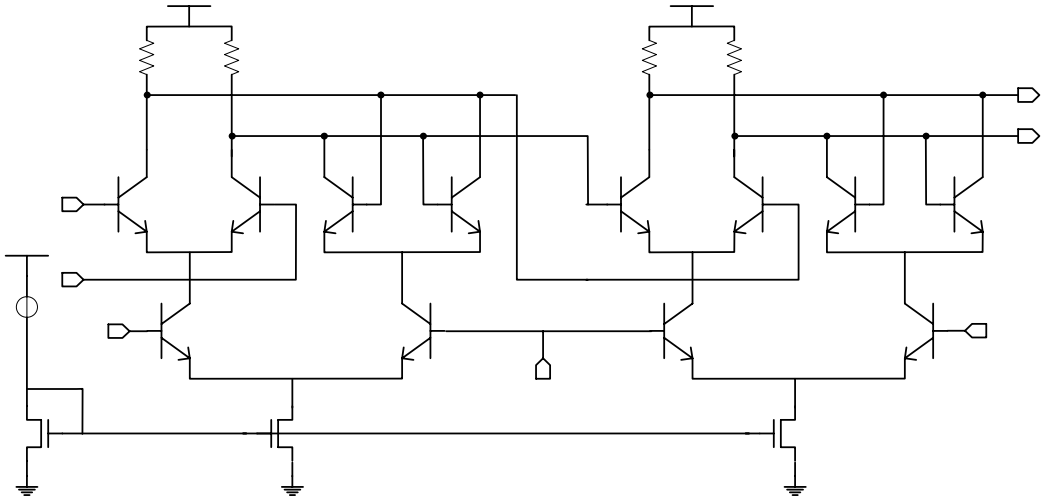

Figure 4.20 ECL D-Flip-Flop with NMOS current source

Small voltage swing is one of the most significant characteristic of ECL. Less voltage swing can lead to lower dynamic power consumption and higher operating frequency. However, there is a limit of the minimum voltage swing. The output swing of the preceding logic should be larger than the fully switching voltage of the next stage. For the bipolar differential pairs, the fully switching voltage is approximately $4V_T$ or larger, where V_T is thermal voltage and known as KT/q. The fully switching voltage of NMOS differential pair is given as [11]

$$V_s = \sqrt{\frac{2I_{EE}}{\mu C_{ox}\frac{W}{L}}}$$

Thus, through designing the transistor size and tail current, we can determine the switching voltage for CMOS CML.

To supply differential voltage to the lower stacks of the EML, the emitter follower is usually used as level shifter. Because of large base-emitter voltage, low supply voltage is not enough to apply appropriate switching voltage to lower differential pairs after level shift.

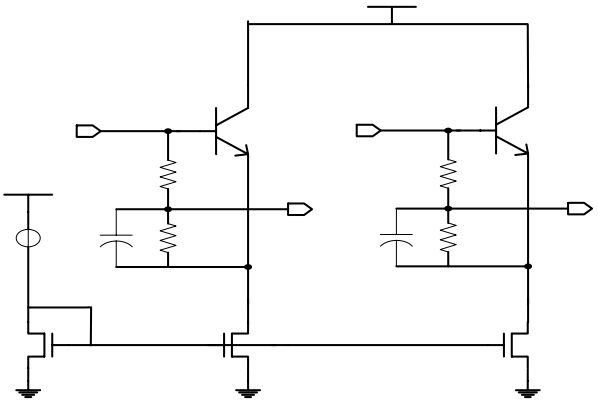

Figure 4.21 Level shifter with resistive voltage divider

To solve this problem, the emitter follower with resistive voltage divider is employed to reduce the voltage shift [18], shown in Figure 4.21.

With the optimized D-FF circuit, the prescaler and divide-by-6 programmable counter can be implemented by the combination of divide-by-2 and divide-by-3 frequency dividers. The swallow counter used in pulse swallow frequency divider is implemented using a synchronous up counter. As illustrated in Figure 4.22, the up counter uses toggle flip-flop (T-FF) to achieve counting. After setting the desired value for swallow counter by the binary input, A0 to A3, the counter starts to count the input clock up to the setting value. Then, modulus control becomes to low and turns prescaler to be divide-by-3 frequency divider. A SR-latch, added between the

swallow counter and prescaler, is needed to keep modulus control at low state until the programmable counter finishes one-period counting [19].

By combining the prescaler, programmable counter, swallow counter and SR-latch together, the pulse swallow frequency is achieved. With the binary setting “1100”, the input frequency is divided by 15 and plotted in Figure 4.23.

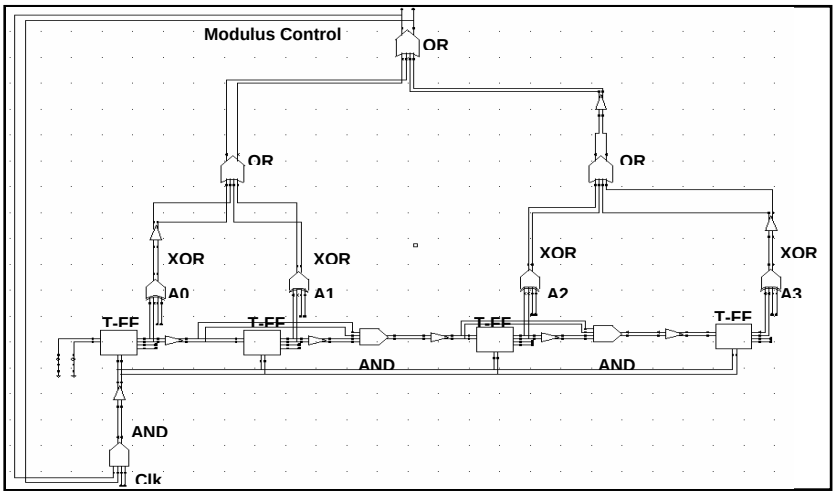

Figure 4.22 Swallow counter used in pulse swallow frequency divider

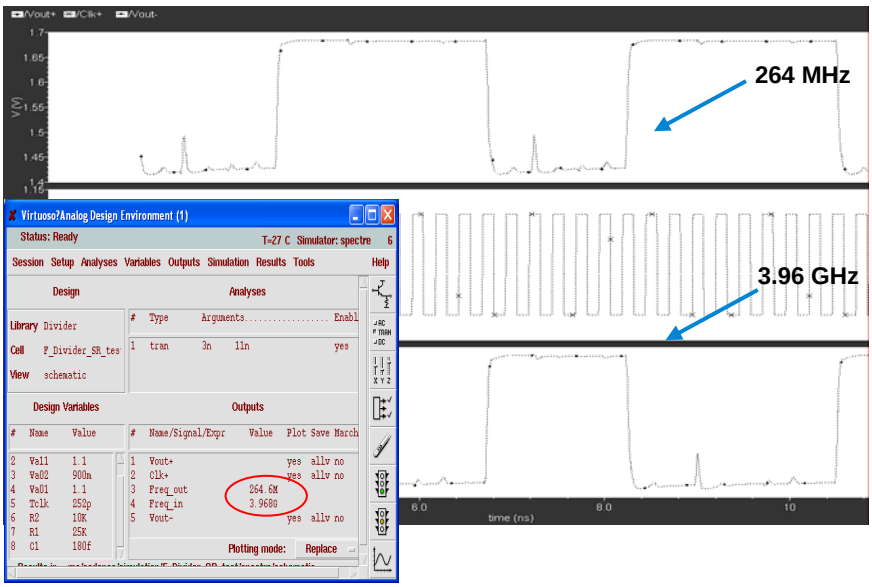

Figure 4.23 output waveform of divide-by-15 pulse swallow frequency divider

4.4.3 Noise performance of Frequency Divider

As is the case with all PFD/CP circuits, the noise sources of the frequency divider include shot noise and flicker noise. By the SpectreRF simulation, the voltage noise spanned from 1 kHz to 10 MHz offset is plotted in the Figure 4.24. As mentioned in the section 4.2.3, the unit of power density of frequency divider's phase noise, $\phi_{FD}{}^2$, is rad^2 / Hz. Due to square like waveform of frequency divider's output signal, the voltage noise should be converted to phase noise by the slew rate. The slew rate is given as

$$Slew\ Rate\left(SR\right) = \frac{\Delta V_{out}}{\Delta t}\left(V / s\right) = \frac{\Delta V_{out}}{\Delta t}\frac{T}{2\pi}\left(V / rad\right)$$

The unit of the voltage noise, in the Figure 4.24, is $V / \sqrt{Hz}$. Dividing the unit of voltage noise by the unit of slew rate, we can get

$$\frac{V}{\sqrt{Hz}} \times \frac{rad}{V} = \frac{rad}{\sqrt{Hz}}$$

This is equal to the square root of the unit of phase noise. Thus, the power density of frequency divider's phase noise can be approximated by

$$\phi_{FD}{}^2 = \left(V_{noise} \times \frac{1}{SR} \times \frac{2\pi}{T} \right)^2$$

The slew rate can be calculated by the simulation output waveform, shown in Figure 4.25. Through Matlab, the phase noise of frequency divider is illustrated in Figure 4.26.

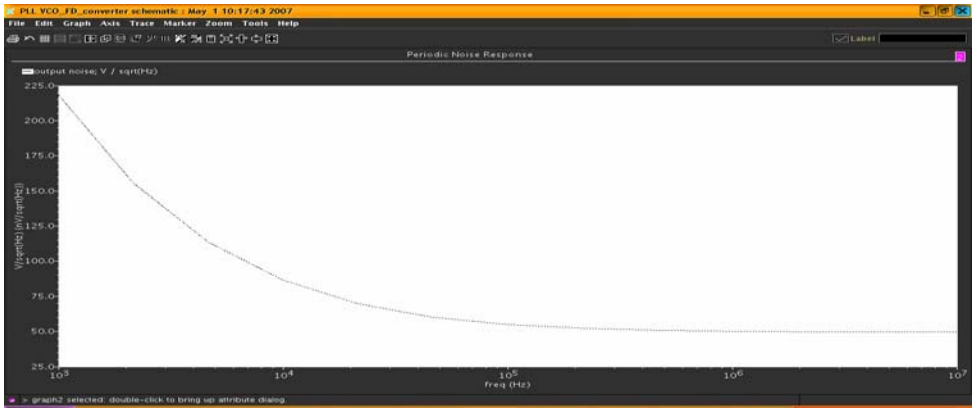

Figure 4.24 Voltage noise of frequency divider

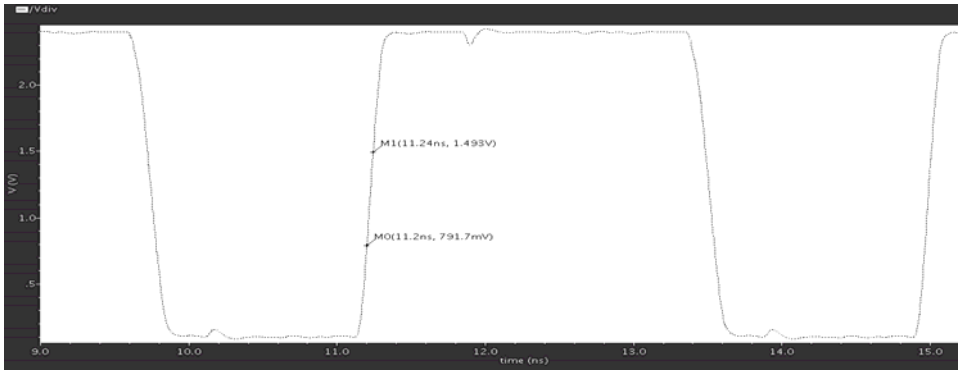

Figure 4.25 output waveform of frequency divider

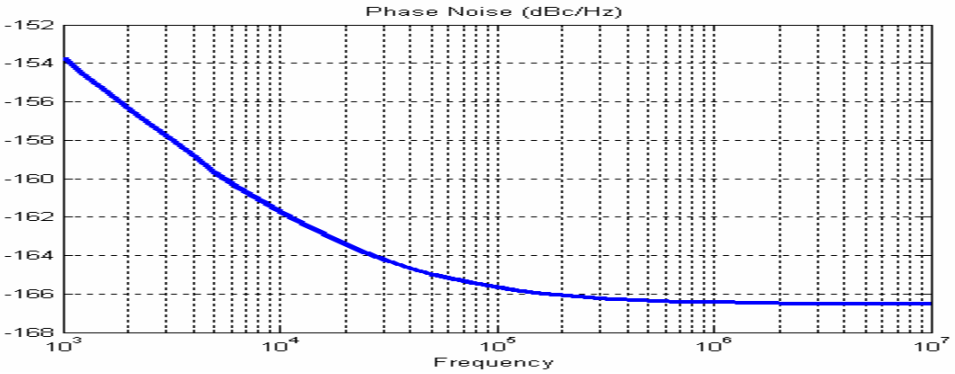

Figure 4.26 Phase noise of frequency divider

4.5 The Loop Filter

Active loop filter is usually used as a voltage buffer when the tuning voltage of the VCO is higher than the voltage charge pump can provide. However, the active components involved in the active loop filter introduce extra noise to the PLL. From the section 4.2, we know the voltage range provided by the designed charge pump is from 0.4 V to 2.3 V, which is wide enough to cover the output frequency range of VCO. Therefore, a second-order passive filter, the highest-order passive filter without series resistors between charge pump and VCO, is adopted to reduce the noise generation.

The loop filter is the most important component in the PLL. It determines the loop's stability, noise performance and settling time. Because the proposed PLL is a third-order system, the concepts of natural frequency and damping factor, which are suitable for second-order system analysis, can't be used to analyze system's stability here. The open-loop bandwidth and phase margin are used to obtain the parameters of loop filter and system's stability. Figure 4.27 shows the second-order passive filter in the PLL. To decide the values of R1, C1 and C2, the open-loop transfer function should be calculated first.

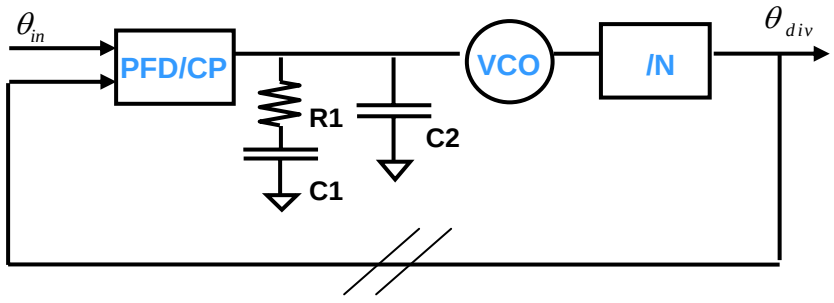

Figure 4.27 second-order passive loop filter in the PLL

From Chapter 3, the open-loop transfer function with second-order filter can be given as

$$G(s) = 2\pi \times \frac{K_{PFD}K_{VCO}}{N} \times \frac{1}{C_1 + C_2} \times \frac{1+\frac{s}{\omega_z}}{s^2(1+\frac{s}{\omega_p})} \qquad (4.11)$$

$$\omega_z = \frac{1}{R_1 C_1}; \quad \omega_p = \frac{1}{R_1}\frac{C_1 + C_2}{C_1 C_2}$$

The phase of the open-loop transfer function, form equation (4.11), is denoted as

$$\varphi(j\omega) = -180^0 + \tan^{-1}(\frac{\omega}{\omega_z}) - \tan^{-1}(\frac{\omega}{\omega_p}) \qquad (4.12)$$

Using the equations (4.11) and (4.12), the system Bode plot is illustrated in Figure 3.14. We re-plot Figure 3.14 in Figure 4.28. The impact of the values of C1 and R1 on system performance can be seen in Figure 4.28. Assuming C2 is much smaller than C1, usually equal to one over tenth of C1, the phase margin increases with the increasing R1 or C1. Conversely, the system becomes more unstable when the value of R1 or C1 decreases. According to [20], large series resistor, R1, not only leads to large ripple in the voltage control line of VCO when loop is locked, but also results in serious phase noise. Thus, increasing series capacitance, C1, is a better way to increase phase margin.

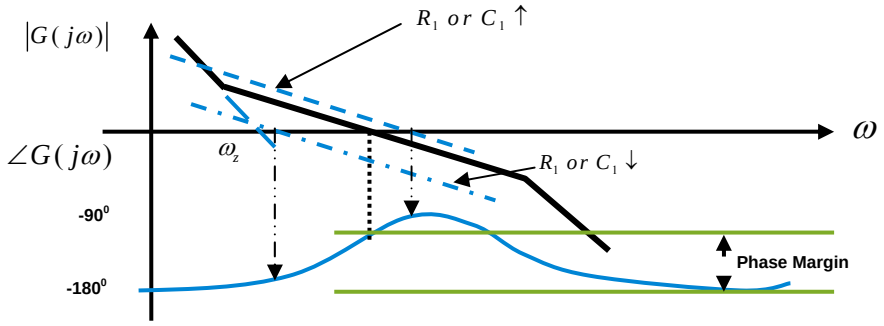

Figure 4.28 Bode plot of open-loop transfer function

By means of setting maximum phase margin at the cross-over frequency, we can decide the parameters of loop filter. The amplitude of the open-loop transfer function at cross-over frequency is equal to one, which can be expressed as

$$\left|G(j\omega_c)\right| = 2\pi \frac{K_{PFD}K_{VCO}}{N} \times \frac{1}{\omega_c{}^2(C_1+C_2)} \times \frac{\sqrt{1+(\omega_c R_1 C_1)^2}}{\sqrt{1+(\frac{\omega_c R_1 C_1 C_2}{C_1+C_2})^2}} = 1 \qquad (4.13)$$

The phase margin at cross-over frequency can be expressed as

$$\phi_M = 180^0 + \arg(G(j\omega_c)) = \tan^{-1}(\omega_c R_1 C_1) - \tan^{-1}(\omega_c \frac{R_1 C_1 C_2}{C_1+C_2}) \qquad (4.14)$$

Because the maximum phase margin located at cross-over frequency, the differentiation of the (4.14) is equal to zero. Through the derivation, we can get

$$\omega_c = \sqrt{\frac{C_1+C_2}{R_1{}^2 C_1{}^2 C_2}} \qquad (4.15)$$

Before substituting the parameters into the equations (4.13) (4.14) (4.15), we need to determine the open-loop bandwidth first.

For the requisite settling time, the open-loop bandwidth can be calculated by [21]

$$f_c = \frac{1}{t_{set}\varsigma_e(\varphi_m)} \ln(\frac{f_{step}}{f_{error}}) \qquad (4.16)$$

In (4.16), t_{set} is the loop settling time, $\varsigma_e(\varphi_m)$ is the effective damping factor according to the phase margin, f_{step} is the frequency jump for one step and f_{error} is the maximum error frequency at loop settling time. In [21], the shortest settling time happens at 50 degree phase margin, corresponding to $\varsigma_e(\varphi_m)$ equal to five. The frequency jump and maximum error frequency are equal to 528 MHz and 1 MHz for our application, respectively. Thus, for 120 ns settling time, the open-loop bandwidth is equal to 12

MHz. For the sake of stability, the input reference frequency should be larger than ten times the open-loop bandwidth, which is satisfied by the reference frequency of 264 MHz.

Finally, by substituting the $K_{PFD}, K_{VCO}, N, \varphi_m$ *and* ω_c into the equations (4.13) (4.14) (4.15), the parameters of loop filter, R1, C1 and C2, can be solved.

Reference

[1] Lawrence E. Larson, "Silicon Technology Tradeoffs for Radio-Frequency/ Mixed-Signal Systems-on-a –Chip," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, March 2003.

[2] D. L. Harame *et al.*, "Semiconductor Technology Choices for Ultrawide-Band (UWB) Systems," *IEEE ICU*, pp. 725-734, Sept. 2005 .

[3] Paul R. Gray *et al.*, *Analysis and Design of Analog Integrated Circuits*, 4th ed., New York: WILEY, 2001.

[4] Marco Racanelli and Paul Kempf, "SiGe BiCMOS Technology for RF Circuit Applications," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, July 2005.

[5] Mozhgan Mansuri, "Fast Frequency Acquisition Phase-Frequency Detectors for GSamples/s Phase-Locked Loops," *IEEE J. Solid-State Circuits*, vol.37, no. 10, Oct. 2002, pp.1331-1334.

[6] Kun-Seok Lee *et al.*, "Phase Frequency Detectors for Fast Frequency Acquisition in Zero-dead-zone CPPLLs for Mobile Communication Systems," *Solid-State Circuits Conference*, Sept. 2003, pp. 525-528.

[7] Sungjoon Kim *et al.*, "A 960-Mb/s/pin Interface for Skew-Tolerant Bus Using Low Jitter PLL," *IEEE J. Solid-State Circuits*, vol. 32, no.5, May. 1997, pp.691-700.

[8] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed., Cambridge: Cambridge University, 2004.

[9] Robert C. Chang and Lung-Chih Kuo, "A New Low-Voltage Charge Pump Circuit for PLL," *IEEE SCAS*, May 2000, pp.701-704.

[10] John G. Maneatis, "Low-Jitter Process Independent PLL and DLL Based on Self-Biased Technology," *IEEE J. Solid-State Circuits*, vol. 31, no.11, Nov. 1996, pp.691-700.

[11] John Rogers *et al.*, *Integrated Circuit Design for High-Speed Frequency Synthesis*, Boston: Artech House, 2006.

[12] Woogeun Rhee, "Design of High-Performance CMOS Charge Pumps in Phase-Locked Loops," *IEEE ISCAS*, vol. 2, July 1999, pp.545-548.

[13] S. Finocchiaro, "Design of Bipolar RF Ring Oscillators," *Proc. ICECS*, vol. 1, pp. 5-8, Sep. 1999.

[14] R. M. Kodkani *et al.*, "A 25 GHz Quadrature Voltage Controlled Ring Oscillator in 0.12 um SiGe HBT," *Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 206, pp.4

[15] Ali Hajimiri, "Jitter and Phase Noise in Ring Oscillators," *IEEE J. Solid-State Circuits*, vol. 34, June 1999, pp. 790-804.

[16] David J. Allstot *et al.*, "Folded Source-Coupled Logic vs. CMOS static Logic for Low-Noise Mixed-Signal ICs," *IEEE Transactions on Circuits and Systems*, vol. 40, no. 9, Sep. 1993, pp. 553-563.

[17] M.W. Allam *et al.*, "Dynamic Current Mode Logic (DyCML), A New Low-Power High-Performance Logic Family," *IEEE Custom Integrated Circuits Conference*, 2000, pp.421-424.

[18] Navid Foroudi *et al.*, "Low-Voltage Low-Power Topology for High-Speed Applications," *IEEE BCTM*, 2001, pp.135-138.

[19] Chin-Sheng Chen *et al.*, "A New Prescaler for Fully Integrated 5-GHz CMOS Frequency Synthesizer," *IEEE ISCAS*, vol.4, May 2004, pp.245-248.

[20] F. M. Gardner *et al.*, "Charge-Pump Phase-Locked Loops," *IEEE Trans. Comm.*, vol.11, Nov. 1980, pp.1849-1858.

[21] Cicero S. Vaucher *et al.*, "An Adaptive PLL Tuning System Architecture Combining High Spectral Purity and Fast Settling Time," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, April 2000.

5

Simulations and Experimental Results For the Frequency Synthesizer

5.1 Introduction

This chapter presents simulations and results for the frequency synthesizer described above. The settling time of the PLL is analyzed by the Cadence Systems Design package with transient response. The linear model behavior of the PLL generated by Advance Design Systems (ADS) is used to compare with the simulation results of Cadence. Then, the reasons leading to the difference between simulation results in transistor level and linear model behavior are described. The frequency responses of PLL are presented to demonstrate the prediction in Chapter 4. The phase noise generated by the building blocks is transferred to the output of PLL, and then combined together to be evaluated. The spurious tones appearing in the spectrum of

desired frequency range are simulated and compared with the specifications derived in the Chapter 2.

5.2 Transient and Loop Frequency Response

5.2.1 Frequency Generation

Since the Zero-IF transceiver is adopted by MB-OFDM UWB systems, the tuning range of frequency synthesizer is set by the operating frequency range of the standard. By fast frequency hopping among carriers, the OFDM signals can be transferred by up to 7.5 GHz bandwidth. For Mode-1 OFDM UWB systems, the operating carriers hop among sub-band 1 to sub-band 3. Thus, the carriers locating at 3432, 3960 and 4488 MHz should be generated accurately by frequency synthesizer. After combining all the building blocks together, shown in Figure 5.1, the frequencies generated at the outputs of VCO by tuning the input signal of frequency divider are plotted in Figure 5.2. By setting the PLL1 to lock at current processing frequency and PLL2 to handle next operating frequency, the fast frequency hopping can be achieved.

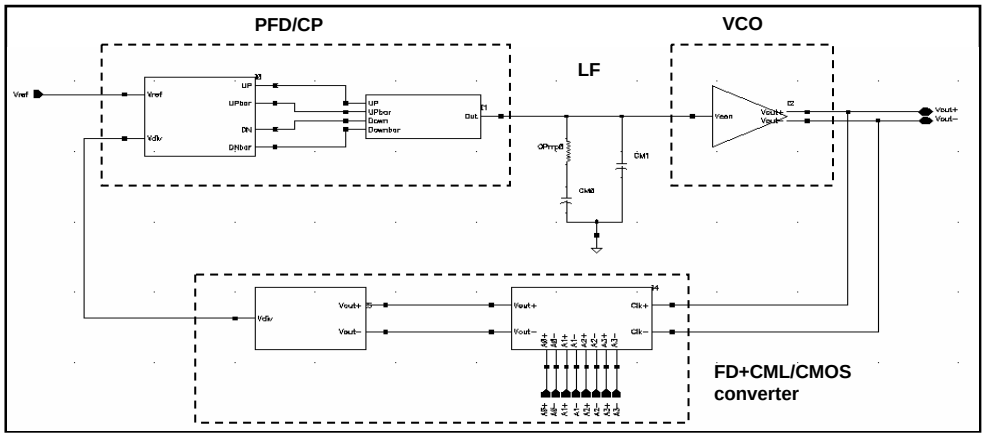

Figure 5.1 The schematic of PLL

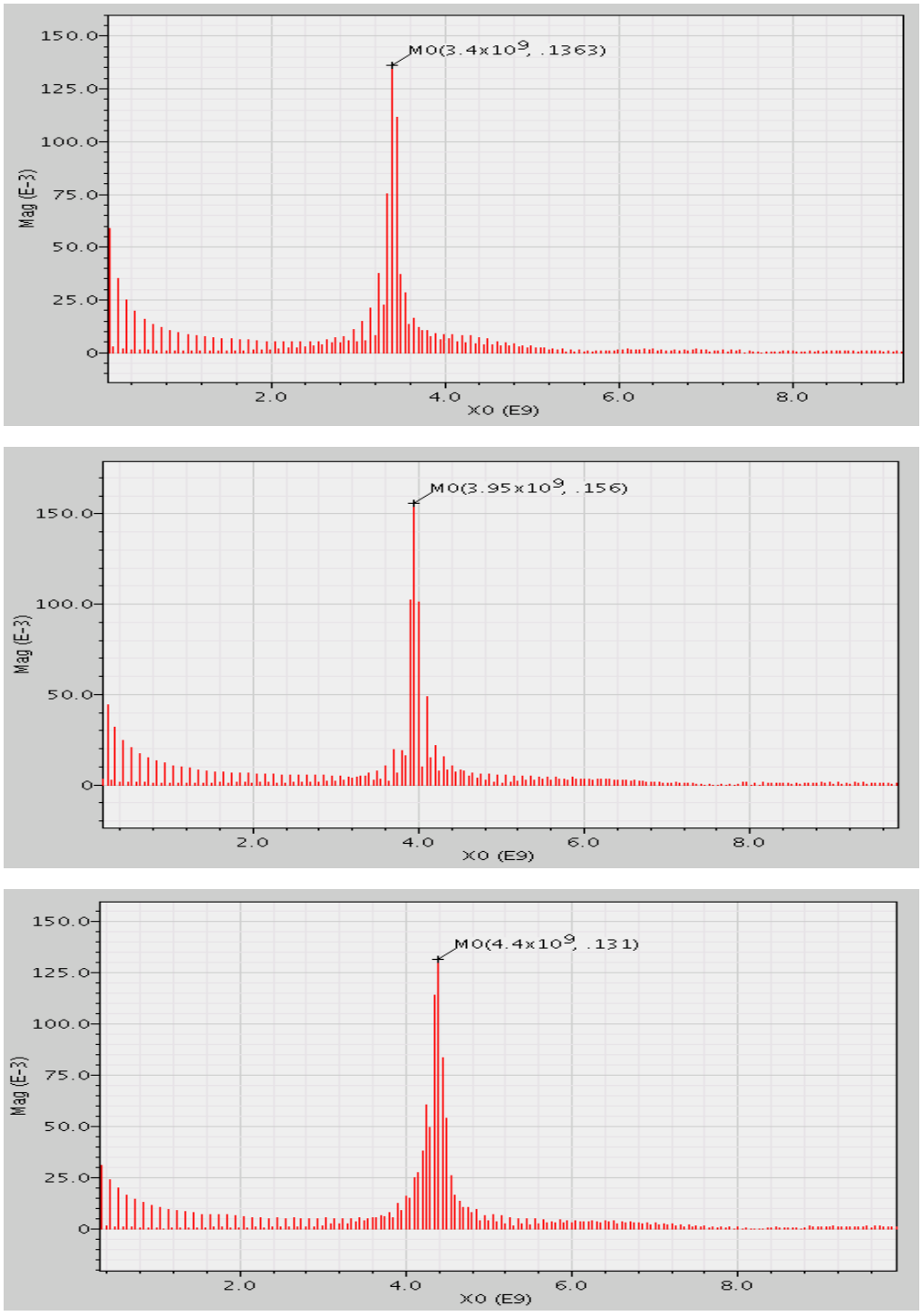

Figure 5.2 Carriers at 3432, 3960 and 4488 MHz generated by frequency synthesizer

5.2.2 Settling Time and Loop Frequency Response

Based on the linear behavior of the PFD/CP, the VCO and frequency divider, the loop frequency response of the PLL relies on the design of the loop filter. To make the system stable, a large phase margin is necessary. However, according to section 4.5, the fastest settling time happens when the system's phase margin is equal to 50 degrees. By substituting the open-loop bandwidth obtained for 120 ns settling time into the formula (4.13) (4.14) (4.15), we can get the parameters, R1, C1 and C2 equal to 5.2 kΩ, 6.75 pF and 1 pF, respectively. The open-loop and close-loop frequency response of the designed PLL are plotted in the Figure 5.3.

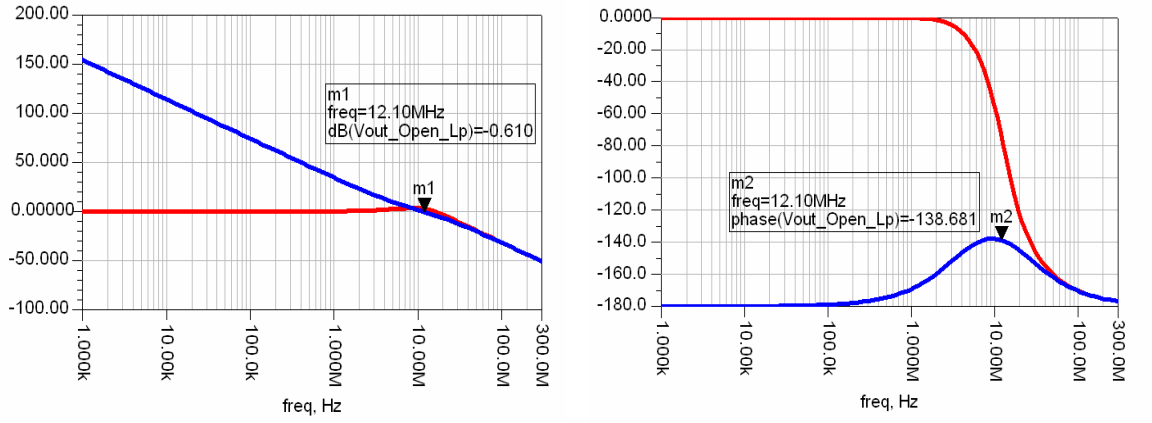

Figure 5.3 Loop frequency response of PLL with large parasitic capacitance

Clearly, the phase margin can be estimated as 41 degree, which makes the system unstable. This is because we achieved a smaller phase margin than predicted due to the parasitic capacitance of the large input device of VCO. Thus, a large phase margin is needed to compensate large parasitic capacitance. To increase the phase margin, we can increase series resistance and capacitance, R1 and C1, in the second-order loop

filter. Since the increasing series resistance will cause serious phase noise at the output of VCO, increasing series capacitance is a better option. Figure 5.4 presents the refined PLL with phase margin equal to 60 degree.

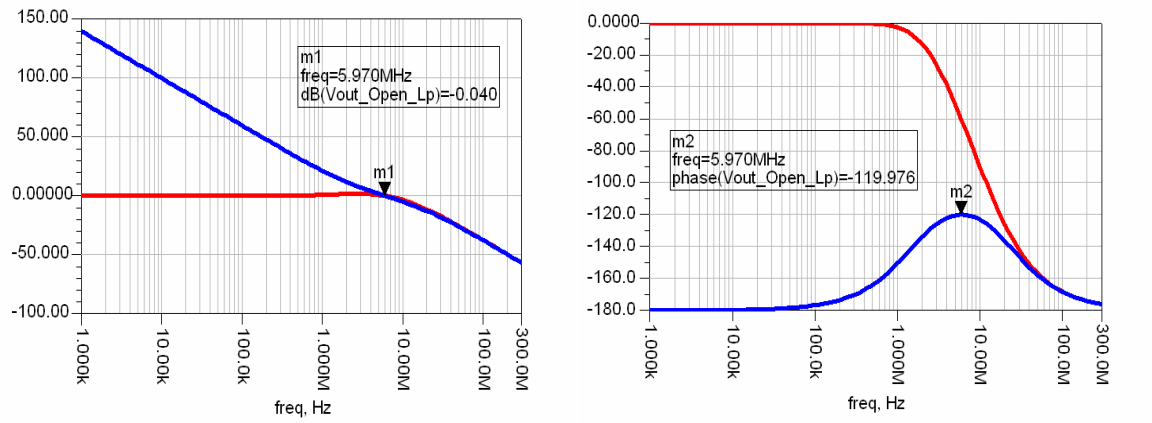

Figure 5.4 Loop frequency response of PLL with 60 degree phase margin

Due to discrete-time PFD/CP operation [1], open-loop bandwidth should be less than the reference frequency over ten to satisfy stable limits of PLL. From the formula (4.16), to obtain 300 ns settling time with 60 degree phase margin, the open-loop bandwidth needs to be 5.97 MHz, which is less than 264/10 MHz. By the linear model built in ADS, the transition response of VCO output frequency displays a settling time equal to 273.5 ns approximately, shown in Figure 5.5. However, the smaller simulation result, made by Cadence, is obtained from the transition response of output frequency and input voltage of VCO, shown in Figure 5.6. The smaller settling time obtained in transistor level than that of linear model is resulted from the large parasitic capacitance of VCO's input and output of charge pump.

According to the simulation results, the settling time of each PLL, 250 ns in Figure 5.6, is less than the OFDM sampling period, 312.5 ns, which implies that the designed frequency synthesizer can satisfy the fast frequency hopping requirement for MB-OFDM UWB systems.

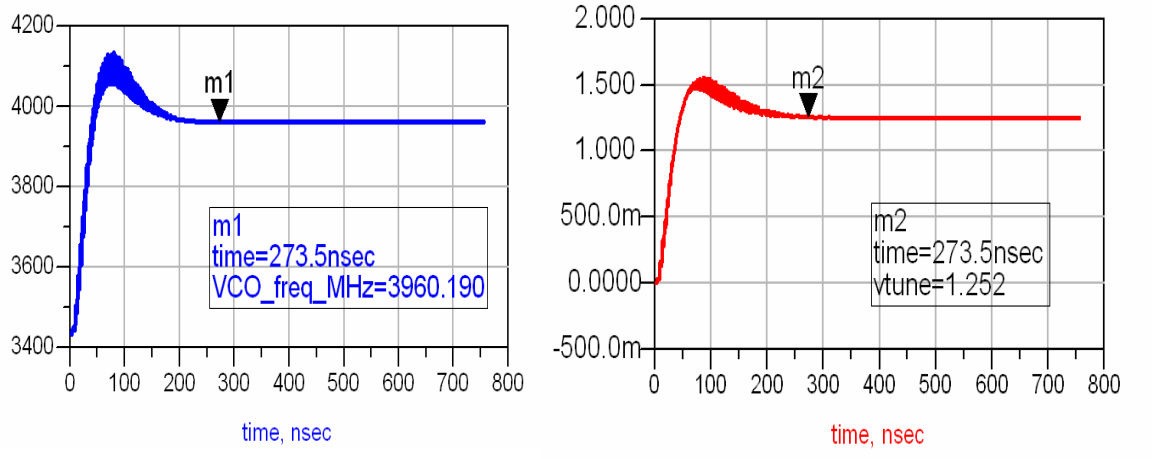

Figure 5.5 Transient response of PLL simulated by ADS

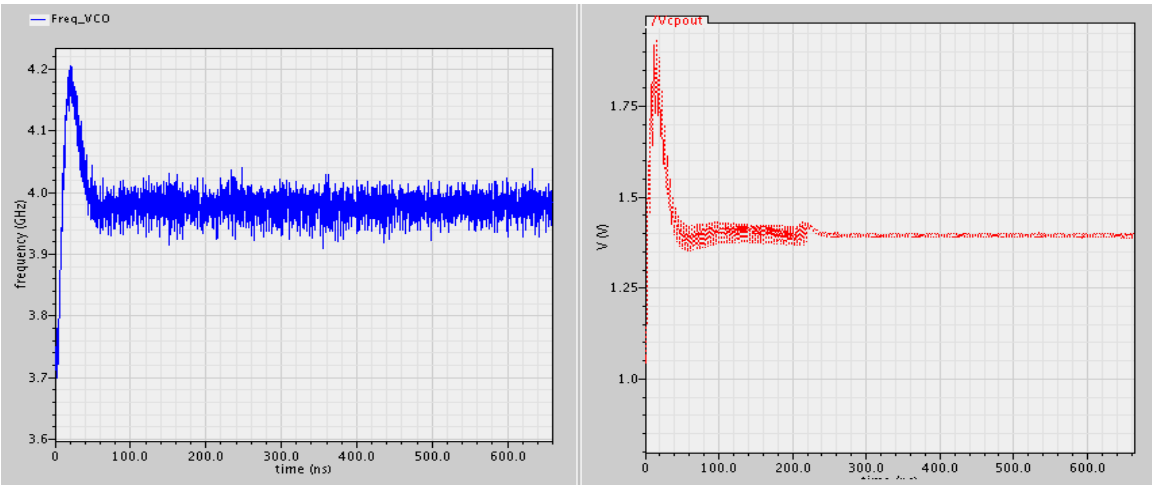

Figure 5.6 Transient response of PLL simulated by Cadence

5.3 Spectral PurityPerformance

5.3.1 Phase Noise

Referring to [1][2], the phase noise of the designed frequency synthesizer is obtained by combining the phase noise contribution of the PFD/CP, the loop filter, the frequency divider and the VCO with the output of PLL using Matlab. However, to improve the output form of the plots, the ADS is used in this thesis. The phase noise of each block is simulated by Cadence and plotted in the Chapter 4. As mentioned in Chapter 3, the noise sources can be divided into two groups: in-band noise dominators and out-of-band noise dominators. By substituting the parameters of the loop filter determined in the Chapter 4 into the transfer functions listed in Chapter 3, the in-band noise of the frequency synthesizer can be obtained by

$$\begin{aligned}\phi_{nin}{}^2 &= N^2 \left|H(j2\pi f_m)\right|^2 (\phi_{PFD/CP}{}^2 + \phi_{FD}{}^2) \\ &= N^2 \left|\frac{G(j2\pi f_m)}{1+G(j2\pi f_m)}\right|^2 (\frac{\Delta I_{noise}{}^2}{K_{PFD/CP}{}^2} + (\frac{V_{noise}}{SR} \times \frac{2\pi}{T})^2)\end{aligned} \tag{5.1}$$

In (5.1), the loop-pass transfer function makes the PFD/CP and frequency divider dominate the in-band noise. Similarly, the out-of-band noise contributed by the VCO can be approximated by

$$\begin{aligned}\phi_{nout}{}^2 &= \left|T(j2\pi f_m)\right|^2 \phi_{VCO}{}^2 \\ &= \left|\frac{1}{1+G(j2\pi f_m)}\right|^2 \phi_{VCO}{}^2\end{aligned} \tag{5.2}$$

Due to the high-pass transfer function shown in (5.2), the out-of-band phase noise is dominated by VCO. Combining the in-band noise and out-of-band noise by ADS, the output phase noise of designed frequency is shown is Figure 5.7.

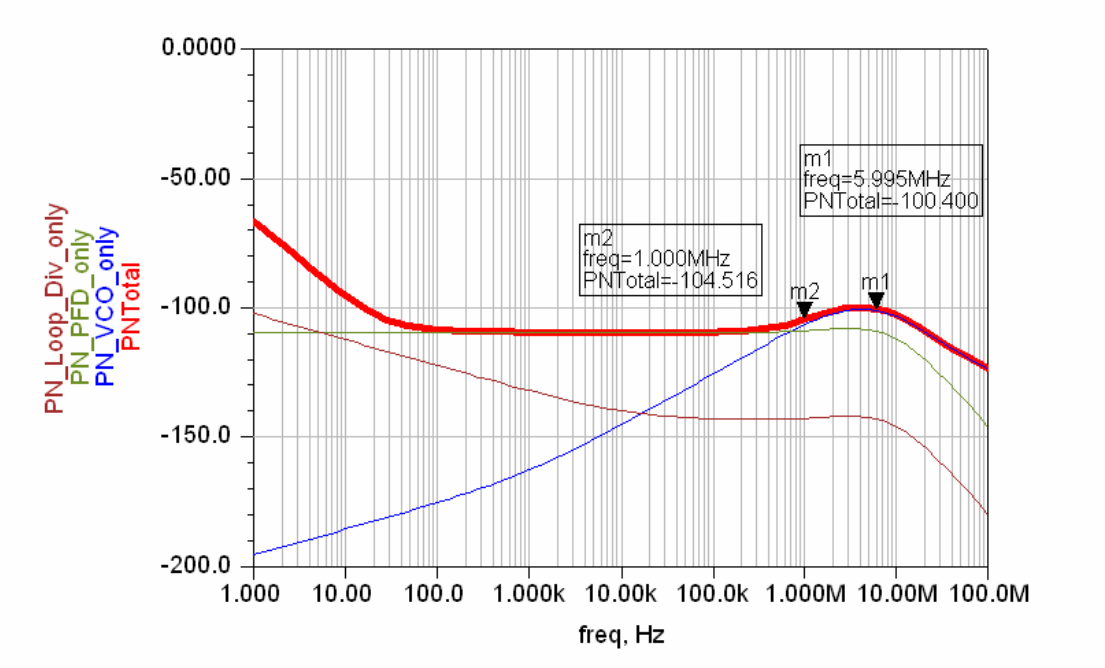

Figure 5.7 Phase noise of frequency synthesizer

Due to large open-loop bandwidth, 5.97 MHz, set in the presented design, phase noise at 1 MHz offset from the carrier locates at in-band area. Thus, the noise contribution from the PFD/CP and frequency divider should be restricted to meet the specifications, while the requirement for the phase noise of VCO is relaxed. From Figure 5.7, we can see the phase noise at 1 MHz offset is equal to -104.516 dBc, which is much smaller than the requirement for the frequency synthesizer of MB-OFDM UWB systems and comparable with other presented literatures.

5.3.2 Spurious Tones Suppression

To co-exist with WiFi, Bluetooth and 802.11a applications, the spurious tones appearing in the spectrum of UWB's frequency synthesizers should be suppressed to some level. According to the derivation in Chapter 2, the spurious tones suppression at 2.4 GHz should be larger than 49.9 dBc and 40 dBc at 5.2 GHz. The Discrete Fourier Transform (DFT) is performed at the output of VCO to display the spectrum of frequency synthesizer. The spurious tones are suppressed to be 50.46 dBc and 42.7 dBc at 2.4 GHz and 5.2 GHz, respectively, as shown in Figure 5.8.

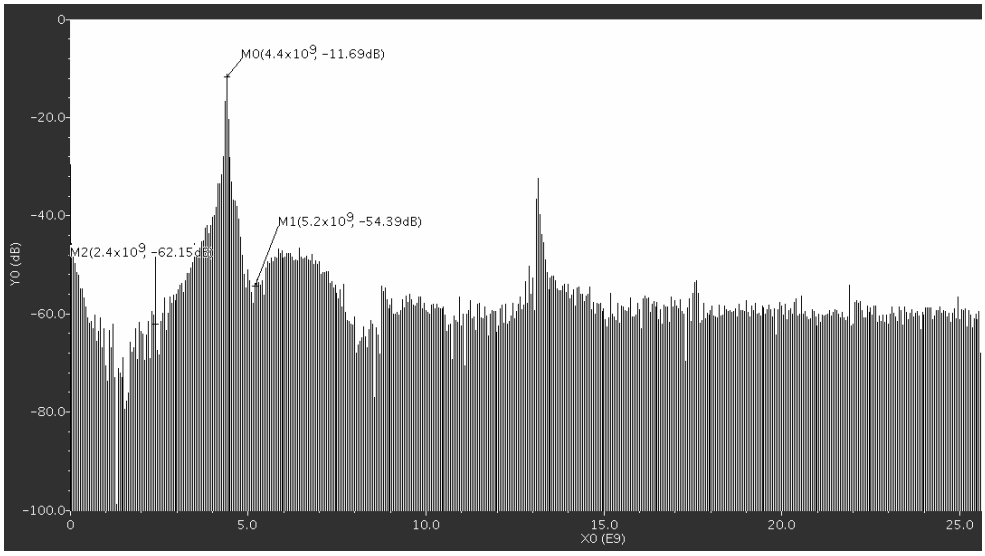

Figure 5.8 Spectrum of designed frequency synthesizer

5.4 Layout

The proposed frequency synthesizer for MB-OFDM UWB system has been implemented in an IBM8HP BiCMOS foundry process. The chip, including two PLLs and one multiplexer, takes 0.16 mm^2 silicon area, 396 × 411 um^2, which saves at least 75 percent die area comparing to other designs in Chapter 1. That is to say, the lowest cost solution for the UWB frequency synthesizer design is provided in this thesis. The layout of frequency synthesizer's core circuit is plotted in Figure 5.9. Figure 5.10 shows the layout of designed circuit with output pins and ESD.

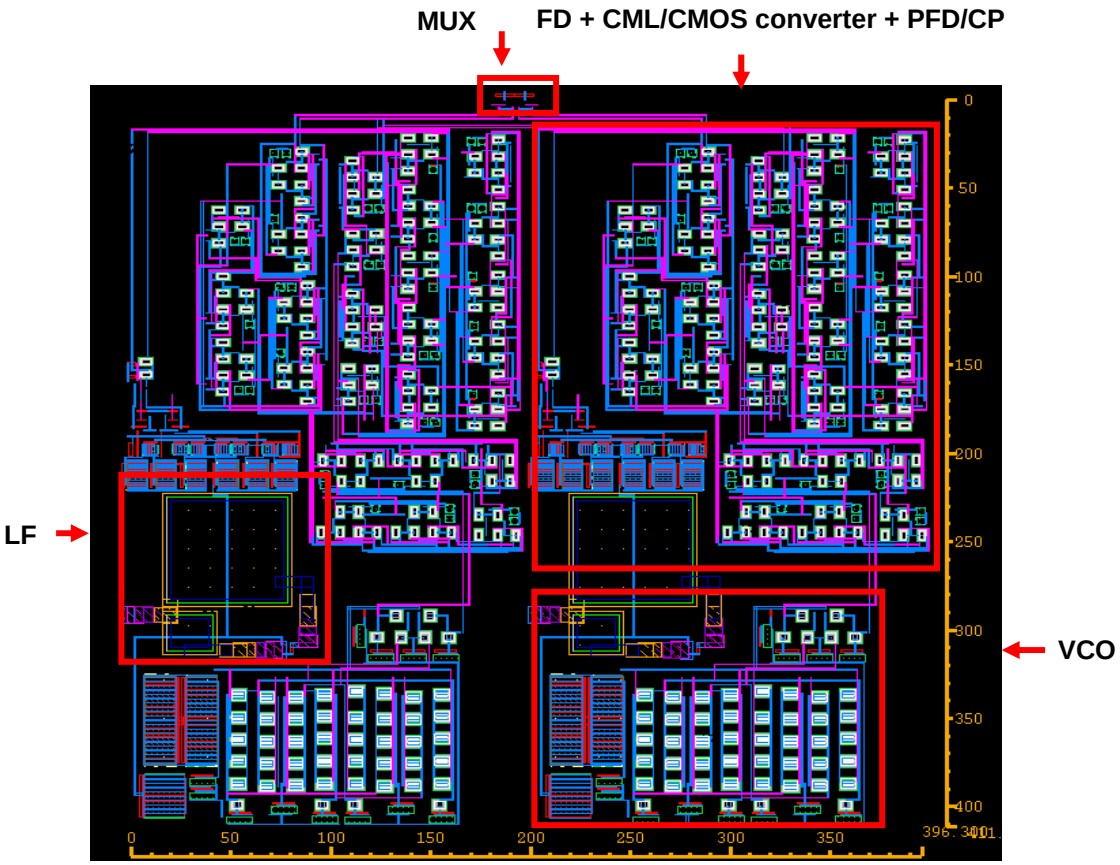

Figure 5.9 Layout of proposed frequency synthesizer

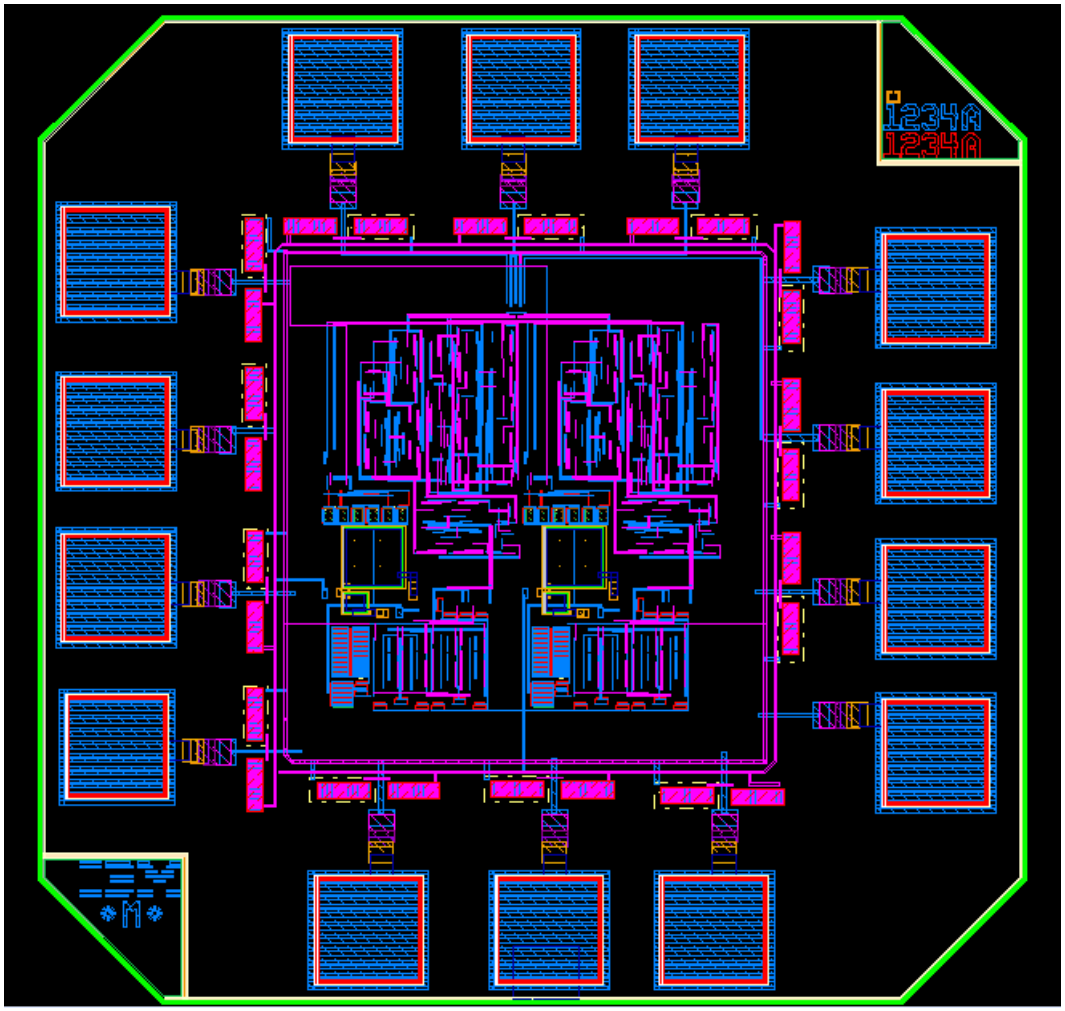

Figure 5.10 Layout of proposed frequency synthesizer with output pins

Reference

[1] Cicero S. Vaucher, *Architectures for RF frequency synthesizers*, Boston: Kluwer Academic Publishers, 2002.

[2] John Rogers *et al.*, *Integrated Circuit Design for High-Speed Frequency Synthesis*, Boston: Artech House, 2006.

6

Conclusion

6.1 Summary of the Work

Due to the characteristics of fast frequency hopping, the frequency synthesizer becomes the largest challenge in the RF front-end design. To obtain the specifications of frequency synthesizer, the scheme, architecture and standards of MB-OFDM UWB transceiver are presented. The basic theory and noise analysis were described to obtain insight into the design issues of frequency synthesizer. To satisfy specifications derived from the standards in system level, the novel structures and simulation methodology are developed to implement building blocks and optimize system's performance.

Providing the smallest die area and great noise performance of frequency synthesizer to the MB-OFDM UWB systems is the main contribution of this work. The concept of making a frequency synthesizer involved two PLLs with ring oscillators and one multiplexer not only saves die area, but also performs better in

terms of spectral purity comparing to other architectures. The simulation results for main specifications of the frequency synthesizer are listed in table 6-1.

Table 6-1

Parameters	Results
Frequency (MHz)	3432, 3960, 4488
Settling Time (ns)	~ 250 (for PLL) < 9.5 (for frequency generator)
Phase Noise (dBc/Hz)	104.516 @ 1 MHz offset
Spurious Tones Suppression (dBc)	50.46 @ 2.4 GHz 42.7 @ 5.2 GHz
Power Consumption (mW)	62.5

6.2 Future Work

For the MB-OFDM UWB application, five frequency groups including 14 sub-bands can be utilized. In this thesis, we place emphasis on Mode-1 OFDM operation, which includes only three sub-bands. With the proposed synthesizer architecture, we can extend operation frequency range, without adding any other component, to cover all 14 sub-bands by simply increasing the output frequency range of VCO. Therefore, a frequency synthesizer operating within whole 7.5 GHz bandwidth can be implemented successfully.